And scaling goes on… Technology Challenges & Opportunities

Presentation to the 2007 EMEA Academic Forum

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12th EMEA Academic Forum

EMEA ACADEMIC FORUM

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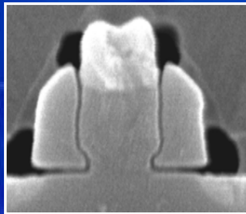
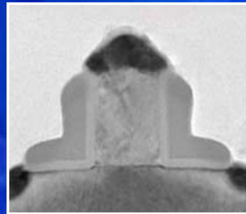
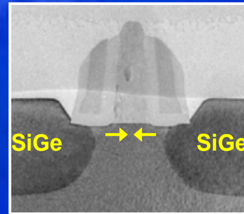
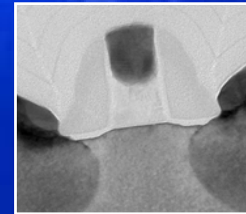
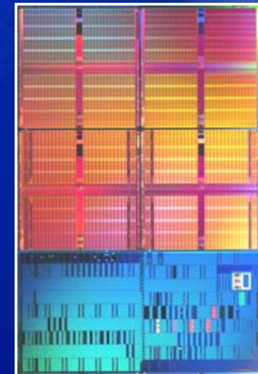
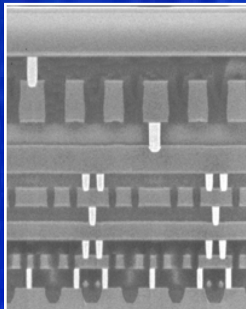
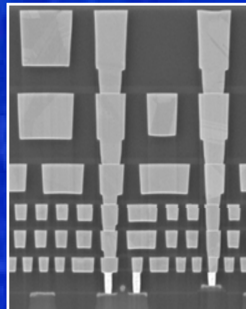
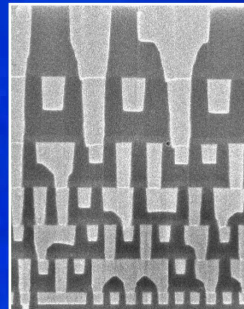
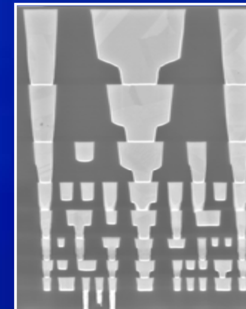
Key Messages

- **Technology scaling continues according to Moore's Law**
  - 2X increase in functionality every 2 years
  - Multicore, integrated functionality or both
  - 65nm in 2005, 45nm 2007, 32nm 2009
- **High rate of innovation is critical to future success**
  - Many new device types and materials
  - A challenge as well as an opportunity
- **Close collaboration with Universities is a key component of a successful Intel strategy**
  - Highly capable universities with outstanding research professors
  - Outstanding students

Technology scaling on a 2 Year Cycle

	180 nm 1999	130 nm 2001	90 nm 2003	65 nm 2005	45 nm 2007
Transistor			 		
Interconnect					
	200mm 100nm L_G $CoSi_2$ 6 Al SiOF	300mm 70nm L_G $CoSi_2$ 6 Cu SiOF	300mm 50nm L_G NiSi Strain Si 7 Cu Low-k	300mm 35nm L_G NiSi 2nd Strain 8 Cu Low-k	Details Coming!

Courtesy: Intel

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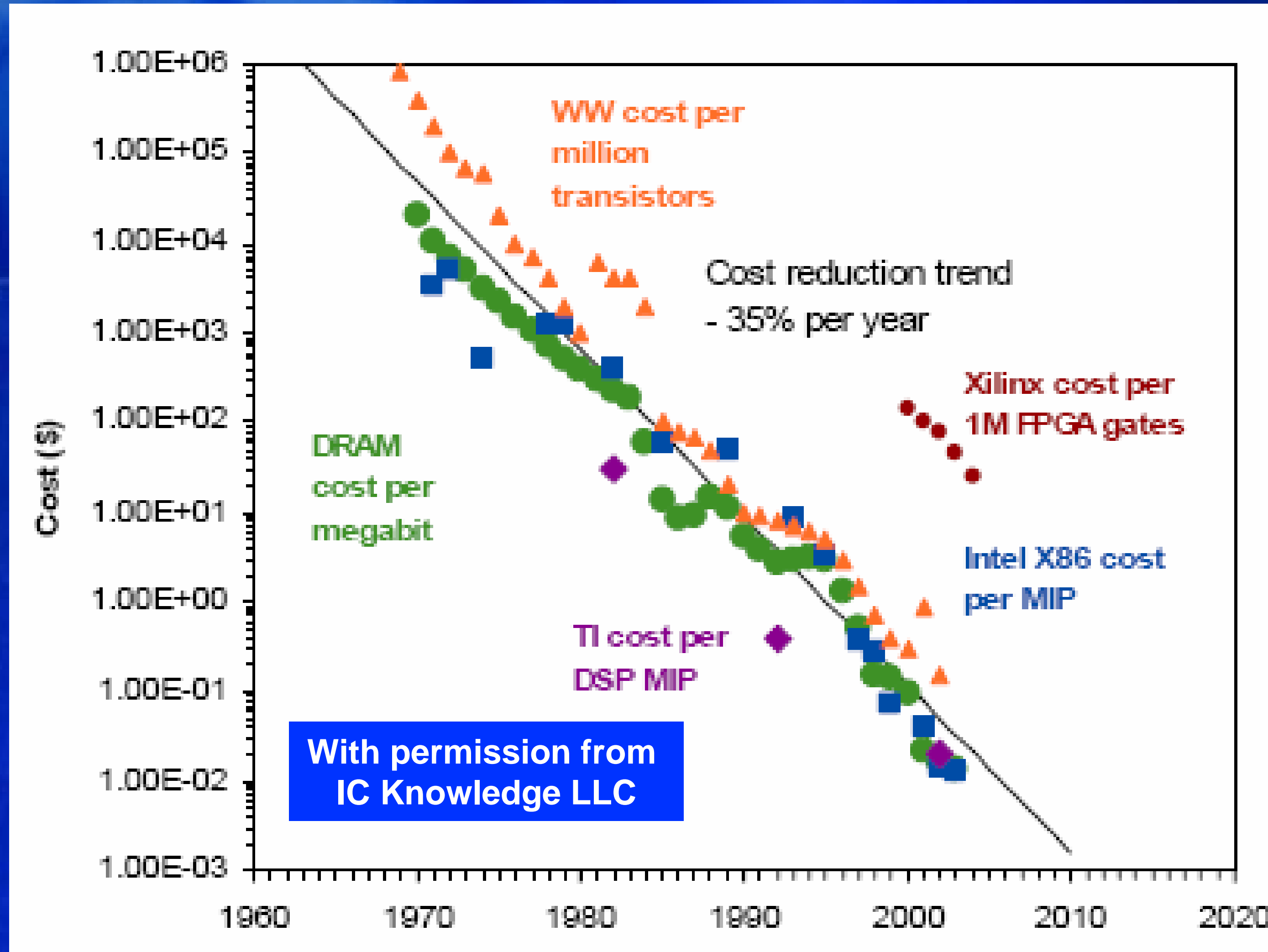
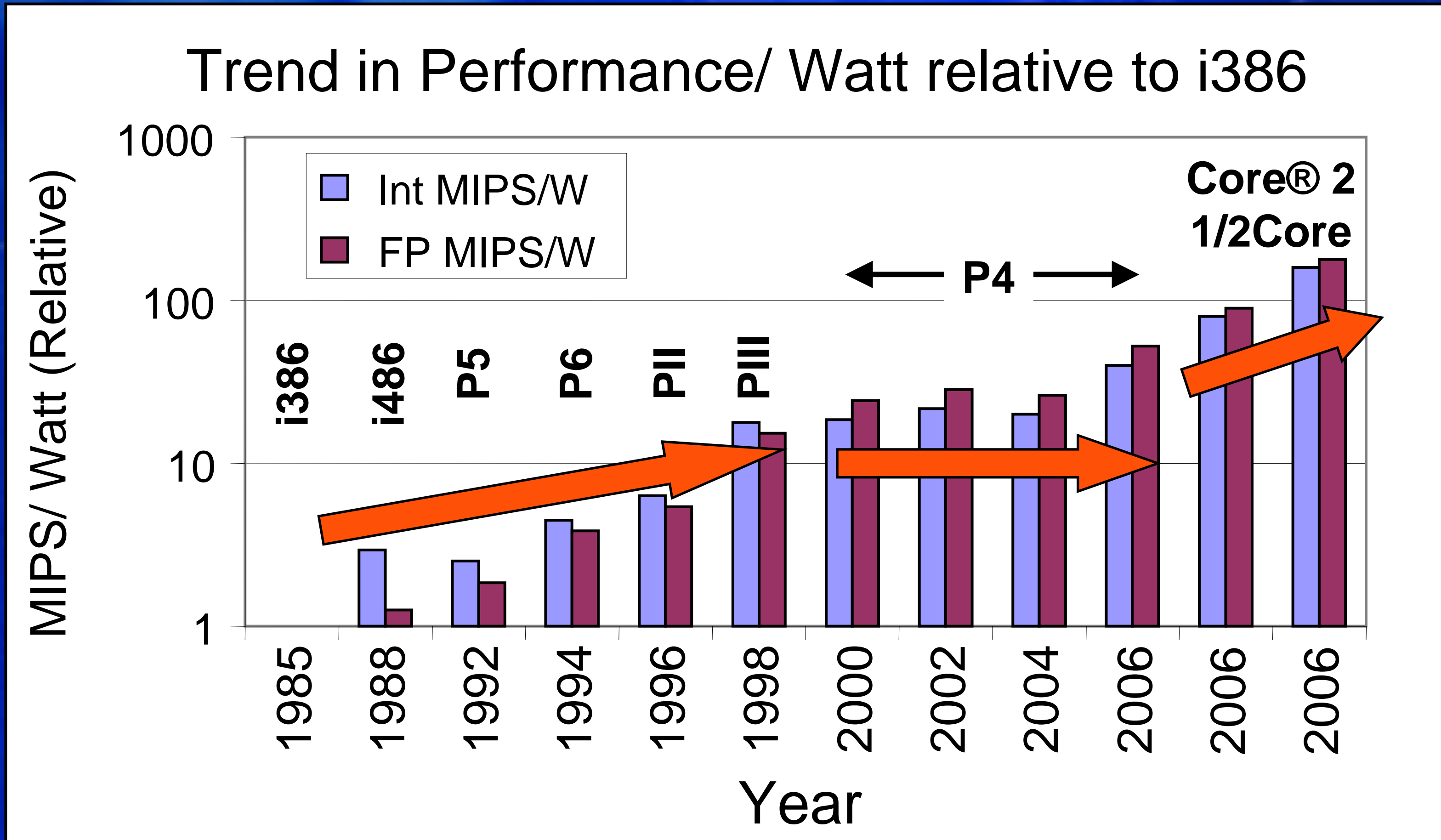
Moore's Law Delivers Value to the End User



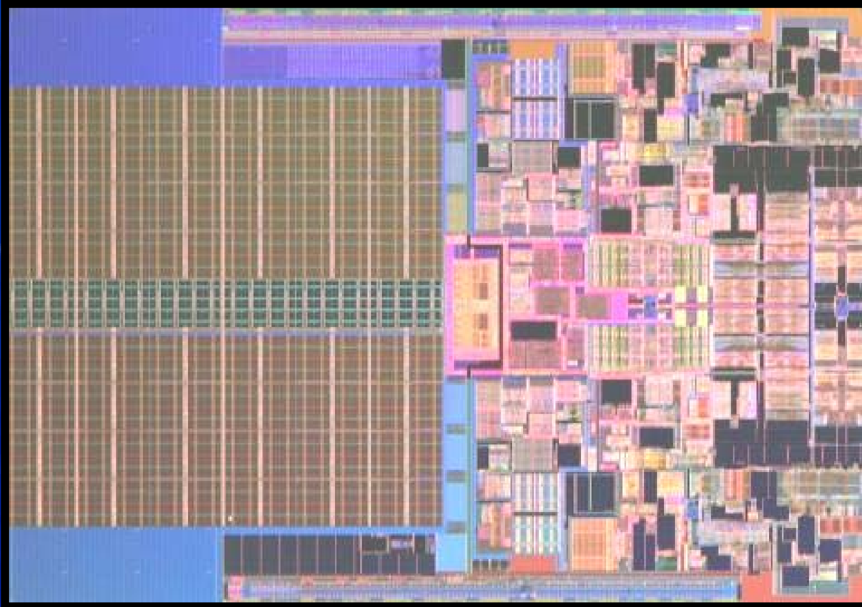
Twice the functionality at the same cost every 2 years

Performance/ Watt



Performance/ watt improvement for both integer and Floating point

Lead in 45nm Technology and Products

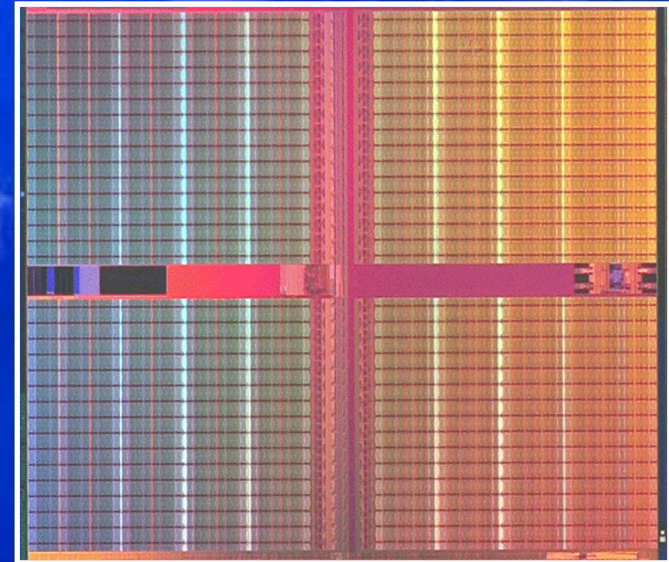


Intel® Penryn

Core™2 family processor

410/820 M transistors (2C/4C)

World's first working 45 nm CPU



153 Mbit SRAM

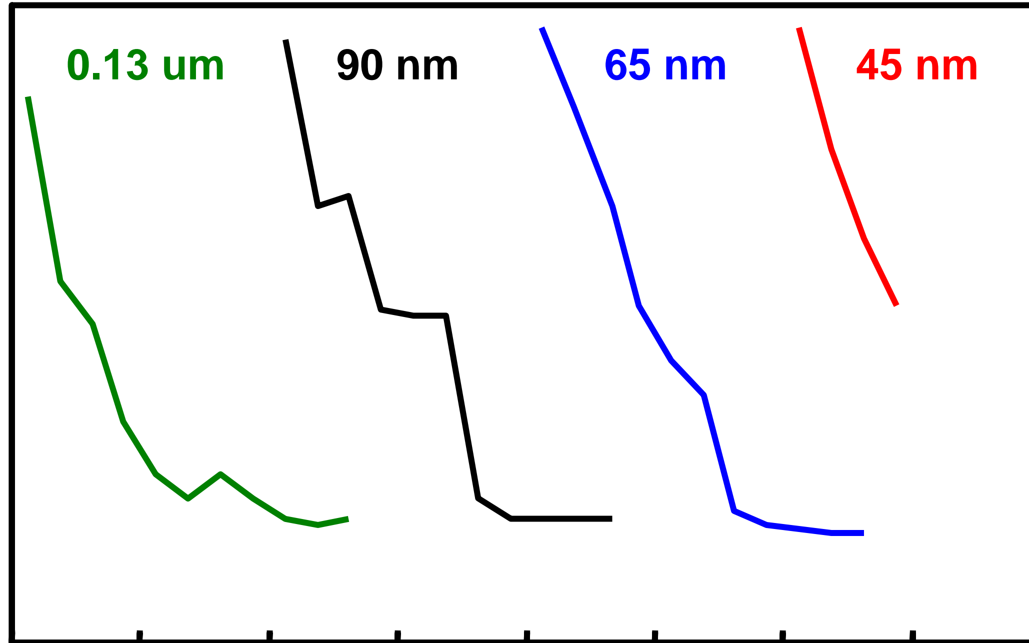
0.346 μm^2 cell

119 mm2 chip size

>1B transistors

Functional in Jan 2006

45 nm Yield Improvement Trend



Excellent Yield learning and good reliability too

On track for production ramp in 2H '07

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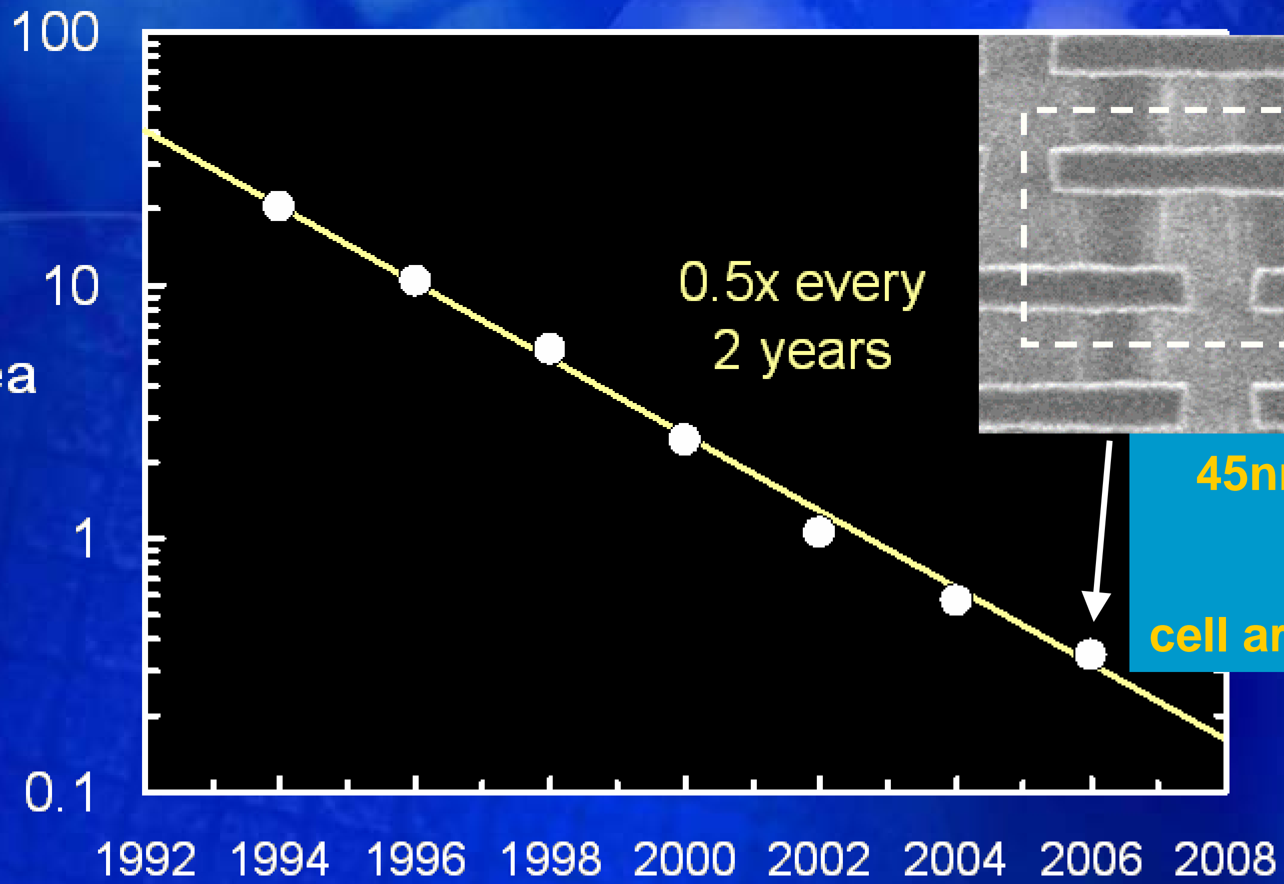
SRAM Cell Size Trend



45nm 6-transistor

SRAM

cell area of 0.346 mm2

M. Bohr

Intel

The trend continues

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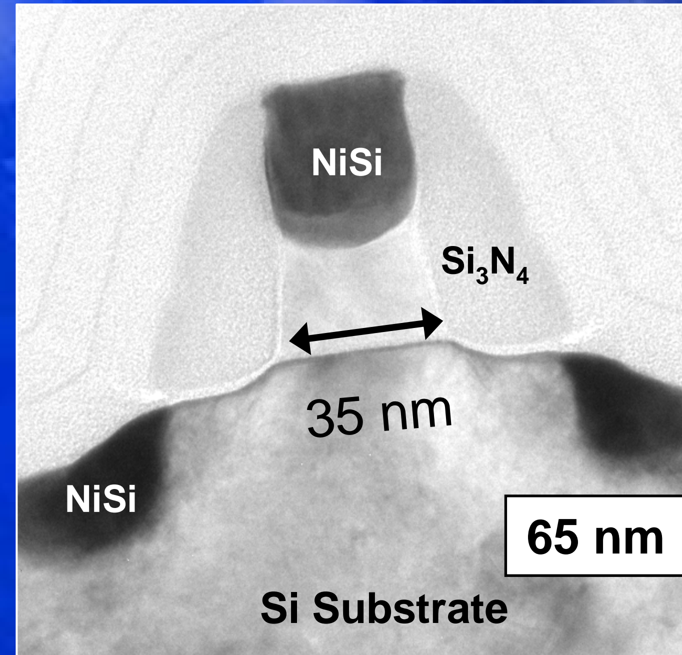
At the core of it is the transistor

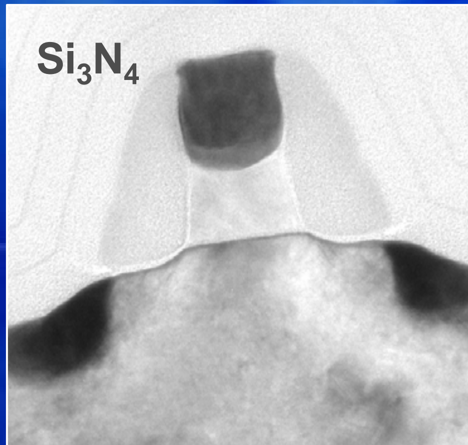
- 35 nm gate length
- 220 nm gate pitch
- 1.2 nm gate oxide
- NiSi for low resistance
- 2ND generation strained silicon



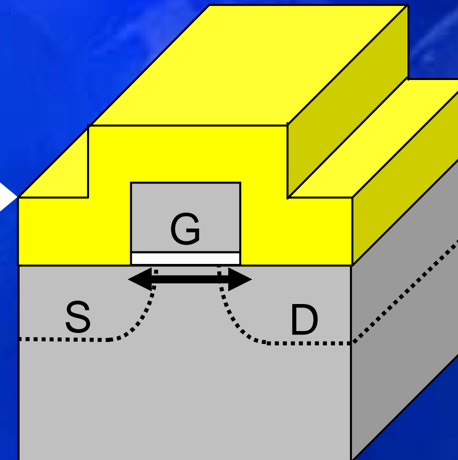
Leading edge transistor technology is unmatched by our competitors

Strained Silicon Transistors

NMOS

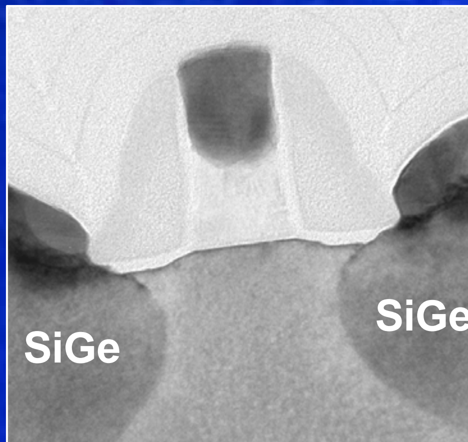


Si_3N_4 Cap Layer

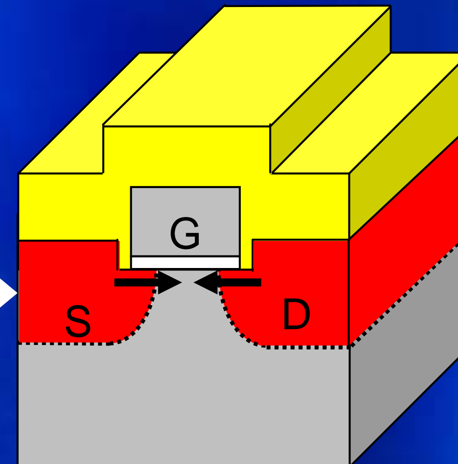


Uni-axial Tensile Strain

PMOS



SiGe Source-Drain



Uni-axial Compressive Strain

Intel's unique strained silicon technology increases transistor drive current by an average of >30%

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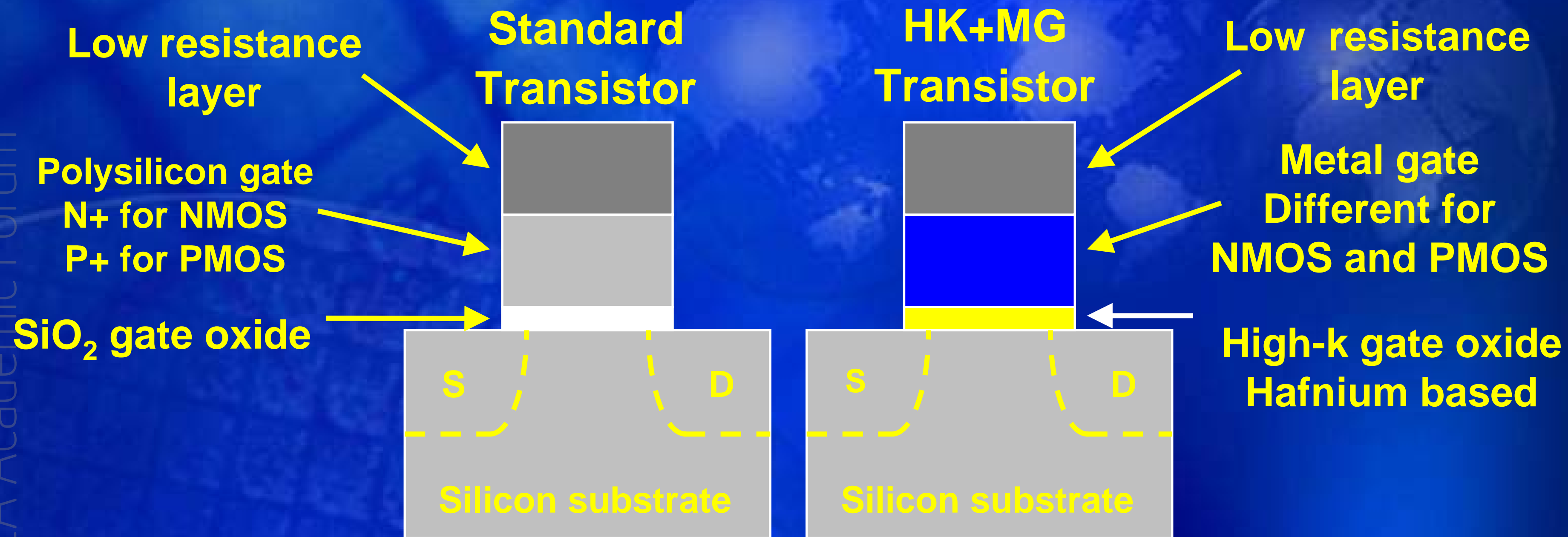
High-k + Metal Gate Transistors



Higher performance + lower leakage

"The implementation of high-k and metal materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s."

Gordon Moore, Intel co-founder

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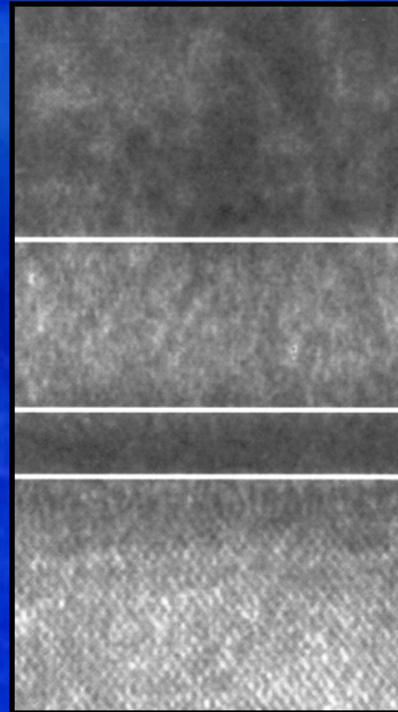
High-k + Metal Gate Transistors

- ✓ Integrated 45 nm CMOS process
- ✓ High performance
- ✓ Low leakage
- ✓ Meets reliability requirements
- ✓ Manufacturable in high volume



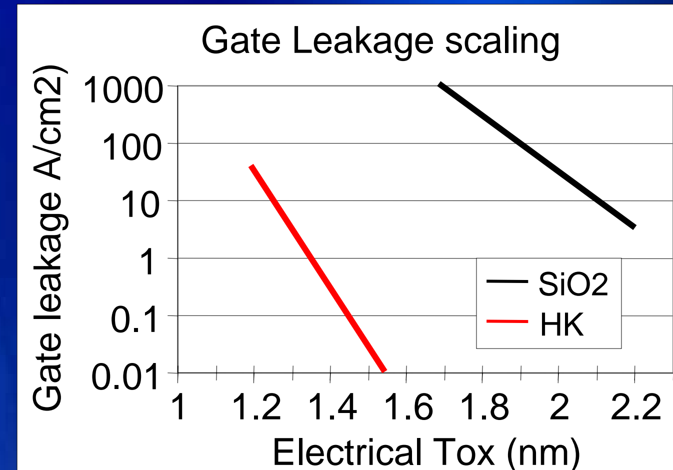
Low Resistance Layer

Work Function Metal
Different for NMOS and PMOS

High-k Dielectric
Hafnium based

Silicon Substrate

	High-k vs. SiO_2	Benefit
Capacitance	60% greater	*Faster transistors*
Gate Leakage	>100x reduction	*Cooler chips*



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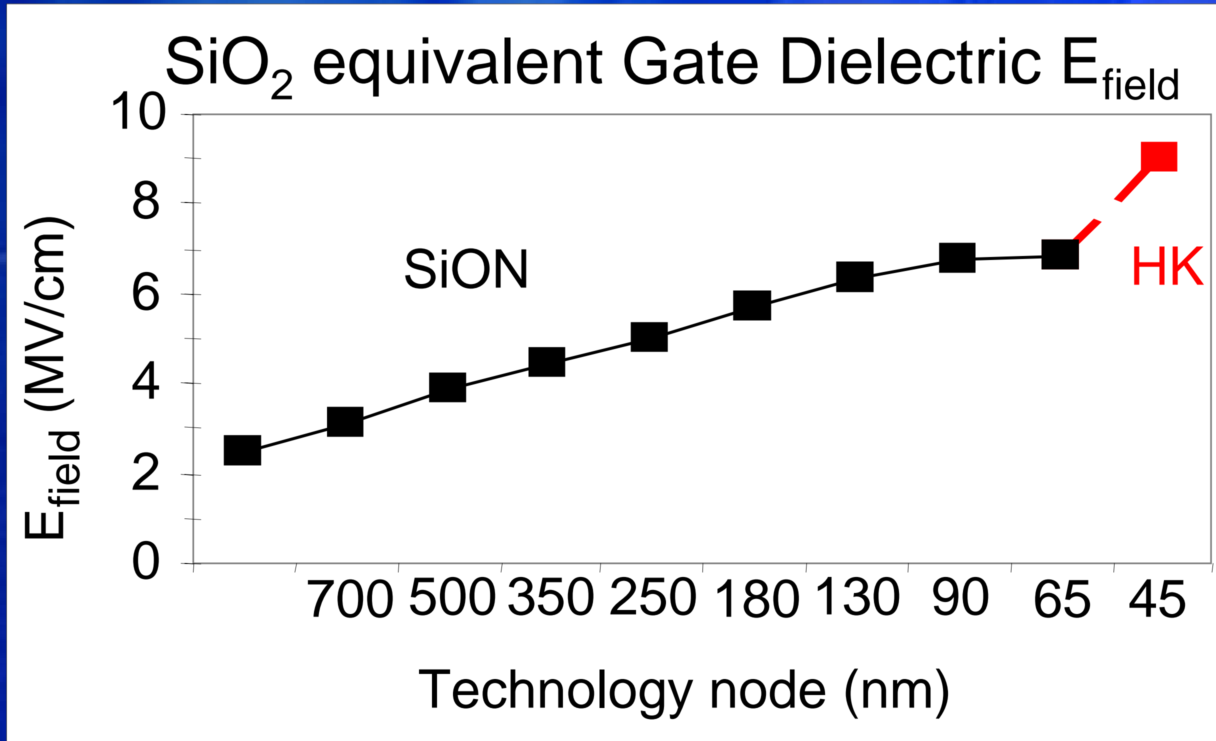
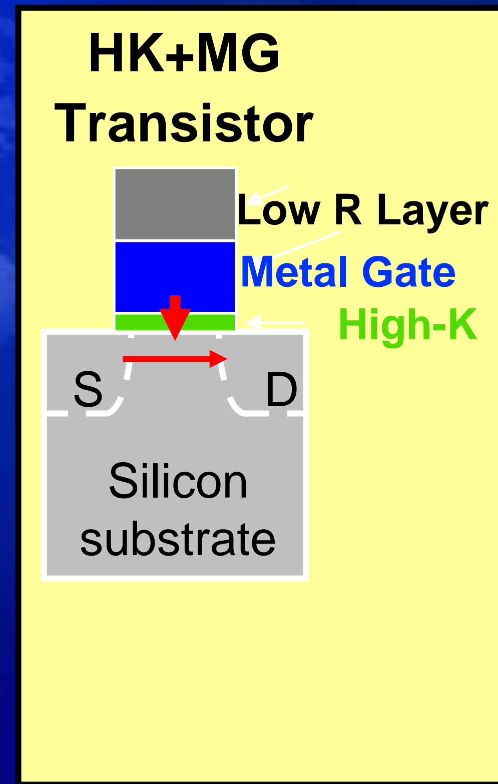
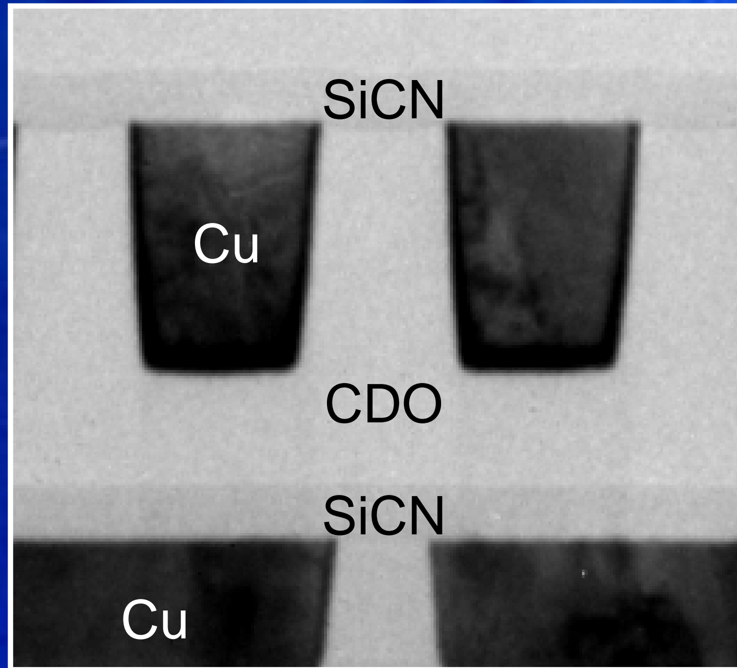
Gate Dielectric Field Trend

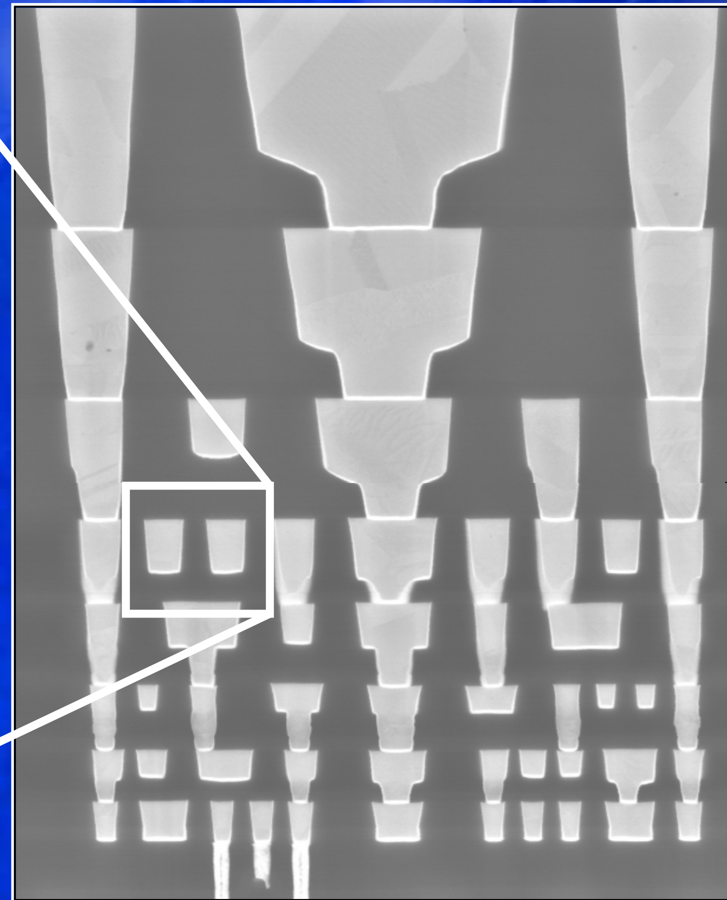




Substantial increases in E_{field} enabled by HK/MG

65 nm Generation Interconnects





Simple 2 layer dielectric stack for low capacitance and low cost

45nm Development/ 65 nm High Volume Manufacturing

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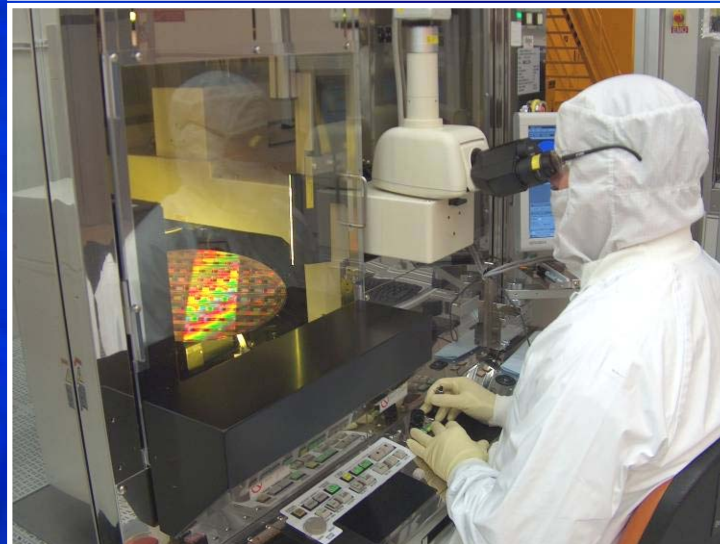
45 nm development
- D1D in Oregon
- 176,000 sq feet clean room
- ~3.5 football fields

65 nm high volume fabs
- D1D in Oregon
- F12 in Arizona
- F24 in Ireland
- D1C in Oregon

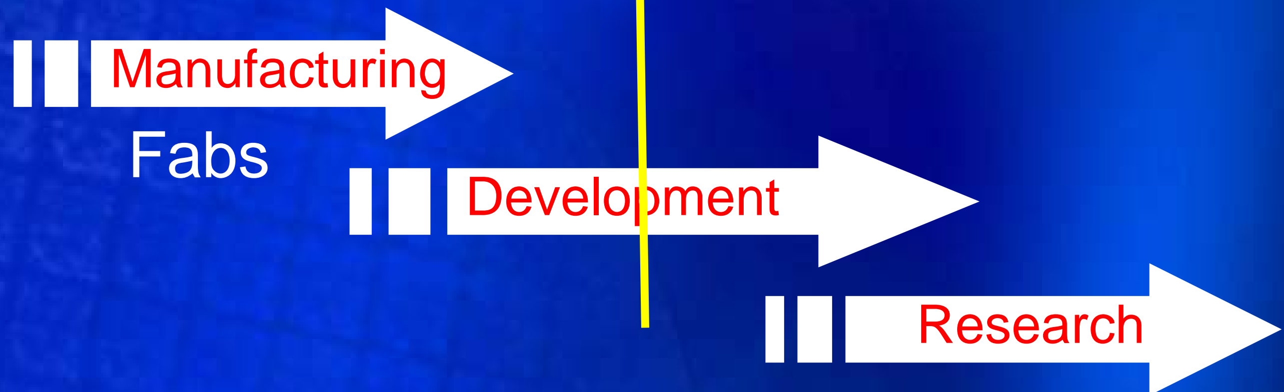
All 300 mm



Logic Technology Evolution

Today

Process Name	P1262	P1264	P1266	P1268	P1270
1st Production	2003	2005	2007	2009	2011
Lithography	90 nm	65 nm	45 nm	32 nm	22 nm



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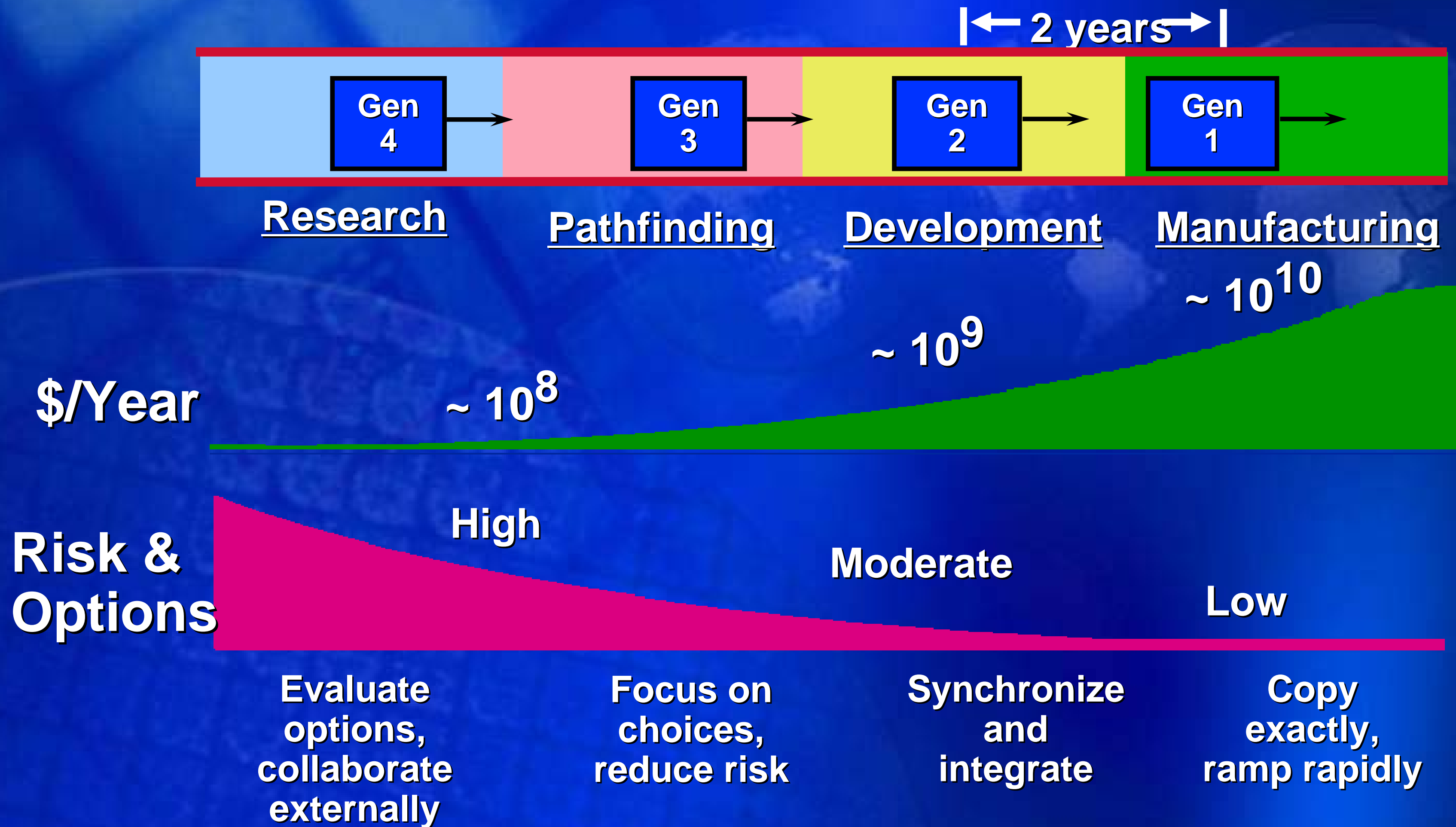
Pipelined Development Enables 2 Yr Cycle



Heavy reliance on Universities & consortia in the early research stages

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Future Transistors

Technology Generation

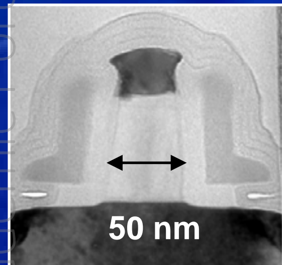
90 nm 2003 — Manufacturing

65 nm 2005 — Development

45 nm 2007

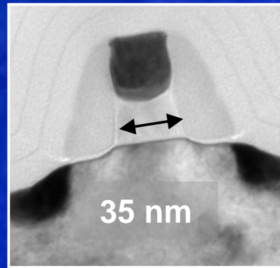
32 nm 2009 — Research

2011+



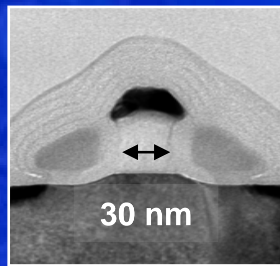
SiGe S/D

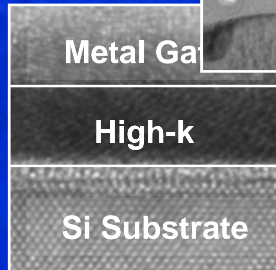
Strained Silicon

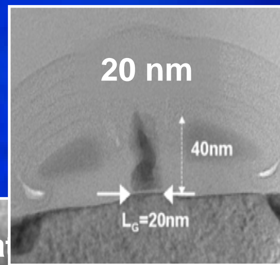


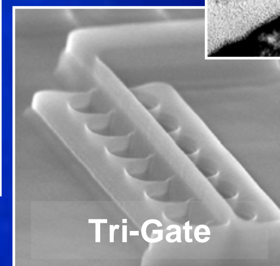
SiGe S/D

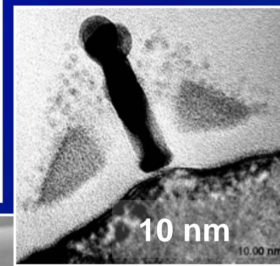
Strained Silicon

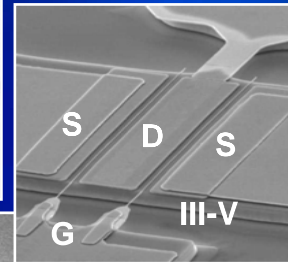


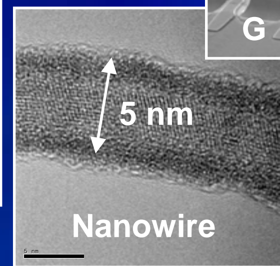




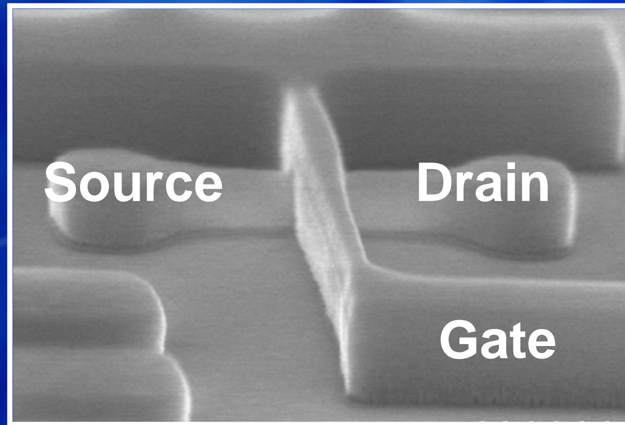


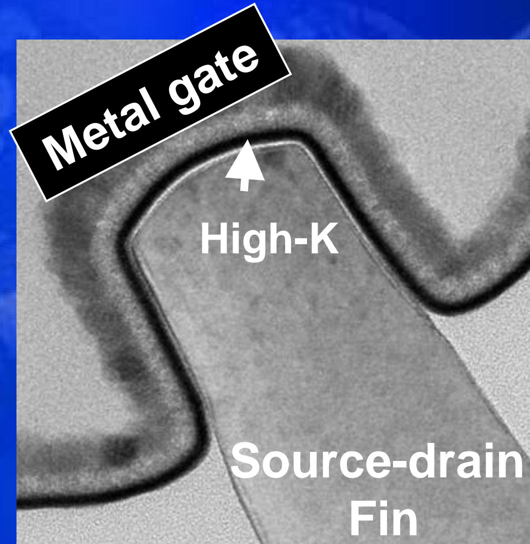


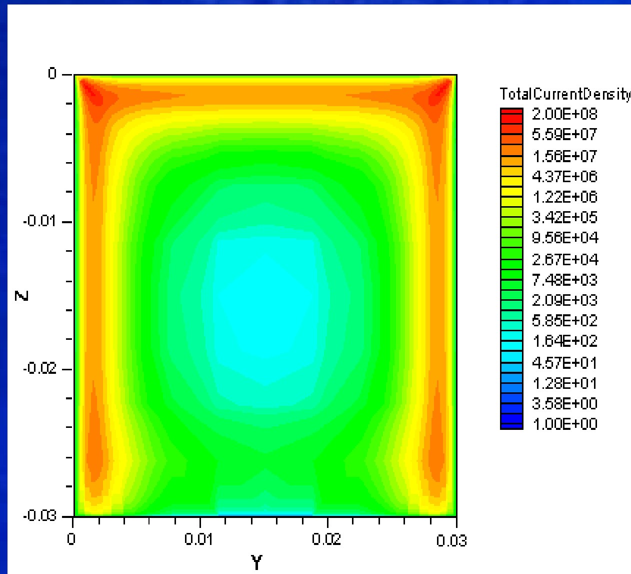


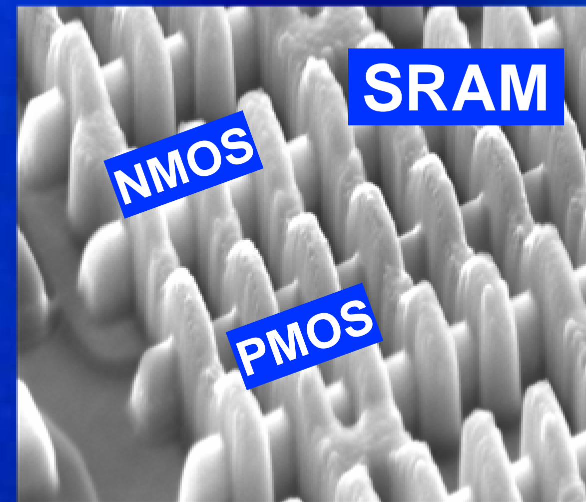


The future: Tri-Gate Transistors?

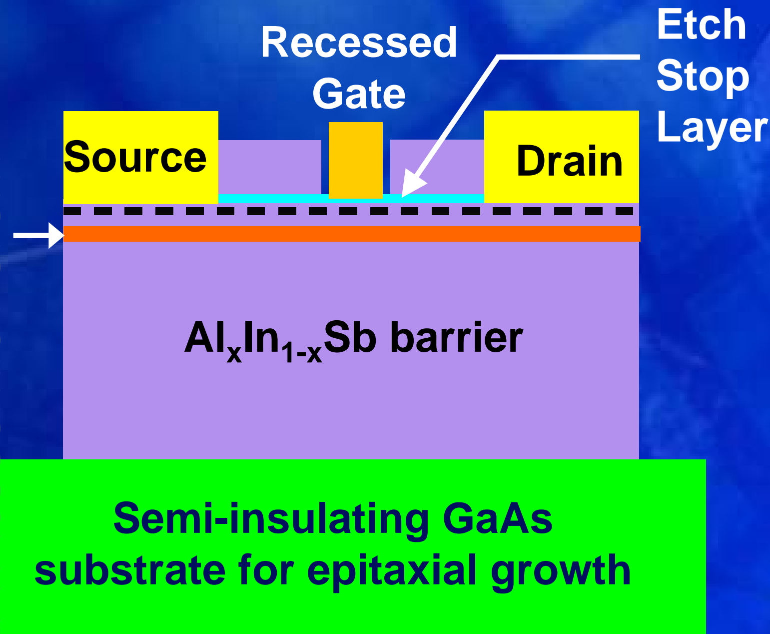








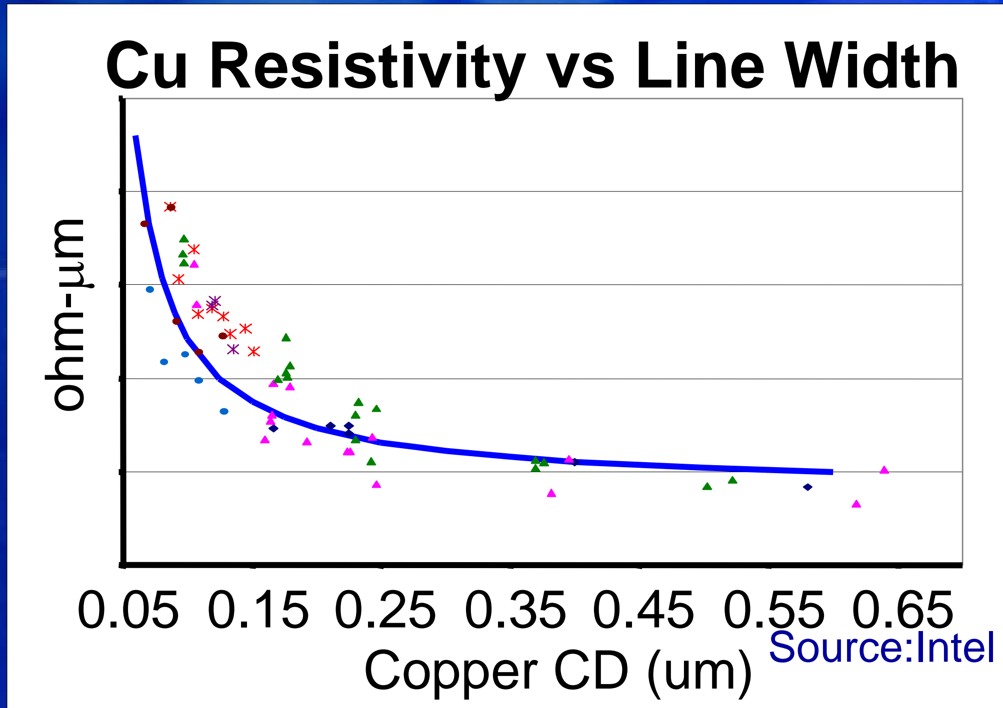
Increasing Electron Mobility

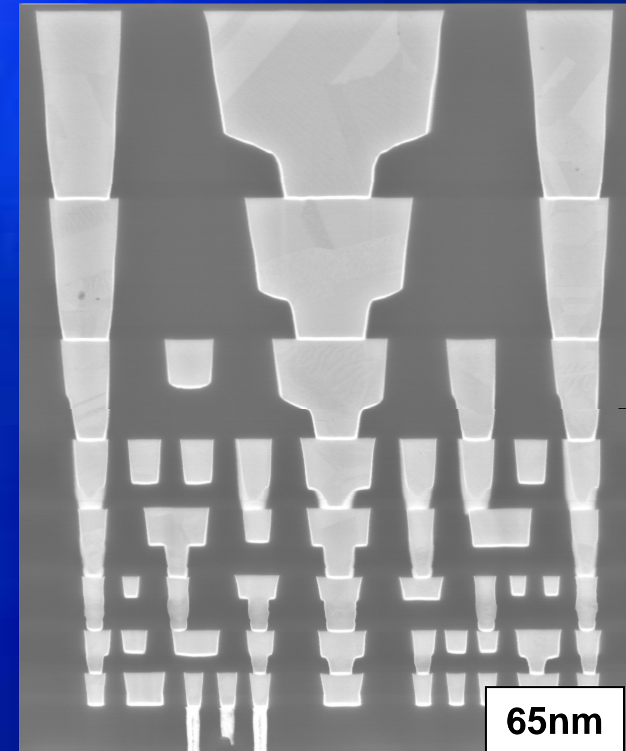


- Increased electron mobility leads to higher performance and less energy consumption
- The challenge is integrating them with Silicon and improving Hole mobility

n-Mobility	Compound Semiconductors		
Si	GaAs	InAs	InSb
1	8	33	50

Scaling of the interconnect





- Effective resistivity increase due to:
  - Cross section reduction due to barriers
  - Increased scattering from grain boundaries and surfaces

Tough but manageable challenges

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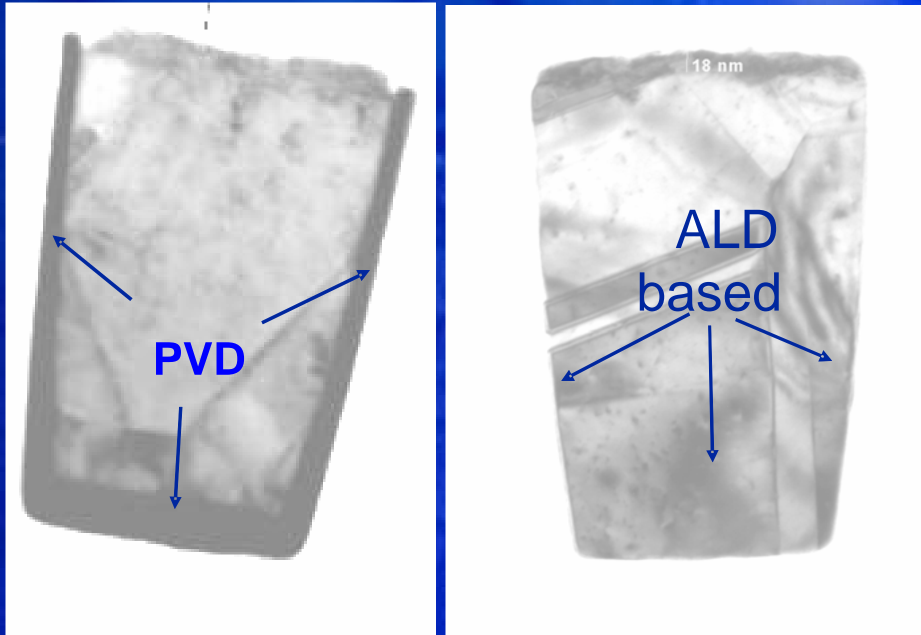
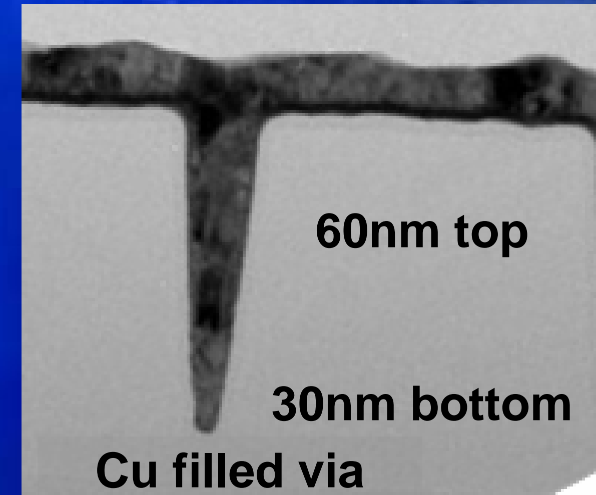
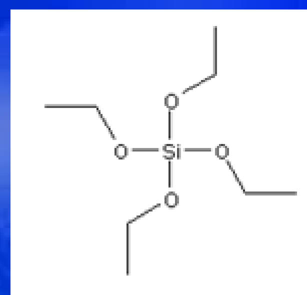
Cu metal line scaling

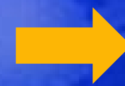


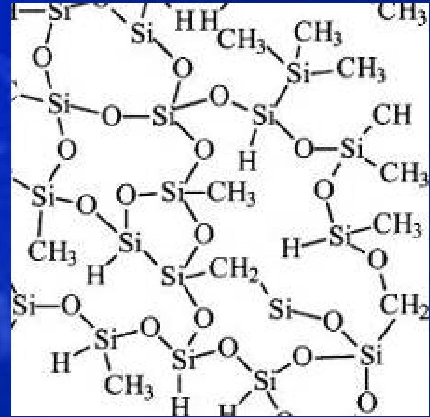


- Barrier scaling for larger copper cross section
- Barrier scaling & Via shaping for easier metal fill

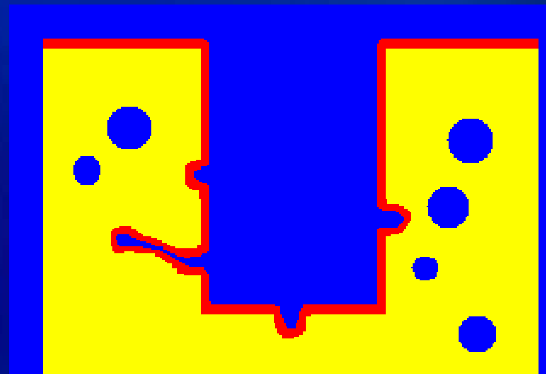
ILDs for Low capacitance interconnects

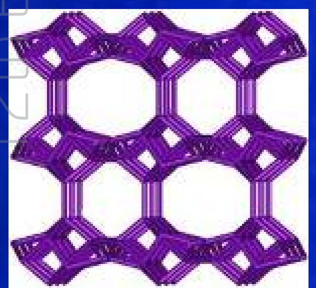


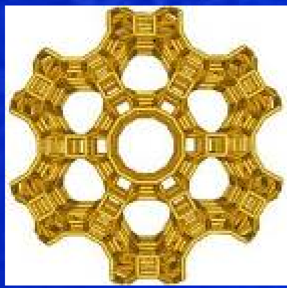




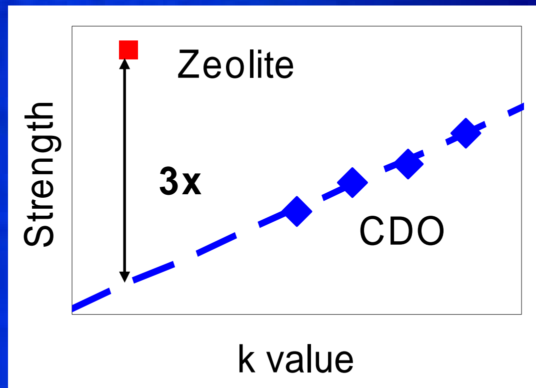
- Reduction of Dielectric Permitivity:
  - Insert Methyl groups (i.e. CDO)
  - Random porous materials
  - Ordered porous materials
  - Polymers with low K







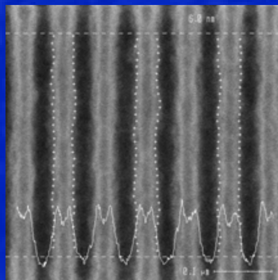
Source: Li et al, UCR, J Phys Chem, 2005



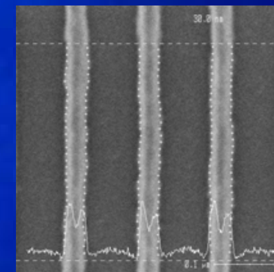
Lithography Challenge

1000
nm
100
10
Feature size
248nm
193nm
Lithography Wavelength
Gap
13nm (EUVL)
'89
'93
'97
'01
'03
'09
Initial Production

Gap closure with EUV



32 nm line/ 64 nm pitch



30 nm line/ 120 nm pitch

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Very High Innovation Rate

Materials		HighK-MGate Xtors for performance & Low Power LowK ILDs for interconnect Si-Ge layers Novel materials for strain and electrical Performance
Transistor Architecture		Novel transistor architectures for HighK-MG TriGate Xtors and III-V integration in the future
Chip Architecture		Efficient Performance/Power with CoreTM2 MultiCore Monolythic integration of Graphics, Mem. Controller etc.
Platform Integration		Power & form factor optimization

High innovation rate in all fronts is critical to Intels success

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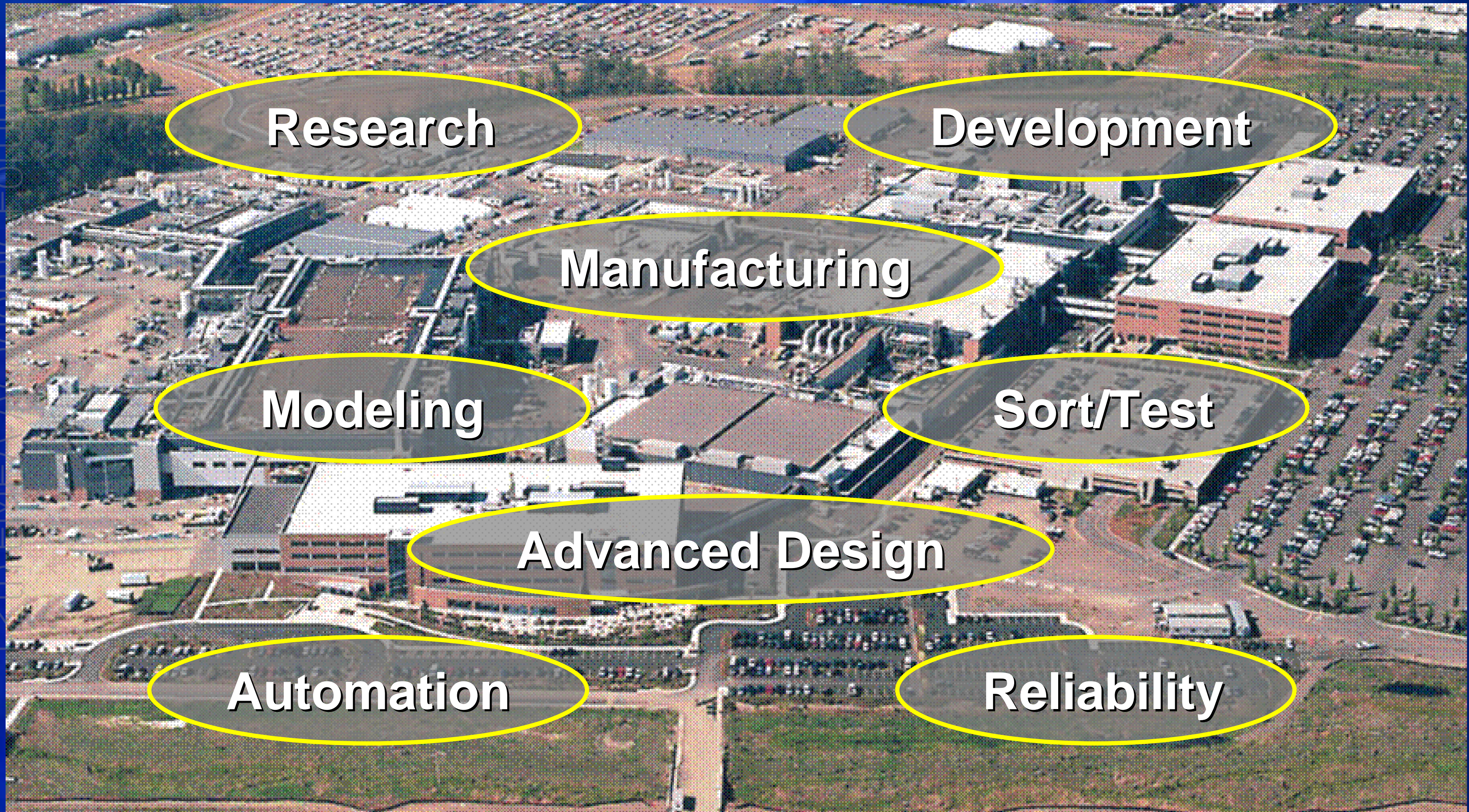
Technology leadership is the result of close multi-group collaboration within Intel +…



The effective collaboration with top research communities around the world

- Collaboration with research consortia like:
  - IMEC (Europe)
  - SEMATECH (USA)
  - SRC
    - GRC: Global Research Corporation
    - FCRP: Focus Center Research Program
    - NRI: Nanotechnology Research Initiative
    - ASET: Association of Super-Advanced Electronic Technologies (Japan)

The effective collaboration with top research communities around the world

- … and research Universities:
  - Funding of projects in ~60 universities worldwide
  - Over $10M funding
  - In the areas of
    - Emerging Devices
    - Interconnects and Reliability
    - Packaging
    - Nano-electronics
    - Opto-devices and optical interconnects
    - Novel memory devices
    - Microsystems

The effective collaboration with top research communities around the world

- Small but growing participation of European Universities/ Institutions
  - IMEC (Belgium)
  - CEIT Research Institute (Spain)
  - University College Cork (Ireland)
  - Forschungszentrum Karlsruhe (Germany)
  - ETH, U Neuchatel (Switzerland)

Some key areas for University Research

- Fundamental understanding of properties and effective metrology for new materials:
  - High K dielectrics and Metal Gate materials
  - CVD/ALD deposited metal barriers/ and seed layers that will be needed to enable plating of lines 30nm and below
  - Ultra Low K ILDs with improved mechanical robustness and pore sealing strategies (if material is porous)
  - Reliability of materials and interfaces and effective metrology
  - Novel materials of interest in both Non-Volatile and 6T Cell replacement schemes
- Promising novel device concepts
  - Improved Power X Delay (Like some III-V?)
  - Improved Ion/Ioff ratios (Like Tri-gate transistors)
  - Novel memory concepts (Both volatile and NV)
- Innovative architectures
  - Low power logic architectures
  - Fault tolerant strategies for logic

Some key areas for University Research

Some additional suggestions:

- Do not compete with industry in integration or in trying to build smaller devices
  - The cost is very high and the likelihood of success is low
- Focus on fundamental understanding, Metrology, and proof of concepts for novel devices (2011+)
- Develop a partnership with some key industry player
  - Guidance on what the relevant problem are, access to advanced equipment, materials and samples

The key core competency for the University is Brain Power, not money or fancy equipment

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