Materials & Metrology Challenges for Planarization and Interconnect Technologies

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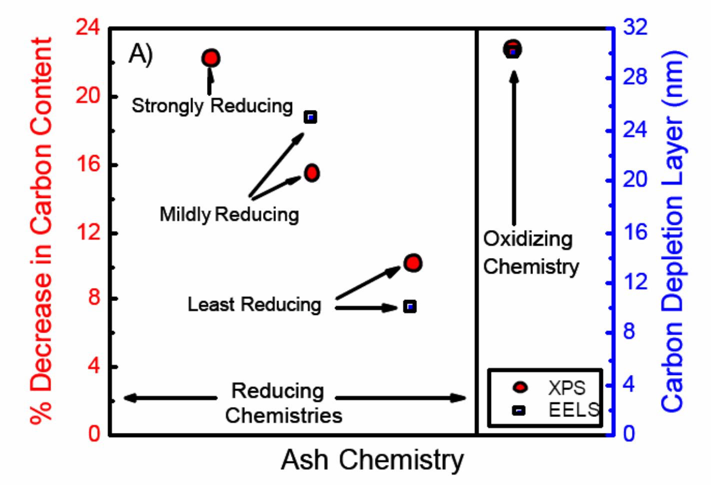
Outline:

- Key Backend challenges
- Integration challenges with current Low K materials
  - Etch & Clean
  - Pore Sealing/Damage Repair
  - Alternative integration schemes
  - Novel Materials
- Metrology Challenges
- Narrow Line Resistivity Challenge
- CMP Technology trends
  - Metrology & Characterization: Few examples
- Beyond Cu/Low K: CNT
- Summary

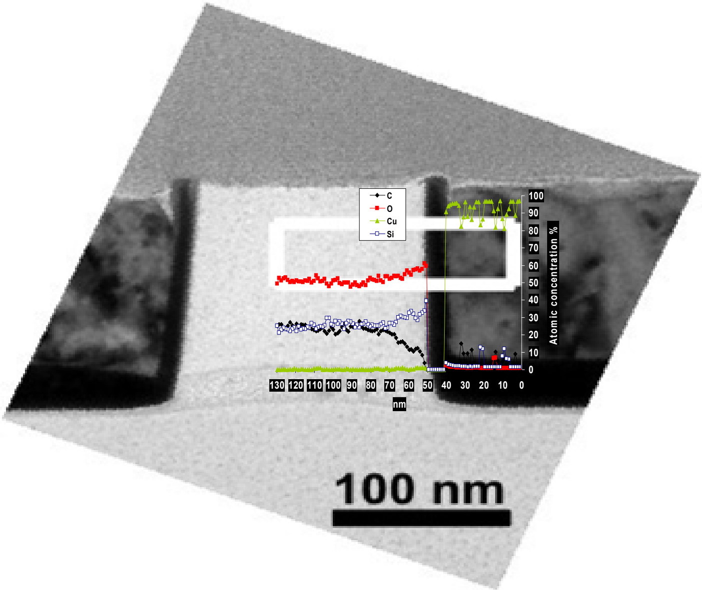
Key Backend Challenges (sub-32nm)

- **Low K Dielectrics**
  - Decreasing low K ILD capacitance while retaining adequate mechanical properties
  - Integration of porous ILD materials (e.g., ALD barrier integration, etch/cleans)
- **Barrier/seed**
  - Controlling line and via resistance in narrow features (minimizing R in the RC delay)
  - Extendibility of PVD vs. new CVD & ALD-based processes
- **Cu Plating**
  - Achieving 100% gapfill in lower metal layer structures
  - Controlling Cu resistivity increase in narrow features
  - Plating gapfill and uniformity when plating on very thin seeds or directly on barrier
- **Planarization**
  - Extendibility of conventional CMP processes is not well defined
- **Electromigration**
  - Achieve EM requirements with no integrated process impact

Ultra Low K Integration Challenges – Etch & Cleans



Dalton, *et al.*, 2004 IITC



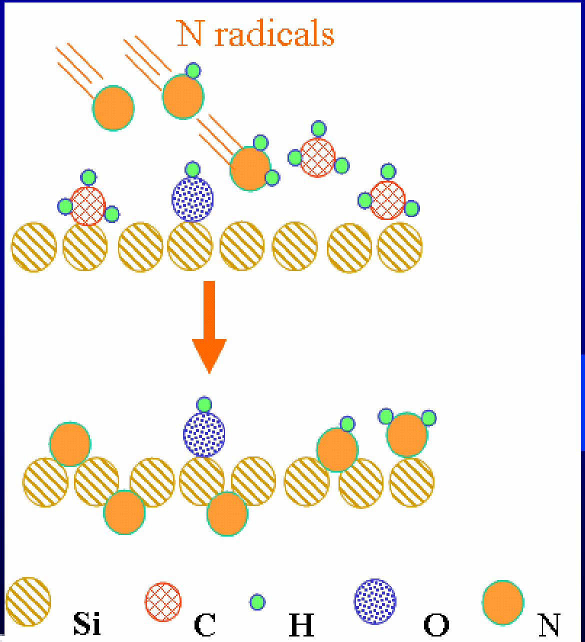
F. Iacopi, IMEC

- **Dry etch → ILD damage → increase k**
  - **C depletion**
  - **Oxidation (introduction of –OH groups)**
  - **Film densification**
- **Wet etch → impact on k and film stability**
  - **Moisture uptake (significant k increase)**

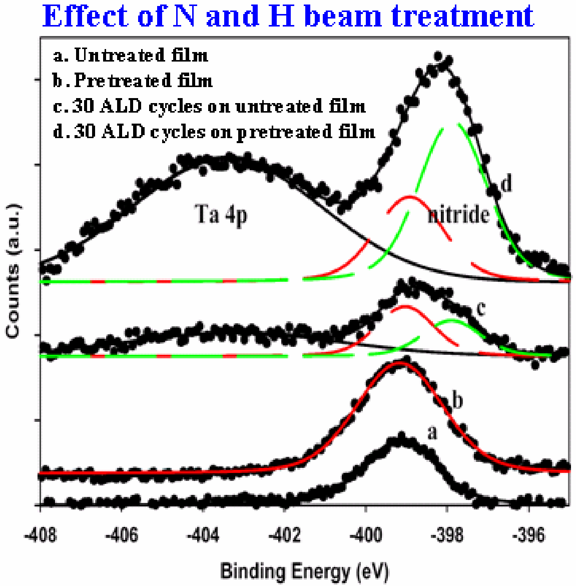
Need solutions to address both surface and bulk ILD damage

Beam Activation of CDO Surface

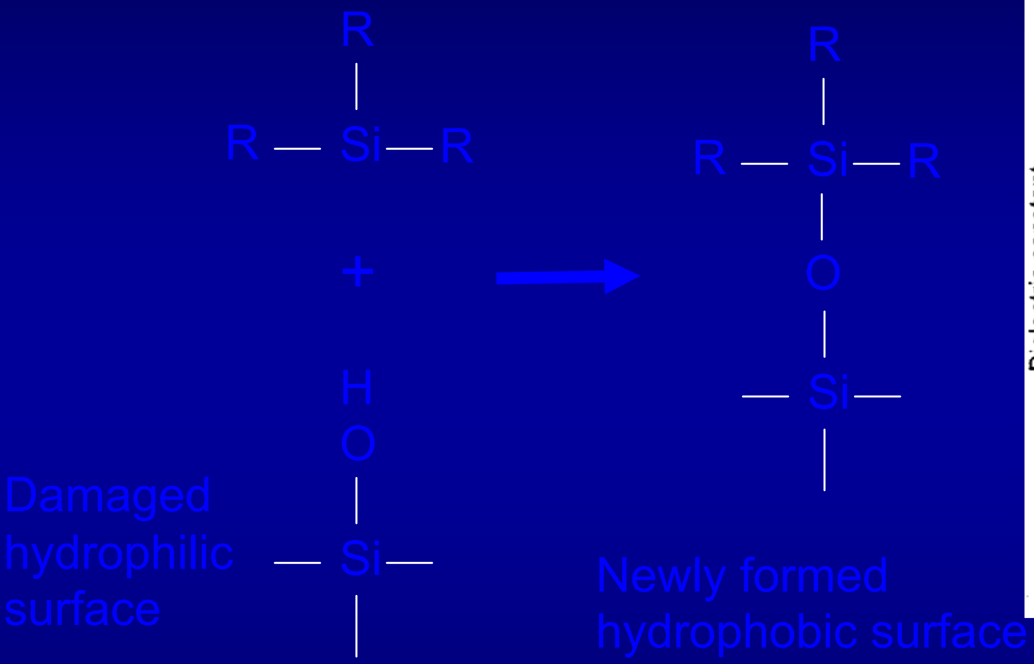
- Beam activation serves two purposes:
  - Simulation of low k process damage
    - Can simulate damage using O_2, N_2, NH_3 and H_2/He beams
    - Can control penetration depth of radicals during activation
    - Will determine k impact, roughness, densification and hydrophobicity
  - Preparation of low k surface for ALD barrier formation
    - N radical activation results in C depletion and N enrichment at low-k surface (enhances nitride formation for metal barrier)

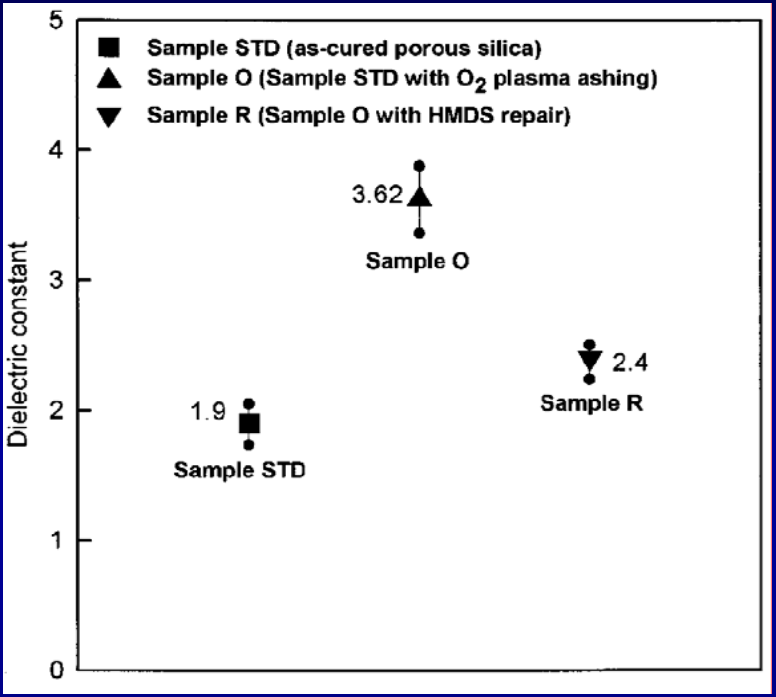


J.J. Liu, J. Bao and P.S. Ho, MRS Symp. April 2004



Solution Path: Dielectric Repair / ”K-value Restoration” → Recovery of k with Silylation Agents





(Y.S. Mor, JVST B 20(4), 2002)

Proper choice of R can promote pore sealing and surface planarization at the same time

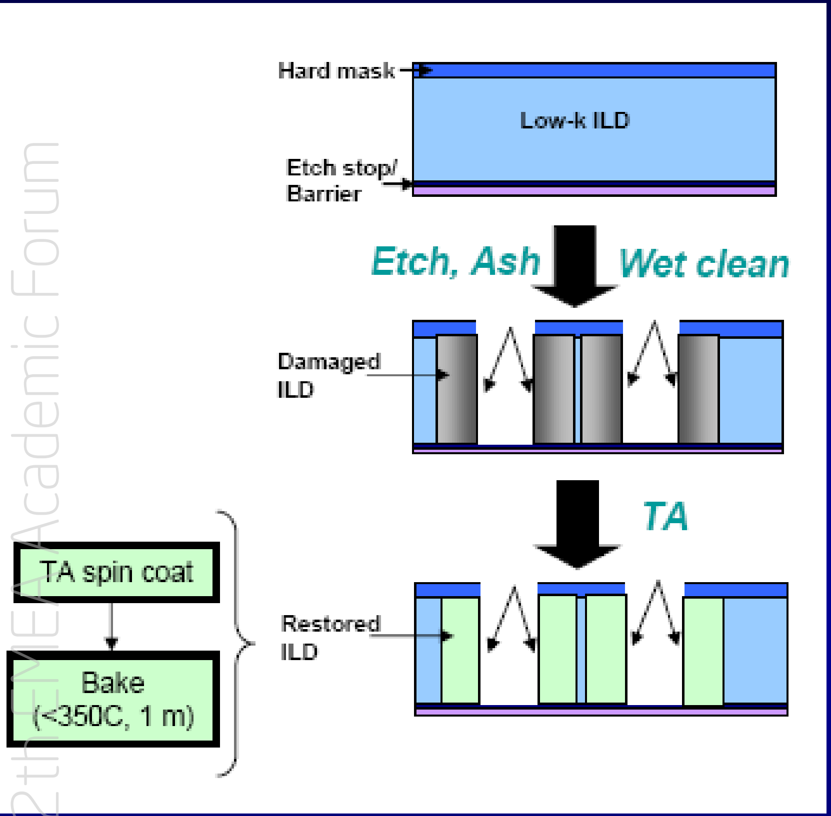
Several silylating agents available: HMDS, TMCS, TMDS

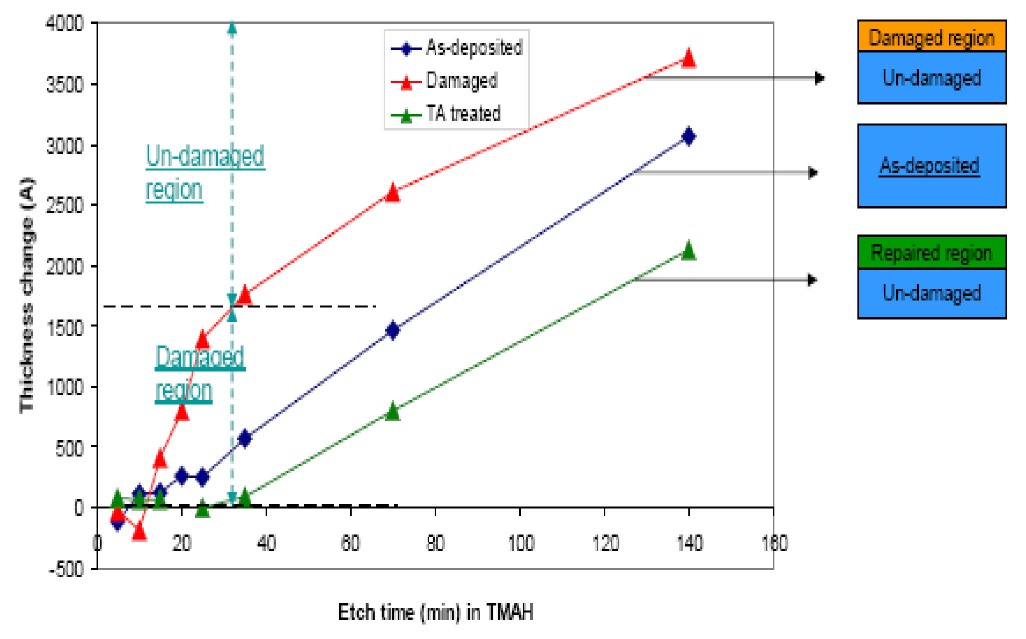
Through chemical reactions, e.g.

$$(CH_3)_3Si\text{-}NH\text{-}Si(CH_3)_3 + HO\text{-}Si\equiv_{(s)} \rightarrow (CH_3)_3 — Si — O — Si\equiv_{(s)} + NH_{3(g)}$$

(HMDS)

Dielectric Repair / ”K-value Restoration”

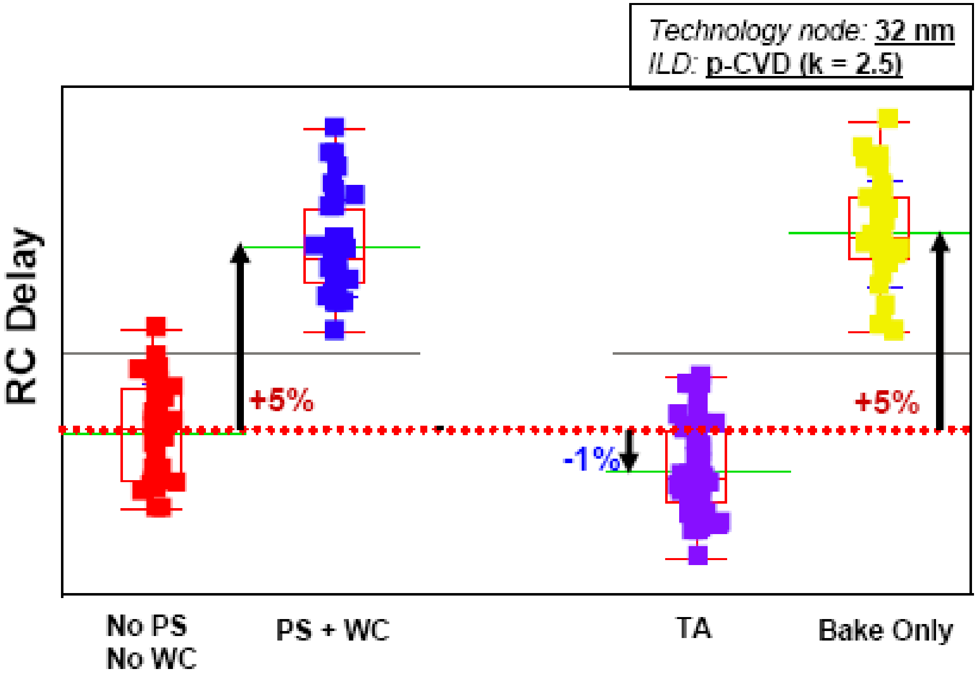




- •Plasma and wet processes lead to carbon loss in SiOCH films
- •TA treatment restores carbon and eliminates SiOH bonds[3]

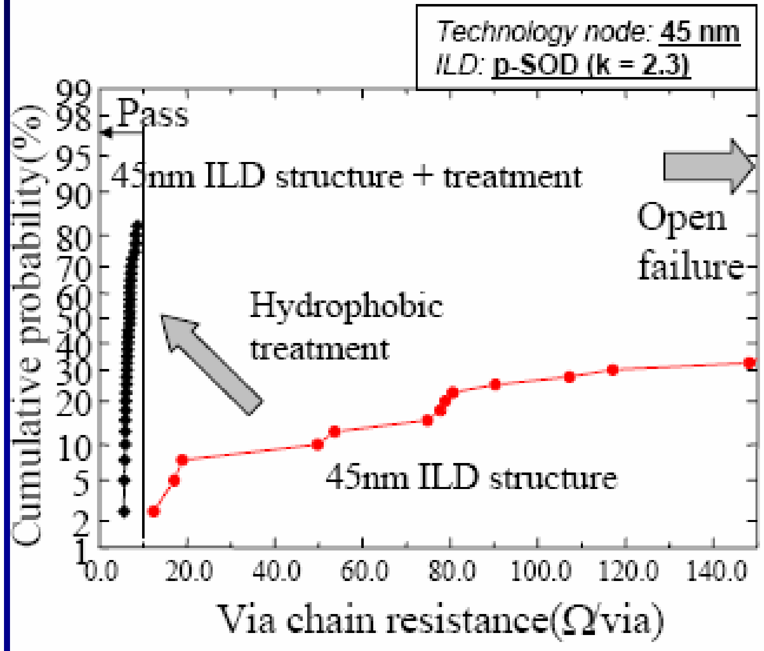
A. Bhanap, et al (Honeywell, HEM), IITC 06

Reduction in RC Delay



PS	Plasma strip
WC	Wet Clean
TA	TA treatment before and after (PS + WC)
Bake only	350C hot plate bake after (PS + WC)

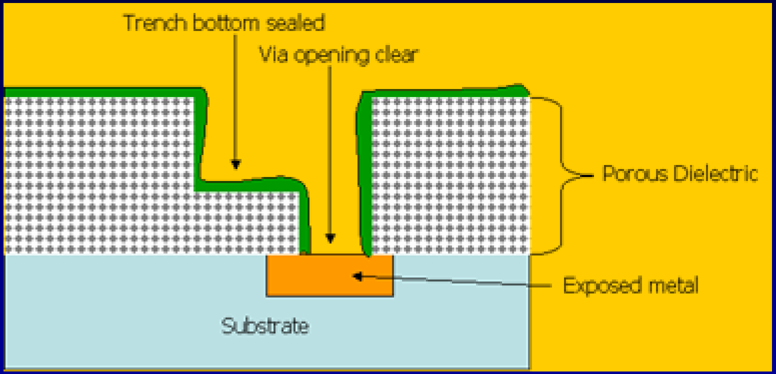
Reduction in Stress Induced Voiding

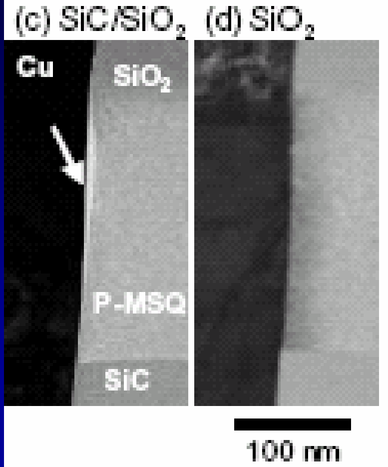


TA Treatment: Replenishes Carbon
Restores Hydrophobicity
Restores K

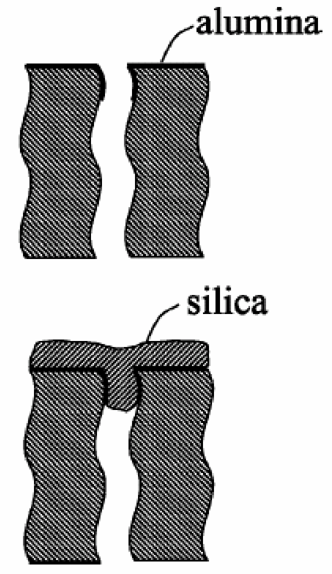
A. Bhanap, et al (Honeywell, HEM), IITC 06

Selective Pore Sealing



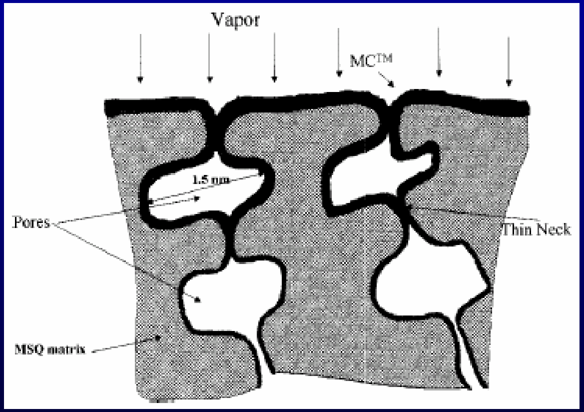


Furuya, *et al.*, 2004 IITC



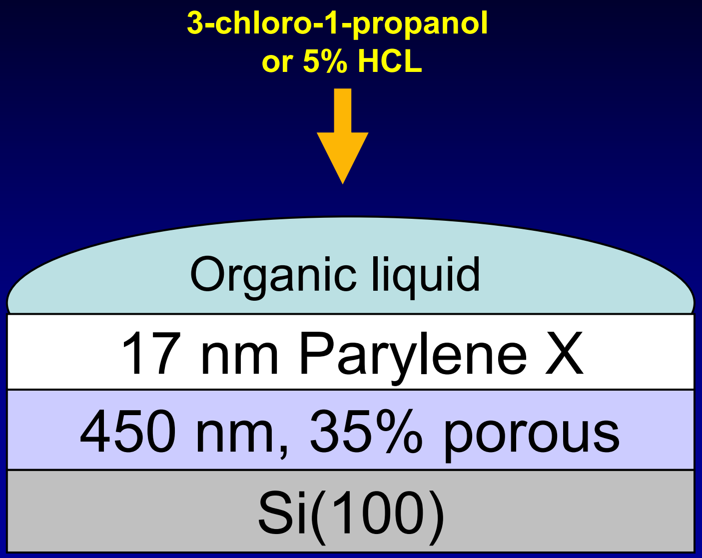
de Rouffignac, *et al.*, Electrochem Solid-State Lett, (2004) v 7, pp G306-G308

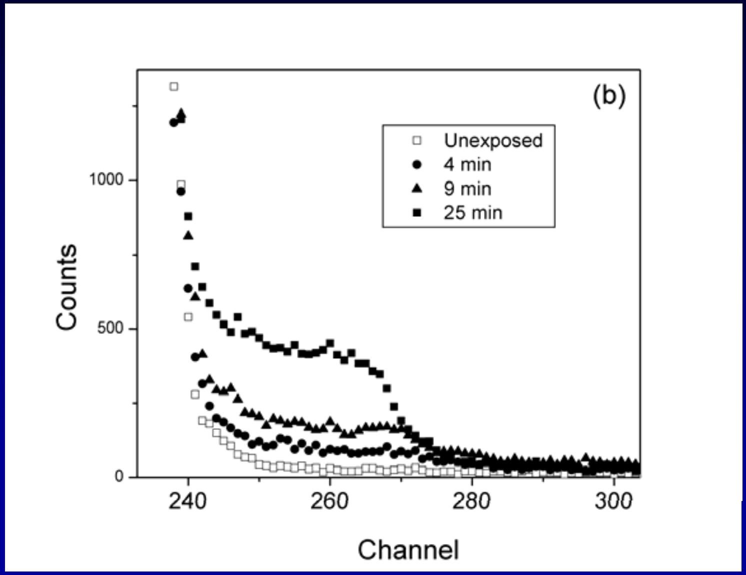
- **Process and materials solutions being explored**
- **Process:**
  - **Etch byproduct redeposition**
    - **Concerns about surface roughness, adhesion and pinhole defects**
- **Materials:**
  - **ALD Silica**
    - **Conformal SiO_2 coatings with Al seed**
    - **Need to tailor penetration and metal selectivity**
    - **Larger k_{eff} impact than low k sealants**
  - **Parylene deposition**
    - **Selective to transition metals**
    - **Must limit penetration to minimize k impact**

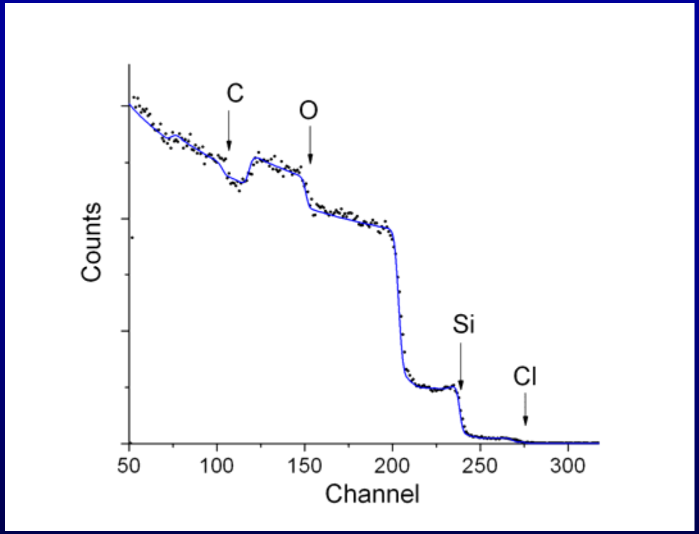


Jezewski, J Electrochem Soc, (2004) v 151, pp F157-F161

Chemical Penetration: Question of appropriate Metrology

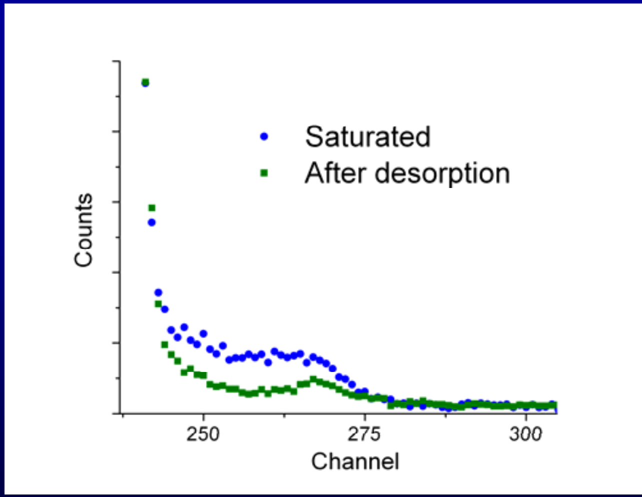






Exposure to vacuum
(1E-4 Torr @ RT)

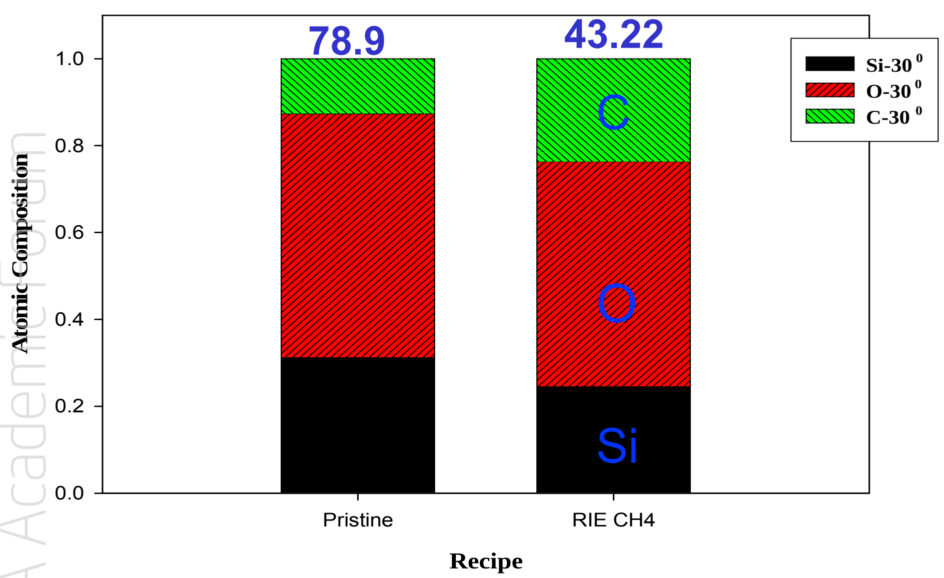
Sample	% desorption
Uncaulked	87
Caulked	52



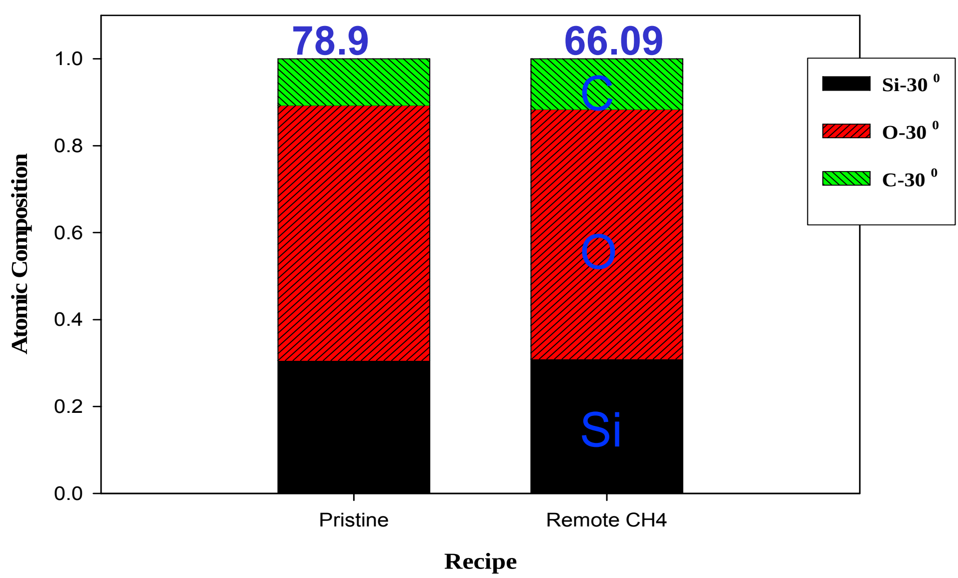
Experimental RBS spectrum (●●●) and simulation (–) of parylene X on porous dielectric exposed to chlorine tagged organics (3-chloro-1-propanol or 5% HCl)

R.D. Geil & J. Senkevitch, MRS 2007

Carbon-rich Sealing Layer by CH_4 Beam



RIE CH_4



Radical CH_4 (Remote Plasma)

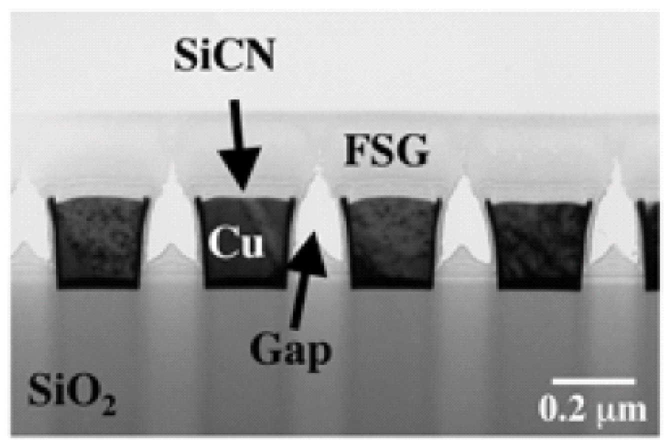
- ➢ XPS analysis showed a large carbon increase at the surface by RIE CH_4 treatment.
- ➢ Remote CH_4 plasma caused a carbon increase at the surface but the effect was smaller than RIE $CH_{4.}$

† blue numbers: contact angles.

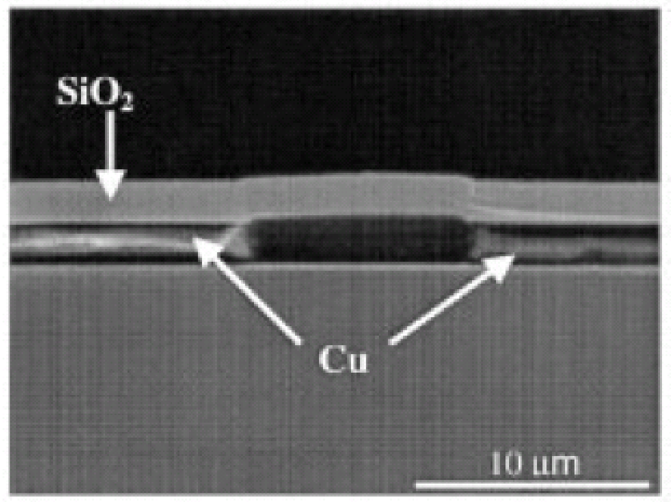
P.S. Ho, et al, UT Austin

Air-Gap: The lowest possible k

- Air-gap incorporates the limiting case $k_{ILD} \rightarrow 1$
- Two approaches to air-gap interconnects:
  - Process: Form air-gap through deposition properties
  - Materials: Remove sacrificial material downstream
- Both have significant challenges:
  - Structural integrity of final structure is questionable
  - Additional process steps add significant cost!
  - Multi-layer processing presents additional challenges…

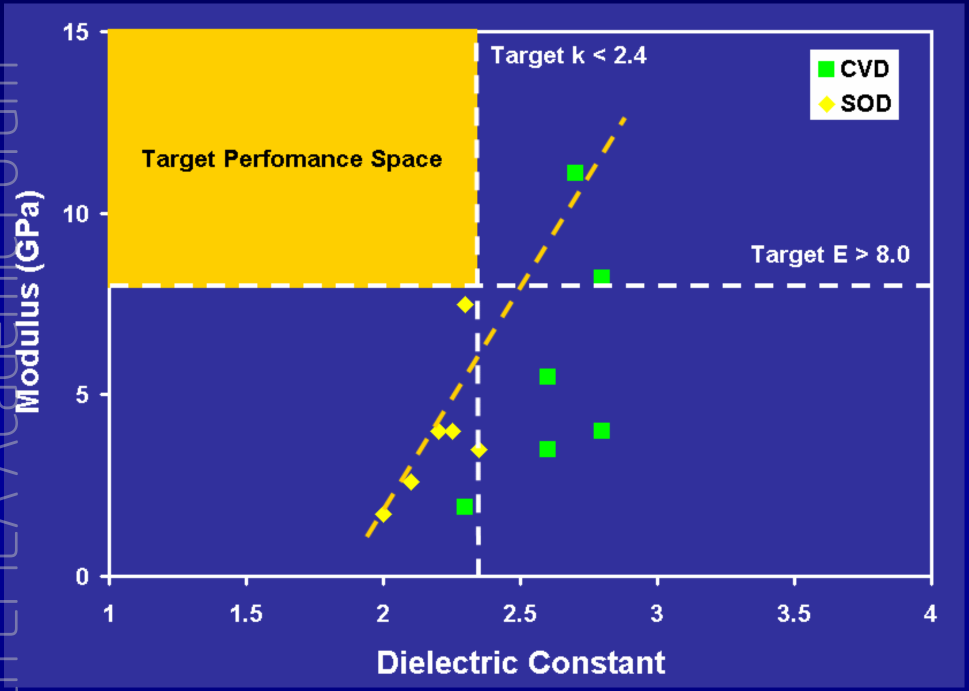


Noguchi, *et al.*, IEEE Transactions on Electron Devices (2005), v 52, n 3, pp 352-359



Bhusari, *et al.*, J. Microelectromechanical Systems, (2001), v 10, n 3, pp 400-408

Novel Materials



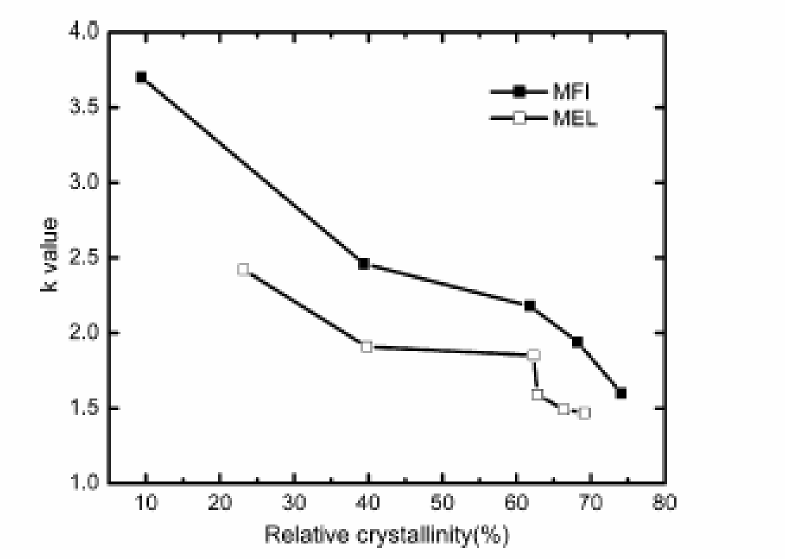
Source: Data from IMEC evaluations, used with permission

- Areas outlined so far do not address ultimate requirement: thermomechanical reliability
- Many CVD and SOD materials lie along (or below) same performance curve
  - Similar trends exist for hardness, cohesive strength
- Cure optimization is not sufficient to move into desired performance space

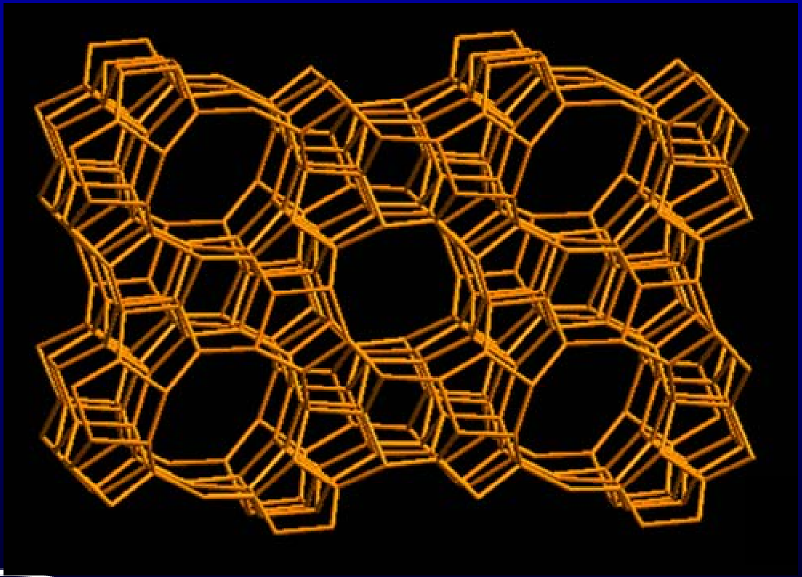
Need fundamental materials changes to enter new performance space

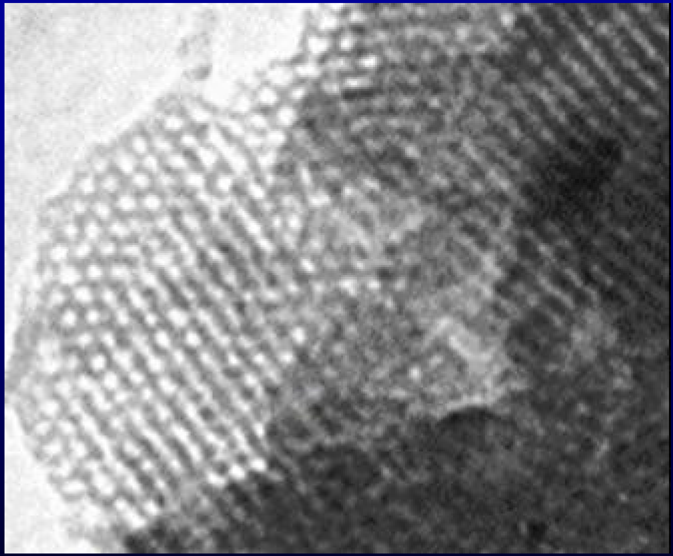
Templated Materials

- Templating allows materials with ordered porosity
  - Can achieve high porosity while maintaining mechanical strength
- Zeolites: class of naturally-occurring ordered porosity materials
  - Synthetic pure SiO_2 zeolite (silicalite) shows ~5x increase in modulus for equivalent k value (Wang, *et al.*, Adv. Mater. 2001)
  - Adding other metals (Al, Ti, Ge, Mn…) can increase strength further
- Currently, only available through spin-on sol-gel processing

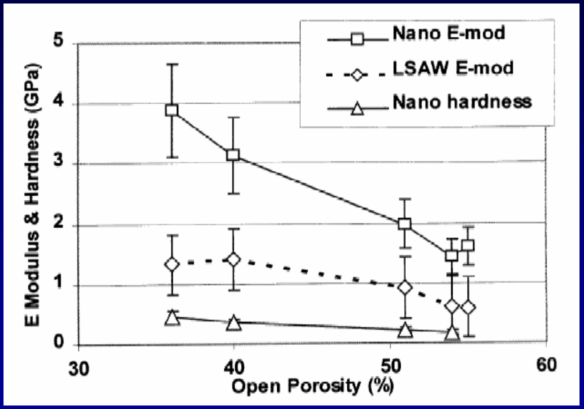


Y. Yan (UC Riverside, J. Phys. Chem. B 2005

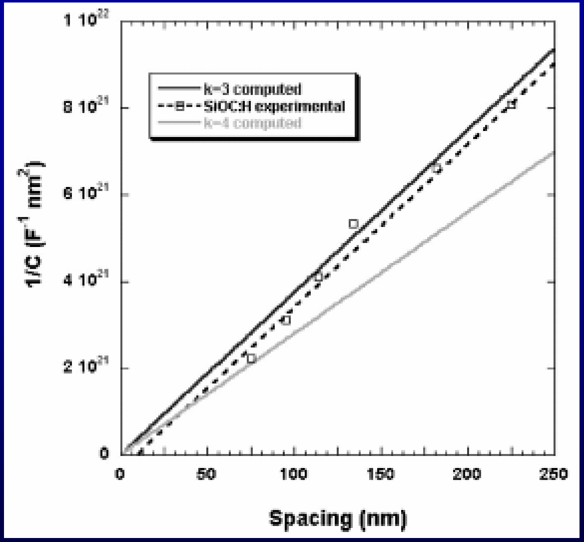




Metrology Development



Murray, *et al.*, Microelectronic Eng, 2002, 60, 133-141

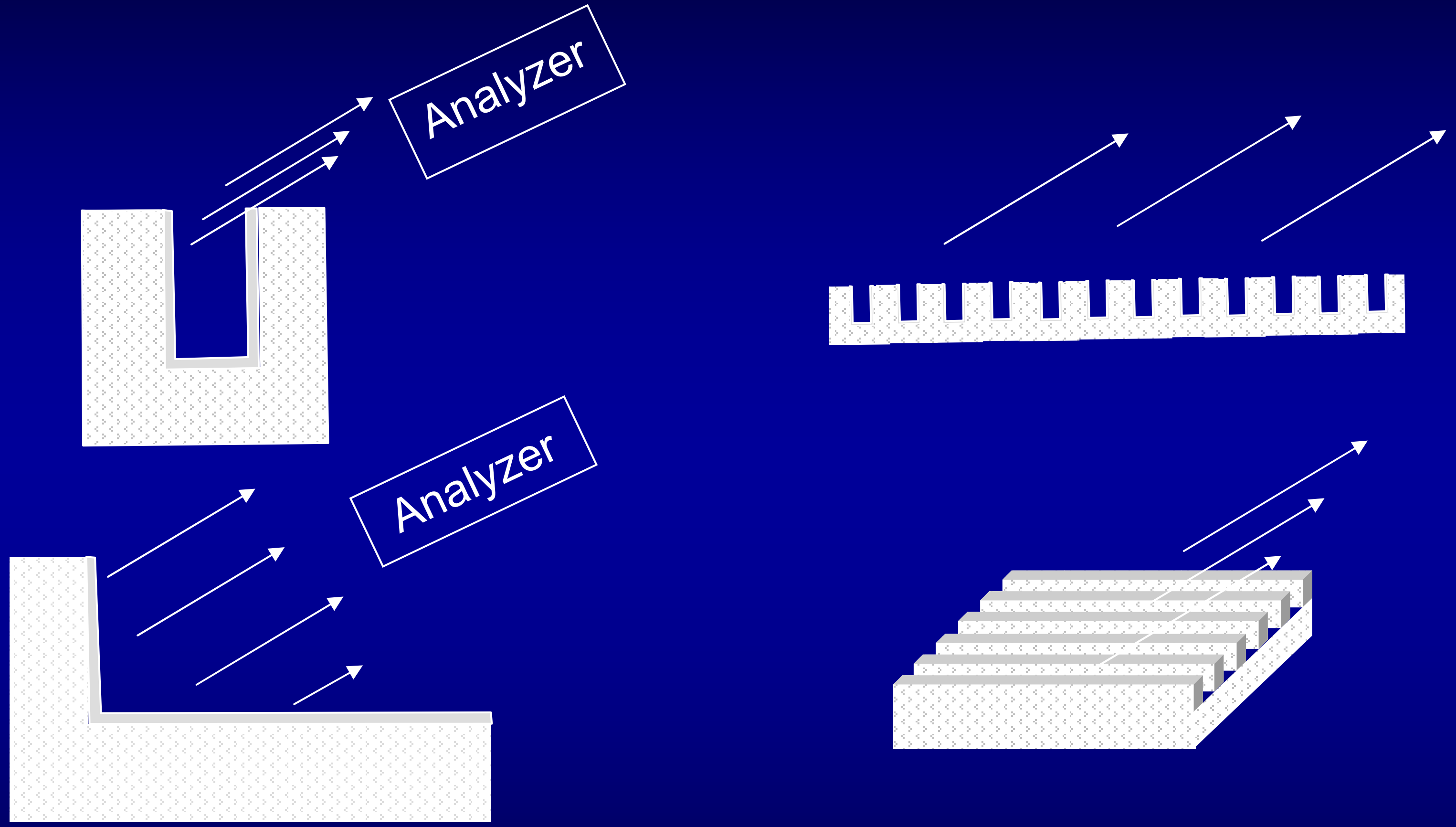


Iacopi, *et al.*, Electrochem Solid State Lett, 2004, 7, G79-G82

- Current methods for measuring mechanical properties
  - Require unrealistic film thickness
  - Give divergent results
- Dielectric damage and pore sealing require new techniques
  - HF decoration is qualitative only
  - EELS and e-test are time-consuming
  - E-test requires full patterning and passivation
- Fab-based real-time characterization techniques will provide significant benefits
  - Only few techniques exist for analysis of patterned structures

New fab-based metrologies are needed for film screening and process control

Angle Dependent X-ray Photoemission Spectroscopy



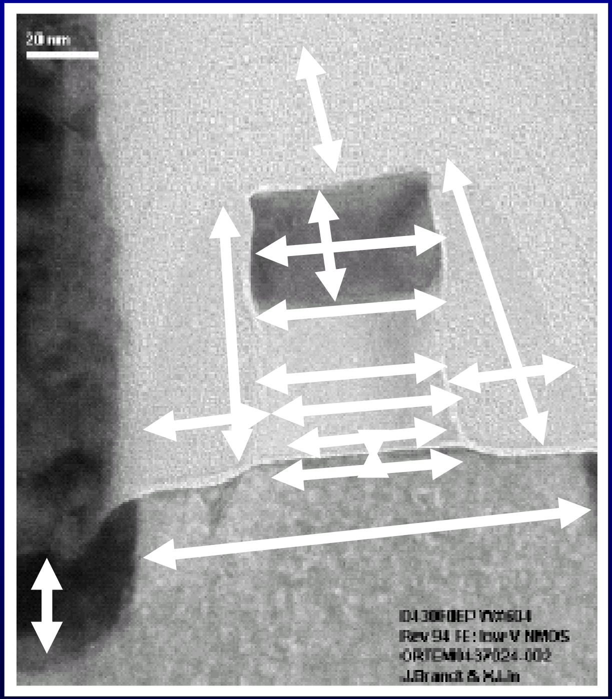
Angle-dependent XPS can obtain sidewall information on surface chemistry and material reaction while maintaining the same sampling depth.

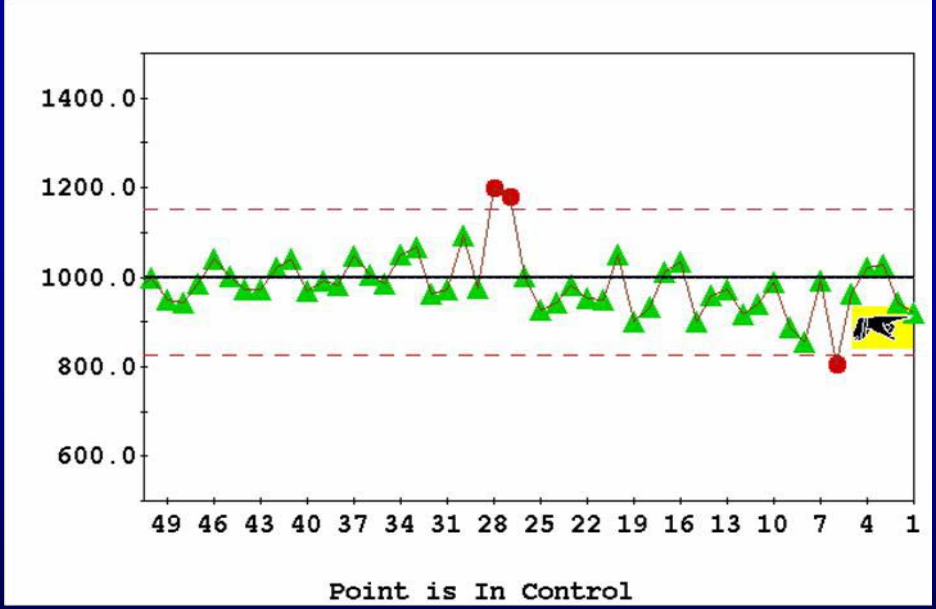
Charging effect may compromise the spectral analysis for chemical states ⇨ can use parallel-line structures to minimize charging effects

Analysis vs. Metrology

- **Analysis: TEM Cross Section**
  - From this data:
    - >15 dimensional measurements
    - Step Coverage
    - Information about composition, strain, defects etc..
  - Time to information for 1 transistor - 0.5 days- 1 week

- **Metrology:**
- **Z-dimensional thickness**
- **CD**
- **Time to information 30 seconds**
- **For 13 sites**





Public Information
From Bohr et. al., 2004 IEEE International Electron Devices Meeting ((IEDM))
December 15, 2004
http://www.intel.com/technology/silicon/micron.htm#65nm

Metal Resistivity

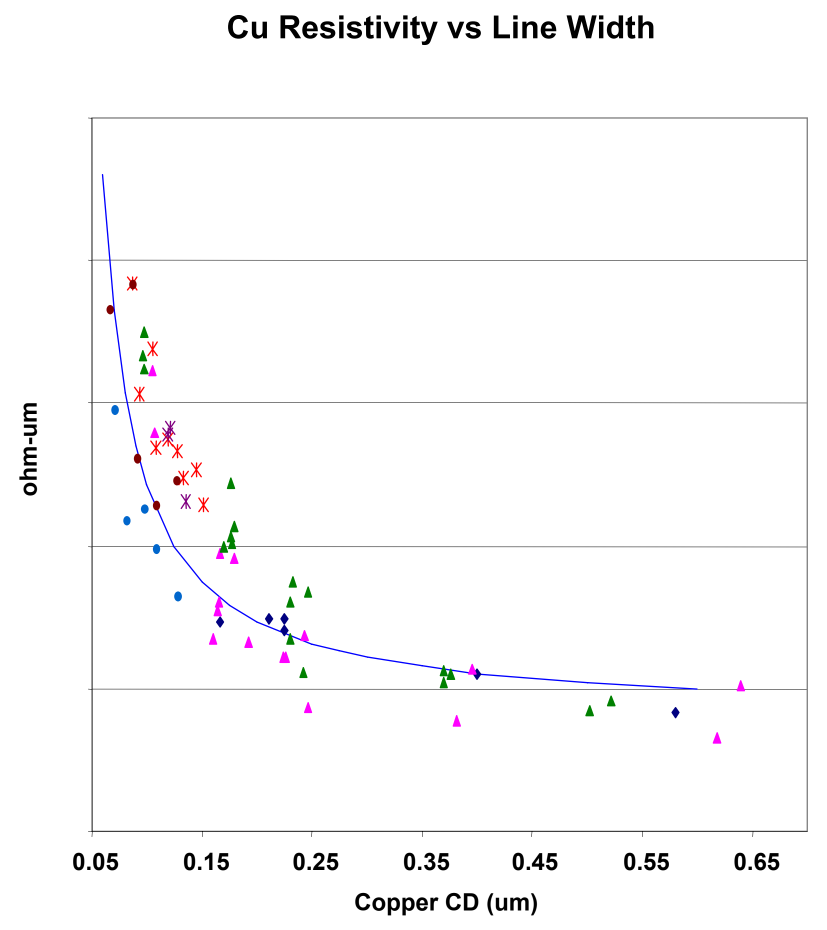
- Resistivity is a growing concern as line widths scale

- Combined effect of liner thickness and electron scattering <u>increases</u> effective resistivity as metal width scales from 150nm to 75nm
  - ➢ ALD liners will maximize Cu volume and minimize resistivity

- Feature size is approaching mean free path of electrons in Cu

Approaches:

- Cu Grain Size Engineering
- Trench Engineering
- Cu seed and barrier films scaling
- Alternative barrier films

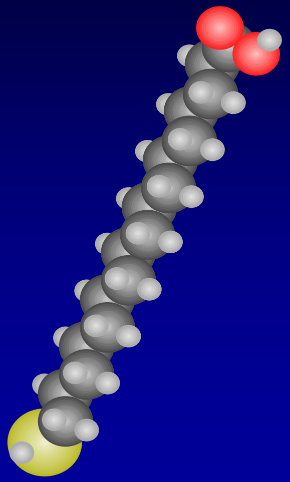


Resistivity Cu_{Bulk} = 1.7 micro Ohm cm

SAMs: Self-assembled monolayer barriers

Self-assembled monolayers: monomolecular organic film

Self-assembly: spontaneous chemisorption of active surfactant on a solid from gas/liquid phase



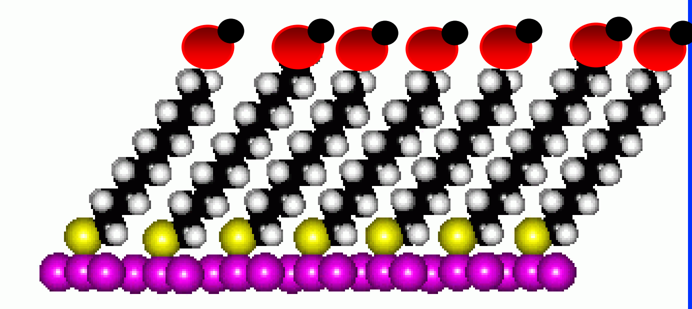
terminal functional group exposed SAM-gas/liquid interface

hydrocarbon segments

lateral interactions and tilt to minimise free volume

generally alkyl chains with Van der Waals interactions

head group bonding to specific substrate sites



‘pseudo-(100)’ octanethiolate on Cu(111)[1]

[1] F. Schreiber, Prog. Surf. Sci. **65** (2000) 151.

Cu passivation: SAM-S (sacrificial)

1-decanethiol $CH_3(CH_2)_9SH$

terminal group	CH_3
CH_2 chain length	9
head group	SH

Cu diffusion barrier: SAM-B (barrier)

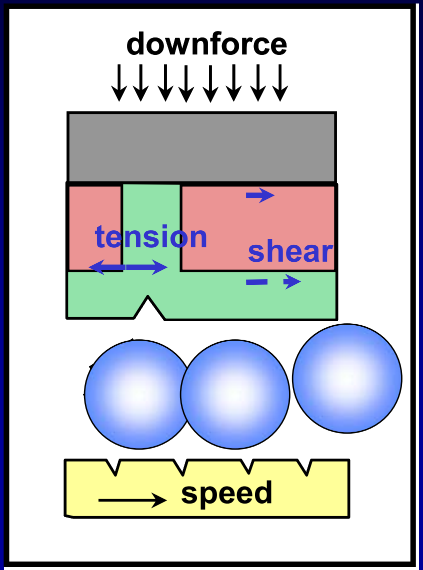
3-mercaptopropyltrimethoxysilane $HS(CH_2)_3Si(OCH_3)_3$

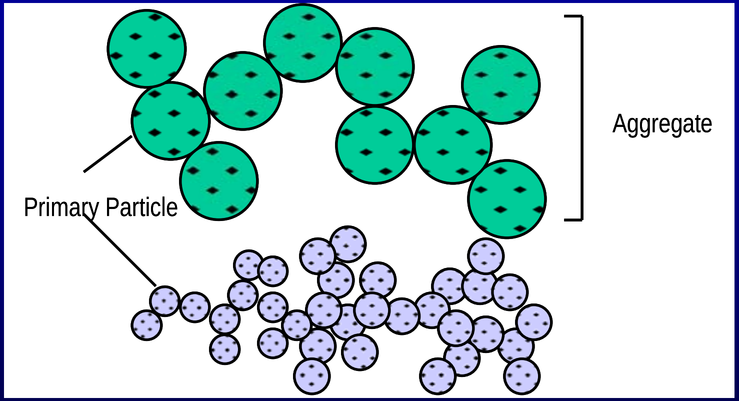
terminal group	SH
CH_2 chain length	3
head group	$Si(OCH_3)_3$

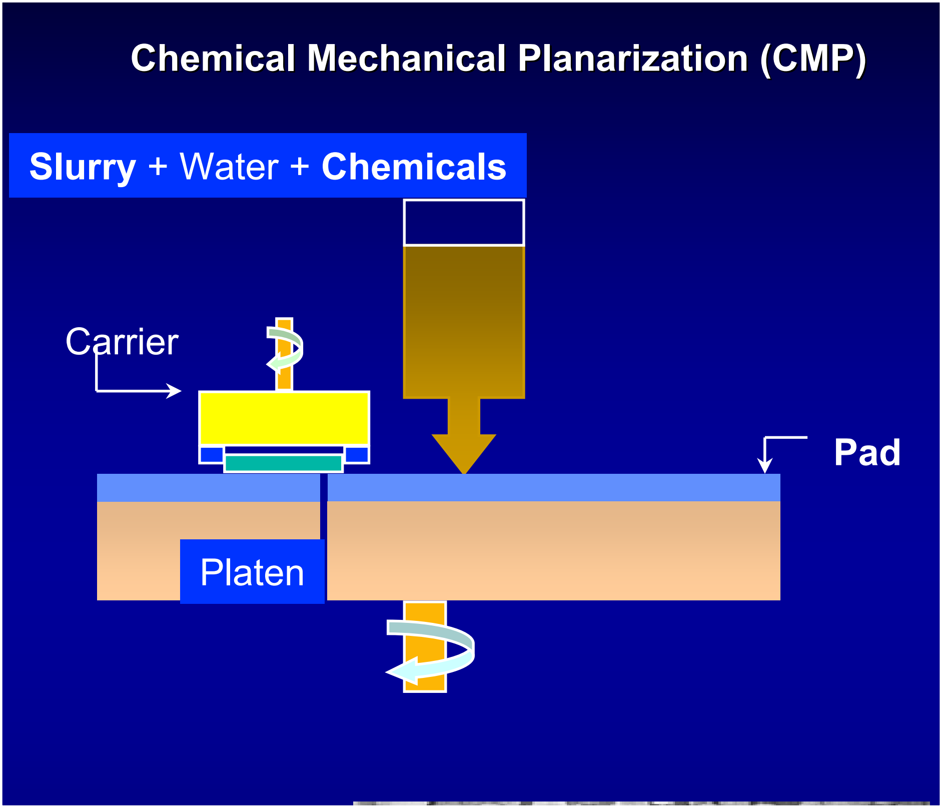
C.Whelan, IMEC

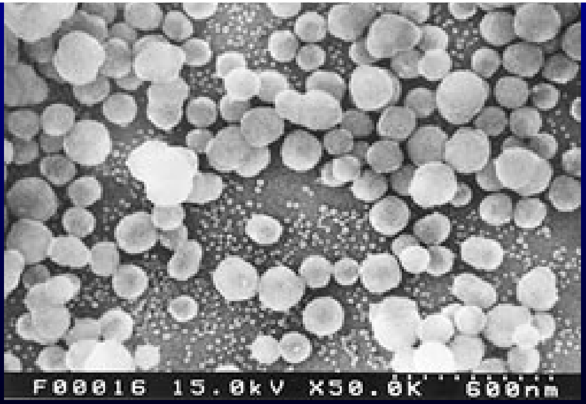
- ❑ Both molecules commercially available
- ❑ Gas/liquid phase deposition possible
- ❑ Both liquid deposited SAMs characterized in literature

Chemical Mechanical Polish





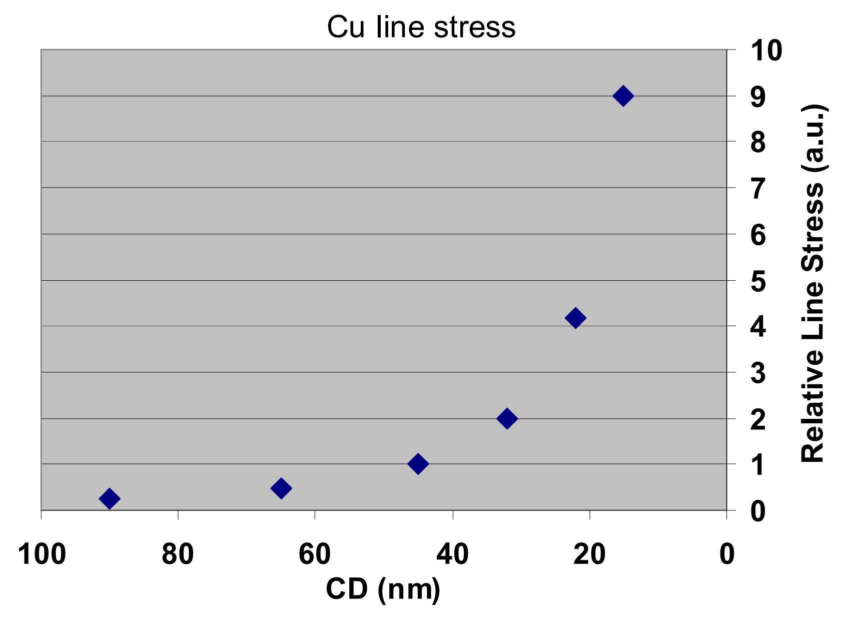




- **Nano Particles & Nano Metrology**
- **New Particle Characterization Methods**

CMP Technology Trends & Challenges

- Topography requirement trends with Moore's Law: 30% reduction every two years — CMP pace is critical in maintaining Moore's law.
- Materials that are subject to polish are diverging due to diverging application needs.
- Each application could deal with heterogeneous materials, leading to complex solutions.
- Key words for future CMP applications are versatility and tunability
- Nano particle engineering and characterization, complex chemistry (<u>during and post CMP</u>) and new metrology for new applications
- Increasing role of nano-particle agglomeration & its impact on defectivity



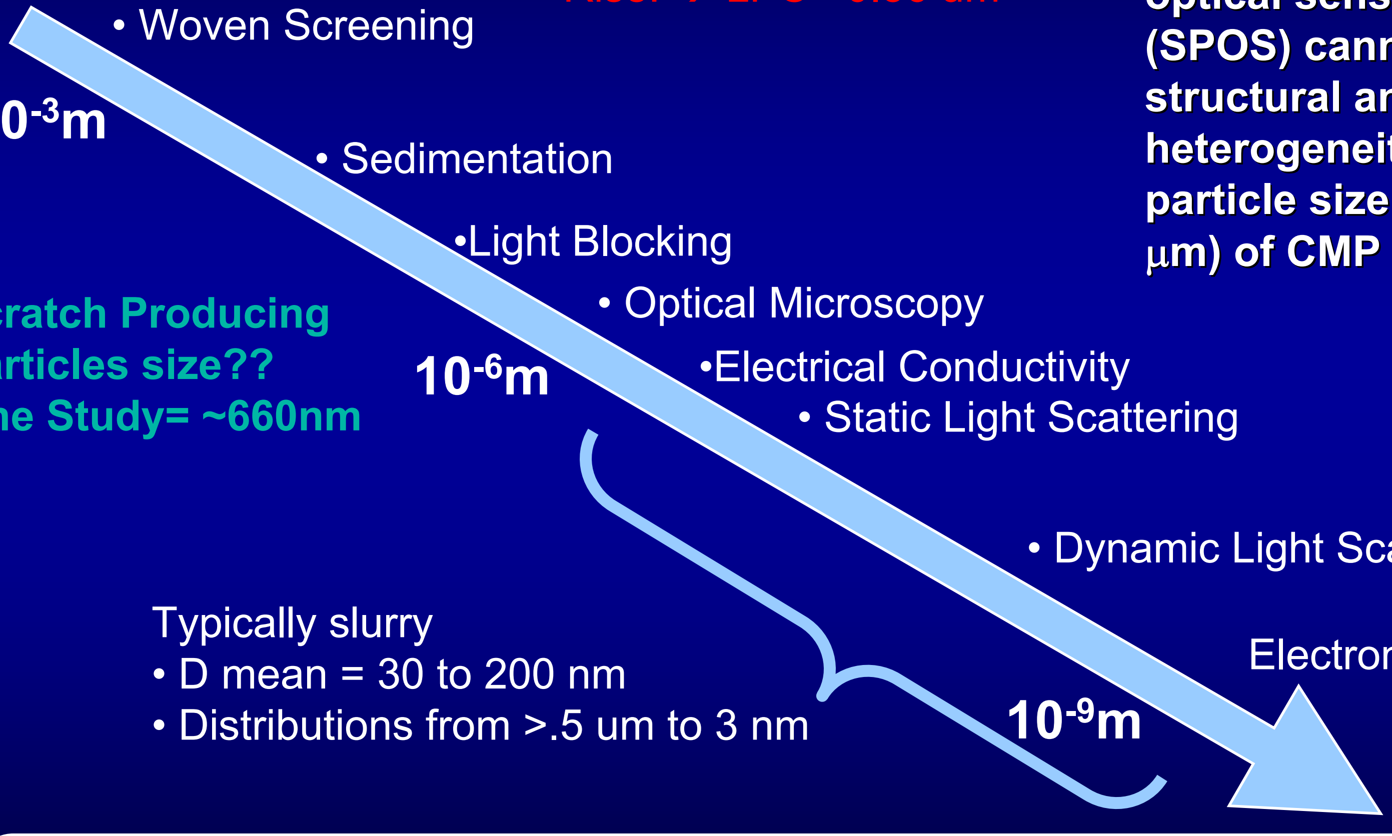
Key Trend in CMP: Softer, gentler polish

Courtesy of C. Barns

Particle Sizing Techniques versus Lowest (best) resolutions

In-line and POU particle Detection methods on the Rise! → LPC >0.56 um

Problem:
Current single particle optical sensing methods (SPOS) cannot characterize structural and morphological heterogeneities in the large particle size fraction (d > 0.5 μm) of CMP slurries



- Woven Screening

10^{-3}m

- Sedimentation
- Light Blocking
- Optical Microscopy

Scratch Producing Particles size??
One Study= ~660nm

10^{-6}m

- Electrical Conductivity
- Static Light Scattering
- Dynamic Light Scattering

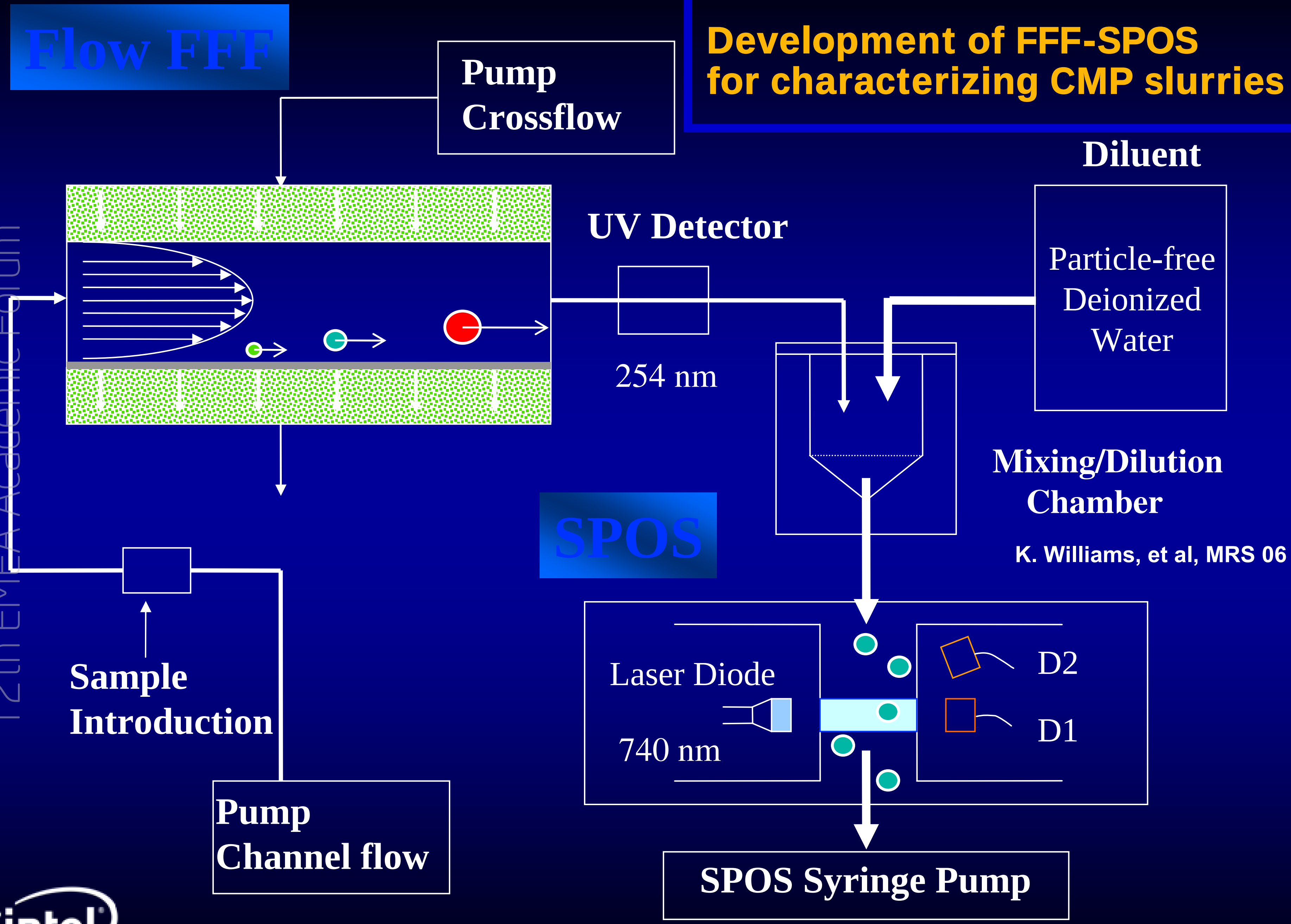
Electron Microscopy

10^{-9}m

Typically slurry
- D mean = 30 to 200 nm
- Distributions from >.5 um to 3 nm

There is a continuing need for new, improved methodologies designed to analyze the particle properties critical to CMP

Development of FFF-SPOS for characterizing CMP slurries



Flow FFF

Pump Crossflow

UV Detector

254 nm

Diluent

Particle-free Deionized Water

Mixing/Dilution Chamber

K. Williams, et al, MRS 06

SPOS

Laser Diode

740 nm

D2

D1

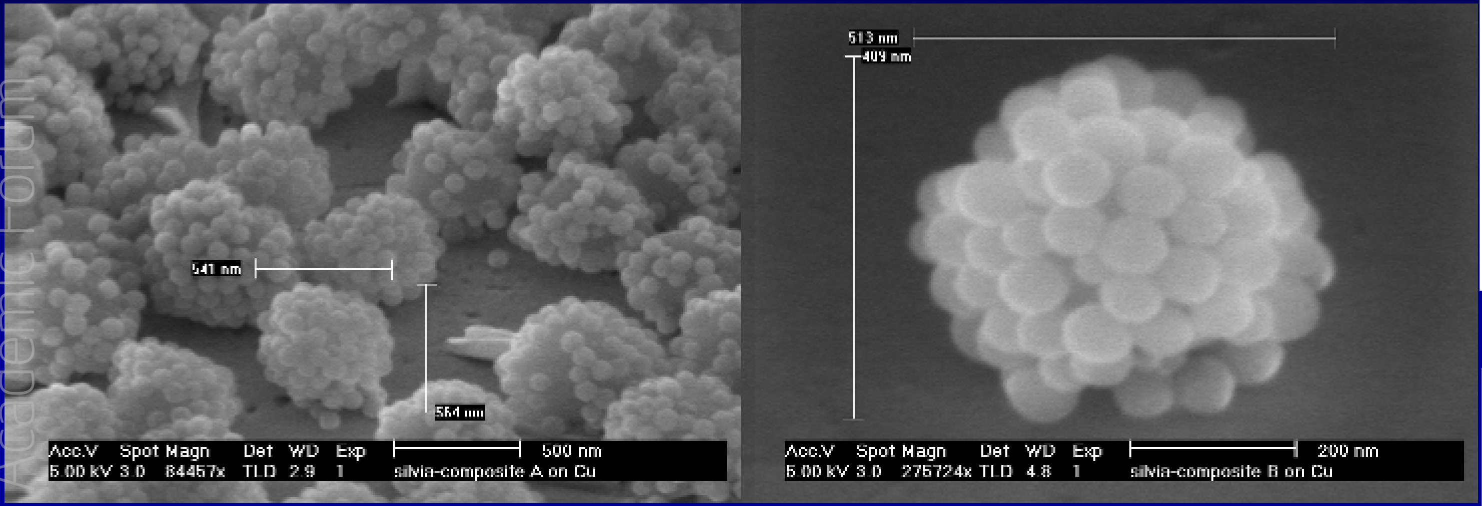
Sample Introduction

Pump Channel flow

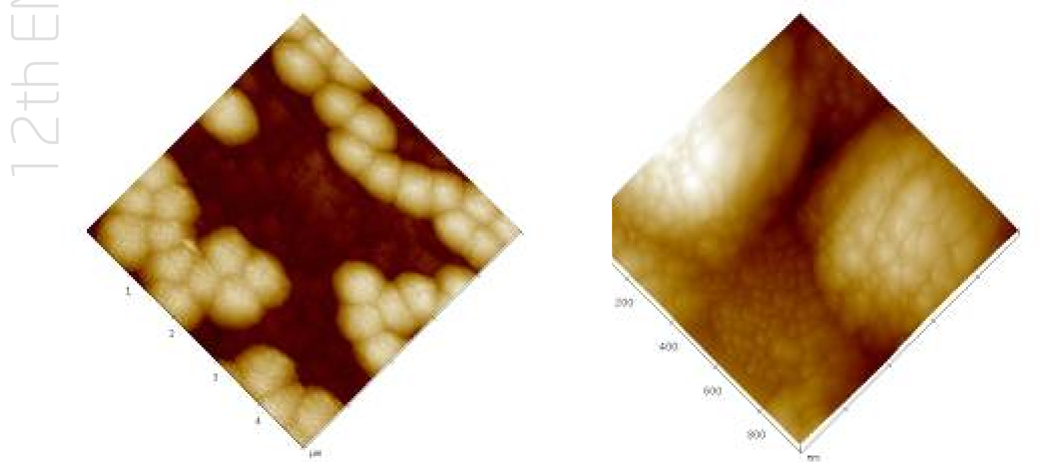
SPOS Syringe Pump

Role of Particle Adhesion & Hardness in CMP & Post CMP Clean

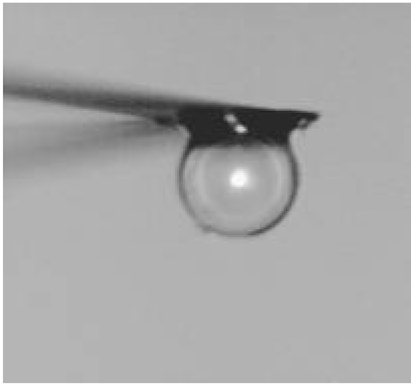
Courtesy of S. Armini , IMEC



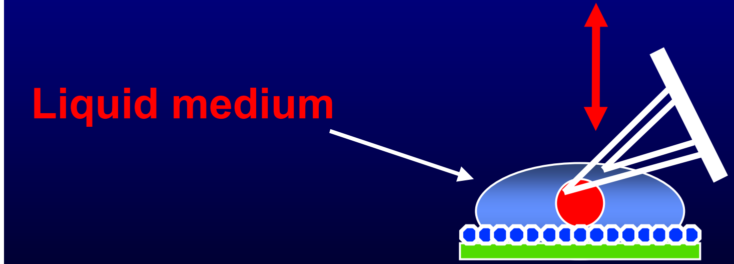
PMMA core (~350nm) + silica shell (~90nm)



Before CVD



After CVD



Courtesy of I. Luzinov , Clemson U

Composite Particles: Defect Studies

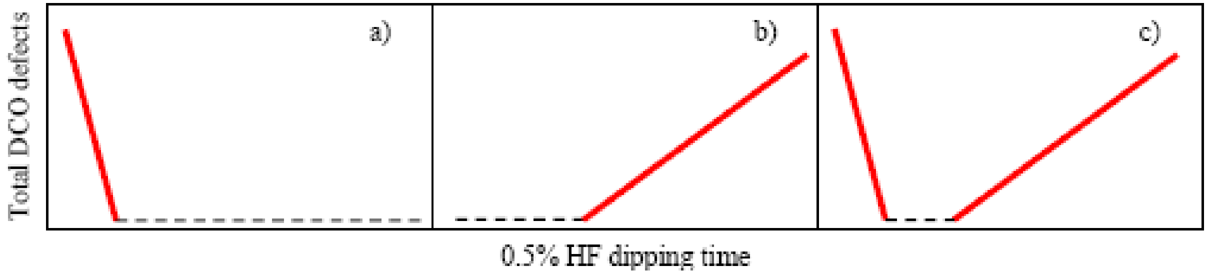


Figure 1. Expected trend of the total number of defects vs. diluted HF dipping time in the case of presence of a) residual slurry particles after CMP and polishing byproducts, b) shallow scratches after CMP, and c) their combination.

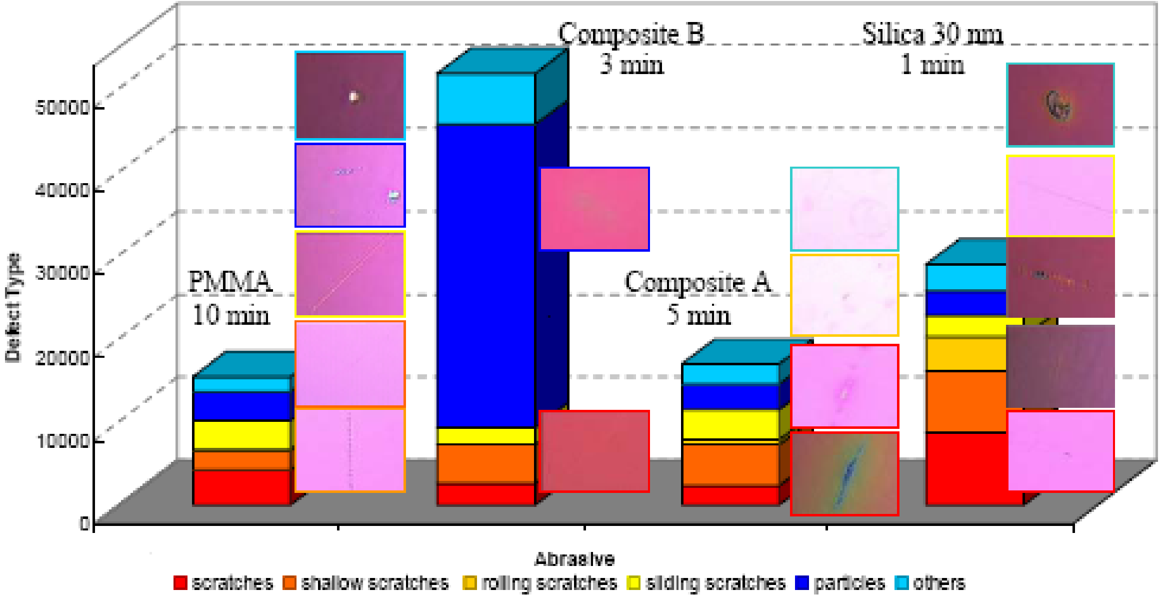
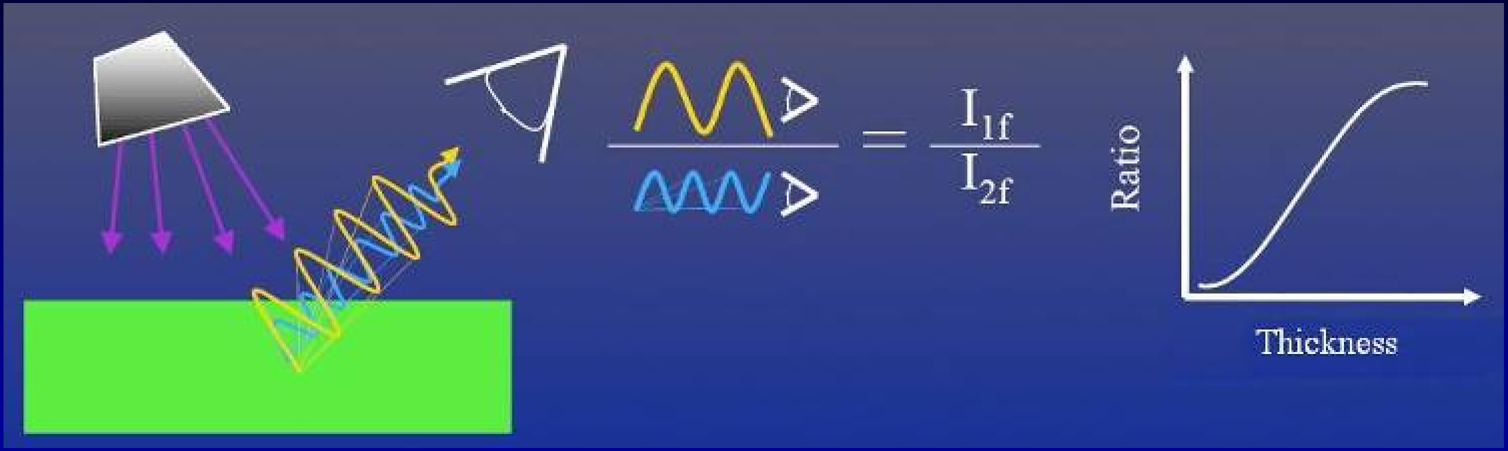
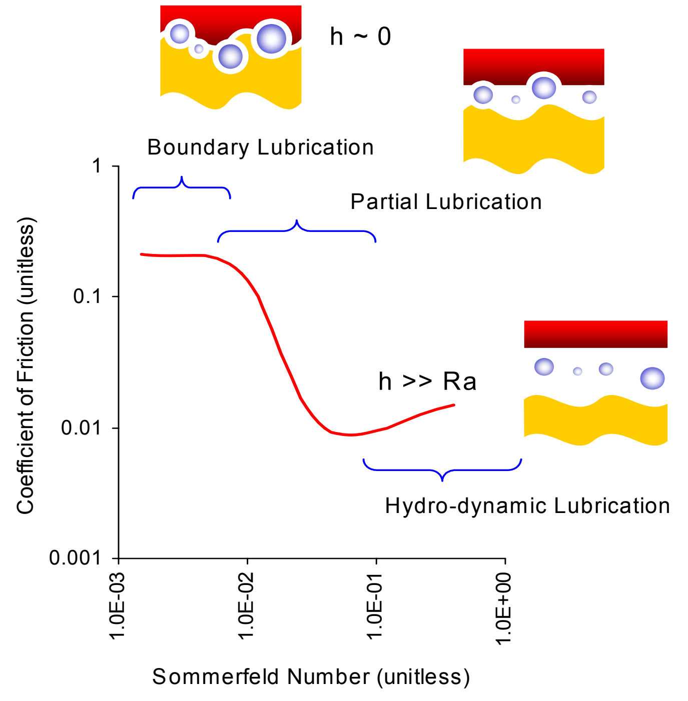


Figure 3. Defect quantification after CMP with different abrasive particles and experimental conditions.

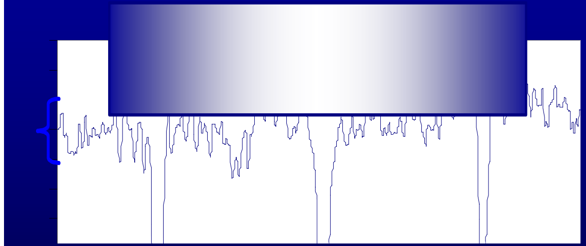
S. Armini, et al
CMPMIC & MRS 07

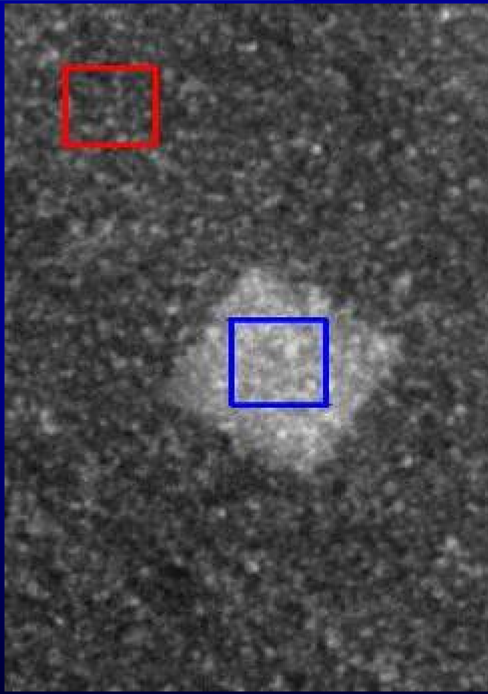
Real Time Pad / Slurry / Wafer Imaging Using Dual Emission Laser Induced Fluorescence





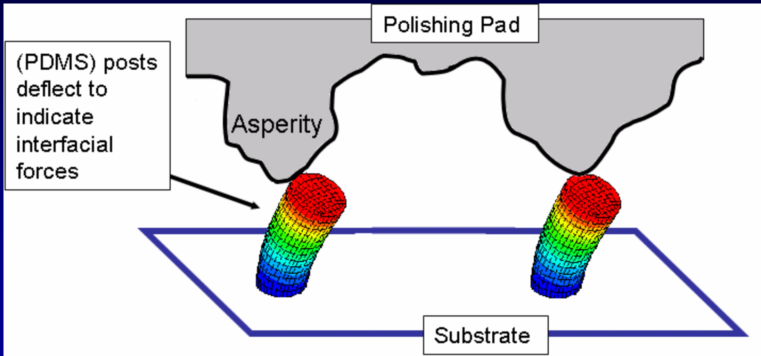
$$So = \frac{(u)\times(\mu)}{(P_{act})\times(\delta_{eff})}$$

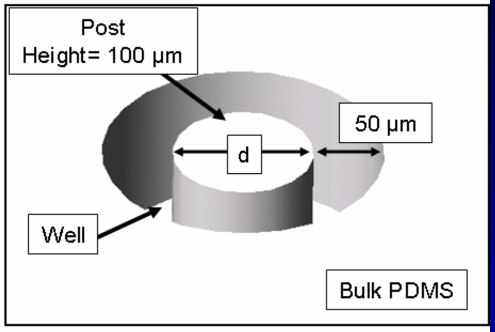




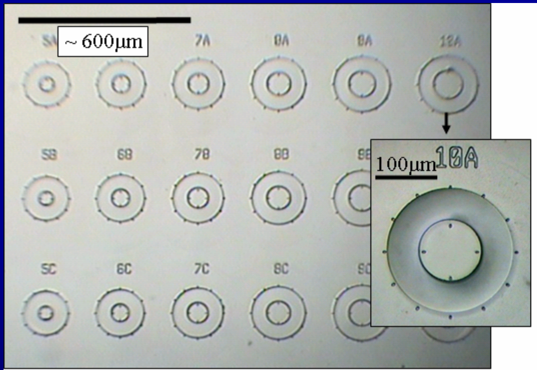
C. Gray, et. al, 2005 CMP-MIC & MRS

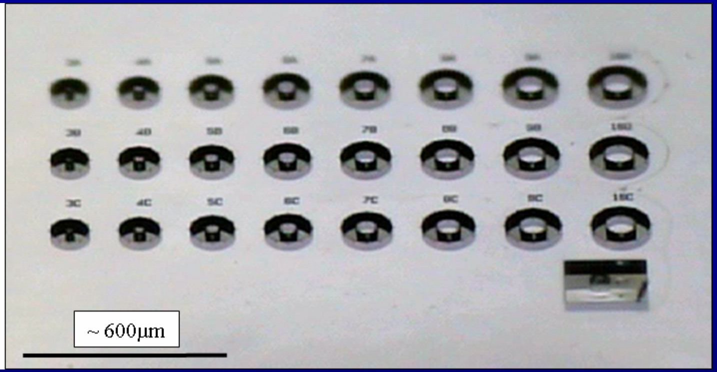
Local Pad / Wafer Contact forces during CMP





Polydimethylsiloxane (PDMS) posts deflect due to shear forces. The basic unit of the shear stress sensor is the recessed micro post . An array of posts with as-designed height 100 microns, and varying diameter, d,



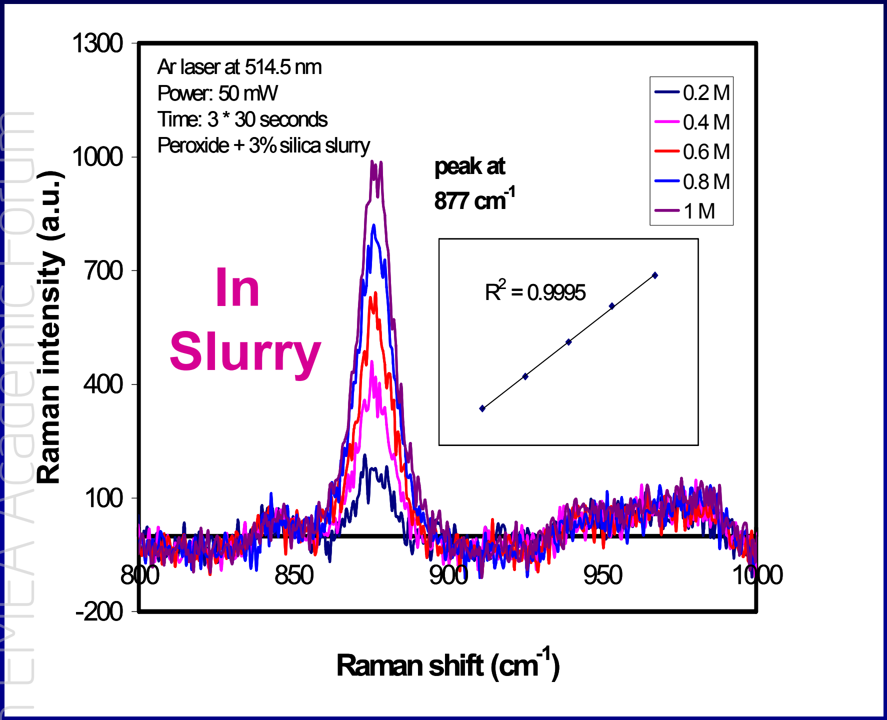


A. Mueller, et al
MRS 2007

COF Values (measured) = 0.3 (+/- 0.03) → Total shear force on wafer = 30N
At applied static pressure of 1.7 Psi, an IC1000 PAD/wafer contact is only ~ 0.7 %
Through pad asperities (from literature)
Mean radius of contact between single asperity & wafer = 5 µm
→ The sensor will be in contact w/ ~ 700,000 pad asperities!
→Mean force delivered by single asperity = ~ 40 µN
→Sensors designed to handle range of 4-400 µN → PDMS post deflection 5-50 um

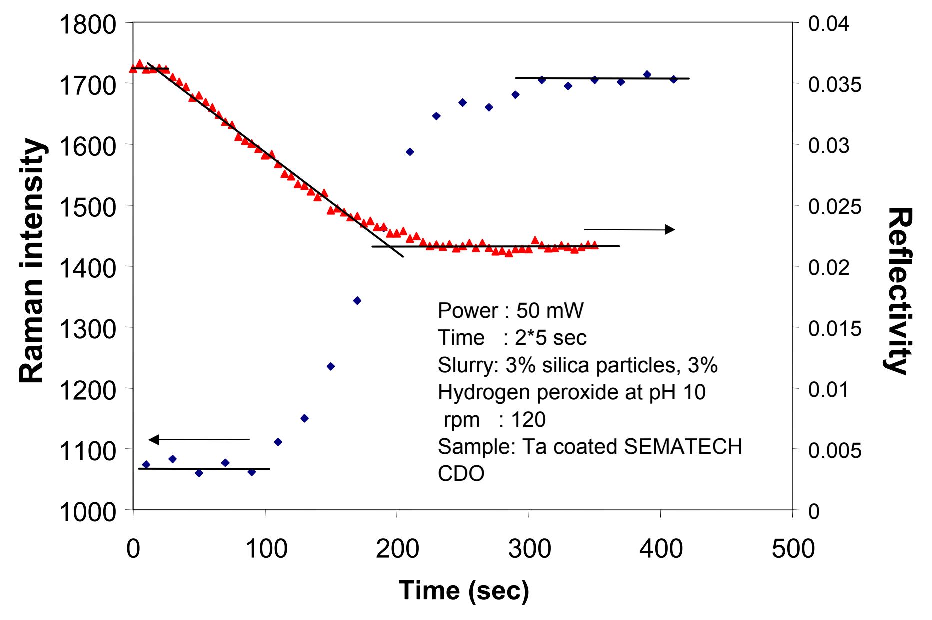
In situ Raman measurements of chemical species: H2O2 Concen.

S. Raghavan et al, Univ. Of AZ, MRS Proceed., 05 & 06



- Raman measurements were taken from the space (~300μ) between the wafer and the sapphire window, *in-situ*

Comparison of Raman to reflectivity (*In situ* measurements)

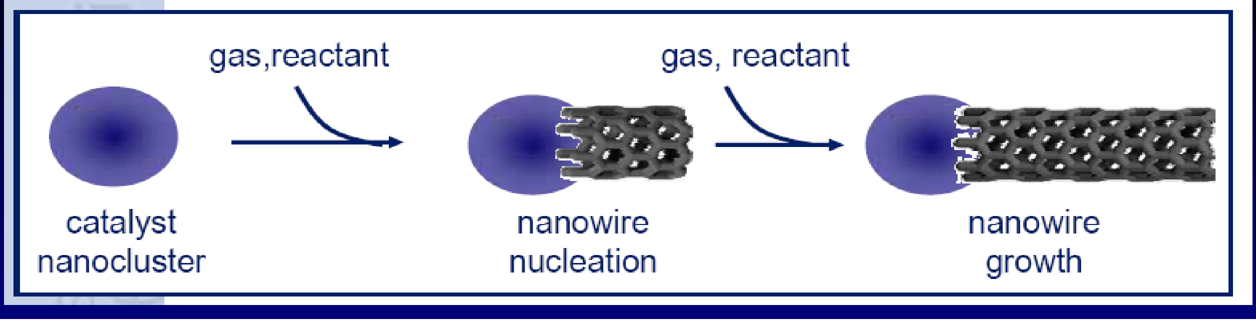


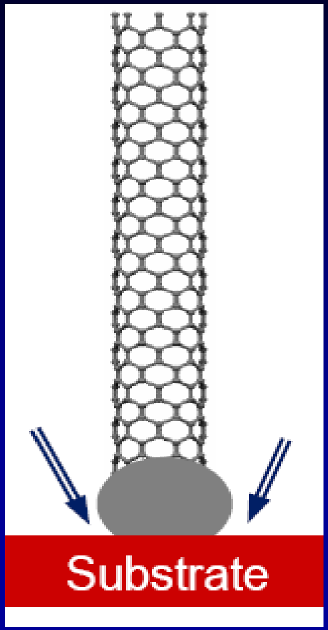
- **Exponential increase in Si peak intensity as Ta removed.**
- **Raman is more sensitive than reflectivity in sensing Ta removal.**

Why CNTs for IC applications?

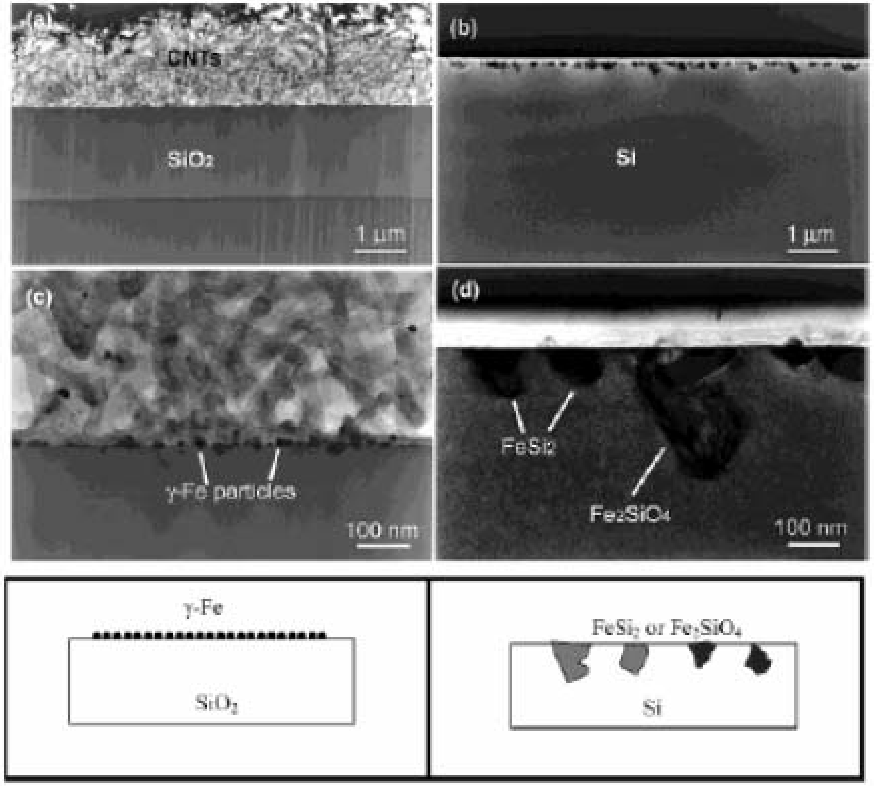
- **Transistors (semiconducting nanotubes)**
  - Single-walled (SW-) CNTs are a novel material that exhibit high hole mobility in devices.
  - Compatible with the Tri-gate architecture.
  - Complimentary research-grade FETs demonstrated, integration conceivable.
- **Interconnects (metallic nanotubes)**
  - Nearly ideal 1-D character with long scattering length (at low bias).
  - Current density without failure: 10^9 A/cm2 (c.f. Cu 10^6 A/cm2).
  - Good mechanical stability (strength/toughness)
- **Unique Properties**
  - SW-CNT size (diameter ~ 1-2nm) chemically controlled
  - Resistant to many standard IC processes (HiK, top gate…)
  - Mechanical strength (~100x steel @ 20% weight)
  - Electrical conductivity (~ Cu, 1000X EM of Cu)
  - Thermal Conductivity (~3x diamond)
  - Improved mobility (~60x electron, ~200x hole)
  - Chemical stability: can be “functionalized” via organic chemistry

CNT Growth on various substrate

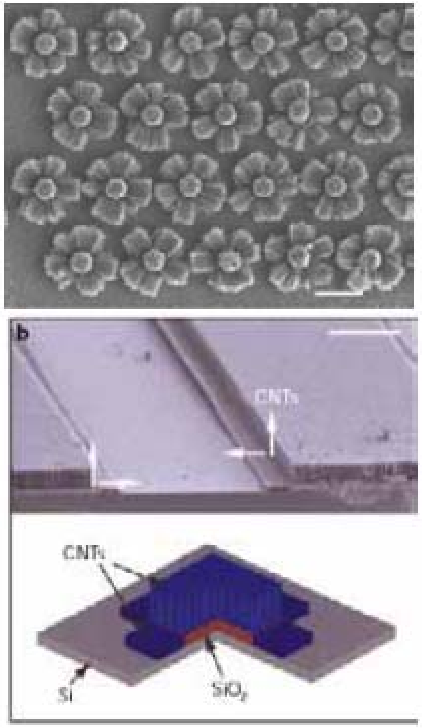




G.S Dusberg, Infineon, 2003

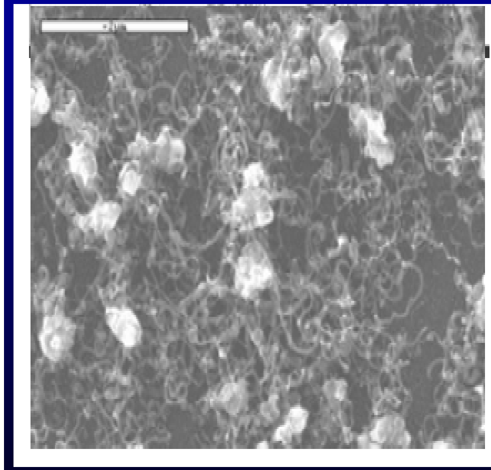


Jung et al. Nanoletters, 4, 2003



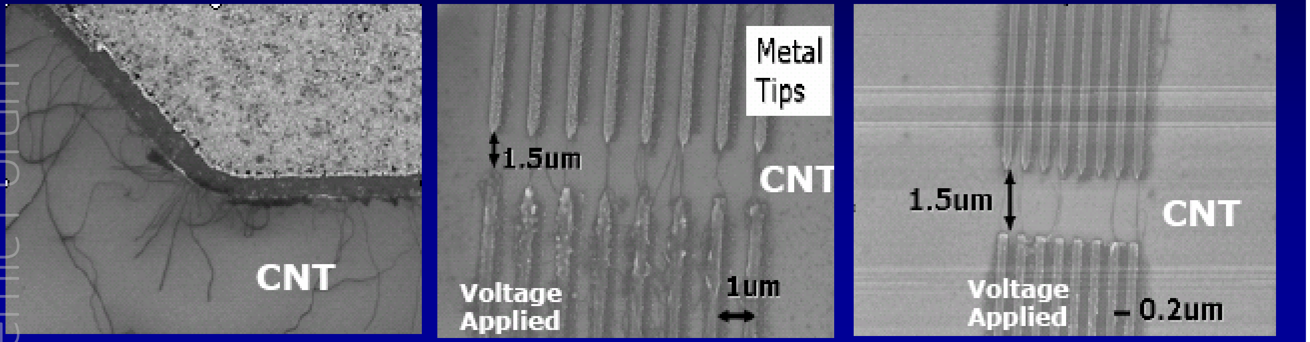
Wei et al., Nature, 416, 495, 2002

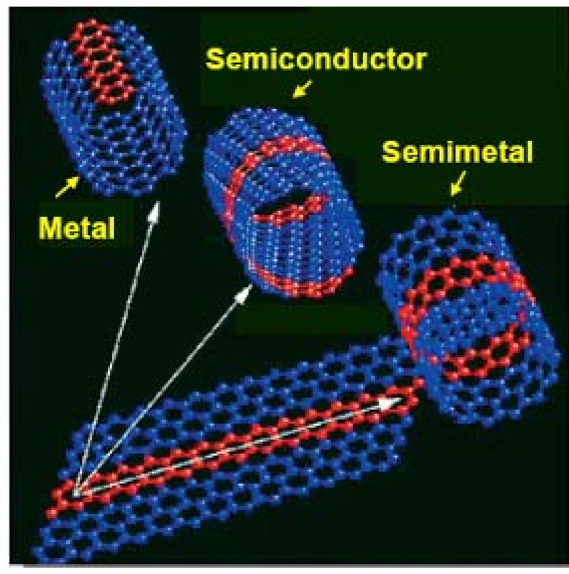
Various Metal Catalysts: Fe, Ni, Co, Ru, Mo, Pt, Ir



TaN

Fundamental Issues for CNTs: Assembly / Alignment and Chirality





- Good progress has been made in assembling bottom-up chemically synthesised CNTs
- Assembly / Alignment
  - In 2015 a leading edge logic device might have >50B transistors
  - Placement requirements of a few nm with error rates $<<10^{-14}$
- Still many problems to solve before transistor arrays can be made for VLSI

Chirality

- (*n*, *n*) tubes are metal;
- (*n*, *m*) tubes with $n – m = 3j$ ($j = 1,2,…$) are very tiny–gap semiconductors;
- (*n*, *m*) tubes with $n – m = 3j \pm 1$ are large–gap semiconductors (ca. 1.0 eV for dt ca. 0.7 nm).

S. Sato, et al
Fujitsu LTD

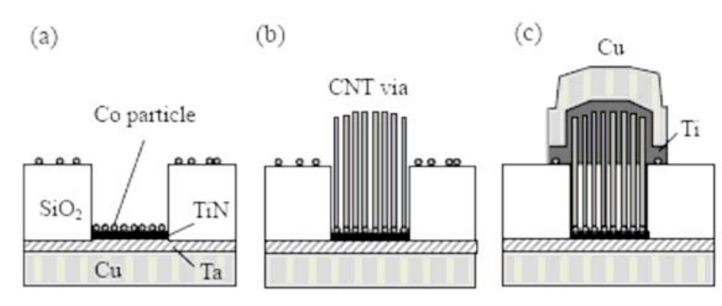


Fig. 1. CNT via process: (a) Fabrication of via hole structure and deposition of Co particles; (b) CNT growth; (c) Deposition and patterning of the top layers

How can we measure the density of NTs in an array?
How can we test the electrical properties?

Areas of emphasis for External Research

- **Cu-low k extendibility:** evolutionary solutions.
    - Metal.
    - Dielectrics.
        - ILD Repair
        - Materials Engineering (e.g. Polymer Low K)
- **Unit processes:**
    - Metal deposition.
    - Etch and cleans.
    - Planarization.
        - Direct Low K CMP, softer-gentler polish
- **Novel interconnect solutions:** beyond conventional metal/dielectric.
- **Reliability:** electrical and mechanical.

- **Unit processes:**
  - **Metal deposition**
    - **Gap fill for 10:1 aspect ratios for line widths below 30 nm (0.7x40 nm), with minimal overhang.**
    - **Barrier and seed layers: thin (< 3 nm), conductive, conformal, smooth (e- scattering) and "electroplatable" barrier/seed layers.**
  - **Etch and cleans.**
  - **Planarization**
- **Novel interconnect solutions:**
  - ☒ **Optical, CNT**
- **Reliability: methods to improve electromigration and stress voiding with minimum impact to interconnect resistance.**
- **Architecture/Design: create architecture solutions to handle significant resistivity increases and non scaling k.**