The end of CMOS scaling – when?

M. Brillouët

Ireland Summer School for Nanotechnology 2011 – Dublin – Aug. 28 to 30, 2011

Outline

How can the new materials and device architectures help?
What are the key challenges, e.g. manufacturability, or affordability?
What are the constraints, patterning, materials, or simply the physics?

- Basics in CMOS scaling
- What fuels the scaling?
  - Higher integration density
  - Material engineering
  - Device architectures
- What could stall the scaling?
  - Lithography / affordability
  - Material engineering
  - Physical limits
- Conclusion

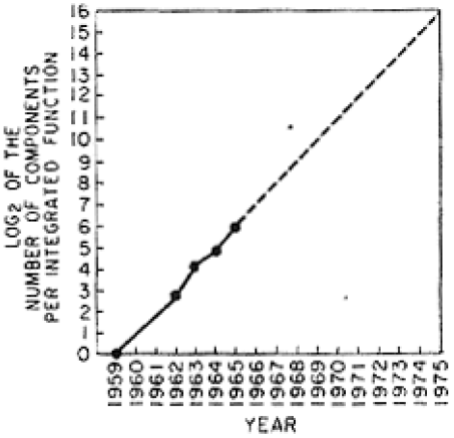
Basics in CMOS scaling

What Gordon Moore actually said?

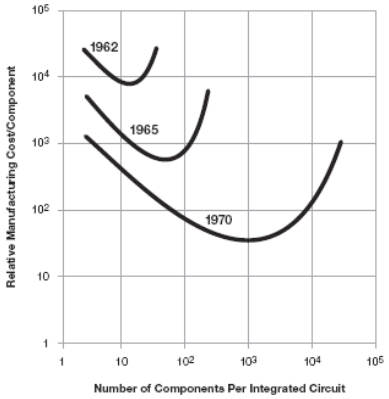
G. Moore - 1975

Higher integration density

nologies were first investigated in the late 1950's. The object was to miniaturize electronics equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including



More at lower cost



Digital revolution

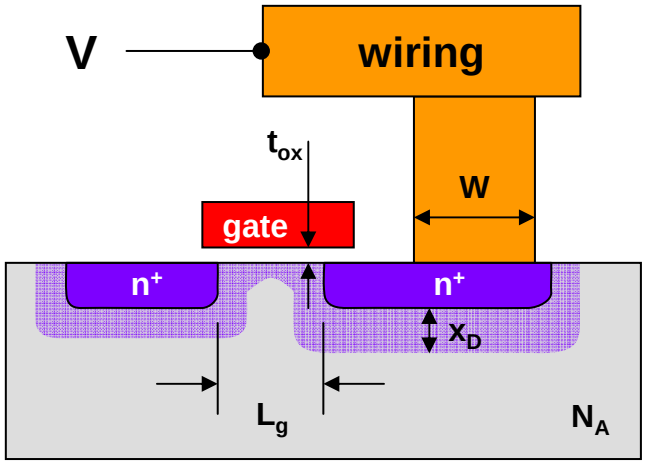
Integration will not change linear systems as radically as digital systems. Still, a considerable degree of integration

no reference to performance increase

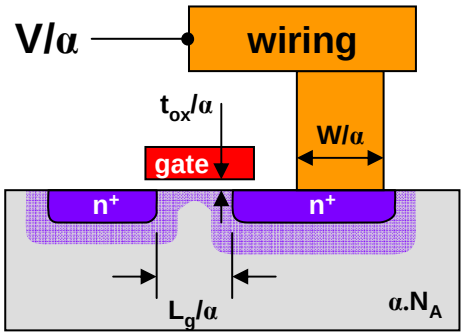
G. Moore Electronics Vol.38 (8) April 19, 1965

The happy scaling

R. Dennard © IEEE



dimensions t_{ox}, L, W	$1/\alpha$
doping	α
voltage	$1/\alpha$
integration density	α^2
delay	$1/\alpha$
power dissipation/Tr	$1/\alpha^2$



The happy scaling

R. Dennard © IEEE

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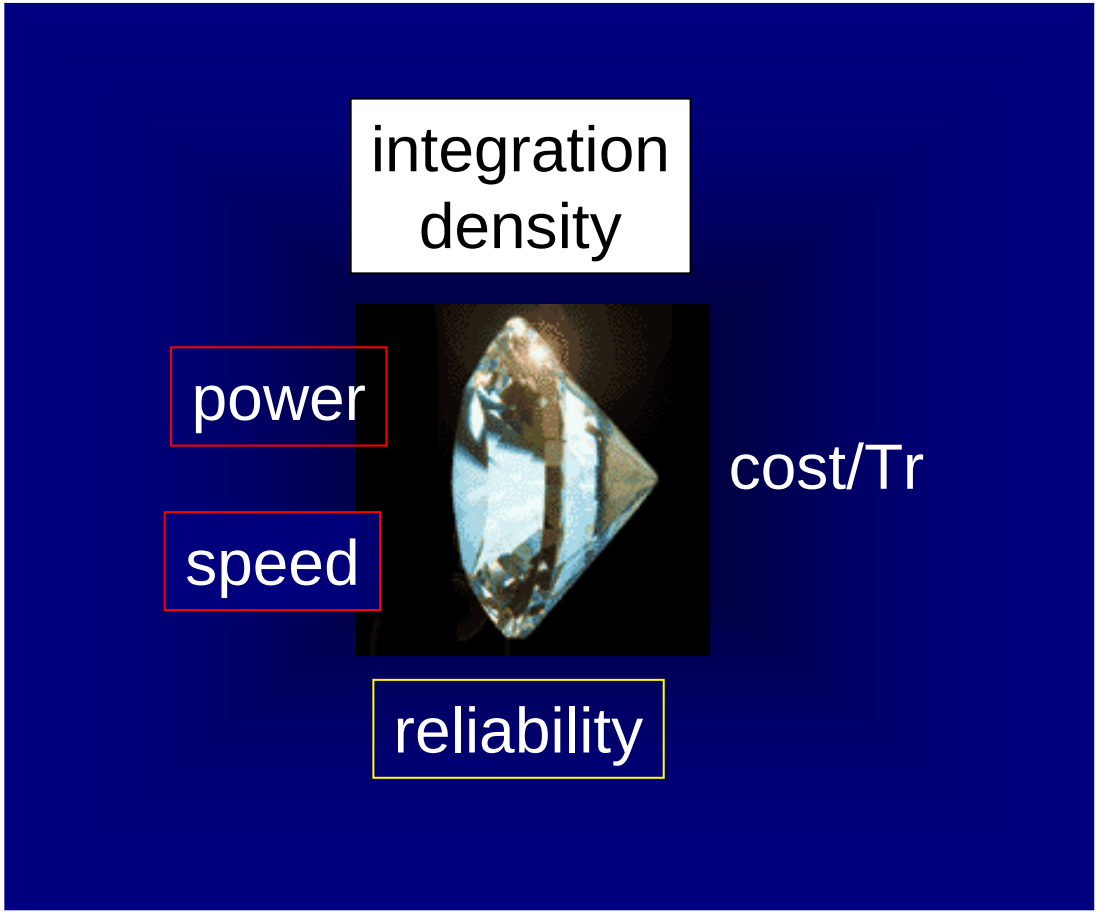
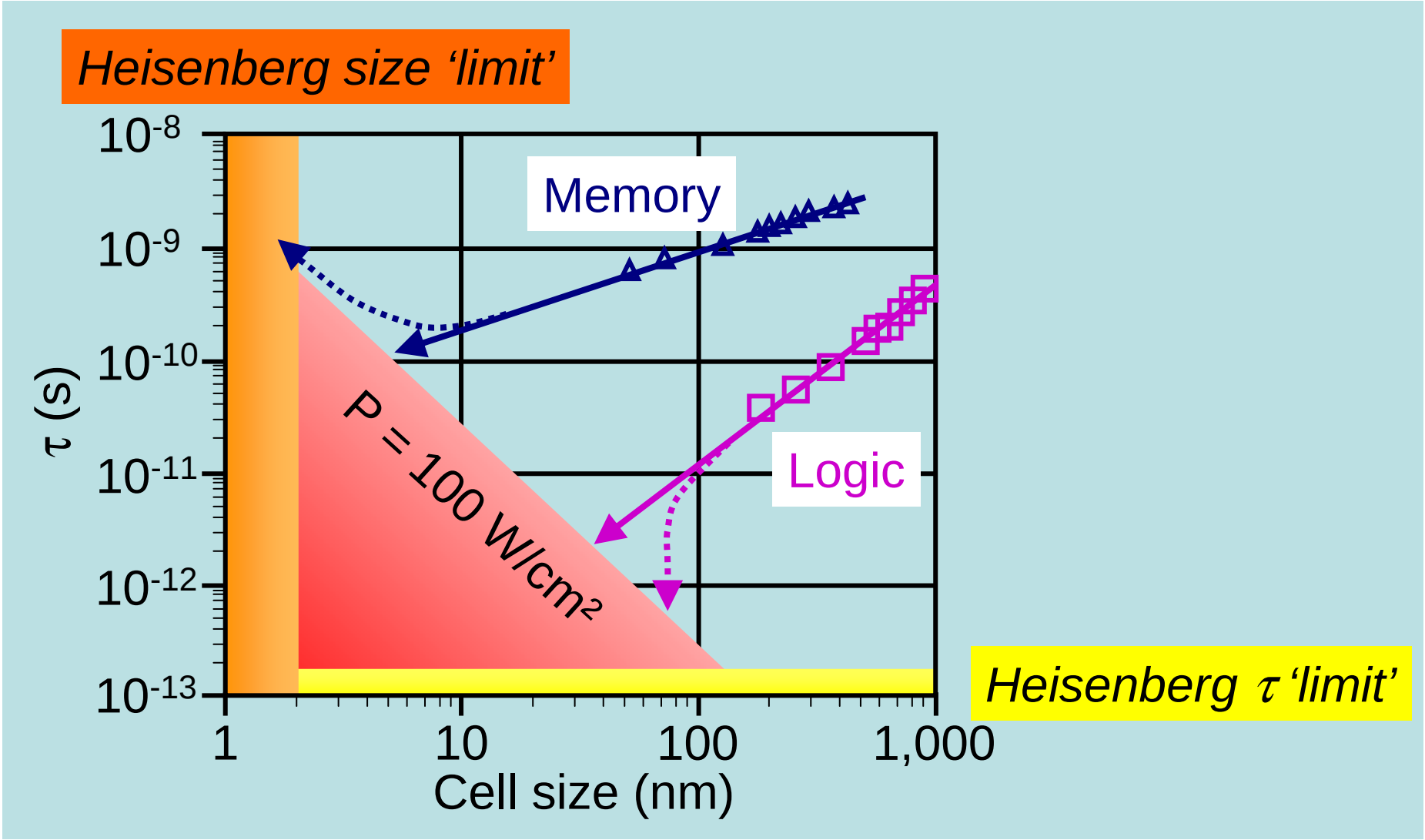


Diverging priorities



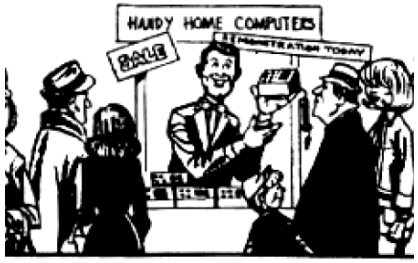
after Zhyrnov

Logic scaling

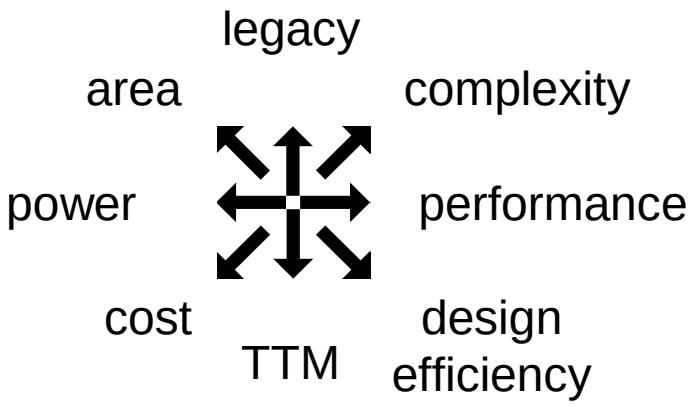
Device view

power ⟺ performance

Product view



from G. Moore Electronics Vol.38 (1965)



after K. Schrüfer VLSI-TSA Short Course 2011

Power – performance trade-off

Active power

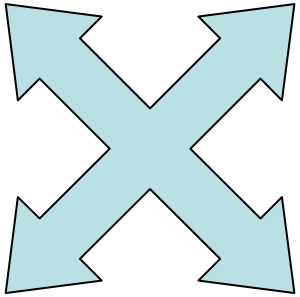
$$P_{dyn} = \alpha \cdot f \cdot C \cdot V_d^2$$

$$\propto V_d^3 \text{ for } f \propto V_d$$

Standby power

$$P_{stat} = I_{leak} \cdot V_d$$

$$\propto V_d^k, k = 4...6$$



Performance

$$f = 1/T \approx \frac{(V_d - V_t)^\alpha}{V_d \cdot C}$$

$$\propto V_d \text{ for } V_d > V_t$$

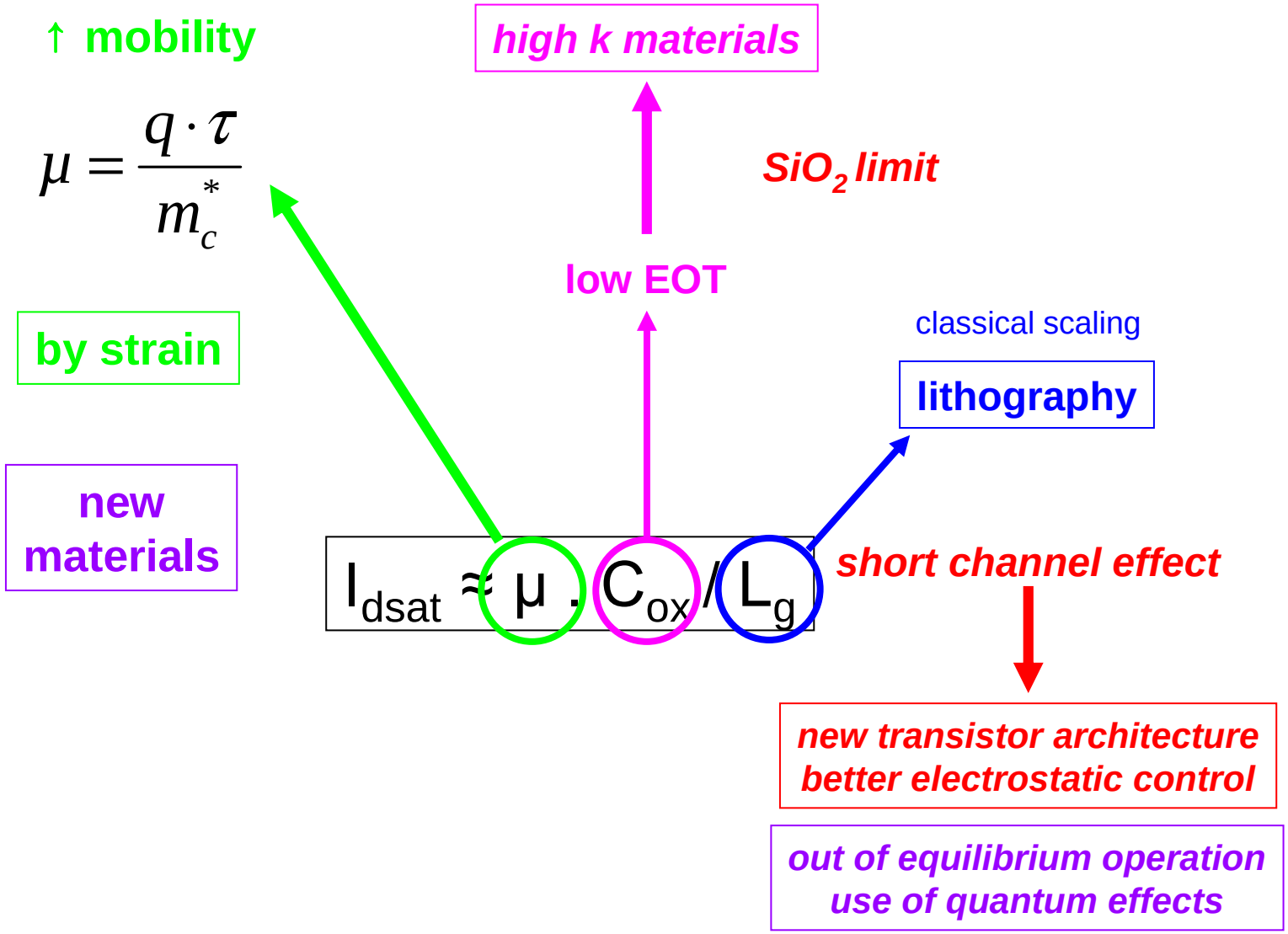
Variability & reliability

$$\sigma = syst. + random$$

$$V_d(t) = V_{d,nom} - \Delta V_{d,IRdrop}$$

after K. Schrüfer VLSI-TSA Short Course 2011

Equivalent scaling for logic devices



Memory drivers

Memory cell = multiple stable and noise-immune states
which can be externally switched and measured

Drivers

#1. Integration density → { Aggressive dimension scaling; Move into the 3rd dimension }

#2. Power consumption (read, write, store)

#2. Speed #2. Non-volatility

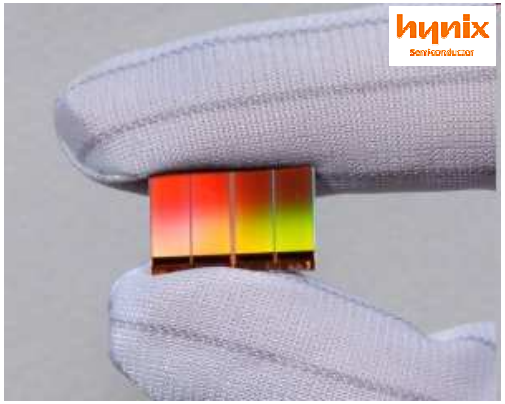
#3. Correction of defective storage

The segmented memory universe

Dense → **DRAM**
Scalable
Non volatile → **NAND, NOR**
Fast → **SRAM**
Low power
Reliable
Cheap

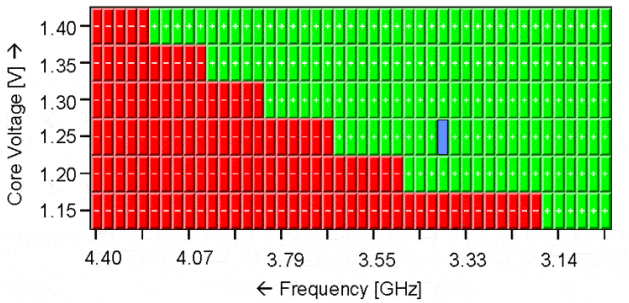
few publications
few pictures
below ≈ 45nm

25nm 2Gb DDR3 DRAM



26nm 64Gb MLC NAND

Courtesy: Intel



256Mb SRAM

The quest for the “universal” memory

Dense
Scalable
Non volatile
Fast
Low power
Reliable
Cheap

Q

flash

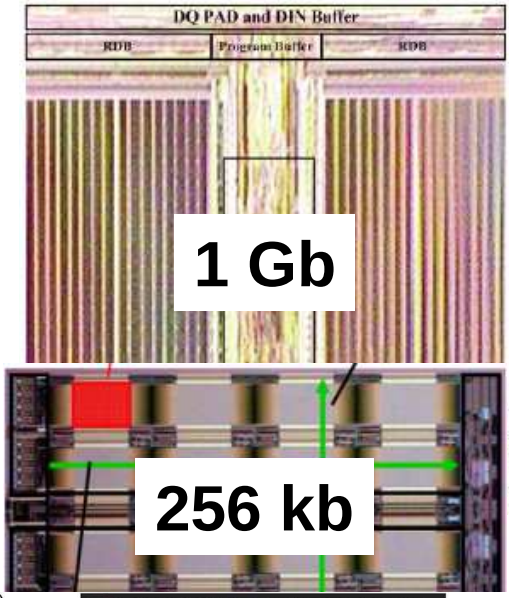
FeRAM

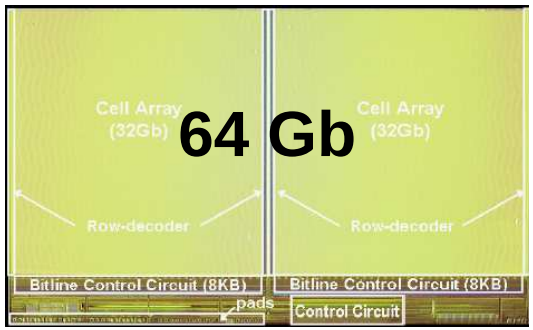
R

PCRAM

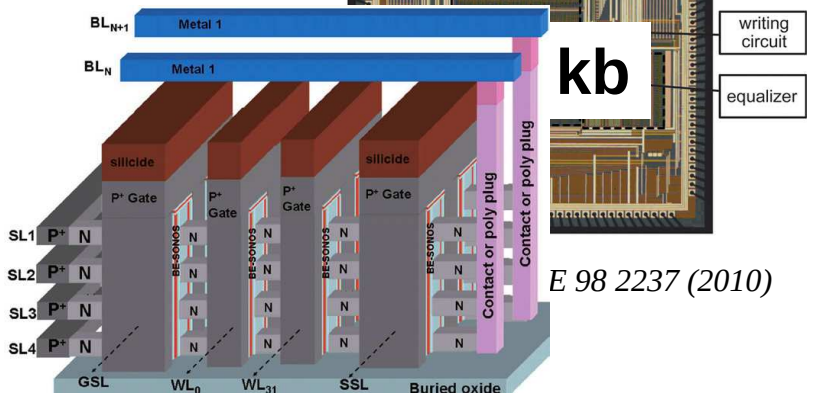
STTRAM

ReRAM





K. Fukuda et al.
ISSCC 2011 #11.1



E 98 2237 (2010)

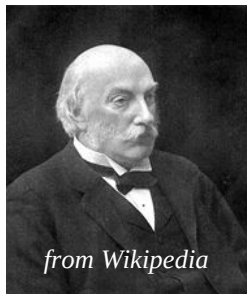
CH. Hung et al. VLSI 2011 #4B-1

Fueling the scaling trend

Higher integration density

Lithography as an enabler

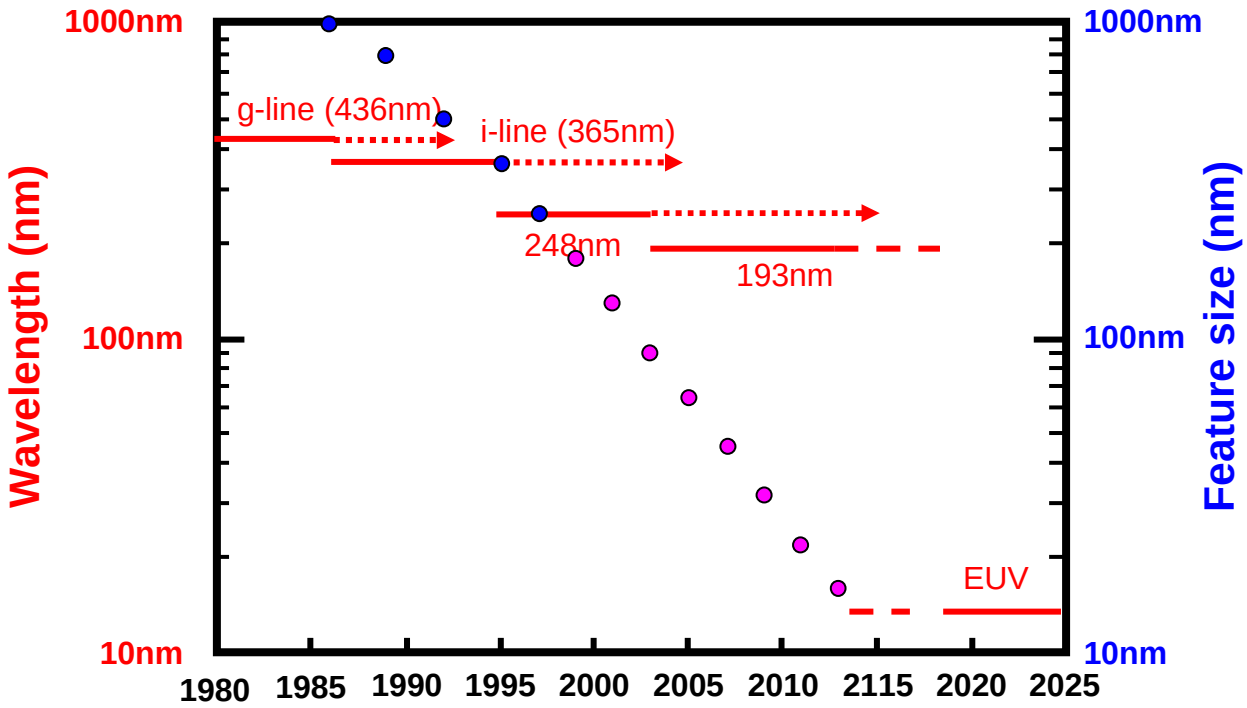
Lithography: forget classical limits



Rayleigh's criterion

$$R = 1.22 \cdot \frac{\lambda}{NA}$$

Work on
- mask
- illumination
- resist
- etc.



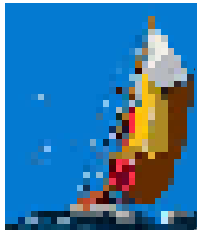
Lithography: the key enabler

High integration density

Resolution

Depth of focus

Overlay



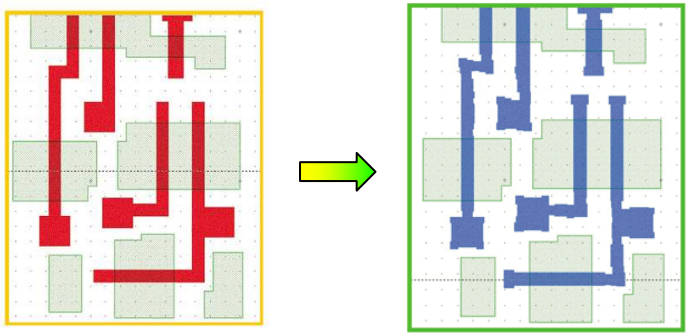
Resolution Enhancement Techniques

$\downarrow \lambda$ (193nm → ~~157nm~~ → **EUV**)

$$R = k_1 \cdot \frac{\lambda}{NA}$$

high NA optics

$$DOF = k_2 \cdot \frac{\lambda}{(NA)^2}$$



from Future Fab vol.16

Material engineering

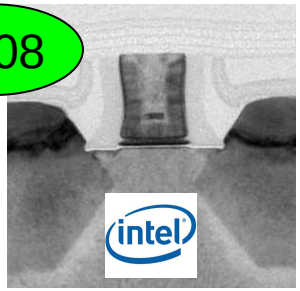
High k – metal gate

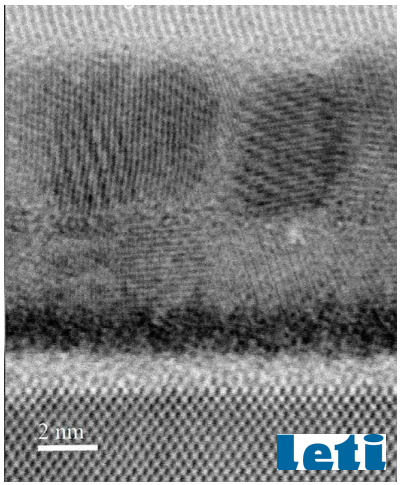
SESSION 14

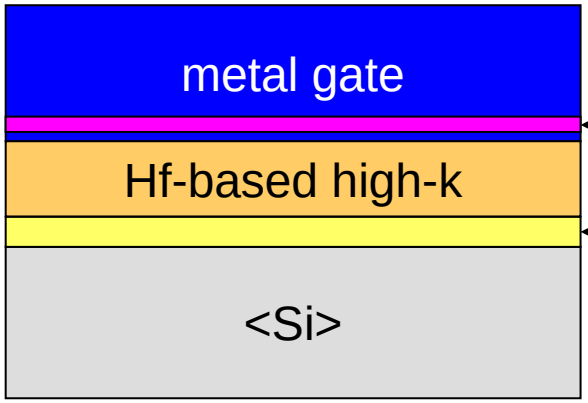
Device Interconnect Technology –
High K Gate Dielectrics/Metal Gate

Tuesday, December 8, 9:00 a.m.
Imperial Room

1998 → 2008







+ O control

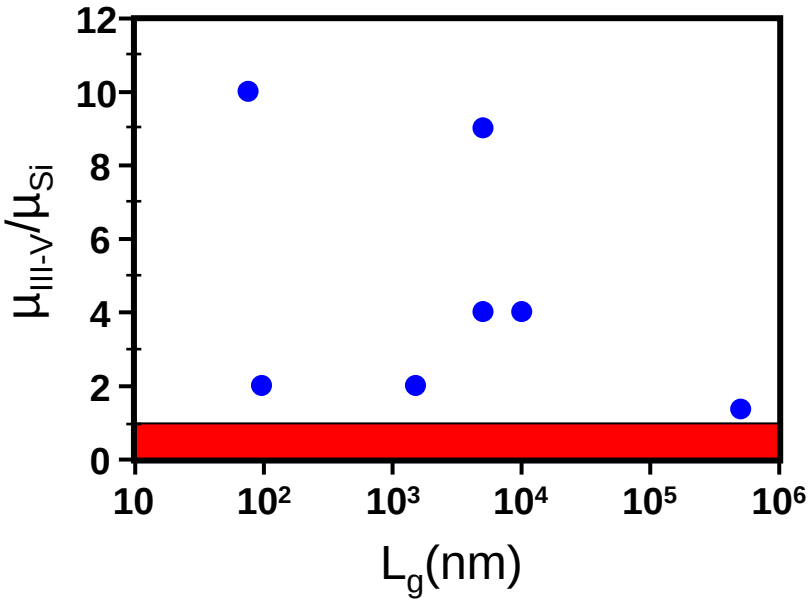
metal cap/doping for φ_m control

SiO_x interfacial layer

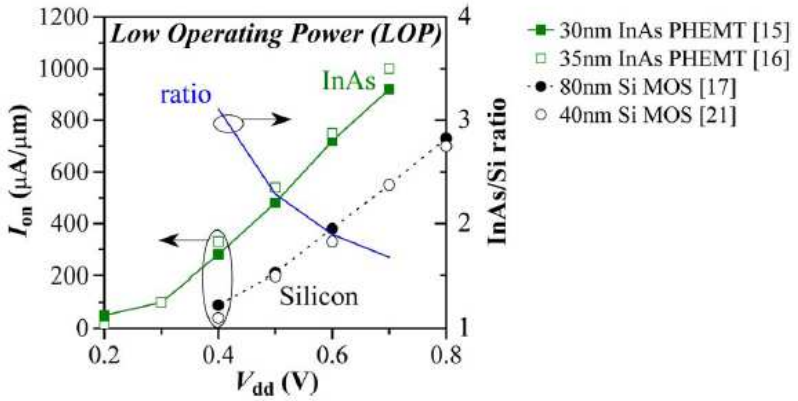
III-V

Material	Si	Ge	GaAs	InGaAs	InAs
μ_e ($cm^2V^{-1}s^{-1}$)	1350	3600	8000	**11200**	30000
μ_h ($cm^2V^{-1}s^{-1}$)	480	**1800**	300	300	450

from A. Lubow et al. APL 96 122105 (2010)



from T. Skotnicki IEDM Short Course 2010



from G. Doornbos et al. IEEE EDL 31 1110 (2010)

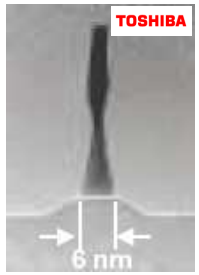
Device architectures

Ultimately scaled CMOS: no limit?

S.Deleonibus et al.
IEEE EDL 2000

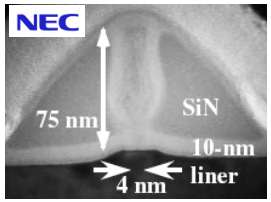
L_g = 25nm

N. Yasutake et al.
VLSI 2004 #9.1



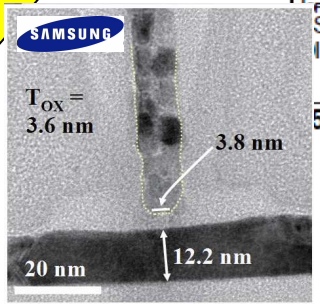
L_g = 10nm

H.Wakabayashi et al.
IEDM 2003 #20.7
Nanotech 2004

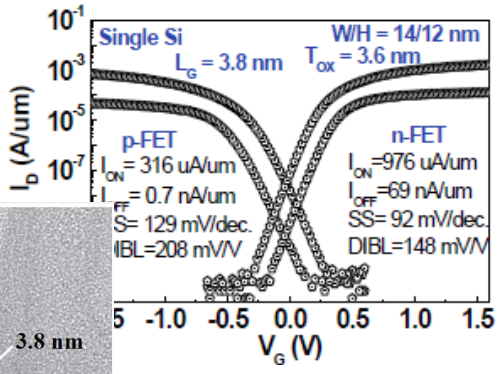


L_g = 5nm

SD Juk et al.
VLSI 2009 #7.4

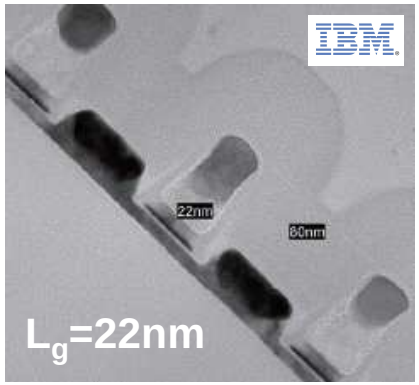


L_g = 3.8nm

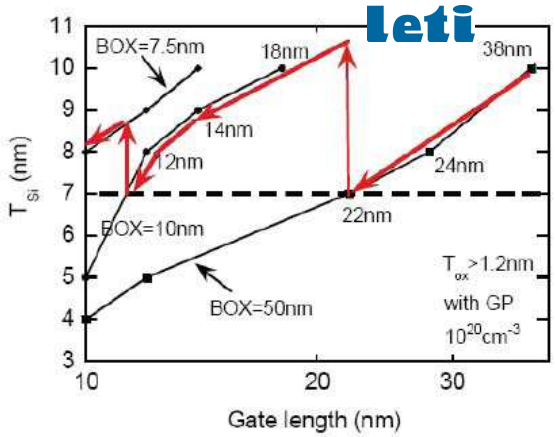


…and new architectures have their own scaling paths down to 10nm

FDSOI

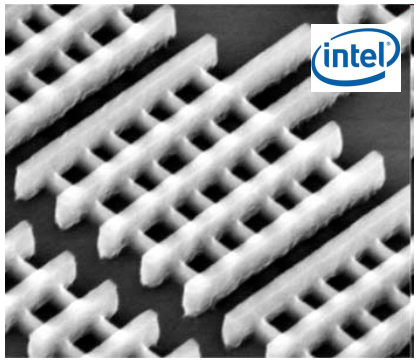


from K. Cheng et al. VLSI 2011 #7.1

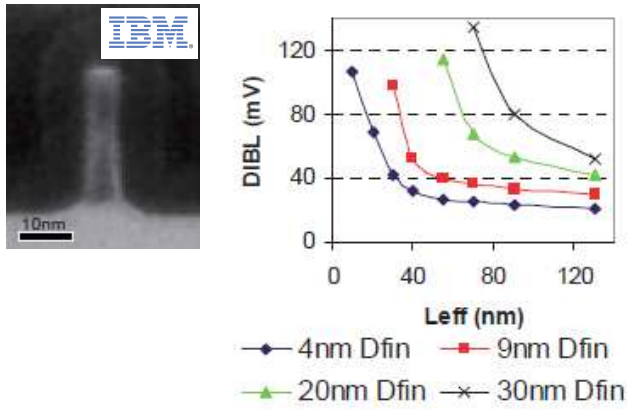


from L. Clavelier et al. IEDM 2010 #2.6

FinFET



22nm CMOS

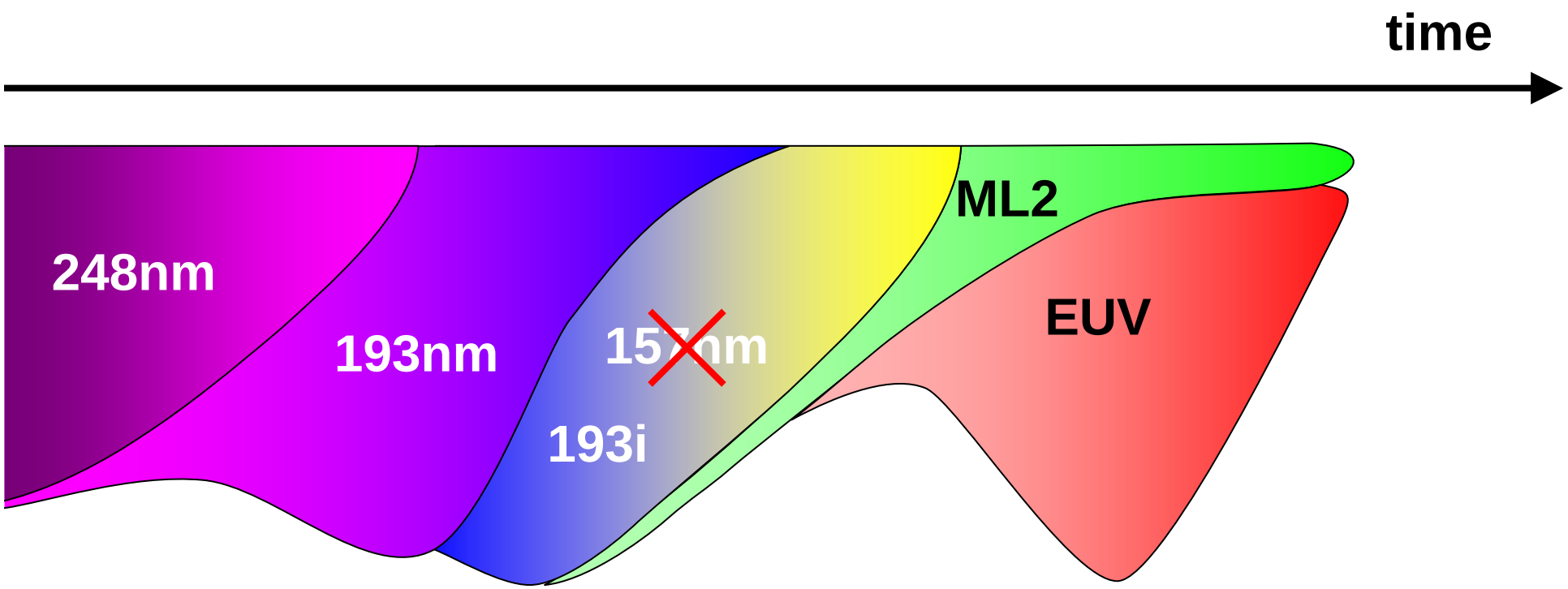


from JB Chang et al. VLSI 2011 #2A-1

Can the scaling stall?

Lithography

Lithography: a 2005 vision



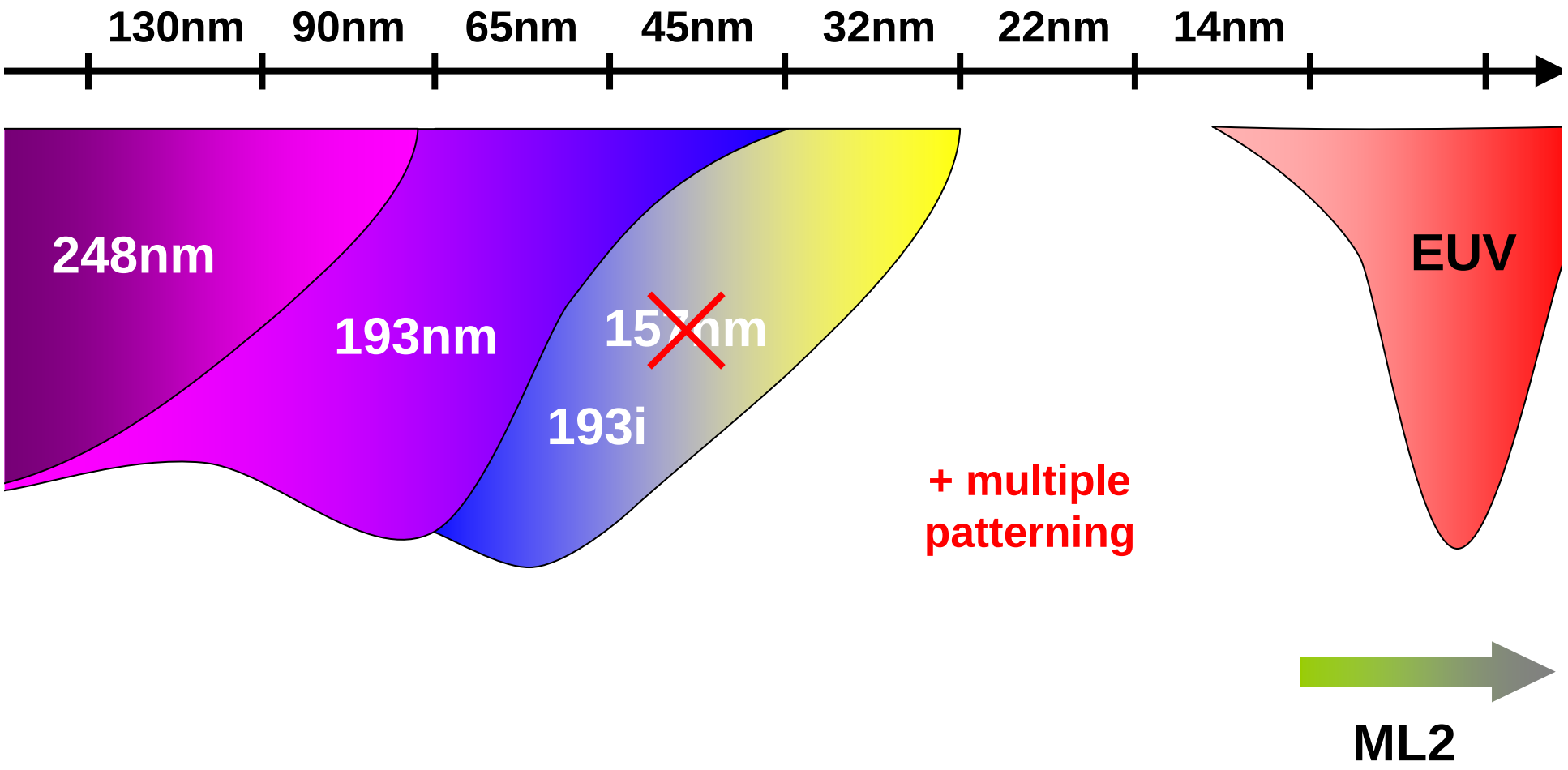
disruptive technologies?

from

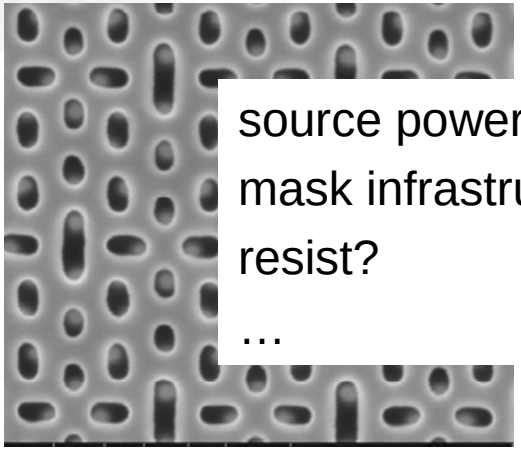
niac

Strategic Research Agenda

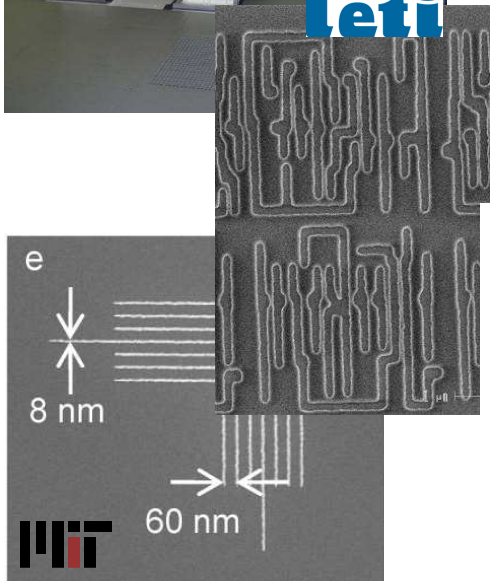
Lithography: present perspective



NGL: "α-tools"and β-tools" exist, but…



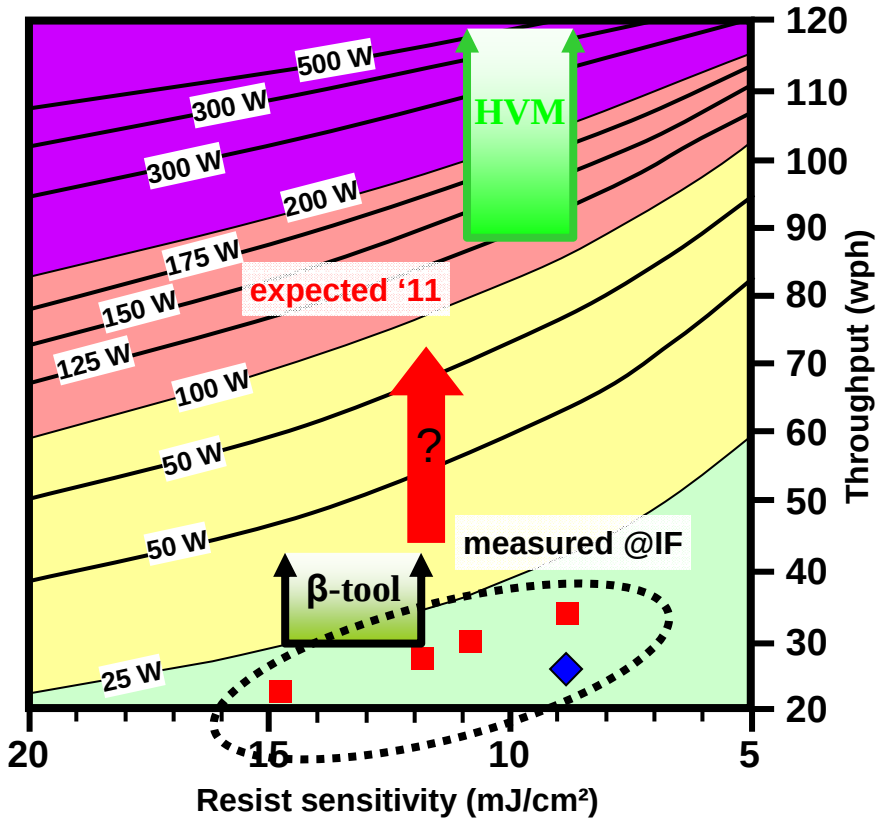
source power?
mask infrastructure?
resist?
…

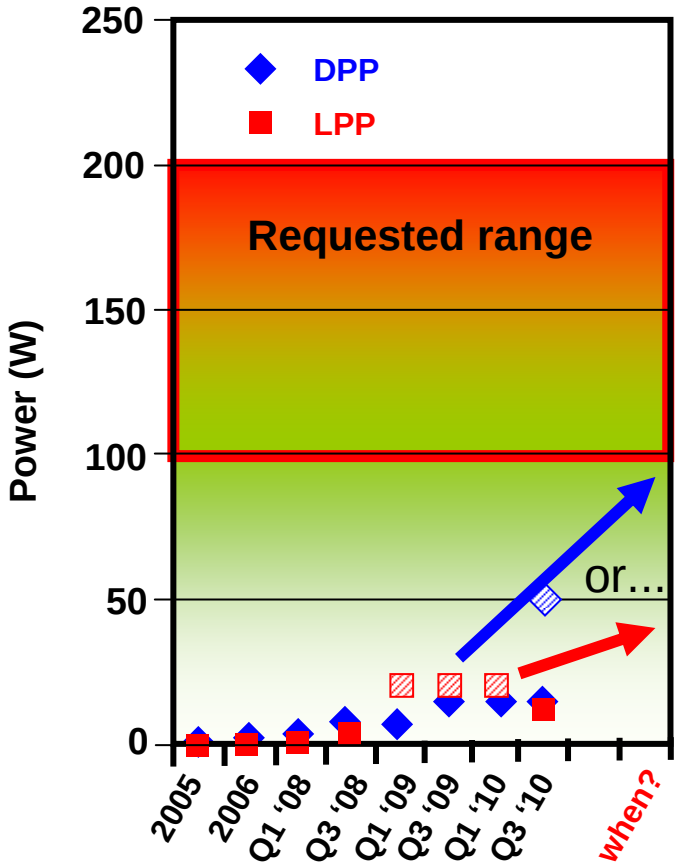


maturity?
throughput?
resist?
…

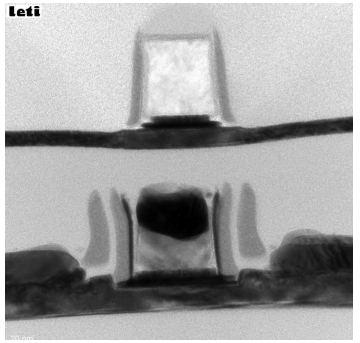
from H. Mailing Semicon West 2010 & IMEC, EUV Symposium '09

Slow progress in EUV source power





What next step?



from P. Batude et al. VLSI 2011 #9A-1

if no shrink through litho …? →

3D

but…

- sequential process ↔ cost
- …

bigger wafer size

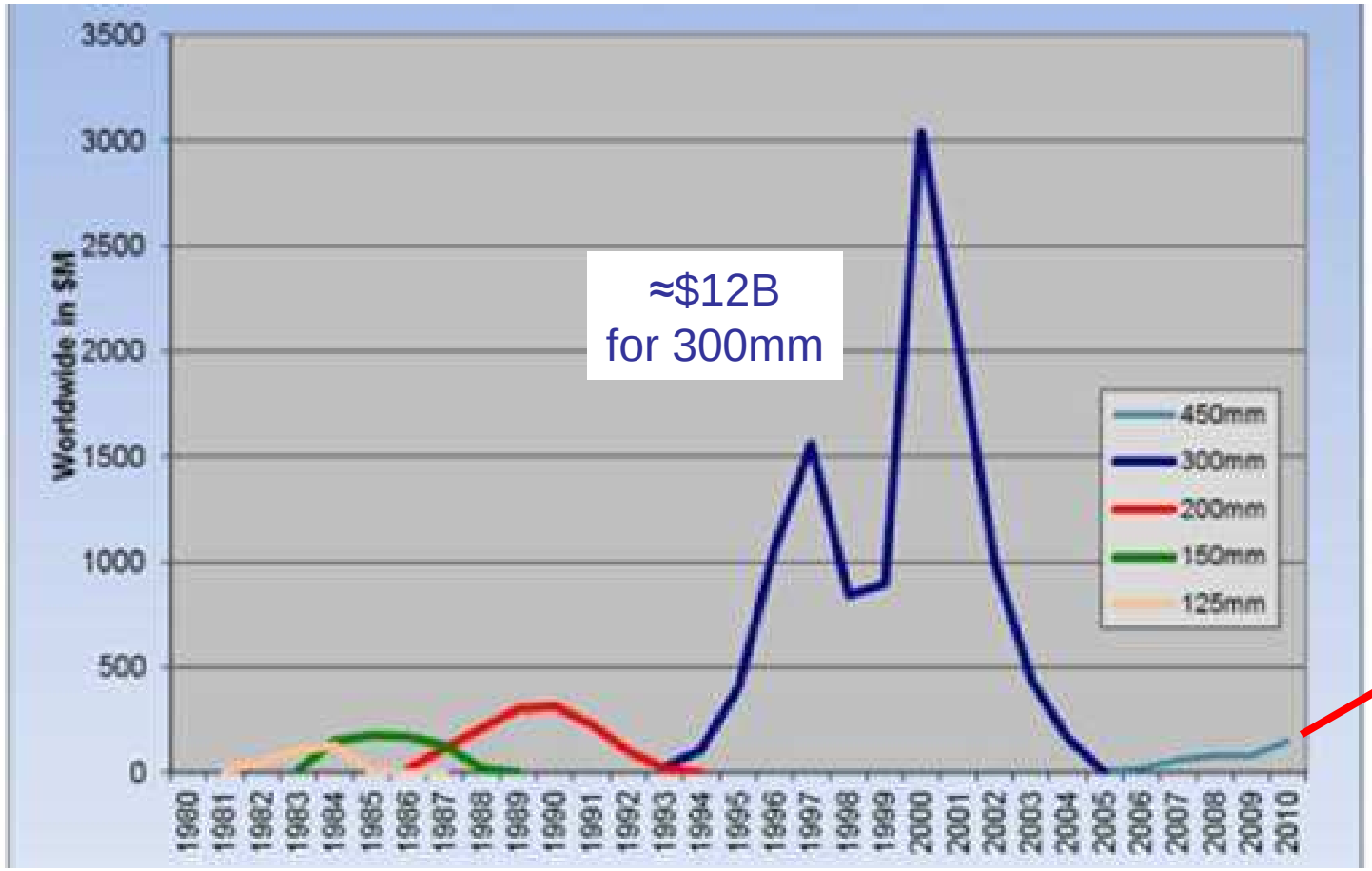
but…

- feasibility on 1+nm CMOS?
- insertion node?
- who will pay?
- …

?

Bigger wafer size: is that affordable?

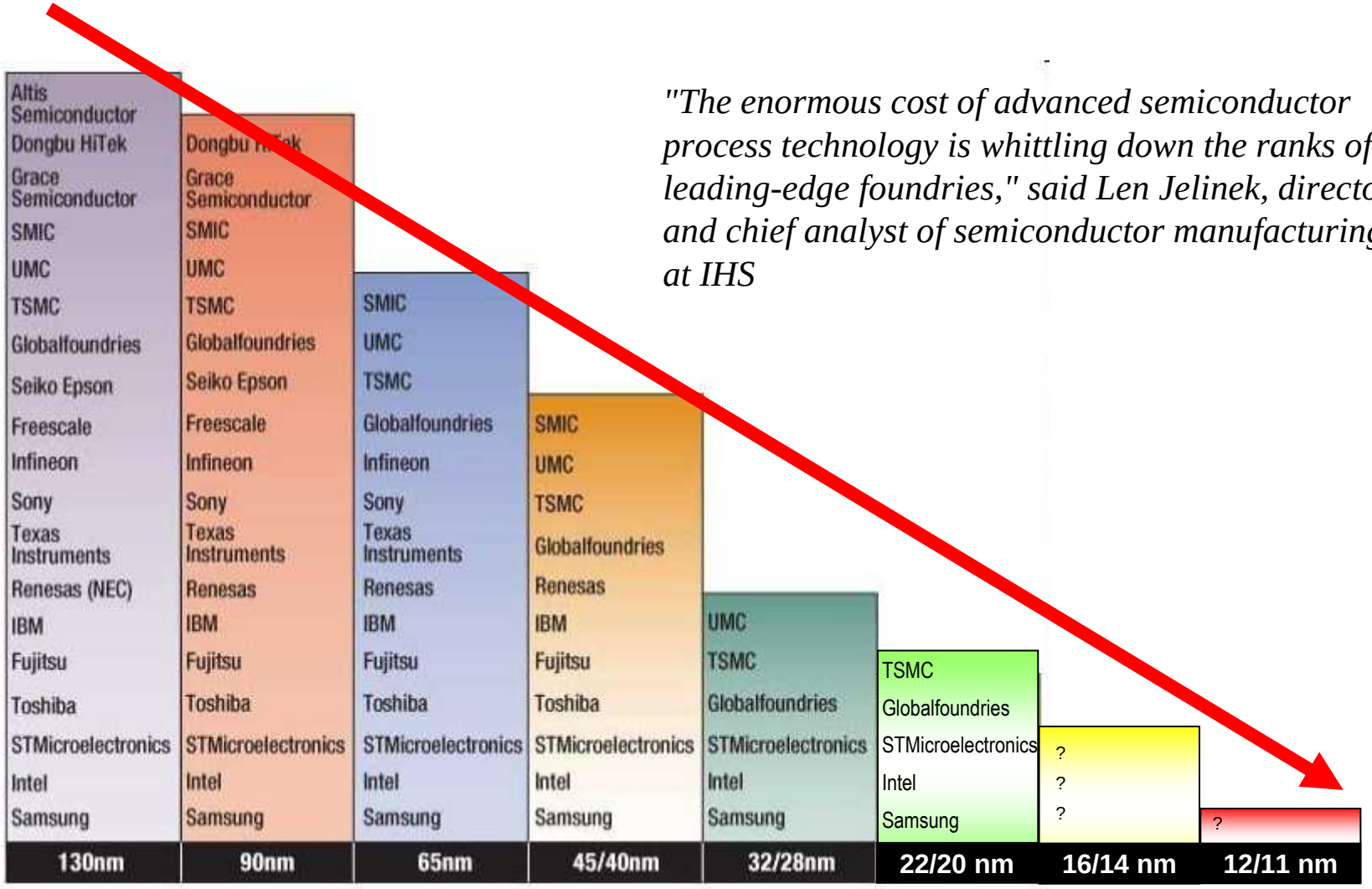
Semiconductor Equipment Industry Spending to Develop New Wafer Size Platforms



≈$10-40⁺B
for 450mm?

Source VLSI Research (2011)

The other side of "*Moore's Law*"

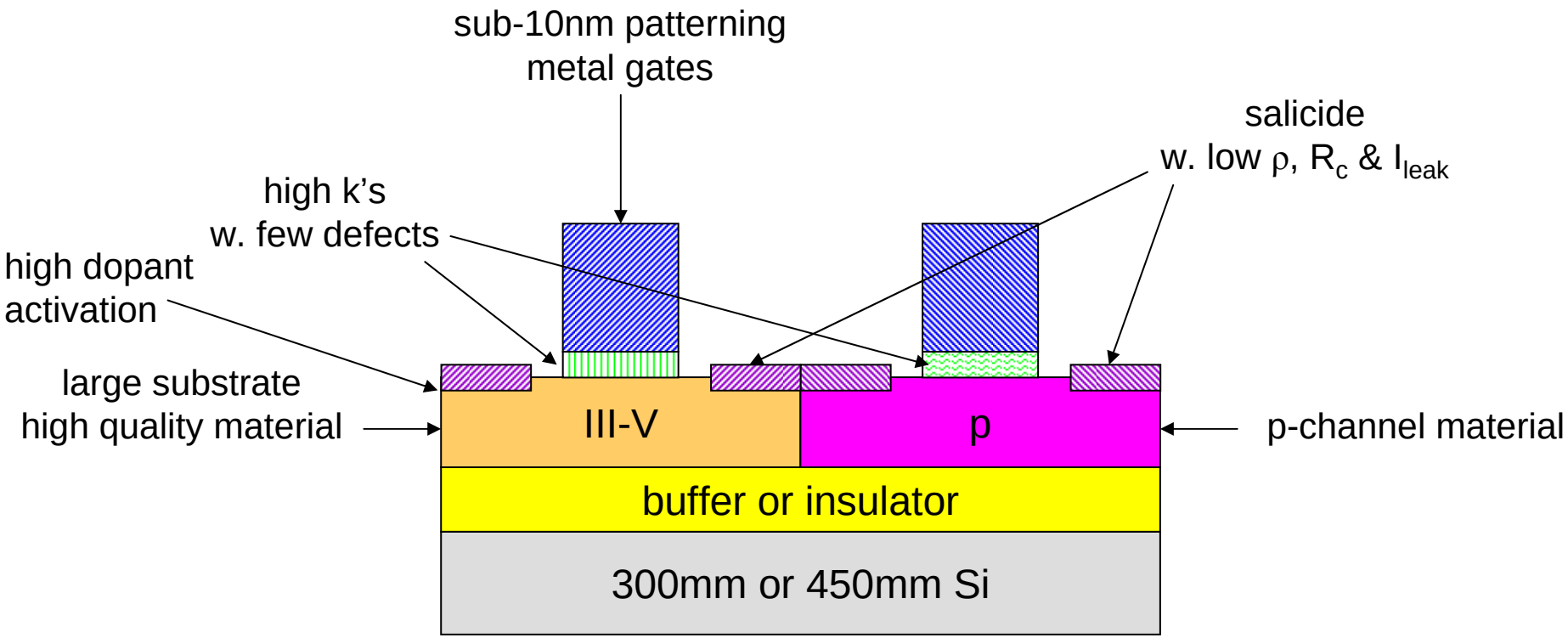


"The enormous cost of advanced semiconductor process technology is whittling down the ranks of leading-edge foundries," said Len Jelinek, director and chief analyst of semiconductor manufacturing at IHS

after IHS iSuppli & S. Tedesco LithoVision 2011

Material engineering

III-V potential technology issues @<10nm

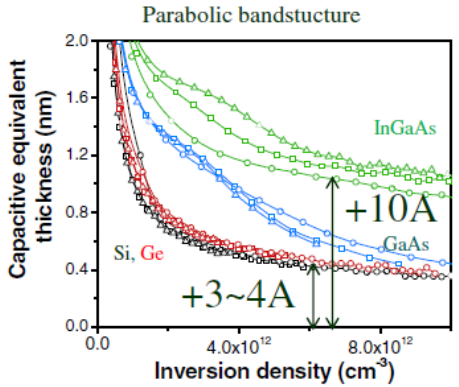


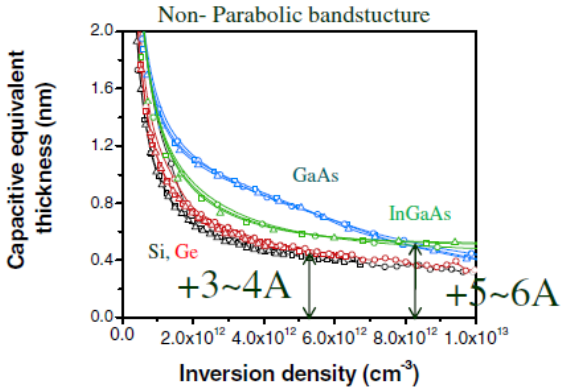
+ ESH

III-V: device physics

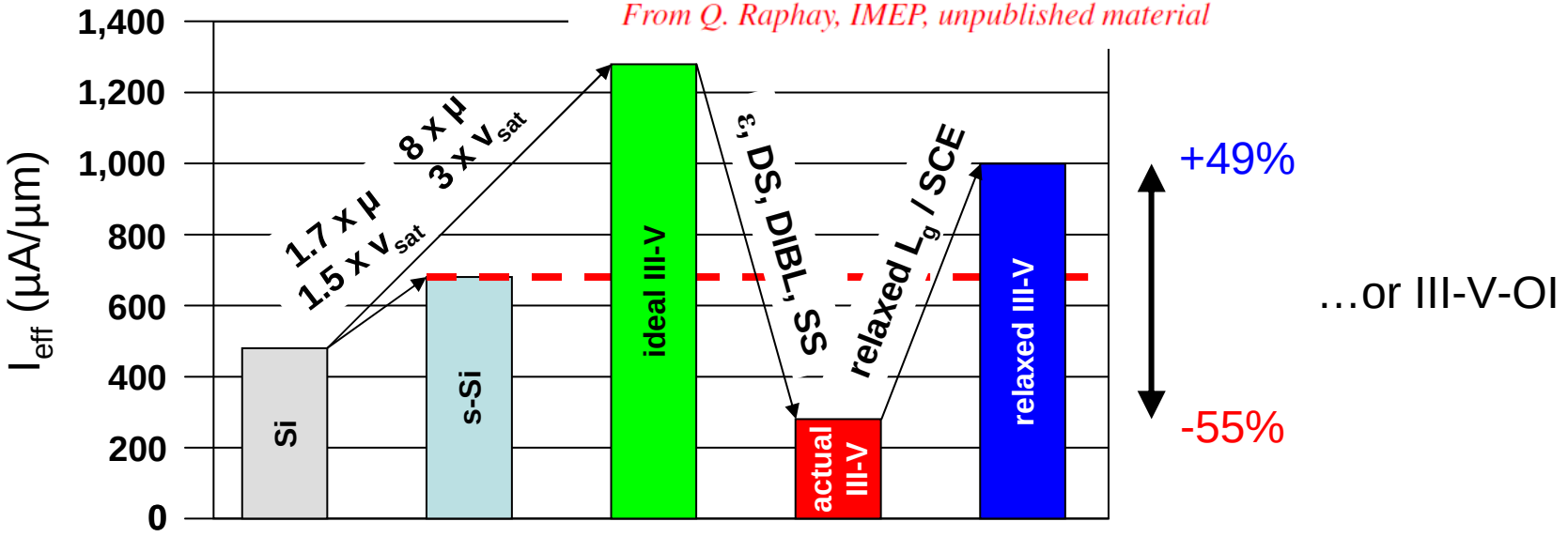
L = 22nm
V_{dd}=1V
I_{off}=10nA/µm

lo
dark sp





From Q. Raphay, IMEP, unpublished material



from T. Skotnicki et al. VLSI 2010 153 & IEDM Short Course 2010

III-V: …as an interim conclusion…

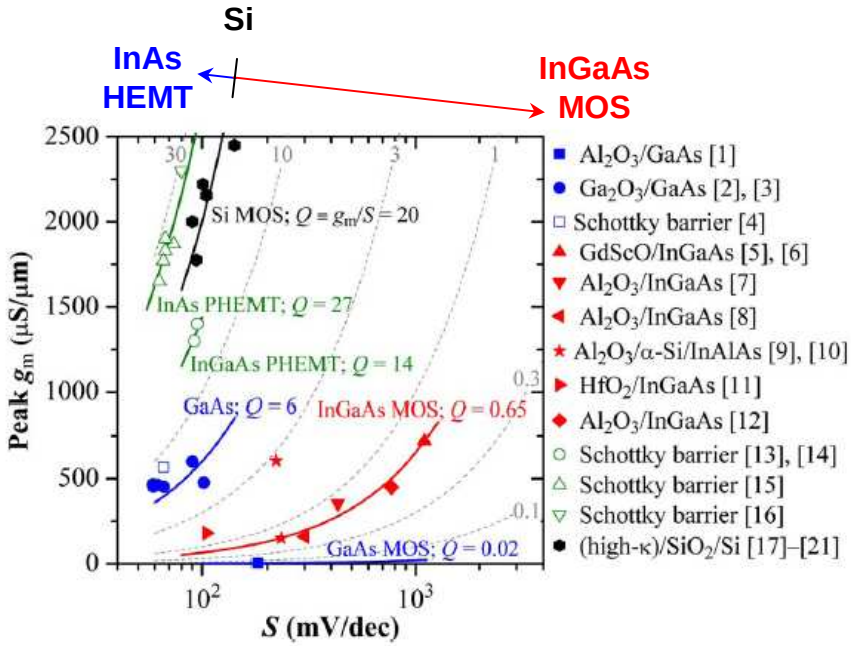
1110 IEEE ELECTRON DEVICE LETTERS, VOL. 31, NO. 10, OCTOBER 2010

Benchmarking of III–V n-MOSFET Maturity and Feasibility for Future CMOS

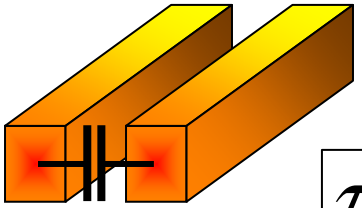
Gerben Doornbos and Matthias Passlack, *Fellow, IEEE*

vices. However, benchmarking those within the realm of III–V and against Si CMOS has been inconsistent and fragmented. This is even more surprising given that the potential insertion of III–V channels in a CMOS has remained controversial and any feasibility study is inconclusive at best without widely accepted standard metrics. In mature Si CMOS, the technolo-

Binary InAs PHEMTs show the highest figure of merit ($Q = 27\,\mu S/\mu m \cdot dec/mV$; the same unit for Q will be used throughout this letter), followed by Si MOSFETs ($Q = 20$) and ternary InGaAs PHEMTs ($Q = 14$). InGaAs MOSFETs appear rather immature ($Q = 0.65$). One important observation



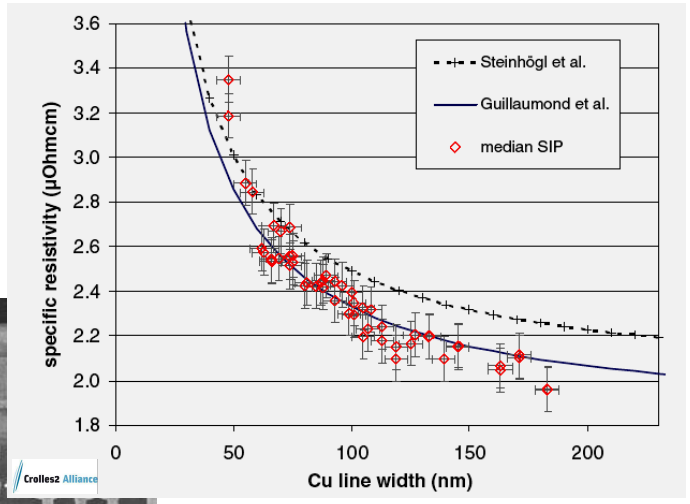
Interconnection: any breakthrough?



$$\tau \approx R \cdot C$$

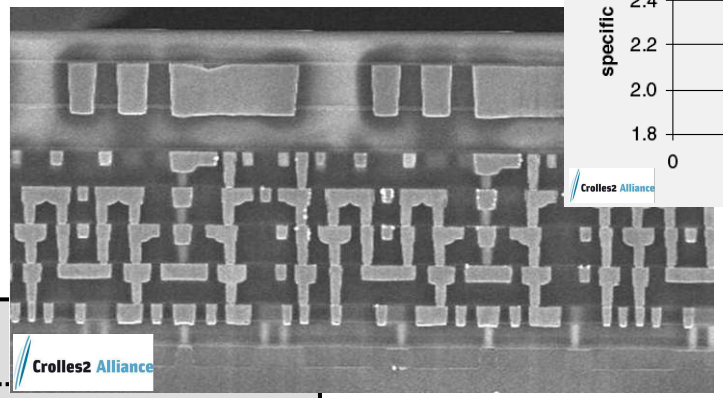
Cu

ideally ρ = 4 → 2 μΩ.cm

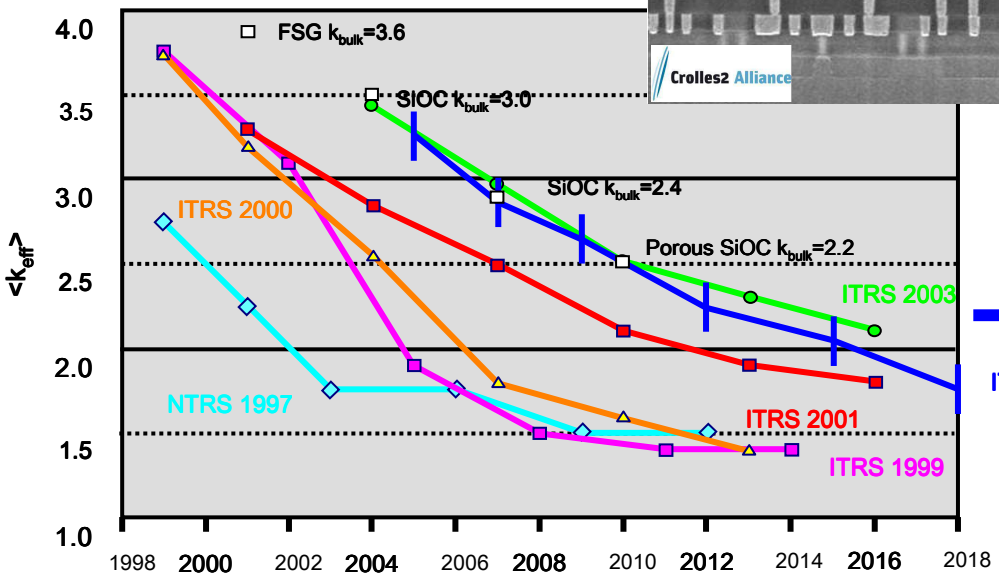


low k material

ideally k=4 → 1



keep ρ ≤ 3 μΩ.cm while scaling



asymptotical trend
$k_{eff} \approx 2.2$

Incubation time for new technologies

- Strained Silicon
  - 1992->2003
- HKMG
  - 1996->2007
- Raised S/D
  - 1993->2009
- EUV
  - 1996->2010

10-20 Years

2011 ISS Europe

P. Gargini 17

Physical limits

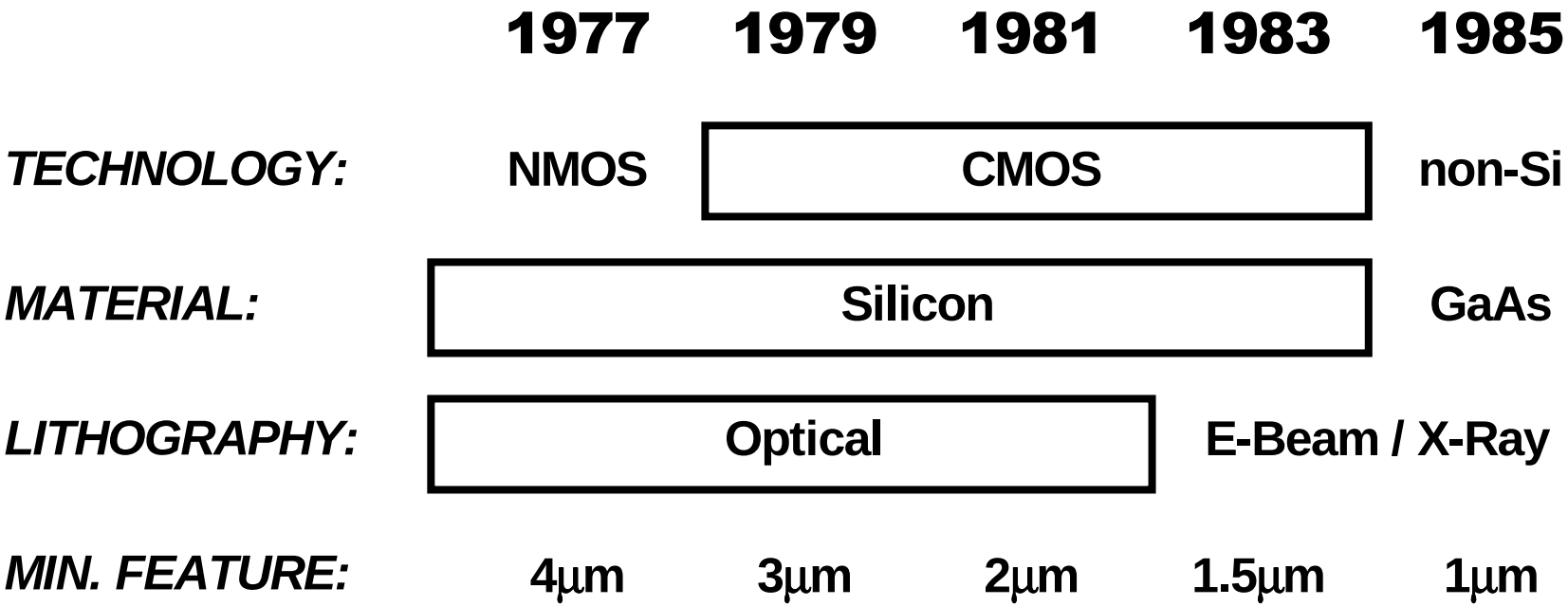
Physical limits?

"I am not convinced that there is any such thing as an
"ultimate" limit.
In fact, finding ways to surmount those obstacles
that, at the present, seem to be the limits
is what technology is all about"

R.W. Keyes, IEEE Spectrum, vol. 6, pp.36-45 (1969)

Conclusion

A 1975 IC Technology Roadmap



What makes us think that we can forecast more than ~5 years of future IC technology any better today ?!!

from R. Doering 8th Annual High Perf Embedded Computing Workshop Sept.28, 2004.

When the roadmap will end?

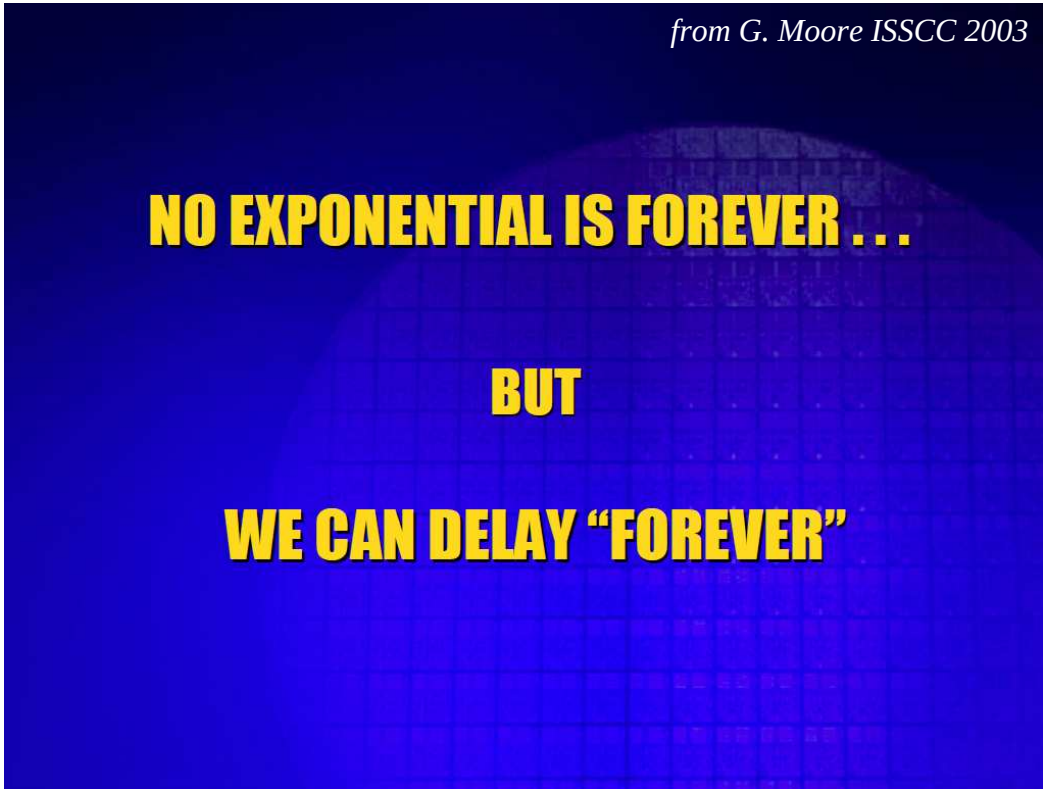
5) **Maximum Packing Density and Minimum Size of Semiconductor Devices**—*J. T. Wallmark and S. M. Marcus, Radio Corporation of America, Sommerville, N. J.*

The absolute upper limit to packi… the absolute minimum size of semiconductor devic… rated or non-integrated, is investigated. It is found… lute limitations of today. Therefore as far as the devices themselves are concerned the end of the road to smaller size has already been reached. A comparison of various components, and various forms of these components is given.

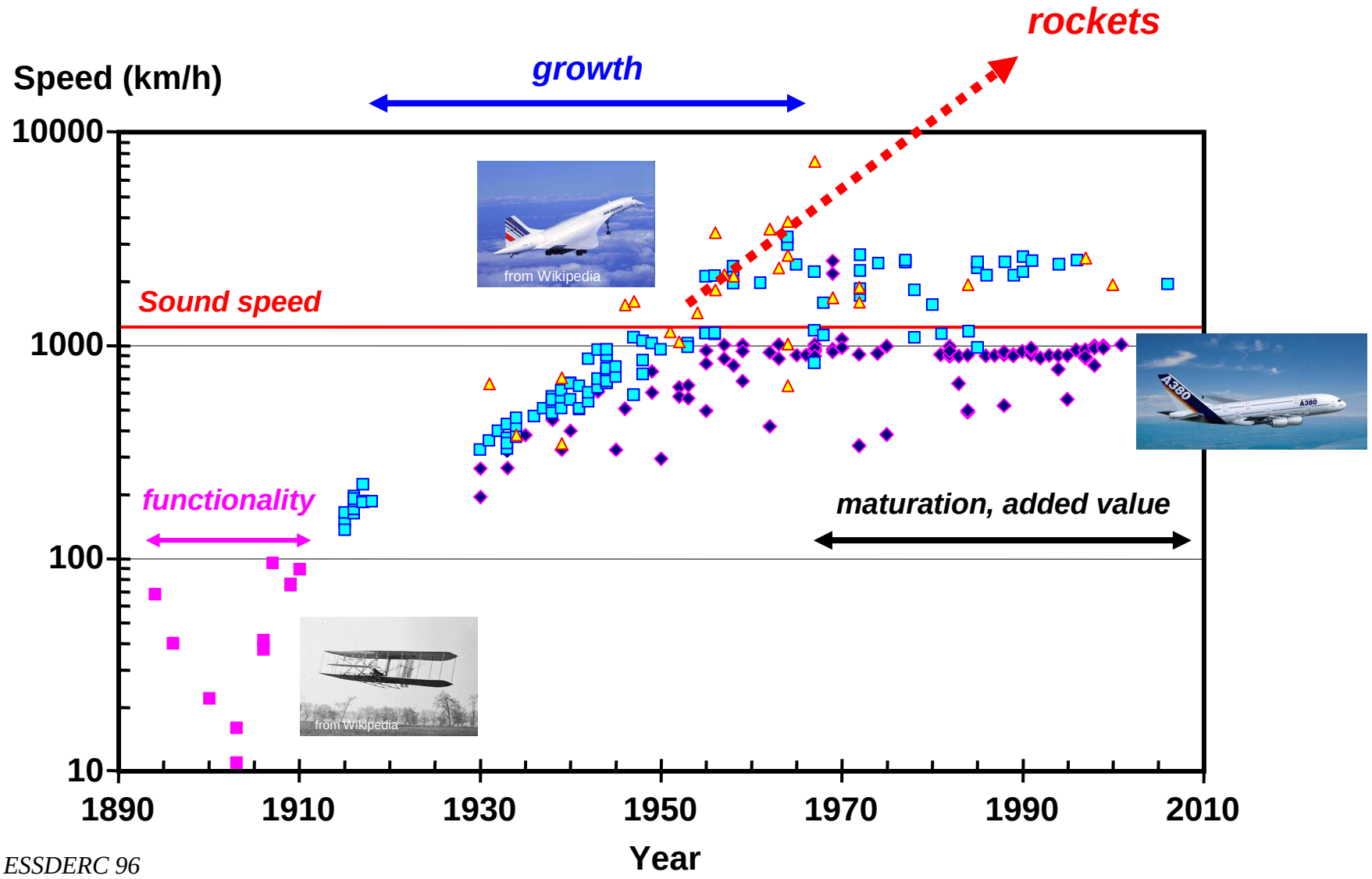
1962!

from T. Wallmart et al. IEEE ED 9 111 (1962)

from G. Moore ISSCC 2003



Exponential growth…for some time



After Iwai, ESSDERC 96

Thank you
for your attention

LABORATOIRE D'ÉLECTRONIQUE
ET DE TECHNOLOGIES
DE L'INFORMATION

CEA-Leti
MINATEC Campus, 17 rue des Martyrs
38054 GRENOBLE Cedex 9
Tel. +33 4 38 78 36 25

www.leti.fr