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From Semiconductors to Chemiconductors?

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Ireland Summer School for Nanotechnology, Kildare, Ireland, August 28-30, 2011

Session Questions

- What are the key enabling materials and methods?
- What new skills will be required?
- What does the nano world enable?
- Is there new Magic at the interfaces?

Enabling materials and methods: *Looking back*

A brief (~2 slides) history of semiconductors

Semiconductors in 1930-1940

Central Breakthrough: **Band structure concept** (Theory)

Experiment: Interesting effects demonstrated, but …

Unreproducible results, not fit subjects for respectable theory

(Minute amounts of impurities drastically change properties)

Nobel Prize 1945

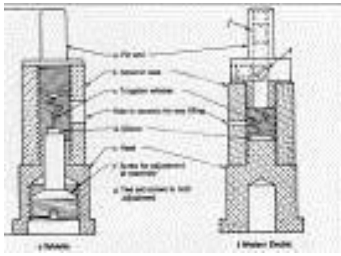
In 1930s most physicists wanted nothing to do with semiconductors

"The residual resistivity is a dirt effect, and one shouldn't wallow in dirt!" (Wolfgang Pauli, 1931)

Nobel Prize 1944

"The physics department at Columbia University will never occupy itself with the physics of dirt" (Isidor Rabi, 1940)

Semiconductors in 1940-1950



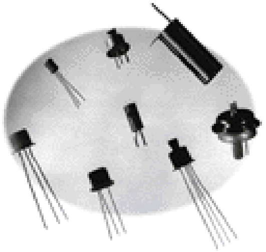
Central Breakthroughs:

Advances in purification and high quality crystal growth of Si and Ge

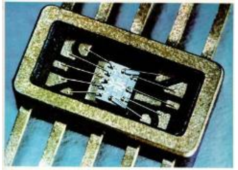
Precisely measured minute amounts of impurities (sub-ppm level) drastically change properties

Beginning about 1946, we began to utilize this knowledge base

Most basic semiconductor devices were demonstrated within 12 years



Bipolar transistor	**1948**
Field effect transistor	**1953**
LED	**1955**
Tunnel diode	**1957**
IC	**1959**
Laser	**1960**



Barrier engineering in semiconductors

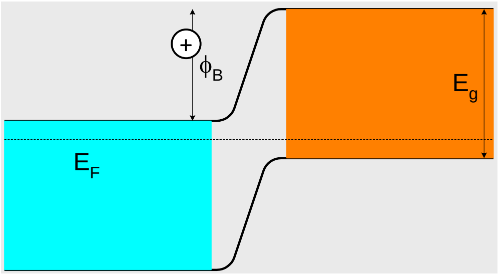
By doping, it is possible to create a built-in field and energy barriers within monolithic semiconductor with

- **Controllable height and**
- **Controllable length**

It allows one to achieve *conditional* electron transport between different energy states inside semiconductors that is needed in the physical realization of devices for information processing.

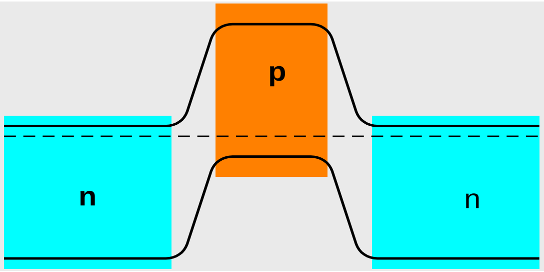
$$W = \sqrt{2\varepsilon\varepsilon_0 V_{bi}\frac{N_A + N_D}{N_A N_D}} \approx \sqrt{\frac{2\varepsilon_0\varepsilon V_{bi}}{N_{A,D}}}$$

pn-junction



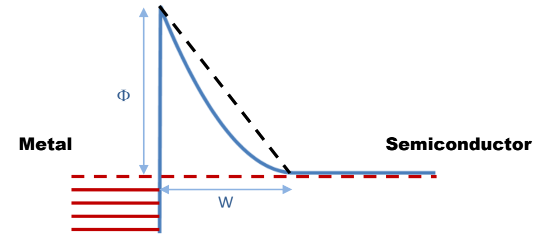
Diode
- rectifier
- switch

npn structure



Transistor
- bipolar
- field-effect

Me-semiconductor contact



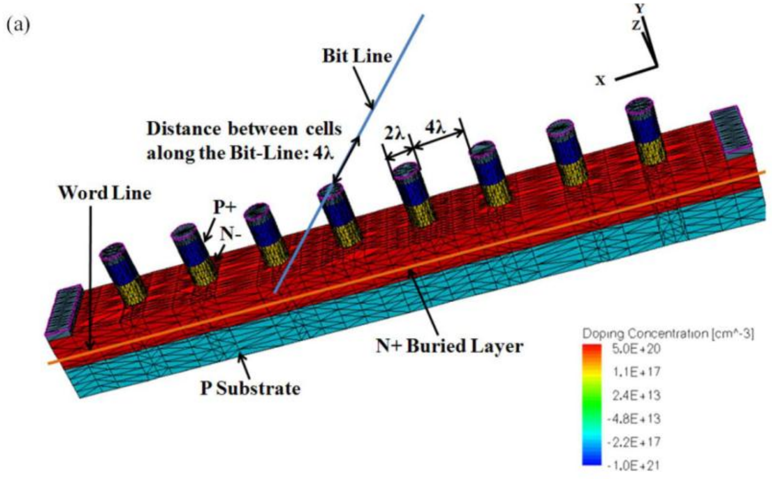
- Schottky diode
- Ohmic contact

Fundamental Scaling Issues

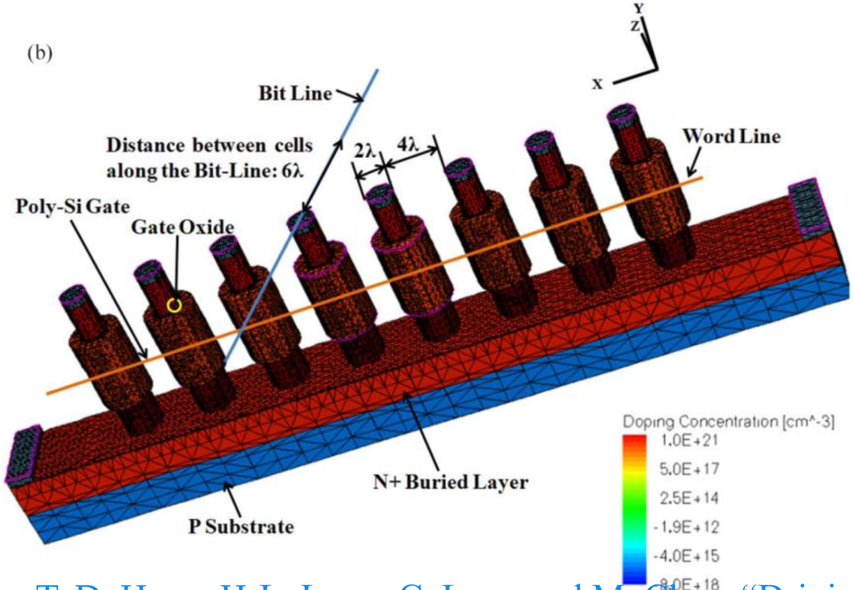
- For scaled diode-type select devices two fundamental challenges are:
  - Contact resistance
  - Lateral depletion effects
  - Very high concentration of dopants are needed to minimize both effects.
    - high dopant concentrations result in increase reverse currents in classical diode structures and therefore in reduced ON/OFF ratio.

Smallest Select Switch (Memory perspective)

Vertical diode



Vertical FET



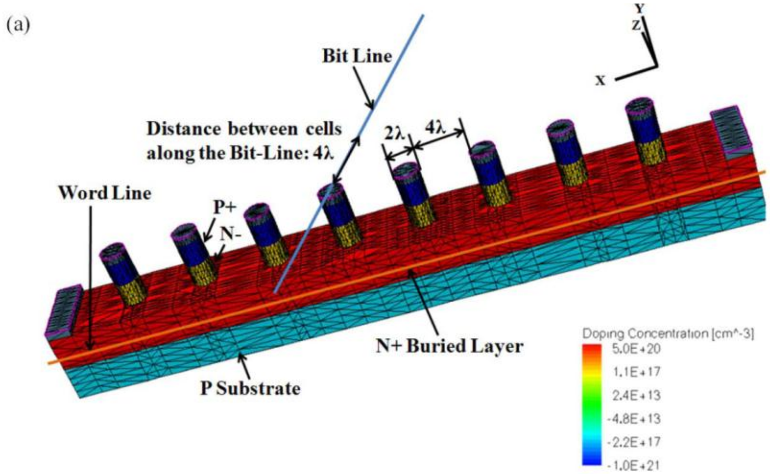
L. Li, K. Lu, B. Rajendran, T. D. Happ, H-L. Lung, C. Lam, and M. Chan, "Driving Device Comparison for Phase-Change Memory", *IEEE Trans. Electron. Dev*. 58 (2011) 664-671

‘Benchmark’ sub-10-nm device

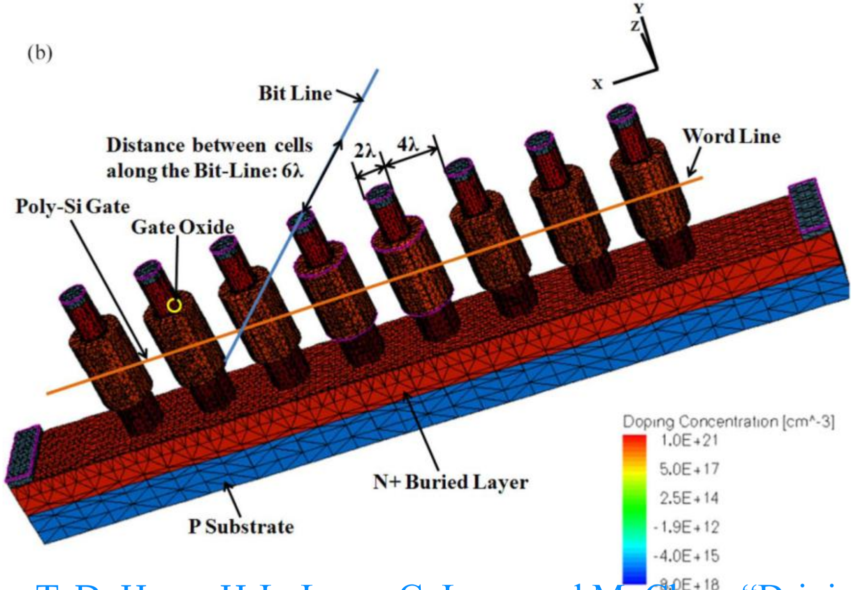
Parameter	**Value**	**Driver**
Device size	<10 nm	Scaling
Operating Voltage, V	~1 V	Low-power operation
Operating current, I_r	~10^{-6} A	Operation speed Sensing of memory state
Switching speed	<10^{-9} s	
ON/OFF ratio	>10^{7}	Low-power operation Low ‘sneak’ currents

Smallest Select Switch (Memory perspective)

Vertical diode



Vertical FET

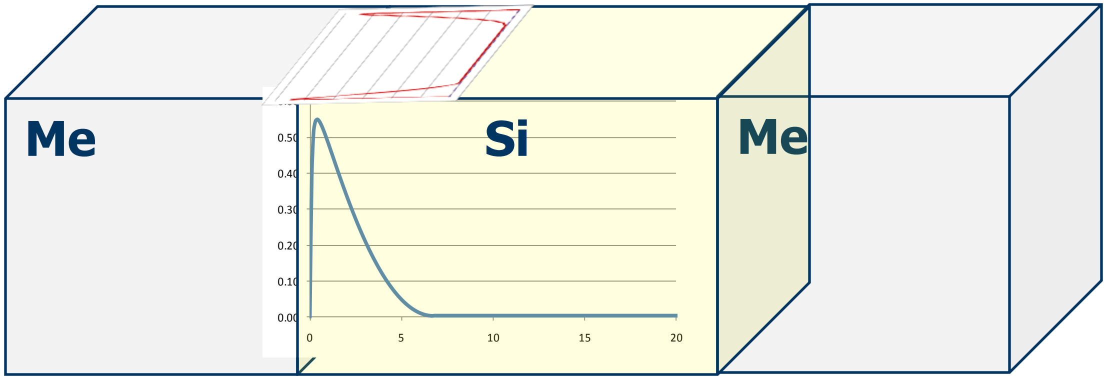


L~10nm

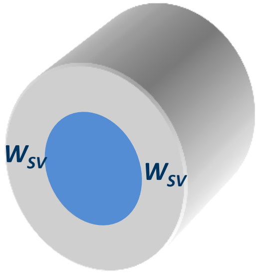
I_{min}=1 μA

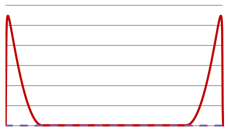
L. Li, K. Lu, B. Rajendran, T. D. Happ, H-L. Lung, C. Lam, and M. Chan, "Driving Device Comparison for Phase-Change Memory", *IEEE Trans. Electron. Dev*. 58 (2011) 664-671

Scaling Limits of Diodes



Reduction of the effective conduction area due to side depletion





$N_d \leq N_C$

$$\boxed{W \approx \sqrt{\frac{2\varepsilon\varepsilon_0 V_{bi}}{N_D}} \geq 10nm}$$

$$I = J \cdot A = J \cdot \left(L - 2W_0\right)^2$$

$N_d \geq N_C$

pn-diode → Esaki tunnel diode

Schottky diode → Ohmic contact

$L_{min} > 2W$

$I_{min} = 1\ \mu A$

N_C – effective density of states in the conduction band, for Si $N_C = 2.8\times10^{19}$ cm^{-3}

Germanium Schottky diodes

N_C=1.04x10^{19} cm^{-3}

Extreme scaling:

$N_d = N_C$ and $V_{on=}$ 1 volt

W_0=8.7 nm

L_{min}=20 nm (I_{on}~ 1μA)

ON/OFF ~ 10^5

$V_{off=}$ 1 volt

‘Relaxed’ case:

L=500 nm

$N_d = 10^{18}$ cm^{-3}

W_0=31 nm

I_{on}~ 2 mA

ON/OFF ~ 10^5

Silicon Schottky diodes

N_C=2.8x10^{19} cm^{-3}

Extreme scaling:

N_d =N_C and $V_{on=}$ 1 volt

W_0=6.2 nm

L_{min}=14 nm (I_{on}~ 1μA)

ON/OFF ~ 10^7

$V_{off=}$ 1 volt

'Relaxed' case:

L=300 nm

N_d =10^{18} cm^{-3}

W_0=31 nm

I_{on}~ 260 μA

ON/OFF ~ 10^{10}

Enabling materials and methods: *Looking ahead*

An introduction to *chemiconductors*

Chemiconductors – semiconducting materials , whose stoichiometry can be varied by oxidative and/or reductive valency state changes. This is equivalent to variable doping with defects rather than with foreign species.

Typical example: metal oxides

B.D. Cahan and C-T. Chen, “The nature of the passive film on iron: The chemi-conductor model and further supporting evidence”, *J. Electrochem. Soc.* 129 (1982) 921-925

Semiconductors vs. Chemiconductors

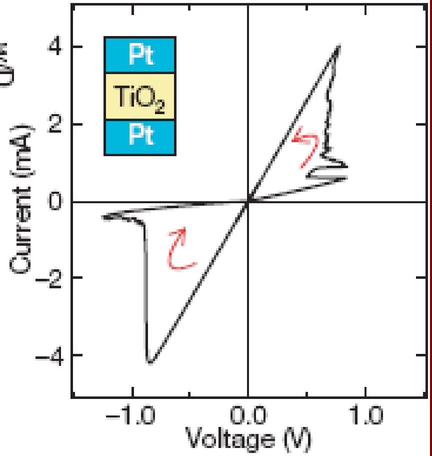
Semiconductor

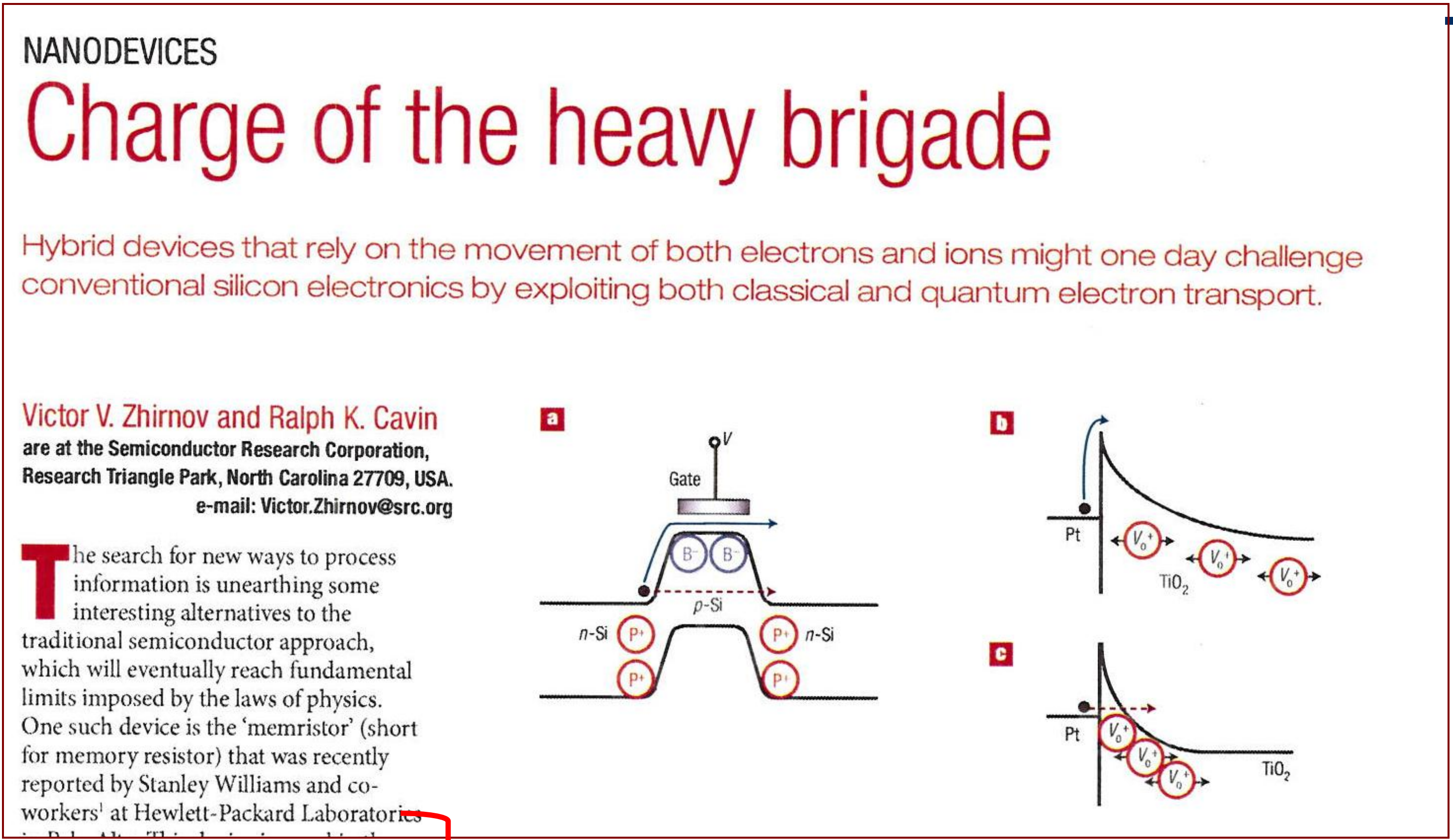
- the ions forming donor and acceptor levels are due impurities (‘foreign bodies’) introduced into the host matrix
  - e.g. P, B atoms in Si
- The *dopants* (i.e. donors and acceptors) don’t change their positions
  - Invreasingly difficult to put them in precise location
- Electrons are the only movable particles
  - Used to represent and sense state
  - Difficult at <10nm
- Rigid interfaces
  - EITHER Ohmic OR Blocking

Chemiconductor

- the ions forming donor and acceptor levels are due to composition variation in the host matrix
  - lattice point defects (e.g. vacancies or interstitial atoms) can electrically act as donors or acceptors
  - e.g. ionized oxygen vacancy VO^{+2} in TiO_2
  - the ions can move in electrical fields
    - e.g. under external bias
- Atoms and electrons are movable
  - e.g. Atoms – repersent state; electrons – sense state
  - Operate at <10nm
- Adaptive interfaces
  - Can switch from Ohmic to Blocking

Moving atoms:
ReRAM, Memristor, Atomic Switch





NANODEVICES

Charge of the heavy brigade

Hybrid devices that rely on the movement of both electrons and ions might one day challenge conventional silicon electronics by exploiting both classical and quantum electron transport.

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The search for new ways to process information is unearthing some interesting alternatives to the traditional semiconductor approach, which will eventually reach fundamental limits imposed by the laws of physics. One such device is the 'memristor' (short for memory resistor) that was recently reported by Stanley Williams and co-workers[1] at Hewlett-Packard Laboratories

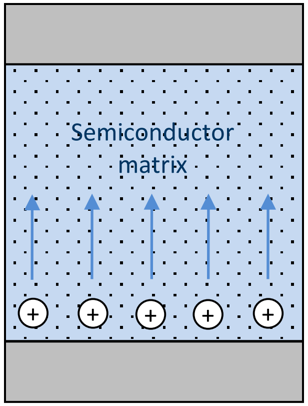
J. J. Yang, M. D. Pickett, X. M. Li, D. A. A. Ohlberg, D. R. Stewart, R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices", *Nature Nanotechnology* 3 (2008) 429-433.

Jeong DS, Schroeder H, Waser R, "Mechanism for bipolar switching in a Pt/TiO_2/Pt resistive switching cell", PHYS. REV. B 79 (2009) 195317

Mechanism of conductance switching in TiO_2 is discussed in terms of modulation of the Schottky barrier as result of variation of the number of the oxygen vacancies close to the interface.

‘Magic’ at the interfaces: interface resistance switching due to atomic re-arrangements

Re-arrangement of *charged* defects/impurities near the interface between the *semiconductor* matrix and an electrode



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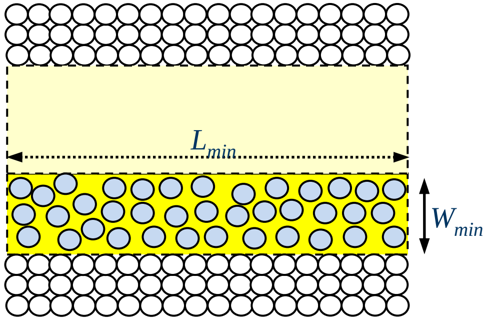
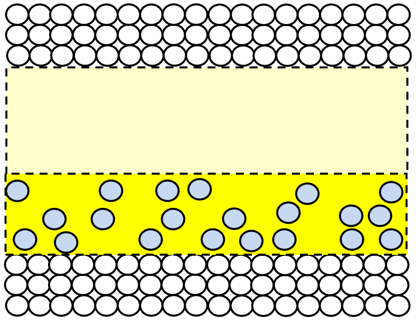
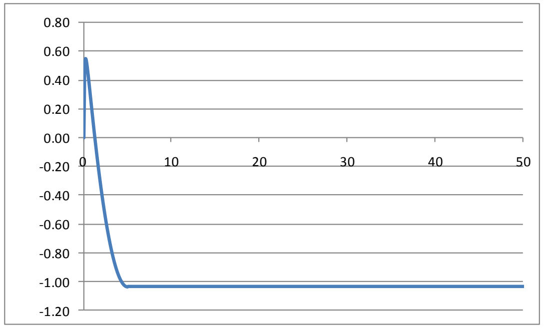
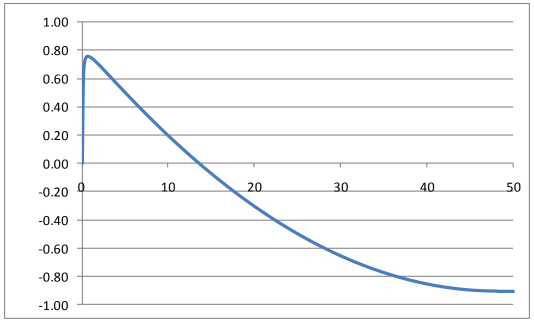


ON

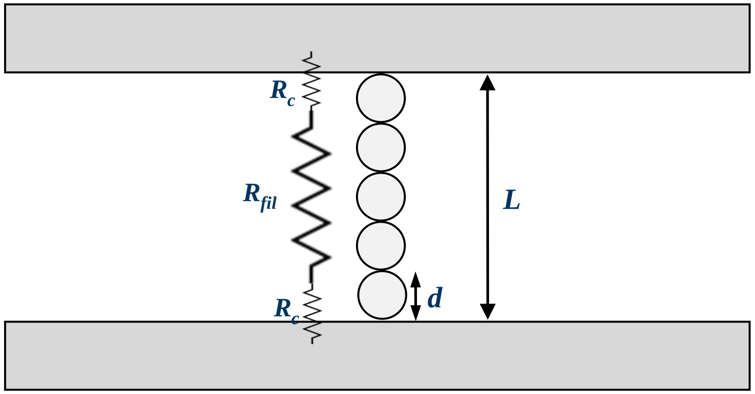


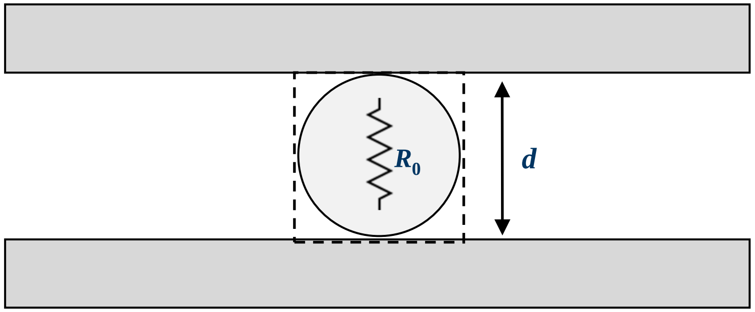
OFF

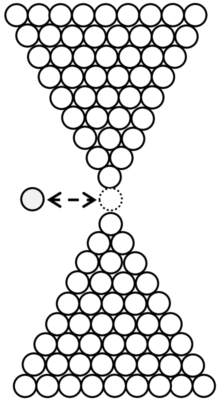




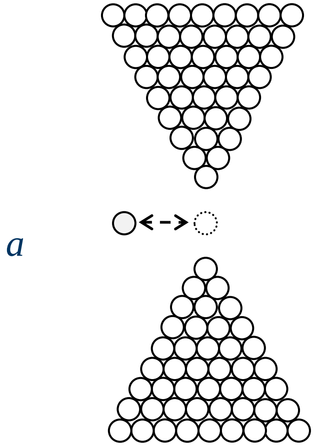
Ultimate case:
Minimal Conductive Bridge

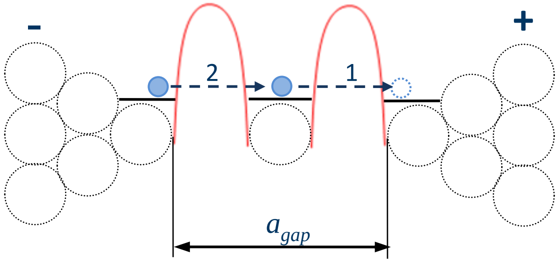






Discontinuous atomic bridge





g	I_{on}, A	I_{off}, A	ON/OFF	a_{gap}, nm
2	7.80E-06	3.37E-07	23	0.77 (3δ)
3	3.39E-06	4.28E-09	792	1.29 (5δ)
4	2.46E-06	1.86E-11	132258	1.81 (7δ)

$$I(g) = \frac{1}{g^2} I_1$$

The minimal 2-gap structure (1 atom in the inter-electrode space) is in principle sufficient to obtain both a sufficiently large ON current and a reasonably large resistance ON/OFF ratio to satisfactorily differentiate the state of the ReRAM cell.

Chemiconductor Devices

- Resistive (RedOx or ionic) **Memory** shows promise
  - Sub-10 nm scaling possible!

V. V. Zhirnov, R. K. Cavin, S. Menzel, E. Linn, S. Schmelzer, D. Bräuhaus, C. Schindler and R. Waser, "**Memory Devices: Energy-Space-Time Trade-offs**", *Proc. IEEE* 98 (Dec. 2010) 2185

- Memory Select **Switch**
  - represents a serious bottleneck for memory scaling to 10 nm and beyond
  - MIEC switch demonstrated

Gopalakrishnan 2010

    - observed in materials that conduct both ions and electronic charges – so called mixed ionic electronic conduction materials (MIEC).
    - The resistive switching mechanism is similar to the ionic memories.
- **Logic** devices are envisioned
  - Memristor (Williams et al. 2008-2011)
  - Atomic switch (Aono et al. 2007-2011)

Summary

- What are the key enabling materials and methods?
  - Materials: Chemiconductors
  - Methods & Skills: Precise control of stoichiometry and ‘defects’ with same accuracy as semiconductor doping

- What does the nano world enable?
  - Heavy particles may offer fast & reliable operation within ~nm dimensions
- Is there new Magic at the interfaces?
  - *Adaptive Interfaces* due to movable dopants

Back-Up slides

The Qualit Binary Switch

A Dilemma

"Quality" factor of a binary switch:

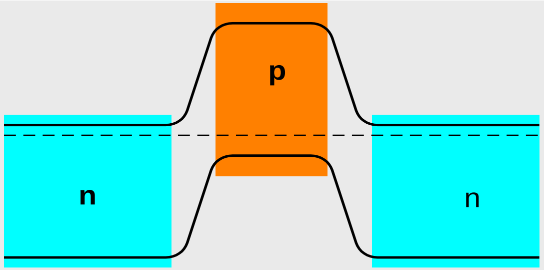
$$Q = \frac{I_{on}}{I_{off}} = \frac{\tau_{store}}{t_{sw}}$$

larger *m* is better

smaller *m* is better

$$t_{sw} = L\sqrt{\frac{m}{2E}}$$

$$\tau_{store} \sim \exp\left(\frac{2\sqrt{2m}}{\eta}(L\sqrt{E_b})\right)$$



How can we go below 5 nm?

Devices having feature sizes less than 5 nm should utilize particles whose mass is greater than the mass of an electron. Below about 5 nm, the mass of information-bearing particle should exceed free electron mass and required particle mass rapidly increases below 5 nm.

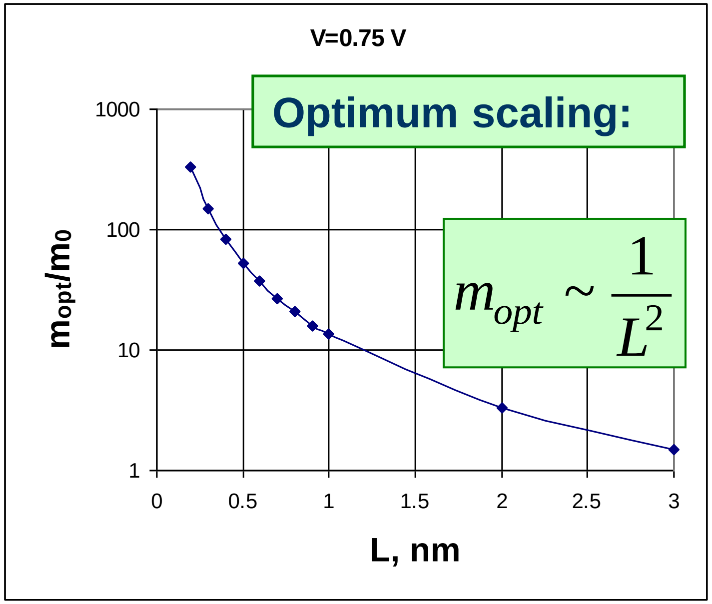
This conclusion resulted from the ON/OFF optimization:

$$I_{on} \sim \frac{\sqrt{E}}{L\sqrt{m}}$$

$$I_{off} \sim \exp\left(-\frac{2\sqrt{2E}}{\eta} L\sqrt{m}\right)$$

(tunneling)

$$L\sqrt{m} = const \Rightarrow \frac{I_{on}}{I_{off}} = const$$

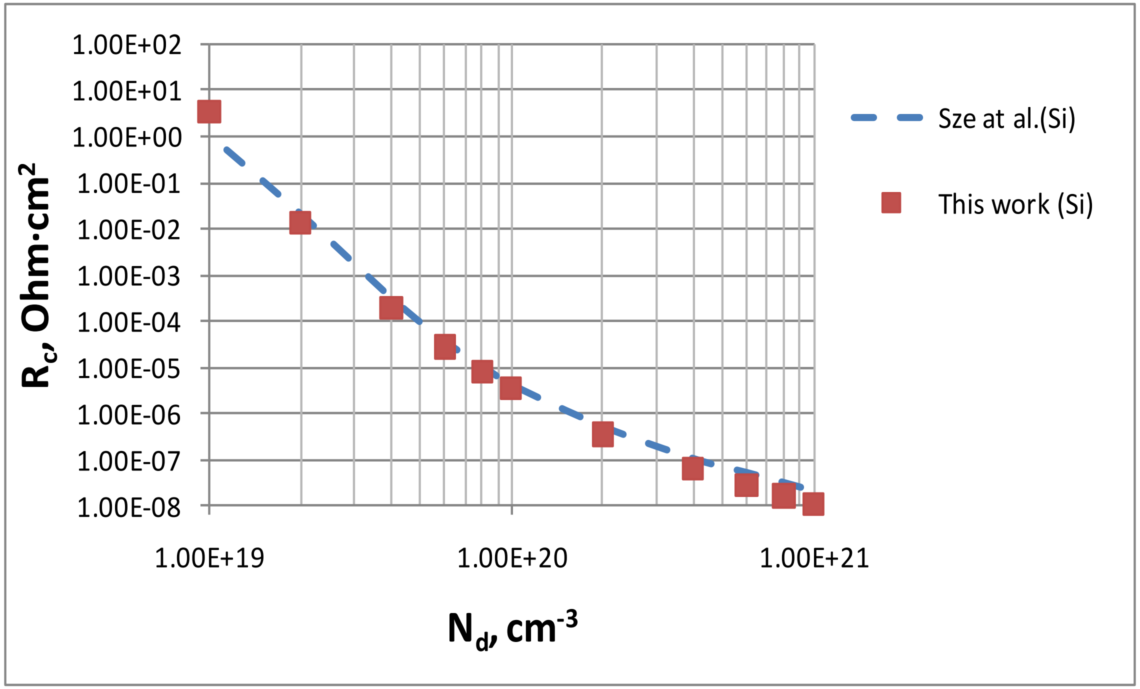


Optimum scaling:

$$m_{opt} \sim \frac{1}{L^2}$$

Heavier mass does not imply slower operation

Contact Resistance Issue



C.Y. Chang, Y. K. Fang, and S. M. Sze, "Specific contact resistance of metal-semiconductor barriers", Soli-State Electron. 14 (1971) 541-550