Intel® 80333 I/O Processor

Datasheet

Product Features

- Integrated Intel XScale® core
  - —500, 667 and 800 MHz
  - —ARM* V5TE Compliant
  - —32 KByte, 32-way Set Associative Instruction Cache with cache locking
  - —32 KByte, 32-way Set Associative Data Cache with cache locking. Supports write through or write back
  - —2 KByte, 2-way Set Associative Mini-Data Cache
  - —128-Entry Branch Target Buffer
  - —8-Entry Write Buffer
  - —4-Entry Fill and Pend Buffer
  - —Performance Monitor Unit
- Internal Bus 333 MHz/64-bit
- PCI Express*-to-PCI Bridges
  - —x8 PCI Express* Upstream Link
  - —PCI Express* Specification 1.0a compliant
  - —PCI-X Bus A (IOP bus - ATU interface)
  - —PCI-X Bus B (Slot Expansion bus) supports standard PCI Hot-Plug Controller
  - —Four output clocks per PCI-X bus
- Address Translation Unit
  - —2 KB or 4 KB Outbound Read Queue
  - —4 KB Outbound Write Queue
  - —4 KB Inbound Read and Write Queue
  - —Connects Internal Bus to PCI/X Bus A
  - —Messaging Unit and Expansion ROM
- Two Programmable 32-bit Timers and Watchdog Timer
- Eight General Purpose I/O Pins
- Two I^2C Bus Interface Units
- Dual-Ported Memory Controller
  - —PC2700 Double Data Rate (DDR333) SDRAM
  - —DDRII 400 SDRAM
  - —Up to 2 GB of 64-bit DDR333
  - —Up to 1 GB of 64-bit DDRII400
  - —Optional Single-bit Error Correction, Multi-bit Detection Support (ECC)
  - —Supports Unbuffered or Registered DIMMs and Discrete SDRAM
  - —32-bit memory support
- DMA Controller
  - —Two Independent Channels Connected to Internal Bus
  - —Two 1KB Queues in Ch0 and Ch1
  - —CRC-32C Calculation
- Application Accelerator Unit
  - —RAID6 support
  - —Performs optional XOR on Read Data
  - —Compute Parity Across Local Memory Blocks
  - —1 KB/512 byte Store Queue
- Two UART (16550) Units
  - —64-byte Receive and Transmit FIFOs
  - —4-pin, Master/Slave Capable
- Peripheral Bus Interface
  - —8-/16-bit Data Bus with Two Chip Selects
- Interrupt Controller Unit
  - —Four Priority Levels
  - —Vector Generation
  - —Sixteen External Interrupt Pins with High Priority Interrupt (HPI#)
- 829-Ball, Flip Chip Ball Grid Array (FCBGA)
  - —37.5 mm^2 and 1.27 mm ball pitch

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Revision History

Date	Revision	Description
July 2005	003	Updated voltages in Section 4.3
May 2005	002	Revised: Table 16, modified pin mode behavior for DQ[63:32] for 32-bit DDR. Table 21, modified Case Temperature Under Bias to 95 C Max Table 22, modified Case Temperature Under Bias to 95 C Max Table 25, added note 4
March 2005	001	Initial release

1.0 Introduction

1.1 About This Document

This document is the *Intel® 80333 I/O Processor Datasheet*. This document contains a functional overview, package signal locations, targeted electrical specifications, and bus functional waveforms. Detailed functional descriptions other than parametric performance are published in the *Intel® 80333 I/O Processor Developer's Manual*.

Intel Corporation assumes no responsibility for any errors which may appear in this document nor does it make a commitment to update the information contained herein.

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1.1.1 Terminology

To aid the discussion of the Intel® 80333 I/O processor (80333) architecture, the following terminology is used:

Core processor	Intel XScale® core within the 80333
Local processor	Intel XScale® core within the 80333
Host processor	Processor located upstream from the 80333
Local bus	80333 Internal Bus
Local memory	Memory subsystem on the Intel XScale® core DDR SDRAM or Peripheral Bus Interface busses
Inbound	At or toward the Internal Bus of the 80333 from the PCI interface of the ATU
Outbound	At or toward the PCI interface of the 80333 ATU from the Internal Bus
Downstream	At or toward a PCI Express* port directed away from the root complex (to a bus with a higher number)
Upstream	At or toward a PCI Express* port directed to the PCI Express* root complex (to a bus with a lower number).
QWORD	64-bit data quantity (8 bytes).
DWORD	32-bit data quantity (4 bytes).
word	16-bit data quantity (2 bytes).

1.1.2 Other Relevant Documents

1. *Intel XScale® Core Developer's Manual* (273473) — Intel Corporation
2. *PCI Hot-Plug Specification,* Revision 1.1 — PCI Special Interest Group
3. *PCI Express* Specification,* Revision 1.0a — PCI Special Interest Group
4. *Intel® 80333 I/O Processor Developer's Manual* (305432) — Intel Corporation
5. *Intel® 80333 I/O Processor Design Guide* (305434) — Intel Corporation
6. *Intel® 80333 I/O Processor Specification Update* (305435) — Intel Corporation
7. *PCI Local Bus Specification,* Revision 2.3 — PCI Special Interest Group
8. *PCI-X Addendum to the PCI Local Bus Specification,* Revision 1.0a — PCI Special Interest Group
9. *PCI Bus Power Management Interface Specification,* Revision 1.1 — PCI Special Interest Group

1.2 About the Intel® 80333 I/O Processor

The 80333 is a multi-function device that integrates the Intel XScale® core (ARM* architecture compliant) with intelligent peripherals and PCI Express*-to-PCI Bridges. The 80333 consolidates, into a single system:

- Intel XScale® core
- ×8 PCI Express* Upstream Link
- Two PCI Express*-to-PCI Bridges supporting PCI-X interface on both segments
- PCI Standard Hot-Plug Controller (segment B)
- Address Translation Unit (PCI-to-Internal Bus Application Bridge) interfaced to the segment A
- High-Performance Memory Controller
- Interrupt Controller with up to 16 external interrupt inputs
- Two Direct Memory Access (DMA) Controllers
- Application Accelerator
- Messaging Unit
- Peripheral Bus Interface Unit
- Two I^2C Bus Interface Units
- Two 16550 compatible UARTs with flow control (four pins)
- Eight General Purpose Input Output (GPIO) ports

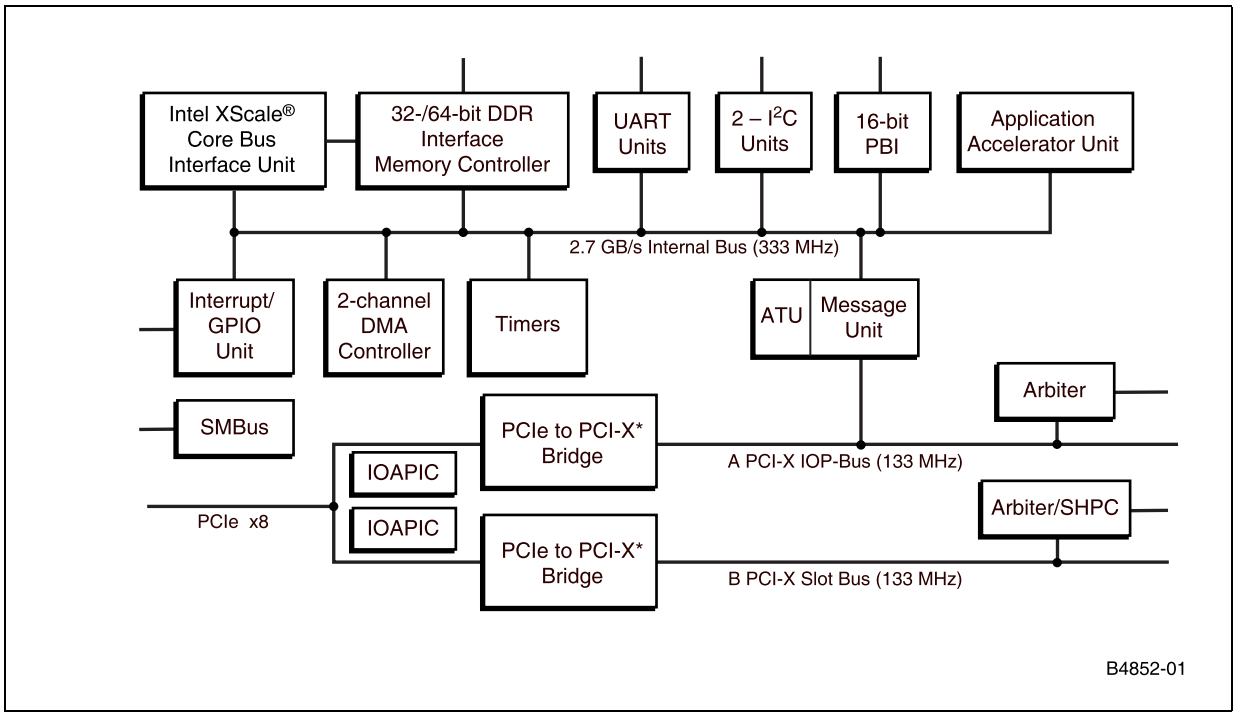
The 80333 is an integrated processor that addresses the needs of intelligent I/O applications and helps reduce intelligent I/O system costs.

PCI Express* is an industry-standard, high-performance, low-latency system interconnect. The PCI Express* upstream link of the 80333 is capable of ×8 lane widths at 2.5 GHz operation, as defined by the *PCI Express* Specification*, Revision 1.0a. The addition of the Intel XScale® core brings intelligence to the PCI Express*-to-PCI Bridges.

The 80333 integrates PCI Express*-to-PCI Bridges with the ATU as an integrated secondary PCI device. The Upstream PCI Express* port implements the PCI-to-PCI Bridge programming model according to the *PCI Express* Specification*, Revision 1.0a. The Primary Address Translation Unit is compliant with the definitions of an “application bridge” as found in the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a.

Figure 1 on page 10 is a functional block diagram of the 80333.

Figure 1. Intel® 80333 I/O Processor Functional Block Diagram



2.0 Features

The Intel® 80333 I/O processor combines the Intel XScale® core with powerful new features to create an intelligent I/O processor. This multi-device I/O processor is fully compliant with the *PCI Local Bus Specification*, Revision 2.3 and the *PCI Express* Specification*, Revision 1.0a. Features specific to the 80333 include the following:

- Intel XScale® core
- Application Accelerator Unit
- Address Translation Unit
- Memory Controller
- Peripheral Bus Interface
- Two I2C Bus Interface Units
- PCI Express* 2.5 GHz ×8 link
- Interrupt Controller Unit
- Messaging Unit
- Internal Bus
- Two DMA Controllers
- Two UART Units
- Eight GPIOs
- Two PCI Express*-to-PCI Bridges to secondary PCI-X 133 MHz Bus interfaces

The subsections that follow briefly overview each feature. Refer to the *Intel® 80333 I/O Processor Developer's Manual* for full technical descriptions.

2.1 Intel XScale® Core

The 80333 is based upon the Intel XScale® core. The core processor operates at a maximum frequency of 800 MHz. The instruction cache is 32 Kbytes in size and is 32-way set associative. Also, the core processor includes a data cache that is 32 Kbytes and is 32-way set associative, and a mini data cache that is 2 Kbytes and is two-way set associative.

2.2 PCI Express*-to-PCI Bridge Units

The 80333 provides PCI Express*-to-PCI Bridge units. These bridge units share a common upstream PCI Express* interface compliant with the *PCI Express* Specification*, Revision 1.0a. The PCI Express* interface supports a port lane width of eight, for up to 2 Gbytes/s per direction (4 Gbytes/s total) at 2.5 Gbits/s bit rate. The PCI-X secondary interfaces support 64-bit 133 MHz, compliant with the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a. These two secondary PCI bus interfaces are referred to as the 'A' and 'B' segment, where the 80333 Address Translation Unit resides on 'A' segment. The 'B' PCI bus interface can be used for slot expansion.

2.3 Address Translation Unit

An Address Translation Unit (ATU) allows PCI transactions direct access to the 80333 local memory. The ATU supports transactions between PCI address space and 80333 address space. Address translation for the ATU is controlled through programmable registers accessible from both the PCI interface and the Intel XScale® core. The PCI interface of the ATU is connected to the 80333 "A" Secondary PCI interface of the bridge. Upstream access to the PCI Express* interface is controlled by inverse decode with the address windows of the bridge. Dual access to registers allows flexibility in mapping the two address spaces. The ATU also supports the power management extended capability configuration header that as defined by the *PCI Bus Power Management Interface Specification*, Revision 1.1.

2.4 Memory Controller

The Memory Controller allows direct control of a DDR SDRAM memory subsystem. It features programmable chip selects and support for error correction codes (ECC). The memory controller may be configured for DDR SDRAM at 333 MHz (with 500 MHz and 667 MHz processors) or DDR-II SDRAM at 400 MHz (with 500 MHz and 800 MHz processors). The memory controller is dual-ported, with a dedicated interface for the Intel XScale® core Bus Interface Unit and a second interface to the Internal Bus. The memory controller supports pipelined access and arbitration control to maximize performance. The memory controller interface configuration support includes Unbuffered DIMMs, Registered DIMMs, and discrete DDR SDRAM devices.

External memory may be configured as host addressable memory or private 80333 memory utilizing the Address Translation Unit and Bridges.

2.5 Application Accelerator Unit

The Application Accelerator Unit (AA) provides low-latency, high-throughput data transfer capability between the AA unit, the 80333 local memory and the PCI bus. It executes data transfers from and to the 80333 local memory, from the PCI bus to the 80333 local memory, or from the 80333 local memory to the PCI bus. The AA unit performs XOR operations, computes parity, generates and verifies an eight byte data integrity field, performs memory block fills, and provides the necessary programming interface. The AA unit in the 80333 has been enhanced to support RAID 6 functionality.

2.6 Peripheral Bus Interface

The Peripheral Bus Interface Unit is a data communication path to the flash memory components or other peripherals of an 80333 hardware system. The PBI includes support for either 8/16 bit devices. To perform these tasks at high bandwidth, the bus features a burst transfer capability which allows successive 8/16-bit data transfers.

2.7 DMA Controller

The DMA Controller allows low-latency, high-throughput data transfers between PCI bus agents and the local memory. Two separate DMA channels accommodate data transfers to the PCI bus. Both channels include a local memory to local memory transfer mode. The DMA Controller supports chaining and unaligned data transfers. It is programmable through the Intel XScale® core only.

2.8 I²C Bus Interface Unit

The I²C (Inter-Integrated Circuit) Bus Interface Unit allows the Intel XScale® core to serve as a master and slave device residing on the I²C bus. The I²C unit uses a serial bus developed by Philips Semiconductor*, consisting of a two-pin interface. The bus allows the 80333 to interface to other I²C peripherals and microcontrollers for system management functions. It requires a minimum of hardware components for an economical system to relay status and reliability information on the I/O subsystem to an external device. Also refer to *I²C Peripherals for Microcontrollers* (Philips Semiconductor).

The 80333 includes two I²C bus interface units.

2.9 Messaging Unit

The Messaging Unit (MU) provides data transfer between the PCI system and the 80333. It uses interrupts to notify each system when new data arrives. The MU has four messaging mechanisms:

- Message Registers
- Doorbell Registers
- Circular Queues
- Index Registers

Each messaging mechanism allows a host processor or external PCI device and the 80333 to communicate through message passing and interrupt generation.

2.10 Internal Bus

The Internal Bus is a high-speed interconnect between internal units and Intel XScale® core processor. The Internal Bus operates at 333 MHz and is 64 bits wide.

2.11 UART Units

The 80333 includes two UART unit. The UART units allow the Intel XScale® core to serve as a master and slave device residing on the UART bus. The UART units use a serial bus consisting of a four-pin interface. The bus allows the 80333 to interface to other peripherals and microcontrollers. Also refer to *16550 Device Specification* (National Semiconductor*).

2.12 Interrupt Controller Unit

The Interrupt Controller Unit (ICU) aggregates interrupt sources both external and internal of the 80333 to the Intel XScale® core processor. The ICU supports high performance interrupt processing with direct interrupt service routine vector generation on a per source basis. Each source has programmability for masking, core processor interrupt input, and priority.

2.13 GPIO

The 80333 includes eight General Purpose I/O (GPIO) pins which can also be used as external interrupt inputs.

2.14 SMBus Unit

The SMBus (System Management Bus) Interface Unit allows the 80333 to serve as a slave device on the SMBus. SMBus is based on the principles of the I^2C bus and allows the 80333 to interface to system SMBus for external access and control of internal registers.

3.0 Package Information

The 80333 is offered in a Flip Chip Ball Grid Array (FCBGA) package. This is a full grid array package with 829 ball connections.

3.1 Functional Signal Descriptions

Table 1. Pin Description Nomenclature

Symbol	Description
C	Configuration
I	Input pin only
O	Output pin only
I/O	Pin may be either an input or output.
OD	Open Drain pin
PWR	Power pin
GND	Ground pin
-	Pin must be connected as described.
Sync(…)	Synchronous. Signal meets timings relative to a clock. Sync(B) Synchronous to **B_CLKIN** Sync(M) Synchronous to **M_CK[2:0]** Sync(A) Synchronous to **A_CLKIN** Sync(T) Synchronous to **TCK**
Async	Asynchronous. Inputs may be asynchronous relative to all clocks. All asynchronous signals are level-sensitive.
Rst(R)	The pin is reset with **PWRGD** or **RSTIN#**.
Rst(A)	The pin is reset with **A_RST#**. Note that **A_RST#** is asserted when **RSTIN#** or **PWRGD** is asserted.
Rst(B)	The pin is reset with **B_RST#**. Note that **B_RST#** is asserted when **RSTIN#** or **PWRGD** is asserted.
Rst(M)	The pin is reset with **M_RST#**. Note that **M_RST#** is asserted when **RSTIN#** or **PWRGD** is asserted or is asserted with software.
Rst(T)	The pin is reset with **TRST#**.

Table 2. DDR SDRAM Signals

Name	Count	Type	Description
M_CK[2:0]	3	O	**Memory Clocks** are used to provide the positive differential clocks to the external SDRAM memory subsystem.
M_CK[2:0]#	3	O	**Memory Clocks** are used to provide the negative differential clocks to the external SDRAM memory subsystem.
M_RST#	1	O Async	**Memory Reset** indicates when the memory subsystem has been reset with **RSTIN#** or **PWRGD** or a software reset.
MA[13:0]	14	O Sync(M), Rst(M)	**Memory Address Bus** carries the multiplexed row and column addresses to the SDRAM memory banks.
BA[1:0]	2	O Sync(M), Rst(M)	**SDRAM Bank Address** indicates which of the SDRAM internal banks are read or written during the current transaction.
RAS#	1	O Sync(M), Rst(M)	**SDRAM Row Address Strobe** indicates the presence of a valid row address on the Multiplexed Address Bus **MA[12:0]**.
CAS#	1	O Sync(M), Rst(M)	**SDRAM Column Address Strobe** indicates the presence of a valid column address on the Multiplexed Address Bus **MA[12:0]**.
WE#	1	O Sync(M), Rst(M)	**SDRAM Write Enable** indicates that the current memory transaction is a write operation.
CS[1:0]#	2	O Sync(M), Rst(M)	**SDRAM Chip Select** enables the SDRAM devices for a memory access (Physical banks 0 and 1).
CKE[1:0]	2	O Sync(M), Rst(M)	**SDRAM Clock Enable** enables the clocks for the SDRAM memory. Deasserting will place the SDRAM in self-refresh mode.
DQ[63:0]	64	I/O Sync(M), Rst(M)	**SDRAM Data Bus** carries 64-bit data to and from memory. During a data cycle, read or write data is present on one or more contiguous bytes. During write operations, unused pins are driven to determinate values.
CB[7:0]	8	I/O Sync(M), Rst(M)	**SDRAM ECC Check Bits** carry the 8-bit ECC code to and from memory during data cycles.
DQS[8:0]	9	I/O Sync(M), Rst(M)	**SDRAM Data Strobes** carry the strobe signals, output in write mode and input in read mode for source synchronous data transfer.
DM[8:0]	9	O Sync(M), Rst(M)	**SDRAM Data Mask** controls which bytes on the data bus should be written. When **DM[8:0]** is asserted, the SDRAM devices do not accept valid data from the byte lanes.
Total	120		

Table 3. DDR-II SDRAM Signals

Name	Count	Type	Description
DQS[8:0]#	9	I/O Sync(M) Rst(M)	**SDRAM Data Strobes** carry the differential strobe signals in DDR-II mode, output in write mode and input in read mode for source synchronous data transfer.
ODT[1:0]	2	O Sync(M) Rst(M)	**On Die Termination Control,** turns on SDRAM termination during writes.
DDRRES[2:1]	2	I/O	**Compensation For DDR OCD** (analog) DDR-II mode only.
Total	13		

Table 4. MISC SDRAM Signals

Name	Count	Type	Description
DDRCRES0	1	O	**Analog VSS Ref Pin** (analog) both **DDRSLWCRES** and **DDRIMPCRES** signals connect to this pin through a reference resistor.
DDRSLWCRES	1	I/O	**Compensation Voltage Reference** (analog) for DDR driver slew rate control connected through a resistor to **DDRCRES0**.
DDRIMPCRES	1	I/O	**Compensation Voltage Reference** (analog) for DDR driver impedance control connected through a resistor to **DDRCRES0**.
Total	3		

Table 5. Peripheral Bus Interface Signals

Name	Count	Type	Description
A[22:16]	7	O Rst(M)	**Address Bus 22:16** carries a demultiplexed version of address bits A22:16. During address (T_a), wait state (T_w) and data cycles (T_d) cycles, **A[22:16]** represents the upper seven address bits for the current access. **A[22:16]** allows the PBI interface to address up to 8 Mbytes per peripheral device. See "*Table 17, "Pin Multiplexing for Functional Modes" on page 36*" for strap inputs which are muxed onto **A[19:16]**, and "*Table 14, "Reset Strap Signals" on page 29*" for a functional description.
AD[15:0]	16	I/O Rst(M)	**Address/Data Bus** carries 16-bit physical addresses and 8- or 16-bit data to and from memory. During an address (T_a) cycle, bits 2-31 contain a physical word address (bits 0-1 indicate **SIZE**; see below). During a data (T_d) cycle, bits 0-7, or 0-15 contain read or write data, depending on the corresponding bus width. During write operations to 8-bit wide memory regions, the PBI drives unused bus pins high or low. **SIZE**, which comprises bits 0-1 of the AD lines during a T_a cycle, specifies the number of data transfers during the bus transaction. **AD1 AD0** 0 0 1 Transfer 0 1 2 Transfers 1 0 3 Transfers 1 1 4 Transfers See "*Table 17, "Pin Multiplexing for Functional Modes" on page 36*" for strap inputs which are muxed onto **AD[15:0]**, and "*Table 14, "Reset Strap Signals" on page 29*" for a functional description.
A[2:0]	3	O Rst(M)	**Address Bus 2:0** carries a demultiplexed version of bits 2:0 of the **AD[15:0]** bus. During an address (T_a) cycle, bits **A[2:0]** matches **AD[2:0]**. During a bursted read data (T_d) cycle, **A[2:0]** will represent the current byte address in the bursted transaction. **A[2:1]** are used for an 16-bit wide peripheral while **A[1:0]** are used for an 8-bit wide peripheral. See "*Table 17, "Pin Multiplexing for Functional Modes" on page 36*" for strap inputs which are muxed onto **A[2:0]**, and "*Table 14, "Reset Strap Signals" on page 29*" for a functional description.
ALE	1	O Rst(M)	**Address Latch Enable** indicates the transfer of a physical address. The pin is asserted during the first address cycle and deasserted during the second address cycle.
POE#	1	O Rst(M)	**Peripheral Output Enable** Indicates whether the bus access is a write or a read with respect to the I/O processor and is valid during the entire bus access. This pin may be used to control the **OE#** input on peripheral devices. 0 = Read 1 = Write
PWE#	1	O Rst(M)	**Peripheral Write Enable** indicates whether the bus access is a write or a read with respect to the I/O processor and is valid during the entire bus access. This pin is use for flash memory accesses and controls the **WE#** input on the ROM. 0 = Write 1 = Read
PCE[1]#	1	O Rst(M)	**Peripheral Chip Enables** specify which of the two memory address ranges are associated with current bus access. The pin remains valid during the entire bus access.
PCE[0]#	1	O Rst(M)	**Peripheral Chip Enables** specify which of the two memory address ranges are associated with current bus access. The pin remains valid during the entire bus access.
Total	31		

Table 6. PCI Express* Signals

Name	Count	Type	Description
REFCLK+/ REFCLK-	2	I	**PCI Express* Differential Clock In:** These pins receive a 100 MHz differential clock input from an external source. This clock is used as the reference clock for the PCI Express* circuitry.
PE0Tp[7:0]/ PE0Tn[7:0]	16	O	**PCI Express* Serial Data Transmit**: These eight differential output pairs carry data and embedded clock for the PCI Express* port 0 interface. • ×8 Mode: All **PE0Tp[7:0]** and **PE0Tn[7:0]** signals are used. • ×4 Mode: Only **PE0Tp[3:0]** and **PE0Tn[3:0]** signals are used.
PE0Rp[7:0]/ PE0Rn[7:0]	16	I	**PCI Express* Serial Data Receive**: These eight differential input pairs receive data and embedded clock for port 0. • ×8 Mode: All **PE0Rp[7:0]** and **PE0Rn[7:0]** signals are used. • ×4 Mode: Only **PE0Rp[3:0]** and **PE0Rn[3:0]** signals are used.
PE_RCOMPO	1	I	**PCI EXPRESS RCOMP**: Connected to external reference resistor. Output current path, used to compensate PCI Express* driver and RX termination.
PE_ICOMPI	1	I	**PCI EXPRESS RCOMP IN:** Connected to the same external resistor as **PE_RCOMPO** on the board, for input voltage sensing comparator.
Total	36		

Table 7. B PCI (Slot Expansion) Bus Signals (Sheet 1 of 2)

Name	Count	Type	Description
B_AD[31:0]	32	I/O Sync(B) Rst(B)	**B PCI Address/Data** is the multiplexed PCI address and lower 32 bits of the data bus.
B_AD[63:32]	32	I/O Sync(B) Rst(B)	**B PCI Address/Data** is the upper 32 bits of the PCI data bus driven during the data phase.
B_PAR	1	I/O Sync(B) Rst(B)	**B PCI Bus Parity** is even parity across **B_AD[31:0]** and **B_C/BE[3:0]#**.
B_PAR64	1	I/O Sync(B) Rst(B)	**B PCI Bus Upper DWORD Parity** is even parity across **B_AD[63:32]** and **B_C/BE[7:4]#**.
B_C/BE[7:0]#	8	I/O Sync(B) Rst(B)	**B PCI Bus Command and Byte Enables** are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables for **B_AD[63:0]**.
B_GNT[4]#	1	O Sync(B) Rst(B)	**B Secondary PCI Bus Grant** signals sent to device 4 on the B-segment PCI bus.
B_GNT[3]#	1	O Sync(B) Rst(B)	**B Secondary PCI Bus Grant** signals sent to device 3 on the B-segment PCI bus.
B_GNT[2]#	1	O Sync(B) Rst(B)	**B Secondary PCI Bus Grant** signal sent to device 2 on the B-segment PCI bus.
B_GNT[1]#	1	O Sync(B) Rst(B)	**B Secondary PCI Bus Grant** signal sent to device 1 on the B-segment PCI bus.
B_GNT[0]#	1	O Sync(B) Rst(B)	**B PCI Bus Grant** is the grant signal sent to device 0 on the B-segment PCI bus.
B_REQ64#	1	I/O Sync(B) Rst(B)	**B PCI Bus Request 64-Bit Transfer** indicates the attempt of a 64-bit transaction on the PCI bus. When the target is 64-bit capable, the target acknowledges the attempt with the assertion of **B_ACK64#**.
B_REQ[4]#	1	I Sync(B)	**B PCI Bus Requests** is the request signal for device 4 on the B-segment PCI bus.
B_REQ[3]#	1	I Sync(B)	**B PCI Bus Requests** is the request signal for device 3 on the B-segment PCI bus.
B_REQ[2]#/ B_HM66EN	1	I Sync(B)	**B PCI Bus Requests** is the request signal for device 2 on the B-segment PCI bus. **PCI 66 Enable** is used to determine when the slot is PCI 66 MHz capable. This signal is only valid for Hot-Plug 1-slot mode.
B_REQ[1]#	1	I Sync(B)	**B PCI Bus Requests** is the request signal for device 1 on the B-segment PCI bus.
B_REQ[0]#	1	I Sync(B)	**B PCI Bus Requests** are the request signals from device 0 on the B-segment secondary PCI bus.
B_ACK64#	1	I/O Sync(B) Rst(B)	**B PCI Bus Acknowledge 64-Bit Transfer** indicates that the device has positively decoded its address as the target of the current access and the target is willing to transfer data using the full 64-bit data bus.
B_FRAME#	1	I/O Sync(B) Rst(B)	**B PCI Bus Cycle Frame** is asserted to indicate the beginning and duration of an access.

Table 7. B PCI (Slot Expansion) Bus Signals (Sheet 2 of 2)

Name	Count	Type	Description
B_IRDY#	1	I/O Sync(B) Rst(B)	**B PCI Bus Initiator Ready** indicates the initiating agent's ability to complete the current data phase of the transaction. During a write, it indicates that valid data is present on the Address/Data bus. During a read, it indicates the processor is ready to accept the data.
B_TRDY#	1	I/O Sync(B) Rst(B)	**B PCI Bus Target Ready** indicates the target agent's ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the Address/Data bus. During a write, it indicates the target is ready to accept the data.
B_STOP#	1	I/O Sync(B) Rst(B)	**B PCI Bus Stop** indicates a request to stop the current transaction on the PCI bus.
B_DEVSEL#	1	I/O Sync(B) Rst(B)	**B PCI Bus Device Select** is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
B_LOCK#	1	I/O Sync(B) Rst(B)	**B PCI Bus Lock** indicates whether or not a transaction is establishing a LOCK across the bridge.
B_SERR#	1	I/O OD Sync(B) Rst(B)	**B PCI Bus System Error** is driven for address parity errors on the PCI bus.
B_PERR#	1	I/O Sync(B) Rst(B)	**B PCI Bus Parity Error** is asserted when a data parity error occurs during a PCI bus transaction.
B_M66EN	1	I/O	**B PCI Bus 66 MHz Enable** indicates the speed of the PCI bus. When this signal is sampled high the PCI bus speed is 66 MHz, when low, the bus speed is 33 MHz.
B_PME#	1	I Sync(B)	**Power Management Event** signal is used to request a change in the device or system power state.
B_PCIXCAP	1	I	**B PCI-X Capability** Analog pad that selects PCI/X mode and frequency capabilities. Non-standard, special purpose analog pin.
B_CLKO[4:0]	5	O	**B PCI Bus Output Clocks** are used to drive external logic on the secondary PCI bus.
B_CLKOUT	1	O	**B PCI Bus Output Clock** is used to drive **B_CLKIN** when secondary bus clocks are enabled.
B_CLKIN	1	I	**B PCI Bus Input Clock** provides the timing for all PCI transactions. Typically connected on the board to **B_CLKOUT**. Provides timing clock for all B-segment PCI interfaces.
B_RST#	1	O	**B PCI BUS RESET** is an output based on **RSTIN#** or **PWRGD**. It brings PCI-specific registers, sequencers, and signals to a consistent state. When **RSTIN#** is asserted or **PWRGD** is deasserted, or the secondary bridge reset bit is asserted, it causes **B_RST#** to assert and: • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • open drain signals such as **B_SERR#** are floated **B_RST#** may be asynchronous to **B_CLKIN** when asserted or deasserted. Although asynchronous, deassertion must be guaranteed to be a clean, bounce-free edge.
B_RCOMP	1	I/O	**PCI Resistor Compensation Pin** is an analog pad that connects to a board resistor to control all B segment PCI output driver strengths (analog).
Total	106		

Table 8. A PCI (IOP) Bus Signals (Sheet 1 of 2)

Name	Count	Type	Description
A_AD[31:0]	32	I/O Sync(A) Rst(A)	**A PCI Address/Data** is the multiplexed PCI address and lower 32 bits of the data bus.
A_AD[63:32]	32	I/O Sync(A) Rst(A)	**A PCI Address/Data** is the upper 32 bits of the PCI data bus.
A_PAR	1	I/O Sync(A) Rst(A)	**A PCI Bus Parity** is even parity across **A_AD[31:0]** and **A_C/BE[3:0]#**.
A_PAR64	1	I/O Sync(A) Rst(A)	**A PCI Bus Upper DWORD Parity** is even parity across **A_AD[63:32]** and **A_C/BE[7:4]#**.
A_C/BE[3:0]#	4	I/O Sync(A) Rst(A)	**A PCI Bus Command and Byte Enables** are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as the byte enables for **A_AD[31:0]**.
A_C/BE[7:4]#	4	I/O Sync(A) Rst(A)	**A PCI Byte Enables** are used as byte enables for **A_AD[63:32]** during secondary PCI data phases.
A_REQ64#	1	I/O Sync(A) Rst(A)	**A PCI Bus Request 64-Bit Transfer** indicates the attempt of a 64-bit transaction on the secondary PCI bus. When the target is 64-bit capable, the target acknowledges the attempt with the assertion of **A_ACK64#**.
A_ACK64#	1	I/O Sync(A) Rst(A)	**A PCI Bus Acknowledge 64-Bit Transfer** indicates that the device has positively decoded its address as the target of the current access, indicates the target is willing to transfer data using 64 bits.
A_FRAME#	1	I/O Sync(A) Rst(A)	**A PCI Bus Cycle Frame** is asserted to indicate the beginning and duration of an access.
A_IRDY#	1	I/O Sync(A) Rst(A)	**A PCI Bus Initiator Ready** indicates the initiating agent's ability to complete the current data phase of the transaction. During a write, it indicates that valid data is present on the secondary Address/Data bus. During a read, it indicates the processor is ready to accept the data.
A_TRDY#	1	I/O Sync(A) Rst(A)	**A PCI Bus Target Ready** indicates the target agent's ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the secondary Address/Data bus. During a write, it indicates the target is ready to accept the data.
A_STOP#	1	I/O Sync(A) Rst(A)	**A PCI Bus Stop** indicates a request to stop the current transaction on the secondary PCI bus.
A_DEVSEL#	1	I/O Sync(A) Rst(A)	**A PCI Bus Device Select** is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
A_SERR#	1	I/O OD Sync(A) Rst(A)	**A PCI Bus System Error** is driven for address parity errors on the secondary PCI bus.

Table 8. A PCI (IOP) Bus Signals (Sheet 2 of 2)

Name	Count	Type	Description
A_RST#	1	O Async	**A PCI Bus Reset** is an output based on **RSTIN#** or **PWRGD**. It brings PCI-specific registers, sequencers, and signals to a consistent state. When **RSTIN#** is asserted or **PWRGD** is deasserted, or the secondary bridge reset bit is asserted, it causes **A_RST#** to assert and: • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • Open drain signals such as **A_SERR#**are floated. **A_RST#** may be asynchronous to **A_CLKIN** when asserted or deasserted. Although asynchronous, deassertion must be ensured to be a clean, bounce-free edge.
A_PERR#	1	I/O Sync(A) Rst(A)	**A PCI Bus Parity Error** is asserted when a data parity error during a secondary PCI bus transaction.
A_LOCK#	1	I/O Sync(A) Rst(A)	**A PCI Bus Lock** indicates the need to perform an atomic operation on the secondary PCI bus.
A_CLKO[3:0]	4	O	**A PCI Bus Output Clocks** are used to drive external logic on the secondary PCI bus.
A_CLKOUT	1	O	**A PCI Bus Output Clock** is used to drive **A_CLKIN** when the IO processor provides secondary bus clocks.
A_CLKIN	1	I	**A PCI Bus Input Clock** provides the timing for all PCI transactions. Typically connected on the board to **A_CLKOUT**. Provides the timing clock for all A segment PCI interfaces.
A_M66EN	1	I/O	**A PCI Bus 66 MHz Enable** indicates the speed of the secondary PCI bus. When this signal is high, the bus speed is 66 MHz and when it is low, the bus speed is 33 MHz.
A_PME#	1	I Sync(A)	**Power Management Event** signal is used to request a change in the device or system power state.
A_REQ[3:0]#	4	I Sync(A)	**A PCI Bus Requests** are the request signals from devices 3 through 0 on the A PCI bus.
A_GNT[3:0]#	4	O Sync(A) Rst(A)	**A PCI Bus Grant** are grant signals sent to devices 3 through 0 on the A PCI bus.
A_PCIXCAP	1	I	**A PCI-X Capability** is an analog pad that selects PCI/X mode and frequency capabilities. Non-standard, special purpose analog pin.
A_RCOMP	1	I/O	**PCI Resistor Compensation Pin** is an analog pad that connects to the board resistor to control all A segment PCI output driver strengths (analog).
Total	103		

Table 9. Interrupt Signals

Name	Count	Type	Description
XINT[7:0]#	8	I Async	**Interrupt Inputs: XINT[7:0]#** interrupts are directed to the input of the IOAPIC, or the Interrupt Controller inputs. When directed to the Interrupt Controller inputs, then the inputs can be steered to either the FIQ or IRQ internal interrupt input of the core. By default, **XINT[7:4]#** interrupts are directed to the input of the B IOAPIC and **XINT[3:0]#** interrupts are directed to the input of the A IOAPIC. These interrupt pins are level sensitive.
HPI#	1	I Async	**High Priority Interrupt** causes a high priority interrupt to the I/O processor. This pin is level-detect only and is internally synchronized.
Total	9		

Table 10. I^2C/SMBus Signals

Name	Count	Type	Description
SCL0	1	I/O	I^2C **Clock** provides synchronous operation of the I^2C bus zero.
SCD0	1	I/O	I^2C **Data** is used for data transfer and arbitration of the I^2C bus zero.
SCL1/SCLK	1	I/O	**I^2C Clock** provides synchronous operation of the I^2C bus zero. **SM Bus Clock** provides synchronous operation of the SM bus.
SCD1/SDTA	1	I/O	**I^2C Data** is used for data transfer and arbitration of the I^2C bus zero. **SM Bus Data** is used for data transfer and arbitration of the SM bus.
Total	4		

Table 11. Hot-Plug Controller Signals for Parallel 1-slot, No-Glue

Name	Count	Type	Description
B_HPWRFLT#	1	I Sync(B) Rst(B)	**Parallel Mode Hot-Plug Power Controller Fault** indication for over-current/under-volt status. When asserted, the device (when enabled) may assert a slot reset and disconnects the slot from the bus.
B_HMRL#	1	I Sync(B) Rst(B)	**Parallel Mode Hot-Plug Status** of the slot 1 MRL sensor switch, when asserted it indicates the MRL latch is closed. When a platform does not support MRL sensors, this must be wired to a logic low level.
B_HPRSNT2#	1	I Sync(B)	**Parallel Mode Hot-Plug PRSNT2** signal is used to indicate whether a card is installed in the slot and its power requirements. These signals are directly connected to the present bits on the PCI card.
B_HPWREN	1	O Sync(B) Rst(B)	**Parallel Mode Hot-Plug Power Enable** signal connected to on-board slot specific power controller to regulate current and voltage of the slot.
B_HPRSNT1#	1	I Sync(B) Rst(B)	**Parallel Mode Hot-Plug PRSNT1** signal is used to indicate whether a card is installed in the slot and its power requirements. These signals are directly connected to the present bits on the PCI card.
B_HATNLED#	1	O Sync(B) Rst(B)	**Parallel Mode Hot-Plug Attention** indicator LED signal that is yellow or amber in color.
B_HPWRLED#	1	O Sync(B) Rst(B)	**Parallel Mode Hot-Plug Power Indicator LED** signal that is green in color.
B_HBUTTON#	1	I Sync(B) Rst(B)	**Parallel Mode Hot-Plug Attention Button** input from the slot. When low, this indicates that the operator has requested attention. When an attention button is not implemented, this input must be wired to a logic high level.
B_HRESET#	1	O	**Parallel Mode Reset Output Signal**. This output signal is always “on”, therefore, it does not tri-state during boundary scan.
Total	9		

Table 12. UART Signals (Sheet 1 of 2)

Name	Count	Type	Description
GPIO[0]/ U0_RXD	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Serial Input**: Serial data input from device pin to receive shift register.
GPIO[1]/ U0_TXD	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Serial Output**: Composite serial data output to the communications link-peripheral, modem, or data set. The TXD signal is set to the MARKING (logic 1) state upon a Reset operation.
GPIO[2]/ U0_CTS#	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Clear To Send**: When low, this pin indicates that the receiving UART is ready to receive data. When the receiving UART deasserts **CTS#** high, the transmitting UART should stop transmission to prevent overflow of the receiving UARTs buffer. The **CTS#** signal is a modem-status input whose condition may be tested by the host processor or by the UART when in Autoflow Mode as described below: **Non-Autoflow Mode**: When not in Autoflow Mode, bit 4 (CTS) of the Modem Status register (MSR) indicates the state of **CTS#**. Bit 4 is the complement of the **CTS#** signal. Bit 0 (DCTS) of the Modem Status register indicates whether the **CTS#** input has changed state since the previous reading of the Modem Status register. **CTS#** has no effect on the transmitter. The user may program the UART to interrupt the processor when DCTS changes state. The programmer may then stall the outgoing data stream by starving the transmit FIFO or disabling the UART with the IER register. ***Note:*** When UART transmission is stalled by disabling the UART, the user may not receive an MSR interrupt when **CTS#** reasserts. This occurs because disabling the UART also disables interrupts. As a workaround, the user may use Auto CTS in Autoflow Mode, or program the **CTS#** pin to interrupt. **Autoflow Mode**: ***Note:*** In Autoflow Mode, the UART Transmit circuitry will check the state of **CTS#** before transmitting each byte. When **CTS#** is high, no data is transmitted.
GPIO[3]/ U0_RTS#	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Request To Send**: When low, this informs the remote device that the UART is ready to receive data. A reset operation sets this signal to its Inactive (high) state. LOOP mode operation holds this signal in its Inactive state. **Non-Autoflow Mode**: The **RTS#** output signal may be asserted by setting bit 1 (RTS) of the Modem Control register to a 1. The RTS bit is the complement of the **RTS#** signal. **Autoflow Mode**: **RTS#** is automatically asserted by the Autoflow circuitry when the Receive buffer exceeds its programmed threshold. It is deasserted when enough bytes are removed from the buffer to lower the data level back to the threshold.

Table 12. UART Signals (Sheet 2 of 2)

Name	Count	Type	Description
GPIO[4]/ U1_RXD	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Serial Input**: Serial data input from device pin to receive shift register.
GPIO[5]/ U1_TXD	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Serial Output**: Composite serial data output to the communications link-peripheral, modem, or data set. The TXD signal is set to the MARKING (logic 1) state upon a Reset operation.
GPIO[6]/ U1_CTS#	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Clear To Send**: When low, this pin indicates that the receiving UART is ready to receive data. When the receiving UART deasserts **CTS#** high, the transmitting UART should stop transmission to prevent overflow of the receiving UARTs buffer. The **CTS#** signal is a modem-status input whose condition may be tested by the host processor or by the UART when in Autoflow Mode as described below: **Non-Autoflow Mode**: When not in Autoflow Mode, bit 4 (CTS) of the Modem Status register (MSR) indicates the state of **CTS#**. Bit 4 is the complement of the **CTS#** signal. Bit 0 (DCTS) of the Modem Status register indicates whether the **CTS#** input has changed state since the previous reading of the Modem Status register. **CTS#** has no effect on the transmitter. The user may program the UART to interrupt the processor when DCTS changes state. The programmer may then stall the outgoing data stream by starving the transmit FIFO or disabling the UART with the IER register. ***Note:*** When UART transmission is stalled by disabling the UART, the user may not receive an MSR interrupt when **CTS#** reasserts. This occurs because disabling the UART also disables interrupts. As a workaround, the user may use Auto CTS in Autoflow Mode, or program the **CTS#** pin to interrupt. **Autoflow Mode:** ***Note:*** In Autoflow Mode, the UART Transmit circuitry will check the state of **CTS#** before transmitting each byte. When **CTS#** is high, no data is transmitted.
GPIO[7]/ U1_RTS#	1	I/O	**General Purpose I/O**: These pins may be selected on a per pin basis as general purpose inputs or outputs. The default mode is a general purpose input. **Request To Send**: When low, this informs the remote device that the UART is ready to receive data. A reset operation sets this signal to its Inactive (high) state. LOOP mode operation holds this signal in its Inactive state. **Non-Autoflow Mode**: The **RTS#** output signal may be asserted by setting bit 1 (RTS) of the Modem Control register to a 1. The RTS bit is the complement of the **RTS#** signal. **Autoflow Mode**: **RTS#** is automatically asserted by the Autoflow circuitry when the Receive buffer exceeds its programmed threshold. It is deasserted when enough bytes are removed from the buffer to lower the data level back to the threshold.
Total	8		

Table 13. Test and Miscellaneous Signals

Name	Count	Type	Description
TCK	1	I	**Test Clock** provides clock input for IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the device on the rising clock edge and data is clocked out on the falling clock edge.
TDI	1	I Sync(T)	**Test Data Input** is the JTAG serial input pin. **TDI** is sampled on the rising edge of **TCK**, during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pull-up to ensure proper operation when this pin is not being driven.
TDO	1	O Sync(T) Rst(T)	**Test Data Output** is the serial output pin for the JTAG feature. **TDO** is driven on the falling edge of **TCK** during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, **TDO** floats. The behavior of **TDO** is independent of **RSTIN#** or **PWRGD**.
TRST#	1	I Async	**Test Reset** asynchronously resets the Test Access Port controller function of IEEE 1149 Boundary Scan Testing (JTAG). This pin has a weak internal pull-up.
TMS	1	I Sync(T)	**Test Mode Select** is sampled on the rising edge of **TCK** to select the operation of the test logic for IEEE 1149 Boundary Scan testing. This pin has a weak internal pull-up.
N/C	7	-	**No Connect**. Do not connect to any signal, power or ground.
PWRDELAY	1	I Async	**Power Fail Delay** is used to delay the reset of the memory controller in a power-fail condition. This allows the self-refresh command to be sent to the DDR SDRAM array.
PWRGD	1	I Async	**Power Supply Good**: Signal that specifies that the motherboard power supply has stabilized. This signal is used to asynchronously reset the 80333 when it is low. The low period of this signal must be long enough for the system power supply to stabilize and for the base PLLs to lock. ***Note:*** This is the same signal as PERST# which is described in the *PCI Express* Card Electromechanical Specification*, Revision 1.0a.
RSTIN#	1	I Async	**Reset Input** brings PCI-specific registers, sequencers, and signals to a consistent state. When **RSTIN#** is asserted: • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • Open drain signals such as **B_SERR#** are floated. **RSTIN#** may be asynchronous to **B_CLKIN** when asserted or deasserted. Although asynchronous, deassertion must be ensured to be a clean, bounce-free edge.
Total	15		

Table 14. Reset Strap Signals (Sheet 1 of 2)

Name	Count	Type	Description
RETRY	1	C	**Configuration Retry Mode**: **RETRY** is latched on the rising (asserting) edge of PWRGD and determines when the PCI interface of the ATU will disable PCI configuration cycles by signaling a retry until the configuration cycle retry bit is cleared in the PCI configuration and status register. 0 = Configuration Cycles enabled (Requires pull down resistor.) 1 = Configuration Retry enabled in the ATU (Default mode) ***Note:*** Muxed onto signal **AD[6]**, see Table 17, "Pin Multiplexing for Functional Modes" on page 36.
CORE_RST#	1	C	**Core Reset Mode** is latched on the rising (asserting) edge of PWRGD and determines when the Intel XScale® core is held in reset until the processor reset bit is cleared in PCI configuration and status register. 0 = Hold in reset. (Requires pull-down resistor.) 1 = Do not hold in reset. (Default mode) ***Note:*** Muxed onto signal **AD[5]**, see Table 17, "Pin Multiplexing for Functional Modes" on page 36.
P_BOOT16#	1	C	**Bus Width** is latched on the rising (asserting) edge of PWRGD, it sets the default bus width for the PBI Memory Boot window. 0 = 16 bits wide (Requires a pull-down resistor.) 1 = 8 bits wide (Default mode) ***Note:*** Muxed onto signal **AD[4]**, see Table 17, "Pin Multiplexing for Functional Modes" on page 36.
MEM_TYPE	1	C	**Memory Type**: **MEM_TYPE** is latched on the rising (asserting) edge of PWRGD and it defines the speed of the DDR SDRAM interface. 0 = DDR-II SDRAM at 400 MHz (Required pull-down resistor.) 1 = DDR SDRAM at 333 MHz (Default mode) ***Note:*** Muxed onto signal **AD[2]**, see Table 17, "Pin Multiplexing for Functional Modes" on page 36.
A_PCIX133EN	1	C	**PCI Bus Segment 'A' 133 MHz Enable: A_PCIX133EN** is latched on the rising (asserting) edge of **PWRGD** and it determines the maximum PCI-X mode operating frequency. 0 = 100 MHz enabled (Requires pull down resistor). 1 = 133 MHz enabled (Default mode). ***Note:*** Muxed onto signal **AD[3]**, see Table 17, "Pin Multiplexing for Functional Modes" on page 36.
B_PCIX133EN	1	C	**PCI Bus Segment 'B' 133 MHz Enable**: **B_PCIX133EN** latched on rising (asserting) edge of **PWRGD** and determines maximum PCI-X mode operating frequency. 0 = 100 MHz enabled (Requires pull down resistor.) 1 = 133 MHz enabled (Default mode) ***Note:*** Muxed onto signal **AD[10]**, see Table 17, "Pin Multiplexing for Functional Modes" on page 36.

Table 14. Reset Strap Signals (Sheet 2 of 2)

Name	Count	Type	Description
B_HSLOT[3:0]	4	C	**Number of Slots**: **B_HSLOT[3:0]** latched on rising (asserting) edge of **PWRGD** and indicates when the 'B' PCI-X bus interface Standard Hot-Plug Controller is enabled, the total number of slots in both Hot-Plug enabled mode and disabled mode, and the Hot-Plug mode. **B_HSLOT[3]** enables Hot-Plug when high and disables Hot-Plug when low. **Hot-Plug disabled** / **Hot-Plug enabled** 0000 = 1 slot / 1000 = reserved 0001 = 2 slots / 1001 = reserved 0010 = 3 slots / 1010 = reserved 0011 = 4 slots / 1011 = reserved 0100 = 5 slots / 1100 = reserved 0101 = 6 slots / 1101 = reserved 0110 = 7 slots / 1110 = reserved 0111 = 8 slots / 1111 = Parallel 1-slot-no-glue ***Note:*** 1111 is Default mode. ***Note:*** Muxed onto signal **AD[15:12]**, see Table 17, "Pin Multiplexing for Functional Modes" on page 36.
SMB_MA5 **SMB_MA3** **SMB_MA2** **SMB_MA1**	4	C	**Manageability Address (MA)**: latched on rising (asserting) edge of **PWRGD** and maps to MA bit 5, 3, 2, and 1, where MA bits[7:0] represent the address the SMBus slave port will respond to when access is attempted. 0 = (Requires pull down resistor.) 1 = (Default mode) ***Note:*** Muxed onto signal **A[19:16]**, see Table 17, "Pin Multiplexing for Functional Modes" on page 36.
PCIODT_EN	1	C	**PCI Bus ODT Enable**: **PCIODT_EN** is latched on the rising (asserting) edge of **PWRGD**, and determines when the PCI-X interface will have On-Die Termination enabled. **PCIODT_EN** is valid for both A and B segments. The following signals are affected by **PCIODT_EN**: **A_ACK64#**, **A_AD[63:32]**, **A_C/BE[7:4]#**, **A_DEVSEL#**, **A_FRAME#**, **A_IRDY#**, **A_LOCK#**, **A_M66EN**, **A_PAR64**, **A_PERR#**, **A_REQ[3:0]#**, **A_REQ64#**, **A_SERR#**, **A_STOP#**, **A_TRDY#**, **B_ACK64#**, **B_AD[63:32]**, **B_C/BE[7:4]#**, **B_DEVSEL#**, **B_FRAME#**, **B_IRDY#**, **B_LOCK#**, **B_M66EN**, **B_PAR64**, **B_PERR#**, **B_REQ[4:0]#**, **B_REQ64#**, **B_SERR#**, **B_STOP#**, **B_TRDY#**, **XINT[7:0]#** 0 = ODT disabled (Requires pull-down resistor). 1 = ODT enabled (Default mode). ***Note:*** Muxed onto signal **A[20]**, see Table 17, "Pin Multiplexing for Functional Modes" on page 36.
PD1	1	C	**Pull-down Resistor** is required for default mode. ***Note:*** Muxed onto signal **AD[7]**, see Table 17, "Pin Multiplexing for Functional Modes" on page 36.
Total	16		

Table 15. Power and Ground Pins

Name	Count	Type	Description
$V_{CCPLL[1-5]}$	5	PWR	**PLL 1-5 Power** is a separate V_{CC15} supply ball for the phase lock loop clock generator. It is to be connected to the board V_{CC15} plane. Each V_{CCPLL} requires a low-pass filter circuit to reduce noise-induced clock jitter and its effects on timing relationships. See the *Intel® 80333 I/O Processor Design Guide* for more information.
V_{CC33}	49	PWR	**3.3 V Power** balls to be connected to a 3.3 V power board plane.
$V_{CC25/18}$	29	PWR	**2.5 V/1.8 V Power** balls to be connected to a 2.5 V or 1.8 V power board plane, dependent on DDR or DDRII mode.
V_{CC15}	56	PWR	**1.5 V Power** balls to be connected to a 1.5 V power board plane. VCC15 = core VCC15E = PCI Express*
V_{CC13}	7	PWR	**1.3 V Power** balls to be connected to a 1.35 V power board plane.
PE_VCCBG	1	PWR	**PCI Express* Band Gap Analog Ref Power**: 2.5 V power for analog reference circuit, separated from all other VCC signals. Requires a low-pass filter.
DDR_VREF	1	PWR	**SDRAM Voltage Reference** is used to supply the reference voltage to the differential inputs of the memory controller pins.
V_{SS}	218	GND	**Ground** balls to be connected to a ground board plane.
$V_{SSA[1-5]}$	5	GND	**Analog Ground** balls need to be connected to the appropriate V_{CCPLL} filter, and not to board ground.
PE_VSSBG	1	GND	**PCI Express* Band Gap Analog Ground:** Ground for analog reference circuit, separated from all other VSS signals.

Table 16. Pin Mode Behavior (Sheet 1 of 4)

Pin	Reset	Norm	ECC Off	32-Bit DDR	32-Bit B_PCI	32-Bit A_PCI
M_CK[2:0]	X[1]	VO	VO	VO	-	-
M_CK[2:0]#	X[1]	VO	VO	VO	-	-
M_RST#	0	VO	VO	VO	-	-
MA[13:0]	0†	VO	VO	VO	-	-
BA[1:0]	0†	VO	VO	VO	-	-
RAS#	1†	VO	VO	VO	-	-
CAS#	1†	VO	VO	VO	-	-
WE#	1†	VO	VO	VO	-	-
CS[1:0]#	1†	VO	VO	VO	-	-
CKE[1:0]	0†	VO	VO	VO	-	-
DQ[63:32]	Z†	VB	VB	ID,Z	-	-
DQ[31:0]	Z†	VB	VB	VB	-	-
CB[7:0]	Z†	VB	VB	VB	-	-
DQS[8]	Z†	VB	ID,Z	VB	-	-
DQS[7:4]	Z†	VB	VB	ID,Z	-	-
DQS[3:0]	Z†	VB	VB	VB	-	-
DQS[8]#	Z†	VB	ID,Z	VB	-	-
DQS[7:4]#	Z†	VB	VB	ID,Z	-	-
DQS[3:0]#	Z†	VB	VB	VB	-	-
DM[8]	Z†	VO	Z	VO	-	-
DM[7:4]	Z†	VO	VO	Z	-	-
DM[3:0]	Z†	VO	VO	VO	-	-
DDR_VREF	VI	VI	VI	VI	-	-
ODT[1:0][2]	0	VO	VO	VO	-	-
DDRRES[2:1]	Z†	VB	VB	VB	-	-
DDRCRES0	VO	VO	VO	VO	-	-
DDRSLWCRES	VB	VB	VB	VB	-	-
DDRIMPCRES	VB	VB	VB	VB	-	-
A[22:16]	H	VO	-	-	-	-
AD[15:0]	H	VB	-	-	-	-
A[2:0]	H	VO	-	-	-	-
ALE	0	VO	-	-	-	-

Notes:

1 = driven to V_{CC}
0 = driven to V_{SS}
X = driven to unknown state
ID = the input is disabled
H = pulled up to V_{CC}
PD = pull-up disabled
AO = analog output level

L = pulled down to V_{SS}
Z = output disabled (floats)
VB = acts like a Valid Bidirectional pin
VO = a Valid Output level is driven
VI = Need to drive a Valid Input level
† = After power fail sequence completes
‡ = Caused by Hi-Z from mode pins only

1. Clocks become valid right before M_RST# deasserts.
2. ODT signal to be low during power up and initialization per DDR-II JEDEC specification.
3. High impedance common mode DC voltage driven per *PCI Express* Specification*, Revision 1.0.
4. Input Disabled, but termination on, per *PCI Express* Specification*, Revision 1.0.
5. Hot-Plug Controller signals are pulled up when SHPC is disabled (B_HSLOT[3] = 0 on rising edge of PWRGD.)

Table 16. Pin Mode Behavior (Sheet 2 of 4)

Pin	Reset	Norm	ECC Off	32-Bit DDR	32-Bit B_PCI	32-Bit A_PCI
POE#	1	VO	-	-	-	-
PWE#	1	VO	-	-	-	-
PCE[1]#	H	VO	-	-	-	-
PCE[0]#	H	VO	-	-	-	-
REFCLK+ REFCLK-	VI	VI	-	-	-	-
PE0Tp[7:0] PE0Tn[7:0]	Z[3]	VO	-	-	-	-
PE0Rp[7:0] PE0Rn[7:0]	ID[4]	VI	-	-	-	-
PE_RCOMPO	VI	VI				
PE_ICOMPI	VI	VI				
B_AD[63:32]	0	VB	-	-	H	-
B_AD[31:0]	0	VB	-	-	VB	-
B_PAR	0	VB	-	-	VB	-
B_PAR64	Z	VB	-	-	H	-
B_C/BE[7:4]#	0	VB	-	-	H	-
B_C/BE[3:0]#	0	VB	-	-	VB	
B_GNT[4:0]#	H	VO	-	-	-	-
B_REQ64#	VO	VB	-	-	-	-
B_REQ[4:0]#	VI	VI	-	-	-	-
B_ACK64#	Z	VB	-	-	-	-
B_FRAME#	Z	VB	-	-	-	-
B_IRDY#	Z	VB	-	-	-	-
B_TRDY#	VO	VB	-	-	-	-
B_STOP#	VO	VB	-	-	-	-
B_DEVSEL#	VO	VB	-	-	-	-
B_LOCK#	Z	VB	-	-	-	-
B_SERR#	Z	VB	-	-	-	-
B_CLKIN	VI	VI	-	-	-	-
PWRGD	VI	VI	-	-	-	-
RSTIN#	VI	VI	-	-	-	-
B_RST#	VO	VO	-	-	-	-

Notes:

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H = pulled up to V_{CC}
PD = pull-up disabled
AO = analog output level

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1. Clocks become valid right before M_RST# deasserts.
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4. Input Disabled, but termination on, per *PCI Express* Specification*, Revision 1.0.
5. Hot-Plug Controller signals are pulled up when SHPC is disabled (B_HSLOT[3] = 0 on rising edge of PWRGD.)

Table 16. Pin Mode Behavior (Sheet 3 of 4)

Pin	Reset	Norm	ECC Off	32-Bit DDR	32-Bit B_PCI	32-Bit A_PCI
B_PERR#	Z	VB	-	-	-	-
B_M66EN	VB	VB	-	-	-	-
B_PME#	VI	VI				
B_PCIXCAP	VI	VI	-	-	-	-
B_CLKO[4:0]	VO	VO	-	-	-	-
B_CLKOUT	VO	VO	-	-	-	-
A_AD[63:32]	Z	VB	-	-	-	H
A_AD[31:0]	0	VB	-	-	-	-
A_PAR	0	VB	-	-	-	-
A_PAR64	Z	VB	-	-	-	H
A_C/BE[3:0]#	0	VB	-	-	-	-
A_C/BE[7:4]#	Z	VB	-	-	-	H
A_REQ64#	VO	VB	-	-	-	-
A_ACK64#	Z	VB	-	-	-	-
A_FRAME#	Z	VB	-	-	-	-
A_IRDY#	Z	VB	-	-	-	-
A_TRDY#	VO	VB	-	-	-	-
A_STOP#	VO	VB	-	-	-	-
A_DEVSEL#	VO	VB	-	-	-	-
A_SERR#	Z	VB	-	-	-	-
A_RST#	VO	VO	-	-	-	-
A_PERR#	Z	VB	-	-	-	-
A_LOCK#	Z	VB	-	-	-	-
A_CLKO[3:0]	VO	VO	-	-	-	-
A_CLKOUT	VO	VO	-	-	-	-
A_CLKIN	VI	VI	-	-	-	-
A_M66EN	VB	VB	-	-	-	-
A_PME#	VI	VI				
A_REQ[3:0]#	VI	VI	-	-	-	-
A_GNT[3:0]#	H	VO	-	-	-	-
A_PCIXCAP	VI	VI	-	-	-	-
A_RCOMP	AO	AO	-	-	-	-

Notes:

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H = pulled up to V_{CC}
PD = pull-up disabled
AO = analog output level

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3. High impedance common mode DC voltage driven per *PCI Express* Specification*, Revision 1.0.
4. Input Disabled, but termination on, per *PCI Express* Specification*, Revision 1.0.
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Table 16. Pin Mode Behavior (Sheet 4 of 4)

Pin	Reset	Norm	ECC Off	32-Bit DDR	32-Bit B_PCI	32-Bit A_PCI
B_RCOMP	AO	AO	-	-	-	-
XINT[7:4]#	VI	VI	-	-	-	-
XINT[3:0]#	VI	VI	-	-	-	-
HPI#	VI	VI	-	-	-	-
B_HPWRFLT# (5)	VI	VI	-	-	-	-
B_HMRL# (5)	VI	VI	-	-	-	-
B_HPRSNT2# (5)	VI	VI	-	-	-	-
B_HPWREN (5)	Z	VO	-	-	-	-
B_HPRSNT1# (5)	VI	VI	-	-	-	-
B_HATNLED# (5)	Z	VO	-	-	-	-
B_HPWRLED# (5)	Z	VO	-	-	-	-
B_HBUTTON# (5)	VI	VI	-	-	-	-
SCL0, **SCD0**, **SCL1/ SCLK**, **SCD1/ SDTA**	H	VB	-	-	-	-
GPIO[3:0]/ U0_RTS#, **U0_CTS#**, **U0_TXD**, **U0_RXD**,	VI	VB	-	-	-	-
GPIO[7:4]/ U1_RTS#, **U1_CTS#**, **U1_TXD**, **U1_RXD**	VI	VB	-	-	-	-
TCK	VI	VI	-	-	-	-
TDI	H	H	-	-	-	-
TDO	VO†	VO	-	-	-	-
TRST#	H	H	-	-	-	-
TMS	H	H	-	-	-	-
PWRDELAY	VI	VI	-	-	-	-
PWRGD	VI	VI	-	-	-	-
NC[3:0]	H	H	-	-	-	-

Notes:

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X = driven to unknown state
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H = pulled up to V_{CC}
PD = pull-up disabled
AO = analog output level

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Table 17. Pin Multiplexing for Functional Modes

Pin	Reset Straps
A[20]	PCIODT_EN
AD[15]	B_HSLOT[3]
AD[14]	B_HSLOT[2]
AD[13]	B_HSLOT[1]
AD[12]	B_HSLOT[0]
AD[10]	B_PCIX133EN
AD[7]	PD1
AD[6]	RETRY
AD[5]	CORE_RST#
AD[4]	P_BOOT16#
AD[3]	A_PCIX133EN
AD[2]	MEM_TYPE
A[19]	SMB_MA5
A[18]	SMB_MA3
A[17]	SMB_MA2
A[16]	SMB_MA1
SCL1/SCLK	-
SCD1/SDTA	-
GPIO[0]/U0_RXD	-
GPIO[1]/U0_TXD	-
GPIO[2]/U0_CTS#	-
GPIO[3]/U0_RTS#	-
GPIO[4]/U1_RXD	-
GPIO[5]/U1_TXD	-
GPIO[6]/U1_CTS#	-
GPIO[7]/U1_RTS#	-

Figure 2. 829-Ball FCBGA Package Diagram

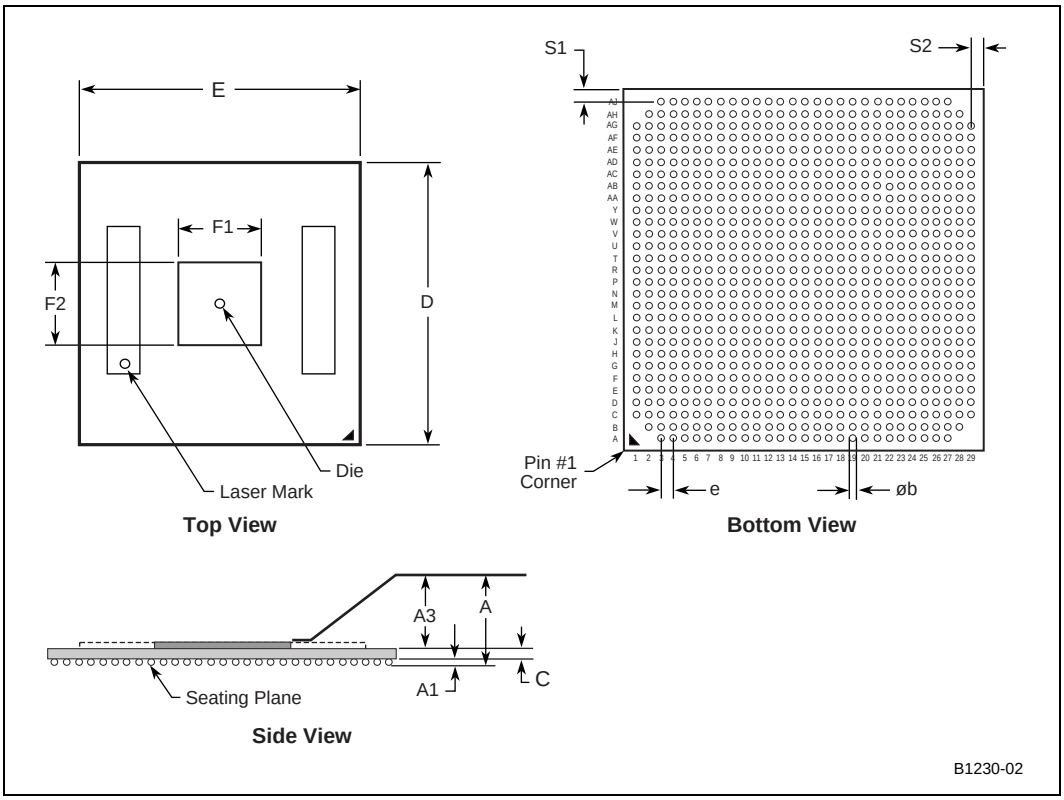


Table 18. FC-style, H-PBGA Package Dimensions

829-Pin BGA		
Symbol	**Minimum**	**Maximum**
A	2.392	2.942
A1	0.50	0.70
A3	0.742	0.872
b	0.61 Ref.	
C	1.15	1.37
D	37.45	37.55
E	37.45	37.55
F1	9.88 Ref.	
F2	10.16 Ref.	
e	1.27 Ref.	
S1	0.97 Ref.	
S2	0.97 Ref.	

Measurement in millimeters.

Figure 3. Intel® 80333 I/O Processor Signal Group Locations (Bottom View)

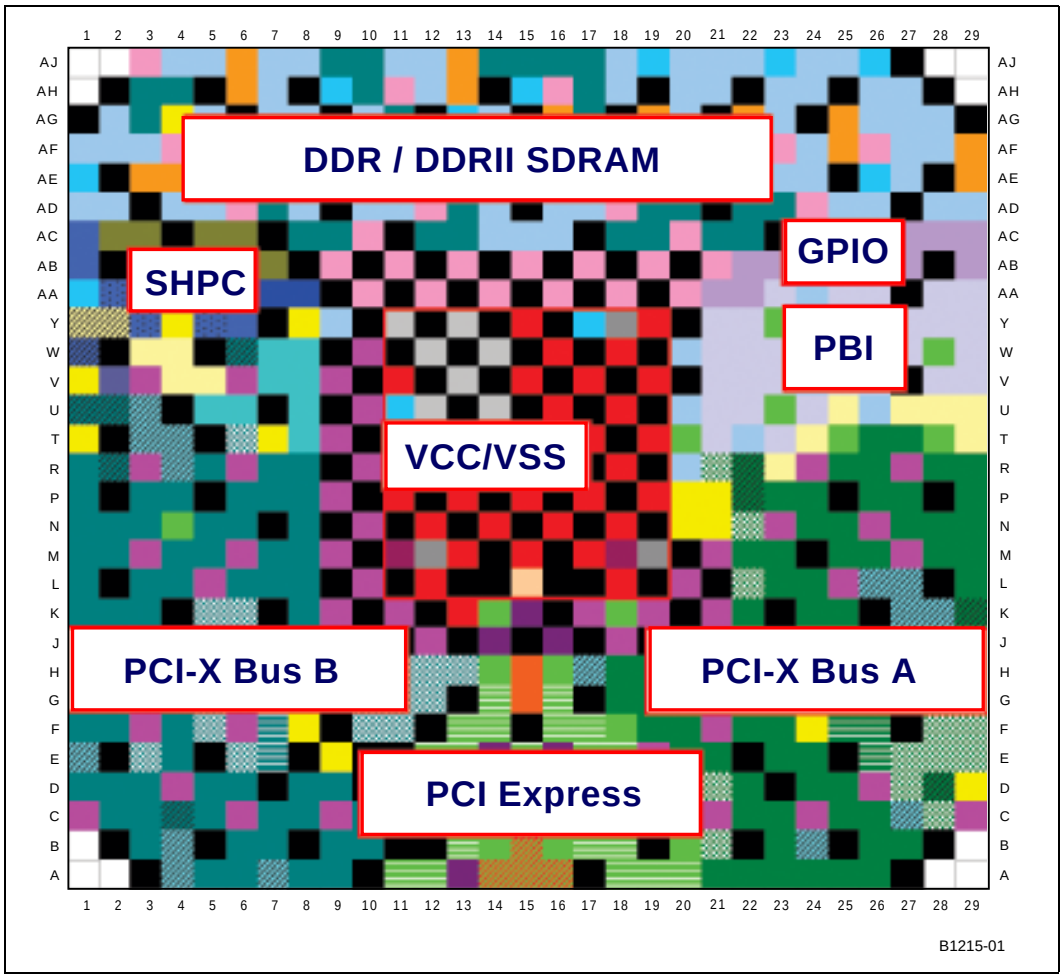
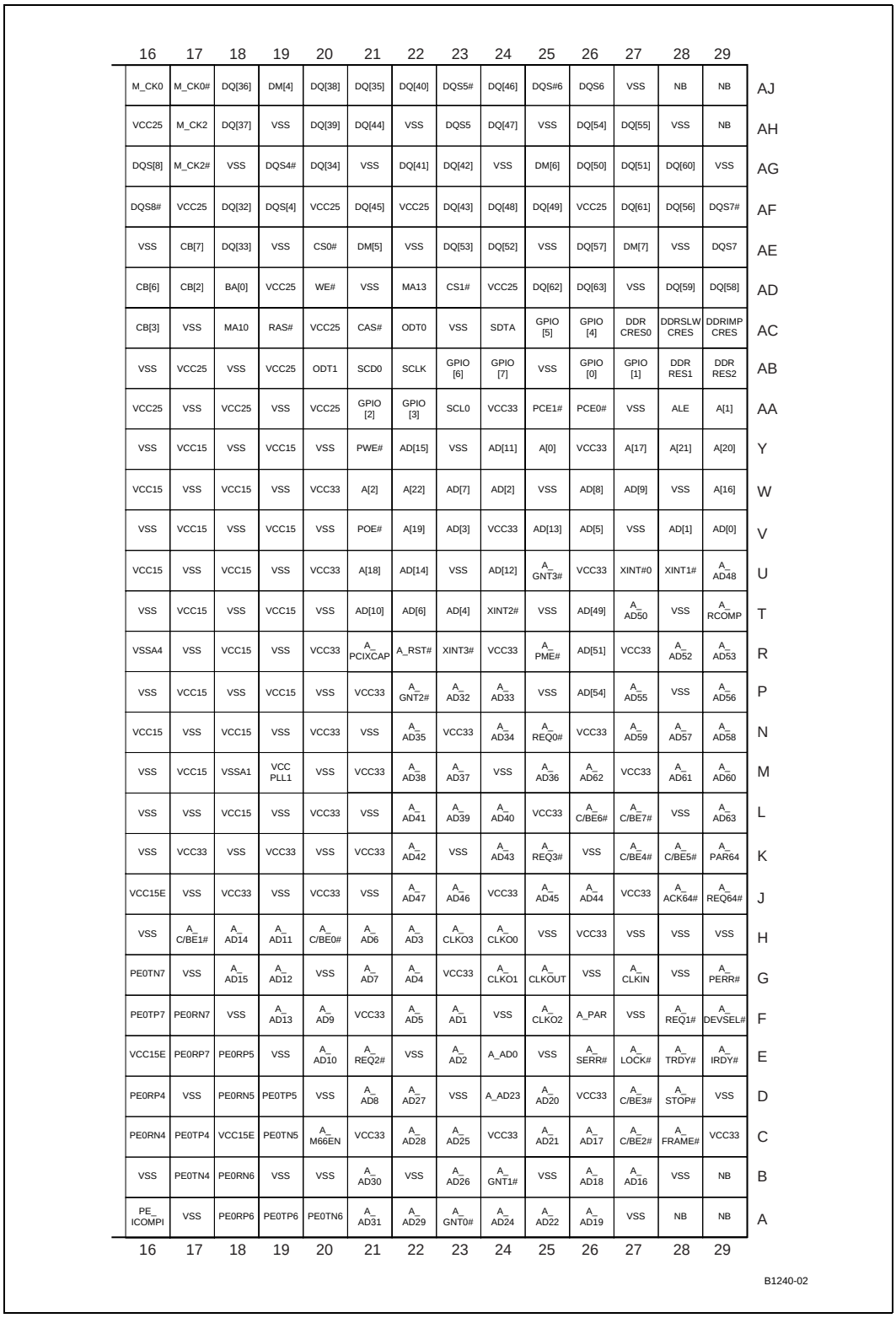


Figure 4. Intel® 80333 I/O Processor Ballout — Left Side (Bottom View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
AJ	NB	NB	VCC25	DQS1#	DQS[1]	DQ[15]	DQ[10]	DQ[17]	DM[2]	MA8	DQ[28]	DQ[25]	DM[3]	M_CK1	M_CK1#
AH	NB	VSS	M_RST#	CKE1	VSS	DQ[14]	DQ[20]	VSS	MA6	MA5	VCC25	DQ[24]	DQS3#	VSS	DM[8]
AG	VSS	DQ[3]	VSS	CKE0	DM[1]	VSS	DQ[11]	DQ[16]	VSS	DQ[18]	MA4	VSS	DQS3	DQ[31]	VSS
AF	DQ[6]	DQ[7]	DQ[2]	VCC25	MA12	DQ[9]	VSS	DQ[21]	DQS2	VCC25	MA3	DQ[29]	VCC25	DQ[30]	CB[1]
AE	DM[0]	VSS	DQS0#	DQS[0]	VSS	DQ[13]	DQ[8]	VSS	DQS2#	DQ[23]	VSS	MA1	DQ[26]	VSS	CB[0]
AD	DQ[5]	DQ[4]	VSS	DQ[1]	DQ[0]	VCC25	MA7	DQ[12]	VSS	DQ[22]	DQ[19]	VCC25	BA1	DQ[27]	VSS
AC	DDR_VREF	VSS	VSS	VSS	VSS	VSS	VSS	MA11	MA9	VCC25	VSS	MA2	MA0	CB[5]	CB[4]
AB	N/C6	VSS	TDO	TMS	VSS	RSTIN#	VCC25	VSS	VCC25	VSS	VCC25	VSS	VCC25	VSS	VCC25
AA	B_H BUTTON #	N/C4	VSS	N/C5	TRST#	VSS	PWRGD	HPI#	VSS	VCC25	VSS	VCC25	VSS	VCC25	VSS
Y	VCC15	TCK	VSS	VSS	N/C0	TDI	VSS	N/C3	VCC13	VSS	VCC13	VSS	VCC13	VSS	VCC15
W	PWR DELAY	VSS	XINT4#	B_ PCIXCAP	VCC33	B_H RESET#	B_ HPWREN	B_H PRSNT2#	VSS	VCC13	VSS	VCC13	VSS	VCC15	VSS
V	B_ RCOMP	XINT7#	VCC33	XINT6#	XINT5#	VSS	B_HP WRLED#	B_RST#	VCC15	VSS	VCC15	VSS	VCC13	VSS	VCC15
U	B_ C/BE4#	B_ C/BE5#	B_ C/BE7#	VSS	B_H PRSNT1#	B_HATN LED#	VCC33	B_HP WRFLT#	VSS	VCC15	VSS	VCC13	VSS	VCC15	VSS
T	N/C2	VSS	B_ C/BE6#	B_ GNT1#	VSS	B_ GNT0#	VSS	B_ HMRL#	VCC15	VSS	VCC15	VSS	VCC15	VSS	VCC15
R	B_ AD63	B_ PAR64	VCC33	B_ REQ0#	B_ AD45	VCC33	B_ AD46	B_ AD47	VSS	VCC15	VSS	VCC15	VSS	VCC15	VCC PLL4
P	B_ AD60	VSS	B_ AD61	B_ AD62	VSS	B_ AD44	B_ AD43	B_ AD42	VCC15	VSS	VCC15	VSS	VCC PLL5	VSSA5	VCC15
N	B_ AD59	B_ AD58	B_ AD57	VSS	B_ AD41	B_ AD40	VSS	B_ AD39	VSS	VCC15	VSS	VCC15	VSS	VCC15	VSS
M	B_ AD56	B_ AD55	VCC33	B_ AD54	B_ AD38	VCC33	B_ AD37	B_ AD36	VCC15	VSS	VCC PLL2	VSSA2	VCC15	VSS	VCC15
L	B_ AD53	VSS	B_ AD52	B_ AD51	VCC33	B_ AD35	B_ AD34	B_ AD33	VSS	VCC15	VSS	VCC15	VSS	VSS	VCC PLL3
K	B_ AD50	B_ REQ4#	B_ REQ3#	VSS	B_ REQ1#	N/C7	VSS	B_ AD32	VCC15	VCC15	VCC15	VSS	VCC15	VSS	VSSA3
J	B_ AD49	B_ AD48	VCC33	B_ PERR#	B_ SERR#	VSS	B_ LOCK#	B_ CLKO1	VSS	VCC15	VSS	VCC15	VSS	VCC15E	VSS
H	B_ AD0	VSS	B_ AD1	B_ AD2	VCC33	B_ ACK64#	B_ CLKO4	B_ CLKO[2]	B_ CLKO3	B_ TRDY#	B_ GNT2#	B_ GNT4#	B_PME#	VSS	REF_ CLKP
G	B_ AD3	B_ AD4	B_ AD5	VSS	DEV SEL#	B_ STOP#	VSS	VSS	B_ CLKIN	VCC33	B_ REQ64#	B_ REQ2#	VSS	PE0RP0	REF CLKN
F	B_ AD6	B_ AD7	VCC33	B_ AD8	B_ IRDY#	VCC33	B_ CLKO0	VSS	VSS	VSS	B_ GNT3#	VSS	PE0TP0	PE0RN0	VSS
E	B_ C/BE0#	VSS	B_ M66EN	B_ AD9	VSS	B_ FRAME#	B_ CLKOUT	VSS	VCC33	VSS	VSS	PE0RP1	PE0TN0	VCC15E	PE0TP3
D	B_ AD10	B_ AD11	B_ AD12	VCC33	B_ C/BE2#	B_ AD19	VSS	B_ AD24	B_ AD27	VSS	PE0TN2	PE0RN1	VSS	PE0RP3	PE0TN3
C	VCC33	B_ AD13	B_ AD14	B_ PAR	B_ AD17	VCC33	B_ AD22	B_ AD25	VSS33	B_ AD30	PE0TP2	PE0TP1	VCC15E	PE0RN3	VSS
B	NB	VSS	B_ AD15	B_ CBE#1	VSS	B_ AD20	B_ AD23	VSS	B_ AD28	B_ AD31	VSS	PE0TN1	VSS	VSS	PE_ RCOMPO
A	NB	NB	VSS	B_ AD16	B_ AD18	B_ AD21	B_ C/BE3#	B_ AD26	B_ AD29	VSS	PE0RP2	PE0RN2	VCC15E	PE_ VSSBG	PE_ VCCBG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

B1239-03

Figure 5. Intel® 80333 I/O Processor Ballout — Right Side (Bottom View)



16	17	18	19	20	21	22	23	24	25	26	27	28	29	
M_CK0	M_CK0#	DQ[36]	DM[4]	DQ[38]	DQ[35]	DQ[40]	DQS5#	DQ[46]	DQS#6	DQS6	VSS	NB	NB	AJ
VCC25	M_CK2	DQ[37]	VSS	DQ[39]	DQ[44]	VSS	DQS5	DQ[47]	VSS	DQ[54]	DQ[55]	VSS	NB	AH
DQS[8]	M_CK2#	VSS	DQS4#	DQ[34]	VSS	DQ[41]	DQ[42]	VSS	DM[6]	DQ[50]	DQ[51]	DQ[60]	VSS	AG
DQS8#	VCC25	DQ[32]	DQS[4]	VCC25	DQ[45]	VCC25	DQ[43]	DQ[48]	DQ[49]	VCC25	DQ[61]	DQ[56]	DQS7#	AF
VSS	CB[7]	DQ[33]	VSS	CS0#	DM[5]	VSS	DQ[53]	DQ[52]	VSS	DQ[57]	DM[7]	VSS	DQS7	AE
CB[6]	CB[2]	BA[0]	VCC25	WE#	VSS	MA13	CS1#	VCC25	DQ[62]	DQ[63]	VSS	DQ[59]	DQ[58]	AD
CB[3]	VSS	MA10	RAS#	VCC25	CAS#	ODT0	VSS	SDTA	GPIO [5]	GPIO [4]	DDR CRES0	DDRSLW CRES	DDRIMP CRES	AC
VSS	VCC25	VSS	VCC25	ODT1	SCD0	SCLK	GPIO [6]	GPIO [7]	VSS	GPIO [0]	GPIO [1]	DDR RES1	DDR RES2	AB
VCC25	VSS	VCC25	VSS	VCC25	GPIO [2]	GPIO [3]	SCL0	VCC33	PCE1#	PCE0#	VSS	ALE	A[1]	AA
VSS	VCC15	VSS	VCC15	VSS	PWE#	AD[15]	VSS	AD[11]	A[0]	VCC33	A[17]	A[21]	A[20]	Y
VCC15	VSS	VCC15	VSS	VCC33	A[2]	A[22]	AD[7]	AD[2]	VSS	AD[8]	AD[9]	VSS	A[16]	W
VSS	VCC15	VSS	VCC15	VSS	POE#	A[19]	AD[3]	VCC33	AD[13]	AD[5]	VSS	AD[1]	AD[0]	V
VCC15	VSS	VCC15	VSS	VCC33	A[18]	AD[14]	VSS	AD[12]	A_ GNT3#	VCC33	XINT#0	XINT1#	A_ AD48	U
VSS	VCC15	VSS	VCC15	VSS	AD[10]	AD[6]	AD[4]	XINT2#	VSS	AD[49]	A_ AD50	VSS	A_ RCOMP	T
VSSA4	VSS	VCC15	VSS	VCC33	A_ PCIXCAP	A_RST#	XINT3#	VCC33	A_ PME#	AD[51]	VCC33	A_ AD52	A_ AD53	R
VSS	VCC15	VSS	VCC15	VSS	VCC33	A_ GNT2#	A_ AD32	A_ AD33	VSS	AD[54]	A_ AD55	VSS	A_ AD56	P
VCC15	VSS	VCC15	VSS	VCC33	VSS	A_ AD35	VCC33	A_ AD34	A_ REQ0#	VCC33	A_ AD59	A_ AD57	A_ AD58	N
VSS	VCC15	VSSA1	VCC PLL1	VSS	VCC33	A_ AD38	A_ AD37	VSS	A_ AD36	A_ AD62	VCC33	A_ AD61	A_ AD60	M
VSS	VSS	VCC15	VSS	VCC33	VSS	A_ AD41	A_ AD39	A_ AD40	VCC33	A_ C/BE6#	A_ C/BE7#	VSS	A_ AD63	L
VSS	VCC33	VSS	VCC33	VSS	VCC33	A_ AD42	VSS	A_ AD43	A_ REQ3#	VSS	A_ C/BE4#	A_ C/BE5#	A_ PAR64	K
VCC15E	VSS	VCC33	VSS	VCC33	VSS	A_ AD47	A_ AD46	VCC33	A_ AD45	A_ AD44	VCC33	A_ ACK64#	A_ REQ64#	J
VSS	A_ C/BE1#	A_ AD14	A_ AD11	A_ C/BE0#	A_ AD6	A_ AD3	A_ CLKO3	A_ CLKO0	VSS	VCC33	VSS	VSS	VSS	H
PE0TN7	VSS	A_ AD15	A_ AD12	VSS	A_ AD7	A_ AD4	VCC33	A_ CLKO1	A_ CLKOUT	VSS	A_ CLKIN	VSS	A_ PERR#	G
PE0TP7	PE0RN7	VSS	A_ AD13	A_ AD9	VCC33	A_ AD5	A_ AD1	VSS	A_ CLKO2	A_PAR	VSS	A_ REQ1#	A_ DEVSEL#	F
VCC15E	PE0RP7	PE0RP5	VSS	A_ AD10	A_ REQ2#	VSS	A_ AD2	A_AD0	VSS	A_ SERR#	A_ LOCK#	A_ TRDY#	A_ IRDY#	E
PE0RP4	VSS	PE0RN5	PE0TP5	VSS	A_ AD8	A_ AD27	VSS	A_AD23	A_ AD20	VCC33	A_ C/BE3#	A_ STOP#	VSS	D
PE0RN4	PE0TP4	VCC15E	PE0TN5	A_ M66EN	VCC33	A_ AD28	A_ AD25	VCC33	A_ AD21	A_ AD17	A_ C/BE2#	A_ FRAME#	VCC33	C
VSS	PE0TN4	PE0RN6	VSS	VSS	A_ AD30	VSS	A_ AD26	A_ GNT1#	VSS	A_ AD18	A_ AD16	VSS	NB	B
PE_ ICOMPI	VSS	PE0RP6	PE0TP6	PE0TN6	A_ AD31	A_ AD29	A_ GNT0#	A_ AD24	A_ AD22	A_ AD19	VSS	NB	NB	A
16	17	18	19	20	21	22	23	24	25	26	27	28	29	

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Table 19. 829-Lead Package — Alphabetical Ball Listings (Sheet 1 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
A1	--	B13	VSS	C25	A_AD21
A2	--	B14	VSS	C26	A_AD17
A3	VSS	B15	PE_RCOMPO	C27	A_C/BE2#
A4	B_AD16	B16	VSS	C28	A_FRAME#
A5	B_AD18	B17	PE0TN4	C29	VCC33
A6	B_AD21	B18	PE0RN6	D1	B_AD10
A7	B_C/BE3#	B19	VSS	D2	B_AD11
A8	B_AD26	B20	VSS	D3	B_AD12
A9	B_AD29	B21	A_AD30	D4	VCC33
A10	VSS	B22	VSS	D5	B_C/BE2#
A11	PE0RP2	B23	A_AD26	D6	B_AD19
A12	PE0RN2	B24	A_GNT1#	D7	VSS
A13	VCC15E	B25	VSS	D8	B_AD24
A14	PE_VSSBG	B26	A_AD18	D9	B_AD27
A15	PE_VCCBG	B27	A_AD16	D10	VSS
A16	PE_ICOMPI	B28	VSS	D11	PE0TN2
A17	VSS	B29	--	D12	PE0RN1
A18	PE0RP6	C1	VCC33	D13	VSS
A19	PE0TP6	C2	B_AD13	D14	PE0RP3
A20	PE0TN6	C3	B_AD14	D15	PE0TN3
A21	A_AD31	C4	B_PAR	D16	PE0RP4
A22	A_AD29	C5	B_AD17	D17	VSS
A23	A_GNT0#	C6	VCC33	D18	PE0RN5
A24	A_AD24	C7	B_AD22	D19	PE0TP5
A25	A_AD22	C8	B_AD25	D20	VSS
A26	A_AD19	C9	VCC33	D21	A_AD8
A27	VSS	C10	B_AD30	D22	A_AD27
A28	--	C11	PE0TP2	D23	VSS
A29	--	C12	PE0TP1	D24	A_AD23
B1	--	C13	VCC15E	D25	A_AD20
B2	VSS	C14	PE0RN3	D26	VCC33
B3	B_AD15	C15	VSS	D27	A_C/BE3#
B4	B_C/BE1#	C16	PE0RN4	D28	A_STOP#
B5	VSS	C17	PE0TP4	D29	VSS
B6	B_AD20	C18	VCC15E	E1	B_C/BE0#
B7	B_AD23	C19	PE0TN5	E2	VSS
B8	VSS	C20	A_M66EN	E3	B_M66EN
B9	B_AD28	C21	VCC33	E4	B_AD9
B10	B_AD31	C22	A_AD28	E5	VSS
B11	VSS	C23	A_AD25	E6	B_FRAME#
B12	PE0TN1	C24	VCC33	E7	B_CLKOUT

Table 19. 829-Lead Package — Alphabetical Ball Listings (Sheet 2 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
E8	VSS	F20	A_AD9	H3	B_AD1
E9	VCC33	F21	VCC33	H4	B_AD2
E10	VSS	F22	A_AD5	H5	VCC33
E11	VSS	F23	A_AD1	H6	B_ACK64#
E12	PE0RP1	F24	VSS	H7	B_CLKO4
E13	PE0TN0	F25	A_CLKO2	H8	B_CLKO2
E14	VCC15E	F26	A_PAR	H9	B_CLKO3
E15	PE0TP3	F27	VSS	H10	B_TRDY#
E16	VCC15E	F28	A_REQ1#	H11	B_GNT2#
E17	PE0RP7	F29	A_DEVSEL#	H12	B_GNT4#
E18	PE0RP5	G1	B_AD3	H13	B_PME#
E19	VSS	G2	B_AD4	H14	VSS
E20	A_AD10	G3	B_AD5	H15	REFCLK+
E21	A_REQ2#	G4	VSS	H16	VSS
E22	VSS	G5	B_DEVSEL#	H17	A_C/BE1#
E23	A_AD2	G6	B_STOP#	H18	A_AD14
E24	A_AD0	G7	VSS	H19	A_AD11
E25	VSS	G8	VSS	H20	A_C/BE0#
E26	A_SERR#	G9	B_CLKIN	H21	A_AD6
E27	A_LOCK#	G10	VCC33	H22	A_AD3
E28	A_TRDY#	G11	B_REQ64#	H23	A_CLKO3
E29	A_IRDY#	G12	B_REQ2#	H24	A_CLKO0
F1	B_AD6	G13	VSS	H25	VSS
F2	B_AD7	G14	PE0RP0	H26	VCC33
F3	VCC33	G15	REFCLK-	H27	VSS
F4	B_AD8	G16	PE0TN7	H28	VSS
F5	B_IRDY#	G17	VSS	H29	VSS
F6	VCC33	G18	A_AD15	J1	B_AD49
F7	B_CLKO0	G19	A_AD12	J2	B_AD48
F8	VSS	G20	VSS	J3	VCC33
F9	VSS	G21	A_AD7	J4	B_PERR#
F10	VSS	G22	A_AD4	J5	B_SERR#
F11	B_GNT3#	G23	VCC33	J6	VSS
F12	VSS	G24	A_CLKO1	J7	B_LOCK#
F13	PE0TP0	G25	A_CLKOUT	J8	B_CLKO1
F14	PE0RN0	G26	VSS	J9	VSS
F15	VSS	G27	A_CLKIN	J10	VCC15
F16	PE0TP7	G28	VSS	J11	VSS
F17	PE0RN7	G29	A_PERR#	J12	VCC15
F18	VSS	H1	B_AD0	J13	VSS
F19	A_AD13	H2	VSS	J14	VCC15E

Table 19. 829-Lead Package — Alphabetical Ball Listings (Sheet 3 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
J15	VSS	K27	A_C/BE4#	M10	VSS
J16	VCC15E	K28	A_C/BE5#	M11	VCCPLL2
J17	VSS	K29	A_PAR64	M12	VSSA2
J18	VCC33	L1	B_AD53	M13	VCC15
J19	VSS	L2	VSS	M14	VSS
J20	VCC33	L3	B_AD52	M15	VCC15
J21	VSS	L4	B_AD51	M16	VSS
J22	A_AD47	L5	VCC33	M17	VCC15
J23	A_AD46	L6	B_AD35	M18	VSSA1
J24	VCC33	L7	B_AD34	M19	VCCPLL1
J25	A_AD45	L8	B_AD33	M20	VSS
J26	A_AD44	L9	VSS	M21	VCC33
J27	VCC33	L10	VCC15	M22	A_AD38
J28	A_ACK64#	L11	VSS	M23	A_AD37
J29	A_REQ64#	L12	VCC15	M24	VSS
K1	B_AD50	L13	VSS	M25	A_AD36
K2	B_REQ4#	L14	VSS	M26	A_AD62
K3	B_REQ3#	L15	VCCPLL3	M27	VCC33
K4	VSS	L16	VSS	M28	A_AD61
K5	B_REQ1#	L17	VSS	M29	A_AD60
K6	N/C7	L18	VCC15	N1	B_AD59
K7	VSS	L19	VSS	N2	B_AD58
K8	B_AD32	L20	VCC33	N3	B_AD57
K9	VCC15	L21	VSS	N4	VSS
K10	VCC15	L22	A_AD41	N5	B_AD41
K11	VCC15	L23	A_AD39	N6	B_AD40
K12	VSS	L24	A_AD40	N7	VSS
K13	VCC15	L25	VCC33	N8	B_AD39
K14	VSS	L26	A_C/BE6#	N9	VSS
K15	VSSA3	L27	A_C/BE7#	N10	VCC15
K16	VSS	L28	VSS	N11	VSS
K17	VCC33	L29	A_AD63	N12	VCC15
K18	VSS	M1	B_AD56	N13	VSS
K19	VCC33	M2	B_AD55	N14	VCC15
K20	VSS	M3	VCC33	N15	VSS
K21	VCC33	M4	B_AD54	N16	VCC15
K22	A_AD42	M5	B_AD38	N17	VSS
K23	VSS	M6	VCC33	N18	VCC15
K24	A_AD43	M7	B_AD37	N19	VSS
K25	A_REQ3#	M8	B_AD36	N20	VCC33
K26	VSS	M9	VCC15	N21	VSS

Table 19. 829-Lead Package — Alphabetical Ball Listings (Sheet 4 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
N22	A_AD35	R5	B_AD45	T17	VCC15
N23	VCC33	R6	VCC33	T18	VSS
N24	A_AD34	R7	B_AD46	T19	VCC15
N25	A_REQ0#	R8	B_AD47	T20	VSS
N26	VCC33	R9	VSS	T21	AD10
N27	A_AD59	R10	VCC15	T22	AD6
N28	A_AD57	R11	VSS	T23	AD4
N29	A_AD58	R12	VCC15	T24	XINT2#
P1	B_AD60	R13	VSS	T25	VSS
P2	VSS	R14	VCC15	T26	A_AD49
P3	B_AD61	R15	VCCPLL4	T27	A_AD50
P4	B_AD62	R16	VSSA4	T28	VSS
P5	VSS	R17	VSS	T29	A_RCOMP
P6	B_AD44	R18	VCC15	U1	B_C/BE4#
P7	B_AD43	R19	VSS	U2	B_C/BE5#
P8	B_AD42	R20	VCC33	U3	B_C/BE7#
P9	VCC15	R21	A_PCIXCAP	U4	VSS
P10	VSS	R22	A_RST#	U5	B_HPRSNT1#
P11	VCC15	R23	XINT3#	U6	B_HATNLED#
P12	VSS	R24	VCC33	U7	VCC33
P13	VCCPLL5	R25	A_PME#	U8	B_HPWRFLT#
P14	VSSA5	R26	A_AD51	U9	VSS
P15	VCC15	R27	VCC33	U10	VCC15
P16	VSS	R28	A_AD52	U11	VSS
P17	VCC15	R29	A_AD53	U12	VCC13
P18	VSS	T1	N/C2	U13	VSS
P19	VCC15	T2	VSS	U14	VCC15
P20	VSS	T3	B_C/BE6#	U15	VSS
P21	VCC33	T4	B_GNT1#	U16	VCC15
P22	A_GNT2#	T5	VSS	U17	VSS
P23	A_AD32	T6	B_GNT0#	U18	VCC15
P24	A_AD33	T7	VSS	U19	VSS
P25	VSS	T8	B_HMRL#	U20	VCC33
P26	A_AD54	T9	VCC15	U21	A18
P27	A_AD55	T10	VSS	U22	AD14
P28	VSS	T11	VCC15	U23	VSS
P29	A_AD56	T12	VSS	U24	AD12
R1	B_AD63	T13	VCC15	U25	A_GNT3#
R2	B_PAR64	T14	VSS	U26	VCC33
R3	VCC33	T15	VCC15	U27	XINT0#
R4	B_REQ0#	T16	VSS	U28	XINT1#

Table 19. 829-Lead Package — Alphabetical Ball Listings (Sheet 5 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
U29	A_AD48	W12	VCC13	Y24	AD11
V1	B_RCOMP	W13	VSS	Y25	A0
V2	XINT7#	W14	VCC15	Y26	VCC33
V3	VCC33	W15	VSS	Y27	A17
V4	XINT6#	W16	VCC15	Y28	A21
V5	XINT5#	W17	VSS	Y29	A20
V6	VSS	W18	VCC15	AA1	B_HBUTTON#
V7	B_HPWRLED#	W19	VSS	AA2	N/C4
V8	B_RST#	W20	VCC33	AA3	VSS
V9	VCC15	W21	A2	AA4	N/C5
V10	VSS	W22	A22	AA5	TRST#
V11	VCC15	W23	AD7	AA6	VSS
V12	VSS	W24	AD2	AA7	PWRGD
V13	VCC13	W25	VSS	AA8	HPI#
V14	VSS	W26	AD8	AA9	VSS
V15	VCC15	W27	AD9	AA10	VCC25
V16	VSS	W28	VSS	AA11	VSS
V17	VCC15	W29	A16	AA12	VCC25
V18	VSS	Y1	VCC15	AA13	VSS
V19	VCC15	Y2	TCK	AA14	VCC25
V20	VSS	Y3	VSS	AA15	VSS
V21	POE#	Y4	VSS	AA16	VCC25
V22	A19	Y5	N/C0	AA17	VSS
V23	AD3	Y6	TDI	AA18	VCC25
V24	VCC33	Y7	VSS	AA19	VSS
V25	AD13	Y8	N/C3	AA20	VCC25
V26	AD5	Y9	VCC13	AA21	GPIO2/U0_CTS#
V27	VSS	Y10	VSS	AA22	GPIO3/U0_RTS#
V28	AD1	Y11	VCC13	AA23	SCL0
V29	AD0	Y12	VSS	AA24	VCC33
W1	PWRDELAY	Y13	VCC13	AA25	PCE1#
W2	VSS	Y14	VSS	AA26	PCE0#
W3	XINT4#	Y15	VCC15	AA27	VSS
W4	B_PCIXCAP	Y16	VSS	AA28	ALE
W5	VCC33	Y17	VCC15	AA29	A1
W6	B_HRESET#	Y18	VSS	AB1	N/C6
W7	B_HPWREN	Y19	VCC15	AB2	VSS
W8	B_HPRSNT2#	Y20	VSS	AB3	TDO
W9	VSS	Y21	PWE#	AB4	TMS
W10	VCC13	Y22	AD15	AB5	VSS
W11	VSS	Y23	VSS	AB6	RSTIN#

Table 19. 829-Lead Package — Alphabetical Ball Listings (Sheet 6 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
AB7	VCC25	AC19	RAS#	AE2	VSS
AB8	VSS	AC20	VCC25	AE3	DQS0#
AB9	VCC25	AC21	CAS#	AE4	DQS0
AB10	VSS	AC22	ODT0	AE5	VSS
AB11	VCC25	AC23	VSS	AE6	DQ13
AB12	VSS	AC24	SDTA/SCD1	AE7	DQ8
AB13	VCC25	AC25	GPIO5/U1_TXD	AE8	VSS
AB14	VSS	AC26	GPIO4/U1_RXD	AE9	DQS2#
AB15	VCC25	AC27	DDRCRES0	AE10	DQ23
AB16	VSS	AC28	DDRSLWCRES	AE11	VSS
AB17	VCC25	AC29	DDRIMPCRES	AE12	MA1
AB18	VSS	AD1	DQ5	AE13	DQ26
AB19	VCC25	AD2	DQ4	AE14	VSS
AB20	ODT1	AD3	VSS	AE15	CB0
AB21	SCD0	AD4	DQ1	AE16	VSS
AB22	SCLK/SCL1	AD5	DQ0	AE17	CB7
AB23	GPIO6/U1_CTS#	AD6	VCC25	AE18	DQ33
AB24	GPIO7/U1_RTS#	AD7	MA7	AE19	VSS
AB25	VSS	AD8	DQ12	AE20	CS0#
AB26	GPIO0/U0_RXD	AD9	VSS	AE21	DM5
AB27	GPIO1/U0_TXD	AD10	DQ22	AE22	VSS
AB28	DDRRES1	AD11	DQ19	AE23	DQ53
AB29	DDRRES2	AD12	VCC25	AE24	DQ52
AC1	DDR_VREF	AD13	BA1	AE25	VSS
AC2	VSS	AD14	DQ27	AE26	DQ57
AC3	VSS	AD15	VSS	AE27	DM7
AC4	VSS	AD16	CB6	AE28	VSS
AC5	VSS	AD17	CB2	AE29	DQS7
AC6	VSS	AD18	BA0	AF1	DQ6
AC7	VSS	AD19	VCC25	AF2	DQ7
AC8	MA11	AD20	WE#	AF3	DQ2
AC9	MA9	AD21	VSS	AF4	VCC25
AC10	VCC25	AD22	MA13	AF5	MA12
AC11	VSS	AD23	CS1#	AF6	DQ9
AC12	MA2	AD24	VCC25	AF7	VSS
AC13	MA0	AD25	DQ62	AF8	DQ21
AC14	CB5	AD26	DQ63	AF9	DQS2
AC15	CB4	AD27	VSS	AF10	VCC25
AC16	CB3	AD28	DQ59	AF11	MA3
AC17	VSS	AD29	DQ58	AF12	DQ29
AC18	MA10	AE1	DM0	AF13	VCC25

Table 19. 829-Lead Package — Alphabetical Ball Listings (Sheet 7 of 7)

Ball	Signal	Ball	Signal	Ball	Signal
AF14	DQ30	AG26	DQ50	AJ9	DM2
AF15	CB1	AG27	DQ51	AJ10	MA8
AF16	DQS_8#	AG28	DQ60	AJ11	DQ28
AF17	VCC25	AG29	VSS	AJ12	DQ25
AF18	DQ32	AH1	--	AJ13	DM3
AF19	DQS4	AH2	VSS	AJ14	M_CK1
AF20	VCC25	AH3	M_RST#	AJ15	M_CK1#
AF21	DQ45	AH4	CKE1	AJ16	M_CK0
AF22	VCC25	AH5	VSS	AJ17	M_CK0#
AF23	DQ43	AH6	DQ14	AJ18	DQ36
AF24	DQ48	AH7	DQ20	AJ19	DM4
AF25	DQ49	AH8	VSS	AJ20	DQ38
AF26	VCC25	AH9	MA6	AJ21	DQ35
AF27	DQ61	AH10	MA5	AJ22	DQ40
AF28	DQ56	AH11	VCC25	AJ23	DQS5#
AF29	DQS7#	AH12	DQ24	AJ24	DQ46
AG1	VSS	AH13	DQS3#	AJ25	DQS6#
AG2	DQ3	AH14	VSS	AJ26	DQS6
AG3	VSS	AH15	DM8	AJ27	VSS
AG4	CKE0	AH16	VCC25	AJ28	--
AG5	DM1	AH17	M_CK2	AJ29	--
AG6	VSS	AH18	DQ37		
AG7	DQ11	AH19	VSS		
AG8	DQ16	AH20	DQ39		
AG9	VSS	AH21	DQ44		
AG10	DQ18	AH22	VSS		
AG11	MA4	AH23	DQS5		
AG12	VSS	AH24	DQ47		
AG13	DQS3	AH25	VSS		
AG14	DQ31	AH26	DQ54		
AG15	VSS	AH27	DQ55		
AG16	DQS8	AH28	VSS		
AG17	M_CK2#	AH29	--		
AG18	VSS	AJ1	--		
AG19	DQS4#	AJ2	--		
AG20	DQ34	AJ3	VCC25		
AG21	VSS	AJ4	DQS1#		
AG22	DQ41	AJ5	DQS1		
AG23	DQ42	AJ6	DQ15		
AG24	VSS	AJ7	DQ10		
AG25	DM6	AJ8	DQ17		

Table 20. 829-Lead Package — Alphabetical Signal Listings (Sheet 1 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
--	A1	A_AD28	C22	A_C/BE5#	K28
--	A2	A_AD29	A22	A_C/BE6#	L26
--	A28	A_AD30	B21	A_C/BE7#	L27
--	A29	A_AD31	A21	A_CLKIN	G27
--	AH1	A_AD32	P23	A_CLKO0	H24
--	AH29	A_AD33	P24	A_CLKO1	G24
--	AJ1	A_AD34	N24	A_CLKO2	F25
--	AJ2	A_AD35	N22	A_CLKO3	H23
--	AJ28	A_AD36	M25	A_CLKOUT	G25
--	AJ29	A_AD37	M23	A_DEVSEL#	F29
--	B1	A_AD38	M22	A_FRAME#	C28
--	B29	A_AD39	L23	A_GNT0#	A23
A_ACK64#	J28	A_AD40	L24	A_GNT1#	B24
A_AD0	E24	A_AD41	L22	A_GNT2#	P22
A_AD1	F23	A_AD42	K22	A_GNT3#	U25
A_AD2	E23	A_AD43	K24	A_IRDY#	E29
A_AD3	H22	A_AD44	J26	A_LOCK#	E27
A_AD4	G22	A_AD45	J25	A_M66EN	C20
A_AD5	F22	A_AD46	J23	A_PAR	F26
A_AD6	H21	A_AD47	J22	A_PAR64	K29
A_AD7	G21	A_AD48	U29	A_PCIXCAP	R21
A_AD8	D21	A_AD49	T26	A_PERR#	G29
A_AD9	F20	A_AD50	T27	A_PME#	R25
A_AD10	E20	A_AD51	R26	A_RCOMP	T29
A_AD11	H19	A_AD52	R28	A_REQ0#	N25
A_AD12	G19	A_AD53	R29	A_REQ1#	F28
A_AD13	F19	A_AD54	P26	A_REQ2#	E21
A_AD14	H18	A_AD55	P27	A_REQ3#	K25
A_AD15	G18	A_AD56	P29	A_REQ64#	J29
A_AD16	B27	A_AD57	N28	A_RST#	R22
A_AD17	C26	A_AD58	N29	A_SERR#	E26
A_AD18	B26	A_AD59	N27	A_STOP#	D28
A_AD19	A26	A_AD60	M29	A_TRDY#	E28
A_AD20	D25	A_AD61	M28	A0	Y25
A_AD21	C25	A_AD62	M26	A1	AA29
A_AD22	A25	A_AD63	L29	A2	W21
A_AD23	D24	A_C/BE0#	H20	A16	W29
A_AD24	A24	A_C/BE1#	H17	A17	Y27
A_AD25	C23	A_C/BE2#	C27	A18	U21
A_AD26	B23	A_C/BE3#	D27	A19	V22
A_AD27	D22	A_C/BE4#	K27	A20	Y29
A21	Y28	B_AD21	A6	B_AD62	P4
A22	W22	B_AD22	C7	B_AD63	R1

Table 20. 829-Lead Package — Alphabetical Signal Listings (Sheet 2 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
AD0	V29	B_AD23	B7	B_C/BE0#	E1
AD1	V28	B_AD24	D8	B_C/BE1#	B4
AD2	W24	B_AD25	C8	B_C/BE2#	D5
AD3	V23	B_AD26	A8	B_C/BE3#	A7
AD4	T23	B_AD27	D9	B_C/BE4#	U1
AD5	V26	B_AD28	B9	B_C/BE5#	U2
AD6	T22	B_AD29	A9	B_C/BE6#	T3
AD7	W23	B_AD30	C10	B_C/BE7#	U3
AD8	W26	B_AD31	B10	B_CLKIN	G9
AD9	W27	B_AD32	K8	B_CLKO0	F7
AD10	T21	B_AD33	L8	B_CLKO1	J8
AD11	Y24	B_AD34	L7	B_CLKO2	H8
AD12	U24	B_AD35	L6	B_CLKO3	H9
AD13	V25	B_AD36	M8	B_CLKO4	H7
AD14	U22	B_AD37	M7	B_CLKOUT	E7
AD15	Y22	B_AD38	M5	B_DEVSEL#	G5
ALE	AA28	B_AD39	N8	B_FRAME#	E6
B_ACK64#	H6	B_AD40	N6	B_GNT0#	T6
B_AD0	H1	B_AD41	N5	B_GNT1#	T4
B_AD1	H3	B_AD42	P8	B_GNT2#	H11
B_AD2	H4	B_AD43	P7	B_GNT3#	F11
B_AD3	G1	B_AD44	P6	B_GNT4#	H12
B_AD4	G2	B_AD45	R5	B_HPWRFLT#	U8
B_AD5	G3	B_AD46	R7	B_HPRSNT2#	W8
B_AD6	F1	B_AD47	R8	B_HMRL#	T8
B_AD7	F2	B_AD48	J2	B_HPWREN	W7
B_AD8	F4	B_AD49	J1	B_HPWRLED#	V7
B_AD9	E4	B_AD50	K1	B_HPRSNT1#	U5
B_AD10	D1	B_AD51	L4	B_HATNLED#	U6
B_AD11	D2	B_AD52	L3	B_HBUTTON#	AA1
B_AD12	D3	B_AD53	L1	B_IRDY#	F5
B_AD13	C2	B_AD54	M4	B_LOCK#	J7
B_AD14	C3	B_AD55	M2	B_M66EN	E3
B_AD15	B3	B_AD56	M1	B_PAR	C4
B_AD16	A4	B_AD57	N3	B_PAR64	R2
B_AD17	C5	B_AD58	N2	B_PCIXCAP	W4
B_AD18	A5	B_AD59	N1	B_PERR#	J4
B_AD19	D6	B_AD60	P1	B_PME#	H13
B_AD20	B6	B_AD61	P3	B_RCOMP	V1

Table 20. 829-Lead Package — Alphabetical Signal Listings (Sheet 3 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
B_REQ0#	R4	DQ1	AD4	DQ42	AG23
B_REQ1#	K5	DQ2	AF3	DQ43	AF23
B_REQ2#	G12	DQ3	AG2	DQ44	AH21
B_REQ3#	K3	DQ4	AD2	DQ45	AF21
B_REQ4#	K2	DQ5	AD1	DQ46	AJ24
B_REQ64#	G11	DQ6	AF1	DQ47	AH24
B_RST#	V8	DQ7	AF2	DQ48	AF24
B_SERR#	J5	DQ8	AE7	DQ49	AF25
B_STOP#	G6	DQ9	AF6	DQ50	AG26
B_TRDY#	H10	DQ10	AJ7	DQ51	AG27
BA0	AD18	DQ11	AG7	DQ52	AE24
BA1	AD13	DQ12	AD8	DQ53	AE23
CAS#	AC21	DQ13	AE6	DQ54	AH26
CB0	AE15	DQ14	AH6	DQ55	AH27
CB1	AF15	DQ15	AJ6	DQ56	AF28
CB2	AD17	DQ16	AG8	DQ57	AE26
CB3	AC16	DQ17	AJ8	DQ58	AD29
CB4	AC15	DQ18	AG10	DQ59	AD28
CB5	AC14	DQ19	AD11	DQ60	AG28
CB6	AD16	DQ20	AH7	DQ61	AF27
CB7	AE17	DQ21	AF8	DQ62	AD25
CKE0	AG4	DQ22	AD10	DQ63	AD26
CKE1	AH4	DQ23	AE10	DQS0	AE4
CS0#	AE20	DQ24	AH12	DQS0#	AE3
CS1#	AD23	DQ25	AJ12	DQS1	AJ5
DDR_VREF	AC1	DQ26	AE13	DQS2	AF9
DDRCRES0	AC27	DQ27	AD14	DQS3	AG13
DDRIMPCRES	AC29	DQ28	AJ11	DQS4	AF19
DDRRES1	AB28	DQ29	AF12	DQS5	AH23
DDRRES2	AB29	DQ30	AF14	DQS6	AJ26
DDRSLWCRES	AC28	DQ31	AG14	DQS7	AE29
DM0	AE1	DQ32	AF18	DQS8	AG16
DM1	AG5	DQ33	AE18	DQS1#	AJ4
DM2	AJ9	DQ34	AG20	DQS2#	AE9
DM3	AJ13	DQ35	AJ21	DQS3#	AH13
DM4	AJ19	DQ36	AJ18	DQS4#	AG19
DM5	AE21	DQ37	AH18	DQS5#	AJ23
DM6	AG25	DQ38	AJ20	DQS6#	AJ25
DM7	AE27	DQ39	AH20	DQS7#	AF29
DM8	AH15	DQ40	AJ22	DQS_8#	AF16
DQ0	AD5	DQ41	AG22	GPIO0/U0_RXD	AB26

Table 20. 829-Lead Package — Alphabetical Signal Listings (Sheet 4 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
GPIO1/U0_TXD	AB27	PE_ICOMPI	A16	REFCLK-	G15
GPIO2/U0_CTS#	AA21	PE_RCOMPO	B15	REFCLK+	H15
GPIO3/U0_RTS#	AA22	PE_VCCBG	A15	RSTIN#	AB6
GPIO4/U1_RXD	AC26	PE_VSSBG	A14	SCD0	AB21
GPIO5/U1_TXD	AC25	PE0RN0	F14	SCD1/SDTA	AC24
GPIO6/U1_CTS#	AB23	PE0RN1	D12	SCL0	AA23
GPIO7/U1_RTS#	AB24	PE0RN2	A12	SCL1/SCLK	AB22
HPI#	AA8	PE0RN3	C14	TCK	Y2
M_CK0	AJ16	PE0RN4	C16	TDI	Y6
M_CK1	AJ14	PE0RN5	D18	TDO	AB3
M_CK2	AH17	PE0RN6	B18	TMS	AB4
M_CK0#	AJ17	PE0RN7	F17	TRST#	AA5
M_CK1#	AJ15	PE0RP0	G14	VCC13	U12
M_CK2#	AG17	PE0RP1	E12	VCC13	V13
M_RST#	AH3	PE0RP2	A11	VCC13	W10
MA0	AC13	PE0RP3	D14	VCC13	W12
MA1	AE12	PE0RP4	D16	VCC13	Y9
MA2	AC12	PE0RP5	E18	VCC13	Y11
MA3	AF11	PE0RP6	A18	VCC13	Y13
MA4	AG11	PE0RP7	E17	VCC15E	A13
MA5	AH10	PE0TN0	E13	VCC15E	C13
MA6	AH9	PE0TN1	B12	VCC15E	C18
MA7	AD7	PE0TN2	D11	VCC15E	E14
MA8	AJ10	PE0TN3	D15	VCC15E	E16
MA9	AC9	PE0TN4	B17	VCC15E	J14
MA10	AC18	PE0TN5	C19	VCC15E	J16
MA11	AC8	PE0TN6	A20	VCC15	J10
MA12	AF5	PE0TN7	G16	VCC15	J12
MA13	AD22	PE0TP0	F13	VCC15	K9
N/C0	Y5	PE0TP1	C12	VCC15	K10
B_HRESET#	W6	PE0TP2	C11	VCC15	K11
N/C2	T1	PE0TP3	E15	VCC15	K13
N/C3	Y8	PE0TP4	C17	VCC15	L10
N/C4	AA2	PE0TP5	D19	VCC15	L12
N/C5	AA4	PE0TP6	A19	VCC15	L18
N/C6	AB1	PE0TP7	F16	VCC15	M9
N/C7	K6	POE#	V21	VCC15	M13
ODT0	AC22	PWE#	Y21	VCC15	M15
ODT1	AB20	PWRDELAY	W1	VCC15	M17
PCE0#	AA26	PWRGD	AA7	VCC15	N10
PCE1#	AA25	RAS#	AC19	VCC15	N12

Table 20. 829-Lead Package — Alphabetical Signal Listings (Sheet 5 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
VCC15	N14	VCC25	AA20	VCC33	J24
VCC15	N16	VCC25	AB11	VCC33	J27
VCC15	N18	VCC25	AB13	VCC33	K17
VCC15	P9	VCC25	AB15	VCC33	K19
VCC15	P11	VCC25	AB17	VCC33	K21
VCC15	P15	VCC25	AB19	VCC33	L5
VCC15	P17	VCC25	AC10	VCC33	L20
VCC15	P19	VCC25	AC20	VCC33	L25
VCC15	R10	VCC25	AD6	VCC33	M3
VCC15	R12	VCC25	AD12	VCC33	M6
VCC15	R14	VCC25	AD19	VCC33	M21
VCC15	R18	VCC25	AD24	VCC33	M27
VCC15	T9	VCC25	AF4	VCC33	N20
VCC15	T11	VCC25	AF10	VCC33	N23
VCC15	T13	VCC25	AF13	VCC33	N26
VCC15	T15	VCC25	AF17	VCC33	P21
VCC15	T17	VCC25	AF20	VCC33	R3
VCC15	T19	VCC25	AF22	VCC33	R6
VCC15	U10	VCC25	AF26	VCC33	R20
VCC15	U14	VCC25	AH11	VCC33	R24
VCC15	U16	VCC25	AH16	VCC33	R27
VCC15	U18	VCC25	AJ3	VCC33	U7
VCC15	V9	VCC33	C1	VCC33	U20
VCC15	V11	VCC33	C6	VCC33	U26
VCC15	V15	VCC33	C9	VCC33	V24
VCC15	V17	VCC33	C21	VCC33	V3
VCC15	V19	VCC33	C24	VCC33	W5
VCC15	W14	VCC33	C29	VCC33	W20
VCC15	W16	VCC33	D4	VCC33	Y26
VCC15	W18	VCC33	D26	VCC33	AA24
VCC15	Y1	VCC33	E9	VCCPLL1	M19
VCC15	Y15	VCC33	F3	VCCPLL2	M11
VCC15	Y17	VCC33	F6	VCCPLL3	L15
VCC15	Y19	VCC33	F21	VCCPLL4	R15
VCC25	AB7	VCC33	G10	VCCPLL5	P13
VCC25	AB9	VCC33	G23	VSS	A3
VCC25	AA10	VCC33	H5	VSS	A10
VCC25	AA12	VCC33	H26	VSS	A17
VCC25	AA14	VCC33	J3	VSS	A27
VCC25	AA16	VCC33	J18	VSS	B2
VCC25	AA18	VCC33	J20	VSS	B5

Table 20. 829-Lead Package — Alphabetical Signal Listings (Sheet 6 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
VSS	B8	VSS	G28	VSS	N7
VSS	B11	VSS	H2	VSS	N9
VSS	B13	VSS	H14	VSS	N11
VSS	B14	VSS	H16	VSS	N13
VSS	B16	VSS	H25	VSS	N15
VSS	B19	VSS	H27	VSS	N17
VSS	B20	VSS	H28	VSS	N19
VSS	B22	VSS	H29	VSS	N21
VSS	B25	VSS	J6	VSS	P2
VSS	B28	VSS	J9	VSS	P5
VSS	C15	VSS	J11	VSS	P10
VSS	D7	VSS	J13	VSS	P12
VSS	D10	VSS	J15	VSS	P16
VSS	D13	VSS	J17	VSS	P18
VSS	D17	VSS	J19	VSS	P20
VSS	D20	VSS	J21	VSS	P25
VSS	D23	VSS	K4	VSS	P28
VSS	D29	VSS	K7	VSS	R9
VSS	E2	VSS	K12	VSS	R11
VSS	E5	VSS	K14	VSS	R13
VSS	E8	VSS	K16	VSS	R17
VSS	E10	VSS	K18	VSS	R19
VSS	E11	VSS	K20	VSS	T2
VSS	E19	VSS	K23	VSS	T5
VSS	E22	VSS	K26	VSS	T7
VSS	E25	VSS	L2	VSS	T10
VSS	F8	VSS	L9	VSS	T12
VSS	F9	VSS	L11	VSS	T14
VSS	F10	VSS	L13	VSS	T16
VSS	F12	VSS	L14	VSS	T18
VSS	F15	VSS	L16	VSS	T20
VSS	F18	VSS	L17	VSS	T25
VSS	F24	VSS	L19	VSS	T28
VSS	F27	VSS	L21	VSS	U4
VSS	G4	VSS	L28	VSS	U9
VSS	G7	VSS	M10	VSS	U11
VSS	G8	VSS	M14	VSS	U13
VSS	G13	VSS	M16	VSS	U15
VSS	G17	VSS	M20	VSS	U17
VSS	G20	VSS	M24	VSS	U19
VSS	G26	VSS	N4	VSS	U23

Table 20. 829-Lead Package — Alphabetical Signal Listings (Sheet 7 of 7)

Signal	Ball	Signal	Ball	Signal	Ball
VSS	V6	VSS	AB14	VSS	AH8
VSS	V10	VSS	AB16	VSS	AH14
VSS	V12	VSS	AB18	VSS	AH19
VSS	V14	VSS	AB25	VSS	AH22
VSS	V16	VSS	AC2	VSS	AH25
VSS	V18	VSS	AC3	VSS	AH28
VSS	V20	VSS	AC4	VSS	AJ27
VSS	V27	VSS	AC5	VSSA1	M18
VSS	W2	VSS	AC6	VSSA2	M12
VSS	W9	VSS	AC7	VSSA3	K15
VSS	W11	VSS	AC11	VSSA4	R16
VSS	W13	VSS	AC17	VSSA5	P14
VSS	W15	VSS	AC23	WE#	AD20
VSS	W17	VSS	AD3	XINT0#	U27
VSS	W19	VSS	AD9	XINT1#	U28
VSS	W25	VSS	AD15	XINT2#	T24
VSS	W28	VSS	AD21	XINT3#	R23
VSS	Y3	VSS	AD27	XINT4#	W3
VSS	Y4	VSS	AE2	XINT5#	V5
VSS	Y7	VSS	AE5	XINT6#	V4
VSS	Y10	VSS	AE8	XINT7#	V2
VSS	Y12	VSS	AE11		
VSS	Y14	VSS	AE14		
VSS	Y16	VSS	AE16		
VSS	Y18	VSS	AE19		
VSS	Y20	VSS	AE22		
VSS	Y23	VSS	AE25		
VSS	AA3	VSS	AE28		
VSS	AA6	VSS	AF7		
VSS	AA9	VSS	AG1		
VSS	AA11	VSS	AG3		
VSS	AA13	VSS	AG6		
VSS	AA15	VSS	AG9		
VSS	AA17	VSS	AG12		
VSS	AA19	VSS	AG15		
VSS	AA27	VSS	AG18		
VSS	AB2	VSS	AG21		
VSS	AB5	VSS	AG24		
VSS	AB8	VSS	AG29		
VSS	AB10	VSS	AH2		
VSS	AB12	VSS	AH5		

3.2 Package Thermal Specifications

See *Intel® 80333 I/O Processor Thermal Design Guidelines Application Note* (306630).

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Table 21. Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–55° C to +125°C
Case Temperature Under Bias	0°C to +95°C
Supply Voltage V_{CC33} wrt. V_{SS}	–0.5 V to +4.1 V
Supply Voltage V_{CC25} wrt. V_{SS}	–0.5 V to +3.2 V
Supply Voltage V_{CC15} wrt. V_{SS}	–0.5 V to +2.1 V
Supply Voltage V_{CC13} wrt. V_{SS}	–0.5 V to +2.1 V
Voltage on Any Ball wrt. V_{SS}	–0.5 V to V_{CCP} + 0.5 V

NOTE: This data sheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product becomes available. The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design.

WARNING: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation beyond the Operating Conditions is not recommended and extended exposure beyond the Operating Conditions may affect device reliability.

Table 22. Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{CC33}	3.3 V PCI/PCI-X Supply Voltage	3.0	3.6	V	±10%
$V_{CC25/18}$	2.5 V/1.8V DDR/DDR-II Supply Voltage	2.3/1.7	2.7/1.9	V	±8%, 5%[1]
V_{CC15}	1.5 V IOP Core Supply Voltage	1.425	1.575	V	±5%[1]
V_{CC13}	1.35 V Intel XScale® core Supply Voltage	1.282	1.418	V	±5%
$V_{CCPLL1-5}$	PLL Supply Voltage	V_{CC15}	V_{CC15}	V	
DDR_VREF	Memory I/O Reference Voltage	0.49$V_{CC25/18}$	0.51 $V_{CC25/18}$	V	
PE_VCCBG	2.5 V PCI Express* VCC Band Gap	2.375	2.625		±5%
REFCLK	Input Clock Frequency	100 -300 ppm	100 + 300 ppm	MHz	100 MHz nominal
T_C	Case Temperature Under Bias	0	95	°C	

Notes:

1. ±3% DC; additional ±2% for AC transients. Under no circumstance may the supply voltage go past the AC min./max. window. The supply voltage window may go outside the DC min./max. window for transient events.

4.2 V_{CCPLL} Pin Requirements

The $V_{CCPLL[1-5]}$ balls for the Phase Lock Loop (PLL) circuit must each have filters, and be connected to the appropriate VSSA ball. See the *Intel® 80333 I/O Processor Design Guide* for specific recommendations.

4.3 Targeted DC Specifications

Table 23. DC Characteristics

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{IL1}	Input Low Voltage (DDR SDRAM)	-0.3	**DDR_VREF** - 0.18	V	(1, 2)
V_{IH1}	Input High Voltage (DDR SDRAM)	**DDR_VREF** + 0.18	$\mathbf{V_{CC25}}$ + 0.3	V	(1, 2)
V_{IL2}	Input Low Voltage (DDR-II SDRAM)	-0.2	**DDR_VREF** - 0.125	V	(1, 3)
V_{IH2}	Input High Voltage (DDR-II SDRAM)	**DDR_VREF** + 0.125	$\mathbf{V_{CC25}}$ + 0.2	V	(1, 3)
V_{IL2}	Input Low Voltage (Misc.)	-0.3	0.8	V	(4, 5)
V_{IH2}	Input High Voltage (Misc.)	2.0	$\mathbf{V_{CC33}}$ + 0.3	V	(4, 5)
V_{IL3}	Input Low Voltage (PCI-X)	-0.5	0.35 × $\mathbf{V_{CC33}}$	V	
V_{IH3}	Input High Voltage (PCI-X/PCI)	0.5 × $\mathbf{V_{CC33}}$	$\mathbf{V_{CC33}}$ + 0.5	V	
V_{IL5}	Input Low Voltage (PCI)	-0.5	0.3 × $\mathbf{V_{CC33}}$	V	
V_{OL2}	Output Low Voltage (Misc.)		0.4	V	$\mathbf{I_{OL}}$ = 6 mA
V_{OH2}	Output High Voltage (Misc.)	2.4		V	$\mathbf{I_{OH}}$ = -2 mA
V_{OL1}	Output Low Voltage (DDR SDRAM)		0.35	V	$\mathbf{I_{OL}}$ = 12.5 mA (1, 2)
V_{OH1}	Output High Voltage (DDR SDRAM)	1.95		V	$\mathbf{I_{OH}}$ = -12.5 mA (1, 2)
V_{OL2}	Output Low Voltage (DDR-II SDRAM)		0.414	V	I_{OL} = 20.7mA (3)
V_{OH2}	Output High Voltage (DDR-II SDRAM)	1.314		V	I_{OH} = -18mA (3)
V_{OL3}	Output Low Voltage (PCI-X)		0.1 × $\mathbf{V_{CC33}}$	V	$\mathbf{I_{OL}}$ = 1500 µA
V_{OH3}	Output High Voltage (PCI-X)	0.9 × $\mathbf{V_{CC33}}$		V	$\mathbf{I_{OH}}$ = -500 µA
$\mathbf{C_{IN}}$	Input pin Capacitance		8	pF	(6)
$\mathbf{C_{CLK}}$	PCI clock pin Capacitance		8	pF	(6)
L_{PIN}	Ball Inductance		15	nH	(1, 2, 6)

Notes:
1. SDRAM signals include **MA[12:0]**, **BA[1:0]**, **CAS#**, **CS[1:0]#**, **CKE[1:0]**, **DM[8:0]**, **RAS#**, **WE#**,**M_CK[2:0]**, **M_CK[2:0]#**, **DQ[63:0]**, **DQS[8:0]** and **CB[7:0]**.
2. For 2.5 V DDR SDRAM support.
3. For 1.8 V DDR-II SDRAM support.
4. Miscellaneous signals include all signals that are not PCI-X or SDRAM signals.
5. Includes PCI-X Express Auxiliary signals; **PWRGD**
6. Ensured by design.

Table 24. I_{CC} Characteristics

Symbol	Parameter	Typ.	Max.	Units	Notes
I_{LI1}	Input Leakage Current for each signal except **TCK**, **TMS**, **TRST#**, **TDI**		± 2	µA	$0 \le \mathbf{V_{IN}} \le \mathbf{V_{CC}}$ (4)
I_{LI2}	Input Leakage Current for **TCK**, **TMS**, **TRST#**, **TDI**	-140	-250	µA	$\mathbf{V_{IN}}$ = 0.45 V (1, 4)
$\mathbf{I_{CC33}}$ Active (Power Supply)	Power Supply Current - PCI-X interfaces Both at 66 MHz Both at 100 MHz Both at 133 MHz		 1.33 1.20 1.04	 A	(1, 2)
$\mathbf{I_{CC25}}$ Active (Power Supply)	Power Supply Current - DDR		0.580	A	(1, 2)
$\mathbf{I_{CC18}}$ Active (Power Supply)	Power Supply Current - DDR-II		0.487	A	(1, 2)
$\mathbf{I_{CC15}}$ Active (Power Supply)	Power Supply Current - IOP/Bridge core		4.7	A	(1, 2)
$\mathbf{I_{CC13}}$ Active (Power Supply)	Power Supply Current - Intel XScale® core 800 MHz 667 MHz 500 MHz		 0.453 0.411 0.358	 A	(1, 2)
$\mathbf{I_{CC33}}$ Active (Thermal)	Thermal Current - PCI-X interfaces Both at 66 MHz Both at 100 MHz Both at 133 MHz	 1.08 1.00 0.914		 A	(1, 3)
$\mathbf{I_{CC25}}$ Active (Thermal)	Thermal Current - DDR	0.295		A	(1, 3)
$\mathbf{I_{CC18}}$ Active (Thermal)	Thermal Current - DDR-II	0.255		A	(1, 3)
$\mathbf{I_{CC15}}$ Active (Thermal)	Thermal Current - IOP/Bridge core	3.8		A	(1, 3)
$\mathbf{I_{CC13}}$ Active (Thermal)	Thermal Current - Intel XScale® core 800 MHz 667 MHz 500 MHz	 0.430 0.390 0.340		 A	(1, 3)

Notes:

1. Measured with device operating and outputs loaded to the test condition in Figure 14, “AC Test Load for All Signals Except PCI and DDR SDRAM” on page 73.
2. I_{CC} Active (Power Supply) value is provided for selecting the system power supply. This is based on the worst case data patterns and skew material at the following worst case voltages: $\mathbf{V_{CC33}}$ = 3.63 V, $\mathbf{V_{CC25}}$ = 2.7 V, $\mathbf{V_{cc18}}$ = 1.9v, $\mathbf{V_{CC15}}$ = 1.575 V, $\mathbf{V_{CC13}}$ = 1.41 V.
3. I_{CC} Active (Thermal) value is provided for selecting the system thermal design power (TDP). This is based on the following typical voltages: $\mathbf{V_{CC33}}$ = 3.3 V, $\mathbf{V_{CC25}}$ = 2.5 V, $\mathbf{V_{cc18}}$ = 1.8v, $\mathbf{V_{CC15}}$ = 1.5 V, $\mathbf{V_{CC13}}$ = 1.35 V.
4. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.

4.4 Targeted AC Specifications

4.4.1 Clock Signal Timings

Table 25. PCI Clock Timings

Symbol	Parameter	PCI-X 133		PCI-X 100		PCI-X 66		PCI 66		PCI 33		Units	Notes
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max		
T_{F1}	PCI clock Frequency	100	133	66	100	50	66	33	66	16	33	MHz	1
T_{C1}	PCI clock Cycle Time - Avg.	7.5	10	10	15	15	20	15	30	30	60	ns	1
	Absolute Minimum	7.375		9.875		14.8		14.8		29.7		ns	3,4
T_{CH1}	PCI clock High Time	3		3		6		6		11		ns	
T_{CL1}	PCI clock Low Time	3		3		6		6		11		ns	
T_{SR1}	PCI clock Slew Rate	1.5	4	1.5	4	1.5	4	1.5	4	1	4	V/ns	2
PCI Spread Spectrum Requirements													
f_{mod}	PCI clock modulation frequency	30	33	30	33	30	33	30	33			KHz	
f_{spread}	PCI clock frequency spread	-1	0	-1	0	-1	0	-1	0			%	

Notes:
1. Clock frequency may not change beyond spread-spectrum limits except while **RSTIN#** is asserted or **PWRGD** deasserted.
2. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.
3. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.
4. Clock jitter class 2, per PCI-X Electrical and Mechanical Rev 2.0a specification

Table 26. DDR Clock Timings

Symbol	Parameter	DDR-II 400		DDR333		Units	Notes
		Minimum	Maximum	Minimum	Maximum		
T_{F2}	DDR SDRAM clock Frequency		200		167	MHz	
T_{C2}	DDR SDRAM clock Cycle Time	5.0		6.0/7.5(1)		ns	
T_{CH2}	DDR SDRAM clock High Time	2.15		2.7/3.37(1)		ns	
T_{CL2}	DDR SDRAM clock LowTime	2.15		2.7/3.37(1)		ns	
T_{CS2}	DDR SDRAM clock Period Stability		350		350	ps	
T_{skew2}	DDR SDRAM clock skew for any differential clock pair (**M_CK[2:0]** - **M_CK[2:0]#**)		100		100	ps	
T_{skew3}	DDR SDRAM clock skew for any clock pair and any system memory strobe (**M_CK** - **DQS**).	-285	285	-285	285	ps	2

Notes:
1. CL = 2.5/2.0.
2. This specification applies for writes only; that is, when the 80333 is driving the strobes as well as the clocks. Refer to the JEDEC specification for an explanation of strobe to clock timing for DDR reads.

Table 27. PCI Express* Clock Timings

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
T_{F2}	PCI Express* clock frequency	-300ppm	100	+300 ppm	MHz	1
T_{C2}	PCI Express* clock cycle time	10		10.2	ns	2
T_{CCJ}	Cycle to Cycle Jitter			200	ps	
	Clock duty cycle	45		55	%	
T_{rise}	REFCLK rise time across 600mV	300		600	ps	3
T_{fall}	REFCLK fall time across 600mV	300		600	ps	3
	Rise-Fall matching			20	%	3,4
	Cross point at 1V	0.51		0.76	V	
	Rising edge ringback	0.85			V	
	Falling edge ringback			0.35	V	

Notes:

1. Spread spectrum clocking is allowed with the following three requirements;
   a. All device timings must be met including jitter, skew, min./max. clock period. Output rise/fall timing MUST meet the existing non-spread spectrum specifications.
   b. All non-spread Host and PCI functionality must be maintained in the spread-spectrum mode (includes all power management functions).
   c. The minimum clock period cannot be violated. The preferred method is to adjust the spread technique to allow for modulation above the nominal frequency. This technique is often called “down-spreading”.
2. Measured at crossing point.
3. Measured from V_{OL} = 0.2 V to V_{OH} = 0.8 V.
4. Determined as a fraction of 2 × (Trise - Tfall)/(Trise + Tfall).

4.4.2 DDR/DDR-II SDRAM Interface Signal Timings

Table 28. DDR SDRAM Signal Timings

Symbol	Parameter	Minimum	Max.	Units	Notes
T_{VB1}	DQ, CB and DM write output valid time before DQS.	2.68		ns	(4)
T_{VA1}	DQ, CB and DM write output valid time after DQS.	2.68		ns	(4)
T_{VB3}	Address and Command write output valid before M_CK rising edge.	2.62		ns	(4,9)
T_{VA3}	Address and Command write output valid after M_CK rising edge.	2.62		ns	(4,9)
T_{VB4}	DQ, CB and DM read input valid time before DQS rising or falling edges.	0.35		ns	(6)
T_{VA4}	DQ, CB and DM read input valid time after DQS rising or falling edges.	0.35		ns	(6)
T_{VB5}	CS[1:0]# control valid before M_CK rising edge.	2.62		ns	(4)
T_{VA5}	CS[1:0]# control valid after M_CK rising edge.	2.62		ns	(4)
T_{VB6}	DQS write preamble duration.	4.50 (nominal)		ns	(7)
T_{VA6}	DQS write postamble duration.	3.00 (nominal)		ns	(7)

Notes:

1. See Figure 7, “Output Timing Measurement Waveforms” on page 69.
2. See Figure 8, “Input Timing Measurement Waveforms” on page 70.
3. Clock to output valid times are specified with a 0 pF loading.
4. See Figure 11, “DDR SDRAM Write Timings” on page 71.
5. See Figure 13 “DQS falling edge output access time to M_CK rising edge.
6. See Figure 12, “DDR SDRAM Read Timings” on page 71. Data to strobe read setup and data from strobe read hold minimum requirements specified are determined with the DQS delay programmed for a 90 degree phase shift.
7. See Figure 13, “Write PreAmble/PostAmble Durations” on page 72.
8. See Figure 15, “AC Test Load for DDR SDRAM Signals” on page 73.
9. Address/Command pin group; **RAS#**, **CAS#**, **WE#**, **MA[12:0]**, **BA[1:0]**.

Table 29. DDR-II SDRAM Signal Timings

Symbol	Parameter	Min.	Max.	Units	Notes
T_{VB1}	DQ, CB and DM write output valid time before DQS crossing.	2.12		ns	4
T_{VA1}	DQ, CB and DM write output valid time after DQS crossing.	2.12		ns	4
T_{VB3}	Address and Command write output valid before M_CK rising edge	2.12		ns	4
T_{VA3}	Address and Command write output valid after M_CK rising edge	2.12		ns	4,8
T_{VB4}	DQ, CB and DM read input valid time before DQS rising or falling edges	0.35		ns	6
T_{VA4}	DQ, CB and DM read input valid time after DQS rising or falling edges	0.35		ns	6
T_{VB5}	CS[1:0]# control valid before M_CK rising edge.	2.12		ns	4
T_{VA5}	CS[1:0]# control valid after M_CK rising edge.	2.12		ns	4
T_{VB6}	DQS write preamble duration.	3.75 (nom.)		ns	9
T_{VA6}	DQS write postamble duration.	2.50 (nom.)		ns	9

Notes:
1. See Figure 7, “Output Timing Measurement Waveforms” on page 69.
2. See Figure 8, “Input Timing Measurement Waveforms” on page 70.
3. Clock to output valid times are specified with a 0 pF loading.
4. See Figure 11, “DDR SDRAM Write Timings” on page 71.
5. See Figure 13 “DQS falling edge output access time to M_CK rising edge.
6. See Figure 12, “DDR SDRAM Read Timings” on page 71. Data to strobe read setup and data from strobe read hold minimum requirements specified are determined with the DQS delay programmed for a 90 degree phase shift.
7. See Figure 15, “AC Test Load for DDR SDRAM Signals” on page 73.
8. Address/Command pin group: **RAS#, CAS#, WE#, MA[12:0], BA[1:0], ODT[1:0]**.
9. See Figure 13, “Write PreAmble/PostAmble Durations” on page 72.

4.4.3 Peripheral Bus Interface Signal Timings

Table 30. Peripheral Bus Signal Timings

Symbol	Parameter	Min.	Max.	Units	Notes
T_{OV1}	Output Valid Delay from M_CK	1	5	ns	(1, 3)
T_{OF}	Output Float Delay from M_CK	1	5	ns	(1, 3)
T_{IS1}	Input Setup to M_CK	4.5		ns	(2)
T_{IH1}	Input Hold from M_CK	2		ns	(2)
T_{AH1}	**ALE** High time	15		ns	
T_{AV1}	**ALE** high to address Valid		0	ns	
T_{AH2}	**ALE** low to address invalid		15	ns	
T_{AS1}	Address valid to **ALE** low	15		ns	
T_{AO1}	**ALE** low to **POE#** low	0		ns	
T_{AW1}	**ALE** low to **PWE#** low	15		ns	
T_{AH3}	**PWE#** high to Data Invalid	15		ns	
T_{AS2}	Data valid to **PWE#** high	60		ns	
T_{AC1}	**ALE** low to **PCE[1:0]#** low	15		ns	

Notes:
1. See Figure 7, “Output Timing Measurement Waveforms” on page 69.
2. See Figure 8, “Input Timing Measurement Waveforms” on page 70.
3. See Figure 14, “AC Test Load for All Signals Except PCI and DDR SDRAM” on page 73.
4. See Table 32, AC Measurement Conditions.
5. All timing referenced to M_CK is for functional testing, for the cases where M_CK × N = IBCLK.
6. PBI Clock is internal only; 66 MHz with 333 MHz internal bus.

Table 31. PCI Signal Timings

Symbol	Parameter	PCI-X 133 PCI-X 100		PCI-X 66		PCI 66		PCI 33		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
T_{OV1}	Clock to Output Valid Delay for bused signals	0.7	3.8	0.7	3.8	1	6	2	11	ns	(1,2,3)
T_{OV2}	Clock to Output Valid Delay for point to point signals	0.7	3.8	0.7	3.8	2	6	2	12	ns	(1,2,3)
T_{OF}	Clock to Output Float Delay		7		7		14		28	ns	(1,7)
T_{IS1}	Input Setup to clock for bused signals	1.2		1.7		3		7		ns	(3,4,8)
T_{IS2}	Input Setup to clock for point to point signals	1.2		1.7		5		10, 12		ns	(3,4)
T_{IH1}	Input Hold time from clock	0.5		0.5		0		0		ns	(4)
T_{RST}	Reset Active Time	1		1		1		1		ms	
T_{RF}	Reset Active to output float delay		40		40		40		40	ns	(5,6)
T_{IS3}	REQ64# to Reset setup time	10		10		10		10		clocks	
T_{IH2}	Reset to REQ64# hold time	0	50	0	50	0	50	0	50	ns	
T_{IS4}	PCI-X initialization pattern to Reset setup time	10		10						clocks	
T_{IH3}	Reset to PCI-X initialization pattern hold time	0	50	0	50					ns	

Notes:

1. See the timing measurement conditions in; Figure 7, “Output Timing Measurement Waveforms” on page 69.
2. See Figure 16, “PCI/PCI-X TOV(max) Rising Edge AC Test Load” on page 73, Figure 17, “PCI/PCI-X TOV(max) Falling Edge AC Test Load” on page 74, and Figure 18, “PCI/PCI-X TOV(min) AC Test Load” on page 74.
3. Setup time for point-to-point signals applies to **REQ#** and **GNT**# only. All other signals are bused.
4. See the timing measurement conditions in Figure 8, “Input Timing Measurement Waveforms” on page 70.
5. RST# is asserted and deasserted asynchronously with respect to **CLK.**
6. All output drivers must be floated when **RST#** is active.
7. For purposes of Active/Float timing measurements, the HI-Z or ‘off’ state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

4.4.4 I²C/SMBus Interface Signal Timings

Table 32. I²C/SMBus Signal Timings

Symbol	Parameter	Std. Mode		Fast Mode		Units	Notes
		Min.	Max	Min.	Max		
F_{SCL}	**SCL** Clock Frequency	0	100	0	400	KHz	
T_{BUF}	Bus Free Time Between STOP and START Condition	4.7		1.3		µs	(1)
T_{HDSTA}	Hold Time (repeated) START Condition	4		0.6		µs	(1, 3)
T_{LOW}	**SCL** Clock Low Time	4.7		1.3		µs	(1, 2)
T_{HIGH}	**SCL** Clock High Time	4		0.6		µs	(1, 2)
T_{SUSTA}	Setup Time for a Repeated START Condition	4.7		0.6		µs	(1)
T_{HDDAT}	Data Hold Time	0	3.45	0	0.9	µs	(1)
T_{SUDAT}	Data Setup Time	250		100		ns	(1)
T_{SR}	**SCL** and **SDA** Rise Time		1000	20 + 0.1$\mathbf{C_b}$	300	ns	(1, 4)
T_{SF}	**SCL** and **SDA** Fall Time		300	20 + 0.1$\mathbf{C_b}$	300	ns	(1, 4)
T_{SUSTO}	Setup Time for STOP Condition	4		0.6		µs	(1)

Notes:
1. See Figure 9, "I2C/SMBus Interface Signal Timings" on page 70.
2. Not tested.
3. After this period, the first clock pulse is generated.
4. C_b = the total capacitance of one bus line, in pF.
5. Std. Mode I²C signal timings apply for SMBus timing.

4.4.5 UART Interface Signal Timings

Table 33. UART Signal Timings

Symbol	Parameter	Std. Mode		Units	Notes
		Min.	Max		
T_{XD1}	Ux_TXD output delay from M_CK rising edge		60	ns	1
T_{RXS1}	Ux_RXD data setup time (to M_CK rising edge).	50		ns	2
T_{RXH1}	Ux_RXD data hold time (to M_CK rising edge).	50		ns	2
T_{CTS1}	Ux_CTS setup time (to M_CK rising edge).	60		ns	
T_{CTH1}	Ux_CTS hold time (to M_CK rising edge).	60		ns	
T_{RTS1}	Ux_RTS setup time (to M_CK rising edge).	60		ns	
T_{RTH1}	Ux_RTS hold time (to M_CK rising edge).	60		ns	

Notes:
1. See Figure 10, "UART Transmitter Receiver Timing" on page 70.
2. All timings referenced to M_CK for functional testing, is for cases where M_CK × N = IBCLK.

4.4.6 PCI Express* Differential Transmitter (Tx) Output Specifications

Table 34. PCI Express* Tx Output Specifications

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
UI	Unit Interval		400		ps	1
$V_{DIFFp-p}$	Differential output voltage	.800		1.200	V	2
T_{rise}, T_{fall}	Driver Rise/Fall Time	0.2		0.4	UI	3
$V_{TX-CM-AC}$	AC Common Mode			20	mV	4
$V_{TX-CM-DC}$ delta	Common Mode Active to Sleep mode delta	-50		+50	mV	
RL-$Diff_{TX}$	Differential Return Loss	15			dB	5
RL-CM_{TX}	Common Mode Return Loss	6			dB	5
$Z_{TX-OUT-DC}$	DC Differential Output Impedance	90	100	110	Ω	6
$Z_{TX-Match-DC}$	D+/D- impedance matching	-5		+5	%	7
$L_{SKEW-TX}$	Lane to Lane Skew at Tx			500	ps	8
J_{TOTAL}	Total Output Jitter.			0.35	UI	9
T_{Deye}	Minimum Transmitter eye opening.	0.65			UI	10
$I_{TX-SHORT}$	Short Circuit Current	-100		100	mA	11
$V_{TX-IDLE}$	Sleep mode Voltage Output	0	0	20	mV	12

Notes:

1. ±300 ppm. UI does not account for SSC dictated variations. No test load is necessarily associated with this value. This UI spec is a 'before transmission' specification and represents the nominal time of each bit transmission or width.
2. Peak-Peak differential voltage. $\mathbf{V_{DIFFp-p}} = 2 \times \mathbf{V_{DMAx}}$. Specified at the package pins into a 100 Ω test load as shown in Figure 19, "Transmitter Test Load (100 W differential load)" on page 74. Max level set by maximum single ended voltage after a reflection from an open. This value is for the first bit after a transition on the data lines. Subsequent bits of the same polarity shall have an amplitude of 6 dB (±0.5 dB) less as measured differentially peak to peak than the specified value.
3. 20–80% at Transmitter. Slower rise/fall times are better.
4. Peak common mode value. $|\mathbf{V_{D+}} + \mathbf{V_{D-}}|/2 - \mathbf{V_{CM-DC(avg)}}$.
5. 50 MHz to 1.6 GHz. The driver output impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.8 GHz. This output impedance requirement applies to all valid output levels. The reference impedance for return loss measurements is 100 Ω for differential return loss and 25 Ω for common mode (i.e., as measured by a Vector Network Analyzer with 100 Ω differential probes). Note this is based on a nominal PCI Express* interconnect differential characteristic impedance of 100 Ω. Applicable during active (L0) and Align states only.
6. DC Differential Mode Impedance 100 Ω ±10% tolerance. All devices shall employ on-chip adaptive impedance matching circuits to ensure the best possible termination/Zout for its Transmitters (as well as Receivers).
7. DC impedance matching between two lanes of a port.
8. Between any two lanes within a single Transmitter.
9. Clock source PPM mismatch is in addition to this value. Measured over 250 UI.
10. See Figure 20, "Transmitter Eye Diagram" on page 75.
11. Between any voltage from max supply to gnd with power on or off.
12. Squelch condition. Both signals brought to $\mathbf{V_{CM-DC-}}|\mathbf{VD+} - \mathbf{VD-}|$.

4.4.7 PCI Express* Differential Receiver (Rx) Input Specifications

Table 35. PCI Express* Rx Input Specifications

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
$V_{DIFFp-p}$	Differential input voltage	0.175		1.200	V	1
J_{TOTAL}	Total Output Jitter.			0.65	UI	2
V_{CM-AC}	AC Common Mode			100	mV	3
T_{Reye}	Receiver eye opening.	0.35			UI	4
RL-$Diff_{RX}$	Differential Return Loss	15			dB	5
RL-CM_{TX}	Common Mode Return Loss	6			dB	5
$Z_{RX-OUT-DC}$	DC Differential Output Impedance	90	100	110	Ω	6
$Z_{RX-Match-DC}$	D+/D- impedance matching	-5		+5	%	7
$V_{RX-SQUELCH}$	Squelch detect threshold	75		175	mV	8
Cin_{RX}	AC coupled	400			pF	9
$L_{SKEW-RX}$	Lane to Lane Skew at Rx			20	UI	10

Notes:

1. Peak-Peak differential voltage. $\mathbf{V_{DIFFp-p}} = 2 \times \mathbf{V_{RMAx}}$. Measured at the package pins of the receiver. See Figure 20, “Transmitter Eye Diagram” on page 75.
2. Max Jitter tolerated by Rx. This is the nominal value tolerated at the package pin of the receiver device. A receiver must therefore tolerate any additional jitter generated by the package to the die.
3. Peak common mode value. $|\mathbf{V_{D+}} + \mathbf{V_{D-}}|/2 - \mathbf{V_{CM-DC(avg)}}$.
4. See Figure 21, “Receiver Eye Opening (Differential)” on page 75.
5. 50 MHz to 1.6 GHz. The driver output impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.8 GHz. This output impedance requirement applies to all valid output levels. The reference impedance for return loss measurements is 100 Ω for differential return loss and 25 Ωs for common mode (i.e., as measured by a Vector Network Analyzer with 100 Ω differential probes). Note this is based on a nominal PCI Express* interconnect differential characteristic impedance of 100 Ω. Applicable during active (L0) and Align states only.
6. DC Differential Mode Impedance 100 Ω ±10% tolerance.
7. DC impedance matching between two lanes of a port.
8. Peak to Peak value. Measured at the pin of the receiver. Differential signal below this level will indicate a squelch condition.
9. All receivers shall be AC coupled to the media.
10. Lane skew at the Receiver that must be tolerated.

4.4.8 Boundary Scan Test Signal Timings

Table 36. Boundary Scan Test Signal Timings

Symbol	Parameter	Min.	Max	Units	Notes
T_{BSF}	**TCK** Frequency	0	$0.5T_F$	MHz	
T_{BSCH}	**TCK** High Time	15		ns	Measured at 1.5 V (1).
T_{BSCL}	**TCK** Low Time	15		ns	Measured at 1.5 V (1).
T_{BSCR}	**TCK** Rise Time		5	ns	0.8 V to 2.0 V (1)
T_{BSCF}	**TCK** Fall Time		5	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to **TCK** — **TDI**, **TMS**	3		ns	(4)
T_{BSIH1}	Input Hold from **TCK** — **TDI**, **TMS**	5		ns	(4)
T_{BSOV1}	**TDO** Valid Delay	5	15	ns	Relative to falling edge of **TCK** (2, 3).
T_{OF1}	**TDO** Float Delay	5	15	ns	Relative to falling edge of **TCK** (2, 5).

Notes:
1. Not tested.
2. Outputs precharged to $\mathbf{V_{CC5}}$.
3. See Figure 7, “Output Timing Measurement Waveforms” on page 69.
4. See Figure 8, “Input Timing Measurement Waveforms” on page 70.
5. A float condition occurs when the output current becomes less than ILO. Float delay is not tested. See Figure 7, “Output Timing Measurement Waveforms” on page 69.

4.5 AC Timing Waveforms

Figure 6. Clock Timing Measurement Waveforms

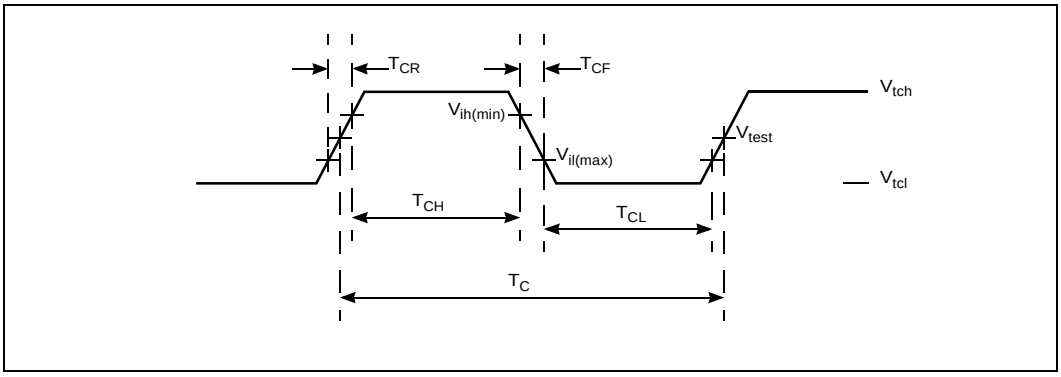


Figure 7. Output Timing Measurement Waveforms

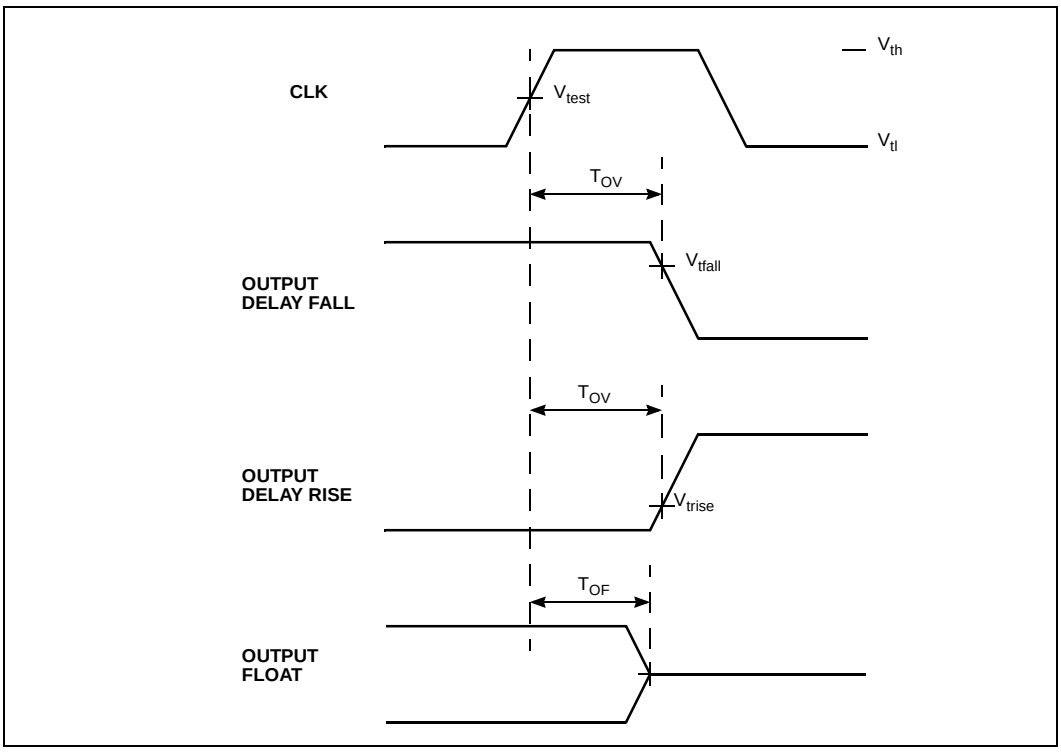


Figure 8. Input Timing Measurement Waveforms

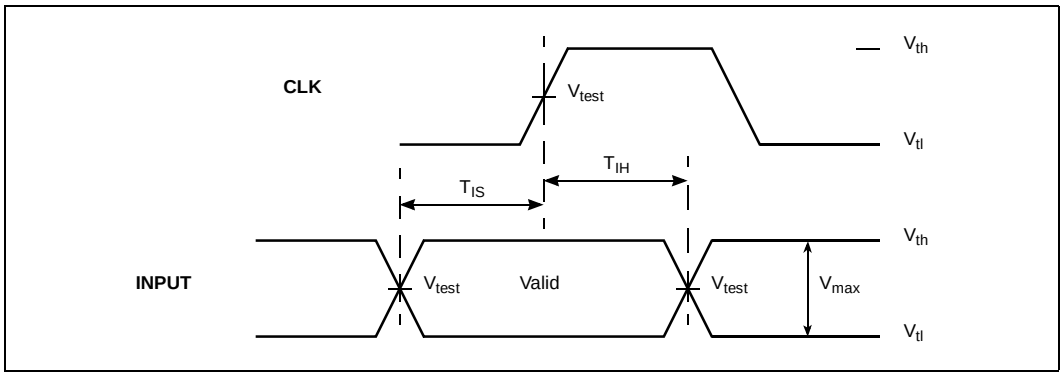


Figure 9. I²C/SMBus Interface Signal Timings

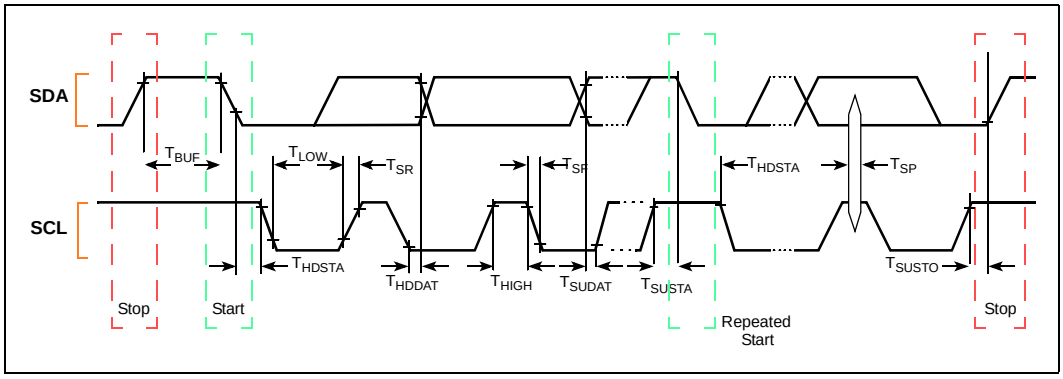


Figure 10. UART Transmitter Receiver Timing

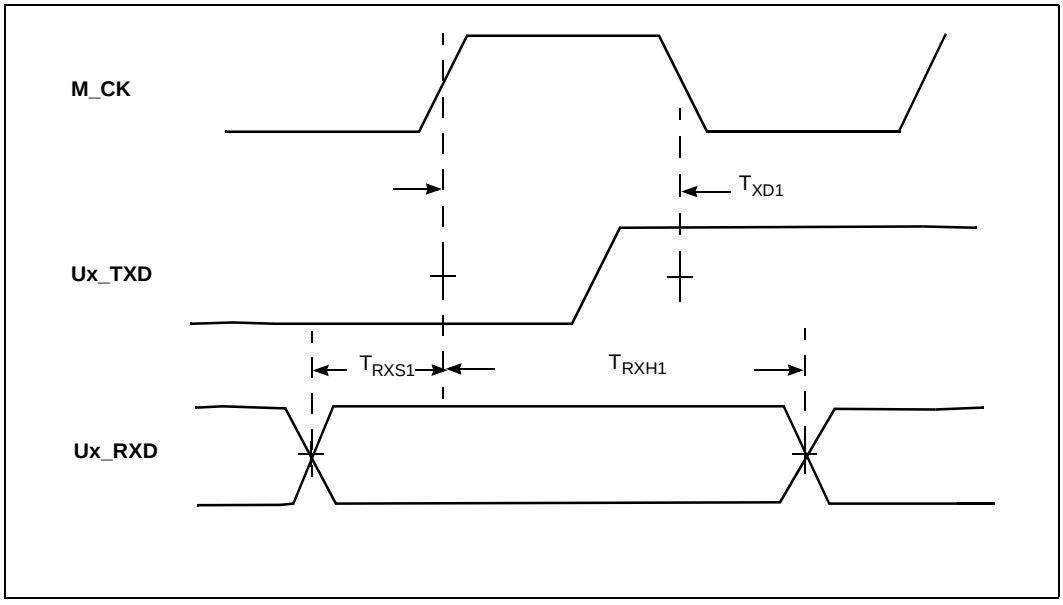


Figure 11. DDR SDRAM Write Timings

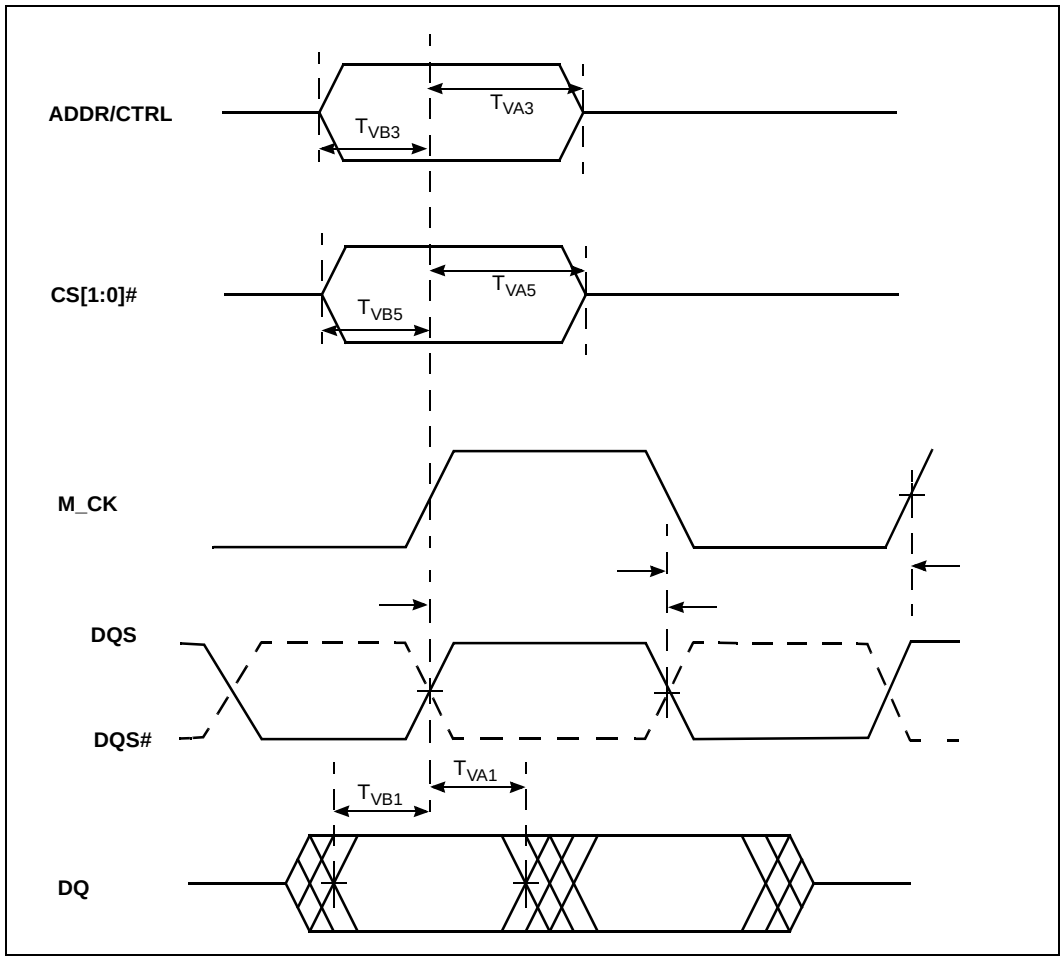


Figure 12. DDR SDRAM Read Timings

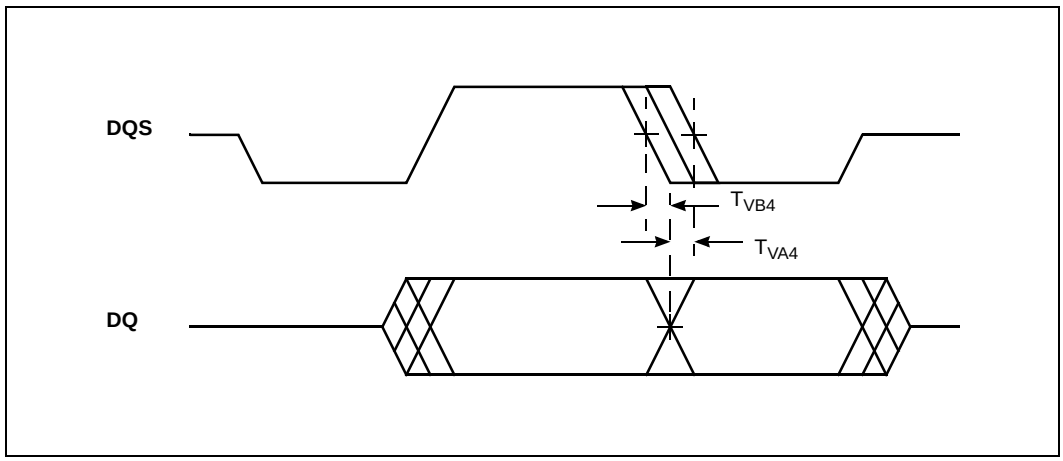
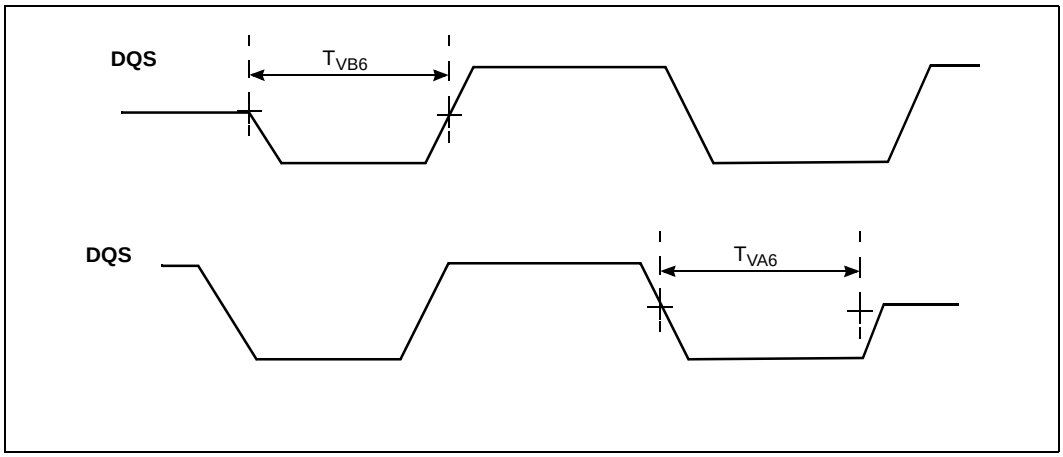


Figure 13. Write PreAmble/PostAmble Durations



4.6 AC Test Conditions

Table 37. AC Measurement Conditions

Symbol	PCI-X	PCI	DDR / DDR-II	DDR-II	PBI	Units
V_{th}	0.6 V_{CC33}	0.6 V_{CC33}	2.0 / 1.15	1.15	2.0	V
V_{tl}	0.25 V_{CC33}	0.2 V_{CC33}	0.5 / 0.2	0.2	0.8	V
V_{test}	0.4 V_{CC33}	0.4 V_{CC33}	1.25 / 0.90	0.90	1.5	V
V_{trise}	0.285 V_{CC33}	0.285 V_{CC33}	1.25 / 0.90	0.90	1.5	V
V_{tfall}	0.615 V_{CC33}	0.615 V_{CC33}	1.25 / 0.90	0.90	1.5	V
V_{max}	0.4 V_{CC33}	0.4 V_{CC33}	1.5 / 0.97	0.97	1.2	V
Slew Rate[1]	1.5	1.5	1.0	1.0	1.0	V/nS

Notes:
1. Input signal slew rate is measured between V_{il} and V_{ih}.

Figure 14. AC Test Load for All Signals Except PCI and DDR SDRAM

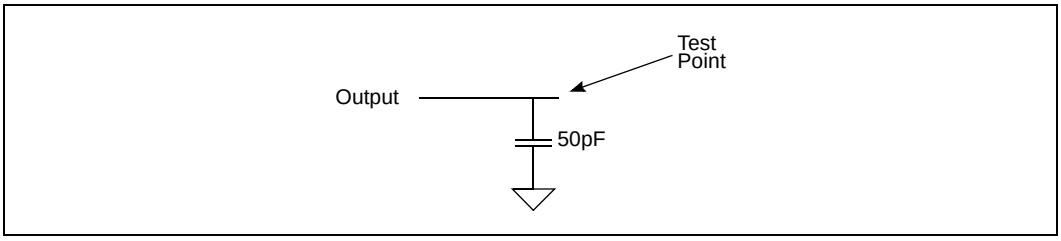


Figure 15. AC Test Load for DDR SDRAM Signals

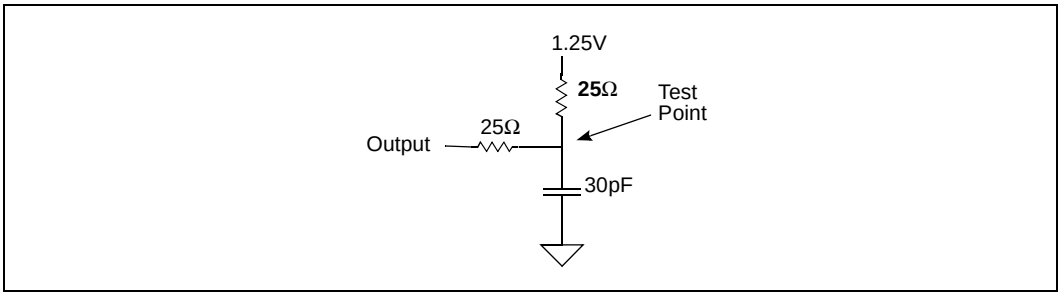


Figure 16. PCI/PCI-X $T_{OV(max)}$ Rising Edge AC Test Load

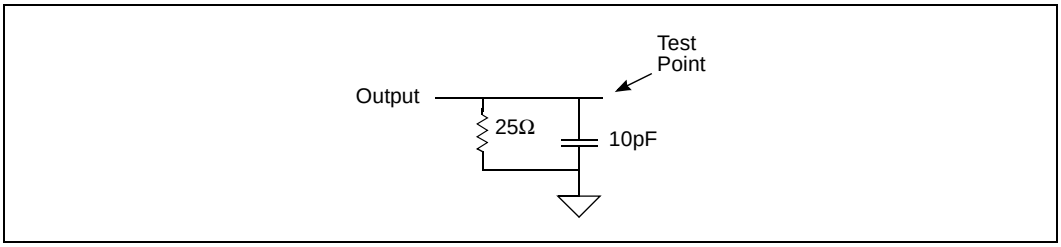


Figure 17. PCI/PCI-X $T_{OV(max)}$ Falling Edge AC Test Load

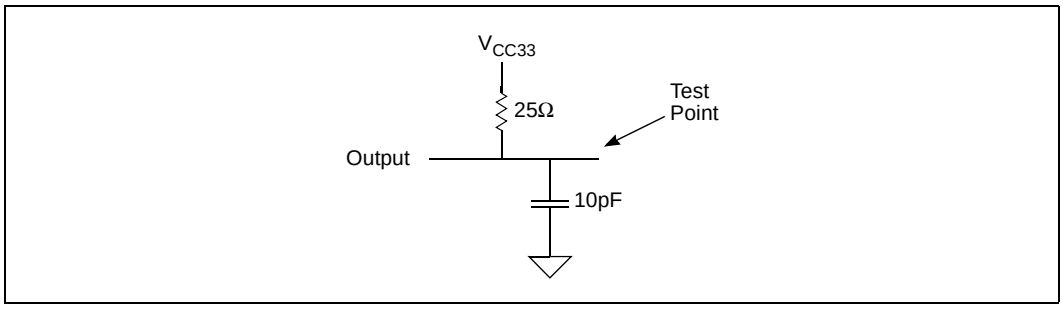


Figure 18. PCI/PCI-X $T_{OV(min)}$ AC Test Load

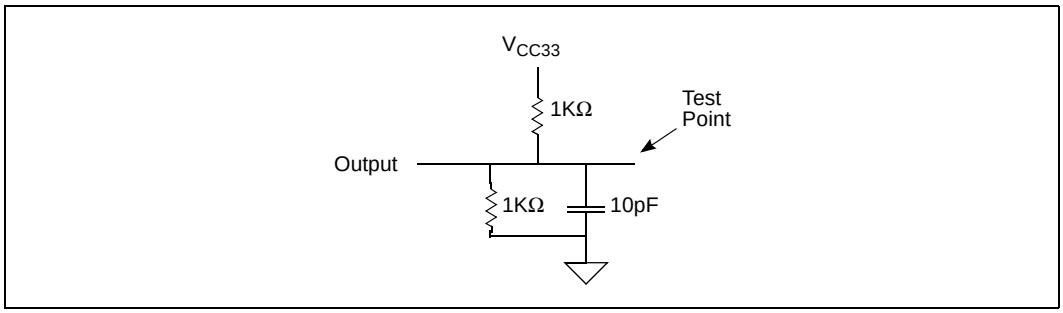


Figure 19. Transmitter Test Load (100 Ω differential load)

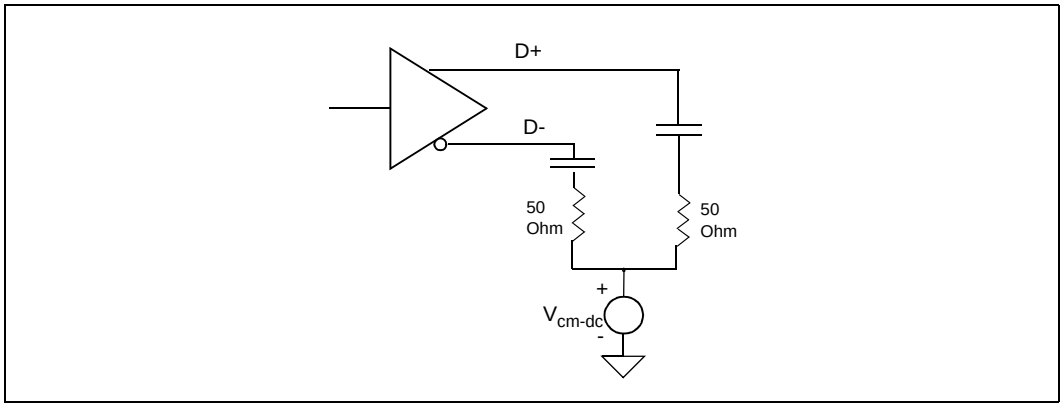


Figure 20. Transmitter Eye Diagram

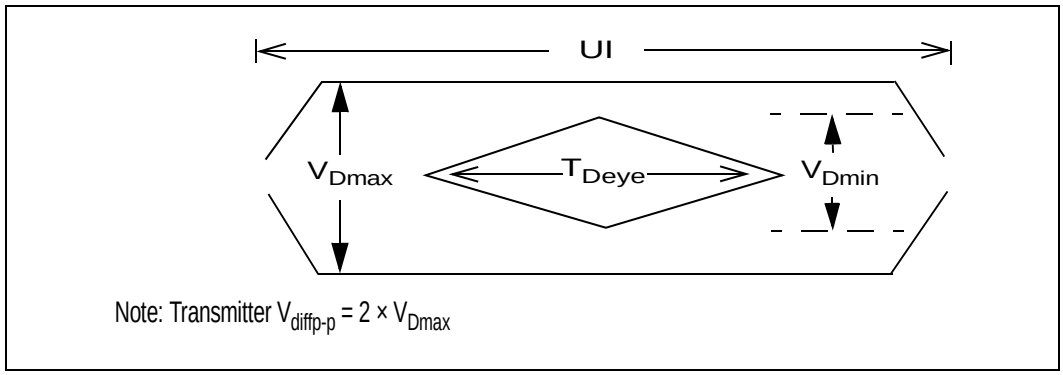


Figure 21. Receiver Eye Opening (Differential)