Intel® 80333 I/O Processor

Design Guide

March 2005

Order Number: 305434-001US

Contents

Figures

Tables

Revision History

Date	Revision	Description
March 2005	001	Initial release

Introduction 1

1.1 About This Document

This document provides layout information and guidelines for designing platform or add-in board applications with the Intel® 80333 I/O Processor (80333), which is ARM* architecture compliant. It is recommended that this document be used as a guideline. Intel recommends employing best-known design practices with board level simulation, signal integrity testing and validation for a robust design.

Designers please note that this guide focuses upon specific design considerations for the 80333 and is not intended to be an all-inclusive list of all good design practices. Use this guide as a starting point and use empirical data to optimize your particular design.

Intel Corporation assumes no responsibility for any errors which may appear in this document nor does it make a commitment to update the information contained herein.

Intel retains the right to make changes to these specifications at any time, without notice. In particular, descriptions of features, timings, packaging, and pin-outs does not imply a commitment to implement them. In fact, this specification does not imply a commitment by Intel to design, manufacture, or sell the product described herein.

1.1.1 Terminology and Definitions

Table 1. Terminology and Definitions (Sheet 1 of 2)

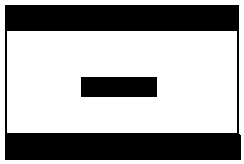
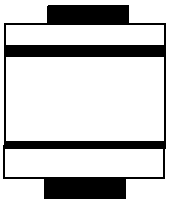
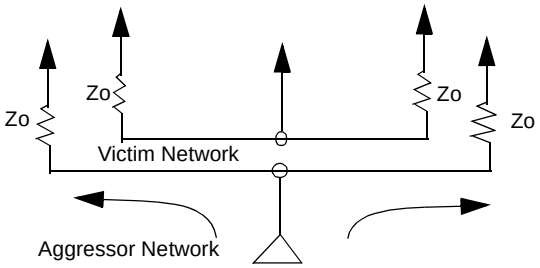
Term	Definition	
80333	Intel® 80333 I/O Processor	
Stripline		Stripline in a PCB is composed of the conductor inserted in a dielectric with GND planes to the top and bottom. **NOTE:** An easy way to distinguish stripline from microstrip is that you need to strip away layers of the board to view the trace on stripline.
Microstrip		Microstrip in a PCB is composed of the conductor on the top layer above the dielectric with a ground plane below
Prepreg	Material used for the lamination process of manufacturing PCBs. It consists of a layer of epoxy material that is placed between two cores. This layer melts into epoxy when heated and forms around adjacent traces.	
Core	Material used for the lamination process of manufacturing PCBs. This material is two sided laminate with copper on each side. The core is an internal layer that is etched.	
PCB	 Example of a Four-Layer Stack	Printed circuit board. Example manufacturing process consists of the following steps: • Consists of alternating layers of core and prepreg stacked • The finished PCB is heated and cured. • The via holes are drilled • Plating covers holes and outer surfaces • Etching removes unwanted copper • Board is tinned, coated with solder mask and silk screened
DDR	Double Data Rate Synchronous DRAM. Data is clocked on both rising and falling edges of the clock.	
DDR II	DDR II is backward compatible with DDR I. However, it has an increased DDR data rate to 3.2 GBytes/sec with a clock rate of 200 MHz for multiple DIMM configurations. It allows data rate of 6.4 Gbytes/sec with a clock rate of 400 MHz for a single DIMM point to point configuration.	
DIMM	Dual Inline Memory Module	
Source Synchronous DDR	• For reads data leaves the DDR or memory controller with a data strobe. The memory controller delays the data strobe internally to line it up with the data valid window. • For writes the memory controller places the data strobe in the middle of the data valid window to ensure that the correct data gets clocked into the DRAM.	
SSTL_2	Series Stub Terminated Logic for 2.5 V	
JEDEC	Provides standards for the semiconductor industry.	
DLL	Delay Lock Loop - refers to the DDR feature used to provide appropriate strobe delay to clock in data.	

Table 1. Terminology and Definitions (Sheet 2 of 2)

Term	Definition
Aggressor	A network that transmits a coupled signal to another network is aggressor network. 
Victim	A network that receives a coupled cross-talk signal from another network is a victim network.
Network	The trace of a PCB that completes an electrical connection between two or more components.
Stub	Branch from a trunk terminating at the pad of an agent.
ISI	Intersymbol Interference (ISI). This occurs when a transition that has not been completely dissipated, interferes with a signal being transmitted down a transmission line. ISI can impact both the timing and signal integrity. It is dependent on frequency, time delay of the line and the refection coefficient at the driver and receiver. Examples of ISI patterns that could be used in testing at the maximum allowable frequencies are the sequences shown below: 0101010101010101 0011001100110011 0001110001110001111
CRB	Customer Reference Board
PC1600	JEDEC Names for DDR based on peak data rates. PC1600= clock of 100 MHz * 2 data words/clock * 8 bytes = 1600 MB/sec
PC2100	JEDEC Names for DDR based on peak data rates. PC2100= clock of 133 MHz * 2 data words/clock * 8 bytes = 2128 MB/sec
PC2700	JEDEC Names for DDR II based on peak data rates. PC2700= clock of 167 MHz * 2 data words/clock * 8 bytes = 2672 MB/sec
PC3200	JEDEC Names for DDR II based on peak data rates. PC3200= clock of 200 MHz * 2 data words/clock * 8 bytes = 3200 MB/sec
Downstream	At or toward a PCI Express port directed to the PCI Express root complex (to a bus with a lower number)
Upstream	At or toward a PCI Express port directed away from root complex (to a bus with a higher number).
Local memory	Memory subsystem on the Intel XScale® core DDR SDRAM or Peripheral Bus Interface busses.
DWORD	32-bit data word.
Local bus	80333 Internal Bus.
Outbound	At or toward the PCI interface of the 80333 ATU from the Internal Bus.
Inbound	At or toward the Internal Bus of the 80333 from the PCI interface of the ATU.
Local processor	Intel XScale® core within the 80333
Core processor	Intel XScale® core within the 80333
Flip Chip	FC-BGA (flip chip-ball grid array) chip packages are designed with core flipped up on the back of the chip, facing away from the PCB. This allows more efficient cooling of the package.
Mode Conversion	Mode Conversions are due to imperfections on the interconnect which transform differential mode voltage to common mode voltage and common mode voltage to differential voltage.
ROMB	Raid on motherboard
ODT	On Die Termination - eliminates the need for termination resistors by placing the termination at the chip.

1.1.2 Other Relevant Documents

1. *Intel® 80333 I/O Processor Specification Update* (305435), Intel Corporation
2. *Intel® 80333 I/O Processor Developer's Manual* (305432), Intel Corporation
3. *Intel® 80333 I/O Processor Datasheet* (305433), Intel Corporation
4. *Intel XScale® 80200 Processor based on Intel® Microarchitecture Developer's Manual* (273411), Intel Corporation
5. *PCI Express Specification*, Revision 1.0a
6. *PCI Express Card Electromechanical Specification 1.0a*
7. *PCI Local Bus Specification*, Revision 2.3 - PCI Special Interest Group
8. *PCI-X Specification*, Revision 1.0b - PCI Special Interest Group
9. *PCI Bus Power Management Interface Specification*, Revision 1.1 - PCI Special Interest Group
10. *IEEE Standard Test Access Port and Boundary-Scan Architecture* (IEEE JTAG-1149.1-1990)
11. *PCI Bus Hot-Plug Specification*, Revision 1.1 - PCI Special Interest Group

1.2 About the Intel® 80333 I/O Processor

The 80333 is a multi-function device that integrates the Intel XScale® core (ARM* architecture compliant) with intelligent peripherals and dual PCI Express-to-PCI Bridges. The 80333 consolidates the following into a single system:

- Intel XScale® core
- x8 PCI Express Upstream Link
- Two PCI Express-to-PCI Bridges supporting PCI-X interface on both segments.
- PCI Standard Hot Plug Controller (segment B)
- Address Translation Unit (PCI-to-Internal Bus Application Bridge) interfaced to the segment A
- High-Performance, Dual-Ported Memory Controller
- Interrupt Controller with up to17 external interrupt inputs
- Two Direct Memory Access (DMA) Controllers
- Application Accelerator with RAID 6 support
- Messaging Unit
- Peripheral Bus Interface Unit
- Two I^2C Bus Interface Units
- Two 16550 compatible UARTs with flow control (four pins)
- Eight General Purpose Input Output (GPIO) ports

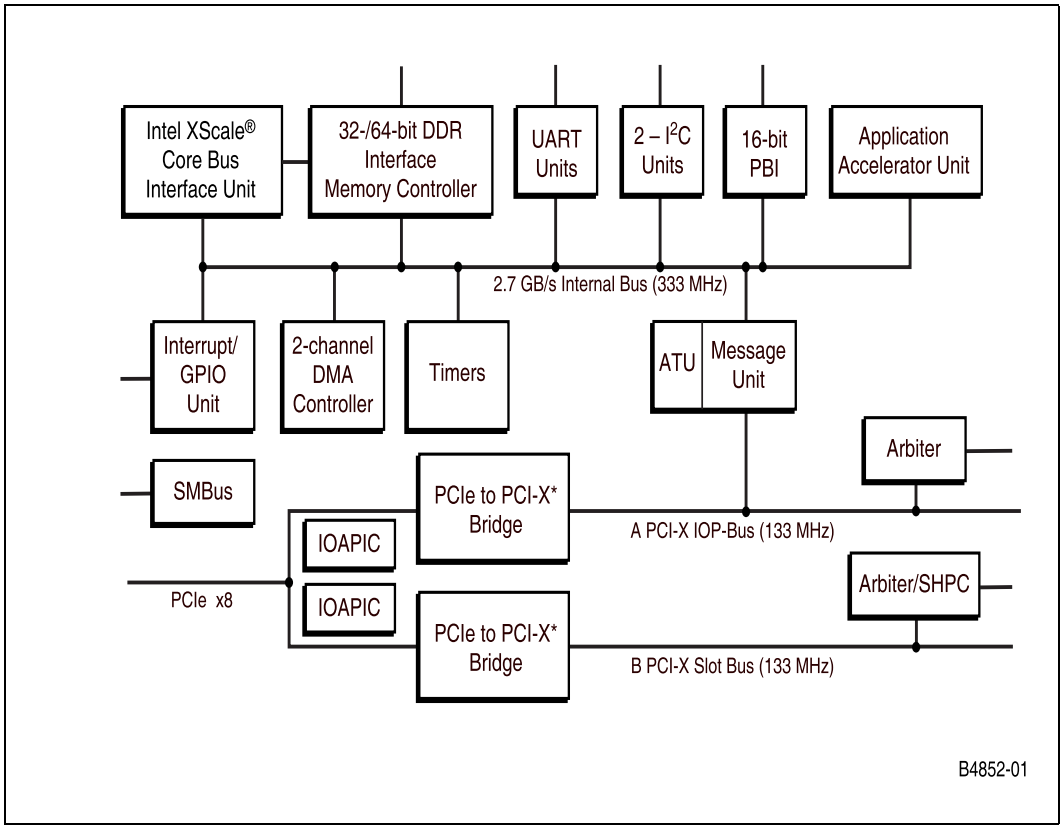
It is an integrated processor that addresses the needs of intelligent I/O applications and helps reduce intelligent I/O system costs.

PCI Express is an industry standard, high performance, low latency system interconnect. The 80333 PCI Express upstream link is capable of x8 lane widths at 2.5 GHz operation as defined by the *PCI Express Specification*, Revision 1.0a. The addition of the Intel XScale® core brings intelligence to the PCI Express-to-PCI Bridges.

The 80333 integrates dual PCI Express-to-PCI Bridges with the ATU as an integrated secondary PCI device. The Upstream PCI Express port implements the PCI-to-PCI Bridge programming model according to the *PCI Express Specification*, Revision 1.0. The Primary Address Translation Unit is compliant with the *PCI-X Specification*, Revision 1.0a definitions of an ‘application bridge’.

Figure 1 provides a block diagram of the 80333.

Figure 1. Intel® 80333 I/O Processor Functional Block Diagram



Package Information 2

The 80333 is offered in a Flip Chip Ball Grid Array (FCBGA) package. This is a full-array package with 829 ball connections. The mechanical dimensions for this package are provided in the Figure 2 and Table 2. Figure 3 and Figure 4 show the 829 pins of the Flip Chip Ball Grid Array (FCBGA), mapped by pin function. This diagram is helpful in placing components around the 80333 for the layout of a PCB. To simplify routing and minimize the number of cross traces, keep this layout in mind when placing components on your board. The signals, by design, are located on the FCBGA package to simplify signal routing and system implementation.

Table 2. FC-style, H-PBGA Package Dimensions

829-Pin BGA		
Symbol	**Minimum**	**Maximum**
A	2.392	2.942
A1	0.50	0.70
A3	0.742	0.872
b	0.61 Ref.	
C	1.15	1.37
D	37.45	37.55
E	37.45	37.55
F1	9.88 Ref.	
F2	10.16 Ref.	
e	1.27 Ref.	
S1	0.97 Ref.	
S2	0.97 Ref.	

NOTE: Measurement in millimeters.

Figure 2. Intel® 80333 I/O Processor 829-Ball FCBGA Package Diagram

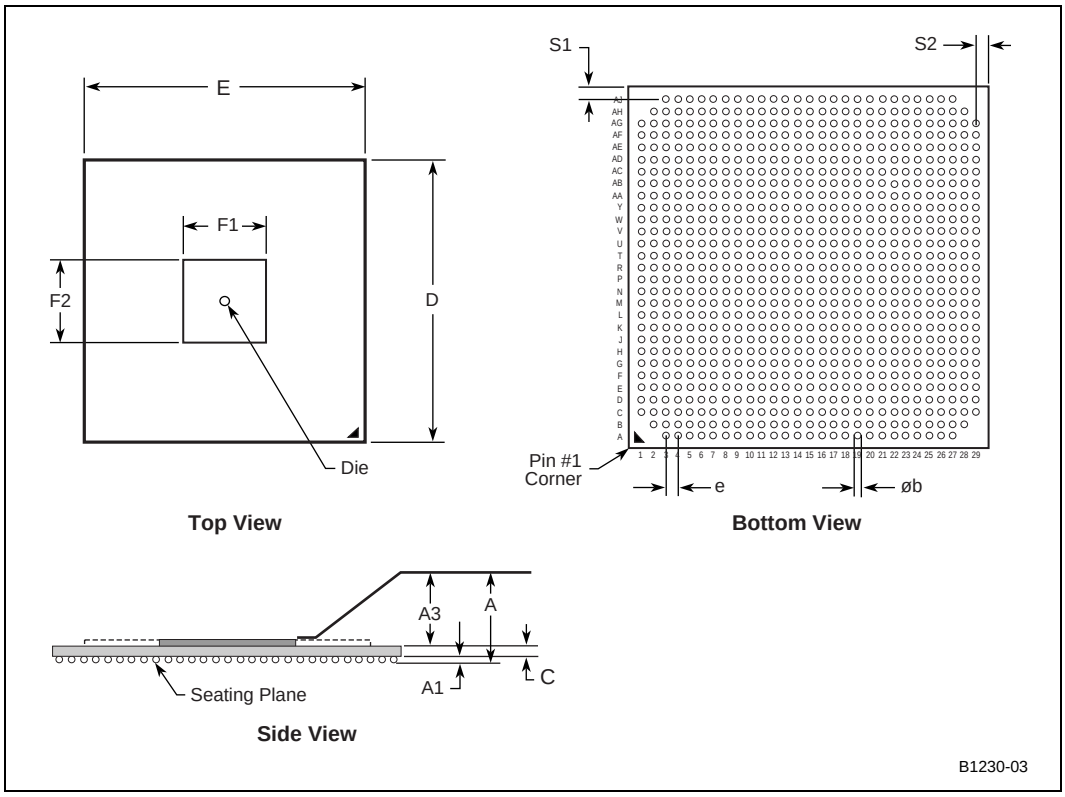


Figure 3. Intel® 80333 I/O Processor Ballout (Top View)

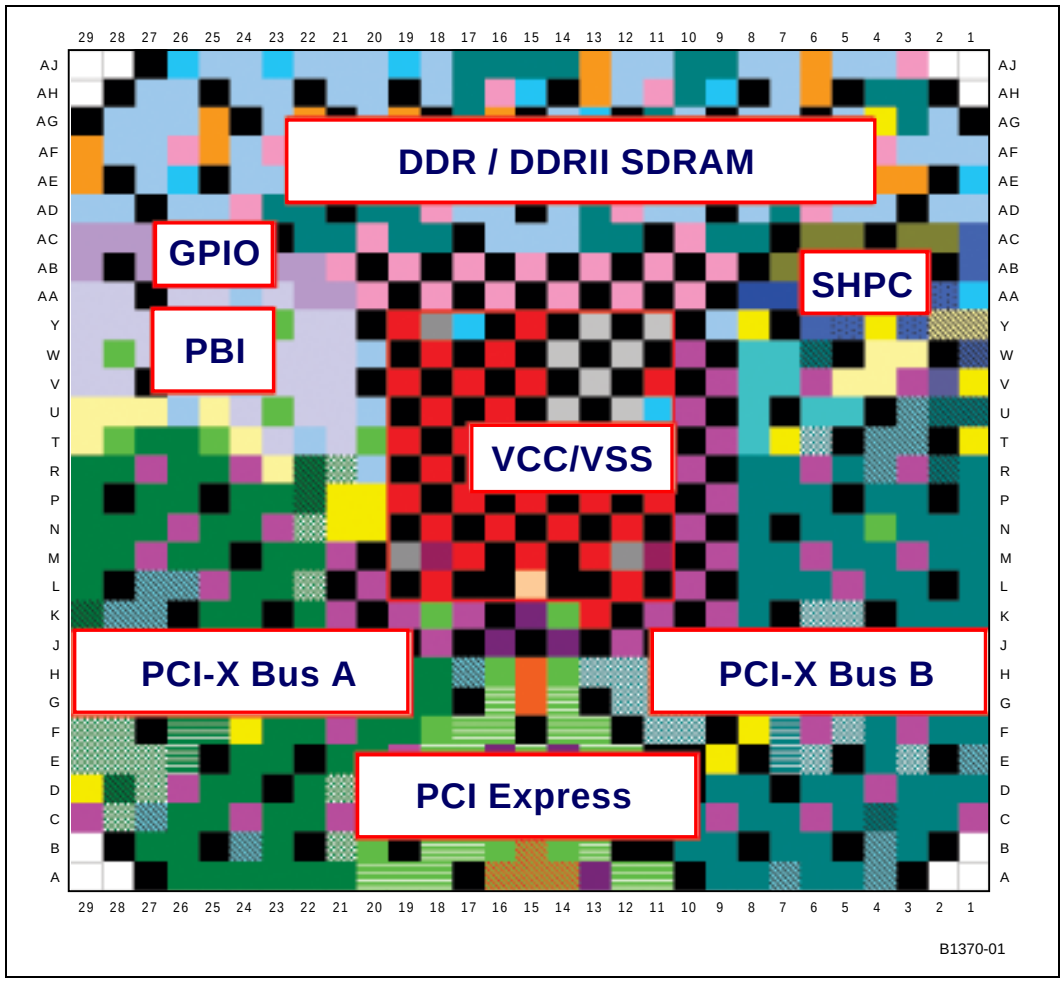
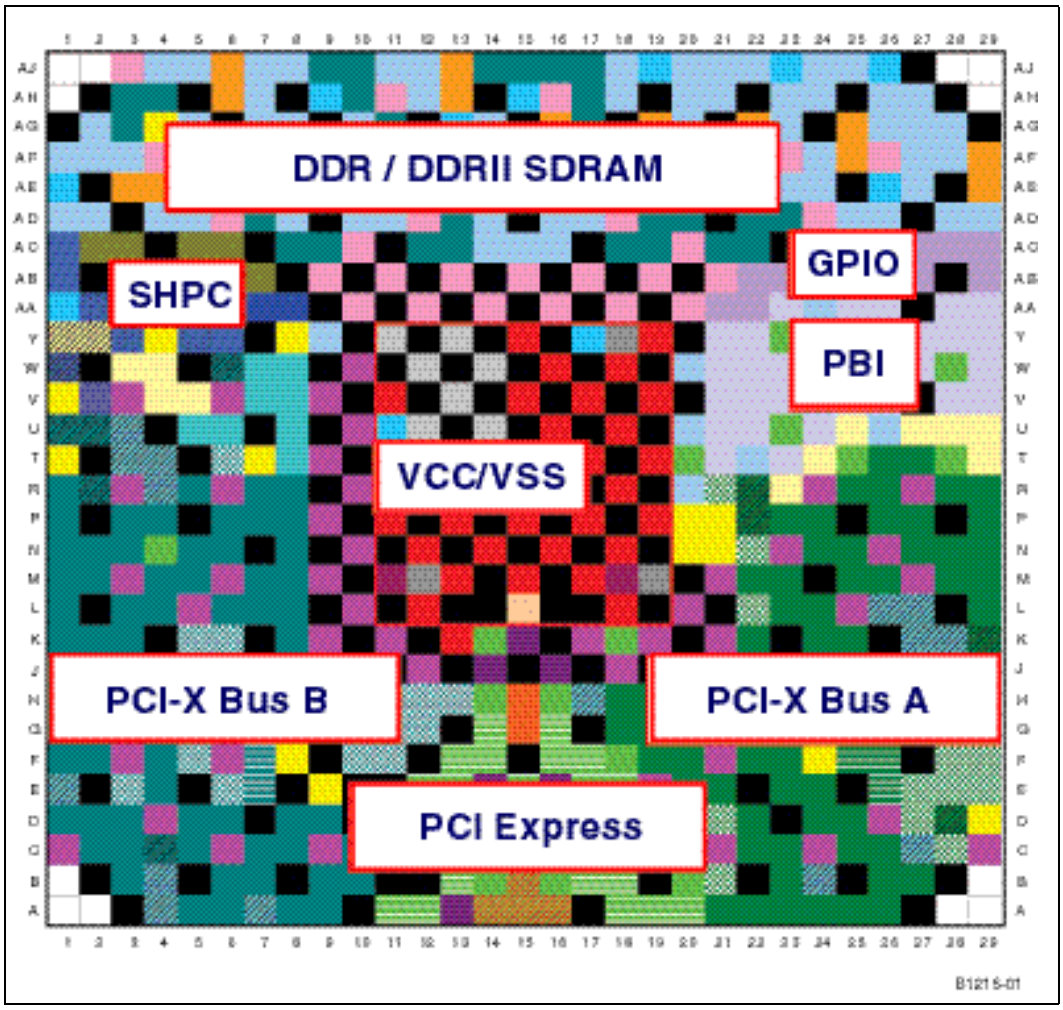


Figure 4. Intel® 80333 I/O Processor Ballout (Bottom View)



2.1 Power Plane Layout

Figure 5 provides the approximate layout of the PCB layers to facilitate the various voltages needed to bias the 80333 package.

Note: The voltage for the PCIX-A bus and PCIX-B bus can be on the same plane.

The 1.5 V PCI-Express interface needs its own voltage regulator (VRM), all to itself. It is allowed no more than 30 mV peak to peak of noise. An alternative is if the core voltage and PCI-Express 1.5V planes are inductively isolated they can share the same regulator. The nominal value of inductance recommended is 2-4 µH as shown in Figure 6.

Figure 5. Intel® 80333 I/O Processor Power Plane Layout

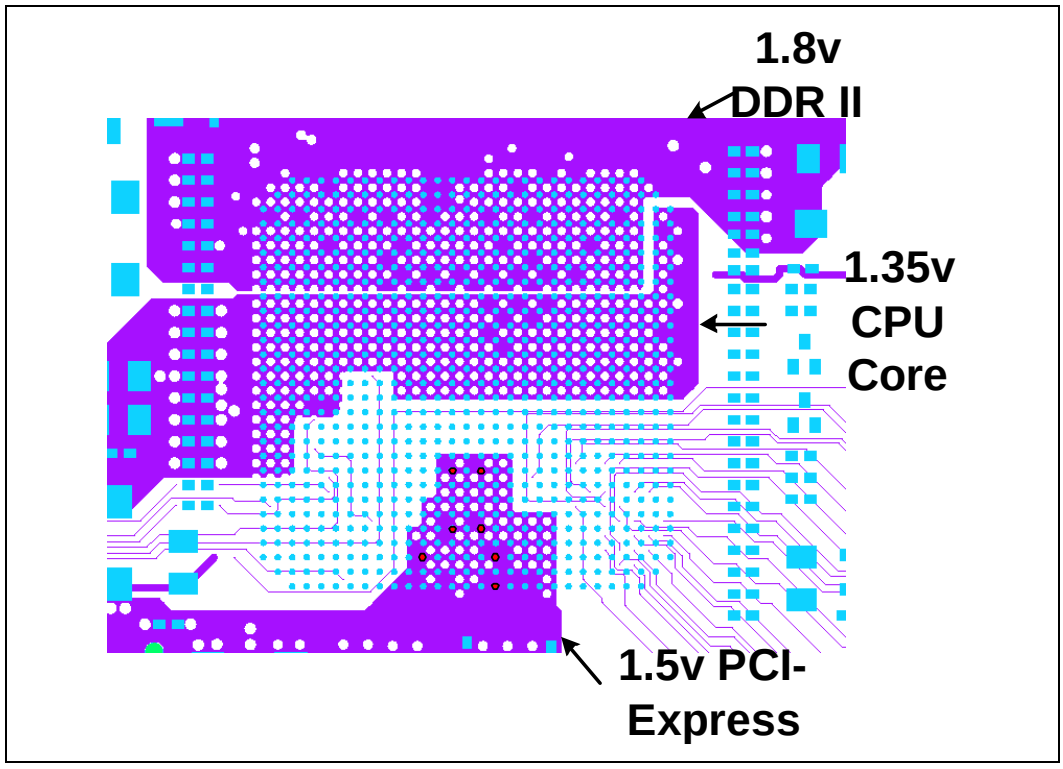
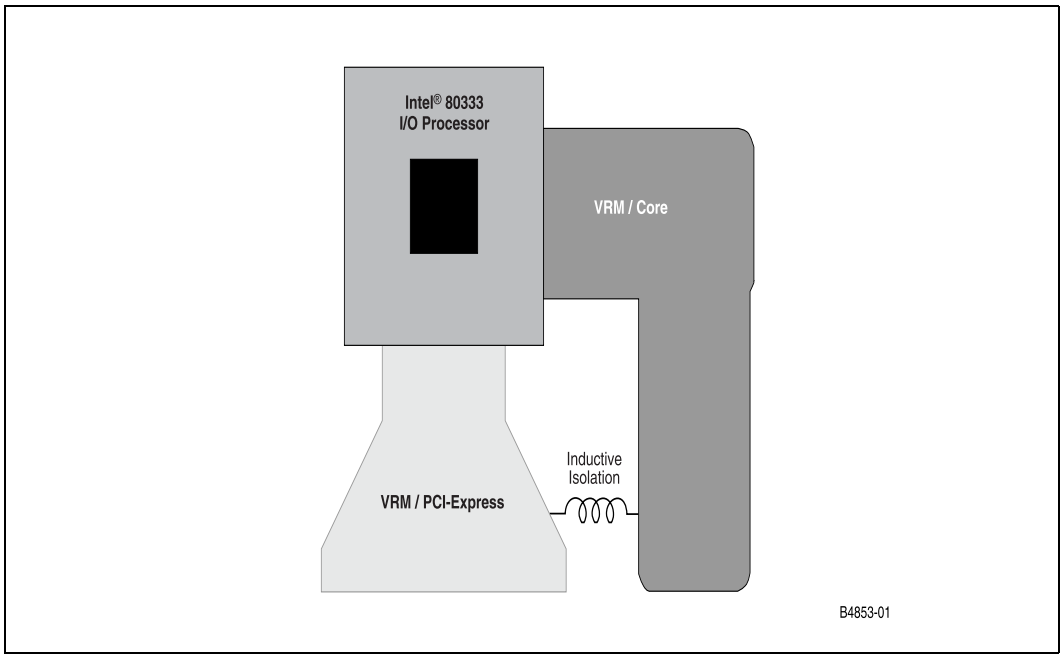


Figure 6. Inductively Isolated Split Plane



2.2 Intel® 80333 I/O Processor Applications

This section provides the block diagrams for 80333 applications. The first consists of a ROMB motherboard application and the second application is a PCI-Express plug-in card application. Figure 7 provides the block diagram of 80333 used in a ROM MCH motherboard application.

Figure 7. Intel® 80333 I/O Processor MCH Motherboard Block Diagram

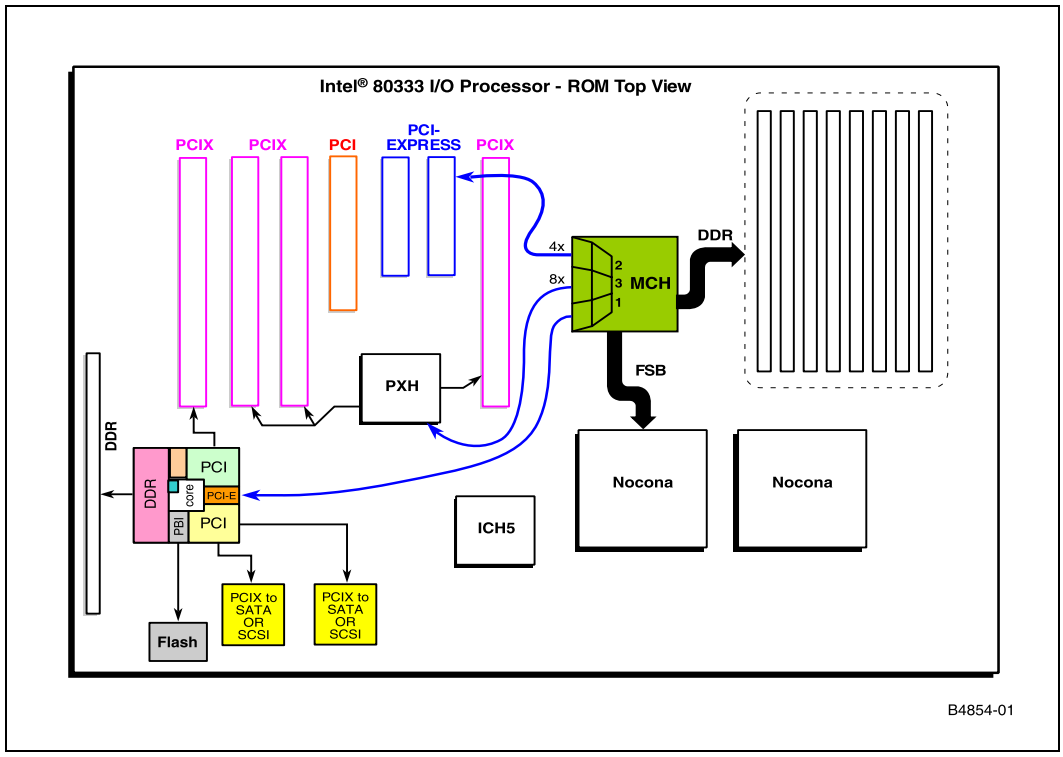
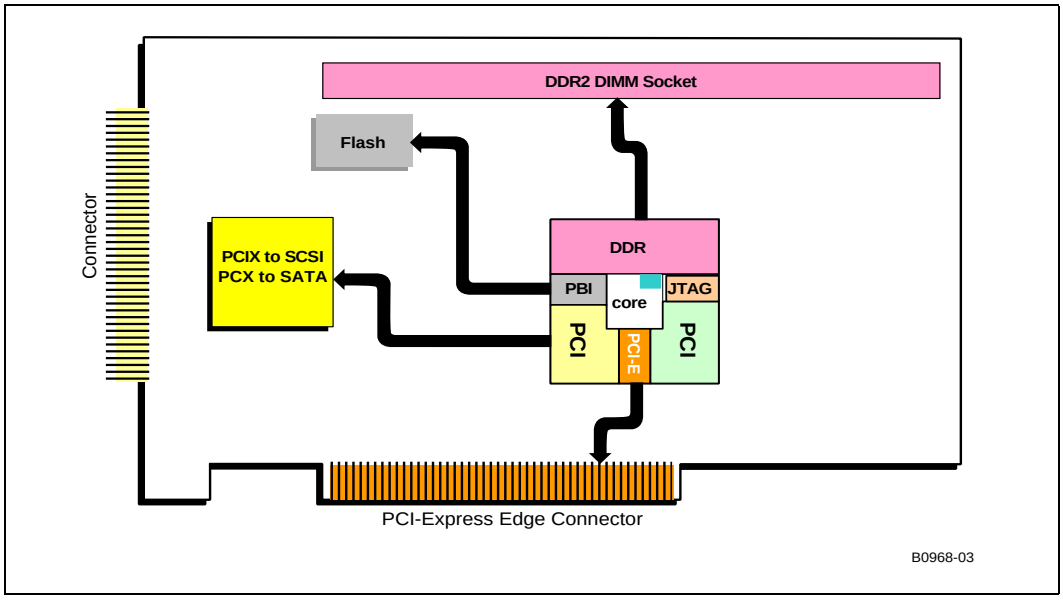


Figure 8 shows 80333 used in a PCI-Express Adapter Card application.

Figure 8. Intel® 80333 I/O Processor PCI-Express Adapter Card Block Diagram



Terminations 3

This chapter provides the recommended pull-up and pull-down terminations for a 80333 layout. Table 3 lists these 80333 termination values. On a motherboard, the *PCI Local Bus Specification*, Revision 2.3 requires that the PCI signals provide the termination resistors. Due to the fact that 80333 is the central resource for both motherboard and add-in card applications, it is required that both the PCI-A bus and PCI-B bus have pull-ups in each of these applications. Pull-ups on the PCI signals are not required with PCIODT_EN = 1 (enabled), because they are implemented on the die. Refer to the Table 3 for more information.

Table 3. Terminations: Pull-up/Pull-down (Sheet 1 of 5)

Signal	Pull-up or Pull-down Resistor Value (in Ohms)	Comments
B_HPWRFLT#	No connect*	**NOTE:** * when Hot Plug is not enabled (internal pull-up is on)
B_HPWREN	No connect	**NOTE:** * when Hot Plug is not enabled (internal pull-up is on)
B_HMRL#	No connect*	**NOTE:** * when Hot Plug is not enabled (internal pull-up is on)
B_HPRSNT2#	No connect*	**NOTE:** * when Hot Plug is not enabled (internal pull-up is on)
B_HPRSNT1#	No connect*	**NOTE:** * when Hot Plug is not enabled (internal pull-up is on)
B_HATNLED#	• If used, connect to amber or yellow LED • Not used -No connect*	Parallel Mode Hot-Plug Attention indicator LED signal that is yellow or amber in color **NOTE:** * when Hot Plug is not enabled (internal pull-up is on) .
B_HPWRLED#	• If used, connect to green LED • Not used - No connect*	Parallel Mode Hot-Plug Power Indicator LED signal that is green in color. **NOTE:** * when Hot Plug is not enabled (internal pull-up is on)
B_HBUTTON#	• If used, connect to Parallel Mode Hot-Plug Attention Button input from the slot. • Not used - No connect*	**NOTE:** * when Hot Plug is not enabled (internal pull-up is on)
B_HRESET#	This output signal is always ‘on’, therefore, it does not tri-state during boundary scan.	

Table 3. Terminations: Pull-up/Pull-down (Sheet 2 of 5)

Signal	Pull-up or Pull-down Resistor Value (in Ohms)	Comments
AD[15:12]/**B_HSLOT[3:0]**	Refer to Comments	Hot plug disabled Hot plug enabled Number of Slots: **B_HSLOT[3:0]** latched on rising (asserting) edge of PWRGD and indicates when the 'B' PCI-X bus interface Standard Hot-Plug Controller is enabled, the total number of slots in both Hot-Plug enabled mode and disabled mode, and the Hot-Plug mode. **B_HSLOT[3]** enables Hot-Plug when high and disables Hot-Plug when low. Hot-Plug disabled / Hot-Plug enabled 0000 = 1 slot / 1000 = reserved 0001 = 2 slots / 1001 = reserved 0010 = 3 slots / 1010 = reserved 0011 = 4 slots / 1011 = reserved 0100 = 5 slots / 1100 = reserved 0101 = 6 slots / 1101 = reserved 0110 = 7 slots / 1110 = reserved 0111 = 8 slots / 1111 = Parallel 1-slot-no-glue **NOTE:** 1111 is Default mode. Muxed onto signal **AD[15:12]** 1 = Requires pull up 8.2K 0 = Requires a pull down 1.5K
PE_RCOMPO	Connect to PE_ICOMPI	Refer to Figure 11
SDTA	For PCI-Express adapter cards: • If the SMBus is used, there should be isolation device such as the LTC4301 between this signal and PE_SMDAT on the PCI Express connector. • If SMBus is unused, a 8.2K pullup is required.	LTC4301 is a hotswappable 2-wire bus buffer that allows card insertion without corruption of the data and clock buses. Refer to the Linear Technology website http://www.linear.com/pdf/4301fa.pdf for more information.
SCLK	For PCI-Express adapter cards: • If the SMBus is used, there should be isolation device such as the LTC4301 between this signal and PE_SMCLK on the PCI Express connector. • If SMBus is unused, a 8.2K pullup is required.	LTC4301 is a hotswappable 2-wire bus buffer that allows card insertion without corruption of the data and clock buses. Refer to the Linear Technology website http://www.linear.com/pdf/4301fa.pdf for more information.
PWRDELAY	If battery backup is implemented: • 1.5 K pull-up to 3.3 V is required on PWRDELAY. Battery Backup not implemented: • This pin can be permanently pulled low with a 1.5K pull-down	

Table 3. Terminations: Pull-up/Pull-down (Sheet 3 of 5)

Signal	Pull-up or Pull-down Resistor Value (in Ohms)	Comments
TRST#	1.5K pull-down*	**NOTES:** • Alternatively tied to **P_RST#** refer to Section 12.4.2, "ARM Multi-ICE" on page 162 for more information about using with a ICE. • When not used this signal is be tied to GND. • This pin has an internal pull-up.
TMS	NC when not being used (has internal pull-up)	
TDI	NC when not being used (has internal pull-up)	
TCK	1.5K pull-down when not used	
GPIO[0]/U0_RXD	8.2 K pull-up	Note: **GPIO[7:0]** initializes as inputs on assertion of **PWRGD**.
GPIO[1]/U0_TXD	8.2 K pull-up	Note: **GPIO[7:0]** initializes as inputs on assertion of **PWRGD**.
GPIO[2]/U0_CTS#	8.2 K pull-up	Note: **GPIO[7:0]** initializes as inputs on assertion of **PWRGD**.
GPIO[3]/U0_RTS#	8.2 K pull-up	Note: **GPIO[7:0]** initializes as inputs on assertion of **PWRGD**.
GPIO[4]/U1_RXD	8.2 K pull-up	Note: **GPIO[7:0]** initializes as inputs on assertion of **PWRGD**.
GPIO[5]/U1_TXD	8.2 K pull-up	Note: **GPIO[7:0]** initializes as inputs on assertion of **PWRGD**.
GPIO[6]/U1_CTS#	8.2 K pull-up	Note: **GPIO[7:0]** initializes as inputs on assertion of **PWRGD**.
GPIO[7]/U1_RTS	8.2 K pull-up	Note: **GPIO[7:0]** initializes as inputs on assertion of **PWRGD**.
A_LOCK#, B_LOCK#	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_SERR#, B_SERR#	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_TRDY#, B_TRDY#	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_PERR#, B_PERR#	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_DEVSEL#, B_DEVSEL#	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_FRAME#, B_FRAME#	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_STOP#, B_STOP#	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_IRDY#, B_IRDY#	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_AD[63:32], B_AD[63:32]	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_C/BE[7:4], B_C/BE[7:4]	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_PAR64, B_PAR64	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_REQ64#, B_REQ64#	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_ACK64#, B_ACK64#	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required.

Table 3. Terminations: Pull-up/Pull-down (Sheet 4 of 5)

Signal	Pull-up or Pull-down Resistor Value (in Ohms)	Comments
A_M66EN, B_M66EN	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed. • When PCIODT_EN = 0, then 8.2 K pull-up is required when operating at 66MHz. This signal is grounded for 33 MHz operation.
A_**RCOMP**	100 ohm +/- 1% to GND	
B_RCOMP	100 ohm +/- 1% to GND	
ACLKIN	Through 33.2ohm resistor to ACLKOUT	
BCLKIN	Through 33.2ohm resistor to BCLKOUT	
B_REQ[3:0]	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_REQ[3:0]	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed • When PCIODT_EN = 0, then 8.2 K pull-up is required.
A_PCIXCAP, B_PCIXCAP	3.3 K Pull-up	
A_PCIX133EN	1.5 K pull-down when needed (refer to comments)	PCI Bus Segment 'A' 133 MHz Enable: A_PCIX133EN is latched on the rising (asserting) edge of PWRGD and it determines the maximum PCI-X mode operating frequency. 0 = 100 MHz enabled (Requires pull down resistor). 1 = 133 MHz enabled (Default mode). Muxed onto signal **AD[3]**
B_PCIX133EN	1.5 K pull-down when needed (refer to comments)	PCI Bus Segment 'B' 133 MHz Enable: **B_PCIX133EN** latched on rising (asserting) edge of PWRGD and determines maximum PCI-X mode operating frequency. 0 = 100 MHz enabled (Requires pull down resistor.) 1 = 133 MHz enabled (Default mode) Muxed onto signal **AD[10]**
PCIODT_EN	1.5 K pull-down when needed (see comments)	PCI Bus ODT Enable: is latched on the rising (deasserting) edge of P_RST#, and determines when the PCI-X interface has On Die Termination enabled valid on the secondary PCI bus only. • 0 = ODT disabled on the secondary PCI bus. (Requires pull-down resistor). • 1 = ODT enabled on the secondary PCI bus. (Default mode). This signal controls termination for the following signals: B_AD[63:32], B_C/BE[7:4]#, B_PAR64, B_REQ64#, B_REQ[4:0]#, B_ACK64#, B_FRAME#, B_IRDY#, B_DEVSEL#, B_TRDY#, B_STOP#, B_PERR#, B_LOCK#, B_M66EN, B_SERR# A_AD[63:32], A_C/BE[7:4]#, A_PAR64, A_REQ64#, A_REQ[3:0]#, A_ACK64#, A_FRAME#, A_IRDY#, A_DEVSEL#, A_TRDY#, A_STOP#, A_PERR#, A_LOCK#, A_M66EN, A_SERR# and XINT[7:0]# NOTE: This signal is muxed onto signal A[20].
M_CK[2:0], M_CK[2:0]#	Refer to comments	For M_CKs and M_CK#s not used leave these pins unconnected.
DQS[8:0]#	Refer to Comments	When not in DDRII mode these signals are NC's
DDRRES[2:1]	• Refer to Figure 12 for the recommended termination for DDRII mode. • When not in DDRII mode these signals have a 1.0 K pull-down.	
RSTIN#	1K Pull-up	

Table 3. Terminations: Pull-up/Pull-down (Sheet 5 of 5)

Signal	Pull-up or Pull-down Resistor Value (in Ohms)	Comments
XINT[3:0]#	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed • When PCIODT_EN = 0, then 8.2 K pull-up is required.
XINT[7:4]#	Refer to comments	• When PCIODT_EN = 1 no external pull-up needed • When PCIODT_EN = 0, then 8.2 K pull-up is required.
HPI#	8.2 K pull-up	
P_BOOT16#	1.5 K pull-down when needed (refer to comments)	Bus Width is latched on the rising (asserting) edge of PWRGD, it sets the default bus width for the PBI Memory Boot window: • 0 = 16 bits wide (Requires a pull-down resistor.) • 1 = 8 bits wide (Default mode) Muxed onto signal **AD[4]**.
MEM_TYPE	1.5 K pull-down when needed (refer to comments)	Memory Type: **MEM_TYPE** is latched on the rising (asserting) edge of PWRGD and it defines the speed of the DDR SDRAM interface. 0 = DDR-II SDRAM at 400 MHz (Required pull-down resistor.) 1 = DDR SDRAM at 333 MHz (Default mode) Muxed onto signal **AD[2]**
RETRY	1.5 K pull-down when needed (refer to comments)	Configuration Retry Mode: **RETRY** is latched on the rising (asserting) edge of**PWRGD** and determines when PCI interface of the ATU disables PCI configuration cycles by signaling a retry until the configuration cycle retry bit is cleared in the PCI configuration and status registerRETRY also controls the behavior of the upstream PCI Express for configuration transactions. 0 = Configuration Cycles enabled (Requires pull down resistor.) 1 = Configuration Retry enabled in the ATU and the Configuration Retry Status response is enabled in the Upstream PCI Express interface. (Default mode) Muxed onto signal **AD[6]**
SMB_MA5 SMB_MA3 SMB_MA2 SMB_MA1	1.5 K pull-down when needed (refer to comments)	Manageability Address (MA): latched on rising (asserting) edge of PWRGD and maps to MA bit 5, 3, 2, and 1, where MA bits 7- 0 represent the address the SMBus slave port responds to when access is attempted. 0 = (Requires pull down resistor.) 1 = (Default mode) Muxed onto signal **A[19:16]**
PD1	1.5 K pull-down	Muxed onto signal AD[7]
CORE_RST#	1.5 K pull-down when needed (refer to comments)	Core Reset Mode is latched on the rising (asserting) edge of PWRGD and determines when the Intel® XScale™ core is held in reset until the processor reset bit is cleared in PCI configuration and status register. 0 = Hold in reset. (Requires pull-down resistor.) 1 = Do not hold in reset. (Default mode) Muxed onto signal **AD[5]**
DDRSLWCRES	Refer to Figure 13	
DDRIMPCRES	Refer to Figure 13	
ODT[1:0]	Connect to ODT on DIMM terminated with 49.9 ohm resistor to VTT	When not used this pin is left as a “no connect”.

1. PCIXCAP - The maximum trace length between the resistor (when installed), capacitor, and the connector contact is 0.25 inches. The maximum trace length between the resistor (when installed), capacitor, and ground is 0.1 inches. A PCI-X card is not permitted to connect **PCIXCAP** to anything else including supply voltages and device input and output pins.

3.1 Analog Filters

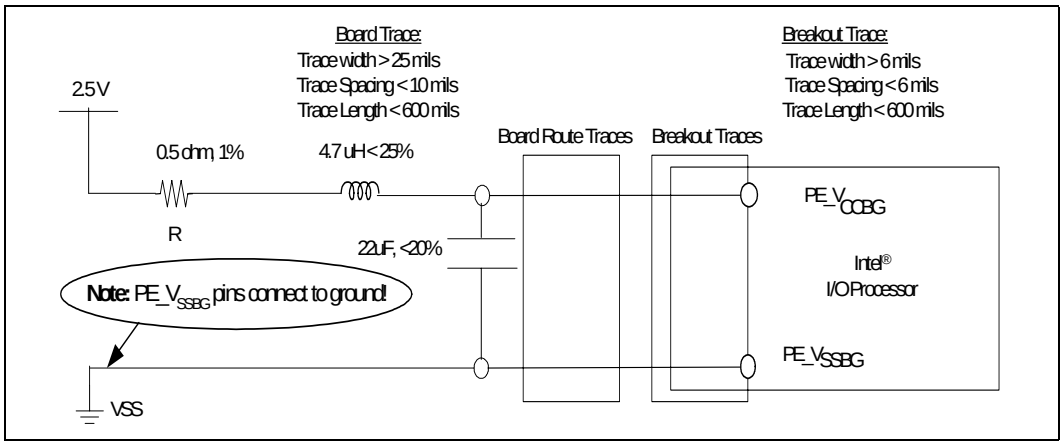
The following section describes filters needed for biasing PCI-Express Bandgap and PLL circuitry.

3.2 PE_V_{CCBG} Pin Requirements

The PCI Express resistor compensation circuit uses a band gap reference circuit that requires 2.5 V on PE_VCCBG. The lowpass filter for this pin is shown in Figure 9. The following notes list the layout guidelines for this filter.

- 4.7 µH (Inductor)
  - — the inductor must be magnetically shielded
  - — ESR: max < 0.4 W
  - — 30 mA for bandgap circuit only
  - — An example of this inductor is TDK part number MLZ2012E4R7P.
- 22 µF (Capacitor)
  - — ESR: maximum < 0.4Ω
  - — ESL < 3.0 nH
  - — Place 22 µF capacitor as close as possible to package pin.
- 0.5 ohm, 1% (Resistor)
  - — 1/16W 6.3 V
  - — 0.5 ohm, 1% resistor must be placed between V_{CC} and L. The resistor rating is 1/16W.
- Route PE_V_{CCBG} and PE_V_{SSBG} as differential traces.
- PE_VSSBG is routed to ground at the capacitor filter only.
- PE_V_{CCBG} and PE_V_{SSBG} traces must be ground referenced (No V_{CC} references).
- Max total board trace length = 1.2”.
- Min trace space to other nets = 30 mils.
- The 2.5 V supply regulator used for the bandgap filter must have < 3% tolerance. The ICC maximum current draw on this supply is 600 µA.

Figure 9. V_{CCBG} Filter Circuit



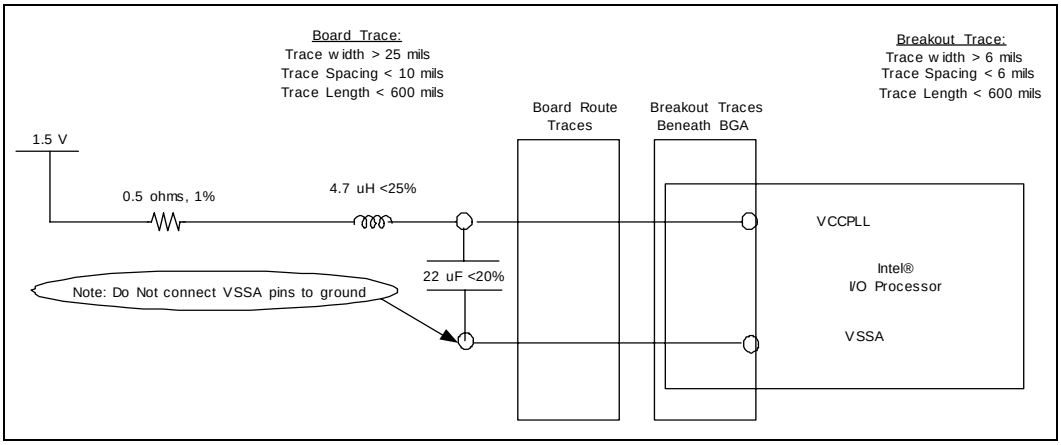
3.2.1 V_{CCPLL} Pin Requirements

To reduce clock skew, the **V_{CCPLL}** balls for the Phase Lock Loop (PLL) circuit are isolated on the package. The lowpass filter, as shown in Figure 10 reduces noise induced clock jitter and its effects on timing relationships in system designs. The node connecting V_{CCPLL} and the capacitor must be as short as possible. The Figure 10 filter circuit is recommended for each of the five PLL pairs: V_{CCPLL1} - V_{SSA1}, V_{CCPLL2} - V_{SSA2}, V_{CCPLL3} - V_{SSA3}, V_{CCPLL4} - V_{SSA4} and V_{CCPLL5} - V_{SSA5} pairs.

The following notes list the layout guidelines for this filter.

- 4.7 µH (Inductor)
  - — L must be magnetically shielded
  - — ESR: max < 0.4Ω
  - — rated at 45mA
  - — An example of this inductor is TDK part number MLZ2012E4R7P.
- 22 µF (Capacitor)
  - — ESR: max < 0.4Ω
  - — ESL < 3.0nH
  - — Place 22 µF capacitor as close as possible to package pin.
- 0.5 ohm 1% (Resistor)
  - — 1/16W 6.3V
- 0.5 ohm 1% resistor must be placed between V_{CC} and L. The resistor rating is 1/16W.
- Route V_{CCPLL}[1-5] and V_{SSA}[1-5] as differential traces.
- V_{CCPLL}[1-5] and V_{SSA}[1-5] traces must be ground referenced (No V_{CC} references).
- Maximum total board trace length = 1.2”.
- Minimum trace space to other nets = 30 mils.
- The 1.5 V supply regulator used for the PLL filter must have less than +/- 3% tolerance.
- **Note:** V_{SSA}[1-5] pins must **not** be connected to ground.

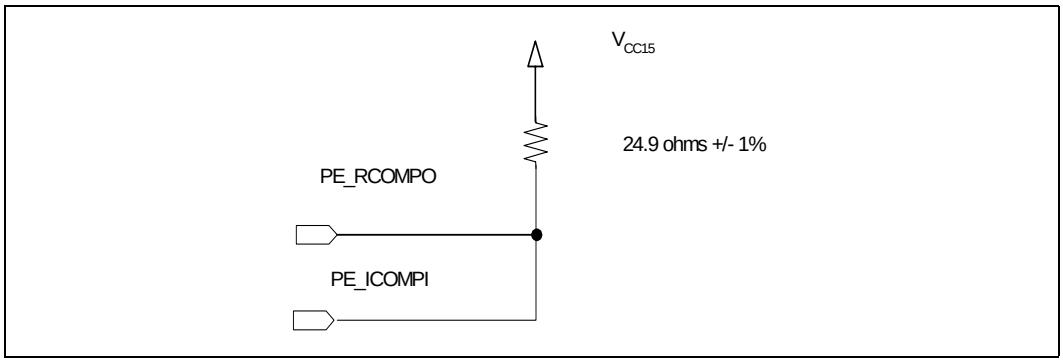
Figure 10. V_{CCPLL} Configuration



3.3 PCI-Express Resistor Compensation

Figure 11 shows the termination required for the PCI Express RCOMP circuit..

Figure 11. PCI-Express RCOMP

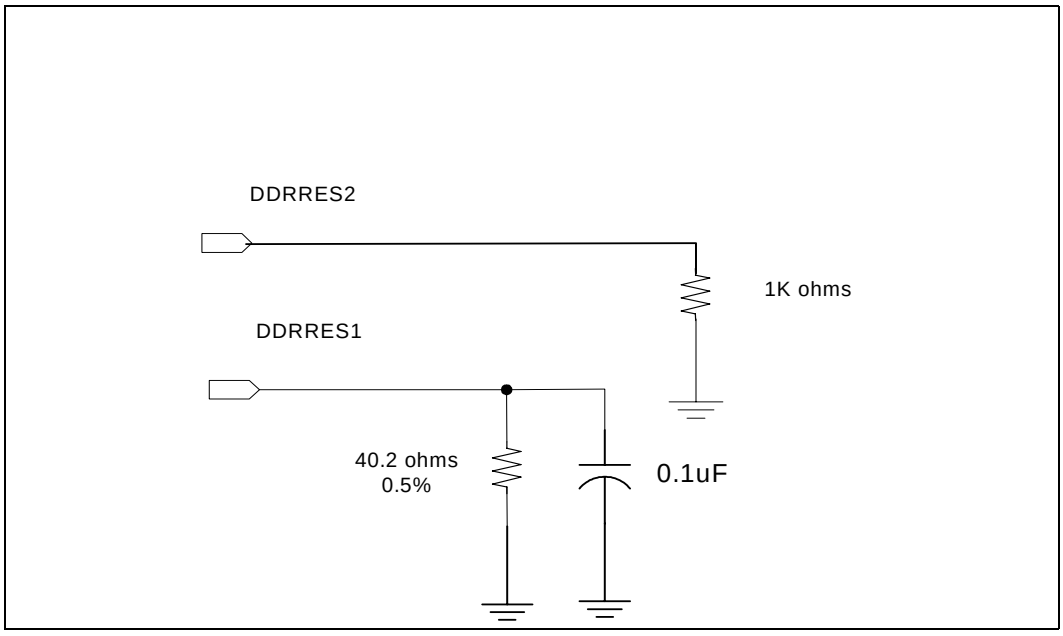


3.4 DDR Resistor Compensation

The Figure 12 provides the 80333 DDR II DDRES circuitry. The DDRRES1 resistor has a tight tolerance of 40.2 ohm 0.5%. DDRRES2 is used as compensation for DDR-II OCD. Due to the fact that OCD is not supported this pin should be pulled to GND with a 1K resistor.

Note: when not in DDR II mode these pins must have a 1.0 K pull-down to GND.

Figure 12. Intel® 80333 I/O Processor DDRRES Resistor Compensation Circuitry



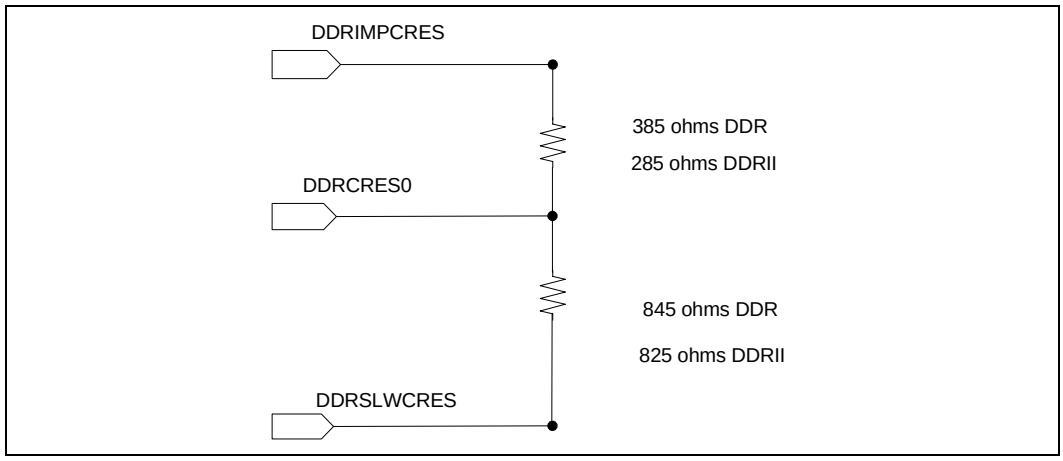
3.5 DDR Driver Compensation

External reference resistors are used to control slew rate and driver impedance. The DDRIMPCRES (or DDRDRVCRES) resistor directly controls the on-die termination (ODT). The recommendations are as follows:

- DDRIMPCRES: controls on-die termination, DDR - 385 ohms, DDRII - 285 ohms. Note that the closest standard 1% resistors are acceptable.
- DDRSLWRCRES: controls slew rate and driver impedance, DDR 845 ohms, DDRII 825 ohms.

With these values the ODT is 150/75 ohms for DDRII and 200/100 ohms for DDR.

Figure 13. DDR Driver Compensation Circuitry



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Routing Guidelines 4

This chapter provides some basic routing guidelines for layout and design of a printed circuit board using 80333. The high-speed clocking required when designing with the 80333 requires special attention to signal integrity. In fact, it is highly recommended that the board design be simulated to determine optimum layout for signal integrity. The information in this chapter provides guidelines to aid the designer with board layout. Several factors influence the signal integrity of a 80333 design. These factors include:

- Power distribution
- Minimizing crosstalk
- Decoupling
- Layout considerations when routing the DDR memory, DDR II memory,PCI Express bus and PCI-X bus interfaces

4.1 General Routing Guidelines

This section details general routing guidelines for designing with 80333. The order in which signals are routed varies from designer to designer. Some designers prefer to route all clock signals first, while others prefer to route all high-speed bus signals first. Either order can be used, provided the guidelines listed here are followed.

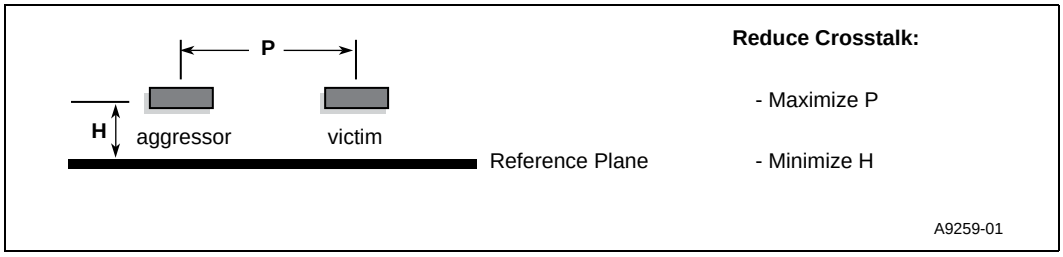
4.2 Crosstalk

Crosstalk is caused by capacitive and inductive coupling between signals. Crosstalk is composed of both backward and forward crosstalk components. Backward crosstalk creates an induced signal on victim network that propagates in the opposite direction of the aggressor signal. Forward crosstalk creates a signal that propagates in the same direction as the aggressor signal.

Circuit board analysis software is used to analyze your board layout for crosstalk problems. Examples of 2D analysis tools include Parasitic Parameters from **ANSOFT*** and XFS from **Quad Design***. Crosstalk problems occur when circuit etch lines run in parallel. When board analysis software is not available, the layout needs to be designed to maintain at least the minimum recommended spacing for bus interfaces.

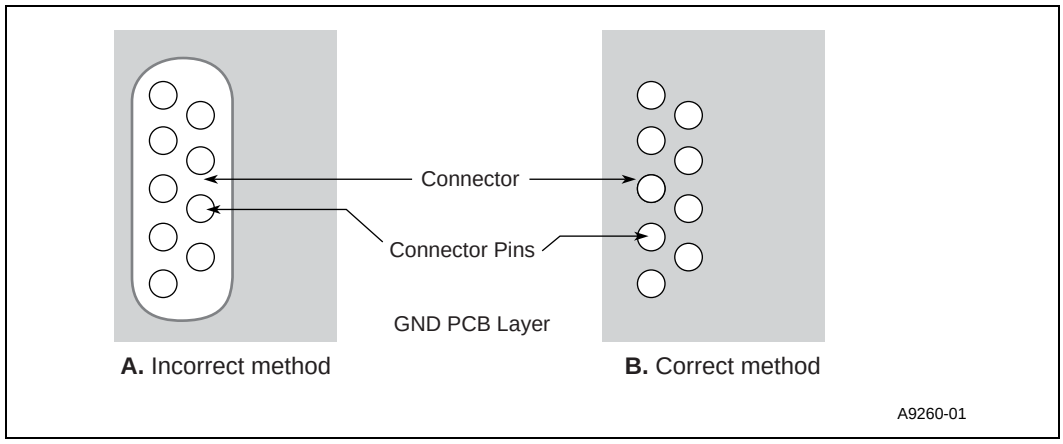
- A general guideline to use is, that space distance between adjacent signals be a least 3.3 times the distance from signal trace to the nearest return plane. The coupled noise between adjacent traces decreases by the square of the distance between the adjacent traces.
- It is also recommended to specify the height of the above reference plane when laying out traces and provide this parameter to the PCB manufacturer. By moving traces closer to the nearest reference plane, the coupled noise decreases by the square of the distance to the reference plane.

Figure 14. Crosstalk Effects on Trace Distance and Height



- Avoid slots in the ground plane. Slots increases mutual inductance thus increasing crosstalk.
- Throughout the design guide unbroken GND reference planes are recommended. If it is not possible to route over an unbroken ground plane then an unbroken power plane is acceptable. If it is necessary to use power plane referencing, it is better to reference the power plane used by the I/O connector (if applicable). It is also recommended to add decoupling to the connector near the pins.
- Make sure that ground plane surrounding connector pin fields are not completely cleared out. When this area is completely cleared out, around the connector pins, all the return current must flow together around the pin field increasing crosstalk. The preferred method of laying out a connector in the GND layer is shown in Figure 15.

Figure 15. PCB Ground Layout Around Connectors



4.3 EMI Considerations

It is highly recommended that good EMI design practices be followed when designing with the 80333.

- To minimize EMI on your PCB a useful technique is to not extend the power planes to the edge of the board.
- Another technique is to surround the perimeter of your PCB layers with a GND trace. This helps to shield the PCB with grounds minimizing radiation.

The below link can provide some useful general EMI guidelines considerations:

http://developer.intel.com/design/auto/mcs96/applnots/272673.htm

4.4 Power Distribution and Decoupling

Have ample decoupling to ground, for the power planes, to minimize the effects of the switching currents. Three types of decoupling are: the bulk, the high-frequency ceramic, and the inter-plane capacitors.

- Bulk capacitance consist of electrolytic or tantalum capacitors. These capacitors supply large reservoirs of charge, but they are useful only at lower frequencies due to lead inductance effects. The bulk capacitors can be located anywhere on the board.
- For fast switching currents, high-frequency low-inductance capacitors are most effective. Place these capacitors as close to the device being decoupled as possible. This minimizes the parasitic resistance and inductance associated with board traces and vias.
- Use an inter-plane capacitor between power and ground planes to reduce the effective plane impedance at high frequencies. The general guideline for placing capacitors is to place high-frequency ceramic capacitors as close as possible to the module.

4.4.1 Decoupling

Inadequate high-frequency decoupling results in intermittent and unreliable behavior.

A general guideline recommends that you use the largest easily available capacitor in the lowest inductance package. The high speed decoupling capacitor should be placed as close to the pin as possible with short, wide trace.

Table 4 provides the details on the recommended decoupling capacitors for each of the voltage planes.

Table 4. Decoupling Recommendations

Voltage Plane	Voltage	Pins	Package	C (µF)	Number of Caps
PCI/PCI-X	3.3V	VCC33	1210	22	3
PCI/PCI-X	3.3V	VCC33	0603	0.1	12
PCI/PCI-X	3.3V	VCC33	7343	150	1
DDR/DDRII	2.5/1.8V	VCC25/18	0603	0.1	14

Table 4. Decoupling Recommendations

Voltage Plane	Voltage	Pins	Package	C (µF)	Number of Caps
DDR/DDRII	2.5/1.8V	VCC25/18	1210	22	2
DDR/DDRII	2.5/1.8V	VCC25/18	7343	150	1
Core	1.5V	VCC15	0603	0.1	17
Core	1.5V	VCC15	1210	22	2
PCI Express	1.5V	VCC15E	0603	0.1	6
PCI Express	1.5V	VCC15E	1210	22	1
CPU	1.35V	VCC13	0603	0.1	6
CPU	1.35V	VCC13	1206	10	1
CPU	1.35V	VCC13	1210	22	1

NOTES:
1. Polymerized organic capacitors recommended for bulk decoupling.
2. X5R, X7R or COG dielectric recommended for ceramic capacitors.

4.5 Trace Impedance

All signal layers require controlled impedance of 50 Ω +/- 15%, microstrip or stripline where appropriate for motherboard applications and 60 Ω +/- 15%, microstrip or stripline, for add-in card applications. Selecting the appropriate board stack-up to minimize impedance variations is very important. When calculating flight times, it is important to consider the minimum and maximum trace impedance based on the switching neighboring traces. Use wider spaces between traces, since this can minimize trace-to-trace coupling, and reduce cross talk.

When a different stack up is used the trace widths must be adjusted appropriately. When wider traces are used, the trace spacing must be adjusted accordingly (linearly).

It is highly recommended that a 2D Field Solver be used to design the high-speed traces. The following Impedance Calculator URL provide approximations for the trace impedance of various topologies. They may be used to generate the starting point for a full 2D Field solver.

http://emclab.umr.edu/pcbtlc/

The following website link provides a useful basic guideline for calculating trace parameters:

http://www.ultracad.com/calc.htm

Note: Using stripline transmission lines may give better results than microstrip. This is due to the difficulty of precisely controlling the dielectric constant of the solder mask, and the difficulty in limiting the plated thickness of microstrip conductors, which can substantially increase cross-talk.

Board Layout Guidelines 5

This section provides details on the motherboard and adapter card stackup suggestions. It is highly recommended that signal integrity simulations be run to verify each 80333 PCB layout especially when it deviates from the recommendations listed in these design guidelines. The information in this chapter is an example of a stackup for a motherboard and an adapter card which can be used as a reference.

5.1 Motherboard Stack Up Information

When 80333 is used in server and workstation Raid On Mother Board (ROMB) applications the motherboard is implemented on eight layers. The specified impedance range for all board implementations are 50 ohms +/-15%. Adjustments are made for interfaces specified at other impedances. Table 5 defines the typical layer geometries for six or eight layer boards.

The motherboard is supporting other components in addition to 80333, so it is assumed that server/workstation motherboard requirements dominates to assure the processor and memory subsystem can be implemented with typical 50-ohm guidelines. Dimensions and tolerances for the motherboard are per Table 5. Refer to Figure 16 for location of variables in Table 5.

Table 5. Motherboard Stack Up, Stripline and Microstrip (Sheet 1 of 2)

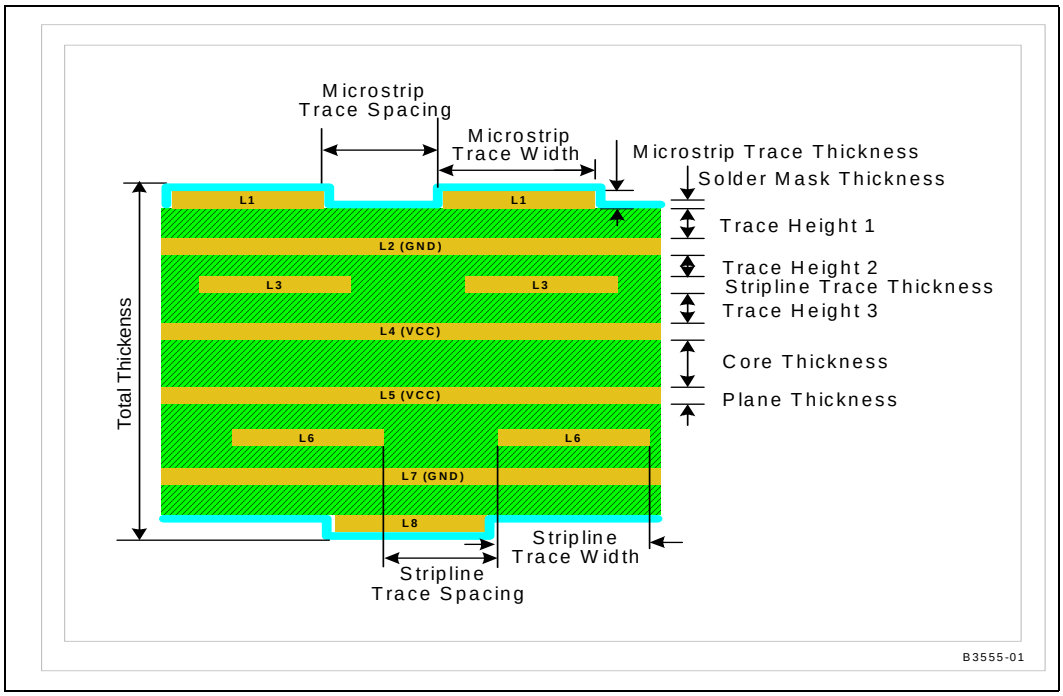
Variable	Type	Nominal (mils)	Minimum (mils)	Maximum (mils)	Notes
Solder Mask Thickness (mil)	N/A	0.8	0.6	1.0	The trace height is determined to achieve a nominal 50 ohms.
Solder Mask E_r	N/A	3.65	3.65	3.65	
Core Thickness (mil)	N/A	9.8	9.6	10	
Core E_r	N/A	4.30	3.75	4.85	2113 material.
Plane Thickness (mil)	Power	2.7	2.5	2.9	
	Ground	1.35	1.15	1.55	
Trace Height (mil)	1	3.5	3.3	3.7	
	2	3.5	3.3	3.7	
	3	10.5	9.9	11.1	
Preg E_r	Microstrip	4.30	3.75	4.85	2113 material.
	Stripline1	4.30	3.75	4.85	2113 material.
	Stripline2	4.66	4.19	5.13	7628 material. Trace height 3 is composed of one piece of 2113 and one piece of 7628. It is assumed that the 7628 material covers the bottom and sides of the layer 3 traces as well as the top and sides of the layer 4 traces. The 2113 material covers the top of the layer three traces and the bottom of the layer 4 traces.
Trace Thickness (mil)	Microstrip	1.75	1.2	2.3	
	Stripline	1.4	1.2	1.6	
Trace Width (mil)	Microstrip	5.0	3.5	6.5	

Table 5. Motherboard Stack Up, Stripline and Microstrip (Sheet 2 of 2)

Variable	Type	Nominal (mils)	Minimum (mils)	Maximum (mils)	Notes
	Stripline	4.0	2.5	5.5	
Trace Spacing (mil)	Microstrip	15.0	-	-	Each interface sets the trace spacing based on its signal integrity of differential impedance requirements. For the purposes of the building the transmission line models, it is assumed the artwork is very accurate and therefore a constant. Thus, all the variability in the trace spacing is the result of the tolerances of the trace width.
	Stripline	12.0	-	-	
Total Thickness (mil)	FR4	62.0	56.0	68.0	
Trace Velocity (ps/in)	Microstrip	-	135	141	Velocity varies based on variation in Er. It cannot be controlled during the fab process.
	Stripline		167	178	
Trace Impedance (ohms)	Microstrip	50	42.5	57.5	
	Stripline	50	45	55	

NOTE: Each interface sets the trace spacing based on its signal integrity of differential impedance requirements. For the purposes of the building the transmission line models, it is assumed the artwork is very accurate and therefore a constant. Thus, all the variability in the trace spacing is the result of the tolerances of the trace width.

Figure 16. Motherboard Stackup Recommendations



5.2 Adapter Card Stackup

The 80333 can be implemented onPCI-E adapter cards with six or eight layer stackups. The specified impedance range for all adapter card implementations are 60ohms +/-15%. Adjustments are made for interfaces specified at other impedances. Table 6 defines the typical layer geometries for six or eight layer boards.

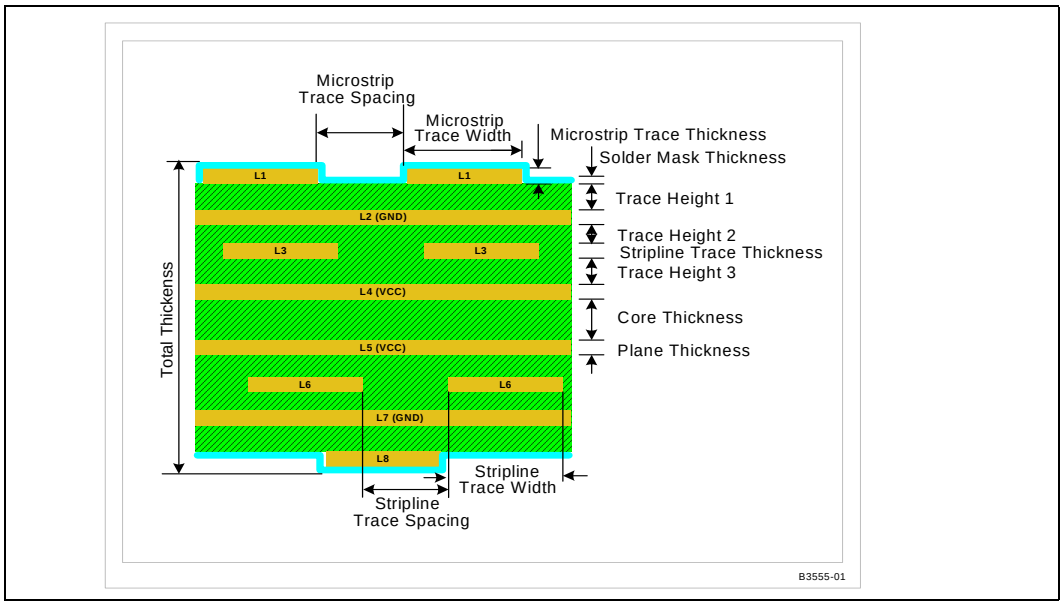
Note: Values are the same as the motherboard stack up with the exception of the impedance.

Table 6. Adapter Card Stack Up, Microstrip and Stripline

Variable	Type	Nominal (mils)	Minimum (mils)	Maximum (mils)	Notes
Solder Mask Thickness (mil)	N/A	0.8	0.6	1.0	
Solder Mask E_r	N/A	3.65	3.65	3.65	
Core Thickness (mil)	N/A	2.8	3.0	3.2	
Core E_r	N/A	4.3	3.75	4.85	2113 material
Plane Thickness (mil)	Power	2.7	2.5	2.9	
	Ground	1.35	1.15	1.55	
Trace Height (mil)	1	3.5	3.3	3.7	The trace height is determined to achieve a nominal 60 ohms.
	2	3.5	3.3	3.7	
	3	10.5	9.9	11.1	
Preg E_r	Microstrip	4.30	3.75	4.85	2113 material
	Stripline1	4.30	3.75	4.85	2113 material
	Stripline2	4.3	3.75	4.85	7628 material. Trace height 3 is composed of one piece of 2113 and one piece of 7628.
Trace Thickness (mil)	Microstrip	1.75	1.2	2.3	
	Stripline	1.4	1.2	1.6	
Trace Width (mil)	Microstrip	4.0	2.5	5.5	
	Stripline	4.0	2.5	5.5	
Total Thickness (mil)	FR4	62.0	56.0	68.0	
Trace Spacing (using microstrip E2E/C2C)	[12]/[16]				
Trace Spacing (using stripline E2E/C2C)	[12]/[16]				
Trace Impedance	Microstrip	60	51	69	
	Stripline	60	51	69	

NOTE: Each interface sets the trace spacing based on its signal integrity of differential impedance requirements. For the purposes of the building the transmission line models, it is assumed the artwork is very accurate and therefore a constant. Thus, all the variability in the trace spacing is the result of the tolerances of the trace width.

Figure 17. Adapter Card Stackup



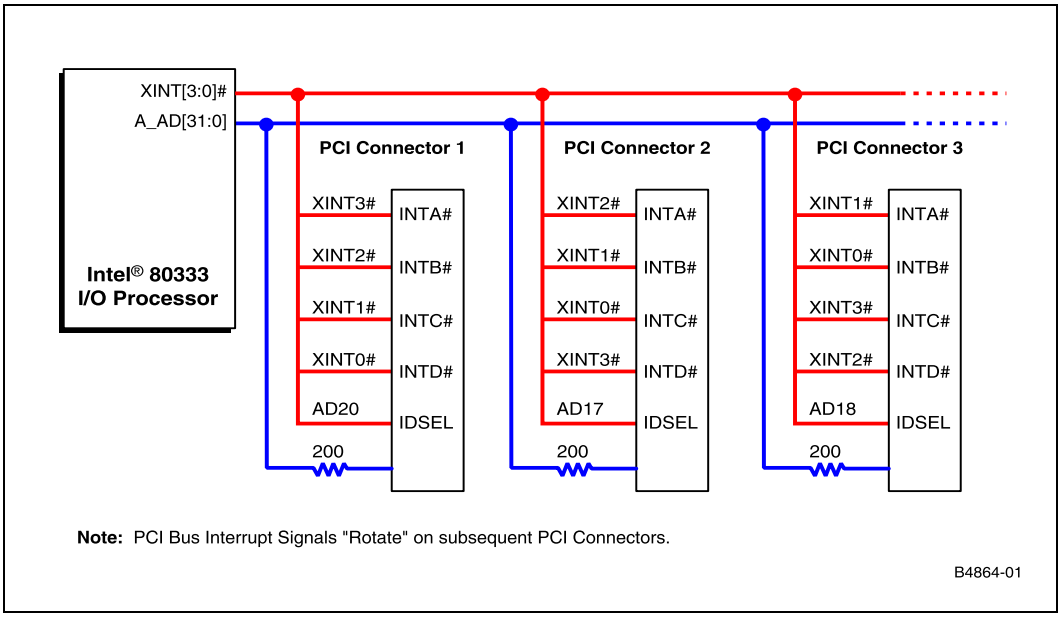
PCI-X Layout Guidelines 6

This chapter describes several factors to be considered with a 80333 PCI/PCI-X design. These include the PCI IDSEL, PCI RCOMP, PCI Interrupts, PCI arbitration and Hot-Plug.

6.1 Interrupt Routing and IDSEL Lines

Figure 18 shows the 80333 connected to three PCI connectors. Notice that the interrupts are rotated for each connector. The practice of Rotating INTs can also be used when connecting 80333 to individual multifunction PCI devices as well. The IDSEL lines acts as chip selects during the configuration cycles. Configuration cycles allow read and write access to one of the device configuration space registers. The IDSEL lines can be mapped to upper address lines which are unused during the configuration cycles. The ATU is hardwired to AD30 for IDSEL. Note that AD16 typically is reserved for a PCI/PCI-X bridge. Each IDSEL line needs a 200 ohm series resistor on it as shown in the figure below.

Figure 18. Interrupt and IDSEL Mapping



6.1.1 PCI Arbitration

80333 contains two PCI Arbiters to facilitate arbitration on the A and B PCI Buses. Refer to the *PCI Local Bus Specification*, Revision 2.3, for more information on arbiter algorithms. The specification essentially states that the algorithm needs to be fair to prevent any one device from consuming to much of the PCI bandwidth.

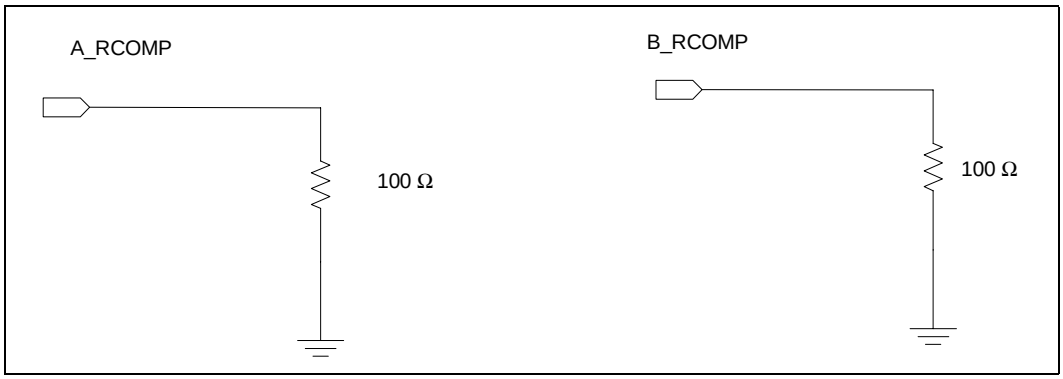
A typical implementation of the arbitration logic is a two-level rotating round robin configuration. A high priority status is assigned to a master request in level one and a low-level priority status is assigned to a master request in level two. The arbiter checks each of the REQ# lines in the first level. When none are asserted it traverses to checking level two. Once the GNT# has been asserted to a master, this master has the lowest priority in its level.

The arbiter also conducts bus parking by driving A/D, C/BE# and PAR lines to a known value while the bus is idle. The arbiter typically leaves the GNT# asserted to the master that used the bus last.

6.1.2 PCI Resistor Compensation

Figure 19 provides the recommended resistor compensation pin termination for the A and PCI BPCI primary. The voltage at the RCOMP pins is 0.75 V and a 1/16 W resistor rating is acceptable.

Figure 19. PCI RCOMP



6.1.3 PCI Hot Plug

The Intel® 80333 I/O processor (80333) integrates a standard Hot-Plug controller on the B PCI segment only, that is compliant with the *PCI Standard Hot-Plug Controller and Subsystem Specification*, Revision 1.0. This standard applies to both PCI and PCI-X modes of operation. The mode supported is 1-slot no-glue parallel.

The B_HSLOT[3] pins (muxed onto signals **AD[15:12]**) is latched on rising (asserting) edge of **PWRGD** and indicates when the 'B' PCI-X bus interface Standard Hot Plug Controller is enabled, the total number of slots in both hot plug enabled mode and disabled mode, and the hot plug mode. The below table provides the details on the hot-plug modes.

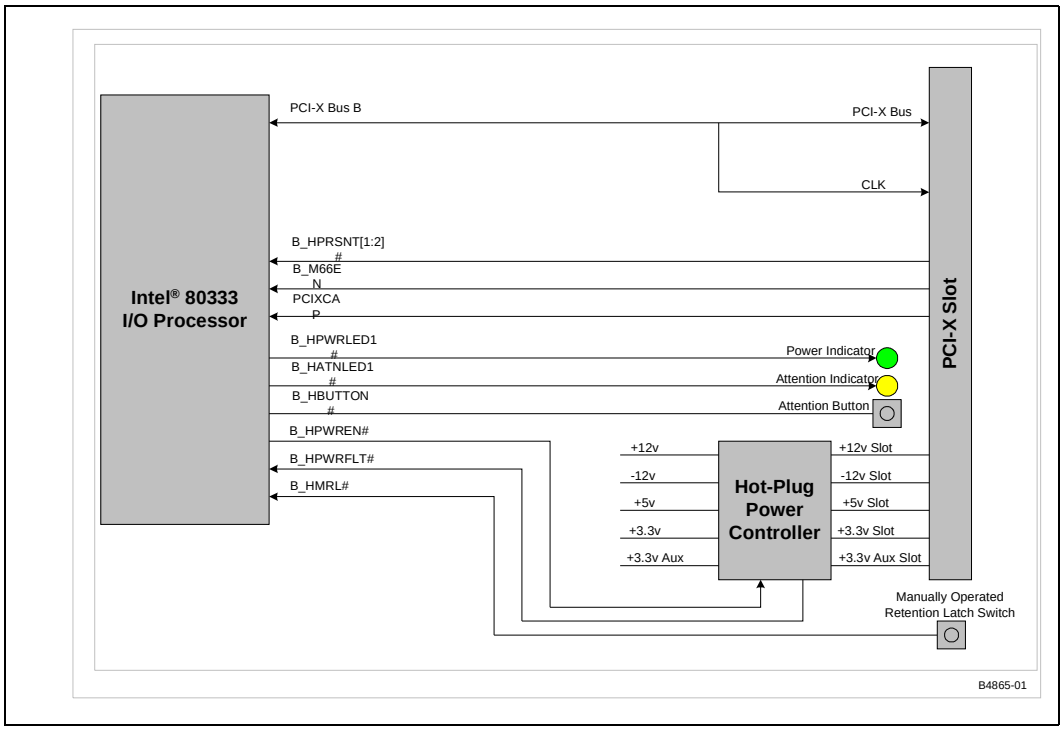
Table 7. Hot-Plug Decoding Mode

Hot-Plug Disabled		Hot-Plug Enabled	
Slots	**B_HSLOT[3]**	**Slots**	**B_HSLOT[3]**
1 slot	0000	Reserved	Reserved
2 slot	0001	Reserved	Reserved
3 slot	0010	Reserved	Reserved
4 slot	0011	Reserved	Reserved
5 slot	0100	Reserved	Reserved
6 slot	0101	Reserved	Reserved
7 slot	0110	Reserved	Reserved
8 slot	0111	1 slot no glue parallel	1111

The following conditions must be met to implement the hot-plug functionality:

- SHPC compliant Hot-Plug Controller is required.
- An independent power control to each Hot-Plug slot is required.
- Bus isolation control to each Hot-Plug slot is required.
- AC timing specs must be met when conducting.
- Valid logic levels are required when card is powered and the bus must be isolated.
- An independent RST# control to each Hot-Plug slot must be maintained.

Figure 20. Intel® 80333 I/O Processor Parallel 1 Slot Hot-Plug No Glue Mode



6.2 PCI General Layout Guidelines

For acceptable signal integrity with bus speeds up to 133 MHz it is important to PCB design layout to have controlled impedance.

- Signal trace velocity needs to be roughly 150 – 190 ps/inch
- The following signals have no length restrictions:**A_INTA#, A_INTB#, A_INTC#, A_INTD#, B_INTA#, B_INTB#, B_INTC#, INTD#** and **TCK**, **TDI**, **TDO**, **TMS** and **TRST#**

6.3 PCI-X Topology Layout Guidelines

The *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a, recommends the following guidelines for the number of loads for your PCI-X designs. Any deviation from these maximum values requires close attention to layout with regard to loading and trace lengths.

Table 8. PCI-X Slot Guidelines

Frequency	Maximum Loads	Maximum Number of Slots
66 MHz	8	4
100 MHz	4	2
133 MHz	2	1

6.4 Intel® 80333 I/O Processor PCI/X Layout Analysis

The following sections describe layout recommendations based on the signal integrity simulation analysis. This analysis was conducted using the following parameters:

- System board stack up: 50 ohm +/- 15% single-ended impedance
- Add-in card stack up: 60 ohm +/- 15% single-ended impedance
- Driver Model 80333 IBIS
- Receiver Model: generic models for PCI-X and PCI
- Driver Package Model: 80333 model
- Connector Model: Multiline coupled model
- Generic Spec Models: PCI-X and PCI
- Cross talk impact on timing was modeled
- Process corners for PCB stack and trace geometries were modeled
- PVT corner cases for buffers and package models were modeled
- Signal quality analysis covered rise time at the receiver, fall time at the receiver, rising flight time, falling flight time, low to high ring-back (noise margin high), high to low ringback (noise margin low) and low and high overshoot.

Note: The overshoot and undershoot exceeded the specifications. The requirement calls for 0.5 V and the observed overshoot in simulation was 1.2 V. This fact needs to be taken into consideration when accessing the reliability of your application.

The following notes should be considered when designing to this section's design guide recommendations:

1. The lengths recommended for AD lines are given as a range of length (for example 2.0" to 5.0"). This means that each AD bit can be routed any where between this range. There is no length matching required among AD bits. For example, AD1 can be 2.0" and AD2 can be 5.0". Routing anywhere in this range assures that the bit will meet the Set up and Hold time requirement. This is because each bit is sampled with respect to a common clock, independent of its relation with other bits.
2. There is **no** length matching requirement between Clock and AD bits. This means, that the clock can be routed to 6" and any AD bit can be 2". However the length matching requirement among clocks to each devices (and feedback clock) remains.
3. If your board aligns to the topology in these recommendations with the exception of one or more devices, these requirements listed are still valid. Each of the recommendations is made with an assumption that any device can be a "no mount". In this case adding the length before and after the "no mount" device, as a single segment is acceptable.

6.4.1 PCI Clock Layout Guidelines

The *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a, allows a maximum of 0.5 ns clock skew timing for each of the PCI-X frequencies: 66 MHz, 100 MHz and 133 MHz. A typical PCI-X application may require separate clock point-to-point connections distributed to each PCI device. 80333 provides five buffered clocks on the PCI bus, B_CLKO[4:0] and four buffered clocks on the PCI bus, A_CLKO[3:0] to connect to multiple PCI-X devices. The Figure 21 shows the use of four PCI "A" clock outputs and length matching requirements. The same rules apply to the 80333 PCI "B" four clock outputs. The recommended clock buffer layout are specified as follows:

- Match each of the 80333 output clock lengths to within 25 mils to help minimize the skew.
- Keep distance between clock lines and other signals "d" at least 25 mils from each other.
- Keep distance between clock line and itself "a" at a minimum of 25 mils apart (for serpentine clock layout).
- A_CLKIN gets connected toA_CLKOUT through a 22 ohm resistor and likewise for B_CLKIN is connected to B_CLKOUT through a 22 ohm resistor.
- The 22 ohm resistor is placed within 1" maximum distance of A_CLKOUT and B_CLKOUT.
- A series termination resistor with the value of 22 ohm resistor is placed within 1" maximum distance of each of the clock outputs A_CLKO[3:0] and B_CLKO[4:0].

Note: Using the value of 33.2 ohm for the series termination resistor is also acceptable.

Figure 21. PCI Clock Distribution and Matching Requirements

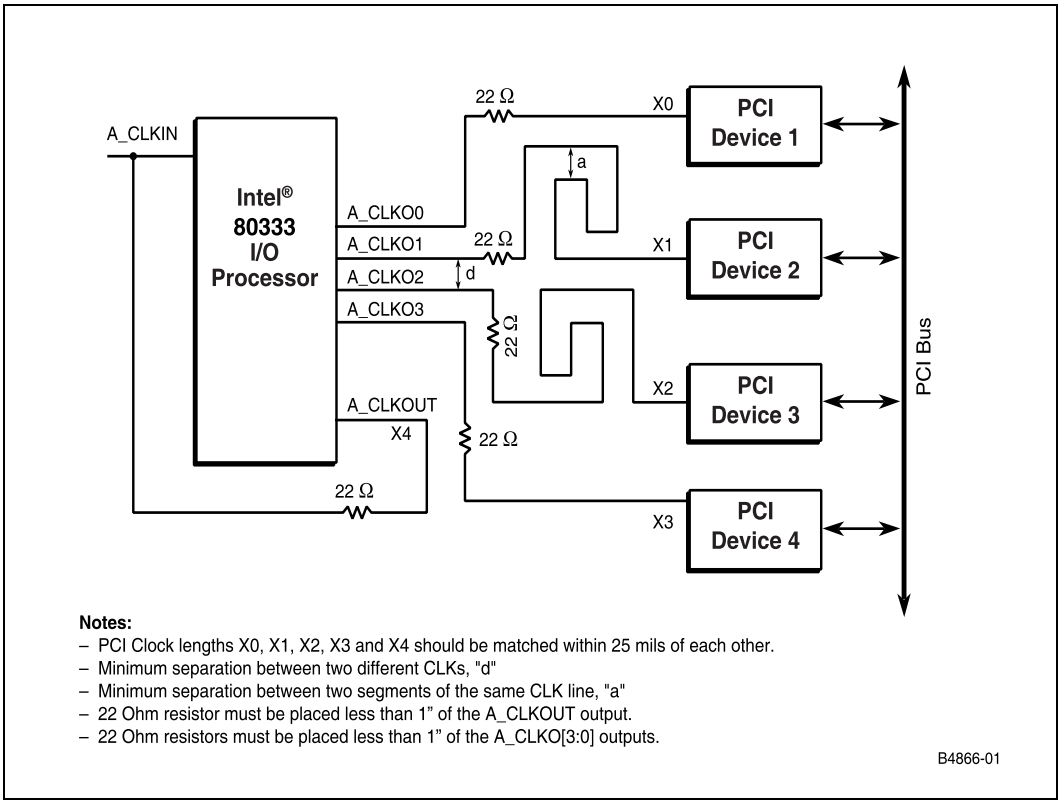


Table 9. PCI-X Clock Layout Requirements Summary (Sheet 1 of 2)

Parameter	Routing Guidelines
Signal Group	PCI Clocks B_CLKO[4:0], A_CLK[3:0]
Reference Plane	Route over unbroken ground plane.
Preferred Topology	Stripline
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils.
Motherboard Impedance (for both microstrip and stripline).	50 ohms +/- 15%.
Add-in card Impedance (for both microstrip and stripline).	57 ohms +/- 15%.
Stripline Trace Spacing: Separation between two different clock lines, “d” clock lines.	25 mils edge to edge from any other signal.
Stripline Trace Spacing: Separation between two segments of the same clock line (on serpentine layout), “a” dimension.	25 mils edge to edge from any other signal.
Stripline Trace Spacing: Separation between clocks and other lines.	50 mils edge to edge from any other signal.
Length Matching Requirements for Topologies having NO Slot	• Each of the Clock out (Clk0 - Clk3) should be length matched to the Feedback Clk (Feedback Clock is that running from CLKOUT to CLKIN). The length matching should be within 25 mills.
Length Matching Requirements for Topologies having only Slot	• Each of the Clock out (Clk0 - Clk3) to the Slots should be length matched to within 25mills. • The Feedback Clk (Feedback Clock is that running from CLKOUT to CLKIN) should be routed 3.5” longer than the Clocks running to the Slots. This should be done to a tolerance of within 25 mills.
Length Matching Requirements for Topologies having both Slots and Embedded Devices	• Each of the Clock out (Clk0 - Clk3) to the Slots (if more than 1 slot) should be length matched to within 25mills. • The Clock out to the Embedded Device(s) should be routed 3.5” longer than the Clocks running to the Slots. This should be done to a tolerance of within 25 mills. • The Feedback Clk (Feedback Clock is that running from CLKOUT to CLKIN) should be routed 3.5” longer than the Clocks running to the Slots. This should be done to a tolerance of within 25 mills.
Total Length of PCI CLKs on a motherboard (or embedded design).	Less than 14.0” maximum.
Total Length of Clock Line in an Add-in Card.	2.4” minimum to 2.6” maximum.
Series Termination.	22 ohms 1%
Trace Length from driver to series termination.	1” maximum.

Table 9. PCI-X Clock Layout Requirements Summary (Sheet 2 of 2)

Parameter	Routing Guidelines
A_CLKIN, B_CLKIN Series Termination	Connect A_CLKIN to one end of a 22 ohm resistor and the other end connected to A_CLKOUT and connect B_CLKIN to one end of a 22 ohm resistor and the other end connected to B_CLKOUT
Maximum skew for PCIX.	0.3 ns.
Maximum skew for PCI.	1.0 ns.
Routing Guideline 1.	Point-to-point signal routing needs to be used to keep reflections low.
Routing Guideline 2.	Same number of vias and routing layers as all the other clock lines from the driver to the receiver.

6.4.2 Single-Slot at 133 MHz

Figure 22 shows one of the chipset PCI AD lines connected through TL_AD1 line segments to a single-slot connector CONN1 through TL1 line segment to the 80333.

Figure 22. Single-Slot Point-to-Point Topology

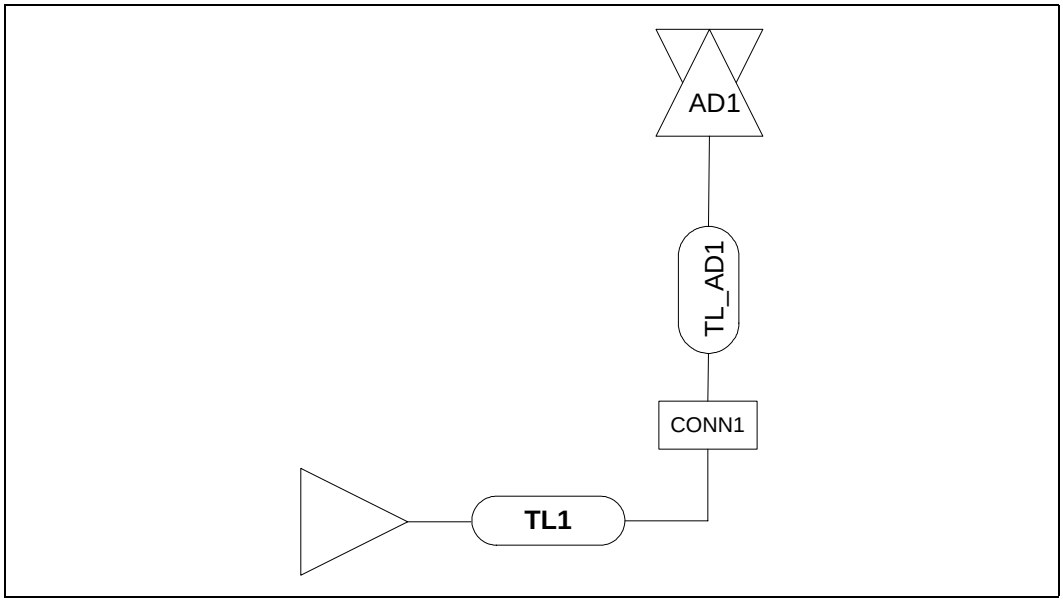


Table 10. PCI-X 133 MHz Single Slot Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus	Routing Guideline for Upper AD Bus
Reference Plane Preferred Layer	Route over an unbroken ground plane Stripline	
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500 mils.	
Motherboard Impedance (for both microstrip and stripline)	50 ohms +/- 15%	
Add-in card Impedance (for both microstrip and stripline)	57 ohms +/- 15%	
Stripline Trace Spacing	12 mils from edge to edge	
Microstrip Trace Spacing	18 mils from edge to edge	
Group Spacing	Spacing from other groups: 25 mils minimum edge to edge	
Trace Length 1 (TL1): From 80333 signal Ball to first junction	2.25” minimum - 7.5” maximum	1.25” minimum - 6.75” maximum
Trace Length 2 (TL_AD1)- from connector to receiver	0.75” minimum - 1.5” maximum	1.75” minimum - 2.75” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of vias	Two vias maximum	

6.4.3 Embedded PCI-X 133 MHz

This section lists the routing recommendations for PCI-X 133 MHz without a slot. Figure 23 shows the block diagram of this topology and Table 11 describes the routing recommendations.

Figure 23. Embedded PCI-X 133 MHz Topology

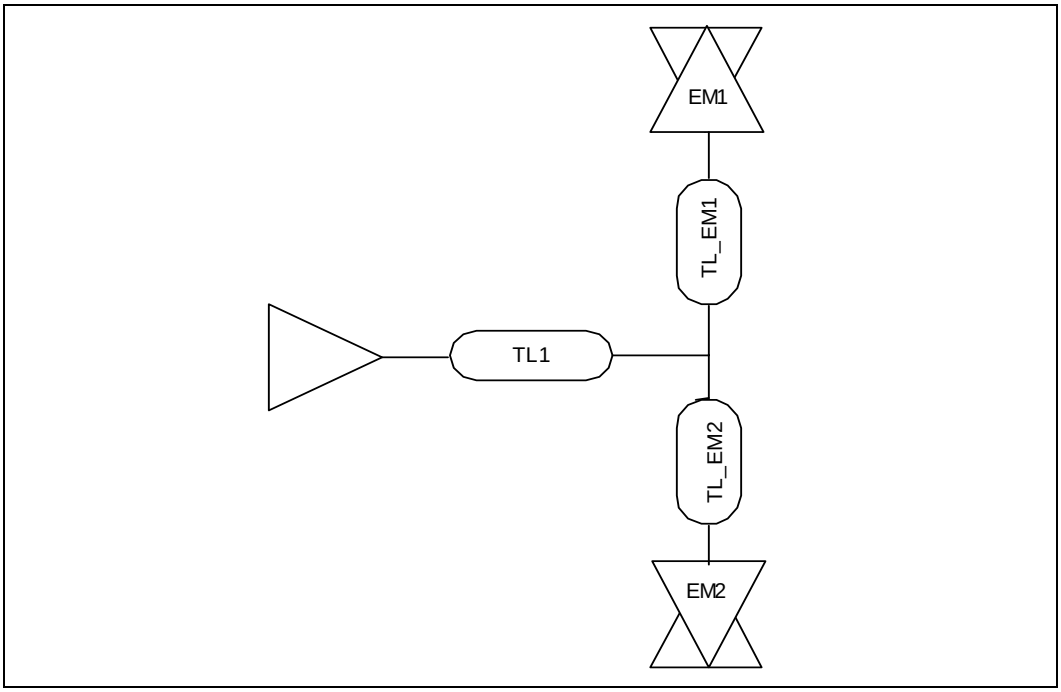


Table 11. Embedded PCI-X 133 MHz Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus
Reference Plane Preferred Layer	Route over an unbroken ground plane Stripline
Break out	5 mils on 5 mils spacing. Maximum length of breakout region is 500 mils
Motherboard impedance (both Microstrip and stripline)	50 ohms +/- 15%
Add-in card impedance (both Microstrip and stripline)	60 ohms +/- 15%
Stripline Trace Spacing	12 mils, edge to edge
Microstrip Trace Spacing	18 mils, edge to edge
Group Spacing	Spacing from other groups: 25 mils minimum edge-to-edge
Trace Length 1 (TL1): From 80333 signal Ball to first junction	1.75” minimum - 4.0” maximum
Trace Length 2 junction of TL_EM1 and TL_EM2 to embedded device	1.25” minimum - 3.25” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.
Number of vias	Three vias for each path

6.4.4 Embedded PCI-X 133 MHz Alternate Topology

This section lists another embedded topology with routing recommendations for PCI-X 133 MHz. Figure 24 shows the block diagram of this topology and Table 12 describes the routing recommendations.

Figure 24. Embedded PCI-X 133 MHz Alternate Topology

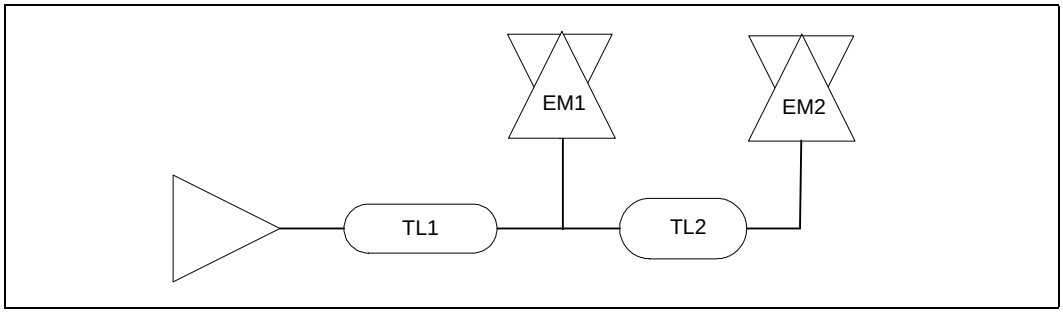


Table 12. Embedded PCI-X 133 MHz Alternate Topology Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus
Reference Plane Preferred Layer	Route over an unbroken ground plane Stripline
Break out	5 mils on 5 mils spacing. Maximum length of breakout region is 500 mils
Motherboard impedance (both Microstrip and stripline)	50 ohms +/- 15%
Add-in card impedance (both Microstrip and stripline)	60 ohms +/- 15%
Stripline Trace Spacing	12 mils edge to edge
Microstrip Trace Spacing	18 mils, edge to edge
Group Spacing	Spacing from other groups: 25 mils minimum edge to edge
Trace Length 1 (TL1): From 80333 signal Ball to first device	1.5” minimum - 3.5” maximum
Trace Length 3 TL2: First device to second device.	1.5” minimum - 3.5” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.
Number of vias	Three vias for each path

6.4.5 Combination of PCI-X 133 MHz Slot and Embedded Topology

Figure 25and Table 13 combine the two topologies using both a slot and an embedded device.

Figure 25. Embedded PCI-X 133 MHz Topology

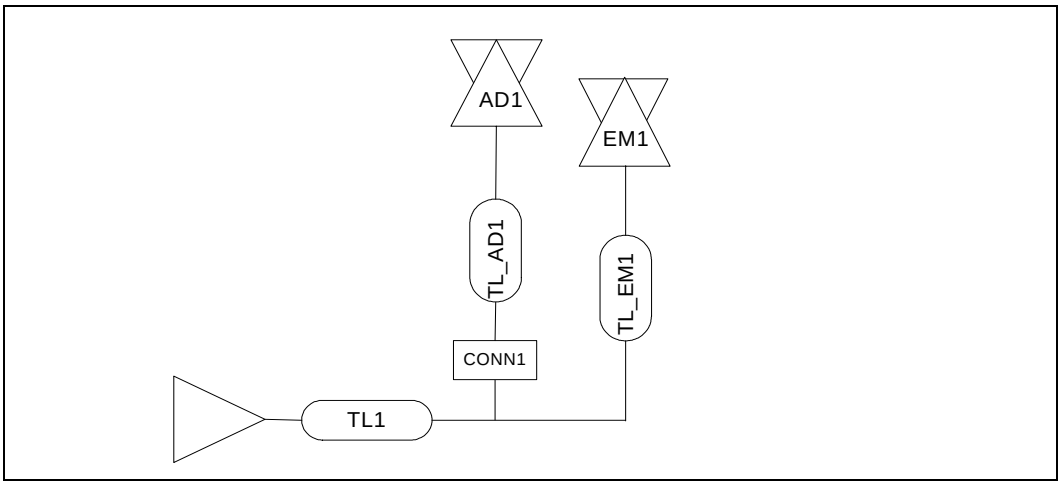


Table 13. Embedded and Slot PCI-X 133 MHz Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus	Routing Guideline for Upper AD Bus
Reference Plane	Route over an unbroken ground plane	
Preferred Layer	Stripline	
Break out	5 mils on 5 mils spacing. Maximum length of breakout region is 500 mils	
Motherboard impedance (both Microstrip and stripline)	50 ohms +/- 15%	
Add-in card impedance (both Microstrip and stripline)	57 ohms +/- 15%	
Stripline Trace Spacing	12 mils edge to edge	
Microstrip Trace Spacing	18 mils, edge to edge	
Group Spacing	Spacing from other groups: 25 mils min, center to center	
Trace Length 1 (TL1): From 80333 signal ball to first junction	1.25” minimum - 3.0” maximum	1.25” minimum - 3.0” maximum
Trace Length 3 TL_EM1 from the first junction to the embedded device	1.25” minimum - 3.75” maximum	1.25” minimum - 3.75” maximum
Trace Length TL_AD1 - from connector to the receiver	0.75” - 1.5” maximum	1.75” - 2.75” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of vias	Three vias max	

6.4.6 Combination PCI-X 133 MHz Slot and Embedded Topology 2

Figure 26and Table 14 combine the two topologies using both a slot and an embedded device.

Figure 26. Embedded PCI-X 133 MHz Topology

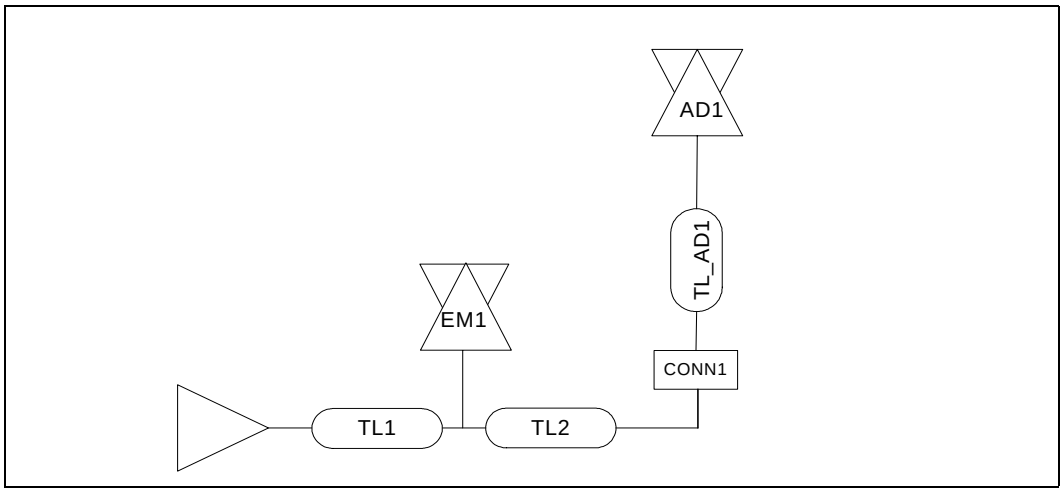


Table 14. Embedded and Slot PCI-X 133 MHz Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus	Routing Guideline for Upper AD Bus
Reference Plane Preferred Layer	Route over an unbroken ground plane Stripline	
Break out	5 mils on 5 mils spacing. Maximum length of breakout region is 500 mils	
Motherboard impedance (both Microstrip and stripline)	50 ohms +/- 15%	
Add-in card impedance (both Microstrip and stripline)	57 ohms +/- 15%	
Stripline Trace Spacing	12 mils edge to edge	
Microstrip Trace Spacing	18 mils, edge to edge	
Group Spacing	Spacing from other groups: 25 mils min, center to center	
Trace Length TL1: From 80333 signal ball to embedded device.	1.25” minimum - 2.0” maximum	1.25” minimum - 2.0” maximum
Trace Length TL2: - from Embedded Device to PCIX connector CONN1	1.25” minimum - 3.5” maximum	1.25” minimum - 3.0” maximum
Trace Length TL_AD1 - from connector to the receiver	0.75” - 1.5” maximum	1.75” - 2.75” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of vias	Three vias max	

6.4.7 PCI-X 133 MHz Hot Plug Topology

Figure 27and Table 15 provide information on PCIX 133MHz Hot Plug Topology.

Figure 27. PCI-X 133 MHz Hot Plug Topology

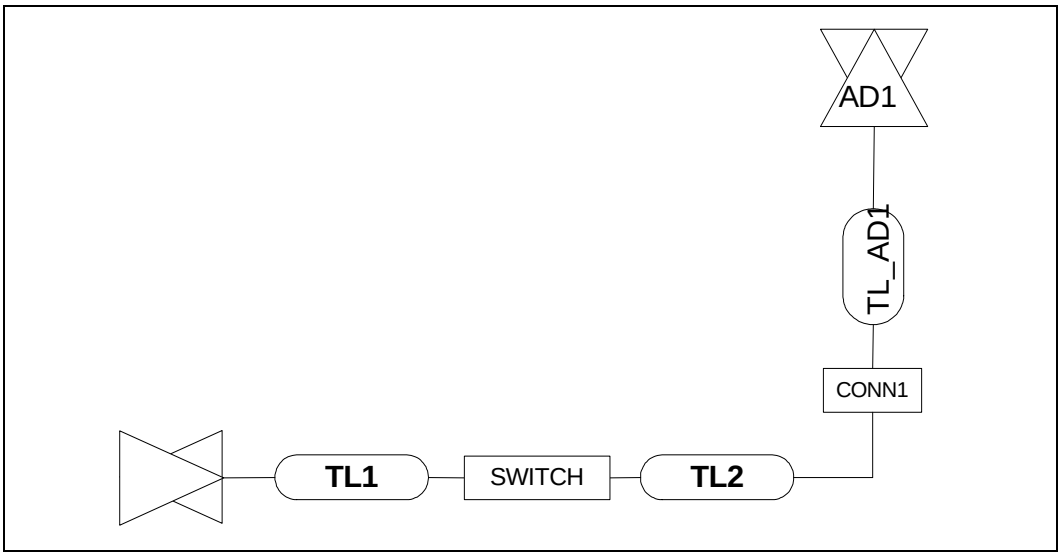


Table 15. PCI-X 133 MHz Hot Plug Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus	Routing Guideline for Upper AD Bus
Reference Plane Preferred Layer	Route over an unbroken ground plane Stripline	
Break out	5 mils on 5 mils spacing. Maximum length of breakout region is 500 mils	
Motherboard impedance (both microstip and stripline)	50 ohms +/- 15%	
Add-in card impedance (both microstip and stripline)	57 ohms +/- 15%	
Stripline Trace Spacing	12 mils edge to edge	
Microstrip Trace Spacing	18 mils, edge to edge	
Group Spacing	Spacing from other groups: 25 mils min, edge to edge	
Trace Length 1 (TL1): From 80333 signal ball to switch	1.5” min - 6.5” max	1.5” min- 5.5” max
Trace Length 2 (TL2)- From switch to the connector CONN1	1.0” max	1.0” max
Trace Length TL_AD1 - from connector to the receiver	0.75” - 1.5” max	1.75” - 2.75” max
Length Matching Requirement	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of vias	2 vias max	

6.4.8 PCI-X 100 MHz Slot Topology

Figure 28and Table 16 provide details on the PCI-X 100 MHz slot topology.

Figure 28. Slot PCI-X 100 MHz Slot Routing Topology

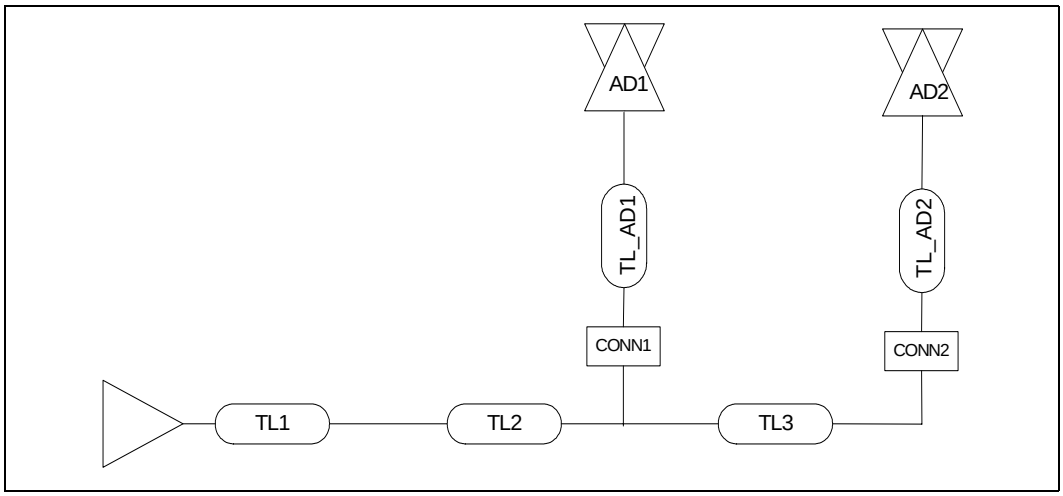


Table 16. PCI-X 100 MHz Slot Topology Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus	Routing Guideline for Upper AD Bus
Reference Plane Preferred Layer	Route over an unbroken ground plane Stripline	
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.	
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%	
Add-in card Impedance (microstrip and stripline)	57 Ohms +/- 15%	
Stripline Trace Spacing	12 mils, from edge to edge	
Microstrip Trace Spacing	18 mils, from edge to edge	
Group Spacing	Spacing from other groups: 25 mils min, center to center	
Trace Length 1 TL1: From 80333 signal Ball to first junction	1.0” minimum - 9.5” maximum	1.0” - 7.0” maximum
Trace Length TL2 - between junction and connector	0.8” - 1.1” maximum	0.8” - 1.1” maximum
Trace Length TL_AD1, TL_AD2- from connector to receiver	0.75” minimum - 1.5” maximum	1.75” minimum - 2.75” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of vias	Three vias max	

6.4.9 PCI-X 100 MHz Embedded Topology

Figure 29and Table 17 combine both a slot and an embedded device.

Figure 29. Embedded PCI-X 100 MHz Routing Topology

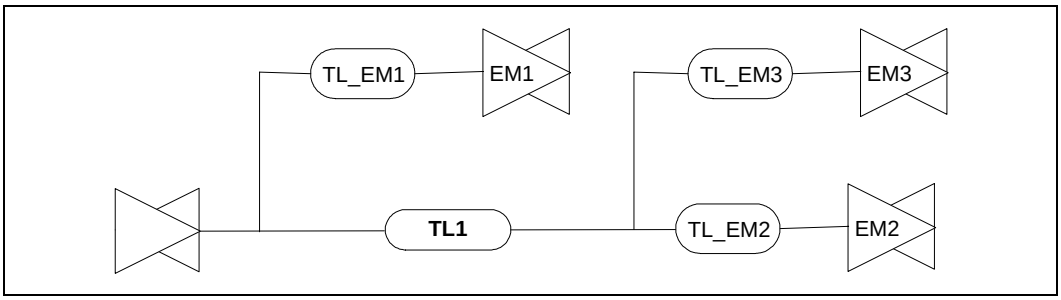


Table 17. PCI-X 100 MHz Embedded Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus
Reference Plane Preferred Layer	Route over an unbroken ground plane Stripline
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%
Add-in card Impedance (microstrip and stripline)	60 Ohms +/- 15%
Stripline Trace Spacing	12 mils, from edge to edge
Microstrip Trace Spacing	18 mils, from edge to edge
Group Spacing	Spacing from other groups: 25 mils minimum edge to edger
Trace Length 1 TL1: From 80333 signal Ball to first junction	0.5” minimum - 3.0” maximum
Trace Length TL_EM1 - between junction and embedded device	2.5” - 3.5” maximum
Trace Length TL_EM2, TL_EM3- from second junction to embedded devices	1.5” minimum to 3.5 maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.
Number of vias	Four vias maximum for each path

6.4.10 PCI-X 100 MHz Slot and Embedded Topology

Figure 30and Table 18 combine both slots and an embedded device.

Figure 30. Combination of Slot and Embedded PCI-X 100 MHz Routing Topology

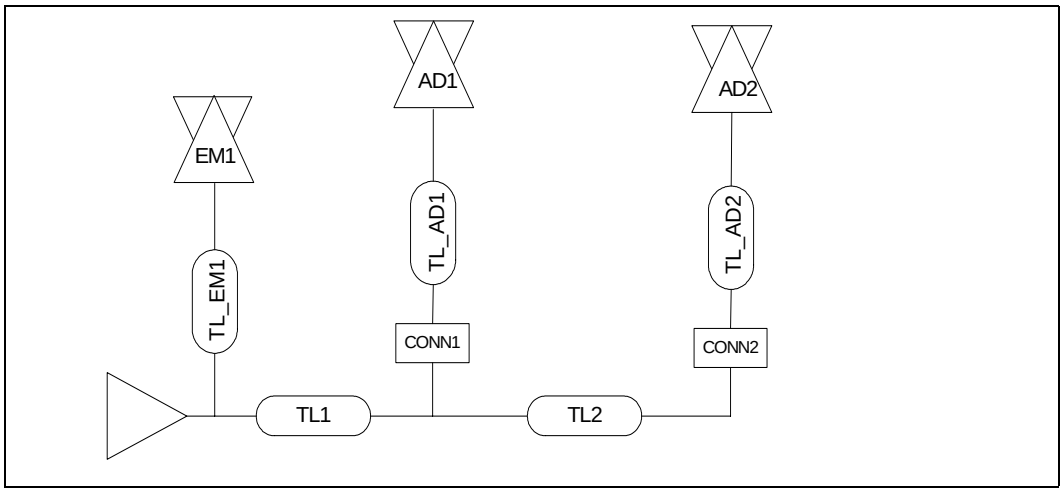


Table 18. Combination of Slot and Embedded PCI-X 100 MHz Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus	Routing Guideline for Upper AD Bus
Reference Plane Preferred Layer	Route over an unbroken ground plane Stripline	
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.	
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%	
Add-in card Impedance (microstrip and stripline)	57 Ohms +/- 15%	
Stripline Trace Spacing	12 mils, from edge to edge	
Microstrip Trace Spacing	18 mils, from edge to edge	
Group Spacing	Spacing from other groups: 25 mils minimum edge to edge	
Trace Length 1 TL1: From 80333 signal Ball to first connector CONN1	2.0” minimum - 3.75” maximum	2.0”minimum - 3.0” maximum
Trace Length TL2 - first PCI connector CONN1 to second PCI connector CONN2	0.8” minimum - 1.2” maximum	
Trace Length TL_AD1, TL_AD2 - from PCI connector to receiver	2.25” minimum - 3.75” maximum	2.25” minimum - 3.5” maximum
Trace Length TL_EM1 - from second connector CONN2 to embedded device	0.75” minimum - 1.5” maximum	1.75” minimum - 2.75” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of vias	Three vias maximum	

6.4.11 PCI-X 100 MHz Slot and Embedded Topology 2

Figure 30and Table 18 combine both a slots and an embedded device.

Figure 31. Combination of Slots and Embedded PCI-X 100 MHz Routing Topology

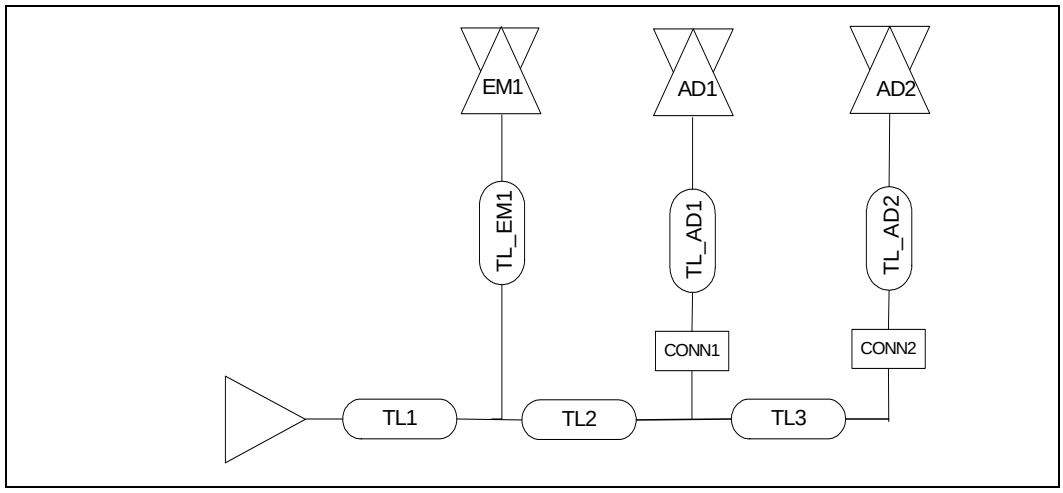


Table 19. Combination of Slot and Embedded PCI-X 100 MHz Routing 2 Recommendations (Sheet 1 of 2)

Parameter	Routing Guideline for Lower AD Bus	Routing Guideline for Upper AD Bus
Reference Plane Preferred Layer	Route over an unbroken ground plane Stripline	
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.	
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%	
Add-in card Impedance (microstrip and stripline)	57 Ohms +/- 15%	
Stripline Trace Spacing	12 mils, from edge to edge	
Microstrip Trace Spacing	18 mils, from edge to edge	
Group Spacing	Spacing from other groups: 25 mils minimum edge to edge	
Trace Length 1 TL1: From 80333 signal Ball to first junction	1.5” minimum - 4.25” maximum	1.5”minimum - 3.75” maximum
Trace Length TL2 - first junction to First PCI Connector	0.0” minimum to 1.0” maximum	
Trace Length TL3 - First PCI Connector to Second PCI Connector	0.8” minimum - 1.2” maximum	
Trace Length TL_EM1 - from first junction to the Embedded Device.	1.0” minimum - 3.25” maximum	1.0” minimum - 3.25” maximum

Table 19. Combination of Slot and Embedded PCI-X 100 MHz Routing 2 Recommendations (Sheet 2 of 2)

Trace Length TL_AD1, TL_AD2 - from connector to receiver	0.75” minimum - 1.5” maximum	1.75” minimum - 2.75” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of vias	Three vias maximum	

6.4.12 PCI-X 100 MHz Hot Plug Topology

Figure 32and Table 15 provide information on PCIX 100MHz Hot Plug Topology.

Figure 32. PCI-X 100 MHz Hot Plug Topology

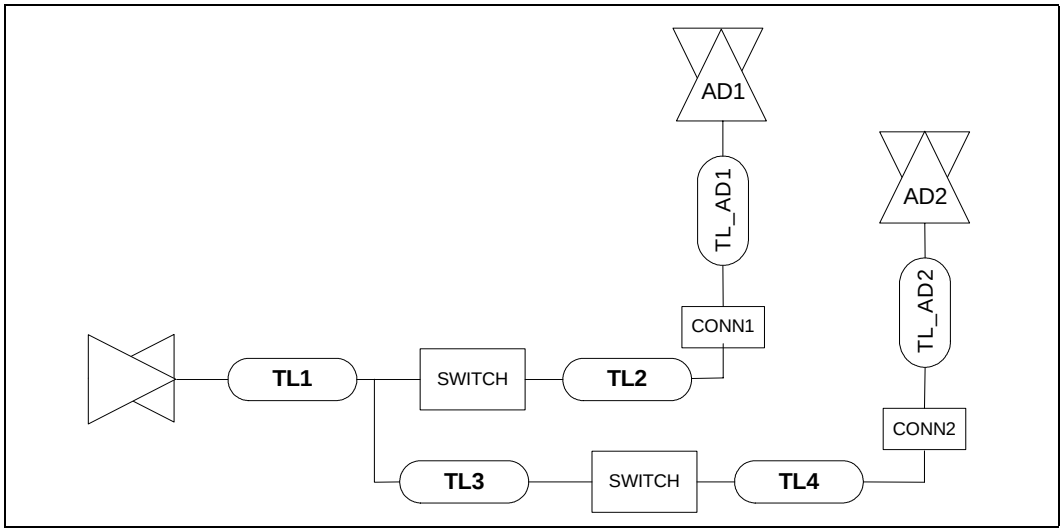


Table 20. PCI-X 100 MHz Hot Plug Routing Recommendations (Sheet 1 of 2)

Parameter	Routing Guideline for Lower AD Bus	Routing Guideline for Upper AD Bus
Reference Plane Preferred Layer	Route over an unbroken ground plane Stripline	
Break out	5 mils on 5 mils spacing. Maximum length of breakout region is 500 mils	
Motherboard impedance (both microstip and stripline)	50 ohms +/- 15%	
Add-in card impedance (both microstip and stripline)	57 ohms +/- 15%	
Stripline Trace Spacing	12 mils edge to edge	
Microstrip Trace Spacing	18 mils, edge to edge	
Group Spacing	Spacing from other groups: 25 mils min, edge to edge	
Trace Length (TL1): From 80333 signal ball to switch	1.5” min - 7.0” max	1.5” min - 5.5” max
Trace Length (TL2)- From 1st switch to the connector CONN1	1.0” max	1.0” max
Trace Length (TL3): From first switch to second switch	2.0” max	2.0” max

Table 20. PCI-X 100 MHz Hot Plug Routing Recommendations (Sheet 2 of 2)

Parameter	Routing Guideline for Lower AD Bus	Routing Guideline for Upper AD Bus
Trace Length (TL4): From second switch to second connector	1.0” max	1.0” max
Trace Length TL_AD1 - from connector to the receiver	0.75” - 1.5” max	1.75” - 2.75” max
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of vias	2 vias max	

6.4.13 PCI-X 66 MHz Slot Topology

Figure 33 and Table 21 provides routing details for a topology with for an embedded PCI-X 66 MHz application.

Figure 33. PCI-X 66 MHz Slot Routing Topology

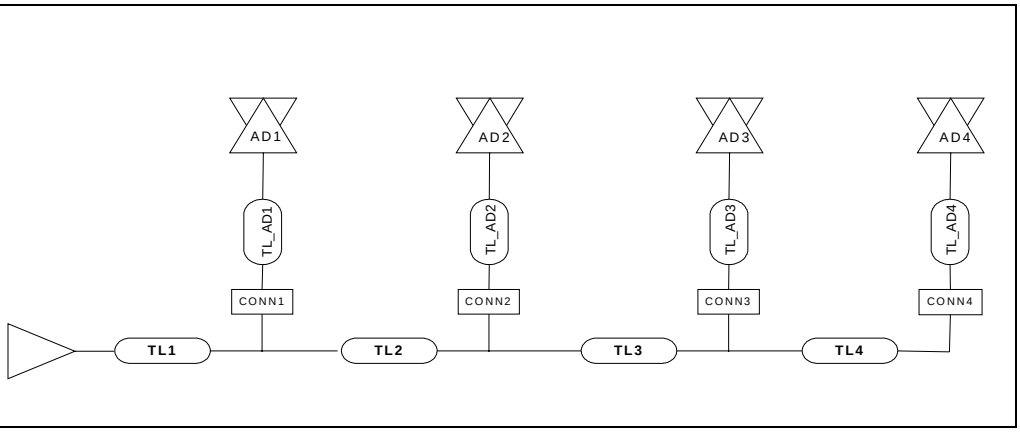


Table 21. PCI-X 66 MHz Slot Routing Recommendations (Sheet 1 of 2)

Parameter	Routing Guideline for AD Bus	
Reference Plane	Route over an unbroken ground plane	
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.	
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%	
Add-in card Impedance (microstrip and stripline)	57 Ohms +/- 15%	
Stripline Trace Spacing	12 mils, from edge to edge	
Microstrip Trace Spacing	18 mils, from edge to edge	
Group Spacing	Spacing from other groups: 25 mils minimum center to center	
Trace Length 1 (TL1): From 80333 signal Ball to first junction	1.0” minimum - 6.0” maximum	1.0” minimum - 4.75” maximum
Trace Length TL2 to TL4 between junctions	0.8” minimum - 1.2” maximum	

Table 21. PCI-X 66 MHz Slot Routing Recommendations (Sheet 2 of 2)

Trace Length TL_AD1 to TL_AD4 - from junction to connector to receiver	0.75” minimum - 1.5” maximum	1.75” minimum - 2.75” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of vias	Four vias maximum	

6.4.14 PCI-X 66 MHz Embedded Topology

Figure 34 and Table 22 provides routing details for a topology with for an embedded PCI-X 66 MHz application.

Figure 34. PCI-X 66 MHz Embedded Routing Topology

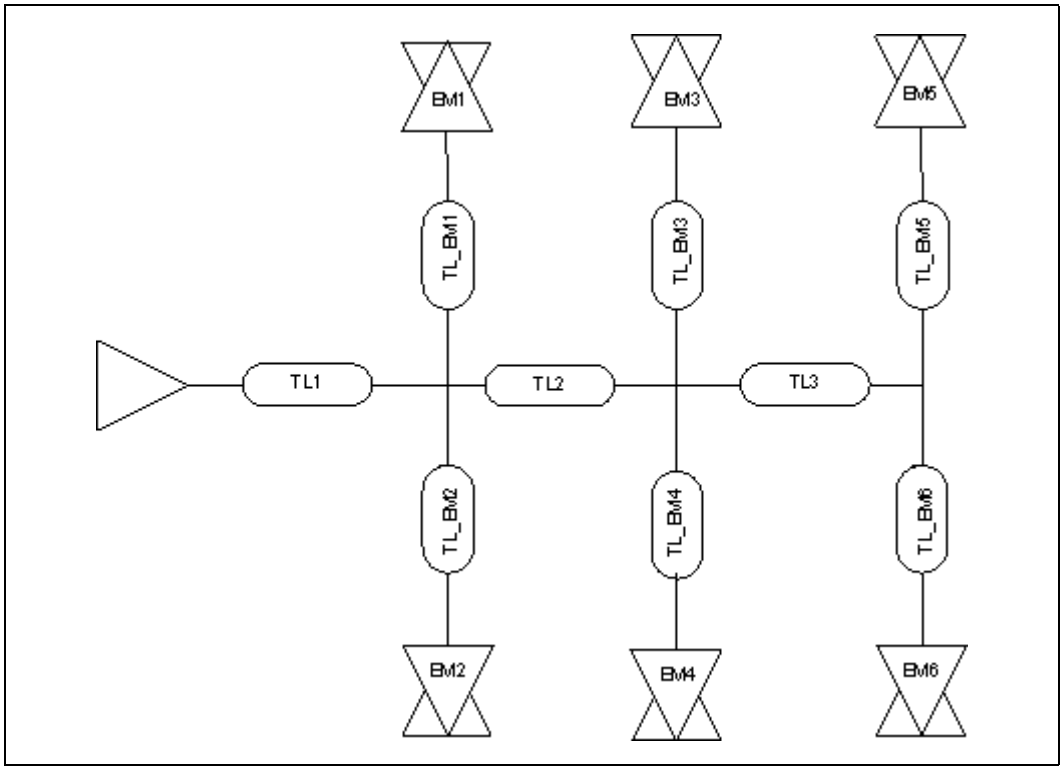


Table 22. PCI-X 66 MHz Embedded Routing Recommendations (Sheet 1 of 2)

Parameter	Routing Guideline for AD Bus
Reference Plane	Route over an unbroken ground plane
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%
Add-in card Impedance (microstrip and stripline)	60 Ohms +/- 15%
Stripline Trace Spacing	12 mils, from edge to edge

Table 22. PCI-X 66 MHz Embedded Routing Recommendations (Sheet 2 of 2)

Microstrip Trace Spacing	18 mils, from edge to edge
Group Spacing	Spacing from other groups: 25 mils minimum center to center
Trace Length 1 (TL1): From 80333 signal Ball to first junction	1.0” minimum - 5.0” maximum
Trace Length TL2 to TL3 between junctions	1.0” minimum - 2.5” maximum
Trace Length TL_EM1 to TL_EM6 - from junction to embedded devices	2.0” minimum - 3.0” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.
Number of vias	Four vias maximum

6.4.15 PCI-X 66 MHz Mixed Mode Topology

Figure 35 and Table 23 provides routing details for a topology with for an embedded PCI-X 66 MHz design with slots.

Figure 35. PCI-X 66 MHz Mixed Mode Routing Topology

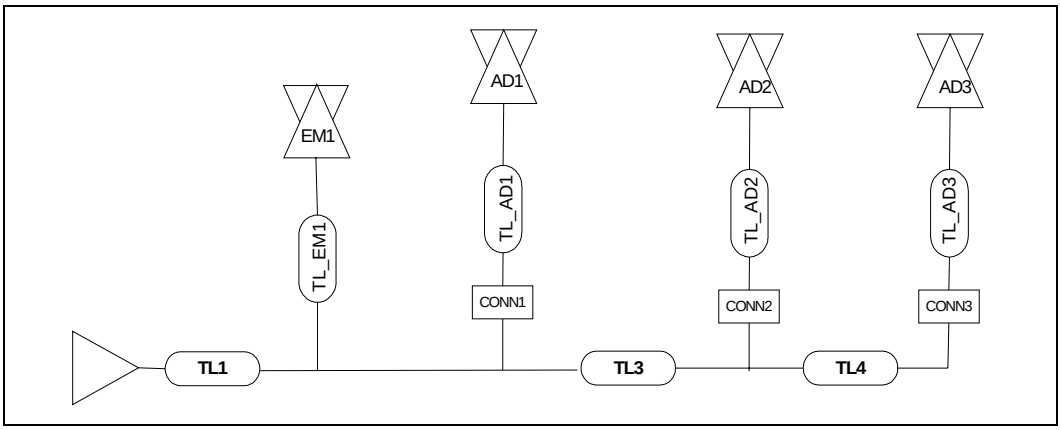


Table 23. PCI-X 66 MHz Mixed Mode Routing Recommendations (Sheet 1 of 2)

Parameter	Routing Guideline for AD Bus	Routing Guideline for Upper AD Bus
Reference Plane	Route over an unbroken ground plane	
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.	
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%	
Add-in card Impedance (microstrip and stripline)	57 Ohms +/- 15%	
Stripline Trace Spacing	12 mils, from edge to edge	
Microstrip Trace Spacing	18 mils, from edge to edge	
Group Spacing	Spacing from other groups: 25 mils minimum center to center	
Trace Length 1 TL1: From 80333 signal Ball to first slot	1.0” minimum - 5.0” maximum	1.0” minimum - 4.5” maximum

Table 23. PCI-X 66 MHz Mixed Mode Routing Recommendations (Sheet 2 of 2)

Trace Length TL3, TL4, between connectors	0.8” minimum - 1.4” maximum	
Trace Length TL_EM1 from the first PCI connector to the embedded device.	1.0” minimum - 3.5” maximum	
Trace Length TL_AD1, TL_AD2, TL_AD3 from PCI connector to the Receiver	0.75” minimum - 1.5” maximum	1.75” minimum - 2.75” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of vias	Four vias maximum	

6.4.16 PCI 66 MHz Slot Topology

Figure 36 and Table 24 provides routing details for a topology with for an PCI 66 MHz design with slots.

Figure 36. PCI 66 MHz Topology

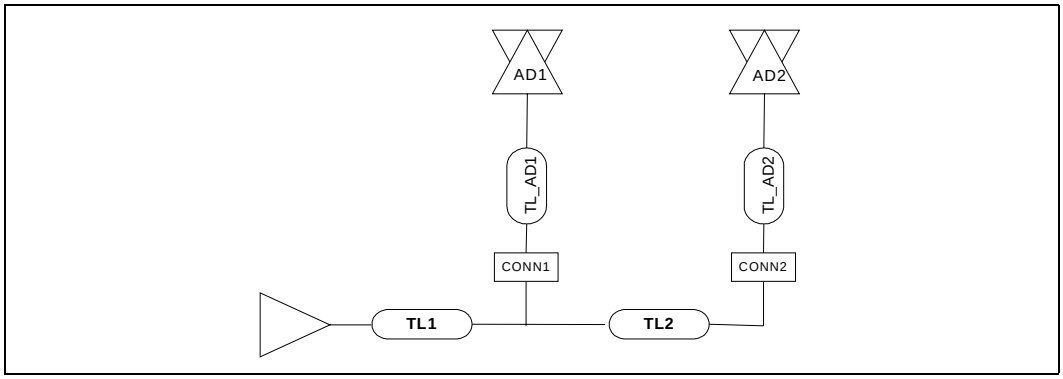


Table 24. PCI 66 MHz Slot Table (Sheet 1 of 2)

Parameter	Routing Guideline for AD Bus	Routing Guideline for Upper AD Bus
Reference Plane	Route over an unbroken ground plane	
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.	
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%	
Add-in card Impedance (microstrip and stripline)	60 Ohms +/- 15%	
Stripline Trace Spacing	10 mils, from edge to edge	
Microstrip Trace Spacing	15 mils, from edge to edge	
Group Spacing	Spacing from other groups: 25 mils minimum edge-to-edge	
Trace Length 1 TL1: From 80333 signal Ball to first connector	1.0” minimum - 7.0” maximum	1.0” minimum - 7.0” maximum
Trace Length TL2 between connectors	0.8” minimum - 1.2” maximum	

Table 24. PCI 66 MHz Slot Table (Sheet 2 of 2)

Parameter	Routing Guideline for AD Bus	Routing Guideline for Upper AD Bus
Trace Length TL_AD1, TL_AD2 from connector to receiver	0.75” minimum - 1.5” maximum	1.75” minimum - 2.75” maximum
Length Matching Requirements	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of Vias	Four vias maximum	

6.4.17 PCI 66 MHz Embedded Topology

Figure 37 and Table 25 provides routing details for a topology with for an embedded PCI 66 MHz design.

Figure 37. PCI 66 MHz Embedded Topology

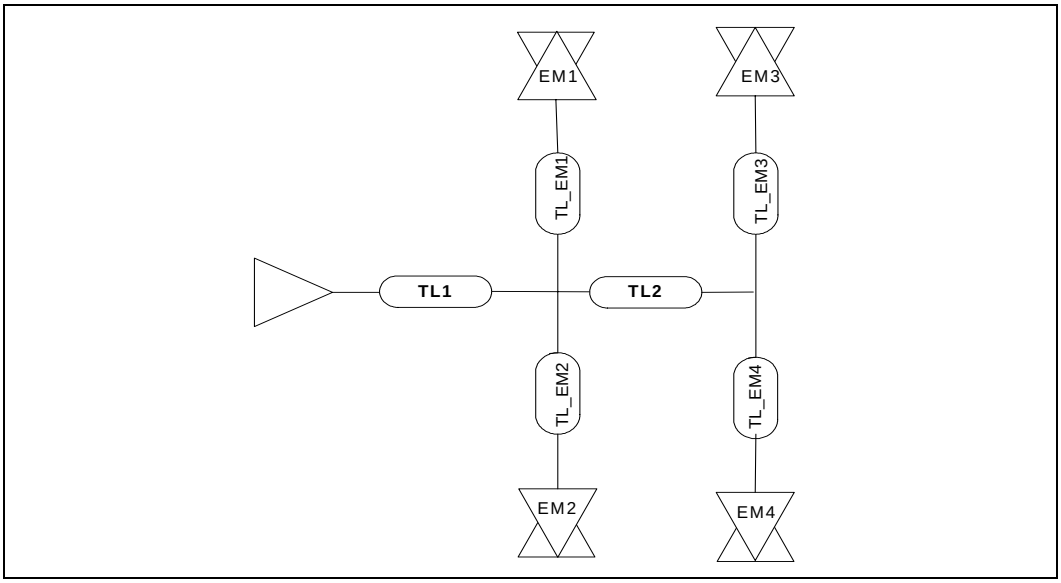


Table 25. PCI 66 MHz Embedded Table (Sheet 1 of 2)

Parameter	Routing Guideline for AD Bus
Reference Plane	Route over an unbroken ground plane
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%
Add-in card Impedance (microstrip and stripline)	60 Ohms +/- 15%
Stripline Trace Spacing	10 mils, from edge to edge
Microstrip Trace Spacing	15 mils, from edge to edge
Group Spacing	Spacing from other groups: 25 mils minimum edge to edge

Table 25. PCI 66 MHz Embedded Table (Sheet 2 of 2)

Parameter	Routing Guideline for AD Bus
Trace Length 1 TL1: From 80333 signal Ball to first junction	5.0” maximum
Trace Length TL2 between junctions	0.5” minimum - 3.5” maximum
Trace Length TL_EM1 to TL_EM4 from junction to embedded devices	2.0” minimum - 3.0” maximum
Length Matching Requirements	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.
Number of vias	Four vias maximum

6.4.18 PCI 66 MHz Mixed Mode Topology

Figure 38 and Table 26 provide routing details for a topology with embedded devices and PCI 66 MHz slots.

Figure 38. PCI 66 MHz Mixed Topology

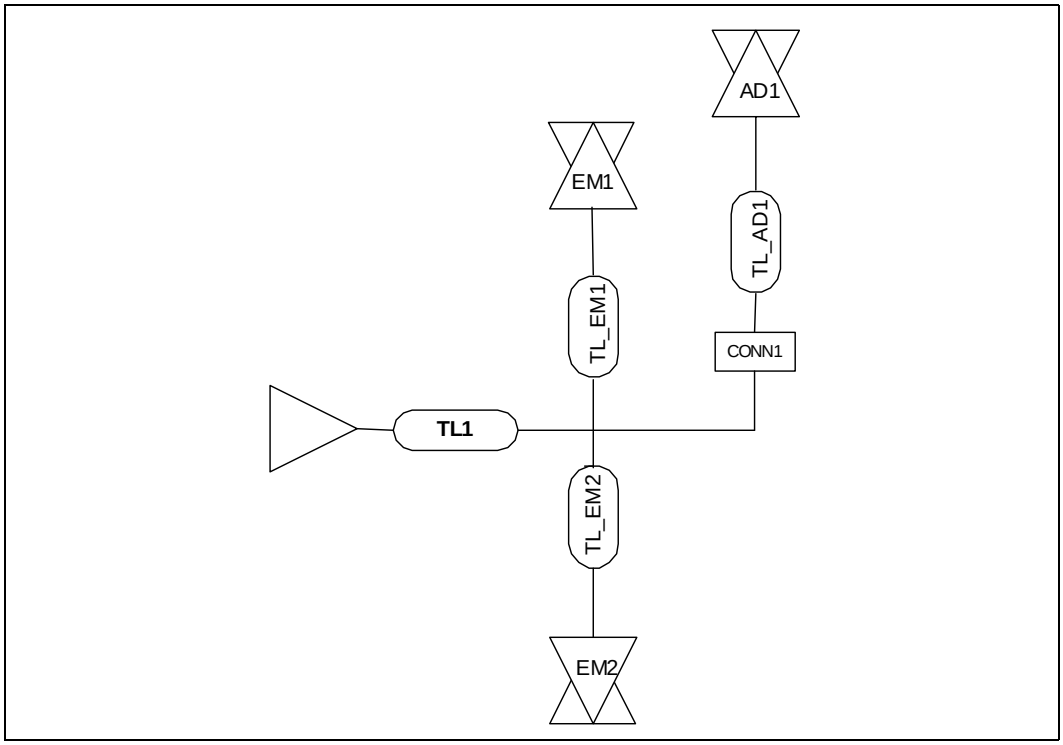


Table 26. PCI 66 MHz Mixed Mode Table (Sheet 1 of 2)

Parameter	Routing Guideline Lower AD Bus	Routing Guideline Upper AD Bus
Reference Plane	Route over an unbroken ground plane	
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.	
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%	

Table 26. PCI 66 MHz Mixed Mode Table (Sheet 2 of 2)

Parameter	Routing Guideline Lower AD Bus	Routing Guideline Upper AD Bus
Add-in card Impedance (microstrip and stripline)	57 Ohms +/- 15%	
Stripline Trace Spacing	10 mils, from edge to edge	
Microstrip Trace Spacing	15 mils, from edge to edge	
Group Spacing	Spacing from other groups: 25 mils minimum edge-to-edge	
Trace Length 1 TL1: From 80333 signal Ball to first connector	1.0” minimum to 5.0” maximum	1.0” minimum - 4.5” maximum
Trace Length TL_EM1, TL_EM2: From 1st PCI connector to embedded device	1.5” minimum - 4.0” maximum	
Trace Length TL_AD1 from PCI connector to receiver	0.75” minimum - 1.5” maximum	1.75” minimum - 2.75” maximum
Length Matching Requirements	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of Vias	Four vias maximum	

6.4.19 PCI 33 MHz Slot Topology

Figure 39 and Table 27 provides routing details for a topology with for a PCI 33 MHz design with slots.

Figure 39. PCI 33 MHz Slot Routing Topology

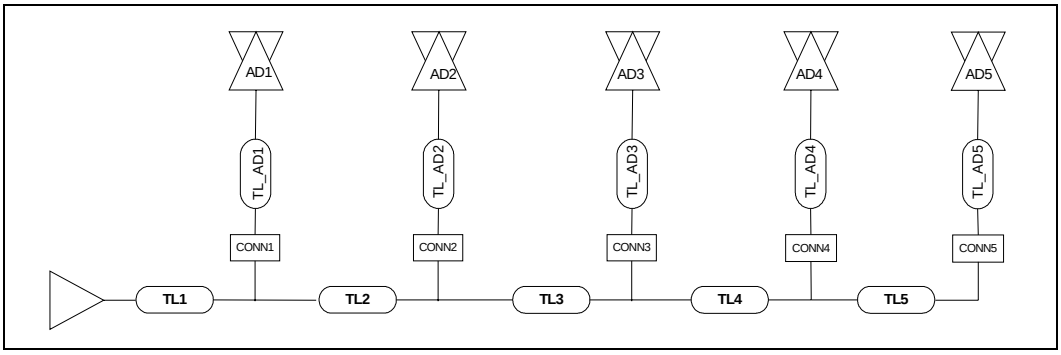


Table 27. PCI 33 MHz Slot Routing Recommendations (Sheet 1 of 2)

Parameter	Routing Guideline for AD Bus	
Reference Plane	Route over an unbroken ground plane	
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.	
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%	
Add-in card Impedance (microstrip and stripline)	57 Ohms +/- 15%	
Stripline Trace Spacing	10 mils, from edge to edge	
Microstrip Trace Spacing	15 mils, from edge to edge	
Group Spacing	Spacing from other groups: 25 mils minimum edge-to-edge	
Trace Length 1 TL1: From 80333 signal Ball to first connector	1” minimum - 7.0” maximum	1” minimum - 6.5” maximum

Table 27. PCI 33 MHz Slot Routing Recommendations (Sheet 2 of 2)

Trace Length TL2 to TL5 between connectors.	0.8” minimum - 1.5” maximum	
Trace Length TL_AD1 to TL_AD5 from connector to receiver	0.75” minimum - 1.5” maximum	1.75” minimum - 2.75” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of vias	Four vias maximum	

6.4.20 PCI 33 MHz Embedded Mode Topology

Figure 40 and Table 28 provides routing details for a topology with for an embedded PCI 33 MHz design.

Figure 40. PCI 33 MHz Embedded Mode Routing Topology

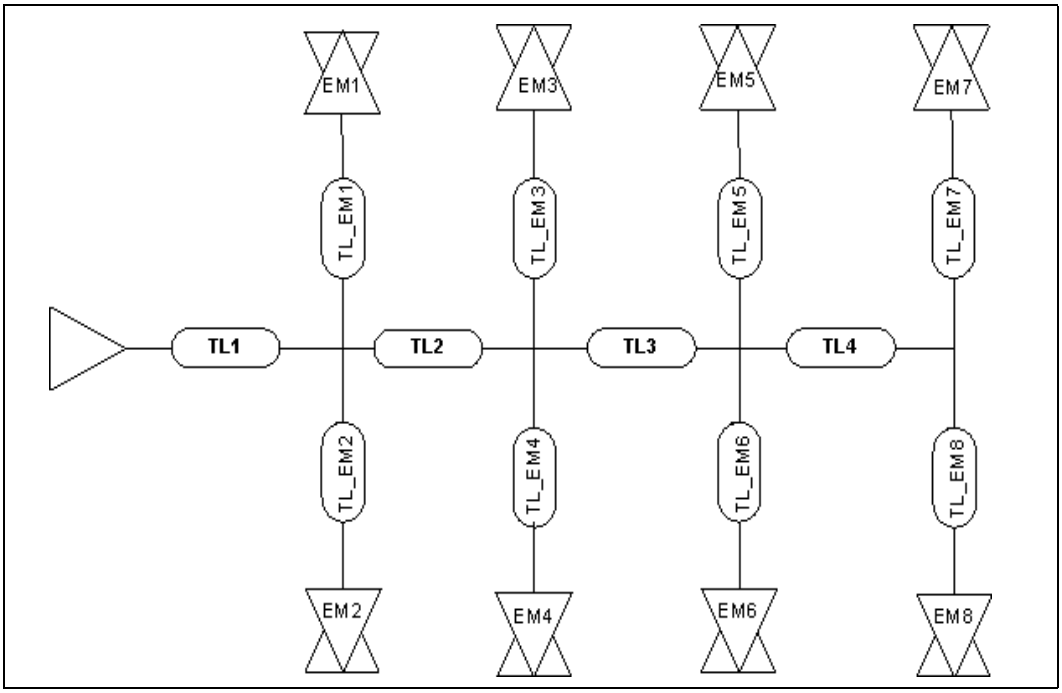


Table 28. PCI 33 MHz Embedded Routing Recommendations (Sheet 1 of 2)

Parameter	Routing Guideline for Lower AD Bus
Reference Plane	Route over an unbroken ground plane
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%
Add-in card Impedance (microstrip and stripline)	60 Ohms +/- 15%
Stripline Trace Spacing	10 mils, from edge to edge
Microstrip Trace Spacing	15 mils, from edge to edge

Table 28. PCI 33 MHz Embedded Routing Recommendations (Sheet 2 of 2)

Group Spacing	Spacing from other groups: 25 mils minimum edge-to-edge
Trace Length 1 TL1: From 80333 signal Ball to first junction	4.5” maximum
Trace Length TL2 to TL4 between junctions	1.5” minimum - 3.0” maximum
Trace Length TL_EM1 to TL_EM8 junction to embedded devices	2.0” minimum - 3.0” maximum
Length Matching Requirements:	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.
Number of vias	Four vias maximum

6.4.21 PCI 33 MHz Mixed Topology

Figure 41 and Table 29 provides routing details for a topology with for an embedded PCI 33 MHz design with slots.

Figure 41. PCI 33 MHz Mixed Mode Routing Topology

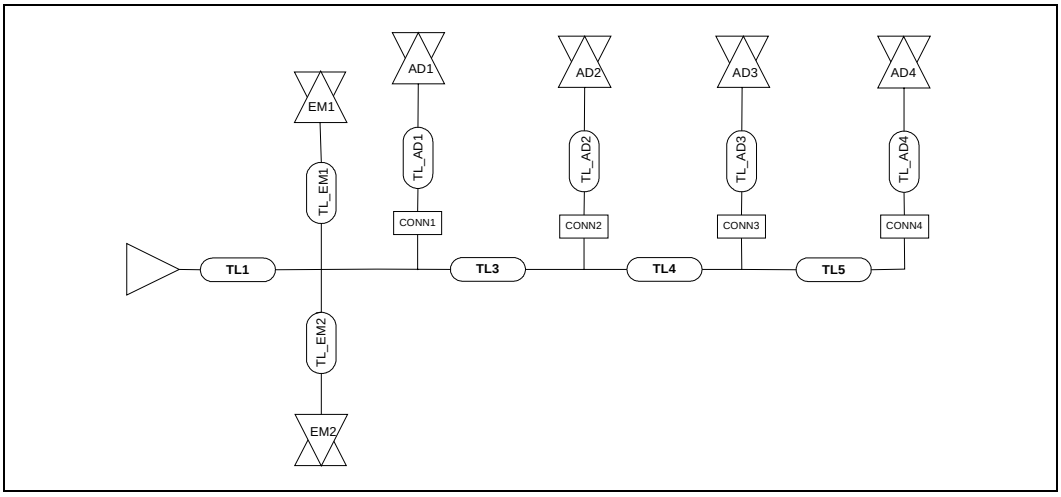


Table 29. PCI 33 MHz Mixed Mode Routing Recommendations (Sheet 1 of 2)

Parameter	Routing Guideline for lower AD Bus	Routing Guideline for upper AD Bus
Reference Plane	Route over an unbroken ground plane	
Breakout	5 mils on 5 mils spacing. Maximum length of the breakout is 500 mils.	
Motherboard Trace Impedance (microstrip and stripline)	50 Ohms +/- 15%	
Add-in card Impedance (microstrip and stripline)	57 Ohms +/- 15%	
Stripline Trace Spacing	10 mils, from edge to edge	
Microstrip Trace Spacing	15 mils, from edge to edge	
Group Spacing	Spacing from other groups: 25 mils minimum edge-to-edge	

Table 29. PCI 33 MHz Mixed Mode Routing Recommendations (Sheet 2 of 2)

Parameter	Routing Guideline for lower AD Bus	Routing Guideline for upper AD Bus
Trace Length 1 TL1: 80333 signal Ball to 1st junction	1.0” minimum - 5.5” maximum	1.0” minimum - 5.5” maximum
Trace Length TL2 from 1st junction to 1st PCI connector	1.5 - 4.0” maximum	
Trace Length TL3 to TL5 between connectors	0.75” minimum - 1.5” maximum	1.75” minimum - 2.75” maximum
Length Matching Requirements	No length matching is required among datalines. For length matching for clocks, refer clock guidelines Table 9.	
Number of vias	Four vias maximum	

PCI Express Layout 7

This section provides an overview of the PCI-Express layout guidelines based on Intel's simulation results.

7.1 General Recommendations

PCI Express is a serial differential low-voltage point-to-point interconnect. The PCI Express was designed to support 20 inches between components with standard FR4.

For more information on the PCI Express standard refer to *PCI Express Base Specification 1.0a* and the *PCI Express Card Electromechanical Specification*, revision1.0a found on the www.pcisig.com website. The PCI Express was designed to support 20 inches between components with standard FR4.

7.1.1 Simulation Conditions

The following lists the conditions for 80333 PCI Express simulations listed in the section.

- Jitter and insertion loss budgets used as per PCIE Specifications
- AC coupling capacitors 75 nF with ESL and ESR
- Both receiver and transmitter eyes were evaluated for the PCI Express mask specifications and eye on the connector pin is evaluated for add-in card case.
- Modified worst case ISI pattern (8B/10B was used)
- Both near end and far end crosstalk were considered separately for system board topology and add-in topology.
- SSO impact was found to be negligible from power delivery simulations.
- PCI Express Layout Guidelines Intel® 80333 I/O Processor on the Motherboard

The following conditions and layout recommendations were determined for a motherboard application.

Figure 42. Motherboard Topology

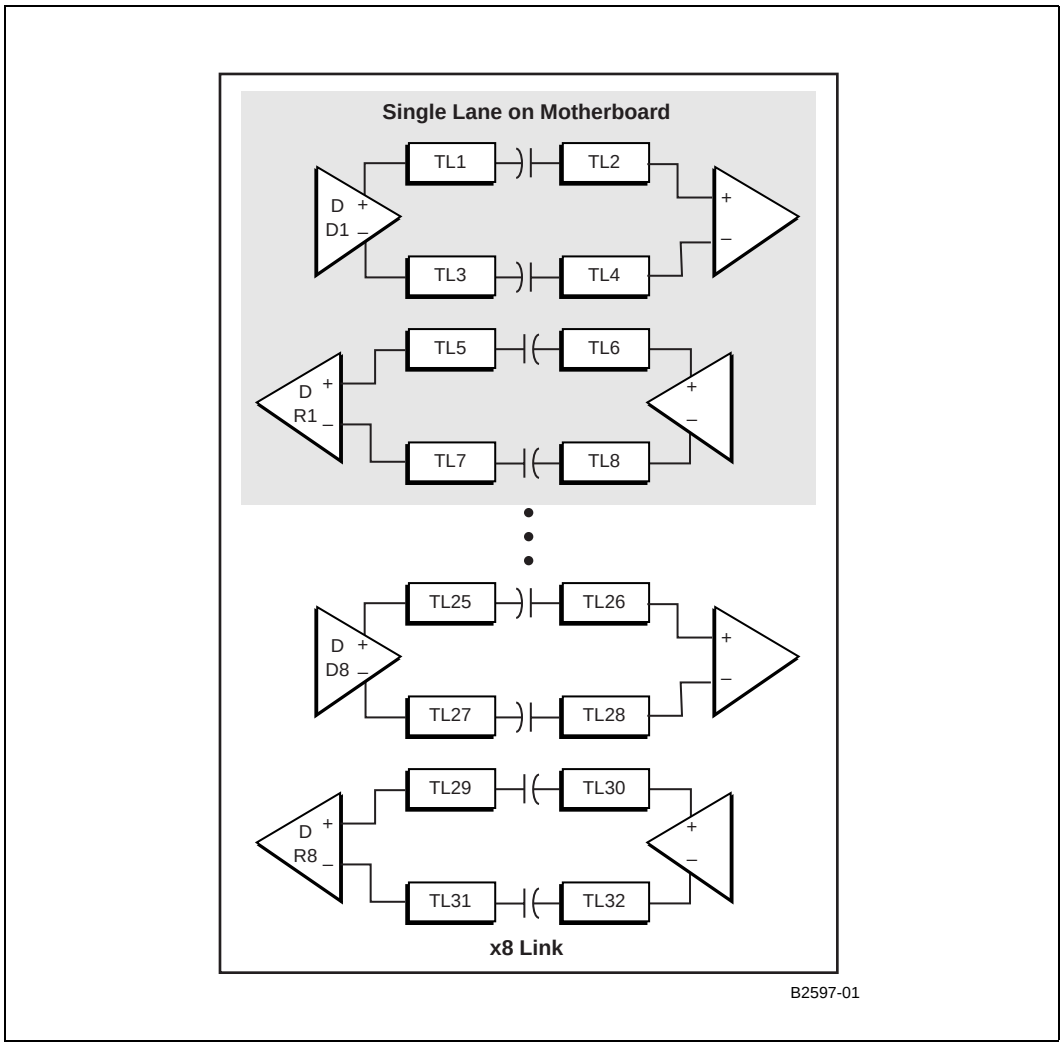


Table 30. PCI Express Layout for 80333 on the Motherboard

Parameter	Routing Guidelines
Signal Group	Transmit and Receive differential pairs
Reference Plane	Route over unbroken ground plane[2]
Target Single Ended microstrip trace impedance	50 ohms +/- 15%
Target Differential microstrip trace impedance	85 ohms nominal +/-15%
Microstrip Trace Width	5 mils
Microstrip Trace Spacing	• Intra pair: 12 mils center to center • Inter pair: ≥ 30 mils center to center • Transmit and Receive pairs should be interleaved. If interleaving not possible, then inter pair spacing should be increased to 50 mils (c2c). Center to center of inter pair is defined as center of Positive of one pair to Center of Negative of the next pair or vice versa
Stripline Trace Width	4 mils
Stripline Trace Spacing	• Intra pair: 10 mils center to center • Interpair: ≥ 30 mils center to center • Transmit and Receive pairs should be interleaved. If interleaving not possible, then inter pair spacing should be increased to 50 mils (c2c). Center to center of inter pair is defined as center of Positive of one pair to Center of Negative of the next pair or vice versa
Group Spacing	Spacing from other groups: ≥ 25 mils minimum from center to center
AC Coupling	AC Coupling capacitors must be located at the transmitter. Required value of 75 nF to 200 nF.s
Trace Length - (Transmitter/Receiver) device signal ball to AC coupling Capacitor	.25” min - 11.0” max
Trace Length - (Transmitter/Receiver) AC coupling capacitor to device pin	1.0” min - 13.85” max
Length Matching Requirements	• Per the PCI-E specification, total allowable intra-pair length mismatch on a system board must not exceed 10 mils. • Total allowable intra-pair trace mismatch for a lane that consists of a system board and an add-in card must not exceed 15 mils. • Length should be matched on a segment by segment basis. • Total skew across all lanes must be less than 20 ns. • Each routing segment to be matched as close as possible. • See the PCI-Express Desktop Design Guidelines for additional routing recommendations.
Number of Vias	4 max

NOTES:
1. Width and Intra Pair Spacing recommendations need not be strictly adhered to, but very important to meet the given differential target impedance and specified tolerance. It is also very important to follow the inter pair spacing recommendations.
2. If it is not possible to route over an unbroken ground plane then an unbroken power plane is acceptable. If it is necessary to use power plane, it is better to choose a reference power plane that is used by the I/O if possible. It is also recommended to decouple the I/O connector near the pins.

7.2 PCI Express Layout Guidelines for an 80333 on a Motherboard-Adapter Card Topology

This section provides the routing guidelines for the motherboard-adapter card topology as shown in Figure 43. Table 31 provides the routing guidelines for a motherboard (baseboard) with a PCI-Express connector on it and Table 32 provides the routing guidelines for the 80333 adapter card.

Figure 43. Motherboard-Adapter Card Topology

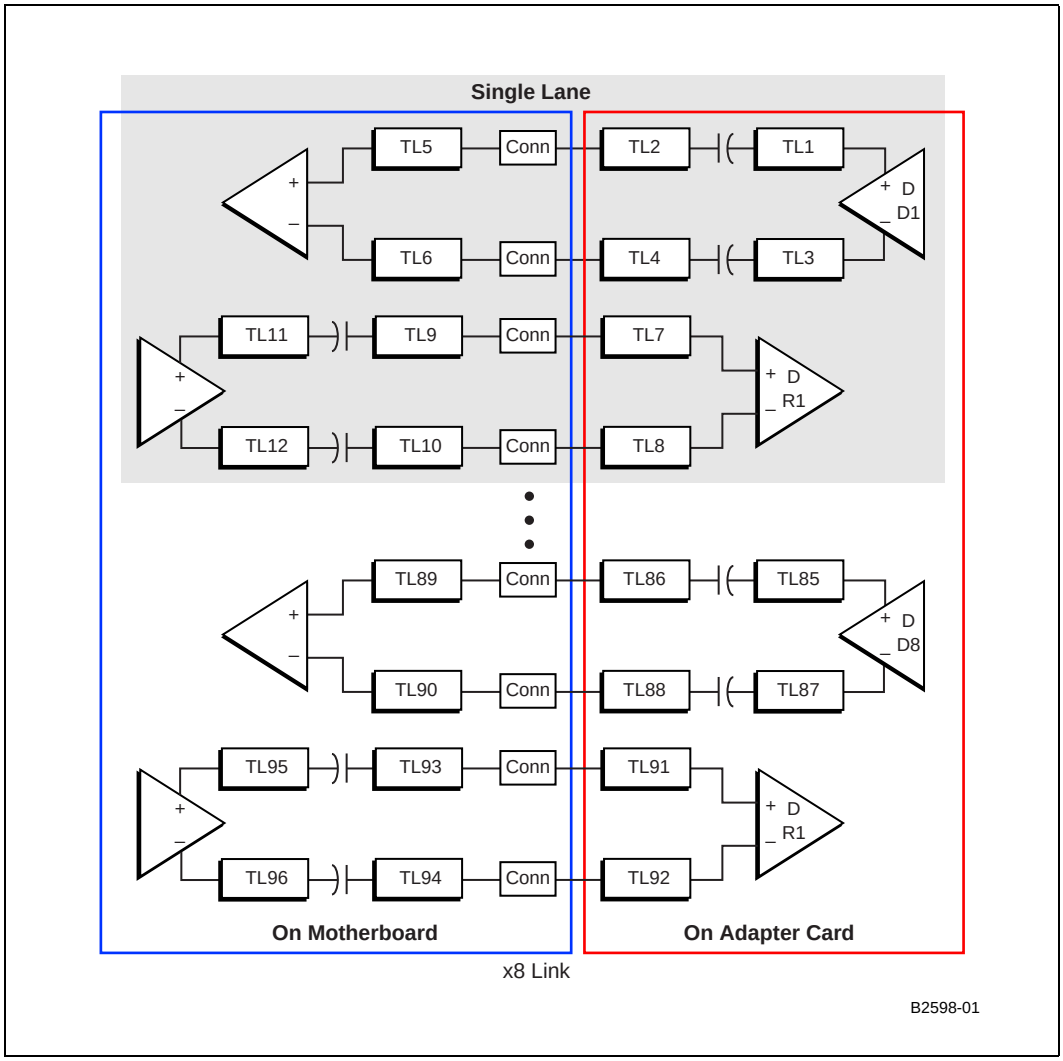


Table 31. PCI Express Layout for Baseboard Topology

Parameter	Routing Guidelines
Signal Group	Transmit and Receive differential pairs
Reference Plane	Route over unbroken ground plane [2]
Characteristic Trace Impedance	System/Baseboard: • Differential: 85 +/-15% ohms nominal • Single Ended: 50 +/-15% ohms nominal
Microstrip Trace Width	5 mils
Microstrip Trace Spacing	• Intra pair: 12 mils center to center (see Table Note) • Inter pair: ≥ 30 mils center to center • Transmit and Receive pairs should be interleaved. If interleaving not possible, then inter pair spacing should be increased to 50 mils (c2c). Center to center of inter pair is defined as center of Positive of one pair to Center of Negative of the next pair or vice versa
Stripline Trace Width	4 mils (see Table Note)
Stripline Trace Spacing	• Intra pair: 10 mils center to center • Interpair: ≥ 30 mils center to center • Transmit and Receive pairs should be interleaved. If interleaving not possible, then inter pair spacing should be increased to 50 mils (c2c). Center to center of inter pair is defined as center of Positive of one pair to Center of Negative of the next pair or vice versa
Group Spacing	Spacing from other groups: ≥ 25 mils minimum from center to center
Receive differential pair Trace Length	1.0” min - 15” max
Transmit differential pair - trace length from device signal ball to AC coupling capacitor	0.25” min - 7” max
Trace Length MB2 - AC coupling capacitor to connector pins	1.0” min - 10.0” max
Length Matching Requirements	• Per the PCI-E specification, total allowable intra-pair length mismatch on a system board must not exceed 10 mils. • Total allowable intra-pair trace mismatch for a lane that consists of a system board and an add-in card must not exceed 15 mils. • Length should be matched on a segment by segment basis. • Total skew across all lanes must be less than 20 ns. • See the PCI-Express Desktop Design Guidelines for additional routing recommendations.
Number of Vias	4 max

NOTES:
1. Width and Intra Pair Spacing recommendations need not be strictly adhered to, but very important to meet the given differential target impedance and specified tolerance. It is also very important to follow the inter pair spacing recommendations.
2. If it is not possible to route over an unbroken ground plane then an unbroken power plane is acceptable. If it is necessary to use power plane, it is better to choose a reference power plane that is used by the I/O if possible. It is also recommended to decouple the I/O connector near the pins.

Table 32. PCI Express Layout for 80333 Adapter Card Topology

Parameter	Routing Guidelines
Signal Group	Transmit and Receive differential pairs
Reference Plane	Route over unbroken ground plane [2]
Characteristic Trace Impedance	Adapter Card: • Differential: 100 +/-15% ohms nominal • Single Ended: 60 +/-15% ohms nominal
Microstrip Trace and Stripline Width	4 mils
Microstrip and Stripline Trace Spacing	• Intra pair: 10 mils center to center (see Table Note) • Inter pair: ≥ 30 mils center to center • Transmit and Receive pairs should be interleaved. If interleaving not possible, then inter pair spacing should be increased to 50 mils (c2c). Center to center of inter pair is defined as center of Positive of one pair to Center of Negative of the next pair or vice versa
Group Spacing	Spacing from other groups: ≥ 25 mils minimum from center to center
AC Coupling	AC Coupling capacitors must be located at the transmitter. Suggested value of 75 nF to 200 nF.
Receive Differential Pair Trace Length	1.0” min - 6.0” max
Trace Length Transmit Differential Pair- from device signal ball to AC coupling	0.25” min - 5.0” max
Trace Length Transmit Differential Pair - from AC coupling to connector pin	1.0” min - 4.5” max
Length Matching Requirements	• The total allowable intra-pair length mismatch on an add in card must not exceed 5 mils. • Total allowable intra-pair trace mismatch for a lane that consists of a system board and an add-in card must not exceed 15 mils. • Length should be matched on a segment by segment basis. • Total skew across all lanes must be less than 20 ns. • See the PCI-Express Desktop Design Guidelines for additional routing recommendations.”
Number of Vias	4 max

NOTES:
1. Width and Intra Pair Spacing recommendations need not be strictly adhered to, but very important to meet the given differential target impedance and specified tolerance. It is also very important to follow the inter pair spacing recommendations.
2. If it is not possible to route over an unbroken ground plane then an unbroken power plane is acceptable. If it is necessary to use power plane, it is better to choose a reference power plane that is used by the I/O if possible. It is also recommended to decouple the I/O connector near the pins.

7.3 Clock Routing Guidelines

This section provides routing guidelines for the PCI-Express Clocks in a 80333 application. The *PCI Express Card Electromechanical Specification Rev 1.0a* states that any terminations required by the clock are to be on the system board.

- The Figure 44 termination would only be required on the system board if these resistors were not already provided.
- PCI Express adapter cards do not have to add Rs, Rs' and Rt, Rt' termination resistors.

Figure 44. PCI Express Clock Routing Topology

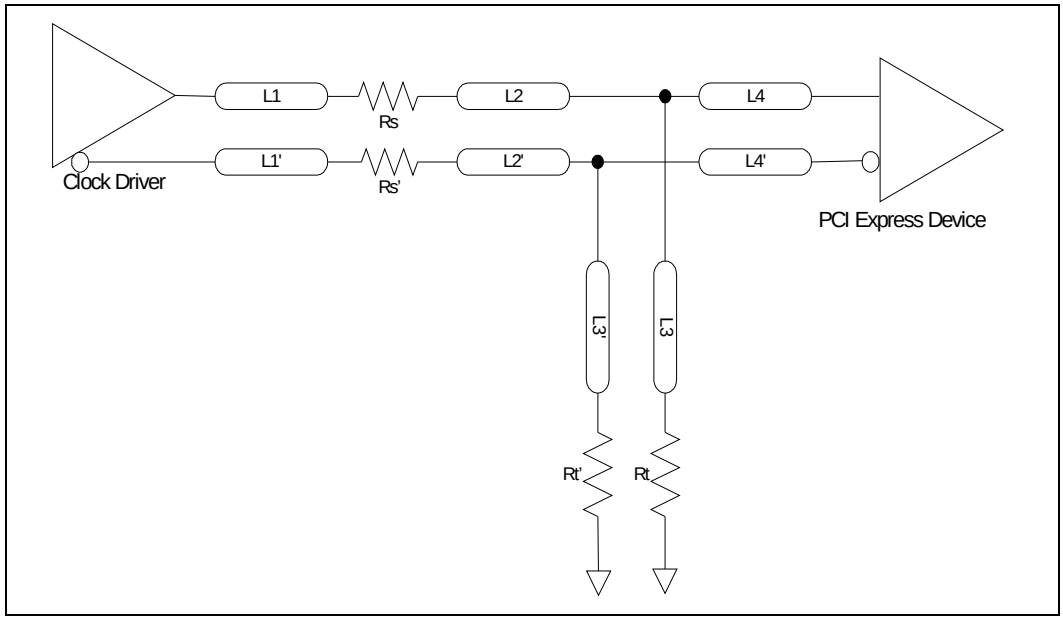


Table 33. PCI Express Layout for 80333 Adapter Card Topology

Parameter	Routing Guidelines
Signal Group	Transmit and Receive differential pairs
Reference Plane	Route over unbroken ground plane [2]
Characteristic Trace Impedance	Adapter Card: • Differential: 100 +/-15% ohms nominal • Single Ended: 50 +/-15% ohms nominal
Trace Width	5 mils (see Note 1)
Differential Clock Pair Spacing	< 1/4 x W (1.4 x Space Width)
Serpentine Spacing	≥ 25 mils
Clock to Other Signal Spacing	≥ 25 mils
Trace Lengths[1]	L1, L1' 0.5" max L2, L2' 0.2" max L3, L3' 0.2" max L4, L4': device down: 2" to 15.3" or Connector: 2" to 11.3" Total Length = L1+L2_+L4: Device Down: 3" to 16" or Connector: 3" to 12"
Serpentine Spacing	25 mils
Length Matching Requirements	+/- 5 mils
Rs Series Resistor [1]	33 +/- 5%
Rt Shunt Resistor [1]	49.9 +/- 1%
Number of Vias	4 max

NOTES:
1. [1] Termination resistors only required on system boards if not already present. Adapter cards do not require Rs and Rt resistors)
2. If it is not possible to route over an unbroken ground plane then an unbroken power plane is acceptable. If it is necessary to use power plane, it is better to choose a reference power plane that is used by the I/O if possible. It is also recommended to decouple the I/O connector near the pins.
3. Width and Intra Pair Spacing recommendations need not be strictly adhered to, but it is very important to meet the given differential target impedance and specified tolerance. It is also very important to follow the inter pair spacing recommendation

Memory Controller 8

The Memory Controller allows direct control of a DDR SDRAM memory subsystem. It features programmable chip selects and support for error correction codes (ECC). The memory controller can be configured for DDR SDRAM at 333 MHz and DDR-II at 400MHz. The memory controller supports pipelined access and arbitration control to maximize performance. The memory controller interface configuration support includes Unbuffered DIMMs, Registered DIMMs, and discrete DDR SDRAM devices.

External memory can be configured as host addressable memory or private 80333 memory utilizing the Address Translation Unit and Bridges.

8.1 DDR Bias Voltages

The 80333 supports 2.5 V DDR memory and 1.8V for DDRII. Table 34 lists the minimum/maximum values for the DDR memory bias voltages and Table 35 lists the minimum/maximum values for the DDR II memory bias voltages.

Table 34. DDR Bias Voltages

Symbol	Parameter	Minimum	Maximum	Units
V_{CC25}	**2.5 V Power** balls to be connected to a 2.5 V power board plane.	2.3	2.7	V
V_{DDQ}	I/O Supply Voltage	2.3	2.7	V
V_{REF}	Memory I/O Reference Voltage	V_{CC25} /2 - 0.05	V_{CC25} /2 + 0.05	V
V_{TT}	DDR Memory I/O Termination Voltage	V_{REF} - 0.04	V_{REF} + 0.04	V

Table 35. DDR II Bias Voltage

Symbol	Parameter	Minimum	Maximum	Units
V_{CC18}	**1.8 V Power** balls to be connected to the 1.8 V power board plane.	1.7	1.9	V
V_{DDQ}	I/O Supply Voltage	1.7	1.9	V
V_{REF}	Memory I/O Reference Voltage	V_{CC18} /2 - 0.05	V_{CC18} /2 + 0.05	V
V_{TT}	DDR Memory I/O Termination Voltage	V_{REF} - 0.04	V_{REF} + 0.04	V

8.2 Intel® 80333 I/O Processor DDR Overview

80333 with the DDR-SDRAM memory sub-system needs continuous ground referencing for all DDR signals. The DDR channel requires the referencing stack-up to allow ground referencing on all of the DDR signals from the 80333 to the parallel termination at the end of the channel.

Note: Leave unused M_CKs and M_CK#s unconnected.

The 80333 signal integrity specifications are for a single DIMM only for both DDR333 and DDR II 400. The DIMM topology supported for the recommendations listed in this section are for x8 single / double banks and x16 single/double banks.

DDR333 = single DIMM and supports both Buffered / Unbuffered DIMM

DDRII 400 = single DIMM and supports Buffered DIMM

Table 36 details the 80333 Core Speed and DDR/DDRII memory configuration.

Table 36. Core Speed and Memory Configuration

Core/DDR	DDR333	DDR-II 400
Low	500MHz	500MHz
Medium	667MHz	N/A
High	N/A	800MHz

The DDR interface is divided up into three groups that each have special routing guidelines:

- Source synchronous signal group: DQ/DQS/DQM/CB signals
- Clocked: M_CK signals
- Control signals: Address/RAS/CAS/CS/WE/CKE signals

8.3 DDR 333 Signal Integrity Simulation Conditions

- Motherboard 50 ohm single ended impedance stackup +/- 15% tolerance.
- Add-in Card 60 ohm single ended impedance stackup +/- 15% tolerance.
- Clock Target Differential Impedance 100 ohms and 50 ohms single-ended impedance.
- Memory Model Micron T17A_DQ and Intel generic models.
- PLL Clock - Pericom* CDCBV857, PI6DCV16859.
- DIMM models and topologies used the JEDEC model as a reference.
- For unbuffered embedded and post PLL/register the standard recommendations were used as a reference.
- Spacing recommendations are for trace edge to edge except for differential pairs in which center to center was specified.
- Signal Quality analysis covered for Rising flight time, Falling flight time, Low to high ring-back (noise margin high), High to Low ring-back (noise margin Low), and Low and High Overshoot.
- Crosstalk Analysis was performed for all the major interfaces with actual package models.
- Frequency: 167MHz (DDR 333 MT/s).
- Connector –E SPICE of DIMM Connector (Derived from SPICE Circuit)
- Package - Actual extracted Package Model used.

The topologies simulated are listed in Table 37.

Table 37. Simulated DDR 333 Topologies

DIMM	Embedded
1. DQ/DQS • Read- RAW A, RAWB • Write -RAW A, RAW B	1. DQ/DQS • Read- Single Bank • Write - Single Bank
2. Clock • Buffered • Unbuffered	2. Clock • Buffered • Unbuffered • Post-PLL • PLL to SDRAM • PLL to Register • PLL to Feedback
3. Address/CMD • Registered • Unbuffered - RAWA, RAWB	3. Address/CMD • Registered • Unbuffered - Single bank ECC and non ECC • Post Register - single bank ECC and non ECC

8.3.1 DDR 333 Stackup Example

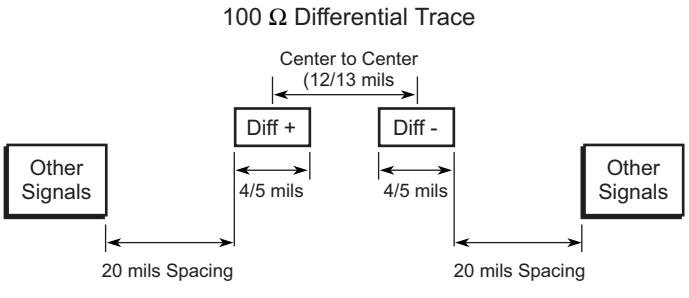
Table 38 below provides an example of a table of recommended topologies for motherboard and add-in card eight layer PCB designs. Figure 45 provides an example of a cross section used to implement 100 ohm differential trace impedance.Throughout this section the important recommendation to meet is the trace impedance. The example in Table 38 is provided as a reference.

Table 38. Example Topologies for DDR Trace

Topology	Trace Width (mils)	Min Trace Spacing (mils)	Trace Impedance (ohms)	Preferred signals	Board Type
Microstrip (layers 1 or 8)	5	5		Breakout	Motherboard/Add-in
	7	12	45	Address/ CMD/Control	Motherboard/Add-in
	6	12	50		Motherboard/Add-in
	4	12	60		Motherboard/Add-in
	5 (note 1)	20	100 differential	Differential Clock/DQS	Motherboard/Add-in
Stripline (layers 3 or 6)	5	5		Break out	Motherboard/Add-in
	6	12	45	DQ/DQS/CB	Motherboard
	5	12	50		Motherboard card
	7	12	45	DQ/DQS/CB	Add-in card
	6	12	50		Add-in card
	4	12	60		Add-in card
	4 (note 2)	20	100 Ohm	Differential Clocks	Motherboard*
	5 (note 3)	20	100 Ohm	Differential Clock	Add-in card*

1. Microstrip Differential Lines: Motherboard/Add-in 100 ohm: Constructed by two microstrips of 5 mils traces separated by center to center distance of 13 mils as shown in Figure 45.
2. Strip Differential Lines: Motherboard Stripline 100 ohms: Constructed by two striplines of 4 mils traces separated by center to center distance of 12 mils as shown in Figure 45.
3. Strip Differential Lines: Add-in stripline 100 ohms: Constructed by two striplines of 4 mils traces separated by center to center distance of 13 mils as shown in Figure 45.

Figure 45. 100 ohm Differential Trace



8.4 DDR Layout Guidelines

The following sections provide layout information for 80333 DDR333 configuration.

8.4.1 Source Synchronous Signal Group

The guidelines below are for the source synchronous signal group which includes Data bits **DQ**, check bits **CB**, data mask **DM**, and **DQS** associated strobe.

The 80333 source synchronous signals are divided into groups consisting of data bits **DQ** and check bits **CB**. There is an associated strobe **DQS** for each **DQ**, **DM** and **CB** group. When data masking is not used system memory **DM** pins on the DDR needs to be tied to ground. The grouping is as follows for the different memory configurations:

Table 39. x64 DDR Memory Configuration

Data Group	Associated Strobe
DQ[7:0], DM[0]	**DQS0**
DQ[15:8], DM[1]	**DQS1**
DQ[23:16], DM[2]	**DQS2**
DQ[31:24], DM[3]	**DQS3**
DQ[39:32], DM[4]	**DQS4**
DQ[47:40], DM[5]	**DQS5**
DQ[55:48], DM[6]	**DQS6**
DQ[63:56], DM[7]	**DQS7**

Table 40. x72 DDR Memory Configuration

Data Group	Associated Strobe
DQ[7:0], DM[0]	**DQS0**
DQ[15:8], DM[1]	**DQS1**
DQ[23:16], DM[2]	**DQS2**
DQ[31:24], DM[3]	**DQS3**
DQ[39:32], DM[4]	**DQS4**
DQ[47:40], DM[5]	**DQS5**
DQ[55:48], DM[6]	**DQS6**
DQ[63:56], DM[7]	**DQS7**
CB[7:0], **DM[8]**	**DQS8**

8.4.1.1 Routing Requirements

Table 41 and Table 42, and Figure 48 and Figure 46 show the routing and termination requirements for the source synchronous signal group.

Table 41. Source Synchronous Termination Requirements

DDR SDRAM	R Series	R Parallel
	22.1 +/- 5% ohms	51.1 +/- 5% ohms

Table 42. Source Synchronous Routing Recommendations (Sheet 1 of 2)

Parameter	Routing Guideline
Reference Plane	Stripline: Route over unbroken ground plane Microstrip Routing: Route over unbroken power or ground plane
Preferred Layer	Stripline
Topology	Stripline (stubs needs to be <250 mils)
Breakout	5 mils x 5 mils Maximum length of breakout region of 500 mils.
Strip line Trace Impedance	45 ohms +/- 15% OR 50 OHMS +/- 15%.
Strip Line Trace Spacing (trace edge to neighbor trace edge)	• 5 mils spacing acceptable between pins and breakout regions • >12 mils edge to edge between any DQ/DQS signals • > 20 mils (edge to edge) maintained from any other groups
Trace Lengths	Refer to DIMM DQ/DQS Topology Figure 46 and Figure 47
DQ Group Spacing	Spacing from other DQ groups 20 mils minimum
Series Resistor Rs	22.1 Ω +/- 5%
Parallel Termination	• Single VTT termination of 51.1 Ω +/- 5% to VTT (1.25V) or • Split terminations of 100 ohms +/- 5% to 2.5V and 100 ohms +/- 5% to ground. • Place the VTT termination in a VTT island.
Length Matching Requirements: within DQS Group	+/- 0.050” within DQS group
Length Matching Requirements: All DQ/DQS lines to Clock	• The package lengths from Die to Ball provided in Table 44 must be accounted for when length matching • When M_CK is routed on a stripline layer, DQS should be routed to within +/- 1.5” of its corresponding M_CK • When M_CK is routed on a micro-strip layer, DQS should be routed to within +/- 1.0” of its corresponding M_CK
Routing Guideline 1	Route all data signals and their associated strobes on the same layer.

Table 42. Source Synchronous Routing Recommendations (Sheet 2 of 2)

Parameter	Routing Guideline
Routing Guideline 2	Minimize layer changes (two vias or less)
Routing Guideline 3	Do not share series terminator resistor packs between DQ/DQS and Address.
Number of Vias	2 (Equal number of vias between DQ and its respective DQS signal)

Table 43. DIMM DQ/DQS Topology Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL1	Breakout	Microstrip		0.5”		5 mils	
TL2	Lead-in	Microstrip	2 “	8”	45 ohms +/- 15% or 50 ohms +/- 15%	12 mils	Lead-in traces are preferred as striplines.
TL3		Microstrip	0.25”	0.5”	Same as TL2		Fan out for series termination
TL4	Vtt	Microstrip	0.15	0.5”		5 mils	Vtt Termination

Table 44. Die to Ball Internal Lengths

Signal Description	Lengths (mils)
BA[0]	366.64
BA[1]	400.1
CAS#	435.86
CB[0]	576.97
CB[1]	576.96
CB[2]	576.99
CB[3]	576.99
CB[4]	577.86
CB[5]	576.95
CB[6]	577
CB[7]	577.9
CKE[0]	768.12
CKE[1]	788.7
CS[0]#	432.83
CS[1]#	482.04
DDR_VREF	1287.52
DDRCRES0	602.21
DDRIMPCRES	674.9
DDRRES[1]	648.04
DDRRES[2]	751.97
DDRSLWCRES	600.29
DM[0]	800.63
DM[1]	940.23
DM[2]	674.86
DM[3]	651.68
DM[4]	651.68
DM[5]	702

Table 44. Die to Ball Internal Lengths

Signal Description	Lengths (mils)
DM[6]	805.36
DM[7]	767.5
DM[8]	577.92
DQ[0]	801.6
DQ[1]	801.46
DQ[10]	940.14
DQ[11]	939.24
DQ[12]	939.27
DQ[13]	939.28
DQ[14]	940.03
DQ[15]	940.19
DQ[16]	674.37
DQ[17]	675.08
DQ[18]	674.24
DQ[19]	674.44
DQ[2]	801.58
DQ[20]	674.16
DQ[21]	674.67
DQ[22]	674.2
DQ[23]	675.04
DQ[24]	652.55
DQ[25]	652.64
DQ[26]	651.67
DQ[27]	651.72
DQ[28]	652.1
DQ[29]	652.61
DQ[3]	800.66
DQ[30]	652.08
DQ[31]	652.58
DQ[32]	651.65
DQ[33]	650.81
DQ[34]	651.69
DQ[35]	650.74
DQ[36]	650.74
DQ[37]	651.71
DQ[38]	650.76
DQ[39]	650.73

Table 44. Die to Ball Internal Lengths

Signal Description	Lengths (mils)
DQ[4]	800.6
DQ[40]	701.56
DQ[41]	702.02
DQ[42]	701.74
DQ[43]	702.25
DQ[44]	701.86
DQ[45]	702.01
DQ[46]	702.03
DQ[47]	701.93
DQ[48]	806.13
DQ[49]	805.43
DQ[5]	800.63
DQ[50]	805.88
DQ[51]	805.96
DQ[52]	806.17
DQ[53]	806.17
DQ[54]	805.54
DQ[55]	805.34
DQ[56]	767.47
DQ[57]	767.45
DQ[58]	768.35
DQ[59]	767.46
DQ[6]	800.62
DQ[60]	767.48
DQ[61]	767.47
DQ[62]	767.63
DQ[63]	767.51
DQ[7]	800.63
DQ[8]	940.16
DQ[9]	940.15
DQS[0]	801
DQS[1]	939.25
DQS[2]	674.68
DQS[3]	652.66
DQS[4]	650.81
DQS[5]	701.98
DQS[6]	805.94

Table 44. Die to Ball Internal Lengths

Signal Description	Lengths (mils)
DQS[7]	767.45
DQS[8]	576.94
DQS[0]#	800.66
DQS[1]#	939.23
DQS[2]#	675.03
DQS[3]#	652.62
DQS[4]#	650.75
DQS[5]#	701.68
DQS[6]#	806.15
DQS[7]#	767.44
DQS[8]#	577.9
M_CK[0]	616.41
M_CK[0]#	616.27
M_CK[1]	762.67
M_CK[1]#	762.65
M_CK[2]	597.08
M_CK[2]#	597.24
M_RST#	760.27
WE#	403.92
RAS#	290.55
MA[0]	326.8
MA[1]	447.68
MA[10]	352.22
MA[11]	390.14
MA[12]	620.5
MA[13]	485.18
MA[2]	338.39
MA[3]	483.4
MA[4]	505.56
MA[5]	629.68
MA[6]	634.85
MA[7]	403.63
MA[8]	638.37
MA[9]	393.04
ODT[0]	372.29
ODT[1]	224.37

Figure 46. DIMM DQ/DQS Topology

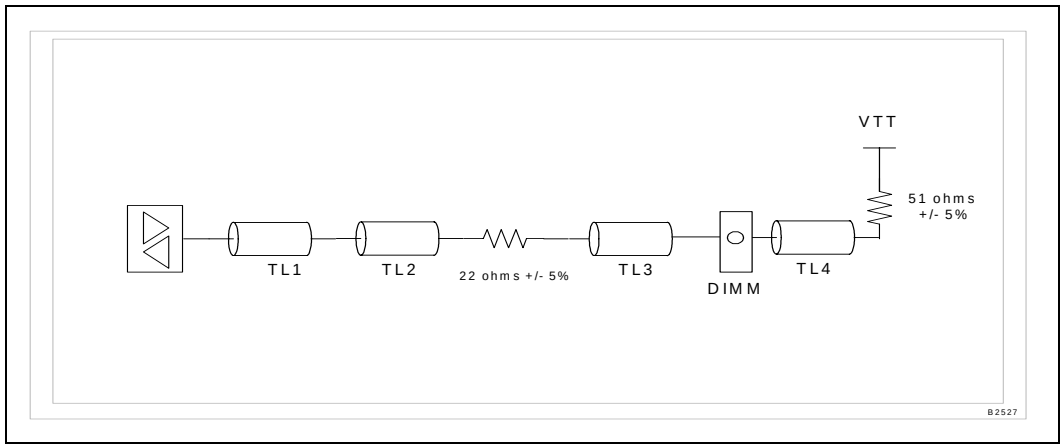


Table 45. DIMM DQ/DQS Split Termination Topology Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL1	Breakout	Microstrip/ Stripline		0.5”		5 mils	
TL2	Lead-in	Microstrip	2 “	8”	45 ohms +/- 15% or 50 ohms +/- 15%	12 mils	Lead-in traces are preferred as striplines.
TL3		Microstrip	0.25”	0.5”	Same as TL2		Fan out for series termination
TL4	Vtt	Microstrip	0.15	0.5”		5 mils	Split termination

Figure 47. DIMM DQ/DQS Split Termination Topology

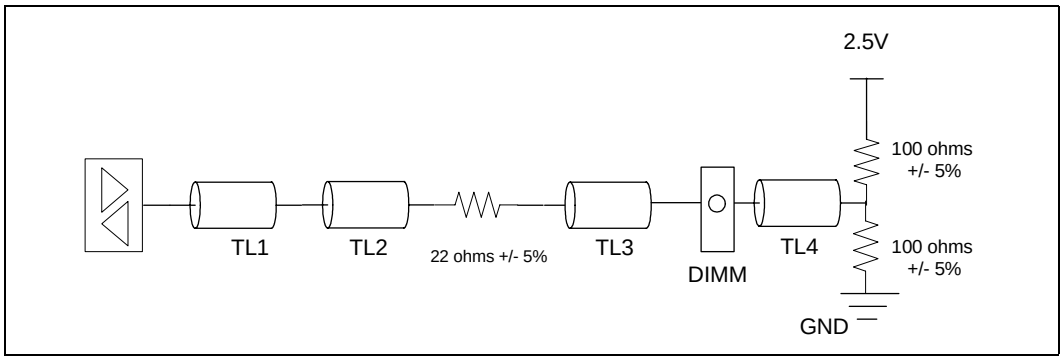


Figure 48. Source Synchronous Length Matching

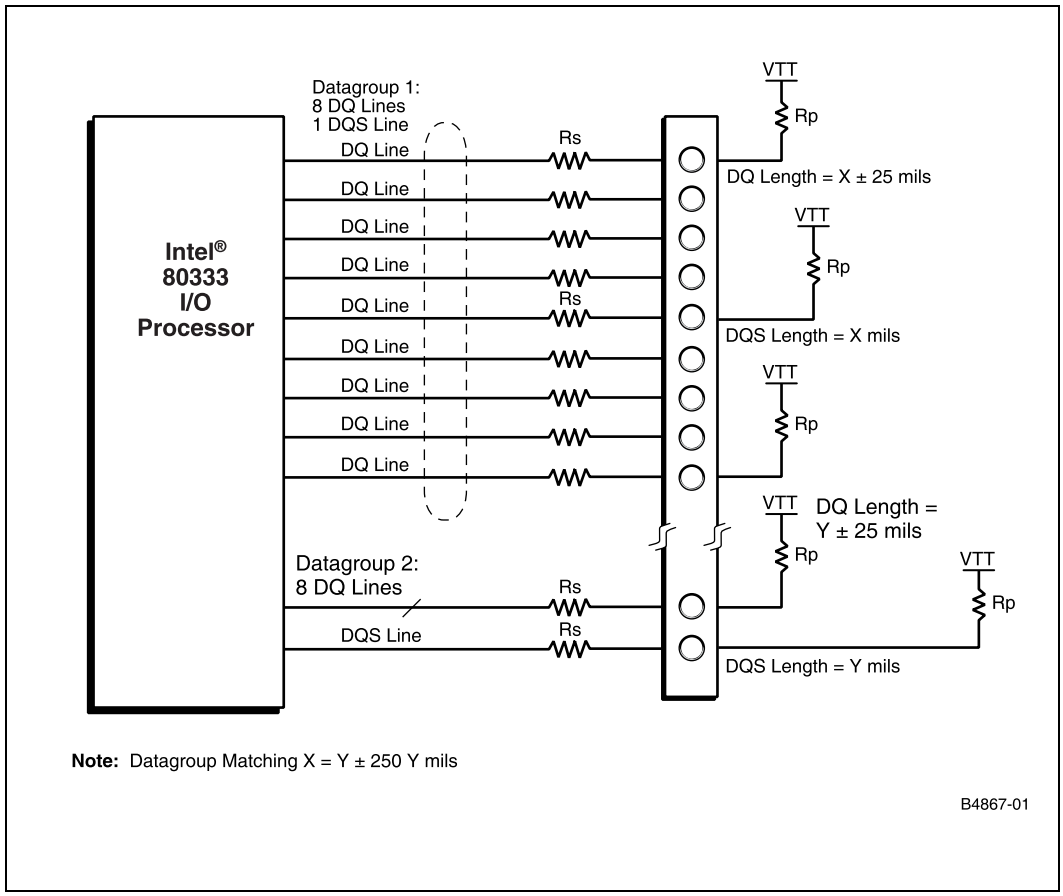
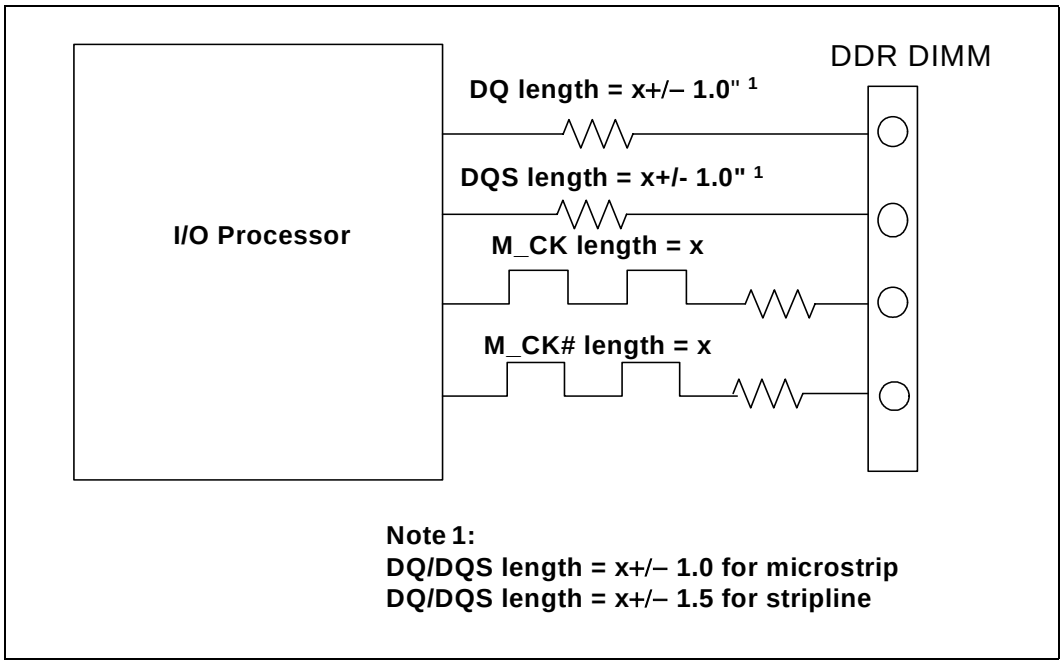


Figure 49. Data Group Length Matching



8.4.2 Clock Signal Groups

The 80333 drives the command clock signals required by the DDR interface. The source-clocked signals are “clocked” into the DIMM using the command clock signals. The 80333 drives the command clock signals and the source-clocked signals together, these signals can be source clocked. The 80333 drives the command clock in the center of the valid window, and the source-clocked signals propagate with the command clock signal. An important timing specification is the difference between the command clock flight time and the source clocked signal flight time. The absolute flight time is not as critical.

The common clock signal group contains **M_CK[2:0]** and **M_CK[2:0]#**. The following tables and figure show the routing requirements for the clock signal group.

Table 46. DIMM Clocked Signal Group Termination

DDR SDRAM	Rs Series	Rp Parallel
	22.1 +/- 5% ohms (non-buffered DDR only)	none

Table 47. Clock Signal Group Registered/Unbuffered DIMM Routing Requirements

Parameter	Routing Guideline
Reference Plane Preferred Topology	Route over unbroken ground plane Differential Microstrip (preferred) or differential stripline
Preferred Topology	Stripline routing is recommended for the clock signals. Micro-strip is also acceptable with strict adherence to all routing recommendations.
Breakout trace width and spacing	5 mils x 5 mils routed as differential pair
Microstrip Trace Width	Differential: Trace impedance of 100 ohms Refer to Figure 48
Trace Spacing (edge to edge)	5 mils for breakout 5 mils from one clock M_CK of the differential pair M_CK#. >20 mils between the other signals or vias including other clock pairs.
Package Trace Length Breakout Trace Length (TL1) Lead-in to Connector Length (TL2)	See Table 44 for the net length details. <= .5” 2.0” to 10” (correlated within +/- 1.0” of DQ/DQS and command trace lengths)
Termination: - Buffered Termination - Un-Buffered Termination	 None required 22.1 ohms +/- 5% series termination on each differential segment after the breakout.
Length matching Requirements:	The package lengths from Die to Ball provided in Table 44 must be accounted for when length matching
• Within differential clock pairs	• +/- 0.025” max. within Pairs [Intra-pair]
• With respect to the DQ/DQS group (from die to DIMM connector)	• +/- 1.5” max. when M_CK is routed Stripline • +/- 1.0” max. when M_CK is routed Micro-strip
• With respect to Address/Command group (from die to DIMM connector)	• For total capacitive loads greater than 36pF, M_CK trace lengths must be 2.0” to 3.0” longer than all ADD/CMD/CTRL trace lengths • For capacitive loads less than or equal to 36pF, M_CK trace lengths must be 1.0” to 3.0” longer than all ADD/CMD/CTRL trace lengths
• Among Unbuffered Clock Pairs	• +/- 0.1” max. between the 3 pairs of Unbuffered Clocks
Series Resistor Rs	• 22.1 +/- 5% ohms unbuffered • no series resistor required for registered DIMM’s
Parallel Resistor Rp	• no parallel resistor required
Routing Guideline 1	Clock signals’ polarity needs to be alternated.
Routing Guideline 2	Maximum of 2 pair of vias from controller to DIMM
Routing Guideline 3	Route clock as differential impedance of 100 ohms with single ended impedance of 50 ohms

Table 48. Registered DIMM Clock Topology Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL1	Breakout	Microstrip		0.5”		5 mils	5 mils trace width OK for breakout.
TL2	Lead-in	Microstrip	2 “	10”	Differential Impedance 100 ohms +/- 15%	20 mils from others	Route as differential pairs

Figure 50. DDR 333 Registered DIMM Clock Topology

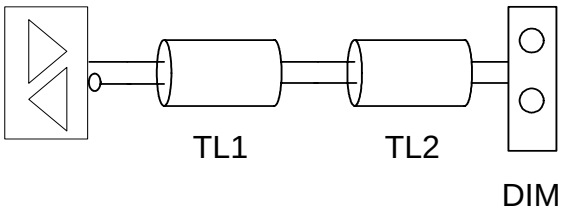


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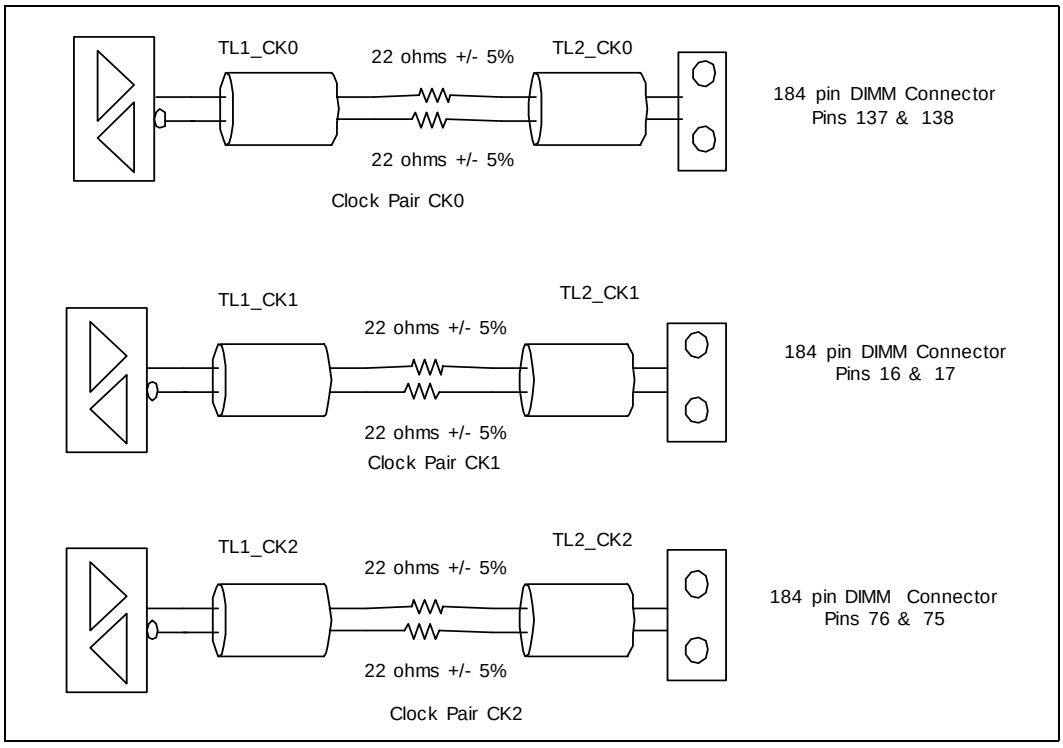
Table 49. DDR 333 Unbuffered DIMM Clock Topology Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL1 (all 3 clock pairs)	Breakout	Microstrip		0.5”		5 mils	5 mils trace width OK for breakout.
TL2 (all 3 x clock pairs)	Lead-in	Microstrip/ Stripline	2 “	10”	Differential Impedance 100 ohms +/- 15%	20 mils from others	• Route as differential pairs. • Series termination of 22 ohms +/- 5%.

NOTE: Length matching should be done from die to DIMM connector
1. Between intra pairs +/- 25 mils
2. Between clock pairs M_CK0, M_CK1, M_CK2 +/- 100mils on unbuffered clocks
3. DQS lengths are within +/- 1.5 “ max. of MCK for stripline
4. DQS lengths are within +/- 1.0 “ max. of MCK for stripline
5. Address/Command/Control lengths are with-in 2” to 3” less than MCK
6. Any address/command/control lengths greater than M_CK from die to DIMM is not guaranteed for x2 bank unbuffered configurations.

Figure 51. DDR 333 Unbuffered DIMM Clock Topology



8.4.2.1 Control Signals Termination

The control signal group includes **RAS#**, **CAS#**, **WE#**, **BA[1:0]**, **MA[12:0]**, **CS[1:0]#, and CKE[1:0]**. The series and parallel termination is shown in Table 50.

Table 50. Source Clocked Signal Routing

DDR SDRAM	Rs Series	Rp Parallel
		51.1 +/- 5% ohms

8.4.2.1.1 Control Signal Routing Guidelines

Figure 52 and Table 51 provide the routing guidelines for the source clocked group of signals.

Figure 52. Trace Length Requirements for Source Clocked Routing

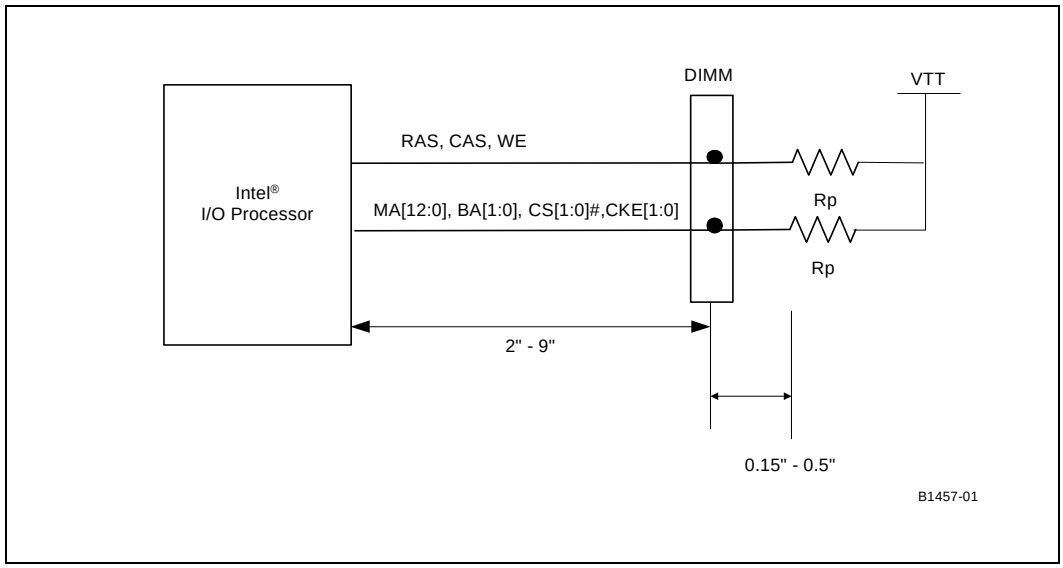


Table 51. Control Signals Routing Guidelines

Parameter	Routing Guideline
Reference Plane	Route over unbroken ground plane is preferred. (Refer to Table for alternatives if this is not feasible).
Preferred Topology	Micro-strip only for Un-buffered memory configurations Either Micro-strip or Stripline for Buffered DIMMs and lightly loaded Un-buffered DIMMs (i.e. single bank or dual bank w/ less than or equal to 36pF input capacitance).
Breakout Trace WIdth and Spacing	5 mils x 5 mils acceptable through pin field and terminations
Trace Impedance	• 45 ohms Motherboard/Add-in card impedance • 50 ohms Motherboard/Add-in Card Impedance
Strip Line Trace Spacing (edge to edge)	• Spacing within group 12 mils minimum • 5 mils acceptable through pin field and terminations • > 20 mils from the Clock/DQ/DQS groups
Series Resistor Rs	No series termination required
Parallel Resistor Rp	51.1 +/- 5% ohms OR Split termination of 100 ohms +/- 5% terminated to 2.5V and 100 ohms +/- 5% terminated to ground Place Vtt terminations in a Vtt island after the DIMM
Package Trace Length: Breakout Trace Length (TL1): Lead-in to Connector Trace Length (TL2): Parallel Termination Route Length (TL3):	See Table 44 for package net length report and Table 52 for more details. ≤ 0.5” 2.0” to 9.0” 0.15” to 0.5”
Length Matching Requirements:	The package lengths from Die to Ball provided in Table 44 must be accounted for when length matching For total capacitive loads greater than 36pF, all ADD/CMD/CTRL trace lengths must be 2.0” to 3.0” shorter than M_CK’s trace length For total capacitive loads less than or equal to 36pF, all ADD/CMD/CTRL trace lengths must be 1.0” to 3.0” shorter than M_CK’s trace length
Routing Guideline 1	Route these signals on the same layer as the M_CKs.
Routing Guideline 2	Minimize layer changes (two vias or less)

Figure 53. DDR 333 DIMM Unbuffered/Registered Address/CMD Topology Lengths

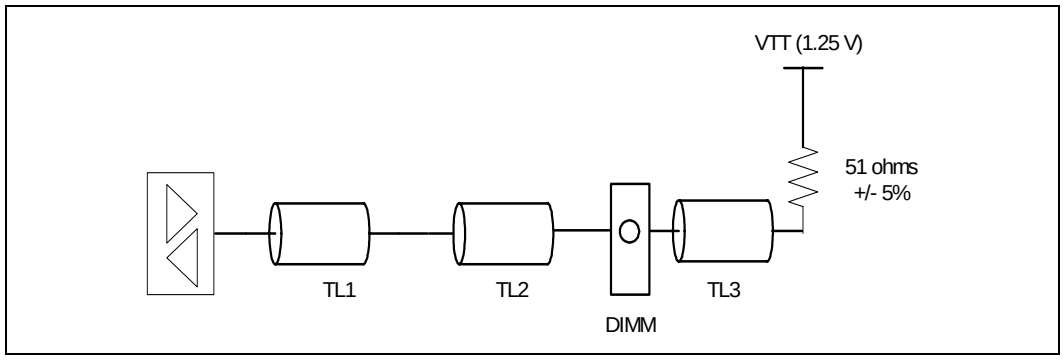


Table 52. Control Signal DIMM Topology Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL1	Breakout	Microstrip or stripline		0.5”	-	5 mils	5 mils trace width OK for breakout.
TL2	Lead-in	Microstrip	2 “	8.5”	45ohms +/- 15% 50 ohms +/- 15%	12 mils from others	• Within the same group >12 mils • Any of the other groups (DQ/DQS/Clock) > 20 mils
TL3	Vtt (preferred) or Split Termination	Microstrip	0.15”	0.5”	-	5 mils	Single VTT termination in VTT island is preferred.

8.4.3 Embedded Configuration

The following tables provide layout guidelines for applications in which the DDR 333 memory SDRAM components are placed directly on the board without a DIMM.

8.4.3.1 DDR 333 Source Synchronous Routine Guidelines

This section lists the recommendations for the DDR 333 embedded source synchronous routing. These signals include all the DQ/DQS signals. Refer to Table 53 and Table 54 for the lengths and matching requirements and Figure 54 for the topology diagram. The topologies simulated are listed in Table 37.

Table 53. DDR 333 Embedded Source Synchronous Routing Recommendations (Sheet 1 of 2)

Parameter	Routing Guideline
Reference Plane	Stripline routing: Route over unbroken ground plane Micro-strip routing: Route over unbroken ground or power plane
Preferred Topology	Stripline. Simulations show that stripline routing of the DQ and DQS signals provides the best solution space. Micro-strip routing is also acceptable.
Breakout Termination, Fan-in and Fanout width and spacing	5 mils x 5 mils. Microstrip is recommended for pin escapes and terminations.
Trace Impedance	• 45 ohm +/- 15% or • 50 ohms +/- 15%
Trace Spacing (trace edge to edge)	• 5 mils is acceptable for pin escapes and fan-in/fan-out from terminations. • >12 mils between any DQ/DQS signals • >20 mils bust be maintained from any other groups
Package Trace Length:	The package lengths from Die to Ball provided in Table 44 must be accounted for when length matching. Refer to Table 54 for more details on segment lengths.
• Breakout Trace Length (TL1)	≤ 0.5”
• Lead-in to Series Term. Trace Length (TL2)	1.0” to 4.0”
• Fan-in/ Fan-out from Series Termination Trace Length (TL3 & TL4)	≤ 0.1”
• Parallel Termination Trace Length (TL5)	0.15” to 0.5” (placed directly after series termination fan-in)
• Lead-in to SDRAM (TL6)	1.0” to 4.0”
Length Matching:	• The package lengths from Die to Ball provided in Table 44 must be accounted for when length matching.
• With respect to the clock signal	• When M_CK is routed on a stripline layer, DQS should be routed to within +/- 1.5” of its corresponding M_CK • When M_CK is routed on a micro-strip layer, DQS should be routed to within +/- 1.0” of its corresponding M_CK
• Length Matching within DQS group	• +/- .05” within DQS group
Series Termination	22 ohms +/- 5%

Table 53. DDR 333 Embedded Source Synchronous Routing Recommendations (Sheet 2 of 2)

Parameter	Routing Guideline
Parallel Termination	51 ohms +/- 5% • Place the VTT terminations in VTT island after the DIMM (trace length of 0.15” to 0.5”). or • Split termination of 100 ohms +/- 5% to 2.5 V and 100 ohms +/- 5% to ground
Routing Guideline 1	Route all data signals and their associated strobes on the same layer.
Routing Guideline 2: Vias	≤ 2 Minimize layer changes especially DQS signals. (two vias or less). Equal number of vias between DQ and its respective DQS signal.

Figure 54. Embedded DDR 333 DQ/DQS Topology

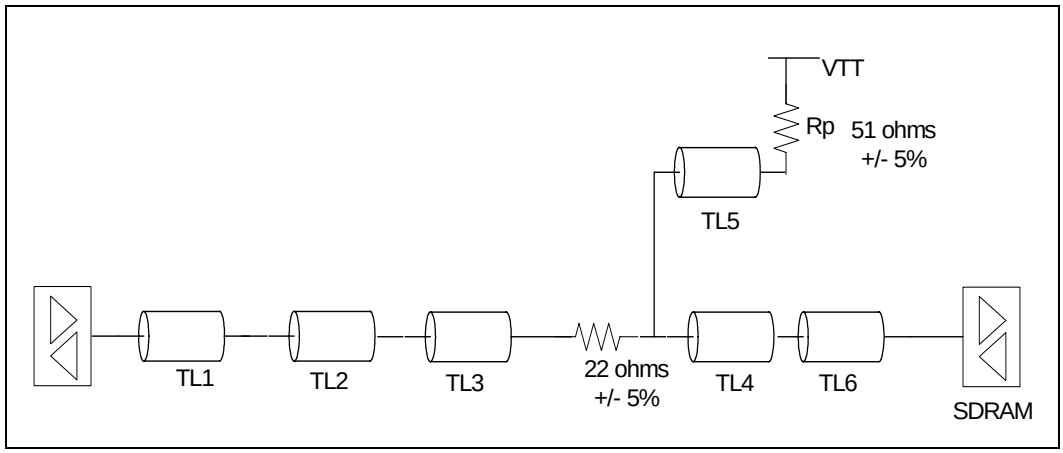


Table 54. Embedded DDR 333 DQ/DQS Topology Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL1	Breakout	Microstrip/ Stripline	0”	0.5”	-	5 mils	5 mil trace width breakout OK
TL2	Lead-in	Stripline	1 “	4”	45 ohms +/- 15% or 50 ohms +/- 15%	12 mils	• WIthin the same group >12 mils • Any other groups (DQ/DQS/Clock) >20 mils
TL3		Microstrip	0”	0.1”	-	5 mils	Fan out for series termination
TL4		Microstrip	0”	0.1”	-	5 mils	Fan out for series termination
TL5	VTT or Split Termination	Microstrip	0.25”	0.5”	-	5 mils	Single VTT termination in VTT island is preferred
TL6	Same as TL2	Stripline	1”	4”	Same as TL2	12 mils	Same as TL2

Notes:

1. Series termination is recommended in the center of the lead-in length
2. Parallel termination with single VTT Termination is preferred than split termination
3. For single VTT termination (preferred) the resistor value = 51 ohms +/- 5%
4. For split termination, the value of the resistors are 100 ohms +/- 5% to 2.5V and 100 ohms +/- 5% to Ground.

8.4.3.2 DDR 333 Embedded Clock Routing Recommendations

This section lists the recommendations for the DDR 333 clock signals. Refer to Figure 55 for buffered clock topology, Figure 56 for unbuffered clock topology. Refer to Table 55 for a summary of DDR 333 embedded clock routing guidelines. Refer to Table 56 for a description of the segment lengths and matching requirements for buffered clock topology. Refer to Table 57 for a description of unbuffered clock topology information.

Figure 55. Embedded DDR 333 Buffered Clock Topology

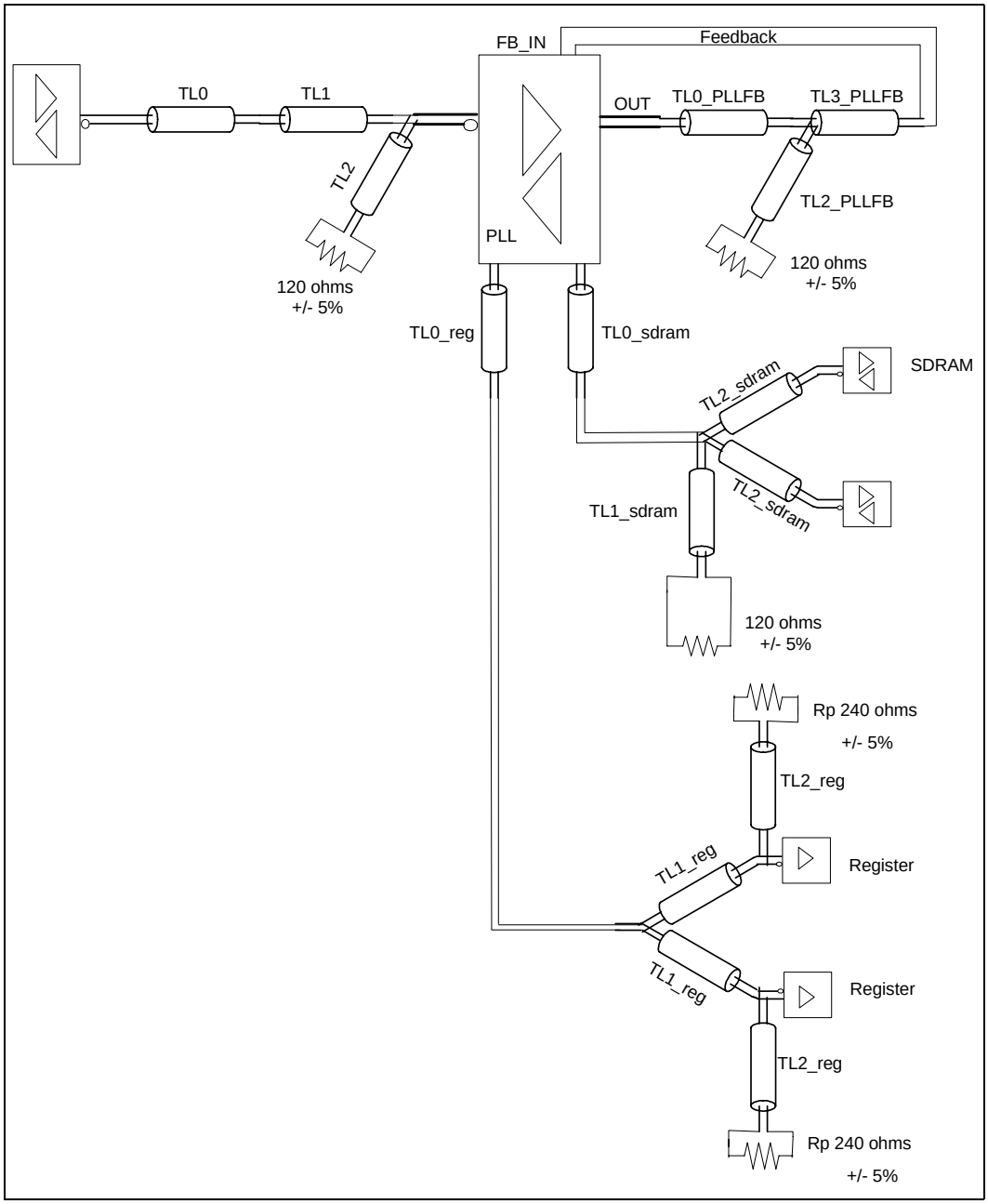


Table 55. DDR 333 Embedded Registered/Unbuffered Clock Routing Recommendations

Parameter	Routing Guideline
Reference Plane	• Route over unbroken ground plane
Preferred Topology	• Stripline routing is recommended for the clock signals. Micro-strip will work with strict adherence to all routing recommendations. Careful simulation and timing analysis of ADD/CMD signals is recommended.
Breakout Termination, Fan-in and Fanout width and spacing	5 mils x 5 mils. Microstrip is recommended for pin escapes and terminations.
Trace Impedance	Differential Target impedance of 100 Ohms +/-15% (Applies to both Buffered and Unbuffered Topologies)
Trace Spacing (trace edge to edge)	5 mils. for breakout region >20 mils. between any other signals or vias including other clock pairs.
Registered Termination	None required
Un-buffered Termination	• 22 ohms +/-5% series termination on each differential leg after breakout route • Post PLL and Unbuffered SDRAM Clock areas to be Routed as T Point differential as per JEDEC Unbuffered and Registered Post PLL Clock Topology
Length matching Requirements:	• The package lengths from Die to Ball provided in Table 44 must be accounted for when length matching. • See respective registered Table 56 and unbuffered Table 57 tables Topology/ Trace Length tables for additional information.
• Within Differential Clock pairs	• +/- 0.025” max. within Pairs [Intra-pair]
• Registered Clock from IOP Die to PLL Input with Respect to DQS	• With-in +/- 1.0” of all strobes (DQS0-8) (strobe length measured from IOP die to SDRAM)
• Registered Clock from IOP Die to PLL Input with Respect to Add/CMD/Control	• 1.0” to 2.0” longer than Add/CMD/Control (Add/CMD/Control length measured from IOP die to Register input)
• Un-buffered Clock from IOP Die to SDRAM input with respect to DQS	• With-in +/- 1.0” of associated strobe (DQS) (strobe length measured from IOP die to SDRAM)
• Un-buffered Clock from IOP Die to SDRAM input with respect to Add/CMD/Control	• 1.0” to 2.0” longer than Add/CMD/Control from (Add/CMD/Control length measured from IOP die to SDRAM input)
• Unbuffered Clock Pairs	• +/- 0.1” max. between the 3 pairs of Unbuffered Clocks (clock length measured from IOP die to SDRAM)
Number of vias	• For Registered: maximum of 3 pairs from IOP to PLL • For Unbuffered: maximum of 4 pairs.
Routing Guideline	All un-buffered clocks utilized in memory implementations must be load balanced. Use capacitors equal to the SDRAM’s clock input capacitance to balance loading across all the clocks used. Topology shown is based on a Raw B implementation. Refer to JEDEC Un-buffered DIMM specs. for Raw Card C implementation specifics.

Table 56. Embedded DDR 333 Buffered Clock Topology Lengths

Traces	Description	Layer	Min Length	Max Length	Trace Impedance	Spacing	Notes
TL0	Breakout	Microstrip/ Stripline		0.5”		5 mils	Differential Routing
TL1	Lead-in	Microstrip/ Stripline	2”	8”	Differential Impedance of 100 ohms +/- 15%	20 mils from others	
TL2	Termination			0.2”		5 mils	
TL0_PLLFB			2”	3”	Same as TL1	20 mils from others	Route per DDR1 JEDEC
TL2_PLLFB	Termination			0.3”			Route per DDR1 JEDEC
TL3_PLLFB			0.05”	0.09”	Same as TL1		Route per DDR1 JEDEC
TL0_sdram			2.5”		Same as TL1		Route per DDR1 JEDEC
TL1_sdram	Termination		0.5”	0.58”			Route per DDR1 JEDEC
TL2_sdram			0.29”	0.3”	Same as TL1		Route per DDR1 JEDEC
TL0_reg				0.05”			Route per DDR1 JEDEC
TL1_reg			2.71”	2.72”	Same as TL1		Route per DDR1 JEDEC
TL2_reg	Termination		0.20”	0.22”			Route per DDR1 JEDEC

NOTES:
1. For any additional loading configurations use same recommendations of TL1_SDRAM and TL2_SDRAM values.
2. JEDEC DDR1 (PC2700) registered DIMM recommendations are referenced for post PLL configurations.

Figure 56. Embedded DDR 333 Unbuffered Clock Topology

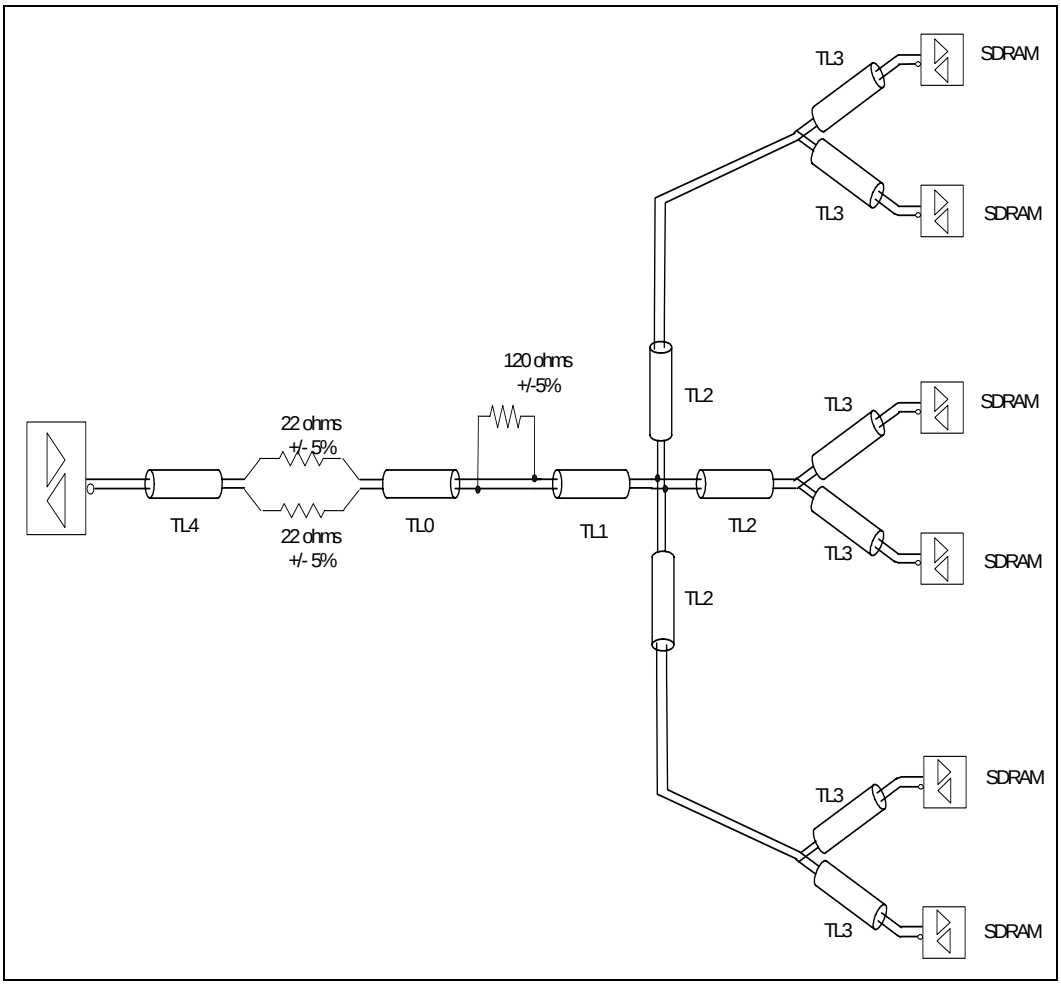


Table 57. Embedded DDR 333 Unbuffered Clock Topology Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL0	Lead-in	Microstrip/ Stripline	2”	10”	Differential 100 ohms +/- 15%	20 mils from any other signals	• Match within +/- 1” of strobes (DQS) from controller to SDRAM and within +/- 1” of Address/CMD control from controller to SDRAM input. • Route as T Differential pairs as per DDR1 DIMM JEDEC.
TL1			0.47”	0.49”	Same as TL0	20 mils	Route per DDR1 JEDEC
TL2			0.72 “	0.73”	Same as TL0	20 mils	Route per DDR1 JEDEC
TL3			0.36	0.37”	Same as TL0	20 mils	Route per DDR1 JEDEC
TL4	Breakout	Any		0.5”		5 mils	Route as differential

8.4.3.3 DDR 333 Embedded Address/Command/Control Routing Guidelines

This section lists the recommendations for the DDR 333 embedded address/command/control signal routing (**RAS#**, **CAS#**, **WE#**, **BA[1:0]**, **MA[12:0]**, **CS[1:0]#**, **and CKE[1:0]**). Refer to Table 58 and Figure 57 for a block diagram of the lengths and matching requirements. Table 59 provides the guidelines from the register to SDRAM.

Table 58. DDR 333 Embedded Address/Command Routing Recommendations (Sheet 1 of 2)

Parameter	Routing Guideline
Reference Plane	Route over unbroken ground plane
Preferred Topology	• Micro-strip only for Un-buffered memory configurations • Either Micro-strip or Stripline for Registered memory implementations and lightly loaded Un-buffered memory implementations (i.e. single bank w/ less than or equal to 36pF input capacitance).
Microstrip Trace Width and spacing	5 mils x 5 mils. Microstrip is recommended for pin escapes and terminations.
Trace Impedance	• 45 ohm +/- 15% or • 50 ohms +/- 15%
Trace Spacing (trace edge to edge)	• 5 mils is acceptable for pin escapes and terminations. • >12 mils within group • >20 mils must be maintained from any other groups (Clock/DQ/DQS)
Trace Length	Refer to following Embedded Addr/CMD Topology Table 59 for unbuffered and Table 60 for registered.
Series Resistor	22 +/- 5% ohms unbuffered configurations only
Parallel Resistor	51 +/- 5% ohms • Place the VTT terminations in VTT island after the DIMM (trace length of 0.15” to 0.5”0. • Split termination of 100 ohms +/- 5% to 2.5 V and 100 ohms +/- 5% to ground
Package Trace Length: Main Route Trace Lengths:	See Package Details for net length report Table 44. Refer to respective following Un-buffered or Registered Topology/ Trace Length tables for more details.

Table 58. DDR 333 Embedded Address/Command Routing Recommendations (Sheet 2 of 2)

Parameter	Routing Guideline
Length Matching	• The package lengths from Die to Ball provided in Table 44 must be accounted for when length matching • For total capacitive loads greater than 36pF, all ADD/CMD/CTRL trace lengths must be 2.0” to 3.0” shorter than M_CK’s trace length • For total capacitive loads less than or equal to 36pF, all ADD/CMD/CTRL trace lengths must be 1.0” to 2.0” shorter than M_CK’s trace length
Number of vias	• For Un-buffered memory implementations: Maximum of 5 • For Registered memory implementations: Maximum of 5 from IOP die to register. Maximum of 6 from Register to SDRAM.
Routing Guideline 1	Topology shown is based on a Raw B implementation. Refer to JEDEC Un-buffered DIMM specs. for Raw Card C implementation specifics.

Table 59. Embedded DDR 333 Unbuffered Address/CMD Topology Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL1		Microstrip/ Strip	1.5”	1.67”	45 ohms+/-15% or 50 ohms +/-15%	12 mils	TL1-TL6 as per JEDEC DDR1 Specifications (PC2700) to be routed as T points
TL2		Microstrip	1.2 “	1.35”	Same as TL1	12 mils	
TL3		Microstrip	0.5”	0.6”	Same as TL1	12 mils	Fan out for series termination (only for unbuffered)
TL4			0.3”	0.35”	Same as TL1	12 mils	
TL5			0.14”	0.18”	Same as TL1	12 mils	
TL6			0.32”	0.35”	Same as TL1	12 mils	
TL7			0.25”	0.5”	Same as TL1	12 mils	
TL8	Breakout	Any	0”	0.5”		5 mils	
TL9	Lead-in	Microstrip/ Stripline	1”	8”	45 ohms+/-15% or 50 ohms +/-15%	12 mils	Spacing: within the same group 12 mils With other groups 20 mils
TL10	VTT	Microstrip	0.25”	0.5”		5 mils	Place in VTT Island

NOTE: All traces except breakout TL8 traces are of the same impedance and spacing requirements.

Figure 57. Embedded DDR 333 Unbuffered ADDR/CMD Topology

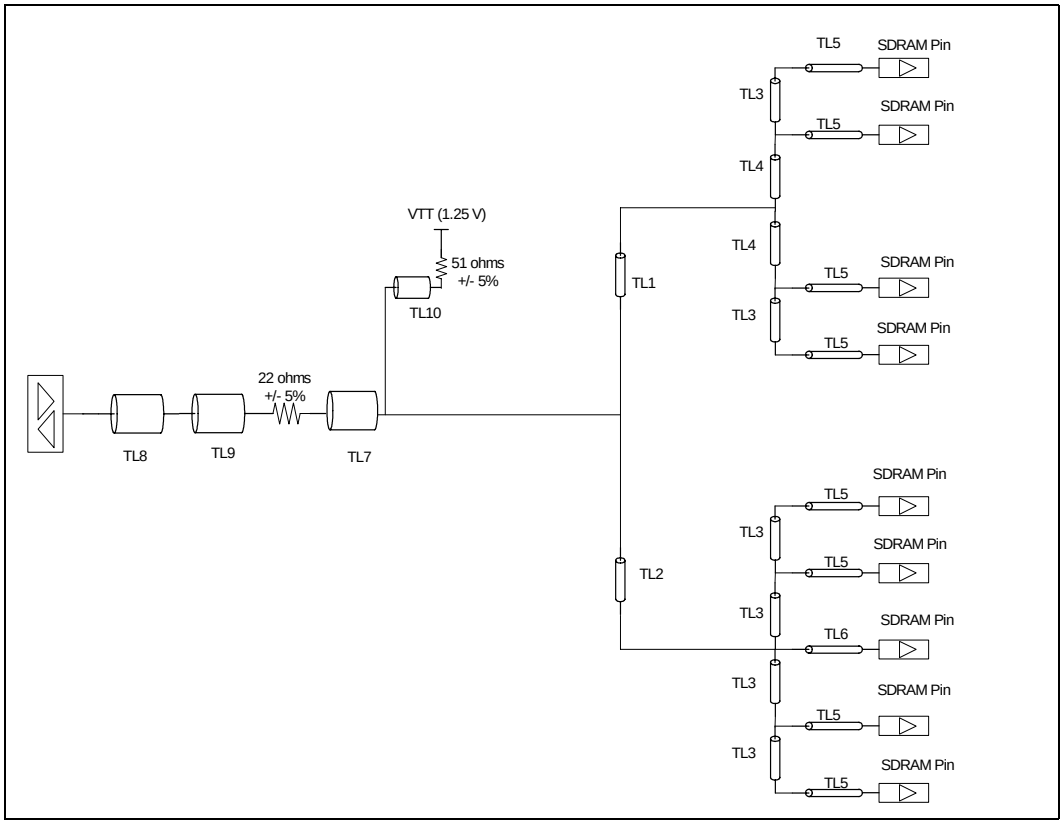
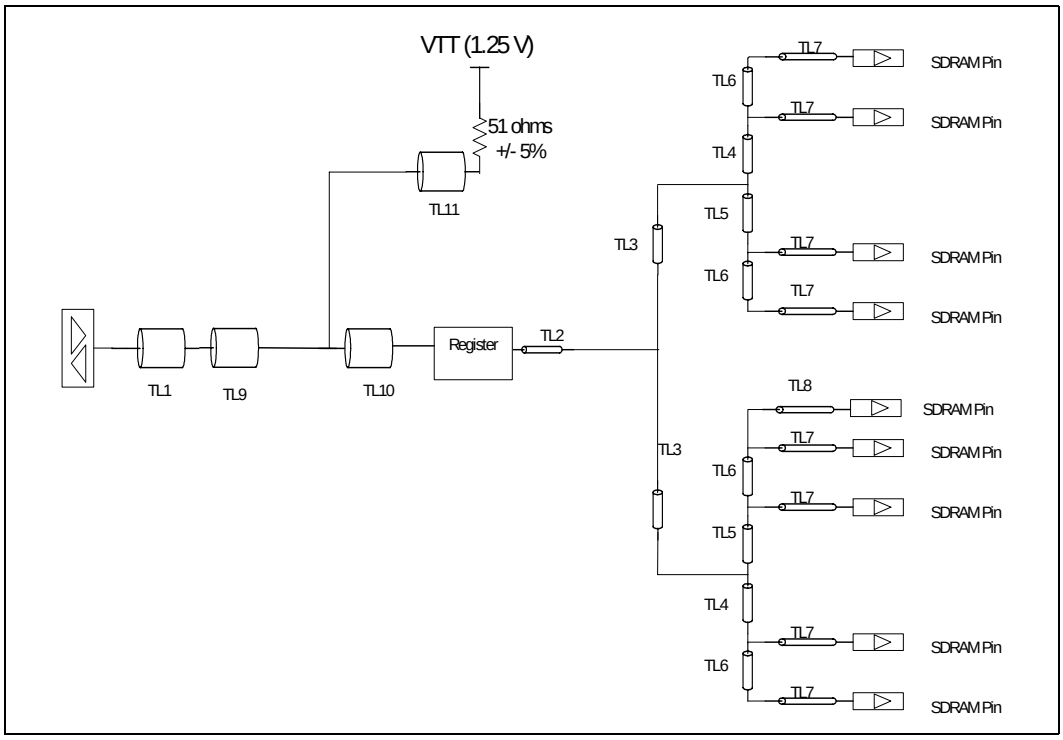


Table 60. Embedded DDR 333 Registered Address/CMD Topology Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL1	Breakout	Microstrip/ Strip	0”	0.5”		5 mils	5 mils trace width for breakout
TL2		Microstrip	0.6 “	1.37”	45 ohms+/-15% or 50 ohms +/-15%	12 mils	Spacing: within the same group 12 mils Other groups 20 mils
TL3			1.39”	2.57”	Same as TL2	12 mils	
TL4			0.4”	0.56”	Same as TL2	12 mils	
TL5			0.14”	0.15”	Same as TL2	12 mils	
TL6			0.48”	0.63”	Same as TL2	12 mils	
TL7			0.20”	0.32”	Same as TL2	12 mils	
TL8			0.49	0.72”	Same as TL2	12 mils	
TL9	Lead-in	Microstrip	1”	9”	45 ohms+/-15% or 50 ohms +/-15%	12 mils	Spacing: within the same group 12 mils With other groups 20 mils
TL10		Microstrip	-	0.2”	Same as TL2	12 mils	
TL11	Vtt	Microstrip	0.25’	0.5”		5 mils	5 mils trace width OK for breakout

NOTES:
1. Post Register recommendations are referenced from JEDEC DDR1 Registered DIMM.
2. TL2 to TL8 are numbered JEDEC references.

Figure 58. Embedded DDR 333 Registered ADDR/CMD Topology



8.5 DDR II 400 Layout Guidelines

This section lists the DDRII layout guidelines for both DIMM and embedded designs. The topologies that were analyzed include registered DIMM (RawA and RawB configurations) and embedded single bank configurations (both ECC and Non-ECC type).

The On Die Termination or ODT for DDR II eliminates some of the termination resistors needed for the source synchronous signals. The value used for simulations was 75Ω. Note that this value must be programmed for both the IOP and the SDRAM locations.

The Table 61 and Table 62 list the DDR II differential strobe alignment with each of the DQ groups.

Table 61. x64 DDR Memory Configuration

Data Group	Positive Strobe	Negative Strobe
DQ[7:0], DM[0]	**DQS0**	**DQS0**#
DQ[15:8], DM[1]	**DQS1**	**DQS1**#
DQ[23:16], DM[2]	**DQS2**	**DQS2**#
DQ[31:24], DM[3]	**DQS3**	**DQS3**#
DQ[39:32], DM[4]	**DQS4**	**DQS4**#
DQ[47:40], DM[5]	**DQS5**	**DQS5**#
DQ[55:48], DM[6]	**DQS6**	**DQS6**#
DQ[63:56], DM[7]	**DQS7**	**DQS7**#

Table 62. x72 DDR Memory Configuration

Data Group	Positive Strobe	Negative Strobe
DQ[7:0], DM[0]	**DQS0**	**DQS0**#
DQ[15:8], DM[1]	**DQS1**	**DQS1**#
DQ[23:16], DM[2]	**DQS2**	**DQS2**#
DQ[31:24], DM[3]	**DQS3**	**DQS3**#
DQ[39:32], DM[4]	**DQS4**	**DQS4**#
DQ[47:40], DM[5]	**DQS5**	**DQS5**#
DQ[55:48], DM[6]	**DQS6**	**DQS6**#
DQ[63:56], DM[7]	**DQS7**	**DQS7**#
CB[7:0], DM[8]	**DQS8**	**DQS8**#

8.5.1 Simulation Conditions

- Motherboard 50 ohm single ended impedance stackup +/- 15% tolerance
- Add-in Card 60 ohm single ended impedance stackup +/- 15% tolerance
- Clock Target Differential Impedance 100 ohms and 50 ohms single-ended impedance
- One Die Termination - ODT value of 75Ω was assumed for all DDR II simulations.
- Memory Model Micron U26 and Intel generic models
- PLL Clock - ICS ICSU877
- Register - IDT IDT74SSTU32864
- DIMM models and topologies used the JEDEC model as a reference.
- For unbuffered embedded and post PLL/register the JEDEC standard recommendations were used as a reference.
- Vias are modeled for all topologies with equal number of vias for differential pair
- Package - actual extracted package model.
- Spacing recommendations are for trace edge to edge except for differential pairs in which center to center was specified.
- Timing analysis was conducted.
- ISI Pattern was simulated for all the major topologies.
- Signal Quality analysis covered for Rising flight time, Falling flight time, Low to high ring-back (noise margin high), High to Low ring-back (noise margin Low), and Low and High Overshoot.
- Crosstalk Analysis was performed for all the major interfaces with actual package models.
- Frequency: 200MHz (DDR 400 MT/s)

The topologies simulated are listed in Table 63.

Table 63. DDR II Topologies Simulated

DIMM (Registered)	Embedded
1. DQ/DQS • Read- RAW A, RAWB • Write -RAW A, RAW B	1. DQ/DQS • Read- Single Bank • Write - Single Bank
2. Clock • Buffered - controller to PLL • Unbuffered	2. Clock • Controller to PLL • Post-PLL • PLL to SDRAM • PLL to Register • PLL to Feedback
3. Address/CMD • Registered - RAWA, RAWB configurations	3. Address/CMD • write single bank non ECC and ECC • Post Register - single bank ECC and non ECC

8.5.2 DDRII-400 Trace Width/Impedance Requirements

The Table 64 below provides an example of a table of recommended topologies for motherboard and add-in card eight layer PCB designs. Throughout this section the important recommendation to meet is the trace impedance. The example in Table 64 is provided as a reference.

Table 64. Example Topology for DDRII Trace Width/Impedance Requirements

Topology	Trace Width (mils)	Min Trace Spacing (mils)	Trace Impedance (ohms)	Preferred signals	Board Type
Microstrip (layers 1 or 8)	5	5		Breakout	Motherboard/Add-in
	7	12	45	Address/ CMD/Control	Motherboard/Add-in
	6	12	50		Motherboard/Add-in
	4	12	60		Motherboard/Add-in
	5 (note 1)	20	100 differential	Differential Clock/DQS	Motherboard/Add-in
Stripline (layers 3 or 6)	5	5		Break out	Motherboard/Add-in
	6	12	45	DQ/CB	Motherboard
	5	12	50		Add-in card
	7	12	45	DQ/CB	Add-in card
	6	12	50		Add-in card
	4	12	60		Add-in card
	4 (note 2)	20	100 Ohm	Differential Clock/DQs	Motherboard*
	5 (note 3)	20	100 Ohm	Differential Clock/DQs	Add-in card*

NOTES:
1. Microstrip Differential Lines: Motherboard/Add-in 100 ohm: Constructed by two microstrips of 5 mils traces separated by center to center distance of 13 mils refer to Figure 45.
2. Strip Differential Lines: Motherboard Stripline 100 ohms: Constructed by two striplines of 4 mils traces separated by center to center distance of 12 mils refer to Figure 45.
3. Strip Differential Lines: Add-in stripline 100 ohms: Constructed by two striplines of 4 mils traces separated by center to center distance of 13 mils refer to Figure 45.

8.5.3 DIMM Layout Design

The following tables provide the source synchronous, clock and control layout guidelines when laying out the board for DDRII 400 registered DIMMs. The guidelines were based on simulating RawA and RawB DIMM topologies.

8.5.3.1 DDR II 400 DIMM Source Synchronous Routing

This section lists the recommendations for the DDR II 400 Source Synchronous Routing. These signals include all the DQ/DQS/DM signals. Refer to Figure 59 and Table 65 for a block diagram of the lengths and matching requirements.

Figure 59. Intel® 80333 I/O Processor DDRII 400 DIMM Source Synchronous Routing

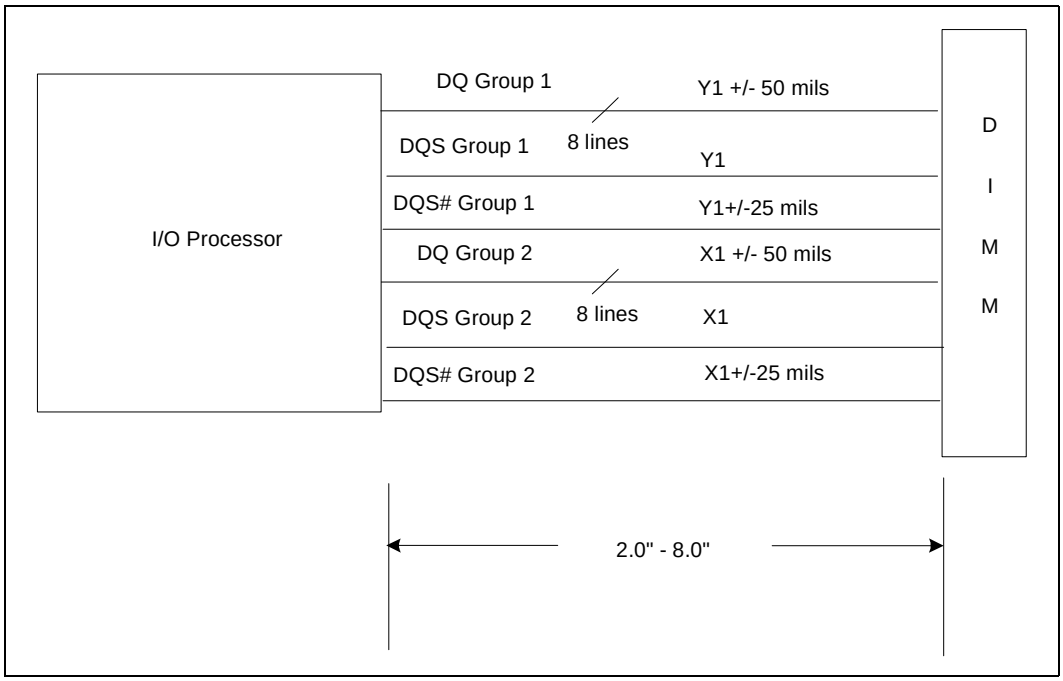


Table 65. DDRII 400 DIMM Source Synchronous Routing Recommendations

Parameter	Routing Guideline
Reference Plane Layer	Route over unbroken ground plane Strip line (layer 3 or layer 6)
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region can be up to 500 mils either microstrip or strip line
Stripline Trace Impedance Motherboard/Add-in Card Differential DQ	• DQ signals: Single ended strip lines at 45 ohm +/15% or 50 ohms +/- 15% impedance. Refer Table 64 and DIMM DQ topologies.
Stripline Trace Impedance Motherboard/Add-in Card Differential DQS	• DQS Signals: Differential ended strip lines at 100ohm impedance. Refer to Table 64 and DIMM DQS Topologies.
DQ Group Spacing (edge to edge)	• Spacing same group: 12 mils minimum • Spacing from other DQ groups 20 mils minimum • For DQS from any other signals: 20 mils minimum
Overall Trace Length: 80333 signal Ball to DIMM connector (no series connector)	2” minimum to 8” maximum (correlated with the clock length from ball to DIMM).
DQS Length Matching: • Trace Length Matching within DQS group • Within one DQS pair plus and minus • All DQ/DQS lines with respect to the clock signal	 +/-0.05” within DQS group +/- 0.0250” +/- 1” (target motherboard clock = +/- 1” of any DQ/DQS pair)
Number of Vias	Two (for differential signals the number of vias on + and - signals must be the same)
Routing Guideline	Route all data signals and their associated strobes on the same layer.

Table 66. DDR II 400 DIMM DQ Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing (edge to edge)	Notes
TL0	Breakout	Microstrip	0”	0.5”		5 mils	5 mils trace width OK for breakout.
TL1	Lead-in	Microstrip	2 “	8”	45 ohms or 50 ohms	Same group 12 mils Other groups 20 mils	

Figure 60. DDR II 400 DIMM DQ Topology

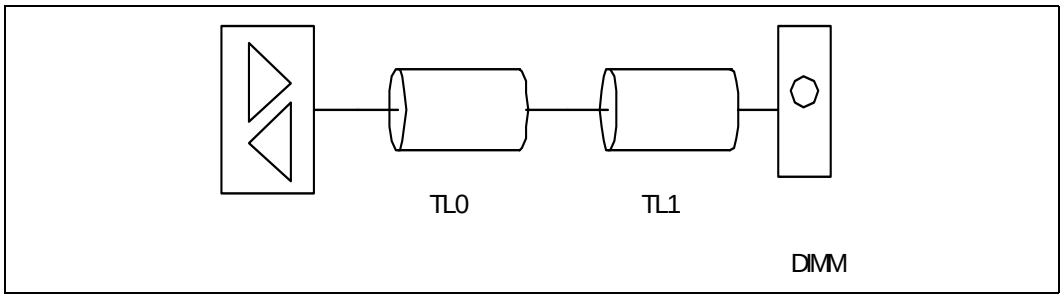
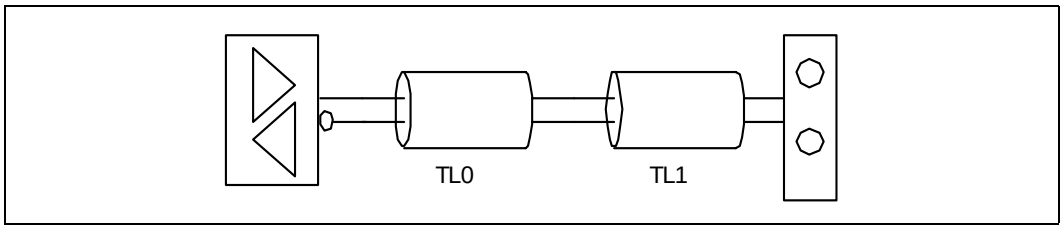


Table 67. DDR II 400 DIMM DQS Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing (edge to edge)	Notes
TL0	Breakout	Microstrip	0”	0.5”		5 mils	5 mils trace width OK for breakout.
TL1	Lead-in	Microstrip	2 “	8”	Differential 100 ohm impedance	20 mils from other signals	Route as differential pair. • Motherboard 100 ohm differential constructed by stripline of two 4 mil traces separated by center to center distance of 12 mils. • Add-in card 100 ohm differential constructed by stripline of two 5 mil traces separated by center to center distance of 12 mils.

Figure 61. DDR II 400 DIMM DQS Topology



8.5.3.2 DDRII 400 Clock Routing Guidelines

This section lists the recommendations for the DDR II 400 Clock signals. Refer to Figure 62 and Table 68 for a description of the segment lengths and matching requirements.

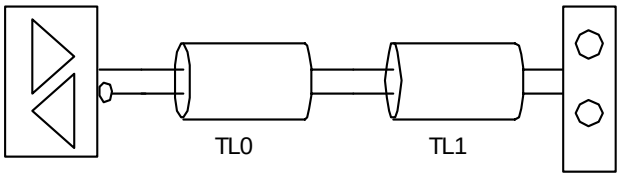
Table 68. DDRII 400 DIMM Clock Routing Recommendations

Parameter	Routing Guideline
Reference Plane	Unbroken Ground plane
Preferred Topology	Microstrip differential lines (preferred) Stripline differential lines
Microstrip Trace Width and spacing	5 mils by 5 mils.
Trace Impedance	Differential impedance of 100 ohms +/- 15% Refer to DIMM Clock Topology
Trace Spacing	> 20 mils between other signals.
Trace Length 1: IOP signal Ball to DIMM connector	2.0”min to 10.0” max correlated within the +/- 1.0” of the DQ/DQS and command signal length (from 80333 to DIMM connector).
Length Matching: • Within differential clock signals • With respect to DQ/DQS group (from controller to DIMM connector) • With respect to address/command group (from controller to DIMM connector)	 +/- 0.0250” within pairs (intra-pair) +/- 1.0” maximum +/- 1.0” maximum
Routing Guideline 1	Maximum of 1 via/layer change for differential clocks. (use the same number of vias between + and - signals of differential clock)
Routing Guideline 2	Route clock signal as differential pair with target differential impedance of 100 ohms.

Table 69. DDR II 400 DIMM Clock Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing (edge to edge)	Notes
TL0	Breakout	Microstrip or stripline	0”	0.5”		5 mils	5 mils trace width OK for breakout.
TL1	Lead-in	Microstrip or stripline	2 “	10”	Differential Impedance of 100 ohms	Other groups 20 mils	Route as differential pair with target impedance of 100 ohms correlated within the +/- 1.0” of the DQ/DQS and command signal length (from 80333 to DIMM connector).

Figure 62. DDR II 400 DIMM Clock Topology



8.5.3.3 DDRII 400 Address/Command/Control Routing Guidelines

This section lists the recommendations for the DDR II 400 Address/Command and Control signals (**RAS#**, **CAS#**, **WE#**, **BA[1:0]**, **MA[12:0]**, **CS[1:0]#, and CKE[1:0]**). Refer to Figure 63 and Table 70 for a description of the segment lengths and matching requirements.

Table 70. DDRII 400 DIMM Address/Command/Control Routing Recommendation

Parameter	Routing Guideline
Reference Plane	Route over unbroken power plane
Preferred Topology	Microstrip lines
Breakout Trace Width and spacing	5 mils x 5mils.
Trace Spacing	• 5 mils acceptable between the pins and the breakout regions. • >12 mils within group • >20 mils from any other clock/DQ/DQS groups.
Trace Impedance	45 ohms +/- 15% or 50 ohms +/- 15%
Trace Length: Overall length from 80333 signal Ball to DIMM Connector	2.0”min to 10” max (Correlated with in +/- 1” of DQ/DQS and command lead-in MB length) Refer to following table for segment lengths.
Length Matching Requirements:	2”-10” matched within +/- 1” of target motherboard M_CK
Single Parallel Termination Split Termination	51 ohms +/- 5% to VTT 100 ohms +/- 5% to ground and 100 ohms to 1.8V
Routing Guideline 1	Route clock signal as differential pair with target differential impedance of 100 ohms
Routing Guideline 2	Place the VTT terminations in the VTT island after the DIMM with a trace length of 0.15” to 0.5”
Routing Guideline 3	For split terminations place the VTT termination in their respective power islands
Number of vias	2 Vias or less

Table 71. DDR II 400 DIMM Address/CMD Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL0	Breakout	Microstrip	0”	0.5”		5 mils	5 mils trace width OK for breakout.
TL1	Lead-in	Microstrip	2 “	10”	45 ohms or 50 ohms	12 mils	• 45 ohm +/- 15% or • 50 ohm +/- 15% • 2”-10” matched within +/- 1” of target motherboard M_CK
TL2	Vtt	Microstrip	0.15 “	0.5”		5 mils	Place terminations in Vtt island

Figure 63. DDR II 400 DIMM Address/CMD Topology

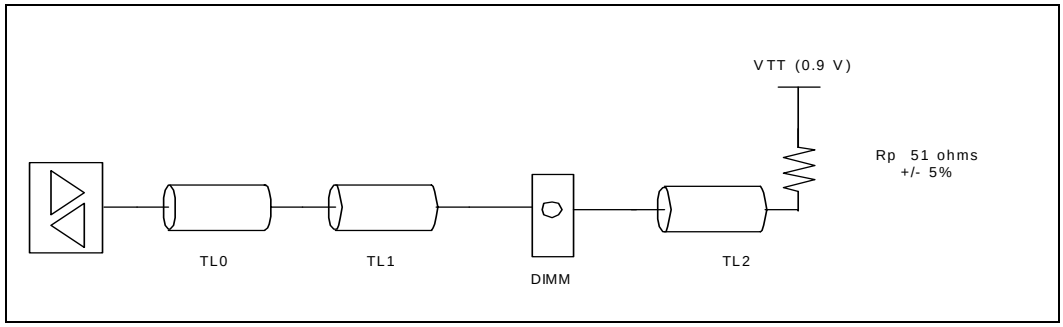
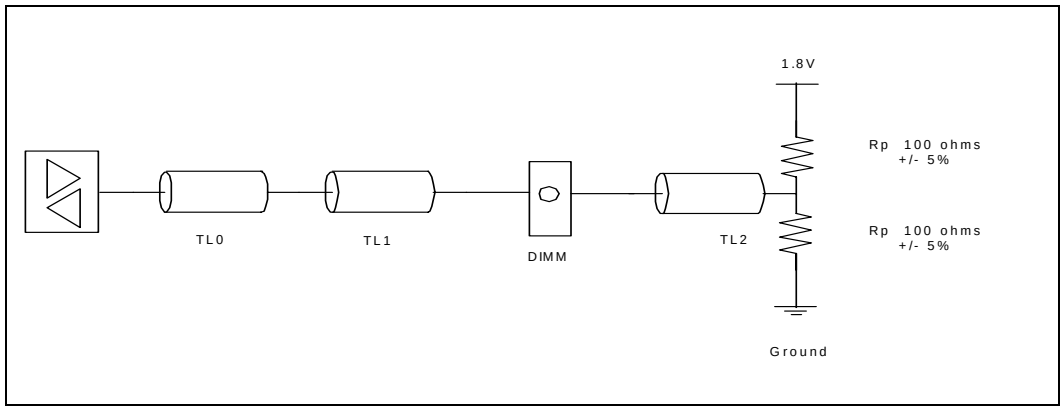


Figure 64. DDR II 400 DIMM Address/CMD Split Termination Topology



8.5.4 Embedded Configuration

The following tables provide layout guidelines for applications in which the DDRII 400 memory SDRAM, registers and PLL components are placed directly on the board without a DIMM.

8.5.4.1 DDRII 400 Embedded Source Synchronous Routine Guidelines

This section lists the recommendations for the DDR II 400 embedded source synchronous routing. These signals include all the DQ/DQS signals. Refer to Table 72 and Figure 65 for a block diagram of the lengths and matching requirements.

Table 72. DDRII 400 Embedded Source Synchronous Routing Recommendations

Parameter	Routing Guideline
Reference Plane	Route over unbroken power plane
Preferred Topology	Stripline
Breakout	5 mils x 5 mils spacing.
Group Trace Spacing (edge to edge)	• 5 mils is acceptable for pin escapes and terminations. • 5 mils for DQS differential pairs (intra-pair) • >12 mils between any DQ/DQS signals • >20 mils bust be maintained from any other groups
Trace Impedance	• 45 ohms +/- 15% • 50 ohms +/- 15% • Differential impedance of 100 ohms +/- 15%
Trace Details	• TL1 and TL4 are approximately same length and the series Termination to be placed in the middle of lead-in trace for Lead-in lengths >6 Inches • When Controller to SDRAM lead-in trace length is less than 6 Inches, Series Termination may be placed anywhere between middle of the lead-in trace to SDRAM • For DQS use differential routing • Route all data signals and associated strobes on same layer as strip lines. • No parallel DQS termination is required with ODT of SDRAMs used. • Refer to Figure 65
DQ Group Spacing	Spacing from other DQ groups 20 mils minimum
Trace Lengths	Refer to Figure 65 for details.
DQS Length Matching: • Trace Length Matching within DQS group • Within one DQS pair plus and minus • Between other DQS groups • With respect to the clock signal	 +/- 0.05” within DQS group +/- 0.0250” +/- 0.250” between each of the DQS groups. +/- 1” (target motherboard clock to PLL input = +/- 1” of any DQS/DQ pair)
Series Termination	22.1 ohms +/- 5%
Parallel Termination	No parallel DQS termination is required with ODT of SDRAMs used.
Routing Guideline 1	Route all data signals and associated strobes on same layer.
Routing Guideline 2	Minimize layer changes especially on clock and DQS signals. (two vias or less)

Table 73. DDR II 400 Embedded DQ Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL0	Breakout	Microstrip	0”	0.5”		5 mils	5 mils trace width OK for breakout.
TL1	Lead-in*	Stripline	1 “	4”	45 ohms or 50 ohms	12 mils	45 ohms +/- 15% 50 ohms +/- 15%
TL2		Microstrip	0”	0.1”		5 mils	5 mils trace width OK for termination fan out
TL3		Microstrip	0”	0.1”		5 mils	5 mils trace width OK for termination fan out
TL4	Same as TL1	Stripline	1”	4”	45 ohms or 50 ohms	12 mils	45 ohms +/- 15% 50 ohms +/- 15%

NOTES:
1. TL1 and TL4 are approximately the same length allowing Rs in the middle of the lead-in trace between the controller and SDRAM.
2. Then controller to SDRAM lead-in traces are less than 6” the series resistor may be places anywhere in between the center of the lead-in trace to SDRAM

Figure 65. DDR II 400 Embedded DQ Topology

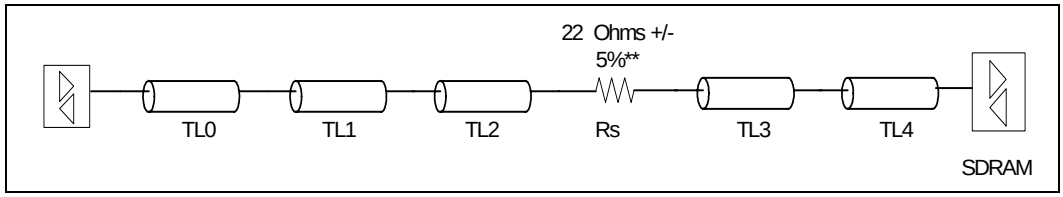
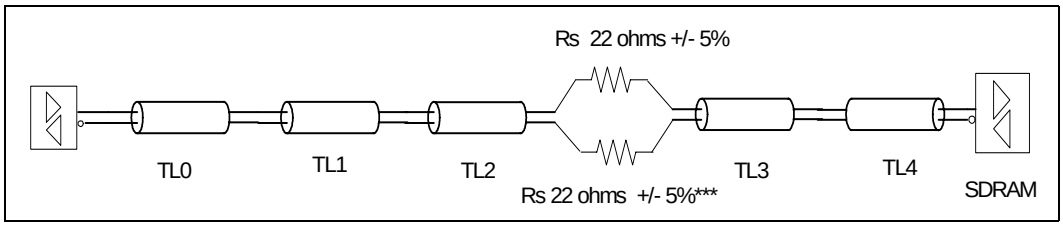


Table 74. DDR II 400 Embedded DQS Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL0	Breakout	Microstrip	0”	0.5”		5 mils	5 mils trace width OK for breakout.
TL1	Lead-in	Stripline	1 “	4”	Differential impedance of 100 ohms +/-15%	20 mils from others	
TL2		Microstrip	0”	0.1”			5 mils trace width OK for termination fan out
TL3		Microstrip	0”	0.1”			Same as TL2
TL4	Same as TL1	Stripline	1 in	4”	Differential impedance of 100 ohms +/-15%	20 mils from others	Same as TL1

NOTES:
1. TL1 and TL4 are approximately the same length allowing Rs in the middle of the lead-in trace between the controller and SDRAM.
2. When controller to SDRAM lead-in traces are less than 6” the series resistor may be places anywhere in between the center of the lead-in trace to SDRAM.

Figure 66. DDR II 400 Embedded DQS Topology



8.5.4.2 DDRII 400 Embedded Clock Routing Recommendations

This section lists the recommendations for the DDR II 400 clock signals. Refer to Figure 67 and Table 75 for a description of the segment lengths and matching requirements Table 76 provides the guidelines from PLL to SDRAM.

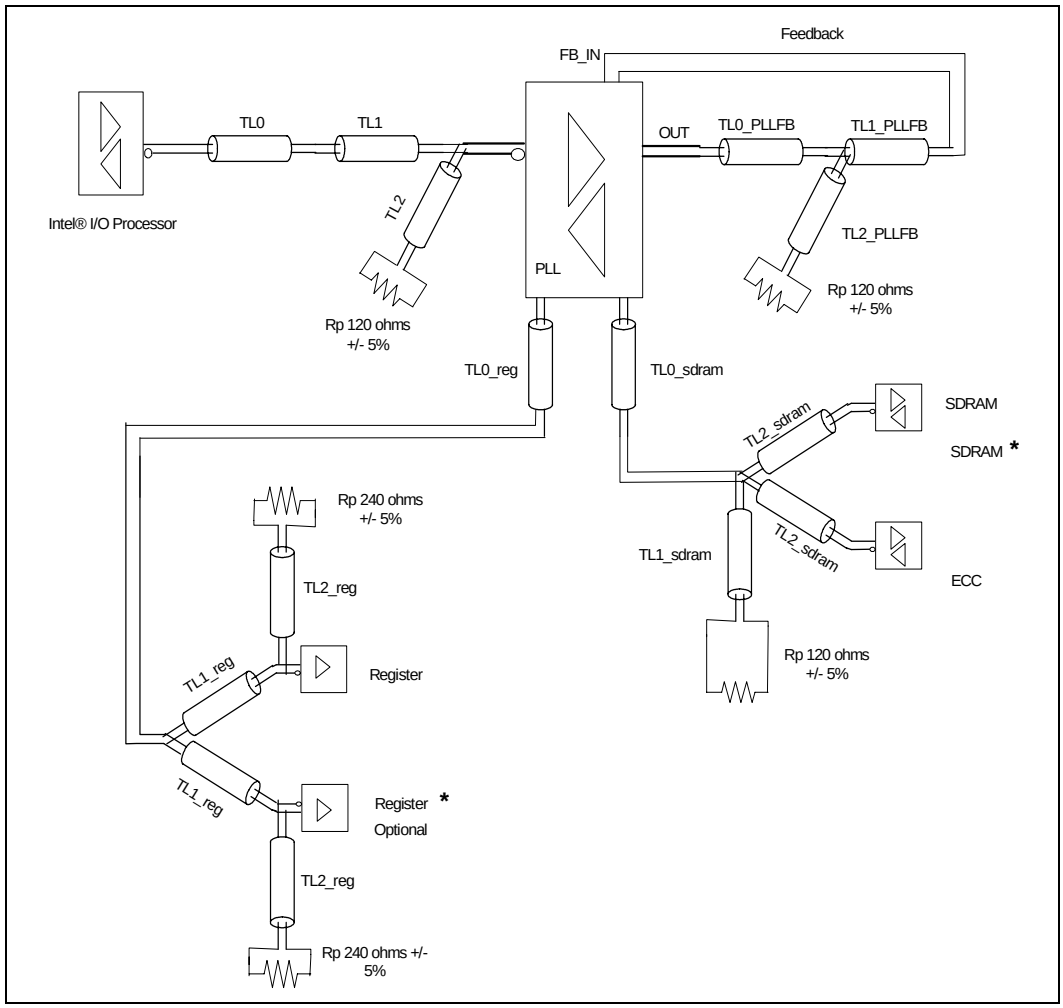
Table 75. DDRII 400 Embedded Clock Routing Recommendations

Parameter	Routing Guideline
Reference Plane	Route over unbroken ground plane
Preferred Topology	Microstrip or Stripline routed differentially
Breakout Trace Width and Spacing	5 mils x 5 mils.
Trace Spacing	• 5 mil spacing acceptable between pin escapes and breakout regions. • 5 mils for clock differential pairs (intra-pair), • >20 mils between other signals.
Trace Impedance	Differential impedance of 100 ohms +/- 15% Refer to Figure 67
Trace Details	Route as differential pair with differential impedance of 100 ohms. Figure 67
Overall Trace Length	2.0”min to 10.0” max; refer to figures and tables that follow for line segment lengths and topology.
DQS Length Matching: • Within differential clock signals	 +/- 0.0250” within pairs (intra-pair)
Overall clock correlation with other signals	• All DQ/DQS groups matching needs to be matched within +/- 1” of the clock signals. • Address/Command/Control lengths from 80333 ball to the register needs to be matched within +/- 1” of the clock signals
Series Termination	No series termination for buffered memory
Parallel Termination	100 ohms
Routing Guideline 1	Maximum of 2 via/layer change for differential clocks.
Routing Guideline 2	Route clock signal as differential pair with target differential impedance of 100 ohms and single ended impedance of 50 ohms with ground referenced strip line only.

Table 76. DDR II 400 Embedded Clock (PLL) Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL0	Breakout	Any	0”	0.5”		5 mils	5 mils trace width OK for breakout.
TL1	Lead-in	Microstrip/Stripline	2 “	10”	Differential impedance of 100 ohms +/- 15%	20 mils from others	• Route as differential pair. Refer to table __ for details
TL2	For Termination	Microstrip	0”	.1”		5 mils	
TL0_PLLFB	PLL Feedback	Microstrip or stripline	2.2 “	2.3”	Same as TL1	20 mils	Route as per DDRII JEDEC
TL1_PLLFB		Microstrip or stripline	20 mils	50 mils		20 mils	Route as per DDRII JEDEC
TL2_PLLFB	For Termination	Microstrip or stripline	0”	100 mils		5 mils	Route as per DDRII JEDEC
TL0_sdram		Microstrip/Stripline	2.7”	2.75”	Same as TL1	20 mils from others	Route as per DDRII JEDEC
TL1_sdram		Microstrip/Stripline	0.5”	0.75”		20 mils from others	Route as per DDRII JEDEC
TL2_sdram	For Termination	Microstrip/Stripline	0”	150mils		5 mils	
TL0_reg		Microstrip/Stripline	2”	2.25”	Same as TL1	20 mils	Route as per DDRII JEDEC
TL1_reg		Microstrip/Stripline	25 mils	50mils		20 mils	Route as per DDRII JEDEC
TL2_reg	For Termination	Microstrip/Stripline	100 mils	125 mils		5 mils	

Figure 67. DDR II 400 Embedded Clock Topology



8.5.4.3 DDRII 400 Embedded Address/Command/Control Routing Guidelines

This section lists the recommendations for the DDR II 400 embedded address/command/control signal routing. Refer to Table 77, Table 78, Figure 68 and Figure 69 for a block diagram of the lengths and matching requirements.

Table 77. DDRII 400 Embedded Address/Command/Control Routing Recommendations

Parameter	Routing Guideline
Reference Plane	Route over unbroken ground plane
Preferred Topology	Microstrip (outer layers) preferred or Stripline (inner layers)
Microstrip Trace Width and Spacing	5 mils x 5 mils. Microstrip is recommended only for pin escapes and terminations.
Trace Impedance	45 ohms +/- 15% or 50 ohms +/- 15% Refer to Embedded Address/CMD topology
Microstrip Trace Spacing (edge to edge)	• 5 mils acceptable through pin field, break out regions and terminations • >12 mils within group • >20 mils from any other clock/DQ/DQS groups.
Overall length 80333 signal Ball to register input	2” minimum - 10” maximum length matched within +/- 1.0” of target motherboard clock M_CK to PLL.
Series Termination	none
Parallel Termination	• 51 ohms, place the VTT terminations in the VTT island after TL1 by trace length of TL10 • or Split Termination of 100Ohms to 1.8V and 100 Ohms to Ground can be used • Place the VTT Terminations in VTT Island after TL1 by Trace Length of TL10 (Single VTT Termination) • Place Split terminations in respective Voltage rails island. • Refer to Embedded Address/CMD Topology and Table for Single VTT Termination or Split Termination
Routing Guideline 1	Post register TL2-TL8 route as per JEDEC DDRII Registered DIMM T routing.
Routing Guideline 2	3 Vias or less for preregister, route as per T routing requirement for post register.

Table 78. DDR II 400 Embedded Address/CMD Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing	Notes
TL0	Breakout	Any	0”	0.5”		5 mils	5 mils trace width OK for breakout.
TL1	Lead-in	Microstrip	2 “	10”	45 ohms or 50 ohms	12 mils	• 45 ohms +/- 15% or • 50 ohms +/- 15%
TL2		Microstrip (MS)	20 mils	25 mils	Same as TL1	12 mils	TL2 to TL8 as per JEDEC DDRII Registered specification routed as T points
TL3		MS	1500 mils	1550 mils	Same as TL1	12 mils	
TL4		MS	1850	1900	Same as TL1	12 mils	
TL5		MS	500	560	Same as TL1	12 mils	
TL6		MS	275	325	Same as TL1	12 mils	
TL7		MS	550	600	Same as TL1	12 mils	
TL8		MS	50	270	Same as TL1	12 mils	
TL9	Fan out	MS	0”	100		5 mils	
TL10	VTT Termination or split termination	MS	150	500		5 mils	To be placed in respective VTT power island.

Figure 68. DDR II 400 Embedded Address/Control Topology

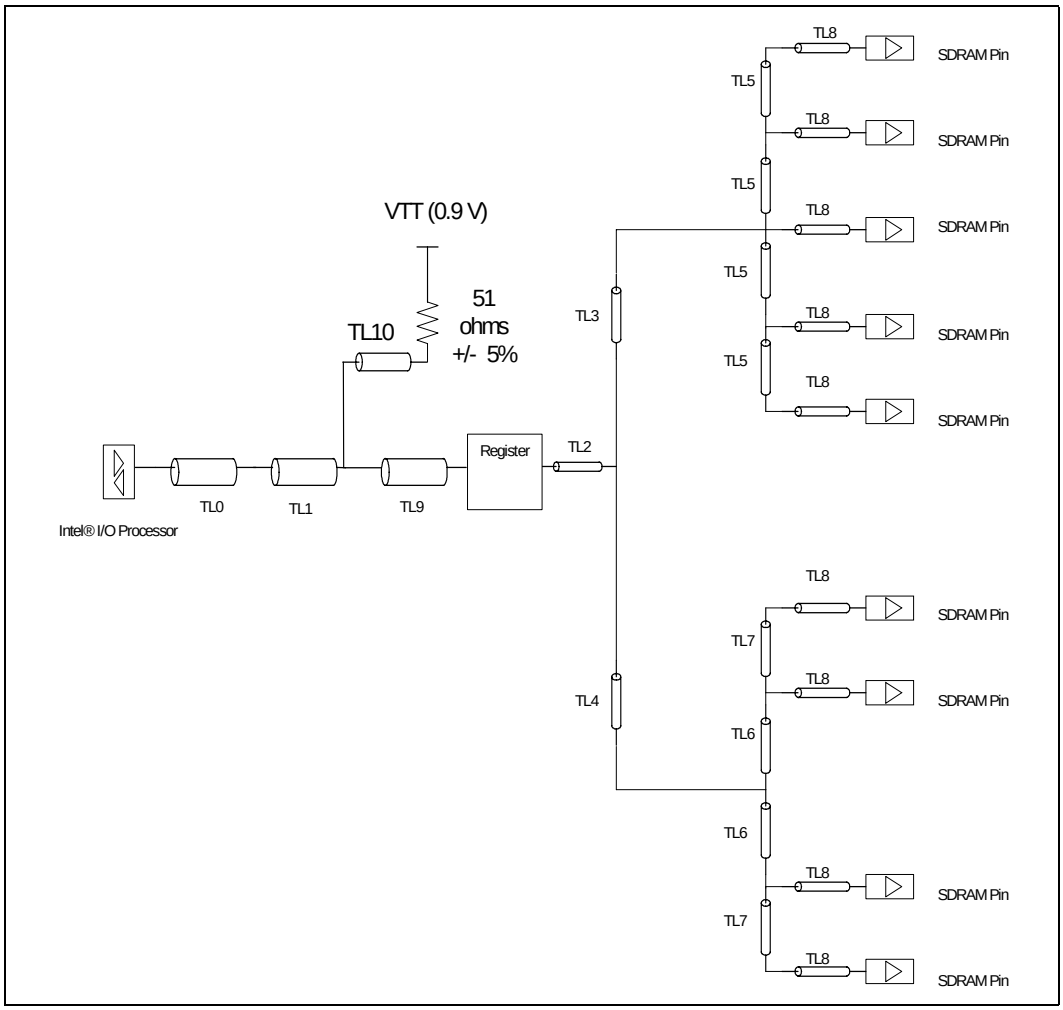
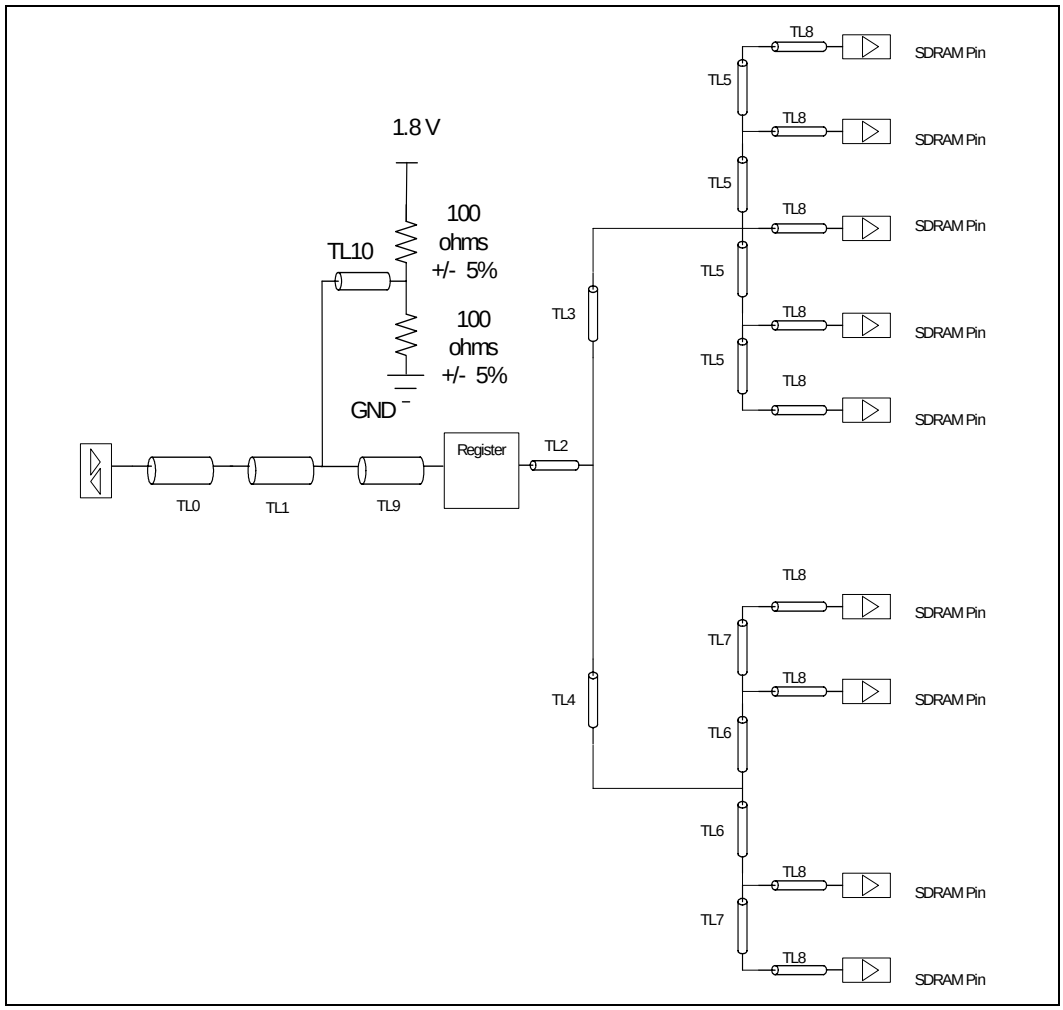


Figure 69. DDR II 400 Embedded Address/Control Topology With Split Termination

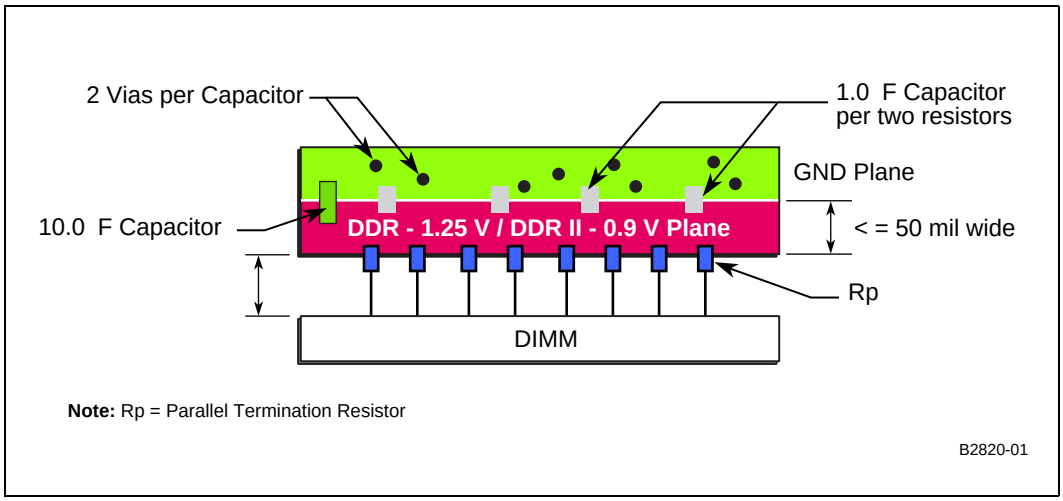


8.6 DDR Signal Termination

This section provides suggested guidelines for layout of the DDR termination resistors:

- Place a 1.25 V termination plane for DDR or a 0.9V termination plane for DDR II 400 on the top layer or one of the inner layers, just beyond the DIMM connector for DDR.
- The $\mathbf{V_{TT}}$ island must be at least 50 mils wide.
- Use this termination plane to terminate all DIMM signals, using the one termination resistor per signal.
- Decouple the $\mathbf{V_{TT}}$ plane using one 0.1 µF decoupling capacitor per two termination resistors.
- Each decoupling capacitor must have at least two vias between the top layer ground fill and the internal ground plane.
- In addition, place one 10 µF or larger (100 µF suggested) Tantalum capacitor on each end of the termination island for bulk decoupling.
- Figure 70 provides an example of how to route the termination resistors.

Figure 70. Routing Termination Resistors (top view)



8.7 DDR Termination Voltage

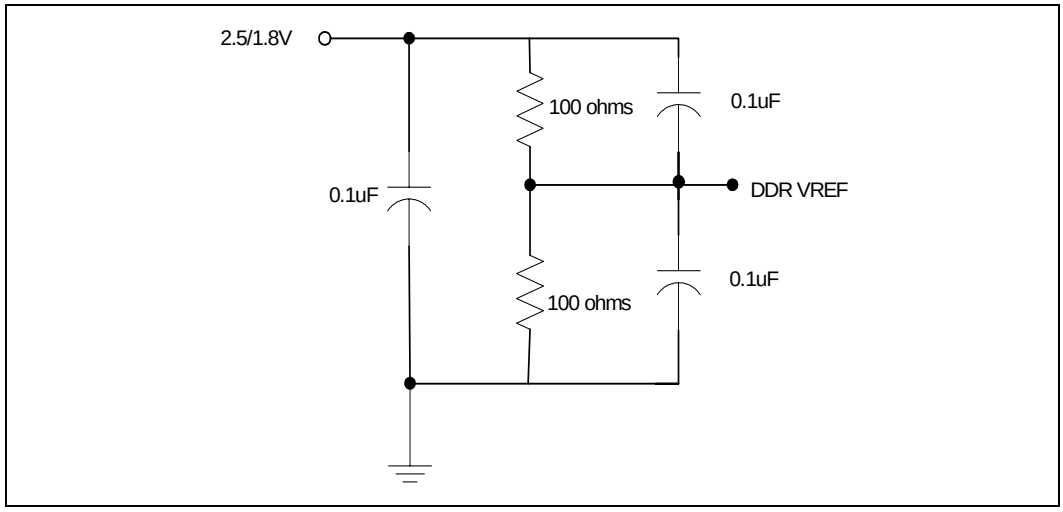
The **VTT** DDR termination voltage must track the **VDDQ** and provide the termination voltage to the termination resistors. This tracking must be 50 percent of (**VDDQ** - **VSSQ**) over voltage, temperature, and noise. It must maintain less than 40 mV offset from **VREF** over these conditions. This voltage must be low-impedance and source-significant current. The source and sink DC current for signal termination is at its absolute maximum current of 2.6 A-2.9 A for a 64/72-bit DIMM.

8.8 DDR V_{REF} Voltage

The Figure 71 shows the DDR Vref voltage. The DDR **VREF** is a low-current source (supplying input leakage and small transients). It must track 50 percent of (**VDDQ** -**VSSQ**) over voltage, temperature, and noise. Use a single source for **VREF** to eliminate variation and tracking of multiple generators. Maintain 15-20 mils clearance around other nets. Use a distributed decoupling scheme. Use a simple resistor divider with 1% or better accuracy.

Note: The 100 ohm resistors can be replaced with 1K +/- 1% resistors to minimize leakage current during battery backup mode.

Figure 71. DDR V_{REF} Circuit



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Peripheral Local Bus 9

The Peripheral Bus Interface Unit (PBI) is a data communication path to Flash memory components and peripherals of a 80333 hardware system. The PBI allows the processor to read and write data to these supported flash components and other peripherals. To perform these tasks at high bandwidth, the bus features a burst transfer capability which allows successive 8- or 16-bit data transfers.

The peripheral bus is controlled by the on-chip bus masters: the Intel XScale® core, the ATU, AAU and DMA units.

The address/data path is multiplexed for economy, and the bus width is programmable to 8-, and 16-bit widths. The PBI performs the necessary packing and unpacking of bytes to communicate properly across the 80333 Internal Bus.

The PBI unit includes two chip enables.The PBI chip enables activate the appropriate peripheral device when the address falls within one of the PBI's two programmable address ranges. Both address ranges incorporate functionality that optimizes an interface for Flash Memory devices.

9.1 Peripheral Bus Signals

Bus signals consist of two groups: address/data, and control/status.

9.1.1 Address/Data Signal Definitions

The address/data signal group consists of 26 lines. 16 of these signals multiplex within the processor to serve a dual purpose. During and address cycle ($T_{A)}$, the processor drives A[22:16] and **AD[15:0]** with the address of the bus access. At all other times, the **AD[15:0]** lines are defined to contain data. **A[2:0]** are demultiplexed address pins providing incrementing byte addresses during burst cycles.

9.1.2 Control/Status Signal Definitions

The control/status signals control peripheral device enables and direction. All output control/status signals are three-state.

The PBI pulses **ALE** (address latch enable) active high for one clock during T_A to latch the multiplexed address on **AD[15:2]** in external address latches.

A peripheral read may be either non-burst or burst. A non-burst read ends after one data transfer to a single location.

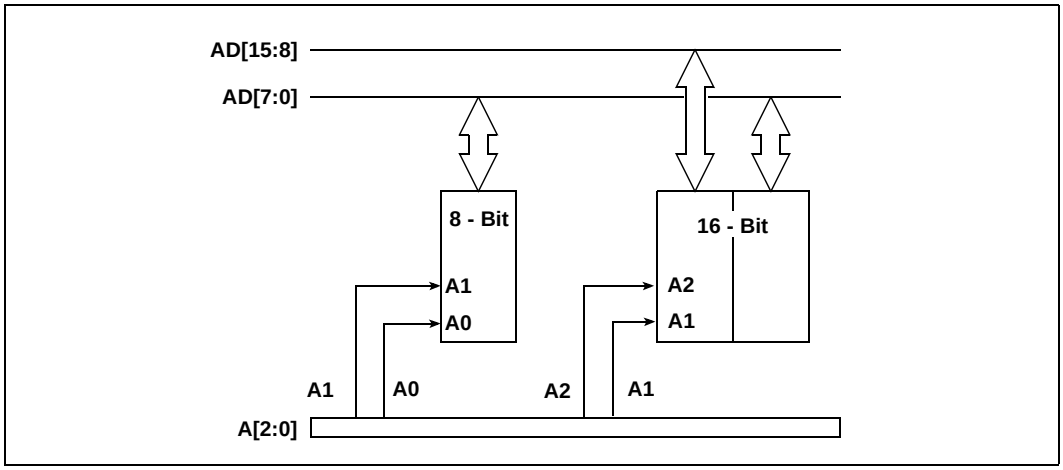
When the data bus is configured for 16 bits, demultiplexed address bits **A[2:1]** are used to burst across up to four short-words. For an 8-bit data bus, demultiplexed address bits **A[1:0]** are used to burst across up to four bytes.

Note: Burst write accesses to Flash Devices are not supported.

9.1.3 Bus Width

Each address range attributes are programmed in the PBIs boundary registers. The PBI allows an 8-, or 16-bit data bus width for each range. The PBI places 8- and 16-bit data on low-order data signals, simplifying the interface to narrow bus external devices. As shown in Figure 72, 8-bit data is placed on lines **AD[7:0]**; 16-bit data is placed on lines **AD[15:0]**.

Figure 72. Data Width and Low Order Address Lines



Flash memories need to be wired up in a manner consistent with the programmed bus width:

- 8-bit region: **A[1:0]** provide the demultiplexed byte address for a read burst.
- 16-bit region: **A[2:1]** provide the demultiplexed short-word address for a read burst.

Note: When using a 16 bit flash device mode A0 is a “don’t care”.

During initialization, bus width is selected for each of the two address ranges in the Peripheral Base Address Registers (PBBAR0 - PBBAR1). In addition, the PBBAR0-PBBAR5 can be used to configure these ranges as Peripheral Windows and to set a Wait state profile.

The PBI drives determinate values on all address/data signals during T_W/T_D write operation states. For an 8-bit bus, the PBI continues to drive address on unused data signals **AD[15:8]**.

9.1.4 Flash Memory Support

PBI peripheral bus interface supports 8-, or 16- bit Flash devices.

The PBI provides programmable wait state functionality for peripheral memory windows.

Note: Potentially, programmable wait state functionality could be connected to any peripheral device that has a deterministic wait state profile. However, data valid and turn-around times need to fit within parameters provided by programmable wait state profiles to support Flash devices.

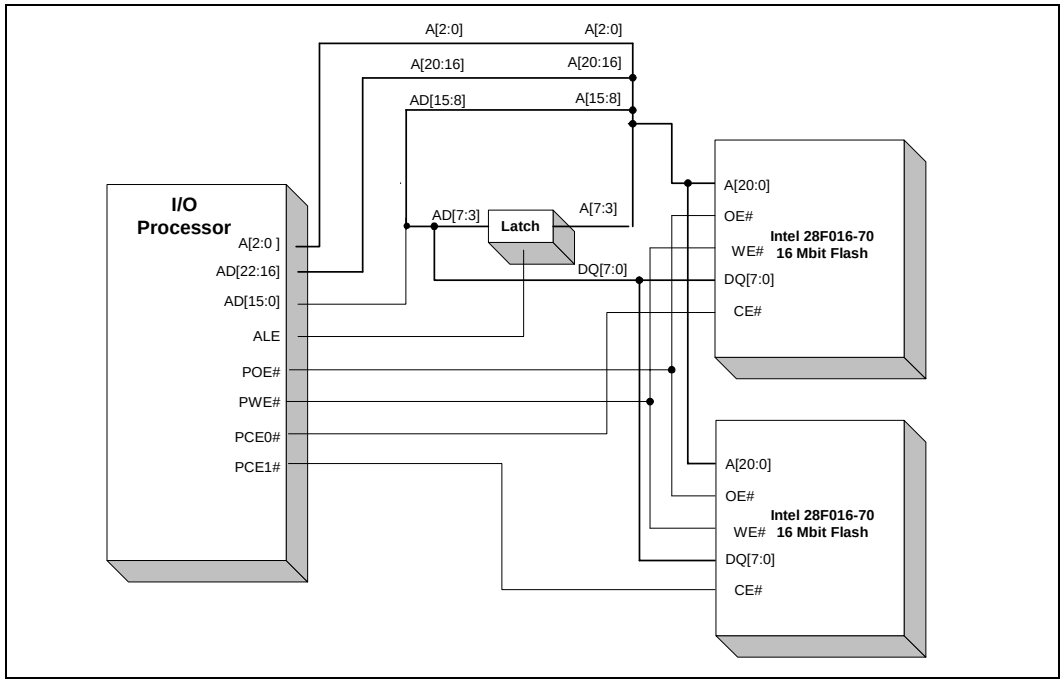
Any write transactions issued to a Flash address space window must always represent a single flash bus data cycle (**strb, strh**).

The peripheral chip enables, **PCE[1:0]#**, activate the appropriate Peripheral window when the address falls within one of the Peripheral address ranges.

Note: By default, bank 0 is enabled with the maximum number of Address-to-Data and Recovery Wait states. The width of the interface can be strapped for either 8-bit wide Flash or 16-bit wide flash. Thus, **PCE0#** is the Peripheral Bus chip enable to be used for booting purposes.

Figure 73 shows how two 8-bit Flash devices interface with through the PBI Interface.

Figure 73. Four MByte Flash Memory System[1]



1. 16-bit wide flash devices requires two latches.

Refer to Table 79 for the programmable address-to data and recovery wait states. These numbers are based on a 66 MHz internal clock for the PBI interface.

Table 79. Flash Wait State Profile Programming[1]

Flash Speed	Address-to-Data Wait States	Recovery Wait States
<= 55 ns	4	0
<= 115 ns	8	2
<= 150 ns	10	2

1. Each Wait State Represents 15 ns.

9.1.5 Layout Guidelines for the Peripheral Bus

This section provides basic layout guidelines for using the Peripheral Bus. Figures below provide the topology for simulation of clock, control and data lines.

Simulation Scope:

- Analysis consisted of an 8- or 16-bit address/data bus interfacing with one or two asynchronous flash devices operating at 66MHz.
- 50 ohm mother board and 60 ohm add-in card stackups were considered
- Lossy uncoupled transmission lines were used for the simulations
- Trace spacing were set 3X height of trace over reference plane to avoid crosstalk.
- The width of the bus (8/16 bits) and the number of flash devices yields six discrete topologies that were examined.
- Flash RC128J3A, CPLDs XC9500XL and Octal Latches 74LVC573A were used as loads in the SI analysis.

9.2 Topology Layout Guidelines

This section provides the topologies for routing the Address/Data bus for single load, latched single load and dual load latched topologies. Note that no length matching is required between the AD lines.

Figure 74. Peripheral Bus Unlatched Bidirectional Single Load Topology

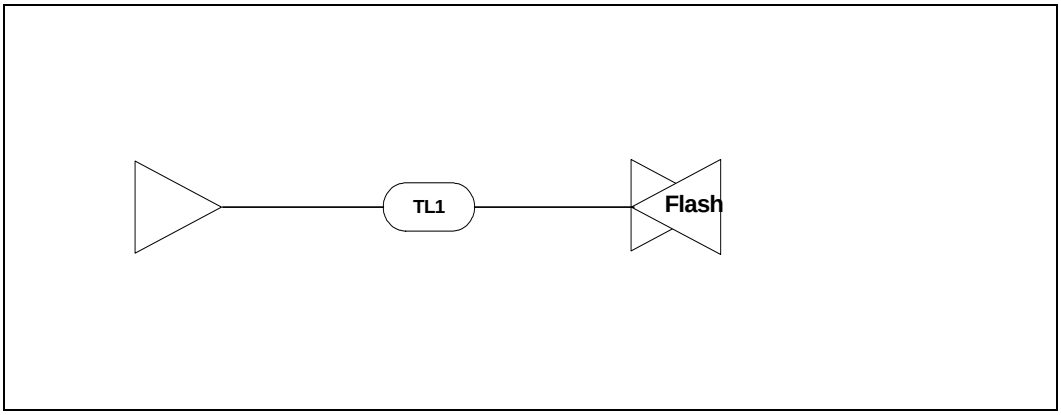


Table 80. Routing Guideline Bidirectional Single Load

Parameter	Routing Guidelines
Reference Plane	Route over unbroken ground plane or power plane. If routing over power plane maintain this consistency throughout the topology.
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils.
Routing	Microstrip or stripline or combination of microstip and stripline.
Motherboard Impedance (for both microstrip and stripline)	50 ohms +/- 15%
Add-in card Impedance (for both microstrip and stripline)	60 ohms +/- 15%
Trace Spacing (center to center)	• > 12 mils between all AD lines • > 20 mils must be maintained from all other signals or vias.
Trace Length TL1	2.0” to 10.0”
Trace Length to strapping resistors	0.5” to 3.0” from the last device on the bus.
Routing Recommendations	Number of vias for microstrip $\leq$ 2
	Number of vias for stripline $\leq$ 4

Figure 75. Peripheral Bus Latched Bidirectional Single Load Topology

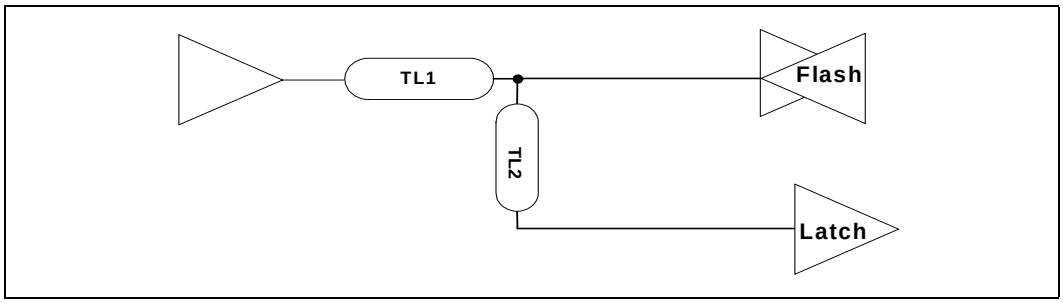


Table 81. Routing Guideline Latched Bidirectional Latch Single Load

Parameter	Routing Guidelines
Reference Plane	Route over unbroken ground plane or power plane. If routing over power plane maintain this consistency throughout the topology.
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils.
Routing	Microstrip or stripline or combination of microstip and stripline.
Motherboard Impedance (for both microstrip and stripline)	50 ohms +/- 15%
Add-in card Impedance (for both microstrip and stripline)	60 ohms +/- 15%
Trace Spacing (center to center)	• > 12 mils between all AD lines • > 20 mils must be maintained from all other signals or vias.
Trace Length TL1	2.0” to 10.0”
Trace Length to TL2	0.5” to 2.0”
Trace Length to strapping resistors	0.5” to 3.0” from the last device on the bus.
Routing Recommendations	Number of vias for microstrip ≤ 2
	Number of vias for stripline ≤ 4
	Route as daisy-chain only.
	Address latches for 16 bit implementations may be in any of the device locations for ease of routing.

Figure 76. Peripheral Bus Latched Bidirectional Two Load Topology

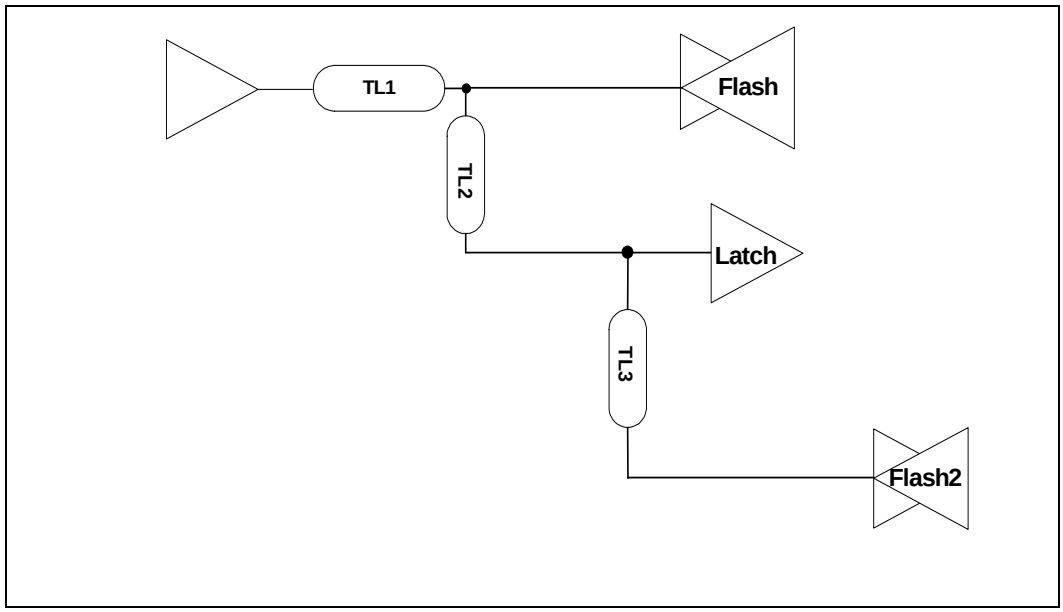


Table 82. Routing Guideline Latch Bidirectional Two Loads

Parameter	Routing Guidelines
Reference Plane	Route over unbroken ground plane or power plane. If routing over power plane maintain this consistency throughout the topology.
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils.
Routing	Microstrip or stripline minimize the layer changes.
Motherboard Impedance (for both microstrip and stripline)	50 ohms +/- 15%
Add-in card Impedance (for both microstrip and stripline)	60 ohms +/- 15%
Trace Spacing (center to center)	16 mils (for microstrip 60 ohms or stripline 50/60 ohms) to 20 mils (for microstrip 50 ohms)
Trace Spacing (center to center)	• > 12 mils between all AD lines • > 20 mils must be maintained from all other signals or vias.
Trace Length TL1	2.0” to 10.0”
Trace Length TL2, TL3	0.5” to 2.0”
Trace Length to strapping resistors	0.5” to 3.0” from the last device on the bus.
Routing Recommendations	Number of vias for microstrip $\leq$ 2
	Number of vias for stripline $\leq$ 4
	Route as daisy-chain only.
	Address latches for 16 bit implementations may be in any of the device locations for ease of routing.

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Power Delivery 10

There are several different voltage domains needed on the 80333. These include the following listed in Table 83:

Table 83. Intel® 80333 I/O Processor Bias Voltages

Voltage Supply	Voltage
PCI/Miscellaneous	3.3V
VCCBG[1]	2.5V
DDRI	2.5V
DDRII	1.8V
IOP Core Voltage	1.5V
Intel XScale® core Voltage	1.35V
DDRI Vref	1.25V
DDRII Vref	0.9V

NOTE: [1] VCCBG can be derived from 3.3V rail using a linear regulator TL431.

10.1 Power Sequencing

The 80333 requires that the VCC33 voltage rail be powered up first and then the VCC15. Note that there are no sequence order requirements for the VCC25 or VCC18 rail. The power down sequence is the same in the reverse order.

1) VCC33 power up first

2) VCC15 power up second

The VCC33 greater than or equal to (or no less than 0.5V below) VCC15 (absolute voltage value) at all times during operations, including during system power-up and power-down. In other words, the following must always be true:

VCC33 >= (VCC15 - 0.5V)

- This can be accomplished by placing a diode (with a voltage drop < 0.5V) between VCC15 and VCC33. an Anode is connected to VCC15 and a cathode is connected to VCC33.
- If a voltage regulator solution is used which shunts VCC15 to ground while VCC33 is powered, the maximum allowable time that VCC15 can be shunted to ground while VCC33 is fully powered is 20ms.
- The maximum allowed time between VCC33 and VCC15 ramping is 525ms. There is no minimum sequencing time requirement.
- Also, all 80333 voltage rails must be stable and within their operating ranges before the PCI Express differential clocks REFCLK+ and REFCLK- begin running. This is a requirement for all devices with PCI Express interfaces.

10.2 Power Failure

This section describes the power failure sequence and associated circuitry that is needed to prevent data loss during a power failure. While the host assumes all written data is stored on the non-volatile disk subsystem, the IOP must ensure that eventually all the data in the disk cache is actually stored onto disk. The power supply could fail to provide power to the I/O subsystem in the case of a power outage or a failed power supply. It is imperative that the cached data within the IOP's local memory is not lost. If power fails, the local memory subsystem must remain powered with a battery backup and some agent must continue to refresh at the appropriate interval specified by the memory component datasheet.

10.2.1 Theory of Operation

DDR SDRAM technology provides a simple way of enabling data preservation through the **self-refresh** command. This command is issued by the memory controller and the DDR SDRAM will refresh itself autonomously with internal logic and timers. The DDR SDRAM device will remain in self-refresh mode as long as:

1. The device continues to be powered.
2. **CKE** is held low until the memory controller is ready to control the DDR SDRAM once again.

Power to the DDR SDRAM subsystem is ensured with an adequate battery backup and a reliable method for switching between system power and battery power. The memory controller is responsible for deasserting **CKE[1:0]** when issuing the **self-refresh** command but while power gradually drops, **CKE[1:0] must** remain deasserted regardless of the state of V_{CC} powering the 80333.

10.2.2 Power Failure Sequence

Upon initial power-up, a power supply provides appropriate voltage to the system. The voltage level increases at a rate dependent on the type of power supply used and components in the system. These variables are not certain, so the power supply often provides a signal called **PWRGD,** which indicates when the voltage has reached a reliable level. The power supply deasserts **PWRGD** when the voltage level drops below a certain minimum threshold. *PCI Local Bus Specification*, Revision 2.2 indicates that once **PWRGD** is deasserted, the PCI reset pin (**P_RST#**) is asserted in order to float the output buffers. In the specification, T_{fail} is defined as the time when **P_RST#** is asserted in response to the power rail going out of specification. T_{fail} is the minimum of:

- 500 ns from either power rail going out of specification (exceeding specified tolerances by more than 500 mV).
- 100 ns from the 5 V rail falling below the 3.3 V rail by more than 300 mV.

For storage applications, it is imperative that data cached within DDR memory system not be lost in a power failure condition. To prevent this from happening the local DDR memory needs to be saved with provisions for battery backup, to allow DDR data to be saved using the refresh mode at an appropriate interval until power is restored. The DDR has a self-refresh command that can be invoked as long as the device remains powered and **CKE** is held low. Power to DDR SDRAM is ensured with an automatic switch over to backup battery power when the system power is lost. Battery backup needs to maintain power on DDR voltages $\mathbf{V_{DD}}$, $\mathbf{V_{DDQ}}$ and $\mathbf{V_{REF}}$ to prevent data loss. Refer to the *Intel® 80333 I/O Processor Developer's Manual*, for more information about this Power Failure Mode.

10.3 Power Failure Circuitry

In a PCI-X or PCI-Express system the central resource will generate a P_RST# or PERST# (PE_RST#) once the system power is stable. The central resource (for example the IO Controller Hub) monitors a POWERGOOD signal that will be assert once the power supply is turned on and stable. On the CRB this reset signal becomes PE_PWRGD (POWERGOOD) and is connected to the **PWRGD** signal on the IOP and is used throughout the board to signal valid power.

10.3.1 Power Delay

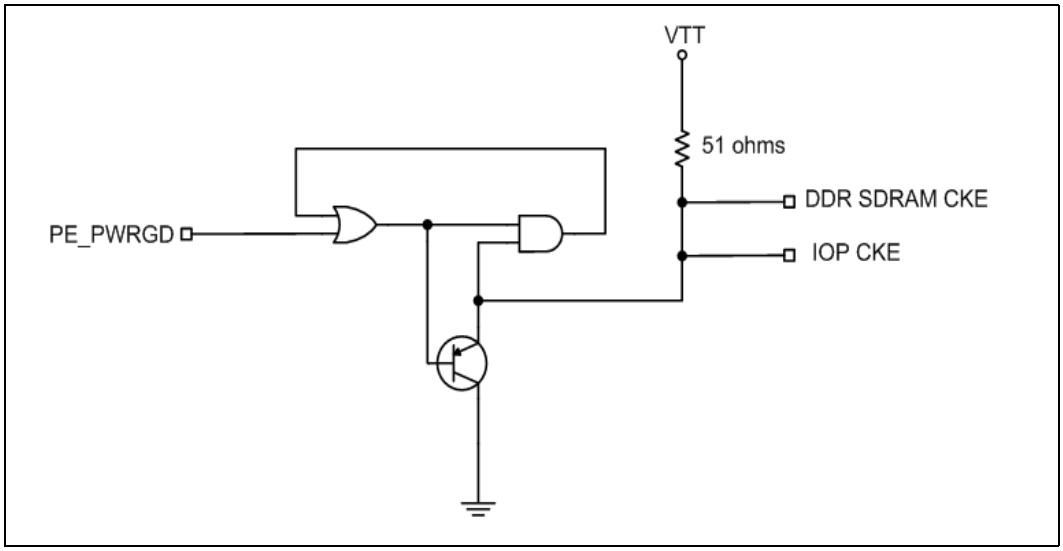
The 80333provides a dedicated input pin, **PWRDELAY** that will be used to distinguish between and initial power up and a power failure assertion of **PWRGD.** This signal should be pulled up with a 1.5K resistor.

10.4 Battery Backup

With a self-refresh command the DDR is able to store data. After a self-refresh command, the DDR refreshes itself autonomously with internal logic and timers. The DDR SDRAM remains in self-refresh mode as long as **CKE[1:0]** are low. CKE signals will stay low providing the DDR voltage is not removed from 80333. If 80333 is isolated from the DDR battery voltage it is recommended that the CKE circuit shown in Figure 77 be implemented. The **CKE** latch circuitry in Figure 77 is battery powered. It allows maintaining the **CKE[1:0]** signals low while the system power is off. The latches are cleared when the 80333 drives **CKE[1:0]** low with a self-refresh command and are reset when **PWRGD** is driven from low to high after system power is recovered. During normal operation, the **CKE** signals are controlled by the 80333. When the power is turned off, the battery powered latches pull the **CKE** signals low using the two transistors.

Note: It is recommended that the power planes for battery backup and the IOP power be isolated to avoid battery drain due to leakage when in battery backup mode. This can be implemented with a FET that isolates these planes during battery backup mode.

Figure 77. SCKE Circuit



10.4.1 Non-Battery Backup Circuits

For applications not supporting battery back-up, this circuit not required. When so, follow these steps:

- Pull DDR **CKE** pins high and leave **CKE** signals on 80333 as ‘no connects’. This keeps SDRAM from entering a pseudo, self-refresh mode, which can cause a lock-up condition on the SDRAM device.
- Pull the **PWRDELAY** pin low through a 1.5 K pull-down. Pulling it low has the effect of keeping the power fail state machine in reset, therefore not allowing the power fail sequence to ever occur.

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Intel® 80333 I/O Processor Evaluation Board 11

The Intel® 80333 Evaluation Board (IQ80333), also known as the evaluation board, is implemented as aPCI Express add-in card. In addition, the board needs to also be able to operate in a powered PCI Express backplane with no host processor.

This section provides an overview of the IQ80333 features and describes the circuits specific to the IQ80333.

Table 84. IQ80333 Features (Sheet 1 of 2)

Feature	Details
Form Factor	Full-length, extended-height PCI card (311mm x 176mm).
Processor	• Integrated Intel XScale® microarchitecture. • 500 MHz, 667 MHz and 800 MHz core frequencies supported. • 500 MHz and 667 MHz are supported when DDR 333 is used.
Memory	DDR: • Double Data Rate II (DDRII) SDRAM. • One vertical DDRII SDRAM DIMM socket. • Battery Back-up.
	Flash Memory 8 MBytes Intel StrataFlash 16-bit interface.
	Non-Volatile RAM (NVRAM) 2 Kbytes serial I^2C EEPROM.
Ethernet	• Intel Gigabit Ethernet controller. • 82545EM MAC/PHY.
I/O Connectors	• PCI Express – 8-lane edge connector. • PCI-X (IOP Bus) – 64-bit card slot connector - 100 MHz. • PCI-X Bus – 64-bit slot connector - 133 MHz. • One vertical DDRII SDRAM DIMM socket. • One RJ45 Gigabit Ethernet port with integrated LEDs and magnetics on bracket. • Dual RJ11 serial port connectors on the bracket.
Headers	• Interrupt & misc. header. • GPIO header. • 3-pin headers for each I^2C bus. • Peripheral bus debug/expansion header • 20 pin JTAG connector for the CPU and CPLD
Logic Analyzer Probe Pads	• Provide access through standard connectors (i.e. PCI-X, PCI Express, DDRII).

Table 84. IQ80333 Features (Sheet 2 of 2)

Feature	Details
Miscellaneous. Functions	Temperature sensor.
	Two 7-Segment LED Displays for debug.
	Compact Flash
	Audible Alarm (Buzzer).
	Power On LED (Green) Indicators for each power plane.
	CPLD • Peripheral bus address latch and data buffers. • Misc. logic collection. • Misc. registers (Revision ID, rotary switch, etc.). • Address decode.

Figure 78. IQ80333 Block Diagram

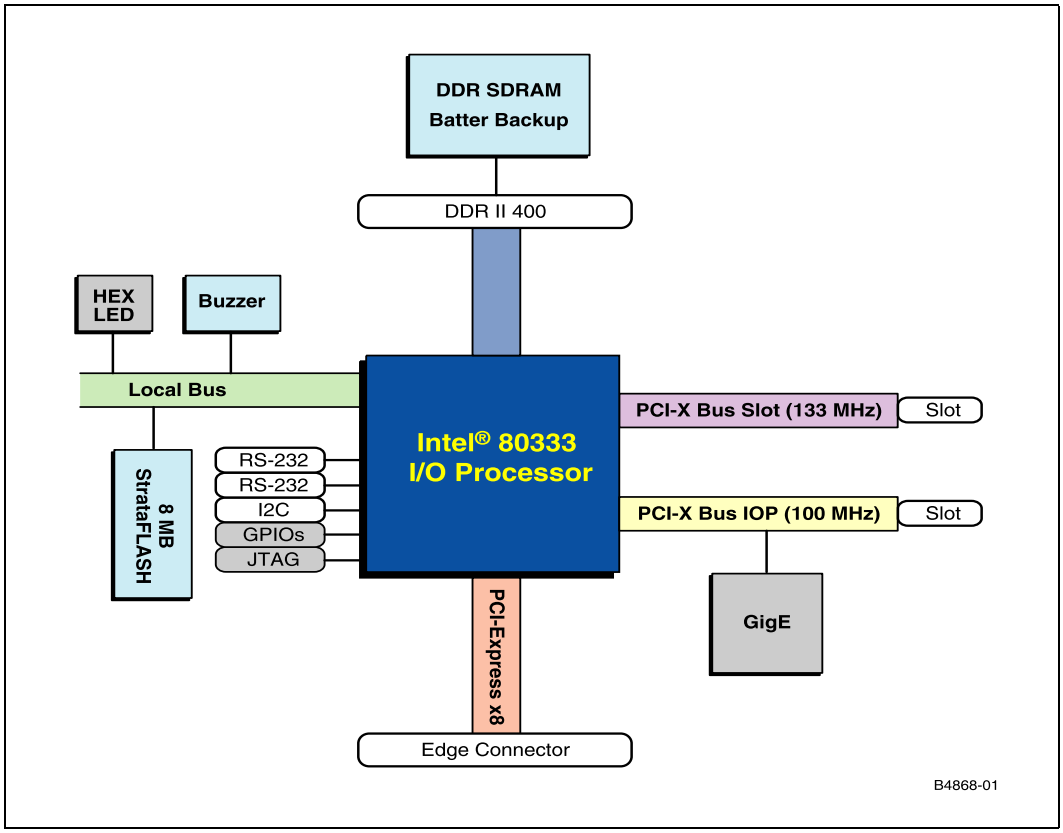

Figure 79. IQ80333 Form Factor

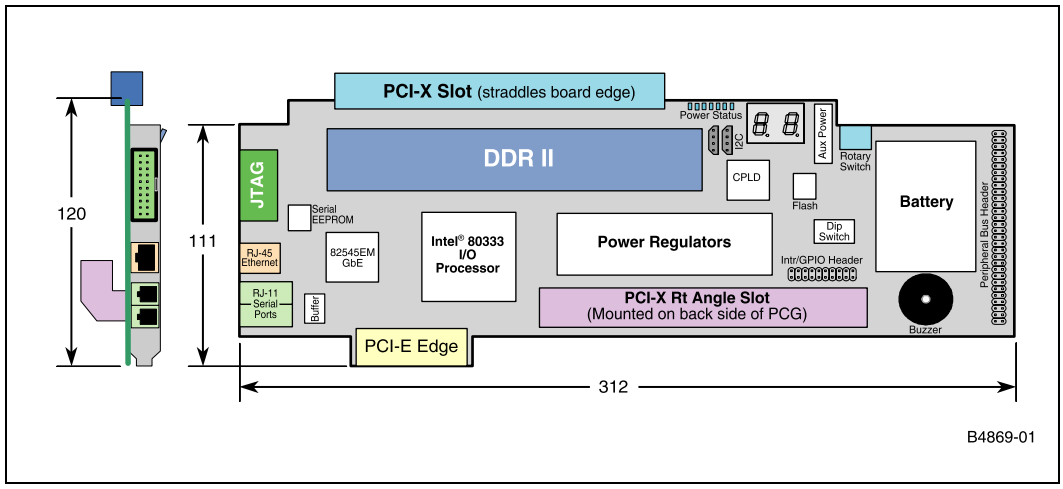

Table 85. Intel® 80333 I/O Processor CPU Frequencies and DDR Configuration

DDR 333	DDR II 400
500 MHz	500 MHz
667 MHz	800 MHz

CPU Frequencies and the IQ80333 provide the following memory features:

- DDRII (400) SDRAM DIMM socket supporting the following configurations:
- Registered with ECC
- Single sided or double sided DIMMs supported
- I^2C bus for SDRAM serial presence detection

Table 86 lists the supported DDR II DIMM configurations. This is based on advanced information, and configuration may not be available from the memory vendors.

Table 86. DDR II DIMM Configurations

Speed	Capacity	Organization	CAS Latency	Features
DDRII 400	(128MB)	16MX72	3, 4	ECC Registered DIMM
DDRII 400	(256MB	32MX72	3, 4	ECC Registered DIMM
DDRII 400	(512MB)	64MX72	3, 4	ECC Registered DIMM
DDRII 400	(1 GB)	128MX72	3, 4	ECC Registered DIMM

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JTAG Circuitry for Debug 12

Certain restrictions exist in order to use JTAG based debuggers with the Intel XScale® microarchitecture. This is primarily due to the Tap Controller reset requirements of the Intel XScale® microarchitecture and the reset requirements of specific JTAG debuggers. The following outlines these requirements along with suggestions for circuitry to alleviate potential problems

12.1 Requirements

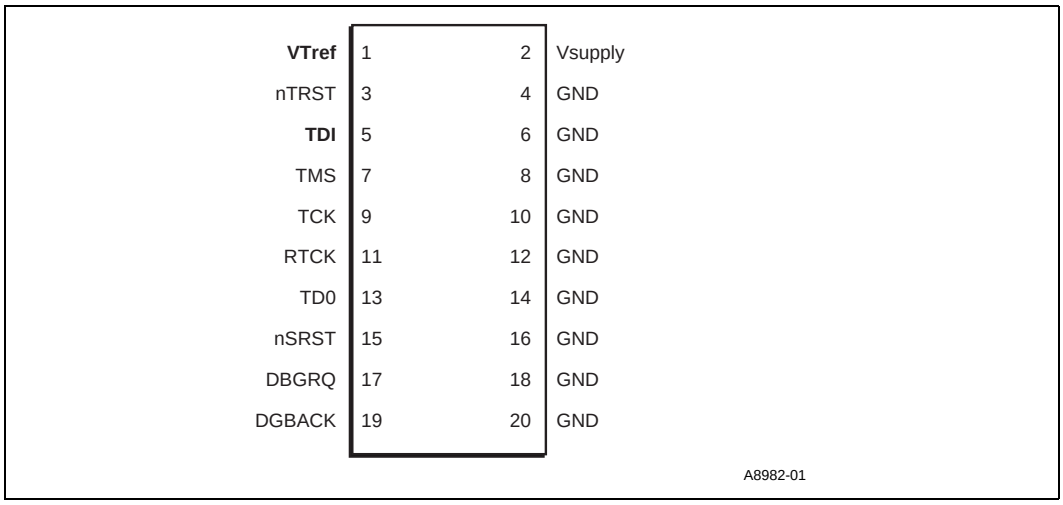
The Intel® 80333 I/O Processor (80333), like many others, requires that nTRST (Tap Reset) is asserted during power up. This is to ensure a fully initialized boundary scan chain. Failure to comply with this requirement may result in spurious behavior of the application.

The ARM* Multi-ICE* JTAG debugger requires that nTRST is always weakly pulled high. This requirement stems from the fact that the debugger can only assert nTRST (drive low). Both reset signals coming from the Multi-ICE™ (nTRST and nSRST) are open collector and must be weakly pulled high in order to avoid unintentional resets (System or TAP).

12.2 JTAG Signals / Header

Figure 80 is the pin definition (20-pin standard ARM connector) for JTAG.

Figure 80. JTAG Header Pin Out



The ARM Multi-ICE debugger along with the Macraigor Raven* and WindRiver Systems* visionPROBE / visionICE utilize this connector. The main difference to be noted is the specific implementation of nTRST for each debugger. The Macraigor Raven implementation actively drives nTRST (high and low). The WindRiver Systems* visionPROBE / visionICE can configure nTRST active or open collector (only drive low). ARM Multi-ICE is configured as open collector only.

12.3 System Requirements

In order to successfully invoke a debug session, the JTAG debug unit must be able to control nTRST and nSRST independently. The nTRST signal allows the debugger to get the TAP controller in a known state. The nSRST signal allows the debugger to control system/processor reset in order to download the debug handler via the JTAG interface.

Figure 81 and Figure 82 are used as examples without reflecting actual signal timings.

Figure 81. JTAG Signals at Powerup

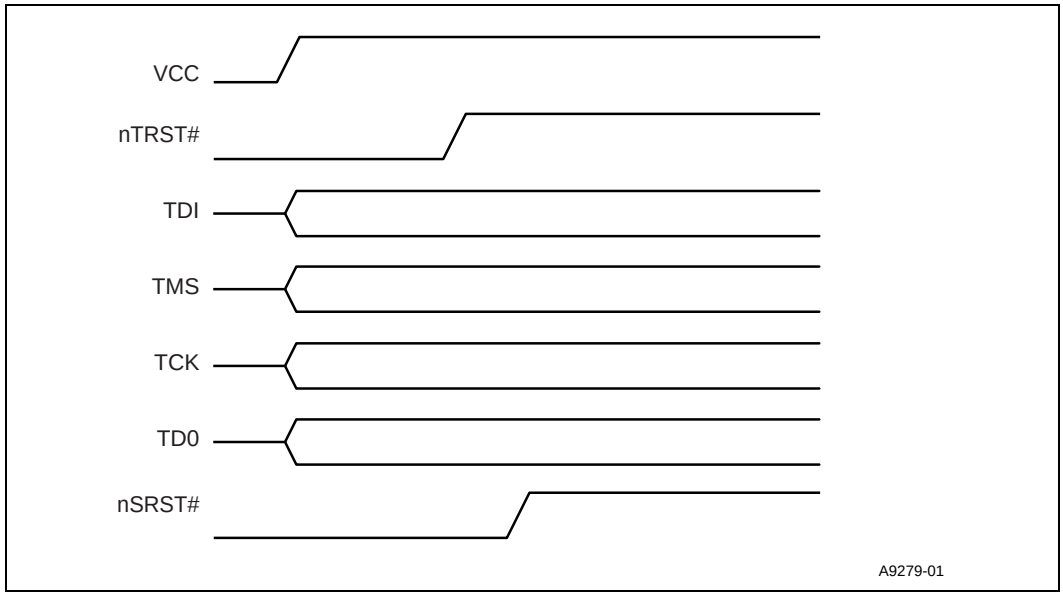
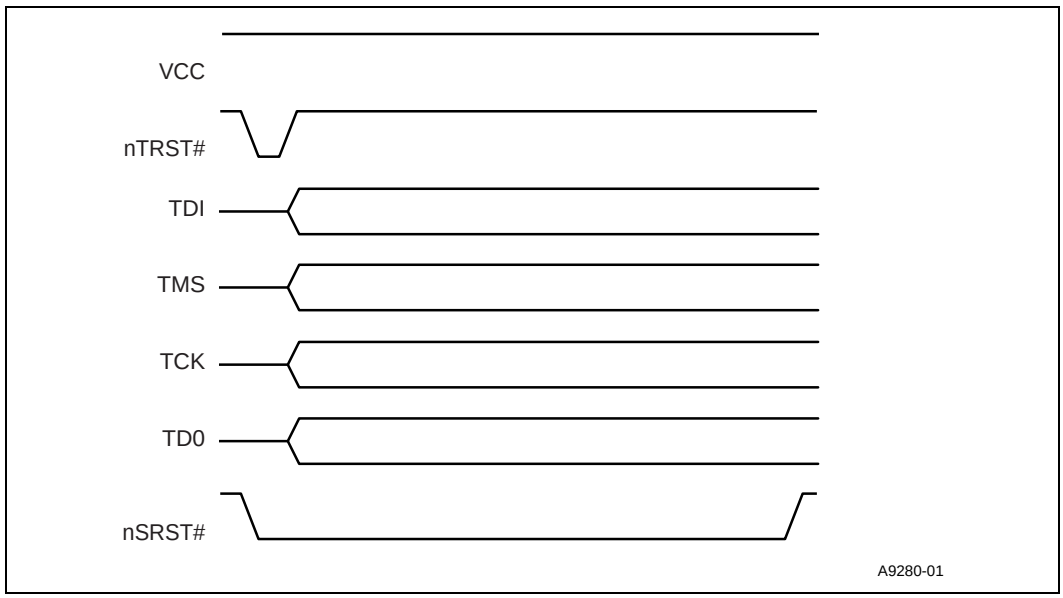


Figure 82. JTAG Signals at Debug Startup



12.4 JTAG Hardware Requirements

Due to the conflicting requirements of Multi-ICE* and the Intel XScale® microarchitecture, it is necessary to incorporate a circuit that can drive **TRST#** low at power up and weakly pull it high at all other times. The following section details the circuits required for the Macraigor Raven*, WindRiver Systems* visionPROBE* / visionICE*, and ARM* Multi-ICE*.

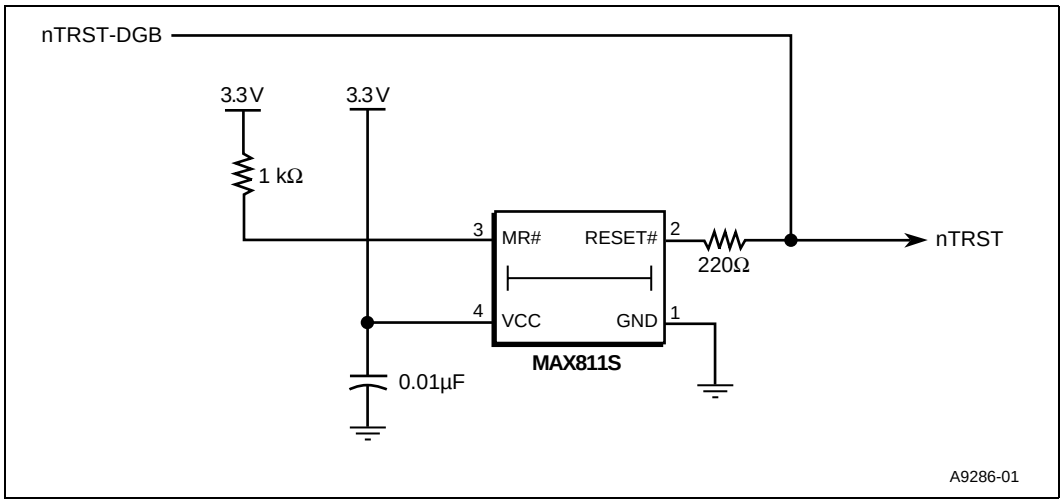
12.4.1 Macraigor Raven and WindRiver Systems visionPROBE / visionICE

Both the Macraigor Raven and WindRiver Systems visionPROBE / visionICE (when configured as active) do not require any special power-up circuitry. The requirement is that nTRST is weakly pulled down at the processor. It is suggested that the value of the pull-down resistor is 10 KΩ or greater. The value of this resistor needs to be confirmed with the JTAG debugger manufacturer to ensure optimal performance.

12.4.2 ARM Multi-ICE

The ARM Multi-ICE debugger requires special power-up circuitry due to the open collector implementation of the nTRST signal. This power-up circuit must ensure that nTRST is asserted (low) at power on and weakly pulled high thereafter. Refer to Figure 83 for the example of the Power-Up Circuit for nTRST.

Figure 83. Example Power-Up Circuit for nTRST



Debug Connectors and Logic Analyzer Connectivity 13

13.1 Probing PCI-X Signals

To ease the probing and debug of the PCI-X signals it is recommended to passively probe the PCI-X bus signals with a logic analyzer. This can be accomplished by placing six AMP* Mictor-38 connectors on the board or probing the bus with an interposer card such as the FuturePlus Systems* FS2007 that works with an Agilent Technologies* Logic Analyzer.

For ease of debugging the pin out of the AMP Mictor-38 connectors, the recommended pin-out matches the FuturePlus Systems* configuration setup, which allow ease of viewing the PCI signals on an Agilent Technologies* Logic Analyzer. Refer to the following test equipment that is used for this analysis:

- Two AMP 2-767004-2 surface mount connectors mounted on the target board and routed to the PCI-X Local bus.
- Two Agilent E5346A or E5351A High-Density Adapter Cables from FuturePlus System or Agilent Technologies.
- Four logic analyzer PODS.
- FS1104 Software from FuturePlus.

The equivalent for other analyzers can be substituted. A FuturePlus Systems configuration file with the FS1104 product that matches the pinout in Table 87.

Table 87. Logic Analyzer Pod 1

Mictor-38 #1 Pin Number Odd Pod	Logic Analyzer Channel Number	PCI-X Name
6	CLKC/16	CLK
8	15	C/BE4
10	14	C/BE5
12	13	C/BE6
14	12	C/BE7
16	11	ACK64
18	10	REQ64
20	9	UNUSED
22	8	PME
24	7	C/BEO
26	6	M66EN
28	5	C/BE1
30	4	SERR
32	3	PAR
34	2	PERR
36	1	LOCK
38	0	STOP

Table 88. Logic Analyzer Pod 2

Mictor-38 #1 Pin Number Odd Pod	Logic Analyzer Channel Number	PCI-X Signal Name
5	CLK/16	FRAME
7	15	DEVSEL
9	14	TRDY
11	13	C/BE2
13	12	C/BE3
15	11	IDSEL
17	10	REQ
19	9	GNT
21	8	INTD
23	7	INTC
25	6	INTB
27	5	INTA
29	4	UNUSED
31	3	UNUSED
33	2	UNUSED
35	1	UNUSED
37	0	UNUSED

Table 89. Logic Analyzer Pod 3

Mictor-38 #2 Pin Number Odd Pod	Logic Analyzer Channel Number	PCI-X Signal Name
6	CLK/16	IRDY
8	15	AD15
10	14	AD14
12	13	AD13
14	12	AD12
16	11	AD11
18	10	AD10
20	9	AD09
22	8	AD08
24	7	AD07
26	6	AD06
28	5	AD05
30	4	AD04
32	3	AD03
34	2	AD02
36	1	AD01
38	0	AD00

Table 90. Logic Analyzer Pod 4

Mictor-38 #2 Pin Number Odd Pod	Logic Analyzer Channel Number	PCI-X Signal Name
5	CLK/16	UNUSED
7	15	AD31
9	14	AD30
11	13	AD29
13	12	AD28
15	11	AD27
17	10	AD26
19	9	AD25
21	8	AD24
23	7	AD23
25	6	AD22
27	5	AD21
29	4	AD20
31	3	AD19
33	2	AD18
35	1	AD17
37	0	AD16

Table 91. Logic Analyzer Pod 5

Mictor-38 #3 Pin Number Odd Pod	Logic Analyzer Channel Number	PCI-X Signal Name
6	CLK/16	PAR64
8	15	AD47
10	14	AD46
12	13	AD45
14	12	AD44
16	11	AD43
18	10	AD42
20	9	AD41
22	8	AD40
24	7	AD39
26	6	AD38
28	5	AD37
30	4	AD36
32	3	AD35
34	2	AD34
36	1	AD33
38	0	AD32

Table 92. Logic Analyzer Pod 6

Mictor-38 Pin Number Even Pod	Logic Analyzer Channel Number	PCI-X Signal Name
5	CLK/16	Unused
7	15	AD63
9	14	AD62
11	13	AD60
13	12	AD59
15	11	AD58
17	10	AD57
19	9	AD56
21	8	AD55
23	7	AD54
25	6	AD53
27	5	AD52
29	4	AD51
31	3	AD50
33	2	AD49
35	1	AD48
37	0	AD48

The recommended placement of the mictor connectors is at either end of the bus segment. The mictors are placed at the end of, as short a stub as possible, daisy chained off either end of the bus. When there is not enough room to place the mictors **0.5 inches** from the target, then an alternate method may be used. That is, to place the logic analyzer termination circuitry on the target and then extend the etch from the end of the termination circuitry over to the mictor connectors. The connection from the mictors to the logic analyzer must then be done with the **E5351A.** The **E5346A** contains the logic analyzer termination circuitry, the **E5351A** does not.

13.2 PCI-Express Debugging

Debugging your PCI-Express 80333 design needs to primarily require analysis at the physical layer to check verify your layout and the transaction layer to make sure that the read and write request packets are being transmitted correctly (data link layer can be checked as well to make sure that 80333 is providing the correct sequence number and CYC to the transaction-layer packet).

13.2.1 Physical Layer Debugging

For PCI Express, the fundamental signaling frequency is 1.25GHz (half the bit rate) and the specified 20-80 rise-time is 100 ps. The Tektronix™TDS6604 Real-Time Digital Storage Oscilloscope and the Agilent Technologies ™ 54855A provides an analog bandwidth of 6 GHz (with a 20GSa/sec sampling rate) sufficient to measure the PCI-Express differential signals with their respective differential probes.

Alternative equipment to the high speed oscilloscopes include a Vector Network Analyzers or a Time Domain Reflectometry (TDR) scopes can help to pinpoint signal integrity of PCBs and connectors. Test Equipment that allows check if the lane-to-lane skew, analyze jitter and measure drive strength and receiver tolerance can also be checked at the physical layer. For more information on using TDR analysis the below link application note from Tektronix may be useful TDR Impedance Measurements: A Foundation for Signal Integrity.

13.2.2 Transaction Layer Testing

The Transaction layer can be debugged and validated with PCI-Express protocol analyzers. Agilent Technology has a PCI Express Packet Analysis Probe that works in conjunction with their 16700 family of logic analyzers as well as a PCI Express Analyzer/Exerciser that be introduced in the coming months. For more information on the PCI Express test equipment refer to Intel's PCI-Express Developer's website http://www.pciexpressdevnet.org/kshowcase/.

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References 14

14.1 Related Documents

The following books and specifications may be helpful for designing with the Intel® 80333 I/O processor.

Table 93. Design References

Design References
Transmission Line Design Handbook, Brian C. Wadell
Microstrip Lines and Slotlines, K. C. Gupta. Et al.
PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a
*PCI-X Electrical Subgroup Report, Version*1.0
Design, Modeling and Simulation Methodology for High Frequency PCI-X Subsystems, Moises Cases, Nam Pham, Dan Neal www.pcisig.com
PCI Local Bus Specification, Revision 2.3 PCI Special Interest Group 1-800-433-5177
High-Speed Digital Design "A Handbook of Black Magic" Howard W. Johnson, Martin Graham
PCI Express Specification, Revision 1.0a
PCI Bus Hot-Plug Specification, Revision 1.1 – PCI Special Interest Group
PCI Bus Power Management Interface Specification, Revision 1.1 – PCI Special Interest Group
"Terminating Differential Signals on PCBs", Steve Kaufer, Kelee Crisafulli, Printed Circuit Design, March 1999
"Board Design Guidelines for PCI Express™ Interconnect", http://www.intel.com/technology/pciexpress/downloads/PCI_EI_PCB_Guidelines.pdf

Intel documentation is available from your local Intel Sales Representative or Intel Literature Sales.

To obtain Intel literature write to or call:

Intel Corporation
Literature Sales
P.O. Box 5937
Denver, CO 80217-9808
(1-800-548-4725) or visit the Intel website at http://www.intel.com

Table 94. Intel Related Documentation

Document Title	Order #
Intel® Packaging Databook	240800

14.2 Electronic Information

Table 95. Electronic Information

The Intel World-Wide Web (WWW) Location:	http://www.intel.com
Customer Support (US and Canada):	800-628-8686