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LPMBX400BRD500 Interposer

Board Manual

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Order Number: 273298-001

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1.0 Introduction

This document introduces the LPMBX400BRD500 Interposer Board and provides installation instructions.

The LPMBX400BRD500 Interposer Board with the Intel[®] Mobile Pentium[®] III processor emulates the functionality of the Pentium III Processor Mobile Module to provide a bus interconnect for emulation and logic analysis tools. This board is used for Pentium III Processor Mobile Module system designs.

Note: Due to additional signal loading and trace lengths, the LPMBX400BRD500 Interposer Board may not function in all system designs.

1.1 Key Terms

- **LPM:** refers to the Low Power Pentium III Processor Module. This module is identical to the Intel Pentium III processor Mobile Module Connector (MMC-2). A complete description of this module is located in the *Intel*[®] *Pentium*[®] *III Processor Mobile Module Connector 2 (MMC-2)* Datasheet (http://developer.intel.com/design/mobile/datashts).
- **82443BX:** refers to the Intel[®] 82443BX Host Bridge Controller.

1.2 Related Documents

Table 1.Related Documents

| Document | Order Number |
|--|-----------------|
| Intel [®] Pentium [®] III Processor Mobile Module Connector 2 (MMC-2) Datasheet | 245304 |
| Intel [®] Pentium [®] III Processor in BGA2 and Micro-PGA2 Packages at 400 MHz, 450MHz and 500 MHz Datasheet | 245302 |
| Intel [®] Pentium [®] III Processor Specification Update | 245306 |
| Intel® 440BX AGPset: 82443BX Host Bridge/Controller Datasheet | 290633 |
| AP-524 Pentium [®] Pro Processor GTL+ Guidelines Application Note | 242765 |
| AP-525 Pentium [®] Pro Processor Thermal Design Guidelines Application Note | 242766 |



1.3 Vendor References

Table 2.Vendor References

| Vendor Name [†] | Contact Information | | |
|--|--|--|--|
| American Arium | (714) 731-1661 http://www.arium.com/aaprod.htm | | |
| Applied Microsystems Corporation | (800) 426-3925 http://www.amc.com | | |
| Hewlett Packard | (800) 452-4844 http://www.tmo.hp.com | | |
| Microtek International | (800) 886-7333 http://www.microtekintl.com | | |
| Tektronix | (800) TEK-WIDE http://www.tek.com | | |
| Ironwood Electronics (for adapters only) | (800) 404-0204 http://www.ironwoodelectronics.com | | |

† Intel does not endorse or recommend third-party vendors.

1.4 Intel[®] Pentium[®] III Processor Mobile Module: Mobile Module Connector 2 or Low Power Pentium III Processor Module

The Pentium III Processor Mobile Module: Mobile Module Connector 2 (400-pin MMC-2) or Low Power Pentium III Processor Module (LPM) is a small, highly integrated assembly containing an Intel Pentium III processor with on die level 2 (L2) cache memory and its immediate system-level support. Specifically, the processor module contains a power regulator and the core logic required to bridge the processor to standard system buses. The module interfaces electrically to its host system via a 3.3 V AGP bus, a 3.3 V PCI bus, a 3.3 V memory bus and some Intel 82443BX Host Bridge Controller signals. Refer to Table 1 for a list of related documents.

1.5 LPMBX400BRD500 Interposer Board Features

The LPMBX400BRD500 Interposer Board contains the same system level support provided by the Pentium III processor mobile module with a few exceptions.

- It includes a 80-pin connector for the Voltage Regulator Module (VRM)
- It provides a few 2-pin headers for power consumption measurement
- It provides two additional interfaces for debug tools:
 - 30-pin debug port connector
 - 190-pin processor system bus connector

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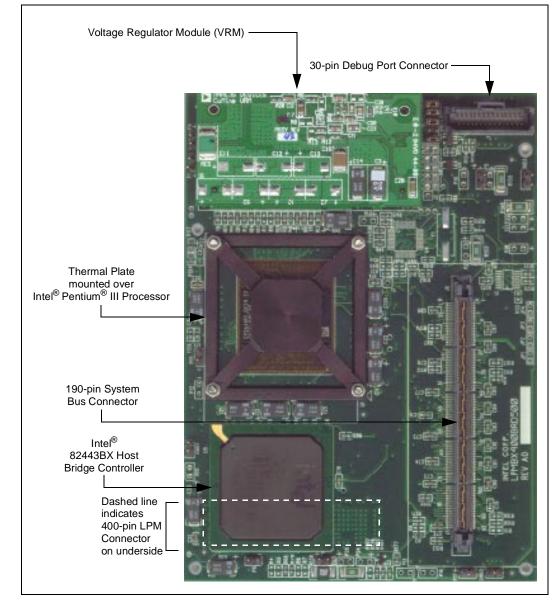


Figure 1. Top View of LPMBX400BRD500 Interposer Board Assembly

The same 400-pin system interface is still provided to allow connection to the target system and maintain the compatible functionality with the Pentium III processor Mobile Module.

The 30-pin debug port connector connects to the run control cable, or debug port, of the emulator or logic analyzer. The 190-pin processor system bus connector connects directly to the emulator or logic analyzer bus preprocessor. This connection allows for full bus trace and triggering. Contact your emulator or logic analyzer vendor for specific tool capabilities. See Table 2 for a reference list of vendors.



1.6 LPMBX400BRD500 Interposer Board Dimensions

This section provides the physical dimensions for the LPMBX400BRD500 Interposer Board.

Note: Notice in Figure 2 the mechanical clearance requirements for the LPMBX400BRD500 Interposer Board compared to the Low Power Module (LPM).

Figure 2. LPMBX400BRD500 Keepout Space Requirements

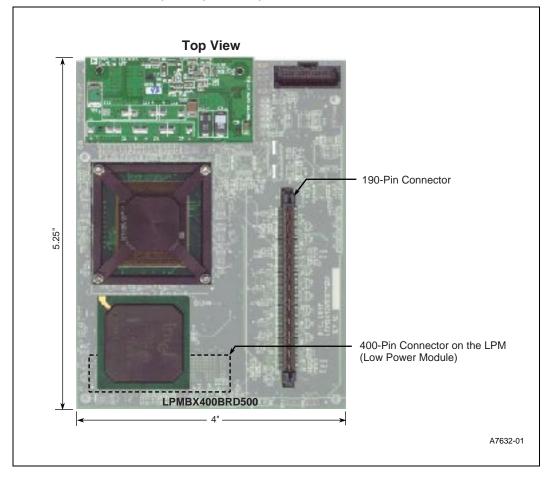
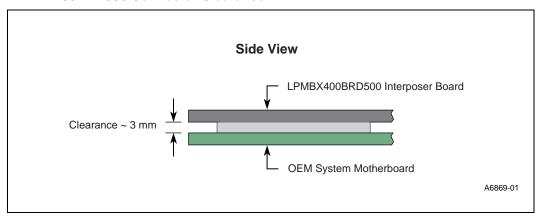


Figure 3. LPMBX400BRD500 Connector Clearance

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The clearance between the LPMBX400BRD500 Interposer Board and the OEM system board is approximately 3 mm as shown in Figure 3. If additional clearance is required, a socket saver can be used adding approximately 8 mm of additional clearance. Contact your Intel Field Sales Representative or a tools vendor to request a socket saver.



2.0 Getting Started

The LPMBX400BRD500 Interposer Board requires a VRM which is mounted on the LPMBX400BRD500.

2.1 Unpacking Instructions

Carefully unpack the contents of the box and verify that all of the items in the packing list are present. If items are missing or damaged, contact Intel or your authorized distributor.

2.1.1 Important Static Electricity Precautions

Take appropriate measures to prevent static electricity damage when removing the Interposer Board from the antistatic bag. This board should only be handled in a static free area.

- Before handling any components or touching any other system units, discharge your body's static electric charge by touching a grounded surface.
- Wear a grounded wrist strap if one is available.
- Remove the board from the antistatic bag only when you are ready to install it.
- Do not lay the board or other components on the bag, only the insides are antistatic.
- When handling the board or other components, hold them by their edges or metal mounting brackets.
- Never slide the board or other components over any surface.

2.2 Installation

Pay careful attention when installing the 400-pin high density connectors. Successful module insertion and extraction consists of three major elements:

- 1. Alignment Rough alignment is required before applying forces to reduce the possibility of contact damage. Fine alignment is provided by the connector housing. Rough alignment is achieved by visually aligning the connector housing and mounting holes.
- 2. **Insertion -** Insertion forces must be applied only on the board surface. Do not apply force to any component. Best results and lower insertion forces are achieved when using a 2-step rolling or "zippering" process. Align the connector length wise from one end of the connector, roll the connector on until the board/module/mini-cartridge is parallel, and then apply force straight down to secure the connector.
- 3. **Extraction** Extraction forces must be applied while securely controlling the board. Rolling out the connector opposite of the insertion process is recommended. Twisting the board or excessively tilting it while removing can result in connector damage.

2.2.1 LPMBX400BRD500

The LPMBX400BRD500 Interposer Board, with the VRM securely mounted on top of the it, replaces the Pentium III mobile module in the system. First, remove the mobile module and its associated mounting hardware, then carefully install the LPMBX400BRD500 Interposer Board on the 400-pin connector.



2.2.2 Cooling Fan

The cooling fan is shipped with the LPMBX400BRD500 kit. To install the fan, peal the plastic film off the base of the fan and place the exposed adhesive section on the center of the Thermal Plate, which is covering the processor (see Figure 4).

Warning: The cooling fan runs on 5 V ONLY! It requires a 5 V power source on the OEM system board.

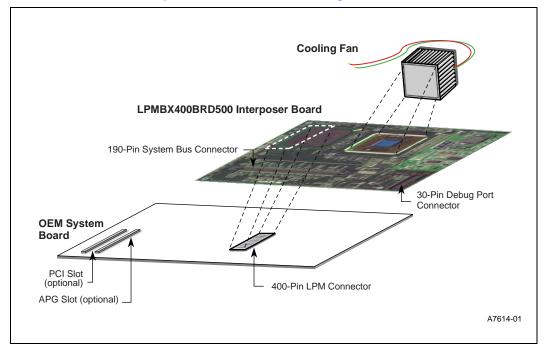
2.2.3 Emulator/Logic Analyzer

Connect the 30-pin cable from the emulator or logic analyzer to the debug port connector on the LPMBX400BRD500 Interposer Board. If you have a debug port designed into your system, only the debug port on the LPMBX400BRD500 Interposer Board will function. The port on the system board will not function with the LPMBX400BRD500 in place.

Warning: Only a 1.5 V emulator 30-pin probe tip can be used with LPMBX400BRD500 debug port. Use of wrong probe tip (2.5 V) might cause permanent damage to the processor. Contact your third-party tools vendors for correct 30-pin probe tip.

Connect the probe from the Mobile Pentium III processor logic analyzer to the 190-pin connector. Contact your logic analyzer vendor for specific details. A list of some third-party vendors is available in Table 2 on page 2.







3.0 Hardware Reference

For a hardware layout of the LPMBX400BRD500 Interposer Board, refer to Figure 5 on page 11. For board dimensions and keepout space requirements, refer to Figure 2 on page 4 and Figure 3 on page 5.

3.1 Connector Definitions

Changes to the hardware are not required for the LPMBX400BRD500 Interposer Board. If necessary, you can refer to the Intel[®] Pentium[®] III Processor in BGA2 and Micro-PGA2 Packages at 400 MHz, 450MHz and 500 MHz Datasheet (order number 245032), Intel[®] Pentium[®] III Processor Mobile Module Connector 2 (MMC-2) Datasheet (order number 245034) for connector definitions.

3.2 Jumper Settings

Changes to the jumper settings are not required for normal operation of the LPMBX400BRD500 Interposer Board.

3.2.1 Voltage Regulator Settings

The voltage setting for the V_{CC} core is determined by the VID pins, which are signal outputs of the Mobile Pentium III processor. Jumper settings are available to vary the V_{CC} core voltage, however, these should only be used for validation/debug purposes. For reference purposes, the jumper settings for the voltage regulator are provided in Table 3.

Warning: The jumpers are preset to default settings at the manufacturing site. The setting for the V_{CC} core voltage is for 1.6 V. Exceeding the default voltage is NOT recommended, unless specified otherwise in the Intel[®] Pentium[®] III Processor in BGA2 and Micro-PGA2 Packages at 400 MHz, 450MHz and 500 MHz Datasheet. Prolonged usage at a higher voltage may have adverse effects on the Intel[®] Pentium[®] III processor's operation.

Table 3.Voltage Regulator Jumper Settings (Sheet 1 of 2)

| JP10 | JP11 | JP12 | JP13 | JP14 | +VCC_CPU |
|-----------------|------|------|------|------------------|----------|
| NS ¹ | NS | NS | NS | NS | NO CPU |
| NS | NS | NS | NS | 1-2 ² | 0.925 V |
| NS | NS | NS | 1-2 | NS | 0.950 V |
| NS | NS | NS | 1-2 | 1-2 | 0.975 V |
| NS | NS | 1-2 | NS | NS | 1.000 V |
| NS | NS | 1-2 | NS | 1-2 | 1.025 V |
| NS | NS | 1-2 | 1-2 | NS | 1.050 V |
| NS | NS | 1-2 | 1-2 | 1-2 | 1.075 V |
| NS | 1-2 | NS | NS | NS | 1.100 V |
| NS | 1-2 | NS | NS | 1-2 | 1.125 V |
| NS | 1-2 | NS | 1-2 | NS | 1.150 V |

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| JP10 | JP11 | JP12 | JP13 | JP14 | +VCC_CPU |
|------------|-----------|------------|------------|------------|---------------------------|
| NS | 1-2 | NS | 1-2 | 1-2 | 1.175 V |
| NS | 1-2 | 1-2 | NS | NS | 1.200 V |
| NS | 1-2 | 1-2 | NS | 1-2 | 1.225 V |
| NS | 1-2 | 1-2 | 1-2 | NS | 1.250 V |
| NS | 1-2 | 1-2 | 1-2 | 1-2 | 1.275 V |
| 1-2 | NS | NS | NS | NS | NO CPL |
| 1-2 | NS | NS | NS | 1-2 | 1.30 V |
| 1-2 | NS | NS | 1-2 | NS | 1.35 V |
| 1-2 | NS | NS | 1-2 | 1-2 | 1.40 V |
| 1-2 | NS | 1-2 | NS | NS | 1.45 V |
| 1-2 | NS | 1-2 | NS | 1-2 | 1.50 V |
| 1-2 | NS | 1-2 | 1-2 | NS | 1.55 V |
| <u>1-2</u> | <u>NS</u> | <u>1-2</u> | <u>1-2</u> | <u>1-2</u> | <u>1.60 V³</u> |
| 1-2 | 1-2 | NS | NS | NS | 1.65 V |
| 1-2 | 1-2 | NS | NS | 1-2 | 1.70 V |
| 1-2 | 1-2 | NS | 1-2 | NS | 1.75 V |
| 1-2 | 1-2 | NS | 1-2 | 1-2 | 1.80 V |
| 1-2 | 1-2 | 1-2 | NS | NS | 1.85 V |
| 1-2 | 1-2 | 1-2 | NS | 1-2 | 1.90 V |
| 1-2 | 1-2 | 1-2 | 1-2 | NS | 1.95 V |
| 1-2 | 1-2 | 1-2 | 1-2 | 1-2 | 2.00 V |

Table 3. Voltage Regulator Jumper Settings (Sheet 2 of 2)

1. 2. 3.

NS = No Shunt. 1-2 = Populate Jumper. Default voltage setting.



3.3 Test Points

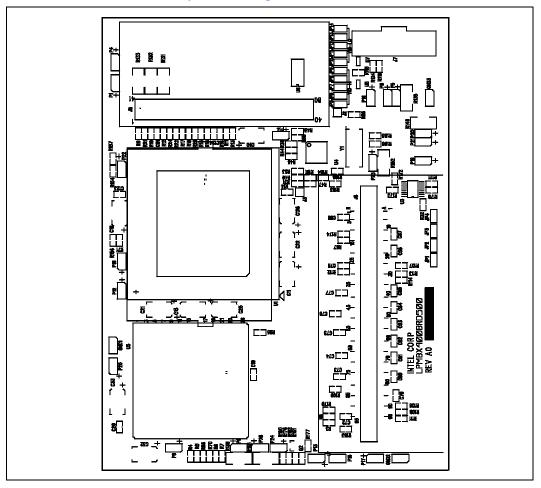
Power measurement header descriptions are provided in Table 4.

Table 4.Power Measurement Header Descriptions

| Header | Voltage Rail | Resistor | Effective Resistance (Ω) | Description |
|--------|-------------------------------|---|--------------------------------|--|
| P1 | +VCC_CORE (1.6V) | R131, 0.01Ω R132, 0.01Ω R133, 0.01Ω | 0.003 | Processor core voltage. |
| P4 | +VCCT_IO (1.5V) | R134 | 0.01 | Processor GTL+ termination voltage rail. |
| P6 | +V3_BX (3.3V) | R136 | 0.01 | 3.3 V rail for BX core. |
| P8 | +VCCT_GTL_PU | R137 | 0.01 | Low Power GTL +voltage rail for all GTL termination resistors and 443BX GTL reference. |
| P9 | +V3_PU (3.3V) | R138 | 0.05 | 3.3 V rail for pull-ups. |
| P15 | +VGTLREF_CPU (2/3 VCCT_IO) | R144 | 0.05 | Processor GTL+ reference voltage. |
| P17 | +VIN_VRM | R146 | 0.01 | Primary DC system power supply [5 V] from system electronics board. |



Figure 5. LPMBX400BRD500 Board Layout Drawing



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