ITP700 Debug Port

Design Guide

February 2004

Document Number: 249679-014

Contents

Figures

Tables

Revision History

Revision	Description	Revision Date
Rev 1.0	Initial Release with Intel® Xeon™ Processor	May 2001
Rev 1.03	Correction of +/- TCLK	May 2001
Rev 1.10	Addition of Chapter 5: Intel® Pentium® 4 Processor in the 478 Pin Package System Implementation Guidelines Addition of termination information for BPM[5:0]# and Reset# signals	August 2001
Rev 1.15	Append to Chapter 5: Intel® Pentium® 4 Processor in the 478 Pin Package / Intel® Pentium® 4 Processor with 512KB L2 Cache on 0.13 micron process System Implementation Guidelines Addition of ITP700 Flex debug port information Addition of Appendix E: Designer's Checklist for Schematic and Layout Reviews	January 2002
Rev 1.20	Addition of Chapter 6: Intel® Xeon™ Processor with 512-KB L2 Cache at 2.20, 2.0, and 1.80 GHz –DP Server System Implementation Guidelines Updated ITP700 Keep-Out Volume Diagram	January 2002
Rev 1.21	Additional explanation of ITP700 Keep-Out Volume changes	February 2002
Rev 1.22	Addition to Chapter 5 to include Mobile Intel® Pentium® 4 Processor-M System Implementation Guidelines	June 2002
Rev 1.30	Chapter 7 added for Intel® Itanium® 2 Processor	July 2002
Rev 1.40	Chapter 8 added for Intel® E8870 Chipset	August 2002
Rev 1.50	Addition of Intel® Xeon™ Processor MP Server System Implementation Guidelines Merge of Chapter 6 with Chapter 4	November 2002
Rev 1.60	Addition to Chapter 7 to include Intel® Centrino™ mobile technology support	March 2003
Rev 1.65	Append to Chapter 7 to include Intel® Pentium® 4 processor on 90 nm process System Implementation Guidelines	January 2004

Definitions

Term	Definition
DPA	Debug Port Adapter. Section of ITP hardware that plugs into the target system Debug Port.
ITP	The acronym “ITP” as used within this document refers to an In-Target Probe run-time control tool as produced by Intel as well as third party vendors. This specification is not meant to imply that any vendor’s debug tool is preferred over any other.
ITP700 Flex	Flex cable adapter to the ITP that connects to a small form factor connector on the target platform, drastically reducing the footprint and vertical clearance from the standard ITP700 style debug port. This debug port style currently supports UP configurations only.
JTAG	Joint Test Access Group
Local TAP Master	A device other than the ITP that is designed to control accesses into an IEEE STD 1149 style scan chain and all TAP agents contained within that scan chain. Usually this device is used for manufacturing test purposes.
LVDPA	Low-Voltage Debug Port Adapter. Section of ITP hardware that plugs into the target system Debug Port that supports operating voltages as low as 0.6V.
TAP	IEEE STD 1149 defined test access port
TAP Master	A device that is designed to control accesses into an IEEE STD 1149 style scan chain and all TAP agents contained within that scan chain. The ITP is an example of a TAP master.
VTERM	Termination voltage of the BPM[5:0]# and RESET# signals.
VTAP	Pull-up voltage for the ITP scan chain signals

How to Use This Document

This document has two primary roles in the design process. First and foremost, this document is a location for recording all of the best-known methods relating to the design of an ITP700 based scan chain in a target. Second, this document serves as the Intel Corporation communication of Design Guide and In Target Probe (ITP) signal specifications for a given processor. The document is structured to serve both purposes.

Chapters 1 and 2 describe the debug port implementation guidelines for a generic uniprocessor (UP) and generic multiprocessor (MP) system, respectively.

Chapter 3, 4, and 5 contain the Electrical and Mechanical Specifications for the ITP700 DPA, ITP700 LVDPA, and ITP700 Flex respectively. These chapters include the specifications of the different types of ITP hardware IO under all drive levels as well as specifications under non-standard current loads and pull-up voltages. This information can be helpful if designers would like to know more about the characteristics of the ITP under non-standard operating conditions, or would like to interpolate the effects of changing recommended implementations to meet other design requirements. This Keepout-Volume (KOV) information in the Mechanical Requirements section is also useful when designing a debug port onto a platform.

Chapters 6 and beyond describe implementation information specific to particular Intel Corporation processor families. This information includes expected input and output voltage characteristics of the ITP (when terminated in the method recommended by this Design Guide) as well as processor-specific implementation details that are not consistent with the ‘generic’ implementation guidelines in Chapter 1 through Chapter 5. These chapters make reference to the ‘generic’ UP and MP routing guidelines found in Chapters 1 and 2.

The Appendices go into detail on certain advanced design topics that are not relevant to the other sections of this document. Appendices also include Spice Models for the ITP and a Designer’s Checklist for a schematic and layout review.

System designers should first familiarize themselves with the general implementation, routing, and termination rules as defined in the UP or MP implementation guidelines chapters of this document as applicable to their design. They should then review the specific chapter for the processor that the system is being designed for. Note that some of the generic implementations may not be applicable based on the content of the processor specific chapter. Any non-standard design topics are described in the appendices of this document.

This page is intentionally left blank.

1 Uniprocessor ITP Debug Port Implementation Guidelines

The signals involved in the ITP debug system are high-speed signals and must be routed with high-speed design considerations in mind. The implementation offers some flexibility in areas such as scan chain routing, addition of non-ITP TAP master to the local scan chain, and clock rate of the scan chain. However, the implementation is not flexible in system bus BPM[5:0]# , RESET#, or BCLK(p/n) connections.

Simulation models of the ITP700 DPA interface hardware is available. Intel highly recommends that customers include this model in platform simulations. These models can be found in Appendix E of this document.

1.1 General Description

The debug port (DP) is the command and control interface for the In-Target Probe (ITP) debug tool. The ITP is a specialized JTAG Test Access Port (TAP) master that interfaces into processors and chipset TAP agents through a carefully routed private scan chain on the target system.

The primary operations of the ITP and associated debug port are to provide system, execution, and TAP interfaces to the target system. The system interface informs the debug tool if power, clock, and access state are available in the target system. The execution interface is used to coordinate debug activities with the current execution state of the agents attached to the debug port. The TAP interface allows for query and editing of registers and state within the agents attached to the scan chain.

The debug port and JTAG signal chain must be designed into a system board to utilize the ITP for debug purposes. There are several mechanical, electrical and functional constraints on the debug port and associated scan chain that must be followed. The mechanical constraints require a debug port connector to be installed in the system with adequate physical clearance for the ITP hardware while the system is running. The electrical constraints require that the debug port operate using the TAP signals at high speed, and that the ITP be connected to the processor system bus break point and reset signals for recovery at full speed through a dedicated BCLK connection. The functional constraint requires the debug port to be able to share the scan chain with any local TAP systems via a handshake and multiplexing scheme.

1.1.1 ITP Features

- Operation at up to 16 MHz.
- Ability to drive up to one EXECUTION signal (BPM5DR#).
- Ability to monitor up to six EXECUTION signals (BPM[5-0]#).
- Accepts a differential system BCLK input.
- Synchronous TAP operations.

- Hot-plug support for the debug port adapter (DPA) into a target system.
- Supports arbitration with a local TAP Master (e.g. manufacturing test chain) through a simple handshake.

1.2 Recommended Signal Terminations

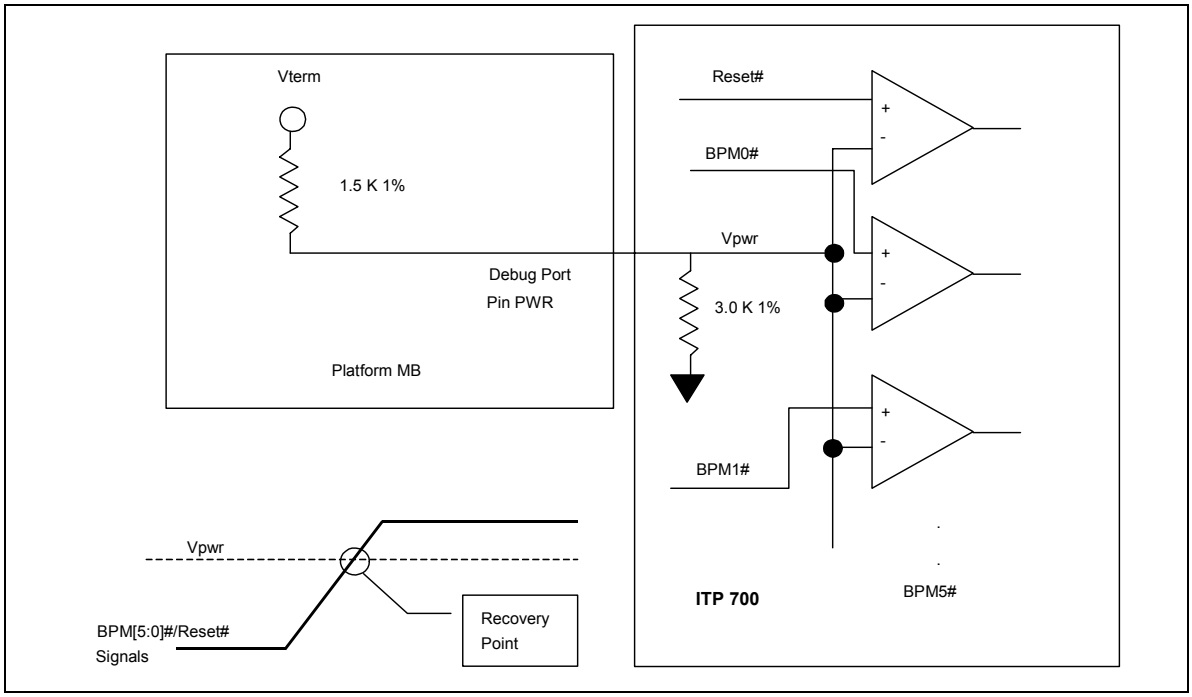
Table 1. Recommended Debug Port Signal Terminations

Signal	Termination Value	Termination Voltage	Termination Location	Notes
PWR	1.5 kΩ 1%	VTERM of BPM[5:0]# and RESET#	Within 1 ns of debug port	1
BCLK(p/n)				2
DBA#	150 – 240 Ω 5%	VCC of target system recovery circuit.	Within 1 ns of debug port	3
DBR#	150 – 240 Ωs 5%	VCC of target system recovery circuit	Within 1 ns of debug port	
FBI	220 Ω 5%	GND	Within 200 ps of the receiver	4
FBO	Connect to TCK pin at the closest BPM[5:0]# bus load device	NA	NA	
TCK	27 Ω 1%	GND	Within 200 ps of the debug port	
TMS	39 Ω 1 %	VTAP	Within 200 ps of the debug port	
TDI	150 Ω 5%	VTAP	Within 300 ps of the receiver	5
TDO	75 Ω 5%	VTAP	Within 300 ps of the debug port	5
TRST#	500 – 680 Ω 5%	GND		
BPM[5:0]#	Characteristic impedance of the transmission line 5%	VTERM		2
RESET#	Characteristic impedance of the transmission line 5%	VTERM		2
BPM5DR#	Connect to BPM[5]# at the debug port	NA	NA	

NOTES:

1. The target system resistor connected between VTERM and the PWR pin is part of a voltage division circuit (see below). The voltage derived from the voltage divider is used as a reference for recovery of the BPM[5:0]# and RESET# signals on the ITP. The recovery point of the BPM[5:0]# and RESET# signals can be modified by scaling the target system resistor. The standard 1.5 K 1% target system resistor will result in a recovery point of 2/3rds of VTERM.
2. Resistance, voltage, and termination location are defined in the Platform Design Guide documentation.
3. Only required if DBA# is used with any target system circuitry. This signal may be left unconnected if unused.
4. Only required if FBI is used to source a buffer for JTAG TCK. This signal may be left unconnected if unused.
5. A termination resistor must be located at the receiver of each scan chain agent

Figure 1. PWR Routing and Usage



NOTE: By varying the platform 1.5-K resistor, the recovery point could be increased or decreased.

1.3 ITP Signal Layout Guidelines

This section contains the layout guidelines for the debug port signals. Please refer to the specification chapter for the debug port electrical and mechanical specifications. Routing to the debug port of Signals BPM[5:0]# and RESET# must be shorter than 1.0 ns of electrical length from the nearest system bus agent. Note that the <1.0 ns requirement applies only to the BPM[5:0]# and RESET# trace segments between the debug port and the nearest system bus agent. All other system bus trace segments must be routed according to the guidelines located in the Platform Design Guides.

There are three signal groups within the debug port. Each group has a different set of layout requirements:

- System - The system signal group indicates the access state of the entire system
- JTAG - The JTAG signal group consists of the five standard JTAG pins. The JTAG signals are to be designed to run up to 16 MHz.
- Execution - The execution signal group contains the reset and run control signals used to indicate operational conditions.

The following three subsections clarify the routing guidelines for each of these signal classes. VTERM is the termination voltage of the system bus BPM[5:0]# and RESET# signals as defined by the processor data sheet. VTAP refers to the pull-up voltage of the JTAG signals on the system board. This pull-up voltage is chosen by the system designers to be consistent with the JTAG IO buffer specs for the processor and the ITP. Information on input voltage specifications, drive strength, and recommended termination values for the processor can be obtained from processor

datasheets. VTAP should be used for the pull-up resistors on all JTAG signals in the scan chain that operates directly from the ITP. If a bus translator is used to translate an ITP scan chain to a higher voltage, VTAP on the opposite side of the translator from the ITP shall change as well.

Note: All termination locations indicated are referenced to the target system.

1.3.1 System Signal Layout Guidelines

Table 2. System Signal Layout Guidelines

Debug Port Signal	Layout Guideline
PWR	If PWR is used to arbitrate with a local TAP master for control of the scan chain: Pull-up resistor to VTERM and an open drain control gate must be located less than 1 ns from the debug port. If PWR is not used to arbitrate with a local TAP master for control of the Scan chain: Pull-up resistor to VTERM must be located less than 1 ns from the debug port.
BCLK(p/n) 1	BCLK for the debug port should originate as a unique output of the system clock tree. The BCLK routed from the clock distribution component to the debug port must have a propagation delay equal to the length of the BCLK traces from the clock distribution component to the other front side bus agents plus the electrical length of the BPM[5:0]# and RESET# signals as measured from the processor to the debug port. This will ensure that these critical signals have the same phase relationship at the debug port as is seen at the processor. BCLK is a differential high speed clock supplied by the target system. It is a critical system signal requiring careful timing and signal integrity considerations.
FBO	FBO is used to monitor the phase relationship of TCK to BCLK and to recover TDO. It is important that the phase of FBO to BCLK at the debug port is the same as the phase of TCK to BCLK at the processor. To meet this requirement, the electrical length fixed by BPM[5:0]# and RESET# (between the processor and the debug port) must also be the electrical length of FBO(TCK) from the processor back to the debug port. See the Execution Signal Layout Guidelines in this chapter for additional information.
FBI	FBI is a fast edge copy of TCK that can optionally be used as the source of scan chain TCK when TCK buffers are implemented on a system board. FBI should be loaded with no greater than 40 pF and have a DC load of no less than 200 Ω to GND. If used, this is a critical clock for the scan chain and must be analyzed for signal quality and timing with respect to the specifications of the intended receiver of the FBI signal.
DBR#	This is a non-critical route.
DBA#	This is a non-critical route.

NOTE: : Refer to BCLK system requirements for proper termination requirements and routing rules

DBA# and DBR# are output signals from the ITP. The ITP provides an open drain FET closure to GND as the drive of DBA# and DBR#. The target system should provide the pull-up for both of these signals. The pull-up can be to any voltage up to five volts that is consistent with the input specifications of the component used to receive these signals on the target system. DBR# is the ITP debug port reset signal that should always be routed to the system reset controller. DBA# is the ITP debug port scan active signal used to indicate that the ITP is currently driving the scan chain. DBA# is an optional signal of the debug port.

1.3.2 JTAG Signal Layout Guidelines

Table 3. JTAG Signal Layout Guidelines

Debug Port Signal	Layout Guideline
TCK	This is a critical JTAG clock signal, sourced by the debug port, which requires thorough timing and signal integrity analysis/simulation. The termination resistor to GND on TCK must be located within 200 ps of the debug port in order to minimize IR losses that would degrade signal voltage levels at the loads. The length of TCK should not exceed 2 ns in electrical length. Note that TCK returns a feedback copy of TCK to FBO at the debug port. The length of the trace between the processor TCK pin and the debug port must be equal to the electrical length of BPM[5:0] and RESET# from the processor to the debug port. Load capacitance at the processor must be no more than 35 pF. It is strongly recommended that this signal be simulated for signal integrity purposes. Non-monotonicity on the rising or falling edge of TCK will render the ITP inoperative. See the Execution Signal Layout Guidelines section of this chapter for additional information.
TMS	Critical JTAG mode select signal, sourced by the debug port, which requires moderate timing and signal integrity analysis / simulation. The termination resistor to VTAP on TMS should be located within 200 ps of the debug port in order to minimize resistive losses that would degrade signal voltage levels at the loads. TMS is driven on the falling edge of TCK at the ITP and recovered on the following rising edge of TCK at the processor.
TDI, TDO	JTAG scan data signals. These signals require minor timing and signal integrity analysis / simulation. The terminations should be located within 300 ps to each load. TDI is driven on the falling edge of TCK at the ITP and recovered on the following rising edge of TCK at the processor.
TRST#	Non-critical JTAG reset signal routed to all scan chain devices. TRST# requires a pull-down resistor to ensure the signal is held in the asserted (low) state if the debug port is not driving the signals. Layout of this signal needs to be such that noise will not be coupled to the signal and cause a false reset of the scan chain.

For a uniprocessor scan-chain that does not include a other scan chain components: The TDI pin of the ITP is connected to the TDI pin of the processor with the pull-up located within 200 ps of the processor. The TDO pin of the processor is routed back to the TDO pin of the debug port with the pull-up located within 200 ps of the debug port.

1.3.3 Execution Signal Layout Guidelines

Table 4. Execution Signal Layout Guidelines

Debug Port Signal	Layout Guideline
BPM[5:0]#	These signals are extremely routing critical. The debug port recovers these signals relative to BCLK at the debug port pins. Therefore, the signals must be routed with closely matched electrical lengths (within ±50 ps) and no greater than 1.0 ns from the processor to the debug port.
BPM5DR#	The debug port BPM5DR# output pin should be connected on the board to the BPM5# pin of the debug port. This allows the ITP or run-control tool to drive BPM5# at reset. It also allows ITP to assert BPM5# if ITP needs to assert a trigger signal that can be seen directly by the target system. Note that ITP asserts / de-asserts this signal asynchronous to the bus BCLK.

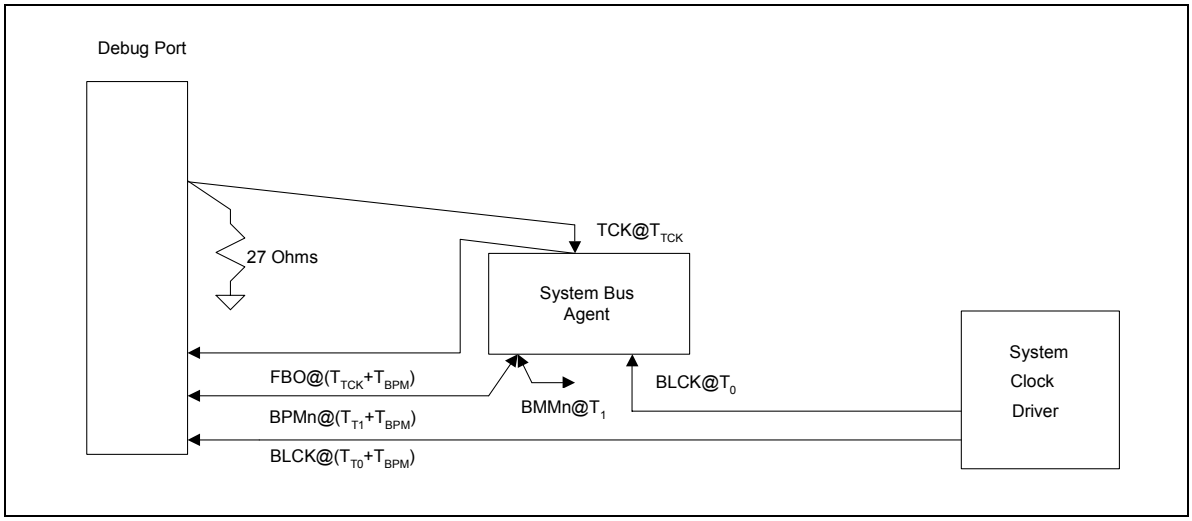
The debug port should be placed as close as is physically reasonable to the processor and no further than 1.0 ns flight time (as measured by trace length of the BPM[5:0]# signals) from the processor. System designers should record the flight time of the BPM[5:0]# signals from the processor to the debug port. This value will be important during the routing of several other debug port signals. Ideally BPM[5]# will be routed from the processor to the debug port BPM[5]# pin matched with the other BPM# signals. From pin 13 the trace will route directly to the debug port BPM5DR# pin and continue to the termination of the transmission line.

Assuming BCLK(p/n) signals are routed from the system clock buffer to each of the synchronous clock agents with a matched length, the copy of BCLK(p/n) from the system clock buffer to the ITP debug port must have a flight time equal to the matched length of the other synchronous clock agents plus the flight time of the BPM[5:0]# signals from the processor to the debug port noted above. This will ensure that the same BCLK to BPM[5:0]# phase relationship seen at the processor will be present at the debug port pins. BCLK trace lengths may be adjusted to center the recovery of BPM[5:0]# and RESET# at the debug port within the ITP receiver setup and hold window.

Multiple layer transitions of the BCLK, BPM, and TCK signals will compromise signal integrity. An effort should be made to minimize the number of layer transitions for these signals. Try to keep the BCLK, BPM, and TCK signals referenced to GND whenever possible. If layer transitions are required, stitching vias should be included near ever every layer transition of the BCLK, BPM, and TCK signals, even when not referencing the same voltage. This is recommended to reduce the lengths of return current loops. Adding an AC bypass capacitor near every layer transition or plane split between the two referenced planes will also help to minimize AC return current loops. An effort should be made to not share ITP AC bypass capacitors with other high-speed signals.

TCK and TMS must be routed with pull-up / pull-downs located at the driver. FBO is routed such that it is connected to the TCK at the processor, and routed back to the debug port with an electrical length equal to the flight time of the BPM[5:0]# and RESET# signals from the processor to the debug port. This is done to guarantee that the BCLK to TCK phase relationship at the processor will be seen at the debug port FBO and BCLK(p/n) pins. The diagram below illustrates these routing relationships.

Figure 2. Recommended Layout Topology



NOTES:
1. All of the above routes must be simulated to ensure signal integrity. Failure to do so may result in non functional ITP.
2. All combination timings in the above drawing are ±50 ps in routing length maximum.

The figure above defines propagation delays of various ITP signals from the driver to the receiver. The following are definitions of individual trace segments that are included in the figure.

- $\mathbf{T_{TCK}}$ – Propagation delay of the TCK trace from the debug port to the system bus agent TCK pin
- $\mathbf{T_{BPM}}$ – Propagation delay of the BPM traces from the debug port to the nearest system bus agent.
- $\mathbf{T_0}$ – Propagation delay of BCLK from the system clock driver to the processors and chipset components
- $\mathbf{T_1}$ – Propagation delay of the BPM traces from the driving system bus agent to the system bus agent closest to the debug port.

1.4 ITP700 Flex Alternative Debug Port

There is a smaller version of the debug port available as an alternative that can be designed into uniprocessor platforms. The ITP700 Flex is a single piece of flexible circuitry with a right-angled standard male debug port connector on one end and the other end is plugged into a small footprint surface mount connector that is soldered to the platform.

The following are the requirements that platforms must meet in order to be able to use the ITP700 Flex debug port.

- The target system cannot require the use of an external buffer for TCK
- BPM[5:0]# pins are not terminated correctly when the ITP700 Flex is not installed. The platform must either not use BPM[5:0]# signals when ITP700 Flex is not plugged in or it must be able to terminate BPM# [5:0]when ITP700 Flex is removed.

The advantages of this ITP700 Flex are a significantly reduced footprint and keepout volume. Please refer to the ITP700Flex specifications chapter for the mechanical specifications.

1.4.1 Signal Descriptions

The pinout of the debug port connector at the end of the ITP700 Flex is identical to that of the standard debug port connector. See Figure 4 for details.

The pinout of the target system surface mount connector for ITP700 Flex is below.

Table 5. ITP700 Flex Edge Connector Pinout

Pad #	Signal Name	Pad #	Signal Name
1	TDI	2	TMS
3	TRST#	4	NC1
5	TCK	6	NC2
7	TDO	8	BCLKn
9	BCLKp	10	GND
11	FBO	12	RESET#
13	BPM5#	14	GND
15	BPM4#	16	GND
17	BPM3#	18	GND
19	BPM2#	20	GND
21	BPM1#	22	GND
23	BPM0#	24	DBA#
25	DBR#	26	VTAP
27	VTT	28	VTT

1.4.2 Termination and Routing Guidelines

Table 6. Recommended Debug Port Signal Terminations

Signal	Termination Value	Termination Voltage	Termination Location	Notes
BCLK(p/n)				1
DBA#	150 – 240 Ω 5%	VCC of target system recovery circuit.	Within 1 ns of debug port	2
DBR#	150 – 240 Ω 5%	VCC of target system recovery circuit	Within 1 ns of debug port	
FBO	Connect to TCK pin at the closest BPM[5:0]# bus load device	NA	NA	
TCK	27 Ω 1%	GND	Within 200 ps of the debug port	
TMS	39 Ω 1 %	VTAP	Within 200 ps of the debug port	
TDI	150 Ω 5%	VTAP	Within 300 ps of the receiver	3
TDO	75 Ω 5%	VTAP	Within 300 ps of the debug port	3
TRST#	500 – 680 Ω 5%	GND		
BPM[5:0]#	Characteristic impedance of transmission line	VTERM		6
RESET#				1, 5
Vtt	N/A			4
All Other Signals	N/A	N/A	N/A	

NOTES:

1. Resistance, voltage, and termination location are defined in the Platform Design Guide documentation. Appendix D is not valid for ITP700 Flex.
2. Only required if DBA# is used with any target system circuitry. This signal may be left unconnected if unused
3. A termination resistor must be located at the receiver of each scan chain agent.
4. Mount debug port directly over the Vtt plane. Connect plane with vias and short, wide traces to Vtt (pins 27 and 28). If a plane is not available, add a 0.1 µF ceramic cap between Vtt and GND within 0.1 inches of the Vtt pins of the debug port.
5. See Figure 3. ITP700 Flex Required Layout of Reset
6. See Figure 4. ITP700 Flex Required Layout of BPM[5:0]#

The most radical difference between the standard ITP700 and ITP700 Flex implementation guidelines is the termination requirements for the BPM[5:0]# signals. For ITP700 Flex the terminations on the debug port end of the transmission line are built into the ITP700 Flex device. Note that this means that there is no termination on BPM[5:0]# if the ITP700 Flex is not installed. If the platform designers require these signals to be terminated when ITP700 Flex is not installed it

is possible to terminate these signals using resistances equal to the characteristic impedance of the motherboard using short (100 ps or less) stubs after the trace meets the ITP700 Flex surface mount connector on the motherboard.

BPM[5:0]# lengths must still be matched on the motherboard to within 50 ps of one another and with RESET# length D1 (see Figure 4 and Figure 5). Note that BPM5DR# is completely removed form the ITP700 Flex design. Its functionality is integrated on the ITP700 Flex hardware. Systems using the ITP700 Flex must only contain one load on the BPM[5:0]# signals and thus there can be no BPM[5:0]# connections on the chipset.

Note: Note that BPM0# and BPM2# as well as BPM1# and BPM3# are no longer tied together at the processor or the debug port. Instead they are routed directly through (eg BPM[5:0]# on the closest agent routed directly to its corresponding pin BPM[5:0]# on the debug port or ITP700 Flex).

Since the BPM[5:0] Signals are terminated on the ITP700 Flex extension, the system bus termination voltage (Vtt) must be connected to the debug port. Preferably the ITP700 Flex will be located over the Vtt plane and pins 27 and 28 will be connected using short, wide traces to vias connected to the Vtt plane. The maximum expected current on these two pins together is 1.5 mA. If a plane is not available directly beneath the debug port connector, add a 0.1 µF ceramic cap between Vtt and Ground within 0.1 inches of the Vtt pins of the debug port.

RESET# signal is a system bus signal and used in many places. The routing of the RESET# signal will be defined by the Platform Design Guide. The following figure illustrates the layout of the RESET# signal at the debug port. The information within the dotted box is a simplified representation of the Platform Design Guide layout. This document will only define the parameters D1, D2, D3, D4 and Ri at the debug port end of the RESET# line. Note that as the debug port will be at one end of the transmission line, it will have a termination resistance of the same value as that defined by the Platform Design Guide. Lengths D2, D3, and D4 should be as short as possible so as not to disturb the signal integrity of this system bus signal.

Figure 3. ITP700 Flex Required Layout of Reset

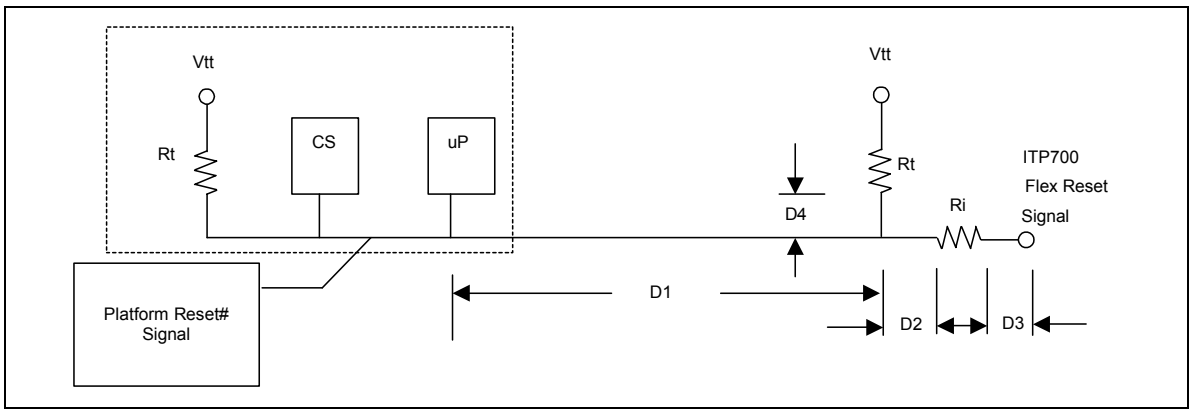


Table 7. Reset Definitions

Parameter	Min	Nominal	Max	Notes
D1			1 ns	1
D2, D3, D4			20 ps	
Ri		150 Ω 5%		

Figure 4. ITP700 Flex Required Layout of BPM[5:0]#

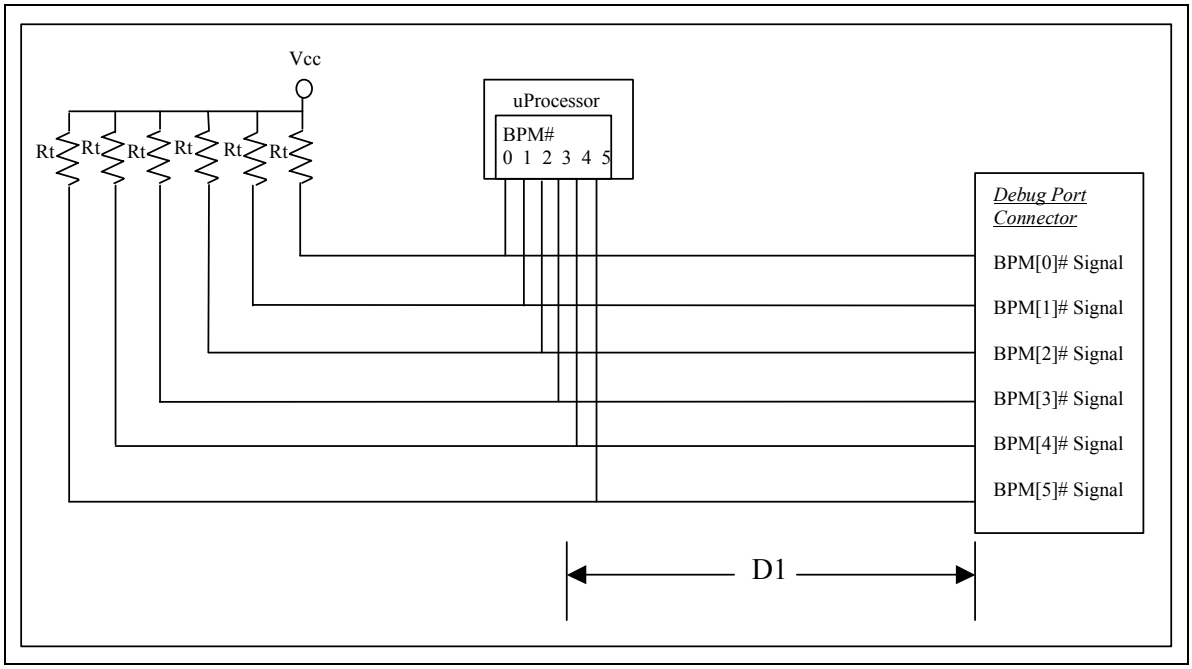


Table 8. BPM[5:0]# Definitions

Parameter	Min	Nominal	Max	Notes
D1			1 ns	1,2
Rt				3

NOTES:
1. This signal must be length matched to RESET# to within 50 ps.
2. D1 is defined as the total length from the processor driver to the corresponding BPM at the connector.
3. Characteristic Impedance of Transmission Line

Vtap should be connected to the same supply as provides the voltage of the JTAG pull-up resistors on the target system. This connection is lightly loaded (<50 mA). Check your platform, as this voltage may be the same as Vtt.

1.4.3 ITP700 Flex Deltas to Standard ITP AC/DC Characteristics

The following data represents the changes to the AC/DC specifications from the ITP700 DPA or the ITP700 LVDPA to be used with the ITP700 Flex. Note that this table only represents the changes to the base tables. Please reference the AC/DC Specifications for the ITP700 DPA or the ITP700 LVDPA in the Specifications chapters for debug port style of choice.

Table 9. ITP700 Flex Deltas from Standard ITP AC/DC Specifications

Signal	Specification	Standard ITP	ITP700 Flex
BCLK(p/n)	V_{PTP}	300 mV	320 mV
DBA#, DBR#	Resistance from pin to ground when active	6 Ω	10 Ω
TCK	$V_{OH\ MIN}$ [2]	1.25 V	1.20 V
TMS	$V_{OL\ MAX}$ [3]	0.30 V	0.32 V
BPM[5:0]#, RESET#	$V_{IH\ MIN}$	PWR+(0.15*VTERM)	PWR+(0.16*VTERM)
BPM[5:0]#, RESET#	$V_{IL\ MAX}$	PWR -(0.15*VTERM)	PWR -(0.16*VTERM)
BPM[5:0]#, RESET#	Min Setup	400 ps	430 ps
BPM[5:0]#, RESET#	Min Hold	200 ps	230 ps

NOTES:
1. At maximum current specified.
2. As measured into a 39 Ω 1% resistor terminated to 1.10 V.

2 Multiprocessor ITP Debug Port Implementation Guidelines

The ITP scan chain of multiprocessor systems with multiple chipset components requires that the debug port and associated scan chain be designed into the system board. An interposer debug port solution will not provide visibility to a multiple load scan chain because an interposer has no physical way to break the scan chain without losing access to the remainder of the processors and chipset. If the traces, termination, and connector footprint (without the header) for the debug port are designed into a system board, it is possible to enable use of a multiple load scan chain by simply populating the debug port header.

The signals involved in the ITP debug system are high-speed signals and must be routed with high speed design considerations in mind. The implementation offers some flexibility in areas such as scan chain routing, addition of non-ITP TAP master to the local scan chain, and clock rate of the scan chain. However, the implementation is not flexible in system bus BPM[5:0]# , RESET#, or BCLK(p/n) connections.

Simulation models of the ITP interface hardware are available. Intel highly recommends that customers include this model in platform simulations. These models can be found in Appendix E of this document.

2.1 General Description

The debug port (DP) is the command and control interface for the In-Target Probe (ITP) debug tool. The ITP is a specialized Test Access Port (TAP) master that interfaces into processors and chipset TAP agents through a carefully routed private scan chain on the target system.

The primary operations of the ITP and associated debug port are to provide system, execution, and TAP interfaces to the target system. The system interface informs the debug tool if power, clock, and access state are available in the target system. The execution interface is used to coordinate debug activities with the current execution state of the agents attached to the debug port. The TAP interface allows for query and editing of registers and state within the agents attached to the scan chain.

The debug port and JTAG signal chain must be designed into a system board to utilize the ITP for debug purposes. There are several mechanical, electrical and functional constraints on the debug port and associated scan chain that must be followed. The mechanical constraints require a debug port connector to be installed in the system with adequate physical clearance for the ITP hardware while the system is running. The electrical constraints require that the debug port operate using the TAP signals at high speed, and that the ITP be connected to the processor system bus debug signals for recovery at full speed through a dedicated BCLK connection. The functional constraint requires the debug port to be able to share the scan chain with any local TAP systems via a handshake and multiplexing scheme.

2.1.1 ITP Features

- Operation at up to 16 MHz.
- Ability to drive up to one EXECUTION signal (BPM5#).
- Ability to monitor up to six EXECUTION signals (BPM[5-0]#).
- Accepts a differential system BCLK.
- Synchronous TAP operations.
- Hot-plug support for the debug port adapter (DPA) into a target system.
- Supports arbitration with a local TAP Master (e.g., manufacturing test chain) through a simple handshake.

2.2 Recommended Signal Terminations

Table 10. Recommended Debug Port Signal Terminations

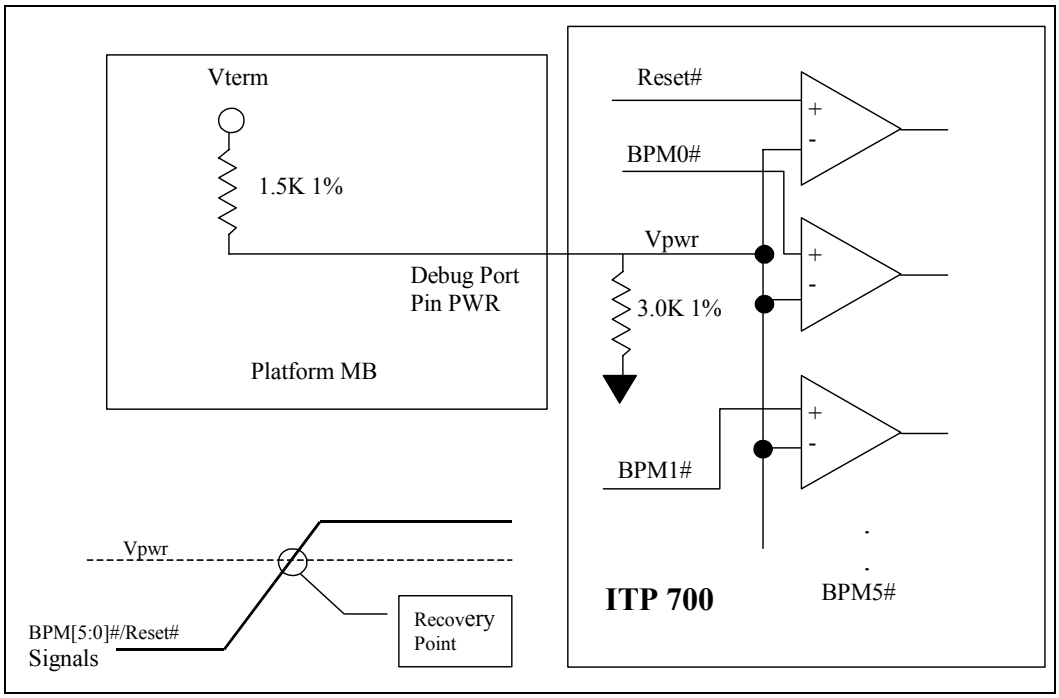
Signal	Termination Value	Termination Voltage	Termination Location	Notes
PWR	1.5 K 1%	VTERM of BPM[5:0]# and RESET#	Within 1 ns of debug port	1
BCLK(p/n)				
DBA#	150 – 240 Ω 5%	VCC of target system recovery circuit	Within 1 ns of debug port	2
DBR#	150 – 240 Ω 5%	VCC of target system recovery circuit	Within 1 ns of debug port	
FBI	220 Ω 5%	GND	Within 200 ps of the receiver	3
FBO	Connect to TCK pin at the closest BPM[5:0]# bus load device	NA	NA	
TCK	27 Ω 1%	GND	At branch of star topology and within 200 ps of the debug port	
TMS	39 Ω 1 %	VTAP	At branch of star topology and within 200 ps of the debug port	
TDI	150 Ω 5%	VTAP	Within 300 ps of the receiver	4
TDO	75 Ω 5%	VTAP	Within 300 ps of the debug port	4
TRST#	500 – 680 Ω 5%	GND		
BPM[5:0]#	Characteristic impedance of the transmission line	VTERM		
RESET#		VTERM		

Signal	Termination Value	Termination Voltage	Termination Location	Notes
BPM5DR#	Connect to BPM[5]# at the debug port	NA	NA	

NOTES:

1. The target system resistor connected between VTERM and the PWR pin is part of a voltage division circuit (see below). The voltage derived from the voltage divider is used as a reference for recovery of the BPM[5:0]# and RESET# signals on the ITP. The recovery point of the BPM[5:0]# and RESET# signals can be modified by scaling the target system resistor. The standard 1.5 K 1% target system resistor will result in a recovery point of 2/3rds of VTERM.
2. Only required if DBA# is used with any target system circuitry. This signal may be left unconnected if unused.
3. Only required if FBI is used to source a buffer for JTAG TCK. This signal may be left unconnected if unused.
4. A termination resistor must be located at the receiver of each scan chain agent

Figure 5. PWR Routing and Usage



NOTE: By varying the Platform 1.5- K resistor the recovery point could be raised or lowered.

2.3 ITP Signal Layout Guidelines

Routing to the debug port of signals BPM[5:0]# must be shorter than 1.0 ns of electrical length from the nearest system bus agent. Note that the <1.0 ns requirement applies only to the BPM[5:0]# trace segments between the debug port and the nearest system bus agent. All other system bus trace segments must be routed according to the guidelines located in the Platform Design Guides.

There are three signal groups within the debug port. Each group has a different set of layout requirements:

- System - The system signal group indicates the access state of the entire system
- JTAG - The JTAG signal group consists of the five standard JTAG pins. The JTAG signals are to be designed to run up to 16 MHz.
- Execution - The execution signal group contains the reset and run control signals used to indicate operational conditions.

The following three subsections clarify the routing guidelines for each of these signal classes. VTERM is the termination voltage of the system bus BPM[5:0]# and RESET# signals defined in the processor datasheet. VTAP refers to the pull-up voltage of the JTAG signals on the system board. This pull-up voltage is chosen by the system designers to be consistent with the JTAG IO buffer specs for the processor and the ITP. Information on input voltage specifications, drive strength, and recommended termination values for the processor can be obtained from processor datasheets. VTAP should be used for the pull-up resistors on all JTAG signals in the scan chain that operates directly from the ITP. If a bus translator is used to translate an ITP scan chain to a higher voltage, VTAP on the opposite side of the translator from the ITP shall change as well.

Note: Note that all termination locations indicated are referenced to the target system.

2.3.1 System Signal Layout Guidelines

Table 11. System Signal Layout Guidelines

Debug Port Signal	Layout Guideline
PWR	**If PWR is used to arbitrate with a local TAP master for control of the scan chain:** Pull-up resistor to VTERM and an open drain control gate must be located less than 1 ns from the debug port. **If PWR is not used to arbitrate with a local TAP master for control of the scan chain:** Pull-up resistor to VTERM must be located less than 1 ns from the debug port.
BCLK(p/n) [1.]	BCLK for the debug port should originate as a unique output of the system clock tree. The BCLK routed from the clock distribution component to the debug port must have a propagation delay equal to the length of the BCLK traces from the clock distribution component to the other front side bus agents plus the electrical length of the BPM[5:0]# and RESET# signals as measured from the nearest system bus agent to the debug port. This will ensure that these critical signals have the same phase relationship at the debug port as is seen at the processor. BCLK is a differential high speed clock supplied by the target system. It is a critical system signal requiring careful timing and signal integrity considerations.
FBO	FBO is used to monitor the phase relationship of TCK to BCLK and to recover TDO. It is important that the phase of FBO to BCLK at the debug port is the same as the phase of TCK to BCLK at the closest system bus agent. To meet this requirement, the electrical length fixed by BPM[5:0]# and RESET# (between the nearest bus agent routed to the debug port) must also be the electrical length of FBO(TCK) from the closest bus agent back to the debug port. See the Execution Signal Layout Guidelines in this chapter for additional information.

Debug Port Signal	Layout Guideline
FBI	FBI is a fast edge copy of TCK that can optionally be used as the source of scan chain TCK when TCK buffers are implemented on a system board. FBI should be loaded with no greater than 40 pF and have a DC load of no less than 200 Ω to GND. If used, this is a critical clock for the scan chain and must be analyzed for signal quality and timing with respect to the specifications of the intended receiver of the FBI signal.
DBR#	This is a non-critical route.
DBA#	This is a non-critical route.

NOTE: Refer to BCLK system requirements for proper termination requirements and routing rules.

DBA# and DBR# are output signals from the ITP. The ITP provides an open drain FET closure to GND as the drive of DBA# and DBR#. The target system should provide the pull-up for both of these signals. The pull-up can be to any voltage up to five volts that is consistent with the input specifications of the component used to receive these signals on the target system. DBR# is the ITP debug port reset signal that should always be routed to the system reset controller. DBA# is the ITP debug port scan active signal used to indicate that the ITP is currently driving the scan chain. DBA# is an optional signal of the debug port.

2.3.2 JTAG Signal Layout Guidelines

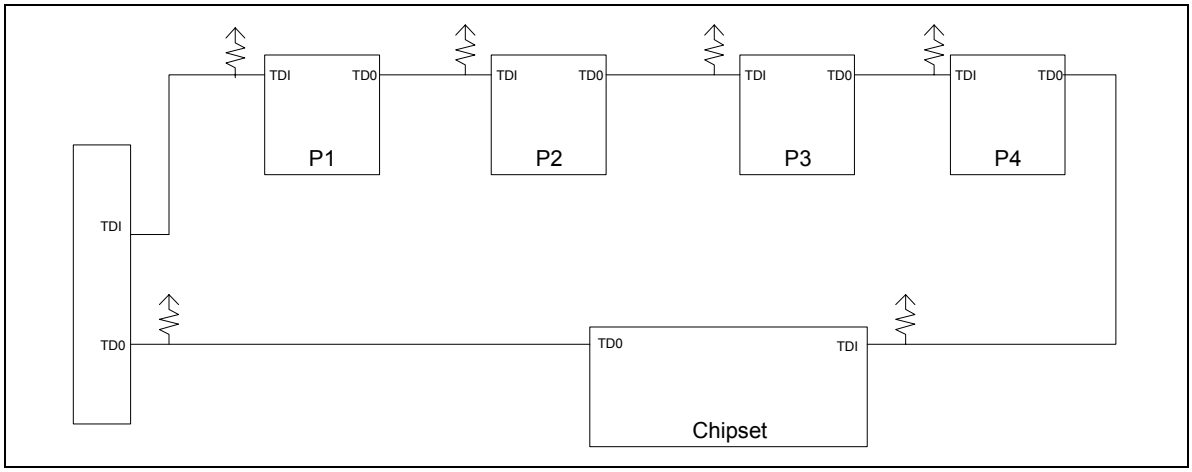
Table 12. JTAG Signal Layout Guidelines

Debug Port Signal	Layout Guideline
TCK	This is a critical JTAG clock signal, sourced by the debug port, which requires thorough timing and signal integrity analysis/simulation. Since there are usually multiple loads on TCK, a matched star topology of up to 8 arms, and originating within 200 ps of the debug port is strongly recommended. The termination resistor to GND on TCK must be located within 200 ps of the debug port in order to minimize IR losses that would degrade signal voltage levels at the loads. Arms for the TCK star should not exceed 2 ns in electrical length and all arms should be matched within 100 ps. Note that one arm of the star should return a feedback copy of TCK to FBO at the debug port. The length of the trace between the processor or chipset TCK pin on this arm and the debug port must be equal to the electrical length of BPM[5:0] and RESET# from the closest system bus agent to the debug port. Load capacitance at the end of each arm must be no more than 35 pF. It is strongly recommended that this signal be simulated for signal integrity purposes. Non-monotonicity on the rising or falling edge of TCK will render the ITP inoperative. See the Execution Signal Layout Guidelines section of this chapter for additional information.
TMS	Critical JTAG mode select signal, sourced by the debug port, which requires moderate timing and signal integrity analysis / simulation. Since there are usually multiple loads on TMS, a matched star topology of up to 8 arms, and originating within 200 ps of the debug port is recommended. The termination resistor to VTAP on TMS should be located within 200 ps of the debug port in order to minimize resistive losses that would degrade signal voltage levels at the loads. Arms for the TMS star should be matched within 400 ps to the length of the TCK star.

Debug Port Signal	Layout Guideline
TDI, TDO	JTAG scan data signals. These signals require minor timing and signal integrity analysis / simulation, These signals are routed point-to-point, possibly through device bypass mechanisms. The terminations should be located within 300 ps to each load. TDI is driven on the falling edge of TCK at the ITP and recovered on the following rising edge of TCK at the processor.
TRST#	Non-critical JTAG reset signal routed to all scan chain devices. TRST# requires a pull-down resistor to ensure the signal is held in the asserted (low) state if the debug port is not driving the signals. Layout of this signal needs to be such that noise will not be coupled to the signal and cause a false reset of the scan chain.

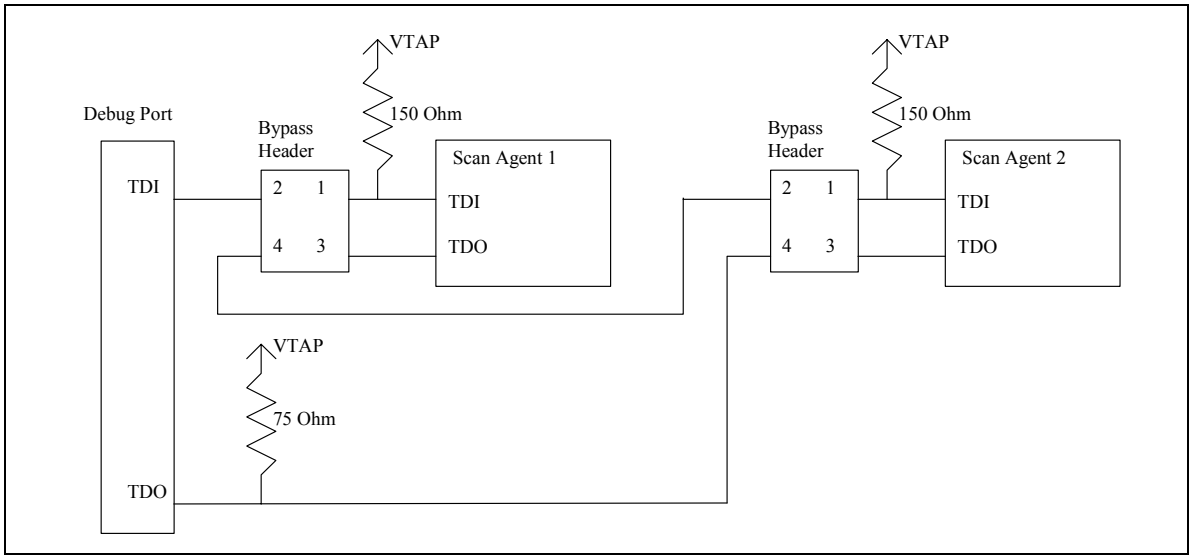
The following figure demonstrates a possible JTAG scan chain for a processor node debug port. It is a requirement to pull up TDI/TDO between each scan chain agent. Note that when the number of processors is changed, a bypass must be used for the empty sites. Care must be taken to ensure that multiple pull-up resistors do not get connected to a single TDI/TDO net if bypassing of empty sites is implemented using “jumpers”. Failure to do so might result in overloading and possibly damaging the sourcing component or the ITP.

Figure 6. TDI/TDO Scan Chain



The following figure shows the recommended bypass option using a four-pin header to bypass a device location. This method can remove devices from the scan chain whether the device is physically present or not. To include a device in the chain, connect the TDO output from the previous device in the chain (Pin-2) to the TDI input of the current device (Pin-1), and connect the TDO output from the current device (Pin-3) to the TDO going to the next device (Pin-4). The pull-up resistor needs to be placed on the current device TDI to function properly. To remove a device from the scan chain, (device can be physically present or not present) connect the TDO output from the previous device (Pin-2) to the TDO going to the next device (Pin-4). This four-pin jumper bypass configuration eliminates drive conflicts encountered when a partially bypassed device is still capable of driving data to onto the JTAG data chain. Note that the TDI/TDO pull-up requirements defined in the beginning of this section are met in the following diagram under any bypass configuration.

Figure 7. Recommended Bypass Jumper Configuration



When well designed, Quickswitches can be used to replace bypass jumpers/headers. System designers should select a Quickswitch package that contains a low resistance (~7 Ω) and low capacitance (~5 pF) analog bypass switch (FET) It should be noted that both the jumper and the Quickswitch designs add capacitance and resistance to the TDI/TDO line for each device bypassed. This RC delay can slow down the rise time significantly when multiple devices are being bypassed. For example, if a design includes an analog switch of ~15 Ω of resistance and ~20 pF of capacitance used for scan chain bypass, and three scan chain agents are bypassed simultaneously, TDI will experience an added time delay of 0.9 ns. This added delay must be accounted for during timing analysis for recovery setup and hold of TDI under all intended operating frequencies. Careless design in this area may result in maximum scan frequency degradation or, even worse, scan data corruption.

2.3.3 Execution Signal Layout Guidelines

Table 13. Execution Signal Layout Guidelines

Debug Port Signal	Layout Guideline
BPM[5:0]#	These signals are extremely routing critical. The debug port recovers these signals relative to BCLK at the debug port pins. Therefore, the signals must be routed with closely matched electrical lengths (within ±50 ps) and no greater than 1.0 ns from the closest system bus agent to the debug port.
BPM5DR#	The debug port BPM5DR# output pin should be connected on the board to the BPM5# pin of the debug port. This allows the ITP or run-control tool to drive BPM5# at reset. It also allows ITP to assert BPM5# if ITP needs to assert a trigger signal that can be seen directly by the target system. Note that ITP asserts / de-asserts this signal asynchronous to the bus BCLK.

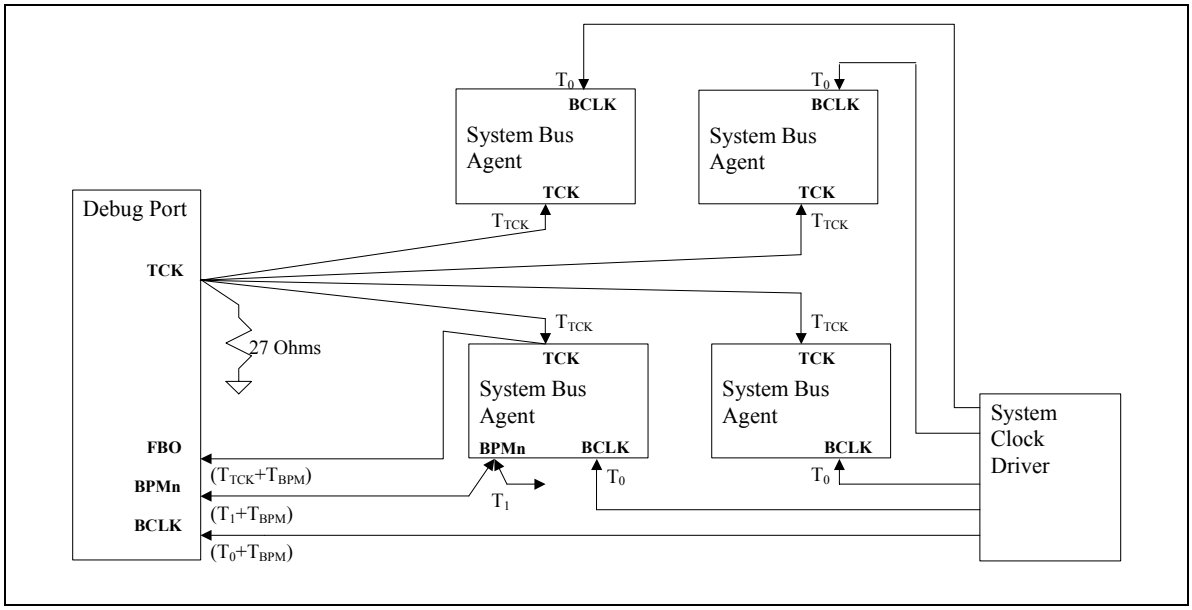
The debug port should be placed as close as is physically reasonable to the processor and no further than 1.0 ns flight time (as measured by trace length of the BPM[5:0]#) from the processor. System designers should record the flight time of the BPM[5:0]# signals from the processor to the debug port. This value will be important during the routing of several other debug port signals. Ideally BPM[5]# will be routed from the processor to the debug port BPM[5]# pin matched with the other BPM# s. From pin 13 the trace will route directly to the debug port BPM5DR# pin and continue to the termination of the transmission line.

Assuming BCLK(p/n) signals are routed from the system clock buffer to each of the synchronous clock agents with a matched length, the copy of BCLK(p/n) from the system clock buffer to the ITP debug port must have a flight time equal to the matched length of the other synchronous clock agents plus the flight time of the BPM[5:0]# signals from the nearest bus agent to the debug port noted above. This will ensure that the same BCLK to BPM[5:0]# phase relationship seen at the closest system bus agent will be present at the debug port pins. BCLK trace lengths may be adjusted to center the recovery of BPM[5:0]# and RESET# at the debug port within the ITP receiver setup and hold window.

Multiple layer transitions of the BCLK, BPM, and TCK signals will compromise signal integrity. An effort should be made to minimize the number of layer transitions for these signals. Try to keep the BCLK, BPM, and TCK signals referenced to GND whenever possible. If layer transitions are required, stitching vias should be included near ever every layer transition of the BCLK, BPM, and TCK signals, even when not referencing the same voltage. This is recommended to reduce the lengths of return current loops. Adding an AC bypass capacitor near every layer transition or plane split between the two referenced planes will also help to minimize AC return current loops. An effort should be made to not share ITP AC bypass capacitors with other high-speed signals.

TCK and TMS have been successfully routed in a star topology with pull-up / pull-downs located at the driver. FBO is routed such that it is connected to the TCK at the nearest system bus agent, and routed back to the debug port with an electrical length equal to the flight time of the BPM[5:0]# signals from the same system bus agent to the debug port. This is done to guarantee that the BCLK to TCK phase relationship at the closest system bus agent will be seen at the debug port FBO and BCLK(p/n) pins. The diagram below illustrates these routing relationships.

Figure 8. Recommended Layout Topology



NOTES:

1. All of the above routes must be simulated to ensure signal integrity. Failure to do so may result in non-functional ITP.
2. All combination timings in the above drawing are ± 50 ps in routing length maximum.

The figure above defines propagation delays of various ITP signals from the driver to the receiver. The following are definitions of individual trace segments that are included in the figure.

- **T_{TCK}** – Propagation delay of the TCK trace from the debug port to the system bus agent TCK pin
- **T_{BPM}** – Propagation delay of the BPM traces from the debug port to the nearest system bus agent.
- **T_0** – Propagation delay of BCLK from the system clock driver to the processors and chipset Components
- **T_1** – Propagation delay of the BPM traces from the driving system bus agent to the system bus agent closest to the debug port.

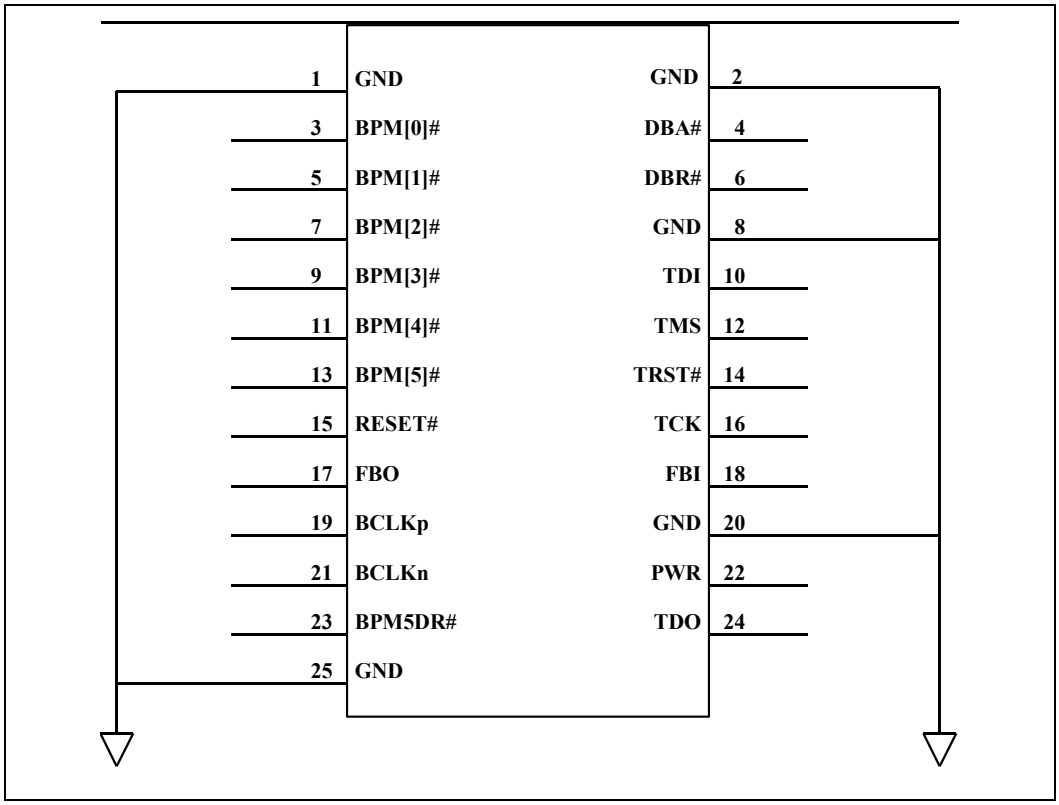
This page is intentionally left blank.

3 ITP700 DPA Specifications

3.1 ITP700 DPA Specifications

The signals used by the ITP are divided into three categories: system, JTAG, and execution. The system signal group indicates the access state of the entire system. The JTAG signal group indicates the IEEE* 1149.1 control signals. The execution signal group contains the reset and run control signals used to coordinate debug activities. The signals in the execution group are system bus signals and are recovered on BCLK. The signals in the JTAG group can operate up to 16 MHz.

Figure 9. ITP700 DPA Debug Port Pinout (Top View)



NOTES:

1. All execution signals, BCLK(p/n), and all JTAG signals must be simulated and routed with care. See the appropriate generic layout and processor specific chapters for details.
2. The system clock of the processor may reference BCLK[1:0] where BCLK0 is the rising edge for the beginning of any transaction and BCLK1 as the falling edge. The ITP uses BCLK[p/n] where BCLKp is the rising edge and BCLKn is the falling edge for the beginning of any transaction. All routing Rules for the BCLK signals do not change.

The following tables identify the signals that make up the ITP debug port connector definition. The I/O direction indicated for each signal is with respect to the debug port. Local TAP refers to a resident TAP master system that has been installed as part of a system designer's manufacturing process. Values of required pull up and pull down resistors are documented in the recommended termination table in this chapter.

Table 14. ITP700 DPA System Signal Descriptions

Debug Port Signal	Pin #	I/O	Description
PWR	22	Input	System Power. PWR is used for three purposes on the ITP hardware: To generate the recovery reference voltage for the BPM[5:0]# and RESET# signals. To sense if the target has stable power at the debug port. To arbitrate for the scan chain (in conjunction with DBA#) if a local TAP master exists. If PWR is asserted (High), the ITP will be allowed to take and maintain control of the JTAG signals, but if PWR is de-asserted (pulled low by an open drain on the target), the debug port output signals will be tristated by the ITP.
BCLK(p/n)	19/21	Input	Differentially driven Bus Clock of the target system. Used to sample execution signals, and to provide a reference for delay align signals driven from the debug port. When the ITP is operating in synchronous mode, TCK is delay locked (skewed) to BCLK(p/n).
DBA#	4	Output	Debug Port Active. The DBA# signal is an output of the ITP that indicates that the ITP is using the target system TAP interface. This signal is optional for ITP implementation. This signal is open drain and must be provided with a pull-up resistor on the target if this signal is used.
DBR#	6	Output	Debug Port Reset. Open drain signal used to tell the target to initiate a reset through the reset controller. The ITP can hold this signal Low for a configurable period or perpetually. This signal is open drain and must be provided with a pull-up resistor on the target.
FBI	18	Output	Alternate source of TAP master clock. FBI is a copy of TCK without passive edge rate control. When a buffered copy of TCK is required for routing or level shifting, FBI should be used as the source for the scan chain TCK. FBI is optional for most ITP implementations since TCK is generally used as the TAP master clock.
FBO	17	Input	FBO is used to register TDO into the ITP tool.

Table 15. JTAG Signal Descriptions

Debug Port Signal	Pin #	I/O	Description
TCK	16	Output	Standard source of TAP master clock. TCK must have a pull down resistor provided on the target system. The debug port drives TCK at up to 16 MHz if so enabled. TCK can be skewed with respect to BCLK(p/n). TCK is optional for ITP implementation only if FBI is used as the TAP master clock.
TDI	10	Output	TAP data input signal. TDI is an output of the ITP driven into the target system and recovered by the first agent of the scan chain. TDI must have a pull up resistor provided on the target system. TDI will require bypass logic for devices that are optionally installed. TDI is driven on TCK's falling edge and should be sampled on TCK's rising edge.
TDO	24	Input	TAP data output signal. TDO is an output of the last agent of the scan chain and recovered by the ITP. TDO must have a pull up resistor provided on the target system. TDO is sampled on the rising edge of FBO (TCK), and should be driven on the falling edge of TCK.
TMS	12	Output	TAP state management signal. This signal must have a pull up resistor provided on the target system. TMS is driven on TCK's falling edge and should be sampled on TCK's rising edge.
TRST#	14	Output	Test Logic Rest. TRST# transitions asynchronously to TCK. TRST# must be provided with a pull-down resistor on the target.

Table 16. Execution Signal Descriptions

Debug Port Signal	Pin #	I/O	Description
BPM[5:0]#	13, 11, 9, 7, 5, 3	Input	BPM[5:0]# are input break point signals from the target system. These inputs are recovered on a rising BCLK(p/n) rising edge using the voltage seen and the debug port PWR pin as a reference. These signals are routing critical.[1]
RESET#	15	Input	RESET# is an input reset signal from the target system. This input is recovered on a rising BCLK(p/n) rising edge using the voltage seen and the debug port PWR pin as a reference. This signal is routing critical. This signal does not reset the ITP hardware.
BPM5DR#	23	Output	BPM5DR# is the debug tool's break at reset signal. [1]

NOTES:
1. BPM5# should be shorted to BPM5DR# on the target system at the debug port.

3.2 ITP700 DPA DC Electrical Characteristics

Table 17. ITP700 DPA System Signal DC Characteristics

Signal		Min	Max	Unit	Note
FBI	V_{OH}	1.00		V	1
	V_{OL}		0.40	V	1
	I_{OH}	-5		mA	
	I_{OL}		5	mA	
FBO	V_{IH}	0.90	1.70	V	
	V_{IL}	0.00	0.55	V	
	I_{IH}	-150		µA	
	I_{IL}		300	µA	
PWR	V_{IH}	0.30	2.80	V	2
	V_{IL}		0.10	V	3
	R_{PWR}	2.95	3.05	kΩ	4
BCLK(p/n)	V_{IH}		1.70	V	
	V_{IL}	0.10		V	
	V_{PTP}	300		mV	5
	I_{IH}	-1		mA	
	I_{IL}		300	µA	
	C_{IN}		10	pF	6
DBA#, DBR#	Ω		6	Ω	7
	I_{DBX}		120	mA	8

NOTES:
1. At maximum output current specified.
2. V_{IH} Max represents the maximum functional voltage of this pin.
3. ITP outputs will be tri-stated when input voltage is sensed low.
4. Resistance from pin to GND.
5. V_{PTP} defined as voltage between both the high and low sides of the signal swing.
6. Including capacitive effects of mated connector.
7. Resistance from pin to GND when active.
8. Maximum sink current of ITP.

Table 18. ITP700 DPA JTAG Signal DC Electrical Characteristics

Signal		Min	Typ	Max	Unit	Note
TCK	V_{OH}	1.25			V	1
	V_{OL}			0.3	V	2
	I_{OH}	-47			mA	
	I_{OL}			0	mA	
	Z_{TCK}		20		Ω	3
TMS	V_{OH}	1.30			V	4
	V_{OL}			0.30	V	4
	I_{OH}	-10			mA	
	I_{OL}			35	mA	
	Z_{TMS}		20		Ω	3
TDI, TRST#	V_{OH}	1.3			V	1
	V_{OL}			0.3	V	1
	I_{OH}	-5			mA	
	I_{OL}			5	mA	
TDO	V_{IH}	0.90		1.7	V	
	V_{IL}	0		0.55	V	
	I_{IH}	-150			µA	
	I_{IH}			300	µA	

NOTES:
1. At maximum current specified.
2. As measured into a 27 Ω 1% resistor to GND.
3. AC Impedance of the driver.
4. As measured into a 39 Ω 1% resistor to 1.10 V

Table 19. ITP700 DPA Execution Signal DC Electrical Characteristics

Signal		Min	Max	Unit	Note
BPM5DR#	I_{OL}		120	mA	1
	R_{OL}		18	Ω	2
	C_{IN}		4	pF	3
BPM[5:0]#, RESET#	V_{IH}	PWR + (0.15*VTERM)	3.00	V	4
	V_{IL}		PWR - (0.15*VTERM)	V	4
	I_{IH}	-150		uA	
	I_{IL}		300	uA	
	C_{IN}		3	pF	3

NOTES:
1. Maximum sink current of the ITP.
2. Series resistance to GND when output is low.
3. Includes capacitive effects of mated connector.
4. Over valid range of VIH of PWR.

3.3 ITP700 DPA AC Electrical Characteristics

Table 20. ITP700 DPA System Signal AC Electrical Characteristics

Signal	Parameter	Min	Max	Unit	Note
PWR	PWR V_{IL} Max to Tristate	150		µs	
FBI	Rise Time	0.5	2	ns	1, 2, 3
	Fall Time	0.5	2	ns	1, 2, 3
	Skew	-9	-6	ns	4
DBA#	DBA#↓ to first TCK↑	75		ns	5
	DBA#↑ to last TCK↓		100	ns	6
DBR#	DBR# Assertion Period	150		µs	

NOTES:
1. Measured from 20% to 80% of transition.
2. Measured into a load to GND of 220 Ω and 10 pF.
3. FBI has the same period; time High, and time Low specifications as TCK.
4. With respect to same edge on TCK.
5. Measured from assertion of DBA# to 50% of first TCK transition.
6. Measured from release of DBA# to 50% of last TCK transition.

Table 21. ITP700 DPA JTAG Signal AC Electrical Characteristics

Signal	Parameter	Min	Max	Unit	Note
TDO	Setup	5		ns	1
	Hold	0.5		ns	1
	Rise/Fall Time		15	ns	2
TCK	Rise/Fall Time	9	13	ns	2, 3
	Period	58		ns	4
	Time High	25		ns	5
	Time Low	25		ns	5
TMS	Rise/Fall Time	7	16	ns	2, 6
	Clock to Out	-5	0	ns	7
TDI	Rise Time	0.5	2.0	ns	2, 8
	Fall Time	0.5	2.0	ns	2, 8
	Clock to Out	-8	0	ns	7
TRST#	Assert Time	300		ns	

NOTES:

1. With respect to rising edge of FBO at the debug port using 50% of transition for both signals.
2. Measured from 20% to 80% of transition.
3. As measured into a 27 Ω and 35pF load to GND.
4. Measured from 50% of rising edge to 50% of next rising edge. This specification is valid for asynchronous and synchronous operation.
5. Measured from 50% of first edge to 50% of second edge.
6. As measured into a 39 Ω load to VTAP and 35pF to GND.
7. With respect to falling edge of TCK at the debug port using 50% of transition for both signals.
8. As measured into a 1500 Ω load to VTAP and 10pF to GND.

Table 22. ITP700 DPA Execution Signal AC Electrical Characteristics

Signal	Parameter	Min	Max	Unit	Note
BPM[5:0]#, RESET	Setup	400		ps	1
	Hold	200		ps	1
BCLK(p/n)	Rise Time		5	ns	2
	Fall Time		5	ns	2
	Period	5	15	ns	3
	Time High	2.2		ns	
	Time Low	2.2		ns	
BPM5DR#	Rise Time	1	4	ns	2, 4
	Fall Time	8	15	ns	2, 4

NOTES:
1. With respect to BCLK(p/n).
2. Measured from 20% to 80% of transition.
3. Specification for valid synchronous operation of the ITP. Asynchronous operation has no Max specification but shares the Min specification listed.
4. Measured into a load to 1.5 V of 50 Ω s and 35 pF to GND.

3.4 Pin Absolute Maximums

The following data represents the maximum voltage that the pins of the ITP can sustain without damage. These values do not reflect a valid operating range. See DC specification sections for valid operating ranges for each signal.

Table 23. P700 DPA Pin Absolute Maximums

Signal	Voltage Low	Voltage High
PWR	0 V	5 V
BCLK	-1.2 V	2.5 V
DBA# DBR#	-0.5 V	5 V
FBI	-0.5 V	4.6 V
FBO	-1.2 V	2.5 V
TCK	-0.5 V	4.6 V
TMS	-0.5 V	4.6 V
TDI	-0.5 V	4.6 V
TDO	-1.2 V	2.5 V
TRST#	-0.5 V	4.6 V
BPM[5:0]#,	-1.2 V	3.3 V
BPM5DR#	-0.5 V	5 V
RESET#	-1.2 V	3.3 V

3.5 Mechanical Requirements

The ITP debug port adapter (DPA) plugs into the target system's onboard debug port connector. The ITP cable connects the DPA hardware to the ITP hardware located on a host system. The host system runs the ITP software. In order for the ITP cabling to egress the system under test, an aperture of two inches minimum width by one-inch minimum height must be available. Please contact your run-control tool vendor for complete mechanical constraints for other tools.

Examples of connectors that will fulfill the requirements of a debug port connector would be either the Framatome Connectors International* (FCI*) #61641-303 which is a 25 pin through-hole mount header or the FCI* #61698-302TR which is a 25 pin surface mount header. The surface mount version is recommended for its compatibility with a new feature on the DPA. This feature provides improved retention of the DPA to the header and is particularly useful on boards that may be oriented vertically or where the DPA is located on the bottom side of the board. Full specifications for these connectors, including PCB layout guidelines, are available from an FCI sales representative. Please note that changes in the keepout volume have been made in order to accommodate the new retention feature of the ITP. All dimensions in the following diagrams are in units of inches.

Figure 10. Debug Port Connectors

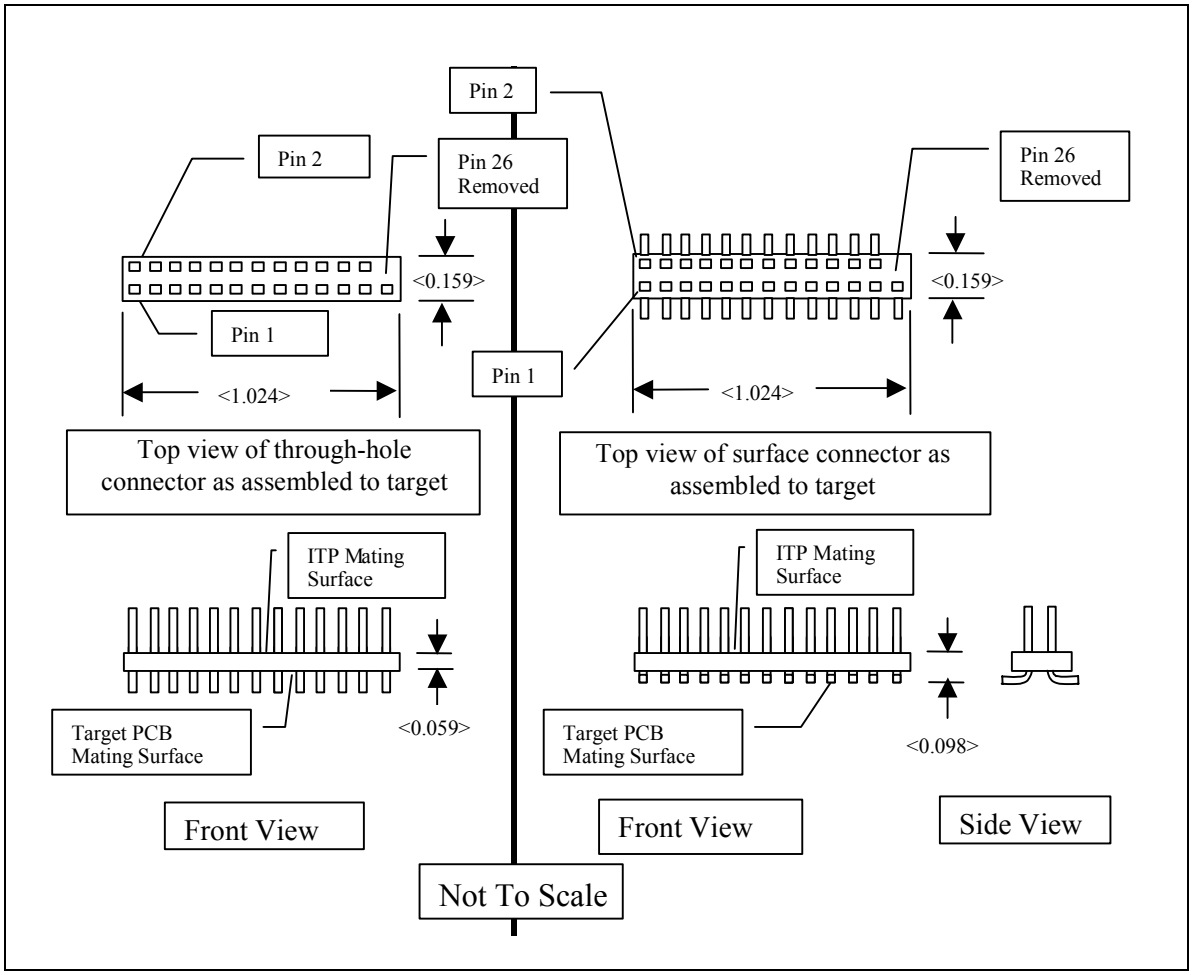
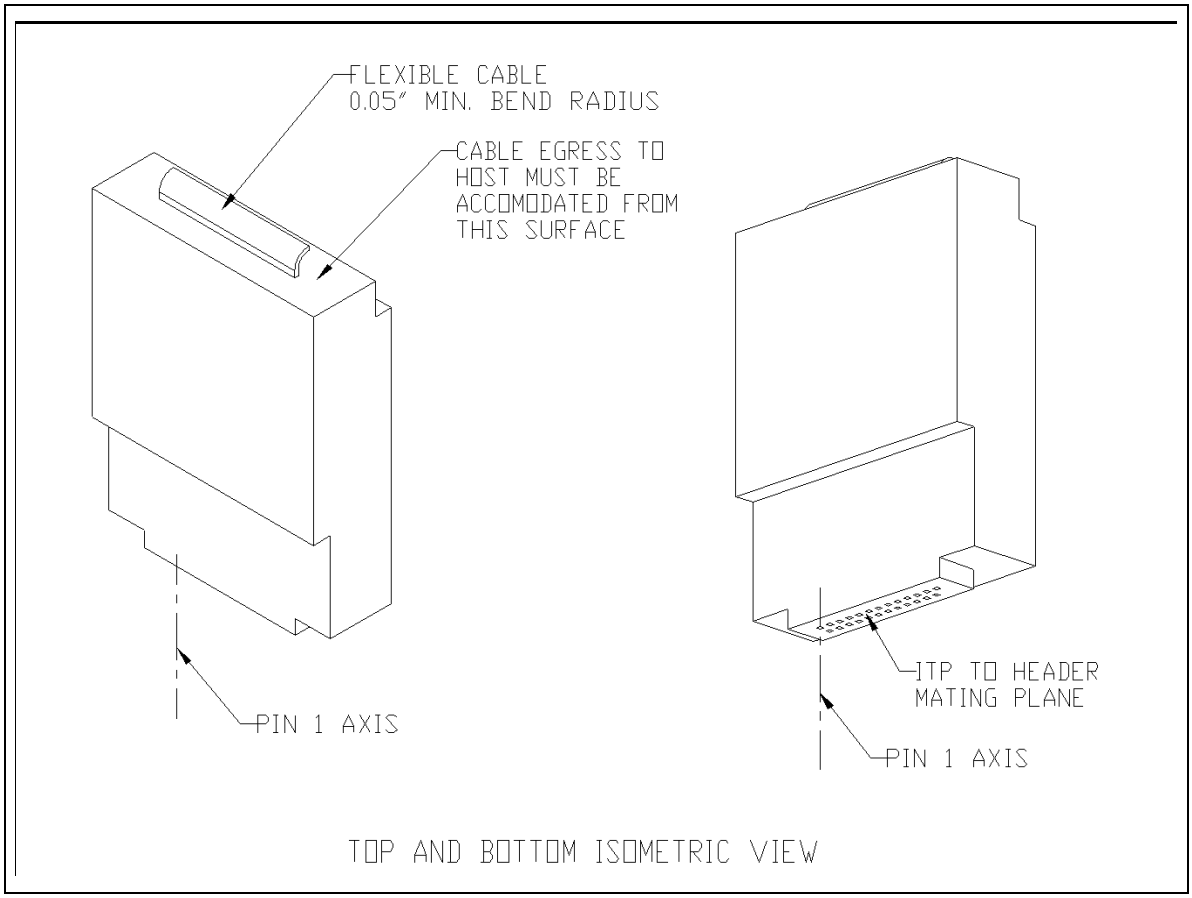
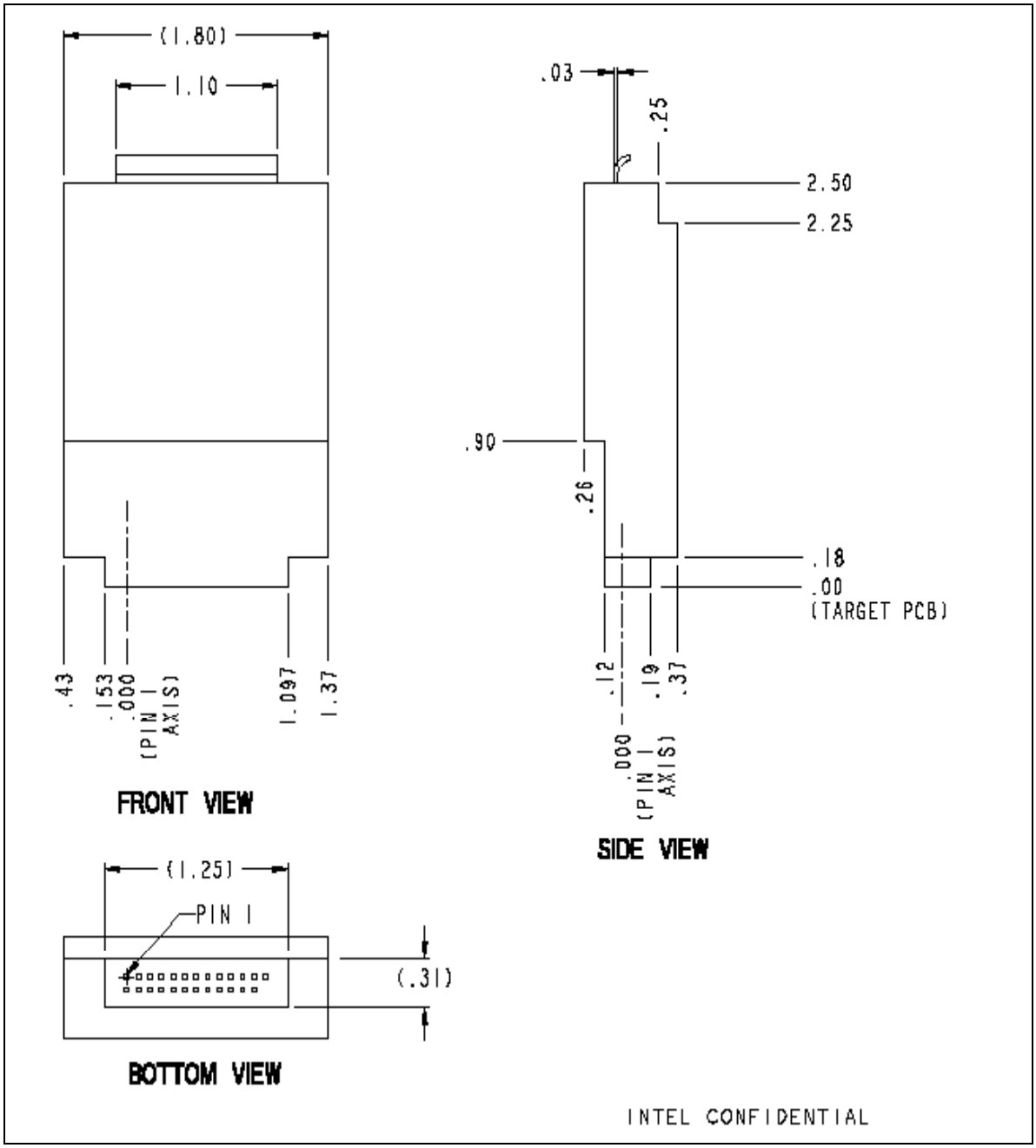


Figure 11. Isometric View of Debug Port Adapter Keepout Volume



NOTE: The above figure has no dimensions other than bend radius

Figure 12. Front, Side, and Top View of ITP Debug Port Adapter Keepout Volume



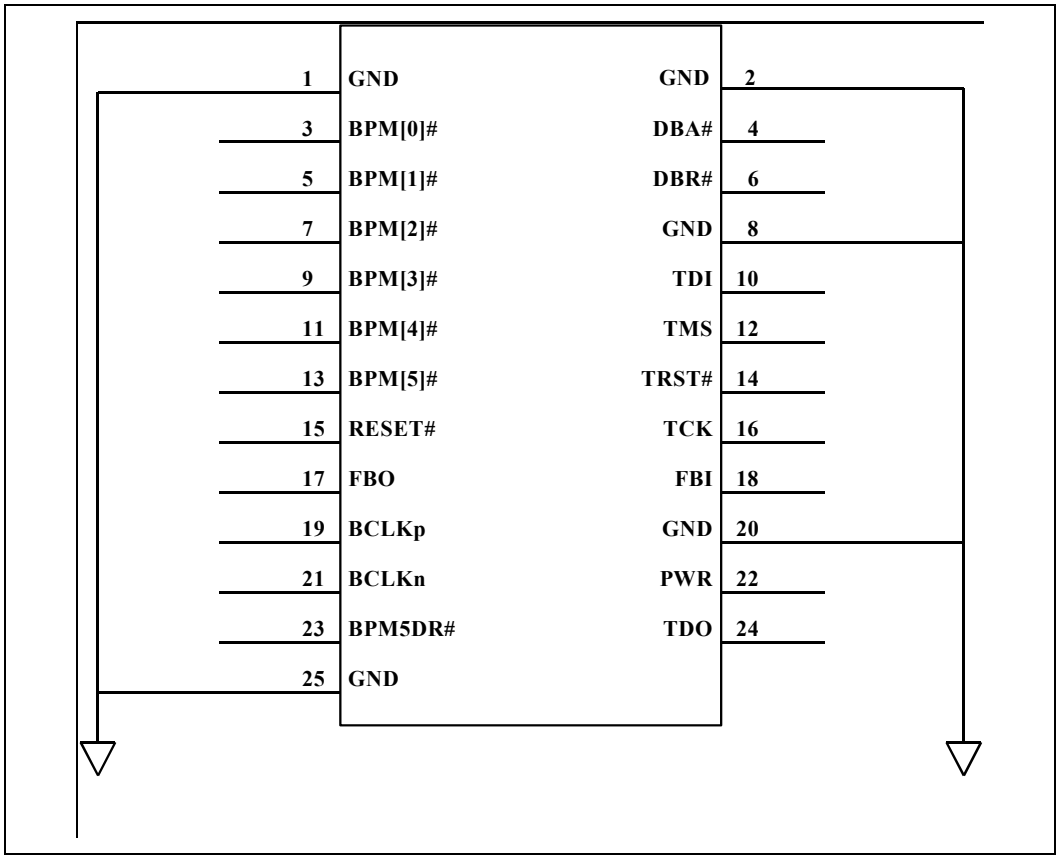
This page is intentionally left blank.

4 ITP700 LVDPA Specifications

4.1 ITP700 LVDPA Signal Descriptions

The signals used by the ITP700 LVDPA are divided into three categories: system, JTAG, and execution. The system signal group indicates the access state of the entire system. The JTAG signal group indicates the IEEE 1149.1 control signals. The execution signal group contains the reset and run control signals used to coordinate debug activities. The signals in the execution group are system bus signals and are recovered on BCLK. The signals in the JTAG group can operate up to 16 MHz.

Figure 13. ITP LVPDA Debug Port Pinout (Top View)



NOTES:

1. All execution signals, BCLK(p/n), and all JTAG signals must be simulated and routed with care. See the appropriate generic layout and processor specific chapters for details.
2. The system clock of the processor may reference BCLK[1:0] where BCLK0 is the rising edge for the beginning of any transaction and BCLK1 as the falling edge. The ITP uses BCLK[p/n] where BCLKp is the rising edge and BCLKn is the falling edge for the beginning of any transaction. All routing Rules for the BCLK signals do not change.

The following tables identify the signals that make up the ITP debug port connector definition. The I/O direction indicated for each signal is with respect to the debug port. Local TAP refers to a resident TAP master system that has been installed as part of a system designer's manufacturing process. Values of required pull up and pull down resistors are documented in the recommended termination table in this chapter.

Table 24. ITP700 LVDPA System Signal Descriptions

Debug Port Signal	Pin #	I/O	Description
PWR	22	Input	System Power. PWR is used for three purposes on the ITP hardware: To generate the recovery reference voltage for the BPM[5:0]# and RESET# signals. To sense if the target has stable power at the debug port. To arbitrate for the scan chain (in conjunction with DBA#) if a local TAP master exists. If PWR is asserted (High), the ITP will be allowed to take and maintain control of the JTAG signals, but if PWR is de-asserted (pulled low by an open drain on the target), the debug port output signals will be tristated by the ITP.
BCLK(p/n)	19/21	Input	Differentially driven Bus Clock of the target system. Used to sample execution signals, and to provide a reference for delay align signals driven from the debug port. When the ITP is operating in synchronous mode, TCK is delay locked (skewed) to BCLK(p/n).
DBA#	4	Output	Debug Port Active. The DBA# signal is an output of the ITP that indicates that the ITP is using the target system TAP interface. This signal is optional for ITP implementation. This signal is open drain and must be provided with a pull-up resistor on the target if this signal is used.
DBR#	6	Output	Debug Port Reset. Open drain signal used to tell the target to initiate a reset through the reset controller. The ITP can hold this signal Low for a configurable period or perpetually. This signal is open drain and must be provided with a pull-up resistor on the target.
FBI	18	Output	Alternate source of TAP master clock. FBI is a copy of TCK without passive edge rate control. When a buffered copy of TCK is required for routing or level shifting, FBI should be used as the source for the scan chain TCK. FBI is optional for most ITP implementations since TCK is generally used as the TAP master clock.
FBO	17	Input	FBO is used to register TDO into the ITP tool.

Table 25. JTAG Signal Descriptions

Debug Port Signal	Pin #	I/O	Description
TCK	16	Output	Standard source of TAP master clock. TCK must have a pull down resistor provided on the target system. The debug port drives TCK at up to 16 MHz if so enabled. TCK can be skewed with respect to BCLK(p/n). TCK is optional for ITP implementation only if FBI is used as the TAP master clock.
TDI	10	Output	TAP data input signal. TDI is an output of the ITP driven into the target system and recovered by the first agent of the scan chain. TDI must have a pull up resistor provided on the target system. TDI will require bypass logic for devices that are optionally installed. TDI is driven on TCK's falling edge and should be sampled on TCK's rising edge.
TDO	24	Input	TAP data output signal. TDO is an output of the last agent of the scan chain and recovered by the ITP. TDO must have a pull up resistor provided on the target system. TDO is sampled on the rising edge of FBO (TCK), and should be driven on the falling edge of TCK.
TMS	12	Output	TAP state management signal. This signal must have a pull up resistor provided on the target system. TMS is driven on TCK's falling edge and should be sampled on TCK's rising edge.
TRST#	14	Output	Test Logic Rest. TRST# transitions asynchronously to TCK. TRST# must be provided with a pull-down resistor on the target.

Table 26. Execution Signal Descriptions

Debug Port Signal	Pin #	I/O	Description
BPM[5:0]#	13, 11, 9, 7, 5, 3	Input	BPM[5:0]# are input break point signals from the target system. These inputs are recovered on a rising BCLK(p/n) rising edge using the voltage seen and the debug port PWR pin as a reference. These signals are routing critical.[1]
RESET#	15	Input	RESET# is an input reset signal from the target system. This input is recovered on a rising BCLK(p/n) rising edge using the voltage seen and the debug port PWR pin as a reference. This signal is routing critical. This signal does not reset the ITP hardware.
BPM5DR#	23	Output	BPM5DR# is the debug tool's break at reset signal. [1]

NOTES:
1. BPM5# should be shorted to BPM5DR# on the target system at the debug port.

4.2 ITP700 LVDPA DC Electrical Characteristics

Table 27. ITP LVDPA System Signal DC Characteristics

Signal		Min	Max	Unit	Note
FBI	V_{OH}	0.9*VTAP	VTAP+0.250	V	1, 9.
	V_{OL}	0	0.1*VTAP	V	1
	I_{OH}	-8		mA	
	I_{OL}		16	mA	
FBO	V_{IH}	0.5*VTAP +0.150		V	
	V_{IL}		0.5*VTAP -0.150	V	
	I_{IH}	-100		µA	
	I_{IL}		100	µA	
PWR	V_{IH}	0.30	2.80	V	2
	V_{IL}		0.10	V	3
	R_{PWR}	2.95	3.05	kΩ	4
BCLK(p/n)	V_{IH}		1.70	V	
	V_{IL}	0.10		V	
	V_{PTP}	300		mV	5
	I_{IH}	-1		mA	
	I_{IL}		300	µA	
	C_{IN}		10	pF	6
DBA#, DBR#	R_{DBX}		6	Ω	7
	I_{DBX}		120	mA	8

NOTES:
1. At maximum output current specified.
2. V_{IH} Max represents the maximum functional voltage of this pin.
3. ITP outputs will be tri-stated when input voltage is sensed low.
4. Resistance from pin to GND.
5. V_{PTP} defined as voltage between both the high and low sides of the signal swing.
6. Including capacitive effects of mated connector.
7. Resistance from pin to GND when active.
8. Maximum sink current of ITP.
9. FBI Voltage tracking for VOH has a lower limit of 1.2 V.

Table 28. ITP700 LVDPA JTAG Signal DC Electrical Characteristics

Signal		Min	Typ	Max	Unit	Note
TCK	V_{OH}	0.9*VTAP		VTAP + 0.250	V	2
	V_{OL}	0		0.1*VTAP	V	2
	I_{OH}	-60mA			mA	
	I_{OL}			0	mA	
	Z_{TCK}		20		Ω	3
TMS	V_{OH}	0.9*VTAP		VTAP + 0.250	V	4
	V_{OL}	0		0.1*VTAP	V	4
	I_{OH}	-16			mA	
	I_{OL}			36	mA	
	Z_{TMS}		20		Ω	3
TDI	V_{OH}				V	5
	V_{OL}	0		0.1*VTAP	V	1
	I_{OH}	0			mA	
	I_{OL}			8	mA	
TRST#	V_{OH}	0.9*VTAP		VTAP + 0.250	V	1
	V_{OL}	0		0.1*VTAP	V	1
	I_{OH}	-8			mA	
	I_{OL}			8	mA	
TDO	V_{IH}	0.5*VTAP +0.150			V	
	V_{IL}			0.5*VTAP -0.150	V	
	I_{IH}	-100			µA	
	I_{IL}			100	µA	

NOTES:
1. At maximum current specified.
2. As measured into a 27 Ω 1% resistor to GND.
3. AC Impedance of the driver.
4. As measured into a 39 Ω 1% resistor to 1.10V.
5. Open Drain Driver on the LVDPA

Table 29. ITP700 LVDPA Execution Signal DC Electrical Characteristics

Signal		Min	Max	Unit	Note
BPM5DR#	I_{OL}		120	mA	1
	R_{OL}		18	Ω	2
	C_{IN}		4	pF	3
BPM[5:0]#, RESET#	V_{IH}	PWR + (0.15*VTERM)	3.00	V	4
	V_{IL}		PWR - (0.15*VTERM)	V	4
	I_{IH}	-150		µA	
	I_{IL}		300	µA	
	C_{IN}		3	pF	3

NOTES:
1. Maximum sink current of the ITP.
2. Series resistance to GND when output is low.
3. Includes capacitive effects of mated connector.
4. Over valid range of VIH of PWR.

4.3 ITP700 LVDPA AC Electrical Characteristics

Table 30. ITP700 LVDPA System Signal AC Electrical Characteristics

Signal	Parameter	Min	Max	Unit	Note
PWR	PWR V_{IL} Max to Tristate	150		µs	
FBI	Rise Time	0.5	2	ns	1, 2, 3
	Fall Time	0.5	2	ns	1, 2, 3
	Skew	-9	-6	ns	4
DBA#	DBA#↓ to first TCK↑	75		ns	5
	DBA#↑ to last TCK↓		100	ns	6
DBR#	DBR# Assertion Period	150		µs	

NOTES:
1. Measured from 20% to 80% of transition.
2. Measured into a load to GND of 220 Ω and 10 pF.
3. FBI has the same period; time High, and time Low specifications as TCK.
4. With respect to same edge on TCK.
5. Measured from assertion of DBA# to 50% of first TCK transition.
6. Measured from release of DBA# to 50% of last TCK transition.

Table 31. ITP700 LVDPA JTAG Signal AC Electrical Characteristics

Signal	Parameter	Min	Max	Unit	Note
TDO	Setup	5		ns	1
	Hold	0.5		ns	1
	Rise/Fall Time		15	ns	2
TCK	Rise/Fall Time	9	13	ns	2, 3
	Period	58		ns	4
	Time High	25		ns	5
	Time Low	25		ns	5
TMS	Rise/Fall Time	7	16	ns	2, 6
	Clock to Out	-5	0	ns	7
TDI	Rise Time	0.5	2.0	ns	2, 8
	Fall Time	0.5	2.0	ns	2, 8
	Clock to Out	-8	0	ns	7
TRST#	Assert Time	300		ns	

NOTES:
1. With respect to rising edge of FBO at the debug port using 50% of transition for both signals.
2. Measured from 20% to 80% of transition.
3. As measured into a 27 Ω and 35 pF load to GND.
4. Measured from 50% of rising edge to 50% of next rising edge. This specification is valid for asynchronous and synchronous operation.
5. Measured from 50% of first edge to 50% of second edge.
6. As measured into a 39 Ω load to VTAP and 35pF to GND.
7. With respect to falling edge of TCK at the debug port using 50% of transition for both signals.
8. As measured into a 1500 Ω load to VTAP and 10pF to GND.

Table 32. ITP700 LVDPA Execution Signal AC Electrical Characteristics

Signal	Parameter	Min	Max	Unit	Note
BPM[5:0]#, RESET	Setup	400		ps	1
	Hold	200		ps	1
BCLK(p/n)	Rise Time		5	ns	2
	Fall Time		5	ns	2
	Period	5	15	ns	3
	Time High	2.2		ns	
	Time Low	2.2		ns	
BPM5DR#	Rise Time	1	4	ns	2, 4
	Fall Time	8	15	ns	2, 4

NOTES:
1. With respect to BCLK(p/n).
2. Measured from 20% to 80% of transition.
3. Specification for valid synchronous operation of the ITP. Asynchronous operation has no Max specification but shares the Min specification listed.
4. Measured into a load to 1.5 V of 50 Ω and 35 pF to GND.

5 ITP700 Flex Mechanical Requirements

The pinout of the debug port connector at the end of the ITP700 Flex is identical to that of the standard debug port connector.

The surface mount device is a Molex #52499-001 or equivalent. This connector does not need to be included on the BOM for production motherboards. It is expected that the connector footprint be included on the baseboard in a location that will allow the connector to be reworked onto the board. Note that this surface mount connector is a fine pitch device.

Contact your surface mound device vendor of choice to obtain keepout volumes and footprints of the Molex connector

Figure 14. ITP700 Flex Mechanical Drawing

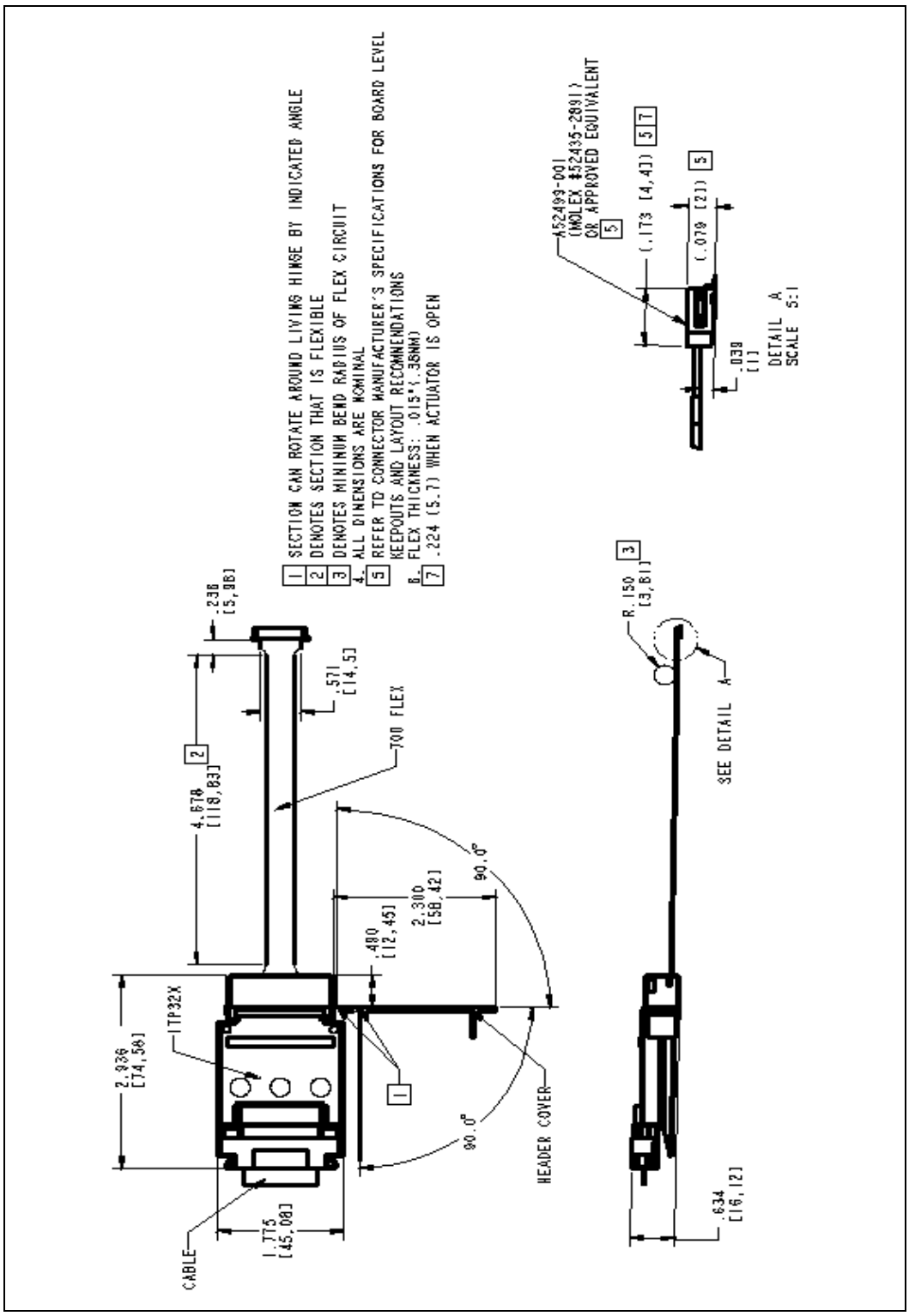
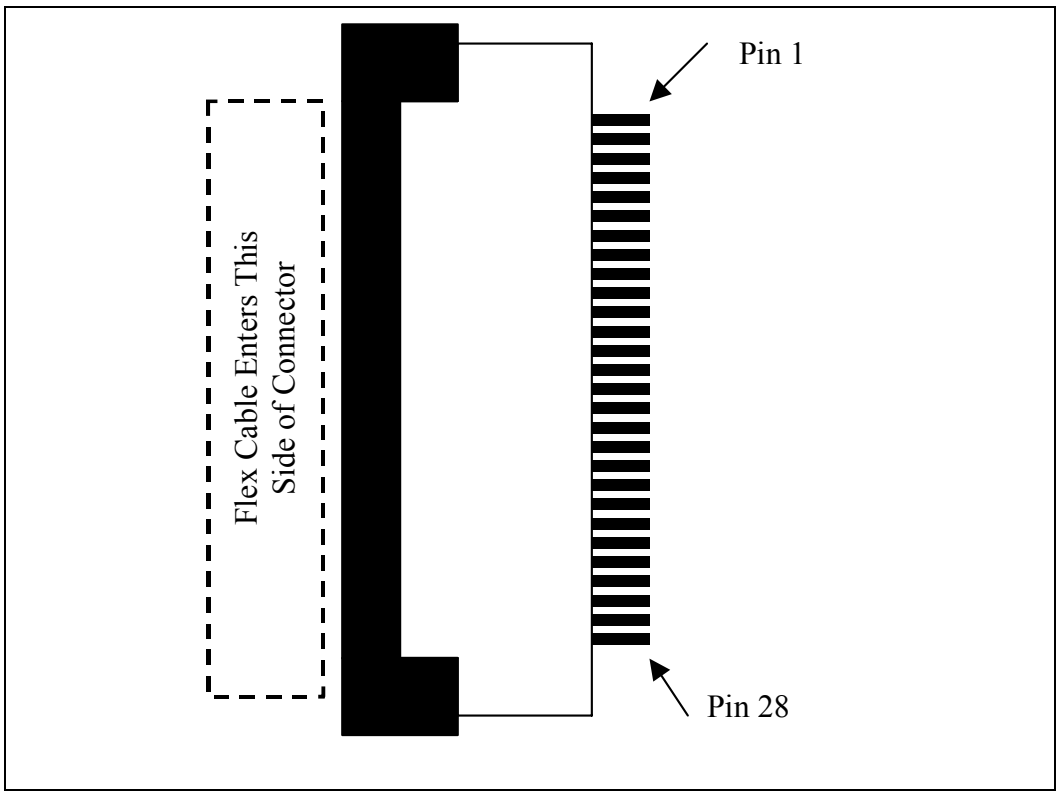


Figure 15. Top View of Surface Mount ITP700 Flex Connector on the Target System



NOTES:
1. Keying of flex cable is the note “This Side Up” on the flex cable.
2. There is no physical keying.

This page is intentionally left blank.

6 Intel® Xeon™ Processor with 512-KB L2 Cache at 2.20, 2.0, and 1.80 GHz DP / Intel® Xeon™ Processor MP Server System Implementation Guidelines

6.1 Termination and Routing Guidelines

The following specifications are for an ITP700 implementation that is terminated according to the content in the Multi-processor ITP debug port Implementation Guidelines chapter of this document adjusted for Intel® Xeon™ processor specific implementation guidelines dictated in section 4.3 of this document. If the system design does not conform to the required terminations exactly, the additional drive specifications listed in the ITP700 DPA Specifications chapter of this document can be used to interpolate specifications at the non-standard operating ranges

All of the termination and routing guidelines defined in Chapter 2 must be adhered to for a multi-processor ITP700 debug port implementation with the following exceptions and clarifications:

Figure 16. BPM[5:0]# Connectivity for Intel® Xeon™ Processor with 512-KB L2 Cache at 2.20, 2.0, and 1.80 GHz DP / Intel® Xeon™ Processor MP Servers

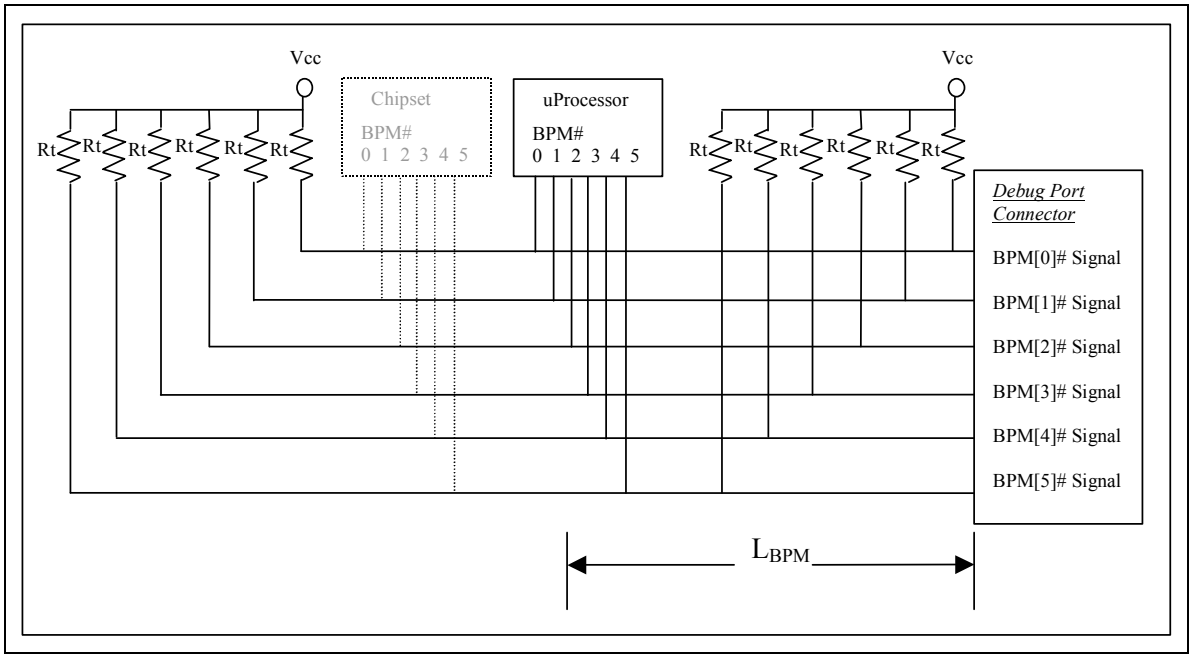


Table 33. BPM[5:0]# Figure Definitions

Parameter	Min	Nominal	Max	Notes
L_{BPM}			1 ns	1

NOTES:
1. BPM[5:0]# must be length matched to within 50 ps of themselves and RESET#.
2. Refer to the Platform Design Guide for BPM parameters between other components.

Clarification 1. The BPM[5:0]# and RESET# traces should be terminated to the processor VCC voltage on both ends of the transmission line, similar to that of the system bus. For systems that require on-die termination of the front-side bus, please note that the Intel Xeon processor with 512-KB L2 cache at 2.20, 2.0, and 1.80 GHz DP and Intel Xeon processor MP server systems do not provide on-die termination of the BPM[5:0]# and RESET# signals. Consult individual chipset documentation to assess if a chipset component should be connected to the BPM[5:0]# , RESET#, or JTAG signals.

Clarification 2. The system clock of the Intel Xeon processor with 512-KB L2 cache at 2.20, 2.0, and 1.80 GHz DP and Intel Xeon processor MP servers reference BCLK[1:0] where BCLK0 is the rising edge for the beginning any transaction and BCLK1 is the falling edge. The ITP uses BCLK[p/n] where BCLKp is the rising edge and BCLKn is the falling edge for the beginning of any transaction. All routing Rules for the BCLK signals do not change.

Note: The BPM[5:0]# routing guidelines has changed. In the past, it was required to have BPM0# and BPM2# tied as well as BPM1# and BPM3# tied together. This is no longer the case. It is now recommended that all BPM[5:0]# signals be straight routed. For all legacy boards, the ITP will still work with the previous routing configuration.

7 Intel® Pentium® 4 Processor / Mobile Intel® Pentium® 4 Processor-M / Intel® Centrino™ Mobile Technology System Implementation Guidelines

7.1 Termination and Routing Guidelines

The following specifications are for an ITP700 implementation that is terminated according to the content in the Uniprocessor ITP Debug Port Implementation Guidelines chapter of this document and adjusted specifically for the Intel® Pentium® 4 processor in the 478-Pin Package, Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process, Intel® Pentium® 4 processor on 90 nm process, and systems based on Intel® Centrino™ mobile technology. If the system design does not conform to the required terminations exactly, the additional drive specifications listed in the Specifications chapter of this document can be used to interpolate specifications at the non-standard operating ranges.

The Pentium 4 processor in the 478 Pin Package, Pentium 4 processor with 512-KB L2 cache on 0.13 micron process, Pentium 4 processor on 90 nm process, and systems based on Intel Centrino mobile technology have identical ITP700 board level implementation requirements. The DC and AC characteristics of the ITP signals, termination requirements and routing guidelines are the identical. Therefore both processor families are discussed within this chapter. It is recommended that systems based on Intel® Centrino™ Mobile Technology implement the ITP700Flex debug port. Implementation details can be found in Chapter 1 and Chapter 5.

All of the termination and routing guidelines defined in Chapter 1 must be adhered to for a uniprocessor ITP700 debug port implementation with the following exceptions and clarifications:

Figure 17 – BPM[5:0]# Connectivity for Intel® Pentium® 4 Processor, Intel® Pentium® 4 Processor-M, and Systems Based on Intel® Centrino™ Mobile Technology

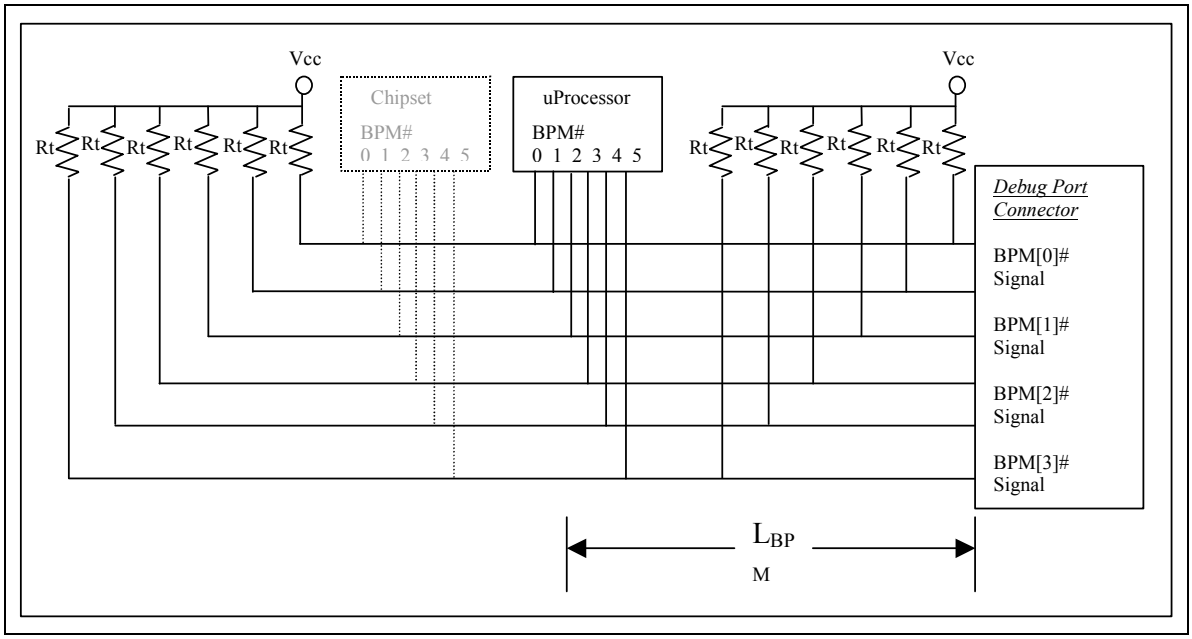


Table 34. BPM[5:0]# Figure Definitions

Parameter	Min	Nominal	Max	Notes
L_{BPM}			1 ns	1

NOTES:
1. BPM[5:0]# must be length matched to within 50 ps of themselves and RESET#.

Exception 1. Additional pins on the Pentium 4 socket support interposer based debug ports. The system bus and TAP port typically cannot provide a stable BCLK(p/n) pair and a method to provide a request for reset to the system reset controller (DBR#). The Pentium 4 socket provides three pins to ease the implementation of an interposer based debug port. One pin is a path for DBR# from the interposer debug port to be routed to the system reset controller. The other pair is a path for a dedicated BCLK(p/n) pair to be routed with the interposer based ITP as the only load. All three pins are isolated from the processor die. It is strongly recommended that a debug port be implemented on the motherboard if it is possible. Ideally a motherboard design will allow for the use of a motherboard based debug port or an interposer based debug port by following the routing requirements for all signals.

In order to support an interposer debug port, The Pentium 4 processor DBR# pin must be connected to the system reset controller with a pull-up to a voltage consistent with the input interface of the reset controller. Systems designed to support both motherboard based as well as interposer based debug ports must connect the motherboard debug port DBR# pin with the processor DBR# pin and the reset controller.

In order to support an interposer debug port, the ITP_BCLK(p/n) pins on the processor socket must have a dedicated clock pair from the system clock source. This clock pair must be routed with the same routing rules as a processor clock. Systems designed to support both motherboard based as well as interposer based debug ports must have two dedicated clock

pairs from the system clock source. One pair is for the motherboard debug port, and the other is for the ITP_BCLK(p/n) pins on the processor socket. The routing guidelines for the motherboard based debug port are defined in Chapter 1. The processor socket ITP_BCLK(p/n) pins have the same routing and termination requirements as a processor clock pair. If an ITP clock pair is to be used for more than one load, all routing requirements for both loads must be met, and simulations must be conducted to ensure that a quality clock is provided at both loads.

Clarification 1. The BPM[5:0]# and RESET# traces should be terminated to the processor VCC voltage on both ends of the transmission line similar to the system bus. For systems that enable on-die termination of the system bus, understand that the Pentium 4 processor does not provide on-die termination of the BPM[5:0]# and RESET# signals. Consult individual chipset documentation to assess if a chipset component should be connected to the BPM[5:0]# , RESET#, or JTAG signals.

Clarification 2. The system clock of the Intel Xeon Processor with 512-KB L2 cache at 2.20, 2.0, and 1.80 GHz DP and Intel Xeon processor MP servers reference BCLK[1:0] where BCLK0 is the rising edge for the beginning any transaction and BCLK1 is the falling edge. The ITP uses BCLK[p/n] where BCLKp is the rising edge and BCLKn is the falling edge for the beginning of any transaction. All routing Rules for the BCLK signals do not change.

Note: The BPM[5:0]# routing has changed. For previous processors, it was recommended to have BPM0# and BPM2# tied as well as BPM1# and BPM3# tied together. This is no longer the case. It is now recommended that each BPM[5:0]# line be routed directly from the processor to the debug port.

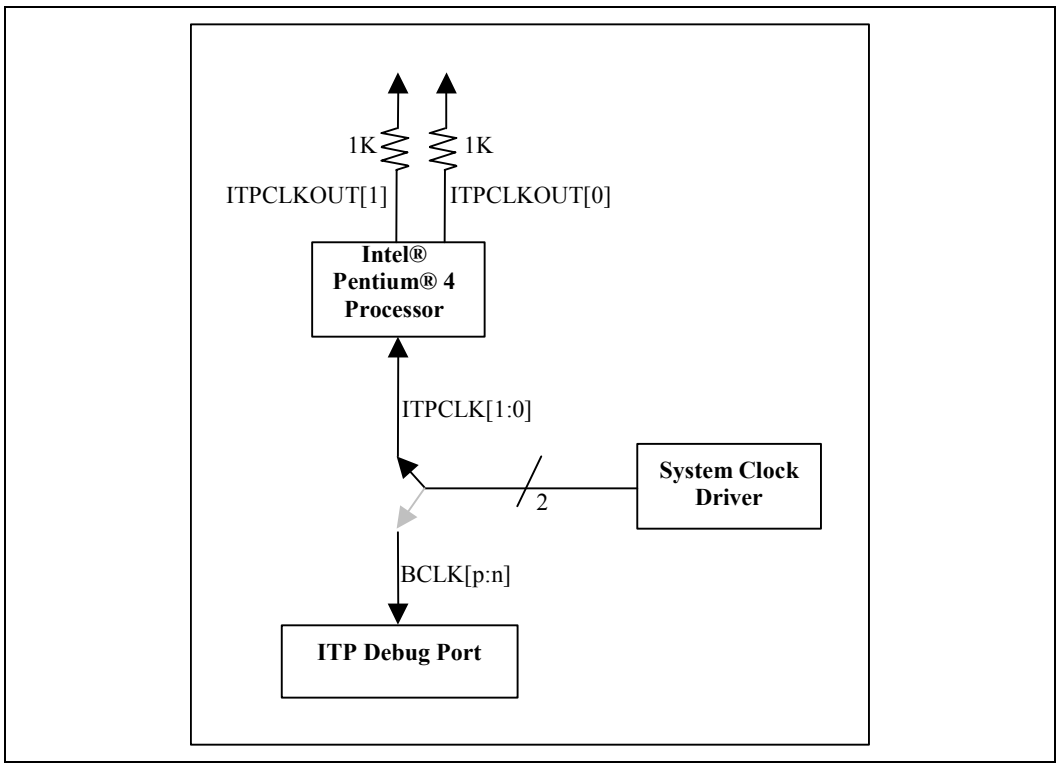
7.1.1 ITP Clock Routing for Intel® Pentium® 4 Processor

These specifications pertain to the ITP clock routing for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. There are essentially two options for providing a clock to the ITP. Option A uses the CK408 clock generator, a choice used in many designs. Option B is only available for B0 silicon or greater, with the new ITPCLKOUT[1:0] pins implemented on the processor. The ITPCLKOUT[1:0] provides a buffered version of BCLK to the ITP. Both routing options as described below will allow for the use of an ITP interposer. ITP interposers are often used in manufacturing test or in place of an on-board ITP.

7.1.1.1 Option A) Using the CK408 Clock Generator

1. Route the BCLK pair from the CK408 to both the ITPCLK[1:0] on the processor and the BCLK[n:p] on the ITP debug port. See Figure below.
2. Terminate ITPCLKOUT[1:0] on the processor (if applicable) with separate1 kΩ pull-up resistors to VCC_CORE.[1]

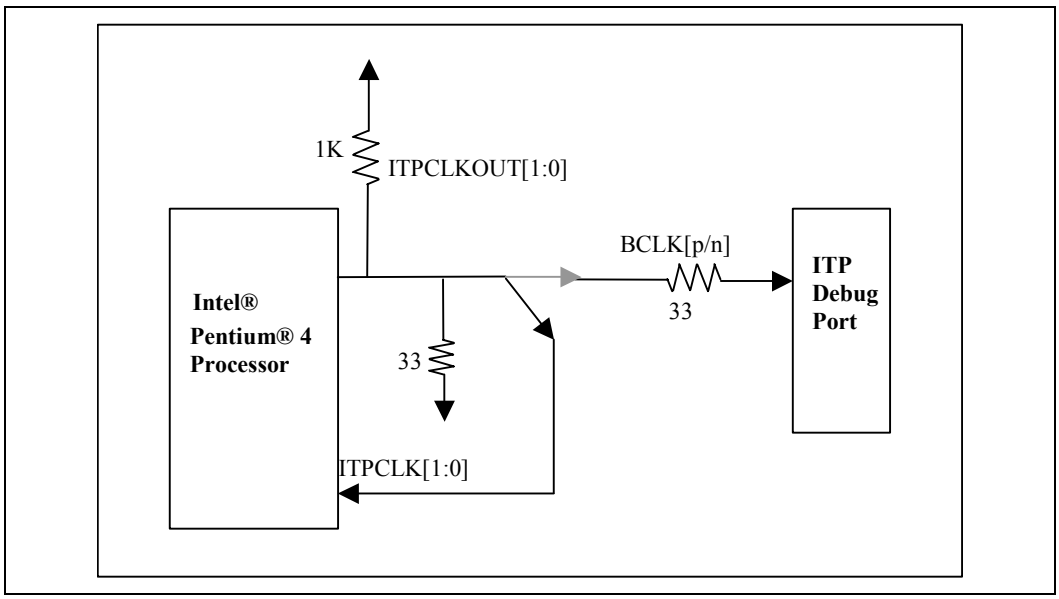
Figure 18 – ITP Clock Routing options using System Clock Driver



7.1.1.2 Option B) Using the ITPCLKOUT[1:0] Pins: (For B0 Silicon or Greater)

1. Route the ITPCLKOUT[1:0] pins directly from the processor to the ITP connector pins BCLK[n:p] using 33 Ω series resistors, 33 Ω pull-down source termination resistors at the processor, and 1 kΩ pull-ups to VCC_CORE.[2]
2. Terminate ITPCLKOUT[1:0] on the processor with separate1 kΩ pull-up resistors to VCC_CORE.[1]
3. When routing the ITP interposer to ITPCLKOUT[1:0] (instead of ITPCLK[1:0]), isolate the ITPCLKOUT[1:0] from connecting to the system to eliminate system board routing stubs. See figure below.

Figure 19 – ITP Clock Routing Options Using ITPCLKOUT[1:0] Pins



NOTES:

1. There was an error in the WW41 Message of the Week (MOW) recommendation. The recommendation stated to use individual matched resistors to terminate ITPCLKOUT[1:0] when these signals are not in use, to provide better immunity to ESD for processor inputs. Since these signals are outputs, a matched (50-60 Ω) or 1 kΩ pull-up resistors this will not affect the ESD. However, using the matched resistors will disable the option of using an ITP interposer. Please use the 1 kΩ pull-up resistors to ensure the option of the ITP interposer solution.
2. For production boards, the 33 Ω pull-down resistor can be left unstuffed. Without the 33 Ω pull-downs, the 1 kΩ pull-ups will effectively disable the ITPCLKOUT[1:0] for power savings and EMI reduction.

This page is intentionally left blank.

8 Intel® Itanium® 2 Processor System Implementation Guidelines

There are three classes of ITP debug tool connections to Intel® Itanium® 2 processor platforms:

- ITP debug port for each processor node for register access and run-time control. A processor node consists of at least one Itanium 2 processor and may contain other TAP devices.
- ITP debug port for each I/O domain for register access and event line monitoring. An I/O domain consists of at least one Itanium 2 processor -based chipset component, no (0) processors, and may contain other TAP devices.
- ITP debug ports for miscellaneous auxiliary scan chains for register access. A miscellaneous debug port may contain TAP devices, but does not contain a processor and does not contain an Itanium 2 processor-based chipset component.

The implementation and routing rules for the I/O domain debug port (class b, above) and the miscellaneous debug port (class c, above) are a subset of the routing rules for processor node debug port. This chapter describes the requirements for implementing a processor node debug port (class a, above). Consult the appropriate chipset DPDG for clarification of requirements for the other two other debug port classes.

8.1 ITP DC and AC Electrical Specifications for Intel® Itanium® 2 Processor Systems

8.1.1 DC Electrical Specifications

The following specifications are for a standard debug port platform implementation using only Itanium 2 processors (and optionally Itanium 2 chipset components). The following specifications also require the debug port platform implementation is designed according to the guidelines found in chapter 1 of this document. If the system design differs from either of these requirements, the additional drive specifications listed in the *Complete Electrical Specifications* chapter of the *ITP700 Debug Port Design Guide* must be used to interpolate appropriate design data for any non-standard operating condition or electrical range.

An explanation of “DPA Type”: existing designs should conform to the ‘ITP700DPA’ DPA Type, for new implementations, Intel recommends all designs conform to the ‘LVDPA’ DPA Type.

Table 35. ITP System Signal DC Characteristics for the Intel® Itanium® 2 Processor

Signal		DPA Type	Min	Max	Unit	Note
FBI	V_{OH}	ITP700DPA	1.00		V	1
		LVDPA	0.9*VTAP	VTAP+0.250	V	1, 9.
	V_{OL}	ITP700DPA		0.40	V	1
		LVDPA	0	0.1*VTAP	V	1
	I_{OH}	ITP700DPA	-5		mA	
		LVDPA	-8		mA	
	I_{OL}	ITP700DPA		5	mA	
		LVDPA		16	mA	
FBO	V_{IH}	ITP700DPA	0.90	1.70	V	
		LVDPA	0.5*VTAP +0.150		V	
	V_{IL}	ITP700DPA	0.00	0.55	V	
		LVDPA		0.5*VTAP - 0.150	V	
	I_{IH}	ITP700DPA	-150		µA	
		LVDPA	-100		µA	
	I_{IL}	ITP700DPA		300	µA	
		LVDPA		100	µA	
PWR	V_{IH}		0.30	2.80	V	2
	V_{IL}			0.10	V	3
	R_{PWR}		2.95	3.05	kΩ	4
BCLK(p/n)	V_{IH}			1.70	V	
	V_{IL}		0.10		V	
	V_{PTP}		300		mV	5
	I_{IH}		-1		mA	
	I_{IL}			300	µA	
	C_{IN}			10	pF	6
DBA#, DBR#	R_{DBX}			6	Ω	7
	I_{DBX}			120	mA	8

NOTES:
1. At maximum output current specified.
2. V_{IH} Max represents the maximum functional voltage of this pin.
3. ITP outputs will be tri-stated when input voltage is sensed low.
4. Resistance from pin to GND.
5. V_{PTP} defined as voltage between both the high and low sides of the signal swing.
6. Including capacitive effects of mated connector.
7. Resistance from pin to GND when active.
8. Maximum sink current of ITP.
9. FBI Voltage tracking for VOH has a lower limit of 1.2 V.

Table 36 - ITP JTAG Signal DC Electrical Characteristics for the Intel® Itanium® 2 Processor

Signal		DPA Type	Min	Typ	Max	Unit	Note
TCK	V_{OH}	ITP700DPA	1.25			V	1
		LVDPA	0.9*VTAP		VTAP + 0.250	V	2
	V_{OL}	ITP700DPA			0.3	V	2
		LVDPA	0		0.1*VTAP	V	2
	I_{OH}	ITP700DPA	-47			mA	
		LVDPA	-60 mA			mA	
	I_{OL}	ITP700DPA			0	mA	
		LVDPA			0	mA	
	Z_{TCK}			20		Ω	3
TMS	V_{OH}	ITP700DPA	1.30			V	4
		LVDPA	0.9*VTAP		VTAP + 0.250	V	4
	V_{OL}	ITP700DPA			0.30	V	4
		LVDPA	0		0.1*VTAP	V	4
	I_{OH}	ITP700DPA	-10			mA	
		LVDPA	-16			mA	
	I_{OL}	ITP700DPA			35	mA	
		LVDPA			36	mA	
	Z_{TMS}			20		Ω	3
TDI	V_{OH}	ITP700DPA	1.3			V	1
		LVDPA				V	5
	V_{OL}	ITP700DPA			0.3	V	1
		LVDPA	0		0.1*VTAP	V	1
	I_{OH}	ITP700DPA	-5			mA	
		LVDPA	0			mA	
	I_{OL}	ITP700DPA			5	mA	
		LVDPA			8	mA	
TRST#	V_{OH}	ITP700DPA	1.3			V	1
		LVDPA	0.9*VTAP		VTAP + 0.250	V	1
	V_{OL}	ITP700DPA			0.3	V	1

Signal		DPA Type	Min	Typ	Max	Unit	Note
TRST# (cont.)		LVDPA	0		0.1*VTAP	V	1
	I_{OH}	ITP700DPA	-5			mA	
		LVDPA	-8			mA	
	I_{OL}	ITP700DPA			5	mA	
		LVDPA			8	mA	
TDO	V_{IH}	ITP700DPA	0.90		1.7	V	
		LVDPA	0.5*VTAP +0.150			V	
	V_{IL}	ITP700DPA	0		0.55	V	
		LVDPA			0.5*VTAP - 0.150	V	
	I_{IH}	ITP700DPA	-150			µA	
		LVDPA	-100			µA	
	I_{IL}	ITP700DPA			300	µA	
		LVDPA			100	µA	

NOTES:
1. At maximum current specified.
2. As measured into a 27 Ω 1% resistor to GND.
3. AC Impedance of the driver.
4. As measured into a 39 Ω 1% resistor to 1.10 V.
5. Open Drain Driver on the LVDPA

Table 37. ITP Execution Signal DC Electrical Characteristics for the Intel® Itanium® 2 Processor

Signal		Min	Max	Unit	Note
BPM5DR#	I_{OL}		120	mA	1
	R_{OL}		18	Ω	2
	C_{IN}		4	pF	3
BPM[5:0]#, RESET#	V_{IH}	PWR + 0.15	3.00	V	4, 5
	V_{IL}		PWR - 0.15	V	4, 5
	I_{IH}	-150		µA	
	I_{IL}		300	µA	
	C_{IN}		3	pF	3

NOTES:
1. Maximum sink current of the ITP.
2. Series resistance to GND when output is low.
3. Includes capacitive effects of mated connector.
4. Over valid range of VIH of PWR.
5. For Itanium 2 processor-based scan chains, PWR of the ITP debug port must be pulled up to 1.2 V through a 1.8 kΩ 1% tolerance resistor

8.1.2 AC Electrical Specifications

Table 38 - ITP System Signal AC Electrical Characteristics for the Intel® Itanium® 2 Processor

Signal	Parameter	Min	Max	Unit	Note
PWR	PWR V_{IL} Max to Tristate	150		µs	
FBI	Rise Time	0.5	2	ns	1, 2, 3
	Fall Time	0.5	2	ns	1, 2, 3
	Skew	-9	-6	ns	4
DBA#	DBA#↓ to first TCK↑	75		ns	5
	DBA#↑ to last TCK↓		100	ns	6
DBR#	DBR# Assertion Period	150		µs	

NOTES:
1. Measured from 20% to 80% of transition.
2. Measured into a load to GND of 220 Ω and 10 pF.
3. FBI has the same period; time High, and time Low specifications as TCK.
4. With respect to same edge on TCK.
5. Measured from assertion of DBA# to 50% of first TCK transition.
6. Measured from release of DBA# to 50% of last TCK transition.

Table 39 - ITP JTAG Signal AC Electrical Characteristics for the Intel® Itanium® 2 Processor

Signal	Parameter	Min	Max	Unit	Note
TDO	Setup	5		ns	1
	Hold	0.5		ns	1
	Rise/Fall Time		15	ns	2
TCK	Rise/Fall Time	9	13	ns	2, 3
	Period	58		ns	4
	Time High	25		ns	5
	Time Low	25		ns	5
TMS	Rise/Fall Time	7	16	ns	2, 6
	Clock to Out	-5	0	ns	7
TDI	Rise Time	0.5	2.0	ns	2, 8
	Fall Time	0.5	2.0	ns	2, 8
	Clock to Out	-8	0	ns	7
TRST#	Assert Time	300		ns	

NOTES:
1. With respect to rising edge of FBO at the debug port using 50% of transition for both signals.
2. Measured from 20% to 80% of transition.
3. As measured into a 27 Ω and 35pF load to GND.
4. Measured from 50% of rising edge to 50% of next rising edge. This specification is valid for asynchronous and synchronous operation.

5. Measured from 50% of first edge to 50% of second edge.
6. As measured into a 39 Ω load to VTAP and 35 pF to GND.
7. With respect to falling edge of TCK at the debug port using 50% of transition for both signals.
8. As measured into a 1500 Ω load to VTAP and 10 pF to GND.

Table 40. ITP Execution Signal AC Electrical Characteristics for the Intel® Itanium® 2 Processor

Signal	Parameter	Min	Max	Unit	Note
BPM[5:0]#, RESET	Setup	400		ps	1
	Hold	200		ps	1
BCLK(p/n)	Rise Time		5	ns	2
	Fall Time		5	ns	2
	Period	5	15	ns	3
	Time High	2.2		ns	
	Time Low	2.2		ns	
BPM5DR#	Rise Time	1	4	ns	2, 4
	Fall Time	8	15	ns	2, 4

NOTES:
1. With respect to BCLK(p/n).
2. Measured from 20% to 80% of transition.
3. Specification for valid synchronous operation of the ITP. Asynchronous operation has no Max specification but shares the Min specification listed.
4. Measured into a load to 1.5 V of 50 Ω and 35 pF to GND.

8.2 ITP Signal Layout Guidelines

- The physical placement of the debug port is critical for the correct implementation of all processor node debug ports.
- The debug port should be treated as a part of the processor group with respect to the BPM[5:0]# and RESET# signals. The debug port must be located within 1.0ns (electrical length) of the BPM[5:0]# and RESET# pins and all next-nearest system bus agent(s). Note that the <1.0 ns requirement applies only to the BPM[5:0]# and RESET# trace segments between the debug port and the nearest system bus agent.
- All other system bus trace segments must be routed according to the guidelines located in the Platform Design Guides.
- The physical placement of I/O domain debug port and the miscellaneous debug port is determined by the routing rules for TCK.
- All receivers of the TCK signal (implemented in a star topology) must be within 2 ns flight time from the debug port.

8.2.1 System Signal Layout Guidelines

The following are additions to the *ITP700 Debug Port Design Guide*'s System Signal Layout Guidelines.

BCLK(p/n)	In addition to the generic MP guidelines in this guide, the BCLK for I/O domain debug ports should be routed with the same length as the clocks to the Intel® Itanium® 2 processor chipset components within that domain. BCLK routing rules for miscellaneous debug ports depend on the use of the debug port. If synchronous recovery of information routed to BPM signals is required, the timing relationship of that interface will determine BCLK routing rules.
FBO	The routing rules for FBO for I/O domain debug ports and miscellaneous debug ports are determined by solving the timing analysis for TDO recovery from the last load of the scan chain.
DBR#	It is possible that the DBR# pin can be used to reset only a portion of the target system (e.g. only one processor node), but some method must be provided for the ITP to reset the entire target system through assertions of one or more DBR# pins.

8.2.2 JTAG Signal Layout Guidelines

In order for the standard I/O Domain debug port and the standard miscellaneous debug port to actively communicate with the PXB, SCSI, or similar components, the scan chain must be (voltage) translated from the ITP drive levels to 3.3V (i.e., PXB drive level). This translation is not a trivial design task. There are several signal integrity and scan chain continuity issues that must be understood. Translation of the JTAG signals from the ITP drive levels to a higher (or lower) voltage can be completed through a voltage translator circuit as long as the debug port signal FBI is used as the source of the TAP clock for this scan chain.

Note: TCK from the ITP has a rise and fall time of around 10ns. If TCK is used as the source of the clock for the translation circuit, the input signal may sweep through the transition point of the translator input slow enough to create metastable edges on the output of the translator. These extra transitions on TCK will render the scan chain inoperative for all devices.

The rise time of the TAP clock edges on the output of the translator should be accounted for in the design. Quick rise and fall times on traces that are not properly terminated may result in glitches on the rising or falling edges of the signal at the receiver. These glitches will render the debug port inoperative. For ITP operations, reserve individual buffers within the translation device for each TAP clock (FBI) and possibly TMS for each load in the scan chain to reduce the possibility of TAP clock signal integrity issues at each load.

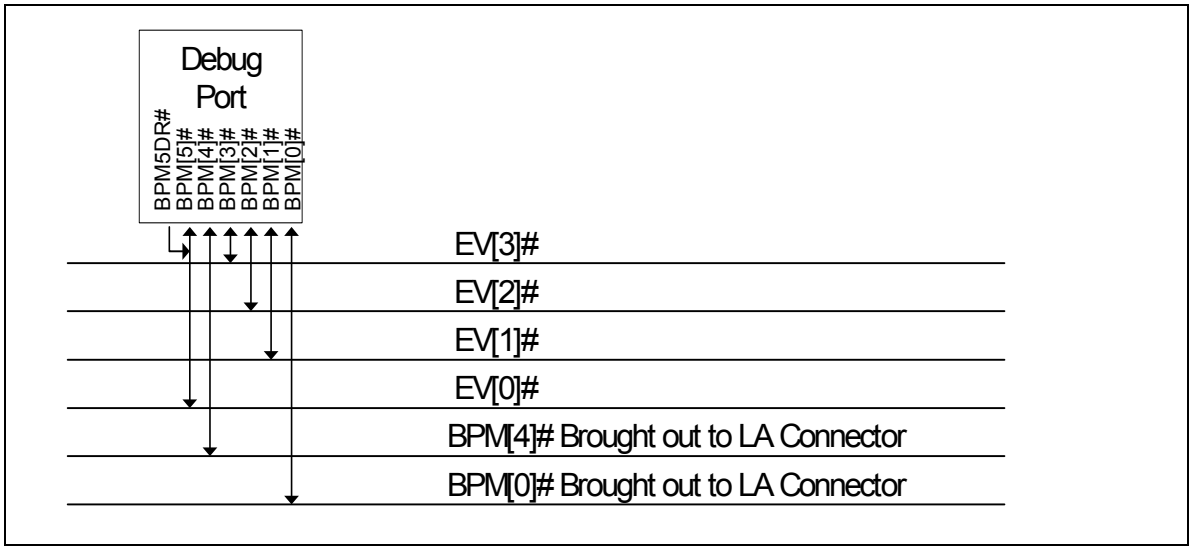
The maximum operating frequency of the scan chain may need to be reduced when a translation device is placed within the scan chain. Therefore it is recommended to provide a method to bypass the translated portion of the scan chain to increase the performance of the non-bypassed portion of the scan chain. When a portion of the scan chain is bypassed, the output enable of the voltage translator should be held inactive to prohibit bypassed chipset components from acting on debug port signals intended for the non-translated portion of the scan chain.

8.2.3 BPM Connectivity for I/O Domain Debug Ports

The Itanium 2 processor-based chipset has the capability to attach an ITP to the chipset components within each IO Domain to provide debug hooks to the IO subsystem and Scalability Port Switch components. IO Domain debug ports must follow the following guidelines:

- For single-domain systems, all SNCs, SPSs and IOHs should be connected to a single wired-OR EV[3:0]# bus. This will support inter-device communication for performance and debugging operations.
- For dual-domain systems, each SNC and IOH is gated by a bus coupler onto either a domain 0 or domain 1 wired-OR EV[3:0]# bus. Control of the bus couplers is normally driven by the GPIO outputs from an SPS with the system configuration mode set to "connect" each device to a bus. This allows the devices to be configured into a single common bus or into a bus for each domain. Note that every SPS should be wired to the domain 0 EV[3:0]# bus, since only the first domain for events is supported.
- An ITP debug port should be installed in each partitioned domain of the IO subsystem to drive the local JTAG scan chain, sense the EV[3:0]# signals and possibly drive the EV[0]# signal. BPM[4,0]# are not used, and must be routed to the "Common" Logic Analyzer Connector as defined in the applicable *Platform Design Guide*.

Figure 20. Intel® Itanium® 2 IO Domain BPM Connectivity



8.3 Intel® Itanium® 2 Processor Routing Guidelines

All of the termination and routing guidelines defined in the multiprocessor chapter of the ITP700 Debug Port Design Guide (found on developer.intel.com) must be adhered to for an ITP700 debug port implementation with an Itanium 2 processor-based platform with the following clarifications:

Clarification 1. The BPM[5:0]# and RESET# traces should be terminated to the system bus termination voltage of 1.2V on both ends of the transmission line. For platforms that make use of on-die termination of the front side bus on processor and Itanium 2 processor-based chipset components, please note that the Itanium 2 processors, and Itanium 2 processor-based chipset components do not provide on-die termination for these signals.

Clarification 2. Itanium 2 processor were designed to support a 1.5 V pull-up voltage for the JTAG signals. Simulations have shown that these processor inputs will function correctly with a VTP pull-up of 1.2 V, but the system will have additional noise margin if the VTAP voltage is 1.5 V.

Clarification 3. For Itanium 2 processor-based scan chains, PWR of the ITP debug port must be pulled up to 1.2 V through a 1.8 kΩ 1% tolerance resistor.

This page is intentionally left blank.

9 Intel® E8870 Chipset System Implementation Guidelines

This chapter describes the I/O domain and the miscellaneous auxiliary scan chain debug port implementation specific to systems utilizing the E8870 chipset. As such, system designers should first familiarize themselves with the general implementation, routing, and termination rules as defined in the Intel® Itanium® 2 Processor System Implementation Guidelines chapter of this document. The I/O domain debug port is noted as a 'class b' ITP debug tool connection; the miscellaneous auxiliary scan chain is noted as a 'class c' ITP debug tool connection.

9.1 The I/O Domain Debug Port Guidelines

The recommended implementation is to have one debug port for each I/O domain. If a system does not support dual domains, then there will normally be only one debug port in the I/O system. For dual-domain systems, there will normally be two debug ports, one for each domain. Some of the debug port signals are optional. They may require use or may be left unconnected, depending on platform architecture.

For either of these configurations, more than the minimum number of debug ports described above may need to be implemented if signal integrity of the JTAG scan chains (particularly TCK) cannot be met. This could occur if the platform partitions devices across several boards such that TCK cannot be driven by the minimum number of debug ports and still provide clean clocks across the board interfaces. Additional debug ports would be required to drive additional independent scan chains in such cases.

Care must be taken to ensure that all JTAG signals of scan chains driven by each debug port are used together for a set of devices. In particular, the TCK, TMS, TRST#, and TDI/TDO chains of one debug port cannot be mixed with signals from another debug port. This is because each debug port operates independently of the others.

Intel® E8870 chipset components were designed to support a 1.5 V pull-up voltage for the JTAG signals. Simulations have shown that these processor inputs will function correctly with a VTP pull-up of 1.2 V, but the system will have additional noise margin if the VTAP voltage is 1.5 V.

Some of the debug port signals are optional. They may require use or may be left unconnected, depending on platform architecture. In particular:

- The DBA# signal will only be necessary if the target system requires selection between alternate sources for control of the JTAG scan chains.
- The DBR# signal will only be necessary if there is a need to independently assert a local reset to that sub-section of the system. Note that at least one DBR# should be implemented from some debug port so that the ITP host can force a hardware reset of the platform.
- The FBI signal will only be necessary if there is a need to drive TCK via clock buffers to devices in the local scan chain. TCK for the scan chain would normally be driven directly by the debug port TCK output.

- The RESET# will only be necessary where a reset, unique and independent from the processor node debug port, is required for devices in the I/O domain.

Note: Timing of debug port TAP signals (to and from the components) must be verified to meet the setup and hold times after component timing, debug port timing, trace delays, and any intermediate buffers are considered. Since the Event Bus signals are asynchronous, there is no requirement to control BCLKP/BCLKN delays from clock source to debug port (as there are for the Processor Node debug port). Please consult the appropriate *Platform Design Guide* for connectivity and termination requirements for Event Bus signals.

9.2 The Miscellaneous Debug Port Guidelines

Some of the debug port signals are optional. They may require use or may be left unconnected, depending on platform architecture. In particular:

- The DBA# signal will only be necessary if the target system requires selection between alternate sources for control of the JTAG scan chains.
- The DBR# signal will only be necessary if there is a need to independently assert a local reset to that sub-section of the system. Note that at least one DBR# should be implemented from some debug port so that the ITP host can force a hardware reset of the platform.
- The FBI signal will only be necessary if there is a need to drive TCK via clock buffers to devices in the local scan chain. TCK for the scan chain would normally be driven directly by the debug port TCK output.
- The RESET# will only be necessary where a reset, unique and independent from the processor node debug port, is required for devices on the miscellaneous debug port.
- The debug port BPM inputs/drive can be used to sense signals of various functionality, as long as the signaling requirements for the ITP (as defined in the RS--Intel 870 Electrical, Mechanical and Thermal Specification) are met.

10 Appendix A – Alternate Bypass Methods

Sections 1.5.2 and 2.5.2 of the attached document describes the recommended bypass method for the ITP scan chain using a four-pin header. The four-pin header is preferred due to the characteristic it has of completely removing the TDO pin from the TDI/TDO path to the next scan chain agent. There are other methods possible for completely bypassing populated scan chain agents. Figure 21 describes a method of completely bypassing the last agent of a scan chain using a three-pin header. Note that this method would require 75 Ω pull ups to VTAP on the TDO pins of both P0 and P1. Figure 22 illustrates a method of completely bypassing two agents using a three-pin header and a pair of two-pin headers.

Figure 21. Complete Bypass of One Out of Two Agents

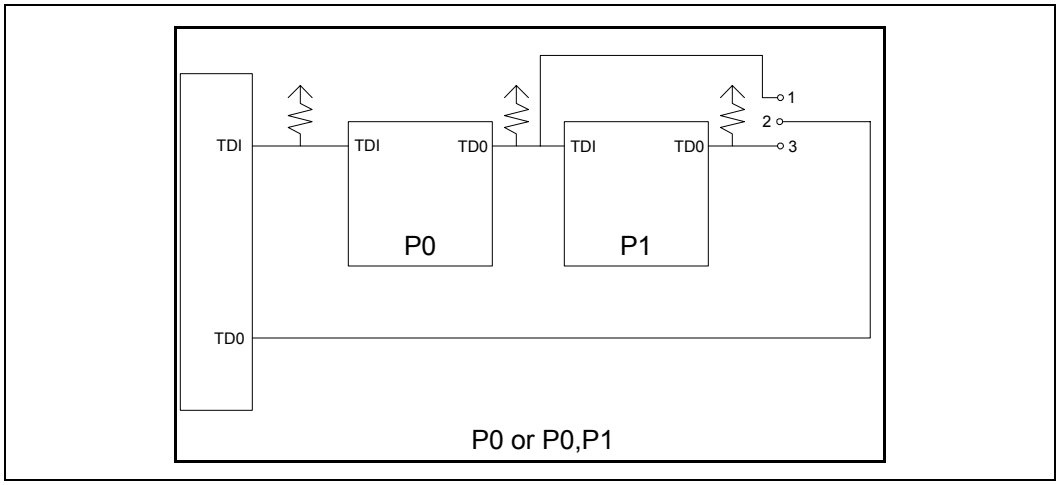
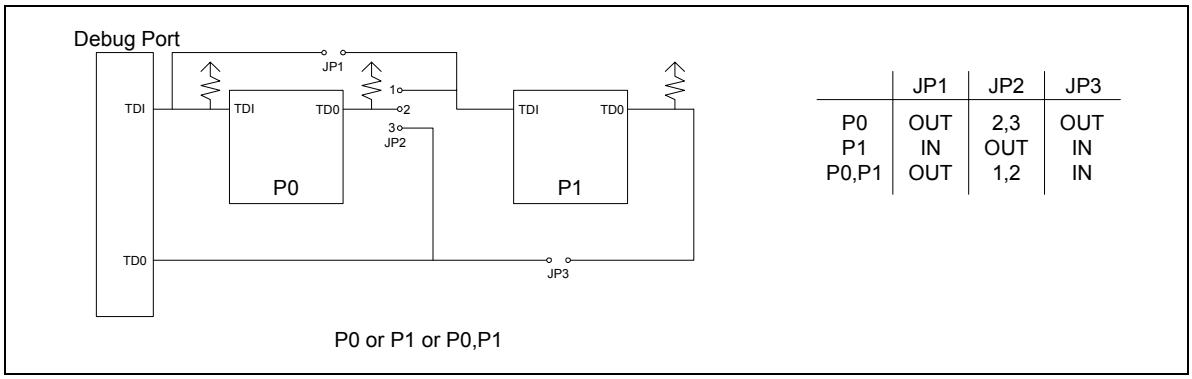


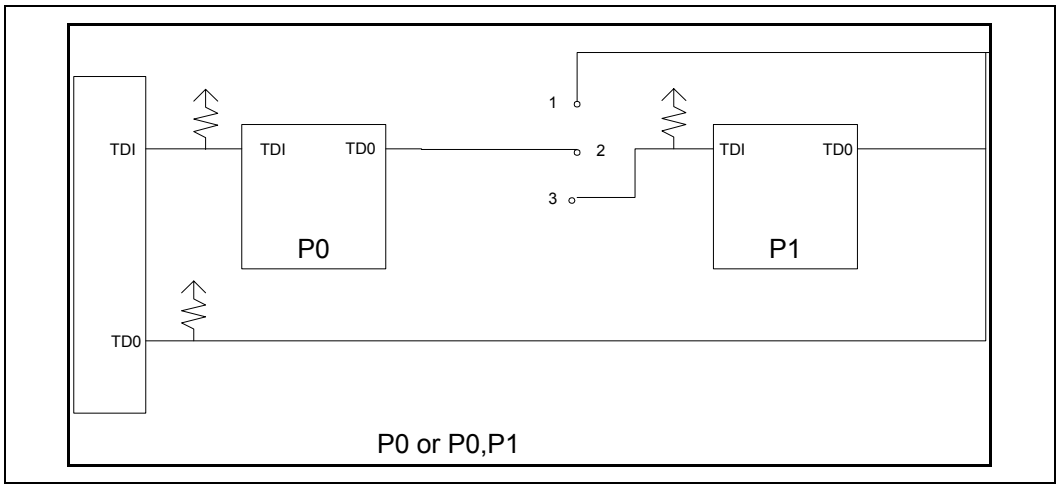
Figure 22. Complete Bypass of Two Agents with Three Headers



	JP1	JP2	JP3
P0	OUT	2,3	OUT
P1	IN	OUT	IN
P0,P1	OUT	1,2	IN

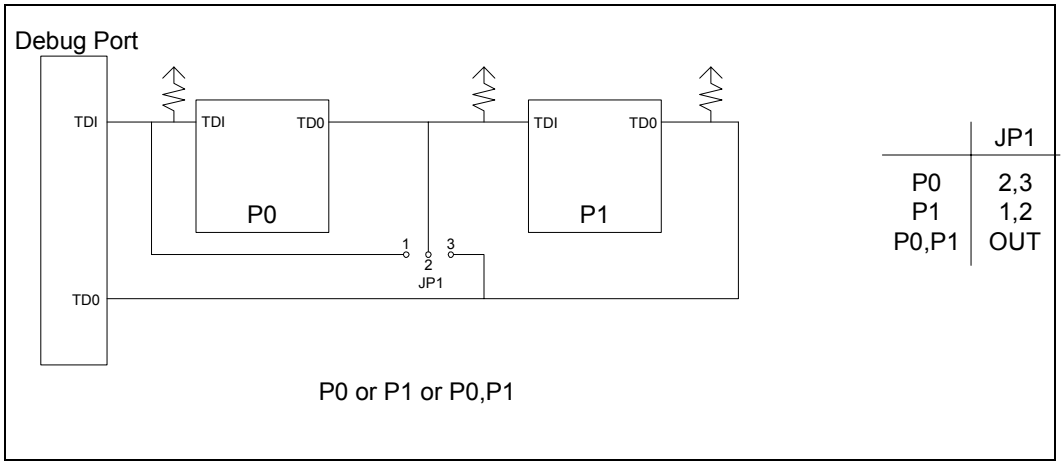
If the customer is sure that bypassed agents in the scan chain will always be depopulated, a three-pin header bypass scheme will be adequate. As long as the bypassed agent is not on the system board, there is no possibility of double-driving the net. Figure 23 illustrates a possible three-pin bypass configuration. Note that when pins one and two are connected, TDO of P0 and TDO of the ITP are connected. It is assumed that the TDO driver of P1 will not be present on this TDO net.

Figure 23. Three-pin Bypass Option



When developing bypass jumper architectures, pay close attention to how many pull-ups are connected to a TDI/TDO net under all bypass conditions. Figure 24 shows a bypass jumper configuration that will lead to two pull-ups on a TDI/TDO net.

Figure 24. Illegal Bypass Configuration



NOTE: Note that dual pull-ups will be seen in bypass conditions. Resistance values will need to be scaled to ensure that no less than 150 Ω is seen by ITP TDI and no less than 75 Ω is seen by ITP TDO.

Quickswitches can be used to replace bypass jumpers/headers if the circuit is well designed. Many quickswitch packages contain a low resistance (~7- Ω), low capacitance (~5 pF) analog bypass switch (FET). Both the jumpers and the quickswitches designs add capacitance and resistance to the TDI/TDO line for each device bypassed. RC delay can slow down the rise time significantly when multiple devices are being bypassed. Careless design in this area can easily cause severe scan frequency degradation or, even worse, scan data corruption. Using quickswitch designs allow the system designer to actively remove agents from the scan chain by using processor present signals as enable lines for the quickswitch. The designer must be careful to ensure that there are no power-up conditions that will corrupt the configuration of the scan chain and therefore render this primary debug tool inoperative.

This page is intentionally left blank.

11 Appendix B – Buffering TCK

While Intel strongly recommends implementing TCK for the scan chain using TCK and a matched star topology, there are situations that require buffers to be placed in the TCK path. Assure that the buffers chosen to drive TCK will be able to operate in the voltage range appropriate to the target TAP interfaces. There have been several successful buffer implementations using a 74VCX style part such as a 74VCX 244. Manufacturer's datasheets indicates this device will operate down to 1.65 V and will drive both high and low sides of the signal swing. GTL drivers will not work for TCK buffers due to the fact that the TCK should be pulled-down to guarantee an idle low. Be mindful of the edge rates of the outputs of the chosen buffer. Some TAP agents will be damaged due to overshoot of high edge rate un-terminated signals.

FBI is provided on the debug port specifically as a source clock for a TCK buffer. FBI is essentially the same signal as TCK on the debug port, but without the passive edge rate filtering present on TCK. FBI must be lightly loaded. It is recommended that a single buffer be used for each scan agent in the chain. If an extra buffer is available in the package, route FBI to this buffer to create a spare copy of TCK to be used for FBO feedback. This net should be routed to FBO with an electrical length equal to the matched length of the scan chain TCK nets plus the electrical length of the BPM[5:0]# and RESET# signals from the nearest system bus agent to back to the debug port.

It is important to verify timing analysis of the scan chain to ensure that there is adequate setup and hold margins on TMS, TDI, and TDO for each scan chain agent as well as the debug port. It might be necessary to route TMS through the buffer in order to guarantee timings for the scan chain.

This page is intentionally left blank.

12 Appendix C – Recovering a Single-Ended BCLK

The ITP uses a differential ECL receiver to recover the system BCLK. It is possible to modify the target system hardware to accept a single-ended system clock. This is accomplished through the creation of a stable reference voltage on the target system. This voltage should equal to the center of the swing of BCLKn as seen at the debug port. Use relatively low resistance values (such as 200 Ω or less) between the BCLK high-side drive voltage and GND. This will ensure that any current draw seen on the BCLK pins due to the differential termination of the ITP hardware will not cause the reference to drift. Include a .01 µF ceramic capacitor to the reference voltage at the debug port (pin 21) to help keep the voltage reference stable. Note that the required swing of a single-ended BCLK is effectively double the required swing of the differential clock because of the nature of a static negative differential reference.

This page is intentionally left blank.

13 Appendix D – Arbitration of the Scan Chain With a Local TAP Master

The basic handshaking mechanism is predicated on the notion that when an alternate local TAP master has requested access to the target system, the debug tool will behave as though it has been unplugged. This suggests that when control is regained, the debug tool must regain the state information needed to operate properly.

The protocol is as follows:

1. The ITP de-asserts the DBA# signal when the current task is complete. The ITP however maintains control of the target system.
2. The local TAP master seeing DBA de-asserted activates an open drain control gate on the ITP PWR pin, thereby pulling PWR low at the ITP.
3. The ITP isolates all signals connected to the target system.
4. The local TAP master is free to perform any actions with the scan chain it requires. When finished the local TAP master must release PWR to allow the debug port to regain control of the scan chain.
5. The ITP seeing PWR asserted, assesses the RESET# state, BCLK(p,n) state, and then re-configures the target to properly use the BPM[5:0]# signals as indicated.
6. The ITP asserts DBA# to regain control of the target and reset the TAP agents prior to performing the next task.

This page is intentionally left blank.

14 Appendix E – Designer's Checklist for Schematic and Layout Reviews

The following tables serve as a guide for a designer to review a generic ITP700 debug port implementation in detail. These guidelines are in no means comprehensive nor serve to replace the recommended design guidelines in this document.

Table 41. Part 1: BPM[5:0]#BCLK(p/n) DBR# and RESET# Connectivity

Pas	FAIL	Don't Care	ISSUE
			RESET# should be connected to the debug port (DP) pin15 and all front side bus agents in a processor scan chain. I/O subspace scan chains may connect to a suitable RESET# signal, but this connection is not required.
			If RESET# is not used, proper pull-up is in place. This is required for ITP S/W functionality.
			BPM[5:0]# (DP pins 13, 11, 9, 7, 5, and 3 respectively) should be connected to the BPM or other event signals according to best known methods.
			BPM5DR# must be connected to BPM5# at the DP (pins 23 and 13 respectively).
			No other loads in a CPU Node ITP implementation are connected to the BPM[5:0]# and RESET# traces other than processor, chipset, or DP loads.
			DBR# is connected to an appropriate position in the reset generation logic. Note that a DBR# reset should not result in any power sequencing on the target system.
			BCLK(p/n) polarity is correct. (BCLKp rising edge is a BCLK assertion)

Table 42. Part 2: TDI/TDO Connectivity

PASS	FAIL	Don't Care	ISSUE
			Is the connectivity of TDI/TDO around the scan chain correct?

Table 43. TDI/TDO Connectivity Through Bypass Circuitry

PASS	FAIL	Don't Care	ISSUE
			If FETs are used for bypass, is there a risk of capacitive effects on timing budgets?
			If FETs are used for bypass, is there a risk of signal leakage through the body diode of the FET?
			If QuickSwitches are used for bypass, is there any risk of signal corruption near the VCC and GND rails of the QuickSwitch that might affect noise margins?
			Will the Bypass Method completely remove a scan agent from the scan chain? (Please note that this may not be a requirement for all systems.
			Is there any chance of dual pull-ups on a TDI/TDO path due to bypass logic?
			Is there any chance of NO pull-ups on a TDI/TDO path due to bypass logic?

Table 44. Part 3: TCK / TMS Implementation

PASS	FAIL	Don't' Care	ISSUE
			Is there a single pull-down on TCK?
			Is there a single pull-up on TMS?
			If any extra locations for on-board filtering of TCK or TMS are in the schematic, they must listed as Do Not Stuff.
			Hysterisis should be implemented for all receivers of TCK
			TCK should be routed to FBO for un-buffered implementations.

Table 45. Buffered TCK / TMS Implementation Issues

PASS	FAIL	Don't' Care	ISSUE
			FBI must be used as the clock input for the buffer.
			Is there an individual buffer for each TCK Load?
			If there is an extra buffer in the package, FBO should be driven from that spare buffer. Otherwise, FBO should be connected to an output of the TCK buffer.
			Can TMS be recovered at each scan chain agent given the delay of TCK through a buffer?
			Does the buffer support the drive currents and voltage regions to drive into the pull-up on the TCK/TMS lines and match the input characteristics of the scan chain loads?
			Are TCK and TMS signals pulled LOW and High respectively through a bias resistor to set the idle condition of the traces seen by the scan chain agents?

Table 46. Part 4: Pull-Up / Pull Downs

PASS	FAIL	N/A	Signal	Pin Number	Pull Up / Pull Down Resistance	Pull Up / Pull Down Voltage
			PWR	22	1.5 kΩ 1% for 2/3rds recovery.	VTT of BPM[5:0]# and RESET#
			BCLK(p/n)	19, 21	See Processor Datasheet	See Processor Datasheet
			DBA#	4	150 – 240 Ω	VCC
			DBR#	6	150 – 240 Ω	VCC
			FBI	18	220 Ω	GND
			FBO	17		
			TCK	16	27 Ω 1%	GND
			TMS	12	39 Ω 1%	VTAP
			TDI	10	150 Ω	VTAP
			TDO	24	75 Ω	VTAP
			TRST#	14	500 – 680 Ω	GND
			BPM[5:0]#	13, 11, 9, 7, 5, 3,	See Processor Datasheet	VTT
			RESET#	15	See Processor Datasheet	VTT
			BPM5DR#	23	Shorted at debug port	BPM[5]#

PASS	FAIL	Don't Care	ISSUE
			Are the Resistance Values and Termination Voltages Listed in the table above adhered to?
			No bypass condition should allow the Pull-up resistance on TDI to be less than 150 Ω.

Part 5 – Layout Issues

Below is a list of basic rules to keep in mind when routing the schematics. These guidelines are in no means comprehensive or serve to replace the recommended layout guidelines in this document.

1. BPM[5:0]# should be routed in matched lengths as full speed Front Side Bus signals. There should be only two terminations on the trace. One should be a passive resistor located just beyond the debug port, and the other a passive resistor located just beyond the last agent on the FSB. Note the flight time of the BPM signals from the closest processor agent on the Front Side Bus to the debug port. This value will be important later. (Tbpm)
2. BCLK (n,p) should be routed with the same matched length as the clock to the rest of the processor/chipset agents but with an additional flight time equal to the BPM signals flight time from the closest processor agent on the front side bus to the debug port (Tbpm). Routing in this manner will place you close to the optimal recovery point of the BPM#s using BCLK and its added length. Fine adjustment may be necessary to place BPM# edges in the center of the ITP Setup and Hold window (400 ps and 500 ps, respectively)
3. TCK should be routed in a star topology from the debug port (or buffer) with matching lengths to each agent in the scan chain. The FBO feedback from the source of the scan chain TCK(or FBI) to the ITP should have a flight time equal to the matched TCK paths plus the flight time of the BPM signals from the closest processor agent on the Front Side Bus to the debug port (Tbpm). If a buffer is used in the creation of TCK, it is recommended that FBO be routed from an extra buffer to the FBO pin with a flight time calculated in the same method as listed above.
4. TMS, like TCK, should also be routed in a star topology from the debug port with matching lengths to each agent in the scan chain. Ideally these traces will be the same length as those of TCK to each agent in the scan chain.

15 Appendix F – ITP700 DPA Spice Models

Intel has a behavioral spice model of the ITP hardware available for simulation of critical routes and topography. Intel strongly recommends that these models be used to simulate at the very least, TCK, BCLK and Execution signal integrity and timing.

The models are created and packaged as single signal models. Each model contains a representation of all passive components on the ITP hardware between the debug port pins to the driver or receiver pin on the ITP (Including a model of the mated debug port Header). The heading of each model documents the input and output path of the circuit and where the model of the driver or receiver is to be located for a full simulation. It is not legal for Intel to package spice models of the actual driver or receiver component with the ITP spice models. The companies that produce these components will have to be contacted directly to obtain these models. A spice model for the VCX16374 is available from Toshiba. A spice model for the QS3125 is available from Quality Semiconductor. Spice models for MC100LVEL17 are available from Motorola. See Motorola Application Note AN1560 for further information on how to use these models.

The ITP models were originally created in VBASE*, a Mentor Graphics analog simulation language. The models are fully compatible with P-SPICE and H_SPICE. Any issues with VBASE may be directed to Mentor Graphics for assistance. The following is a list of models that are available for the ITP hardware.

Drive Pins:

```
************************************************
        * TCKDR
* TCK DRIVE MODEL LEVEL 1
* UPDATED: NOVEMBER 18, 1998
* EXPANDED DOCUMENTATION: AUGUST 18, 2000
*
* PINS:
*    GNDREF=GROUND
*    DRV=DRIVE FROM SEVEN VCX OUTPUTS,
*    M2=MINITEK* CONNECTOR AT TARGET
*
* ADDITIONAL REQUIRED SUBCIRCUITS INCLUDED IN PACKAGES.TXT:
*    QSOP = QSOP PIN MODEL, PACKAGE APPROXIMATION
```

```
*     MINITEK* = ITP DPA HEADER MODEL
*
* ADDITIONAL MODELS THAT MAY BE ADDED:
*     VCX16374 = TOSHIBA* VCX BUFFER/DRIVER
*     qs3vh125 = QUALITY SEMICONDUCTOR* QUICKSWITCH
*
************************************************
.SUBCKT TCKDR GNDREF DRV M2
* Declare VCX (Created on DPI/DPA)
VINIT1 VCX GNDREF DC 1.65
* Load Elements
L2 DRV M1 100Nh
C13 M1 TCKN1 100pF
R16 TCKN1 GNDREF 10
R13 M1 EVCCQS 17.4
*
* The following is a generalization of the qs3vh125.
* A true spice model of the quickswitch may be
* added between pins VCX and EVCCQS.
* Be sure to remove the following generalization
* if the true spice model is used.
************************************************
* Path from VCX to EVCCQS through quickswitch
* QSOP Pin Model
X1 EVCCQS INT1 GNDREF QSOP
* Quickswitch Internal Resistance
RQS INT1 INT2 4
* QSOP Pin Model
```

X2 VCX INT2 GNDREF QSOP

****

* Setup Minitek* connector nodes

* MINITEK* PAD CAPACITANCE

CMT1 M1 GNDREF 5.00E-13

CMT2 M2 GNDREF 5.00E-13

* Tie all other Minitek* Model Pins to Ground

RMT2 M3 GNDREF 250

RMT3 M4 GNDREF 250

RMT4 M5 GNDREF 250

RMT5 M6 GNDREF 250

RMT6 M7 GNDREF 250

RMT7 M8 GNDREF 250

RMT8 M9 GNDREF 250

RMT9 M10 GNDREF 250

RMT10 M11 GNDREF 250

RMT11 M12 GNDREF 250

RMT12 M13 GNDREF 250

RMT13 M14 GNDREF 250

RMT14 M15 GNDREF 250

RMT15 M16 GNDREF 250

* Include Minitek* connector model.

X3 M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11 M12 M13 M14 M15 M16 MINITEK*

.ENDS TCKDR **********

* TMSDR

* TMS DRIVE MODEL LEVEL 1

* UPDATED: NOVEMBER 18, 1999

* EXPANDED DOCUMENTATION: AUGUST 18, 2000

```
*
* PINS:
*     GNDREF = GROUND
*     DRV = DRIVE FROM TWO VCX OUTPUTS
*     M2 = MINITEK* CONNECTOR AT TARGET
*
* ADDITIONAL REQUIRED SUBCIRCUIT INCLUDED IN PACKAGES.TXT:
*     MINITEK* = ITP DPA HEADER MODEL
*
* ADDITIONAL MODELS THAT MAY BE ADDED:
*     VCX16374 = TOSHIBA* VCX BUFFER/DRIVER
*
************************************************
.SUBCKT TMSDR GNDREF DRV M2
* Load elements
L1 DRV M1 100Nh
C3 M1 GNDREF 100Pf
* Setup Minitek* connector nodes
* Minitek* pad capacitance
CMT1 M1 GNDREF 5.00E-13
CMT2 M2 GNDREF 5.00E-13
* Tie all other Minitek* Model Pins to Ground
RMT2 M3 GNDREF 250
RMT3 M4 GNDREF 250
RMT4 M5 GNDREF 250
RMT5 M6 GNDREF 250
RMT6 M7 GNDREF 250
RMT7 M8 GNDREF 250
```

```
RMT8 M9 GNDREF 250
RMT9 M10 GNDREF 250
RMT10 M11 GNDREF 250
RMT11 M12 GNDREF 250
RMT12 M13 GNDREF 250
RMT13 M14 GNDREF 250
RMT14 M15 GNDREF 250
RMT15 M16 GNDREF 250
* Include Minitek* connector model
X1 M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11 M12 M13 M14 M15 M16 MINITEK*
.ENDS TMSDR
************************************************
* DBADBR
* DBR_ & DBA_ DRIVE MODEL LEVEL 1
* UPDATED: NOVEMBER 22, 1997
* EXPANDED DOCUMENTATION: AUGUST 18, 2000
*
* DRIVE DBADBR TO GROUND WHEN ACTIVE
*
* PINS:
*     GNDREF = GROUND
*     M2 = MINITEK* CONN. AT TARGET
*
* ADDITIONAL REQUIRED SUBCIRCUITS INCLUDED IN ITP700_PACKAGES.TXT:
*     QSOP = QSOP PIN MODEL, PACKAGE APPROXIMATION
*     MINITEK* = ITP DPA HEADER MODEL
*
* ADDITIONAL MODEL THAT MAY BE ADDED:
```

```
*     qs3vh125 = QUALITY SEMICONDUCTOR* QUICKSWITCH
*
************************************************
.SUBCKT DBADBR GNDREF M2
*
* The following is a generalization of the qs3vh125.
* A true spice model of the quickswitch may be
* added between pins M1 and GNDREF.
* Be sure to remove the following generalization
* if the true spice model is used.
************************************************
* GND path through quickswitch
* QSOP Pin Model
X1 GNDREF INT1 GNDREF QSOP
* Quickswitch Internal Resistance
RQS INT1 INT2 4
* QSOP Pin Model
X2 M1 INT2 GNDREF QSOP
************************************************
* setup Minitek* connector nodes
* Minitek* pad capacitance
CMT1 M1 GNDREF 5.00E-13
CMT2 M2 GNDREF 5.00E-13
* Tie all other Minitek* Model Pins to Ground
RMT2 M3 GNDREF 250
RMT3 M4 GNDREF 250
RMT4 M5 GNDREF 250
RMT5 M6 GNDREF 250
```

```
RMT6 M7 GNDREF 250
RMT7 M8 GNDREF 250
RMT8 M9 GNDREF 250
RMT9 M10 GNDREF 250
RMT10 M11 GNDREF 250
RMT11 M12 GNDREF 250
RMT12 M13 GNDREF 250
RMT13 M14 GNDREF 250
RMT14 M15 GNDREF 250
RMT15 M16 GNDREF 250
* Include Minitek* connector model.
X3 M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11 M12 M13 M14 M15 M16 MINITEK*
.ENDS DBADBR
************************************************
* BPM5DR
* BPM[5] DRIVE MODEL LEVEL 1
* UPDATED: NOVEMBER 18 1999
*
* DRIVE BPM5DR TO GROUND WHEN ACTIVE
*
* PINS:
*    GNDREF=GR0UND
*    M2=MINITEK* CONNECTOR AT TARGET
*
* ADDITIONAL REQUIRED SUBCIRCUITS INCLUDED IN ITP700_PACKAGES.TXT:
*    QSOP = QSOP PIN MODEL, PACKAGE APPROXIMATION
*    MINITEK* = ITP DPA HEADER MODEL
*
```

```
* ADDITIONAL MODEL THAT MAY BE ADDED:
*     qs3vh125 = QUALITY SEMICONDUCTOR* QUICKSWITCH
*
************************************************
.SUBCKT BPM5DR GNDREF M2
* Declare VCX (produced on DPI/DPA)
VINIT1 VCX GNDREF DC 1.65
*
* The following is a generalization of the qs3vh125.
* A true spice model of the quickswitch may be
* added between pins BPM5QS and GNDREF.
* Be sure to remove the following generalization
* if the true spice model is used.
************************************************
* BPM5QS path to GND through quickswitch
* QSOP Pin Model
X1 GNDREF INT1 GNDREF QSOP
* Quickswitch Internal Resistance
RQS INT1 INT2 4
* QSOP Pin Model
X2 BPM5QS INT2 GNDREF QSOP
************************************************
* Load elements
R17 BPM5QS VCX 249
L3 BPM5QS BPM5A 3.30E-7
R15 BPM5A M1 10
* Setup Minitek* connector nodes
* Minitek* pad capacitance
```

CMT1 M1 GNDREF 5.00E-13

CMT2 M2 GNDREF 5.00E-13

* Tie all other Minitek* Model Pins to Ground

RMT2 M3 GNDREF 250

RMT3 M4 GNDREF 250

RMT4 M5 GNDREF 250

RMT5 M6 GNDREF 250

RMT6 M7 GNDREF 250

RMT7 M8 GNDREF 250

RMT8 M9 GNDREF 250

RMT9 M10 GNDREF 250

RMT10 M11 GNDREF 250

RMT11 M12 GNDREF 250

RMT12 M13 GNDREF 250

RMT13 M14 GNDREF 250

RMT14 M15 GNDREF 250

RMT15 M16 GNDREF 250

* Include Minitek* connector model.

X3 M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11 M12 M13 M14 M15 M16 MINITEK*

.ENDS BPM5DR

Receive Pins:

```
************************************************
* BCK
* BCLK(pn), LOAD MODEL LEVEL 1
* CREATED: NOVEMBER 22, 1999
* EXPANDED DOCUMENTATION: AUGUST 18, 2000
*
* PINS:
*    M2=MINITEK* BCKP CONN AT TARGET
*    M4=MINITEK* BCKN CONN AT TARGET
*    ECLP=BCKP ECL INPUT
*    ECLN=BCKN ECL INPUT
*
* ADDITIONAL REQUIRED SUBCIRCUITS INCLUDED IN PACKAGES.TXT:
*    QSOP = QSOP PIN MODEL, PACKAGE APPROXIMATION
*    MINITEK* = ITP DPA HEADER MODEL
*
* ADDITIONAL MODELS THAT MAY BE ADDED:
*    mc100lvel17 = MOTOROLA ECL RECEIVER
*    qs3vh125 = QUALITY SEMICONDUCTOR* QUICKSWITCH
*
************************************************
*
.SUBCKT BCK M2 M4 ECLP ECLN GNDREF
* Voltages supplied by the DPA
VINIT1 VEE GNDREF -1.2
VINIT2 VCC GNDREF 2.1
*
```

```
*
* The following is a generalization of the qs3vh125.
* A true spice model of the quickswitch may be
* added between pins M1 and BCLKQSP and pins
* M3 and BCLKQSN. Be sure to remove the following
* generalization If the true spice model is used
************************************************
* BCLKP path through quickswitch
* QSOP Pin Model
X1 M1 INT1 GNDREF QSOP
* Quickswitch Internal Resistance
RQS1 INT1 INT2 4
* QSOP Pin Model
X2 BCLKQSP INT2 GNDREF QSOP
*
* BCLKN path through quickswitch
* QSOP Pin Model
X3 M3 INT3 GNDREF QSOP
* Quickswitch Internal Resistance
RQS2 INT3 INT4 4
* QSOP Pin Model
X4 BCLKQSN INT4 GNDREF QSOP
************************************************
* Load Elements
R9 BCLKQSP ECLP 24.9
R10 BCLKQSN ECLN 24.9
RP11A VEE ECLP 5600
RP11B VCC ECLN 5600
```

RP11C GNDREF ECLN 5600

RP11D GNDREF ECLN 5600

R21 ECLN ECLP 100

* Setup of Minitek* connector nodes

* Minitek* pad capacitance

CMT1 M1 GNDREF 5.00E-13

CMT2 M2 GNDREF 5.00E-13

CMT3 M3 GNDREF 5.00E-13

CMT4 M4 GNDREF 5.00E-13

* Tie all other Minitek* Model Pins to Ground

RMT4 M5 GNDREF 250

RMT5 M6 GNDREF 250

RMT6 M7 GNDREF 250

RMT7 M8 GNDREF 250

RMT8 M9 GNDREF 250

RMT9 M10 GNDREF 250

RMT10 M11 GNDREF 250

RMT11 M12 GNDREF 250

RMT12 M13 GNDREF 250

RMT13 M14 GNDREF 250

RMT14 M15 GNDREF 250

RMT15 M16 GNDREF 250

* Include the model of the Minitek* connector

X5 M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11 M12 M13 M14 M15 M16 MINITEK*

.ENDS BCK

****

* BPMRESET

* TDO,BPM[5..O]n, AND RESETn LOAD MODEL LEVEL 1

```
* UPDATED: NOVEMBER 22, 1999
* EXTENDED DOCUMENTATION: AUGUST 18, 2000
*
* PINS:
*     GNDREF=GR0UND
*     M2 = MINITEK* AT TARGET
*     ECL = OUTPUT OF ATTENUATOR AT INPUT OF ECL RECEIVER
*
* ADDITIONAL REQUIRED SUBCIRCUIT INCLUDED IN ITP700_PACKAGES.TXT:
*     MINITEK* = ITP DPA HEADER MODEL
*
* ADDITIONAL MODEL THAT MAY BE ADDED:
*     mc100lvel17 = MOTOROLA* ECL RECEIVER
*
************************************************
.SUBCKT BPMRESET GNDREF M2 ECL
* ATTENUATOR MODEL
C3 M1 ATTX 3.30E-12
C4 ATTX GNDREF 1.0E-12
R16 M1 ATTX 5600
R17 ATTX GNDREF 5600
RS7 ATTX ECL 61.9
*
* Setup Minitek* connector nodes
* Minitek* pad capacitance
CMT1 M1 GNDREF 5.00E-13
CMT2 M2 GNDREF 5.00E-13
* Tie all other Minitek* Model Pins to Ground
```

RMT2 M3 GNDREF 250

RMT3 M4 GNDREF 250

RMT4 M5 GNDREF 250

RMT5 M6 GNDREF 250

RMT6 M7 GNDREF 250

RMT7 M8 GNDREF 250

RMT8 M9 GNDREF 250

RMT9 M10 GNDREF 250

RMT10 M11 GNDREF 250

RMT11 M12 GNDREF 250

RMT12 M13 GNDREF 250

RMT13 M14 GNDREF 250

RMT14 M15 GNDREF 250

RMT15 M16 GNDREF 250

* Include Minitek* connector model

X1 M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11 M12 M13 M14 M15 M16 MINITEK*

.ENDS BPMRESET

****

* FBO

* FBO LOAD MODEL LEVEL 1

* CREATED: NOVEMBER 22, 1999

* EXPANDED DOCUMENTATION: AUGUST 18, 2000

*

* PINS:

* GNDREF=GROUND

* M2=MINITEK* CONN AT TARGET

* ECL= ECL INPUT

* POW= TARGET VCC VOLTAGE

```
* ADDITIONAL REQUIRED SUBCIRCUITS INCLUDED IN ITP700_PACKAGES.TXT:
*     QSOP = QSOP PIN MODEL, PACKAGE APPROXIMATION
*     MINITEK* = ITP DPA HEADER MODEL
*
* ADDITIONAL MODELS THAT MAY BE ADDED:
*     mc100lvel17 = MOTOROLA* ECL RECEIVER
*     qs3vh125 = QUALITY SEMICONDUCTOR* QUICKSWITCH
*
************************************************
*
.SUBCKT FBO GNDREF M2 ECL POW
*THE FOLLOWING SETS UP VREF AS .66 POW NODE
EM1 VREF GNDREF POW GNDREF .66
*
* The following is a generalization of the qs3vh125
* a true spice model of the quickswitch may be
* added between pins M1 and FBOQS.
* Be sure to remove the following
* generalization If the true spice model is used
************************************************
* FBO Path through quickswitch
* QSOP Pin Model
X1 M1 INT1 GNDREF QSOP
* Quickswitch Internal Resistance
RQS INT1 INT2 4
* QSOP Pin Model
X2 FBOQS INT2 GNDREF QSOP
************************************************
```

* Load elements

R8 FBOQS ECL 24.9

R20 ECL VREF 51

C21 VREF GNDREF .1E-6

* Set up Minitek* connector nodes

* Minitek* pad capacitance

CMT1 M1 GNDREF 5.00E-13

CMT2 M2 GNDREF 5.00E-13

* Tie all other Minitek* Model Pins to Ground

RMT2 M3 GNDREF 250

RMT3 M4 GNDREF 250

RMT4 M5 GNDREF 250

RMT5 M6 GNDREF 250

RMT6 M7 GNDREF 250

RMT7 M8 GNDREF 250

RMT8 M9 GNDREF 250

RMT9 M10 GNDREF 250

RMT10 M11 GNDREF 250

RMT11 M12 GNDREF 250

RMT12 M13 GNDREF 250

RMT13 M14 GNDREF 250

RMT14 M15 GNDREF 250

RMT15 M16 GNDREF 250

* Include model of Minitek* connector

X3 M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11 M12 M13 M14 M15 M16 MINITEK*

.ENDS FBO

****

* PWR

```
* PWR LOAD MODEL LEVEL 1
* CREATED: NOVEMBER 22, 1999
* EXPANDED DOCUMENTATION: AUGUST 18, 2000
*
* PINS:
*     GNDREF=GROUND
*     M2=MINITEK* BCKP CONN AT TARGET
*
* ADDITIONAL REQUIRED SUBCIRCUIT INCLUDED IN ITP700_PACKAGES.TXT
*     MINITEK* = ITP DPA HEADER MODEL
*
************************************************
.SUBCKT PWR GNDREF M2
* Load elements
RDIV M1 GNDREF 3000
* Setup Minitek* connector nodes
* Minitek* pad capacitance
CMT1 M1 GNDREF 5.00E-13
CMT2 M2 GNDREF 5.00E-13
* Tie all other Minitek* Model Pins to Ground
RMT2 M3 GNDREF 250
RMT3 M4 GNDREF 250
RMT4 M5 GNDREF 250
RMT5 M6 GNDREF 250
RMT6 M7 GNDREF 250
RMT7 M8 GNDREF 250
RMT8 M9 GNDREF 250
RMT9 M10 GNDREF 250
```

RMT10 M11 GNDREF 250

RMT11 M12 GNDREF 250

RMT12 M13 GNDREF 250

RMT13 M14 GNDREF 250

RMT14 M15 GNDREF 250

RMT15 M16 GNDREF 250

* Include Minitek* connector model

X1 M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11 M12 M13 M14 M15 M16 MINITEK*

.ENDS PWR

Package:

****

* Minitek* SPICE Subcircuit

* BERG Electronics*

* DCG1092*

****

.SUBCKT MINITEK* 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

X1 1 17 3 21 5 25 7 29 9 33 11 37 13 41 15 45 SECT

X2 17 18 21 22 25 26 29 30 33 34 37 38 41 42 45 46 SECT

X3 18 19 22 23 26 27 30 31 34 35 38 39 42 43 46 47 SECT

X4 19 20 23 24 27 28 31 32 35 36 39 40 43 44 47 48 SECT

X5 20 2 24 4 28 6 32 8 36 10 40 12 44 14 48 16 SECT

.ENDS MINITEK*

*

*PORTS 1A 1B 2A 2B 3A 3B 4A 4B 5A 5B 6A 6B 7A 7B 8A 8B

*LENGTH 5.69 mm

.SUBCKT SECT 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

L11 1 2 3.936342E-10

L22 3 4 4.116146E-10

L33 5 6 4.116146E-10

L44 7 8 3.936342E-10

L55 9 10 3.936342E-10

L66 11 12 4.116146E-10

L77 13 14 4.116146E-10

L88 15 16 3.936342E-10

C11 2 0 4.240507E-14

C22 4 0 2.854559E-15

C33 6 0 2.854480E-15

C44 8 0 4.240475E-14

C55 10 0 4.240512E-14

C66 12 0 2.854593E-15

C77 14 0 2.854605E-15

C88 16 0 4.240524E-14

K12 L11 L22 6.355457E-01

C12 2 4 1.071086E-13

K13 L11 L33 4.534765E-01

C13 2 6 1.729760E-15

K14 L11 L44 3.313096E-01

C14 2 8 7.302546E-16

K15 L11 L55 5.582538E-01

C15 2 10 7.375378E-14

K16 L11 L66 5.069099E-01

C16 2 12 7.890892E-15

K17 L11 L77 4.102210E-01

C17 2 14 1.064030E-16

K18 L11 L88 3.133854E-01

C18 2 16 1.342840E-16

K23 L22 L33 6.472215E-01

C23 4 6 1.065396E-13

K24 L22 L44 4.534765E-01

C24 4 8 1.735450E-15

K25 L22 L55 5.069099E-01

C25 4 10 7.892030E-15

K26 L22 L66 6.010506E-01

C26 4 12 6.228274E-14

K27 L22 L77 5.275090E-01

C27 4 14 7.815784E-15

K28 L22 L88 4.102210E-01

C28 4 16 1.065168E-16

K34 L33 L44 6.355457E-01

C34 6 8 1.071086E-13

K35 L33 L55 4.102210E-01

C35 6 10 1.065965E-16

K36 L33 L66 5.275090E-01

C36 6 12 7.815784E-15

K37 L33 L77 6.010506E-01

C37 6 14 6.228274E-14

K38 L33 L88 5.069099E-01

C38 6 16 7.892030E-15

K45 L44 L55 3.133854E-01

C45 8 10 1.346254E-16

K46 L44 L66 4.102210E-01

C46 8 12 1.062664E-16

K47 L44 L77 5.069099E-01

C47 8 14 7.890892E-15

```
K48 L44 L88 5.582538E-01
C48 8 16 7.375378E-14
K56 L55 L66 6.355457E-01
C56 10 12 1.071086E-13
K57 L55 L77 4.534765E-01
C57 10 14 1.729760E-15
K58 L55 L88 3.313096E-01
C58 10 16 7.301408E-16
K67 L66 L77 6.472215E-01
C67 12 14 1.065396E-13
K68 L66 L88 4.534765E-01
C68 12 16 1.735450E-15
K78 L77 L88 6.355457E-01
C78 14 16 1.071086E-13
.ENDS SECT
**********************************************************
********** Package Models ***********
* QSOP Package Model (QSOP)
*EXT =(External Input to Pin) INT= (Internal Output of the Pin) GNDREF= (0V)
**************************************************************
.SUBCKT QSOP EXT INT GNDREF
CPAD EXT GNDREF 0.5PF
CPKG 82 GNDREF 0.5PF
RPKG3 83 INT 0.01
LPKG1 EXT 82 1NH
LPKG2 82 83 1NH
.ENDS QSOP
**********************************************************
```