Intel® Pentium® III Processor – Low-Power Module Design Guide

Application Note

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Revision History

Revision	Date	Notes
002	April 2000	Changed the V_DC definition in Table 64. DC voltage driven from the power supply and is required to be 5 V ± 5%.
001	February 2000	First release of this document.

1.0 Introduction

This document provides design guidelines for developing systems based on the Intel® Pentium® III Processor – Low-Power Module. System board and memory subsystem design guidelines are included. Special design recommendations and concerns are presented. Likely design errors have been listed here in a checklist format. These are recommendations only. It is recommended that you perform your own simulations to meet design-specific requirements.

1.1 Key Terms

The Pentium® III Processor – Low-Power Module is specific to the applied computing market segment. It supports a V_{DC} of 5 V only and a fixed frequency. A complete description of the module is located in the *Intel® Pentium® III Processor – Low-Power Module* datasheet.

Intel 440BX AGPset refers to both the 82443 BX Host Bridge/Controller and the 82371EB PCI ISA IDE Xcelerator.

82443BX refers to the Intel 82443BX Host Bridge/Controller.

PIIX4E refers to the Intel 82371EB PCI ISA IDE Xcelerator.

Design Features are items that allow the designer to fully use the capabilities of the Pentium III processor and the Intel 440BX AGPset.

Design Checklists are items which provide recommendations for designing a Low-Power Module-based platform.

Design Considerations are items that should be considered but may not be applicable to your design.

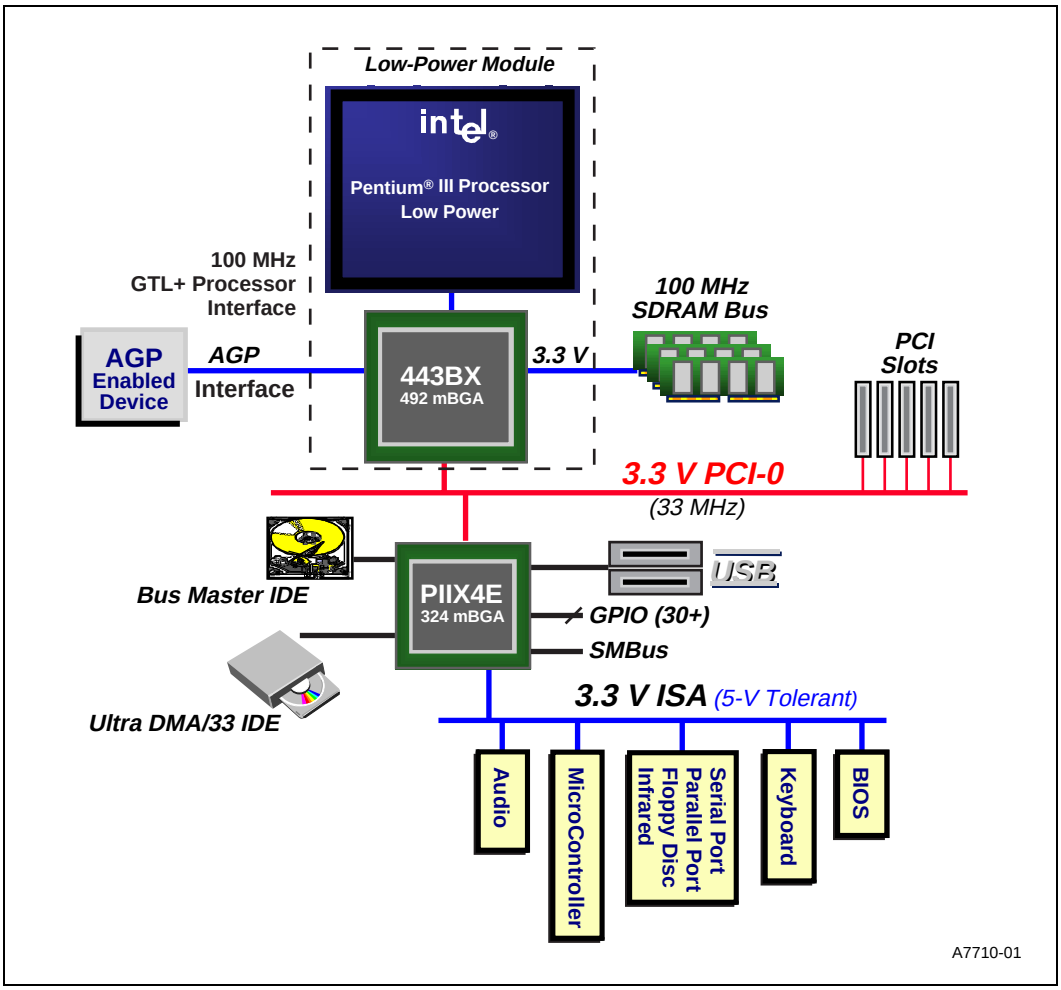
1.2 Overview

Low-Power Module features are summarized below. Figure 1 is a block diagram of a typical Low-Power Module system design.

- Full support for the Pentium® III Processor – Low-Power with system bus frequencies of 100 MHz
- Intel 440BX AGPset
  - 82443BX Host Bridge/Controller (443BX)
  - 82371EB PCI ISA IDE Accelerator (PIIX4E)
- 100 MHz memory interface: A wide range of DRAM support including:
  - 64-bit memory data interface plus 8 ECC bits and hardware scrubbing
  - 100 MHz SDRAM Support
  - 64-Mbit and 128-Mbit DRAM technologies
- 5 PCI masters
  - PCI Specification Rev 2.1 Compliant

- Accelerated Graphics Port (AGP) Slot:
  - — AGP Interface Specification Revision 1.0 compliant
  - — AGP - 66/133 MHz, 3.3-V device support
- Integrated IDE controller with Ultra DMA/33 support
  - — PIO Mode 4 transfers
  - — PCI IDE bus master support
- Integrated Universal Serial Bus (USB) controller with two USB ports
- Integrated System Power Management support

Figure 1. Low-Power Module/440BX AGPset System Block Diagram



1.3 Related Documents

Table 1. Related Intel Documents

Document	Order Number
Intel® Pentium® III Processor – Low-Power Module datasheet	273299
Mobile Pentium® III Processor Specification Update	245306
Intel® 440BX AGPset: 82443BX Host Bridge/Controller datasheet	290633
Intel® 440BX AGPset 82443BX Host Bridge/Controller Specification Update	290639
Intel® 82371AB PCI-to-ISA/IDE Xcelerator (PIIX4) datasheet	290562
Intel® 82371EB PCI-to-ISA/IDE Xcelerator (PIIX4E) Specification Update	290635
Intel® Architecture Software Developer's Manual, Volume 1; Basic Architecture	243190
Intel® Architecture Software Developer's Manual, Volume 2; Instruction Set Reference	243191
Intel® Architecture Software Developer's Manual, Volume 3; System Programming Guide	243192
Intel® Architecture MMX™ Technology Developer's Guide	243006
Low-Power Module Memory Bus Simulation Methodology	273316
Low-Power Module SDRAM DIMM Routing Guidelines	273317
CK97 Clock Synthesizer Design Guidelines application note	243867
AP-485 *Intel Processor Identification and the CPUID Instruction* application note	241618
AP-585 *Pentium® III Processor GTL + Guidelines* application note	243330
AP-586 *Pentium® III Processor Thermal Design Guidelines* application note	243331
PIIX4 Universal Serial Bus Design Guide	NDA†

† NDA documents are only available through an Intel Field Sales Representative.

Table 2. Related Specifications

Document	URL/Contact
PCI Local Bus Specification, Revision 2.1	http://www.pcisig.com/specs.html
Universal Serial Bus Specification, Revision 1.0	http://www.usb.org/usb/developers/index.html
AGP Interface Specification, Revision 1.0	http://www.agpforum.org/index.htm
AGP Platform Design Guide, Revision 1.1A	http://www.agpforum.org/index.htm
Information Technology – AT Attachment with Packet Interface Extension (ATA/ATAPI-4)	ftp://fission.dt.wdc.com/pub/standards/
System Management Bus Specification	http://www.sbs-forum.org/
66-MHz Unbuffered SDRAM 64-bit (Non-ECC/Parity) 144-pin SO-DIMM Specification, Revision 1.0	Contact an Intel Field Sales Representative

2.0 Design Features

2.1 Intel® Pentium® III Processor – Low Power

The Pentium III processor – Low Power is the first of the Pentium III processor family to be offered for the applied computing platform. It is offered at 500 MHz with a processor system bus speed of 100 MHz. It consists of a Pentium III processor core with an integrated 256-Kbyte second-level cache and a 64-bit high-performance host bus. The second-level cache bus complements the host bus by providing critical data faster, improving performance, and reducing total system power consumption. The Pentium III processor – Low Power's 64-bit wide Low-power GTL+ host bus is compatible with the Intel® 440BX AGPset and provides a glueless, point-to-point interface for an I/O bridge and memory controller.

2.2 Intel® 440BX AGPset

The Intel® 440BX AGPset is based on the Pentium III processor architecture. It interfaces with the Pentium III processor's system bus at 100 MHz. Along with its Host-to-PCI bridge interface, the 82443BX Host Bridge/Controller has been optimized with a 100 MHz SDRAM memory controller and data path unit. The 82443BX also features the Accelerated Graphics Port (AGP) interface. The 82443BX component includes the following functions and capabilities:

- 64-bit Low Power GTL+ based system data bus interface
- 32-bit system address bus support
- 64-bit main memory interface with optimized support for SDRAM
- 32-bit PCI bus interface with integrated PCI arbiter
- AGP interface with up to 133 MHz data transfer capability
- Extensive data buffering between all interfaces for high throughput and concurrent operations

Figure 1 shows a block diagram of a typical platform based on the 440BX AGPset. The 82443BX system bus interface supports a Pentium III processor at a bus frequency of 100 MHz. The physical interface design is based on the Low Power GTL+ specification and is compatible with the Intel 440BX AGPset. The 440BX provides an optimized 72-bit DRAM interface (64-bit Data plus ECC). This interface supports 3.3-V DRAM technologies.

The 82443BX is designed to support the PIIX4E I/O bridge. The PIIX4E is a highly-integrated multifunctional component that supports the following functions and capabilities:

- PCI Revision 2.1 compliant PCI-to-ISA bridge with support for 33 MHz PCI operations
- ACPI Power Management support
- Enhanced DMA controller, interrupt controller and timer functions
- Integrated IDE controller with Ultra DMA/33 support
- USB host interface with support for two USB ports
- System Management Bus (SMB) with support for DIMM Serial Presence Detect

2.2.1 System Bus Interface

The 82443BX supports a maximum of 4 Gbytes of memory address space from the processor perspective. The largest address size is 32 bits. The 82443BX provides bus control signals and address paths for transfers between the processor bus, PCI bus, Accelerated Graphics Port and main memory. The 82443BX supports a 4-deep-in-order queue, which provides support for pipelining of up to four outstanding transaction requests on the system bus. The Pentium III processor supports a second-level cache. All cache-control logic is provided on the processor.

For system bus-to-PCI transfers, the addresses are either translated or directly forwarded on the PCI bus, depending on the PCI address space being accessed. When the access is to a PCI configuration space, the processor I/O cycle is mapped to a PCI configuration space cycle. When the access is to a PCI I/O or memory space, the processor address is passed without modification to the PCI bus. Certain memory address ranges are dedicated for a graphics memory address space. When this space or a portion of it is mapped to main DRAM, the address is translated by the AGP address remapping mechanism and the request is forwarded to the DRAM subsystem. A portion of the graphics aperture can be mapped on the AGP, and the corresponding system bus cycles accessing that range are forwarded to the AGP without any translation. The AGP address map defines other system bus cycles that are forwarded to the AGP.

2.2.2 DRAM Interface

The 82443BX integrates a main memory controller that supports a 64-bit DRAM interface which operates at 100 MHz. The integrated DRAM controller features include:

- 3.3-V interface
- Support for up to three double-sided SODIMMs
  - 384 Mbytes using 128-Mbit technology
  - 192 Mbytes using 64-Mbit technology
  - 48 Mbytes using 16-Mbit technology
- Support for ECC with hardware scrubbing

2.2.3 Accelerated Graphics Port Interface

The 82443BX supports an AGP interface. The AGP interface has a maximum theoretical transfer rate of ~532 Mbytes/s.

2.2.4 PCI Interface

The 82443BX PCI interface operates at 33 MHz, is Revision 2.1 compliant, and supports up to five external PCI bus masters in addition to the PIIX4E I/O bridge. The PCI interface is only 3.3 V. If the developer requires a 5-V interface, a level shifter implementation is recommended.

2.2.5 System Clocking

Used with the Pentium® III processor, the 82443BX operates the system bus interface at 100 MHz, the PCI bus at 33 MHz and the AGP at a transfer rate of 66/133 MHz. The 82443BX clocking scheme uses an external clock synthesizer that produces reference clocks for the system bus and PCI interfaces. The 82443BX generates the AGP and DRAM clock signals. Please refer to the *CK97 Clock Synthesizer/Design Guidelines* (order number 243867).

2.3 PCI ISA IDE Xcelerator (PIIX4E)

The PCI ISA IDE Xcelerator (PIIX4E) is a multi-function PCI device that implements a PCI-to-ISA bridge function, a PCI IDE function, a Universal Serial Bus host/hub function, and an Enhanced Power Management function. Because it is a PCI-to-ISA bridge, the PIIX4E integrates many common I/O functions found in ISA-based PC systems; a seven channel DMA Controller, two 82C59 Interrupt Controllers, an 8254 Timer/Counter, and a Real Time Clock. In addition to DMA Compatible transfers, each DMA channel also supports Type F transfers.

The PIIX4E contains full support for PC/PCI and Distributed DMA protocols that implement PCI-based DMA. The Interrupt Controller has edge or level sensitive programmable inputs. Chip select decoding is provided for a BIOS, Real Time Clock, Keyboard Controller, second external microcontroller, and two Programmable Chip Selects. The PIIX4E provides full Plug-and-Play compatibility. The PIIX4E can be configured as a subtractive decode bridge or as a positive decode bridge.

The PIIX4E supports two IDE connectors. This provides an interface for IDE/EIDE hard disks and CD-ROMs. Up to four IDE devices can be supported in Bus Master mode. The PIIX4E contains support for Ultra DMA/33 compatible synchronous DMA devices.

The PIIX4E contains a Universal Serial Bus (USB) host controller that is Universal Host Controller Interface (UHCI) compatible. The host controller's root hub has two programmable USB ports.

The PIIX4E supports Enhanced Power Management, including full clock control, device management for up to 14 devices, and suspend and resume logic with Power On Suspend, Suspend to RAM, or Suspend to Disk. The PIIX4E fully supports operating-system-directed power management according to the Advanced Configuration and Power Interface (ACPI) specification. The PIIX4E integrates both a System Management bus (SMBus) host and slave interface for serial communication with other devices.

For more information on the PIIX4E, please refer to the *82371AB PCI-to-ISA/IDE Xcelerator (PIIX4)* datasheet (order number 290562) and the 82371EB PCI-to-ISA/IDE Xcelerator (PIIX4E) Specification Update (order number 290635).

3.0 Memory Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. The order in which signals are routed first and last will vary from designer to designer. Some designers prefer routing the clock signals first, while others prefer routing the high-speed bus signals first. Either order can be used, as long as the guidelines listed here are followed. When the guidelines listed here are not followed, it is very important to simulate the design. Even when the guidelines are followed, it is recommended that you simulate these signals for proper signal integrity, flight time and cross talk.

3.1 100 MHz SDRAM Interface Overview

The 82443BX integrates a main memory DRAM controller that supports a 64-bit DRAM array for 100 MHz embedded environments. The Pentium III Processor – Low-Power Module supports Synchronous DRAM (SDRAM); it does not support EDO memory. The 82443BX DRAM

interface runs at 100 MHz. The DRAM controller interface is fully configured through a set of control registers. Complete descriptions of these registers are given in the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet.

The 443BX supports industry standard 64-bit wide 144-pin SODIMM modules with SDRAM devices. Both symmetric and asymmetric addressing is supported. For write operations of less than a Qword in size, the 443BX will either perform a byte-wide write cycle (non-ECC protected configuration) or a read-modify-write cycle by merging the write data on a byte basis with the previously read data (ECC or error correction configurations). The 82443BX requires SDRAM with CAS latency of 2 (CL2), and supports 1-and 2-row SODIMMs. The 82443BX provides refresh functionality with programmable rates (normal DRAM rate is 1 refresh/15.6 µs). The 82443BX can be configured via the paging policy register to keep multiple pages open within the memory array. Pages can be kept open in all rows of memory. When using two bank SDRAM devices in a particular row, up to two pages can be kept open within that row.

The DRAM interface of the 82443BX is configured by the DRAM control registers, DRAM timing register, SDRAM control register, bits in the NBXCFG register and the eight DRAM row boundary (DRB) registers. The DRAM configuration registers control the DRAM interface to select EDO or SDRAM, RAS timing, and CAS rates. The eight DRB registers define the size of each row in the memory array, enabling the 82443BX to assert the proper CSA[7:0]#, CSB[7:0]# pair for accesses to the array.

3.1.1 SDRAM Signal Description

The following sections explain which signals are used in applied computing platforms, and how they should be connected. Note that MAB[13,10] are not inverted because these address bits are used to define various SDRAM commands. Also note that MECC[7:0] should be left unconnected, because the Pentium® III Processor - Low Power does not support ECC.

Table 3 identifies the SDRAM signals and the corresponding description.

Table 3. SDRAM Signal Descriptions (Sheet 1 of 2)

Name	Type	Voltage	Description
MECC[7:0][1]	I/O CMOS	V_3	**Memory ECC Data:** These signals carry Memory ECC data during access to DRAM. These pins are implemented by design (NOT TESTED) on the module.
CSA[5:0]#	O CMOS	V_3	**Chip Select (SDRAM):** These pins activate SDRAM. SDRAM accepts any command when its CS# pin is active low.
DQMA[7:0]	O CMOS	V_3	**Input/Output Data Mask (SDRAM):** These pins act as synchronized output enables during a read cycle and as a byte mask during a write cycle.
MAB[9:0]# MAB[10][2] MAB[12:11]# MAB[13][1]	O CMOS	V_3	**Memory Address (SDRAM):** This is the row and column address for DRAM. The 443BX Host Bridge system controller has two identical sets of address lines (MAA and MAB#). The Pentium III Processor - Low Power Module supports only the MAB set of address lines. For additional addressing features, please refer to the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller Datasheet*.
MWEA#	O CMOS	V_3	**Memory Write Enable (SDRAM):** MWEA# should be used as the write enable for the memory data bus.
SRASA#	O CMOS	V_3	**SDRAM Row Address Strobe (SDRAM):** When active low, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and pre-charge.

Table 3. SDRAM Signal Descriptions (Sheet 2 of 2)

SCASA#	O CMOS	V_3	**SDRAM Column Address Strobe (SDRAM):** When active low, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access.
CKE[5:0]	O CMOS	V_3	**SDRAM Clock Enable (SDRAM):** The SDRAM clock enable pin. When these signals are deasserted, SDRAM enters power-down mode. Each row is individually controlled by its own clock enable.
MD[63:0]	I/O CMOS	V_3	**Memory Data:** These signals are connected to the DRAM data bus. They are not terminated on the module.

NOTES:
1. MECC[7:0] signals should be left unconnected, because the Pentium III Processor - Low Power does not support ECC.
2. MAB[13,10] signals are not inverted because these address bits are used to define various SDRAM commands.

3.1.2 SDRAM Signal Connectivity

The DRAM expansion socket is a 144-pin SO-DIMM. Table 4 identifies the SDRAM signals and the corresponding SO-DIMM pins. Table 5 identifies the module SDRAM signals and the corresponding onboard SDRAM signals.

Table 4. SDRAM Signals and Corresponding SO-DIMM Pins

Signal Name	SO-DIMM Pin
MAB[11]#	106
MAB[12]#	70, 110
MAB[13]#	72, 112

Table 5. Module SDRAM Signals and Corresponding Onboard SDRAM Signals

Signal Name	SDRAM Component Pin
MAB[11]#	A13/BA0
MAB[12]#	A12/BA1
MAB[13]#	A11

3.1.3 Pin Groups

The 82443BX has multiple copies of many of the signals interfacing to memory. However, the Low-Power Module/440BX AGPset only supports a single copy of the memory signals. See “Single Set DRAM Interface” on page 17 for more information. The interface consists of the following pins:

Multiple copies:

MAA[13:0], MAB[12:11,9:0]# and MAB[13, 10]
CSA[7:0]#, CSB[7:0]#
SRASA#, SRASB#
SCASA#, SCASB#
WEA#, WEB#
DQMA[7:0], DQMB[5:1]

Single copies:

CKE[5:0] (for three SODIMM configuration)
MD[63:0]
MECC[7:0]
GCKE (for four DIMM configuration)
FENA (FET switch control for four DIMM configuration)

Two CS# lines are provided per row. These are functionally equivalent. The extra copy is provided for loading reasons. The two SRAS#, SCAS# and WE# pins are also functionally equivalent and each copy drives two rows of DRAM. Most pins use programmable strength output buffers. When a row contains 16-Mbit SDRAMs, MAA11 and MAB11# function as Bank Select lines. When a row contains 64-Mbit SDRAMs, MAA[12:0], MAB[12:11] function as Bank Addresses (BA[1:0], or Bank Selects). If the design does not support ECC, you may leave MECC[7:0] unconnected. When the design supports ECC, perform simulations to determine which buffer strength is needed for loading requirements. This may require a BIOS change.

3.1.4 Single Set DRAM Interface

The following two sections explain which signals are used in embedded platforms. Note that MAB[13,10] are not active low because these address bits are used to define various SDRAM commands.

3.1.4.1 SDRAM

Single copies used:

MAB[12:11,9:0]# and MAB[13,10]
MD[63:0]
MECC[7:0]
CSA[5:0]#
DQMA[7:0]
CKE[5:0]
SRASA#
SCASA#
WEA#

3.2 General SDRAM Layout Guidelines

The following list identifies the SDRAM layout guidelines:

1. To obtain the most advantageous system electronics board layout, byte lanes may be swapped. Bits within a byte lane may also be swapped. However, bits between byte lanes may not be swapped.
2. A system electronics board nominal trace width should have an impedance of 55 Ω ± 10%. Impedance of a nominal trace width is a key parameter specified to board fabricators. Typically, nominal trace width is constrained by design density, the substrate material, and the board fabrication process. Common trace widths are 4 mils, 5 mils, and 6 mils.
3. All resistors should have a maximum ± 5% tolerance.
4. Populate the furthest SO-DIMM first to avoid stub reflections.

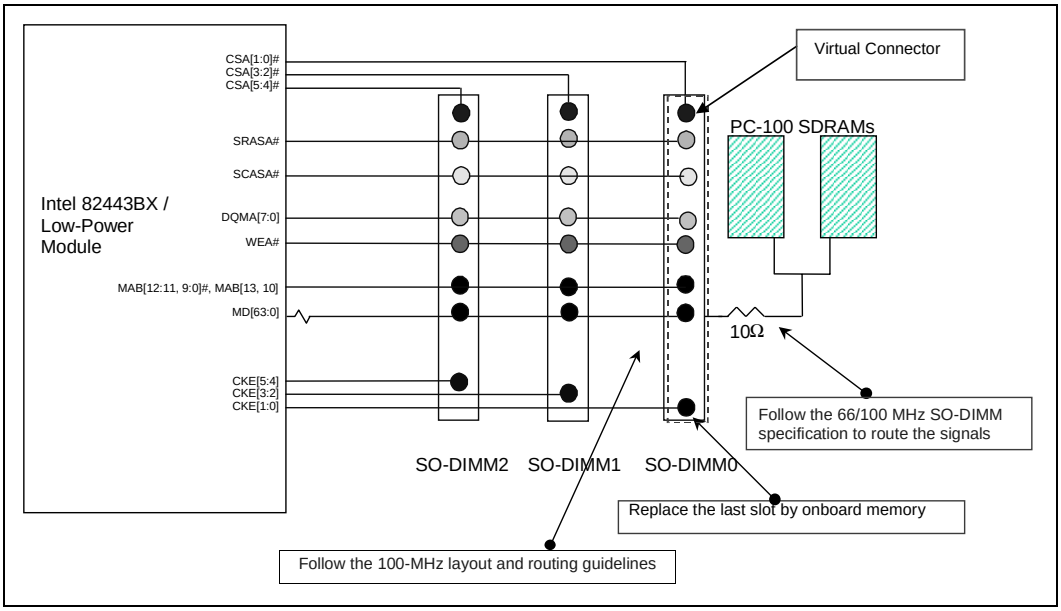
5. Any onboard memory should replace the furthest SO-DIMM socket.
6. Place onboard DRAM and SO-DIMM connectors as near as possible to each other.
7. CKBF-M should be powered by V_3 (the 3.3V rail power supply which remains on during Suspend).

3.2.1 SO-DIMM Connection to SDRAM

Guidelines for the following memory configurations are provided: three SO-DIMM sockets, two SO-DIMM sockets, or two SO-DIMM sockets with onboard memory. For memory configurations with onboard memory, the onboard memory routing can be treated as a third SO-DIMM. For example, the onboard memory is routed to a place on the board where a third SO-DIMM connector would otherwise be placed. In this document, the space is identified as a "virtual" SO-DIMM connector. See Figure 2 for more detail.

The "virtual" SO-DIMM connector is not a physical component but a design reference point (placeholder).

Figure 2. SDRAM Connections



3.3 Trace Lengths for Three or Two SO-DIMM Designs

The figures and tables below show the topology, and provide the minimum and maximum trace lengths to the SODIMM connector pads for each signal group in a three or two SO-DIMM design.

3.3.1 MD[63:0] Signals

Figure 3 and Table 6 lists the three SO-DIMM socket trace lengths and illustrates the corresponding topology.

Figure 3. MD[63:0] Topology, Three SO-DIMM Sockets

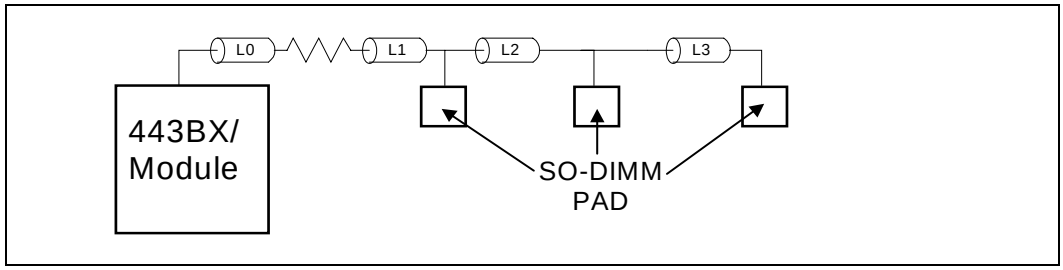


Table 6. MD[63:0] Topology, Three SO-DIMM Sockets - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	0.0 in	1.00 in
L0+L1	1.1 in	N/A
L2+L3	0.0 in	2.75 in
L0+L1+L2+L3	1.1 in	4.25 in

Figure 4 and Table 7 lists the two SO-DIMM socket trace lengths and illustrates the corresponding topology.

Figure 4. MD[63:0] Topology, Two SO-DIMM Sockets

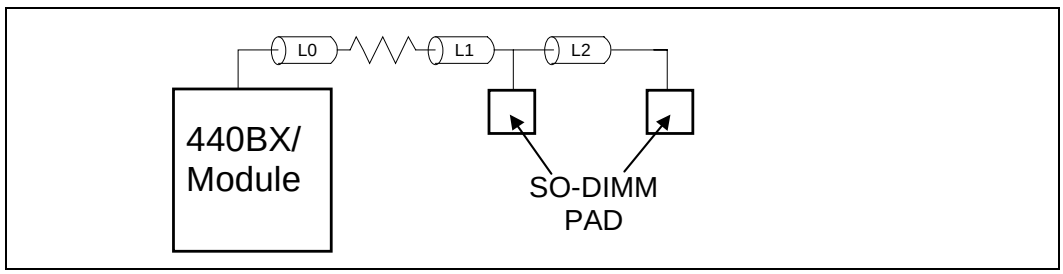


Table 7. MD[63:0] Topology, Two SO-DIMM Sockets - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	0.0 in	1.0 in
L0+L1	1.1 in	N/A
L0+L1+L2	1.1 in	6.0 in

3.3.2 DQMA[7:0] Signals

Figure 5 and Table 8 lists the three SO-DIMM trace lengths and illustrates the corresponding topology.

Figure 5. DQMA [7:0] Topology, Three SO-DIMM Sockets

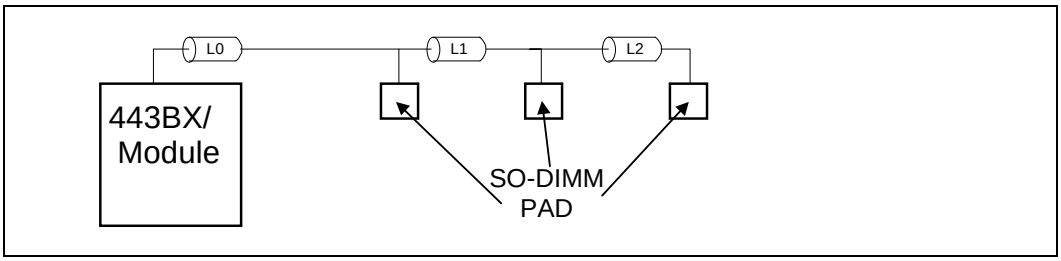


Table 8. DQMA [7:0] Topology, Three SO-DIMM Sockets, Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	1.0	N/A
L0+L1+L2	1.0	4.0

Figure 6 and Table 9 lists the two SO-DIMM trace lengths and illustrates the corresponding topology.

Figure 6. DQMA [7:0] Topology, Two SO-DIMM Sockets

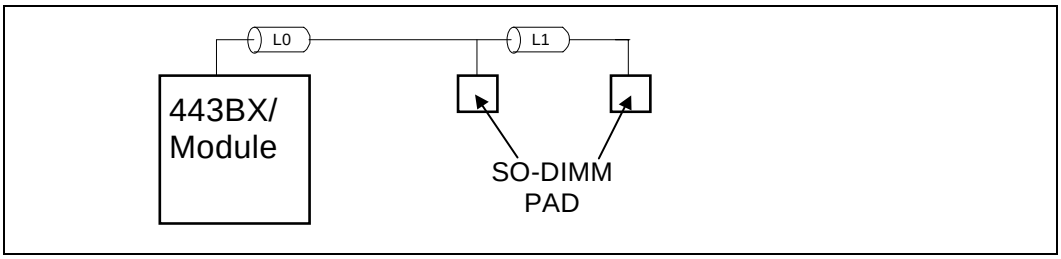


Table 9. DQMA [7:0] Topology, Two SO-DIMM Sockets - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	1.0	N/A
L0+L1	1.0	6.0

3.3.3 Chip Select Signals - CSA[5:0]

Figure 7 and Table 10 lists the Chip Select signals and illustrates the corresponding topology.

Figure 7. CSA [5:0] Topology

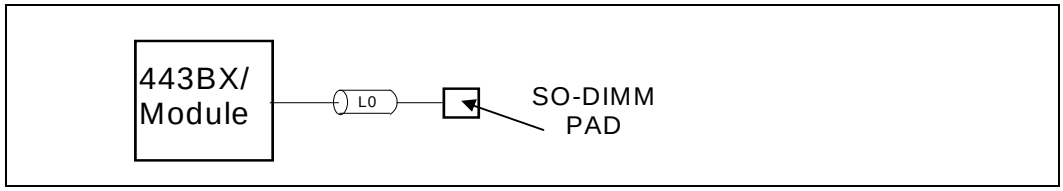


Table 10. CSA[5:0] Topology - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	1.0	6.0

3.3.4 Clock Enable Signals - CKE[5:0]

Figure 8 and Table 11 lists the Clock Enable signals and illustrates the corresponding topology.

Figure 8. CKE[5:0] Topology

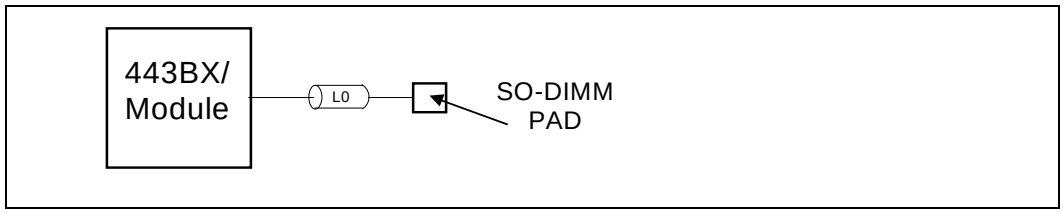


Table 11. CKE[5:0] Topology - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	1.0	6.0

3.3.5 Command Signals - MAB[13:0]x, WEA#, SRASA#, and SCASA

Figure 9 and Table 12 lists the three SO-DIMM trace lengths for the command signals and illustrates the corresponding topology.

Figure 9. Command Signals Topology, Three SO-DIMM

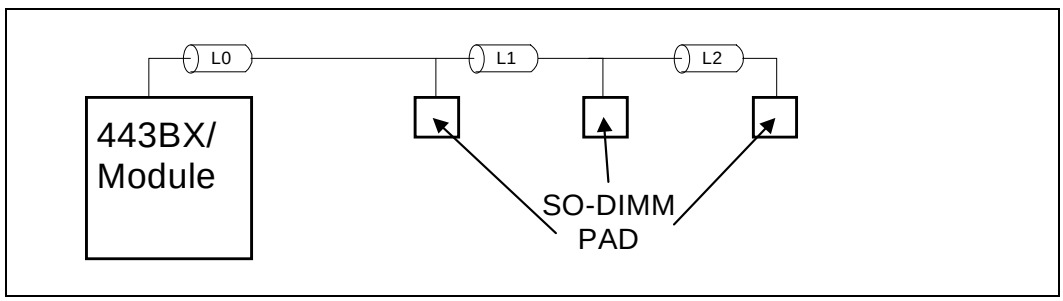


Table 12. Command Signals Topology, Three SO-DIMM - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	1.0	N/A
L0+L1+L2	1.0	6.0

Figure 10 and Table 13 lists the two SO-DIMM trace lengths for the command signals and illustrates the corresponding topology.

Figure 10. Command Signals Topology, Two SO-DIMM

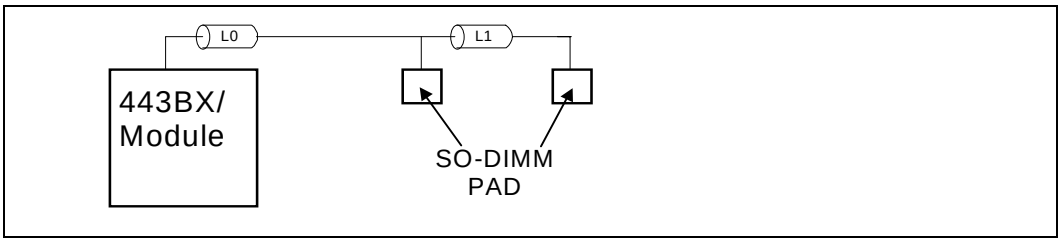


Table 13. Command Signals Topology, Two SO-DIMM - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L0	1.0	N/A
L0+L1	1.0	6.0

3.4 SODIMM DRAM Organization

The 144-pin SODIMM (1” height) has a maximum capacity of eight devices and provides the following configuration possibilities (see Table 14) for SDRAM or EDO.

Table 14. SODIMM DRAM Organization

Technology	SODIMM Organization	Component Organization	Devices per Row	Mbyte per SODIMM
16 Mbit	1 M x 64 / S	1 M x 16	4	8 Mbyte
	2 M x 64 / D	1 M x 16	4	16 Mbyte
	2 M x 64 / S	2 M x 8	8	16 Mbyte
64 Mbit	2 M x 64 / S	2 M x 32	2	16 Mbyte
	4 M x 64 / D	2 M x 32	2	32 Mbyte
	4 M x 64 / S	4 M x 16	4	32 Mbyte
	8 M x 64 / D	4 M x 16	4	64 Mbyte
	8 M x 64 / S	8 M x 8	8	64 Mbyte
128 Mbit	16 M x 64 /S	8 M x1 6	4	128 Mbyte

NOTE: “S” denotes single-sided SODIMMs. “D” denotes double-sided SODIMMs.

3.4.1 64-Mbit SDRAM System Examples

Table 15 lists five system examples. Each example is based on using three SODIMM sockets or one on-board DRAM and two SODIMM sockets. The terms used in Table 15 are defined below:

144 SODIMM: Number of SODIMM sockets plus on-board DRAM
Row: RAS[5:0]# or CS[5:0]# connection.
Technology: DRAM technology 16 Mbit, 64 Mbit
Density/Width: DRAM configuration 16 Mbit: 2 M x 8, or 1 M x 16
64 Mbit: 8 M x 8, 4 M x16, or 2 M x 32
128 Mbit: 8 M x 16, or 16 M x 8
Devices/Row: Number of DRAM components per row.

Table 15. System Examples for Supporting 64-Mbit SDRAM

144 SODIMM	Row	Technology	Density x Width	# Devices/Row	Mbytes per SODIMM
Example #1					
#1 or on-board	0	16 Mbit	2 M x 8	8	16 Mbytes
#2	1	16 Mbit	1 M x 16	4	8 Mbytes
	2	16 Mbit	1 M x 16	4	8 Mbytes
#3	3	16 Mbit	2 M x 8	8	16 Mbytes
Total	4			24	48 Mbytes
Example #2					
#1 or on-board	0	16 Mbit	2 M x 8	8	16 Mbytes
#2	1	16 Mbit	2 M x 8	8	16 Mbytes
#3	2	16 Mbit	2 M x 8	8	16 Mbytes
Total	3			24	48 Mbytes
Example #3					
#1 or on-board	0	16 Mbit	2 M x 8	8	16 Mbytes
#2	1	64 Mbit	8 M x 8	8	64 Mbytes
#3	2	64 Mbit	4 M x 16	4	32 Mbytes
Total	3			20	112 Mbytes
Example #4					
#1 or on-board	0	64 Mbit	8 M x 8	8	64 Mbytes
#2	1	64 Mbit	8 M x 8	8	64 Mbytes
#3	2	64 Mbit	8 M x 8	8	64 Mbytes
Total	3			24	192 Mbytes
Example #5					
#1 or on-board	0	128 Mbit	8 M x 16	4	64 Mbytes
	1	128 Mbit	8 M x 16	4	64 Mbytes
#2	2	128 Mbit	8 M x 16	4	64 Mbytes
	3	128 Mbit	8 M x 16	4	64 Mbytes
#3	4	128 Mbit	8 M x 16	4	64 Mbytes
	5	128 Mbit	8 M x 16	4	64 Mbytes
Total	6			24	384 Mbytes

3.5 SO-DIMM Placement Options

There are many ways to place the SO-DIMMs on the system electronics. The following diagrams illustrate a few of the possibilities. The dotted outline indicates the SO-DIMM socket is on the other side of the board. In all the configurations, the last SO-DIMM (SODIMM0) slot can be replaced by on-board memory.

Figure 11. Three SO-DIMM Slots on One Side (First Two Back-to-Back)

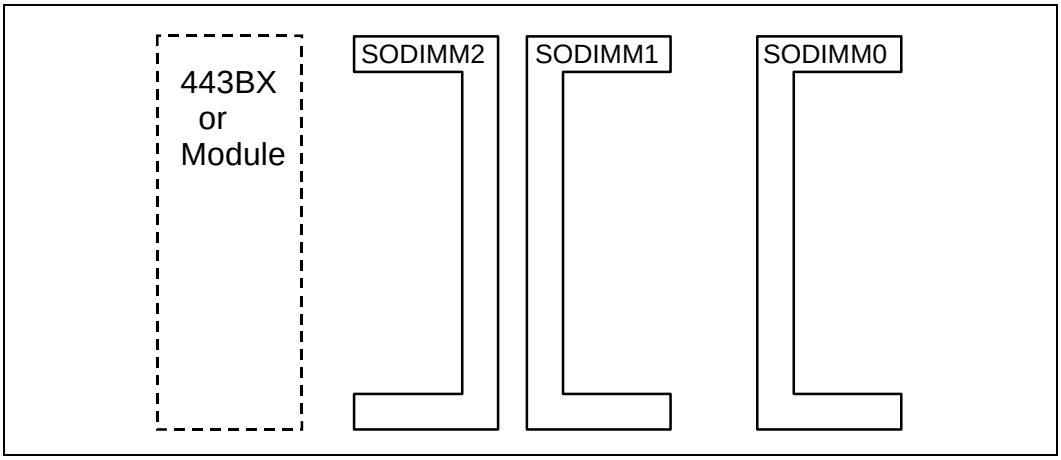


Figure 12. Two SO-DIMM Slots Back-to-Back, Third Slot on the Other Side

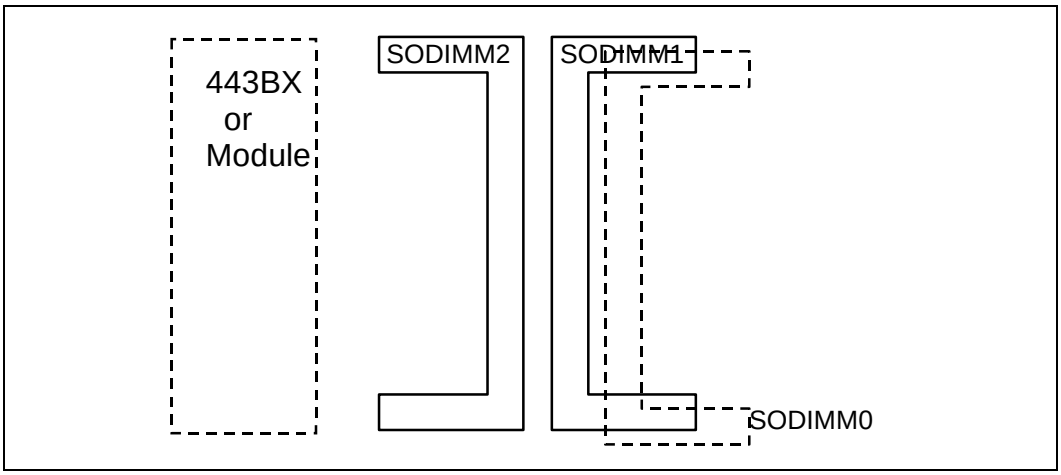


Figure 13. Two SO-DIMM Slots on One Side, Third Slot on the Other Side

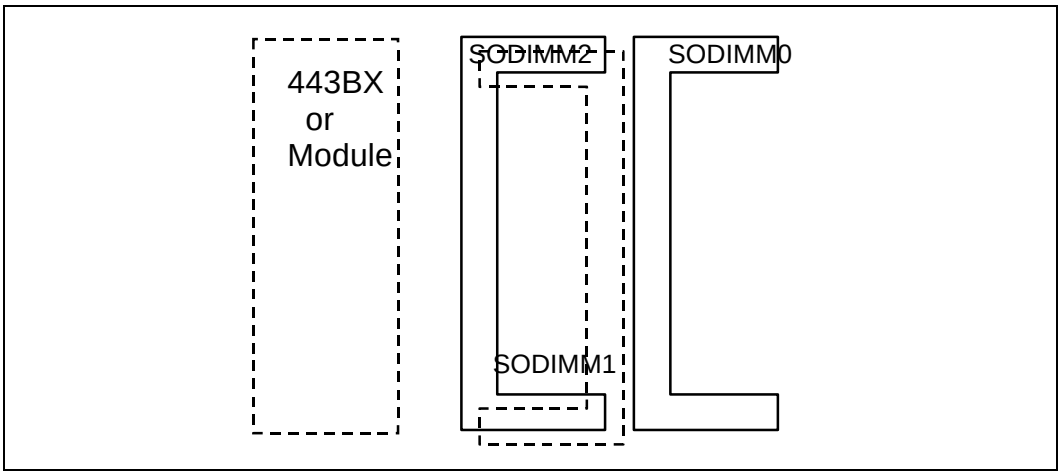
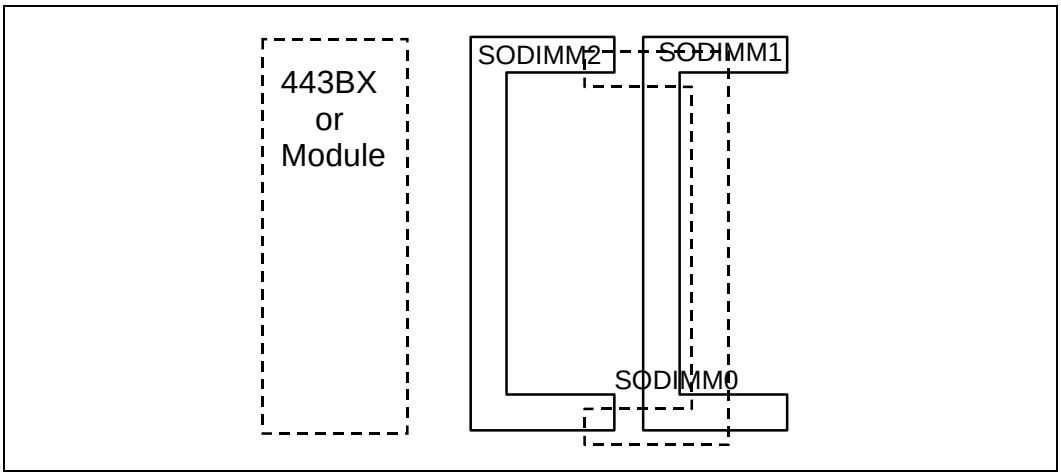


Figure 14. Two SO-DIMM Slots on One Side, Third Slot on the Other Side (Alternate Method)



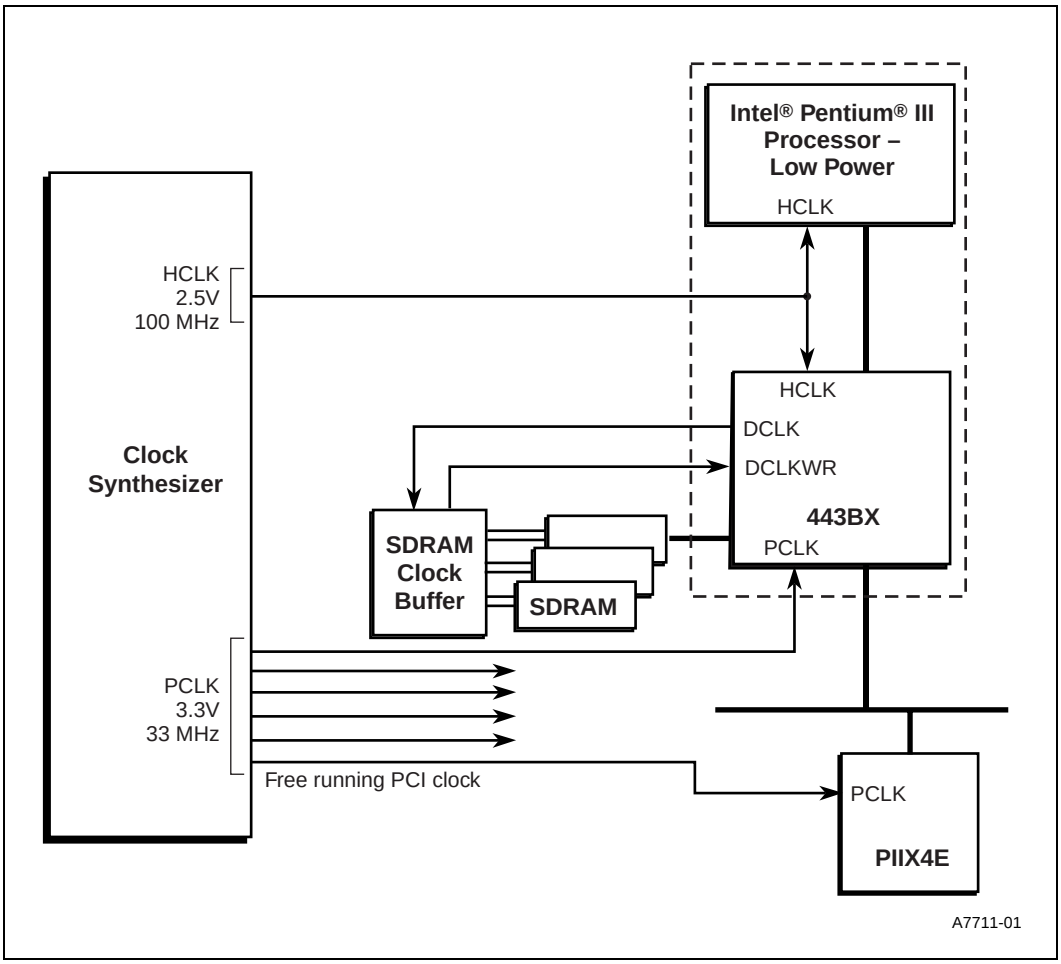
4.0 Clocking Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. The order in which signals are routed will vary from designer to designer. Some designers prefer routing all of the clock signals first, while others prefer routing the high-speed bus signals first. Either order can be used, as long as the guidelines listed here are followed. When the guidelines listed here are not followed, it is very important to simulate the design. Even when the guidelines are followed, it is recommended that you simulate signals for proper signal integrity, flight time and cross talk.

4.1 Clocking System Overview

This section provides guidelines and application information for clock layout in a Low-Power Module/440BX AGPset system. These guidelines are based on the HCLK, PCICLK and SDRAMCLK requirements and should be implemented along with the application instructions supplied by your clock chip vendor. Figure 15 shows the clock synthesizer connection to the processor, 443BX, and SDRAM when using a Low-Power Module.

Figure 15. Clock Connections to the Low-Power Module



4.2 Clock Synthesizer Pinout and Specifications

A clock synthesizer that meets the *CK97 Clock Synthesizer Design Guidelines* (order number 243867) will meet the requirement for a Low-Power Module/440BX AGPset-based system. Table 21 lists clock vendors that provide clock synthesizers which meet the *CK97 Clock Synthesizer Design Guidelines.*

Note: The CK100-M compatible clock synthesizer operates in multi-voltage mode. The processor clocks operate at 100 MHz at 2.5 V, and the PCI clocks operate at 33 MHz at 3.3 V. The CKBF-M compatible clock buffer provides clocks for SDRAM operating at 100 MHz at 3.3 V. See Figure 16 and Figure 17 for more details.

Figure 16. Pinout for CK100-M Compatible Clock Synthesizer

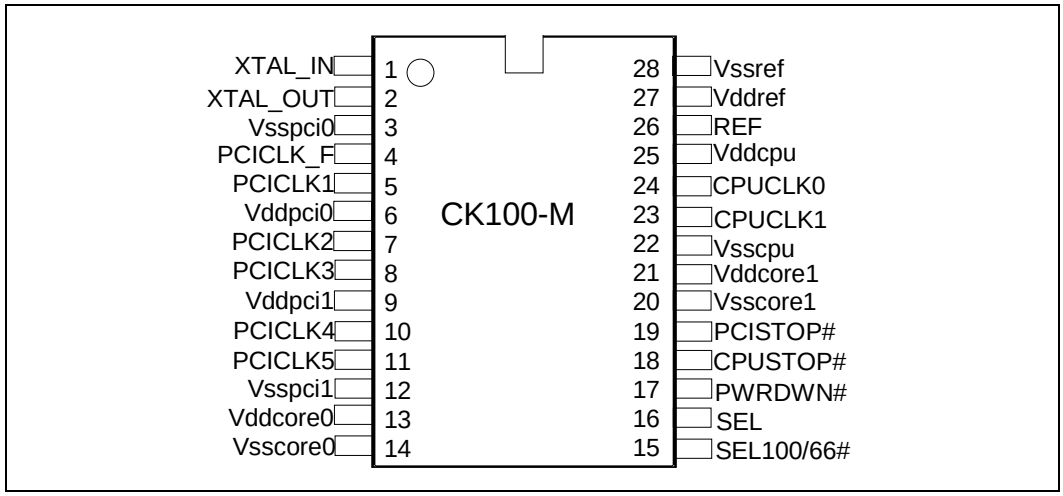
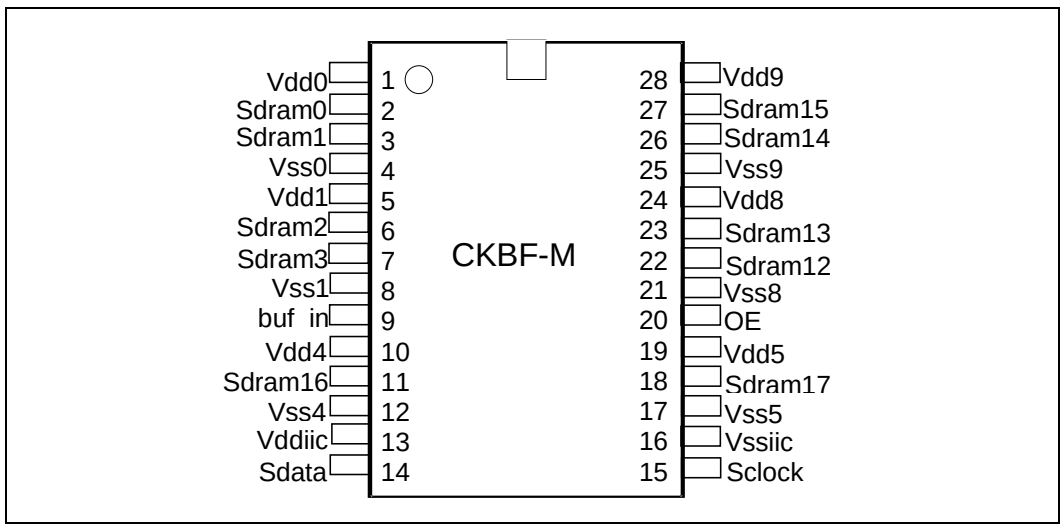


Figure 17. Pinout for CKBF-M Compatible Clock Buffer



4.3 Timing Guidelines

Trace lengths should be matched within clock signal groups to minimize skew between copies of the clocks. This applies to the HCLK-to-HCLK and the PCICLK-to-PCICLK clock trace lengths. Figure 18 shows a simplified clocking layout for the timing specifications. See Table 16 for the clock skews.

Figure 18. Timing Specifications Layout

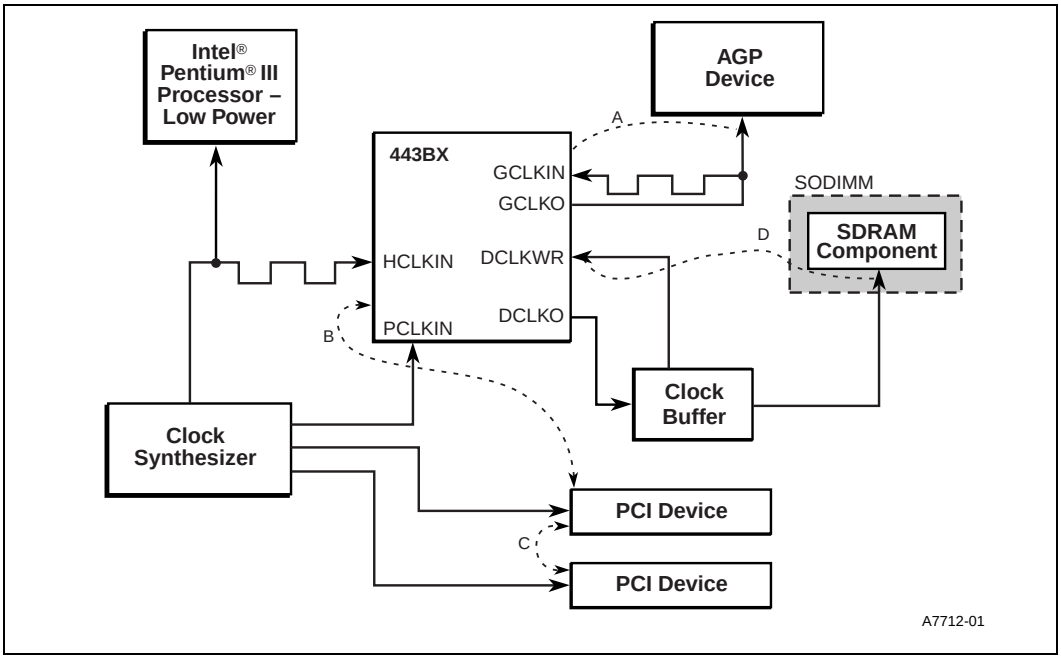


Table 16. Timing Specifications for Maximum and Minimum Clock Skews

Symbol	Description	CK100-M Pin-to-Pin	Boards	Total
A	AGP device (GCLK) to 440BX AGPset (GCLKIN) skew	N/A	100 ps (max) - 100 ps (min)	100 ps (max) - 100 ps (min)
B	440BX AGPset (HCLK) to PCI (PCLK) skew	4.0 ns (max.) 1 1.5 ns (min.)	1.0 ns (max.) 0 ns (min.)	5.0 ns (max.) 1.5 ns (min.)
C	PCI (PCLK) to PCI (PCLK) skew	500 ps (max) - 500 ps (min)	1.5 ns (max) -1.5 ns (min)	2.0 ns (max) - 2.0 ns (min)
D	DCLKWR to SDRAM (SCLK) skew	250 ps (max) -250 ps (min)	380 ps (max) 2 – 380 ps (min) 2	630 ps (max) - 630 ps (min)

NOTES:
1. The 82443BX PCICLK input should lag its HCLK input by a minimum of 1.5 ns to a maximum of 4.0 ns at the pins of the CK100-M device. An integrated buffer offers the best control over these output-to-output drive skews.
2. This skew allowance includes ±280 ps for I/O capacitance and SODIMM routing variation. Motherboards should allow for no more than ±100 ps contribution to the total skew.
3. Use the same clock output pin for both the 443BX HCLK input and the processor clock input in a “T” signal trace configuration.

Note: Clock period, jitter, offset and skew are measured on the rising edge of the clock signals at 1.25 V for the 2.5-V clocks and at 1.5 V for the 3.3-V clocks.

4.4 HCLK Layout Guidelines for the Low-Power Module

The following list provides the HCLK0 guidelines for the Low-Power Module design.

1. A 22-Ω series resistor for impedance matching is required. Place the series resistor as near to the driver pin as possible (within 1 inch).
2. Route HCLK0 on one contiguous internal layer to provide better trace delay consistency, signal integrity, and EMI containment. Intel recommends that this signal be routed as a stripline layer with an adjacent GND plane.
3. A system electronics board nominal trace width should have an impedance of 55 Ω ± 10%. Impedance of a nominal trace width is a key parameter specified to board fabricators. Typically, nominal trace width is constrained by design density, the substrate material, and the board fabrication process. Common trace widths are 4 mils, 5 mils, and 6 mils.
4. HCLK0 should be routed with a trace width twice the width of a nominal trace. This is required to match the impedance of the system electronics to that of the HCLK0 on the module. For example, a board with a nominal trace width of 5 mils would yield an HCLK0 trace width of 10 mils.
5. The target impedance for HCLK0 is 40 Ω. By specifying the impedance of a nominal trace to be 55 Ω ± 10%, the impedance of a trace width twice the width of nominal is constrained to be approximately 40 Ω nominally. This applies to nominal traces of 4 mils, 5 mils, and 6 mils. In all cases, the impedance of the trace routed at twice nominal width (8 mils, 10 mils, and 12 mils) is 40 Ω.
6. The keep-out zone around HCLK0 should be twice the width of the HCLK0 trace, or four times the width of the nominal trace. For example, a design with a nominal trace width of 5 mils would route HCLK0 in a 10-mil trace. The nearest trace to HCLK0 would then be 20 mils away (10 mils * 2).
7. Avoid crossing power or ground plane splits.
8. Do not locate vias within the HCLK0 keep-out area.
9. To generate HCLK0, use either a CK100-M or a CK100-SM compliant part. These parts use buffers that are approximately twice the strength of desktop parts (CK100).
10. The CK100-M/-SM compliant clock part should have its core powered by the +3.3 volt supply (V3_S), which turns off during suspend.
11. Ensure that “V_CLK” (+2.5 volts), which powers the clock buffer, has high-frequency bypass capacitors. Note that “V_CLK” filtering should be located next to the system clock synthesizer.

Figure 19 illustrates the HCLK0 layout guidelines.

Figure 19. Pentium® III Processor Low-Power Module Based Clocking Layout

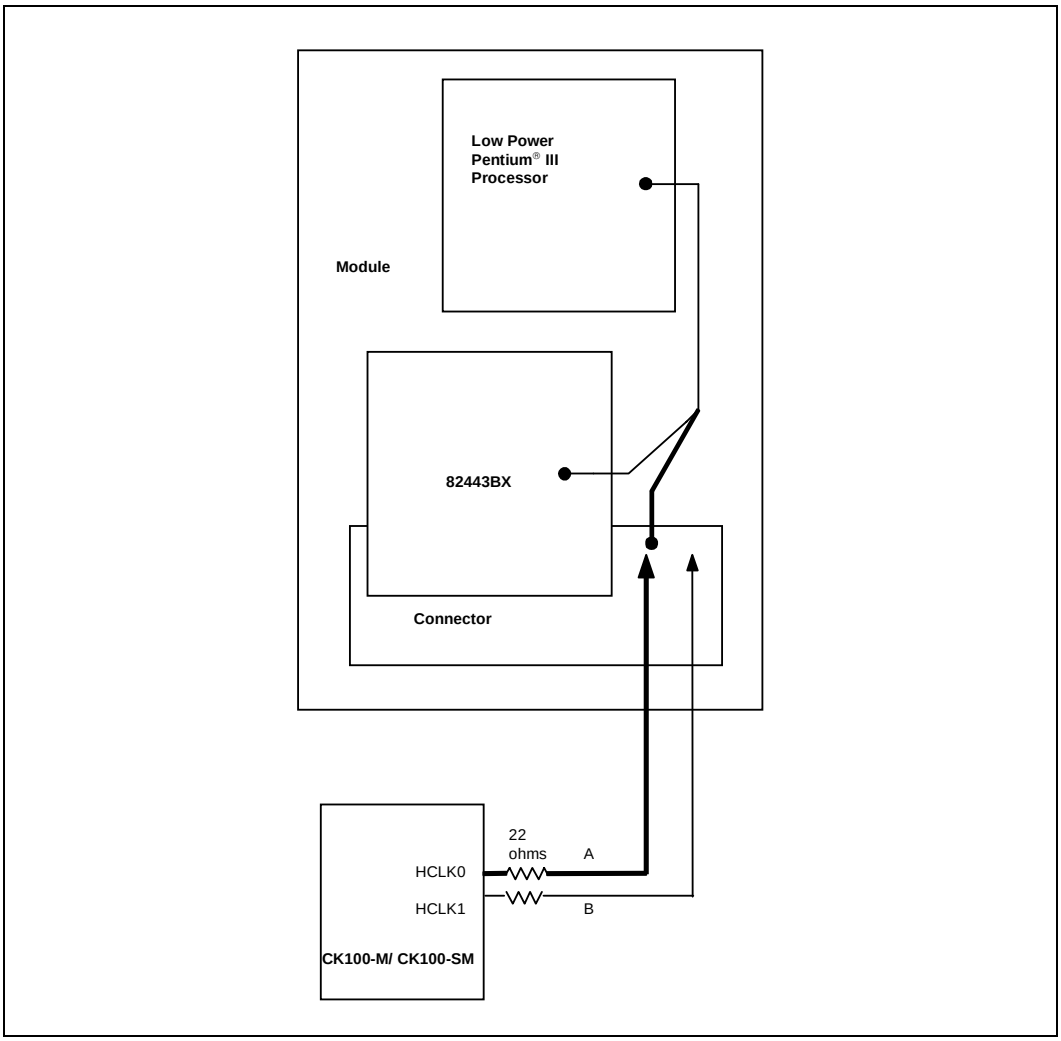


Table 17 lists the clocking trace lengths.

Table 17. Clocking Trace Lengths

Variable	Trace Width	Trace Length (min)		Trace Length (max)		Impedance Target	Resistor
A	Twice the nominal trace width	0.0 in	0.0 mm	4.0 in	101.6 mm	40 Ω	22 Ω ± 5%
B	Nominal trace width	0.0 in	0.0 mm	4.0 in	101.6 mm	55 Ω	22 Ω ± 5%

NOTE: HCLK1 is only used on the instrumented version of the Pentium III Processor Low-Power Module.

4.5 SDRAM Clock Layout Guidelines

This section defines the clock lengths and series termination for 100-MHz SDRAM clocks.

4.5.1 General Clocking Guidelines

The goal of the SDRAM clock guidelines is to route all SDRAM clock signals as near to the same length as possible, not deviating more than 0.2 inches from maximum to minimum.

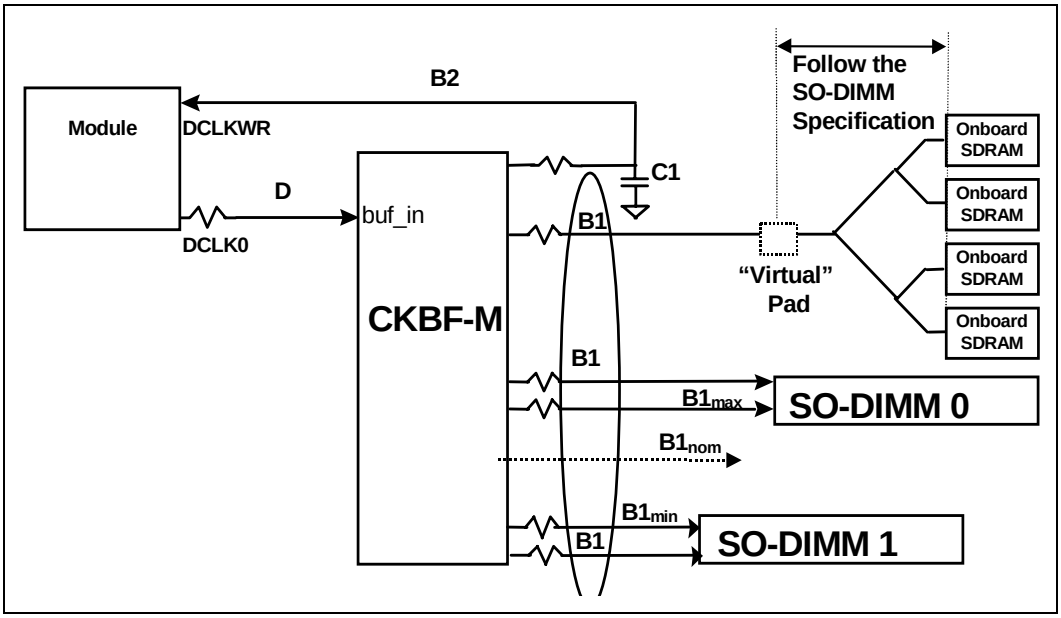
The following list provides design considerations for the SDRAM clocks.

1. Series termination resistors are required. Place them as close to the driver pin as possible (within 1 inch).
2. Route all SDRAM clocks and DCLKWR on the same internal layer to provide better trace delay consistency as well as EMI containment.
3. A system electronics board nominal trace width should have an impedance of 55 Ω ± 10%. Impedance of a nominal trace width is a key parameter specified to board fabricators. Typically, nominal trace width is constrained by design density, the substrate material, and the board fabrication process. Common trace widths are 4 mils, 5 mils, and 6 mils.
4. Minimize the use of vias in clock signals.
5. All clocks should have 1:2 width-to-spacing ratio.

4.5.2 SDRAM Clock Layout Guidelines

Figure 20 shows the SDRAM clock layout guidelines and Table 18 provides the measurement values.

Figure 20. Clocking Layout Diagram



NOTES:
1. B1 represents memory SDRAM clock signals.
2. $B1_{max}$ represents the "Maximum" SDRAM clock trace length.

3. $B1_{nom}$ represents an imaginary “Nominal” SDRAM clock trace length.
4. $B1_{min}$ represents the “Minimum” SDRAM clock trace length.

Intel recommends the following guidelines for SDRAM clock trace length design. The terms used in Figure 20 are mathematically defined as follows:

1. SDRAM clock trace lengths should not differ in length from maximum to minimum by more than 0.2 inches. This means that the longest SDRAM clock trace length ($B1_{max}$) minus the shortest SDRAM clock trace length ($B1_{min}$) should be within 0.2 inches of each other; $B1_{max} - B1_{min} \leq 0.2$ inches.
2. $B1_{nom}$ is an imaginary target nominal SDRAM clock trace length that is centered in length between the maximum and the minimum SDRAM clock lengths. This is defined as:

$$B1_{nom} = B1_{min} + \frac{B1_{max} - B1_{min}}{2}$$

3. B1= $B1_{nom}$ ± 0.1 inches (maximum = $B1_{nom}$ + 0.1 in, minimum = $B1_{nom}$ - 0.1 in).
4. B2 = DCLKWR = $B1_{nom}$ + 2.5 inches ± 0.1 inches (maximum = $B1_{nom}$ + 2.6 in, minimum = $B1_{nom}$ + 2.4 in).

Table 18. SDRAM Clocks and DCLK Trace Lengths

Variable	Trace Zo	Trace Length (min)		Trace Length (max)		Resistor
$B1_{nom}$	N/A	0.0 in	0.0 mm	4.0 in	101.6 mm	N/A
B1	55 Ω ± 10%	$B1_{nom}$ - 0.1 in	$B1_{nom}$ - 2.5 mm	$B1_{nom}$ + 0.1 in	$B1_{nom}$ + 2.5 mm	10 Ω ± 5%
B2	55 Ω ± 10%	$B1_{nom}$ + 2.4 in	$B1_{nom}$ + 61 mm	$B1_{nom}$ + 2.6 in	$B1_{nom}$ + 66.0 mm	22 Ω ± 5%
D	55 Ω ± 10%	0.0 in	0.0 mm	4.0 in	101.6 mm	18 Ω ± 5%
C1	15 pF ± 5%	Use a 0603 package size with an NPO or C0G dielectric and place it within 0.2 inches of the resistor. Route from the resistor pad through the capacitor pad and then into the via going into the system electronics board.				

4.5.3 DCLKWR Layout Guidelines

Intel recommends that a capacitor be added to the system electronics on the DCLKWR signal. Notebook designers should use a capacitor value that will minimize the skew between the SDRAM clocks and the Intel 82443BX component. The capacitor should be placed no more than 0.2 inches from the 22-Ω series dampening resistor. Intel recommends using the topology shown in Figure 21. This allows the capacitor to be removed from a design without creating an open-ended stub on DCLKWR. See Table 19 for section tolerances.

1. Series matching resistors are required. Placement: As near to the driver pin as possible (within 1 inch).
2. Route all clocks on internal layers to provide better trace delay consistency as well as EMI containment.
3. Board impedance should be 55 Ω ± 10%.
4. Minimize the use of vias in clock signals.
5. All clocks should have 1:2 width to spacing ratio.

Figure 21. DCLKWR (Figure 16, Variable B2) Guidelines

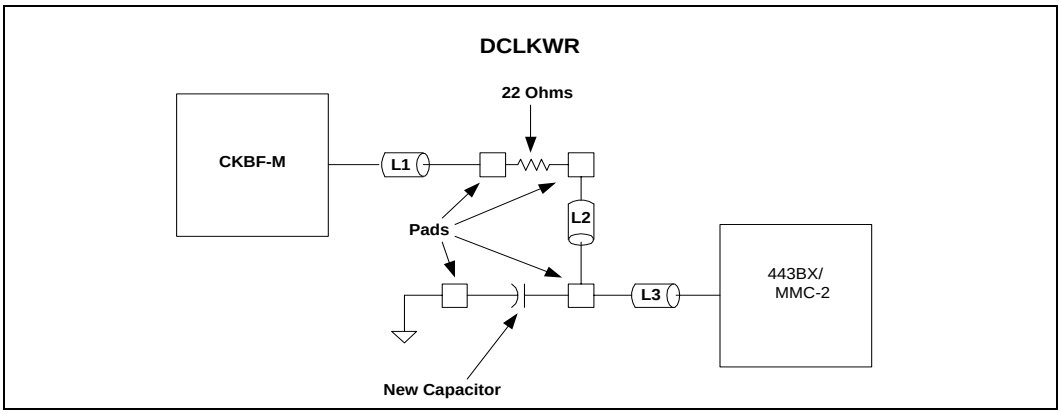


Table 19. DCLKWR Guidelines - Section Tolerances

Section	Minimum (inches)	Maximum (inches)
L1	0.0	1.0
L2	0.0	0.2
L3	N/A	N/A
L1+L2+L3	$B1_{nom}$ +2.4 in	$B1_{nom}$ +2.6 in

4.6 PCI/AGP Clock Layout Guidelines

Figure 22. Low-Power Module Clocking Layout

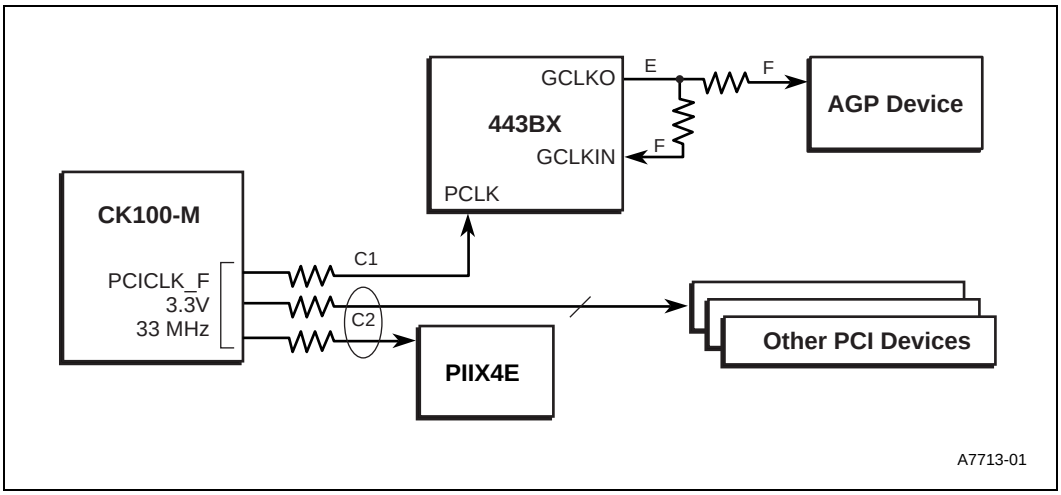


Table 20. PCI and AGP Clock Trace Length

Variable	Trace Width	Minimum Trace Length	Maximum Trace Length	Tolerance	Resistor Value
C_1	5 mil	A	A+4 inch (A+101.6 mm)		33 Ω ± 5%
C_2	5 mil	C_1	C_1	± 4.5 inch (± 114.3mm)	33 Ω ± 5%
E	10 mil	0 inch (0 mm)	1 inch (25.4 mm)		None
F	5 mil	0 inch (0 mm)	8.5 inch (215.9 mm)		18 Ω ± 5%

4.7 Clock Vendors

This vendor list is provided as a service to our customers for reference only. The inclusion of this list should not be considered a recommendation or product endorsement by Intel Corporation.

Table 21. Clock Vendors

Vendor Name	Address
International Microcircuits, Inc.	525 Los Coches Street Milpitas, CA 95035 (408) 263-6300 http://www.imicorp.com
Integrated Circuit Systems, Inc.	1271 Parkmoor Avenue San Jose, CA 95126-3448 (408) 925-9493 http://www.icst.com
Cypress Semiconductor	12020 113th Ave. Northeast Kirkland, WA 98034 (425) 398-3400 http://www.cypress.com

5.0 82443BX AGP Interface for Low-Power Module Design

This section lists guidelines to be followed when routing the signal traces for the board design. Even when the guidelines are followed, it is recommended that you simulate as many signals as possible for proper signal integrity and cross talk. See Section 6.2.10, “AGP Signals” on page 43 for AGP pull-up requirements. See Section 4.0, “Clocking Guidelines” on page 26 for AGP clocking information.

5.1 Layout and Routing Guidelines

For the definition of AGP interface functionality (protocols, rules and signaling mechanisms, and the platform level aspects of AGP functionality), refer to the latest *AGP Interface Specification* and *AGP Platform Design Guide.* This document focuses only on specific 440BX platform recommendations for the AGP interface.

Throughout this section the term “data” refers to G_AD[31:0], G_C/BE[3:0]# and SBA[7:0]. The term “strobe” refers to AD_STB[B:A] and SB_STB. When the term “data” is used, it is referring to one of three groups of data as indicated in Table 22. When the term “strobe” is used it is referring to one of the three strobes as it relates to the data in its associated group.

Table 22. Data and Associated Strobe

Data	Associated Strobe
G_AD[15:0] and G_C/BE[1:0]#	AD_STBA
G_AD[31:16] and G_C/BE[3:2]#	AD_STBB
SBA[7:0]	SB_STB

5.1.1 On-board AGP Compliant Device Layout Guidelines

Longer trace lengths require a greater amount of spacing between traces in order to reduce crosstalk. When using 1:2 spacing, maximum trace length of data lines is 9.5 inches. The line length mismatch is 0.5 inches. The strobe is the longest trace of the group. This restricts the maximum trace length of data lines to less than 4.5 inches for a 1:1 trace spacing. The strobe requires a 1:2 trace spacing. Trace length guidelines given in this section do not reflect signal integrity and EMI. It is recommended that you simulate the routes to ensure that signal quality requirements are met. See Figure 23 for the AGP compliant device layout guidelines and Figure 24 for signal layout recommendations.

Figure 23. On-board AGP Compliant Device Layout Guidelines

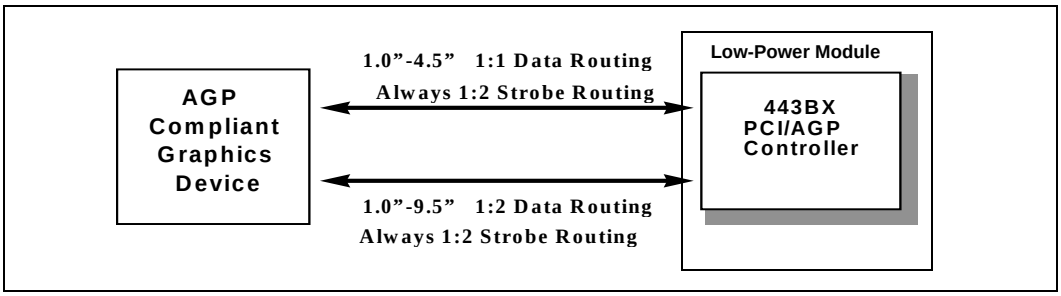
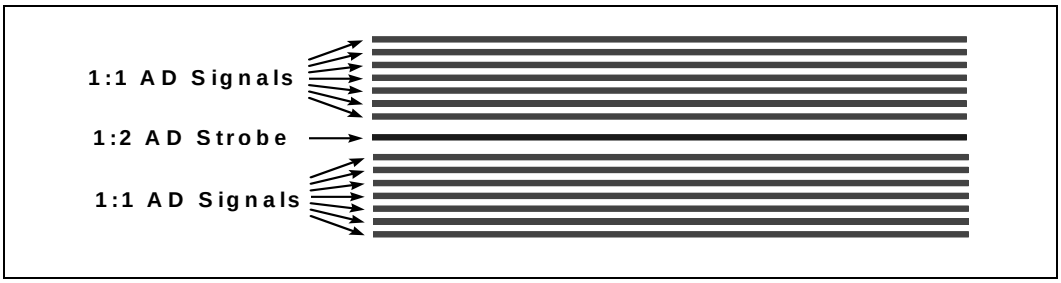


Figure 24. Signal Layout Recommendations



5.1.1.1 Data and Strobe Signal Routing Recommendations

Table 23. Motherboard Recommendations

Width:Space	Trace	Line Length	Line Length Matching
1:1(Data)/1:2(Strobe)	Data /Strobe	1.0 in < line length < 4.5 in	0.5 in, strobe longest trace
1:2	Data/Strobe	1.0 in < line length < 9.5 in	0.5 in, strobe longest trace

The line length mismatch must be less than 0.5” and the strobe must be the longest signal of the group. For example, if the strobe is at 4.0 inches, the data line can be from 3.5 to 4.0 inches in length. It is best to reduce the line length mismatch wherever possible to ensure added margin. The strobe is always required to have 1:2 trace spacing. It is also best to separate the traces by as much as possible in order to reduce the amount of trace-to-trace coupling.

Note: Under certain layouts, crosstalk and ground bounce can be observed on the AD_STB signals of the AGP interface. Although Intel has not observed system failures due to this issue, noise margin has been improved by enhancing the AGP buffers on the 82443BX. For new designs, additional margin can be obtained by following AGP layout guidelines.

5.1.1.2 Control Signal Routing Recommendations

Some of the control signals require pull-up resistors to be installed on the motherboard. Pull-up resistors should be discrete resistors, since resistor packs will need longer stub lengths and may violate timing requirements. The stub length to these pull-up resistors must be controlled. The maximum stub length on a strobe trace is < 0.1 inch. The maximum stub trace length on all other traces is < 0.5 inch. See Table 27 for control signal line length recommendations. For pull-up recommendations, see “AGP Signals” on page 43.

Table 24. Control Signal Line Length Recommendations

Width:Space	Board	Trace	Line Length	Pull-up Stub Length
1:1	Motherboard	Control Signals	1.0 in < line length < 8.5 in	< 0.5 in (Strobes < 0.1 in)
1:2	Motherboard	Control Signals	1.0 in < line length < 10.0 in	< 0.5 in (Strobes < 0.1 in)

5.2 ACPI Compliance Requirements

Based on the Advanced Configuration and Power Interface (ACPI) specification, the AGP graphics device must be ACPI compliant and must implement its self power management circuitry, such as self clock-gating and an idle bus detection mechanism to reduce power. However, in a Pentium III processor-based platform the AGP device clock is a derivative of the host clock.

When the host clock stops (C3 state - Deep Sleep), the AGP clock also stops. An AGP_BUSY# protocol solves this instantaneous AGP stop clock problem. The AGP graphics device must signal the operating system or the south bridge that it is currently busy and the AGP clock should not be stopped.

The AGP device internally protects its core logic to ensure that an illegal clock will not corrupt the AGP device state. This protection gates the internal clock nets used for the device's logic from the time STP_AGP# is asserted until it is deasserted. The STP_AGP# signal is an indication that the AGP clock will not be valid for much longer and should be gated off for protection. STP_AGP# should be connected to the PIIX4E's SUS_STAT1# signal.

The AGP_BUSY# signal indicates that the graphics controller requires the GCLK to be running. This signal should be connected to one of the PIIX4E's PCIREQ# pins. When the PCIREQ# pin must be shared, it can be logically ORed with one of the PIIX4E's PCIREQ# inputs. AGP_BUSY# is an open-drain signal from the graphics device and requires a 10 KΩ pull-up resistor.

AGP_SUSPEND# is for AGP devices that support Suspend mode. The AGP_SUSPEND# signal can be connected to the PIIX4E's SUSB# signal.

5.3 AGP IDSEL Routing

An AGP compliant master is composed of a PCI compliant target interface and an AGP compliant master interface. (Optionally the device can also include a PCI compliant master interface when required.) When used in a PCI mode of operation, the AGP device must provide an external IDSEL that is connected to AD16. When the AGP device is designed for exclusive operation on the AGP interface the device does not have an external IDSEL pin, therefore IDSEL does not need to be routed.

6.0 Design Guideline Checklists

Design checklists provided in this section are intended to be used for schematic reviews of the 500 MHz Low-Power Module-based platform designs. The checklists do not represent the only way to design a system, but do provide recommendations. The system designer should examine the checklist items for correctness. Additional design considerations are also provided.

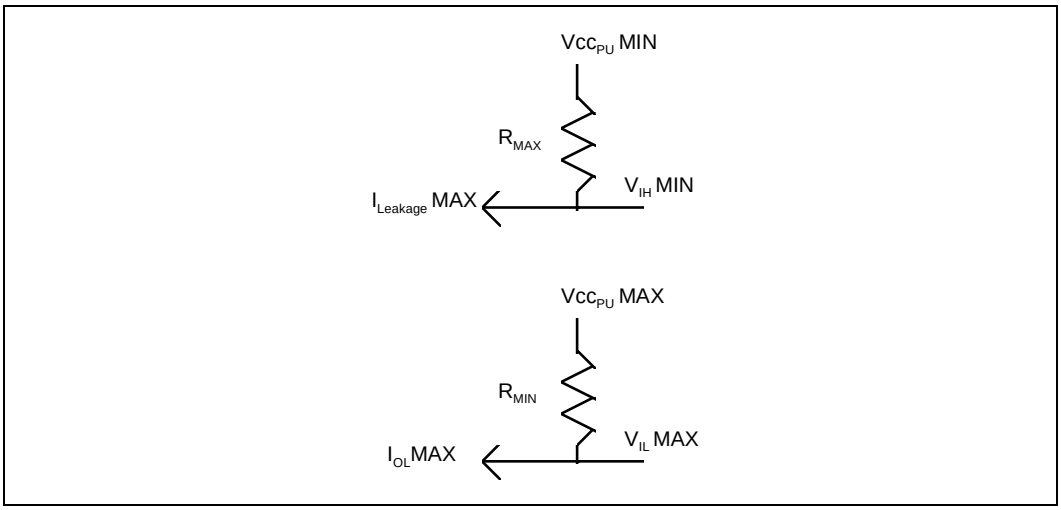
6.1 Resistor Values

Pull-up and pull-down register values are system dependent. The appropriate value for your system can be determined from an AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high/low voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be done to determine the minimum and maximum values that may be used on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications and other considerations. See Figure 25 for an example for a pull-up resistor configuration.

A simplistic DC calculation for a pull-up value is:

$$R_{MAX} = (Vcc_{PU}\ MIN - V_{IH}\ MIN) / I_{Leakage}\ MAX$$
$$R_{MIN} = (Vcc_{PU}\ MAX - V_{IL}\ MAX) / I_{OL}\ MAX$$

Figure 25. Pull-up Resistor Example



6.2 Low-Power Module Design Checklist [ ]Pass, [ ]Fail

For PIIX4E recommendations on the I/O system electronics board, please see "82371EB (PIIX4E) Design Checklist [ ]Pass, [ ]Fail" on page 45.

6.2.1 Low-Power Module Errata

Please see the *Mobile Pentium® III Processor Specification Update* (order number 245306) for workarounds for any errata that may be present on the stepping used.

6.2.2 Power and Ground Pins

- V_DC is the DC voltage driven from the power supply and is required to be 5 V ±5%. The module cannot be inserted or removed while V_DC is powered on.
- V_3S is a SUSB#-controlled 3.3-V voltage supply which is an output of the voltage regulator on the system electronics. This rail should be off during Suspend-to-RAM (STR), Suspend-to-Disk (STD), and Soft-Off (SOff) modes.
- V_5 is a SUSC# controlled 5-V voltage supply which is an output of the voltage regulator on the system electronics. This rail should be off during Suspend-to-Disk (STD), and Soft-Off (SOff) modes.
- V_3 is a SUSC# controlled 3-V voltage supply which is an output of the voltage regulator on the system electronics. This rail should be off during Suspend-to-Disk (STD), and Soft-Off (SOff) modes.
- V_CPUPU is driven by the Low-Power Module to power processor interface signals such as the PIIX4E open-drain pull-ups for the processor/PIIX4E sideband signals.
- V_CLK is driven by the Low-Power Module to power the HCLK drivers from the CK100-M clock source.
- VCCAGP is the VDDQ AGP voltage, and should be connected to V_3.

- V_{TT} is an output of the DC-DC regulator on the Low-Power Module, and is driven to the core voltage (VCC_CORE) of the processor. V_{TT} is used for ITP implementations.
- All unused active low 3.3-V tolerant inputs should be connected to V_3S with a 10-KΩ resistor unless otherwise stated.
- All unused active high inputs should be connected to ground (V_{SS}) through a 10-KΩ resistor unless otherwise stated.

6.2.3 Decoupling Requirements

The placement of sufficient bulk capacitance on the system electronics board is critical to the operation of the Pentium III Processor – Low-Power Module. Intel has provided the maximum possible bulk capacitance on the module. However, in order to achieve proper filtering and in-rush current protection, it is imperative that additional filtering be provided on the system electronics board. Table 25 indicates the minimum bulk capacitance requirements for the system electronics.

Note: Observe the voltage rating requirement for the capacitors on each respective voltage rail.

Table 25. Capacitance Requirement per Power Plane

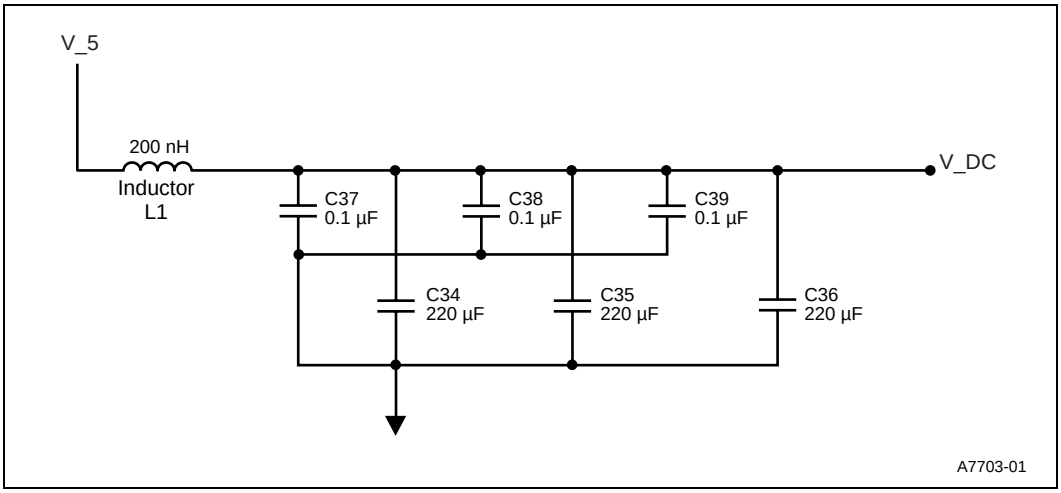
Power Plane	Bulk Capacitance Requirements			High Frequency Capacitance Requirements
	Total Capacitance[4]	ESR[3]	Ripple Current	
V_DC	100 µF	20 mΩ	3 A ~ 5 A	0.1 µF, 0.01 µF[1]
V_5	100 µF	100 mΩ	1 A	0.1 µF, 0.01 µF[1]
V_3	470 µF	100 mΩ	1 A	0.1 µF, 0.01 µF[1]
V_3S	100 µF	100 mΩ	N/A	0.1 µF, 0.01 µF[1]
VCC_AGP	22 µF	100 mΩ	1A	0.1 µF, 0.01 µF[1]
V_CPUPU	2.2 µF	N/A	N/A	8200 pF[1]
V_CLK	10 µF	N/A	N/A	8200 pF[2]

NOTES:
1. Placement of the above capacitance requirements should be located near the connector.
2. V_CLK filtering should be located next to the system clock synthesizer.
3. In order to reduce ESR, Intel recommends the use of multiple bulk capacitors rather than a single large capacitor.
4. Intel strongly recommends that customers pay close attention to capacitor design considerations. Specifically, the “Capacitance vs. Temperature De-rating Curve,” “Capacitance vs. Applied DC Voltage De-rating Curve,” and the “Capacitance vs. Frequency De-rating Curve.” Some capacitor dielectrics are particularly susceptible to these conditions, for example Y5V ceramic capacitors.

6.2.3.1 V_DC and V_5 Decoupling

If V_DC and V_5 are tied together, ensure that decoupling guidelines are strictly followed to avoid noise from the V_DC rail coupling to the V_5 rail. Noise could trigger the undervoltage lockout circuits on the module. Figure 26 is an example of an LC decoupling circuit.

Figure 26. V_DC to V_5 Decoupling



Exact component values are system dependent. Intel recommends that specific component values be determined through full simulation and parasitic modeling.

6.2.4 Clock and Test Signals

- See “Clocking Guidelines” on page 26 for clocking guidelines.
- Use discrete resistors for the HCLK signals from the CK100-M. Do not mix HCLK, and PCLK signals coming from the CK100-M in resistor packs.
- FQS should be connected to the SEL pin of the CK100-M to provide the host clock frequency. CKBF-M should be on the V_3 rail and the CK100-M should be on the V_3S rail.
- The clock signal from the CKBF-M to the SO-DIMM should have 10 Ω series termination resistors.
- CONFIG[1] should be pulled to V_3ALWAYS with a 100-KΩ resistor on the system I/O.
- CONFIG[2] should be pulled to GND in all 440BX AGPset based designs. A weak 100-KΩ resistor may be used.

See Table 26 for clock and test signal resistor values.

Table 26. Clock and Test Signal Resistor Values (Sheet 1 of 2)

Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω)
HCLK	22 (see above)	None
PCLK	33 (see above)	None
DCLKO	18	None
DCLKWR	22	None

Table 26. Clock and Test Signal Resistor Values (Sheet 2 of 2)

GCLKO	18	None
GCLKIN	18	None
SDRAM_CLK	10	None
FQS	None	None

6.2.5 SDRAM Signals

- See "Memory Guidelines" on page 14 for memory guidelines.
- MD[63:0] should have 10 Ω series termination resistors.

See Table 27 for SDRAM signal resistor values.

Table 27. SDRAM Signal Resistor Values

Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω)
MD[63:0]	10	None

6.2.6 Module Strapping Options

- MAB9# is the AGP Disable strapping option on the Low-Power Module. This pin should be pulled up to V_3 with a 10-KΩ resistor when the AGP is disabled.

See Table 28 for low-power module strapping options.

Table 28. Low-Power Module Strapping Options

Pin Name	Function	Low	High	Internal Resistor	Status Register
MAB9#	AGP Disable	AGP Enabled	AGP Disabled	Pull-down	PMCR[1]

6.2.7 PCI Bus Signals

- See "PCI Bus Signals" on page 46.
- The Low-Power Module supports only 3.3-V PCI.
- An 8.2 KΩ – 10 KΩ pull-up to V_3S should be placed on the CLKRUN# signal.
- The 82443BX does not implement the PERR# pin. Data parity errors are still detected and reported on SERR# (when enabled by SERRE and PERRE).

6.2.7.1 PCI Design Considerations

The 82443BX supports up to five PCI masters with its REQ[4:0]#/GNT[4:0]# pairs. The PCI bus supports up to 10 PCI loads. The 82443BX and the PIIX4E each represent one load; other PCI components soldered on the motherboard add one load each; and each PCI connector adds approximately two loads. A design with four PCI slots and no motherboard devices uses all available PCI loads. When all five REQ[4:0]#/GNT[4:0]# pairs are used, simulation is required to ensure that the PCI Bus Specification Rev. 2.1 timings are met. It is recommended, per the PCI specification, that the design have series resistors (~100 Ω) on each of the PCI connector IDSEL lines. See Table 29 for PCI bus signal resistor values.

Table 29. PCI Bus Signal Resistor Values

Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω)
AD[31:0]	None	None
C/BE[3:0]#	None	None
FRAME#	None	10 K pull-up to V_3S
DEVSEL#	None	10 K pull-up to V_3S
IRDY#	None	10 K pull-up to V_3S
TRDY#	None	10 K pull-up to V_3S
STOP#	None	10 K pull-up to V_3S
REQ[4:0]#	None	10 K pull-up to V_3S if unused
GNT[4:0]#	None	10 K pull-up to V_3S if used
PHOLD#	None	10 K pull-up to V_3S
PHLDA#	None	10 K pull-up to V_3S
PAR	None	None
SERR#	None	10 K pull-up to V_3S
CLKRUN#	None	8.2 ~ 10 K pull-up to V_3S
PCIRST#	33 (see “PCI Bus Signals” on page 46)	None
PLOCK#	None	10 K pull-up to V 3S

6.2.8 Processor/PIIX4E ISA Bridge Sideband Signals

- Pull-ups to V_CPUPU: INIT# - 1 KΩ, STPCLK# - 680 Ω; LINT1#/NMI, LINT0#/INTR, IGNNE#, A20M#, SMI# - 4.7 KΩ. These are open collector outputs from the PIIX4E component.
- CPURST can be left unconnected for Low-Power Module designs.
- Refer to the *System Management Bus Specification* (see Table 2) for descriptions and specifications of the three SMBus signals: SMBALERT#, SMBCLK, and SMBDATA. A pull-up resistor is required. Values will vary depending on V_{DD} and the actual capacitance of the bus.

See Table 30 for sideband signal resistor values.

Table 30. Sideband Signal Resistor Values (Sheet 1 of 2)

Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω)
FERR#	None	1.5 K pull-up to V_CPUPU if used
CPURST	None	None
IGNNE#	None	1.5 K pull-up to V_CPUPU
INIT#	None	1 K pull-up to V_CPUPU
INTR	None	1.5 K pull-up to V_CPUPU
NMI	None	1.5 K pull-up to V_CPUPU

Table 30. Sideband Signal Resistor Values (Sheet 2 of 2)

A20M#	None	1.5 K pull-up to V_CPUPU
SMI#	None	1.5 K pull-up to V_CPUPU
STPCLK#	None	680 pull-up to V_CPUPU

6.2.9 Power Management Signals

- MID[3:0] should have a 100 KΩ pull-up to V_3S.
- BXPWROK must transition from inactive (low) to active (high) a minimum of 1 ms after BX_VCC is within the specified Functional Operating Range. See “82443BX Host Bridge/ Controller Power Sequencing” on page 75 for more information.

See Table 31 for power management signal resistor values.

Table 31. Power Management Signal Resistor Values

Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω)
SUS_STAT#	None	None
VR_ON	None	None
VR_PWRGD	None	None
SM_CLK	None	Refer to the *System Management Bus Specification*
SM_DATA	None	Refer to the *System Management Bus Specification*
ATF_INT#	None	Refer to the *System Management Bus Specification*
MID[3:0]	None	100 K pull-up to V_3S

6.2.10 AGP Signals

- See “82443BX AGP Interface for Low-Power Module Design” on page 34.
- The MAB9# strapping option for the 443BX is on the I/O system electronic board. This allows the designers to enable or disable the AGP.
- When the AGP is disabled all AGP signals are three-stated and isolated. They do not need external pull-up resistors.
- Unconnected pins on a disabled AGP interface: PIPE#, SBA[7:0], RBF#, ST[2:0], AD_STBA, AD_STBB, SB_STB, G_FRAME#, G_IRDY#, G_TRDY#, G_STOP#, G_DEVSEL#, G_REQ#, G_GNT#, G_AD[31:0], G_C/BE[3:0]#, G_PAR.
- The AGP graphic card must be able to signal the operating system, or the south bridge, that it is currently busy and the AGP clock should not be stopped. See “ACPI Compliance Requirements” on page 36.
- The LOCK# signal is not supported on the AGP interface, even for PCI operations.
- AGP signals that require pull-ups should use discrete resistors not resistor packs.
- When the AGP is enabled the following AGP signals must have pull-up resistors of approximately 8.2 KΩ to VCCAGP to ensure they contain stable values when no agent is actively driving the bus: G_FRAME#, G_TRDY#, G_IRDY#, G_DEVSEL#, G_STOP#, SERR#, PERR#, RBF#, INTA#, INTB#, PIPE#, G_REQ#, G_GNT#, SB_STB, AD_STBA, AD_STBB.

- GPAR requires a 100 KΩ pull-down resistor when the design is interfacing to an AGP connector, or when the AGP compliant device uses PIPE# or side band addressing. When the AGP compliant device uses GFRAME# only, the pull-down resistor is not needed.
- When side band addressing is disabled, SBA[7:0] are isolated and no external pull-ups are required.
- When PIPE# is used to queue addresses the master is not allowed to queue addresses using the side band addressing bus.
- No external termination (for signal quality) is required by the specification. Termination can be added to improve signal integrity, provided that performance (timing) constraints are still satisfied.
- AGP interrupts may be shared with PCI interrupts similar to the recommendations in the PCI Revision 2.1 specification. For example, in a system with three PCI slots and one AGP, interrupts should be connected such that each of the four INTA# lines connects to a unique input on the PIIX4E. It is recommended that the interrupts be staggered. It is also recommended that each PIRQ be programmed to a different IRQ, if possible.
- The system electronics board designer must properly interface the AGP interrupts to the PCI bus.
- In order to minimize the impact of any impedance mismatch between the system electronics board and the add-in card, an impedance of 55 Ω ± 10% is strongly recommended.
- The AGP strobe signals must be grouped with their associated data signals. AD_STBA with G_AD[15:0], AD_STBB with G_AD[31:16], SB_STB with SBA[7:0]. See Section 5.1, “Layout and Routing Guidelines” on page 34.
- Some onboard AGP devices may require their own VREF. This should be generated locally from the AGP interface VCCAGP rail. You should use a separate voltage divider from the AGP_REF for 82443BX. Do not connect the two. The VCCAGP rail is the AGP controller I/O ring voltage supply.

See Table 32 for AGP signal resistor values.

Table 32. AGP Signal Resistor Values (Sheet 1 of 2)

Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω)
GAD[31:0]	None	None
GC/BE[3:0]#	None	None
GFRAME#	None	8.2 K pull-up to VCCAGP
GDEVSEL#	None	8.2 K pull-up to VCCAGP
GIRDY#	None	8.2 K pull-up to VCCAGP
GTRDY#	None	8.2 K pull-up to VCCAGP
GSTOP#	None	8.2 K pull-up to VCCAGP
GREQ#	None	8.2 K pull-up to VCCAGP
GGNT#	None	8.2 K pull-up to VCCAGP
GPAR	None	100 K pull-down (If AGP device does NOT use GFRAME# ONLY)
PIPE#	None	8.2 K pull-up to VCCAGP
SBA[7:0]	None	None
RBF#	None	8.2 K pull-up to VCCAGP

Table 32. AGP Signal Resistor Values (Sheet 2 of 2)

Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω)
ST[2:0]	None	None
ADSTB[B:A]	None	8.2 K pull-up to VCCAGP
SBSTB	None	8.2 K pull-up to VCCAGP

6.3 82371EB (PIIX4E) Design Checklist [ ]Pass, [ ]Fail

6.3.1 82371EB (PIIX4E) Errata

- Please see the *82371EB (PIIX4E) PCI ISA IDE Xcelerator Specification Update* for workarounds or any errata that may be applicable to the stepping used.

6.3.2 Power and Ground Pins

- V_3ALWAYS is a 3.3-V rail that is connected to V_{CC}(SUS) of the PIIX4E. V_3ALWAYS should power off only when the system is mechanically off.
- V_{CC} and V_{CC}(USB) must be tied to V_3S. V_{CC}(USB) should be tied to the same voltage rail as the PIIX4E core.
- V_{CC}(RTC) should be tied to the 3.3-V supply voltage for the RTC logic.
- V_{REF} must be tied to 5 V in a 5-V tolerant system. This signal must power up before or simultaneous to V_3S, and it must power down after or simultaneous to V_3S. Note that most IDE devices operate at 5 V, so even when running a 3.3-V PCI bus, the PIIX4E IDE interface must be 5-V tolerant.
- V_{REF} can be tied to V_3S in a non-5-V tolerant system. IDE devices are generally 5-V devices.
- Tie V_{SS} and V_{SS}(USB) to ground.
- All unused active low 3.3-V tolerant inputs should be connected to V_3S with a 10-KΩ resistor unless otherwise stated.
- All unused active high inputs should be connected to ground (V_{SS}) through a 10-KΩ resistor unless otherwise stated.

See Table 33 for PIIX4E power signal pin assignments.

Table 33. PIIX4E Power Signal Pin Assignments

Power Pins	Ball Number
VCC	E9, E11, E12, E16, F5, F6, F14, F15, G6, P15, R6, R7, R15, T6
VCC(RTC)	L16
VCC(SUS)	N16,R16
VCC(USB)	K5
VSS(USB)	J5
VSS	D10, E7, E13, J9-J12, K9-K12, L9-L12, M9-M12

6.3.3 Clock and Test Signals

- USB Clock - A 48 MHz clock with a duty cycle of better than 40/60% should be fed into the PIIX4E's USB clock input, pin L3.
- Place a 10-KΩ pull-up resistor on TEST# to V_3ALWAYS. Test signals reside in the Suspend/ Resume well.
- In a Pentium III processor-based system, CONFIG[1] should be pulled to V_3ALWAYS with a 100-KΩ resistor.
- CONFIG[2] should be pulled to GND with a 100-KΩ resistor in all 440BX AGPset-based designs.

See Table 34 for clock and test signal resistor values.

Table 34. Clock and Test Signal Resistor Values

Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω)
TEST#	None	10 K Pull-up to V_3ALWAYS
CONFIG[1]	None	100 K Pull-up to V_3ALWAYS
CONFIG[2]	None	100 K Pull-down

6.3.4 PCI Bus Signals

- All unused general purpose inputs (GPIs) should be pulled to a valid logic level with a 10-KΩ resistor. When pulled high, they should be pulled to V_3S except for the GPIs that are in the V_{CC}(SUS) well.
- All unused outputs can be left as no-connects.
- All IDSEL signals should have a 100-Ω series resistor at each device.
- In a 5-V PCI environment, place 2.7 KΩ pull-up resistors to 5 V on PIRQ[A:D]#, SDONE, SBO#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, SERR#, REQ64# and ACK64# on the PCI bus.
- Place the 10-KΩ pull-up resistors to V_3S on PCIREQ[D:A]# and REQ[A:C]# when these signals are unused or when using a PCI add-in slot to insure that these signals do not float.
- In a 3.3-V PCI environment, place 10-KΩ pull-up resistors to V_3S on PIRQ[A:D]#, SDONE, SBO#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, SERR#, REQ64# and ACK64# on the PCI bus.
- For all new designs, make sure that the PIIX4E does not connect IDSEL to AD12, becoming device 1. On 82443BX, AGP is known as device 1 whether disabled or not. Connect IDSEL from PIIX4E to AD18.
- For systems in which the PCIRST# signal is lightly loaded (<50 pF), place a 33-Ω series termination resistor on this signal. This resistor should be placed as close as possible to the PIIX4E.
- See Table 35 for PCI bus signal resistor values.

Table 35. PCI Bus Signal Resistor Values

Name	Termination Resistor (Ω)	Pull-up (pull-down) Resistor (Ω)
Unused GPIs	None	10 K to a valid level
IDSEL signals	100	None
PIRQ[A:D]#	None	10 K Pull-up to V_3S
SDONE	None	10 K Pull-up to V_3S
SBO#	None	10 K Pull-up to V_3S
FRAME#	None	10 K Pull-up to V_3S
TRDY#	None	10 K Pull-up to V_3S
STOP#	None	10 K Pull-up to V_3S
IRDY#	None	10 K Pull-up to V_3S
DEVSEL#	None	10 K Pull-up to V_3S
PLOCK#	None	10 K Pull-up to V_3S
PERR#	None	10 K Pull-up to V_3S
SERR#	None	10 K Pull-up to V_3S
REQ64#	None	10 K Pull-up to V_3S
ACK64#	None	10 K Pull-up to V_3S
PCIREQ[D:A]#	None	10 K Pull-up to V_3S
REQ[A:C]#	None	10 K Pull-up to V_3S

6.3.5 ISA/EIO Signals

- When implementing Power On Suspend (POS) mode, ISA signals should be pulled up to V_3S. Otherwise use V_5S.
- Use 4.7 KΩ pull-up resistors on SD[15:0], MEMR#, MEMW#, IOR#, IOW#, IOCS16#.
- Use 1 KΩ pull-up resistors on IOCHRDY, MEMCS16#, REFRESH#, ZEROWS#.
- Use 10 KΩ pull-up resistors on IRQ*x*. IRQ8# resides in the V_{CC}(SUS) well, it must be pulled to V_3ALWAYS. When IRQ8# is not used, its default is GPI[6] and it requires a 10 KΩ external pull-up resistor.
- Use a 4.7 KΩ pull-down resistor on DRQ*x*.
- When using the EIO bus, IOCHK# becomes a general-purpose input and in ISA, IOCHK# requires a 4.7 KΩ pull-up resistor.

See Table 36 for ISA/EIO signal resistor values.

Table 36. ISA/EIO Signal Resistor Values (Sheet 1 of 2)

Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω)
SD[15:0]	None	4.7 K Pull-up to V_3S
MEMR#	None	4.7 K Pull-up to V_3S
MEMW#	None	4.7 K Pull-up to V_3S
IOR#	None	4.7 K Pull-up to V_3S
IOW#	None	4.7 K Pull-up to V_3S

Table 36. ISA/EIO Signal Resistor Values (Sheet 2 of 2)

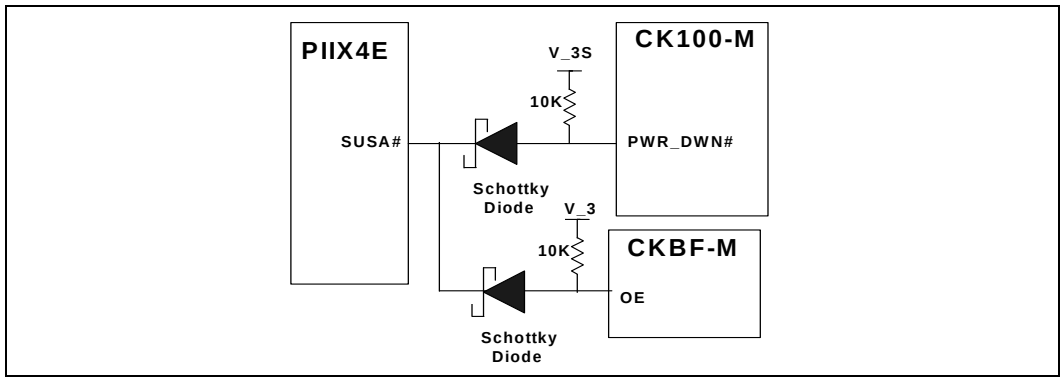
Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω)
IOCS16#	None	4.7 K Pull-up to V_3S
IOCHRDY	None	1 K Pull-up to V_3S
MEMCS16#	None	1 K Pull-up to V_3S
REFRESH#	None	1 K Pull-up to V_3S
ZEROWS#	None	1 K Pull-up to V_3S
IRQx	None	10 K Pull-up to V_3S (see above)
DRQx	None	4.7 K (Pull-down)
SIRQ	None	10 K Pull-up to V_3S
IOCHK#	None	4.7 K Pull-up (if using ISA bus)

6.3.6 Power Management Signals

- Power management signals that reside in the V_{CC}(SUS) well may require pull-ups, the pull-ups must be connected to V_3ALWAYS. These signals do not support 5-V input levels.
- EXTSMI# is an input at reset and an open drain output when activating an SMI# within the Serial IRQ function. Designers may need an 8.2 KΩ pull-up to V_3ALWAYS when it is not always being driven to a valid state.
- When CLKRUN# is not connected between the PIIX4E and the 82443BX, it should be tied low through a 100 Ω resistor at the 82443BX. When CLKRUN# is connected between the PIIX4E and the 82443BX, an 8.2 KΩ – 10 KΩ pull-up to V_3S should be placed on the CLKRUN# signal.
- SUS_STAT1# is connected between the 82443BX and the PIIX4E.
- SUS_STAT2# is connected from the PIIX4E to the devices that must be informed of the stopping of the clocks.
- PCI_STP# is connected to the clock synthesizer to stop the PCI clocks.
- CPU_STP# is connected to the clock synthesizer to stop the processor clock.
- SUSA# is connected to the clock synthesizer's PWR_DWN# pin through a Schottky diode with a 10 KΩ pull-up resistor. Alternatively, SUSA# may be used to control the clock synthesizer's power plane.

See Figure 27 for the clock design block diagram and Table 37 for power management signal resistor values.

Figure 27. Clock Design Block Diagram



- SUSB# and SUSC# are used to control the power planes.
- THRM# is connected to the thermal protection logic.
- PCIREQ[D:A]# is connected between the PIIX4E and the PCI bus. Bus master requests are considered to be power management events.
- Connect RI# to the modem when this feature is used.
- Connect BATLOW# to the battery monitoring logic when this feature is implemented.
- Connect LID to the lid monitoring logic of the system.
- PWRBTN# is connected to logic that allows the user to switch from and to suspend.
- RSMRST# is connected to a switch to allow a complete system reset. This signal resides in the V_{CC}(RTC) well. Its potential must not exceed that of V_{CC}(RTC).

Table 37. Power Management Signal Resistor Values

Name	Damping Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω)
EXTSMI#	None	See above
CLKRUN#	None	8.2 KΩ~10 KΩ Pull-up to V_3S (if connected from PIIX4E to 82443BX) 100 KΩ (pull-down) otherwise

6.3.7 USB Interface

- Refer to the *PIIX4 USB Design Guide* (see Table 2) for the layout recommendations for USB, clock, over-current detection circuit and general board layout recommendations.

6.3.8 IDE Interface

See Table 38 for IDE interface signal resistor values.

- 5.6 KΩ pull-down resistors on PDDREQ and SDDREQ.
- 1 KΩ pull-up resistors on PIORDY and SIORDY.
- 470 Ω pull-down resistor on pin 28 of the IDE connector (CSEL). Support Cable Select (CSEL) is a PC97 requirement. The state of the cable select pin determines the master/slave configuration of the hard drive at the end of the cable.
- The primary IDE connector uses IRQ14, and the secondary IDE connector uses IRQ15.

- The ATA-4 specification requires 33 Ω series terminating resistors on P/SDIOR, P/SDIOW#, P/SDCS[1,3]#, P/SDA[2:0], P/SDDACK# and P/SDD[15:0]. These series termination resistors should be placed as close as possible to the PIIX4E.
- For Ultra-DMA enabled systems, the ATA-4 specification also requires 82 Ω series terminating resistors on P/SDDREQ, INTRQx and P/SIORDY. These series terminating resistors should be placed as close as possible to the PIIX4E.
- When the distance between the PIIX4E and connector is greater than 4", the terminating resistor should be placed within 1" of the PIIX4E.
- When using the ISA reset signal RSTDRV from the PIIX4E, it should be routed through a Schmitt trigger for RESET# signals.
- Ground pins 19, 2, 22, 24, 26, 30, 40 of both ATA connectors
- Pins 20 and 34 of both ATA connectors should be left unconnected.
- According to ATA-4 specification, a 10 KΩ pull-down resistor is required on DD7 to allow a host to recognize the absence of a device at power-up.
- Exceptions: When the PIIX4E's IDE interface is configured as Primary 0/Primary 1, and two IDE devices are connected, it should appear to the devices as if they are on the same cable. See *Intel® 82371AB PCI-to-ISA/IDE Xcelerator (PIIX4)* datasheet (order number 290562).
  - — Both IDE devices should connect to IRQ14.
  - — CSEL connected (pin28) together between the two ATA connectors and be pulled down with a 470 Ω resistor to meet PC97 requirement.
  - — DIAG (pin 34) connected together between the two ATA connectors.

Table 38. IDE Interface Signal Resistor Values

Name	Termination Resistor (Ω)	Pull-up (pull-down) Resistor (Ω)
PDDREQ	33 (82 for Ultra DMA)	5.6 K (pull-down)
SDDREQ	33 (82 for Ultra DMA)	5.6 K (pull-down)
PIORDY	82 (Ultra DMA only)	1 K Pull-up
SIORDY	82 (Ultra DMA only)	1 K Pull-up
CSEL (Pin 28)	None	470 (pull-down)
All signals to the two IDE connectors	33	None
DD7	33	10 K (pull-down)

6.3.9 BIOS to Flash Memory Interface

Two Mbits of flash is usually all that is required to support the 82443BX in all configurations. These are the recommendations for an Intel 28F200BV flash part.

- Use 0.01 µF - 0.1 µF capacitors for power supply (V_{CC} and V_{PP}) decoupling.
- Connect BYTE# to GND when a x16 flash device is used to configure it for x8.
- Use GPO*x* to control the WP# signal.
- Connect V_{PP} to 5 V.
- Use GPO*x* to control the RP# signal.

6.3.10 ITP/JTAG Interface

When implementing an ITP debug port, terminate RESET and PRDY# signals properly at the debug port. Terminations should include a 240 Ω series resistor. The module provides the pull-ups internally, except for TDO, which needs a 150 Ω pull-up to V_CPUPU.

Table 39. ITP/JTAG Interface

Signal Name	Termination Resistor	Pull-up (Pull-down) Resistor
RESET	240 Ω	None required, provided on module
PRDY#	240 Ω	None required, provided on module
TCK	47 Ω	None required, provided on module
TMS	47 Ω	None required, provided on module
TDI	None	None required, provided on module
TDO	None	150 Ω pull up to V_CPUPU
TRST#	None	None required, (pull-down) provided on module
PREQ#	None	None required, provided on module

7.0 Power Sequencing

This section provides a summary of the power sequencing requirements and options of the 440BX AGPset. It provides a detailed description of the PIIX4E Suspend/Resume sequence, signaling protocols, and timings. The recommended usage model for power plane control in a 440BX platform using PIIX4E power management signals is described.

This section does not represent the only way to design a system, but it does provide recommendations for using the 440BX AGPset.

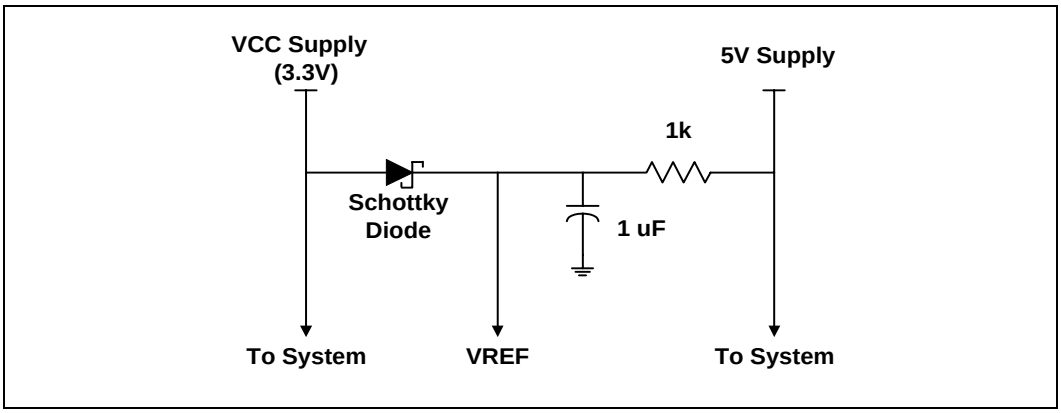
7.1 PIIX4E Power Sequencing

7.1.1 Power Sequencing Requirements

In systems requiring 5-V tolerance, the VREF signal must be tied to 5 V. This signal must power up before or simultaneous to V_{CC}. It must power down after or simultaneous to V_{CC}. In a non-5-V tolerant system (3.3 V only), this signal can be tied directly to V_{CC}. There are then no sequencing requirements. Refer to Figure 28 for an example circuit schematic, which may be used to ensure the proper VREF sequencing.

The PIIX4E V_{CC} and V_{CC}(USB) supplies are separated internally in order to reduce noise on USB signals. They should not be powered up or down independently of one another. They should be connected to the same power plane on the motherboard. There are no other power sequencing requirements for the various V_{CC} power supplies to the PIIX4E.

Figure 28. VREF Supply Schematic



7.1.2 Suspend/Resume and Power Plane Control

The PIIX4E supports three different Suspend modes. The common system usage model for these modes is described here and includes Power On Suspend (POS), Suspend to RAM (STR), and Suspend to Disk (STD). This mode definition allows for other system usage models that use the PIIX4E suspend/resume control signals in other ways. The common system mode names are used throughout this document.

The PIIX4E power management architecture is designed to allow systems to support multiple suspend modes, and to switch between those modes as required. A suspended system can be resumed by a number of different events. The system returns to full operation, and can then continue processing or be placed into another suspend mode. The new mode can be at a lower power mode than the mode from which it resumed.

7.1.2.1 Power On Suspend (POS) System Model

All devices are powered up except for the clock synthesizer. The Host and PCI clocks are inactive, and the PIIX4E provides control signals and the 32 KHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer. The only power consumed in the system while it is in POS mode is due to DRAM refresh and leakage current of the powered devices.

When the system resumes from POS mode, the PIIX4E can resume without resetting the system, can reset the processor only, or can reset the entire system. When no reset is performed, the PIIX4E only needs to wait for the clock synthesizer and processor PLLs to lock before the system is resumed. This takes typically 20 ms.

7.1.2.2 Suspend to RAM (STR)

Power is removed from most of the system components during STR, except the DRAM. Power is supplied to the host bridge (for DRAM Suspend Refresh) and the PIIX4E's RTC and Suspend Well logic. The PIIX4E provides control signals and a 32 KHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer and other power planes.

The PIIX4E resets the system on resume from STR.

7.1.2.3 Suspend to Disk (STD) and Soft Off (SOff)

Power is removed from most of the system components during STD. Power is maintained to the RTC and Suspend Well logic in the PIIX4E.

The PIIX4E resets the system on resume from STD.

The STD state is also called the Soft Off (SOff) state. The difference depends on whether the system state is restored by software to a pre-suspend condition or the system is rebooted.

7.1.2.4 Mechanical Off (MOff)

This is not a suspend state. This is a condition where all power except the RTC battery has been removed from the system. It is typically controlled by a mechanical switch that turns off AC power to a power supply. It could be used as a condition in which an embedded system's main battery has been removed.

The PIIX4E controls the system entering the various suspend states through the suspend control signals listed in Table 40. Upon initiation of suspend, the PIIX4E asserts the SUS_STAT[1-2]#, SUSA#, SUSB#, and SUSC# signals in a well defined sequence to switch the system into the desired power state. The SUSA#, SUSB#, and SUSC# signals can be used to control various power planes in the system. The SUS_STAT1# signal is a status signal that indicates to the host bridge when to enter or exit a suspend state, or when to enter or exit a stop clock state (when the system is still running). This is typically used to place the DRAM controller into a Suspend Refresh mode of operation. The SUS_STAT2# signal is a status signal that can be used to indicate to other system devices when to enter or exit a suspend state (like the graphics and Cardbus controllers). See "System Suspend and Resume Control Signaling" on page 55 for sequencing details. Note that these signals are associated with a particular type of suspend mode and power plane for descriptive purposes here. The system designer is free to use these signals to control any type of function desired.

The system is placed into a suspend mode by programming the Power Management Control register. The Suspend Type is first programmed and then the Suspend Enable bit is set. This causes the PIIX4E to automatically sequence into the programmed suspend mode.

Table 40. Power State Decode

Power State	RSMRST#	SUS_STAT1#	SUS_STAT2#	SUSA#	SUSB#	SUSC#
On	1	x†	1	1	1	1
POS	1	0	0	0	1	1
STR	1	0	0	0	0	1
STD/SOFF	1	0	0	0	0	0
Mechanical Off	0	0	0	0	0	0

† SUS_STAT1# is also used when the system is running. It indicates to the Host-to-PCI bridge when to switch between the normal and suspend refresh mode for DRAM Stop Clock support. In the Stop Clock condition, HCLK is stopped and the Host-to-PCI bridge must run DRAM refresh from the internal oscillator.

7.1.3 System Resume

The PIIX4E can be resumed from either a Suspend or Soft Off state. Depending on the suspend state that the system is in, different features can be enabled to resume the system. There are two classes of resume events, those whose logic resides in the PIIX4E main power well and those whose logic resides in the PIIX4E suspend well. Those in the suspend well can resume the system from any Suspend or Soft Off state. Those in the main power well can only resume the system from a Power On Suspend state. Table 41 lists the suspend states for which a particular resume event can be enabled.

Upon detection of an enabled resume event, the PIIX4E sets appropriate status signals and automatically transitions its suspend control signals to bring the system into a “full on” condition. The sequencing is shown in “System Suspend and Resume Control Signaling” on page 55.

Table 41. Resume Events Supported In Different Power States

Resume Event	Suspend States			
	POS	STR	STD/SOff	MOff
RTC Alarm (IRQ8) †	x	x	x	
SMBus Resume Event (Slave Port Match)	x	x	x	
Serial A Ring (RI)	x	x	x	
Power Button (PWRBTN#)	x	x	x	
EXTSMI (EXTSMI#)	x	x	x	
LID (LID)	x	x	x	
GPI 1	x	x	x	
GSTBY Timer Expiration	x	x	x	
Interrupt (IRQ 1,3-15)	x			
USB	x			

† RTC Alarm only supports internal RTC. For external RTC implementations, the IRQ8 must be tied to one of the other resume input signals (GPI[1], LID, EXTSMI#,RI#) for the resume functionality.

7.1.3.1 System Resume Events

Table 42 indicates the various resume events and their corresponding programming models.

Table 42. Resume Event Programming Model

System Resume Event	Programming Model
PWRBTN# Asserted	[PWRBTN_EN]
LID Asserted - Polarity Select	[LID_EN] [LID_POL]
GPI[1] Asserted	[GPI_EN]
EXTSMI# Asserted	[EXTSMI_EN]

† RTC Alarm only supports internal RTC. For external RTC implementations, the IRQ8 must be tied to one of the other resume input signals (GPI[1], LID, EXTSMI#,RI#) for the resume functionality.

Table 42. Resume Event Programming Model

System Resume Event	Programming Model
SMBus Events:	[ALERT_EN] [SLV_EN] [SHDW1_EN] [SHDW2_EN]
Global Standby Timer Expiration:	[GSTBY_EN]
Ring Indicate Assertion (RI#)	[RI_EN]
RTC Alarm (IRQ8)†	[RTC_EN]
USB Resume Signaling: (POS Only)	[USB_EN]
IRQ[1,3-7,9-15]: (POS Only)	[IRQ_RSM_EN]

† RTC Alarm only supports internal RTC. For external RTC implementations, the IRQ8 must be tied to one of the other resume input signals (GPI[1], LID, EXTSMI#,RI#) for the resume functionality.

7.1.3.2 Global Standby Timer Resume

The Global Standby Timer is used to monitor system activity during normal operation and can be reloaded by system activity events. Upon expiration, it generates an SMI#. When the system is placed in a Suspend Mode, the Global Standby Timer can be used to generate a resume event. The Global Standby Timer can enable two different timer resolutions for wake-up times from approximately 30 seconds to 8.5 hours. This can allow the system to transition into a lower power suspend state.

See the System Management Section of the *82371AB PCI-to-ISA/IDE Xcelerator (PIIX4)* datasheet for additional information about the Global Standby Timer.

7.1.4 System Suspend and Resume Control Signaling

The PIIX4E automatically controls the signals required to transition the system between the various power states. It provides control for Host and PCI clocks, main memory and video memory refresh, system power plane control, and system reset. Table 43 and Table 44 indicate the common usage model for power plane control using the SUS[C:A]# signals. The PIIX4E Resume well should always be powered by a trickle supply (main battery or backup battery in an embedded system).

Table 43. Power Plane Control

SUSA# (POS)	SUSB# (STR)	SUSC# (STD)
Clock synthesizer Video display[1]	Processor (Low Power GTL+ supplies) PIIX4E Core Other system devices[2]	82443BX Host Bridge/Controller DRAM Graphics Controller

NOTES:
1. The video display (flat panel or CRT) may optionally be powered off in POS. This could be accomplished by using the PIIX4E's SUSA# or SUS_STAT2# signals to assert the video controller's STANDBY signal.
2. Devices may include mass storage, audio, or other devices that will not generate system resume events.

Table 44. Power Plane Control Using SUS[C:A]# Signals

Power Plane	Suspend Mode (Suspend Mode Signals Asserted by the PIIX4E)			
	Full On (None)	POS (SUSA#, SUS_STAT[2:1]#)	STR (SUS[B:A]# SUS_STAT[2:1]#)	STD (SUS[C:A]# SUS_STAT[2:1]#)
Clock Synthesizer	On	Off	Off	Off
Video Display	On	On/Off[1]	Off	Off
CPU	On	On	Off	Off
PIIX4E Core	On	On	Off	Off
Other Devices[2]	On	On	Off	Off
82443BX	On	On	On	Off
DRAM	On	On	On	Off
Graphics Controller	On	On	On	Off
PIIX4E Resume	On	On	On	On
PIIX4E RTC	On	On	On	On

NOTES:
1. The video display (flat panel or CRT) may optionally be powered off in POS. This could be accomplished by using the PIIX4E's SUSA# or SUS_STAT2# signals to assert the video controller's STANDBY signal.
2. Devices may include mass storage, audio, or other devices that will not generate system resume events.

7.1.4.1 Power Well and Reset Signal Timings

Figure 29 shows the system timings for changing the power states of a system using the POS/STR/ STD models.

7.1.4.2 PIIX4E Power Well Timings

Figure 29 describes the relative transitions for PIIX4E power supplies. Table 45 indicates the PIIX4E power well timing tolerances.

Figure 29. PIIX4E Power Well Timings

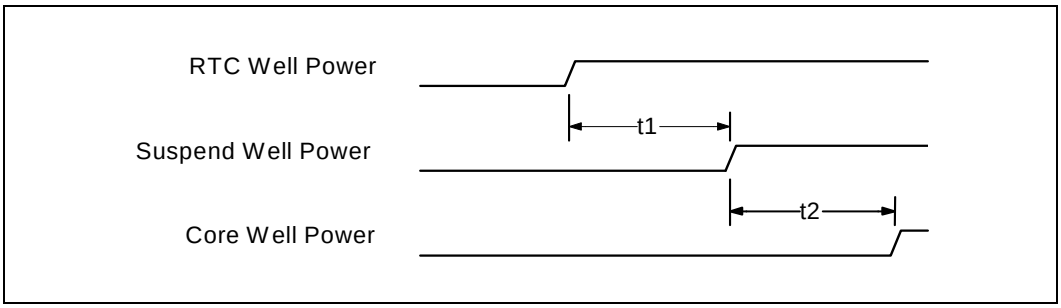


Table 45. PIIX4E Power Well Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t1	RTC Well Power to Suspend Well Power	0		ns	
t2	Suspend Well Power to Core Well Power	0		ns	

7.1.4.3 RSMRST# and PWROK Timing

Figure 30 describes the required timings for PIIX4E power level active status signals. Table 46 indicates the RSMRST# and PWROK timing tolerances.

Figure 30. RSMRST# and PWROK Timings

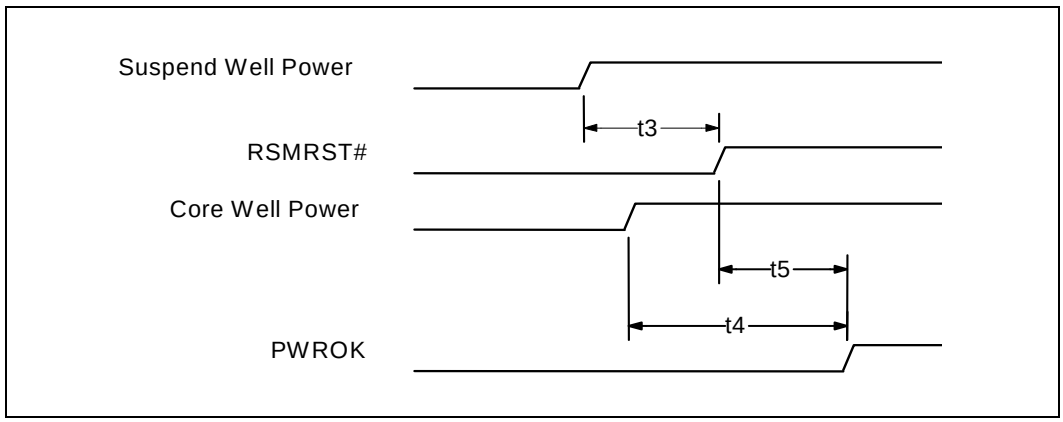


Table 46. RSMRST# and PWROK Timing Tolerance

Sym	Parameter	Min	Max	Unit	Notes
t3	Suspend Well Power to RSMRST# Inactive	1		ms	
t4	Core Well Power to PWROK Active	1		ms	
t5	RSMRST# Inactive to PWROK Active	0		ns	

7.1.4.4 Suspend Well Power and RSMRST# Activated Signals

Figure 31 shows the timing relationships for the PIIX4E power management signals that are powered from the Suspend Well Power signal. These timings hold independent of the condition of Core Well Power or the PWROK signal. Table 47 indicates the Suspend Well Power and RSMRST# timing tolerances.

Figure 31. Suspend Well Power and RSMRST# Activated Signals

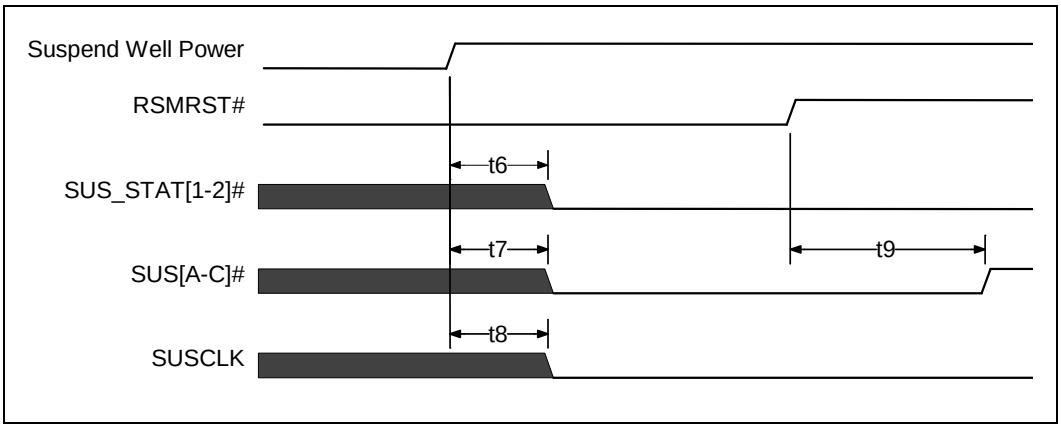


Table 47. Suspend Well Power and RSMRST# Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t6	Resume Well Power and RSMRST# Active to SUS_STAT[1:2]# Active		1	RTC	1
t7	Resume Well Power and RSMRST# Active to SUS [A:C]# Active		1	RTC	1
t8	Resume Well Power and RSMRST# Active to SUSCLK Low		1	RTC	1
t9	RSMRST# Inactive to SUS[A:C]# Inactive	1	2	RTC	1

NOTE:
1. These signals are controlled off an internal RTC clock. One RTC unit is approximately 32 µs.

7.1.4.5 PCI Clock Control Timings

This section describes the timing requirements for the control of the system PCICLK. The system PCICLK timing shown in Figure 32 must be followed exactly for proper operation of the PC/PCI DMA or Serial IRQ logic. When the PC/PCI DMA and Serial IRQs are not used in the system, the system PCICLK stop timings must meet the system developer's requirements.

Figure 32. PCI Clock Stop Timing

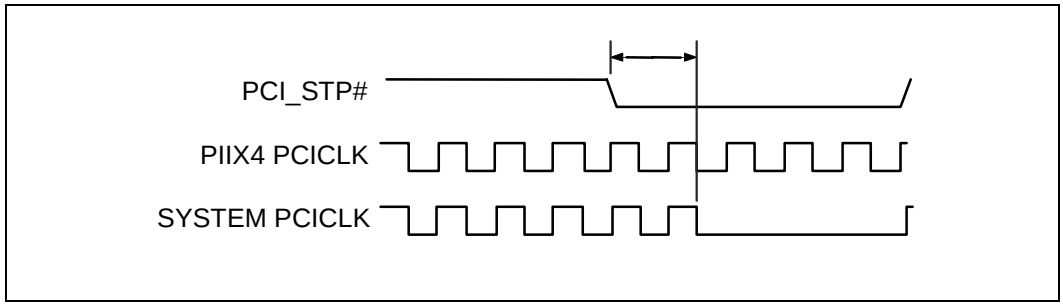
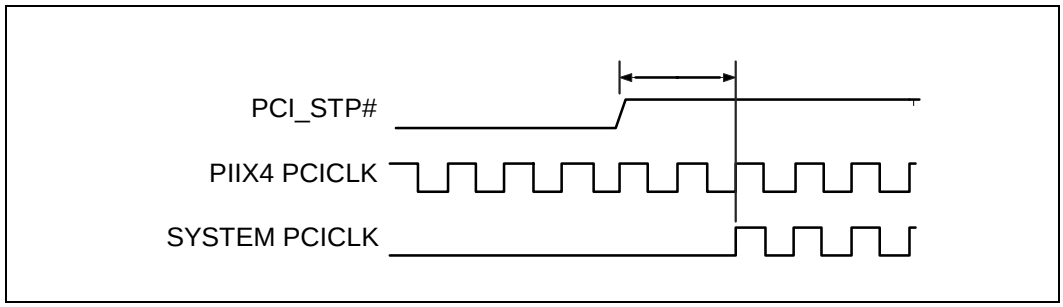


Figure 33 describes the timing requirements for the control of the system PCICLK. The system PCICLK timings shown in Figure 33 must be followed exactly for proper operation of PC/PCI DMA or Serial IRQ logic. When PC/PCI DMA and Serial IRQs are not used in the system, the system PCICLK stop timings must meet the system developer's requirements.

Figure 33. PCI Clock Start Timing



7.1.4.6 Core Well Power and PWROK Activated Signals (RSMRST# Inactive Before Core Well Power Applied)

Figure 34 shows the timing relations for Power Management signals powered from the PIIX4E Main Core well. The Suspend Well Power active status signals (RSMRST#) transitions before the application of core well power to the PIIX4E. This figure corresponds to the usage model for PIIX4E power management. Table 48 indicates the Core Well Power and PWROK timing tolerances.

Figure 34. Core Well Power and PWROK Activated Signals (RSMRST# Inactive before Core Well Power Applied)

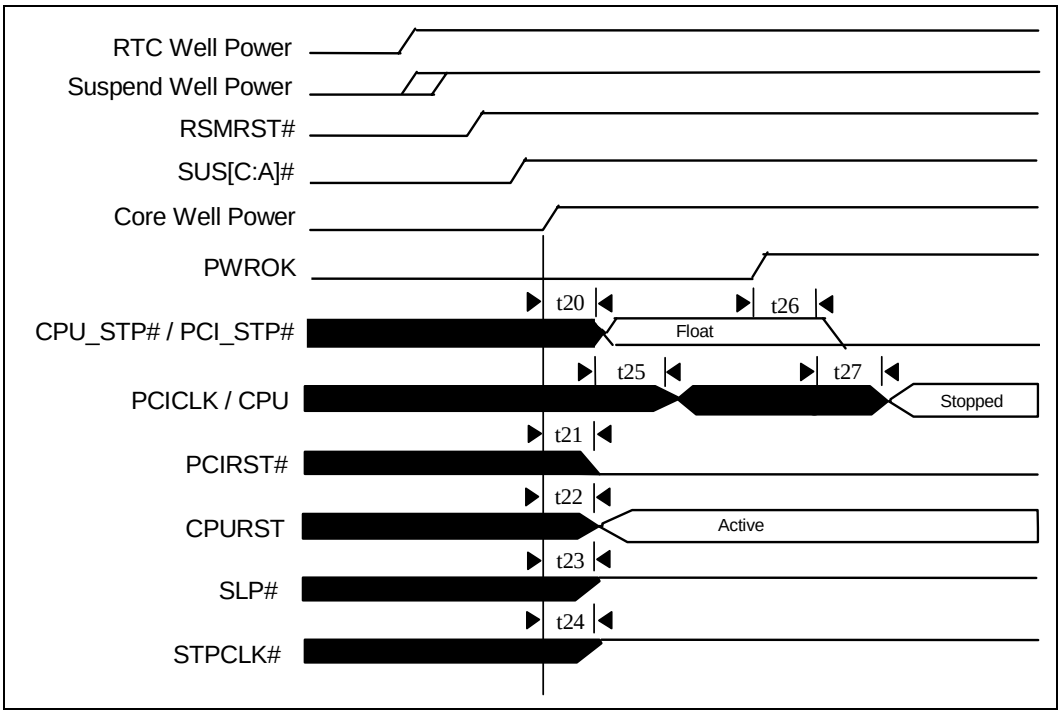


Table 48. Core Well Power and PWROK Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t20	Core Well Power and PWROK Inactive to CPU_STP# and PCI_STP# Float		1	RTC	1
t21	Core Well Power and PWROK Inactive to PCIRST# Active		1	RTC	1
t22	Core Well Power and PWROK Inactive to CPURST Active		1	RTC	1
t23	Core Well Power and PWROK Inactive to SLP# Active		1	RTC	1
t24	Core Well Power and PWROK Inactive to STPCLK# Active		1	RTC	1
t25	CPU_STP# and PCI_STP# Float to Clocks Running				2
t26	PWROK Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t27	CPU_STP# and PCI_STP# Active to Clocks Stopped				2

NOTES:
1. These signals are controlled off an internal RTC clock. One RTC unit is approximately 32 µs.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks on power up meet any other system specifications. As a minimum, the clocks must be available and stable after time t29 shown in Figure 36.

7.1.4.7 Core Well Power and PWROK Activated Signals (Core Well Power Applied Before RSMRST# Inactive)

Figure 35 shows the timing relations for Power Management signals powered from the PIIX4E Core well. Here the power active status signals (RSMRST# and PWROK) transition after the application of all power to the PIIX4E. This is an example of an implementation in which the Core Well power plane is not controlled by the SUSB# signal. It can be applied to situations where two or more of the PIIX4E power planes are connected together. It also shows timings when RSMRST# and PWROK are connected together.

Figure 35. Core Well Power and PWROK Activated Signals (Core Well Power Applied before RSMRST# Inactive)

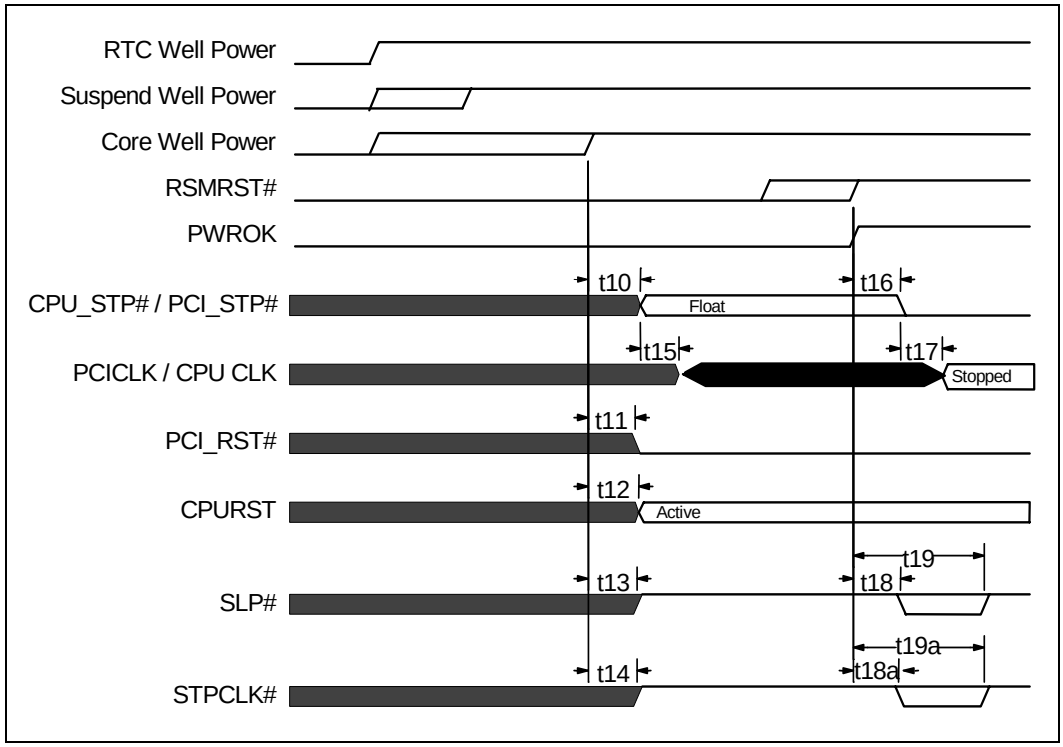


Table 49. Core Well Power and PWROK Timing

Sym	Parameter	Min	Max	Unit	Notes
t10	Core Well Power and PWROK Inactive to CPU_STP# and PCI_STP# Float		1	RTC	1
t11	Core Well Power and PWROK Inactive to PCIRST# Active		1	RTC	1
t12	Core Well Power and PWROK Inactive to CPURST Active		1	RTC	1
t13	Core Well Power and PWROK Inactive to SLP# Inactive		1	RTC	1
t14	Core Well Power and PWROK Inactive to STPCLK# Inactive		1	RTC	1
t15	CPU_STP# and PCI_STP# Float to Clocks Running				2
t16	PWROK Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t17	CPU_STP# and PCI_STP# Active to Clocks Stopped				2
t18	PWROK Active to SLP# Active	0		ns	3
t18a	PWROK Active to STPCLK# Active	0		ns	3
t19	PWROK Active to SLP# Inactive	1	2	RTC	1, 3
t19a	PWROK Active to STPCLK# Inactive	1	2	RTC	1, 3

NOTES:
1. These signals are controlled off an internal RTC clock. One RTC unit is approximately 32 µs.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks on power up meet any other system specifications. As a minimum, the clocks must be available and stable after time t29 shown in Figure 36.
3. These timings depend on the relative timings between RSMRST# and PWROK. If RSMRST# goes inactive two RTC periods before PWROK active, then SLP# and STPCLK# will remain inactive. If RSMRST# goes inactive less than two RTC periods before PWROK active, then an active pulse will be seen on SLP# and STPCLK#.

7.1.5 Power Management State Transition Timings

7.1.5.1 Mechanical Off to On

Figure 36 shows the transition from a Mechanical Off condition to the On condition. Table 50 describes the mechanical Off to On timing tolerances.

Figure 36. Mechanical Off to On

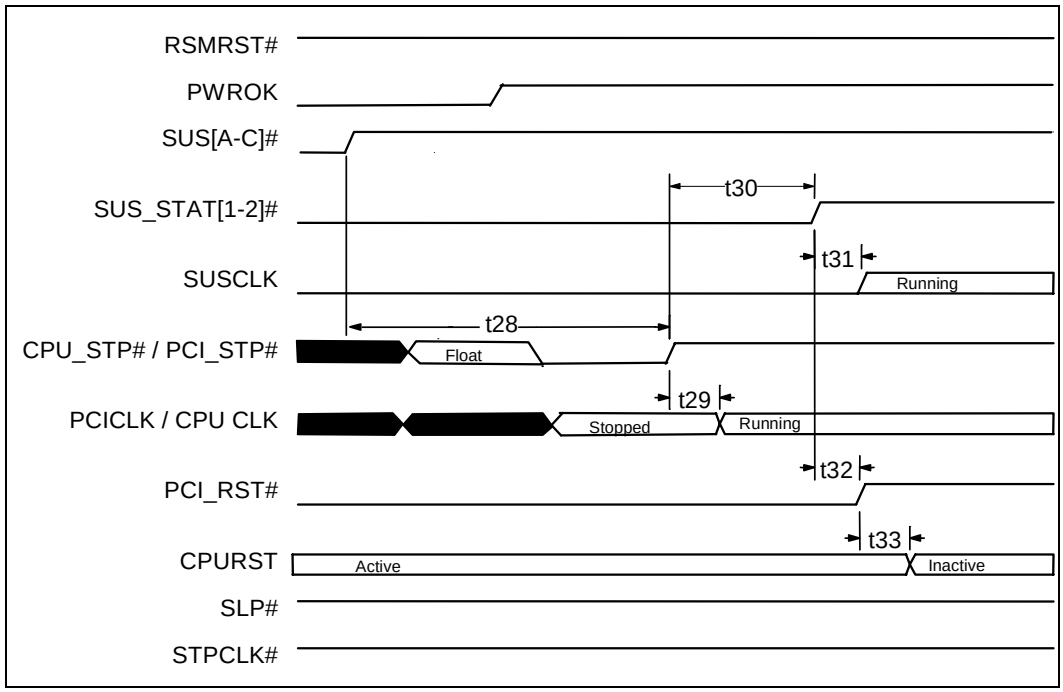


Table 50. Mechanical Off to On Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t28	SUS[A:C]# Inactive to CPU_STP# and PCI_STP# Inactive	16		ms	1
t29	CPU_STP# and PCI_STP# Inactive to Clocks Running		2	PCICLK	2
t30	CPU_STP# and PCI_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t31	SUS_STAT[1:2]# Inactive to SUSCLK Running		1	RTC	3
t32	SUS_STAT[1:2]# Inactive to PCI_RST# Inactive		1	RTC	3
t33	PCI_RST# Inactive to CPURST Inactive		1	RTC	3

NOTES:
1. This transition requires a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. If PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition occurs a minimum of one RTC period from PWROK active.
2. See Table 32 and Table 33 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.
3. These signals are controlled from an internal RTC clock. One RTC unit is approximately 32 µs.

7.1.5.2 On to POS

Figure 37 describes the signal transitions from the On state to the Power On Suspend state. Table 51 indicates the On to POS timing tolerances.

Figure 37. On to POS

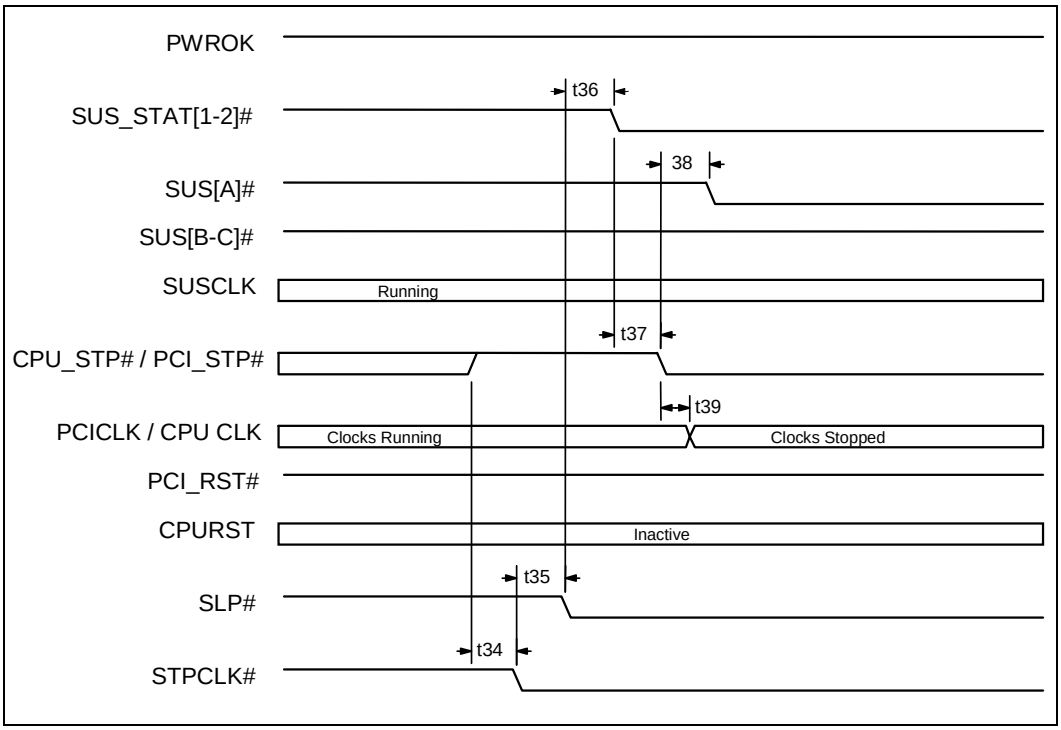


Table 51. On to POS Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t34	CPU_STP# and PCI_STP# Inactive to STPCLK# Active	1		RTC	1, 2
t35	STPCLK# Active to SLP# Active	1		RTC	1, 3
t36	SLP# Active to SUS_STAT[1:2]# Active		1	RTC	1
t37	SUS_STAT[1:2]# Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t38	CPU_STP# and PCI_STP# Active to SUS[A]# Active		1	RTC	1
t39	CPU_STP# and PCI_STP# Active to Clocks Stopped (if applicable)		2	PCICLK	4, 5

NOTES:
1. These signals are controlled from an internal RTC clock. One RTC unit is approximately 32 µs.
2. CPU_STP# and PCI_STP# will only be active when the system is under clock control.
3. This transition waits for the Stop Grant cycle to execute.
4. It is up to the system vendor to determine whether CPU_STP# and PCI_STP# signals are used to control system clocks.
5. See Table 32 and Table 33 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.

7.1.5.3 POS to On (with Processor and PCI Reset)

Figure 38 describes the system transition from Power On Suspend to On with a full system reset. Table 52 indicates the POS to On timing tolerances.

Figure 38. POS to On (with Processor and PCI Reset)

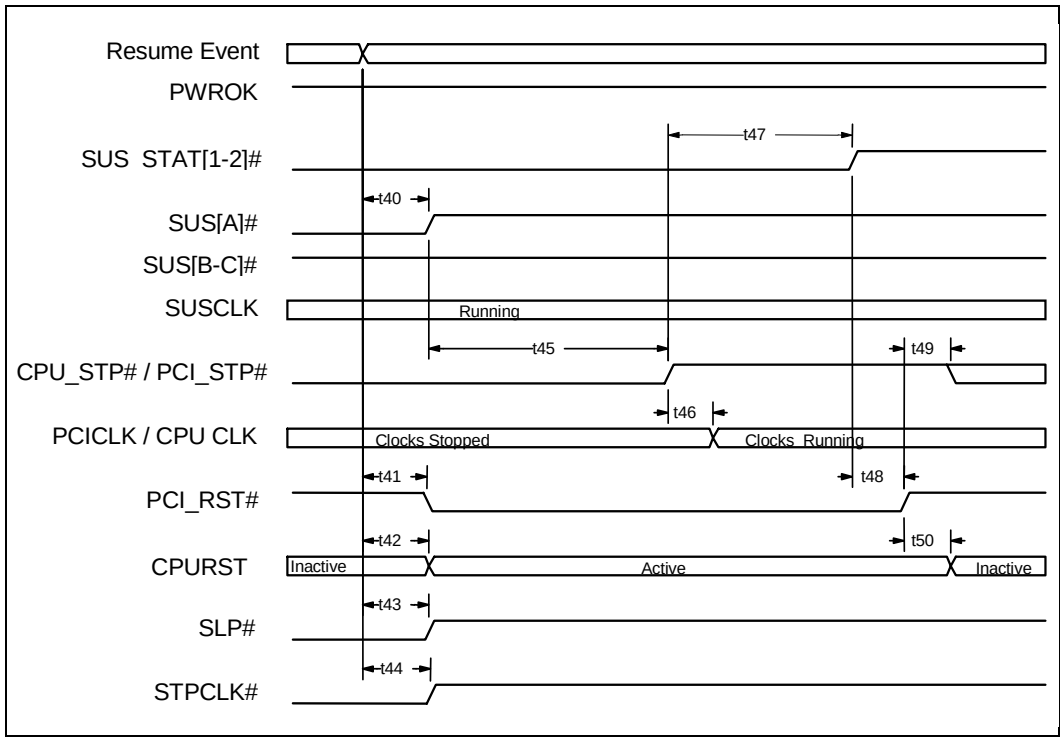


Table 52. POS to On Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t40	Resume Event to SUS[A]# Inactive	1		RTC	1
t41	Resume Event to PCI_RST# Active	1		RTC	1
t42	Resume Event to CPURST Active	1		RTC	1
t43	Resume Event to SLP# Inactive	1		RTC	1
t44	Resume Event to STPCLK# Inactive	1		RTC	1
t45	SUS[A]# Inactive to PCI_STP# and CPU_STP# Inactive	16		ms	2
t46	PCI_STP# and CPU_STP# Inactive to Clocks Running		2	PCICLK	3
t47	PCI_STP# and CPU_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t48	SUS_STAT[1:2]# Inactive to PCI_RST# Inactive		1	RTC	1
t49	PCI_RST# Inactive to PCI_STP# and CPU_STP# allowed to change		1	RTC	1
t50	PCI_RST# Inactive to CPURST Inactive		1	RTC	1

NOTES:
1. These signals are controlled from an internal RTC clock. One RTC unit is approximately 32 µs.
2. This transition requires a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. If PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition will occur a minimum of one RTC period from PWROK active. PWROK remains active throughout POS system usage.
3. See Table 32 and Table 33 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.

7.1.5.4 POS to On (with Processor Reset)

Figure 39 describes the system transition from Power On Suspend (POS) to On with only a processor reset. Table 53 indicates the POS to On (with processor reset) timing tolerances.

Figure 39. POS to On (with Processor Reset)

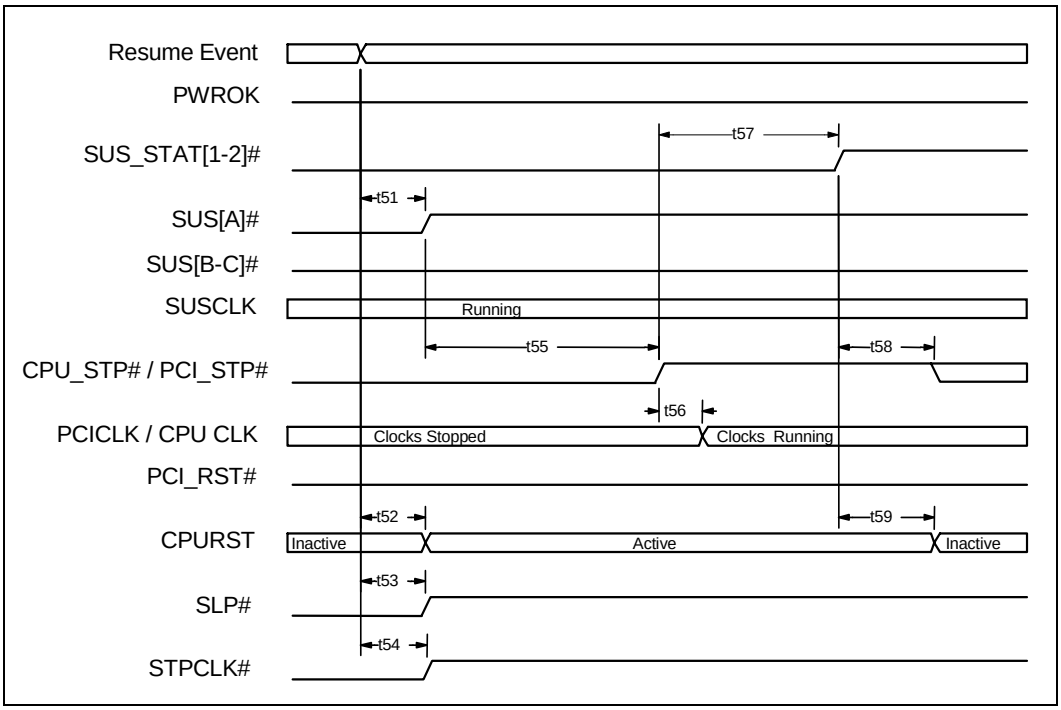


Table 53. POS to On (with Processor Reset) Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t51	Resume Event to SUSA# Inactive	1		RTC	1
t52	Resume Event to CPURST Active	1		RTC	1
t53	Resume Event to SLP# Inactive	1		RTC	1
t54	Resume Event to STPCLK# Inactive	1		RTC	1
t55	SUS[A]# Inactive to PCI_STP# and CPU_STP# Inactive	16		ms	2
t56	PCI_STP# and CPU_STP# Inactive to Clocks Running		2	PCICLK	3
t57	PCI_STP# and CPU_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t58	SUS_STAT[1:2]# Inactive to PCI_STP# and CPU_STP# allowed to change		2	RTC	1
t59	SUS_STAT[1:2]# Inactive to CPURST Inactive		2	RTC	1

NOTES:
1. These signals are controlled from an internal RTC clock. One RTC unit is approximately 32 µs.
2. This transition requires both a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. If PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition will occur a minimum of one RTC period from PWROK active. PWROK remains active throughout POS system usage.
3. See Table 32 and Table 33 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.

7.1.5.5 POS to On (No Reset)

Figure 40 describes the system transition from Power On Suspend to On with no resets performed. Table 54 indicates the POS to On (no reset) timing tolerances.

Figure 40. POS to On (No Reset)

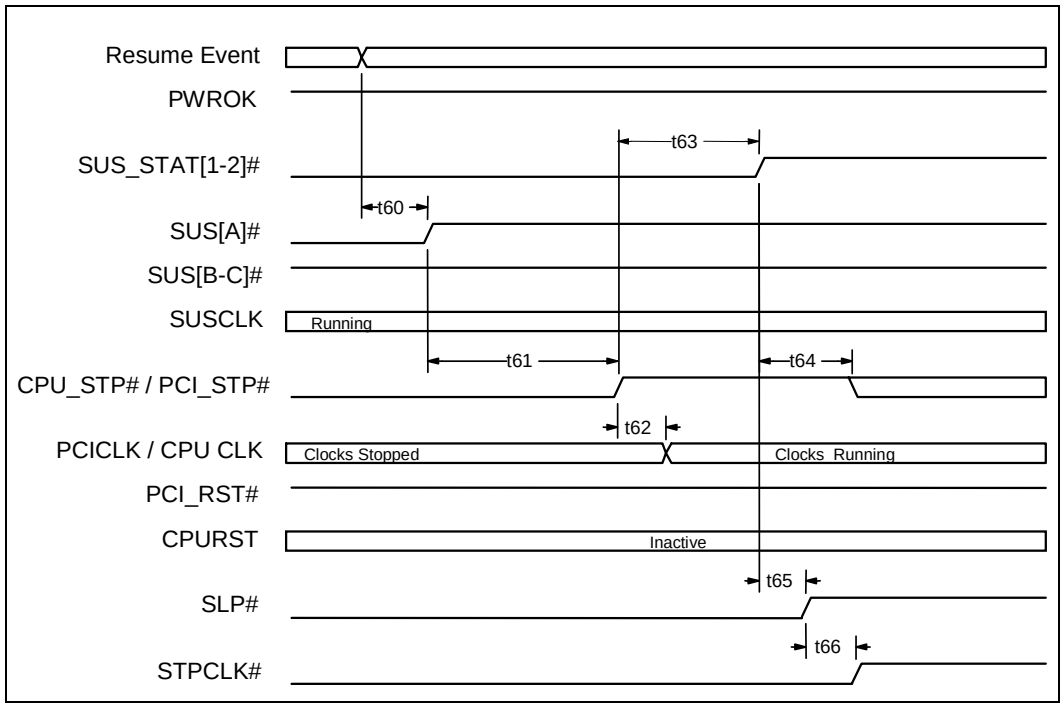


Table 54. POS to On (No Reset) Timing

Sym	Parameter	Min	Max	Unit	Notes
t60	Resume Event to SUS[A]# Inactive	1		RTC	1
t61	SUS[A]# Inactive to PCI_STP# and CPU_STP# Inactive	16		ms	2
t62	PCI_STP# and CPU_STP# Inactive to Clocks Running		2	PCICLK	3
t63	PCI_STP# and CPU_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t64	SUS_STAT[1:2]# Inactive to PCI_STP# and CPU_STP# allowed to change		2	RTC	1
t65	SUS_STAT[1:2]# Inactive to SLP# Inactive		1	RTC	1
t66	SLP# Inactive to STPCLK# Inactive		1	RTC	1

NOTES:
1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. This transition requires both a minimum of 16 ms wait for the clock synthesizer PLL to lock and PWROK to be active. If PWROK goes active after 16 ms from SUS[A:C]# inactive, the transition will occur a minimum of one RTC period from PWROK active. PWROK remains active throughout POS system usage.
3. See Figure 32 and Figure 33 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.

7.1.5.6 On to STR

Figure 41 describes the signal transitions from On state to Suspend to RAM state. Table 55 indicates the On to STR timing tolerances.

Figure 41. On to STR

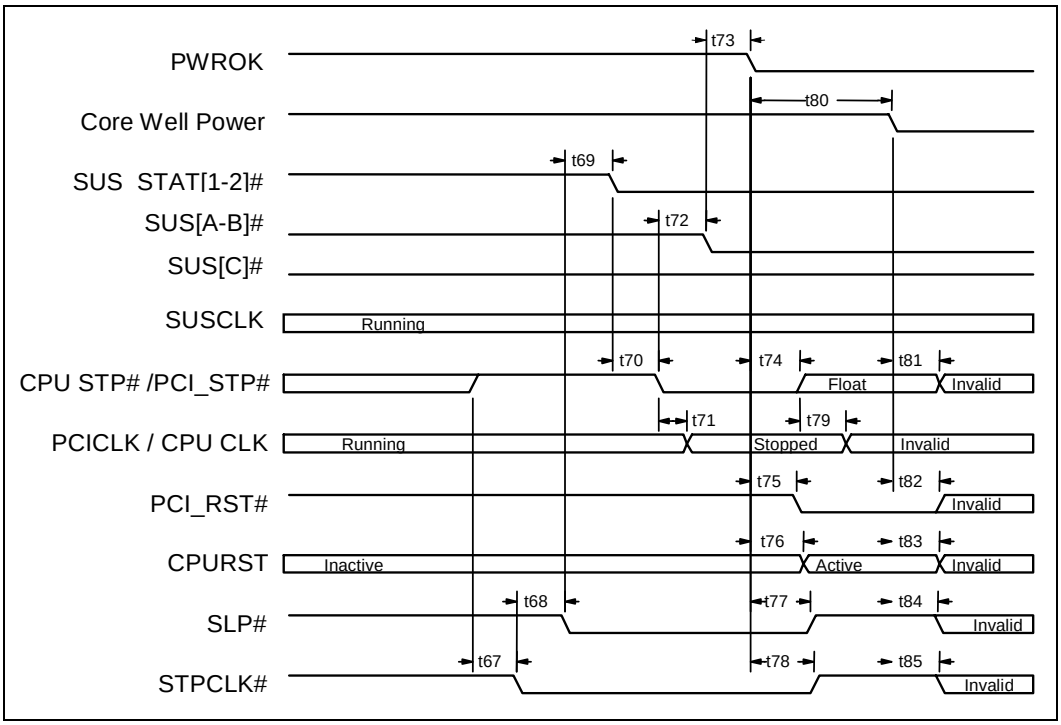


Table 55. On to STR Timing Tolerances

Sym	Parameter	Min	Max	Unit	Notes
t67	CPU_STP# and PCI_STP# Inactive to STPCLK# Active	1		RTC	1, 2
t68	STPCLK# Active to SLP# Active	1		RTC	1, 3
t69	SLP# Active to SUS_STAT[1:2]# Active		1	RTC	1
t70	SUS_STAT[1:2]# Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t71	CPU_STP# and PCI_STP# Active to CLOCKS Stopped		2	PCICLK	4, 5
t72	CPU_STP# and PCI_STP# Inactive to SUS[A:B]# Active		1	RTC	1
t73	SUS[A:B]# Active to PWROK Inactive	0		ns	6
t74	PWROK Inactive to CPU_STP# and PCI_STP# Float		1	RTC	1
t75	PWROK Inactive to PCI_RST# Active		1	RTC	1
t76	PWROK Inactive to CPURST Active		1	RTC	1
t77	PWROK Inactive to SLP# Inactive		1	RTC	1
t78	PWROK Inactive to STPCLK# Inactive		1	RTC	1
t79	CPU_STP# and PCI_STP# Float to Clocks Invalid	0		ns	7
t80	PWROK Inactive to Core Well Power Removed	0		ns	
t81	Core Well Power Removed to PCI_STP# and CPU_STP# Invalid	0		ns	
t82	Core Well Power Removed to PCIRST# Invalid	0		ns	
t83	Core Well Power Removed to CPURST Invalid	0		ns	
t84	Core Well Power Removed to SLP# Invalid	0		ns	
t85	Core Well Power Removed to STPCLK# Invalid	0		ns	

NOTES:
1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. CPU_STP# and PCI_STP# will only be active if the system is under clock control.
3. This transition will also wait for the Stop Grant cycle to execute.
4. It is up to the system vendor to determine if CPU_STP# and PCI_STP# signals are used to control system clocks.
5. See Figure 32 and Figure 33 for exact PCICLK requirements for use with PC/PCI DMA and Serial IRQs.
6. It is up to the system vendor to determine if SUS[A:B]# signals are used to control system power planes. If power remains applied to system board and PWROK stays active during STR, the PIIX4E signals will remain in the states shown after t73.
7. Clocks may or may not be running depending on the condition of the Power Supply voltages.

7.1.5.7 STR to On

Figure 42 describes the system transition from Suspend To RAM to On with a full system reset. Table 56 indicates the STR to On timing tolerances.

Figure 42. STR to On

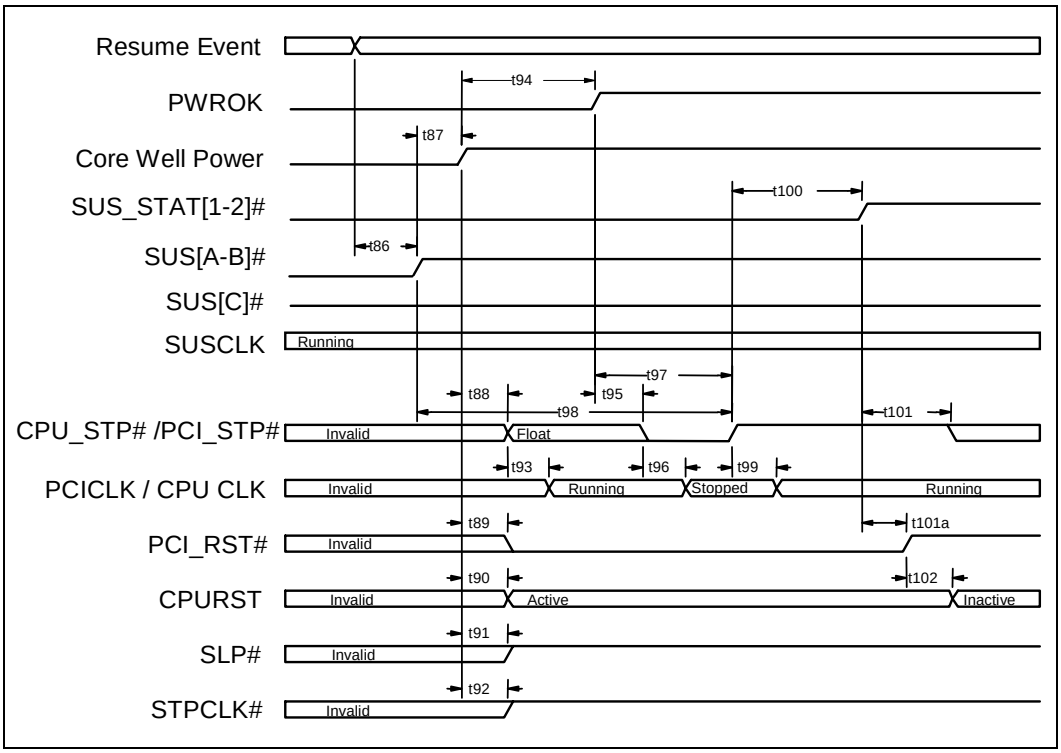


Table 56. STR to On Timing Tolerances (Sheet 1 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t86	Resume Event to SUS[A:B]# Inactive	1		RTC	1
t87	SUS[A:B]# Inactive to Core Well Power Applied	0		ns	
t88	Core Well Power Applied to PCI_STP# and CPU_STP# Float	0		ns	
t89	Core Well Power Applied to PCI_RST# Active	0		ns	
t90	Core Well Power Applied to CPURST Active	0		ns	
t91	Core Well Power Applied to SLP# Inactive	0		ns	
t92	Core Well Power Applied to STPCLK# Inactive	0		ns	
t93	PCI_STP# and CPU_STP# Float to Clocks Running				2

NOTES:
1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks meet any other system specifications upon power up. At a minimum, the clocks must be available and stable after time t99.
3. See Figure 32 and Figure 33 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.

Table 56. STR to On Timing Tolerances (Sheet 2 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t94	Core Well Power Applied to PWROK Active	1		ms	
t95	PWROK Active to CPU_STP# and PCI_STP# Active	0		ns	
t96	PCI_STP# and CPU_STP# Active to Clocks Stopped		2	PCICLK	3
t97	PWROK Active to CPU_STP# and PCI_STP# Inactive	1		RTC	1
t98	SUS[A-B]# Inactive to CPU_STP# and PCI_STP# Inactive	16		ms	
t99	CPU_STP# and PCI_STP# Inactive to Clocks Running		2	PCICLK	3
t100	CPU_STP# and PCI_STP# Inactive to SUS_STAT[1-2]# Inactive	1		ms	
t101	SUS_STAT[1-2]# Inactive to CPU_STP# and PCI_STP# allowed to change	2		RTC	1
t101a	SUS_STAT[1-2]# Inactive to PCI_RST# Inactive	1		RTC	1
t102	PCI_RST# Inactive to CPURST Inactive	1		RTC	1

NOTES:
1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks meet any other system specifications upon power up. At a minimum, the clocks must be available and stable after time t99.
3. See Figure 32 and Figure 33 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.

7.1.5.8 On to STD/SOff

Figure 43 describes the signal transitions from the On state to the Suspend to Disk/Soft Off state. Table 57 indicates the On to STD/SOff timing tolerances.

Figure 43. On to STD/SOff

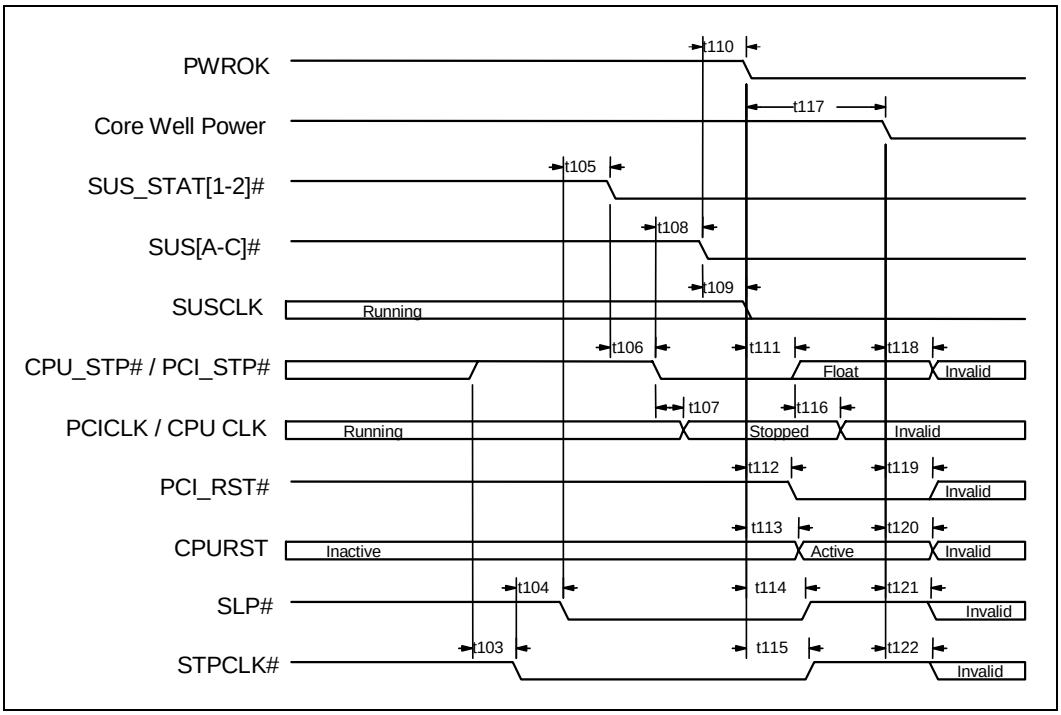


Table 57. On to STD/SOff Timing Tolerances (Sheet 1 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t103	CPU_STP# and PCI_STP# Inactive to STPCLK# Active	1		RTC	1, 2
t104	STPCLK# Active to SLP# Active	1		RTC	1, 3
t105	SLP# Active to SUS_STAT[1:2]# Active		1	RTC	1
t106	SUS_STAT[1:2]# Active to CPU_STP# and PCI_STP# Active		1	RTC	1
t107	CPU_STP# and PCI_STP# Inactive to CLOCKS Stopped		2	PCICLK	1, 4, 5

NOTES:
1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. CPU_STP# and PCI_STP# will only be active if the system is under clock control.
3. This transition will also wait for the Stop Grant cycle to execute.
4. It is up to the system vendor to determine if CPU_STP# and PCI_STP# signals are used to control system clocks.
5. See Figure 32 and Figure 33 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.
6. It is up to the system vendor to determine if SUS[A:C]# signals are used to control system power planes. If the power remains applied to the system board and the PWROK stays active during STD, the PIIX4E signals will remain in the states shown after t110.

Table 57. On to STD/SOff Timing Tolerances (Sheet 2 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t108	CPU_STP# and PCI_STP# Inactive to SUS[A:C]# Active		1	RTC	1
t109	SUS[A:C]# Active to SUSCLK Low		1	RTC	1
t110	SUS[A:C]# Active to PWROK Inactive	0		ns	6
t111	PWROK Inactive to CPU_STP# and PCI_STP# Float		1	RTC	1
t112	PWROK Inactive to PCI_RST# Active		1	RTC	1
t113	PWROK Inactive to CPURST Active		1	RTC	1
t114	PWROK Inactive to SLP# Inactive		1	RTC	1
t115	PWROK Inactive to STPCLK# Inactive		1	RTC	1
t116	CPU_STP# and PCI_STP# Float to Clocks Invalid	0		ns	1
t117	PWROK Inactive to Core Well Power Removed	0		ns	
t118	Core Well Power Removed to PCI_STP# and CPU_STP# Invalid	0		ns	
t119	Core Well Power Removed to PCIRST# Invalid	0		ns	
t120	Core Well Power Removed to CPURST Invalid	0		ns	
t121	Core Well Power Removed to SLP# Invalid	0		ns	
t122	Core Well Power Removed to STPCLK# Invalid	0		ns	

NOTES:
1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. CPU_STP# and PCI_STP# will only be active if the system is under clock control.
3. This transition will also wait for the Stop Grant cycle to execute.
4. It is up to the system vendor to determine if CPU_STP# and PCI_STP# signals are used to control system clocks.
5. See Figure 32 and Figure 33 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.
6. It is up to the system vendor to determine if SUS[A:C]# signals are used to control system power planes. If the power remains applied to the system board and the PWROK stays active during STD, the PIIX4E signals will remain in the states shown after t110.

7.1.5.9 STD/SOff to On

Figure 44 describes the system transition from Suspend To Disk to On with a full system reset. Table 58 indicates the STD/SOff to On timing tolerances.

Figure 44. STD/SOff to On

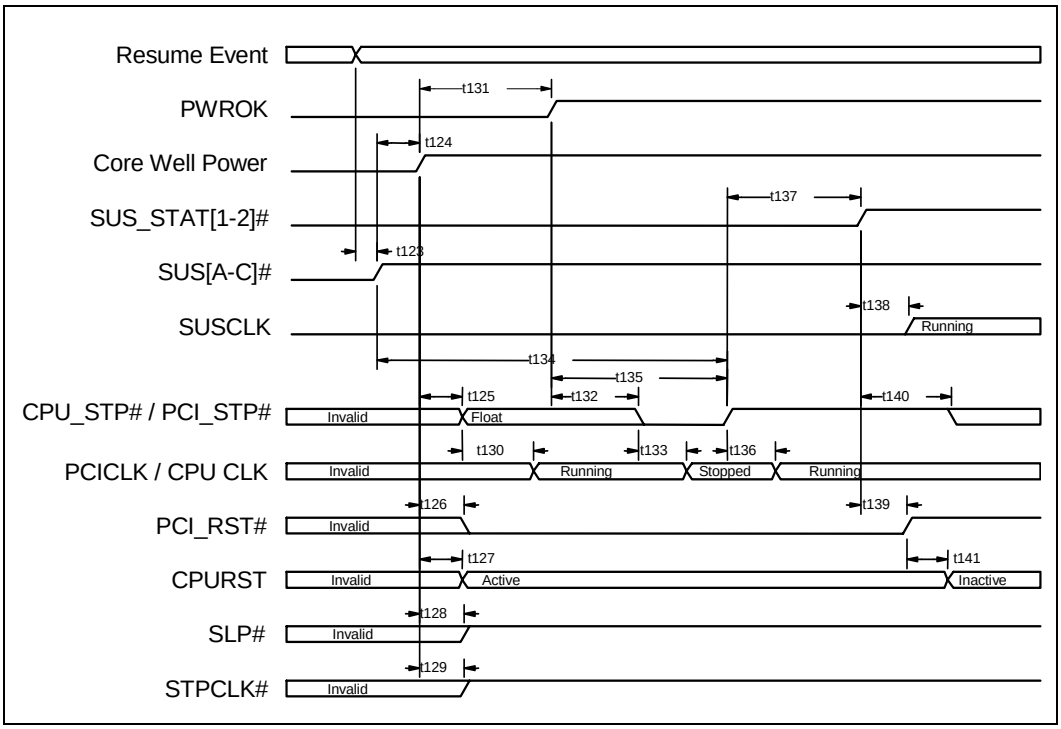


Table 58. STD/SOff to On Timing Tolerances (Sheet 1 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t123	Resume Event to SUS[A:C]# Inactive	1		RTC	1
t124	SUS[A-C]# Inactive to Core Well Power Applied	0		ns	
t125	Core Well Power Applied to PCI_STP# and CPU_STP# Float	0		ns	
t126	Core Well Power Applied to PCI_RST# Active	0		ns	
t127	Core Well Power Applied to CPURST Active	0		ns	
t128	Core Well Power Applied to SLP# Inactive	0		ns	
t129	Core Well Power Applied to STPCLK# Inactive	0		ns	
t130	PCI_STP# and CPU_STP# Float to Clocks Running				2
t131	Core Well Power Applied to PWROK Active	1		ms	

1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks on power up meet any other system specifications. At a minimum, the clocks must be available and stable after time t136.
3. See Figure 32 and Figure 33 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.

Table 58. STD/SOff to On Timing Tolerances (Sheet 2 of 2)

Sym	Parameter	Min	Max	Unit	Notes
t132	PWROK Active to CPU_STP# and PCI_STP# Active	0		ns	
t133	PCI_STP# and CPU_STP# Active to Clocks Stopped		2	PCICLK	3
t134	SUS[A-C]# Inactive to CPU_STP# and PCI_STP# Inactive	16		ms	
t135	PWROK Active to CPU_STP# and PCI_STP# Inactive	1		RTC	1
t136	PCI_STP# and CPU_STP# Active to Clocks Running	1	2	PCICLK	3
t137	CPU_STP# and PCI_STP# Inactive to SUS_STAT[1:2]# Inactive	1		ms	
t138	SUS_STAT[1:2]# Inactive to SUSCLK Running		1	RTC	1
t139	SUS_STAT[1:2]# Inactive to PCI_RST# Inactive	1		RTC	1
t140	SUS_STAT[1:2]# Inactive to CPU_STP# and PCI_STP# allowed to change	2		RTC	1
t141	PCI_RST# Inactive to CPURST Inactive	1		RTC	1

1. These signals are controlled from the internal RTC clock. One RTC is approximately 32 µs.
2. There are no specific requirements for these timings related to the PIIX4E. The system manufacturer should make sure that the clocks on power up meet any other system specifications. At a minimum, the clocks must be available and stable after time t136.
3. See Figure 32 and Figure 33 for exact PCICLK requirements for use with the PC/PCI DMA and Serial IRQs.

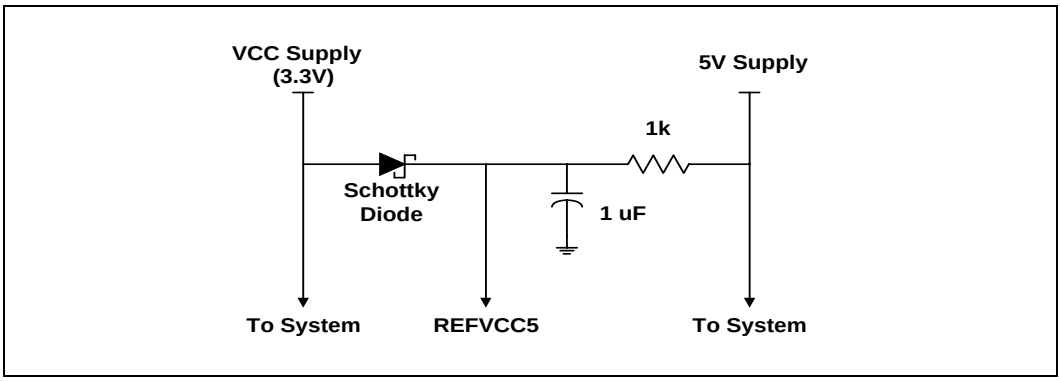
7.2 82443BX Host Bridge/Controller Power Sequencing

7.2.1 Power Sequencing Requirements

In systems requiring 5-V tolerance, the REFVCC5 signal must be tied to 5 V. This signal must power up before or simultaneous to V_{CC}. It must power down after or simultaneous to V_{CC}. In a non-5-V tolerant system (3.3 V only), this signal can be tied directly to V_{CC}. There are then no sequencing requirements. Refer to Figure 45 for an example circuit schematic that may be used to ensure the proper REFVCC5 sequencing. This is the same circuit that is recommended for the PIIX4E VREF supply. However, different power planes may supply the PIIX4E core and the 82443BX Host Bridge/Controller (the PIIX4E core may be powered down during STR). In this case a separate circuit must be used for each of the two devices.

V_{CC} must power up before or simultaneous to the AGP supplies (VCC_AGP and AGP_REF) and Low Power GTL+ supplies (VTT and GTL_REF). V_{CC} must power down after or simultaneous to the AGP and Low Power GTL+ supplies. The AGP and Low Power GTL+ supplies must not be powered up while V_{CC} is powered down. There are no other power sequencing requirements for the 82443BX Host Bridge/Controller.

Figure 45. REFVCC5 Supply Circuit Schematic



7.2.2 440BX AGPset Power Management

The 440BX AGPset supports a variety of system-wide low-power modes using the following functions:

- Hardware interface with the PIIX4E that is used to indicate:
  - — Suspend mode entry
  - — Resume from suspend
  - — Whether to automatically switch from suspend to normal refresh
- Automatic transition from normal to suspend refresh
- Optional automatic transition from suspend to normal refresh
- Optional CPU reset during resume from Power On Suspend (POS)
- Variety of Suspend refresh types:
  - — Self Refresh for SDRAMs
  - — Optional Self Refresh for EDO
  - — Optional CAS Before RAS (CBR) refresh for EDO. An Integrated Ring oscillator is used to provide the time base for the associated logic.
  - — Programmable slow refresh (relevant for CBR refresh only)
- Isolated I/O pins to significantly reduce power consumption while in POS and STR modes

Based on the above functions, the 440BX AGPset recognizes the following system-wide low power modes:

- STR and POS suspend entry and exit are generally handled in the same manner. The following exceptions are related to POS mode:
  - — The POS resume sequence may or may not include a processor reset. STR, with PCIRST# active always includes a processor reset.
  - — The POS resume sequence requires a hardware transition from suspend to a normal refresh. STR with PCIRST# active requires a software initiated transition.
- STD resume is handled in the same way as the power on sequence, including a complete reset of the 440BX AGPset state.

7.2.2.1 System Power Modes

Table 59 provides an overview of how the above features map into system-wide low power modes.

Table 59. System-wide Low-power Modes

System Suspend State	82443BX State	Description	POS Exit PCIRST	External Clk HCLK	External Clk PCLK
Power On	ON	82443BX is fully on and operating normally. Internal clock gating as well as PCI CLKRUN# may be enabled.	N/A	Active	Active
CPU STOP_GRANT or QUICK_START (C2)	ON	This is transparent to the 82443BX since the external HCLK and PCLK are unaffected. The Host Bus is Idle. Internal clock gating and PCI CLKRUN# may be enabled.	N/A	Active	Active
CPU STOP CLOCK (C3) (DEEP SLEEP)	POS	System PLLs remain powered, but are disabled. HCLK clock is kept low. The only guaranteed running clock is SUSCLK. The 82443BX maintains DRAM refresh using suspend refresh. The 82443BX's internal PLLs are disabled. The 82443BX PCI and AGP arbiters are disabled.	N	Low	Low or Active
Power On Suspend (POS)	POS	System PLLs are powered down. The only running clock is the RTC clock and SUSCLK. The 82443BX maintains DRAM refresh using suspend refresh. The 82443BX's PLLs are disabled. The 82443BX PCI and AGP arbiters are disabled. When resumed, the 82443BX may or may not generate a processor reset. All 82443BX logic, with the exception of resume and refresh, are inactive.	Y	Low	Low
Suspend to RAM (STR)	POS	The processor and other components (with the exception of the DRAM and PIIX4E resume logic) are assumed to be powered OFF. The 82443BX V_{CC} supply is on and all I/O buffers are isolated (with the exception of suspend and DRAM signals). The 82443BX Low Power GTL+ supplies should be powered down with the processor. The 82443BX maintains DRAM refresh using a suspend refresh. All 82443BX logic, with the exception of resume and refresh, are inactive.	Y	Low	Low
Suspend -to-Disk (STD) or Powered-Off	OFF	The entire system is powered OFF except for the PIIX4E resume and RTC wells. Upon resume, the 82443BX resets its entire state.	N/A	X	X

NOTE: The processor will generally be powered off during STR (the processor voltage regulator will be controlled by the PIIX4E's SUSB# signal). In this case, the 82443BX Low Power GTL+ supply (VTT and GTL_REF) should also be controlled by SUSB#, and hence be powered off during STR.

7.2.2.2 System Power-up Sequencing

The waveforms in Figure 46 show the powerup sequence and timing information for the 440BX AGPset. Table 60 indicates the system power-up sequencing tolerances.

Figure 46. System Power-up Sequencing

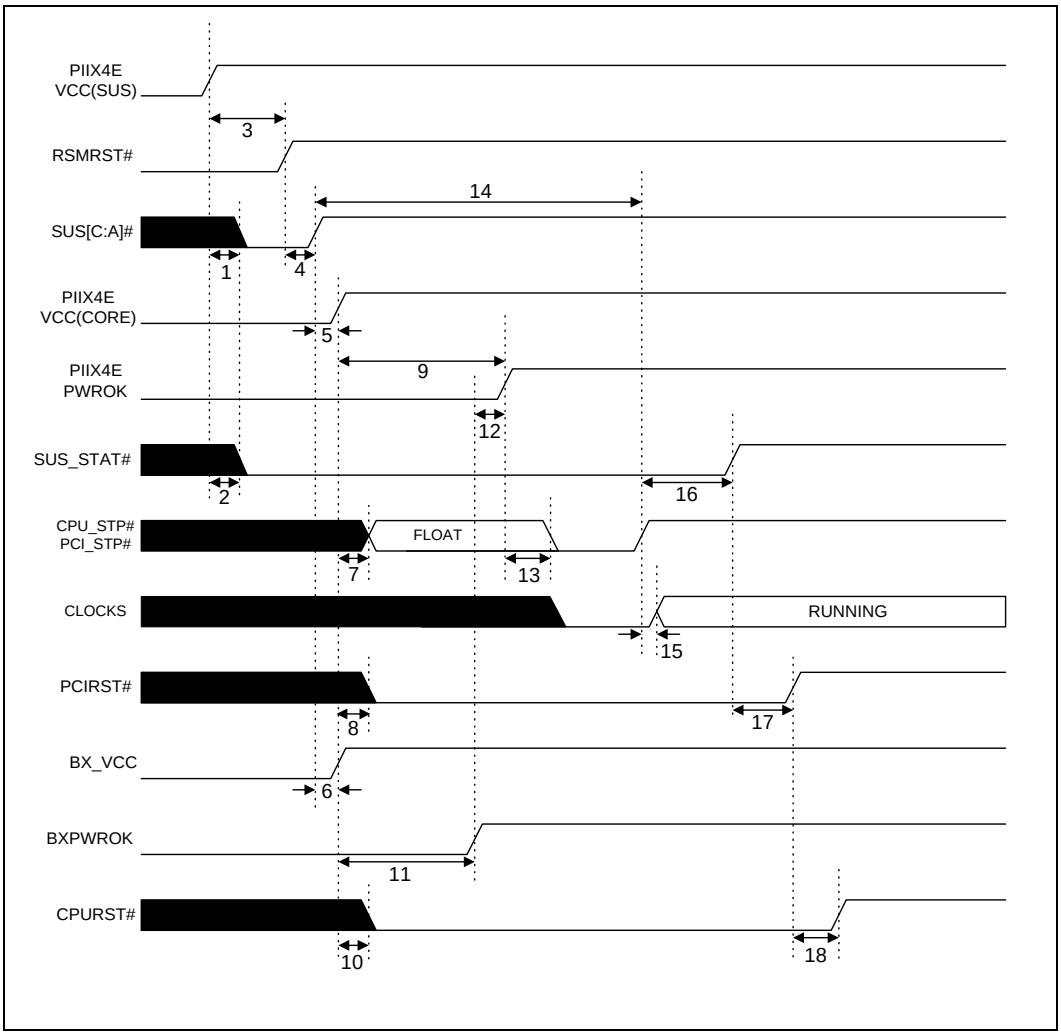


Table 60. System Power-up Sequencing Tolerances

Sym	Parameter	Min	Max	Units	Notes
t_1	PIIX4E VCC(SUS) nominal to SUS[C:A]# active		1	RTC	1
t_2	PIIX4E VCC(SUS) nominal to SUS_STAT[2:1]# active		1	RTC	1
t_3	PIIX4E VCC(SUS) nominal to RSMRST# active	1		ms	
t_4	RSMRST# inactive to SUS[C:A]# inactive	1	2	RTC	1
t_5	SUS[B]# inactive to PIIX4E VCC(CORE) nominal	0		ms	
t_6	SUS[C]# inactive to BX_VCC nominal	0		ms	
t_7	PIIX4E VCC(CORE) nominal to CPU_STP#, PCI_STP# float		1	RTC	1
t_8	PIIX4E VCC(CORE) nominal to PCIRST# active		1	RTC	1
t_9	PIIX4E VCC(CORE) nominal to PIIX4E PWROK active	1		ms	
t_{10}	BX_VCC nominal to CPURST# active		10	ns	
t_{11}	BX_VCC nominal to BXPWROK active	1		ms	
t_{12}	BXPWROK active to PIIX4E PWROK active	0		ns	2
t_{13}	PIIX4E PWROK active to CPU_STP#, PCI_STP# active		1	RTC	1
t_{14}	SUS[C:A]# inactive to CPU_STP#, PCI_STP# inactive	16		ms	3
t_{15}	CPU_STP#, PCI_STP# inactive to clocks running		2	PCICLK	
t_{16}	CPU_STP#, PCI_STP# inactive to SUS_STAT[2:1]# inactive	1		ms	
t_{17}	SUS_STAT[2:1]# inactive to PCIRST# inactive		1	RTC	1
t_{18}	PCIRST# inactive to CPURST# inactive	1		ms	

NOTES:
1. One RTC unit is approximately 32 µs
2. This parameter only applies if BXPWROK will not transition to an active state within 15 ms of SUS[C:A]# de-assertion
3. This transition requires both a minimum of 16 ms wait for the clock synthesizer PLL lock and PIIX4 PWROK to be active. If PWROK goes active after 16 ms from SUS[C:A]# inactive, the transition will occur a minimum of one RTC period from PWROK active.

7.2.2.3 Suspend Resume Protocols

The suspend resume sequences are indicated to the 82443BX by the PIIX4E, using SUS_STAT# and PCIRST#. In addition, the 82443BX contains NREF_EN and CRst_En configuration bits that participate in the suspend resume sequences.

As a result of suspend resume, the 82443BX performs the following activities:

- Changing its refresh mode
- Performing internal and processor reset
- Isolate or re-enable normal IO buffers

Table 61 indicates the suspend resume events and activities.

Table 61. Suspend Resume Events And Activities

SUSSTAT#	PCIRST#	CrstEn	Reset	Refresh	I/O Buffers
Assert	Inactive	-	-	Switch to suspend refresh	Isolate
Deassert	Active	-	Reset exclude resume/ref logic	Suspend refresh NREF_EN remains inactive	Enable
Deassert	Inactive	0	No resets	Auto switch to normal ref NREF_EN is set	Enable
Deassert	Inactive	1	Reset processor only	Auto switch to normal ref NREF_EN is set	Enable

The requirements for suspending the 82443BX are:

- The system must be idle when SUS_STAT# is asserted. There must be no active processor or bus masters' cycles and there must be no meaningful pending cycle's information in a chipset or peripheral device's buffers.
- After the assertion of SUS_STAT#, the PIIX4E provides the 82443BX 32 µs with stable power and clocks to perform the necessary suspend sequence.
- The PCICLK must not be stopped with CLKRUN# during the suspend sequence.
- The 82443BX isolates its IO buffers within less than 32 µs time allocated from SUS_STAT# assertion.
  - — The 82443BX does not isolate PCIRST# (being pulled up) or clock inputs. The clock inputs are driven low by the clock synthesizer, and 32 µs later the clock synthesizer device may be powered down.

The requirements for resuming the 82443BX are:

- Power and clocks must be stable for at least 1 ms before SUS_STAT# is deasserted.
- When resuming from POS, STPCLK# remains active for about 100 µs after SUS_STAT# deassertion, to allow an automatic switch to normal DRAM operation before processor pending cycles take place.

The 82443BX provides isolation of its I/O buffers during POS and STR. During the events that were specified in Table 61, the isolation takes effect. Table 62 provides information about the state of each of the 82443BX signals during POS and STR.

Table 62. 443BX Signal States During POS and STR Modes (Sheet 1 of 3)

Signal Name	State During POS/STR
CPURST#	Three-state
A[31:3]#	Three-state
HD[63:0]#	Three-state
ADS#	Three-state
BNR#	Three-state
BPRI#	Three-state
DBSY#	Three-state
DEFER#	Three-state
DRDY#	Three-state
HIT#	Three-state
HITM#	Three-state
HLOCK#	
HREQ[4:0]#	Three-state
HTRDY#	Three-state
RS[2:0]#	Three-state
RASA[5:0]# / CSA[5:0]#	High1
RASB[5:0]# / CSB[5:0]#	High1
CKE[3:2] / CSA[7:6]#	Low/High2
CKE[5:4] / CSB[7:6]#	Low/High2
CASA[7:0]# / DQMA[7:0]#	High1
CASB[5,1]# / DQMB[5,1]#	High1
GCKE / CKE1	Low/High2
SRAS[B:A]#	Low/High2
CKE0 / FENA	Low/High2
SCAS[B:A]#	High/Low2
MAA[13:0]	Driven3
MAB[9:7]# / MAB[13,10]	Driven3
MAB[12:11]#	Driven3
MAB[6:0]#	Driven3
WEA#, WEB#	High
MD [63:0]	Driven3
MECC[7:0]	Driven3
AD[31:0]	Low
DEVSEL#	Three-state
FRAME#	Three-state
IRDY#	Three-state
C/BE[3:0]#	Low
PAR	Low

NOTES:
1. SDRAM Mode: After putting the SDRAMs into self-refresh mode, these signals are driven high. EDO Mode: For self-refresh mode, RAS and CAS are driven low. Otherwise, the 82443BX continues to refresh during the POS/STR state.
2. SDRAM Mode: SRAS#, SCAS#, CKE[5:0] and GCKE are driven to the first value listed. EDO Mode: These signals are driven to the second value listed.
3. MA lines are always driven by the 82443BX, except for MAB[13:11,9:0]# and MAB10, which are three-stated during reset. MD/MECC are always driven by the 82443BX when there is no active cycle. The values driven on MA, MD and MECC are indeterminate during and after reset.

Table 62. 443BX Signal States During POS and STR Modes (Sheet 2 of 3)

Signal Name	State During POS/STR
PLOCK#	Three-state
TRDY#	Three-state
SERR#	Three-state
STOP#	Three-state
PHOLD#	Three-state
PHLDA#	Three-state
WSC#	Three-state
PREQ[4:0]#	Three-state
PGNT[4:0]#	Three-state
PIPE#	Three-state
SBA[7:0]	Three-state
RBF#	Three-state
ST[2:0]	Low
AD_STBA	Three-state
AD_STBB	Three-state
SB_STB	Three-state
G_FRAME#	Three-state
G_IRDY#	Three-state
G_TRDY#	Three-state
G_STOP#	Three-state
G_DEVSEL#	Three-state
G_REQ#	Three-state
G_GNT#	Three-state
G_AD[31:0]	Low
G_C/BE[3:0]#	Low
G_PAR	Low
HCLKIN	
PCLKIN	
DCLKO	Low
DCLKRD	
DCLKWR	
CRESET#	Three-state
PCIRST#	
GCLKIN	
GCLKO	Low
TESTIN#	
SMBCLK	Three-state

NOTES:
1. SDRAM Mode: After putting the SDRAMs into self-refresh mode, these signals are driven high. EDO Mode: For self-refresh mode, RAS and CAS are driven low. Otherwise, the 82443BX continues to refresh during the POS/STR state.
2. SDRAM Mode: SRAS#, SCAS#, CKE[5:0] and GCKE are driven to the first value listed. EDO Mode: These signals are driven to the second value listed.
3. MA lines are always driven by the 82443BX, except for MAB[13:11,9:0]# and MAB10, which are three-stated during reset. MD/MECC are always driven by the 82443BX when there is no active cycle. The values driven on MA, MD and MECC are indeterminate during and after reset.

Table 62. 443BX Signal States During POS and STR Modes (Sheet 3 of 3)

Signal Name	State During POS/STR
SMBDATA	Three-state
CLKRUN#	Three-state
SUSTAT#	

NOTES:
1. SDRAM Mode: After putting the SDRAMs into self-refresh mode, these signals are driven high. EDO Mode: For self-refresh mode, RAS and CAS are driven low. Otherwise, the 82443BX continues to refresh during the POS/STR state.
2. SDRAM Mode: SRAS#, SCAS#, CKE[5:0] and GCKE are driven to the first value listed. EDO Mode: These signals are driven to the second value listed.
3. MA lines are always driven by the 82443BX, except for MAB[13:11,9:0]# and MAB10, which are three-stated during reset. MD/MECC are always driven by the 82443BX when there is no active cycle. The values driven on MA, MD and MECC are indeterminate during and after reset.

7.2.2.4 82443BX Suspend/Resume Sequences and Timing

Table 63 indicates the suspend/resume timing tolerances.

Table 63. Suspend/Resume Timing Tolerances

Sym	Parameter	Min	Max	Unit
t1	BX_VCC stable to BXPWROK asserted. †	1		ms
t2	BXPWROK asserted to SUS_STAT# inactive	1		ms
t3	Clocks running to SUS_STAT# inactive, guarantee	1		ms
t4	BX_VCC active and BXPWROK inactive to CPURST# active		10	ns
t5	SUS_STAT# deasserted to PCIRST# de-asserted, guarantee		32	µs
t6	PCIRST# deasserted to CPURST# deasserted	1		ms
t7	SUS_STAT# deasserted to buffers valid	2		HCLK
t8	SUS_STAT# asserted to clocks stopped, guarantee	32		µs
t9	SUS_STAT# asserted to suspend refresh		32	µs
t10	SUS_STAT# asserted to buffers isolated		32	µs
t11	PCIRST# asserted to CPURST# asserted		10	ns
t12	PCIRST# asserted to SUS_STAT# de-asserted, guarantee	1		ms
t13	SUS_STAT# de-asserted to normal refresh		32	µs
t14	SUS_STAT# de-asserted to CPURST# asserted	0	4	HCLK
t15	CPURST# pulse width	1		ms

† “BX_VCC stable” means BX_VCC is within the specified Functional Operating Range.

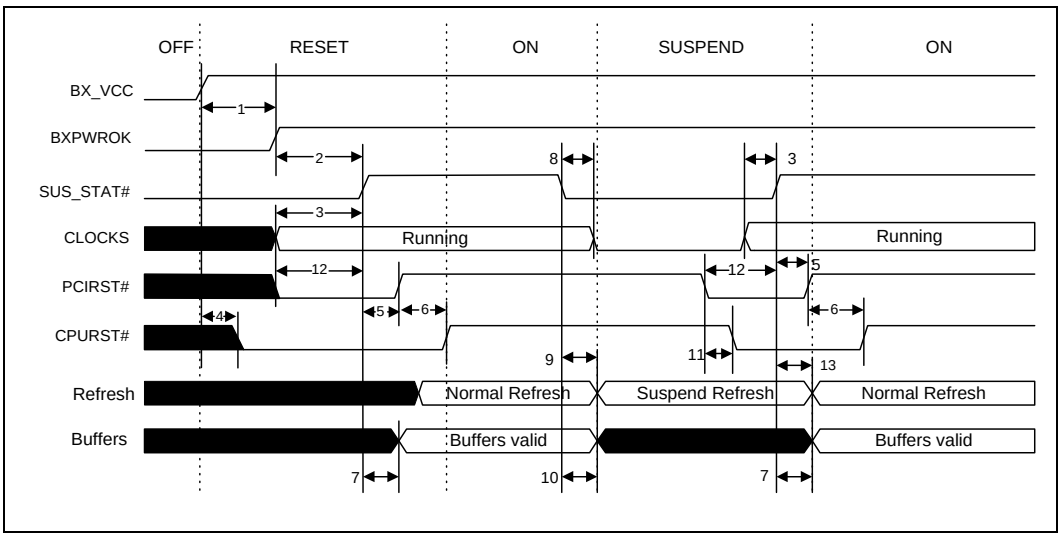
7.2.2.5 Suspend/Resume with PCIRST# Active

The following resume sequence is typically used when resuming from STR. It includes the following components:

- BXPWROK must transition from inactive (low) to active (high) a minimum of 1 ms after BX_VCC is within the specified Functional Operating Range.
- When 15 ms or more may elapse from the time that the PIIX4E deasserts SUS[C:A]# until BXPWROK is asserted, BXPWROK must be asserted before or simultaneous to PWROK being asserted to the PIIX4E.
- Upon resume, the 82443BX detects that the PCIRST# signal is active (low) and drives CPURST# to the processor. Note that CPURST# is driven active based on PCIRST# timing, independent of SUS_STAT# timing.
- Based on the assertion of SUS_STAT#, the 82443BX isolates its I/O buffer within 32 µs.
- Based on the deassertion of SUS_STAT#, the 82443BX enables its I/O buffer to normal operation within 32 µs. Clock inputs and PCIRST# are never gated by the 82443BX and thus affect it before the deassertion of SUS_STAT#.
- Software must release the memory controller from its suspend refresh state to its normal refresh state.
- The 82443BX clears its internal state, with the exception of resume/refresh logic, since it sampled PCIRST# asserted.

Figure 47 shows the suspend resume sequence with PCIRST# active.

Figure 47. Suspend/Resume with PCIRST# Active



7.2.2.6 Suspend/Resume with CPURST#, PCIRST# Inactive

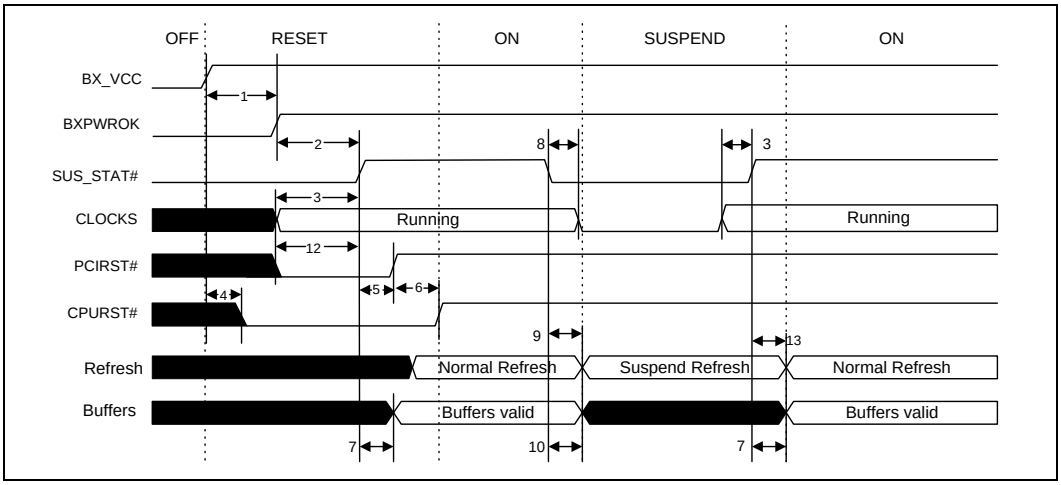
The following resume sequence is typically used when resuming from POS. It includes the following components:

- Since PCIRST# signal is inactive, per resume the 82443BX does not drive CPURST# to the processor, since CrstEn is ‘0’.

- Based on the assertion of SUS_STAT#, the 82443BX isolates its I/O buffer within 32 µs.
- Based on the deassertion of SUS_STAT#, the 82443BX enables its I/O buffer to normal operation within 32 µs.
- The 82443BX switches from suspend refresh to normal DRAM operation mode.
- The processor starts execution from the instruction just prior to the stop grant request being recognized. The 82443BX switches to normal DRAM operation before the deassertion of STPCLK#.
- The 82443BX state is not reset.

Figure 48 shows the suspend/resume sequence with CPURST#, PCIRST# inactive.

Figure 48. Suspend/Resume with CPURST#, PCIRST# Inactive



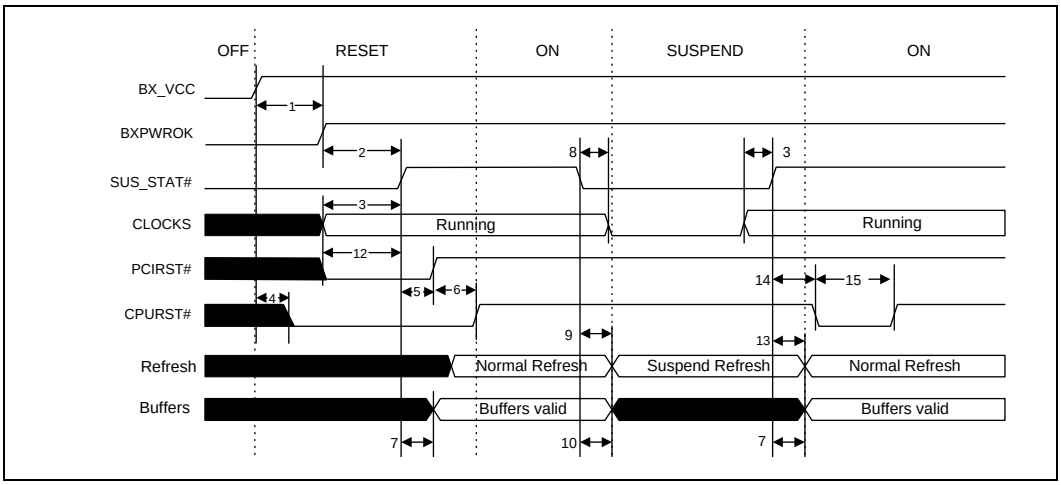
7.2.2.7 Suspend/Resume with CPURST Active, PCIRST# Inactive

The following resume sequence is typically used when resuming from POS. It includes the following components:

- The PCIRST# signal is inactive, upon resume the 82443BX drives CPURST# to the processor since CrstEn is ‘1’. CPURST# is active for 1 ms.
- Based on the assertion of SUS_STAT#, the 82443BX isolates its I/O buffer within 32 µs.
- Based on the deassertion of SUS_STAT#, the 82443BX enables its I/O buffer to normal operation within 32 µs.
- The 82443BX automatically switches from suspend refresh to normal DRAM operation mode when SUS_STAT# deassertion is detected.
- The 82443BX state is not reset.

Figure 49 shows the suspend/resume sequence with CPURST# active, PCIRST# inactive.

Figure 49. Suspend/Resume with CPURST# Active, PCIRST# Inactive



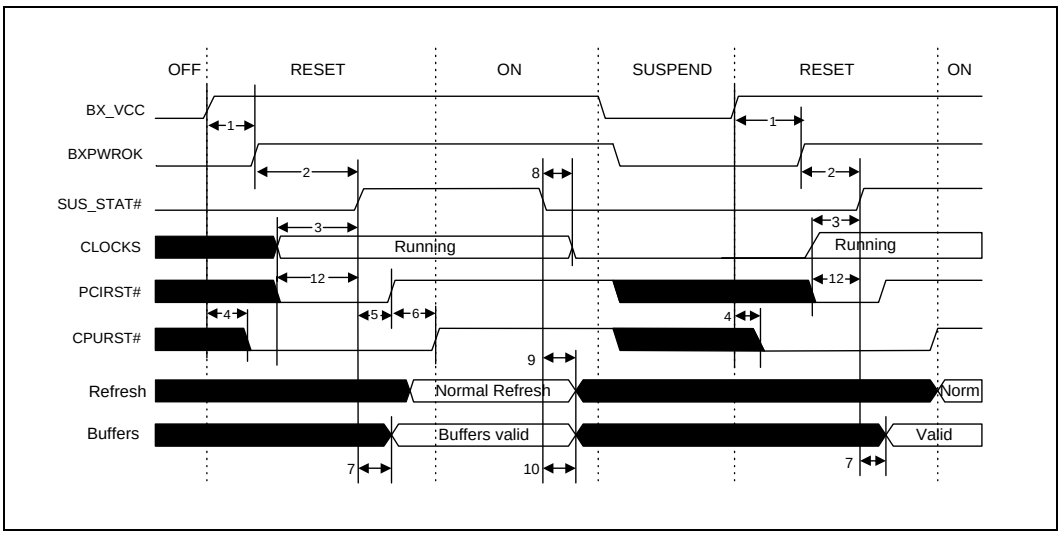
7.2.2.8 Suspend/Resume from STD

The following resume sequence is typically used when resuming from STD. It includes the following components:

- When BXPWROK is sampled low ‘0’, the 82443BX undergoes a complete reset and asserts CPURST#.
- Based on the deassertion of SUS_STAT#, the 82443BX enables its buffer to normal operation within less than 32 µs. Clock inputs and PCIRST# are never gated by the 82443BX and thus affect it before the deassertion of SUS_STAT#.
- Software must release the memory controller from its suspend refresh state to its normal refresh state, and enable refresh with the appropriate refresh rate.

Figure 50 shows the suspend/resume sequence from STD.

Figure 50. Suspend/Resume from STD



7.3 Low-Power Module Power Sequencing

7.3.1 Voltage Regulator Control

The Low-Power Module VR_ON pin on the Low-Power Module connector allows a digital signal (3.3 V, 5 V safe) to control the voltage regulator. The system manufacturer can use this signal to turn the Pentium III processor module voltage regulator on or off. VR_ON should be controlled as a function of the same digital control signal (SUSB#) used to control the system's switched 5-V /3.3-V power planes. The PIIX4E defines Suspend to RAM (STR) as the power-management state in which power is physically removed from most of the system components except DRAM. In this state, the SUSB# pin on the PIIX4E controls these power planes.

Caution: VR_ON should switch high only when the following conditions are met: V_5(s) ≥ 4.5 V, and V_DC ≥ 4.75 V. Turning on VR_ON prior to meeting these conditions will severely damage the module.

7.3.2 Voltage Signal Definition and Sequencing

Table 64 indicates the voltage signal definitions and sequences.

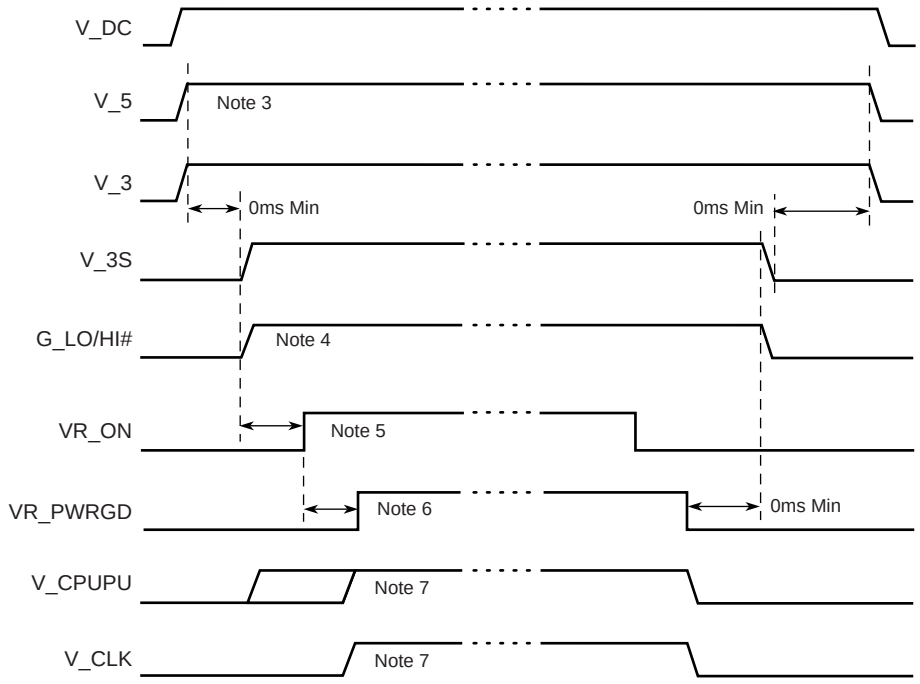
Table 64. Voltage Signal Definitions and Sequences

Signal	Source	Definitions and Sequences
V_DC	System Electronics	DC voltage driven from the power supply and is required to be 5 V ± 5%. V_DC powers the processor module's DC-to-DC converter for processor core and I/O voltages. The processor module cannot be inserted or removed while V_DC is powered on.
V_3	System Electronics	V_3 is supplied by the system electronics for the 82443BX.
V_5	System Electronics	V_5 is supplied by the system electronics for the 82443BX's 5-V reference voltage and processor module's voltage regulator.
V_3S	System Electronics	V_3S is supplied by the system electronics for the L2 cache devices. Each must be powered off during system STR and STD states.
VR_ON	System Electronics	VR_ON enables the processor module's voltage regulator circuit. When driven active high (3.3 V) the voltage regulator circuit on the processor module is activated. The signal driving VR_ON should be a digital signal with a rise/fall time of less than or equal to 1 µs.
V_CORE (also used as host bus GTL+ termination voltage VTT)	Processor module only; not on module interface.	A result of VR_ON being asserted, V_CORE is an output of the DC-DC regulator on the processor module and is driven to the core voltage of the processor. It is also used as the host bus GTL+ termination voltage (VTT).
V_BSB_IO	Processor module only; not on module interface.	V_BSB_IO is 1.8 V. The system electronics uses this voltage to power the L2 cache-to-processor interface circuitry.
VR_PWRGD	Processor module	Upon sampling the voltage level of V_CORE for the processors, minus tolerances for ripple, VR_PWRGD is driven active high (3.3 V) for the system electronics to sample prior to providing PWROK to the PIIX4. If VR_PWRGD is not sampled active within 1 second of the assertion of VR_ON the system electronics should de-assert VR_ON.
V_CPUPU	Processor module	V_CPUPU is 2.5 V. The system electronics uses this voltage to power the PIIX4E-to-processor interface circuitry
V_CLK	Processor module	V_CLK is 2.5 V. The system electronics uses this voltage to power the HCLK_(0:1) drivers for the processor clock.

Figure 51 details the sequencing of signals and voltage planes required for normal operation of the processor module.

The processor module provides the VR_PWRGD signal, which indicates that the voltage regulator power is operating at a stable voltage level. The system manufacturer should use this signal on the system electronics to control power inputs and to gate PWROK to the PIIX4E.

Figure 51. Power On Sequence



NOTES:
1. PWROK on the I/O board should be active on when VR_PWRGD is active and V_3S is good.
2. CPU_RST from the I/O board should be active for a minimum of 6 ms after PWROK is active and PLL_STP# and CPU_STP# are inactive. Note that PLL_STP# is an AND condition of RSMRST# and SUSB# on the PIIX4E.
3. This is the 5-V power supplied to the Low Power Module. This should be the first 5.0-V plane to power up. Stays on during suspend.
4. G_LO/HI# must be high at the rising edge of VR_ON. If it is not, the BIOS must assert this signal very early in core execution.
5. V_DC ≥ 4.75 V, V_5 ≥ 4.5 V, V_3S ≥ 3.0 V.
6. When asserting VR_ON, VR_PWRGD is guaranteed to be stable after 6 ms.
7. V_CPUPU and V_CLK are generated on the module.