REFERENCE ONLY

32-MBIT FlashFile™ MEMORY

DD28F032SA

- **User-Selectable 3.3 V or 5 V V_{CC}**
- **User-Configurable x8 or x16 Operation**
- **70 ns Maximum Access Time**
- **28.6 MB/sec Burst Write Transfer Rate**
- **1 Million Typical Erase Cycles per Block**
- **56-Lead, 1.2 x 14 x 20 mm Advanced Dual Die TSOP Package Technology**
- **64 Independently Lockable Blocks**
- **Revolutionary Architecture**
  - **100% Backwards-Compatible with Intel 28F016SA**
  - **Pipelined Command Execution**
  - **Program during Erase**
- **2 mA Typical I_{CC} in Static Mode**
- **2 µA Typical Deep Power-Down**
- **State-of-the-Art 0.6 µm ETOX™ IV Flash Technology**

Intel's DD28F032SA 32-Mbit FlashFile™ memory is a revolutionary architecture which enables the design of truly mobile, high performance, personal computing and communication products. With innovative capabilities, low power operation and very high read/program performance, the DD28F032SA is also the ideal choice for designing embedded mass storage flash memory systems.

The DD28F032SA is the result of highly-advanced packaging innovation which encapsulates two 28F016SA die in a single Dual Die Thin Small Outline Package (DDTSOP).

The DD28F032SA is the highest density, highest performance nonvolatile read/program solution for solid-state storage applications. Its symmetrically-blocked architecture (100% compatible with the 28F016SA 16-Mbit FlashFile memory), very high-cycling, low-power 3.3 V operation, very fast program and read performance and selective block locking provide a highly flexible memory component suitable for high-density memory cards, Resident Flash Arrays and PCMCIA-ATA Flash Drives. The DD28F032SA's dual read voltage enables the design of memory cards which can be read/written in 3.3 V and 5.0 V systems interchangeably. Its x8/x16 architecture allows the optimization of memory to processor interface. The flexible block locking option enables bundling of executable application software in a Resident Flash Array or memory card. The DD28F032SA will be manufactured on Intel's 0.6 µm ETOX IV technology.

New Design Recommendations:

For new 3.3 V and 5 V V_{CC} designs with this device, Intel recommends using the Intel StrataFlash™ memory technology. Reference *Intel StrataFlash™ Technology 32 and 64 Mbit 28F320J5, 28F640J5* datasheet, order number 290606.

This document is also available at Intel's website, http://www.intel.com/design/flcomp.

December 1997

Order Number: 290490-006

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The DD28F032SA may contain design defects or errors known as errata. Current characterized errata are available upon request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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REVISION HISTORY

Number	Description
-001	Original Version
-002	Never Published
-003	Full Datasheet with Specifications CE_0#, CE_1# control 28F016SA No. 1 CE_0#, CE_2# control 28F016SA No. 2
-004	DC Characteristics (3.3V V_{CC}): I_{CCR}[1] (TTL): BYTE# = V_{IL} or V_{IH} Full Chip Erase Time (3.3V V_{CC}) = 51.2 sec typ Full Chip Erase Time (5.0V V_{CC}) = 38.4 sec typ Section 6.7: Added specifications t_{PHEL3}, t_{PHEL5} TSOP dimension A_1 = 0.05 mm (min) Revised Product Status to Preliminary t_{WHGL} (3.3V) = 120 ns Minor cosmetic changes
-005	Updated AC/DC parameters
-006	Added *New Design Recommendations* section to cover page

SEE NEW DESIGN RECOMMENDATIONS

1.0 PRODUCT OVERVIEW

The DD28F032SA is a high-performance 32-Mbit (33,554,432-bit) block erasable nonvolatile random access memory organized as either 2 Mword x 16, or 4 Mbyte x 8. The DD28F032SA is built using two 28F016SA chips encapsulated in a single 56- lead TSOP Type I package. The DD28F032SA includes sixty-four 64-KB (65,536) blocks or sixty-four 32-KW (32,768) blocks.

The DD28F032SA architecture allows operations to be performed on a single, 16-Mbit chip at a time.

The implementation of a new architecture, with many enhanced features, will improve the device operating characteristics and results in greater product reliability and ease of use.

Among the significant enhancements on the DD28F032SA:

- 3.3V Low Power Capability
- Improved Program Performance
- Dedicated Block Program/Erase Protection

A 3/5# input pin reconfigures the device internally for optimized 3.3V or 5.0V read/program operation.

The DD28F032SA will be available in a 56-lead, 1.2 mm thick, 14 mm x 20 mm Dual Die TSOP Type I package. This form factor and pinout allow for very high board layout densities. The DD28F032SA is pinout and footprint compatible with the 28F016SA.

Two Command User Interfaces (CUI) serve as the system interface between the microprocessor or microcontroller and the internal memory operation.

Internal algorithm automation allows word/byte programs and block erase operations to be executed using a two-write command sequence to the CUI in the same way as the 28F016SA 16-Mbit FlashFile memory.

A super-set of commands has been added to the basic 28F008SA (8-Mbit FlashFile memory) command-set to achieve higher program performance and provide additional capabilities. These new commands and features include:

- Page Buffer Writes to Flash
- Command Queueing Capability
- Automatic Data Programs during Erase
- Software Locking of Memory Blocks
- Two-Byte Successive Programs in 8-bit Systems
- Erase All Unlocked Blocks

These operations can only be performed on one 16-Mbit device at a time. If the WSM is busy performing an operation, the system should not attempt to select the other device.

Writing of memory data is performed in either byte or word increments typically within 6 µs, a 33% improvement over the 28F008SA. A block erase operation erases one of the 64 blocks in typically 0.6 sec, independent of the other blocks, which is a 65% improvement over the 28F008SA.

Each block can be written and erased a minimum of 100,000 cycles. Systems can achieve typically 1 million block erase cycles by providing wear-leveling algorithms and graceful block retirement. These techniques have already been employed in many flash file systems. Additionally, wear leveling of block erase cycles can be used to minimize the program/erase performance differences across blocks.

The DD28F032SA incorporates two Page Buffers of 256 bytes (128 words) on each 28F016SA to allow page data programs. This feature can improve a system program performance by up to 4.8 times over previous flash memory devices.

All operations are started by a sequence of command writes to the device. Three Status Registers (described in detail later) and a RY/BY# output pin provide information on the progress of the requested operation.

The DD28F032SA allows queueing of the next operation while the memory executes the current operation. This eliminates system overhead when writing several bytes in a row to the array or erasing several blocks at the same time. The DD28F032SA can also perform program operations to one block of memory while performing erase of another block. However, simultaneous program and/or erase operations are not allowed on both 28F016SA devices. See *Modes of Operation*, Section 3.0.

SEE NEW DESIGN RECOMMENDATIONS

The DD28F032SA provides user-selectable block locking to protect code or data such as device drivers, PCMCIA card information, ROM-executable O/S or application code. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the DD28F032SA has a master Write Protect pin (WP#) which prevents any modifications to memory blocks whose lock-bits are set.

The DD28F032SA contains three types of Status Registers to accomplish various functions:

- A Compatible Status Register (CSR) which is 100% compatible with the 28F008SA FlashFile memory's Status Register. This register, when used alone, provides a straightforward upgrade capability to the DD28F032SA from a 28F008SA-based design.
- A Global Status Register (GSR) which informs the system of Command Queue status, Page Buffer status, and overall Write State Machine (WSM) status.
- 64 Block Status Registers (BSRs) which provide block-specific status information such as the block lock-bit status.

The GSR and BSR memory maps for byte-wide and word-wide modes are shown in Figures 4 and 5.

The DD28F032SA incorporates an open drain RY/BY# output pin. This feature allows the user to OR-tie many RY/BY# pins together in a multiple memory configuration such as a Resident Flash Array. Other configurations of the RY/BY# pin are enabled via special CUI commands and are described in detail in the *16-Mbit Flash Product Family User's Manual*.

The DD28F032SA also incorporates three chip-enable input pins, CE_0#, CE_1# and CE_2#. The active low combination of CE_0# and CE_1# controls the first 28F016SA. The active low combination of CE_0# and CE_2# controls the second 28F016SA.

The BYTE# pin allows either x8 or x16 read/programs to the DD28F032SA. BYTE# at logic low selects 8-bit mode with address A_0 selecting between low byte and high byte. On the other hand, BYTE# at logic high enables 16-bit operation with address A_1 becoming the lowest order address and address A_0 is not used (don't care). A device block diagram is shown in Figure 1.

The DD28F032SA is specified for a maximum access time of 70 ns (t_{ACC}) at 5.0V operation (4.75V to 5.25V) over the commercial temperature range (0°C to +70°C). A corresponding maximum access time of 150 ns at 3.3V (3.0V to 3.6V and 0°C to +70°C) is achieved for reduced power consumption applications.

The DD28F032SA incorporates an Automatic Power Saving (APS) feature which substantially reduces the active current when the device is in static mode of operation (addresses not switching).

A deep power-down mode of operation is invoked when the RP# (called PWD# on the 28F008SA) pin is driven low. This mode provides additional write protection by acting as a device reset pin during power transitions. In the deep power-down state, the WSM is reset (any current operation will abort) and the CSR, GSR and BSR registers are cleared.

A CMOS standby mode of operation is enabled when either CE_0#, or both CE_1# and CE_2#, transition high and RP# stays high with all input control pins at CMOS levels.

2.0 DEVICE PINOUT

The DD28F032SA Standard 56-Lead Dual Die TSOP Type I pinout configuration is shown in Figure 2.

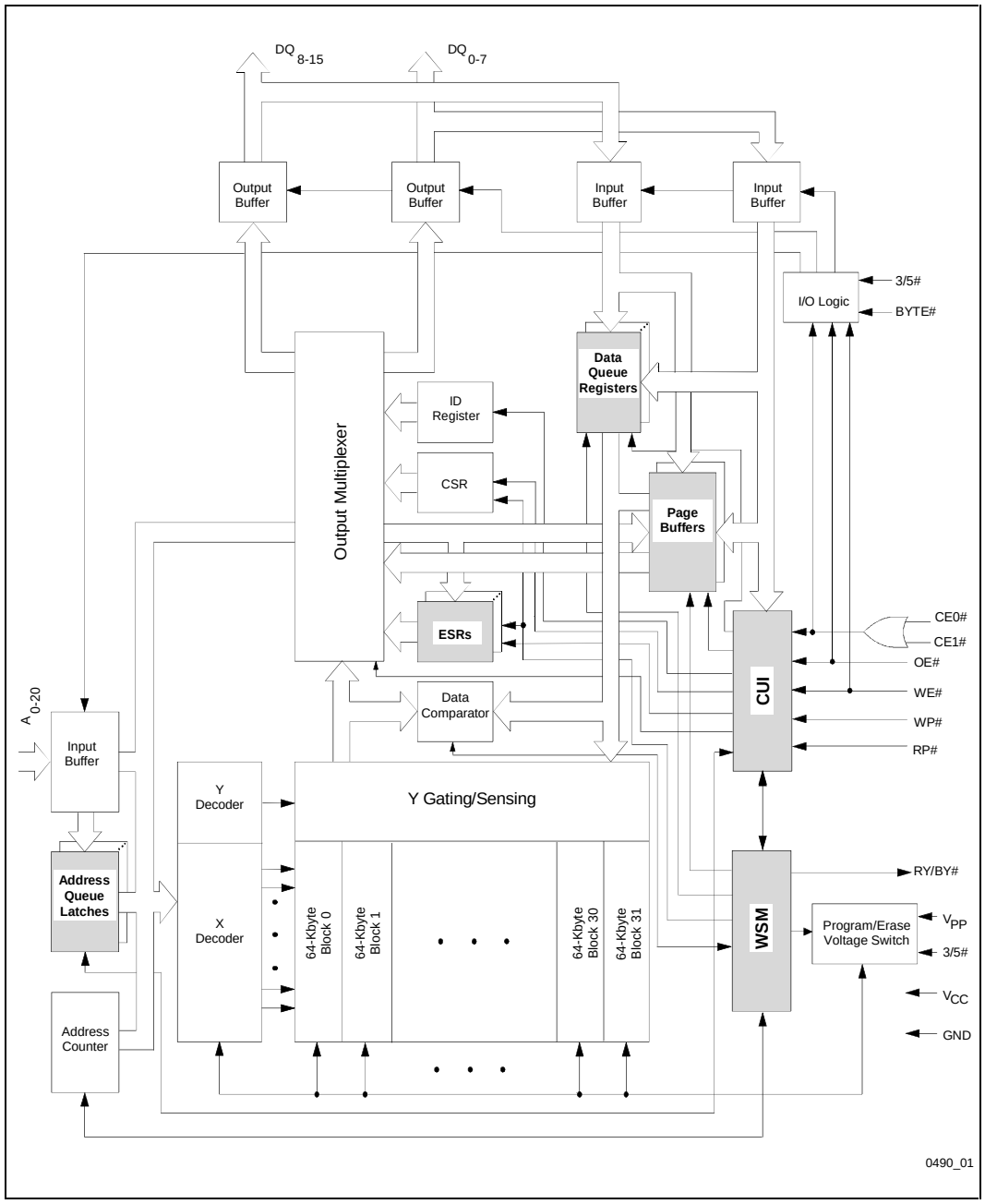


Figure 1. Block Diagram of 16-Mbit Devices in DD28F032SA
Architectural Evolution Includes Page Buffers, Queue Registers and Extended Registers

SEE NEW DESIGN RECOMMENDATIONS

2.1 Lead Descriptions

Symbol	Type	Name and Function
A_0	INPUT	**BYTE-SELECT ADDRESS:** Selects between high and low byte when device is in x8 mode. This address is latched in x8 data programs. Not used in x16 mode (i.e., the A_0 input buffer is turned off when BYTE# is high).
A_1–A_{15}	INPUT	**WORD-SELECT ADDRESSES:** Select a word within one 64-Kbyte block. A_{6-15} selects 1 of 1024 rows, and A_{1-5} selects 16 of 512 columns. These addresses are latched during data programs.
A_{16}–A_{20}	INPUT	**BLOCK-SELECT ADDRESSES:** Select 1 of 32 erase blocks in each of the two 28F016SAs. These addresses are latched during data programs, block erase and lock block operations.
DQ_0–DQ_7	INPUT/OUTPUT	**LOW-BYTE DATA BUS:** Inputs data and commands during CUI write cycles. Outputs array, buffer, identifier or status data in the appropriate read mode. Floated when the chip is de-selected or the outputs are disabled.
DQ_8–DQ_{15}	INPUT/OUTPUT	**HIGH-BYTE DATA BUS:** Inputs data during x16 data program operations. Outputs array, buffer or identifier data in the appropriate read mode; not used for Status Register reads. Floated when the chip is de-selected or the outputs are disabled.
CE_0# CE_X# = CE_1# or CE_2#	INPUT	**CHIP ENABLE INPUTS**: Activate the device's control logic, input buffers, decoders and sense amplifiers. CE_0#/CE_1# enable/disable the first 28F016SA (16 Mbit No. 1) while CE_0#/CE_2# enable/disable the second 28F016SA (16 Mbit No. 2). CE_0# active low enables chip operation while CE_1# or CE_2# select between the first and second device, respectively CE_1# and CE_2# must not be active low simultaneously. Reference Table 3.0.
RP#	INPUT	**RESET/POWER-DOWN:** RP# low places the device in a deep power-down state. All circuits that burn static power, even those circuits enabled in standby mode, are turned off. When returning from deep power-down, a recovery time is required to allow these circuits to power-up. When RP# goes low, any current or pending WSM operation(s) are terminated, and the device is reset. All Status Registers return to ready (with all status flags cleared).
OE#	INPUT	**OUTPUT ENABLE:** Gates device data through the output buffers when low. The outputs float to tri-state off when OE# is high. **NOTE:** CE_X# overrides OE#, and OE# overrides WE#.
WE#	INPUT	**WRITE ENABLE:** Controls access to the CUI, Page Buffers, Data Queue Registers and Address Queue Latches. WE# is active low, and latches both address and data (command or array) on its rising edge.
RY/BY#	OPEN DRAIN OUTPUT	**READY/BUSY:** Indicates status of the internal WSM. When low, it indicates that the WSM is busy performing an operation. RY/BY# high indicates that the WSM is ready for new operations (or WSM has completed all pending operations), or block erase is suspended, or the device is in deep power-down mode. This output is always active (i.e., not floated to tri-state off when OE# or CE_0#/CE_1#/CE_2# are high), except if a RY/BY# Pin Disable command is issued.

2.1 Lead Descriptions (Continued)

Symbol	Type	Name and Function
WP#	INPUT	**WRITE PROTECT:** Erase blocks can be locked by writing a nonvolatile lock-bit for each block. When WP# is low, those locked blocks as reflected by the Block-Lock Status bits (BSR.6), are protected from inadvertent data programs or block erases. When WP# is high, all blocks can be written or erased regardless of the state of the lock-bits. The WP# input buffer is disabled when RP# transitions low (deep power-down mode).
BYTE#	INPUT	**BYTE ENABLE:** BYTE# low places device in x8 mode. All data is then input or output on DQ_{0-7}, and DQ_{8-15} float. Address A_0 selects between the high and low byte. BYTE# high places the device in x16 mode, and turns off the A_0 input buffer. Address A_1 then becomes the lowest order address.
3/5#	INPUT	**3.3/5.0 VOLT SELECT:** 3/5# high configures internal circuits for 3.3V operation. 3/5# low configures internal circuits for 5.0V operation. **NOTES:** Reading the array with 3/5# high in a 5.0V system could damage the device. There is a significant delay from 3/5# switching to valid data.
V_{PP}	SUPPLY	**ERASE/PROGRAM POWER SUPPLY:** For erasing memory array blocks or writing words/bytes/pages into the flash array.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY (3.3V ± 0.3V, 5.0V ± 0.5V, 5.0V ± 0.25V):** Do not leave any power pins floating.
GND	SUPPLY	**GROUND FOR ALL INTERNAL CIRCUITRY:** Do not leave any ground pins floating.
NC		**NO CONNECT:** Lead may be driven or left floating.

SEE NEW DESIGN RECOMMENDATIONS

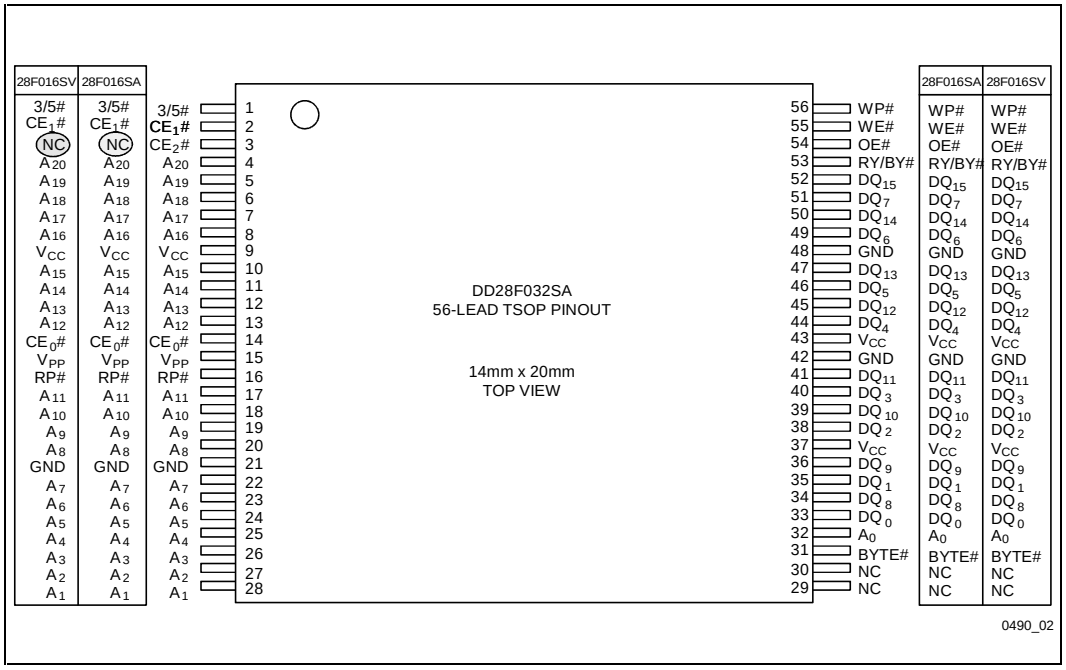


Figure 2. Dual Die TSOP Pinout Configuration

3.0 MODES OF OPERATION

RP#	CE_0#	CE_1#	CE_2#	28F016SA No. 1	28F016SA No. 2	DD28F032SA Chip
0	X	X	X	DPD	DPD	DPD
1	1	X	X	Standby	Standby	Standby
1	0	0	1	Standby	Active	Active
1	0	1	0	Active	Standby	Active
1	0	1	1	Standby	Standby	Standby
1	0	0	0	Illegal Condition		

NOTES:

X = Don't Care

DPD = Deep Power-Down

28F016SA No. 1 = First 16-Mbit Device

28F016SA No. 2 = Second 16-Mbit Device

4.0 MEMORY MAPS

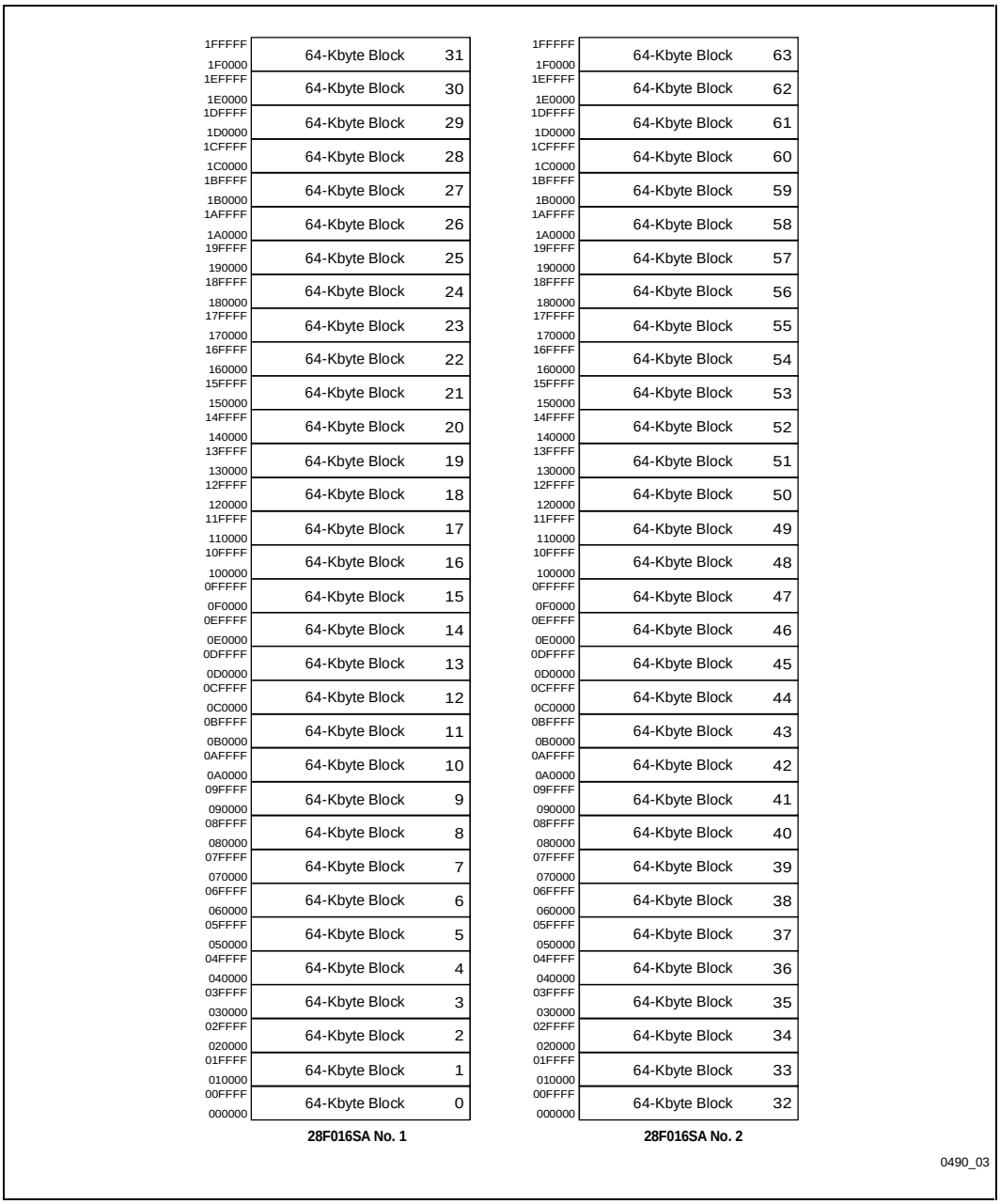


Figure 3. DD28F032SA Memory Map (Byte-Wide Mode)

SEE NEW DESIGN RECOMMENDATIONS

4.1 Extended Status Registers Memory Map for Either 28F016SA No. 1 or 28F016SA No. 2

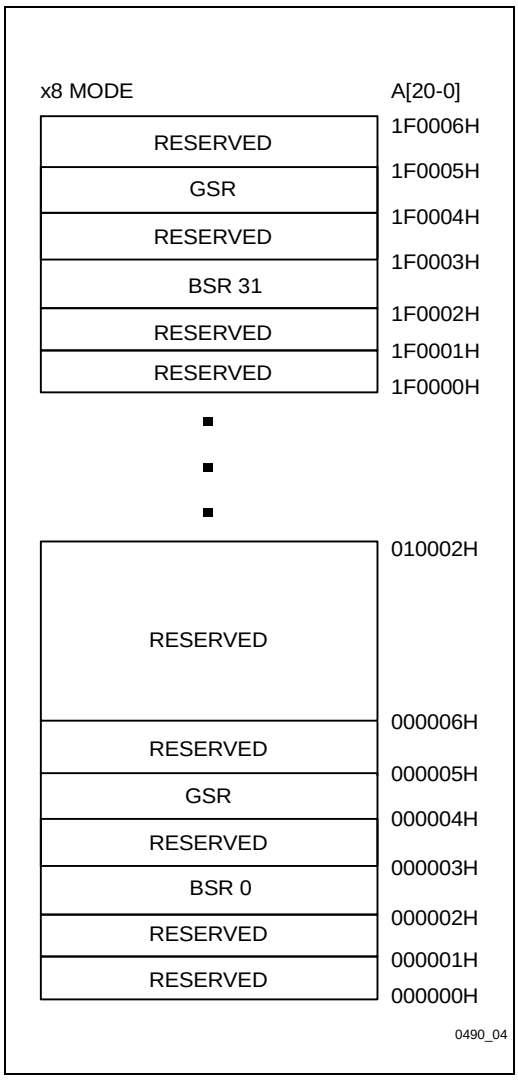


Figure 4. Extended Status Register Memory Map (Byte-Wide Mode)

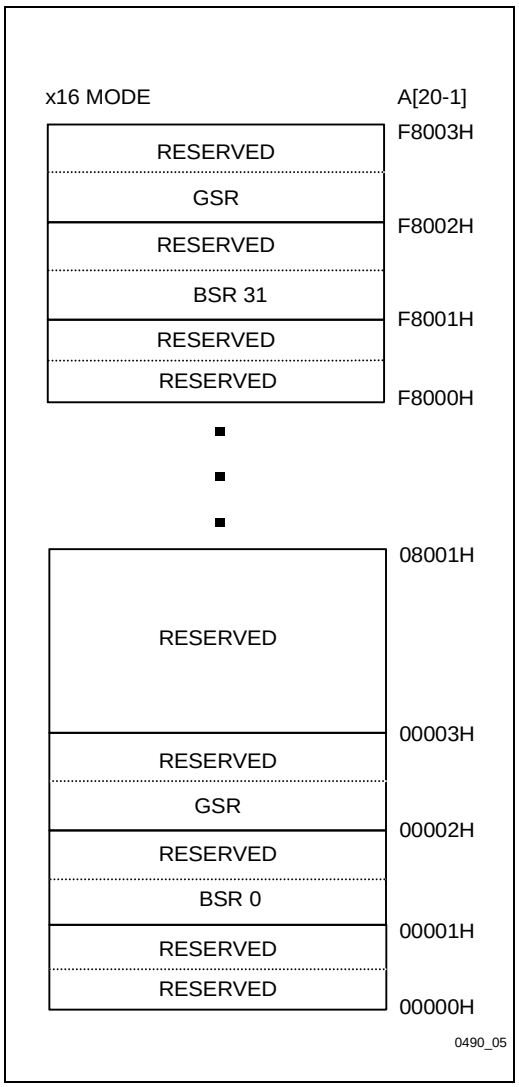


Figure 5. Extended Status Register Memory Map (Word-Wide Mode)

5.0 BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS

5.1 Bus Operations for Word-Wide Mode (BYTE# = V_{IH})

Mode	Notes	RP#	CE_X#(8)	CE_0#	OE#	WE#	A_1	DQ_{0-15}	RY/BY#
Read	1,2,7	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X
Output Disable	1,6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	High Z	X
Standby	1,6,7	V_{IH}	V_{IL} V_{IH} V_{IH}	V_{IH} V_{IL} V_{IH}	X	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Manufacturer ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	0089H	V_{OH}
Device ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	66A0H	V_{OH}
Write	1,5,6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X

5.2 Bus Operations for Byte-Wide Mode (BYTE# = V_{IL})

Mode	Notes	RP#	CE_X#(8)	CE_0#	OE#	WE#	A_0	DQ_{0-7}	RY/BY#
Read	1,2,7	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X
Output Disable	1,6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	High Z	X
Standby	1,6,7	V_{IH}	V_{IL} V_{IH} V_{IH}	V_{IH} V_{IL} V_{IH}	X	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Manufacturer ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	89H	V_{OH}
Device ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A0H	V_{OH}
Write	1,5,6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X

NOTES:

1. X can be V_{IH} or V_{IL} for address or control pins except for RY/BY#, which is either V_{OL} or V_{OH}.
2. RY/BY# output is open drain. When the WSM is ready, block erase is suspended or the device is in deep power-down mode, RY/BY# will be at V_{OH} if it is tied to V_{CC} through a resistor. RY/BY# at V_{OH} is independent of OE# while a WSM operation is in progress.
3. RP# at GND ± 0.2V ensures the lowest deep power-down current.
4. A_0 and A_1 at V_{IL} provide device manufacturer codes in x8 and x16 modes respectively. A_0 and A_1 at V_{IH} provide device ID codes in x8 and x16 modes respectively. All other addresses are set to zero.
5. Commands for different block erase operations, data program operations or lock-block operations can only be successfully completed when $V_{PP} = V_{PPH}$.
6. While the WSM is running, RY/BY# in level-mode (default) stays at V_{OL} until all operations are complete. RY/BY# goes to V_{OH} when the WSM is not busy or in erase suspend mode.
7. RY/BY# may be at V_{OL} while the WSM is busy performing various operations; for example, a Status Register read during a data program operation.
8. CE_X# = CE_1# or CE_2#.

SEE NEW DESIGN RECOMMENDATIONS

5.3 28F008SA Compatible Mode Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	xxFFH	Read	AA	AD
Intelligent Identifier	1	Write	X	xx90H	Read	IA	ID
Read Compatible Status Register	2	Write	X	xx70H	Read	X	CSRD
Clear Status Register	3	Write	X	xx50H			
Word/Byte Program		Write	X	xx40H	Write	PA	PD
Alternate Word/Byte Program		Write	X	xx10H	Write	PA	PD
Block Erase/Confirm		Write	X	xx20H	Write	BA	xxD0H
Erase Suspend/Resume		Write	X	xxB0H	Write	X	xxD0H

ADDRESS
A = Array Address
BA = Block Address
IA = Identifier Address
PA = Program Address
X = Don't Care

DATA
AD = Array Data
CSRD = CSR Data
ID = Identifier Data
PD = Program Data

NOTES:
1. Following the Intelligent Identifier command, two read operations access the manufacturer and device signature codes.
2. The CSR is automatically available after device enters data program, block erase, or suspend operations.
3. Clears CSR.3, CSR.4 and CSR.4. Also clears GSR.4 and all BSR.4 and BSR.2 bits.
4. The upper byte of the data bus (DQ_{8-15}) during command writes is a "Don't Care" in x16 operation of the device.

   See Status Register definitions.

5.4 28F016SA-Performance Enhancement Command Bus Definitions

Command	Mode	Notes	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
			Oper	Addr	Data(12)	Oper	Addr	Data(12)	Oper	Addr	Data
Read Extended Status Register		1	Write	X	xx71H	Read	RA	GSRD BSRD			
Page Buffer Swap		7	Write	X	xx72H						
Read Page Buffer			Write	X	xx75H	Read	PBA	PD			
Single Load to Page Buffer			Write	X	xx74H	Write	PBA	PD			
Sequential Load to Page Buffer	x8	4,6,10	Write	X	xxE0H	Write	X	BCL	Write	X	BCH
	x16	4,5,6,10	Write	X	xxE0H	Write	X	WCL	Write	X	WCH
Page Buffer Write to Flash	x8	3,4,9,10	Write	X	xx0CH	Write	A_0	BC(L,H)	Write	PA	BC(H,L)
	x16	4,5,10	Write	X	xx0CH	Write	X	WCL	Write	PA	WCH
Two-Byte Write	x8	3	Write	X	xxFBH	Write	A_0	WD(L,H)	Write	PA	WD(H,L)
Lock Block/Confirm			Write	X	xx77H	Write	BA	xxD0H			
Upload Status Bits/Confirm		2	Write	X	xx97H	Write	X	xxD0H			
Upload Device Information			Write	X	xx99H	Write	X	xxD0H			
Erase All Unlocked Blocks/Confirm			Write	X	xxA7H	Write	X	xxD0H			
RY/BY# Enable to Level-Mode		8	Write	X	xx96H	Write	X	xx01H			
RY/BY# Pulse-On-Write		8	Write	X	xx96H	Write	X	xx02H			
RY/BY# Pulse-On-Erase		8	Write	X	xx96H	Write	X	xx03H			
RY/BY# Disable		8	Write	X	xx96H	Write	X	xx04H			
Sleep		11	Write	X	xxF0H						
Abort			Write	X	xx80H						

ADDRESS

BA = Block Address
PBA = Page Buffer Address
RA = Extended Register Address
PA = Program Address
X = Don't Care

DATA

AD = Array Data
PD = Page Buffer Data
BSRD = BSR Data
GSRD = GSR Data

WC (L,H) = Word Count (Low, High)
BC (L,H) = Byte Count (Low, High)
WD (L,H) = Write Data (Low, High)

SEE NEW DESIGN RECOMMENDATIONS

NOTES:

1. RA can be the GSR address or any BSR address. See Figures 4 and 5 for Extended Status Register Memory Maps.
2. Upon device power-up, all BSR lock-bits come up locked. The Upload Status Bits command must be written to reflect the actual lock-bit status.
3. A_0 is automatically complemented to load the second byte of data. BYTE# must be at V_{IL}.
   The A_0 value determines which WD/BC is supplied first: A_0 = 0 looks at the WDL/BCL, A_0 = 1 looks at the WDH/BCH.
4. BCH/WCH must be at 00H for this product because of the 256-byte (128-word) Page Buffer size and to avoid writing the Page Buffer contents to more than one 256-byte segment within an array block. They are simply shown for future Page Buffer expandability.
5. In x16 mode, only the lower byte DQ_{0-7} is used for WCL and WCH. The upper byte DQ_{8-15} is a don't care.
6. PBA and PD (whose count is given in cycles 2 and 3) are supplied starting in the fourth cycle, which is notshown.
7. This command allows the user to swap between available Page Buffers (0 or 1).
8. These commands reconfigure the RY/BY# output to one of two pulse-modes or enable and disable the RY/BY# function.
9. Program address, PA, is the destination address in the flash array which must match the source address in the Page Buffer. Refer to the *16-Mbit Flash Product Family User's Manual*.
10. BCL = 00H corresponds to a byte count of 1. Similarly, WCL = 00H corresponds to a word count of 1.
11. To ensure that the DD28F032SA's power consumption during sleep mode reads the deep power-down current level, the system also needs to de-select the chip by taking either or both CE_0# or CE_1#/CE_2# high.
12. The upper byte of the data bus ($DQ_{8–15}$) during command programs is a "Don't Care" in x16 operation of the device.

5.5 Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

NOTES:

CSR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

RY/BY# output or WSMS bit must be checked to determine completion of an operation (erase suspend, block erase or data program) before the appropriate Status bit (ESS, ES or DWS) is checked for success.

CSR.6 = ERASE-SUSPEND STATUS
1 = Erase Suspended
0 = Erase In Progress/Completed

CSR.5 = ERASE STATUS
1 = Error in Block Erasure
0 = Successful Block Erase

If DWS and ES are set to "1" during a block erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.

CSR.4 = DATA WRITE STATUS
1 = Error in Data Program
0 = Data Program Successful

CSR.3 = V_{PP} STATUS
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP}'s level only after the Data Program or Block Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

CSR.2–0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use; mask them out when polling the CSR.

5.6 Global Status Register

WSMS	OSS	DOS	DSS	QS	PBAS	PBS	PBSS
7	6	5	4	3	2	1	0

GSR.7 = WRITE STATE MACHINE STATUS
- 1 = Ready
- 0 = Busy

GSR.6 = OPERATION SUSPEND STATUS
- 1 = Operation Suspended
- 0 = Operation in Progress/Completed

GSR.5 = DEVICE OPERATION STATUS
- 1 = Operation Unsuccessful
- 0 = Operation Successful or Currently Running

GSR.4 = DEVICE SLEEP STATUS
- 1 = Device in Sleep
- 0 = Device Not in Sleep

MATRIX = 5/4
- 0 0 = Operation Successful or Currently Running
- 0 1 = Device in Sleep Mode or Pending Sleep
- 1 0 = Operation Unsuccessful
- 1 1 = Operation Unsuccessful or Aborted

GSR.3 = QUEUE STATUS
- 1 = Queue Full
- 0 = Queue Available

GSR.2 = PAGE BUFFER AVAILABLE STATUS
- 1 = One or Two Page Buffers Available
- 0 = No Page Buffer Available

GSR.1 = PAGE BUFFER STATUS
- 1 = Selected Page Buffer Ready
- 0 = Selected Page Buffer Busy

GSR.0 = PAGE BUFFER SELECT STATUS
- 1 = Page Buffer 1 Selected
- 0 = Page Buffer 0 Selected

NOTES:

[1] RY/BY# output or WSMS bit must be checked to determine completion of an operation (block lock, erase suspend, any RY/BY# reconfiguration, Upload Status Bits, block erase or data program) before the appropriate Status bit (OSS or DOS) is checked for success.

If operation currently running, then GSR.7 = 0.
If device pending sleep, then GSR.7 = 0.

Operation aborted: unsuccessful due to Abort command.

Each 28F016SA device contains two Page Buffers.

Selected Page Buffer is currently busy with WSM operation

NOTE:

1. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7, or CSR.7, provides indication when all queued operations are completed.

5.7 Block Status Register

BS	BLS	BOS	BOAS	QS	VPPS	R	R
7	6	5	4	3	2	1	0

BSR.7 = BLOCK STATUS
1 = Ready
0 = Busy

BSR.6 = BLOCK LOCK STATUS
1 = Block Unlocked for Program/Erase
0 = Block Locked for Program/Erase

BSR.5 = BLOCK OPERATION STATUS
1 = Operation Unsuccessful
0 = Operation Successful or Currently Running

BSR.4 = BLOCK OPERATION ABORT STATUS
1 = Operation Aborted
0 = Operation Not Aborted

MATRIX 5/4
0 0 = Operation Successful or Currently Running
0 1 = Not a Valid Combination
1 0 = Operation Unsuccessful
1 1 = Operation Aborted

BSR.3 = QUEUE STATUS
1 = Queue Full
0 = Queue Available

BSR.2 = V_{PP} STATUS
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

BSR.1-0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use; mask them out when polling the BSRs.

NOTES:
[1] RY/BY# output or BS bit must be checked to determine completion of an operation (block lock, erase suspend, any RY/BY# reconfiguration, Upload Status Bits, block erase or data program) before the appropriate Status bits (BOS, BLS) is checked for success.

The BOAS bit will not be set until BSR.7 = 1.

Operation halted via Abort command.

NOTE:

1. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7, or CSR.7, provides indication when all queued operations are completed.

6.0 ELECTRICAL SPECIFICATIONS

NOTICE: This is a production datasheet. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

6.1 Absolute Maximum Ratings*

Temperature Under Bias..... 0°C to +80°C

Storage Temperature.....–65°C to +125°C

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

V_{CC} = 3.3V ± 0.3V Systems

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
T_A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V_{CC}	V_{CC} with Respect to GND	2	–0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	2,3	–0.2	14.0	V	
V	Voltage on any Pin (except V_{CC},V_{PP}) with Respect to GND	2	–0.5	V_{CC} + 0.5	V	
I	Current into Any Non-Supply Pin	5		± 30	mA	
I_{OUT}	Output Short Circuit Current	4		100	mA	

V_{CC} = 5.0V ± 0.5V, V_{CC} = 5.0V ± 0.25V Systems(6)

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
T_A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V_{CC}	V_{CC} with Respect to GND	2	–0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	2,3	–0.2	14.0	V	
V	Voltage on Any Pin (except V_{CC},V_{PP}) with Respect to GND	2	–2.0	7.0	V	
I	Current into Any Non-Supply Pin	5		± 30	mA	
I_{OUT}	Output Short Circuit Current	4		100	mA	

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is –0.5V on input/output pins. During transitions, this level may undershoot to–2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods <20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. This specification also applies to pins marked "NC."
6. 5% V_{CC} specifications refer to the DD28F032SA-070 in its High Speed Test configuration.

SEE NEW DESIGN RECOMMENDATIONS

6.2 Capacitance

For a 3.3V System:

Symbol	Parameter	Notes	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	12	16	pF	T_A = +25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	16	24	pF	T_A = +25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1		50	pF	For V_{CC} = 3.3V ± 0.3V
	Equivalent Load Timing Circuit			2.5	ns	50Ω Transmission Line Delay

For a 5.0V System:

Symbol	Parameter	Notes	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	12	16	pF	T_A = +25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	16	24	pF	T_A = +25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1		100	pF	For V_{CC} = 5.0V ± 0.5V
				30	pF	For V_{CC} = 5.0V ± 0.25V
	Equivalent Testing Load Circuit for V_{CC} ± 10%			2.5	ns	25Ω Transmission Line Delay
	Equivalent Testing Load Circuit for V_{CC} ± 5%			2.5	ns	83Ω Transmission Line Delay

NOTE:

1. Sampled, not 100% tested.

6.3 Timing Nomenclature

All 3.3V system timings are measured from where signals cross 1.5V.

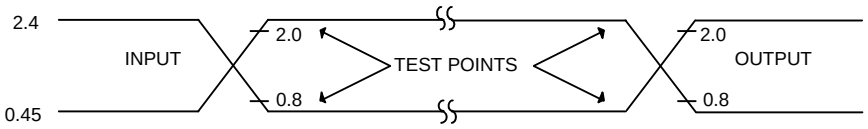
For 5.0V systems use the standard JEDEC cross point definitions.

Each timing parameter consists of 5 characters. Some common examples are defined below:

- t_{CE} t_{ELQV} time(t) from CE_X# (E) going low (L) to the outputs (Q) becoming valid (V)
- t_{OE} t_{GLQV} time(t) from OE # (G) going low (L) to the outputs (Q) becoming valid (V)
- t_{ACC} t_{AVQV} time(t) from address (A) valid (V) to the outputs (Q) becoming valid (V)
- t_{AS} t_{AVWH} time(t) from address (A) valid (V) to WE# (W) going high (H)
- t_{DH} t_{WHDX} time(t) from WE# (W) going high (H) to when the data (D) can become undefined (X)

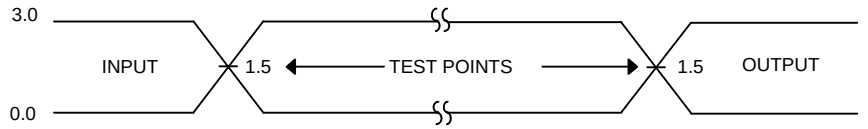
	Pin Characters		Pin States
A	Address Inputs	H	High
D	Data Inputs	L	Low
Q	Data Outputs	V	Valid
E	CE_X# (Chip Enable)	X	Driven, but not necessarily valid
F	BYTE# (Byte Enable)	Z	High Impedance
G	OE# (Output Enable)		
W	WE# (Write Enable)		
P	RP# (Deep Power-Down Pin)		
R	RY/BY# (Ready Busy)		
V	Any Voltage Level		
Y	3/5# Pin		
5V	V_{CC} at 4.5V Minimum		
3V	V_{CC} at 3.0V Minimum		

SEE NEW DESIGN RECOMMENDATIONS



AC test inputs are driven at V_{OH} (2.4 VTTL) for a Logic "1" and V_{OL} (0.45 VTTL) for a Logic "0." Input timing begins at V_{IH} (2.0 VTTL) and V_{IL} (0.8 VTTL). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.

Figure 6. Transient Input/Output Reference Waveform (V_{CC} = 5.0V) for Standard Test Configuration(1)



AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

Figure 7. Transient Input/Output Reference Waveform (V_{CC} = 3.3V) and High Speed Reference Waveform (2) (V_{CC} = 5.0V ± 5%)

NOTES:

1. Testing characteristics for DD28F032SA-080/DD28F032SA-100.
2. Testing characteristics for DD28F032SA-070/DD28F032SA-150.

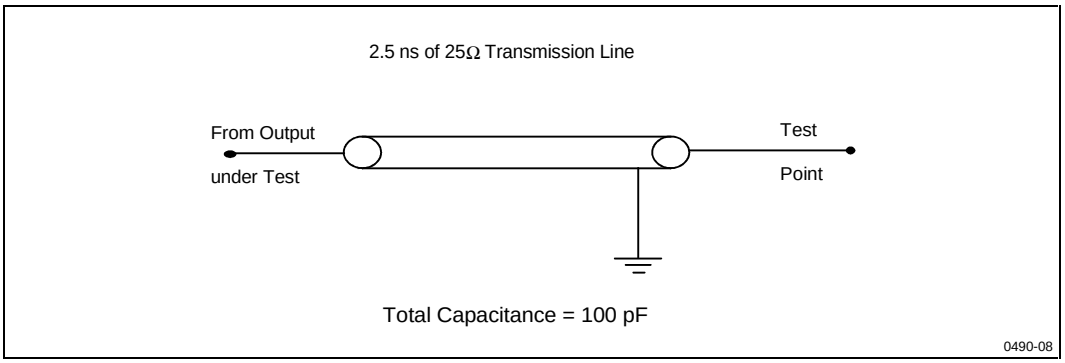


Figure 8. Transient Equivalent Testing Load Circuit (V_{CC} = 5.0V ± 10%)

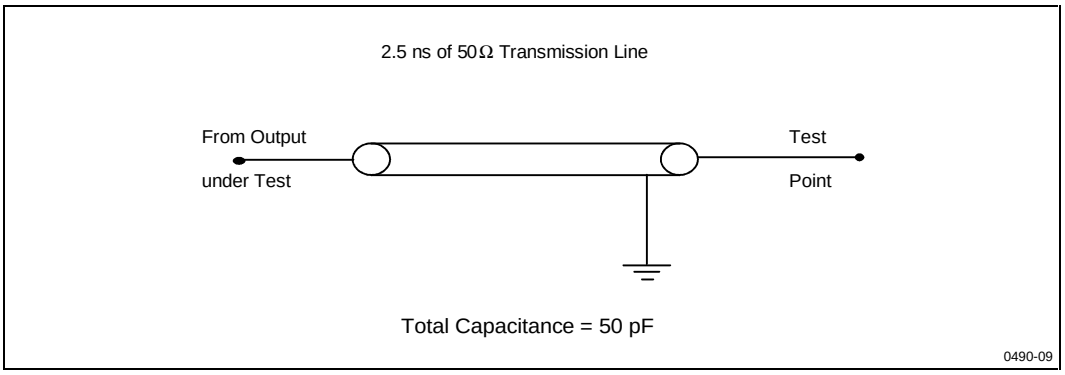


Figure 9. Transient Equivalent Testing Load Circuit (V_{CC} = 3.3V ± 0.3V)

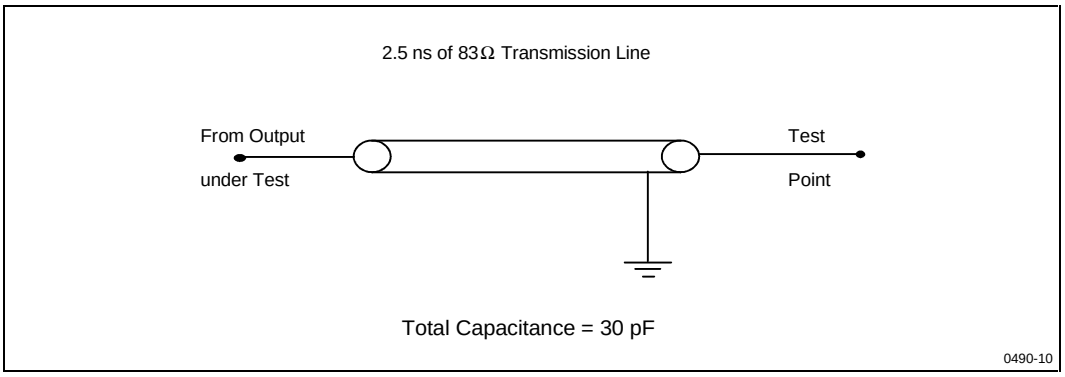


Figure 10. High Speed Transient Equivalent Testing Load Circuit (V_{CC} = 5.0V ± 5%)

SEE NEW DESIGN RECOMMENDATIONS

6.4 DC Characteristics

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# = Pin Set High for 3.3V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Load Current	1			± 2	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1			± 20	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,5,6,8		100	200	µA	$V_{CC} = V_{CC}$ Max CE_0#, CE_X#, RP#, = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
				2	8	mA	V_{CC}= V_{CC} Max CE_0#, CE_X#, RP# = V_{IH} BYTE#, WP#, 3/5# = V_{IH} or V_{IL}
I_{CCD}	V_{CC} Deep Power-Down Current	1		2	10	µA	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCR}1	V_{CC} Read Current	1,4,5,6		25	30	mA	$V_{CC} = V_{CC}$ Max CMOS: CE_0#, CE_X# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V f = 6.67 MHz, I_{OUT} = 0 mA
				26	34	mA	TTL: CE_0#, CE_X# = V_{IL}, BYTE# = V_{IL} or V_{IH}, Inputs = V_{IL} or V_{IH} f = 6.67 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Program Current for Word or Byte	1,7		8	12	mA	Program in Progress
I_{CCE}	V_{CC} Block Erase Current	1,7		6	12	mA	Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2,6,7		3	6	mA	CE_0#, CE_X# = V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby/ Read Current	1		± 2	± 20	µA	$V_{PP} \leq V_{CC}$
I_{PPR}				130	400	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.4	10	µA	RP# = GND ± 0.2V

6.4 DC Characteristics (Continued)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# Pin Set High for 3.3V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{PPW}	V_{PP} Program Current for Word or Byte	1		10	15	mA	$V_{PP} = V_{PPH}$ Program in Progress
I_{PPE}	V_{PP} Block Erase Current	1		4	10	mA	$V_{PP} = V_{PPH}$ Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		130	400	µA	$V_{PP} = V_{PPH}$ Block Erase Suspended
V_{IL}	Input Low Voltage		–0.3		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} ± 0.3	V	
V_{OL}	Output Low Voltage				0.4	V	$V_{CC} = V_{CC}$ Min I_{OL} = 4 mA
$V_{OH}1$	Output High Voltage		2.4			V	$V_{CC} = V_{CC}$ Min I_{OH} = –2.0 mA
$V_{OH}2$			V_{CC} – 0.2				$V_{CC} = V_{CC}$ Min I_{OH} = –100 µA
V_{PPL}	V_{PP} during Normal Operations	3	0.0		6.5	V	
V_{PPH}	V_{PP} during Program/Erase Operations		11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Program/Erase Lock Voltage		2.0			V	

NOTES:

1. All current are in RMS unless otherwise noted. Typical values at V_{CC} = 3.3V, V_{PP} = 12.0V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases, word/byte programs and lock block operations are inhibited when $V_{PP} = V_{PPL}$ and not guaranteed in the range between V_{PPH} and V_{PPL}.
4. Automatic Power Savings (APS) reduces I_{CCR} to <1 mA in static operation.
5. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.
6. CE_X# = CE_1# or CE_2#.
7. If operating with TTL levels, add 4 mA of V_{CC} Standby Current to max $I_{CCR}1$, $I_{CCR}2$, I_{CCW}, I_{CCE} and I_{CCES}.
8. Standby current levels are not reached when putting the chip in standby mode immediately after reading the page buffer. Default the device into read array or read Status Register mode before entering standby to ensure standby current levels.

SEE NEW DESIGN RECOMMENDATIONS

6.5 DC Characteristics

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C
3/5# Pin Set Low for 5.0V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Load Current	1			± 2	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1			± 20	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,5,6,8		100	200	µA	$V_{CC} = V_{CC}$ Max CE_0#, CE_X#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
				4	8	mA	$V_{CC} = V_{CC}$ Max CE_0#, CE_X#, RP# = V_{IH} BYTE#, WP#, 3/5# = V_{IH} or V_{IL}
I_{CCD}	V_{CC} Deep Power-Down Current	1		4	25	µA	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V
$I_{CCR}1$	V_{CC} Read Current	1,4,5, 6,7		50	60	mA	$V_{CC} = V_{CC}$ Max CMOS: CE_0#, CE_X# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V f = 10 MHz, I_{OUT} = 0 mA
				52	64	mA	TTL: CE_0#, CE_X# = V_{IL}, BYTE# = V_{IL} or V_{IH}, Inputs = V_{IL} or V_{IH} f = 10 MHz, I_{OUT} = 0 mA
$I_{CCR}2$	V_{CC} Read Current	1,4,5, 6,7		30	35	mA	$V_{CC} = V_{CC}$ Max CMOS: CE_0#, CE_X# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V Inputs = GND ± 0.2V or V_{CC} ± 0.2V f = 5 MHz, I_{OUT} = 0 mA
				32	39	mA	TTL: CE_0#, CE_X# = V_{IL}, BYTE# = V_{IL} or V_{IH}, Inputs = V_{IL} or V_{IH} f = 5 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Prog. Current for Word or Byte	1,7		25	35	mA	Program in Progress

6.5 DC Characteristics (Continued)

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C
3/5# Pin Set Low for 5.0V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{CCE}	V_{CC} Block Erase Current	1,7		18	25	mA	Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2,6,7		5	10	mA	CE_0#, CE_X# = V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby/ Read Current	1		± 2	± 20	µA	$V_{PP} \le V_{CC}$
I_{PPR}				130	400	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.4	10	µA	RP# = GND ± 0.2V
I_{PPW}	V_{PP} Prog. Current for Word or Byte	1		7	12	mA	V_{PP} = V_{PPH} Program in Progress
I_{PPE}	V_{PP} Block Erase Current	1		5	10	mA	V_{PP} = V_{PPH} Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		130	400	µA	V_{PP} = V_{PPH} Block Erase Suspended
V_{IL}	Input Low Voltage		–0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	V_{CC} = V_{CC} Min, I_{OL} = 5.8 mA
$V_{OH}1$	Output High Voltage		0.85 V_{CC}			V	V_{CC} = V_{CC} Min, I_{OH} = –2.5 mA
$V_{OH}2$			V_{CC} – 0.4				V_{CC} = V_{CC} Min, I_{OH} = –100 µA
V_{PPL}	V_{PP} during Normal Operations	3	0.0		6.5	V	
V_{PPH}	V_{PP} during Prog. Erase Operations		11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Program/Erase Lock Voltage		2.0			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = +25°C. These currents are valid for all product versions (package and speeds).
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases, word/byte programs and lock block operations are inhibited when V_{PP} = V_{PPL} and not guaranteed in the range between V_{PPH} and V_{PPL}.
4. Automatic Power Saving (APS) reduces I_{CCR} to <2 mA in static operation.
5. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.
6. CE_X#= CE_1# or CE_2#.
7. If operating with TTL levels, add 4 mA of V_{CC} standby current. to max $I_{CCR}1$, $I_{CCR}2$, I_{CCW}, I_{CCE} and I_{CCES}.
8. Standby current levels are not reached when putting the chip in standby mode immediately after reading the page buffer. Default the device into read array or read Status Register mode before entering standby to ensure standby current levels.

SEE NEW DESIGN RECOMMENDATIONS

6.6 AC Characteristics—Read Only Operations(1)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Versions (5)			DD28F032SA-150		
Symbol	**Parameter**	**Notes**	**Min**	**Max**	**Units**
t_{AVAV}	Read Cycle Time		150		ns
t_{AVQV}	Address to Output Delay			150	ns
t_{ELQV}	CE_X# to Output Delay	2		150	ns
t_{PHQV}	RP# High to Output Delay			750	ns
t_{GLQV}	OE# to Output Delay	2		50	ns
t_{ELQX}	CE_X# to Output in Low Z	3	0		ns
t_{EHQZ}	CE_X# to Output in High Z	3		35	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# to Output in High Z	3		20	ns
t_{OH}	Output Hold from Address, CE_X# or OE# Change, Whichever Occurs First	3	0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		150	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		40	ns
t_{ELFL} t_{ELFH}	CE_X# Low to BYTE# High or Low	3		5	ns

For Extended Status Register Reads

t_{AVEL}	Address Setup to CE_X# Going Low	3,4	0		ns
t_{AVGL}	Address Setup to OE# Going Low	3,4	0		ns

6.6 AC Characteristics—Read Only Operations[1] (Continued)

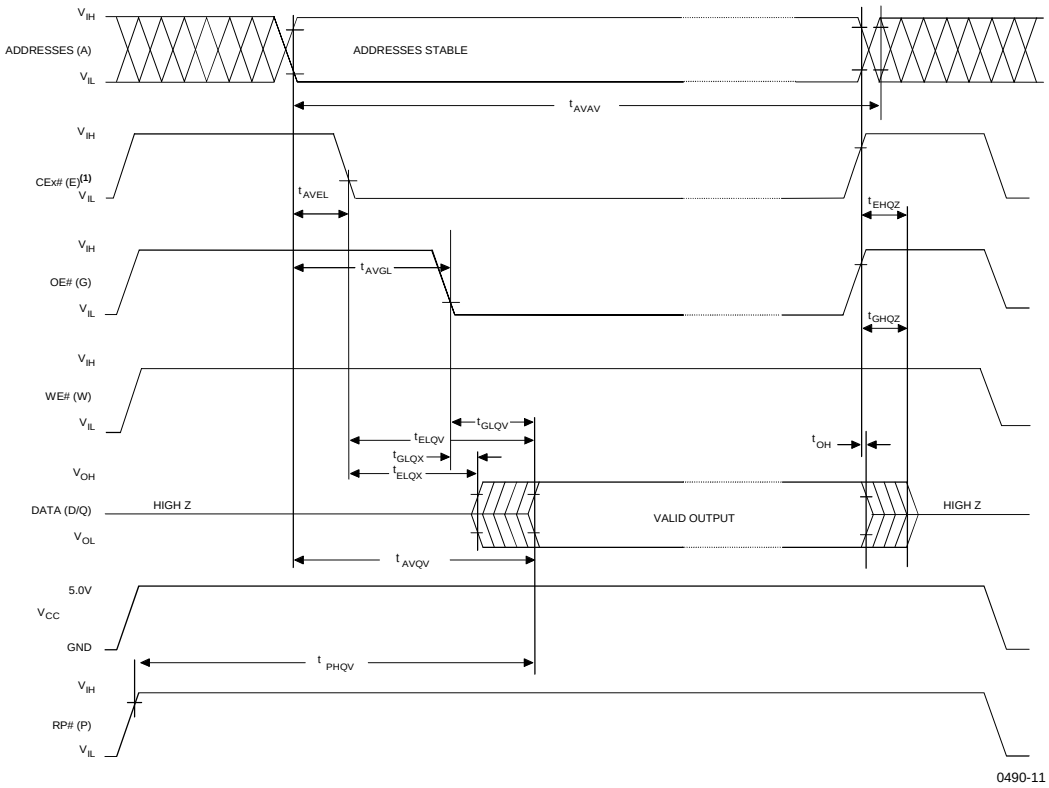
V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C

Versions[5]		V_{CC} ± 5%	DD28F032SA-070[6]						Units
		V_{CC} ± 10%			DD28F032SA-080[7]		DD28F032SA-100[7]		
Sym	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{AVAV}	Read Cycle Time		70		80		100		ns
t_{AVQV}	Address to Output Delay			70		80		100	ns
t_{ELQV}	CE_X# to Output Delay	2		70		80		100	ns
t_{PHQV}	RP# to Output Delay			400		480		550	ns
t_{GLQV}	OE# to Output Delay	2		30		35		40	ns
t_{ELQX}	CE_X# to Output in Low Z	3	0		0		0		ns
t_{EHQZ}	CE_X# to Output in High Z	3		25		30		30	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		0		ns
t_{GHQZ}	OE# to Output in High Z	3		25		15		15	ns
t_{OH}	Output Hold from Address, CE_X# or OE# Change, Whichever Occurs First	3	0		0		0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		70		80		100	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		25		30		30	ns
t_{ELFL} t_{ELFH}	CE_X# Low to BYTE# High or Low	3		5		5		5	ns
For Extended Status Register Reads									
t_{AVEL}	Address Setup to CE_X# Going Low	3,4	0		0		0		ns
t_{AVGL}	Address Setup to OE# Going Low	3,4	0		0		0		ns

SEE NEW DESIGN RECOMMENDATIONS

NOTES:

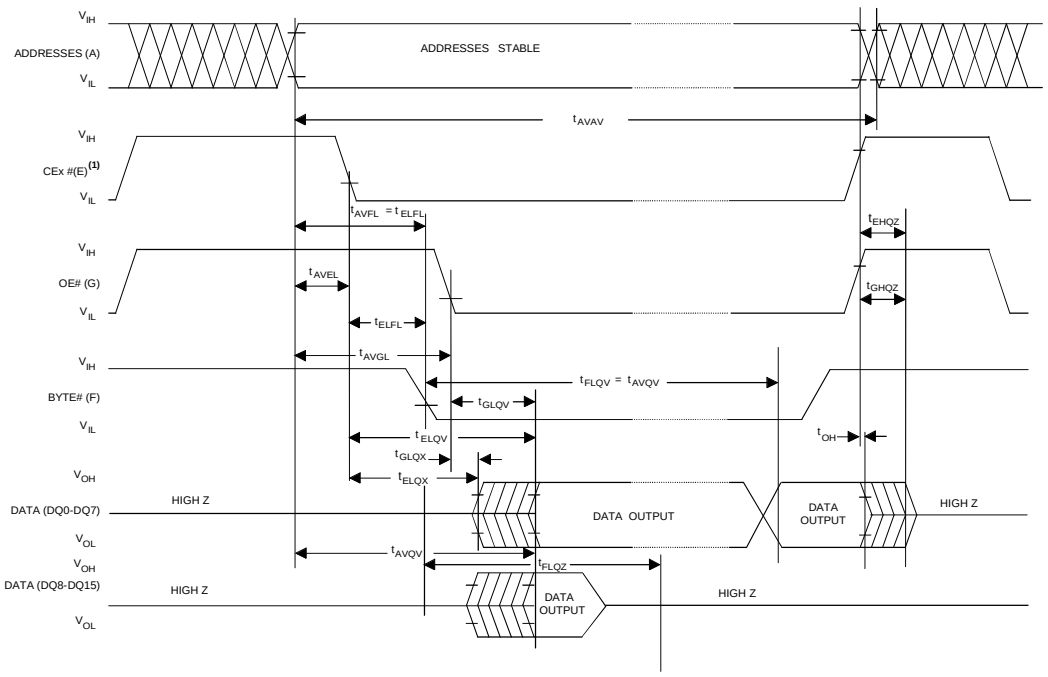
1. See AC Input/Output Reference Waveforms for timing measurements, Figures 6 and 7.
2. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CE_X# without impact in t_{ELQV}.
3. Sampled, not 100% tested.
4. This timing parameter is used to latch the correct BSR data onto the outputs.
5. Device speeds are defined as:
   70/80 ns at V_{CC} = 5.0V equivalent to
   150 ns at V_{CC} = 3.3V
   100 ns at V_{CC} = 5.0V equivalent to
   150 ns at V_{CC} = V_{CC} = 3.3V
6. See AC Input/Output Reverence Waveforms and AC Testing Load Circuits for High Speed Test Configuration.
7. See Standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.



NOTES:

For 28F016SA No. 1: CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
For 28F016SA No. 2: CE_X# is defined as the latter of CE_0# or CE_2# going low, or the first of CE_0# or CE_2# going high.

Figure 11. Read Timing Waveforms



NOTES:

For 28F016SA No. 1: CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
For 28F016SA No. 2: CE_X# is defined as the latter of CE_0# or CE_2# going low, or the first of CE_0# or CE_2# going high.

Figure 12. BYTE# Timing Waveforms

SEE NEW DESIGN RECOMMENDATIONS

6.7 Power-Up and Reset Timings

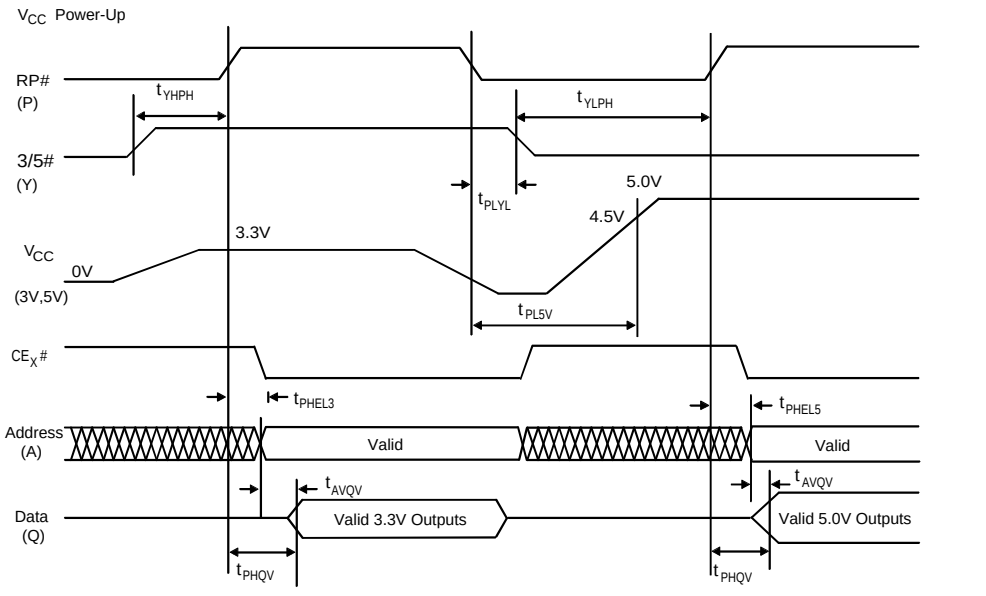


Figure 13. V_{CC} Power-Up and RP# Reset Waveforms

Symbol	Parameter	Notes	Min	Max	Units
t_{PLYL} t_{PLYH}	RP# Low to 3/5# Low (High)		0		µs
t_{YLPH} t_{YHPH}	3/5# Low (High) to RP# High	1	2		µs
t_{PL5V} t_{PL3V}	RP# Low to V_{CC} at 4.5V Minimum (to V_{CC} at 3.0V min or 3.6V max)	2	0		µs
t_{PHEL3}	RP# High to CE# Low (3.3V V_{CC})	1	500		
t_{PHEL5}	RP# High to CE# Low (5V V_{CC})	1	330		
t_{AVQV}	Address Valid to Data Valid for V_{CC} = 5.0V ± 10%	3		80	ns
t_{PHQV}	RP# High to Data Valid for V_{CC} = 5.0V ± 10%	3		480	ns

NOTES:

CE_0#, CE_X# and OE# are switched low after Power-Up.

1. The t_{YLPH}/t_{YHPH} and t_{PHEL3}/t_{PHEL5} times must be strictly followed to guarantee all other read and program specifications.
2. The power supply may start to switch concurrently with RP# going low.
3. The address access time and RP# high to data valid time are shown for the DD28F032SA-80 and 5.0V V_{CC} operation. Refer to the AC Characteristics-Read Only Operations for 3.3V V_{CC} operation and all other speed options.

6.8 AC Characteristics for WE#—Controlled Command Write Operations(1)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Versions			DD28F032SA-150			
Symbol	**Parameter**	**Notes**	**Min**	**Typ**	**Max**	**Unit**
t_{AVAV}	Write Cycle Time		150			ns
t_{VPWH}	V_{PP} Setup to WE# Going High	3	100			ns
t_{PHEL}	RP# Setup to CE_X# Going Low		480			ns
t_{ELWL}	CE_X# Setup to WE# Going Low		10			ns
t_{AVWH}	Address Setup to WE# Going High	2,6	75			ns
t_{DVWH}	Data Setup to WE# Going High	2,6	85			ns
t_{WLWH}	WE# Pulse Width		75			ns
t_{WHDX}	Data Hold from WE# High	2	10			ns
t_{WHAX}	Address Hold from WE# High	2	10			ns
t_{WHEH}	CE_X# Hold from WE# High		10			ns
t_{WHWL}	WE# Pulse Width High		75			ns
t_{GHWL}	Read Recovery before Write		0			ns
t_{WHRL}	WE# High to RY/BY# Going Low				100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			ns
t_{PHWL}	RP# High Recovery to WE# Going Low		1			µs
t_{WHGL}	Write Recovery before Read		120			ns
t_{QVVL}	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			µs
$t_{WHQV}1$	Duration of Word/Byte Program Operation	4,5	5	9	Note 7	µs
$t_{WHQV}2$	Duration of Block Erase Operation	4	0.3		10	sec

SEE NEW DESIGN RECOMMENDATIONS

6.8 AC Characteristics for WE#—Controlled Command Write Operations(1)

(Continued)

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C

Versions		V_{CC} ± 5%	DD28F032SA-070									Unit
		V_{CC} ± 10%				DD28F032SA-080			DD28F032SA-100			
Sym	Parameter	Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AVAV}	Write Cycle Time		70			80			100			ns
t_{VPWH}	V_{PP} Setup to WE# Going High	3	100			100			100			ns
t_{PHEL}	RP# Setup to CE_X# Going Low		480			480			480			ns
t_{ELWL}	CE_X# Setup to WE# Going Low		0			0			0			ns
t_{AVWH}	Address Setup to WE# Going High	2,6	50			50			50			ns
t_{DVWH}	Data Setup to WE# Going High	2,6	60			60			60			ns
t_{WLWH}	WE# Pulse Width		40			50			50			ns
t_{WHDX}	Data Hold from WE# High	2	0			0			0			ns
t_{WHAX}	Address Hold from WE# High	2	10			10			10			ns
t_{WHEH}	CE_X# Hold from WE# High		10			10			10			ns
t_{WHWL}	WE# Pulse Width High		30			30			50			ns
t_{GHWL}	Read Recovery before Write		0			0			0			ns
t_{WHRL}	WE# High to RY/BY# Going Low				100			100			100	ns

6.8 AC Characteristics for WE#—Controlled Command Write Operations(1)

(Continued)

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C

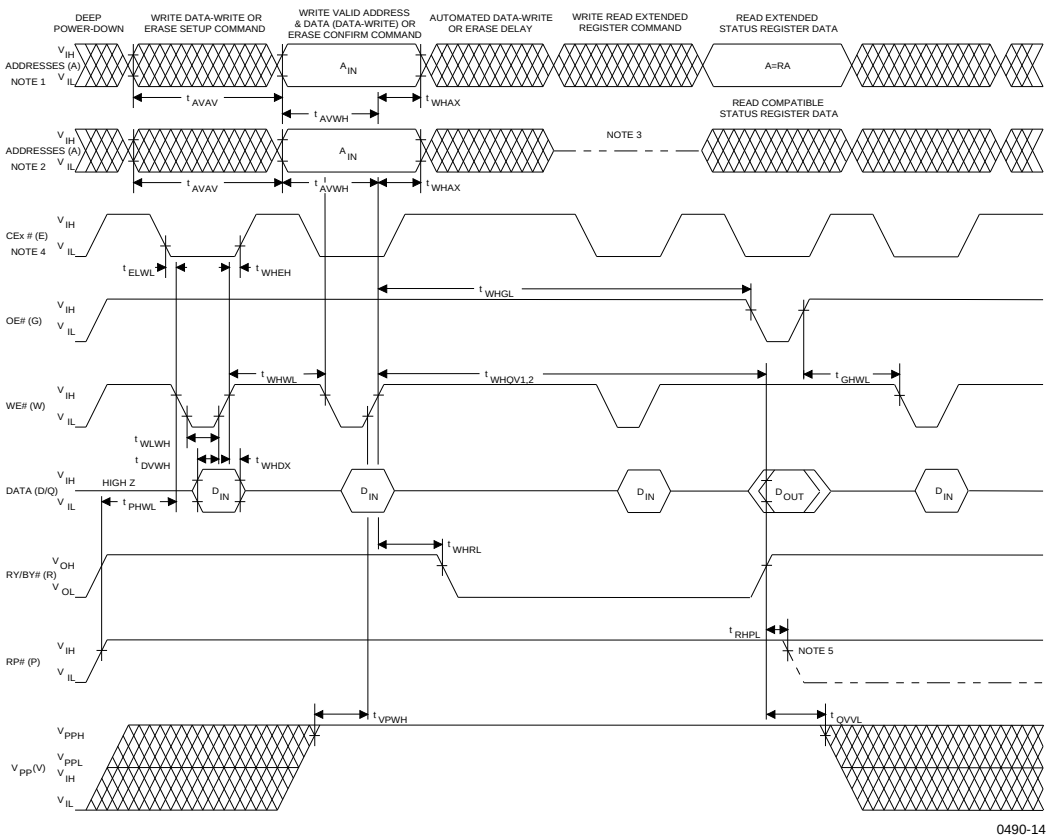
Versions		V_{CC} ± 5%	DD28F032SA-070									Unit
		V_{CC} ± 10%				DD28F032SA-080			DD28F032SA-100			
Sym	**Parameter**	**Notes**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			0			ns
t_{PHWL}	RP# High Recovery to WE# Going Low		1			1			1			µs
t_{WHGL}	Write Recovery before Read		60			65			65			ns
t_{QVVL}	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			0			0			µs
$t_{WHQV}1$	Duration of Word/Byte Program Operation	4,5	4.5	6	Note 7	4.5	6	Note 7	4.5	6	Note 7	µs
$t_{WHQV}2$	Duration of Block Erase Operation	4	0.3		10	0.3		10	0.3		10	sec

NOTES:

For 28F016SA No. 1: CE_X# is defined as the latter of CE_0# or CE_1# going low or the first of CE_0# or CE_1# going high.
For 28F016SA No. 2: CE_X# is defined as the latter of CE_0# or CE_2# going low or the first of CE_0# or CE_2# going high.

1. Read timings during data program and block erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested
4. Data program/block erase durations are measured to valid Status Register data.
5. Word/byte program operations are typically performed with 1 programming pulse.
6. Address and data are latched on the rising edge of WE# for all command write operations.
7. This information will be available in a technical paper. Please call Intel's Applications Hotline or your local sales office for more information.

SEE NEW DESIGN RECOMMENDATIONS



NOTES:

1. This address string depicts data program/block erase cycles with corresponding verification via ESRD.
2. This address string depicts data program/block erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during data program/block erase operations.
4. For 28F016SA No. 1: CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
   For 28F016SA No. 2: CE_X# is defined as the latter of CE_0# or CE_2# going low, or the first of CE_0# or CE_2# going high
5. RP# low transition is only to show t_{RHPL}; not valid for above Read and Program cycles.

Figure 14. AC Waveforms for Command Write Operations

6.9 AC Characteristics for CE_X#—Controlled Command Write Operations(1)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Versions			DD28F032SA-150			
Symbol	**Parameter**	**Notes**	**Min**	**Typ**	**Max**	**Unit**
t_{AVAV}	Write Cycle Time		150			ns
t_{VPEH}	V_{PP} Setup to CE_X# Going High	3	100			ns
t_{PHWL}	RP# Setup to WE# Going Low		480			ns
t_{WLEL}	WE# Setup to CE_X# Going Low		0			ns
t_{AVEH}	Address Setup to CE_X# Going High	2,6	75			ns
t_{DVEH}	Data Setup to CE_X# Going High	2,6	85			ns
t_{ELEH}	CE_X# Pulse Width		75			ns
t_{EHDX}	Data Hold from CE_X# High	2	10			ns
t_{EHAX}	Address Hold from CE_X# High	2	10			ns
t_{EHWH}	WE# Hold from CE_X# High		10			ns
t_{EHEL}	CE_X# Pulse Width High		75			ns
t_{GHEL}	Read Recovery before Write		0			ns
t_{EHRL}	CE_X# High to RY/BY# Going Low				100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			ns
t_{PHEL}	RP# High Recovery to CE_X# Going Low		1			µs
t_{EHGL}	Write Recovery before Read		120			ns
t_{QVVL}	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			µs
$t_{EHQV}1$	Duration of Word/Byte Program Operation	4,5	5	9	Note 7	µs
$t_{EHQV}2$	Duration of Block Erase Operation	4	0.3		10	sec

SEE NEW DESIGN RECOMMENDATIONS

6.9 AC Characteristics for CE_X#—Controlled Command Write Operations(1)

(Continued)

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C

Versions		V_{CC} ± 5%	DD28F032SA-070									Unit
		V_{CC} ± 10%				DD28F032SA-080			DD28F032SA-100			
Sym	Parameter	Notes	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AVAV}	Write Cycle Time		70			80			100			ns
t_{VPEH}	V_{PP} Setup to CE_X# Going High	3	100			100			100			ns
t_{PHWL}	RP# Setup to WE# Going Low	3	480			480			480			ns
t_{WLEL}	WE# Setup to CE_X# Going Low		0			0			0			ns
t_{AVEH}	Address Setup to CE_X# Going High	2,6	50			50			50			ns
t_{DVEH}	Data Setup to CE_X# Going High	2,6	60			60			60			ns
t_{ELEH}	CE_X# Pulse Width		40			50			50			ns
t_{EHDX}	Data Hold from CEX# High	2	0			0			0			ns
t_{EHAX}	Address Hold from CE_X# High	2	10			10			10			ns
t_{EHWH}	WE# Hold from CE_X# High		10			10			10			ns
t_{EHEL}	CE_X# Pulse Width High		30			30			50			ns
t_{GHEL}	Read Recovery before Write		0			0			0			ns
t_{EHRL}	CE_X# High to RY/BY# Going Low				100			100			100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			0			ns

6.9 AC Characteristics for CE_X#—Controlled Command Write Operations(1)

(Continued)

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C

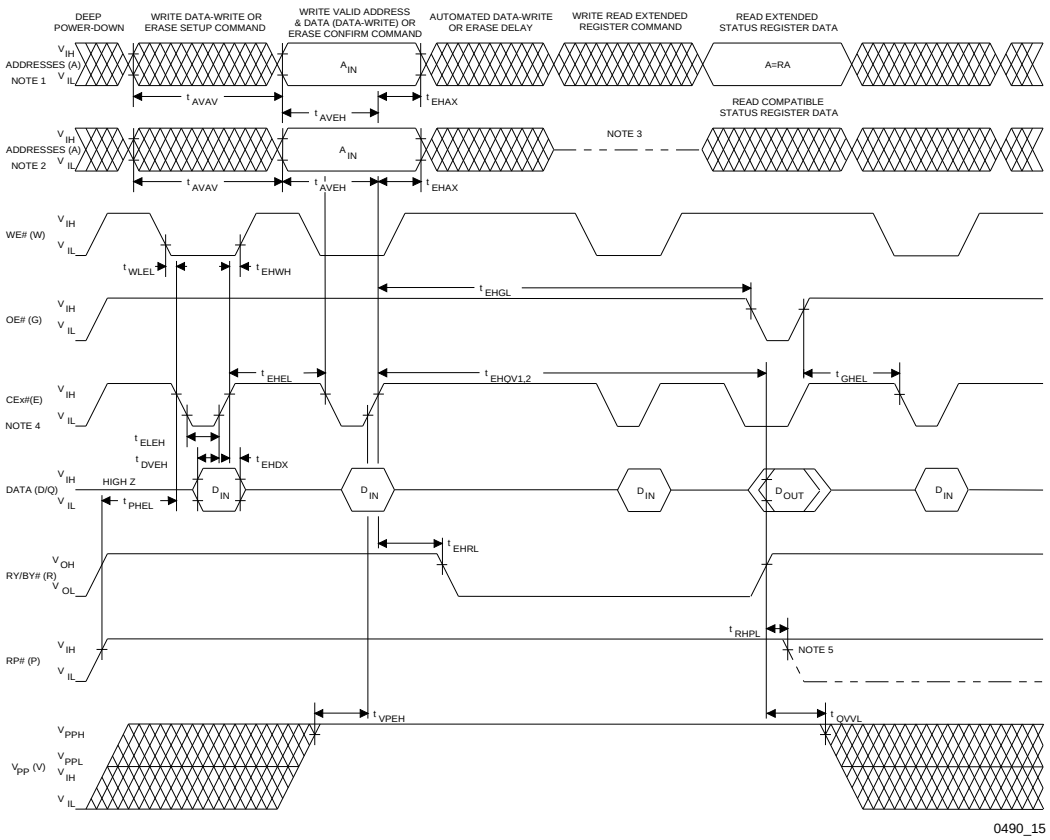
Versions		V_{CC} ± 5%	DD28F032SA-070									Unit
		V_{CC} ± 10%				DD28F032SA-080			DD28F032SA-100			
Sym	**Parameter**	**Notes**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
t_{PHEL}	RP# High Recovery to CE_X# Going Low		1			1			1			µs
t_{EHGL}	Write Recovery before Read		60			65			80			ns
t_{QVVL}	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data at RY/BY# High		0			0			0			µs
$t_{EHQV}1$	Duration of Word/Byte Program Operation	4,5	4.5	6	Note 7	4.5	6	Note 7	4.5	6	Note 7	µs
$t_{EHQV}2$	Duration of Block Erase Operation	4	0.3		10	0.3		10	0.3		10	sec

NOTES:

For 28F016SA No. 1: CE_X# is defined as the latter of CE_0# or CE_1# going low or the first of CE_0# or CE_1# going high.
For 28F016SA No. 2: CE_X# is defined as the latter of CE_0# or CE_2# going low or the first of CE_0# or CE_2# going high.

1. Read timings during data program and block erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Data program/block erase durations are measured to valid Status Register data.
5. Word/byte program operations are typically performed with 1 programming pulse.
6. Address and data are latched on the rising edge of CE_X# for all command write operations.
7. This information will be available in a technical paper. Please call Intel's Applications Hotline or your local sales office for more information.

SEE NEW DESIGN RECOMMENDATIONS



NOTES:

1. This address string depicts data program/block erase cycles with corresponding verification via ESRD.
2. This address string depicts data program/block erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during data program/block erase operations.
4. For 28F016SA No. 1:CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
   For 28F016SA No. 2: CE_X# is defined as the latter of CE_0# or CE_2# going low, or the first of CE_0# or CE_2# going high.
5. RP# low transition is only to show t_{RHPL}; not valid for above Read and Write cycles.

Figure 15. Alternate AC Waveforms for Command Write Operations

6.10 AC Characteristics for Page Buffer Write Operations(1)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Versions			DD28F032SA-150			
Symbol	**Parameter**	**Notes**	**Min**	**Typ**	**Max**	**Unit**
t_{AVAV}	Write Cycle Time		150			ns
t_{ELWL}	CE_X# Setup to WE# Going Low		10			ns
t_{AVWL}	Address Setup to WE# Going Low	3	0			ns
t_{DVWH}	Data Setup to WE# Going High	2	75			ns
t_{WLWH}	WE# Pulse Width		75			ns
t_{WHDX}	Data Hold from WE# High	2	10			ns
t_{WHAX}	Address Hold from WE# High	2	10			ns
t_{WHEH}	CE_X# Hold from WE# High		10			ns
t_{WHWL}	WE# Pulse Width High		75			ns
t_{GHWL}	Read Recovery before Write		0			ns
t_{WHGL}	Write Recovery before Read		120			ns

SEE NEW DESIGN RECOMMENDATIONS

6.10 AC Characteristics for Page Buffer Write Operations[1] (Continued)

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_A = 0°C to +70°C

Versions			DD28F032SA-070			DD28F032SA-080			DD28F032SA-100			
Symbol	**Parameter**	**Notes**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
t_{AVAV}	Write Cycle Time		70			80			100			ns
t_{ELWL}	CE_X# Setup to WE# Going Low		0			0			0			ns
t_{AVWL}	Address Setup to WE# Going Low	3	0			0			0			ns
t_{DVWH}	Data Setup to WE# Going High	2	50			50			50			ns
t_{WLWH}	WE# Pulse Width		40			50			50			ns
t_{WHDX}	Data Hold from WE# High	2	0			0			0			ns
t_{WHAX}	Address Hold from WE# High	2	10			10			10			ns
t_{WHEH}	CE_X# Hold from WE# High		10			10			10			ns
t_{WHWL}	WE# Pulse Width High		30			30			50			ns
t_{GHWL}	Read Recovery before Write		0			0			0			ns
t_{WHGL}	Write Recovery before Read		60			65			80			ns

NOTES:

For 28F016SA No. 1: CE_X # is defined as the latter of CE_0# or CE_1# going low or the first of CE_0# or CE_1# going high.
For 28F016SA No. 2: CE_X # is defined as the latter of CE_0# or CE_2# going low or the first of CE_0# or CE_2# going high.

1. These are WE#-controlled write timings, equivalent CE_X#-controlled write timings apply.
2. Sampled, not 100% tested.
3. Address must be valid during the entire WE# low pulse or the entire CE_X # low pulse (for CE_X #-controlled write timings).

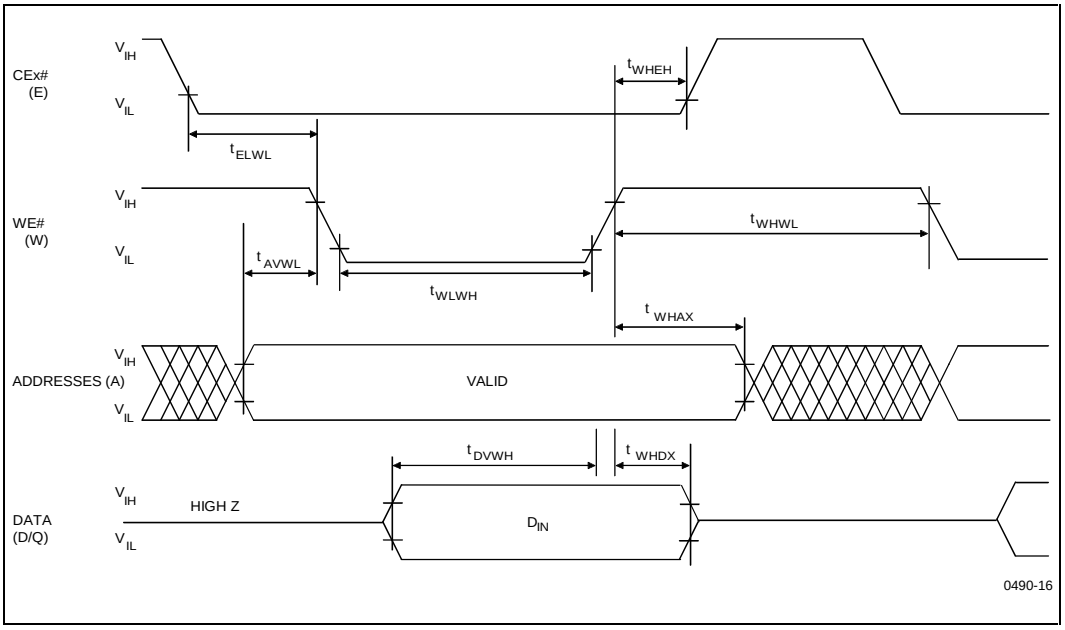


Figure 16. Page Buffer Write Timing Waveforms (Loading Data to the Page Buffer)

SEE NEW DESIGN RECOMMENDATIONS

6.11 Erase and Word/Byte Write Performance, Cycling Performance and Suspend Latency(3)

V_{CC} = 3.3V ± 0.3V, V_{PP} = 12.0V ± 0.6V, T_A = 0°C to +70°C

Sym	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
	Page Buffer Byte Write Time	2,4		3.26	Note 6	µs	
	Page Buffer Word Write Time	2,4		6.53	Note 6	µs	
$t_{WHRH}1$	Word/Byte Program Time	2		9	Note 6	µs	
$t_{WHRH}2$	Block Program Time	2		0.6	2.1	sec	Byte Program
$t_{WHRH}3$	Block Program Time	2		0.3	1.0	sec	Word Program
	Block Erase Time	2		0.8	10	sec	
	Full Chip Erase Time	2		51.2		sec	
	Erase Suspend Latency Time to Read			7.0		µs	
	Auto Erase Suspend Latency Time to Program			10.0		µs	
	Erase Cycles	5	100,000	1,000,000		Cycles	

V_{CC} = 5.0V ± 0.5V, V_{PP} = 12.0V ± 0.6V, T_A = 0°C to +70°C

Sym	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
	Page Buffer Byte Write Time	2,4		2.76	Note 6	µs	
	Page Buffer Word Write Time	2,4		5.51	Note 6	µs	
$t_{WHRH}1$	Word/Byte Program Time	2		6	Note 6	µs	
$t_{WHRH}2$	Block Program Time	2		0.4	2.1	sec	Byte Program
$t_{WHRH}3$	Block Program Time	2		0.2	1.0	sec	Word Program
	Block Erase Time	2		0.6	10	sec	
	Full Chip Erase Time	2		38.4		sec	
	Erase Suspend Latency Time to Read			5.0		µs	
	Auto Erase Suspend Latency Time to Program			8.0		µs	
	Erase Cycles	5	100,000	1,000,000		Cycles	

NOTES:

1. +25°C, V_{CC} = 3.3V or 5.0V nominal, V_{PP} = 12.0V nominal, 10K cycles.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. This assumes using the full Page Buffer to program to the flash memory (256 bytes or 128 words).
5. 1,000,000 cycle performance assumes the application uses block retirement techniques.
6. This information will be available in a technical paper. Please call Intel's Application hotline or your local Intel sales office for more information.

7.0 DERATING CURVES

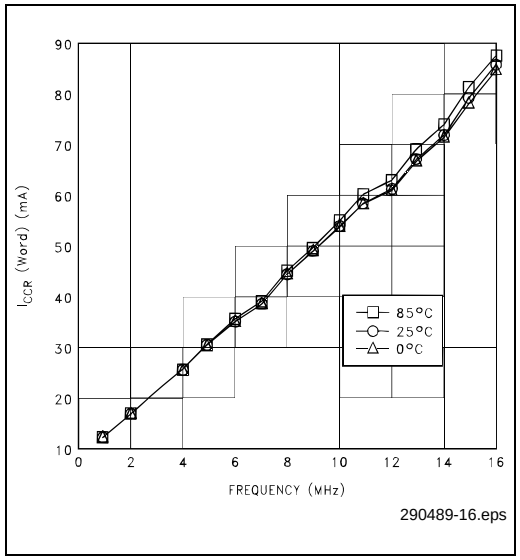


Figure 17. I_{CC} vs. Frequency (V_{CC} = 5.5V) for x8 or x16 Operation

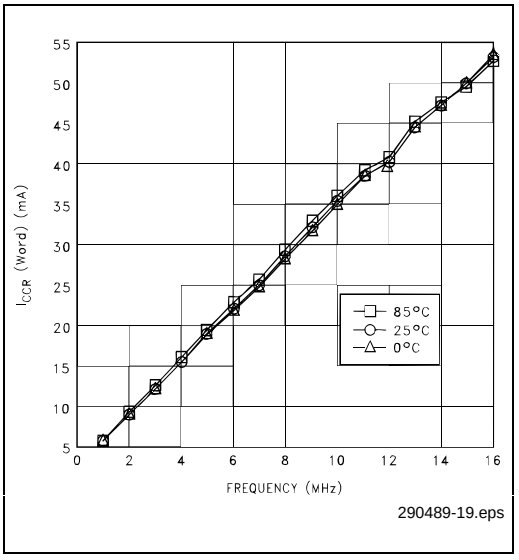


Figure 19. I_{CC} vs. Frequency (V_{CC} = 3.6V) for x8 or x16 Operation

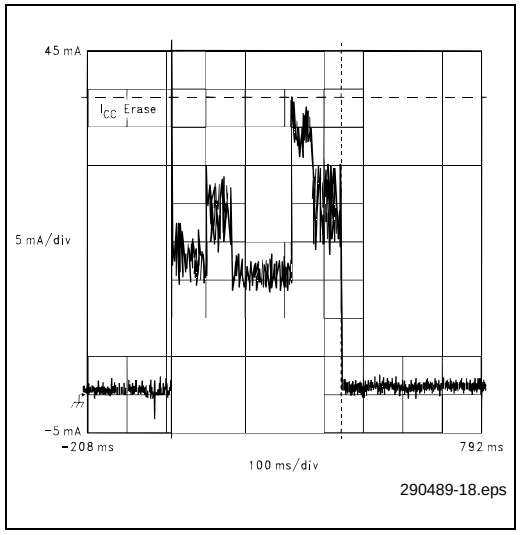


Figure 18. I_{CC} during Block Erase

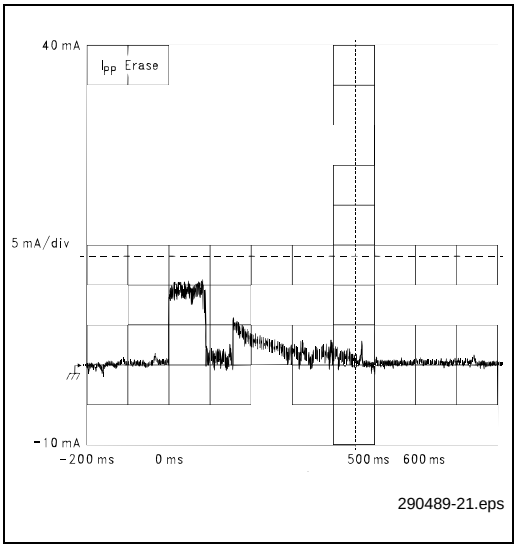


Figure 20. I_{PP} during Block Erase

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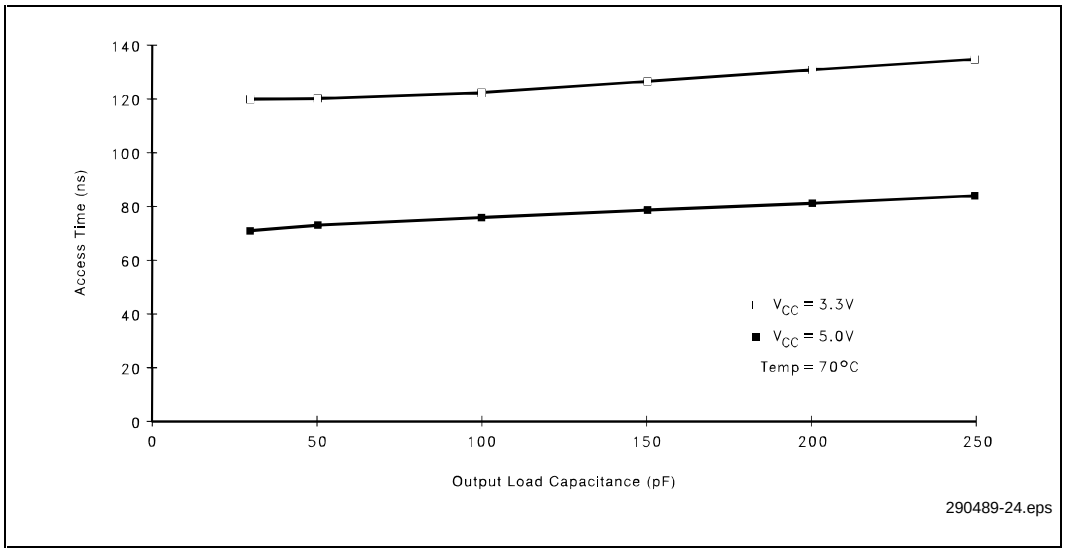

Figure 21. Access Time (t_{ACC}) vs. Output Loading

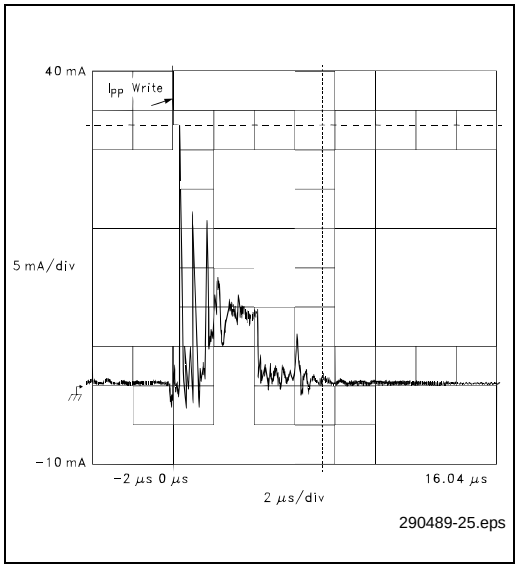

Figure 22. I_{PP} during Word Write Operation

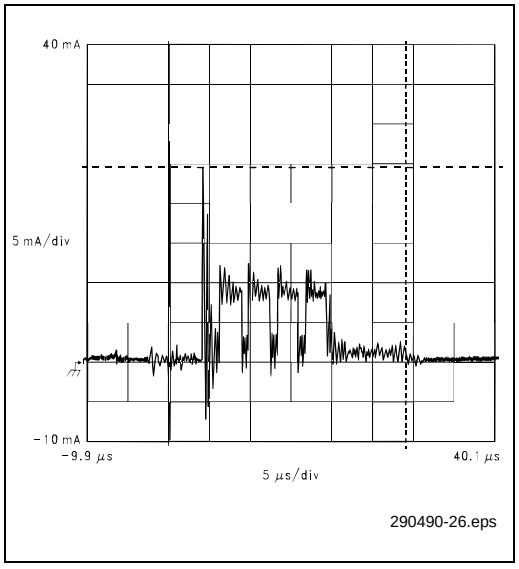

Figure 23. I_{PP} during Page Buffer Write Operation

8.0 MECHANICAL SPECIFICATIONS

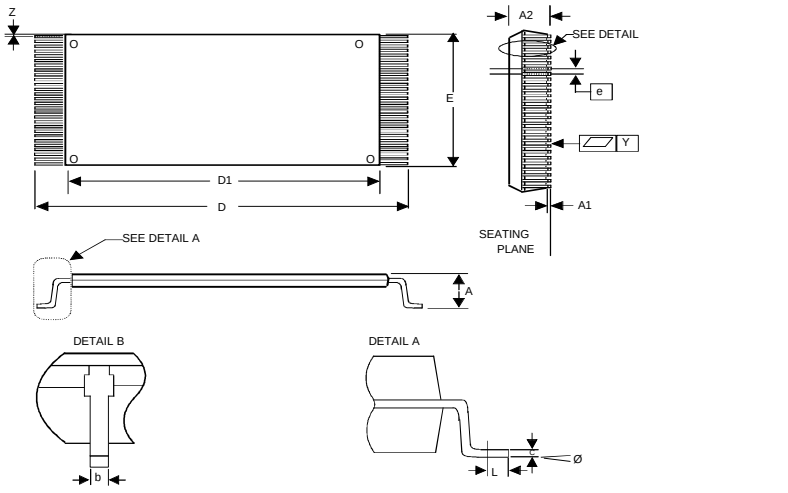

Figure 24. Mechanical Specifications of the Dual Die 56-Lead TSOP Type I Package

Family: Dual Die Thin Small Out-Line Package				
Symbol	**Millimeters**			**Notes**
	Minimum	**Nominal**	**Maximum**	
A			1.20	
A_1	0.05			
A_2	0.965	0.995	1.025	
b	0.100	0.150	0.200	
c	0.115	0.125	0.135	
D_1	18.20	18.40	18.60	
E	13.80	14.00	14.20	
e		0.50		
D	19.80	20.00	20.20	
L	0.500	0.600	0.700	
N		56		
∅	0°	3°	5°	
Y			0.100	
Z	0.150	0.250	0.350	

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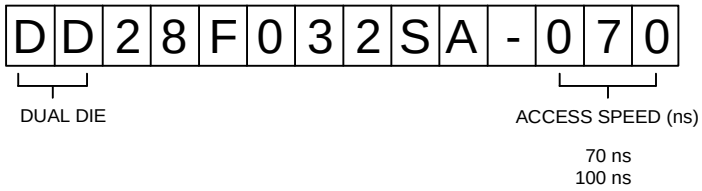
9.0 DEVICE NOMENCLATURE/ORDERING INFORMATION



NOTES:
Two valid combinations of speeds exist:
DD28F032SA-070, DD28F032SA-080, DD28F032SA-150
or
DD28F032SA-100, DD28F032SA-150

Option	Order Code	Valid Combinations		
		V_{CC} = 3.3V ± 0.3V, 50 pF	**V_{CC} = 5.0V ± 5%, 30 pF**	**V_{CC} = 5.0V ± 10%, 100 pF**
1	DD28F032SA-070	DD28F032SA-150	DD28F032SA-070	DD28F032SA-080
2	DD28F032SA-100	DD28F032SA-150		DD28F032SA-100

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10.0 ADDITIONAL INFORMATION

Order Number	Document/Tool
297372	*16-Mbit Flash Product Family User's Manual*
290606	*Intel StrataFlash™ Technology 32 and 64 Mbit* Datasheet
290429	*28F008SA 8-Mbit FlashFile™ Memory* Datasheet
292126	*AP-377 16-Mbit Flash Product Family Software Drivers 28F016SA, 28F016SV, 28F016XS, 28F016XD*
292144	*AP-393 28F016SV Compatibility with 28F016SA*
292159	*AP-607 Multi-Site Layout Planning with Intel's Flash File™ Components*
297508	FLASHBuilder Design Resource Tool
297408	*28F016SA/DD28F032SA Specification Update*

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.

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