AB-58

APPLICATION BRIEF

28F016XD-Based SIMM Designs

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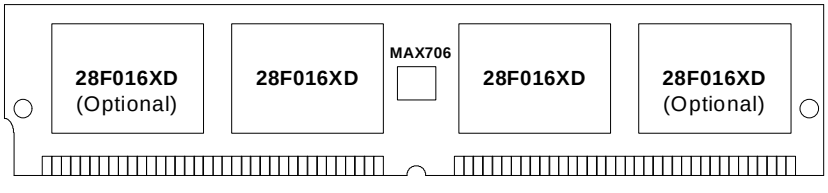
1.0 INTRODUCTION

This application brief provides design information for SIMM (**S**ingle **I**n-Line **M**emory **M**odule) configurations based on the 28F016XD flash memory. The 28F016XD is an Intel 16-Mbit flash memory component with a multiplexed address bus hardware interface, compatible with system DRAM controllers. As such, it is an ideal high-density flash memory for use in existing designs with DRAM SIMM connectors, or in new designs where flexibility in system memory configuration is needed. The 28F016XD preserves all traditional FlashFile™ memory attributes, including per-bit programmability and per-block eraseability. Its low power consumption, full nonvolatility (i.e., no refresh required) and in-system updateability are desirable attributes in comparison to the DRAM memory alternative. The 28F016XD supports both standard and fast page mode reads/writes and all refresh cycles (which it internally disregards).

The example design explained in detail in this application brief (Section 2), uses the JEDEC 72-lead DRAM SIMM standard and supports densities of 1-Mbyte x 32 and 2-Mbyte x 32. Section 3 discusses ideas for extrapolating this design to other JEDEC DRAM SIMM pinouts, while Section 4 provides software guidelines corresponding to flash memory-based SIMM hardware designs. See Section 6 for additional information on Intel's flash memory products.

2.0 72-LEAD SIMM DESIGN EXAMPLE

Figure 1 shows a full-size layout for the 72-lead SIMM explained in this section, while Tables 1 and 2 show and describe the SIMM pinout. Figure 2 shows the SIMM component interconnect.



NOTE:
Filter and bypass capacitors not shown.

Figure 1. Flash Memory-Based 72-Lead SIMM (1M x 32 or 2M x 32) with Identical Dimensions and Pinout as the DRAM-Based Alternative

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Table 1. 72-Lead SIMM Pinout

1	GND	13	A_1	25	DQ_{22}	37	NC	49	DQ_8	61	DQ_{13}
2	DQ_0	14	A_2	26	DQ_7	38	NC	50	DQ_{24}	62	DQ_{30}
3	DQ_{16}	15	A_3	27	DQ_{23}	39	GND	51	DQ_9	63	DQ_{14}
4	DQ_1	16	A_4	28	A_7	40	CAS_0#	52	DQ_{25}	64	DQ_{31}
5	DQ_{17}	17	A_5	29	NC	41	CAS_2#	53	DQ_{10}	65	DQ_{15}
6	DQ_2	18	A_6	30	V_{CC}	42	CAS_1#	54	DQ_{26}	66	NC
7	DQ_{18}	19	NC	31	A_8	43	CAS_3#	55	DQ_{11}	67	PD_1
8	DQ_3	20	DQ_4	32	A_9	44	RAS_0#	56	DQ_{27}	68	PD_2
9	DQ_{19}	21	DQ_{20}	33(1)	NC/RAS_3#	45(1)	NC/RAS_1#	57	DQ_{12}	69	PD_3
10	V_{CC}	22	DQ_5	34	RAS_2#	46	NC	58	DQ_{28}	70	PD_4
11	NC	23	DQ_{21}	35	NC	47	W#	59	V_{CC}	71	NC
12	A_0	24	DQ_6	36	NC	48	NC	60	DQ_{29}	72	GND

NOTES:

1. Pin 33 is a NC for the 1M x 32 SIMM and RAS_3# for the 2M x 32 SIMM.
2. Pin 45 is a NC for the 1M x 32 SIMM and RAS_1# for the 2M x 32 SIMM.

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Table 2. 72-Lead SIMM Pin Description

Symbol	Type	Name and Function
A_0 - A_9	INPUT	**MULTIPLEXED ROW/COLUMN ADDRESSES:** Select a location within the flash memory array in conjunction with appropriate RAS# and CAS# signals. Row (upper) addresses are latched on the falling edge of RAS#, while column (lower) addresses are latched on the falling edge of CAS#.
DQ_0 - DQ_{31}	INPUT/ OUTPUT	**DATA BUS:** Inputs flash memory data and commands during CUI write cycles. Outputs flash memory array, buffer, identifier or status data in the appropriate read mode. Floated when the SIMM is de-selected or the outputs are disabled.
RAS_{0-3}#	INPUT	**ROW ADDRESS STROBE:** Latches row address information on inputs A_{0-9} when RAS# transitions low. A subsequent CAS# low transition initiates flash memory read or write operations. RAS_0# selects the lower 1M x 32 memory bank, while RAS_1# selects the upper 1M x 32 bank (for the 2M x 32 SIMM). Signals RAS_2# and RAS_3# are not used in the design shown in Section 2.
CAS_{0-3}#	INPUT	**COLUMN ADDRESS STROBE:** Latches column address information on inputs A_{0-9} when CAS# transitions low. When preceded by a RAS# low transition, CAS# low initiates flash memory read or write operations in conjunction with W#. Subsequent CAS# low transitions, with RAS# held low, enable fast page mode reads/writes. CAS_0# selects the lower 16 bits of a memory bank, while CAS_2# selects the upper 16 bits. Signals CAS_1# and CAS_3# are not used in the design shown in Section 2.
W#	INPUT	**WRITE ENABLE:** Controls access to the CUI, Page Buffers, Data Queue Registers and Address Queue Latches. W# is active low and initiates writes in combination with RAS# and CAS# low. W# inactive high with RAS# and CAS# low signifies a flash memory read operation. RAS# and CAS# high override W# low.
PD_{1-4}	OUTPUT	**PRESENCE DETECT:** Indicates SIMM speed/density information for system identification. Various combinations of PD pins, either connected to GND or left not connected (pulled high by a resistor on the system board) refer to JEDEC standards, as indicated in Table 3.
V_{CC}	INPUT	**OPERATIONAL AND ERASE/WRITE POWER SUPPLY (5V ± 0.5V).** Do not leave any power pins unconnected. V_{CC} also provides the flash memory V_{PP} update voltage. The design example in Section 2 does not support operation at V_{CC} = 3.3V ± 0.3V (see Section 3.4).
GND	SUPPLY	**GROUND FOR ALL INTERNAL CIRCUITRY:** Do not leave any ground pins floating.
NC		**NO CONNECT:** Lead may be driven or left floating.

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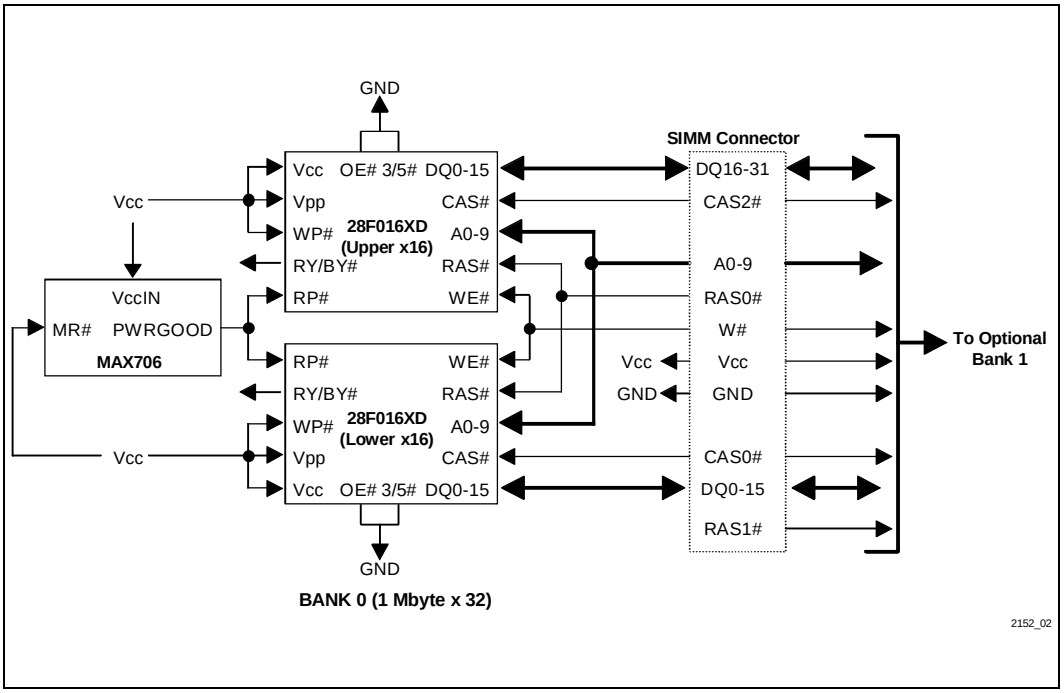

Figure 2. The 28F016XD's Multiplexed Address Bus Interface Makes DRAM-Compatible SIMM Designs Simple

2.1 Address and Data Bus

The multiplexed address and data buses of all flash memories are connected together. See the 28F016XD data sheet (Additional Information, Section 6) for per-component address and data bus pin capacitance. RAS#, CAS# and W# control prevents data bus contention between multiple flash memory components.

2.2 RAS#, CAS#, W#

The 28F016XD is a x16-only flash memory, and each 28F016XD contains one CAS# input. CAS_0# connects to the lower 16-bit component in each 28F016XD bank, while CAS_2# connects to the upper 16-bit component. Therefore, this interface supports x16 or x32 reads and writes. RAS_0# selects the first 1 Mbyte x 32 bank, while RAS_1# selects the optional second bank. W# from the SIMM interface connects to all flash memories.

2.3 SIMM Power Pins

V_{CC} from the SIMM interface connects to the V_{CC} and V_{PP} inputs of all 28F016XD flash memories, and V_{CC} also connects to the optional supply voltage monitoring circuit. GND from the SIMM interface connects to all SIMM component GNDs. This design uses the 5.0V V_{PP} option of Intel's SmartVoltage technology. A small ceramic capacitor filters each flash memory V_{CC} and V_{PP} input, while a larger decoupling capacitor filters V_{CC} at the SIMM interface. See Section 3.4 for alternate V_{CC} and V_{PP} techniques.

2.4 Other 28F016XD Signals

RP# Reset/Power-Down

This design includes an optional low-cost supply voltage monitoring circuit (Maxim MAX706) whose POWERGOOD output controls flash memory RP# inputs. This scheme protects the flash memory from

spurious command writes during system power transitions. Include the monitoring circuit unless you can guarantee that your DRAM controller holds the RAS#/CAS# combination and W# inactive with V_{CC} above V_{LKO} (see 28F016XD specifications) in all cases except when intentionally writing to flash memory. Experience has shown that many memory controllers have unspecified and unpredictable operation during system power transitions.

If the monitoring circuit is not used, remove the 8-pin SOIC layout from the SIMM and connect RP# to V_{CC}. Alternatively, connect SOIC layout pins corresponding to the (non-present) monitoring circuit V_{CC} input and POWERGOOD output, together with a 0-ohm resistor.

WP#

This design connects WP# to V_{CC}, driving this input inactive at all times.

RY/BY#

This design does not use the RY/BY# output, leaving it disconnected. System software should poll the flash memory Status Registers to determine device status and completion of internal operations.

OE#

This design connects OE# to GND. RAS# and CAS# active, in conjunction with an inactive high W#, initiate a flash memory read. W# active low overrides the state of OE#. RAS# and CAS# inactive high override OE# active low.

3/5#

This design connects 3/5# to GND (for 5V V_{CC} Operation). This design example does not support operation at 3.3V V_{CC} (see Section 3.4).

2.5 Other SIMM Signals

PD_{1-4}

PD leads are connected to GND or left unconnected on the SIMM, and are connected to V_{CC} via pull-up resistors on the system board. Their state (“1” or “0”), when read by system logic, provide SIMM speed/density information and reference the speed bin of the 28F016XD flash memories. JEDEC standard Presence Detect pin combinations for 4-MB, 8-MB and 16-MB (x36 72-pin) SIMMs with t_{RAC} = 100 ns are shown in Table 3. PD combinations for other “non-standard” speed/density combinations are user definable.

Table 3. PD Signal Combinations for Various Densities (t_{RAC} = 100 ns)

	PD_1	PD_2	PD_3	PD_4
4 MB	GND	GND	GND	GND
8 MB	NC	NC	GND	GND
16 MB	GND	NC	GND	GND

3.0 RECOMMENDATIONS FOR DESIGN MODIFICATIONS AND OTHER SIMM INTERFACES

The 72-lead SIMM interface is only one of several pinouts approved by JEDEC and other standards bodies. This section gives recommendations for adapting the design techniques of Section 2 to other SIMM interfaces. In addition, it discusses providing voltages other than 5.0V to the 28F016XD SIMM and enhancing system control of 28F016XD operations.

3.1 Parity

Flash memory is not subject to the alpha particle soft errors that plague DRAM, as it stores the data value (“1” or “0”) intrinsically on the floating gate of the flash memory transistor. For this reason, a parity output was not included as part of the 28F016XD pinout. In systems that employ parity check to confirm the integrity of the DRAM memory subsystem, on-SIMM programmable or dedicated logic can generate parity bits required for the flash memory-based SIMM read interface, if required. See Figure 3 for an example.

3.2 8-Bit or 9-Bit SIMM Interfaces

The 28F016XD is a x16-only flash memory component. When used in a x8 or x9 (see Section 3.1) SIMM pinout, interface logic like that shown in Figure 4 should be used to route system data to the correct 8 bits of the flash memory bus and drive the alternate 8 bits to “1”s. System software must write commands to the flash memory only on the lower 8 bits for such an interface.

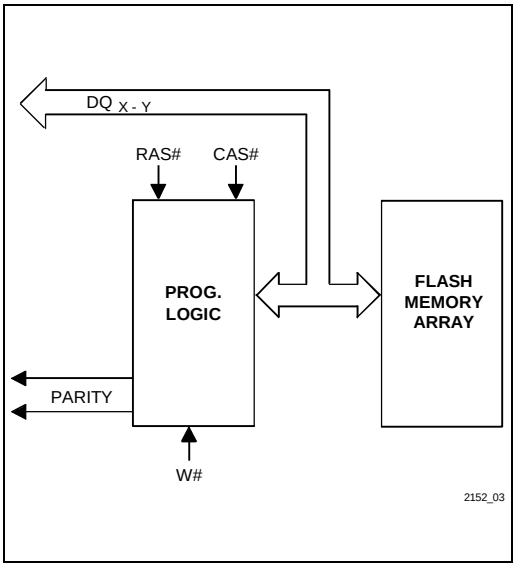

Figure 3. Parity Generation for DRAM Controller Compatibility

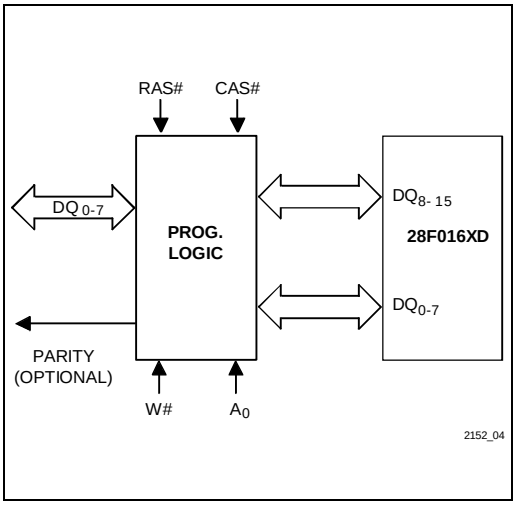

Figure 4. Converting the 16-Bit Flash Memory Data Bus to a x8/x9 System Interface

3.3 Flash Memory Control Input/Output and V_{PP} Control

SIMMs other than the 72-lead version described in Section 2 may include additional inputs and outputs that can provide a system RESET# to the supply voltage monitoring circuit MR# input. Alternatively, if system RESET# includes power supply monitoring, this signal can directly control the 28F016XD RP# inputs. Additionally, system I/O signals can control the flash memory WP# input and route the RY/BY# output to a system port pin or hardware interrupt line. Finally, by separating out supply and program/erase voltage pins, alternate or semi-custom SIMM interfaces can provide 12.0V to the 28F016XD flash memory V_{PP} inputs for fast write performance and switch this program/erase voltage to GND when not updating flash memory contents for additional write protection.

3.4 V_{CC} and V_{PP} Flexibility

The 28F016XD, by virtue of its SmartVoltage technology can be operated at either 3.3V or 5.0V V_{CC}, and at either 5.0V or 12.0V V_{PP}. If 3.3V V_{CC} operation is desired (for lower power), an on-SIMM 3.3V-to-5.0V converter can generate the necessary 5.0V V_{PP} voltage.

Some designs may desire to program and erase the 28F016XD at 12.0V V_{PP} for high write performance. In these cases, include a 5.0V-to-12.0V or 3.3V-to-12.0V converter on the SIMM to generate the 12.0V V_{PP} voltage. See application note AP-357 for industry-representative 12V-converters.

4.0 SOFTWARE GUIDELINES

System software should not attempt to scan/check the 28F016XD memory space as part of system initialization. The 28F016XD does not support the DRAM self-check function. Data combinations written to the 28F016XD may be decoded as valid commands and result in unintended flash memory operations. Checksum calculation and comparison with a checksum data value stored in the flash memory is a recommended technique for ensuring data/code integrity.

The hardware interface described in Section 2 allows only 16- and 32-bit command/data writes to flash memory. When programming a flash memory location, set bits not to be programmed to “1”s as part of the data write. This technique can also be used to mask a write to the alternate byte of a 16-bit word when performing a byte program operation.

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The 72-lead SIMM interface of Section 2 does not allow use of the flash memory RY/BY# output. System software should poll flash memory Status Registers to determine status of device operations, including program and erase.

System software should separate temporary data from code and “permanent” data tables, and route writes to the former to the system DRAM memory space. Flash memory is per-bit programmable (changing data “1”s to “0”s) and per-block erasable (changing data “0”s to “1”s), unlike DRAM, which is fully per-bit alterable.

5.0 CONCLUSION

This application brief has described one possible SIMM design using Intel’s 28F016XD Flash memory, and has provided design recommendations for alternative SIMM approaches. Consult reference documentation for a more complete understanding of device capabilities and design techniques. Please contact your local Intel or distribution sales office for more information on Intel’s flash memory products.

6.0 ADDITIONAL INFORMATION

6.1 References

Order Number	Document/Tool
290533	28F016XD DRAM-Interface Flash Memory Datasheet
297372	"16-Mbit Flash Product Family User's Manual"
292165	AB-62, “Compiled Code Optimizations for Flash Memories”
292092	AP-357, “Power Supply Solutions for Flash Memory”
292123	AP-374, "Flash Memory Write Protection Techniques"
292126	AP-377, "16-Mbit Flash Product Family Software Drivers, 28F016SA/SV/XS/XD"
292131	AP-384, “Designing with the 28F016XD”
292163	AP-610, “Flash Memory In-System Code and Data Update Techniques”
292168	AP-614, “Adapting DRAM Based Designs for the 28F016XD”
Contact Intel/Distribution Sales Office	FLASHBuilder Utility
Contact Intel/Distribution Sales Office	28F016XD Benchmarking Utility
Contact Intel/Distribution Sales Office	28F016XD iBIS Models
Contact Intel/Distribution Sales Office	28F016XD VHDL Model
Contact Intel/Distribution Sales Office	28F016XD Timing Designer Library Files
Contact Intel/Distribution Sales Office	28F016XD Orcad and ViewLogic Schematic Symbols

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6.2 Revision History

Number	Description
-001	Original Version
002	Added 3/5# pin to Figure 2 and Section 2.4. Corrected Figures 1 and 2 to reference the MAX706 supply monitoring circuit. Updated “Additional Information” Section Minor cosmetic changes throughout document.

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