Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845GE/845PE Chipset

Platform Design Guide

October 2002

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Contents

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Revision History

Rev. No.	Description	Date
-001	• Initial Release.	October 2002

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1 Introduction

This design guide has Intel design recommendations for systems based on the Intel® Pentium® 4 processor in the 478-pin package, the Intel® 845GE GMCH / 845PE MCH, and the Intel® ICH4. Design issues (e.g., thermal considerations) should be addressed using specific design guides or application notes for the processor, the (G)MCH, and the ICH4.

These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into two categories:

- **Design Recommendations:** Items based on Intel's simulations and lab experience to date and are strongly recommended, if not necessary, to meet the timing and signal quality specifications.
- **Design Considerations:** Suggestions for platform design that provide one way to meet the design recommendations. Design considerations are based on the reference platforms designed by Intel. They should be used as an example, but may not be applicable to particular designs.

Unless otherwise specified, the information in this document applies to both the 845GE chipset and 845PE chipset. The term (G)MCH refers to both the 82845GE GMCH and 82845PE MCH.

Note: In this document "processor" and "Pentium 4 processor" refer to the Intel Pentium 4 processor in the 478-pin package.

Note: The guidelines recommended in this document are based on experience and simulation work completed by Intel while developing systems with Pentium 4 processor in the 478-pin package and the 845GE/845PE chipset. This work is ongoing, and the recommendations and considerations are subject to change.

Platform schematics can be obtained and are intended as a reference for board designers. While the schematics may cover a specific design, the core schematics remain the same for most platforms. The schematic set provides a reference schematic for each platform component, and common system board options. Additional flexibility is possible through other permutations of these options and components.

1.1 Terminology

This section defines conventions and terminology that will be used throughout this document.

Table 1-1. Platform Conventions and Terminology

Convention/ Terminology	Definition
ADD Card	AGP Digital Display Card provides digital display options for 845GE/845PE (G)MCH when plugged into an AGP connector.
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGP	Accelerated Graphics Port. Refers to the AGP/PCI interface that is in the (G)MCH. It supports a 1.5 V 66/266 MHz component.
AGTL+	The Processor System Bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors that provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Corner	Describes how a component performs when all parameters that could impact performance are adjusted simultaneously to have the best or worst impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. Performance of an electronic component may change as a result of (including, but not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the “slow” corner means having a component operating at its slowest, weakest drive strength performance. Similar discussion of the “fast” corner means having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bind the extremes between slowest, weakest performance and fastest, strongest performance.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. Backward Crosstalk – coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal. Forward Crosstalk – coupling that creates a signal in a victim network that travels in the same direction as the aggressor’s signal. Even Mode Crosstalk – coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. Odd Mode Crosstalk – coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
DDR	Double Data Rate SDRAM
DVO	Digital Video Out port. Used for the 845GE chipset digital display channel. The 845GE has two DVO ports that are multiplexed with AGP. This port is not on the 845PE chipset.

Convention/ Terminology	Definition
Flight Time	Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, *flight time* is defined to be: Time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; e.g., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings. Maximum and Minimum Flight Time – Flight time variations can be caused by many different variables. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects. • Maximum flight time is the largest acceptable flight time a network will experience under all variations of conditions. • Minimum flight time is the smallest acceptable flight time a network will experience under all variations of conditions.
FWH	Firmware Hub
GMCH	The Graphics-Memory Controller Hub component that contains the processor interface, DRAM controller, AGP interface and an integrated 3D/2D/display core. It communicates with the ICH4 through the Hub Interface
GTL+	GTL+ is the bus technology used by the Intel® Pentium® Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) bus technology.
Hub Interface	Proprietary Hub interconnect that ties the (G)MCH to the ICH4.
Intel® ICH4	The I/O Controller Hub component that contains various IO functions. It communicates with the (G)MCH through the Hub Interface.
IGD	Internal/Integrated Graphics Device. Graphics device integrated into the GMCH
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
LPC	Low Pin Count interface.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	The distance between one agent pin and the corresponding agent pin at the far end of the bus.
Overshoot	Maximum voltage observed for a signal at the device pad.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulation.
PSB	Processor System Bus. Connection between the 82845GE GMCH / 82845PE MCH and the processor.

Convention/ Terminology	Definition
Pin	The contact point of a component package to the traces on a substrate, like the system board. Signal quality and timings can be measured at the pin.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena.
SDRAM	Synchronous Dynamic Random Access Memory
System Bus	The System Bus is the microprocessor bus of the Intel® Pentium® 4 processor in the 478-pin package. It may also be termed “system bus” in implementations where the System Bus is routed to other components. The P6 bus was the microprocessor bus of the Intel® Pentium® Pro, Intel® Pentium II, and Intel® Pentium III processors. The System Bus is not compatible with the P6 bus.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
SSO	Simultaneous Switching Output (SSO) effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or “push-out”), or a decrease in propagation delay (or “pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Test Load	Intel uses a 50 Ω test load for specifying its components.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	Minimum voltage observed for a signal to extend below VSS at the device pad.
USB	Universal Serial Bus
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
VREF Guardband	A guardband defined above and below VREF to provide a more realistic model accounting for noise such as VTT and VREF variation.

1.2 Related Documentation

Reference the following documents or models for more information. All Intel issued documentation revision numbers are subject to change, and the latest revision should be used. The specific revision numbers referenced should be used for all documents not released by Intel. Contact your field representative for information on how to obtain Intel issued documentation.

Document	Document Number/Source
Intel® 845GE/845PE Chipset: Intel® 82845GE Graphics and Memory Controller Hub (GMCH) and Intel® 82845PE Memory Controller Hub (MCH) Datasheet	http://developer.intel.com/design/chipsets/datashts/251924.htm
Intel® 845GE/845PE Chipset Thermal Design Guide	http://developer.intel.com/design/chipsets/designex/251926.htm
AGP Design Guide Revision 1.5	http://developer.intel.com/technology/agp/downloads/DesignGuide/062601.htm
Intel® Pentium® 4 Processor in the 478-pin Package at 1.40 GHz, 1.50 GHz, 1.60 GHz, 1.70 GHz, 1.80 GHz, 1.90 GHz, and 2 GHz Datasheet	http://developer.intel.com/design/pentium4/datashts/249887.htm
Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process at 2 GHz, 2.20 GHz, 2.26 GHz, 2.40 GHz, 2.50 GHz, 2.53 GHz, 2.60 GHz, 2.66 GHz, and 2.80 GHz	http://developer.intel.com/design/Pentium4/datashts/298643.htm
Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines	http://developer.intel.com/design/pentium4/guides/249889.htm
Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet	http://developer.intel.com/design/chipsets/datashts/290744.htm
Intel® 82801DB I/O Controller Hub 4 (ICH4): Thermal and Mechanical Design Guidelines	http://developer.intel.com/design/chipsets/designex/258651.htm
Intel® Pentium® 4 Processor VR Down Design Guidelines	http://developer.intel.com/design/pentium4/guides/249891.htm
Intel® Pentium® 4 Processor 478-Pin Socket (mPGA478) Design Guidelines	http://developer.intel.com/design/pentium4/guides/249890.htm
Intel® PC SDRAM Unbuffered DIMM Specification	http://developer.intel.com/technology/memory/pcsdram/spec/index.htm
Intel® PC SDRAM Specification	http://developer.intel.com/technology/memory/pcsdram/spec/index.htm
Accelerated Graphics Port Interface Specification	http://www.agpforum.org/
Low Pin Count Interface Specification	http://www.intel.com/design/chipsets/industry/lpc.htm
PCI Local Bus Specification	www.pcisig.com
PCI-to-PCI Bridge Specification	www.pcisig.com
PCI Bus Power Management Interface Specification	www.pcisig.com
Universal Serial Bus Revision 2.0, Specification	http://www.usb.org/developers/docs.html

Document	Document Number/Source
Advanced Configuration and Power Interface Specification (ACPI), Revision 1.0b	http://www.teleport.com/~acpi/
Communication and Networking Riser (CNR) Specification Revision 1.2	http://developer.intel.com/technology/cnr/index.htm
ITP700 Debug Port Design Guide	http://developer.intel.com/design/Xeon/guides/249679.htm
AC '97 Specification, Revision 2.2	http://developer.intel.com/ial/scalableplatforms/audio/index.htm#97spec/
Intel® Pentium® 4 Processor VR-Down Design Guidelines	http://developer.intel.com/design/Pentium4/guides/249891.htm
Intel® JEDEC® DDR 200 Registered DIMM Specification Addendum	http://www.intel.com/technology/memory/pcsdram/spec/ddr200_dimm_rev09.htm
Advanced Configuration and Power Interface Specification (ACPI) Revision 2.0a	http://www.acpi.info/spec.htm

NOTE: For additional information, contact your Intel Field Representative.

1.3 System Overview

The Pentium 4 processor in the 478-pin package with the (G)MCH and the ICH4 delivers a stable mainstream desktop platform solution. The processor and the chipset support the System Bus Protocol.

The (G)MCH component provides the processor interface, system memory interface, Hub Interface, AGP interface, and an integrated graphics device with analog and digital display ports. This product provides flexibility and scalability in graphics subsystem performance. Competitive internal graphics may be scaled with the addition of an AGP interface card or an ADD card.

The ICH4 integrates a Universal Serial Bus 2.0 controller, Ultra ATA/100 controller, Low Pin Count interface, Firmware Hub Flash BIOS interface controller, PCI interface controller, integrated LAN, AC ’97 digital controller, and a Hub Interface for communication with the (G)MCH.

An ACPI compliant 845GE/845PE chipset platform can support the *Full-On (S0), Stop Grant (S1), Suspend to RAM (S3), Suspend to Disk (S4), and Soft-Off (S5)* power management states. Through the use of an appropriate LAN connect, the chipset also supports *Wake-On LAN** for remote administration and troubleshooting. The use of AC ’97 allows the OEM to use *software configurable* AC ’97 audio and modem coder/decoders (codecs).

The chipset architecture also enables a security and manageability infrastructure through the Firmware Hub (FWH) component.

1.3.1 Intel® 845GE/845PE Chipset

The 845GE/845PE chipsets each contain two *core* components designed for the desktop platform:

- For the 845GE chipset, the components are the 82845GE Graphics and Memory Controller Hub (GMCH) and the 82801DB Intel® I/O Controller Hub 4 (ICH4).
- For the 845PE chipset, the components are the 82845PE Memory Controller Hub (MCH) and the 82801DB I/O Controller Hub 4 (ICH4).

The (G)MCH and ICH4 are interconnected via an Intel proprietary interface called hub interface. The Hub Interface is designed into the 845GE/845PE chipsets to provide an efficient, high bandwidth communication channel between the (G)MCH and the ICH4.

1.3.2 Intel® 82845GE GMCH and 82845PE MCH

The (G)MCH is available in a 760 ball FCBGA package, and has the following functionality:

- Supports 2 DIMMS of DDR-SDRAM (DDR266/333)
- AGTL+ host bus with integrated termination supporting 32-bit host addressing
- 1.5 V AGP interface with 4x SBA/data transfer and 2x/4x fast write capability
    - Multiplexed with DVO ports (845GE chipset only)
- 8-bit, 66 MHz 4x Hub Interface to the ICH4
- IGD with analog and digital display ports (845GE chipset only)

1.3.2.1 Packaging/Power

- 37.5 mm x 37.5 mm 760-ball FCBGA package with 1-mm ball pitch
- 1.5 V core with 1.5 V, 2.5 V, 3.3 V and AGTL+ I/O

1.3.2.2 Processor System Bus

- Supports single processor
- Processor packaging: mPGA 478 package
- Supports 400/533 MHz System Bus
- System Bus interrupt delivery
- Supports 32-bit addressing for access to 4-GB memory
- Supports AGTL+ on-die termination

1.3.2.3 System Memory Interface

- Supports one 64-bit wide DDR SDRAM data channel
- Available bandwidth up to 2.7 GB/s (DDR333)
- Supports 64-Mb, 128-Mb, 256-Mb, and 512-Mb SDRAM technologies
- Supports only x8 and x16 SDRAM devices with 4-banks
- Does not support ECC functionality
- Registered DIMMs not supported
- Supports unbuffered non-ECC DIMMs only
- Up to 16 simultaneously open pages (4 per row, 4 rows maximum)
- SPD (Serial Presence Detect) scheme for DIMM detection
- Suspend-to-RAM support using CKE

Double Data Rate (DDR) SDRAM Configuration

- Up to 2.0 GB of 266 MHz or 333 MHz DDR SDRAM
- Supports up to 2 DDR DIMMs, single-sided and/or double-sided
- Supports DDR266/333 unregistered 184-pin non-ECC DDR SDRAM DIMMs
- Supports configurations defined in the JEDEC DDR DIMM specification only
- Does not support double-sided x16 DDR DIMMs
- Supports Command-Per-Clock Accesses

1.3.2.4 Graphics Interface

Integrated Graphics Controller (82845GE only)

- Integrated 2D/3D graphics accelerator
- 256 bit graphics core
- Texture mapped 3D with point sampled, Bilinear, Trilinear, and Anisotropic filtering
- Hardware setup with support for strips and fans
- Hardware motion compensation assist for software MPEG/DVD decode
- Intel Digital Video Out (DVO) ports add support for digital displays and TV-out
- Integrated 350 MHz RAMDAC

Accelerated Graphics Port (AGP) Interface

- Supports a single, 1.5 V only, AGP 2.0 compliant device
- High priority access support
- Delayed transaction support for AGP reads that cannot be serviced immediately
- AGP semantic traffic to the DRAM is not snooped on the PSB and is therefore not coherent with the processor caches
- AGP interface multiplexed with 2 DVO ports (845GE chipset only)
- Supports ADD cards (845GE chipset only)

1.3.2.5 Hub Interface

- 1.5 V operation; 266 MB/s point-to-point 8-bit Hub Interface to the ICH4
- 66 MHz base clock

1.3.3 Intel® I/O Controller Hub (ICH4)

The ICH4 provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many I/O functions. The ICH4 integrates:

- Upstream Hub Interface for access to the (G)MCH
- 2 channel Ultra ATA/100 Bus Master IDE controller
- 6 USB 2/1.1 ports
- I/O APIC
- SMBus 2.0 controller
- FWH interface
- LPC interface
- AC ’97 2.2 interface
- PCI 2.2 interface
- Integrated System Management Controller
- Integrated LAN Controller

The ICH4 also contains the arbitration and buffering necessary to ensure efficient utilization of these interfaces.

1.3.3.1 Packaging/Power

- 31 mm x 31 mm 421-BGA package
- 1.5 V core, 1.5 V standby, and 3.3 V standby with 1.5 V and 3.3 V I/O

1.3.3.2 Expanded USB Support

- 3 UHCI Host Controllers that includes a root hub with two separate USB ports each, for a total of six legacy USB ports
- 1 EHCI Host Controller that includes a root hub that supports up to six USB 2.0 ports
- Supports a maximum of 6 USB ports at any given time. The connection to either a UCHI or the EHCI is dynamic and dependent on the USB device capability.

1.3.3.3 Integrated LAN Controller

- WfM 2.0 Compliant
- Interface to discrete platform LAN connect component
- 10/100 Mbit/sec Ethernet support

1.3.3.4 Ultra ATA/100 Support

- Ultra ATA/100/66/33, BMIDE and PIO modes
- Independent timing of up to 4 drives, with separate IDE connections for Primary and Secondary cables
- Supports “Native Mode” Register and Interrupt support

1.3.3.5 AC ’97 6-Channel Support

- Supports AC ’97 2.3.
- 20 bit/16 bit audio capability with support for up to six channels of PCM audio output (full AC3 decode)
- Supports 3 codecs with independent PCI functions for audio and modem
- Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center and Woofer for a complete surround sound effect
- Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution.
- Integrated digital link allows several external codecs to be connected
- Third SDATA_IN line
- S/PDIF directed output
- Supports wake-up events (Wake on ring from suspend is supported with an appropriate modem codec)

Note: Modem implementation for different countries must be considered because telephone systems may vary.

1.3.3.6 Manageability and Other Enhancements

- Integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system.
- System management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

1.3.3.7 SMBus 2.0

- Provides an interface to manage peripherals such as serial presence detection (SPD) on DIMMs.
- 32 byte buffer
- Hardware Packet Error Checking
- Host interface allows the processor to communicate via SMBus
- Slave interface allows an external microcontroller to access system resources
- Compatible with most 2-Wire components that are also I^2C compatible.

1.3.3.8 Interrupt Controller

- Support for up to 8 PCI interrupt pins
- Supports PCI 2.2 Message Signaled Interrupts
- Two cascaded 82C59 with 15 interrupts
- Integrated I/O APIC capability with 24 interrupts
- Supports Serial Interrupt Protocol
- Supports Front-Side Bus interrupt delivery

1.3.4 Bandwidth Summary

Table 1-2 describes the bandwidth of critical 845GE/845PE chipset platform interfaces:

Table 1-2. Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth
System Bus	100\133	4	8	3.2 GB/s / 4.2 GB/s
AGP	66	4	4	1.06 GB/s
DVO[1]	Up to 165	2	1.5\3	165 Mpixel/s / 330 Mpixel/s
DAC[1]	Up to 350	N/A	N/A	Up to 350 Mpixel/s
Hub Interface	66	4	1	266 MB/s
PCI 2.2	33	1	4	133 MB/s
DDR-SDRAM	133\166	2	8	2.1 GB/s / 2.7 GB/s

NOTES:
1. 845GE chipset designs only

1.3.5 System Configuration

Figure 1-1 illustrates a typical Pentium 4 processor in the 478-pin package and 845GE chipset-based system configuration for mainstream desktop segments.

Figure 1-1. Typical Intel® 845GE Chipset System Configuration

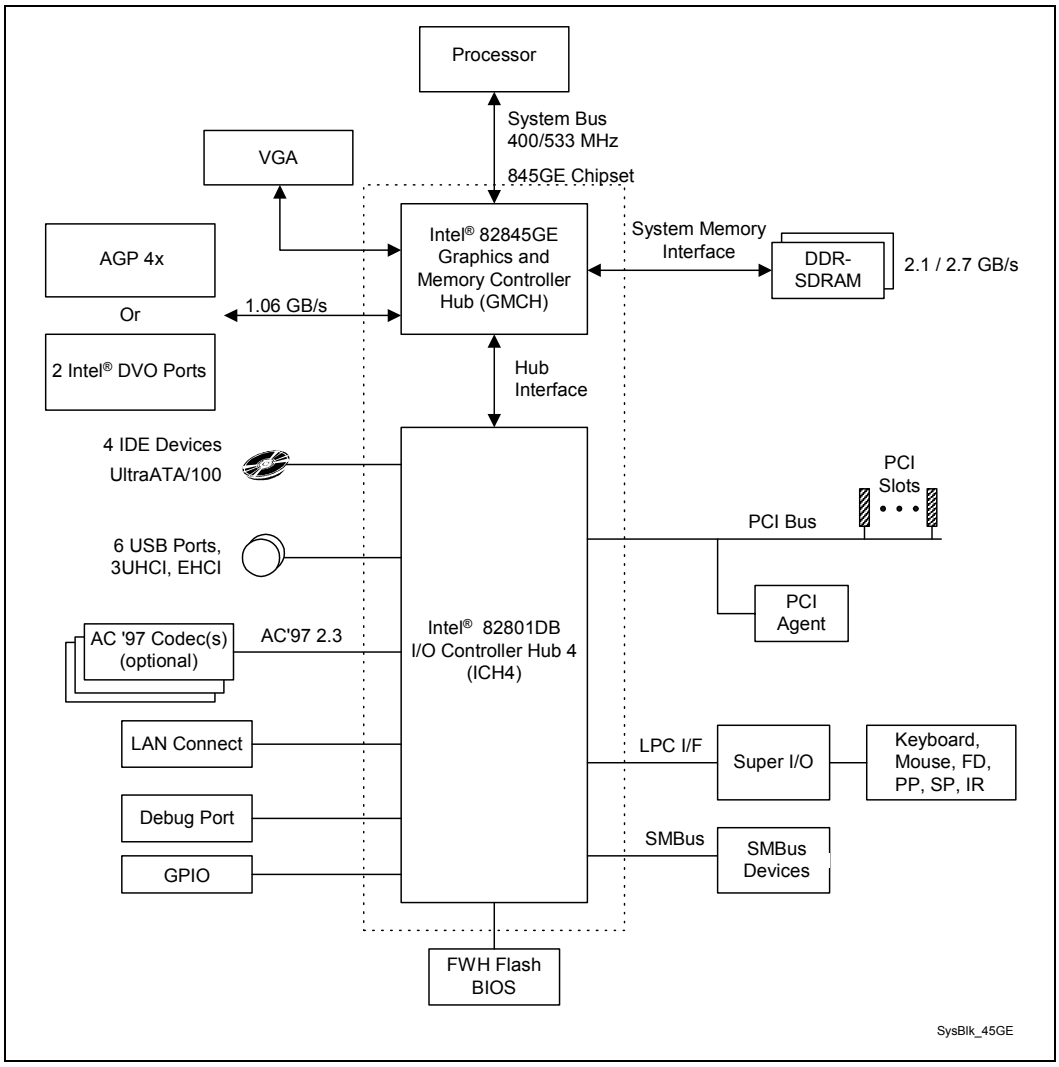
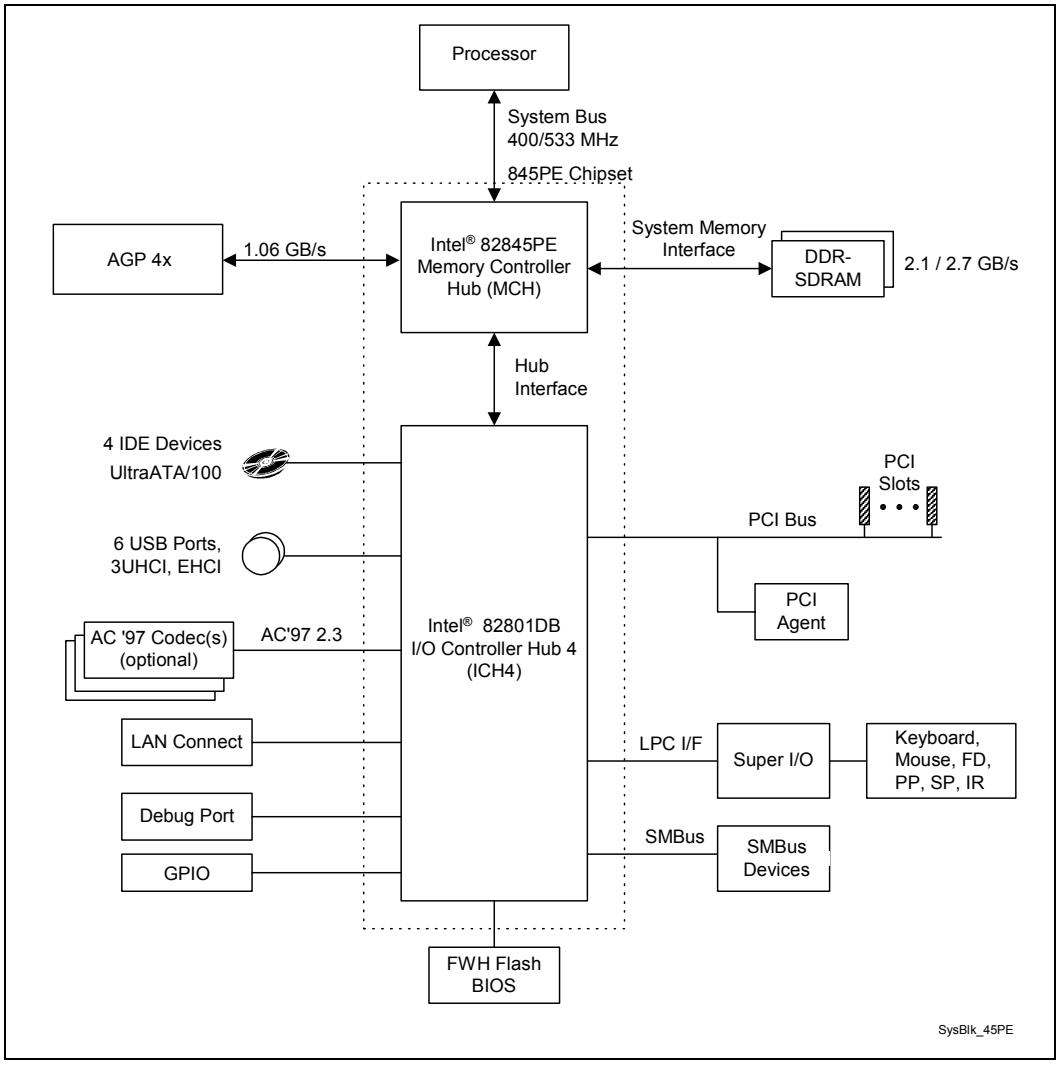


Figure 1-2 illustrates a typical Pentium 4 processor in the 478-pin package and 845PE chipset-based system configuration for mainstream desktop segments.

Figure 1-2. Typical Intel® 845PE Chipset System Configuration



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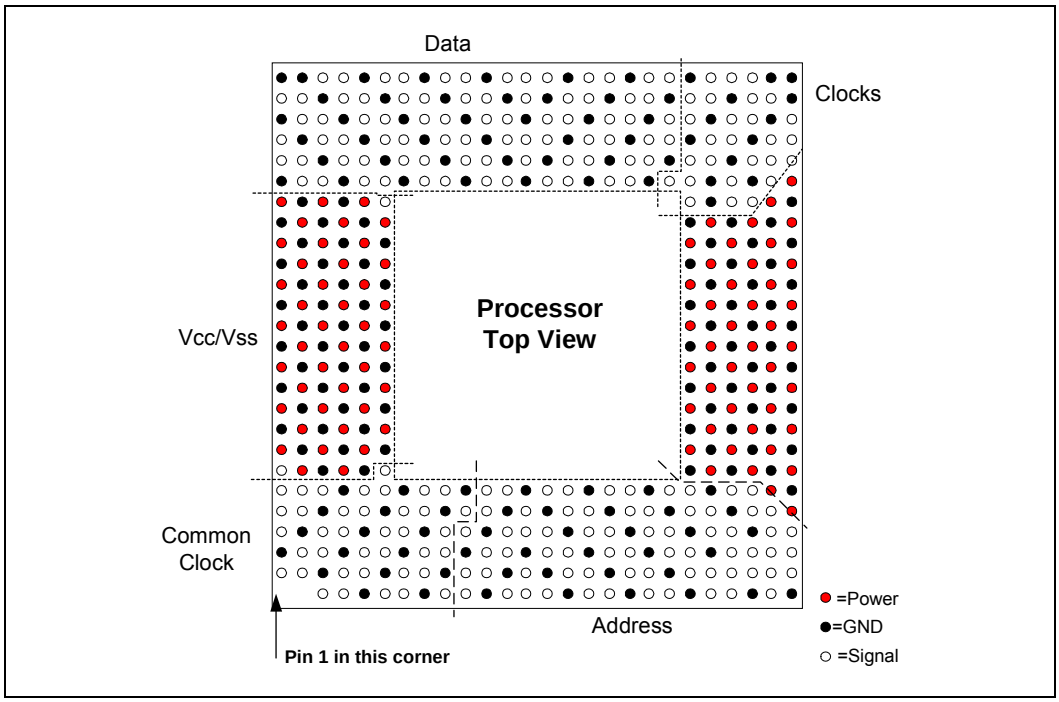
2 Component Quadrant Layout

The preliminary quadrant layouts shown are approximations. The quadrant layout figures do not show the exact component ball count; only general quadrant information is presented and is intended for reference while using this document. Only the exact pin or ball assignment should be used to conduct routing analysis. Refer to the following documents for pin or ball assignment information.

- *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*
- *Intel® Pentium® 4 Processor with 512-KB L2 Cache on .13 Micron Process Datasheet*
- *Intel® 845GE/845PE Chipset Datasheet*
- *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*

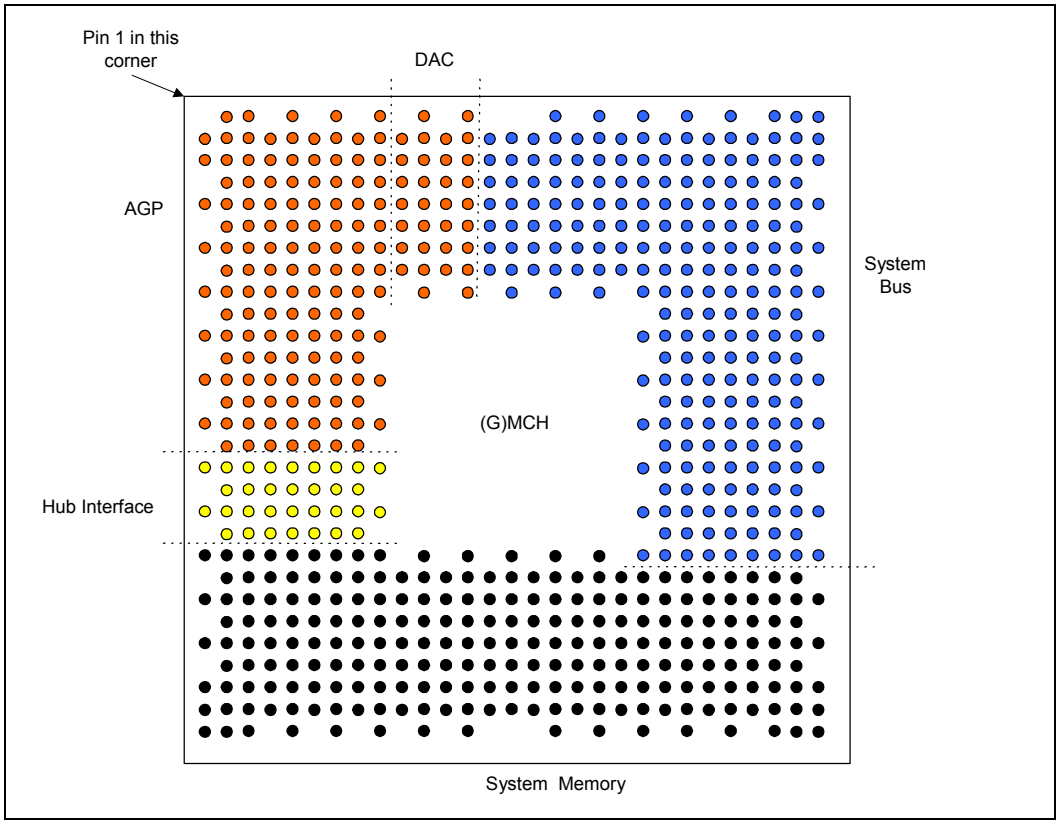
2.1 Intel® Pentium® 4 Processor Component Quadrant Layout

Figure 2-1. Intel® Pentium® 4 Processor in the 478-pin Package Component Quadrant Layout (Top View)



2.2 Intel® (G)MCH Component Quadrant Layout

Figure 2-2. Intel® (G)MCH Component Quadrant Layout (Top View)

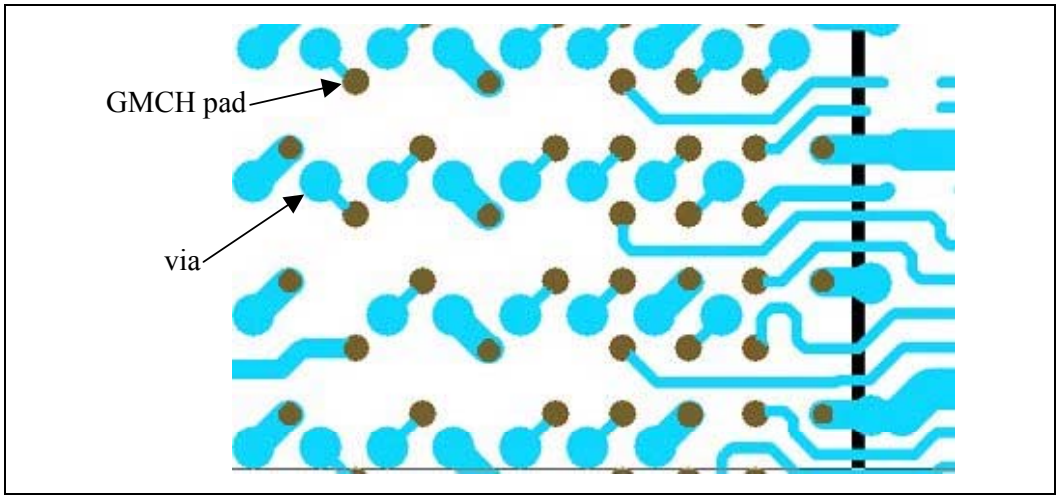


Note: DAC signals are used for 845GE only

2.2.1 Offset-Ballout Advantages

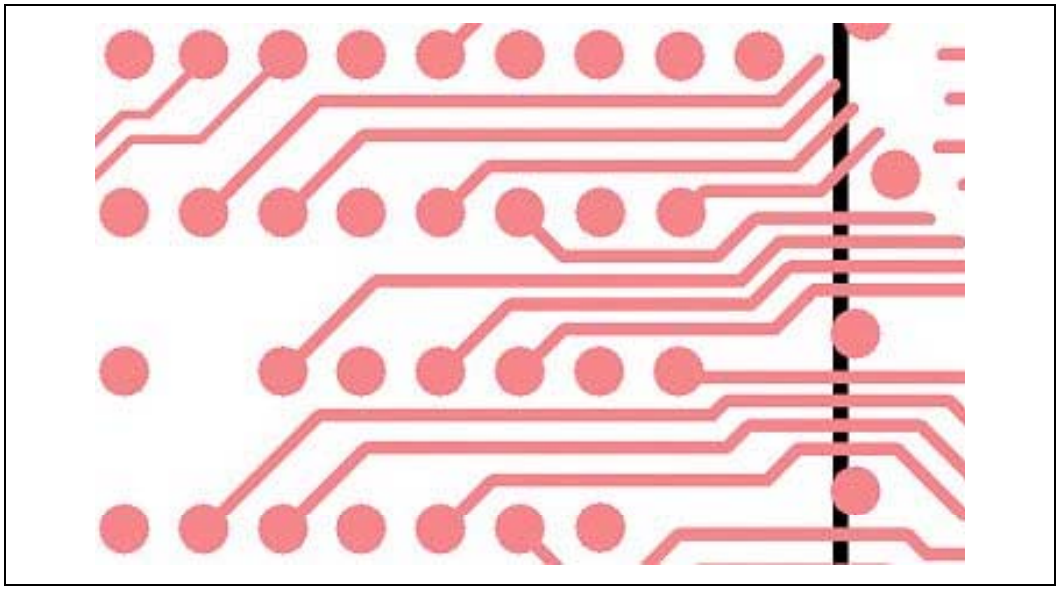
The (G)MCH utilizes an offset ballout pattern to allow for robust power delivery while utilizing the traditional vias discussed in Section 3.2.1. It is strongly recommended that the following breakout and via strategies be used with the (G)MCH. The following two figures show layer one and layer four and illustrate the breakout on the top layer and the breakout for the bottom layer. Notice the vias are arranged in rows, with the rows occurring between every other row of balls. Also notice that the breakout is clean, both on the top layer and on the bottom layer.

Figure 2-3. Layer One Breakout



NOTE: Large circles are vias, and small circles are pads.

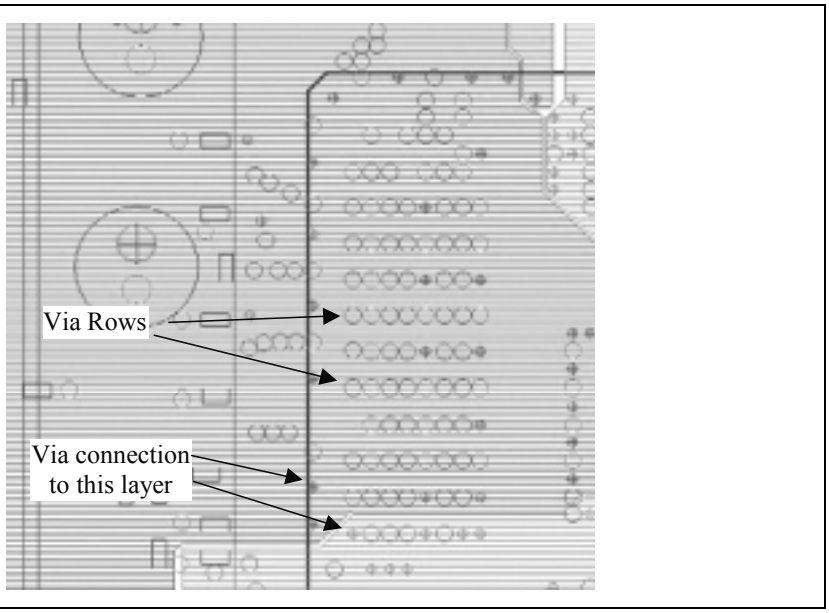
Figure 2-4. Layer Four Breakout



NOTE: Large circles are vias.

Figure 2-5 shows the results of the via rows on layer two (layer two has a ground shape and a power shape underneath the (G)MCH – see Chapter 13 for implementation).

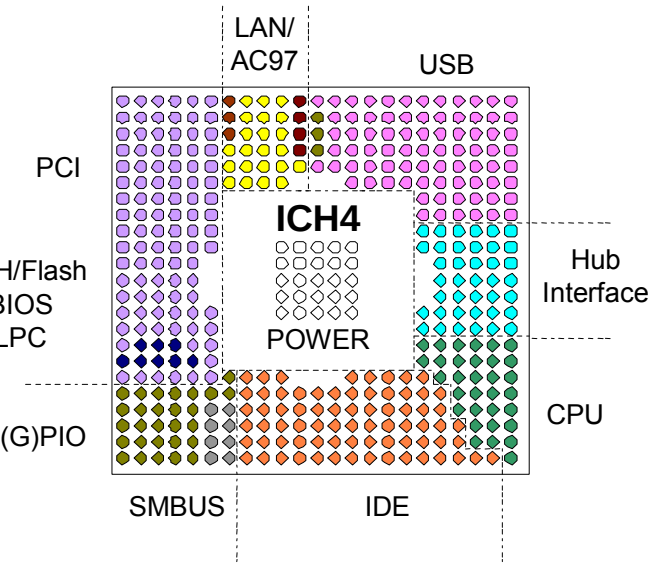
Figure 2-5. Layer Two Vias



The resulting rows of vias allow wide copper paths for power and ground. This fosters good power delivery and low impedance return paths for current to follow.

2.3 Intel® ICH4 Component Quadrant Layout

Figure 2-6. Intel® ICH4 Quadrant Layout (Top View)



3 Platform Stack-Up and Placement Overview

In this section, an example of an 845GE/845PE chipset platform component placement and stack-up is presented for a desktop system in µATX board form factor for DDR266/333 SDRAM.

3.1 General Design Considerations

This section describes motherboard layout and routing guidelines for 845GE/845PE chipset platforms. This section does not describe the functional aspects of any bus, or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e., 60 Ω ± 15%) is the "nominal" trace impedance for a 5-mil wide trace. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

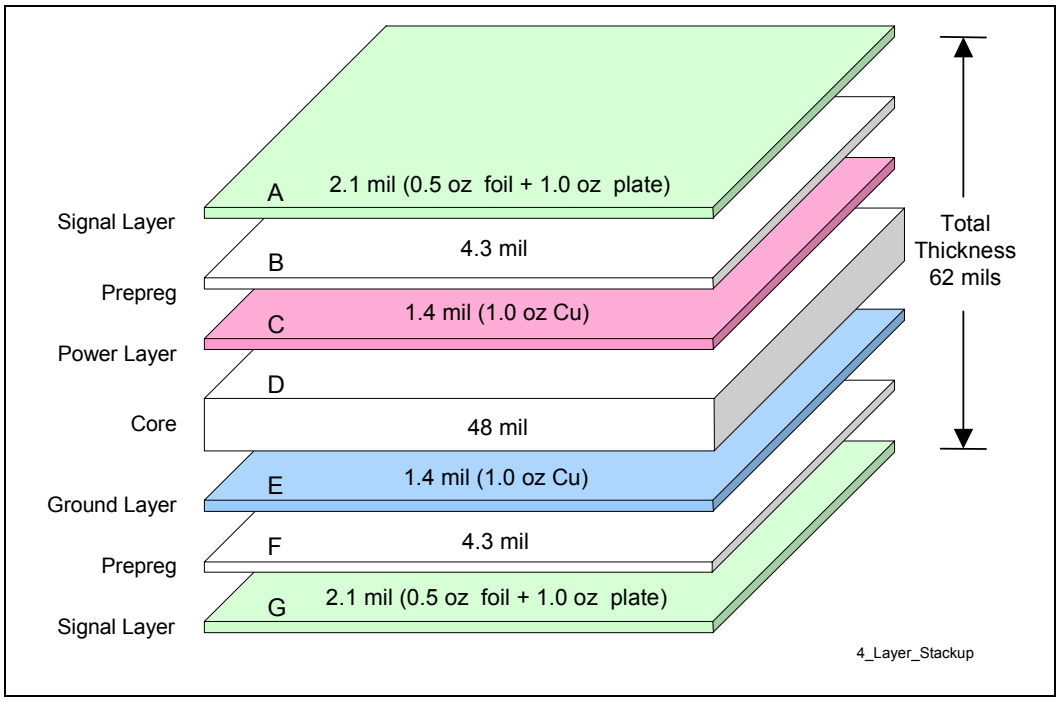
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

Additionally, these routing guidelines are created using a PCB stack-up similar to that illustrated in Figure 3-1.

3.2 Nominal 4-Layer Board Stack-Up

The 845GE/845PE chipset platform requires a board stack-up yielding a target board impedance of 60 Ω ± 15%. **Recommendations in this design guide are based on the following a 4-layer board stack-up:**

Figure 3-1. 4-layer PCB Stack-Up

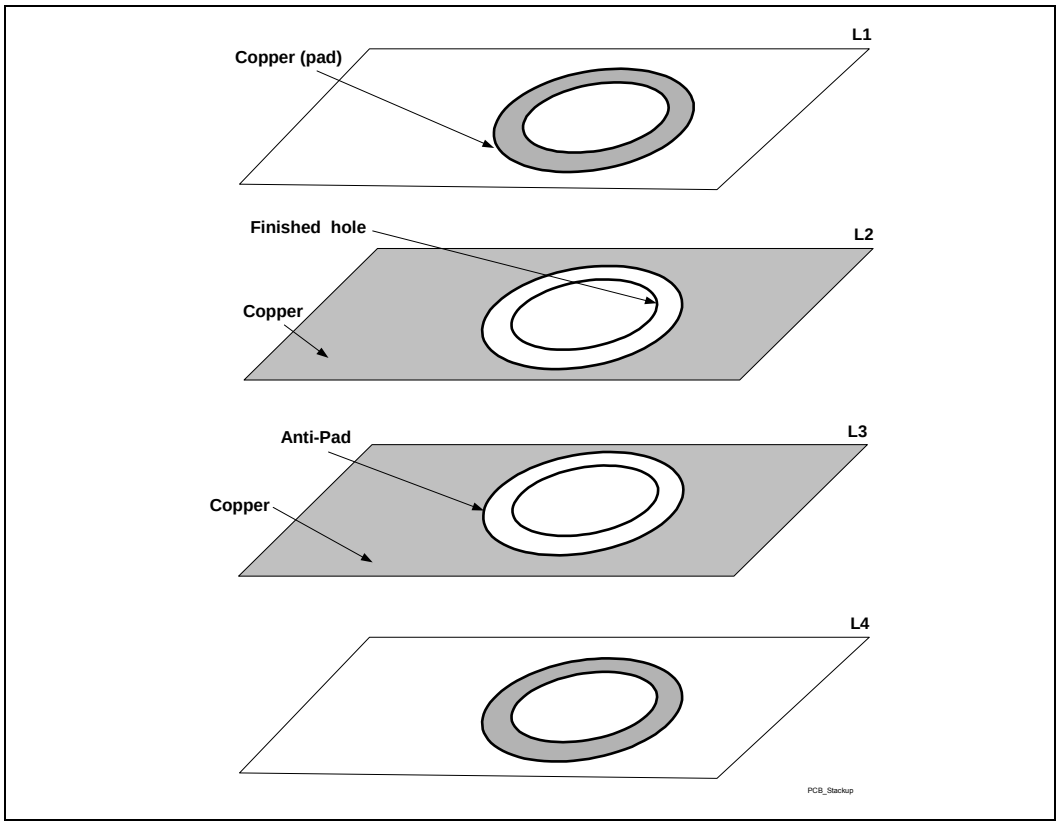


Description	Nominal Value	Tolerance	Comments
Board Impedance Z_0	60 Ω	± 15%	With nominal 5 mil trace width
Dielectric Thickness	4.3 mils	± 0.5 mils	1 x 2116 Pre-Preg
Micro-stripline Er	4.1	± 0.4	@ 100 MHz
Trace Width	5.0 mils	± 0.5 mils	Standard trace
Trace Thickness	2.1 mils	± 0.5 mils	0.5 oz foil + 1.0 oz plate
Soldermask Er	4.0	± 0.5	@ 100 MHz
Soldermask Thickness	1.0 mils	± 0.5 mils	From top of trace

3.2.1 PCB Technology Considerations

Intel has found that the following recommendation aids in the design of an 845GE/845PE chipset based platform. Simulations and reference platform are based on the following technology, and Intel recommends that designers adhere to these guidelines.

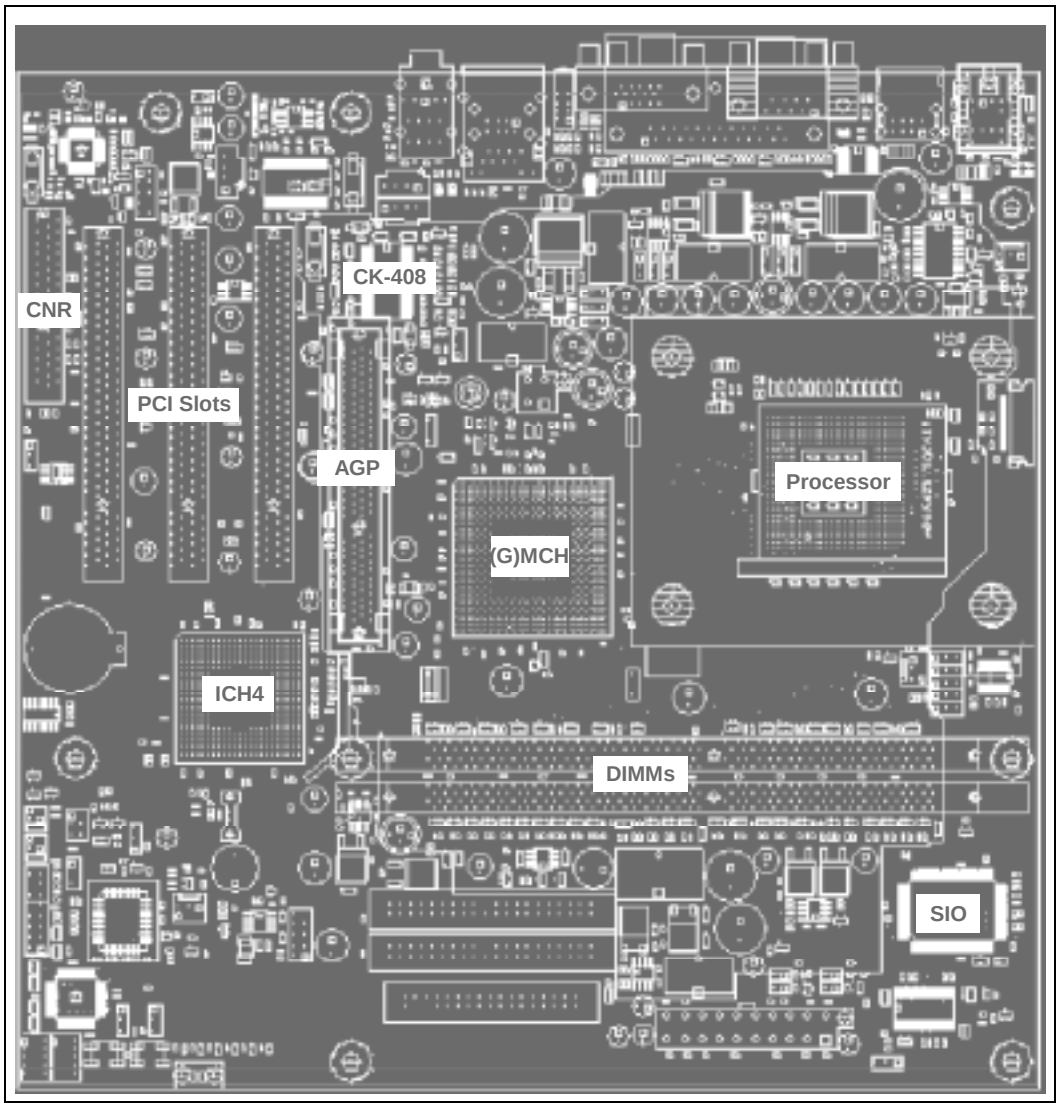
Figure 3-2. PCB Technologies – Stack-Up



Number of Layers	
Stack Up	4 Layer
Cu Thickness	0.5 oz Outer (before plating); 1oz inner
Final Board Thickness	62 mils (- 5mils / +8mils)
Material	Fiberglass made of FR4
Signal and Power Via Stack	
Via Pad	26 mils
Via Anti-Pad	40 mils
Via Finished Hole	14 mils

3.3 Platform Component Placement

Figure 3-3. Intel® 845GE/845PE Chipset Component Placement



4 Processor System Bus Guidelines

This section addresses layout recommendations for a Pentium 4 processor in the 478-pin package with a 400/533 MHz PSB configuration.

4.1 Processor System Bus Design Guidelines

Table 4-1 summarizes the layout recommendations for a Pentium 4 processor in the 478-pin package with a 400/533 MHz PSB configuration, and expands on specific design issues and recommendations.

Table 4-1. System Bus Routing Summary for the Processor

Parameter	Processor Routing Guidelines
Line to line spacing	Data and common clock system bus must be routed at 7-mil wide traces and with 13 mils spacing.
Breakout Guidelines (processor and (G)MCH)	7 mil wide with 5-mil spacing for a maximum of 250 mils from the component ball.
Group Spacing	Non Clock Spacing = 20 mils to any other signal
Data Line lengths (agent to agent spacing)	2” – 8” from pin-to-pin Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Signals should be referenced to VSS.
DSTBN/P[3:0]#	DSTBN/P# should be routed to the same length as their corresponding data signals' mean pad-to-pad length ± 25 mils. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (VSS) and the layers are all of the same configuration (all stripline or all microstrip). A data strobe and its complement should be routed within ± 25 mils of the same pad-to-pad length. If one strobe switches layers, its complement must switch layers in the same manner. DSTBN/P# should be referenced to VSS.
Address line lengths (agent to agent spacing) ADSTB[1:0]#	2” – 10” from pin-to-pin Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (VSS) and the layers are all of the same configuration (all stripline or all microstrip).

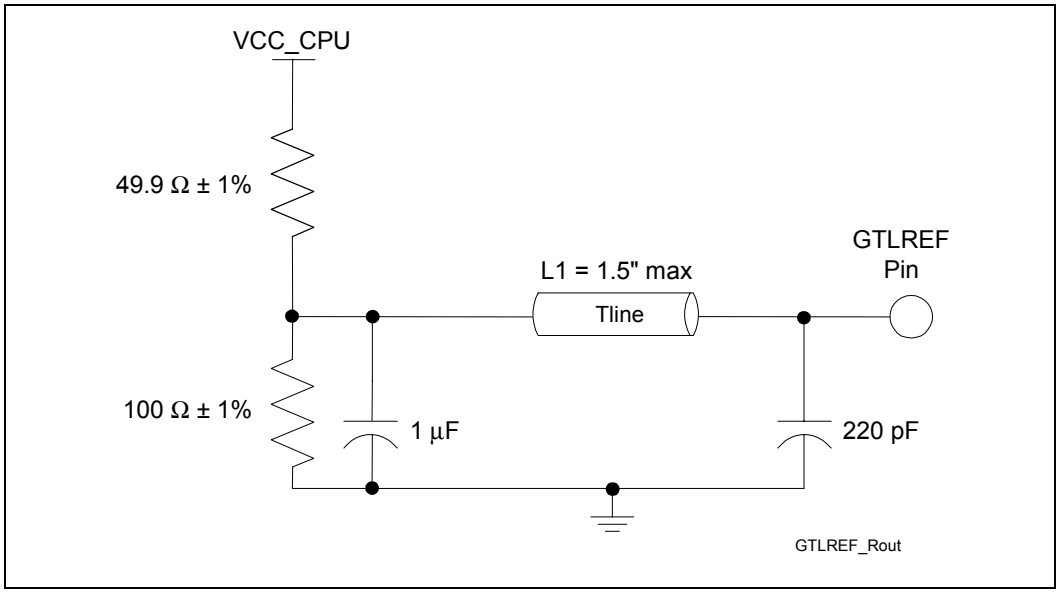
Parameter	Processor Routing Guidelines
Common Clock Trace Lengths	• 3.0” - 10” from pin-to-pin Note: No length compensation is necessary.
Topology	Point-to-Point (chipset to processor).
Routing priorities	All signals should be referenced to VSS. Ideally, layer changes should not occur for any signals. If a layer change must occur, reference plane must be VSS and the layers must all be of the same configuration (all stripline or all microstrip for example). The Data Bus must be routed first, then the address bus and then common clock.
Clock keep out zones	Refer to Table 12-3 Host Clock Routing Guidelines
Trace Impedance	50 Ω ± 15%
Maximum via count per signal	4 (Avoid layer change as much as possible.) No layer change is recommended.

Note: Refer to the *Intel® 845GE/845PE Chipset Datasheet* for (G)MCH package dimensions, and refer to the *Intel® Pentium® 4 Processor in the 478-pin package Signal Integrity Models* for processor package dimensions.

4.1.1 GTLREF Layout and Routing Recommendations

There are four AGTL+ GTLREF pins on the processor that are used to set the reference voltage level for the AGTL+ signals (GTLREF). Because all of these pins are connected inside the processor package, the GTLREF voltage must be supplied to only one of the four pins.

Figure 4-1. GTLREF Routing



- The processor must have one dedicated voltage divider.
- Decouple the voltage divider with a 1 µF capacitor.
- Keep the voltage divider within 1.5 inches of the GTLREF pin.
- Decouple the pin with a high-frequency capacitor (such as a 220 pF 603) as close to the pin as possible.
- Keep signal routing at least 10 mils separated from the GTLREF routes. Use a minimum 7-mil trace for routing.
- Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the front side bus signals.)

4.1.2 HVREF, HSWNG, HRCOMP Layout and Routing Recommendations at the Intel® (G)MCH

The HVREF signals must be tied to a resistor divider network that supplies 2/3*VCC_CPU. Use one 49.9 Ω 1% resistor to the VCC_CPU plane and one 100 Ω 1% resistor to ground for the divider. Decouple with one 0.1 µF capacitor at the (G)MCH. The trace to the voltage divider should be routed at a maximum of 3 inches at 12-mils width. Keep this trace at a minimum of 10 mils away from other signals.

The HSWNG signals must be tied to a resistor divider network that supplies 1/3*VCC_CPU. Use one 300 Ω 1% resistor to the VCC_CPU plane, and one 150 Ω 1% resistor to ground for the divider. Decouple with one 0.01 µF capacitor at the (G)MCH. The trace to the voltage divider should be routed at a maximum of 3 inches with 12-mils width. Keep this trace at a minimum of 10 mils away from other signals.

Each HRCOMP signal must be tied to ground through a 24.9 Ω 1% resistor. The trace to each resistor should be routed a maximum of 0.5 inch with 10-mils width. Keep each trace a minimum of 7 mils away from other signals.

4.2 Processor Configuration

4.2.1 Intel® Pentium® 4 Processor Configuration

This section provides more details for routing Pentium 4 processor-based systems. Both recommendations and considerations are presented.

For proper operation of the processor and the 845GE/845PE chipset, it is necessary that the system designer meet the timing and voltage specifications of each component. The following recommendations are Intel guidelines based on extensive simulation and experimentation that make design assumptions that may be different than an OEM's assumptions. The most accurate way to understand the signal integrity and timing of the system bus in a platform is by performing a comprehensive simulation analysis. It is conceivable that adjustments to trace impedance, line length, termination impedance, board stack-up, and other parameters can be made that improve system performance.

Refer to the *Intel® Pentium® 4 Processor in the 478-pin package Datasheet* for a system bus signal list, signal types and definitions.

4.2.2 Topology and Routing

Table 4-2. Source Synchronous Signal Groups and the Associated Strobes

Signals	Associated Strobe
REQ[4:0]#, A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#, DINV_0#	DSTBP0#, DSTBN0#
D[31:16]#, DINV_1#	DSTBP1#, DSTBN1#
D[47:32]#, DINV_2#	DSTBP2#, DSTBN2#
D[63:48]#, DINV_3#	DSTBP3#, DSTBN3#

Note: DINV_[3:0] pins on the (G)MCH are referred to as DBI[3:0] on the processor.

Design recommendations will be presented first followed by design considerations

4.2.2.1 Design Recommendations

The following are the design recommendations for the data, address, strobes, and common clock signals. Based on the illustration shown in Figure 4-2, the data, address, strobe and common clock should be routed 7 mils with a 13-mil spacing. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate.

Data

The pin-to-pin distance for the data signals from the processor to the chipset should be between 2.0 inches to 8 inches (i.e., 2.0 inches < L1 < 8 inches). Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. As a result, additional trace is added to some data nets on the system board for all trace lengths within the same data group to be the same length (± 100 mils) from the pad of the processor to the pad of the chipset. This length compensation minimizes the source synchronous skew that exists on the system bus. Without the length compensation, the flight times between a data signal and its strobe will be different, which results in an inequity between the setup and hold times. Data signals may change layers if the reference plane remains VSS.

Equation 1. Calculation to Determine Package Delta Addition to Motherboard Length

$$\text{delta}_{\text{net,strobe}} = (\text{cpu\_pkglen}_{\text{net}} - \text{cpu\_pkglen}_{\text{strobe*}}) + (\text{cs\_pkglen}_{\text{net}} - \text{cs\_pkglen}_{\text{strobe}})$$

NOTE: * Strobe package length is the average of the strobe pair.

Refer to Section 4.8 in this design guide for package lengths.

Address

Address signals follow the same rules as data signals, except they should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. Address signals may change layers if the reference plane remains VSS.

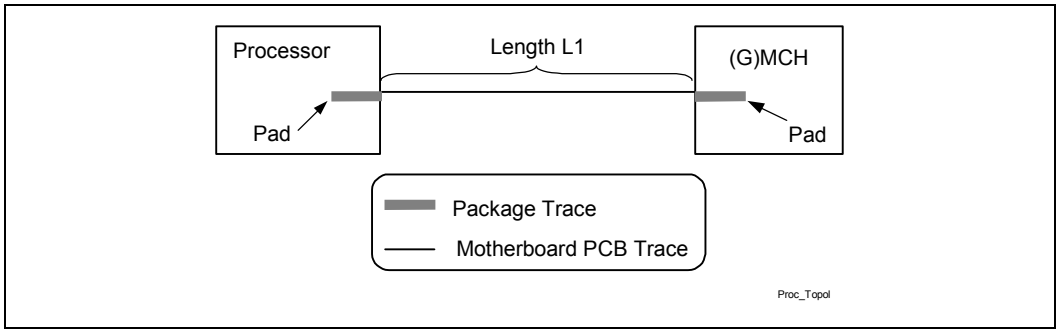
Data Strobes

A strobe and its complement should be routed to a length equal to their corresponding data group's mean pad-to-pad length ± 25 mils. This causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. A strobe and its complement (xSTBp/n#) should be routed to ± 25 mils of the same length. It is recommended that skew be simulated to determine the length that best centers the strobe for a given system.

Common Clock

Common clock signals should be routed to a minimum pin-to-pin motherboard length of 3 inches, and a maximum motherboard length of 10 inches.

Figure 4-2. Processor Topology



4.3 Routing Guidelines for Asynchronous GTL+ and Other Signals

This section describes layout recommendations for signals other than data, strobe and address. Table 4-3 lists the signals covered in this section.

Table 4-3 Miscellaneous Signals (Signals that are not Data, Address, or Strobe)

Signal Name	Type	Direction	Topology	Driven by
A20M#	Asynchronous GTL+	I	2A	Intel® ICH4
BREQ0#	AGTL+	I/O	4	Processor
COMP[1:0]	Analog	I	5	
FERR#	Asynchronous GTL+ Open Drain	O	1A	Processor
IGNNE#	Asynchronous GTL+	I	2A	ICH4
INIT#	Asynchronous GTL+	I	2B	ICH4
LINT0/INTR LINT1/NMI	Asynchronous GTL+	I	2A	ICH4
PROCHOT#	Asynchronous GTL+ Open Drain	O	1B	Processor
PWRGOOD	Other	I	2C	ICH4
RESET#	AGTL+ Open Drain	I	4	(G)MCH
SLP#	Asynchronous GTL+	I	2A	ICH 4
SMI#	Asynchronous GTL+	I	2A	ICH4
STPCLK#	Asynchronous GTL+	I	2A	ICH4
THERMTRIP#	Asynchronous GTL+ Open Drain	O	1C	Processor
VCCA	Power	I	3	External logic
VCCIOPLL	Power	I	3	External logic
VCC_SENSE	Other	O		Processor
VID[4:0]	Open Drain 3.3 V Tolerant	O	8	Processor
VSSA	Power	I	3	Ground
VSS_SENSE	Other	O		Processor
THERMDA/THERMDC	Other	I/O	6	External logic
TESTHI	Other	I/O	7	External logic

All signals must meet the AC and DC specifications as documented in the *Intel® Pentium® 4 Processor in the 478-pin package Datasheet*.

4.3.1 Topologies

The following sections describe the topologies and layout recommendations for the miscellaneous signals.

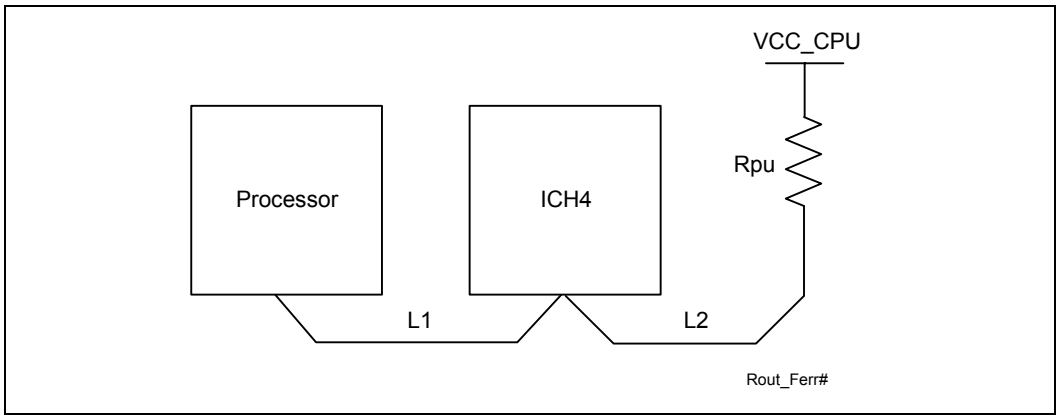
4.3.1.1 Topology 1A: Asynchronous GTL+ Signals Driven by the Processor: FERR#

FERR# should adhere to the following routing and layout recommendations:

Table 4-4. Layout Recommendations for FERR# Signal — Topology 1A

Trace Z_0	Trace Spacing	L1	L2	Rpu
60 Ω	7 mil	1”-12"	3" max	62 ± 5% Ω

Figure 4-3. Routing Illustration for FERR#



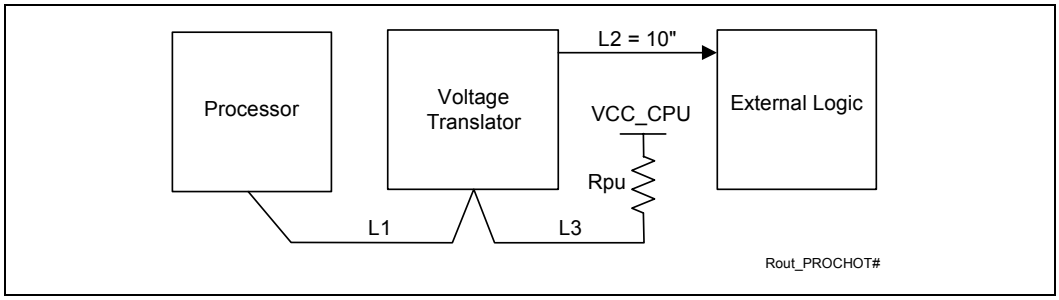
4.3.1.2 Topology 1B: Asynchronous GTL+ Signals Driven by the Processor: PROCHOT#

PROCHOT# should adhere to the following routing and layout recommendations. If PROCHOT# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

Table 4-5. Layout Recommendations for PROCHOT# Signal — Topology 1B

Trace Z_0	Trace Spacing	L1	L2	L3	Rpu
60 Ω	7 mil	1”-17"	10" max	3" max	62 ± 5% Ω

Figure 4-4. Routing Illustration for PROCHOT#



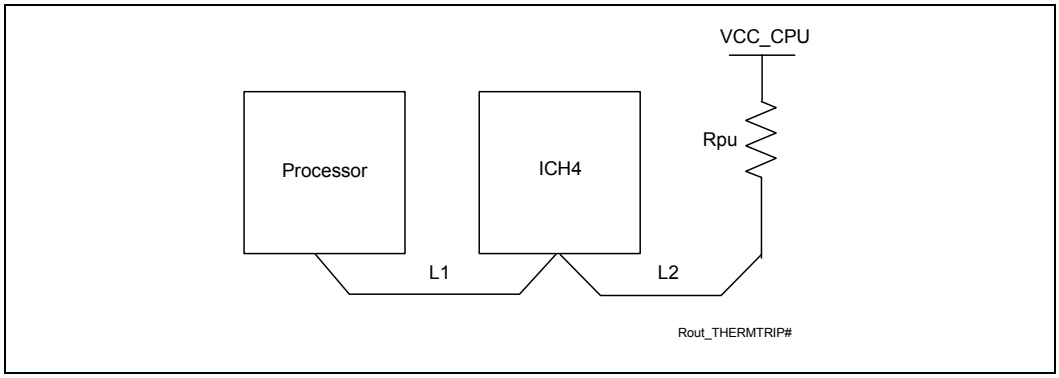
4.3.1.3 Topology 1C: Asynchronous GTL+ Signals Driven by the Processor: THERMTRIP#

THERMTRIP# should adhere to the following routing and layout recommendations. If THERMTRIP# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

Table 4-6. Layout Recommendations for THERMTRIP# Signal — Topology 1C

Trace Z_0	Trace Spacing	L1	L2	Rpu
60 Ω	7 mil	1”-12"	3" max	62 ± 5% Ω

Figure 4-5. Routing Illustration for THERMTRIP#



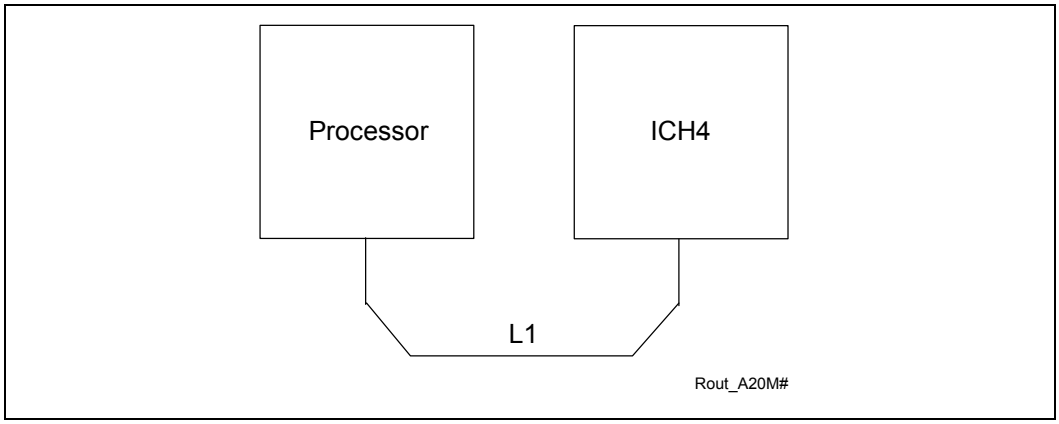
4.3.1.4 Topology 2A: Asynchronous GTL+ Signals Driven by the Intel® ICH4: A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#

These signals should adhere to the following routing and layout recommendations. Figure 4-6 shows the recommended topology.

Table 4-7. Layout Recommendations for Miscellaneous Signals — Topology 2A

Trace Z_0	Trace Spacing	L1	Rpu
60 Ω	7 mil	17” max	None

Figure 4-6. Routing Illustration for A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#

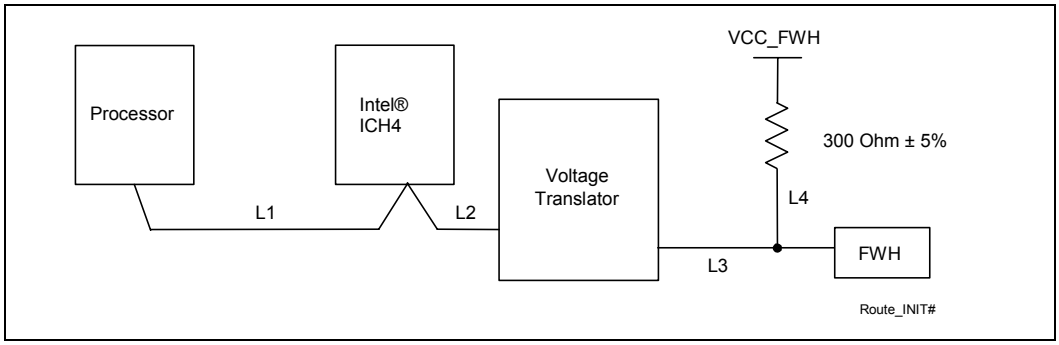


4.3.1.5 Topology 2B: INIT#

Table 4-8. Layout Recommendations for INIT# — Topology 2B

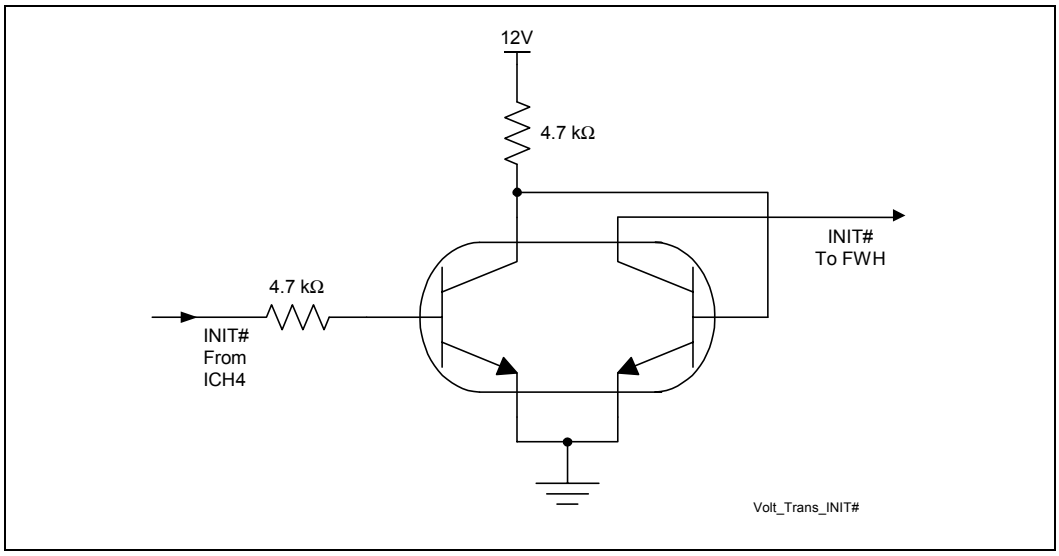
Trace Z_0	Trace Spacing	L1	L2	L3	L4	Rpu
60 Ω	7mil	17” max	2” max	10” max	3” max	None

Figure 4-7. Routing Illustration for INIT#



Level shifting is required for the INIT# signal to the FWH to meet the input logic levels of the FWH. Figure 4-8 illustrates one method of implementing this.

Figure 4-8. Voltage Translation of INIT#



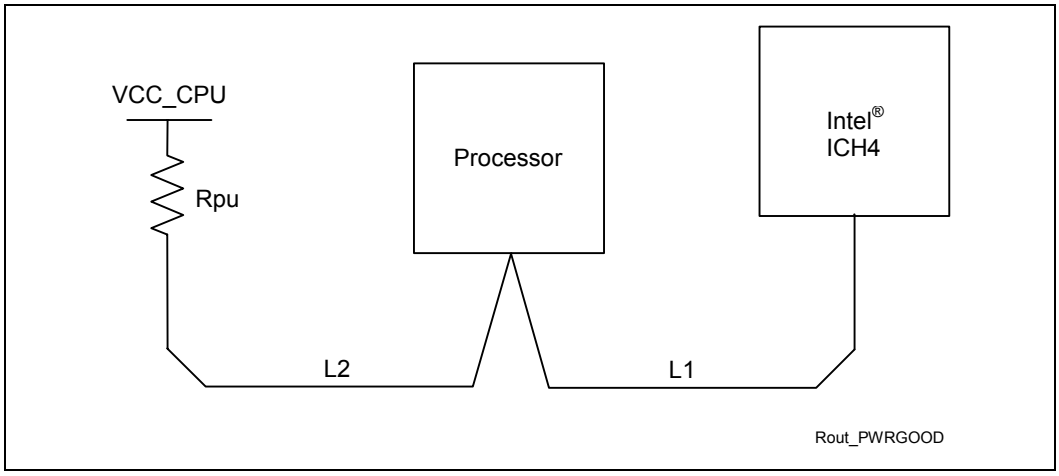
4.3.1.6 Topology 2C: Miscellaneous Signal Driven by the Intel® ICH4 Open Drain: PWRGOOD

This signal should adhere to the following routing and layout recommendations. Figure 4-9 illustrates the recommended topology.

Table 4-9. Layout Recommendations for Miscellaneous Signals — Topology 2B

Trace Zo	Trace Spacing	L1	L2	Rpu
60 Ω	7 mil	1"-12"	3" max	300 Ω ± 5%

Figure 4-9. Routing Illustration for PWRGOOD



4.3.1.7 Topology 3: VCCIOPLL, VCCA, and VSSA

Refer to Section 4.7.2.1 (Filter Specifications for VCCA, VCCIOPLL, and VSSA) of this design guide for VCCIOPLL, VCCA, and VSSA information.

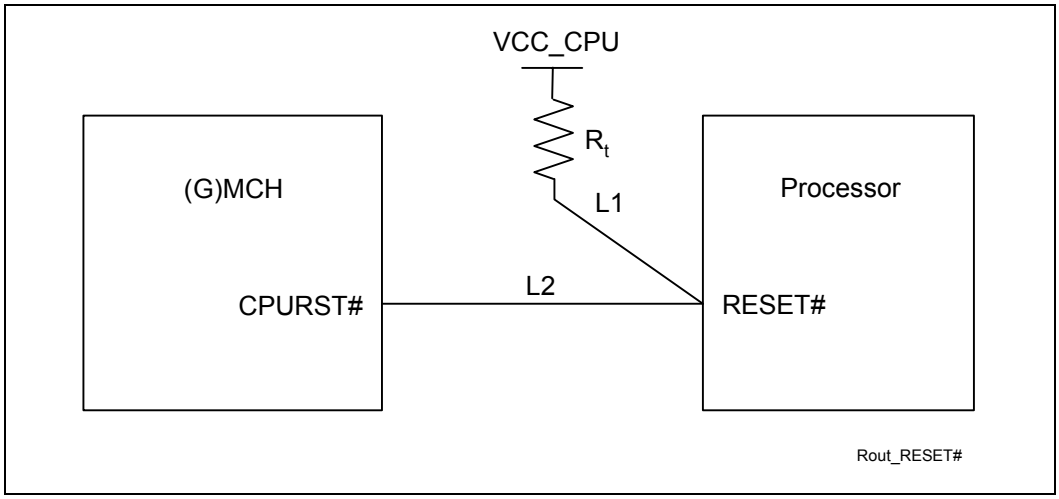
4.3.1.8 Topology 4: BREQ0# and RESET#

Because the processor does not have on-die termination on the BREQ0# and RESET# signals, it is necessary to terminate using discrete components on the system board. Connect the signals between the components as shown in Figure 4-10. Routing Illustration for BREQ0# and RESET# is listed in the following table. The (G)MCH has on-die termination and thus it is necessary to terminate only at the processor end. The value of Rt should be 51 Ω ± 5% for RESET#. The value of Rt should be 150 Ω to 220 Ω ± 5% for BREQ0#.

Table 4-10. Layout Recommendations for BREQ0# and RESET# — Topology 4

Signal	Rt	L1	L2
BREQ0#	150 Ω to 220 Ω	≤ 1" – 2"	3" – 10"
RESET#	51 Ω	≤ 1" – 2"	3" – 10"

Figure 4-10. Routing Illustration for RESET#



NOTE: BREQ0# is similarly terminated.

4.3.1.9 Topology 5: COMP[1:0] Signals

Terminate the COMP[1:0] pins to ground through a 51 Ω ± 1% resistor as close as possible to the pin. Do not wire COMP pins together; connect each pin to its own termination resistor. RCOMP value can be adjusted to set external drive strength of I/O and to control the edge rate.

4.3.1.10 Topology 6: THERMDA/THERMDC Routing Guidelines

The processor incorporates an on-die thermal diode. THERMDA (diode anode) and THERMDC (diode cathode) pins on the processor can be connected to a thermal sensor located on the system board to monitor the die temperature of the Processor for thermal management/long term die temperature change monitoring purpose. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Because the thermal diode is used to measure a very small voltage from the remote sensor, care must be taken to minimize noise induced at the sensor inputs. Below are some guidelines:

- Remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4 to 8 inches away as long as the worst noise sources such as clock generators, data buses, address buses, etc., are avoided.
- Route the THERMDA and THERMDC lines in parallel and close together with ground guards enclosed.
- Use wide tracks to reduce inductance and noise pickup that may be introduced by narrow ones. A width of 10 mils and spacing of 10 mils is recommended.

4.3.1.11 Topology 7: TESTHI and RESERVED Pins

The TESTHI pins should be tied to the processor VCC using a matched resistor, where a matched resistor has a resistance value within ± 20% of the impedance of the board transmission line traces. For example, if the trace impedance is 50 Ω, then a value between 40 Ω and 60 Ω is required.

The TESTHI pins may use individual pull-up resistors or be grouped together as detailed below. A matched resistor should be used for each group.

- TESTHI[1:0]
- TESTHI[5:2]
- TESTHI[10:8]
- TESTHI[12:11]

Additionally, if the ITPCLKOUT[1:0] pins are not used then they may be connected individually to VCC using matched resistors or grouped with TESTHI[5:2] with a single matched resistor. If they are being used, individual termination with 1 kΩ resistors is acceptable. Tying ITPCLKOUT[1:0] directly to VCC or sharing a pull-up resistor to VCC, will prevent use of debug interposers. This implementation is strongly discouraged for system boards that do not implement an onboard debug port.

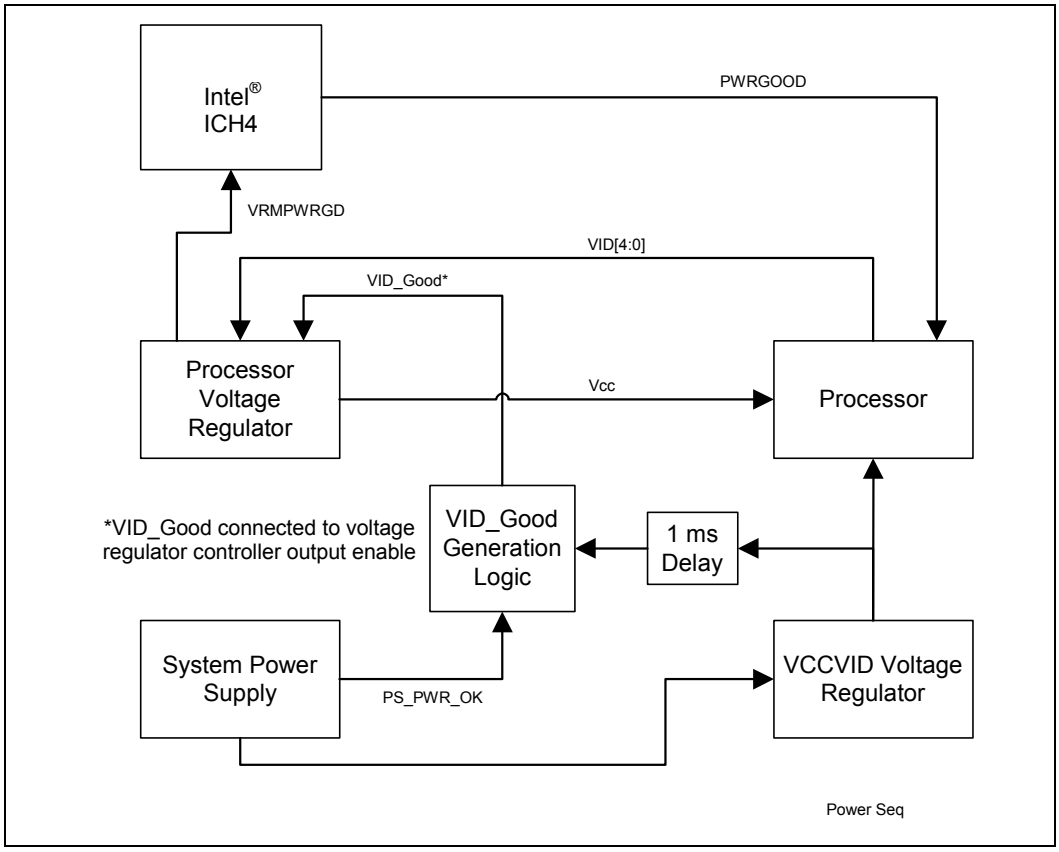
As an alternative, group 2 (TESTHI[5:2]), and the ITPCLKOUT[1:0] pins may be tied directly to the processor VCC. This has no impact on system functionality. TESTHI0 and TESTHI12 may also be tied directly to processor VCC if resistor termination is a problem, but matched resistor termination is recommended. In the case of the ITPCLKOUT[1:0], direct tie to VCC is strongly discouraged for system boards that do not implement an onboard debug port.

Reserved Pins on the (G)MCH and on the processor should be left as No Connect unless otherwise specified.

4.3.1.12 Topology 8: Processor Voltage Regulator Sequencing Requirements

The processor requires a 1.2 V supply to the VCCVID pins to support the on-die VID generation circuitry. A linear regulator is recommended to generate this voltage. The on-die VID generation circuitry has some power sequencing requirements. Figure 4-11 shows a block diagram of a power sequencing implementation.

Figure 4-11. Power Sequencing Block Diagram



4.3.1.13 Topology 9: PSB Frequency Select

The BSEL circuit determines the Processor System Bus (PSB) frequency. This circuit should be implemented as described in this section.

Figure 4-12. PSB Frequency Select Circuitry

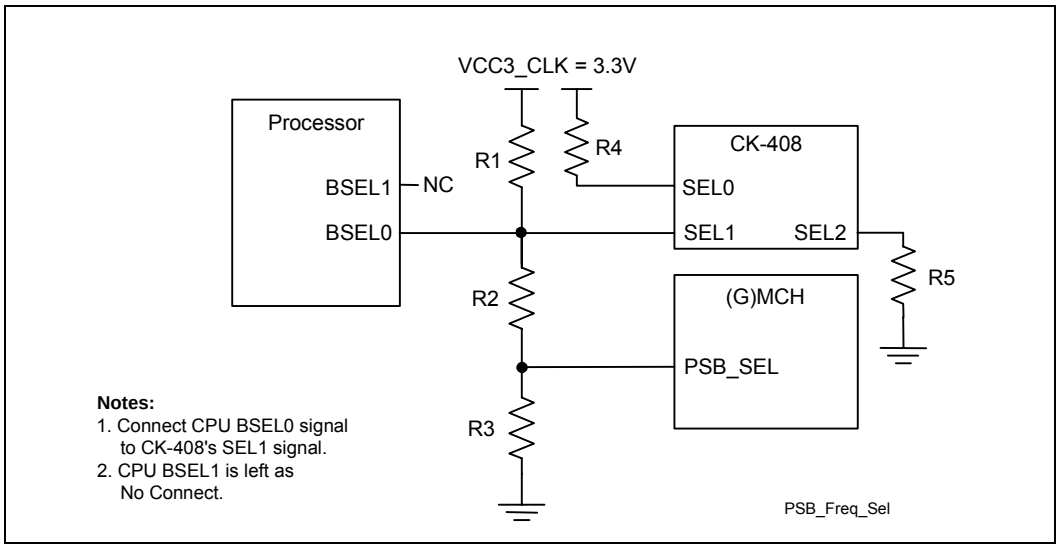


Table 4-11. PSB Frequency Select Circuit Resistor Values

Resistor	Value
R1	1.5 kΩ
R2	8.2 kΩ
R3	8.2 kΩ
R4	1 kΩ
R5	> 470 Ω

Table 4-12. Frequency Select Settings

SEL [2:0]	CK408 Speed	BSEL0	Processor
001	100 MHz	L	400 MHz
011	133 MHz	Hi-Z	533 MHz

Do not exceed the max current rating for the BSEL. Refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet* for the max current specifications.

4.4 Additional Processor Design Considerations

This section documents system design considerations not addressed in previous sections.

4.4.1 Retention Mechanism Placement and Keep-Outs

The retention mechanism requires a keep out zone, for a limited component height area under the retention mechanism as shown in the following figures. The figures show the relationship between the retention mechanism mounting holes and pin one of the socket. In addition it also documents the keep-outs.

The retention holes should be a non-plated hole. The retention holes should have a primary and secondary side route keep-out area of 0.409 inch diameter.

For heatsink volumetric information refer to the *Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines*.

Figure 4-13. Retention Mechanism Keep-Out Drawing 1

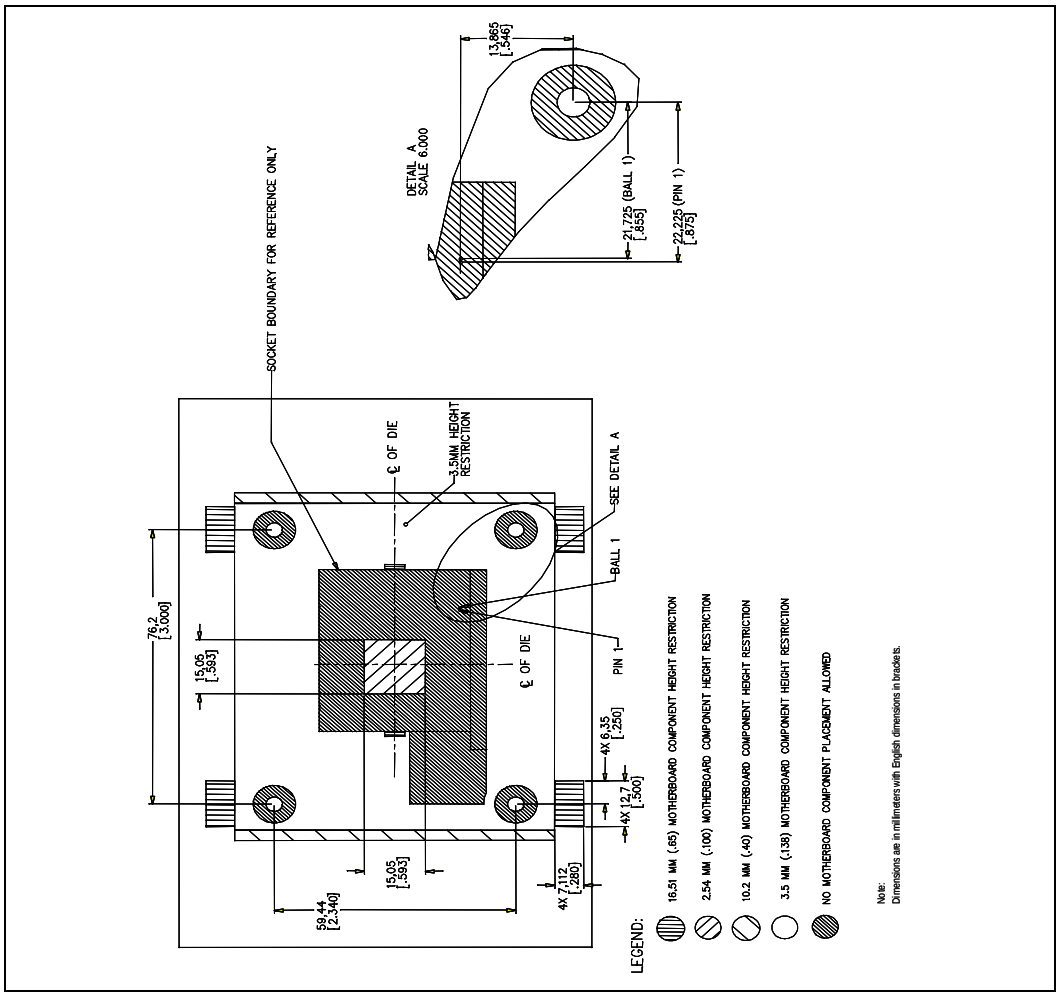
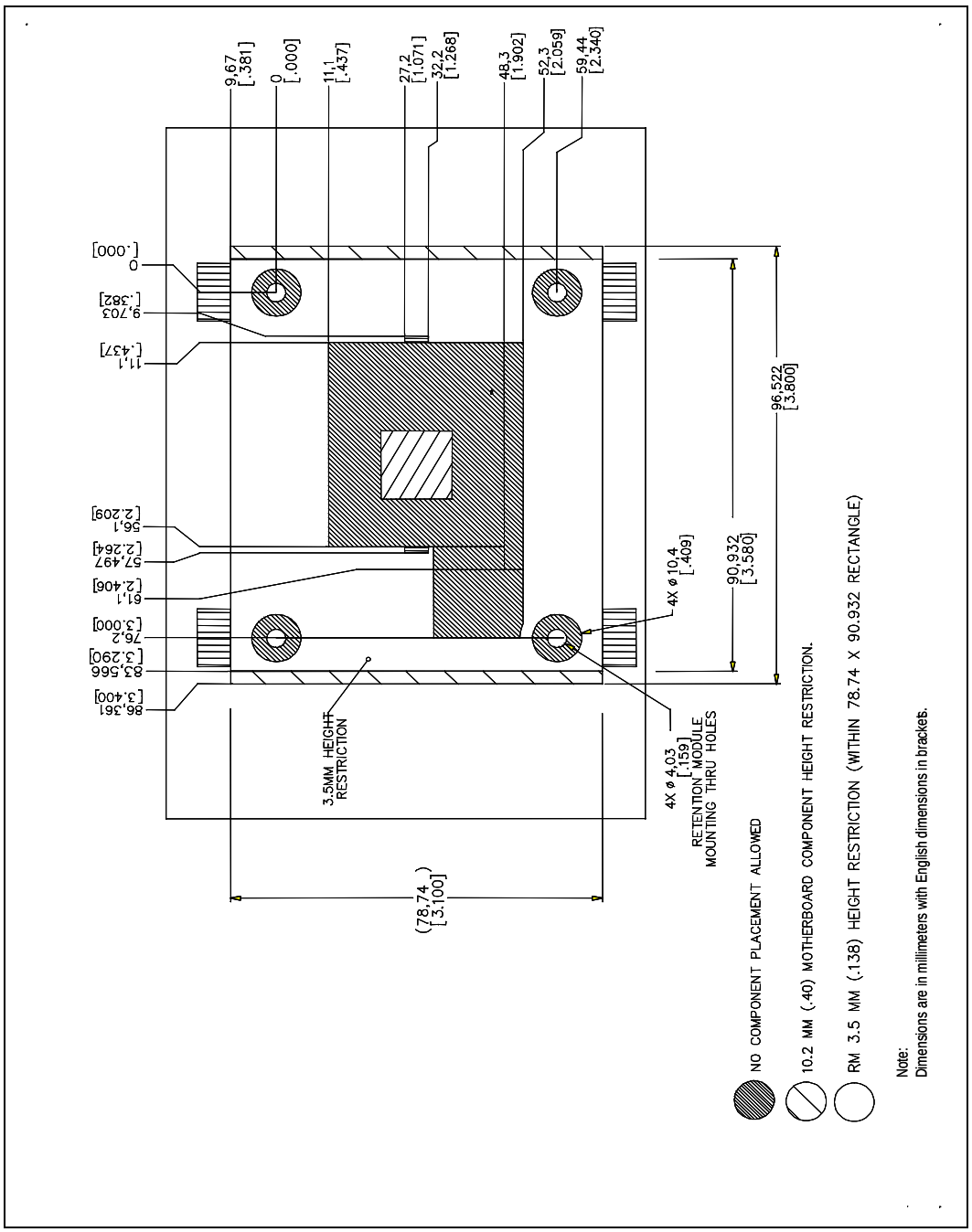


Figure 4-14. Retention Mechanism Keep-Out Drawing 2



4.4.2 Power Header for Active Cooling Solutions

The reference-design heatsink includes an integrated fan. The recommended connector for the active cooling solution is a Walden /Molex 22-01-3037, AMP 643815-3 or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. The fan connector pinout is described in Table 4-13.

Table 4-13. Reference Solution Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	No Connect

The Intel boxed processor heatsink includes an integrated fan. The recommended connector for the active cooling solution is a Walden /Molex 22-23-2037, AMP 640456-3 or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. The fan connector pinout is described in Table 4-14.

Table 4-14. Boxed Processor Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	SENSE

The fan heatsink outputs a SENSE signal, which is an open-collector output that pulses at a rate of two pulses per fan revolution. The system board requires a pull-up resistor to provide the appropriate VOH level to match the fan speed monitor. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 should be tied to GND.

For more information on boxed processor requirements, refer to the *Intel® Pentium® 4 Processor in the 478-pin Package Datasheet* or the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on .13 Micron Process Datasheet.*

4.5 ITP Debug Port Routing Guidelines

Refer to the latest revision of the *Intel® Pentium® 4 Processor in the 478-pin Package Debug Port Design Guide* for details on the implementation of the debug port.

4.5.1 Debug Tools Specifications

4.5.1.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the Pentium 4 processor in the 478-pin package system. Tektronix and Agilent should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of the Pentium 4 processor in the 478-pin package system, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a Pentium 4 processor in the 478-pin package system that can make use of an LAI: mechanical and electrical.

4.5.1.2 Mechanical Considerations

The LAI is installed between the processor socket and the Pentium 4 processor in the 478-pin package. The LAI pins plug into the socket, while the Pentium 4 processor in the 478-pin package pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Pentium 4 processor in the 478-pin package and a logic analyzer. The maximum volume occupied by the LAI, known as the keep-out volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keep-out volume remains unobstructed inside the system. Note that it is possible that the keep-out volume reserved for the LAI may include space normally occupied by the Pentium 4 processor in the 478-pin package heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

4.5.1.3 Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

4.6 Intel® Pentium® 4 Processor in the 478-pin Package Power Distribution Guidelines

See Chapter 13 for general platform power delivery guidelines.

4.6.1 Power Requirements

Intel recommends using an *Intel® Pentium® 4 Processor VR Down Design Guidelines*-compliant regulator for the processor system board designs that meets FMB2 requirements (refer to Section 4.7.1 for airflow requirements). An *Intel® Pentium® 4 Processor VR Down Design Guidelines* -compliant regulator may be integrated as part of the system board or on a module. The system board designer should properly place high-frequency and bulk-decoupling capacitors as needed between the voltage regulator and the processor to ensure voltage fluctuations remain within the *Intel® Pentium® 4 Processor in the 478-pin package Datasheet* and the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on .13 Micron Process Datasheet*. See Section 4.6.2 for recommendations on the amount of decoupling needed.

Specifications for the processor voltage are contained in the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on .13 Micron Process Datasheet* and the *Intel® Pentium® 4 Processor in the 478-Pin Package Datasheet*. These specifications are for the processor die. For guidance on correlating the die specifications to socket level measurements, refer to the socket loadlines in the *Intel® Pentium® 4 Processor VR Down Design Guidelines*.

The voltage tolerance of the loadlines contained in the above mentioned documents help the system designer to achieve a flexible motherboard design solution for many different frequencies of the processor. Failure to meet the load line requirements when modeling the system power delivery may result in a system that is not upgradeable. For maximum flexibility in system design, it is recommended to use an FMB2 compliant regulator. Two example regulator designs that meet FMB2 specifications are described in this section. Each of these designs has benefits, as well as drawbacks.

The processor requires local regulation due to its higher current requirements, and to maintain power supply tolerance. For example, an on-board DC-to-DC converter converts a higher DC voltage to a lower level using either a linear or a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses (I x R). More importantly however, a discrete regulator regulates the voltage locally, which minimizes DC line losses by reducing motherboard resistance on the processor voltage. Figure 4-15 shows an example of the placement of the local voltage regulation circuitry.

In this section, North and South are used to describe a specific side of the socket based on the placement of the customer reference board shown in Figure 3-3. North refers to the side of the processor closest to the back panel and South refers to the side of the processor closest to the system memory.

Figure 4-15. Four-Phase VR Component Placement

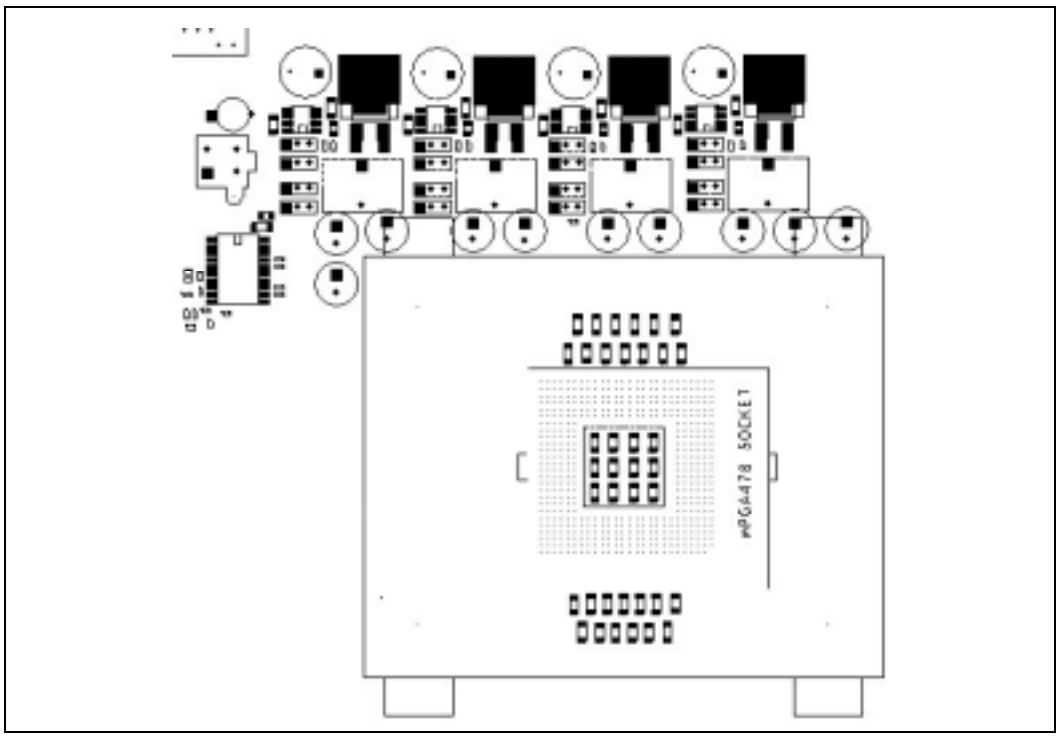
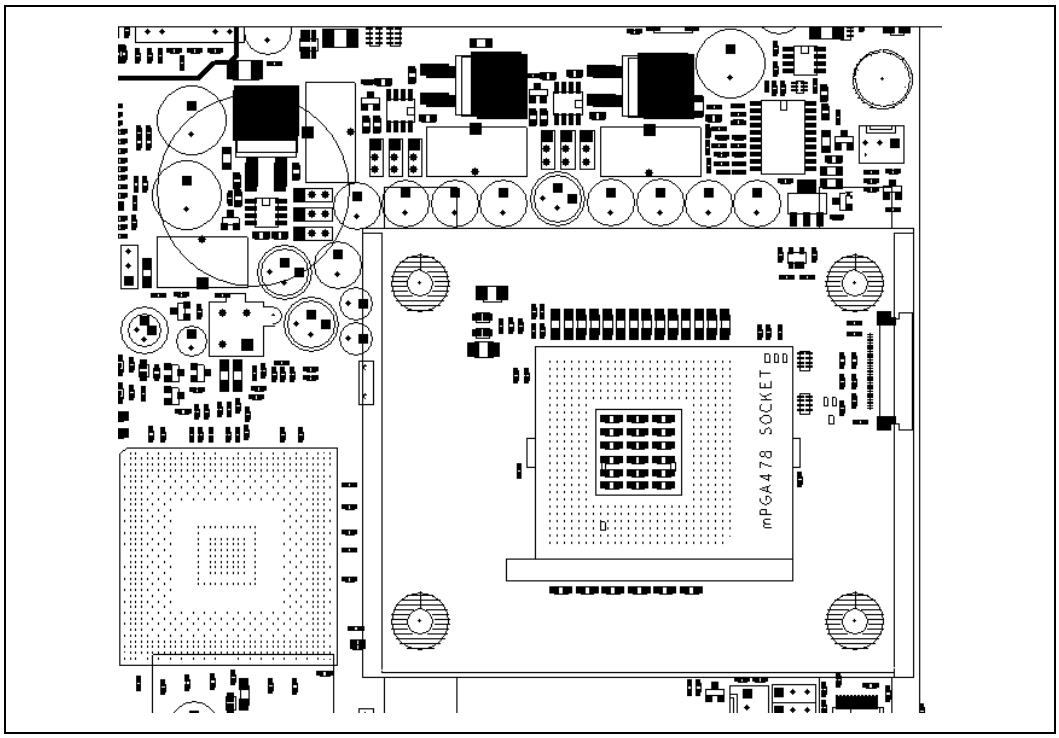


Figure 4-16. Three-Phase VR Component Placement



4.6.2 Decoupling Requirements

For the processor voltage regulator circuitry to meet the transient specifications of the processor, proper bulk and high-frequency decoupling is required. The decoupling requirements for the processor power delivery in this case are described in Table 4-15:

Table 4-15. Four Phase Decoupling Requirement

Capacitance	ESR (Each)	ESL (Each)	Ripple Current Rating (Each)	Notes
10 OSCONs*, 560 µF	9.28 mΩ, max	6.4 nH, max	4.080 A	1
38 1206 package, 10 µF	3.5 mΩ, typ	1.15 nH, typ		1

NOTES:
1. The ESR, ESL and ripple current values in this table are based on the values used in power delivery simulation by Intel and they are not vendor specifications.

Table 4-16. Three-Phase Decoupling Requirements

Capacitance	ESR (Each)	ESL (Each)	Ripple Current Rating (Each)	Notes
9 OSCONs*, 560 µF	9.28 mΩ, max	6.4 nH, max	4.080 A	1
3 Al Electrolytic, 3300 µF	12 mΩ	5 nH		1
24 0805 package, 10 µF				1,2
14 1206 package, 10 µF	3.5 mΩ, typ	1.15 nH, typ		1,2

NOTES:
1. The ESR, ESL and ripple current values in this table are based on the values used in power delivery simulation by Intel and they are not vendor specifications.
2. If only 1206s are used, 38 are needed.

The decoupling should be placed as close as possible to the processor power pins. Table 4-17 and Table 4-18 and Figure 4-17 and Figure 4-18 describe and illustrate the recommended placement.

Table 4-17. Four-Phase Decoupling Locations

Type	Number	Location
560 µF OSCONs*	10	North side of the processor as close as possible to the keep-out area for the retention mechanism
1206 package, 10 µF	13	North side of the processor as close as possible to the processor socket
1206 package, 10 µF	12	Inside the processor socket cavity
1206 package, 10 µF	13	South side of the processor as close as possible to the processor socket

Table 4-18. Three-Phase Decoupling Locations

Type	Number	Location
560 µF OSCONs*	9	North side of the processor as close as possible to the keep-out area for the retention mechanism
Al Electrolytic, 3300 µF	3	North side of the processor as close as possible to the keep-out area for the retention mechanism
1206 package, 10 µF	14	North side of the processor as close as possible to the processor socket
0805 package, 10 µF	18	Inside the processor socket cavity
0805 package, 10 µF	6	South side of the processor as close as possible to the processor socket

NOTE: If (38) 1206s are used, place 14 north, 10 inside, and 14 south of the socket.

Figure 4-17. Four-Phase Decoupling Placement

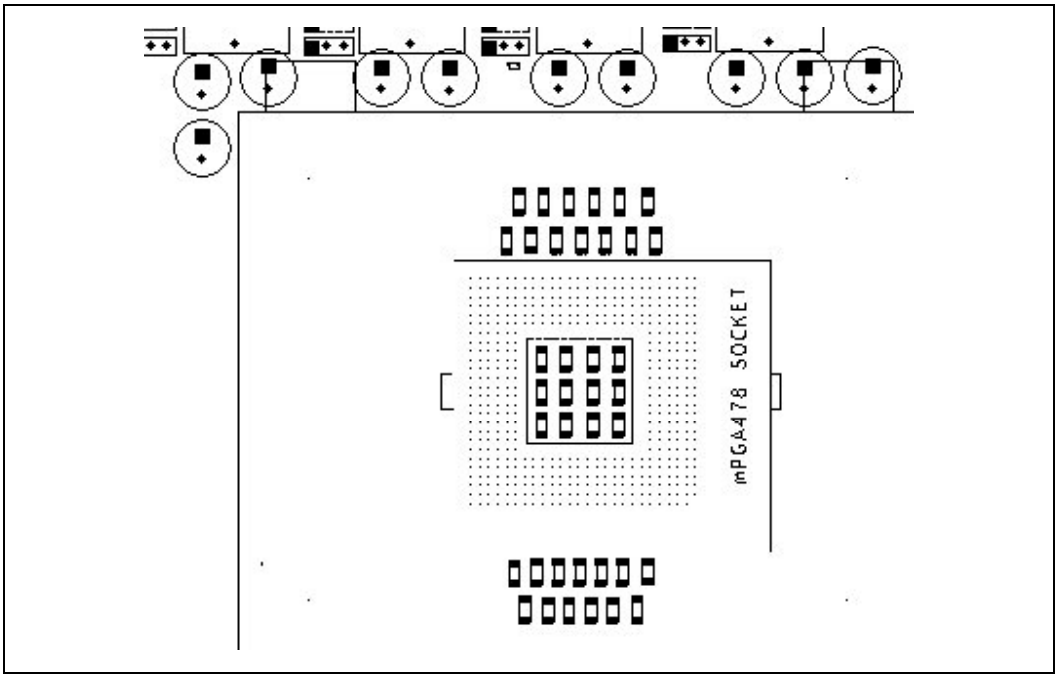
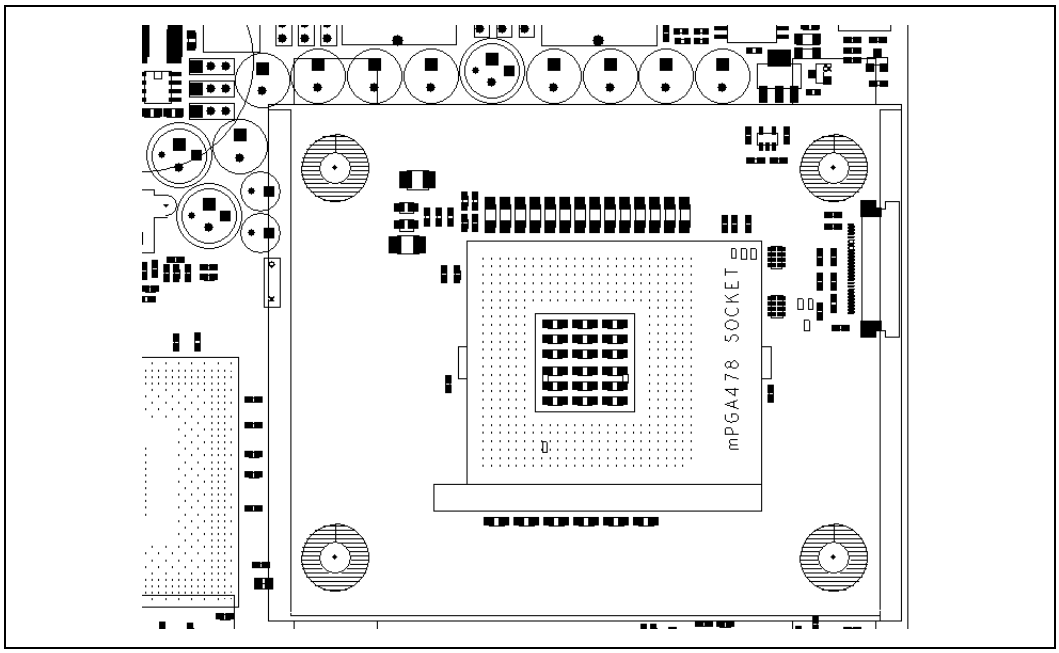


Figure 4-18. Three-Phase Decoupling Placement



4.6.3 Four-Phase Layout

All four layers in the processor area should be used for power delivery. Two layers should be used for VCC_CPU and two layers should be used for ground. Traces are not sufficient for supplying power to the processor due to the high current and low resistance required to meet the processor voltage specifications. To satisfy these requirements shapes that encompass the power delivery part of the processor pin field are required. The following figures show examples of how to use shapes to delivery power to the processor.

Figure 4-19. Top Layer Power Delivery Shape (VCC_CPU)

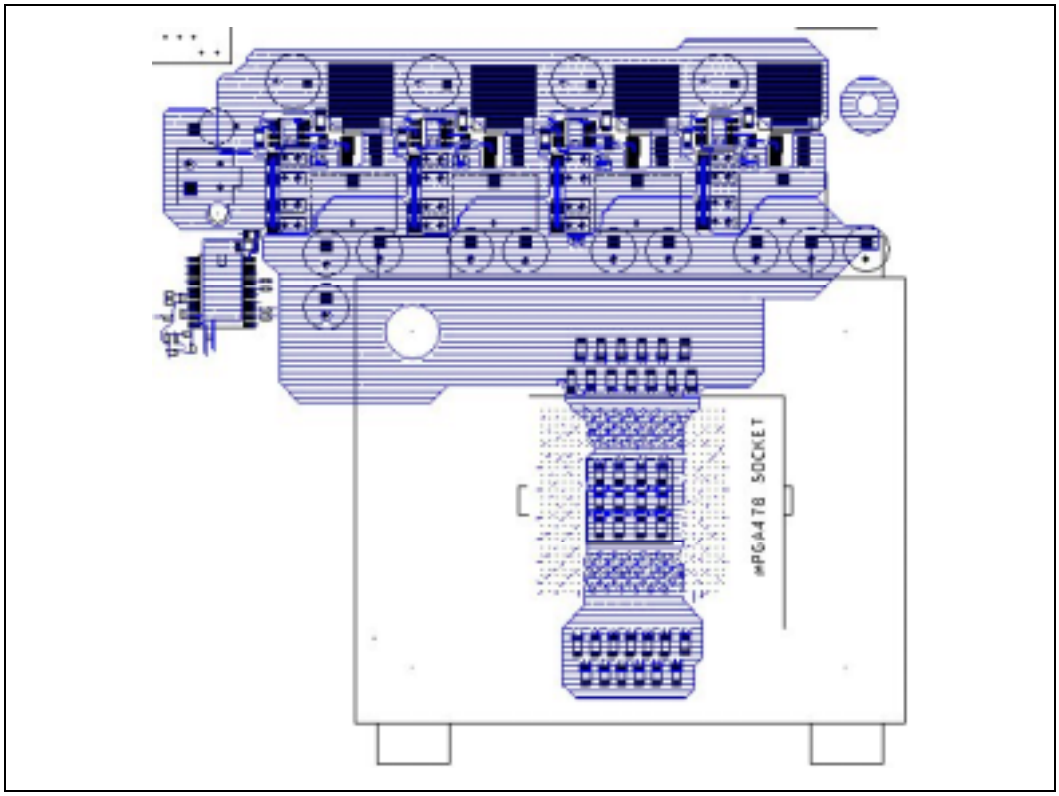


Figure 4-20. Layer 2 Power Delivery Shape (VSS)

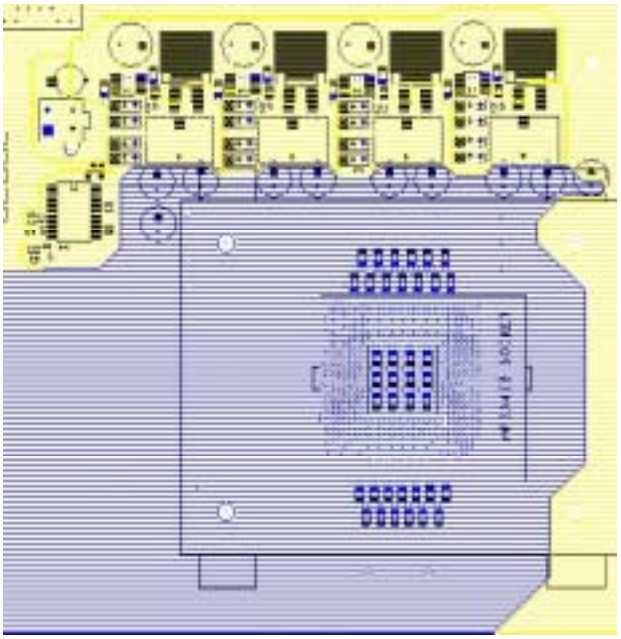


Figure 4-21. Layer 3 Power Delivery Shape (VSS)

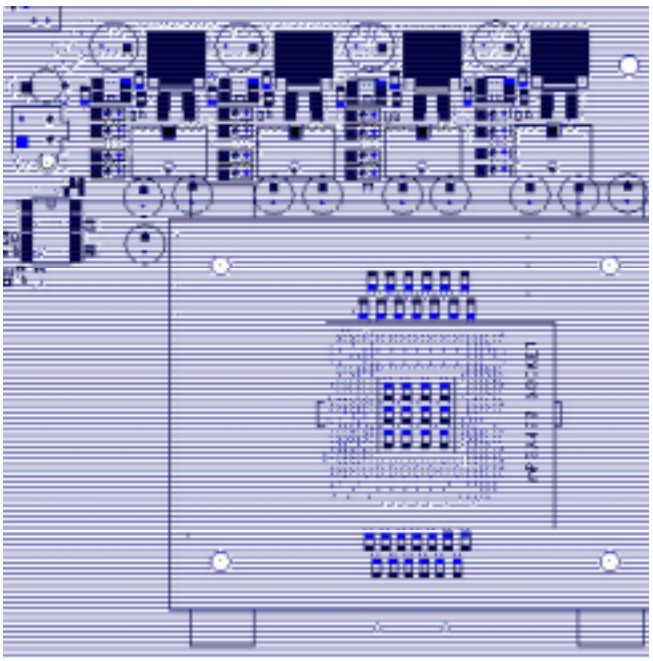
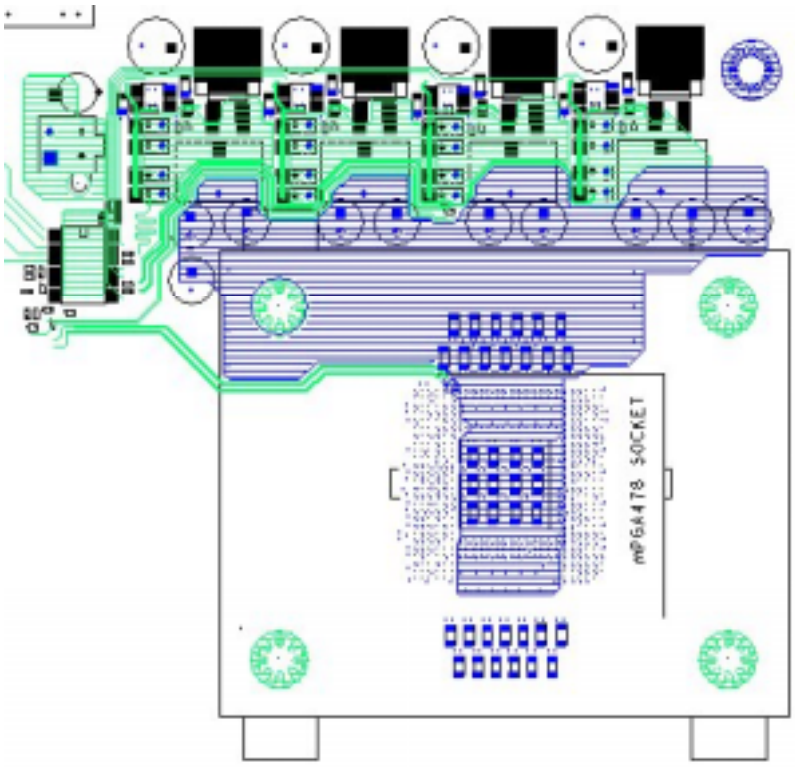


Figure 4-22. Bottom Layer Power Delivery Shape (VCC_CPU)



4.6.4 Three-Phase Layout

All four layers in the processor area should be used for power delivery. Two layers should be used for VCC_CPU and two layers should be used for ground. Traces are not sufficient for supplying power to the processor due to the high current and low resistance required to meet the processor voltage specifications. To satisfy these requirements shapes that encompass the power delivery part of the processor pin field are required. The following figures show examples of how to use shapes to delivery power to the processor.

Figure 4-23. Top Layer Power Delivery Shape (VCC_CPU)

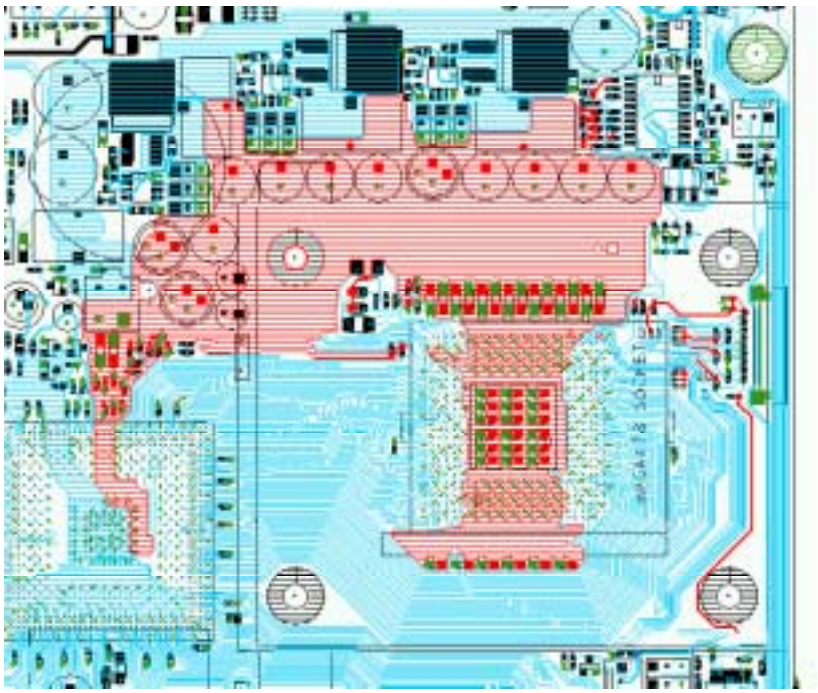


Figure 4-24. Layer 2 Power Delivery Shape (VSS)

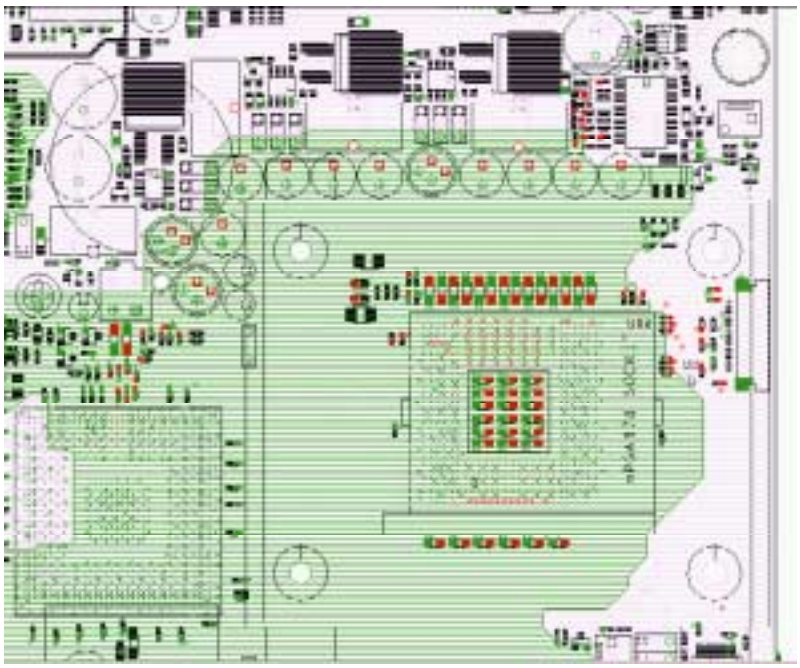


Figure 4-25. Layer 3 Power Delivery Shape (VSS)

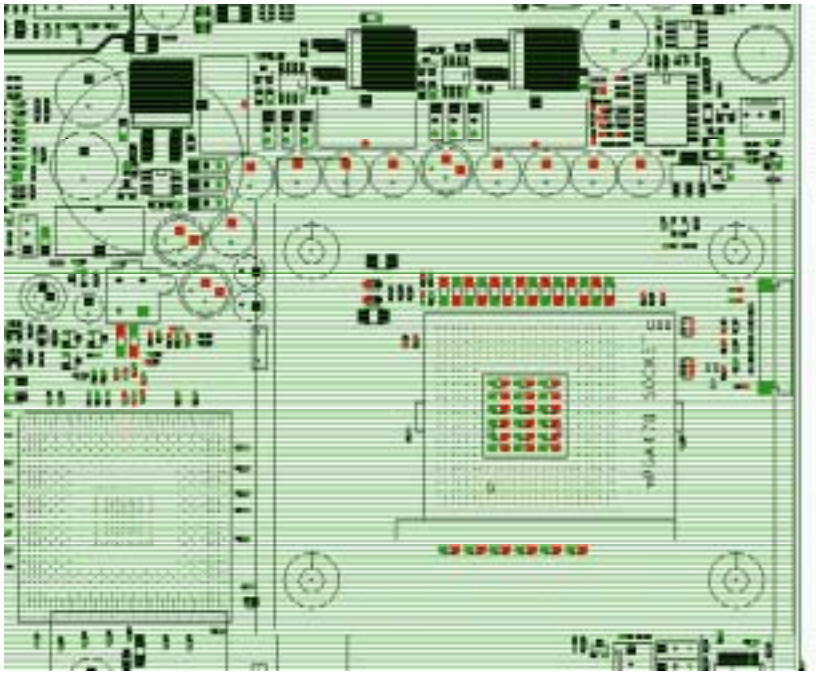
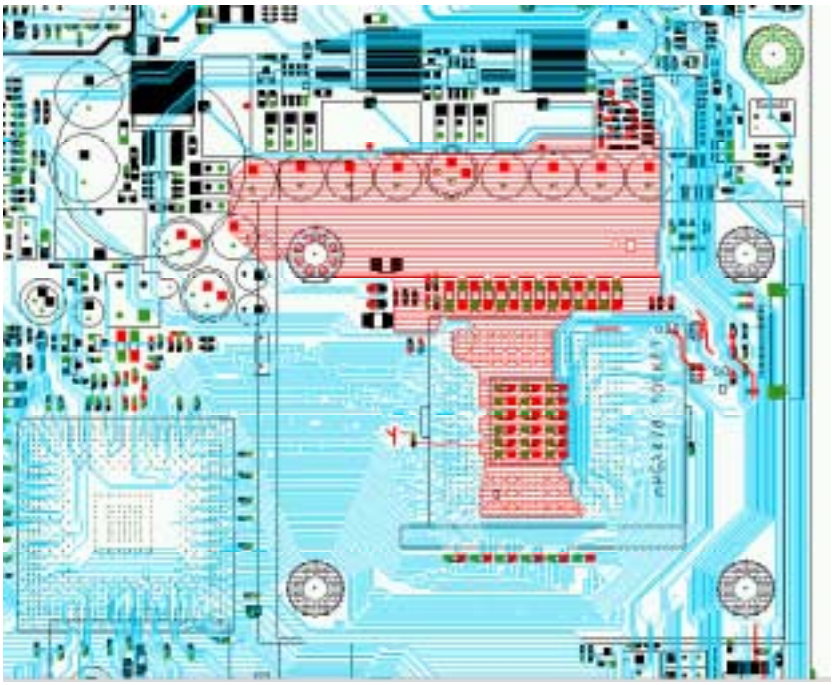


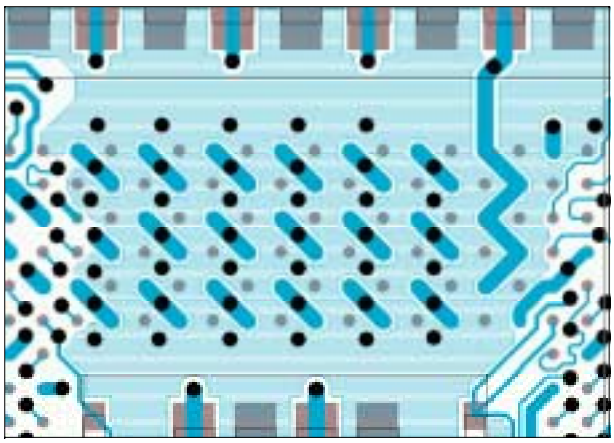
Figure 4-26. Bottom Layer Power Delivery Shape (VCC_CPU)



4.7 Common Layout Issues

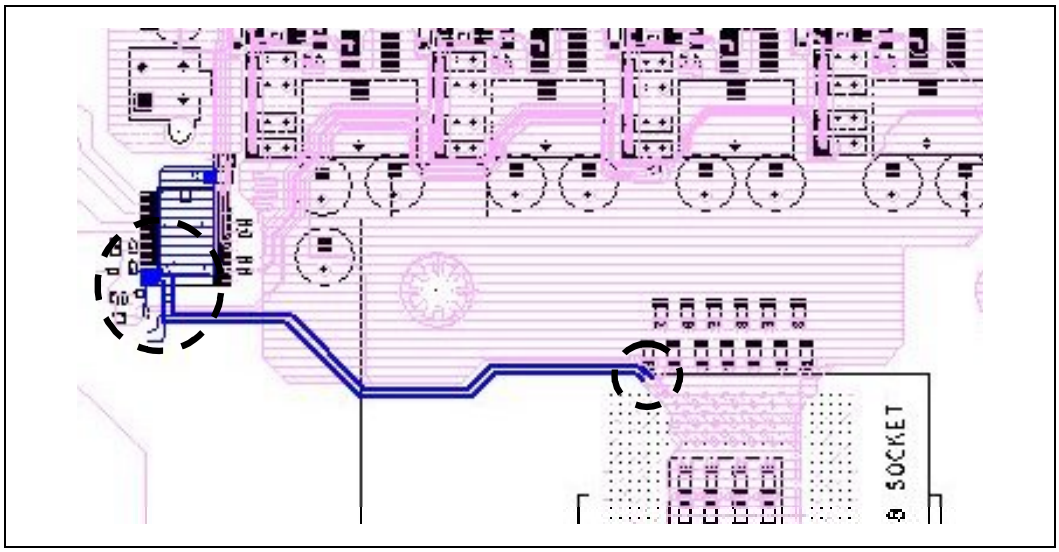
The processor socket has 478 pins with 50-mil pitch. The routing of the signals, power and ground pins will require creation of many vias. These vias cut up the power and ground planes beneath the processor resulting in increased inductance of these planes. To provide the best path through the via field, it is recommended that vias are shared for every two processor ground pins and for every two processor power pins. The following illustrates this via sharing.

Figure 4-27. Shared Power and ground Vias



The switching voltage regulators typically used for processor power delivery require the use of a feedback signal for output error correction. The VCC_SENSE and VSS_SENSE pins on the processor should not be used for generating this feedback. These pins should be used as measurement points for lab measurements only. They can be routed to a test point or via on the back of the motherboard with a trace that is a maximum length of 100 mils for this purpose. The socket loadline defined in the *Intel® Pentium® 4 Processor VR Down Design Guidelines* is defined from pins AC14 (VCC_CPU) and AC15 (VSS) and should be validated from these pins as well. These pins are located approximately in the center of the pin field on the North side of the processor. Feedback for the voltage regulator controller should therefore be taken close to this area of the power delivery shape. Figure 4-28 shows an example routing of the feedback signal. It is routed as a trace from the 1206 capacitor in the Northwest corner of the processor back to the voltage regulator controller. Because the feedback in this case is not taken from the exact point that defines the socket loadline (pins AC14/AC15), it is important to consider any voltage drop from the feedback point to these pins in the design

Figure 4-28. Routing of VR Feedback Signal



4.7.1 Thermal Considerations

For a power delivery solution to meet the flexible motherboard (FMB2) requirements, it must be able to delivery a high amount of current. This high amount of current also requires that the solution is able to dissipate the associated heat generated by the components and keep all of the components and the PCB within their thermal specifications. OEMs should evaluate their component configurations, system airflow and layout to ensure adequate thermal performance of the processor power delivery solution.

The table below shows the required amount of airflow needed for the documented designs to meet FMB2 specifications and component thermal requirements.

Table 4-19. Airflow Requirements

Design Example	Minimum Airflow	Notes
Three Phase	110 LFM	1
Four Phase	0 LFM	2

NOTES:
1. Assumes dedicated fan for Voltage Regulator (VR).
2. Assumes expanded layout area as compared to the three-phase VR design.

4.7.2 Simulation

To completely model the system board, one must include the inductance and resistance that exists in the cables, connectors, PCB planes, pins and body of components (e.g., resistors and capacitors), processor socket, and the voltage regulator module. More detailed models showing these effects are shown in Figure 4-29.

Figure 4-29. Detailed Power Distribution Model for Processor with Voltage Regulator on System Board

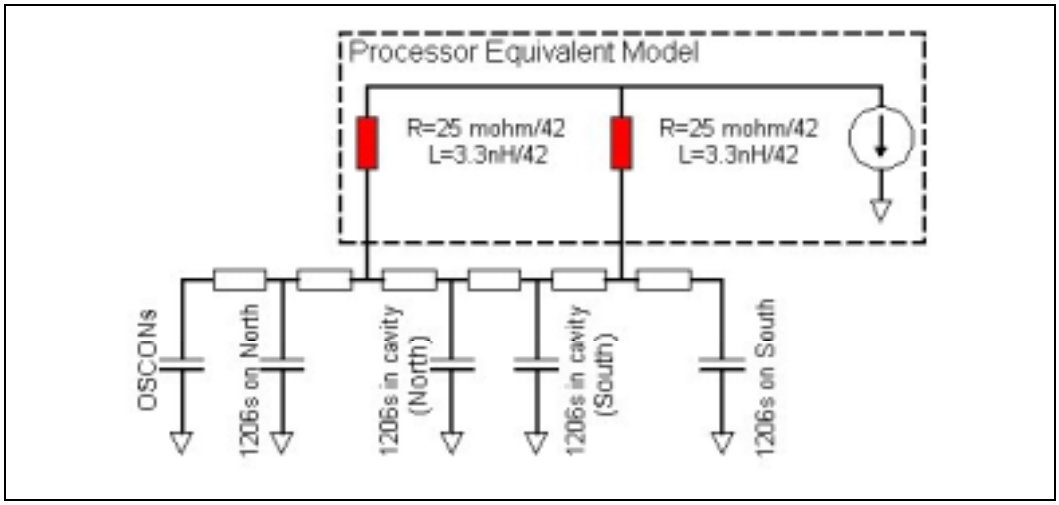


Table 4-20 lists model parameters for the system board shown in Figure 3-3. The values listed may be different depending on board layout.

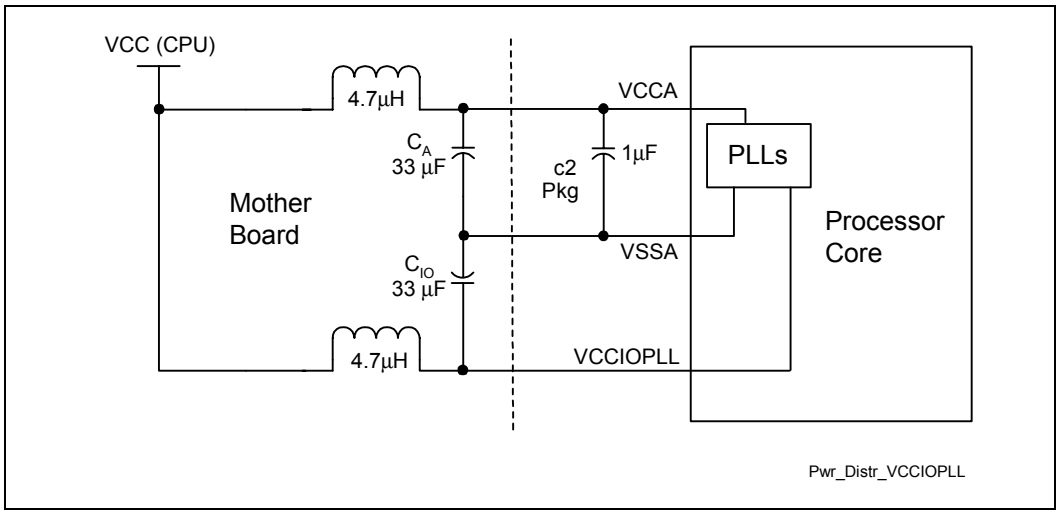
Table 4-20. Intel® Pentium® 4 Processor Power Delivery Model Parameters

Segment	Resistance	Inductance
L1	0.27 mΩ	80 pH
L2	0.33 mΩ	11.3 pH
L3	0.392 mΩ	104 pH
L4	0.196 mΩ	52 pH
L5	0.392 mΩ	104 pH
L6	0.64 mΩ	200 pH

4.7.2.1 Filter Specifications for VCCA, VCCIOPLL, and VSSA

VCCA and VCCIOPLL are power sources required by the PLL clock generators on the processor silicon. Because these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation these supplies must be low pass filtered from VCC. The general desired filter topology is shown in the following figure. Not shown in the core is parasitic routing. Excluded from the external circuitry are parasitics associated with each component.

Figure 4-30. Typical VCCIOPLL, VCCA, and VSSA Power Distribution



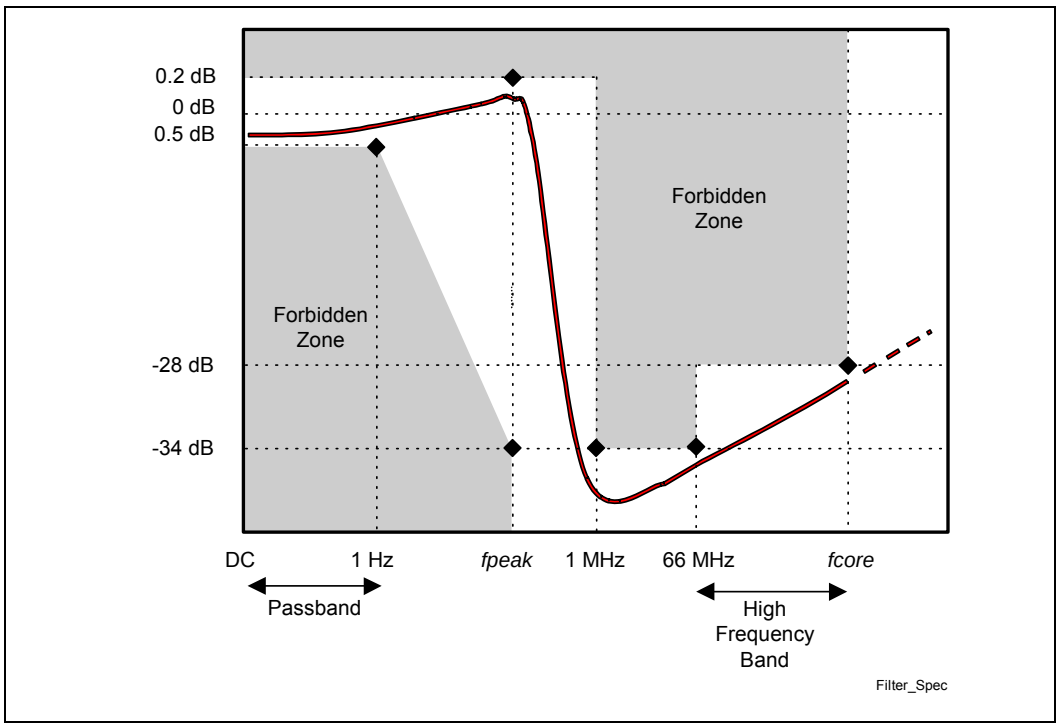
The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity this document will address the recommendation for the VCCA filter design. The same characteristics and design approach is applicable for the VCCIOPLL filter design.

The AC low-pass recommendation, with input at VCC and output measured across the capacitor (C_A or C_{IO} in Figure 4-30), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter recommendation (AC) is graphically shown in Figure 4-31.

Figure 4-31. Filter Recommendation



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond fcore (core frequency).
3. fpeak, if existent, should be less than 0.05 MHz.

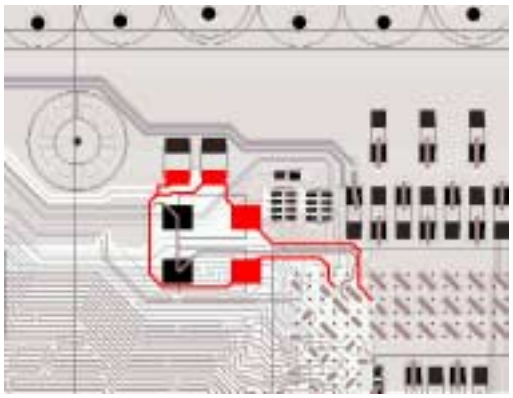
Other Recommendations

- Use shielded type inductors to minimize magnetic pickup
- Capacitors for the filter can be any value between 22 µF and 100 µF as long as components with ESL ≤ 5 nH and ESR < 0.3 Ω are used.
- Values of either 4.7 µH or 10 µH may be used for the inductor
- Filter should support DC current > 60 mA
- DC voltage drop from VCC to VCCA should be < 60 mV
- To maintain a DC drop of less than 60 mV, the total DC resistance of the filter from VCC_CPU to the processor socket should be a maximum of 1 Ω.

Other Routing Requirements

- C should be within 600 mils of the VCCA and VSSA pins. An example of the component placement is shown in Figure 4-32.
- VCCA route should be parallel and next to VSSA route (minimize loop area)
- A minimum of a 12-mil trace should be used to route from the filter to the processor pins.
- L should be close to C

Figure 4-32. Example Component Placement for PLL Filter



4.7.3 Electrostatic Discharge Platform Recommendations

Electrostatic discharge (ESD) into a system can lead to system instability, and possibly cause functional failures when a system is in use. There are system level design methodologies that when followed can lead to higher ESD immunity. Electromagnetic fields due to ESD are introduced into a system through chassis openings such as the I/O back panel and PCI slots. These fields can introduce noise into signals and cause the system to malfunction. One can reduce the potential for issues at the I/O area by adding more ground plane on the motherboard around the I/O area. This can lead to a higher ESD immunity.

Intel recommends that the I/O area on the top and bottom signal layers of a 4-layer motherboard near the I/O back panel be filled with a ground fill as shown in the following figures. In addition, a ground fill cutout should be placed on the VCC layer in the area where the ground fill is done on the top and bottom layers. Intel recommends filling the I/O area as much as possible without effecting the signal routing. The board designer should fill the entire I/O area along the board edge.

The spacing from the ground fill to other shapes/traces should be at least 20 mils. It is recommended that these ground fill areas be connected to two chassis mounting holes (as shown in Figure 4-34). This will allow ESD current to travel to the chassis instead of the board. Ground stitching vias should be placed throughout the entire ground fill if possible. It is important that the vias are placed along the board edge. Ground stitching vias for the ground fill should be 100–150 mils apart or less.

Intel recommends the following:

- Fill the I/O area with the ground fill in all layers including signal layers whenever possible
- Extend the ground fill along the entire back I/O area
- Connect the ground fill to mounting holes
- Place stitching vias 100–150 mils apart in the entire ground fill

Figure 4-33. Top Signal Layer before the Ground Fill Near the I/O Area

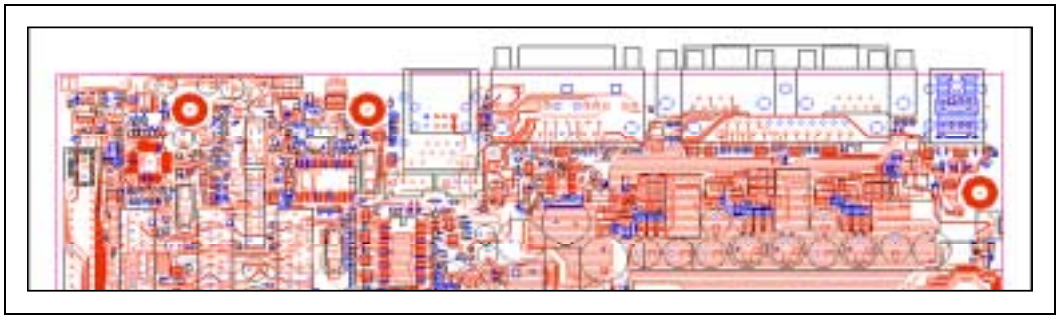


Figure 4-34. Top Signal Layer After the Ground Fill Near the I/O Area

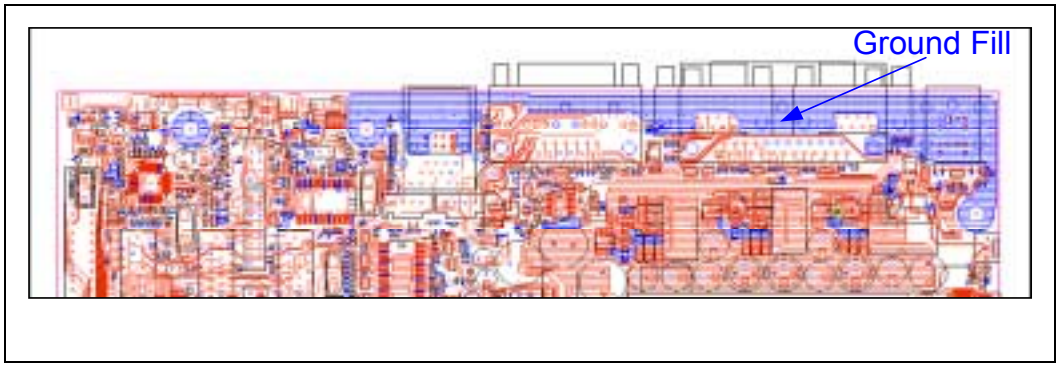


Figure 4-35. Bottom Signal Layer Before the Ground Fill Near the I/O Area

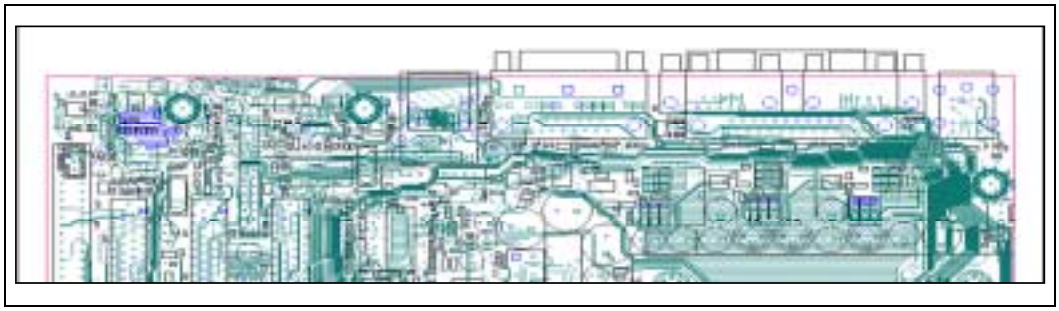
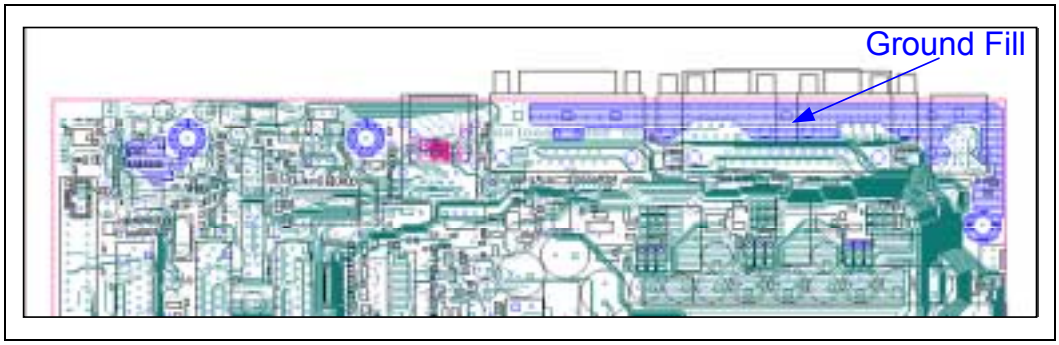


Figure 4-36. Bottom Signal Layer After the Ground Fill Near the I/O Area



4.8 Intel® Pentium® 4 Processor and Intel® (G)MCH Chipset PSB Package Lengths

Table 4-21. Processor / Intel® (G)MCH PSB Package Lengths

Processor Lengths			Intel® (G)MCH Lengths		
Signal	**Processor Ball**	**Length (inches)**	**Signal**	**(G)MCH Ball**	**Length (inches)**
Address Group 0					
ADSTB0#	L5	0.210	HADSTB_0#	AB35	0.569
A3#	K2	0.368	HA3#	W31	0.362
A4#	K4	0.265	HA4#	AA33	0.468
A5#	L6	0.155	HA5#	AB30	0.353
A6#	K1	0.415	HA6#	V34	0.520
A7#	L3	0.304	HA7#	Y36	0.597
A8#	M6	0.144	HA8#	AC33	0.497
A9#	L2	0.372	HA9#	Y35	0.575
A10#	M3	0.327	HA10#	AA36	0.636
A11#	M4	0.246	HA11#	AC34	0.521
A12#	N1	0.394	HA12#	AB34	0.566
A13#	M1	0.408	HA13#	Y34	0.516
A14#	N2	0.349	HA14#	AB36	0.612
A15#	N4	0.241	HA15#	AC36	0.604
A16#	N5	0.198	HA16#	AC31	0.465
REQ0#	J1	0.427	HREQ0#	V36	0.594
REQ1#	K5	0.207	HREQ1#	AA31	0.413
REQ2#	J4	0.270	HREQ2#	W33	0.443
REQ3#	J3	0.337	HREQ3#	AA34	0.535
REQ4#	H3	0.356	HREQ4#	W35	0.555
Address Group 1					
ADSTB1#	R5	0.214	HADSTB_1#	AF30	0.442
A17#	T1	0.470	HA17#	AF35	0.631
A18#	R2	0.404	HA18#	AD36	0.617
A19#	P3	0.303	HA19#	AD35	0.598
A20#	P4	0.246	HA20#	AE34	0.558
A21#	R3	0.334	HA21#	AD34	0.566
A22#	T2	0.388	HA22#	AE36	0.623
A23#	U1	0.458	HA23#	AF36	0.663

Processor Lengths			Intel® (G)MCH Lengths		
Signal	**Processor Ball**	**Length (inches)**	**Signal**	**(G)MCH Ball**	**Length (inches)**
A24#	P6	0.156	HA24#	AE33	0.508
A25#	U3	0.379	HA25#	AF34	0.553
A26#	T4	0.281	HA26#	AG34	0.634
A27#	V2	0.417	HA27#	AG36	0.663
A28#	R6	0.166	HA28#	AE31	0.531
A29#	W1	0.493	HA29#	AH35	0.658
A30#	T5	0.217	HA30#	AG33	0.557
A31#	U4	0.285	HA31#	AG31	0.494
Data Group 0					
DSTBN0#	E22	0.338	HDSTB_N0#	N31	0.520
DSTBP0#	F21	0.326	HDSTB_P0#	L31	0.528
D0#	B21	0.414	HD0#	T30	0.385
D1#	B22	0.475	HD1#	R33	0.465
D2#	A23	0.538	HD2#	R34	0.544
D3#	A25	0.608	HD3#	N34	0.578
D4#	C21	0.386	HD4#	R31	0.400
D5#	D22	0.386	HD5#	L33	0.540
D6#	B24	0.535	HD6#	L36	0.632
D7#	C23	0.464	HD7#	P35	0.575
D8#	C24	0.515	HD8#	J36	0.691
D9#	B25	0.590	HD9#	K34	0.561
D10#	G22	0.274	HD10#	K36	0.652
D11#	H21	0.203	HD11#	M30	0.383
D12#	C26	0.589	HD12#	M35	0.612
D13#	D23	0.462	HD13#	L34	0.588
D14#	J21	0.183	HD14#	K35	0.620
D15#	D25	0.550	HD15#	H36	0.695
DBI0#	E21	0.309	DINV_0#	N33	0.560
Data Group 1					
DSTBN1#	K22	0.301	HDSTB_N1#	G33	0.646
DSTBP1#	J23	0.306	HDSTB_P1#	J34	0.777
D16#	H22	0.272	HD16#	G34	0.660
D17#	E24	0.480	HD17#	G36	0.728
D18#	G23	0.358	HD18#	J33	0.526

Processor Lengths			Intel® (G)MCH Lengths		
Signal	**Processor Ball**	**Length (inches)**	**Signal**	**(G)MCH Ball**	**Length (inches)**
D19#	F23	0.418	HD19#	D35	0.787
D20#	F24	0.443	HD20#	F36	0.747
D21#	E25	0.508	HD21#	F34	0.696
D22#	F26	0.513	HD22#	E36	0.793
D23#	D26	0.597	HD23#	H34	0.644
D24#	L21	0.176	HD24#	F35	0.696
D25#	G26	0.524	HD25#	D36	0.818
D26#	H24	0.412	HD26#	H35	0.645
D27#	M21	0.171	HD27#	E33	0.687
D28#	L22	0.245	HD28#	E34	0.739
D29#	J24	0.401	HD29#	B35	0.846
D30#	K23	0.313	HD30#	G31	0.548
D31#	H25	0.473	HD31#	C36	0.876
DBI1#	G25	0.458	DINV_1#	C35	0.786
Data Group 2					
DSTBN2#	K22	0.252	HDSTB_N2#	C30	0.694
DSTBP2#	J23	0.266	HDSTB_P2#	E29	0.616
D32#	M23	0.300	HD32#	D33	0.750
D33#	N22	0.226	HD33#	D30	0.672
D34#	P21	0.178	HD34#	D29	0.621
D35#	M24	0.371	HD35#	E31	0.627
D36#	N23	0.271	HD36#	D32	0.694
D37#	M26	0.454	HD37#	C34	0.802
D38#	N26	0.437	HD38#	B34	0.878
D39#	N25	0.383	HD39#	D31	0.661
D40#	R21	0.165	HD40#	G29	0.514
D41#	P24	0.343	HD41#	C32	0.762
D42#	R25	0.381	HD42#	B31	0.751
D43#	R24	0.329	HD43#	B32	0.800
D44#	T26	0.420	HD44#	B30	0.754
D45#	T25	0.380	HD45#	B29	0.716
D46#	T22	0.221	HD46#	E27	0.570
D47#	T23	0.279	HD47#	C28	0.718
DBI2#	P26	0.441	DINV_2#	B33	0.825

Processor Lengths			Intel® (G)MCH Lengths		
Signal	**Processor Ball**	**Length (inches)**	**Signal**	**(G)MCH Ball**	**Length (inches)**
Data Group 3					
DSTBN3#	W22	0.298	HDSTB_N3#	D25	0.596
DSTBP3#	W23	0.300	HDSTB_P3#	E25	0.606
D48#	U26	0.419	HD48#	B27	0.718
D49#	U24	0.324	HD49#	D26	0.633
D50#	U23	0.270	HD50#	D28	0.663
D51#	V25	0.384	HD51#	B26	0.692
D52#	U21	0.167	HD52#	G27	0.599
D53#	V22	0.252	HD53#	H26	0.577
D54#	V24	0.341	HD54#	B25	0.666
D55#	W26	0.447	HD55#	C24	0.591
D56#	Y26	0.454	HD56#	B23	0.645
D57#	W25	0.426	HD57#	B24	0.715
D58#	Y23	0.336	HD58#	E23	0.482
D59#	Y24	0.386	HD59#	C22	0.586
D60#	Y21	0.222	HD60#	G25	0.459
D61#	AA25	0.426	HD61#	B22	0.632
D62#	AA22	0.268	HD62#	D24	0.583
D63#	AA24	0.394	HD63#	G23	0.399
DBI3#	V21	0.202	DINV_3#	C26	0.689

5 DDR System Memory Design Guidelines

The 845GE/845PE chipset Double Data Rate (DDR) SDRAM system memory interface provides support for DDR266 or DDR333 memory.

The first two sections in this chapter provide information on the DDR reference stack-up. The third section describes the DDR topologies, layout, and routing guidelines organized by signal group (see Table 5-1).

Table 5-1. Intel® (G)MCH DDR Signal Groups

Section	Group	Signal Name	Description
5.2.1	Data	SDQ_[63:0]	Data Bus
		SDM_[7:0]	Data Masks
		SDQS_[7:0]	Data Strobes
5.2.2	Control	SCKE_[3:0]	Clock Enable
		SCS_[3:0]#	Chip Select
5.2.3	Address / Command	SMAA_[12:6, 3, 0]	Memory Address Bus
		SBA_[1:0]	Bank Address (Bank Select)
		SRAS#	Row Address Select
		SCAS#	Column Address Select
		SWE#	Write Enable
5.2.4	CPC Address	SMAA_[5,4,2,1]	Memory Address Bus CPC signals
		SMAB_[5,4,2,1]	Memory Address Bus CPC signals
5.2.5	Clocks[1]	SCMD_SCK[5:0]	DDR-SDRAM Differential Clocks
		SCMD_SCK[5:0]#	DDR-SDRAM Inverted Differential Clocks
5.2.6	Feedback	SRCVEN_OUT#	Output Feedback Signal
		SRCVEN_IN#	Input Feedback Signal

NOTES:
1. The recommended routing order is listed in the beginning of Section 5.2.

The remaining two sections contain information and details on the system memory bypass capacitor guidelines and DDR power delivery requirements. Together, these design guidelines provide for a robust DDR solution for an 845GE/845PE chipset-based design.

The 845GE/845PE chipset does not support Error Checking and Correction (ECC). Refer to the *Intel® 845GE/845PE Chipset Datasheet* for more signal details.

5.1 DDR-SDRAM Stack-Up and Referencing Guidelines

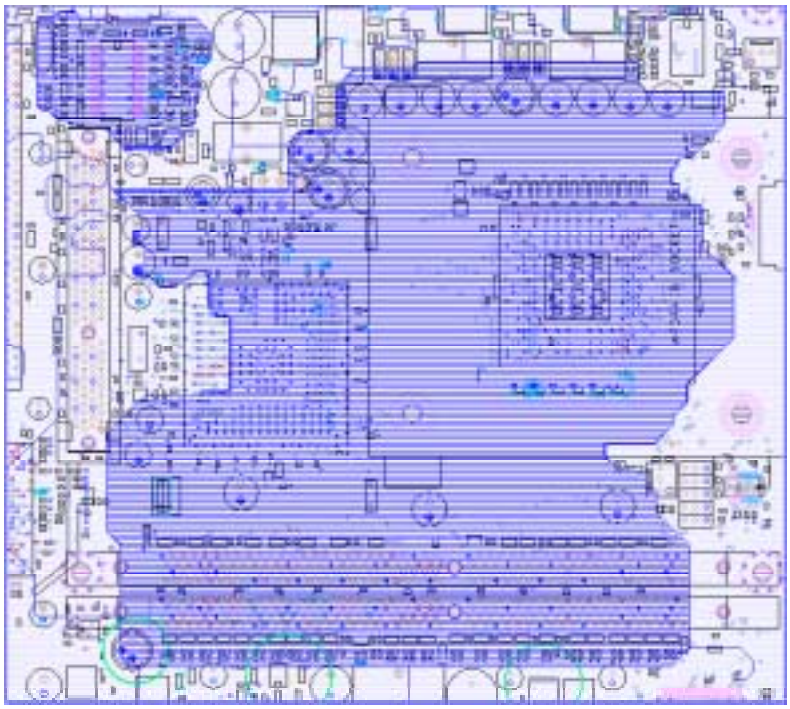
The 845GE/845PE platform designs using the DDR-SDRAM memory sub-system requires continuous ground referencing for all DDR signals. Based on the four-layer stack-up in Section 3.2, the DDR channel requires the following referencing stack-up to ground reference all of the DDR signals from the (G)MCH to the parallel termination at the end of the channel. Note the DDR channel stack-up applies to the DDR channel only.

Table 5-2. DDR Channel Referencing Stack-Up

Motherboard Layer	Description
Layer 1	Signal / Power
Layer 2	Ground Flood
Layer 3	Ground
Layer 4	Signal / Power

A solid continuous ground flood must be placed under the DDR channel on layer two from the (G)MCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel to provide an optimal current return path. Any split in the ground flood will provide a sub-optimal return path. The DDR and the processor ground flood must be connected to together, as shown in Figure 5-1.

Figure 5-1. Layer Two Preliminary Ground Flood Picture



Ground Stitching

The ground flood must be well stitched to the ground plane on layer three to ensure the same potential between the two layers. Any ground pin or ground via that is placed in the DDR routing area must connect to both the ground flood and the ground plane:

- DIMM Connector ground pins
- (G)MCH DDR ground pins in the DDR interface section.
- Ground ends of the DDR-DIMM high-frequency bypass capacitors
- Ground vias for the (G)MCH 2.5 V high-frequency decoupling capacitors
- Ground ends connecting to the VTT termination decoupling capacitors
- Ground vias wherever possible around the edge of the ground flood
- Ground vias along the edge where the DDR and PSB ground floods connect on layer two

5.2 DDR System Memory Topology and Layout Design Guidelines

The 845GE/845PE chipset Double Data Rate (DDR) SDRAM system memory interface implements SSTL_2 topology. This section is organized by signal group.

- Section 5.2.1 - Data
- Section 5.2.2 - Control
- Section 5.2.3 - Address / Command
- Section 5.2.4 - CPC Address
- Section 5.2.5 – Clock
- Section 5.2.6 – Feedback

Routing Order

To help maximize routing efficiency, it is **highly recommended** to follow the routing order below. The following routing order has been developed and optimized for the guidelines.

1. CPC Address
2. Control (SCS#, SCKE)
3. Clocks (see note)
4. Address/command
5. Data (includes mask and strobes)

Note: Clock lengths in the following sections refer to the total clock lengths, which are measured from (G)MCH die to DIMM connector.

The CPC address and control (SCS#, SCKE) signals should be routed first on layer 4 because these signals can help determine the system clock length. A portion of the address/command signal group will likely have to be routed at the same time as the CPC address signals because the address/command signals are intermixed with the CPC Address signal routing. Be mindful of the 2.5 V power delivery to the (G)MCH, which is flooded on Layer 4 in between the various signals on Layer 4 (see Section 5.4)

As an example, after routing the CPC address, take the longest routed CPC address length for each associated DIMM and use the CPC address length matching guidelines to help determine the minimum total target clock length (versus routed length) based on CPC address routing. If the minimum total target clock length for second DIMM is over 0.5 inch greater than for the first DIMM, use the second DIMM target clock length as your base target, and subtract 0.5 inch to get the first DIMM target clock length. Do the same for Control signals, and determine whether the CPC address signals or the Control signals are your limiting factor.

Once the total target clock length has been determined, use the DIMM clock matching guidelines (Section 5.2.5) to match all total target clock lengths to each associated DIMM. The difference between the total target clock length for the first DIMM and the second DIMM should be 0.5 inch. The remaining address/command and data signals can then be routed.

The following DDR guidelines should be followed based on the 4-layer stack-up (Section 3.2), the (G)MCH ball field, and that all DDR signals must be referenced to ground.

5.2.1 Data Signals — SDQ_[63:0], SDQS_[7:0], SDM_[7:0]

The (G)MCH data signals are source synchronous signals that include the 64-bit wide data bus, 8 data masks (SDM), and 8 data strobe signals (SDQS). There is an associated data strobe (SDQS) for each data (SDQ) and data mask (SDM) group. Table 5-3 summarizes the SDQ/SDM to SDQS mapping. SDQ/SDM are tuned to SDQS, and SDQS are tuned to SCMDCLK.

Table 5-3. SDQ/SDM to SDQS Mapping

SDQ/SDM	SDQS
SDQ_[7:0] / SDM_0	SDQS_0
SDQ_[15:8] / SDM_1	SDQS_1
SDQ_[23:16] / SDM_2	SDQS_2
SDQ_[31:24] / SDM_3	SDQS_3
SDQ_[39:32] / SDM_4	SDQS_4
SDQ_[47:40] / SDM_5	SDQS_5
SDQ_[55:48] / SDM_6	SDQS_6
SDQ_[63:56] / SDM_7	SDQS_7

All data and strobe signals **must** be routed on layer one. The (G)MCH system memory pin out has been optimized to breakout all the data and strobe signals on the top signal layer. The data signals should break out of the (G)MCH and route entirely on the top signal layer referenced to ground, from the (G)MCH to the series termination resistor, from the series termination resistor to the first DIMM, from DIMM to DIMM, and from the second DIMM to the parallel termination.

Resistor packs are acceptable for the series (Rs) and parallel (Rtt) data and data strobe termination resistors, but data and strobe signals **cannot** be routed to the same resistor pack (RPACK) used by address/command, CPC address, or control signals. Termination resistor packs for the data group must remain dedicated to data group signals, and not be used for any other signal groups.

The following figures and table describe the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Figure 5-2. Data Signal Routing Topology

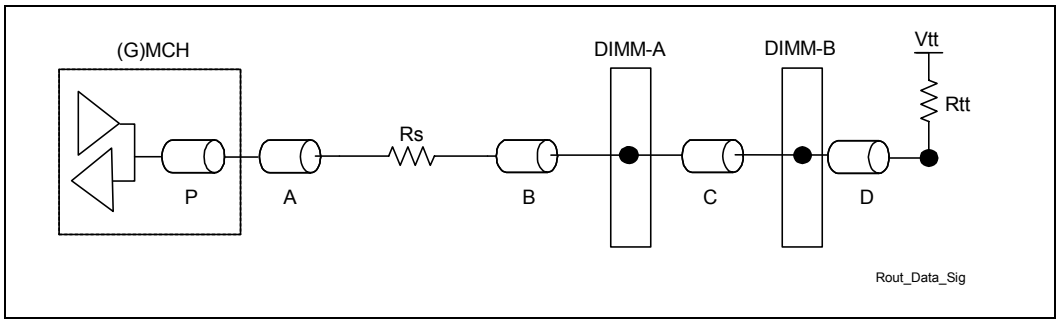
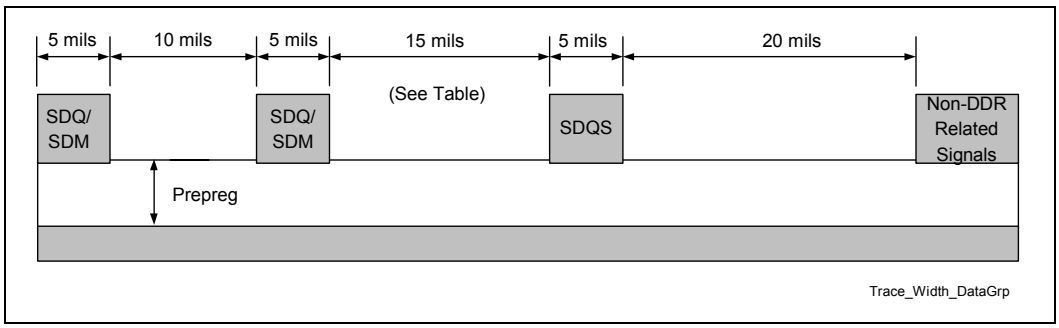


Table 5-4. Data Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	Data – SDQ_[63:0], SDQS_[7:0], SDM_[7:0]
Topology	Daisy Chain
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Nominal Trace Width	5 mils
Nominal Trace Spacing	• SDQS to SDQ/SDM = 15 mils • SDQ/SDM to SDQ/SDM = 10 mils • Within DIMM Pin Field = 7 mils minimum • From DIMM to DIMM = 12 mils • Second DIMM to Rtt = 7 mils minimum
Group Spacing	Isolation from non-DDR related signals = 20 mils minimum
(G)MCH Breakout Guidelines	5 mil width with 6-mil spacing for a max of 350 mils. **Note:** Use of breakout guidelines should be minimized.
Total Trace Length **P + A + B** – (G)MCH signal Pad to First DIMM Pin	Max = 5.8 inches Note: See Section 5.2.7 for package length P.
Trace Length B – Series Termination Resistor Pad to First DIMM Pin	Max = 500 mils The resistor should be placed within 500 mils of the first DIMM.
Trace Length C – DIMM Pin to DIMM Pin	Min = 400 mils Max = 600 mils
Trace Length D – Last DIMM Pin to Parallel termination Resistor Pad	Max = 800 mils
Series Resistor (Rs)	10 Ω ± 5%
Termination Resistor (Rtt)	56 Ω ± 5%
Maximum via Count per signal	0 (all signals are routed on the top layer)
Length Tuning Method	• SDQ_[63:0] / SDM_[7:0] to associated SDQS_[7:0] • SDQS_[7:0] to SCMDCLK_[5:0]/SCMDCLK_[5:0]# per DIMM See Section 5.2.1.1.1 and Section 5.2.1.1.2 for details

Figure 5-3. Data Group Signal Trace Width/Spacing Routing



5.2.1.1 Data Group Signal Length Matching Requirements

5.2.1.1.1 Data to Strobe Length Matching Requirements

Data/data mask (SDQ_[63:0], SDM_[7:0]) and data strobe (SDQS_[7:0]) signals **require** tuning from (G)MCH internal **pads** to the first DIMM **and** from (G)MCH internal pads to the second DIMM connector pins for data/data mask to the associated data strobe within each byte group.

SDQS Total Length = X

Associated SDQ/SDM Byte Group Total Length = Y, where (X – 25 mils) ≤ Y ≤ (X + 25 mils)

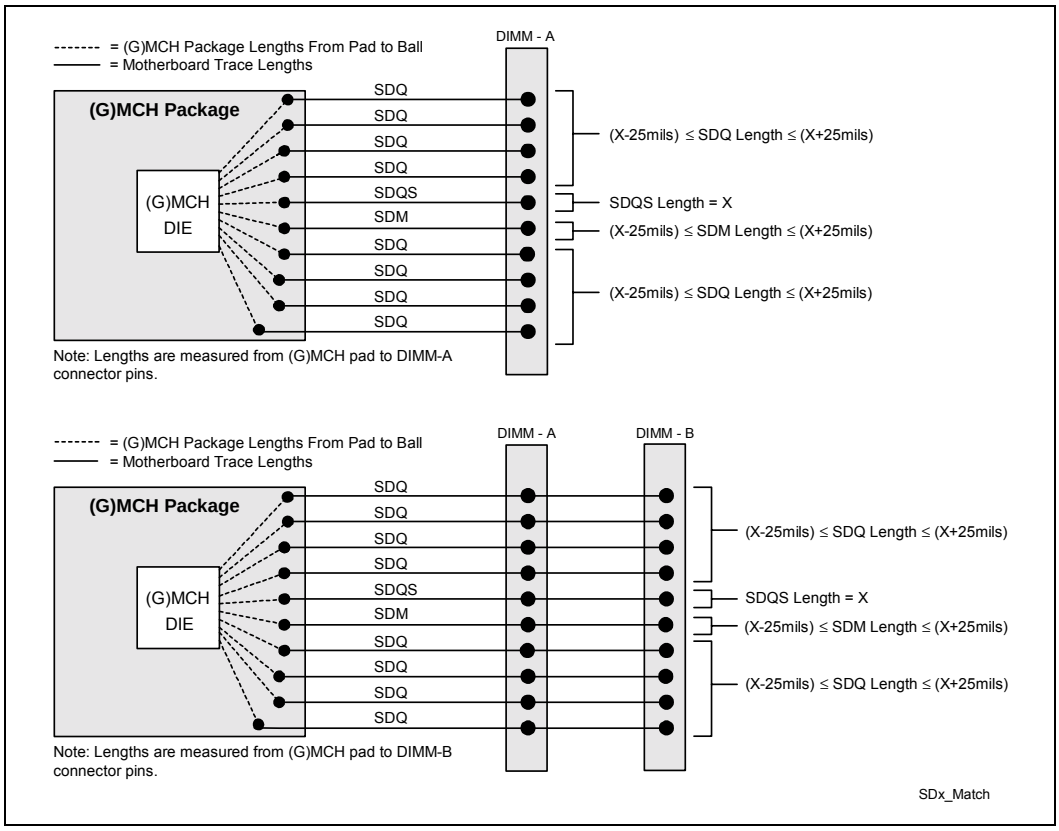
Length X and Y to first DIMM includes the (G)MCH Package Length P + Motherboard Trace Length A + B.

Length X and Y to second DIMM includes the (G)MCH Package Length P + Motherboard Trace Lengths A + B + C.

SDQS_[7:0] motherboard trace length guidelines A, B and C are described in Table 5-4. No length matching is required from the second DIMM to the parallel termination resistors. Refer to Section 5.2.7 for (G)MCH data and strobe package length data.

Figure 5-4 shows the length matching requirements between the SDQ, SDM, and SDQS signals.

Figure 5-4. SDQ/SDM to SDQS Trace Length Matching Requirements



5.2.1.1.2 Strobe to Command Clock Length Matching Requirements

Tuning is required from (G)MCH internal **pad** to the pins of the DIMM connector for strobe to the differential clock signals.

- On an 845GE/845PE chipset based DDR platform, the total target data strobe lengths must be longer than the total target differential clock minus 4.4 inches for the associated DIMM.

  SCMDCLK/SCMDCLK# Total Length = X

  SDQS Total Length = Y, where (X – 4.4 inches) ≤ Y

Length X to first and second DIMM includes the (G)MCH Package Length P + Motherboard Trace Length A.

Length Y to first DIMM includes the (G)MCH Package Length P + Motherboard Trace Lengths A + B.

Length Y to second DIMM includes the (G)MCH Package Length P + Motherboard Trace Lengths A + B + C

SDQS_[7:0] motherboard trace length guidelines A, B and C are documented in Table 5-4. No length matching is required from the second DIMM to the parallel termination resistors. Refer to Section 5.2.7 for (G)MCH data and strobe package length data.

The diagram below depicts the length matching requirements between the SDQS and clock signals.

Figure 5-5. SDQS to SCMDCLK/SCMD_CLK# Trace Length Matching Requirements

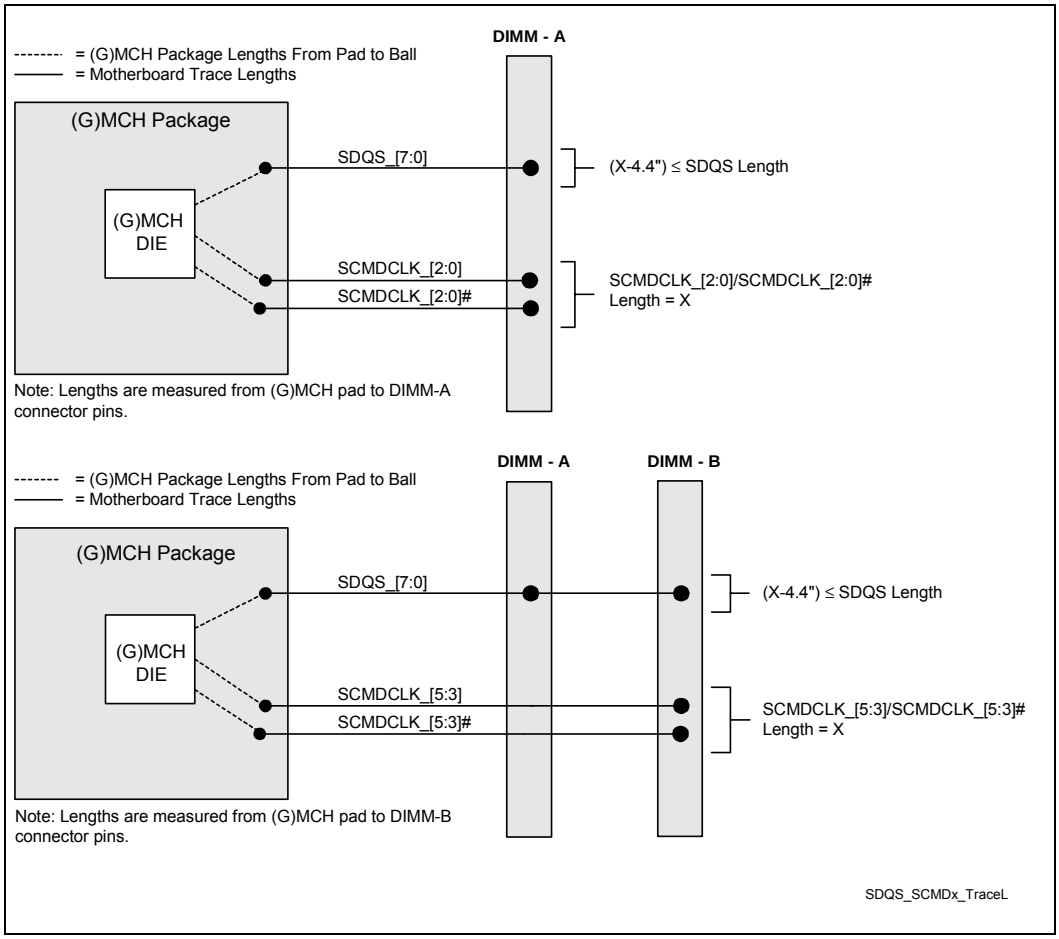
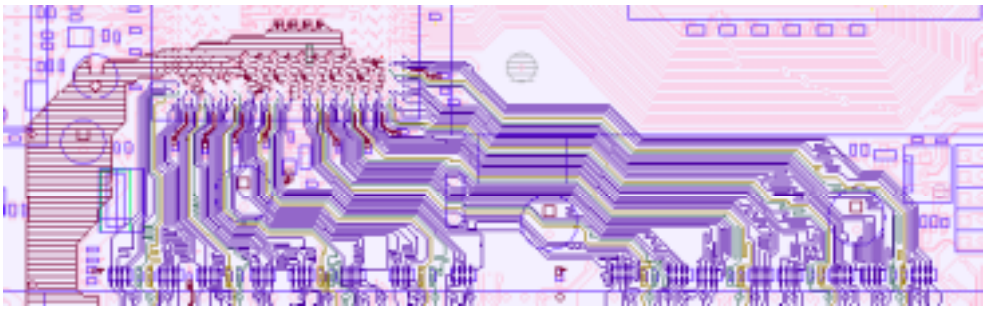


Figure 5-6. Data Group Top Layer to First DIMM Routing Example



5.2.2 Control Signals (SCKE_[3:0], SCS_[3:0]#)

The (G)MCH control signals that include the enable (SCKE) and chip select (SCS#) are source-clocked signals. One chip select (SCS#) and one clock enable (SCKE) signals are needed per row. SCKE and SCS# are tuned to SCMD_CLK. Table 5-5 summarizes the SCKE/SCS# to DIMM and DIMM pin mapping.

Table 5-5. Control Signal DIMM Mapping

Signal	Relative To	DIMM Pin
SCS_0#	DIMMA	157
SCS_1#	DIMMA	158
SCS_2#	DIMMB	157
SCS_3#	DIMMB	158
SCKE_0	DIMMA	21
SCKE_1	DIMMA	111
SCKE_2	DIMMB	21
SCKE_3	DIMMB	111

The (G)MCH system memory pin out has been optimized to breakout the control signals on the **bottom** signal layer and all control signals need to be routed on the same layer. They should transition from the top signal layer to the bottom signal layer under the (G)MCH. They should be routed on the bottom signal layer until the first DIMM or until they transition to the top signal layer within 500 mils before the first DIMM connector. Finally they should route from the DIMM connector pins to the parallel termination resistors at the end of the memory channel on the top signal layer.

Because the control signals are routed on the bottom signal layer between the (G)MCH and the first DIMM, 2.5 V flooding on the bottom signal layer is reduced and the control signals should be kept as short as possible. Also, because the control signals transition signal layers near the first DIMM, a via connecting the ground flood and ground plane on layer two and three should be placed as close as possible to each control signal transition via.

Resistor packs are acceptable for the parallel (Rtt) control termination resistors, but the control signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, address/command, or CPC address signals. Termination resistor packs for the control group must remain dedicated to control group signals, and not be used for any other signal groups.

The following figures and tables describe the recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

Figure 5-7. DIMM-A Control Signal Routing Topology (SCS_[1:0]#, SCKE_[1:0])

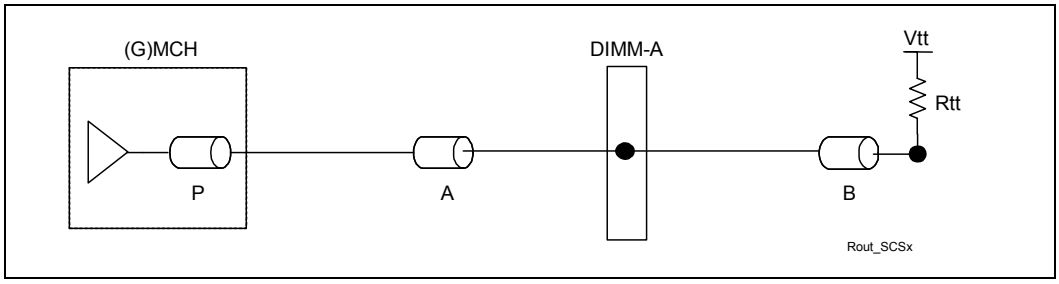


Figure 5-8. DIMM-B Control Signal Routing Topology (SCS_[3:2]#, SCKE_[3:2])

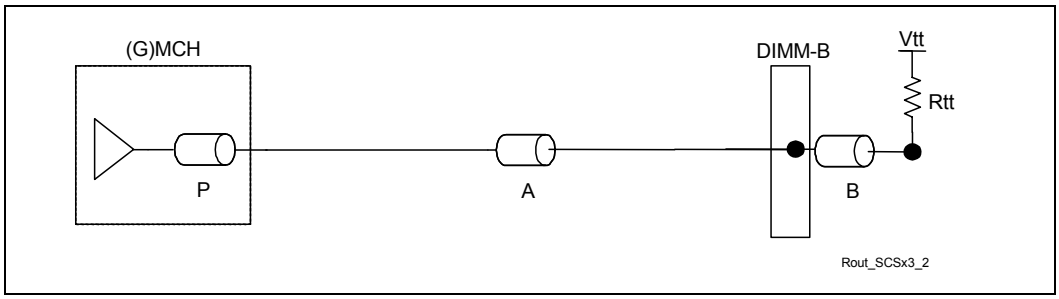
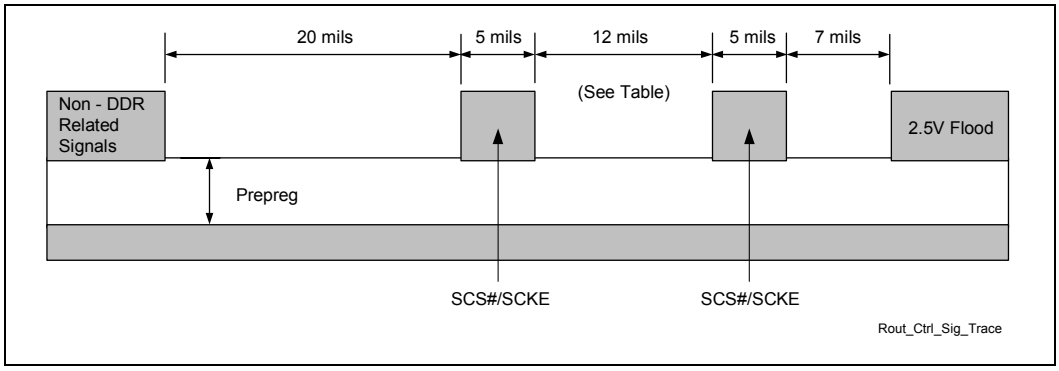


Table 5-6. Control Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	Control – SCS_[3:0]#, SCKE_[3:0]
Topology	Point-to-Point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	60Ω ± 15%
Nominal Trace Width	5 mils
Nominal Trace Spacing	• (G)MCH to first DIMM = 12 mils • Within DIMM Pin Field = 7 mils minimum • From DIMM to DIMM = 12 mils • Second DIMM to Rtt = 7 mils minimum
Group Spacing	Isolation spacing from non-DDR related signals = 20 mils
2.5 V Flood Spacing	Isolation from the 2.5 V flood on layer four = 7 mils minimum
(G)MCH Breakout Guidelines	5 mils width with 6-mil spacing for a max of 350 mils. Note: Use of breakout guidelines should be minimized.
Trace Length A – (SCS#/SCKE_[1:0]) – (G)MCH Signal Ball to DIMM Pins on **first DIMM**	Max = 3.5 inches The trace length from ball to first via should be within 50 mils. The trace length from the second via to the first DIMM should be within 500 mils.

Parameter	Routing Guidelines
Trace Length A – (SCS#/SCKE_[3:2]) – (G)MCH Signal Ball to DIMM Pins on **second DIMM**	Max = 4.0 inches The trace length from ball to first via should be within 50 mils. The trace length from the second via to the second DIMM should be within 1 inch.
Trace Length B – (SCS#/SCKE_[1:0]) – DIMM pins on **first DIMM** to Rtt Pad	Max = 1.4 inches
Trace Length B – (SCS#/SCKE_[3:2]) – DIMM pins on **second DIMM** to Rtt Pad	Max = 800 mils
Termination Resistor (Rtt)	56 Ω ± 5%
Maximum via Count per signal	4 vias (The number of vias over 2 should be minimized)
Length Tuning Method	SCS#/SCKE_[3:0] to SCMD_CLK/SCMD_CLK[5:0]# See Section 5.2.2.1

Figure 5-9. Control Signal Trace Width/Spacing Routing



5.2.2.1 Control Group Signal Length Matching Requirements

Tuning is required from (G)MCH ball to DIMM pin for control signals, and from (G)MCH pad to DIMM pin for clock signals. Clock Total Length includes clock package length.

- On an 845GE/845PE chipset based DDR platform, the total target differential clock length must be at least 3.4 inches longer than the longest routed control signal length for the associated DIMM.

  SCMDCLK/SCMDCLK# Total Length = X

  Associated SCS#/SCKE Max Length = Y, where Y ≤ (X – 3.4 inches)
  where Max Length = Longest (Motherboard trace length) for each associated DIMM

Length X to first and second DIMM include the (G)MCH Package Length P + Motherboard Trace Length A.

Length Y to first and second DIMM includes the Motherboard Trace Length A.

SCS#/SCKE motherboard trace length guideline A is described in Table 5-6. No length matching is required from the DIMM to the parallel termination resistors. Refer to Section 5.2.7 for (G)MCH clock package length data.

The diagram below depicts the length matching requirements between the control signals and the clock signals.

Figure 5-10. Control Signal to SCMDCLK/SCMDCLK# Trace Length Matching Requirements

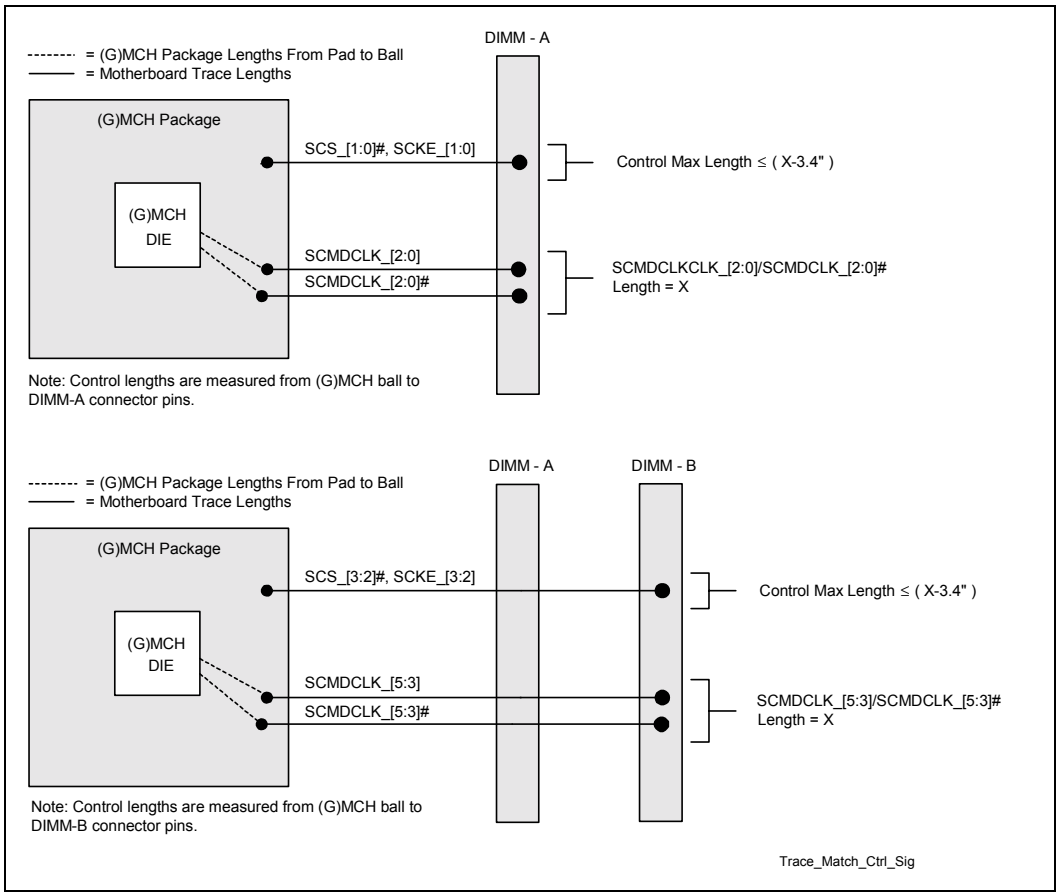


Figure 5-11. Control Group Bottom Layer to First DIMM Routing Example

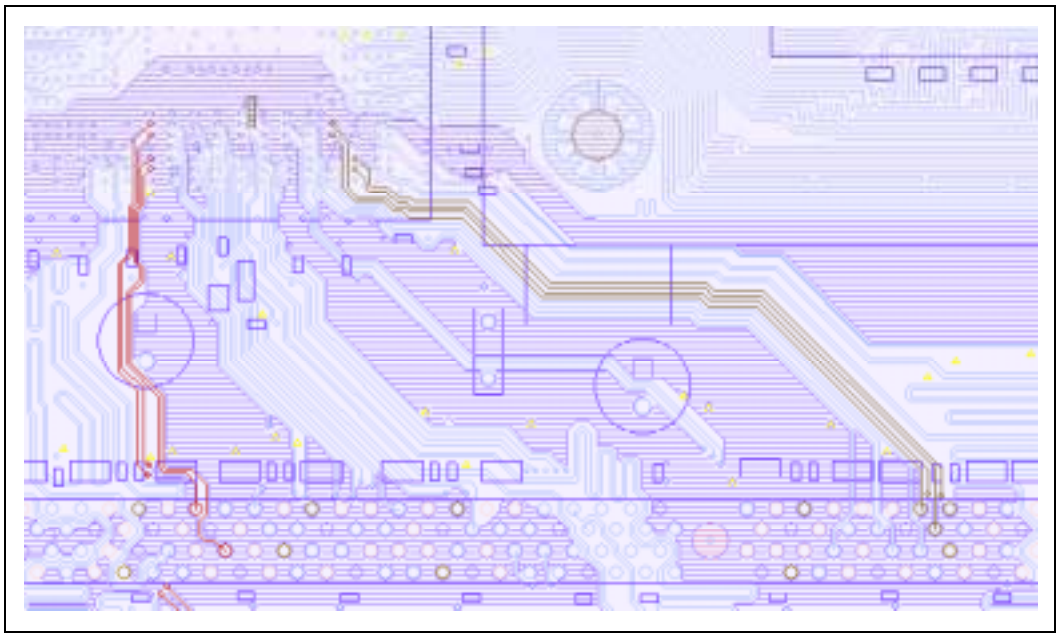


Figure 5-12. Control Group Bottom Layer Second DIMM Routing Example

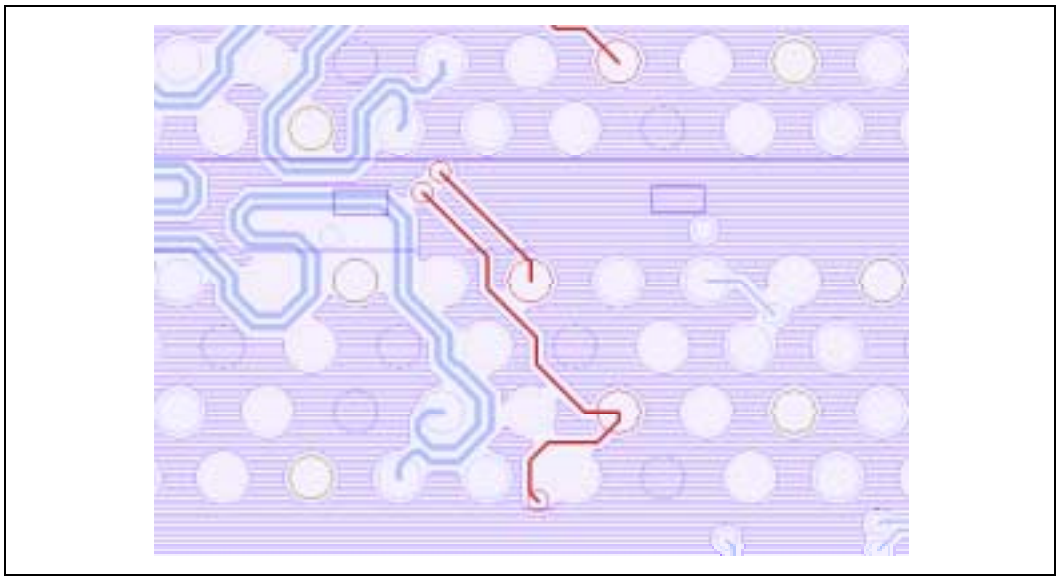
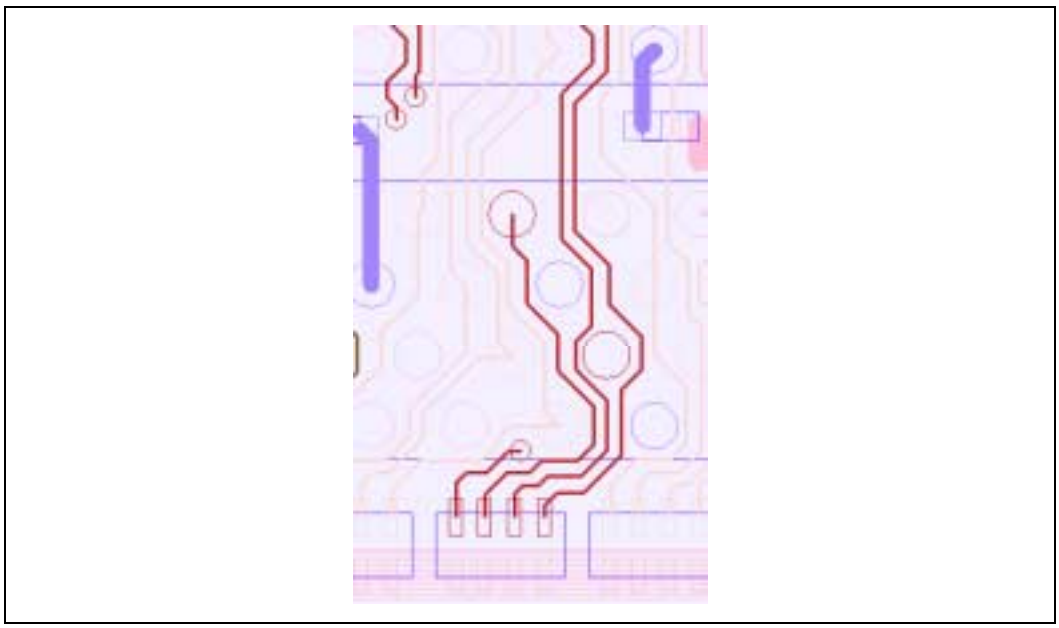


Figure 5-13. Control Group Top Layer Second DIMM to Termination Routing Example



5.2.3 Address/Command Signals — SMAA_[12:6, 3, 0], SBA_[1:0], SRAS#, SCAS#, SWE#

The (G)MCH address/command signals are source-clocked signals that include memory address signals SMAA_[12:6, 3, 0], SBA, SRAS#, SCAS#, and SWE#. The address signals (SMAA_/SMAB_[5,4,2,1]) are addressed in the next section. The address/command signals are tuned to SCMDCLK.

The (G)MCH system memory pin out has been optimized to breakout the address/command signals on the **bottom** signal layer and all address/command signals need to be routed on the same layer. They should transition from the top signal layer to the bottom signal layer under the (G)MCH. They should be routed on the bottom signal layer until the first DIMM or until they transition to the top signal layer within 500 mils before the first DIMM connector. Finally they should route from the DIMM connector pins to the parallel termination resistors at the end of the memory channel on the top signal layer.

Because the address/command signals are routed on the bottom signal layer between the (G)MCH and the first DIMM, 2.5 V flooding on the bottom signal layer is reduced, and the address/command signals should be kept as short as possible. Also, because the address/command signals transition signal layers near the first DIMM, a via connecting the ground flood and ground plane on layer two and three should be placed as close as possible to each control signal transition via.

Resistor packs are acceptable for the parallel (Rtt) address/command termination resistors, but address/command signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, control, or CPC address signals. Termination resistor packs for the address/command group must remain dedicated to address/command group signals, and not be used for any other signal groups.

The following figures and table describe the recommended topology and layout routing guidelines for the DDR-SDRAM address/command signals.

Figure 5-14. Address/Command Signal Routing Topology

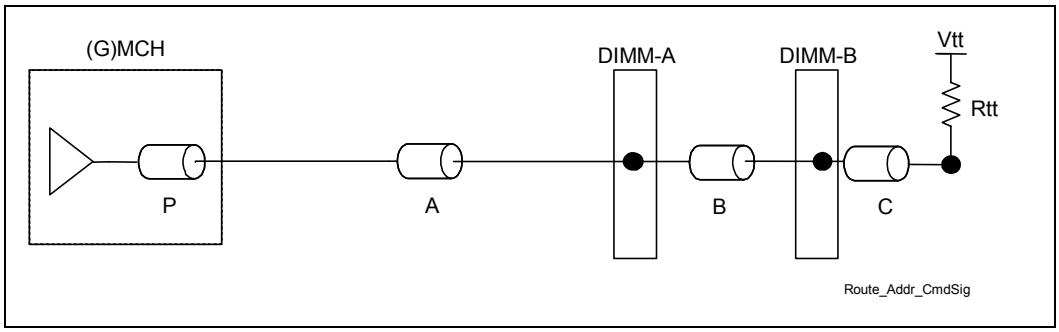
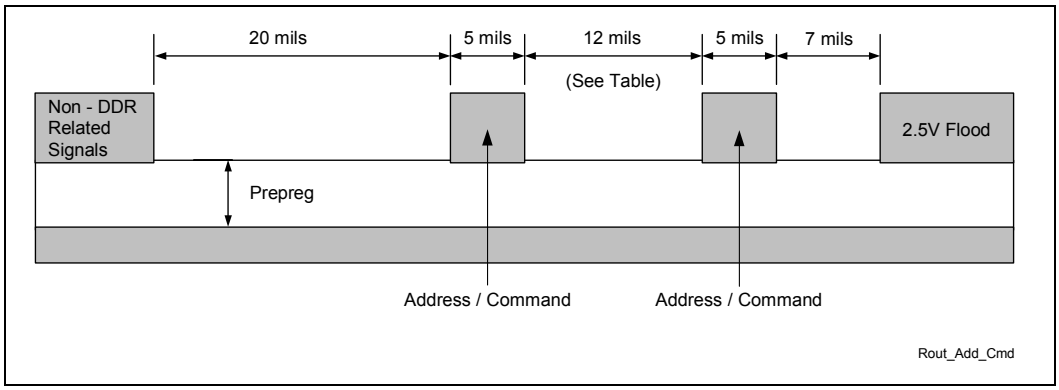


Table 5-7. Address/Command Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	Address/command – SMAA_[12:6, 3, 0], SBA_[1:0], SRAS#, SCAS#, SWE#
Topology	Daisy Chain
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Nominal Trace Width	5 mils
Nominal Trace Spacing from (G)MCH	• (G)MCH to first DIMM = 12 mils • Within DIMM Pin Field = 7 mils minimum • From DIMM to DIMM = 12 mils • Second DIMM to Rtt = 7 mils minimum
Group Spacing	Isolation spacing from non-DDR related signals = 20 mils
2.5 V Flood Spacing	Isolation from the 2.5 V flood on layer four = 7 mils minimum
(G)MCH Breakout Guidelines	5 mils width with 6-mil spacing for a max of 350 mils. **Note:** Use of breakout guidelines should be minimized.
Trace Length A – (G)MCH Signal Ball to first DIMM Pin	Max = 4.0 inches The trace length from ball to first via should be within 50 mils.
Trace Length B – DIMM Pin to DIMM Pin	Min = 400 mils Max = 600 mils
Trace Length C – Last DIMM Pin to Parallel Termination Resistor Pad	Max = 800 mils
Termination Resistor (Rtt)	56 Ω ± 5%
Maximum via Count per signal	4 vias (The number of vias over 2 should be minimized.)
Length Tuning Method	SMAA_[12:6,3,0], SBA_[1:0], SRAS#, SCAS#, SWE# to SCMDCLK_[5:0]/ SCMDCLK_[5:0]# per DIMM See Section 5.2.3.1

Figure 5-15. Address/Command Signal Trace Width/Spacing Routing



5.2.3.1 Address/Command Group Signal Length Matching Requirements

SMAA_[12:6,3,0], SBA_[1:0], SRAS#, SCAS#, SWE# require tuning to differential clock signals from (G)MCH ball to DIMM pin for address/command signals, and from (G)MCH pad to DIMM pin for clock signals. Clock Total Length includes clock package length.

On an 845GE/845PE chipset based DDR platform, the longest routed address/command signals must shorter than the total target differential clock for the associated DIMM by at least 1.9 inches.

SCMDCLK/SCMDCLK# Total Length = X

Associated Address/Command Max Length = Y, where Y ≤ (X – 1.9 inches)

where Max Length = Longest (Motherboard trace length) for each associated DIMM

Length X to first and second DIMM include the (G)MCH Package Length P + Motherboard Trace Length A.

Length Y to first DIMM includes the Motherboard Trace Length A.

Length Y to second DIMM include the Motherboard Trace Lengths A + B.

Address/command motherboard trace length guidelines A and B are documented in Table 5-7. No length matching is required from the DIMM to the parallel termination resistors. Refer to Section 5.2.7 for (G)MCH clock package length data.

Figure 5-16 shows the length matching requirements between the address/command signals and the clock signals.

Figure 5-16. Address/Command Signal to SCMDCLK/SCMDCLK# Trace Length Matching Requirements

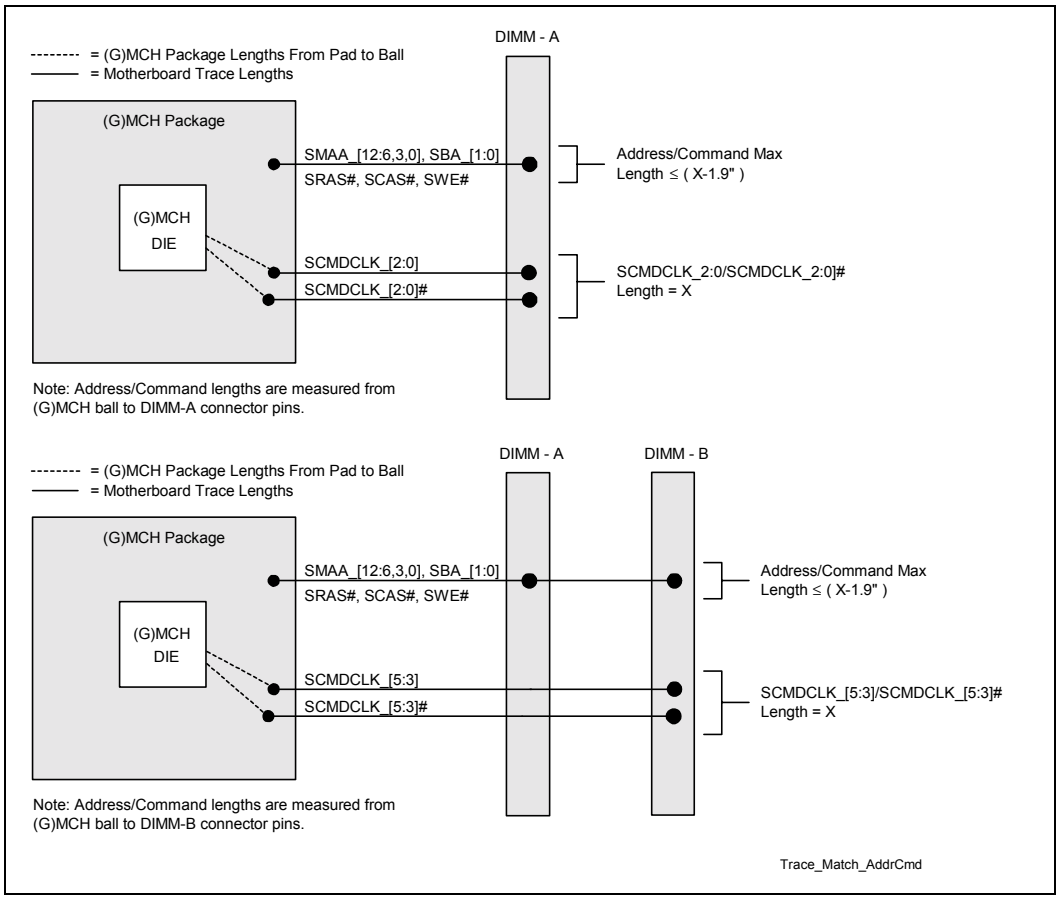


Figure 5-17. Address/Command Group Bottom Layer to First DIMM Routing Example

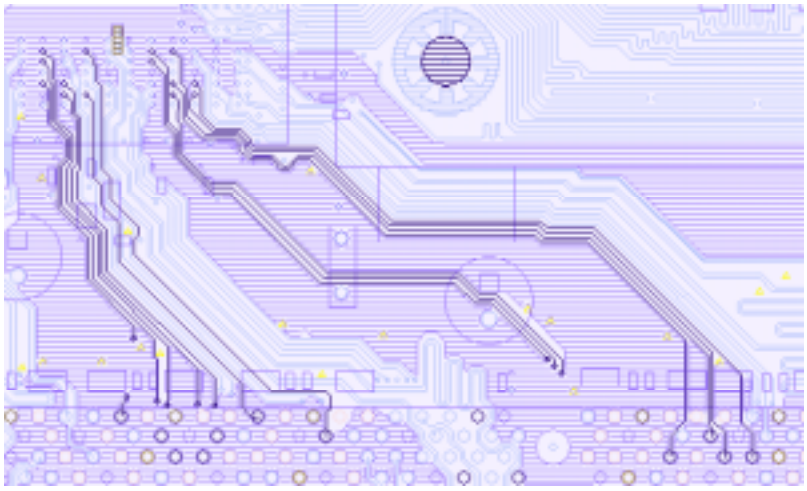
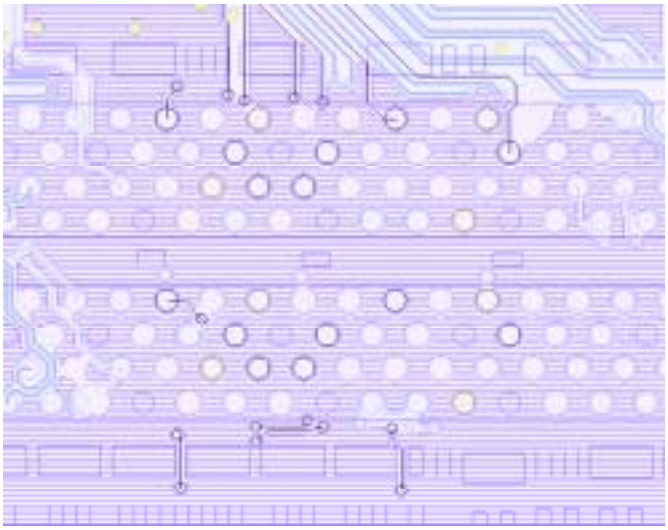


Figure 5-18. Address/Command Group Bottom Layer Routing Example



5.2.4 CPC Address Signals (SMAA_[5,4,2,1] and SMAB_[5,4,2,1])

The (G)MCH CPC address signals are source-clocked signals that include SMAA_[5,4,2,1] and SMAB_[5,4,2,1].

It is recommended to route CPC address signals before routing the differential clock signals. For more information, see the beginning of Section 5.2. The CPC address signals should be kept as short as possible, and must be tuned to SCMDCLK.

The (G)MCH system memory pin out has been optimized to breakout the CPC address signals on the **bottom** signal layer and all CPC address signals need to be routed on the same layer. Table 5-8 lists the correct SMAA/SMAB_[5,4,2,1] signal to DIMM mapping.

Table 5-8. CPC Address to DIMM Mapping

SMAA/SMAB	DIMM
SMAA_[5,4,2,1]	DIMM-A
SMAB_[5,4,2,1]	DIMM-B

Because CPC address signals are routed on the bottom signal layer, they should be kept as short as possible. A via connecting the ground flood and ground plane on layer two and three should be placed as close as possible to each control signal transition via.

Resistor packs are acceptable for the parallel (Rtt) CPC address termination resistors, but CPC address signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, control, or address/command signals. Termination resistor packs for the CPC address group must remain dedicated to CPC address group signals, and not be used for any other signal groups.

The following figures and table describe the recommended topology and layout routing guidelines for the DDR-SDRAM CPC address signals.

Figure 5-19. DIMM-A CPC Address Signal Routing Topology

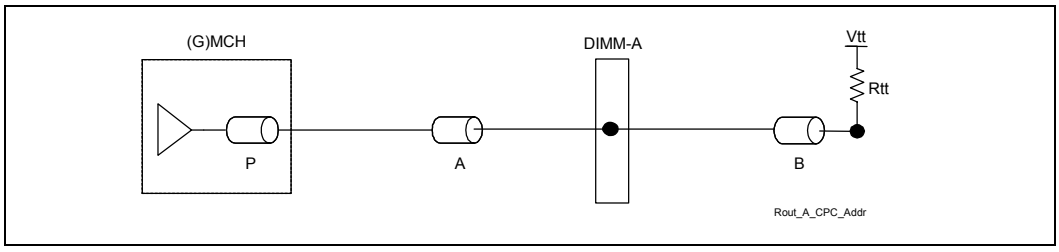


Figure 5-20. DIMM-B CPC Address Signal Routing Topology

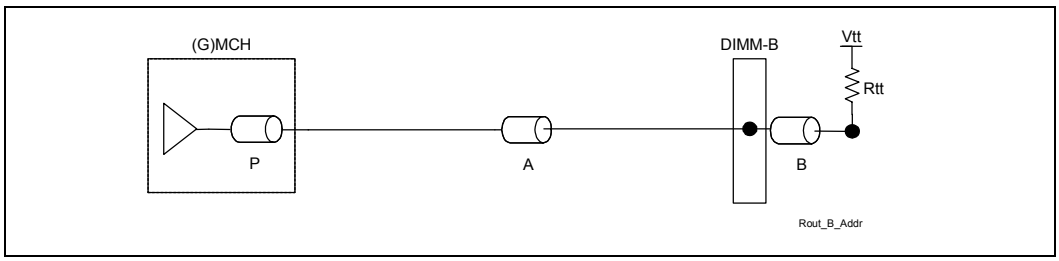
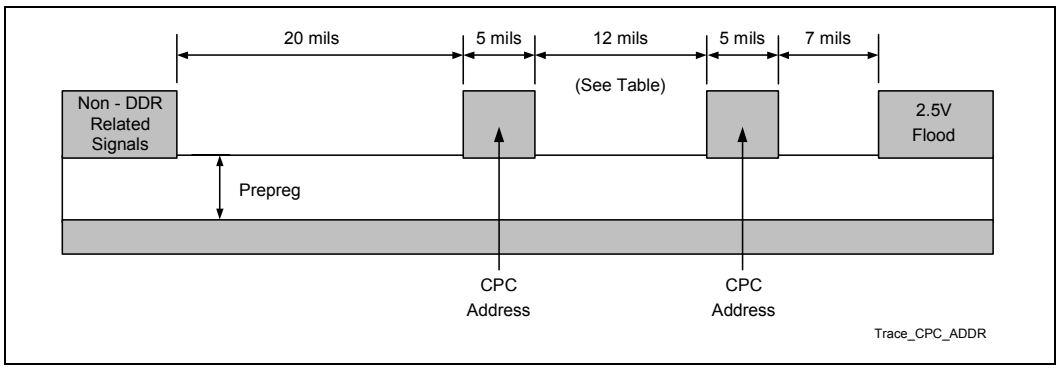


Table 5-9. CPC Address Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	CPC Address – SMAA_[5,4,2,1] and SMAB_[5,4,2,1]
Topology	Point-to-Point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Nominal Trace Width	5 mils
Nominal Trace Spacing	• (G)MCH to DIMM = 12 mils • Within DIMM Pin Field = 8 mils minimum • DIMM to Rtt = 8 mils minimum
Group Spacing	Isolation spacing from non-DDR related signals = 20 mils A maximum of 1 address/command signal can be routed adjacent to a CPC Address signal.
2.5 V Flood Spacing	Isolation from the 2.5 V flood on layer four = 7 mils minimum
(G)MCH Breakout Guidelines	5-mil width on 6-mil spacing up to the first 200 mils from ball. 5-mil width on 8-mil spacing up to an additional 550 mils after the first 200 mils from ball. **Note:** Use of breakout guidelines should be minimized.
Trace Lengths A – (SMAA_[5,4,2,1]) – (G)MCH Signal Ball to **first DIMM**	Max = 2.5 inches The trace length from ball to first via should be within 50 mils.
Trace Lengths A – (SMAB_[5,4,2,1]) – (G)MCH Signal Ball to **second DIMM**	Max = 3.0 inches The trace length from ball to first via should be within 50 mils.
Trace Length B – (SMAA_[5,4,2,1]) – **first DIMM** Pin to Parallel Termination Resistor Pad	Max = 1.4 inches
Trace Length B – (SMAB_[5,4,2,1]) – **second DIMM** Pin to Parallel Termination Resistor Pad	Max = 800 mils
Termination Resistor (Rtt)	33 Ω ± 5%
Maximum via Count per signal	4 vias (The number of vias over 2 should be minimized)
Length Tuning Method	SMAA_[5,4,2,1], SMAB_[5,4,2,1] to SCMDCLK_[5:0]/ SCMDCLK_[5:0]# for corresponding DIMM See Section 5.2.4.1 for details

Figure 5-21. CPC Address Signal Trace Width/Spacing Routing



5.2.4.1 CPC Address Group Signal Length Matching Requirements

Tuning is required from (G)MCH ball to DIMM pin for CPC address signals, and from (G)MCH pad to DIMM pin for clock signals. Clock Total Length includes clock package length.

- The total target differential clock must be at least 4.4 inches longer than the longest routed CPC address signal SMAA_[5,4,2,1] and SMAB_[5,4,2,1] for the associated DIMM.

  SCMDCLK/SCMDCLK# Total Length = X

  Associated CPC address Max Length = Y, where Y ≤ (X – 4.4 inches)

  where Max Length = Longest (Motherboard trace length) for each associated DIMM*

Length X to first and second DIMM include the (G)MCH Package Length P + Motherboard Trace Length A.

Length Y to first and second DIMM includes the Motherboard Trace Length A.

SMAA_[5,4,2,1] and SMAB_[5,4,2,1] motherboard trace length guidelines A are listed in Table 5-9. No length matching is required from the DIMM to the parallel termination resistors. Refer to Section 5.2.7 for (G)MCH clock package length data.

Note: It is recommended to route CPC address before routing the clocks. This tuning is applied to the longest first-DIMM signal, and is also applied to the longest second-DIMM signal. See the diagram below.

Figure 5-22 shows the length matching requirements between the CPC address signals and the clock signals.

Figure 5-22. CPC Address Signal to SCMDCLK/SCMDCLK# Trace Length Matching Requirements

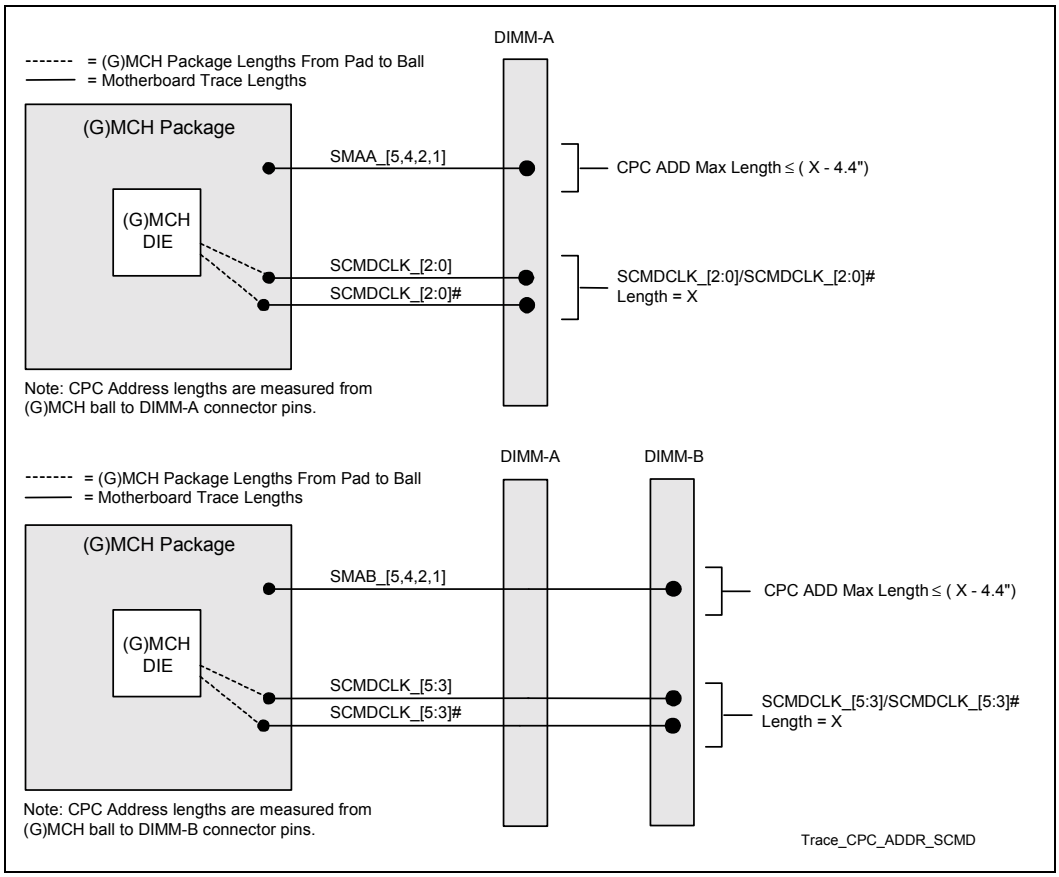


Figure 5-23. CPC Address Group Bottom Layer to First DIMM Routing Example

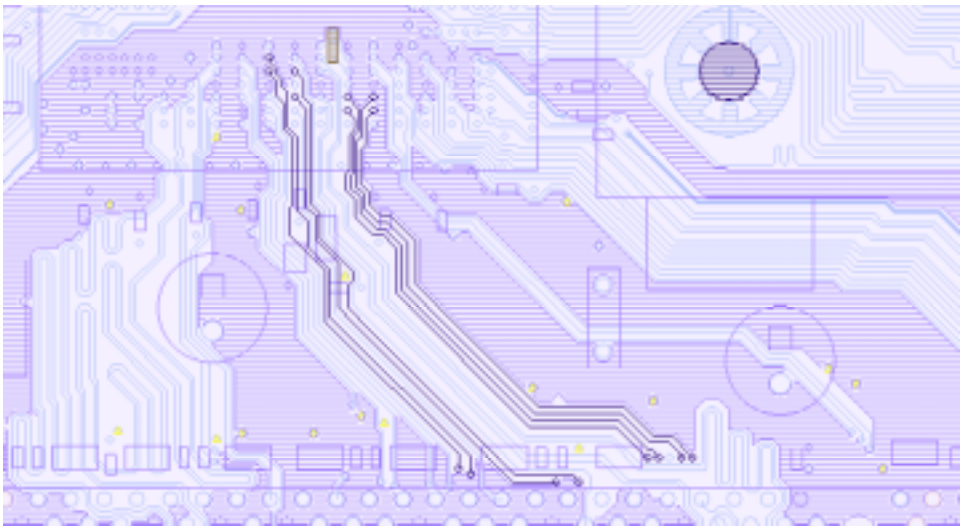
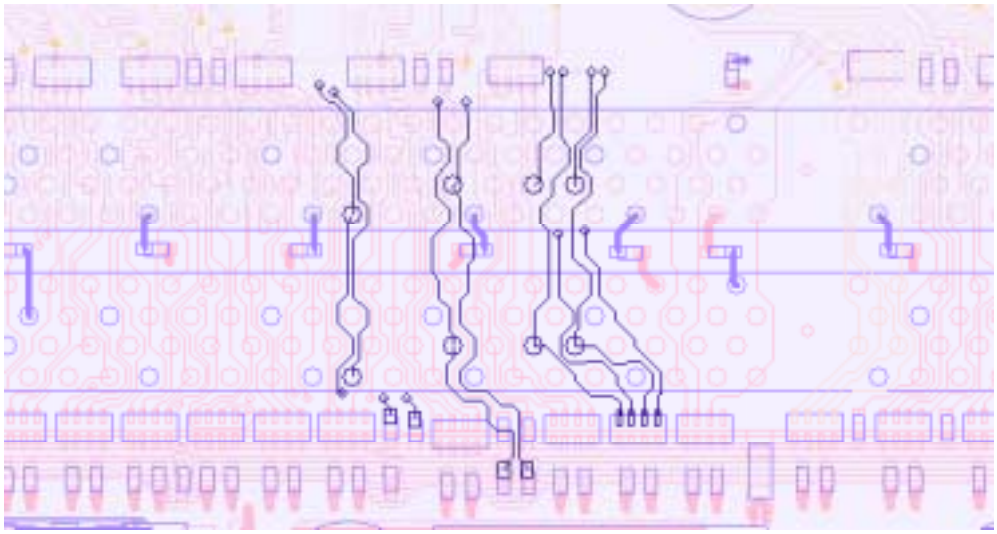


Figure 5-24. CPC Address Group Top Layer DIMM to Termination Routing Example



5.2.5 Clock Signals (SCMDCLK_[5:0], SCMDCLK_[5:0]#)

The (G)MCH clock signals include 6 differential clock pairs SCMDCLK_[5:0] and SCMDCLK_[5:0]#. The (G)MCH generates and drives these differential clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. Because the (G)MCH only supports unbuffered DDR DIMMs, three differential clock pairs are routed to each DIMM connector.

Before routing the clocks, refer to the beginning of Section 5.2 for the recommended routing order. This will help determine your target total clock length. Table 5-10 summarizes the clock signal mapping.

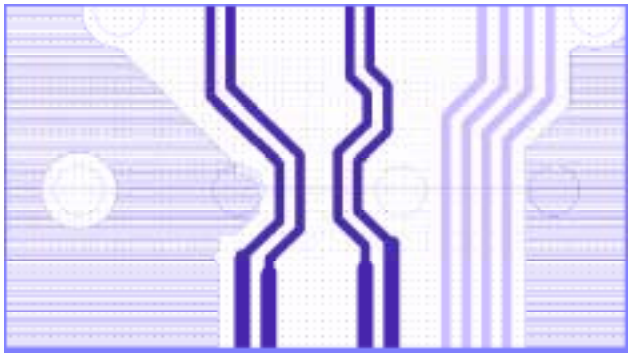
Table 5-10. Clock Signal DIMM Mapping

Signal	Relative To
SCMDCLK_[2:0], SCMDCLK_[2:0]#	DIMMA
SCMDCLK_[5:3], SCMDCLK_[5:3]#	DIMMB

All differential clock signals **must** be routed on the same layer. The (G)MCH system memory pin out has been optimized to breakout the clock signals on the **bottom** signal layer. The clock signals should transition from the top signal layer to the bottom signal layer under the (G)MCH and route referenced to ground on the bottom signal layer for the entire length to their associated DIMM pins.

DDR clocks can breakout of the (G)MCH with a reduced width for a max of 350 mil length, but use should be minimized where possible. Figure 5-25 shows an example of clock neck down in the (G)MCH region.

Figure 5-25. Clock Breakout Neck Down Example



The differential clock pairs must be routed differentially from the (G)MCH to their associated DIMM pins. They must maintain correct spacing of 5 mils **between** themselves to remain differential. In addition, they must maintain an isolation spacing of 20 mils **away** from other signals and itself (during serpentines). See Figure 5-26.

Figure 5-26. Differential Clock Spacing Example

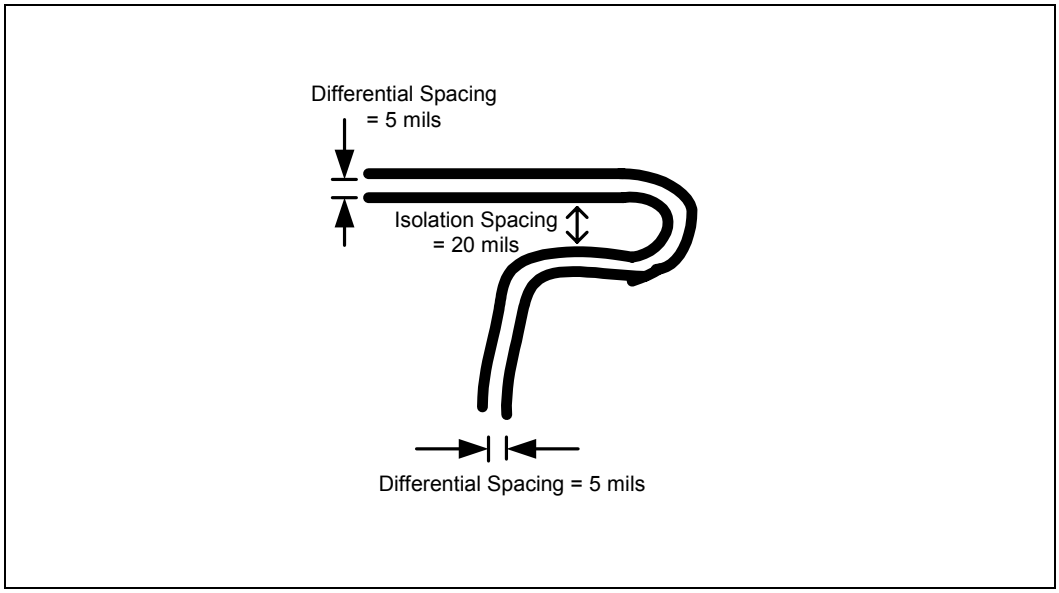


Table 5-11 summarizes a clock-signal-to-DIMM-pin mapping.

Table 5-11. DDR Clock Signal DIMM Pin Mapping

Signal	Relative To	DIMM Pin
SCMDCLK_0	DIMMA	137
SCMDCLK_0#	DIMMA	138
SCMDCLK_1	DIMMA	16
SCMDCLK_1#	DIMMA	17
SCMDCLK_2	DIMMA	76
SCMDCLK_2#	DIMMA	75
SCMDCLK_3	DIMMB	137
SCMDCLK_3#	DIMMB	138
SCMDCLK_4	DIMMB	16
SCMDCLK_4#	DIMMB	17
SCMDCLK_5	DIMMB	76
SCMDCLK_5#	DIMMB	75

System memory signal lengths must be tuned to the total target length of the clock pairs SCMDCLK/SCMDCLK#. Refer to the individual group signal length matching requirements found in their corresponding chapter for each system memory group. In addition, SCMDCLK must be tuned to SCMDCLK#.

Special attention must be paid upon how the clock signals would affect the 2.5 V flood to any of the 2.5 V DIMM pins because the clock signals are routed on the bottom signal. This is especially important in the area where the clocks must serpentine in or near the DIMM connector area. For an example of the clock routing on the bottom signal layer, see Figure 5-30 and Figure 5-31 (DDR Clock Bottom Signal Layer Routing Example 1 and 2).

There are no external termination resistors needed for SCMDCLK#/SCMDCLK. The following figures and table describe the recommended topology and layout routing guidelines for the DDR-SDRAM differential clocks.

Figure 5-27. DDR Clock Routing Topology (SCMDCLK_[2:0]/SCMDCLK_[2:0]#)

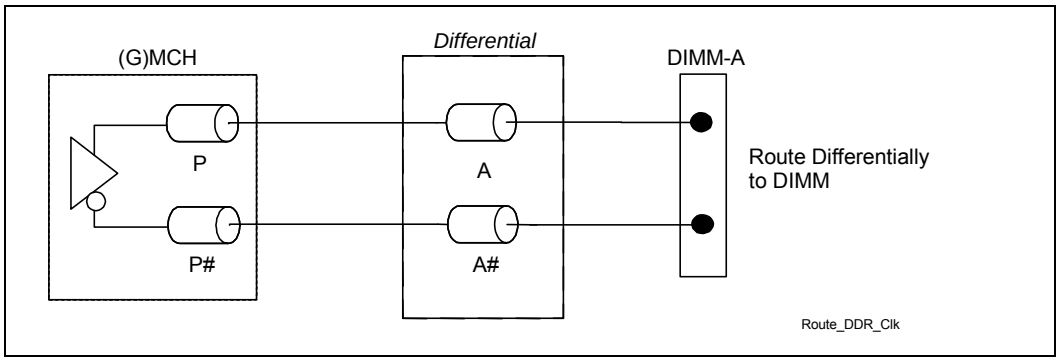


Figure 5-28. DDR Clock Routing Topology (SCMDCLK_[5:3]/SCMDCLK_[5:3]#)

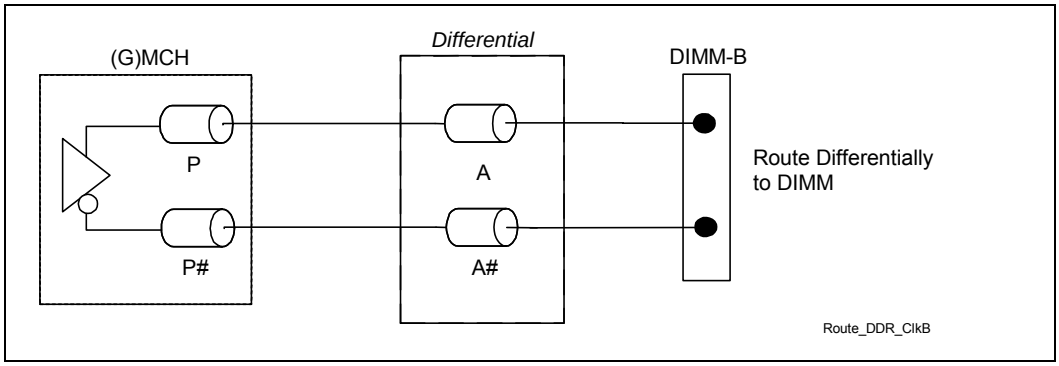


Table 5-12. Clock Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	Clocks – SCMDCLK_ [5:0], SCMDCLK_ [5:0]#
Topology	Point-to-Point
Reference Plane	Ground Referenced
Nominal Characteristic Trace Impedance (Zo)	Differential (odd-mode) = 70 Ω
Nominal Trace Width	8 mils
Differential Trace Spacing - spacing between SCMDCLK and its SCMDCLK#	5 mils
Group Spacing	Isolation spacing from another DDR signal group = 20 mils Isolation spacing from non-DDR related signals = 20 mils
Serpentine Spacing	Isolation spacing from itself when serpentining = 20 mils
2.5 V Flood Spacing	Isolation from the 2.5 V flood on layer four = 10 mils minimum
(G)MCH Breakout Guidelines	5-mil width with 5-mil differential spacing with a minimum of 5- mil isolation from any other signals for a max length of 350 mils Note: Use of breakout guidelines should be minimized.
Total Trace Length P + A - SCMDCLK_ [2:0] - (G)MCH Signal Pad to first DIMM	Max = 7.4 inches The trace length from ball to via should be within 50 mils. See Section 5.2.7 for package length P.
Total Trace Length P + A - SCMDCLK_ [5:3] - (G)MCH Signal Pad to second DIMM	Max = 7.9 inches The trace length from ball to via should be within 50 mils. See Section 5.2.7 for package length P.
Total Clock Length Relationship - between first DIMM and second DIMM	(P + Y) = ((P + X) + 0.5 inch) where (P+X) = Total target clock length to first DIMM where (P+Y) = Total target clock length to second DIMM
Maximum via Count per signal	1 via (for breakout to bottom layer)
Length Tuning Method	• SCMD_CLK length to SCMD_CLK# length, within ± 10 mils • All 3 clock pairs to each DIMM are equal in length, within ± 10 mils where length includes package length compensation (P + A) See Section 5.2.5.1 for details

Figure 5-29. Clock Signal Trace Width/Spacing Routing

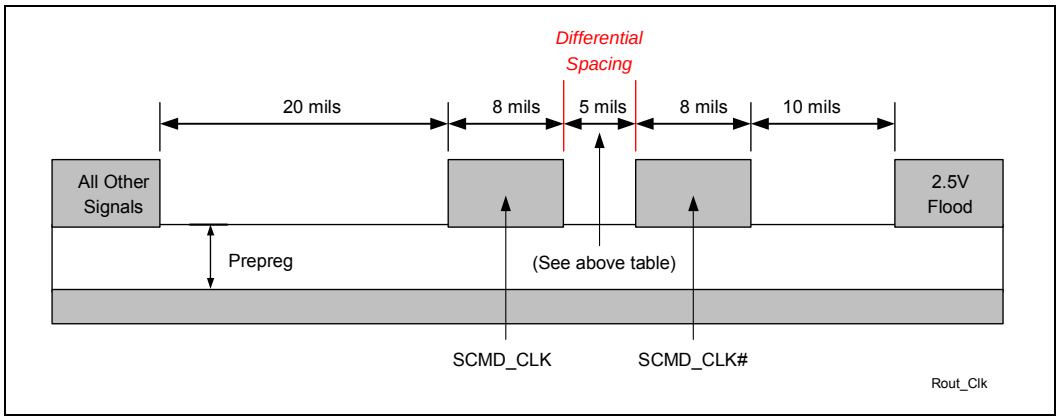


Figure 5-30. DDR Clock Bottom Signal Layer Routing Example 1

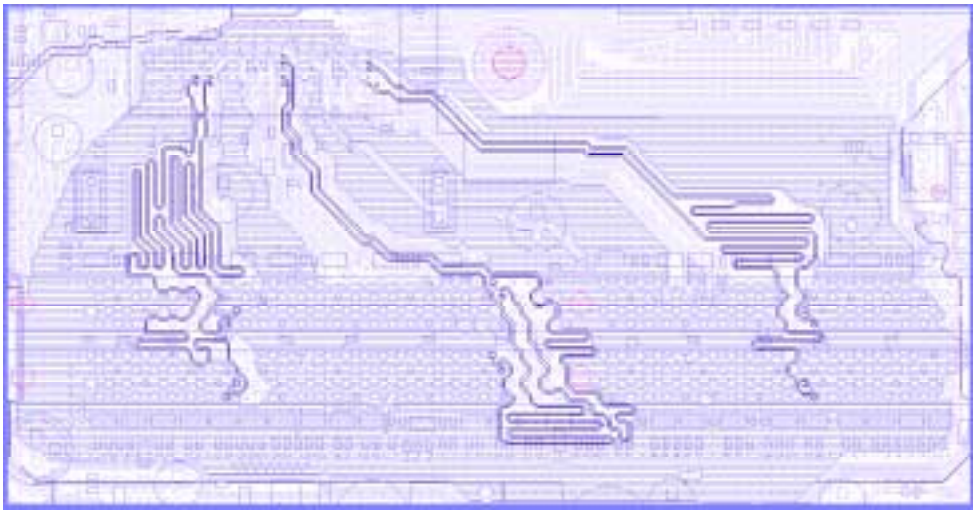


Figure 5-31. DDR Clock Bottom Signal Layer Routing Example 2

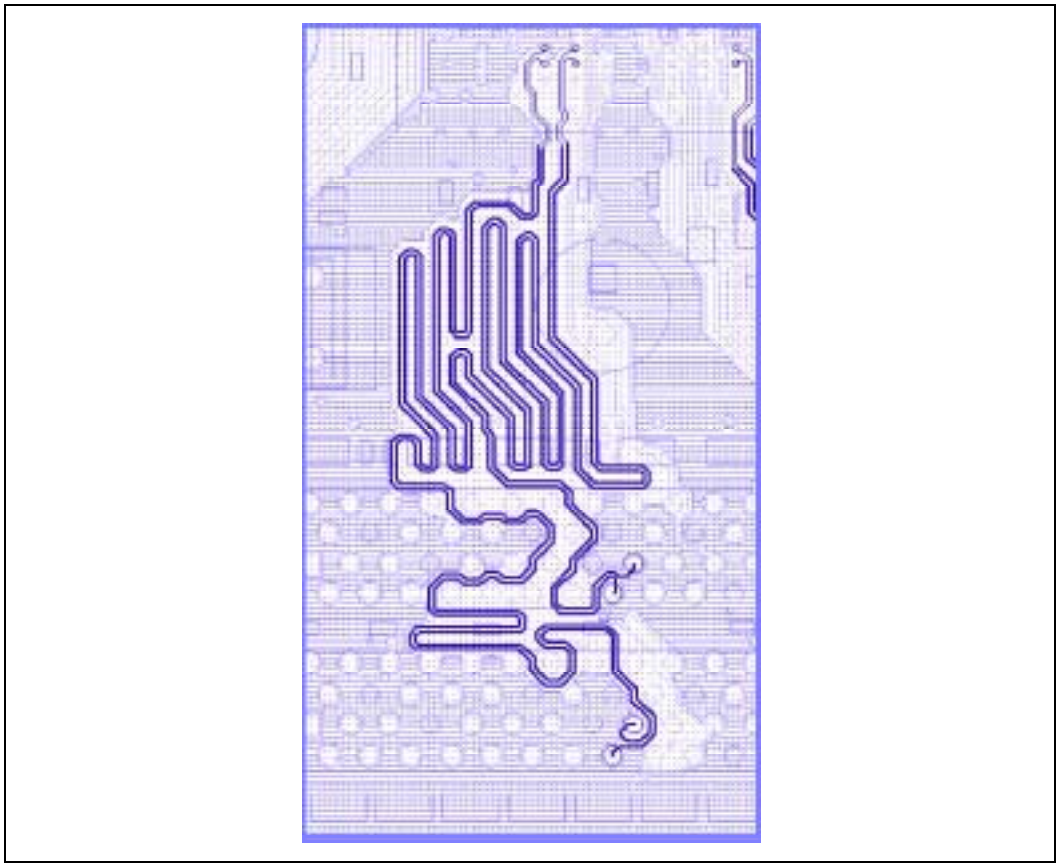


Figure 5-32. DDR Clock Bottom Signal Layer Routing Example 3

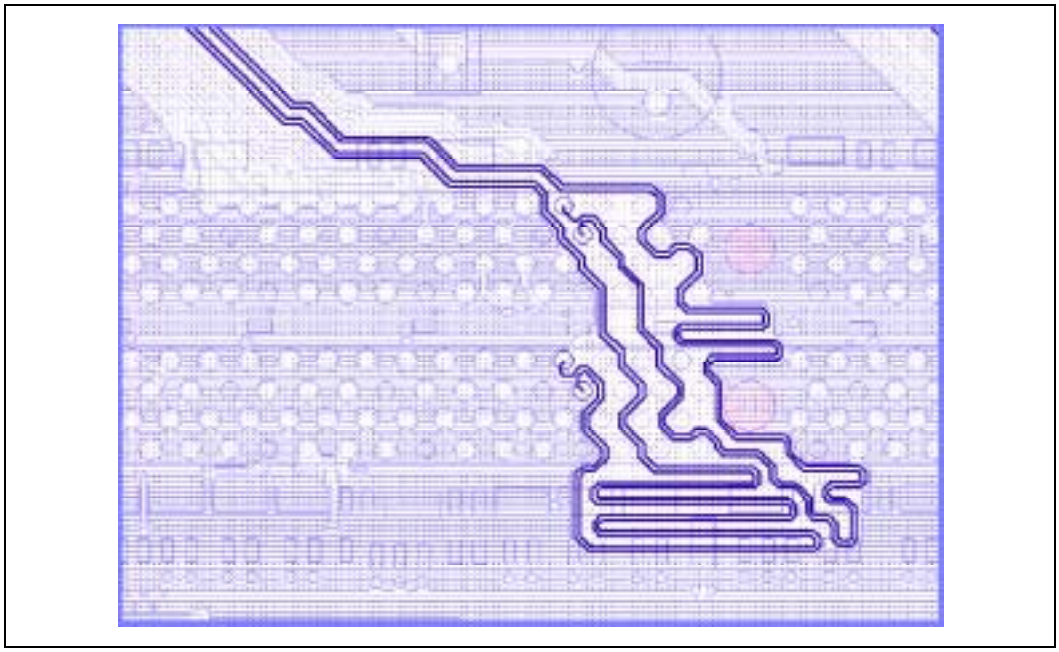
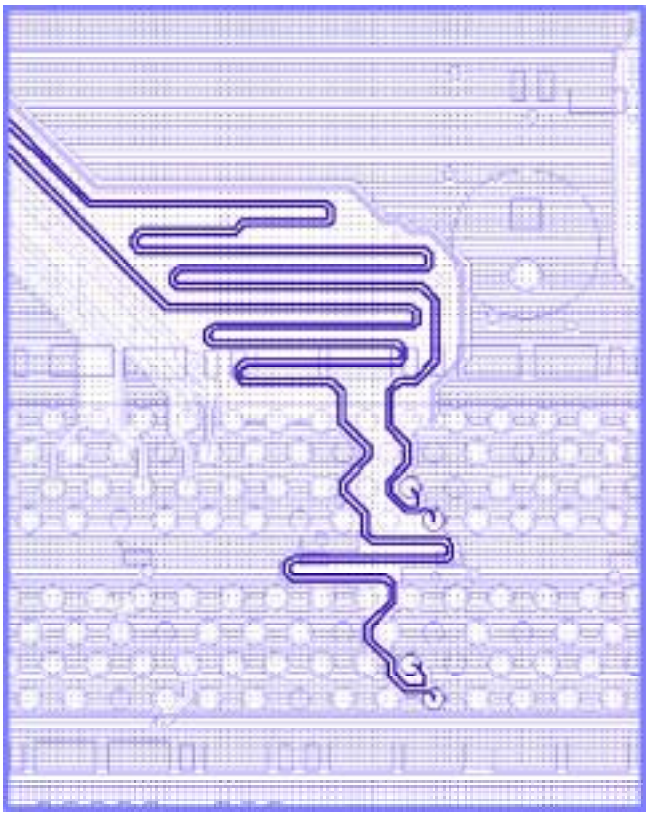


Figure 5-33. DDR Clock Bottom Signal Layer Routing Example 4



5.2.5.1 Clock Group Signal Length Matching Requirements

Clock length matching is required for every clock and its complement, and between clock pairs associated to the same DIMM. See Figure 5-34.

- Every SCMD_CLK must be length matched to its complement SCMDCLK# from (G)MCH pad to the pins of the DIMM connector. (P + A = P# + A#)
- All clock pairs to the first DIMM (SCMDCLK_[2:0]/SCMDCLK_ [2:0]#) are matched to each other from (G)MCH internal pad to the pin of the first DIMM connector.
- All clock pairs to the second DIMM (SCMDCLK_[5:3]/SCMDCLK_[5:3]#) are matched to each other from the (G)MCH internal pad to the pin of the second DIMM connector.
- The total target clock length to second DIMM is 0.5 inch longer than the total target clock length to first DIMM.

Table 5-13. Clock Group Signal Length Matching Requirements

First DIMM:	Second DIMM:
SCMDCLK_0 = SCMDCLK_0# = SCMDCLK_1 = SCMDCLK_1# = SCMDCLK_2 = SCMDCLK_2#	SCMDCLK_3 = SCMDCLK_3# = SCMDCLK_4 = SCMDCLK_4# = SCMDCLK_5 = SCMDCLK_5#

Length SCMDCLK to first and second DIMM include the (G)MCH Package Length P + Motherboard Trace Length A.

Length SCMDCLK# to first and second DIMM include the (G)MCH Package Length P# + Motherboard Trace Length A#.

SCMDCLK and SCMDCLK# (G)MCH internal package trace lengths can be found in Section 5.2.7.

Clock pairs can be matched within ± 10 mils and associated DIMM clocks can be matched within ± 10 mils

Note that the total target differential clock lengths must also be tuned with the data strobes, address/command, CPC address, and control signals lengths. For more information, see their corresponding length matching sections. The diagram below depicts the length matching requirements for the differential clock signals.

Figure 5-34. SCMDCLK_x to SCMDCLK_x# Trace Length Matching Requirements

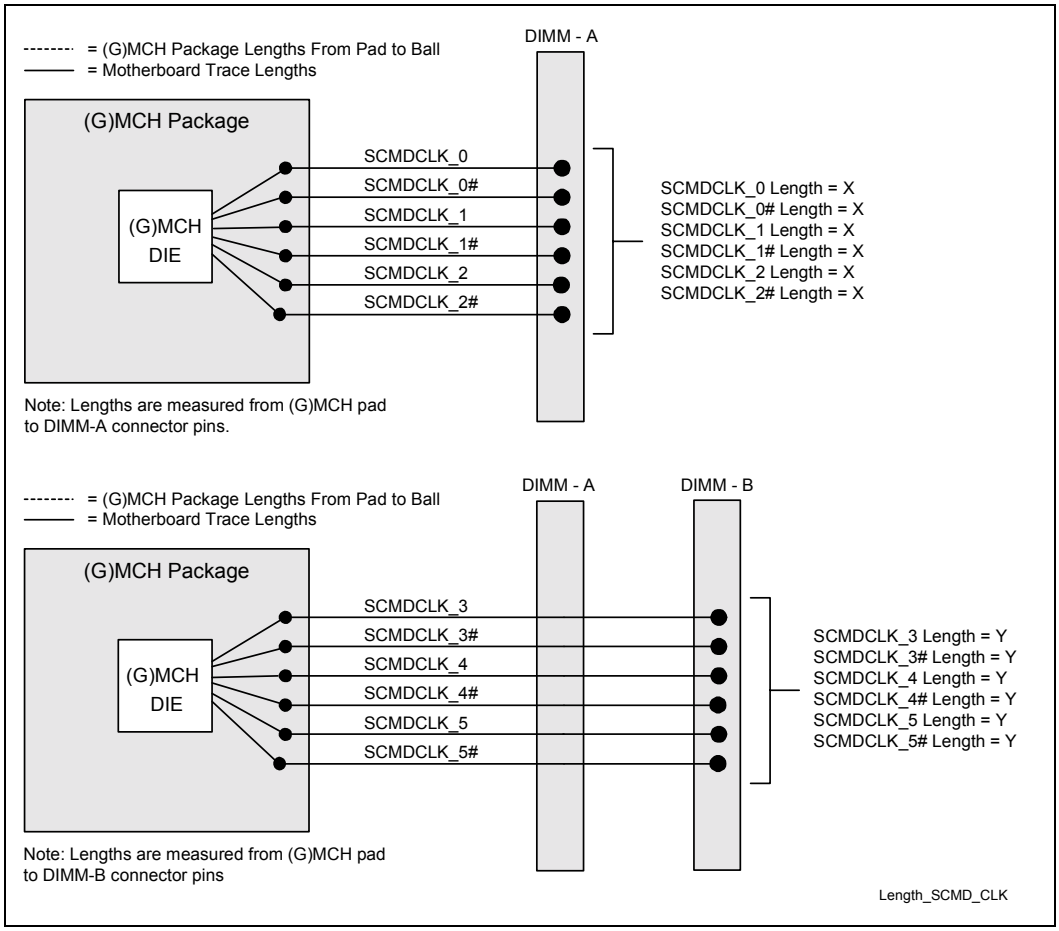
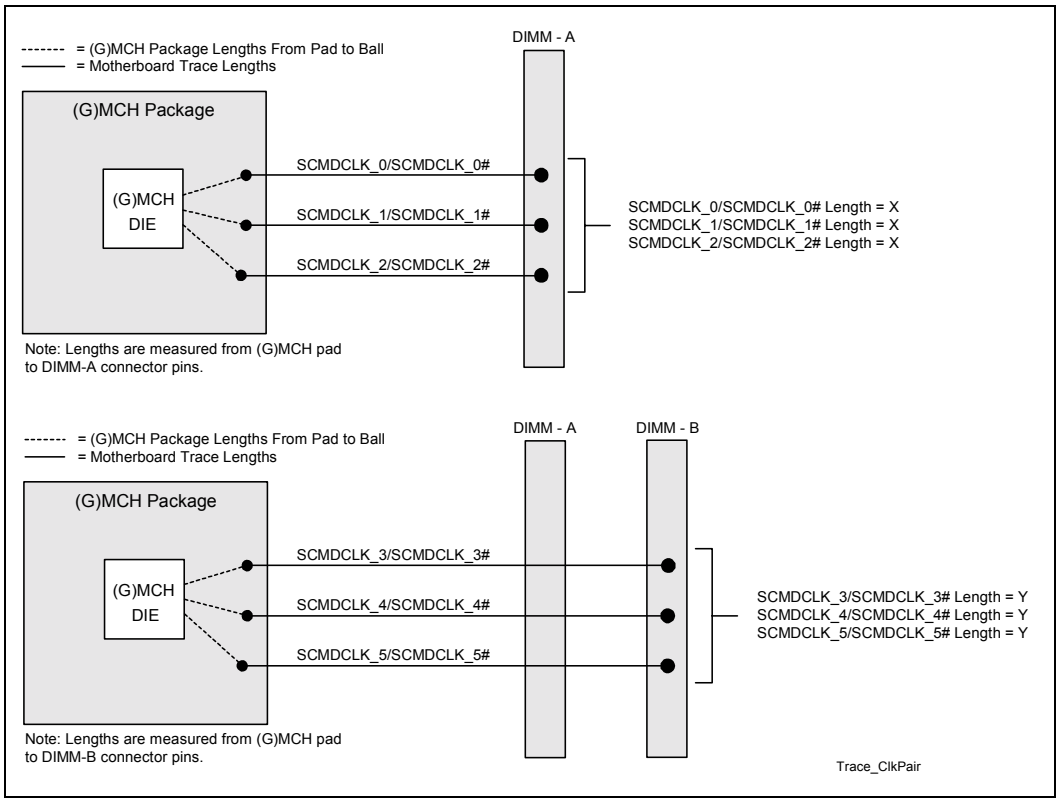


Figure 5-35. Clock Pair Trace Length Matching Requirements



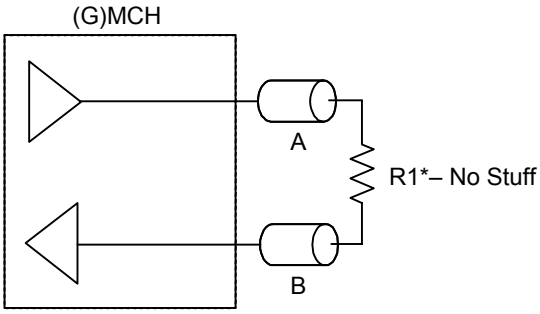
5.2.6 Feedback (SRCVEN_OUT#, SRCVEN_IN#)

On the 845GE/845PE chipset platform, two signals on the (G)MCH facilitate testing of "receive enable". A very short trace on the motherboard to each end of the resistor site can be routed from each of the two balls. The resistor site can be located on the bottom side, routed directly from layer one to layer four through two vias.

The implementation of the receive enable resistor site is optional. If a resistor site is implemented, the resistor site must not be populated connecting SRCVEN_OUT# to SRCVEN_IN#. The resistor site should be left unpopulated.

The following figures and table describe the recommended topology and layout routing guidelines for the DDR-SDRAM feedback signal.

Figure 5-36. DDR Feedback (SRCVEN_OUT# / SRCVEN_IN#) Routing Topology



Notes:
1. Leave resistor site R1 unpopulated.
2. The site can be placed on the bottom side of the motherboard.

DDR_FB

Table 5-14. Feedback SRCVEN_OUT# and SRCVEN_IN#

Parameter	Routing Guidelines
Signal Group	Feedback – SRCVEN_OUT# and SRCVEN_IN#
Topology	Point-to-Point, w/ resistor site
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Nominal Trace Width	5 mils
Group Spacing	Isolation from another DDR signal group = 10 mils minimum Isolation from non-DDR related signal = 10 mils minimum
Trace Length Limits – A	Max = 100 mils
Trace Length Limits – B	Max = 100 mils
Maximum via Count per signal	2
Resistor - R1	Not populated

5.2.7 Intel® (G)MCH DDR Signal Package Lengths

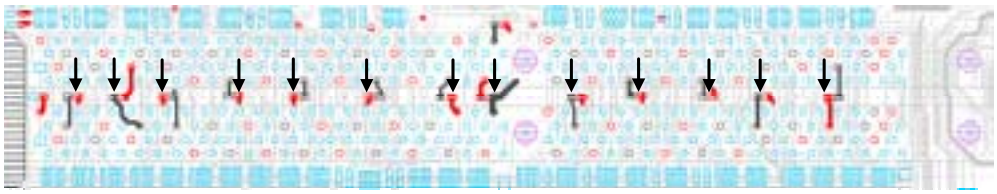
Signal	Intel® (G)MCH Ball	Package Length (Inches)	Signal	Intel® (G)MCH Ball	Package Length (Inches)
Data Signals					
SDQ_0	AN4	0.652	SDQ_32	AR22	0.575
SDQ_1	AP2	0.758	SDQ_33	AP22	0.578
SDQ_2	AT3	0.802	SDQ_34	AP24	0.508
SDQ_3	AP5	0.680	SDQ_35	AT26	0.614
SDQ_4	AN2	0.754	SDQ_36	AT22	0.638
SDQ_5	AP3	0.747	SDQ_37	AT23	0.616
SDQ_6	AR4	0.710	SDQ_38	AT25	0.619
SDQ_7	AT4	0.815	SDQ_39	AR26	0.638
SDQ_8	AT5	0.728	SDQ_40	AP26	0.621
SDQ_9	AR6	0.665	SDQ_41	AT28	0.657
SDQ_10	AT9	0.650	SDQ_42	AR30	0.743
SDQ_11	AR10	0.646	SDQ_43	AP30	0.630
SDQ_12	AT6	0.780	SDQ_44	AT27	0.645
SDQ_13	AP6	0.642	SDQ_45	AR28	0.588
SDQ_14	AT8	0.684	SDQ_46	AT30	0.707
SDQ_15	AP8	0.603	SDQ_47	AT31	0.783
SDQ_16	AP10	0.576	SDQ_48	AR32	0.725
SDQ_17	AT11	0.628	SDQ_49	AT32	0.752
SDQ_18	AT13	0.723	SDQ_50	AR36	0.830
SDQ_19	AT14	0.621	SDQ_51	AP35	0.762
SDQ_20	AT10	0.662	SDQ_52	AP32	0.652
SDQ_21	AR12	0.610	SDQ_53	AT33	0.801
SDQ_22	AR14	0.561	SDQ_54	AP34	0.712
SDQ_23	AP14	0.591	SDQ_55	AT35	0.804
SDQ_24	AT15	0.589	SDQ_56	AN36	0.762
SDQ_25	AP16	0.479	SDQ_57	AM36	0.825
SDQ_26	AT18	0.563	SDQ_58	AK36	0.759
SDQ_27	AT19	0.613	SDQ_59	AJ36	0.736
SDQ_28	AR16	0.556	SDQ_60	AP36	0.794
SDQ_29	AT16	0.588	SDQ_61	AM35	0.736
SDQ_30	AP18	0.472	SDQ_62	AK35	0.681
SDQ_31	AR20	0.578	SDQ_63	AK34	0.667

Signal	Intel® (G)MCH Ball	Package Length (Inches)	Signal	Intel® (G)MCH Ball	Package Length (Inches)
Data Mask Signals					
SDM_0	AP4	0.681	SDM_4	AT24	0.631
SDM_1	AR8	0.660	SDM_5	AP28	0.561
SDM_2	AP12	0.541	SDM_6	AR34	0.766
SDM_3	AR18	0.529	SDM_7	AL34	0.662
Data Strobe Signals					
SDQS_0	AR2	0.780	SDQS_4	AR24	0.564
SDQS_1	AT7	0.704	SDQS_5	AT29	0.670
SDQS_2	AT12	0.628	SDQS_6	AT34	0.823
SDQS_3	AT17	0.579	SDQS_7	AL36	0.744
Clock Signals					
SCMDCLK_0	AL21	0.387	SCMDCLK_0#	AK22	0.387
SCMDCLK_1	AN11	0.722	SCMDCLK_1#	AP11	0.720
SCMDCLK_2	AM34	0.826	SCMDCLK_2#	AL33	0.827
SCMDCLK_3	AP21	0.520	SCMDCLK_3#	AN21	0.523
SCMDCLK_4	AP9	0.793	SCMDCLK_4#	AN9	0.779
SCMDCLK_5	AP33	0.899	SCMDCLK_5#	AN34	0.898

5.3 System Memory Bypass Capacitor Guidelines

Discontinuities in the DDR signal return paths will occur when the signals transition between the motherboard and the DIMMs. To account for this ground to 2.5 V discontinuity, a minimum of nine 0603 0.1 µF high-frequency bypass capacitors are required between the DIMMs to help minimize any anticipated return path discontinuities that will be created. The bypass capacitors connect to 2.5 V and ground. A wide trace should connect to a via that transitions to the ground cutout on layer two and to the ground plane on layer three. The ground via should be placed as close to the ground pad as possible. A wide trace should connect the 2.5 V side of the capacitor to a via that transitions to the 2.5 V plane on layer four, then to the closest 2.5 V DIMM pin on either DIMM. These 2.5 V traces should be distributed evenly between the two DIMMs as shown in Figure 5-37. Finally, the 2.5 V via should be placed as close to the 2.5 V pad as possible.

Figure 5-37. DDR-DIMM Bypass Capacitor Placement



5.4 Power Delivery

The following guidelines are recommended for an 845GE/845PE chipset DDR system memory design. The main focus of these (G)MCH guidelines is to minimize signal integrity problems and improve the power delivery of the (G)MCH system memory interface and the DDR-DIMMs.

5.4.1 2.5 V Power Delivery Guidelines

The 2.5 V power for the (G)MCH system memory interface and the DDR-DIMMs is delivered on layer one and on layer four around the DDR signals. Special attention must be paid to the 2.5 V copper flooding to ensure proper (G)MCH and DIMM power delivery. This 2.5 V flood must extend from the (G)MCH 2.5 V power vias all the way to the 2.5 V DDR voltage regulator and its bulk capacitors. The 2.5 V DDR voltage regulator must connect to the 2.5 V flood with a minimum of six vias, and the DIMM connector 2.5 V pins as well as the (G)MCH 2.5 V power vias must connect to the 2.5 V copper flood on layer four.

The copper flooding to the (G)MCH should include at least one finger on layer 1 and five fingers on layer 4 to allow for the routing of the DDR signals and for optimal (G)MCH power delivery. The copper fingers must be kept as wide as possible to keep the loop inductance path from the 2.5 V voltage regulator to the (G)MCH at a minimum. In the areas where the copper flooding necks down under the (G)MCH make sure to keep these neck down lengths as short and wide as possible.

Table 5-15 lists the minimum width requirements for the copper fingers going from the DIMM high-frequency capacitors to the (G)MCH high-frequency capacitors. It also details the minimum neck down width requirements that the copper fingers can be reduced to for short distances from the (G)MCH high-frequency capacitors through the (G)MCH ball field. **These neck down lengths must be kept as short as possible.** The width requirements listed below must be met at a minimum by the copper fingers to have good 2.5 V power delivery to the (G)MCH. Table 5-15 references Figure 5-40, which has a total of five copper fingers for (G)MCH 2.5 V power delivery. The copper finger numbering starts from the far left and moves to the right.

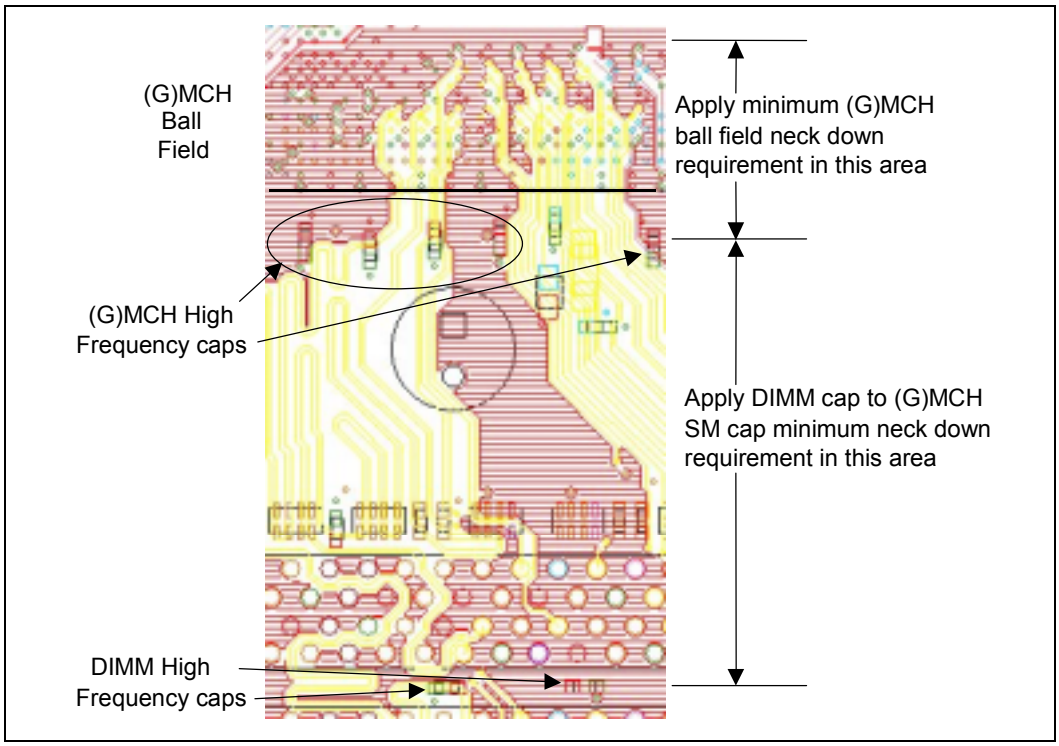
Table 5-15. Minimum 2.5 V Copper Finger Width Requirements

Cu Finger	Min Width (From DIMM Caps to (G)MCH SM Caps)	Min Neck Down Widths (Within (G)MCH Ball Field)
Layer 1	130 mils	100 mils
Layer 4 Number 1 (Left most finger)	150 mils	115 mils
Layer 4 Number 2	135 mils	40 mils
Layer 4 Number 3	90 mils	60 mils
Layer 4 Number 4	100 mils	50 mils
Layer 4 Number 5 (Right most finger)	80 mils	30 mils

To meet DC power delivery requirements to the (G)MCH, the layer one shape must connect to the following VCCSM balls: all in row AL (except AL37), all in row AK (except AK33), all in row AJ, all in row AH, all in row AG, and all in row AD. Also, to meet the DC requirements, the left most finger on layer 4 (finger 1) must have vias placed by the following VCCSM balls (vias may be shared between balls): AU5, AU9, AP7, AL2, AL3, AL4, AL5, AL7, AL9, AK2, AK3, AK4, AK6, AK8, AJ3, AJ4, AJ5, AJ7, AJ9, AJ15, AJ19, AJ23, AJ27, and all in row AD.

To meet AC power delivery requirements, fingers that have capacitors placed in them (see recommendations later in this section) should meet the minimum width as stated above, but the width should be maximized as much as possible.

Figure 5-38. Example Implementation of Finger Width Requirement



The 2.5 V copper flooding must encompass all the DIMM 2.5 V pins. Figure 5-40 is an example of the layer four 2.5 V power delivery to the DIMMs.

Because the DDR control, address/command, CPC address, and clock signals are routed on the bottom signal layer between the (G)MCH and the first DIMM, the 2.5 V copper flooding on layer four is limited. To maximize the copper flooding, these signals should be kept as short as possible.

Finally, the eight (G)MCH 2.5 V high-frequency decoupling capacitors, located on the top signal layer, should have their 2.5 V via placed directly over and connected to a 2.5 V copper finger. For guidelines on the (G)MCH 2.5 V high-frequency decoupling capacitors, reference Section 5.4.2.1.

The following figures show examples of the 2.5 V power delivery copper flood for the (G)MCH and the DIMMs.

Figure 5-39. Layer One 2.5 V Power Delivery

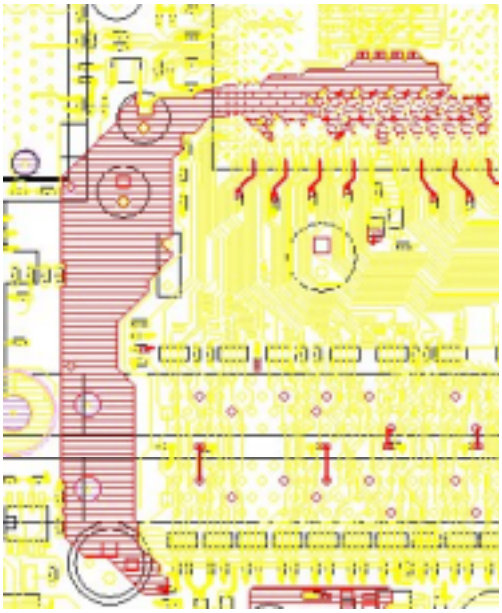
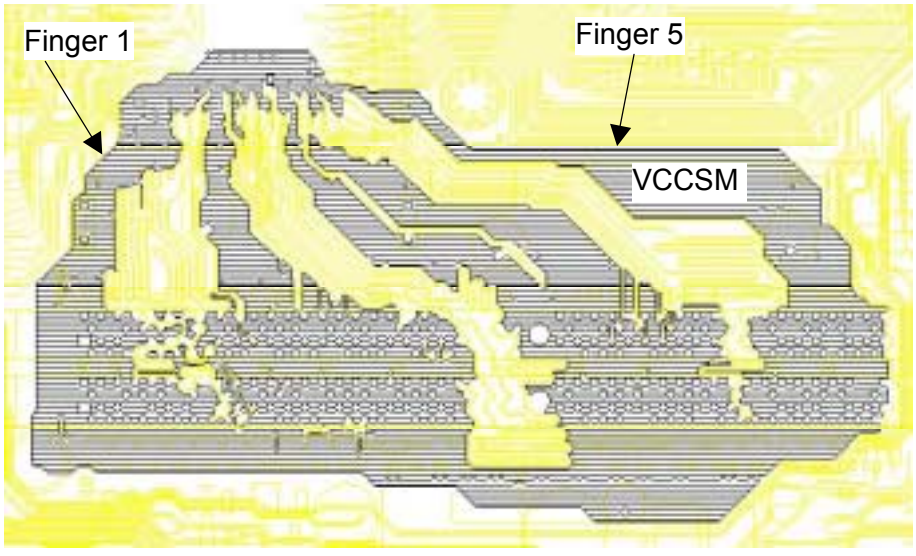


Figure 5-40. Layer Four 2.5 V Power Delivery



Maximize the amount of copper that is flooded on layer one and layer four from the 2.5 V VREG through the DIMMs and to the (G)MCH. Care must be taken to ensure that enough copper is poured after the tuning of the DDR clocks and other signals.

5.4.2 Intel® (G)MCH System Memory Interface Decoupling Requirements

5.4.2.1 Intel® (G)MCH System Memory High-Frequency Decoupling

Every (G)MCH ground and power ball in the system memory interface should have its own via, where possible. For 2.5 V high-frequency decoupling, a minimum of eight 0603 0.1 µF high-frequency capacitors are required, and must be within 100 mils of the (G)MCH package. These capacitors must be placed perpendicular to the (G)MCH, when appropriate, with the 2.5 V side of the capacitors facing the (G)MCH. The trace from the power end of the capacitor should be as wide as possible and it must connect to a 2.5 V power ball on the outer row of balls on the (G)MCH. The power balls that require a capacitor are: AL37, AU5, AU9, AU13, AU17, AU25, AU29, and AU33. Each capacitor should have two vias placed directly over a 2.5 V copper finger that is located on layer four. One via should be placed within 25 mils of the capacitor pads, while the other via should be placed within 25 mils of the power ball. If the trace from the solder ball to the capacitor is less than 100 mils, one of the vias may be omitted. The ground end of the capacitors must connect to the ground cutout on layer two and to the ground plane on layer three through a via that is placed within 25 mils of the capacitor pad. The trace from the ground via to the capacitor pad must be as wide as possible. The following figures represent the (G)MCH DDR 2.5 V high-frequency decoupling requirements.

Figure 5-41. Intel® (G)MCH DDR 2.5 V Decoupling Picture

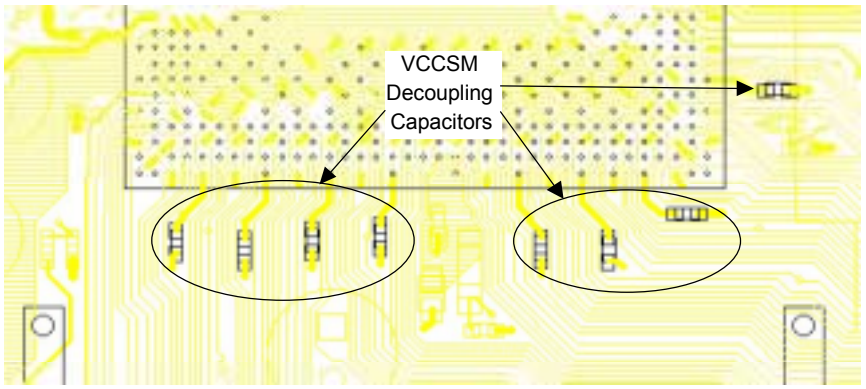


Figure 5-42. Intel® (G)MCH DDR 2.5 V Decoupling Capacitor Routing Alignment

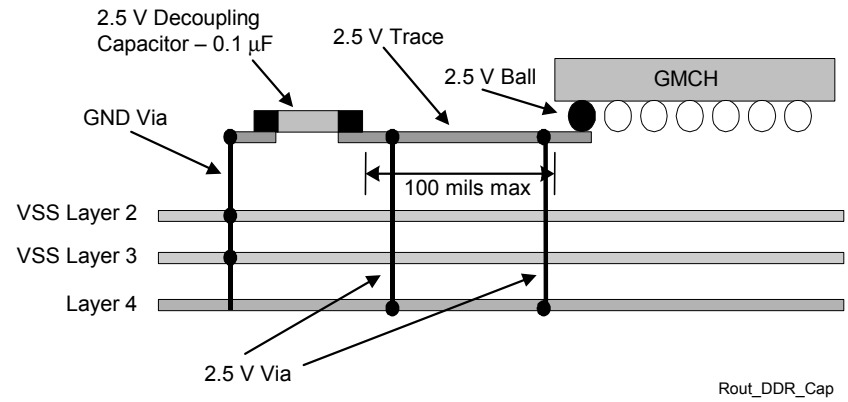


Table 5-16. Intel® (G)MCH System Memory Decoupling Capacitor Requirements

Parameter	Guideline
Capacitor number	Eight 0603 0.1 µF MLC capacitors – placed with trace leading to the following balls: AL37, AU5, AU9, AU13, AU17, AU25, AU29, and AU33
Capacitor placement	Within 100 mils of the (G)MCH
Capacitor pad to power ball trace width	Route as wide as possible minimum width of 18 mils
Power vias	Two vias, one placed within 25 mils of the capacitor pad and one placed within 25 mils of the power ball
Capacitor pad to ground via trace width	Route as wide as possible with a minimum width of 18 mils
Ground via	Placed within 25 mils of the capacitor pad

NOTE: If the trace from the power ball to the capacitor pad is less than 100 mils, one of the vias may be omitted.

5.4.2.2 Intel® (G)MCH System Memory Low-Frequency Bulk Decoupling

The (G)MCH system memory interface requires low-frequency bulk decoupling. Place four 100 µF electrolytic capacitors between the (G)MCH and the first DIMM connector. The power end of the capacitors must connect to 2.5 V on layer one or layer four, and the ground end of the capacitors must connect to ground on layer two and three. These capacitors are in addition to the bulk decoupling required by the 2.5 V regulator (regulator bulk decoupling is design specific).

Figure 5-43. Shared Intel® (G)MCH/DIMM 2.5 V Bulk Decoupling Example

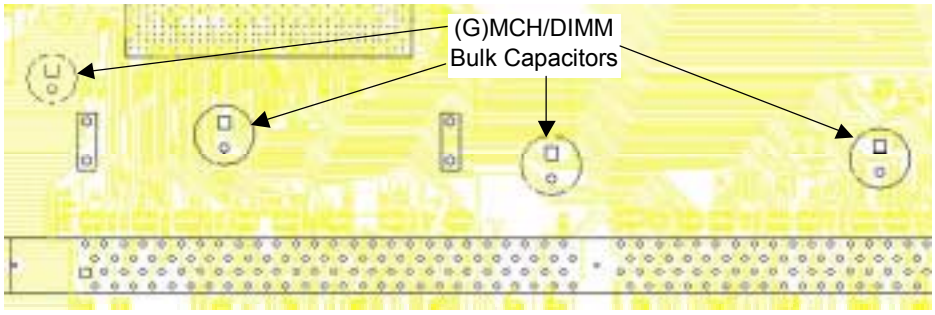


Table 5-17. Intel® (G)MCH System Memory Bulk Capacitor Requirements

Parameter	Guideline
Capacitor number	Four 100 µF capacitors
Capacitor placement	Evenly placed between the (G)MCH and the DIMMs with one of the 100 µF capacitors connecting to the top layer copper flood.

5.4.3 DDR-DIMM Decoupling Requirements

The DDR DIMMs require bulk decoupling in addition to what is required by the (G)MCH. Place three more 100 µF capacitors DIMM connectors as shown in Figure 5-44. The power end of the capacitors must connect to 2.5 V on layer one and layer four, and the ground end of the capacitors must connect to ground on layer two and three.

Figure 5-44. DDR DIMM 2.5 V Bulk Decoupling Example

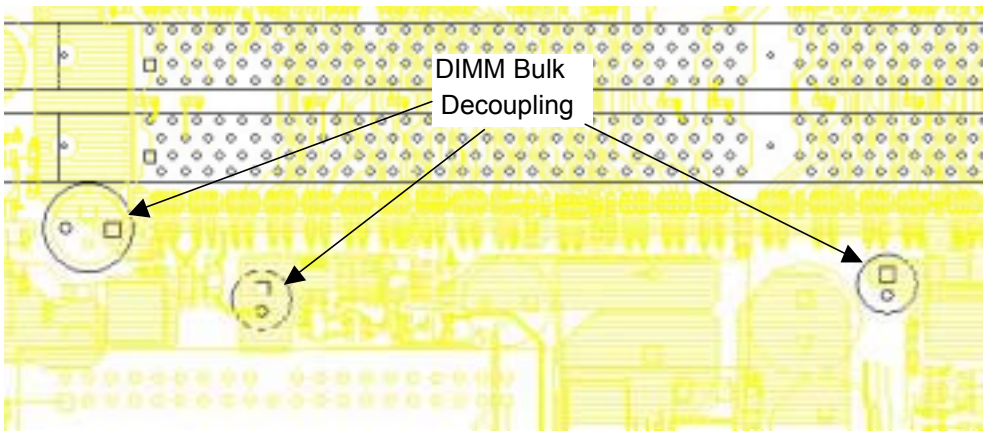


Table 5-18. Intel® (G)MCH System Memory Bulk Capacitor Requirements

Parameter	Guideline
Capacitor number	Three 100 µF capacitors
Capacitor placement	Place along bottom side of the DIMMs as shown in Figure 5-44.

5.4.4 DDR Reference Voltage

The DDR system memory reference voltage (VREF) is used by the DDR-SDRAM devices to compare the input signal levels of the data, command, and control signals, and is also used by the (G)MCH to compare the input data signal levels. VREF must be generated as shown in Figure 5-45. It should be generated from a typical resistor divider using 1%-tolerance resistors. The VREF resistor divider should be placed no further than 1.0 inch from the DIMMs. Additionally, VREF must be decoupled locally at each DIMM connector and at the (G)MCH. Finally, the VREF signal should be routed with as wide a trace as possible (12 mils minimum width) and isolated from other signals with a minimum of 12 mils spacing (during breakout from the (G)MCH a minimum of 7-mil spacing can be maintain for a maximum length of 350 mils).

Figure 5-45. DDR VREF Generation Example Circuit

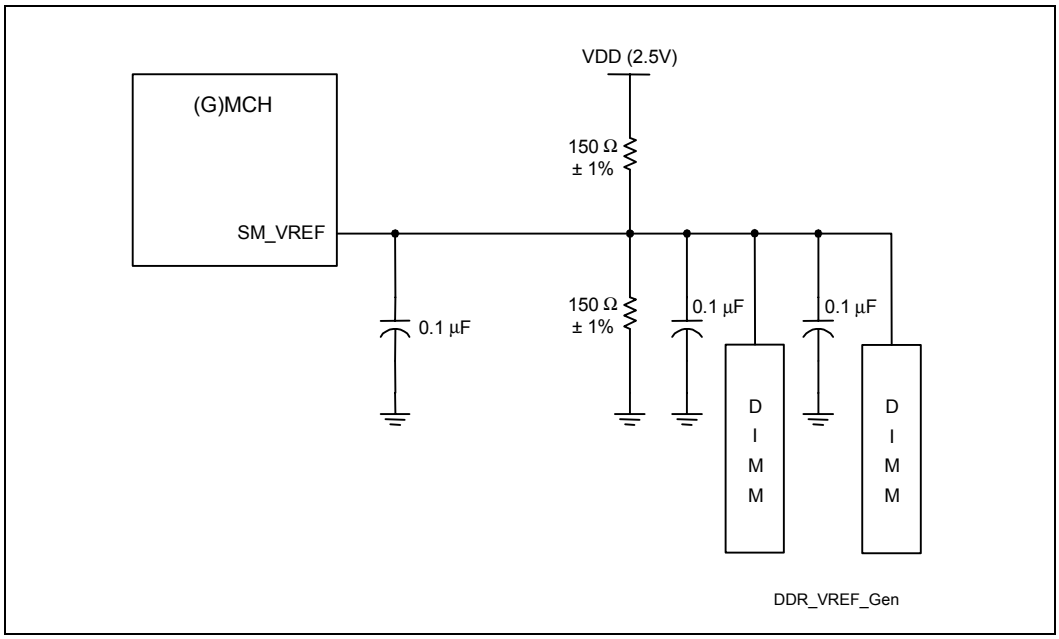


Table 5-19. DDR VREF Generation Requirements

Parameter	Guideline
VREF Routing	Minimum 12-mils wide and separated from other traces with a minimum 12 mils spacing, except during breakout, which is allowed 7-mil spacing to other signals for no more than 350 mils
Voltage Divider	Place resistor divider consisting of two resistors (50 Ω – 150 Ω, 1%) within 1.0 inch of the DIMM sockets. Note: Both resistors must be the same, have the same resistance value, and be 1%).
Decoupling requirements	Three 0603 0.1 µF capacitors
Decoupling placement	Place one decoupling cap at each of the DIMM sockets and one decoupling cap at the (G)MCH

5.4.5 DDR SMRCOMP Resistive Compensation

The (G)MCH uses a compensation signal to adjust the system memory buffer characteristics over temperature, process, and voltage variations. The DDR system memory (SMRCOMP) must be connected to the DDR voltage (2.5 V) through a 60.4 Ω ± 1% resistor and connected to ground through a 60.4 Ω ± 1% resistor. A 0603 0.1 µF decoupling capacitor connected to 2.5 V and to ground should be used as illustrated in Figure 5-46. Do not connect any capacitor to the SMRCOMP signals. Place the capacitors within 1.0 inch of the (G)MCH package. The compensation signal and the power trace should be routed with a minimum of 12-mils wide and isolated from other signals with a minimum of 10-mils spacing.

Figure 5-46. DDR SMRCOMP Resistive Compensation

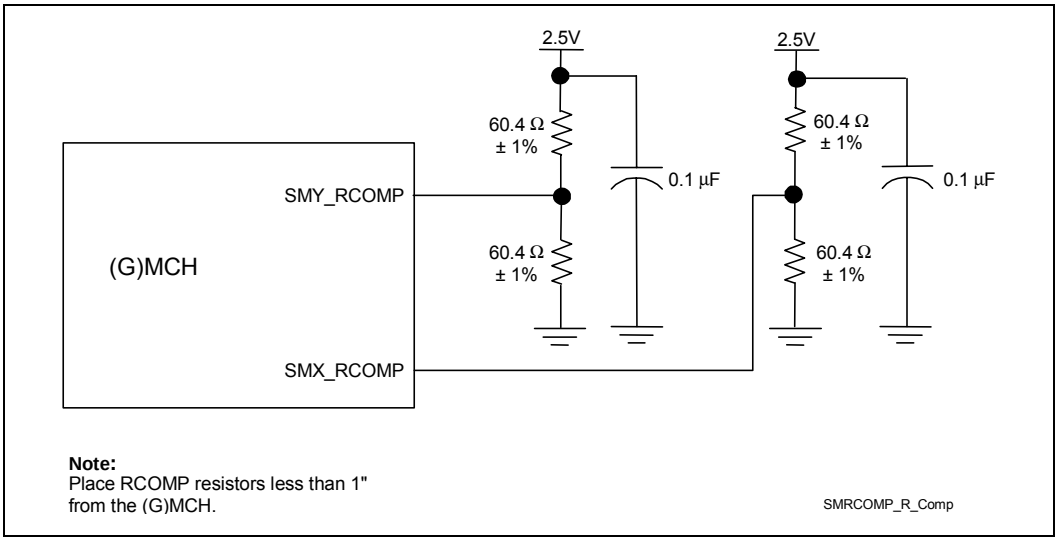


Table 5-20. DDR SMRCOMP Requirements

Parameter	Guideline
RCOMP Resistors	60.4 Ω ±1% pulled to DDR 2.5 V, and 60.4 Ω ± 1% tied to ground.
RCOMP Routing	Minimum width of 12 mils and isolated from other signals by 10 mils spacing.
Decoupling	Decouple each divider as shown in Figure 5-46.

5.4.6 DDR VTT Termination

All DDR signals, except the command clocks, must be terminated to 1.25 V (VTT) using 5% resistors at the end of the channel opposite the (G)MCH. Place a solid 1.25 V (VTT) termination island on the top signal layer, just beyond the last DIMM connector, as shown in the following figures. The VTT Termination Island must be at least 50-mils wide. Use this termination island to terminate all DDR signals, using one resistor per signal. Resistor packs are acceptable, with the understanding that the signals within an RPACK must be from the same DDR signal group. Termination resistor packs for each group must remain dedicated to that group, and not be shared with any other signal groups. No mixing of signals from different DDR signal groups is allowed within an RPACK. The parallel termination resistors connect directly to the VTT Island on the top signal layer.

Figure 5-47. DDR VTT Termination Island Example

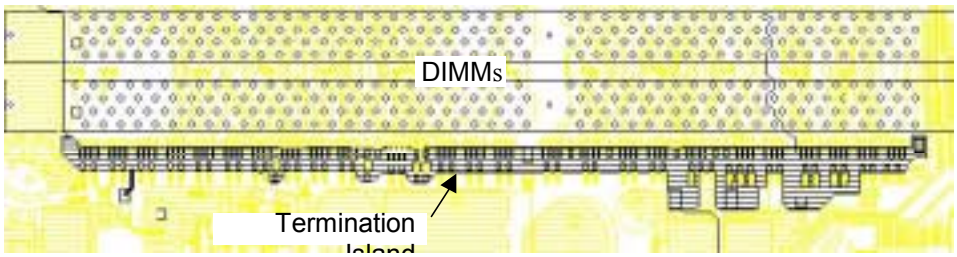


Table 5-21. DDR VTT Termination Island Requirements

Parameter	Guideline
Island Width	50 mils minimum
Resistor and capacitor connectivity	Connect termination resistors and decoupling capacitors directly to the termination island

5.4.6.1 VTT Termination Island High-Frequency Decoupling Requirements

The VTT Island must be decoupled using high-speed bypass capacitors, one 0603 0.1-µF capacitor per two DDR signals (or two capacitors per RPACK). These decoupling capacitors connect directly to the VTT Island and to ground, and must be spread-out across the Termination Island so that all the parallel termination resistors are near high-frequency capacitors. The capacitor ground via connecting the ground cutout on layer two and the ground plane on layer three should be within 25 mils of the capacitor pad and the via and the pad should be connected with as wide a trace as possible. The distance from any DDR termination resistor pin to a 0.1 µF VTT capacitor pin must not exceed more than 100 mils.

Finally, place one 4.7 µF ceramic capacitor on each end of the termination island and place one 4.7 µF ceramic capacitor near the center of the termination island. The power end of these capacitors must connect to the VTT termination island directly and the ground end of the capacitors must connect to ground on layer two and three.

Figure 5-48. DDR VTT Termination 0.1 µF High-Frequency Capacitor Example 1

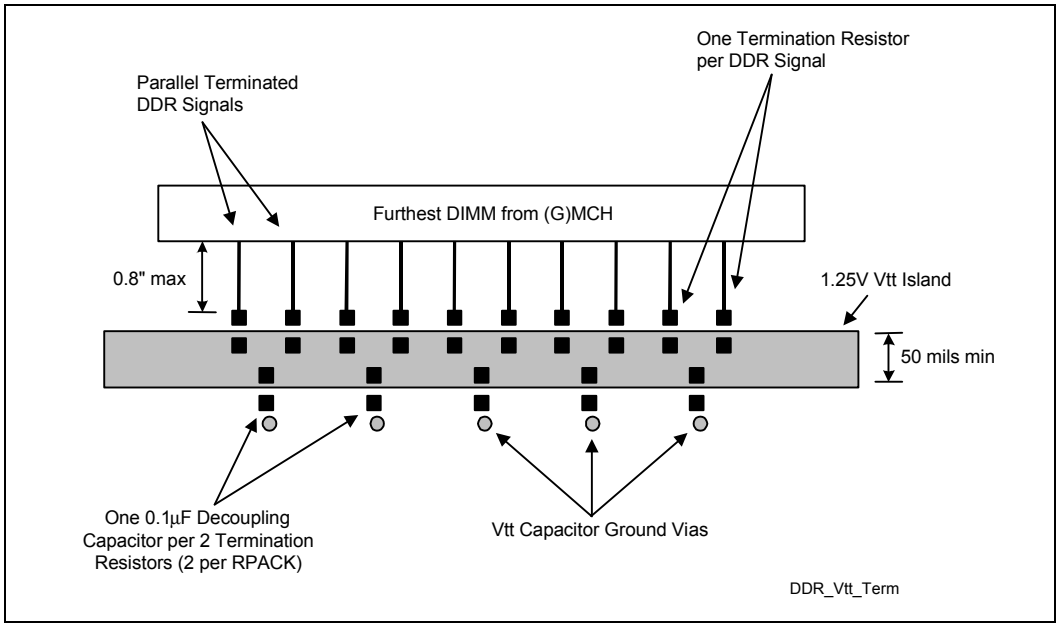


Figure 5-49. DDR VTT Termination 0.1 µF High-Frequency Capacitor Example 2

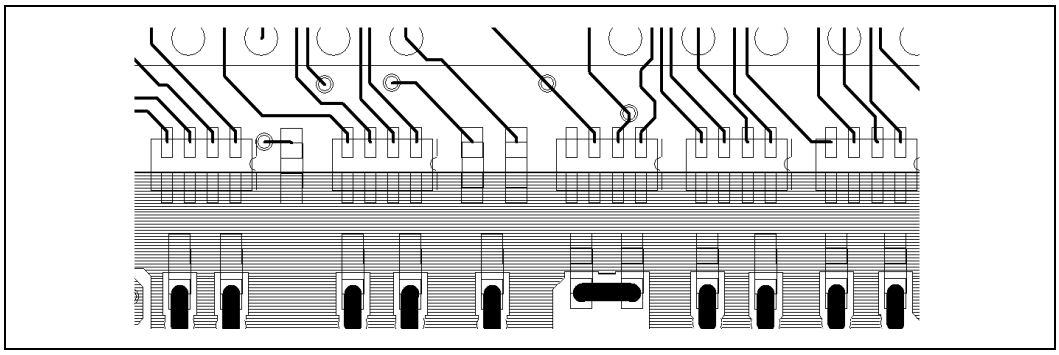


Figure 5-50. DDR VTT Termination 4.7 µF High-Frequency Capacitor Example

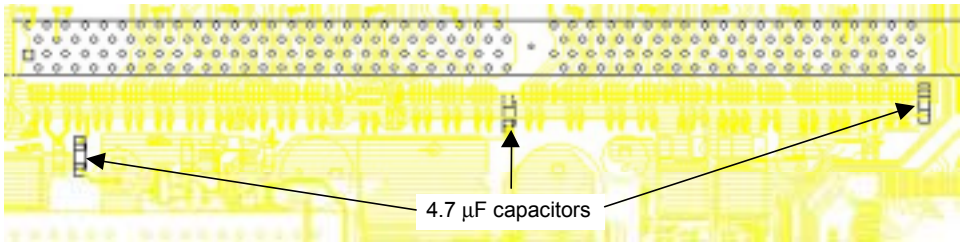


Table 5-22. DDR VTT Termination Island High-Frequency Decoupling Requirements

Parameter	Guideline
0.1 µF capacitors	Place one decoupling cap for every two DDR signals/termination resistors (or two caps for every RPACK). The distance from any termination resistor to decoupling capacitor should not exceed 100 mils.
4.7 µF capacitors	Three capacitors needed. Place one capacitor each at the middle, left, and right sides of the termination island as shown in Figure 5-50.

5.4.6.2 VTT Termination Island Low-Frequency Bulk Decoupling Requirements

The VTT Termination Island requires low-frequency bulk decoupling. Ensure adequate decoupling of the DDRVTT rail to meet the DC and AC electrical requirements found in Section 5.4.7.7. Different VTT regulator designs may require different bulk decoupling requirements (refer to the latest version of the Customer Reference Board (CRB) schematics for an implementation example). Also, the output of the 1.25 V regulator must have enough bulk decoupling to ensure the stability of the regulator. The amount of bulk decoupling required at the output of the 1.25 V regulator will vary according to the needs of different OEM design targets.

Figure 5-51. DDR VTT Termination Low-Frequency Capacitor Example

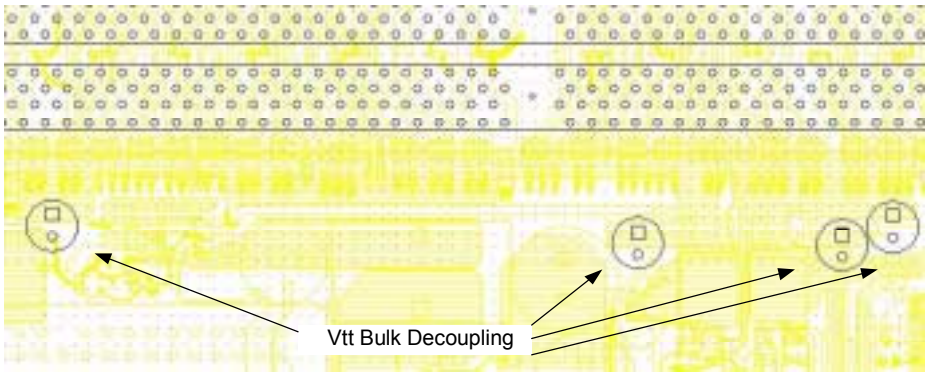


Table 5-23. DDR VTT Termination Island Low-Frequency Capacitor Example (As Seen on CRB)

Parameter	Guideline
Capacitor number	Four 470 µF capacitors (One 470 µF capacitor is empty site only)
Capacitor placement	Place one capacitor at each end of the termination island.

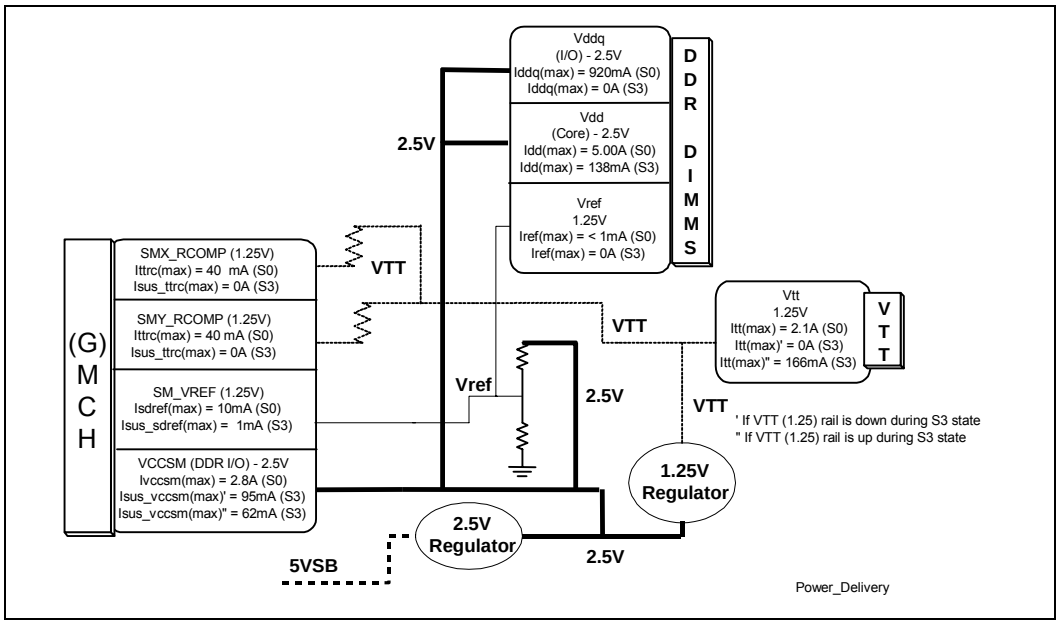
5.4.7 DDR Voltage Regulator Guidelines

The 845GE/845PE chipset designs using the DDR-SDRAM memory sub-system require several different voltages; VDD\VDDQ, VTT, and VREF. To generate these voltages, a 2.5 V and a 1.25 V regulator are required and must be designed to supply the required voltage and current levels to meet both the (G)MCH and DDR-SDRAM device requirements. The following sections define the range of DC and AC operating Voltage and Current conditions the 2.5 V and 1.25 V voltage regulators should meet for a two DIMM DDR-SDRAM based system with the 845GE/845PE chipset. It does not attempt to define a specific voltage regulator implementation. DDR voltage regulation will be governed by either an on-motherboard regulator circuitry or a module with the necessary complement of external capacitance, and will vary according to the requirements of specific OEM design targets.

5.4.7.1 Intel® 845GE/845PE Chipset DDR Reference Board Power Delivery

Figure 5-52 shows the power delivery architecture for the 845GE/845PE chipset DDR memory subsystem. This power delivery example provides support for the suspend-to-RAM (STR) and the full Power-on State.

Figure 5-52. Intel® 845GE/845PE Chipset DDR Power Delivery Example



5.4.7.2 DDR 2.5 V Power Plane

The 2.5 V power plane, which is generated by the 2.5 V regulator, is used to supply power to the (G)MCH 2.5 V I/O Ring, the DDR-SDRAM 2.5 V core, and the DDR-SDRAM 2.5 V I/O Ring. The 2.5 V regulator should be placed at the end of the DDR channel near the VTT Termination Island.

5.4.7.3 DDR 1.25 V Power Plane

The 1.25 V power plane, which is generated by the 1.25 V regulator, is used to supply the DDR termination voltage (VTT) and the (G)MCH SMRCOMP pull-up voltage (VTT). Special considerations need to be taken for the 1.25 V regulator design because it must be able to source and sink a significant amount of current. The 1.25 V regulator should be placed at the end of the DDR channel near the VTT Termination Island.

5.4.7.4 DDR Reference Voltage (VREF)

The (G)MCH and DDR-DIMM reference voltage (VREF) is generated from a typical resistor divider circuit off of the 2.5 V power plane. For guidelines on the VREF resistor divider refer to the previous DDR VREF generation section.

5.4.7.5 DC and AC Electrical Characteristics (DIMM Supply Rails)

The DDR 2.5 V voltage regulator supplies the required voltages (VDD\VDDQ, and VREF) and current for up to two DDR-DIMMs as shown in the following tables. The following DRAM Device specifications were determined at the DIMM connectors.

5.4.7.5.1 DDR-SDRAM DIMM Core and I/O Voltage (VDD, VDDQ)

The following conditions apply to the specifications listed below:

- IDD and IDDQ are measured at maximum VDD/VDDQ and under maximum signal loading conditions.
- Note that these worst case values are for reference only, and are based on current and future expected DRAM vendor specific specifications for maximum current.
- The worst-case IDD current draw was determined with the following criteria:
  - — Both DIMM slots are populated with double-sided Non-ECC x8 device DDR-DIMMs
  - — Continuous back-to-back burst reads, with a burst length of 4, to one single bank in the same physical DIMM device Row.
  - — All other banks are in the active standby state where a row in each bank is activated/open.

Table 5-24. DDR-SDRAM DIMM Core and I/O Voltage and Current Requirements (Measured at the DIMM Connectors)

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
Core Supply Voltage, Static	VDD	V	2.3	2.5	2.7
I/O Supply Voltage, Static	VDDQ	V	2.3	2.5	2.7
Core Supply Current, Static	Idd	A			5.0
I/O Supply Current, Static	IddQ	A			0.920

5.4.7.5.2 DDR-SDRAM DIMM Reference Voltage (VREF)

The following conditions apply to the specifications listed below:

- IREF is measured at maximum VREF under maximum signal loading conditions.

Table 5-25. DDR-SDRAM DIMM Reference Voltage and Current Requirements (Measured at the DIMM Connectors)

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
Absolute I/O Reference Supply Voltage, Static	VREF	V	VDD/2 – 0.05	VDD/2	VDD/2 + 0.05
I/O Reference Supply Current, Static	Iref	A			< 0.001

5.4.7.6 DC and AC Electrical Characteristics (Intel® (G)MCH Supply Rails)

The 2.5 V DDR voltage regulator supplies the required (G)MCH voltages, VCCSM and SDREF, and current as shown in the following tables. The following (G)MCH specifications were determined at the (G)MCH supply pins.

5.4.7.6.1 Intel® (G)MCH DDR Supply Voltage (VCCSM)

The following conditions apply to the specifications:

- IVCCSM is measured at maximum VCCSM under maximum signal loading conditions.

Note: These values are for reference only. Refer to the *Intel® 845GE/845PE Chipset Datasheet.*

Table 5-26. Intel® (G)MCH DDR Supply Voltage and Current Requirements (Measured at the (G)MCH)

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
(G)MCH DDR Supply Voltage, Static	VCCSM	V	2.375	2.5	2.625
(G)MCH DDR Supply Current, Static	IVCCSM	A			2.8

5.4.7.6.2 Intel® (G)MCH Reference Voltage (VREF)

The following conditions apply to the specifications:

- ISDREF is measured at maximum VSDREF under maximum signal loading conditions.

Note: These values are for reference only. Refer to the *Intel® 845GE/845PE Chipset Datasheet*.

Table 5-27. Intel® (G)MCH DDR Reference Voltage and Current Requirements (Measured at the (G)MCH)

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
(G)MCH Reference Supply Voltage, Static	SDREF	V	VCCSM/2 – 2%	VCCSM/2	VCCSM/2 + 2%
(G)MCH Reference Supply Current, Static	ISDREF	A			0.01

5.4.7.7 DC and AC Electrical Characteristics (VTT Supply Rail)

The 1.25 V DDR voltage regulator supplies the required DDR Termination Voltage (VTT) and current (ITT), and supplies the (G)MCH system memory resistive compensation pull-up voltage (VTT), and current (ITTRC) as shown in the following tables.

5.4.7.7.1 DDR Termination Voltage (VTT)

The following conditions apply to the specifications:

- ITT is measured at maximum VTT under maximum signal loading conditions by looking at all the DDR signals, excluding the command clocks, with their specified series and parallel termination resistors.

Table 5-28. DDR Termination Voltage and Current Requirements

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
Termination Supply Voltage, Static	VTT	V	SM_VREF – 0.04	SM_VREF	SM_VREF + 0.04
Termination Supply Current, Static	ITT	A			2.1

5.4.7.7.2 DDR SMRCOMP Pull-up Voltage (VTT)

The following conditions apply to the specifications:

- ITTRC is measured at maximum VTT under maximum signal loading conditions.

Table 5-29. DDR Termination Voltage and Current Requirements

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
SMRCOMP Termination Supply Voltage, Static	VTT	V	SM_VREF – 0.04	SM_VREF	SM_VREF + 0.04
SMRCOMP Termination Supply Current, Static	ITTRC	A			25mA

5.4.7.8 DDR Voltage Regulator Reference Design Example

Refer to the Reference Schematics (DDR) in Appendix A.

5.4.8 Power Sequencing Requirements

5.4.8.1 Intel® (G)MCH Power Sequencing Requirements

There is no (G)MCH power sequencing requirements. All (G)MCH power rails should be stable before deasserting reset, but the power rails can be brought up in any order desired. Good design practice would have all (G)MCH power rails come up as close in time as practical, with the core voltage (1.5 V) coming up first.

5.4.8.2 DDR-SDRAM Power Sequencing Requirements

No DDR-SDRAM power sequencing requirements are specified during power up or power down if the following criteria are met:

- VDD and VDDQ are driven from a single power converter output.
- VTT is limited to 1.44V (reflecting VDDQ(max)/2 + 50 mV VREF variation + 40 mV VTT variation)
- VREF tracks VDDQ/2
- A minimum resistance of 42 Ω (22 Ω series resistor + 22 Ω parallel resistor - 5% tolerance) limits the input current from the VTT supply into any pin.

If the above criteria cannot be met by the system design, the Table 5-30 must be adhered to during power up:

Table 5-30. Power-up Initialization Sequence

Voltage Description	Sequencing	Voltage Relationship to Avoid Latch-up
VDDQ	After or with VDD	< VDD + 0.3V
VTT	After or with VDDQ	< VDDQ + 0.3V
VREF	After or with VDDQ	< VDDQ + 0.3V

NOTE: The information in the table applies if the previously-listed requirements are not met.

6 AGP / Multiplexed Intel® DVO Design Guidelines

For detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms), refer to the latest *AGP Interface Specification, Revision 2.0*, which can be obtained from http://www.agpforum.org.

6.1 AGP

A single AGP connector is supported by the (G)MCH AGP interface. SERR# and PERR# from the AGP connector are not supported. The AGP buffers operate in only one mode:

- 1.5 V drive, not 3.3 V safe. This mode is compliant with the AGP 2.0 specification. The 845GE/845PE chipset can make use of a 1.5 V only AGP connector.

AGP 4X, 2X and 1X must operate at 1.5 V. The AGP interface supports up to 4X AGP signaling. AGP semantic cycles to DRAM are not snooped on the host bus.

The (G)MCH supports PIPE# or SBA_[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA_[7:0] mechanism must be selected during system initialization

The AGP interface is clocked from a 66-MHz clock. The AGP interface is asynchronous to the host bus, system memory and internal graphics device. The AGP interface is synchronous to the hub interface with a clock ratio of 1:1 (66 MHz : 66 MHz).

The Intel® 815 chipset multiplexed a display cache interface with its AGP interface. A Graphics Performance Accelerator (GPA) card was required to make use of that display cache interface. This feature is not supported with the 845GE/845PE chipset and the GPA will not function in an 845GE/845PE chipset system. Because GPA's are keyed for a 3.3 V AGP connector, they are not compatible with the 1.5 V AGP connector used with the (G)MCH.

6.1.1 AGP 2.0

The *AGP Interface Specification*, rev. 2.0, enhances the functionality of the original *AGP Interface Specification* (rev. 1.0) by allowing 4X data transfers (i.e., 4 data samples per clock) and 1.5-V operation. The 4X operation of the AGP interface provides for "quad-pumping" of the AGP AD (address/data) and SBA (side-band addressing) buses. That is, data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is ¼ of a 15-ns (66-MHz) clock or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, data is sampled twice during a 66-MHz clock cycle; therefore, the data cycle time is 7.5 ns. To allow for these high-speed data transfers, the 2X mode of AGP operation uses source-synchronous data strobing. During 4X operation, the AGP interface uses differential source-synchronous strobing.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be long. If the mismatch between a data line and the associated strobe is too great or if there is noise on the interface, incorrect data will be sampled. The low-voltage operation on AGP (1.5 V) requires even more noise immunity.

6.1.2 AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: 1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals. Each group has different routing requirements. In addition, within the 2X/4X timing domain signals, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements as well as trace width and spacing requirements. There are trace length matching requirements in each set of 2X/4X signals, as well as between sets of 2X/4X signals. Signal groups are listed in Table 6-1.

Table 6-1. AGP 2.0 Signal Groups

1X Timing Domain	2X / 4X Timing Domain	Miscellaneous, Async
CLK (3.3 V) GRBF# GWBF# GST_[2:0] GPIPE# GREQ# GGNT# GPAR GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL#	**Set 1** GAD_[15:0] GC/BE[1:0]# GADSTB_0 GADSTB_0# (see note) **Set 2** GAD_[31:16] GC/BE[3:2]# GADSTB_1 GADSTB_1# (see note) **Set 3** GSBA_[7:0] GSB_STB GSB_STB# (see note)	USB+ USB- OVRCNT# PME# TYPDET# PERR# SERR# INTA# INTB#

NOTE: These signals are used in 4X AGP mode ONLY.

Table 6-2. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobe in 2X	Associated Strobes in 4X
GAD_[15:0] and GC/BE_[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	GADSTB_0	GADSTB_0, GADSTB_0#
GAD_[31:16] and GC/BE_[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	GADSTB_1	GADSTB_1, GADSTB_1#
GSBA_[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	GSB_STB	GSB_STB, GSB_STB#

Throughout this section, the term “data” refers to GAD_[31:0], GC/BE_[3:0]#, and GSBA_[7:0]. The term “strobe” refers to GADSTB_[1:0], GADSTB_[1:0]#, GSBSTB, and GSBSTB#. When the term data is used, it refers to one of the three sets of data signals, as in Table 6-1. When the term strobe is used, it refers to one of the strobes as it relates to the data in its associated group.

The routing guidelines for each group of signals (1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals) will be addressed separately.

6.2 AGP Routing Guidelines

6.2.1 1X Timing Domain Routing Guidelines

- The AGP 1X timing domain signals (refer to Table 6-1) have a maximum trace length of 6 inches. This maximum applies to ALL signals listed as 1X timing domain signals in the table.
- AGP 1X timing domain signals can be routed with 5 on 7-trace separation.
- Trace length matching requirements for 1X timing domain signals apply only to 1X signals multiplexed with DVO signals. GIRDY# and GDEVSEL# should be matched (± 250 mils), as should GTRDY# with GFRAME# and GSTOP# with GAD_15.

6.2.2 2X/4X Timing Domain Routing Guidelines

These trace length guidelines apply to ALL signals listed in Table 6-1 as 2X/4X timing domain signals. These signals should be routed using 5-mil (60 Ω) traces.

For motherboards that utilize an AGP connector, the maximum length of AGP 2X/4X timing domain signals is 6 inches.

- 1:3- trace width-to-spacing is required for AGP 2X/4X signal traces.
- AGP 2X/4X signals must be matched with their associated strobe (as described in Table 6-2) from (G)MCH pad to AGP pin within ±0.125 inch. Refer to Table 6-3 for (G)MCH AGP nominalized package lengths.
- Strobes should match their complement to ± 50 mils.
- GADSTB_0 should match GADSTB_1 to ± 0.125 inch.

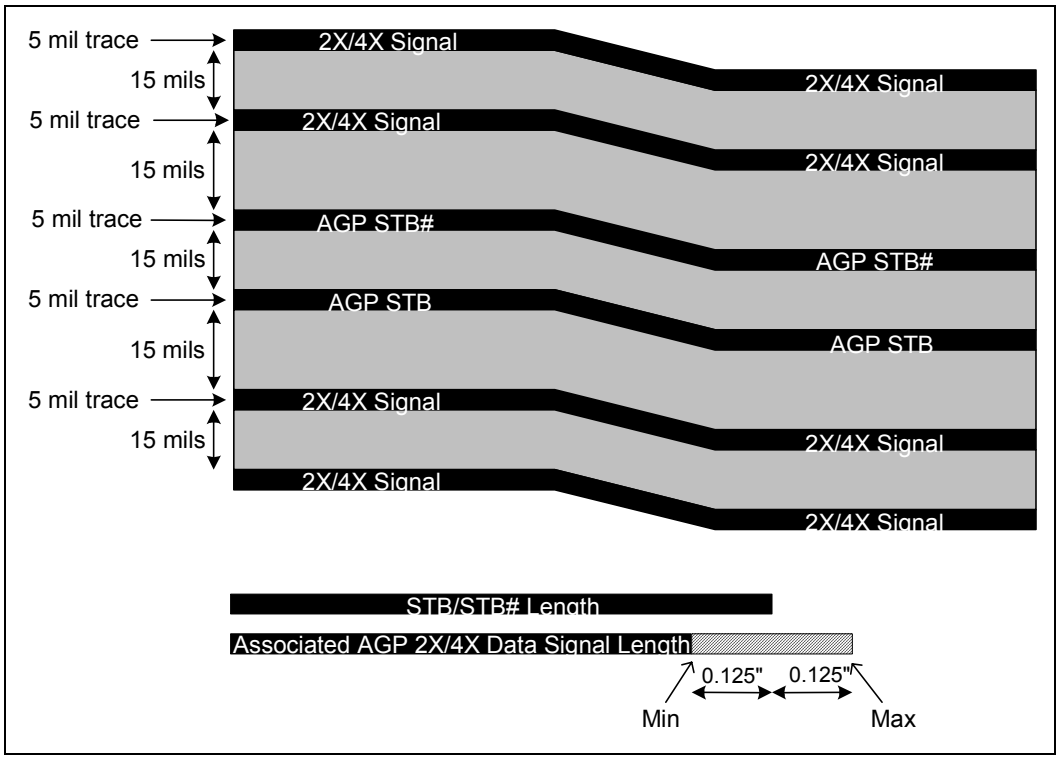
For example, if GADSTB_0 is 2.6 inches long, GADSTB_0# should also be 2.6 inches. The data signals associated with those strobe signals (e.g., GAD_[15:0] and GC/BE_[1:0]#) must be no more than 0.125 inch different in length from *either* of their associated strobes. This means that if GADSTB_0 is 2.6 inches long and GADSTB_0# is 2.65 inches long, then GAD_[15:0] and GC/BE_[1:0]# must be between 2.525 inches and 2.725 inches long. The GADSTB_1 pair should also be matched to 2.6 inches ± 0.125 inch, their associated data signals then matched to ±0.125 inch of the GADSTB_1 pair. The GSBSTBs are not directly related to the GADSTBs.

The strobe signals (GADSTB_0, GADSTB_0#, GADSTB_1, GADSTB_1#, GSBSTB, and GSBSTB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Because AGP 4X uses a differential clocking scheme, the pair should be routed together and on the same layer (e.g., GADSTB_0 and GADSTB_0# should be routed next to each other). The two strobes in a strobe pair should be routed using 5-mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals - and all other signals - by at least 20 mils (1:4). The strobe pair must be length-matched to less than ± 50 mils.

Table 6-3. Intel® (G)MCH AGP Nominalized Package Lengths

Data Signal	Intel® (G)MCH Ball	Package Length (Inches)	Data Signal	Intel® (G)MCH Ball	Package Length (Inches)
GSBSTB	F4	0.662	GADSTB_1	M8	0.443
GSBSTB#	E5	0.671	GADSTB_1#	L7	0.458
GSBA_7	F2	0.763	GAD_31	G4	0.628
GSBA_6	F3	0.688	GAD_30	K8	0.437
GSBA_5	E2	0.760	GAD_29	H3	0.679
GSBA_4	E4	0.716	GAD_28	J7	0.505
GSBA_3	D2	0.769	GAD_27	J5	0.580
GSBA_2	D3	0.767	GAD_26	J4	0.616
GSBA_1	C2	0.832	GAD_25	K3	0.640
GSBA_0	C3	0.812	GAD_24	G2	0.742
			GAD_23	H4	0.623
GADSTB_0	V8	0.384	GAD_22	L4	0.605
GADSTB_0#	U7	0.395	GAD_21	L5	0.549
GAD15	P3	0.573	GAD_20	M3	0.641
GAD14	T8	0.367	GAD_19	J2	0.676
GAD13	R7	0.410	GAD_18	K2	0.663
GAD12	R5	0.493	GAD_17	K4	0.575
GAD_11	R2	0.638	GAD_16	P8	0.364
GAD_10	T4	0.524			
GAD_9	T3	0.586			
GAD_8	T2	0.635	GC/BE_3#	H2	0.754
GAD_7	V3	0.574	GC/BE_2#	M2	0.675
GAD_6	U2	0.602	GC/BE_1#	N4	0.581
GAD_5	U4	0.514	GC/BE_0#	R4	0.557
GAD_4	U5	0.494			
GAD_3	W5	0.461			
GAD_2	W4	0.529			
GAD_1	V2	0.607			
GAD_0	V4	0.492			

Figure 6-1 2X/4X Routing Example



6.2.3 AGP Routing Guideline Considerations and Summary

- The 2X/4X timing domain signals can be routed with 5-mil spacing when breaking out of the (G)MCH. It is recommended that the routing widen to the documented requirements < 0.3 inch from the (G)MCH package.
- Reduce line length mismatch to ensure added margin. Trace length mismatch for all signals within a signal group should be as close to zero as possible, to provide timing margin.
- To reduce trace-to-trace coupling (crosstalk), separate the traces as much as possible.
- Ideally, all signals in a signal group should be routed on the same layer. Data and associated strobe signals must not be routed on a separate layer for more than 3 inches.

The trace length and trace spacing requirements must not be violated by any signal.

Table 6-4. AGP 2.0 Routing Summary

Signal	Max. Length	Trace Spacing (5-mil Traces)	Length Mismatch	Relative To	Notes
1X Timing Domain	6 inches	7 mils	No requirement	N/A	None
2X/4X Timing Domain Set 1	6 inches	15 mils[1]	±0.125 inch	GADSTB_0 and GADSTB_0#	GADSTB_0, GADSTB_0# must be the same length (± 50 mils); match GADSTB_0 to GADSTB_1 within 0.125 inch
2X/4X Timing Domain Set 2	6 inches	15 mils[1]	±0.125 inch	GADSTB_1 and GADSTB_1#	GADSTB_1, GADSTB_1# must be the same length (± 0 mils); match GADSTB_1 to GADSTB_0 within 0.125 inch
2X/4X Timing Domain Set 3	6 inches	15 mils[1]	±0.125 inch	GSBSTB and GSBSTB#	GSBSTB, GSBSTB# must be the same length (± 50 mils)

NOTES:
1. These guidelines apply to board stack-ups with 15% impedance tolerance.

6.2.4 AGP Clock Routing

The maximum total AGP clock skew, between the (G)MCH and the graphics component, is 1 ns for all data transfer modes. This 1 ns includes skew and jitter that originates on the motherboard, add-in card, and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but also at all points on the clock edge that fall within the switching range. The 1 ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew. (The motherboard designer determines how the 0.9 ns is allocated between the board and the synthesizer.)

For the 845GE/845PE chipset platform's AGP clock routing guidelines, refer to the clocking guidelines in Section 12.2.4.

6.2.5 AGP Signal Noise Decoupling Guidelines

The following routing guidelines are recommended for the optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the (G)MCH. The following guidelines are not intended to replace thorough system validation on 845GE/845PE chipset-based products.

- (5) 0.1 µF capacitors are required and must be as close as possible to the (G)MCH. These should be placed within 100 mils of the outer row of balls on the (G)MCH for VDDQ decoupling. The closer the placement, the better.
- The designer should evenly distribute placement of decoupling capacitors in the AGP interface signal field.
- It is recommended that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.

- To add the decoupling capacitors within 100 mils of the (G)MCH and/or close to the vias, the trace spacing for AGP signals may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible.
- In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. On a typical four layer PCB design, the signals transition from one side of the board to the other. One 0.01 µF capacitor is required per 5 vias. The capacitor should be placed as close as possible to the center of the via field.

6.2.5.1 1.5 V AGP Connector Decoupling

The designer should ensure that the AGP connector is well decoupled. The following recommendations are derived from the *AGP Design Guide, Revision 1.0*, Section 1.5.3.3 Connector AC Signal Decoupling Requirements:

The decoupling capacitor recommendations for the AGP connector are intended to address AC signaling issues and not power delivery issues. The main reason for not addressing power delivery issues with the motherboard connector decoupling is due to the connector inductance and the distance the capacitors are from the graphics device. These two factors negate much of the usefulness of the connector decoupling on the motherboard for power delivery purposes. The following are recommendations for decoupling at the AGP connector on the motherboard:

- VCC3.3: Three 0.01 µF or larger, low ESL capacitors. Each capacitor should be placed as close as possible to a VCC3.3 pair of pins on the connector.
- VDDQ: Six 0.01 µF or larger, low ESL capacitors. Each capacitor should be placed as close as possible to a VDDQ pair of pins on the connector.
- +5 V: One 0.01 µF or larger, low ESL capacitor placed as close as possible to the +5 V connector pins.
- +12 V: One 0.01 µF or larger, low ESL capacitor placed as close as possible to the +12 V connector pin.
- 3.3VAUX: One 0.01 µF or larger, low ESL capacitors placed as close as possible to the 3.3VAUX connector pin(s).

6.2.6 AGP Routing Ground Reference

It is strongly recommended that the following critical signals be referenced to ground from the (G)MCH to an AGP connector (or to an AGP video controller, if implemented as a "down" solution on the motherboard), using a minimum number of vias on each net: GADSTB_0, GADSTB_0#, GADSTB_1, GADSTB_1#, GSBSTB, GSBSTB#, GTRDY#, GIRDY#, GGNT#, and GST_[2:0].

For the AGP interface, it is strongly recommended that all the AD/CBE signals be referenced to ground. In an ideal design, the complete AGP interface signal field would be referenced to ground. This recommendation is not specific to any particular PCB stack-up, but should be applied to all 845GE/845PE chipset designs.

6.3 AGP 2.0 Power Delivery Guidelines

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller (or the DVO device in an ADD scenario). This voltage is always 3.3 V. If the graphics controller (or DVO device) needs a lower voltage, then the add-in card must regulate the 3.3 V VCC voltage to the device's requirements. The graphics controller may **only** power AGP I/O buffers with the 1.5 V VDDQ power pins. In the ADD card scenario, any output signal from the card must not exceed 1.5 V. This means that I^2C (normally 3.3 V) and DDC (normally 5 V) signals must have a level-shifting device *on the ADD card* to ensure that 1.5 V is not exceeded.

Because the (G)MCH only supports 1.5 V signaling, flexible VDDQ (1.5 V or 3.3 V) voltage regulation and TYPEDET# circuitry should not be implemented. TYPEDET# does not need to be routed from the AGP connector as it is not used to set VDDQ on 845GE/845PE chipset-based platforms.

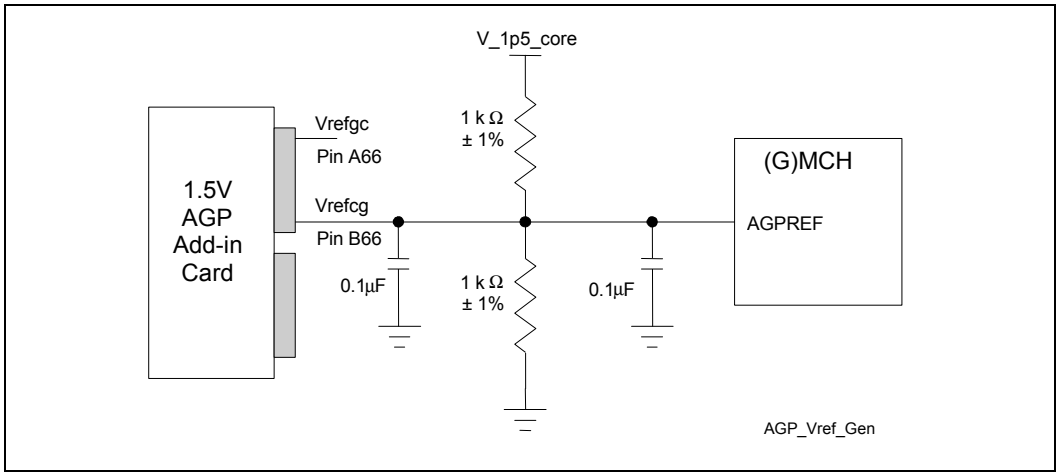
6.3.1 VREF Generation for AGP 2.0

Both the graphics controller and the (G)MCH are required to generate VREF and distribute it through the connector. The following two pins are defined on the AGP 2.0 universal connector to allow this VREF passing:

- VREFGC: VREF from the graphics controller to the chipset
- VREFCG: VREF from the chipset to the graphics controller

The (G)MCH does not make use of the VREFGC, but 845GE/845PE chipset systems are still required to supply a voltage (½ of VDDQ) through VREFCG. Regardless of whether or not the platform uses AGP, VREF must always be supplied to the (G)MCH. See Figure 6-2 for an example circuit.

Figure 6-2. AGP VREF Generation



6.4 Additional AGP Design Guidelines

6.4.1 Compensation

The (G)MCH AGP interface supports resistive buffer compensation (RCOMP). Tie the AGP_RCOMP pin to a 40 Ω, 1% pull-down resistor (to ground) through a very short (<0.5 inch) trace.

6.4.2 AGP Pull-Ups

AGP control signals require resistors that pull up to VDDQ to ensure that they contain stable values when no agent is actively driving the bus. The (G)MCH has integrated the following pull-up resistors:

1X Timing Domain Signals

- GFRAME#
- GSTOP#
- GWBF#
- GTRDY#
- GRBF#
- GGNT#
- GIRDY#
- GPIPE#
- GST_[2:0]
- GDEVSEL#
- GREQ#
- GPAR (see note)

Note: The strobe signals have internal pull-ups/pull-downs to ensure that they contain stable values when no agent is driving the bus.

SERR#/PERR# should be pulled up to VDDQ at the AGP connector.

2X/4X Timing Domain Signals

- GADSTB_[1:0] (pull up to 1.5 V)
- GSBSTB (pull up to1.5 V)
- GADSTB_[1:0]# (pull down to ground)
- GSBSTB# (pull down to ground)

6.4.2.1 AGP Signal Voltage Tolerance List

The following signals on the AGP interface are 3.3 V tolerant during 1.5 V operation:

- PME#
- INTA#
- INTB#
- CLK
- RST

The following signals on the AGP interface are 5 V tolerant (refer to the USB 2.0 specification):

- USB+
- USB-
- OVRCNT#

The following special AGP signal is either GROUNDED or NOT CONNECTED on an AGP card.

- TYPEDET#

Note: All other signals on the AGP interface are in the VDDQ group. For an 82845GE/82845PE (G)MCH, they are only 1.5 V tolerant!

Note: INTA# and INTB# should be pulled to 3.3 V, not VDDQ.

6.5 AGP/Intel® DVO Shared Interface (Intel® 845GE chipset only)

6.5.1 Overview (Intel® 82845GE only)

The AGP interface of the 845GE chipset is multiplexed or shared with a digital display interface. In other words, the same component pins (balls) are used for both interfaces, although obviously only one interface can be supported at any given time. As a result, DVO signals are mapped onto the AGP interface. This interface can be configured in either AGP mode or Digital Video Out (DVO) mode. Additionally, if an AGP connector is used, DVO down cannot be implemented. In the AGP mode, the interface supports a full AGP 4X interface. In DVO mode, the interface becomes a digital display interface.

6.5.1.1 Multiplexed AGP Interface (Intel® 82845GE only)

The 82845GE GMCH multiplexes the AGP signal interface with two Digital Video Out (DVO) ports. When an external AGP device is used, the multiplexed DVO ports are not available and the 82845GE IGD is disabled. For flexible motherboard designs that want to make use of a 1.5 V AGP connector, the multiplexed DVO ports can only be utilized via an AGP Digital Display (ADD) card.

The guidelines for AGP card support and ADD card support are the same. There are **not** separate guidelines for systems that only support AGP cards.

A single AGP connector is supported by the GMCH AGP interface. SERR# and PERR# from the AGP connector are not supported. The AGP buffers operate in only one mode:

- 1.5 V drive, not 3.3 V safe. This mode is compliant with the AGP 2.0 specification. The 845GE chipset can make use of a 1.5 V only AGP connector.

AGP 4X, 2X and 1X must operate at 1.5 V. The AGP interface supports up to 4X AGP signaling. AGP semantic cycles to DRAM are not snooped on the host bus.

The GMCH supports PIPE# or SBA_[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA_[7:0] mechanism must be selected during system initialization

The AGP interface is clocked from a 66-MHz clock. The AGP interface is asynchronous to the host bus, system memory and internal graphics device. The AGP interface is synchronous to the Hub Interface with a clock ratio of 1:1 (66 MHz : 66 MHz).

6.5.1.2 AGP Digital Display (ADD) Card (Intel® 82845GE only)

The GMCH multiplexes the AGP signal interface with two DVO ports. These DVO ports are capable of supporting a variety of digital display devices, such as TMDS transmitters and TV-Out encoders. It is possible to use the DVO ports in dual-channel mode to support higher resolutions and refresh rates (single channel mode is limited to a 165 MHz pixel clock rate).

Flexible motherboard designs may make use of a 1.5 V AGP connector. In this scenario, an ADD card is required to make use of the multiplexed DVO ports. The ADD card is designed to plug into

a 1.5 V AGP connector. When an ADD card is populated, the GMCH cannot support an external AGP device. When an external 1.5 V AGP device is populated, the GMCH cannot support the ADD card.

6.5.1.3 AGP Digital Display (ADD) Card Considerations (Intel® 82845GE only)

To support the fullest display flexibility, a digital display device may reside on an ADD card that complies with the 1.5 V AGP connector form factor. If the motherboard designer follows the routing guidelines for the AGP interface detailed in previous sections, the customer has a wide variety of options. A 1.5 V AGP connector on an 845GE chipset platform can utilize either an AGP Graphics card or an ADD card, or be left unpopulated to obtain the lowest-cost solution. Some ADD/845GE chipset interfacing implications are as follows.

- A pull-up resistor is required on GPAR/ADD_DETECT# to allow the GMCH to determine whether an ADD card or AGP card is populated. The GMCH has integrated a pull-up for this function, but an external site may still be required on the motherboard. The ADD card will pull this signal down, stronger than the on-board pull-up, to communicate to the GMCH that it should operate in DVO mode.

Any I/O signals on the ADD card that exceed the 1.5 V signaling level (e.g. I^2C and DDC), must have a level shifting device on the ADD card. No output signal from the ADD card to the GMCH may exceed 1.5 V.

6.5.1.4 Motherboard/Add-In Card Interoperability (Intel® 82845GE only)

There are three AGP connectors*: 3.3 V AGP connector*, *1.5 V AGP connector* and *Universal AGP connector*. The **GMCH only supports the 1.5 V AGP connector.**

The GMCH can support either an external 1.5 V capable AGP device or an ADD card. The GMCH cannot support both devices simultaneously.

The 815 chipset multiplexed a display cache interface with its AGP interface. A Graphics Performance Accelerator (GPA) card was required to make use of that display cache interface. Because the GMCH has a multiplexed digital display interface, not a multiplexed display cache interface, the GPA will not function in an 845GE system. Because GPA's are keyed for a 3.3 V AGP connector, they are not compatible with the 1.5 V AGP connector used with the GMCH.

All assumptions relating to AGP routing include 2 inches of trace on the AGP card. If an AGP device is used down on the board, then 2 inches can be added to trace lengths; all other guidelines still apply.

6.5.1.5 ADD Clocking (Intel® 82845GE only)

The digital display interface is clocked source synchronously by the GMCH. The digital display interface clocking scheme uses four output clock signals: DVOB_CLK and DVOB_CLK#, and DVOC_CLK and DVOC_CLK#, and a single clock input: DVOBC_CLKINT#. The four output clocks are multiplexed with the AD strobes and should be routed according to the AGP strobe guidelines detailed in previous sections. DVOBC_CLKINT# is only an input clock when the DVO device on the ADD card is running in TV-Out mode. This input clock is multiplexed with the AD13 line.

6.5.2 Multiplexed Intel® DVO Down (Intel® 82845GE only)

If an external AGP device\connector is not implemented, it is possible to solder DVO devices down on the motherboard. GMCH multiplexed DVO ports (DVOB and DVOC) are 1.5 V interfaces that can each support transactions up to 165 MHz. The DVO ports are capable of interfacing with a wide variety of DVO port compliant devices (e.g. discrete TV encoder, discrete TMDS transmitter, combination TV encoder and TMDS transmitter or LVDS transmitters).

All assumptions relating to DVO routing include 1.5 inches of trace on the ADD card. If a DVO device is used down on the board, then 1.5 inches can be added to trace lengths from the previous section.

In a DVO device down scenario, a 330 Ω pull-down to GND is required on GPAR/ADD_DETECT# as well as SBA_7/ADD_ID7.

The GMCH controls the video front-end devices via the multiplexed I^2C interfaces. The MI2C_DATA and MI2C_CLK pins should be used to communicate with I^2C compliant DVO devices. I^2C is a two-wire communications bus/protocol. The protocol and bus are used to configure registers in the DVO device. GMCH also uses the MDVI_CLK and MDVI_DATA to collect EDID (Extended Display Identification) from a digital display panel.

Do not interchange or modify the functionality of MI2C and MDVI signals. Each of these signals requires a 4.7-kΩ pull-up to 1.5 V (or pull-up with the appropriate value derived from simulation). These signals are 1.5 V tolerant. If higher signaling voltages are needed (3.3 V for MI2C and 5 V for MDVI), then level-shifting devices will be required on the motherboard.

6.5.2.1 Intel® DVO Interface Routing Guidelines (Intel® 82845GE only)

Route data signals (DVOx_D[11:0]) with a trace width of 5 mils and a trace spacing of 15 mils. To break out of the GMCH, the DVO data signals can be routed with a trace width of 5 and a trace spacing of 5. The signals should be separated to a trace width of 5 and a trace spacing of 15 within 0.3 inch of the GMCH component. The maximum trace length for the DVO data signals is 7.5 inches. These signals should each be matched within ± 0.125 inch of their associated Clk(#) signals.

Route the DVOx_Clk (#) signals 5-mils wide and 15 mils apart. This signal pair should be a minimum of 20 mils from any adjacent signals. The maximum length for DVOx_Clk(#) is 7.5 inches, and the two signals should be the same length.

DVOx_CLK is the primary clock of the differential pair. Care should be taken to ensure that DVOx_CLK is connected to the primary clock receiver on the DVO device. If the DVO device supports differential clocking mode (highly recommended), then DVOx_CLK# should be connected to the complementary clock receiver of the DVO device.

6.5.3 Leaving the Intel® 845GE Chipset AGP/Intel® DVO Port Unconnected

If the motherboard does not implement any of the possible graphics/display devices with the AGP/DVO port, the following is recommended on the motherboard:

- Voltages, including AGP_VREF, must still be supplied to the GMCH.
- Signals can be left as NCs – initial boards may want to have empty back up sites for the pull-up resistors outlined in Section 6.4.2
- AGPRCOMP should still be connected to a 40 Ω 1% pull down to ground.

7 Analog Display Port

7.1 Analog RGB/CRT for Intel® 845PE Chipset Design Guidelines

The Analog Display Port is available only on 845GE chipsets. This port is not on the 845PE chipset. For motherboards designed to support the 845PE chipset only, the associated DAC signal pins should be connected as described in the following table. For motherboards designed to support both the 845GE chipset and the 845PE chipset, see the following note.

Note: A single motherboard can be designed to support both the 845GE chipset and the 845PE chipset with Bill Of Material (BOM) changes. When the 845PE chipset is used on a board designed to support both the 845GE chipset and 845PE chipset, the analog port signals should be left as no connects by leaving the related external components unpopulated (i.e., pi filter and termination on RED, GREEN, BLUE and RED#, GREEN#, BLUE#, pull-up resistors to DDC, level shifting to sync, and any VCCDAC specific components).

Table 7-1. Analog RGB/CRT Guidelines for Intel® 845PE Chipset

Signal	Intel® 82845PE MCH Ball	Guideline
RED, GREEN, BLUE	C15, E15, G15	Tie directly to ground
RED#, GREEN#, BLUE#	D16, F16, H16	
VCCA_DAC	A15, B14	
VSSA_DAC	B15, C14	
VCCA_DPLL	A13	
REFSET	B16	
DREFCLK	D14	
HSYNC	B7	No Connect
VSYNC	C6	No Connect
DDCA_DATA	C7	Tie directly to ground
DDCA_CLK	D7	

7.2 Analog RGB/CRT for Intel® 845GE Chipset Design Guidelines

7.2.1 RAMDAC/Display Interface (Intel® 845GE chipset only)

The 82845GE integrated graphics device interfaces to an analog display via a RAMDAC. The RAMDAC is a subsection of the graphics controller display engine and consists of three identical 8-bit digital-to-analog converter (DAC) channels, one for the display's red, green, and blue electron guns.

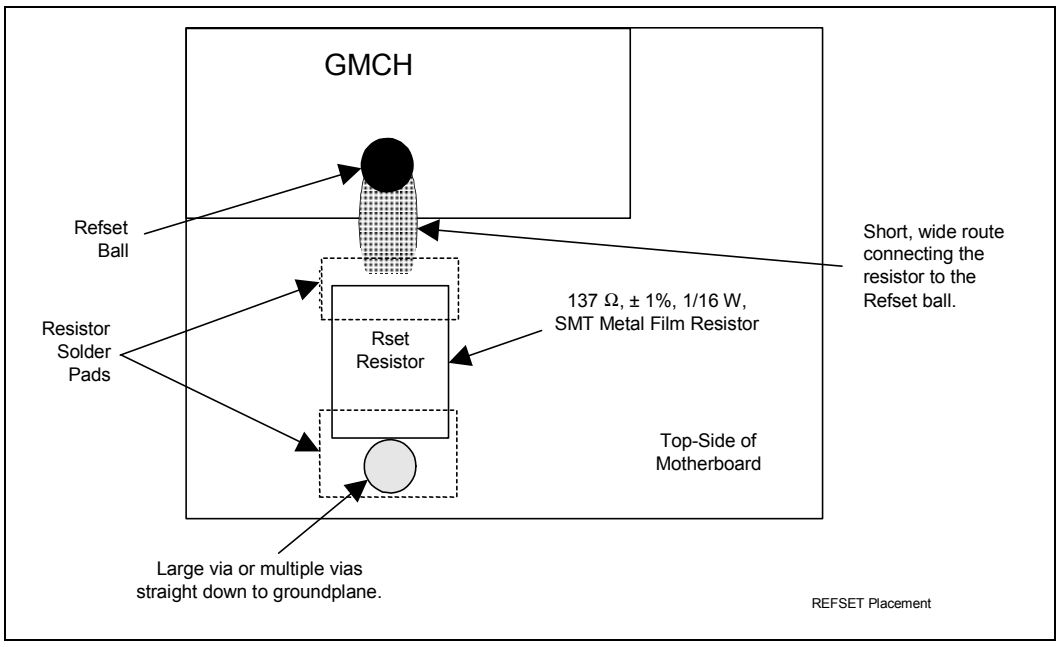
Each RGB output is doubly terminated with a 75 Ω resistance: One 75 Ω resistance is connected from the DAC output to the board ground, and the other termination resistance exists within the display. The equivalent DC resistance at the output of each DAC is 37.5 Ω. The current output from each DAC flows into this equivalent resistive load to produce a video voltage, without the need for external buffering. There is also a CLC pi-filter on each channel that is used to reduce high-frequency noise and to reduce EMI. To maximize the performance, the filter impedance, cable impedance, and load impedance should be matched.

Because the 82845GE DAC runs at speeds up to 350 MHz, special attention should be paid to signal integrity and EMI. RGB routing, component placement, component selection, cable and load impedance (monitor) all play a large role in the analog display's quality and robustness. This holds true for all resolutions, but especially for those at 1600x1200 or higher.

7.2.2 Reference Resistor (REFSET) (Intel® 845GE chipset only)

A reference resistor of 137 Ω is used to set the reference current for the RAMDAC. This resistor is an external resistor with a 1% tolerance that is placed on the circuit board.

Figure 7-1. REFSET Placement



7.2.3 RAMDAC Board Design Guidelines (Intel® 845GE chipset only)

For the DAC to successfully run at speeds up to 350 MHz, care should be taken when routing the analog RAMDAC signals. A variety of routing options are available, be sure to thoroughly validate any DAC routing design you choose to use. If routed differentially, each analog RGB signal should be routed differentially with its complement RED#, GREEN#, BLUE# signal. A pair (i.e., RED and RED#) should be routed 75 Ω odd-mode differential. For the assumed stack-up, this equates to ~8 mil trace for both traces with as little space (~5 mils) between the pair as possible. Spacing between pairs and to other signals should be maximized, 20-mil spacing is recommended. The RGB signals should utilize pi filters placed near the VGA connector. An example pi-filter will consist of two 3.3 pF capacitors with a 75 Ω @ 100 MHz FB between them. Prior to hitting this filter, the RGB signals should have a 75 Ω 1% terminating pull-down resistor. If routed differentially, the complement signals (RED#, GREEN#, and BLUE#) do not require a pi filter and should be terminated with a ~37.5 Ω 1% resistor to ground.

If routed differentially, each analog signal should be matched to its complement as closely as possible. This includes the routing channel for each signal as well as the loading on that signal. To have the complements' loading and edge rates more closely resemble that of the RGB signals, the complements may have a capacitor across their terminating resistors to mimic the pi filter. Also, the three pairs (RED/RED# combined) should closely resemble each other. If possible, try to match bends in one pair to the other two.

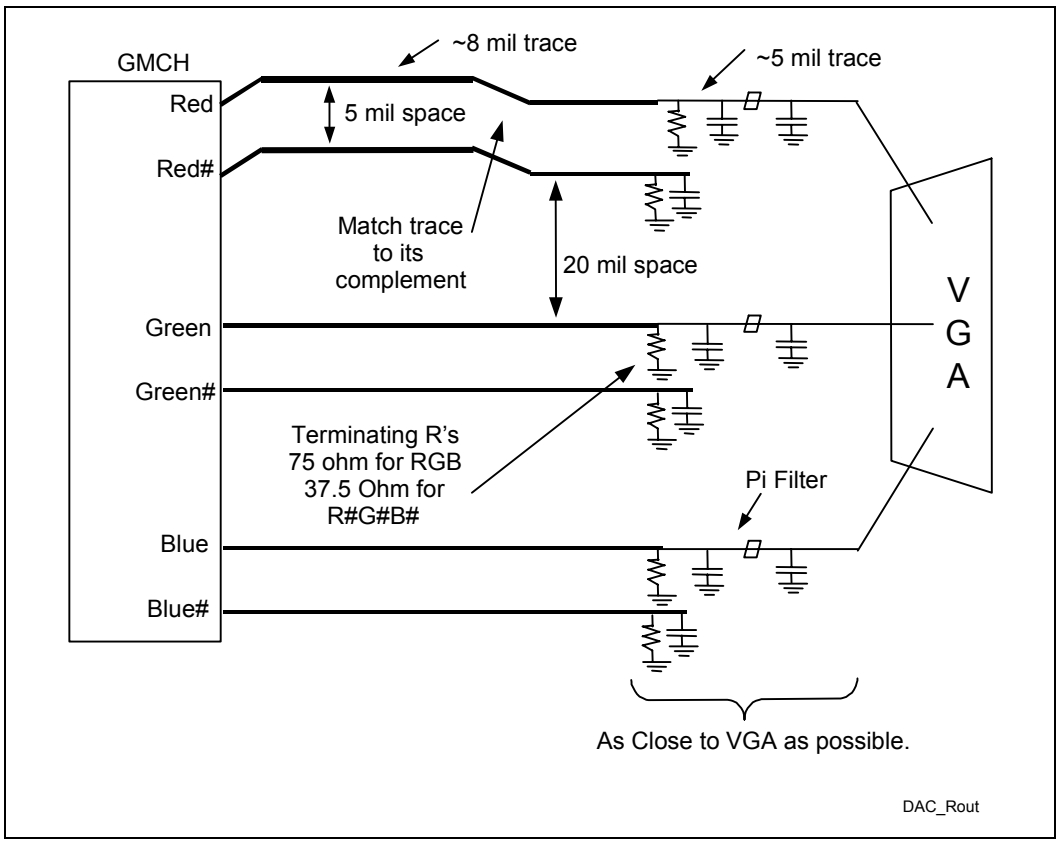
If routed differentially, signals within a pair should be routed with 5-mil spacing for as long a length as possible. To accomplish this, it is recommended that the pi filter and terminating resistors be placed as close as possible to the VGA connector. The complement signals should terminate through their 37.5 Ω resistors at the same location that the RGB signals hit their 75 Ω terminating resistors. After hitting their 75 Ω terminating resistors, the RGB signals should continue on to their pi filters and the VGA connector, *but should now ideally be routed with a 75 Ω impedance (~ 5 mil traces).*

If single-ended routing is desired, the RGB traces should be routed 5-mils wide all the way from the GMCH, through the pi-filter to the VGA connector. The complement signals (RED#, GREEN#, and BLUE#) should be terminated to ground with as little trace as possible. Terminating resistors are not needed on the #'s if routing the RGB single-ended. In this scenario, the RGB signals should be routed 5-mils wide with at least 20-mil spacing. Termination and pi-filter recommendations for the RGB signals are identical to those mentioned above. Namely, they should have a 75 Ω 1% termination resistor, followed by the pi-filter as close as possible.

Regardless of routing preference, the RGB signals also require protection diodes between 1.5 V and ground. These diodes should have low C ratings (~5 pF max) and small leakage current (~ 10 uA @ 120 °C) and should be properly decoupled with a 0.1 µF capacitor. These diodes and decoupling should be placed to minimize power rail inductance. To have the complements' loading more closely resemble that of the RGB signals, the complements may have similar diodes. The choice between diodes (or diode packs) should comprehend the recommended electrical characteristics in addition to cost.

The RGB signals should be length matched as closely as possible (from GMCH to VGA connector) and should not exceed 200 mils of mismatch.

Figure 7-2. Generic DAC Routing — Differential Style



NOTE: This figure does not illustrate the recommended diodes.

7.2.4 DAC Power Requirements (Intel® 845GE chipset only)

The DAC requires a 1.5 V supply through its two VCCA_DAC balls. The two may share a set of capacitors (0.1 µF and 0.01 µF) but this connection should have low inductance. This supply should be connected directly to the main 1.5 V plane – it should **not** be connected to 1.5 V through an LC filter (like DPLL). Separate analog power or ground planes are not required for the DAC.

However, because the DAC is an analog circuit, it is particularly sensitive to AC noise seen on its power rail. Designs should provide as clean and quiet a supply as possible to the VCCA_DAC. Additional filtering and/or separate voltage rail may be needed to do so. Refer to the *Intel® 845GE/845PE Chipset Datasheet* for DC specifications for this supply.

7.2.5 Sync and DDCA Considerations (Intel® 845GE chipset only)

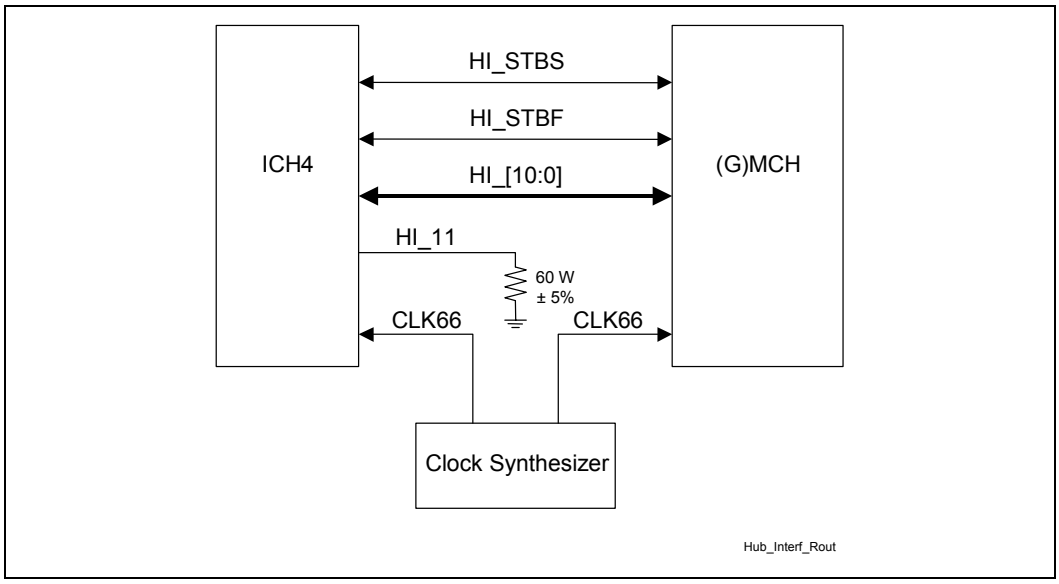
HSYNC and VSYNC should have ~50 Ω 5% series resistors on them. These are 3.3 V outputs from the GMCH, if higher signaling voltages are needed (5 V), level-shifting devices will be required. DDCA_DATA and DDCA_CLK should be connected to the analog display attached to the DAC. 4.7 kΩ pull-ups (or pull-ups with the appropriate value derived from simulation) are required on each of these signals. These signals are 3.3 V tolerant. If higher signaling voltages are needed (5 V), then level-shifting devices will be required.

8 Hub Interface

The (G)MCH and ICH4 ballout assignments have been optimized to simplify the hub interface routing between these devices. It is recommended that the hub interface signals be routed directly from the (G)MCH to ICH4 with all signals referenced to VSS. Layer transition should be kept to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signal on the same layer.

The hub interface signals are broken into two groups: data signals (HI) and strobe signals (HI_STB). For the 8-bit hub interface, HI_[10:0] are associated with HI_STBS and HI_STBF.

Figure 8-1. Hub Interface Routing Example



8.1 Hub Interface Routing Guidelines

This section documents the routing guidelines for the hub interface. This hub interface connects the ICH4 to the (G)MCH. The ICH4 should strap its HICOMP pin to VCCHI=1.5 V. The trace impedance must equal 60 Ω ± 15%.

8.1.1 Hub Interface Strobe Signals

The Hub Interface strobe signals should be routed 5-mils wide with 15-mils trace spacing (5 on 15). This strobe pair should have a minimum of 20 mils spacing from any adjacent signals. The maximum length for the strobe signals is 2 inches to 8 inches. The length between two strobes must be matched within ± 100 mil. Additionally, each data signal must be matched within ± 100 mils of the strobe signals. To break out of the (G)MCH and ICH4 package, the hub interface strobe signals can be routed 5 on 5 within 300 mils of the package.

8.1.2 Hub Interface Data Signals

The Hub Interface data signal traces should be routed 5-mils wide with 15-mils trace spacing (5 on 15). To break out of the (G)MCH and ICH4 package, the hub interface data signals can be routed 5 on 5 within 300 mils of the package.

The maximum hub interface data signal trace length is 2 inches to 8 inches. Each data signal must be matched within ± 100 mils of the HI_STBF/HI_STBS pair.

8.1.3 Hub Interface Signal Referencing

The hub interface signal traces (HI_[10:0]) and the two hub interface strobe signals (HI_STBS and HI_STBF) must all be referenced to ground to insure proper noise immunity.

8.1.4 Hub Interface HI_REF/HI_SWING Generation/Distribution

HI_REF is the Hub Interface reference voltage. The ICH4 uses HI_SWING to control voltage swing and impedance strength of the Hub Interface buffers. The HI_REF and HI_SWING voltage requirement and associated resistor/capacitor recommendations for the voltage divider circuit are listed in Table 8-1.

Table 8-1. Hub Interface HI_REF/HI_SWING Generation Circuit Specifications

HI_REF Voltage Specification	HI_SWING Voltage Specification	Recommended Values for the HI_REF / HI_SWING Divider Circuit
350 mV ± 2% at 1.5 V nominal	700 mV ± 2% at 1.5 V nominal	R1 = 226 Ω ± 1%, R2 = R3 = 100 Ω ± 1% C2 and C5 = 0.1 µF C1, C3, C4, and C6 = 0.01 µF

The resistor values, R1, R2, and R3, must be rated at 1% tolerance. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. Two 0.1 µF capacitors (C2, C5) should be placed close the divider. In addition, the 0.01 µF bypass capacitors (C1, C3, C4, C6) should be placed within 0.25 inch of the component HI_REF/VREF pin (for C3 and C4) and HI_SWING pin (for C1 and C6). The max distance from divider to device is 4 inches (less is better). Normal care must be taken to minimize crosstalk to other signals (< 10–15 mV). If the single HI_REF/HI_SWING divider circuit is located more than 4 inches away, then the locally generated reference divider should be used. The following figure is an example of the HI_REF/HI_SWING divider circuit.

Figure 8-2. Hub Interface Single HI_REF/HI_VSWING Generation Circuit

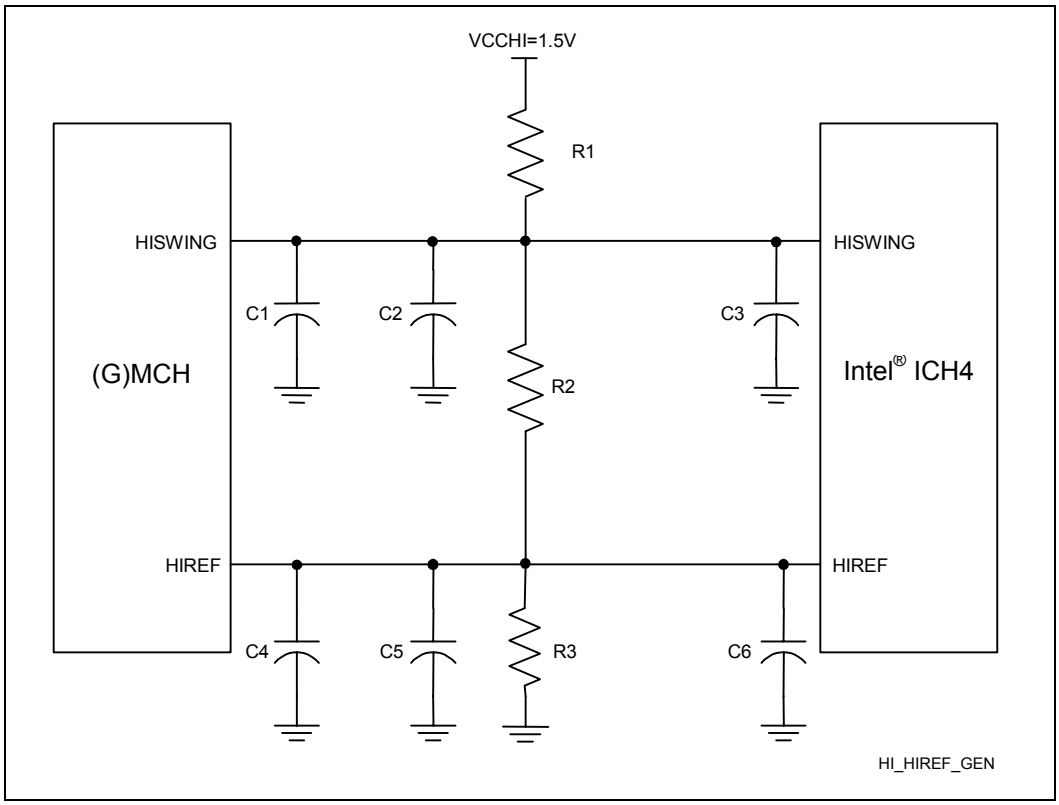
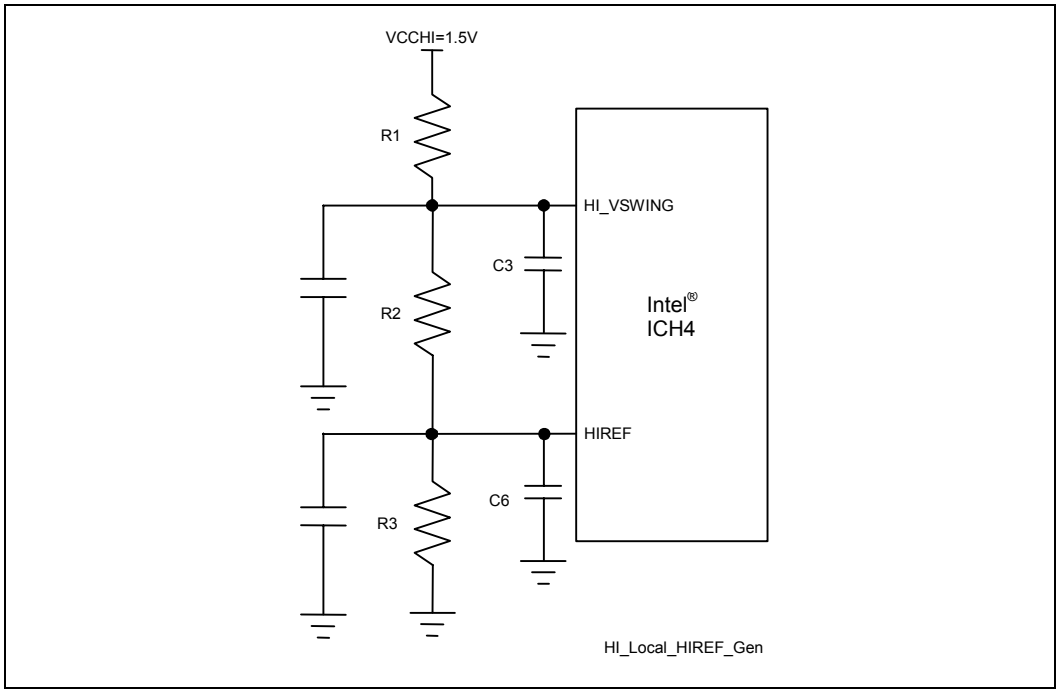


Figure 8-3. Hub Interface Local HI_REF/HI_VSWING Generation Circuit (Intel® ICH4 side)



8.1.5 Hub Interface Compensation

The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The Hub Interface requires Resistive Compensation (HICOMP).

Table 8-2. Hub Interface HICOMP Resistor Values

Trace Impedance	HICOMP Calculation	HICOMP Resistor Value	HICOMP Resistor Tied To
60Ω ± 15%	[(1.5 - 0.7) / (0.7)] * 60	68.1 Ω ± 1%	VCCHI = 1.5 V

8.1.6 Hub Interface Decoupling Guidelines

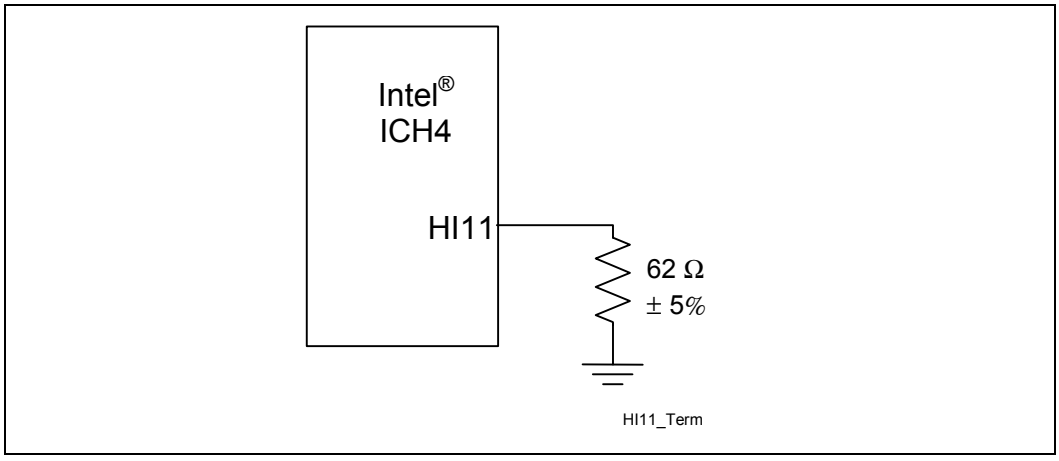
To improve I/O power delivery, use two 0.1 µF capacitors per each component (i.e., the ICH4 and (G)MCH). These capacitors should be placed within 100 mils from each package, adjacent to the rows that contain the Hub Interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCCHI=1.5 V side of the capacitors to the VCCHI=1.5 V power pins. Similarly, if layout allows, metal fingers running on the VCCHI=1.5 V side of the board should connect the ground side of the capacitors to the VSS power pins.

8.2 Additional Considerations

8.2.1 Hub Interface Intel® ICH4 Signals

The hub interface signal HI11 is an ICH4 only signal and does not exist on the (G)MCH. This ICH4 signal should be terminated to VSS through a 62 Ω ± 5% resistor.

Figure 8-4. Intel® ICH4 HI11 Termination



9 Intel® ICH4

9.1 IDE Interface

This section contains guidelines for connecting and routing the ICH4 IDE interface. The ICH4 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH4 has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors may be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5-mil traces on 7-mil spaces and must be less than 8 inches long (from ICH4 to IDE connector). Additionally, the maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inch.

Table 9-1. IDE Routing Summary

Trace Impedance	IDE Routing Requirements	Maximum Trace Length	IDE Signal Length Matching
51Ω to 69 Ω, 60 Ω Target	5 on 7	8 inches	No more than 0.5 inch (500 mils) between the shortest data signal and the longest strobe signal of a channel.

9.1.1 Cabling

Length of cable: Each IDE cable must be equal to or less than 18 inches.

Capacitance: Less than 35 pF.

Placement: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).

Grounding: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

9.1.1.1 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH4 IDE controller supports PIO, Multi-word (8237 style) DMA, and Ultra DMA modes 0 through 5, and native mode IDE. Note that there are no motherboard hardware requirements for supporting native mode IDE. Native mode IDE is supported through the operating system and system driver. The ICH4 must determine the type of cable that is present to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra ATA/66 and Ultra ATA/100. This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector).

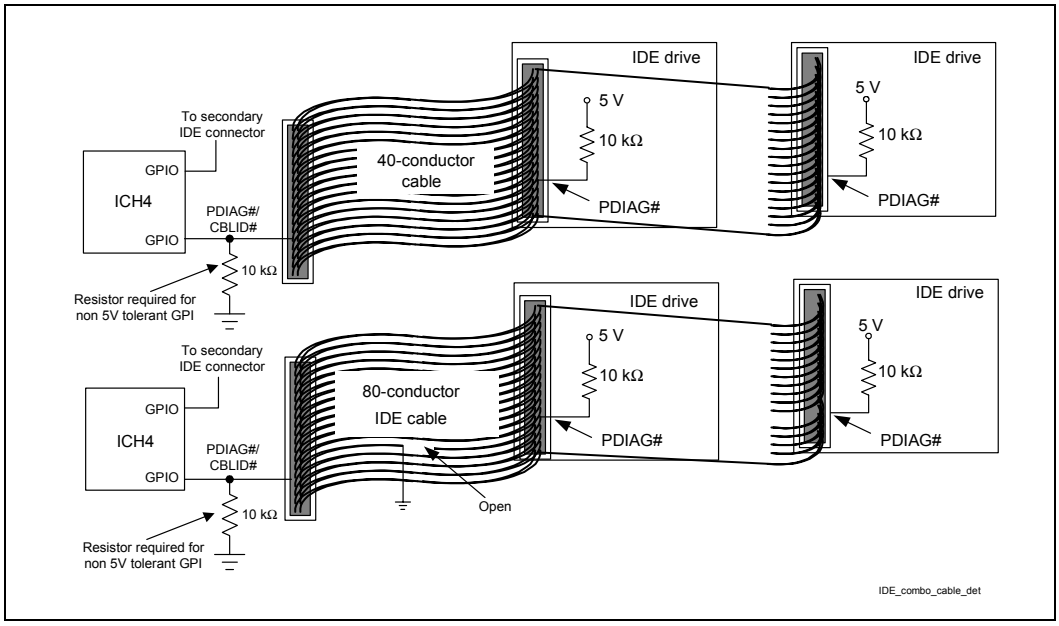
To determine if Ultra DMA modes greater than 2 (Ultra ATA/33) can be enabled, the ICH4 requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA mode 2 (Ultra ATA/33).

Intel recommends that cable detection be done using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system, because this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side Detection mechanism only.

9.1.1.2 Combination Host-Side/Device-Side Cable Detection

Host side detection (described in the *ATA/ATAPI-6 Standard*) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 9-1. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. A 10 kΩ pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present and allows for use of a non-5 V tolerant GPIO.

Figure 9-1. Combination Host-Side/Device-Side IDE Cable Detection



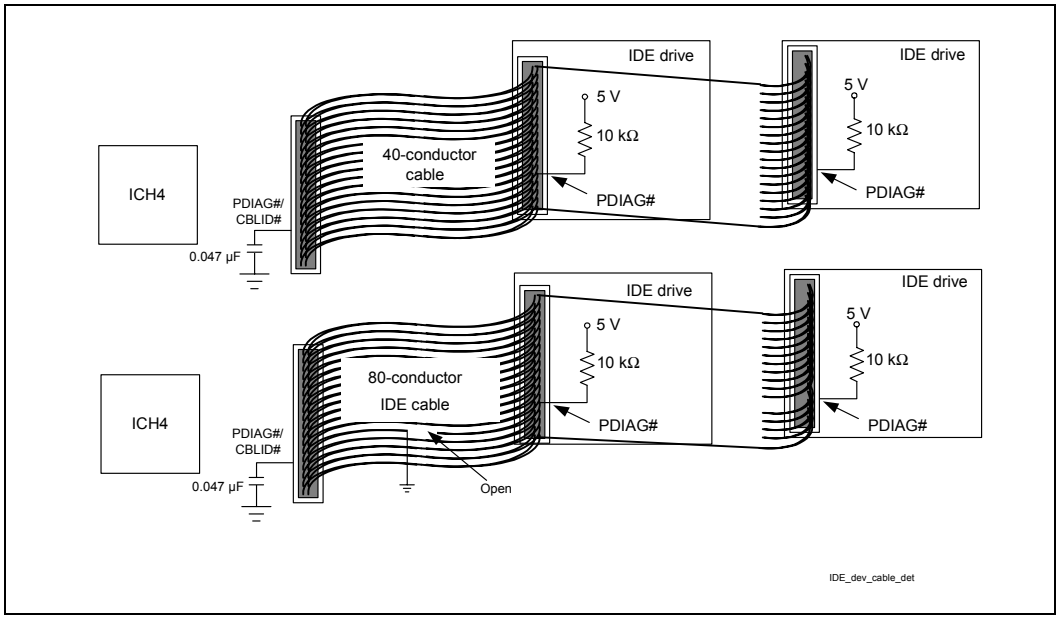
This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high, there is 40-conductor cable in the system and Ultra DMA modes greater than 2 must not be enabled.

If PDIAG#/CBLID# is detected low, there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the *ATA/ATAPI-6 Standard*. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13 is a 1, an 80-conductor cable is present. If this bit is 0, a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present, and notify the user of the problem.

9.1.1.3 Device-Side Cable Detection

For platforms that must implement Device-Side detection only (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in Figure 9-2. This capacitor should not be populated when implementing the recommended combination Host-Side/Device-Side cable detection mechanism described above. Note that some drives may not support device-side cable detection.

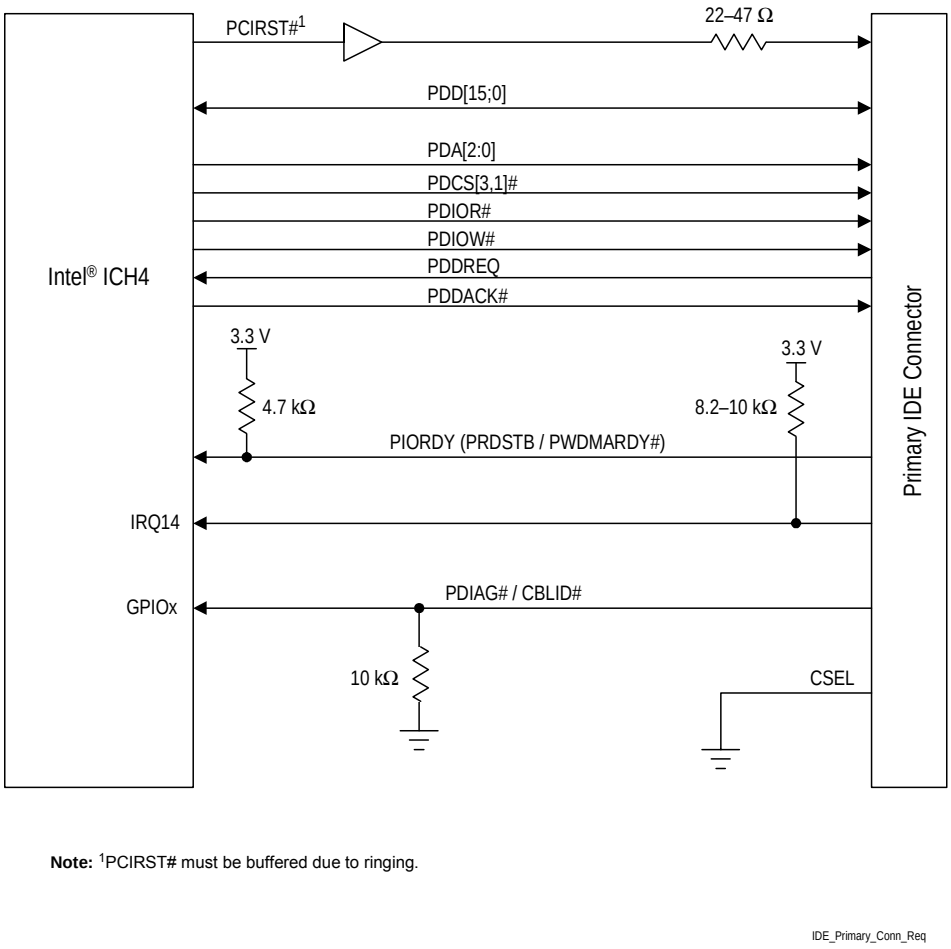
Figure 9-2. Device Side IDE Cable Detection



This mechanism creates a resistor-capacitor (RC) time constant. Drives supporting Ultra DMA modes greater than 2 (Ultra DMA/33) drive PDIAG#/CBLID# low and then release it (pulled up through a 10 kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host and therefore the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host. Therefore, the signal rises more slowly, as the capacitor charges. The drive can detect the difference in rise times and it will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the *ATA/ATAPI-6 Standard*.

9.1.2 Primary IDE Connector Requirements

Figure 9-3. Connection Requirements for Primary IDE Connector

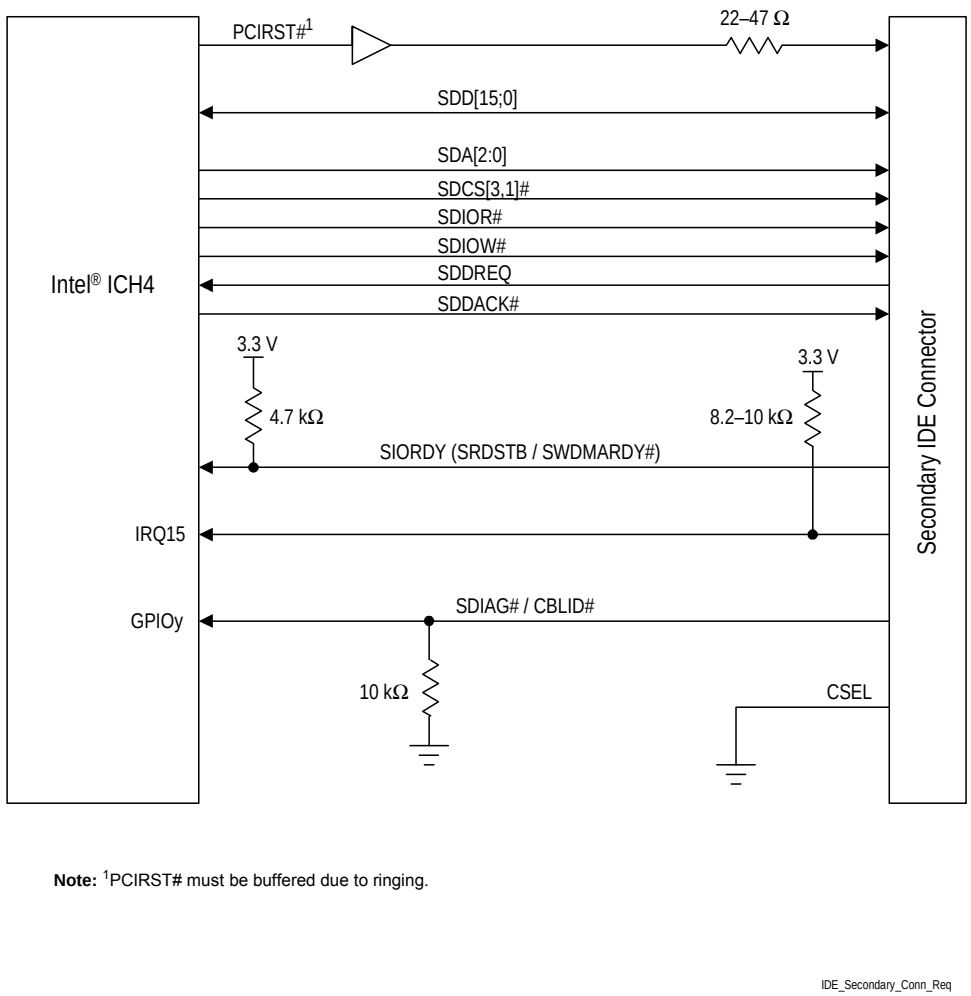


NOTES:

1. 22 kΩ – 47 kΩ series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 to VCC3_3.
3. A 4.7 kΩ pull-up resistor to VCC3_3 is required on PIORDY.
4. Series resistors can be placed on the control and data line to improve signal quality. The resistors are place as close to the connector as possible. Values are determined for each unique motherboard design.
5. The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is required on the primary connector. This change is to prevent the GPIO pin from floating if a device is not present on the IDE interface.

9.1.3 Secondary IDE Connector Requirements

Figure 9-4. Connection Requirements for Secondary IDE Connector



Note: [1]PCIRST# must be buffered due to ringing.

NOTES:

1. 22 kΩ – 47 kΩ series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ15 to VCC3_3.
3. A 4.7 kΩ pull-up resistor to VCC3_3 is required on SIORDY.
4. Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
5. The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is required on the secondary connector. This change is to prevent the GPIO pin from floating if a device is not present on the IDE interface.

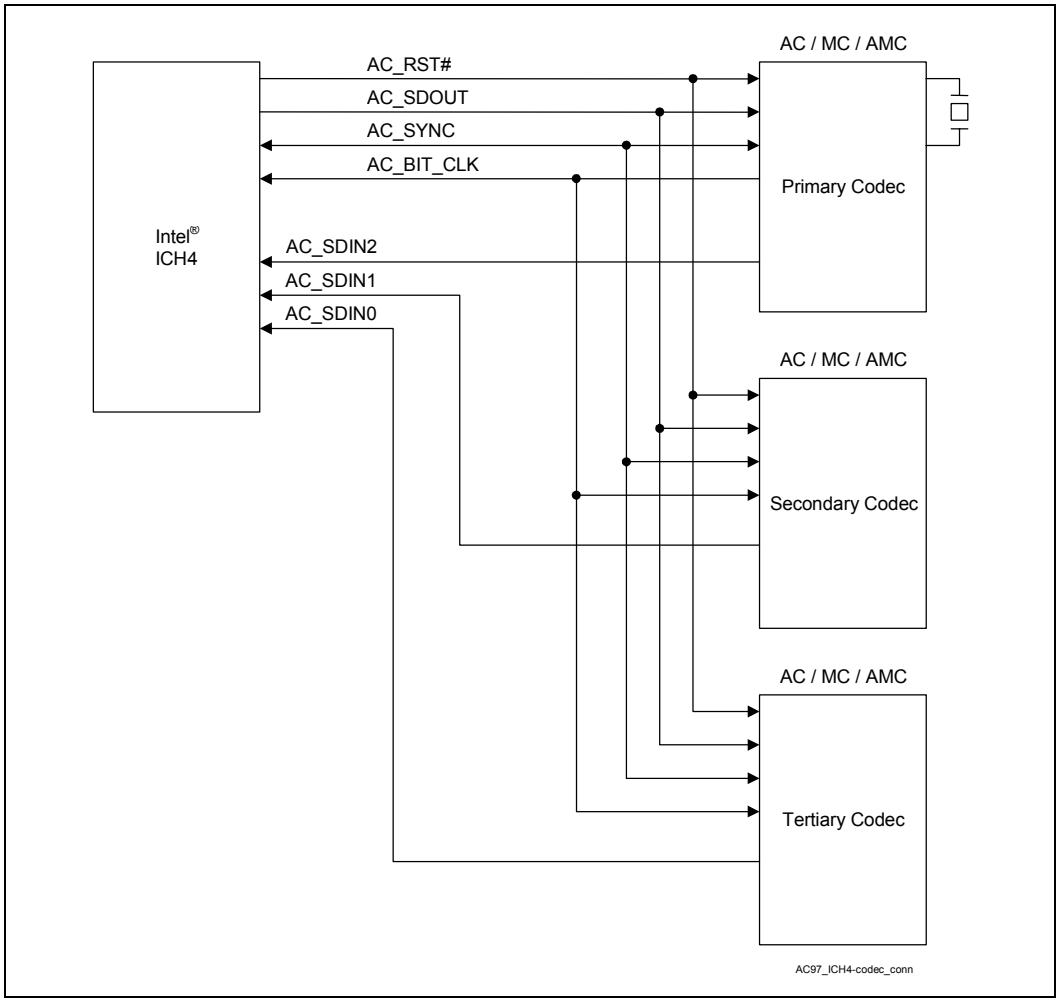
9.2 AC '97

The ICH4 implements an AC '97 2.3 compatible digital controller. Contact your codec IHV (Independent Hardware Vendor) for information on AC '97 2.3 compliant products. The AC '97 2.3 specification is on the Intel website:

http://developer.intel.com/ial/scalableplatforms/audio/index.htm#97spec

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH4 AC-link allows a maximum of three codecs to be connected. Figure 9-5 shows a three-codec topology of the AC-link for the ICH4.

Figure 9-5. Intel® ICH4 AC '97 — Codec Connection



NOTE: If a modem codec is configured as the primary AC-link Codec, there should not be any Audio Codecs residing on the AC-link. The primary codec must be connected to AC_SDIN2 if also routing to CNR. If no CNR exists on the platform, the primary codec may be connected to AC_SDIN0 (see the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet)*.

Using the assumed 4-layer stack-up, the AC '97 interface can be routed using 5 mil traces with 5-mil spacing between the traces. Maximum length between ICH4 to down CODEC is 14 inches. Maximum length between ICH4 to CNR is 14 inches. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 6 inches for the AC-link. Trace impedance should be $Z_0 = 60\ \Omega \pm 15\%$.

Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH4), and to any other codec present. That clock is used as the time base for latching and driving data. **Clocking AC_BIT_CLK directly off the CK408 14.31818 MHz clock is not supported.**

The ICH4 supports wake on ring from S1–S5 via the AC-link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH4 has weak pull-downs/pull-ups that are always enabled. This will keep the link from floating when the AC-link is off, or there are no codecs present.

If the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOUT will be driven by the codec and ICH4 respectively. However, AC_SDIN0, AC_SDIN1 and AC_SDIN2 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

Figure 9-6. Intel® ICH4 AC '97 — AC_BIT_CLK Topology

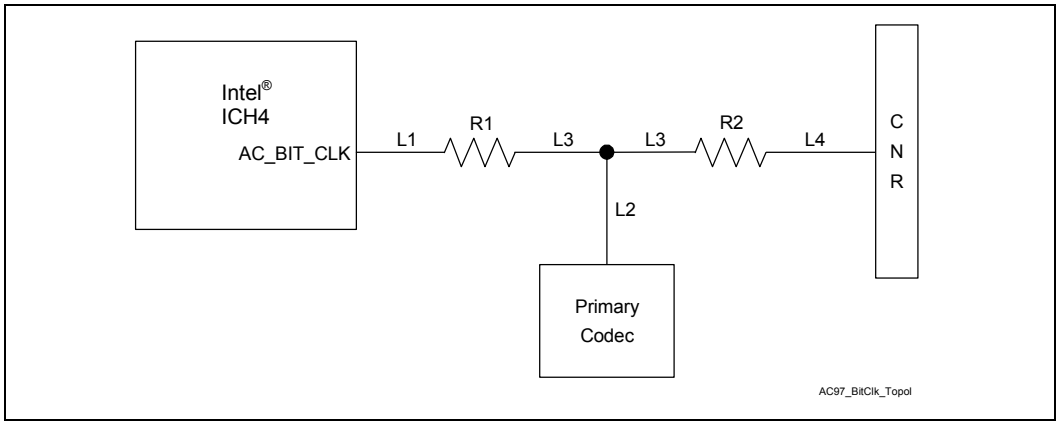


Table 9-2. AC '97 AC_BIT_CLK Clock Routing Summary

Trace Impedance	AC '97 Routing Requirements	Maximum Trace Length	Series Termination Resistance	AC_BIT_ CLK Signal Length Matching
51Ω to 69 Ω, 60 Ω Target	5 on 5	L1 = (1 to 8) – L3 inches L2 = (0.1 to 6) inches L3 = (0.1 to 0.4) inches L4 = (1 to 6) – L3 inches	R1 = 33 Ω - 47Ω R2 = Optional 0 Ω resistor for debug purposes	N/A

NOTES:
1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel 9750 codec

Figure 9-7. Intel® ICH4 AC '97 — AC_SDOUT/AC_SYNC Topology

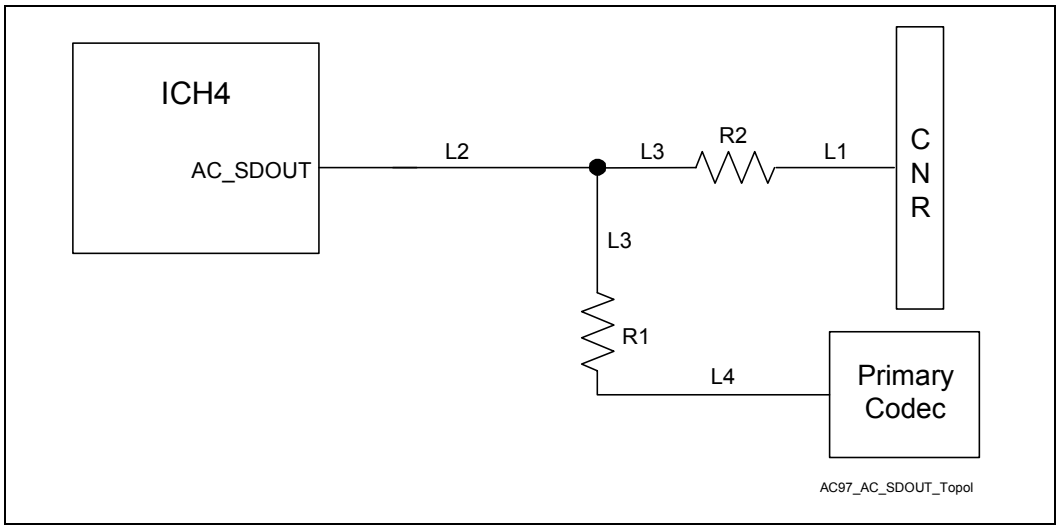


Table 9-3. AC '97 AC_SDOUT/AC_SYNC Routing Summary

Trace Impedance	AC '97 Routing Requirements	Maximum Trace Length	Series Termination Resistance	AC_SDOUT/ AC_SYNC Signal Length Matching
51Ω to 69Ω, 60 Ω Target	5 on 5	L1 = (1 to 6) – L3 inches L2 = (1 to 8) inches L3 = (0.1 to 0.4) inches L4 = (0.1 to 6) – L3 inches	R1 = 33 Ω – 47 Ω R2 = R1 if the CNR card that will be used with the platform does not have a series termination resistor on the card. Otherwise, R2 = 0 Ω	N/A

NOTES:
1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel 9750 codec

Figure 9-8. Intel® ICH4 AC '97 — AC_SDIN Topology

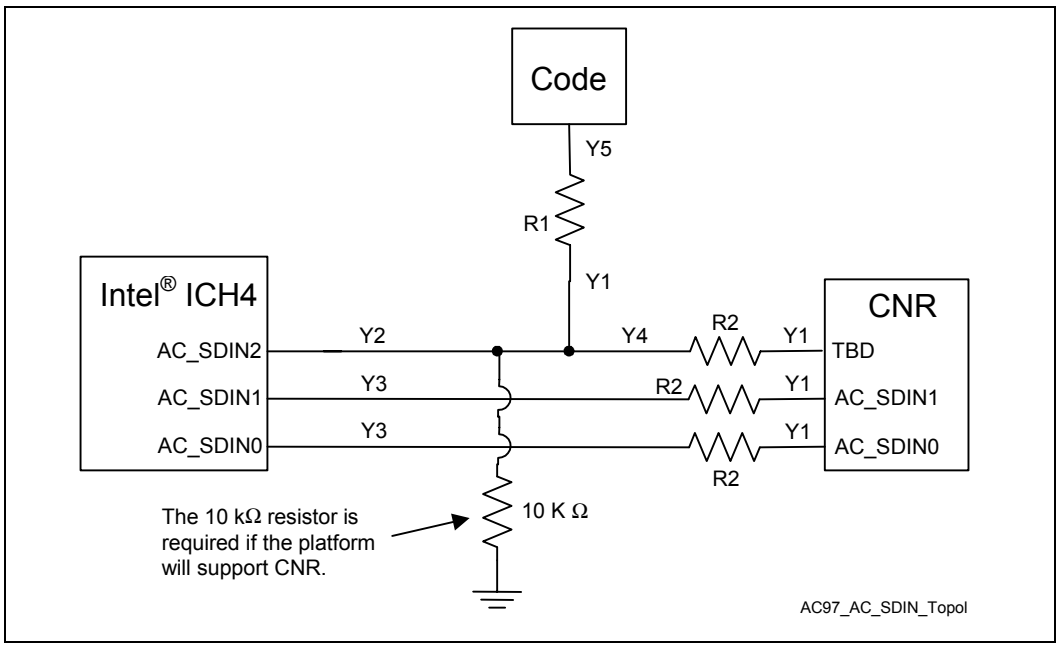


Table 9-4. AC '97 AC_SDIN Routing Summary

Trace Impedance	AC '97 Routing Requirements	Maximum Trace Length	Series Termination Resistance	AC_SDIN Signal Length Matching
50 Ω to 69 Ω, 60 Ω Target	5 on 5	Y1 = (0.1 to 0.4) inches Y2 = (1 to 8) – Y1 inches Y3 = (1 to 14) – Y1 inches Y4 = (1 to 6) – Y1 inches Y5 = (0.1 to 6) – Y1 inches	R1 = 33 Ω – 47 Ω R2 = R1 if the CNR card that will be used with the platform does not have a series termination resistor on the card. Otherwise, R2 = 0 Ω	N/A

NOTES:
1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel 9750 codec

9.2.1 AC '97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

9.2.2 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH4 platform using AC ’97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH4 platform.

- Active Components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH4 supports wake-on-ring from S1-S5 states via the AC-link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

9.2.2.1 Valid Codec Configurations

Table 9-5. Codec Configurations

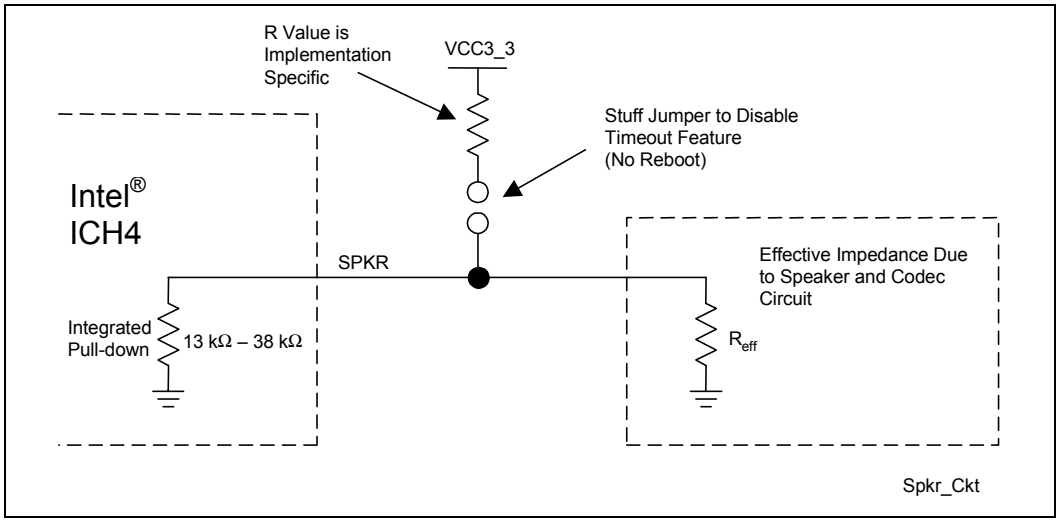
Option	Primary Codec	Secondary Codec	Tertiary Codec
1	Audio	Audio	Audio
2	Audio	Audio	Modem
3	Audio	Audio	Audio / Modem
4	Audio	Modem	Audio
5	Audio	Audio / Modem	Audio
6	Audio / Modem	Audio	Audio

NOTES:
1. For power management reasons, codec power management registers are in audio space. As a result, if there is an audio codec in the system, it must be Primary.
2. There cannot be two modems in a system because there is only one set of modem DMA channels
3. The ICH4 supports a modem codec on any of the AC_SDIN lines; however, the Modem Codec ID must be either 00 or 01.

9.2.3 SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH4 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see Figure 9-9). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{eff}), and the ICH4 integrated pull-down resistor will be read as logic high (0.5 VCC3_3 to VCC3_3 + 0.5 V).

Figure 9-9. Example Speaker Circuit



9.3 CNR

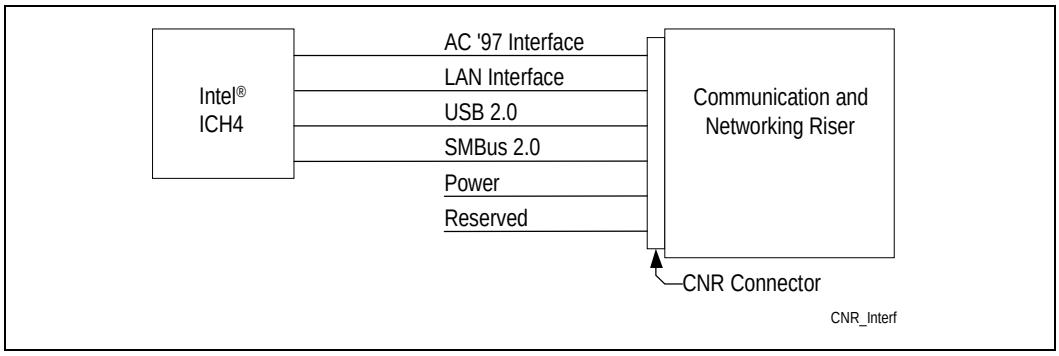
The Communication and Networking Riser (CNR) Specification defines a hardware scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. For more information on the specification, refer to the following document:

- *Communication Network Riser Specification Revision 1.2*
  Available at http://developer.intel.com/technology/cnr

The CNR interface supports multi-channel audio, V.90 analog modem, phone-line based networking, 10/100 Ethernet based networking, SMBus Interface Power Management Revision 1.1, and USB 2.0. The CNR specification defines the interface, which should be configured prior to shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot; therefore, the system designer will not sacrifice a PCI slot if they decide not to include a CNR in a particular build.

Figure 9-10 indicates the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. The Platform LAN connection (PLC) can either be an 82562ET/EZ or 82562EM/EX component. Refer to the CNR specification for additional information.

Figure 9-10. CNR Interface



9.3.1 AC ’97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. Refer to the *Communication Network Riser Specification, Revision 1.2* for Intel’s recommended codec configurations

Table 9-6. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, this signal indicates that the codec on the motherboard is enabled and primary on the AC ’97 Interface. When high, the signal indicates that the motherboard codec(s) must be removed from the AC ’97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC ’97 Interface.
AC_RST#	Reset signal from the AC ’97 Digital Controller (ICH4).
AC_SDIN*n*	AC ’97 serial data from an AC ’97-compaible t codec to an AC ’97-compatible controller (i.e., the ICH4).

9.3.1.1 CNR 1.2 AC ’97 Disable and Demotion Rules for the Motherboard

The following are the CNR1.1/1.2 AC ’97 disable and demotion rules for the motherboard.

- All AC ’97 Revision 2.2 *non-chaining* codecs on the motherboard **must** always disable themselves when the CDC_DWN_ENAB# signal is in a high state.
- A motherboard AC ’97 codec **must** never change its address or AC_SDIN line used, regardless of the state of the CDC_DWN_ENAB# signal.
- A motherboard containing an AC ’97 controller supporting three AC ’97 codecs the AC ’97 Revision 2.2 or AC ’97 Revision 2.3 codec, on the motherboard, **must** be connected to the AC_SDIN2 signal of the CNR connector.
- A motherboard should not contain any more than a single AC ’97 codec.

These rules allow for forward and backward compatibility between CNR Version 1.1/1.2 cards. For more information on chaining, consult the *Communication Network Riser Specification, Revision 1.2*.

Figure 9-11. Motherboard AC '97 CNR Implementation with a Single Codec Down On Board

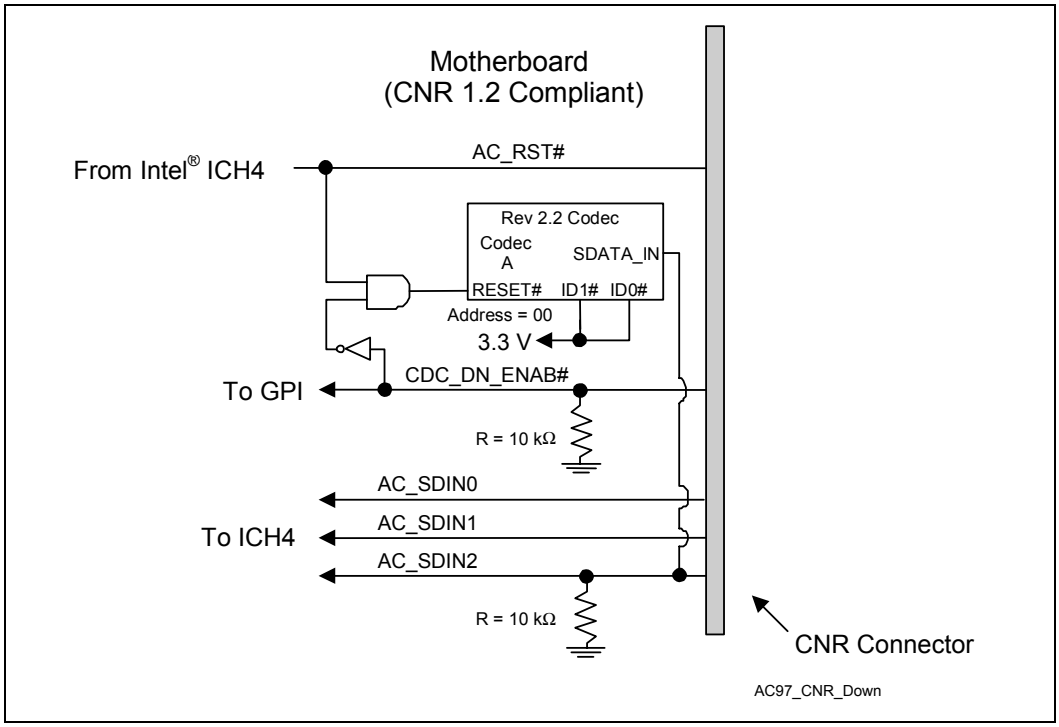
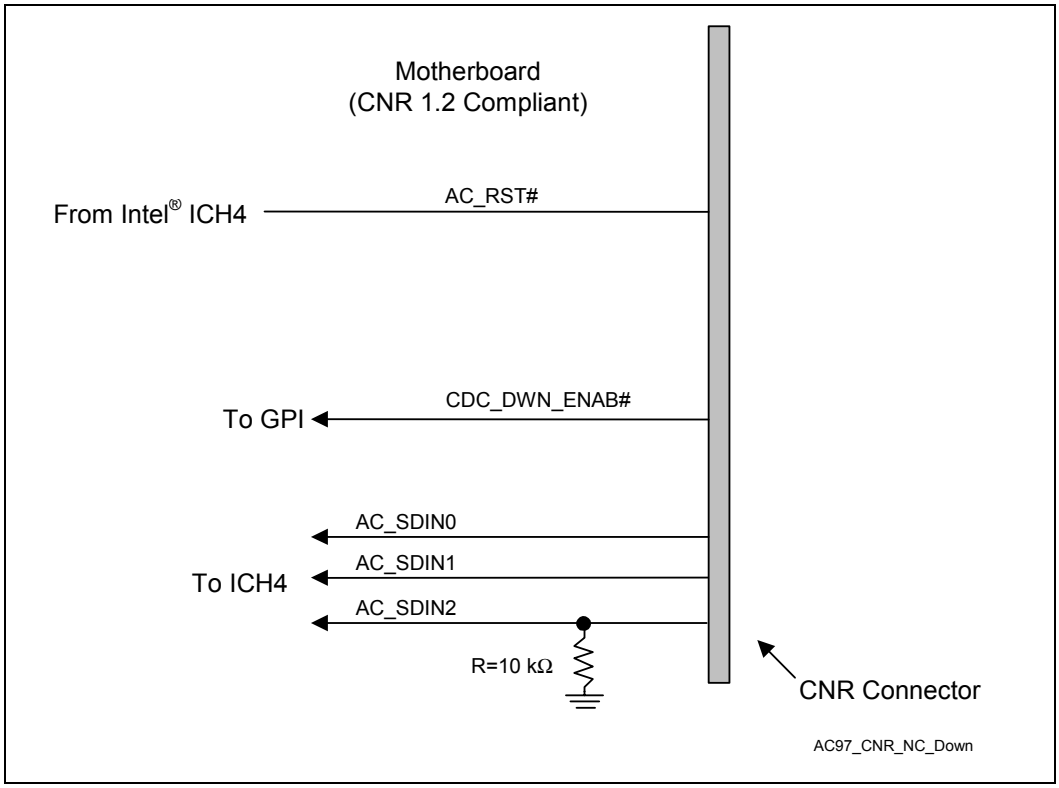


Figure 9-12. Motherboard AC '97 CNR Implementation with No Codec Down On Board



9.3.2 CNR Routing Summary

Table 9-7 is a summary of the various interfaces routing requirements to the CNR Riser.

Table 9-7. CNR Routing Summary

Trace Impedance	CNR Routing Requirements	Maximum Trace Length to CNR Connector	Signal Length Matching	Signal Referencing
77 Ω to 103 Ω Differential, 90 Ω Differential Target	USB (7.5 on 7.5) Data pair must be at least 20 mils from nearest neighbor	10 inches	No more than 150-mils trace mismatch	Ground
51 Ω to 69 Ω, 60 Ω Target	AC '97 (5 on 5)	AC_BIT_CLK (See Table 9-2) AC_SDOUT (See Table 9-3) AC_SDIN (See Table 9-4)	N/A	Ground
51 Ω to 69 Ω, 60 Ω Target	LAN (5 on 10)	9.5 inches (See Table 9-19)	Equal to or up to 500 mils shorter than the LAN_CLK trace	Ground

9.4 USB 2.0

9.4.1 Layout Guidelines

9.4.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems. The USB 2.0 validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second plane is power, the third plane is ground and the fourth is a signal layer. This results in placing most of the routing on the fourth plane closest to the ground plane, and allowing a higher component density on the first plane.

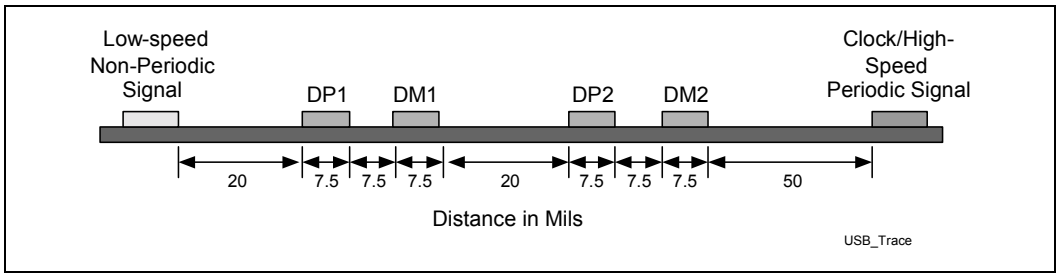
- Place the ICH4 and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
- USB 2.0 signals should be ***ground referenced***
- Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
- When it becomes necessary to turn 90 degree, use two 45-degree turns or an arc instead of making a single 90-degree turn. This reduces reflections on the signal by minimizing impedance discontinuities. (See Figure 9-41).
- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices, or IC's that use and/or duplicate clocks.
- Stubs on high speed USB signals should be avoided, as stubs will cause signal reflection and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils.
- Route all traces over continuous planes (VCC or GND) with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 9.4.2.
- Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
- Keep USB 2.0 signals clear of the core logic set. High current transients are produced during internal state transitions, which can be very difficult to filter out.
- Follow the 20*h thumb rule by keeping traces at least 20* (height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack-up the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

9.4.1.2 USB 2.0 Trace Separation

Use the following separation guidelines. Figure 9-13 shows the recommended trace spacing.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. Deviations normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.
- Use an impedance calculator to determine the trace width and spacing required for the specific board stack-up being used. For the board stack-up parameters referred to in Section 3.2, 7.5-mil traces with 7.5-mil spacing results in approximately 90 Ω differential trace impedance.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

Figure 9-13. Recommended USB Trace Spacing



9.4.1.3 USBRBIAS Connection

The USBRBIAS pin and the USBRBIAS# pin can be shorted and routed 5 on 5 to one end of a 22.6 Ω ± 1% resistor to ground. Place the resistor within 500 mils of the ICH4 and avoid routing next to clock pins.

Figure 9-14. USBRBIAS Connection

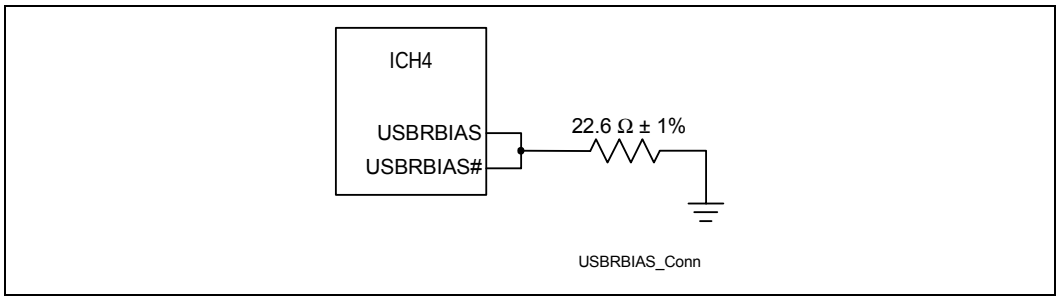


Table 9-8. USBRBIAS/USBRBIAS# Routing Summary

Trace Impedance	USBRBIAS/ USBRBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
51 Ω to 69 Ω, 60 Ω Target	5 on 5	500 mils	N/A	N/A

9.4.1.4 USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See Section 9.4.4 for common-mode choke details.

9.4.1.5 USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pair should be no greater that 150 mils.

9.4.1.6 USB 2.0 Trace Length Guidelines

Use the following trace length guidelines.

Table 9-9. USB 2.0 Trace Length Preliminary Guidelines (with Common-Mode Choke)

Trace Imped.	USB 2.0 Routing Req.	Topology	Signal Ref	Signal Matching	Motherboard Trace Length	Card Trace Length	Maximum Total Length
77Ω to 103 Ω differential, 90 Ω Differential Target	7.5 on 7.5	Back Panel	Ground	The max mismatch between data pairs should not be greater than 150 mils	17 inches	N/A	17 inches
		CNR			8 inches	6 inches	14 inches
		Front Panel			**Cable Length** / **Motherboard Trace Length** / **Daughter Card Trace Length** / **Max. Total Length**		
					9 / 6 / 2 / 17		
					10.5 / 5 / 2 / 17.5		
					12 / 4 / 2 / 18		
					13.5 / 3 / 2 / 18.5		
					15 / 2 / 2 / 19		

NOTES:
1. These lengths are based upon simulation results and may be updated in the future.
2. All lengths are based upon using a common-mode choke (see Section 9.4.4.1 for details on common-mode choke).
3. Numbers in this table are based on the following simulation assumptions:
   CNR configuration: max 6 inches trace on add-on card.
4. An Approximate 1:1 trade-off can be assumed from Motherboard Trace Length vs. Daughter card Trace Length (e.g., trade 1 inch of Daughter card for 1 inch of Motherboard Trace Lengths).
5. Routing guidelines are based on the stack-up assumptions in Section 3.2
6. Numbers in this table are based on the following simulation assumptions
   a. Trace length on front panel connector card assumed a max of 2 inches.
   b. USB twisted-pair shielded cable as specified in USB 2.0 specification was used.
7. For front panel solutions, signal matching is considered from the ICH4 to the front panel header.

9.4.2 Plane Splits, Voids and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cutouts.

9.4.2.1 VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the VCC plane.

- Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them. USB signaling is not purely differential in all speeds (i.e. the full-speed single-ended zero is common mode).
- Avoid routing of USB 2.0 signals 25-mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

If crossing a plane split is completely unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates VCC5 and VCC3_3 planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to VCC5 and the other side should tie to VCC3_3. Stitching caps provide a high-frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

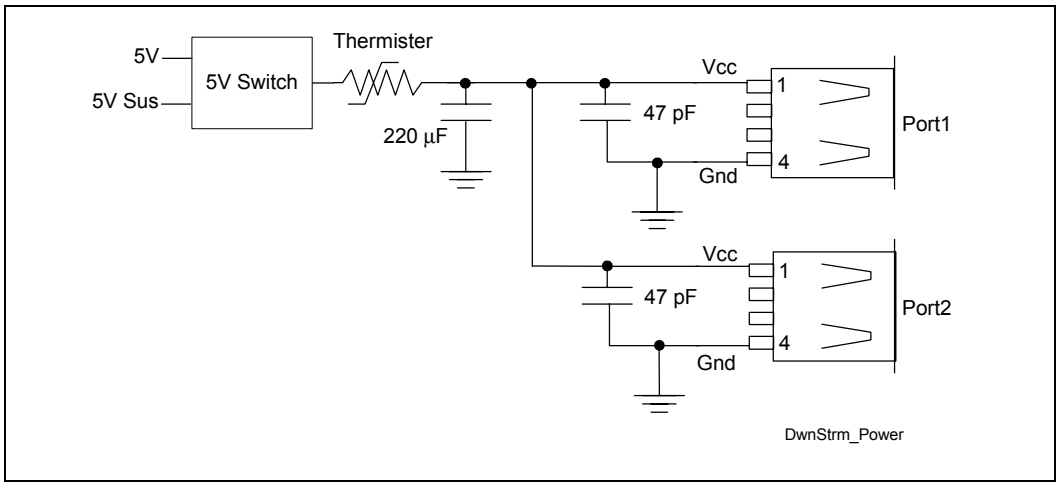
9.4.2.2 GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

9.4.3 USB Power Line Layout Topologies

The following is a suggested topology for power distribution of VBUS to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach flyback protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach flyback voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane. A good "rule-of-thumb" is to make the power-carrying traces wide enough that the system fuse will blow on an over current event. If the system fuse is rated at 1amps then the power-carrying traces should be wide enough to carry at least 1.5 amps.

Figure 9-15. Good Downstream Power Connection



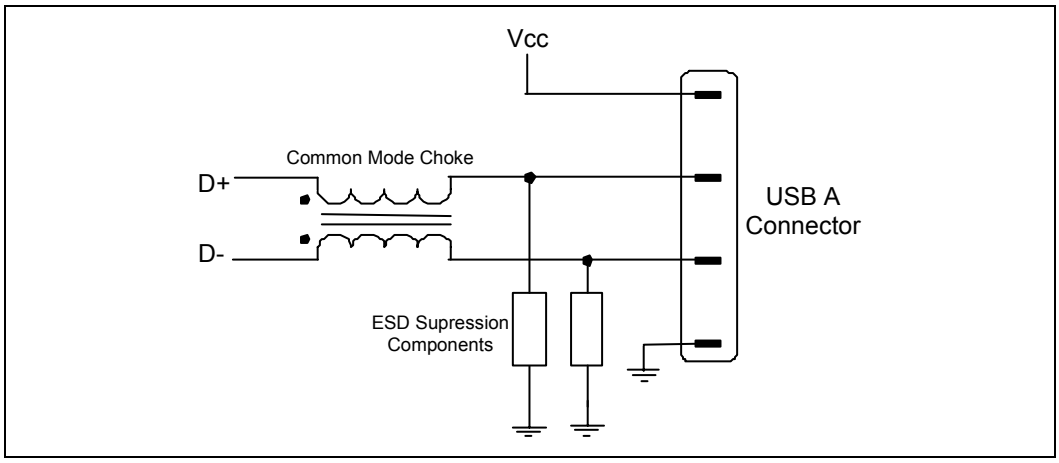
9.4.4 EMI Considerations

The following guidelines apply to the selection and placement of common chokes and ESD protection devices.

9.4.4.1 Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design should include a common mode choke footprint to provide a stuffing option **in the event** the choke is needed to pass EMI testing. Figure 9-16 shows the schematic of a typical common mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins. In systems that route USB to a front panel header the choke should be placed on the front panel card.

Figure 9-16. A Common-Mode Choke



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion will increase, so the effects of the common mode choke on full-speed and high-speed signal quality should be tested. Common Mode Chokes with a target impedance of 80 Ω to 90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's requirements is a two-step process.

- A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
- Once you have a part that gives passing EMI results the second step is to test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for Low-speed, Full-speed and High-speed USB operation.

9.4.5 ESD

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common mode choke and the USB connector data pins as shown in Figure 9-16. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, it is recommended to include footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

9.4.6 Front Panel Solutions

9.4.6.1 Internal USB Cables

The front panel internal cable solution chosen must meet all the requirements of Chapter 6 of the *USB 2.0 Specification* for high-/full-speed cabling for each port with the exceptions described in Cable Option 2.

9.4.6.1.1 Internal Cable Option 1

Use standard High-Speed/Full-Speed compatible USB cables. These must meet all cabling requirements called out in Chapter 6 of the *USB 2.0 Specification*. Recommended motherboard mating connector pin-out is covered in detail later in this document.

9.4.6.1.2 Internal Cable Option 2

Use custom cables that meet all of the requirements of Chapter 6 of *the USB 2.0 Specification* with the following additions/exceptions.

- They can share a common jacket, shield and drain wire.
- Two ports with signal pairs that share a common jacket may combine VBUS and ground wires into a single wire provided the following conditions are met:
  a. The bypass capacitance required by Section 7.2.4.1 of the USB 2.0 Specification is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughter card). Refer to the front panel daughter card referenced later for details.
  b. Selecting proper wire size: A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the USB 2.0 Specification that has ≤ ½ the resistance of either of the two wires being combined. The data is provided for reference in Table 9-10.

Table 9-10. Conductor Resistance

American Wire Gauge (AWG)	Ohm (Ω) / 100 Meters Maximum
28	23.20
26	14.60
24	9.09
22	5.74
20	3.58

Example: 2 – 24 gauge (AWG) power or ground wires can be replaced with one 20-gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the *USB 2.0 Specification* at the USB connectors as well as at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure the system passes droop requirements. Cables that provide individual power and ground conductors for each port can usually meet droop requirements by providing adequate capacitance near the motherboard mating connector because droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case, all transients will be seen/dampened by the capacitance at the motherboard mating connector before they can cause problems with the adjacent port sharing the same cable. See section 7.2.2 and 7.2.4.1 of the *USB 2.0 Specification* for more details.

Cables that contain more than two signal pairs are not recommended due to unpredictable impedance characteristics.

9.4.6.2 Motherboard/PCB Mating Connector

Proper selection of a motherboard mating connector for front panel USB support is important to ensure signal quality is not adversely affected due to a poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the *USB 2.0 Specification*.

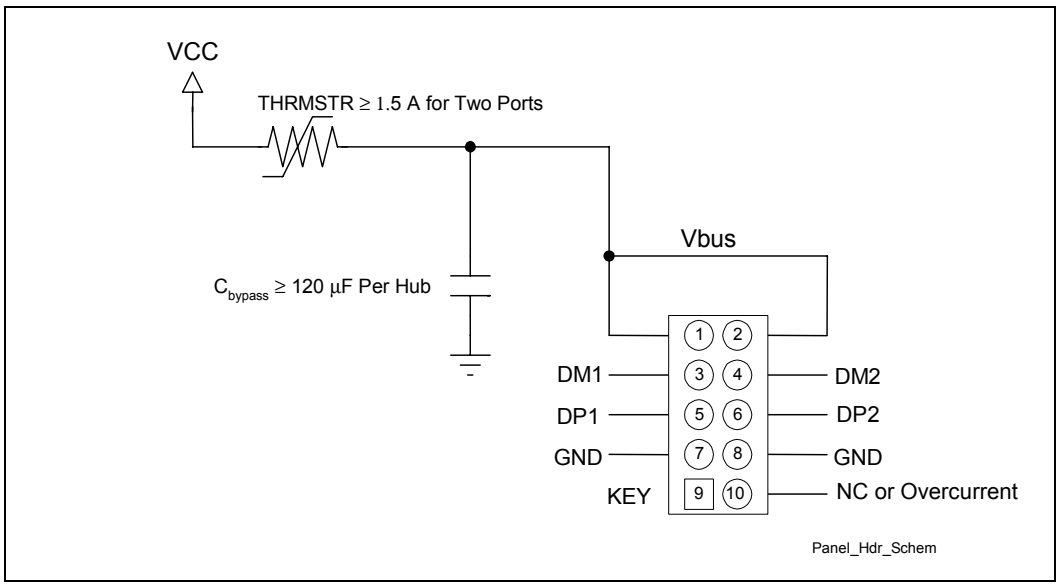
9.4.6.2.1 Pinout

A ten pin, 0.1-inch pitch stake pin assembly is recommended with the pinout listed in Table 9-11 and in the following schematic.

Table 9-11. Front Panel Header Pinout

Pin	Description
1	VCC
2	VCC
3	Dm1
4	Dm2
5	Dp1
6	Dp2
7	Gnd
8	Gnd
9	key
10	No connect or over-current sense

Figure 9-17. Front Panel Header Schematic



It is **highly** recommended that the fuse element (thermistor) for the front panel header be included on the motherboard to protect the motherboard from damage.

- This protects the motherboard from damage in the case where an un-fused front panel cable solution is used.
- It also provides protection from damage if an un-keyed cable is inadvertently plugged onto the front panel USB connector.
- It provides protection to the motherboard in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between VBUS and ground.

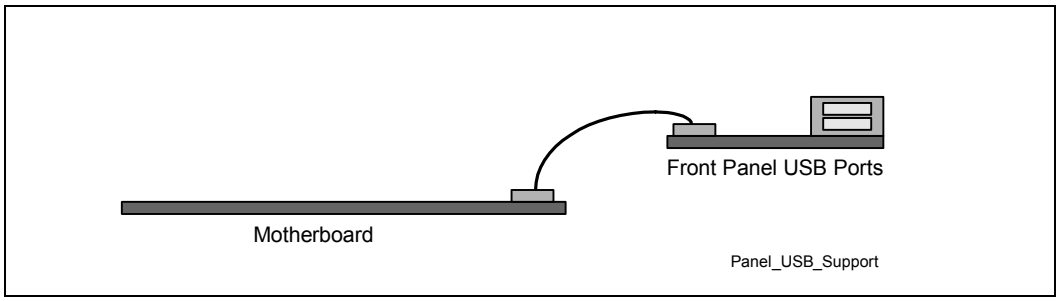
9.4.6.2.2 Routing Considerations

- Traces or surface shapes from VCC to the thermistor, to Cbypass and to the connector power and ground pins should be at least 50-mils wide to ensure adequate current carrying capability.
- There should be double vias on power and ground nets and the trace lengths should be kept as short as possible.

9.4.6.3 Front Panel Connector Card

The best way to provide front or side panel support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. Figure 9-18 shows the major components associated with a typical front/side panel USB solution that uses a front panel connector card.

Figure 9-18. Motherboard Front Panel USB Support



Note: The terms "connector card" and "daughter card" are used interchangeably.

When designing the motherboard with front/side panel support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a connector card, ensure that there aren't duplicate EMI/ESD/thermistor components placed on the motherboard, as this will usually cause drop/droop and signal quality degradation or failure.

9.4.6.3.1 Front Panel Daughter Card Design Guidelines

- Place the VBUS bypass capacitance, Common Mode Choke, and ESD suppression components on the daughter card as close as possible to the connector pins.
- Follow the same layout, routing and impedance control guidelines as specified for motherboards.
- Minimize the trace length on the front panel connector card. Less than 2-inch trace length is recommended.
- Use the same mating connector pin-out as outlined for the motherboard in Section 9.4.6.2.1.
- Use the same routing guidelines as described in Section 9.4.1.
- Trace length guidelines are given in Table 9-9.

9.5 I/O APIC Design Recommendation

UP systems not using the IOAPIC Bus should follow these recommendations:

On the ICH4

- Tie APICCLK directly to ground
- Tie APICD [1:0] to ground through a 10 kΩ resistor (Separate pull-downs are required if using XOR chain testing.)

On the processor

- Consult processor documentation

9.5.1 PIRQ Routing Example

Table 9-12 describes how the ICH4 uses the PCI IRQ when the I/O APIC is active.

Table 9-12. IOAPIC Interrupt Inputs 16 Through 23 Usage

No	I/O APIC INTIN PIN	Function in Intel® ICH4 Using the PCI IRQ in IOAPIC
1	I/O APIC INTIN PIN 16 (PIRQA)	USB1 UHCI Controller 1
2	I/O APIC INTIN PIN 17 (PIRQB)	AC '97 Audio and Modem; option for SMBus
3	I/O APIC INTIN PIN 18 (PIRQC)	USB1 UHCI Controller 3; Native IDE
4	I/O APIC INTIN PIN 19 (PIRQD)	USB1 UHCI Controller 2
5	I/O APIC INTIN PIN 20 (PIRQE)	Internal LAN; option for SCI, TCO, MMT 0,1,2
6	I/O APIC INTIN PIN 21 (PIRQF)	Option for SCI, TCO, MMT 0,1,2
7	I/O APIC INTIN PIN 22 (PIRQG)	Option for SCI, TCO, MMT 0,1,2
8	I/O APIC INTIN PIN 23 (PIRQH)	USB2 EHCI Controller, Option for SCI, TCO, MMT 0,1,2

Due to different system configurations, IRQ line routing to the PCI slots ("swizzling") should be made to minimize the sharing of interrupts between both internal ICH4 functions and PCI functions. Figure 9-19 shows an example of IRQ line routing to the PCI slots (note: it is not necessarily an optimal routing scheme; an optimal scheme depends on individual system PCI IRQ usage).

Figure 9-19. Example PIRQ Routing

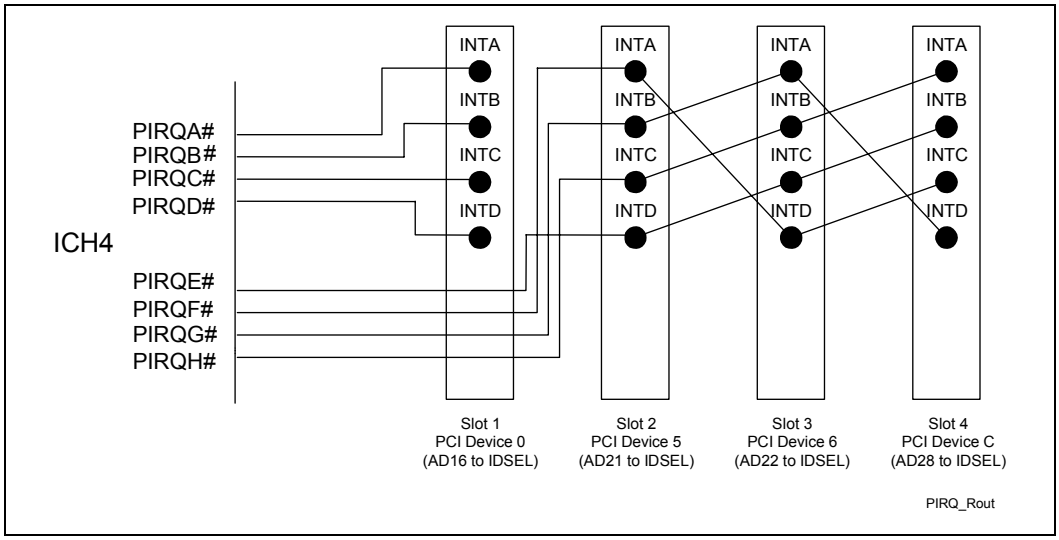


Figure 9-19 is an example. It is up to the board designer to route these signals in a way that will prove the most efficient for their particular system. A PCI slot can be routed to share interrupts with any of the ICH4 internal device/functions (but at a higher latency cost).

9.6 SMBus 2.0/SMLink Interface

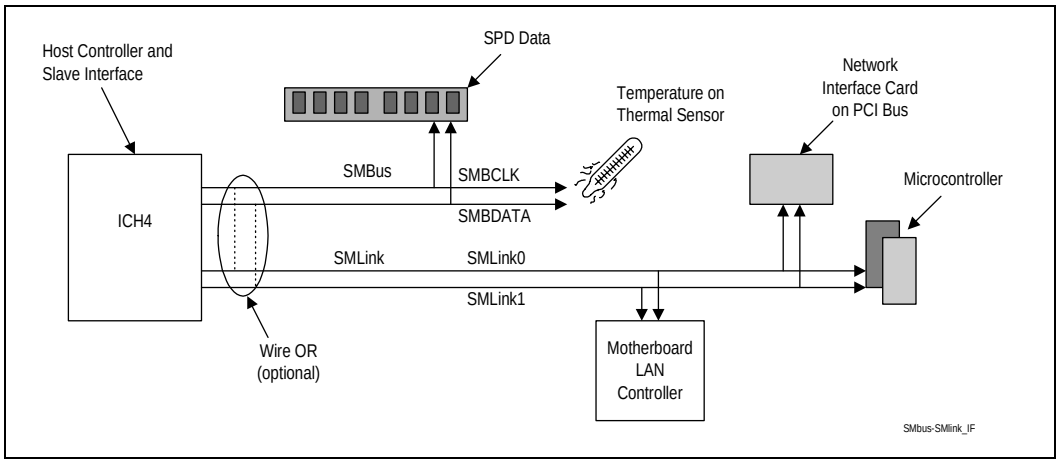
The SMBus interface on the ICH4 uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH4.

The ICH4 incorporates an SMLink interface supporting Alert on LAN*, Alert on LAN2* and a slave functionality. It uses two signals SMLINK[1:0]. SMLINK0 corresponds to an SMBus clock signal and SMLINK1 corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert on LAN* functionality, the ICH4 transmits heartbeat and event messages over the interface. When using the 82562EM/82562EX platform LAN connect component, the ICH4 integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert on LAN2*-enabled LAN Controller (i.e., 82562EM/82562EX 10/100 Mbps platform LAN connect) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH4 SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (such as 82562EM/82562EX 10/100 Mbps platform LAN connect) to access targets on the SMBus as well as the ICH4 Slave interface. Additionally, the ICH4 supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, to be fully compliant with the SMBus 2.0 specification (which requires the Host Notify cycle), the SMLink and SMBus signals **must** be tied together externally. This is done by connecting SMLink0 to SMBCLK and SMLink1 to SMBDATA.

Figure 9-20 SMBUS 2.0/SMLink Interface



Note: Intel does not support external access of the ICH4 Integrated LAN Controller via the SMLink interface. Also, Intel does not support access of the ICH4 SMBus Slave Interface by the ICH4 SMBus Host Controller. Refer to the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

9.6.1 SMBus Architecture and Design Considerations

SMBus Design Considerations

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging because they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in choosing a design are based on:

- Devices that must run in S3
- Amount of VCC_Suspend current available (i.e., minimizing load of VCC_Suspend)
- Device class: High power/Low power. Most designs use primarily high power devices.

General Design Issues / Notes

Regardless of the architecture used, there are some general considerations.

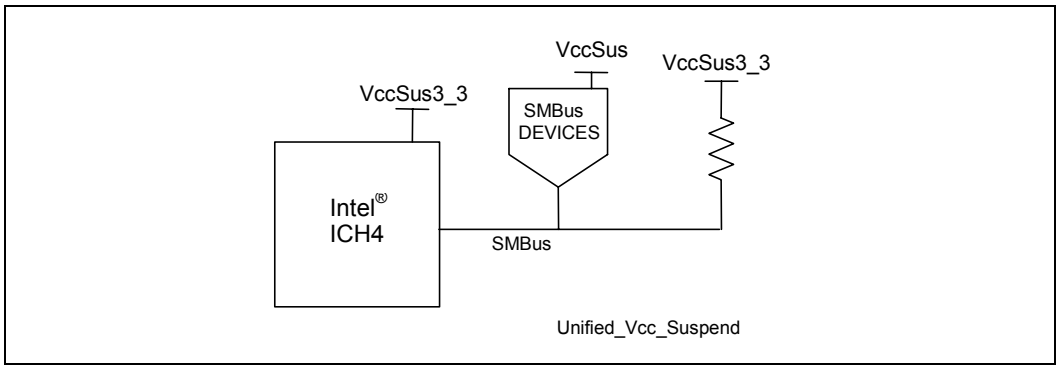
- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor can not be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and fall time specification.
- The maximum bus capacitance that a physical segment can reach is 400 pF.
- The ICH4 does not run SMBus cycles while in S3
- SMBus devices that can operate in S3 must be powered by the VCC_Suspend supply.
- If SMBus is to be connected to PCI, it must be connected to all PCI slots.

9.6.1.1 Power Supply Considerations

The Unified VCC_ Suspend Architecture

In this design all SMBus devices are powered by the VCC_Suspend supply. Consideration must be made to provide enough VCC_Suspend current while in S3.

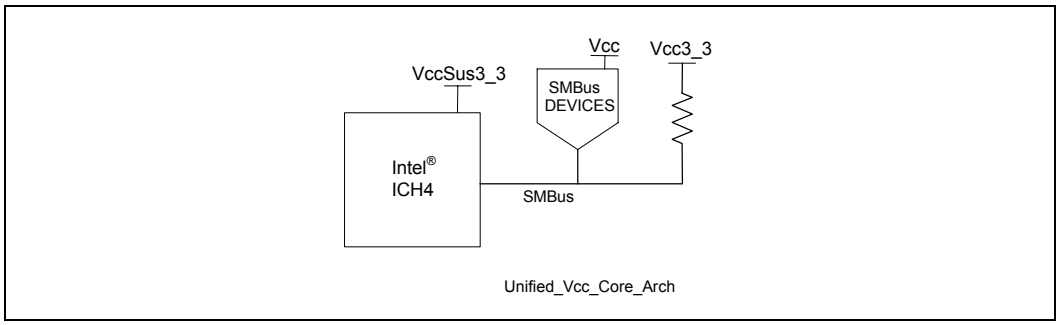
Figure 9-21. Unified VCC_Suspend Architecture



The Unified VCC_CORE Architecture

In this design, all SMBUS devices are powered by the VCC_CORE supply. This architecture allows none of the devices to operate in S3, but minimizes the load on VCC_Suspend.

Figure 9-22. Unified VCC_CORE Architecture

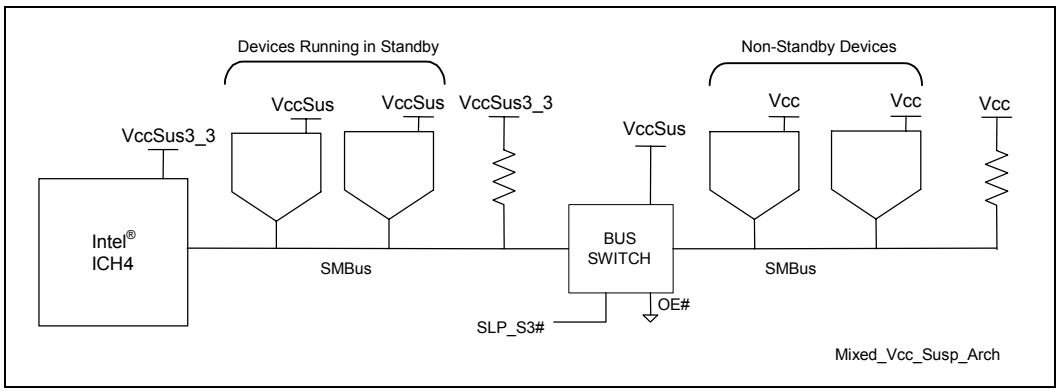


NOTES:
1. The SMBus device must be back-drive safe while its supply (Vcore) is off and VCC_Suspend is still powered.
2. In suspended modes where VCC_CORE is OFF & VCC_Suspend is on, the VCC_CORE node will be very near ground. In this case the input leakage of the ICH4 will be approximately 10 uA.

Mixed Power Supply Architecture

This design allows for SMBus devices to communicate while in S3, yet minimizes VCC_Suspend leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a "bus switch" to isolate the devices powered by the core and suspend supplies. See Figure 9-23.

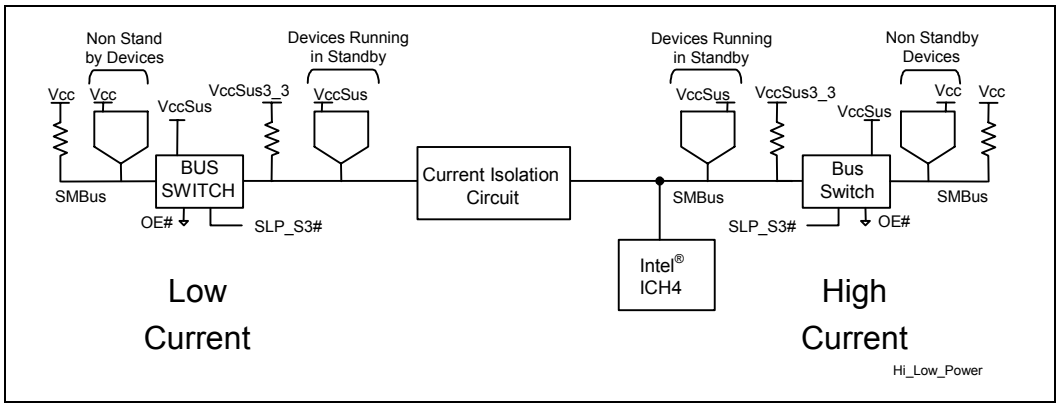
Figure 9-23. Mixed VCC_Suspend/VCC_CORE Architecture



9.6.1.2 Device Class Considerations

In addition to the power supply considerations described above, system designers should take into consideration the SMBus device class (high power/low power) used on the bus. If the design supports both high- power and low-power devices on the bus, current isolation of high-power segment and low-power segment of the bus is needed as shown in Figure 9-24.

Figure 9-24. High Power/Low Power Mixed VCC_SUSPEND/VCC_CORE Architecture



9.7 PCI

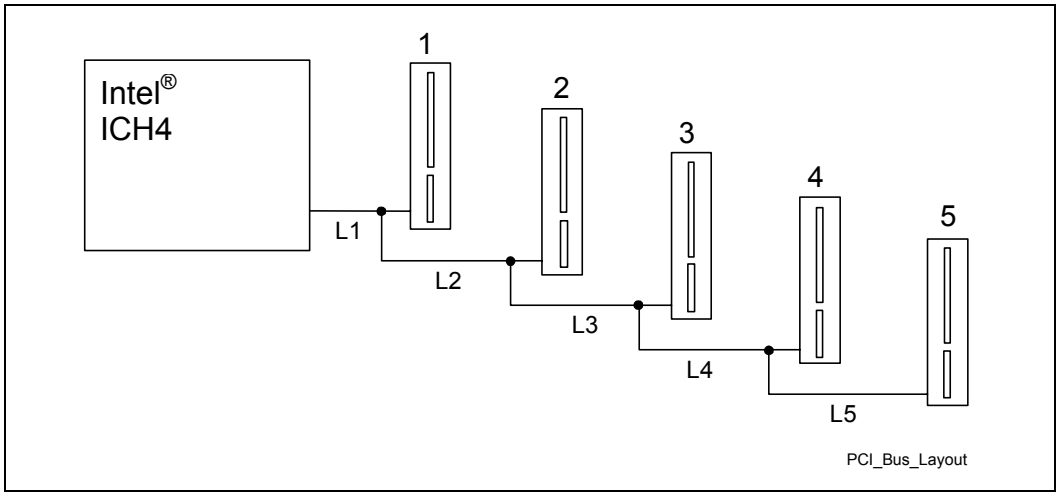
The ICH4 provides a PCI Bus interface that is compliant with the PCI Local Bus Specification, Revision 2.2. The implementation is optimized for high-performance data streaming when the ICH4 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification Revision 2.2*.

The ICH4 supports six PCI Bus masters (excluding the ICH4), by providing six REQ#/GNT# pairs. In addition, the ICH4 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

9.7.1 PCI Routing Summary

The following represents a summary of the routing guidelines for the PCI Slots. Simulations assume that PCI cards follow the *PCI Local Bus Specification, Revision 2.2* trace length guidelines.

Figure 9-25. PCI Bus Layout Example



Note: Note that if a CNR connector is placed on the platform, it will share a slot space with one of the PCI slots; however, it will not take away from the slot functionality unless the CNR slot is occupied by a CNR card.

Figure 9-26. PCI Bus Layout Example with IDSEL

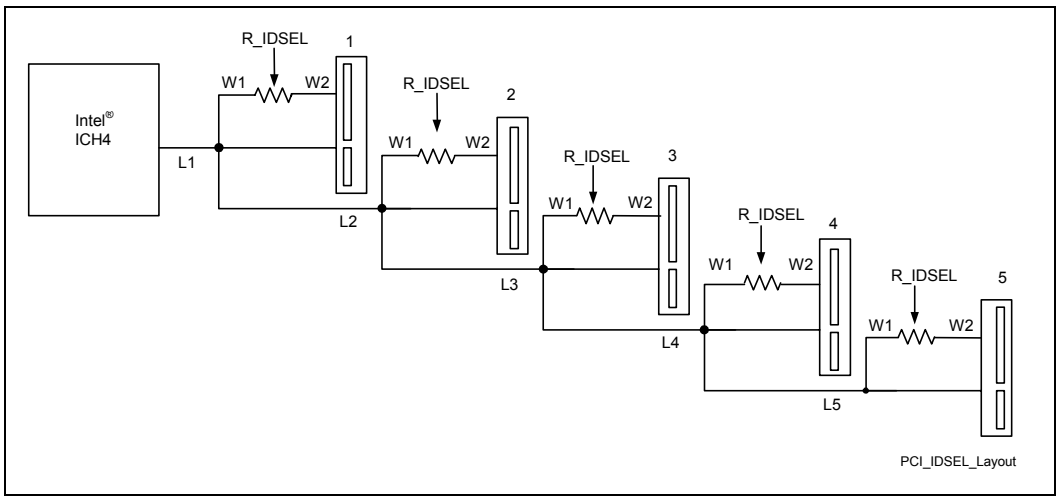
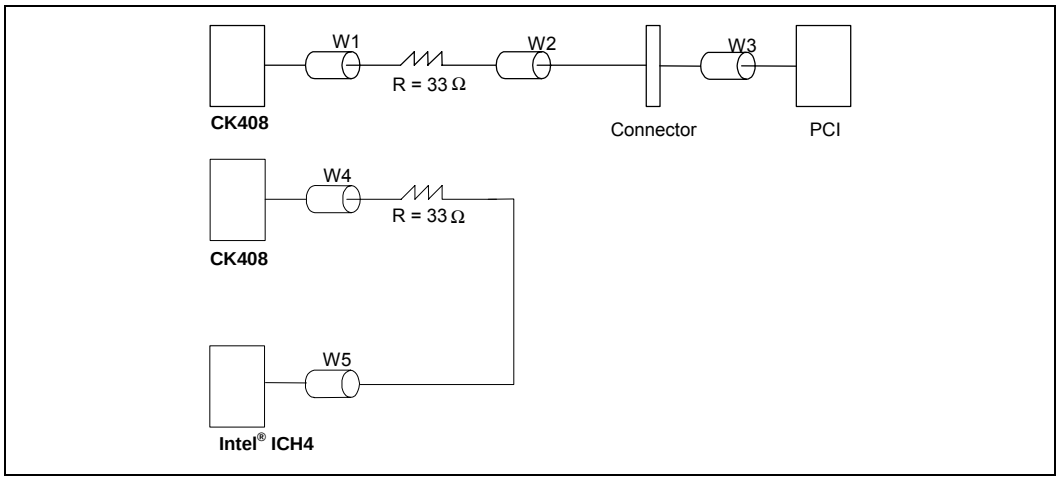


Table 9-13. PCI Data Signals Routing Summary

PCI Routing Req.	Trace Impedance	Topology	Maximum Trace Length (Inches)					
			L1	L2	L3	L4	L5	L6
5 of 7	47Ω to 69 Ω 60 Ω target	2 Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1.5	N/A	N/A	N/A	N/A
		2 Slots with 1 down device W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1.0	3.0	N/A	N/A	N/A
		3 Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1.5	1.5	N/A	N/A	N/A
		3 Slots with 1 down device W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1.0	1.0	3.0	N/A	N/A
		4 Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1.0	1.0	1.0	N/A	N/A
		4 Slots with 1 down device W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1.0	1.0	1.0	3.0	N/A
	51Ω to 69 Ω 60 Ω target	5 Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 8	1.0	1.0	1.0	1.0	N/A
		6 Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 7	1.0	1.0	1.0	1.0	1.0

Figure 9-27. PCI Clock Layout Example



NOTE: Clocks should be routed first.

Table 9-14. PCI Clock Signals Routing Summary

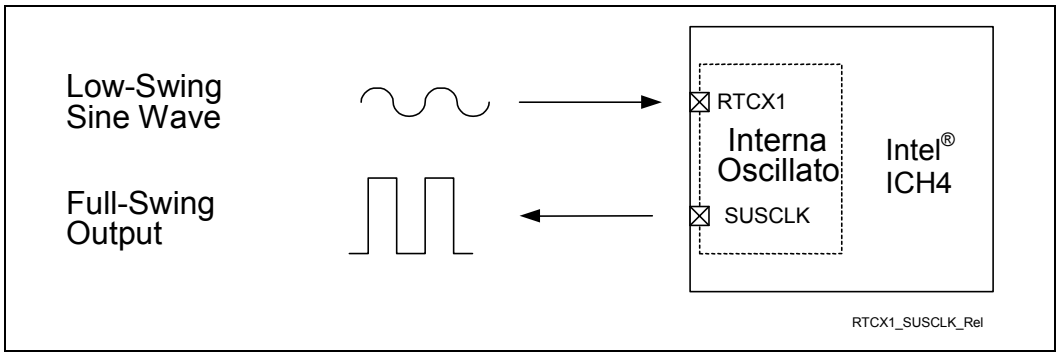
Trace Impedance	PCI Routing Requirements	Topology	Maximum Trace Length				
			W1	W2	W3	W4	W5
51 Ω to 69 Ω, 60 Ω Target	5 on 7	2 – 5 Slots	0.5”	W5 – 4.5”	2.5 inches (Shown as a reference only)	0.5”	Can be as long as needed (as long as W2 is scaled accordingly

9.8 RTC

The ICH4 contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH4 uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH4, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use. This output ball of the ICH4 is called SUSCLK. This is shown in Figure 9-28.

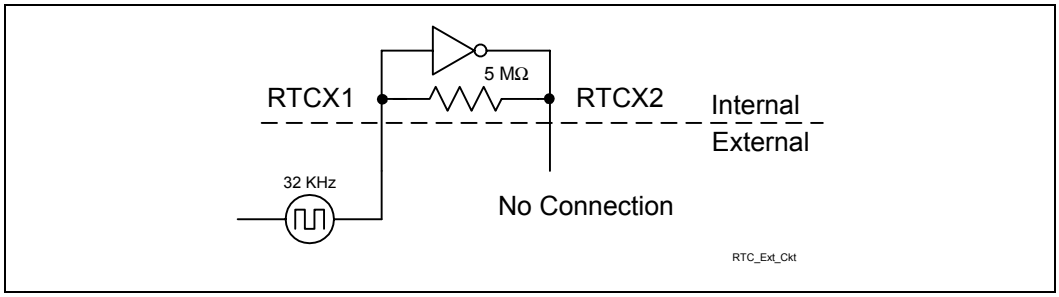
Figure 9-28. RTCX1 and SUSCLK Relationship in the Intel® ICH4



For further information on the RTC, consult Application Note AP-728 *"ICH/ICH2/ICH2M/ICH3S/ICH3M Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions"*. This application note is valid for ICH4.

Even if the ICH4 internal RTC is not used, it's still necessary to supply a clock input to RTCX1 of the ICH4 because other signals are gated off that clock in suspend modes. However, in this case, the frequency accuracy (32.768 kHz) of the clock inputs is not critical. A crystal can be used or a single clock input can be driven into RTCX1with RTCX2 left as no connect. Figure 9-29 illustrates the connection. This is not a validated feature on ICH4. Note that the peak-to-peak swing on RTCX1 cannot exceed 1.0 V.

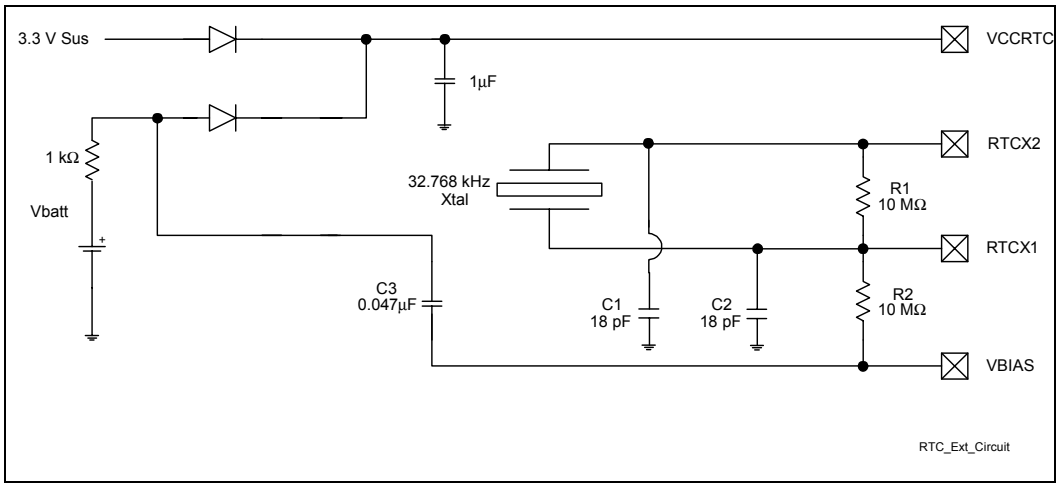
Figure 9-29. External Circuitry for the Intel® ICH4 Where the Internal RTC Is Not Used



9.8.1 RTC Crystal

The ICH4 RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 9-30 shows the external circuitry that comprises the oscillator of the ICH4 RTC.

Figure 9-30. External Circuitry for the Intel® ICH4 RTC



NOTES:

1. The exact capacitor value must be based on what the crystal maker recommends. (Typical values for C1 and C2 are 18 pF – based on crystal load 12.5 pF).
2. Reference designators are arbitrarily assigned.
3. 3.3 V Sus is active whenever the system is plugged in.
4. Vbatt is voltage provided by the battery.
5. VCCRTC, RTCX2, RTCX1, and VBIAS are ICH4 pins.
6. VCCRTC: Power for RTC Well.
7. RTCX2: Crystal Input 2 – Connected to the 32.768 kHz crystal.
8. RTCX1: Crystal Input 1 – Connected to the 32.768 kHz crystal.
9. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.
10. VSS: Ground.

Table 9-15. RTC Routing Summary

Trace Impedance	RTC Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R1, R2, C1, and C2 Tolerances	Signal Referencing
45 Ω to 69 Ω, 60 Ω Target	5 mil trace width (results in ~2pF per inch)	1 inch	NA	R1 = R2 = 10 MΩ ± 5% C1 = C2 = (NPO class) See Section 9.8.2 for calculating a specific capacitance value for C1 and C2	Ground

9.8.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C_3 must be 0.047 µF and capacitor values C_1 and C_2 should be chosen to provide the manufacturer's specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})*(C_2 + C_{in2} + C_{trace2})]/[(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

- C_{load} = Crystal's load capacitance. This value can be obtained from Crystal's specification.
- C_{in1}, C_{in2} = input capacitances at RTCX1, RTCX2 balls of the ICH4. These values can be obtained in the ICH4 data sheet.
- C_{trace1}, C_{trace2} = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. Typical value, based on a 5 mil wide trace and a ½ ounce copper pour, is approximately equal to:

  $$C_{trace} = \text{trace length} * 2\text{pF/inch}$$

- $C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the existence of 2 electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C_1, C_2 can be chosen such that $C_1 = C_2$. Using the equation of C_{load} above, the value of C_1, C_2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C_2 can be chosen such that $C_2 > C_1$. Then C_1 can be trimmed to obtain the 32.768 kHz.

In certain conditions, both C_1, C_2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C_1, C_2 values are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example will illustrates the use of the practical values C_1, C_2 in the case that theoretical values can not guarantee the accuracy of the RTC in low temperature condition:

Example

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH4, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25 °C) to yield a 32.768 kHz oscillation.

At 0 °C the frequency stability of crystal gives –23 ppm (assumed that the circuit has 0 ppm at 25 °C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C_1, C_2 are chosen to be 6.8 pF instead of 10 pF, this will make the RTC oscillate at higher frequency at room temperature (+23 ppm) but this configuration of C_1 / C_2 makes the circuit oscillate closer to 32.768 kHz at 0 °C. The 6.8 pF value of C1 and 2 is the **practical value**.

Note that the temperature dependency of crystal frequency is parabolic relationship (ppm / degree square). The effect of changing crystal's frequency when operating at 0 °C (25 °C below room temperature) is the same when operating at 50 °C (25 °C above room temperature).

9.8.3 RTC Layout Considerations

Because the RTC circuit is very sensitive and requires high accurate oscillation, reasonable care must be taken during layout and routing RTC circuit. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. ICH4 requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of board's material. On FR-4, a 5-mil trace has approximately 2 pF per inch.
- Trace signal coupling must be importantly reduced, by avoiding routing of adjacent PCI signals close to RTCX1 & RTCX1, VBIAS.
- Ground guard plane is highly recommended.
- The oscillator VCC should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

9.8.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH4 is not powered by the system.

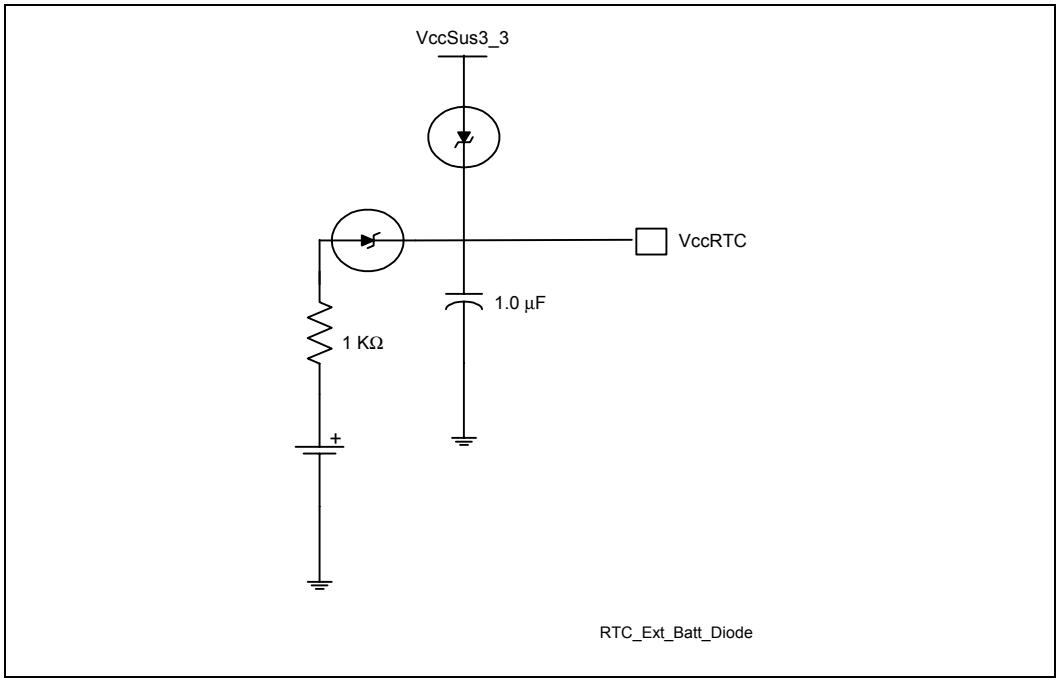
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 5 uA, the battery life will be at least:

170,000 uAh / 5 uA = 34,000 h = 3.9 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH4 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH4 RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 9-31 is an example of a diode circuit that is used.

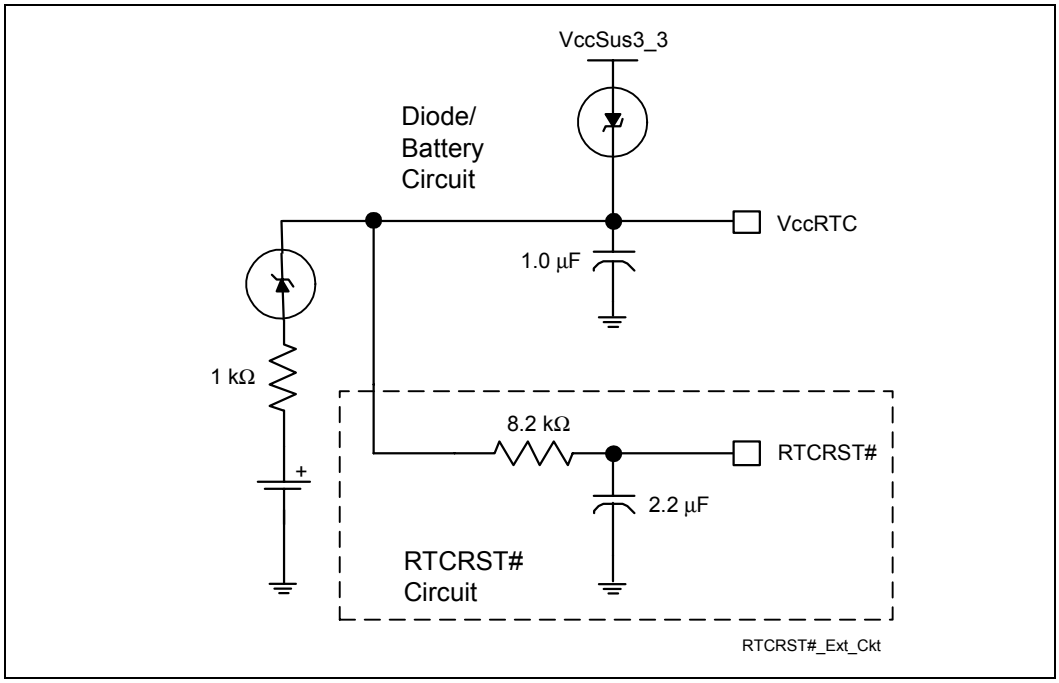
Figure 9-31. A Diode Circuit to Connect the RTC External Battery



A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

9.8.5 RTC External RTCRST# Circuit

Figure 9-32. RTCRST# External Circuit for the Intel® ICH4 RTC



The ICH4 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18 ms – 25 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 9-31) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 9-32 is an example of this circuitry that is used in conjunction with the external diode circuit.

9.8.6 VBIAS DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC Network of R2 and C3 (see Figure 9-30) therefore it is self-adjusted voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

- VBIAS should be at least 200 mV DC. The RC network of R2 and C3 will filter out most of AC signal that exist on this ball, however, the noise on this ball should be kept minimal to guarantee the stability of the RTC oscillation.
- Probing VBIAS requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). See Application Note AP-728 for further details on measuring techniques.
- Note that VBIAS is also very sensitive to environmental conditions.

9.8.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30 – 70%. If the SUSCLK duty cycle is beyond 30 – 70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50 Ω input impedance probe) and it is an appropriated signal to check the RTC frequency to determine the accuracy of the ICH4's RTC Clock (see Application Note AP-728 for further details).

9.8.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST#, when configured as shown in Figure 9-32, meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VCCRTC. This prevents these nodes from floating in G3, and correspondingly prevents ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

9.9 Internal LAN Layout Guidelines

The ICH4 provides several options for integrated LAN capability. The platform supports several components depending on the target market. Available LAN components include the 82540EM Gigabit Ethernet controller (GbE), 82551QM Fast Ethernet controller, 82562EZ/82562ET and 82562EX/82562EM platform LAN connect (PLC) components.

Table 9-16. LAN Component Connections/Features

LAN Component	Interface To ICH4	Connection	Features
82540EM (196 BGA)	PCI	Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting	Gigabit Ethernet, ASF 1.0 alerting, PCI 2.2 compatible
82551QM (196 BGA)	PCI	Performance 10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible
82562EM (48 Pin SSOP) 82562EX (196 BGA)	LCI	10/100 Ethernet with Alert on LAN (AoL) alerting	Ethernet 10/100 connection, Alert on LAN (AoL)
82562ET (48 Pin SSOP) 82562EZ (196 BGA)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

Which LAN component to use on the ICH4 platform will depend on the end user's need for connection speed, manageability needs, and bus connection type. In addition, footprint compatible packages make it possible to design a platform that can use any of the LAN components without the need for a motherboard redesign.

9.9.1 Footprint Compatibility

The 82540EM GbE controller, 82551QM Fast Ethernet controller, and the 82562EX/82562EZ platform LAN connect devices are all manufactured in a footprint compatible 15 mm x 15 mm (1 mm pitch), 196-ball grid array package. Many of the critical signal pin locations on the 82540EM, 82551QM, and 82562EX/82562EZ are identical, allowing designers to create a single design that accommodates any one of these parts. Because the usage of some pins on the 82540EM differ from the usage on the 82551QM or the 82562EX/82562EZ, the parts are not referred to as "pin compatible". The term "footprint compatible" refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design. Therefore, it is easy to populate a single board design with either part to maximize value while matching your customers' performance needs.

Design guidelines are provided for each required interface and connection. Refer to the following figures and table for the corresponding section of the design guide. The guidelines use the 82546EZ to refer to both the 82562EZ and 82562EX. The 82562EX is specified in those cases where there is a difference.

Figure 9-33. Intel® ICH4/Platform LAN Connect Section

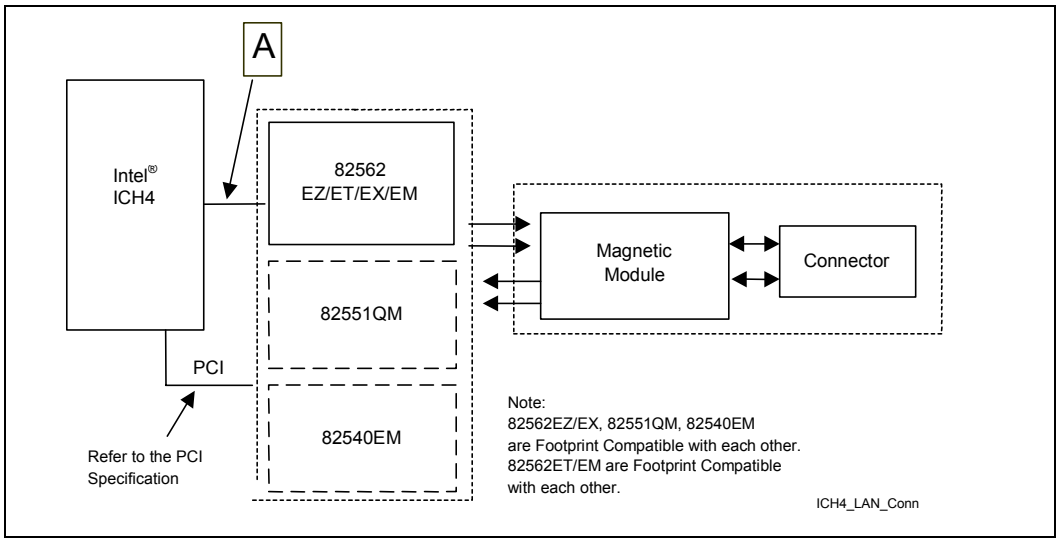


Table 9-17. LAN Design Guide Section Reference

Layout Section	Figure 9-33 Reference	Design Guide Section
ICH4 – LAN Connect Interface (LCI)	A	9.9.2, Intel® ICH4 — LAN Connect Interface Guidelines
82562EZ/EX 82562ET / 82562EM	A	9.9.3, Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM and Intel® 82551QM
82551QM	PCI	9.9.3, Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM and Intel® 82551QM
82540EM	PCI	9.10.2, Design and Layout Considerations for Intel® 82540EM

9.9.2 Intel® ICH4 — LAN Connect Interface Guidelines

This section contains guidelines on how to implement a Platform LAN connect device on a system motherboard or on a CNR riser card. It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH4 to LAN connect interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports 82562EZ/ET and 82562EX/EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD0, and LAN_TXD0 are shared by all components. The AC characteristics for this interface are found in the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*.

9.9.2.1 Bus Topologies

The platform LAN connect interface can be configured in several topologies:

- Direct point-to-point connection between the ICH4 and the LAN component
- LOM/CNR Implementation

9.9.2.1.1 LOM (LAN on Motherboard) or CNR Point-to-Point Interconnect

The following are guidelines for a single solution motherboard. Either 82562EZ/ET, 82562EX/EM, or CNR are uniquely installed.

Figure 9-34. Single Solution Interconnect

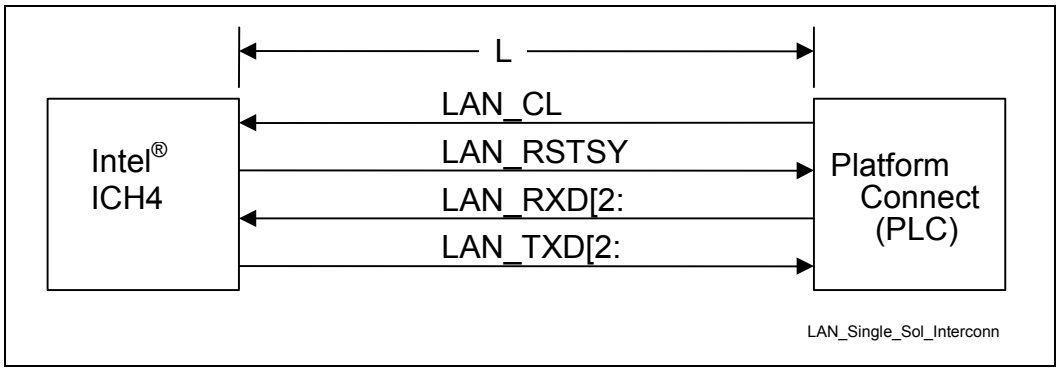


Table 9-18. LAN LOM or CNR Routing Summary

Trace Impedance	LAN Routing Requirements	Maximum Trace Length		Signal Referencing	LAN Signal Length Matching
51 Ω to 69 Ω, 60 Ω Target	5 on 10	82562EZ/ET /EX/EM	4.5” to 12”	Ground	Data signals must be equal to no more than 0.5 inch (500 mils) shorter than the LAN clock trace.
		82562EZ/ET /EX/EM on CNR	2” to 9.5”		

9.9.2.1.2 LOM (LAN on Motherboard) and CNR Interconnect

The following guidelines apply to an all-inclusive configuration of PLC design. This layout combines LAN on motherboard and the CNR solutions. The resistor pack ensures that either a CNR option or a LAN on motherboard option can be implemented at one time.

Figure 9-35. LOM/CNR Interconnect

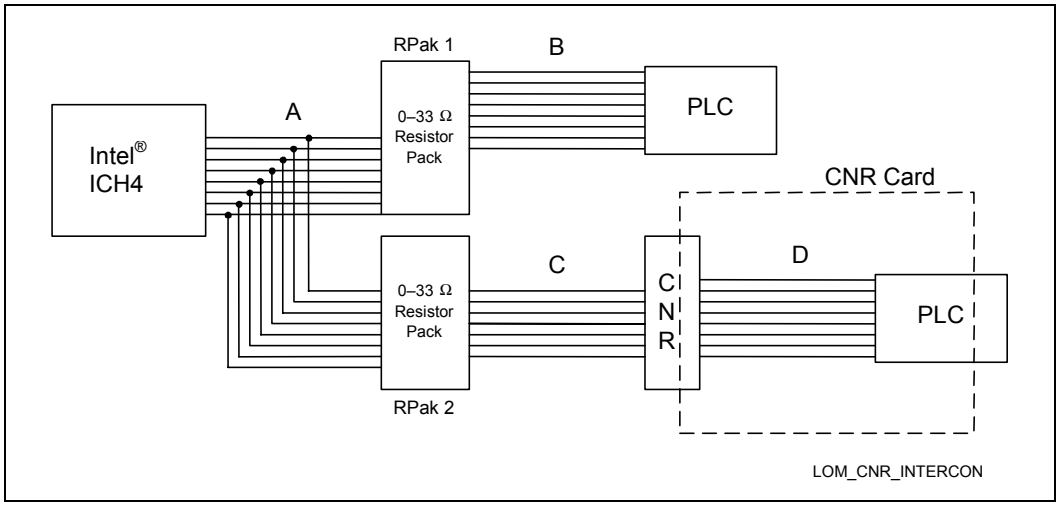


Table 9-19. LOM/CNR Dual Routing Summary

Trace Impedance	LAN Routing Req.	Maximum Trace Length	Sig. Ref.	LAN Signal Length Matching
51 Ω to 69 Ω, 60 Ω Target	5 on 10	**82562EZ /ET/EX/EM** **A** 0.5” to 7.5”; **B** 4” to (11.5 – A) “; **C** NA; **D** NA **82562EZ /ET/EX/EM on CNR[1]** **A** 0.5” to 7.5”; **B** NA; **C** 1.5” to (9.0 – A) “; **D** 0.5” to 3”	Gnd.	Data signals must be equal to or no more than 0.5 inch (500 mils) shorter than the LAN clock trace.

NOTES:
1. Total motherboard trace length should not exceed 9.0”

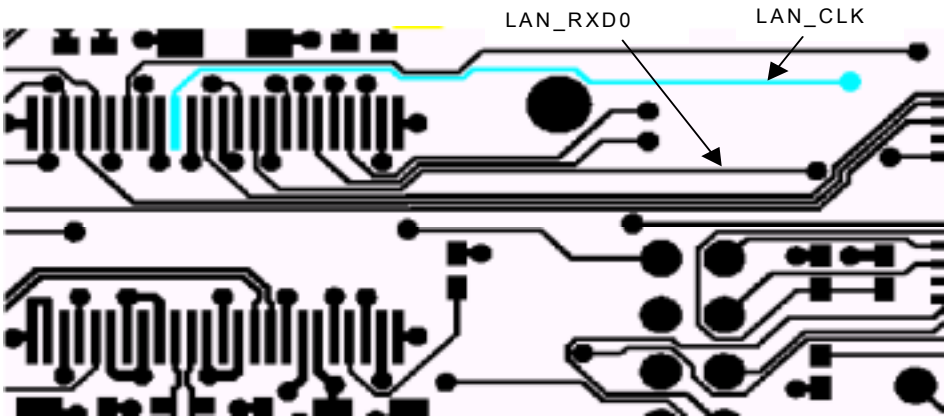
Additional guidelines for this configuration are as follows:

- Stubs due to the resistor pack should not be present on the interface.
- The resistor pack value can be 0 Ω to 33 Ω (See Section 9.9.2.5).

9.9.2.2 Signal Routing and Layout

Platform LAN connect Interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inch shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 9-36. LAN_CLK Routing Example



9.9.2.3 Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the tRMATCH skew parameter. TRMATCH is the sum of the trace length mismatch between LAN_CLK and LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inch shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-PLC signals.

9.9.2.4 Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 Ω ±15% is strongly recommended; otherwise, signal integrity requirements may be violated.

9.9.2.5 Line Termination

Line termination mechanisms are not specified for the LAN connect interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 0 to 33 Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

9.9.2.6 Terminating Unused LAN Connect Interface Signals

The LAN connect interface on the ICH4 can be left as a no-connect if it is not used.

9.9.3 Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM and Intel® 82551QM

For correct LAN performance, designers must follow the general guidelines outlined in Section 9.9.2 (General LAN Routing Guidelines and Considerations). Additional guidelines for implementing an 82562EZ/ET/EX/EM or 82551QM platform LAN connect component are provided below.

9.9.3.1 Guidelines for Intel® 82562EZ/ET/EX/EM / Intel® 82551QM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.9.3.2 Crystals and Oscillators

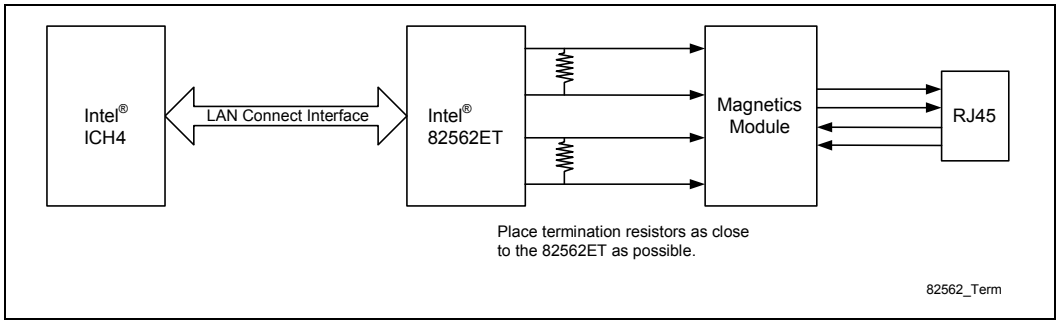
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562EZ/ET/EX/EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

9.9.3.3 Intel® 82562EZ/ET/EX/EM / Intel® 82551QM Termination Resistors

The 100 Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 121 Ω (±1%) receive differential pairs (RDP/RDN) should be placed as close to the platform LAN connect component (82562EZ/ET/EX/EM and 82551QM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

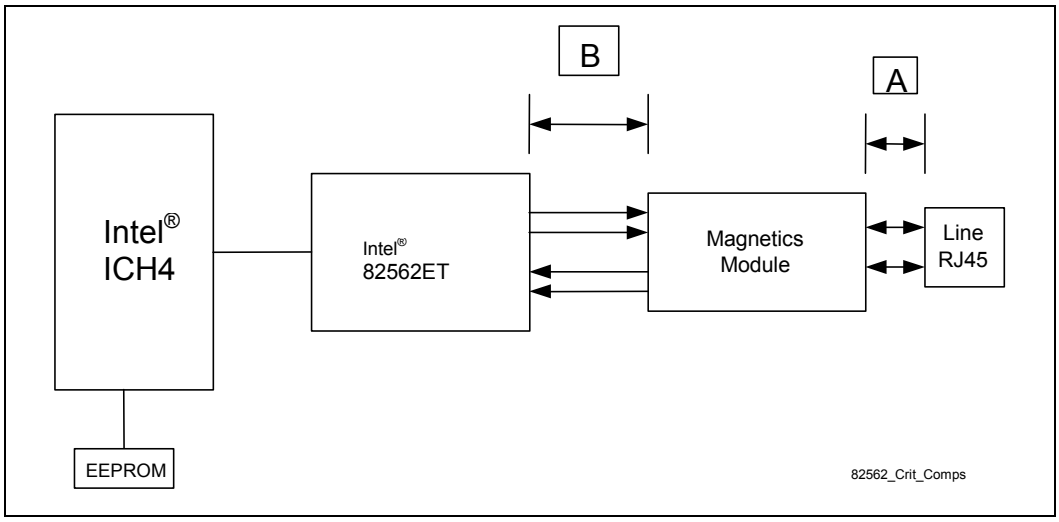
Figure 9-37.Intel® 82562ET/82562EM Termination



9.9.3.4 Critical Dimensions

There are two dimensions to consider during layout. Distance ‘A’ from the line RJ45 connector to the magnetics module and distance ‘B’ from the 82562EZ/ET/EX/EM or 82551QM to the magnetics module. The combined total distances of A and B must not exceed 4 inches (preferably, less than 2 inches — see Figure 9-38).

Figure 9-38. Critical Dimensions for Component Placement



Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

9.9.3.4.1 Distance from Magnetics Module to RJ45 (Distance A)

The distance A in the preceding figure should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- **Differential Impedance:** The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 60 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- **Trace Symmetry:** Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit’s performance and contribute to radiated emissions from the transmit circuit. If the 82562EZ/ET/EX/EM or 82551QM must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562EZ/ET/EX/EM or 82551QM and RJ45 as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105–110 Ω should compensate for second order effects.

9.9.3.4.2 Distance from Intel® 82562EZ/ET/EX/EM / Intel® 82551QM to Magnetics Module (Distance B)

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and equal length within each differential pair.

9.9.3.5 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Signals with fast rise and fall times contain many high-frequency harmonics, which can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

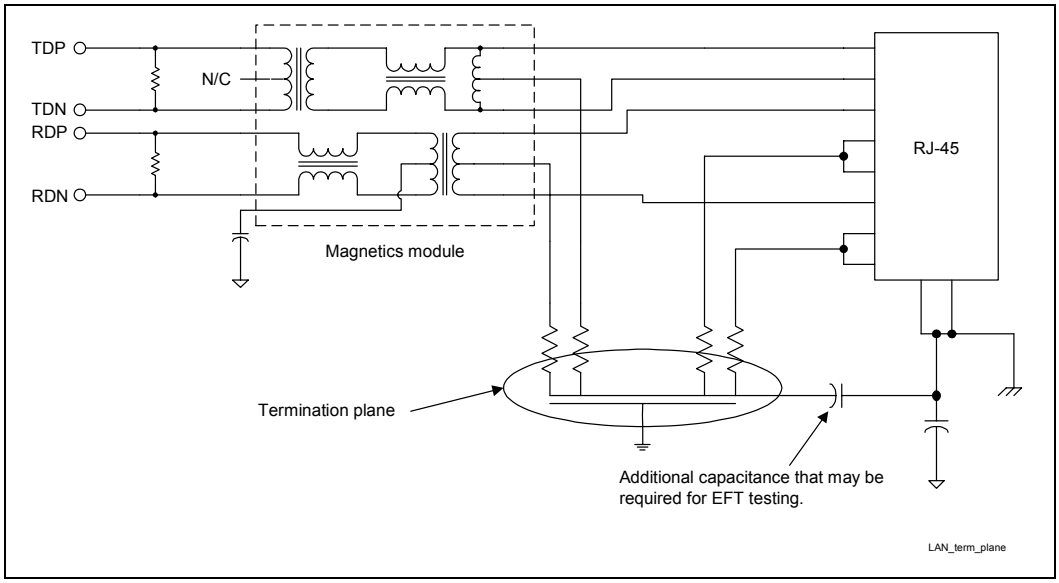
Terminating Unused Connections

In Ethernet designs it is common practice to terminate unused connections on the RJ45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

9.9.3.5.1 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

Figure 9-39. Termination Plane

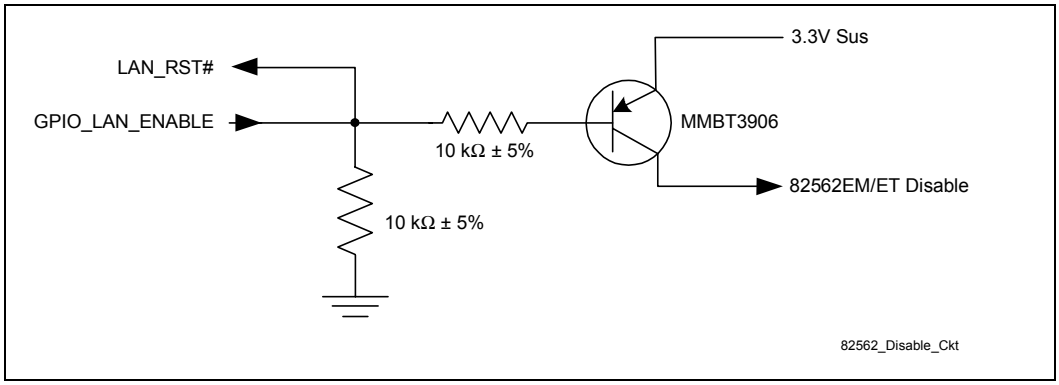


9.10 Intel® 82562EZ/ET/EX/EM Disable Guidelines

9.10.1 Intel® 82562EZ/ET/EX/EM Disable Guidelines

To disable the 82562EZ/ET/EX/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. The BIOS controlling the GPIO can disable the LAN microcontroller.

Figure 9-40. Intel® 82562EZ/ET/EX/EM Disable Circuitry



There are 4 pins that are used to put the 82562EZ/ET/EX/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 9-20 describes the operational/disable features for this design.

The four control signals shown in Table 9-20 should be configured as follows: Test_En should be pulled-down thru a 100 Ω resistor. The remaining 3 control signals should each be connected thru 100 Ω series resistors to the common node “82562EZ/ET/EX/EM _Disable” of the disable circuit.

Table 9-20. Intel® 82562EZ/ET/EX/EM Control Signals

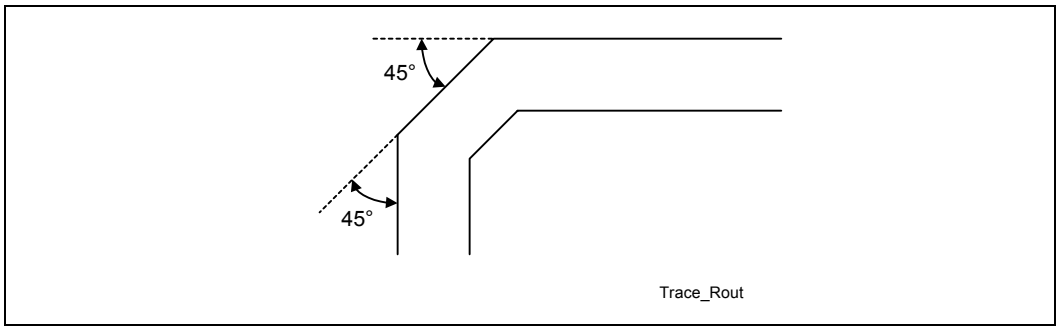
Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

9.10.1.1 General Intel® 82562ET/82562EM Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance: (Note: Some suggestions are specific to a 4.3 mil stack-up.)

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).]
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces. (300 mils recommended)
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, it is recommended to use two 45-degree bends instead. Refer to Figure 9-41.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 9-41. Trace Routing



9.10.1.1.1 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by 10 Ω, when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

9.10.1.1.2 Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.

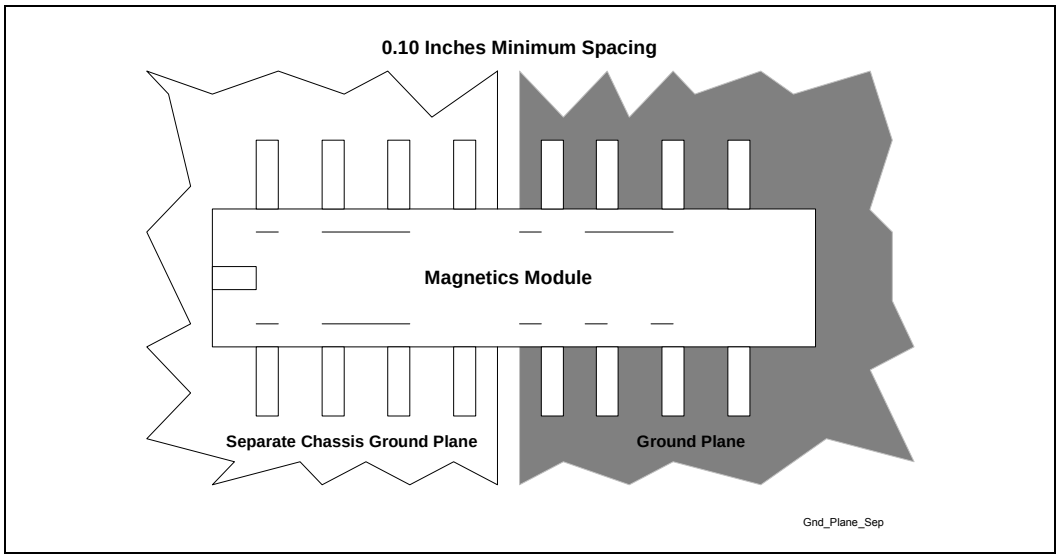
  Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.

- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

9.10.1.1.3 Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 9-42. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both back planes and motherboards.

- Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high-frequency harmonics that can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

9.10.1.2 Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

- Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
- Lack of symmetry between the two traces within a differential pair. [Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.] Asymmetry can create common-mode noise and distort the waveforms.
- Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer. The magnetics should be as close to the connector as possible (less than or equal to one inch).
- Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
- Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45, and the PLC.
- Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
- Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or application note.
- Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or term plane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The AP-Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
- Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they've designed for 100 Ω. [To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive

coupling between the two traces. When the two traces within a differential pair are kept close† to each other the edge coupling can lower the effective differential impedance by 5 to 20 Ω. A 10 to 15 Ω drop in impedance is common.] Short traces will have fewer problems if the differential impedance is a little off.

- Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetics transmit center-tap (on the 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. [6 pF to 12 pF values have been used on past designs with reasonably good success.] These caps are not necessary, unless there is some overshoot in 100 Mbps mode.

Note: It is important to keep the two traces within a differential pair close† to each other. Keeping them close† helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces.

Note: † Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

9.10.2 Design and Layout Considerations for Intel® 82540EM

For specific design and layout considerations for the 82540EM refer to the *82540EM Gigabit Ethernet Controller Preliminary Datasheet and Hardware Design Guide.*

9.11 Intel® ICH4 – SYS_RESET#/PWRBTN# Usage Models and Power-Well Isolation Control Strap Requirements

This section describes the SYS_RESET# and PWRBTN# Usage Models and Power-Well Isolation Control Strap Requirements.

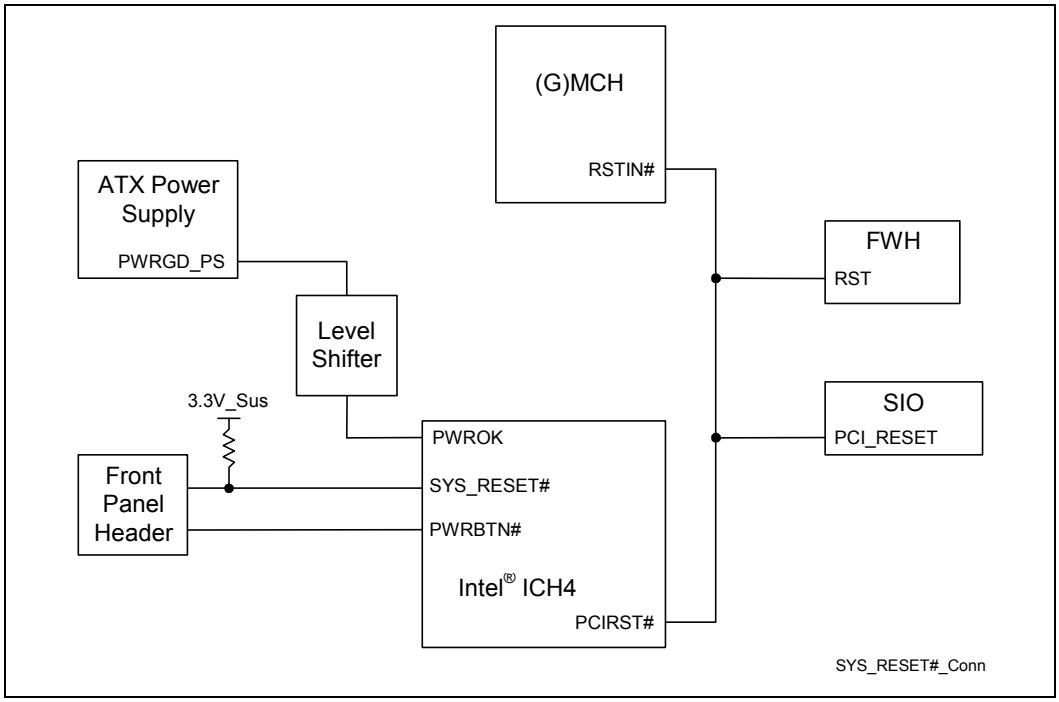
9.11.1 SYS_RESET# Usage Model

The System Reset ball (SYS_RESET#) on the ICH4 can be connected directly to the reset button on the systems front panel provided that the front panel header pulls this signal up to 3.3 V standby through a weak pull-up resistor. The ICH4 will debounce signals on this pin (16ms) and allow the SMBus to go idle before resetting the system; thus helping prevent a slave device on the SMBus from "hanging" by resetting in the middle of a cycle.

9.11.2 PWRBTN# Usage Model

The Power Button ball (PWRBTN#) on the ICH4 can be connected directly to the power button on the systems front panel. This signal is internally pulled-up in the ICH4 to 3.3 V standby through a weak pull-up resistor (24 kΩ nominal). The ICH4 has 16ms of internal debounce logic on this pin.

Figure 9-43. SYS_RESET# and PWRBTN# Connection

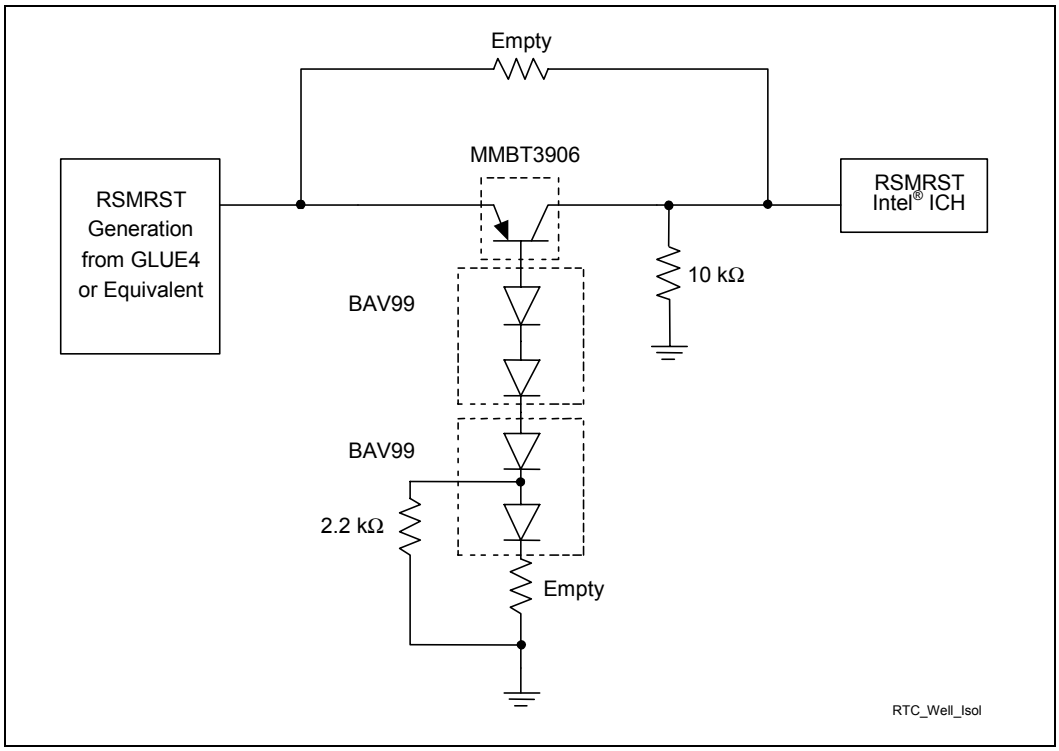


9.11.3 Power-Well Isolation Control Requirement

The RSMRST# signal of the ICH4 must transition from 20 % signal level to 80 % signal level and vice-versa in 50 µs. Slower transitions may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power). Droop on this node can potentially cause the CMOS to be cleared or corrupted, the RTC to loose time after several AC power cycles, or the intruder bit might assert erroneously.

The circuit shown in Figure 9-44 can be implemented to control well isolation between the VccSus3_3 and RTC power-wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail or does not meet the above rise/fall time.

Figure 9-44. RTC Power Well Isolation Control



9.12 General Purpose I/O

9.12.1 GPIO Summary

The ICH4 has 12 general purpose inputs, 8 general purpose outputs, and 16 general purpose inputs/outputs.

Table 9-21. GPIO Summary

GPIO Number	Power Well	Input, Output, I/O	Tolerance	Note
0	Core	Input	5 V	2
1	Core	Input	5 V	2
2	Core	Input	5 V	2
3	Core	Input	5 V	2
4	Core	Input	5 V	2
5	Core	Input	5 V	2
6	Core	Input	5 V	
7	Core	Input	5 V	
8	Resume	Input	3.3 V	
11	Resume	Input	3.3 V	2
12	Resume	Input	3.3 V	
13	Resume	Input	3.3 V	
16	Core	Output	3.3 V	2
17	Core	Output	3.3 V	2
18	Core	Output	3.3 V	
19	Core	Output	3.3 V	
20	Core	Output	3.3 V	
21	Core	Output	3.3 V	
22	Core	Output (Open Drain)	3.3 V	
23	Core	Output	3.3 V	
24	Resume	I/O	3.3 V	1
25	Resume	I/O	3.3 V	1
27	Resume	I/O	3.3 V	1
28	Resume	I/O	3.3 V	1
32	Core	I/O	3.3 V	1
33	Core	I/O	3.3 V	1
34	Core	I/O	3.3 V	1
35	Core	I/O	3.3 V	1
36	Core	I/O	3.3 V	1
37	Core	I/O	3.3 V	1
38	Core	I/O	3.3 V	1
39	Core	I/O	3.3 V	1
40	Core	I/O	3.3 V	1
41	Core	I/O	3.3 V	1
42	Core	I/O	3.3 V	1
43	Core	I/O	3.3 V	1

NOTES:
1. Defaults as an output.
2. Can be used as a GPIO if the native function is not needed. ICH4 defaults these signals to native functionality.

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10 FWH Guidelines

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the FWH BIOS Specification or equivalent.

10.1 FWH Vendors

The following vendors manufacture firmware hubs, which conform to the *Intel® FWH Specification*. Contact the vendor directly for information on packaging and density.

SST:	http://www.ssti.com/
STM:	http://us.st.com/stonline/index.shtml
ATMEL:	http://www.atmel.com/

10.2 FWH Decoupling

A 0.1 µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple high-frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple low-frequency noise. The capacitors should be placed no further than 390 mils from the VCC supply pins.

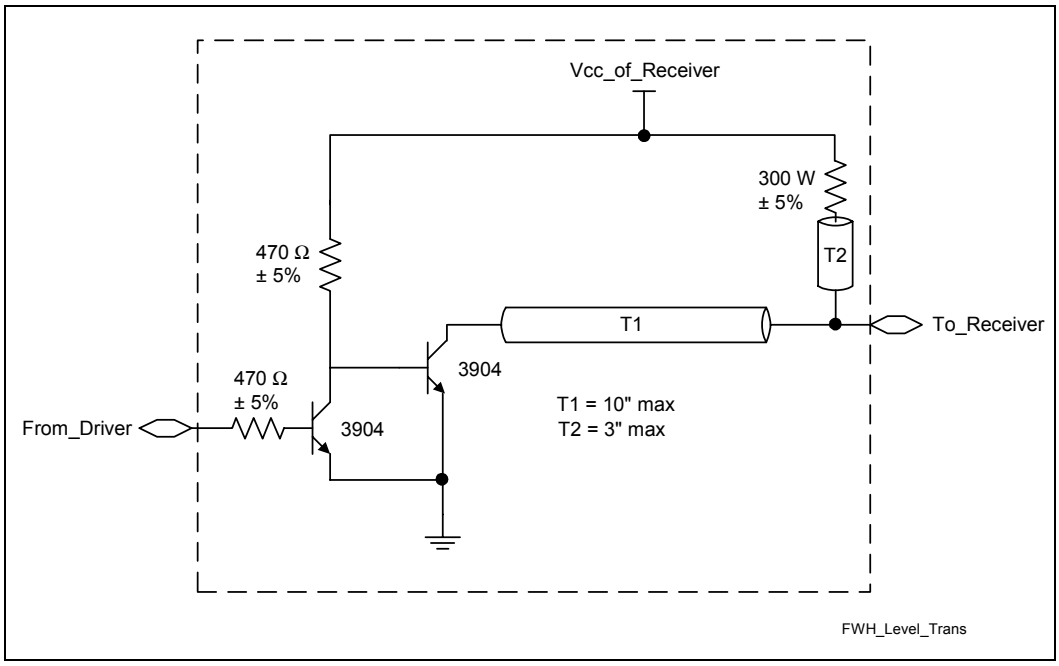
10.3 In Circuit FWH Programming

All cycles destined for the FWH will appear on PCI. The ICH4 Hub Interface to PCI Bridge will put all processor boot cycles out on PCI (before sending them out on the FWH interface). If the ICH4 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. To boot off a PCI card it is necessary to keep the ICH4 in subtractive decode mode. If a PCI boot card is inserted and the ICH4 is programmed for positive decode, there will be two devices positively decoding the same cycle.

10.4 FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points need to be considered because they are **not** consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the ICH4 INIT# signal must be at a value slightly higher than the VIH min FWH INIT# pin specification. The ICH4 inactive state of this signal is typically governed by the formula V_CPU_IOmin - noise margin. Therefore, if the V_CPU_IOmin of the processor is 1.6 V, the noise margin is 200 mV and the VIH min specification of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because 1.6 V – 0.2 V = 1.40 V which is greater than the 1.35 V minimum of the FWH. If the VIH min of the FWH was 1.45 V, then there would be an incompatibility and logic translation would need to be used. Note that these examples do not take into account actual noise that may be encountered on INIT#. Care must be taken to ensure that the VIH min specification is met with ample noise margin. In applications where it is necessary to use translation logic, refer to the circuit in Figure 10-1.

Figure 10-1 FWH Level Translation Circuitry



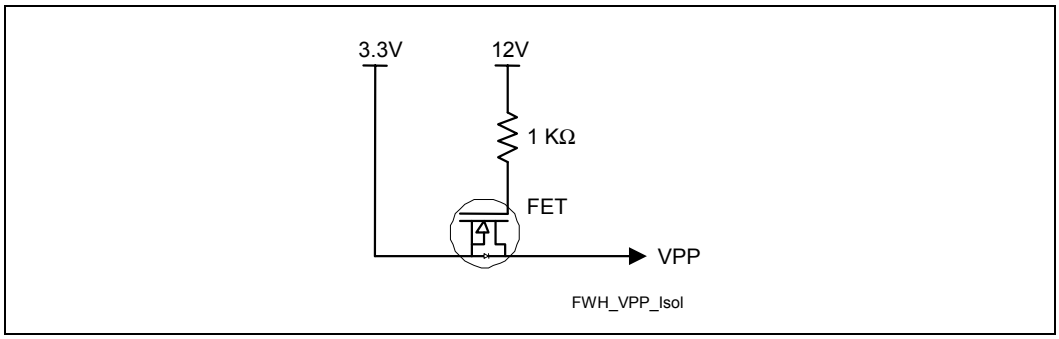
Note: This translation circuit is optimized to function with low voltage processors that the ICH4 supports.

10.5 FWH VPP Design Guidelines

The VPP pin on the FWH is used for programming the flash cells. The FWH supports VPP of 3.3 V or 12 V. If VPP is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12 V VPP for 80 hours (3.3 V on VPP does not affect the life of the device). The 12 V VPP would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The VPP pin MUST be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. To decrease programming time, it becomes necessary to apply 12 V to the VPP pin. The following circuit will allow testers to put 12 V on the VPP pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 10-2. FWH VPP Isolation Circuitry



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11 Miscellaneous Logic

The ICH4 requires additional external circuitry to function properly. Some of these functionalities include meeting timing specifications, buffering signals, and switching between power wells. This logic may be implemented through the use of the Glue Chip or discrete logic.

11.1 Glue Chip 4

To reduce the component count and BOM (Bill of Materials) cost of the ICH4 platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The ICH4 Glue Chip is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Features

- Dual, Strapping, Selectable Feature Sets
- Audio-disable circuit
- Mute Audio Circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK (PWRGD_3V) signal generation
- Power Sequencing / BACKFEED_CUT
- Power Supply turn on circuitry
- RSMRST# generation
- Voltage Translation for DDC to VGA monitor
- HSYNC / VSYNC voltage translation to VGA monitor
- Tri-state buffers for test
- Extra GP Logic Gates
- Power LED Drivers
- Flash FLUSH# / INIT# circuit

More information regarding this component is available from the following vendors:

Vendor	Contact Information	Part Number
Philips Semiconductors	http://www.semiconductors.philips.com	PCA9504A
Fujitsu Microelectronics	http://www.fujitsumicro.com/	MB87B302ABPD-G-ER

Note: These vendors and devices are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

11.2 Discrete Logic

As an alternative solution, discrete circuitry may be implemented into a design instead of using the Glue Chip.

12 Platform Clock Routing Guidelines

The following information details platform clock and routing layout guidelines for an 845GE/845PE chipset-based platform.

12.1 Clock Generation

Only one clock generator component is required in an 845GE/845PE chipset-based platform. Clock synthesizers that meet the *Intel® CK408 Clock Synthesizer/Driver Specification* are suitable for an 845GE/845PE chipset based platform. For more information on CK408 compliance, refer to the *Intel® CK408 Clock Synthesizer/Driver Specification* Document. The following tables and figure list and describe the 845GE/845PE chipset clock groups, the platform system clock cross-reference, and the platform clock distribution.

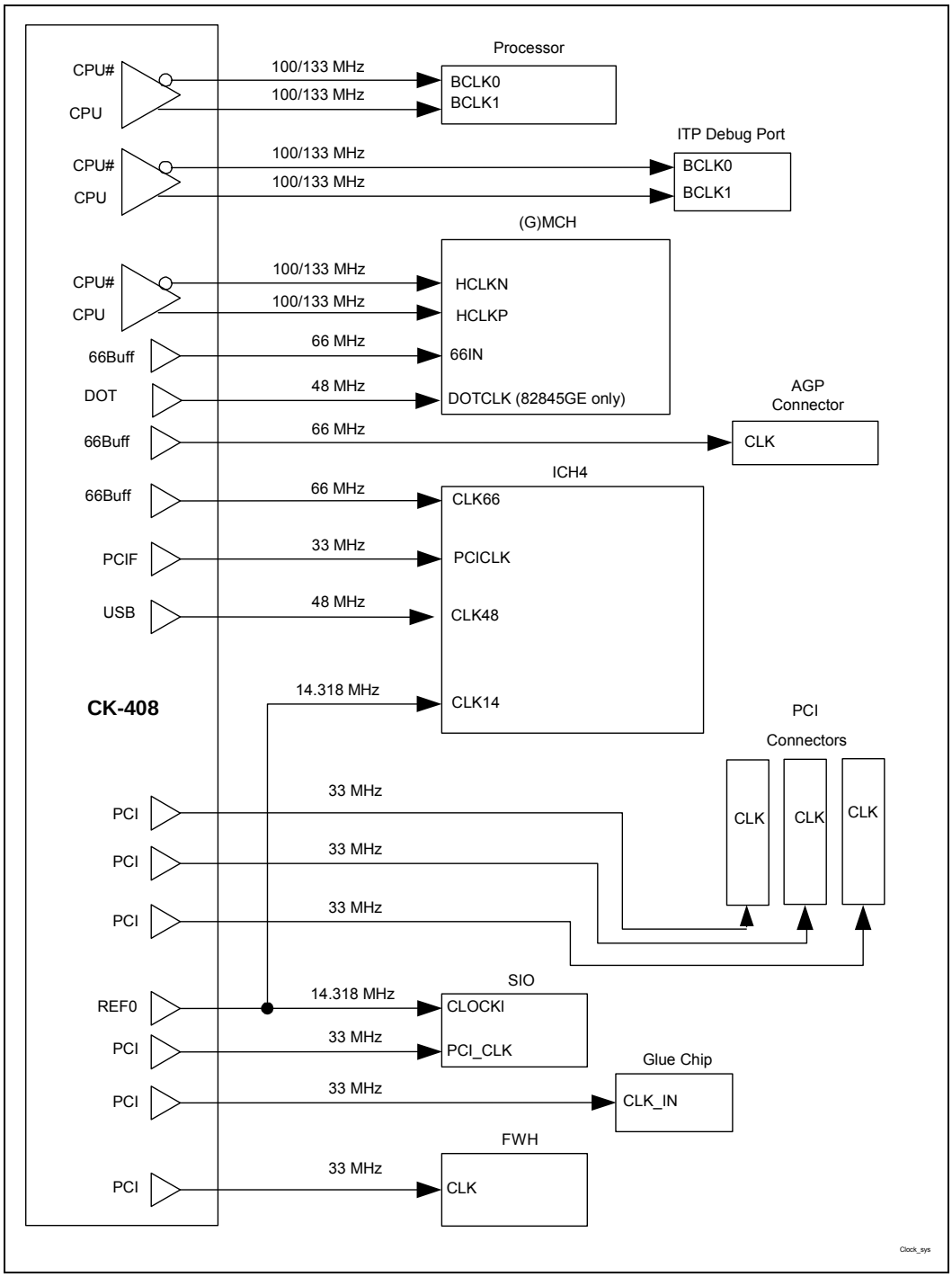
Table 12-1. Intel® 845GE/845PE Chipset Clock Groups

Clock Name	Frequency	Receiver
Host_CLK	100/133 MHz	Processor, ITP Debug Port, and (G)MCH
DOT_CLK	48 MHz	GMCH (845GE chipset only)
CLK66	66 MHz	(G)MCH and Intel® ICH4
AGPCLK	66 MHz	AGP Connector or AGP Device
CLK33	33 MHz	ICH4, SIO, Glue Chip, and FWH/Flash BIOS
CLK14	14.318 MHz	ICH4 and SIO
PCICLK	33 MHz	PCI Connector
USBCLK	48 MHz	ICH4

Table 12-2. Platform System Clock Cross-Reference

Clock Group	CK408 Pin	Component	Component Pin Name
HOST_CLK	CPU	CPU	BCLK0
	CPU#	CPU	BCLK1
	CPU	ITP Debug Port	BCK
	CPU#	ITP Debug Port	BCK#
	CPU#	(G)MCH	HCLKN
	CPU	(G)MCH	HCLKP
DOT_CLK	DOT_48 MHz	GMCH (845GE chipset only)	DREFCLK
CLK66	3V66	(G)MCH	GCLKIN
		Intel® ICH4	CLK66
AGPCLK	3V66	AGP Connector or AGP Device	AGPCLK
CLK33	PCIF	ICH4	PCICLK
	PCI	SIO	PCI_CLK
	3V66	Glue Chip	CLK_IN
	PCI	FWH/Flash BIOS	CLK
CLK14	REF0	ICH4	CLK14
		SIO	CLOCKI
PCICLK	PCI	PCI Connector 1	CLK
		PCI Connector 2	CLK
		PCI Connector 3	CLK
USBCLK	USB_48MHz	ICH4	CLK48

Figure 12-1. Platform Clocking Block Diagram



12.2 Clock Group Topology and Layout Routing Guidelines

12.2.1 HOST_CLK Clock Group

The clock synthesizer provides four sets of differential clock outputs. The differential clocks are driven to the processor, the 845GE/845PE chipset, and the processor debug port as shown in Figure 12-1.

The clock driver differential bus output structure is a "Current Mode Current Steering" output which develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt. The resulting amplitude is determined by multiplying IOUT by the value of Rt. The current IOUT is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of Rt to match impedances or to accommodate future load requirements.

The recommended termination for the differential bus clock is a "Shunt Source termination." Refer to Figure 12-2 for this termination scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be selected to match the characteristic impedance of the system board and Rs should be between 20 and 33 Ω. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

- Mult0 pin (pin 43) connected to HIGH – making the multiplication factor as 6.
- Iref pin (pin 42) is connected to ground through a 475 Ω (± 1 % tol.) resistor – making the Iref as 2.32 mA.

Figure 12-2. Processor BCLK Topology and Source Shunt Termination

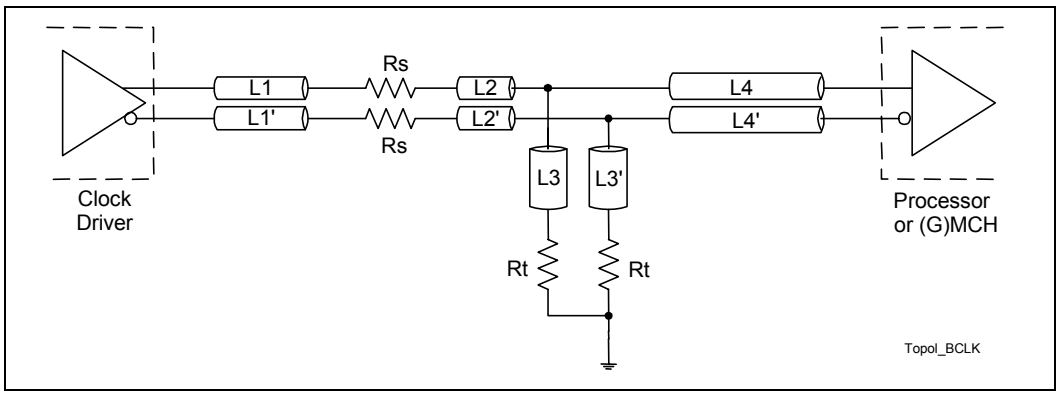


Table 12-3. Host Clock Routing Guidelines (BCLK[1:0]#, HCLKP, HCLKN)

Layout Guideline	Value	Notes
Host Clock Skew between agents	400 ps total Budget: 150 ps for Clock driver 250 ps for interconnect	2, 3, 4,5
Reference Plane	Ground Referenced (Contiguous over entire length)	
Differential pair spacing = S	8 mils	6, 7
Spacing to other traces	3S to 4S	
Nominal trace width = W	7.0 mils	8
System board Impedance – Differential	100 Ω ± 15%	9
System board Impedance – odd mode	50 Ω ± 15%	10
Processor routing length – L1, L1': Clock driver to Rs	0.5 inch max	13
Processor routing length – L2, L2': Rs to Rs-Rt node	0 – 0.2 inch	13
Processor routing length – L3, L3': RS-RT node to Rt	0 – 0.2 inch	13
Processor routing length – L4, L4': RS-RT Node to Load	2 – 12 inches	
(G)MCH routing length – L1, L1': Clock Driver to RS	0.5 inch max	13
(G)MCH routing length – L2, L2': Rs to Rs-Rt node	0 – 0.2 inch	13
(G)MCH routing length – L3, L3': RS-RT node to Rt	0 – 0.2 inch	13
(G)MCH routing length – L4, L4': RS-RT Node to Load	2 – 12 inches	
Clock driver to Processor and clock driver to chipset length matching (L1+L2+L4)	Clock pair to (G)MCH must be 100 mils longer than clock pair to processor socket	10
HCLKP – HCLKN, BCLK0 – BCLK1 length matching	± 10 mils	
Rs Series termination value	27 Ω ± 1%	11
Rt Shunt termination value	49.9 Ω ± 1% (for 50 Ω MB impedance)	12
Maximum Via Count Per Signal	3	

NOTES:

1. The skew budget includes clock driver output pair to output pair jitter (differential jitter), and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes clock pairs are routed on multiple routing layers and routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two bus agents. Measured at the crossing point.
5. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network.
7. Set line width to meet correct system board impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack-up.

8. The differential impedance of each clock pair is approximately 2*Zsingle-ended*(1-2*Kb) where Kb is the backwards cross-talk coefficient. For the recommended trace spacing, Kb is very small and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
9. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the BCLK traces vary within the tolerances specified, both traces of a differential pair must vary equally.
10. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the system board trace length for the chipset will be longer than that for the processor. Details of this additional length will be included in a future revision of the processor package files.
11. Rt shunt termination value should match the system board impedance.
12. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ring back.
13. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in Er and the impedance variations due to physical tolerances of circuit board material.

Host Clock Routing Guidelines

- When routing the 100/133 MHz differential clocks do not split up the two halves of a differential clock pair between layers and route to all agents on the same physical routing layer referenced to ground.
- If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Do not place Vias between adjacent complementary clock traces, and avoid differential Vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential Vias can be placed within length L1, between clock driver and RS, if needed to shorten length L1.

Differential Routing

- The host clock pairs must be routed differentially and on the same physical routing layer.
- **Do not** split the two halves of a differential clock pair. Route them referenced to ground for the entire length.

EMI constraints

- Clocks are a significant contributor to EMI and should be treated with care. Following recommendations can aid in EMI reduction:
- Maintain uniform spacing between the two halves of differential clocks
- Route clocks on physical layer adjacent to the VSS reference plane only

Figure 12-3. Clock Skew as Measured from Agent to Agent

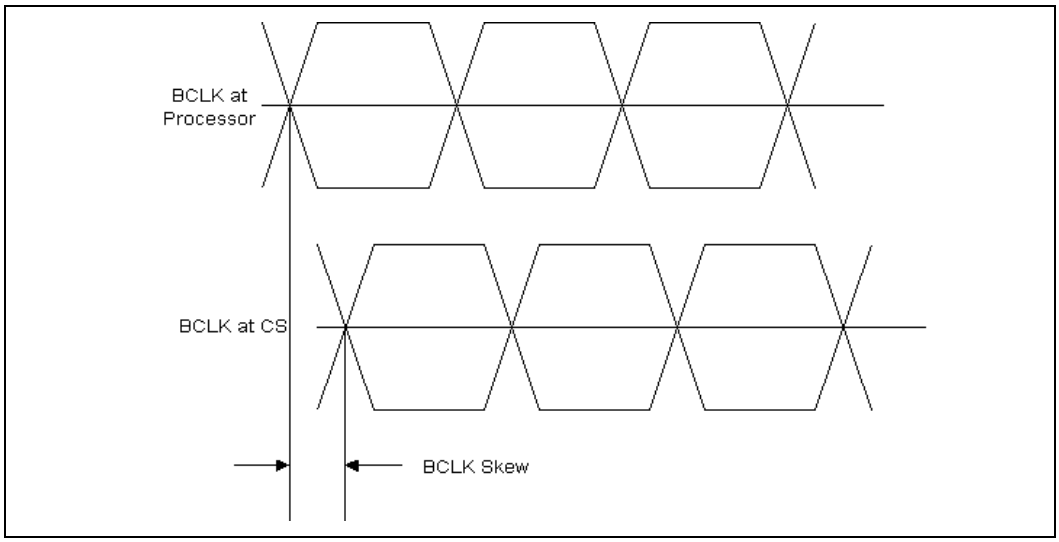
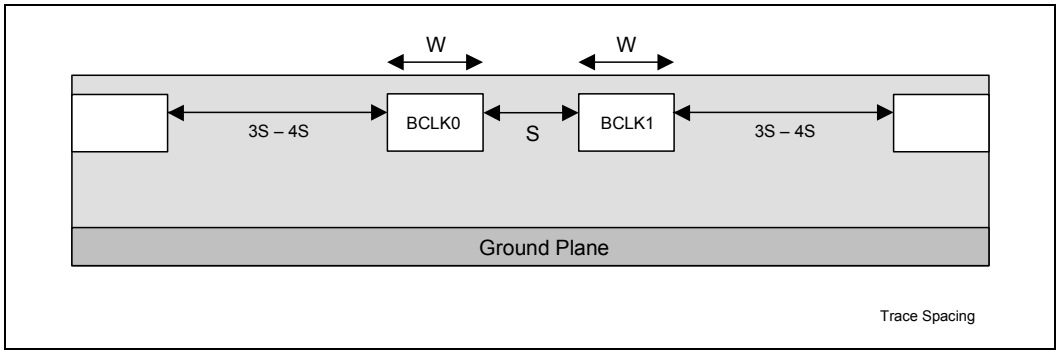


Figure 12-4. Trace Spacing



12.2.2 DOT_CLK Clock Group (Intel® 845GE chipset only)

The driver is the clock synthesizer 48 MHz clock output buffer and the receiver is the 48 MHz clock input buffer at the GMCH. Note that this clock is asynchronous to any other clock on the board.

Figure 12-5. Topology for DOT_CLK

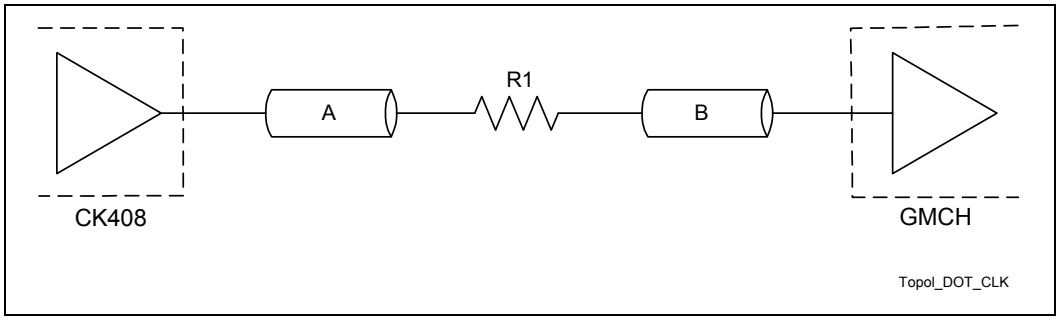


Table 12-4. DOT_CLK Routing Guidelines

Parameter	Routing Guidelines
Clock Group	DOT_CLK
Topology	Point-to-point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Spacing to other traces	20 mils
Trace Length – A	0.00 inch to 0.50 inch
Trace Length – B	2.0 inches to 9.0 inches
Resistor	R1 = 27 Ω ± 1%
Maximum Via Count Per Signal	3

12.2.3 CLK66 Clock Group

The driver is the clock synthesizer 66 MHz clock output buffer and the receiver is the 66 MHz clock input buffer at the Glue 4, (G)MCH and the ICH4. Note that the goal is to have as little skew between the clocks within this group. The 66 MHz clock to the Glue 4 chip has no trace length matching requirements with the rest of the clocks in this group.

Figure 12-6. Topology for CLK66

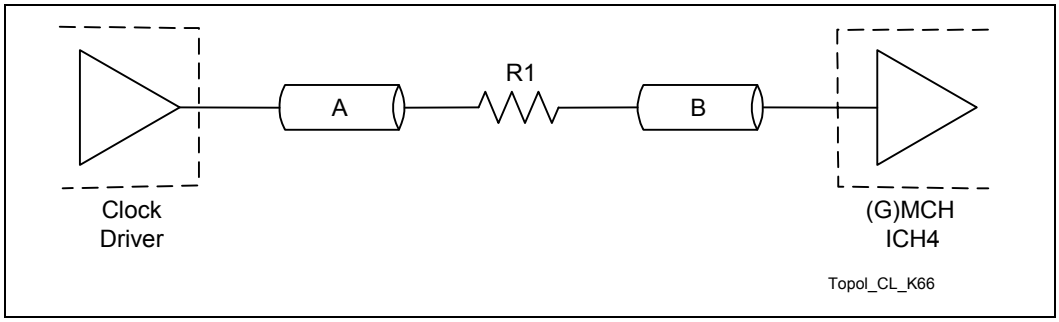


Table 12-5. CLK66 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK66
Topology	Point-to-point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Trace Spacing	20 mils
Spacing to other traces	20 mils
Trace Length – A	0.00 inch to 0.50 inch
Trace Length – B	4.00 inches to 8.50 inches
Resistor	R1 = 33 Ω ± 1%
Skew Requirements	All the clocks in the CLK66 group should have minimal skew (~0) between each other.
Clock Driver to (G)MCH	X
Clock Driver to ICH	X ± 100 mils
Maximum Via Count Per Signal	3

NOTE: If the trace length from the clock driver to the (G)MCH is X the trace length from clock to ICH4 must be X ± 100 mils.

12.2.4 AGPCLK Clock Group

The driver is the clock synthesizer 66 MHz clock output buffer and the receiver is the 66 MHz clock input buffer at the AGP device. Note that the goal is to have minimal (~ 0) skew between this clock and the clocks in the clock group CLK66.

Figure 12-7. Topology for AGPCLK to AGP Connector

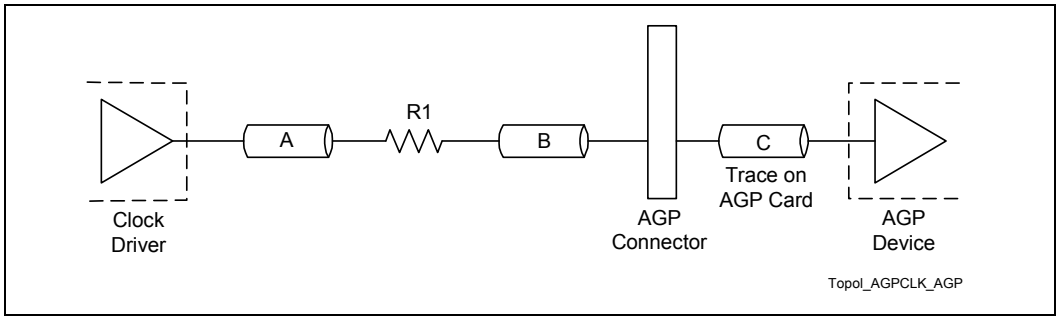


Figure 12-8. Topology for AGPCLK to AGP Device Down

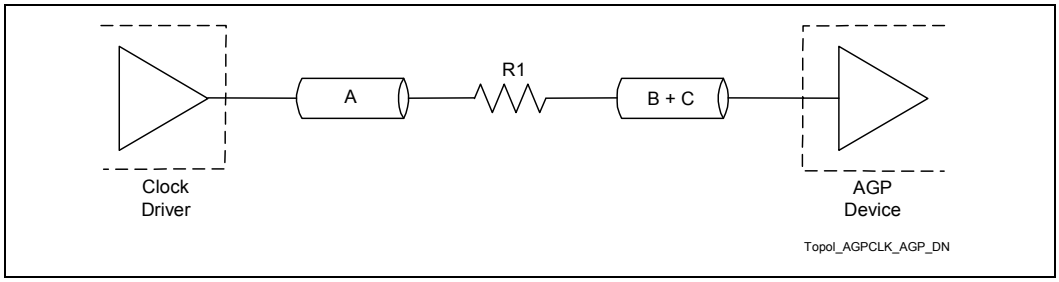


Table 12-6. AGPCLK Routing Guidelines

Parameter	Routing Guidelines
Clock Group	AGPCLK
Topology	Point-to-Point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Trace Spacing	15 mils
Spacing to other traces	15 mils
Trace Length – A	0.00 inch to 0.50 inch
Trace Length – B	(CLK66 Trace B) – 4 inches
Trace Length – C	Routed 4 inches per the AGP Specification
Resistor	R1 = 33 Ω ± 1%
Skew Requirements	Should have minimal (~ 0) skew between the AGPCLK and the clocks in the CLK66 clock group.
Maximum Via Count Per Signal	3

12.2.5 CLK33 Clock Group

The driver is the clock synthesizer 33 MHz clock output buffer and the receiver is the 33 MHz clock input buffer at the ICH4, FWH, Glue Chip, and SIO. Note that the goal is to have minimal (~ 0) skew between the clocks within this group, and also minimal (~ 0) skew between the clocks of this group and that of group CLK66.

Figure 12-9. Topology for CLK33

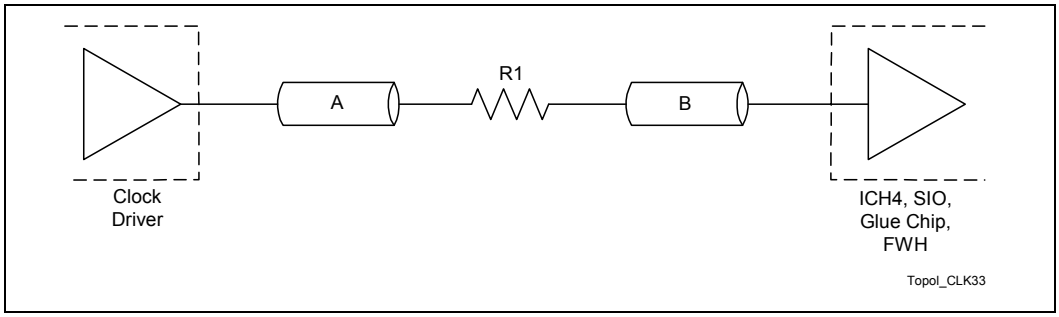


Table 12-7. CLK33 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point-to-Point
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Trace Spacing	15 mils
Spacing to other traces	15 mils
Trace Length – A	0.5 inch max
Trace Length – B	4.0” to 8.5”
Total Trace Length – A + B	(CLK66) ± 100 mils
Resistor	R1 = 33 Ω ± 5 %
Skew Requirements	Should have minimal (~ 0) skew between the clocks within this group, and also minimal (~ 0) skew between the clocks of this group and that of group CLK66.
Maximum Via Count Per Signal	4

12.2.6 CLK14 Clock Group

The driver is the clock synthesizer 14.318 MHz clock output buffer and the receiver is the 14.318 MHz clock input buffer at the ICH4 and SIO. Note that the clocks within this group should have minimal skew (~ 0) between each other, however each of the clocks in this group is asynchronous to clocks of any other group.

Figure 12-10. Topology for CLK14

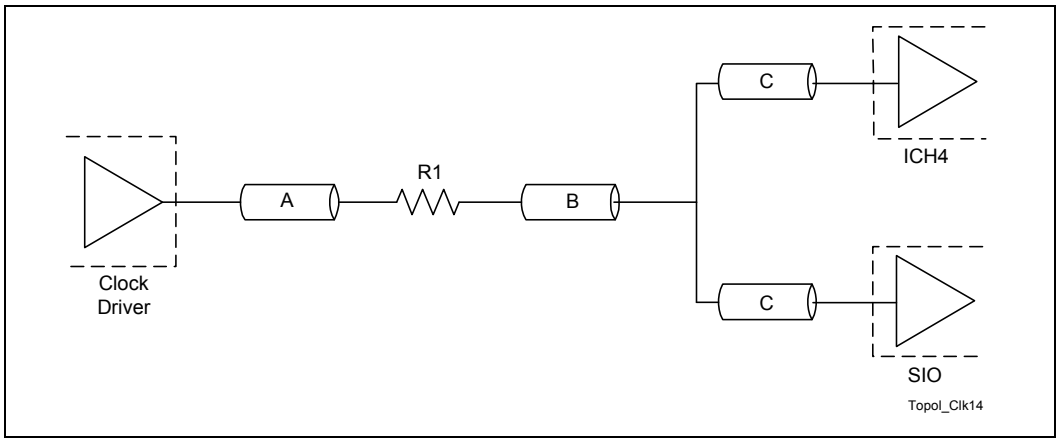


Table 12-8. CLK14 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK14
Topology	Balanced Topology
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Trace Spacing	10 mils
Spacing to other traces	10 mils
Trace Length – A	0.00 inch to 0.50 inch
Trace Length – B	0.00 inch to 12 inches
Trace Length – C	0.00 inch to 6 inches
CLK14 Total Length (A+B+C)	Matched to ± 0.5 inch of each other
Resistor	R1 = 33 Ω ± 5%

12.2.7 PCICLK Clock Group

The driver is the clock synthesizer 33 MHz clock output buffer and the receiver is the 33 MHz clock input buffer at the PCI devices. Note that the goal is to have a maximum of ±1 ns skew between the clocks within this group, and also a maximum of ±1 ns skew between the clocks of this group and that of group CLK33.

Figure 12-11. Topology for PCICLK to PCI Device Down

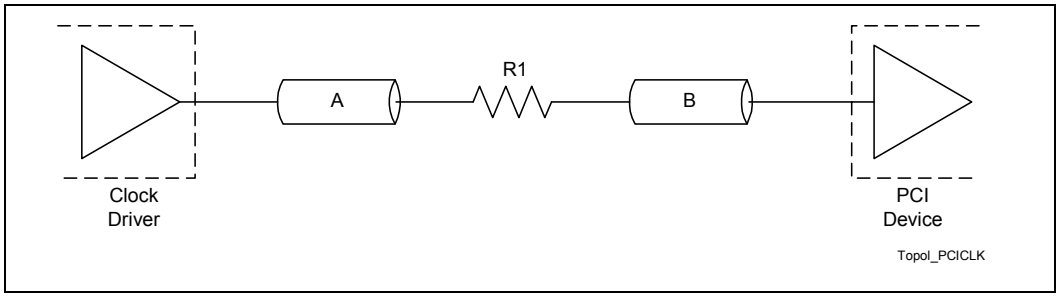


Table 12-9. PCICLK Routing Guidelines for PCI Device Down

Parameter	Routing Guidelines
Clock Group	PCICLK
Topology	Point-to-Point
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Trace Spacing	15 mils
Spacing to other traces	15 mils
Trace Length – A	0.50 inch max
Trace Length – B	Not Specified
Total Trace Length – A + B	(CLK33) ± 500 mils
Resistor	R1 = 33 Ω ± 5%
Maximum Via Count Per Signal	4

Figure 12-12. Topology for PCICLK to PCI Slot

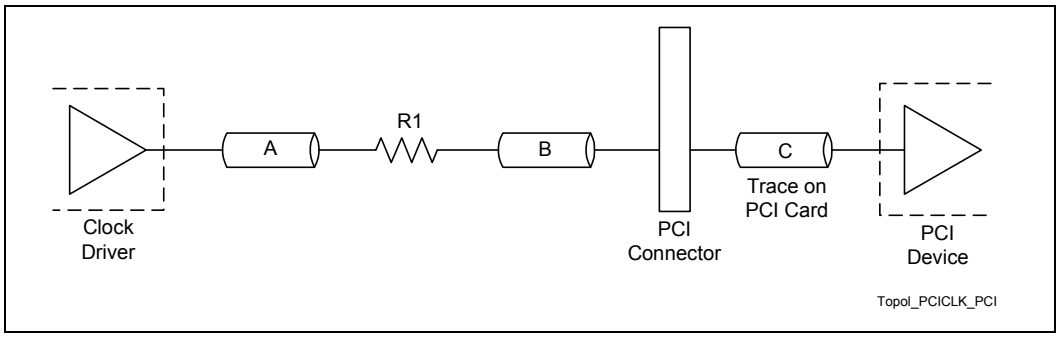


Table 12-10. PCICLK Routing Guidelines for Devices on PCI Cards

Parameter	Routing Guidelines
Clock Group	PCICLK
Topology	Point-to-Point
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Trace Spacing	15 mils
Spacing to other traces	15 mils
Trace Length – A	0.5 inch max
Trace Length – B	Not Specified Trace Length B constraints are indicated in the Total MB Trace Length – A + B parameters in this table.
Trace Length – C	2.50 inches, As per the PCI Specification
Total MB Trace Length – A + B	(CLK33 – 2.5 inches) ± 500 mils
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	Should have a maximum of ±1 ns skew between the clocks within this group, and also a maximum of ±1 ns skew between the clocks of this group and that of group CLK33.
Maximum via Count per signal	4

12.2.8 USBCLK Clock Group

The driver is the clock synthesizer USB clock output buffer and the receiver is the USB clock input buffer at the ICH4. Note that this clock is asynchronous to any other clock on the board.

Figure 12-13. Topology for USB_CLOCK

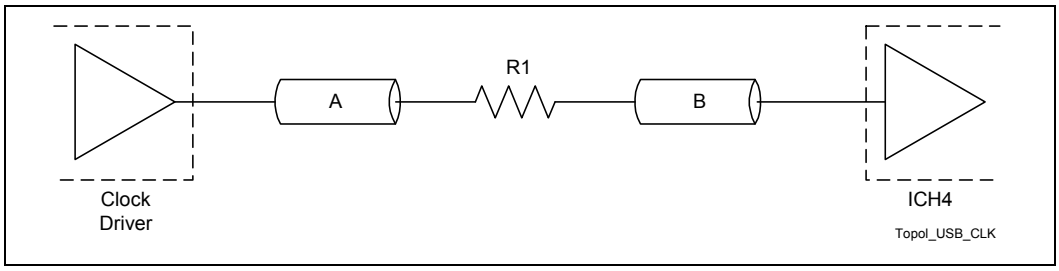


Table 12-11. USBCLK Routing Guidelines

Parameter	Routing Guidelines
Clock Group	USBCLK
Topology	Point-to-Point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Spacing to other traces	20 mils
Trace Length – A	0.00 inch – 0.50 inch
Trace Length – B	3.00 inches – 12.00 inches
Resistor	R1 = 27 Ω ± 5%
Skew Requirements	None – USBCLK is asynchronous to any other clock on the board
Maximum via Count per signal	3

12.3 CK408 Power Delivery

12.3.1 Power Plane Isolation

- Special care must be taken to provide quiet supplies to VDD, VDDA and 48 MHz VDD.
- The VDDA signal is especially sensitive to switching noise induced by the other VDD signals on the clock chip
    - The VDDA signal is also sensitive to switching noise generated elsewhere in the system (e.g., processor VRM). The LC Pie filter should be designed to provide the best reasonable isolation.

12.3.2 Referencing

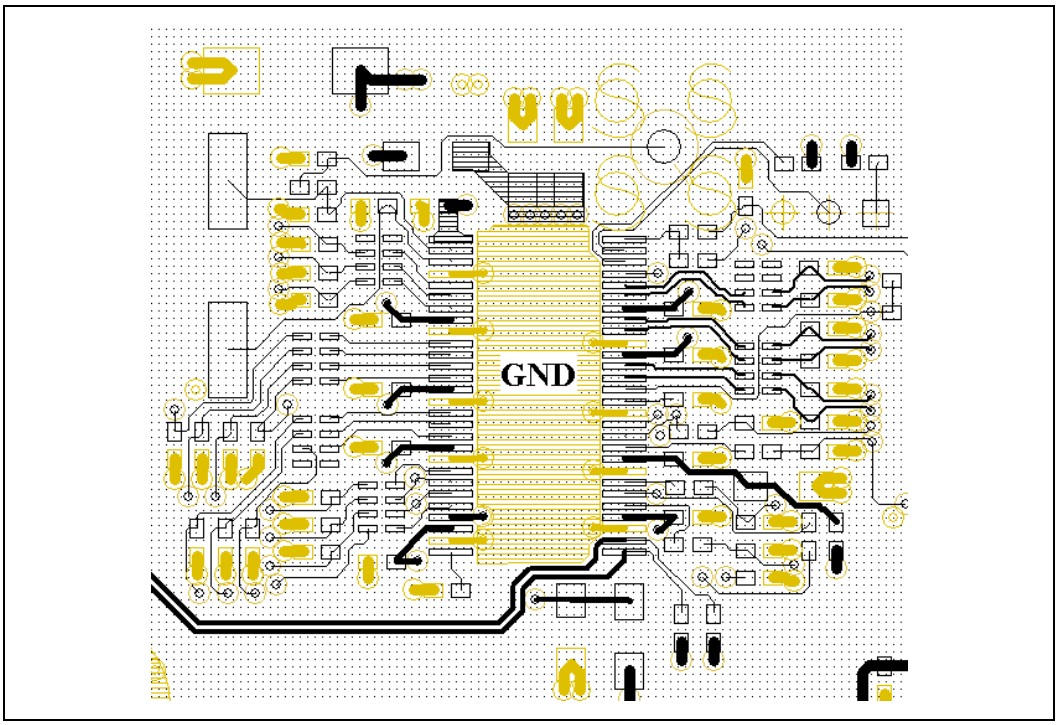
- Ground referencing is strongly recommended on all Host, 66 MHz, 48 MHz platform clocks.
- Motherboard layer transitions and power plane split crossing must be kept at a minimum.

12.3.3 Flooding

12.3.3.1 Option 1. (Signal-Power-Ground-Signal)

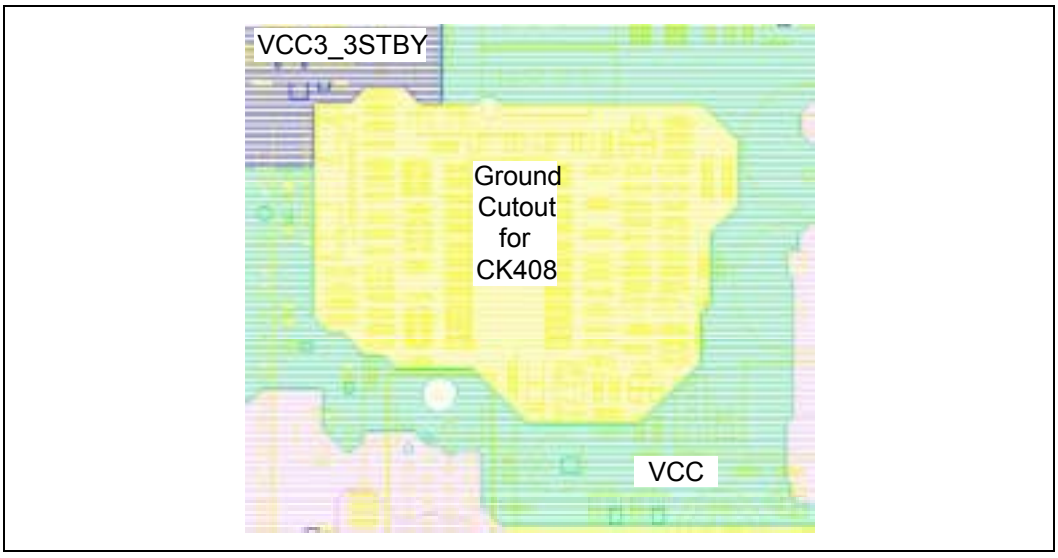
For a Signal-Power-Ground-Signal stack-up, it is **strongly recommended** that a solid ground flood be placed on layer 1 (signal layer) inside the part pads.

Figure 12-14. Layer 1 — Ground Flood on Signal Layer



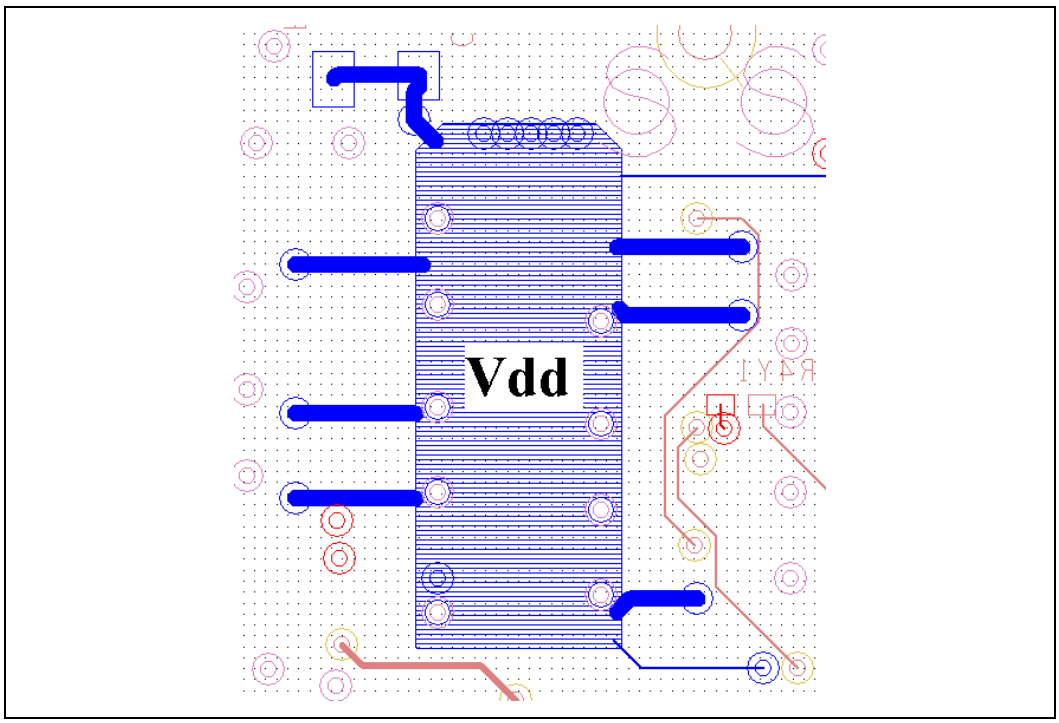
NOTE: A solid ground flood must be placed on layer 2 (power layer) to maintain ground referencing for critical signals.

Figure 12-15. Layer 2 — Ground Flood on Power Layer



NOTES:
1. A solid ground plane must be present on layer 3 (ground layer).
2. A solid 3.3 V power flood must be present on layer 4 (signal layer) inside the part pads.

Figure 12-16. Layer 4 — Power Flood on Signal Layer



NOTE: Signals after termination should via to the backside to be ground referenced on layer 4.

12.3.3.2 Option 2. (Signal-Ground-Power-Signal)

For a Signal-Ground-Power-Signal stack up, it is **strongly recommended** that:

- A ground flood be present on layer 1 (signal layer) inside the part pads.
- A solid ground plane be present on layer 2 (ground layer).
- A solid 3.3 V Power plane be present on layer 3 (power layer).
- Signals after termination should remain on the top layer to be ground referenced. (via to the front side).

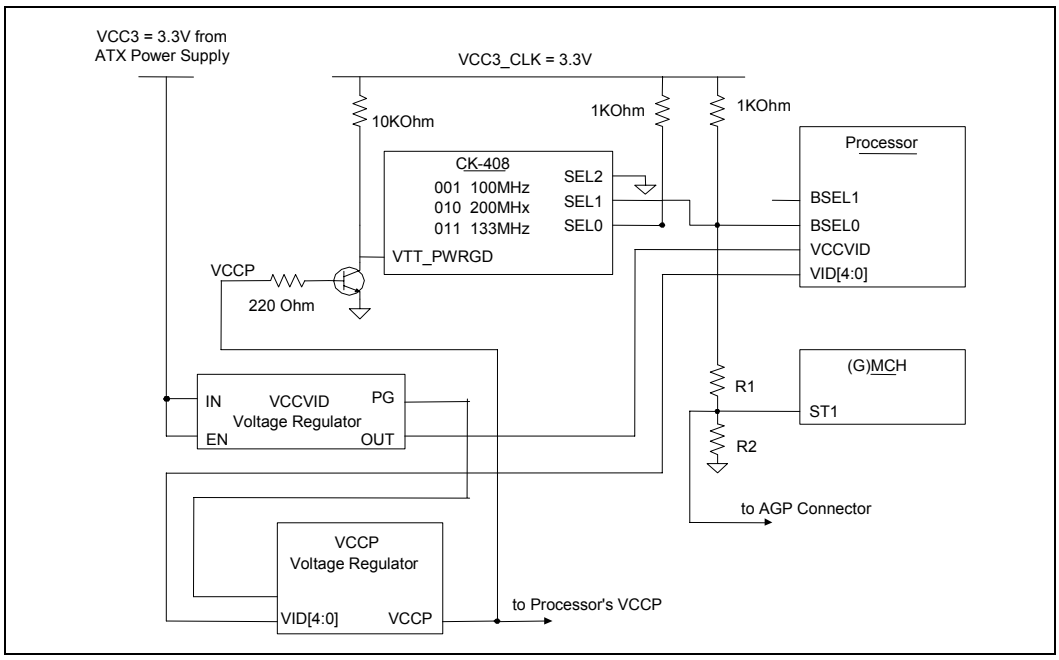
12.3.4 Clock Chip Decoupling

- For **all** power connections to planes, decoupling caps and vias, the **maximum** trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance.
- The VSS pins should not be connected directly to the VSS side of the caps. They should be connected to the ground flood under the part that is via'd to the ground plane to avoid VDD glitches propagating out, getting coupled through the decoupling caps to the VSS pins. This method has been shown to provide the best clock performance.
- The ground flood should be via'd through to the ground plane with no less than 12 – 16 vias under the part. It should be well connected.
- For all power connections, heavy duty and/or dual vias should be used.
- It is imperative that the standard signal vias and small traces not be used for connecting decoupling caps and ground floods to the power and ground planes.

12.3.5 CK408 Power Sequencing

Platforms need proper power sequencing of the CK408 with respect to the voltage regulators, processor, and (G)MCH. Figure 12-17 is a schematic showing the relationship between the VCCVID voltage regulator, the VCCP voltage regulator, CK408, processor, and (G)MCH

Figure 12-17. CK408, VREG, Intel® (G)MCH and Processor Interconnectivity



12.3.6 CK408 Power Plane Filtering

12.3.6.1 VDD Plane Filtering

The VDD decoupling requirements for a CK408 compliant clock synthesizer are as follows:

- (1) 300 Ω (@ 100 MHz) Ferrite Bead is recommended for the VDD plane.
- 10 µF of bulk decoupling in a 1206 package, placed close to the VDD generation circuitry, is recommended for the VDD plane. Although a 10 µF capacitor is recommended, (2) 4.7 µF capacitors can be used in place of a single 10 µF capacitor. It is also recommended that the capacitor be placed as close to the VDD generation circuitry as possible.
- (7) 0.1 µF high-frequency decoupling caps in 0603 packages are recommended for the VDD plane. It is recommended that one capacitor be placed as close to each VDD pin as possible.

12.3.6.2 VDDA Plane Filtering

The VDDA decoupling requirements for a CK408 compliant clock synthesizer are as follows:

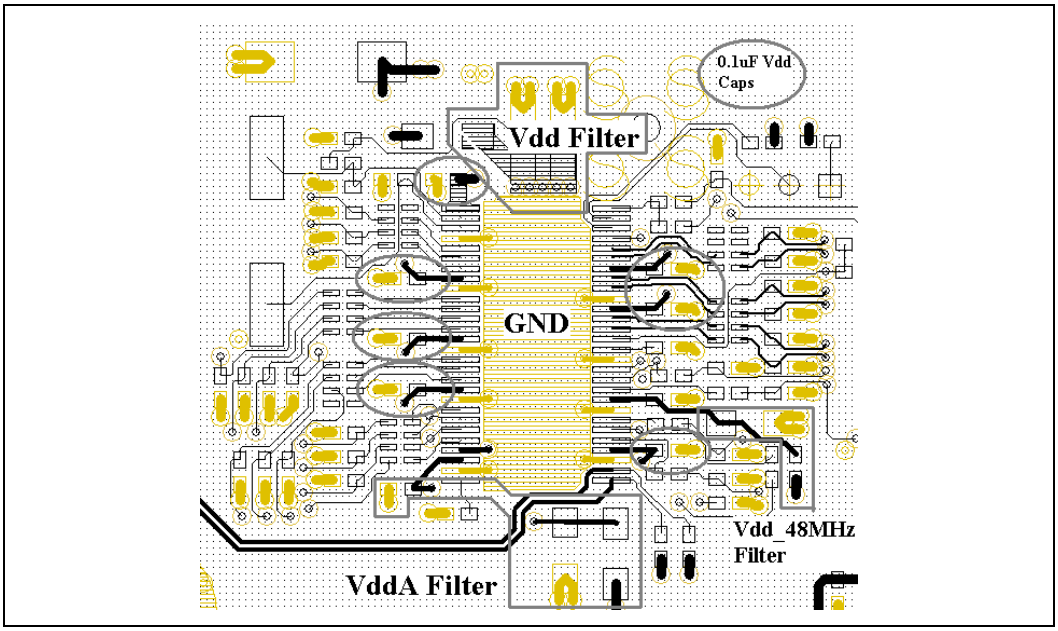
- (1) 300 Ω (@ 100 MHz) Ferrite Bead is recommended for the VDDA plane.
- 10 µF of bulk decoupling in a 1206 package, placed close to the VDDA generation circuitry, is recommended for the VDDA plane. Although a 10 µF capacitor is recommended, (2) 4.7 µF capacitors can be used in place of a single 10 µF capacitor. It is also recommended that the capacitor be placed as close to the VDDA generation circuitry as possible.
- (1) 0.1 µF high-frequency decoupling caps in 0603 packages are recommended for the VDD plane. It is recommended that one capacitor be placed as close to each VDD pin as possible.

12.3.6.3 VDD_48MHz Plane Filtering

The VDD_48MHz decoupling requirements for a CK408 compliant clock synthesizer are as follows:

- (1) 10 Ω (5%) series resistor is recommended for the VDD_48MHz plane.
- (1) 4.7 µF bulk-decoupling cap in a 1206 package is recommended for the VDD_48MHz plane. It is also recommended that the capacitor be placed as close to the VDD_48MHz generation circuitry as possible.
- (1) 0.1 µF high-frequency decoupling caps in 0603 packages are recommended for the VDD_48MHz plane. It is recommended that one capacitor be placed as close to each VDD_48MHz pin as possible.

Figure 12-18. Decoupling Capacitors Placement and Connectivity



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13 Platform Power Guidelines

This chapter presents the power guidelines for an 845GE/845PE chipset platform. Power delivery architecture, power supply decoupling, power sequencing and power management are covered. Table 13-1 defines some of the terms used in this chapter.

Table 13-1. Power Terms and Definitions

Term	Description
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered.
Full-power operation	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state and the S1 (processor stop-grant state) state.
Suspend operation	During suspend operation, power is removed from some components on the motherboard. The customer reference board supports three suspend states: Suspend-to-RAM (S3), Suspend-to- Disk (S4), and Soft-off (S5).
Power rails	An ATX power supply has 6 power rails: +5 V, -5 V, +12 V, -12 V, +3.3 V, 5 V SB In addition to these power rails, several other power rails are created with voltage regulators.
Core power rail	A power rail that is only on during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX 12 V power supply are +5 V, -5 V, +12 V, -12 V, +3.3 V.
Standby power rail	A power rail that in on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is: 5 V SB (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived power rail	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3 V SB is usually derived (on the motherboard) from 5 V SB using a voltage regulator.
Dual power rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during suspend operation and derived from a core supply during full-power operation. Note that the voltage on a dual power rail may be misleading.

13.1 Power Delivery Map

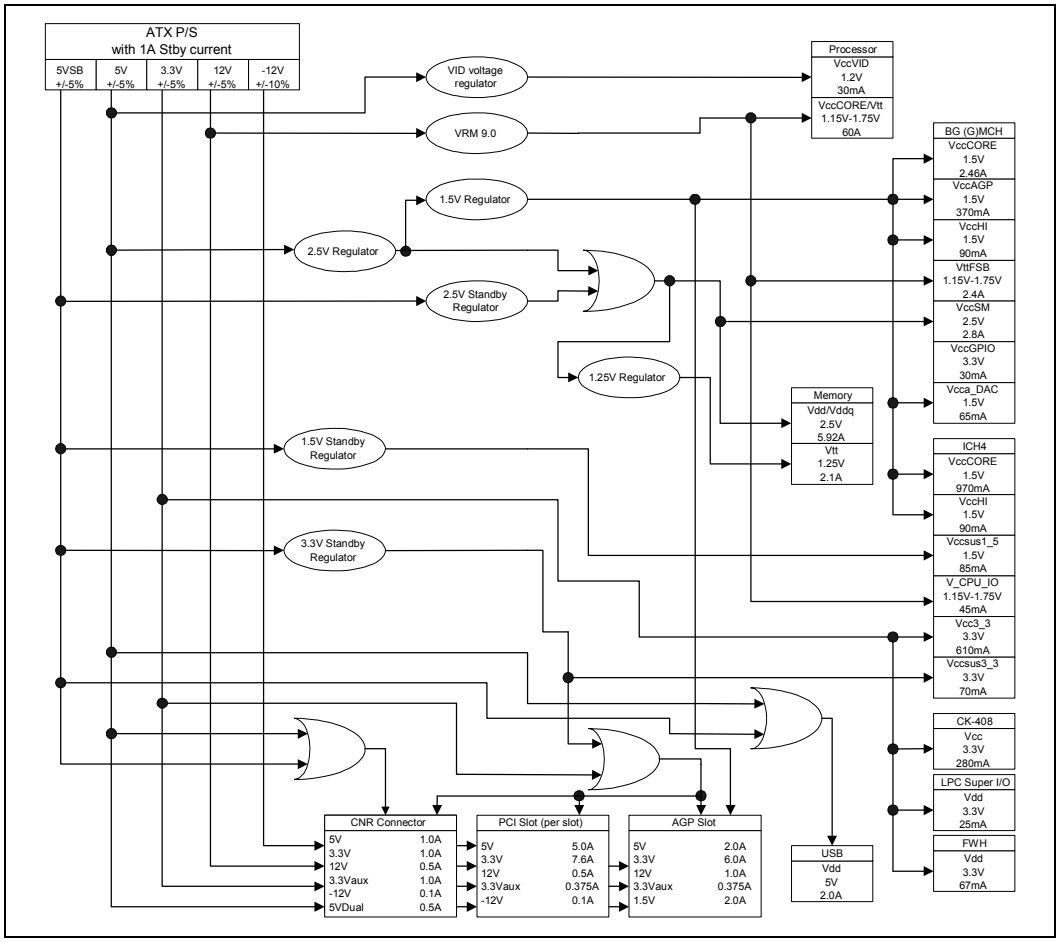
Figure 13-1 shows the power delivery architecture for an example 845GE/845PE chipset platform. This power delivery architecture supports the “Instantly Available PC Design Guidelines”.

During STR, only the necessary devices are powered. These devices include: main memory, the ICH4 resume well, PCI wake devices (via 3.3 VAUX), AC ’97, and USB. To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device’s power requirements, both in *suspend* and in *full-power*.

The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 VAUX (and possibly other devices in the system), it is necessary to create **dual** power rails.

The solutions in this design guide are only examples. Many power distribution methods achieve the similar results. When deviating from these examples, it is critical to consider the effect of a change.

Figure 13-1. Intel® 845GE/845PE Chipset DDR Platform Power Delivery Map



13.2 Intel® (G)MCH Power Delivery and Decoupling

13.2.1 Power Sequencing

There are no (G)MCH power sequencing requirements; however, the following must be observed:

- GCLKIN must be valid at least 10 µs prior to the rising edge of PWROK
- HCLKN/HCLKP must be valid at least 10 µs prior to the rising of RSTIN#

Good design practice would have all power rails come up as close in time as practical.

13.2.2 Intel® (G)MCH Analog Power Delivery

There are five analog circuits that require filtered supplies on the (G)MCH. They are: VCCQSM, VCCASM, VCCA_FSB, VCCA_DAC, and VCCA_DPLL (VCCA_DAC and VCCA_DPLL analog circuits are for 845GE chipset only). VCCA_DAC does not require an LC filter. It must be connected directly to the 1.5 V power plane through a trace. Its decoupling requirements are listed in Table 13-4.

Figure 13-2. Example Analog Supply Filter for VCCQSM, VCCASM, VCCA_DPLL, and VCCA_FSB

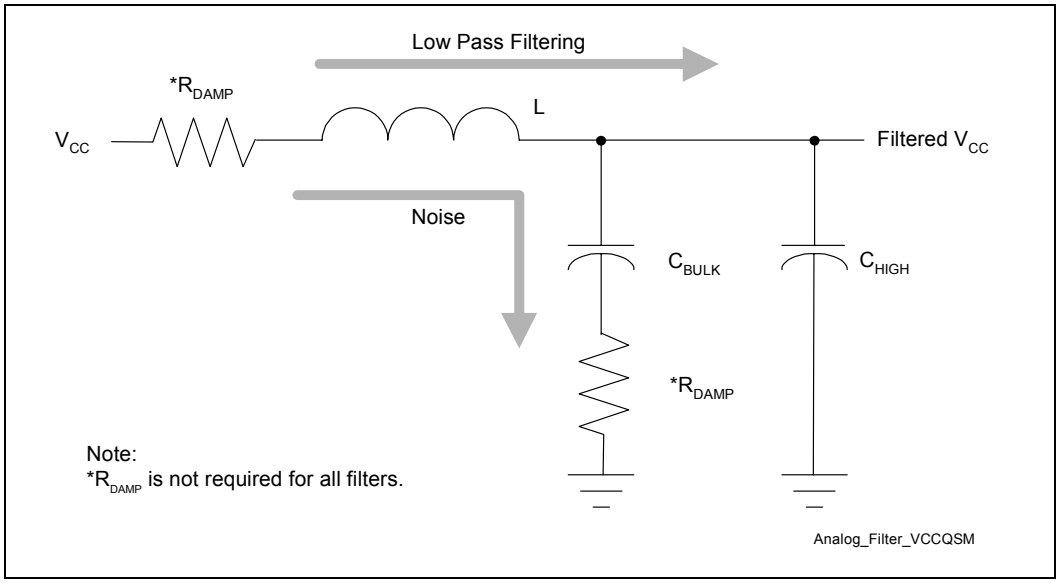


Figure 13-3. Filter Characteristics

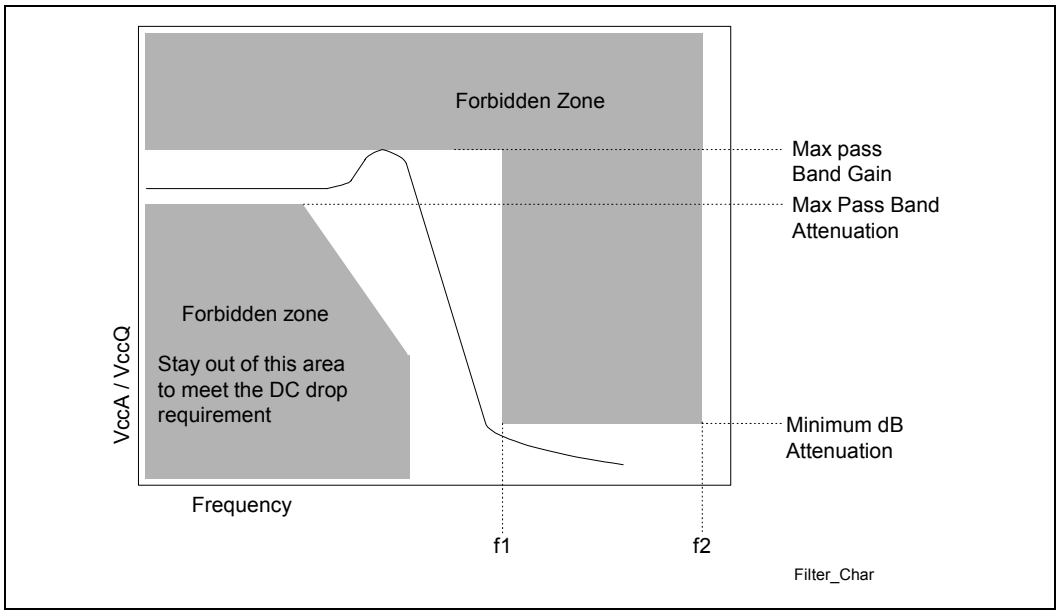


Table 13-2. Filter Requirements

Required Intel® 845GE/845PE Chipset Filters	Filter Current Capability (mA)	Filter DC Resistance (Ohms)[1]	Max DC Drop (mV)[2]	Pass Band Gain (dB)	f1	f2	Attenuation From f1 to f2 (dB)
VCCA_DPLL – (845GE chipset only)	35	2	70	<+0.2, >0.5	10 kHz	1 MHz	-20
VCCQSM – DDR	150	0.8	120	<+0.2, >-0.5	50 MHz	133 MHz	-30
VCCASM – DDR	500	0.14	70	<+0.2, >-0.5	50 MHz	266 MHz	-30
VCCA_FSB	30	2.3	70	<+0.2, >-0.5	50 MHz	533 MHz	-30

NOTES:
1. Filter DC resistance is the inductor resistance + MB routing resistance
2. DC drop across filter includes voltage drop across the inductor and across the MB trace

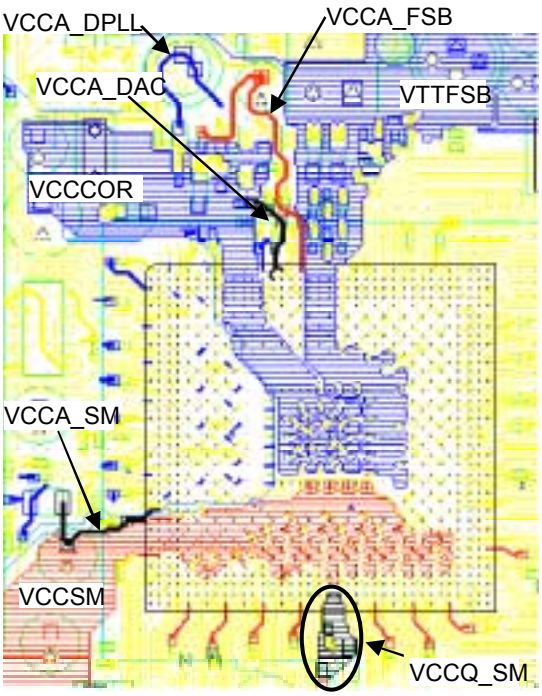
Table 13-3. Recommended Filter Components

Required Intel® 845GE/845PE Chipset Filters	Rdamp	Rdamp Location	L	Cbulk	Chigh
VCCA_DPLL (845GE chipset only)	1 Ω	In series with inductor	0805 10 µH	680 µF	0603 0.1 µF X5R (empty)
VCCQSM – DDR	1 Ω	In series with capacitor	0805 0.68 µH DCRmax 0.80 Ω	1206 4.7 µF X5R	0603 0.1 µF X5R
VCCASM – DDR	none	N/A	1210 1 µH DCRmax 0.078 Ω	100 µF AlEl	0603 0.1 µF X5R
VCCA_FSB	none	N/A	0603 0.82uH	22 µF AlEl	0603 0.1 µF X5R

13.2.3 Intel® (G)MCH Power Delivery

Power is delivered to the (G)MCH through three different layers: layer 1, layer 2, and layer 4.

Figure 13-4. Intel® (G)MCH DDR Layer 1 Power Delivery



NOTE: VCCA_DAC ties directly into the 1.5 V rail. (845GE chipset only)

Figure 13-5. Intel® (G)MCH DDR Layer 2 Power Delivery

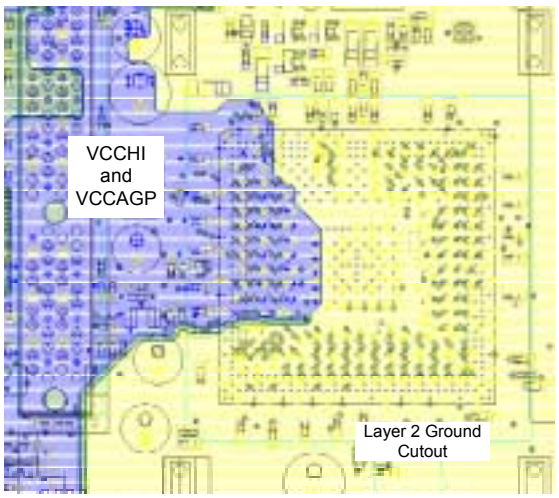
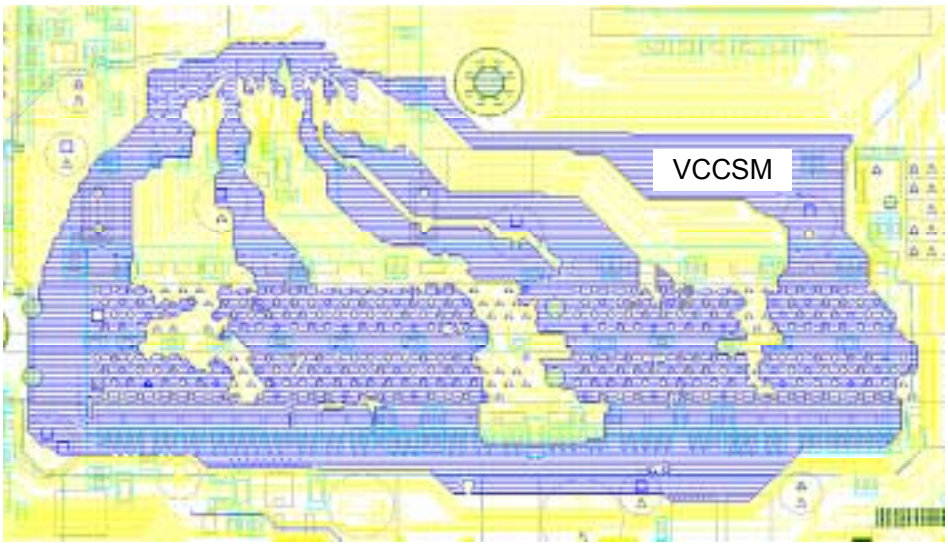
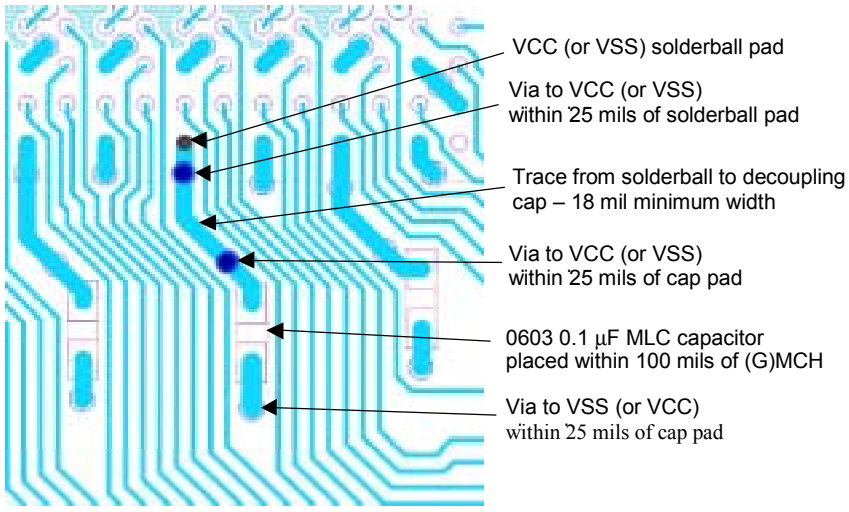


Figure 13-6. Intel® (G)MCH DDR Layer 4 Power Delivery



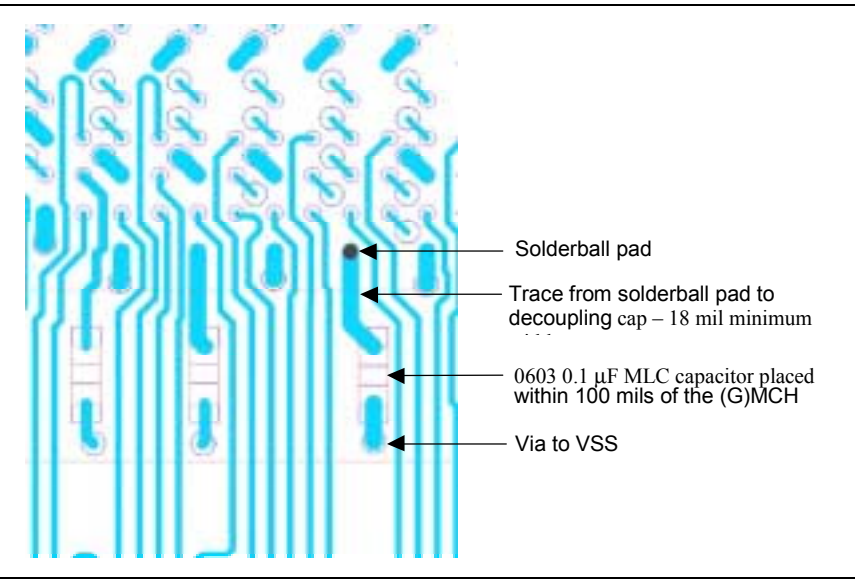
13.2.4 Intel® (G)MCH Decoupling

Figure 13-7. Example Decoupling Capacitor



NOTES:
1. Decoupling capacitors placed in/by a power corridor do not require the vias between the solder ball and the capacitor pad all other decoupling capacitors require the vias to the appropriate power or ground plane.
2. If the trace from the solder ball to the capacitor is less than 100 mils, one of the two vias may be omitted.

Figure 13-8. Example Edge Cap



NOTE: There **must not** be any vias placed in the trace leading from the solder ball pad to an edge capacitor.

Table 13-4. High-Frequency Decoupling Requirements for Intel® (G)MCH

Pin	Decoupling Requirements	Decoupling Type (Ball Type)	Decoupling Placement [1]
VTT_DECAP	(5) 0.1 µF	Edge Cap [2]	Place near balls: AC37, R37, L37, G37, and A31
VTTFSB	(5) 0.1 µF	Decoupling Cap (VTT)	Place within 250 mils of the package in the VTT corridor
VCC	(1) 0.1 µF	Decoupling Cap (VCC)	Place within 100 mils of the package in or near the VCC corridor
VCCAGP	(5) 0.1 µF	Decoupling Cap (VSS)	Place near balls: A5, E1, J1, N1, and U1
VCCHI	(2) 0.1 µF	Decoupling Cap (VSS)	Place near balls: AA1 and AE1
VCCSM	(8) 0.1 µF	Decoupling Cap (VCC)	Place near balls: AL37, AU5, AU9, AU13, AU17, AU25, AU29, and AU33
VCCA_DAC (82845GE Only)	(1) 0.1 µF (1) 0.01 µF	Decoupling Cap (VCC)	Place near balls: B14 and A15

NOTES:
1. Unless otherwise noted, capacitors should be placed less than 100 mils from the package.
2. Edge Caps **must not** have vias in the trace from the cap to the (G)MCH solder ball. They also **must not** connect to the motherboard VTT plane.

Figure 13-9. Intel® (G)MCH High-Frequency Decoupling Capacitor Placement

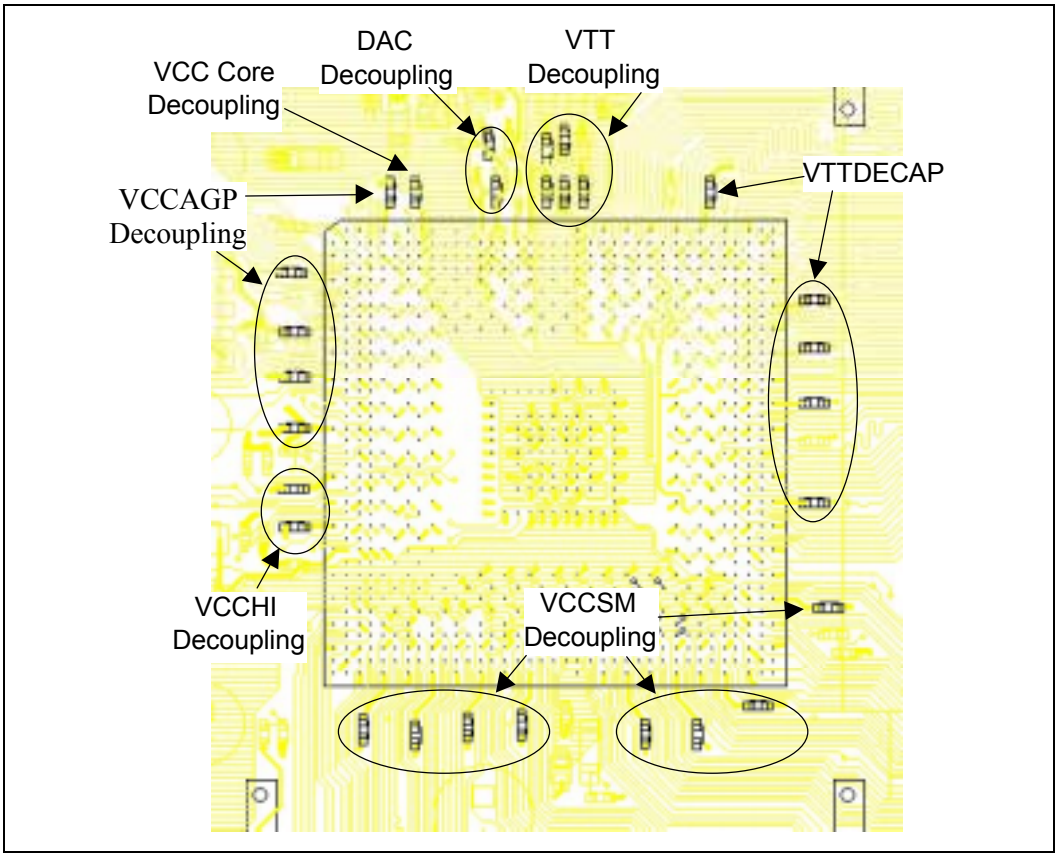


Figure 13-10. Intel® (G)MCH Bulk Decoupling Capacitor Placement

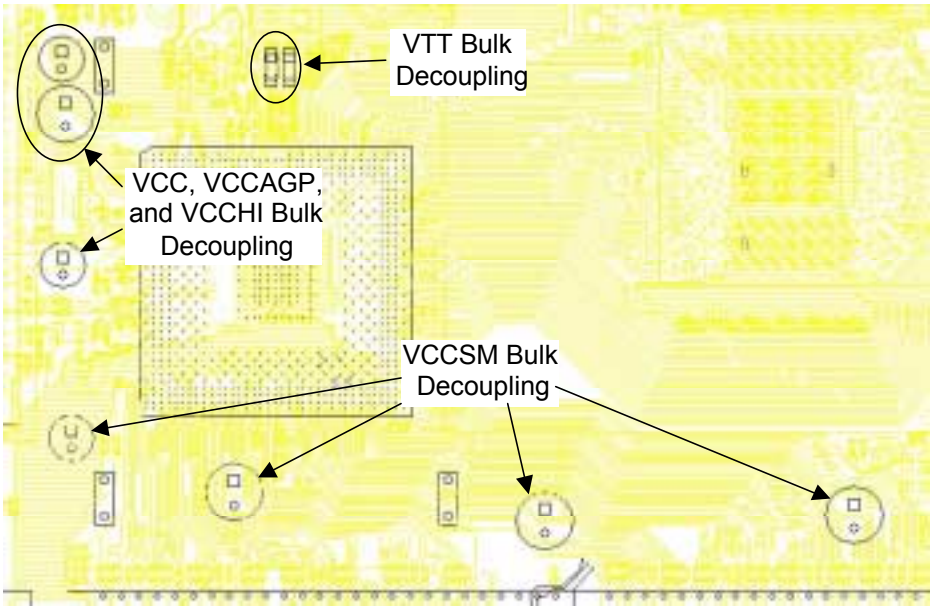


Table 13-5. Bulk Decoupling requirements for Intel® (G)MCH

Plane	Decoupling Requirements	Decoupling Placement
VTTFSB	(2) 10 µF	Place in VTT power corridor as shown in the above finger
VCC/VCCAGP/VCCHI	(2) 100 µF (1) 220 µF	Place between the AGP connector and the GMCH as shown in Figure 13-10. The 220 µF and one 100 µF cap must be placed in the VCC_CORE plane.
VCCSM	(4) 100 µF	Placed between the (G)MCH and DIMMs as shown in Figure 13-10 (one of the capacitors must be placed in the layer one shape)

13.3 Intel® ICH4 Power Delivery and Decoupling

13.3.1 Power Sequencing

13.3.1.1 1.5 V / 3.3 V Power Sequencing

There is no power sequencing requirements for the 3.3 V and 1.5 V rails of the ICH4. It is generally good design practice to power core up as closely to the other rails as possible.

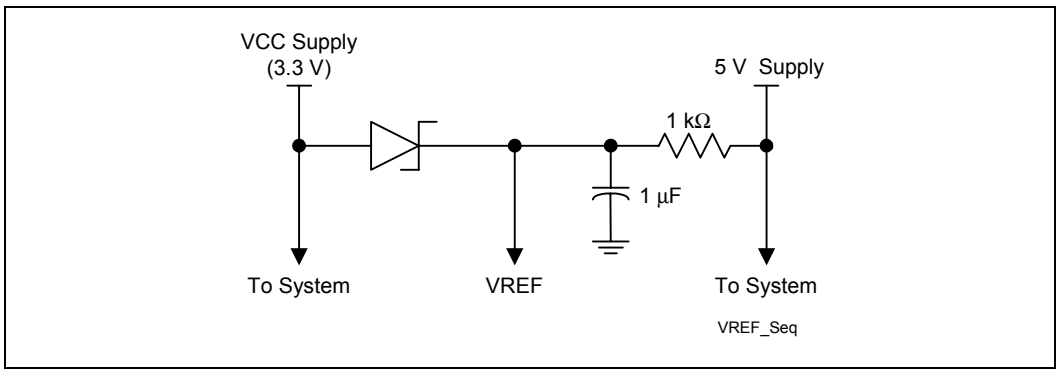
13.3.1.2 3.3 V / V5REF Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH4. V5REF must be powered up before VCC3_3, or after VCC3_3 within 0.7 V. Also, V5REF must power down after VCC3_3, or before VCC3_3 within 0.7 V. This rule must be followed to ensure the safety of the ICH4. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 13-11 shows a sample implementation of how to satisfy the V5REF/3.3 V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the VccSus3_3 rail is derived from the VccSus5 rail and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

Additionally, the ICH4 requires the V5REF_Sus rail to be hooked to a 5 V sustained source.

Figure 13-11. Example 3.3 V / V5REF Sequencing Circuitry



13.3.1.3 Power Supply PS_ON Consideration

If a pulse on SLP_S3# or SLP5# is short enough (~ 10 – 100 ms) such that PS_ON is driven active during the exponential decay of the power rails, a few power supply designs may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back-up. These power supplies would need to be unplugged and re-plugged to bring the system back-up. Power supplies not designed to handle this condition must have their

power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

The ATX specification does not specify a minimum pulse width on PS_ON deassertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

The platform designer must ensure that the power supply used with the platform is not affected by this issue.

13.3.2 Intel® ICH4 Analog Power Delivery

There are no analog ICH4 circuits requiring filters.

13.3.3 Intel® ICH4 Power Delivery

ICH4 Power Delivery is accomplished through layer 1, layer 2, and layer 4.

Figure 13-12. Intel® ICH4 Layer 1 Power Delivery

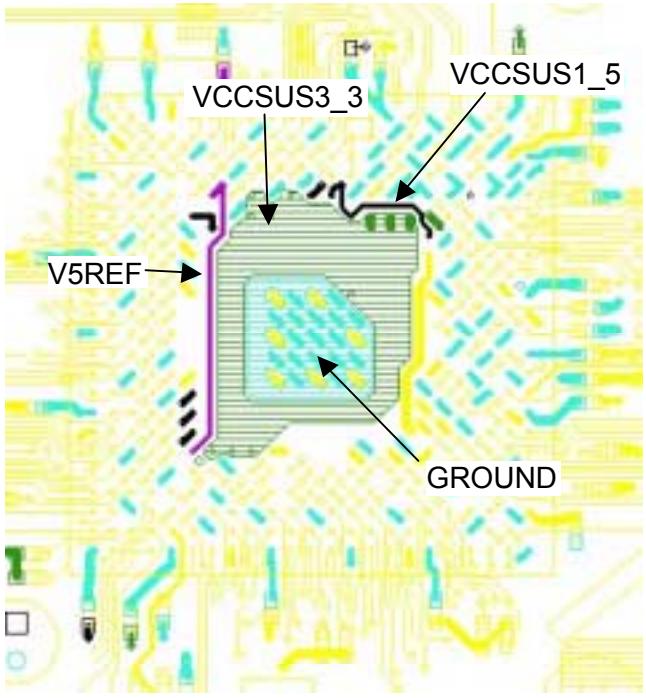


Figure 13-13. Intel® ICH4 Layer 2 Power Delivery

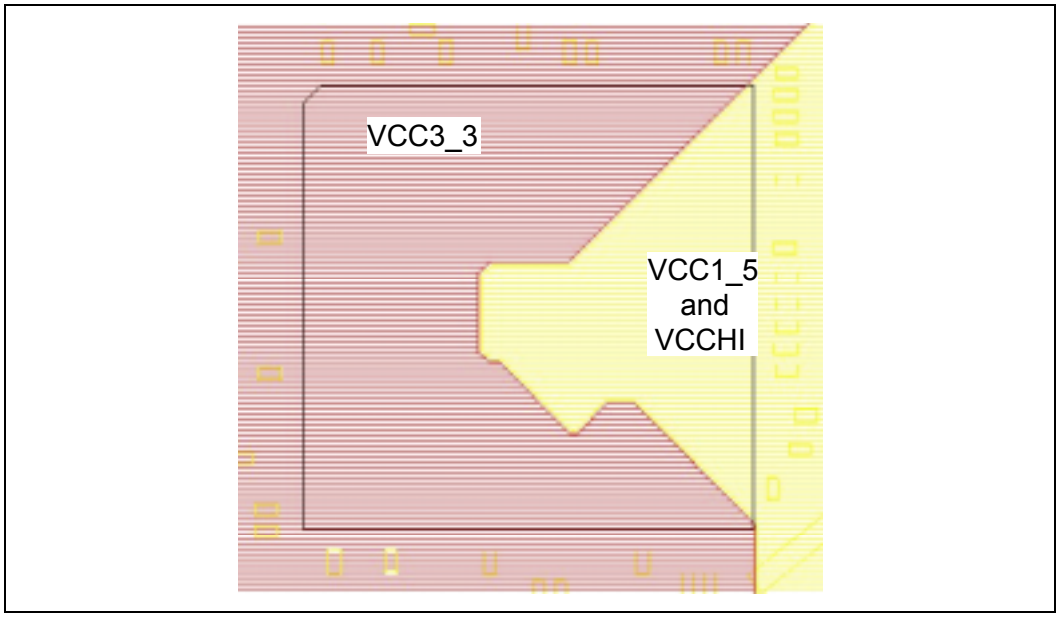
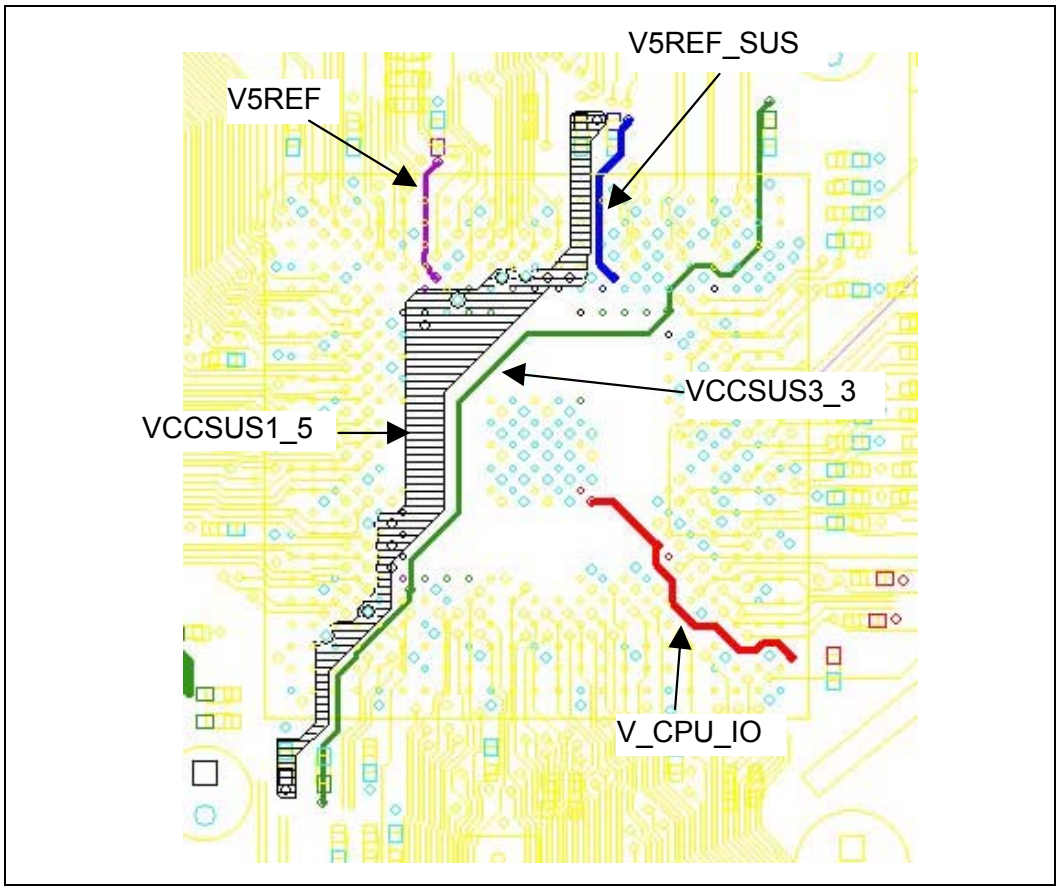


Figure 13-14. Intel® ICH4 Layer 4 Power Delivery



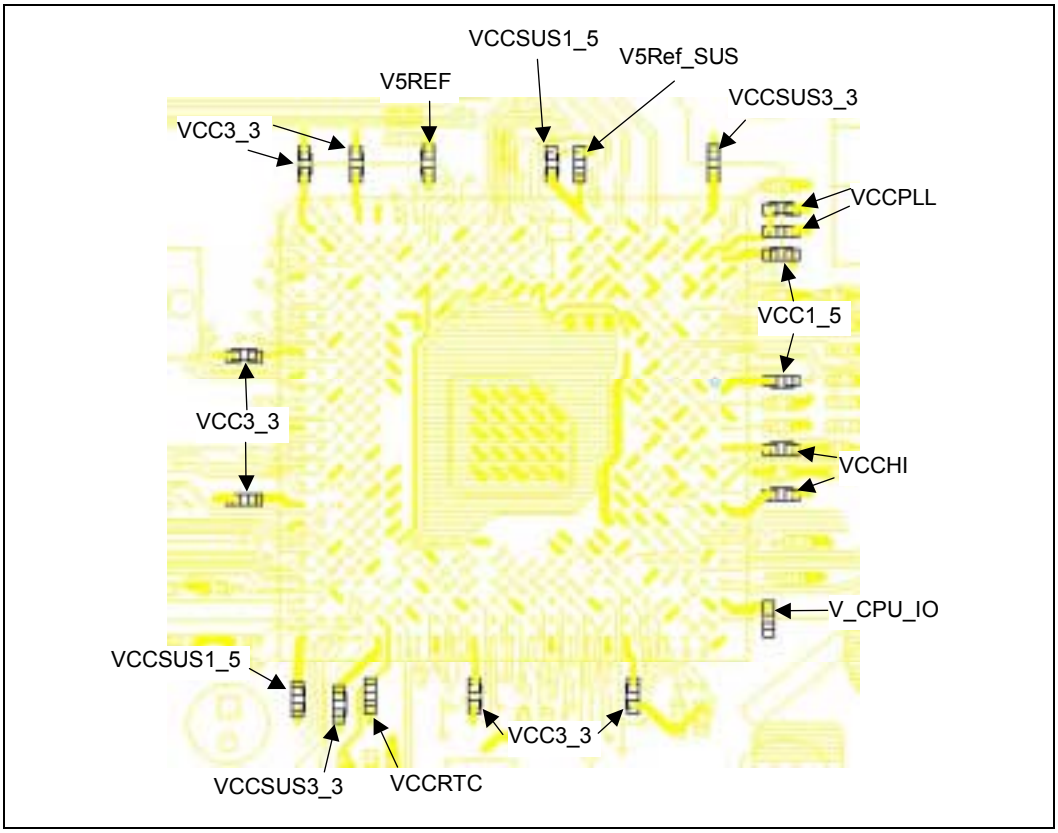
13.3.4 Intel® ICH4 Decoupling

Table 13-6. Decoupling Requirements for Intel® ICH4

Pin	Decoupling Requirements	Decoupling Type (Ball Type)	Decoupling Placement
VCC3_3	(6) 0.1 µF	Decoupling Cap (VSS)	Place near balls: A4, A1, H1, T1, AC10, and AC18
VCCSUS3_3	(2) 0.1 µF	Decoupling Cap (VSS)	Place near balls: A22 and AC5
V_CPU_IO	(1) 0.1 µF	Decoupling Cap (VCC)	Place near ball: AA23
VCC1_5	(2) 0.1 µF	Decoupling Cap (VSS)	Place near balls: K23 and C23
VccSus1_5	(2) 0.1 µF	Decoupling Cap (VSS)	Place near balls: A16 and AC1
V5REF	(1) 0.1 µF	Decoupling Cap (VCC)	Place near ball: E7
V5_REF_SUS	(1) 0.1 µF	Decoupling Cap (VSS)	Place near ball: A16
VCCRTC	(1) 0.1 µF	Decoupling Cap (VCC)	Place near ball: AB5
VCCHI	(2) 0.1 µF	Decoupling Cap (VSS)	Place near balls: T23 and N23
VCCPLL	(1) 0.1 µF (1) 0.01 µF	Decoupling Cap (VCC)	Place near ball: C22

NOTE: Capacitors should be placed less than 100 mils from the package.

Figure 13-15. Intel® ICH4 Decoupling Capacitor Placement



13.4 Thermal Design Power

The thermal design power is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus. For 845GE/845PE chipset package thermal characteristics, refer to the following:

- *Intel® 82801DB I/O Controller Hub 4 (ICH4): Thermal and Mechanical Design Guidelines*
- *Intel® 845GE/845PE Chipset Thermal Design Guide*

14 Platform Mechanical Guidelines

14.1 Intel® (G)MCH Retention Mechanism and Keep-Outs

Figure 14-1 shows the motherboard keep-out dimensions intended for the reference thermal/mechanical components for the 845GE/845PE chipset.

Figure 14-1. Intel® (G)MCH Retention Mechanism and Keep-Out Drawing

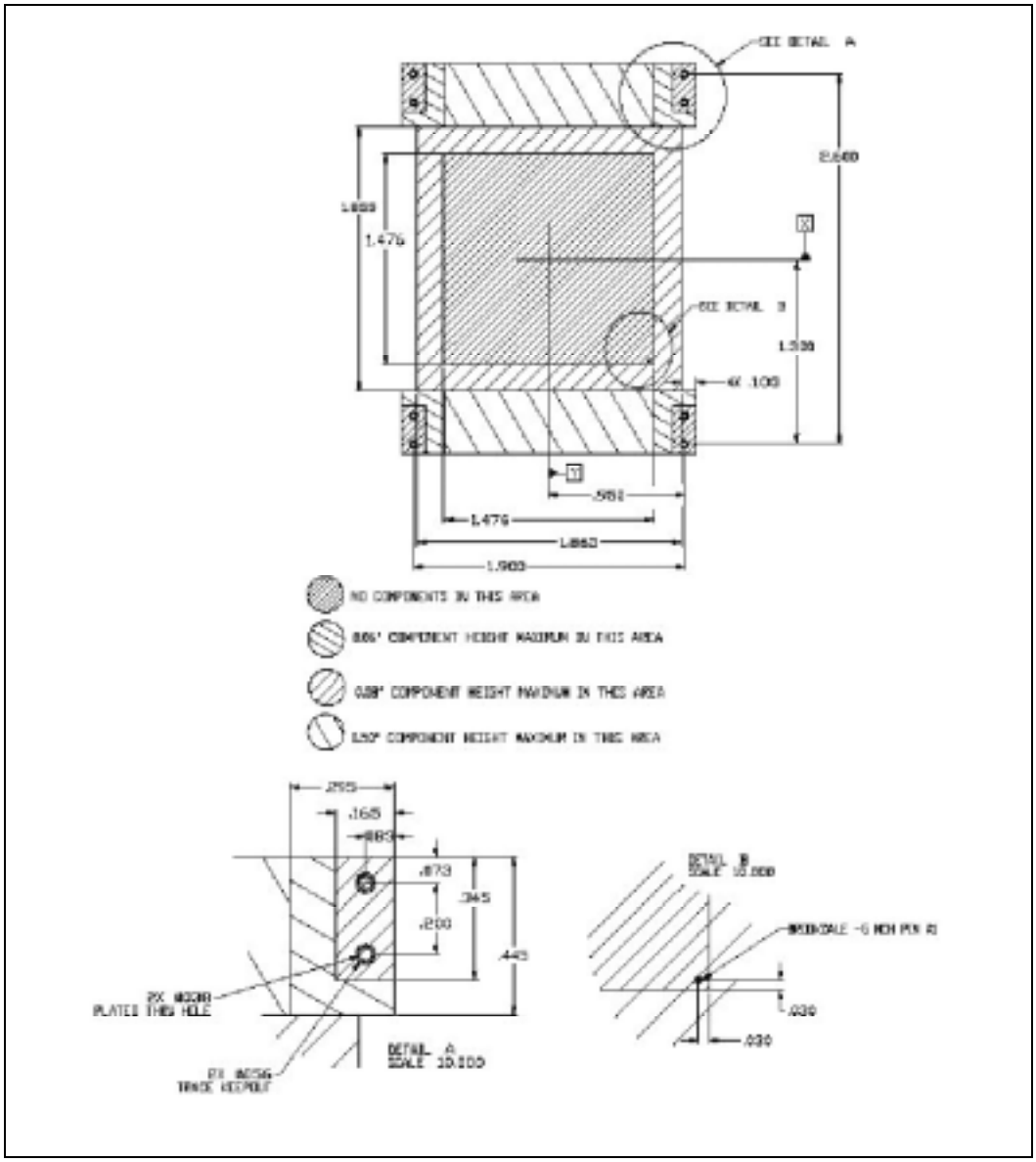
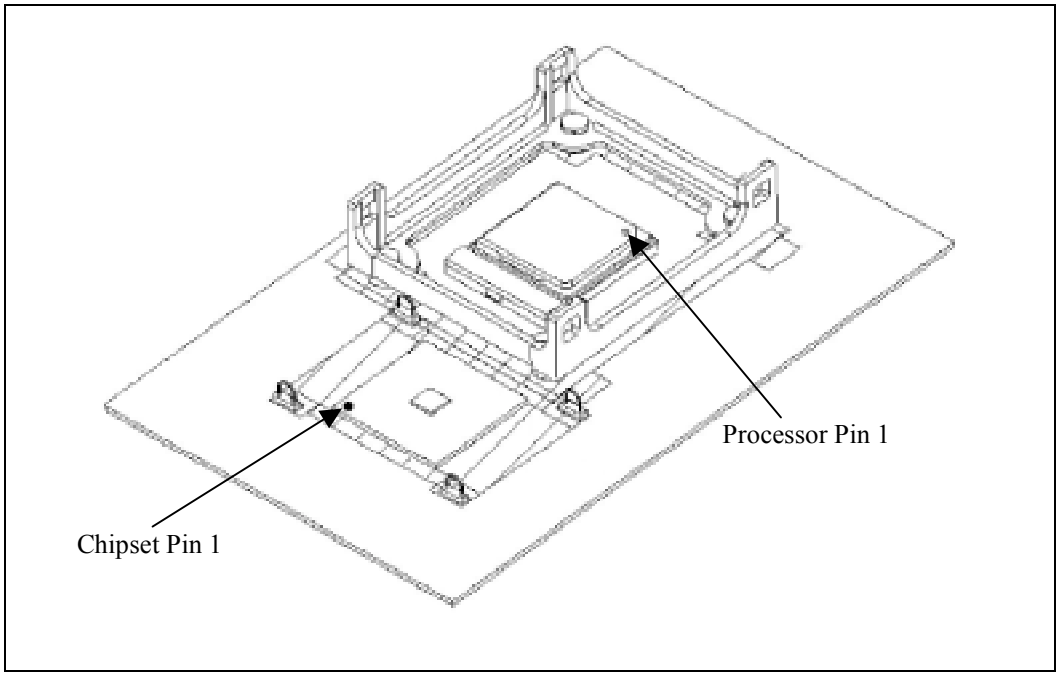


Figure 14-2. Typical Orientation of the Chipset Relative to the Processor



14.2 Intel® (G)MCH Package

Figure 14-3. Intel® (G)MCH Package (Bottom View)

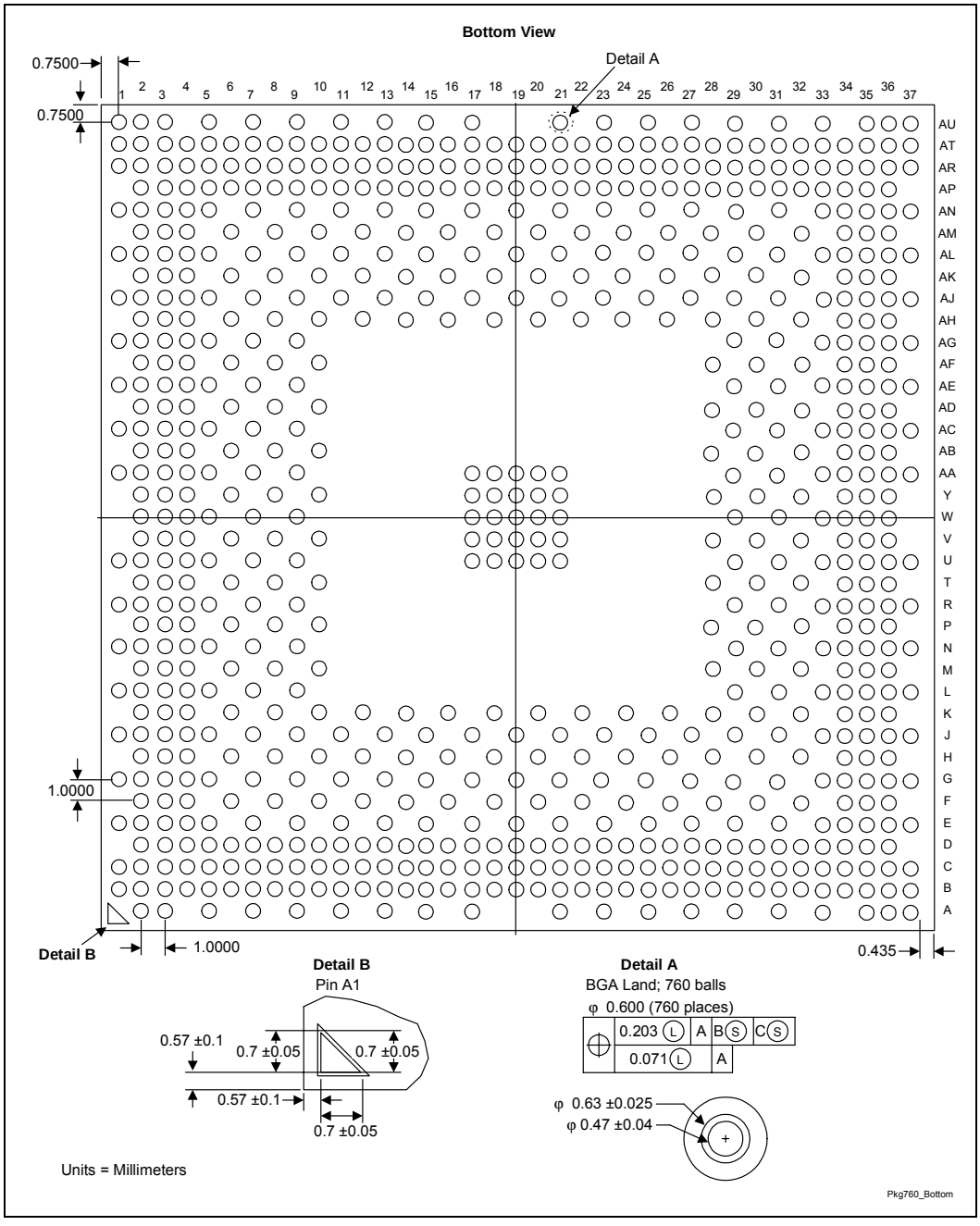
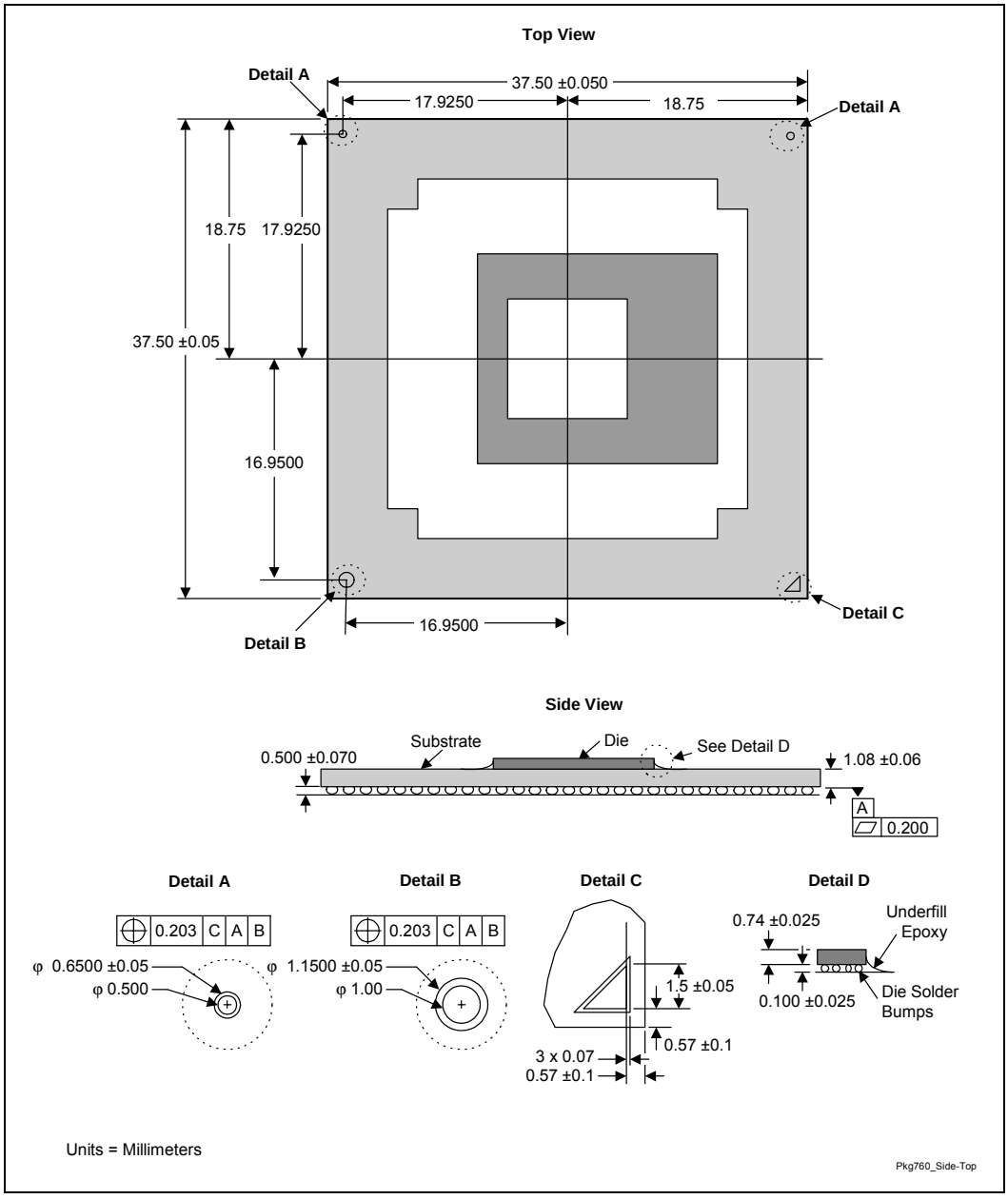


Figure 14-4. Intel® (G)MCH Package (Top and Side Views)



15 Intel® 845GE/845PE Chipset Design Layout Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements the 845GE/845PE chipset. The items contained within this checklist attempt to address important connections to these devices and any critical supporting circuitry. **This is not a complete list and does not guarantee that a design will function properly**. In addition, refer to the Customer Reference Schematics in Appendix A for more detailed instructions on designing a motherboard. This work is ongoing, and the recommendations and considerations herein are subject to change.

15.1 Processor and System Bus

15.1.1 AGTL+ Signals

Data Signals: HD[63:0]#, DINV_[3:0]# Data Strobes: HDSTB_P[3:0]#, HDSTB_N[3:0]# Address Signals: HA[31:3]#, HREQ_[4:0]# Address Strobes: HADSTB_[1:0]#	
Recommendation	**Reason/Impact/Documentation**
General Guidelines	
• Point-to-Point Topology	Refer to Table 4-1
• Referenced to VSS	Layer changes should not occur for any signals. If a layer change must occur, reference plane must be VSS and the layers must all be of the same configuration Refer to Table 4-1
• Route Data bus first • Route Address bus second (after the Data bus) • Route Common clock third	Refer to Table 4-1
• Breakout Guidelines (processor and (G)MCH): 7-mil wide with 5-mil spacing for a max of 250 mils from component ball	Refer to Table 4-1
• Data and common clock traces should be 7-mils wide with 13-mil spacing	Intel has simulated these recommendations for normal conditions. Refer to Section 4.2.2.1.
Group Spacing: Non Clock Spacing = 20 mils to any other signal	Refer to Table 4-1

Data Signals: HD[63:0]#, DINV_[3:0]# Data Strobes: HDSTB_P[3:0]#, HDSTB_N[3:0]# Address Signals: HA[31:3]#, HREQ_[4:0]# Address Strobes: HADSTB_[1:0]#	
Recommendation	**Reason/Impact/Documentation**
Data Signals / Data Strobes	
• Data line 2.0 inches to 8 inches pin-to-pin data signal lengths • Length compensation required	The length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without trace matching and length compensation flight times between the data signals and the strobes will result in inequity between the setup and hold times. Refer to Section 4.2.2.1.
• Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Signals should be referenced to VSS.	The length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without trace matching and length compensation flight times between the data signals and the strobes will result in inequity between the setup and hold times. Refer to Section 4.2.2.1.
• Data strobe and its complement should be routed to the same length as their corresponding data signals, mean pad to pad length should be ± 25 mils. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (VSS) and the layers are all of the same configuration (all stripline or all microstrip). • DSTBN/P[3:0]#	The impact of this recommendation causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. It is recommended to simulate skew to determine the length that best centers the strobe for a given system. Refer to Section 4.2.2.1.
• Data strobes and their complements should be routed within ± 25 mils of the same pad to pad length • If one strobe switches layers, its complement must switch layers in the same manner	The impact of this recommendation causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. It is recommended to simulate skew to determine the length that best centers the strobe for a given system. Refer to Section 4.2.

Data Signals: HD[63:0]#, DINV_[3:0]# Data Strobes: HDSTB_P[3:0]#, HDSTB_N[3:0]# Address Signals: HA[31:3]#, HREQ_[4:0]# Address Strobes: HADSTB_[1:0]#	
Recommendation	**Reason/Impact/Documentation**
Address Signals / Address Strobes	
• Address line 2.0 inches to 10.0 inches pin to pin data signal lengths • Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (VSS) and the layers are all of the same configuration (all stripline or all microstrip). • Length compensation required	The length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without trace matching and length compensation flight times between the data signals and the strobes will result in inequity between the setup and hold times. Refer to Section 4.2.2.1..
• Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes • Length compensation required • Address signals may change layers if reference plane remains the same (VSS) and the layers are all of the same configuration.	The length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without trace matching and length compensation flight times between the Address signals and the strobes will result in inequity between the setup and hold times. Refer to Section 4.2.
• Address Strobes (HADSTB_[1:0]#) should be routed to the same length as their corresponding address signals, mean pad to pad length should be ± 25 mils • Length compensation required • Address strobes may change layers if reference plane remains the same (VSS) and the layers are all of the same configuration.	The impact of this routing recommendation causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. Refer to Section 4.1.
• ADSTB0 and ADSTB1 should be routed within ± 25 mils of the same pad-to-pad length	Refer to Table 4-1
Common Clock BCLK[1:0]	
• 3.0 inches to 10.0 inches pin-to-pin common clock lengths. • No length compensation necessary	Refer to Table 4-1
• Common clock should be 7-mils wide and 13-mils spacing.	Refer to Section 4.2.2.1.
Trace Impedance	• 50 Ω ± 15%
Maximum via count per signal	• 4 • Avoid layer change as much as possible. • No layer change is recommendation. Refer to Section 4.1.

15.1.2 Asynchronous GTL+ and Miscellaneous AGTL+ Signals

Processor: FERR#, PROCHOT#, THERMTRIP# Intel® ICH4: A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI#, STPCLK#, PWRGOOD Miscellaneous AGTL+: BREQ0#, RESET#	
Recommendation	**Reason/Impact/Documentation**
General Guidelines	
• Point-to-Point Topology	
• Referenced to VSS	
• 5-mils wide with 7-mil spacing	
• Breakout Guidelines: None	
FERR#, THERMTRIP# • 1”-12” from processor to ICH4 • 3” max from ICH4 to VDD	Refer to Sections 4.3.1.1 and 4.3.1.3
PROCHOT# • 1” – 17” from processor to voltage translator • 3” max from Voltage translator to VDD • 10 inches max from Voltage translator to external logic	Refer to Section 4.3.1.2.
A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, STPCLK# • 17.0 inches max from Processor to Rs • 2.0 inches max from Rs to ICH4	Refer to Section 4.3.1.4.
INIT# • 3” max from VCC_CPU to Processor • 17” max from Processor to ICH4. • 2.0 inches max from ICH4 to Voltage Translator. • 10 inches max from voltage translator to FWH. • 3” max from VCC_FWH to FWH • Level shifting is required from the INIT# pin to FWH.	Refer to Section 4.3.1.5.
PWRGOOD • 1.0 inch to 12.0 inches max from processor to Rs • 2” max from Rs to ICH4 • 3.0 inches max from processor to VDD	Refer to Section 4.3.1.6.

Processor: FERR#, PROCHOT#, THERMTRIP# Intel® ICH4: A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI#, STPCLK#, PWRGOOD Miscellaneous AGTL+: BREQ0#, RESET#	
Recommendation	**Reason/Impact/Documentation**
BREQ0#, Reset# • Terminate using discrete components on the system board • Connect the signals between these components • ≤ 1" – 2" max from processor to Rt. • BREQ0#: Rt = 150 Ω to 220 Ω ± 5% • RESET#: Rt = 51 Ω ± 5% • ≤ 3" – 10 inches max from processor to (G)MCH	Refer to Section 4.3.1.8.

15.1.3 Miscellaneous Signals

Miscellaneous: COMP[1:0], THERMDA, THERMDC	
Recommendation	**Reason/Impact/Documentation**
COMP[1:0] • Terminate to ground through a 51 Ω ± 1% resistor as close as possible to the pin. • Do not wire COMP pins together. Connect each pin to its own termination resistor. • RCOMP value can be adjusted to set external drive strength of I/O and to control the edge rate. • Minimize the distance from terminating resistor	Refer to Section 4.3.1.9
THERMDA, THERMDC • 10-mils wide by 10-mil spacing • Remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4.0 inches to 8.0 inches away as long as the worst noise sources such as clock generators, data, buses and address buses, etc are avoided • Route in parallel and close together with ground guards enclosed	Refer to Section 4.3.1.10.
TESTHI Pins • The TESTHI pins should be tied to the VCC_CPU via a matched resistor that has a resistance value within ± 20% of the impedance of the board transmission line traces.	Refer to Section 4.3.1.11.
Reserved Pins • Leave as No Connects	

15.1.4 VREF and Filtering

Recommendation	Reason/Impact/Documentation
Processor GTLREF • The processor must have one dedicated voltage divider • Keep the voltage divider within 1.5 inch of the GTLREF pin • Keep signal routing at least 10 mils separated from the GTLREF routes. Use a minimum of a 7-mil trace for routing • Do not allow signal lines to use the GTLREF routing as part of their return path **GTLREF Decoupling:** • Decouple voltage divider with a 1 µF capacitor • Decouple pin with a high-frequency capacitor (such as a 220 pF 603) • Place cap as close to pin as possible	Refer to Section 4.1.1.
VCCA, VCCIOPLL, and VSSA Filtering for Processor • Use shielded type inductors • Minimize the distance between VCCA, VSSA pins and capacitors • VCCA should be routed parallel and next to VSSA route • Filter capacitors and inductors should be routed next to each other	Refer to Section 4.7.2.1.
(G)MCH HVREF • 12mils wide, 3.0 inches max length • 10-mil group spacing • Place 0.1 µF decoupling capacitor at the (G)MCH • Minimize the distance between the voltage divider, decoupling capacitors and (G)MCH	Refer to Section 4.1.2.
(G)MCH HSWNG • Trace to voltage divider 12-mils wide, 3.0 inches max length • 10-mil group spacing • Place 0.01 µF decoupling capacitor at the (G)MCH • Minimize the distance between the voltage divider, decoupling capacitors and (G)MCH	Refer to Section 4.1.2.
(G)MCH HRCOMP • Trace to each resistor 10-mils wide, 0.5 inch max length • 7-mil group spacing • Minimize the distance between HRCOMP and the (G)MCH	Refer to Section 4.1.2.

15.1.5 Voltage Regulator Decoupling

15.1.5.1 Four-Phase Voltage Regulator Decoupling Example

Recommendation	Reason/Impact/Documentation
VCC_CPU Decoupling. Recommended Bulk and High-Frequency Decoupling devices: • (9) OSCONs*, 560 µF caps — ESR 9.28 mΩ, max — ESL 6.4 nH, max — Ripple Current Rating 4.080 A • (38) 1206 package, 10 µF caps — ESR 3.5m, typ — ESL 1.15 nH, typ • The decoupling should be placed as close as possible to the processor power pins	Refer to Table 4-15

15.1.5.2 Three-Phase Voltage Regulator Decoupling Example

Recommendation	Reason/Impact/Documentation
VCC_CPU Decoupling. Recommended Bulk and High-Frequency Decoupling devices: • (10) OSCONs*, 560 µF caps — ESR 9.28 mΩ, max — ESL 6.4 nH, max — Ripple Current Rating 4.080 A • (3) Al Electrolytic, 3300 µF — ESR 12 mΩ — ESL 5 nH • (24) 0805 package, 10 µF caps • (14) 1206 package, 10 µF caps — ESR 3.5m , typ — ESL 1.15 nH, typ • The decoupling should be placed as close as possible to the processor power pins • If (38) 1206s are used, place 14 north, 10 inside, and 14 south of the socket.	Refer to Table 4-16

15.2 System Memory (DDR)

15.2.1 DDR-SDRAM

Data Signals: SDQ_[63:0], SDM_[7:0], SDQS_[7:0]	
Recommendation	**Reason/Impact/Documentation**
• Daisy Chain Topology	Refer to Section 5.2.1.
• Resistor packs for Data signals are not shared with any other signal groups	
• Ground Referenced	To provide an optimal current return path. The ground flood should be solid and continuous from the (G)MCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel. Refer to Section 5.2.1.
• Data and strobe signals should be routed entirely on the top signal layer	The (G)MCH pinout has been optimized to breakout all data and strobe signals on the top signal layer. Refer to Section 5.2.1.
• 5-mils wide	Refer to Section 5.2.1.
Trace Spacing • 15-mil spacing SDQS to SDQ/SDM • 10-mil spacing SDQ/SDM to SDQ/SDM • 7-mil min spacing within DIMM Pin Field • 12-mil spacing from DIMM to DIMM • 7-mil min spacing from second DIMM to Rtt	Refer to Section 5.2.1.
• 20-mil min Isolation Spacing from Non-DDR Related Signals	Refer to Section 5.2.1.
Breakout guideline: • 5-mils wide by 6-mil spacing for a max of 350 mils • This breakout spacing should be minimized	Refer to Section 5.2.1.
• 5.8” max total trace length from (G)MCH signal Pad to First DIMM Pin	Refer to Section 5.2.7. Max value includes package length.
• 500-mils max trace length from series termination resistor (10 Ω ± 5%) pad to first DIMM pin	Refer to Section 5.2.1.
• 400-mils to 600-mils trace length from DIMM pin to DIMM pin	Refer to Section 5.2.1.
• 800-mils max trace length from last DIMM pin to parallel termination resistor (56 Ω ± 5%) pad	Refer to Section 5.2.1.
• 0 vias max (all signals are routed on the top layer)	

Data Signals: SDQ_[63:0], SDM_[7:0], SDQS_[7:0]	
Recommendation	**Reason/Impact/Documentation**
Required length matching: • SDQ_[63:0] / SDM_[7:0] to associated SDQS_[7:0] • SDQS_[7:0] to SCMD_CLK/SCMDCLK_[5:0]# for corresponding DIMM	Refer to Section 5.2.1.1.1 and 5.2.1.1.2.

Control Signals: SCKE_[3:0], SCS_[3:0]#	
Recommendation	**Reason/Impact/Documentation**
• Point-to-Point Topology	Refer to Section 5.2.2.
• Ground Referenced	To provide an optimal current return path. The ground flood should be solid and continuous from the (G)MCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel. Refer to Section 5.2.2.
• Control signals should be routed on the bottom signal layer or until they transition to the top signal layer, within 500 mils before the first DIMM connector. • Control signals need to be routed on the same layer	The (G)MCH pinout has been optimized to breakout the control signals onto the bottom signal layer. Refer to Section 5.2.2.
• Control signals should be as short as possible	Because the control signals are routed on the bottom signal layer, the 2.5 V copper flooding on the bottom layer is reduced. This flooding should be maximized for better 2.5 V power delivery to the (G)MCH and DIMMs. Refer to Section 5.2.2.
• Resistor packs for Control signals must not be shared with any other signal groups.	
• 5-mils wide	Refer to Section 5.2.2.
Trace Spacing • 12-mil spacing from (G)MCH to first DIMM • 7-mil min spacing within DIMM Pin Field • 12-mil spacing from DIMM to DIMM • 7-mil min spacing from second DIMM to Rtt	Refer to Section 5.2.2.
• 20-mil min Isolation Spacing from Non-DDR Related Signals	Refer to Section 5.2.2.
• 7-mil minimum Isolation Spacing from the 2.5 V Copper Flood on Layer Four	Refer to Section 5.2.2.

Control Signals: SCKE_[3:0], SCS_[3:0]#	
Recommendation	**Reason/Impact/Documentation**
Breakout Guidelines • 5-mils wide with 6-mils spacing for a max of 350 mils • Breakout spacing should be minimized	Refer to Section 5.2.2.1.
• 3.5 inch max from (G)MCH signal ball to DIMM Pins on first DIMM (SCS#/SCKE_[1:0]) • 50 mil max from (G)MCH signal ball to first DIMM • 500 mil max from second Via to first DIMM	Refer to Section 5.2.2.
• 4.0 inches max from (G)MCH signal ball to DIMM Pins on second DIMM (SCS#/SCKE_[3:2]) — 50 mil max from (G)MCH signal ball to first DIMM — 1” max from second Via to second DIMM	Refer to Section 5.2.2.
• 1.4” max from DIMM pins on first DIMM to Rtt (56 Ω ± 5%) Pad (SCS#/SCKE_[1:0])	Refer to Section 5.2.2.
• 800-mils max from DIMM pins on second DIMM to Rtt Pad (56 Ω ±5%)	Refer to Section 5.2.2.
• 4 via max (minimize number of vias over 2)	
Length Tuning Method • SCS#/SCKE_[3:0] TO SCMDCLK_[5:0]/SCMDCLK_[5:0]#	Refer to Section 5.2.2.1.

Address/Command Signals: SMAA_[12:6,3,0], SBA_[1:0], SRAS#, SCAS#, SWE#	
Recommendation	**Reason/Impact/Documentation**
• Daisy Chain Topology	Refer to Section 5.2.3.
• Ground Referenced	To provide an optimal current return path. The ground flood should be solid and continuous from the (G)MCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel. Refer to Section 5.2.3.
• Address/Command signals are routed on the bottom signal layer • All Address/Command need to be routed on the same layer	The (G)MCH pinout has been optimized to breakout the address/ command signals onto the bottom signal layer. Refer to Section 5.2.3.

Address/Command Signals: SMAA_[12:6,3,0], SBA_[1:0], SRAS#, SCAS#, SWE#	
Recommendation	**Reason/Impact/Documentation**
• Address/Command signals should be as short as possible	Because the control signals are routed on the bottom signal layer, the 2.5 V copper flooding on the bottom layer is reduced. This flooding should be maximized for better 2.5 V power delivery to the (G)MCH and DIMMs. Refer to Section 5.2.3.
• Resistor packs for Address/Command signals are not shared with any other signal groups.	
• 5-mils wide	Refer to Section 5.2.3.
Trace Spacing • 12-mil spacing from (G)MCH to first DIMM • 7-mil min spacing within DIMM Pin Field • 12-mil spacing from DIMM to DIMM • 7-mil min spacing from second DIMM to Rtt	Refer to Section 5.2.3.
• 20 mil minimum Isolation Spacing from Non-DDR Related Signals	Refer to Section 5.2.3.
• 7-mil min Isolation Spacing from the 2.5 V Copper Flood on Layer Four	Refer to Section 5.2.3.
Breakout Guideline • 5-mils wide with 6-mil spacing for a max of 350 mils. • This breakout spacing should be minimized.	Refer to Section 5.2.3.
• 4.0 inches max from (G)MCH signal ball to first DIMM pin • 50 mil max from (G)MCH signal ball to first via	Refer to Section 5.2.3.
• 400 mils to 600 mils from DIMM pin to DIMM pin	Refer to Section 5.2.3.
• 800 mils max from Last DIMM Pin to Parallel Termination Resistor (56Ω ± 5%) Pad	Refer to Section 5.2.3.
• 4 vias max (Minimize number of vias over 2)	
Length Tuning Required • SMAA_[12:6,3,0], SBA_[1:0], SRAS#, SCAS#, SWE# to SCMDCLK_[5:0]/SCMDCLK_[5:0]# for corresponding DIMM.	Refer to Section 5.2.3.1.

CPC Address Signals: SMAA_[5,4,2,1] and SMAB_[5,4,2,1]	
Recommendation	**Reason/Impact/Documentation**
• Point-to-Point Topology	Refer to Section 5.2.4.
• Ground Referenced	To provide an optimal current return path. The ground flood should be solid and continuous from the (G)MCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel. Refer to Section 5.2.4.
• Resistor packs for CPC Address signals are not shared with any other signal groups.	
• CPC Address signals are routed on the bottom signal layer • All CPC Address signals need to be routed on the same layer	The (G)MCH pinout has been optimized to breakout the CPC Address signals onto the bottom signal layer. Refer to Section 5.2.4.
• 5-mils wide SMAA_[5,4,2,1] to first DIMM	Refer to Section 5.2.4.
• 5-mils wide SMAB_[5,4,2,1] to second DIMM	Refer to Section 5.2.4.
Trace Spacing • 12-mil spacing from (G)MCH to DIMM • 8-mil min spacing within DIMM Pin Field • 8-mil min spacing from DIMM to Rtt	Refer to Section 5.2.4.
• 20-mil minimum Isolation Spacing from Non-DDR Related Signals • Max of 1 Address/Command signal can be routed next to a CPC signal.	Refer to Section 5.2.4.
• 7-mil min Isolation Spacing from the 2.5 V Copper Flood on Layer Four	Refer to Section 5.2.4.
Breakout Guideline • 5-mils wide with 6-mil spacing for up to the first 200 mils from ball • 5-mils wide with 8-mil spacing for up to an additional 550 mils after the first 200 mils from the ball • Use of breakout spacing should be minimized	Refer to Section 5.2.4.
• 2.5 inch max from (G)MCH signal ball to first DIMM (SMAA_[5,4,2,1]) • 50 mil max from (G)MCH signal ball to first via	Refer to Section 5.2.4.
• 3.0 inches max from (G)MCH signal ball to second DIMM (SMAB_[5,4,2,1]) • 50 mil max from (G)MCH signal ball to first via	Refer to Section 5.2.4.
• 1.4” max from first DIMM pin to Parallel Termination resistor (33 Ω ± 5%) pad (SMAA_[5,4,2,1])	Refer to Section 5.2.4.

CPC Address Signals: SMAA_[5,4,2,1] and SMAB_[5,4,2,1]	
Recommendation	**Reason/Impact/Documentation**
• 800 mils max from second DIMM Pin to Parallel Termination Resistor (33Ω ± 5%) Pad (SMAB_[5,4,2,1])	Refer to Section 5.2.4.
• 4 vias max (minimize number of vias over 2)	
• Termination Resistor (Rtt) 33 Ω ± 5%	
Length Tuning Required • SMAA_[5,4,2,1], SMAB_[5,4,2,1] to SCMDCLK_[5:0]/ SCMDCLK_[5:0]# for corresponding DIMM	Refer to Section 5.2.4.1.

Clock Signals: SCMDCLK_[5:0], SCMDCLK_[5:0]#	
Recommendation	**Reason/Impact/Documentation**
• Point-to-Point Topology	Refer to Section 5.2.5.
• Ground Referenced	To provide an optimal current return path. The ground flood should be solid and continuous from the (G)MCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel. Refer to Section 5.2.5.
• Clock signals should be routed on the bottom signal layer	The (G)MCH pinout has been optimized to breakout the CPC Address signals onto the bottom signal layer. Refer to Section 5.2.5.
• All different clocks must be routed on the same layer.	
• Differential clock pairs must be routed differentially from the (G)MCH to their associated DIMM pins and must maintain the correct isolation spacing from other signals.	Refer to Section 5.2.5.
• Clocks must remain isolation spacing from itself during serpentines.	Refer to Section 5.2.5.
• 8-mils wide	Refer to Section 5.2.5.
• 5-mil Differential Trace Spacing between SCMDCLK and its corresponding SCMDCLK#	Refer to Section 5.2.5.
• Isolation spacing from another DDR signal group = 20 mils • Isolation spacing form non-DDR related signals = 20 mils	Refer to Section 5.2.5.
• 10-mil minimum Isolation Spacing from the 2.5 V Copper Flood on Layer Four	Refer to Section 5.2.5.
• 20-mil min spacing from itself when serpentining	Refer to Section 5.2.5.

Clock Signals: SCMDCLK_[5:0], SCMDCLK_[5:0]#	
Recommendation	**Reason/Impact/Documentation**
Breakout Guideline • 5-mils wide with 5-mils differential spacing with a minimum of 5-mils isolation spacing from another signal for a max of 350 mils.	Refer to Section 5.2.5.
• Total trace length of 7.4” max from (G)MCH signal pad to first DIMM (SCMDCLK_[2:0]) • 50-mils max length from (G)MCH signal ball to via	Refer to DG Section 5.2.5. See Section 5.2.7 for package length
• Total trace length of 7.9” max from (G)MCH signal pad to second DIMM (SCMDCLK_[5:3]) • 50-mils max length from (G)MCH signal ball to via	Refer to DG Section 5.2.5. See Section 5.2.7 for package length
Total Clock length relationship between first DIMM and second DIMM: • (P+Y) = ((P+X)+0.5 inch) • (P+X) = Total target clock length to first DIMM • (P+Y) = Total target clock length to second DIMM	
• 1 via max (for breakout to bottom layer)	
• System memory signal lengths must be tuned to the total target length of the clock pairs SCMDSCK/SCMDCLK#.	
Length Tuning Required • SCMD_CLK length to SCMD_CLK# length, within ± 10 mils • All 3 clock pairs to each DIMM are equal in length, within ± 10 mils where length includes package length compensation (P + A)	Refer to DG Section 5.2.5.1

Feedback Signals: SRCVEN_OUT#, SRCVEN_IN#	
Recommendation	**Reason/Impact/Documentation**
• Point-to-Point Topology with resistor site (unpopulated)	Refer to Section 5.2.6.
• Ground Referenced	Refer to Section 5.2.6.
• 5-mils wide	Refer to Section 5.2.6.
• 10-mil minimum Isolation Spacing from another DDR Signal Group or from Non-DDR Related Signals	
• 100-mils max from (G)MCH SRCVEN_OUT# to series resistor	Refer to Section 5.2.6.
• 100 mils max from series resistor to (G)MCH SRCVEN_IN#	Refer to Section 5.2.6.
• 2 vias max	

15.2.2 DDR-SDRAM Decoupling, Compensation, and VREF

Recommendation	Reason/Impact/Documentation
System Memory Bypass Caps • Place nine, evenly-spaced 0.1 µF 0603 capacitors between the DIMMs • A wide trace should connect to a via that transitions to the ground cutout on layer two and to the ground plane on layer three. • The ground via should be placed as close to the ground pad as possible. • A wide trace should connect the 2.5 V side of the cap to a via that transitions to the 2.5 V plane on layer four and then to the closest 2.5 V DIMM pin on either DIMM • The 2.5 V traces should be distributed evenly between the two DIMMs • The 2.5 V via should be placed as close to the 2.5 V pad as possible	Helps minimize return path discontinuities Refer to Section 5.3.
2.5 V Power Delivery Guidelines	Refer to Section 5.4.1.
(G)MCH System Memory High-Frequency Decoupling • Place eight, 0.1 µF 0603 caps within 100 mils of the (G)MCH package • Caps must be placed perpendicular to the (G)MCH, when appropriate, with the 2.5 V side of the caps facing the (G)MCH. • The trace from the power end of the cap should be as wide as possible and it must connect to a 2.5 V power ball on the outer row of balls on the (G)MCH. • Each capacitor should have two vias placed directly over a 2.5 V copper finger that is located on layer four. • One via should be placed within 25 mils of the cap pad, while the other via should be placed within 25 mils of the power ball. If the trace from the solder ball to the capacitor is less than 100 mils, one of the vias may be omitted. • The cap ground end must connect to the ground cutout on layer two and to the ground plane on layer three through a via that is placed within 25 mils of the cap pad. • The trace from the ground via to the cap pad must be as wide as possible.	Refer to Section 5.4.2.1.
(G)MCH System Memory Low-Frequency Bulk Decoupling • Place four, 100 µF electrolytic evenly between the (G)MCH and the first DIMM connector. • Place one, 22 µF cap between the (G)MCH and the first DIMM connector on the top layer copper flood • Power end of caps must connect to the 2.5 V on layer one or layer four. • Ground end of caps must connect to ground on layer two and three.	Refer to Section 5.4.2.1.

Recommendation	Reason/Impact/Documentation
DDR DIMM Decoupling • Place three, 100 µF caps • One placed at the upper left, one at the bottom left, and one at the bottom right of the DIMM connectors • Power end of caps must connect to the 2.5 V on layer one and layer four. • Ground end of caps must connect to ground on layer two and three.	Refer to Section 5.4.3
DDR VREF • Place VREF divider within 1.0 inch from the DIMMs (Two identical resistors 50 Ω – 150 Ω, 1%) • Place 0.1 µF decoupling cap at the (G)MCH and one 0.1 µF cap at each of the DIMM sockets • 12-mils wide min • 12-mil group spacing • Breakout: 7-mil spacing, 350 mils max.	Refer to Section 5.4.4
DDR SMRCOMP • RCOMP Resistors – 60.4 Ω ± 1% pulled to DDR 2.5 V, and 60.4 Ω ± 1% tied to ground • 12-mils wide minimum • 10-mil group spacing	Refer to Figure 5-46
DDR VTT Termination • All DDR signals, except the command clocks, must be terminated to 1.25 V (VTT) using 5% resistors at the end of the channel opposite the (G)MCH. • Place a solid 1.25 V (VTT) termination island on the top signal layer, just beyond the last DIMM connector. The VTT Termination Island must be at least 50-mils wide. • Use this termination island to terminate all DDR signals, using one resistor per signal. Resistor packs are acceptable, with the understanding that the signals within an RPACK must be from the same DDR signal group. • Termination resistor packs for each group must remain dedicated to that group, and not be shared with any other signal groups. • No mixing of signals from different DDR signal groups is allowed within an RPACK. The parallel termination resistors connect directly to the VTT Island on the top signal layer.	Refer to Section 5.4.6.

15.3 AGP

15.3.1 1X Signals

1X Signals: CLK(3.3 V), GRBF#, GWBF#, GST_[2:0], GPIPE#, GREQ#, GGNT#, GPAR/ADD_DETECT, GFRAME#, GIRDY#, GTRDY#, GSTOP#, GDEVSEL#	
1X Timing Domain Routing Recommendation	**Reason/Impact/Documentation**
• 6” max trace length	Refer to Section 6.2.1.
• 5-mils wide with 7-mil trace separation.	Refer to Section 6.2.1.
• GIRDY# and GDEVSEL# should be matched (± 250 mils) • GTRDY# with GFRAME# should be matched (± 250 mils) • GSTOP# with GAD_15 should be matched (± 250 mils)	Refer to Section 6.2.1.

15.3.2 2X/4X Signals

2X/4X Signals: GAD_[15:0], GC/BE_[1:0]#, GADSTB_0, GADSTB_1#, GAD_[31:16], GC/BE_[3:2]#, GADSTB_1, GADSTB_1#, GSBA_[7:0], GSB_STB, GSB_STB1#	
2X/4X Timing Domain Routing Recommendation	**Reason/Impact/Documentation**
• 6” max trace length	Refer to Section 6.2.2.
• 1:3 trace width-to-spacing	Refer to Section 6.2.2.
• Breakout Guidelines: 5-mil spacing, 0.3” max length	Refer to Section 6.2.2.
• Strobes should match their complement to ± 50 mils	Refer to Section 6.2.2.
• Data to Strobe length mismatch ±0.125” from (G)MCH pad to AGP pin	Refer to Section 6.2.2 and Table 6-4.
• GADSTB_0 should match GADSTB_1 to ± 0.125”	Refer to Section 6.2.2.

15.3.3 AGP 1X and 2X/4X Common Routing

Recommendation	Reason/Impact/Documentation
• Trace length mismatch for all signals within a signal group should be as close to zero as possible	To provide timing margin Refer to Table 6-4
• Separate the traces as much as possible	Reduce trace-to-trace coupling Refer to Table 6-4
• Data and associated strobe signals must not be routed on a separate layer for more than 3”.	Refer to Table 6-4
• These guidelines apply to board stack-ups with 15% impedance tolerance.	Refer to Table 6-4

15.3.4 AGP Clock Routing, Decoupling, VREF

Recommendation	Reason/Impact/Documentation
Clock • Max 1 ns clock skew for all data transfer modes between the (G)MCH and the graphic component.	Refer to Section 6.2.4.
Decoupling • (5) 0.1 µF capacitors required • Must be as close as possible to the (G)MCH, within 100 mils of the (G)MCH outer row of balls. • AGP signal trace spacing may be reduced as the traces go around each cap. This space reduction should be minimal and for as short a distance as possible. • Evenly distribute placement of decoupling caps in the AGP interface signal field. • Use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dieletric. • Place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another.	Refer to Section 6.2.5 and 6.2.5.1.
AGP Connector Decoupling • VCC3_3: three, 0.01 µF or larger, low ESL caps. Place as close as possible to a VCC3_3 pair of pins on the connector • VDDQ: six, 0.01 µF or larger, low ESL caps. Place as close as possible to a VDDQ pair of pins on the connector • +5 V: one, 0.01 µF or larger, low ESL cap placed as close as possible to the +5 V connector pins • +12 V: one, 0.01 µF or larger, low ESL cap placed as close as possible to the +12 V connector pins • 3.3VAUX: one, 0.01 µF or larger, low ESL cap placed as close as possible to the 3.3 VAUX connector pin(s)	To address AC signaling issues. Refer to Section 6.2.5.1.
AGP VREF • Voltage divider with 1k 1% to produce 0.75 V – connected to both AGP_ref on (G)MCH and VREFCG on AGP connector. 0.1 µF Cap on net at both AGP connector and (G)MCH.	Refer to Section 6.3.1.
AGP RCOMP • 0.5 inch max length • 40 Ω ± 1% down to ground	Refer to Section 6.4.1.

15.4 Analog Display Port (Intel® 845PE chipset only)

15.4.1 Analog RGB/CRT

Recommendation	Reason/Impact/Documentation
• RED, GREEN, BLUE and RED#, GREEN#, BLUE# should be tied directly to ground.	Refer to Section 7.1
• VCCA_DPLL, VCCA_DAC, and VSSA_DAC should be tied directly to ground	Refer to Section 7.1
• REFSET and DREFCLK should be tied directly to ground	Refer to Section 7.1
• DDCA_DATA and DDCA_CLK should be tied directly to ground	Refer to Section 7.1
• HYSNC and VSYNC should be left as no connect	Refer to Section 7.1

15.5 Analog Display Port (Intel® 845GE chipset only)

15.5.1 Analog RGB/CRT

Recommendation	Reason/Impact/Documentation
• RED, GREEN, BLUE and RED#, GREEN#, BLUE# should be routed differentially	Refer to Section 7.2.3.
• 10-mil width-with 5-mil spacing (Targeting 75 Ω odd mode differential impedance)	Refer to Section 7.2.3.
• 20-mil group spacing	Refer to Section 7.2.3.
• Each analog signal should be matched to its complement as closely as possible.	Refer to Section 7.2.3.
• RGB signals should be length matched as closely as possible from the (G)MCH to the VGA connector within ± 200 mils	Refer to Section 7.2.3.
• Terminate Rs (75 Ω for RED, GREEN, BLUE; 37.5 Ω for RED#, GREEN#, BLUE#) close to each other and the VGA connector.	Refer to Section 7.2.3.

15.6 Hub Interface

15.6.1 Interface Signals

Recommendation	Reason/Impact/Documentation
• It is recommended that all signals be referenced to VSS.	Refer to Section 8.
• The trace impedance must equal 60 Ω ± 15%.	Refer to Section 8.1.
HI Strobe Signal: HI_STBS, HI_STBF	
• Strobe signals need to be routed 5-mils wide with 15-mil spacing	Refer to Section 8.1.1.
• Strobe pair should have a minimum of 20 mils spacing from any adjacent signals.	Refer to Section 8.1.1.
• 2” to 8” max trace length	Refer to Section 8.1.1.
• Strobe length mismatch ± 100 mils max	Refer to Section 8.1.1.
• For breakout, strobe signals can be routed to 5 on 5 within 300 mils of the package	Refer to Section 8.1.1.
HI Data Signals: HI_[10:0]	
• Data signals need to be routed 5-mils wide with 15 mils spacing	Refer to DG Section 8.1.2.
• Data signals must be matched within ± 100 mils of the HI_STBF/ HI_STBS differential pair	Refer to DG Section 8.1.2.
• For breakout, data signals can be routed to 5 on 5 within 300 mils of the package	Refer to DG Section 8.1.2.
• 2” to 8” max trace length	Refer to DG Section 8.1.2.

15.6.2 Hub Interface Decoupling, Compensation, and VREF

Recommendation	Reason/Impact/Documentation
HI_REF/HI_SWING generation circuit • Should be placed no more than 4" away from (G)MCH or ICH4. • If more than 4" is needed, locally generated divider should be used. • Place (2) 0.1 µF caps close to the divider • Place the 0.01 µF bypass caps within 0.25" of the component's pin (HI_REF/VREF/HI_SWING).	Refer to Section 8.1.4.
HICOMP • Trace must be as short as possible.	Refer to Section 8.1.5.
VCCHI1_5 Decoupling • Decouple each component, the (G)MCH and the ICH4, with two 0.1µF capacitors within 100 mils from each package. • Capacitors should be adjacent to hub interface rows	Refer to DG Section 8.1.6.

15.7 Intel® ICH4

15.7.1 IDE Interface

Recommendation	Reason/Impact/Documentation
• 5-mil wide and 7 mil	Refer to Section 9.1.
• 8.0 inches max trace length from ICH4 to IDE connector	Refer to Section 9.1.
• The Maximum length difference between the data and strobe lengths is 0.5 inch.	Refer to Section 9.1.

15.7.2 AC '97

Recommendation	Reason/Impact/Documentation
• Trace impedance Z_O AC97 = 60 Ω ± 15%	Refer to Section 9.2.
• 5 mil trace wide, 5-mil spacing	Refer to Section 9.2.
• 14" max length from ICH4 to Codec/CNR connector • 6" max length from primary codec and CNR	Refer to Section 9.2.
AC_SDIN Max Trace Length ICH4 to: • Primary Codec: L = 14 inches • From Primary Codec T junction to: CNR: L = 6 inches • CNR: L = 14 inches.	

Recommendation	Reason/Impact/Documentation
AC_SDOUT Max trace length ICH4 to: Primary Codec: L = 14 inches CNR: L = 14 inches.	
AC_BIT_CLK Max trace length ICH4 to: Primary Codec: L = 13.6 inches CNR: L = 13.6 inches.	
Series termination resistor on AC_BIT_CLK line should be no more than 0.9 to 7.6 inches from the ICH4	
Series termination resistors on AC_SDIN lines if needed should be no more than 100 to 400 mils from the CNR card or the on board codec.	

15.7.3 USB 2.0

Recommendation	Reason/Impact/Documentation
• 7.5-mils wide, 7.5-mil spacing	Refer to Section 9.4.1.2.
• 20 mil min spacing between USB signal pair and other traces	This helps to minimize crosstalk. Refer to Section 9.4.1.2.
• 150 mil max trace length mismatch between USB signal pair	Refer to Section 9.4.1.5.
• With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first	Refer to Section 9.4.1.1.
• Route USB signals ground referenced.	Refer to Section 9.4.1.1.
• Route USB signals using a minimum of vias and corners	This reduces signal reflections and impedance changes. Refer to Section 9.4.1.1.
• When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn.	This reduces reflections on the signal by minimizing impedance discontinuities Refer to Section 9.4.1.1.
• Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.	Refer to Section 9.4.1.1.
• Stubs on USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs on a given data line should not be greater than 200 mils.	Refer to Section 9.4.1.1.

Recommendation	Reason/Impact/Documentation
• Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.)	Refer to Section 9.4.1.1.
• Keep USB signals clear of the core logic set.	High current transients are produced during internal state transitions, which can be very difficult to filter out. Refer to Section 9.4.1.1.
• Keep traces at least 50 mils away from the edge of the plane (VCC or GND depending on which plane to which the trace is routed)	Helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB. Refer to Section 9.4.1.1.
• Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance.	Refer to Section 9.4.1.2.
• Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines. The minimum recommended spacing to clock signals is 20 mils	Minimize crosstalk Refer to Section 9.4.1.2.
• Use 20 mils minimum spacing between USB signal pairs and other signal traces.	This helps to prevent crosstalk.
• USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pair (such as DM1 and DP1) should be no greater than 150 mils.	Refer to Section 9.4.1.5.
• No termination resistors needed for USB.	
• USBRBIAS (ball A23) and USBRBIAS# (ball B23) should be routed 5 on 5 with a single trace 500 mils or less to the 22.6 Ω 1% resistor to ground.	
• 17” max trace length from ICH4 to the backpanel. • 8” max trace length from ICH4 to CNR connector. • Refer to Table 9-9 for front panel trace lengths.	

15.7.4 PCI Guidelines

Recommendation	Reason/Impact/Documentation
• Data Lines – See specific topology guidelines	Refer to Table 9-13
• Clock Lines	Refer to Table 9-14
• IDSEL	See related figure in ICH4 PCI section

15.7.5 RTC

Recommendation	Reason/Impact/Documentation
• 5 mil trace width (results in ~2 pF per inch)	
• 1” max trace length to crystal	
• RTC LEAD length ≤ 1.0 inches Max	
• Minimize capacitance between RTCX1 and RTCX2	
• Put GND plane underneath Crystal components	
• Don’t route switching signals under the external components (unless on other side of board)	
• If SUSCLK is not used in the platform it should be routed to a testpoint.	The ability to probe this signal can decrease the resolution time for RTC related issues

15.7.6 Platform LAN Connect Interface

Recommendation	Reason/Impact/Documentation
• 5-mils wide, 10-mil spacing	
• LOM to PLC • 0.5 inch to 7.5 inches max trace length (A) from ICH4 to RPAK • 4" to (11.5 – A)" from RPAK to PLC • LOM to CNR • 0.5 inch to 7.5" max trace length (A) from ICH4 to RPAK • 1.5 inches to (9 – A)" max trace length from ICH4 to CNR • (0.5 inch to 3" on card)	To meet timing requirements. Refer to Section 9.9.2.1.2.
• Stubs due to R-pak CNR/LOM stuffing option should not be present.	To minimize inductance.
Point-to- Point Single Solution Maximum Trace Lengths: ICH4 to: 82562EZ/ET/EX/EM: L = 4.5 to 12 inches CNR: L = 2 to 9.5 inches	To meet timing requirements. Refer to Section 9.9.2.1.1.
• Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inch (clock must be longest trace)	To meet timing and signal quality requirements. Refer to Section 9.9.2.2.
• Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN PHY.	To meet timing and signal quality requirements. Refer to Section 9.10.1.1.
• Keep the total length of each differential pair under 4 inches. • (Preferably less than 2 inches)	Issues found with traces longer than 4 inches: IEEE phy conformance failures, excessive EMI and or degraded receive BER. Refer to Section 9.10.1.1
• Do not route the transmit differential traces closer than 100 mils to the receive differential traces.	To minimize crosstalk. Refer to Section 9.10.1.1
• Signal traces and differential traces not route in parallel and closer than 100mil (300 mils recommended)	To minimize crosstalk. Refer to Section 9.10.1.1
• Route 5 mils on 10 mils for differential pairs (out of LAN phy)	To meet timing and signal quality requirements.
• Differential trace impedance should be controlled to be ~100 Ω .	To meet timing and signal quality requirements. Refer to Section 9.10.1.1.1.

Recommendation	Reason/Impact/Documentation
• For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, it is recommended to use two 45-degree bends.	To meet timing and signal quality requirements. Refer to Section 9.10.1.1.
• Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards. Refer to Section 9.10.1.1.
• Do not route traces and vias under crystals or oscillators.	This will prevent coupling to or from the clock. Refer to Section 9.10.1.1.
• Trace width to height ratio above the ground plane ratio is between 1:1 and 3:1.	To control trace EMI radiation. Refer to Section 9.10.1.1.1.
• Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors. Refer to Section 9.10.1.1.1.
• Vias to decoupling capacitors should be sufficiently large in diameter.	To decrease series inductance. Refer to Section 9.10.1.1.1.
• Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.	To minimize crosstalk. Refer to Section 9.10.1.1.2.
• Isolate I/O signals from high-speed signals.	To minimize crosstalk. Refer to Section 9.10.1.1.2.
• Place the 82562EZ/ET/EX/EM part more than 1.5 inches away from any board edge.	This minimizes the potential for EMI radiation problems.
• Place at least one bulk capacitor (4.7 µF or greater OK) on each side of the 82562EZ/ET/EX/EM.	Research and development has shown that this is a robust design recommendation.
• Place decoupling caps (0.1 µF) as close to 82562EZ/ET/EX/EM as possible.	
• Design and Layout Guidelines for the 82540EM and 1000BASE-T Designs	Refer to DG Section 9.10.2

15.8 FWH Decoupling

Recommendation	Reason/Impact/Documentation
• 0.1 µF capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins.	
• 4.7 µF capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins.	

15.9 Platform Clocks

15.9.1 Host Clock (CPU#, CPU)

Recommendation	Reason/Impact/Documentation
• Ground referenced	Refer to Section 12.2.1.
• 7-mils wide with 8 mil differential pair spacing	Refer to Section 12.2.1.
• Spacing to other traces should be 3 to 4 times greater than distance from BCLK1 to BCKL0	Refer to Section 12.2.1.
• Processor routing length- Clock driver to Rs should be 0.5 inch max	Minimize the impact on skew and impedance variation Refer to Section 12.2.1.
• Processor routing length- Rs to Rs-Rt should be 0 inch to 0.2 inch	Minimize the impact on skew and impedance variation Refer to Section 12.2.1.
• Processor routing length- Rs-Rt node to Rt should be 0 inch to 0.2 inch	Minimize the impact on skew and impedance variation Refer to Section 12.2.1.
• Processor routing length- Rs-Rt node to load should be 2” to 12”	Refer to Section 12.2.1.
• (G)MCH routing length- Clock driver to Rs should be 0.5 inch max	Minimize the impact on skew and impedance variation Refer to Section 12.2.1.
• (G)MCH routing length- Rs to Rs-Rt should be 0 inch to 0.2 inch	Minimize the impact on skew and impedance variation Refer to Section 12.2.1.
• (G)MCH routing length- Rs-Rt node to Rt should be 0 inch to 0.2 inch max	Minimize the impact on skew and impedance variation Refer to Section 12.2.1.
• (G)MCH routing length- Rs-Rt node to load should be 2.0 inches to 12” max	Refer to Section 12.2.1.

Recommendation	Reason/Impact/Documentation
• Clock pair to (G)MCH must be 100 mils longer than clock pair to processor socket	Rs values between 20 – 33 Ω have been shown to be effective Refer to Section 12.2.1.
• ±10 mil length matching between BCLK0 to BCLK1	Refer to Section 12.2.1.
• Host clock pairs must be routed differentially and on the same physical routing layer.	Refer to Section 12.2.1.
• Route all agents on the same physical routing layer referenced to ground of the differential clock	Refer to Section 12.2.1.
• Make sure that the skew induced by the vias is compensated in the traces to other agents	Refer to Section 12.2.1.
• Do not place vias between adjacent complementary clock traces	Refer to Section 12.2.1.
• Maintain uniform spacing between the two halves of differential clocks	EMI Constraints. Refer to Section 12.2.1.
• Route clocks on physical layers adjacent to the VSS reference plane only	EMI Constraints. Refer to Section 12.2.1.

15.9.2 DOT_CLK Clock Group (Intel® 845GE chipset only)

Recommendation	Reason/Impact/Documentation
• Point-to-Point Topology	Refer to Section 12.2.2.
• 5-mils wide with 20-mil spacing	Refer to Section 12.2.2.
• 0.0 inch to 0.5 inch max from driver to series termination	Refer to Section 12.2.2.
• 2” to 9” max from series termination to (G)MCH	Refer to Section 12.2.2.

15.9.3 66 MHz Clock Group

Recommendation	Reason/Impact/Documentation
• Point-to-Point Topology	Refer to Section 12.2.3.
• 5-mils wide and 20-mil spacing	Refer to Section 12.2.3.
• 20-mil group spacing	Refer to Section 12.2.3.
• 0.0 inch to 0.5 inch max trace length from clock driver to series termination	Refer to Section 12.2.3.
• 4.0 inches and 8.5” max trace length from series termination to receiver on the motherboard	Refer to Section 12.2.3.
• X Trace length from the clock driver to the (G)MCH	Refer to Section 12.2.3.
• X ± 100 mils max trace length from the clock driver to ICH4	If the trace length from the clock driver to the (G)MCH is X, the trace length from the clock drive to the ICH4 must be X ± 100 Refer to Section 12.2.3.
• Minimal (~0) skew between CLK33 group and CLK66 group	Refer to Sections 12.2.3 and 12.2.5.

15.9.4 AGPCLK (When Routing to an AGP Connector)

Recommendation	Reason/Impact/Documentation
AGPCLK to AGP Connector	
• Point-to-Point Topology	Refer to Section 12.2.4.
• 5-mils wide and 15-mil spacing	Refer to Section 12.2.4.
• 15-mil group spacing	Refer to Section 12.2.4.
• Series termination within 0.5 inch of the driver	Refer to Section 12.2.4.
• The total trace length must be 4.0 inches less than the CLK66 total trace length ± 100mils.	Refer to Section 12.2.4.
AGPCLK to AGP Down	
• Point-to-Point Topology	Refer to Section 12.2.4.
• 5-mils wide and 15-mil spacing	Refer to Section 12.2.4.
• 15-mil group spacing	Refer to Section 12.2.4.
• Series termination within 0.5 inch of the driver	Refer to Section 12.2.4.
• The total trace length must be the CLK66 total trace lengths ± 100 mils.	Refer to Section 12.2.4.

15.9.5 33 MHZ Clock Group

Recommendation	Reason/Impact/Documentation
• Point-to-Point Topology	Refer to Section 12.2.5.
• 5-mils wide and 15-mil spacing	Refer to Section 12.2.5.
• 15-mil group spacing	Refer to Section 12.2.5.
• Series termination within 0.5 inch of the driver	Refer to Section 12.2.5.
• 4.0 inches and 8.5” max trace length from series termination to receiver on the motherboard	Refer to Section 12.2.5.
• The 33 MHz clock to the receiver must be matched to ± 100mils of the CLK66	Refer to Section 12.2.5 and 12.2.3.
• Clocks in 33 MHZ and 66 MHZ clock group should have minimal (~0) skew.	Refer to Section 12.2.5 and 12.2.3.

15.9.6 14 MHz Clock Group

Recommendation	Reason/Impact/Documentation
• Balanced Topology	Refer to Section 12.2.6.
• 5-mils wide and 10 mils spacing	Refer to Section 12.2.6.
• 10-mil group spacing	Refer to Section 12.2.6.
• Series termination within 0.5 inch of the driver	Refer to Section 12.2.6.
• Signal must T within 12” of the series termination	Refer to Section 12.2.6.
• Max trace length of stubs is 6”	Refer to Section 12.2.6.
• Total trace length matched to ± 0.5 inch of each other	Refer to Section 12.2.6.

15.9.7 PCICLK Clock Group

Recommendation	Reason/Impact/Documentation
PCICLK to PCI Device Down	
• Point-to-Point Topology	Refer to Section 12.2.7.
• 5-mils wide and 15 mils spacing	Refer to Section 12.2.7.
• 15-mil group spacing	Refer to Section 12.2.7.
• Series termination within 0.5 inch of the driver	Refer to Section 12.2.7.
• Total trace length matched to CLK33 ± 500 mils	Refer to Section 12.2.7.
PCICLK to Devices on PCI Cards	
• Point-to-Point Topology	Refer to Section 12.2.7.
• 5-mils wide and 15 mils spacing	Refer to Section 12.2.7.
• 15-mil group spacing	Refer to Section 12.2.7.
• Series termination within 0.5 inch of the driver	Refer to Section 12.2.7.
• Length from series resistor to PCI Slot is not specified: It is dependent on total motherboard trace length.	Refer to Section 12.2.7.
• 2.5” from PCI Slot to PCI device.	Refer to Section 12.2.7.
• Total trace length from driver to PCI Connector matched to (CLK33 – 2.5”) ± 500 mils	Refer to Section 12.2.7.

15.9.8 USBCLK

Recommendation	Reason/Impact/Documentation
• Point-to-Point Topology	Refer to Section 12.2.8.
• 5-mils wide	Refer to Section 12.2.8.
• 20-mil group spacing	Refer to Section 12.2.8.
• Series termination within 0.5 inch of the driver	Refer to Section 12.2.8.
• Trace length from series termination to receiver on the motherboard between 3.0 inches and 12”	Refer to Section 12.2.8.

15.9.9 Clock Decoupling (VDDA/VDD Decoupling)

Recommendation	Reason/Impact/Documentation
• Place (1) 10µF Bullk decoupling cap in a 1206 package close to the VDD generation circuitry	Refer to Section 12.3.
• Place (6) 0.1µF caps in a 0603 package close to the VDD pins on the clock driver	Refer to Section 12.3.
• Place (3) 0.01µF high-frequency decoupling caps in 0603 package close to the VDDA pins on the clock driver	Refer to Section 12.3.
• Place (1) 10µF bulk decoupling cap in 1206 package close to the VDDA generation circuitry	Refer to Section 12.3.

15.10 Platform Power

15.10.1 Intel® (G)MCH High-Frequency Decoupling

Recommendation	Reason/Impact/Documentation
VTT_DECAP • (5) 0.1 µF Caps (Edge Cap – VTT) • Edge Caps **must not** have vias in the trace from the cap to the (G)MCH solder ball. They also **must not** connect to the motherboard VTT plane. • Place near balls: AC37, R37, L37, G37, and A31 • Unless otherwise noted, capacitors should be placed less than 100 mils from the package.	Refer to Section 13.2.4.
VTTFSB • (5) 0.1 µF Caps (Decoupling Cap – VTT) • Place within 250 mils of the package within the VTT corridor • Unless otherwise noted, capacitors should be placed less than 100 mils from the package.	Refer to Section 13.2.4.
VCC • (1) 0.1 µF Caps (Decoupling Cap – VCC) • Place within 100 mils of the package in or near the VCC corridor • Unless otherwise noted, capacitors should be placed less than 100 mils from the package.	Refer to Section 13.2.4.
VCCAGP • (5) 0.1 µF Caps (Decoupling Cap – VSS) • Place near balls: A5, E1, J1, N1, and U1 • Unless otherwise noted, capacitors should be placed less than 100 mils from the package.	Refer to Section 13.2.4.

Recommendation	Reason/Impact/Documentation
VCCHI • (2) 0.1 µF Caps (Decoupling Cap – VSS) • Place near balls: AA1 and AE1 • Unless otherwise noted, capacitors should be placed less than 100 mils from the package.	Refer to Section 13.2.4.
VCCSM • (8) 0.1 µF Caps (Decoupling Cap – VCC) • Place near balls: AL37, AU5, AU9, AU13, AU17, AU25, AU29, and AU33 • Unless otherwise noted, capacitors should be placed less than 100 mils from the package.	Refer to Section 13.2.4.
VCCA_DAC (845GE chipset only) • (1) 0.1 µF Caps; (1) 0.01 µF Caps (Decoupling Cap – VCC) • Place near balls: B14 and A15	Refer to Section 13.2.4.
• Unless otherwise noted, caps should be placed less than 100 mils from the package.	Refer to Section 13.2.4.
• Edge caps must not have vias in the trace from the cap to the (G)MCH solder ball	Refer to Section 13.2.4.

15.10.2 Intel® (G)MCH Bulk Decoupling

Recommendation	Reason/Impact/Documentation
VTTFSB • (2) 10 µF caps • Place in VTT power corridor as shown in the above finger	Refer to Section 13.2.4.
VCC/VCCAGP/VCCHI • (2) 100 µF caps • (1) 220 µF caps • Place between the AGP connector and the (G)MCH. The 220 µF and one 100 µF cap must be placed in the VCC_CORE plane.	Refer to Section 13.2.4.
VCCSM • (4) 100 µF caps • Placed between the (G)MCH and DIMMs (one of the capacitors must be placed in the layer one shape)	Refer to Section 13.2.4.
• Unless otherwise noted, caps should be placed less than 100 mils from the package.	Refer to Section 13.2.4.
• Edge caps must not have vias in the trace from the cap to the (G)MCH solder ball	Refer to Section 13.2.4.

15.10.3 Intel® ICH4 Decoupling

Recommendation	Reason/Impact/Documentation
• Place caps within 100 mils from the package	Refer to Section 13.3.4.
VCC3_3 • (6) 0.1 µF caps - Decoupling Cap (VSS) • Place cap near A4, A1, H1, T1, AC10, and AC18	Refer to Section 13.3.4.
VCCSUS3_3 • (2) 0.1 µF caps - Decoupling Cap (VSS) • Place cap near balls: A22 and AC5	Refer to Section 13.3.4.
V_CPU_IO • (1) 0.1 µF cap - Decoupling Cap (VCC) • Place cap near ball: AA23	Refer to Section 13.3.4.
VCC1_5 • (2) 0.1 µF caps - Decoupling Cap (VSS) • Place cap near balls: K23 and C23	Refer to Section 13.3.4.
VCCSUS1_5 • (2) 0.1 µF caps - Decoupling Cap (VSS) • Place cap near balls: A16 and AC1	Refer to Section 13.3.4.
V5REF • (1) 0.1 µF cap - Decoupling Cap (VCC) • Place cap near ball: E7 • V5REF is the reference voltage for 5 V tolerant inputs in the ICH4. Tie to pins V5REF[2:1]. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3	Refer to Section 13.3.4.
V5_REF_SUS • (1) 0.1 µF cap - Decoupling Cap (VSS) • Place cap near ball: A16 • V5_REF_Sus only affects 5 V tolerance for USB OC[5:0]# pins and can be connected to VccSus3_3 if 5 V tolerance on these signals are not required.	Refer to Section 13.3.4.
VCCRTC • (1) 0.1 µF cap - Decoupling Cap (VCC) • Place cap near ball: AB5	Refer to Section 13.3.4.
VCCHI • (2) 0.1 µF cap – Decoupling Cap (VSS) • Place cap near balls: T23 and N23	Refer to Section 13.3.4.
VCCPLL • (1) 0.1 µF and (1) 0.01 µF cap – Decoupling Cap (VCC) • Place cap near balls: C22	Refer to Section 13.3.4.

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16 Signal Routing Reference

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements the 845GE/845PE chipset. The items contained within this checklist attempt to address important connections to these devices and any critical supporting circuitry. **This is not a complete list and does not guarantee that a design will function properly**. In addition to the items in this chapter, refer to the schematics in Appendix A. This work is ongoing, and the recommendations and considerations herein are subject to change.

16.1 Processor System Bus

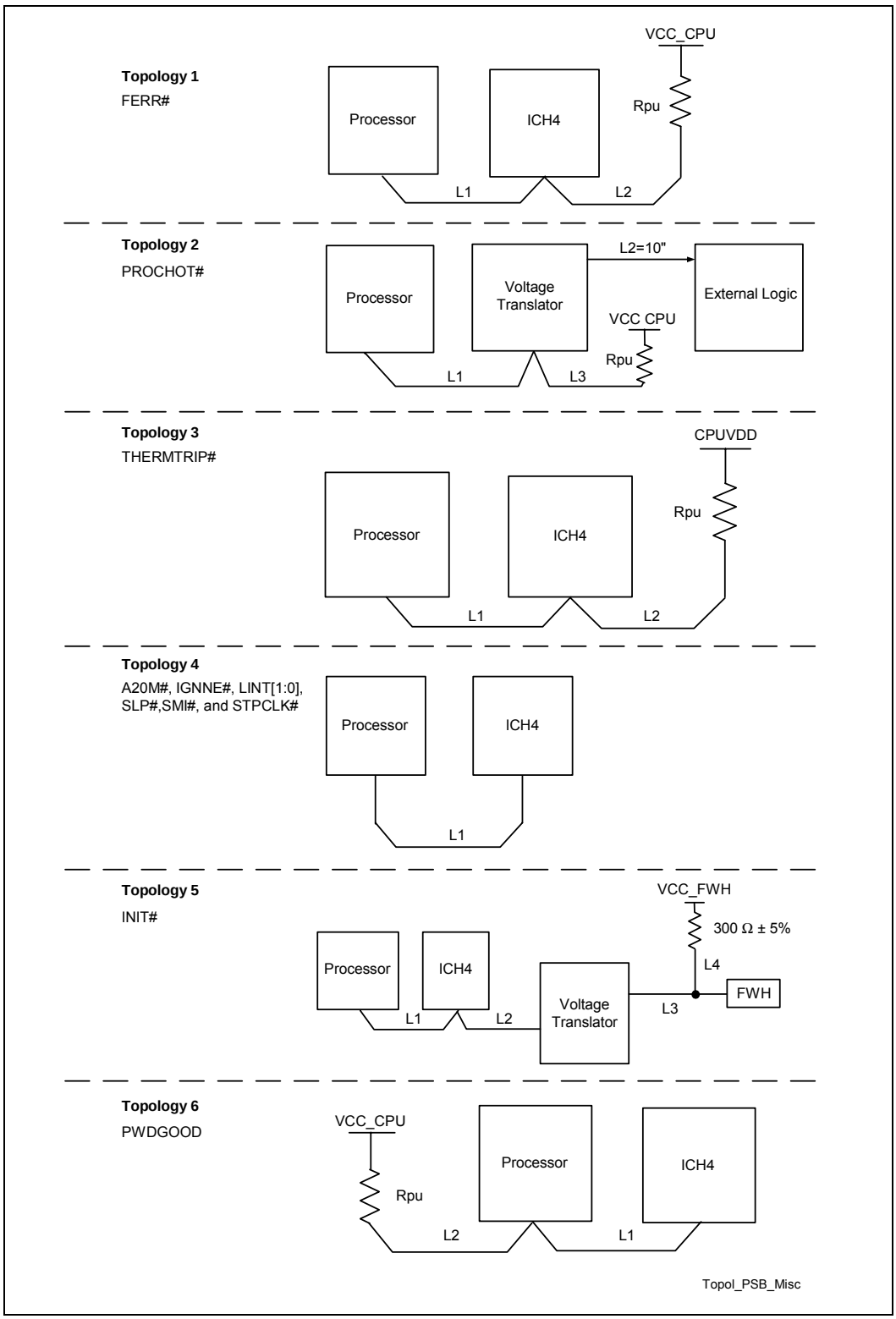
Table 16-1. Processor System Bus Routing

Intel® (G)MCH	I/O	Type	Plane Ref	Net Width (mils)	Net Spacing (Same Signal Group)	Spacing to other signals (mils)	Min MB length	Max MB length	Associated Strobe	Matching	Topology	Termination	Reference Section
HA[16:3]#	I/O	AGTL+	VSS	7	Breakout for a maximum of 250 mils from the component ball with 5 mils spacing. After that, spacing of 13 mils.	20	2"	10"	HADSTB_0#	Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ±200 mils of the associated strobes.	P to P	On Die	4.2.2.1
HREQ_[4:0]#	I/O	AGTL+	VSS	7					—				
HA[31:17]#	I/O	AGTL+	VSS	7					HADSTB_1#				
HADSTB_[1:0]#	I/O	AGTL+	VSS	7					—				
HD[15:0]#	I/O	AGTL+	VSS	7		20	2"	8"	HDSTB_P0# HDSTB_N0#	Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ±100 mils of the associated strobes	P to P	On Die	4.2.2.1
DINV_0#	I/O	AGTL+	VSS	7									
HD[31:16]#	I/O	AGTL+	VSS	7					HDSTB_P1# HDSTB_N1#				
DINV_1#	I/O	AGTL+	VSS	7									
HD[47:32]#	I/O	AGTL+	VSS	7					HDSTB_P2# HDSTB_N2#				
DINV_2#	I/O	AGTL+	VSS	7									
HD[63:48]#	I/O	AGTL+	VSS	7					HDSTB_P3# HDSTB_N3#				
DINV_3#	I/O	AGTL+	VSS	7									
HDSTB_P[3:0]#	I/O	AGTL+	VSS	7		20	2"	8"	—	DSTBN/P# routed to the same length as corresponding data signal mean pad-to-pad length ±25 mils	P to P	On Die	4.2.2.1
HDSTB_N[3:0]#	I/O	AGTL+	VSS	7					—				
ADS#	I/O	AGTL+	VSS	7		20	3"	10"	—	—	P to P	On Die	—
BNR#	I/O	AGTL+	VSS	7									
BPRI#	O	AGTL+	VSS	7									
CPURST#	O	AGTL+	VSS	7									
DBSY#	I/O	AGTL+	VSS	7									
DEFER#	O	AGTL+	VSS	7									
DRDY#	I/O	AGTL+	VSS	7									
HIT#	I/O	AGTL+	VSS	7									
HITM#	I/O	AGTL+	VSS	7									
HLOCK#	I	AGTL+	VSS	7									
HTRDY#	O	AGTL+	VSS	7									
RS_[2:0]#	O	AGTL+	VSS	7									

Table 16-2. Processor System Bus Miscellaneous Signals Routing

Intel® (G)MCH	I/O	Type	Plane Reference	Net Width (mils)	Spacing to other signals (mils)	Topology	L1		L2	L3	L4	Termination	Reference Section
							Min	Max	Max	Max	Max		
FERR#	O	Asyn GTL+	VSS	7	20	1	1"	12"	3"	—	—	62 Ohm series to VCC_CPU	4.3.1.1
PROCHOT#	O	Asyn GTL+	VSS	7	20	2	1"	17"	10"	3"	—	62 Ohm series to VCC_CPU	4.3.1.2
THERMTRIP#	O	Asyn GTL+	VSS	7	20	3	1"	12"	3"	—	—	62 Ohm series to VCC_CPU	4.3.1.3
A20M#	I	Asyn GTL+	VSS	7	20	4	—	17"	—	—	—	—	4.3.1.4
IGNNE#	I	Asyn GTL+	VSS	7	20		—		—	—	—	—	
LINT0 / INTR	I	Asyn GTL+	VSS	7	20		—		—	—	—	—	
LINT1 / NM		Asyn GTL+	VSS	7	20		—		—	—	—	—	
SLP#	I	Asyn GTL+	VSS	7	20		—		—	—	—	—	
SMI#	I	Asyn GTL+	VSS	7	20		—		—	—	—	—	
STPCLK#	I	Asyn GTL+	VSS	7	20		—		—	—	—	—	
INT#	I	Asyn GTL+	VSS	7	20	—	—	17"	2"	10"	3"	—	1.3.2.5
PWRGOOD	I	Asyn GTL+	VSS	7	20	5	1"	12"	3"	—	—	300 Ohm series to VCC_CPU	4.3.1.6

Figure 16-1. PSB Miscellaneous Signals Routing Topologies



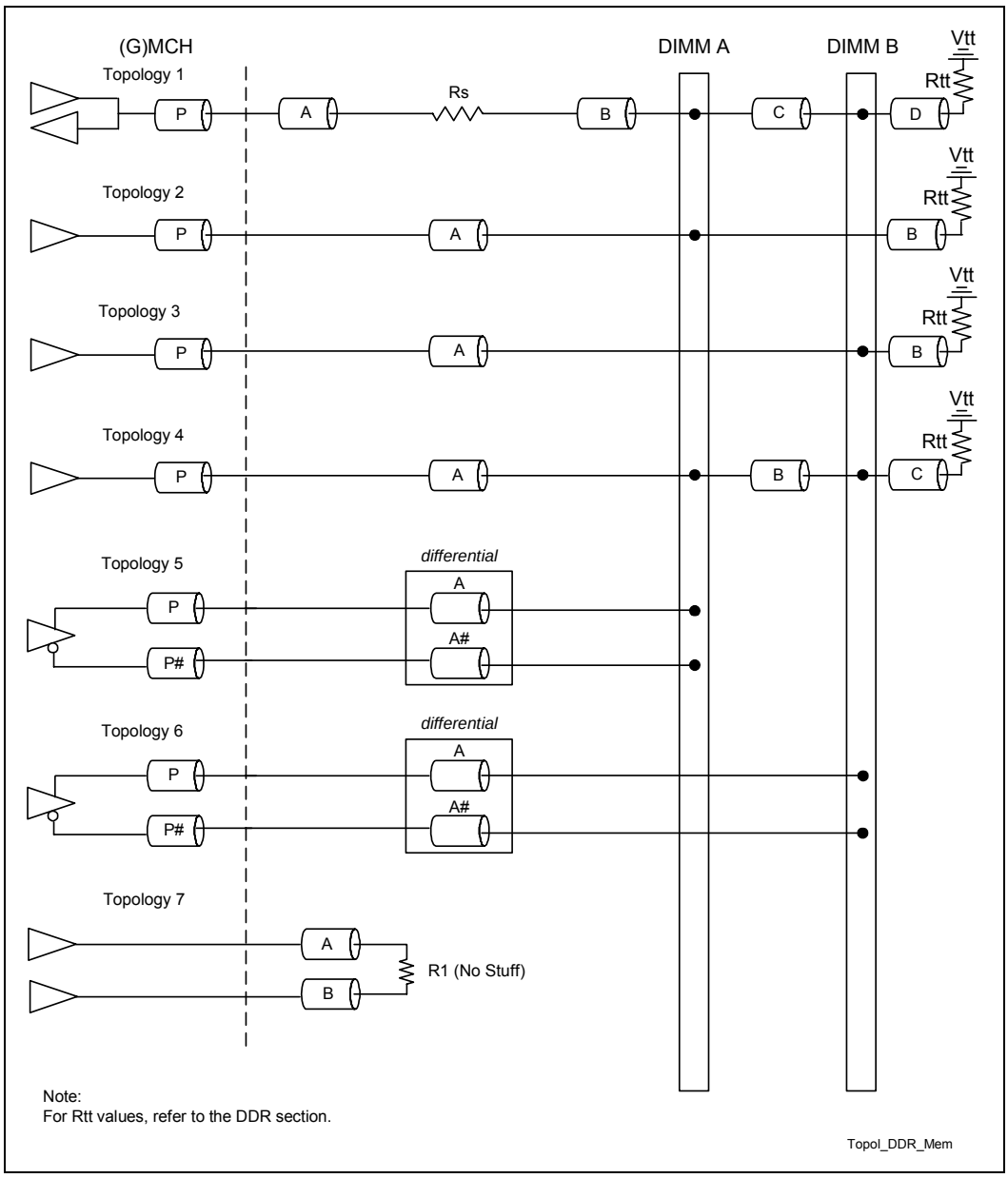
16.2 System Memory Interface

16.2.1 DDR – SDRAM

Table 16-3. DDR System Memory Interface Routing

Intel® (G)MCH	I/O	Type	Signal Group	Plane Reference	Layer Target	Nominal Width	Net Spacing (Same Signal Group)	Spacing to other signals (mils)	Topology	A	B		C		D	P	P+A+B	P+A	Intel® (G)MCH Breakout Guidelines	Length Tuning Method Section	Reference Section
										Max	Min	Max	Min	Max							
SDQ_[63:0]	I/O	SSTL2	Data	GND	1	5	Table 5-4	20	1	—	—	0.5"	0.4"	0.6"	0.8"	—	5.8"	—	5 mil width with 6 mil spacing for max of 350 mils	5.2.1.1	5.2.1
SDQS_[7:0]	I/O																				
SDM_[7:0]	O																				
SCS_[1:0]#	O	SSTL2	Control	GND	4	5	Table 5-6	20	2	3.5"	—	1.4"	—	—	—	—	—	—	5 mil width with 6 mil spacing for max of 350 mils	5.2.2.1	5.2.2
SCKE_[1:0]#	O																				
SCS_[3:2]#	O								3	4.0"	—	0.8"	—	—	—	—	—	—			
SCKE_[3:2]	O																				
SMAA_[12:6,3,0]	O	SSTL2	Addr/ Cmd	GND	4	5	Table 5-7	20	4	4.0"	0.4"	0.6"	—	0.8"	—	—	—	—	5 mil width with 6 mil spacing for max of 350 mils	5.2.3.1	5.2.3
SBA_[1:0]	O																				
SRAS#	O																				
SCAS#	O																				
SWE#	O																				
SMAA_[5,4,2,1]	O	SSTL2	CPC Addr	GND	4	5	Table 5-9	20	2	2.5"	—	1.4"	—	—	—	—	—	—	5 mil on 6 mil to the first 200 mils from ball. 5 mil on 8 mil to an additional 550 mils after the first 200 mils from ball	5.2.4.1	5.2.4
SMAB_[5,4,2,1]	O								3	3.0"	—	0.8"	—	—	—	—	—	—			
SCMD_CLK[2:0]	O	SSTL2	Clock	GND	4	8	Table 5-13	20	5	—	—	—	—	—	—	—	—	7.4"	5 mil width with 5 mil differential spacing with a min of 5 mils isolation from any other signal for max of 350 mils	5.2.5.1	5.2.5
SCMD_CLK[2:0]#	O																				
SCMD_CLK[5:3]	O								6	—	—	—	—	—	—	—	—	7.9"			
SCMD_CLK[5:3]#	O																				
SRCVEN_IN#	I	SSTL2	Feed back	GND	4	5	Table 5-15	10	7	0.1"	—	0.1"	—	—	—	—	—	—	N/A	N/A	5.2.6
SRCVEN_OUT#	O																				

Figure 16-2. DDR System Memory Routing Topologies

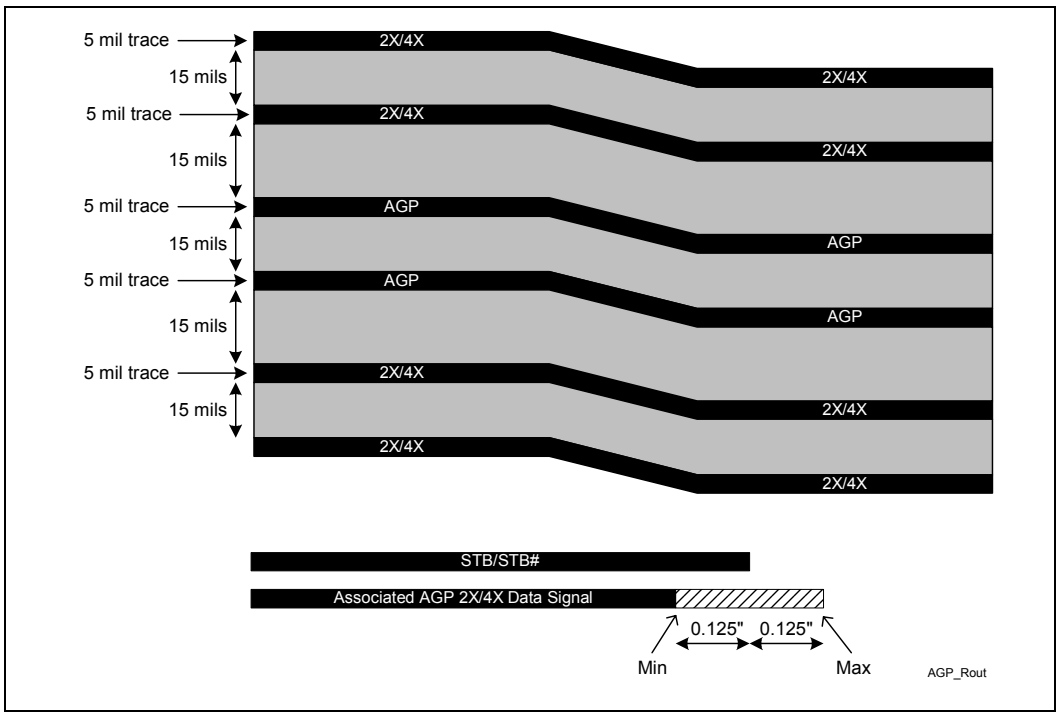


16.3 AGP Signals

Table 16-4. AGP Interface Routing

Intel® (G)MCH	I/O	Timing Domain	Plane Reference	Layer Target	Net Width (mils)	Net Spacing (Same Signal Group)	Max MB Length	Matching	Intel® (G)MCH Breakout Guidelines	Reference Section
GFRAME#	I/O	1X	—	—	5	7	6"	Match GTRDY# ±250 mils	—	6.2.1
GTRDY#	I/O		GND	4				Match GFRAME# ±250 mils		
GSTOP#	I/O		—	—				Match GAD_15# ±250 mils		
GIRDY#	I/O		GND	4				Match DEVSEL# ±250 mils		
GDEVSEL#	I/O		—	—				Match GIRDY# ±250 mils		
GRBF#	I		—	—				—		
GPIPE#	I		—	—						
GREQ#	I		—	—						
GWBF#	I		—	—						
GGNT#	O		GND	4						
GST_[2:0]	O		GND	4						
GPAR / ADD_DETECT	I/O		—	—						
GADSTB_[1:0]	I/O	2X/4X	—	—		15		Strobe should match complement to ±50 mils GADSTB_0 should match GADSTB_1 to ±125 mils (Note Strobes are not used for 1X mode)	5-mil spacing allowed. <0.3" from the (G)MCH package	6.2.2
GADSTB_[1:0]#	I/O		—	—						
GSB_STB	I		—	—						
GSB_STB#	I		—	—						
GAD_[15:0]	I/O		GND	4				Match with GADSTB_0 and GADSTB_0# from (G)MCH pad to AGP pin within ±125 mils		
GC/BE_[1:0]#	I/O		—	—						
GAD_[31:16]	I/O		—	—				Match with GADSTB_1 and GADSTB_1# from (G)MCH pad to AGP pin within ±125 mils		
GC/BE_[3:2]#	I/O		—	—						
GSBA_[7:0]	I		—	—				Match with GADSTB and GADSTB# from (G)MCH pad to AGP pin within ±125 mils		

Figure 16-3. AGP 2X, 4X Routing Example



16.4 Display Interface Signals (Intel® 845GE chipset only)

Table 16-5. Display Interface: DVO Down Signal Routing (Intel® 845GE chipset only)

Intel® GMCH	I/O	Plane Reference	Layer Target	Net Width	Net Spacing (Same Signal Group)	Spacing to other signals (mils)	Maximum MB Length	Matching	Intel® GMCH Breakout Guidelines	Reference Section
DVOB_CLK / DVOB_CLK#	O	GND	4	5	15	20	7.5"	Match complement ±50 mils	—	—
DVOB_D[11:0]	O	GND	4	5	15	15	7.5"	Match to DVOB_CLK / DVOB_CLK# within ±0.1"	Width and Space 5 mils on 5 mils. 5 mils spacing allowed <0.3" from GMCH package	6.5.2
DVOB_HSYNC	O	GND	4	5	15	15	7.5"			
DVOB_VSYNC	O	GND	4	5	15	15	7.5"			
DVOB_BLANK#	O	GND	4	5	15	15	7.5"			
DVOBC_CLKINT#	I	GND	4	5	15	15	7.5"	—		
DVOB_FLDSTL	I	GND	4	5	15	15	7.5"	—		
DVOC_CLK / DVOC_CLK#	O	GND	4	5	15	20	7.5"	Match complement ±50 mils		
DVOC_D[11:0]	O	GND	4	5	15	15	7.5"	Match to DVOC_CLK / DVOC_CLK# within 0.1"		
DVOC_HSYNC	O	GND	4	5	15	15	7.5"			
DVOC_VSYNC	O	GND	4	5	15	15	7.5"			
DVOC_BLANK#	O	GND	4	5	15	15	7.5"			
DVOBC_INTR#	I	GND	4	5	15	15	7.5"	—		
DVOC_FLDSTL	I	GND	4	5	15	15	7.5"	—		
MI2C_CLK	I/O	GND	4	5	15	15	7.5"	—		
MI2C_DATA	I/O	GND	4	5	15	15	7.5"	—		
MDVI_CLK	I/O	GND	4	5	15	15	7.5"	—		
MDVI_DATA	I/O	GND	4	5	15	15	7.5"	—		
MDDC_CLK	I/O	GND	4	5	15	15	7.5"	—		
MDDC_DATA	I/O	GND	4	5	15	15	7.5"	—		

Table 16-6. Display Interface: Analog Display Routing Signal (Intel® 845GE chipset only)

Intel® GMCH	I/O	Type	Type	Net Width	Net Spacing (Same Signal Group)	Spacing to other signals (mils)	Matching	Reference Section
VSYNC	O	3.3 V	GPIO	—	—	—	—	7.1 7.2
HSYNC	O	3.3 V	GPIO	—	—	—	—	
RED	O	NA	Analog	8	5	20	*Routing parallel complement (i.e., RED and RED#) to terminating resistor *Match RGB signals ±200 mils to VGA connector	
RED#	O	NA	Analog	8	5	20		
GREEN	O	NA	Analog	8	5	20		
GREEN#	O	NA	Analog	8	5	20		
BLUE	O	NA	Analog	8	5	20		
BLUE#	O	NA	Analog	8	5	20		
REFSET	I	NA	Analog	8	5	20		
DDCA_CLK	I/O	3.3 V	GPIO	—	—	—	—	
DDCA_DATA	I/O	3.3 V	GPIO	—	—	—	—	

16.5 Hub Interface Signals

Table 16-7. Hub Interface Routing

Intel® (G)MCH	I/O	Type	Plane Reference	Layer Target	Net Width (mils)	Net Spacing (Same Signal Group)	Spacing to other signals	Min MB Length	Max MB Length	Matching	Reference Section
HSTRS	I/O	H	GND	4	5	15	20	2"	8"	Length between two strobes match within ±100 mils	8.1
HSTRF	I/O	H	GND	4	5	15	20	2"	8"		
H[7:0]	I/O	H	GND	4	5	15	20	2"	8"	Each data signal match within ±100 mils of the strobe pair	
H8	O	H	GND	4	5	15		2"	8"		
H9	I	H	GND	4	5	15		2"	8"		
H10	I/O	H	GND	4	5	15		2"	8"		

16.6 Clocking Signals

Table 16-8. Clocking Signals Routing

Intel® (G)MCH	I/O	Type	Freq.	Plane Ref	Net Width (mils)	Net Spacing (same signal group - mils)	Spacing to other signals (mils)	Topology	A	B		C		A + B	A + B + C	Reference Section
									Max	Min	Max	Min	Max			
HOST_CLK	O	CMOS	100/133	GND	7	—	—	1	—	—	—	—	—	—	—	12.2.1
DOT_CLK (845GE chipset only)	O	LVTTL	48	GND	5	NA	20	2	0.5"	2.0"	9.0"	—	—	—	—	12.2.2
CLK66	O	LVTTL	66	GND	5	20	20	3	0.5"	4.0"	8.5"	—	—	—	—	12.2.3
AGPCLK	O	—	66	GND	5	15	15	4	0.5"	(CLK66 Trace B) - 4	—	Route per the AGP Spec		—	—	12.2.4
CLK33	O	—	33	GND	5	15	15	5	0.5"	4"	8.5"	—	—	CLK66 ±100 mils	—	12.2.5
CLK14	O	—	14.318	GND	5	10	10	6	0.5"	0"	12"	0"	6"	CLK33 ±500 mils	Match to ±5" of each other	12.2.6
PCICLK	O	—	33	GND	5	15	15	7	0.5"	—	—	—	—	PCI device down: (CLK33) ±500 mils. Devices on PCI cards:(CLK33 – 2.5") ±500 mils	—	12.2.7
USBCLK	O	—	48	GND	5	NA	20	8	0.5"	3"	12"	—	—	—	—	12.2.8

NOTES: DOT_CLK applies to the 845GE chipset only.

Figure 16-4. Clocking Signals Routing Topologies

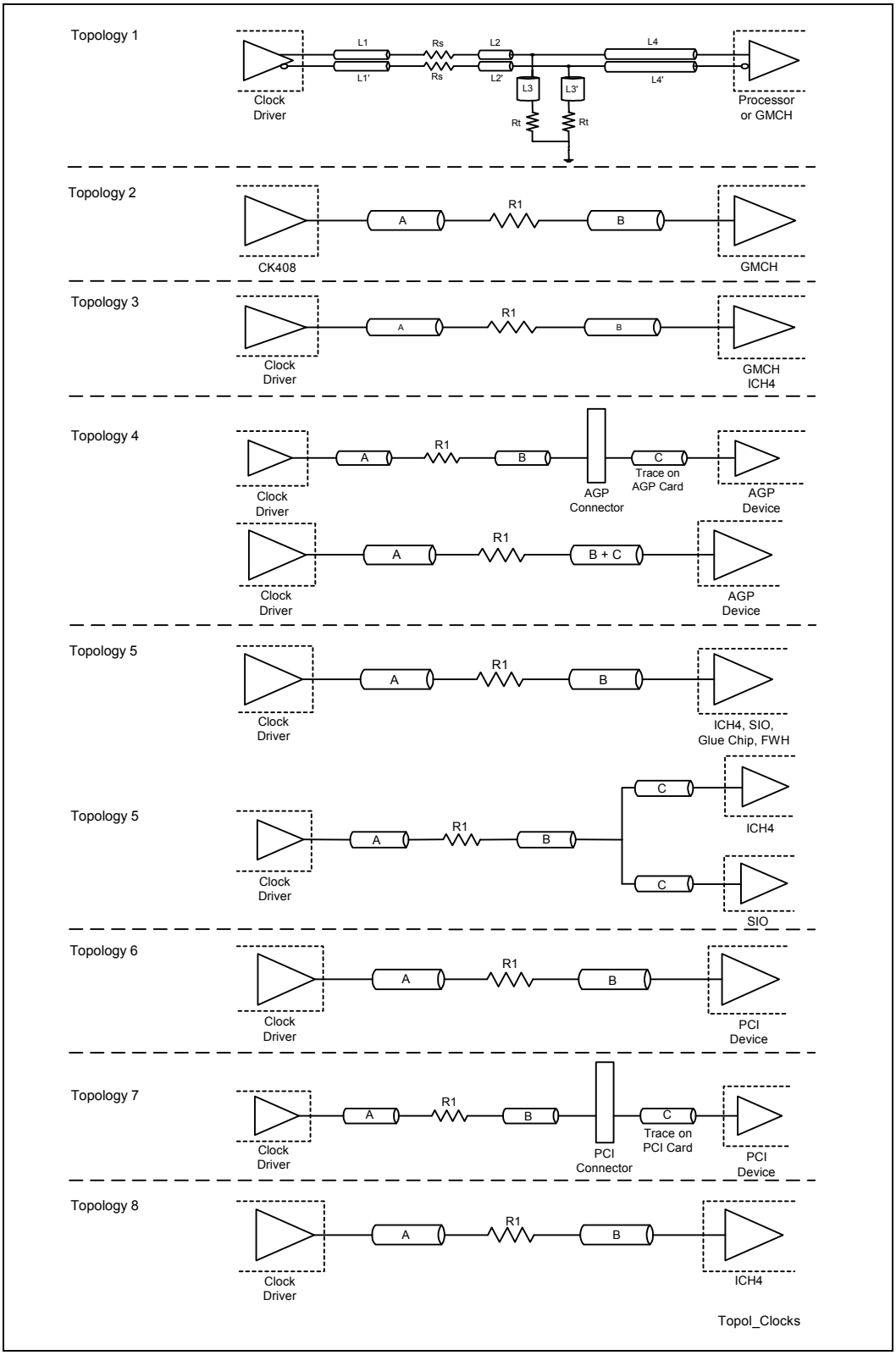


Figure 16-5. Host Clocking Signals Routing Topologies

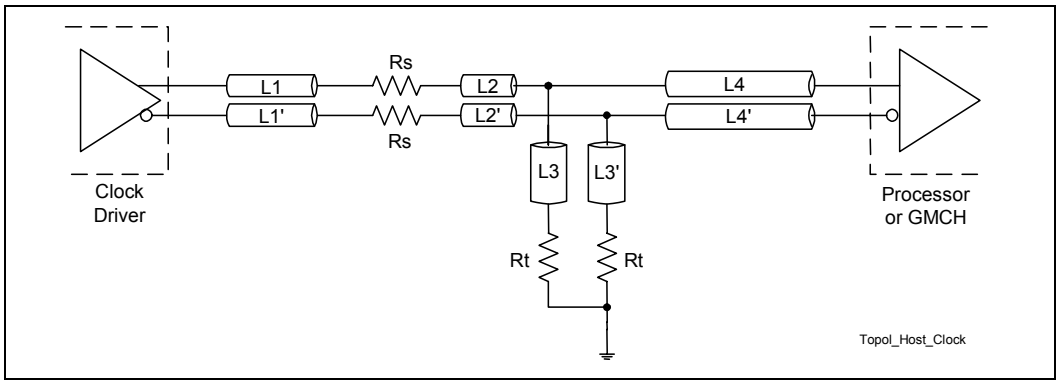


Table 16-9. Host Clock Routing Guidelines (BCLK[1:0]#, HCLKP, HCLKN)

Layout Guideline	Value	Notes
Host Clock Skew between agents	400 ps total Budget: 150 ps for Clock driver 250 ps for interconnect	2, 3, 4,5
Reference Plane	Ground Referenced (Contiguous over entire length)	--
Differential pair spacing = S	8 mils	6, 7
Spacing to other traces	3S to 4S	--
Nominal trace width = W	7.0 mils	8
System board Impedance – Differential	100 Ω ± 15%	9
System board Impedance – odd mode	50 Ω ± 15%	10
Processor routing length – L1, L1': Clock driver to Rs	0.5” max	13
Processor routing length – L2, L2': Rs to Rs-Rt node	0 – 0.2 inch	13
Processor routing length – L3, L3’: RS-RT node to Rt	0 – 0.2 inch	13
Processor routing length – L4, L4': RS-RT Node to Load	2 – 12"	
(G)MCH routing length – L1, L1’: Clock Driver to RS	0.5” max	13
(G)MCH routing length – L2, L2': Rs to Rs-Rt node	0 – 0.2 inch	13
(G)MCH routing length – L3, L3’: RS-RT node to Rt	0 – 0.2 inch	13
(G)MCH routing length – L4, L4': RS-RT Node to Load	2 – 12"	
Clock driver to Processor and clock driver to chipset length matching (L1 + L2 + L4)	Clock pair to (G)MCH must be 100 mils longer than clock pair to processor socket	10
HCLKP – HCLKN, BCLK0 – BCLK1 length matching	± 10 mils	--
Rs Series termination value	27 Ω ± 1%	11
Rt Shunt termination value	49.9 Ω ± 1% (for 50 Ω MB impedance)	12
Maximum Via Count Per Signal	3	

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17 Intel® 845GE/845PE Chipset Schematic Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements the 845GE/845PE chipset. The items contained within this checklist attempt to address important connections to these devices and any critical supporting circuitry. **This is not a complete list and does not guarantee that a design will function properly**. In addition to the information in this chapter, refer to the schematics in Appendix A. This work is ongoing, and the recommendations and considerations herein are subject to change.

17.1 Host Interface

17.1.1 Processor/ Intel® (G)MCH Items

Checklist Item	Recommendation	Reason/Impact/Documentation
A[31:3]#	• Connect to HA[31:3] pins on (G)MCH • Leave A[35:32]# as No Connect.	Chipset does not support extended addressing over 4 GB, leave A[35:32]# unconnected. AGTL+ Source Synch I/O Signal
ADS#	• Connect to the same pin name on the (G)MCH	AGTL+ Common Clock I/O Signal
ADSTB[1:0]#	• Connect to HADSTB_[1:0]# pins on (G)MCH	AGTL+ Source Synch I/O Signal
BNR#	• Connect to the same pin name on the (G)MCH	AGTL+ Common Clock I/O Signal
BPRI#	• Connect to the same pin name on the (G)MCH	AGTL+ Common Clock Input Signal
BREQ0#	• Connect to BREQ0# on the (G)MCH • Terminate to VCCP through a 150 Ω – 220 Ω ±5% resistor near the processor	The chipset contains on die termination for the BREQ0# signal. The Intel® Pentium® 4 processor does not contain on die termination for this particular AGTL+ signal thus external termination is required only on the processor end. BR0# termination should equal the resistance value of on die AGTL+ termination resistance (Rtt) value. AGTL+ Common Clock I/O Signal Refer to Section 4.3.1.8 and Figure 4-10
D[63:0]#	• Connect to HD[63:0]# pins on (G)MCH	AGTL+ Source Synch I/O Signal.
DBI[3:0]#	• Connect to DINV_[3:0]# pin on the (G)MCH	AGTL+ Source Synch I/O Signal.

Checklist Item	Recommendation	Reason/Impact/Documentation
DBSY#	• Connect to the same pin name on the (G)MCH	AGTL+ Common Clock I/O Signal
DEFER#	• Connect to the same pin name on the (G)MCH	AGTL+ Common Clock Input Signal.
DRDY#	• Connect to the same pin name on the (G)MCH	AGTL+ Common Clock I/O Signal.
DSTBN[3:0]#	• Connect to HDSTB_N[3:0]# pins on (G)MCH	AGTL+ Source Synch I/O Signal.
DSTBP[3:0]#	• Connect to HDSTB_P[3:0]# pins on (G)MCH	AGTL+ Source Synch I/O Signal.
HIT#	• Connect to the same pin name on the (G)MCH	AGTL+ Common Clock I/O Signal.
HITM#	• Connect to the same pin name on the (G)MCH	AGTL+ Common Clock I/O Signal.
LOCK#	• Connect to HLOCK# pin on (G)MCH	AGTL+ Common Clock I/O Signal.
REQ[4:0]#	• Connect to HREQ_[4:0]# pins on (G)MCH	AGTL+ Source Synch I/O Signals.
RESET#	• Connect to the CPURST# on the (G)MCH • Terminate to VCCP through a 51Ω ±5% resistor near the processor	The chipset contains on die termination for the CPURST# signal. The Intel® Pentium® 4 processor does not contain on die termination for this particular AGTL+ signal thus external termination is required only on the processor end. RESET# termination should equal the resistance value of on die AGTL+ termination resistance (Rtt) value. AGTL+ Common Clock I/O Signal Refer to Section 4.3.1.8 and Figure 4-10
RS_[2:0]#	• Connect to the same pin name on the (G)MCH	AGTL+ Common Clock Input Signal.
TRDY#	• Connect to HTRDY# pin on (G)MCH	AGTL+ Common Clock Input Signal.

17.1.2 Intel® (G)MCH Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
HA_VREF HCC_VREF HDVREF_[2:0]	• Connect voltage divider circuit to VCCP through a 49.9 Ω ±1% pull-up resistor and to GND through a 100 Ω ±1% pull-down resistor Decouple the voltage divider with a 0.1µF ±10% capacitor.	Refer to DG Section 4.1.1
HCLKN	• Connect to CPU2 in CK408 • Connect to a series 27.4 Ω ± 1% resistor and terminate to GND through a 49.9 Ω ±1% resistor	
HCLKP	• Connect to CPU2# in CK408 • Connect to a series 27.4 Ω ± 1% resistor and terminate to GND through a 49.9 Ω ±1% resistor	
HX_RCOMP HY_RCOMP	• Pull-down to GND through a 24.9 Ω ±1% resistor	
HX_SWING HY_SWING	• Connect voltage divider circuit to VCCP through a 301Ω ± 1% pull-up resistor and to GND through a 150 Ω ± 1% pull-down resistor • Decouple the voltage divider with a 0.01 µF ± 10% capacitor to VCCP	
VTTDECAP	• GND through a 0.1µF ±10% capacitor	
VTTFSB	• Connect to Processor Vreg (2) 10 µF and (5) 0.1 µF capacitor	Refer to Section 13.2.4.

17.1.3 Processor/ Intel® ICH4 Items

Checklist Item	Recommendation	Reason/Impact/Documentation
A20M#	• Connect to the same pin name on the ICH4 through a 60 Ω – 80 Ω series resistor. (No extra pull-up resistors required)	Asynch GTL+ Input Signal Refer to Section 4.3.1.4
FERR#	• Connect to the same pin name on the ICH4 • Terminate to VCCP through a 62 Ω ±5% resistor	This output signal is not terminated on the processor. Termination is required on system board. Asynch GTL+ Output Signal Refer to DG Section 4.3.1.1
IGNNE#	• Connect to the same pin name on the ICH4 through a 60 Ω – 80 Ω series resistor. (No extra pull-up resistors required)	Asynch GTL+ Input Signal Refer to Section 4.3.1.4
INIT#	• Connect to the same pin name on the ICH4 (No extra pull-up resistors required) • Level shifting required to connect to Firmware Hub • From FWH tie to VCC_FWH through a 300 Ω ± 5% resistor	Termination not required. Asynch GTL+ Input Signal. Refer to DG Section 4.3.1.3
LINT[1:0]	• LINT0 connects to INTR on ICH4 through a 60 Ω – 80 Ω series resistor (No extra pull-up resistors required) • LINT1 connects to NMI on ICH4 through a 60 Ω – 80 Ω series resistor (No extra pull-up resistors required)	Asynch GTL+ Input Signal Refer to Section 4.3.1.4
PWRGOOD	• Connects to CPUPWRGD in ICH4 through a 60 Ω – 80 Ω series resistor (Weak external pull-up resistor required) • Terminate to VCCP through a 300 Ω ±5% resistor	Asynch GTL+ Input Signal Refer to Section 4.3.1.6
SLP#	• Connect to CPUSLP# on the ICH4 through a 60 Ω – 80 Ω series resistor (No extra pull-up resistors required)	
SMI#	• Connect to the same pin name on the ICH4 through a 60 Ω – 80 Ω series resistor (No extra pull-up resistors required	Asynch GTL+ Input Signal Refer to Section 4.3.1.4
STPCLK#	• Connect to the same pin name on the ICH4 through a 60 Ω – 80 Ω series resistor (No extra pull-up resistors required	Asynch GTL+ Input Signal Refer to Section 4.3.1.4

17.1.4 Processor Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
A[35:32]#	• No Connect	Chipset does not support extended addressing over 4GB, leave A[35:32]# unconnected.
AP[1:0]#	• No Connect	Chipset does not support parity protection on the address bus. AGTL+ Common Clock I/O Signal.
BCLK[1:0]	• BLCK0 connects to CPU0 in CK408 thru a 27.4 Ω ± 1% resistor • BLCK1 connects to CPU0# in CK408 thru a 27.4 Ω ± 1% resistor	Rt resistors should be selected to match the characteristic impedance of the board. System Bus Clock Signal Refer to Section 12.2.1
BPM[5:0]#	• These signals should be terminated with a 51 Ω ± 5% resistor to VCCP near the processor. If a debug port is implemented termination is required near the debug port as well. Refer to the processor Debug Port Design Guide for further information.	
BINIT#	• No Connect	Chipset does not support this signal. AGTL+ Common Clock I/O Signal
BSEL[1:0]	• BSEL1 – No Connect • BSEL0 - Connect to (G)MCH PSB_SEL • Terminate to (G)MCH 3.3 V supply through a 1.5 kΩ ± 5% resistor	
COMP[1:0]	• Terminate to GND through a 51.1Ω ±1% resistor • Minimize the distance from termination resistor and processor pin	Each COMP pin requires a separate resistor for each pin. RCOMP value can be adjusted to set external drive strength of I/O and to control edge rate. Refer to Section 4.3.1.8
DBR#	• Connect to SYS_RST# in ICH4 • Refer to the processor Debug Port Design Guide for further information.	
DP[3:0]#	• No Connect	Not supported by chipset
IERR#	• No Connect • Ok to Testpoint	Not supported by chipset Asynch GTL+ Output Signal.
GTLREF[3:0]	• GTLREF[3:1] – No Connect • GTLREF0 - Terminate to VCCP through a 49.9 Ω ±1% resistor • Terminate to GND through a 100 Ω ±1% resistor • Should be 2/3 VCCP	Correct settings are critical. This signal controls the signal reference of the AGTL+ input pins. Refer to Section 4.1.1

Checklist Item	Recommendation	Reason/Impact/Documentation
ITP_CLK0	• Connect to CPU1 in CK_408 through a 27.4 Ω ±1% resistor • Refer to the processor Debug Port Design Guide for further information.	
ITP_CLK1	• Connect to CPU1# in CK_408 through a 27.4Ω ±1% resistor • Refer to the processor Debug Port Design Guide for further information.	
MCERR#	• No Connect	Chipset does not support this signal. AGTL+ Common Clock I/O Signal.
PROCHOT#	• No connect	Asynch GTL+ Output Signal Refer to Section 4.3.1.2.
RSP#	• No Connect	Chipset does not support this signal. AGTL+ Common Clock Input Signal.
SKTOCC#	• Connect to CPU_Present on Glue Chip thru 33 Ω ± 5% resistor or to Discrete Logic (If pin is used)	Processor pulls this signal to GND. System board designers may use this pin to determine if the processor is present in the socket.
TCK	• Refer to the processor Debug Port Design Guide for further information.	
TDI	• Refer to the processor Debug Port Design Guide for further information	
TDO	• Refer to the processor Debug Port Design Guide for further information.	
TESTHI[12:0]	• The TESTHI pins should be tied to the VCC_CPU via a matched resistor that has a resistance value within ± 20% of the impedance of the board transmission line traces. • See DG Section 4.3.1.11 for further details.	Tying any of the TESTHI pins together will prevent the ability to perform boundary scan testing. Refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*
THERMTRIP#	• Terminate to VCCP through a 62 Ω ±5% resistor near the processor	Asynch GTL+ Output Signal Refer to Section 4.3.1.3
THERMDA	• Connect to thermal monitor circuitry if used Connect to REMOTE1+ in HECETA	Refer to Section 4.3.1.10.
THERMDC	• Connect to thermal monitor circuitry if used Connect to REMOTE1-/NTESTIN in HECETA	Refer to Section 4.3.1.10.
TMS	• Refer to the processor Debug Port Design Guide for further information. Connect to the same name in ITP port	
TRST#	• Refer to the processor Debug Port Design Guide for further information. Terminate to ground through a 680 Ω ± 5 resistor	

Checklist Item	Recommendation	Reason/Impact/Documentation
VCCA	• Connect with isolated power circuitry to VCCP	Isolated power for internal processor system bus PLLs Refer to Sections 4.3.1.7 and 4.7.2.1.
VCCIOPLL	• Connect with isolated power circuitry to VCCP	Isolated power for internal processor system bus PLLs Refer to Sections 4.3.1.7 and 4.7.2.1.
VCC_SENSE	• Connect through test point header to VSS_SENSE	Isolated low impedance connection to processor core power (VCC) Refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*.
VCCVID	• Connect to 1.2 V linear regulator	Refer to Section 4.3.1.12
VID[4:0]	• Connect to VR or VRM. These signals need to be pulled up to 3.3 V through either 1 kΩ pull-ups on the motherboard or with internal pull-ups in the VR or VRM.	Refer to the *VRM9.0 DC-DC Converter Design Guidelines*
VSSA	• Connect with isolated power circuitry to VCCP	Isolated GND for internal PLLs Refer to Sections 4.3.1.7 and 4.7.2.1.
VSS_SENSE	• Connect through test point header to VCC_SENSE	Isolated low impedance connection to core VSS. Refer to the processor datasheet.

17.2 Memory Interface

17.2.1 DDR SDRAM

17.2.1.1 Intel® (G)MCH/DIMM Connector Items (DDR)

Checklist Item	Recommendation	Reason/Impact/Documentation
SBA_[1:0]	• Connect to BA[1:0] pin on both DIMMA and DIMMB • Terminate to VTT through a 56 Ω ±5% resistor	Follow DDR Address/Command Signal routing topology guidelines. Refer to Section 5.2.3.
SCAS#	• Connect to CAS# pin on both DIMMA and DIMMB • Terminate to VTT through 56 Ω ±5% resistor	Follow DDR Address/Command Signal routing topology guidelines. Refer to Section 5.2.3.
SDM_[7:0]	• Connect to DM[7:0] on both DIMMA and DIMMB connect through a series 10 Ω ± 5% resistor and terminate to VTT through a 56 Ω ±5% resistor.	Follow DDR Data Signal routing topology guidelines. Refer to Section 5.2.1.
SCMDCLK_[2:0]	• Connect to CK[2:0] in DIMMA	Refer to DG Section 5.2.5.
SCMDCLK_[5:3]	• Connect to CK[2:0] in DIMMB	Refer to DG Section 5.2.5.
SCMDCLK_[2:0]#	• Connect to CK[2:0]# in DIMMA	Refer to DG Section 5.2.5.
SCMDCLK_[5:3]#	• Connect to CK[2:0]# in DIMMB	Refer to DG Section 5.2.5.
SCKE_[1:0]	• Connect to CKE[1:0] on DIMMA • Terminate to VTT through a 56 Ω ±5% resistor	Refer to DG Section 5.2.2.
SCKE_[3:2]	• Connect to CKE[1:0] on DIMMB • Terminate to VTT through a 56Ω ±5% resistor	Refer to DG Section 5.2.2.
SCS_[1:0]#	• Connect to CS[1:0]# on DIMMA • Terminate to VTT through a 56Ω ±5% resistor	Refer to DG Section 5.2.2.
SCS_[3:2]#	• Connect to CS[1:0]# on DIMMB • Terminate to VTT through a 56 Ω ±5% resistor	Refer to DG Section 5.2.2.
SDQ_[63:0]	Connect to DQ[63:0] on both DIMMA and DIMMB through a series 10 Ω ±5% resistor and terminate to VTT through a 56 Ω ±5% resistor	Follow DDR Data Signal routing topology guidelines. Refer to Section 5.2.1.
SDQS_[7:0]	• Connect to DQS[7:0] pins on both DIMMA and DIMMB • Connect to a series 10 Ω ±5% resistors and terminate to VTT through a 56 Ω ±5% resistor	Follow DDR Data Signal routing topology guidelines. Refer to Section 5.2.1.

Checklist Item	Recommendation	Reason/Impact/Documentation
SMAA_[12:6,3,0]	• Connect to A[12:6,3,0] pins on DIMMA and DIMMB • Terminate to VTT through a 56 Ω ±5% resistor	Follow DDR Address/Command Signal routing topology guidelines. Refer to Section 5.2.3.
SMAA_[5,4,2,1]	• Connect to A[5,4,2,1] on DIMMA • Terminate to VTT through a 33 Ω ±5% resistor	Refer to Section 5.2.4.
SMAB_[5,4,2,1]	• Connect to A[5,4,2,1] on DIMMB • Terminate to VTT through a 33 Ω ± 5% resistor.	Refer to Section 5.2.4.
SRAS#	• Connect to RAS# pin on both DIMMA and DIMMB • Terminate to VTT through a 56 Ω ±5% resistor	Follow DDR Address/Command Signal routing topology guidelines. Refer to Section 5.2.3.
SWE#	• Connect to WE# pin on each DIMMA and DIMMB • Terminate to VTT through a 56 Ω ±5% resistor	Follow DDR Address/Command Signal routing topology guidelines. Refer to Section 5.2.3.

17.2.1.2 Intel® (G)MCH Only Items (DDR)

Checklist Item	Recommendation	Reason/Impact/Documentation
SRCVEN_OUT#	• Connect directly to (G)MCH SRCVEN_IN# pin through an un-populated resistor site.	Refer to Section 5.2.6.
SRCVEN_IN#	• Connect directly to (G)MCH SRCVEN_OUT# pin through an un-populated resistor site.	Refer to Section 5.2.6.
SM_VREF	• Connect to DDR Reference Voltage (VREF) 1.25 V • Resistor divider consists of two identical resistors (50 Ω – 150 Ω, 1%) • Terminate to ground through a 0.1 uF 10% capacitor	Refer to Section 5.4.4.
SMX_RCOMP SMY_RCOMP	• 60.4 Ω 1% resistor pulled to DDR 2.5 V, and 60.4 Ω ± 1% resistor tied to ground • The 0.1 µF 20% cap connected to 2.5 V and GND should be used as illustrated in Figure 5-46 of this DG.	Refer to Section 0.
VCCSM	• Connect to 2.5 V	

17.2.1.3 DIMM Connector Only Items (DDR)

Checklist Item	Recommendation	Reason/Impact/Documentation
A13 / NC	• No Connect both DIMMA and DIMMB	
DM[8]/DQS17	• No Connect both DIMMA and DIMMB	
SDQS_8	• No Connect both DIMMA and DIMMB	
CB[7:0]	• No Connect both DIMMA and DIMMB	
BA2	• No Connect both DIMMA and DIMMB	
SA[2:0]	• DIMMA: Connect to GND • DIMMB: Connect SA[2:1] to GND, and Connect SA0 to 2.5 V	
WP	• No Connect both DIMMA and DIMMB	
RESET#	• No Connect both DIMMA and DIMMB	
FETEN	• No Connect both DIMMA and DIMMB	
SDA	• Connect to SMBDATA and SMLINK1 in ICH4 through SMBUS isolation circuitry.	
SCL	• Connect to SMBCLK and SMILINK0 in ICH4 through SMBUS isolation circuitry.	
VREF	• Connect to DDR Reference Voltage (VREF) • Terminate to ground through a 0.1 µF 10% capacitor	
VDDSPD	• Connect to power (from a minimum of 2.3 V to a maximum of 3.6 V) • Strongly recommend connecting to 2.5 V core	
VDDID	• No Connect	
VDD	• Connect to 2.5 V both DIMMA and DIMMB	
VDDQ	• Connect to 2.5 V both DIMMA and DIMMB	
VSS	• Connect to GND	
NC	• No Connect both DIMMA and DIMMB	
CS[3:2]#	• No Connect both DIMMA and DIMMB	

17.3 AGP Interface

17.3.1 AGP Connector / Intel® (G)MCH Items

Checklist Item	Recommendation	Reason/Impact/Documentation
GADSTB_[1:0]	• Connect to GADSTB_[1:0] in (G)MCH • Recommend site for a pull up resistor to 1.5 V (4 kΩ to 16 kΩ if populated)	The (G)MCH has integrated pull-ups for these signals, but external resistors may still be required. Refer to Section 6.4.2.
GADSTB_[1:0]#	• Connect to GADSTB_[1:0]# in (G)MCH • Recommend site for a pull-down resistor to GND (4 kΩ to 16 kΩ if populated)	The (G)MCH has integrated pull-downs for these signals, but external resistors may still be required. Refer to Section 6.4.2.
GAD_[31:0]	• Connect to GAD_[31:0] in (G)MCH	
GC/BE[3:0]#	• Connect to GC/BE_[3:0]# in (G)MCH	
GDEVSEL#	• Connect to GDEVSEL# in (G)MCH • Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated)	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 6.4.2.
GFRAME#	• Connect to GFRAME# in (G)MCH • Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated)	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 6.4.2.
GGNT#	• Connect to GGNT# in (G)MCH • Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ)	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 6.4.2.
GIRDY#	• Connect to GIRDY# in (G)MCH • Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated)	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 6.4.2.
GPAR	• Connect to GPAR/ADD_DETECT in (G)MCH • Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated)	Chipset has integrated pull-ups, but signal may still require
PIPE#	• Connect to GPIPE# in (G)MCH • Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated)	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 6.4.2.
GREQ#	• Connect to GREQ# in (G)MCH • Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated)	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 6.4.2.

Checklist Item	Recommendation	Reason/Impact/Documentation
GSTOP#	• Connect to GSTOP# in (G)MCH • Recommend site for a pull-up resistor to VDDQ (4 kΩ to 1 6kΩ if populated)	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 6.4.2.
GTRDY#	• Connect to GTRDY# in (G)MCH • Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated)	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 6.4.2.
RBF#	• Connect in GRBF# in (G)MCH • Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated)	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 6.4.2.
SBA_[7:0]	• Connect to GSBA_[7:0] in (G)MCH	Chipset has integrated pull-ups for these signals.
SB_STB	• Connect to GSBSTB in (G)MCH • Recommend site for a pull-up resistor to 1.5 V (4 kΩ to 16 kΩ if populated)	The (G)MCH has integrated pull-ups for these signals, but external resistors may still be required. Refer to Section 6.4.2.
SB_STB#	• Connect to GSBSTB# (G)MCH • Recommend site for a pull-down resistor to GND (4 kΩ to 16 kΩ if populated)	The (G)MCH has integrated pull-downs for these signals, but external resistors may still be required. Refer to Section 6.4.2.
ST[2:0]	• Connect to GST_[2:0] in (G)MCH Recommend site for a pull up resistor to 1.5 V (4 kΩ to 16 kΩ if populated)	Refer to Section 6.4.2.
WBF	• Connect GWBF# in (G)MCH • Recommend site for a pull up resistor to VDDQ (4 kΩ to 16 kΩ if populated)	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 6.4.2.
VREFCG	• Should be connected to a resistor divider network. This net should be connected to both VDDq and VSS through 1 kΩ, 1% resistors. In addition to this, a 0.1 µF capacitor should be on this net at both (G)MCH and the AGP connector.	

17.3.2 AGP Connector Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
INTA	• Connect PIRQA# in ICH4 • Terminate to 3.3 V through a 8.2 kΩ ± 5% resistor	
INTB	• Connect PIRQB# in ICH4 • Terminate to 3.3 V through a 8.2 kΩ ± 5% resistor	
3.3VAUX	• Connect to PCI 3.3 in VAUX	
VCC3	• Connect to 3.3 V	
12 V	• Connect to 12 V	
VCC	• Connect to 5 V	
VDDQ	• Connect to V_1P5_CORE	
AGPCLK	• Connect through a 33 Ω ± 5% resistor to 3V66_4 in CK408	
GPERR#	• Recommend site for a Pull-up resistor to VDDQ (4 kΩ to 16 kΩ; 6.8 kΩ ± 5% resistor value recommended)	
GSERR#	• Recommend site for a Pull-up resistor to VDDQ (4 kΩ to 16 kΩ; 6.8 kΩ ± 5% resistor value recommended)	
OVRCNT	• No Connect	
PCIRST	• Connect to RST# slot PCI 1, 2, 3	
PME#	• Connect to PME in PCI 1, 2, 3	
TYPEDET#	• No Connect	Signal should either be GROUNDED or NOT CONNECTED on an AGP card. Refer to Section 6.4.2.1.
USB+	• No Connect	5 V tolerant
USB-	• No Connect	5 V tolerant
RSVD	• No Connect	
VREFGC	• No Connect	

17.3.3 AGP Intel® (G)MCH Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
AGP_RCOMP	• Pull-down to GND through a 40.2 Ω ±1% resistor	
VCCAGP	• Connect to 1.5 V power plane	Refer to Section 13.2.4.

17.4 DVO Down / Intel® GMCH Items (Intel® 845GE chipset only)

Checklist Item	Recommendation	Reason/Impact/Documentation
DVOB_CLK	• Connect to GADSTB_0 on GMCH	
DVOB_CLK#	• Connect to GADSTB_0# on GMCH	
DVOC_CLK	• Connect to GADSTB_1 in GMCH	
DVOC_CLK#	• Connect to GADSTB_1# in GMCH	
DVOB_D0	• Connect to GAD_3 on GMCH	
DVOB_D1	• Connect to GAD_2 on GMCH	
DVOB_D2	• Connect to GAD_5 on GMCH	
DVOB_D3	• Connect to GAD_4 on GMCH	
DVOB_D4	• Connect to GAD_7 on GMCH	
DVOB_D5	• Connect to GAD_6 on GMCH	
DVOB_D6	• Connect to GAD_8 on GMCH	
DVOB_D7	• Connect to GC/BE_0# on GMCH	
DVOB_D8	• Connect to GAD_10 on GMCH	
DVOB_D9	• Connect to GAD_9 on GMCH	
DVOB_D10	• Connect to GAD_12 on GMCH	
DVOB_D11	• Connect to GAD_11 on GMCH	
DVOB_HSYNC	• Connect to GAD_0 on GMCH	
DVOB_VSYNC	• Connect to GAD_1 on GMCH	
DVOB_BLANK#	• Connect to GC/BE_1# on GMCH	
DV0BCCLKINT	• Connect to GAD_13 on GMCH	
DVOB_FLDSTL	• Connect to GAD_14 on GMCH	
DVOBCRCOMP	• Pull down through a 40.2Ω 1% resistor connect to AGP_RCOMP on GMCH	
DVOC_D5	• Connect to GC/BE_3# in GMCH	
MI2C_DATA	• Connect to GDEVSEL# in GMCH • Pull-up resistor to VDDQ • May require level shifting	
MDVI_DATA	• Connect to GFRAME# in GMCH • Pull-up resistor to VDDQ • May require level shifting	
MI2C_CLK	• Connect to GIRDY# in GMCH • Pull-up resistor to VDDQ • May require level shifting	
MDDC_CLK	• Connect to G_AD15 in GMCH • Pull-up resistor to VDDQ • May require level shifting	

Checklist Item	Recommendation	Reason/Impact/Documentation
DVOC_D0	• Connect to GAD_19 on GMCH	
DVOC_D1	• Connect to GAD_20 on GMCH	
DVOC_D2	• Connect to GAD_21 on GMCH	
DVOC_D3	• Connect to GAD_22 on GMCH	
DVOC_D4	• Connect to GAD_23 on GMCH	
DVOC_D6	• Connect to GAD_25 on GMCH	
DVOC_D7	• Connect to GAD_24 on GMCH	
DVOC_D8	• Connect to GAD_27 on GMCH	
DVOC_D9	• Connect to GAD_26 on GMCH	
DVOC_D10	• Connect to GAD_29 on GMCH	
DVOC_D11	• Connect to GAD_28 on GMCH	
DVOC_HSYNC	• Connect to GAD_17 on GMCH	
DVOC_VSYNC	• Connect to GAD_16 on GMCH	
DVOC_BLANK	• Connect to GAD_18 on GMCH	
DVOBC_INTR#	• Connect to GAD_30 on GMCH	
DVOBC_FLDSTL	• Connect to GAD_31 on GMCH	
MDDC_DATA	• Connect to GSTOP# in GMCH • May require level shifting	
MDVI_CLK	• Connect to GTRDY# in GMCH • May require level shifting	
ADDID[7:0]	• Connect to GSBA_[7:0] in GMCH	Chipset has integrated pull-ups for these signals.

17.5 Intel® GMCH / DAC Items (Intel® 845PE chipset only)

Checklist Item	Recommendation	Reason/Impact/Documentation
RED	• Connect directly to ground	
RED#	• Connect directly to ground	
GREEN	• Connect directly to ground	
GREEN#	• Connect directly to ground	
BLUE	• Connect directly to ground	
BLUE#	• Connect directly to ground	
REFSET	• Connect directly to ground	
DREFCLK	• Connect directly to ground	
HSYNC	• Leave as No Connect	
VSYNC	• Leave as No Connect	
DDCA_CLK	• Connect directly to ground	
DDCA_DATA	• Connect directly to ground	

17.5.1 DAC Intel® GMCH Only Items (Intel® 845PE chipset only)

Checklist Item	Recommendation	Reason/Impact/Documentation
VCCA_DPLL	• Connect directly to ground	
VCCA_DAC	• Connect directly to ground	
VSSA_DAC	• Connect directly to ground	

17.6 Intel® GMCH / DAC Items (Intel® 845GE chipset only)

Checklist Item	Recommendation	Reason/Impact/Documentation
HSYNC	• Output to VGA connector through a 47 Ω ± 5% resistor	
VSYNC	• Output to VGA connector through a 47 Ω ± 5% resistor	
RED	• Output through pi filter to VGA connector. Terminate to GND through a 75 Ω ± 1% resistor.	
RED#	• Terminate to GND through a 37.4 Ω ± 1% resistor	
GREEN	• Output through pi filter to VGA connector. Terminate to GND through a 75 Ω ± 1% resistor.	
GREEN#	• Terminate to GND through a 37.4 Ω ± 1% resistor	
BLUE	• Output through pi filter to VGA connector. Terminate to GND through a 75 Ω ± 1% resistor.	
BLUE#	• Terminate to GND through a 37.4 Ω ± 1% resistor	
REFSET	• Terminate to GND through a 137 Ω ± 1% resistor	
DREFCLK	• Connect to DOT_48 MHZ in CK_408 through a 33 Ω ± 5% resistor	
DDCA_CLK	• Pull-up to 3.3 V through 2.7 kΩ resistor • Level shift (example: through glue 4) they output to VGA Connector.	
DDCA_DATA	• Pull-up to 3.3 V through 2.7 kΩ resistor • Level shift (example: through glue 4) they output to VGA Connector.	

17.6.1 DAC Intel® GMCH Only Items (Intel® 845GE chipset only)

Checklist Item	Recommendation	Reason/Impact/Documentation
VCCA_DPLL	• Connect to 1.5 V through appropriate LC filter	
VCCA_DAC	• Connect 1.5 V with a 0.1 µF and 0.01 µF capacitor	Refer to Section 7.2.4.
VSSA_DAC	• Connect directly to ground	

17.7 Hub Interface

17.7.1 Hub Interface Intel® (G)MCH / ICH4 Items

Checklist Item	Recommendation	Reason/Impact/Documentation
HI_[10:0]	• Connect to HI[10:0] in ICH4	Refer to Section 8.1.2.
HI_STBS	• Connect to HI_STBS in ICH4	Refer to Section 8.1.1.
HI_STBF	• Connect to HI_STBF in ICH4	Refer to Section 8.1.1.
HI_REF	• Connect to voltage divider circuit	Refer to Section 8.1.4.
HI_SWING	• Connect to voltage divider circuit	Refer to Section 8.1.4.

17.7.2 Hub Interface Intel® (G)MCH Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
HI_RCOMP	• Pull-up to VCC1_5 through a 68.1 Ω ±1% resistor	
VCCHI	• Connect to 1.5 V through (2) 0.1 µF decoupling capacitor. Place near balls: AA1 and AE1	Refer to Section 8.1.

17.7.3 Hub Interface Intel® ICH4 Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
HICOMP	• Terminate to VCC1_5 through a 68.1 Ω ±1% resistor	
HI11	• Terminate to VSS through a 60 Ω ± 5% resistor	

17.8 Miscellaneous Intel® (G)MCH Items

Checklist Item	Recommendation	Reason/Impact/Documentation
PWROK	• Connect to PWRGD_3V in Glue4	Refer to Section 9.
RSTIN#	• Connect to PCIRST# on the ICH4 through a 0 Ω resistor and tie to GND through a 10 pF 5% cap	
RSVD	• No Connect	
VCCGPIO	• Connect to 3.3 V and termination to GND with a 0.1 µF decoupling capacitor	
VCC	• Connect to 1.5 V power plane	Refer to Section 13.2.

17.9 Clock Interface CK_408 Items

Checklist Item	Recommendation	Reason/Impact/Documentation
3V66_0	• Connect to CLKIN in GLUECHIP4 • Connect to a series 33 Ω ± 5% resistor	
3V66_1	• No Connect	
3V66_2	• Connect to GCLKIN in (G)MCH • Connect to a series 33 Ω ± 5% resistor	CLK66 Clock Group Refer to Section 12.1.
3V66_3	• Connect to CLK66 in ICH4 • Connect to a series 33 Ω ± 5% resistor	CLK66 Clock Group Refer to Section 12.1.
3V66_4	• Connect to AGPCLK in AGP • Connect to a series 33 Ω ± 5% resistor	CLK66 Clock Group Refer to Section 12.1.
66_IO	• No Connect	
CPU0	• Connect to BCLK0 in processor • Connect to a series 27.4 Ω ± 1% resistor and terminate to GND through a 49.9 Ω ±1% resistor	Host Clock Group Refer to Section 12.2.1.
CPU0#	• Connect BCLK1 in processor • Connect to a series 27.4 Ω ± 1% resistor and terminate to GND through a 49.9 Ω ±1% resistor	
CPU1	• Connect to ITP_CLK0 in processor • Connect to BCLKP on ITP • Connect to a series 27.4 Ω ± 1% resistor and terminate to GND through a 49.9 Ω ± 1% resistor	Host Clock Group Refer to Section 12.2.1.
CPU1#	• Connect to ITP_CLK1 in processor • Connect to BCLKN on ITP • Connect to a series 27.4 Ω ± 1% resistor and terminate to GND through a 49.9 Ω ± 1% resistor	
CPU2	• Connect to HCLKN in (G)MCH • Connect to a series 27.4 Ω ± 1% resistor and terminate to GND through a 49.9 Ω ±1% resistor	Host Clock Group Refer to Section 12.2.1.
CPU2#	• Connect to HCLKP in (G)MCH • Connect to a series 27.4 Ω ± 1% resistor and terminate to GND through a 49.9 Ω ±1% resistor	Host Clock Group Refer to Section 12.2.1.
CPU_STOP#	• Connect to VCC3_CLK through a 1 kΩ ±5% resistor	Host Clock Group Refer to Section 12.2.1.
DOT_48MHz- (845GE chipset only)	• Connect to DREFCLK in (G)MCH • Connect to a series 33 Ω ± 5% resistor	Refer to Section 12.2.2

Checklist Item	Recommendation	Reason/Impact/Documentation
REF0	• Connect to CLK14 in ICH4 through a series 33 Ω ±5% resistor • Connect to CLK14 in SIO through a series 33 Ω ±5% resistor	Refer to Section 12.2.6.
IREF	• Terminate to GND through a 475 Ω ±1% resistor	Refer to Section 12.2.1.
VSS_IREF	• Terminate to GND	
MULT0	• Connect to VCC3_CLK through a series 10 kΩ ±5% resistor and terminate to GND through a 1 kΩ ±1% resistor	Refer to Section 12.2.1.
PCI0	• Connect to PCICLK on ICH4 • Connect through a series 33 Ω ±5% resistor	PCICLK Group Refer to Section 12.2.7.
PCI1	• Connect to PCI_CLK on SIO • Connect through a series 33 Ω ±5% resistor	
PCI2	• Connect to CLK in FWH • Connect through a series 33 Ω ±5% resistor	
PCI3	No connect	
PCI4	• No connect or slot 4 for ATX MB • Connect through a series 33 Ω ±5% resistor	
PCI5	• No connect or slot 5 for ATX MB • Connect through a series 33 Ω ±5% resistor	
PCI6	• No connect or slot 6 for ATX MB • Connect through a series 33 Ω ±5% resistor	
PCIF[2:0]	• Connect to a series 33 Ω ±5% resistor	PCICLK Group Refer to Section 12.2.7.
PCI_STOP#	• Terminate to VCC3_CLK through a 1 kΩ ±5% resistor	PCICLK Group Refer to Section 12.2.7.
PWRDWN#	• Terminate to VCC3_CLK through a 1 kΩ ±5% resistor	
SEL_[1:0]	• SEL0 terminate to VCC3_CLK through a 1 KΩ ± 5% resistor and terminate to GND through a series 0 Ω resistor. SEL1 connect to (G)MCH	
SEL_2	• Terminate to GND through a 1 kΩ ±5% resistor	
SCLK	• Connect to SCL in DIMMs	
SDATA	• Connect to SDA in DIMMs	
USB_48Mhz	• Connect to CLK48 in ICH4 through a series 33 Ω ±5% resistor	
VDD	• Terminate to VCC3_CLK	

Checklist Item	Recommendation	Reason/Impact/Documentation
VDD_48MHz	• Terminate to VCC3 through a 10 Ω ±5% resistor and terminate to GND through two parallel capacitor	
VDDA	• Terminate to VCC3 and terminate to GND through two parallel capacitor	
VSS	• Terminate to GND	
VSS_48MHz	• Terminate to GND	
VSSA	• Terminate to GND	
VTT_PWRGD#	• Refer to DDR CRB for example	
XTAL_IN	• Terminate to GND through a 10 pF ±5% capacitor	Capacitor values may vary slightly from manufacturer to manufacturer.
XTAL_OUT	• Terminate to GND through a 10 pF ±5% capacitor	Capacitor values may vary slightly from manufacturer to manufacturer.

17.10 Intel® ICH4 Interface

17.10.1 Intel® ICH4 IDE Items

Checklist Item	Recommendation	Reason/Impact/Documentation
IDERST#	• The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal.	
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.
PDD[15:0], SDD[15:0]	No extra series termination resistors or other pull-ups/pull-downs are required. • PDD7/SDD7 does not require a 10 kΩ pull-down resistor. Refer to ATA ATAPI-6 specification.	These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.
PDDREQ, SDREQ	• No extra series termination resistors. • No pull down resistors needed.	These signals have integrated series resistors in the ICH4. These signals have integrated pull down resistors in the ICH4.

Checklist Item	Recommendation	Reason/Impact/Documentation
PIORDY, SIORDY	• No extra series termination resistors. • Pull-up to VCC3_3 via a 4.7 kΩ resistor.	These signals have integrated series resistors in the ICH4.
IRQ14, IRQ15	Recommend 8.2 kΩ–10 kΩ pull-up resistors to VCC3_3. No extra series termination resistors.	Open drain outputs from drive.
Cable Detect:	**Host Side/Device Side Detection (*recommended method*):** Connect IDE pin PDIAG#/CBLID to an ICH4 GPIO pin. Connect a 10 kΩ resistor to terminate to GND on the signal line. **Device side detection:** Connect a 0.047 µF capacitor from IDE pin PDIAG#/CBLID to terminate to GND. No ICH4 connection.	The 10 kΩ resistor to GND prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. **NOTE:** All Ultra DMA drives supporting modes greater than Mode 2 will have the capability to detect cables

17.10.2 Intel® ICH4 AC '97 Items

Checklist Item	Recommendation	Reason/Impact/Documentation
AC_SDOUT	• Requires a jumper to 8.2 kΩ Pull Up resistor. Should not be stuffed for default operation. • Series termination resistor 0 Ω to 47 Ω to on board codec and to the CNR	This pin has a weak internal 20 kΩ nominal pull down. To properly detect a safe_mode condition a strong pull up will be required to over-ride this internal pull down.
AC_SDIN1, AC_SDIN0	• Internal pull-downs in ICH4; no external pull-downs required. • Series termination resistor 0 Ω to 47 Ω from the AC_SDIN lines to the ICH4	These pins have a weak internal 20 kΩ nominal pull-down.
AC_SDIN2	• Requires a 10K pull-down to ground if a CNR card is used on the platform. • Series termination resistor 33 Ω to 47 Ω from the AC_SDIN lines to the ICH4.	This pin has a weak internal 20 kΩ nominal pull-down. For platforms routing AC_SDIN2 to CNR the additional 10 kΩ pull-down is required to set the proper DC level for CNR card switching circuitry. Used for a codec detection/addressing mechanism on the CNR card.
AC_BITCLK	• No extra pull-down resistors required. • Series termination resistor 33 Ω to 47 Ω from the motherboard codec to the ICH4 and also to the CNR	This pin has a weak internal 20 kΩ nominal pull-down.
AC_SYNC	• No extra pull-down resistors required.	Some implementations add termination for signal integrity. Design specific.

17.10.3 Intel® ICH4 USB Items

Checklist Item	Recommendation	Reason/Impact/Documentation
USBRBIAS	• 22.6 Ω ±1% connected to ground	
USBRBIAS#	• Connected to the same 22.6 Ω ±1% resistor to ground as USBRBIAS	
USBP[5:0]P, USBP[5:0]N	• No external resistors are required.	Effective output driver impedance of 45 Ω provided
OC[5:0]#	• If not used, use 10 kΩ ±5% to VccSus3_3	Inputs must not float
Unconnected USB data signals	• Unconnected USB data signals can be left as no-connects	

17.10.4 Intel® ICH4 Interrupt Interface Items

Checklist Item	Recommendation	Reason/Impact/Documentation
PIRQ[D:A]#	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull up resistor to VCC5 or 8.2 kΩ ±5% to VCC3_3.	In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering Section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the ISA interrupts.
PIRQ[H:E]#/ GPIO[5:2]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull up resistor to VCC5 or 8.2 kΩ ±5% to VCC3_3.	In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering Section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees the ISA interrupts.
SERIRQ	• External weak (8.2 kΩ) pull up resistor to VCC3_3 is recommended.	Open drain signal.

Checklist Item	Recommendation	Reason/Impact/Documentation
APIC	**If the APIC is used:** 150 Ω pull-up resistors on APICD[1:0] Connect APICCLK to clock generator with a 20 Ω – 33 Ω series termination resistor. • **If the APIC is not used on up systems** The APICCLK should be tied directly to GND. Pull APICD[1:0] to GND through a 10 kΩ pull-down resistor. If using XOR chain testing, a pull-down for each APIC signal is required (i.e., two 10 kΩ pull-down resistors).	

17.10.5 Intel® ICH4 System Bus / SMLink Interface Items

Checklist Item	Recommendation	Reason/Impact/Documentation
SMBDATA, SMBCLK	Require external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.) Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. Required to be tied to SMLink signals for SMBus 2.0 compliance. SMBCLK should be tied to SMLINK0 and SMBDATA should be tied to SMLINK1	Value of pull-ups resistors determined by line load.
SMBALERT#/ GPIO11	See GPIO section if SMBALERT# not implemented.	
SMLINK[1:0]	Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.) Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. Required to be tied to SMLink signals for SMBus 2.0 compliance. SMBCLK should be tied to SMLINK0 and SMBDATA should be tied to SMLINK1	Value of pull-ups resistors determined by line load.
INTRUDER#	Pull signal to VCCRTC (VBAT) through 10 kΩ resistor.	Signal in VCCRTC (VBAT) well.

17.10.6 Intel® ICH4 PCI Interface Items

Checklist Item	Recommendation	Reason/Impact/Documentation
FYI	All inputs to the ICH4 must not be left floating	Many GPIO signals are fixed inputs that must be pulled up to different sources. See GPIO section for recommendations.
PERR#, SERR#, PLOCK#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#, REQ[4:0]#, GPIO0/REQA#, GPIO1/REQB#/ REQ5	• These signals require a pull up resistor. Recommend an 8.2 kΩ pull up resistor to VCC3_3 or a 2.7 kΩ pull up resistor to VCC5.	See PCI 2.2 Component Specification pull-up recommendations for VCC3_3 and VCC5.
PCIGNT[4:0]#	• No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented they must be pulled up to VCC3_3.	These signals are actively driven by the ICH4
GNTA# /GPIO16, GNTB/GNT5#/ GPIO17	• No extra pull-up needed	These signals have integrated pull-ups of 24 kΩ. GNTA has an added strap function of “top block swap”. The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull down resistor can be added to manually enable the function.
PCIRST#	• The PCIRST# signal should be buffered to form the IDERST# signal 33 Ω series resistor to IDE connectors.	Improves Signal Integrity
PME#	• No extra pull-up needed	This signal has integrated pull-up of 18 kΩ to 42 kΩ.
IDSEL (on PCI Connector	• If connected must have a 300 Ω to 900 Ω series termination resistor	

17.10.7 Intel® ICH4 RTC Items

Checklist Item	Recommendation	Reason/Impact/Documentation
VBIAS	• The VBIAS pin of the ICH4 is connected to a 0.047 µF cap.	For noise immunity on VBIAS signal
RTCX1, RTCX2	• Connect a 32.768 kHz Crystal Oscillator across these pins with a 10 MΩ resistor and use 18 pF decoupling caps at each signal (based on a crystal load of 12.5 pF).	The ICH4 implements new internal oscillator circuit as compared with the PIIX4 to reduce power consumption. The external circuitry shown in the DG will be required to maintain the accuracy of the RTC. The circuitry is required because the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.
RTCRST#	• Time constant due to RC filter on this line should be 18–25 ms. Recommended value for Resistor = 180 kΩ and Capacitor is 0.1 µF	Timing Requirement.

17.10.8 Intel® ICH4 LAN Items

Checklist Item	Recommendation	Reason/Impact/Documentation
LANCLK	• Connect to LAN_CLK on platform LAN connect device.	ICH4 contains integrated 100 kΩ nominal pull-down resistor on signal.
LANRXD[2:0]	• Connect to LAN_RXD on platform LAN connect device.	ICH4 contains integrated 10 kΩ pull-up resistors on interface.
LANTXD[2:0], LANRSTSYNC	• Connect to LAN_TXD on platform LAN connect device.	
If the LAN connect Interface is not used	• Platform LAN connect interface can be left NC if not used.	Input buffers internally terminated.
82540EM and 1000Base-T designs if applicable		Refer to DG Section 9.10.2.

17.10.9 Intel® ICH4 FWH/LPC Interface Items

Checklist Item	Recommendation	Reason/Impact/Documentation
FWH[3:0]/ LAD[3:0], LDRQ[1:0]	• No extra pull-ups required. Connect straight to FWH/LPC.	ICH4 Integrates 20 kΩ nominal pull-up resistors on these signal lines.
FWH Decoupling	• Follow Vendor recommendation	

17.10.10 Intel® ICH4 EEPROM Interface Items

Checklist Item	Recommendation	Reason/Impact/Documentation
EE_DIN	• No extra circuitry required. • Connect to EE_DOUT of EEPROM or CNR Connector.	ICH4 contains integrated 20 kΩ nominal pull-up resistor for this Signal. Connected to EEPROM data output signal. (Output from EEPROM perspective and input from ICH4 perspective.)
EE_DOUT	• Prototype Boards using internal LAN should include a placeholder for a pull-down resistor on this signal line, but do not populate the resistor. • Connect to EEDIN of EEPROM or CNR Connector.	ICH4 contains integrated 20 kΩ nominal pull-up resistor for this Signal. Connected to EEPROM data input signal (Input from EEPROM perspective and output from ICH4 perspective.)

17.10.11 Intel® ICH4 Power Management Items

Checklist Item	Recommendation	Reason/Impact/Documentation
LAN_RST#	• Recommend a 10 kΩ pull-down to ground. • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Can be tied to RSMRST#.	Timing Requirement.
PWRBTN#	• No extra pull-up resistors	This signal has an integrated pull-up of 18 kΩ – 42 kΩ. This signal is internally debounced inside the ICH4.
PWROK	• Recommend a 10 kΩ pull-down to ground. • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both Vcc3_3 and VCC1_5 have reached their nominal voltages	Timing Requirement.

Checklist Item	Recommendation	Reason/Impact/Documentation
RI#	• RI# does not have an internal pull-up. Recommend an 8.2 kΩ pull-up resistor to Resume well.	If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.
RSMRST#	• Recommend a 10 kΩ pull-down to ground. • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Can be tied to LAN_RST#.	Timing Requirement.
SLP_S3#, SLP_S4#, SLP_S5#	• No pull up/down resistors needed. Signals driven by ICH4.	Signals driven by ICH4.
SYS_RESET#	• Recommend an 8.2 kΩ pull-up resistor to VccSus3_3. Also a (100 Ω to 8.2 kΩ) pull-down resistor isolated from SYS_RESET# by means of a normally open switch	Input to ICH4 cannot float. This pin forces an internal reset to the ICH4 after the signal is internally debounced.
THRM#	• Connect to temperature Sensor. Pull up if not used (an 8.2 KΩ pull up resistor to VCC3_3).	Input to ICH4 cannot float. THRM# polarity bit defaults THRM# to active low, so pull up.
THRMTRIP#	• A weak (62 Ω ±5%) pull-up resistor to the V_CPU_IO well. See processor design guide for specific pull-up value	Input to ICH4 cannot float.
GPIO[24]	• No pull-up required.	

17.10.12 Processor Items

Checklist Item	Recommendation	Reason/Impact/Documentation
A20M#, CPU_SLP#, IGNNE#, INTR, NMI, SMI#, STPCLK#	• Pull-up resistor to VCCCPU required if input to V_CPU_IO ≤ 0.8 V.	Push/pull buffers now drive the output signals.
INIT#		See Section 4.3.1.
FERR#	• Requires weak (62 Ω ±5%) external pull-up resistor to V_CPU_IO.	
RCIN#, A20GATE	• Pull up signals to VCC3_3 through a 10 kΩ resistor.	Typically driven by Open Drain External Micro-controller.
CPUPWRGD	• Connect to the CPU's CPUPWRGD input. Requires weak external pull-up resistor.	Refer to processor documentation of the processor for specific values. This signal represents a logical AND of the ICH4's PWROK and VRMPWRGD signals.

17.10.13 Intel® ICH4 GPIO Items

Checklist Item	Recommendation	Reason/Impact/Documentation
GPIO Pins	**GPIO[7:0]:** • These pins are in the Main Power Well. Pull-ups must use the VCC3_3 plane. • Unused core well inputs must be pulled up to VCC3_3. • GPIO[1:0] can be used as REQ[B:A]#. • GPIO1 can be used as PCI REQ5#. • GPIO[5:2] can be used as PIRQ[H:E]#. • GPIO6 • These signals are 5 V tolerant • These pins are inputs **GPIO8 & [13:11]:** • These pins are in the Resume Power Well. Pull-ups go to VccSus3_3 plane. • Unused resume well inputs must be pulled up to VccSus3_3. • These signals are **NOT** 5 V tolerant. • GPIO11 can be used as SMBALERT#. • These pins are inputs **GPIO[23:16]:** • Fixed as output only. Can be left NC. • GPIO22 is open drain. • GPIO[17:16] can be used as GNT[B:A]#. • GPIO17 can be used as PCI GNT5#. • GPIO18 • GPIO19 • GPIO20 • GPIO21 • GPIO22 • GPIO23 • These signals are **NOT** 5 V tolerant **GPIO[28, 27, 25, 24]:** • I/O pins. Default as outputs so can be left as NC • These pins are in the Resume Power Well • GPIO[28:27, 25] From resume power well. (Note: use pull-up to VccSus3_3 if these signals are pulled_up) • GPIO24: No pull-up required • These signals are **NOT** 5 V tolerant **GPIO[43:32]:** • I/O pins. From main power well. • Default as outputs. • These signals are **NOT** 5 V tolerant.	*Ensure ALL unconnected signals are OUTPUTS ONLY!*

17.10.14 Intel® ICH4 Miscellaneous Items

Checklist Item	Recommendation	Reason/Impact/Documentation
SPKR	• Refer to Section 9.2.3	Has integrated pull-down. The integrated pull-down is only enabled at boot/reset for strapping functions; at all other times, the pull-down is disabled.
TP0	• Requires external pull-up resistor to VccSus3_3	

17.11 Platform Power and Ground

17.11.1 Intel® ICH4 Power and Ground Items

Checklist Item	Recommendation	Reason/Impact/Documentation
HI_REF	• 350 mV (See voltage divider recommendations in the HI section of this DG)	
VCC3_3	• Use six 0.1 µF decoupling cap	
VCC1_5	• Use two 0.1 µF decoupling caps	
V5_REF	• Use one 0.1 µF decoupling cap • V5_REF is the reference voltage for 5 V tolerant inputs in the ICH4. V5_REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3.	
VccSus3_3	• Use two 0.1 µF decoupling caps	
VccSus1_5	• Use two 0.1 µF decoupling caps	
V5_REF_SUS	• Use one 0.1 µF decoupling cap • V5REF is the reference voltage for 5 V tolerant inputs in the ICH4. V5_REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3. For most platforms this is not an issue because VccSus3_3 is usually derived from V5_REF_Sus.	
V_CPU_IO[2:0]	• Connect to the proper power plane for the processor's CMOS compatibility signals. • Connect one 0.1 µF decoupling capacitor	Used to pull up all processor interface signals.
VccPLL	• Use one 0.1 µF decoupling cap and one 0.01 µF decoupling cap.	
VccHI	• Use two 0.1 µF decoupling caps.	

Checklist Item	Recommendation	Reason/Impact/Documentation
VccRTC	• No clear CMOS jumper on VccRTC. • Use a jumper on RTCRST# or a GPI, or use a safe mode strapping for Clear CMOS. • Use one 0.1 µF decoupling cap.	
VSS	• Connect to GND.	

Appendix A: Customer Reference Board Schematics

This appendix provides a set of example schematics for the FMB2 VR implementation of Intel® Pentium 4 processor in 478-pin package with an Intel 845GE chipset platform Customer Reference Board (CRB).

Intel® 845GE Chipset FMB2 Schematics (Three Phase VR implementation)

Refer to the following pages for schematics on the FMB2 three phase VR implementation.

Intel® 845GE Chipset FMB2 Schematics (Four Phase VR implementation)

The FMB2 four phase VR implementation schematic pages follow the schematic pages for the three phase VR implementation.

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PAGE #	COMPONENT/FUNCTION
1	COVER PAGE.
2	TABLES: BLOCK DIAGRAM
3	TABLES: RESET MAP
4	TABLES: CLOCK DISTRIBUTION
5	TABLES: GPIO/IDSEL MAPPING
6	TABLES: VOLTAGE DISTRIBUTION
7	CORE: CK_408 (MAIN CLOCK GENERATOR)
8	CORE: CPU CONNECTOR
9	CORE: CPU PULLUPS & PULLDOWNS /VCCPVID, VCC_VIDSEL
10	CORE: CPU ANALOG FILTER
11-13	CORE: INTEL(R) 845G GMCH
14	BLANK
15	CORE: INTEL(R) 845G DECOUPLING & REFERENCE VOLTAGES
16	CORE: DDR SERIES TERMINATION
17	CORE: DIMM CONNECTORS
18-19	CORE: DDR PARALLEL TERM (STROBES, CNTL)
20	CORE: DDR VTERM CAPS
21	CORE: AGP SLOT & AGP PULL-UPS/PULL-DOWNS
22	CORE: VGA CONNECTOR
23-24	ICH: 82801DB I/O CONTROLLER HUB
25	ICH: ICH PULL-UP/PULL-DOWNS
26	ICH: LAN LINK
27	ICH: IDE PRIMARY & SECONDARY
28	ICH: USB BACK PANEL CONNECTORS
29	BLANK
30	ICH: USB FRONT PANEL/CNR VREG & OC#,
31-33	ICH: PCI SLOTS 3 - 1
34	ICH: PCI PULL-UPS
35	SMBUS ISOLATION
36	CNR CONNECTOR
37	BLANK
38	AUDIO: CODEC (AD1885 OR CS4201)
39	AUDIO: CODEC FILTERING CAPS
40	AUDIO: AUX-IN, CD-IN, LINE-IN: ATAPI HEADERS
41	AUDIO: MIC-IN
42	AUDIO: LINE-OUT
43	AUDIO: FRONT PANEL AUDIO HEADER
44	AUDIO: TRANSIENT CONTROL
45	AUDIO: ANALOG VREG
46	SIO: LPC47M102
47	SIO: FLOPPY
48	SIO: KEYBOARD & MOUSE PORTS (PS/2)

PAGE #	COMPONENT/FUNCTION
49	SIO: PARALLEL PORT
50	SIO: COM1
51	FWH: MFG MODE AND RECOVERY JUMPERS
52	GLUE4
53	HECETA4 & HECETA6
54	PC SPEAKER
55	FRONT PANEL HEADER
56	LABELS / MOUNTING HOLES
57	FAN: FAN HEADERS (3)
58	VREG: 2.5V MEMORY, STANDBY-MEMORY
59	VREG: 1.25V MEMORY VTT
60	VREG: POWER CONNECTOR 2X10
61	VREG: BATTERY, PCI VAUX, USB_NCH & USB_PCH
62	VREG: USB BACK PANEL, PS/2
63	VREG: 1.5V STBY & 3.3V STBY
64	VREG: BULK DECOUPLING
65	VREG: 2.5V STR DECOUPLING
66	VREG: CORE 1.5V
67	VREG: CPU MAIN REGULATOR (VCCP)
68	VREG: CPU DECOUPLING, 12V CONN/FILTER INDUCTOR
69	DCL TRACK SPLITTERS
70	BLANK
71	DEBUG: ITP PORT AND PULL-UPS
72	MOON ISA RESISTORS
73-74	BLANK
75	DEBUG: PORT80 DECODER

INTEL(R) 845GE DDR SCHEMATICS REV 2.0

POWER SYMBOLS USED:

VCC3

VCC

+12V

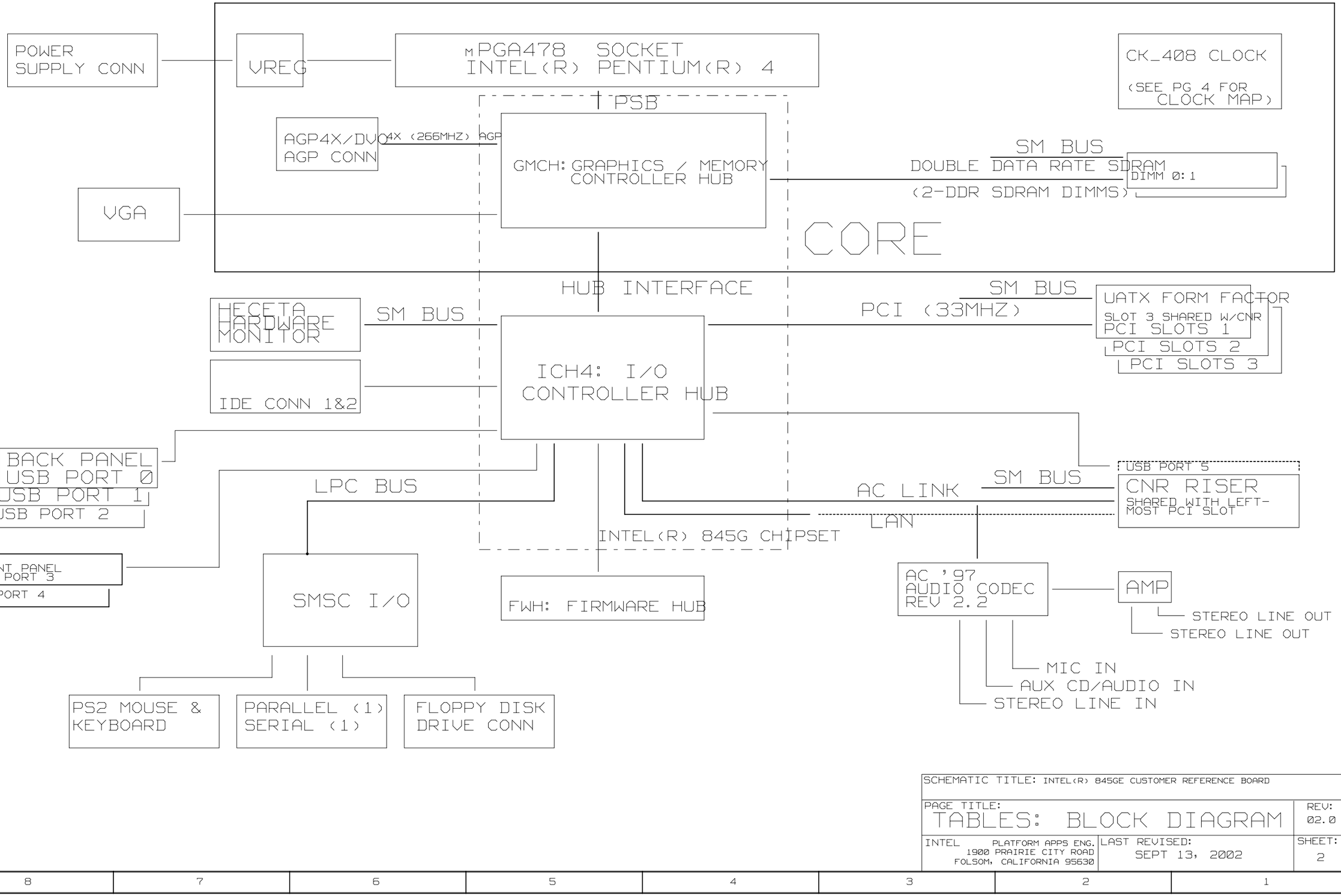
-12V

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPL'S FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5 VOLTS UNLESS OTHERWISE SPECIFIED.
4. VCC3 = +3.3 VOLTS UNLESS OTHERWISE SPECIFIED.
5. * SUFFIX INDICATES ACTIVE LOW SIGNAL.

INTEL(R) PENTIUM(R) 4 SKT-N/INTEL(R) 845GE CUSTOMER REFERENCE BOARD (CRB) 2-DDR SDRAM, 4 LAYER, UATX

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: COVER PAGE		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 1



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PAGE TITLE: TABLES: BLOCK DIAGRAM

REV: 02.0

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SHEET: 2

CORE

GMCH: GRAPHICS/MEMORY CONTROLLER HUB
RSTIN*
PWROK
H_CPURST*

RESET*
MPGA478 SOCKET
H_PWRGD

P_PCIRST*

FWH_RST*
FWH; FIRMWARE HUB

SIO_PCI_RST*
SMC I/O
KBRST*

POWER SUPPLY CONN
PS_ON* PWRGD_PS

H_PWRGD
P_RST_SLOTS*
AUD_RST*
P_PCIRST*
PWRGD_PS
PWRGD_3V
RSMRST*
PS_ON*
GLUECHIP4
FP_RST*
IDE_RST*
SLP_S5*
SLP_S3*

RSMRST*

IDE_RST*
IDE CONN1
IDE CONN2

SLOTS_P_RST*
PCI SLOT 1
PCI SLOT 2
PCI SLOT 3

SLOTS_P_RST*
AGP4X
AGP CONN
CORE

PORT 80
BUFFER
P_PCIRST_DEBUG*

CPU: DBRESET (ITP)
DBR*
CORE

FWH
WAKE USB

AC97 AUDIO CODEC
AUD_LINK_RST*
RES (OPTION)
DYNAMIC PRIMARY DOWN CNTL

CNR(SHARED SLOT)
AUD_LINK_RST*
ICH_LAN_RST

FRONT PANEL CONN
FP_RST*
SW_ON*

PWRGD_3V
RSMRST*
H_PWRGD
SYS_RST*
ICH4: I/O CONTROLLER HUB
SW_ON*
KBRST*
P_PCIRST*
AUD_LINK_RST*
ICH_LAN_RST
SLP_S5*
SLP_S4*
SLP_S3*

VREG: USB
FRNT: LED

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD			
PAGE TITLE: RESET MAP			REV: 02.0
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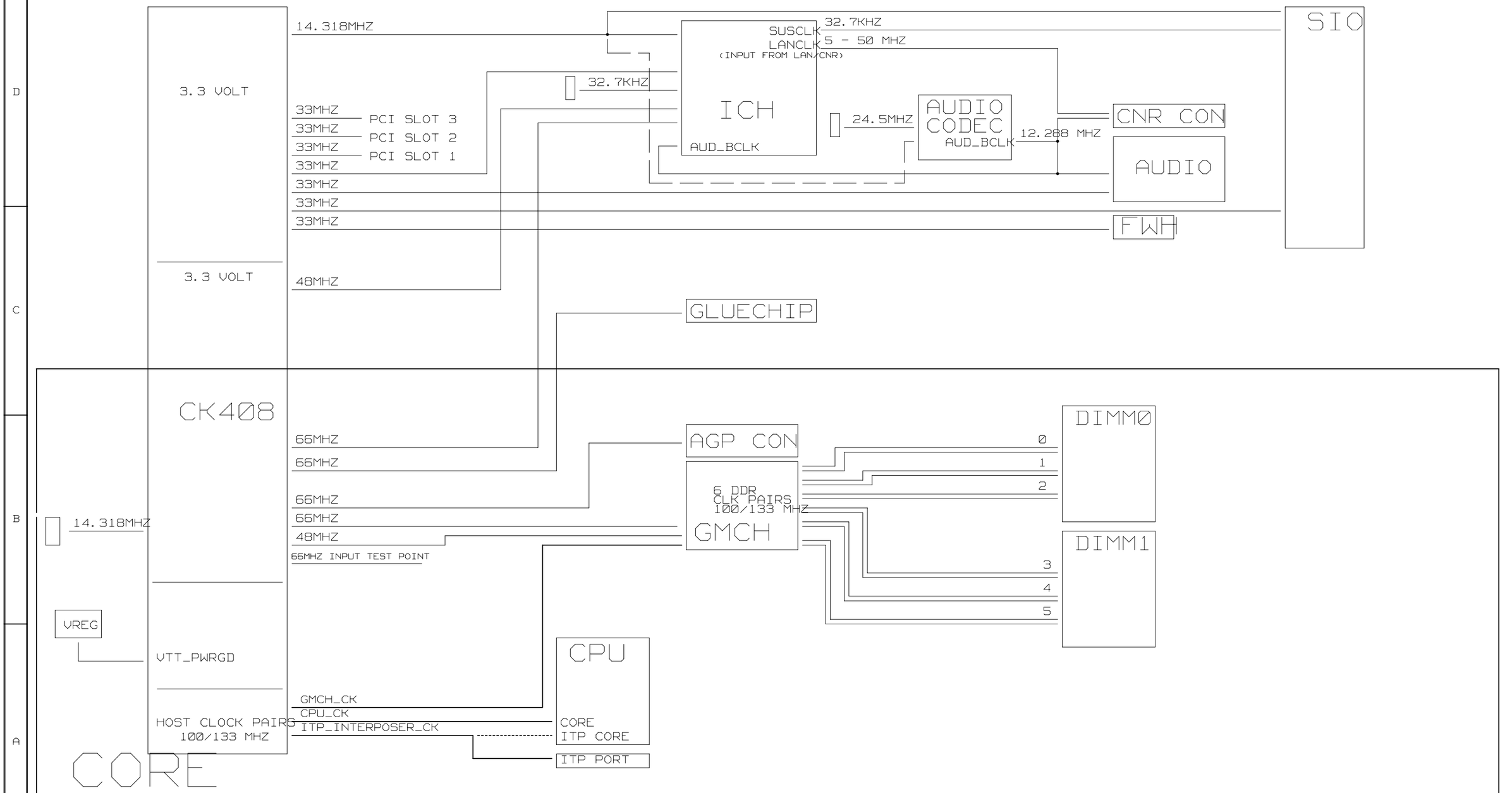

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PAGE TITLE: CLOCK DISTRIBUTION

REV: 02.0

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: SEPT 13, 2002

SHEET: 4

ICH4

	PIN NAME	PWR WELL	USAGE	DURING RESET	S3/S4/S5	INTERNAL PULL-UP	NOTES
	GPI(0)	CORE	P_REQA#	---	---		
	GPI(1)	CORE	P_REQ5#	---	---		
	GPI(2)	CORE	P_IRQE#	---	---		
	GPI(3)	CORE	P_IRQF#	---	---		
	GPI(4)	CORE	P_IRQG#	---	---		
	GPI(5)	CORE	P_IRQH#	---	---		
	GPI(6)	CORE	UNUSED	---	---		
	GPI(7)	CORE	UNUSED	---	---		
	GPI(8)	RESUME	UNUSED	---	---		
	GPI(11)	RESUME	SMB_ALERT#	---	---		
	GPI(12)	RESUME	LPC_SIO_SMI#	---	---		
	GPI(13)	RESUME	LPC_SIO_PME#	---	---		
	GPO(16)	CORE	P_GNTA#	HIGH	OFF	24K	
	GPO(17)	CORE	P_GNT5#	HIGH	OFF	24K	
	GPO(18)	CORE	UNUSED	HIGH	OFF		
	GPO(19)	CORE	UNUSED	HIGH	OFF		
	GPO(20)	CORE	UNUSED	HIGH	OFF		
	GPO(21)	CORE	ISA_GO_NOGO	HIGH	OFF		
	GPO(22)	CORE	UNUSED	HIGH-Z	OFF		
	GPO(23)	CORE	UNUSED	LOW	OFF		
	GPIO(24)	RESUME	UNUSED	LOW	DEFINED		
	GPIO(25)	RESUME	GPO_GRN_BLNK	HIGH	DEFINED		
	GPIO(27)	RESUME	GPO_YEL_BLNK	HIGH	DEFINED		
	GPIO(28)	RESUME	GPO_LAN_DISABLE	HIGH	DEFINED		
	GPIO(32)	CORE	NO_POP*	HIGH	OFF		
	GPIO(33)	CORE	UNUSED	HIGH	OFF		
	GPIO(34)	CORE	UNUSED	HIGH	OFF		
	GPIO(35)	CORE	UNUSED	HIGH	OFF		
	GPIO(36)	CORE	UNUSED	HIGH	OFF		
	GPIO(37)	CORE	(BOARD1)	HIGH	OFF		
	GPIO(38)	CORE	(BOARD2)	HIGH	OFF		
	GPIO(39)	CORE	(BOARD3)	HIGH	OFF		
	GPIO(40)	CORE	(BOARD4)	HIGH	OFF		
	GPIO(41)	CORE	UNUSED	HIGH	OFF		
	GPIO(42)	CORE	UNUSED	HIGH	OFF		
	GPIO(43)	CORE	CDC_DWN_ENAB*	HIGH	OFF		
	RI*	RESUME					
	THERM*	CORE					

FWH

GPI4		CONFIG JUMPER	INPUT	DEFINED		CONFIG JUMPER
GPI3		MANUF MODE	INPUT	DEFINED		MANUF MODE
GPI2		HI/LOW BIOS CONFIG	INPUT	DEFINED		SPARE HI/LOW BIOS CONFIG STRAP
GPI1		GPIO_DMA66_DETECT_SEC	INPUT	DEFINED		ATA66 CABLE DETECT - SECONDARY
GPI0		GPIO_DMA66_DETECT_PRI	INPUT	DEFINED		ATA66 CABLE DETECT - PRIMARY

SIO

GPIO20		RESISTOR STRAP OPTION	INPUT	DEFINED		DESIGN FEATURE WITH RESISTOR STRAPPING
GPIO21		RESISTOR STRAP OPTION	INPUT	DEFINED		DESIGN FEATURE WITH RESISTOR STRAPPING
GP027/IOSMI*		IO_SMI*	INPUT	DEFINED		SENDS IO SMI REQUEST TO ICH2

MULTI-PLEXED GPIO PINS ON SIO USED FOR SPECIFIC FUNCTIONS (NOT AS GPIO) ARE NOT IDENTIFIED HERE
UN-USED GPIO PINS ON SIO ARE NOT IDENTIFIED HERE

IRQ ROUTING TABLE

	AGP	SLOT1	SLOT2	SLOT3	AC97/ SMBUS	LAN
INT A	A			D		
INT B	B			C	A	
INT C				A		
INT D				B		
INT E		D	C			A
INT F		A	B			
INT G		B	A			
INT H		C	D			
REG /GNT						
IDSEL		16	17	18		24

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: GPIO, IRQ, IDSEL MAPS		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 5

GMCH

ATX P/S WITH 1A 5VSB

5VSB

5V

3.3V

+12V

-12V

ATX 12V P/S

+12V

+12V

VRM 9.0
PG 67,68

VCC_VID
VREG
PG 9

1.5V
REGULATOR
PG 66

V_1P5_CORE

V_2P5_CORE

2.5V
REGULATOR
PG 58

VCC

VSB
REGULATOR

PG 58

V_2P5_SM

1.25V
REGULATOR
PG 59

V_1P25_MEMVTT

1.5VSB
REGULATOR
PG 63

V_5P0_STBY

V_1P5_STBY

3.3VSB
REGULATOR
PG 63

V_5P0_STBY

V_3P3_STBY

OR

BATTERY
PG 61

V_3P3_STBY

PG 61

VCC3

V_3P3_STBY

V_3P3_PCIAUX

PG 30

VCC

V_USB_PWR_CNR

PG 62

V_5P0_STBY

VCC

AUDIO
SPO
PG 45

+12V

GMCH VTT
PSB I/O:
1.15-1.75V
2.4 A
S0, S1

MPGA478
VCCP
60 A, S0, S1
VCC_VID
30 MA, S0, S1

ICH4
VCCCPU-VRM OUT
?MA
S0, S1

VCCCORE:
CORE LOGIC:
1.5V
1.06 A
S0, S1

VCCHI:
HI I/O:
1.5V
90 MA
S0, S1

VCC3_3:
3.3V
610 MA
S0, S1

VCCSUS1_5-ICH
RESUME:
1.5V
85 MA S0, S1
85 MA S3, S5

VCCSUS3_3-ICH
RESUME:
3.3V
70 MA S0, S1
70 MA S3, S5

VCCRTC-ICH RTC:
VBAT
5UA
S0, S1, S3, S5

VCCHI, HI I/O:
1.5V
90 MA, S0, S1

VCC, CORE LOG.
1.5V
2.46 A, S0, S1

VCCAGP, AGP I/O
1.5V
370 MA, S0, S1

VCCDAC, DAC I/O
1.5V
65 MA, S0, S1

VCCGPIO
3.3V
30 MA, S0, S1

VCCSM, DDR I/O
2.5V
0.8 A S0, S1
95 MA S3

DDR 2 DIMMS:
2.5V
5.402 A S0, S1
138 MA S3

DDR VTT
1.25V
2.1 A S0, S1
0 MA S3

PCI PER SLOT:
3.3V 7.6 A
5V 5 A
+12V 0.5 A
-12V 0.1 A

PCI 3.3VAUX
PER SLOT:
3.3V
1A S0, S1
475MA S3, S5

CNR CONNECTOR POWER:
3.3V 1 A
3.3V 1 A DUAL
5V 1 A
5V 0.5 A DUAL
+12V 0.5 A
112V 0.1 A

CK_408:
3.3V
280 MA S0, S1

LPC SUPER I/O:
3.3V
25 MA S0, S1

FWH CORE:
3.3V
67MA S0, S1

USB AND PS/2 CABLE
POWER:
5V
500MA * 6 S0, S1
1MA S3, S5

AC'97 AUDIO CODEC:
5V
?A S0, S1
0A S3, S5

AGP CONNECTOR
1.5V 2.0A
3.3V 6A
5V 2A
+12V 1A

VCC3

V_3P3_STBY

VCC3

VREG_USB_BPL
VREG_USB_BPR
VREG_PS2

VCC3

+12V

VCC3

VCC

V_5P0_STBY

-12V

+12V

VCC3

VCC

V_5P0_STBY

-12V

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD

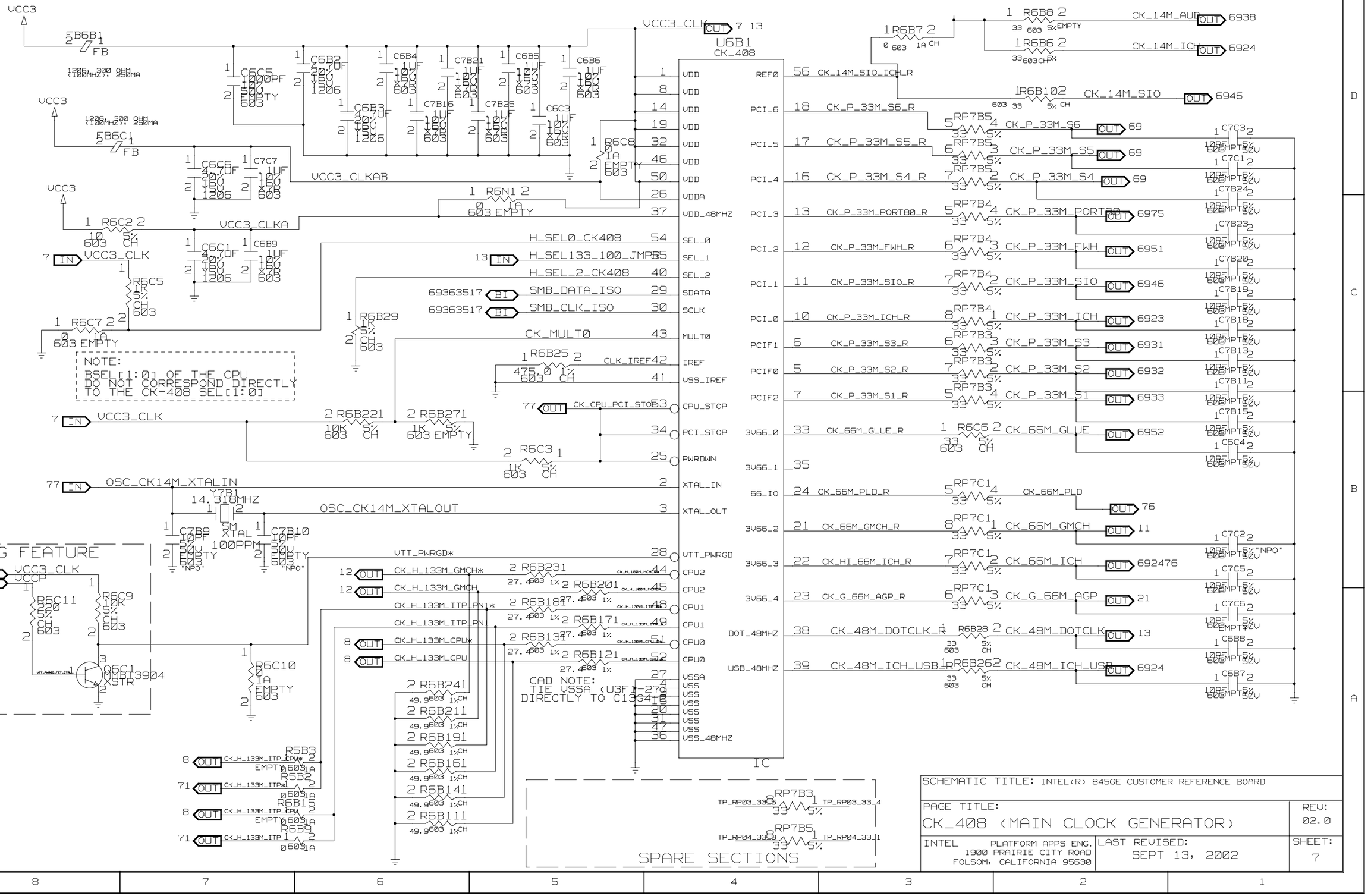
PAGE TITLE: VOLTAGE DISTRIBUTION

REV: 02.0

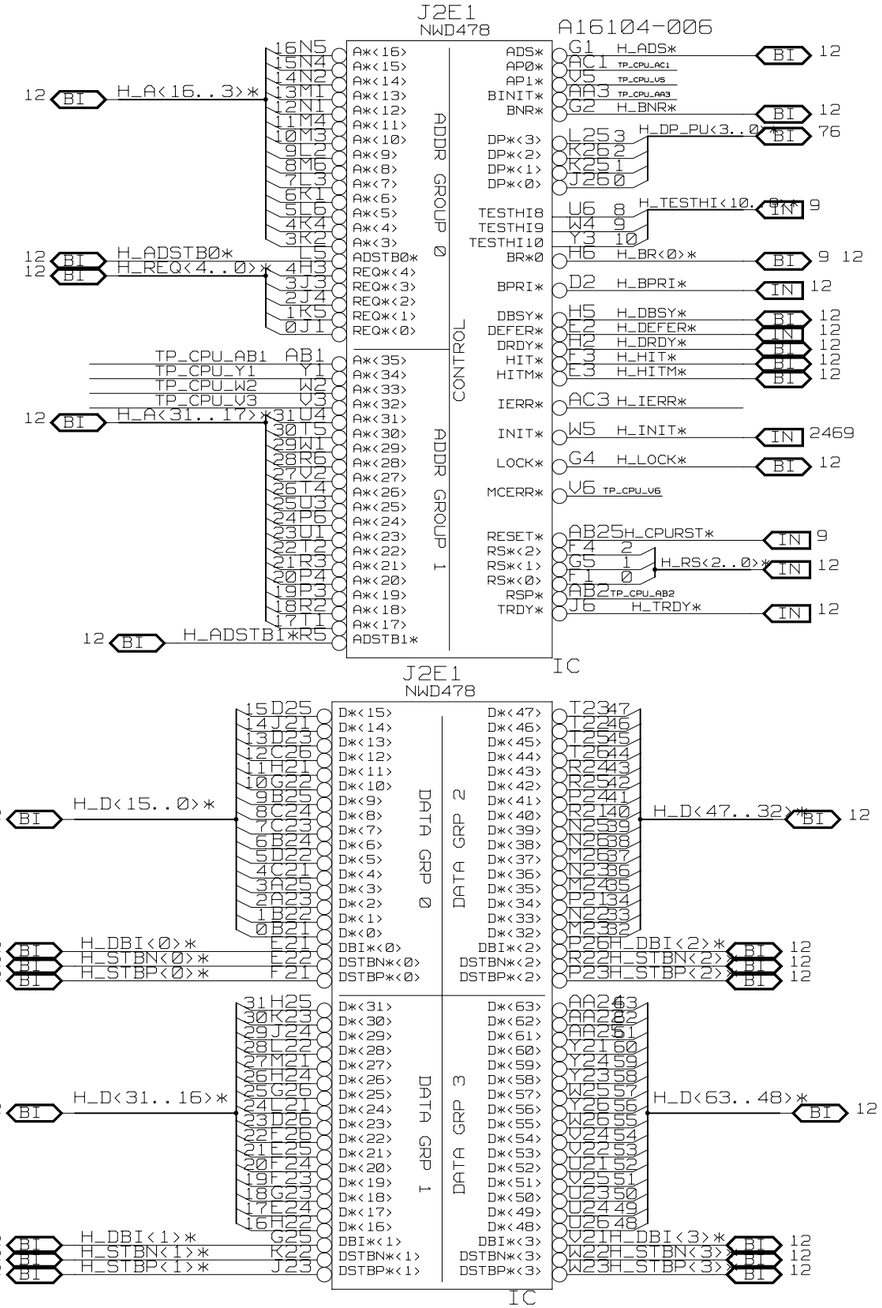
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

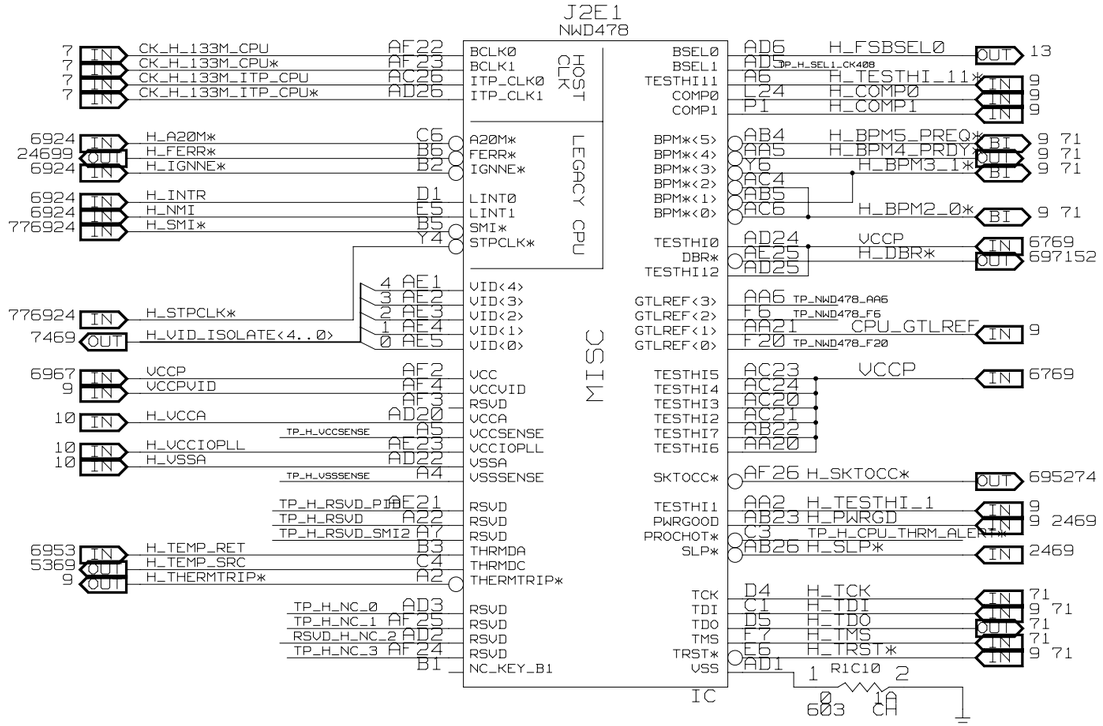
LAST REVISED: SEPT 13, 2002

SHEET: 6


U6B1
CK_408
VCC3_CLK
VCC3_CLKAB
VCC3_CLKA
H_SEL0_CK408
H_SEL133_100_JMPR
H_SEL_2_CK408
SMB_DATA_ISO
SMB_CLK_ISO
CK_MULT0
CLK_IREF
CK_CPU_PCI_STOP
PCI_STOP
PWRDWN
OSC_CK14M_XTALIN
OSC_CK14M_XTALOUT
VTT_PWRGD#
CK_H_133M_GMCH#
CK_H_133M_GMCH
CK_H_133M_ITP_PN1#
CK_H_133M_ITP_PN1
CK_H_133M_CPU#
CK_H_133M_CPU
CK_H_133M_ITP_CPU#
CK_H_133M_ITP#
CK_H_133M_ITP_CPU
CK_H_133M_ITP
CK_14M_SIO_ICH_R
CK_P_33M_S6_R
CK_P_33M_S5_R
CK_P_33M_S4_R
CK_P_33M_PORT80_R
CK_P_33M_FWH_R
CK_P_33M_SIO_R
CK_P_33M_ICH_R
CK_P_33M_S3_R
CK_P_33M_S2_R
CK_P_33M_S1_R
CK_66M_GLUE_R
CK_66M_PLD_R
CK_66M_GMCH_R
CK_HI_66M_ICH_R
CK_G_66M_AGP_R
CK_48M_DOTCLK_R
CK_48M_ICH_USB_R
CK_14M_AUD
CK_14M_ICH
CK_14M_SIO
CK_P_33M_S6
CK_P_33M_S5
CK_P_33M_S4
CK_P_33M_PORT80
CK_P_33M_FWH
CK_P_33M_SIO
CK_P_33M_ICH
CK_P_33M_S3
CK_P_33M_S2
CK_P_33M_S1
CK_66M_GLUE
CK_66M_PLD
CK_66M_GMCH
CK_66M_ICH
CK_G_66M_AGP
CK_48M_DOTCLK
CK_48M_ICH_USB
SMB_DATA_ISO
SMB_CLK_ISO
VCCP
NOTE:
BSEL[1:0] OF THE CPU
DO NOT CORRESPOND DIRECTLY
TO THE CK-408 SEL[1:0]
CAD NOTE:
TIE VSSA (U3F1 - 27)
DIRECTLY TO C1364 1
VREG FEATURE
SPARE SECTIONS
IC
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD
PAGE TITLE:
CK_408 (MAIN CLOCK GENERATOR)
REV:
02.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
SEPT 13, 2002
SHEET:
7

ROOM=DCL_CORE_CPU





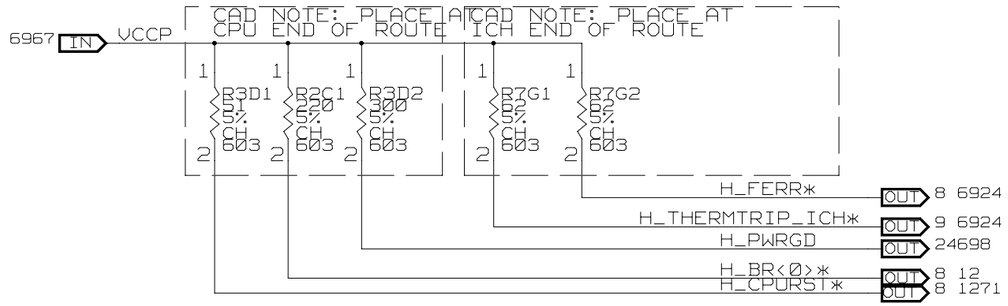
GND=AE7, AE24, AE22, AE10
GND=AD7, AD12, AD10, AD8, AD4, AD23, AD21, AE17, AE15, AE13, AE11, AE9, AE26
GND=AB20, AC12, AC10, AC8, AC3, AC1, AC24, AC22, AC19, AD18, AD16
GND=AB18, AB16, AB14, AB12, AB10, AB8, AB6, AB3, AB24, AB21
GND=C4, C1, C23, W6, W3, W21, AA26
VCCCB=AD11, AD9, AD7, AD19, AE18, AE16, AE14, AE12, AE10, AE8, AE6, AE20
VCCCB=AB15, AB13, AB11, AB9, AB7, AB19, AC18, AC16, AC14, AC12, AC10, AC8, AD17, AD15, AD13
VCCCB=B14, B12, B10, E8, E10, E7, E11, E5, E13, E15, E17, E19, E21, AB18, AA16, AA12, AA10, AA8, AB17
VCCCB=B13, B11, B9, B7, E9, B15, B17, B19, B21, AA14, AA18, AA20, AA22, AA24, AB16, AB14, AB12, AB10, AB8, AB19, AB17, AB15, AB13, AB11, AB9, AB7, AB5, AB23, AB25, AA6, AA4, AA2, AA24, AA22, AA20, AA18, AA16, AA14, AA12, AA10, AA8, AB26, B17, B15
GND=K24, Y2, Y5, Y22, Y25, AA1, AA4, AA7, AA9, AA11, AA13, AA15, AA17, AA19, AA23, AA26
GND=K6, N3, N24, N21, P5, P2, P25, R22, R25, R4, R1, R23, T5, T3, T24, T21, U5, U2, U25, U22, V26
GND=G21, H26, H4, H1, H23, J5, J2, J25, J22, K6, K3, K24, K21, L26, L4, L1, L23, M5, M2, M25, M22
GND=F11, F9, F26, F7, F4, F1, F23, F13, F18, F16, F14, F12, F10, F8, F5, F2, F25, F22, G6, G3, G24
GND=C3, C2, C25, C22, C19, D6, D3, D24, D21, D14, D12, D10, D8, D5, D23, D20, E17, E15, E13
GND=B3, B24, A6, A1, A25, B22, B5, B20, B18, B16, B8, B6, B4, B23, B2, C21, C18, C11, C9, C7
GND=AF18, AF16, AF14, AF12, AF10, AF8, AF6, AF1, AF20, A17, A15, A13, A11, A9, A26

CAD NOTE:

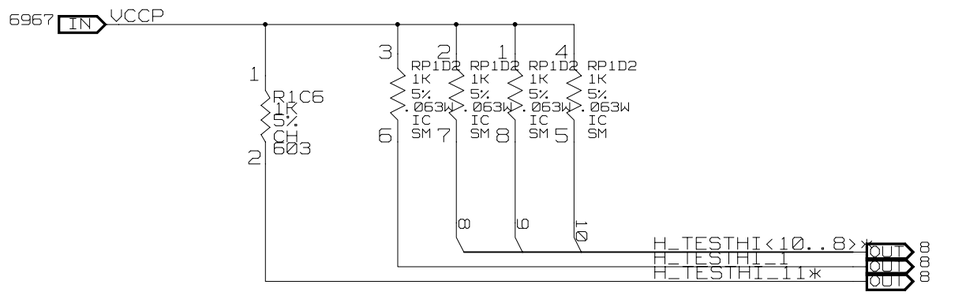
H_D AND H_A (AND ASSOCIATED SIGNALS)
MUST BE LENGTH MATCHED TO THE STROBE (STB OR STBP/STBN)
SIGNAL(S) WITHIN THE SAME COLOR GROUP TO +/-25 MILS,
AND STBP/STBN PAIRS MUST BE MATCHED TO +/-10 MILS OF EACH OTHER.

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: CPU CONNECTOR (SKT-N)		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 8

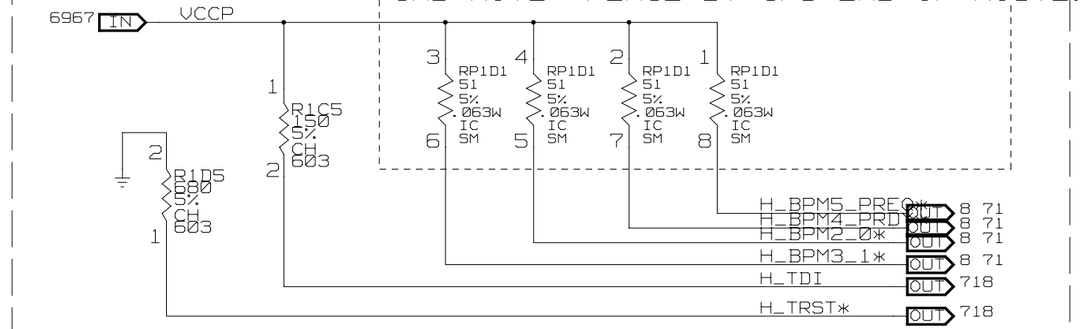
CPU SIGNAL TERMINATION

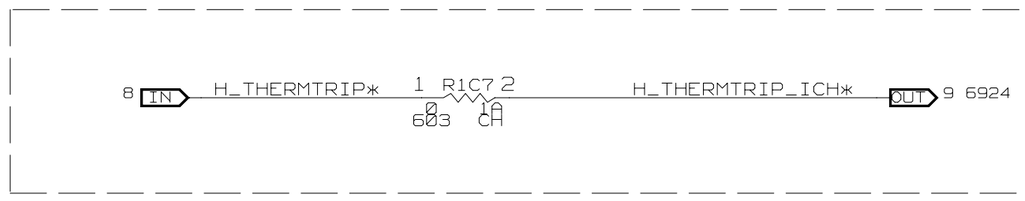


TESTHI PULLUPS

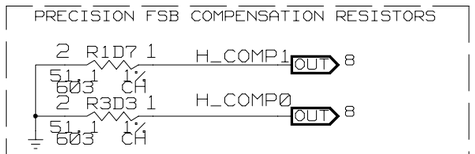


ITP/TAP TERMINATION

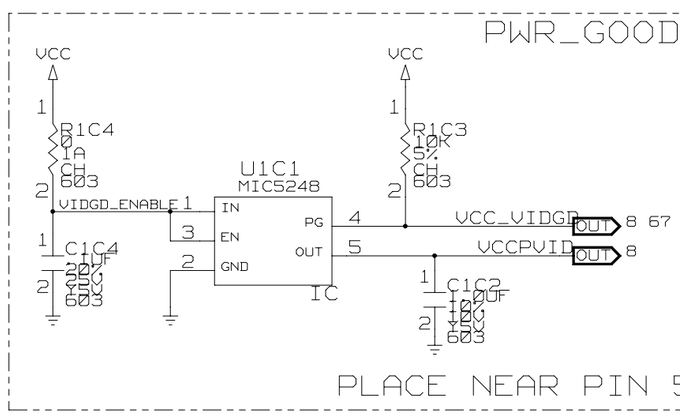




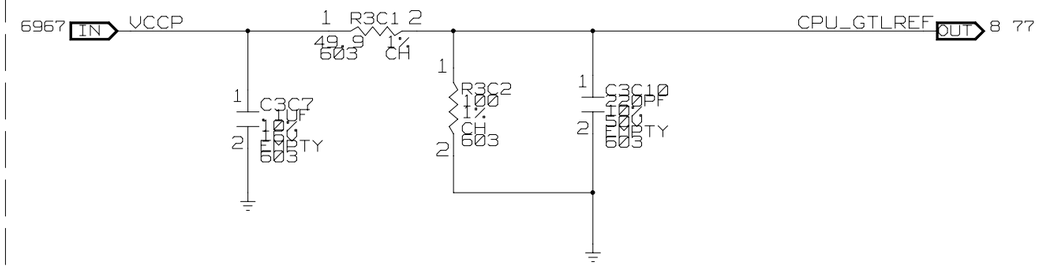
PRECISION FSB COMPENSATION RESISTORS



PWR_GOOD

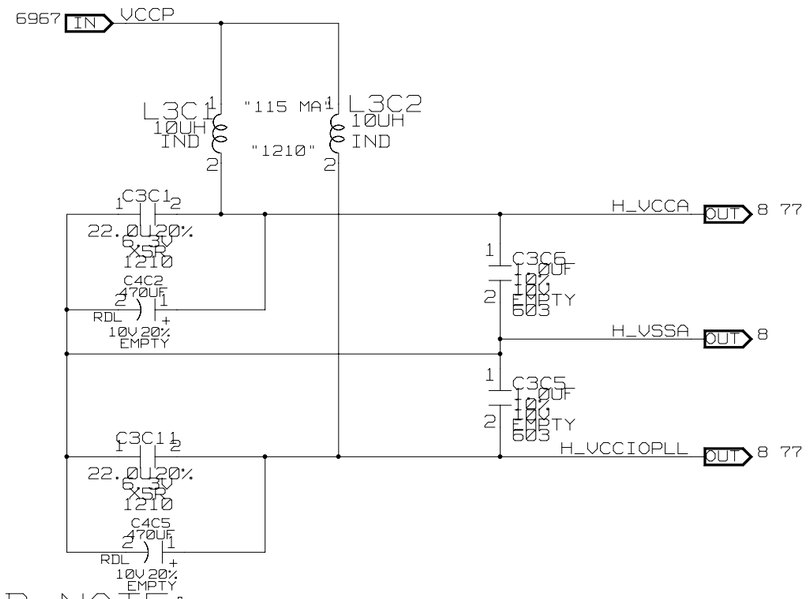


GTLREF GENERATION CIRCUITS



SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: CPU PULLUPS/PULLDNS/TERMINATION		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 9

PLL SUPPLY FILTER

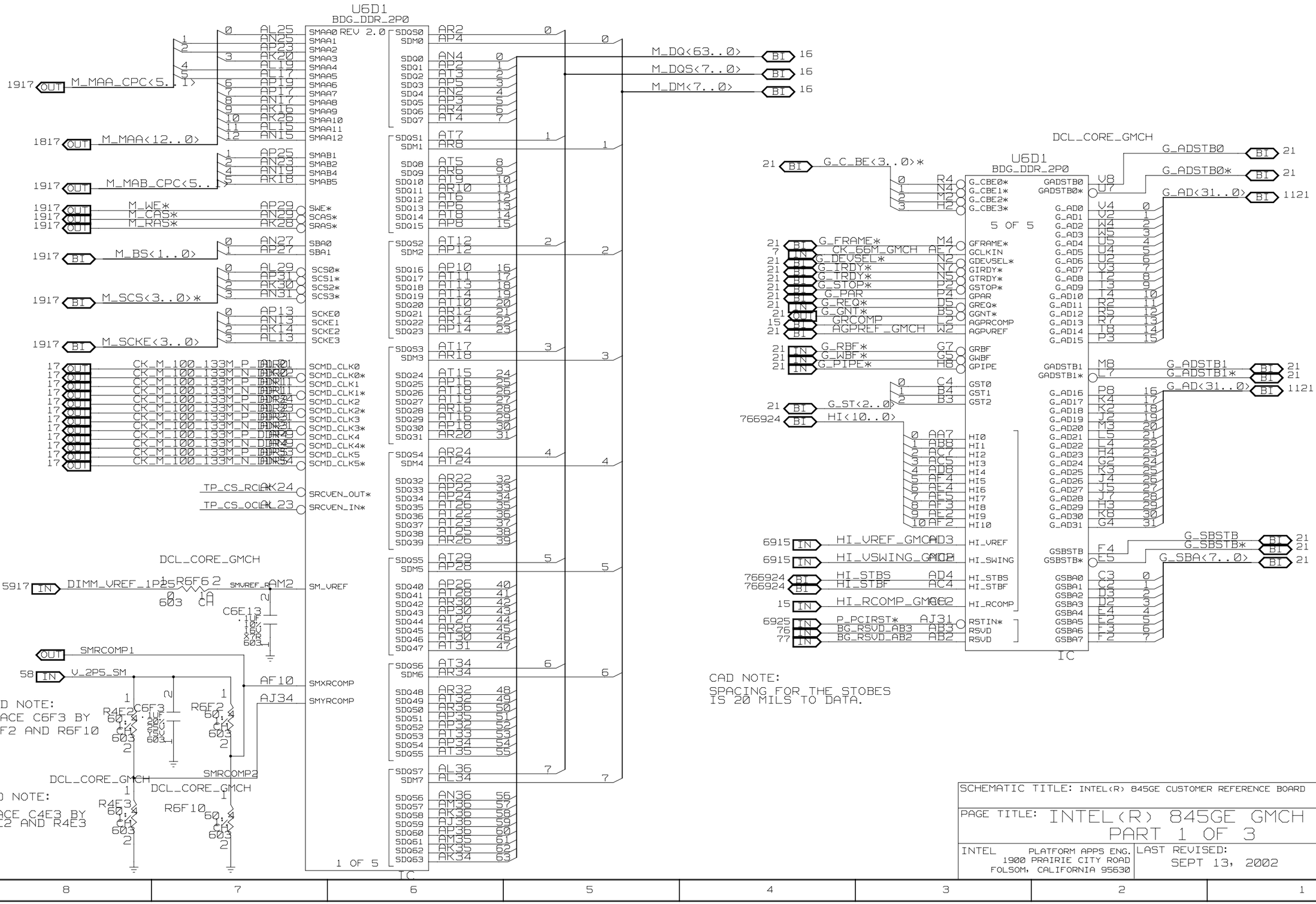


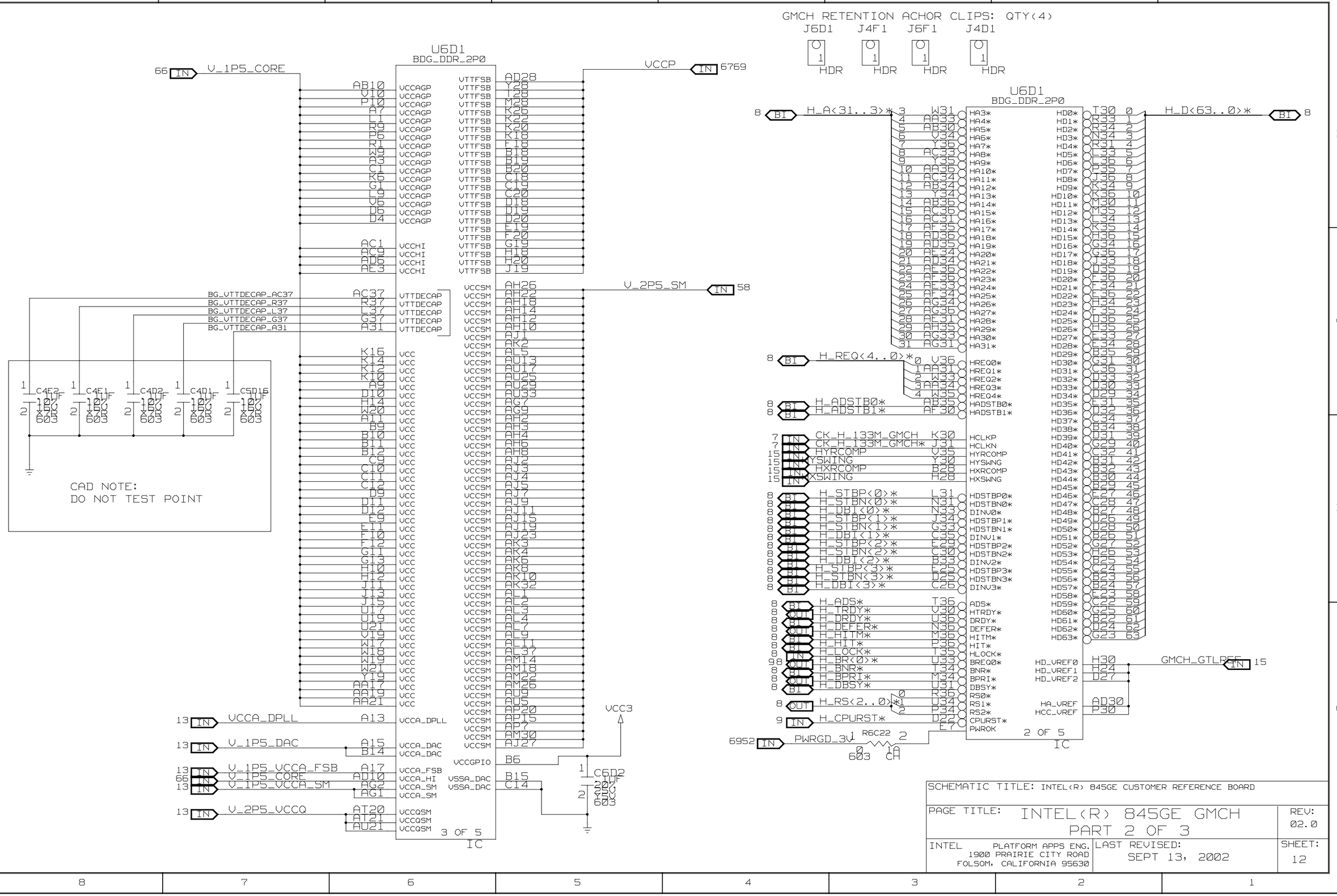
CAD NOTE:

PLACE THMT CAPS OUTSIDE RM BOUNDARY.
TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MIL

CAD NOTE: PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: FILTERED ANALOG SUPPLY		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 10


U6D1
BDG_DDR_2P0
SMAA0 REV 2.0
SMAA1
SMAA2
SMAA3
SMAA4
SMAA5
SMAA6
SMAA7
SMAA8
SMAA9
SMAA10
SMAA11
SMAA12
SMAB1
SMAB2
SMAB4
SMAB5
SWE*
SCAS*
SRAS*
SBA0
SBA1
SCS0*
SCS1*
SCS2*
SCS3*
SCKE0
SCKE1
SCKE2
SCKE3
SCMD_CLK0
SCMD_CLK0*
SCMD_CLK1
SCMD_CLK1*
SCMD_CLK2
SCMD_CLK2*
SCMD_CLK3
SCMD_CLK3*
SCMD_CLK4
SCMD_CLK4*
SCMD_CLK5
SCMD_CLK5*
SRCVEN_OUT*
SRCVEN_IN*
SMXRCOMP
SMYRCOMP
SDQS0
SDM0
SDQ0
SDQ1
SDQ2
SDQ3
SDQ4
SDQ5
SDQ6
SDQ7
SDQS1
SDM1
SDQ8
SDQ9
SDQ10
SDQ11
SDQ12
SDQ13
SDQ14
SDQ15
SDQS2
SDM2
SDQ16
SDQ17
SDQ18
SDQ19
SDQ20
SDQ21
SDQ22
SDQ23
SDQS3
SDM3
SDQ24
SDQ25
SDQ26
SDQ27
SDQ28
SDQ29
SDQ30
SDQ31
SDQS4
SDM4
SDQ32
SDQ33
SDQ34
SDQ35
SDQ36
SDQ37
SDQ38
SDQ39
SDQS5
SDM5
SDQ40
SDQ41
SDQ42
SDQ43
SDQ44
SDQ45
SDQ46
SDQ47
SDQS6
SDM6
SDQ48
SDQ49
SDQ50
SDQ51
SDQ52
SDQ53
SDQ54
SDQ55
SDQS7
SDM7
SDQ56
SDQ57
SDQ58
SDQ59
SDQ60
SDQ61
SDQ62
SDQ63
1 OF 5
IC
M_DQ<63..0>
M_DQS<7..0>
M_DM<7..0>
M_MAA_CPC<5..1>
M_MAA<12..0>
M_MAB_CPC<5..
M_WE*
M_CAS*
M_RAS*
M_BS<1..0>
M_SCS<3..0>*
M_SCKE<3..0>
CK_M_100_133M_P_DDR0
CK_M_100_133M_N_DDR0
CK_M_100_133M_P_DDR1
CK_M_100_133M_N_DDR1
CK_M_100_133M_P_DDR2
CK_M_100_133M_N_DDR2
CK_M_100_133M_P_DDR3
CK_M_100_133M_N_DDR3
CK_M_100_133M_P_DDR4
CK_M_100_133M_N_DDR4
CK_M_100_133M_P_DDR5
CK_M_100_133M_N_DDR5
TP_CS_RCLK
TP_CS_OCLK
DCL_CORE_GMCH
DIMM_VREF_1P25
R6F62
SMVREF_R
SM_VREF
C6E13
.1UF
10%
16V
X7R
603
SMRCOMP1
V_2P5_SM
CAD NOTE:
PLACE C6F3 BY
R6F2 AND R6F10
R4E2
C6F3
.1UF
R6F2
SMRCOMP2
CAD NOTE:
PLACE C4E3 BY
R4E2 AND R4E3
R4E3
R6F10
DCL_CORE_GMCH
U6D1
BDG_DDR_2P0
5 OF 5
G_C_BE<3..0>*
G_FRAME*
CK_66M_GMCH
G_DEVSEL*
G_IRDY*
G_TRDY*
G_STOP*
G_PAR
G_REQ*
G_GNT*
GRCOMP
AGPREF_GMCH
G_RBF*
G_WBF*
G_PIPE*
G_ST<2..0>
HI<10..0>
HI_VREF_GMCH
HI_VSWING_GMCH
HI_STBS
HI_STBF
HI_RCOMP_GMCH
P_PCIRST*
BG_RSVD_AB3
BG_RSVD_AB2
G_CBE0*
G_CBE1*
G_CBE2*
G_CBE3*
GFRAME*
GCLKIN
GDEVSEL*
GIRDY*
GTRDY*
GSTOP*
GPAR
GREQ*
GGNT*
AGPRCOMP
AGPVREF
GRBF
GWBF
GPIPE
GST0
GST1
GST2
HI0
HI1
HI2
HI3
HI4
HI5
HI6
HI7
HI8
HI9
HI10
HI_VREF
HI_SWING
HI_STBS
HI_STBF
HI_RCOMP
RSTIN*
RSVD
RSVD
IC
G_ADSTB0
G_ADSTB0*
G_AD<31..0>
G_AD0
G_AD1
G_AD2
G_AD3
G_AD4
G_AD5
G_AD6
G_AD7
G_AD8
G_AD9
G_AD10
G_AD11
G_AD12
G_AD13
G_AD14
G_AD15
G_ADSTB1
G_ADSTB1*
G_AD16
G_AD17
G_AD18
G_AD19
G_AD20
G_AD21
G_AD22
G_AD23
G_AD24
G_AD25
G_AD26
G_AD27
G_AD28
G_AD29
G_AD30
G_AD31
GADSTB0
GADSTB0*
GADSTB1
GADSTB1*
G_SBSTB
G_SBSTB*
G_SBA<7..0>
GSBSTB
GSBSTB*
GSBA0
GSBA1
GSBA2
GSBA3
GSBA4
GSBA5
GSBA6
GSBA7
CAD NOTE:
SPACING FOR THE STOBES
IS 20 MILS TO DATA.
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD
PAGE TITLE: INTEL(R) 845GE GMCH
PART 1 OF 3
REV: 02.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
SEPT 13, 2002
SHEET: 11


GMCH RETENTION ACHOR CLIPS: QTY(4)
J6D1 J4F1 J6F1 J4D1
HDR
U6D1
BDG_DDR_2P0
66 IN V_1P5_CORE
VCCP IN 6769
V_2P5_SM IN 58
BG_VTTDECAP_AC37
BG_VTTDECAP_R37
BG_VTTDECAP_L37
BG_VTTDECAP_G37
BG_VTTDECAP_A31
C4E3 C4E1 C4D3 C4D1 C5D16
10UF X5R 603
CAD NOTE:
DO NOT TEST POINT
13 IN VCCA_DPLL
13 IN V_1P5_DAC
13 IN V_1P5_VCCA_FSB
66 IN V_1P5_CORE
13 IN V_1P5_VCCA_SM
13 IN V_2P5_VCCQ
VCC3
C6D2 10UF X5R 603
3 OF 5
IC
8 BI H_A<31..3>*
H_D<63..0>* BI 8
8 BI H_REQ<4..0>*
8 BI H_ADSTB0*
8 BI H_ADSTB1*
7 IN CK_H_133M_GMCH
7 IN CK_H_133M_GMCH*
15 IN HYRCOMP
15 IN HYSWING
15 IN HXRCOMP
15 IN HXSWING
8 BI H_STBP<0>*
8 BI H_STBN<0>*
8 BI H_DBI<0>*
8 BI H_STBP<1>*
8 BI H_STBN<1>*
8 BI H_DBI<1>*
8 BI H_STBP<2>*
8 BI H_STBN<2>*
8 BI H_DBI<2>*
8 BI H_STBP<3>*
8 BI H_STBN<3>*
8 BI H_DBI<3>*
8 BI H_ADS*
8 BI H_TRDY*
8 BI H_DRDY*
8 BI H_DEFER*
8 BI H_HITM*
8 BI H_HIT*
8 BI H_LOCK*
9 8 IN H_BR<0>*
8 BI H_BNR*
8 BI H_BPRI*
8 BI H_DBSY*
8 OUT H_RS<2..0>*
9 IN H_CPURST*
6952 IN PWRGD_3V
R6C22 0 603 1A CH
2 OF 5
IC
HD_VREF0 H30
HD_VREF1 H24
HD_VREF2 D27
HA_VREF AD30
HCC_VREF P30
GMCH_GTLREF IN 15
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD
PAGE TITLE: INTEL(R) 845GE GMCH PART 2 OF 3
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ANALOG FILTERS

L6D1 10UH
R6D2 1.0 5% CA 603
C5C6 470UF 20% EMPTY RDL
C6C11 470UF 20% POLYM RDL
C5D19 10UF 10% 10V TANTY 603
DFP
66 IN V_1P5_CORE
VCCA_DPLL OUT 12

R5D5 0 1A CA 603
C5D20 10UF 10% 10V X5R 603
C5D10 10UF 10% 10V X5R 603
66 IN V_1P5_CORE
V_1P5_DAC OUT 12

L5D1 .82UH IND
C5C7 22UF 20% 25V EFFC RDL
C5D9 10UF 10% 10V X5R 603
66 IN V_1P5_CORE
V_1P5_VCCA_FSB OUT 12

L6E1 1UH IND
C6E11 100UF 20% 25V EFFC RDL
C6E10 1UF 10% 10V X5R 603
66 IN V_1P5_CORE
V_1P5_VCCA_SM OUT 12

L5F1 .68UH IND
C5F7 47UF 10% 10V X5R 1206
R5F1 1.0 5% CH 603
C5F1 1UF 10% 10V X5R 603
58 IN V_2P5_SM
V_2P5_VCCQ OUT 12

R6C4 1.5K 5% CH 603
R6C12 8.2K 5% CA 603
R6C16 8.2K 5% CH 603
2R6C13 1 1A 0 EMPTY 603
H_FSBSEL0 IN 8
HDR TH J6C2

DEFAULT 1-2

J6C2	SPEED
1-2	CPU SELECT
2-3	100MHZ
EMPTY	133MHZ

VCC3_CLK IN 7
H_SEL133_100_JMPR OUT 7

U6D1
BDG_DDR_2P0

TP_BG_RSVD_Y3 Y3 PSBSEL
TP_BG_RSVD_Y2 Y2 MEMSEL
TP_BG_RSVD_AA2 AA2 RSVD
TP_BG_RSVD_AA4 AA4 RSVD
TP_BG_RSVD_AA3 AA3 RSVD
TP_BG_RSVD_AA5 AA5 RSVD
TP_BG_RSVD_W7 W7 RSVD
TP_BG_RSVD_Y4 Y4 RSVD
TP_BG_RSVD_Y8 Y8 RSVD
TP_BG_RSVD_A37 A37 RSVD
4 OF 5
IC

DDCA_DATA C7
DDCA_CLK D7
GLUE4_DDCSDA_3V B1 5269
GLUE4_DDCSCL_3V B1 5269

RED C15
RED* D15
GREEN E15
GREEN* F15
BLUE G15
BLUE* H15
VGA_RED OUT 6922
VGA_RED* OUT 6922
VGA_GREEN OUT 6922
VGA_GREEN OUT 6922
VGA_BLUE OUT 6922
VGA_BLUE* OUT 6922

HSYNC B7 BG_HSYNC_B7
VSYNC C6 BG_VSYNC_C6
DREFCLK D14
REFSET B16
R5D6 130 1% CH 603
REFSET

CR5D3 GP SOT23S DIO
CR5D1 GP SOT23S DIO
CR5D2 GP SOT23S DIO
V_1P5_CORE IN 66
C5D3 1UF 10% 10V X5R 603

1 R6C192 47 5% CA 603
1 R6C202 47 5% CA 603
U6C2 74AHCT1G08
U6C1 74AHCT1G08
EMPTY
VCC=5 GND=3
R6C18 0 1A CA 603
R6C17 0 1A CA 603
HSYNC_5V OUT 6922
VSYNC_5V OUT 6922
CR6C1 GP SOT23S EMPTY
CR6C2 GP SOT23S EMPTY
VCC3
CK_48M_DOTCLK IN 7

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: INTEL(R) 845GE GMCH PART 3 OF 3		REV: 02.0
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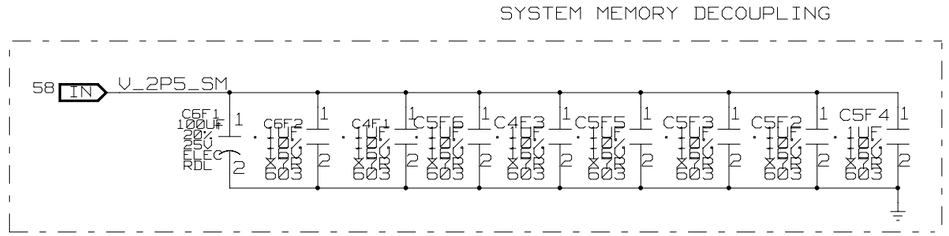
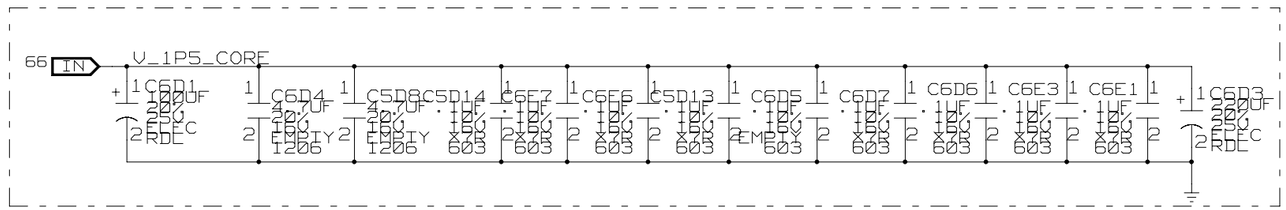
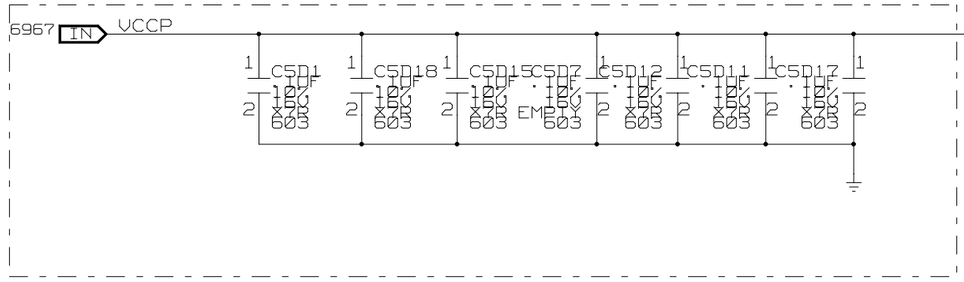
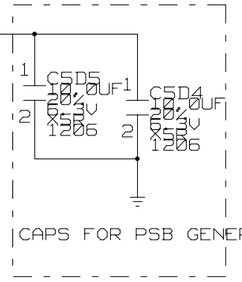
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD			
PAGE TITLE: BLANK			REV: 02.0
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 14

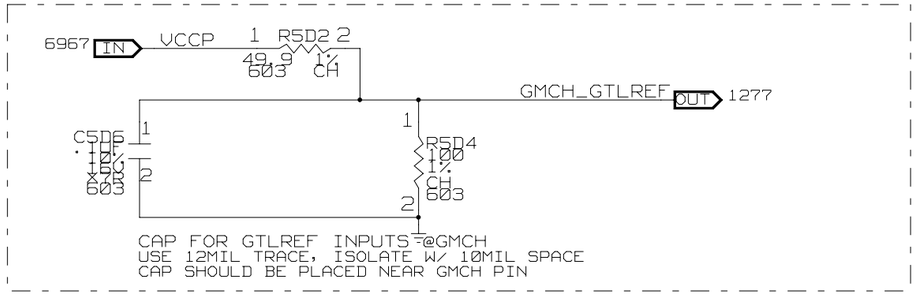
SYSTEM MEMORY DECOUPLING

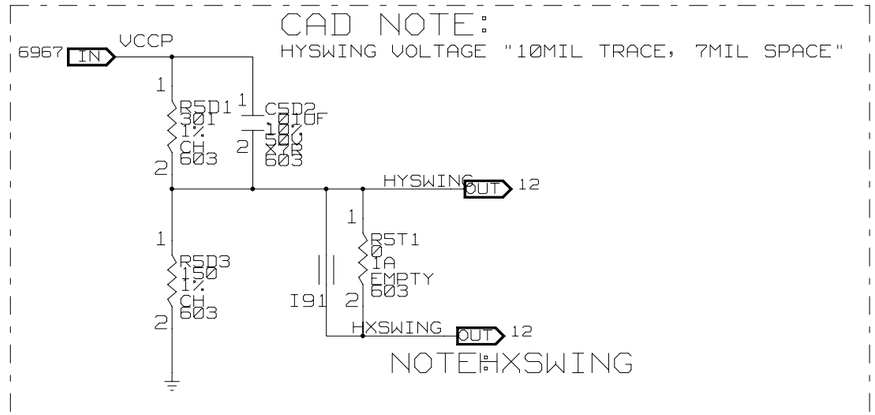


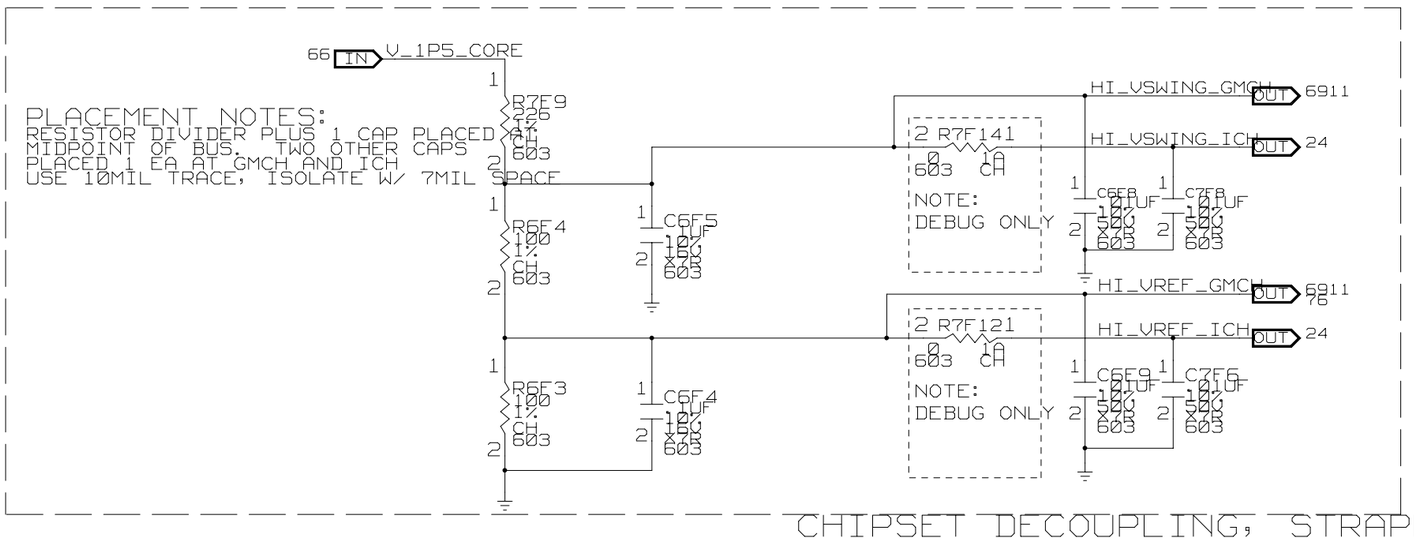


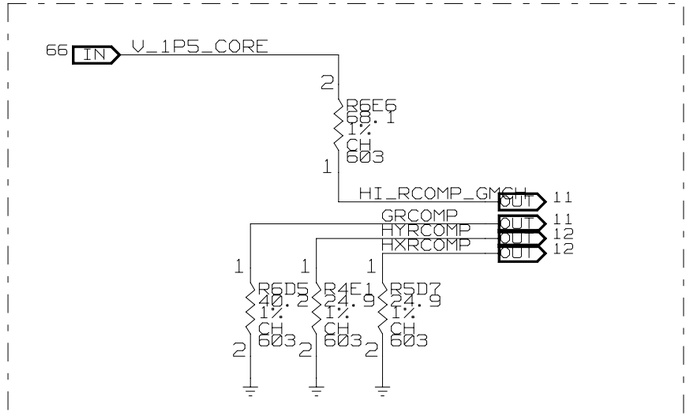












CHIPSET DECOUPLING, STRAPPING

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: DECOUPLING & REFERENCE VOLTAGES		REV: 02.0
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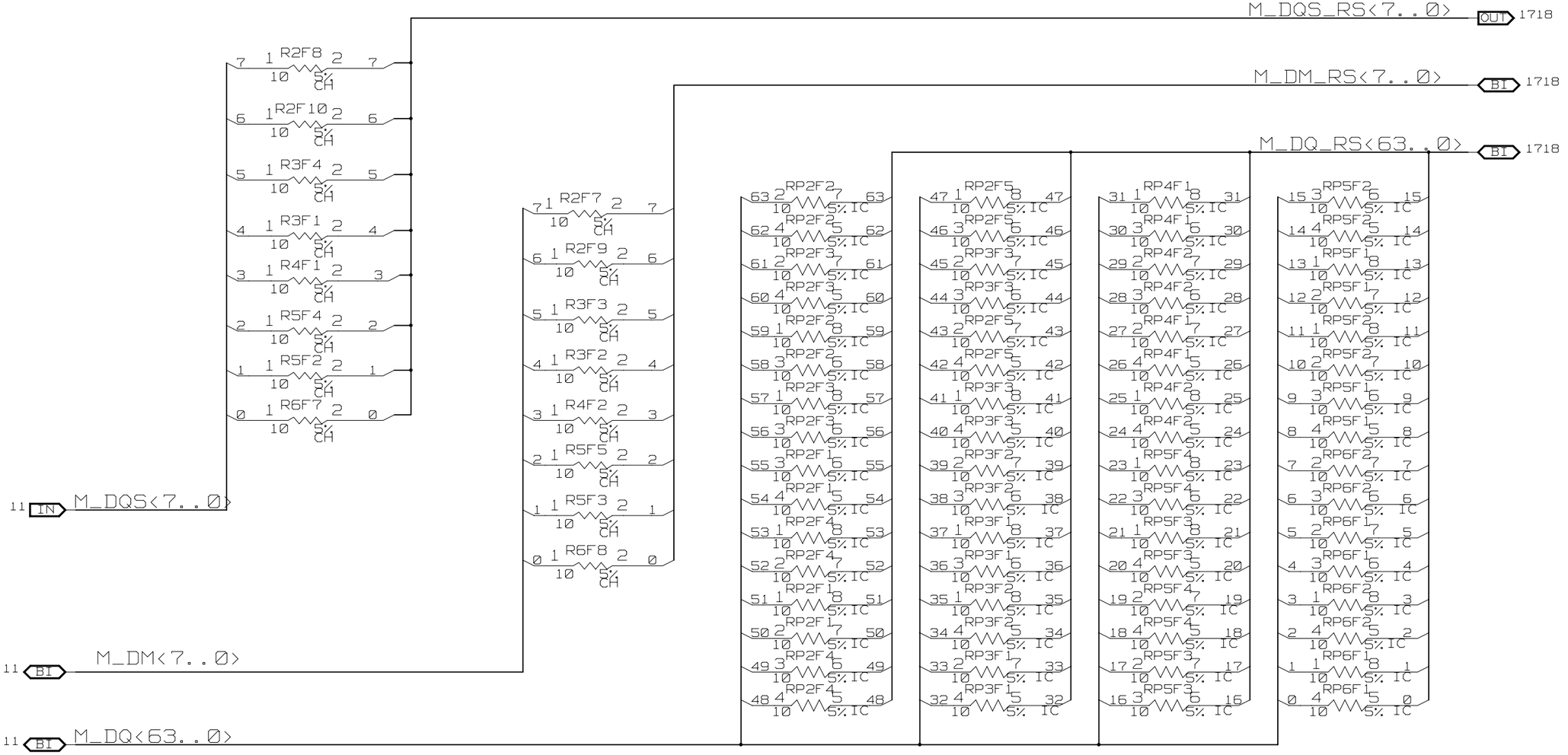
DDR SERIES RESISTORS



SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD	
PAGE TITLE: DDR SERIES RESISTORS	REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002
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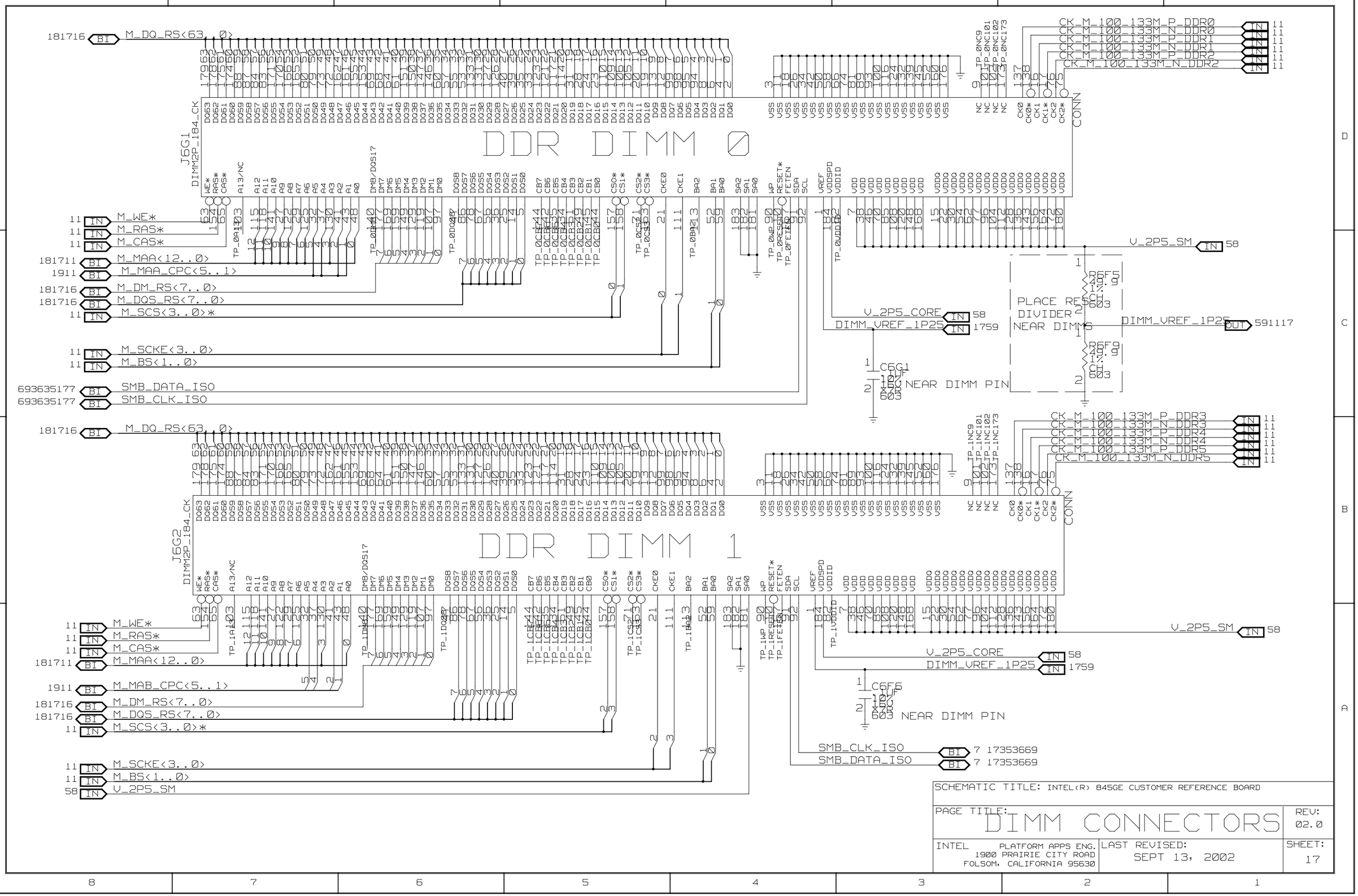

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: DIMM CONNECTORS

REV: 02.0

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DDR TERMINATION RESISTORS

1716 IN M_DQS_RS<7..0>

1716 BI M_DM_RS<7..0>

1716 BI M_DQ_RS<63..0>

1711 BI M_MAA<12..0>

59 IN V_1P25_MEMVTT

RP2G5 RP2G3 R2G2 R3G1 RP4G5 RP5G7 RP5G2 RP6G2

RP6G2 RP5G2 RP5G7 R4G3 RP3G2 R2G1 RP2G5 RP2G5

RP1G1 RP1G1 RP2G5 RP1G1 RP2G5 RP2G4 RP2G3 RP2G2 RP2G4 RP2G2 RP2G4 RP2G2

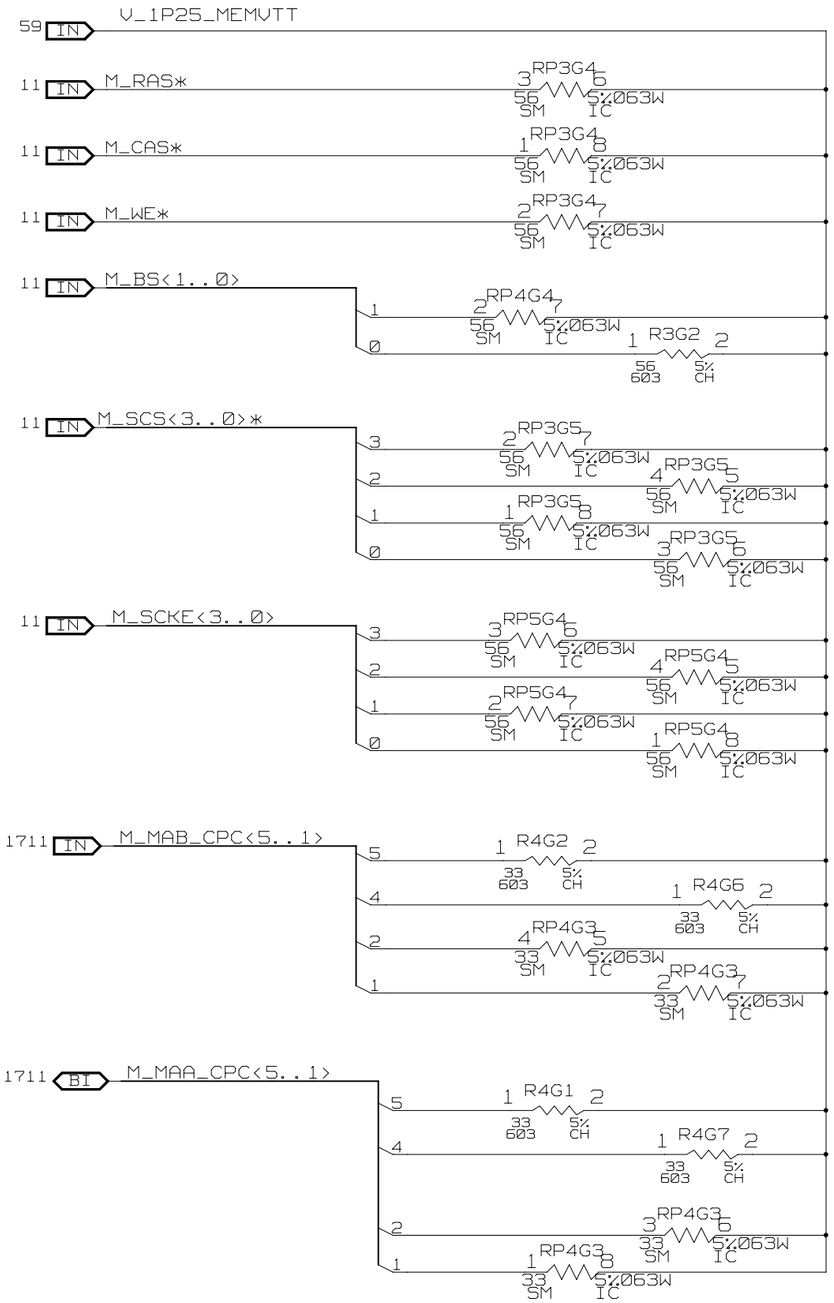
RP2G1 RP2G1 RP3G3 RP3G3 RP2G1 RP2G1 R3G3 RP3G3 RP3G2 RP3G1 RP3G1 RP3G3 RP3G2 RP3G1 RP3G1

RP4G2 RP4G2 RP4G5 RP4G5 RP4G2 RP4G2 RP4G5 RP4G1 RP5G7 RP5G5 RP4G1 RP5G7 RP5G5 RP5G5

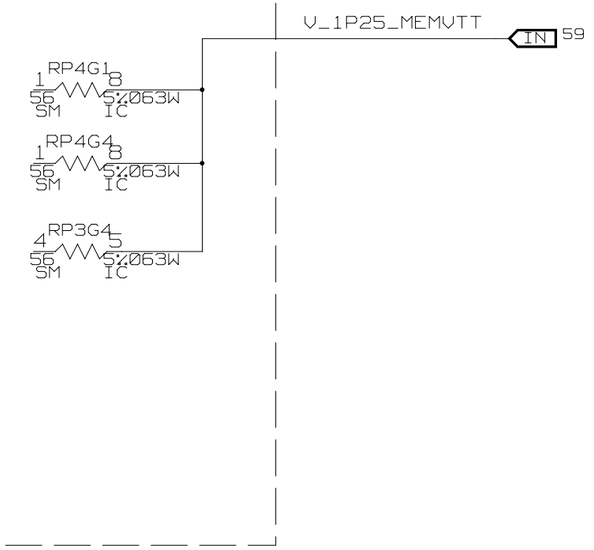
RP5G3 RP5G3 RP5G2 RP5G2 RP5G3 RP5G3 RP5G1 RP5G1 RP6G2 RP6G1 RP6G1 RP5G1 RP6G1 RP6G1

R5G1 RP5G6 RP4G4 RP5G6 RP5G6 R4G5 R4G4 RP4G4

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: DDR TERMINATION RESISTORS		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 18



SPARES



NOTE:

CS SIGNALS MUST HAVE IT'S OWN RES/RPACK
CKE SIGNALS MUST HAVE IT'S OWN RES/RPACK
CPC SIGNALS MUST HAVE IT'S OWN RES/RPACK

SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: DDR TERMINATION RESISTORS

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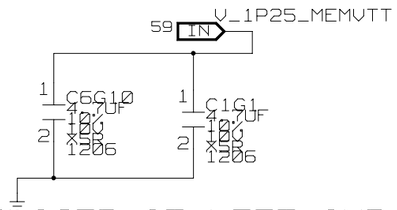
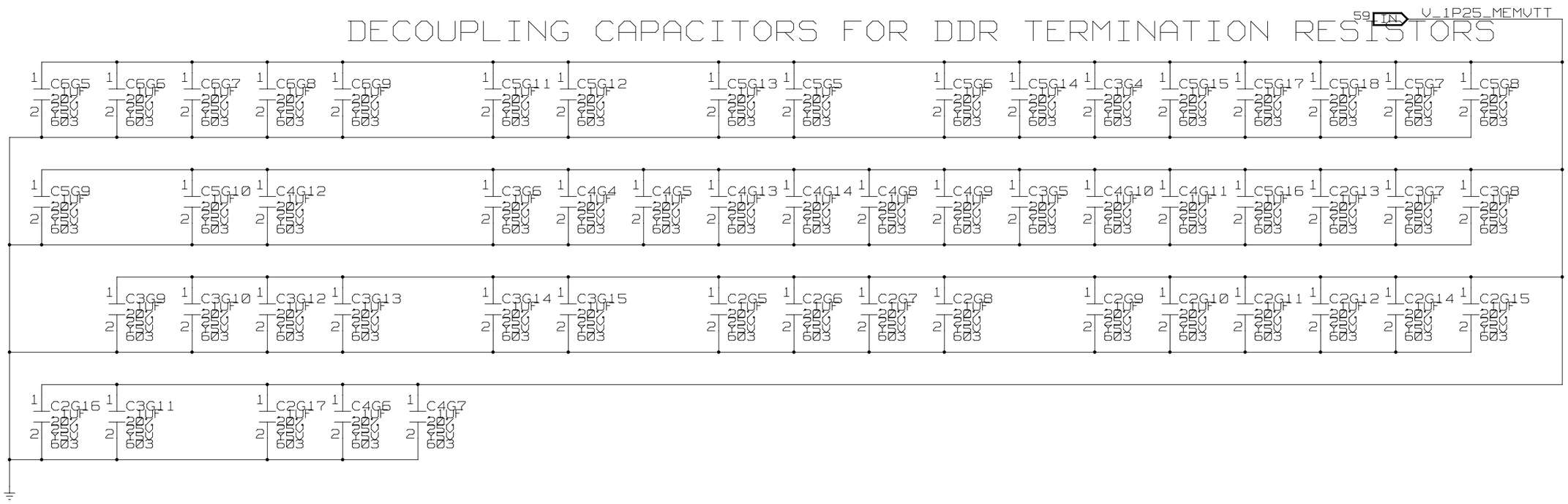


PLACED AT LEFT AND RIGHT ENDS
OF VTT ISLAND

DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS



SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS		REV: 02.0
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OPTION TO STUFF AT ALTERED ASSEMBLY LEVEL

RM6C1 AGP RETENTION MECH

66 IN V_1P5_CORE EMPTY

RP7C2 6.80K 5% .063W EMPTY SM

11 IN G_ST<2..0>

11 BI G_AD<31..0>

J6C1 1.5V CONAGP

CAD PLACEMENT NOTE:
ENSURE STUB LENGTH TO
RESN. IS < 100MIL

::REMOVE ON FAB_B::
PLACE ON CHIPSET SIDE
OF AGP CONN

66 IN V_1P5_CORE

R6C21 R6D3 R6E7 8.8K 5% EMPTY 603

11 BI G_ADSTB0
11 BI G_ADSTB1
11 BI G_ADSTB0*
11 BI G_ADSTB1*
11 BI G_SBSTB
11 OUT G_SBSTB*
11 BI G_C_BE<3..0>*

R6D1 R6D4 R6E8 8.8K 5% EMPTY 603

23693431 BI P_INTA*
23693431 BI P_INTB*
7 IN CK_G_66M_AGP
3332316952 BI P_RST_SLOTS*
2369333231 BI P_PME*

NC=1, 2, 3
GND=A5, B5, A13, B13, A19, B19, A23, B23, A31, B31, A37, B37, A49, B49, A55, B55, A61, B61

66 IN V_1P5_CORE

R6E102 1K 1% CH 603

AGPREF_GMCH OUT 11

R6E9 1K 1% CH 603

C6E4 10UF 10V X5R 603 PLACE NEAR GMCH

R6F1 0 1A CH 603

CAD NOTE:
PLACE NEAR
GMCH PINS

AGPREF_CON

C7F3 1UF 10V X5R 603 PLACE NEAR AGP

CAD PLACEMENT NOTE:
PLACE RESISTORS NEAR AGP CONN

V_1P5_CORE CHECK PULL-UP VALUES PER AGP2.0

R7E3 R7E2 R7E1 8.8K 5% CH 603

RP7D1 6.80K 5% .063W EMPTY SM

RP7C2 6.80K 5% .063W EMPTY SM

RP7C3 6.80K 5% .063W EMPTY SM

R7E4 8.8K 5% EMPTY 603

PLACE ON CHIPSET SIDE OF AGP CONN

G_PERR_R*
G_SERR_R*

G_DEVSEL* G_IRDY* G_TRDY* G_FRAME* G_STOP* G_PAR G_WBF* G_REQ* G_GNT* G_RBF* G_PIPE*

R7E5 330 5% EMPTY 603

NOTE:
DVO SUPPORT

VCC3 C7D6 100UF 20% 25Q 2 FLEC RDL

VCC3 C7C10 22UF 20% 25Q 2 FLEC RDL

VCC C6C8 22UF 20% 25Q 2 FLEC RDL

+12V C6C9 1UF 10% X5R 603

VCC C6C7 1UF 10% X5R 603

VCC3 C6C12 .2UF 10% X5R 603 C7D5 .2UF 10% X5R 603 C7D1 .2UF 10% X5R 603

C7D2 1UF 10% X5R 603

V_3P3_PCIVAUX IN 616972

66 IN V_1P5_CORE

C6E2 100UF 20% 6.3V 2 TPSC RDL

C7D7 C7E4 C6E5 C6E12 C7E2 C7D9 .2UF 10% X5R 603

CAD NOTE:
PLACE NEAR AGPCONN

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: AGP		REV: 02.0
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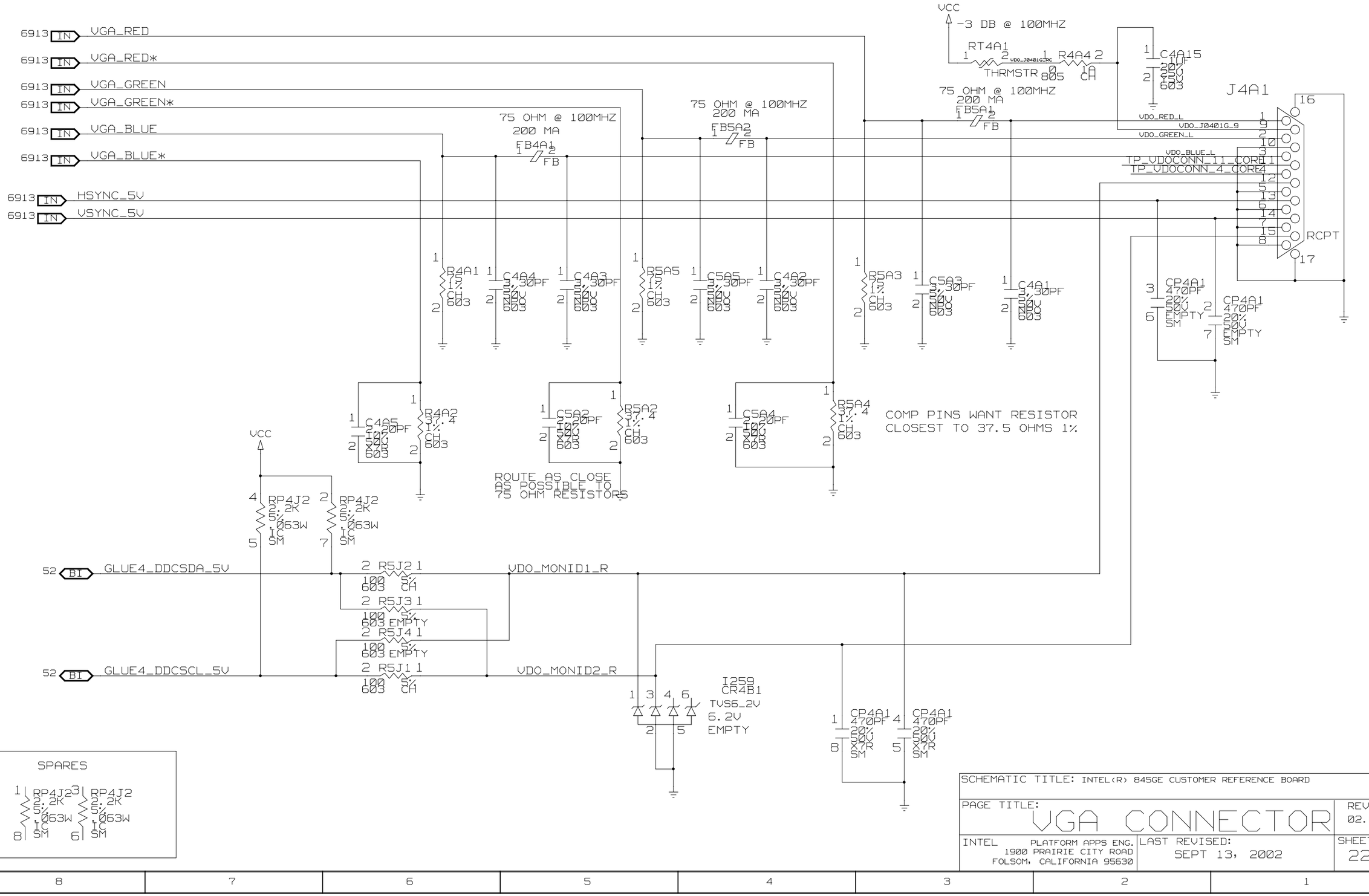

SCHEMATIC TITLE: INTEL‹R› 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: VGA CONNECTOR

REV: 02.0

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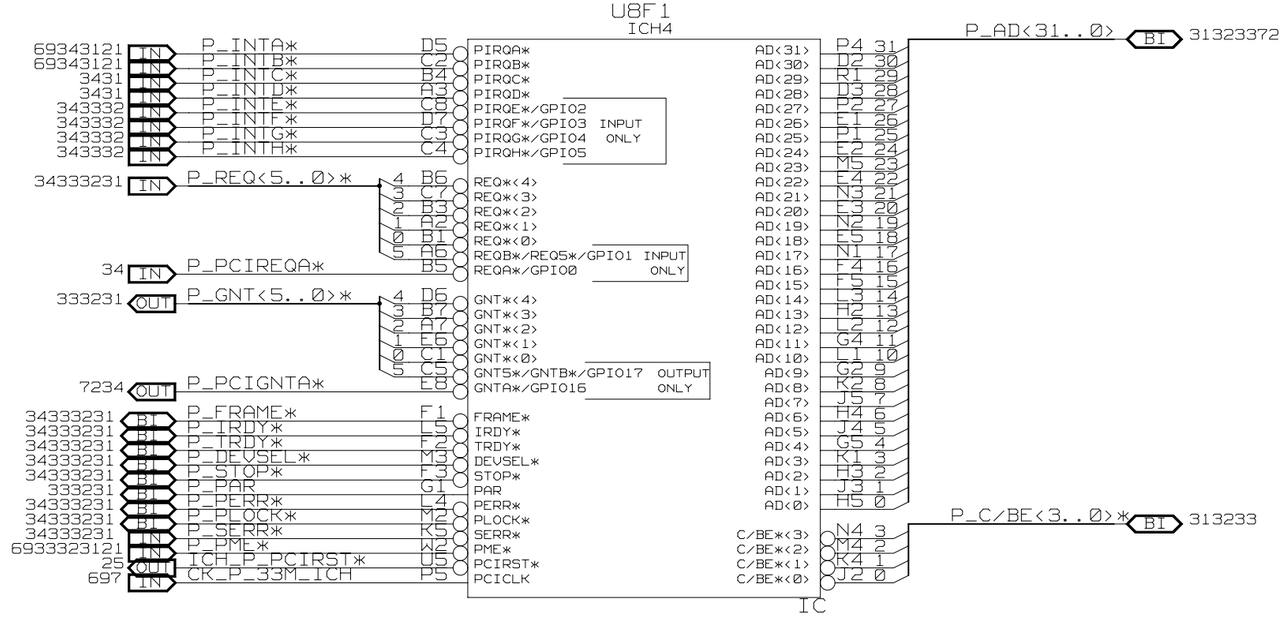

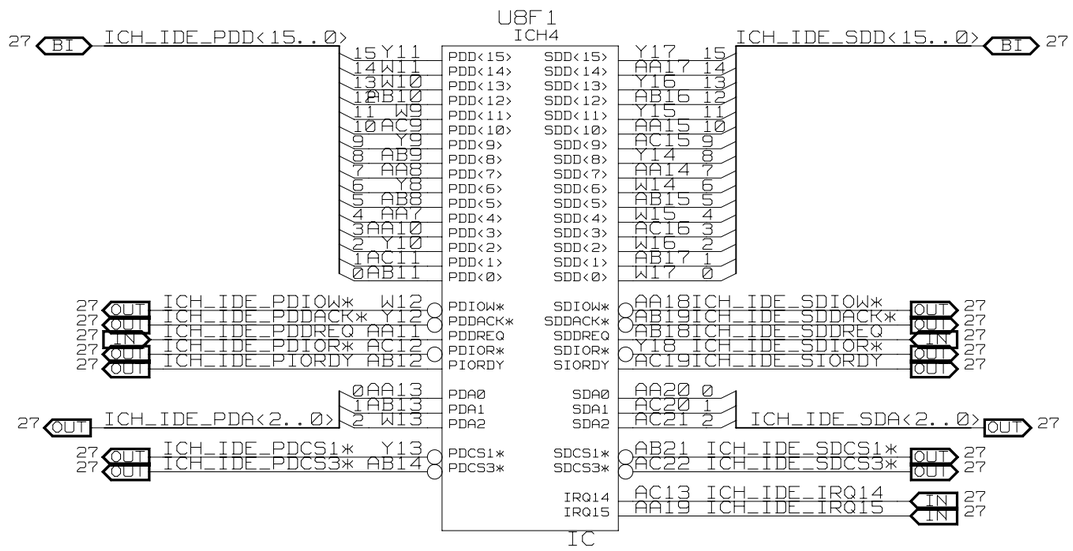

ICH4

SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: PCI/IDE/CPU/SYS_MGMT

REV: 02.0

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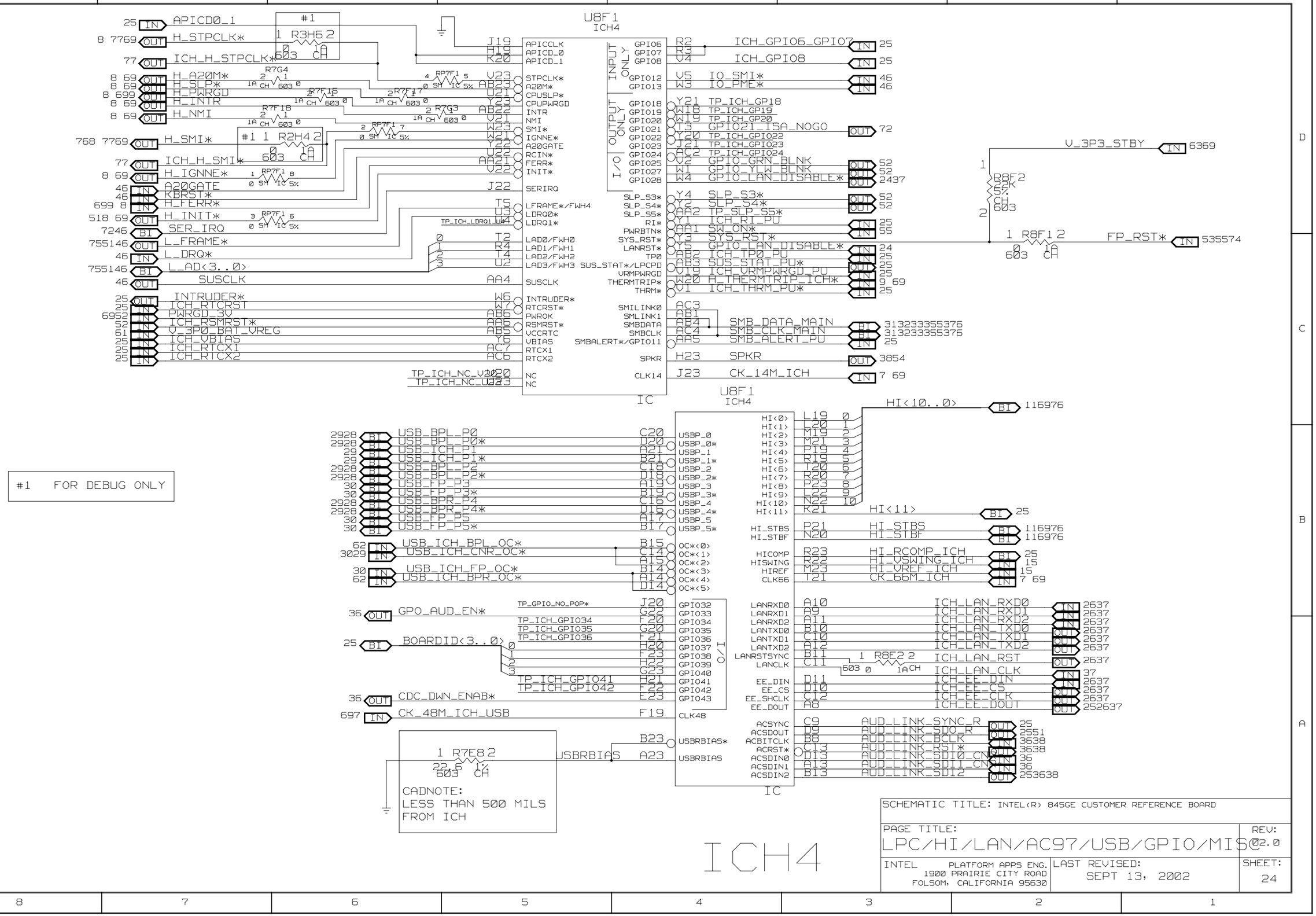
U8F1
ICH4
IC
#1
R3H62
R7G4
R2H42
R7F18
R7G3
R7F15
R7F16
R7F17
RP7F1
R7E82
22.6 1%
603 CH
#1 FOR DEBUG ONLY
CADNOTE:
LESS THAN 500 MILS
FROM ICH
APICD0_1
H_STPCLK*
ICH_H_STPCLK*
H_A20M*
H_SLP*
H_PWRGD
H_INTR
H_NMI
H_SMI*
ICH_H_SMI*
H_IGNNE*
A20GATE
KBRST*
H_FERR*
H_INIT*
SER_IRQ
L_FRAME*
L_DRQ*
L_AD<3..0>
SUSCLK
INTRUDER*
ICH_RTCRST
PWRGD_3V
ICH_RSMRST*
V_3P0_BAT_VREG
ICH_VBIAS
ICH_RTCX1
ICH_RTCX2
TP_ICH_NC_V20
TP_ICH_NC_U22
TP_ICH_LDRQ1_U4
STPCLK*
A20M*
CPUSLP*
CPUPWRGD
INTR
NMI
SMI*
IGNNE*
A20GATE
RCIN*
FERR*
INIT*
SERIRQ
LFRAME*/FWH4
LDRQ0*
LDRQ1*
LAD0/FWH0
LAD1/FWH1
LAD2/FWH2
LAD3/FWH3
SUSCLK
INTRUDER*
RTCRST*
PWROK
RSMRST*
VCCRTC
VBIAS
RTCX1
RTCX2
NC
NC
SUS_STAT*/LPCPD
VRMPWRGD
THERMTRIP*
THRM*
SMILINK0
SMLINK1
SMBDATA
SMBCLK
SMBALERT*/GPIO11
SPKR
CLK14
GPIO06
GPIO07
GPIO08
GPIO12
GPIO13
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO25
GPIO27
GPIO28
SLP_S3*
SLP_S4*
SLP_S5*
RI*
PWRBTN*
SYS_RST*
LANRST*
TP0
ICH_GPIO06_GPIO07
ICH_GPIO08
IO_SMI*
IO_PME*
TP_ICH_GP18
TP_ICH_GP19
TP_ICH_GP20
GPIO21_ISA_NOGO
TP_ICH_GPIO22
TP_ICH_GPIO23
TP_ICH_GPIO24
GPIO_GRN_BLNK
GPIO_YLW_BLNK
GPIO_LAN_DISABLE*
SLP_S3*
SLP_S4*
TP_SLP_S5*
ICH_RI_PU
SW_ON*
SYS_RST*
GPIO_LAN_DISABLE*
ICH_TP0_PU
SUS_STAT_PU*
ICH_VRMPWRGD_PU
H_THERMTRIP_ICH*
ICH_THRM_PU*
SMB_DATA_MAIN
SMB_CLK_MAIN
SMB_ALERT_PU
SPKR
CK_14M_ICH
V_3P3_STBY
R8F2
FP_RST*
R8F12
USB_BPL_P0
USB_BPL_P0*
USB_ICH_P1
USB_ICH_P1*
USB_BPL_P2
USB_BPL_P2*
USB_FP_P3
USB_FP_P3*
USB_BPR_P4
USB_BPR_P4*
USB_FP_P5
USB_FP_P5*
USB_ICH_BPL_OC*
USB_ICH_CNR_OC*
USB_ICH_FP_OC*
USB_ICH_BPR_OC*
USBP_0
USBP_0*
USBP_1
USBP_1*
USBP_2
USBP_2*
USBP_3
USBP_3*
USBP_4
USBP_4*
USBP_5
USBP_5*
OC*<0>
OC*<1>
OC*<2>
OC*<3>
OC*<4>
OC*<5>
GPO_AUD_EN*
BOARDID<3..0>
CDC_DWN_ENAB*
CK_48M_ICH_USB
TP_GPIO_NO_POP*
TP_ICH_GPIO34
TP_ICH_GPIO35
TP_ICH_GPIO36
TP_ICH_GPIO41
TP_ICH_GPIO42
GPIO32
GPIO33
GPIO34
GPIO35
GPIO36
GPIO37
GPIO38
GPIO39
GPIO40
GPIO41
GPIO42
GPIO43
CLK48
USBRBIAS*
USBRBIAS
HI<10..0>
HI_STBS
HI_STBF
HICOMP
HISWING
HIREF
CLK66
HI_RCOMP_ICH
HI_VSWING_ICH
HI_VREF_ICH
CK_66M_ICH
LANRXD0
LANRXD1
LANRXD2
LANTXD0
LANTXD1
LANTXD2
LANRSTSYNC
LANCLK
EE_DIN
EE_CS
EE_SHCLK
EE_DOUT
ACSYNC
ACSDOUT
ACBITCLK
ACRST*
ACSDIN0
ACSDIN1
ACSDIN2
R8E22
ICH_LAN_RXD0
ICH_LAN_RXD1
ICH_LAN_RXD2
ICH_LAN_TXD0
ICH_LAN_TXD1
ICH_LAN_TXD2
ICH_LAN_RST
ICH_LAN_CLK
ICH_EE_DIN
ICH_EE_CS
ICH_EE_CLK
ICH_EE_DOUT
AUD_LINK_SYNC_R
AUD_LINK_SDO_R
AUD_LINK_BCLK
AUD_LINK_RST*
AUD_LINK_SDI0_CNR
AUD_LINK_SDI1_CNR
AUD_LINK_SDI2
SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD
PAGE TITLE:
LPC/HI/LAN/AC97/USB/GPIO/MISC
REV: 02.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
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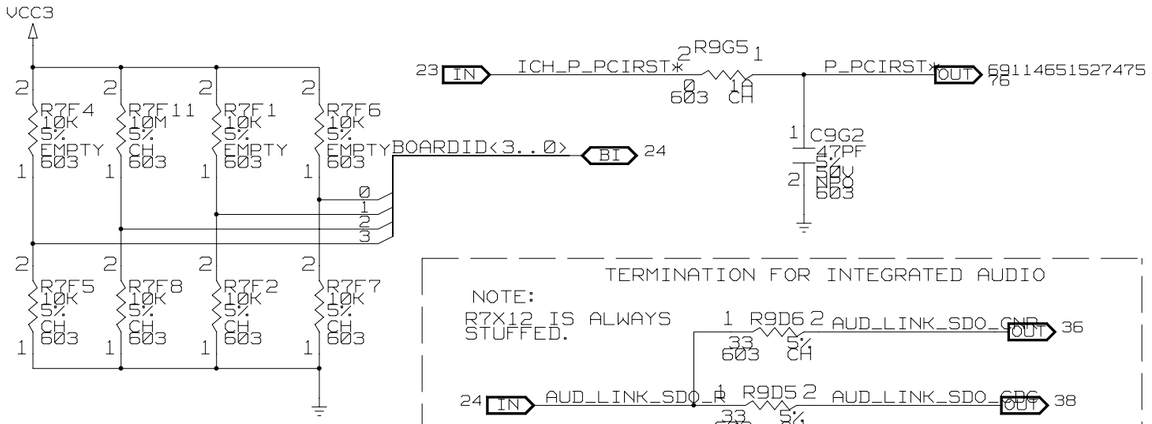
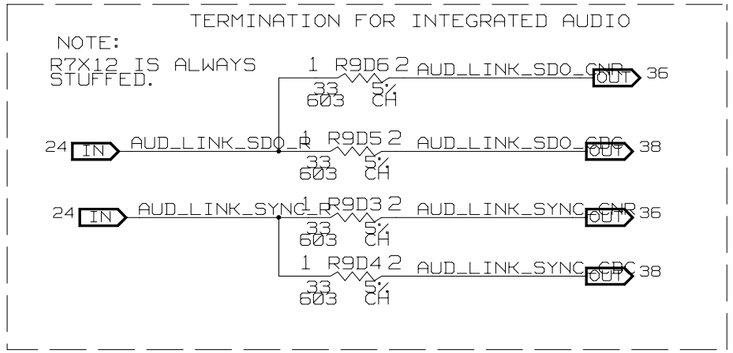
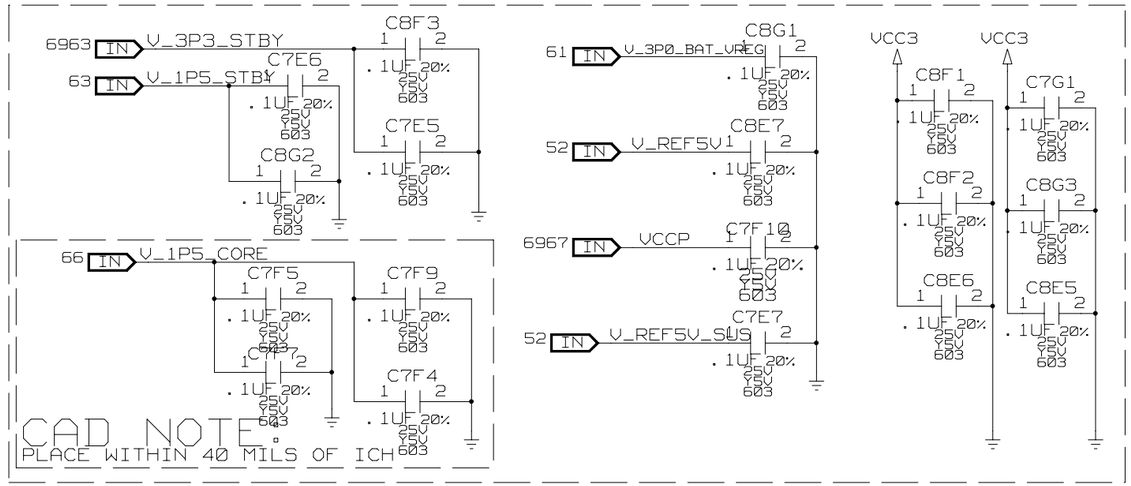
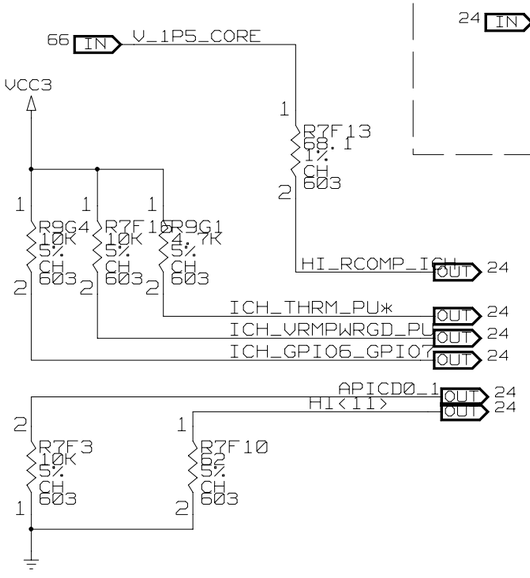
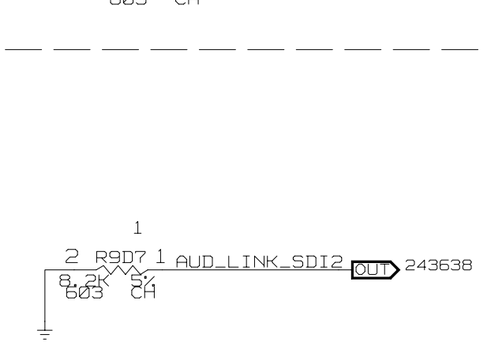
LAST REVISED:
SEPT 13, 2002
SHEET:
24
ICH4

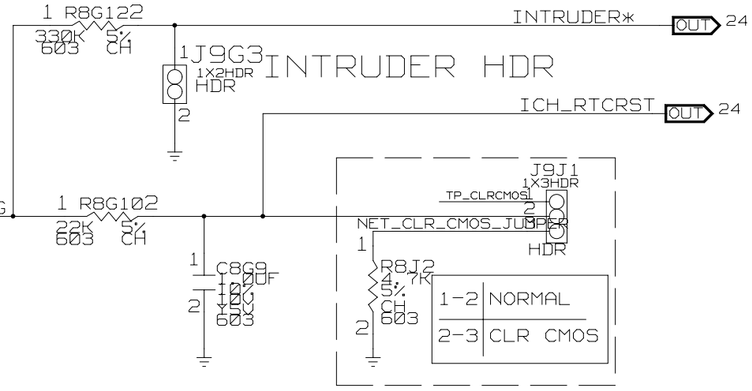


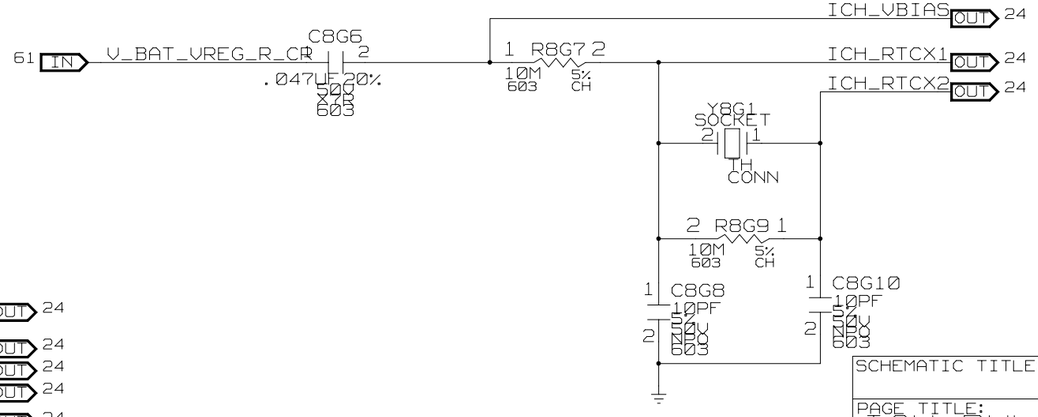


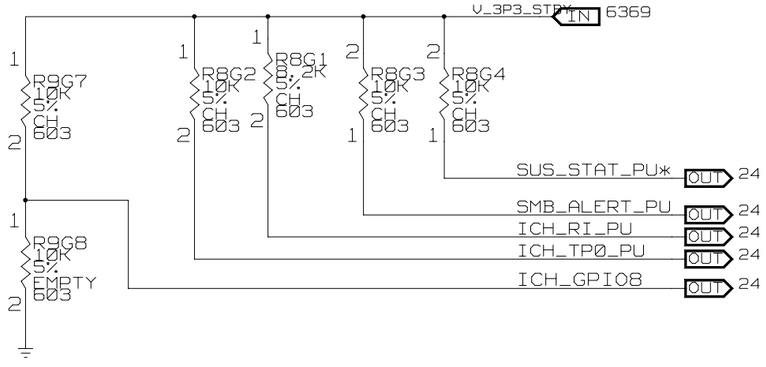












ICH4

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: ICH PULLUPS & DECOUPLING

REV: 02.0

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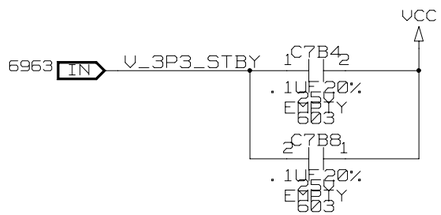
ICH AND CNR LINK

CAD NOTE:

PLACE THESE R-PACKS UNDERNEATH THE LAN CHIP, RIGHT BY THE PINS TO MINIMIZE STUB FROM PIN TO R-PACK

CNR OPTION FOR LAN-UP SOLUTION



0-OHMS ARE PROVIDED TO MINIMIZE STUBS ON LAN INTERFACE

ICH_360

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: ICH: CNR LAN LINK		REV: 02.0
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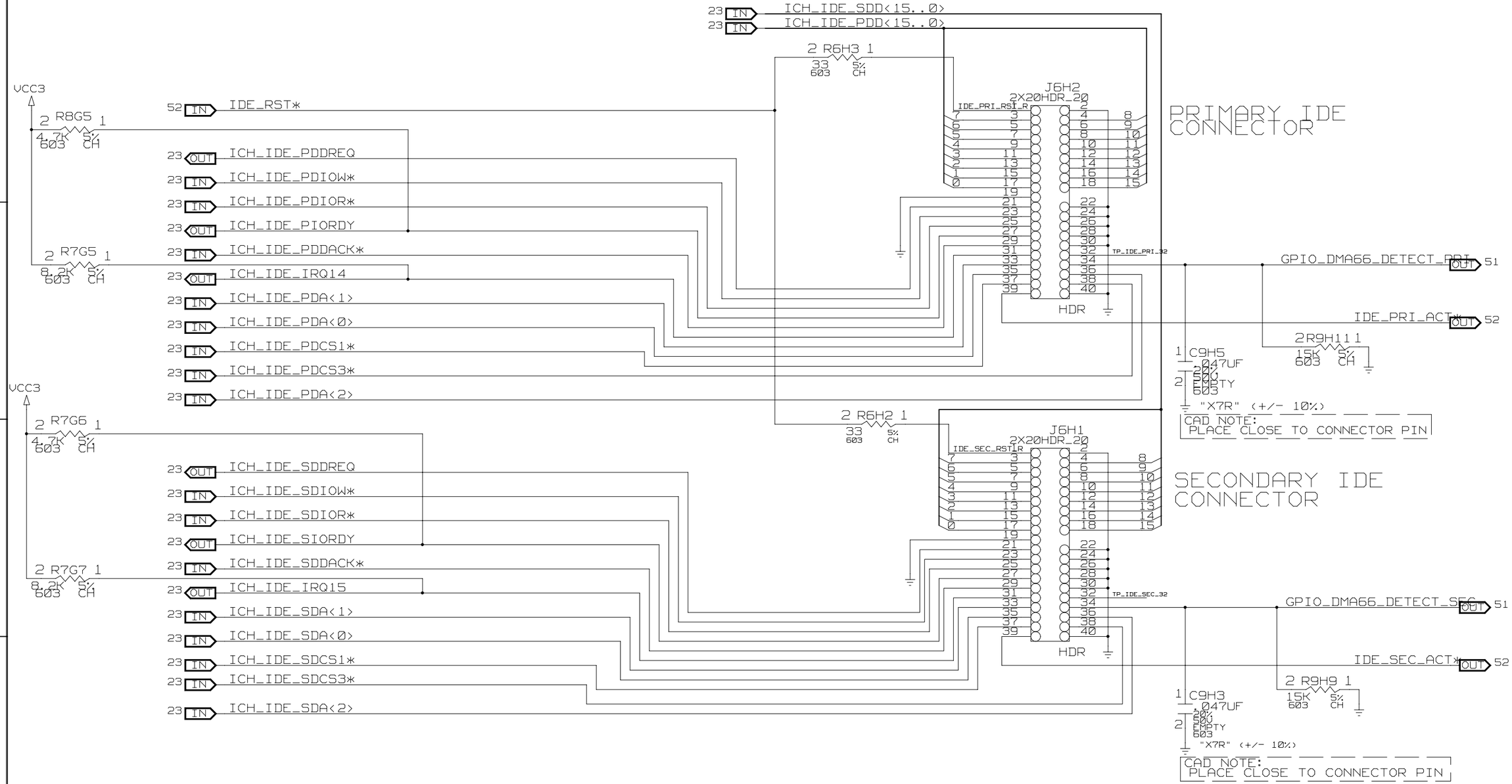

DESIGN NOTE:
DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR*, XIORDY*) WITHIN +/-250MIL
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/-10MIL

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: IDE CONNECTORS

REV: 02.0

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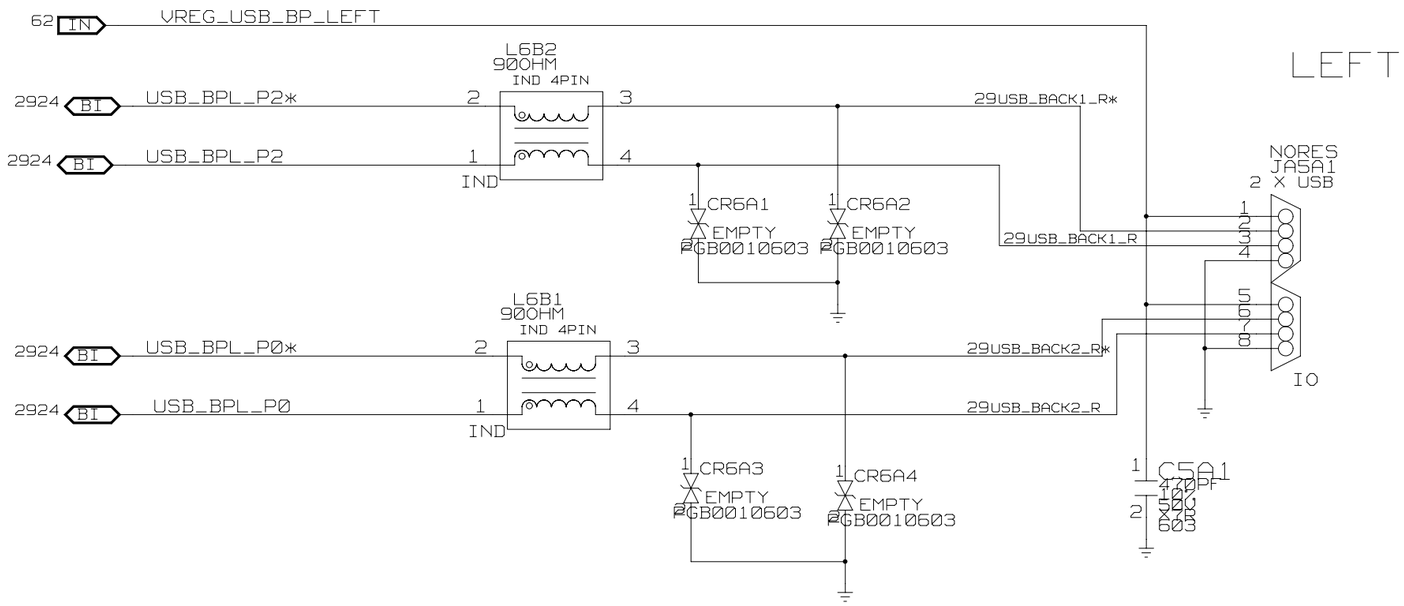

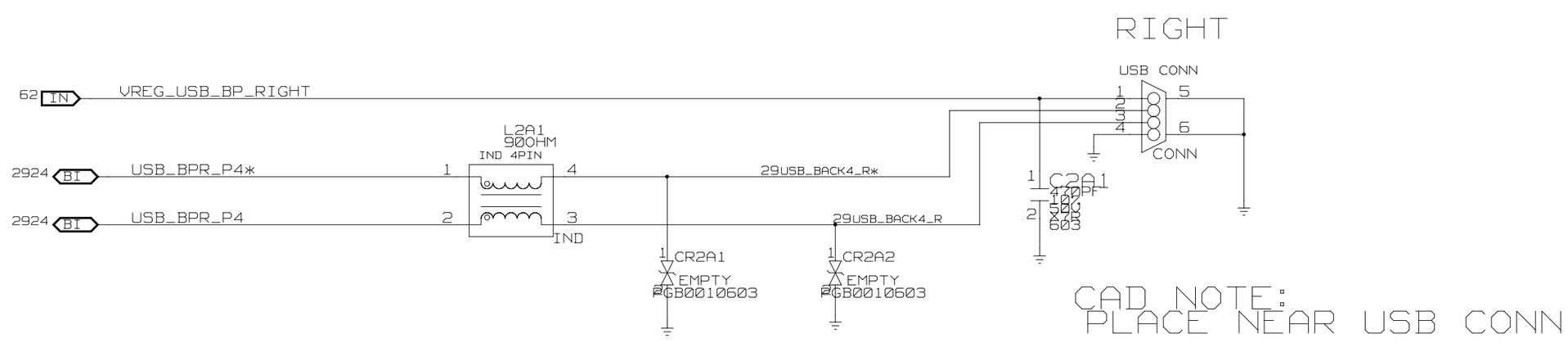

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: USB BACKPANEL		REV: 02.0
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SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD			
PAGE TITLE: BLANK			REV: 02.0
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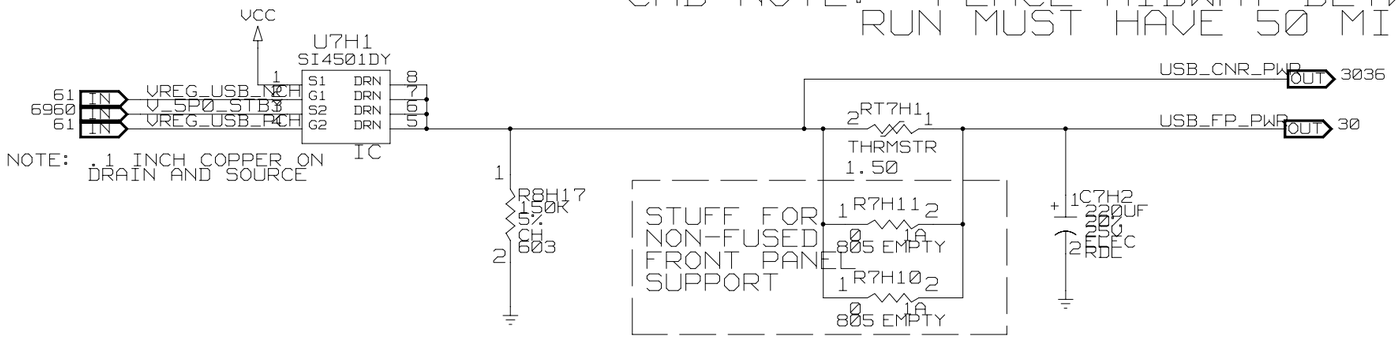
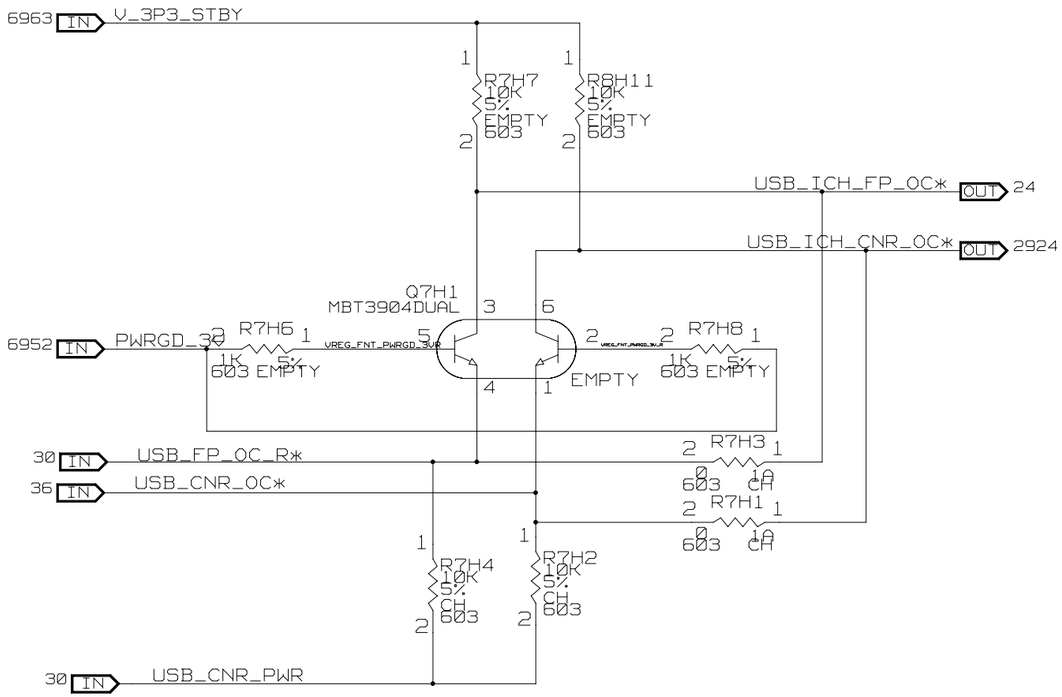
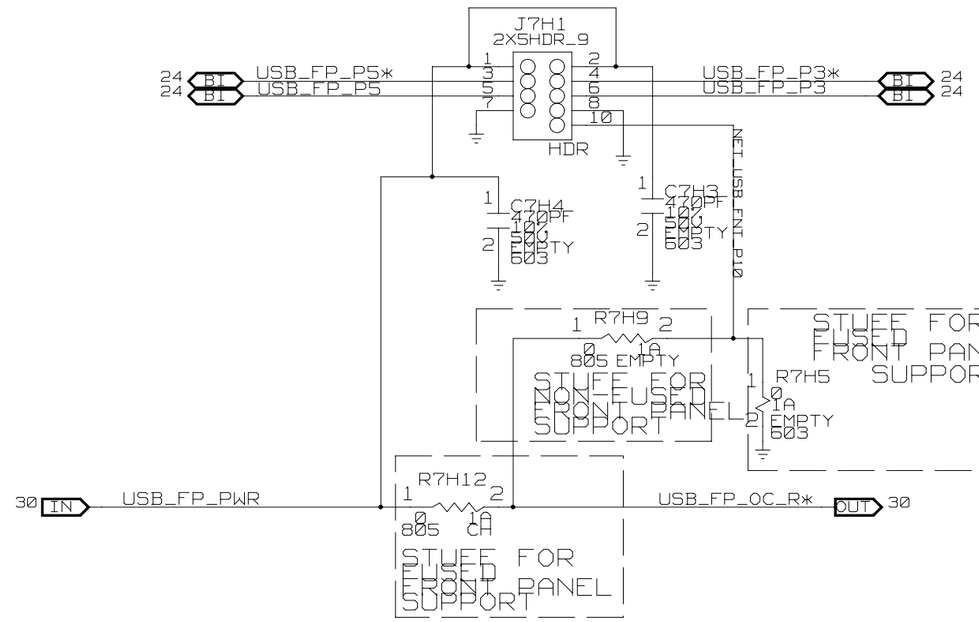
CAD NOTE;
TRACE ROUTING IS 7.5 MIL, 7.5 MIL SPACING

CAD NOTE: PLACE MIDWAY BETWEEN THE FPANEL (2X5) & CNR
RUN MUST HAVE 50 MIL POWER TO BOTH LOCATIONS.







SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: USB FRONT PANEL		REV: 02.0
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PCI SLOT 3

J9B2
PCI CONN2_2 CONN

NC=1,2

SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: PCI SLOT3

REV: 02.0

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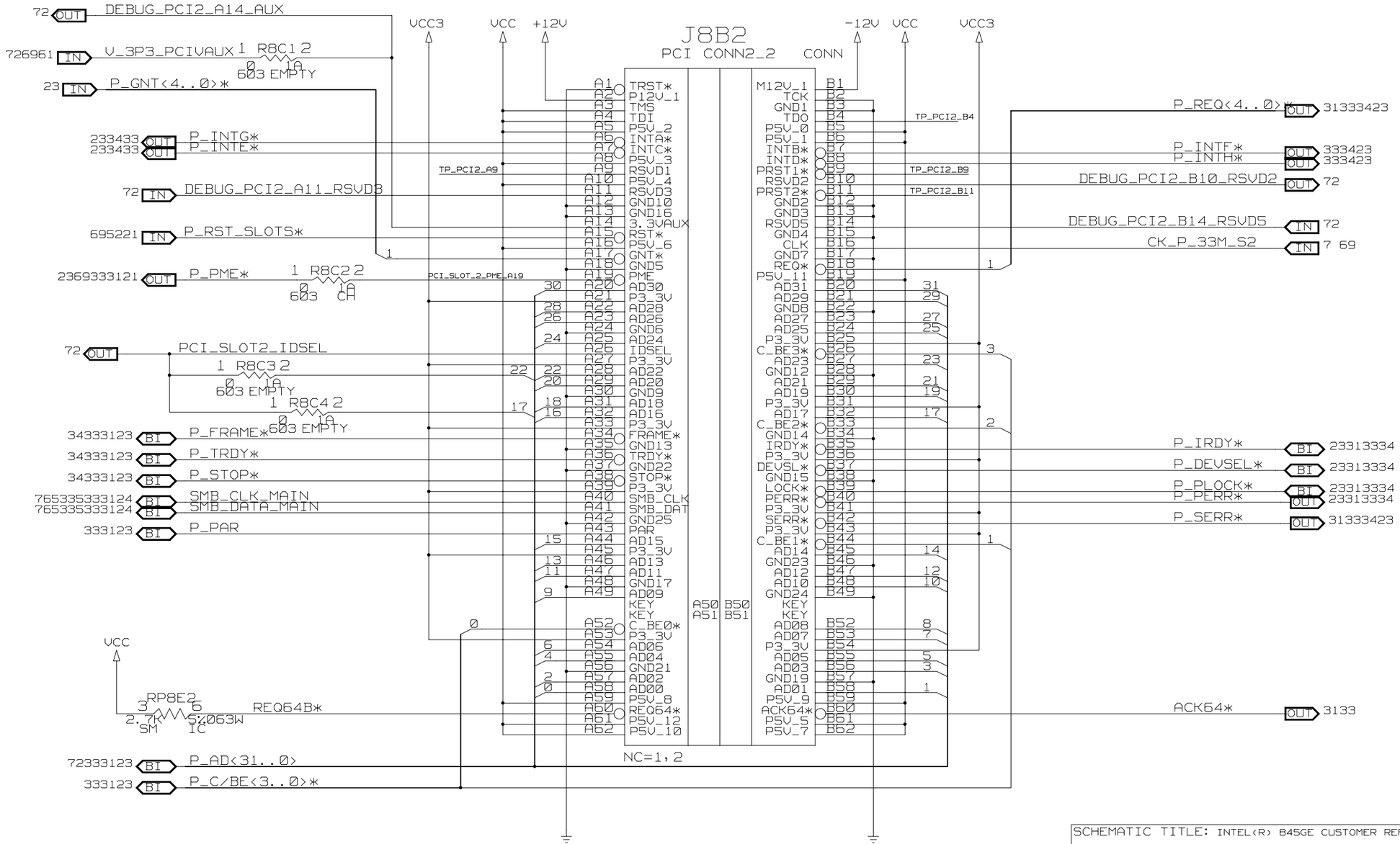
PCI SLOT 2



SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI SLOT2		REV: 02.0
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PCI_SLOT_1
CLOSEST TO AGP

J7B1
PCI CONN2_2 CONN

VCC3 VCC +12V -12V VCC VCC3

726961 IN V_3P3_PCIVAUX
23 IN P_GNT<4..0>*
233432 OUT P_INTF*
233432 OUT P_INTH*
695221 IN P_RST_SLOTS*
2369323121 OUT P_PME*

34323123 BI P_FRAME*
34323123 BI P_TRDY*
34323123 BI P_STOP*
765335323124 BI SMB_CLK_MAIN
765335323124 BI SMB_DATA_MAIN
323123 BI P_PAR

72323123 BI P_AD<31..0>
323123 BI P_C/BE<3..0>*

P_REQ<4..0>* OUT 31323423
P_INTG* OUT 323423
P_INTE* OUT 323423
CK_P_33M_S1 IN 7 69

P_IRDY* BI 23313234
P_DEVSEL* BI 23313234
P_PLOCK* BI 23313234
P_PERR* OUT 23313234
P_SERR* OUT 31323423

3231 IN ACK64*

				TP_PCI1_A1	A1	TRST*	M12V_1 B1
					A2	P12V_1	TCK B2
				TP_PCI1_A3	A3	TMS	GND1 B3
				TP_PCI1_A4	A4	TDI	TDO B4 TP_PCI1_B4
					A5	P5V_2	P5V_0 B5
					A6	INTA*	P5V_1 B6
					A7	INTC*	INTB* B7
					A8	P5V_3	INTD* B8
				TP_PCI1_A9	A9	RSVD1	PRST1* B9 TP_PCI1_B9
					A10	P5V_4	RSVD2 B10 TP_PCI1_B10
				TP_PCI1_A11	A11	RSVD3	PRST2* B11 TP_PCI1_B11
					A12	GND10	GND2 B12
					A13	GND16	GND3 B13
					A14	3.3VAUX	RSVD5 B14 TP_PCI1_B14
					A15	RST*	GND4 B15
					A16	P5V_6	CLK B16
					A17	GNT*	GND7 B17
					A18	GND5	REQ* B18 0
					A19	PME	B19
				30	A20	AD30	P5V_11 B20 31
					A21	P3_3V	AD29 B21 29
				28	A22	AD28	GND8 B22
				26	A23	AD26	AD27 B23 27
					A24	GND6	AD25 B24 25
				24	A25	AD24	P3_3V B25
				16	A26	IDSEL	C_BE3* B26 3
					A27	P3_3V	AD23 B27 23
				22	A28	AD22	GND12 B28
				20	A29	AD20	AD21 B29 21
					A30	GND9	AD19 B30 19
				18	A31	AD18	P3_3V B31
				16	A32	AD16	AD17 B32 17
					A33	P3_3V	C_BE2* B33 2
					A34	FRAME*	GND14 B34
					A35	GND13	IRDY* B35
					A36	TRDY*	P3_3V B36
					A37	GND22	DEVSL* B37
					A38	STOP*	GND15 B38
					A39	P3_3V	LOCK* B39
					A40	SMB_CLK	PERR* B40
					A41	SMB_DAT	P3_3V B41
					A42	GND25	SERR* B42
					A43	PAR	P3_3V B43
				15	A44	AD15	C_BE1* B44 1
					A45	P3_3V	AD14 B45 14
				13	A46	AD13	GND23 B46
				11	A47	AD11	AD12 B47 12
					A48	GND17	AD10 B48 10
				9	A49	AD09	GND24 B49
					KEY		A50 B50 KEY
					KEY		A51 B51 KEY
					A52	C_BE0*	AD08 B52 8
					A53	P3_3V	AD07 B53 7
				6	A54	AD06	P3_3V B54
				4	A55	AD04	AD05 B55 5
					A56	GND21	AD03 B56 3
				2	A57	AD02	GND19 B57
				0	A58	AD00	AD01 B58 1
					A59	P5V_8	P5V_9 B59
					A60	REQ64*	ACK64* B60
					A61	P5V_12	P5V_5 B61
					A62	P5V_10	P5V_7 B62

NC=1,2

VCC
RP8E2
1 8 REQ64A*
2.7K SM 5%063W IC

VCC
RP8E2
7 2
2.7K SM 5%063W IC

SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI SLOT1		REV: 02.0
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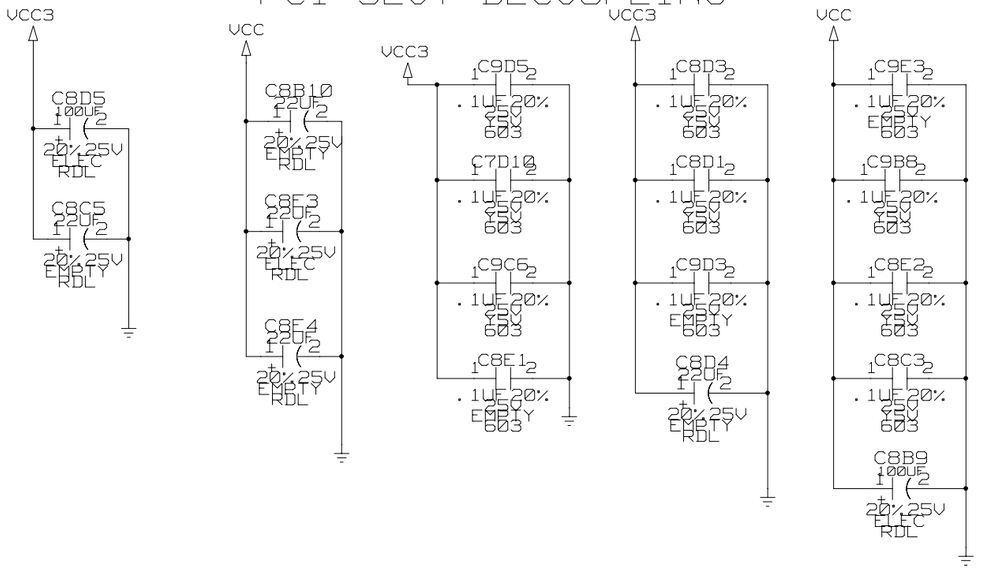
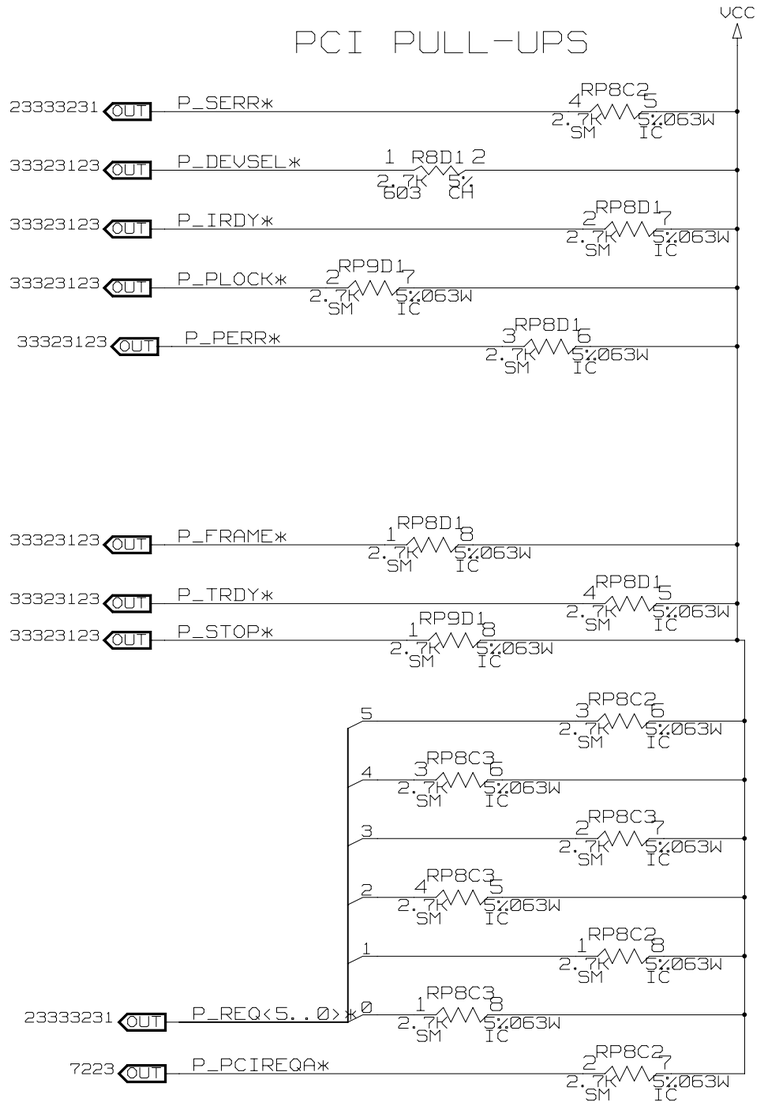
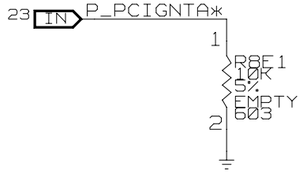
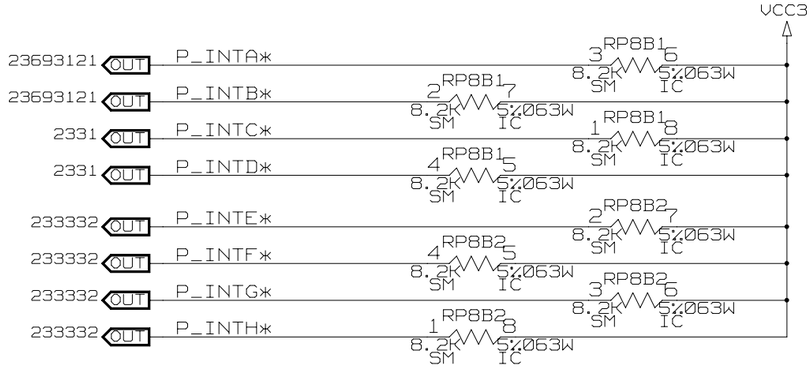
PCI SLOT DECOUPLING



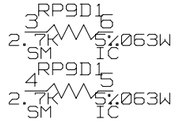
PCI PULL-UPS



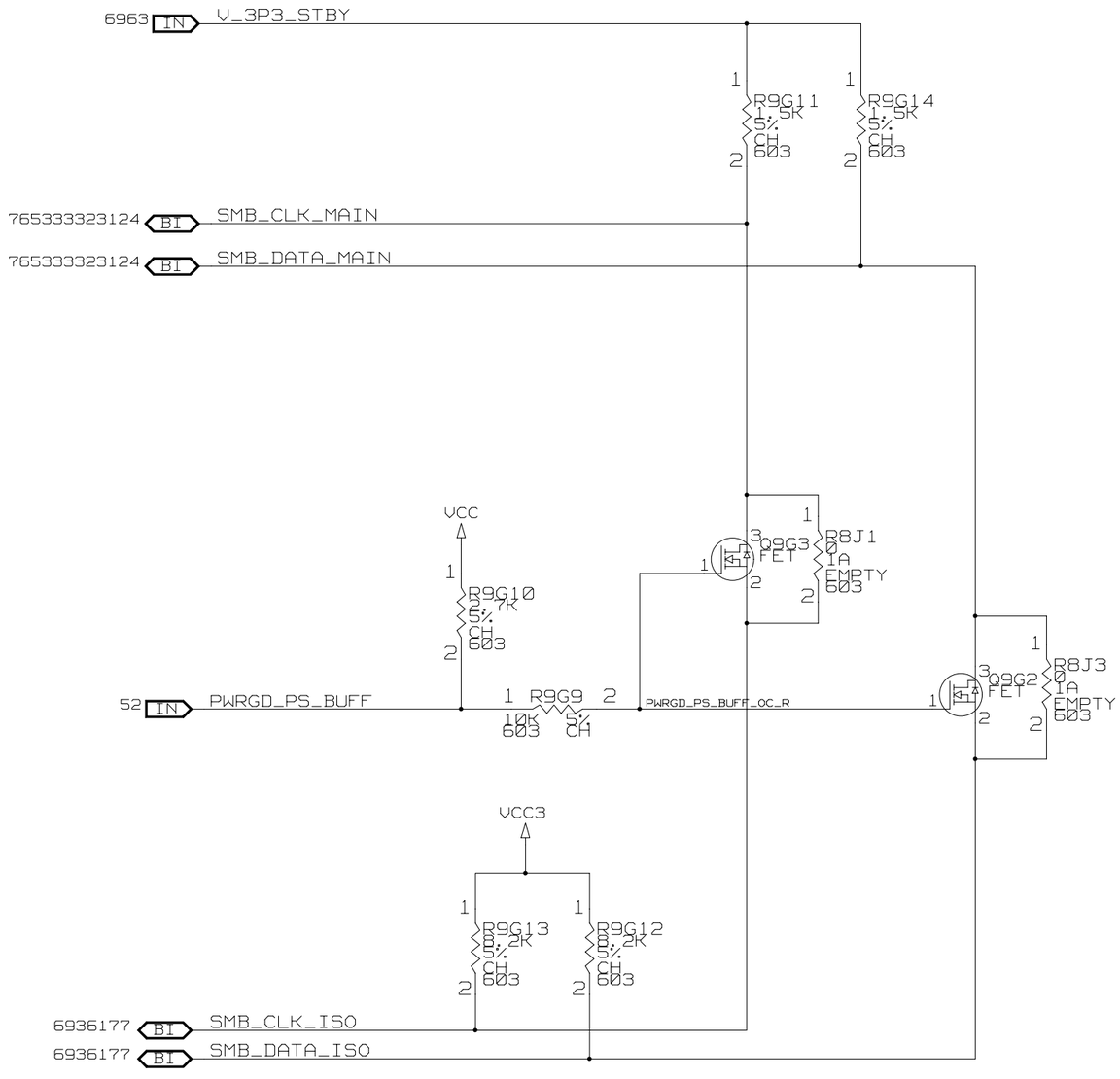


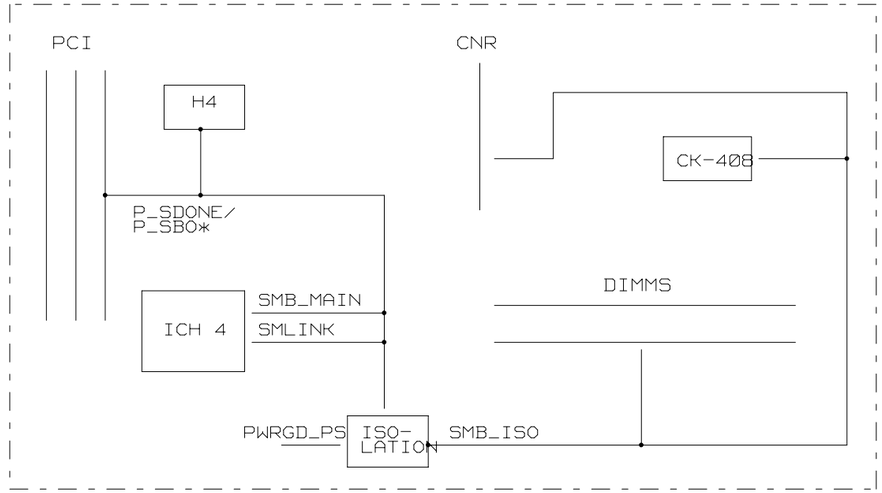


SPARE SECTIONS



SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: ICH PCI TERMINATION		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 34





SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: SMBUS_ISOLATION

REV: 02.0

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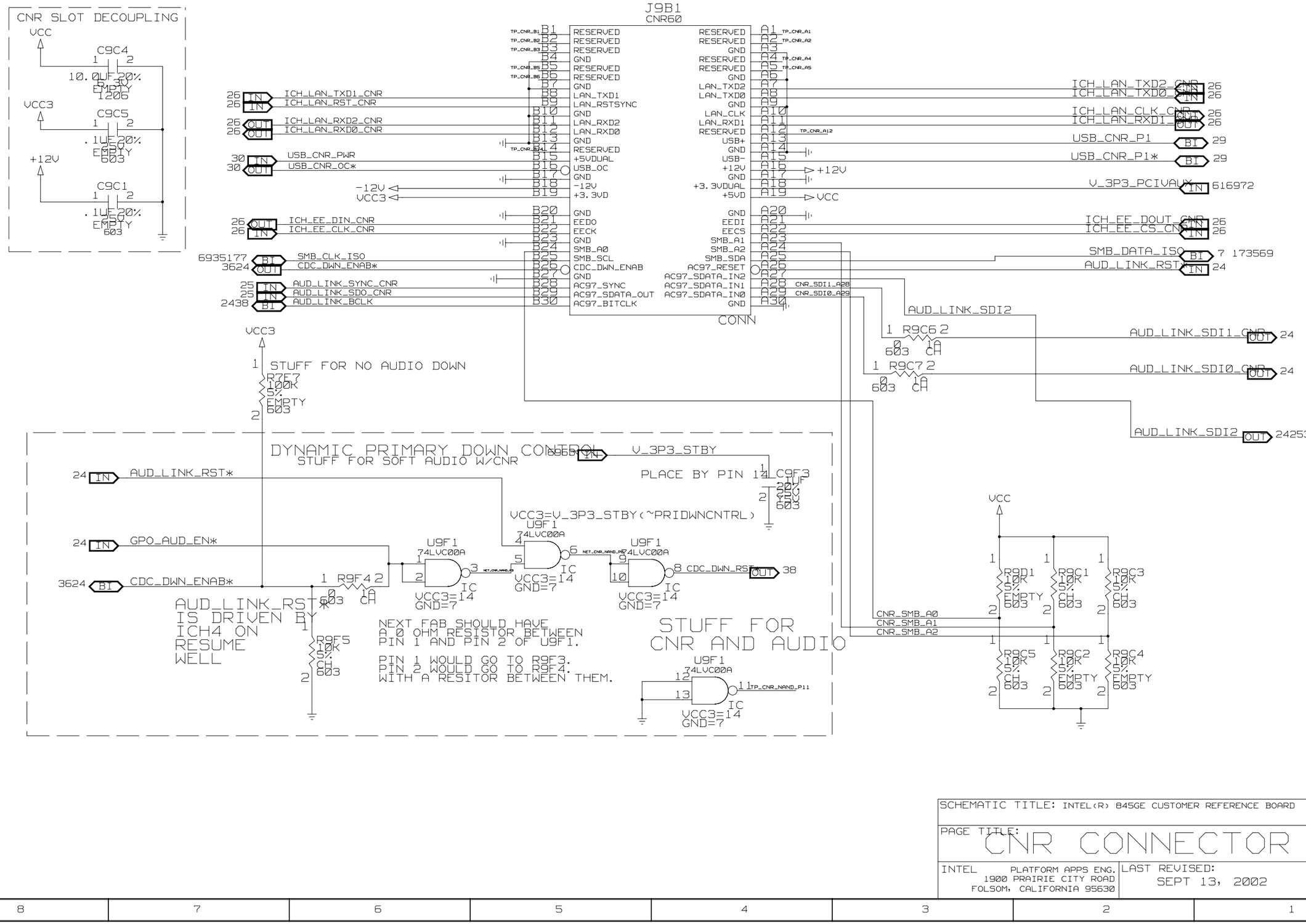
CNR SLOT DECOUPLING
VCC
C9C4
10.0UF 20% 6.3V EMPTY 1206
VCC3
C9C5
.1UF 20% 16V EMPTY 603
+12V
C9C1
.1UF 20% 50V EMPTY 603
J9B1
CNR60
RESERVED
GND
LAN_TXD1
LAN_RSTSYNC
LAN_RXD2
LAN_RXD0
+5VDUAL
USB_OC
-12V
+3.3VD
EEDO
EECK
SMB_A0
SMB_SCL
CDC_DWN_ENAB
AC97_SYNC
AC97_SDATA_OUT
AC97_BITCLK
LAN_TXD2
LAN_TXD0
LAN_CLK
LAN_RXD1
USB+
USB-
+12V
+3.3VDUAL
+5VD
EEDI
EECS
SMB_A1
SMB_A2
SMB_SDA
AC97_RESET
AC97_SDATA_IN2
AC97_SDATA_IN1
AC97_SDATA_IN0
CONN
ICH_LAN_TXD1_CNR
ICH_LAN_RST_CNR
ICH_LAN_RXD2_CNR
ICH_LAN_RXD0_CNR
USB_CNR_PWR
USB_CNR_OC*
ICH_EE_DIN_CNR
ICH_EE_CLK_CNR
SMB_CLK_ISO
CDC_DWN_ENAB*
AUD_LINK_SYNC_CNR
AUD_LINK_SDO_CNR
AUD_LINK_BCLK
ICH_LAN_TXD2_CNR
ICH_LAN_TXD0_CNR
ICH_LAN_CLK_CNR
ICH_LAN_RXD1_CNR
USB_CNR_P1
USB_CNR_P1*
V_3P3_PCIVAUX
ICH_EE_DOUT_CNR
ICH_EE_CS_CNR
SMB_DATA_ISO
AUD_LINK_RST*
AUD_LINK_SDI2
AUD_LINK_SDI1_CNR
AUD_LINK_SDI0_CNR
CNR_SDI1_A28
CNR_SDI0_A29
R9C62 0 603 1A CH
R9C72 0 603 1A CH
VCC3
STUFF FOR NO AUDIO DOWN
R7E7 100K 5% EMPTY 603
DYNAMIC PRIMARY DOWN CONTROL
STUFF FOR SOFT AUDIO W/CNR
V_3P3_STBY
PLACE BY PIN 14 C9F3 .1UF 20% 16V CER 603
VCC3=V_3P3_STBY(~PRIDWNCNTRL)
U9F1 74LVC00A
GPO_AUD_EN*
CDC_DWN_ENAB*
R9F42 0 603 1A CH
CDC_DWN_RST
AUD_LINK_RST* IS DRIVEN BY ICH4 ON RESUME WELL
R9F5 10K 5% CH 603
NEXT FAB SHOULD HAVE A 0 OHM RESISTOR BETWEEN PIN 1 AND PIN 2 OF U9F1.
PIN 1 WOULD GO TO R9F3.
PIN 2 WOULD GO TO R9F4.
WITH A RESITOR BETWEEN THEM.
STUFF FOR CNR AND AUDIO
TP_CNR_NAND_P11
VCC3=14
GND=7
IC
R9D1 10K 5% EMPTY 603
R9C1 10K 5% CH 603
R9C3 10K 5% CH 603
R9C5 10K 5% CH 603
R9C2 10K 5% EMPTY 603
R9C4 10K 5% EMPTY 603
CNR_SMB_A0
CNR_SMB_A1
CNR_SMB_A2
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD
PAGE TITLE: CNR CONNECTOR
REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
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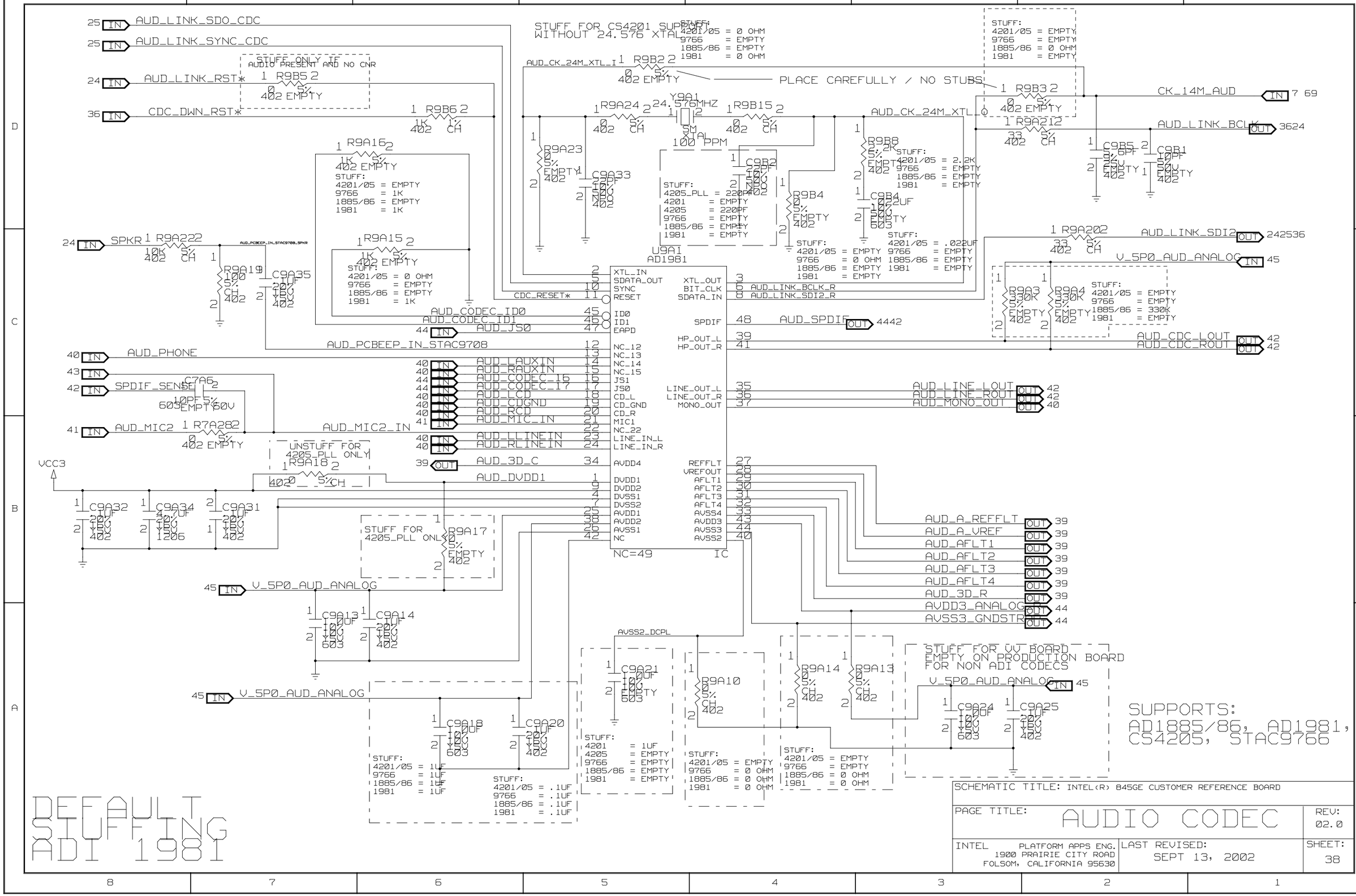
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: BLANK		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 37


AUD_LINK_SDO_CDC
AUD_LINK_SYNC_CDC
AUD_LINK_RST*
CDC_DWN_RST*
STUFF ONLY IF AUDIO PRESENT AND NO CNR
R9B5 0 5% 402 EMPTY
R9B6 1K 1% 402 CA
STUFF FOR CS4201 SUPPORT WITHOUT 24.576 XTAL
STUFF: 4201/05 = 0 OHM 9766 = EMPTY 1885/86 = EMPTY 1981 = 0 OHM
AUD_CK_24M_XTL_I
R9B2 0 5% 402 EMPTY
PLACE CAREFULLY / NO STUBS
Y9A1 24.576MHZ SM XTAL 100 PPM
R9A24 0 5% 402 CA
R9B15 0 5% 402 CA
R9A23 0 5% EMPTY 402
C9A33 22PF 50V NPO 402
C9B2 22PF 50V NPO 402
R9B4 0 5% EMPTY 402
C9B4 .022UF 16V X7R 603
STUFF: 4205_PLL = 220PF 4201 = EMPTY 4205 = 220PF 9766 = EMPTY 1885/86 = EMPTY 1981 = EMPTY
STUFF: 4201/05 = EMPTY 9766 = 0 OHM 1885/86 = EMPTY 1981 = EMPTY
STUFF: 4201/05 = .022UF 9766 = EMPTY 1885/86 = EMPTY 1981 = EMPTY
R9B3 0 5% 402 EMPTY
STUFF: 4201/05 = EMPTY 9766 = EMPTY 1885/86 = 0 OHM 1981 = EMPTY
R9B8 2.2K 5% 402 EMPTY
STUFF: 4201/05 = 2.2K 9766 = EMPTY 1885/86 = EMPTY 1981 = EMPTY
R9A212 33 5% 402 CA
C9B5 5.0PF 50V NPO 402 EMPTY
C9B1 50PF 50V NPO 402 EMPTY
CK_14M_AUD
AUD_LINK_BCLK
R9A16 1K 5% 402 EMPTY
STUFF: 4201/05 = EMPTY 9766 = 1K 1885/86 = EMPTY 1981 = 1K
R9A15 1K 5% 402 EMPTY
STUFF: 4201/05 = 0 OHM 9766 = EMPTY 1885/86 = EMPTY 1981 = 1K
SPKR
R9A222 10K 5% 402 CA
AUD_PCBEEP_IN_STAC9708_SPKR
R9A19 100 5% CH 402
C9A35 .1UF 10V X7R 402
U9A1 AD1981
XTL_IN
SDATA_OUT
SYNC
RESET
ID0
ID1
EAPD
NC_12
NC_13
NC_14
NC_15
JS1
JS0
CD_L
CD_GND
CD_R
MIC1
NC_22
LINE_IN_L
LINE_IN_R
AVDD4
DVDD1
DVDD2
DVSS1
DVSS2
AVDD1
AVDD2
AVSS1
NC
NC=49
XTL_OUT
BIT_CLK
SDATA_IN
SPDIF
HP_OUT_L
HP_OUT_R
LINE_OUT_L
LINE_OUT_R
MONO_OUT
REFFLT
VREFOUT
AFLT1
AFLT2
AFLT3
AFLT4
AVSS4
AVDD3
AVSS3
AVSS2
IC
CDC_RESET*
AUD_CODEC_ID0
AUD_CODEC_ID1
AUD_JS0
AUD_PCBEEP_IN_STAC9708
AUD_PHONE
SPDIF_SENSE
C7A6 10PF 5% 603 EMPTY 50V
AUD_MIC2
R7A282 0 5% 402 EMPTY
AUD_MIC2_IN
AUD_LAUXIN
AUD_RAUXIN
AUD_CODEC_I6
AUD_CODEC_I7
AUD_LCD
AUD_CDGND
AUD_RCD
AUD_MIC_IN
AUD_LLINEIN
AUD_RLINEIN
AUD_3D_C
AUD_DVDD1
UNSTUFF FOR 4205_PLL ONLY
R9A18 0 5% CH 402
STUFF FOR 4205_PLL ONLY
R9A17 0 5% EMPTY 402
VCC3
C9A32 .1UF 10V X7R 402
C9A34 4.7UF 10V X5R 1206
C9A31 .1UF 10V X7R 402
V_5P0_AUD_ANALOG
C9A13 10UF 10V X5R 603
C9A14 .1UF 10V X7R 402
AVSS2_DCPL
C9A21 10UF 10V X5R 603
STUFF: 4201 = 1UF 4205 = EMPTY 9766 = EMPTY 1885/86 = EMPTY 1981 = EMPTY
R9A10 0 5% CH 402
STUFF: 4201/05 = EMPTY 9766 = 0 OHM 1885/86 = 0 OHM 1981 = 0 OHM
R9A14 0 5% CH 402
R9A13 0 5% CH 402
STUFF: 4201/05 = EMPTY 9766 = EMPTY 1885/86 = 0 OHM 1981 = 0 OHM
STUFF FOR VV BOARD EMPTY ON PRODUCTION BOARD FOR NON ADI CODECS
C9A24 10UF 10V X5R 603
C9A25 .1UF 10V X7R 402
STUFF: 4201/05 = 1UF 9766 = 1UF 1885/86 = 1UF 1981 = 1UF
STUFF: 4201/05 = .1UF 9766 = .1UF 1885/86 = .1UF 1981 = .1UF
R9A202 33 5% 402 CA
AUD_LINK_SDI2
R9A3 330K 5% EMPTY 402
R9A4 330K 5% EMPTY 402
STUFF: 4201/05 = EMPTY 9766 = EMPTY 1885/86 = 330K 1981 = EMPTY
AUD_CDC_LOUT
AUD_CDC_ROUT
AUD_SPDIF
AUD_LINE_LOUT
AUD_LINE_ROUT
AUD_MONO_OUT
AUD_A_REFFLT
AUD_A_VREF
AUD_AFLT1
AUD_AFLT2
AUD_AFLT3
AUD_AFLT4
AUD_3D_R
AVDD3_ANALOG
AVSS3_GNDSTR
SUPPORTS: AD1885/86, AD1981, CS4205, STAC9766
DEFAULT STUFFING ADI 1981
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD
PAGE TITLE: AUDIO CODEC
REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
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KEEP CAPS AS CLOSE AS POSSIBLE TO AC97 CODEC.

38 IN AUD_A_REFFLT

38 IN AUD_A_VREF

STUFF:
4201/05 = .1UF
9766 = EMPTY
1885/86 = .1UF
1981 = EMPTY

C9A12 1UF 20% 10V X5R 402

STUFF:
4201/05 = EMPTY
9766 = EMPTY
1885/86 = 10UF
1981 = 10UF

C9A1 10UF 20% 10V X5R EMPTY

38 IN AUD_AFLT1
38 IN AUD_AFLT2
38 IN AUD_AFLT3
38 IN AUD_AFLT4

38 IN AUD_3D_R

38 IN AUD_3D_C

C9A17 .1UF 20% 16V X7R EMPTY 402

STUFF:
4201 = 1000PF
4205 = EMPTY
9766 = EMPTY
1885/86 = .1UF
1981 = EMPTY

C9A16 .047UF 20% 16V X7R EMPTY 402

STUFF:
4201/05 = EMPTY
9766 = EMPTY
1885/86 = .047UF
1981 = EMPTY

R9A2 0 5% EMPTY 402

STUFF:
4201 = 0 OHM
4205 = EMPTY
9766 = EMPTY
1885/86 = EMPTY
1981 = EMPTY

C9A9 1UF 20% 10V X5R EMPTY 805

STUFF:
4201/05 = 2.2UF
9766 = 1UF
1885/86 = EMPTY
1981 = EMPTY

C9A5 1UF 20% 10V X5R EMPTY 402

STUFF:
4201 = .01UF
4205 = EMPTY
9766 = .1UF
1885/86 = .1UF
1981 = EMPTY

C9A4 270PF 5% 50V NPO 603

STUFF:
4201 = 1UF
4205 = EMPTY
9766 = 1UF
1885/86 = 1UF
1981 = 270PF

C9A10 270PF 5% 50V NPO 603

STUFF:
4201 = EMPTY
4205 = 1000PF
9766 = EMPTY
1885/86 = 1UF
1981 = 270PF

C9A11 270PF 5% 50V NPO 603

C9A3 270PF 5% 50V NPO 603

STUFF:
4201/05 = 1000PF
9766 = 470PF
1885/86 = 270PF
1981 = 270PF

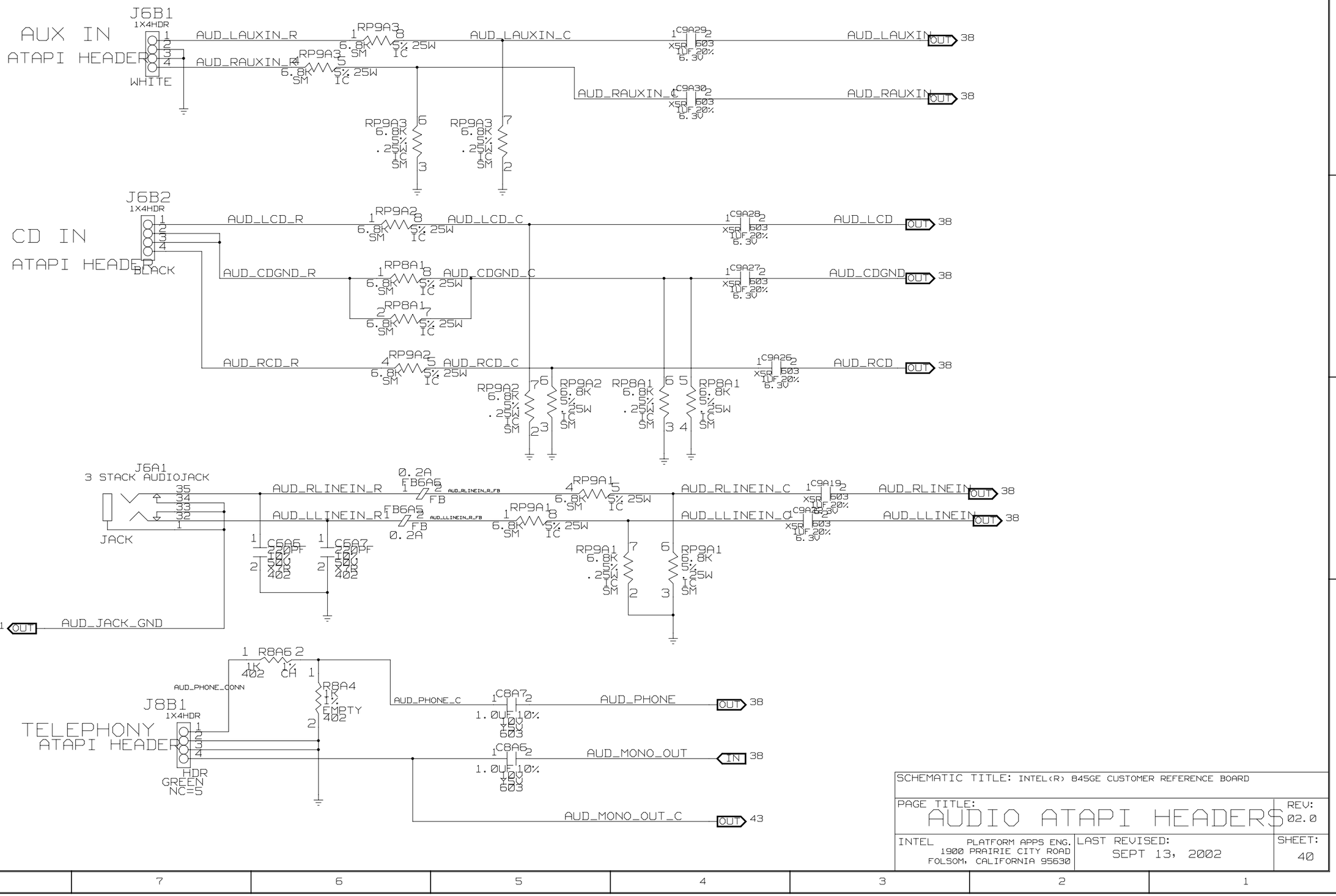
C9A2 1UF 20% 10V X5R 402

STUFF:
4201/05 = .1UF
9766 = .1UF
1885/86 = .1UF
1981 = .1UF

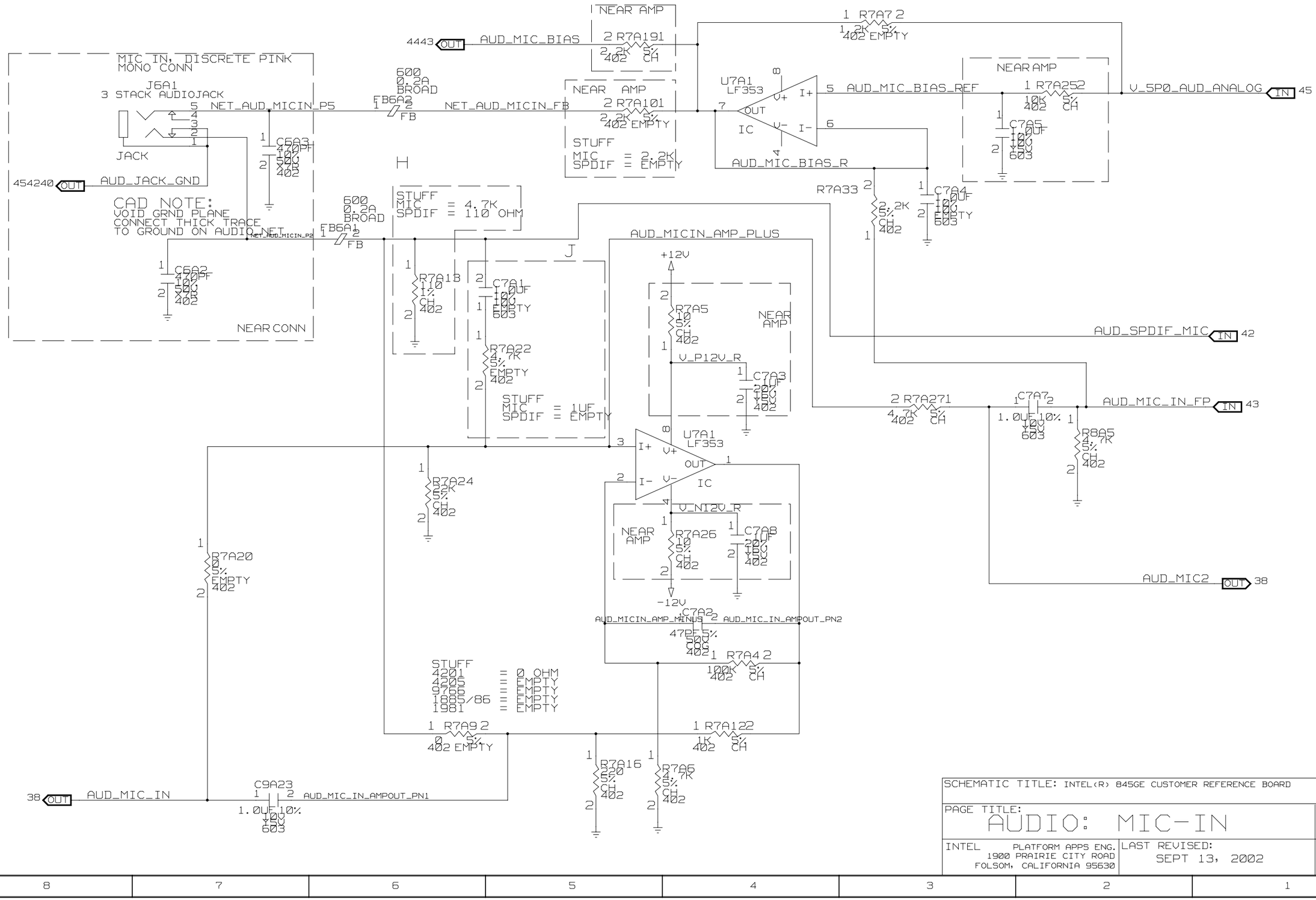
CODEC FILTER CAPS:
1981, 1885/86, 4205, 9766

DEFAULT STUFFING ADI 1981

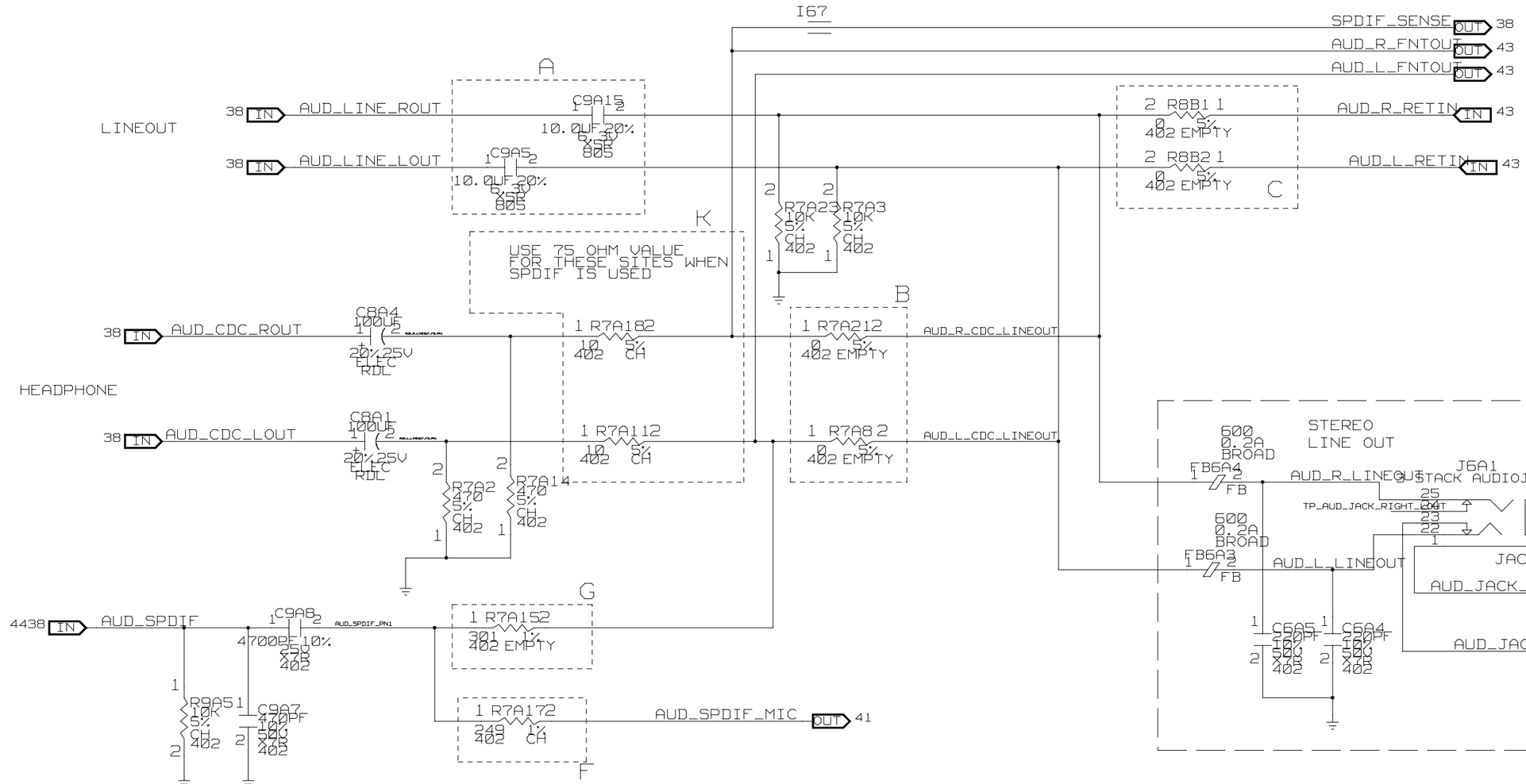
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: AUDIO CODEC FILTERING CAPS		REV: A02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 39



SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: AUDIO ATAPI HEADERS		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 40



SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: AUDIO: MIC-IN		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 41



	BP ONLY	FP-->BP
HEADPHONE	STUFF B EMPTY A, C	STUFF C EMPTY A, B
LINEOUT	STUFF A EMPTY B, C	N/A

SPDIF	BP LO	BP MIC
F	EMPTY	STUFF
G	STUFF	EMPTY
H	EMPTY	110 OHM
J	STUFF	EMPTY
K	75 OHM	10 OHM

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: AUDIO: LINE-OUT

REV: 02.0

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

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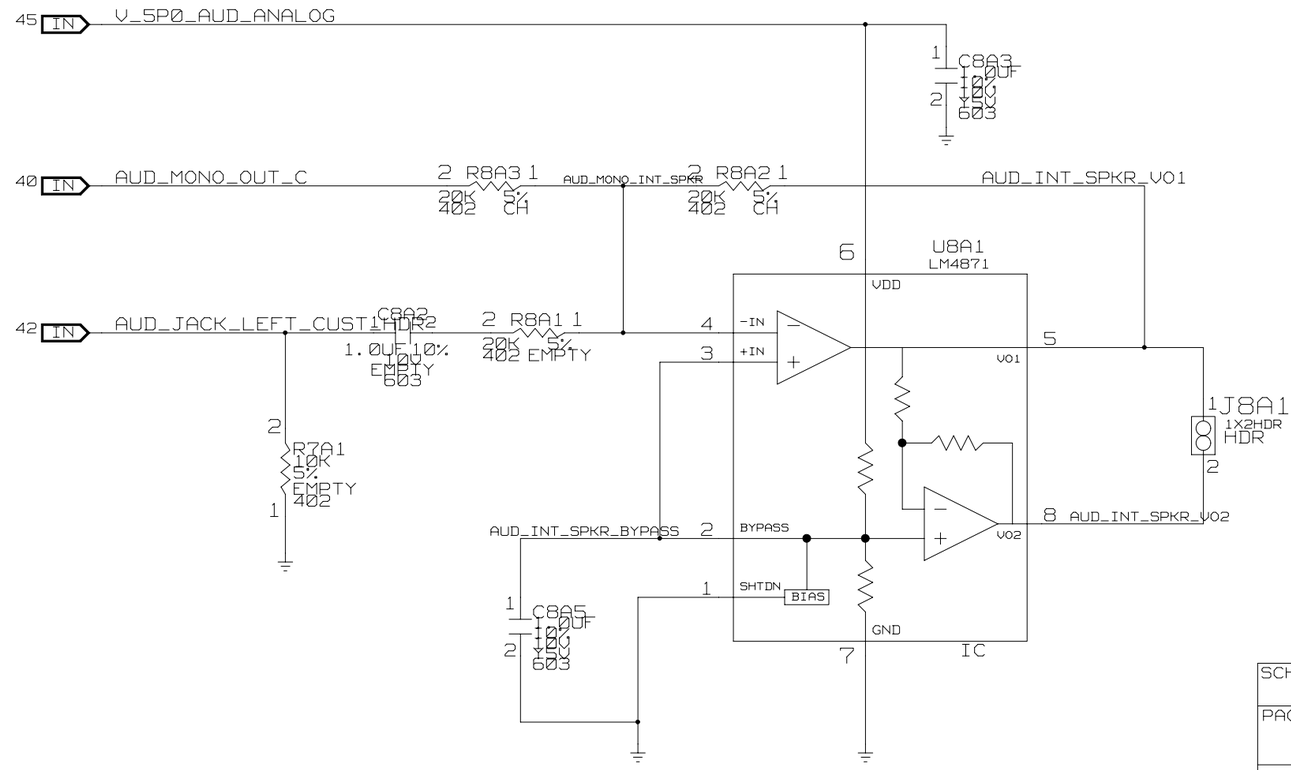
NOTE:
FP DONGLE MUST HAVE MIC JACK RING SHUNT SPRING TERMINAL CONNECTED TO GND FOR PROPER MIC SENSING OPERATION

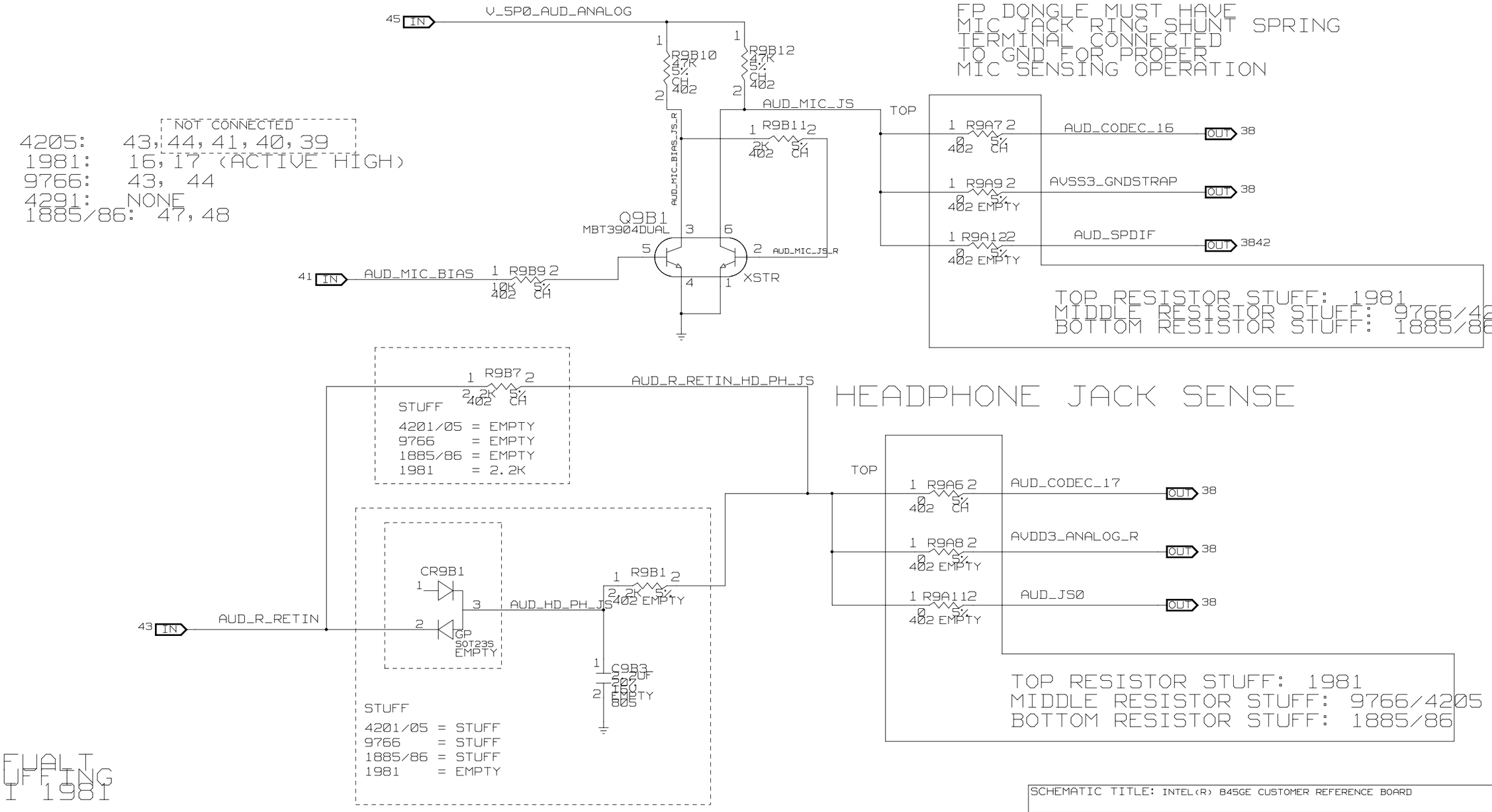
AUDIO FRONT PANEL
PLACE NEAR AUDIO CIRCUIT

INTERNAL SPEAKER CIRCUIT



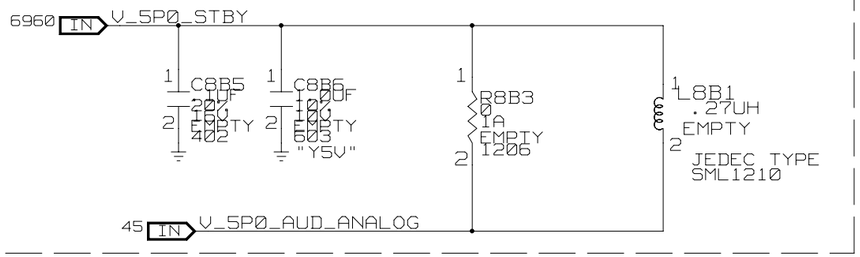
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: AUDIO_FRONT PANEL		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 43

MIC JACK SENSE

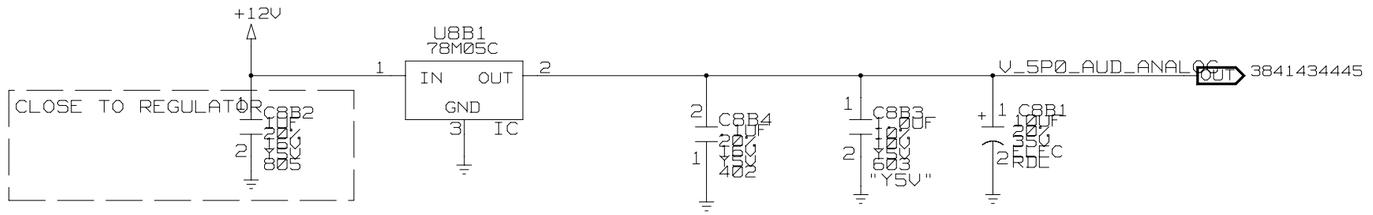


SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: JACK SENSE		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 44

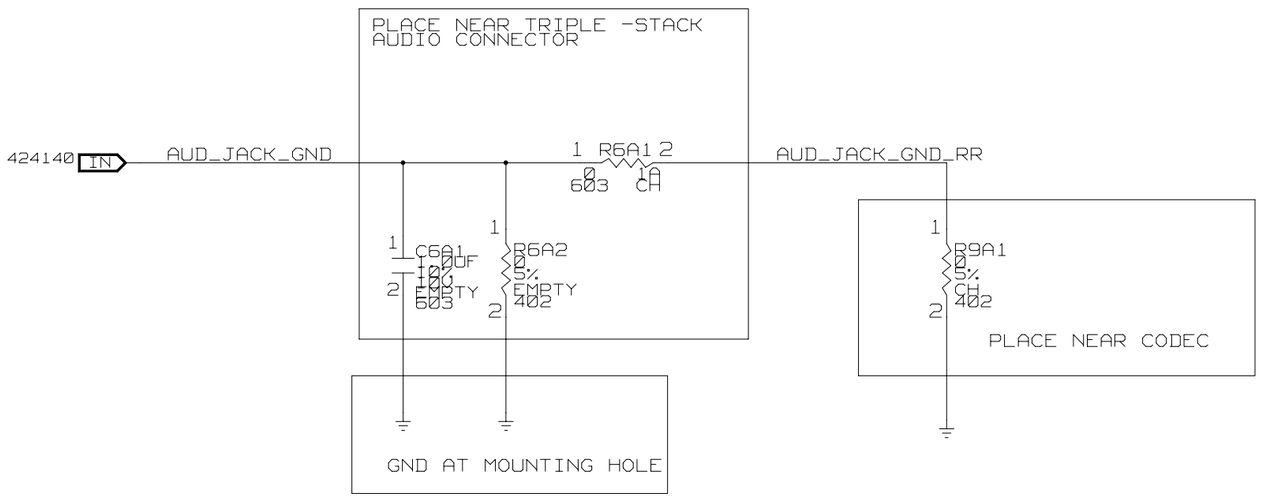
SPECIAL OPTION



REGULATOR THERMAL TAB SHOULD BE SOLDERED TO A COPPER PAD THAT IS LARGE ENOUGH TO ALLOW 5 TO 10 GROUND VIAS AROUND THE COMPONENT FOR COOLING



NOTE:
LAYOUT SHOULD GO FROM PIN 2 TO CAPS AND THEN THROUGH SEVERAL VIAS TO V_5P0_AUD_ANALOG



SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: AUDIO VREG		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 45

SPARE SECTIONS

TP_RP10_10000_4

RP1H1 10K 5% .063W IC SM

TP_RP10_10000_5

U1H1
LPC47M102

FLOPPY
- SIO_FDD_DRVDEN0 1 — DRVDEN0/GP40
- SIO_FDD_DRVDEN1 2 — DRVDEN1/GP41
- SIO_FDD_MTR0* 3 — MTR0
- SIO_FDD_DS0* 4 — DS0
- SIO_FDD_DIR* 8 — DIR
- SIO_FDD_STEP* 9 — STEP
- SIO_FDD_WDATA* 10 — WDATA
- SIO_FDD_WGATE* 11 — WGATE
- SIO_FDD_HDSEL* 12 — HDSEL
- SIO_FDD_INDEX* 13 — INDEX
- SIO_FDD_TRK0* 14 — TRK0
- SIO_FDD_WRTPRT* 15 — WRTPRT
- SIO_FDD_RDATA* 16 — RDATA
- SIO_FDD_DSKCHG* 4 — DSKCHG

6963 IN V_3P3_STBY

RP1H1 10K 5% .063W IC SM

24 OUT IO_PME* 17 — IOPME*/GP42

LPC
- 755124 BI L_AD<3..0> — AD0 20, AD1 21, AD2 22, AD3 23
- 24 IN L_FRAME* 24 — FRAME
- DRQ 25
- SIO_PCI_RST* 26 — PCI_RESET
- L_PD* 27 — PD
- 697 IN CK_P_33M_SIO 29 — PCI_CLK
- 7224 BI SER_IRQ 30 — SER_IRQ

VCC3

RP1H2 10K 5% .063W IC SM

24 OUT L_DRQ*
6925 IN P_PCIRST*

R1H8 0 603 1A CH

SERIAL 1
- 50 IN SIO_COM_RXD1 84 — RXD1
- 50 OUT SIO_COM_TXD1 85 — TXD1
- 50 IN SIO_COM_DSR1* 86 — DSR1
- 50 OUT SIO_COM_RTS1* 87 — RTS1
- 50 IN SIO_COM_CTS1* 88 — CTS1
- 50 OUT SIO_COM_DTR1* 89 — DTR1
- 50 IN SIO_COM_RI1* 90 — RI1
- 50 IN SIO_COM_DCD1* 91 — DCD1

SERIAL 2 /GPIO
- TP_SIO_COM_RI2* 92 — GP50/R12*
- TP_SIO_COM_DCD2* 94 — GP51/DCD2*
- TP_SIO_COM_RXD2* 95 — GP52/RXD2/IRRX
- TP_SIO_COM_TXD2* 96 — GP53/TXD2/IRTX
- TP_SIO_COM_DSR2* 97 — GP54/DSR2*
- TP_SIO_COM_RTS2* 98 — GP55/RTS2*
- TP_SIO_COM_CTS2* 100 — GP56/CTS2*
- TP_SIO_COM_DTR2* 100 — GP57/DTR2*

1

VCC

C1H3 .1UF 20% 50V Y5V 603

6963 IN V_3P3_STBY — 18 VTR

44 VREF

40 AVSS

VCC3=53,65,93
GND=7,31,60,76

IC

JOY
- GP10/J1B1 32 TP_SIO_GAME_J1B1
- GP11/J1B2 33 TP_SIO_GAME_J1B2
- GP12/J2B1 34 TP_SIO_GAME_J2B1
- GP13/J2B2 35 TP_SIO_GAME_J2B2
- GP14/J1X 36 TP_SIO_GAME_J1X
- GP15/J1Y 37 TP_GP15
- GP16/J2X 38 TP_GP16
- GP17/J2Y 39 TP_SIO_39
- GP25/MIDI_IN 46 TP_SIO_46
- GP26/MIDI_OUT 47 TP_SIO_GP26

1

6963 IN V_3P3_STBY

RP1H1 10K 5% .063W IC SM

GPIO
- P17/GP20 41 GP20_STRAP — IN 77
- P16/GP21 42 GP21_STRAP — IN 77
- P12/GP22 43 TP_SIO_GP22
- SYSOPT/GP24 45 SIO_GP24
- LED1/GP60 48 TP_SIO_GP60
- LED2/GP61 49 TP_SIO_GP61
- IOSMI*/GP27 50 IO_SMI* — OUT 24
- FDC_PP/DDRC/GP43 28 TP_SIO_GP43

1

KEY/MOUSE
- KDAT 56 SIO_KBDATA — BI 48
- KCLK 57 SIO_KBCLOCK — BI 48
- MDAT 58 SIO_MSDATA — BI 48
- MCLK 59 SIO_MSCLOCK — BI 48
- GP36/KBDRST 63 KBRST*
- GP37/A20M 64 A20GATE

PARALLEL
- INIT 66 SIO_LPT_INIT* — BI 49
- SLCTIN 67 SIO_LPT_SLCTIN — OUT 49
- PD0 68 0
- PD1 69 1
- PD2 70 2
- PD3 71 3
- PD4 72 4
- PD5 73 5
- PD6 74 6
- PD7 75 7 — SIO_LPT_PD<7..0> — BI 49
- SLCT 77 SIO_LPT_SLCT — IN 49
- PE 78 SIO_LPT_PE — IN 49
- BUSY 79 SIO_LPT_BUSY — IN 49
- ACK 80 SIO_LPT_ACK* — IN 49
- ERR 81 SIO_LPT_ERR* — IN 49
- ALF 82 SIO_LPT_ALF* — OUT 49
- STROBE 83 SIO_LPT_STROBE — OUT 49

IR
- IRRX2/GP34 61 SIO_IRRX2 — IN 55
- IRTX2/GP35 62 SIO_IRTX2 — OUT 55

FAN
- GP32/FAN2 54 TP_SIO_FAN2_PWM
- GP33/FAN1 55 FAN1_PWM
- FAN_TACH2/GP30 51 FRONT_FAN_TACH — IN 57
- FAN_TACH1/GP31 52 REAR_FAN_TACH — IN 57

CLOCK
- CLOCKI 19 CK_14M_SIO — IN 7 69
- CLKI32 6 SUSCLK — IN 24

BIOS DETECTS ADDRESS WITHOUT STUFFING

VCC3

R1H3 4.7K 5% EMPTY 603

R1H2 4.7K 5% CH 603

VCC3

RP1H2 10K 5% .063W IC SM

OUT 24
OUT 24

EMPTY IF HECETA6 IS STUFFED

R1H1 0 603 1A CH — FNT_REAR_FAN_PWM — OUT 5357

VCC3

6963 IN V_3P3_STBY

C1H4 .1UF 20% 50V Y5V 603

C1H2 .1UF 20% 50V Y5V 603

C2H2 .1UF 20% 50V Y5V 603

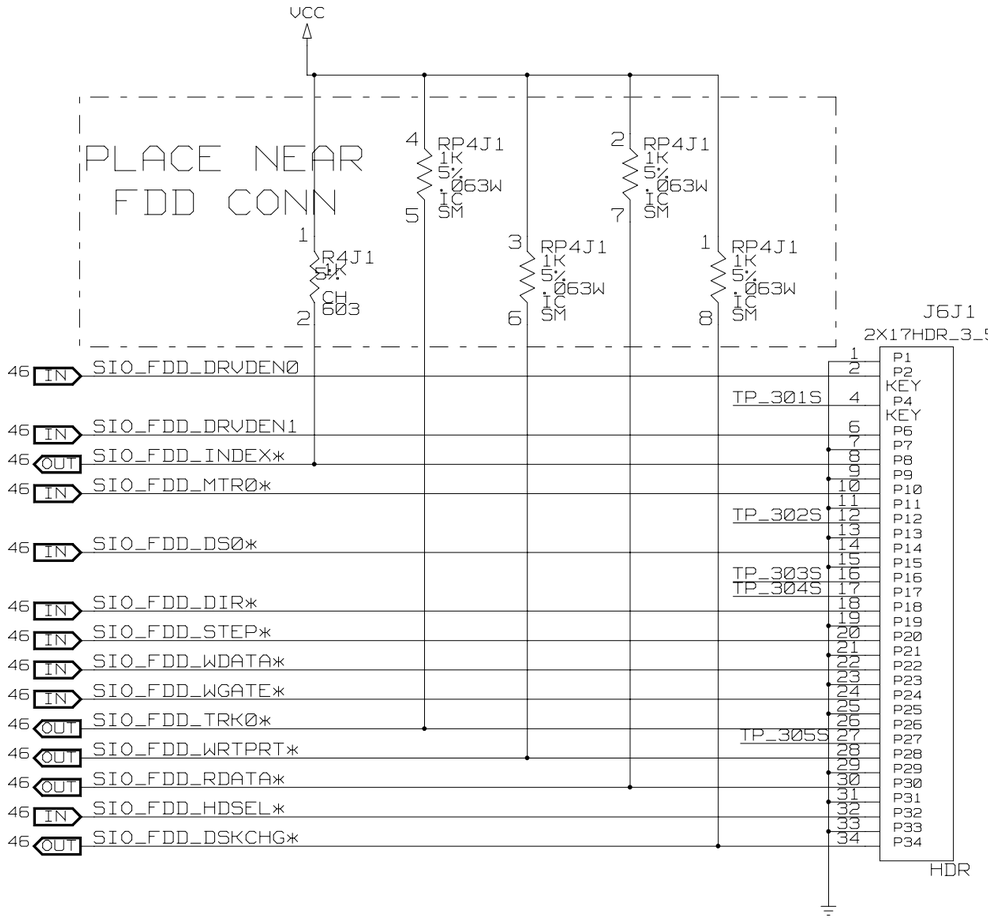
C1H1 .1UF 20% 50V Y5V 603

PLACE NEAR SMC DEVICE PINS 56,65,93,125

NOTE: #1

BIOS TO PROGRAM THESE GPIO'S AS OUTPUTS

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: SIO: LPC		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 46



SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: FLOPPY CONNECTOR

REV: 02.0

INTEL PLATFORM APPS ENG.
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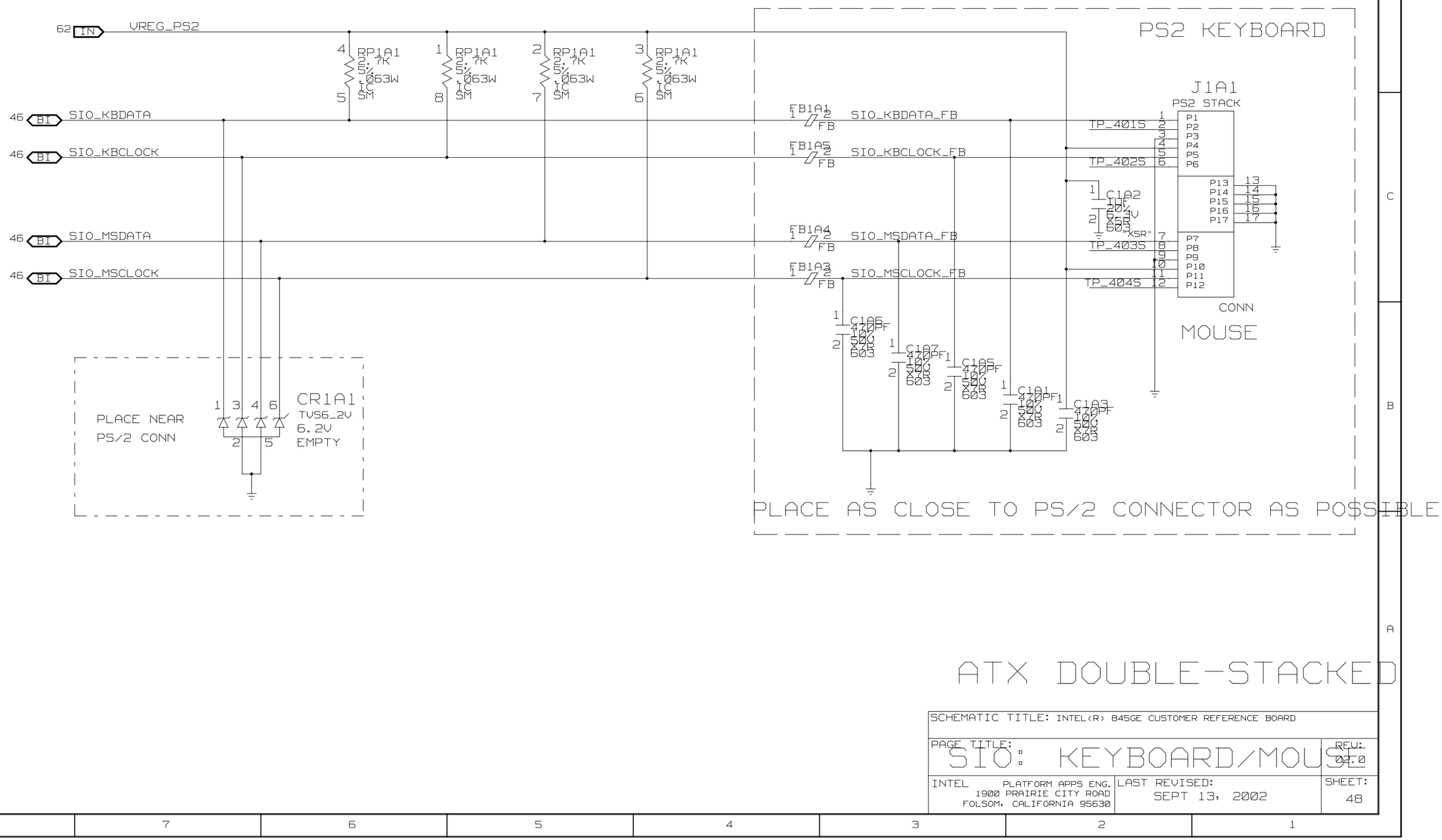
FOLSOM, CALIFORNIA 95630

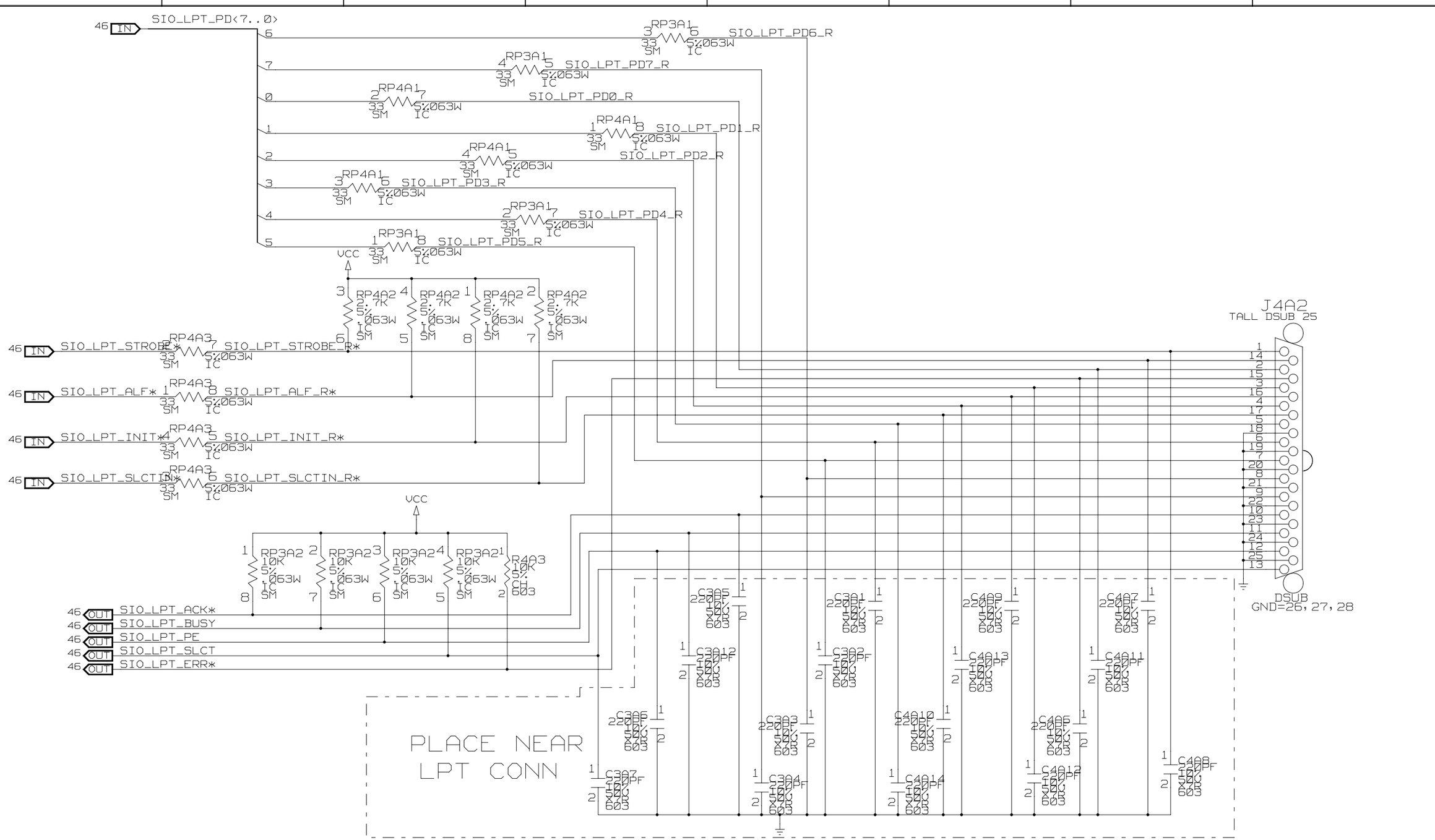
LAST REVISED: SEPT 13, 2002

SHEET: 47



ATX DOUBLE-STACKED

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: SIO: KEYBOARD/MOUSE		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 48



SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: SIO: PARALLEL CONNECTOR

REV: 02.0

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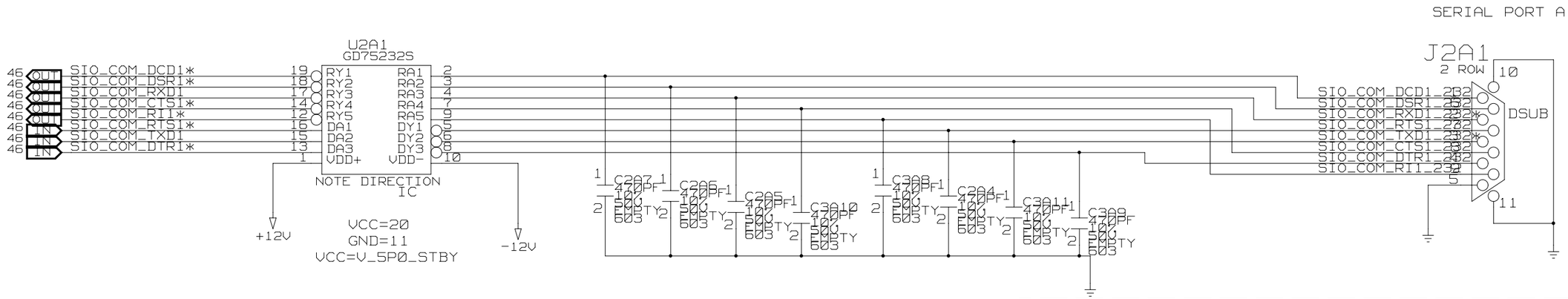
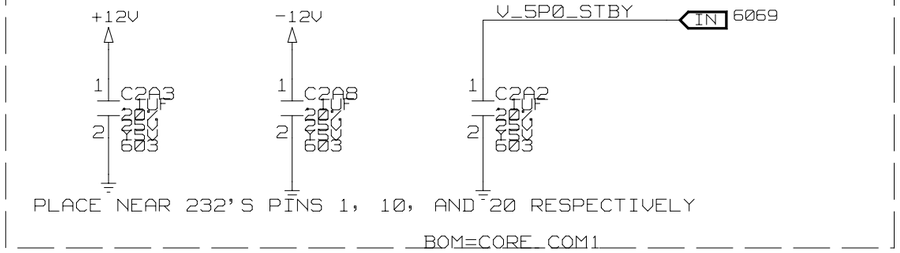
SERIAL PORT A





SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD			
PAGE TITLE: SERIAL CONNECTOR			REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: SEPT 13, 2002	SHEET: 50

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

CONFIGURE= SAFE MODE

754624 BI L_AD<3..0>

U9H1 FWH

6952 IN PWRGD_3V — RP9H1 8 1 4.7K 5% .063W SM IC — 7 WP

RP9H1 6 3 4.7K 5% .063W SM IC — 8 TBL

TP_FWH_29 — 29 IC

6925 IN P_PCIRST* — R8H9 2 1 FWH_PCIRST# 47 5% 603 CA — 2 RST

697 IN CK_P_33M_FWH — 31 CLK

24 IN L_FRAME* — 23 FWH4

FWH3 17 3
FWH2 15 2
FWH1 14 1
FWH0 13 0

DQ4/RFU 18 TP_FWH_13
DQ5/RFU 19 TP_FWH_19
DQ6/RFU 20 TP_FWH_20
DQ7/RFU 21 TP_FWH_21
RY/BY/RFU 22 TP_FWH_22
FGPI4 30 PN_FWH_GPI4
FGPI3 3 PN_FWH_GPI3
FGPI2 4 PN_FWH_GPI2
FGPI1 5 GPIO_DMA66_DETECT_SEC — IN 27
FGPI0 6 GPIO_DMA66_DETECT_PRI — IN 27
INIT 24 FWH_H_INIT* — IN 51

+12V — R9H2 1K 5% CH 603 — 2 — PN2201T — Q8H1 FET

VCC3 — FWH_VPP — 1 VPP

C9G9 1UF 20% Y5V 603

VCC3 — 27 VCCA/NC; 32 VCC; 25 VCC

28 GNDA/NC; 16 GND; 26 GND

ID3 9 TP_FWH_9
ID2 10 TP_FWH_10
ID1 11 TP_FWH_11
ID0 12 TP_FWH_12

IC

J8J3 JUMPER 2 1 EMPTY

ALWAYS EMPTY

RP9H1 4 5 4.7K 5% .063W IC SM

R8G11 1K 5% CH 603 — VCC3

J8G1 1X3HDR 1 2 3 HDR

RECOVERY_CONFIGURE_PULLUP
24 IN AUD_LINK_SDO_R

VCC3

VCC3 — RP9H1 7 2 4.7K 5% .063W IC SM

R8H14 1K 5% CH 603

R9H5 10K 5% EMPTY 603

VCC3

R9H7 10K 5% CH 603

FIRMWARE HUB DECOUPLING

VCC3 — C8H6 1UF 20% Y5V 603 EMPTY; C8H2 1UF 20% Y5V 603; C8H3 1UF 20% Y5V 603

VOLTAGE MODIFIER; ICH(VCCP) ISOLATE FROM FWH(VCC3)

STUFF FOR VCCP > 1.5-V

+12V — R8H13 4.7K 5% CH 603

R7G9 0 1A 603 EMPTY; R8H16 0 1A 603 EMPTY

FWH_H_INIT* — OUT 51

H_FLUSH_FEEDBACK_R*

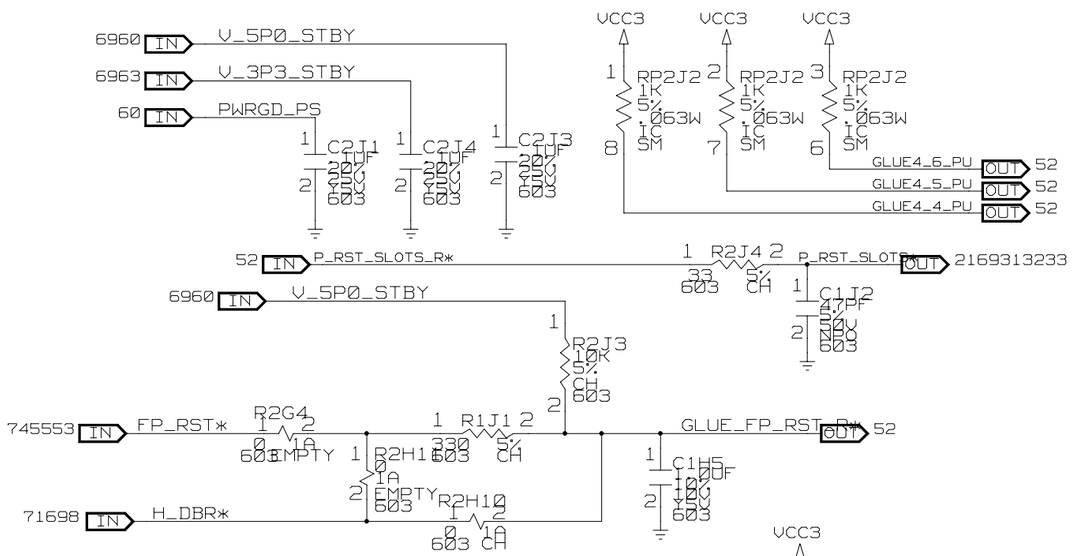
Q8H4 MBT3904DUAL

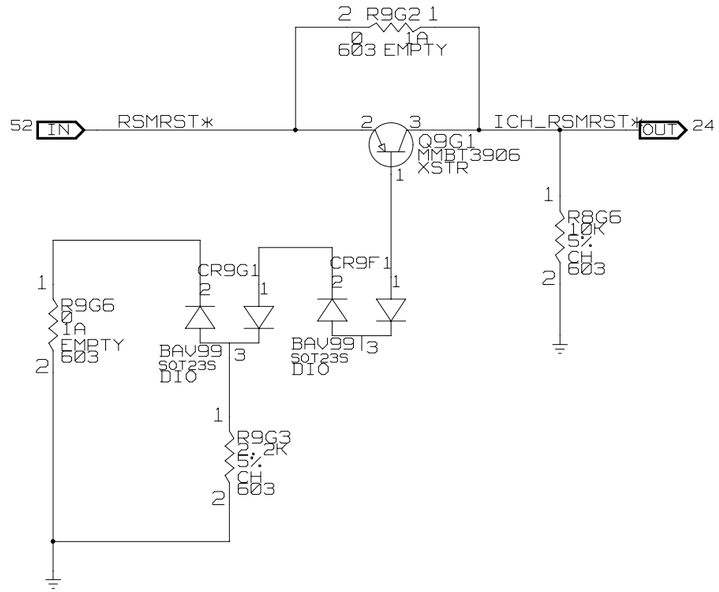
6924 IN H_INIT* — R7G11 4.7K 5% 603 CA — H_INIT_R*

XSTR

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: FIRMWARE HUB		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 51

GLUECHIP4

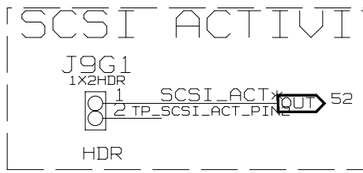


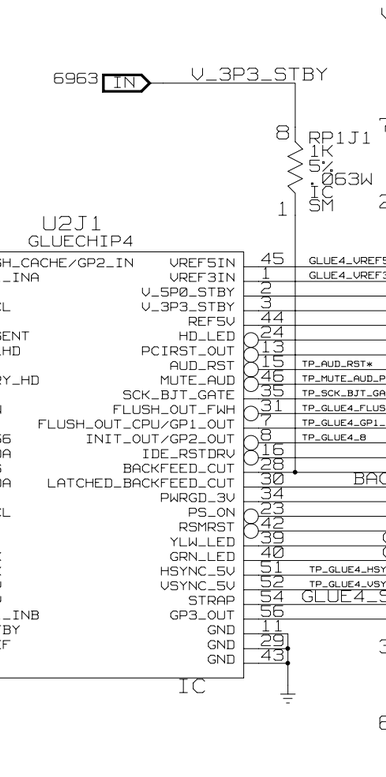


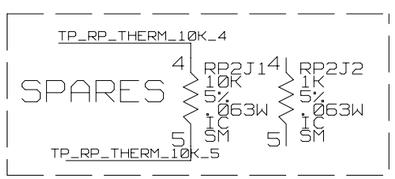
GLUE4 INPUTS

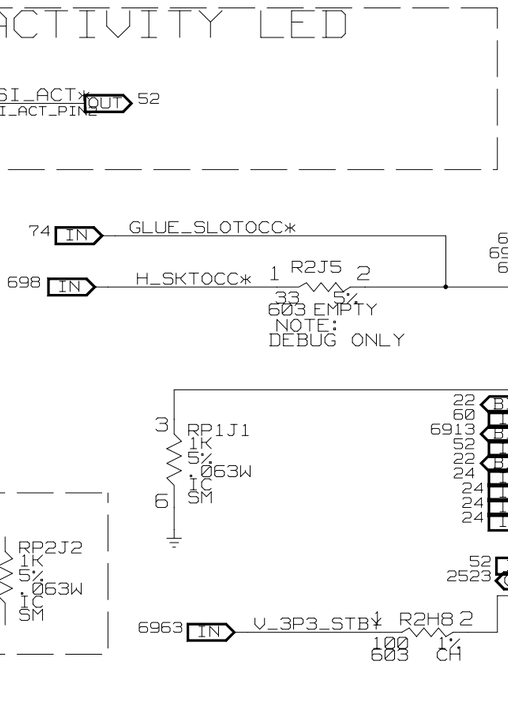
PIN	FUNCTION	TYPE
1	VREF3IN	3I
2	5VSB	PI
3	3VSB	PI
4	GP2_IN	3IU
5	GP1_INB	VCCP REF
6	GP1_INA	VCCP REF
9	CLK_IN	3I
10	SEL_33_66	3IU
12	PCIRST*	3I
14	AUD_EN	3IU
17	3V_DDCSCL	3IOD
18	5V_DDCSCL	5IOD
19	3V_DDCSDA	3IOD
20	5V_DDCSDA	5IOD
21	CPU_PRESENT*	3IU
22	SLP_S3*	3I
25	PRIMARY_HD*	5IU
26	SCSI*	5IU
27	SECONDARY_HD*	5IU
32	PWRGD_PS	5IU
33	FPRST*	5IU
36	SLP_S5*	3I
37	GRN_BLNK	3IU
38	YLW_BLNK	3IU
41	TEST_EN	5ID
45	VREF5IN	5I
46	MUTE_AUD*	3IU
49	HSYNCH_3V	3I
50	VSYNCH_3V	3I
53	VCCP_VREF	AI
54	STRAP	3IU
55	GP3_IN	5I

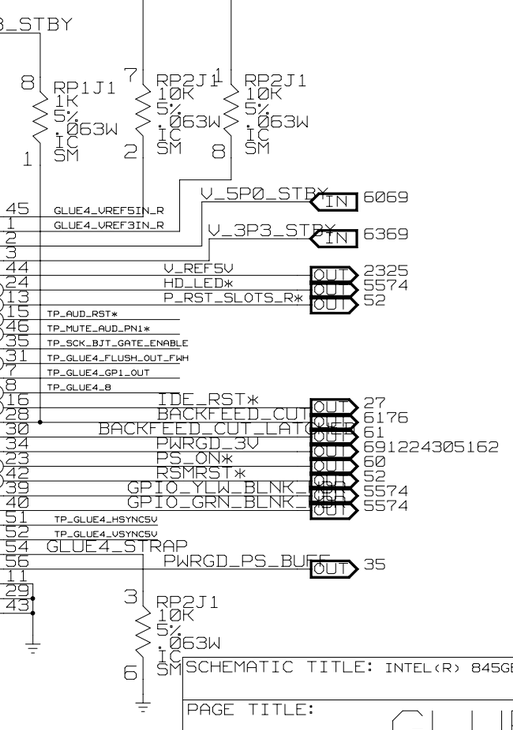
SCSI ACTIVITY LED











SCHEMATIC TITLE: INTEL‹R› 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: GLUE4

REV: 02.0

INTEL PLATFORM APPS ENG.
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CAD NOTE:
SOUTHEAST THERMAL ZONE SENSOR
PLACE BELOW DIMMS

CAD NOTE:
10MIL TRACE ON SE_ZONE_TDN AND TDP

Q1C2
MMBT3904
EMPTY

C1C2
100PF
10V
5%
X7R
EMPTY
603

57 OUT CPU_FAN_PWM1
763533323124 BI SMB_DATA_MAIN
763533323124 BI SMB_CLK_MAIN
8_69 OUT H_TEMP_RET
698 IN H_TEMP_SRC
SE_ZONE_TDP
SE_ZONE_TDN
7468 IN H_VID<4..0>

R2F6
0
1A
603
EMPTY

PRELIMINARY
U1F1
HECETA6

24	PWM1/NTESTOUT	VCCP_IN	23
		2.5V	22
1	SDA	5V	20
2	SCL	3.3SBY	4
		12V	21
18	REMOTE1+		
17	REMOTE1-/NTESTIN	PWM2	10
16	REMOTE2+	PWM3	13
15	REMOTE2-		
		TACH1	11
4	VID4	TACH2	12
3	VID3	TACH3	9
2	VID2	TACH4	14
1	VID1		
0	VID0	GND	3

EMPTY

VCC
+12V

R1F7
0
1A
EMPTY
603

VCCP IN 6769
V_1P5_CORE IN 66
V_3P3_STBY IN 6369
TP_HECETA6_PWM2_P10
FNT_REAR_FAN_PWM3 OUT 4657
CPU_FAN_TACH IN 57
H6_TAC4_PD
FRONT_FAN_TACH IN 57
REAR_FAN_TACH IN 57

R1F2
10K
5%
EMPTY
603

ALL STUFFED IF HECETA6
ALL EMPTY IF HECETA4

6963 IN V_3P3_STBY

R1F3
1K
5%
EMPTY
603

H4_RSTIN_H6_PWM1
H4_VCC3_H6_12V

VCC3

R1F9
0
1A
CH
603

52247455 OUT FP_RST*

R2F4
0
1A
603
CA

U1F2
HECETA4

16	A0/NTEST_OUT	+VCCP_IN	15
		+2.5VIN	14
1	SDA	+5VIN	12
2	SCL	VDD/3.3VIN	4
		+3.3V	13
10	RMT_DIODE+		
9	RMT_DIODE-		
4	+12V/VID4		
3	VID3		
2	VID2	GNDD	3
1	VID1		
0	VID0		

IC

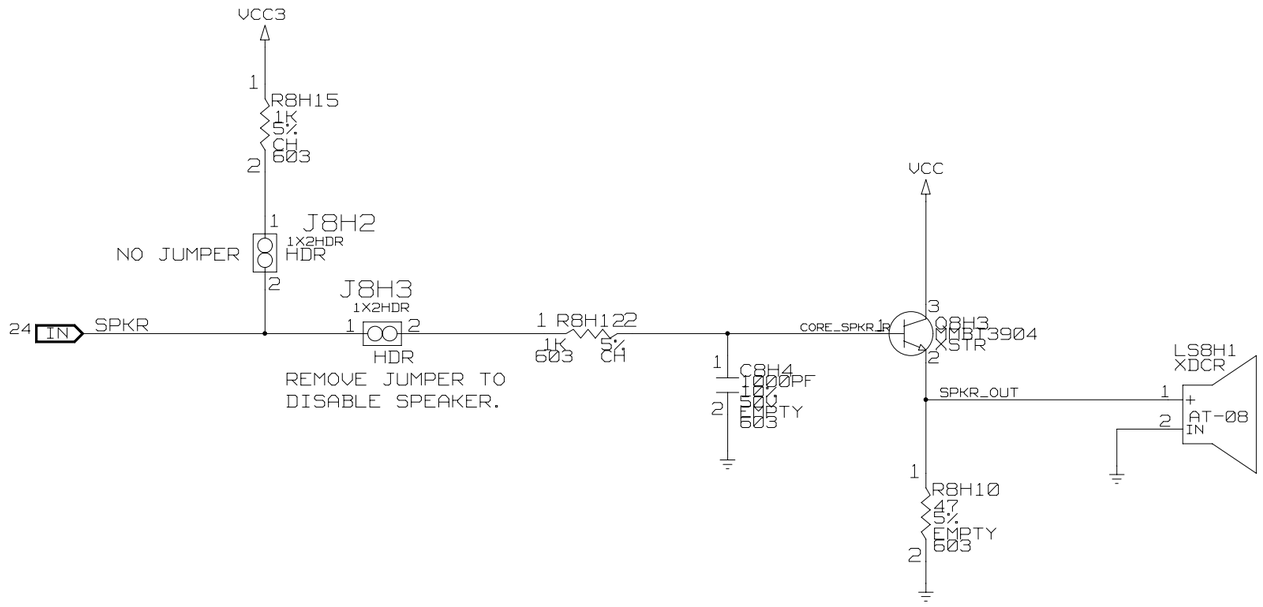
C1F1
1UF
10V
X7R
603

C1F2
1UF
10V
X7R
603

ALL STUFFED IF HECETA4
ALL EMPTY IF HECETA6

HARDWARE MANAGEMENT: HECETA

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: HW MANAGEMENT: HECETA		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 53



SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD			
PAGE TITLE: SPEAKER			REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: SEPT 13, 2002	SHEET: 54

J9G2
2X3HDR_2
TP_IR_FP_11
VCC
5546 OUT SIO_IRTX2
SIO_IRRX2 IN 55
HDR

CAD NOTE: OVERLAY SO PINS
1-9 MATCH UP (DUAL FP).
J9G2 DOES NOT NEED TO BE DUAL FP'D

J9H2
2X5HDR_10
VCC
R9H8 0 1A 603 EMPTY
FP_PWR_5V
STUFF R9H8 ONLY WHEN
J9H3 IS STUFFED
HDR

V_5P0_STBY IN 6069
R9H1 220 5% CH 603
R9H3 220 5% CH 603

R9H4 10K 5% 603 CH
VCC3
UNSTUFF FOR R9H12
VCC 330 5% 603 CH

52 IN HD_LED*
52247453 OUT FP_RST*
5546 OUT SIO_IRRX2
5546 IN SIO_IRTX2

GPIO_GRN_BLNK HDR IN 52
GPIO_YLW_BLNK HDR IN 52

J9H3
2X3HDR_4
EMPTY
109717-021
VCC

VCC
CP9H2 470PF 20% 50V EMPTY SM
CP9H2 470PF 20% 50V EMPTY SM
CP9H1 470PF 20% 50V EMPTY SM
602431-0052 CP9H2 470PF 20% 50V X7R 603
CP9H1 470PF 20% 50V EMPTY SM
"X7R"
CP9H1 470PF 20% 50V EMPTY SM
CP9H1 470PF 20% 50V EMPTY SM
CP9H2 470PF 20% 50V EMPTY SM
CP9H2 470PF 20% 50V EMPTY SM

BOM=CORE_STDFNTPNL_E

J9H1
1X3HDR2
HDR
GPIO_GRN_BLNK_HDR IN 52
C9G5 470PF 10% 50V X7R 603
GPIO_YLW_BLNK_HDR IN 52
C9H1 470PF 10% 50V X7R 603

DECOUPLING
VCC3
C9G8 22UF 20% 10V TANT 603
BOM = VREG_DCPL_BULK

6963 IN V_3P3_STBY R9H6 22K 5% 603 CH 2
SW_ON* OUT 24
74 IN SWITCH_ON*
R9H10 33 5% 603 CH 2
C9H4 10UF 10% 10V TANT 603

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: STD FRONT PANEL HDR		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 55

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SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD			
PAGE TITLE: BLANK			REV: 02.0
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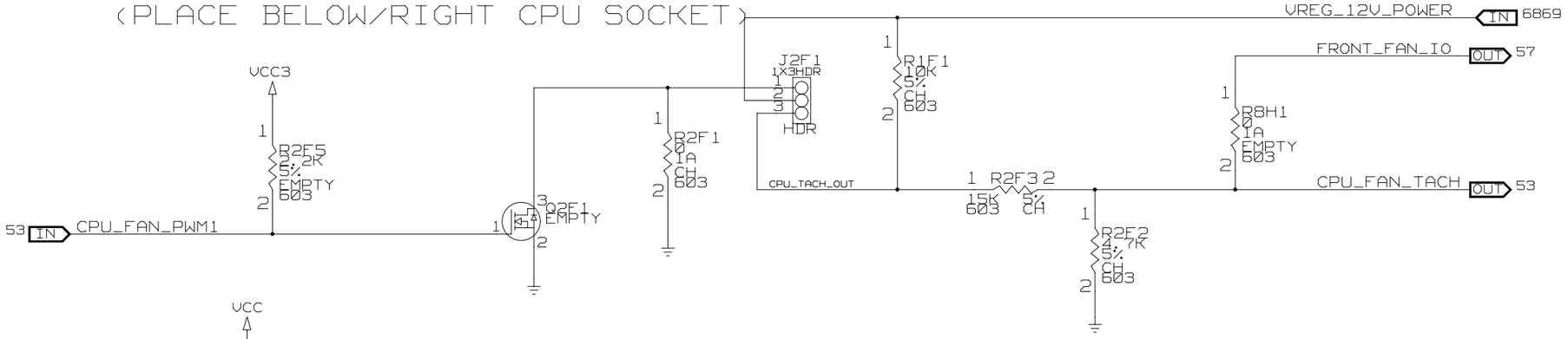
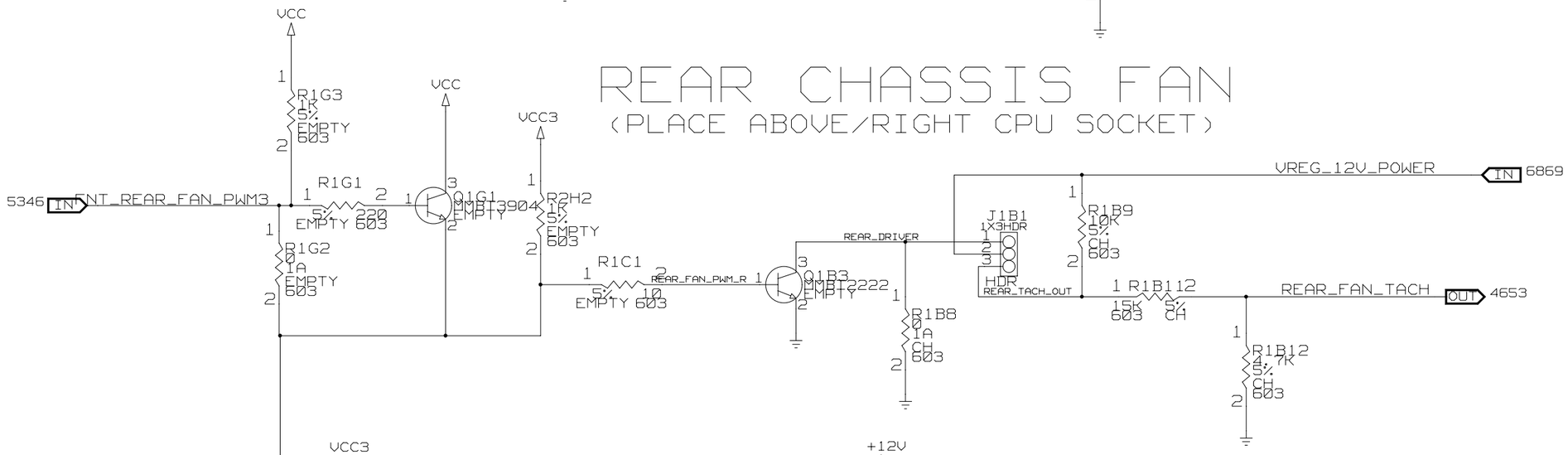
CPU ALWAYS-ON FAN

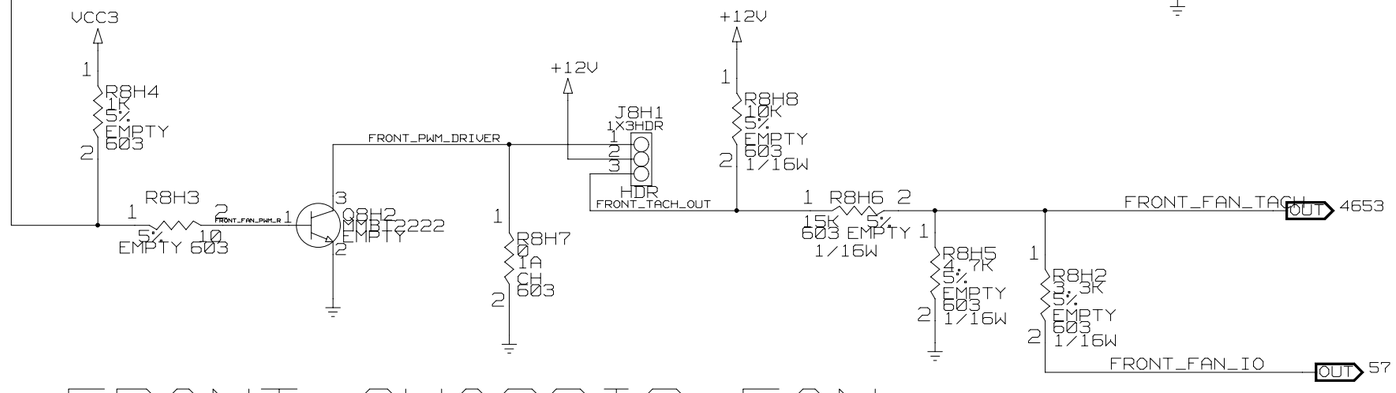
(PLACE BELOW/RIGHT CPU SOCKET)



REAR CHASSIS FAN

(PLACE ABOVE/RIGHT CPU SOCKET)

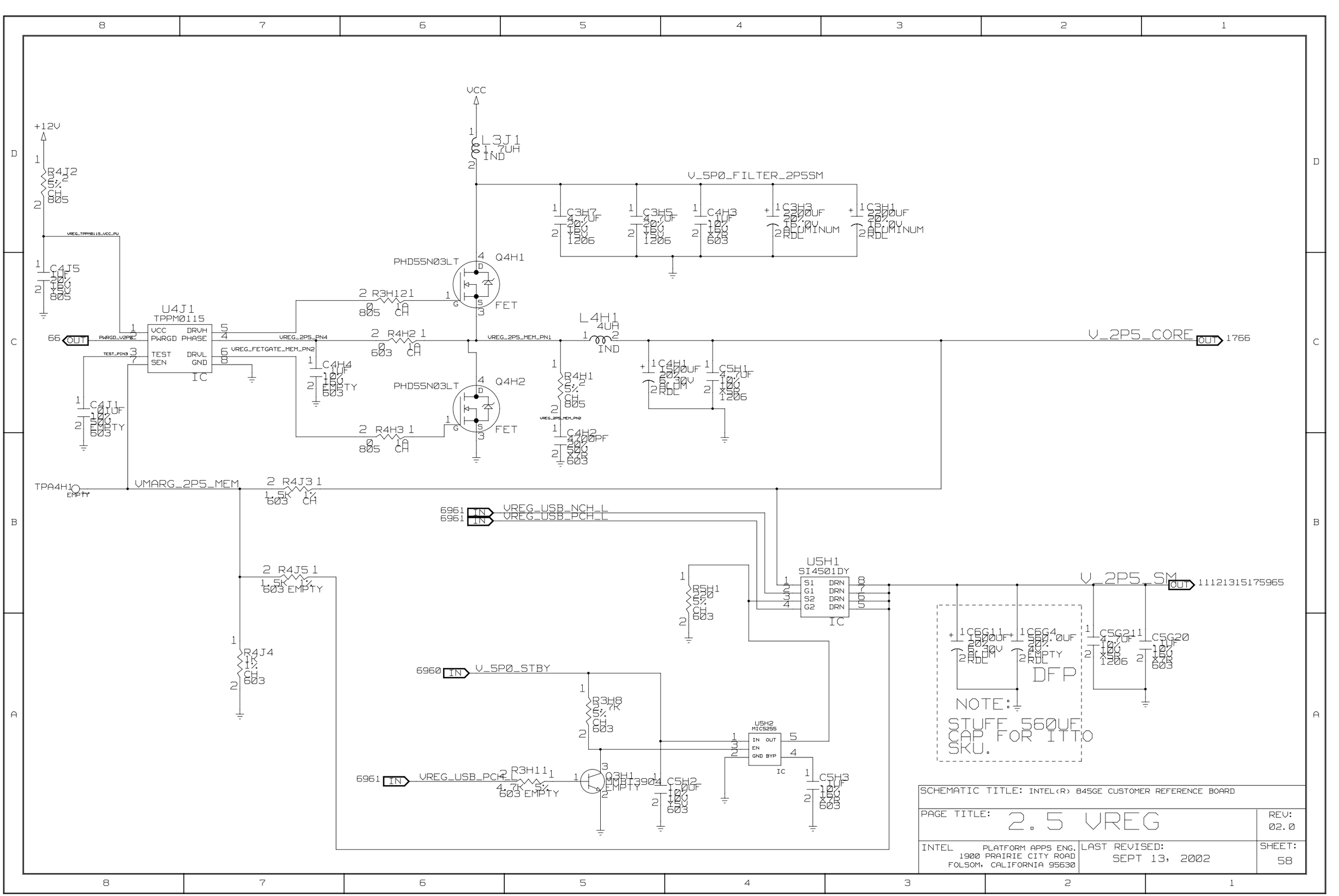




FRONT CHASSIS FAN

(PLACE LOWER LEFT CORNER OF PLATFORM)

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: FAN HEADERS		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 57


+12V
R4J2 5% 1/8W CH 805
VREG_TPPM0115_VCC_PU
C4J5 10UF 20% 16V TANTALUM 805 VCC
U4J1
TPPM0115
VCC DRVH
PWRGD PHASE
TEST DRVL
SEN GND
IC
66 OUT PWRGD_V2P5
TEST_PIN3
C4J1 10UF 20% 16V TANTALUM 603
VREG_2P5_PN4
VREG_FETGATE_MEM_PN2
C4H4 1UF 10% 16V CERAMIC X7R 603
R3H12 0 1A 805 CH
R4H2 0 1A 603 CH
VCC
L3J1 1.7UH IND
V_5P0_FILTER_2P5SM
C3H7 4.7UF 20% 16V TANTALUM 1206
C3H5 4.7UF 20% 16V TANTALUM 1206
C4H3 1UF 10% 16V CERAMIC X5R 603
C3H3 2200UF 20% 10V ALUMINUM RDL
C3H1 2200UF 20% 10V ALUMINUM RDL
PHD55N03LT
Q4H1 FET
R3H11 0 1A 805 CH
L4H1 4UH IND
VREG_2P5_MEM_PN1
V_2P5_CORE OUT 1766
R4H1 5% 1/8W CH 805
VREG_2P5_MEM_PN2
C4H2 4700PF 10% 50V CERAMIC X7R 603
C4H1 1500UF 20% 6.3V POLYMER RDL
C5H1 4.7UF 10% 10V CERAMIC X5R 1206
PHD55N03LT
Q4H2 FET
R4H3 0 1A 805 CH
TPA4H1 EMPTY
VMARG_2P5_MEM
R4J3 1.5K 1% 603 CH
6961 IN VREG_USB_NCH_L
6961 IN VREG_USB_PCH_L
R4J5 1.5K 1% 603 EMPTY
R4J4 1K 1% 603 CH
U5H1
SI4501DY
S1 DRN
G1 DRN
S2 DRN
G2 DRN
IC
R5H1 20 5% 603
V_2P5_SM OUT 11121315175965
C5G11 1500UF 20% 6.3V POLYMER RDL
C5G4 330.0UF 20% 2.5V TANTALUM EMPTY RDL
C5G21 4.7UF 10% 10V CERAMIC X5R 1206
C5G20 1UF 10% 10V CERAMIC X7R 603
DFP
NOTE:
STUFF 560UF CAP FOR ITT0 SKU.
6960 IN V_5P0_STBY
R3H8 4.7K 5% 603
U5H2
MIC5255
IN OUT
EN
GND BYP
IC
6961 IN VREG_USB_PCH_L
R3H11 4.7K 5% 603 EMPTY
Q3H1 MMBT3904 EMPTY
C5H2 100UF 20% 16V TANTALUM 603
C5H3 1UF 10% 10V CERAMIC X7R 603
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD
PAGE TITLE: 2.5 VREG
REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
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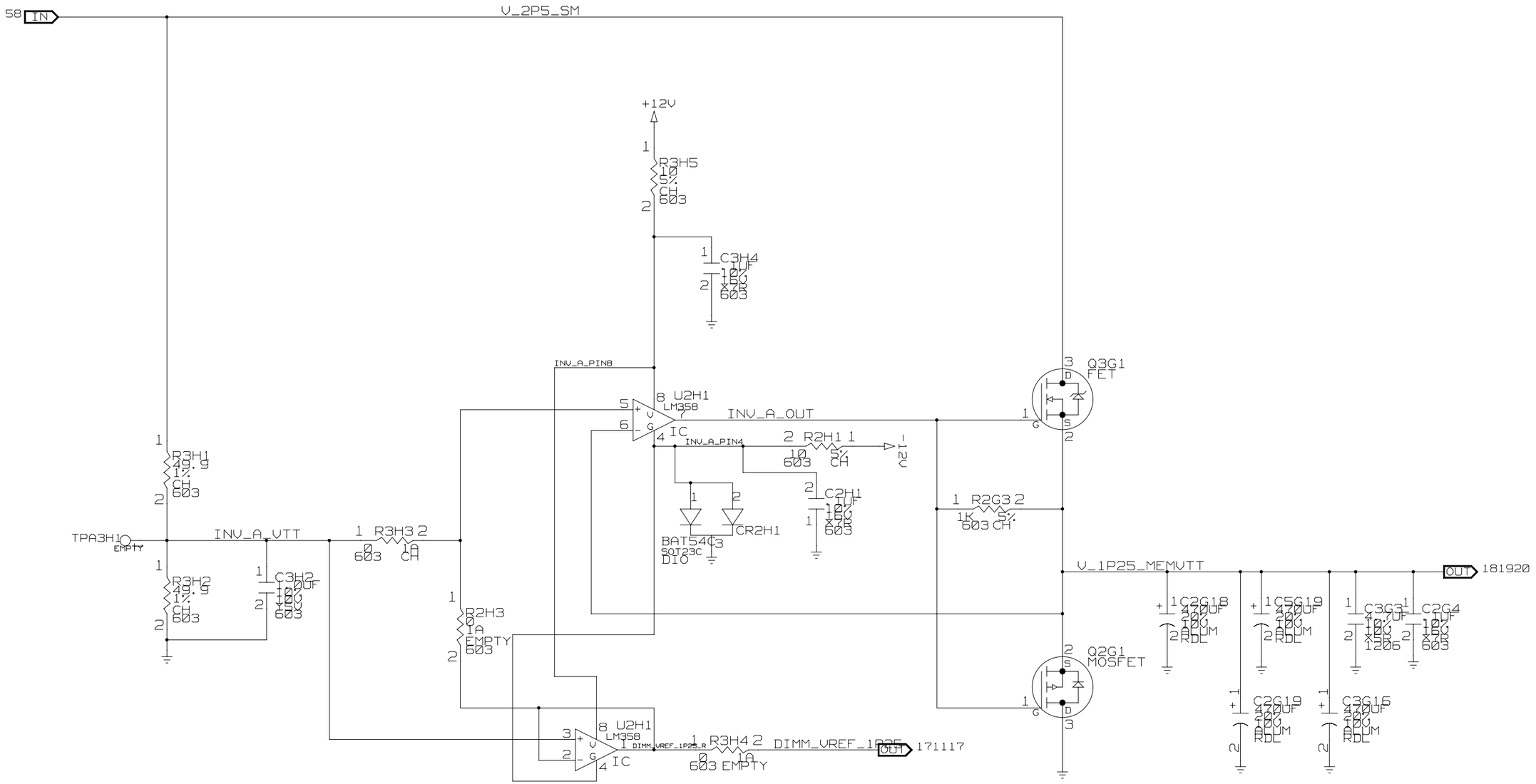
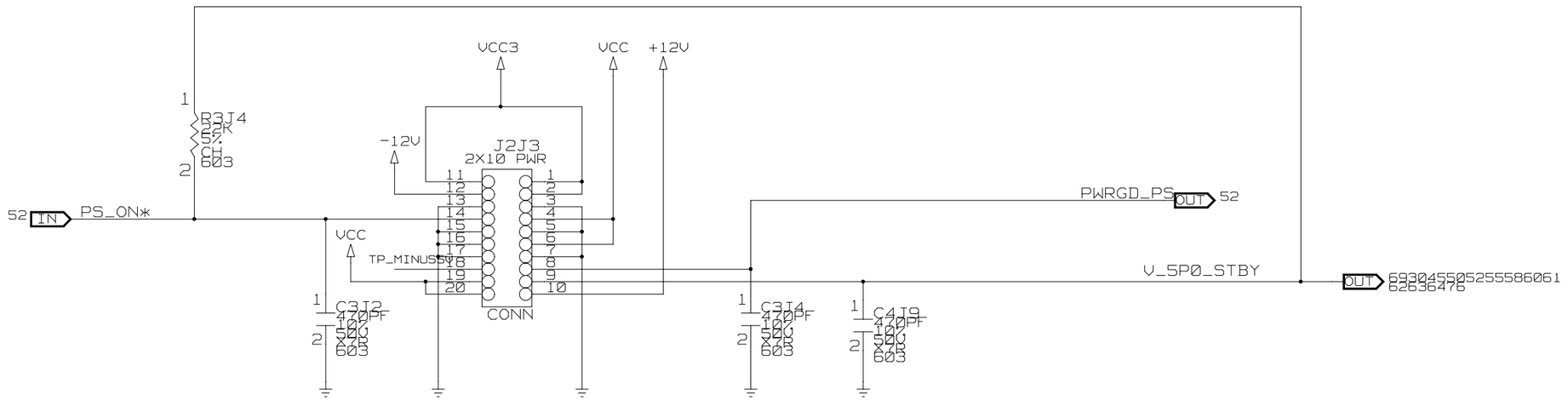
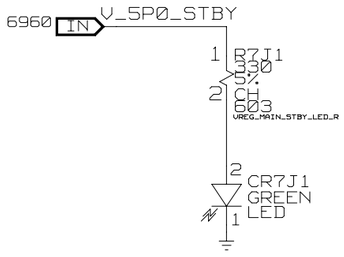
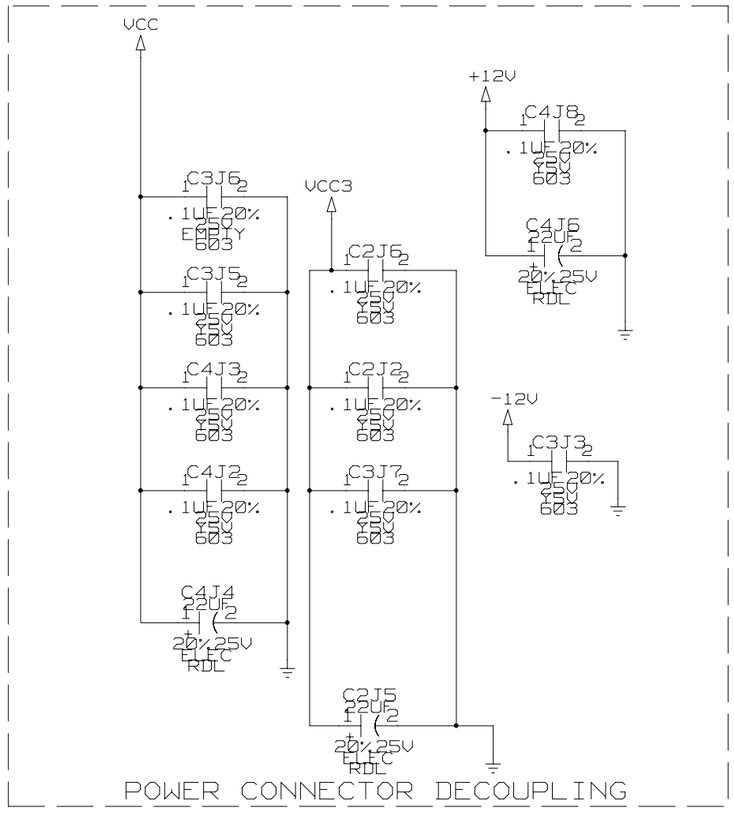
1.25V DDR



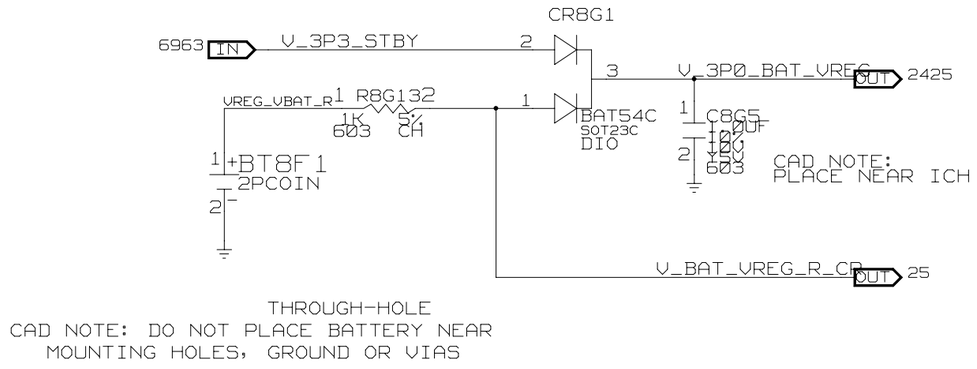
SCHEMATIC TITLE: INTEL‹R› 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: 1P25 VREG		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 59

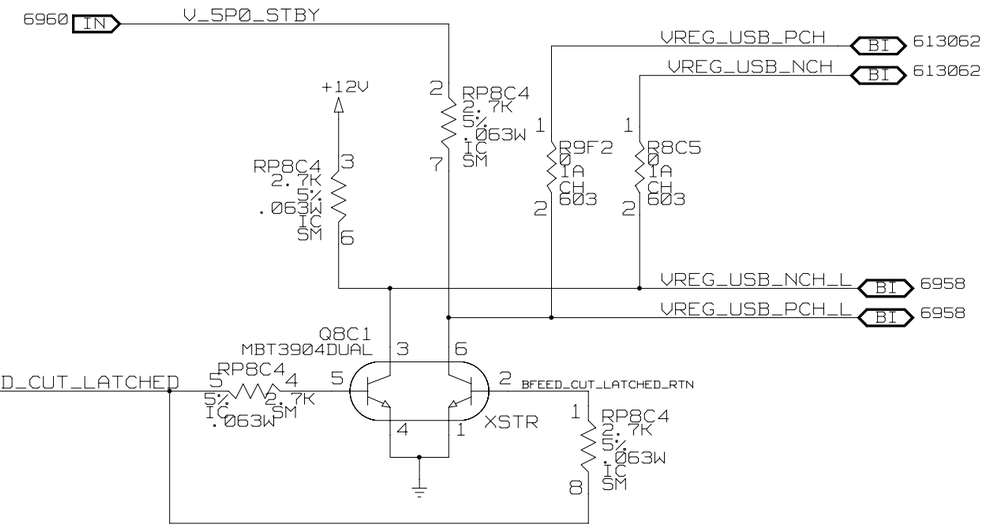


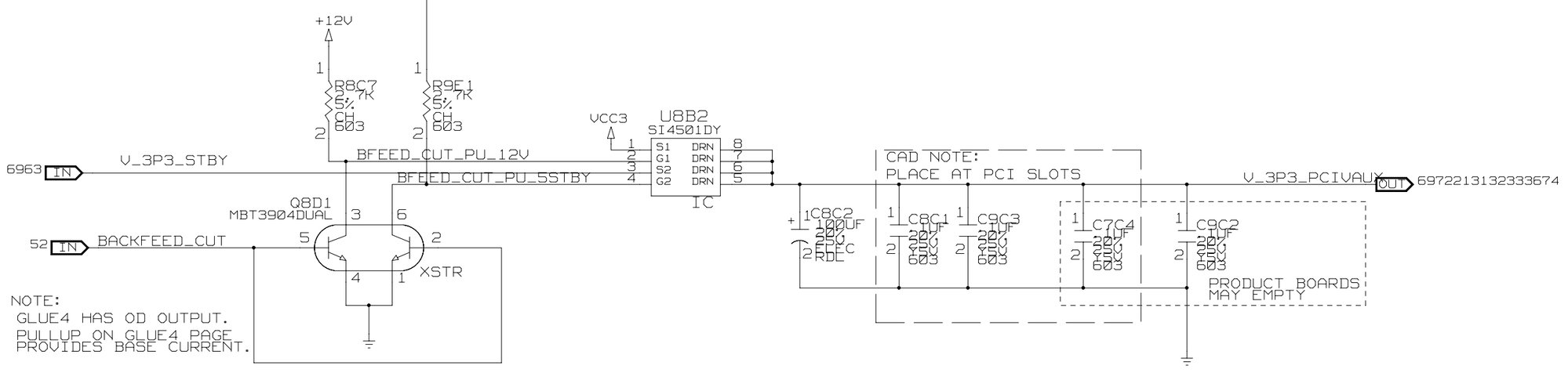




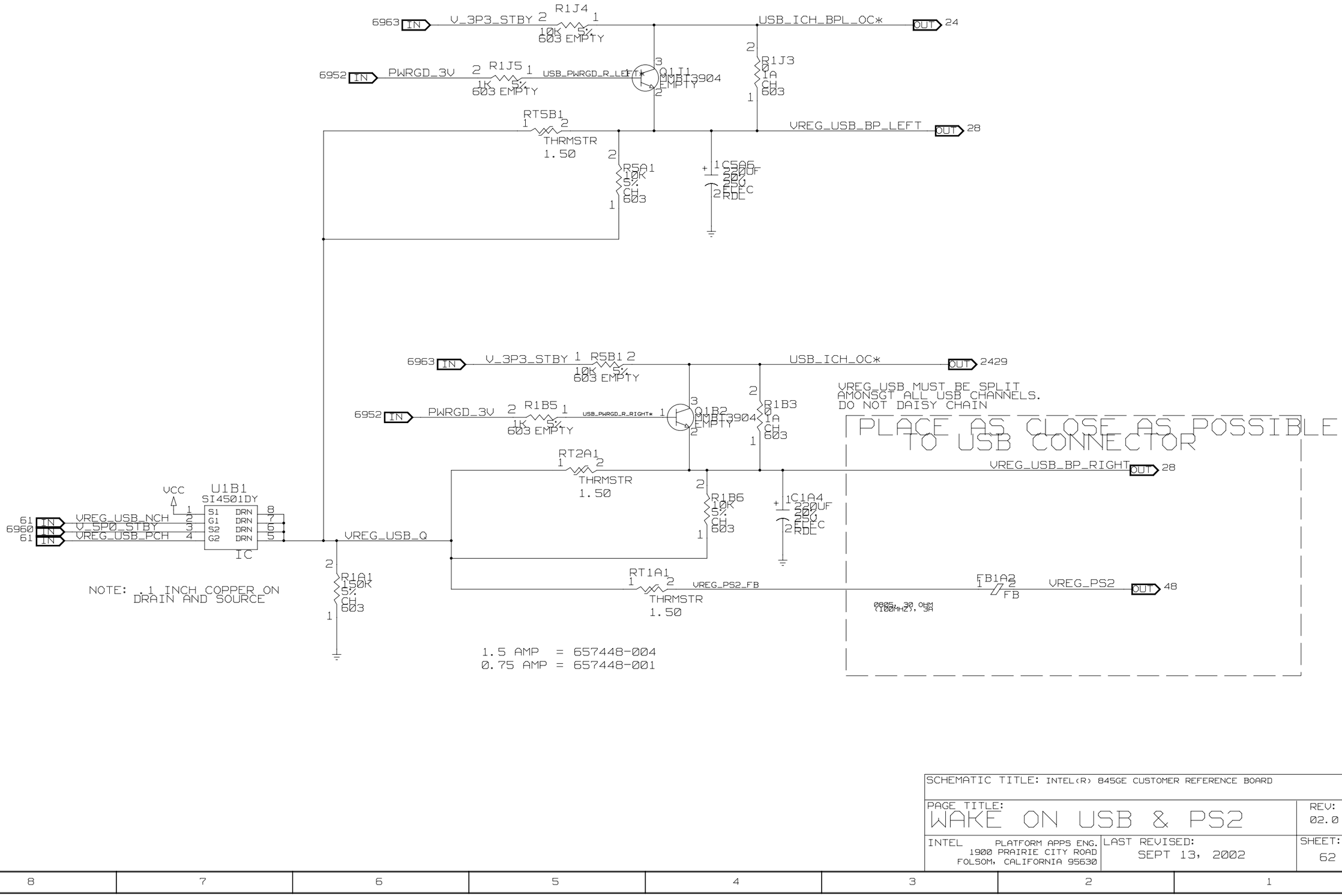
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: STANDARD POWER CONNECTOR		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 60







SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI VAUX		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 61



SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD

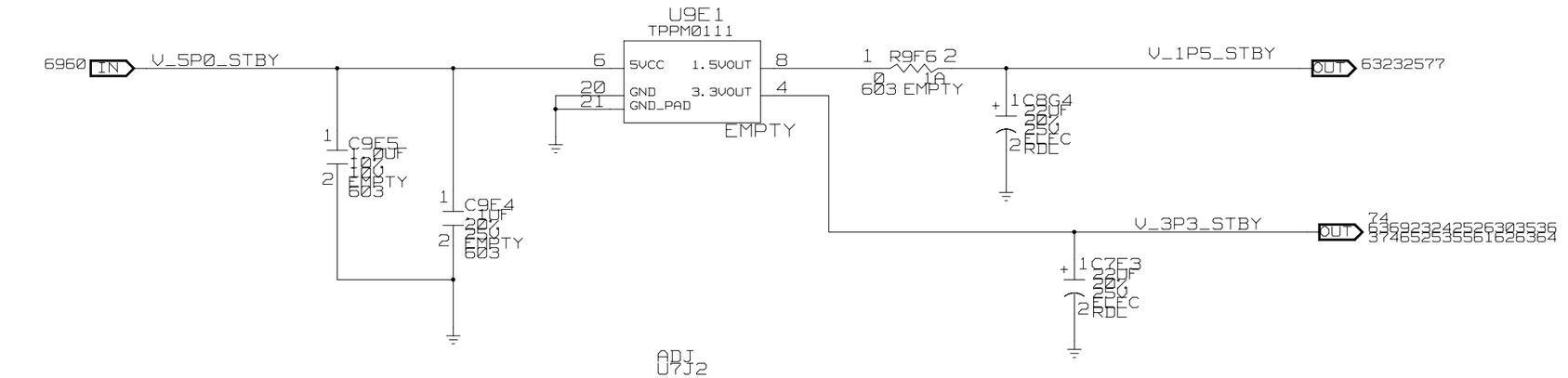
PAGE TITLE: WAKE ON USB & PS2

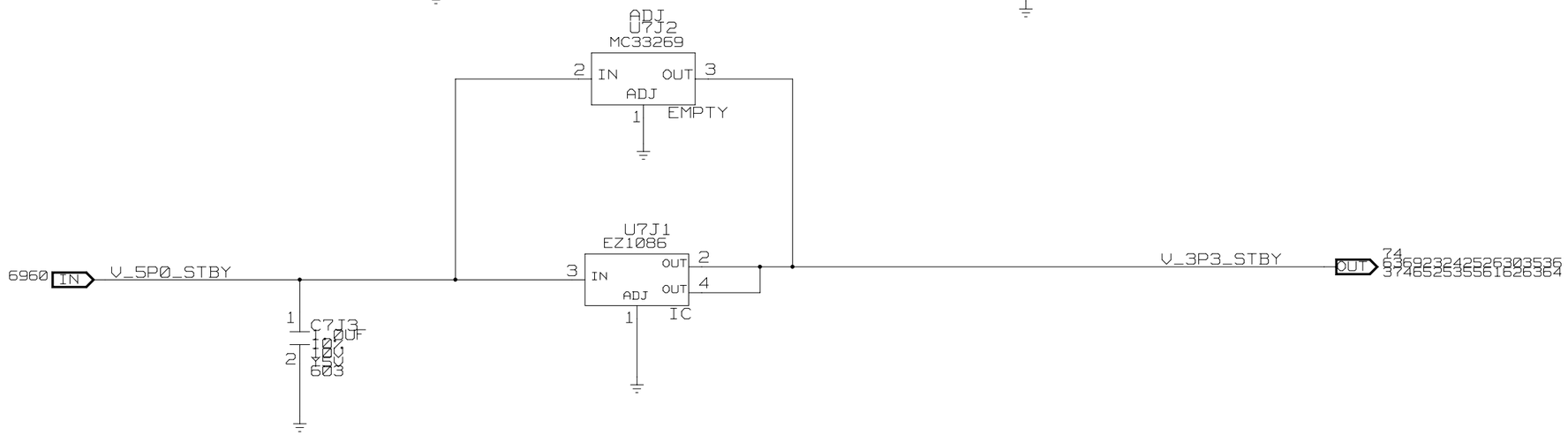
REV: 02.0

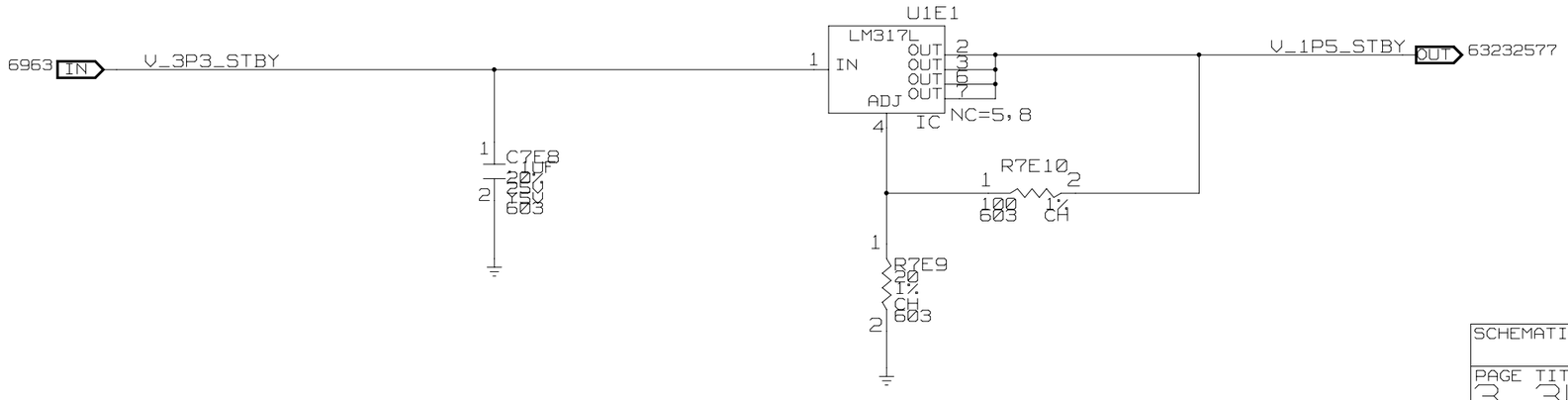
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: SEPT 13, 2002

SHEET: 62







SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD	
PAGE TITLE: 3.3V/1.5V STANDBY	REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002
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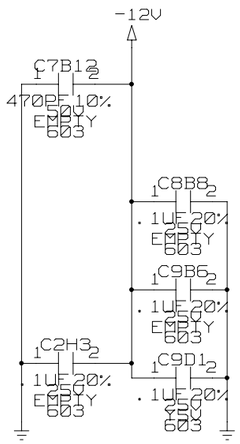
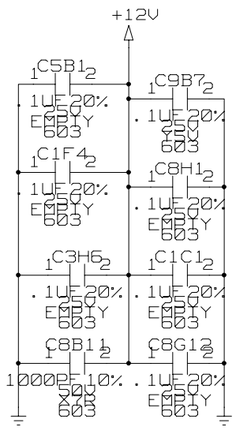
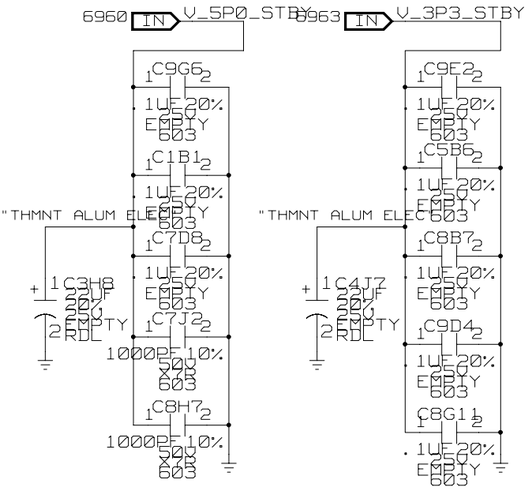
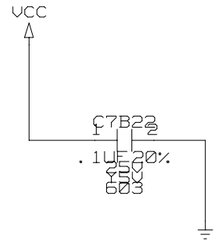
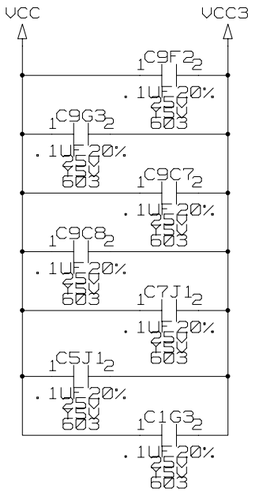
VREG_DCPL_BULK

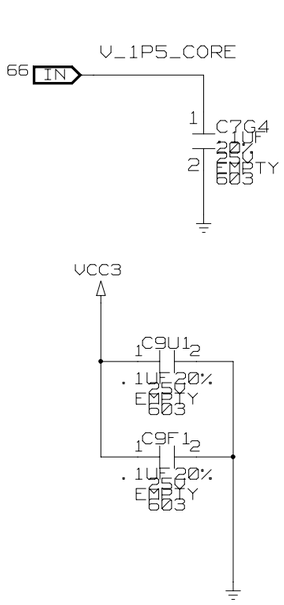


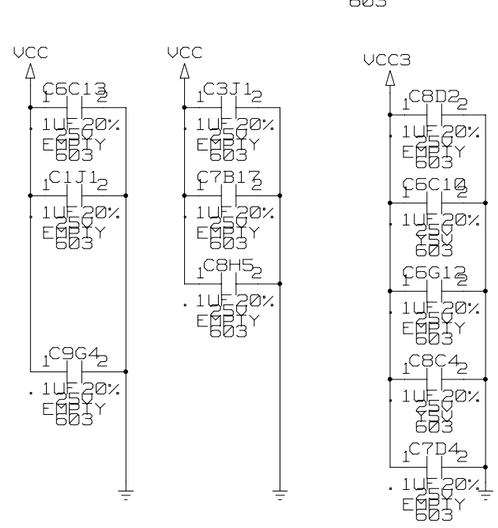


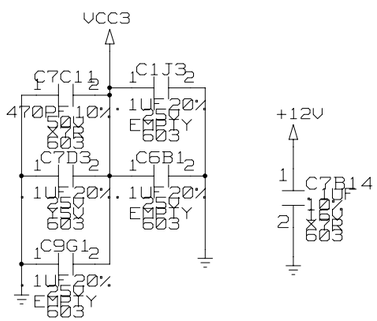


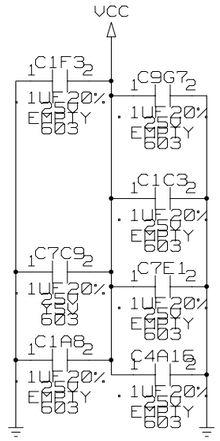


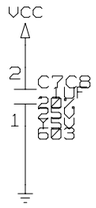




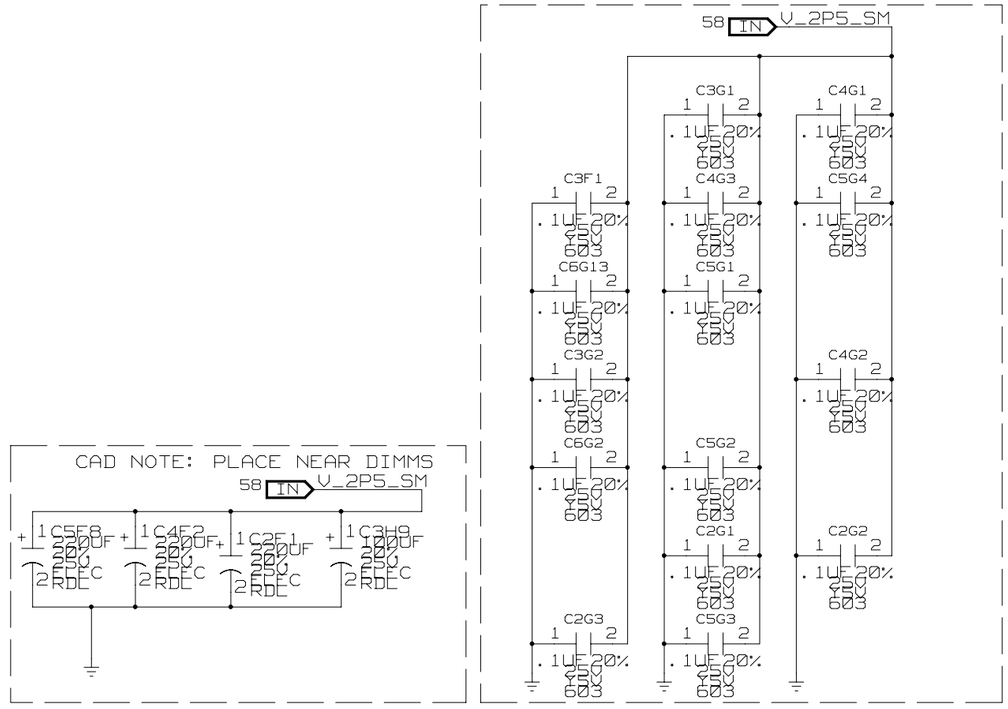








SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: VREG BULK DECOUPLING		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 64



SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD

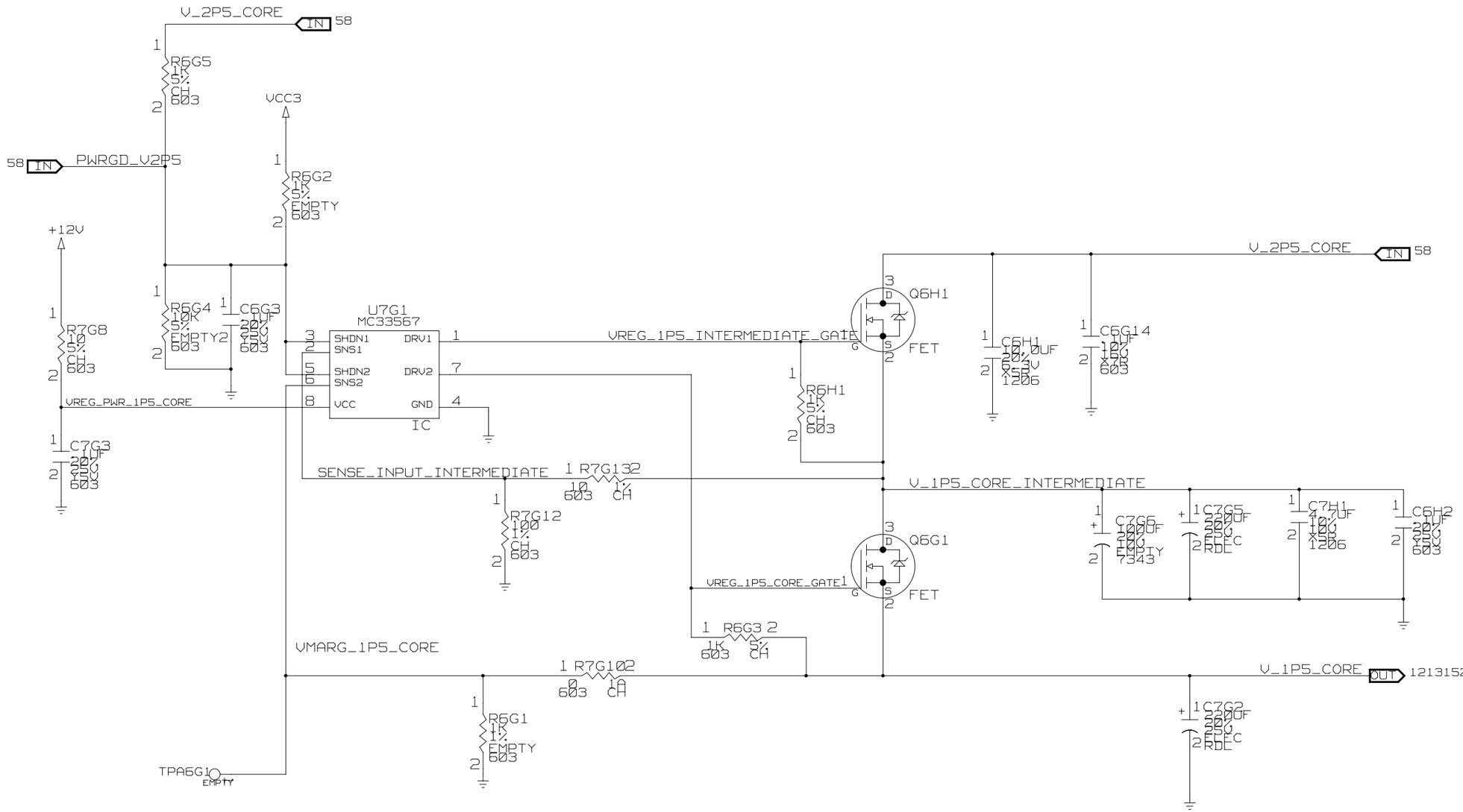
PAGE TITLE: DDR 2P5_SM DECOUPLING

REV: 02.0

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: SEPT 13, 2002

SHEET: 65



SCHEMATIC TITLE: INTEL‹R› 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: 1P5 VREG		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 66

COMPOMENTS ARE DFM 29

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: CPU MAIN REGULATOR (VCCP)

REV: 02.0

INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630

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ROOM = DCL_CORE_CPU_VREG

6967 IN VCCP

C3C2 C2C1 C3C4 C3C8 C2C4 C2C2 C3C3 C2C5 C2C7 C3C9 C2C8 C2C3 C2C6 C2C9
10.0UF 10V X5R 1206

NOTE: PLACE THESE NORTH OF THE CPU SOCKET

C2D2 C2D1 C2D3 C2D8 C2D9 C2D4 C2D10 C2D7 C2D13 C2D11 C2D6 C2D14 C2D15 C2D12 C2D18 C2D5 C2D17 C2D16
10.0UF 10V X5R 805

NOTE: PLACE THESE IN THE CAVITY OF THE CPU SOCKET

C3E2 C3E1 C2E4 C2E2 C2E1 C2E3
10.0UF 10V X5R 805

NOTE: PLACE THESE SOUTH OF THE CPU SOCKET

C2B11 C2B13 C2B10 C3B5 C4B5 C4B4 C4C1 C4B6 C2B12
330UF 20% 2V RADIAL

C4C3 C3B6
560.0UF 20% 2V EMPTY RDL

C3B4 C4C4
560.0UF 20% 2V EMPTY RDL

C5C2 C5C3
560.0UF 20% 2V EMPTY RDL

DFP DFP DFP

L5C1
1.7UH
IND

VREG_12V_FILTERED OUT 67

C5B7 C5B10 C2B1
2200UF 20% 10V ALUMINUM RDL

VREG_12V_POWER OUT 69576774

J5C1
2X2HDR
CONN

C5C4 C5C5
470PF 10% 50V X7R 603
"Y5V" "Y5V"

675374 OUT H_VID<0> 1 R1F152 1K 1% 603 CH
675374 OUT H_VID<1> 1 R1F142 1K 1% 603 CH
675374 OUT H_VID<2> 1 R1F132 1K 1% 603 CH
675374 OUT H_VID<3> 1 R1F122 1K 1% 603 CH
675374 OUT H_VID<4> 1 R1F112 1K 1% 603 CH

VCC3

CAPACITORS

SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: CPU DECOUPLING		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 68

762411 BI HI<0> TS01
762411 BI HI<1> TS02
762411 BI HI<2> TS03
762411 BI HI<3> TS04
762411 BI HI<4> TS05
762411 BI HI<5> TS06
762411 BI HI<6> TS07
762411 BI HI<7> TS08
762411 BI HI<8> TS09
762411 BI HI<9> TS10
762411 BI HI<10> TS11
762411 BI HI_STBS TS12
762411 BI HI_STBF TS13
761115 BI HI_VREF_GMCH TS14
768 7724 BI H_SMI* TS15
8 7724 BI H_STPCLK* TS16
8 53 BI H_TEMP_RET TS17
538 BI H_TEMP_SRC TS18
748 BI H_VID_ISOLATE<4> TS19
748 BI H_VID_ISOLATE<3> TS20
748 BI H_VID_ISOLATE<2> TS21
748 BI H_VID_ISOLATE<1> TS22
748 BI H_VID_ISOLATE<0> TS23
2213 BI VGA_RED TS24
2213 BI VGA_RED* TS25
2213 BI VGA_GREEN TS26
2213 BI VGA_GREEN* TS27

249 BI H_THERMTRIP_ICH* TS28
625130241252 BI PWRGD_3V TS29
1115 BI HI_VSWING_GMCH TS30
467 BI CK_14M_SIO TS31
247 BI CK_14M_ICH TS32
74528 BI H_SKTOCC* TS33
5861 BI VREG_USB_PCH_L TS34
5861 BI VREG_USB_NCH_L TS35
52718 BI H_DBR* TS36
7574525146112576 BI P_PCIRST* TS37
693635177 BI SMB_DATA_ISO TS38
693635177 BI SMB_CLK_ISO TS39
8 24 BI H_A20M* TS40
8 24 BI H_SLP* TS41
249 8 BI H_FERR* TS42
8 24 BI H_IGNNE* TS43
518 24 BI H_INIT* TS44
8 24 BI H_INTR TS45
8 24 BI H_NMI TS46
8 249 BI H_PWRGD TS47
2213 BI VGA_BLUE TS48
2213 BI VGA_BLUE* TS49
247 BI CK_48M_ICH_USB TS50
76247 BI CK_66M_ICH TS51
527 BI CK_66M_GLUE TS52
337 BI CK_P_33M_S1 TS53
327 BI CK_P_33M_S2 TS54

317 BI CK_P_33M_S3 TS55
7 BI CK_P_33M_S4 TS56
7 BI CK_P_33M_S5 TS57
7 BI CK_P_33M_S6 TS58
237 BI CK_P_33M_ICH TS59
517 BI CK_P_33M_FWH TS60
757 BI CK_P_33M_PORT80 TS61
467 BI CK_P_33M_SIO TS62
387 BI CK_14M_AUD TS63
23343121 BI P_INTA* TS64
23343121 BI P_INTB* TS65
2333323121 BI P_PME* TS66
3332315221 BI P_RST_SLOTS* TS67
7436333231217261 BI V_3P3_PCIVAUX TS68
5213 BI GLUE4_DDCSDA_3V TS69
5213 BI GLUE4_DDCSCL_3V TS70
2213 BI HSYNC_5V TS71
2213 BI VSYNC_5V TS72
-12V TS73
+12V TS74
+12V TS75
+12V TS76
VCC3 TS77
TS78

7454
3635302625242363 BI V_3P3_STBY TS80
6362615553524637
6058555250453050 BI V_5P0_STBY TS81
7664636261
231512109_8_7_67 BI VCCP TS83
767168675325
74675768 BI VREG_12V_POWER TS84
693635177 BI SMB_DATA_ISO TS86
693635177 BI SMB_CLK_ISO TS87

SCHEMATIC TITLE: INTEL<R> 845GE CUSTOMER REFERENCE BOARD

PAGE TITLE: DCL TRACK SPLITTERS

REV: 02.0

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
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SHEET: 69

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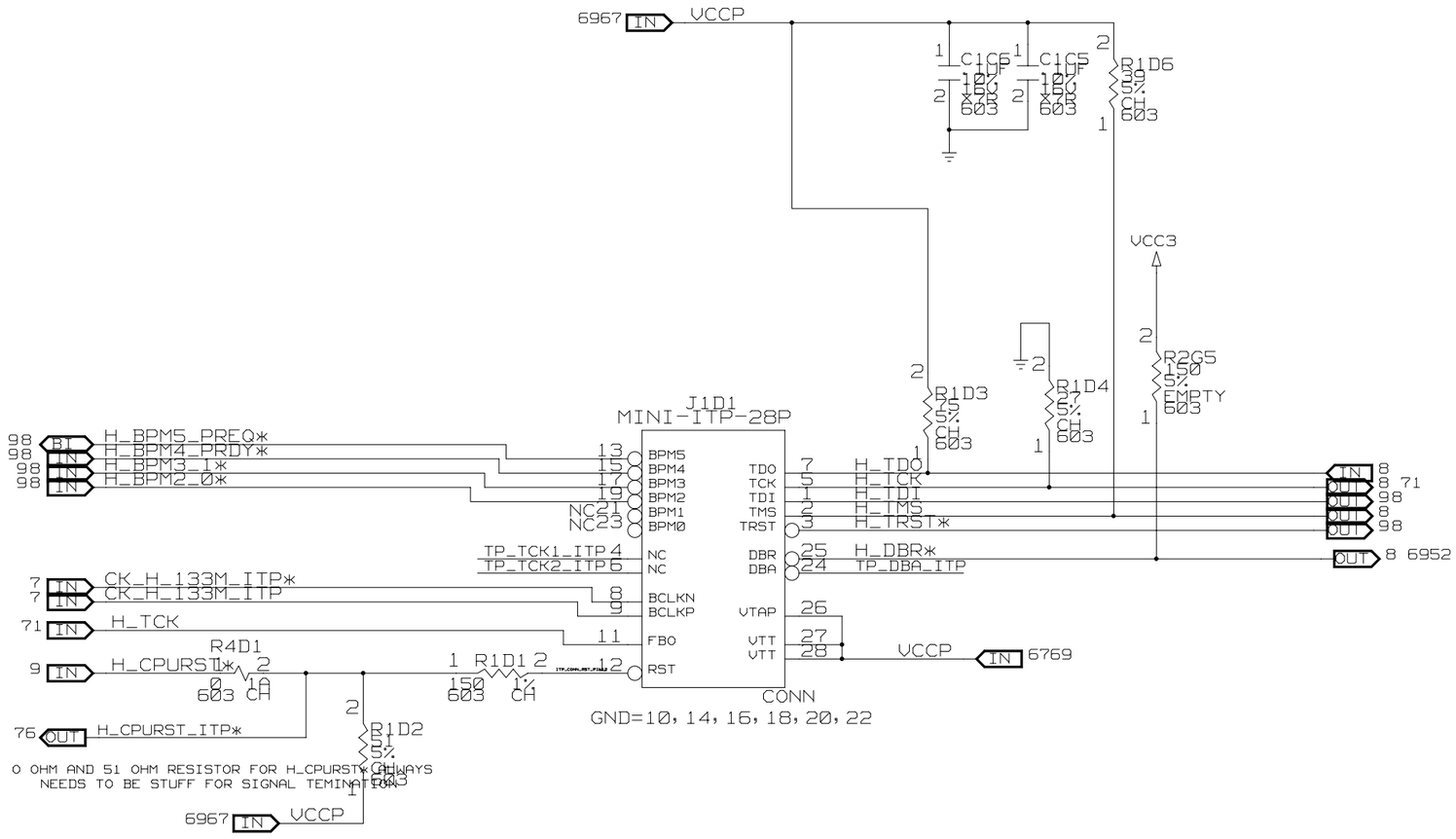
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: BLANK		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 70

ITP 700FLEX CONNECTOR



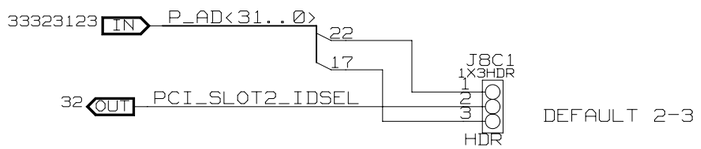
CAD NOTE: ROUTE H_TCK FROM THE TCK PIN OF THE CONNECTOR TO THE PROCESSOR PIN. FBO LENGTH = TCK + BPM LENGTHS TO CPU.

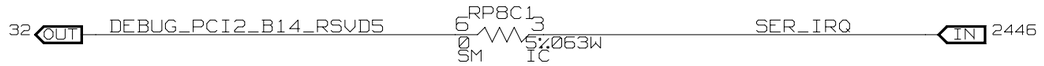
SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: ITP 700FLEX CONNECTOR		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 71

DEBUG HOOKS MOON ISA

J8B3/J8C1	PCI SLOT 2 MODE
1-2	MOON ISA
2-3	PCI (DEFAULT)





SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: MOON ISA		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 72

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SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD			
PAGE TITLE: BLANK			REV: 02.0
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 73

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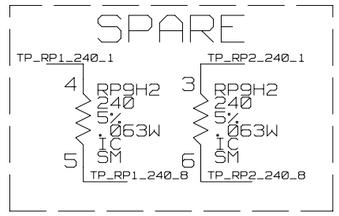
SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: BLANK		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 74

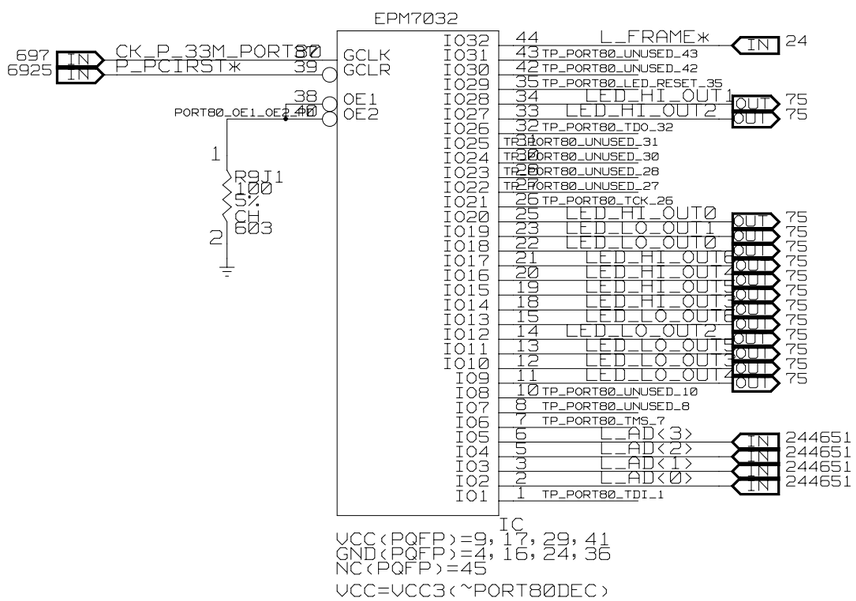


EPM7032AETC44-10

44 PIN TQFP

U9J1

EPM7032

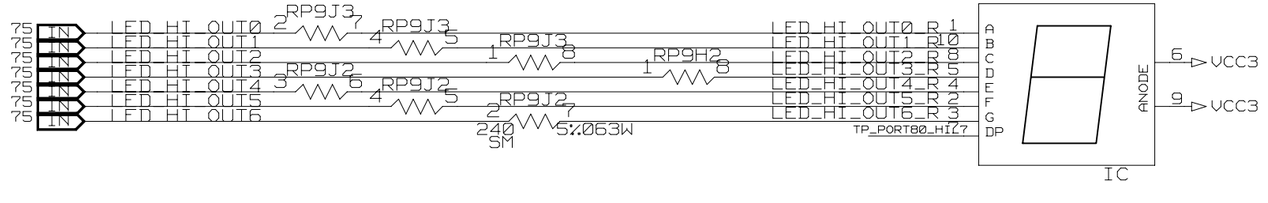


VCC(PQFP)=9,17,29,41
GND(PQFP)=4,16,24,36
NC(PQFP)=45
VCC=VCC3(~PORT80DEC)

CAD NOTE: ORIENT TO LEFT

DS9J1

LED_DISPLAY_10P

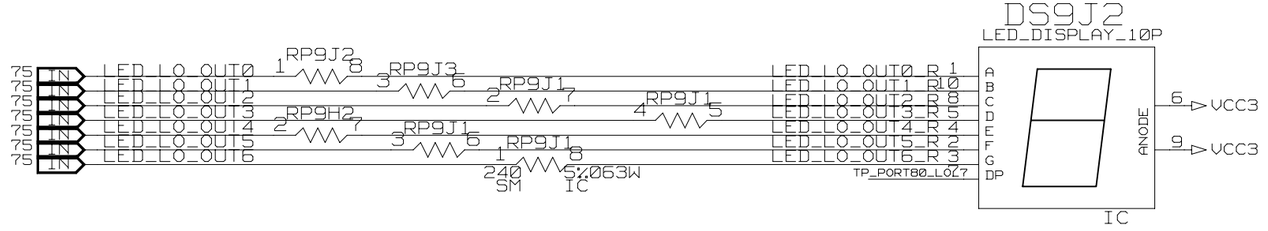


ALL RPACKS 240 OHMS

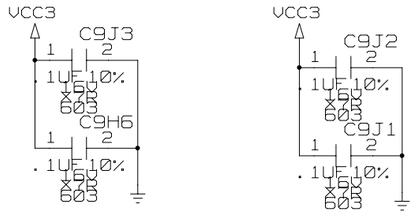
CAD NOTE: ORIENT TO RIGHT

DS9J2

LED_DISPLAY_10P



CAD NOTE: PLACE 1 EACH ON PINS 6 & 9 OF EACH DISPLAY



DEBUG/EV FEATURE: PORT 80 DECODER & DISPLAY

SCHEMATIC TITLE: INTEL(R) 845GE CUSTOMER REFERENCE BOARD		
PAGE TITLE: PORT 80 DECODER & DISPLAY		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 75

PAGE #	COMPONENT/FUNCTION
1	COVER PAGE.
2	CPU VREG CONTROLLER (INTERSIL)
3 & 4	CPU VREG DRIVERS AND PHASES
5	CPU VREG DECOUPLING

INTEL(R) 845GE/PE FMB2 VOLTAGE REGULATOR (FOUR PHASE IMPLEMENTATION)

THESE SCHEMATIC PAGES WILL REPLACE PAGES 67 AND 68 IN THE INTEL(R) 845GE DDR SCHEMATICS REV 2.0 FOR IMPLEMENTATION OF AN INTEL(R) 845GE/PE FMB2 FOUR PHASE VR

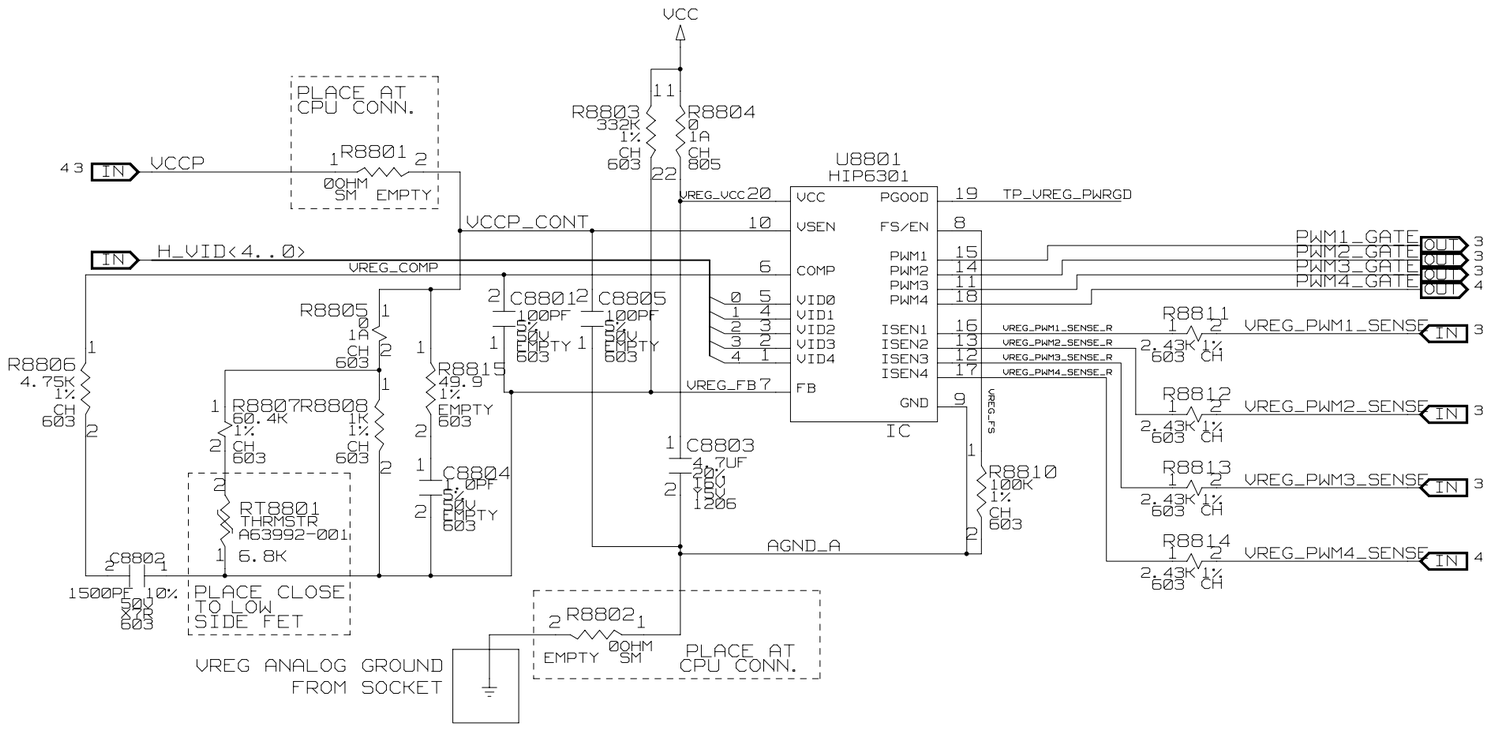
POWER SYMBOLS USED:

VCC3
VCC
+12V
-12V

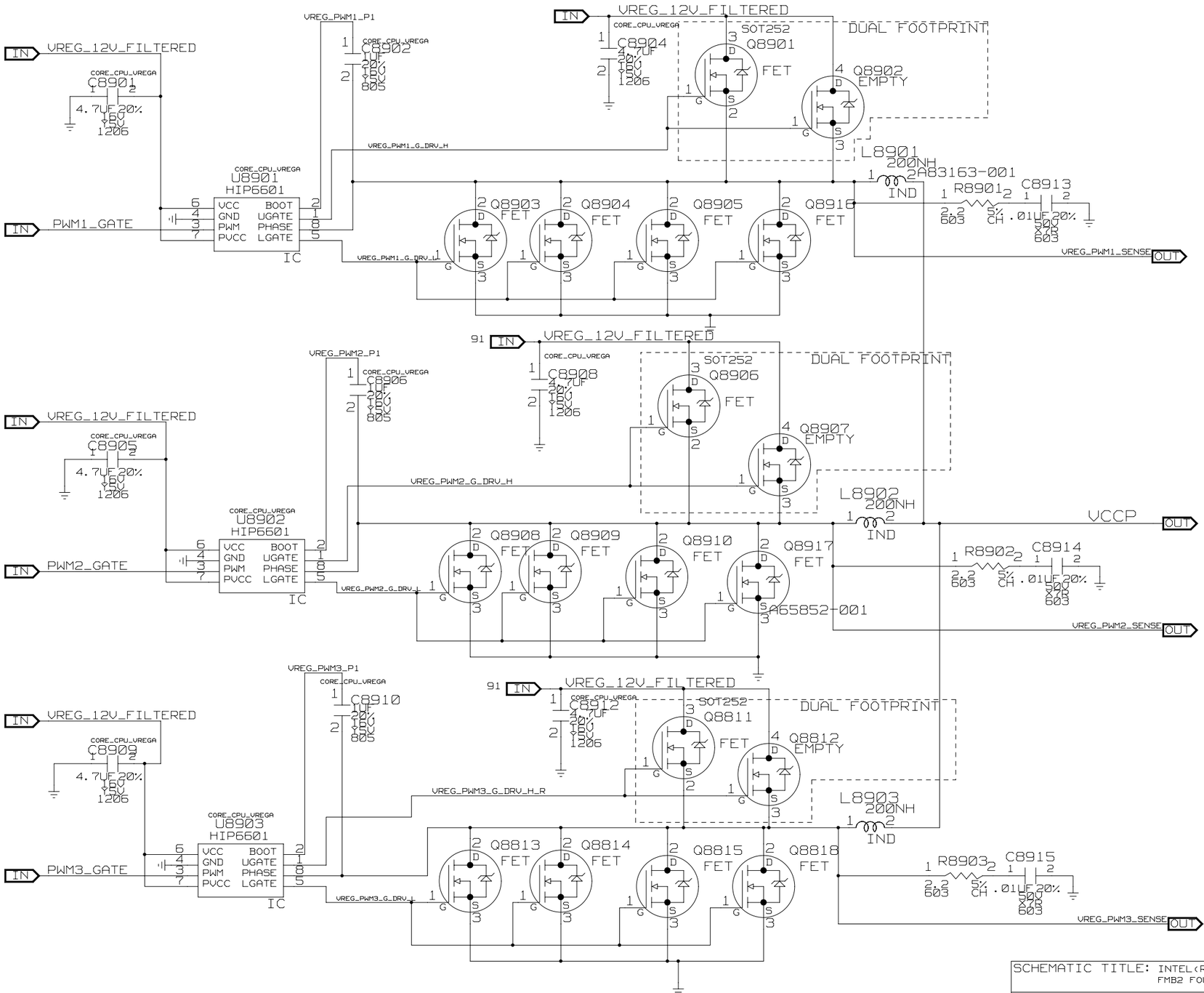
NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

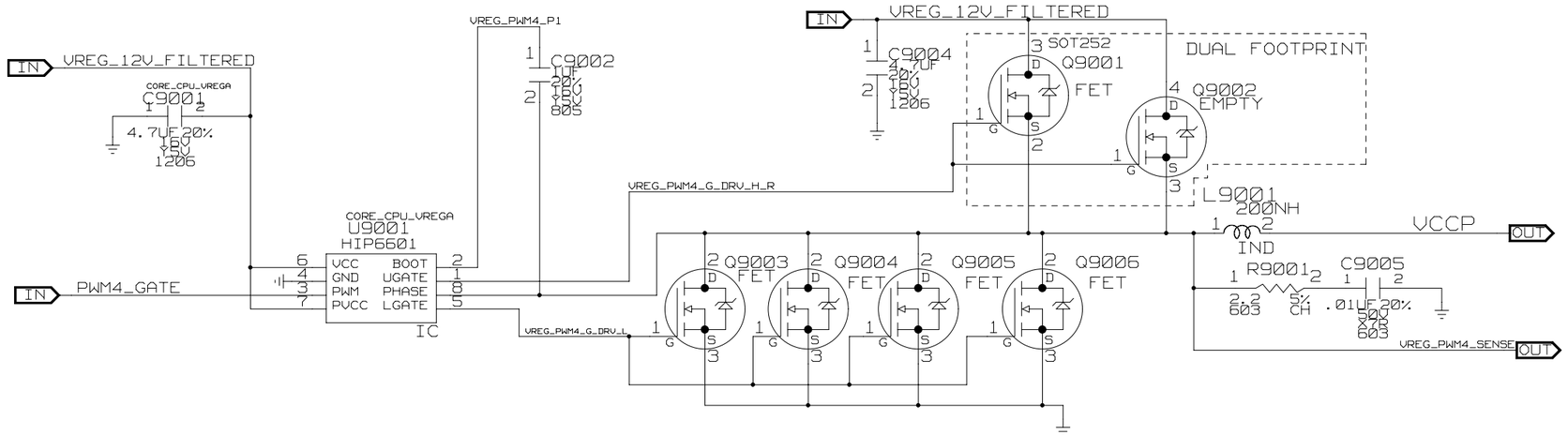
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL 845GE/PE DDR FMB2 FOUR PHASE VOLTAGE REGULATOR - 4 LAYER UATX		
PAGE TITLE: COVER PAGE		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 1



SCHEMATIC TITLE:	INTEL(R) PENTIUM(R) 4 SKT-N INTEL 845GE/PE DDR FMB2 FOUR PHASE VOLTAGE REGULATOR - 4 LAYER UATX
PAGE TITLE:	CPU VREG CONTROLLER
REV:	02.0
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED:	SEPT 13, 2002
SHEET:	2



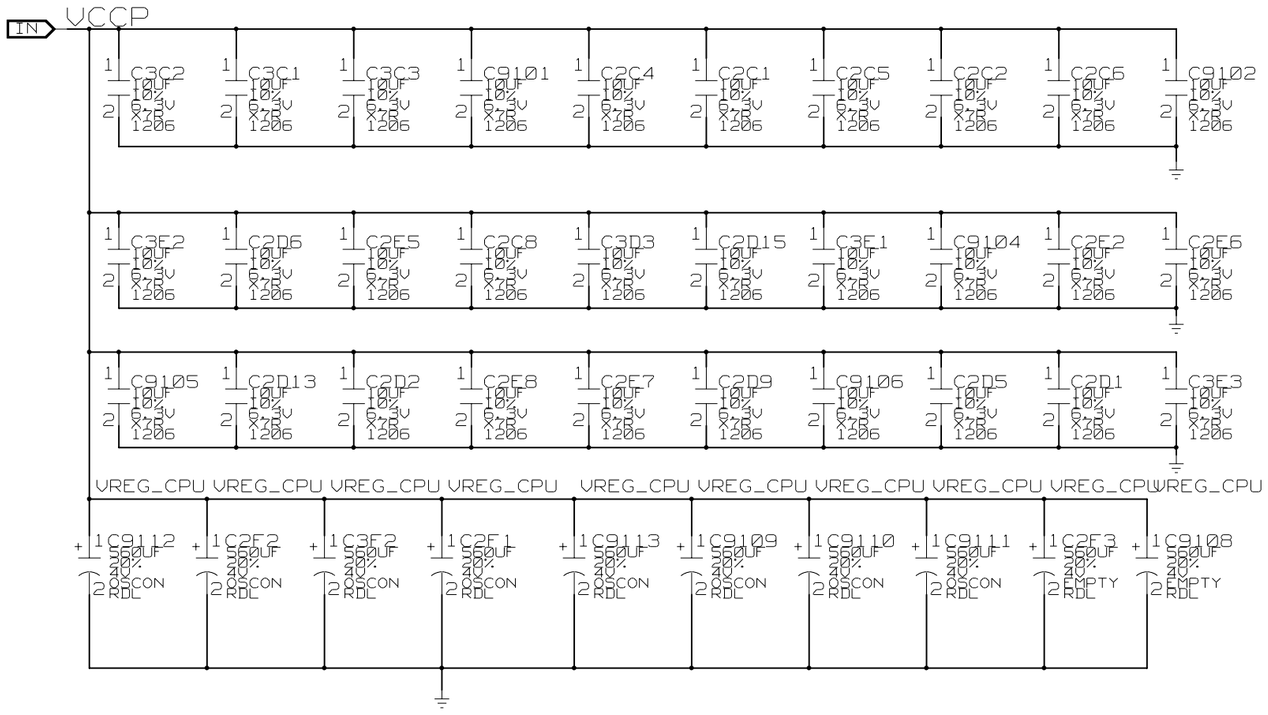
SCHEMATIC TITLE:	INTEL(R) PENTIUM(R) 4 SKT-N INTEL 845GE/PE DDR FMB2 FOUR PHASE VOLTAGE REGULATOR - 4 LAYER UATX
PAGE TITLE: CPU MAIN VREG (VCCP) 1/2	REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002
	SHEET: 3

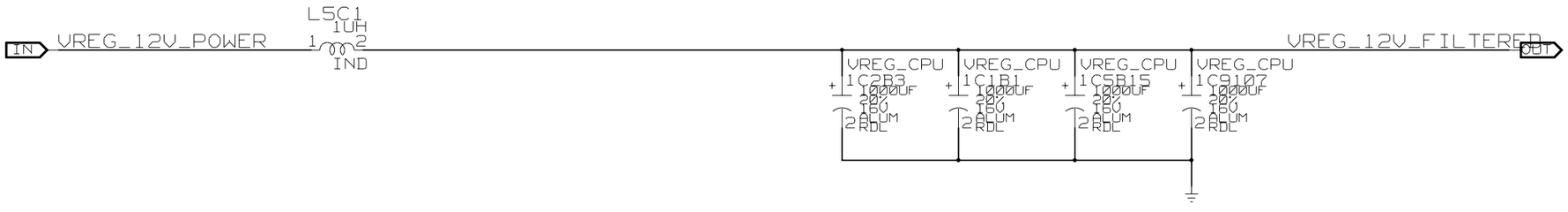


SCHEMATIC TITLE:	INTEL(R) PENTIUM(R) 4 SKT-N INTEL 845GE/PE DDR FMB2 FOUR PHASE VOLTAGE REGULATOR - 4 LAYER UATX
PAGE TITLE: CPU MAIN VREG (VCCP) 2/2	REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002
	SHEET: 4

CAD NOTE: PLACE AS MANY 1206 CAPACITORS AS POSSIBLE WITHIN CPU CAVITY

PLACEMENT NOTE FOR 1206:
PLACE 9 INSIDE CPU SOCKET
PLACE 12 NORTH OF SOCKET
PLACE 9 SOUTH OF SOCKET





SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL 845GE/PE DDR FMB2 FOUR PHASE VOLTAGE REGULATOR - 4 LAYER UATX		
PAGE TITLE: CPU DECOUPLING		REV: 02.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: SEPT 13, 2002	SHEET: 5