Intel® 848P Chipset

Platform Design Guide

For Use with the Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process and the Intel® Pentium® 4 Processor on 90 nm Process

March 2004

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Revision History

Revision	Description	Date
-001	Initial release	August 2003
-002	Added Section 15.3.2, Intel® Pentium® 4 Processor on 90 nm Process with Loadline A Requirements to Processor Power Requirements Replaced table, Section 17.4, MCH / Miscellaneous Items	February 2004
-003	Revised 3.3 V/1.5 V Power Sequencing, Section 15.3.6.3 and Added Section 15.3.6.4, 1.5V/V_CPU_IO Power Sequencing. Replaced Figure 10-40 in Section 10.11.1, RTC Crystal.	March 2004

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Introduction 1

This design guide describes Intel's design recommendations for systems based on the Intel® Pentium® 4 processor, the Intel® Pentium® 4 processor on 90 nm process, and the Intel® 848P chipset. In addition to providing motherboard design recommendations (e.g., layout and routing guidelines), this document also addresses other system design issues (e.g., power delivery).

The 848P chipset platforms support the following processors:

- Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process in the 478-pin package.
- Intel® Pentium® 4 processor on 90 nm process.

Carefully follow the design information, debug recommendations, and system checklists provided in this document. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues.

Note that the guidelines recommended in this document are based on experience and simulation work performed at Intel while developing the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process in the 478-pin package and Pentium 4 processor on 90 nm process in an 848P chipset-based system.

Board designers may use the associated Intel schematics as a reference. These schematics are provided in separate documents (see Section 1.1). The schematic sets provide reference schematics for the 848P chipset as well as common motherboard options. Additional flexibility is possible through other permutations of these options and components. Refer to the appropriate schematics document for the schematic diagrams.

Note: Unless otherwise specified, the term ICH5 in this document refers to both the 82801EB ICH5 and 82801ER ICH5R.

Note: Refer to the *Intel®848P Chipset Thermal Design Guid*e for package and retention mechanism keepout information.

Note: The main part of the processor-related power descriptions in this document are for processor loadline B specifications. Section 15.3.2 covers some of the differences between loadline B and loadline A.

1.1 Reference Documentation

Document[1]	Document Number / Location
Intel® 848P Chipset Customer Reference Board Schematics	253661
Intel® 865G/865GV/865PE/865P Chipset CRB Schematics Addendum for the Intel® Pentium® 4 Processor on 90 nm Process w/Loadline A Platforms -2 Phase VR	http://developer.intel.com/design/chipsets/schematics/300683.htm
Intel® 865G/865GV/865PE/865P Chipset CRB Schematics Addendum for the Intel® Pentium® 4 Processor on 90 nm Process w/Loadline A Platforms -3 Phase VR	http://developer.intel.com/design/chipsets/schematics/300684.htm
Intel® 848P Chipset Datasheet	http://developer.intel.com/design/chipsets/datashts/253575.htm
Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process and Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology Datasheet	http://developer.intel.com/design/pentium4/datashts/298643.htm
Intel® Pentium® 4 Processor on 90 nm Process Datasheet	http://developer.intel.com/design/pentium4/datashts/300561.htm
Intel® Pentium® 4 Processor on 90 nm Process Thermal and Mechanical Design Guide	http://developer.intel.com/design/Pentium4/guides/300564.htm
Voltage Regulator-Down (VRD) 10.0: for Desktop Socket 478 Design Guide	http://developer.intel.com/design/Pentium4/guides/252885.htm
Intel® 82801EB I/O Controller Hub 5 (ICH5) and Intel® 82801ER I/O Controller Hub 5 R (ICH5R) Datasheet	http://developer.intel.com/design/chipsets/datashts/252516.htm
Intel® 82801EB I/O Controller Hub 5 (ICH5) and Intel® 82801ER I/O Controller Hub 5 R (ICH5R) Thermal Design Guide	http://developer.intel.com/design/chipsets/designex/252673.htm
Intel® 848P Chipset Thermal Design Guide	253662
Intel® 82801EB I/O Controller Hub 5 (ICH5) and Intel® 82801ER I/O Controller Hub 5R (ICH5R) Thermal Design Guide	http://developer.intel.com/design/chipsets/designex/252673
PCI Bus Power Management Interface Specification	http://pcisig.com/
PCI Hot-Plug Specification	http://pcisig.com/
PCI Local Bus Specification	http://pcisig.com/
PCI-to-PCI Bridge Specification	http://pcisig.com/
Universal Serial Bus Specification 2.0	http://usb.org/developers/docs.html/
AGP Interface Specification V3.0	http://agpforum.org/
PCI Local Bus Specification, Revision 2.3	http://pcisig.com/
System Management Bus Specification	http://www.smbus.org/
AC '97 Specification, Revision 2.3	http://www.intel.com/ial/scalableplatforms/audio/index.htm/
Communication and Network Riser Specification, Revision 1.2	http://developer.intel.com/technology/cnr/download.htm
AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6)	http://T13.org (T13 1410D)
AP-728 Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test	http://www.intel.com/design/chipsets/applnots/292276.htm
AP-414 Intel® 82562ET LAN on Motherboard Design Guide Application Note	http://www.intel.com/design/network/applnots/82562ET_AP414.htm

Document[1]	Document Number / Location
AP-434 82562EZ(EX)/82540EM Dual Footprint Design Guide	http://www.intel.com/design/network/applnots/82562EZ-EM_ap434.htm
Alert Standard Format Specification, Revision 1.03	http://www.dmtf.org/standards/standard_alert.php
Serial ATA Specification, Revision 1.0	http://www.serialata.org/cgi-bin/SerialATA10gold.zip
Universal Serial Bus Specification, Revision 2.0	http://www.usb.org/developers/docs.html
Front Panel I/O Connectivity Design Guide	http://www.formfactors.org/developer/fpio_design_guideline.pdf

NOTES:
1. Contact your Intel field representative for information on additional documents.

1.2 Conventions and Terminology

This section defines conventions and terminology that are used throughout the design guide.

Term	Description
Aggressor	A network that transmits a coupled signal to another network.
AGTL+	The processor front side bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain, and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to assist the pull-up resistors during the first clock of a low-to-high voltage transition.
Asynchronous GTL+	The processor does not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output signals (FERR# and IERR#) and non-AGTL+ signals (THERMTRIP# and PROCHOT#) also utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0], and are therefore referred to as “Asynchronous GTL+ Signals”. However, all of the Asynchronous GTL+ signals are required to be asserted for at least two BCLKs in order for the processor to recognize them.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Crosstalk - Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal. • Forward Crosstalk - Coupling that creates a signal in a victim network that travels in the same direction as the aggressor’s signal. • Even Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Flight Time	Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the Tco of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, flight time is defined as: The time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer’s conditions required for AC timing specifications; i.e., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver’s AC timings. Maximum and Minimum Flight Time - Flight time variations are caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance, and differences in I/O buffer performance as a function of temperature, voltage, and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects. Maximum flight time is the largest acceptable flight time a network will experience under all conditions. Minimum flight time is the smallest acceptable flight time a network will experience under all conditions.
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.

Term	Description
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Overshoot	The maximum voltage observed for a signal at the device pad, measured with respect to VCC.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.
Pin	The contact point of a component package to the traces on a substrate, such as the motherboard. Signal quality and timings can be measured at the pin.
Power-Good	“Power-Good,” “PWRGOOD,” or “CPUPWRGOOD” (an active high signal) indicates that all of the system power supplies and clocks are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.
Ringback	The voltage to which a signal changes after reaching its maximum absolute value. Ringback may be caused by reflections, driver oscillations, or other transmission line phenomena.
Front Side Bus	The Front Side Bus is the processor bus that connects the processor to the MCH.
Setup Window	The time between the beginning of Setup to Clock (TSU_MIN) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
SSO	Simultaneous Switching Output (SSO) effects are differences in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal or in the same direction. These are called odd mode and even mode switching, respectively. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (“push-out”) or a decrease in propagation delay (“pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	The minimum voltage extending below VSS observed for a signal at the device pad.
VCC_CPU	VCC_CPU is the core power for the processor. The FSB is terminated to VCC_CPU.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
VRD 10.0	“VRD 10.0” refers to the Voltage Regulator Module (a down on the board solution) specification for the Intel® Pentium® 4 processor on 90 nm process. It is a DC-DC converter module that supplies the required voltage and current to a single processor.
AC	Audio Codec
ASF	Alert Standard Format
AMC	Audio/Modem Codec.
Anti-Etch	Any plane-split, void or cutout in a VCC or GND plane is referred to as an anti-etch
BER	Bit Error Rate
BMC	Baseboard Management Controller.
CMC	Common Mode Choke
CNR	Communications and Networking Riser
EHCI	Enhanced Host Controller Interface
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge

Term	Description
FS	Full-speed. Refers to USB
HS	High-speed. Refers to USB
Intel® ICH5	I/O Controller Hub Fifth Generation
LCI	LAN Connect Interface
LOM	LAN on Motherboard
LPC	Low Pin Count
LS	Low-speed. Refers to USB
MC	Modem Codec
PCM	Pulse Code Modulation
PLC	Platform LAN Connect
RTC	Real Time Clock
SATA	Serial ATA
SMBus	System Management Bus. A two-wire interface through which various system components can communicate
SPD	Serial Presence Detect
S/PDIF	Sony/Phillips Digital Interface
STD	Suspend To Disk
STR	Suspend To RAM
TCO	Total Cost of Ownership
TDM	Time Division Multiplexed
TDR	Time Domain Reflectometry
UBGA	Micro Ball Grid Array
UHCI	Universal Host Controller Interface
USB	Universal Serial Bus

System Overview 2

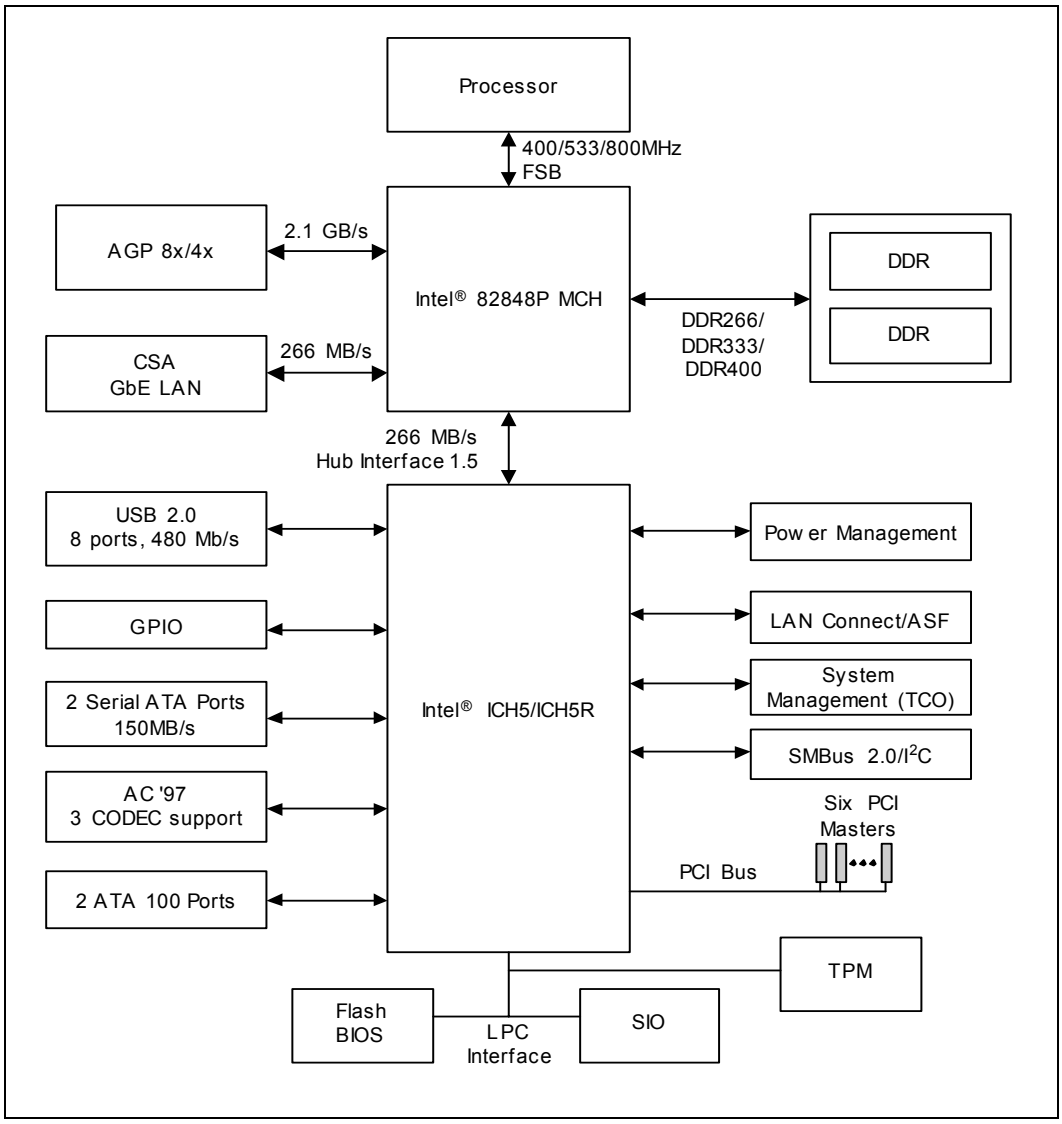
The 848P chipset is designed for use with the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process processor and the Pentium 4 processor on 90 nm process. The MCH component provides the processor interface, DDR interface, AGP interface, hub interface, and CSA interface.

The processor interface supports the Pentium 4 processor subset of the extended mode of the Scalable Bus Protocol. The MCH memory interface supports one channels of DDR, and the AGP interface supports 0.8 V/1.5 V signaling with 8X/4X data transfers and 8X/4X AGP fast writes.

The 848P chipset platform supports the fifth generation I/O controller hub (ICH5/ICH5R).

The MCH's role in a system is to manage the flow of information between its interfaces: the processor front side bus (FSB), the memory attached to the DDR controller, the AGP 2.0/3.0 port, the hub interface, and CSA interface. This includes arbitrating between the interfaces when each initiates an operation. While doing so, the MCH must support data coherency via snooping and must perform address translation for access to AGP Aperture memory. To increase system performance, the MCH incorporates several queues and a write cache.

Figure 2-1. Intel® 848P Chipset System Block Diagram



2.1 MCH

2.1.1 Host Interface

The 848P chipset is designed for systems based on the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process in a 478-pin package and the Pentium 4 processor on 90 nm process. The chipset supports FSB frequencies of 400 MHz, 533 MHz, and 800 MHz (100 MHz, 133 MHz, and 200 MHz HCLK, respectively) using a scaleable FSB VCC_CPU. The 848P chipset MCH supports 32-bit host addressing and decodes up to 4 GB of the processor's memory address space. Host-initiated I/O cycles are decoded to AGP/PCI_B, CSA, hub interface, or MCH configuration space. Host-initiated memory cycles are decoded to AGP/PCI_B, hub interface, or system memory. All memory accesses from the host interface that hit the graphics aperture are translated using an AGP address translation table. AGP/PCI_B device accesses to non-cacheable system memory are not snooped on the host bus. Memory accesses initiated from AGP/PCI_B using PCI semantics and from the hub interface to system memory will be snooped on the host bus.

2.1.2 System Memory Interface

The MCH integrates a system memory DDR controller with one 64-bit wide interface. The MCH supports DDR memory, the buffers support SSTL_2 signal interfaces, and the memory controller interface is fully configurable through a set of control registers.

System Memory Interface

- Supports one 64-bit wide DDR data channel
- Available bandwidth up to 3.2GB/s (DDR400)
- Supports non ECC DIMMs.
- Supports 128-Mb, 256-Mb, 512-Mb DDR technologies
- Supports only x8, x16, DDR devices with four banks
- Registered DIMMs not supported
- Supports opportunistic refresh
- Up to 16 simultaneously open pages (four per row, four rows maximum)
- SPD (Serial Presence Detect) scheme for DIMM detection support
- Suspend-to-RAM support using CKE
- Supports configurations defined in the JEDEC DDR1 DIMM specification only

2.1.3 Hub Interface

The hub interface connects the MCH to the ICH5. The MCH supports only HI 1.5, which uses HI 1.0 protocol with HI 2.0 electrical characteristics. The hub interface runs at 266 MT/s (with 66 MHz base clock) and uses 1.5 V signaling. Accesses between the hub interface and AGP are limited to hub interface originated memory writes to AGP.

2.1.4 Communications Streaming Architecture (CSA) Interface

The CSA interface connects the MCH to a Gigabit Ethernet (GbE) controller (e.g., Intel® 82547EI GbE controller). The CSA interface supports only HI 1.5 over the interface, which uses HI 1.0 protocol with HI 2.0 electrical characteristics. The CSA interface runs at 266 MT/s (with 66 MHz base clock) and uses 1.5 V signaling.

2.1.5 AGP Interface

A single AGP or PCI 66 component or connector (not both) is supported by the MCH's AGP interface. Support for AGP 3.0 including 0.8 V and 1.5 V AGP electrical characteristics. Support for a single PCI-66 device is limited to the subset supported by the AGP 2.0 specification.

The AGP/PCI_B interface supports both AGP 2.0 and AGP 3.0 signaling and up to 4X/8X Fast Writes. AGP semantic cycles to system DDR are not snooped on the host bus. PCI semantic cycles to system DDR are snooped on the host bus. The MCH supports PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization. The MCH contains a 32-deep AGP request queue. High-priority accesses are supported.

2.2 Intel® I/O Controller Hub 5 (ICH5)

The I/O controller hub provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many I/O functions:

- Upstream hub interface for access to the MCH
- 2-channel Ultra ATA/100 Bus Master IDE controller
- Two Serial ATA host controllers
- One EHCI controller and four UHCI controllers (Expanded capabilities for eight, USB 2.0 ports)
- I/O APIC
- SMBus 2.0 controller
- Integrated ASF management controller
- LPC / flash BIOS interface
- AC '97 2.3 interface
- PCI 2.3 interface
- Integrated System Management controller
- Integrated LAN controller

2.2.1 Integrated LAN Controller

The ICH5 incorporates an integrated LAN controller. Its bus master capabilities enable the component to process high-level commands and perform multiple operations, which lowers processor utilization by off-loading communication tasks from the processor.

The ICH5 supports several components depending upon the target market. Available LAN components include the Intel® 82562ET/82562EZ for basic Ethernet 10/100 connection, Intel® 82562EM/82562EX component that provides an Ethernet 10/100 connection with the added manageability capabilities, Intel® 82540EM GbE controller, and Intel® 82551QM fast ethernet controller.

2.2.2 Serial ATA (SATA)

The ICH5 contains two integrated Serial ATA host controllers capable of independent DMA operation on two ports. The SATA controllers are completely software transparent with the IDE interface, while providing a lower pin count and higher performance. The ICH5 SATA interface supports data transfer rates up to 150 MB/s.

2.2.3 Expanded USB Support

The ICH5 contains four UHCI host controllers and one EHCI host controller. Each UHCI Host controller includes a root hub with two separate USB ports each, for a total of eight USB ports. The EHCI host controller includes a root hub that supports up to eight USB 2.0 ports. The ICH5 supports a maximum of eight USB ports at any given time. The connection to either a UHCI or the EHCI is dynamic and dependent on the USB device capability meaning that all ports support HS/FS/LS USB devices.

2.2.4 Manageability and Other Enhancements

The ICH5 platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

2.2.4.1 SMBus 2.0

The ICH5 integrates an SMBus 2.0 controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on RAM, thermal sensors, CNR cards, PCI cards, etc. The slave interface allows an external microcontroller to access system resources.

2.2.4.2 ASF Management Controller

The ICH5 integrates an ASF 1.03-compliant management controller for platform management. The ICH5 ASF controller uses the SMLink internally as a dedicated bus to interface with the ICH5 LAN controller.

2.2.4.3 Interrupt Controller

The interrupt capabilities of the ICH5 platform maintain the support for up to eight PCI interrupt pins and PCI 2.3 Message-Based Interrupts. In addition, the ICH5 supports processor front side bus interrupt delivery.

2.2.4.4 Intel-Compatible Flash BIOS

The ICH5 platform supports Intel-compatible flash BIOS memory size up to 8 Mbytes for increased system flexibility.

2.2.5 AC ’97 6-Channel Support

The Audio Codec ’97 (AC ’97) Specification defines a digital interface that can be used to attach an audio codec (AC), a modem codec (MC), and/or an audio/modem codec (AMC) in various configurations. The AC ’97 Specification defines the interface between the system logic and the audio or modem codec known as the AC-link.

The ICH5 platform’s AC ’97 (with the appropriate codecs) improves overall platform integration by incorporating the AC-link. By using an audio codec, the AC-link allows for cost-effective, high-quality, integrated audio on the ICH5 platform. In addition, an AC ’97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC ’97. The ICH5 integrated digital link allows several external codecs to be connected to the ICH5. The system designer can provide audio with an audio codec, a modem with a modem codec, or an integrated audio/modem codec (Figure 2-2). The digital link is expanded to support three audio codecs or a combination two audio codecs and a modem codec (Figure 2-3 and Figure 2-5).

The digital link in the ICH5 supports AC ’97 Revision 2.3 allowing for up to three codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec.

The ICH5 expands audio capability with support for up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center, and SubWoofer for a complete surround sound effect. ICH5 has expanded support for three audio codecs on the AC-link.

Figure 2-2. AC '97 with Audio/Modem Codec

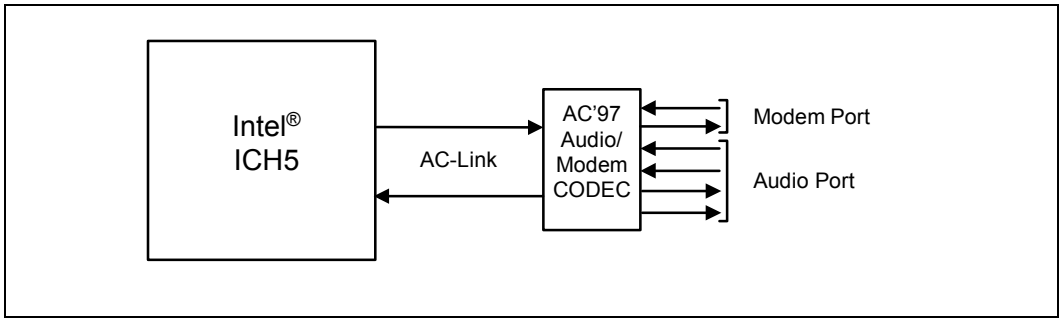


Figure 2-3. AC '97 with Audio Codecs (4 Channel Secondary)

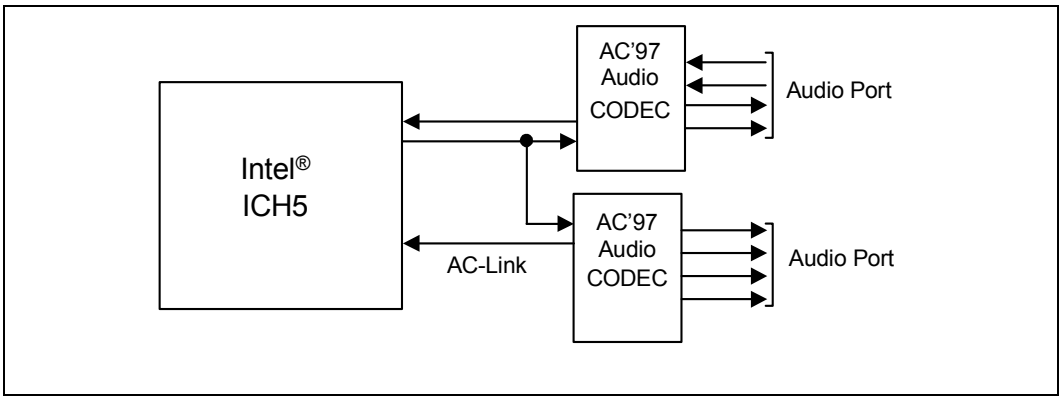


Figure 2-4. AC '97 with 2 Audio and a Modem Codec (4 Channel Secondary)

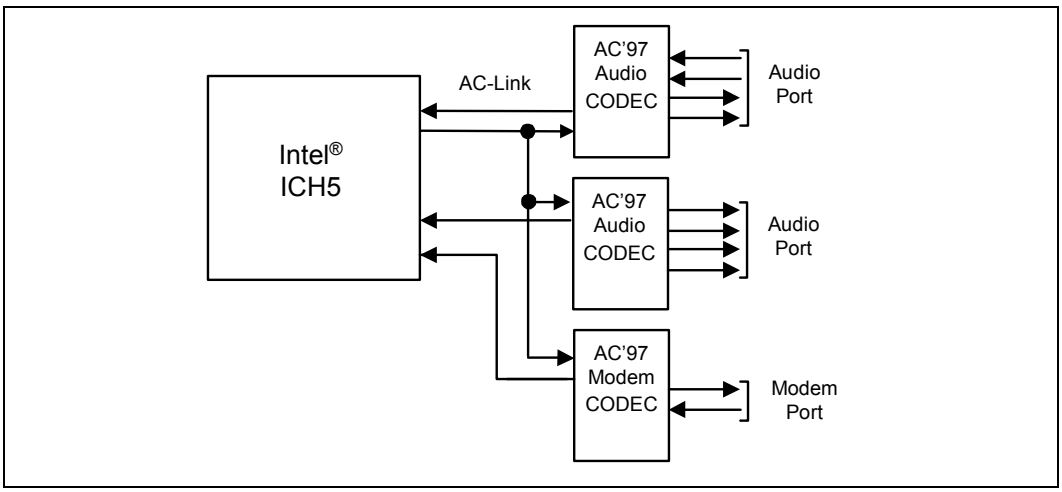
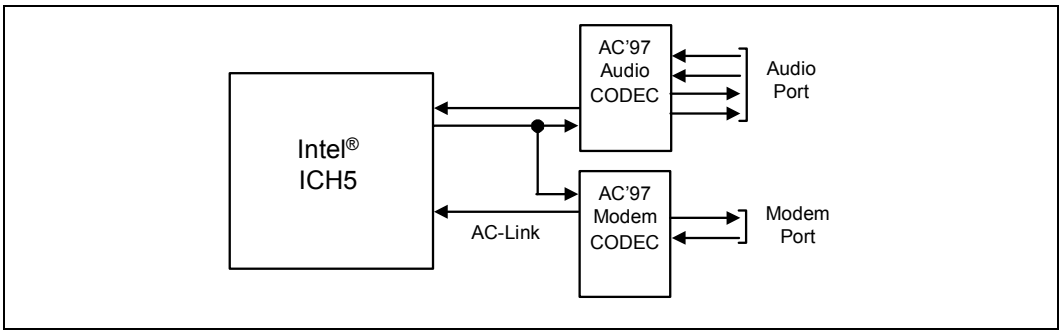


Figure 2-5. AC '97 with Audio and Modem Codec



2.3 Bandwidth Summary

Table 2-1 and Table 2-2 provides a summary of the bandwidth requirements for the 848P chipset MCH and ICH5.

Table 2-1. Intel® 848PMCH System Bandwidth Summary

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth
Front Side Bus	100/133/200	4	8	3.2 / 4.2 / 6.4 GB/s
DDR-SDRAM	133/166/200	2	8	2.1 / 2.7 / 3.2 GB/s
AGP	66	8	4	2.1 GB/s
CSA	66	4	1	266 MB/s

Table 2-2. Intel® ICH5 System Bandwidth Summary

Interface	Clock Speed (MHz)	Samples Per Clock	Data Rate (Mega-samples/s)	Data Width (Bits)	Bandwidth (MB/s)
Hub Interface	66	4	266	8	266
PCI 2.3	33	1	33	32	133
IDE	Up to 44.444 Write Up to 50 Read	1	44.444 (Write) 50 (Read)	16	88.9 (Write) 100 (Read)
SATA	750	2	1500	1	150
LCI	5 - 50	1	5 - 50	3	1.875 – 18.75
AC ’97	12.288	1	12.288	1	1.536
LPC	33	1	33	4	16.5
USB 2.0 High-speed	Up to 240 (embedded in data)	Up to 2	480	1	60
SMBus	10-16 kHz	1	10	1	1.25 KB/s

2.4 Safer Computing

Today, most protection against computer viruses and unauthorized intrusions consists of adding and updating software that installs outer barriers and surveillance tools. The goal of Safer Computing is to go much deeper, integrating a level of trust into the actual hardware and pre-operating system environments. Applications intended for e-business are based on trust in the communication partner and the reliability of the connection.

The Trusted Computing Platform Alliance (TCPA), an industry consortium of hardware and software manufacturers, has created a specification for a Trusted Platform Module (TPM). The objective of the TPM is to establish a baseline of platform integrity and enhance system security. TPMs are available from several integrated circuit vendors in the form of a silicon component and accompanying software. When integrated into the PC, a TPM provides protected storage of platform data allowing for platform-level authentication toward the goal of making data files, transactions and communication more trustworthy.

The TPM connects to the ICH5 via the Low Pin Count (LPC) bus to communicate with the rest of the platform. See Section 10.13 for TPM implementation guidelines. For more information on TPMs and Safer Computing, refer to the Intel Desktop Platform Vision Guide for 2003 and the TCPA web site http://www.trustedcomputing.org.

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Platform Stack-Up and Placement Overview 3

In this chapter, an example of a 848P chipset platform component placement and stack-up is presented for a desktop system in a µATX or ATX board form factor with single-channel, DDR266/333/400 SDRAM memory capabilities.

3.1 General Design Considerations

This section documents motherboard layout and routing guidelines for 848P chipset platforms. This section does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

Caution: **If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.**

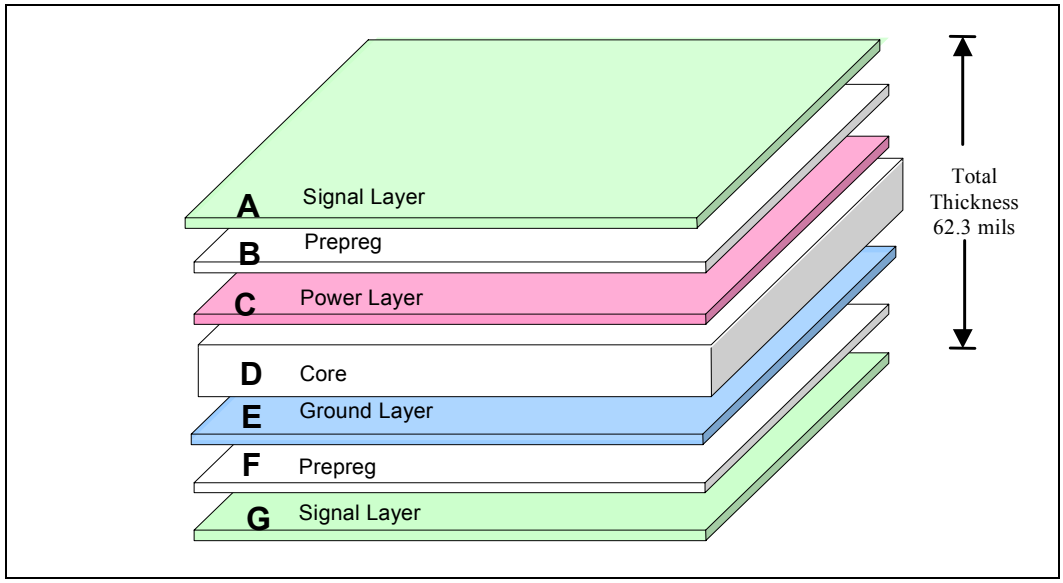
The trace impedance typically noted (i.e., 60 Ω ± 15%) is the “nominal” trace impedance for a 5-mil wide trace (i.e., the impedance of the trace when not subjected to the fields created by changing current in neighboring traces). When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. Additionally, these routing guidelines are created using a PCB (Printed Circuit Board) stack-up as illustrated in Figure 3-1.

3.2 Nominal 4-Layer Board Stack-Up

The 848P chipset platforms require a board stack-up yielding a target board impedance of 60 Ω ± 15%. Recommendations in this design guide are based on the following 4-layer board stack-up. The stack-up numbers may vary; thus, it is important to stay within the specified tolerances.

Figure 3-1. 4-Layer PCB Stack-Up Example



Description	Nominal Value	Tolerance	Comments
Board Impedance Z_0	60 Ω	± 15%	With nominal 5-mil trace width
Prepreg Dielectric Er	4.1	± 0.3	@ 100 MHz
Soldermask Er	4.0	± 0.5	@ 100 MHz
Soldermask Thickness	1.0 mil	± 0.5 mils	From top of trace
Trace Width	5.0 mils	± 0.5 mils	Standard trace

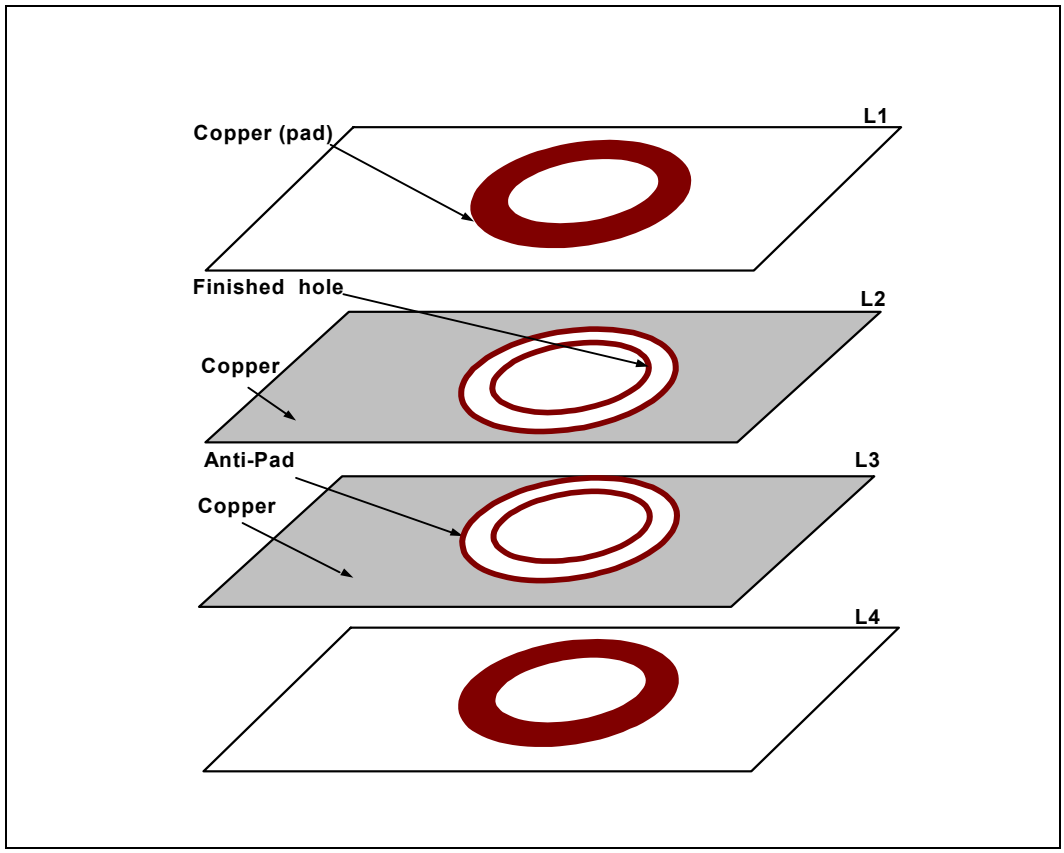
Layer	Description	Nominal Value	Tolerance	Comments
A	Signal Layer	0.7 mils	(See Note 2)	0.5 oz Cu (See note 1)
B	Prepreg	4.4 mils	± 0.6 mils	1 sheet 2116 Pre-Preg
C	Power Layer	1.4 mils	± 0.2 mils	1 oz unplated Cu
D	Core	47 mils	± 5.0 mils	6 sheets 7628 Prepreg (7.8 ± 0.5 mils)
E	Ground Layer	1.4 mils	± 0.2 mils	1 oz unplated Cu
F	Prepreg	4.4 mils	± 0.6 mils	1 sheet 2116 Pre-Preg
G	Signal Layer	0.7 mils	(See Note 2)	0.5 oz Cu (See note 1)

NOTES:
1. Thickness before plating
2. Thickness after plating varies, 0.7 + (1.3 mils – 1.42 mils)

3.3 PCB Technology Considerations

Intel has found that the following recommendation aids in the design of a 848P chipset-based platform. Simulations and reference platform are based on the following technology and is recommended that designers adhere to these guidelines.

Figure 3-2. PCB Technologies Stack-Up



Number of Layers	
Stack-up	4 Layer
Cu Thickness	0.5 oz outer (plated); 1 oz Inner
Final Board Thickness	62.3 mils (± 5 mils)
Material	Fiberglass made of FR4
Signal and Power Via Stack	
Via Pad	25 mils
Via Anti-Pad	40 mils
Via Finished Hole	14 mils

3.3.1 Component Motherboard Layout (Pads and Vias)

Intel currently recommends non-soldermask defined pads (metal defined pads) on connecting vias for the chipset for improved solder-joint reliability.

The solder mask opening and the registration accuracy of that opening relative to the pad is critical to ensure good solder joints and minimize shorting. If the opening is too large, misregistration may uncover a nearby trace increasing the possibility of a short occurring. Regardless of opening size, misregistration may cause soldermask material to cover part or the entire pad, yielding a joint with a poor cross-section (reliability) or a complete open.

Tips:

- Inconsistent soldermask coverage between the via and pad may lead to top and bottom side tenting in order to avoid accidentally wicking the solder ball into the via-hole creating an open or unreliable joint. Tenting both sides may trap moisture in the via during reflow causing severe soldermask damage as it vents. One solution is to ensure that the raw printed circuit boards are dry; an alternative is to allow for a small topside vent-hole (pin-hole) in the tenting.
- A reliability consideration to take into account when choosing a pad size: The pad size also affects the joint height; a smaller pad forces a taller joint. There are industry claims that a taller joint increases the mechanical flexibility of the joint and thus may improve power cycle and temperature cycle joint life.
- Solder mask must cap the vias on the bottom side of the board to minimize heat transfer to the solder.

Figure 3-3. Via-Pad Layout Metal-Defined Pads

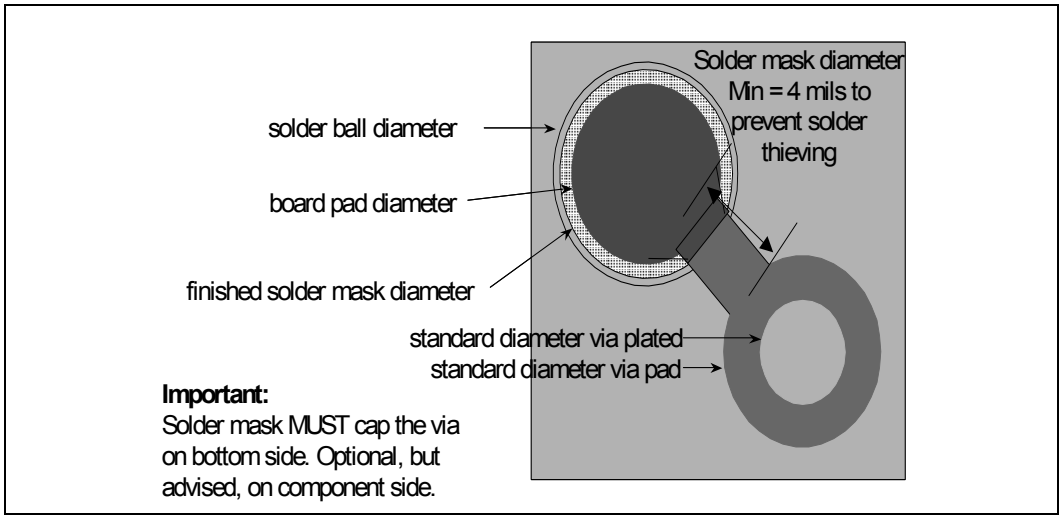


Table 3-1. Via-Pad Layout Metal-Defined Pads

Component	Solder Ball Pitch	Solder Ball Diameter	Board Pad Diameter	Finished Solder Mask Diameter
Processor	1.27 mm	30 mils	20 mils	22 – 26 mils
MCH	1.00 mm	24 mils	18 mils	20 – 24 mils
Intel® ICH5	1.27 mm	30 mils	20 – 24 mils	24 – 27mils

Figure 3-4. Via-Pad Layout Solder Mask-Defined Pads

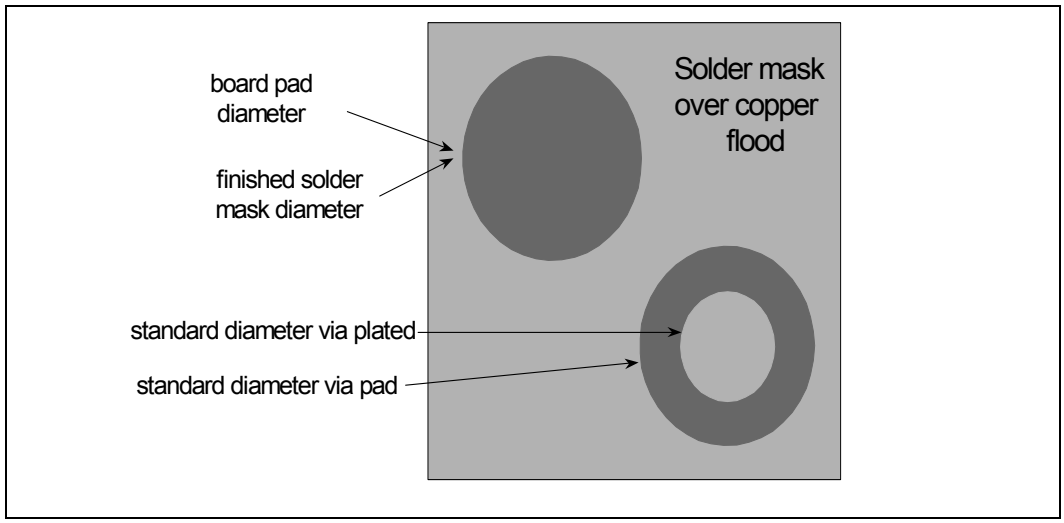


Table 3-2. Via-Pad Layout Solder Mask-Defined Pads

Component	Solder Ball Pitch	Solder Ball Diameter	Board Pad Diameter	Finished Solder Mask Diameter
Processor	1.27 mm	30 mils	22 – 26 mils	22 – 26 mils
MCH	1.00 mm	24 mils	18 mils	18 mils
Intel® ICH5	1.27 mm	30 mils	20 – 24 mils	20 – 24 mils

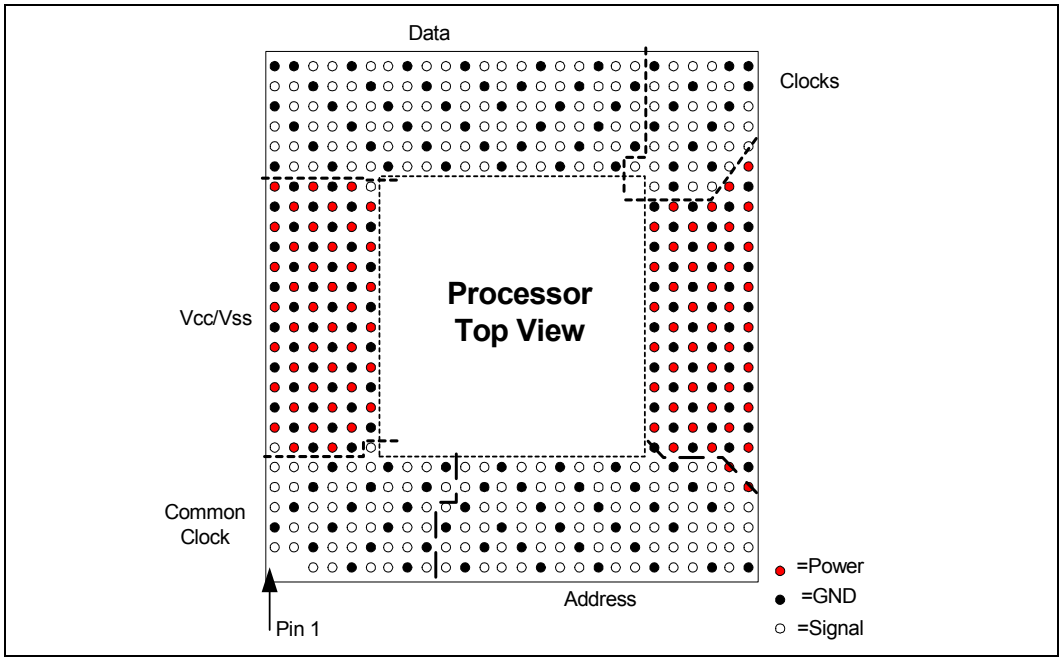
3.4 Component Quadrant Layout

The quadrant layouts shown are approximations. The quadrant layout figures do not show the exact component ball count; only general quadrant information is presented and is intended for reference while using this document. Only the exact pin or ball assignment should be used to conduct routing analysis. Refer to the respective component datasheet for pin or ball assignment information.

3.4.1 Processor Quadrant Layout

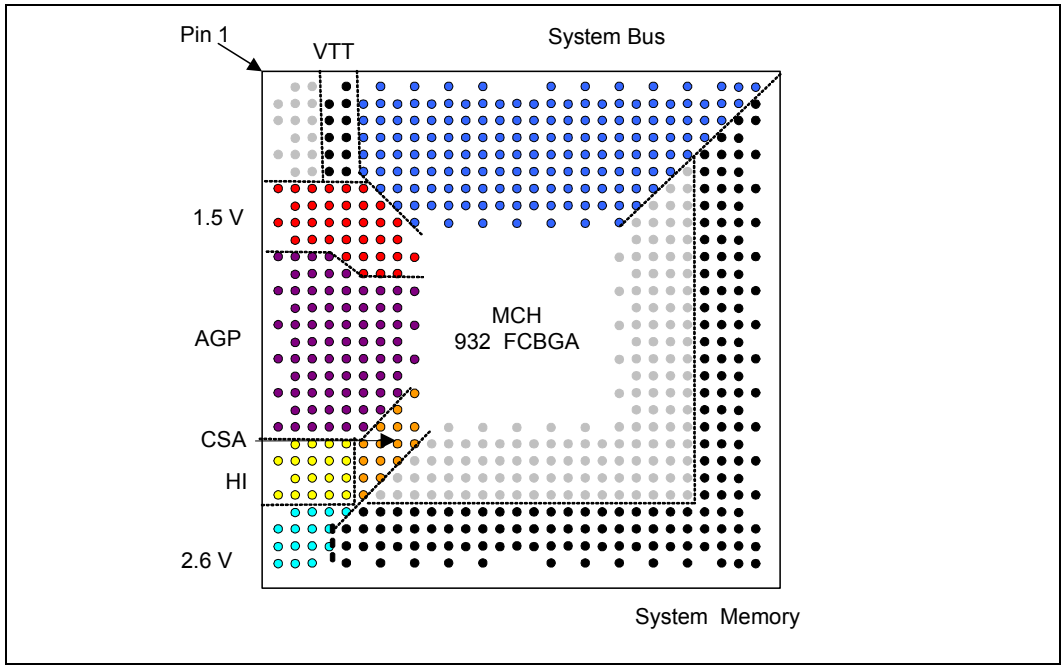
Figure 3-5 shows the quadrant layout of the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Pentium 4 processor on 90 nm process.

Figure 3-5. Processor Component Quadrant Layout (Top View)



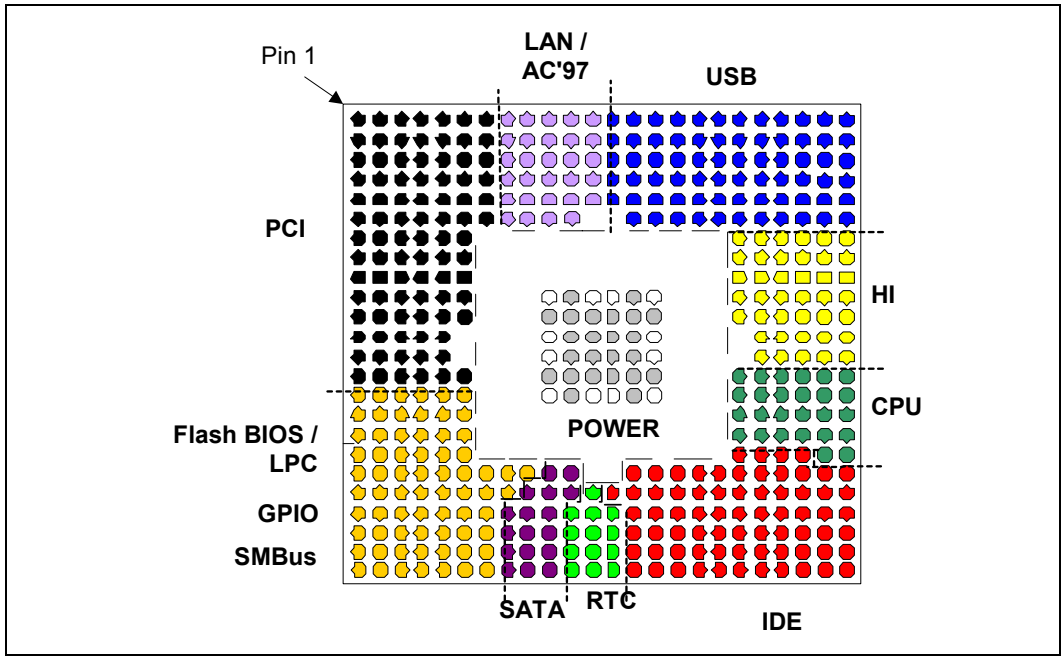
3.4.2 MCH Component Quadrant Layout

Figure 3-6. MCH Component Quadrant Layout (Top View)



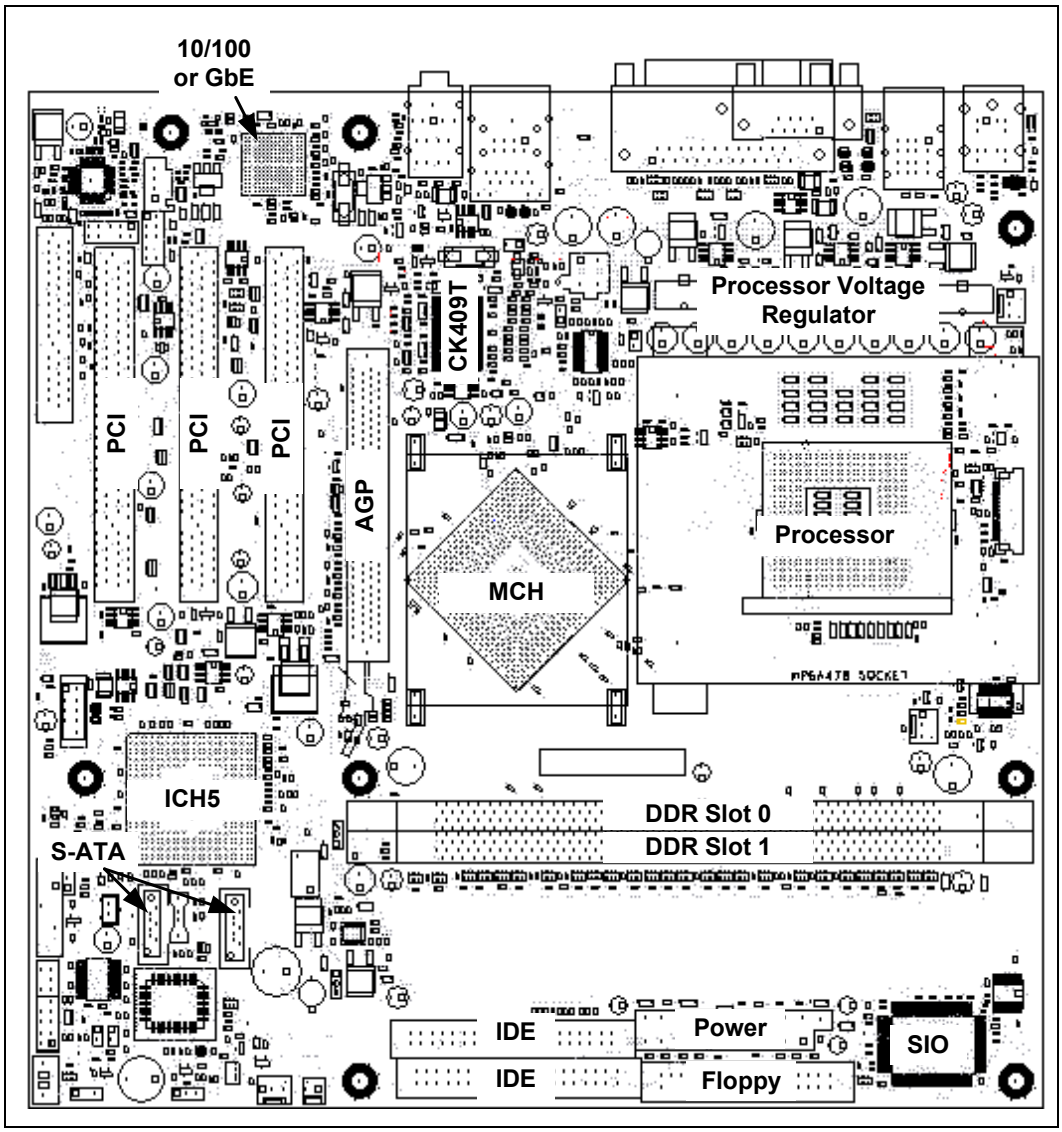
3.4.3 Intel® ICH5 Component Quadrant Layout

Figure 3-7. Intel® ICH5 Quadrant Layout (Top View)



3.5 Platform Component Placement

Figure 3-8. Component Placement Example Using a 2-DIMM µATX Board



Platform Clock Routing Guidelines 4

To minimize jitter, improve routing, and reduce cost, the 848P chipset-based systems should use a single-chip clock solution; the CK409.

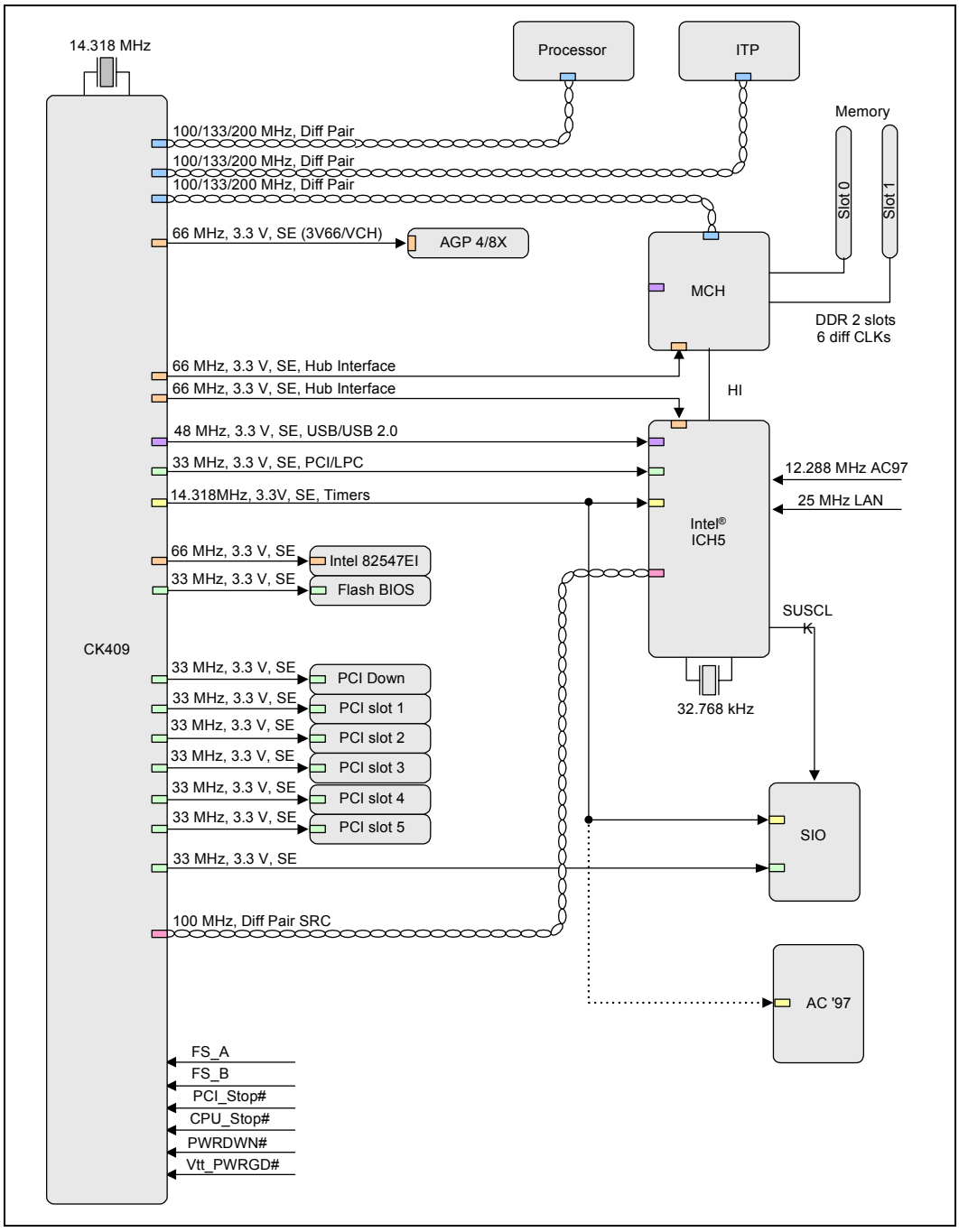
- The CK409 provides three100/133/200 MHz selectable differential outputs pairs for all of the host bus agents, one 100 MHz differential output pair for serial ATA, two 48 MHz clocks, five 66 MHz clocks, ten 33 MHz clocks, and two 14 MHz clocks. Figure 4-1 shows the implementation of the clocks for a typical 848P chipset platform.

For more information on CK409 compliance, refer to the *CK409 Clock Synthesizer/ Driver Specification* document.

Table 4-1. Intel® 848P Chipset Platform Clock Group

Clock Name	Frequency (MHz)	Receiver
Host_CLK	100/133/200	Processor, Debug Port and MCH
CLK66	66	MCH, Intel® ICH5, Intel® 82547EI GbE controller and AGP connector
CLK33_ICH5	33	ICH5
CLK14	14.318	ICH5 and SIO
CLK33	33	PCI Connectors, SIO, and flash BIOS
SRC	100	ICH5-Serial ATA
USBCLK	48	ICH5

Figure 4-1. Intel® 848P Chipset-Based System Clocking Diagram



4.1 HOST_CLK Clock Group

4.1.1 HOST_CLK Clock Topology

The clock synthesizer provides three sets of 100/133/166 MHz differential clock outputs. The differential clocks are driven to the processor, the chipset, and the processors' debug ports as shown in Figure 4-1 and Figure 4-2.

The clock driver differential bus output structure is a "Current Mode Current Steering" output that develops a clock signal by alternately steering a programmable constant current to the external termination resistors "Rt."

The recommended termination for the differential bus clock is a "Shunt Source Termination." Refer to Figure 4-2 for an illustration of this terminology scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors "Rs" provide isolation from the clock driver's output parasitics that would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be selected to match the characteristic impedance of the motherboard, and Rs should be 33 Ω. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

- IREF pin (pin # 52) is connected to ground through a 475 Ω ± 1% resistor – making the IREF 2.32 mA

For more information on CK409 compliance, refer to the *CK409 Clock Synthesizer/ Driver Specification* document.

The CK409 allows for different host clock frequencies. The FS_A and FS_B pins on the CK409 control the output host clock frequencies. See Table 4-2 for different CK409 host clock frequency configurations.

Table 4-2. Host Clock Frequency Select on CK409

FS_A	FS_B	Host Clock Frequency
0	0	100 MHz
1	0	133 MHz
0	1	200 MHz

Figure 4-2. Source Shunt Termination

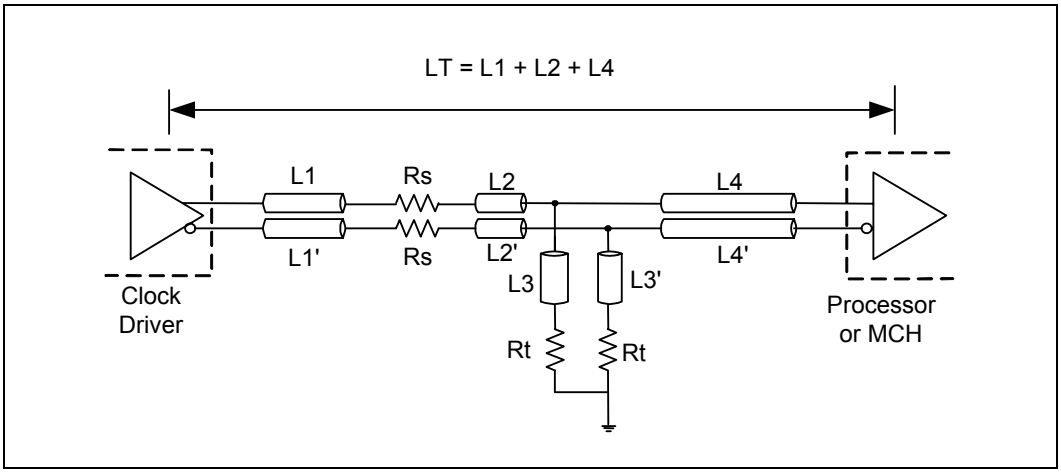


Table 4-3. HOST_CLK[1:0]# Routing Guidelines (Sheet 1 of 2)

Layout Guideline	Value	Illustration	Notes
HOST_CLK Skew between Agents	300 ps total budget: 150 ps for clock driver 150 ps for interconnect	Figure 4-2 and Figure 4-3	1,2,3, 4
Trace Width	5 mils	Figure 4-4	6
Differential Pair Spacing	11 mils	Figure 4-3	5,7
Spacing to Other Traces	25 mils	Figure 4-4	
Serpentine Spacing	Maintain a minimum 25 mils Keep parallel serpentine sections as short as possible. Minimize 90° bends. Make 45° bends if possible.		
Motherboard Impedance – Differential	100 Ω typical		7
Processor Routing Length – L1, L1': Clock Driver to Rs	0.5 inch max	Figure 4-2	9
Processor Routing Length – L2, L2': Rs to Rs-Rt Node	0 – 0.2 inch	Figure 4-2	9
Processor Routing Length – L3, L3': Rs-Rt Node to Rt	0 – 0.2 inch	Figure 4-2	9
Processor Routing Length – L4, L4': Rs-Rt Node to Load	2 – 15 inches	Figure 4-2	
MCH Routing Length – L1, L1': Clock Driver to sS	0.5 inch max	Figure 4-2	9
MCH Routing Length – L2, L2': Rs to Rs-Rt Node	0 – 0.2 inch	Figure 4-2	9
MCH Routing Length – L3, L3': Rs-Rt Node to Rt	0 – 0.2 inch	Figure 4-2	9
MCH Routing Length – L4, L4': Rs-Rt Node to Load	2–15 inches	Figure 4-2	

Table 4-3. HOST_CLK[1:0]# Routing Guidelines (Sheet 2 of 2)

Layout Guideline	Value	Illustration	Notes
Processor to MCH Length Matching (LT)	Host clocks to processor should be 165 mils longer	Figure 4-2	8
HOST_CLK0 – HOST_CLK1 Length Matching	± 10 mils		
Rs Series Termination Value	33 Ω ± 5%	Figure 4-2	
Rt Shunt Termination Value	49.9 Ω ± 1% (for 50 Ω odd mode MB impedance)	Figure 4-2	

NOTES:
1. The skew budget includes clock driver output pair to output pair jitter (differential jitter) and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes clock pairs are routed on multiple routing layers and routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two-bus agents. Measured at the crossing point.
5. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Uniform spacing should be maintained along the entire length of the trace. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network.
6. Set line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack up.
7. The differential impedance of each clock pair is approximately 2*Zsingle-ended*(1–2*Kb) where Kb is the backwards cross-talk coefficient. For the recommended trace spacing, Kb is very small, and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
8. The host clocks to the processor must be 165 mils longer than the host clocks to the MCH.
9. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ringback.

Figure 4-3. Clock Skew As Measured from Agent to Agent

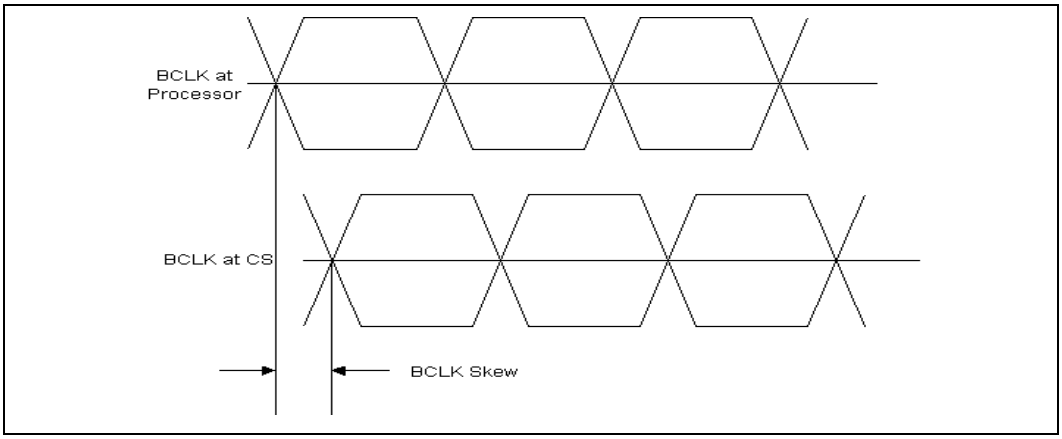
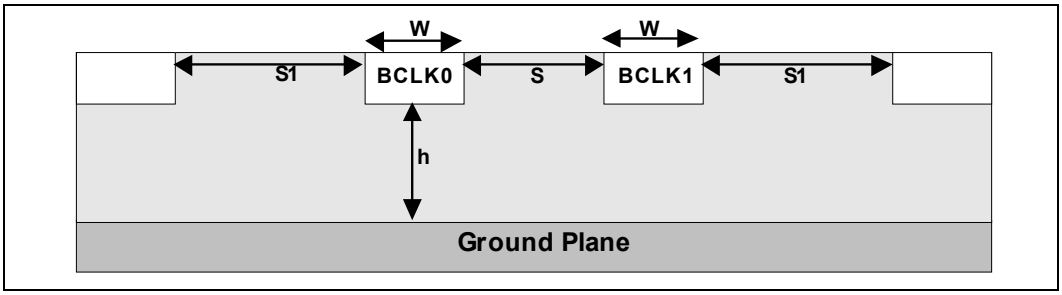


Figure 4-4. Trace Spacing for HOST_CLK Clocks



4.1.2 BCLK General Routing Guidelines

- When routing the 100/133/200 MHz selectable differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.
- If a layer transition is required, make sure to do simulations to determine the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Also, if a layer transition is required then both clock traces must transition layers so that differential routing is maintained.

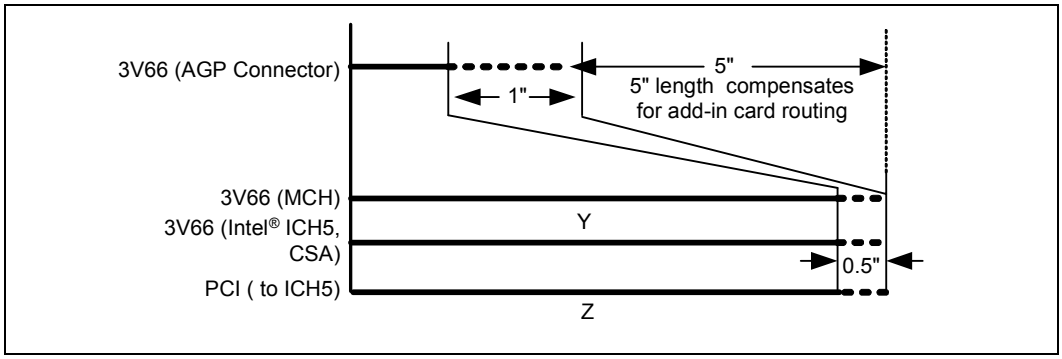
4.2 CLK66 and CLK33 Clock Groups

4.2.1 Length Matching

When routing the 33 MHz and 66 MHz clock group signals, it is important to understand the length matching relationships between all of these signals. Trace length matching is required in each group to help minimize skew and ensure good signal integrity.

4.2.1.1 CLK_66 and Intel® ICH5 CLK_33 Length Matching

Figure 4-5. 66 MHz/33 MHz Clock Relationships



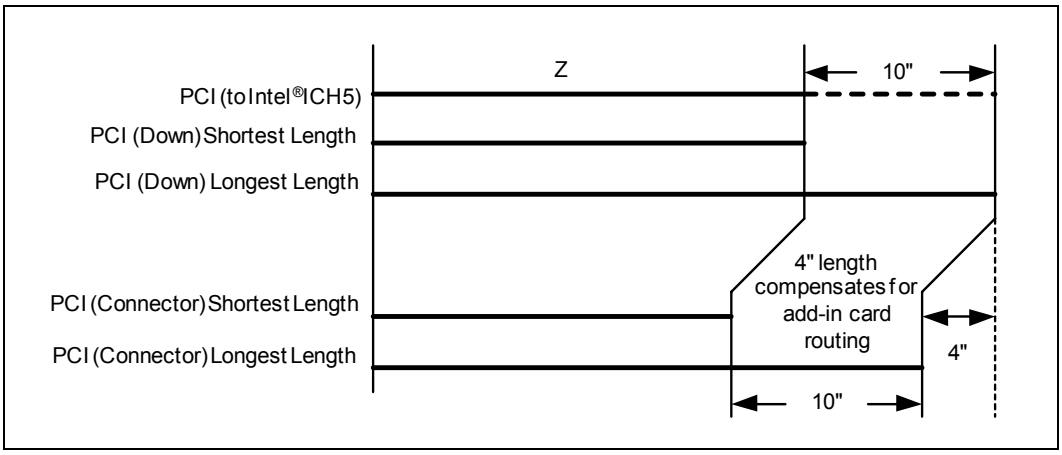
NOTES:
1. Length "Y" denotes the 66 MHz clock length to the MCH and dictates the lengths of the 66 MHz clocks and length "Z" to the ICH5.
2. Length "Z" denotes the 33 MHz clock length to the ICH5 and dictates the lengths of the 33 MHz clocks.

If Y is the length of the 66 MHz clock length to the MCH, then the 66 MHz clocks to CSA, AGP, and ICH5, as well as the 33 MHz clock to the ICH5 (length "Z"), should be length matched to Y ± 0.5 inch. These lengths are strictly dependant on their clock matching relationships to the MCH. AGP add-in card routing (including connector) reduces motherboard trace length by 5 inches, thus maximum routable mismatch to the AGP connector is Y – 5 ± 0.5 inch. In addition, designers are allowed up to an additional inch of routing flexibility to meet AGP timing specifications.

Thus, if Y is 9 inches, then CLK_66 to CSA can be anywhere between 8.5 to 9.5 inches, while CLK_66 to AGP is routed between 3.5 to 4.5 inches. This minimum length may decrease an additional inch to 2.5 inches based on simulation results.

4.2.1.2 CLK_33 Length Matching

Figure 4-6. 33 MHz Clock Relationships



NOTE: Length "Z" denotes the 33 MHz clock length to the ICH5 and dictates the lengths of the 33 MHz clocks.

The 33 MHz clock group signals should be length matched up to a maximum of 10 inches. Length "Z" denotes the 33 MHz clock to the ICH5 and will dictate the length of all other 33 MHz clock signals. PCI add-in card routing and connector routing reduces the total allowable motherboard trace length by 4 inches. If the CLK_33 length to the ICH5 is 17 inches, then the shortest allowable routed motherboard length to any PCI slot is 17– 10 – 4 = 3 inches. Likewise, if the CLK_33 length to the ICH5 is 5 inches trace, then the longest allowable routed length to any PCI slot is 5+ 10– 4 = 11 inches.

4.2.2 CLK_66 Clock Group

In the CLK66 clock group, the driver is the clock synthesizer 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the MCH, ICH5, the AGP connector, and the Intel 82547EI GbE controller.

Figure 4-7. Topology for CLK66 to AGP Connector

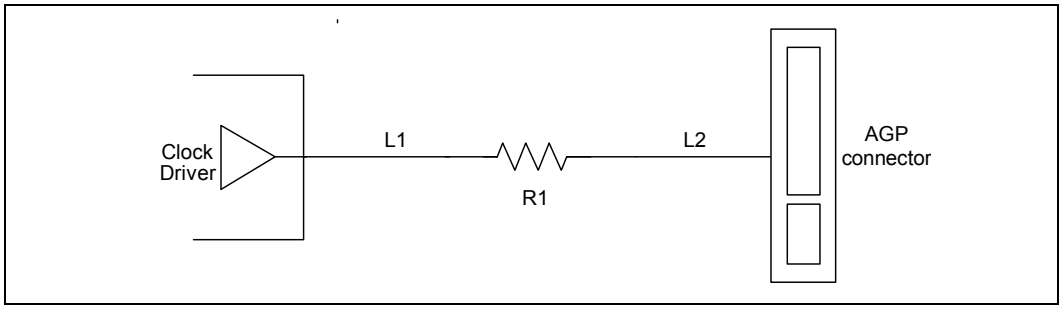


Figure 4-8. Topology for CLK66 to MCH, Intel® ICH5, and Intel® 82647EI GbE Controller

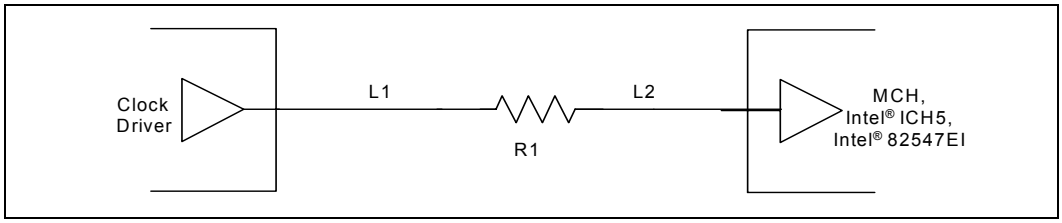


Table 4-4. CLK66 Routing Guidelines for CLK66 to MCH, Intel® ICH5, Intel® 82647EI GbE Controller, and AGP Connector

Parameters	Routing Guidelines	Notes
Clock Group	CLK66	
Topology	Point-to-Point	
Reference Plane	Ground referenced (contiguous over entire length)	
Characteristic Trace Impedance (Z_0)	60 Ω ± 15%	
Trace Width	5 mils	
Trace Spacing	10 mils	
Resistor	33 Ω ± 5%	
AGP Connector, MCH, Intel® ICH5, CSA Trace Length – L1	0 to 0.5 inch	
Clock Driver to MCH – L2	Y; 2 inches to 20 inches	1
Clock Driver to ICH5, GbE, and CLK_33 (Length "Z") Trace Length – L2	Y ± (0 to 0.5 inch); max length is 20 inches	1, 2
Clock Driver to AGP Connector Trace Length – L2	Y – 5 ± (0 to 0.5 inch); additional inch of routing flexibility; max length is 20 inches	1, 3

NOTES:
1. Length "Y" is the distance from the 66-MHz clock driver to the ICH5 66-MHz input buffer. Refer to Figure 4-5. "Y" can be 2 inches to 20 inches long.
2. Length "Z" is the distance from the 33 MHz clock driver to the ICH5 33 MHz input buffer. Refer to Figure 4-5. "Z" can be 2 inches to 20 inches long.
3. 5 inches is incorporated in the AGP add-in card and connector routing. Up to 1 inch of routing flexibility is added to meet timing specifications.

4.2.3 CLK_33 Clock Group

For the CLK33 clock group, the driver is the clock synthesizer 33 MHz clock output buffer and the receiver is the 33 MHz clock input buffer at the various down devices and the PCI slots.

Figure 4-9. Topology for CLK33 to Down Devices

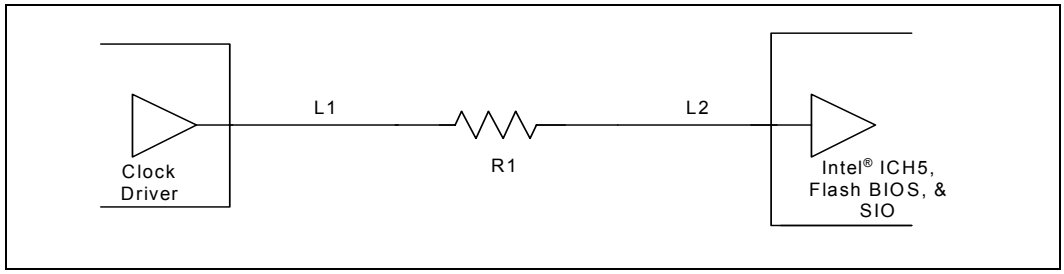


Figure 4-10. Topology for CLK33 to PCI Slot

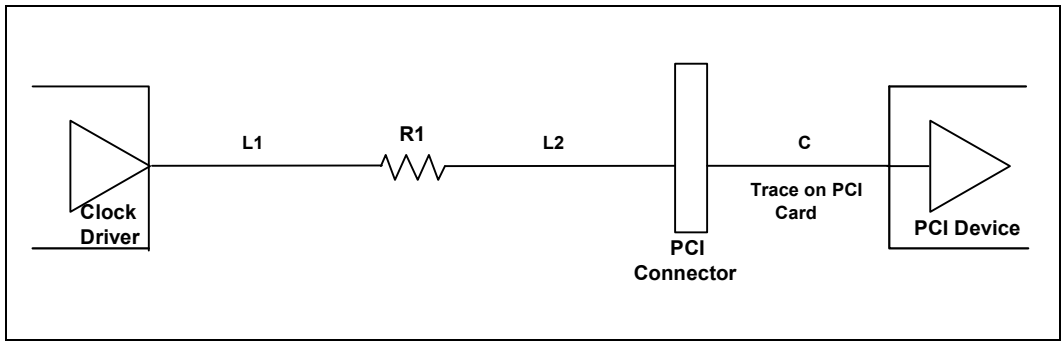


Table 4-5. CLK33 Routing Guidelines to Intel® ICH5, Flash BIOS, SIO, and PCI Slots

Parameter	Routing Guidelines	Notes
Clock Group	CLK33	
Topology	Point-to-Point	
Reference Plane	Ground referenced (contiguous over entire length)	
Characteristic Trace Impedance (Z_0)	60 Ω ± 15%	
Trace Width	5 mils	
Trace Spacing	10 mils	
Intel® ICH5, Flash BIOS, SIO, PCI slots Trace Length – L1	0 to 0.5 inch	
ICH5 – L2	Z; 2 inches to 20 inches	1
Flash BIOS, SIO Trace Length– L2	Z ± (0 to 10 inches); max length is 20 inches	1
PCI slots Trace Length – L2	Z – 4 ± (0 to 10 inches); max length is 20 inches	1, 2
Resistor	R1 = 33 Ω ± 5%	

NOTES:
1. Refer to Figure 4-12 for length of "Z"
2. Four inches is incorporated in the PCI add-in card and connector routing and is immediately subtracted from routing length.

4.2.3.1 Sharing 33 MHz Clocks

In some cases the motherboard designer may have a need to share one PCI 33 MHz clock between two PCI down devices. In this case the driver is the clock synthesizer 33 MHz clock output buffer, and the receivers are the 33 MHz clock input buffers of two, separate PCI down devices.

Figure 4-11. Topology for Sharing CLK33 between Two PCI Down Devices

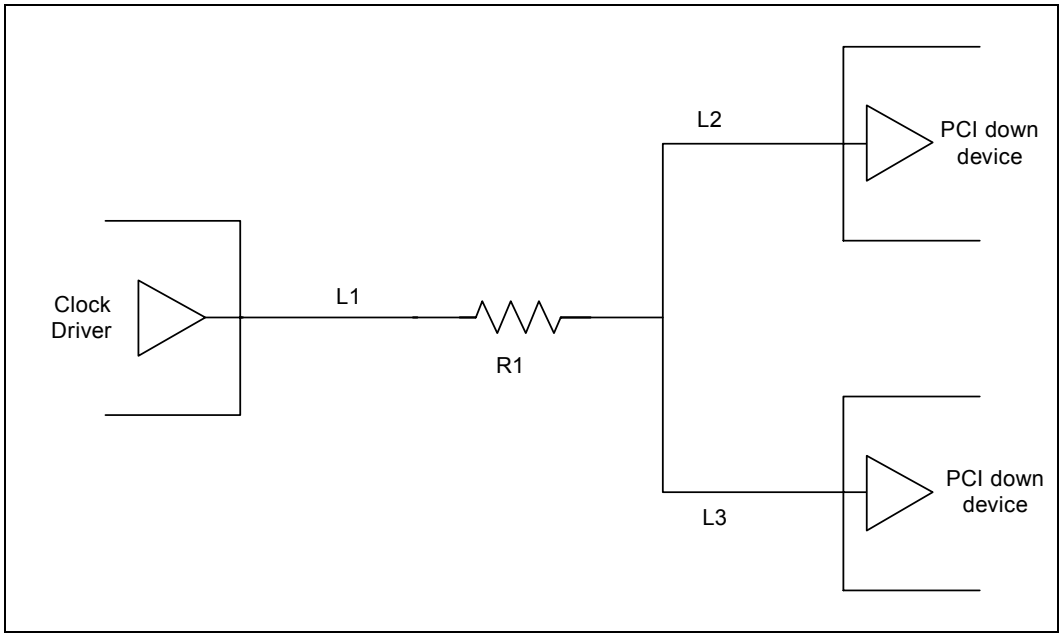


Table 4-6. CLK33 Routing Guidelines for Sharing CLK66 between Two PCI Down Devices

Parameters	Routing Guidelines
Clock Group	CLK66
Topology	“T”
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	60 Ω ± 15%
Trace Width	5 mils
Trace spacing	10 mils
Resistor	10 Ω ± 5%
PCI down devices– L1	0 to 0.5 inch; max length is 20 inches
PCI down devices – L2 and L3	Z ± (0 to 7 inches); max length is 20 inches. L2 and L3 should be length matched to within 250 mils.

NOTES:
1. Length “Z” is the distance from the 33 MHz clock driver to the ICH5, 33 MHz input buffer. “Z” can be 2 inches to 20 inches long.

4.3 CLK14 Clock Group

The driver in the CLK14 clock group is the clock synthesizer 14.318 MHz clock output buffer and the receiver is the 14.318 MHz clock input buffer at the ICH5 and SIO.

Figure 4-12. Topology for CLK14

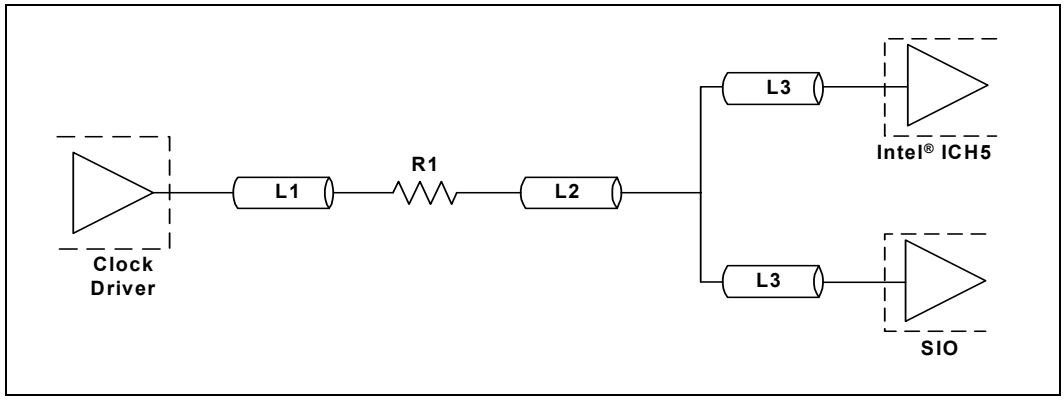


Table 4-7. CLK14 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK14
Topology	Balanced T Topology
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	60 Ω ± 15%
Trace Width	5 mils
Trace Spacing	10 mils
Trace Length – L1	0 to 0.5 inch
Trace Length – L2	0 to 12 inches
Trace Length – L3	0 to 6 inches
CLK14 total length (L1+L2+L3)	(L1+L2+L3) to ICH5 must be within 500 mils of (L1+L2+L3) to SIO
Resistor	10 Ω ± 5%
Skew Requirements	None

4.4 USB Clock

For the USBCLK clock group, the driver is the clock synthesizer USB clock output buffer, and the receiver is the USB clock input buffer at the ICH5. Note that this clocks are asynchronous to any other clock on the board.

Figure 4-13. Topology for USBCLK

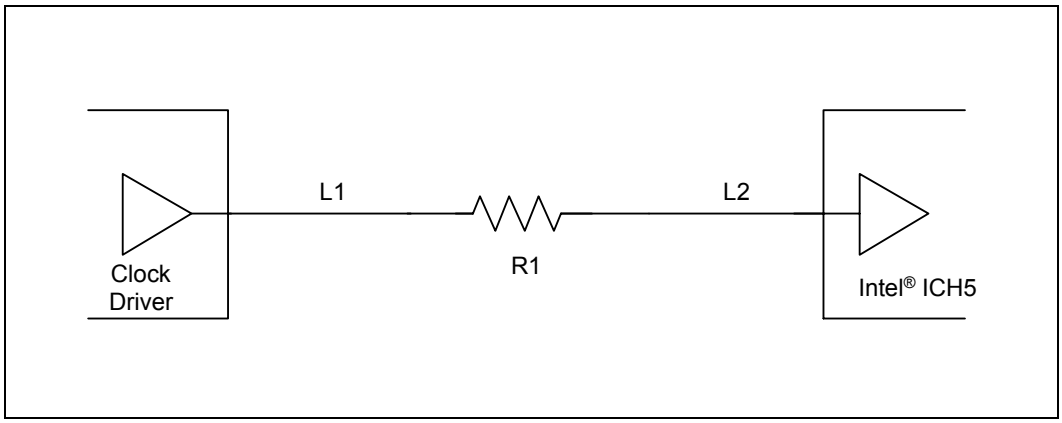


Table 4-8. USBCLK Routing Guidelines

Parameter	Routing Guideline
Clock Group	USBCLK
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	60 Ω ± 15%
Trace Width	5 mils
Trace Spacing	20 mils
Trace Length – L1	0 to 0.5 inch
Trace Length – L2	2 to 20 inches
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	None – USBCLK is asynchronous to any other clock on the board
Maximum via Count	2

4.5 SRC Clock Group

4.5.1 SRC Clock Topology

The clock synthesizer provides one set of 100 MHz differential clock outputs. The differential clocks are driven to the ICH5 for serial-ATA as shown in Figure 4-1.

The clock driver differential bus output structure is a “Current Mode Current Steering” output which develops a clock signal by alternately steering a programmable constant current to the external termination resistors “Rt.”

The recommended termination for the differential bus clock is a “Shunt Source Termination.” Refer to Figure 4-14 for an illustration of this terminology scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors “Rs” provide isolation from the clock driver’s output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be 49 Ω and Rs should be 33 Ω. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

Figure 4-14. Source Shunt Termination

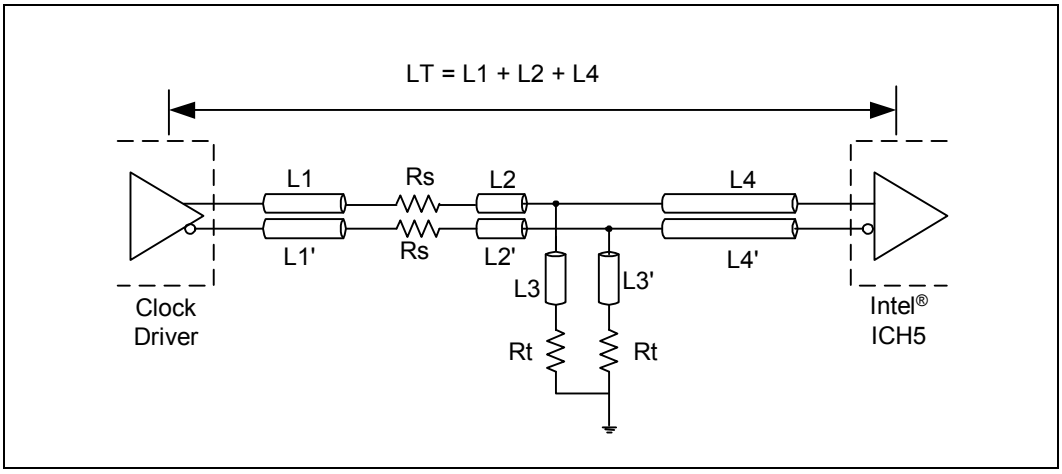


Table 4-9. SCR/SCR# Routing Guidelines (Sheet 1 of 2)

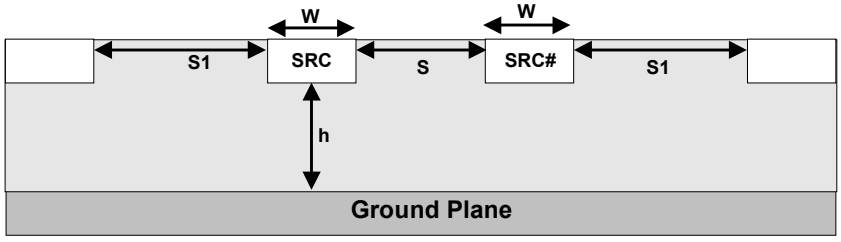
Layout Guideline	Value	Figures	Notes
Trace Width	5 mil	Figure 4-15	
Differential Pair Spacing	11 mils	Figure 4-15	1,2,3
Spacing to Other Traces	25 mils	Figure 4-15	
Serpentine Spacing	Maintain a minimum 25 mils. Keep parallel serpentine sections as short as possible. Minimize 90° bends. Make 45° bends, if possible.		
Motherboard Impedance – Differential	100 Ω typical		4
Routing Length – L1, L1’: Clock Driver to Rs	0.5 inch max	Figure 4-14	7,8

Table 4-9. SCR/SCR# Routing Guidelines (Sheet 2 of 2)

Layout Guideline	Value	Figures	Notes
Routing Length – L2, L2': Rs to Rs-Rt Node	0 – 0.2 inch	Figure 4-14	7,8
Routing Length – L3, L3': Rs-Rt Node to Rt	0 – 0.2 inch	Figure 4-14	7,8
Routing Length – L4, L4': Rs-Rt Node to Load	2 – 15 inches	Figure 4-14	
SCR – SCR# Length Matching	± 10 mils		
Rs Series Termination Value	33 Ω ± 5%	Figure 4-14	5
Rt Shunt Termination Value	49.9 Ω± 1% (for 50 Ω odd mode MB impedance)	Figure 4-14	6

NOTES:
1. Edge-to-edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
2. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network
3. Set line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack up.
4. The differential impedance of each clock pair is approximately 2*Zsingle-ended*(1–2*Kb) where Kb is the backwards cross-talk coefficient. For the recommended trace spacing, Kb is very small, and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
5. Rs values of 33 Ω have been shown to effectively force reflected signals to properly terminate through the source termination by isolating the line from clock driver parasitic capacitances. Refer to the clock synthesizer specification for further clarification.
6. Rt shunt termination value should match the motherboard impedance.
7. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ringback.
8. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in Er and the impedance variations due to physical tolerances of circuit board material.

Figure 4-15. Trace Spacing for SRC Clocks



4.5.2 SRC General Routing Guidelines

- When routing the 100 MHz differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.
- If a layer transition is required, make sure skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Do not place vias between adjacent complementary clock traces, and avoid differential vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

4.6 Clock Driver Decoupling

- For **all** power connection to planes, decoupling caps and vias, the **maximum** trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance.
- The VSS pins should not be connected directly to the VSS side of the caps. They should be connected to the ground flood under the part which is viaed to the ground plane in order to avoid VDD glitches propagating out, getting coupled through the decoupling caps to the VSS pins. This method has been shown to provide the best clock performance.
- The ground flood should be viaed through the ground plane with no less than 12–16 vias under the part. It should be well connected.
- For all power connections, heavy duty and/or dual vias should be used.
- It is imperative that the standard signal vias and small traces not be used for connecting decoupling caps and ground floods to the power or ground planes.

4.6.1 VDD Plane Filtering

The VDD decoupling requirements for a CK409-compliant clock synthesizer are as follows:

- One, 300 Ω (100 MHz) ferrite bead is recommended for the VDD plane
- One 10 µF bulk decoupling capacitor placed near the clock chip is recommended for the VDD plane. Two, 4.7 µF capacitors can also be used in place of the one 10 µF bulk decoupling capacitor.
- Seven 0.1 µF high-frequency decoupling capacitors should be placed as close to each VDD pin as possible.

4.6.2 VDDA Plane Filtering

The VDDA decoupling requirements for a CK409-compliant clock synthesizer are as follows:

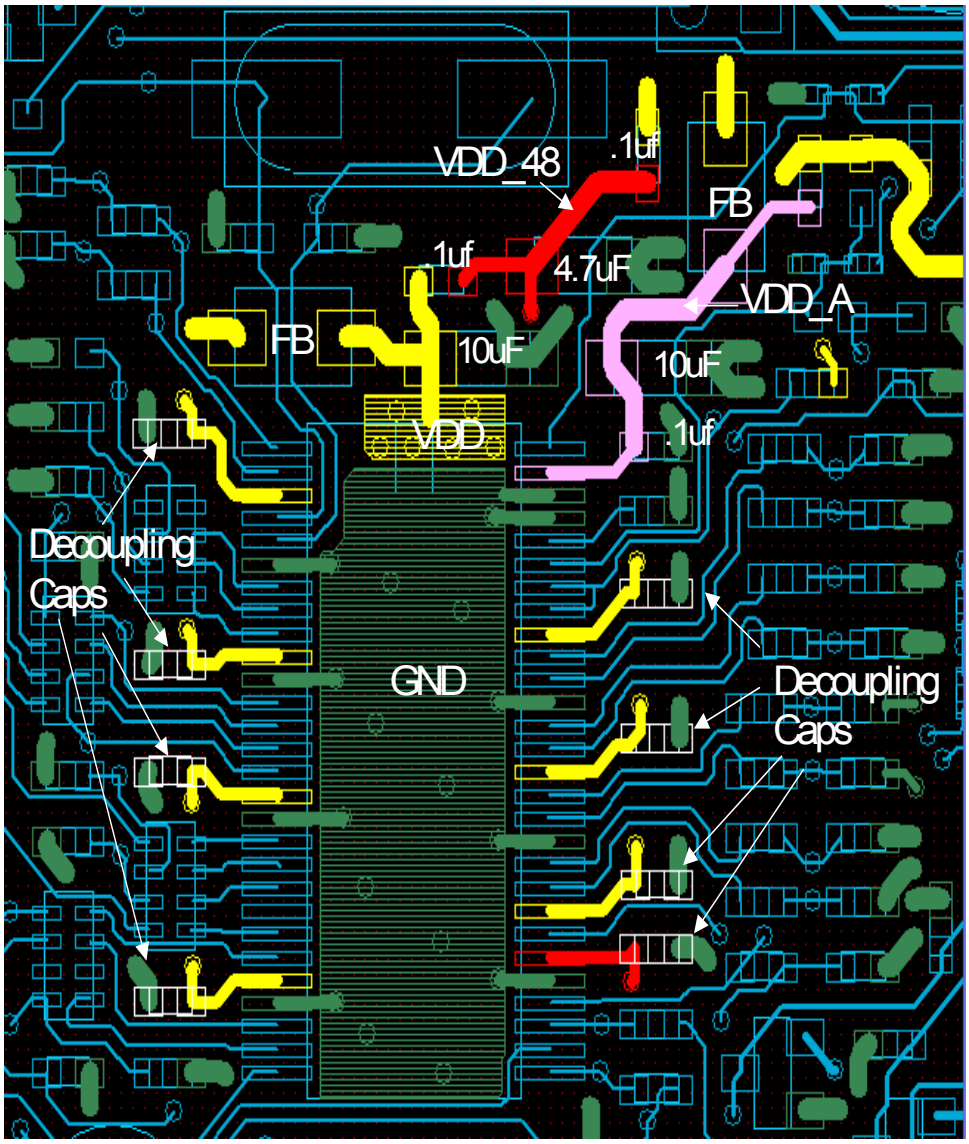
- One 300 Ω (100 MHz) ferrite bead is recommended for the VDDA plane
- One 10 µF bulk decoupling capacitor placed near the VDDA pin is recommended for the VDDA plane. Two 4.7 µF capacitors can also be used in place of the one 10 µF bulk decoupling capacitor.
- One 0.1 µF high-frequency decoupling capacitor should be placed as close to each VDDA pin as possible.

4.6.3 VDD_48 Plane Filtering

The VDD _48 decoupling requirements for a CK409-compliant clock synthesizer are as follows:

- One 5 Ω series resistor is recommended for the VDD _48 plane
- One 4.7 µF bulk decoupling capacitor placed near the VDD _48 pin is recommended for the VDD _48 plane.
- One, 0.1 µF high-frequency decoupling capacitor should be placed as close to the VDD_48 pin as possible.

Figure 4-16. Decoupling Capacitors Placement and Connectivity



4.7 EMI Constraints

Clocks are a significant contributor to EMI. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to the VSS reference plane only.

Front Side Bus (FSB) 5

5.1 General Topologies and Layout Guidelines

This section covers the front side bus source synchronous (data, address, and associated strobes) and common clock signal routing for a Pentium 4 processor with 512-KB L2 cache on 0.13 micron process or the Pentium 4 processor on 90 nm process in an 848P chipset-based platform. Table 5-1 lists the signals and their corresponding signal types.

Table 5-1. Frontside Bus Signal Groups

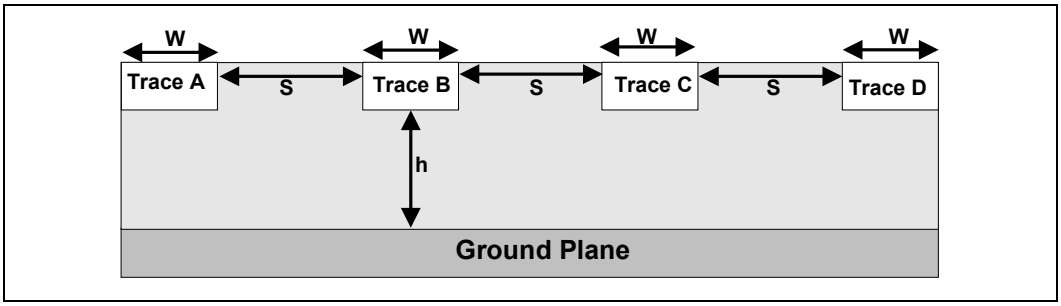
Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, RESET#[3, 5], RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	AP[1:0]#, ADS#, BINIT#, BNR#, BPM[5:0]#[3, 5], BR0#[3], DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#
AGTL+ Source Synchronous I/O	Synchronous to associated strobe	**Signals** / **Associated Strobe** REQ[4:0]#, A[16:3]#[4] — ADSTB0# A[35:17]#[4] — ADSTB1# D[15:0]#, DBI0# — DSTBP0#, DSTBN0# D[31:16]#, DBI1# — DSTBP1#, DSTBN1# D[47:32]#, DBI2# — DSTBP2#, DSTBN2# D[63:48]#, DBI3# — DSTBP3#, DSTBN3#
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
Asynchronous GTL+ Input[3]		A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, SLP#, STPCLK#
Asynchronous GTL+ Output[3]		FERR#, IERR#, THERMTRIP#[5]
Asynchronous GTL+ Input/Output		PROCHOT#
TAP Input[3]	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output[3]	Synchronous to TCK	TDO[5]
FSB Clock	Clock	BCLK[1:0], ITP_CLK[1:0][2]
Power/Other		VCC, VCCA, VCCIOPLL, VID[5:0], VSS, VSSA, GTLREF[3:0], COMP[1:0], RESERVED, TESTHI[12:0], THERMDA, THERMDC, VCC_SENSE, VSS_SENSE, VCCVID, VCCVIDLB, BSEL[1:0], SKTOCC#, DBR#[2], VIDPWRGD, BOOTSELECT, OPTIMIZED/COMPAT#[3] (Intel® Pentium® 4 Processor on 90 nm process signal), IMPSEL[3] (Intel® Pentium® 4 processor 0.13 micron process signal) PWRGOOD[3, 5]

NOTES:
1. Refer to the processor datasheet for signal descriptions.
2. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
3. These signal groups are not terminated by the processor. Refer to the processor debug port design guide, and Section 5.1.6 for termination requirements and further details.
4. The value of these pins during the active-to-inactive edge of RESET# defines the processor configuration options. See the processor datasheet for details.
5. These signals do not have R_L termination on die.

5.1.1 Trace Spacing Rules

The spacing rules are based on board stack-up and dielectric thickness, not on trace width. A 3:1 spacing rule corresponds to the air gap (distance S) between traces and must be 3x the distance from the trace to the ground plane (distance h). For instance, if the dielectric thickness was 4.1 mils, and the trace space guidelines calls for 3:1 spacing, the air gap between traces must be 12.3 mils.

Figure 5-1. Spacing Diagram



5.1.2 Signal Groups

This section covers the AGTL+ FSB 1X, 2X, and 4X signals as well as their associated strobe pairs.

Table 5-2. 1X, 2X and 4X Signal Groups

1X	2X Group	4X Group
BPRI#,DEFER#,RS[2:0]#, TRDY#,ADS#,BNR#,DBSY,DRDY#, HIT#,HITM#,LOCK#	A[31:3]#, REQ[4:0]#, ADSTB[1:0]#	D[63:0]#, DSTBP[3:0]#, DSTBN[3:0]#,DBI[3:0]#

Table 5-3. Address and Data, and Associated Strobe Pairs

Data/Address Group	Associated Strobes
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#
D[47:32]#, DBI2#	DSTBP2#, DSTBN2#
D[31:16]#, DBI1#	DSTBP1#, DSTBN1#
D[15:0]#, DBI0#	DSTBP0#, DSTBN0#
A[31:17]#	ASTB1#
A[16:3]#, REQ[4:0]#	ASTB0#

5.1.3 Motherboard Layout Rules for AGTL+ Signals

The following topologies and layout guidelines are preliminary and are subject to change. These guidelines are derived from simulations with the processor and 848P chipset package models. All lengths are pin-to-pin lengths, but length matching must be pad-to-pad.

5.1.3.1 4X Routing Guidelines

Table 5-4. 4X Routing Guidelines

Signal Name	Spacing	Length	Referencing	Topology	Impedance	Matching	Notes
D[63:0]#	3:1	2.5” to 6”	VSS	1	60 Ω ± 15%	± 25 mils	2,3,4,5
DSTBP[3:0]#	4:1	2.5” to 6”	VSS	1	60 Ω ± 15%	± 25 mils	1,2,3,4
DSTBN[3:0]#	4:1	2.5” to 6”	VSS	1	60 Ω ± 15%	± 25 mils	1,2,3,4
DBI[3:0]#	3:1	2.5” to 6”	VSS	1	60 Ω ± 15%	± 25 mils	2,3,5

NOTE:
1. HDSTBP[3:0]# and HDSTBN[3:0]# must **not** be routed adjacent to each other and have 4:1 spacing.
2. All signal groups within the 4X data group must be routed on the same layer.
3. Length matching must include motherboard compensation for MCH and processor package trace lengths.
4. Strobe length matching: Length_DSTBPx = Length_DSTBNx ± 25 mils.
5. Data to strobe length matching: Length_data = (LengthDSTBPx + Length_DSTBNx)/2 ± 25.

5.1.3.2 2X Routing Guidelines

Table 5-5. 2X Routing Guidelines

Signal Name	Spacing	Length	Referencing	Topology	Impedance	Matching	Notes
A[31:3]#	3:1	3” to 10”	VSS	1	60 Ω ± 15%	± 100 mils	2,3
ADSTB[1:0]#	4:1	3” to 10”	VSS	1	60 Ω ± 15%	± 100 mils	1,2,3
REQ[4:0]#	3:1	3” to 10”	VSS	1	60 Ω ± 15%	± 100 mils	2,3

NOTE:
1. ADSTB[1:0]# need to be routed 4:1 from everything.
2. Length matching must include motherboard compensation for package trace lengths.
3. Address to strobe length matching: Length_address = LengthADSTB ± 100.

5.1.3.3 1X Routing Guidelines

Table 5-6. 1X Routing Guidelines

Signal Name	Spacing	Length	Referencing	Topology	Impedance	Notes
BPRI#	3:1	3” to 8”	VSS	1	60 Ω ± 15%	1,2
DEFER#	3:1	3” to 8”	VSS	1	60 Ω ± 15%	1,2
RS[2:0]#	3:1	3” to 8”	VSS	1	60 Ω ± 15%	1,2
TRDY#	3:1	3” to 8”	VSS	1	60 Ω ± 15%	1,2
ADS#	3:1	3” to 8”	VSS	1	60 Ω ± 15%	1,2
BNR#	3:1	3” to 8”	VSS	1	60 Ω ± 15%	1,2
DBSY#	3:1	3” to 8”	VSS	1	60 Ω ± 15%	1,2
DRDY#	3:1	3” to 8”	VSS	1	60 Ω ± 15%	1,2
HIT#	3:1	3” to 8”	VSS	1	60 Ω ± 15%	1,2
HITM#	3:1	3” to 8”	VSS	1	60 Ω ± 15%	1,2
LOCK#	3:1	3” to 8”	VSS	1	60 Ω ± 15%	1,2

NOTE:
1. 3:1 spacing is the minimum requirement, if 4:1 spacing is achievable, 4:1 spacing is preferred.
2. For routes 7 inches to 8 inches, 4:1 spacing is required.

5.1.3.4 Ground Referencing

It is strongly recommended that AGTL+ signals be routed on a signal layer that is next to the ground layer (referenced to ground). It is important to provide effective signal return paths with low inductance. The best routing is directly adjacent to a solid ground plane with no splits or cuts.

Reference Plane Splits

Splits in reference planes disrupt signal return paths and increase overshoot, undershoot, and ring-back due to significantly increased inductance. This is very hard to predict and suppress; thus, such plane splits under AGTL+ signals should be avoided.

5.1.4 Motherboard Layout Rules for Async AGTL+ Signals

For all asynchronous AGTL+ signals, routing can be done on any layer or combination of layers. Table 5-7 provides insight for routing these signals, but Section 5.1.6 further details the routing topologies and layout requirements.

Table 5-7. Routing Guidelines for Asynchronous AGTL+ Signals

Signal	Impedance	Spacing	Trace Width	Topology
THERMTRIP#	60 Ω ± 15%	7 mils	5 mils	2
FERR#	60 Ω ± 15%	7 mils	5 mils	2
A20M#	60 Ω ± 15%	7 mils	5 mils	3
IGNNE#	60 Ω ± 15%	7 mils	5 mils	3
SMI#	60 Ω ± 15%	7 mils	5 mils	3
SLP#	60 Ω ± 15%	7 mils	5 mils	3
STPCLK#	60 Ω ± 15%	7 mils	5 mils	3
LINT[1:0]	60 Ω ± 15%	7 mils	5 mils	3
IERR#	60 Ω ± 15%	7 mils	5 mils	4
BR0#	60 Ω ± 15%	13 mils	5 mils	5
RESET#	60 Ω ± 15%	13 mils	5 mils	5
INIT#	60 Ω ± 15%	7 mils[1]	5 mils	6
PWRGOOD	60 Ω ± 15%	13 mils	5 mils	7
PROCHOT#	60 Ω ± 15%	7 mils	5 mils	8
TESTHI	60 Ω ± 15%	7 mils	5 mils	9
COMP[1:0]	60 Ω ± 15%	13 mils	5 mils	10
BOOTSELECT	60 Ω ± 15%	7 mils	5 mils	11
RESERVED	NA	NA	NA	12
OPTIMIZED/COMPAT# (Intel® Pentium® 4 processor on 90 nm process signal) IMPSEL (Intel® Pentium® 4 processor on 0.13 micron process signal)	NA	NA	NA	13
RSP#	NA	NA	NA	13

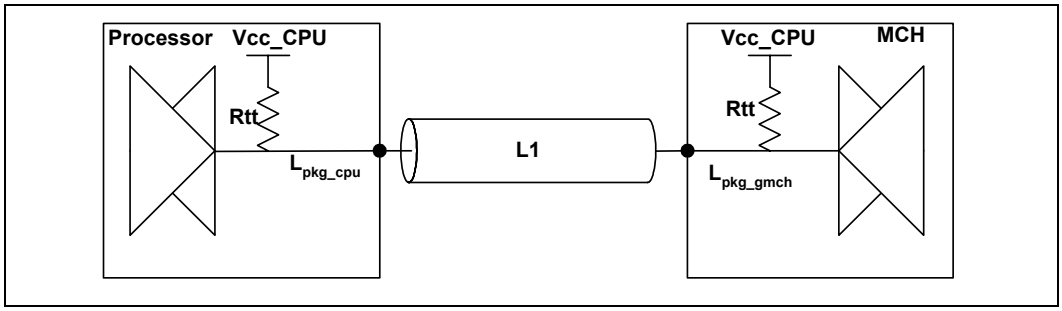
NOTE:
1. It is recommended to use 7-mil spacing around the INIT# signal. If 5-mil spacing is used, the total portion routed at this width cannot exceed 8 inches.

5.1.5 AGTL+ Layout Topologies

5.1.5.1 Topology 1

Topology 1 requires that the signals be routed directly from the processor to the chipset. Both the processor and the chipset have on-die termination (ODT), which removes the need for termination resistors on the motherboard. Thus, the signal is dual-end terminated. The allowable break-in and breakout region for AGTL+ signals is 500 mils at 5-mil traces with 5-mil separation.

Figure 5-2. Topology 1



5.1.6 Non AGTL+ Topologies

5.1.6.1 Topology 2: THERMTRIP# and FERR#

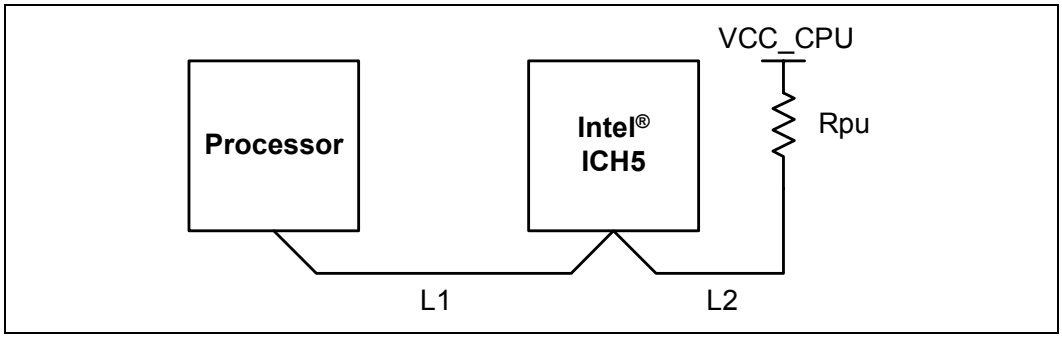
These signals adhere to the following routing and layout recommendations. Figure 5-3 illustrates the recommended topology. If THERMTRIP# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

Table 5-8. Layout Recommendations for FERR# and THERMTRIP# - Topology 3

Trace Z_0	Trace Spacing	L1	L2	Rpu
60Ω ± 15%	7 mils	1 inch to 12 inches	3 inches maximum	62 Ω ± 5%

NOTE:
1. THERMTRIP# can be routed next to FERR# with 5-mil spacing for up to 17 inches.
2. THERMTRIP# or FERR# cannot be routed next to any other signal for more than 8 inches at 7-mil spacing.

Figure 5-3. Routing Illustration for FERR# and THERMTRIP#



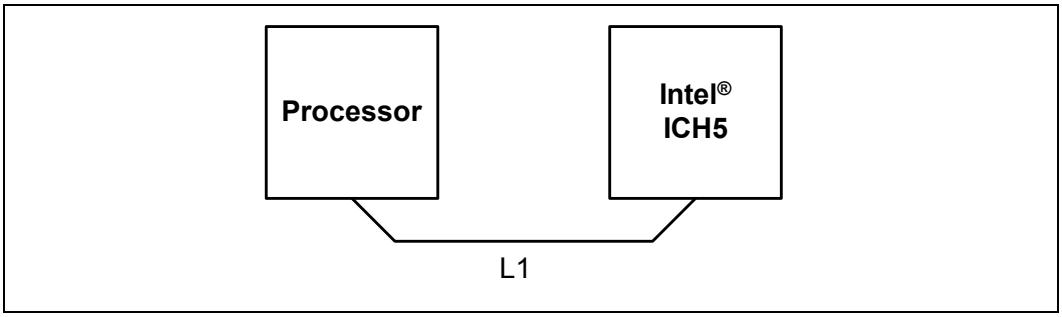
5.1.6.2 Topology 3: A20M#, IGNNE#, SMI#, SLP#, STPCLK#, LINT[1:0]

These signals adhere to the following routing and layout recommendations. Figure 5-4 illustrates the recommended topology.

Table 5-9. Layout Recommendations for Miscellaneous Signals – Topology 4

Trace Z_0	Trace Spacing	L1
60Ω ± 15%	7 mils	17 inches maximum

Figure 5-4. Routing Illustration for A20M#, IGNNE#, SMI#, SLP#, STPCLK#, and LINT[1:0]



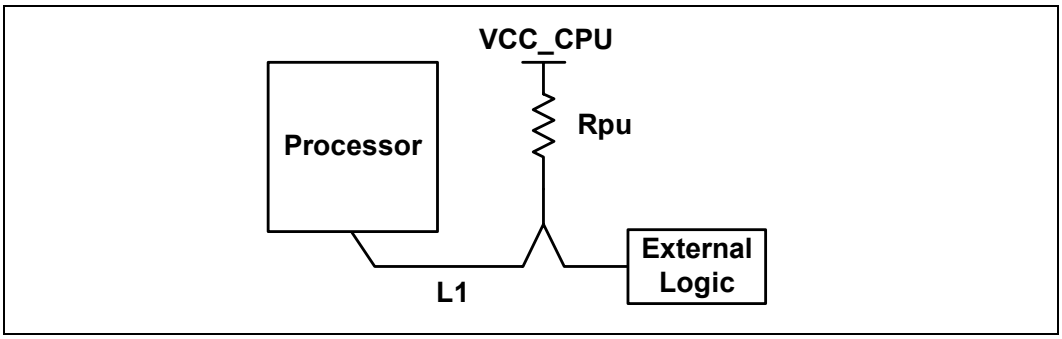
5.1.6.3 Topology 4: IERR#

The IERR# signal does not have on-die termination and must be terminated if it is used. If the signal is not used, it can be left as a no connect. Figure 5-5 illustrates the recommended topology if the pin is used.

Table 5-10. Layout Recommendations for IERR#

Trace Z_0	Trace Spacing	L1	Rpu
60 Ω ± 15%	7 mils	1 inch maximum	62 Ω ± 5%

Figure 5-5. Routing Illustration for IERR



5.1.6.4 Topology 5: RESET# and BR0#

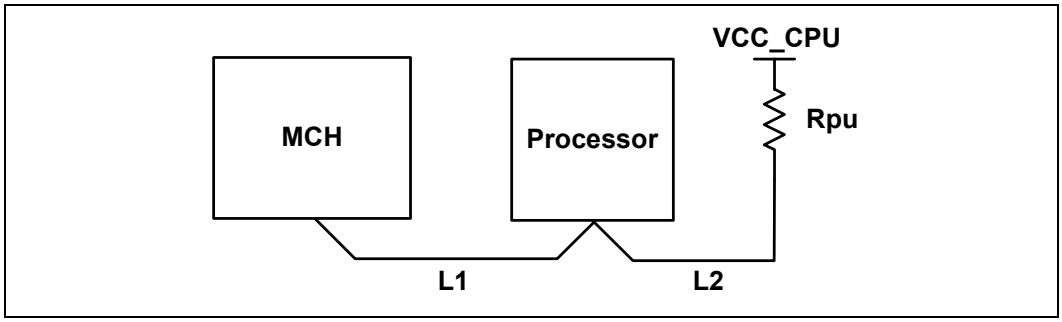
Since the processor does not have on-die termination on the RESET# or BR0# signals, it is necessary to terminate using discrete components on the system board. Connect the signals between the MCH and the processor as shown in Figure 5-6.

Table 5-11. Layout Recommendations for RESET# and BR0#

Pin Name	Trace Z_0	Trace Spacing	L1	L2	Rpu
RESET#	60 Ω ± 15%	13 mils	2” to 10”	1” to 2”	62 Ω ± 5%
BR0#	60 Ω ± 15%	13 mils	2” to 10”	1” to 2”	200 Ω ±5%

NOTES:
1. BR0# can be routed with 7-mil spacing for up to 8 inches.

Figure 5-6. Routing Illustration for RESET# and BR0#



5.1.6.5 Topology 6: INIT#

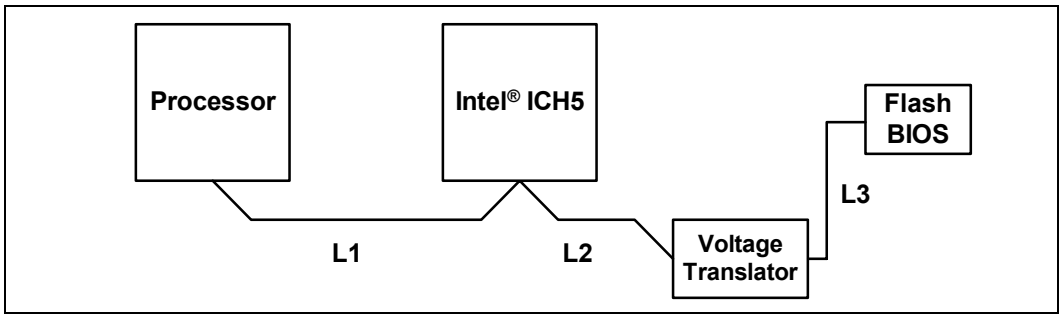
The INIT# signal adheres to the following routing and layout recommendations. Figure 5-7 illustrates the recommended topology.

Table 5-12. Layout Recommendations For INIT#

Trace Z_0	Trace Spacing	L1	L2	L3
60Ω ± 15%	7 mils[1]	17 inches maximum	2 inches maximum	10 inches maximum

NOTE:
1. It is recommended to use 7-mil spacing around the INIT# signal. If 5-mil spacing is used, the total portion routed at this width cannot exceed 8 inches.

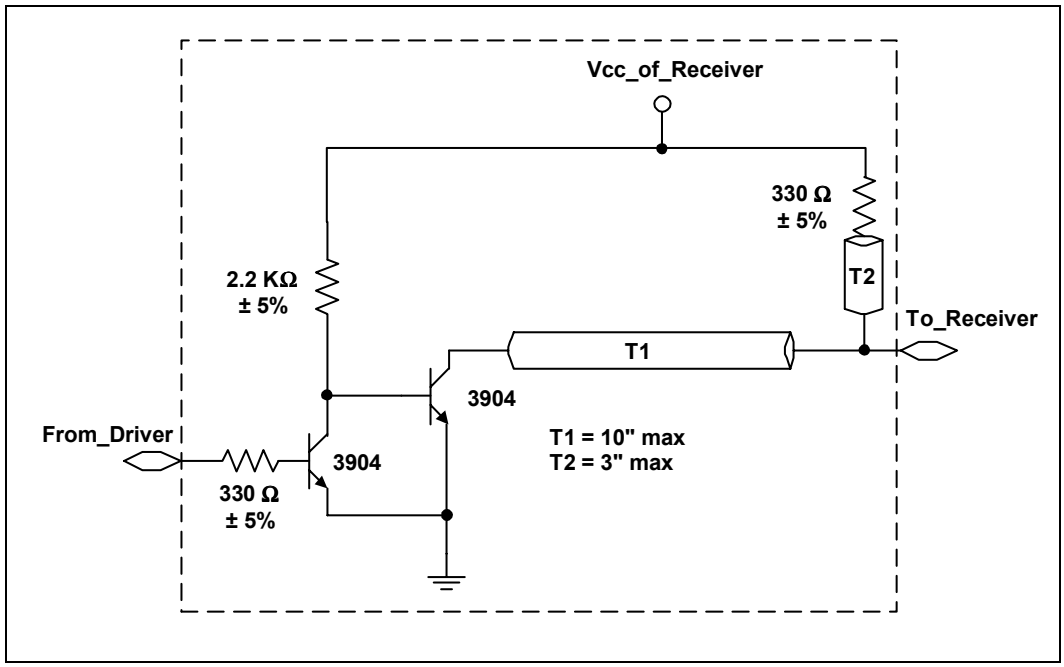
Figure 5-7. INIT# Topology



NOTE: External logic is represented by Figure 5-8.

Level shifting is required for the INIT# signals to the flash BIOS to meet the input logic levels of the flash BIOS. Figure 5-8 illustrates one method of implementing this function.

Figure 5-8. Voltage Translation of INIT#



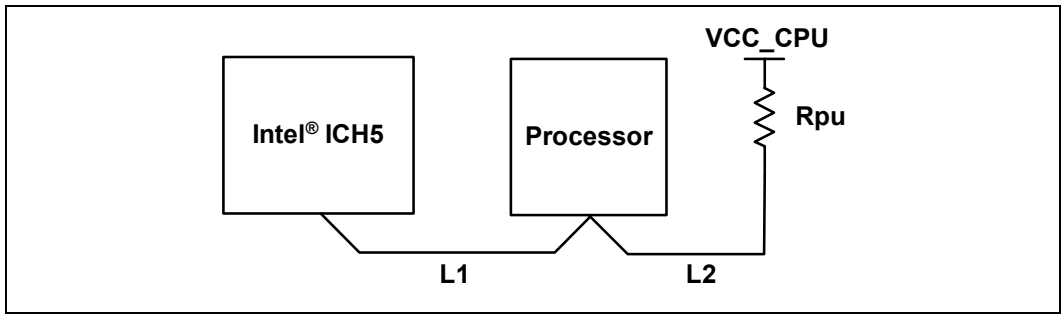
5.1.6.6 Topology 7: PWRGOOD

The PWRGOOD signal adheres to the following routing and layout recommendations. Figure 5-9 illustrates the recommended topology.

Table 5-13. Layout Recommendations for PWRGOOD

Trace Z_0	Trace Spacing	L1	L2	Rpu
60 Ω ± 15%	13 mils	1 inch to 12 inches	3 inches maximum	300 Ω ± 5%

Figure 5-9. Routing Illustration for PWRGOOD



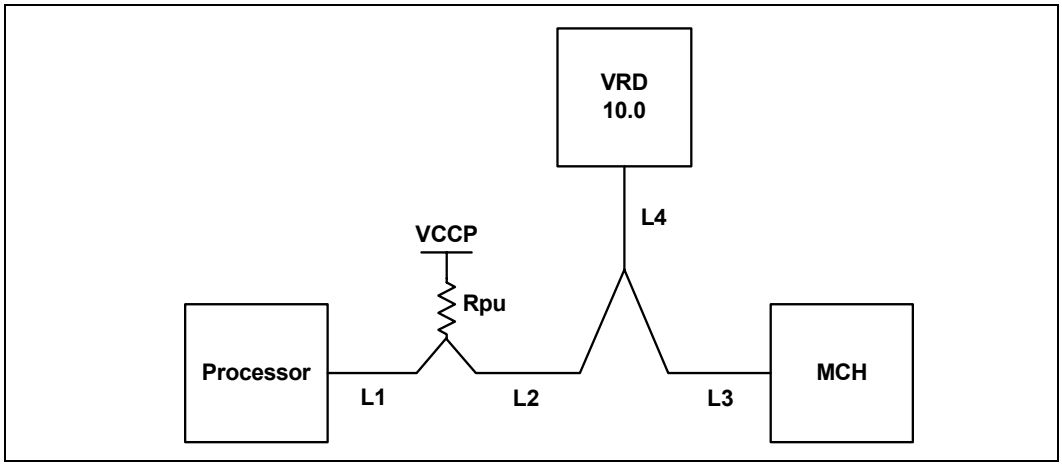
5.1.6.7 Topology 8: PROCHOT#

PROCHOT# adheres to the following routing and layout recommendations. Figure 5-10 illustrates the recommended topology. If PROCHOT# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for external logic.

Table 5-14. Layout Recommendations for PROCHOT#

Trace Z_0	Trace Spacing	L1	L2	L3	L4	Rpu
60 Ω ± 15%	7 mils	0.75 inch maximum	10 inches maximum	10 inches maximum	0.5 inch maximum	120 Ω –140 Ω ± 5%

Figure 5-10. Routing Illustration for PROCHOT#



5.1.6.8 Topology 9: TESTHI Signals

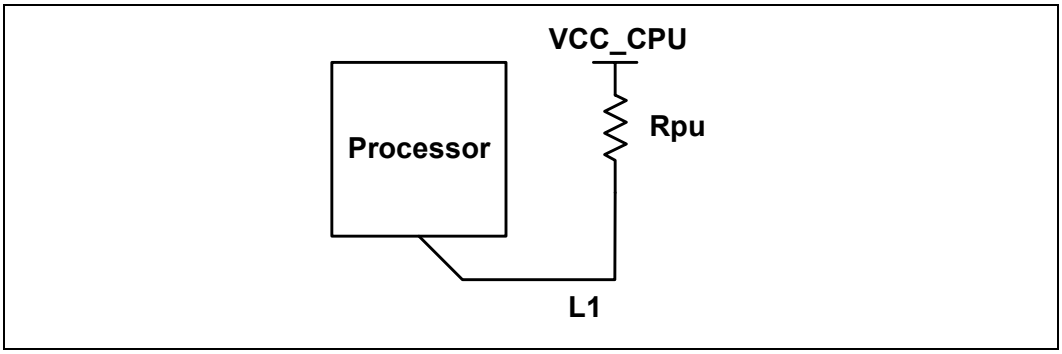
The TESTHI pins adhere to the following routing and layout recommendations. Figure 5-11 illustrates the recommended topology. The TESTHI pins may use individual pull-up resistors, or be grouped together as detailed below. A matched resistor, Rpu, should be used for each group.

- TESTHI[1:0]
- TESTHI[7:2]
- TESTHI8 - Cannot be grouped with any other TESTHI signal
- TESTHI9 - Cannot be grouped with any other TESTHI signal
- TESTHI10 - Cannot be grouped with any other TESTHI signal
- TESTHI11 - Cannot be grouped with any other TESTHI signal
- TESTHI12 - Cannot be grouped with any other TESTHI signal

Table 5-15. Layout Recommendations for TESTHI Signals

Trace Z_0	Trace Spacing	L1	Rpu
60 Ω ± 15%	7 mils	1 inch maximum	62 Ω ± 5%

Figure 5-11. Routing Illustration for TESTHI and Signals



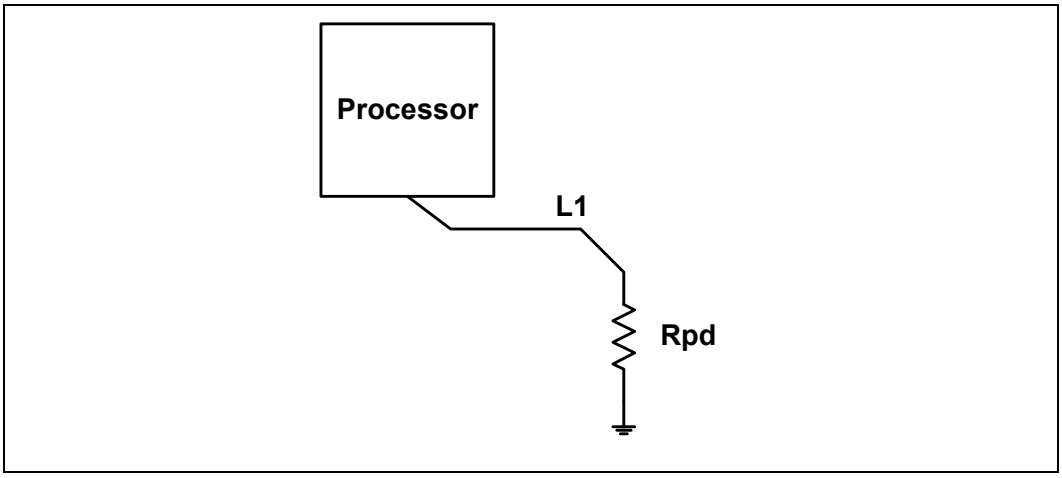
5.1.6.9 Topology 10: COMP[1:0]

The COMP[1:0] signals adhere to the following routing and layout recommendations. Figure 5-12 illustrates the recommended topology.

Table 5-16. Layout Recommendations for COMP[1:0]

Trace Z_0	Trace Spacing	L1	Rpd
60 Ω ± 15%	13 mils	1.5 inches maximum	61.9 Ω ± 1%

Figure 5-12. Routing Illustration for COMP[1:0]



5.1.6.10 Topology 11: BOOTSELECT

The Pentium 4 processor on 90 nm process processor and Pentium 4 processor with 512-KB L2 Cache on 0.13 micron process loadlines require a different slope. Therefore, the VRD must switch feedback networks depending on which processor is installed. The BOOTSELECT signal is used by the VRD to detect whether an Intel Pentium 4 processor on 90 nm process or Pentium 4 processor with 512-KB L2 Cache on 0.13 micron process is inserted into the processor socket and switches the feedback network. Figure 5-13 shows a block diagram of the switching logic. Figure 5-14 shows an example switching circuit.

Figure 5-13. VRD Feedback Switching Diagram

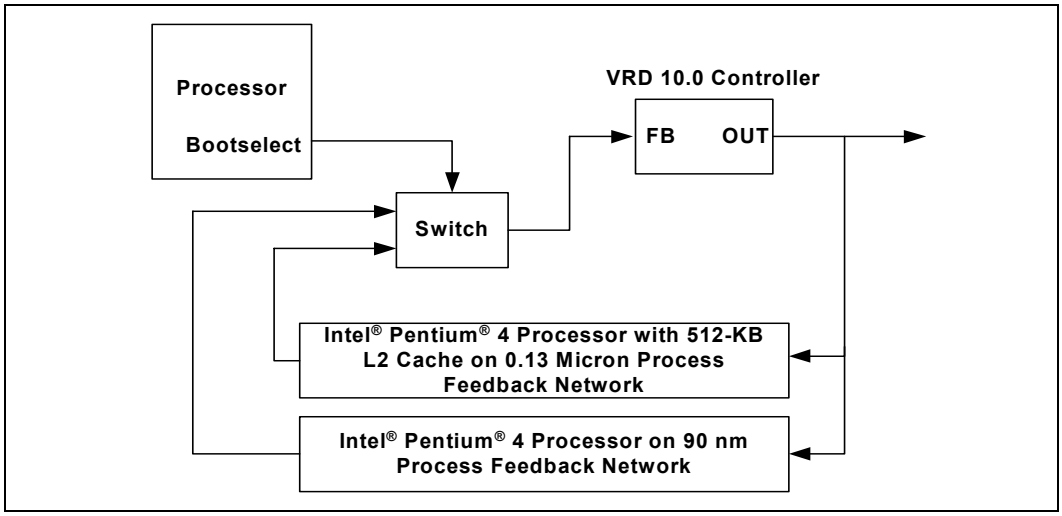
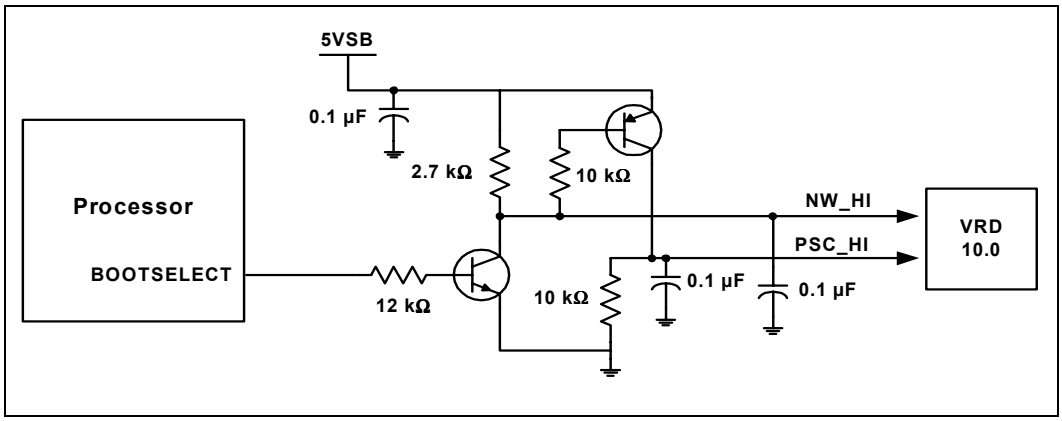


Figure 5-14. Routing Illustration for BOOTSELECT



5.1.6.11 Topology 12: RESERVED

All RESERVED pins must remain unconnected. Connection of these pins to VCC, VSS, or any other signal (including each other) can result in component malfunction or incompatibility with the Pentium 4 processor with 512-KB L2 Cache on 0.13 process or Pentium 4 processor on 90 nm process.

5.1.6.12 Topology 13: OPTIMIZED/COMPAT# and IMPSEL, and RSP#

For the Pentium 4 processor on 90 nm process, the OPTIMIZED/COMPAT# pin on the processor socket should be left as a no connect (NC).

For the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process, the IMPSEL pin on the processor socket should be left as a no connect (NC).

The RSP# signal is on both the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Pentium 4 processor on 90 nm process; this signal on the processor socket should be left as a no connect (NC).

5.1.6.13 Host VREFs

The AGTL+ VREF provides a reference voltage for all of the front side bus signals on the processor and MCH. It is required that a voltage divider yields 0.63 *VCC_AVG where VCC_AVG is the average voltage of VCC_CPU and MCH_VTT. The output is then routed to the processor's GTLREF and to the MCH's HDVREF pin. The trace should be a minimum of 12 mils wide and have a minimum of 15-mils separation from any other trace.

Figure 5-15. HD_VREF Circuit Topology

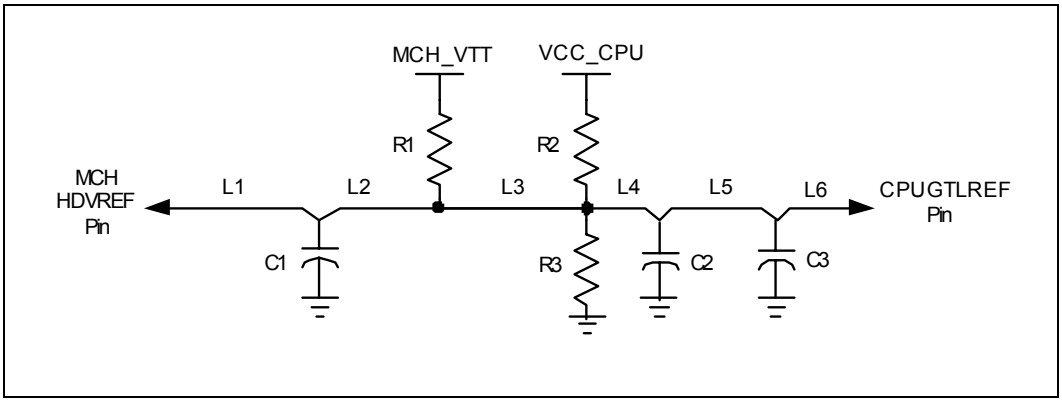


Table 5-17. Host VREF Resistor Values

Resistor	Value
R1	200 Ω ± 1%
R2	200 Ω ± 1%
R3	169 Ω ± 1%
C1	0.1 µF or 220 pF
C2	0.1 or 1.0 µF
C3	220 pF
L1+L2	3.5 inches maximum
L3	3 inches maximum
L4+L5+L6	1.5 inches maximum

NOTE:
1. C1 should be placed as close to the MCH pin as possible.
2. C3 should be placed as close to the processor pin as possible.

5.1.6.14 Host VID Topology

The host VID signals are used to set the processor's core and VCC_CPU voltages. These signals are open drain and require pull-up resistors. The resistors should be 1 kΩ ± 5% and pulled up to 3.3 V.

For the VID code to arrive at the VRD, System Management controller, and SIO with good signal integrity, it is required that the VID topology be as shown in Figure 5-16. Note, it is not required to route each leg of the diagram. For instance, if you only needed to route the VID lines from the processor to the VRD, you do not need to route legs L3 and L4. If the following topology cannot be followed, then it is recommended that thorough simulation be done to guarantee good signal integrity. The pull-up resistors can be located anywhere in the topology.

Figure 5-16. VID Topology

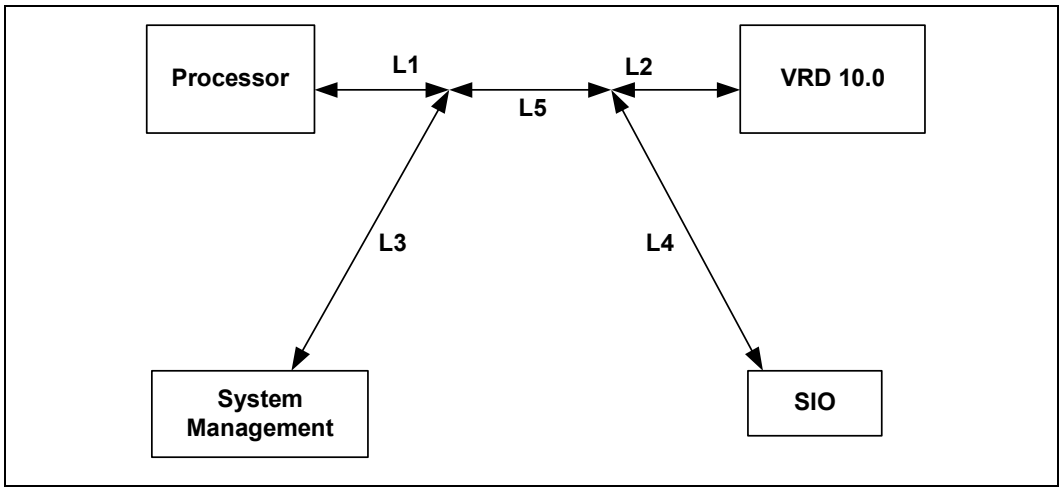


Table 5-18. VID Topology Trace Lengths

Dimension	Min	Max	Units
L1	—	12	Inches
L2	—	—	Inches
L1+L2+L5	—	15	Inches
L3	—	6	Inches
L4	—	6	Inches
L5	—	12	Inches

5.1.6.15 THERMDA/THERMDC

The processor incorporates an on-die thermal diode. THERMDA (diode anode) and THERMDC (diode cathode) pins on the processor can be connected to a thermal sensor located on the system board to monitor the die temperature of the processor for thermal management/long term die temperature change monitoring purpose. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Because the thermal diode is used to measure a very small voltage from the remote sensor, care must be taken to minimize noise induced at the sensor inputs. Below are some guidelines:

- Remote sensor should be placed as close as possible to the THERMDA/THERMDC pins. It can be approximately 4 to 8 inches away as long as the worst noise sources (e.g., clock generators, data buses and address busses, etc.) are avoided.
- Route the THERMDA/THERMDC lines in parallel and close together with ground guards enclosing the them.
- Use wide traces to reduce inductance and noise pickup that may be introduced by narrow traces or the system. A width of 10 mils and spacing of 10 mils is recommended.

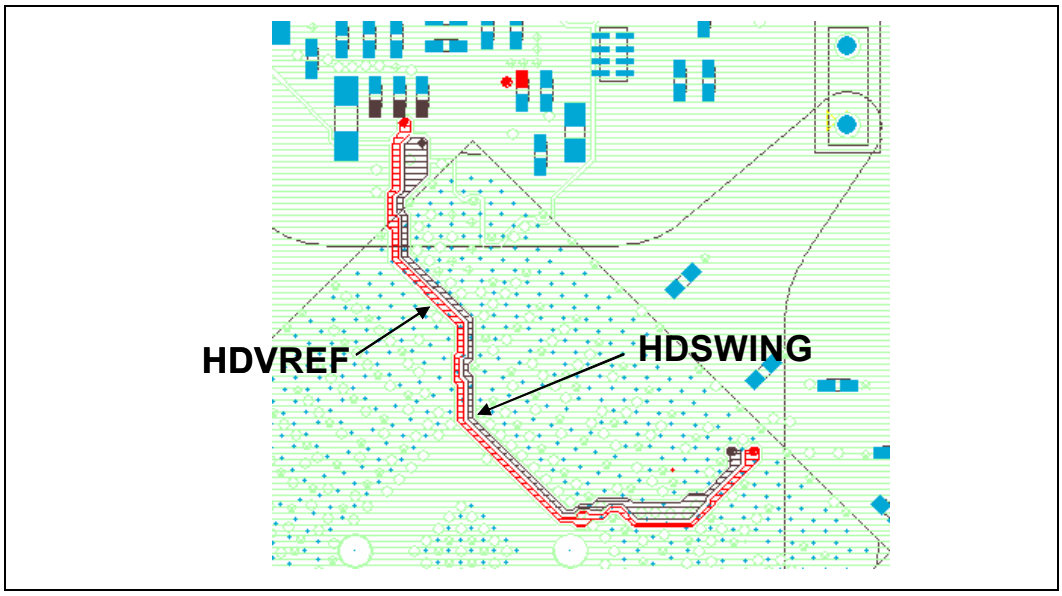
5.1.6.16 Host RCOMP

The RCOMP pins are used to calibrate the AGTL+ buffers and need to be terminated to a 20 Ω ± 1% pull-down resistor. It is recommended that the trace be a maximum of 0.5 inch long and be a minimum of 10-mils wide to reduce trace inductance. Keep this trace a minimum of 7 mils away from other traces.

5.1.6.17 Host SWING

VSWING needs to be 1/4*MCH_VTT, so a resistor divider with a 301 Ω ± 1% pull-up and a 102 Ω ±1% pull-down are recommended. The HXSWING and HYSWING can be tied together on the motherboard to reduce redundant circuitry. Decouple with one 0.01 µF capacitor at the MCH. The trace to the MCH should be routed at a maximum of 3 inches long at 12-mils wide and 10-mil spacing. This can be accomplished on Layer 2 (see Figure 5-17).

Figure 5-17. Host SWING Routing Example



5.1.6.18 BSEL

The BSEL circuit determines the FSB frequency. Connect processor's BSEL0 signal to CK409's FS_A pin. There should be a pull-up resistor and two pull-down resistors whose values are listed in Table 5-19. The middle of the voltage divider circuit should then connect to the MCH's BSEL0 pin. The two pull-down resistors form a voltage divider and are required for proper voltage levels for the MCH. Connect the MCH's BSEL1 to the CK409 FS_B pin in the same manner.

Figure 5-18. BSEL Topology

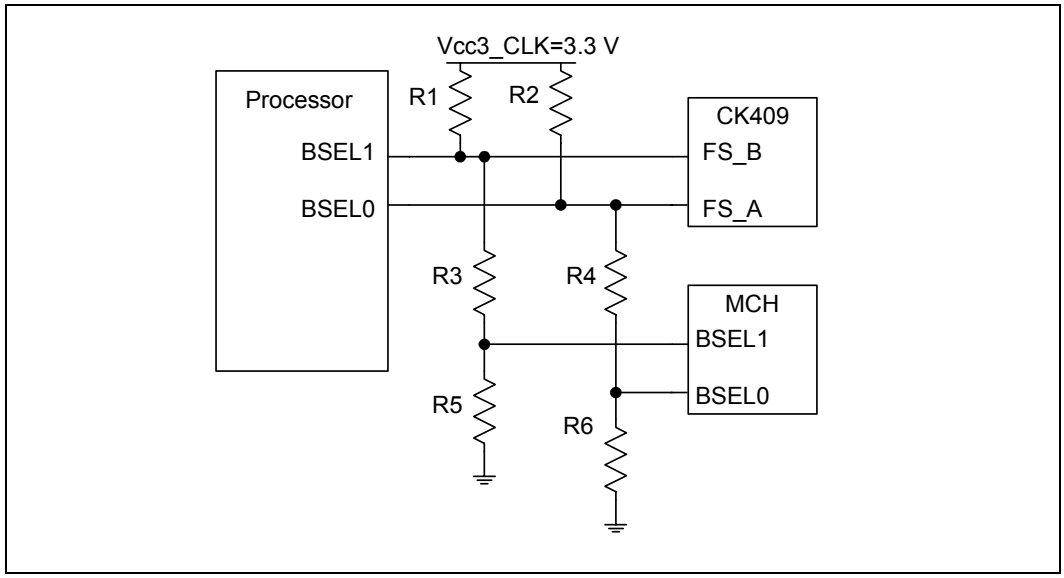


Table 5-19. BSEL Resistor Values

Resistor	Value
R1	1 kΩ ± 1%
R2	1 kΩ ± 1%
R3	2 kΩ ± 1%
R4	2 kΩ ± 1%
R5	2.49 kΩ ± 1%
R6	2.49 kΩ ± 1%

Table 5-20. FSB Frequency Selection

FS_A,FS_B	FSB Frequency
0,0	400 MHz
1,0	533 MHz
0,1	800 MHz

NOTE: Refer to the processor datasheet for FS_A and FS_B input latching.

5.2 Trace Length Matching

Trace length matching is required within each source synchronous group to compensate for the package trace length differences between data signals and the associated strobe. This will balance the strobe-to-signal skew in the middle of the setup and hold window. An example of trace length matching is given in Example 5-1 .

Trace length matching consists of matching the pad-to-pad lengths for every signal within a signal group (e.g., HA[35:17]# and ADSTB1#) to the associated strobe. A pad-to-pad length is measured as follows:

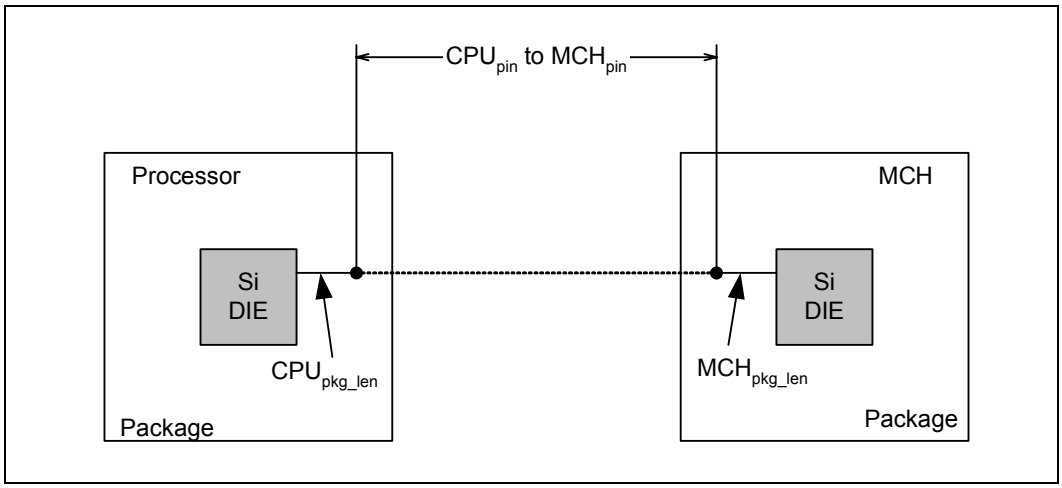
$$CPU_{pad}\text{-to-}MCH_{pad}\ Length = CPU_{pkg\_len} + CPU_{pin}\text{-to-}MCH_{pin} + MCH_{pkg\_len}$$

Where:

CPU_{pin}-to-MCH_{pin} = Motherboard trace length between Processor 1 and MCH.
pkg_len = Pad to pin length within the package.
$CPU1_{pkg\_comp}$ =CPUpkg_len * (capacitive loading compensation)

The package trace lengths for the MCH and processor are in the Intel® *848P Platform Trace Length Calculator*. Contact your field representative for this calculator.

Figure 5-19. Trace Length Matching for the Front Side Bus



When length matching, every signal's pad-to-pad length within a group is set equal to the pad-to-pad length of the associated strobe (± 25 mils). This yields the following equation:

CPUpkg_len (Signal) + CPUpin_len to MCHpin_len (Signal) + MCHpkg_len (Signal) =
CPUpkg_len (Strobe) + CPUpin_len to MCHpin_len (Strobe) + MCHpkg_len (Strobe)

To length match the signal and strobe, hold one of the signals constant, and vary the second signal until the equation is satisfied. Since all the pkg_len values are constant, we can solve for the Strobe:

CPUpin_len to MCHpin_len (Strobe) =
CPUpkg_len (Strobe)+CPUpin_len to MCHpin_len (Strobe) + MCHpkg_len (Signal)
– (CPUpkg_len (Signal) + MCHpkg_len (Signal))

Generally, when length matching a group of signals, a designer will first layout all signals to the shortest length possible allowed by specification. Then, keeping the longest signal as the constant value (Signal 1), lengthen all the other signals so that the pad-to-pad lengths are all equal.

Example 5-1. Trace Length Matching

Consider the signals HD4 and DSTBP0 and DSTBN0, from the same group. Calculate processor-to-MCH length for HD4:

CPU_{pkg_len} (DSTBP0) = 0.190 inch
CPU_{pkg_len} (DSTBN0) = 0.180 inch

CPU_{pin_len} to MCH_{pin_len} (DSTBP0) = 5.0 inches
CPU_{pin_len} to MCH_{pin_len} (DSTBN0) = 5.1 inches

MCH_{pkg_len} (DSTBP0) = 0.240 inch
MCH_{pkg_len} (DSTBN0) = 0.250 inch

CPU_{pad}-to-MCH_{pad} Length(DSTBP0) = 5.43 inches
CPU_{pad}-to-MCH_{pad} Length(DSTBN0) = 5.53 inches
CPU_{pad}-to-MCH_{pad} Length(DSTBavg) = 5.48 inches

CPU_{pkg_len} (HD4) = 0.198 inch
MCH_{pkg_len} (HD4) = 0.225 inch

CPU_{pin_len}-to-MCH_{pin_len}(HD4) =
CPU_{pad}-to-MCH_{pad} Length(DSTBavg) – (CPU_{pkg_len} (HD4) + MCH_{pkg_len} (HD4))

Therefore, the PCB trace length of HD4 must be within ± 25 mils of 5.507 inches from the processor-to-MCH.

5.3 Retention Mechanism Placement and Keepouts

The retention mechanism requires a keep-out zone, for limited component height area under the retention mechanism as shown in Figure 5-20 and Figure 5-21. The figures show the relationship between the retention mechanism mounting holes and pin one of the socket. In addition, these figures also document the keepouts. For heatsink volumetric information, refer to the appropriate Processor Thermal Design Guidelines document.

Figure 5-20. Retention Mechanism Keepout Drawing 1

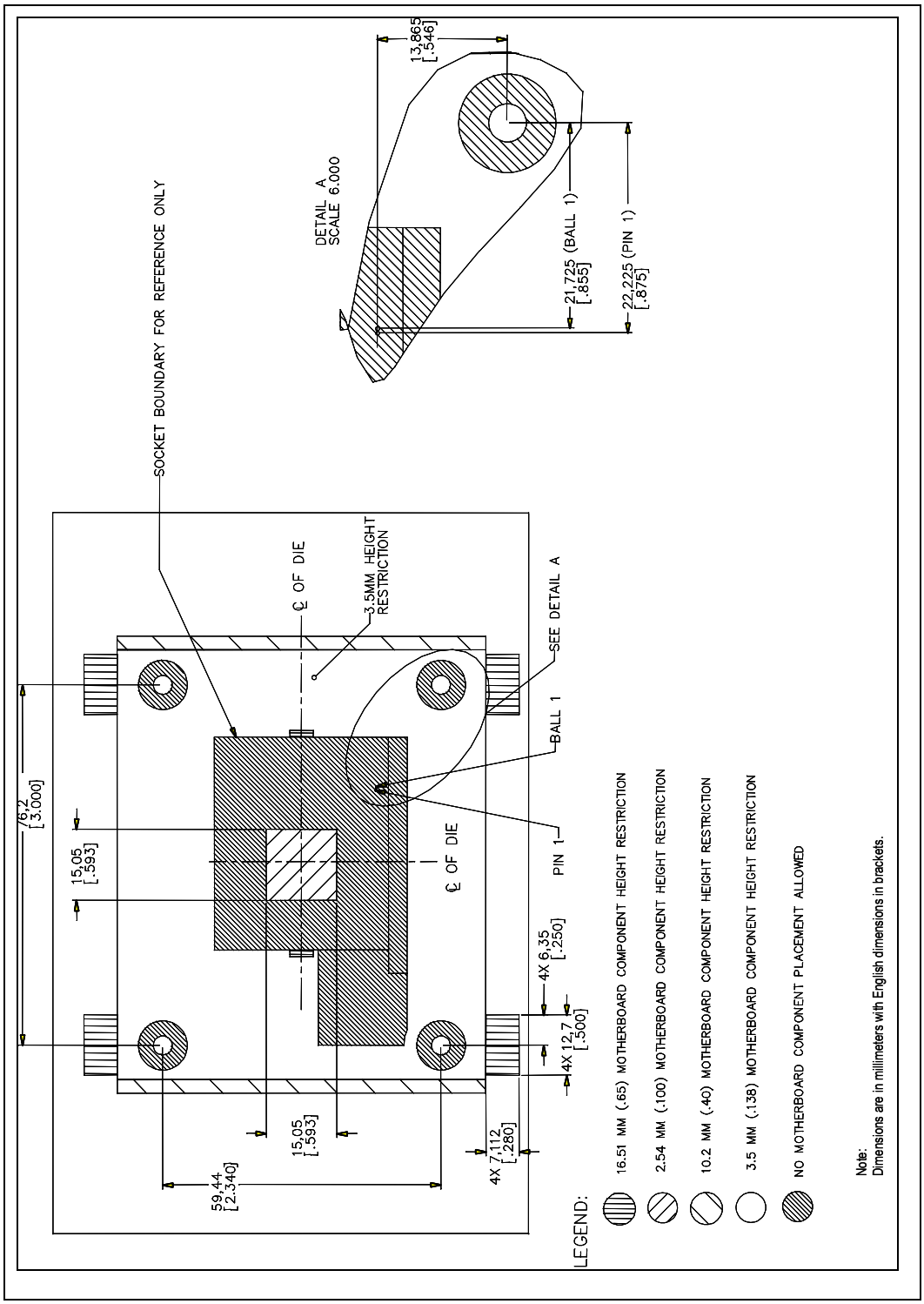
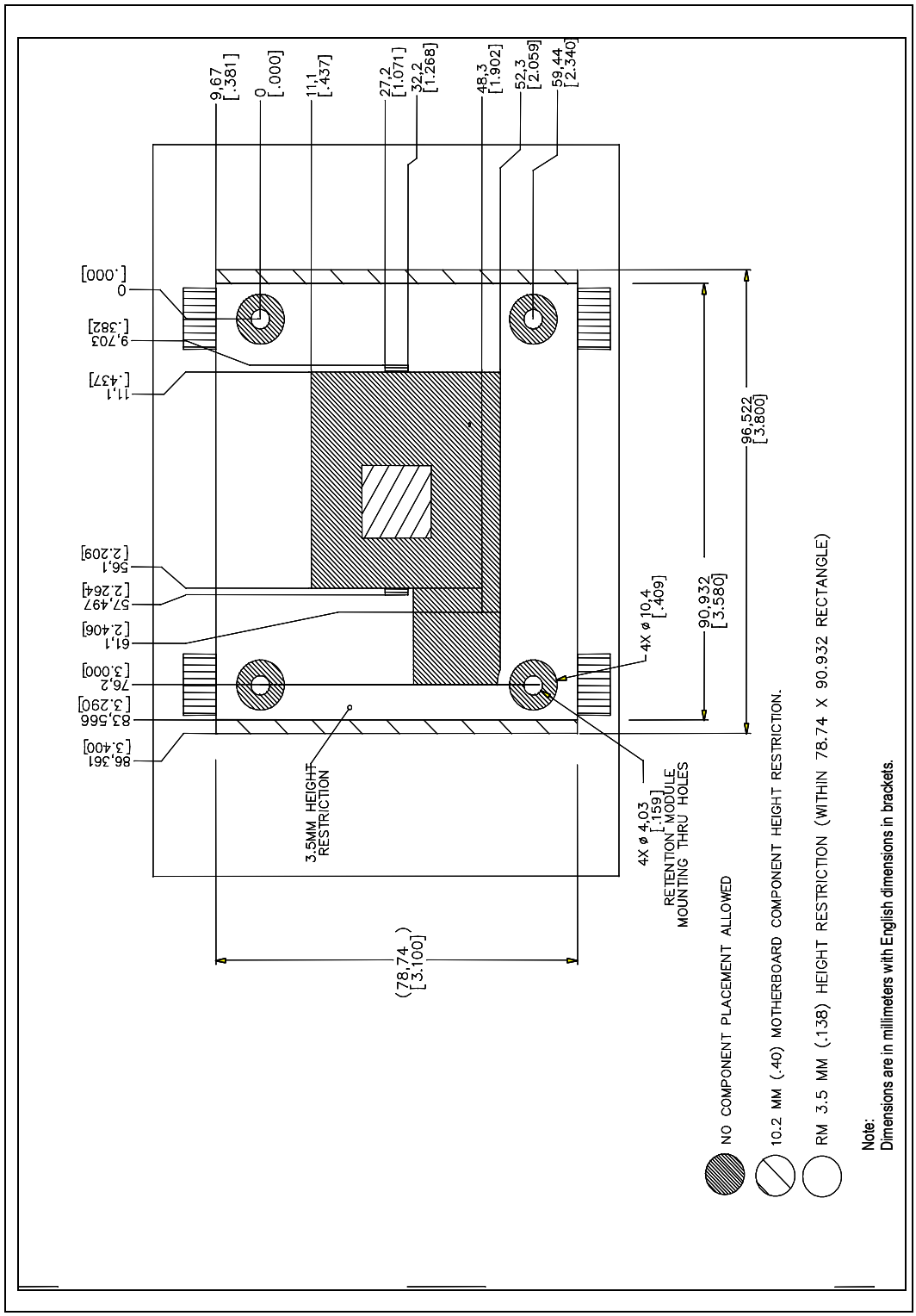


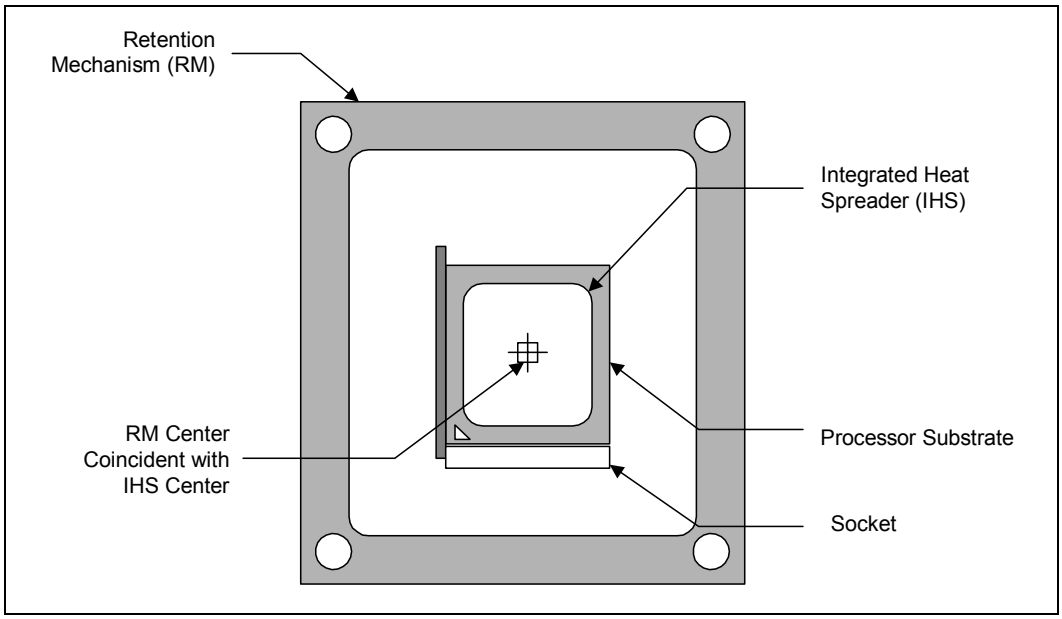
Figure 5-21. Retention Mechanism Keepout Drawing 2



5.4 Processor Location Relative to Retention Mechanism

To ensure the optimal thermal performance of a processor fan heatsink, the center of the processor integrated heat spreader (IHS) should be coincident with the center of the RM. Failure to center the IHS with respect to the RM may result in heatsink tilt and/or reduced thermal performance. Refer to Figure 5-22 for a diagram of IHS placement.

Figure 5-22. Processor Location Recommendation Relative to Retention Mechanism



5.5 Power Header for Active Cooling Solutions

The reference-design heatsink solution includes an integrated fan. The recommended connector for the active cooling solution is a Walden/Molex 22-01-3037, AMP 643815-3, or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. The fan connector pinout is described in Table 5-21.

Table 5-21. Reference Solution Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	No Connect

The Intel® boxed processor heatsink solution includes an integrated fan. The recommended connector for the active cooling solution is a Walden/Molex 22-23-2037, AMP 640456-3, or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. The fan connector pinout is described in Table 5-22.

Table 5-22. Boxed Processor Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	Sense

The fan heatsink outputs a SENSE signal which is an open-collector output that pulses at a rate of two pulses per fan revolution. The system board requires a pull-up resistor to provide the appropriate VOH level to match the fan speed monitor. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 should be tied to ground. For more information on boxed processor requirements, refer to the appropriate processor datasheet.

5.5.1 Fan Header Startup Current Capability

The fan header should be capable of supplying up to 2 A of fan startup current for 1-second duration. This startup current draw is a characteristic of the Intel reference design heatsink fan, and may potentially exist for other processor heatsink fans.

5.6 Debug Port Guidelines

Refer to the latest revision of the processor debug port design guide for details on the implementation of the debug port.

5.6.1 Debug Tools Specifications

5.6.1.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the Pentium 4 processor in the 478-pin package system. Tektronix and Agilent should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Pentium 4 processor in the 478-pin package system, the LAI is critical in providing the ability to probe and capture FSB signals. There are two sets of considerations to keeping mind when designing a Pentium 4 processor in the 478-pin package system that can make use of an LAI: mechanical and electrical.

5.6.1.2 Mechanical Considerations

The LAI is installed between the processor socket and the Pentium 4 processor in the 478-pin package. The LAI pins plug into the socket, while the Pentium 4 processor in the 478-pin package pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Pentium 4 processor in the 478-pin package and a logic analyzer. The maximum volume occupied by the LAI, known as the keep-out volume, as well as the gable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keep-out volume remains unobstructed inside the system. Note that it is possible that the keep-out volume reserved for the LAI may include space normally occupied by the Pentium 4 processor in the 478-pin package heatsink. If this is the case the logic analyzer vendor will provide a cooling solution as part of the LAI.

5.6.1.3 Electrical Considerations

The LAI will also affect the electrical performance of the FSB; therefore, it is critical to obtain the electrical load models from each of the logic analyzer to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

5.7 Processor Termination Summary

Table 5-23. Processor Signal Pull-Up/Pull-Down Summary (Sheet 1 of 4)

Signal Name	Type	Signal Buffer	Resistors	Design Guidelines
Address Bus				
A[35:32]#	I/O	Source Synch	Internal 54 Ω–66 Ω R_{TT} and 600 Ω R_L	NC
A[31:03]#	I/O	Source Synch	Same as above	Connect directly to MCH. No other termination required.
ADS#	I/O	Source Synch	Same as above	Connect directly to MCH. No other termination required.
ADSTB[1:0]#	I/O	Source Synch	Same as above	Connect directly to MCH. No other termination required.
AP[1:0]#	I/O	Common clk	Same as above	NC if unused
REQ[4:0]#	I/O	Source Synch	Same as above	Connect directly to MCH. No other termination required.
Data Bus				
D[63:0]#	I/O	Source Synch	Internal 54 Ω–66 Ω R_{TT} and 600 Ω R_L	Connect directly to MCH. No other termination required.
DBI[3:0]#	I/O	Source Synch	Same as above	Connect directly to MCH. No other termination required.
DSTBN[3:0]#	I/O	Source Synch	Same as above	Connect directly to MCH. No other termination required.
DSTBP[3:0]#	I/O	Source Synch	Same as above	Connect directly to MCH. No other termination required.
Control Pins				
BINIT#	I/O	Common clk	Internal 54 Ω–66 Ω R_{TT}	NC if unused
BNR#	I/O	Common clk	Internal 54 Ω–66 Ω R_{TT}	Connect directly to MCH. No other termination required.
BPRI#	I	Common clk	Internal 54 Ω–66 Ω R_{TT} and 600 Ω R_L	Connect directly to MCH. No other termination required.
BR0#	I/O	Common clk	Internal 600 Ω R_L	Connect to MCH. Place a 200 Ω external pull-up to VCC_CPU near processor.
DBSY#	I/O	Common clk	Internal 54 Ω–66 Ω R_{TT} and 600 Ω R_L	Connect directly to MCH. No other termination required.
DEFER#	I	Common clk	Same as above	Connect directly to MCH. No other termination required.
DP[3:0]#	I/O	Common clk	Same as above	NC if unused
DRDY#	I/O	Common clk	Same as above	Connect directly to MCH. No other termination required.
HIT#	I/O	Common clk	Internal 54 Ω–66 Ω R_{TT}	Connect directly to MCH. No other termination required.
HITM#	I/O	Common clk	Internal 54 Ω–66 Ω R_{TT}	Connect directly to MCH. No other termination required.
IERR#	OD	Common clk	Internal 600 Ω R_L	62 Ω external pull-up to VCC_CPU if used

Table 5-23. Processor Signal Pull-Up/Pull-Down Summary (Sheet 2 of 4)

Signal Name	Type	Signal Buffer	Resistors	Design Guidelines
LOCK#	I/O	Common clk	Internal 54 Ω–66 Ω R_{TT} and 600 ohm R_L	Connect directly to MCH. No other termination required.
MCERR#	I/O	Common clk	Internal 54 Ω–66 Ω R_{TT}	NC if unused
PROCHOT#	I/O	Asynch GTL+	Internal 54 Ω–66 Ω R_{TT}	120 Ω ~ 140 Ω external pull-up to VCC_CPU for Northwood
RESET#	I	Common clk	External pull-up	Connect to MCH. Place a 62 Ω external pull-up to VCC_CPU near processor.
RS[2:0]#	I	Common clk	Internal 54 Ω–66 Ω R_{TT} and 600 Ω R_L	Connect directly to MCH. No other termination required.
RSP#	I	Common clk	Same as above	NC if unused
TRDY#	I	Common clk	Same as above	Connect directly to MCH. No other termination required.
Intel® ICH5 Interface				
A20M#	I	Asynch GTL+	None	Connect directly to ICH5. No other termination required.
FERR#	OD	Asynch GTL+	Internal 600 Ω R_L	Connect to ICH5. Place a 62 Ω external pull-up to VCC_CPU near ICH5.
IGNNE#	I	Asynch GTL+	None	Connect directly to ICH5. No other termination required.
INIT#	I	Asynch GTL+	None	Connect to ICH5. Connect to flash BIOS through voltage translation
LINT0	I	Asynch GTL+	None	Connect to ICH5 INTR.
LINT1	I	Asynch GTL+	None	Connect to ICH5 NMI.
PWRGOOD	I	Asynch GTL+	External Pull-up (ICH's CPUPWRGD is OD)	Connect directly to ICH5. Place a 300 Ω external pull-up to VCC_CPU near processor
SMI#	I	Asynch GTL+	None	Connect directly to ICH5. No other termination required.
STPCLK#	I	Asynch GTL+	None	Connect directly to ICH5. No other termination required.
SLP#	I	Asynch GTL+	None	Connect directly to ICH5. No other termination required.
THERMTRIP#	O	Asynch GTL+	External pull-up	Connect to ICH5. Place a 62 Ω pull-up to VCC_CPU near ICH5.

Table 5-23. Processor Signal Pull-Up/Pull-Down Summary (Sheet 3 of 4)

Signal Name	Type	Signal Buffer	Resistors	Design Guidelines
Clock Pins				
BCLK[1:0]	I	Differential System Clock	External termination	Connect to output of CK409. Proper termination required at CK409
BSEL0	O	High Voltage Tolerant Buffer	External pull-up	Connect to CK409 FS_A pin. Connect to MCH SELx pins. 1 kΩ pull-up to 3.3 V required at CK409. MCH requires divider for 1.5 V tolerant inputs.
BSEL1	O	High Voltage Tolerant Buffer	External pull-up	Connect to CK409 FS_B pin. Connect to MCH SELx pins. 1 kΩ pull-up to 3.3 V required at CK409. MCH requires divider for 1.5 V tolerant inputs.
ITP_CLK0	I	Differential ITP clock	External termination required at CK409	Connect to BCLK0 of one of the CK409 BCLK pairs, or NC for no interposer support
ITP_CLK1	I	Differential ITP Clock	External termination required at CK409	Connect to BCLK1 of one of the CK409 BCLK pairs, or NC for no interposer support.
Voltage Regulator Interface				
VCC_SENSE	NA	Power/Other	None	Connect to VR control silicon if used.
VID[5:0]	O	Power/Other	External Pull-up	Connect to VR control silicon and possibly hardware monitor circuitry. Requires 1 kΩ pull-ups to 3.3 V
VIDPWRGD	I	Power/Other	External pull-up	Connect to power good output of the 1.2 V linear supply w/ 8.2 kΩ pull-up.
VSS_SENSE	NA	Power/Other	None	Connect to VR control silicon if used.
ITP Interface (Refer to Processor Debug Port Design Guide for more detail)				
TDO	O	TAP	External pull-up	51Ω 5% pull-up to VCC_CPU near 47Ω 5% series resistor to ITP.
TCK	I	TAP	External pull-down	27.4 Ω 1% pull-down to GND near ITP and 47Ω 5% pull-down to GND near processor for ITP-USB.
TDI	I	TAP	External pull-up	150 Ω pull-up to VCC_CPU near processor.
TMS	I	TAP	External pull-up	39.2 Ω 1% pull-up to VCC_CPU near ITP and 47Ω 5% pull-up to VCC_CPU near processor for ITP-USB.
TRST#	I	TAP	External pull-down	510 Ω ~ 680 Ω pull-down to GND.
DBR#	OD	Power/Other	External pull-up	8.2 kΩ pull-up to VccSus3_3 near ICH5 and connect to system reset logic (FP reset).
BPM[5:0]#	I/O	Common clk	External pull-up	62 Ω pull-up to VCC_CPU near processor.

Table 5-23. Processor Signal Pull-Up/Pull-Down Summary (Sheet 4 of 4)

Signal Name	Type	Signal Buffer	Resistors	Design Guidelines
Miscellaneous Pins				
BOOTSELECT	I	Power/Other	Internal 500 ~ 5000 Ω pull-up to VCCVID	Connect to dual loadline select circuitry.
COMP0	I/O	Compensation	External pull-down	61.9 Ω pull-down to VSS.
COMP1	I/O	Compensation	External pull-down	61.9 Ω pull-down to VSS.
GTLREF[3:0]	I	Analog	External voltage divider (1% resistor)	0.63*VCC_CPU divider to one of the 4 GTLREF pins; others are NC. See Section 5.1.6.13.
OPTIMIZED/ COMPAT# (Intel® Pentium® 4 processor on 90 nm process) IMPSEL (Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process)	I	Power/Other	Internal 500 ~ 5000 Ω pull-up to VCCVID	NC
SKTOCC#	NA	Power/Other	Internal pull to GND	Depends on customer need
TESTHI[1:0]	I	Analog	External Pull-up	62 Ω pull-up to VCC_CPU; can be grouped.
TESTHI[7:2]	I	Analog	External Pull-up	62 Ω pull-up to VCC_CPU.
TESTHI8	I	Analog	External pull-up	62 Ω pull-up to VCC_CPU.
TESTHI9	I	Analog	External pull-up	62 Ω pull-up to VCC_CPU.
TESTHI10	I	Analog	External pull-up	62 Ω pull-up to VCC_CPU.
TESTHI11	I	Analog	External pull-up	62 Ω pull-up to VCC_CPU.
TESTHI12	I	Analog	External pull-up	62 Ω pull-up to VCC_CPU.
THERMDA	I	Diode	None	Connect to external diode monitoring circuit if used.
THERMDC	O	Diode	None	Connect to external diode monitoring circuit if used.

DDR System Memory Guidelines 6

The guidelines documented in this chapter are based on the use of standard 90-degree 184 pin DDR DIMM connectors, standard JEDEC and Intel compliant DIMMs (x16SS, x8SS, x8DS), standard JEDEC and Intel compliant DRAMs, and other physical motherboard parameters outlined in this document. Deviations from the recommended DDR system memory guidelines in terms of topology, layout, connector type, and configuration can cause system instability. If any deviations from this design guide occur, Intel highly recommends extensive modeling, simulation, and validation be performed to ensure the changes meet DDR DRAM (both JEDEC and Intel Addendum requirements) and system requirements.

The MCH memory interface consists of one DDR memory channel consisting of 64 data bits.

This section covers routing guidelines for the DDR interface. The DDR interface has six signal groups: Clocks, Address/Command, Data, Control, Command per Clock (CPC) Address, Receive Enable and Miscellaneous. Table 6-1 summarizes the signal groupings.

For details on the signals listed in Table 6-1, refer to the *Intel® 848P Chipset Datasheet*. Refer to Chapter 15 of this design guide for DDR power delivery considerations.

Table 6-1. MCH DDR Signal Groups

Section	Group	Signal	Description
Section 6.2.2	Clocks	SCMDCLK_A[5:0] SCMDCLK_A[5:0]#	DDR Differential Clocks DDR Differential Inverted Clocks
Section 6.2.3	Address/Command	SMAA_A[12:6,0] SRAS_A# SCAS_A# SWE_A# SBA_A[1:0]	Memory Address Bus Row Address Select Column Address Select Write Enable Bank Address (Bank Select)
Section 6.2.4	Data	SDQS_A[7:0] SDQ_A[63:0]	Data Strobes Data Bus
Section 6.2.5	Control	SCS_A[3:0]# SCKE_A[3:0]	Chip Select Clock Enable
Section 6.2.6	CPC Address	SMAA_A[5:1] SMAB_A[5:1] / TESTP[29:25]	Memory Address Bus CPC Signals

Note: The 848P chipset does not support Error Checking and Correction (ECC). Refer to the *Intel® 848P Chipset Datasheet* for more signal details.

6.1 DDR-SDRAM Stack-Up and Referencing Guidelines

The 848P chipset platform designs require ground referencing for all DDR signals. Based on a typical four layer stack-up, the DDR channel will require the following stack-up to ground reference all of the DDR signals from the MCH to the termination at the end of the channel.

Note: The DDR channel stack-up applies to the DDR channel only.

Table 6-2. DDR Channel Referencing Stack-Up

Motherboard Layer	Description
Layer 1, Signal Top	Signal/Power
Layer 2, Power	Ground Cutouts
Layer 3, Ground	Ground
Layer 4, Signal Bottom	Signal/Power

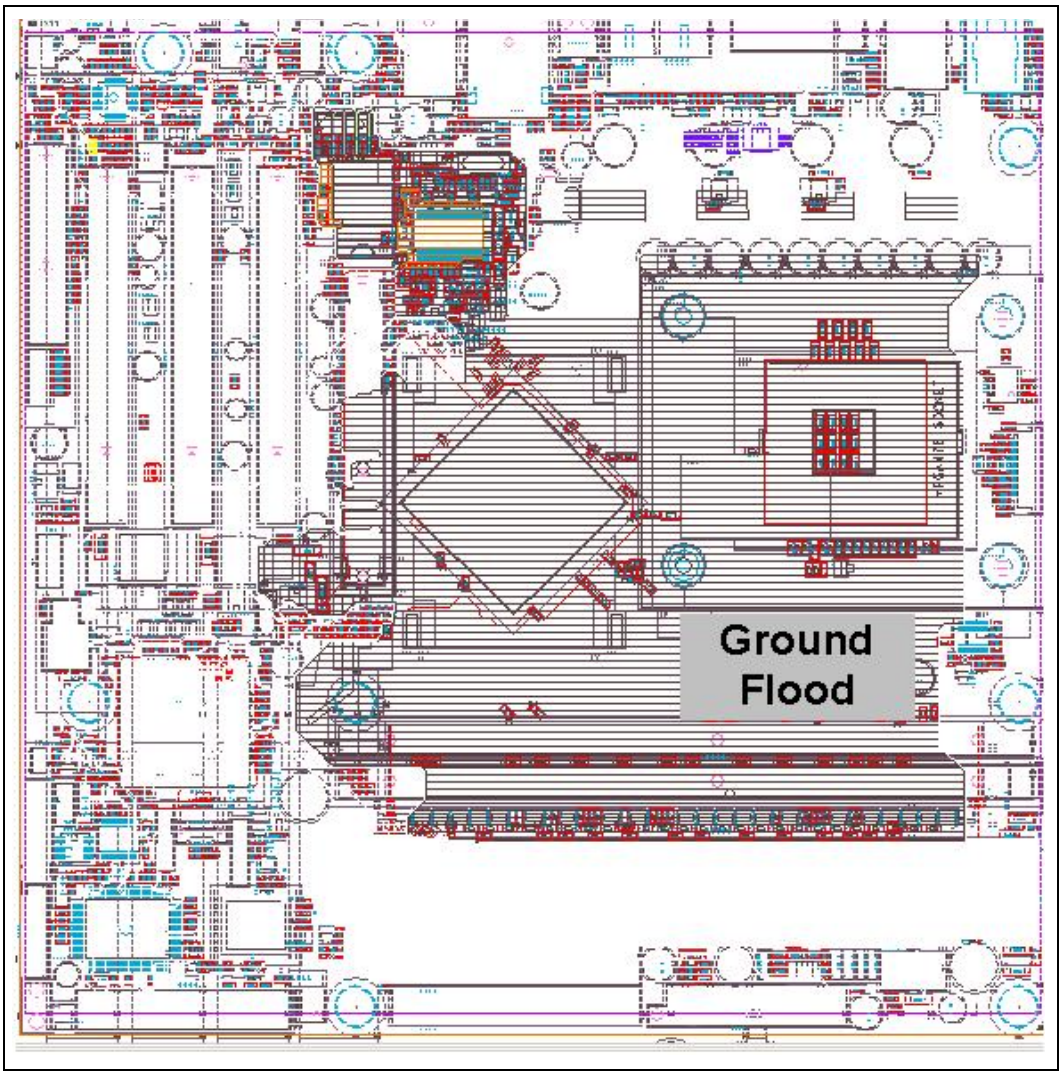
A solid ground flood needs to be placed under the DDR channel on layer 2 from the MCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel to provide an optimal return current path. Any split in the ground flood will provide a sub-optimal return path.

Ground Stitching

Ground floods must be well stitched to the ground plane on layer 3 to ensure the same potential between the two planes. Any ground pin or ground via that is placed in the DDR routing area must connect to both the ground flood and the ground plane.

Note: No power to the MCH is delivered on Layer 2. This is due to the strict ground referencing requirements. As a result, this region on Layer 2 is a large ground flood. Consequently, power must be delivered on Layer 4 (bottom); thus, care must be taken to allow for proper power delivery on this external layers. Refer to Chapter 15, “Power Distribution Guidelines” for more information.

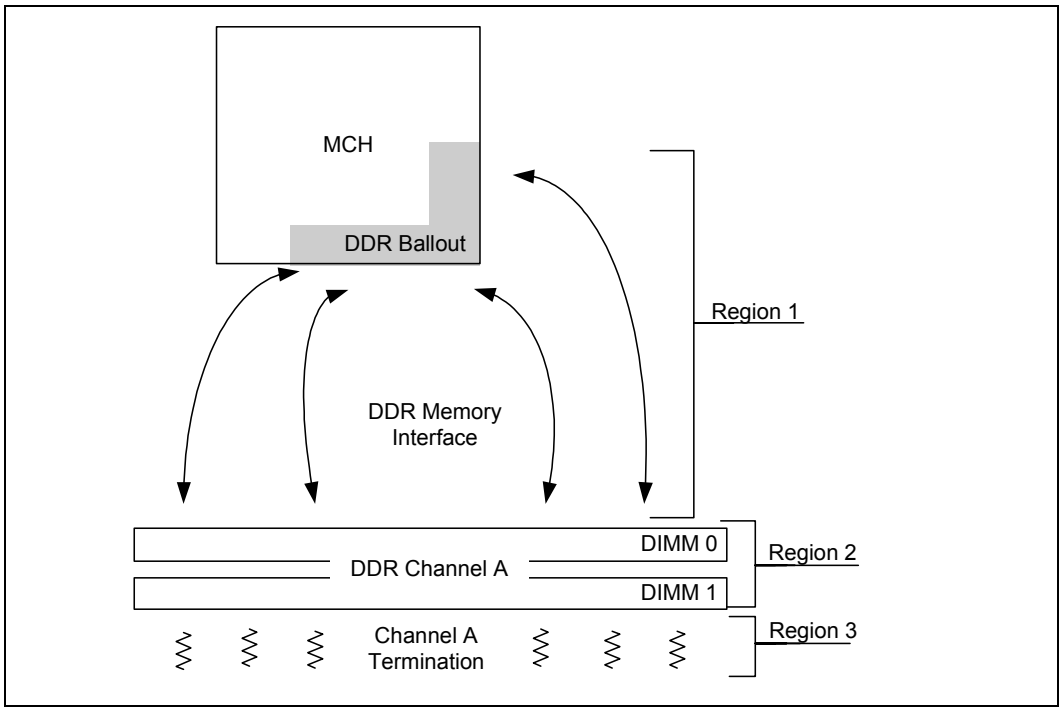
Figure 6-1. Example of Ground Flood on Layer 2



6.2 DDR Design Guidelines

The layout guidelines all reference Figure 6-2 for trace width and spacing.

Figure 6-2. DDR Regions for Trace Width and Spacing



NOTES:
1. Refer to this drawing when using DDR trace width and spacing tables.
2. Channel A signals that terminate in Region 3 will all neck down to 5 on 5 routing

The layout guidelines in this chapter were developed with the following design assumptions:

- A standard 4-layer motherboard stack up (signal, power, ground, signal)
- One DDR channel
- **All** channel A DDR signals are routed on layer 1

6.2.1 Target Impedances

The target impedances listed throughout Section 6.2 all refer to Region 1 of Figure 6-2; this is the area between the MCH and first DIMM.

Due to the congested routing in the DIMM connector and termination regions of the routing channel, it is not possible to meet the target impedances in these regions. As a result, it is not possible to maintain the target impedances once the signals reach the first DIMM connector. The resulting guidelines for Regions 2 and 3 do not meet the target impedance but have been simulated and are believed to offer the best possible electrical characteristics given the severely constrained routing area.

6.2.2 Clocks (SCMDCLK_A[5:0], SCMDCLK_A[5:0]#)

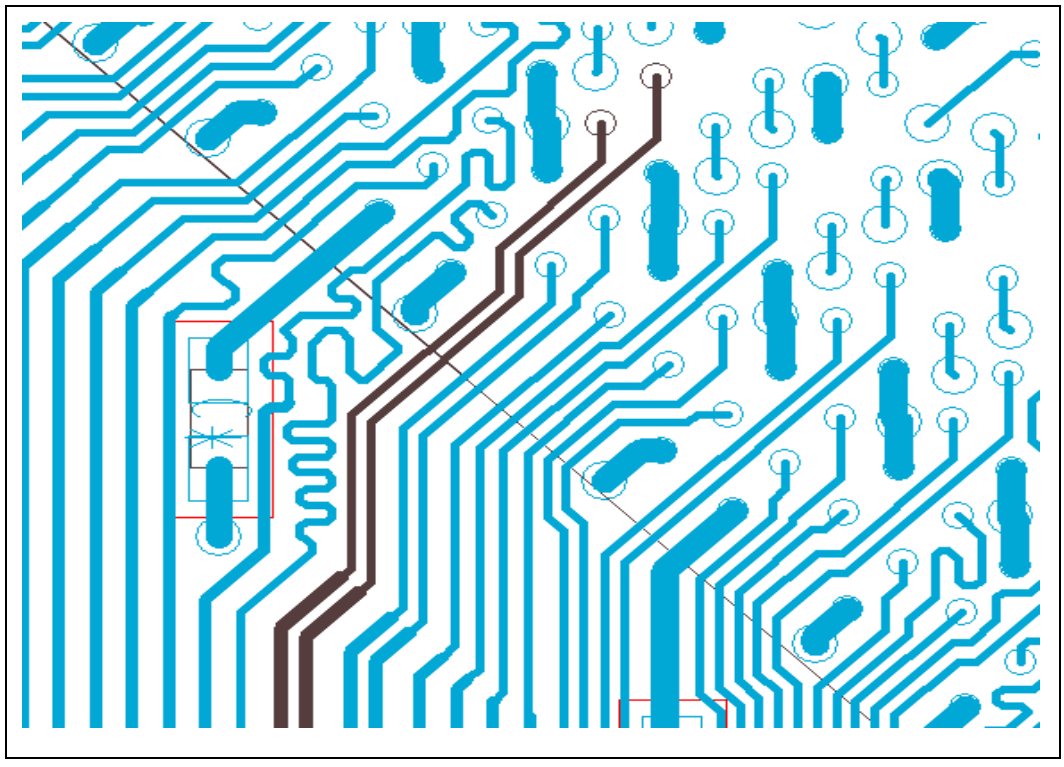
The MCH clock signals include six differential clock pairs. The MCH generates and drives these differential clock signals required by the DDR interface. Therefore, no external clock driver is required for the DDR interface. Since the MCH only supports unbuffered DDR DIMMs, three differential clock pairs are routed to each DIMM connector.

Table 6-3. Clock Signal DIMM Mapping per DIMM

Signal	Relative To
SCMDCLK_A[2:0] SCMDCLK_A[2:0]#	DIMM0
SCMDCLK_A[5:3] SCMDCLK_A[5:3]#	DIMM1

DDR clocks can breakout of the MCH with reduced width (neckdown to 5 on 5) for a maximum length of 550 mils; however, use of this reduced trace width should be minimized where possible. Figure 6-3 shows and example of the clock neckdown in the MCH breakout.

Figure 6-3. Example of DDR Clock Neckdown at MCH



The clock pairs must be routed differentially from the MCH to their DIMM pins. They must maintain correct spacing of 5 mils between themselves to remain differential. Additionally, the clocks must maintain an isolation spacing of 20 mils away from other signals or from itself in a serpentine.

There are no external termination resistors needed for the SCMDCLK_A/SCMDCLK_A# signals. Table 6-4, Table 6-5, Figure 6-4, and Figure 6-5 depict the recommended topology and layout routing guidelines for the DDR differential clocks.

Table 6-4. DDR Clock Trace Width and Spacing Guidelines

Routing Region	Routing Guidelines (width and spacing in mils)
Target Differential Impedance	70 Ω ± 15%
MCH to 1st DIMM (Region1)	8 on 5
DIMM pin field (Region 2)	6 on 5
Termination (Region 5)	N/A

Table 6-5. DDR Clock Length Matching Guidelines

Parameter	Routing Guideline
MCH die to DIMM pin: Length = P + A	Max = 6.3 inches
Total Clock Length Relationship between DIMM0 and DIMM1 for a channel	The total clock length difference should be no more than 1 inch.
Maximum via count per signal	1 via (for breakout to bottom layer)
Length Matching method, Length = P + A	Each SCMDCLK_A and SCMDCLK_A# pair must be tuned to within 20 mils. All three clock pairs on a given DIMM must be less than 600 mils different in length.

NOTE: Refer to Figure 6-4 and Figure 6-5.

Figure 6-4. DDR Differential Clock Length Matching Topology

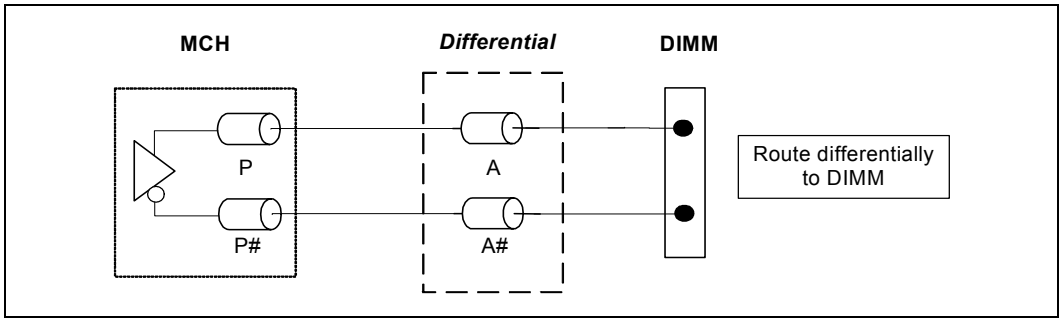
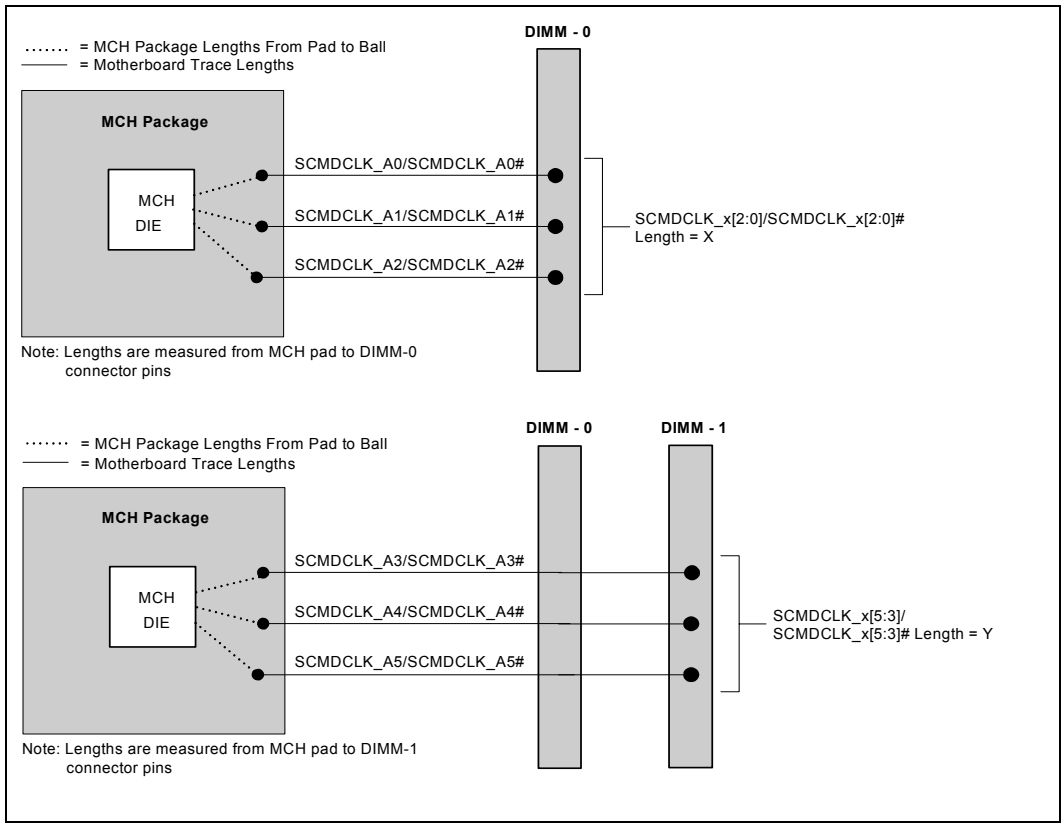


Figure 6-5. Differential Clock Trace Length Matching Requirements



6.2.3 Address/Command (SMAA_A[12:0], SBA_A[1:0], SRAS_A#, SCAS_A#, SWE_A#)

The MCH address/command signals are source-clocked signals that include memory address signals SMAA_A[12:6,0], SBA_A[1:0], SRAS_A#, SCAS_A#, SWE_A#. The address signals SMAA_A[5:1]/SMAB_A[5:1] are detailed in Section 6.2.6. The address/command signals are tuned to SCMDCLK_A.

Table 6-6, Table 6-7, Figure 6-6, and Figure 6-7 show the recommended topology and routing guidelines for the DDR address/command signals.

Table 6-6. Address/Command Trace Width and Spacing Guidelines

Routing Region	Routing Guidelines (width on spacing)
Target Impedance	60 Ω ± 15%
MCH Breakout	5 on 5 up to a max of 550 mils
MCH to 1st DIMM (Region 1)	5 on 12
DIMM pin field (Regions 2)	5 on 6
Termination (Regions 3)	5 on 5

Table 6-7. Address/Command Length Matching Guidelines

Parameter	Routing Guideline
Trace Length B (First DIMM Pin to Second DIMM pin)	Length must be 200–600 mils, but with ≤ 200 mils variance between the longest and shortest trace segments for that channel.
Trace Length C (Last DIMM Pin to termination)	Max = 800 mils
MCH die to last DIMM pin One DIMM/channel: Length = P + A Two DIMM/channel: Length = P + A + B	Max = 5.3 inches
Termination Resistor (Rtt)	47 Ω ± 5%
Max via count per signal	Two vias (for bottom layer signals, one at MCH ballout and the other at termination, where needed).
Length Tuning to DIMM-0 (Length = P + A)	SCMDCLK_A[2:0] = X Xmin – 2.1 inches ≤ Addr/Cmd length ≤ Xmax
Length Tuning to DIMM-1 (Length = P + A + B)[1]	SCMDCLK_A[5:3] = Y Ymin – 2.1 inches ≤ Addr/Cmd length ≤ Ymax.

NOTES:.
1. Refer to Figure 6-6 and Figure 6-7.

Figure 6-6. Address/Command Length Matching Topology

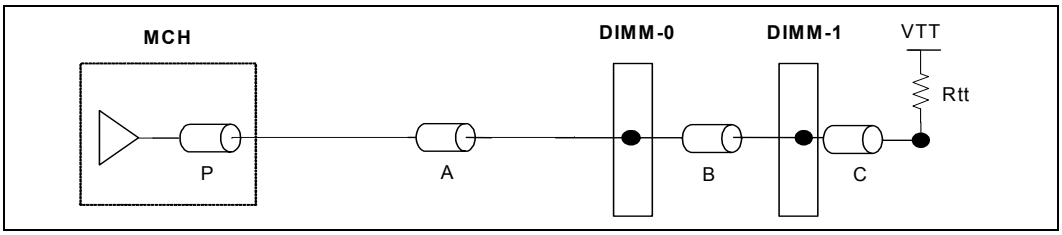
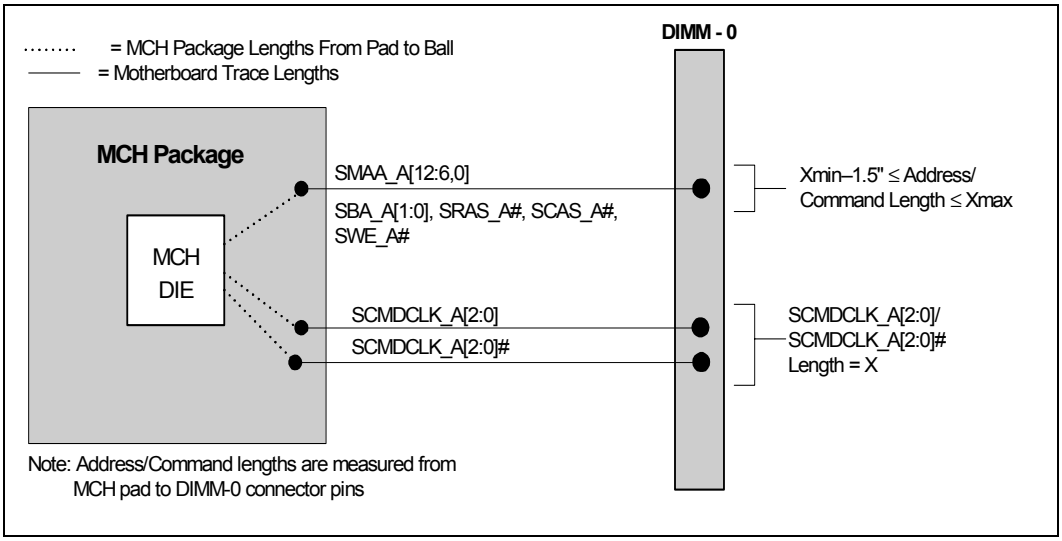


Figure 6-7. Address/Command to Clock Length Matching Requirements



6.2.4 Data Signals (SDQ_A[63:0], SDQS_A[7:0])

The MCH DDR data signals are source synchronous signals. The channel includes a 64-bit wide data bus and eight data strobe signals. There is an associated data strobe (SDQS_A) for each data group. Table 6-8 summarizes the SDQ_A /SDM_A to SDQS_A mapping. SDQ_A /SDM_A signals are tuned to their associated SDQS_A signal, and SDQS_A signals are tuned to SCMDCLK_A lengths.

Table 6-8. SDQ_A to SDQS Byte Lanes Mapping

SDQ_A	SDQS_A
SDQ_A[7:0]	SDQS_A0
SDQ_A[15:8]	SDQS_A1
SDQ_A[23:16]	SDQS_A2
SDQ_A[31:24]	SDQS_A3
SDQ_A[39:32]	SDQS_A4
SDQ_A[47:40]	SDQS_A5
SDQ_A[55:48]	SDQS_A6
SDQ_A[63:56]	SDQS_A7

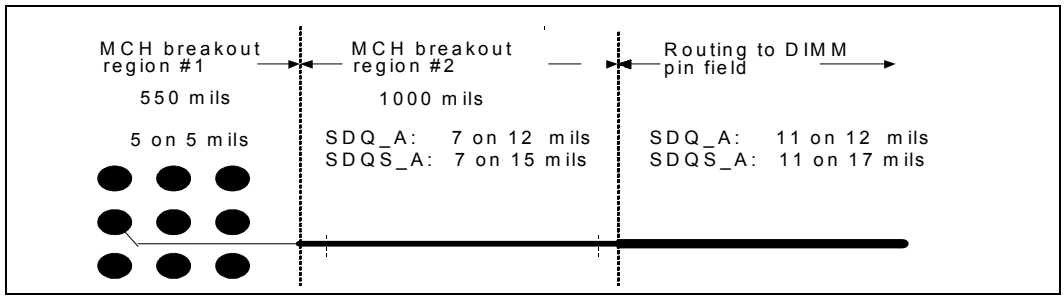
Table 6-8 through Table 6-10 and Figure 6-8 through Figure 6-11 show the recommended topology and layout routing guidelines for the DDR data signals.

Table 6-9. Data Signal Trace Width and Spacing Guidelines

Routing Region	3.0” < Byte Lane Length ≤ 5.7”	5.7” < Byte Lane Length ≤ 6.9”
Target Impedance	50 Ω ± 15%	40 Ω ± 15%
MCH Breakout	5 on 5 up to a max of 550 mils	5 on 5 up to a max of 550 mils then: 7 on 12 for up to 1000 mils (SDQ_A) 7 on 15 for up to 1000 mils (SDQS_A)
MCH to First DIMM (Region 1)	7 on 12 mils for SDQ_A 7 on 15 mils for SDQS_A	11 on 12 for SDQ_A 11on 17 for SDQS_A
DIMM pin field (Regions 2)	SDQ_A: 5 on 5 mils SDQS_A: 5 on 10 mils	SDQ_A: 7 on 5 mils SDQS_A: 7 on 10 mils
Termination (Regions 3)	5 on 5	5 on 5

NOTES:
1. Byte Lane (SDQS_A and associated strobe SDQ_A signals) routed from MCH to last DIMM connector.
2. When implementing the wider 11-mil trace width rule on long byte lanes, the wider trace width should be implemented on all DQ and DQS signals within a byte lane. If necessary, the wider trace width may be achieved incrementally; however, the widest possible width should be achieved as quickly as possible. The final 11-mil trace width should be achieved within 2.0 inches of the ball. Also, note that normal L2 spacing rules apply for the transition region.

Figure 6-8. Data Signal Breakout Topology for Byte Lane Lengths > 5.7 Inches



If the trace width and spacing rules for the different routing regions cannot be met, follow the recommendations below in sequential order:

1. Decrease SDQS_A-to-SDQ_A spacing to 11 mils on byte lanes shorter than or equal to 5.7 inches.
2. Gradually increase trace width and spacing on byte lanes greater than 5.7 inches.

- Follow region 1 and 2 breakout recommendations from Figure 6-8.
- Transition to routing to DIMM pin field as soon as possible:
  - SDQ_A = 8 on 12 mils, SDQS_A = 8 on 15 mils
  - Maximize all SDQ_A/SDQS_A trace width and SDQS_A signal spacing as much as possible
- Routing to DIMM pin field: SDQ_A = 11 on 12 mils, SDQS_A = 11 on 17 mils.

Table 6-10. Data Signal Length Matching Guidelines

Parameter	Routing Guidelines
Trace Length B (DIMM Pin-to-Pin)	Length must be 200–600 mils, but with ≤ 200 mils variance between the longest and shortest trace segments for that channel
Trace Length C (Last DIMM Pin to Termination)	Max = 800 mils
MCH die to last DIMM pin One DIMM/channel: Length = P+A Two DIMM/channel: Length = P+A+ B	Max = 6.9”
Termination Resistor (Rtt)	56 Ω ± 5%
Max Via Count per Signal	Two vias (for bottom layer signals, one at MCH ballout and the other at termination, where needed).
SDQ_A Length Tuning	**Tuning to DIMM0** SDQ_A must be tuned to within ± 25 mils of their associated SDQS_A (see **Table 6-8** for SDQS_A mapping) from MCH pad to DIMM0 pin. **Tuning to DIMM1** SDQ_A must be tuned to within ± 25 mils of their associated SDQS_A (see **Table 6-8** for SDQS mapping) from MCH pad to DIMM1 pin.
DQS Length Tuning (Length = P+A)	SCMDCLK_A[2:0] = X (Xmin – 2.1 inches) ≤ SDQS_A ≤ (Xmax +1.5 inches) All lengths include both package and motherboard trace lengths.
DQS Length Tuning (Length = P+A+B)[1]	SCMDCLK_A[5:3] = Y (Ymin – 2.1 inches) ≤ SDQS_A ≤ (Ymax +1.5 inches) All lengths include both package and motherboard trace lengths.

1. Refer to Figure 6-9 through Figure 6-11

Figure 6-9. Data Signal Length Matching Topology

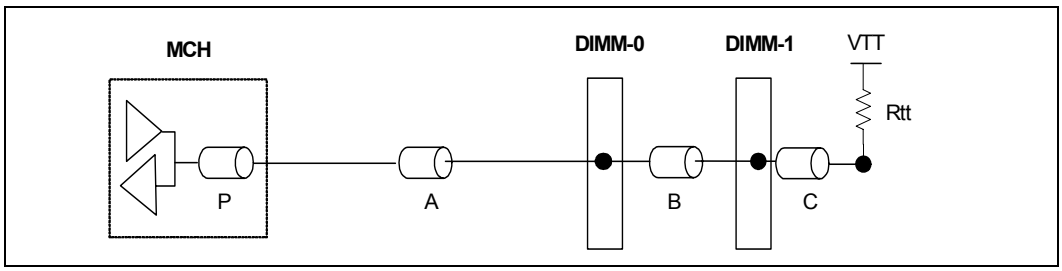


Figure 6-10. Data Strobe Length Matching Requirements to DDR Clock

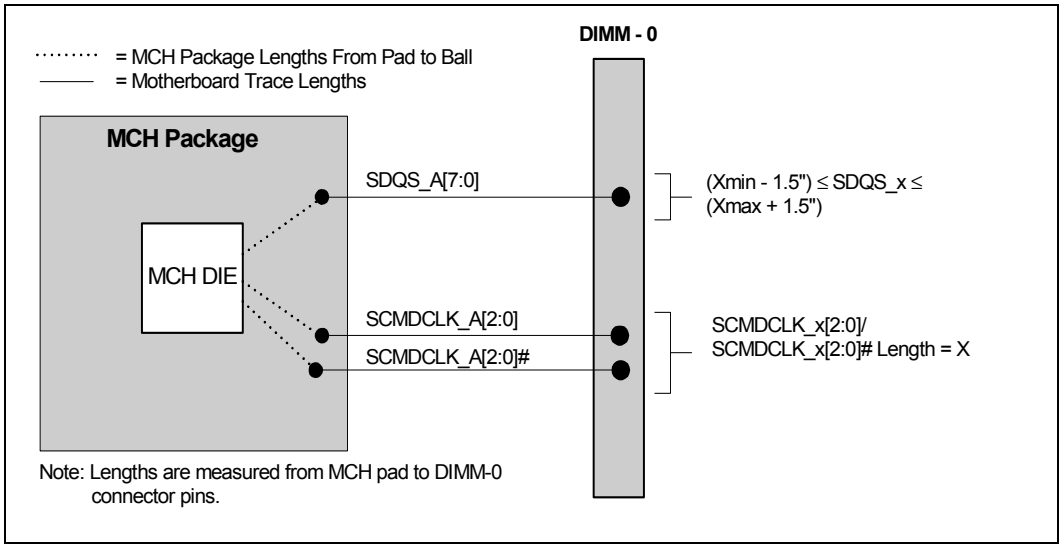
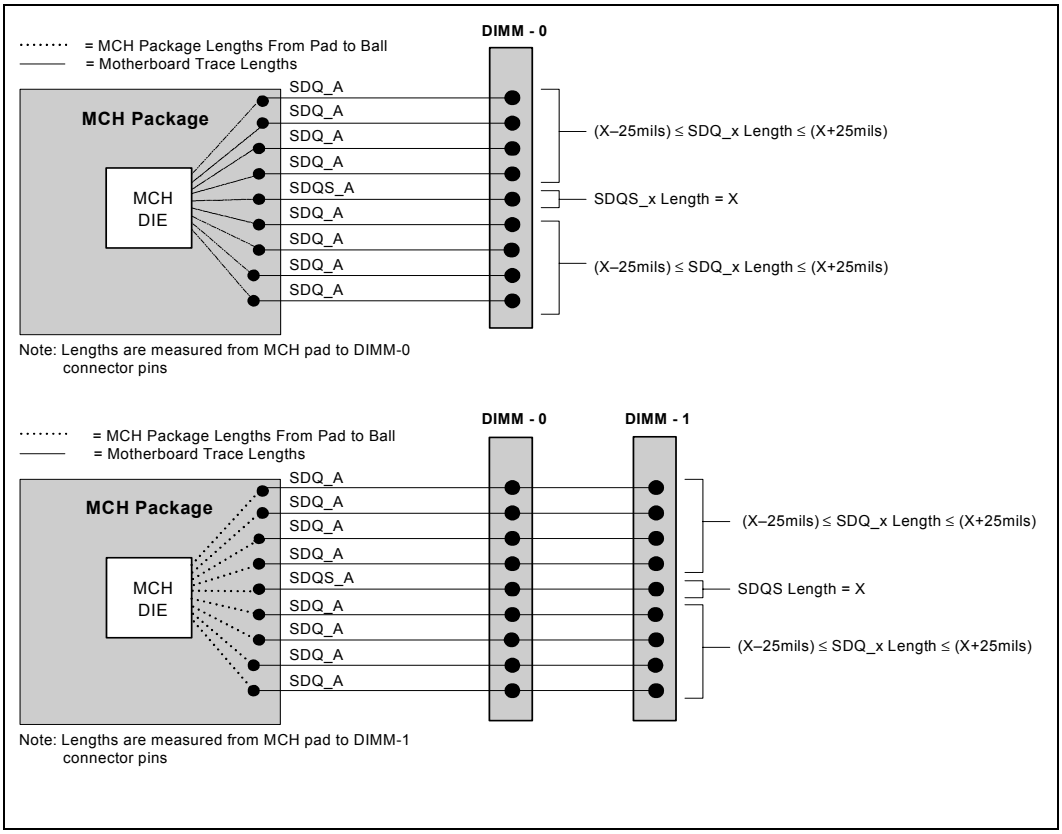


Figure 6-11. Data Signal Length Matching Requirements to Data Strobe



6.2.5 Control Signals (SCKE_A[3:0]#, SCS_A[3:0]#)

The MCH control signals that include the enable (SCKE_A) and chip select (SCS_A#) are source-clocked signals. One SCKE_A and SCS_A# are needed per row. SCKE_A and SCS_A# are tuned to SCMDCLK_A.

Table 6-11. Control Signal to DIMM Mapping

Control Signal Mapping (per Channel)	Relative To
SCKE_A[1:0]	DIMM0
SCS_A[1:0]#	DIMM0
SCKE_A[3:2]	DIMM1
SCS_A[3:2}#	DIMM1

Table 6-12, Table 6-13, Figure 6-12, and Figure 6-13 show the recommended topology and layout guidelines for the DDR control signals.

Table 6-12. Control Signal Trace Width and Spacing Guidelines

Routing Region	Routing Guidelines (width on spacing)
Target Impedance	60 Ω ± 15%
MCH Breakout	5 on 5 up to a max of 550 mils
MCH to 1st DIMM (Region 1)	5 on 12
DIMM pin field (Region 2)	5 on 6
Termination (Region 3)	5 on 5

NOTE: This table refers to the routing regions defined in Figure 6-2.

Table 6-13. Control Signal Length Matching Guidelines

Parameter	Routing Guidelines
Trace Length B (DIMM Pin to Termination)	Max = 1.4 inches
Termination Resistor (Rtt)	47 Ω ± 5%
Max via count per signal	Two vias (if needed for bottom layer signals, one at MCH ball out and the other at termination).
Length Tuning Method (Length = package + motherboard trace length, L = P + A)	SCMDCLK_A = X (Xmin – 1.5 inches) ≤ Control ≤ Xmax All lengths include both package and motherboard trace lengths.

NOTE: Refer to Figure 6-12 and Figure 6-13.

Figure 6-12. Control Signal Length Matching Topology

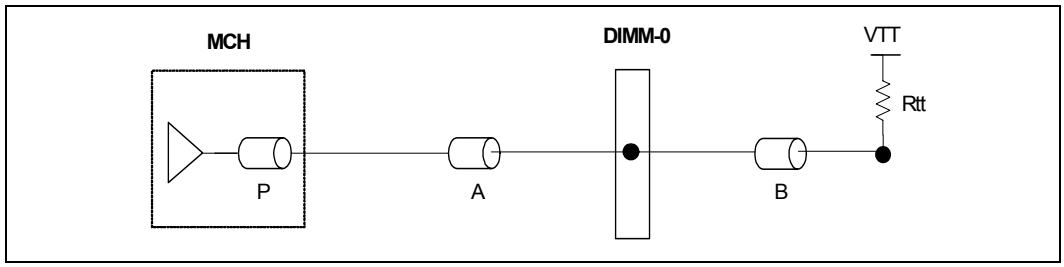
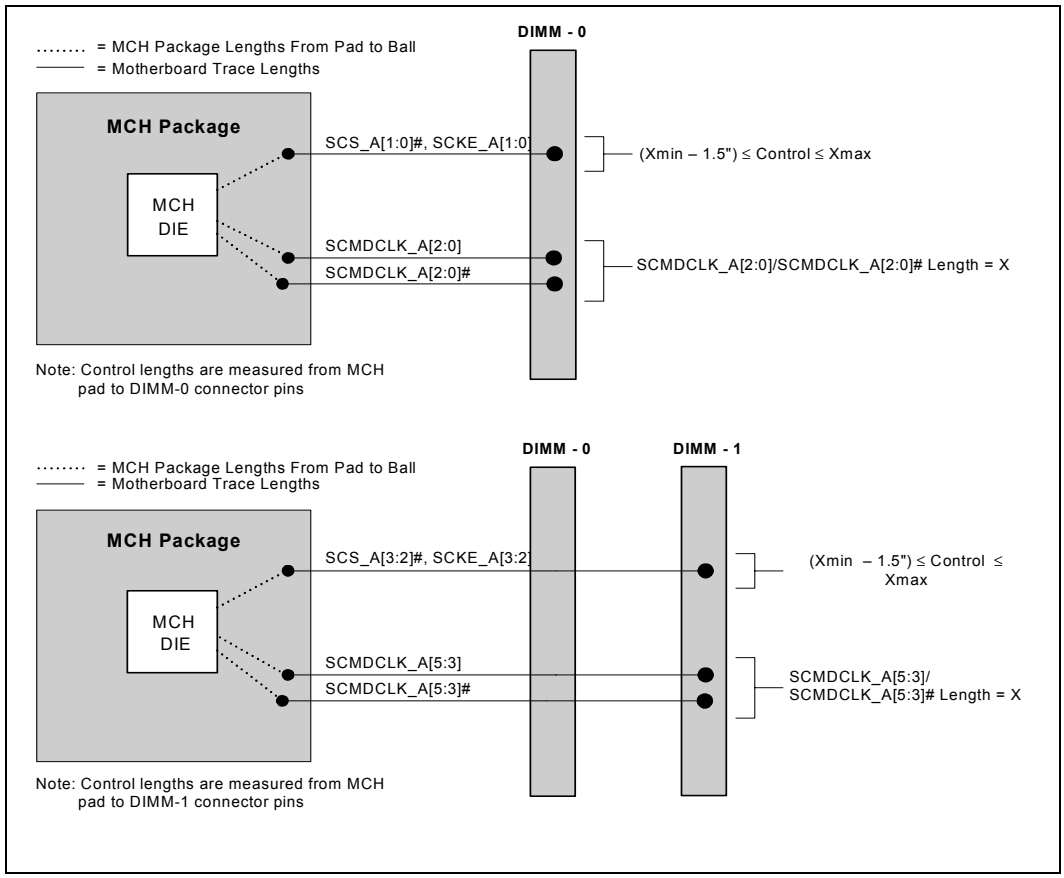


Figure 6-13. Control Signal Length Matching Requirements



6.2.6 CPC Address Signals (SMAA_A[5:1], SMAB_A[5:1])

The MCH CPC address signals are source-clocked signals that include SMAA_A[5:1] and SMAB_A[5:1]. CPC address signals should be kept as short as possible and must be tuned to SCMDCLK_A.

Table 6-14. CPC Address to DIMM Mapping per Channel

SMAA_A/SMAB_A	DIMM
SMAA_A[5:1]	DIMM0
SMAB_A[5:1]	DIMM1

Table 6-15, Table 6-16, Figure 6-14, and Figure 6-15 show the recommended topology and layout routing guidelines for the DDR CPC address signals.

Table 6-15. CPC Address Trace Width and Spacing Guidelines

Routing Region	Routing Guidelines (width on spacing)
Target Impedance	50 Ω ± 15%
MCH Breakout	5 on 5 up to a max of 550 mils
MCH to First DIMM (Region 1)	7 on 12
DIMM pin field (Regions 2)	5 on 5
Termination (Regions 3)	5 on 5

NOTE: This table refers to the routing regions defined in Figure 6-2.

Table 6-16. CPC Address Signals Length Matching Guidelines

Parameter	Routing Guidelines
Trace Length B (DIMM pin to Termination)	Max = 1.4 inches
Termination Resistor (Rtt)	47 Ω ± 5%
Max via count per signal	Two vias (for bottom layer signals, one at MCH ballout and the other at termination).
Length Tuning to DIMM 0 (Length = P + A)	SCMDCLK_A = X CPC < 3.7": CPCmax ≤ Xmax – 1.1" 3.7" < CPC < 4.7": CPCmax ≤ Xmax – 1.7" CPCmin = CPCmax (theoretical based on Xmin) – 2.5"
Length Tuning to DIMM 1 (Length P + A)	SCMDCLK_A = Y CPC < 3.7": CPCmax ≤ Ymax – 1.1" 3.7" < CPC < 4.7": CPCmax ≤ Ymax – 1.7" CPCmin = CPCmax (theoretical based on Ymin) – 2.5"

Figure 6-14. CPC Address Length Matching Topology

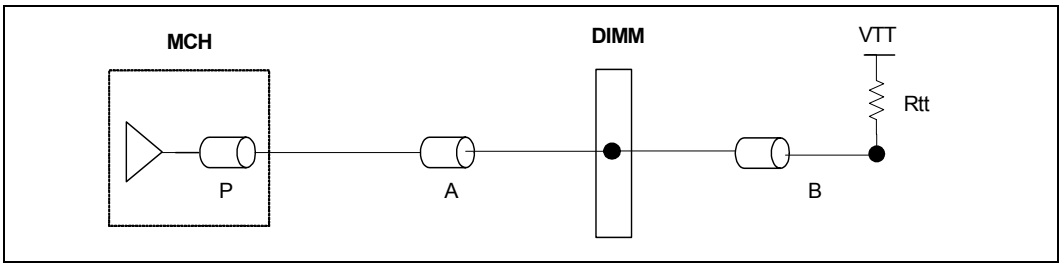
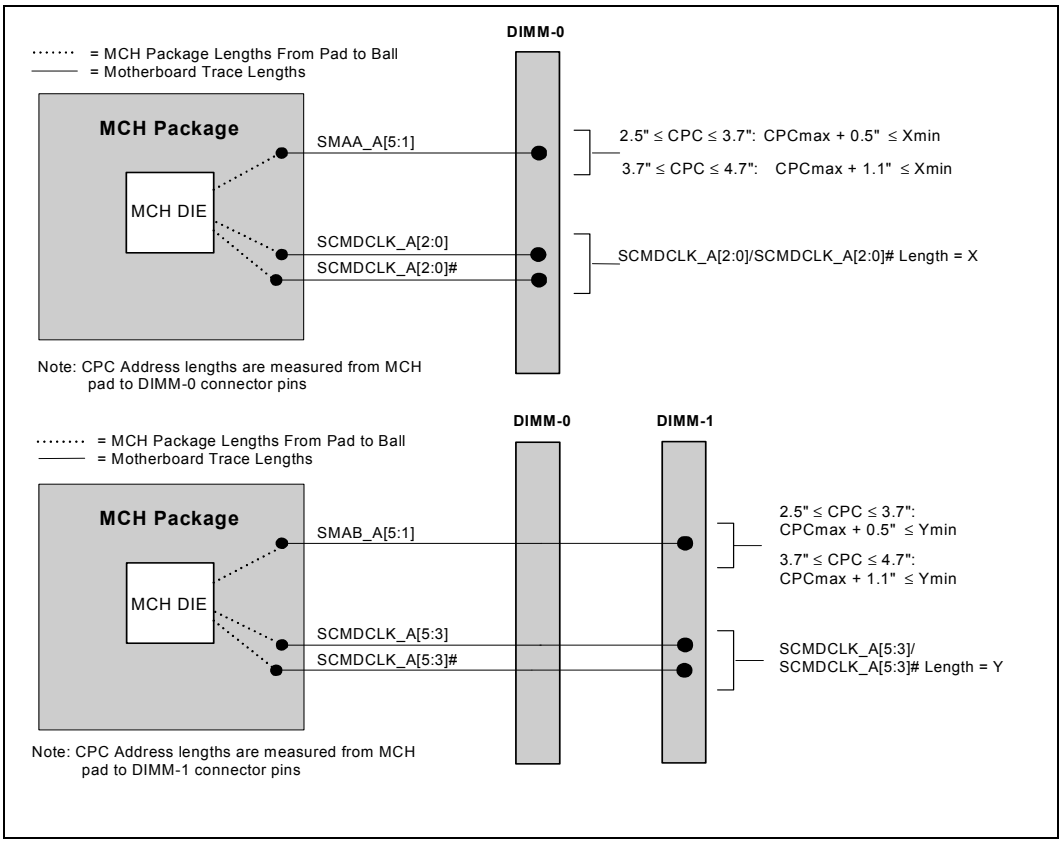


Figure 6-15. CPC Address Length Matching Requirements



6.3 DDR Reference Voltage

The DDR system memory reference voltage (VREF) is used by the DDR devices to compare the input signal levels of the data, command and control signals, and is also used by the MCH to compare the input data signal levels.

Two VREF circuits are used to generate the VREF voltage for the DDR interface. One for the MCH and one for the DDR channel at the DIMMs.

6.3.1 DDR VREF at the MCH

On the MCH there are two VREF pins (SMVREF_A and SMVREF_B). These two pins are connected inside the package. As such, only one of these pins requires a VREF voltage divider; the other should be decoupled.

On the reference design, the VREF circuitry is attached to SMVREF_B and the decoupling is attached to SMVREF_A. The VREF divider is shown in Figure 6-16. It should be generated from a typical resistor divider using 1% tolerance resistors. The VREF resistor divider should be placed no further than 1.0 inch from the SMVREF pin being used. The VREF signal should be routed with as wide a trace as possible (12 mils minimum width) and isolated from other signals with a minimum of 12-mils spacing. In the MCH breakout a 7-mil trace may be used, if needed, for up to a maximum length of 350 mils.

Figure 6-16. DDR VREF Generation Example Circuit at the MCH

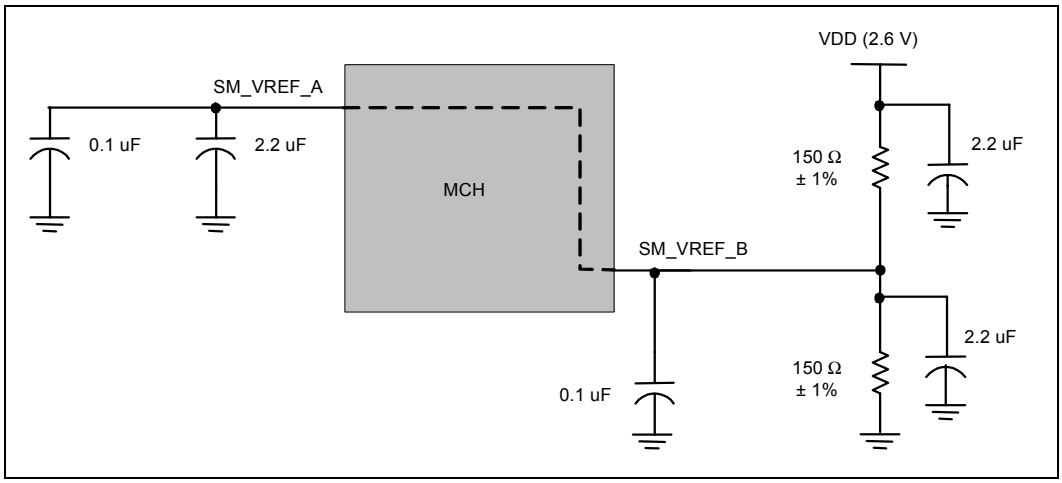


Table 6-17. DDR VREF Generation Requirements at the MCH

Parameter	Guideline
VREF Routing	Minimum 12-mils wide and separated from other traces by a minimum of 12-mils spacing, except during breakout that allows for 7-mil spacing to other signals for no more than 350 mils.
Voltage Divider	Place resistor divider consisting of two 150 Ω 1% resistors within 1.0 inch of the MCH pin being used.
Decoupling at the resistor divider	Two 2.2 µF capacitors. Place one 2.2 µF capacitor between SM_VREF and ground and the other between VDD (2.6 V) and ground. **NOTE:** The 2.2 µF capacitor between VDD (2.6 V) and ground is only need if no other decoupling on the 2.6 V plane is near by.
Decoupling at SM_VREF source pin	Place one 0.1 µF capacitor as close as possible to the MCH SM_VREF source pin.
Decoupling for un-used SM_VREF pin	Place two capacitors, a 2.2 µF and a 0.1 µF, on the unsourced SM_VREF pin.

6.3.2 DDR VREF at the DIMMs

A separate DDR VREF circuit is needed for the DDR channel at the DIMMs. The VREF divider is shown in Figure 6-17. It should be generated from a typical resistor divider using 1% tolerance resistors. The VREF resistor divider should be placed no further than 1.0 inch from the VREF pin being used. The VREF signal should be routed with as wide a trace as possible (12 mils minimum width) and isolated from other signals with a minimum of 12-mils spacing.

Figure 6-17. DDR VREF Generation Example Circuit at the DIMMs

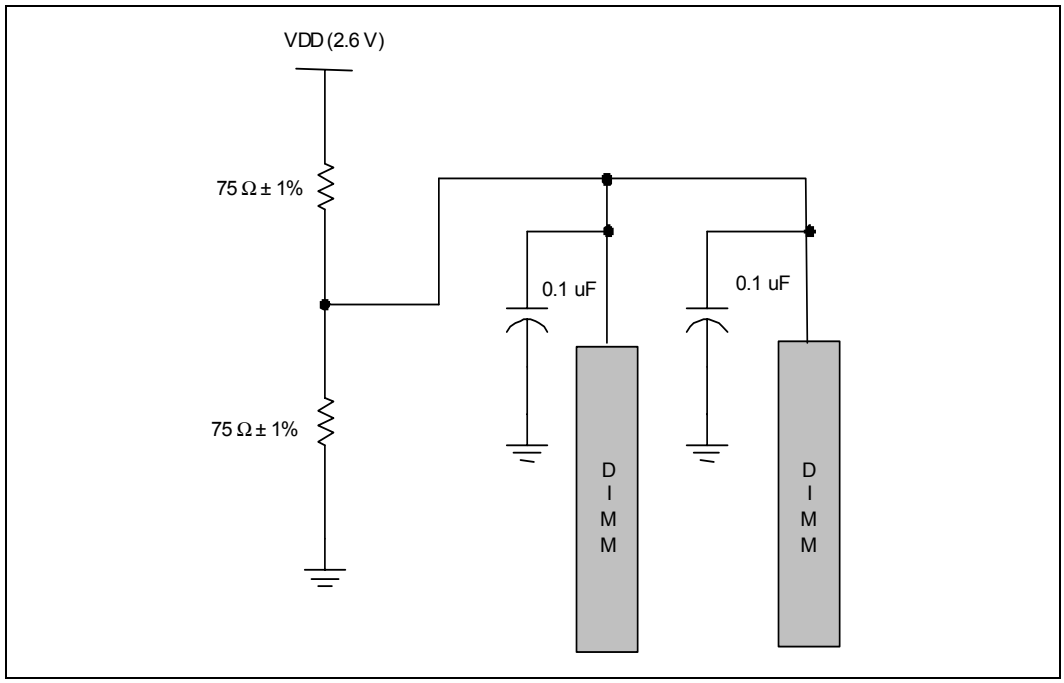


Table 6-18. DDR VREF Generation Requirements at the DIMMs

Parameter	Guideline
VREF Routing	Minimum 12-mils wide and separated from other traces by a minimum of 12-mils spacing.
Voltage Divider	Place resistor divider consisting of two 75 Ω 1% resistors within 1.0 inch of the DIMM connectors.
Decoupling at the resistor divider	Two 0.1 µF capacitors. Place one 0.1 µF capacitor as close as possible to each DIMM VREF pin.

6.4 DDR Resistive Compensation (SMRCOMP) per-Channel

The MCH uses a compensation signal to adjust the system memory buffer characteristics over temperature, process, and voltage variations. The DDR system memory compensation (SMRCOMP) must be connected to the VDD (2.6 V) rail through a 42.2 Ω ± 1% resistor and one 2.2 µF capacitor to ground as shown in Figure 6-18. Place the resistor and capacitor within 1.0 inch of the MCH package; however, they should be placed as close as possible to the MCH. The compensation signal and the VDD trace should be routed a minimum of 12-mils wide and isolated from other signals with a minimum of 10-mils spacing.

Figure 6-18. DDR (SMRCOMP) Resistive Compensation

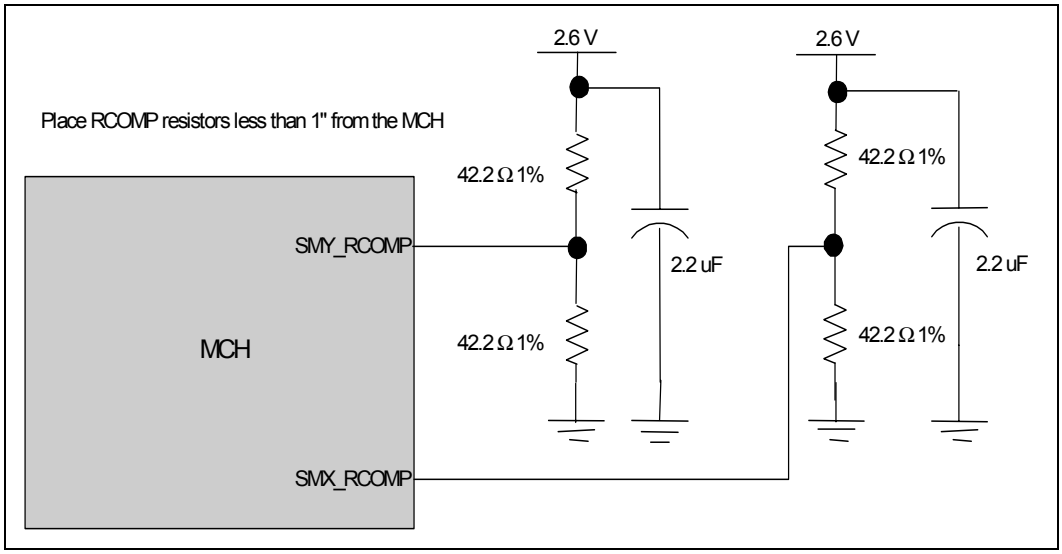


Table 6-19. DDR SMRCOMP Requirements

Parameter	Guideline
RCOMP Resistors	42.2 Ω 1% pulled to VDD (2.6 V); place resistors within 1.0 inch of the MCH.
RCOMP Routing	Minimum trace width of 12 mils and minimum spacing from other signals of 10 mils.
Decoupling	Decouple each RCOMP circuit as shown in Figure 6-18 with 2.2 µF capacitors.

Figure 6-19. DDR RCOMP VOH and VOL Circuitry

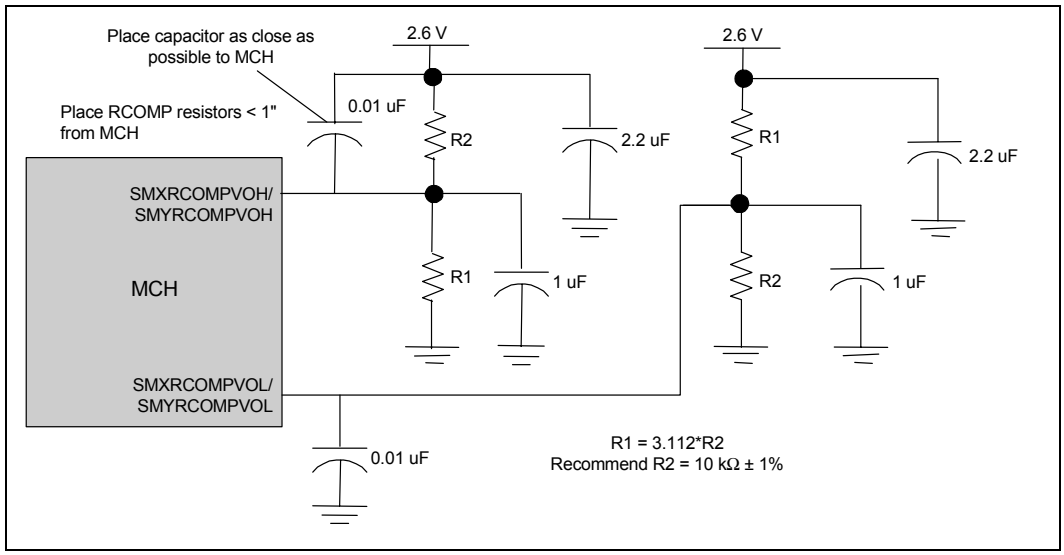


Table 6-20. DDR RCOMP VOH and VOL Requirements

Parameter	Guideline
Nominal RCOMPVOH	Nominal VOH = 1.89 V ± 2%
Nominal RCOMPVOL	Nominal VOL = 0.61 V ± 2%
RCOMP Resistors	R1 = 3.112*R2, Recommend R2 = 10 kΩ ± 1%
RCOMP Routing	Minimum trace width of 12 mils and minimum spacing from other signals of 10 mils.
Decoupling	Place the 0.01 µF capacitors no more than 1 inch from the MCH; place the 1 µF and 2.2 µF capacitors at the resistor divider.

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Hub Interface 7

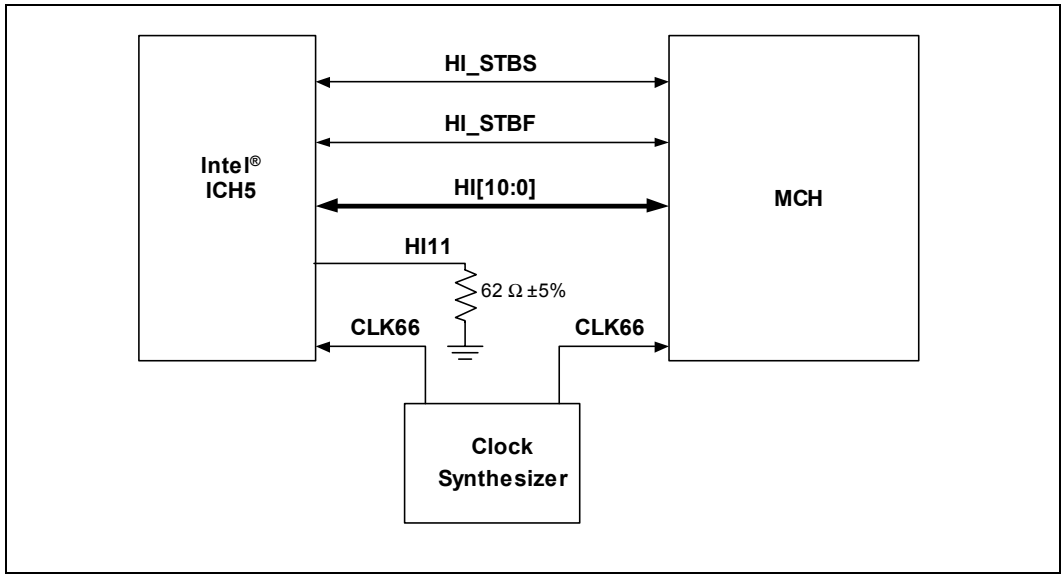
The MCH and ICH5 ballout assignments have been optimized to simplify the hub interface routing between these devices. It is recommended that the hub interface signals be routed directly from the MCH to the ICH5 with all signals referenced to VSS. Layer transition should be kept to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signals on the same layer.

The hub interface signals are broken into two groups: strobe signals (HI_STB) and data signals (HI). For the 8-bit hub interface, HI[10:0] are associated with HI_STBS and HI_STBF.

Note: The hub interface strobe signal names are slightly different between the ICH5 and MCH. On the ICH5, the signals are called HI_STBS and HI_STBF. On the MCH, these signals are called HISTRS and HISTRF. Unless otherwise specified, the strobe signal names HI_STBS and HI_STBF will be used throughout this chapter.

Note: The hub interface signal HI11 is an ICH5 only signal and does not exist on the MCH. This ICH5 signal should be terminated to VSS through a 62 Ω ± 5% resistor.

Figure 7-1. Hub Interface Routing Example



7.1 Hub Interface Routing Guidelines

This section documents the routing guidelines for the hub interface. This hub interface connects the ICH5 to the MCH. The ICH5 should strap its HICOMP pin to 1.5 V. The trace impedance must equal 60 Ω ± 15%.

Figure 7-2. Hub Interface Signal Routing Topology

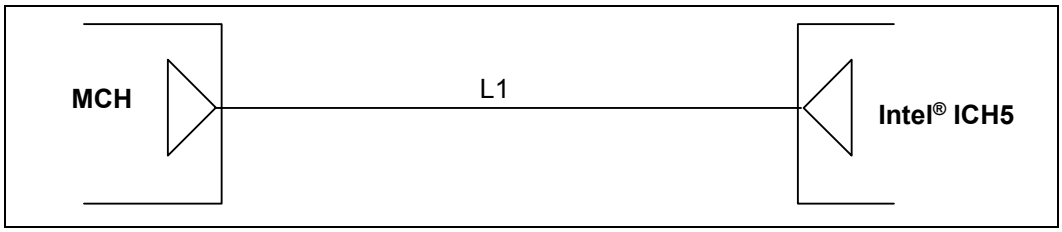


Table 7-1. Hub Interface Routing Parameters

Parameters	Routing Guidelines	Notes
Group	Hub Interface	
Topology	Point-to-Point	
Reference Plane	Ground referenced (contiguous over entire length)	
Characteristic Trace Impedance (Z_0)	60 Ω ± 15%	
Trace Width	5 mils	
Trace spacing	15 mils	
L1	2 inches to 10 inches	1
MCH Breakout	5 on 5 for 2 inches MAX	
Intel® ICH5 Breakout	5 on 5 for 0.3 inch MAX	
Strobe -to-Strobe length matching Data-to-Data length matching	WIthin 100 mils	
Strobes-to-Data length matching	Within 100 mils	

NOTES:
1. L1 also includes MCH and the ICH5 breakout length.

Using the recommended stack-up, the HI data signal traces must be routed 5 mils wide. There must be 15-mils spacing between traces (5 on 15). To break out of the MCH the HI data signals can be routed 5 on 5 for a distance of up to 2 inches maximum. To break out of the ICH5 the HI data signals can be routed 5 on 5 for a distance of up to 0.3 inch maximum. Again, all hub interface signals should be continuously referenced to GND.

The strobes, HI_ STBF and HI_STBS should be routed next to each other to reduce the coupling on the strobes. The hub interface must be tuned to within 100 mils, this includes all hub interface signals.

7.1.1 Hub Interface Signal Referencing

The hub interface signal traces (HI[10:0]) and the two hub interface strobe signals (HISTRF/ HISTRS) must all be referenced to ground to insure proper noise immunity.

7.1.2 Hub Interface HIVREF/HISWING Generation/Distribution

HIVREF is the hub interface reference voltage. The ICH5 uses HISWING to control voltage swing and impedance strength of the hub interface buffers. The HIVREF and HISWING voltage requirement and associated resistor/capacitor recommendations for the voltage divider circuit are listed in the Table 7-2.

Table 7-2. Hub Interface HIVREF/HISWING Generation Circuit Specifications

HIVREF Voltage Specification	HISWING Voltage Specification	Recommended Values for the HIVREF / HISWING Divider Circuit
350 mV ± 2% at 1.5 V nominal	800 mV ± 2% at 1.5 V nominal	R1 = 226 Ω ± 1%, R2 =147Ω ± 1% R3 = 113 Ω ± 1% C2 and C5 = 0.1 µF (near divider) C1, C3, C4, and C6 = 0.01 µF (near component)

NOTE: HIREF and HI_VSWING is derived from 1.5 V which is the nominal core voltage for the ICH5. Voltage supply tolerance for driver voltage must be within a ± 5% range of nominal.

In Figure 7-3 the resistor values, R1, R2, and R3, must be rated at 1% tolerance. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. Two 0.1 µF capacitors (C2, C5) should be placed close the divider. In addition, 0.01 µF bypass capacitors (C1, C3, C4, C6) should be placed within 0.25 inch of the component HIVREF/VREF pin (for C3 and C4) and HISWING pin (for C1 and C6). The maximum distance from divider to device should be as close as possible, to a maximum of 4 inches. Normal care needs to be taken to minimize crosstalk to other signals (< 10–15 mV). If the single HIVREF/HISWING divider circuit is located more than 4 inches away, then the locally generated reference divider should be used. In Figure 7-3 is an example of a shared single HIVREF/HISWING divider circuit. In Figure 7-4 a local generated HIVREF/HISWING generation circuit is shown. This can be used for either the MCH or the ICH5.

Figure 7-3. Hub Interface Single HIVREF/HISWING Generation Circuit

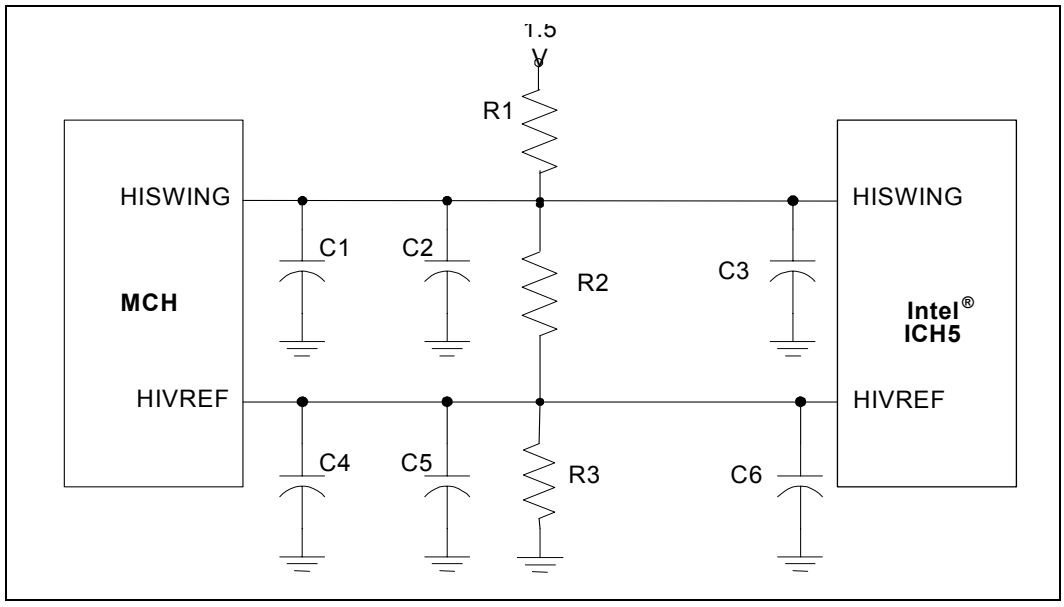
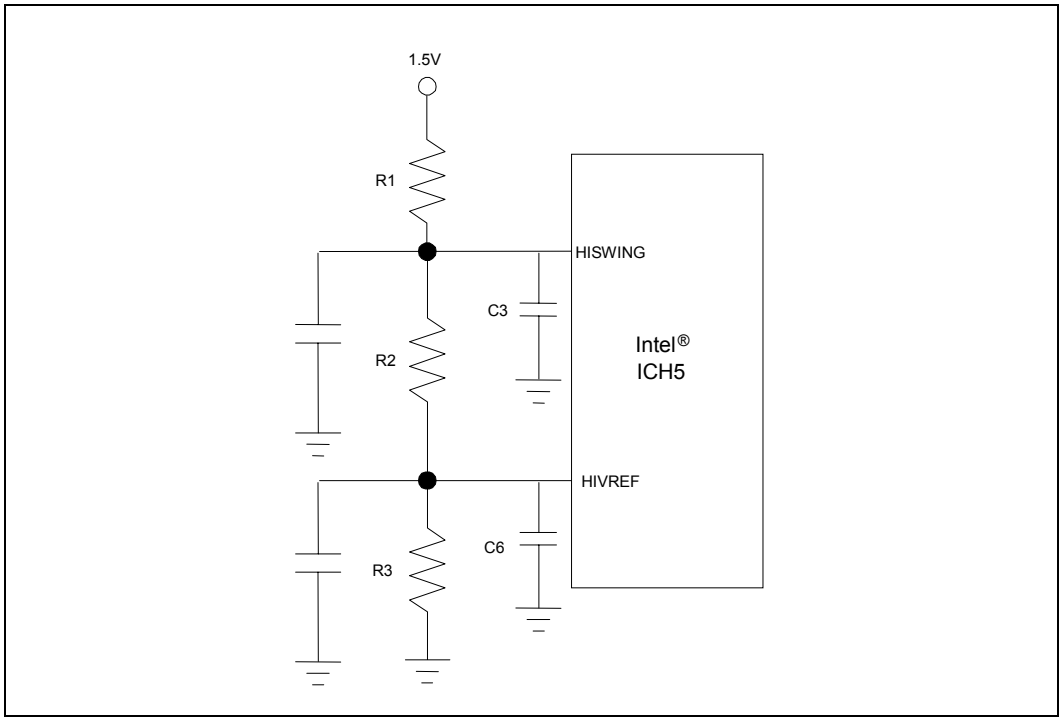


Figure 7-4. Hub Interface Local HIVREF/HISWING Generation Circuit (Intel® ICH5 Side)



7.1.3 Hub Interface Compensation

The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The hub interface requires Resistive Compensation (HICOMP).

Table 7-3. RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied to
Hub Interface	60 Ω ± 15%	HICOMP = 52.3 Ω ± 1%	VCC = 1.5 V
Intel® ICH5	60 Ω ± 15%	HICOMP = 52.3 Ω ± 1%	VCC = 1.5 V

7.1.4 Hub Interface Decoupling Guidelines

Refer to the Power Delivery chapter (Chapter 15)

Accelerated Graphics Port (AGP) 8

8.1 AGP 3.0

For AGP 2.0 mode, the peak bandwidth is 1066 MB/s and this is achieved by using a quad-clocked data transfer methodology. In AG P 3.0 (8X speed) mode the data is octal-pumped from the common clock frequency of 66 MHz achieving a peak bandwidth of 2.1 GB/s. To achieve these higher data rates across the standard AGP connector, AGP 3.0 mode uses a parallel-terminated bus with low signal swings of 0.8 V. The AGP 2.0 mode 1.5 V I/O power supply is used for backward compatibility for designs which wish to be universal low voltage. It is likely that a 0.25 µm or better technology will be required to meet the tight timing specifications.

8.1.1 AGP Interface Signal Groups

This section describes layout and routing guidelines to ensure a robust AGP interface design. These guidelines ensure that the AGP specifications can be met and that the motherboard will function properly. This solution is based on the reference platform. Other implementations of AGP routing may be used with proper simulation based on parameters specified in the design guide available at www.agpforum.org. Table 8-1 and Table 8-2 show the signal groups and associated strobes.

Table 8-1. Logical Signal Groups

Group	Signals	Signal Type
1	GAD[15:0], DBI_LO, GC#/BE[1:0], GADSTBF0, GADSTBS0	Source Synchronous
2	GAD[31:16], GC#/BE[3:2], DBI_HI, GADSTBF1, GADSTBS1	Source Synchronous
3	GSBA[7:0]#, GSBSTBF, GSBSTBS	Source Synchronous
4	GIRDY, GTRDY, GFRAME, SERR, PERR, GSTOP, GDEVSEL, GPAR	Common Clock
5	GRBF, GWBF, GREQ, GGNT	Common Clock

Table 8-2. Associated First and Second Strobes (Layout Routing Groups)

Group	Signals	1st Strobe	2nd Strobe
1	GAD[15:0], GC#/BE[1:0]	GADSTBF0	GADSTBS0
2	GAD[31:16], GC#/BE[3:2], DBI_HI, DBI_LO	GADSTBF1	GADSTBS1
3	GSBA[7:0]#	GSBSTBF	GSBSTBS

8.2 AGP 8X Implementations

8.2.1 Motherboard Layout Recommendations

The traces should be as short and direct as route length matching rules allow. Avoid changing the power plane reference during routing. Any change in reference plane will need to be bypassed by capacitors placed as close to the vias as possible. The power plane design should be considered during the entire design process and not left to the end. The planes should be cut so that the number of "neckdown" points are minimized.

8.2.2 AGP 8X Routing Guidelines

The AGP 8X signals must be routed directly from the MCH to the AGP connector with all signals referenced to ground. A consistent ground reference plane must be maintained. In addition, all signals within an address/data group must be routed on the same layer (see Table 8-2 for address/data groups). Table 8-3 summarizes the routing parameters for the AGP interface.

The 8X mode source synchronous signals and the 66 MHz clock signal should not cross any plane splits (crossing two separate voltage planes). If the common clock signals cross split planes, they should be simulated to ensure signal quality is not compromised.

Since the strobe signals (GADSTBF0, GADSTBS0, GADSTBF1, GADSTBS1, GSBSTBS, and GSBSTBF) act as clocks on the source synchronous AGP interface, special care should be taken when routing these signals.

Table 8-3. Motherboard Interconnect Requirements

Parameter	Min	Max	Units	Notes
Source Synchronous Signals (Groups 1, 2, and 3)				
Interconnect Length	0.5	3.5	inches	2
Strobe-to-Strobe (Interconnect Mismatch)		5	mils	2
Strobe-to-Data (Interconnect Mismatch)		25	mils	3
Data-to-Data Spacing	3/1		S/H	4
Strobe-to-Strobe Spacing	5/1		S/H	4
Strobe-to-Data Spacing	5/1		S/H	4
Trace Impedance	51	69	Ω	
Connector Breakout		200	mils	10
MCH Breakout		550	mils	
Common Clock Signals (Groups 4 and 5)				
Interconnect Length	0.5	3.5	inches	2
Common Clock-to-Common Clock Spacing	2/1		S/H	4
Common Clock-to-Data Spacing	3/1		S/H	4
Common Clock-to-Strobe Spacing	5/1		S/H	4
Trace Impedance	51	69	Ω	
Connector Breakout		200	mils	10
MCH Breakout		550	mils	

NOTE: The AGP maximum trace length (3.5 inches) indicated in Table 8-3 applies to 3:1 space to height routing. Per the AGP 3.0 specification, if 4:1 space to height routing is used, the maximum length is 6 inches (see Figure 8-1).

Interconnect Notes

1. All interconnects must be ground referenced.
2. Worst-case interconnect skews listed in Table 8-3 are based on simulations that take into account likely layout topologies and a wide range of interconnect. Listed trace lengths include pin-to-trace breakout and trace-to-connector fan-in/out.
3. This mismatch budget applies to the combined trace lengths of the package **and** board signals. Further, note that the set of 16 data signals and the corresponding strobes, etc., must be routed on the same PCB layer(s).
4. Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane. Definitions for microstrip and described in subsequent text.
5. Sum of all interconnect skew contributors, including crosstalk, interconnect mismatch, etc., across the entire channel (including package and connector).
6. Propagation delay must account for all contributors up to the connector pins.
7. Effective impedance incorporates all coupling effects including crosstalk.
8. This represents the contribution to skew on the motherboard and includes **all** causes, not just interconnect.
9. Package information is added here for simple reference. Flip-chip packaging is highly recommended.
10. This is the fan-in/out length that does not follow the normal trace separation requirements in the connector area on the motherboard and the edge fingers of the graphic cards.

Table 8-3 gives the routing rules for the control signals and clock lines. There are no external pull-up or pull-down resistors for control signals on AGP 8X mode board design. The resistors are integrated inside the device buffers.

8.2.2.1 Length Matching Recommendation

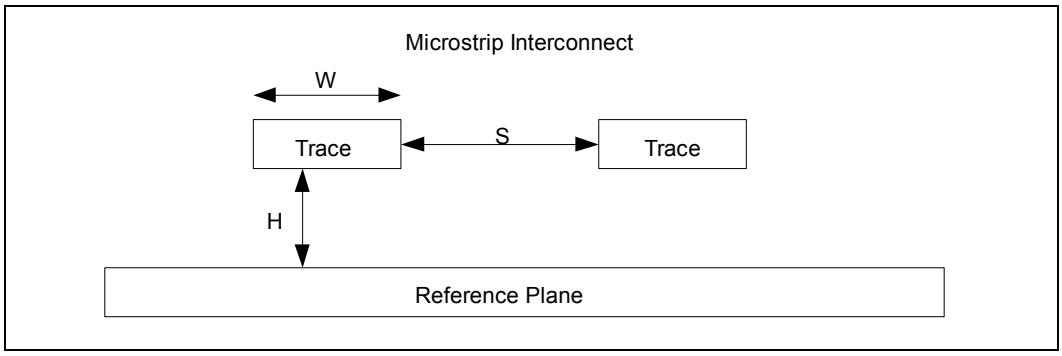
The data groups shown in Table 8-2 must match the strobes within 25 mils. First and second strobes must match within 5 mils. There are no requirements for length matching between groups and there are no length matching requirements for signals in groups 4 and 5.

8.2.2.2 Board Constraints

All AGP 3.0 mode source synchronous signals should be routed on a layer referenced to a ground plane. To minimize the effect of trace velocity difference between circuit board layers, the source synchronous signals within the same group should be routed on the same layer. The total number of trace via transitions should match within the group. Dummy vias should be used to match the total via count for each group.

In all cases, it is best to reduce the line length mismatch wherever possible to minimize timing variations. It is also best to separate the traces by as much as possible to reduce trace-to-trace coupling. The physical/electrical length matching requirements include compensation for the package length delta. For motherboard layouts, length matching is specified form pad to connector pins.

Figure 8-1. Spacing to Dielectric Height Diagram



8.2.3 AGP Signal Noise Decoupling Guidelines

8.2.3.1 1.5 V AGP Connector Decoupling

The designer should ensure that the AGP connector is well decoupled. The following recommendations are derived from the AGP Design Guide Revision 1.0, Section 1.5.3.3, *Connector AC Signal Decoupling Requirements*:

The decoupling capacitors recommendations for the AGP connector are intended to address AC signaling issues and not power delivery issues. The main reason for not addressing power delivery issues with the motherboard connector decoupling is due to the connector inductance and the distance the capacitors are from the graphic device. These two factors negate much of the usefulness of the connector decoupling on the motherboard for power delivery purposes. The following recommendations are for decoupling at the AGP connector on the motherboard:

- VCC3.3: Three 0.1 µF or larger, low-ESL capacitors; one 22 µF and one 100 µF electrolytic capacitor. Each capacitor should be placed as close as possible to a VCC3.3 pair of pins on the connector.
- 1.5 V core: Six 0.1 µF or larger, low-ESL capacitors; one 22 µF and two 100 µF tantalum capacitors. Each capacitor should be placed as close as possible to a 1.5 V core pair of pins on the connector.
- +5 V: One 0.1 µF or larger, low-ESL capacitor placed as close as possible to the +5 V connector pins.
- +12 V: One 0.1 µF or larger, low-ESL capacitors and one 470 pF electrolytic capacitor should be placed as close as possible to the +12 V connector pin.
- 3.3VAUX: One 0.1 µF or larger, low-ESL capacitor placed as close as possible to the 3.3VAUX connector pin(s).

8.2.4 Miscellaneous Signal Requirements

8.2.4.1 PERR

See Figure 8-2 for a PERR reference circuit. The circuit will supply pull-down to ground during AGP 3.0 mode operation and a pull-up to 1.5 V during AGP 2.0 mode operation.

8.2.4.2 AGP 2.0 and AGP 3.0 Mode Detection

Two new signals are provided in the AGP 3.0 specification to allow for detection of an AGP 3.0 capable graphics card by the motherboard and an AGP 3.0 capable motherboard by the graphics card respectively.

- GC_DET#: Pulled low by an AGP 3.0 graphics card; left floating by an AGP 2.0 graphics card
- MB_DET#: Pulled low by an AGP 3.0 motherboard; left floating by an AGP 2.0 motherboard.

The MCH uses GC_DET# to determine whether to generate VREF of 0.75 V (floating GC_DET# for AGP 2.0 graphics card), or 0.35 V (GC_DET# low) to the graphics card. This is sent to the graphics card via the VREFCG pin on the AGP connector.

There are two recommended implementation options for using GC_DET# for AGP 2.0 and AGP 3.0 modes of operations as illustrated in Figure 8-2 and Figure 8-3. Figure 8-2 is preferred since the FET allows tighter tolerance on the GVREF/GVSWING signals. The sum of the FET Ron and resistor should be approximately 45 Ω.

Figure 8-2. AGP Mode Detection Circuit (Option 1)

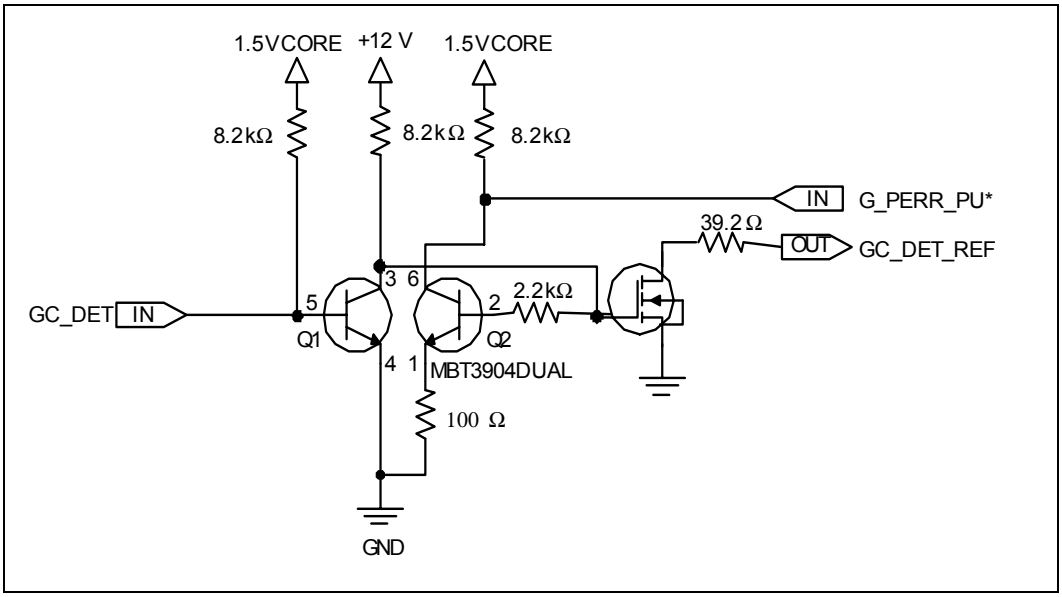
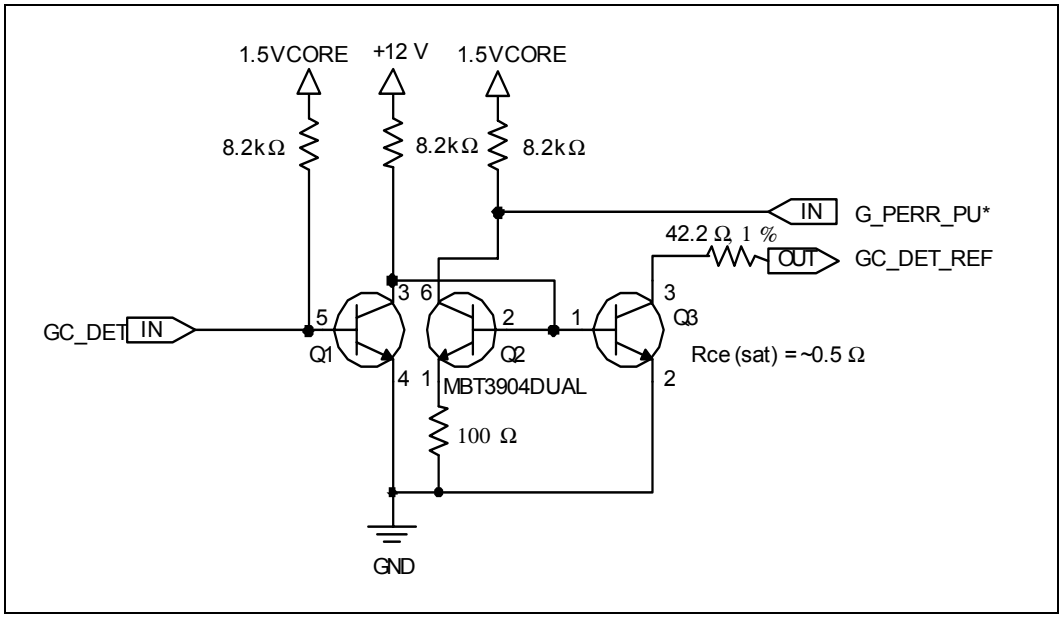


Figure 8-3 shows an optional circuit that does not require re-layout from the previous recommendation. BJTs with a narrow range for Rce have been found to be deterministic over process, voltage, and temperature. The impedance of the BJT Rce and the 42.2 Ω resistor must add up to ~45 Ω. The board designer must make sure the values are chosen such that the GVREF and GVSWING are within the AGP 2.0 and 3.0 specifications. An example part for the BJT in this circuit is the Philips PBSS4320T.

Figure 8-3. AGP Mode Detection Circuit (Option 2)



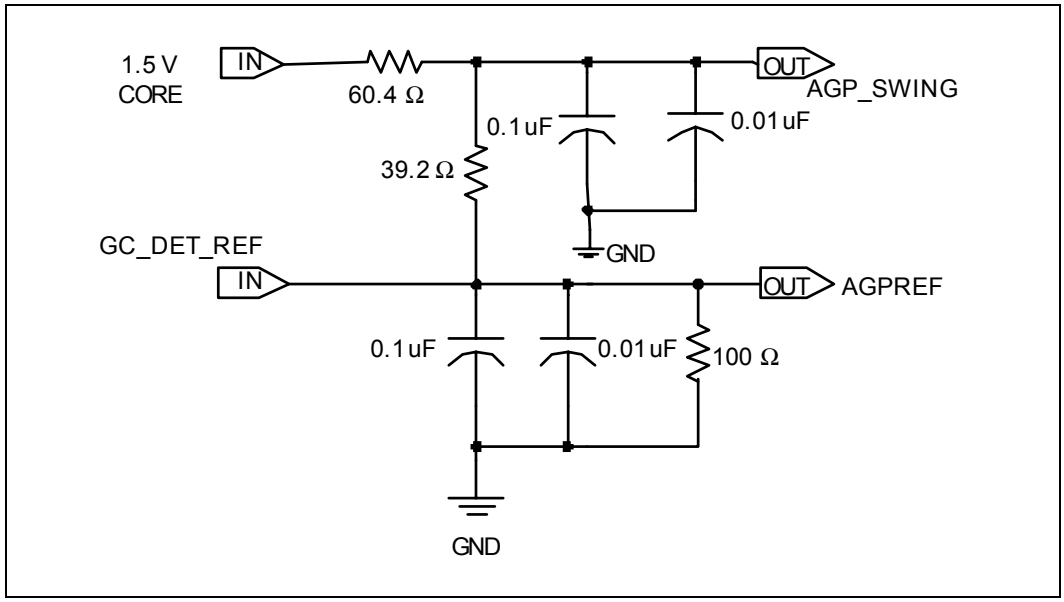
8.2.4.3 GRCOMP

These signals are used to calibrate the AGP buffers. The GRCOMP signals need to be pulled up to 1.5 V core through a 43.2 Ω ± 1% resistor.

8.2.4.4 GVREF

A complex VREF circuit is required to meet the reference voltage requirements for AGP 2.0 and AGP 3.0 modes. See Figure 8-4 for a complete detailed information.

Figure 8-4. GVREF/GSWING Circuit



8.2.4.5 GSWING

GSWING provides the reference voltages used by the GRCOMP circuits. GSWING is based on a resistor divider circuit and comes from 1.5 V. The voltage level is 0.8 V and is the maximum voltage for the AGP signal bus in AGP 3.0 mode.

It is important to place the 0.01 µF capacitors within 0.25 inch of the device pins (MCH, ICH5, and AGP), and to place the 0.1 µF capacitors close to the resistor circuit. See Figure 8-4 for details.

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CSA Port 9

This chapter of the design guide describes the layout guidelines when implementing the Communications Streaming Architecture(CSA) port on the 848P chipset. The CSA port is a dedicated 11-bit connection between the MCH and a Gigabit Ethernet (GbE) LAN controller, the 82547EI. The CSA port provides a theoretical bandwidth of 266 MB/s. The CSA port is a point-to-point interface; therefore, it can only support one device.

This chapter covers the CSA port connection to the 82547EI GbE controller. For CLK66 routing guidelines to the MCH and the GbE controller, refer to Section 4.2.

If the CSA port is not used, leave all the CSA interface signals disconnected on the MCH except CI_VREF, CI_SWING, and CI_RCOMP. See section Section 9.2 for CI_VREF and CI_SWING and Section 9.3 for CI_RCOMP details.

Note: There are minor differences in the corresponding signal names between the MCH and the Intel 82547EI GbE controller (see Table 9-1). For general discussions in this chapter, the 82547EI GbE controller signal name is used.

9.1 CSA Port Routing Guidelines

The following guidelines should be followed when the CSA interface is routed to the 82547EI GbE controller. The CSA Port signal groups are listed in Table 9-1.

Table 9-1. CSA Port Signal Groups

Group	Signals	
	MCH	Intel® 82547EI GbE Controller
Common Clock Signals	CI[10:8]	CI_[10:8]
Source Synchronous Signals	CI[7:0], CISTRF, CISTRS	CI_A[7:0], CI_STBF, CI_STBS
Miscellaneous Signals	CI_RCOMP, CI_SWING, CI_VREF	CI_RCOMP, CI_SWING, CI_VREF

Figure 9-1. CSA Port Signal Routing Topology

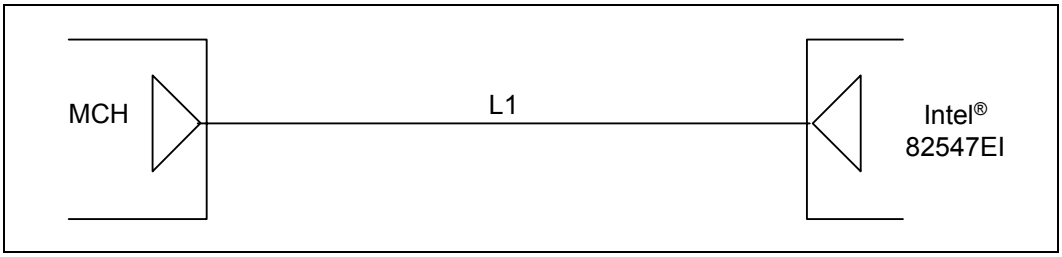


Table 9-2. CSA Port Routing Parameters

Parameters	Routing Guidelines	Notes
Group	CSA Port	
Topology	Point-to-Point	
Reference Plane	Ground referenced (contiguous over entire length)	
Characteristic Trace Impedance (Z_0)	60 Ω ± 15%	
Trace Width	5 mils	
Trace spacing	10 mils	
L1	2 inches to 10 inches	1
MCH Breakout	5 on 5 for 2 inches	
Intel® 82547EI GbE Controller Breakout	5 on 5 for 0.3 inch	
Strobe to Strobe Length Matching	Within 100 mils	
Strobes to Data Length Matching	Within 100 mils	

NOTES:
1. L1 also includes the MCH and the 82547EI GbE controller breakout length.

Using the recommended stack-up, the CSA port data signal traces must be routed 5 mils wide. There must be 15-mils spacing between traces (5/10). To break out of the MCH, the CSA port data signals can be routed 5/5 for a distance of up to 2 inches only. To break out of the 82547EI GbE controller, the CSA port data signals can be routed 5/5 for a distance of up to 0.3 inch only. Again, all CSA port should be continuously referenced to GND.

The strobes, CI_STBF and CI_STBS should be routed next to each other to reduce the coupling on the strobes. All CSA strobes and data signals should be tuned to within 100 mils.

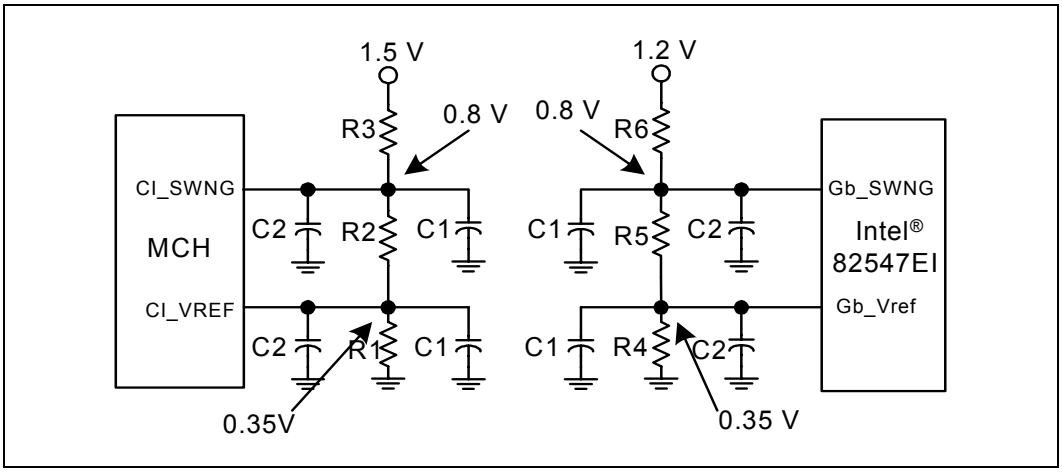
9.2 CSA Port Generation/Distribution of Reference Voltages

The 11-bit CSA port on the MCH has a dedicated CI_VREF pin to sample this reference voltage. The nominal CSA port reference voltage is 0.35 V ± 3%. In addition to the reference voltage, a reference swing voltage, CI_SWING must be supplied to control buffer voltage swing characteristics. The nominal CSA port reference voltage swing must be 0.8 V ± 3%. The 82547EI GbE controller also has a dedicated VREF and SWING pins. The reference voltage is 0.35 ± 3% and the swing voltage must be 0.8 V ± 3%.

Table 9-3. CSA Port Reference Circuit Specifications

Reference Voltage Specification	Reference Swing Voltage Specification	1.5 V Voltage Divider Circuit Recommended Resistor Values	1.2 V Voltage Divider Circuit Recommended Resistor Values
0.350 V ± 3%	For MCH and Intel® 82547EI GbE controller = 0.8 V ± 3%	R1 = 113 Ω ± 1% R2 = 147 Ω ± 1% R3 = 226 Ω ± 1%	R4 = 523 Ω ± 1% R5 = 665 Ω ± 1% R6 = 604 Ω ± 1%

Figure 9-2. CSA Port Locally Generated Reference Divider Circuits



The values of R1, R2, R3, R4, and R5 must be rated at ± 1% tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A 0.1 µF capacitor (C1 in Figure 9-2) should be placed within 0.5 inch to each resistor divider, and a 0.01 µF bypass capacitor (C2 in Figure 9-2) should be placed within 0.25 inch of reference voltage pins. If the length of the trace from the voltage divider to the pin is greater than 1 inch, place more than one 0.01 µF capacitor near the reference voltage pin. The trace length from the voltage divider circuit to the CI_REF and GB_REF pins must be no longer than 3.5 inches.

Both the voltage reference and voltage swing reference signals should be routed at least 10-mils wide and spaced at least 20 mils from all other signals.

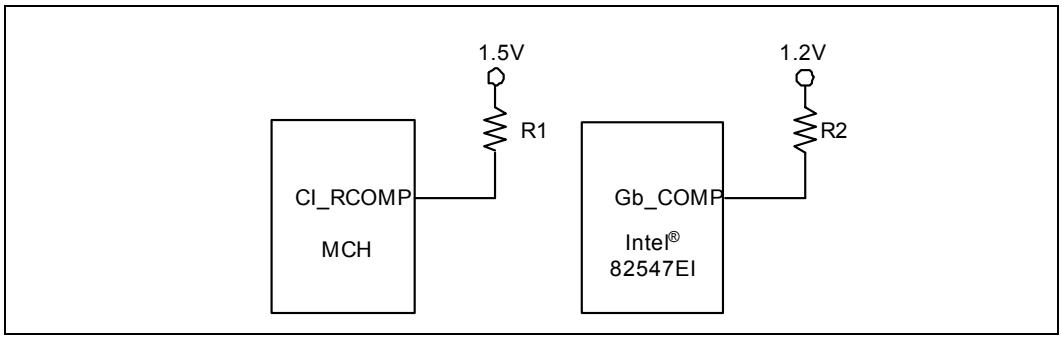
9.3 CSA Port Resistive Compensation

The CSA port uses a resistive compensation signal (RCOMP) to compensate buffer characteristics for temperature, voltage, and process.

Table 9-4. CSA Port RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
MCH	60 Ω ± 15%	R1 = 52.3 Ω ± 1%	VCC1.5
Intel® 82547EI GbE Controller	60 Ω ± 15%	R2 = 30.0 Ω ± 1%	VCC1.2

Figure 9-3. CSA Port RCOMP Circuits



9.3.1 Intel® 82547EI GbE Controller Layout Considerations

When implementing the CSA port on the 848P chipset platform, there are several options for LAN capability. The platform supports several components with footprint compatibility depending on the target market. Available LAN components with the same footprint include the 82547EI GbE controller and Intel 82562EZ/82562EX Platform LAN Connect (PLC) components. For design information on implementing a dual footprint LAN design or just a 82547EI GbE controller design, refer the *82562EZ(EX)/82547EI Dual Footprint Design Guide*.

Intel® ICH5 Layout/Routing Guidelines10

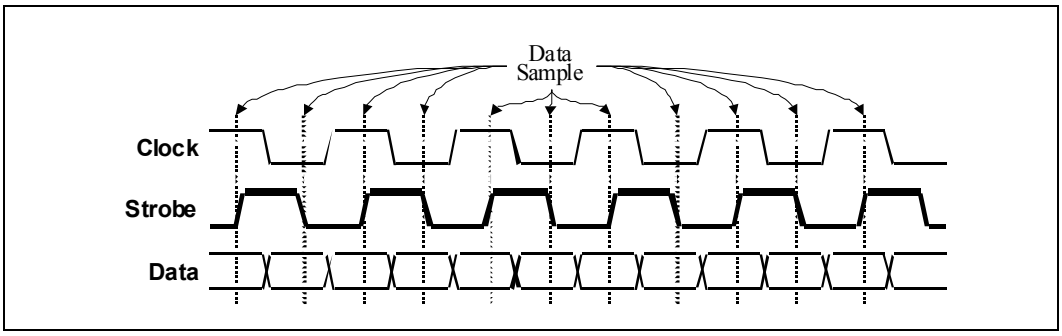
All recommendations in this section (except where noted) assume 5-mil wide traces. If trace width is greater than 5 mils, the trace spacing requirements must be adjusted accordingly (linearly).

10.1 Source Synchronous Strobing

Source synchronous strobing is one of the technologies used in the hub interface that allow very high data transfer rates. As buses get faster, and cycle times get shorter, the propagation delay is becoming a limiting factor in bus speed. Source synchronous strobing is used to minimize the impact of propagation delay (T_{prop}) on maximum bus frequency.

A source synchronous strobed interface uses strobe signals (instead of the clock) to indicate that data is valid. Refer to Figure 10-1 for an example.

Figure 10-1. Data Strobing Example



For a source synchronous strobed interface, it is very important that the strobe signals are routed carefully. These signals must be very clean (free of noise). Data signals are typically latched on the rising or falling edge of the strobe signal (or both). If there is noise on these signals, it could cause an extra “edge” to be detected, thus latching incorrect data. Refer to Figure 10-2 and Figure 10-3.

Figure 10-2. Correct Strobing Example (no noise)

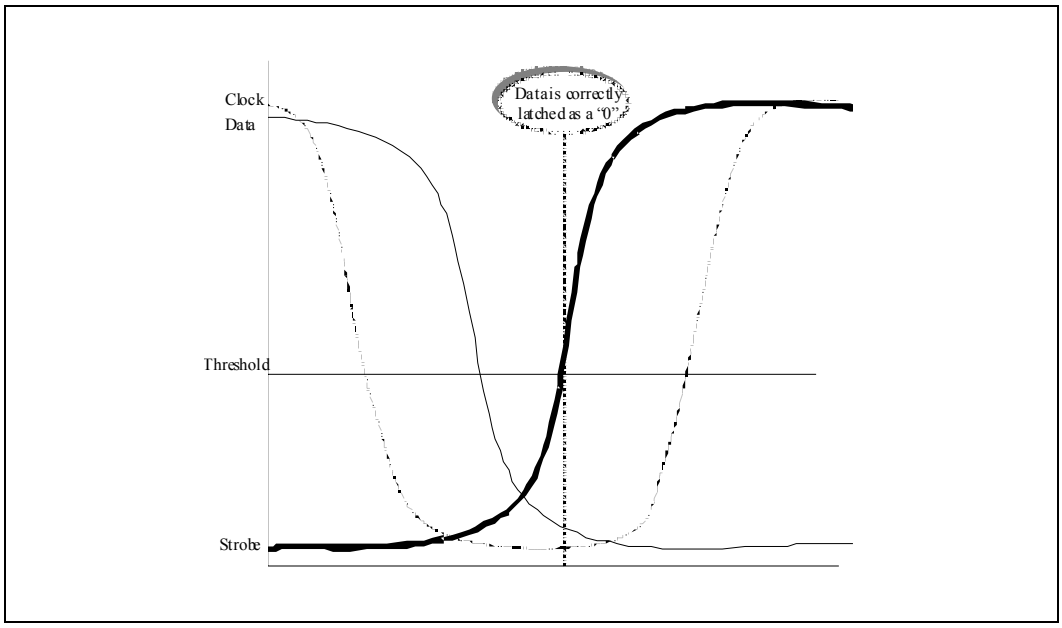
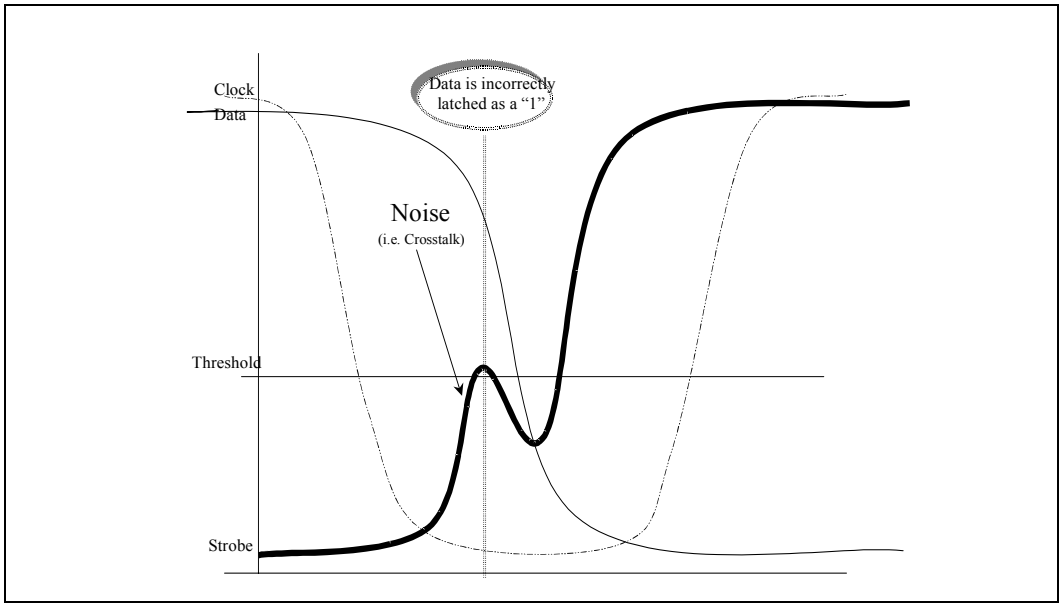


Figure 10-3. Effect of Crosstalk on Strobe Signal



When routing strobes and their associated data lines, trace length mismatch is very important (in addition to noise immunity). The primary benefit of source synchronous strobing is that the data and the strobe arrive at the receiver simultaneously. Thus, a strobe and its associated data signals have very critical length mismatch requirements. With accurately matched trace lengths (as well as matched impedance), the propagation delay for the strobe, and the propagation delay for the data will be very close. Hence, the strobe and the data arrive at the receiver simultaneously. For some interfaces, the trace length mismatch requirement is less than 0.25 inch.

10.2 IDE Interface

This section contains guidelines for connecting and routing the ICH5 IDE interface. The ICH5 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH5 has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date. If used, these resistors should be placed close to the connector.

Table 10-1. IDE Signal Groups

Signal Group	Primary	Secondary
Data	PDD[15:0]	SDD[15:0]
Strobes	PDIOR# (write), PIORDY (read)	SDIOR# (write), SIORDY (read)

The IDE interface can be routed with 5-mil traces on 7-mil spaces (dependent upon stack-up parameters), and must be less than 10 inches long (from ICH5 to IDE connector). Additionally, the maximum length difference between the data signals and the strobe signal (Table 10-2) of a channel is 500 mils.

Table 10-2. IDE Routing Summary

Trace Impedance	IDE Routing Requirements	Maximum Trace Length	IDE Signal Length Matching
60 Ω ± 15%	5 on 7 (Based on stack-up described in Chapter 3.)	10 inches	The two strobe signals must be matched within 100 mils of each other. The data lines must be within ± 450 mils of the average length of the two strobe signals.

10.2.1 Cabling

Length of Cable: Each IDE cable must be equal to or less than 18 inches.

Capacitance: Less than 35 pF.

Placement: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).

Grounding: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

10.3 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH5 IDE controller supports PIO, Multi-word (8237 style) DMA, and Ultra DMA modes 0 through 5. The ICH5 needs to determine the type of cable that is present to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra DMA modes greater than 2 (Ultra ATA/33). This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

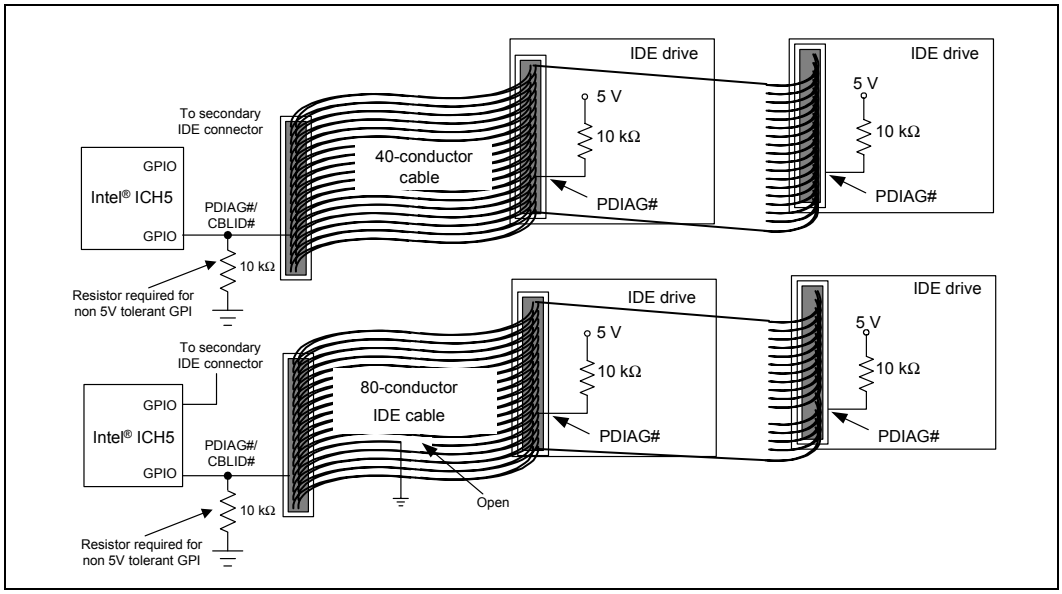
To determine if Ultra DMA modes greater than 2 (Ultra ATA/33) can be enabled, the ICH5 requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be done using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system, since this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side Detection mechanism only.

10.3.1 Combination Host-Side/Device-Side Cable Detection

Host side detection (described in the *ATA/ATAPI-6 Standard*) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 10-4. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. A 10 kΩ pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present and allows for use of a non-5 V tolerant GPIO.

Figure 10-4. Combination Host-Side/Device-Side IDE Cable Detection



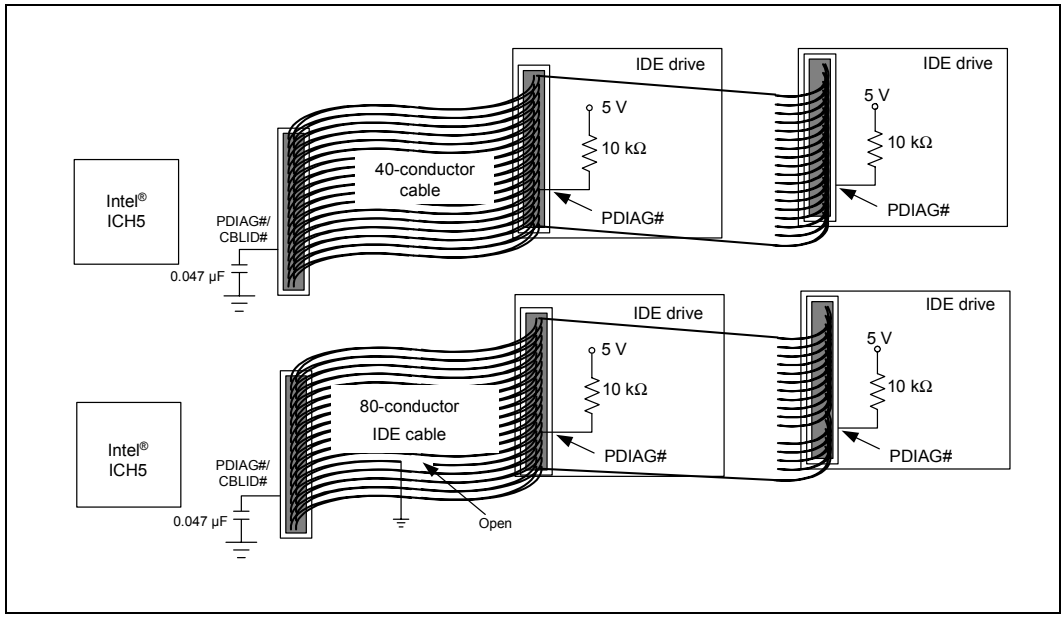
This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high, then there is 40-conductor cable in the system and Ultra DMA modes greater than 2 (Ultra ATA/33) must not be enabled.

If PDIAG#/CBLID# is detected low, then there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the *ATA/ATAPI-6 standard*. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13 is a 1, then an 80-conductor cable is present. If this bit is 0, then a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present, and notify the user of the problem.

10.3.2 Device-Side Cable Detection

For platforms that must implement Device-Side detection only (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in Figure 10-5. This capacitor should not be populated when implementing the recommended combination Host-Side/Device-Side cable detection mechanism described above. Note that some drives may not support device-side cable detection.

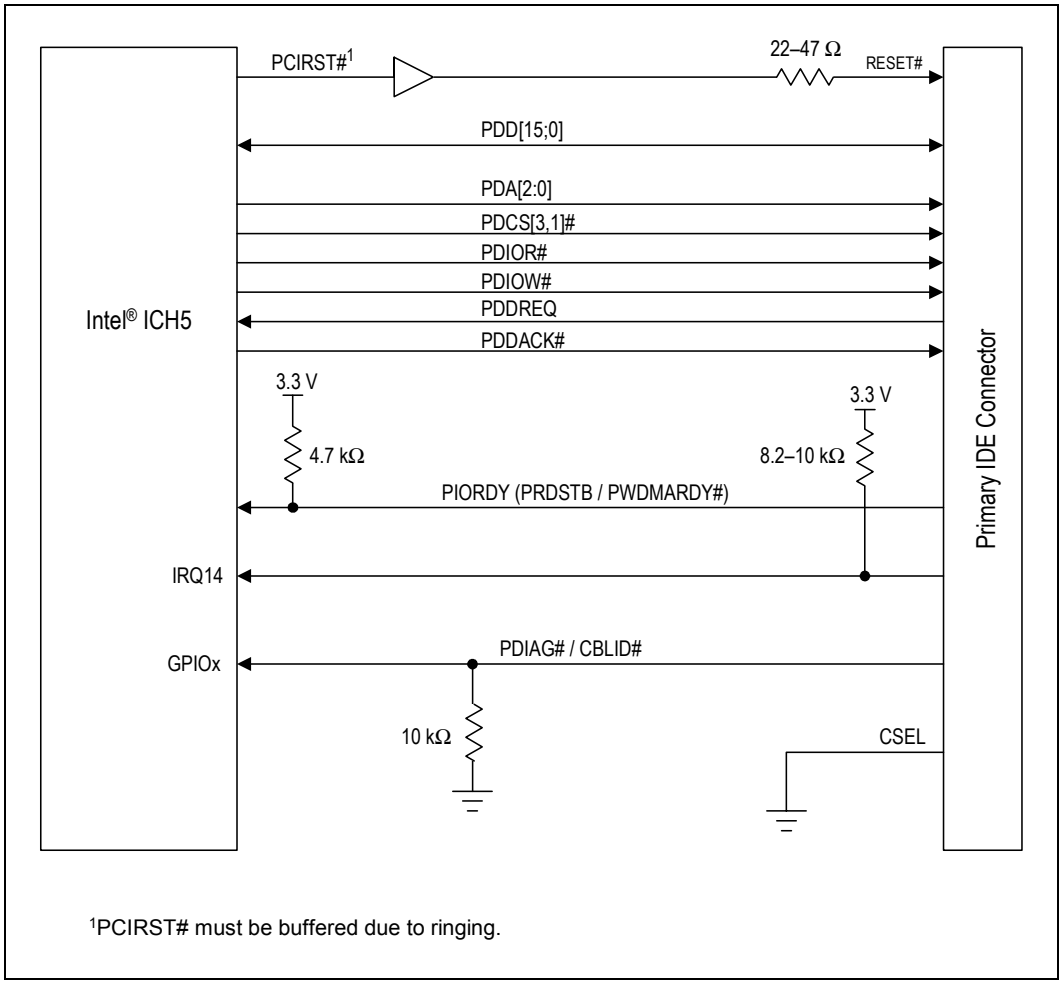
Figure 10-5. Device Side IDE Cable Detection



This mechanism creates a resistor-capacitor (RC) time constant. Drives supporting Ultra DMA modes greater than 2 (Ultra DMA/33) will drive PDIAG#/CBLID# low and then release it (pulled up through a 10 kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host and therefore the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host. Therefore, the signal will rise more slowly as the capacitor charges. The drive can detect the difference in rise times and it will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/ATAPI-4 Standard.

10.3.3 Primary IDE Connector Requirements

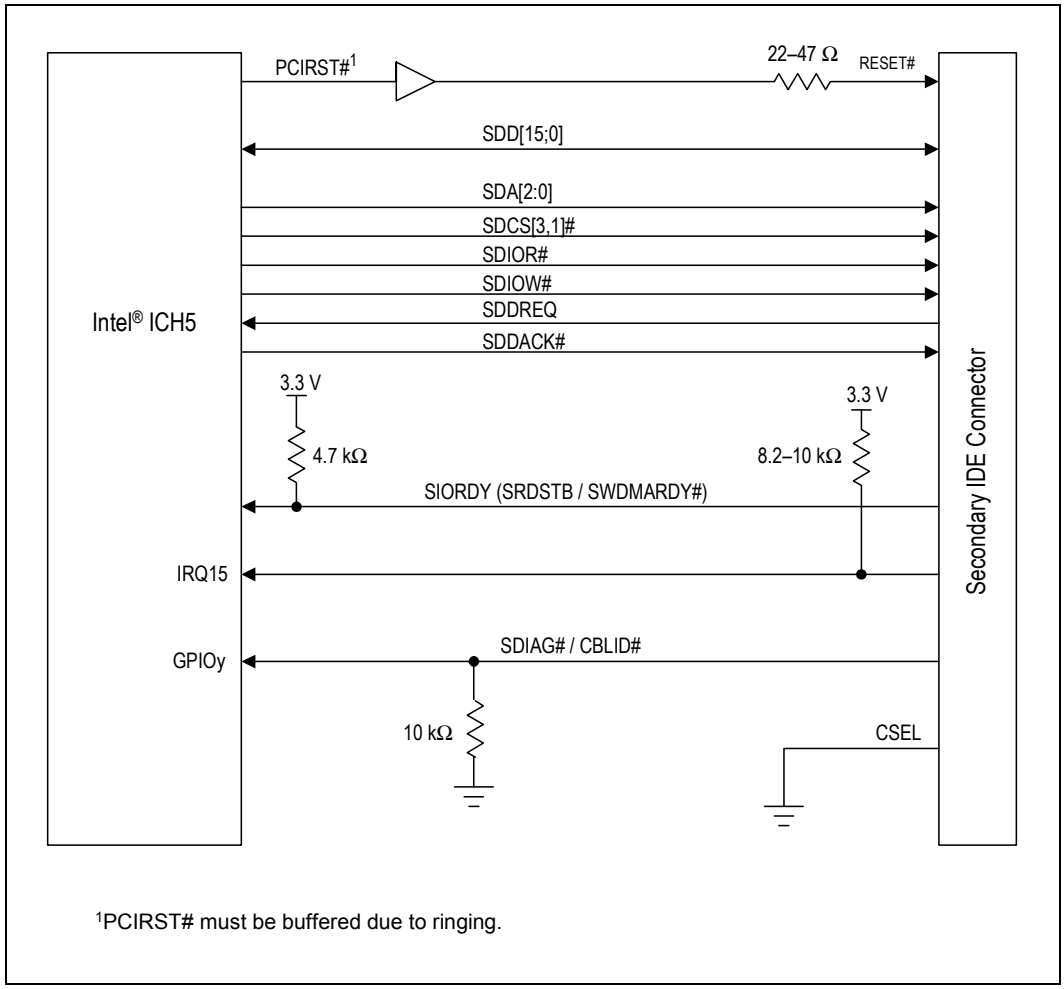
Figure 10-6. Connection Requirements for Primary IDE Connector



NOTES:
1. 22 Ω – 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 to VCCHI3_3.
3. A 4.7 kΩ pull-up resistor to VCCHI3_3 is required on PIORDY.
4. Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
5. The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

10.3.4 Secondary IDE Connector Requirements

Figure 10-7. Connection Requirements for Secondary IDE Connector



NOTES:
1. 22 Ω – 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ15 to VCC3_3.
3. A 4.7 kΩ pull-up resistor to VCC3_3 is required on SIORDY.
4. Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
5. The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is required on the Secondary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

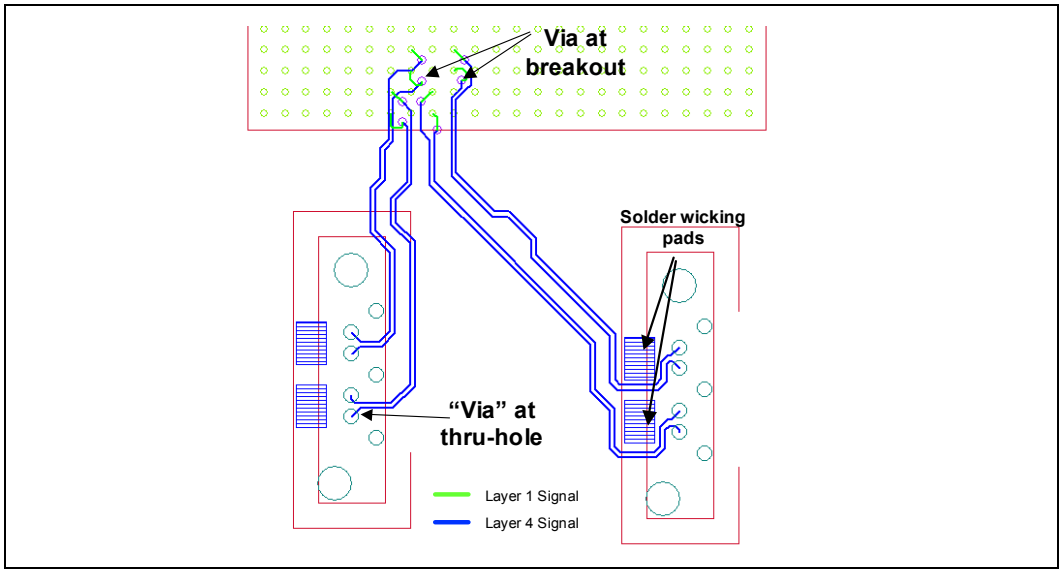
10.4 Serial ATA Interface

10.4.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design.

1. Serial ATA signals must be ground referenced.
2. Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane can cause signal reflections and should be avoided.
3. Layer changes should be minimized. Use a maximum of two vias per SATA trace (via count should include thru-hole connector as an effective via). If a layer change is necessary, ensure that trace matching for either transmit or receive pair occurs within the same layer.
4. Do not route SATA traces under crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use and/or duplicate clocks.
5. Avoid stubs (usually introduced by test points) whenever possible. Utilize vias and connector pads as test points instead.
6. It can be helpful for testability to route the TX and RX pairs for a given port on the same layer and close to each other to help ensure that the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of RX pair layout quality can be approximated by using the results from actively testing the TX pair's signal quality.
7. In certain systems (e.g., a closed-box small form factor system) where a short, very low loss cable is to be exclusively used, it may be desirable to use longer trace lengths to optimize SATA signal quality at the device receiver (RX connector specification). Careful simulation and/or studies on prototypes of signal quality are required to balance this trade off effectively.
8. See Section 18.7.2, “SATA Interface for further general routing guidelines.

Figure 10-8. SATA Layout and Routing Example



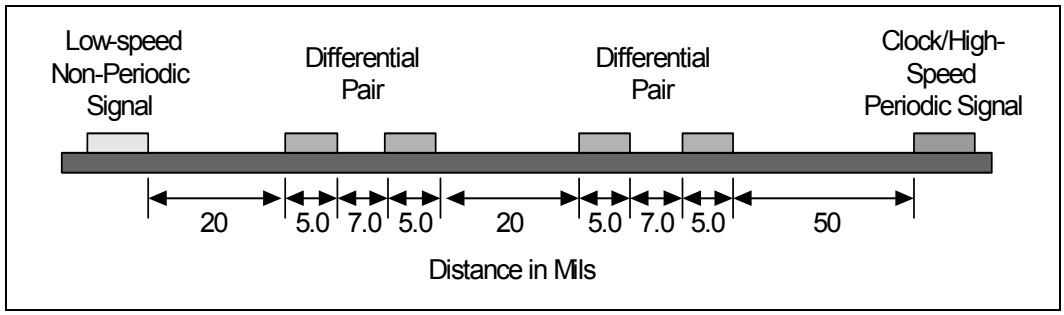
Note: Some manufacturing processes have difficulties with the fine-pitched SATA thru-hole connector. In some cases, solder bridging can occur between the connector pins. Solder wicking pads, as shown in Figure 10-8, can be used to minimize this effect by wicking solder away from the pins.

10.4.2 Serial ATA Trace Separation

Use the following separation guidelines. Figure 10-9 provides an illustration of the recommended trace spacing.

1. Maintain parallelism between SATA differential signals with the trace spacing needed to achieve 100 Ω ± 15% differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Ensure that the amount and length of the deviations are kept to the minimum possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used; keeping in mind that the target is a 100 Ω ± 15% differential impedance. For the board stackup parameters referred to in Chapter 3, 5.0-mil traces with 7.0-mil spacing results in approximately 100 Ω ± 15% differential trace impedance.
3. Based on simulation data, use 20-mil minimum spacing between ICH5 Serial ATA signal pairs and other signal traces for optimal signal quality. Clocks and other high-speed periodic signals should use a 50-mil minimum spacing between the SATA data pairs. This helps to prevent crosstalk.

Figure 10-9. Recommended Serial ATA Trace Spacing



10.4.3 Serial ATA Trace Length Pair Matching

Serial ATA signal pair traces should be trace length matched. The difference of two line traces in a differential pair should be restricted to below 150 mils, but less trace mismatch is encouraged.

10.4.4 Serial ATA Trace Length Guidelines

The length of the differential pairs (i.e., Tx pair and Rx pair) should be designed as short as possible. The minimum trace length is 0.5 inch and the maximum trace length is 4 inches. If the trace length of the differential pair is longer than recommended, the high-frequency differential signal will suffer signal attenuation and increase of rise time/fall time.

Table 10-3. SATA Routing Summary

Trace Impedance	SATA Routing Requirements	Maximum Trace Length	SATA Signal Length Matching
100 Ω ± 15% differential	5 on 7 (Based on recommended stack-up, Chapter 3	0.5 – 4 inches	Length mismatch between signals in a data pair should be no more 150 mils.

NOTE: A pitch (center to center) of 12 mils is recommended for microstrip layout. For optimum routability, this results in a common mode impedance target of approximately 25 – 40 Ω. The actual width and spacing may vary from the above table depending on the manufacturing process used.

10.4.5 SATARBIAS/SATARBIAS# Connection

It is recommended that the SATARBIAS and the SATARBIAS# pins be shorted at the package and then routed to one end of a 24.9 Ω ± 1% resistor to ground. Place the resistor within 500 mils of the ICH5. Avoid routing next to clock pins.

Figure 10-10. SATARBIAS/SATARBIAS# Connection

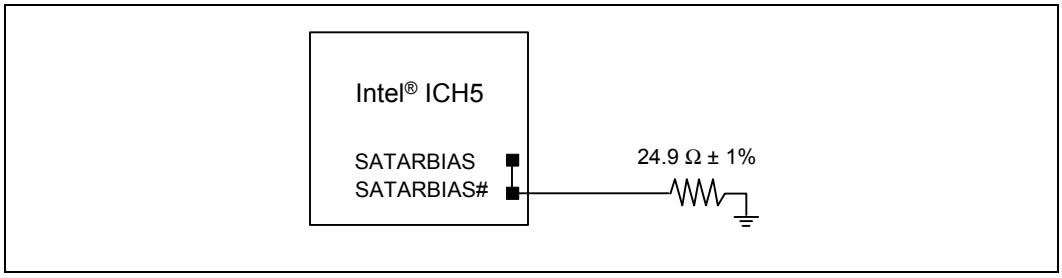


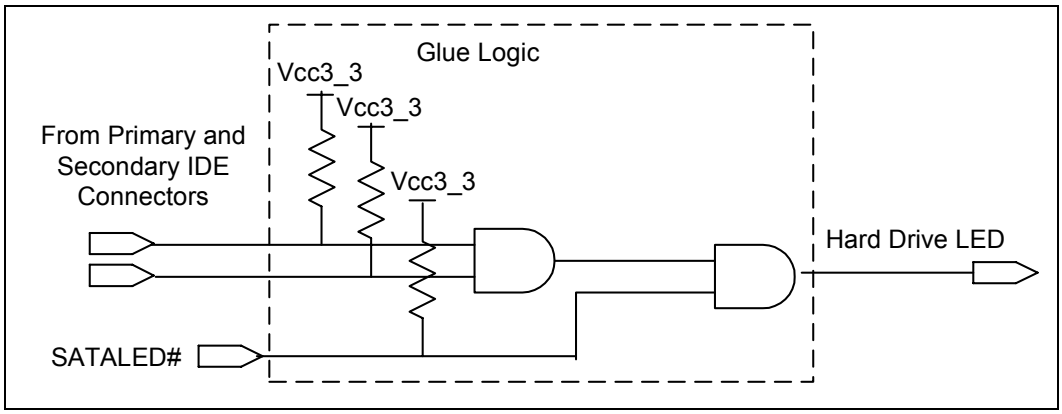
Table 10-4. SATARBIAS/SATARBIAS# Routing Summary

Trace Impedance	SATARBIAS / SATARBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
60 Ω ± 15%	NA	500 mils	NA	NA

10.4.6 SATALED# Implementation

The ICH5 provides a signal (SATALED#) to indicate SATA device activity. For this signal to work in conjunction with parallel ATA hard drives, it is recommended that the following glue logic is implemented.

Figure 10-11. SATALED# Circuitry Example



The SATALED# signal is open-drain and requires a weak external pull-up to VCC3_3. When low, SATALED# indicates SATA device activity and should activate the hard drive LED. When tri-stated, the signal will not activate the LED.

10.4.7 Serial ATA Host Connector Placement Considerations

When placing SATA host connectors, applicable keep-out regions must be comprehended in the layout of the board. Figure 10-12 shows an example cable and the height required for bending the cable to a 90-degree bend. This can be used as an example when considering height obstruction regions. Figure 10-13 shows the ATX Specification, Revision 2.1 height restriction regions. With the example cable, Area C (near the traditional parallel ATA connector sites) is the recommended placement region to allow the cable to fully bend to avoid any obstructions.

Figure 10-12. SATA Cable 90-Degree Bend Height Example

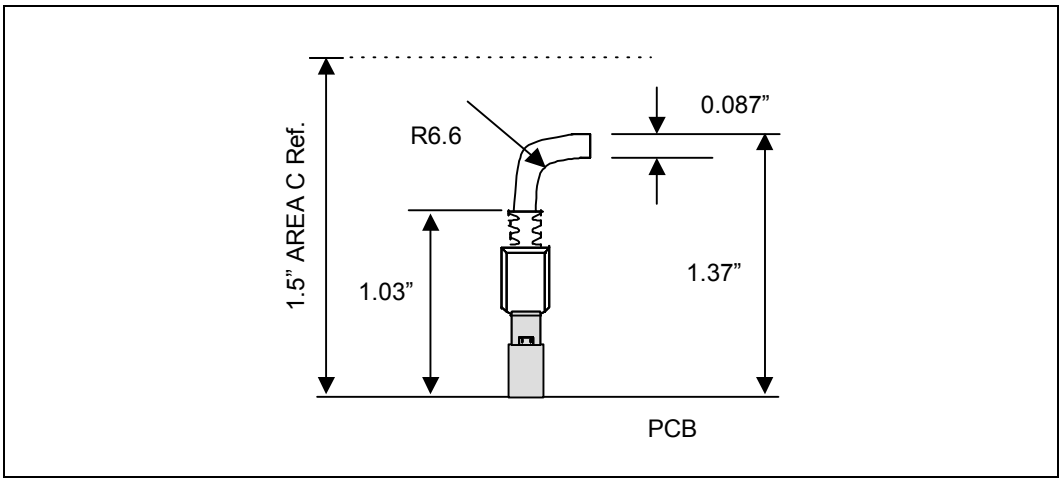
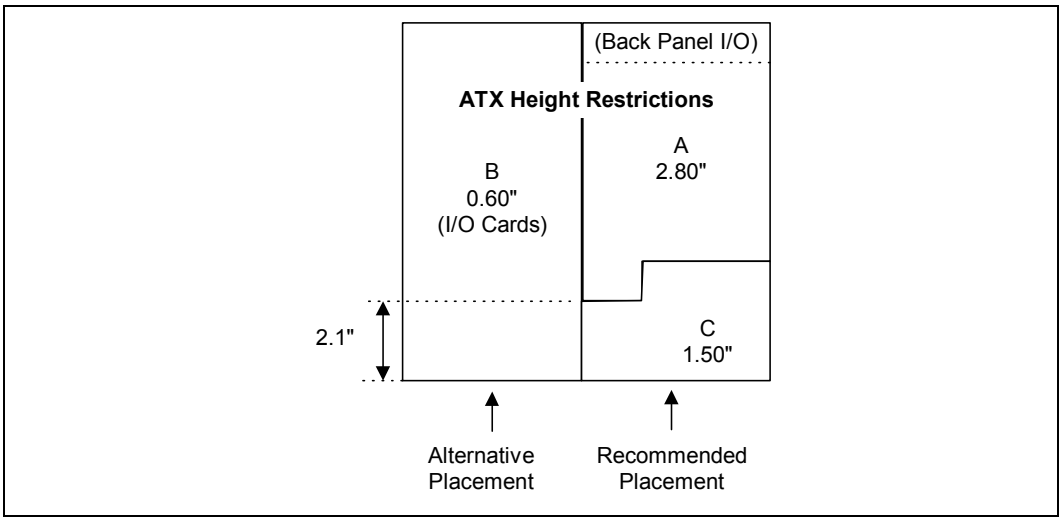
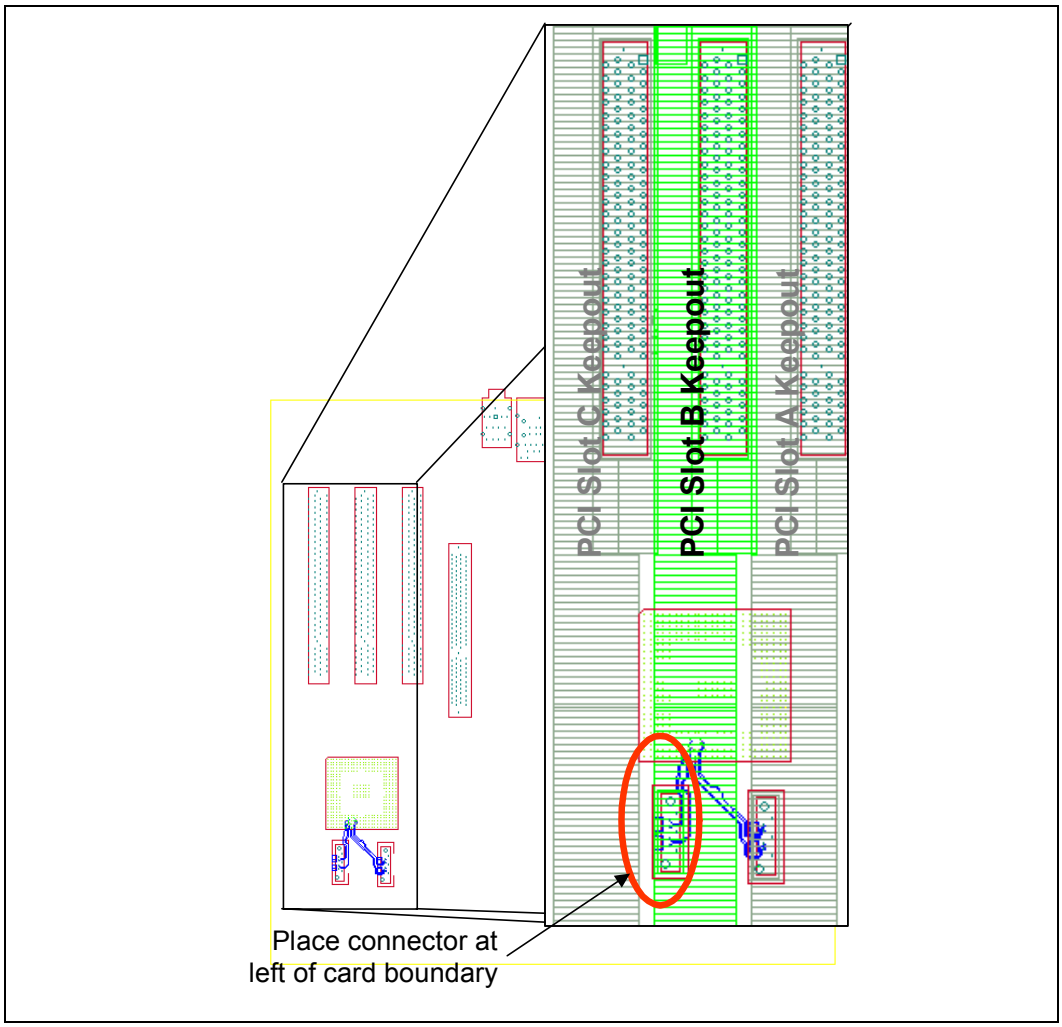


Figure 10-13. SATA Host Connector Placement Region Recommendations



If Area B (the area designated for I/O cards) must be used, great care must be exercised to minimize conflicts with I/O cards (e.g., PCI cards). As noted in Figure 10-13, the lower 2.1 inches can reduce conflicts with short PCI cards. Also, horizontal placement relative to the I/O cards can be optimized to minimize conflicts with protrusions from the I/O card. Figure 10-14 shows an example implementation that places the host connector to left edge of the PCI card keep-out region.

Figure 10-14. SATA Host Connector Placement ATX Area B Example



An additional consideration is the relative placement to other SATA host connectors as well as other neighboring parts and devices on the motherboard. Figure 10-15 shows an example of a case where two adjacent SATA host connectors were placed too close to one another. Figure 10-16 shows the minimum host connector spacings recommended in the SATA specification.

Figure 10-15. Example of Poor Host Connector Placement

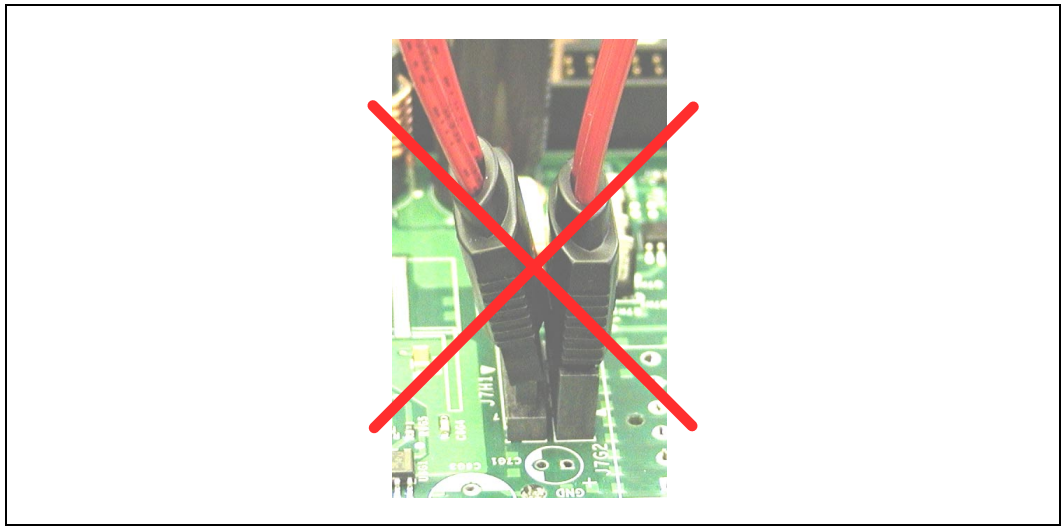
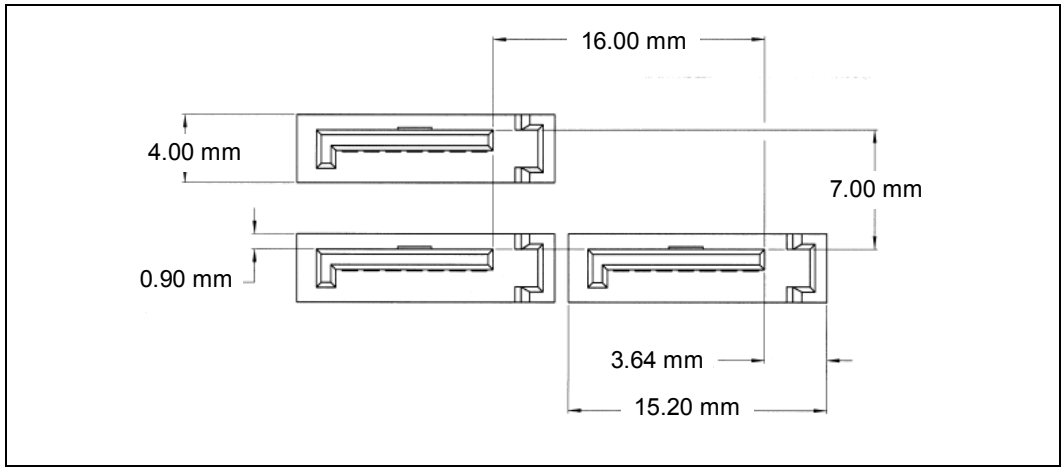


Figure 10-16. Minimum Host Connector Placement Spacing from SATA Specification



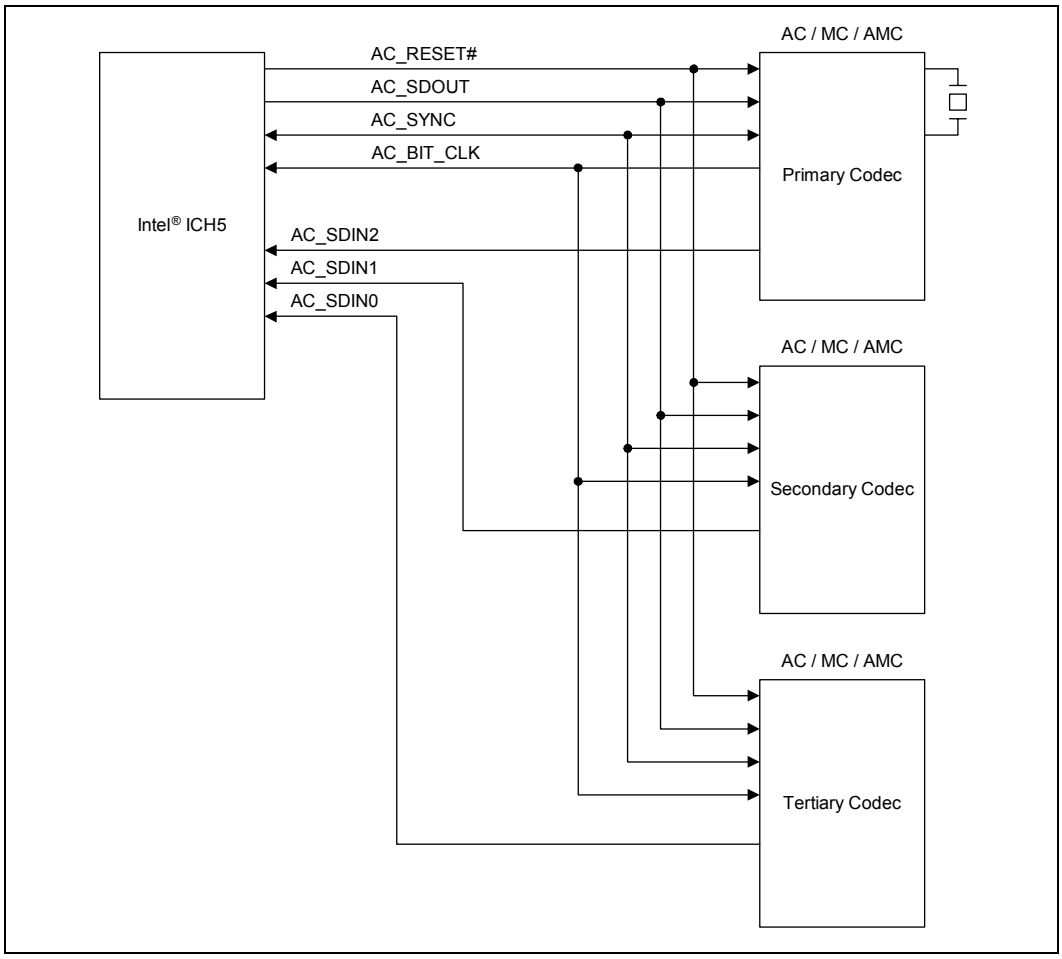
10.5 AC ’97

The ICH5 digital audio controller supports AC ’97 2.3. Contact your codec IHV (Independent Hardware Vendor) for information on AC ’97 2.3 products. The AC ’97 2.3 specification is available on the Intel website:

http://www.intel.com/ial/scalableplatforms/audio/index.htm

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH5 AC-link allows a maximum of three codecs to be connected. Figure 10-17 shows a three-codec topology of the AC-link for the ICH5.

Figure 10-17. Intel® ICH5 AC '97 (Codec Connection)



NOTE: If a modem codec is configured as the primary AC-link codec, there should not be any audio codecs residing on the AC-link. The primary codec must be connected to AC_SDIN2 if also routing to CNR. If no CNR exists on the platform, the primary codec may be connected to AC_SDIN0 as documented in the *Intel® 82801EB I/O Controller Hub 5 (ICH5) and Intel® 82801ER I/O Controller Hub 5 R (ICH5R) Datasheet*.

Using the assumed 4-layer stack-up, the AC ’97 interface can be routed using 5-mil traces with 5-mil spacing between the traces. Maximum length between ICH5 to CODEC/CNR is 14 inches. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 6 inches for the AC-link. Trace impedance should be $Z_0 = 60\ \Omega \pm 15\%$.

Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH5) and to any other codec present. That clock is used as the time base for latching and driving data.

The ICH5 supports wake on ring from S1–S5 via the AC-link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH5 has weak pull-downs/pull-ups that are always enabled. This will keep the link from floating when the AC-link is off, or there are no codecs present.

If the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOUT will be driven by the codec and ICH5 respectively. However, AC_SDIN0, AC_SDIN1, and AC_SDIN2 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

Figure 10-18. Intel® ICH5 AC '97 – AC_BIT_CLK Topology

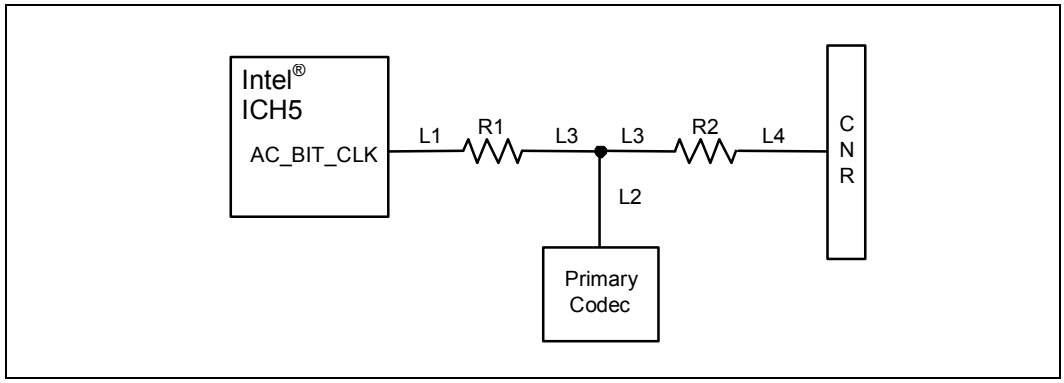


Table 10-5. AC ’97 AC_BIT_CLK Routing Summary

Trace Impedance	AC ’97 Routing Requirements	Maximum Trace Length	Series Termination Resistance	AC_BIT_CLK Signal Length Matching
60 Ω ± 15%	5 on 5 (Based on stack-up described in Chapter 3)	L1 = (1 to 8) – L3 inches L2 = (0.1 to 6) inches L3 = (0.1 to 0.4) inch L4 = (1 to 6) – L3 inches	R1 = 33 to 47 Ω R2 = Optional 0 Ω resistor for debug purposes	N/A

1. Simulations were performed using Analog Device’s codec (AD1885) and the Cirrus Logic’s codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel 9750 codec.

Figure 10-19. Intel® ICH5 AC '97 – AC_SDOUT/AC_SYNC Topology

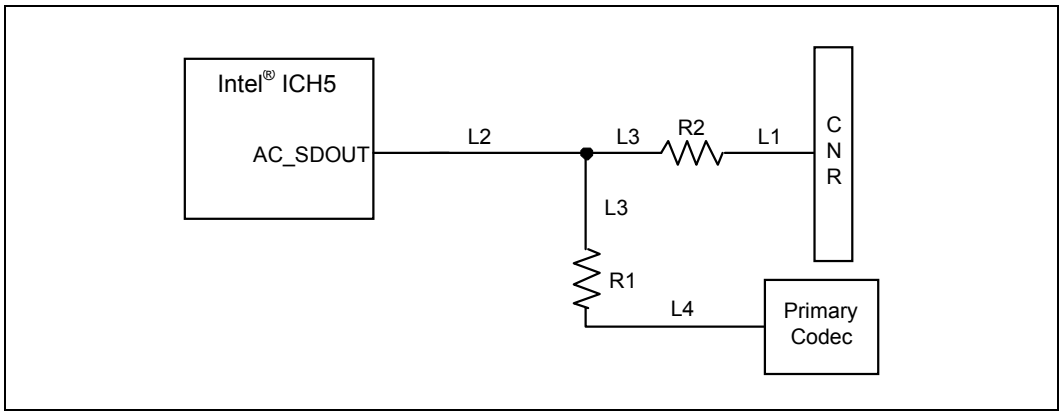


Table 10-6. AC '97 AC_SDOUT/AC_SYNC Routing Summary

Trace Impedance	AC '97 Routing Requirements	Maximum Trace Length	Series Termination Resistance	AC_SDOUT/ AC_SYNC Signal Length Matching
60 Ω ± 15%	5 on 5 (Based on stack-up described in Chapter 3)	L1 = (1 to 6) – L3 inches L2 = (1 to 8) inches L3 = (0.1 to 0.4) inch L4 = (0.1 to 6) – L3 inches	R1 = 33 to 47 Ω R2 = R1 if the CNR card that will be used with the platform does not have a series termination on the card. Otherwise R2 = 0 Ω	NA

NOTES:
1. Simulations were performed using Analog Device's codec (AD1885) and the Cirrus Logic's codec (CS4205b). Results showed that if the AD1885 codec was used, a 33 Ω resistor was best for R1 and if the CS4205b codec was used, a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1is best for the Sigmatel 9750 codec.

Figure 10-20. Intel® ICH5 AC '97 – AC_SDIN Topology

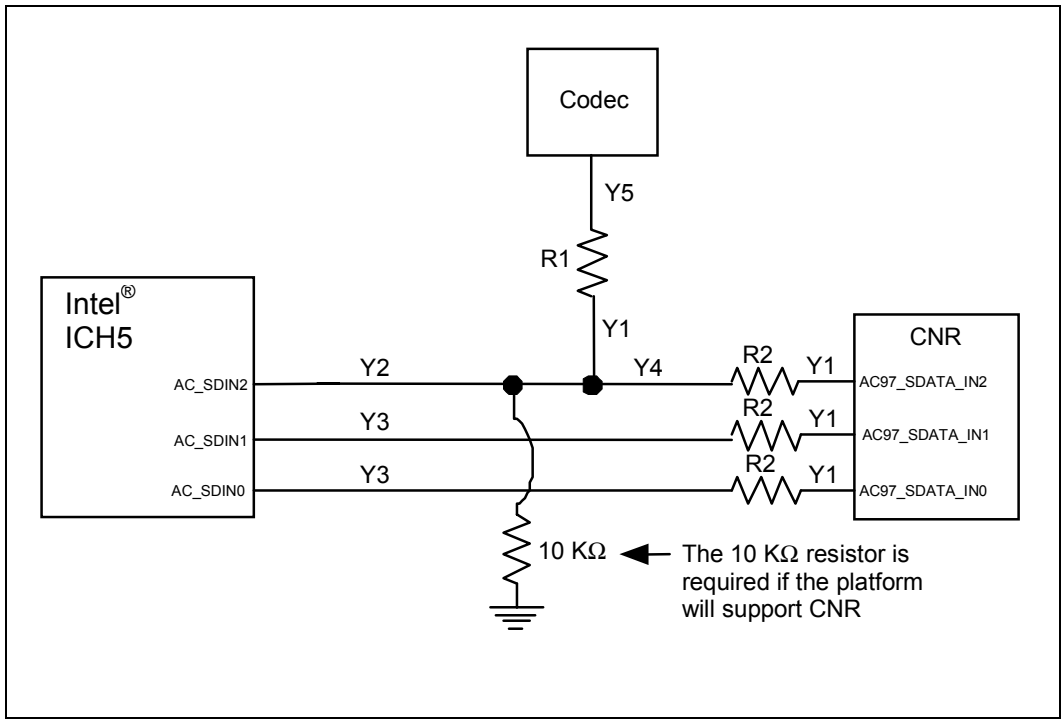


Table 10-7. AC '97 AC_SDIN Routing Summary

Trace Impedance	AC '97 Routing Requirements	Maximum Trace Length	Series Termination Resistance	AC_SDIN Signal Length Matching
60 Ω ± 15%	5 on 5 (Based on stack-up described in Chapter 3)	Y1 = (0.1 to 0.4) inch Y2 = (1 to 8) – Y1 inches Y3 = (1 to 14) – Y1 inches Y4 = (1 to 6) – Y1 inches Y5 = (0.1 to 6) – Y1 inches	R1 = 33 to 47 Ω R2 = R1 if the CNR card that will be used with the platform does not have a series termination on the card. Otherwise R2 = 0 Ω	N/A

1. Simulations were performed using Analog Device's codec (AD1885) and the Cirrus Logic's codec (CS4205b). Results showed that if the AD1885 codec was used, a 33 Ω resistor was best for R1 and if the CS4205b codec was used, a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1is best for the Sigmatel 9750 codec.

10.5.1 AC ’97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, and analog power supplies, from the rest of the motherboard. This also includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations. The following sections provide the basic recommendations.

10.5.1.1 General Board Routing Recommendations

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Try to minimize via count on each AC-link trace (no more than eight are recommended).
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

10.5.1.2 Codec Reference and Anti-Aliasing Recommendations

ADC/DAC anti-aliasing filter and reference capacitors should be placed within 0.5 inch of their respective codec pins. All filter capacitors’ ground connections should attach to a ground point common to the codec. This is often accomplished by routing a ground trace from the codec to the capacitors without allowing vias to the digital ground plane.

10.5.1.3 Codec Analog Power Decoupling Recommendations

Analog power decoupling is extremely critical and is essential on all codec analog power pins. Unfiltered power supply noise on these pins will negatively affect the audio performance and quality.

Each codec analog power pin should have one 0.1 µF and one 1.0 µF capacitor placed next to the pin. The capacitor dielectric should be Y5V or better (X5R/X7R). Once leaving the 5-V plane, the power traces should pass directly over the capacitor pads and terminate at the codec pin without ever connecting back to the 5-V analog plane.

Ensure that the traces connecting the power and ground pins are wide (15–25 mils). Do not share vias to GND on decoupling capacitors. The GND path to the 5-V plane should be kept as short as possible.

10.5.1.4 Codec Digital Power Decoupling Recommendation

DVDD1 and DVDD2 provide power for the digital section of a codec. The digital section includes the AC-link and the SPDIF output. These pins are tied to the VCC3.3 power plane. Decoupling for the digital power is provided by two, 0.1 µF (Y5V, 0603) capacitors (the goal is one capacitor per input pin) plus a single, 10–22 µF SMT or thru-hole aluminum capacitor.

If a codec is desired to be active during the S5 state, the analog and digital power pins should utilize the appropriate standby supplies.

DVSS1 and DVSS2 are the digital ground pins for the codec and are to be connected directly to the board's internal GND layer.

- Ensure that the traces connecting the power and ground pins are wide (15–25 mils). Do not share vias to GND on decoupling capacitors; shorter paths to GND are preferable.

10.5.2 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH5 platform using AC '97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH5 platform.

- Active Components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH5 supports wake-on-ring from S1-S5 states via the AC-link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

10.5.2.1 Valid Codec Configurations

Table 10-8. Supported Codec Configurations

Option	Primary Codec	Secondary Codec	Tertiary Codec
1	Audio	Audio	Audio
2	Audio	Audio	Modem
3	Audio	Audio	Audio/Modem
4	Audio	Modem	Audio
5	Audio	Audio/Modem	Audio
6	Audio/Modem	Audio	Audio

NOTES:
1. For power management reasons, codec power management registers are in audio space. As a result, if there is an audio codec in the system it must be Primary. In addition, there cannot be two modems in a system since there is only one set of modem DMA channels.
2. The ICH5 supports a modem codec on any of the AC_SDIN lines, however the Modem Codec ID must be either 00 or 01.

10.5.3 Design Considerations for Audio Quality

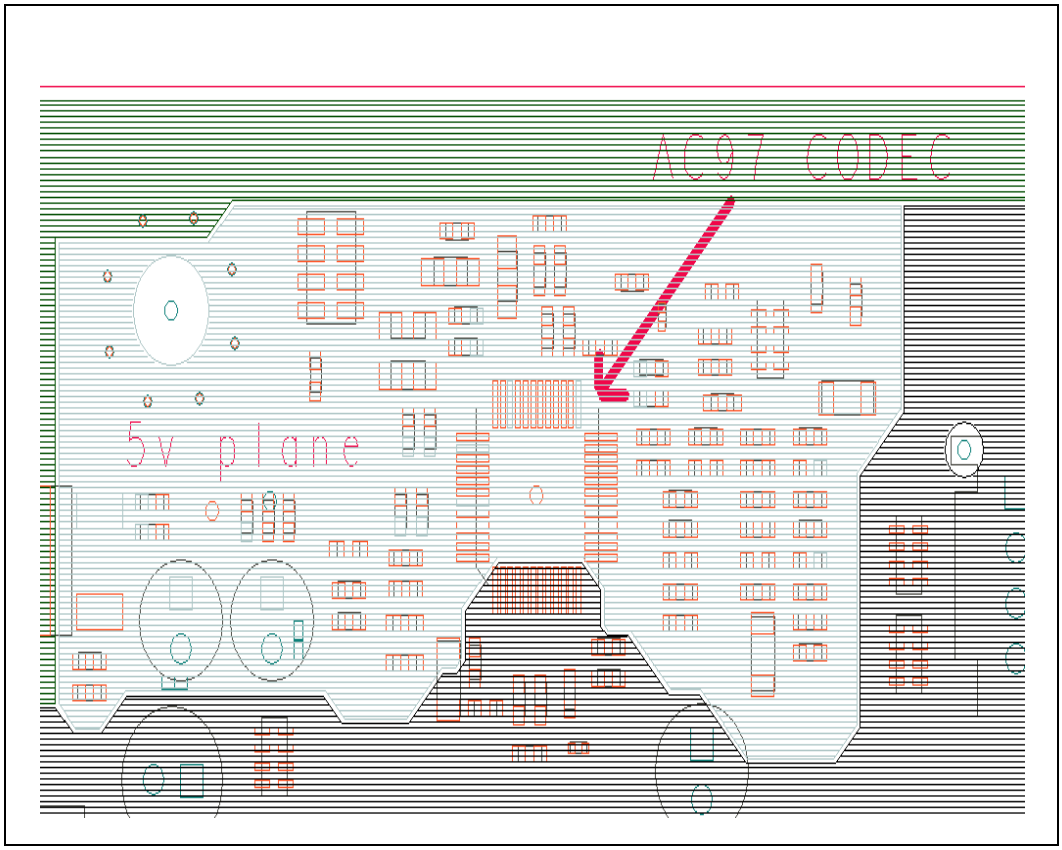
10.5.3.1 Audio Codec Placement

Proper audio codec placement, routing, and general design practices play a key roll in delivering clean audio in the noisy environment of a motherboard. The audio codec should be placed in the quietest (away from significant current paths and ground bounce) part of the motherboard. Typically, the top left corner of the board is the quietest location given the surrounding components. Furthermore, this location provides a convenient routing path to the back panel audio jacks.

10.5.3.2 Power Plane Configurations

To prevent the digital section of the codec from affecting the analog section, it is prudent to split the power-planes across the codec. The split isolates power currents and signal return currents between the two sections. The 5-V analog plane also provides analog power to audio circuits external to the codec (amplifiers, microphones, etc.). The 5-V analog plane should encompass all codec pins except for pins 1–12. The AC ’97 digital interface nets, along with codec clocking nets, should not route onto or cross over the 5-V analog plane split. Analog nets routing out to the back panel audio jacks should avoid crossing the plane split as well. This can be accomplished by bottom side routing. The analog power plane should not extend under the PCI connectors or LAN solution. Figure 10-21 shows an example of power plane split at the codec.

Figure 10-21. AC '97 Power Plane Configurations

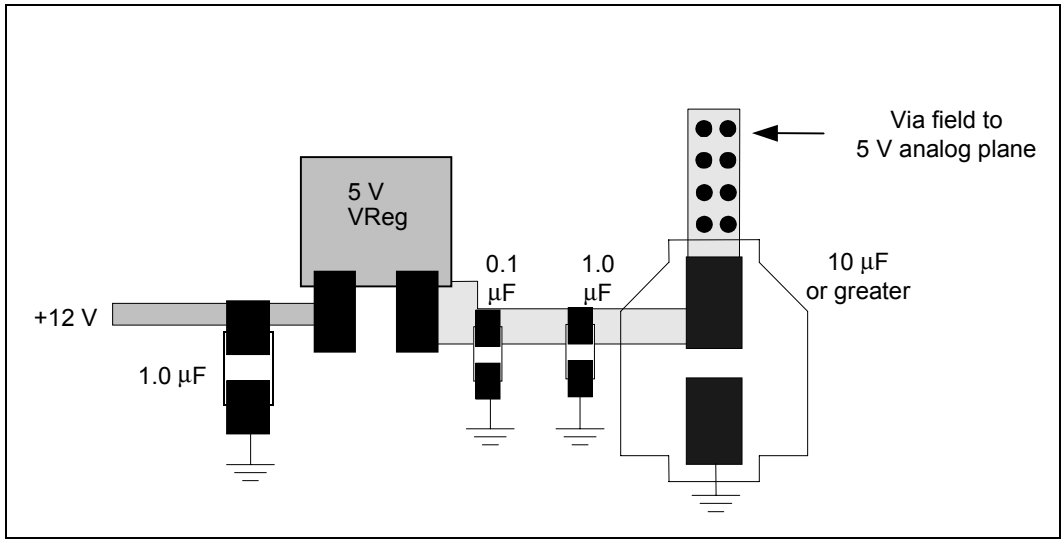


10.5.3.3 Analog Power Delivery

Clean analog power delivery to the audio codec and other audio components using the 5 V analog supply is critical. Excessive system noise on this supply will degrade the entire audio sub-system. Following are the considerations for analog power delivery; Figure 10-22 illustrates those points.

- Place 0.1 µF, 1.0 µF, and 10 µF (or larger) decoupling capacitors close to the via field that supplies the 5-V analog plane. To minimize inductance, drop vias to the VSS (Ground) plane as close as possible to the capacitor ground pads.
- Use a relatively wide trace for the 5-V analog power to reduce inductance between the regulator and the 5-V analog plane.
- Do not via to the 5-V analog plane until all the decoupling capacitors are used, as shown in Figure 10-22.
- A radial bulk decoupling capacitor site is recommended to provide for values greater than 10 µF.

Figure 10-22. AC '97 Analog Power Delivery



10.5.3.4 Power On Audio Transitions

Power on audio pop is typically caused when a codec is initially powered on or when it is coming out of a reset state. This noise is often related to rapid charging or discharging of the AC coupling output capacitors. Excessive power-on audio pop should be kept to a minimum through the use of anti-pop circuitry.

Most, if not all, AC ’97 version 2.3 codecs include protection circuitry to help minimize power-on pop. Should a design utilize an audio codec that does not provide audio pop suppression, external anti-pop circuitry should be implemented.

10.5.3.5 Line Output

Two-channel line output jacks should be capable of driving low-impedance headphone loads. Furthermore, the back panel line out jack should mute when a connection is made to the front panel headphone jack in a design that supports both back panel and front panel line output jacks. Failure to support this functionality may result in weak audio output levels and unwanted functionality that will detract from the end user's audio experience.

Line output AC coupling capacitors should be at least 100 µF or greater to prevent diminished low frequency response when low impedance loads (headphones) are connected.

10.5.3.6 Line In / Auxiliary In

Audio designs that support up to 2 V RMS line input signals are recommended, but not required. To support audio inputs up to 2 V RMS, a voltage divider network should be implemented to effectively reduce the input level by 6 dB prior to reaching the codec.

10.5.3.7 Grounding Techniques

Care should be taken when grounding back panel audio jacks, especially the line in and microphone jacks. Grounding the audio jacks to the ground plane directly under the connectors should be avoided. Doing so raises the potential for audio noise to be induced on the inputs due to the difference in ground potential between the audio jacks and the codec's grounding point.

Jack and shunt spring grounding should use a controlled ground return path traced back to the codec. A trace width of 15 mils–20 mils with bottom side routing is recommended.

10.5.3.8 CD ATAPI Input

Most, if not all, codecs have pseudo-differential CD inputs that provide enhanced common mode noise rejection. Designs supporting 2 V RMS input using a voltage divider network should implement the input voltage divider on the ground input, in addition to the left and right input channels.

10.5.4 Stereo Microphone Consideration

The microphone (stereo or mono) input signal is the most sensitive input to the codec. Most codecs contain internal microphone gain stages capable of up to +30 dB of gain. Therefore, small amounts of noise present on these input pins can result in audible noise detectable by the end user. The higher the microphone gain setting, the more noise becomes an issue.

The following should be considered for microphone support:

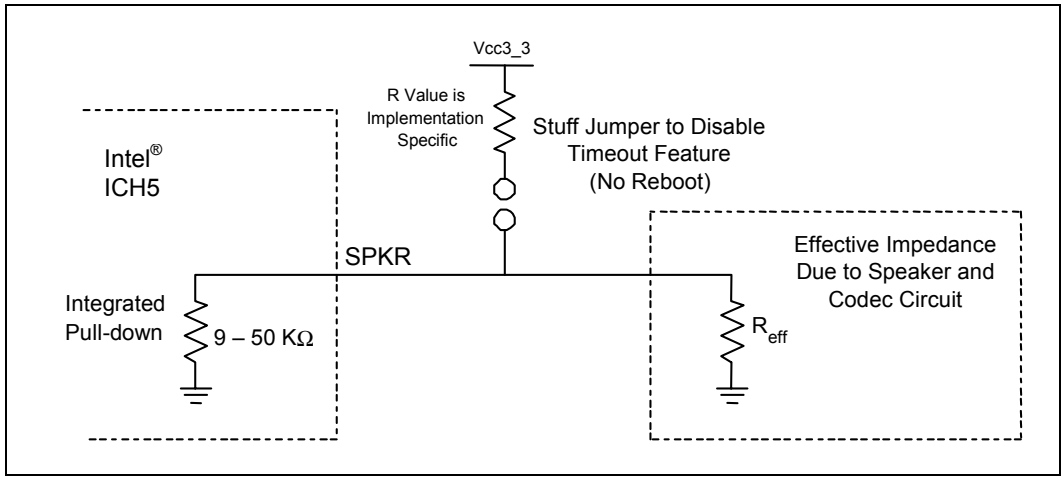
- Back panel and front panel microphone inputs (mono or stereo) should be passively mixed together prior to connecting to the codec microphone input pin(s) unless the codec supports independent front and back panel microphone inputs.
- Microphone ground-return-paths should be isolated from the motherboard ground plane. It is recommended that they be routed as discrete traces that follow the same path as the microphone signal traces. It is recommended that the ground-plane not be "slotted."
- For non-jack sharing, microphone input tip/ring pins should be grounded via shunt spring wipers when the microphone is removed from the connector. A dedicated audio jack ground connecting to the codec's grounding point should be used for shunt spring grounding.

- A 22 µF or greater capacitor should be used to filter noise from the microphone bias net feeding all microphone jacks. This capacitor helps reduce crosstalk between stereo microphone channels.
- Microphone traces should be isolated from non-microphone traces.
- The DC microphone bias voltage can be supplied by either the 5-V analog power plane or by the codec's VREF output pin depending upon the codec's capabilities. Ensure clean power is used for supplying the DC microphone bias voltage. The bias voltage applied to each of the four possible microphone elements must meet the requirements specified within Microsoft's PC 2001 specification.Value changes to the series resistor connecting the microphone bias network to codec's VREF pin may be required depending upon the codec's VREF output voltage level.

10.5.5 SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH5 sends a SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see Figure 10-23). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (REFF), and the ICH5's integrated pull-down resistor will be read as logic high (0.5 VCC3_3 to VCC3_3 + 0.5 V).

Figure 10-23. Example Speaker Circuit

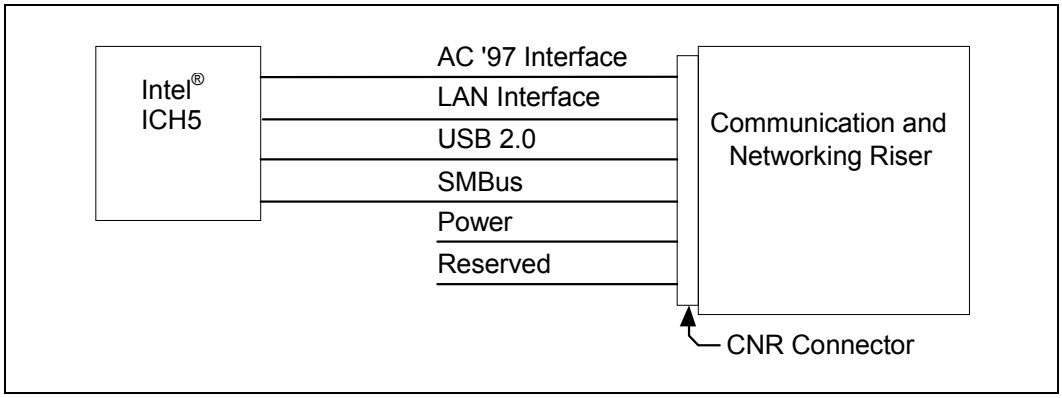


10.6 CNR

The Communication and Networking Riser (CNR) Specification defines a hardware scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. This interface supports multi-channel audio, V.90 analog modem, phone-line based networking, 10/100 Ethernet based networking, SMBus interface power management, and USB 2.0. The CNR specification defines the interface, which should be configured prior to shipment of the system. Standard I/O expansion slots (e.g., those supported by the PCI bus architecture) are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot; therefore, the system designer will not sacrifice a PCI slot if they decide not to include a CNR in a particular build.

Figure 10-24 shows the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. The Platform LAN Connection (PLC) can either be an 82562ET/EZ or 82562EM/EX PLC component. Refer to the *Communication Network Riser Specification, Revision 1.2,* for additional information.

Figure 10-24. CNR Interface



10.6.1 AC ’97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. Refer to the *Communication Network Riser Specification, Revision 1.2,* for Intel’s recommended codec configurations.

Table 10-9. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, this signal indicates that the codec on the motherboard is enabled and primary on the AC ‘97 interface. When high, this signal indicates that the motherboard codec(s) must be removed from the AC ’97 interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC ’97 interface.
AC97_RESET#	Reset signal from the AC ’97 digital controller (Intel® ICH5).
SDATA_IN*n*	AC ’97 serial data from an AC ’97-compliant codec to an AC ’97-compliant controller (i.e., the ICH5).

10.6.1.1 CNR 1.2 AC ’97 Disable and Demotion Rules for the Motherboard

The following are the CNR1.2 AC ’97 disable and demotion rules for the motherboard:

- All AC ’97 *R2.3* codecs on the motherboard **must** always disable themselves when the CDC_DN_ENAB# signal is in a high state.
- A motherboard AC ’97 codec **must** never change its address or SDATA_IN line used, regardless of the state of the CDC_DN_ENAB# signal.
- On a motherboard containing an AC ’97 controller supporting three AC ’97 codecs, the AC ’97 Revision 2.3 codec on the motherboard **must** be connected to the SDATA_IN2 signal of the CNR connector.
- A motherboard should not contain any more than a single AC ’97 codec.

The above rules allow for forward and backward compatibility between CNR Version 1.1/ 1.2 cards. For more information on chaining, consult the *Communication Network Riser Specification Revision 1.2*.

Figure 10-25. Motherboard AC ’97 CNR Implementation with a Single Codec down on Board

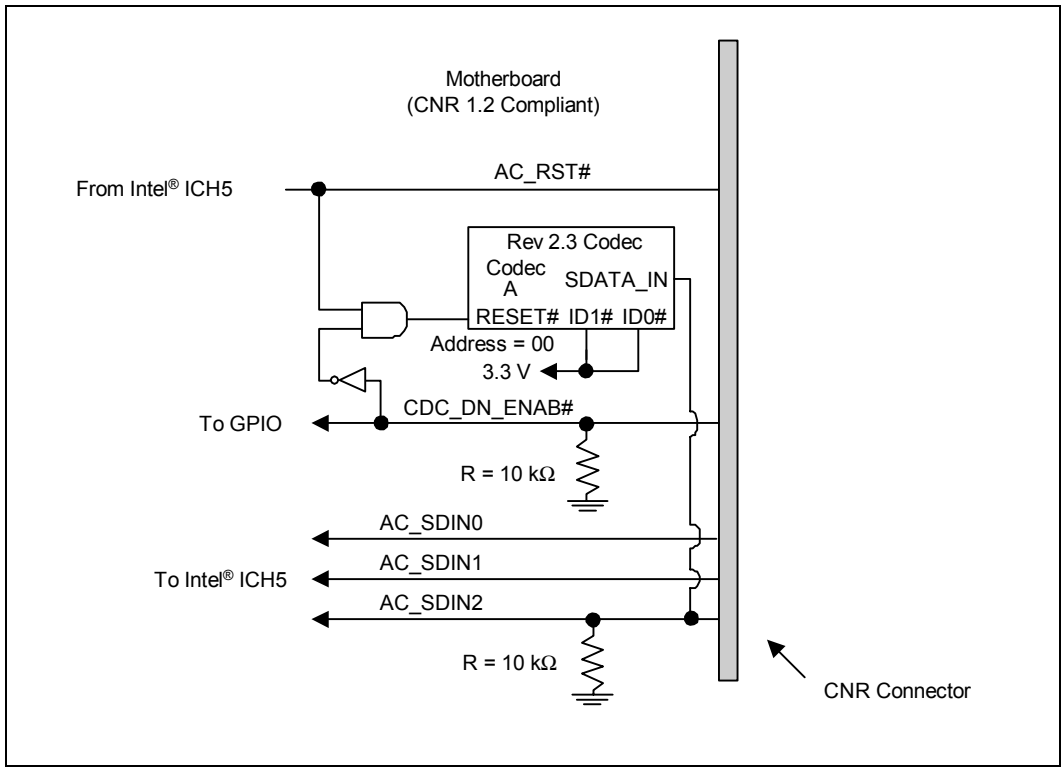
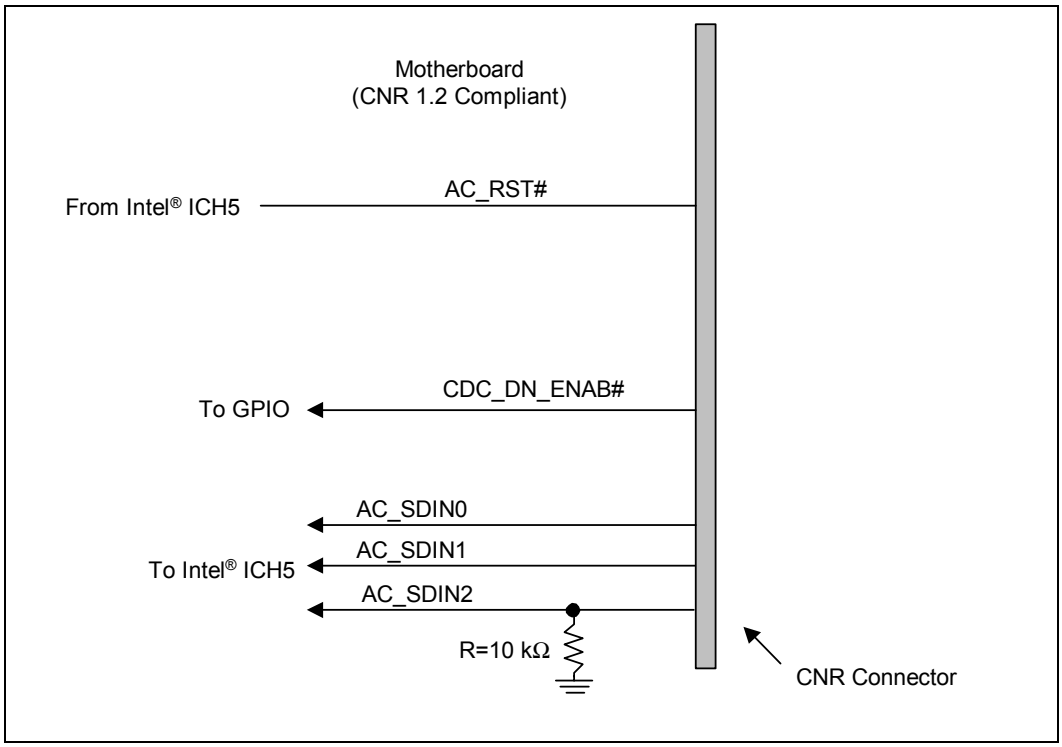


Figure 10-26. Motherboard AC '97 CNR Implementation with No Codec down on Board



10.6.2 CNR Routing Summary

Table 10-10 represents a summary of the various interfaces routing requirements to the CNR Riser.

Table 10-10. CNR Routing Summary

Trace Impedance	CNR Routing Requirements	Maximum Trace Length to CNR connector	Signal Length Matching	Signal Referencing
90 Ω ± 15% Differential	USB (7.5 on 7.5) Data pair must be at least 20 mils from nearest neighbor	10 inches	No more than 150 mils trace mismatch	Ground
60 Ω ± 15%	AC '97 (5 on 5)	AC_BIT_CLK (See Table 10-5) AC_SDOUT (See Table 10-6) AC_SDIN (See Table 10-7)	N/A	Ground
60 Ω ± 15%	LAN (5 on 10)	9 inches (See Table 10-23)	Equal to or up to 500 mils shorter than the LAN_CLK trace	Ground

10.7 USB 2.0

10.7.1 Layout Guidelines

10.7.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems.

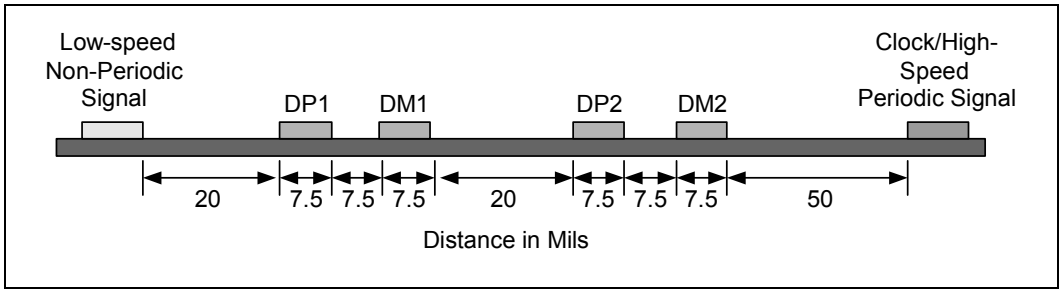
- Place the ICH5 and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
- USB 2.0 signals should be **ground referenced** (on recommended stack-up this would be bottom signal layer).
- Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
- When it becomes necessary to turn 90 degrees, use two 45-degree turns, or an arc, instead of making a single 90-degree turn. This reduces reflections on the signal by minimizing impedance discontinuities. (as shown in Figure 10-52.)
- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- Stubs on high-speed USB signals should be avoided, as stubs cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils.
- Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 10.7.2
- Separate signal traces into similar categories and route similar signal traces together (e.g., routing differential pairs together).
- Keep USB 2.0 USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
- Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack-up, the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

10.7.1.2 USB 2.0 Trace Separation

Use the following separation guidelines. Figure 10-27 shows the recommended trace spacing.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.
- Use an impedance calculator to determine the trace width and spacing required for the specific board stack-up being used; keeping in mind that the target is a 90 Ω differential impedance. For the board stack-up parameters referred to in Chapter 3, 7.5-mil traces with 7.5-mil spacing results in approximately 90 Ω differential trace impedance.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to high-speed USB signal lines, to minimize crosstalk. The minimum suggested spacing to clock signals is 50 mils.
- Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

Figure 10-27. Recommended USB Trace Spacing



10.7.1.3 USBRBIAS/USBRBIAS# Connection

It is recommended that the USBRBIAS and the USBRBIAS# pins be shorted at the package and then routed to one end of a 22.6 Ω ± 1% resistor to ground. Place the resistor within 500 mils of the ICH5. Avoid routing next to clock pins.

Figure 10-28. USBRBIAS/USBRBIAS# Connection

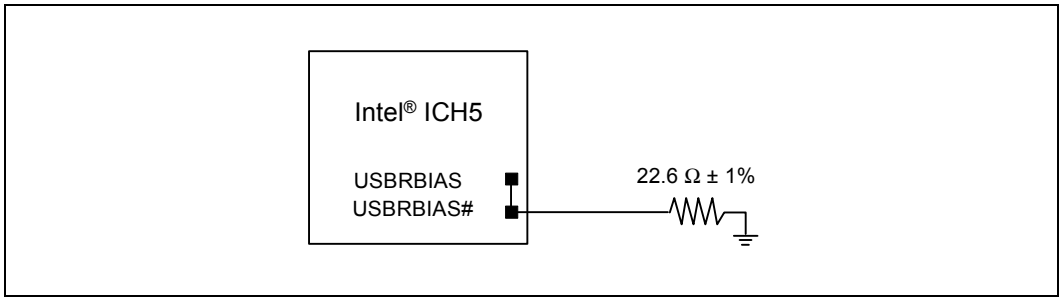


Table 10-11. USBRBIAS/USBRBIAS# Routing Summary

Trace Impedance	USBRBIAS/ USBRBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
60 Ω ± 15%	NA	500 mils	NA	NA

10.7.1.4 USB 2.0 Termination

A common-mode choke may be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See Section 10.7.4 for details.

10.7.1.5 USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Maximum trace length mismatch between USB 2.0 signal pair should be no greater that 150 mils.

10.7.1.6 USB 2.0 Trace Length Guidelines

Use the following trace length guidelines.

Table 10-12. USB 2.0 Trace Length Preliminary Guidelines (with Common-Mode Choke)

Topology	USB 2.0 Routing Requirements/ Trace Impedance	Cable Length	Motherboard Trace Length	Card Trace Length	Maximum Total Length	Signal Referencing	Signal Matching
Back Panel	7.5 on 7.5 / 90 Ω ± 15% differential	NA	17 inches	NA	17 inches	Ground	The max mismatch between data pairs should not be greater than 150 mils
CNR	7.5 on 7.5 / 90 Ω ± 15% differential	NA	8 inches	6 inches	14 inches		
Front Panel	7.5 on 7.5 / 90 Ω ± 15% differential	9	6	2	17		
		10.5	5	2	17.5		
		12	4	2	18		
		13.5	3	2	18.5		
		15	2	2	19		

NOTES:
1. These lengths are based on simulation results and may be updated in the future.
2. All lengths are based on using a common-mode choke (see Section 10.7.4.1 for details on common-mode choke).
3. Numbers in Table 10-12 are based on the following simulation assumptions:
   a. CNR configuration: max 6 inches trace on add-on card.
   b. An approximate 1:1 trade-off can be assumed for Motherboard Trace Length vs. Daughter card Trace Length (e.g., trade 1 inch of Daughter card for 1 inch of Motherboard Trace Lengths).
4. Routing guidelines are based on the stack-up assumptions in Chapter 3.
5. Numbers in Table 10-12 are based on the following simulation assumptions:
   a. Trace length on front panel connector card assumed a max of 2 inches.
   b. USB twisted-pair shielded cable as specified in *USB 2.0 Specification* was used.
6. For front panel solutions signal matching is considered from the ICH5 to the front panel header.

10.7.2 Plane Splits, Voids, and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cut-outs.

10.7.2.1 VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the VCC plane.

- Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces which might be coupling to them. USB signaling is not purely differential in all speeds (i.e., the full-speed, single-ended zero is common mode).
- Avoid routing of USB 2.0 signals 25-mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages, it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

If crossing a plane split is completely unavoidable, proper placement of stitching capacitors can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge voltage plane splits close to where High-speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates VCC5 and VCC3_3 planes should have a stitching capacitor placed near any high-speed signal crossing. One side of the capacitor should tie to VCC5 and the other side should tie to VCC3_3. Stitching capacitors provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

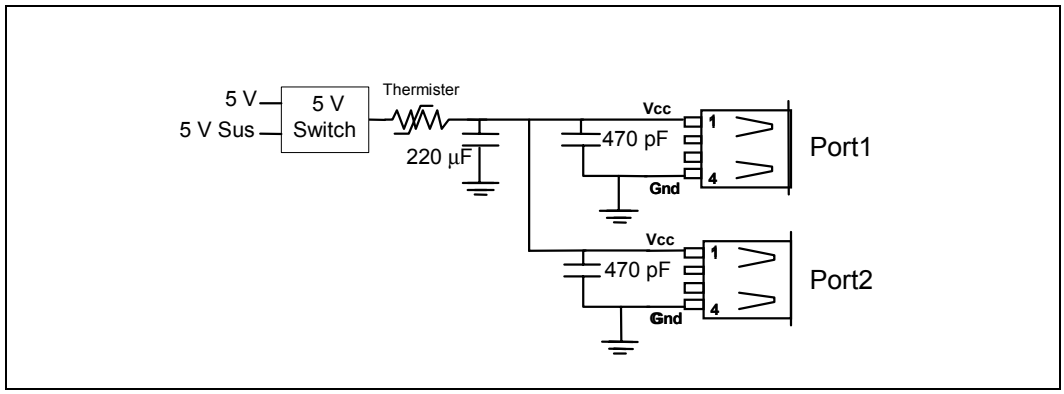
10.7.2.2 GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

10.7.3 USB Power Line Layout Topology

The following is a suggested topology for power distribution of Vbus to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach flyback protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach flyback voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane. A good practice is to make the power-carrying traces wide enough that the system fuse will blow on an over current event. If the system fuse is rated at 1 A, the power-carrying traces should be wide enough to carry at least 1.5 A.

Figure 10-29. Good Downstream Power Connection



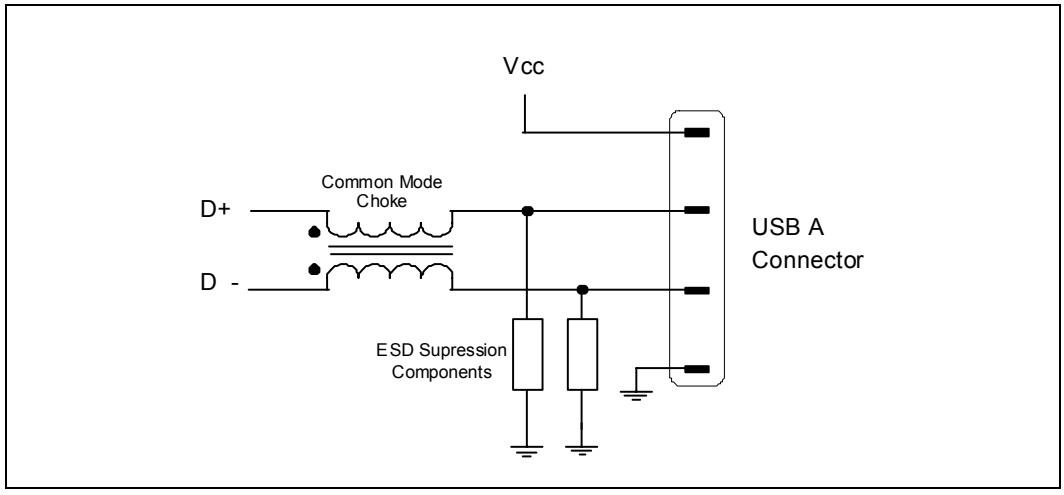
10.7.4 EMI Considerations

The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices.

10.7.4.1 Common-Mode Chokes

Testing has shown that common-mode chokes can provide required noise attenuation. A design should include a common-mode choke footprint to provide a stuffing option **in the event** the choke is needed to pass EMI testing. Figure 10-30 shows the schematic of a typical common-mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins. In systems that route USB to a front panel header the choke should be placed on the front panel card. See Chapter 10.7.6.3.

Figure 10-30. A Common-Mode Choke



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion will increase, so you should test the effects of the common mode choke on full speed and high-speed signal quality. Common-mode chokes with a target impedance of 80 Ω to 90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common-mode choke that meets the designer's needs is a two-step process:

- A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
- Once a part provides passing EMI results, the second step is to test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed, and high-speed USB operation.

Note: Further common-mode choke information can be found on the high-speed USB Platform Design Guides available at:

http://www.usb.org/developers/docs.html.

10.7.5 ESD

Classic USB (1.0/1.1) provided ESD suppression using inline ferrites and capacitors that formed a low pass filter. This technique does not work for USB 2.0 due to the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 10-30. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, it is recommended to include footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

Note: Further ESD information can be found on the high-speed USB Platform Design Guides available at www.usb.org/developers/docs.html.

10.7.6 Front Panel Solutions

10.7.6.1 Internal USB Cables

The front panel internal cable solution must meet all the requirements of Chapter 6 of the *USB 2.0 Specification* for High/Full-speed cabling for each port with the exceptions described in Cable Option 2. For more information refer to the FPIO design guideline available at:

http://www.formfactors.org/developer/fpio_design_guideline.pdf.

10.7.6.1.1 Internal Cable Option 1

Use standard high-speed/full-speed compatible USB cables. These must meet all cabling requirements called out in Chapter 6 of the *USB 2.0 Specification*. Recommended motherboard mating connector pin-out is covered in detail later in this document.

10.7.6.1.2 Internal Cable Option 2

Use custom cables that meet all of the requirements of Chapter 6 of the *USB 2.0 Specification* with the following additions/exceptions:

1. They can share a common jacket, shield, and drain wire.
2. Two ports with signal pairs that share a common jacket may combine Vbus and ground wires into a single wire provided the following conditions are met:
   a. The bypass capacitance required by Section 7.2.4.1 of the *USB 2.0 Specification* is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughter card). Refer to the front panel daughter card referenced later for details.
   b. Selecting proper wire size: A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the *USB 2.0 Specification* that has equal or less than one-half the resistance of either of the two wires being combined. The data is provided for reference in Table 10-13.

Table 10-13. Conductor Resistance (Table 6-6 from *USB 2.0 Specification*)

American Wire Gauge (AWG)	Ohm / 100 Meters Maximum
28	23.20
26	14.60
24	9.09
22	5.74
20	3.58

Example: Two 24-gauge (AWG) power or ground wires can be replaced with one 20-gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the *USB 2.0 Specification* at the USB connectors as well as at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure the system passes droop requirements. Cables that provide individual power and ground conductors for each port can usually meet droop requirements by providing adequate capacitance near the motherboard mating connector since droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case, all transients will be seen/dampened by the capacitance at the motherboard mating connector before they can cause problems with the adjacent port sharing the same cable. See Sections 7.2.2 and 7.2.4.1 of the *USB 2.0 Specification* for more details.

Cables that contain more than two signal pairs are not recommended due to unpredictable impedance characteristics.

10.7.6.2 Motherboard/PCB Mating Connector

Proper selection of a motherboard mating connector for front panel USB support is important to ensure signal quality is not adversely affected due to a poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the *USB 2.0 Specification*.

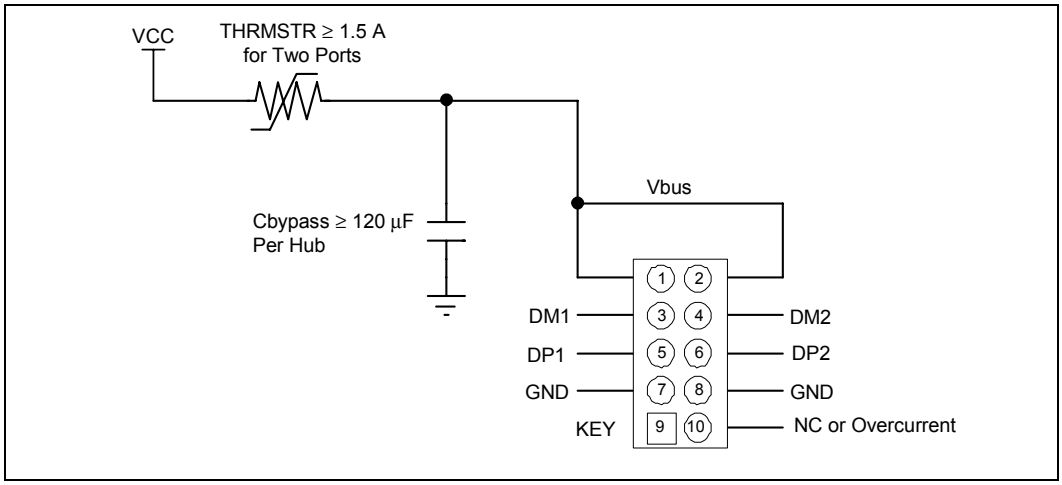
10.7.6.2.3 Pinout

A ten pin, 0.1 inch pitch stake pin assembly is recommended with the pinout listed in Table 10-14 and schematic shown in Figure 10-19.

Table 10-14. Front Panel Header Pinout

Pin	Description
1	VCC
2	VCC
3	dm1
4	dm2
5	dp1
6	dp2
7	VSS
8	VSS
9	key
10	No connect or over-current sense

Figure 10-31. Front Panel Header Schematic



It is highly recommended that the fuse element (thermistor) for the front panel header be included on the motherboard to protect the motherboard from damage for the following reasons:

- This protects the motherboard from damage in the case where an un-fused front panel cable solution is used.
- It also provides protection from damage if an un-keyed cable is inadvertently plugged onto the front panel USB connector.
- It provides protection to the motherboard in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between VBUS and ground.

10.7.6.2.4 Routing Considerations

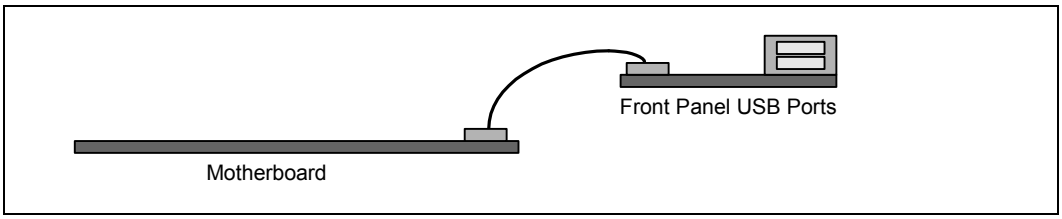
- Traces or surface shapes from VCC to the thermistor, to C_{BYPASS} and to the connector power and ground pins should be at least 50-mils wide to ensure adequate current carrying capability.
- There should be double vias on power and ground nets and the trace lengths should be kept as short as possible.

10.7.6.3 Front Panel Connector Card

The best way to provide front or side panel support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. Figure 10-20 shows the major components associated with a typical front/side panel USB solution that uses a front panel connector card. For more information, refer to the FPIO design guideline available at:

http://www.formfactors.org/developer/fpio_design_guideline.pdf.

Figure 10-32. Motherboard Front Panel USB Support



When designing the motherboard with front/side panel support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a connector card, ensure that there are not duplicate EMI/ESD/thermistor components placed on the motherboard, as this will usually cause drop/droop and signal quality degradation or failure.

10.7.6.3.5 Front Panel Daughter Card Design Guidelines

- Place the VBUS bypass capacitance, CMC, and ESD suppression components on the daughter card as close as possible to the connector pins.
- Follow the same layout, routing, and impedance control guidelines as specified for motherboards.
- Minimize the trace length on the front panel connector card. Less than 2-inch trace length is recommended.
- Use the same mating connector pin-out as outlined for the motherboard in Chapter 10.7.6.2.
- Use the same routing guidelines as described in Chapter 10.7.1.
- Trace length guidelines are given in Table 10-12.

10.8 Interrupt Interface

The interrupt capabilities of the ICH5 platform maintain the support for up to eight PCI interrupt pins and PCI 2.3 Message-Based Interrupts. In addition, the ICH5 supports FSB interrupt delivery.

10.8.1 PIRQ Routing Example

Table 10-15 shows how the ICH5 uses the PCI IRQ when the I/O APIC is active.

Table 10-15. I/O APIC Interrupt Inputs 16 thru 23 Usage

No	IOAPIC INTIN PIN	Function in Intel® ICH5 using the PCI IRQ in I/O APIC
1	IOAPIC INTIN PIN 16 (PIRQA)	USB UHCI Controller #1; USB UHCI Controller #4
2	IOAPIC INTIN PIN 17 (PIRQB)	AC '97 Audio and Modem; option for SMBus
3	IOAPIC INTIN PIN 18 (PIRQC)	USB UHCI Controller #3; SATA/IDE Native Mode
4	IOAPIC INTIN PIN 19 (PIRQD)	USB UHCI Controller #2
5	IOAPIC INTIN PIN 20 (PIRQE)	Internal LAN; option for SCI, TCO, HPET #0,1,2
6	IOAPIC INTIN PIN 21 (PIRQF)	Option for SCI, TCO, HPET #0,1,2
7	IOAPIC INTIN PIN 22 (PIRQG)	Option for SCI, TCO, HPET #0,1,2
8	IOAPIC INTIN PIN 23 (PIRQH)	USB EHCI Controller, Option for SCI, TCO, HPET #0,1,2

Due to different system configurations, IRQ line routing to the PCI slots ("swizzling") should be made to minimize the sharing of interrupts between both internal ICH5 functions and PCI functions. Figure 10-33 shows an example of IRQ line routing to the PCI slots (note: it is not necessarily an optimal routing scheme; an optimal scheme depends on individual system PCI IRQ usage).

Figure 10-33. Example PIRQ Routing

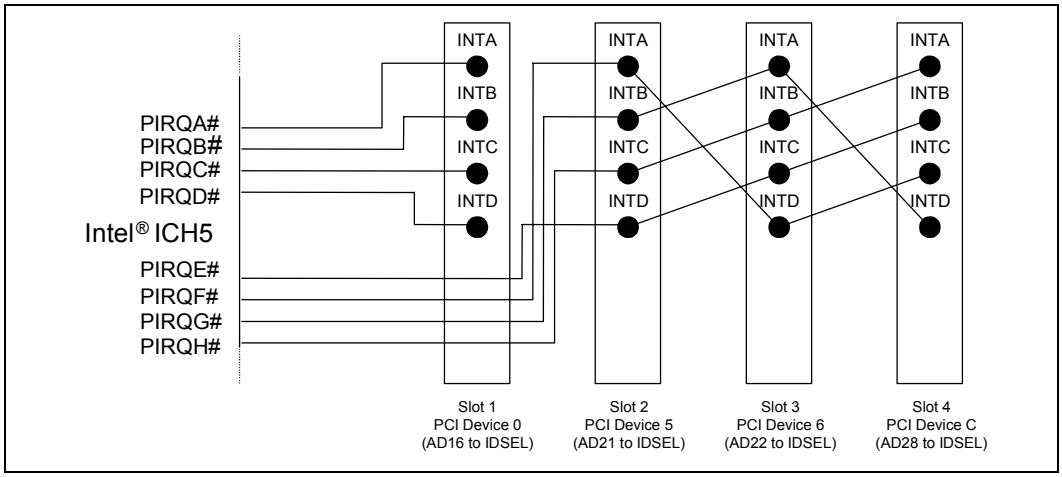


Figure 10-33 is an example. It is up to the board designer to route these signals in a way that will prove the most efficient for their particular system. A PCI slot can be routed to share interrupts with any of the ICH5's internal device/functions (but at a higher latency cost).

10.9 SMBus 2.0/SMLink Interface

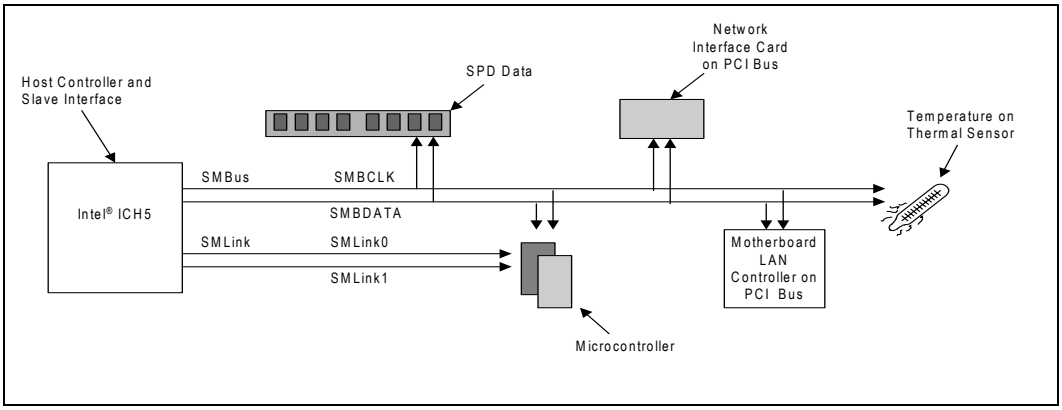
The SMBus interface on the ICH5 uses two signals (SMBCLK and SMBDATA) to send and receive data from components residing on the bus. These signals are used by the SMBus Host, SMBus Slave, and TCO controllers. These controllers reside inside the ICH5.

The ICH5 incorporates a SMLink interface, through SMLINK[1:0], supporting ASF Management. The SMLink is a dedicated bus between the ICH5 LAN controller and the integrated ASF Management controller. If the integrated ASF controller is disabled, an external microcontroller (e.g., a Baseboard Management Controller (BMC)) may communicate with the ICH5 LAN controller via SMLink and to the TCO logic through the Host SMBus signals. This also allows an external LAN controller to receive TCO messages on the SMBus if the integrated LAN controller is not enabled.

Note: In previous ICHx products a BMC communicated to the internal TCO logic through the SMLink signals. However, to have TCO connectivity on ICH5 platforms, the BMC must be connected to the SMBus signals of the ICH5. TCO connectivity is no longer routed internally through the SMLink.

Note: The requirement to tie both SMLink and SMBus signals externally is not needed, as slave functionality is available on the SMBus pins.

Figure 10-34. SMBUS 2.0/SMLink Interface



10.9.1 SMBus Design Considerations

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

- Device class (High/Low power). Most designs use primarily High Power Devices.
- Are there devices that must run in S3?
- Amount of VCC_SUSPEND current available (i.e., minimizing load of VCC_SUSPEND).

10.9.2 General Design Issues / Notes

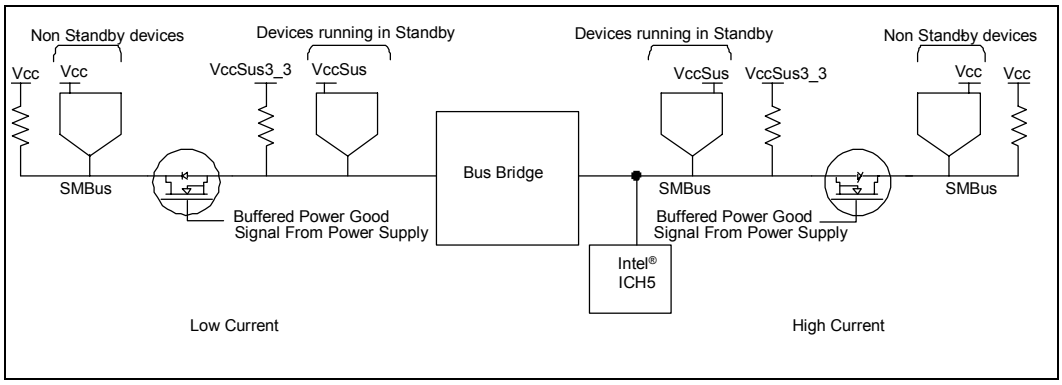
Regardless of the architecture used, there are some general considerations:

- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and fall time specification.
- The maximum bus capacitance that a physical segment can reach is 400 pF.
- SMBus devices that can operate in STR must be powered by the VCC_SUSPEND supply.
- It is recommended that I^2C devices be powered by the VCC_CORE supply. During an SMBus transaction in which the device is sending information to the ICH5, the device may not release the SMBus if the ICH5 receives an asynchronous reset. VCC_CORE is used to allow BIOS to reset the device if necessary. SMBus 2.0-compliant devices have a timeout capability which makes them insusceptible to this I^2C issue, allowing flexibility in choosing a voltage supply.
- If SMBus is connected to PCI it must be connected to all PCI slots.

10.9.3 High-Power/Low-Power Mixed Architecture

This design allows for current isolation of high and low current devices while also allowing SMBus devices to communicate while in S3. VCC_SUSPEND leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of a “FET” to isolate the devices powered by the core and suspend supplies (see Figure 10-35).

Figure 10-35. High Power/Low Power Mixed VCC_SUSPEND/ VCC_CORE_Architecture



Added considerations for mixed architecture are:

- The bus switch must be powered by VCC_SUSPEND.
- Devices that are powered by the VCC_SUSPEND well must not drive into other devices that are powered off. This is accomplished with the “bus switch.”
- The bus bridge can be a device like the Phillips PCA9515.

10.9.4 Calculating The Physical Segment Pull-Up Resistor

Table 10-16 and Table 10-17 are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. If any physical bus segment exceeds 400 pF, then a bus bridge device, like the Phillips PCA9515, must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 10-16. Bus Capacitance Reference Chart

Device	No. of Devices/ Trace Length	Capacitance Includes	Cap (pF)
Intel® ICH5	1	Pin Capacitance	12
CK409	1	Pin Capacitance	10
DIMMS	2	Pin Capacitance (10 pF) + 1 inch worth of trace capacitance (2 pF/inch) per DIMM and 2 pF connector capacitance per DIMM.	28
	3		42
PCI Slots	2	Each PCI add-in card is allowed up to 40 pF + 3 pF per each connector.	86
	3		129
	4		172
	5		215
	6		258
SMBus Trace Length in inches	=24	2 pF per inch of trace length	48
	=36		72
	=48		96
CNR	1	Pin Capacitance (10 pF) + 6 inches worth of trace capacitance (2 pF/inch) and 2 pF connector capacitance	24

Table 10-17. Bus Capacitance/Pull-Up Resistor Relationship

Physical Bus Segment Capacitance	Pull-Up Range (For VCC = 3.3 V
0 to 100 pF	8.2 kΩ to 1.2 kΩ
100 to 200 pF	4.7 kΩ to 1.2 kΩ
200 to 300 pF	3.3 kΩ to 1.2 kΩ
300 to 400 pF	2.2 kΩ to 1.2 kΩ

10.10 PCI

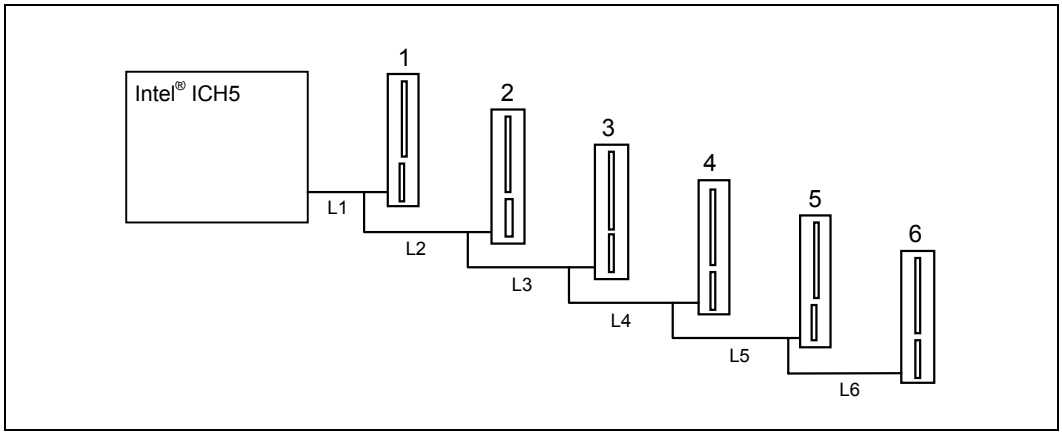
The ICH5 provides a PCI Bus interface that is compliant with the PCI Local Bus Specification, Revision 2.3. The implementation is optimized for high-performance data streaming when the ICH5 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.3*.

The ICH5 supports six PCI Bus masters (excluding the ICH5), by providing six REQ#/GNT# pairs. In addition, the ICH5 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

10.10.1 PCI Routing Summary

The following represents a summary of the routing guidelines for the PCI Slots. Simulations assume that PCI cards follow the *PCI Local Bus Specification, Revision 2.3* trace length guidelines.

Figure 10-36. PCI Bus Layout Example



Note: If a CNR connector is placed on the platform, it will share a slot space with one of the PCI slots; however, it will not take away from the slot functionality unless the CNR slot is occupied by a CNR card.

Figure 10-37. PCI Bus Layout Example with IDSEL

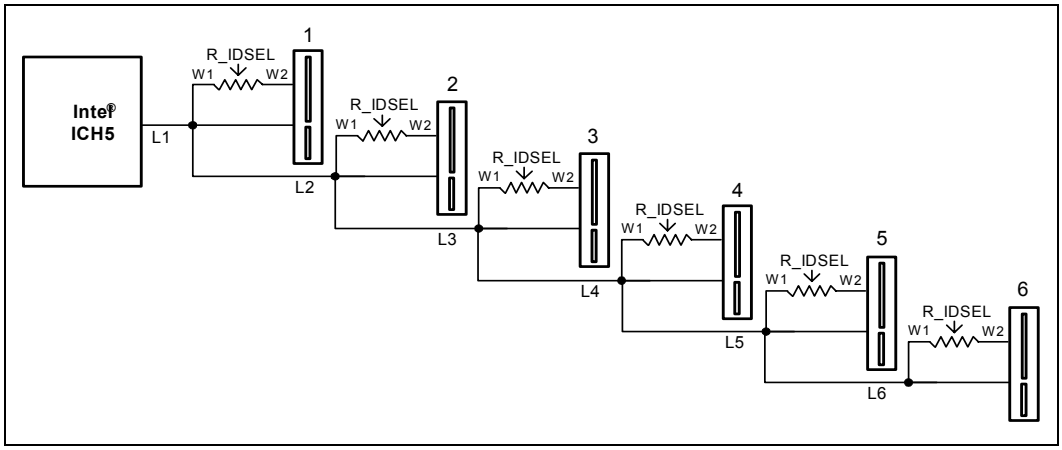


Table 10-18. PCI Data Signals Routing Summary

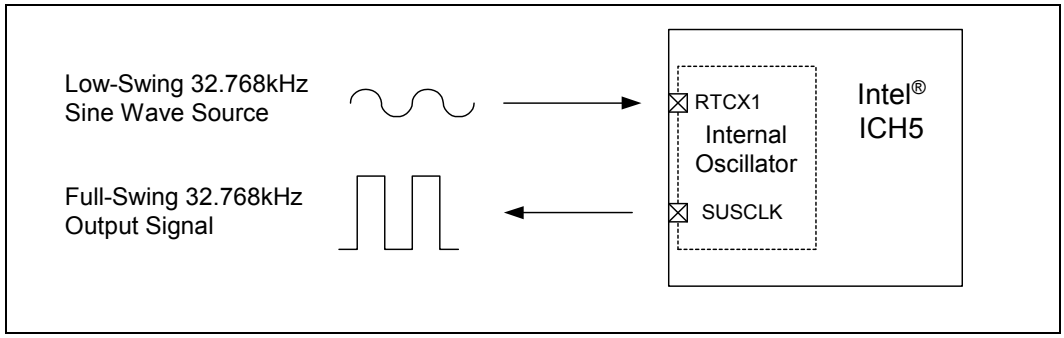
Trace Impedance	PCI Routing Requirements	Topology	Maximum Trace Length					
			L1	L2	L3	L4	L5	L6
60 Ω ± 15%	5 on 7 (Based on stack-up described in Chapter 3).	2 Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10 inches	1.0 inch	N/A	N/A	N/A	N/A
		3 Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10 inches	1.0 inch	1.0 inch	N/A	N/A	N/A
		4 Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10 inches	1.0 inch	1.0 inch	1.0 inch	N/A	N/A
		5 Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 8 inches	1.0 inch	1.0 inch	1.0 inch	1.0 inch	N/A
		6 Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 7 inches	1.0 inch	1.0 inch	1.0 inch	1.0 inch	1.0 inch

10.11 RTC

The ICH5 contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH5 uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH5, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use. This output ball of the ICH5 is called SUSCLK. This is illustrated in Figure 10-38.

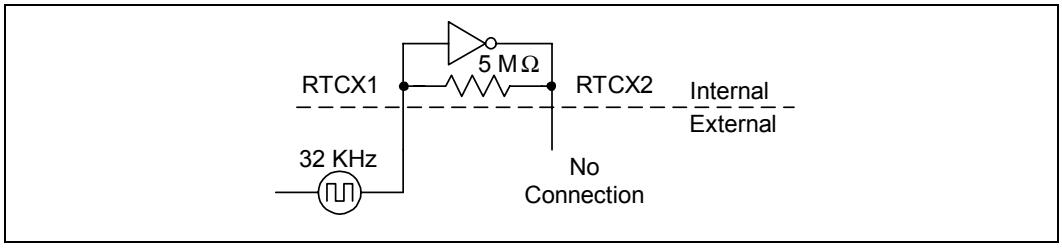
Figure 10-38. RTCX1 and SUSCLK Relationship in Intel® ICH5



For further information on the RTC, refer to Application Note *AP-728, ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*. This application note is valid for ICH5.

Even if the ICH5 internal RTC is not used, it is still necessary to supply a clock input to RTCX1 on the ICH5 because other signals are gated from that clock in suspend modes. However, in this case, the frequency accuracy (32.768 kHz) of the clock inputs is not critical; a cheap crystal can be used or a single clock input can be driven into RTCX1with RTCX2 left as no connect; Figure 10-39 illustrates the connection.

Figure 10-39. External Circuitry for the Intel® ICH5 Where the Internal RTC Is Not Used



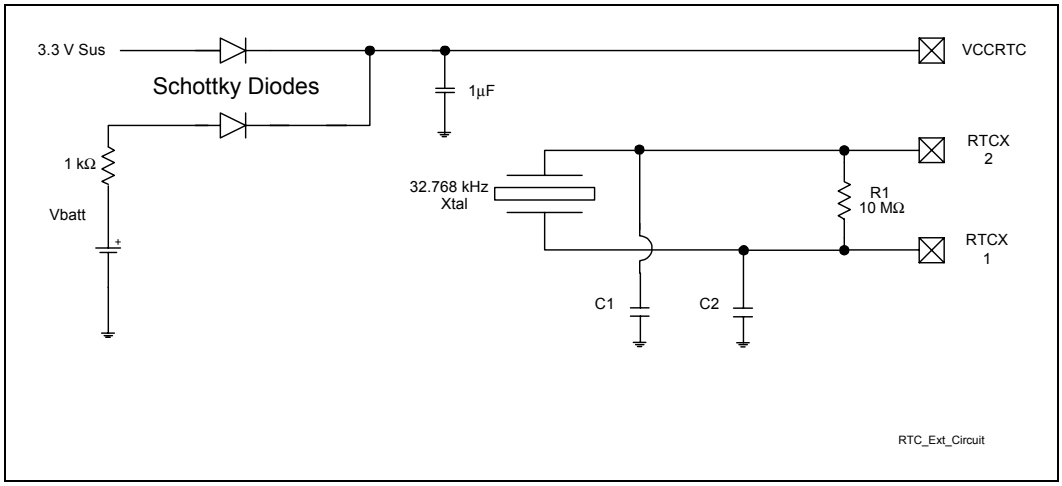
Note: Although this is a not a validated solution on ICH5, note that the peak-to-peak swing on RTCX1 can not exceed 700 mV or swing below 300 mV.

10.11.1 RTC Crystal

The ICH5 RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 10-40 shows the external circuitry that comprises the oscillator of the ICH5 RTC.

Note: The VBIAS ball was used in ICH4 to provide a reference voltage for the oscillator and buffer circuitry. This functionality is integrated in the ICH5. The VBIAS ball was removed from ICH5.

Figure 10-40. External Circuitry for the Intel® ICH5 RTC



NOTES:
1. The exact capacitor values for C1 and C2 must be based on the crystal maker recommendations. Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.
2. Reference designators are arbitrarily assigned.
3. 3.3 V Sus is active when the system is plugged in.
4. Vbatt is voltage provided by the battery.
5. VCCRTC, RTCX1, and RTCX2 are ICH5 pins.
6. VCCRTC powers the ICH5 RTC well.
7. RTCX1 is the input to the internal oscillator.

8. RTCX2 is the feedback for the external crystal.

Table 10-19. RTC Routing Summary

Trace Impedance	RTC Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R1, R2, C1, and C2 tolerances	Signal Referencing
60 Ω ± 15%	5-mil trace width (results in ~2 pF per inch)	1 inch	N/A	R1 = 10 MΩ ± 5% C1 = C2 = (NPO class) See Section 10.11.2 for calculating a specific capacitance value for C1 and C2	Ground

10.11.2 External Capacitors

To maintain the RTC accuracy, the external capacitor values C_1 and C_2 should be chosen to provide the manufacturer's specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})*(C_2 + C_{in2} + C_{trace2})] / [(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

- C_{load} = Crystal's load capacitance. This value can be obtained from the Crystal specification.
- Cin1, Cin2 = input capacitances at RTCX1, RTCX2 balls of the ICH5. These values can be obtained in the ICH5 datasheet.
- C_{trace1}, C_{trace2} = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. A typical value, based on a 5 mil wide trace and a ½ ounce copper pour, is approximately equal to: C_{trace} = trace length * 2 pF/inch
- $C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the exist of 2 electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C1, C2 can be chosen such that C1 = C2. Using the equation of C_{load} above, the value of C1, C2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C2 can be chosen such that C2 > C1. Then C1 can be trimmed to obtain the 32.768 kHz.

In certain conditions, both C_1, C_2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C_1, C_2 value are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example illustrates the use of the practical values C_1, C_2 in the case that theoretical values can not guarantee the accuracy of the RTC in low temperature condition:

Example

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH5, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25 °C) to yield a 32.768 kHz oscillation.

At 0 °C the frequency stability of the crystal gives –23 ppm (assumed that the circuit has 0 ppm at 25 °C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C_1, C_2 are chosen to be 6.8 pF instead of 10 pF. This will make the RTC oscillate at higher frequency at room temperature (+23 ppm) but this configuration of C_1 / C_2 makes the circuit oscillate closer to 32.768 kHz at 0 °C. The 6.8 pF value of C1 and 2 is the **practical value**.

Note: The temperature dependency of crystal frequency is parabolic relationship (ppm / degree square). The effect of changing the crystal's frequency when operating at 0 °C (25 °C below room temperature) is the same when operating at 50 °C (25 °C above room temperature). See the crystal datasheet for more details.

10.11.3 RTC Layout Considerations

Since the RTC circuit is very sensitive and requires highly accurate oscillation, reasonable care must be taken during layout and routing RTC circuit. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. The ICH5 recommends a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR-4, a 5-mil trace has approximately 2 pF per inch.
- Trace signal coupling must be importantly reduced, by avoiding routing of adjacent PCI signals close to RTCX1 and RTCX2.
- Ground guard plane is highly recommended.
- The oscillator VCC should be clean; use a filter, such as a RC low-pass, or a ferrite inductor.

10.11.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH5 is not powered by the system.

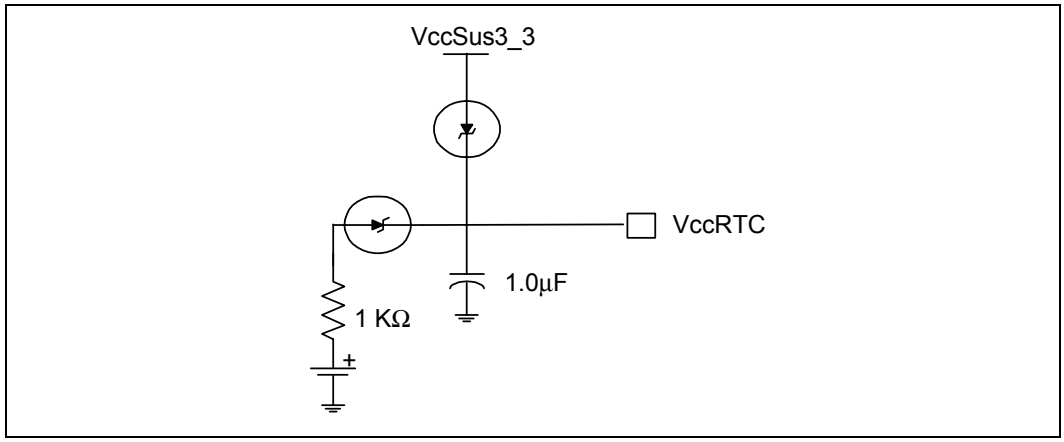
Example batteries are: Duracell 2032, 2025, or 2016 (or equivalent) that can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 5 µA, the battery life will be at least:

$$170{,}000\ \mu Ah / 5\ \mu A = 34{,}000\ h = 3.3\ years$$

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases.

The battery must be connected to the ICH5 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH5 RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 10-41 is an example of a diode circuit that is used.

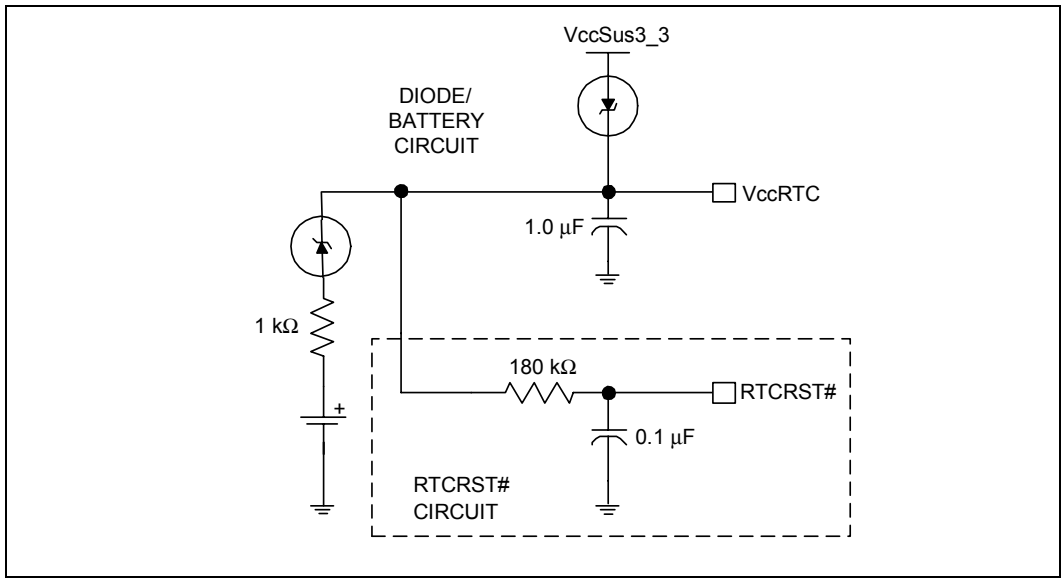
Figure 10-41. A Diode Circuit to Connect RTC External Battery



A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

10.11.5 RTC External RTCRST# Circuit

Figure 10-42. RTCRST# External Circuit for the Intel® ICH5 RTC



The ICH5 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create a RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18 ms – 25 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

The RTCRST# signal may also be used to detect a low battery voltage. RTCRST# will be asserted during a power up from G3 state if the battery voltage is below 2 V. This will set the RTC_PWR_STS bit as described above. If desired, BIOS may request that the user replace the battery.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 10-41) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 10-42 is an example of this circuitry that is used in conjunction with the external diode circuit.

10.11.6 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), the SUSCLK duty cycle can be between 30 – 70%.

If the SUSCLK duty cycle is beyond 30 – 70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50 Ω input impedance probe) and it is an appropriate signal to check the RTC frequency to determine the accuracy of the ICH5's RTC Clock (see *AP-728, Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions* for further details).

10.11.7 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST#, when configured as shown in Figure 10-42, meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VCCRTC. This prevents these nodes from floating in G3, and correspondingly prevents ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

10.12 Internal LAN Layout Guidelines

The ICH5 provides several options for LAN capability. The platform supports several components depending on the target market. Available LAN components include the 82547EI Gigabit Ethernet controller (GbE), the Intel 82540EM GbE controller, Intel 82551QM Fast Ethernet controller, 82562EZ/ET and 82562EX/EM Platform LAN Connect (PLC) components.

Note: Although the 82547EI GbE controller is a possible LAN solution in an ICH5 platform, this LAN device interfaces through the CSA port. See Chapter 9, "CSA Port".

Table 10-20. LAN Component Connections/Features

LAN Component	Interface To Intel® ICH5	Connection	Features
Intel® 82547EI (196 BGA)	N/A	GbE (1000BASE-T) with Alert Standard Format (ASF) alerting	GbE, ASF 2.0 alerting, CSA Port
Intel® 82540EM (196 BGA)	PCI	GbE (1000BASE-T) with Alert Standard Format (ASF) alerting	GbE, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82551QM (196 BGA)	PCI	Performance 10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82562EM (48 Pin SSOP) Intel® 82562EX (196 BGA)	LCI	10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting
Intel® 82562ET (48 Pin SSOP) Intel® 82562EZ (196 BGA)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

NOTE: The 82547EI, 82540EM, 82551QM, and 82562EX/EZ PLC devices are all footprint compatible. See Section 10.12.1

Which LAN component to use on the ICH5 platform depends on the end-user's need for connection speed, manageability needs, and bus connection type. In addition, footprint compatible packages make it possible to design a platform that can use any of the LAN components without the need for a motherboard redesign.

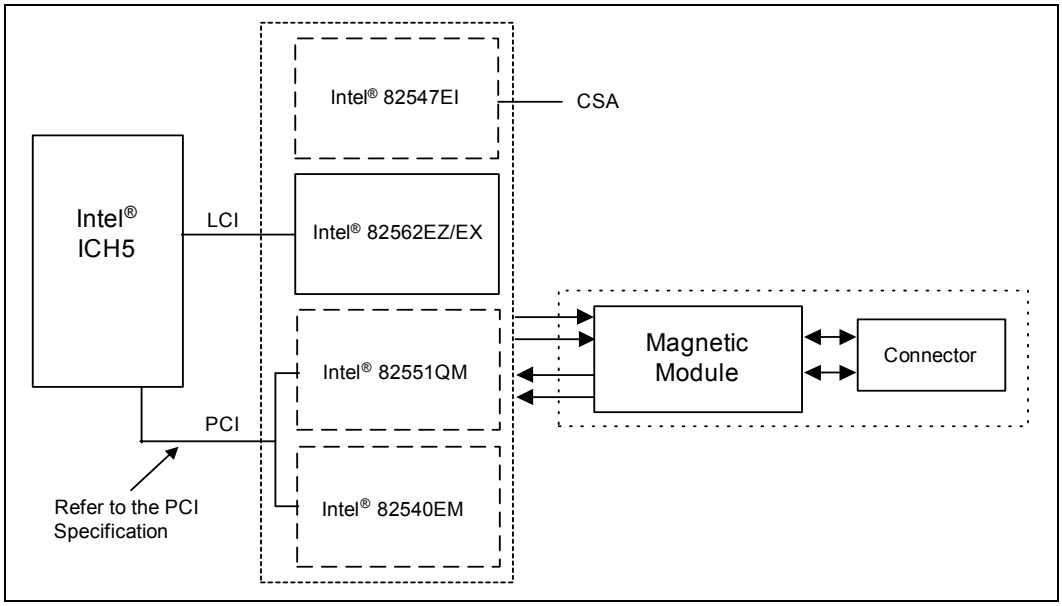
10.12.1 Footprint Compatibility

The 82547EI and 82540EM Gigabit Ethernet controllers, 82551QM Fast Ethernet controller, and 82562EX/EZ PLC devices are all manufactured in a footprint compatible15 mm x 15 mm (1 mm pitch), 196-ball grid array package. Many of the critical signal pin locations on the 82547EI, 82540EM, 82551QM, and 82562EX/82562EZ are identical, allowing designers to create a single design that accommodates any one of these parts. Because the usage of some pins on the 82547EI and 82540EM differ from the usage on the 82551QM or the 82562EX/82562EZ, the parts are not referred to as "pin compatible." The term "footprint compatible" refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design.

For those customers who are interested in dual-footprint designs for LAN on motherboard (LOM) with either 82547EI and 82562EZ(EX), 82540EM and 82562EZ(EX) or 82540EM and 82551QM, refer to the *82547EI/82562EZ(EX) Dual Footprint Design Guide*.

Design guidelines are provided for each required interface and connection. Refer to Figure 10-43 and Table 10-21 for the corresponding section of the design guide. The guidelines use the Intel 82562EZ to refer to both the 82562EZ and 82562EX. The 82562EX is specified in those cases where there is a difference.

Figure 10-43. Intel® ICH5/Platform LAN Connect Sections



NOTE: 82562EZ/EX PLC component, 82551 QM Fast Ethernet controller, and 82540EM GbE controller are footprint compatible with each other.

Table 10-21. LAN Design Guide Section Reference

Layout Section	Interface	Design Guide Section
Intel® 82562EZ/EX	LCI	Section 10.12.2, “Intel® ICH5 – LAN Connect Interface Guidelines through Section 10.12.4, “Intel® 82562EZ/EX Disable Guidelines
Intel® 82551QM	PCI	Section 10.12.5, “Design and Layout Considerations for Intel® 82540EM GbE Controller and Intel® 82551 QM Fast Ethernet Controller
Intel® 82540EM		
Intel® 82547EI	CSA	See Section 9.3.1, “Intel® 82547EI GbE Controller Layout Considerations

10.12.2 Intel® ICH5 – LAN Connect Interface Guidelines

This section contains guidelines on how to implement a Platform LAN Connect device on a system motherboard or on a CNR riser card. It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH5 LAN Connect interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports 82562EZ/ET and 82562EX/EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD0, and LAN_TXD0 are shared by all components.

10.12.2.1 Bus Topologies

The Platform LAN Connect interface can be configured in several topologies:

- Direct point-to-point connection between the ICH5 and the LAN component
- LOM/CNR Implementation

10.12.2.1.6 LOM (LAN On Motherboard) or CNR Point-to-Point Interconnect

The following are guidelines for a single solution motherboard. Either 82562EZ/ET PLC components, 82562EX/EM PLC components, or CNR are uniquely installed.

Figure 10-44. Single Solution Interconnect

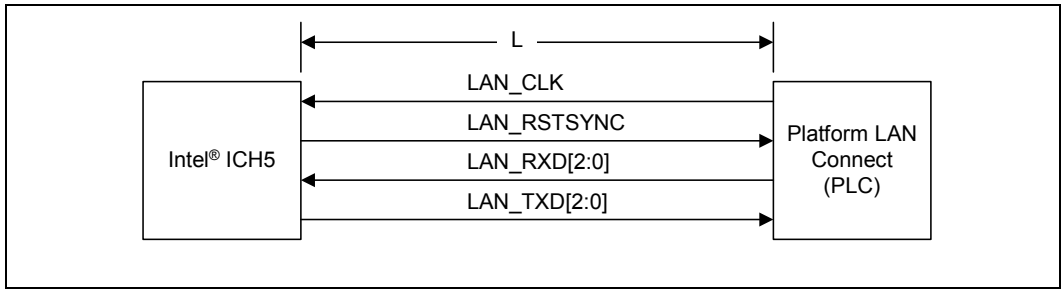


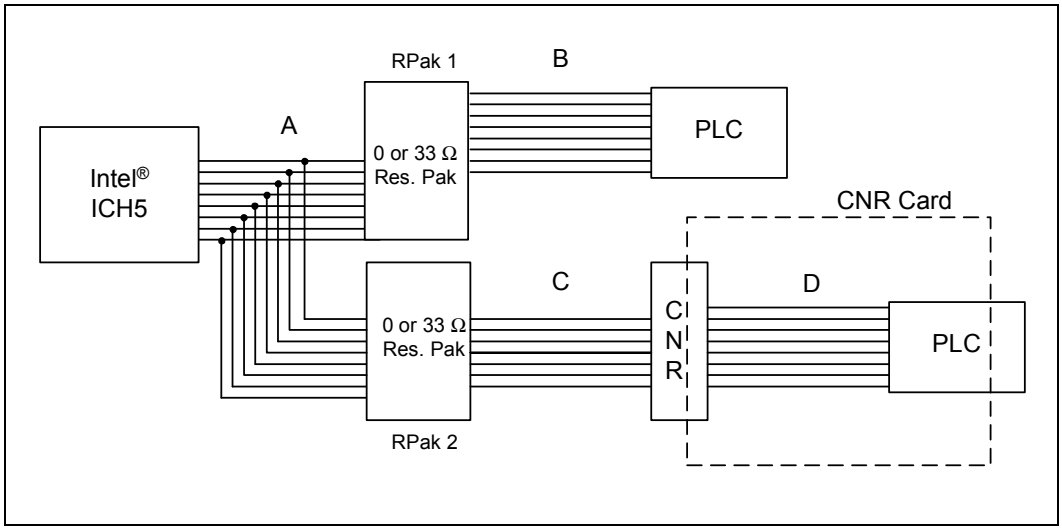
Table 10-22. LAN LOM or CNR Routing Summary

Device	Maximum Trace Length	Trace Impedance	LAN Routing Requirements	Signal Referencing	LAN Signal Length Matching
Intel® 82562EZ/EX	0.5 to 11.5 inches	60 Ω ± 15%	5 on 10 (Based on stack--up described in Chapter 3)	Ground	Data signals must be equal to or no more than 0.5 inch (500 mils) shorter than the LAN clock trace.
Intel® 82562EZ/EX on CNR	2 to 9 inches				

10.12.2.1.7 LOM (LAN On Motherboard) and CNR Interconnect

The following guidelines apply to an all-inclusive configuration of PLC design. This layout combines LAN on motherboard and the CNR solutions. The resistor pack ensures that either a CNR option or a LAN on motherboard option can be implemented at one time.

Figure 10-45. LOM/CNR Interconnect



NOTE: Either RPak 1 or RPak 2 can be populated, but not both.

Table 10-23. LAN LOM/CNR Dual Routing Summary

Device	Maximum Trace Length				LAN Trace Impedance/ Routing	Signal Reference	LAN Signal Length Matching
	A	B	C	D			
Intel® 82562EZ/ ET/EX/EM	0.5 to 6.5 inches	5 to (11.5 – A) inches	NA	NA	60 Ω ± 15% 5 on 10 (Based on stack-up described in Chapter 3)	Ground	Data signals must be equal to or no more than 0.5 inch (500 mils) shorter than the LAN clock trace.
Intel® 82562EZ/ ET/EX/EM on CNR[1]	0.5 to 6.5 inches	NA	1.5 to (9 – A) inches	0.5 to 3 inches			

NOTE:
1. Total motherboard trace length should not exceed 9 inches

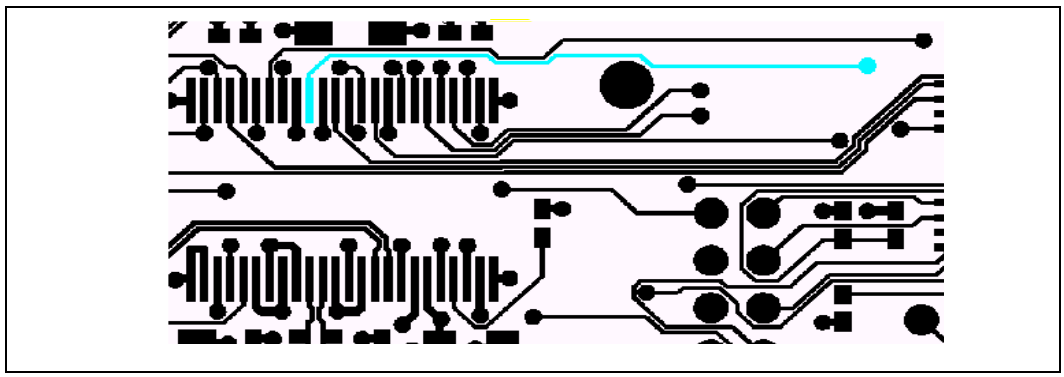
Additional guidelines for this configuration are as follows:

- Stubs due to the resistor pack should not be present on the interface.
- The resistor pack value can be 0 Ω or 33 Ω (see Section 10.12.2.5).

10.12.2.2 Signal Routing and Layout

Platform LAN Connect interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inch shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 10-46. LAN_CLK Routing Example



10.12.2.3 Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the t_{RMATCH} skew parameter. t_{RMATCH} is the sum of the trace length mismatch between LAN_CLK and the LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inch shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-PLC signals.

10.12.2.4 Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 Ω ± 15% is strongly recommended; otherwise, signal integrity requirements may be violated.

10.12.2.5 Line Termination

Line termination mechanisms are not specified for the LAN Connect interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 0 Ω or 33 Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

10.12.2.6 Terminating Unused LAN Connect Interface Signals

The LAN Connect interface on the ICH5 can be left as a no-connect if it is not used.

10.12.3 Design and Layout Considerations for Intel® 82562EZ/EX

For correct LAN performance, designers must follow the general guidelines outlined in Section 10.12.2. Additional guidelines for implementing an 82562EZ/EX Platform LAN Connect component are provided in the following sub-sections.

10.12.3.1 Guidelines for Intel® 82562EZ/EX Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section provides guidelines for component placement. Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

10.12.3.2 Crystals and Oscillators

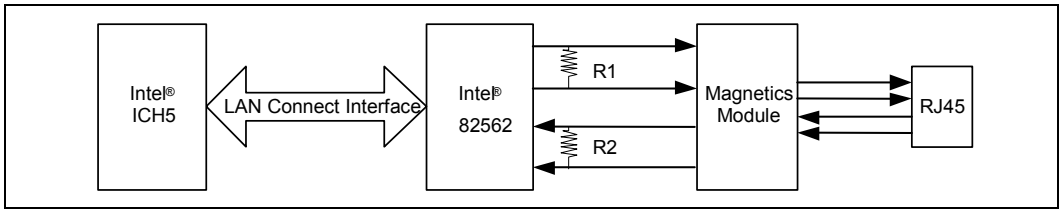
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562EZ/EX components, keeping the trace length as short as possible and do not route any noisy signals in this area.

10.12.3.3 Intel® 82562EZ/EX Termination Resistors

The 100 Ω ± 1% (R1) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 121 Ω ± 1% (R2) receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN connect component (82562EZ/EX) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (e.g., 82562EZ/EX), including the wire impedance reflected through the transformer.

Figure 10-47. Intel® 82562EZ/ET/EX/EM PLC Components/ Intel® 82551QM PLC Components Termination



NOTE: Place termination resistors as close to the Intel® 82562ET PLC component as possible.

10.12.3.4 Critical Dimensions with Discrete Magnetics Module

There are two dimensions to consider during layout. Distance ‘A’ from the line RJ45 connector to the magnetics module and distance ‘B’ from the 82562EZ/EX to the magnetics module. The combined total distances A and B must not exceed 4 inches (preferably, less than 2 inches—see Figure 10-48).

Figure 10-48. Critical Dimensions for Component Placement

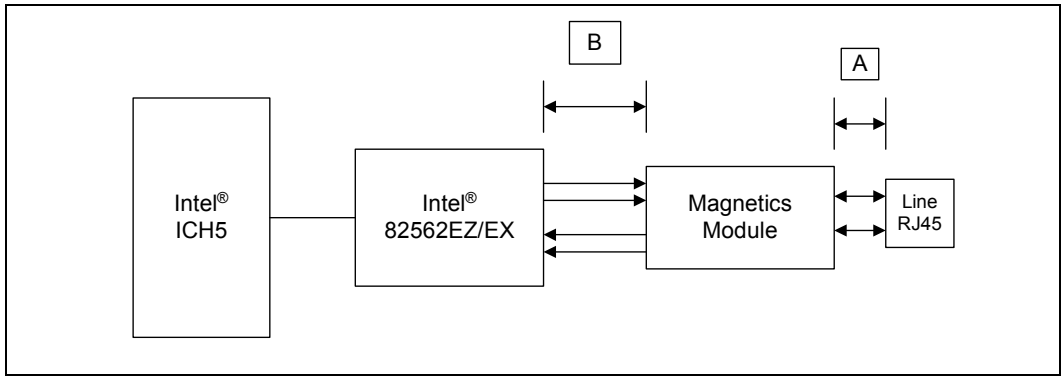


Table 10-24. Critical Dimensions for Component Placement

Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

10.12.3.4.8 Distance from Magnetics Module to RJ45 (Distance A)

The distance A in Figure 10-48 should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than 1 inch of separation. The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 60 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit’s performance and contribute to radiated emissions from the transmit circuit. If the 82562EZ/EX must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562EZ/EX and RJ45 as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105– 110 Ω should compensate for second order effects.

10.12.3.4.9 Distance from Intel® 82562EZ/EX to Magnetics Module (Distance B)

Distance B should also be designed to be less than 1 inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and equal length within each differential pair.

10.12.3.5 Critical Dimensions with Integrated Magnetics Module

For designs where the magnetics module is integrated into the RJ45 connector, the following guidelines apply. There are two dimensions to consider during layout. Distance 'A' from the line RJ45 connector to the 82562EZ/EX and distance 'B' from the 82562EZ/EX to the edge of the PCB as shown in Figure 10-49.

Figure 10-49. Critical Dimensions for Component Placement

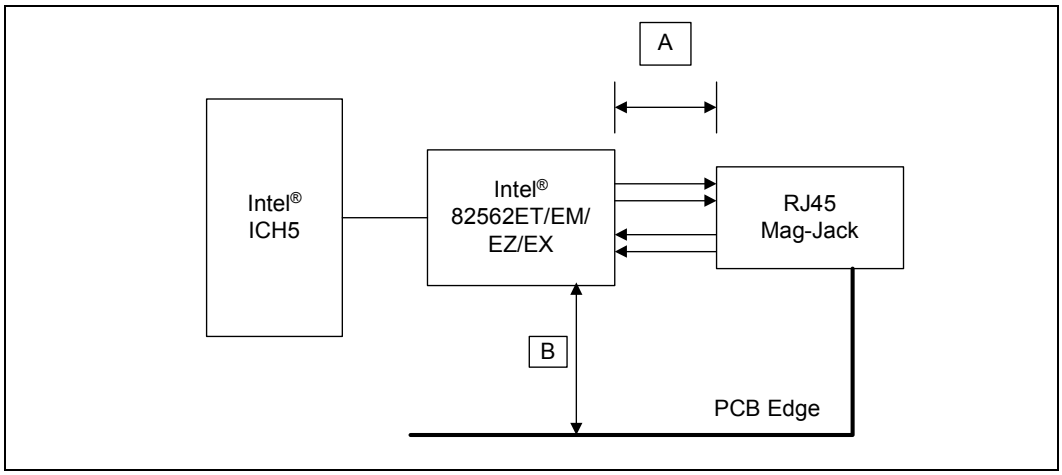


Table 10-25. Critical Dimensions for Component Placement

Distance	Guideline
A	Distance A must be such that the length of the differential signal pairs is less than 4 inches
B	Distance B must be greater than 2 inches

10.12.3.5.10 Distance from Intel® 82562EZ/EX to Mag-Jack (Distance A)

Distance A in Figure 10-49 should be chosen in such a way that the maximum length of the differential pairs from 82562EZ/EX to the Mag-jack should be less than 4 inches. The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 60 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (e.g., TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. Keeping the total distance between the 82562EZ/EX and Mag-jack as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 Ω – 110 Ω should compensate for second order effects.

10.12.3.5.11 Distance from Intel® 82562EZ/EX to PCB Edge (Distance B)

The distance from the 82562EZ/EX to the edge of the PCB should be greater than 2 inches.

10.12.3.6 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Signals with fast rise and fall times contain many high frequency harmonics that can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This results in a smaller loop area and reduces the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

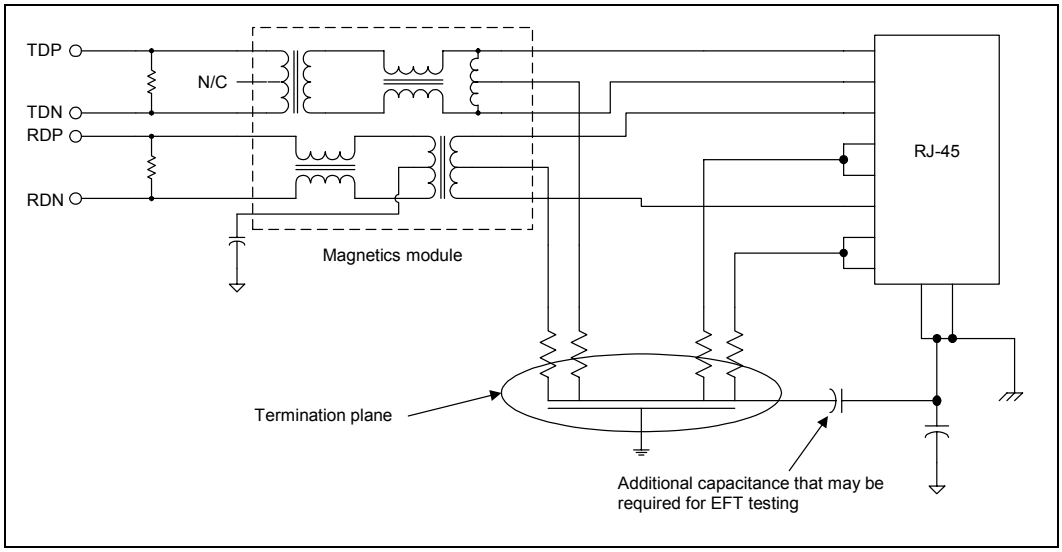
Terminating Unused Connections

In Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the "Bob Smith" Termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

10.12.3.6.12 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

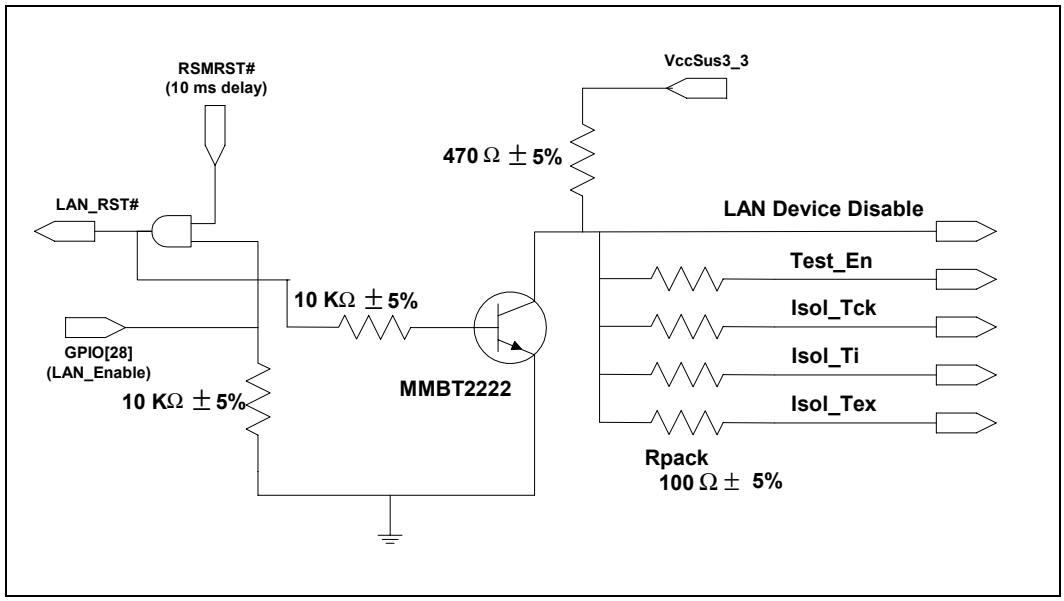
Figure 10-50. Termination Plane



10.12.4 Intel® 82562EZ/EX Disable Guidelines

To power down the 82562EZ/EX, the device must be isolated (disabled) prior to or during reset (LAN_RST#) asserting. Using a GPIO, such as GPIO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss, since GPIO28 is high during and after reset. The example circuit shown in Section 10-51 will correct this behavior. The BIOS controlling the GPIO can disable the 82562EZ/EX.

Figure 10-51. Intel® 82562EZ/ET/EX/EM PLC Components Disable Circuitry



NOTE: LAN_RST# needs to be held low for 10 ms after power is stable. It is assumed that the RSMRST# logic will provide this delay. Because GPIO[28] will be defaulted to high on power up, an AND gate has been implemented to ensure the required delay for LAN_RST# is met

There are four pins which are used to put the 82562EZ/EX in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 10-26 describes the operational/disable features for this design.

The four control signals shown in Table 10-26 should be configured as follows:

- Test_En should be pulled-down through a 100 Ω resistor.
- The remaining three control signals should each be connected through 100 Ω series resistors to the common node *Intel® 82562EZ/EX Disable* of the disable circuit.

Table 10-26. Intel® 82562EZ/EX Control Signals

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/o Clock (lowest power)

10.12.5 Design and Layout Considerations for Intel® 82540EM GbE Controller and Intel® 82551 QM Fast Ethernet Controller

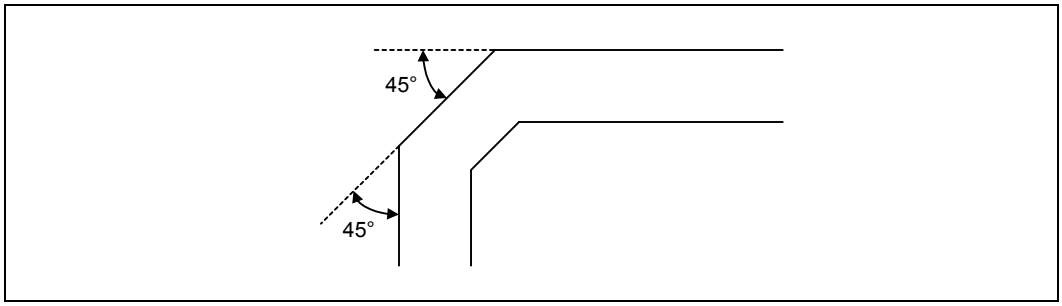
For specific design and layout considerations for the 82540EM GbE controller, refer to the *82540EM Gigabit Ethernet Controller Preliminary Datasheet and Hardware Design Guide.*

10.12.6 General LAN Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance (Note: Some suggestions are specific to a 4.3-mil stack-up.):

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. (Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).)
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, it is recommended to use two, 45-degree bends instead. Refer to Figure 10-52.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. As a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 10-52. Trace Routing



10.12.6.1 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge-to-edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than 1 inch to the connector/ magnetics/edge of the board.

10.12.6.2 Signal Isolation

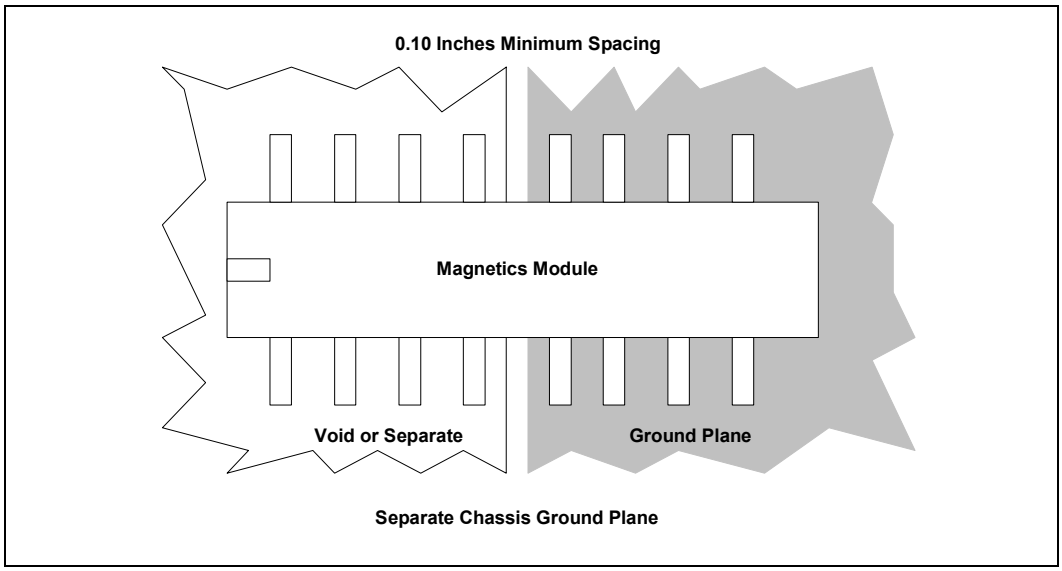
Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Note that over the length of the trace run, each differential pair should be at least 0.3 inch away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk that can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

10.12.6.3 Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 10-53. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

The following guidelines help reduce circuit inductance in both back planes and motherboards:

- Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics that can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

10.12.6.4 Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN On Motherboard designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. (Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise and distort the waveforms.
3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (= 1 inch).
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 300 mils from the differential traces.
5. Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 300 mils or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45, and the PLC.
6. Use of an inferior magnetics module. The magnetics modules that Intel uses have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
7. Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or application note.
8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The application notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they've designed for 100 Ω. (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close (see note) to each other, the edge coupling can lower the effective differential impedance by 5 Ω – 20 Ω. A 10 Ω – 15 Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.

10. Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the 82562ET PLC component side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a capacitor is put in either of these locations. If a capacitor is used; it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) These capacitors are not necessary, unless there is some overshoot in 100 Mbps mode.

Note: It is important to keep the two traces within a differential pair close to each other. *Close* should be considered to be less than 30 mils between the two traces within a differential pair. A 7 mil trace-to-trace spacing is recommended. Keeping the traces close helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces.

10.13 Trusted Platform Module Guidelines

Trusted Platform Module(s) (TPM) are a Trusted Computing Platform Alliance (TCPA) low cost security solution to increase confidence on Internet security. The TPM is a device that resides on the motherboard and is connected to the ICH5 using the Low Pin Count (LPC) bus to communicate with the rest of the platform.

10.13.1 TPM Design Considerations

Refer to the Platform Vision Guide for TPM specific design considerations.

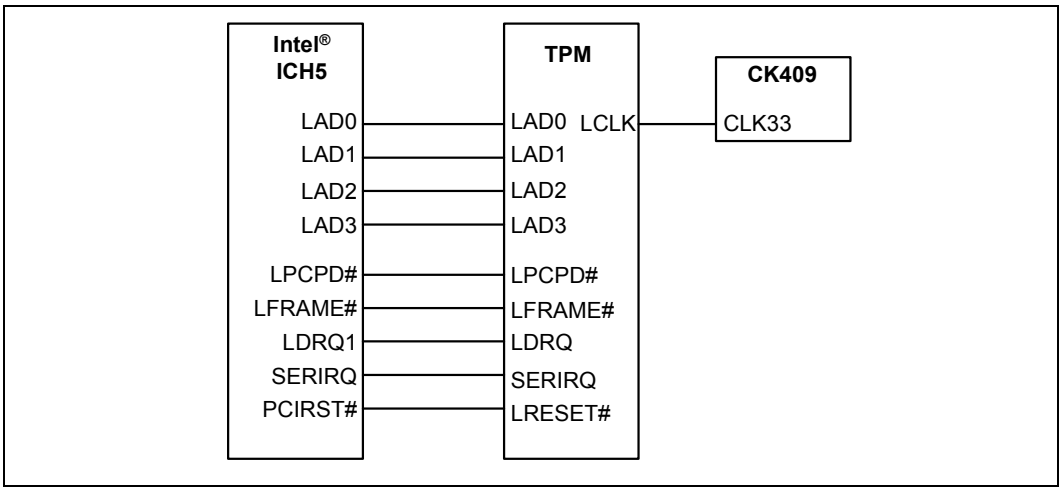
10.13.2 LPC Design Considerations

Routing requirements for the TPM's LPC interface are as follows:

- LAD[3:0] (address/data lines) are shared with the flash BIOS interface component and the Super I/O (SIO) device.
- LCLK (clock) should be connected to the 33 MHz clock.
- LRESET# (reset) should be connected to PCIRST#.
- LFRAME# (cycle termination) is shared with the flash BIOS and the SIO.
- SERIRQ (serialized IRQ) is shared with the SIO.
- LDRQ (DMA bus master request):
  - — ICH5 LDRQ1 should connect to the TPM.
  - — ICH5 LDRQ0 should connect to the SIO.
- LPCPD# (suspend status) is shared with the SIO.

Figure 10-54 is a block diagram showing the TPM LPC interconnect with the ICH5. The LPC signals shown in the block diagram are shared with other LPC components that reside on the LPC interconnect (e.g., SIO and flash BIOS).

Figure 10-54. TPM LPC Block Diagram



An example TPM implementation is available in the Customer Reference Board Schematics.

10.13.3 Motherboard Placement Consideration

Optimum routing can typically be achieved by placing the TPM in proximity to the ICH5 or other LPC peripherals (e.g., Firmware Hub, Super I/O).

The TPM is a security device that should be shielded as much as possible from physical access. In high-security implementations there are a number of mechanisms that can be used to detect or prevent physical system intrusion; such mechanisms are beyond the scope of this Design Guide. However, convenience of physical access to the TPM can be minimized by placing the TPM behind the memory DIMMs. In an ATX or µATX chassis the area behind the memory is positioned behind the disk drives when installed in a tower chassis. Drive bays or cables will make physical access to the TPM more difficult than if it was left out in the open portions of the motherboard.

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Intel® ICH5 Power Management 11

11.1 SYS_RESET# Usage Model

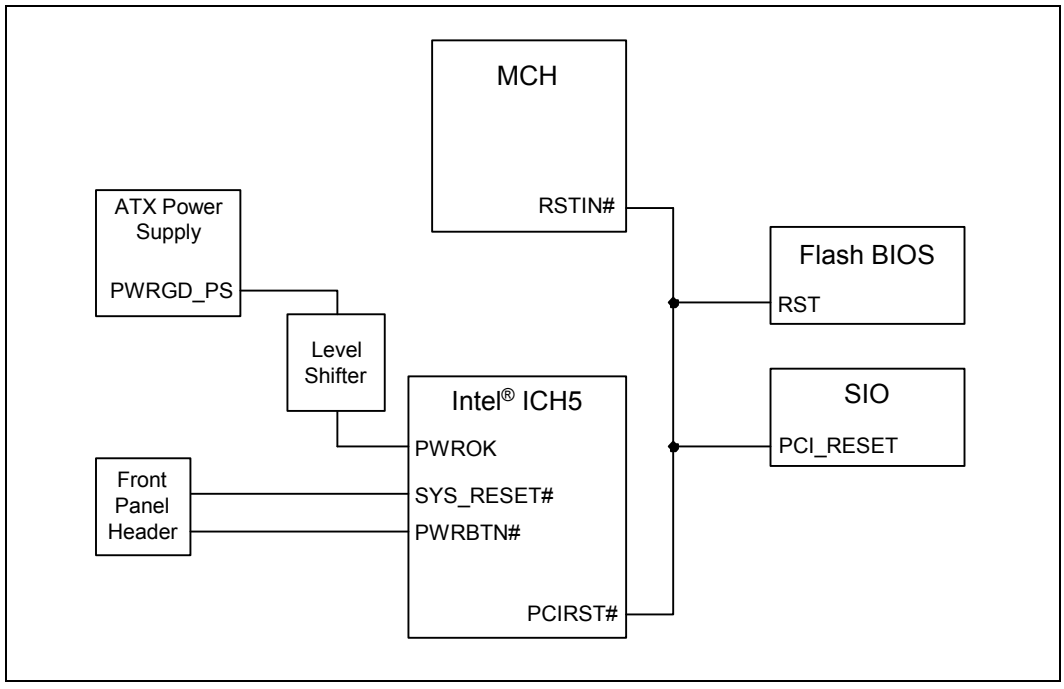
The System Reset ball (SYS_RESET#) on the ICH5 can be connected directly to the reset button on the systems front panel provided that the front panel header pulls this signal up to 3.3 V SB through a weak pull-up resistor. The ICH5 will debounce signals on this pin (16 ms) and allow the SMBus to go idle before resetting the system. This helps prevent a slave device on the SMBus from "hanging" by resetting in the middle of a cycle.

Note: The PWROK signal should not be used to implement front panel reset.

11.2 PWRBTN# Usage Model

The Power Button ball (PWRBTN#) on the ICH5 can be connected directly to the power button on the systems front panel. This signal is internally pulled-up in the ICH5 to 3.3 V SB through a weak pull-up resistor (24 kΩ nominal). The ICH5 has 16 ms of internal debounce logic on this pin.

Figure 11-1. SYS_RESET# and PWRBTN# Connection

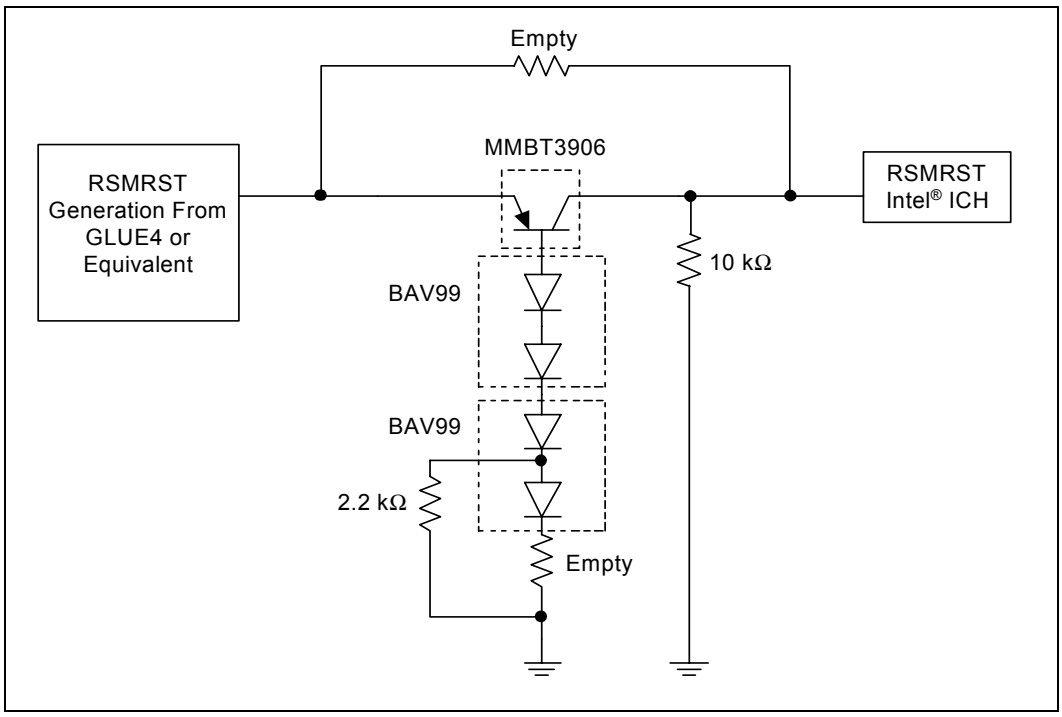


NOTE: SYS_RESET# is 3.3 V tolerant and should be pulled up to 3.3 V SB by the front panel header.

11.3 Power-Well Isolation Control Strap Requirements

The circuit shown in Figure 11-2 can be implemented to control well isolation between the VCCSUS3_3 and RTC power-wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail. Failure to implement this circuit or a circuit that functions similar to this may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power). Droop on this node can potentially cause the CMOS to be cleared or corrupted, the RTC to loose time after several AC power cycles, or the intruder bit might assert erroneously.

Figure 11-2. RTC Power Well Isolation Control



Intel® ICH5 General Purpose I/O 12

12.1 GPIO Summary

The ICH5 has 12 general purpose inputs, 8 general purpose outputs, and 16 general purpose inputs/ outputs. Some of these general purpose inputs and outputs have native functions assigned.

Table 12-1. GPIO Summary (Sheet 1 of 2)

GPIO #	Power Well	Input/ Output/ Input-Output	Tolerance
0(2)	Core	Input	5 V
1(2)	Core	Input	5 V
2(2)	Core	Input	5 V
3(2)	Core	Input	5 V
4(2)	Core	Input	5 V
5(2)	Core	Input	5 V
6	Core	Input	5 V
7	Core	Input	5 V
8	Resume	Input	3.3 V
9	Resume	Input	3.3 V
10	Resume	Input	3.3 V
11(2)	Resume	Input	3.3 V
12	Resume	Input	3.3 V
13	Resume	Input	3.3 V
14	Resume	Input	3.3 V
15	Resume	Input	3.3 V
16(2)	Core	Output	3.3 V
17(2)	Core	Output	3.3 V
18	Core	Output	3.3 V
19	Core	Output	3.3 V
20	Core	Output	3.3 V
21	Core	Output	3.3 V
22	Core	Output (Open Drain)	3.3 V
23	Core	Output	3.3 V
24	Resume	Input-Output (1)	3.3 V
25	Resume	Input-Output (1)	3.3 V
27	Resume	Input-Output (1)	3.3 V
28	Resume	Input-Output (1)	3.3 V
32	Core	Input-Output (1)	3.3 V

Table 12-1. GPIO Summary (Sheet 2 of 2)

GPIO #	Power Well	Input/ Output/ Input-Output	Tolerance
34	Core	Input/Output (1)	3.3 V
40	Core	Input	3.3 V
41	Core	Input	3.3 V
48	Core	Output	3.3 V
49	Processor I/O	Output	3.3 V

NOTES:
1. Defaults as an output to the ICH5
2. Can be used as GPIO if the native function is not needed. ICH5 defaults these signals to native functionality.

Intel® ICH5 System Design Considerations 13

13.1 Intel® ICH5 Power Consumption

Table 13-1 shows the ICH5 power consumption estimates.

Table 13-1. Intel® ICH5 Maximum Power Consumption Estimates

Power Plane	Maximum Power Consumption				
	S0	S1	S3	S4/S5	G3
1.5 V Core	770 mA	201 mA	N/A	N/A	N/A
3.3 V I/O	480 mA	1 mA	N/A	N/A	N/A
3.3 V SUS[1,2]	360 mA	73 mA	73 mA	73 mA	N/A
VCCRTC[3,4]	N/A	N/A	N/A	N/A	6 µA
V_CPU_IO	2.5 mA	2.5 mA	N/A	N/A	N/A

NOTES:
1. 3.3 V SUS assumes eight high-speed ports populated.
2. Due to the integrated voltage regulator, 1.5 V SUS is included in the 3.3 V SUS rail.
3. Only the G3 state of this rail is shown to provide an estimate of battery life.
4. Icc (RTC) data is taken with VccRTC at 3.0 V while the system in a mechanical off (G3) state at room temperature.

13.2 Thermal Design Power

For Information on ICH5/ICH5R thermal design, refer to the *Intel® 82801EB I/O Controller Hub 5 (ICH5) and Intel® 82801ER I/O Controller Hub 5 R (ICH5R) Thermal Design Guide.*

13.3 Glue Chip 4 (Intel® ICH5 Glue Chip)

To reduce the component count and Bill-Of-Material (BOM) cost of the ICH5 platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The ICH5 glue chip is designed to integrate the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Features

- Dual, Strapping, Selectable Feature Sets
- Audio-Disable Circuit
- Mute Audio Circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK (PWRGD_3 V) signal generation
- Power Sequencing / BACKFEED_CUT
- Power Supply turn on circuitry
- RSMRST# generation
- Tri-state buffers for test
- Extra GP Logic Gates
- Power LED Drivers
- Flash FLUSH# / INIT# circuit

More information regarding this component is available from the following vendors:

Vendor	Contact Information	Part Number
Philips Semiconductors	http://www.semiconductors.philips.com	PCA9504A
Fujitsu Microelectronics	http://www.fujitsumicro.com/	MB87B302ABPD-G-ER

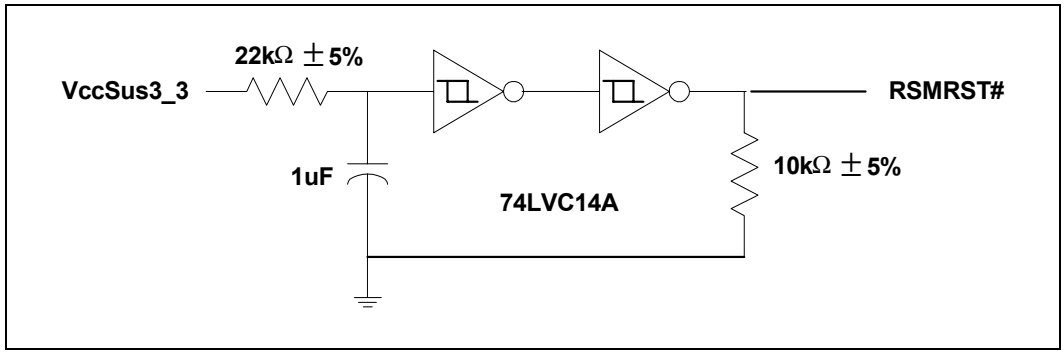
NOTE: These vendors/devices are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

13.4 Discrete Glue Logic

13.4.1 RSMRST# Generation

RSMRST# can be generated by causing an RC delay on the output of the VCCSUS3_3 well. The inverting Schmitt Triggers are used to resolve the slow edge rate caused by the RC delay.

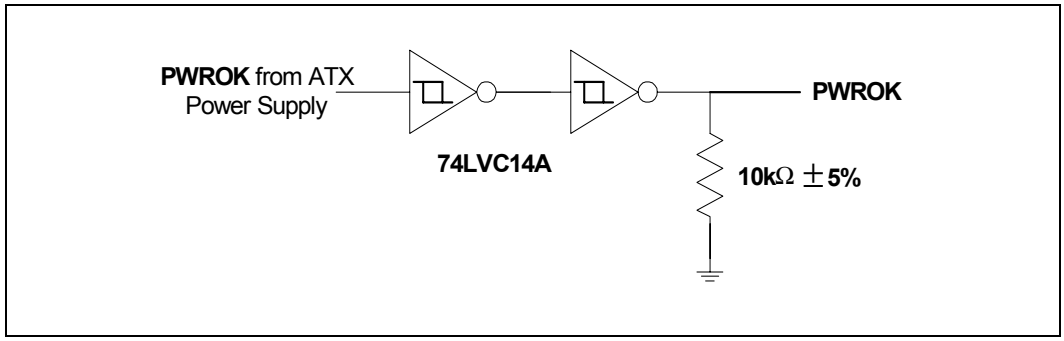
Figure 13-1. RSMRST# Generation from VCCSUS3_3



13.4.2 PWROK Generation

PWR_OK is generated by the ATX power supply. The ATX Power Supply asserts this signal a minimum of 100 ms after the core power wells are above the undervoltage thresholds listed in Section 3.2.1 of the *ATX/ATX12V Power Supply Design Guide*. The circuit in Figure 13-2 is used to ensure adequate rise and fall times (>40 mV/µs) on this signal. The 74LVC14A Inverting Schmitt Trigger or equivalent device is also used to avoid the need for translation circuitry (from the 5 V PWR_OK output of the power supply to the 3.3 V PWROK input to the ICH5) since the inputs/outputs of the device are 5 V tolerant.

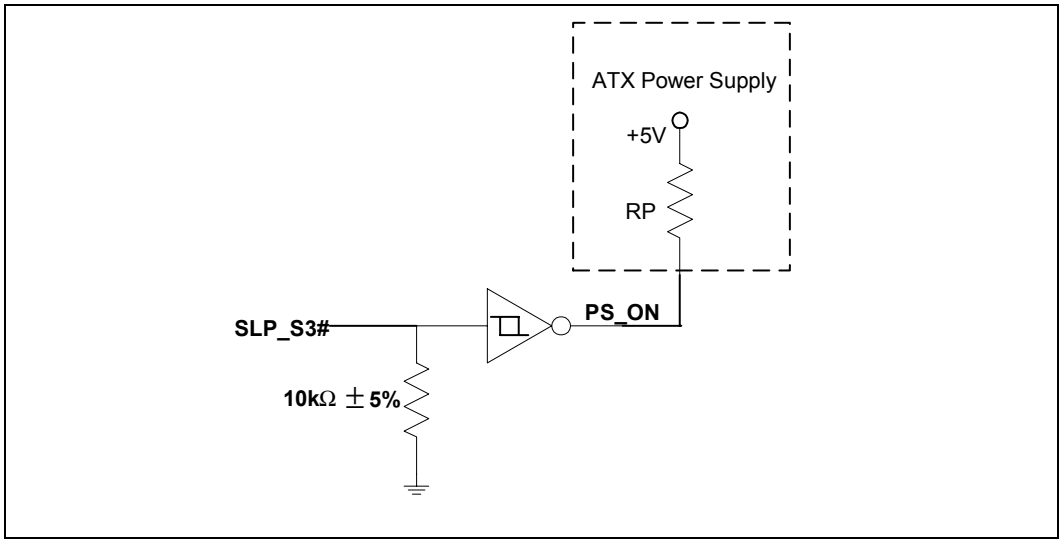
Figure 13-2. PWROK Generation from PWR_OK Output of ATX Supply



13.4.3 PS_ON Generation

The deassertion of the SLP_S3# signal is used to indicate to the power supply that the core power wells supplied by the power supply may be turned on. The circuit in Figure 13-3 is used to actively pull-down the PS_ON input signal to the power supply when SLP_S3# from the ICH5 becomes deasserted.

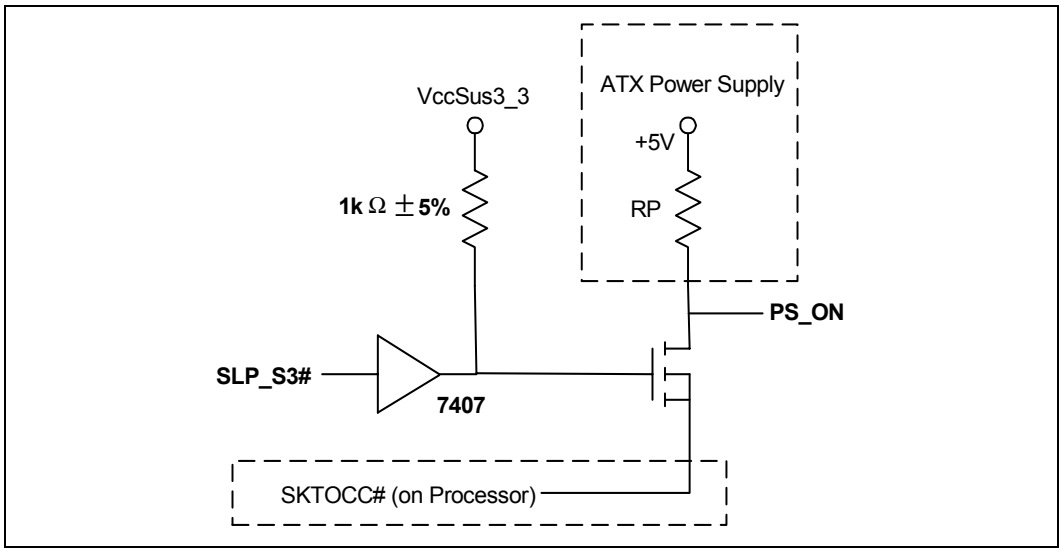
Figure 13-3. PS_ON Generation from SLP_S3#



NOTE: This circuit has not yet been validated.

The circuit in Figure 13-4 is used to actively pull down the PS_ON input signal to the power supply when SLP_S3# from the ICH5 becomes deasserted and the SKTOCC# pin is driven to ground. The SKTOCC# pin will be driven to ground by the processor when the processor is socketed in the system; otherwise, the SKTOCC# signal will be floating.

Figure 13-4. PS_ON Generation from SLP_S3# and SKTOCC#



NOTE: This circuit has not yet been validated.

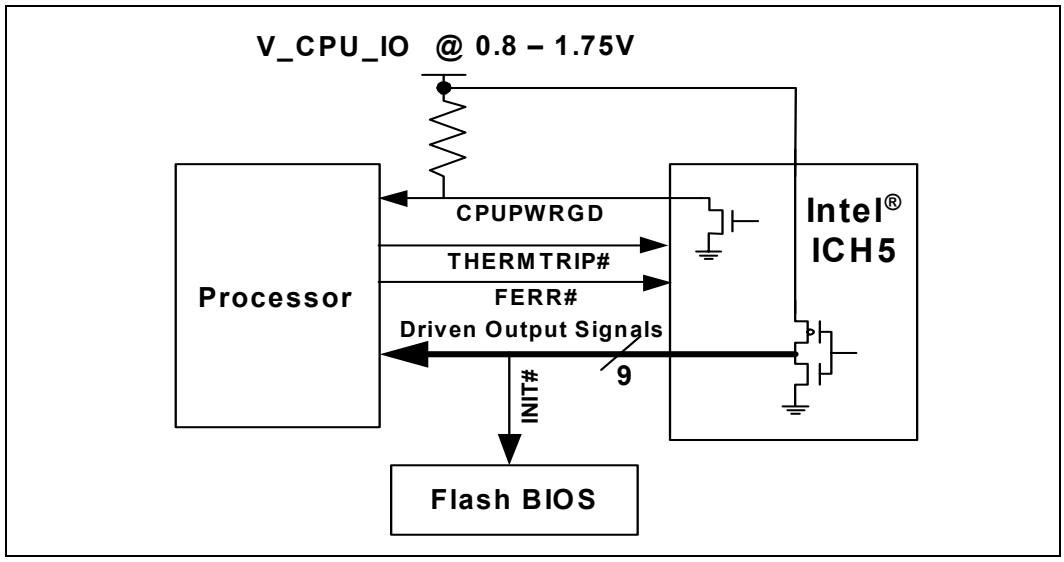
13.5 Suspend-to-RAM Sequencing

The system memory suspend voltage regulator is controlled by the LATCHED_BACKFEED_CUT signal. This signal should be generated using the SLP_S4# signal from the ICH5, rather than the SLP_S5# signal, even if the platform does not support the S4 Sleep State. The SLP_S4# logic in the ICH5 ensures that system memory will be properly initialized when returning from S4 and S5 states.

13.6 Processor CMOS Considerations

The ICH5 has been designed to work with low voltage processors that operate within the range of 0.8 V to 1.75 V. A voltage compatibility issue may arise when interfacing higher voltage processors (>1.75 V) with the ICH5. It is important to verify that the voltage requirements of all processor and ICH5 signals are compatible with one another as well as with the flash BIOS. Figure 13-5 shows a typical interface between the ICH5, processor, and flash BIOS.

Figure 13-5. Intel® ICH5 Processor CMOS Signals with Processor and Flash BIOS



13.6.1 Intel® ICH5 Outputs (A20M#, SMI#, IGNNE#, CPUPWRGD, STPCLK#, CPUSLP#, NMI, INTR, INIT#)

The V_CPU_IO signals are documented to only support 0.8 V to 1.75 V. The ICH5 processor CMOS output signal voltage swing depends on the voltage passed into these signals (V_CPU_IO:[2:0]) and voltages below 0.8 V are not supported by the ICH5's buffers.

Platforms using processors with On-Die Termination (ODT) on these processor CMOS signals must carefully comprehend the current requirements with respect to the ICH5 capabilities as defined in the datasheet. Platforms with ODT may likely need extra external buffer circuitry on these processor CMOS signals to boost the current capability.

13.7 Resistor Summary

Table 13-2. Intel® ICH5 Signal Pull-Up/Pull-Down Summary (Sheet 1 of 6)

Signal Name	Type	Power Well	Resistors	Design Guidelines
Hub Interface				
HI[11:0]	I/O	Core	Internal Termination	
HI_STBS	I/O	Core	Internal Termination	
HI_STBF	I/O	Core	Internal Termination	
HICOMP	I/O	Core	External Resistor (See Chapter 7.)	
HI_VSWING	I	Core	External Resistor (See Chapter 7)	See Chapter 7
HIREF	I	Core	External Resistor (See Chapter 7)	See Chapter 7
LAN Interface				
LAN_CLK	I	LAN	Internal Pull-Down (45 kΩ to 170 kΩ)	Can float if not used
LAN_RXD[2:0]	I	LAN	Internal Pull-Ups (7.5 kΩ to 16 kΩ)	Can float if not used
LAN_RSTSYNC	O	LAN	None	Can float if not used
LAN_TXD[2:0]	O	LAN	None	Can float if not used
LAN EEPROM Interface				
EE_SHCLK	O	LAN	None	Can float if not used
EE_DIN	I	LAN	Internal Pull-Up (15 kΩ to 35 kΩ)	Can float if not used
EE_DOUT	O	LAN	Strap Pin Internal Pull-Up (15 kΩ to 35 kΩ)	Can float if not used, placeholder for pull-down required
EE_CS	O	LAN	Strap Pin Internal Pull-Up (15 kΩ to 35 kΩ)	Can float if not used
PCI Interface				
AD[31:0]	I/O	Core	None	
C/BE[3:0]#	I/O	Core	None	
DEVSEL#	I/O	Core	External Pull-Up	8.2 kΩ pull-up to VCC3_3 or 2.7 kΩ to VCC5
FRAME#	I/O	Core	External Pull-Up	8.2 kΩ pull-up to VCC3_3 or 2.7 kΩ to VCC5
IRDY#	I/O	Core	External Pull-Up	8.2 kΩ pull-up to VCC3_3 or 2.7 kΩ to VCC5
TRDY#	I/O	Core	External Pull-Up	8.2 kΩ pull-up to VCC3_3 or 2.7 kΩ to VCC5
STOP#	I/O	Core	External Pull-Up	8.2 kΩ pull-up to VCC3_3 or 2.7 kΩ to VCC5
PAR	I/O	Core	None	
PERR#	I/O	Core	External Pull-Up	8.2 kΩ pull-up to VCC3_3 or 2.7 kΩ to VCC5

Table 13-2. Intel® ICH5 Signal Pull-Up/Pull-Down Summary (Sheet 2 of 6)

Signal Name	Type	Power Well	Resistors	Design Guidelines
REQ[0:3]# REQ[4]# /GPIO40 REQ[5]# / REQ[B]# / GPIO1	I	Core	External Pull-Ups	8.2 kΩ pull-ups to VCC3_3 or 2.7 kΩ to VCC5
GNT[0:3]# GNT4# / GPIO48 GNT5# / GNTB# / GPIO17	O	Core	None	
PCICLK	I	Core	None	
PCIRST#	O	Suspend	None	
PLOCK#	I/O	Core	External Pull-Up	8.2 kΩ pull-up to VCC3_3 or 2.7 kΩ to VCC5
SERR#	I/OD	Core	External Pull-Up	8.2 kΩ pull-up to VCC3_3 or 2.7 kΩ to VCC5
PME#	I/OD	Suspend	Internal Pull-Up (15 kΩ to 35 kΩ)	Can float if not used
REQ[A]# / GPIO[0]	I	Core	External Pull-Up	8.2 kΩ pull-up to VCC3_3 or 2.7 kΩ to VCC5
GNTA# / GPIO16	O	Core	Strap pin Internal Pull-Up (15 kΩ to 35 kΩ)	Strap Function: TOP SWAP OVERRIDE See ICH5 datasheet
SATA Interface				
SATA0TXP SATA0TXN	O	Core	None	
SATA0RXP SATA0RXN	I	Core	None	
SATA1TXP SATA1TXN	O	Core	None	
SATA1RXP SATA1RXN	I	Core	None	
SATARBIAS SATARBIAS#	I	Core	External Pull-Down	24.9 Ω ± 1%
SATALED#/GPIO33	O			
LPC Interface				
LAD[3:0]	I/O	Core	Internal Pull-Up (15 kΩ to 35 kΩ)	
LFRAME#	O	Core	None	
LDRQ0#, LDRQ1# / GPIO41	I	Core	Internal Pull-Up (15 kΩ to 35 kΩ)	

Table 13-2. Intel® ICH5 Signal Pull-Up/Pull-Down Summary (Sheet 3 of 6)

Signal Name	Type	Power Well	Resistors	Design Guidelines
USB Interface				
USBP[7:0]P/N	I/O	Suspend	Internal Pull-Downs (14.25 kΩ to 24.8 kΩ)	
OC[3:0]# OC4# / GPIO9 OC5#/ GPIO10 OC6#/ GPIO14 OC7#/ GPIO15	I	Suspend	None	If not used, use 10 kΩ pull-up to VCCSUS3_3
USBRBIAS USBRBIAS#	I	Suspend	External Pull-Down	22.6 Ω ± 1%
IDE Interface				
PDCS1#, SDCS1#	O	Core	Internal Series Resistors (21 Ω to 75 Ω)	
PDCS3#, SDCS3#	O	Core	Internal Series Resistors (21 Ω to 75 Ω)	
PDA[2:0], SDA[2:0]	O	Core	Internal Series Resistors (21 Ω to 75 Ω)	
PDD[15:0], SDD[15:0]	I/O	Core	Internal Pull-Downs (5.7 kΩ to 28.3 kΩ) on PDD[7] and SDD[7] Internal Series resistors (21 Ω to 75 Ω)	
PDDREQ, SDDREQ	I	Core	Internal Pull-downs (5.7 kΩ to 28.3 kΩ) Internal Series Resistors (21 Ω to 75 Ω)	
PDDACK#, SDDACK#	O	Core	Internal Series Resistors (21 Ω to 75Ω)	
PDIOW#/ (PDSTOP) SDIOW# / (SDSTOP)	O	Core	Internal Series Resistors (21 Ω to 75 Ω)	
PIORDY / (PDRSTB / PWDMARDY#) SIORDY / (SDRSTB / SWDMARDY#)	I	Core	Internal Series Resistors (21 Ω to 75 Ω) Use External Pull-Ups	4.7 kΩ pull-up to VCC3_3
IRQ[14:15]	I	Core	Internal Series Resistors 21 Ω to 75 Ω) Use External Pull-Ups	8.2 kΩ – 10 kΩ pull-ups to VCC3_3
PDIOR#/ (PDWSTB/ PRDMARDY#) SDIOR#/ (SDWSTB/ SRDMARDY#)	O	Core	Internal Series Resistors (21 Ω to 75 Ω)	

Table 13-2. Intel® ICH5 Signal Pull-Up/Pull-Down Summary (Sheet 4 of 6)

Signal Name	Type	Power Well	Resistors	Design Guidelines
Interrupt Pins				
SERIRQ	I/O	Core	External Pull-Up	8.2 kΩ pull-up to VCC3_3
PIRQ[A:D]#	I/OD	Core	External Pull-Ups	8.2 kΩ pull-ups to VCC3_3 or 2.7 kΩ to VCC5
PIRQ[E:H]# / GPIO[2:5]	I/OD	Core	External Pull-Ups When Used as PIRQ	8.2 kΩ pull-up to VCC3_3 or 2.7 kΩ to VCC5
AC '97 Interface				
AC_RST#	O	Suspend	Internal Pull-Down (9 kΩ to 50 kΩ)	
AC_SYNC	O	Core	Strap Pin Internal Pull-Down during reset (9 kΩ to 50 kΩ)	
AC_BIT_CLK	I	Core	Internal Pull-Down (10 kΩ to 40 kΩ)	
AC_SDATA_OUT	O	Core	Strap Pin Internal Pull-Down during Reset (9 kΩ to 50 kΩ)	Strap Mode: SAFE MODE See ICH5 datasheet
AC_SDATA_IN[2:0]	I	Suspend	Internal Pull-Down (9 kΩ to 50 kΩ)	
Power Management Pins				
THRM#	I	Core	None	
THRMTRIP#	I	CPU_IO		
SLP_S3# SLP_S4# SLP_S5#	O	Suspend	None	
SYS_RESET#	I	Suspend		
PWROK	I	RTC	None	
PWRBTN#	I	Suspend	Internal Pull-Up (15 kΩ to 35 kΩ)	
RI#	I	Suspend	None	
RSMRST#	I	RTC	None	
SUS_STAT#	O	Suspend	None	
SUSCLK	O	Suspend	None	
VRMPWRGD	I	Core	None	
LAN_RST#	I	Suspend	None	
TP0	I	Suspend	External Pull-Up	10 kΩ pull-up to VCCSUS3_3

Table 13-2. Intel® ICH5 Signal Pull-Up/Pull-Down Summary (Sheet 5 of 6)

Signal Name	Type	Power Well	Resistors	Design Guidelines
Processor Interface Pins				
A20M#	O	Processor I/O	Integrated Pull-Up to V_CPU_IO	No external pull-up required
CPU_SLP#	O	Processor I/O	None	No external pull-up required
FERR#	I	Processor I/O	External Pull-Up	Weak pull-up required (value processor dependent)
IGNNE#	O	Processor I/O	Integrated Pull-Up to V_CPU_IO	No external pull-up required
INIT#	O	Processor I/O	Integrated Pull-Up to V_CPU_IO	No external pull-up required§
INTR	O	Processor I/O	Integrated Pull-Up to V_CPU_IO	No external pull-up required
NMI	O	Processor I/O	None	No external pull-up required
SMI#	O	Processor I/O	None	No external pull-up required
STPCLK#	O	Processor I/O	Integrated Pull-Up to V_CPU_IO	No external pull-up required
RCIN#	I	Core	External Pull-Up	10 kΩ pull-up to VCC3_3 (pull-up required if hooked to external open-collector keyboard controller)
A20GATE	I	Core	External Pull-Up	10 kΩ pull-up to VCC3_3 (pull-up required if hooked to external open-collector keyboard controller)
CPUPWRGD	OD	Processor I/O	External Pull-Up	Weak pull-up required (value processor dependent)
SMBus and System Management Pins				
SMBDATA	I/OD	Suspend	External Pull-Up	Typ. 8.2 kΩ; rail depends upon platform implementation (see DG)
SMBCLK	I/OD	Suspend	External Pull-Up	Typ. 8.2 kΩ; rail depends upon platform implementation (see DG)
SMBALERT# / GPIO11	I	Suspend	External Pull-Up (for SMBALERT#)	10 kΩ pull-up to VCCSUS3_3
LINKALERT#	I/OD	Suspend	Strap Pin External Pull-Up	10 kΩ pull-up to VCCSUS3_3
SMLINK[1:0]	I/OD	Suspend	External Pull-Up	10 kΩ pull-up to VCCSUS3_3
INTRUDER#	I	RTC	External Pull-Up	1 MΩ pull-up to VccRTC (VBAT)

Table 13-2. Intel® ICH5 Signal Pull-Up/Pull-Down Summary (Sheet 6 of 6)

Signal Name	Type	Power Well	Resistors	Design Guidelines
Real Time Clock Pins				
RTCX1	Special	RTC	None	
RTCX2	Special	RTC	None	
Miscellaneous Pins and GPIO				
CLK14	I	Core	None	
CLK48	I	Core	None	
CLK66	I	Core	None	
CLK100P CLK100N	I	Core	None	
INTVRMEN	I	RTC	External Pull-Up	300–400kΩ pull-up to VccRTC (VBAT)
SPKR	O	Core	Strap Pin Internal Pull-Down (9 kΩ to 50 kΩ)	Strap Function: NO REBOOT (See ICH5 datasheet) Pull-up to VCC3_3. The value is dependent on platform specifics
RTCRST#	I	RTC	None	External RTC circuit
GPIO7	I	Core	None	Pull-up needed
GPIO8	I	Suspend	None	Any pull-up must use VCCSUS3_3
GPIO[13:12]	I	Suspend	None	Any pull-up must use VCCSUS3_3
GPIO[21:18]	O	Core	None	
GPIO22	OD	Core	None	
GPIO23	O	Core	None	
GPIO[25:24]	I/O	Suspend	None	Any pull-up must use VCCSUS3_3
GPIO[28:27]	I/O	Suspend	None	Any pull-up must use VCCSUS3_3
GPIO[34:32]	I/O	Core	None	Any pull-up must use VCC3_3

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Flash BIOS Guidelines 14

The following provides general guidelines for compatibility and design recommendations for supporting the flash BIOS device. The majority of the changes will be incorporated in the BIOS.

14.1 Flash BIOS Vendors

The following vendors manufacture firmware hubs that conform to the *Intel® Flash BIOS Specification*. Contact the vendor directly for information on packaging and density.

SST: http://www.ssti.com/

STM: http://us.st.com/stonline/index.shtml

ATMEL: http://www.atmel.com

14.2 Flash BIOS Decoupling

A 0.1 µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple high frequency noise that may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the VCC supply pins.

14.3 In Circuit Flash BIOS Programming

All cycles destined for the flash BIOS will appear on PCI. The ICH5 hub interface-to-PCI Bridge will put all processor boot cycles out on PCI (before sending them out on the flash BIOS interface). If the ICH5 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. To boot from a PCI card it is necessary to keep the ICH5 in subtractive decode mode. If a PCI boot card is inserted and the ICH5 is programmed for positive decode, there will be two devices positively decoding the same cycle.

14.4 Flash BIOS INIT# Voltage Compatibility

The flash BIOS INIT# signal trip points need to be considered because they are **not** consistent among different flash BIOS manufacturers. The INIT# signal is active low. Therefore, the inactive state of the ICH5 INIT# signal needs to be at a value slightly higher than the V_{IH} min flash BIOS INIT# pin specification. The ICH5 inactive state of this signal is typically governed by the formula V_CPU_IOmin – noise margin. Therefore, if the V_CPU_IOmin of the processor is 1.6 V, the noise margin is 200 mV and the VIH min specification of the flash BIOS INIT# input signal is 1.35 V, there would be no compatibility issue because 1.6 V – 0.2 V = 1.40 V, which is greater than

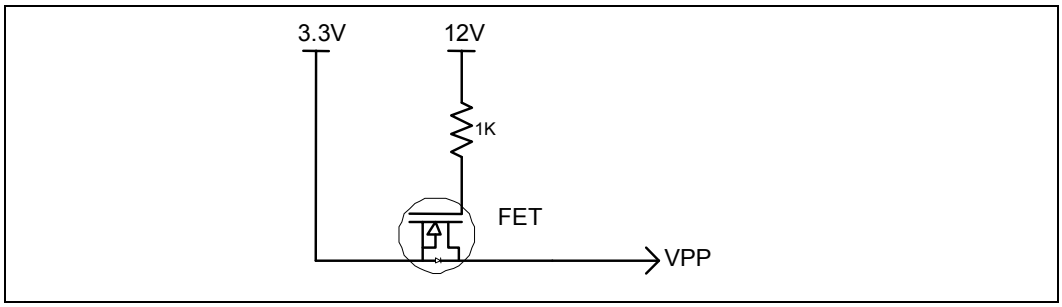
the 1.35 V minimum of the flash BIOS. If the VIH min of the flash BIOS was 1.45 V, then there would be an incompatibility and logic translation would need to be used. Note that these examples do not take into account actual noise that may be encountered on INIT#. Care must be taken to ensure that the V_{IH} minimum specification is met with ample noise margin. In applications where it is necessary to use translation logic, refer to Section 5.1.6.5

14.5 Flash BIOS VPP Design Guidelines

The VPP pin on the flash BIOS is used for programming the flash cells. The flash BIOS supports VPP of 3.3 V or 12 V. If VPP is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the flash BIOS only supports 12 V VPP for 80 hours (3.3 V on VPP does not affect the life of the device). The 12 V VPP would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The VPP pin **must** be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the flash BIOS during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the VPP pin. The following circuit will allow testers to put 12 V on the VPP pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 14-1. Flash BIOS VPP Circuitry



Power Distribution Guidelines 15

This chapter addresses power delivery recommendation for 848P chipset reference designs. These guidelines allow support for both the Pentium 4 processor on 90 nm process and the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process processors.

15.1 Terminology and Definitions

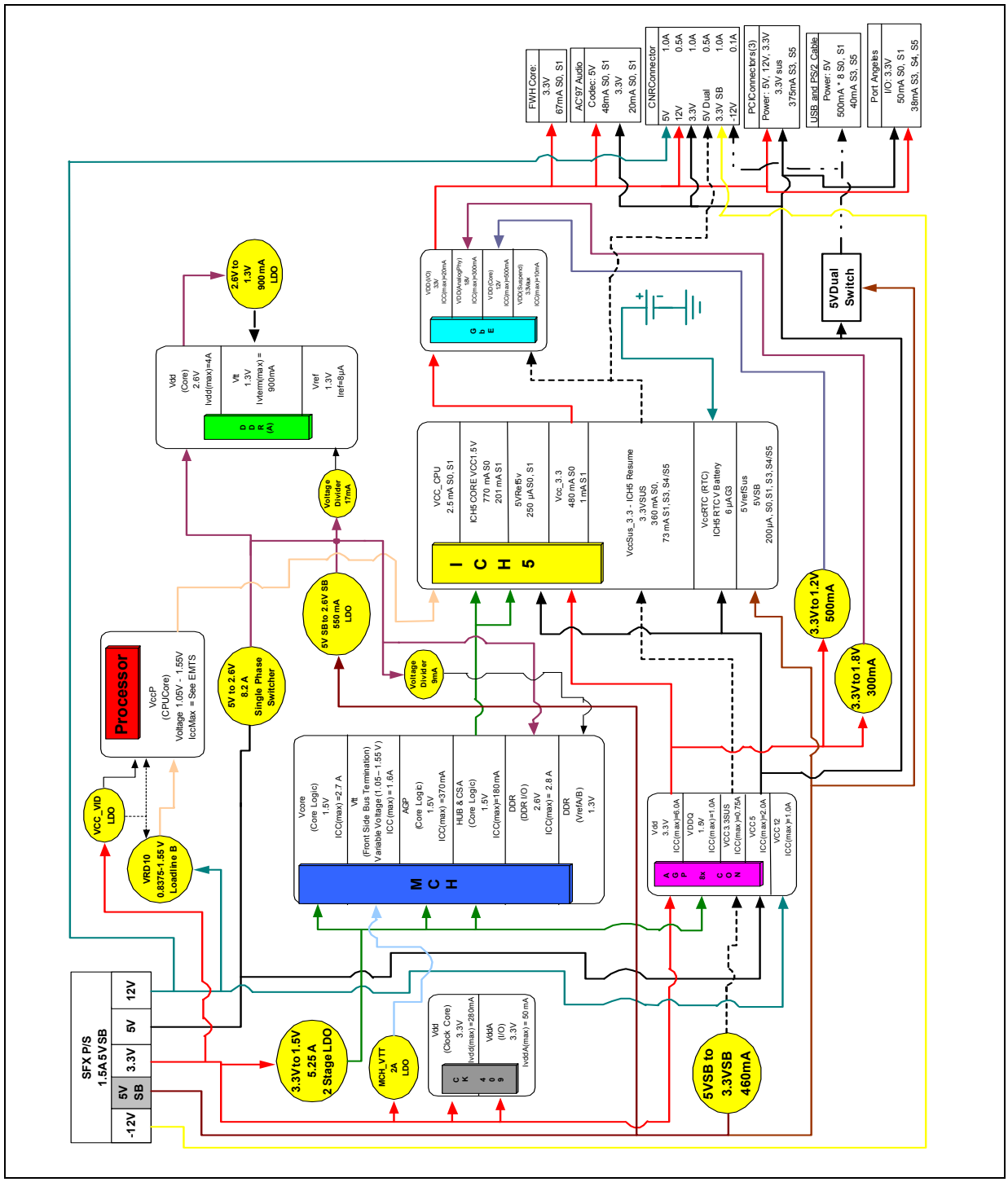
Term	Description
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered. This state is used in the Customer Reference Board to satisfy the S3 ACPI power management state.
Full-power	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state and the S1 (processor stop-grant state) state.
Suspend Operation	During suspend operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3) and Soft-Off (S5).
Power Rails	An ATX power supply has six power rails: +12 V, –12 V, +5 V, -5 V, +3.3 V, and +5 V SB. In addition to these power rails coming off the power supply, several other power rails are created by voltage regulators on the 848P chipset.
Core Power	A power rail that is only on during full-power operation. These power rails are on when the PS_ON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX power supply are: ±5 V, ±12 V and +3.3 V.
Standby Power Rail	A power rail that is on during suspend operation (these rails are also on during full power operation) is a standby power rail. These rails are on at all times as soon as the power supply is plugged into AC power. The only standby power rail that is distributed directly from the ATX power supply is 5 V SB. The other standby rails on the motherboard are created by voltage regulators.
Derived Power	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, +2.6 V can be derived from a +5 V power rail using a voltage regulator.
Dual Power Rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from standby supply during suspend operation and derived from a core supply during full-power operation.
VRM and VRD	VRM stands for Voltage Regulator Module while VRD stands for Voltage Regulator Down.

15.2 Customer Reference Board Power Delivery

Figure 15-1 shows the power delivery architecture for an 848P chipset solution. This power delivery architecture supports the “Instantly Available PC Design Guidelines” via the suspend-to-RAM (STR) state.

During STR, only the necessary devices are powered. These devices include main memory, the ICH5 resume well, PCI wake devices (via 3.3 VAUX), and USB (USB can be powered only if sufficient standby power is available). To insure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device’s power requirements, both in suspend and in full power modes. The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory, the PCI 3.3 VAUX (and possibly other devices in the system), it is necessary to create **a dual** power rail.

Figure 15-1. Customer Reference Board Power Delivery Map



NOTE: Always refer to the component's specification document for the latest ICCs.

15.2.1 VCC_CPU (Processor Core and VTT)

The VCC_CPU power plane is used to power the processor core and VTT. The processor's voltage regulator must be compatible with a VRD 10.0 design. Refer to the *Voltage Regulator-Down (VRD) 10.0 Design Guidelines* for more information. This is required for all designs.

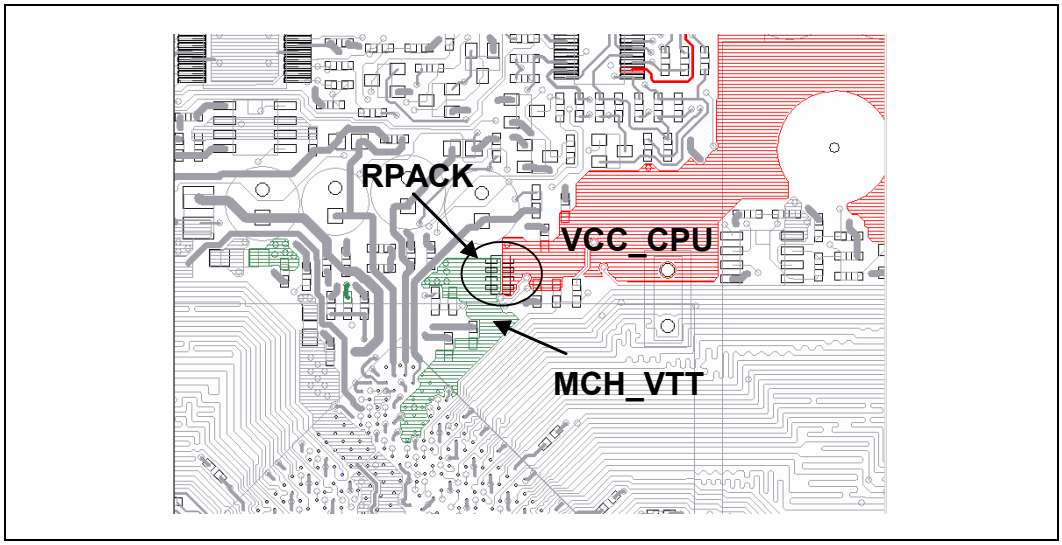
15.2.2 MCH_VTT

The MCH_VTT regulator is required for use with the Pentium 4 processor on 90 nm process and recommended for Pentium 4 processor with 512-KB L2 cache on 0.13 micron process platforms. The MCH_VTT power plane powers the MCH's FSB interface. It is important that the MCH_VTT plane be separate from the processor's core and VTT plane. When a Pentium 4 processor on 90 nm process is inserted into the platform, the output of the MCH_VTT regulator should be set to 1.225 V. When a Pentium 4 processor with 512-KB L2 Cache on 0.13 micron process is inserted into the platform, the output of the MCH_VTT regulator should be set to 1.45 V. This regulator must be able to source 2 A and sink 600 mA in normal operation.

The power up/down timing requirements for the MCH VTT is that it must come up after or at the same time as the processor core voltage and power down before or at the same time as the processor core. The BOOTSELECT pin from the processor socket will be used to switch the output voltage on the regulator. At a minimum, the regulator should have tolerance of ± 7%, but ± 5% is preferred.

For cost reduced Pentium 4 processor with 512-KB L2 Cache on 0.13 micron process only platforms, the MCH_VTT regulator and switch (discussed in Section 5.1.6.10) should be left unstuffed. In addition, a resistor package (RPACK) should be stuffed as outlined in Figure 15-2 to connect the two separate planes: MCH_VTT and VCC_CPU. And finally, the BOOTSELECT pin from the processor socket must be tied low.

Figure 15-2. RPACK for Combining VCC_CPU and MCH_VTT



15.2.3 VCCVID (Processor VID)

VCCVID is a 1.2 V power plane and is used to power pins AF4 and AF3 on the processor. It is derived from 3.3 V and should be able to source 150 mA of current. This regulator is required for all designs.

15.2.4 2.6 V Dual (DDR Core)

The 2.6 V dual power plane is used to provide power to the DDR DRAM core, the MCH DDR I/O ring, and reference voltage to the 1.3 V linear regulator. The 2.6 V power plane is created using a switch between a switching regulator and a linear stand-by regulator. The switching regulator receives its input directly from the 5 V power rail of the power supply while the linear regulator receives its input from 5 V SB. This regulator is required in all designs.

15.2.5 1.3 V (DDR Termination)

The 1.3 V voltage regulator is for the DDR termination voltage (VTERM). A linear regulator divides the 2.6 V power rail by 2 to drive the 1.3 V DDR termination rail. VTERM is defined as: VTERM_min = SMVREF – 40 mV and VTERM_max = SMVREF + 40 mV. By deriving the VTERM voltage from the 2.6 V plane, this provides some common mode noise rejection between the DDR termination and I/O voltages. This is required for all designs.

In S3, the memory channel termination voltage, VTT, should be turned off. If VTT is not turned off, the VTT regulator must be able to support 200 mA for the MCH.

15.2.6 1.5 V (MCH Core, HI, AGP, Intel® ICH5 HI, and AGP Connector)

The 1.5 V power plane is created using a dual linear regulator sourcing from the 3.3 V power rail. The 1.5 V plane powers the ICH5 core logic and HI, the MCH core, HI, CSA, AGP, and the AGP connector. Sequencing on this rail should ensure that the 1.5 V power plane is shut off during S3. This voltage rail requires approximately 6.75 A maximum current. This regulator is required in all designs.

15.2.7 5 V Dual

This rail is powered from the 5 V core ATX supply during full-power operation and from 5 V SB during Suspend to Ram (STR). There is a resistive drop through the 5 V dual switch that must be considered. Therefore, **no components** should be connected directly to the 5 V dual plane. On the Customer Reference Board, voltage regulators are the only devices on the 5 V dual rail.

Note: The voltage on the 5 V dual plane is not 5 V.

Note: This switch is not required in an ICH5 chipset based system that does not support STR.

15.2.8 5 V SB (Standby)

The 5 V SB power plane comes directly off the 5 V SB power rail from the ATX power supply and has two functions: to provide power to resume functions via a 3.3 V SB regulator in I/O devices off of the ICH5 and to provide 2.6 V power to the memory devices during the S3 state. The ICH5 requires 3.3 V SB only due to the integrated 1.5 V SB regulator. It is recommended that the ATX power supply be capable of handling 2 A of standby current.

15.2.9 3.3 V SB (Standby)

The 3.3 V SB power plane is the output of a 5 V SB-to-3.3 V SB voltage regulator. The 3.3 V SB plane powers the resume well of the ICH5 and the PCI 3.3 VAUX suspend power pins. The 3.3 VAUX requirements state that during suspend, the system must deliver 375 mA to each wake-enabled card and 20 mA to each non-wake enabled card. During full-power operation, the system must be able to supply 375 mA to **each** card. Therefore, the total current requirement is:

- Full-power Operation: 375 mA * (number of PCI slots)
- Suspend Operation: 375 mA + 20 mA* (number of PCI slots –1)

In addition to the PCI 3.3 VAUX, the ICH5 suspend well power requirements must be considered. This regulator is required for all designs.

The integrated 1.5 V standby regulator should be used to power the resume well of the ICH5. Connect the INTVRMEN signal to VCCRTC to enable the integrated voltage regulator. The VCCSUS1_5 pins are grouped into three sets of signals: VCCSUS1_5_A, VCCSUS1_5_B, and VCCSUS1_5_C. Each group needs to be independently connected to its corresponding decoupling capacitor for optimum noise isolation. Only one decoupling capacitor is needed per VCCSUS1_5 signal group.

Note: Do not connect the three sets of VCCSUS1_5 signal groups on the ICH5 together.

15.2.10 2.6 V SB (Standby)

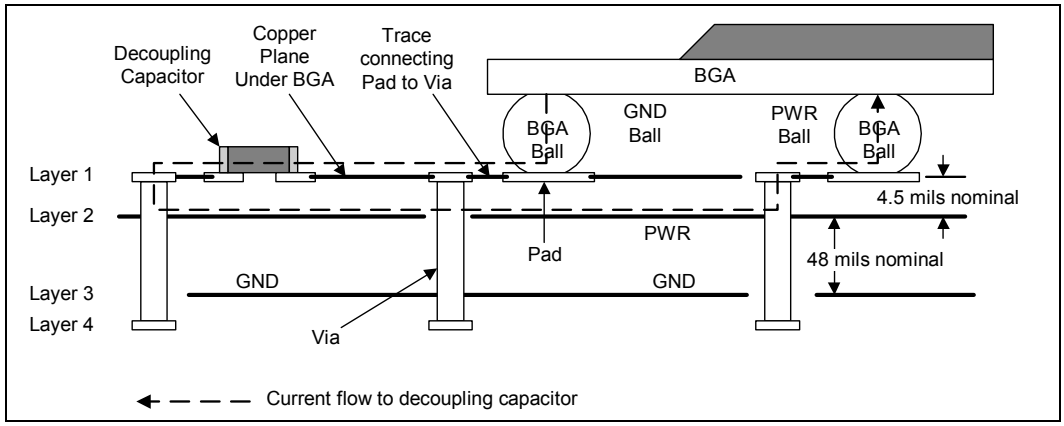
The 2.6 V SB power plane is the output of the 5 V SB-to-2.6 V SB voltage regulator. The power plane is used for the DDR DIMMs and MCH during the S3 suspend state. The suspend voltage regulator for system memory is controlled by the LATCHED_BACKFEED_CUT signal. This signal should be generated using the SLP_S4# signal from the ICH5, rather than the SLP_S5# signal, even if the platform does not support the S4 Sleep State. The SLP_S4# logic in the ICH5 ensures that system memory will be properly initialized when returning from S4 and S5 states (note that the LATCHED_BACKFEED_CUT signal also derived from the SLP_S3# and PS_PWRGD signals, so as not to cause potential confusion). This regulator is required for any design (see Section 15.3.4.3).

15.3 Component Power Delivery Guidelines

Large current swings cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. The capacitors should be placed as close to the package as possible and rotated such that they set over power planes. This orientation minimizes the loop inductance (see Figure 15-3). The basic theory for minimizing loop inductance is to consider which voltage is

on layer two (power or ground) and spin the decoupling cap with the opposite voltage towards the BGA (Ball Grid Array). This greatly minimizes the total loop inductance. It is recommended that, for prototype board designs, the designer include pads for extra power plane decoupling capacitors.

Figure 15-3. Minimized Loop Inductance Example



Note: Do not use this solution for VccSus1_5 signal group decoupling.

15.3.1 Processor Power Distribution Guidelines

15.3.1.1 Processor Power Requirements

Intel recommends using a *Voltage Regulator-Down (VRD) 10.0 Design Guidelines* -compliant regulator for the processor system board design. The system board designer should properly place high frequency and bulk-decoupling capacitors as needed between the voltage regulator and processor to ensure the voltage fluctuations remain within the processor electrical, mechanical, and thermal specifications (see processor datasheet). See Table 15-1 for recommendations on the amount of decoupling needed.

Specifications for the processor voltage are contained in the processor datasheet. These specifications are for the processor die. For guidance on correlating the die specifications to socket level measurements, refer to the *Voltage Regulator-Down (VRD) 10.0 Design Guidelines.*

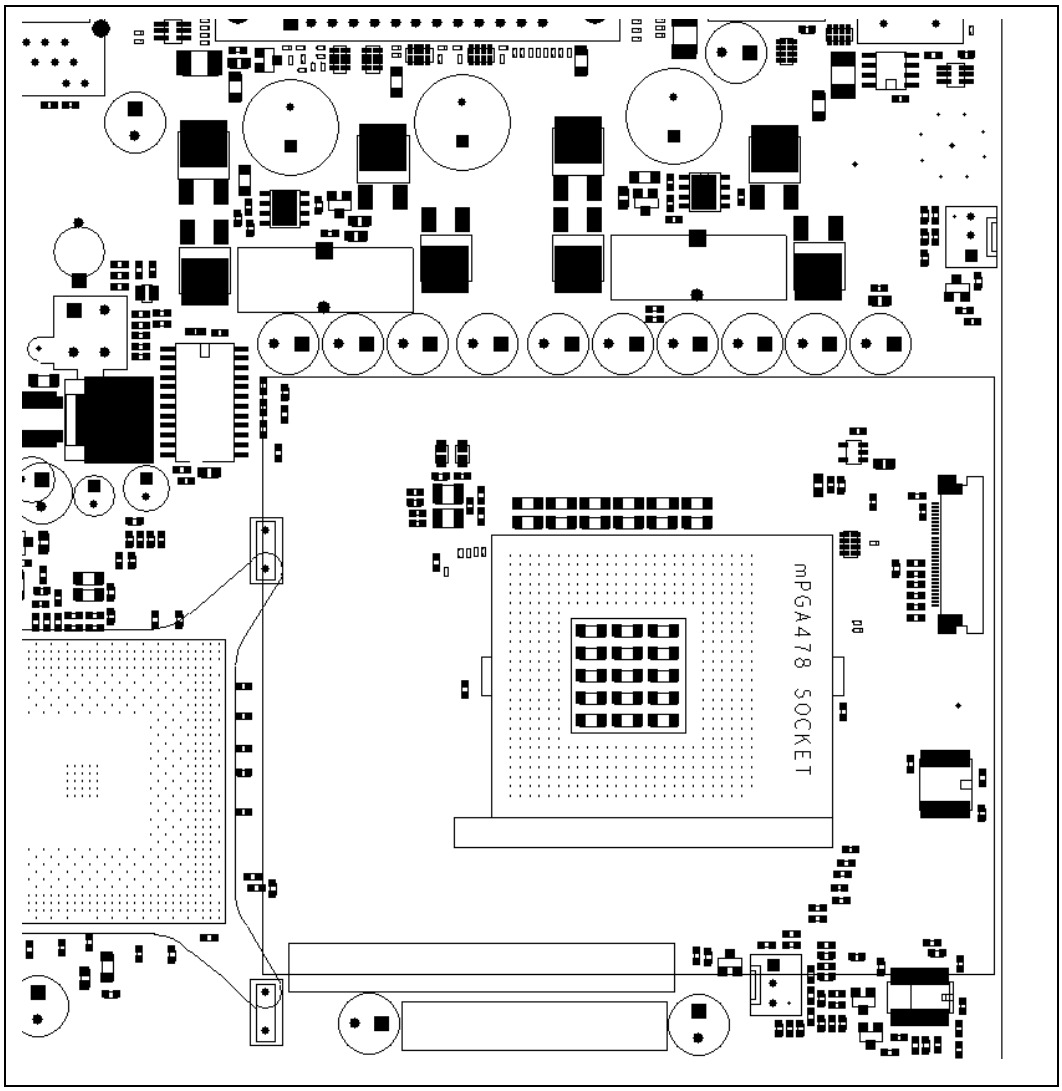
The voltage tolerance of the load lines contained in the documents mentioned above help the system designer to achieve a flexible motherboard design solution for all different frequencies of the processor. Failure to meet the load line requirements when modeling the system power delivery may result in a system that is not upgradeable.

The processor requires local regulation due to its higher current requirements, and to maintain power supply tolerance. For example, an on-board DC-to-DC converter converts a higher DC voltage to a lower DC voltage using a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses (I x R). More importantly however, an on-board regulator regulates the voltage locally, which minimizes DC line losses by reducing motherboard resistance on the processor voltage. Figure 15-4 shows an example of the placement of the local voltage regulation circuitry.

Note: In this section, North and South are used to describe a specific side of the socket based on the placement of the customer reference board shown in Figure 15-4. North refers to the side of the

processor closest to the back panel and South refers to the side of the processor closest to the system memory.

Figure 15-4. VR Component Placement



15.3.1.2 Decoupling Requirements

For the processor voltage regulatory circuitry to meet the transient specifications of the processor, proper bulk and high frequency decoupling is required. The decoupling requirements for the processor power delivery in this case are shown in Figure 15-1.

Table 15-1. Decoupling Requirements

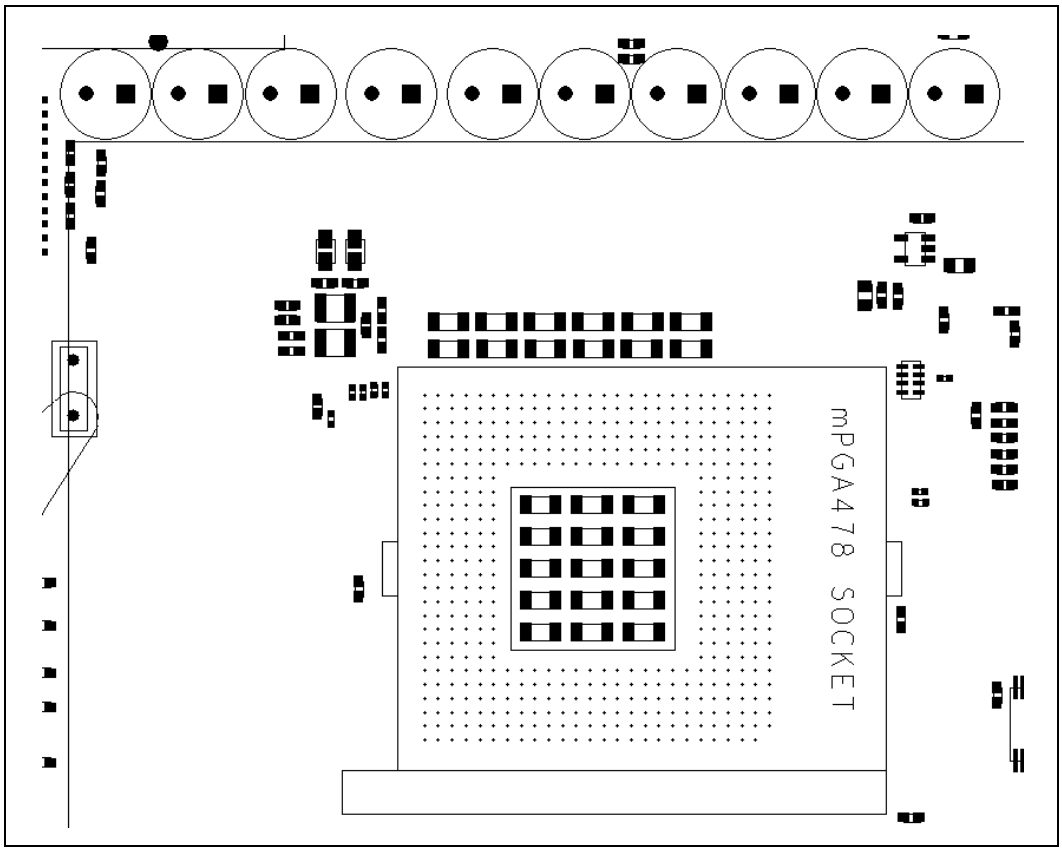
Capacitance	ESR (each)	ESL (each)	Filter	Notes
(10) Aluminum Polymer 560µF	5 mΩ	4 nH	Output	1
(24) 1206 pkg 22 µF X5R	3.5 mΩ	1.4 nH	Output	1,2
(4) Al Electrolytic 1200 µF16V 2.1A Ripple	22 mΩ	30 nH	Input	1
(4) 1206 pkg 4.7 µF	6 mΩ	1.1 nH	Input	1

NOTES:
1. The ESR, ESL, and ripple current values in this table are based on the values used in power delivery simulations used by Intel and they are not vendor specifications.
2. The decoupling should be placed as close as possible to the processor power pins. Table 15-1 details the recommended values and Figure 15-5 illustrates the recommended placement. The placement drawings shows sites for 10 AL Polymer capacitors and 24, 1206 package, 22 µF capacitors. The sites are populated as shown in Table 15-2. The voltage regulator designer should ensure that an adequate amount of decoupling is present such that the circuit meets the processor specifications.

Table 15-2. Decoupling Location

Type	Number	Location
560 µF Aluminum Polymer	10	North side of processor, as close as possible to the keep-out area for the retention mechanism.
22 µF	12	Inside the processor socket cavity; all sites stuffed.
22 µF	12	North of processor socket; four sites stuffed.

Figure 15-5. Decoupling Placement



15.3.1.3 Layout

VCC_CPU shapes on both the top and bottom layers should be maximized, within the constraints of the FSB and PLL routing and placement requirements. The copper plane areas on VCC_CPU (and also GND) directly impact the motherboard parasitics for processor power delivery, which in turn impact the amount of bulk decoupling required to meet the Socket Load Line specification. Therefore, the most cost-effective design practice is to maximize VCC_CPU shapes in the processor area on both top and bottom layers. Figure 15-6 through Figure 15-10 show examples of how to use shapes to deliver power to the processor.

Figure 15-6. Top Layer Power Delivery Shape (VCC_CPU)

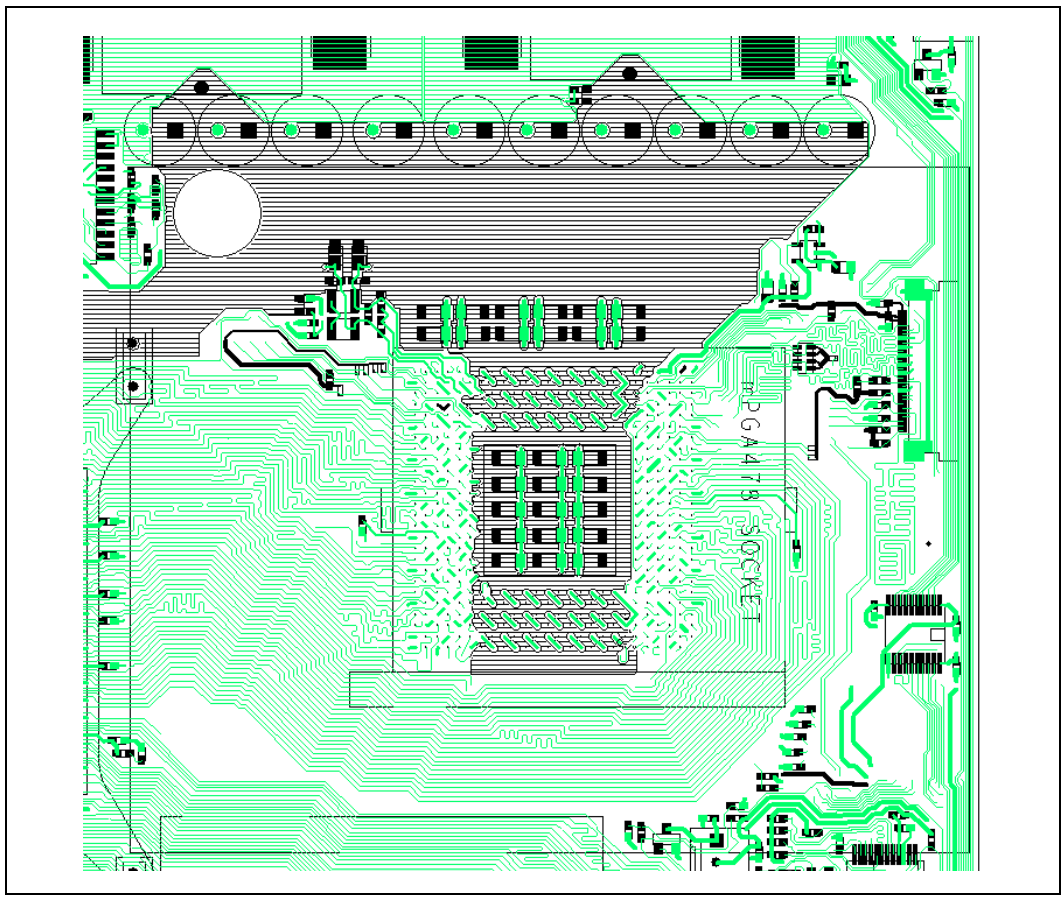


Figure 15-7. Layer 2 Power Delivery Shape (VSS)

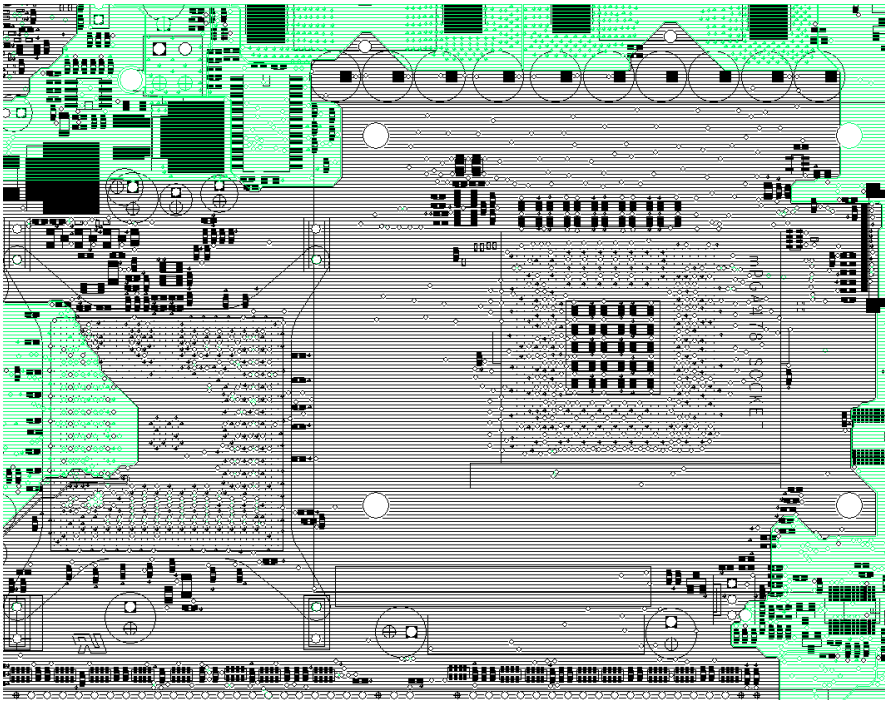
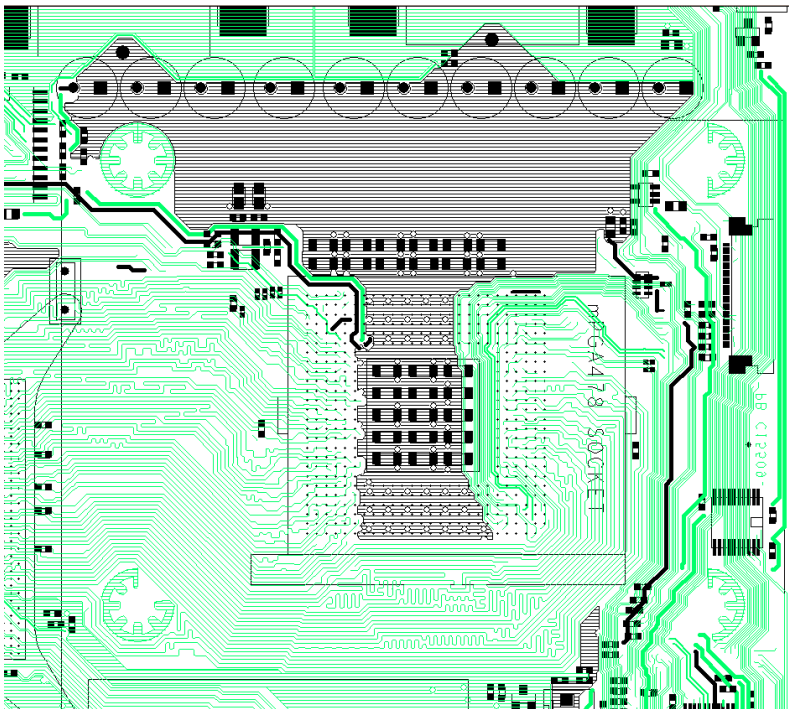
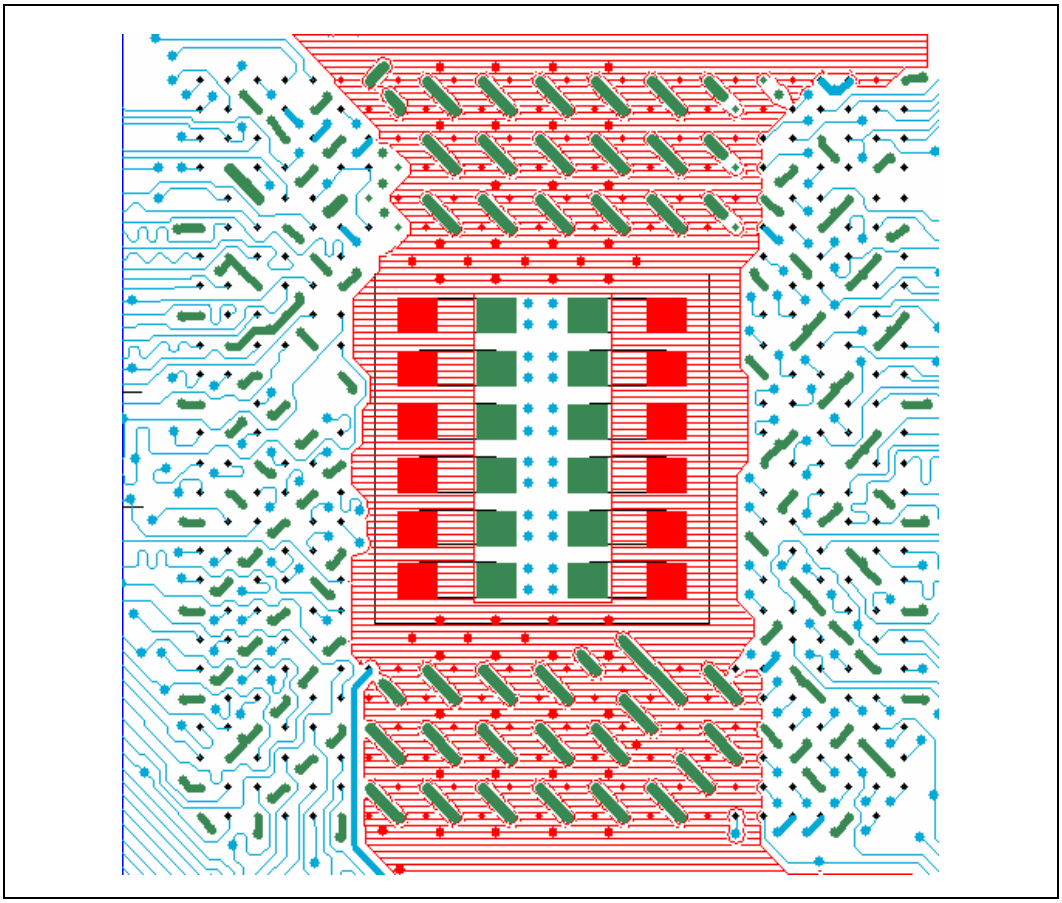


Figure 15-8. Bottom Layer Power Delivery Shape (VCC_CPU)



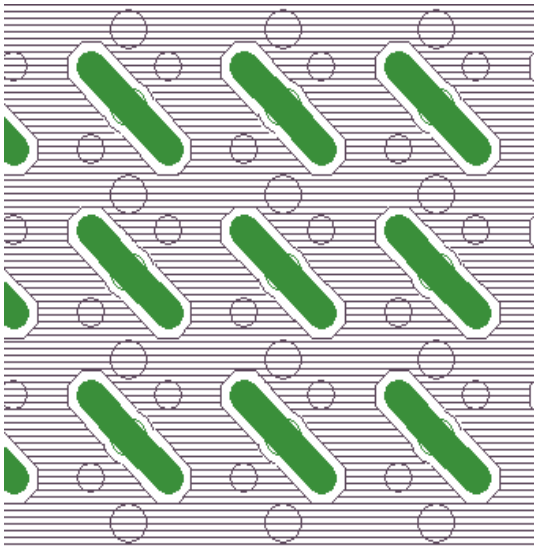
The 22 µF 1206 capacitors inside of the socket cavity should be oriented such that the current flow through the capacitor field is maximized. This can be accomplished by orientating the capacitors in an east/west direction with the grounds on the inside. This can be seen in Figure 15-9.

Figure 15-9. Capacitor Orientation



The processor socket has 478 pins with 50-mil pitch. When routing the signals, power and ground pins will require creation of many vias. These vias cut up the power and ground planes beneath the processor resulting in increased inductance in of these planes. To provide the best path through the via field, it is recommended that the vias are shared for every two processor ground pins and every two processor power pins. Figure 15-10 illustrates this via sharing.

Figure 15-10. Shared Ground and Power Vias

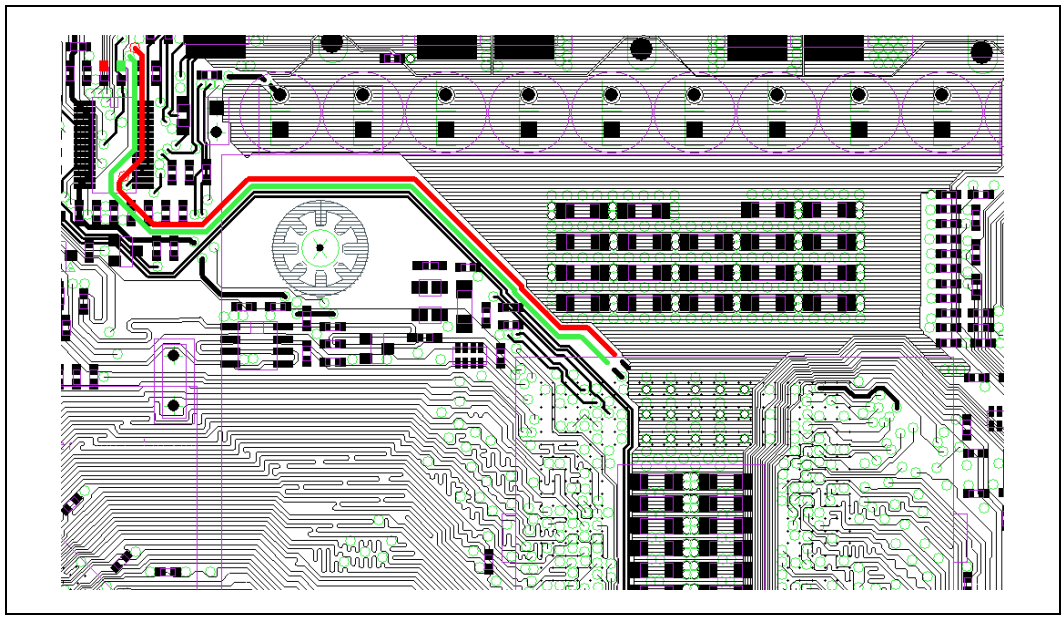


15.3.1.4 VRD 10.0 Feedback Network

The switching voltage regulators typically used for processor power delivery require the use of the feedback signal for output error correction. Intel recommends that the voltage regulator feedback is taken from the motherboard voltage plane near the north side of the socket.

The socket load line defined in the Voltage Regulator-Down (VRD)10.0 Design Guidelines is defined at pins AC14 (VCC_CPU) and AC15 (VSS) and should be validated from these pins as well. These pins are located approximately in the center of the pin field on the north side of the processor. Socket feedback for the voltage regulator controller should therefore be taken close to this area of the power delivery shape using wide, low inductive traces.

Figure 15-11. Routing of Feedback Signal



15.3.1.5 Thermal Considerations

For a power delivery solution to meet the Loadline A and Loadline B requirements, it must be able to deliver a fairly high amount of current. This high amount of current also requires that the solution is able to dissipate the associated heat generated by the components and keep all of the components and the PCB within their thermal specifications. OEMs should evaluate their component configurations, system airflow, and layout to ensure adequate thermal performance of the processor power delivery solution.

Intel recommends that the 848P chipset system boards be designed to support the full Pentium 4 processor on 90 nm process Loadline A guidelines. These guidelines include an I_{CC_MAX} electrically for brief time periods. The voltage regulator solution should also be designed to support a minimum of VR_TDC indefinitely within the envelope of operation conditions of the system. The VR_TDC limits of the system board are typically governed by the system board thermal limits. Intel recommends that system boards designed to the above guidelines implement a VR thermal monitor circuit.

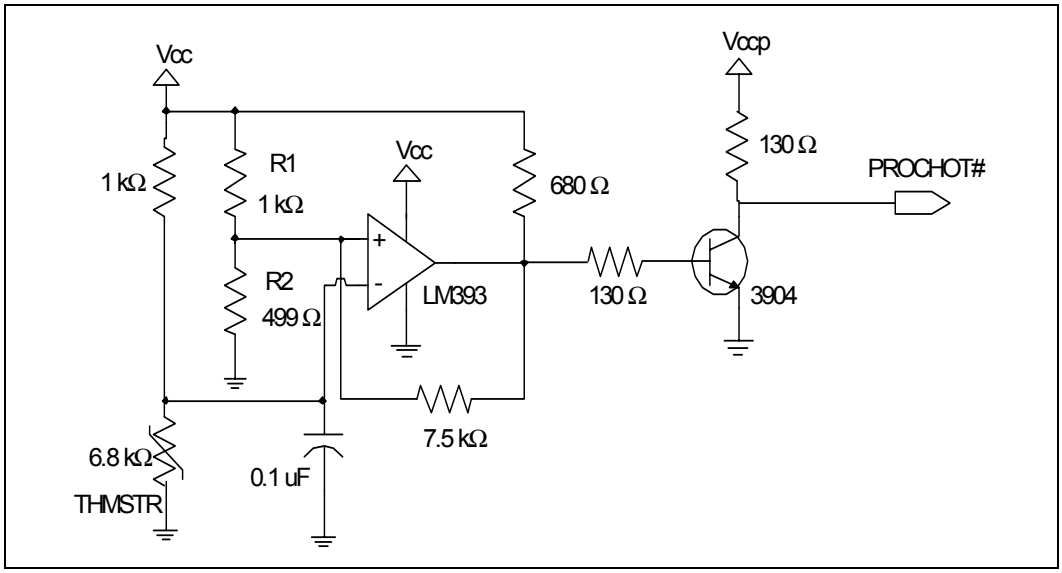
The voltage regulator shown is a two phase solution with four FETs per phase. The layout is optimized to provide adequate thermal relief for the motherboard and other components. The voltage regulator thermal performance was validated using the Intel reference heatsink and the boxed processor heatsink in a representative chassis running in a 25 °C and 35 °C external ambient environment.

Note: The specifications for Loadline A guidelines and I_{CC_MAX} of the processor are contained in the corresponding processor datasheet.

Note: The recommendation for the VR_TDC is contained in the *Voltage Regulator-Down (VRD) 10.0 Design Guidelines.*

The bi-directional PROCHOT# pin on the processor may be used to implement a thermal monitor for the processor VR. When PROCHOT# is asserted by a VR thermal monitor, the thermal control circuit in the processor will activate and will reduce the current consumption of the processor. This mechanism should only be used as a safety mechanism for the VR. The thermal monitor circuit should not degrade the processor performance during normal operation. PROCHOT# should only be asserted in the event of a failure that caused the VR over temperature. For this type of thermal monitor to act as a safety device for the system board, it is important that the thermal time constant of the VR be longer than the thermal time constant of the processor combined with its thermal solution. Figure 15-12 shows an example circuit that can be used as a VR thermal monitor.

Figure 15-12. Example VR Thermal Monitor Circuit



For this circuit implementation, the thermistor (THMSTR) should be placed in the hottest area of the VR. As the thermistor heats up, its resistance goes down. This creates an error voltage based on the resistance of the thermistor and the voltage reference provided by R1 and R2. The values of R1 and R2 should be adjusted to calibrate the circuit for a specific system board design so that it asserts PROCHOT# when the VR reaches its thermal limit. The values for R1 and R1 in Figure 15-12 are included as an example. The value of R2 is adjusted to calibrate the circuit so that PROCHOT# is asserted when the VR reached its thermal limit in the system that it is in tended to operate. An adequate VR cooling solution should be implemented such that VR_TDC current levels can be maintained indefinitely.

15.3.1.6 Simulation

To completely model the system board, one must include the inductance and resistance that exists in the cables, connectors, PCB planes, pins, and body of components (e.g., resistors and capacitors), processor socket, and the voltage regulator module. More detailed models showing these effects are shown in Figure 15-13.

Figure 15-13. Detailed Power Distribution Model for Processor with Voltage Regulator on System Board

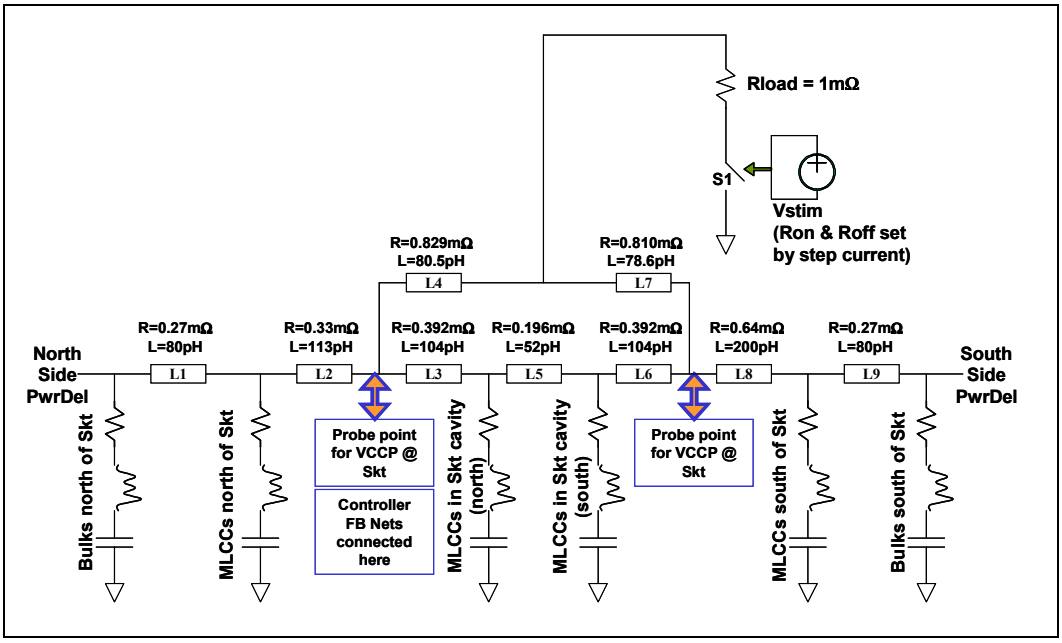


Table 15-3 lists the parameters for the system board shown in Table 15-13.

Table 15-3. Intel® Pentium® 4 Processor Power Delivery Model Parameters

Segment	Resistance	Inductance
L1	0.27 mΩ	80 pH
L2	0.33 mΩ	113 pH
L3	0.392 mΩ	104 pH
L4	0.829 mΩ	80.5 pH
L5	0.196 mΩ	52 pH
L6	0.329 mΩ	104 pH
L7	0.810 mΩ	78.6 pH
L8	0.64 mΩ	200 pH
L9	0.27 mΩ	80 pH

15.3.1.7 VCC_VID Regulator Guidelines

The VCC_VID power plane powers pins AF4 and AF3 of the processor and adheres to the following guidelines. Figure 15-15 shows an example of the VCC_VID routing. For details on timing requirements for VCC_VID, refer to the appropriate processor datasheet.

- The output of the voltage regulator used to generate VCC_VID should be no more than 1.5 inches away from pins AF3 and AF4 on the processor.
- The trace connecting the voltage regulator output to pins AF3 and AF4 should be as wide as practical, but no less than 25 mils.
- The trace connecting the voltage regulator output to pin AF3 and AF4 should have both a 0.1 µF and a 1.0 µF capacitor for decoupling. The 1.0 µF capacitor should be located as close as possible to the output of the voltage regulator and the 0.1 µF capacitor should be located as close as possible to pins AF3 and AF4 on the processor.
- The PG signal of the VCC_VID regulator should be pulled up to VCC_VID through a 2.43 kΩ resistor.

During power-on, the rising edge of the VCC_VID power supply needs to be monotonic.

Figure 15-14. VCC_VID Regulator Topology

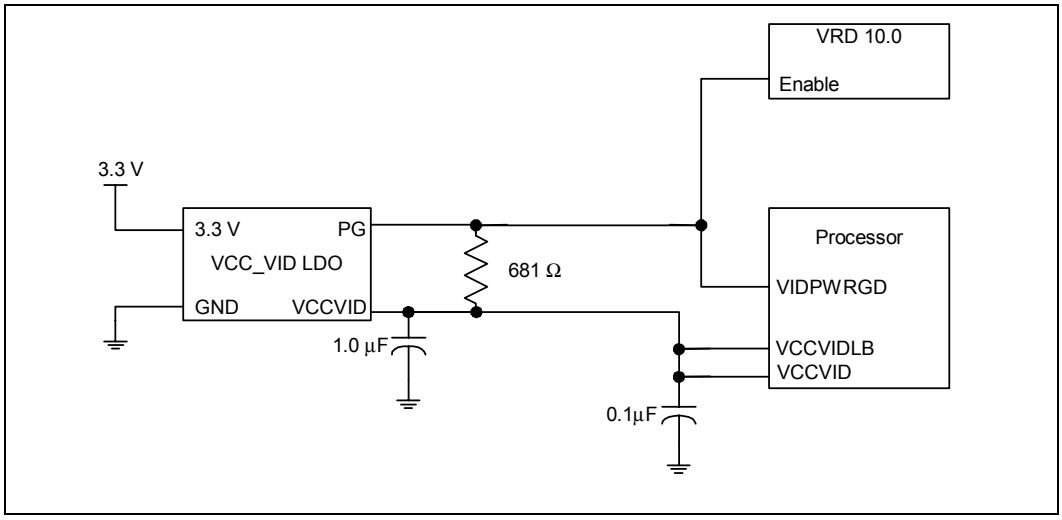
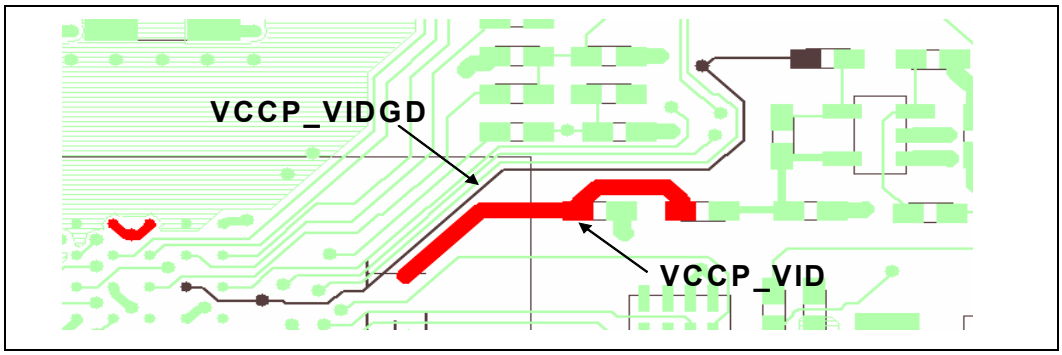


Figure 15-15. Example of VCC_VID Routing Layer 1

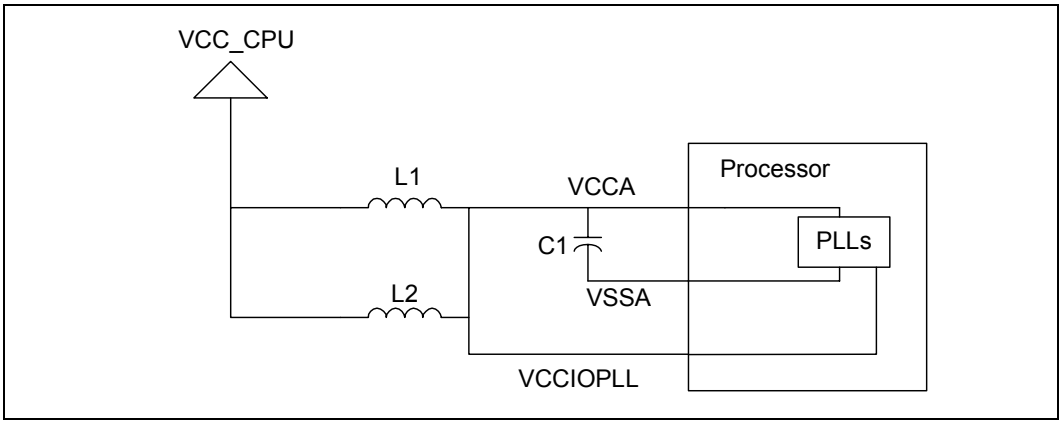


The bottom layer route is a straight route to the pin where it via's back to layer 1.

15.3.1.8 Processor Filter Specifications (VCCA, VCCIOPLL, and VSSA)

VCCA and VCCIOPLL are required by the PLL clock generators on the processor's silicon. Since these PLLs are analog circuits, they require quiet power supplies for minimum jitter. Jitter is detrimental to a system; it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). To prevent this degradation these supplies must be low-pass filtered from VCC_CPU. The general desired filter topology is shown in Figure 15-16. Not shown in the core is parasitic routing. Excluded from the external circuitry are parasitics associated with each component.

Figure 15-16. Typical VCCIOPLL, VCCA, and VSSA Power Distribution



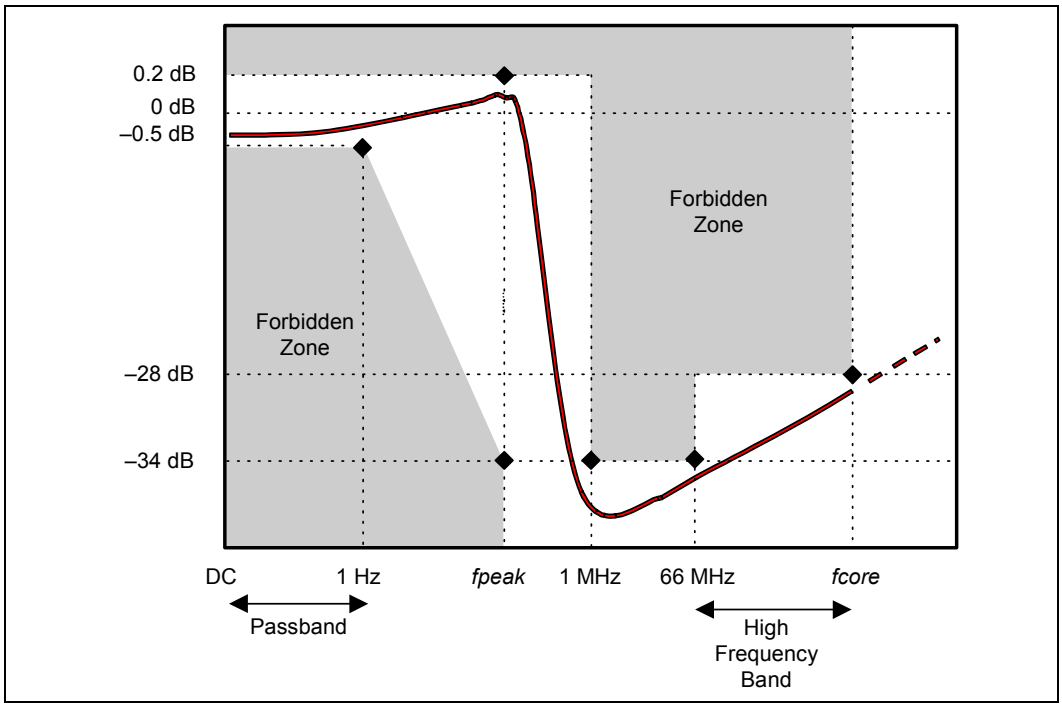
The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation; it also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity, we are addressing the recommendation for VCCA filter design. The same characteristics and design approach is applicable for the PLL filter design.

The AC low-pass specification, with input at VCC_CPU and output measured across the capacitor, is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- 34 dB attenuation from 1 MHz to 66 MHz
- 28 dB attenuation from 66 MHz to core frequency

The filter specification (AC) is graphically shown in Figure 15-17.

Figure 15-17. AC Filter Specification



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond *fcore (core frequency)*.
3. *Fpeak*, if existent, should be less than 0.05 MHz.

Other requirements:

- Use shielded type inductor to reduce crosstalk.
- Capacitor, C1: 22 µF – 33 µF with a 20% tolerance. The ESL is ≤ 2.5 nH and the ESR ≤ 0.225 Ω.
- Inductor: 10µH ± 25%. Rdc = 0.4 ± 30%. Self Resonant Frequency ≥ 30 MHz. IDC = 60 mA.
- Filter should support DC current of 100 mA.
- DC voltage drop from VCC_CPU to VCCA should be < 70 mV.
- To maintain a DC drop of less than 70 mV, the total DC resistance of the filter from VCC_CPU to the processor socket should be a maximum of 0.7 Ω.
- It is recommended that the total resistance of DCR plus routing does not exceed 0.36 Ω. This results in a maximum drop of 36 mV for 100 mA maximum.

Other routing requirements:

- C1 should be within 600 mils of the VCCA and VSSA pins. An example of the component placement is shown in Figure 15-18 and Figure 15-19.
- VCCA route should be parallel and next to VSSA route (minimize loop area).
- A minimum of a 12-mil trace should be used to route the filter to the processor pins.
- The inductors (L1 and L2) should be close to the capacitor C1.

Figure 15-18. VCCA and VSSA Layer 1 Routing

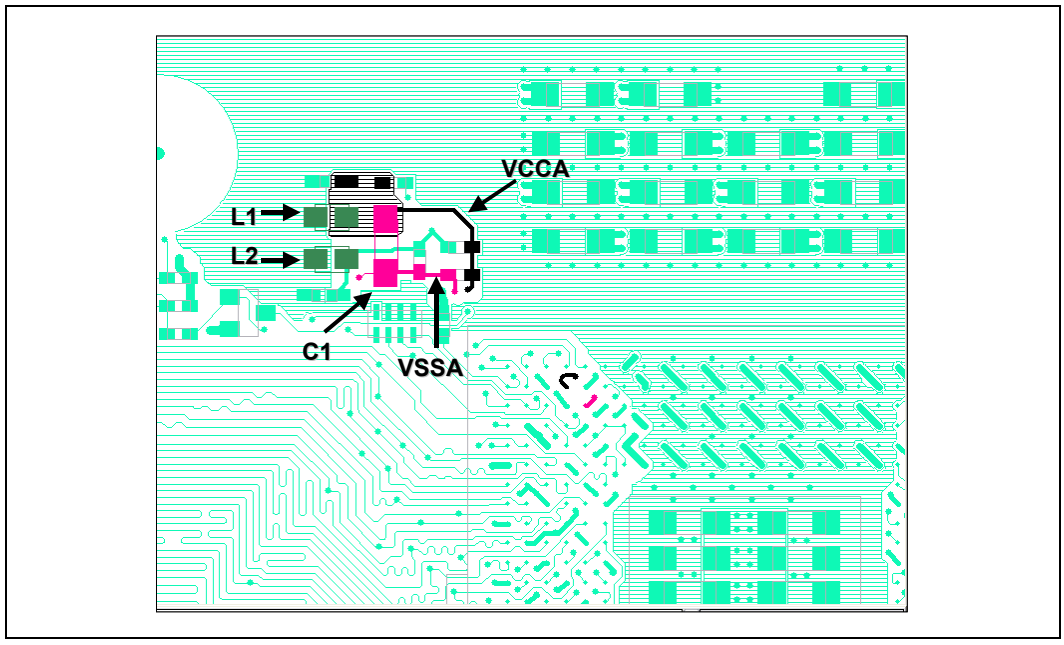
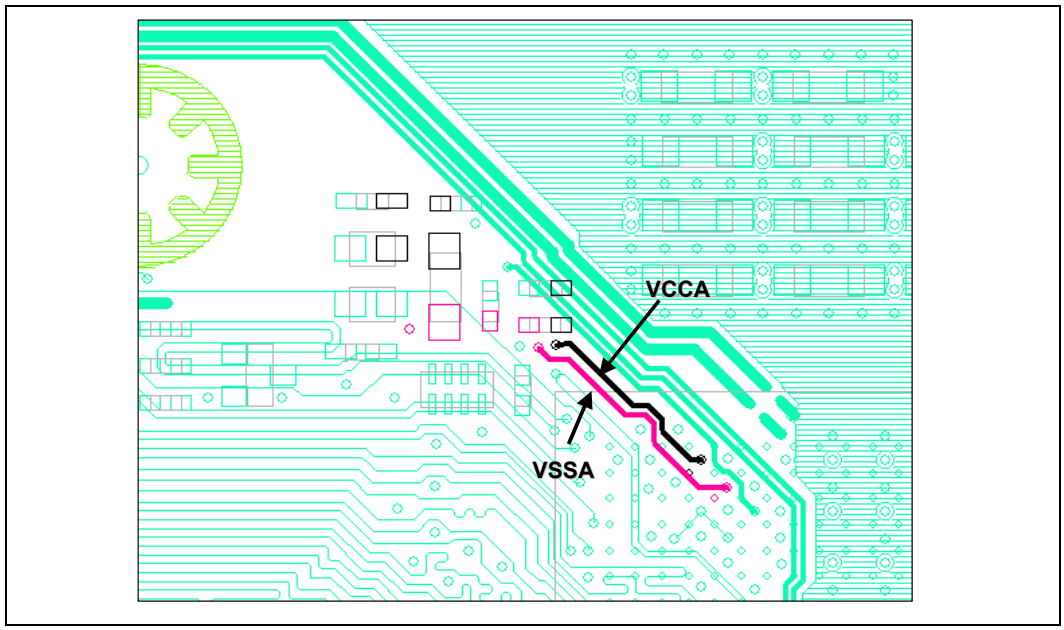


Figure 15-19. VCCA and VSSA Layer 4 Routing



15.3.1.9 Processor Power Sequencing

The Intel Pentium 4 Processor on 90 nm process has specific power-up sequencing requirements. For additional information on this processor, contact your Intel field representative.

15.3.2 Intel® Pentium® 4 Processor on 90 nm Process Loadline A Specifications

Refer to the *Intel® Pentium® 4 Processor on 90 nm Process Datasheet* for the latest Loadline A specifications.

15.3.2.1 Loadline Requirements

Platforms designed to Loadline A specifications should meet the loadline specifications listed in Table 15-4. Refer to the *Intel® Pentium® 4 Processor on 90 nm Process Datasheet* and the *Voltage Regulator-Down (VRD) 10.0 Design Guide* for the latest information.

Table 15-4. Loadline Requirements

Parameter	Loadline B	Loadline A
Socket Loadline	1.30 mΩ	1.24 mΩ
VRD Tolerance Band	± 25 mV	± 19 mV

15.3.2.2 Decoupling Requirements

For the processor voltage regulatory circuitry to meet the transient specifications of the processor, the bulk capacitor decoupling requirements have changed (see Table 15-5).

Table 15-5. Bulk Capacitor Decoupling Requirements

Parameter	Loadline B Bulk Cap Requirements	Loadline A Bulk Cap Requirements
Bulk Capacitors	560 µF	680 µF
ESR	5 mΩ	5 mΩ

15.3.2.3 VR Component Tolerance Requirements

The output inductor tolerances and the current sense capacitor tolerances have changed to meet the 1.24 mΩ loadline. Refer to the *Intel® 865G/865GV/865PE/865P Chipset Customer Reference Board Schematics Addendum for Intel® Pentium® 4 Processor on 90 nm Process and Loadline A platforms* for more details.

Table 15-6. Component Tolerance Requirements

Parameter	Loadline B Component Tolerance Requirements	Loadline A Component Tolerance Requirements
Output Inductor	25%	10%
Current Sense Caps	10% X7R	5% COG

15.3.2.4 VR Resistor and Capacitor Changes

There are changes to the VR feedback resistors and capacitors to set the static loadline to 1.24 mΩ and to set a no load offset of ± 19 mV. Refer to the *Intel® 865G/865GV/865PE/865P Chipset Customer Reference Board Schematics Addendum for Intel® Pentium® 4 Processor on 90 nm process and Loadline A Platforms* for more details about the resistor and capacitor changes.

15.3.2.5 Thermal Considerations

For a power delivery solution to meet the Loadline A requirements, it must be able to deliver a fairly high amount of current. This high amount of current also requires that the solution is able to dissipate the associated heat generated by the components and keep all of the components and the PCB within their thermal specifications. OEMs should evaluate their component configurations, system airflow, and layout to ensure adequate thermal performance of the processor power delivery solution.

The thermal solution requirements remain unchanged. Refer to the *Intel® Pentium® 4 Processor on 90 nm Process Thermal and Mechanical Design Guidelines* and the *Power Delivery Thermal Management for 478-Pin Socket Based Platform Design Guidelines* documents for the latest information.

Intel recommends that the Intel® 865 chipset family system boards be designed to support the full Pentium 4 processor on 90 nm process Loadline A guidelines. These guidelines include an I_{CC_MAX} electrically for brief time periods. The voltage regulator solution should also be designed to support a minimum of VR_TDC indefinitely within the envelope of operation conditions of the system. The VR_TDC limits of the system board are typically governed by the system board thermal limits.

Intel recommends the implementation of a bi-directional PROCHOT# based VR Thermal Monitor circuit for all Pentium 4 processor on 90 nm process platforms to enhance thermal robustness of VR designs.

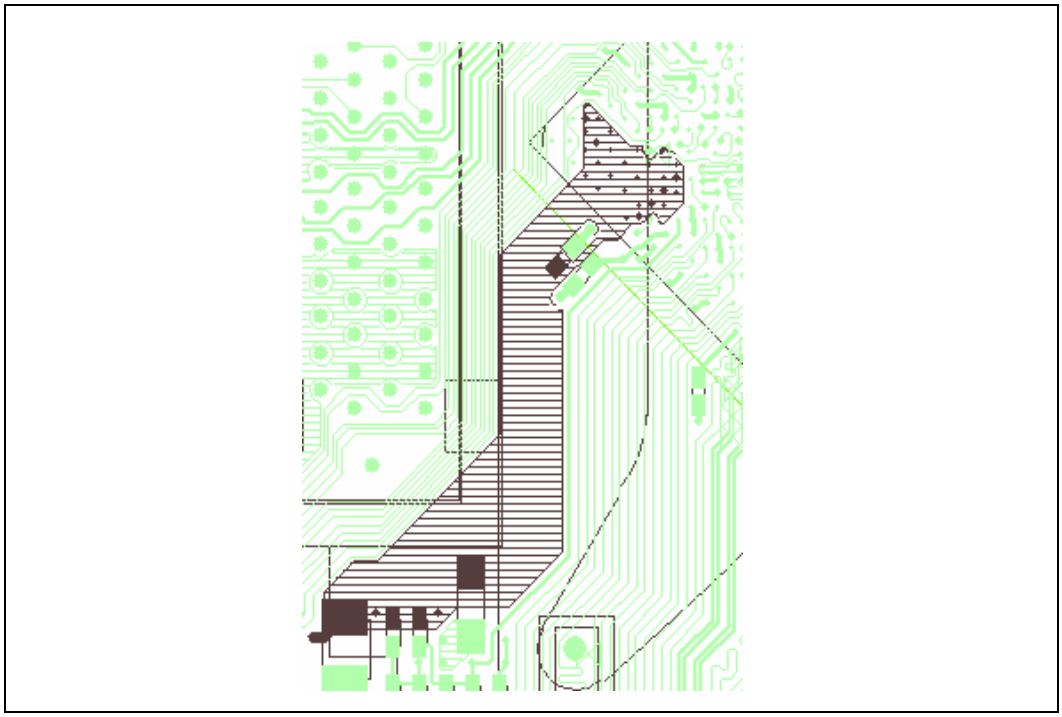
The specifications for I_{CC_MAX} of the Pentium 4 processor on 90 nm process are contained in the *Intel® Pentium® 4 Processor on 90 nm Process Datasheet*.

15.3.3 MCH Power Delivery Guidelines

Power is delivered to the MCH on all layers. Layer 1 provides 1.5 V HI/CSA/AGP and 2.6 V DDR. Layers 2 and 3 provide ground while layer 4 provides 1.5 V core power.

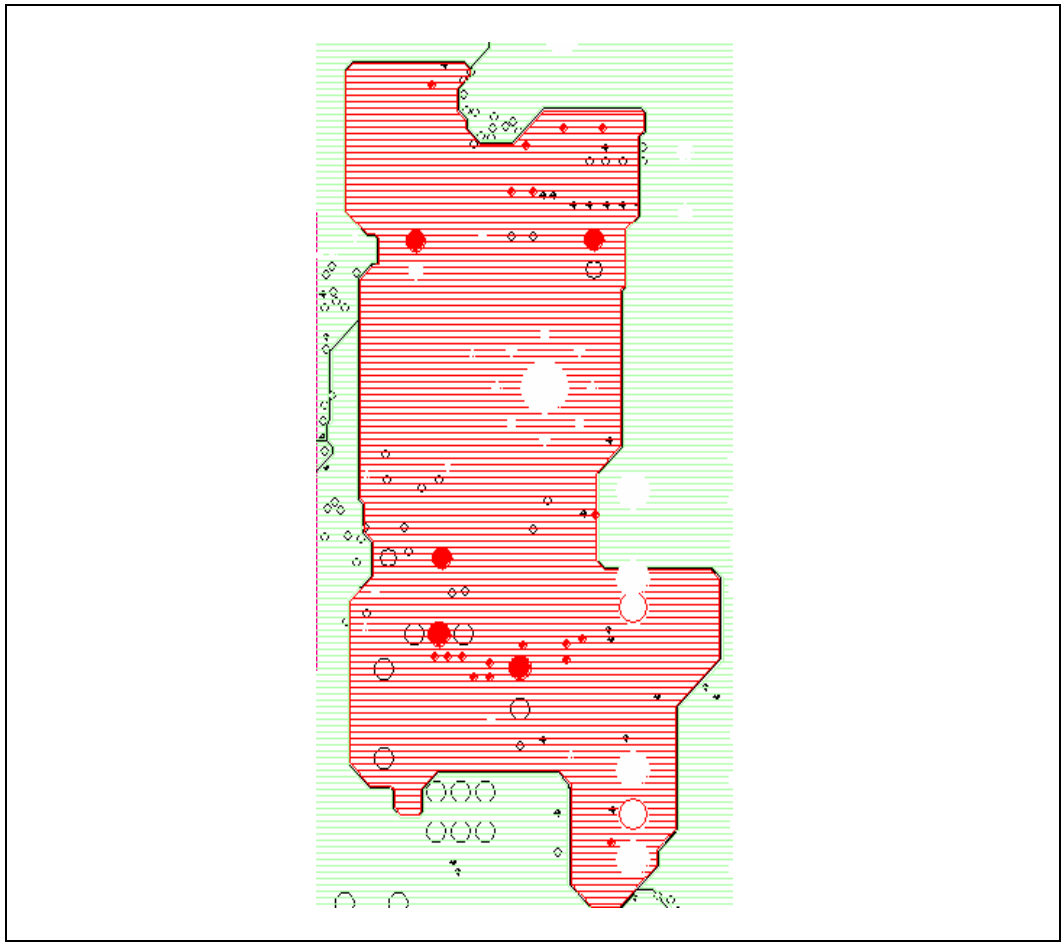
15.3.3.1 DDR (2.6 V Power Plane)

Figure 15-20. DDR Power Plane Layer 1



To meet the timings for DDR, it is imperative that the DDR power plane to the MCH and to the DIMMs have a maximum impedance of 15 mΩ. To accomplish this, it is very important to use wide, unobstructed planes with good current carrying capability. An example of this is shown in Figure 15-20 and in Figure 15-21.

Figure 15-21. 2.6 V Layer 2 DDR Power Plane



15.3.3.2 MCH_VTT (FSB Power Plane)

Figure 15-22. MCH_VTT Power Plane (Layer 1)

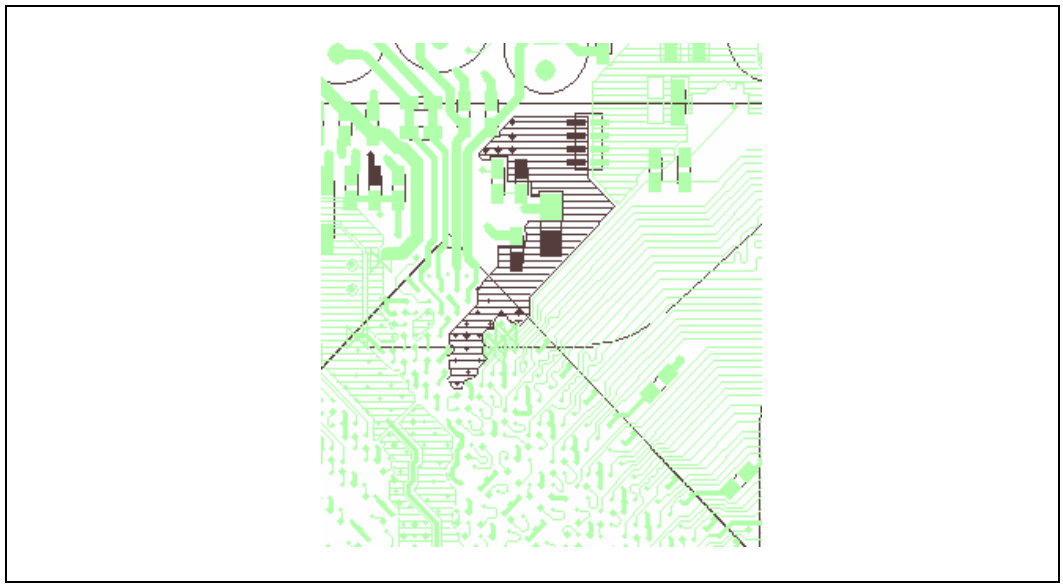
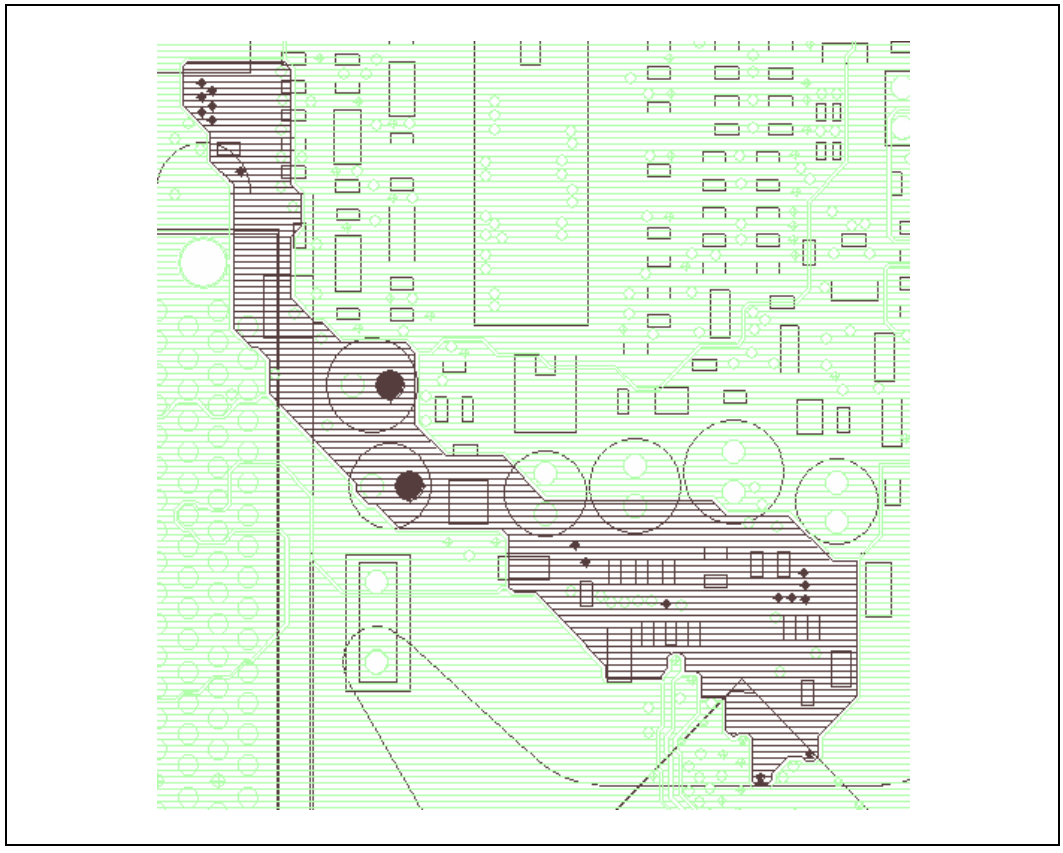


Figure 15-23. VCC_CPU Power Plane (Layer 2)



15.3.3.3 Hub, CSA, AGP, and Core Interface (1.5 V Power Plane)

Figure 15-24. 1.5 V Power Plane (Layer 1)

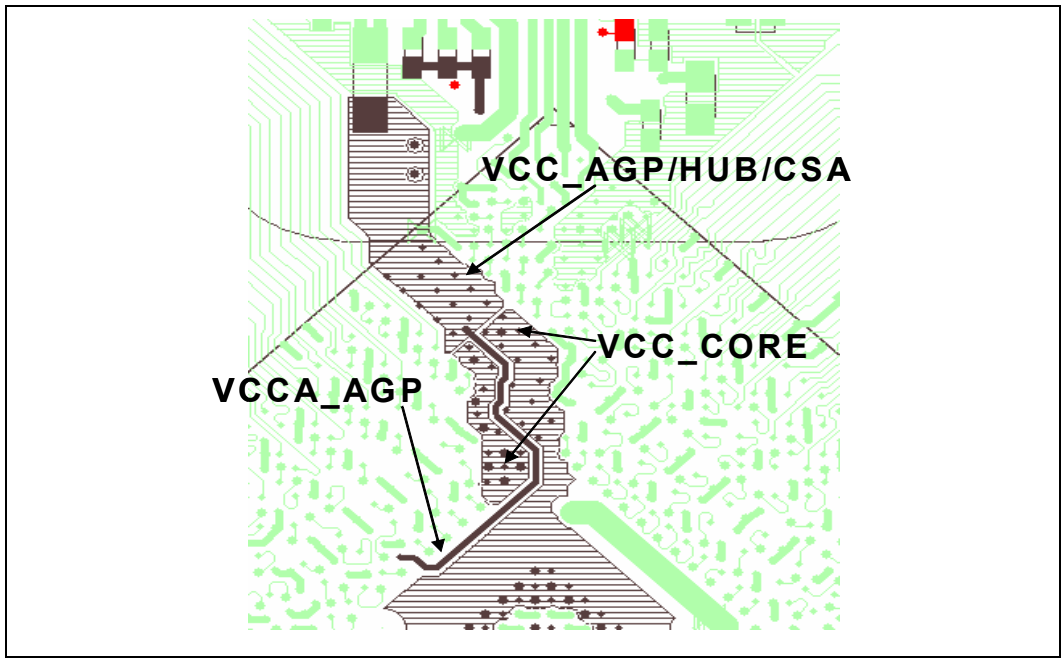


Figure 15-25. 1.5 V Power Plane (Layer 2)

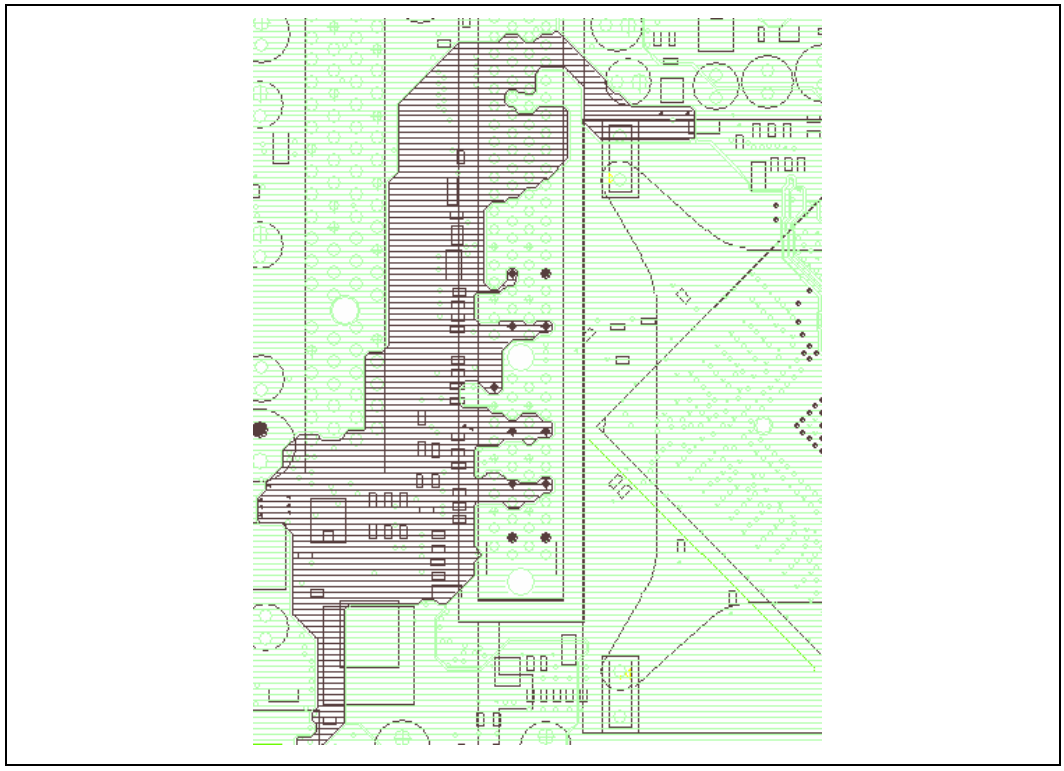
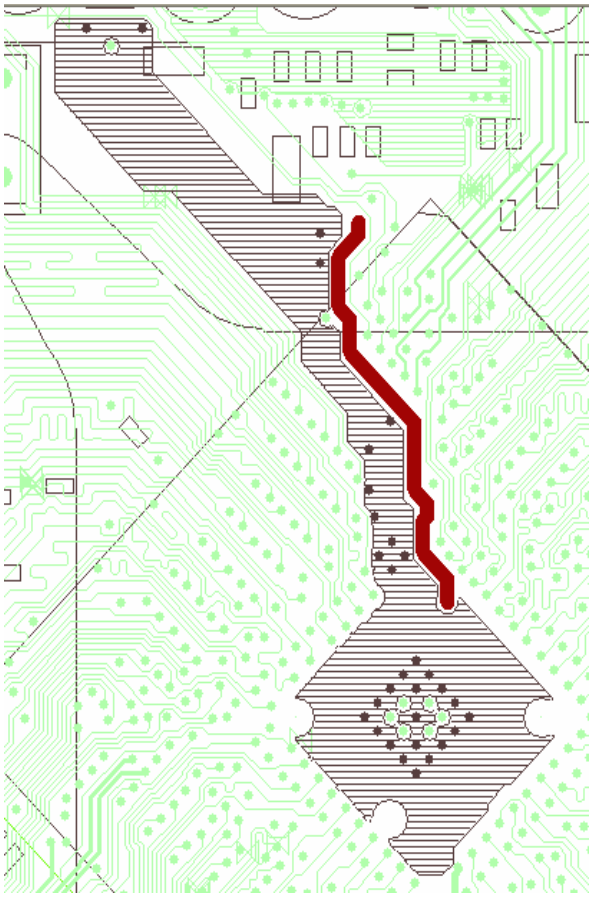


Figure 15-26. 1.5 V Power Plane (Layer 4)



15.3.3.4 Decoupling Recommendations

The following guidelines are recommended for an optimal MCH power delivery. The main focus of these guidelines is to minimize power noise and signal integrity problems to the 848P chipset. The following guidelines are not intended to replace thorough system validation on 848P chipset-based products.

Table 15-7. High-Frequency Decoupling Requirements for the MCH

Pin	Decoupling Requirements	Decoupling Type (Pin Type)	Decoupling Placement
MCH_VTT	(1) 0.47 µF (1) 0.47 µF (1) 0.1 µF (1) 0.1 µF	Edge Caps[2] Edge Caps[2] Edge Caps[2] Power Plane Decoupling	As close to ball A15 as possible As close to ball A21 as possible As close to ball A31 as possible As close to MCH as possible
VCC_1.5 HI, AGP, CSA	(1) 0.1 µF (1) 0.1 µF	Edge Cap[2]	As close to ball AG1 as possible As close to ball Y1 as possible
VCC_2.6	(1) 0.1 µF (1) 0.47 µF (1) 0.22 µF (1) 0.1 µF (1) 0.22 µF (1) 0.1 µF (1) 0.1 µF	Edge Cap[2] Edge Cap[2] Edge Cap[2] Edge Cap[2] Edge Cap[2] Edge Cap[2] Power Plane Decoupling	As close to ball AA35as possible As close to ball E35 as possible As close to ball R35 as possible As close to ball AL35 as possible As close to ball AR21 as possible As close to ball AR15 as possible As close to MCH as possible

NOTE: .
1. Unless otherwise noted, capacitors should be placed less than 100 mils from the package.
2. Edge Caps **must not** have vias in the trace from the capacitor to the MCH solder ball.

Figure 15-27. MCH High-Frequency Decoupling Capacitor Placement

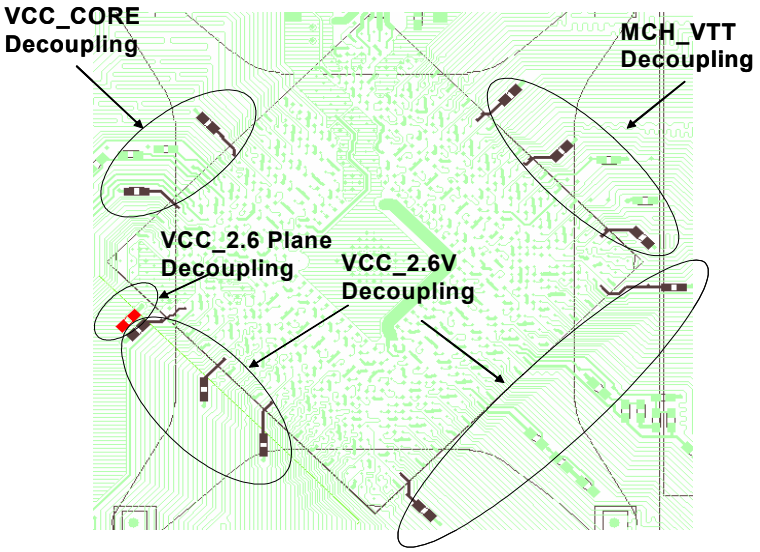


Figure 15-28. MCH Bulk Decoupling Capacitor Placement

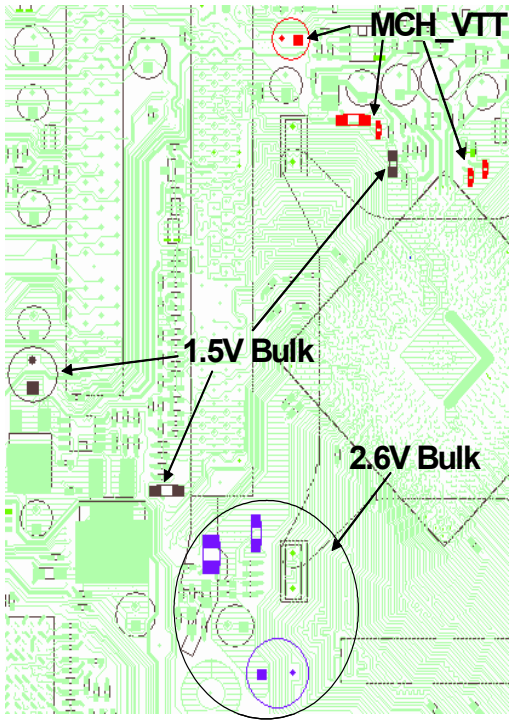


Table 15-8. Bulk Decoupling Requirements for MCH

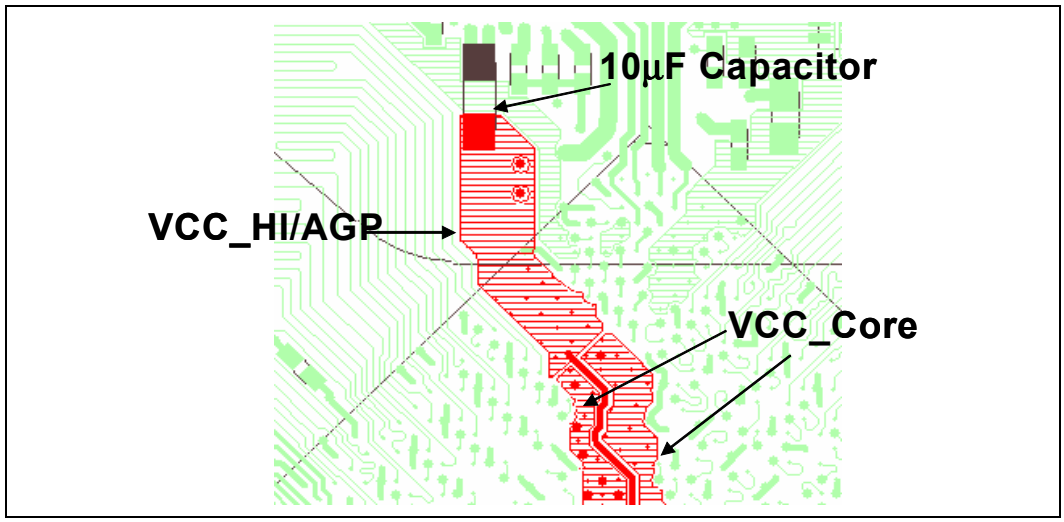
Plane	Decoupling Requirements	Decoupling Placement
MCH_VTT	(1) 0.1 µF (1) 0.47 µF (1) 1.0 µF (2) 4.7 µF (1) 470 µF	Place on MCH VTT plane using good layout practices (e.g., placing the smaller value capacitors closer to the MCH than the higher value capacitors).
VCC_2.6	(1) 22 µF (1) 4.7 µF	Place at the 2.6 V power plane transitions to layer 1 at the MCH.
VCC_1.5	10 µF 470 µF 4.7 µF	Place as close to where the 1.5 V core and 1.5 V AGP/CSA planes diverge. Place at the output of the 1.5 V VR Place between the VR and the MCH

15.3.4 MCH Filter Specifications

15.3.4.1 Plane Filter

A 1.5 V core power needs to be filtered from the 1.5 V AGP, HI, and CSA power. This is easily accomplished by having two separate power floods into the MCH for 1.5 V power. One power flood will be on layer 4 which will supply 1.5 V power for the core, while on layer 1 the 1.5 V power flood will supply power for AGP, HI, and CSA. To filter these planes, each flood will need to be referenced to ground and at the point where the two planes separate, there needs to be one, 0805 10 µF capacitor.

Figure 15-29. MCH Filter Topology for 1.5 V Core



15.3.4.2 Analog Filters

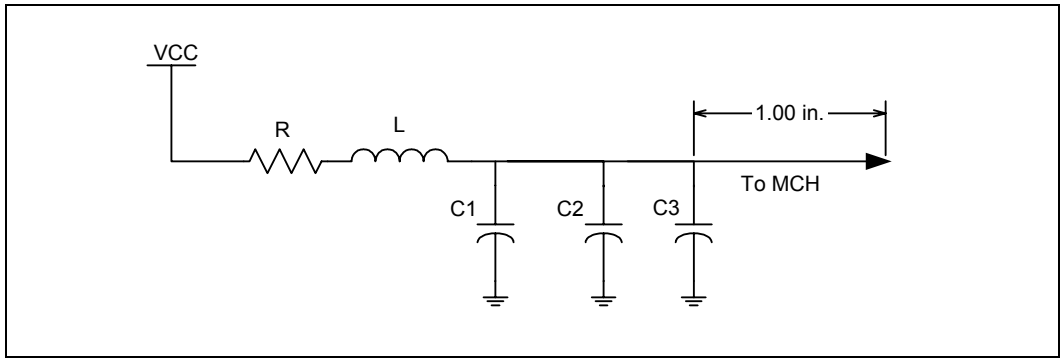
In addition to the plane filters, there are an additional four analog filter circuits that are required for the MCH's VCCA_DDR and VCCA_FSB pins.

Table 15-9. MCH Analog Filter Requirements

Required Filters	Filter Current Capability (mA)	Filter DC Resistance (Ω)[1]	Max DC Drop (mV)[2]	Pass Band Gain (dB)	f1	f2	Attenuation from f1 to f2 (dB)
VCCA_FSB	30	2.3	70	< +0.2, > -0.5	50 MHz	800 MHz	-30
VCCA_DDR	1000	0.070	70	< +0.2, > -0.5	50 MHz	400 MHz	-30

NOTES:
1. Filter DC resistance is the inductor resistance + MB routing resistance.
2. DC drop across filter includes voltage drop across the inductor and across the MB trace.

Figure 15-30. MCH Analog Filter Topologies



The recommended component values for the filter are listed in Table 15-10. The VCCA_AGP does not require a filter, but it does need to connect to the VCCA_AGP power plane. Therefore, a 14-mil wide trace or wider needs to be routed from the VCCA_AGP pin to the power plane. Figure 15-31 shows an example of this routing.

Figure 15-31. VCCA_AGP Routing

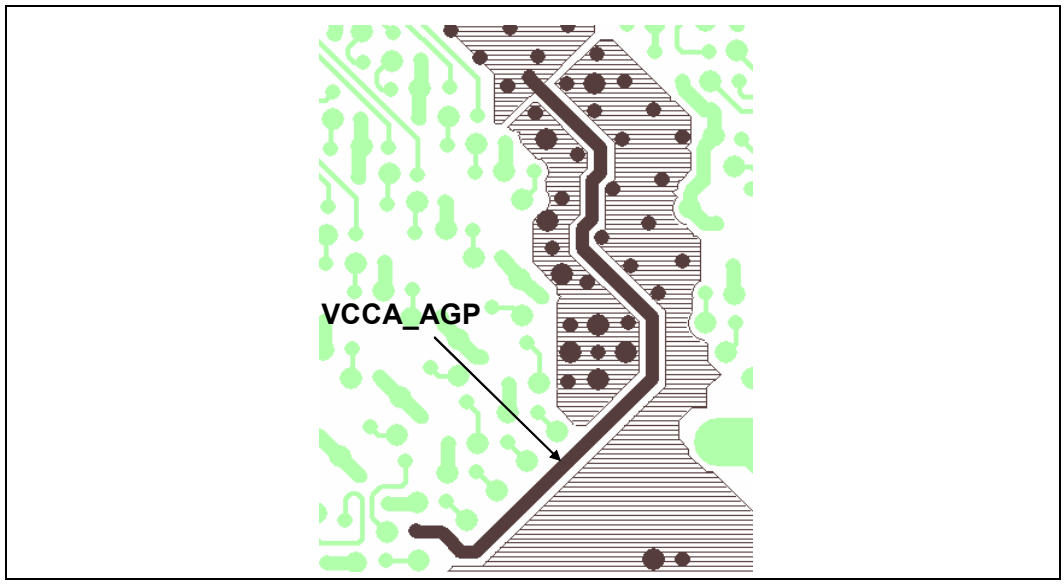


Table 15-10. MCH Analog Filter Components

Component	Value	Package Type
VCCA_DDR Filter		
VCC	1.5 V	
R	0 Ω	NA
L[2]	1 µH	1210
C1	NA	NA
C2	100 µF	Aluminum
C3	0.1 µF	0603
VCCA_FSB Filter		
VCC	1.5 V	
R	0 Ω	NA
L[3]	0.82 µH	0603
C1	NA	NA
C2	100 µF	Aluminum
C3	0.1 µF	0603

NOTES:
1. R can be created with a trace and should be placed in series in front of the inductor. The trace resistor can be calculated using the following equation: R=(0.65866x10^{-6})(Trace Length")/(trace width" * trace thickness").
2. The DCR of the inductor must be < 50 mΩ.
3. The DCR of the inductor must be ≤ 2.1 Ω.

The VCCA_DDR trace is carrying 1 A of current and DC resistance of this trace needs to be kept at or below 50 mΩ. To do this, it is recommended to route the VCCA_DDR with a trace width of 50 mils when possible. When routing under the MCH ball field, it is acceptable to neck the trace down to 35 mils. Figure 15-32 and Figure 15-33 show an example of the recommended routing.

Figure 15-32. Layer 1 VCCA_DDR

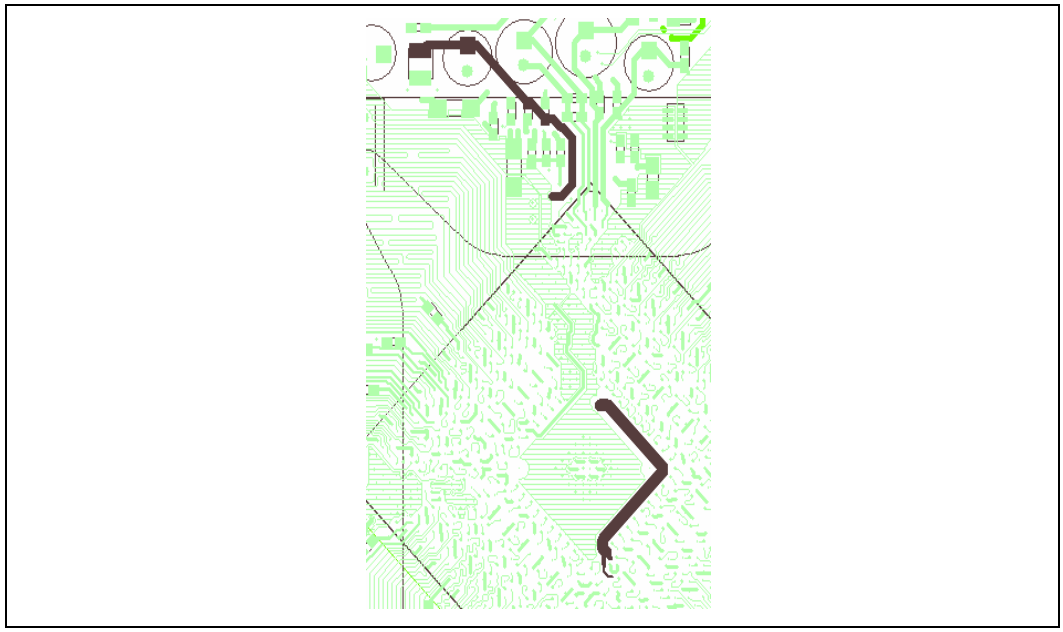
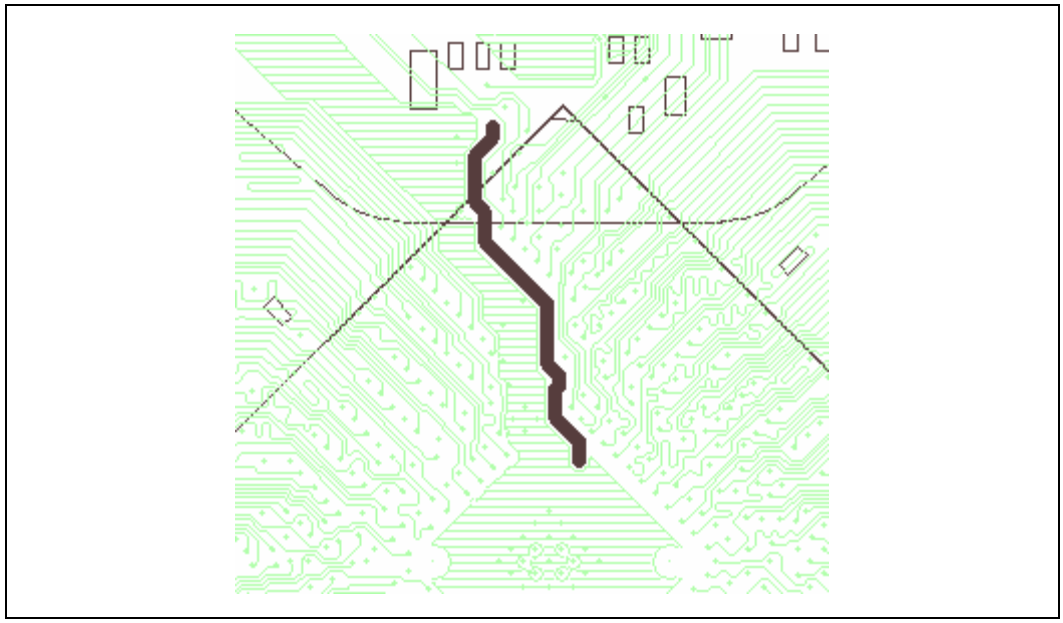


Figure 15-33. Layer 4 VCCA_DDR



15.3.4.3 MCH Power/Reset Sequencing Requirements

There are no power sequencing requirements for the MCH; however, the following timings must be met:

- GCLKIN must be valid at least 10 µs prior to the rising edge of PWROK.
- HCLKN/HCLKP must be valid at least 10 µs prior to the rising edge of RSTIN#.
- The MCH core VCC must be held at a nominal (>95%) level for at least 30 µs after PWROK is deasserted. Also, the 2.6 V rail should be able to supply the nominal MCH current (not to exceed maximum specifications documented in the datasheet) until 100 ns after PWROK to the MCH is deasserted (S3 entry) and 100 ns before PWROK is re-asserted (S3 exit).
- If the MCH PWROK and ICH5 PCIRST# signals are deasserted, then power must be fully cycled on the platform to ensure proper MCH operation.

15.3.5 DDR DIMM Power Deliver

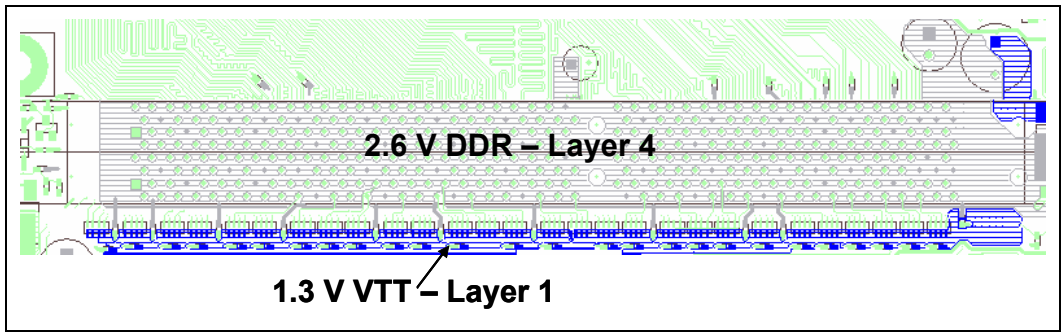
15.3.5.1 2.6 V Power Delivery

The 2.6 V power is delivered on layer 4 using a copper flood under the DIMMs. This copper flood forms a parallel plate capacitor with the ground plane on layer 3. To meet DDR timings, it is important to make sure that DC resistance of the 2.6 V power plane is as low as possible. Figure 15-34 shows an example of this power delivery scheme.

15.3.5.2 1.3 V VTT Power Delivery

The 1.3 V VTT power is delivered on layer 1 as shown in Figure 15-34.

Figure 15-34. DDR DIMMs Layer 4 Power Delivery

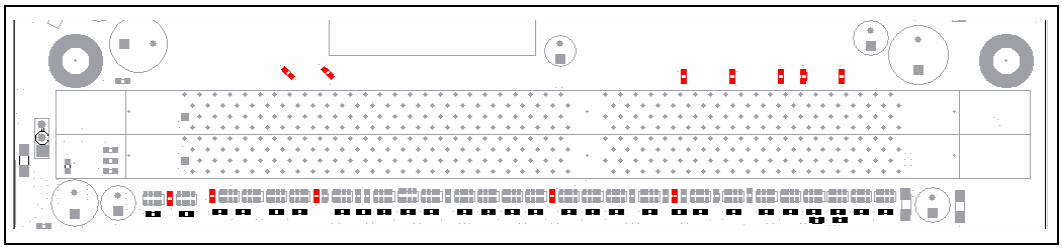


15.3.5.3 DDR DIMMs Decoupling

Table 15-11. DDR DIMMs High-Frequency Decoupling

Pin	Decoupling Requirements	Decoupling Type (Pin Type)	Decoupling Placement
VCC_2.6	(21) 0.1 µF	Decoupling Capacitors	As close to power the DIMM power pins as possible and sprinkled through out the DDR power flood.
VTT_1.3	(27) 0.1 µF	Decoupling Capacitors	As close to Termination resistors as possible

Figure 15-35. DDR DIMM High-Speed Decoupling



NOTES:
1. 2.6 V high-frequency decoupling is marked in red
2. 1.3 V high-frequency decoupling is marked in black

Table 15-12. Bulk Decoupling Requirement for DIMMs

Pin	Decoupling Requirements	Decoupling Placement
VCC_2.6	(1) 4.7 µF (1) 22 µF (1) 333 µF (1) 560 µF (4) 470 µF	Place at output of the VR as close to the DIMMs as possible. Place at each corner of the DIMMs.
VTT_1.3	(1) 4.7 µF (1) 470 µF (1) 1500 µF	Place at output of the VR as close to the DIMMs as possible.

15.3.6 Intel® ICH5 Power Delivery Guidelines

15.3.6.1 Power Supply PS_ON Consideration

If a pulse on SLP_S3# or SLP_S5# is short enough (~10 – 100 ms) such that PS_ON is driven active during the exponential decay of the power rails, a few power supply designs may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. **These power supplies would need to be unplugged and re-plugged to bring the system back up.** Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

The ATX specification does not specify a minimum pulse width on PS_ON deassertion. This means that power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issues in all case).

The platform designer must endure that the power supply used with the platform is not affected by this issue.

15.3.6.2 SLP_S4# Assertion Width

When removing and reapplying power to the DRAM, the DRAMs need to see the power supply down for a minimum period of time before it may be treated as a “cold reset” and safely power up. All cases in which the DRAM power is removed could potentially be a problem if the minimum time requirement is not met. This potentially could occur during resume from S4/S5. To address this potential issue the ICH5 has implemented timers to help ensure that this minimum period of time is met.

The aforementioned time is the assertion width of SLP_S4#. If the assertion width is less than the minimum period of time set in SLP_S4# Minimum Assertion Width register (D31:F0, offset A4h), the ICH5 has provided a means to help ensure that this minimum time is met. The amount of time required to safely power up is DRAM-specific.

To correctly set this value in the BIOS, the VCC_DDR ramp down time from SLP_S4# signal going active must first be measured. Measurements should be made from the assertion of SLP_S4# until the complete deassertion of VCC_DDR -> 0 V. On the Customer Reference Board (CRB), the 2.6 V ramp down time is less than 1 sec; therefore, the BIOS can program ICH5 Device 31, Function 0 Register A4h, bits 5:4 to a value of 11b (i.e., SLP_S4# minimum assertion width of 1 to 2 seconds). Contact your Intel field representative for the latest BIOS information for programming the correct value. This feature can be disabled using bit 3 of the same register.

15.3.6.3 3.3 V/1.5 V Power Sequencing

There is a power sequencing requirement for the associated 3.3 V/1.5 V rails or the rail of the ICH5. Vcc1_5 should come up prior to Vcc3_3 or after within 0.7 V.

15.3.6.4 1.5V/V_CPU_IO Power Sequencing

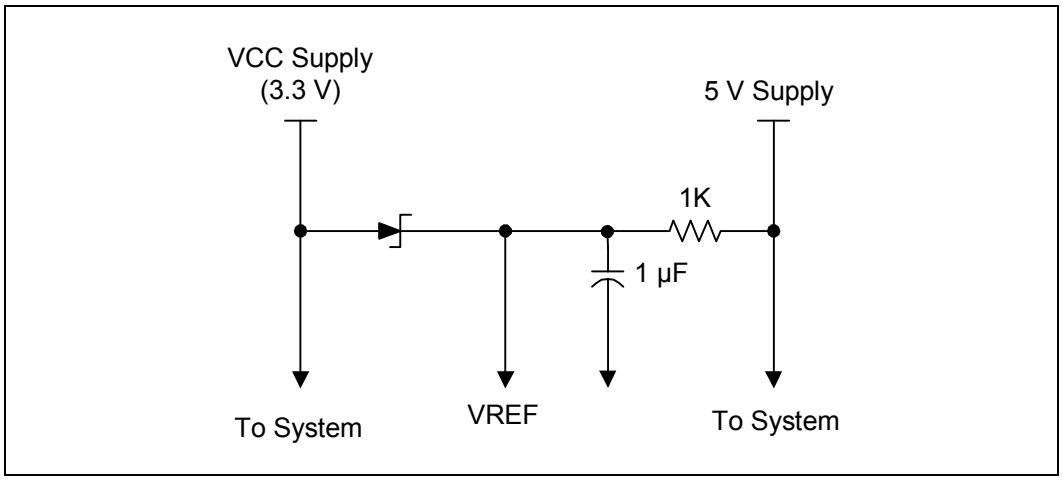
Vcc1_5 should come up prior to V_CPU_IO or after within 0.7 V.

15.3.6.5 3.3 V/V5REF Sequencing

V5REF is the reference voltage for the 5 V tolerant input buffers on the ICH5. V5REF must be powered up before VCC3_3, or after VCC3_3 within 0.7 V. Also, 5VREF must also power down after VCC3_3 or before VCC3_3 within 0.7 V. These rules must be followed to ensure the safety of the ICH5. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 15-36 shows a sample implementation of how to satisfy the V5REF/VCC3_3 sequencing rule.

This rule also applies to V5REF_Sus and VccSus3_3. However, in most platforms, the VccSus3_3 rail is derived from the 5 VSB through a voltage regulator and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus (which is derived directly from VccSus5) will always be powered up before VccSus3_3; thus circuitry to satisfy the sequence requirement is not needed. However, in platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be observed in the platform design as described above (See Figure 15-36).

Figure 15-36. Example 3.3 V/V5REF Sequencing Circuitry



15.3.6.6 Intel® ICH5 Power Delivery

Power delivery to the ICH5 is accomplished on all four layers.

Figure 15-37. Intel® ICH5 Layer 1 Power Delivery

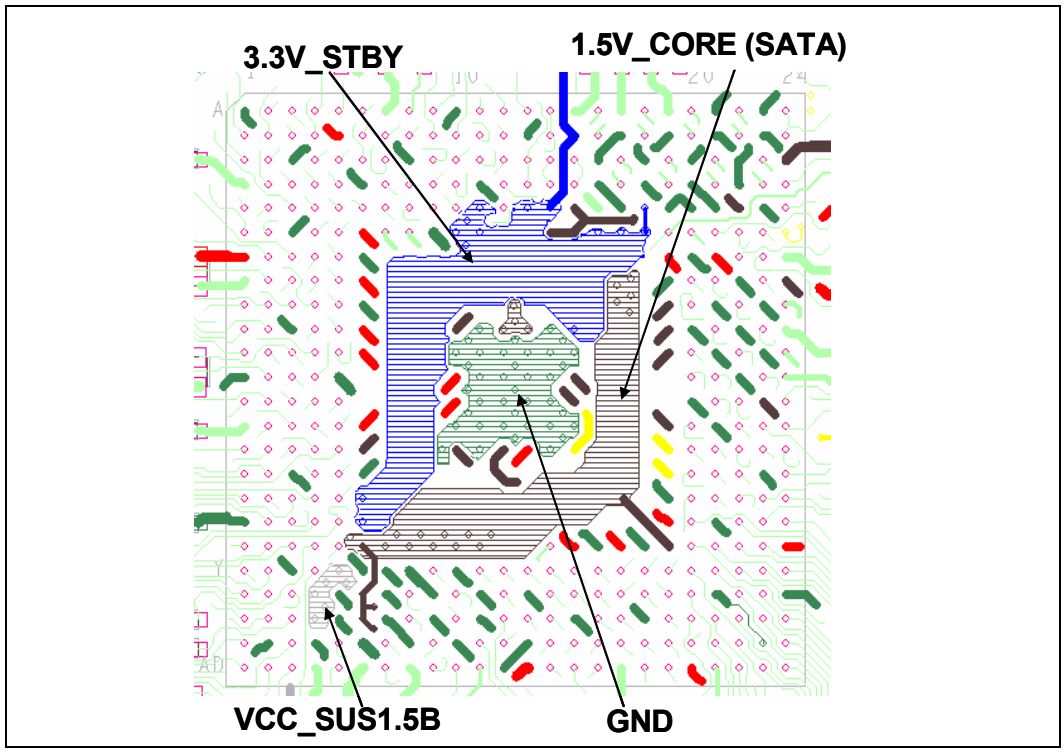
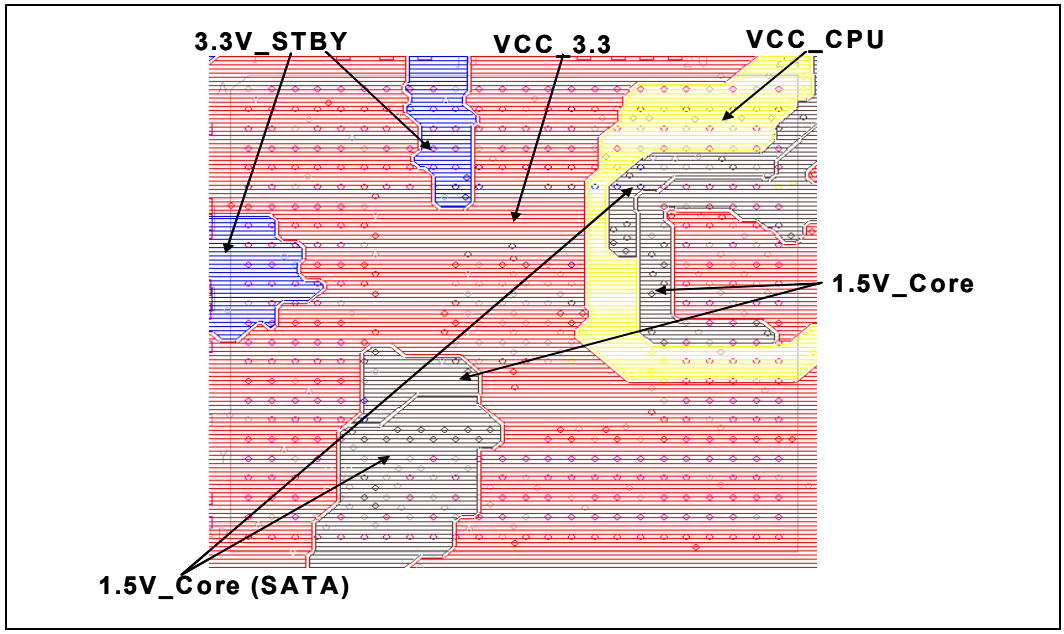


Figure 15-38. Intel® ICH5 Layer 2 Power Delivery



To reduce noise coupling from the ICH5 core plane to the ICH5 SATA power plane, it is recommended that the two rails be separated on the motherboard even though they are powered by the same voltage regulator. A split should be made in the 1.5 V core power plane to isolate the SATA/USB power balls (W6–W11, AA6, AB6, W19, E22, C24, F14, F15, E15) from the core power balls (H24, J19, K19, L19, P19, N23, R6, R10, R12, M15, N15, K10, K12, K13). Figure 15-39 and Figure 15-40 show examples of this.

Figure 15-39. Layer 2 Close Up

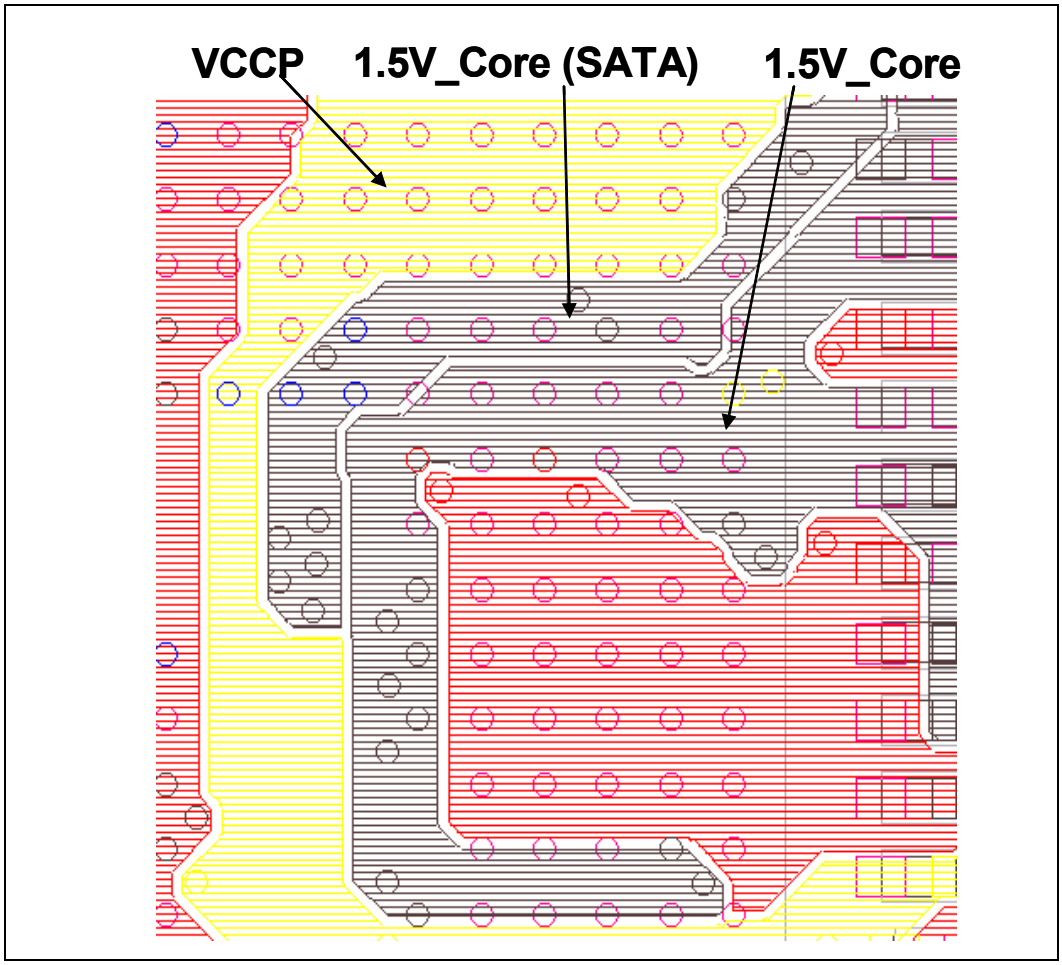


Figure 15-40. Layer 2 Close Up

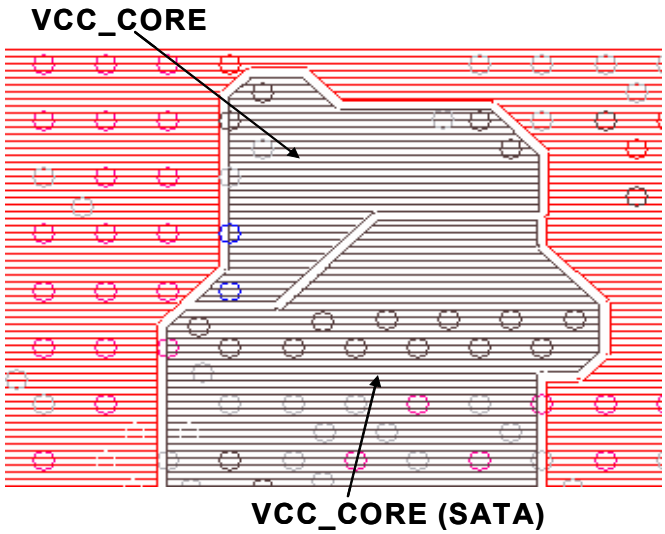
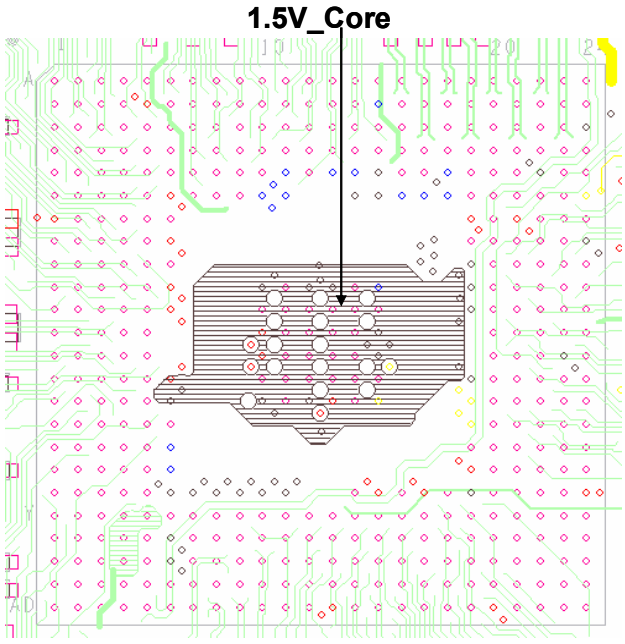


Figure 15-41. Intel® ICH5 Layer 4 Power Delivery



15.3.6.7 Intel® ICH5 Decoupling

The ICH5 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in Table 15-42 to ensure the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible (100 mils nominal). It is recommended that for prototype board designs the designer include pads for extra power plane decoupling capacitors.

Figure 15-42. Decoupling Requirements for Intel® ICH5

Pin	Capacitor	Quantity	Decoupling Type (Pin Type)	Decoupling Placement
VCC3_3	0.1 µF	6	Decoupling Cap (VSS)	• Place near balls A1, A7, H1, P1, AD12, and AD21.
VccSus3_3	0.1 µF 0.01 µF 1.0 µF	3 1 1	Decoupling Cap (VSS)	• Place 0.1 µF capacitors near balls A15, A23, and V1. • Place additional capacitors near balls A17, A19, and A21.
V_CPU_IO	0.1 µF	1	Decoupling Cap (VSS)	• Place near ball T24
Vcc1_5	0.1 µF 0.01 µF	4 1	Decoupling Cap (VSS)	• Place 0.1 µF capacitors near balls L24, C24, D8, G24, M24, and AD18. • Place 0.01 µF capacitor near ball AD18.
VccSus1_5_A	0.01 µF	1	Decoupling Cap (VSS)	• Place capacitor for VccSus1_5_A near ball A19. See Figure 15-43.
VccSus1_5_B	0.01 µF	1	Decoupling Cap (VSS)	• Place capacitor for VccSus1_5_B near ball AD4. See Figure 15-43.
VccSus1_5_C	0.01 µF	1	Decoupling Cap (VSS)	• Place capacitor for VccSus1_5_C near ball A7. See Figure 15-43.
V5REF	0.1 µF	1	Decoupling Cap (VSS)	• Place near ball A8.
V5REF_Sus	0.1 µF	1	Decoupling Cap (VSS)	• Place near ball A17.
VccRTC	0.1 µF	2	Decoupling Cap (VSS)	• Place near ball AD11.
VccUSBPLL	0.1 µF 0.01 µF	1 1	Decoupling Cap (VSS)	• Place near ball D24.
VccSATAPLL	0.1 µF 0.01 µF	1 1	Decoupling Cap (VSS)	• Place near ball AD6.

NOTE: Capacitors should be placed less than 100 mils from the package.

Figure 15-43. Intel® ICH5 Decoupling Capacitor Placement for VccSus1_5

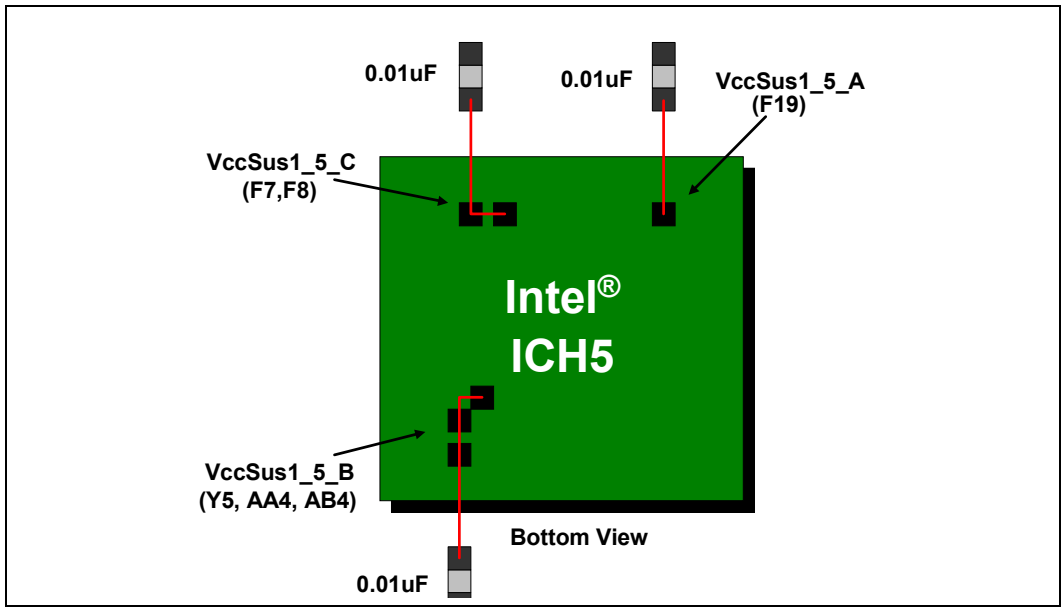
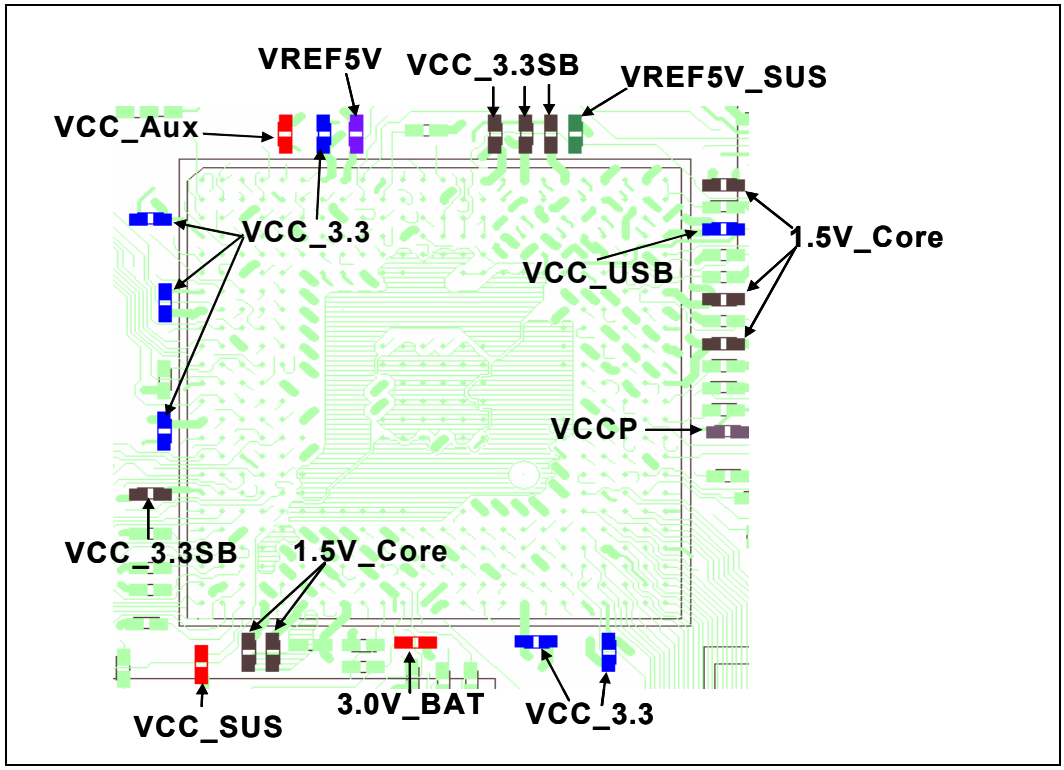


Figure 15-44. Intel® ICH5 Example Decoupling Capacitor Placement



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EMI Design Guidelines 16

This chapter contains general EMI design considerations.

16.1 Introduction

This section is intended to provide electrical and mechanical design engineers with information that will aid in developing a platform that will meet government EMI regulations. Processor shielding, differential and spread spectrum clocking, and the test methodology impact to FCC Class B requirements are specifically discussed.

Designers should be aware that implementing all the recommendations in this guideline will not guarantee compliance to EMI regulations. Rather, these guidelines may help to reduce the emissions from processors and motherboards and make chassis design easier.

Terminology

Electromagnetic Interference (EMI): Electromagnetic radiation from an electrical source that interrupts the normal function of an electronic device.

Electromagnetic Compatibility (EMC): The successful operation of electronic equipment in its intended electromagnetic environment.

16.1.1 Brief EMI Theory

Electromagnetic energy transfer can be viewed in four ways: radiated emissions, radiated susceptibility, conducted emissions, and conducted susceptibility. For system designers, reduction of radiated and conducted emissions is the way to achieve EMC compliance. Susceptibility is typically not a major concern in the server environment although it may be more important in an industrial environment.

The main component of EMI is a radiated electromagnetic wave, which consists of both electric (E-fields) and magnetic (H-fields) waves traveling together and oriented perpendicular to one another. Although E- and H-fields are intimately tied together, they are generated by different sources. E-fields are created by voltage potentials while H-fields are created by current flow. In a steady state environment (where voltage or current is unchanging), E- and H-fields are also static and of no concern to EMI. Changing voltages and currents are of concern since they contribute to EMI. If a dynamic E-field is present, there must be a corresponding dynamic H-field, and vice versa. Motherboards with fast processors will generate high frequency E- and H-fields from currents and voltages present in the component silicon and signal traces.

Two methods exist for minimizing E- and H-field system emissions: prevention and containment. Prevention is achieved by implementing design techniques that minimize the ability of the motherboard to generate EMI fields. Containment is used in a chassis environment to contain radiated energy within the chassis. Careful consideration of board layout, trace routing, and grounding may significantly reduce a motherboards' radiated emissions and make the chassis design easier.

16.1.2 EMI Regulations and Certifications

Original Equipment Manufacturers (OEMs) ensure EMC compliance by meeting EMI regulatory requirements. System designers must ensure that their computer systems do not exceed the emission limit standards set by applicable regulatory agencies. Regulatory requirements referenced in this document include:

- United States Federal Communication Commission (FCC) Part 15 Class B
- International Electrotechnical Commission's International Special Committee on Radio Interference (CISPR) Publication 22 Class B limits

The FCC rules are viewed to require any OEM who sells an "off-the-shelf" motherboard in the United States to pass an open chassis test. Open chassis testing is defined as removing the chassis cover (or top and 2 sides) and testing for EMI compliance (although permitted emission levels are allowed to be higher). Removing the cover greatly reduces the shielding provided by the chassis and increases the amount of EMI radiation. The purpose of this regulation is to ensure that system boards have reasonable emission levels since they are one of the main contributors to EMI.

16.2 EMI Design Considerations

The following sections discuss design techniques that may be applied to minimize EMI emissions. Some ideas have been incorporated into Intel-enabled designs (differential clock drivers, selective clock gating, etc.) and some must be implemented by motherboard designers (trace routing, clocking schemes, etc.).

16.2.1 Spread Spectrum Clocking (SSC)

Spread Spectrum Clocking is defined as continuously ramping (or modulating) the processor clock frequency over a predefined range (see Figure 16-1). SSC reduces radiated emissions by spreading the radiated energy over a wider frequency band (see Figure 16-2). Thus, instead of maintaining a constant system frequency, SSC modulates the clock frequency along a predetermined path (or modulating profile). Figure 16-1 shows an example of a predetermined modulation frequency. The modulation frequency is usually selected to be larger than 30 kHz (above the audio band) while small enough not to upset system timings (less than 0.8% of the clock frequency). SSC has been demonstrated to effectively reduce peak radiation levels, making EMC compliance easier to achieve.

To conserve the minimum period requirement for bus timing, the SSC clock is modulated between fnom and (1-δ)*fnom where fnom is the nominal frequency for a constant frequency clock. The"δ" specifies the total amount of spreading as a relative percentage of fnom. The modulation percentage is always a function of 1-δ and not 1+δ, as increasing the clock frequency above the rated speed of the processor may cause unpredictable operation.

Figure 16-1. Spread Spectrum Modulation Profile

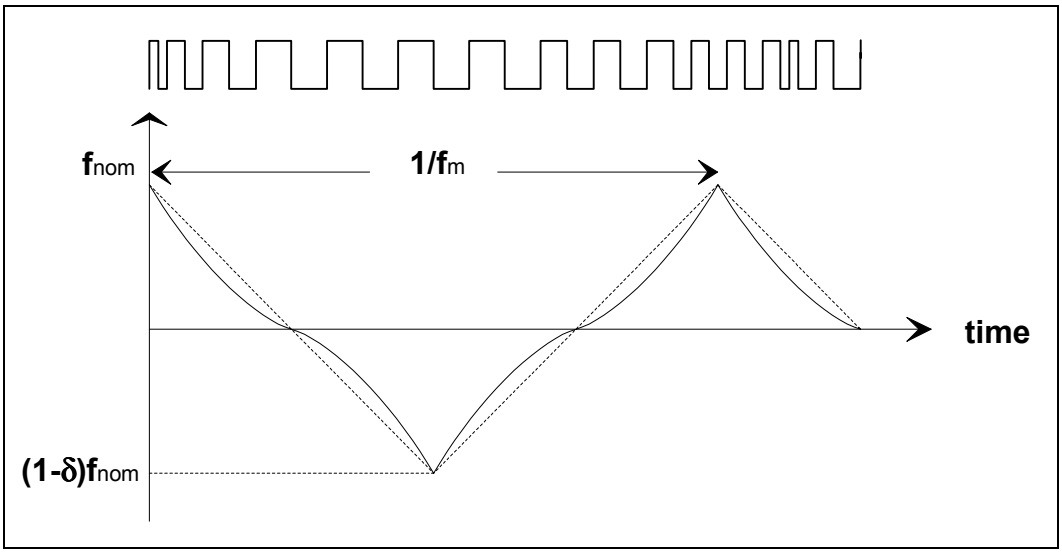
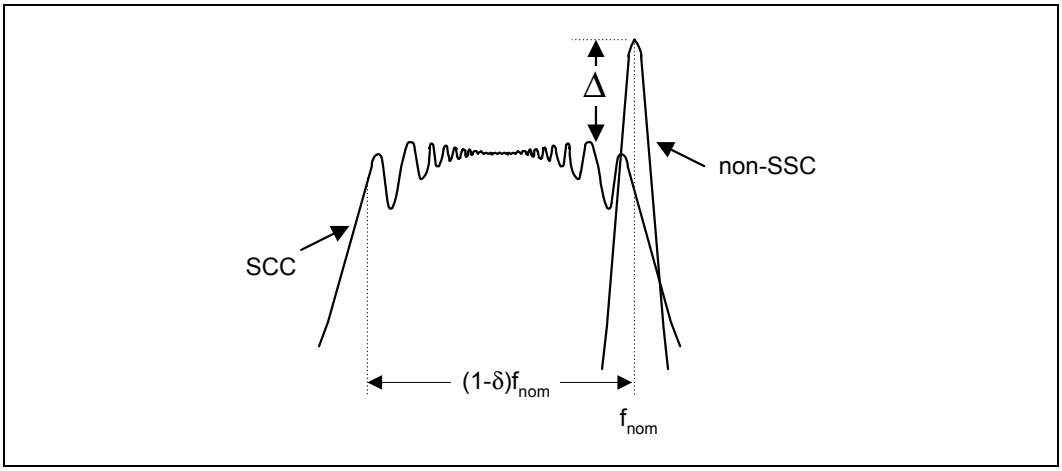


Figure 16-2. Impact of Spread Spectrum Clocking on Radiated Emissions

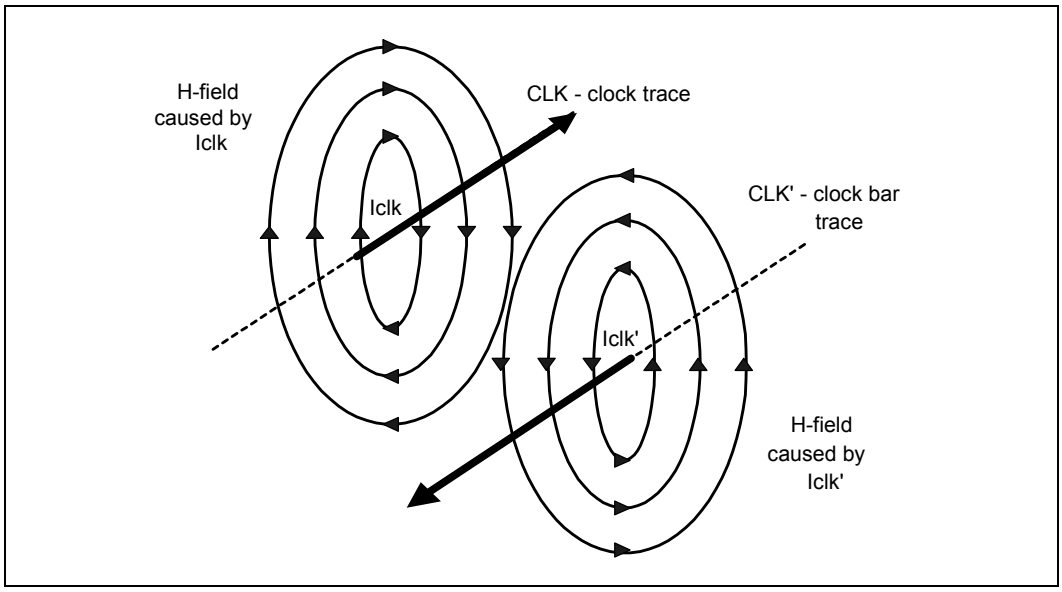


16.2.2 Differential Clocking

Differential clocking requires that the clock generator supply both clock and clock-bar traces. Clock-bar has equal and opposite current as the primary clock and is also 180 degrees out of phase. To maximize the benefit of differential clocking, both clock lines must be routed parallel to each other for their entire length. Devices connected to the clock must also be designed to accept both the clock and clock-bar signals.

EMI reduction due to differential clocking is caused by H-field cancellation. Since H-field orientation is generated by and is dependent upon current flow, two equal currents flowing in opposite directions and 180 degrees out of phase will have their H-fields cancelled (see Figure 16-3). Lower H-fields will result in reduced EMI radiation.

Figure 16-3. Cancellation of H-Fields through Inverse Currents



Differential clocking can also reduce the amount of noise coupled to other traces, which improves signal quality and reduces EMI. I/O signals are particularly important because they often leave the system chassis (serial and parallel ports, keyboards, mouse, etc.) and will radiate noise that has been induced onto them. A single-ended clock's return path is usually a reference plane, which is shared by other signals/traces. When noise is created on a single-ended clock, the noise will appear on the reference plane and may be coupled to I/O traces. A differential clock's return path is the clock-bar signal/trace, which is more isolated than the reference plane and minimizes potential I/O trace coupling.

For best results, the trace lengths and routing of the clock lines must be closely matched and spacing between the two traces should be kept as small as possible. This will minimize loop area and maximize H-field cancellation. In addition, the real and parasitic terminations of each signal of a differential pair should be the same. Also, the skew between the signal level transitions on the two lines must be small compared to the rise time of the level transitions.

Placing ground traces on the outside of the differential pair may further reduce emissions. Intermediate vias to ground may be needed to reduce the opportunity for re-radiation from the ground traces themselves. Distance between vias should be less than ¼ of a wavelength of the fifth harmonic of the processor core frequency.

16.2.3 PCI Bus Clock Control

Experimental data has indicated a reduction in EMI may be possible by disabling the clocks to unused (and therefore unterminated) PCI slots. CK409, the clock chip that has been specified and designed for this platform, supports individual control of the various PCI clocks. Designers have the option to enable or disable individual PCI clocks depending on their specific system configuration requirements. Refer to the *CK409 Clock Synthesizer Design Guidelines* for details on how to configure the PCI clocks.

16.2.4 EMI Test Capabilities

FCC regulations in the United States specify the maximum test frequency for products with clocks in excess of 1 GHz is five times the highest clock frequency or 40 GHz, which ever is lower. OEMs are advised to inquire into the capabilities of their preferred EMC test lab to ensure they are able to scan up to the required frequency range.

History indicates that processor performance and frequency double approximately every two years. With this in mind, it would be advisable to be prepared for the frequencies that will need to be scanned in the next few years.

Since the FCC rules ultimately require testing to 40 GHz, commercial test equipment has been developed which is capable of making measurements to that frequency. Although it will be some time before processors require testing at this frequency, it may be cheaper to upgrade to 40 GHz now rather than making several intermediate steps.

It is also possible to upgrade various parts at different times. The spectrum analyzer may be upgraded to 40 GHz today while only obtaining the necessary antennas to support the initial processor frequencies. As processor speed increases, the necessary antennas and cables could be purchased which would support testing to the higher levels. Cost flexibility in antenna selection is probably the greatest, as different antenna designs are necessary for different frequency ranges.

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Schematic Checklist 17

This chapter highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements the 848P chipset.

17.1 Processor Interface

17.1.1 Processor Connector / MCH Items

Checklist Items	Connections/Recommendations	Reason/Impact
ADS#	• Connect to ADS# pin on the MCH • No other termination required	• AGTL + Common Clock I/O Signal
BNR#	• Connect to BNR# pin on the MCH • No other termination required	• AGTL + Common Clock I/O Signal
BPRI#	• Connect to BPRI# pin on the MCH • No other termination required	• AGTL + Common Clock Input Signal
BR0#	• Connect to BREQ0# pin on the MCH • Terminate to VCC_CPU through a 200 Ω ± 5% resistor external pull-up	• The chipset contains on die termination for the BREQ0# signal. The processor does not contain on die termination for this particular AGTL + signal; thus, external termination is required only on the processor end. • AGTL + common clock I/O signal. Refer Section 5.1.6.4
RESET#	• Connect to the CPURST# on the MCH • Terminate to VCC_CPU through a 62 Ω ± 5% resistor near the processor	• The chipset contains on die termination for the HCPURST# signal. The processor does not contain on die termination for this particular AGTL + signal; thus, external termination is required only on the processor end. RESET# termination should equal the resistance value of on die AGTL + termination resistance (Rtt) value. • AGTL + common clock input signal. Refer Section 5.1.6.4
DBSY#	• Connect to DBSY# pin on the MCH • No other termination required	• AGTL + common clock I/O signal
DEFER#	• Connect to DEFER# pin on the MCH • No other termination required	• AGTL + common clock input signal
DBI[3:0]#	• Connect to DINV[3:0]# pin on the MCH • No other termination required	• AGTL + Source synch I/O signal

Checklist Items	Connections/Recommendations	Reason/Impact
DRDY#	• Connect to DRDY# pin on the MCH • No other termination required	• AGTL + common clock I/O signal
A[31:3]#	• Connect to HA[31:3]# pins on MCH • No other termination required	• Chipset does not support extended addressing over 4 GB, leave A[35:32]# unconnected • AGTL + source synch I/O signal
ADSTB[1:0]#	• Connect to HADSTB[1:0]# pins on MCH • No other termination required	• AGTL + source synch I/O signal
D[63:0]#	• Connect to HD[63:0]# pins on MCH • No other termination required	• AGTL + source synch I/O signal
DSTBP[3:0]#	• Connect to HDSTBP[3:0]# pins on MCH • No other termination required	• AGTL + source synch I/O signal
DSTBN[3:0]#	• Connect to HDSTBN[3:0]# pins on MCH • No other termination required	• AGTL + source synch I/O signal
HIT#	• Connect to HIT# pin on MCH • No other termination required	• AGTL +common clock I/O signal
HITM#	• Connect to HITM# pin on MCH • No other termination required	• AGTL + common clock I/O signal
LOCK#	• Connect to HLOCK# pin on MCH • No other termination required	• AGTL + common clock I/O signal
REQ[4:0]#	• Connect to HREQ[4:0]# pin on MCH • No other termination required	• AGTL + source Synch I/O Signal
TRDY#	• Connect to HTRDY# pin on MCH • No other termination required	• AGTL + common clock input signal
PROCHOT#	• Connect to PROCHOT# on VRD and MCH • Terminate to VCC_CPU through a 120 Ω –140 Ω ± 5% resistor on the processor	• Asynch GTL+ input/output signal. Refer to Section 5.1.6.7
RS[2:0]#	• Connect to RS[2:0]# pin on the MCH • No other termination required	• AGTL + common clock input signal

17.1.2 Processor Connector / Intel® ICH5 Items

Checklist Items	Connections/Recommendations	Reason/Impact
A20M#	• Connect to A20M# pin on the Intel® ICH5 • No other termination required	• Asynch GTL + input signal • Refer to Section 5.1.6.2, Table 5-9 and Table 5-4
FERR#	• Connect to FERR# pin on the ICH5 • Terminate to VCC_CPU through a 62 Ω ± 5% resistor near ICH5	• This output signal is not terminated on the processor. Termination is required on system board. • Asynch GTL + output signal. Refer to Section 5.1.6.1
IGNNE#	• Connect to IGNNE# pin on the ICH5 • No other termination required	• Asynch GTL + input signal. Refer to Section 5.1.6.2
INIT#	• Connect to INIT# pin on the ICH5 and to flash BIOS through voltage translation • Level shifting is required to meet the input logic levels of the flash BIOS	• Asynch GTL + input signal. Refer to Section 5.1.6.5
LINT[1:0]	• LINT0/INTR connects to INTR on ICH5 • LINT1/NMI connects to NMI on ICH5 • No termination is required	• Asynch GTL + input signal. Refer to Section 5.1.6.2
PWRGOOD	• Connects to CPUPWRGD/GPO49 in ICH5 • Terminate to VCC_CPU through a 300 Ω ± 5% resistor near processor	• Asynch GTL + input signal. Refer to Section 5.1.6.6
SLP#	• Connect to CPUSLP# on the ICH5 • No other termination required	• Asynch GTL + input signal. Refer to Section 5.1.6.2
SMI#	• Connect to SMI# pin on the ICH5 • No other termination required	• Asynch GTL + input signal. Refer to Section 5.1.6.2
STPCLK#	• Connect to STPCLK# pin on the ICH5 • No other termination required	• Asynch GTL + input signal. Refer to Section 5.1.6.2

17.1.3 Processor Connector Only Items

Checklist Items	Connections/Recommendations	Reason/Impact
A[35:32]#	• No Connection	• Chipset does not support extended addressing over 4 GB, leave A[35:32]# unconnected
AP[1:0]#	• No connection if unused	• Chipset does not support parity protection on the address bus • AGTL + common clock I/O signal
BCLK0	• Connect to CPU0 on the CK409 through a 33 Ω ± 5% resistor • Terminate to GND through a 49.9 Ω ± 1% resistor	• FSB clock signal • Refer to Section 5.1.6.18
BCLK1	• Connect to CPU0# on the CK409 through a 33 Ω ± 5% resistor • Terminate to GND through a 49.9 Ω ± 1% resistor	• FSB clock signal • Refer to Section 5.1.6.18
BOOTSELECT	• Connect to dual loadline select circuitry	
BPM[5:0]#	• Connect to BPM[5:0] on the ITP • Terminate to VCC_CPU through a 62 Ω ± 5% resistor place near the processor • Pull up to VCC_CPU using a 20 Ω – 1 kΩ resistor if no interposer support	• AGTL + common clock I/O signal
BINIT#	• No Connect if unused	• Chipset does not support this signal • AGTL + common clock I/O signal
BSEL0	• Connect to MCH's SEL0 pin • 1 kΩ pull-up to 3.3 V required at CK409 • MCH requires divider for 1.5 V tolerant inputs	• Refer Section 5.1.6.18
BSEL1	• Connect to MCH's SEL1 pin • 1 kΩ pull-up to 3.3 V required at CK409 • MCH requires divider for 1.5 V tolerant inputs	• Refer Section 5.1.6.18
COMP[1:0]	• Terminate to GND through a 61.9 Ω ± 1% resistor • Minimize the distance from termination resistor and processor pin	• Refer to Section 5.1.6.9
DBR#	• Connect to front panel HDR and switches • 8.2 kΩ pull-up to VCC Sus3_3 near Intel® ICH5 and connect to system reset logic (FP reset) • Can be left NC for no interposer support	
DP[3:0]#	• No connection if unused	• AGTL + common clock I/O signal

Checklist Items	Connections/Recommendations	Reason/Impact
IERR#	• No connection if unused • Terminate to VCC_CPU through a 62 Ω ± 5% resistor from the processor if used	• Asynch GTL + output signal Refer to Section 5.1.6.3
GTLREF[3:0]	• Connect 0.63*VCC_AVG divider to one of the 4 GTLREF pins. Others are NC. • Terminate to VCCP through a 200 Ω resistor. Decouple with a 0.1 µF or 1.0 µF at the voltage divider circuit through a 220 pF at the processor pin.	• Refer to Section 5.1.6.13
ITP_CLK0	• Connect to CPU1#on CK409 through a 33 Ω ± 5% resistor • Terminate to GND through a 49.9 Ω ± 1% resistor • Connect to NC for no interposer support	• FSB clock signal
ITP_CLK1	• Connect to CPU1# on CK409 through a 33 Ω ± 5% resistor • Terminate to GND through a 49.9 Ω ± 1% resistor • Connect to NC for no interposer support	• FSB clock signal
OPTIMIZED / COMPAT# (Intel® Pentium® 4 processor on 90 nm process) IMPSEL (Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process)	• No connection	
MCERR#	• No connection if unused	• Chipset does not support this signal
RSP#	• No connection if unused	• Chipset does not support this signal • AGTL + common clock input signal
SKTOCC#	• Connect to CPU_PRESENT# pin on the Port Angeles[1] • Depends on customer need	
TCK	• Connect to TCK on ITP • 27.4 Ω ± 1% pull-down to GND near ITP and 47Ω ± 5% pull-down to GND near processor for ITP-USB • Pull down to VSS using a 20 Ω – 1 kΩ resistor if no interposer support	• TAP input signal. Refer to appropriate processor Debug Port Design Guide.
TDI	• Connect to TDI on ITP • Terminate to VCC_CPU through a 150 Ω ± 5% resistor near processor • Pull up to VCC_CPU using a 20 Ω – 1 kΩ resistor if no interposer support	• TAP input signal. Refer to appropriate processor Debug Port Design Guide.

Checklist Items	Connections/Recommendations	Reason/Impact
TDO	• Connect to TDO on ITP • Terminate to VCC_CPU through 51 Ω ± 5% resistor near 47 Ω ± 5% series Res to ITP • Can be left NC if no interposer support	• TAP output signal
TESTHI[12:0]	• Terminate VCC_CPU through 62 Ω ± 5% resistor • TESHI[7:2] can be grouped together	• Refer to Section 5.1.6.8
THERMTRIP#	• Connect to THRMTRIP# pin on the ICH5 • Terminate to VCC_CPU through a 62 Ω ± 5% resistor near the ICH5	• Asynch GTL + output signal. Refer to Section 5.1.6.1
THERMDA	• Connect to REMOTE1+ on HECETA • Connect to external diode monitoring circuit if used	• Refer to Section 5.1.6.15
THERMDC	• Connect to REMOTE1- / NTESTIN on HECETA[2] • Connect to external diode monitoring circuit if used	• Refer to Section 5.1.6.15
TMS	• Connect to TMS pin on the ITP • 39.2 Ω ± 1% pull-up to VCC_CPU near ITP and 47 Ω ± 5% pull-up to VCC_CPU near processor for ITP-USB • Pull up to VCC_CPU using a 20 Ω – 1 kΩ resistor if no interposer support	• TAP input signal
TRST#	• Connect to TRST pin on the ITP connect • Terminate to GND through 510 Ω ~ 680 Ω ± 5% resistor • Pull down to VCC_CPU using a 20 Ω – 1 kΩ resistor if no interposer support	• TAP input signal
VCCA	• Connect to PLL supply filter	• Refer to Section 15.3.1.8
RESERVED	• All pins must remain unconnected	• Refer to Section 5.1.6.11
VCCIOPLL	• Connect to PLL supply filter	• Refer to Section 15.3.1.8
VCC_SENSE	• Connect to VR control silicon if used	• Refer to Figure 15-11
VCCVID	• Connect to processor VREGn	• Refer to the Section 15.3.1.7
VID[5:0]	• Connect to VR control silicon and possibly hardware monitor circuitry • Requires 1 kΩ pull-up to 3.3 V	• Refer to Section 5.1.6.14
VIDPWRGD	• Connect to power good output of the 1.2 V linear supply w/ 2.43 kΩ pull-up	•
VSSA	• Connect to PLL supply filter	• Refer to Section 15.3.1.8
VSS_SENSE	• Connect to VR control silicon if used	• Refer to Figure 15-11

NOTE:
1. Port Angeles is an Intel enabled specification for building an integrated super I/O and Glue Logic chip. At this time, National Semiconductor Corporation and SMSC Corporation make IC devices that implement this specification. For National Semiconductor Corporation, the part number is PC87372. For SMSC Corporation, the part number is LPC47M172.
2. Heceta is an Intel enabled specification for building an integrated Glue Logic chip. At this time, National Semiconductor Corporation, SMSC Corporation, and ADI Corporation make IC devices that implement the Heceta 6 specification. For National Semiconductor, the part number is LM85. For SMSC, the part number is EMC6D102. For ADI, the part number is ADM1027ARQ.

17.2 MCH SD Interface

17.2.1 MCH / FSB Items

Checklist Items	Connections/Recommendations	Reason/Impact
ADS#	• Connect to ADS# pin on the processor	
BNR#	• Connect to BNR# pin on the processor	
BPRI#	• Connect to BPRI# pin on the processor	
BREQ0#	• Connect to BR0# pin on the processor • Terminate to VCCP through a 200 Ω ± 5% resistor near the processor	• Refer to Section 5.1.6.4
CPURST#	• Connect to the RESET# on the processor • Terminate to VCCP through a 62 Ω ± 5% resistor near the processor	• Refer to Section 5.1.6.4
DBSY#	• Connect to DBSY# pin on the processor	
DEFER#	• Connect to DEFER# pin on the processor	
DINV[3:0]#	• Connect to DBI[3:0]# pin on the processor	
DRDY#	• Connect to DRDY# pin on the processor	
HA[31:3]#	• Connect to A[31:3]# pins on processor	
HADSTB[1:0]#	• Connect to ADSTB[1:0]# pins on processor	
HD[63:0]#	• Connect to D[63:0]# pins on processor	
HDSTBP[3:0]#	• Connect to DSTBP[3:0]# pins on processor	
HDSTBN[3:0]#	• Connect to DSTBN[3:0]# pins on processor	
HIT#	• Connect to HIT# pin on processor	
HITM#	• Connect to HITM# pin on processor	
HLOCK#	• Connect to LOCK# pin on processor	
HREQ[4:0]#	• Connect to REQ[4:0]# pin on processor	
HTRDY#	• Connect to TRDY# pin on processor	
PROCHOT#	• Connect to PROCHOT# on VRD and processor • Pull-up to VCCP through a 120 Ω ± 5% resistor	• Refer to Section 5.1.6.7
RS[2:0]#	• Connect to RS[2:0]# pin on the processor	

17.2.2 MCH / FSB Only Items

Checklist Items	Connections/Recommendations	Reason/Impact
HCLKN	• Connect to CPU2# in CK409 • Connect to a series 27 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor	
HCLKP	• Connect to CPU2 in CK409 • Connect to a series 27 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor	
HDVREF	• Connect voltage divider through 200 Ω pull-up to MCH_VTT and to GND through a 169 Ω resistor. Decouple with a 0.1 µF or a 220 pF capacitor as close to MCH as possible.	• Refer to Section 5.1.6.13
HDRCOMP	• Pull-down to GND through a 20 Ω ± 1% resistor	• Refer to Section 5.1.6.16
HDSWING	• Connect voltage divider circuit to MCH_VTT through a 301 Ω ± 1% pull-up resistor and to GND through a 102 Ω ± 1% pull-down resistor • Decouple voltage divider with a 0.01 µF at the pin of the MCH	• Refer to Section 5.1.6.17
PWROK	• Connect PWRGD_3V on Port Angeles[1]	
BSEL[1:0]	• For a voltage divider with the BSEL[1:0] to the processor, use a 2 kΩ resistor from power to the BSEL line and a 2.49 kΩ resistor from BSEL to GND	• Refer to Section 5.1.6.18

NOTE:
1. Port Angeles is an Intel enabled specification for building an integrated super I/O and Glue Logic chip. At this time, National Semiconductor Corporation and SMSC Corporation make IC devices that implement this specification. For National Semiconductor Corporation, the part number is PC87372. For SMSC Corporation, the part number is LPC47M172.

17.2.3 MCH / DDR Channel A Items

Checklist Items	Connections/Recommendations	Reason/Impact
SCMDCLK_A0	• Connect to CK0P in DIMM0	• Refer to Section 6.2.2
SCMDCLK_A0#	• Connect to CK0N in DIMM0	• Refer to Section 6.2.2
SCMDCLK_A1	• Connect to CK1 in DIMM0	• Refer to Section 6.2.2
SCMDCLK_A1#	• Connect to CK1# in DIMM0	• Refer to Section 6.2.2
SCMDCLK_A2	• Connect to CK2 in DIMM0	• Refer to Section 6.2.2
SCMDCLK_A2#	• Connect to CK2# in DIMM0	• Refer to Section 6.2.2
SCMDCLK_A3	• Connect to CK0P in DIMM1	• Refer to Section 6.2.2
SCMDCLK_A3#	• Connect to CK0N in DIMM1	• Refer to Section 6.2.2
SCMDCLK_A4	• Connect to CK1 in DIMM1	• Refer to Section 6.2.2
SCMDCLK_A4#	• Connect to CK1# in DIMM1	• Refer to Section 6.2.2
SCMDCLK_A5	• Connect to CK2 in DIMM1	• Refer to Section 6.2.2
SCMDCLK_A5#	• Connect to CK2# in DIMM1	• Refer to Section 6.2.2
SCS_A[3:0]#	• Connect to CS[1:0]# on DIMM0 and DIMM1 • Terminate to VTT through a 47 Ω ± 5% resistor	• Refer to Section 6.2.2
SMAA_A[12:0]	• Connect to A[12:0] on DIMM0 • Connect to A[12:6,0] on DIMM1 • Terminate to VTT through a parallel of 47 Ω ± 5% resistor	• Refer to Section 6.2.3
SMAB_A[5:1]	• Connect to A[5:1] on DIMM1 • Terminate to VTT through a parallel of 47 Ω ± 5% resistor	• Refer to Section 6.2.3
SBA_A[1:0]	• Connect to BA[1:0] pin on both DIMM0 and DIMM1 • Terminate to VTT through a 47 Ω ± 5% resistor	• Follow DDR address/command signal routing topology guidelines • Refer to Section 6.2.3
SRAS_A#	• Connect to RAS# pin on both DIMM0 and DIMM1 • Terminate to VTT through a 47 Ω ± 5% resistor	• Follow DDR address/command signal routing topology guidelines • Refer to Section 6.2.3
SCAS_A#	• Connect to CAS# pin on both DIMM0 and DIMM1 • Terminate to VTT through a 47 Ω ± 5% resistor	• Follow DDR address/command signal routing topology guidelines • Refer to Section 6.2.3
SWE_A#	• Connect to WE# pin on each DIMM0 and DIMM1 • Terminate to VTT through a 47 Ω ± 5% resistor	• Follow DDR address/command signal routing topology guidelines • Refer to Section 6.2.3
SDQ_A[63:0]	• Connect to SDQ[63:0] on both DIMM0 and DIMM1 • Terminate to VTT through a 56Ω ± 5% resistor	• Follow DDR data signal routing topology guidelines • Refer to Section 6.2.4
SDQS_A[7:0]	• Connect to SDQS[7:0] pins on both DIMM0 and DIMM1 • Terminate to VTT through a 56 Ω ± 5% resistor	• Follow DDR data signal routing topology guidelines • Refer to Section 6.2.4
SCKE_A[3:0]	• Connect to CKE[1:0] on DIMM0 and DIMM1 • Terminate to VTT through a 47 Ω ± 5% resistor	• Refer to Section 6.2.5
SMVREF_A	• Connect to chipset filters • Terminate to ground through a 2.2 µF ± 20% capacitor and 0.1 µF ± 20% capacitor	• Refer to Section 6.3

Checklist Items	Connections/Recommendations	Reason/Impact
SMVREF_B	• Connect to chipset filters • Terminate to ground through a 2.2 µF ± 20% capacitor and a 0.1 µF ± 20% capacitor	• Refer to Section 6.3
SMXRCOMP	• 42.2 Ω ± 1% pulled to VDD (2.6 V), place resistors within 1.0 inch of the MCH and pull to GND through a 42.2 ± 1% resistor • Decouple 2.6 V with a 2.2 µF capacitor locally	• Refer to Section 6.4
SMXRCOMP VOH and VOL	• R2 = 3.112*R1, recommend R1 = 10 kΩ ± 1%	• Refer to Section 6.4
SMYRCOMP	• 42.2 Ω ± 1% pulled to VDD (2.6 V), place resistors within 1.0 inch of the MCH and 42.2 Ω ± 1% pull to GND • Decouple 2.6 V with a 2.2 µF capacitor locally	• Refer to Section 6.4
SMYRCOMP VOH and VOL	• R2 = 3.112*R1, recommend R1 = 10 kΩ ± 1%	• Refer to Section 6.4

17.2.4 MCH / AGP Items

Checklist Items[1]	Connections/Recommendations	Reason/Impact
GADSTBF[1:0]	• Connect to GAD_STB[1:0] in AGP	• Refer to Section 8.2.2
GADSTBS[1:0]	• Connect to GAD_STB[1:0]# in AGP	
GAD[31:0]	• Connect to GAD[31:0] in AGP	
GC#/BE[3:0]	• Connect toGC_BE[3:0]# in AGP	
GDEVSEL	• Connect to GDEVSEL# in AGP	
GFRAME	• Connect to GFRAME# in AGP	
GGNT	• Connect to GGNT# in AGP	
GIRDY	• Connect to GIRDY# in AGP	
GPAR	• Connect to GPAR in AGP	
DBI_HI	• Connect to DBI_HI/PIPE# in AGP	
DBI_LO	• Connect to GBI_LO in AGP	
GREQ	• Connect to GREQ# in AGP	
GSTOP	• Connect to GSTOP# in AGP	
GTRDY	• Connect to GTRDY# in AGP	
GRBF	• Connect to RBF# in AGP	
GSBA[7:0]#	• Connect to SBA[7:0] in AGP	
GSBSTBF	• Connect to SB_STB in AGP	
GSBSTBS	• Connect to SB_STB# AGP	
GST[2:0]	• Connect to ST[2:0] in AGP	
GWBF	• Connect to WBF# in AGP	

NOTE:
1. AGP 3.0 signal names are used for the MCH signals listed in this column. For the corresponding AGP 2.0 signal name, refer to the *Intel® 848P Chipset Datasheet*.

17.2.5 MCH / AGP Only Items

Checklist Items	Connections/Recommendations	Reason/Impact
GRCOMP	• Pulled up to 1.5 V core through a 43.2 Ω ± 1% resistor on chipset decoupling	
GSWING	• Connects from the MCH to a resistor divider network of the AGP SWING/VREF reference circuit	• Section 8.2.4.5 and Figure 8-4 for more detailed information
GVREF	• Connect to the AGP Ref pin of the AGP connector and to a resistor divider network of the AGP SWING/VREF reference circuit	• Section 8.2.4.4 and Figure 8-4 for more detailed information
GCLKIN	• Connect to 3V662/pin#26 on CK409 through a 33 Ω ± 5% resistor	

17.2.6 MCH / Hub Interface Items

Checklist Items	Connections/Recommendations	Reason/Impact
HI[10:0]	• Connect to HI[10:0] on Intel® ICH5	• Refer to Section 7.1
HISTRS	• Connect to HI_STBS on ICH5	• Refer to Section 7.1
HISTRF	• Connect to HI_STBF on ICH5	• Refer to Section 7.1
HI_VREF	• Connect to MCH REF of Hub connector voltage divider circuit on chipset decoupling	• Refer to Section 7.1.2
HI_SWING	• Connect to voltage divider circuit on chipset decoupling	• Refer to Section 7.1.2
HI_RCOMP	• Pull up to 1.5 V core through 51.1Ω ± 1% resistor on decoupling	

17.2.7 MCH / CSA Items

Checklist Items	Connections/Recommendations	Reason/Impact
CI[10:0]	• CI[10:0] connect to CI[0:10] on Intel® 82547EI GbE LAN controller	
CISTRF	• Connect to CI_STBF on Intel 82547EI GbE LAN controller	
CISTRS	• Connect to CI_STBS on Intel 82547EI GbE LAN controller	
CI_RCOMP	• Pull up to 1.5 V core through a 52.3 Ω ± 1% resistor	
CI_SWING	• Connect to SWING generation circuit with 0.1 µF decoupling capacitor at MCH pin	
CI_VREF	• Connect to VREF generation circuit with 0.1 µF decoupling capacitor at MCH pin	

17.3 MCH / POWER Items

Checklist Items	Connections/Recommendations	Reason/Impact
VTT	• Connect to output of MCH_VTT regulator	
VCC_DDR	• Connect to output of 2.6 V VREG	
VCC_DAC	• Connect to 3.3 V rail	
VCCA_AGP	• Connect to output of VCCA_AGP filter	
VCCA_FSB	• Connect to output of VCCA_FSB filter	• Refer to Section 15.3.4.2
VCCA_DPLL	• Connect directly to ground	• Refer to Section 15.3.4.2
VCCA_DAC	• Connect directly to ground	• Refer to Section 15.3.4.2
VCCA_DDR	• Connect to output of VCCA_DDR filter	• Refer to Section 15.3.4.2
VCC	• Connect to 1.5 V core through plane filter	• Refer to Section 15.3.4.1
VCC_AGP	• Connect to 1.5 V core	
VSSA_DAC	• Connect directly to ground	

17.4 MCH / Miscellaneous Items

Checklist Items	Connections/Recommendations	Reason/Impact
RSTIN#	• Connect to RCIRST# on the Intel® ICH5 through a 0 Ω resistor and tie to GND through a 10 pF ± 5% capacitor	
RESERVED	• No Connect	
TESTP[1:0]	• No Connect	
TESTP[3:2]	• Route to test point for XOR chain testing, else connect to GND	
TESTP[16:4]	• No Connect	•
TESTP[24:17]	• Connect directly to GND	•
TESTP[139:25]	• No Connect	•
TESTP[147:140]	• Connect directly to GND	•

17.5 Clock CK409 Interface

Checklist Items	Connections/Recommendations	Reason/Impact
3V66_0 (Pin 22)	• Connect to 66 MHz in of CSA device, MCH, or Intel® ICH5, AGP • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor	• CLK66 clock group
3V66_1 (Pin 23)	• Connect to 66 MHz in of CSA device, MCH • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor	• CLK66 clock group
3V66_2 (Pin 26)	• Connect to 6 6 MHz in of CSA device, MCH, or ICH, AGP • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor	• CLK66 clock group
3V66_3 (Pin 27)	• Connect to 66 MHz in of CSA device, MCH, or ICH, AGP • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor	• CLK66 clock group
3V66_4 / VCH (Pin 29)	• Connect to 66 MHz in of CSA device, MCH, or ICH, AGP • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor	• CLK66 clock group
CPU0 (Pin 41)	• Connect to processor, MCH, or ITP • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor	• Host clock group
CPU0# (Pin 40)	• Connect to processor, MCH, or ITP • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor	• Host clock group
CPU1 (Pin 44)	• Connect to processor, MCH, or ITP • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor	• Host clock group
CPU1# (Pin 43)	• Connect to processor, MCH, or ITP • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor	• Host clock group
CPU2 (Pin 47)	• Connect to processor, MCH, or ITP • connect to a series 33 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor	• Host clock group
CPU2# (Pin 46)	• Connect to processor, MCH, or ITP • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor	• Host clock group

Checklist Items	Connections/Recommendations	Reason/Impact
CPU_STOP# (Pin 50)	• Pull-up to VCC3_CLK through a 1 kΩ ± 5% resistor	• Host Clock Group
FS_B / FS_A (Pin 56 / Pin 51)	• Connect to Host clock frequency select circuit. See the *CK409 Clock Synthesizer/ Driver Specification* for more details.	
REF0 (Pin 2)	• Connect to 14 MHz input Buffer of ICH5 or Audio device • Connect through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor	
REF1 (Pin 1)	• Connect to 14 MHz input Buffer of ICH5 or Audio device • Connect through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor	
IREF (Pin 52)	• Terminate to GND through a 475 Ω ± 1% resistor	
VSS_IREF (Pin 53)	• Terminate to GND of IREF resistor	
PCI0 (Pin 12)	• Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or ICH5 through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% terminate to GND through a 10 pF ± 5% capacitor.	
PCI1 (Pin 13)	• Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or ICH5 through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% terminate to GND through a 10 pF ± 5% capacitor.	
PCI2 (Pin 14)	• Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or ICH5 through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% terminate to GND through a 10 pF ± 5% capacitor.	
PCI3 (Pin 15)	• Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or ICH5 through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% terminate to GND through a 10 pF ± 5% capacitor.	
PCI4 (Pin 18)	• Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or ICH5 through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% terminate to GND through a 10 pF ± 5% capacitor.	
PCI5 (Pin 19	• Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or ICH5 through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% terminate to GND through a 10 pF ± 5% capacitor.	

Checklist Items	Connections/Recommendations	Reason/Impact
PCI6 (Pin 20)	• Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or ICH5 through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% terminate to GND through a 10 pF ± 5% capacitor.	
PCIF0 (Pin 7)	• Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or ICH5 through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% terminate to GND through a 10 pF ± 5% capacitor.	
PCIF1 (Pin 8)	• Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or ICH5 through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% terminate to GND through a 10 pF ± 5% capacitor.	
PCIF2 (Pin 9)	• Connect to 33 MHz input buffer of PCI devices, PCI connector, BIOS chip, or ICH5 through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% terminate to GND through a 10 pF ± 5% capacitor.	
PCI_STOP# (Pin 49)	• If not used pull up to VCC3 through 1 kΩ. Otherwise, see the *CK409 Clock Synthesizer/Driver Specification* for more details.	• PCICLK Group
PWRDWN# (Pin 21)	• Pull-up to VCC3 through a 1 kΩ resistor	
SCLK (Pin 28)	• Connect to SMBus CLK	
SDATA (Pin 30)	• Connect to SMBus Data	
SRC (Pin 38)	• Connect to Serial ATA clock input to ICH5 through a series 33.2 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor	
SRC# (Pin 37)	• Connect to Serial ATA clock input to ICH5 through to a series 33.2 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor	
USB_48Mhz (Pin 31)	• Connect to ICH_USB clock input through a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor	
VDD (Pin [3,10,16, 24,42,48])	• Connect through a 300 Ω (100 MHz) FB to VCC3 with one 10 µF bulk decoupling capacitor and one 0.1 µF capacitor for each VDD pin	
VDD48 (Pin 34	• Terminate to VCC3_CLK through a 10 Ω ± 5% resistor and terminate to GND through one 4.7 µF capacitor and one 0.1 µF capacitor	

Checklist Items	Connections/Recommendations	Reason/Impact
VDDA (Pin 55)	• Connect through a 300 Ω (100 MHz) FB to VCC3 with one 10 µF bulk decoupling capacitor and one 0.1 µF capacitor for each VDD pin	
VSS (Pin [6,11,17,39, 25,33,45, 54])	• Terminate to GND	
VTT_PWRGD# (Pin 35)	• Connect to PWRGD circuitry. See the *CK409 Clock Synthesizer/Driver Specification* for more details. • Connect to VCC3_CLK through a 10 Ω ± 5% resistor	
XTAL_IN (Pin 4)	• Connect to 14.318 MHz Crystal. See the *CK409 Clock Synthesizer/Driver Specification* for decoupling capacitor calculation.	• Capacitor values may vary slightly from manufacturer to manufacturer
XTAL_OUT (Pin 5)	• Connect to 14.318 MHz Crystal. See the *CK409 Clock Synthesizer/Driver Specification* for decoupling capacitor calculation.	• Capacitor values may vary slightly from manufacturer to manufacturer

17.6 AGP 4X/8X Interface

17.6.1 AGP Connector / MCH Items

Checklist Items	Connections/Recommendations[1]	Reason/Impact
GAD_STB[1:0]	• Connect to GADSTBF[1:0] on MCH	• Refer to Section 8.2.2
GAD_STB[1:0]#	• Connect to GADSTBS[1:0] on MCH	
GAD[31:0]	• Connect to GAD[31:0] on MCH	
GC_BE[3:0]#	• Connect to GC#/BE[3:0] on MCH	
GDEVSEL#	• Connect to GDEVSEL on MCH	
GFRAME#	• Connect to GFRAME on MCH	
GGNT#	• Connect to GGNT on MCH	
GIRDY#	• Connect to GIRDY on MCH	
GPAR	• Connect to GPAR on MCH	
PIPE# / DBI_HI	• Connect to DBI_HI on MCH	
GREQ#	• Connect to GREQ on MCH	
GSTOP#	• Connect to GSTOP on MCH	
GTRDY#	• Connect to GTRDY on MCH	
RBF#	• Connect to GRBF on MCH	
SBA[7:0]	• Connect to GSBA[7:0]# on MCH	
SB_STB	• Connect to GSBSTBF on MCH	
SB_STB#	• Connect to GSBSTBS on MCH	
ST[2:0]	• Connect to GST[2:0] on MCH	
WBF#	• Connect GWBF on MCH	
VREFCG	• Connect to AGPREF_MCH of the AGP SWING/VREF and the resistor divider of the GC_DET# Reference Circuit	• Refer to Section 8.2.4.4
GC_DET	• Connect to the input of the GC_DET# on AGP SWING/VREF reference schematics	• Pulled low by an AGP 3.0 graphics card, and left floating by an AGP 2.0 graphics card • Refer to Section 8.2.4.2 and Figure 8-2 for more detailed information
MB_DET	• Connect to GND	

NOTE:
1. AGP 3.0 signal names are used for the MCH signals listed in this column. For the corresponding AGP 2.0 signal name, refer to the *Intel® 848P Chipset Datasheet*.

17.6.2 AGP Connector Only Items

Checklist Items	Connections/Recommendations	Reason/Impact
INTA#	• Connect P_INTA# on PCI	
INTB#	• Connect P_INTB# on PCI	
3.3VAUX	• Connect to V_3P3_PCI on PCI VAUX	
VCC3	• Connect to VCC3	
12V	• Connect to +12 V	
VCC	• Connect to VCC	
VDDQ	• Connect to V_1P5_CORE on 1.5 V core	
AGPCLK	• Connect to a 66 MHz clock of the CK409	
GPERR#	• Connect to the input of the G_PERR_PU# on AGP SWING/VREF reference circuit	• See Section 8.2.4.1 and Figure 8-2 for more detailed information
GSERR#	• Pull up to 1.5 V core through a 6.8 kΩ ± 5%	
OVRCNT	• No Connect	
PCIRST	• Connect to reset on each PCI slot (P_RST_SLOTS#)	
PME#	• Connect to P_PME# on PCI	
TYPEDET#	• No Connect	• Signal not required due to the use of 1.5 V connector
USB+	• No Connect	• 5 V tolerant
USB-	• No Connect	• 5 V tolerant
RSVD	• No Connect	
VREFGC	• No Connect	

17.7 DDR Interface

17.7.1 DDR Channel A DIMM0 and DIMM1 / MCH Items

Checklist Items	Connections/Recommendations	Reason/Impact
CK0P	• DIMM0: Connect to SCMDCLK_A0 • DIMM1: Connect to SCMDCLK_A3	• Refer to Section 6.2.2
CK0N	• DIMM0: Connect to SCMDCLK_A0# • DIMM1: Connect to SCMDCLK_A3#	• Refer to Section 6.2.2
CK1	• DIMM0: Connect to SCMDCLK_A1 • DIMM1: Connect to SCMDCLK_A4	• Refer to Section 6.2.2
CK1#	• DIMM0: Connect to SCMDCLK_A1# • DIMM1: Connect to SCMDCLK_A4#	• Refer to Section 6.2.2
CK2	• DIMM0: Connect to SCMDCLK_A2 • DIMM1: Connect to SCMDCLK_A5	• Refer to Section 6.2.2
CK2#	• DIMM0: Connect to SCMDCLK_A2# • DIMM1: Connect to SCMDCLK_A5#	• Refer to Section 6.2.2
CS[1:0]#	• DIMM0 and DIMM1: Connect to SCS_A[3:0]# • Terminate to VTT through a 47 Ω ± 5% resistor	• Refer to Section 6.2.5
A[12:0]	• DIMM0: Connect to SMAA_A[12:0] • DIMM1: A[5:1] connect to SMAB_A[5:1] and A[12:6,0] connect to SMAA_A[12:6,0] • Terminate to VTT through a parallel of 47 Ω ± 5% resistor	• Refer to Section 6.2.3and Section 6.2.6
BA[1:0]	• DIMM0 and DIMM1: Connect to SBA_A[1:0] • Terminate to VTT through a 47 Ω ± 5% resistor	• Follow DDR address/ command signal routing topology guidelines • Refer to Section 6.2.3
RAS#	• DIMM0 and DIMM1: Connect to SRAS_A# • Terminate to VTT through a 47 Ω ± 5% resistor	• Follow DDR address/ command signal routing topology guidelines • Refer to Section 6.2.3
CAS#	• DIMM0 and DIMM1: Connect to SCAS_A# • Terminate to VTT through a 47 Ω ± 5% resistor	• Follow DDR address/ command signal routing topology guidelines • refer to Section 6.2.3
WE#	• DIMM0 and DIMM1: Connect to SWE_A# • Terminate to VTT through a 47 Ω ± 5% resistor	• Follow DDR address/ command signal routing topology guidelines • Refer to Section 6.2.3
DQ[63:0]	• DIMM0 and DIMM1: Connect to SDQ_A[63:0] • Terminate to VTT through a 56 Ω ± 5% resistor	• Follow DDR data signal routing topology guidelines • Refer to Section 6.2.4
DM[7:0]	• Connect directly to GND	• Not used

Checklist Items	Connections/Recommendations	Reason/Impact
DQS[7:0]	• DIMM0 and DIMM1: Connect to SDQS_A[7:0] • Terminate to VTT through a 56 Ω ± 5% resistor	• Follow DDR data signal routing topology guidelines • Refer to Section 6.2.4
CKE[1:0]	• DIMM0 and DIMM1: Connect to SCKE_A[3:0] • Terminate to VTT through a 47 Ω ± 5% resistor	• Refer to Section 6.2.5
DIMM VREF		• Refer to Section 6.3

17.7.2 DDR Channel A DIMM0 and DIMM1 Only Items

Checklist Items	Connections/Recommendations	Reason/Impact
A13 / NC	• No Connect for both DIMM0 and DIMM1	
DM8 / SDQS17	• No Connect for both DIMM0 and DIMM1	
DQS8	• No Connect for both DIMM0 and DIMM1	
CB[7:0]	• No Connect for both DIMM0 and DIMM1	
BA2	• No Connect for both DIMM0 and DIMM1	
SA[2:0]	• DIMM0: Connect to GND • DIMM1: Connect SA[2:1] to GND, and Connect SA0 to 2.6 V	
WP / NC	• No Connect for both DIMM0 and DIMM1	
RESET#	• No Connect for both DIMM0 and DIMM1	
FETEN / NC	• No Connect for both DIMM0 and DIMM1	
SDA	• Connect to Port Angeles[1], CNR60, and CK409	
SCL	• Connect to SMB_CLK_MAIN	
VDDSPD	• Connect to power (from a minimum of 2.3 V to a maximum of 3.6 V) • Strongly recommend connecting to 2.6 V core	
VDDID	• No Connect for both DIMM0 and DIMM1	
VDD	• Connect to 2.6 V on both DIMM0 and DIMM1	
VDDQ	• Connect to 2.6 V on both DIMM0 and DIMM1	
VSS	• Connect to GND on both DIMM0 and DIMM1	
NC	• No Connect for both DIMM0 and DIMM1	
CS3#	• No Connect for both DIMM0 and DIMM1	
CS2#	• No Connect for both DIMM0 and DIMM1	

NOTE:
1. Port Angeles is an Intel enabled specification for building an integrated super I/O and Glue Logic chip. At this time, National Semiconductor Corporation and SMSC Corporation make IC devices that implement this specification. For National Semiconductor Corporation, the part number is PC87372. For SMSC Corporation, the part number is LPC47M172.

17.8 Intel® ICH5 Interface

17.8.1 Intel® ICH5 / PCI Items

Checklist Items	Connections/Recommendations	Reason/Impact
PERR#, SERR#, PLOCK#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#	• These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to VCC3_3 or a 2.7 kΩ pull-up resistor to VCC5.	• See PCI 2.3 Component Specification pull-up recommendations for VCC3_3 and VCC5
REQ[0:4]#	• These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to VCC3_3 or a 2.7 kΩ pull-up resistor to VCC5.	• See PCI 2.3 Component Specification pull-up recommendations for VCC3_3 and VCC5
GPIO0/REQA#	• These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to VCC3_3 or a 2.7 kΩ pull-up resistor to VCC5.	• See PCI 2.3 Component Specification pull-up recommendations for VCC3_3 and VCC5
GPIO1/REQB#/ REQ5#	• These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to VCC3_3 or a 2.7 kΩ pull-up resistor to VCC5.	• See PCI 2.3 Component Specification pull-up recommendations for VCC3_3 and VCC5
PCIRST#	• The PCIRST# signal should be buffered to form the IDERST# signal 33 Ω series resistor to IDE connectors.	• Improves Signal Integrity
PCIGNT[4:0]#	• No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented, they must be pulled up to VCC3_3.	• These signals are actively driven by the Intel® ICH5
PME#	• No extra pull-up resistor	• This signal has integrated pull-up of 18 kΩ to 42 kΩ
GNTA# /GPIO16, GNTB#/ GNT5#/ GPIO17	• No extra pull-up needed	• These signals have integrated pull-ups of 24 kΩ • GNTA# has an added strap function of “top block swap”. The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull-down resistor can be added to manually enable the function. • GNTB# has a reserved strap function. This signal should not be pulled low.
IDSEL (on PCI Connector)	• If connected, this signal must have a 300 Ω to 900 Ω series termination resistor	

17.8.2 Intel® ICH5 / Interrupt Items

Checklist Items	Connections/Recommendations	Reason/Impact
PIRQ[D:A]#	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3_3.	• In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15. Each PIRQx# line has a separate Route Control Register (see the *Intel® 82801EB I/O Controller Hub 5 (ICH5) and Intel® 82801ER I/O Controller Hub 5R (ICH5R) Datasheet*). • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19.
PIRQ[H:E]#/ GPIO[5:2]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3_3.	• In Non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described. Each PIRQx# line has a separate Route Control Register (See the *Intel® 82801EB I/O Controller Hub 5 (ICH5) and Intel® 82801ER I/O Controller Hub 5R (ICH5R) Datasheet*). • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23.
SERIRQ	• External weak (8.2 kΩ) pull-up resistor to VCC3_3 is recommended	• Open drain signal

17.8.3 Intel® ICH5 / IDE Items

Checklist Items	Connections/Recommendations	Reason/Impact
PDD[15:0], SDD[15:0]	• Connect to 2X20HDR_20 • No extra series termination resistors or other pull-ups/pull-downs are required • PDD7/SDD7 does not require a 10 kΩ pull-down resistor • Refer to ATA ATAPI-6 specification	• These signals have integrated series resistors **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 21 Ω to 75 Ω • Refer to Section 10.3.3 and Section 10.3.4
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	• Connect to 2X20HDR_20 • No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	• These signals have integrated series resistors **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 21 Ω to 75 Ω
PDDREQ, SDDREQ	• Connect to 2X20HDR_20 • No extra series termination resistors • No pull-down resistors needed	• These signals have integrated series resistors in the Intel® ICH5 • These signals have integrated pull-down resistors in the ICH5
PIORDY, SIORDY	• Connect to 2X20HDR_20 • No extra series termination resistors • Pull-up to VCC3_3 via a 4.7 kΩ resistor	• These signals have integrated series resistors in the ICH5
IRQ14, IRQ15	• Connect to 2X20HDR_20 • Recommend 8.2 kΩ to 10 kΩ pull-up resistors to VCC3_3 • No extra series termination resistors	• Open drain outputs from drive
IDERST#	• The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal.	
Cable Detect	Host Side/Device Side Detection (recommended method): • Connect IDE pin PDIAG#/CBLID to an ICH5 GPIO pin. Connect a 10 kΩ resistor to VSS on the signal line. Device Side Detection: • Connect a 0.047 µF capacitor from IDE pin PDIAG#/CBLID to VSS. No ICH5 connection.	• The 10 kΩ resistor to VSS prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. **NOTE:** All Ultra DMA drives supporting modes greater than Mode 2 will have the capability to detect cables.

17.8.4 Intel® ICH5 / SATA Items

Checklist Items	Recommendations	Reason/Impact
SATALED#	• Recommend weak external pull-up to Vcc3_3	• Open drain signal. Refer to Section 10.4.6
SATARBIASP	• 24.9 Ω ±1% connected to ground	
SATARBIASN	• Connected to the same 24.9 Ω ± 1% resistor to ground as SATARBIASP	
SATA[1:0]TXP/N	• Connect to TXP/N • No extra series termination resistors or other pull-ups/pull-downs are required	
SATA[1:0]RXP/N	• Connect to RXP/N • No extra series termination resistors or other pull-ups/pull-downs are required	
CLK100P	• Connect SRC on CK409 • Pull down through 49.9 Ω ± 1%	
CLK100N	• Connect SRC# on CK409 • Pull down through 49.9 Ω ± 1%	

17.8.5 Intel® ICH5 / Flash BIOS and LPC Items

Checklist Items	Connections/Recommendations	Reason/Impact
FB[3:0]/LAD[3:0], LDRQ[1:0]#/GPI41	• No extra pull-ups required. Connect straight to flash BIOS/LPC.	• Intel® ICH5 Integrates 20 kΩ nominal pull-up resistors on these signal lines
Flash BIOS Decoupling	• Follow vendor recommendation	
LFRAME#		

17.8.6 Intel® ICH5 / RTC Items

Checklist Items	Connections/Recommendations	Reason/Impact
RTCX1, RTCX2	• Connect a 32.768 kHz crystal oscillator across these pins with a 10 MΩ resistor	• The external circuitry required to maintain the accuracy of the RTC • The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VccRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.
RTCRST#	• Time constant due to RC filter on this line should be 18 – 25 ms. Recommended value for resistor = 180 kΩ and capacitor is 0.1 µF.	• Timing Requirement

17.8.7 Intel® ICH5 / GPIO Items

Checklist Items	Connections/Recommendations	Reason/Impact
GPIO Pins	*GPIO[7:0]* • These pins are in the Main Power Well. Pull-ups must use the VCC3_3 plane. • Unused core well inputs must be pulled up to VCC3_3 • GPIO[1:0] can be used as REQ[B:A]# • GPIO1 can be used as PCI REQ5# • GPIO[5:2] can be used as PIRQ[H:E]# • These signals are 5 V tolerant • These pins are inputs *GPIO[15:8]* • These pins are in the Resume Power Well. Pull-ups must use the VccSus_3 plane. • Unused resume well inputs must be pulled up to VccSus3_3 • These signals are **NOT** 5 V tolerant • GPIO11 can be used as SMBALERT# • These pins are inputs	Ensure that **all** unconnected signals are **outputs only!**

Checklist Items	Connections/Recommendations	Reason/Impact
GPIO Pins (Continued)	*GPIO[23:16]* • Fixed as output only. Can be left NC. • GPIO22 is open drain • GPIO[17:16] can be used as GNT[B:A]# • GPIO17 can be used as PCI GNT5# • These signals are **NOT** 5 V tolerant *GPIO[28, 27, 25, 24]* • I/O pins. Default as outputs so can be left as NC. • These pins are in the resume power well • GPIO[28:27, 25] From resume power well. (Note: use pull-up to VccSus3_3 if these signals are pulled-up). • These signals are **NOT** 5 V tolerant *GPIO[34:32]* • I/O pins. From main power well. • Default as outputs • These signals are **NOT** 5 V tolerant *GPIO[41:40]* • Input pins. From main power well. • GPIO40 can be used as REQ4# • GPIO41 can be used as LDRQ1# • These signals are **NOT** 5 V tolerant *GPIO48* • Output pin. From main power well. • GPIO48 can be used as GNT4# • These signals are **NOT** 5 V tolerant *GPIO49* • Output pin. From processor I/O power well. • GPIO49 can be used as CPUPWRGD • These signals are **NOT** 5 V tolerant	Ensure that **all** unconnected signals are **outputs only!**

17.8.8 Intel® ICH5 / SMBus and SMLink Items

Checklist Items	Connections/Recommendations	Reason/Impact
SMBDATA, SMBCLK	• Require external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination thereof.) • Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections.	• Value of pull-ups resistors determined by line load. Typical value used is 8.2 kΩ. **NOTE:** For PCI compliance, SMBus signals should be routed to either all or none of the PCI slots in a chassis.
SMBALERT#/ GPIO11	• Pull up to 3.3 V through 10 kΩ ± 5%. See GPIO section if SMBALERT# not implemented.	
SMLINK[1:0]	• Requires external 10 kΩ pull-up resistors to VccSus3_3 • Do not tie to SMBus signals	
LINKALERT#	• Requires external 10 kΩ pull-up resistors to VccSus3_3	
INTRUDER#	• Pull signal to VccRTC (VBAT) through 1 MΩ	• Signal in VccRTC (VBAT) well
SMBus Device Power	• Recommend that I^2C devices are powered by core voltage	

17.8.9 Intel® ICH5 / Miscellaneous Items

Checklist Items	Connections/Recommendations	Reason/Impact
INTVRMEN	• Pull signal to VccRTC (VBAT) through 330 kΩ pull-up resistor	
SPKR		• Has integrated pull-down. The integrated pull-down is only enabled at boot/reset for strapping functions; at all other times, the pull-down is disabled.
TP0	• Requires external pull-up to 3.3 V SB	

17.8.10 Intel® ICH5 / Power Management Items

Checklist Items	Connections/Recommendations	Reason/Impact
THRM#	• Connect to temperature sensor. Pull-up if not used (an 8.2 kΩ pull-up resistor to VCC3_3).	• Input to Intel® ICH5 cannot float. THRM# polarity bit defaults THRM# to active low, so pull-up.
THRMTRIP#	• A weak pull-up resistor to the V_CPU_IO well. See Processor Design Guide for specific pull-up value.	• Input to ICH5 cannot float
SLP_S3#, SLP_S4#, SLP_S5#	• No pull-up/down resistors needed. Signals driven by ICH5.	
PWROK	• Recommend a 10 kΩ pull-down to ground • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCC3_3 and Vcc1_5 have reached their nominal voltages	• Timing Requirement
PWRBTN#	• No extra pull-up resistors	• This signal has an integrated pull-up of 18 kΩ – 42 kΩ. This signal is internally debounced inside the ICH5.
SYS_RESET#	• Recommend an 8.2 kΩ pull-up resistor to VccSus3_3. Also a 100 Ω to 1 kΩ pull-down resistor isolated from SYS_RESET# by means of a normally open switch.	• Input to ICH5 cannot float. This pin forces an internal reset to the ICH5 after the signal is internally debounced.
RI#	• RI# does not have an internal pull-up. Recommend an 8.2 kΩ pull-up resistor to Resume well.	• If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns, the RI_STS bit will be set and the system will interpret that as a wake event.
RSMRST#	• Recommend a 10 kΩ pull-down to ground • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Can be tied to LAN_RST#	• Timing Requirement
LAN_RST#	• Recommend a 10 kΩ pull-down to ground • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Can be tied to RSMRST#	• Timing Requirement

17.8.11 Intel® ICH5 / Hub Items

Checklist Items	Connections/Recommendations	Reason/Impact
HI[10:0]	• Connect to HI[10:0] on MCH hub interface	
HI11	• Pull down to GND through 61.9 Ω ±5% resistor	
HI_STBF	• Connect to HISTRF on MCH hub interface	
HI_STBS	• Connect to HISTRS on MCH hub interface	
HIRCOMP	• Pull up to 1.5 V through 52.3 Ω ±1% resistor	
HI_VSWING	• Connect to HI_VSWING_ICH voltage divider circuit on chipset decoupling	• 800 mV
HIREF	• Connect to HI_VREF_ICH on voltage divider circuit on chipset decoupling	• 350 mV
CLK66	• Connect to 3V66_3 on CK409	

17.8.12 Intel® ICH5 / LAN Items

Checklist Items	Connections/Recommendations	Reason/Impact
LAN_CLK	• Connect to LAN_CLK on platform LAN connect device	• Intel® ICH5 contains integrated 100 kΩ nominal pull-down resistor on signal
LAN_RXD[2:0]	• Connect to LAN_RXD on platform LAN connect device	• ICH5 contains integrated 10 kΩ nominal pull-up resistors on interface
LAN_TXD[2:0], LAN_RSTSYNC	• Connect to LAN_TXD on platform LAN connect device	
If the LAN connect interface is not used	• Platform LAN connect interface can be left NC if not used	• Input buffers internally terminated

17.8.13 Intel® ICH5 / EEPROM Items

Checklist Items	Connections/Recommendations	Reason/Impact
EE_DOUT	• Connect to EE_DIN of EEPROM or CNR Connector • No extra circuitry required	• Intel® ICH5 contains integrated 20 kΩ nominal pull-up resistor for this signal • Connected to EEPROM data input signal • (Input from EEPROM perspective and output from ICH5 perspective)
EE_DIN	• No extra circuitry required. Connect to EE_DOUT of EEPROM or CNR connector.	• ICH5 contains integrated 20 kΩ nominal pull-up resistor for this signal • Connected to EEPROM data output signal • (Output from EEPROM perspective and input from ICH5 perspective)
EE_CS		
EE_SWCLK		

17.8.14 Intel® ICH5 / AC '97 Items

Checklist Items	Connections/Recommendations	Reason/Impact
AC_SDOUT	• Requires a jumper to 8.2 kΩ pull-up resistor. Should not be stuffed for default operation. • Series termination resistor 0 Ω to 47 Ω to on board codec and to the CNR	• This pin has a weak internal 20 kΩ nominal pull-down. To properly detect a safe mode condition a strong pull-up will be required to over-ride this internal pull-down.
AC_SDIN1, AC_SDIN0	• Internal pull-downs in Intel® ICH5; no external pull-downs required • Series termination resistors 0 Ω to 47 Ω from the AC_SDIN lines to the ICH5	• These pins have a weak internal 20 kΩ nominal pull-down
AC_SDIN2	• Requires a10 kΩ pull-down to ground if a CNR card is used on the platform • Series termination resistor 33 Ω to 47 Ω from the AC_SDIN lines to the ICH5	• This pin has a weak internal 20 kΩ nominal pull-down. For platforms routing AC_SDIN2 to CNR, the additional 10 kΩ pull-down is required to set the proper DC level for CNR card switching circuitry. • Used for a codec detection/ addressing mechanism on the CNR card
AC_BIT_CLK	• No extra pull-down resistors required • Series termination resistor 33 Ω to 47 Ω from the motherboard codec to the ICH5	• This pin has a weak internal 20 kΩ nominal pull-down
AC_SYNC	• No extra pull-down resistors required	• Some implementations add termination for signal integrity. This is platform specific.
AC_RST#	• Connect to AC97_RESET# on CNR • Connect to RESET# on Audio Codec • Connect to AUD_LINK_RST# on Port Angeles[1]	

NOTE:
1. Port Angeles is an Intel enabled specification for building an integrated super I/O and Glue Logic chip. At this time, National Semiconductor Corporation and SMSC Corporation make IC devices that implement this specification. For National Semiconductor Corporation, the part number is PC87372. For SMSC Corporation, the part number is LPC47M172.

17.8.15 Intel® ICH5 / USB Items

Checklist Items	Connections/Recommendations	Reason/Impact
USBRBIAS	• 22.6 Ω ± 1% connected to ground	• Refer to Section 10.7.1.3
USBRBIAS#	• Connected to the same 22.6 Ω ± 1% resistor to ground as USBRBIAS	• Refer to Section 10.7.1.3
USBP[7:0]P, USBP[7:0]N	• Connect to USB Panel • No external resistors are required	• Effective output driver impedance of 45 Ω provided
OC[7:0]#	• Connect to Wake on USB • If not used, use 10 kΩ to VccSus3_3	• Inputs must not float
Unconnected USB data signals	• Unconnected USB data signals can be left as no-connects	

17.9 Platform Power and Ground

17.9.1 Intel® ICH5 / Power and Ground Items

Checklist Items	Connections/Recommendations	Reason/Impact
V_CPU_IO[2:0]	• The power pins should be connected to the proper power plane for the processor CMOS compatibility signals. Use one 0.1 µF decoupling capacitor (VCC).	• Used to pull-up all processor I/F signals
VccRTC	• Use one 0.1 µF decoupling capacitor (VCC) • No clear CMOS jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safe mode strapping for Clear CMOS.	
VCC3_3	• Use six 0.1 µF decoupling capacitors (VSS)	
VccSus3_3	• Use three 0.1 µF, one 0.01 µF, one 1.0 µF decoupling capacitors (VSS)	
Vcc1_5	• Use six 0.1 µF, one 0.01 µF decoupling capacitors (VSS)	
VccSus1_5	• Use one 0.1 µF decoupling capacitors (VSS)	
V5REF_Sus	• Use one 0.1 µF decoupling capacitor (VSS) • V5REF is the reference voltage for 5 V tolerant inputs in the Intel® ICH5. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3. For most platforms this is not an issue because VccSus3_3 is usually derived from V5REF_Sus.	
V5REF	• Use one 0.1 µF decoupling capacitor (VCC) • V5REF is the reference voltage for 5 V tolerant inputs in the ICH5. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3.	
VccUSBPLL	• Use one 0.1 µF and one 0.01 µF decoupling capacitor (VSS)	
VccSATAPLL	• Use one 0.1 µF and one 0.01 µF decoupling capacitor (VSS)	
HIREF	• 350 mV	

Layout Checklist 18

This chapter highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements the 848P chipset.

18.1 Platform Clock

18.1.1 Clock Groups

18.1.1.1 HOST_CLK Clock Group

#	Layout Recommendations	Yes	No	Comments[1]
1	HOST_CLK Skew between Agents: 150 ps for clock driver 150 ps for interconnect			
2	Trace Width: 5 mils Differential Pair Spacing: 11 mils Spacing to Other Traces: 25 mils			
3	Serpentine Spacing: Maintain a minimum 25 mils. Keep parallel serpentine sections as short as possible. Minimize 90 degree bends. Make 45 degree bends if possible.			
4	Motherboard Impedance: Differential 100 Ω typical			
5	Processor Routing Length: Clock Driver to Rs; L1 – L1” = 0.5 inch Max Rs to Rs-Rt Node; L2 – L2” = 0 – 0.2 inch Rs-Rt Node to Rt; L3 – L3” = 0 – 0.2 inch Rs-Rt Node to Load; L4 – L4” = 2 – 15 inches			
6	MCH Routing Length: Clock Driver to Rs; L1 – L1” = 0.5 inch Max Rs to Rs-Rt Node; L2 – L2” = 0 – 0.2 inch Rs-Rt Node to Rt; L3 – L3” = 0 – 0.2 inch Rs-Rt Node to Load; L4 – L4” = 2 – 15 inch			
7	Processor to MCH Length Matching (LT), Host clocks to processor should be 165 mils longer			
8	HOST_CLK0_HOST_CLK1 Length Matching: ± 10 mils			
9	Rs Series Termination Value: 33 Ω ± 5%			
10	Rt Shunt Termination Value 49.9 Ω ± 1% (for 50 Ω odd mode MB impedance)			

NOTES:
1. Refer to Section 4.1.1.

18.1.1.2 BCLK General Routing

#	Layout Recommendations	Yes	No	Comments[1]
1	When routing 100/133/166 MHz selectable differential clocks, do not split up the two halves of a differential clock pair between layers, and rout to all agents on the same physical routing layer referenced to ground.			
2	If a layer transition is required, make sure to do simulations to determine the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.			
3	If a layer transition is required, then both clock traces part must transition layers so that differential routing is maintained.			

NOTES:
1. Refer to Section 4.1.2.

18.1.2 CLK66 and CLK33 Clock Groups

18.1.2.1 TCLK33 Clock Group

#	Layout Recommendations	Yes	No	Comments[1]
1	Characteristic Trace Impedance: 60 Ω ± 15%			
2	Trace Width: 5 mils Trace Spacing: 10 mils			
3	Intel® ICH5, Flash BIOS, SIO, PCI slots: Trace Length - L1; 0 inch – 0.5 inch			
4	ICH5 – L2; Z, 2 inches – 20 inches			
5	Flash BIOS, SIO Trace Length - L2; Z ± (0 inch – 10 inches); max length is 20 inches			
6	PCI slots Trace Length - L2; Z - 4 ± (0 inch – 10 inches); max length is 20 inches			
7	Resistor: R1 = 33 Ω ± 5%			

NOTES:
1. Refer to Section 4.2.3.

18.1.2.2 Sharing 33 MHz Clocks

#	Layout Recommendations[1]	Yes	No
1	Characteristic Trace Impedance: 60 Ω ± 15%		
2	Trace Width: 5 mils Trace Spacing: 10 mils		
3	PCI down devices – L1; 0 – 5 inches; max length is 20 inches		
4	PCI down devices – L2 and L3 Z ± (0 – 7 inches); max length is 20 inches. L2 and L3 should be length matched to within 250 mils		
5	Resistor: 33 Ω ± 5%		

NOTES:
1. Refer to Section 4.2.3.1.

18.1.2.3 CLK66 Clock Group

#	Layout Recommendations[1]	Yes	No
1	Characteristic Trace Impedance: 60 Ω ± 15%		
2	Trace Width: 5 mils Trace Spacing: 10 mils		
3	AGP connector, MCH, Intel® ICH5, CSA Trace Length – L1; 0 – 0.5 inch		
4	Clock Driver to MCH – L2; Y, 2 – 20 inches		
5	Clock Driver to ICH5, GbE, and CLK_33 to ICH5 (Length “Z”) Trace Length – L2; Y ± (0 – 0.5 inch); Maximum length is 20 inches		
6	Clock Driver to AGP connector Trace Length – L2; Y - 5 ± (0 – 0.5 inch); Maximum length is 20 inches		
7	Resistor: 33 Ω ± 1%		

NOTES:
1. Refer to Section 4.2.2.

18.1.2.4 CLK14 Clock Group

#	Layout Recommendations[1]	Yes	No
1	Characteristic Trace Impedance: 60 Ω ± 15%		
2	Trace Width: 5 mils Trace Spacing: 10 mils		
3	Trace Length – L1; 0 inch – 0.5 inch		
4	Trace Length – L2; 0 inch – 12 inches		
5	Trace Length – L3; 0 inch – 6 inches		
6	CLK14 total length (L1+L2+L3) (L1+L2+L3) to Intel® ICH5 must be within 500 mils of (L1+L2+L3) to SIO		
7	Resistor: 33 Ω ± 5%		

NOTES:
1. Refer to Section 4.3.

18.1.2.5 USBCLK Clock

#	Layout Recommendations[1]	Yes	No
1	Characteristic Trace Impedance: 60 Ω ± 15%		
2	Trace Width: 5 mils Trace Spacing: 20 mils		
3	Trace Length – L1; 0 – 0.5 inch		
4	Trace Length – L2; 2 – 20 inches		
5	Resistor: R1 = 22 Ω ± 1%		
6	Skew Requirements: USBCLK is asynchronous to any other clock on the board		
7	Maximum via Count: 2		

NOTES:
1. Refer to Section 4.4.

18.1.2.6 SRC Clock Group

#	Layout Recommendations	Yes	No	Comments
1	Trace Width: 5 mils Differential Pair Spacing: 11 mils Spacing to Other Traces: 25 mils			Note 1
2	Serpentine Spacing: Maintain a minimum 25 mils. Keep parallel serpentine sections as short as possible. Minimize 90 -degree bends. Make two, 45-degree bends if possible.			Note 1
3	Motherboard Impedance - Differential: 100 Ω typical			Note 1
4	Routing Length - L1, L1': Clock Driver to Rs; 0.5 inch Max L2, L2': Rs to Rs-Rt Node; 0 – 0.2 inch L3, L3': Rs-Rt Node to Rt; 0 – 0.2 inch L4, L4': Rs-Rt Node to Load; 2 – 15 inches			Note 1
5	SCR - SCR# Length Matching: ± 10 mils			Note 1
6	Rs Series Termination Value: 33 Ω ± 1%			Note 1
7	Rt Shunt Termination Value: 49.9 Ω ± 5% (for 50 Ω odd mode MB impedance)			Note 1
8	When routing the 100 MHz differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.			Note 2
9	If a layer transition is required, make sure skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.			Note 2
10	Do not place vias between adjacent complementary clock traces, and avoid differential vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.			Note 2

NOTES:
1. Refer to Section 4.5.1.
2. Refer to Section 4.5.2.

18.1.3 Clock Driver Decoupling

#	Layout Recommendations[1]	Yes	No
1	For All power connection to planes, decoupling capacitors and vias, the Maximum trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance.		
2	The VSS pins should not be connected directly to the VSS side of the capacitors. They should be connected to the ground flood under the part that is viaed to the ground plane to avoid VDD glitches propagating out, getting coupled through the decoupling capacitors to the VSS pins. This method has been shown to provide the best clock performance.		
3	The ground flood should be viaed through the ground plane with no less than 12–16 vias under the part. It should be will connected.		
4	For all power connections, heavy duty and /or dual vias should be used.		
5	It is imperative that the standard signal vias and small traces not be used for connecting decoupling capacitors and ground floods to the power or ground planes.		

NOTES:
1. Refer to Section 4.6.

18.2 Front Side Bus (FSB)

18.2.1 AGTL + 4X Routing

Signal	Layout Recommendations[1]	Yes	No
D[63:0]#	Spacing: [3:1], Length: 2.5 inches to 6 inches, Ref: VSS, Impedance: 60 Ω ± 15%, Matching: ± 25 mils		
DSTBP[3:0]#	Spacing: [4:1], Length: 2.5 inches to 6 inches, Ref: VSS, Impedance: 60 Ω ± 15%, Matching: ± 25 mils		
DSTBN[3:0]#	Spacing: [4:1], Length: 2.5 inches to 6 inches, Ref: VSS, Impedance: 60 Ω ± 15%, Matching: ± 25 mils		
DBI[3:0]#	Spacing: [3:1], Length: 2.5 inches to 6 inches, Ref: VSS, Impedance: 60 Ω ± 15%, Matching: ± 25 mils		

NOTES:
1. Refer to Section 5.1.3.1.

18.2.2 AGTL + 2X Routing

Signal	Layout Recommendations[1]	Yes	No
A[31:3]#	Spacing: [3:1], Length: 3 – 10 inches, Ref: VSS, Impedance: 60 Ω ± 15%, Matching: ± 100 mils		
ADSTB[1:0]#	Spacing: [4:1], Length: 3 – 10 inches, Ref: VSS, Impedance: 60 Ω ± 15%, Matching: ± 100 mils		
REQ[4:0]#	Spacing: [3:1], Length: 3 – 10 inches, Ref: VSS, Impedance: 60 Ω ± 15%, Matching: ± 100 mils		

NOTES:
1. Refer to Section 5.1.3.2.

18.2.3 AGTL + 1X Routing

Signal	Layout Recommendations[1]	Yes	No
BPRI#	Spacing: [3:1], Length: 3 – 8 inches, Ref: VSS, Impedance: 60 Ω ± 15%		
DEFER#	Spacing: [3:1], Length: 3 – 8 inches, Ref: VSS, Impedance: 60 Ω ± 15%		
RS[2:0]#	Spacing: [3:1], Length: 3 – 8 inches, Ref: VSS, Impedance: 60 Ω ± 15%		
TRDY#	Spacing: [3:1], Length: 3 – 8 inches, Ref: VSS, Impedance: 60 Ω ± 15%		
ADS#	Spacing: [3:1], Length: 3 – 8 inches, Ref: VSS, Impedance: 60 Ω ± 15%		
BNR#	Spacing: [3:1], Length: 3 – 8 inches, Ref: VSS, Impedance: 60 Ω ± 15%		
DBSY#	Spacing: [3:1], Length: 3 – 8 inches, Ref: VSS, Impedance: 60 Ω ± 15%		
DRDY#	Spacing: [3:1], Length: 3 – 8 inches, Ref: VSS, Impedance: 60 Ω ± 15%		
HIT#	Spacing: [3:1], Length: 3 – 8 inches, Ref: VSS, Impedance: 60 Ω ± 15%		
HITM#	Spacing: [3:1], Length: 3 – 8 inches, Ref: VSS, Impedance: 60 Ω ± 15%		
LOCK#	Spacing: [3:1], Length: 3 – 8 inches, Ref: VSS, Impedance: 60 Ω ± 15%		

NOTES:
1. Refer to Section 5.1.3.3.

18.2.4 Asynchronous GTL + Signals Group

Signal	Layout Recommendations	Yes	No	Comments
THERMTRIP#	Impedance: 60 Ω ± 15%, Spacing: 7 mils, Width: 5 mils L1: 1 – 12 inches, L2: 3 inches maximum, Rpu: 62 Ω ± 5%			Refer to Section 5.1.6.1
FERR#	Impedance: 60 Ω ± 15%, Spacing: 7 mils, Width: 5 mils L1: 1 – 12 inches, L2: 3 inches maximum, Rpu: 62 Ω ± 5%			Refer to Section 5.1.6.1
A20M#	Impedance: 60 Ω ± 15%, Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum			Refer to Section 5.1.6.2
IGNNE#	Impedance: 60 Ω ± 15% Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum			Refer to Section 5.1.6.2
SMI#	Impedance: 60 Ω ± 15% Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum			Refer to Section 5.1.6.2
SLP#	Impedance: 60 Ω ± 15% Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum			Refer to Section 5.1.6.2
STPCLK#	Impedance: 60 Ω ± 15% Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum			Refer to Section 5.1.6.2
LINT[1:0]	Impedance: 60 Ω ± 15% Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum			Refer to Section 5.1.6.2
IERR#	Impedance: 60 Ω ± 15% Spacing: 7 mils, Width: 5 mils L1: 1 inch maximum, Rpu: 62 Ω ± 5%			Refer to Section 5.1.6.3
RESET#	Impedance: 60 Ω ± 15% Spacing: 13 mils, Width: 5 mils L1: 2 – 10 inches, L2: 1 – 2 inches, Rpu: 62 Ω ± 5%			Refer to Section 5.1.6.4
BR0#	Impedance: 60 Ω ± 15% Spacing: 13 mils, Width: 5 mils L1: 2 – 10 inches, L2: 1 – 2 inches, Rpu: 200 Ω ± 5%			Refer to Section 5.1.6.4

Signal	Layout Recommendations	Yes	No	Comments
INIT#	Impedance: 60 Ω ± 15% Spacing: 7 mils, Width: 5 mils L1: 17 inches maximum, L2: 2 inches maximum, L3: 10 inches maximum **NOTE:** It is recommended to use 7 mil spacing around the INIT# signal. If 5 mil spacing is used, the total portion routed at this width cannot exceed 8 inches.			Refer to Section 5.1.6.5
PWRGOOD	Impedance: 60 Ω ± 15% Spacing: 13 mils, Width: 5 mils L1: 1 – 12 inches, L2: 3 inches maximum, Rpu: 300 Ω ± 5%			Refer to Section 5.1.6.6
PROCHOT#	Impedance: 60 Ω ± 15% Spacing: 7 mils, Width: 5 mils L1: 0.75 inch maximum, L2: 10 inches maximum, L3: 10 inches maximum, L4: 0.5 inch maximum, Rpu: 120 Ω –140 Ω± 5%			Refer to Section 5.1.6.7
TESTHI	Impedance: 60 Ω ± 15% Spacing: 7 mils, Width: 5 mils L1: 1 inch maximum, Rpu: 62 Ω ± 5%			Refer to Section 5.1.6.8
COMP[1:0]	Impedance: 60 Ω ± 15% Spacing: 13 mils, Width: 5 mils L1: 1.5 inches maximum, Rpd: 61.9 Ω ± 1%			Refer to Section 5.1.6.9
BOOTSELECT	Impedance: 60 Ω ± 15%, Spacing: 7 mils, Width: 5 mils			Refer to Section 5.1.6.10
RESERVED	NA			Refer to Section 5.1.6.11
OPTIMIZED/ COMPAT# (Intel® Pentium® 4 processor on 90 nm process) IMPSEL (Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process)	NA			Refer to Section 5.1.6.12

18.2.5 Power / Other Signals

Signal	Layout Recommendations	Yes	No	Comments
GTLVREF[3:0]	Spacing: 15 mils, Width: 12 mils. L1+L2: 3.5 inches max, L3: 3 inches max, L4+L5+L6: 1.5 inches maximum			Refer to Section 5.1.6.13
VID[5:0]	Spacing: 5 mils, Width: 5 mils. L1+L2+L5: 15 inches maximum			Refer to Section 5.1.6.14
VCCVID / VCCVIDLB	Trace connecting AF3 and AF4 should be as wide as practical, but no less than 25 mils			Refer to Section 15.3.1.7
VCCA / VSSA / VCCIOPLL	Trace should be a minimum of 12 mils. VCCA and VSSA should be routed together. Place decoupling capacitor within 600 mils of VCCA/VSSA pins.			Refer to Section 15.3.1.8
THERMDA / THERMDC	Spacing: 10 mils, Width: 10 mils. Route two lines in parallel and close together. L1: 4 inches ~ 8 inches			Refer to Section 5.1.6.15
Host RCOMP	Spacing: 7 mils, Width: 10 mils, L1: 0.5 inch maximum, Rpd: 20 Ω ± 1%			Refer to Section 5.1.6.16
Host SWING	Spacing: 10 mils, Width: 12 mils, L1: 3 inches maximum			Refer to Section 5.1.6.17
BSEL[1:0]	Spacing: 5 mils, Width: 5 mils			Refer to Section 5.1.6.18

18.3 DDR System Memory

18.3.1 Clocks (SCMDCLK_A[5:0], SCMDCLK_A[5:0]#)

#	Layout Recommendations[1]	Yes	No
1	MCH to 1st DIMM: Width 8 mils on Spacing 5 mils		
2	Channel A DIMMs and beyond: Width 6 mils on Spacing 5 mils		
5	Total Trace Length P + A: Max = 6.3 inches		
6	Total Clock Length Relationship between DIMM0 and DIMM1 across the channel: The total clock length difference should be no more than 1 inch		
7	Maximum via count per signal: 1 via (for breakout to bottom layer)		
8	Length Matching method, Length = P + A: Each SCMDCLK_A and SCMDCLK_A# pair must be tuned to within 20 mils All three Clock pairs on a given DIMM must be less than 600 mils different in length		

NOTES:
1. Refer to Section 6.2.2.

18.3.2 Address/Command (SMAA_A[12:6,0], SBA_A[1:0], SRAS_A#, SCAS_A#, SWE_A#)

#	Layout Recommendations[1]	Yes	No
1	Target Impedance: 60 Ω ± 15%		
2	MCH to 1st DIMM: Width 5 mils on Spacing 12 mils		
3	DIMM pin field: Width 5 mils on Spacing 6 mils		
4	Termination: Width 5 mils on Spacing 5 mils		
5	1st DIMM pin to 2nd DIMM pin: 200–600 mils, but with ≤ 200 mils variance between the longest and shortest trace segments for that channel		
6	Last DIMM pin to termination: Max = 800 mils		
7	MCH die to last DIMM pin: 5.3 inches		
8	Termination Resistor (Rtt): 47 Ω ± 5%		
9	Maximum via count per signal: 2 vias (for bottom layer signals, one at MCH ballout and the other at termination, where needed)		
10	Length Tuning: SCMDCLK_A[2:0] = X Xmin – 2.1 inches ≤ Addr/Cmd length ≤ Xmax All lengths include both package and motherboard trace lengths		
11	Length Tuning: SCMDCLK_A[5:3] = Y Ymin – 2.1 inches ≤ Addr/Cmd length ≤ Ymax All lengths include both package and motherboard trace lengths		

NOTES:
1. Refer to Section 6.2.3.

18.3.2.1 Data Signals (SDQ_A[63:0], SDQS_A[7:0]) (3” < Byte Lane Length)

#	Layout Recommendations[1]	Yes	No
	3.0” < Byte Lane Length ≤ 5.7”		
1	Target Impedance: 50 Ω ± 15%		
2	Breakout: Width 5 mils on Spacing 5 mils for up to 550 mils		
3	MCH to 1st DIMM: Width 7 mils on Spacing 12 mils for SDQ_A Width 7 mils on Spacing 15 mils for SDQS_A		
4	DIMM pin field: SDQ_A: Width 5 mils on Spacing 5 mils SDQS_A: Width 5 mils on Spacing 10 mils		
5	Termination: Width 5 mils on Spacing 5 mils		
6	If the trace width and spacing rules for the different routing regions cannot be met, decrease SDQ_A-to-SDQ_A spacing to 11 mils.		
	5.7” < Byte Lane Length ≤ 6.9”		
1	Target Impedance: 40 Ω ± 15%		
2	Breakout: Width 5 mils on Spacing 10 mils up to 550 mils then: SDQ_A: Width 7 mils on Spacing 10 mils for up to 1000 mils SDQS_A: Width 7 mils on Spacing 15 mils for up to 1000 mils		
3	MCH TO 1st DIMM: Width 11mils on Spacing 12 mils for SDQ_A Width 11 mils on Spacing 15 mils for SDQS_A When implementing the wider 11 mil trace width rule, the wider trace width should be implemented on all DQ and DQS signals within a byte lane. If necessary, the wider trace width may be achieved incrementally, however, the widest possible width should be achieved as quickly as possible. The final 11 mil trace width should be achieved within 2.0” of the ball. Also note that normal L2 spacing rules apply for the transition region.		
4	DIMM pin field: SDQ: Width 5 mils on Spacing 5 mils SDQS: Width 5 mils on Spacing 10 mils		
5	Termination: Width 5 mils on Spacing 5 mils		
	If the trace width and spacing rules for the different routing regions cannot be met, gradually increase trace width and spacing as noted below: • Follow region 1 and 2 breakout recommendations from Figure 6-8 • Transition to routing to DIMM pin field as soon as possible: - SDQ_A = 8 on 12 mils, SDQS_A = 8 on 15 mils. - Maximize SDQ/SDQS trace width and SDQS signal spacing as much as possible • Routing to DIMM pin field: SDQ_A = 11 on 12 mils, SDQS_A = 11 on 17 mils		

#	Layout Recommendations[1]	Yes	No
	Length Matching		
1	1st DIMM pin to 2nd DIMM pin: 200–600 mils, but with ≤ 200 mils variance between the longest and shortest trace segments for that channel.		
2	Last DIMM pin to termination: Max = 800 mils		
3	Termination Resistor (Rtt): 56 Ω ± 5%		
4	Max via count per signal: 2 vias (for bottom layer signals, one at MCH ballout and the other at termination, where needed).		
5	SDQ_A Length Tuning to DIMM[1:0]: SDQ_A must be tuned to within ± 25 mils of their associated SDQS from MCH pad to DIMM[1:0] pin.		
6	DQS Length Tuning: SCMDCLK_A[2:0] = X Xmin – 2.1 inches ≤ SDQS_A ≤ Xmax – 1.5 inches All lengths include both package and motherboard trace lengths.		
7	DQS Length Tuning: SCMDCLK_A[5:3] = Y Ymin – 2.1 inches ≤ SDQS_A ≤ Ymax – 1.5 inches All lengths include both package and motherboard trace lengths.		

NOTES:
1. Refer to Section 6.2.4.

18.3.2.2 Control Signals (SCKE_A[3:0]#, SCS_A[3:0]#)

#	Layout Recommendations[1]	Yes	No
1	Target Impedance: 60 Ω ± 15%		
2	MCH to 1st DIMM: Width 5 mils on Spacing 12 mils		
3	DIMM pin field: Width 5 mils on Spacing 6 mils		
4	Termination: Width 5 mils on Spacing 5 mils		
5	DIMM pin to Termination: Max = 1.4 inches		
6	Termination Resistor (Rtt): 47 Ω ± 5%		
7	Max via count per signal: 2 vias (for bottom layer signals, one at MCH ballout and the other at termination)		
8	Length Tuning Method: SCMDCLK = X Xmin – 1.5 inches ≤ Control ≤ Xmax All lengths include both package and motherboard trace lengths		

NOTES:
1. Refer to Section 6.2.5.

18.3.2.3 CPC Address Signals (SMAA_A[5:1], SMAB_A[5:1])

#	Layout Recommendations[1]	Yes	No
1	Target Impedance: 50 Ω ± 15%		
2	Breakout: 5 on 5 up to 550 mils		
2	MCH to 1st DIMM: Width 7 mils on Spacing 12 mils		
3	DIMM pin field: Width 5 mils on Spacing 5 mils		
4	Termination: Width 5 mils on Spacing 5 mils		
7	DIMM pin to Termination: Max = 1.4 inches		
8	Termination Resistor (Rtt): 47 Ω ± 5%		
9	Max via count per signal: 2 vias (for bottom layer signals, one at MCH ballout and the other at termination)		
10	Length Tuning Method: SCMDCLK_A = X 2.5” < CPC < 3.7”: Xmin ≥ CPCmax + 1.1” 3.7” < CPC < 4.7”: Xmin > CPCmax + 1.7” All lengths include both package and motherboard trace lengths		

NOTES:
1. Refer to Section 6.2.6

18.3.3 DDR Reference Voltage

18.3.3.1 DDR VREF at the MCH

Parameter	Layout Recommendations[1]	Yes	No
VREF Routing	Minimum 12-mils wide and separated from other traces by a minimum of 12-mils spacing, except during breakout, which allows for 7-mils spacing to other signals for no more than 350 mils.		
Voltage Divider	Place resistor divider consisting of two 150 Ω ± 1% resistors within 1 inch of the DIMM connectors.		
Decoupling at the Resistor Divider	Two 2.2 µF capacitors Place one 2.2 µF capacitor between SM_VREF and ground and the other between VDD (2.6 V) and ground.		
Decoupling at SM_VREF Source Pin	Place one 0.1 µF capacitor as close as possible to the MCH SM_VREF source pin.		
Decoupling for un-used SM_VREF pin	Place two capacitors, a 2.2 µF and a 0.1 µF, on the unsourced SM_VREF pin.		

NOTES:
1. Refer to Section 6.3.1.

18.3.3.2 DDR VREF at the DIMMs

Parameter	Layout Recommendations[1]	Yes	No
VREF Routing	Minimum 12 mils wide and separated from other traces by a minimum of 12-mils spacing.		
Voltage Divider	Place resistor divider consisting of two 75 Ω ± 1% resistors within 1 inch of the DIMM connectors.		
Decoupling at the resistor divider	Two 0.1 µF capacitors Place one 0.1 µF capacitor as close as possible to each DIMM VREF pin.		

NOTES:
1. Refer to Section 6.3.2.

18.3.4 DDR Resistive Compensation (SMRCOMP) per-Channel

18.3.4.1 DDR SMRCOMP

Parameter	Layout Recommendations[1]	Yes	No
RCOMP Resistors	42.2 Ω ± 1% pulled to VDD (2.6 V), place resistors within 1 inch of the MCH		
RCOMP Routing	Minimum trace width of 12 mils and minimum spacing from other signals of 10 mils		
Decoupling	Decouple each RCOMP circuit with a 2.2 µF capacitor.		

NOTES:
1. Refer to Section 6.4.

18.3.4.2 DDR RCOMP VOH and VOL

Parameter	Layout Recommendations[1]	Yes	No
Nominal RCOMPVOH	Nominal VOH = 1.89 Ω ± 2%		
Nominal RCOMPVOL	Nominal VOH = 0.61 Ω ± 2%		
RCOMP Resistors	R1 = 3.112*R2, Recommend R2 = 10 kΩ ± 1%		
RCOMP Routing	Minimum trace width of 12 mils and minimum spacing from other signals of 10 mils.		
Decoupling	Place the 0.01 µF capacitors no more than 1 inch from the MCH; place the 1 µF and 2.2 µF capacitors at the resistor divider.		

NOTES:
1. Refer to Section 6.4.

18.4 HUB Interface

18.4.1 8-Bit Hub Interface

#	Layout Recommendations[1]	Yes	No
1	Board impedance must be 60 Ω ± 15% or 50 Ω ± 10%		
2	Traces must be routed 5 mils wide with 15 mils spacing (using given example 4-layer 4.3 mil prepreg stack-up).		
3	To breakout of the MCH and Intel® ICH5 package, the hub interface signals can be routed 5 on 5.		
4	MCH Breakout: 5 on 5 for 2 inches Maximum ICH5 Breakout: 5 on 5 for 0.3 inch Maximum		
5	Data signals must be matched within ± 0.1 inch of the HI_STB differential pair.		
6	HI_STBS and /HI_STBF lengths must be matched.		
7a	(Single Reference Diver Circuit only) HIREF divider should be placed no more than 4 inches of away from MCH or ICH5.		
7b	(Local Reference Divider Circuit only) HIREF dividers should be placed no more than 4 inches of away from MCH or ICH5.		
8	HI signals must be referenced to ground.		

NOTES:
1. Refer to Section 7.1.

18.4.2 Hub Interface Routing

#	Layout Recommendations[1]	Yes	No
1	60 Ω ± 15% trace impedance		
2	Width: 5 mils and Spacing 15 mils. L1: 2 inches to 10 inches		
3	MCH Breakout: 5 on 5 for 2 inches Maximum Intel® ICH5 Breakout: 5 on 5 for 0.3 inch Maximum		
4	Strobe to Strobe Length Matching: ± 100 mils Data to Data Length Matching: ± 100 mils		
5	Strobe to Data Length Matching: ± 100 mils		

NOTES:
1. Refer to Section 7.1.

18.4.3 Hub Interface HIVREF/HISWING

Parameter	Layout Recommendations[1]	Yes	No
HIVREF Voltage Specification	350 mV ± 1.5% at 1.5 V nominal		
HISWING Voltage Specification	800 mV ± 1.5% at 1.5 V nominal		
HIVREF / HISWING Divider CRT	R1 = 226 Ω ± 1%, R2 = 147 Ω ± 1%, R3 = 113 Ω ± 1% C2 and C5 = 0.1 µF (near divider) C1, C3, C4, and C6 = 0.01 µF (near component)		

NOTES:
1. Refer to Section 7.1.2.

18.4.4 Hub Interface Compensation

18.4.4.1 RCOMP Resistor Values for Hub Interface

#	Layout Recommendations[1]	Yes	No
1	Trace Impedance: 60Ω ± 15%		
2	HICOMP Calculation: 52.3 Ω ± 1%		
3	VCC = 1.5 V		

NOTES:
1. Refer to Section 7.1.3.

18.4.4.2 RCOMP Resistor Values for Intel® ICH5

#	Layout Recommendations[1]	Yes	No
1	Trace Impedance: 60 Ω ± 15%		
2	HICOMP Calculation: 52.3 Ω ± 1%		
3	VCC = 1.5 V		

NOTES:
1. Refer to Section 7.1.3.

18.5 AGP 8X

18.5.1 AGP 8X Routing

18.5.1.1 Source Synchronous Signals

Parameter	Layout Recommendations[1]	Yes	No
Interconnect Length	Min: 0.5 inch, Max: 3.5 inches Worst-case interconnect skews listed in Table 8-3 are based on simulations that take into account likely layout topologies and a wide range of interconnect. Listed trace lengths include pin-to-trace breakout and trace-to-connector fan-in/out.		
Strobe-to-Strobe	Max: 5 mils Worst-case interconnect skews listed in Table 8-3 are based on simulations that take into account likely layout topologies and a wide range of interconnect. Listed trace lengths include pin-to-trace breakout and trace-to-connector fan-in/out.		
Strobe-to-Data	Max: 25 mils This mismatch budget applies to the combined trace lengths of the combined trace lengths of the package and board signals.		
Data-to-Data Spacing	Min: 3/1 S/H Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane.		
Strobe-to-Strobe Spacing	Min: 5/1 S/H Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane.		
Strobe-to-Data Spacing	Min: 5/1 S/H Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane.		
Trace Impedance	Min: 51 Ω, Max: 69 Ω		
Connector Breakout	Max: 200 mils This is the fan-in/out length that does not follow the normal trace separation requirements in the connector area on the motherboard and the edge fingers of the graphic cards.		
MCH Breakout	Max: 550 mils		

NOTES:
1. Refer to Section 8.2.2.

18.5.1.2 Common Clock Signals

Parameter	Layout Recommendations[1]	Yes	No
Interconnect Length	Min: 0.5 inch, Max: 3.5 inches Worst-case interconnect skews listed in are based on simulations that take into account. Listed trace lengths include pin-to-trace breakout and trace-to-connector fan-in/out.		
Common Clock-to-Common Clock Spacing	Min: 2/1 S/H Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane.		
Common Clock-to-Data Spacing	Min: 3/1 S/H Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane.		
Common Clock-to-Strobe Spacing	Min: 5/1 S/H Parameter refers to the Space-to-Height ratio of spacing between signal traces and the height above the associated ground plane.		
Trace Impedance	Min: 51 Ω, Max: 69 Ω		
Connector Breakout	Max: 200 mils This is the fan-in/out length that does not follow the normal trace separation requirements in the connector area on the motherboard and the edge fingers of the graphic cards.		
MCH Breakout	Max: 550 mils		

NOTES:
1. Refer to Section 8.2.2.

18.6 CSA Port

18.6.1 CSA Port Routing

#	Layout Recommendations[1]	Yes	No
1	Characteristic Trace Impedance: 60 Ω ± 15%		
2	Trace Width: 5 mils		
3	Trace Spacing: 10 mils		
4	L1: 2 inches to 10 inches Also includes MCH and the Intel® 82547EI chipset platform breakout length.		
5	MCH Breakout: 5 on 5 for 2 inches		
6	Intel 82547EI Breakout: 5 on 5 for 300 mils		
7	Strobe-to-Strobe Length Matching: ± 10 mils		
8	Strobe-to-Data Length Matching: ± 100 mils		

NOTES:
1. Refer to Section 9.1.

18.6.2 CSA Port Generation/Distribution of Reference Voltage

#	Layout Recommendations[1]	Yes	No
1	Reference Voltage Specification (V): 0.350 Ω ± 3%		
2	Reference swing Voltage Specification (V): For MCH and Intel® 82547EI = 0.8 Ω ± 3%		
3	1.5 V Voltage Divider Circuit Recommended Resistor Values: R1 = 113 Ω ± 1% R2 = 147 Ω ± 1% R3 = 226 Ω ± 1%		
4	1.2 V Voltage Divider Circuit Recommended Resistor Values: R4 = 523 Ω ± 1% R5 = 665 Ω ± 1% R6 = 604 Ω ± 1%		

NOTES:
1. Refer to Section 9.2.

18.6.3 CSA Port Resistive Compensation

18.6.3.1 RCOMP Resistor Values for MCH

#	Layout Recommendations[1]	Yes	No
1	Trace Impedance: 60 Ω ± 15%		
2	RCOMP Resistor Value: R1 = 52.3 Ω ± 1%		
3	RCOMP Resistor Tied to: VCC = 1.5		

NOTES:
1. Refer to Section 9.3.

18.6.3.2 RCOMP Resistor Values for Intel® 82547EI Chipset Platform

#	Layout Recommendations[1]	Yes	No
1	Trace Impedance: 60 Ω ± 15%		
2	RCOMP Resistor Value: R2 = 30.0 Ω ± 1%		
3	RCOMP Resistor Tied to: VCC = 1.2		

NOTES:
1. Refer to Section 9.3.

18.7 Intel® ICH5

18.7.1 IDE Interface

#	Layout Recommendations[1]	Yes	No
1	5-mil wide and 7-mil spaces (using given example 4-layer 4.3-mil prepreg stack up).		
2	Max trace length is 10 inches long.		
3	The two strobe signals must be matched within 100 mils of each other. The data lines must be within ± 450 mils of the average length of the two strobe signals.		
4	If series resistors are used, they should be placed close to the connector.		

NOTES:
1. Refer to Section 10.2.

18.7.2 SATA Interface

#	Layout Recommendations[1]	Yes	No
1	Route SATA signals ground referenced.		
2	Route SATA signals using a minimum of vias and corners. This reduces signal reflections and impedance changes. Use a maximum of 2 vias per trace. Vias should be matched on traces within a transmit or receive pair.		
3	When it becomes necessary to turn 90 degrees, use two 45 degree turns or an arc instead of making a single 90 degree turn. This reduces reflections on the signal by minimizing impedance discontinuities.		
4	Do not route SATA traces under crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use and/or duplicate clocks.		
5	Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to SATA signals, high-speed clocks, as well as slower signals that might be coupling to them.)		
6	Keep SATA signals clear of the core logic set. High current transients are produced during internal state transitions that can be very difficult to filter out.		
7	Keep traces at least 90 mils away from the edge of the plane (VCC or GND depending on which plane to which the trace is routed). This helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB.		
8	Maintain parallelism between SATA differential signals with the trace spacing needed to achieve 100 Ω differential impedance. (Recommended: 5 on 7 spacing with 4-layer, 4.3-mil prepreg stack-up.)		
9	Minimize the length of high-speed clock and periodic signal traces that run parallel to SATA signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 50 mils.		
10	Use 20-mil minimum spacing between SATA signal pairs and other signal traces. This helps to prevent crosstalk.		

#	Layout Recommendations[1]	Yes	No
11	SATA signal pair traces should be trace length matched. Max trace length mismatch between SATA signal pair (such as TXN and TXP) should be no greater than 150 mils.		
12	Trace lengths from the Intel® ICH5 to the SATA connector should be between 0.5 – 4 inches.		
13	SATARBIASP and SATARBIASN should be routed 5 on 5 with a single trace 500 mils or less to the 24.9 Ω 1% resistor to ground.		

NOTES:
1. Refer to Section 10.4.

18.7.3 AC '97

#	Layout Recommendations[1]	Yes	No
1	Z_0 AC97 = 60 Ω ± 15%		
2	5-mil trace width, 5-mil spacing between traces (using given example 4-layer 4.3 mil prepreg stack-up).		
3	*AC_SDIN Max Trace Lengths:* • Intel® ICH5 to primary codec: L = 14 inches • From Primary Codec T junction to CNR: L = 6 inches • CNR: L = 14 inches. (Using given example 4-layer 4.3-mil prepreg stack-up.)		
4	*AC_SDOUT Max Trace Lengths:* • ICH5 to primary codec: L = 14 inches • CNR: L = 14 inches. (Using given example 4-layer 4.3-mil prepreg stack-up.)		
5	*AC_BIT_CLK Max Trace Lengths*: • ICH5 to primary codec: L = 13.6 inches • CNR L = 13.6 inches. (Using given example 4-layer 4.3-mil prepreg stack-up.)		
6	Series termination resistor on AC_BIT_CLK line should be no more than 0.9 inch to 7.6 inches from the ICH5.		
7	Series termination resistors on AC_SDIN lines if needed should be no more than 100 to 400 mils from the CNR card or the on board codec.		

NOTES:
1. Refer to Section 10.5.

18.7.4 USB 2.0

#	Layout Recommendations[1]	Yes	No
1	With minimum trace lengths, route high-speed clock and USB differential pairs first.		
2	Route USB signals ground referenced.		
3	Route USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.		
4	When it becomes necessary to turn 90 degrees, use two 45-degree turns or an arc instead of making a single 90-degree turn. This reduces reflections on the signal by minimizing impedance discontinuities.		
5	Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use and/or duplicate clocks.		
6	Stubs on USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs on a given data line should not be greater than 200 mils.		
7	Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.)		
8	Keep USB signals clear of the core logic set. High current transients are produced during internal state transitions, which can be very difficult to filter out.		
9	Keep traces at least 90 mils away from the edge of the plane (Vcc or GND depending on which plane to which the trace is routed). This helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB.		
10	Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. (Recommended: 7.5 on 7.5 spacing with 4-layer, 4.3-mil prepreg stack-up.)		
11	Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 50 mils.		
12	Use 20 mil minimum spacing between USB signal pairs and other signal traces. This helps to prevent crosstalk.		
13	USB signal pair traces should be trace length matched. Maximum trace length mismatch between USB signal pair (such as DM1 and DP1) should be no greater than 150 mils.		
14	No termination resistors needed for USB.		
15	USBRBIAS and USBRBIAS# should be routed 5 on 5 with a single trace 500 mils or less to the 22.6 Ω 1% resistor to ground.		
16	Maximum length from the Intel® ICH5 to the back panel should not be greater than 17 inches. Maximum length from the ICH5 to the CNR should not be greater than 8 inches.		

NOTES:
1. Refer to Section 10.7.

18.7.5 PCI

#	Layout Recommendations[1]	Yes	No
1	For 2 to 4 slot boards (5 to 10 inches to the first slot and then 1 inch to each subsequent slot). For 5 slot boards (5 to 8 inches to the first slot and then 1 inch to each subsequent slot). For 6 slot boards (5 to 7 inches to the first slot and then 1 inch to each subsequent slot).		
2	IDSEL (See Section 10.10.1)		

NOTES:
1. Refer to Section 10.10.

18.7.6 RTC

#	Layout Recommendations[1]	Yes	No
1	RTC LEAD length = 1 inch Max.		
2	Minimize capacitance between RTCX1 and RTCX2.		
3	Put GND plane underneath Crystal components.		
4	Do not route switching signals under the external components (unless on other side of board).		
5	RTC traces should be ground referenced.		

NOTES:
1. Refer to Section 10.11.

18.7.7 LAN Connect Interface

#	Layout Recommendations[1]	Yes	No	Comments
1	Trace spacing: 5 mils wide, 10 mil (using given example 4-layer 4.3-mil prepreg stack-up).			
2	*Point-to- Point Single Solution* Maximum trace lengths: Intel®ICH5 to Intel® 82562EZ/ET/EX/EM: L = 0.5 to 11.5 inches. ICH5 to CNR: L = 2 to 9 inches.			To meet timing requirements.
3	*LOM and CNR Solution* Maximum trace lengths: ICH5 to resistor pack: L1 = 0.5 to 8 inches. Resistor pack to 82562EZ/ET/EX/EM: L2 = 4 to (11.5 – L1) inches. Resistor pack to CNR: L2 = 1.5 to (9 – L1) inches.			To meet timing requirements.
4	Stubs due to R-pak CNR/LOM stuffing option should not be present.			To minimize inductance.
5	Data signals must be equal to or no more than 0.5 inch shorter than the LAN CLK trace. Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inch.			To meet timing and signal quality requirements.
6	Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN PHY.			To meet timing and signal quality requirements.
7	Keep the total length of each differential pair (from PHY to connector) under 4 inches (preferably less than 2 inches).			Issues found with traces longer than 4 inches: IEEE phy conformance failures, excessive EMI and or degraded receive BER.
8	Do not route the transmit differential traces closer than 100 mils to the receive differential traces.			To minimize crosstalk.
9	Distance between differential traces and any other signal line is 100 mils (300 mils recommended).			To minimize crosstalk.
10	Route 5 mils on 10 mils for differential pairs (out of LAN phy) (using given example 4-layer 4.3-mil prepreg stack-up).			To meet timing and signal quality requirements.
11	Differential trace impedance should be controlled to be ~100 Ω.			To meet timing and signal quality requirements.
12	For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, it is recommended to use two 45-degree bends.			To meet timing and signal quality requirements.
13	Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.			This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.

#	Layout Recommendations[1]	Yes	No	Comments
14	Do not route traces and vias under crystals or oscillators.			This will prevent coupling to or from the clock.
15	Trace width to height ratio above the ground plane should be between 1:1 and 3:1.			To control trace EMI radiation.
16	Traces between decoupling and I/O filter capacitors should be as short and wide as practical.			Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.
17	Vias to decoupling capacitors should be sufficiently large in diameter.			To decrease series inductance.
18	Avoid routing high-speed LAN near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.			To minimize crosstalk.
19	Isolate I/O signals from high-speed signals.			To minimize crosstalk.
20	Place the Intel® 82562ET/EM part more than 1.5 inches away from any board edge.			This minimizes the potential for EMI radiation problems.
21	Place at least one bulk capacitor (4.7 µF or greater OK) on each side of the 82562ET/EM.			Research and development has shown that this is a robust design recommendation.
22	Place decoupling capacitors (0.1 µF) as close to the 82562ET/EM as possible.			

NOTES:
1. Refer to Section 10.12.

18.8 Flash BIOS Interface

18.8.1 Flash BIOS Decoupling

#	Layout Recommendations[1]	Yes	No
1	0.1 µF capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins.		
2	4.7 µF capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins.		

NOTES:
1. Refer to Section 14.2.

18.8.2 Processor / Intel® ICH5 Flash BIOS

#	Layout Recommendations[1]	Yes	No
1	Trace Impedance: 60 Ω ± 15%, Trace Spacing: 5 mils, L1: 17 inches max, L2: 2” max, L3: 10 inches max		

NOTES:
1. Refer to Section 14.4.

18.9 Power Distribution

18.9.1 Power Delivery

Signal	Layout Recommendations	Yes	No	Comments
VCC_CPU Processor Core VTT	The VCC_CPU power plane is used to power the processor core and VTT. The processor’s voltage regulator must be compatible with a VRD 10.0 design.			Refer to Section 15.2.1
MCH_VTT	When an Intel® Pentium® 4 processor on 90 nm process is inserted into the platform, the output of the MCH_VTT regulator should be set to 1.225 V. When an Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process is inserted into the platform, the output of the MCH_VTT regulator should be set to 1.45 V. This regulator must be able to source 2 A and sink 600 mA in normal operation.			Refer to Section 15.2.2
VCCVID Processor VID	VCCVID is a 1.2 V power plane used to power pins AF4 and AF3 on the processor. It is derived form 3.3 V and should be able to source 150 mA of current. This regulator is required for all designs.			Refer to Section 15.2.3
2.6 V Dual DDR Core	The 2.6 V dual power plane is used to provide power to the DDR DRAM core, the MCH DDR I/O ring, reference voltage to the 1.25 V linear regulator, and the 2.6 V to 1.5 V linear regulator. The 2.6 V power plane is created using a switch between a switching regulator and a linear stand-by regulator. The switching regulator should be able to support up to 19.5 A of current while the stand-by regulator needs only to supply 500 mA of current. The switching regulator receives its input directly from the 5 V power rail of the power supply while the linear regulator receives its input form 5 V SB. The DDR DRAM VDD and VDDQ requires at most 13 A of current in the S1state. The current dedicated for the MCH’s VCC_2.6 is 4.9 A.			Refer to Section 15.2.4

Signal	Layout Recommendations	Yes	No	Comments
1.3 V DDR TERM	The 1.3 V voltage regulator is for the DDR termination voltage (VTERM). A linear regulator divides the 2.6 V power rail by 2 to drive a 1.3 V reference voltage. VTERM is defined as: VTERM_min = SMVREF – 40 mV and VTERM_max = SMVREF + 40 mV. By deriving the VTERM voltage form the 2.6 V plane, this provides some common mode noise rejection between the DDR termination and I/O voltages. The entire power plane requires 1.8 A of current, and can be delivered a couple of different ways. One way is to use two regulators, one for each channel or one regulator for both channels.			Refer to Section 15.2.5
1.5 V CONN	The 1.5 V power plane is created using a dual linear regulator sourcing from the 2.6 V power rail. The 1.5 V plane powers the Intel® ICH5 core logic and HI, the MCH core, HI, CSA, AGP, and the AGP Connector. Sequencing on this rail should ensure that the 1.5 V power plane is shut off during S3. This voltage rail requires approximately 6.6 A maximum current. This regulator is required in all designs.			Refer to Section 15.2.6
5 V DUAL	This rail will powered from the 5 V core ATX supply during full-power operation and from 5 V SB during STR. There is a resistive drop through the 5 V dual w\switch that must be considered. Therefore, no components should be connected directly to the 5 V dual plane.			Refer to Section 15.2.7
5 V SB (Standby)	The 5 V SB power plane comes directly off the 5 V SB power rail from the ATX power supply and has two functions. One function is to provide power to resume functions via a 3.3 V SB regulator in I/O devices off of the ICH5, and the other function is to provide 2.6 V power to the memory devices during the S3 state. The ICH5 requires 3.3 V SB only due to the integrated 1.5 V SB regulator. It is recommended that the ATX power supply be capable of handling 2 A of SB current.			Refer to Section 15.2.8
3.3 V SB (Standby)	The 3.3 V SB power plane is the output of a 5 V SB-to-3.3 V SB voltage regulator. The 3.3 V SB plane powers the resume well of the ICH5 and the PCI 3.3 VAUX suspend power pins. The 3.3 VAUX requirements state that during suspend, the system must deliver 375 mA to each wake-enabled card and 20 mA to each non-wake enabled card. During full-power operation, the system must be able to supply 375 mA to each card. Therefore, the total requirement is: Full-power Operation: 375 mA *(# of PCI slots) Suspend Operation: 375 mA+20 mA* (#PCI slots-1)			Refer to Section 15.2.9

Signal	Layout Recommendations	Yes	No	Comments
2.6 V SB (Standby)	The 2.6 V SB power plane is the output of the 5 V SB-to-2.6 V SB voltage regulator. The power plane is used solely for the DDR DIMMs during the S3 suspend state (some minimal 2.6 V rail current will also be supplied to the MCH). The suspend voltage regulator for system memory is controlled by the LATCHED_BACKFEED_CUT signal. This signal should be generated using the SLP_S4# signal from the ICH5, rather than the SLP_S5# signal, even if the platform does not support the S4 Sleep State. The SLP_S4# logic in the ICH5 ensures that system memory will be properly initialized when returning from S4 and S5 states.			Refer to Section 15.2.10

18.9.2 Decoupling Requirements

Signal	Layout Recommendations[1]	Yes	No
AL Polymer 560 µF	10 capacitors, ESR: 5 mΩ, ESL: 4 nH, Filter: Output		
1206 pkg 22 µF X5R	24 capacitors, ESR: 3.5 mΩ, ESL: 1.4 nH, Filter: Output		
Al Electrolytic 1200 µF 16 V 2.1 A Ripple	4 capacitors, ESR: 22 mΩ, ESL: 30 nH, Filter: Input		
1206 pkg 4.7 µF	4 capacitors, ESR: 6 mΩ, ESL: 1.1 nH, Filter: Input		

NOTES:
1. Refer to Section 15.3.1.2.

18.9.3 MCH Power Delivery

18.9.3.1 Decoupling Recommendations

Signal	Layout Recommendations[1]	Yes	No
MCH_VTT	(1) 0.47 µF edge capacitor as close to ball A15 (1) 0.47 µF edge capacitor as close to ball A21 (1) 0.1 µF edge capacitor as close to ball A31 (1) 0.1 µF power plane decoupling capacitor as close to MCH		
VCC_1.5 HI AGP, CSA	(1) 0.1 µF edge capacitor as close to ball AA35 (1) 0.1 µF edge capacitor as close to ball Y1		
VCC_2.6 DDR	(1) 0.1 µF edge capacitor as close to ball AA35 (1) 0.47 µF edge capacitor as close to ball E35 (1) 0.22 µF edge capacitor as close to ball R35 (1) 0.1 µF edge capacitor as close to ball AL35 (1) 0.1 µF edge capacitor as close to ball AR15 (1) 0.1 µF edge capacitor as close to MCH		

NOTES:
1. Refer to Section 15.3.3.4.

18.9.3.2 Bulk Decoupling Requirements

Signal	Layout Recommendations[1]	Yes	No
MCH_VTT	(1) 0.1 µF, (1) 0.47 µF, (1) 1.0 µF, (2) 4.7 µF, (1) 470 µF. Place on MCH VTT plane using good layout practices. That is, place the smaller value capacitors closer to the MCH than the higher value capacitors.		
VCC_2.6	(1) 22 µF, (1) 4.7 µF Place at the 2.6 V power plane transitions to layer 1 at the MCH.		
VCC_1.5	10 µF, 470 µF, 4.7 µF Place as close to where the 1.5 V core and 1.5 V AGP/CSA planes diverge. Place at the output of the 1.5 V VR. Place between the VR and the MCH.		

NOTES:
1. Refer to Section 15.3.3.4.

18.9.4 DDR DIMM Power Delivery

18.9.4.1 Decoupling Requirements

Signal	Layout Recommendations[1]	Yes	No
VCC_2.6	(21) 0.1 µF Decoupling capacitors Place as close to power the DIMM power pins as possible and sprinkled through out the DDR power flood.		
VTT_1.3	(27) 0.1 µF Decoupling capacitors Place as close to termination resistors as possible.		

NOTES:
1. Refer to Section 15.3.5.3.

18.9.4.2 Bulk Decoupling for DIMMs

Pin	Layout Recommendations[1]	Yes	No
VCC_2.6	(1) 4.7 µF, (1) 22 µF, (1) 333 µF, (1) 560 µF: Place at output of the VR as close to the DIMMs as possible: (4) 470 µF: Place at each corner of the DIMMs		
VTT_1.3	(1) 4.7µF, (1) 470 µF, (1) 1500 µF. Place at output of the VR as close to the DIMMs as possible		

NOTES:
1. Refer to Section 15.3.5.3.

18.9.5 Intel® ICH5 Power Delivery

18.9.5.1 Decoupling Requirements

Signal	Layout Recommendations[1]	Yes	No
VCC3_3	(6) 0.1 µF decoupling capacitors (VSS) Place near balls D1, A7, H1, P1, W24, and AD 21.		
VccSus3_3	(3) 0.1 µF, (1) 0.01 µF, (1) 1.0 µF decoupling capacitors (VSS) Place 0.1 µF capacitors near balls A17, A23, and V1. Place additional capacitors near balls A15 and A19.		
V_CPU_IO	(1) 0.1 µF decoupling capacitors (VCC) Place near balls T24		
VCC1_5	(4) 0.1 µF, (1) 0.01 µF decoupling capacitors (VSS) Place 0.1 µF capacitors near balls G24, H24, K24, M24, AD4, and AD18. Place 0.01 µF capacitor near balls AD8.		
VccSus1_5_A	(1) 0.01 µF decoupling capacitors (VSS) Place near balls A19.		
VccSus1_5_B	(1) 0.01 µF decoupling capacitors (VSS) Place near balls AD4.		
VccSus1_5_C	(1) 0.01 µF decoupling capacitors (VSS) Place near balls A7.		
V5REF	(1) 0.1 µF decoupling capacitors (VCC) Place near balls A8.		
V5REF_Sus	(1) 0.1 µF decoupling capacitors (VSS) Place near balls A17.		
VCCRTC	(1) 0.1 µF decoupling capacitors (VCC) Place near balls AD11.		
VCCUSBPLL	(1) 0.1 µF, (1) 0.01 µF decoupling capacitors (VSS) Place near balls D24.		
VCCSATAPLL	(1) 0.1 µF, (1) 0.01 µF decoupling capacitors (VSS) Place near balls AD6.		

NOTES:
1. Refer to Section 15.3.6.7.

Reference Schematics A

Refer to the appropriate schematics document (*Intel® 848P Chipset Customer Reference Board Schematics, Intel® 865G/865GV/865PE/865P Chipset CRB Schematics Addendum for the Intel® Pentium® 4 Processor on 90 nm Process w/Loadline A Platforms 2 Phase*, or *Intel® 865G/865GV/865PE/865P Chipset CRB Schematics Addendum for the Intel® Pentium® 4 Processor on 90 nm Process w/Loadline A Platforms 3 Phase)* for the Customer Reference Board (CRB) schematic diagrams (see Section 1.1).