Intel® 848P Chipset

Platform Design Guide Update

For use with the Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process and the Intel® Pentium® 4 Processor on 90 nm Process

March 2004

Notice: The Intel® 848P chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 254080-004

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Contents

Contents 3

Revision History 4

Preface 5

General Design Considerations 7

Schematic, Layout, and Routing Updates 9

Documentation Changes 11

Revision History

Revision	Draft/Changes	Date
-001	Initial Release	November 2003
-002	Documentation change, New Checklist Items for Section 17.4, MCH / Miscellaneous Schematic Checklist, moved to Intel® 848P Chipset Design Guide, 253576-003	February 2004
-003	Added Documentation Change 1 and 2	February 2004
-004	Added Documentation Change 3	March 2004

Preface

This public Design Guide Update document is an update to the specifications and information contained in the *Intel® 848P Chipset Platform Design Guide*, August 2003, Document Number 253576-002. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2003. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public design guide update document when the public design guide document is first published. This design guide update document contains a complete list of all known information types.

Affected Documents

Document Title	Document Number
Intel® 848P Chipset Platform Design Guide, February 2004	253576-002

Related Documents

Document Title	Document Number
Intel® 848P Chipset Datasheet, Intel® 82848P Memory Controller Hub (MCH), February 2004	253575-002
Intel® 82801EB I/O Controller Hub 5 (ICH5) / Intel® 82801ER I/O Controller Hub 5R (ICH5R) Datasheet, April 2003	252516-001

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 848P Chipset: 82848P Memory Controller Hub (MCH).

Schematic, Layout, and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Doc:	Document change or update that will be implemented.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
		There are no General Design Consideration changes in this Design Guide Update revision.

NO.	Plans	SCHEMATIC, LAYOUT, AND ROUTING UPDATES
		There are no Schematic, Layout, And Routing Updates changes in this Design Guide Update revision.

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Revised Checklist Item for Section 17.1.3, Processor Connector Only Items, Item VIDPWRGD
2	Doc	In Section 5.1.6.10, replace Figure 46 “Routing Illustration for BOOTSELECT”
3	Doc	Revised Section 18.1.2, Processor Connector/Intel® ICH5 Items, PWRGOOD

General Design Considerations

There are no General Design Considerations in this Design Guide Update revision.

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Schematic, Layout, and Routing Updates

There are no Schematic, Layout, and Routing Updates in this design guide update revision.

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Documentation Changes

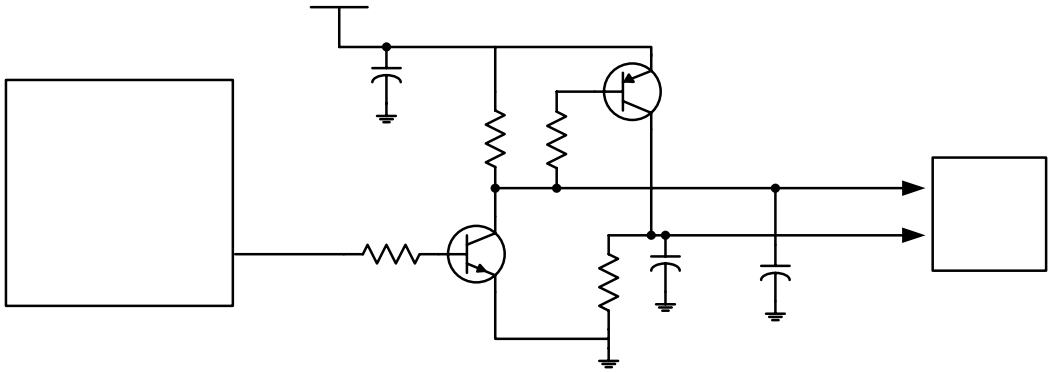
1. Revised Checklist Item for Section 17.1.3, Schematic Checklist, Processor Connector Only Items, item VIDPWRGD

Replace Section 17.1.3, Schematic Checklist, Processor Connector Only Items, item VIDPWRGD with the following:

Checklist Items	Connections/Recommendations	Reason/Impact
VIDPWRGD	Connect to power good output of the 1.2V linear supply w/ 681Ω, 1% pull-up.	

2. Replace Figure 46 "Routing Illustration for BOOTSELECT"

In Section 5.1.6.10 on page 80, replace Figure 46 "Routing Illustration for BOOTSELECT" with the following:



3. Revise Section 18.1.2, Schematic Checklist, Processor Connector/Intel® ICH5 Items, PWRGOOD

Revise Section 18.1.2, Schematic Checklist, Processor Connector/Intel® ICH5 Items, Connections/Recommendations, PWRGOOD, as follows:

Checklist Items	Connections/Recommendations
PWRGOOD	Connects to CPUPWRGD/GPO49 in ICH5. Note that a weak pullup to VCCP (V_CPU_IO) is required and that such value should not exceed ICH5s Ioh2/Iol2 specs.