# Intel® 810E2 Chipset Platform

## Design Guide

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# Revision History

| Rev. | Description | Date |
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| -001 | • Initial Release | January 2001 |
| -002 | • Replaced Figure 84. Power Delivery Map<br>• Revised Section 7.2.6, ICH2 Checklist, Interrupt interface, APIC<br>• Revised Section 7.2.16, Power, ICH2 Checklist: Recommendations for 5V_REF_SUS<br>• Revised Section 6.4.3, 3.3V/5VREF Sequencing<br>• Added Section 3.20.8, Power-well Isolation Control<br>• Revised Figure 49. Trace Routing in General Trace Routing Considerations, Section 3.21.2.1<br>• Added SUSCLK to ICH2 Checklist Section 7.2.13, RTC<br>• Added Section 6.5, Power_Supply PS_ON Considerations<br>• Revised ICH2 Checklist Section 7.2.9, Power Management<br>• Revised Section 3.15, USB<br>• Added RTCRST# to ICH2 Checklist Section 7.2.13, RTC<br>• Added 82562ET/EM Disable Guidelines, Section 3.21.4.6<br>• Revised Section 3.22.2., FWH Vpp Design Guidelines<br>• Revised Section 3.21.5, 82562ET / 82562EH Dual Footprint Guidelines<br>• Revised Section 3.1, General Recommendations<br>• Revised ICH2 Checklist Section 7.2.13, RTC, RTCX1-RTCX2<br>• Revised RTC Crystal, Section 3.20.1<br>• Revised ICH2 Checklist, Section 7.2.9, Power Management, PWRBTN#<br>• Revised ICH2 Checklist, PCI Interface, Section 7.2.1, PME#<br>• Revised VCCcore Decoupling Design, Section 2.2.10.1<br>• Revised Figure 23 and Figure 24 in Compensation, Section 3.6.4<br>• Revised 82562ET / 82562EH Dual Footprint Guidelines, Section 3.21.5<br>• Revised 82562ET / 82562EM Termination Resistors, Section 3.21.4.3<br>• Revised General Trace Routing Considerations, Section 3.21.2.1<br>• Revised Table 23, in Point-To-Point Interconnect, Section 3.21.1.2<br>• Revised LAN Layout Guidelines, Section 3.21 | August 2002 |

# 1. Introduction

This design guide provides motherboard design guidelines for Intel® 810E2 chipset systems. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. In addition to design guidelines, this document discusses 810E2 chipset system design issues (e.g., thermal requirements).

The debug recommendations should be consulted when debugging an 810E2 chipset system. However, the debug recommendations should be understood before completing board design to ensure that the debug port, in addition to other debug features, will be implemented correctly.

## 1.1. About This Design Guide

This design guide is intended for hardware designers who are experienced with PC architectures and board design. The design guide assumes that the designer has a working knowledge of the vocabulary and practices of PC hardware design.

- Chapter 1, “Introduction”—This chapter introduces the designer to the organization and purpose of this design guide, and provides a list of references of related documents. This chapter also provides an overview of the 810E2 chipset.
- Chapter 2, “PGA370 Processor Design Guidelines”—This chapter provides design guidelines for the PGA370 processor including processor-specific layout guidelines.
- Chapter 3, “Layout and Routing Guidelines”—This chapter provides a detailed set of motherboard layout and routing guidelines, except for processor-specific layout guidelines. The motherboard functional units are covered (e.g., chipset component placement, system bus routing, system memory layout, display cache interface, hub interface, IDE, AC’97, USB, interrupts, SMBUS, PCD, LPC/ FWH Flash BIOS, and RTC). For the PGA370 processor specific layout guidelines, refer to Chapter 2.
- Chapter 4, “Advanced System Bus Design”—The goal of this chapter is to provide the system designer with the information needed for the implementation of 133 MHz and 100 MHz single processor AGTL+ bus PCB layout.
- Chapter 5, “Clocking”— This chapter provides motherboard clocking guidelines (e.g., clock architecture, routing, capacitor sites, clock power decoupling, and clock skew).
- Chapter 6, “Power delivery” — This chapter includes guidelines regarding power delivery, decoupling, thermal, and power sequencing.
- Chapter 7, “Design Checklist”— This chapter provides a design review checklist. ATA/66 and ATA/100 detection, calculation of pull-up/pull-down resistors, minimizing RTC ESD, and power management signals are also discussed.
- Chapter 8, “Flixible Motherboard Guidelines”— This chapter includes guidelines regarding power deliver, decoupling, thermal, and power sequencing.
- Chapter 9, “Third Party Vendor Information”— This chapter includes information regarding various third-party vendors who provide products to support the 810E2 chipset.
- Appendix A, “Intel® 810E2 Chipset Platform Reference Schematics”— This appendix includes schematics for the 810E2 Reference Board

| Term | Definition |
|---|---|
| Suspend-To-RAM (STR) | In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered. |
| Full-power operation | During *full-power* operation, all components on the motherboard remain powered. Note that *full-power* operation includes both the *full-on* operating state (S0) and the processor Stop Grant state (S1). |
| Suspend operation | During *suspend* operation, power is removed from some components on the motherboard. The customer reference board supports three suspend states: processor Stop Grant (S1), Suspend-to-RAM (S3) and Soft-off (S5). |
| Power rails | An ATX power supply has 6 power rails: +5V, -5V, +12V, -12V, +3.3V, +5VSB. In addition to these power rails, several other power rails can be created with voltage regulators. |
| Core power rail | A power rail that is only on during *full-power* operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed *directly* from the ATX power supply are: ±5V, ±12V and +3.3V. |
| Standby power rail | A power rail that in on during *suspend* operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed *directly* from the ATX power supply is 5VSB (5V Standby). There can be other standby rails that are created with voltage regulators. |
| Derived power rail | A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3VSB is usually derived (on the motherboard) from 5VSB using a voltage regulator. |
| Dual power rail | A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation. |
| Aggressor | A network that transmits a coupled signal to another network is called the aggressor network. |
| AGTL+ | The processor system bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors for providing the high logic level and termination. The processor AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition. Additionally, the processor Single Edge Connector (S.E.C.) cartridge contains 56 Ω pull-up resistors to provide termination at each bus load. |
| Bus Agent | A component or group of components that, when combined, represent a single load on the AGTL+ bus. |
| Corner | Describes how a component performs when all parameters that could impact performance are adjusted to have the same impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. The results in performance of an electronic component that may change as a result of corners include (but are not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the “slow” corner would mean having a component operating at its slowest, weakest drive strength performance. Similar discussion of the “fast” corner would mean having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance. |

| Term | Definition |
|---|---|
| Crosstalk | The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks.<br>• Backward Crosstalk - coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal.<br>• Forward Crosstalk - coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal.<br>• Even Mode Crosstalk - coupling from multiple aggressors when all the aggressors switch in the same direction that the victim is switching.<br>• Odd Mode Crosstalk - coupling from multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching. |
| Edge Finger | The cartridge electrical contact that interfaces to the SC242 connector. |
| Flight Time | Flight Time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the $T_{CO}$ of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver.<br>More precisely, *flight time* is defined to be:<br>The time difference between a signal at the input pin of a receiving agent crossing $V_{REF}$ (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.), and the output pin of the driving agent crossing $V_{REF}$ if the driver was driving the Test Load used to specify the driver's AC timings.<br>See Section 4.1 for details regarding flight time simulation and validation.<br>The $V_{REF}$ Guardband takes into account sources of noise that may affect the way an AGTL+ signal becomes valid at the receiver. See the definition of the $V_{REF}$ Guardband.<br>• **Maximum and Minimum Flight Time** - Flight time variations can be caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, $V_{TT}$ noise, $V_{REF}$ noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of *Simultaneous Switching Output (SSO)* and packaging effects.<br>— The **Maximum Flight Time** is the largest flight time a network will experience under all variations of conditions. Maximum flight time is measured at the appropriate $V_{REF}$ Guardband boundary.<br>— The **Minimum Flight Time** is the smallest flight time a network will experience under all variations of conditions. Minimum flight time is measured at the appropriate $V_{REF}$ Guardband boundary.<br>For more information on flight time and the $V_{REF}$ Guardband, see the *Intel® Pentium® II Processor Developer's Manual.* |
| GTL+ | GTL+ is the bus technology used by the Pentium Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) technology. See the *Intel® Pentium® II Processor Developer's Manual* for more details of GTL+. |
| Network | The trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components. |
| Network Length | The distance between extreme bus agents on the network and does not include the distance connecting the end bus agents to the termination resistors. |
| Overdrive Region | Is the voltage range, at a receiver, located above and below $V_{REF}$ for signal integrity analysis. See the *Intel® Pentium® II Processor Developer's Manual* for more details. |
| Overshoot | Maximum voltage allowed for a signal at the processor core pad. See each processor's datasheet for overshoot specification. |

| Term | Definition |
|---|---|
| Pad | A feature of a semiconductor die contained within an internal logic package on the S.E.C cartridge substrate used to connect the die to the package bond wires. A pad is only observable in simulation. |
| Pin | A feature of a logic package contained within the S.E.C. cartridge used to connect the package to an internal substrate trace. |
| Ringback | Ringback is the voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, etc. See the respective processor's datasheet for ringback specification. |
| Settling Limit | Defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. See the respective processor's datasheet for settling limit specification. |
| Setup Window | Is the time between the beginning of Setup to Clock ($T_{SU\_MIN}$) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system. |
| Simultaneous Switching Output (SSO) Effects | Refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "pushout"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects. |
| Stub | The branch from the trunk terminating at the pad of an agent. |
| Test Load | Intel uses a 50 Ω test load for specifying its components. |
| Trunk | The main connection, excluding interconnect branches, terminating at agent pads. |
| Undershoot | Maximum voltage allowed for a signal to extend below $V_{SS}$ at the processor core pad. See the respective processor's datasheet for undershoot specifications. |
| Victim | A network that receives a coupled crosstalk signal from another network is called the victim network. |
| $V_{REF}$ Guardband | A guardband ($DV_{REF}$) defined above and below $V_{REF}$ to provide a more realistic model accounting for noise such as crosstalk, $V_{TT}$ noise, and $V_{REF}$ noise. |

### 1.1.1. References

- Intel® 810E Chipset: 82810E Graphics and Memory Controller Hub (GMCH) Datasheet (Document Number: 290676)
- Intel® 82801BA I/O Controller Hub (ICH2) Datasheet (Document Number: 290687)
- Intel® 82802AB/AC Firmware Hub (FWH) Datasheet (Document Number: 290658)
- Intel® Celeron® Processor Datasheet (Document Number: 243658)
- Intel® Celeron® Processor Specification Update (Document Number: 243748)
- Intel® 810E Chipset Clock Synthesizer/Driver Specification
- PPGA 370 Power Delivery Guidelines
- Intel® Pentium® II Processor AGTL+ Guidelines (Document Number: 243330)
- Intel® Pentium® II Processor Power Distribution Guidelines (Document Number: 243332)
- Intel® Pentium® II Processor Developer's Manual (Document Number: 243341)
- Intel® Pentium® II Processor at 350 MHz, 400 MHz and 450 MHz Datasheet (Document Number: 243657)
- Intel® Pentium® II Processor Specification Update (Document Number: 243337)
- Intel® Pentium® III Processor Datasheet (Document Number: 244452)
- Intel® Pentium® III Processor Specification Update (Document Number: 244453)
- AP-907: Intel® Pentium® III Power Distribution Guidelines (Document Number: 245085)
- PCI Local Bus Specification, Revision 2.2
- Universal Serial Bus Specification, Revision 1.0

## 1.2. System Overview

The 810E2 chipset enhances the performance of the first generation Integrated Graphics chipset designed for the Intel® Celeron® processor and Intel® Pentium® III processor. The graphics accelerator architecture consists of dedicated multi-media engines executing in parallel to deliver high performance 3D, 2D, and motion compensation video capabilities. An integrated centralized memory arbiter allocates memory bandwidth to multiple system agents to optimize system memory utilization. A new chipset component interconnect, the hub interface, is designed into the 810E2 chipset to provide an efficient communication channel between the memory controller hub and the I/O hub controller.

The 810E2 chipset architecture also enables a new security and manageability infrastructure through a Firmware Hub Flash BIOS component.

An ACPI compliant 810E2 chipset platform can support the *Full-on (S0)*, *Stop Grant (S1)*, *Suspend to RAM (S3)*, *Suspend to Disk (S4)*, and *Soft-off (S5)* power management states. Through the use of an appropriate LAN device, the 810E2 chipset also supports *wake-on-LAN** for remote administration and troubleshooting.

The 810E2 chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true *plug-and-play* for the 810E chipset platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC'97 allows the OEM to use *software configurable* AC'97 audio and modem coder/decoders (codecs) instead of the traditional ISA devices.

The 810E2 chipset contains two core components:

- Intel® 82810E Graphics and Memory Controller Hub (GMCH)
- Intel® 82801BA I/O Controller Hub 2 (ICH2)

The GMCH integrates a 66/100/133 MHz, P6 family system bus controller, integrated 2D/3D graphics accelerator, 100 MHz SDRAM controller and a high-speed hub interface for communication with the I/O Controller Hub (ICH2). The ICH2 integrates an Ultra ATA/100 controller, 2 USB host controllers with a total of 4 ports, LPC interface controller, FWH Flash BIOS interface controller, PCI interface controller, AC'97 digital controller and a hub interface for communication with the GMCH.

### 1.2.1. Graphics and Memory Controller Hub (GMCH)

The GMCH provides the interconnect between the SDRAM and the rest of the system logic:

- 421 Mini BGA
- Integrated Graphics controller
- 230 MHz RAMDAC
- Support for the Celeron processor and Pentium III processor with a 66 MHz , 100 MHz, or 133 MHz system bus.
- 100 MHz SDRAM interface supporting 64 MB/256 MB/512 MB with 16Mb/64Mb/128Mb SDRAM technology
- Optional 4 MB Display Cache
- Downstream hub interface for access to the ICH2
- TV-Out/Flat Panel Display support

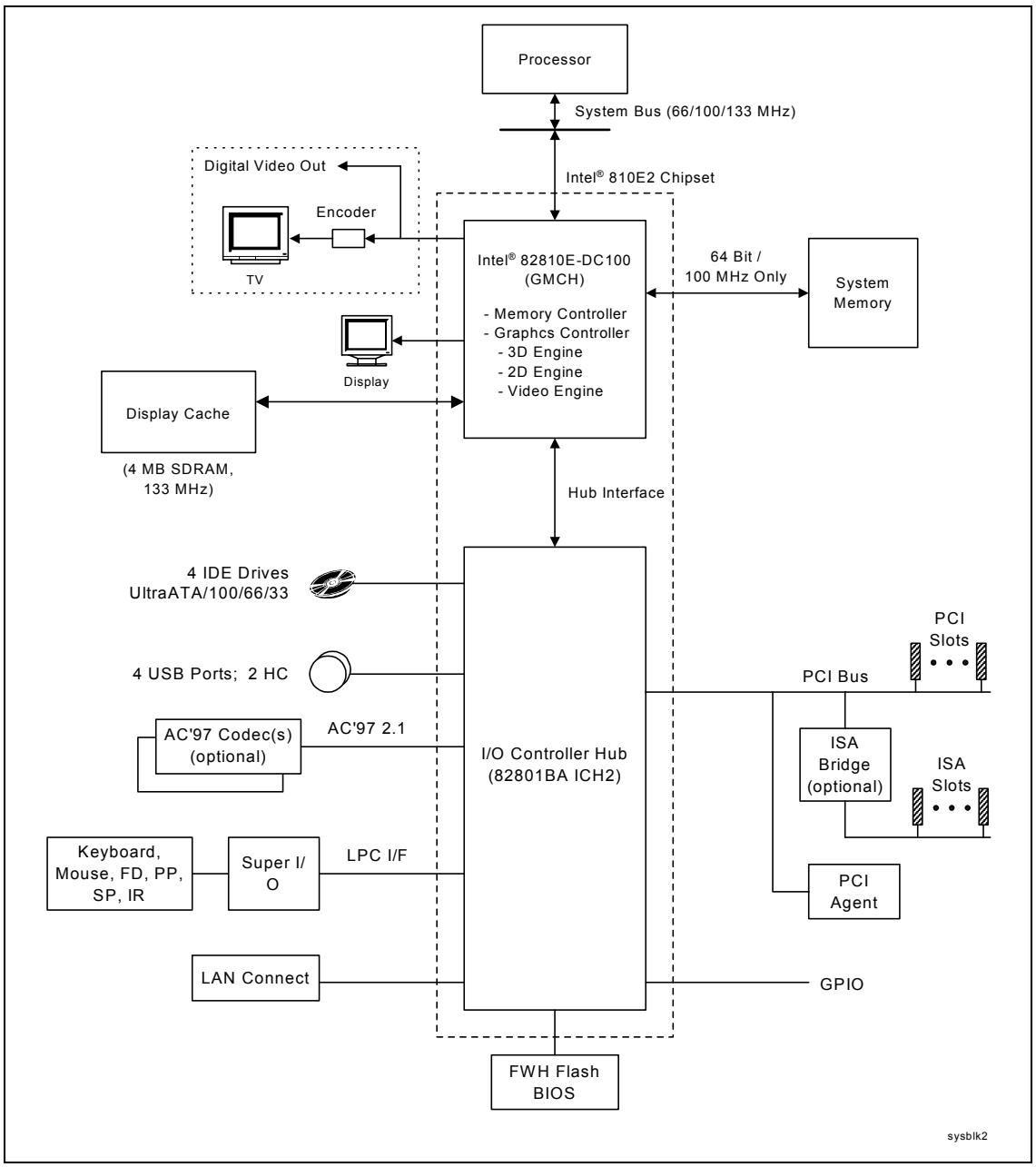
### 1.2.2. Intel® 82801BA I/O Controller Hub 2 (ICH2)

The I/O Controller Hub 2 provides the I/O subsystem with access to the rest of the system:

- Upstream hub interface for access to the GMCH
- PCI 2.2 interface with 6 PCI Req/Grant Pairs
- Bus Master IDE controller; supports Ultra ATA/100
- I/O APIC
- USB controller
- SMBus controller
- FWH interface
- LPC interface
- AC’97 2.1 interface
- Integrated System Management Controller
- Alert-on-LAN
- Interrupt controller
- Packaging / Power
  - 360 EBGA
  - 1.8 V core and 3.3 V standby

## 1.2.3. System Configurations

**Figure 1. Intel® 810E2 Chipset System**



# 1.3. Platform Initiatives

## 1.3.1. Hub Interface

As I/O speeds increase, the demand placed on the PCI bus by the I/O bridge has become significant. With the addition of AC'97 and Ultra ATA/100, coupled with the existing USB, I/O requirements could impact PCI bus performance. The 810E2 chipset's *hub interface architecture* ensures that the I/O subsystem (both PCI and the integrated I/O features such as IDE, AC'97, USB, etc.), receives adequate bandwidth. By placing the I/O bridge on the hub interface (instead of PCI), the hub architecture ensures that both the I/O functions integrated into the ICH2 and the PCI peripherals obtain the bandwidth necessary for peak performance.

## 1.3.2. Integrated LAN Controller

The 810E2 chipset platform incorporates an ICH2 integrated LAN Controller. Its bus master capabilities enable the component to process high-level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor.

The ICH2 functions with several options of LAN connect components to target the desired market segment. The 82562EH provides a HomePNA 1-Mbit/sec connection. The 82562ET provides a basic Ethernet 10/100 connection. The 82562EM provides an Ethernet 10/100 connection with the added flexibility of Alert on LAN.

## 1.3.3. Ultra ATA/100 Support

The 810E2 chipset platform incorporates the ICH2 IDE controller with two sets of interface signals (primary and secondary) that can be independently enabled, tri-stated or driven low. The platform supports Ultra ATA/100 for transfers up to 100 MB/sec, in addition to Ultra ATA/66 and Ultra ATA/33 modes.

## 1.3.4. Expanded USB Support

The 810E2 chipset platform contains two USB Host Controllers. Each Host Controller includes a root hub with two separate USB ports each, for a total of 4 USB ports. The addition of a second USB Host Controller expands the functionality of the platform.

## 1.3.5. SMBus

The ICH2 integrates a SMBus controller. The SMBus provides an interface for managing peripherals such as serial presence detection (SPD) and thermal sensors. The slave interface allows an external microcontroller to access system resources.

## 1.3.6. Interrupt Controller

The interrupt capabilities of the 810E2 chipset platform expand support for up to 8 PCI interrupt pins and PCI 2.2 message-based interrupts. In addition, the ICH2 supports system bus interrupt delivery.

## 1.3.7. Firmware Hub (FWH) Flash BIOS

The 810E2 chipset platform supports firmware hub BIOS memory sizes up to 8 MB for increased system flexibility.

## 1.3.8. AC'97 6-Channel Support

The *Audio Codec '97* (AC'97) Specification defines a digital interface that can be used to attach an *audio codec* (AC), a *modem codec* (MC), an *audio/modem codec* (AMC), or both an AC and a MC. The AC'97 Specification defines the interface between the system logic and the audio or modem codec known as the *AC-link*.

The 810E2 chipset's AC'97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC-link. Using 810E2 chipset's integrated AC-link reduces cost and eases migration from ISA.

By using an audio codec, the AC-link allows for cost-effective, high-quality, integrated audio on the 810E2 chipset platform. In addition, an AC'97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC'97. The 810E2 chipset's integrated digital link allows several external codecs to be connected to the ICH2. The system designer can provide audio with an audio codec, a modem with a modem codec, or an integrated audio/modem codec. The digital link is expanded to support two audio codecs or a combination of an audio and modem codec.

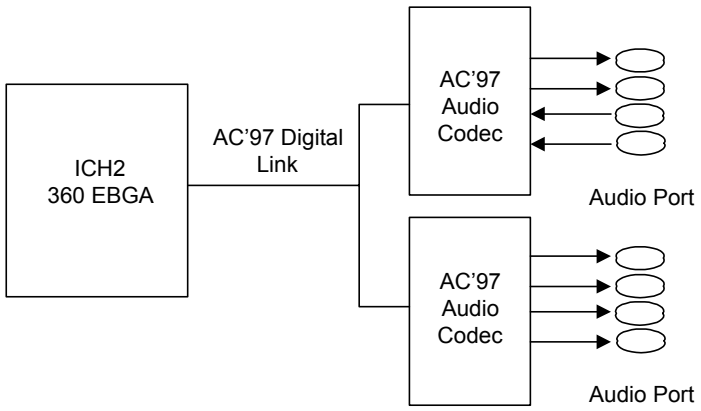
Modem implementation for different countries must be taken into consideration, as telephone systems may vary. By implementing a split design, the audio codec can be on board and the modem codec can be placed on a riser. Intel is developing a Communications and Networking Riser connector.

The digital link in the ICH2 is AC'97 Rev. 2.1 compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high-quality, two-speaker audio solution. Wake-on-ring-from-suspend also is supported with the appropriate modem codec.

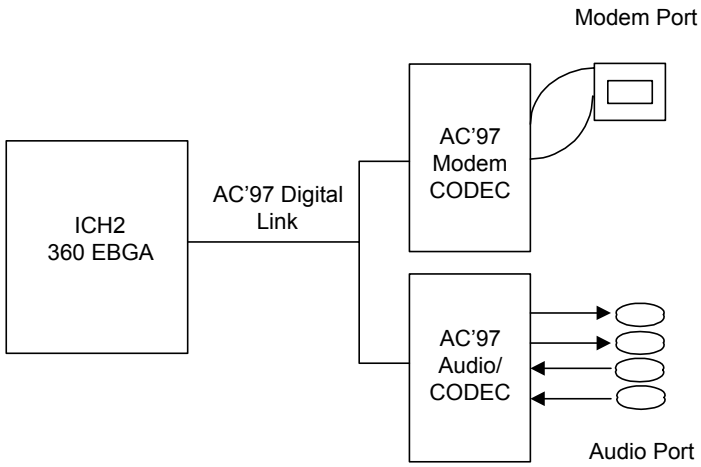
The 810E2 chipset platform expands audio capability with support for up to six channels of PCM audio output (i.e., full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center and Woofer, for a complete surround sound effect. ICH2 has expanded support for two audio codecs on the AC-link.

**Figure 3. AC'97 with Audio and Modem Codec Connections**

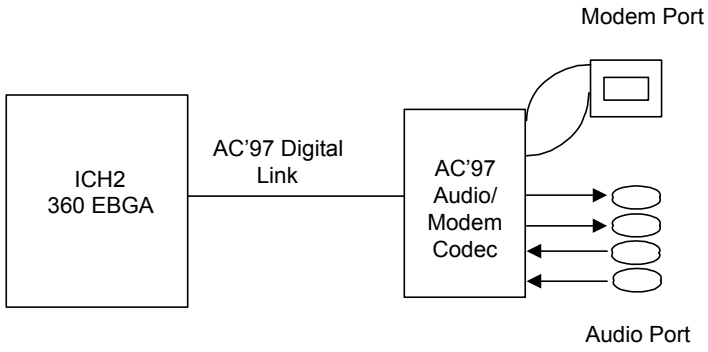
a) AC'97 with Audio Codecs (4-Channel Secondary)




b) AC'97 with Modem and Audio Codecs




c) AC'97 with Audio/Modem Codec




AC97_connections

## 1.3.9. Low Pin Count (LPC) Interface

In the 810E2 chipset platform, the Super I/O (SIO) component has migrated to the Low-Pin-Count (LPC) interface. Migration to the LPC interface allows for lower-cost Super I/O designs. The LPC Super I/O component requires the same feature set as traditional Super I/O components. It should include a keyboard and mouse controller, floppy disk controller, and serial and parallel ports. In addition to the Super I/O features, an integrated game port is recommended because the AC'97 interface does not provide support for a game port. In systems with ISA audio, the game port typically existed on the audio card. The fifteen-pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface. Consult your preferred Super I/O vendor for a comprehensive list of the devices offered and the features supported.

In addition, depending on system requirements, specific system I/O requirements may be integrated into the LPC Super I/O. For example, a USB hub may be integrated to connect to the ICH2 USB output and extend it to multiple USB connectors. Other SIO integration targets include a device bay controller or an ISA-IRQ-to-serial-IRQ converter to support a PCI-to-ISA bridge. Contact your Super I/O vendor to ensure the availability of desired LPC Super I/O features.

# 2. PGA370 Processor Design Guidelines

This chapter provides PGA370 processor design guidelines including the PGA370 socket, Layout Guidelines, BSEL implementation, CLKREF, Undershoot/Overshoot requirements, Reset, Decoupling guidelines, Thermal/EMI differences, and Debug Port changes. The layout guidelines are processor-specific and should be used in conjunction with Chapter 3. For this chapter, the following terminology applies:

- *Legacy PGA370* refers to today's 810 chipset utilizing the PGA370 socket for the microprocessor. In general, these designs support 66/100 MHz host bus operation, *VRM 8.2 DC-DC Converter Guidelines*, and Celeron processors.
- *Flexible PGA370* refers to new generation 810/810E/810E2 chipsets utilizing the PGA370 socket and designed for microprocessor flexibility. In general, these designs support 66/100/133 MHz host bus operation, *VRM 8.4 DC-DC Converter Guidelines* and Celeron processor and Pentium III processor PGA single processor based designs.

## 2.1. Electrical Differences for Flexible PGA370 Designs

There are several electrical changes between the legacy and flexible PGA370 design. They include:

- Changes to the PGA370 socket pin definitions. Pentium III processors utilize a superset of the Celeron processor pin definition.
- Addition of VTT (AGTL+ termination voltage) delivery to the PGA370 socket.
- BSEL[1:0] implementation differences. BSEL1 has been added to select either a 100 MHz or 133 MHz host bus frequency setting from the CK810E clock synthesizer.
- Additional PLL reference voltage, 1.25V, on new CLKREF pin.
- More stringent undershoot/overshoot requirements for CMOS and AGTL+ signals.
- Addition of on-die Rtt (AGTL+ termination resistors) for the Pentium III processor. The requirement remains for on-motherboard Rtt implementation if supporting the Celeronprocessor (PPGA). If only supporting Pentium III processors, the reset signals (RESET#) still requires termination to VTT on the motherboard.

## 2.2. PGA370 Socket Definition Details

The following tables compare legacy pin names and functions to new flexible pin names and functions. Designers need to pay close attention to the notes section for this table for compatibility concerns regarding these pin changes.

## Table 1. Platform Pin Definition Comparison for Single Processor Designs

| Pin # | Legacy PGA370 Pin Name | Flexible PGA370 Pin Name | Function | Type | Notes |
|---|---|---|---|---|---|
| A29 | Reserved | DEP7# | Data bus ECC data | AGTL+, I/O | 2 |
| A31 | Reserved | DEP3# | Data bus ECC data | AGTL+, I/O | 2 |
| A33 | Reserved | DEP2# | Data bus ECC data | AGTL+, I/O | 2 |
| AC1 | Reserved | A33# | Additional AGTL+ address | AGTL+, I/O | 2 |
| AC37 | Reserved | RSP# | Response parity | AGTL+, I | 2 |
| AF4 | Reserved | A35# | Additional AGTL+ address | AGTL+, I/O | 2 |
| AH20 | Reserved | VTT | AGTL+ termination voltage | Power | |
| AH4 | Reserved | RESET# | Processor reset (Intel® Pentium® III processor) | AGTL+, I | 3 |
| AJ31 | GND | BSEL1 | System bus frequency select | CMOS, I/O | 1 |
| AK16 | Reserved | VTT | AGTL+ termination voltage | Power | |
| AK24 | Reserved | AERR# | Address parity error | AGTL+, I/O | 2 |
| AL11 | Reserved | AP0# | Address parity | AGTL+, I/O | 2 |
| AL13 | Reserved | VTT | AGTL+ termination voltage | Power | |
| AL21 | Reserved | VTT | AGTL+ termination voltage | Power | |
| AM2 | GND | Reserved | Reserved | Reserved | 1 |
| AN11 | Reserved | VTT | AGTL+ termination voltage | Power | |
| AN13 | Reserved | AP1# | Address parity | AGTL+, I/O | 2 |
| AN15 | Reserved | VTT | AGTL+ termination voltage | Power | |
| AN23 | Reserved | RP# | Request parity | AGTL+, I/O | |
| B36 | Reserved | BINIT# | Bus initialization | AGTL+, I/O | 2 |
| C29 | Reserved | DEP5# | Data bus ECC data | AGTL+, I/O | 2 |
| C31 | Reserved | DEP1# | Data bus ECC data | AGTL+, I/O | 2 |
| C33 | Reserved | DEP0# | Data bus ECC data | AGTL+, I/O | 2 |
| E29 | Reserved | DEP6# | Data bus ECC data | AGTL+, I/O | 2 |
| E31 | Reserved | DEP4# | Data bus ECC data | AGTL+, I/O | 2 |
| G35 | Reserved | VTT | AGTL+ termination voltage | Power | |
| V4 | Reserved | BERR# | Bus error | AGTL+, I/O | 2 |
| W3 | Reserved | A34# | Additional AGTL+ address | AGTL+, I/O | 2 |
| X4 | RESET# | RESET2# | Processor reset (Value processors) | AGTL+, I | 3 |
| X6 | Reserved | A32# | Additional AGTL+ address | AGTL+, I/O | 2 |
| Y33 | GND | CLKREF | 1.25V PLL reference | Power | 1 |

**NOTES:**

1. These signals were previously defined as ground (Vss) connections in legacy designs utilizing the PGA370 socket to provide termination for unused inputs. For new Flexible PGA370 designs, use the new signal definitions. These new signal definitions are backwards compatible with the Celeron processor (PPGA).
2. While these signals are not used with 810E/810E2 chipset designs, they are available for chipsets that do support these functions. Only the Pentium III processor offers these capabilities in the PGA370 platform.
3. The AGTL+ reset signal, RESET#, is delivered to pin X4 on Legacy PGA370 designs. On Flexible PGA370 designs it is delivered to X4 and AH4 pins. See Figure 2 for more details.

## 2.2.1. Layout Guidelines for Intel® Pentium® III Processors

The following layout guide supports designs using Celeron processors and the Pentium III processor with the 810E2 chipset. The solution covers system bus speeds of 66/100 MHz for the Celeron processor and 100/133 MHz for the Pentium III processors. The solution proposed in this segment requires the motherboard design to terminate the system bus AGTL+ signals with a 56 Ω ± 5% Rtt. The Pentium III processor must also be configured to 110 Ω internal Rtt.

### Initial Timing Analysis

The table below lists the AGTL+ component timings of the processors and 82810E GMCH defined at the pins. These timings are for reference only; obtain each processor's specifications from its respective processor datasheet and appropriate 810E2 chipset component specification.

**Table 2. Intel® Pentium® III Processor and Intel® 82810E GMCH AGTL+ Parameters for Example Calculations**

| IC Parameters | Intel® Pentium® III processor core at 133 MHz System Bus | Intel® 82810E GMCH | Notes |
|---|---|---|---|
| Clock to Output maximum ($T_{CO\_MAX}$) | 2.70 | 3.70 | 2 |
| Clock to Output minimum ($T_{CO\_MIN}$) | 0.20 | 0.95 | 2 |
| Setup time ($T_{SU\_MIN}$) | 1.20 | 2.72 | 2,3 |
| Hold time ($T_{HOLD}$) | 0.80 | 0.10 | |

**NOTES:**
1. All times in nanoseconds.
2. **Numbers in table are for reference only**. These timing parameters are subject to change. Check the appropriate component documentation for valid timing parameter values.
3. $T_{SU\_MIN}$ = 2.72 ns assumes the 82810E GMCH sees a minimum edge rate equal to 0.3 V/ns.

Table 3 provides an example AGTL+ initial maximum flight time and Table 4 is an example minimum flight time calculation for a 133 MHz, uni-processor system using the Pentium III processor/ 810E2 chipset system bus. Note that assumed values for clock skew and clock jitter were used. **Clock skew and clock jitter values are dependent on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.**

Table 3 and Table 4 are derived assuming:

- $CLK_{SKEW}$ = 0.20 ns (Note: Assumes clock driver pin-to-pin skew is reduced to 50 ps by tying two host clock outputs together ("ganging") at clock driver output pins, and the PCB clock routing skew is 150 ps. System timing budget must assume 0.175 ns of clock driver skew if outputs are not tied together and a clock driver that meets the *CK810E Clock Synthesizer/ Driver Specification* is being used.)
- $CLK_{JITTER}$ = 0.250 ns

See the appropriate 810E2 chipset documentation, and *CK810E Clock Synthesizer/Driver Specification* for details on clock skew and jitter specifications. Exact details of host clock routing topology are provided with the platform design guideline.

### Table 3. Example $T_{FLT\_MIN}$ Calculations for 133 MHz Bus[1]

| Driver | Receiver | Clk Period[2] | TCO_MAX | TSU_MIN | ClkSKEW | ClkJITTER | MADJ | Recommended TFLT_MIN[3] |
|---|---|---|---|---|---|---|---|---|
| Processor | GMCH | 7.50 | 2.70 | 2.72 | 0.20 | 0.25 | 0.40 | 3.73 |
| GMCH | Processor | 7.50 | 5.35 | 1.20 | 0.20 | 0.25 | 0.40 | 2.60 |

**NOTES:**
1. All times in nanoseconds.
2. BCLK period = 7.50 ns @ 133.33 MHz.
3. The flight times in this column include margin to account for the following phenomena that Intel has observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect flight time and signal quality and are sometimes not accounted for in simulation. Accordingly, maximum flight times depend on the baseboard design and additional adjustment factors or margins are recommended.
   - SSO push-out or pull-in.
   - Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay.
   - Crosstalk on the PCB and internal to the package can cause variation in the signals.

There are additional effects that **may not** necessarily be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. Examples include:

- The effective board propagation constant ($S_{EFF}$), which is a function of:
  - Dielectric constant ($\varepsilon_r$) of the PCB material.
  - The type of trace connecting the components (stripline or microstrip).
  - The length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time **but not necessarily equal to** the flight time.

### Table 4. Example TFLT_MIN Calculations (Frequency Independent)[1]

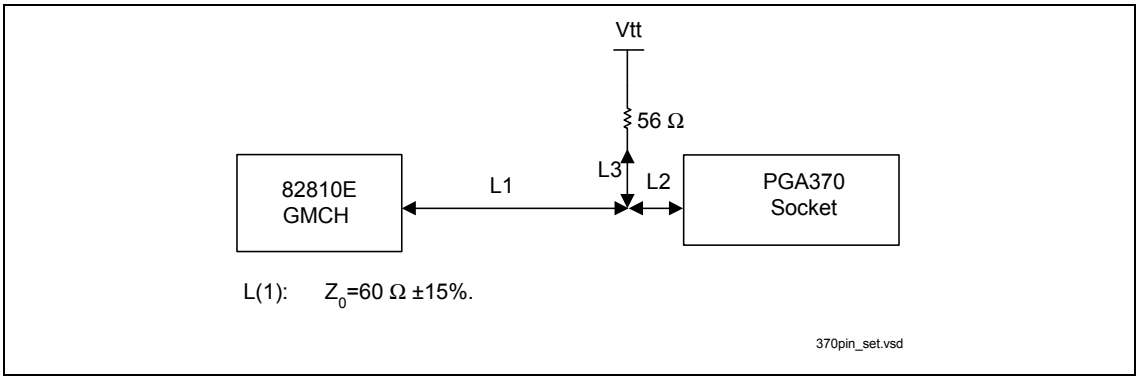
| Driver | Receiver | THOLD | ClkSKEW | TCO_MIN | Recommended TFLT_MIN |
|---|---|---|---|---|---|
| Processor | 82810E GMCH | 0.10 | 0.15 | 0.35 | 0.40 |
| Intel® 82810E GMCH | Processor | 1.0 | 0.15 | 0.35 | 0.23 |

**NOTES:**
1. All times in nanoseconds.

## 2.2.2. Determine General Topology and Layout

In the SET (Set Ended Termination) topology for the 370-pin socket (PGA370), the termination should be placed close to the processor on the motherboard. There is no termination present at the chipset end of the network. Due to the lack of termination, SET will exhibit much more ringback than the dual-terminated topology. Extra care is required in SET simulations to make sure that the ringback specifications are met under the worst case signal quality conditions. 810E2 chipset designs require all AGTL+ signals to be terminated with a 56 Ω termination on the motherboard. To ensure processor signal integrity requirements **it is highly recommended that all system bus signal segments to be referenced to the ground plane for the entire route (See Chapter 4 for details).**

### Figure 2. Topology for 370-Pin Socket Designs with Single-Ended Termination (SET)




### Table 5. Segment Descriptions and Lengths for Figure 2 [1]

| Segment | Description | Min length (inches) | Max length (inches) |
|---|---|---|---|
| L1 + L2 | Intel® 82810E GMCH to Rtt Stub | 1.90 | 4.50 |
| L2 | PGA370 Pin to Rtt stub | 0.0 | 0.20 |
| L3 | Rtt Stub length | 0.50 | 2.50 |

**NOTES:**
1. All AGTL+ bus signals should be referenced to the ground plane for the entire route. See Chapter 4.

- AGTL+ signals should be routed with trace lengths within the range specified for L1+L2 from the processor pin to the chipset.
- Use an intragroup AGTL+ spacing to line width to dielectric thickness ratio of at least 2:1:1 for microstrip geomety. If $\varepsilon_r$ = 4.5, this should limit coupling to 3.4%. For example, intragroup AGTL+ routing could use 10 mil spacing, 5 mil traces, and a 5 mil prepreg between the signal layer and the plane it references (assuming a 4-layer motherboard design).
- The trace width is recommended to be 5 mils and not greater than 6 mils.

The following table contains the trace width: space ratios assumed for this topology. The crosstalk cases considered in this guideline involve three types: Intragroup AGTL+, Intergroup AGTL+, and AGTL+ to non-AGTL+. Intragroup AGTL+ crosstalk involves interference between AGTL+ signals within the same group. Intergroup AGTL+ crosstalk involves interference from AGTL+ signals in a particular group to AGTL+ signals in a different group. An example of AGTL+ to non-AGTL+ crosstalk is when CMOS and AGTL+ signals interfere with each other.

### Table 6. Trace Width:Space Guidelines

| Crosstalk Type | Trace Width:Space Ratios |
|---|---|
| Intragroup AGTL+ signals (same group AGTL+) | 5:10 or 6:12 |
| Intergroup AGTL+ signals (different group AGTL+) | 5:15 or 6:18 |
| AGTL+ to non-AGTL+ Processor Signals | 5:20 or 6:24 |

### 2.2.2.1. Motherboard Layout Rules for AGTL+ Signals

#### Minimizing Crosstalk

The following general rules will minimize the impact of crosstalk in the high-speed AGTL+ bus design:

- Maximize the space between traces. Maintain a minimum of 10 mils (assuming a 5 mil trace) between trace edges wherever possible. It may be necessary to use tighter spacing when routing between component pins. When traces have to be close and parallel to each other, minimize the distance that they are close together, and maximize the distance between the sections when the spacing restrictions relaxes.
- Avoid parallelism between signals on adjacent layers if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
- Since AGTL+ is a low signal swing technology, it is important to isolate AGTL+ signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings (e.g., 5V PCI).
- Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL+ specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes the crosstalk.
- Route AGTL+ address, data and control signals in separate groups to minimize crosstalk between groups. Comply with the requirements pointed out in the Intergroup AGTL+ signals in the “Trace Width:Space Guidelines” table.
- Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus, reduces the crosstalk magnitude.
- Minimize the dielectric process variation used in the PCB fabrication.
- Minimize the cross sectional area of the traces. This can be done by narrower traces and/or by using thinner copper, but the tradeoff for this smaller cross-sectional area is a higher trace resistivity that can reduce the falling edge noise margin because of the I*R loss along the trace.

### 2.2.2.2. Motherboard Layout Rules for Non-AGTL+ (CMOS) Signals

#### Non-AGTL+ (CMOS) Signals

Route these signals on any layer or any combination of layers.

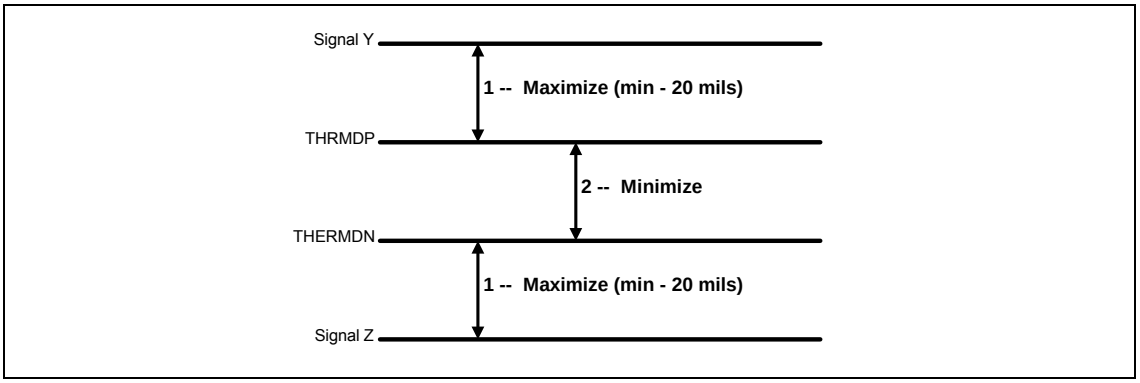
**Table 7. Routing Guidelines for Non-AGTL+ Signals**

| Signal | Trace Width | Spacing to Other Traces | Trace Length |
|---|---|---|---|
| A20M# | 5 mils | 10 mils | 1” to 6” |
| FERR# | 5 mils | 10 mils | 1” to 6” |
| FLUSH# | 5 mils | 10 mils | 1” to 6” |
| IERR# | 5 mils | 10 mils | 1” to 6” |
| IGNNE# | 5 mils | 10 mils | 1” to 6” |
| INIT# | 5 mils | 10 mils | 1” to 6” |
| LINT[0] (INTR) | 5 mils | 10 mils | 1” to 6” |
| LINT[1] (NMI) | 5 mils | 10 mils | 1” to 6” |
| PICD[1:0] | 5 mils | 10 mils | 1” to 8” |
| PREQ# | 5 mils | 10 mils | 1” to 6” |
| PWRGOOD | 5 mils | 10 mils | 1” to 6” |
| SLP# | 5 mils | 10 mils | 1” to 6” |
| SMI# | 5 mils | 10 mils | 1” to 6” |
| STPCLK | 5 mils | 10 mils | 1” to 6” |
| THERMTRIP# | 5 mils | 10 mils | 1” to 6” |

### 2.2.2.3. THRMDP and THRMDN

These traces (THRMDP and THRMDN) route the processor’s thermal diode connections. The thermal diode operates at very low currents and may be susceptible to crosstalk. The traces should be routed close together to reduce loop area and inductance (Refer to the figure below).

**Figure 3. Routing for THRMDP and THRMDN**




- Rule
  - — Length Equalization route these traces parallel ±0.5”
  - — Layer route both on the same layer

#### 2.2.2.4. Additional Considerations

- Distribute VTT with a wide trace. A 0.050” minimum trace is recommended to minimize DC losses. Route the VTT trace to all components on the host bus. Be sure to include decoupling capacitors.
- The VTT voltage should be 1.5V ± 3% for static conditions and 1.5 V ± 9% for worst case transient condition.
- Place resistor divider pairs for $V_{REF}$ generation at the 82810E GMCH component. $V_{REF}$ is also delivered to the processor.

### 2.2.3. Undershoot/Overshoot Requirements

Undershoot and overshoot specificaitons become more critical as the process technology for microprocessors shrinks due to thinner gate oxide. Violating these undershoot and overshoot limits will degrade the life expectancy of the processor.

### 2.2.4. BSEL[1:0] Implementation for PGA370 Designs

The Pentium III processor utilizes the BSEL1 pin to select either a 100 MHz or 133 MHz system bus frequency setting from the CK810E clock synthesizer. While the BSEL0 signal is still connected to the PGA370 socket, the Pentium III processor does not utilize it. Only the Celeron processor (CPUID=0665) utilizes the BSEL0 signal. The Pentium III processors are 3.3 V tolerant for these signals, as are the CK810E and GMCH. However, the Celeron processor requires 2.5V logic levels on the BSEL signals.

A new clock synthesizer, the CK810E, has been designed to support selections of 66 MHz, 100 MHz, and 133 MHz. The REF input pin has been redefined to be a frequency selection strap (BSEL1) during power-on and then becomes a 14 MHz reference clock output. This maintains pin compatibility with the CK810 clock synthesizer. The following figure details the new BSEL[1:0] circuit design for *Flexible PGA370* designs. **Note that BSEL[1:0] are now pulled up using 1 kΩ resistors.** The following figure shows the 82810E GMCH and processor straps for selecting the system bus frequency.

**Figure 4. BSEL[1:0] Circuit Implementation for PGA370 Designs**

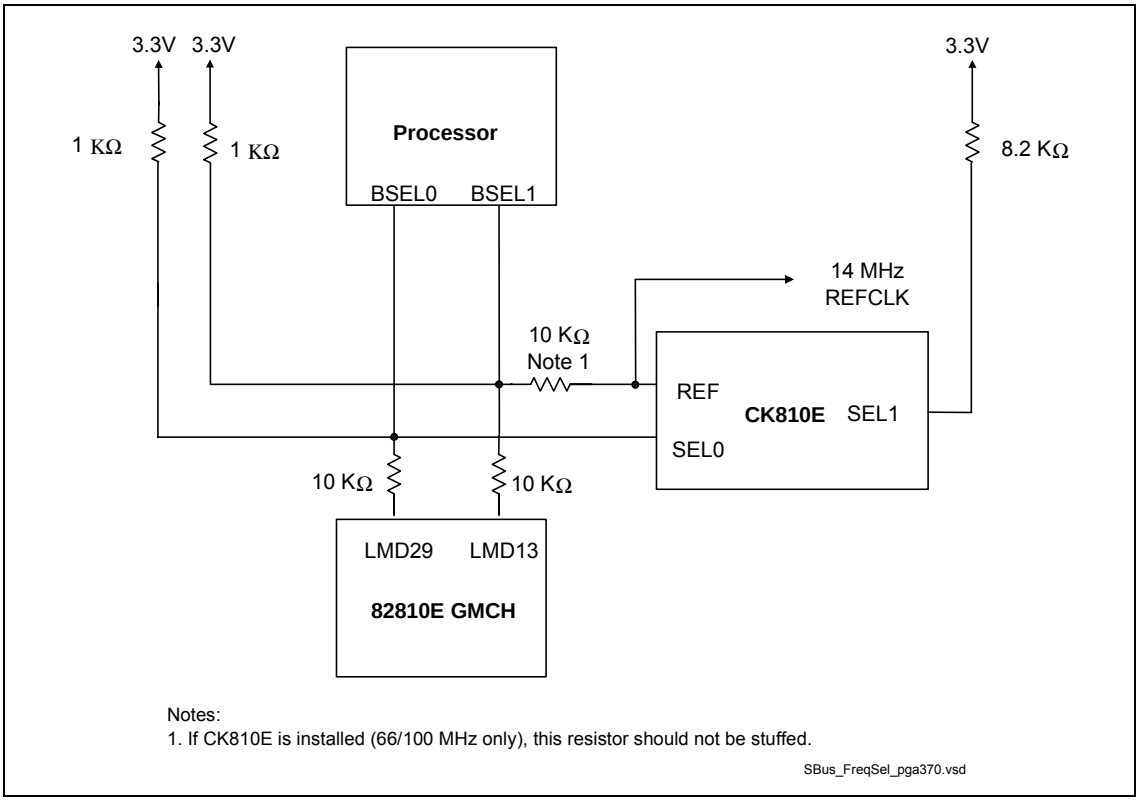



**Table 8. Intel® CK810E Reset Strapping Matrix**

| REF | SEL1 | SEL0 | Intel® CK810E Function |
|---|---|---|---|
| X | 0 | 0 | Tristate |
| X | 0 | 1 | Test |
| 0 | 1 | 0 | Active processor = 66 MHz |
| 0 | 1 | 1 | Active processor = 100 MHz |
| 1 | 1 | 1 | Active processor = 133 MHz |
| 1 | 1 | 0 | Reserved |

## 2.2.5. CLKREF Circuit Implementation

The CLKREF input requires a 1.25V source. It can be generated from a voltage divider on the Vcc2.5 or Vcc3.3 sources utilizing 1% tolerance resistors. A 4.7 µF decoupling capacitor should be included on this input. See the following figure and table for example CLKREF circuits. **Do not use VTT as the source for this reference!**

**Figure 5. Examples for CLKREF Divider Circuit**

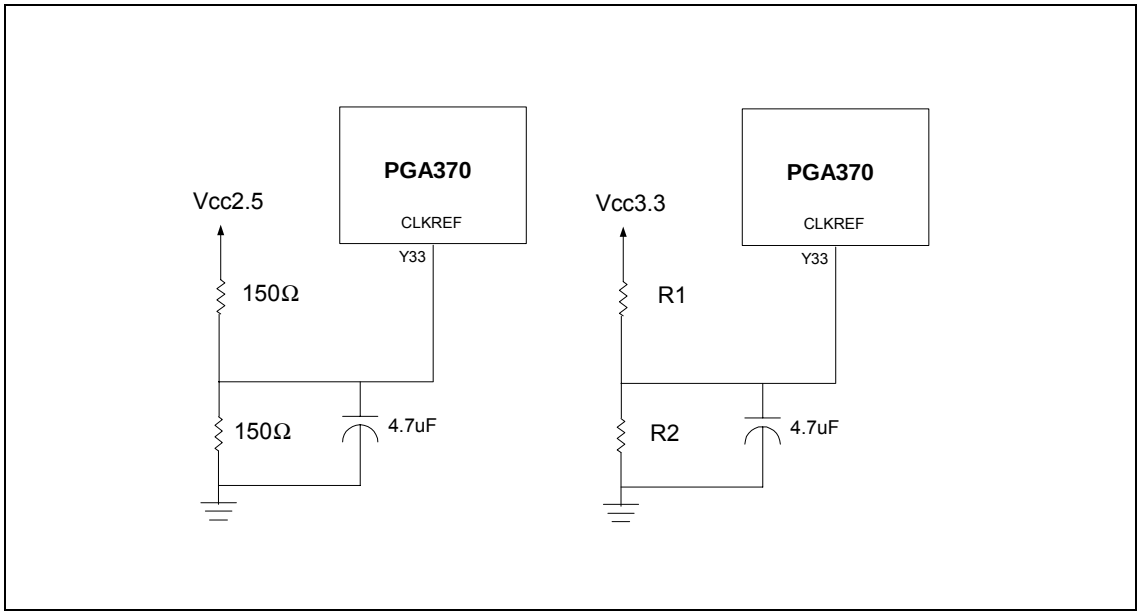



**Table 9. Examples for CLKREF Divider Circuit**

| R1 (Ω) | R2 (Ω) | CLKREF Voltage (V) |
|---|---|---|
| 182 | 110 | 1.243 |
| 301 | 182 | 1.243 |
| 374 | 221 | 1.226 |
| 499 | 301 | 1.242 |

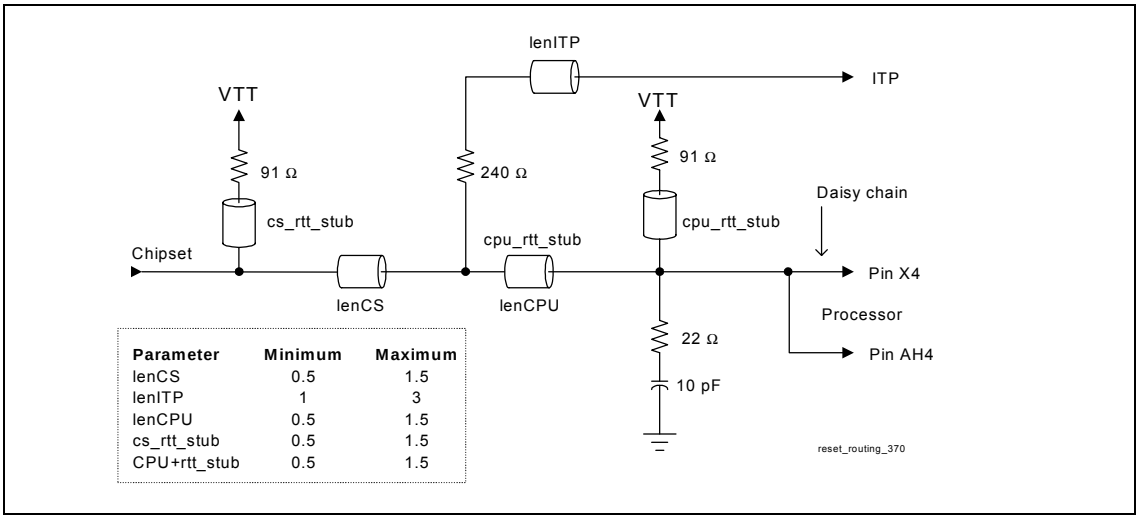
## 2.2.6. Undershoot/Overshoot Requirements

The Pentium III processor has more restrictive overshoot and undershoot requirements for system bus signals than previous processors. These requirements stipulate that a signal at the output of the driver buffer and at the input of the receiver buffer must not exceed a maximum absolute overshoot voltage limit (2.1V) and a minimum absolute undershoot voltage limit (- 0.35V). Exceeding these limits will cause damage to the Pentium III processor. There is also a time dependent, non-linear overshoot and undershoot requirement that is dependent on the amplitude and duration of the overshoot/undershoot. See the Pentium III processor datasheet for more details on overshoot/undershoot specifications.

## 2.2.7. Connecting RESET# and RESET2# on a Flexible PGA370 Design

The 810E2 chipset platform designs that support both the Celeron processor and Pentium III processor must route the AGTL+ reset signal from the chipset to two pins on the processor, as well as to the ITP connector. This reset signal is connected to pins AH4 (RESET#) and X4 (RESET#) at the PGA370 socket (See the following figure).

**Figure 6. RESET# Schematic for PGA370 Designs**




| Parameter | Minimum | Maximum |
|---|---|---|
| lenCS | 0.5 | 1.5 |
| lenITP | 1 | 3 |
| lenCPU | 0.5 | 1.5 |
| cs_rtt_stub | 0.5 | 1.5 |
| CPU+rtt_stub | 0.5 | 1.5 |

On legacy 810 chipset platforms (ones that only have support for Celeron processors), RESET# is delivered only to pin X4. On flexible 810E chipset platforms (ones that have support for both the Celeron processor and the Pentium II processors) using a 370-pin socket, RESET# is delivered to both pins X4 *and* AH4.

## 2.2.8. Reset Strapping Options

LMD26 on the 82810E GMCH is used as a strap at reset to determine whether the system board is supporting a 370-pin socket or an SC242 connector:

LMD26: 0 (or floating) = 370-pin socket [leave as no connect]

1 = SC242 slot [pull-up to 3.3V through an (approximately) 8.2 kΩ pull-up resistor]

### 2.2.8.1. Power-Up/Reset Strap Options

Table 10 lists power-up options that are loaded into the 82810E GMCH during cold reset.

**Table 10. Power Up Options**

| Signal | Description |
|---|---|
| LMD[31] | **XOR Chain Test Select:** LMD[31] is set to 0 for normal operation. It must be set to 1 to enter XOR tree mode during reset. This signal must remain 1 during the entire XOR tree test. |
| LMD[30] | **ALL Z select:** If LMD[30] is set to 1, it tri-states all signals during reset. For normal operation, LMD[30] should be set to 0 |
| LMD[29] | **Host Frequency Select:** If LMD[13] is 0 and LMD[29] is set to 0 during reset, the host bus frequency is 66 MHz. If LMD[13] is 0 and LMD[29] is set to 1, the host bus frequency is 100 MHz. |
| LMD[28] | **In-Order Queue Depth Status:** The value on LMD[28] sampled at the rising edge of CPURST# reflects if the IOQD is set to 1 or 4. If LMD[28] is set to 0, IOQD is 4. If LMD[28] is set to 1, IOQD is 1. |
| LMD[13] | **Host Frequency Select:** If LMD[13] is a 0, LMD[29] determines host bus frequency. If LMD[13] is a 1, the host bus frequency is 133 MHz. |

**Table 11. Host Frequency Strappings**

| LMD[13] | LMD[29] | Host Bus Frequency |
|---|---|---|
| 0 | 0 | 66 MHz |
| 0 | 1 | 100 MHz |
| 1 | X | 133 MHz |

## 2.2.9. Voltage Regulation Differences

The Pentium III (FC-PGA w/256K L2 cache) processor requires the VRM or on-board voltage regulator to be compliant with Intel *VRM 8.4 DC-DC Converter Design Guidelines* revision 1.5 or greater. Important points to note regarding VRM 8.4 as follow:

- Celeron processor (PPGA) operates at $VCC_{CORE}$ of 2.0V, Pentium III (FP-PGA w/128-K L2 cache) operates at 1.5V, and Pentium III 256K operates at 1.6V.
- Requirement for VRM 8.4 to support the Pentium III processor at speeds greater than 650 MHz has changed from previous processors. Transient and static tolerances are tighter than VRM 8.2.
- Maximum current is increased to 18.4A for flexible motherboard designs.
- Additional motherboard decoupling is required to meet VRM 8.4.

## 2.2.10. Decoupling Guidelines for Flexible PGA370 Designs

These are preliminary decoupling guidelines for *Flexible PGA370* designs and are estimated to meet VRM 8.4 V1.5 flexible motherboard guidelines (Vcc=1.6V, Icc = 0.8 - ~18.4A).

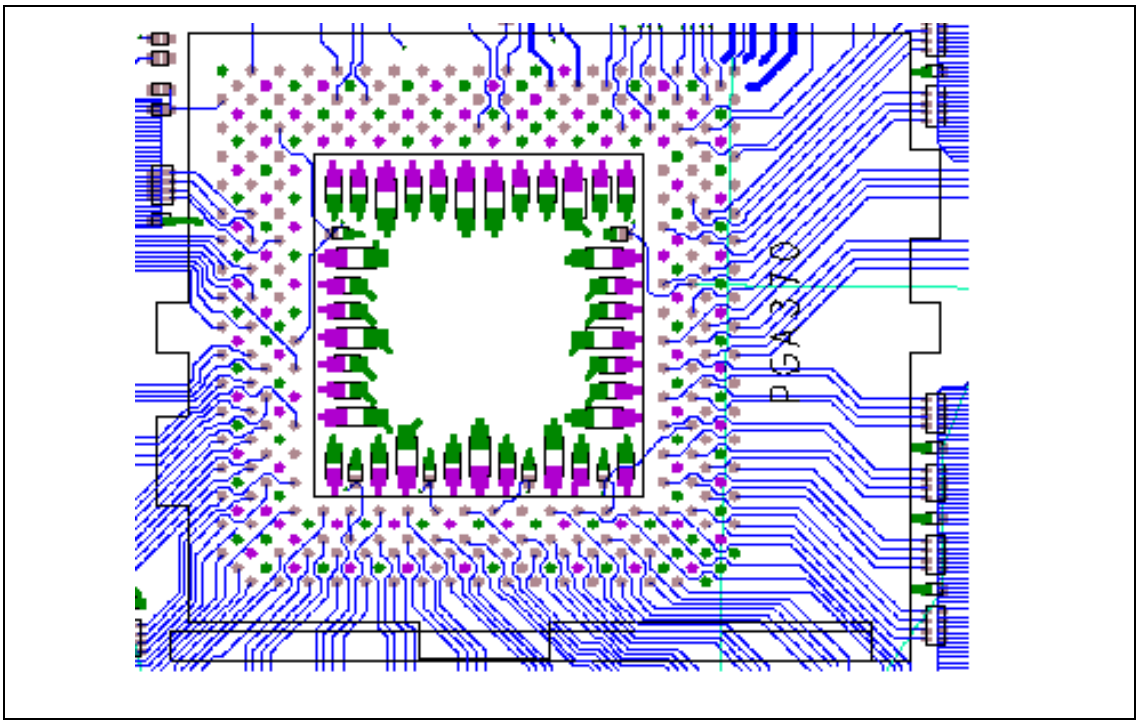
### 2.2.10.1. VCCcore Decoupling Design

- **Ten** or more 4.7 µF capacitors in 1206 packages.

  All capacitors should be placed within the PGA370 socket cavity and mounted on the primary side of the motherboard. The capacitors are arranged to minimize the overall inductance between $VCC_{CORE}$/Vss power pins, as shown in the following figure.

- 8 ea (min) 1 µF 0612 package placed in the Intel® PGA370 socket cavity.

**Figure 7. Capacitor Placement on the Motherboard**



### 2.2.10.2. VTT Decoupling Design

For Itt = 3.0 A (max).

- ***Nineteen*** - 0.1 µF capacitors in 0603 packages placed within 200 mils of AGTL+ termination R-packs, one capacitor for every two R-packs. These capacitors are shown on the outer exterior of Figure 7. These are located on the motherboard.

### 2.2.10.3. VREF Decoupling Design

***Four*** - 0.1 µF capacitors in 0603 package placed near $V_{REF}$ pins (within 500 mils).

## 2.2.11. Thermal/EMI Differences

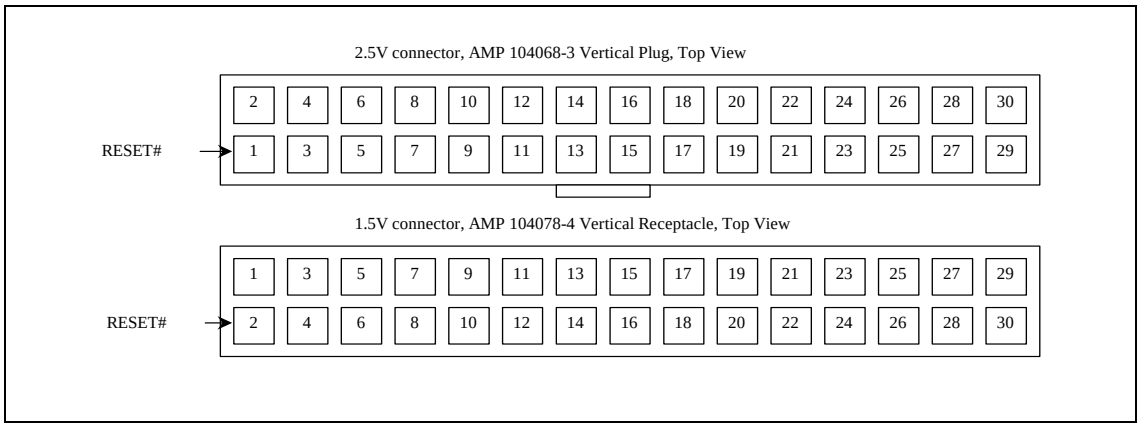
Heatsink requirements will be different for FC-PGA processors from previous processors using PPGA packaging. The current flexible motherboard guidelines for Pentium III (FC-PGA w/256-K L2 cache) processors calls for 28.4 W.

- Increased power density for Pentium III processor (approximately 27 W/cm$^2$).
- Different thermal design verification for FC-PGA compared to PPGA packaged processors. Pentium III processors are specified using Tjunction versus Tcase (used with Celeron processors).
- New heatsink for FC-PGA package which is not backwards compatible with PPGA processors.
- New heatsink clips for FC-PGA processor heatsinks.

## 2.2.12. Debug Port Changes

Due to the lower voltage technology employed with the Pentium III processor, changes are required to support the debug port. Previously, the test access port (TAP) signals used 2.5V logic. This is the case with the Celeron processor in the PPGA package. Pentium III utilizes 1.5V logic levels on the TAP. As a result, a new ITP connector is to be used on flexible PGA370 designs. The new 1.5V connector is the mirror image of the older 2.5V connector. Either connector will fit into the same printed circuit board layout. Just the pin numbers would change, as can be seen in the drawing below.

**Figure 8. TAP Connector Comparison**




***Caution:*** The Pentium III processor requires an in-target probe (ITP) with a 1.5V tolerant buffer. Previous ITPs are designed to work with higher voltages and may damage the processor if they are connected to an Pentium III processor.

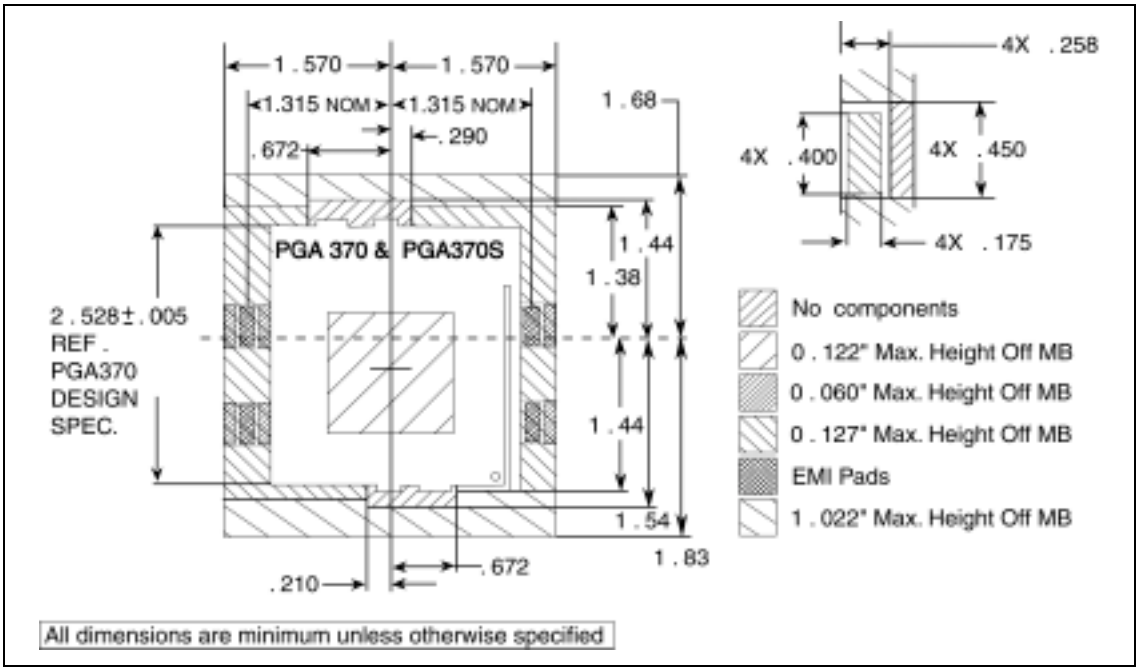
## 2.2.13. PGA370 Socket Connector Strapping Option

Clarifications of the keep-out zone changes are as follows:

- An increase in the height of the heatsink volumetric area from 2.10” to 2.52” including a 0.420” area above the heatsink to allow adequate area for fan inlet air.
- Growth in the x direction of the top of the heatsink keep-out zone from 2.55” to 3.504“ to enable a thumb tab for a heatsink-attach clip
- Growth in the x direction of the bottom of the heatsink keep-out zone from 2.55” to 2.70” to enable a fan/shroud heatsink attach mechanism.

OEMs can anticipate that the Intel reference design thermal solution will be larger than Intel Celeron™ processor thermal solutions. Enlarging this thermal solution may cause interference fit issues, please ensure that if you plan on using the Intel Reference solution, the motherboard and system can accommodate these adjusted dimensions.

**Figure 9. Component Keep-Out Zones**




***Note:*** Performance results of Intel reference design thermal solutions are dependent upon multiple system parameters and should therefore be evaluated individually by perspective users. ****Actual required transition points (processor speed) for OEMs should be determined through system-level thermal evaluation.***

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# 3. Layout and Routing Guidelines

This chapter describes motherboard layout and routing guidelines for 810E2 chipset systems, except for the processor layout guidelines. For the PGA370 processor specific layout guidelines, refer to Chapter 2. This chapter does not discuss the functional aspects of any bus or the layout guidelines for an add-in device.

***Note:*** If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from these guidelines should be simulated.

## 3.1. General Recommendations

The trace impedance typically noted (i.e., 60 Ω ±15%) is the “nominal” trace impedance for a 5 mil wide trace (i.e., the impedance of the trace when not subjected to the fields created by changing current in neighboring traces). When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

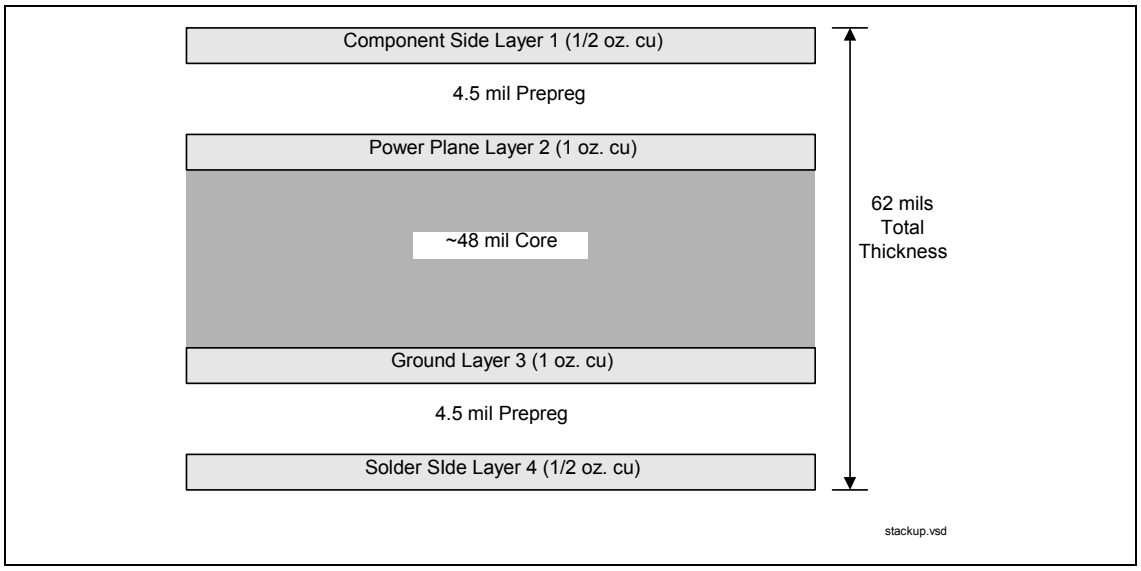
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this chapter should be followed.

Additionally, these routing guidelines are created using a PCB stack-up similar to that illustrated in the following figure. If this stack-up is not used, extremely thorough simulations of every interface must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

## 3.2. Nominal Board Stackup

The 810E2 chipset platform requires a board stackup yielding a target impedance of 60 Ω ±15% with a 5 mil nominal trace width. The following figure presents an example stackup to achieve this. It is a 4-layer fabrication construction using 53% resin, FR4 material.

**Figure 10. Nominal Board Stackup**




# 3.1 Component Quadrant Layouts

**Figure 11. GMCH Quadrant Layout (top View)**

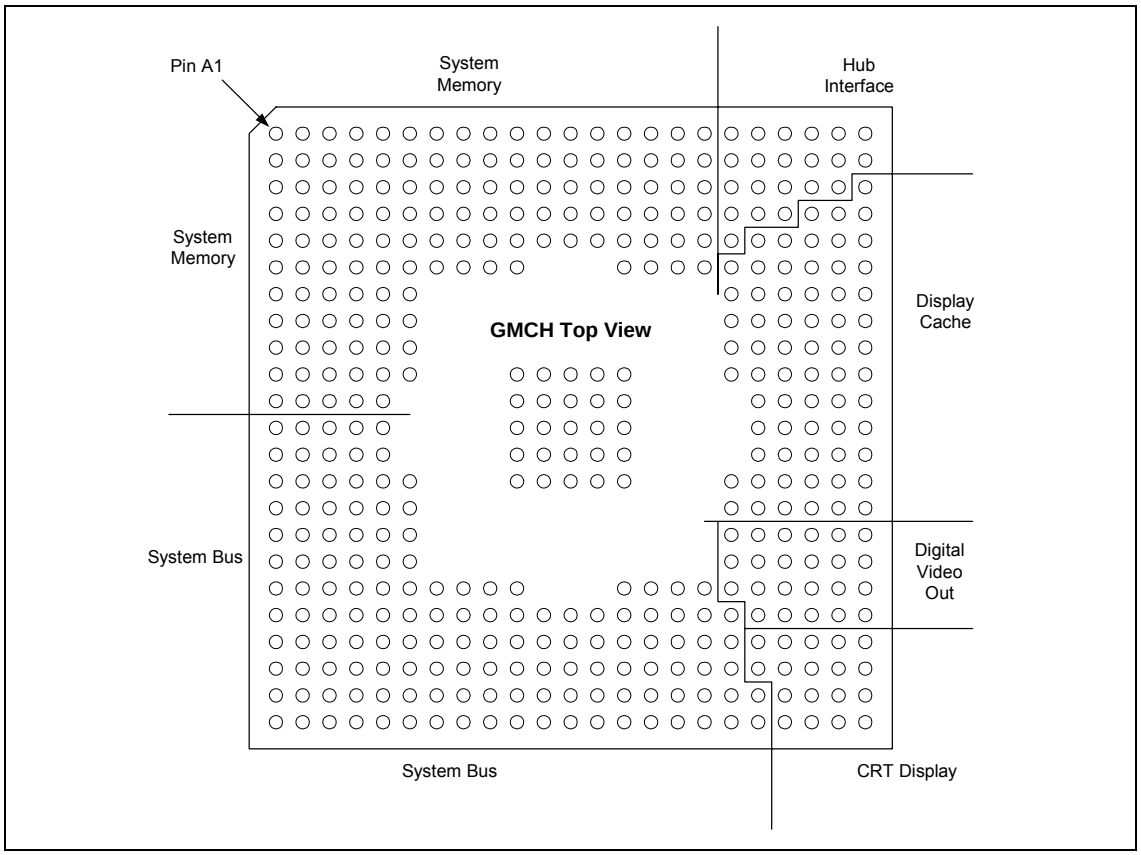
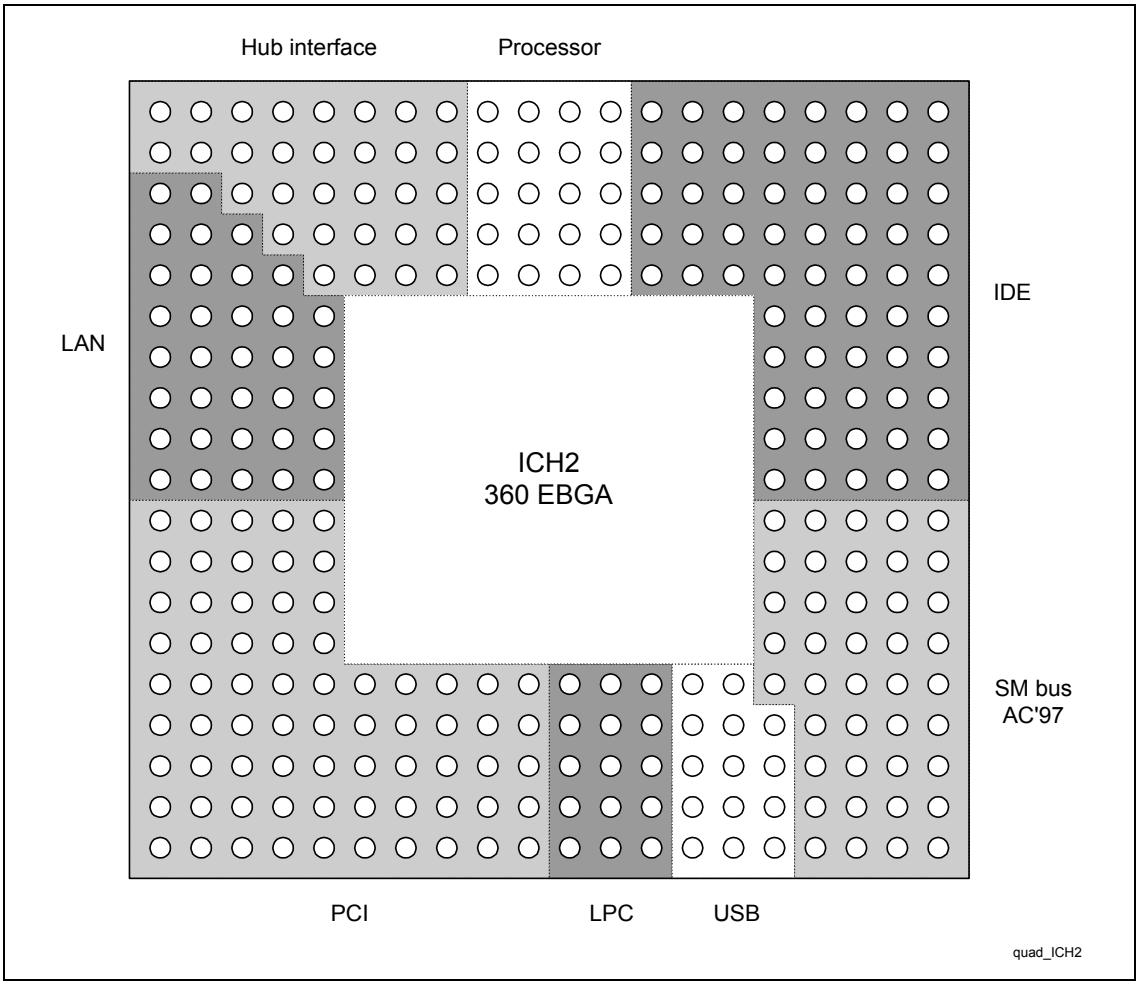
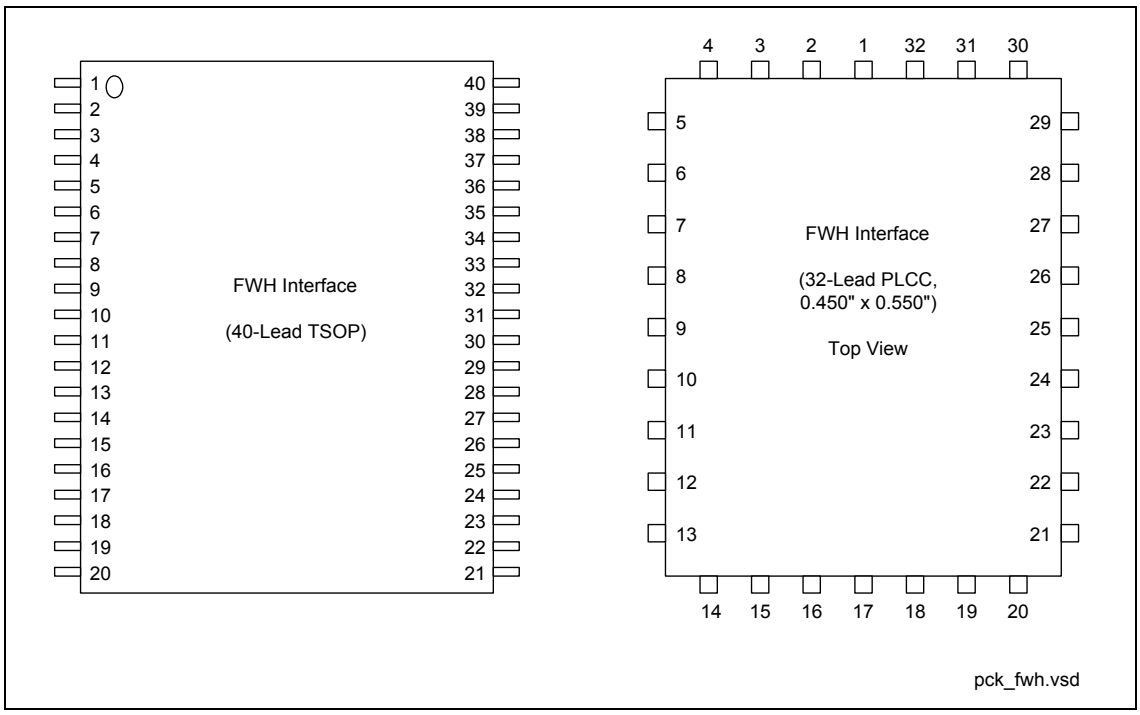


**Figure 12. Intel® ICH2 Quadrant Layout (Top View)**




The diagram in the previous figure illustrates the relative signal quadrant locations on the ICH2 ballout. It does not represent the actual ballout. Refer to the *Intel® 82801BA I/O Controller Hub 2 (ICH2) Datasheet* for the actual ballout.

**Figure 13. Firmware Hub (FWH) Packages**

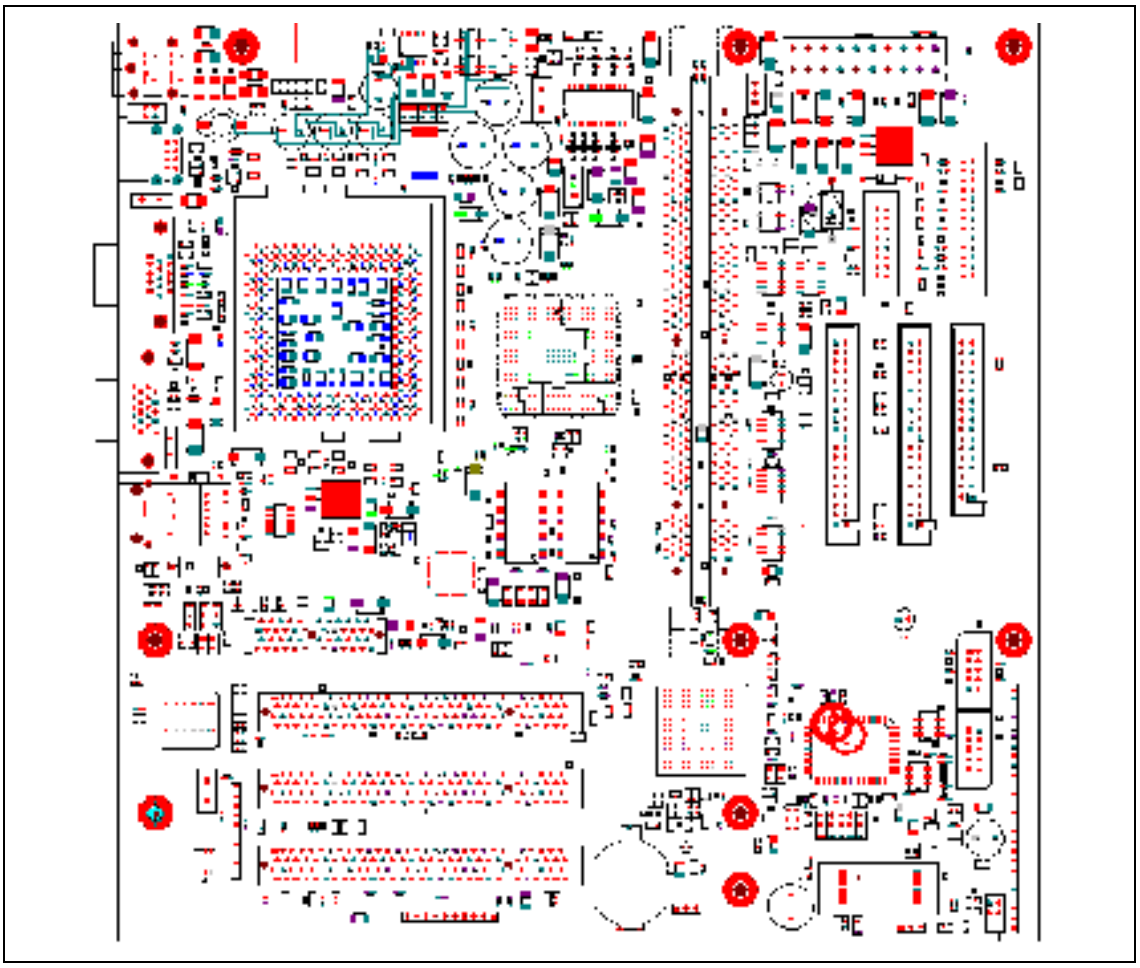


## 3.3. Intel® 810E2 Chipset Component Placement

The assumptions for component placement are:

- uATX form factor
- 4-Layer motherboard
- Single-sided assembly

**Figure 14. uATX Placement Example for PGA370 Processors**



# 3.4. System Memory Layout Guidelines

## 3.4.1. System Memory Solution Space

**Figure 15. System Memory Topologies**

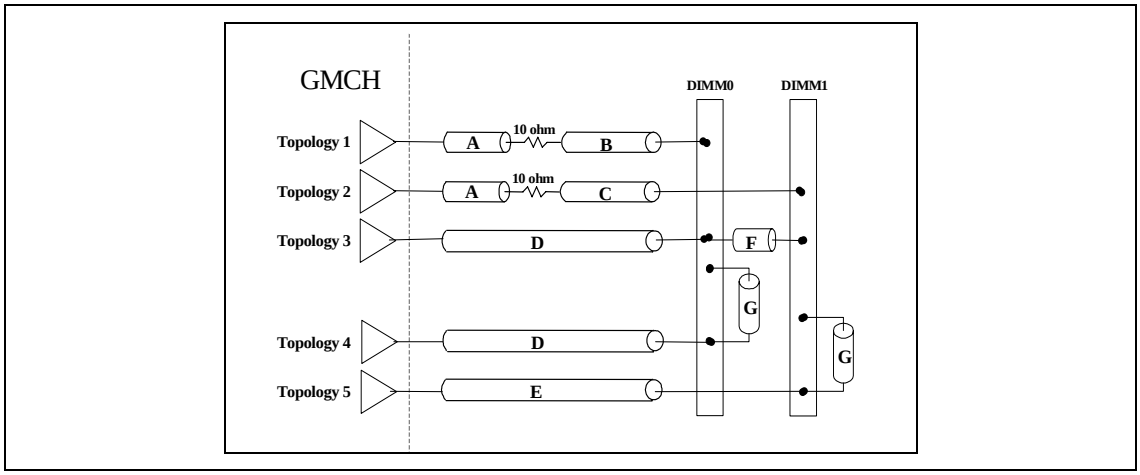



**Table 12. System Memory Routing**

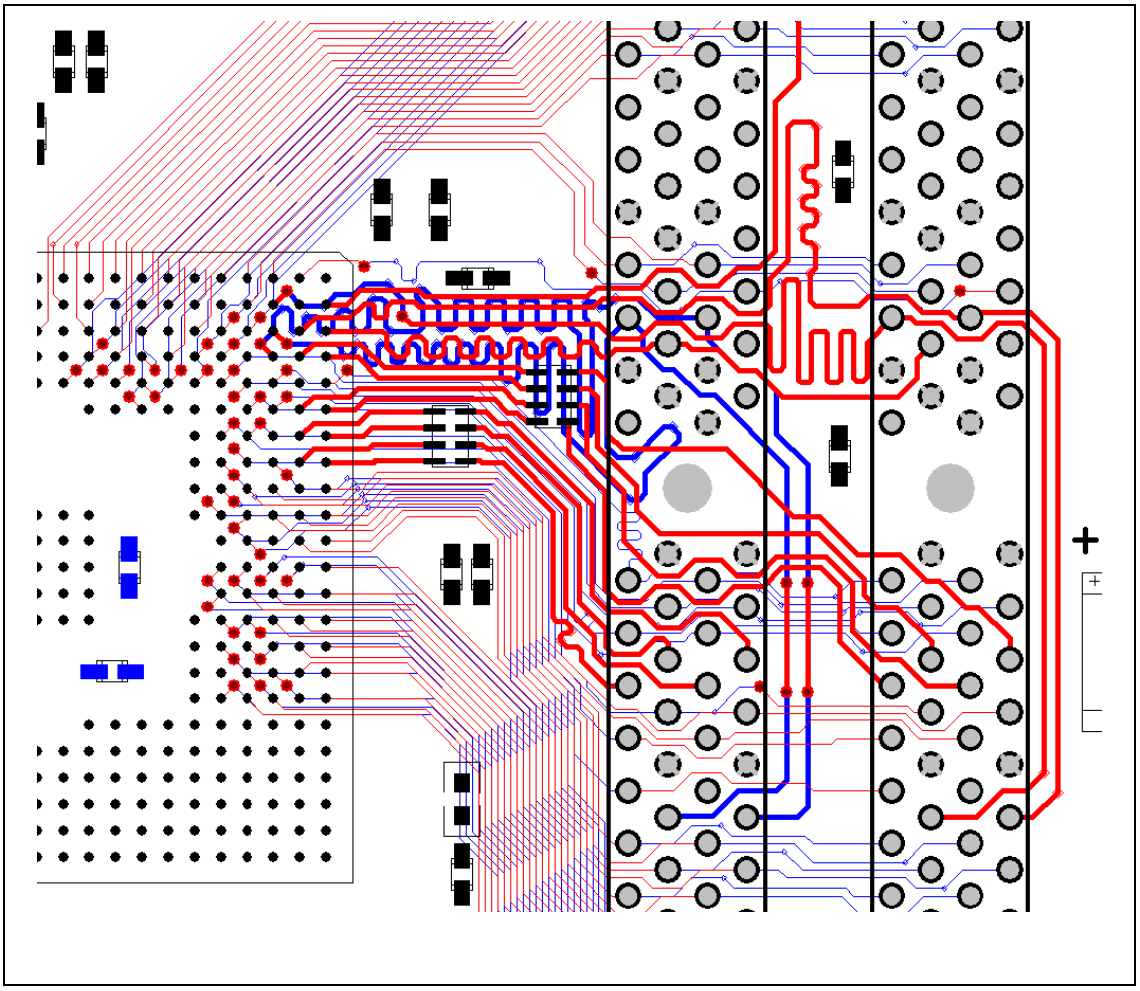
| Signal | | Top. | Trace (mils) | | Trace Lengths (inches) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | A | B | | C | | D | | E | | F | | G | |
| | | | Width | Space | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| SCS[3:2]# | Opt.1 | 5 | 10 | 8 | | | | | | | | 3 | 5 | | | 1.5 | 2 |
| | Opt.2 | 5 | 10 | 8 | | | | | | | | 2.2 | 5 | | | 1.5 | 1.8 |
| | Opt.3 | 5 | 10 | 8 | | | | | | | | 1.6 | 5 | | | 1.15 | 1.5 |
| SCS[1:0]# | Opt.1 | 4 | 10 | 8 | | | | | | 3 | 5 | | | | | 1.5 | 2 |
| | Opt.2 | 4 | 10 | 8 | | | | | | 2.2 | 5 | | | | | 1.5 | 1.8 |
| | Opt.3 | 4 | 10 | 8 | | | | | | 1.6 | 5 | | | | | 1.15 | 1.5 |
| SMAA[7:4] | | 1 | 10 | 8 | 0.5 | 0.5 | 2 | | | | | | | | | | |
| SMAB[7:4]# | | 2 | 10 | 8 | 0.5 | | | 0.5 | 2 | | | | | | | | |
| SCKE[1:0] | | 3 | 10 | 8 | | | | | | 1 | 2.5 | | | 0.4 | 1 | | |
| SMD[63:0], SDQM[7:0] | | 3 | 5 | 7 | | | | | | 1 | 3 | | | 0.4 | 1 | | |
| SCAS#, SRAS#, SWE# | | 3 | 5 | 7 | | | | | | 1 | 3.5 | | | 0.4 | 1 | | |
| SBS[1:0], SMAA[11:8, 3:0] | | 3 | 5 | 7 | | | | | | 1 | 2.5 | | | 0.4 | 1 | | |

**NOTES:**

1. It is recommended to add 10 Ω series resistors to the MAA[7:4] and the MAB[7:4] lines, as close as possible to GMCH for signal integrity.

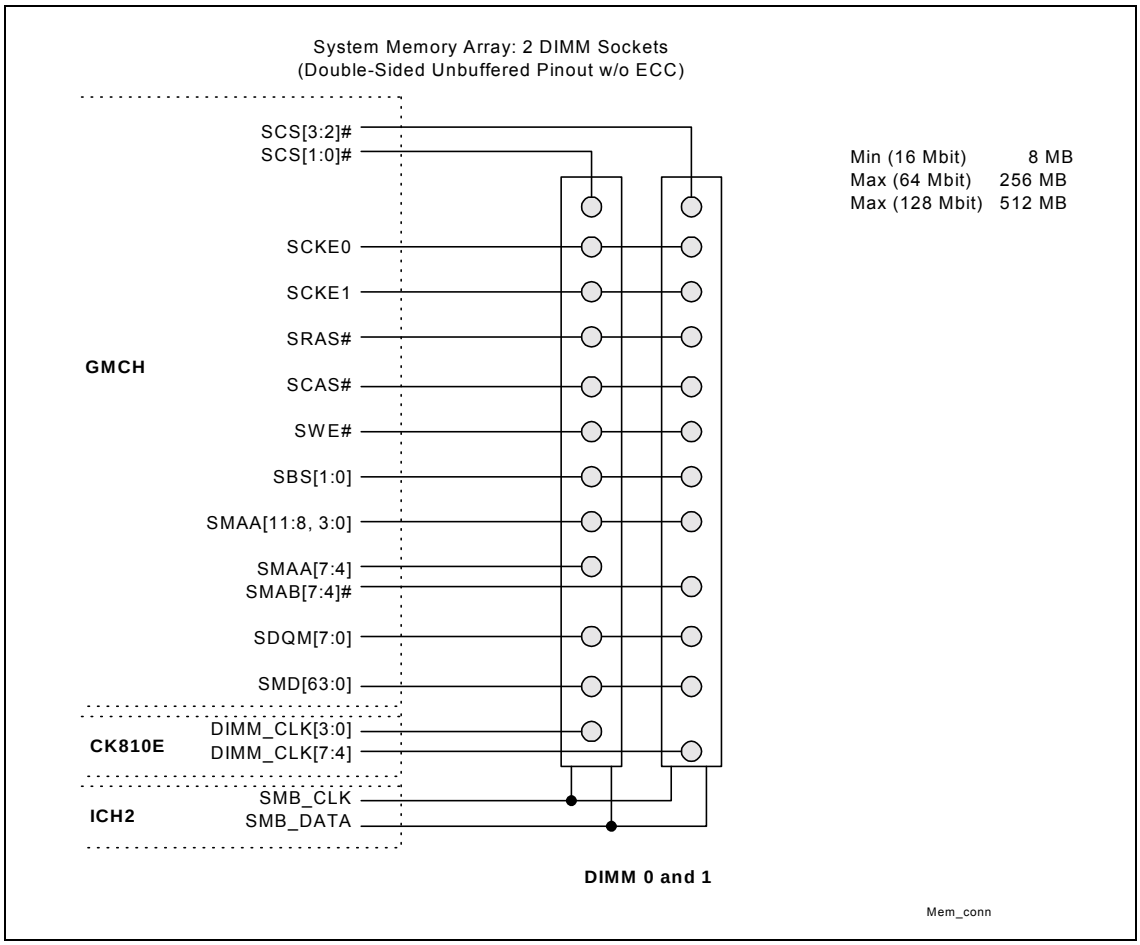
### 3.1.1 System Memory Routing Example

**Figure 16. System Memory Routing Example**



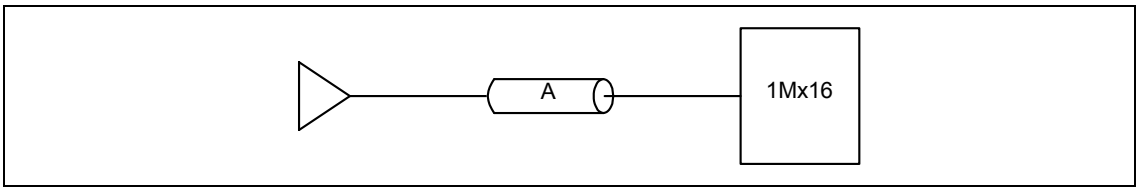
## 3.4.2. System Memory Connectivity

**Figure 17. System Memory Connectivity**



## 3.5. Display Cache Interface

**Figure 18. Display Cache (Topology 1)**




### 3.5.1. Display Cache Solution Space

**Table 13. Display Cache Routing (Topology 1)**

| Signal | Topology | Trace (mils) | | A (inches) | |
|---|---|---|---|---|---|
| | | Width | Spacing | Min | Max |
| LMD[31:0], LDQM[3:0] | 1 | 5 | 7 | 1 | 5 |

**NOTES:**
1. Trace Length (inches)

**Figure 19. Display Cache (Topology 2)**

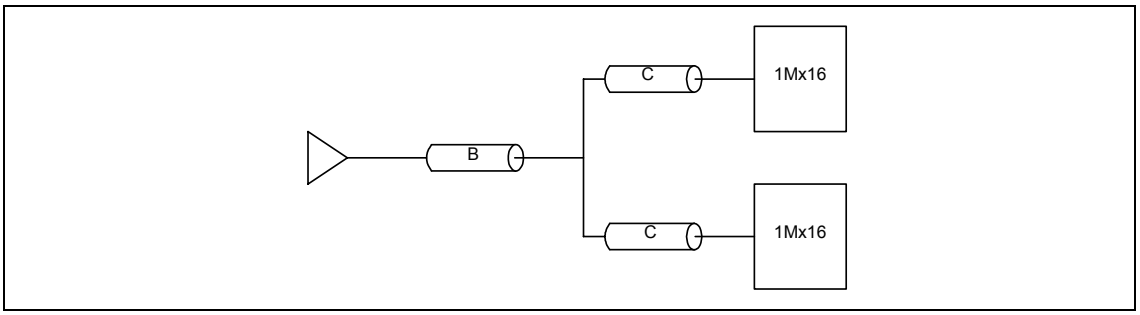
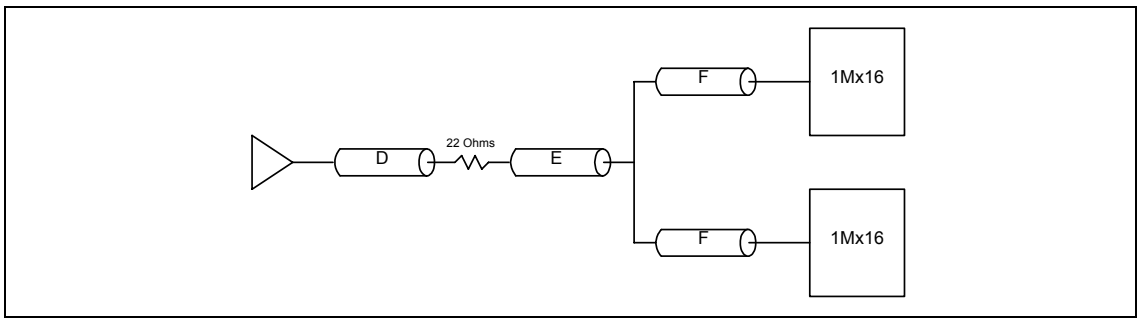



**Table 14. Display Cache Routing (Topology 2)**

| Signal | Topology | Trace (units=mils) | | B (inches) | | C (inches) | |
|---|---|---|---|---|---|---|---|
| | | Width | Spacing | Min | Max | Min | Max |
| LMA[11:0], LWE#, LCS#, LRAS#, LCAS# | 2 | 5 | 7 | 1 | 3.75 | 0.75 | 1.25 |

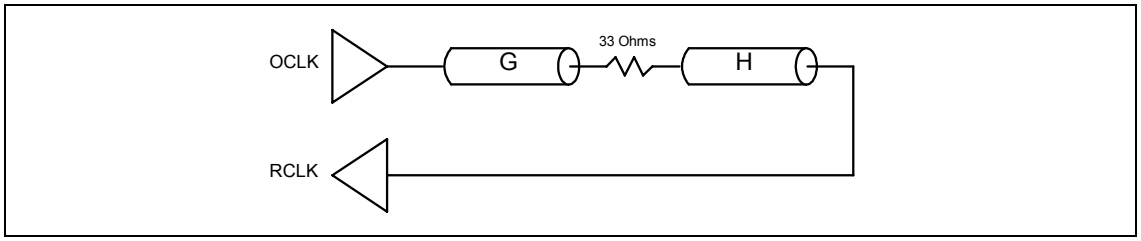
### Figure 20. Display Cache (Topology 3)




### Table 15. Display Cache Routing (Topology 3)

| Signal | Topology | Trace (units=mils) | | D (inches) | E (inches) | | F (inches) | |
|---|---|---|---|---|---|---|---|---|
| | | Width | Spacing | Length | Min | Max | Min | Max |
| TCLK | 3 | 5 | 7 | 0.5 | 1.5 | 2.5 | 0.75 | 1.25 |

### Figure 21. Display Cache (Topology 4)




### Table 16. Display Cache Routing (Topology 4)

| Signal | Topology | Trace (units=mils) | | G (inches) | H (inches) | |
|---|---|---|---|---|---|---|
| | | Width | Spacing | Length | Min | Max |
| OCLK | 4 | 5 | 6 | 0.5 | 3.25 | 3.75 |

## 3.6. Hub Interface

The 810E2 chipset's GMCH ball assignment and ICH2 ball assignment have been optimized to simplify hub interface routing. It is recommended that the hub interface signals be routed directly from the GMCH to the ICH2 on the top signal layer. Refer to the following figure.

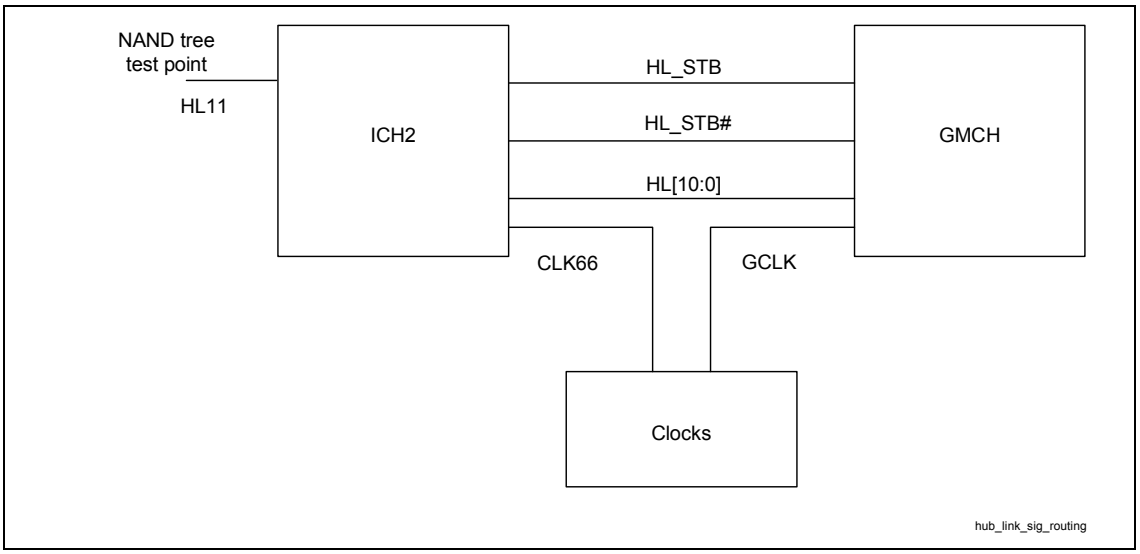
The hub interface is divided into two signal groups: data signals and strobe signals.

- Data Signals:
  - HL[10:0]
- Strobe Signals:
  - HL_STB
  - HL_STB#

***Note:*** HL_STB/HL_STB# is a differential strobe pair.

No pull-ups or pull-downs are required on the hub interface. HL[11] on the ICH2 should be brought out to a test point for NAND Tree testing. Each signal should be routed such that it meets the guidelines documented for its signal group.

**Figure 22. Hub Interface Signal Routing Example**




### 3.6.1. Data Signals

Hub interface data signals should be routed with a trace width of *5* mils and a trace spacing of *20* mils. These signals can be routed with a trace width of *5* mils and a trace spacing of *15* mils for navigation around components or mounting holes. To break out of the GMCH and the ICH2, the hub interface data signals can be routed with a trace width of *5* mils and a trace spacing of *5* mils. The signals should be separated to a trace width of *5* mils and a trace spacing of *20* mils, within 0.3" of the GMCH/ICH2 components.

The maximum trace length for the hub interface data signals is 7". These signals should each be matched within ±0.1" of the HL_STB and HL_STB# signals.

## 3.6.2. Strobe Signals

Due to their differential nature, the hub interface strobe signals should be 5 mils wide and routed 20 mils apart. This strobe pair should be a minimum of 20 mils from any adjacent signals. The maximum length for the strobe signals is 7”, and the two strobes should be the same length. Additionally, the trace length for each data signal should be matched to the trace length of the strobes, within ±0.1”.

## 3.6.3. HREF Generation/Distribution

HREF, the hub interface reference voltage, is 0.5 * 1.8 V = 0.9 V ± 2%. It can be generated using a single HREF divider or locally generated dividers (as shown in the following two figures). The resistors should be equal in value and rated at 1% tolerance, to maintain 2% tolerance on 0.9 V. The values of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. The recommended range for the resistor value is from a minimum of 100 Ω to a maximum of 1 kΩ (300 Ω shown in example).

The single HREF divider should not be located more than 4” away from either GMCH or ICH2. If the single HREF divider is located more than 4" away, then the locally generated hub interface reference dividers should be used instead.

The reference voltage generated by a single HREF divider should be bypassed to ground at each component with a 0.01-µF capacitor located close to the component HREF pin. If the reference voltage is generated locally, the bypass capacitor must be close to the component HREF pin.

## 3.6.4. Compensation

Independent Hub interface compensation resistors are used by the 810E2 chipset’s GMCH and the ICH2 to adjust buffer characteristics to specific board characteristics. Refer to the *Intel® 810E2 Chipset Family: 82810 Graphics and Memory Controller Hub (GMCH) Datasheet* and the *Intel® 82801BA I/O Controller Hub 2* (*ICH2) Datasheet* for details on compensation. The resistive Compensation (RCOMP) guidelines are as follows:

- **RCOMP:** Tie the HLCOMP pin of each component to a 40-Ω, 1% or 2% pull-up resistor (to 1.8 V) via a 10-mil-wide, 0.5” trace (targeted at a nominal trace impedance of 40 Ω). The GMCH and ICH2 each requires its own RCOMP resistor.

**Figure 23. Single Hub Interface Reference Divider Circuit**

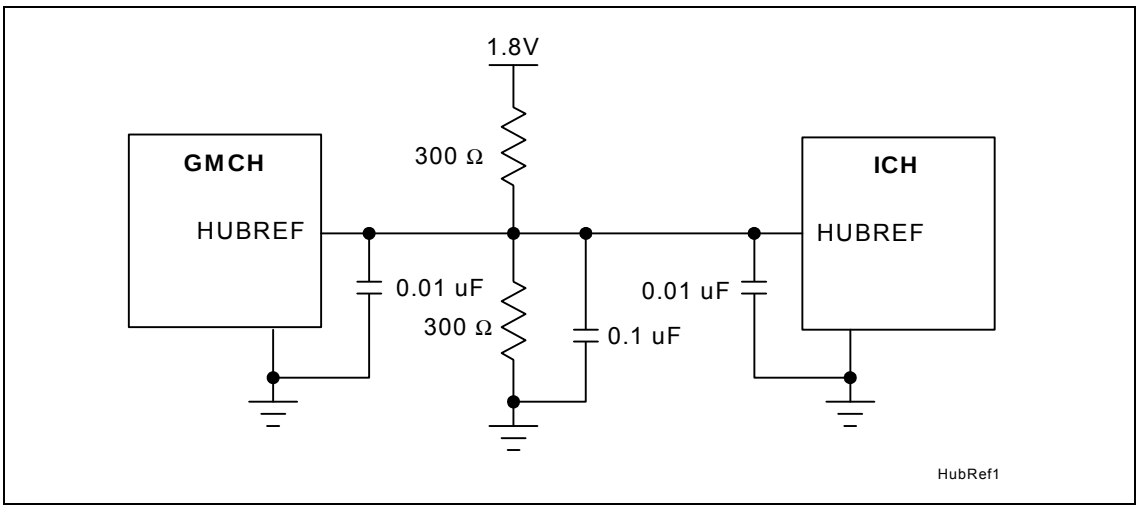
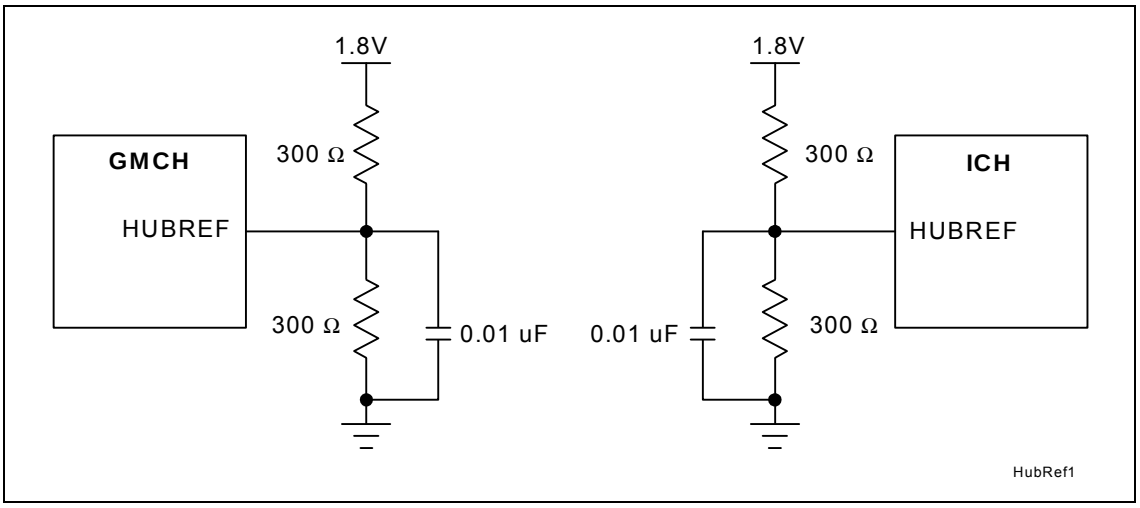



**Figure 24. Locally Generated Hub Interface Reference Dividers**



# 3.7. Intel® ICH2

## 3.7.1. Decoupling

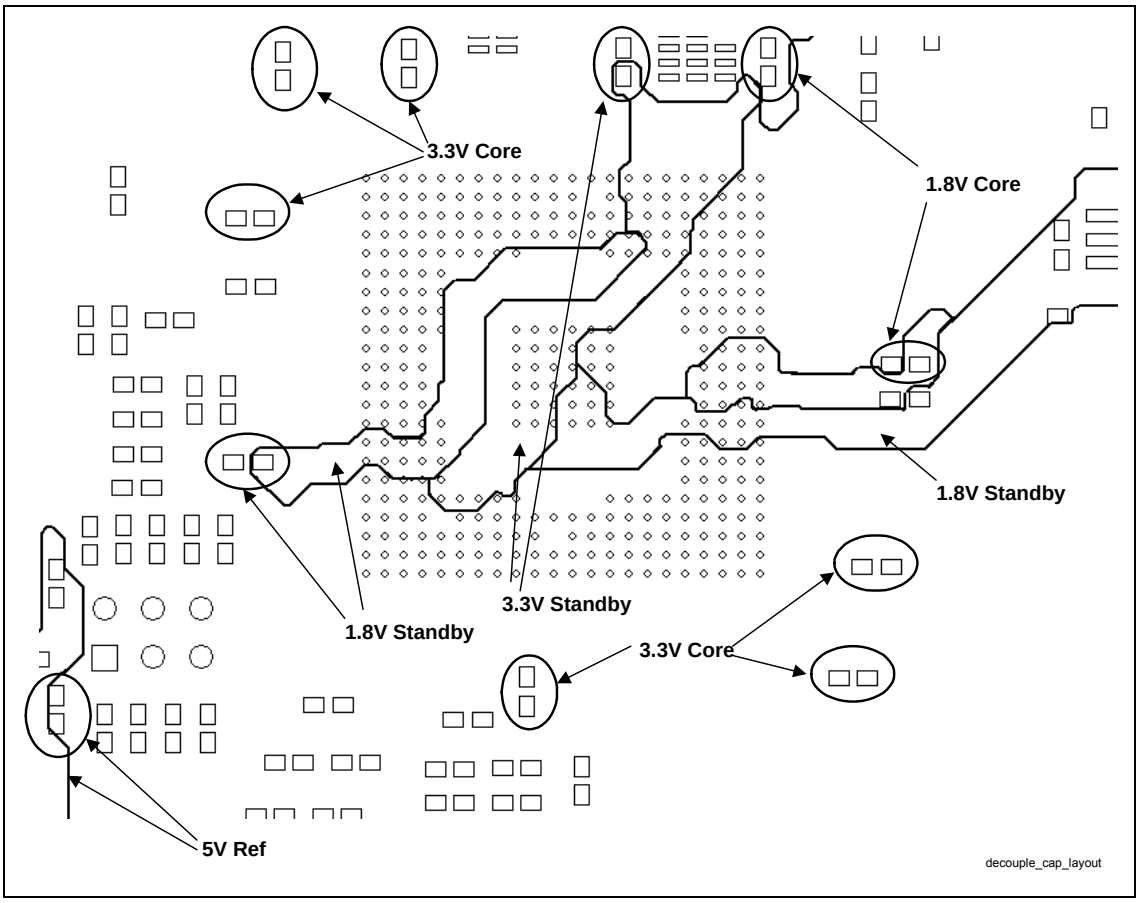
The ICH2 is capable of generating large current swings when switching between logic High and logic Low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in the following table to ensure that the component maintains stable supply voltages. The capacitors should be placed as close as possible to the package, without exceeding 400 mils (100–300 mils nominal).

***Note:*** Routing space around the ICH2 is tight. A few decoupling caps may be placed more than 300 mils away from the package. System designers should simulate the board to ensure that the correct amount decoupling is implemented. Refer to the following figure for a layout example. It is recommended that, for prototype board designs, the designer include pads for extra power plane decoupling caps.

**Table 17. Decoupling Capacitor Recommendation**

| Power Plane/Pins | Decoupling Capacitors | Capacitor Value |
|---|---|---|
| 3.3-V core | 6 | 0.1 µF |
| 3.3-V standby | 1 | 0.1 µF |
| Processor interface (1.3 ~ 2.5 V) | 1 | 0.1 µF |
| 1.8-V core | 2 | 0.1 µF |
| 1.8-V standby | 1 | 0.1 µF |
| 5-V reference | 1 | 0.1 µF |
| 5-V reference standby | 1 | 0.1 µF |

Figure 25. Intel® ICH2 Decoupling Capacitor Layout




## 3.8. 1.8V/3.3V Power Sequencing

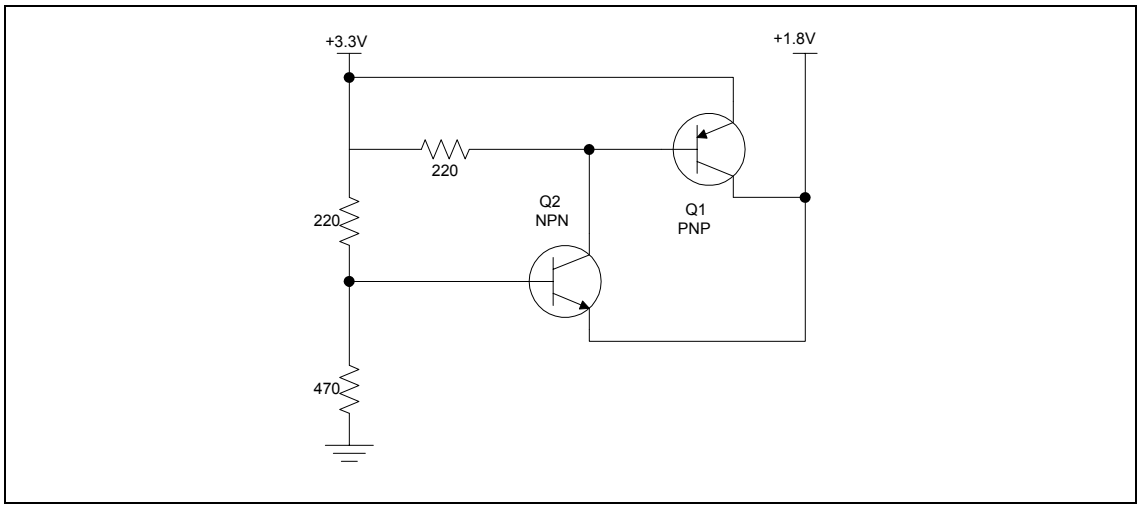
The ICH2 has two pairs of associated 1.8V and 3.3V supplies. These are Vcc1_8, Vcc3_3 and VccSus1_8, VccSus3_3. These pairs are assumed to power up and power down together. **The difference between the two associated supplies must never be greater than 2.0V.** The 1.8V supply may come up before the 3.3V supply without violating this rule (though this is generally not practical in a desktop environment, since the 1.8V supply is typically derived from the 3.3V supply by means of a linear regulator).

One serious consequence of violation of this "2V Rule" is electrical overstress of oxide layers, resulting in component damage.

The majority of the ICH2 I/O buffers are driven by the 3.3V supplies, but are controlled by logic that is powered by the 1.8V supplies. Thus, another consequence of faulty power sequencing arises if the 3.3V supply comes up first. In this case the I/O buffers will be in an undefined state until the 1.8V logic is powered up. Some signals that are defined as "Input-only" actually have output buffers that are normally disabled, and the ICH2 may unexpectedly drive these signals if the 3.3V supply is active while the 1.8V supply is not.

The following figure shows an example power-on sequencing circuit that ensures the “2V Rule” is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.8V supply tracks the 3.3V supply. The NPN transistor controls the current through PNP from the 3.3V supply into the 1.8V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8V plane, current will not flow from the 3.3V supply into 1.8V plane when the 1.8V plane reaches 1.8V.

**Figure 26. Example 1.8V/3.3V Power Sequencing Circuit**



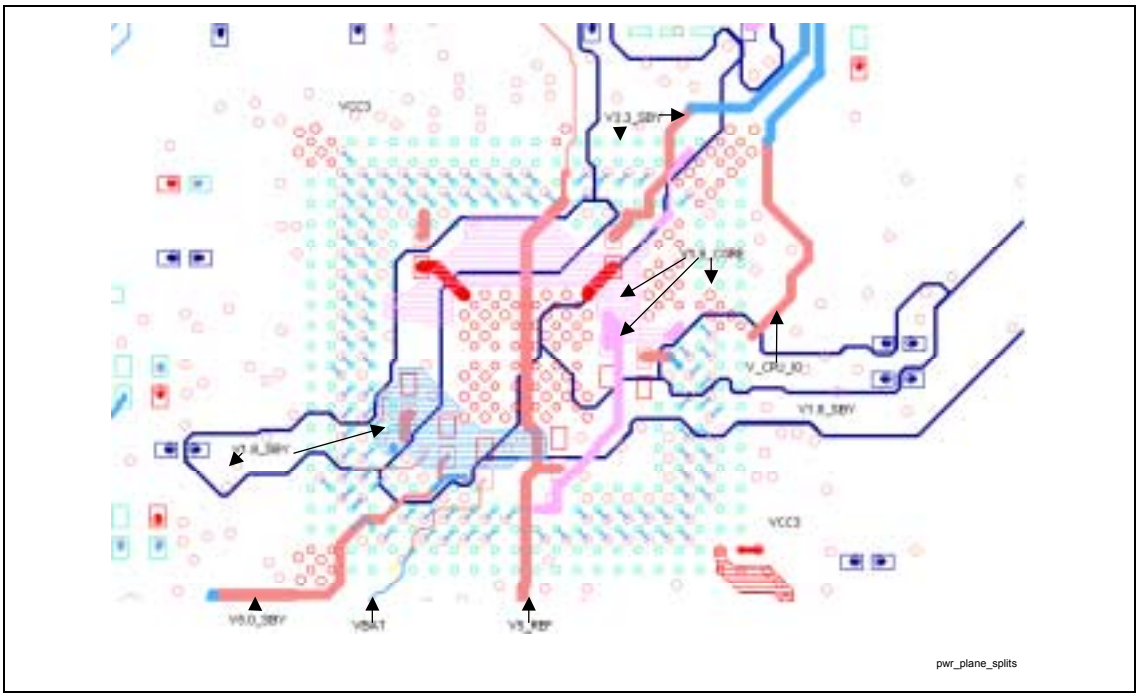

When analyzing systems that may be "marginally compliant" to the 2V Rule, pay close attention to the behavior of the ICH2's RSMRST# and PWROK signals, since these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the Resume wells.
- PWROK controls isolation between the Resume wells and Main wells

If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

## 3.9. Power Plane Splits

**Figure 27. Power Plane Split Example**




## 3.10. Thermal Design Power

The thermal design power is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus.

The thermal design power for the ICH2 is 1.5 W ±15%.

## 3.11. IDE Interface

This section contains guidelines for connecting and routing the ICH2 IDE interface. The ICH2 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement and signal termination for both IDE channels. The ICH2 has integrated the series resistors that typically have been required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. Intel does not anticipate requiring additional series termination, but OEMs should verify the motherboard signal integrity via simulation. Additional external 0-Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by providing future stuffing options.

The IDE interface can be routed with 5-mil traces on **7-mil spaces** and must be less than 8” long (from ICH2 to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 0.5” shorter than the longest IDE signal (on that channel).

### 3.11.1. Cabling

- **Length of cable:** Each IDE cable must be equal to or less than 18”.
- **Capacitance:** Less than 30 pF
- **Placement:** A maximum of 6” between drive connectors on the cable. If a single drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the connector next closest to the end of the cable (6” away from the end of the cable).
- **Grounding:** Provide a direct, low-impedance chassis path between the motherboard ground and hard disk drives.
- **ICH2 Placement:** The ICH2 must be placed at most 8” from the ATA connector(s).
- **PC99 Requirement:** Support Cable Select for master-slave configuration is a system design requirement of Microsoft* PC99. The CSEL signal of each ATA connector must be grounded at the host side.

## 3.12. Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH2 IDE controller supports PIO, multiword (8237-style) DMA, and Ultra DMA modes 0 through 5. The ICH2 must determine the type of cable present, to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra ATA/66 and Ultra ATA/100. This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal. All ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the Small Form Factor Specification SFF-8049, which is obtainable from the Small Form Factor Committee.

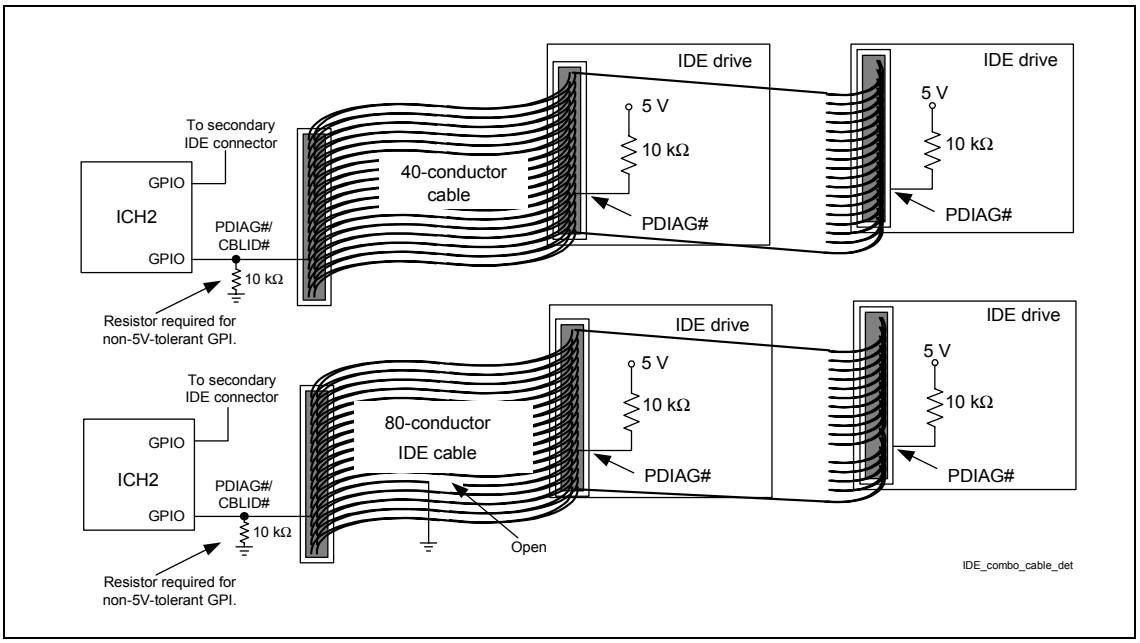
To determine whether the ATA/66 or ATA/100 mode can be enabled, the ICH2 requires that the system software attempt to determine the type of cable used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be performed using a combination host-side/device-side detection mechanism. Note that host-side detection cannot be implemented on an NLX form factor system, since this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the device-side detection mechanism only.

### 3.12.1. Combination Host-Side/Device-Side Cable Detection

Host-side detection (described in the *ATA/ATAPI-4 Standard*, Section 5.2.11) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in the following figure. All IDE devices have a 10-kΩ pull-up resistor to 5 volts on this signal. Not all GPI and GPIO pins on the ICH2 are 5-volt tolerant. If non 5-volt tolerant inputs are used, a resistor divider is required to prevent 5 V on the ICH2 or FWH pins. The proper value of the divider resistor is 10 kΩ (as shown in the following figure).

**Figure 28. Combination Host-Side / Device-Side IDE Cable Detection**



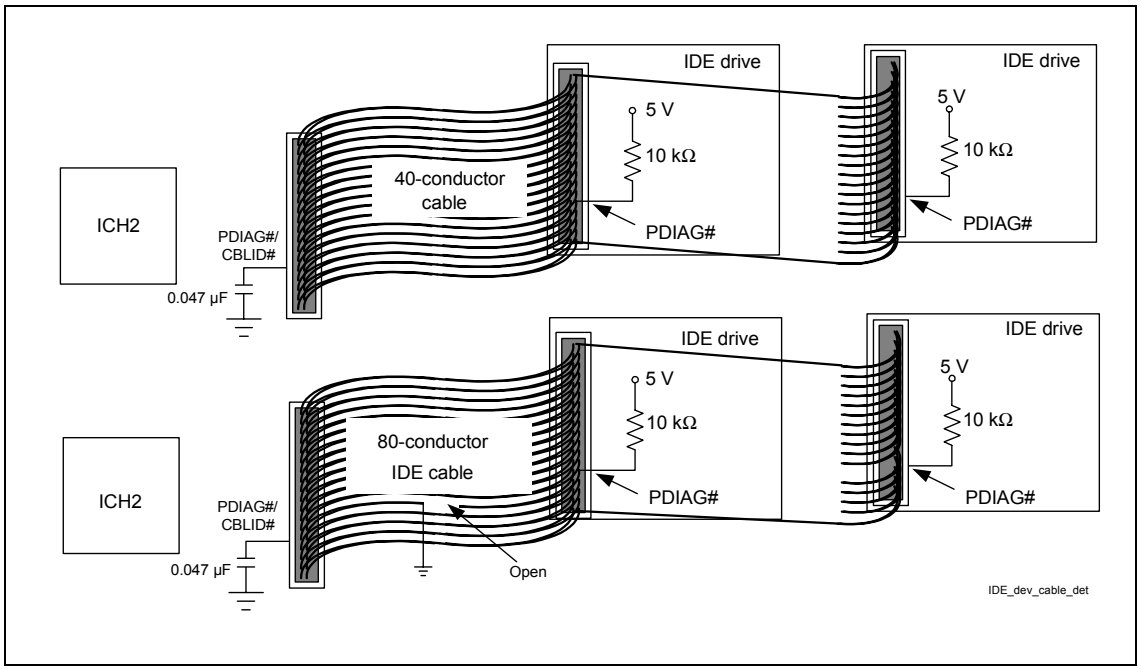

This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is High, then there is a 40-conductor cable in the system and ATA modes 3, 4 and 5 must not be enabled.

If PDIAG#/CBLID# is detected Low, then there may be an 80-conductor cable in the system or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-4 standard. In this case, the BIOS should check the **Identify Device** information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13, is set to 1, then an 80-conductor cable is present. If this bit is set to 0, then a legacy slave (Device 1) is preventing proper cable detection, so the BIOS should configure the system as though a 40-conductor cable were present and then notify the user of the problem.

## 3.12.2. Device-Side Cable Detection

For platforms that must implement device-side detection only (e.g., NLX platforms), a 0.047-µF capacitor is required on the motherboard as shown in the figure below. This capacitor **should not be populated** when implementing the recommended combination host-side/device-side cable detection mechanism described previously.

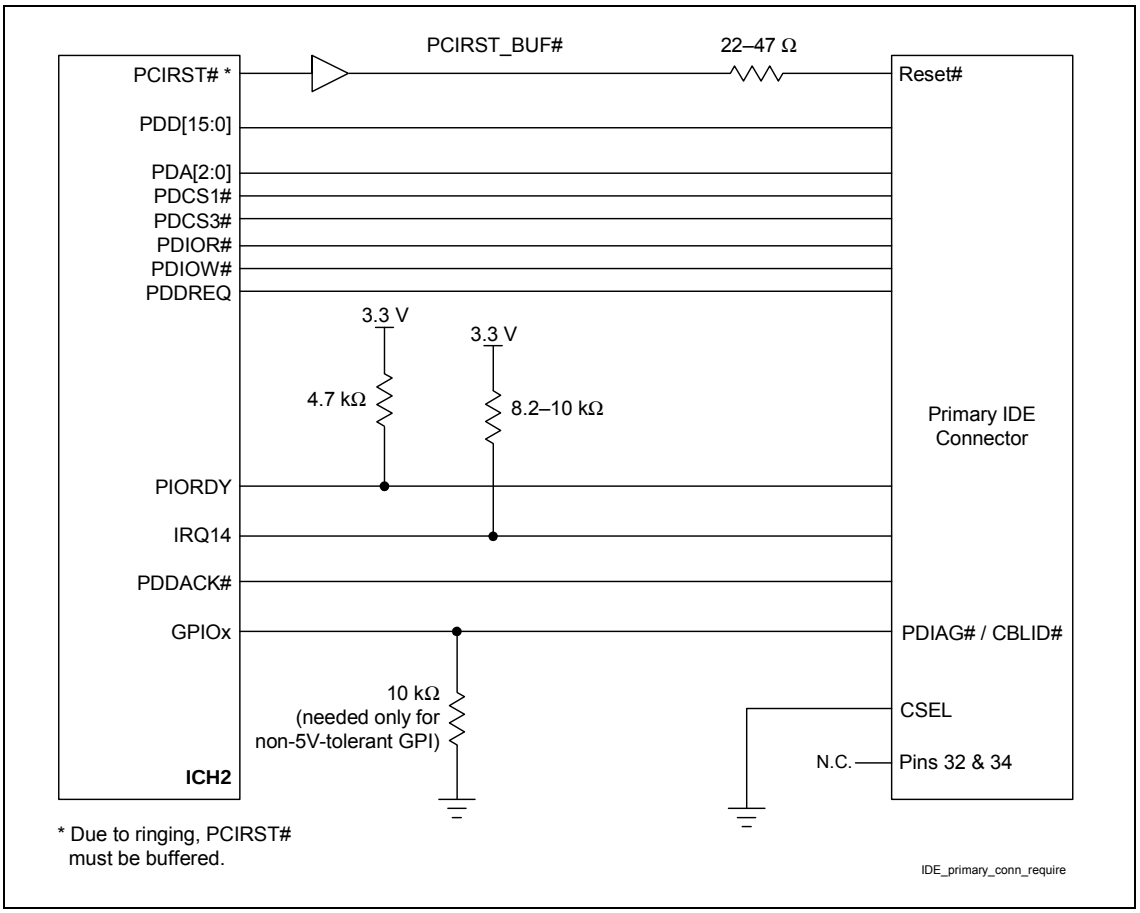
**Figure 29. Device-Side IDE Cable Detection**




This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3, 4 or 5 drive will drive PDIAG#/CBLID# Low and then release it (pulled up through a 10-kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host, so the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host, so the signal will rise more slowly as the capacitor charges. The drive can detect the difference in rise times and will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot, as described in the ATA/66 specification.

## 3.12.3. Primary IDE Connector Requirements

**Figure 30. Connection Requirements for Primary IDE Connector**

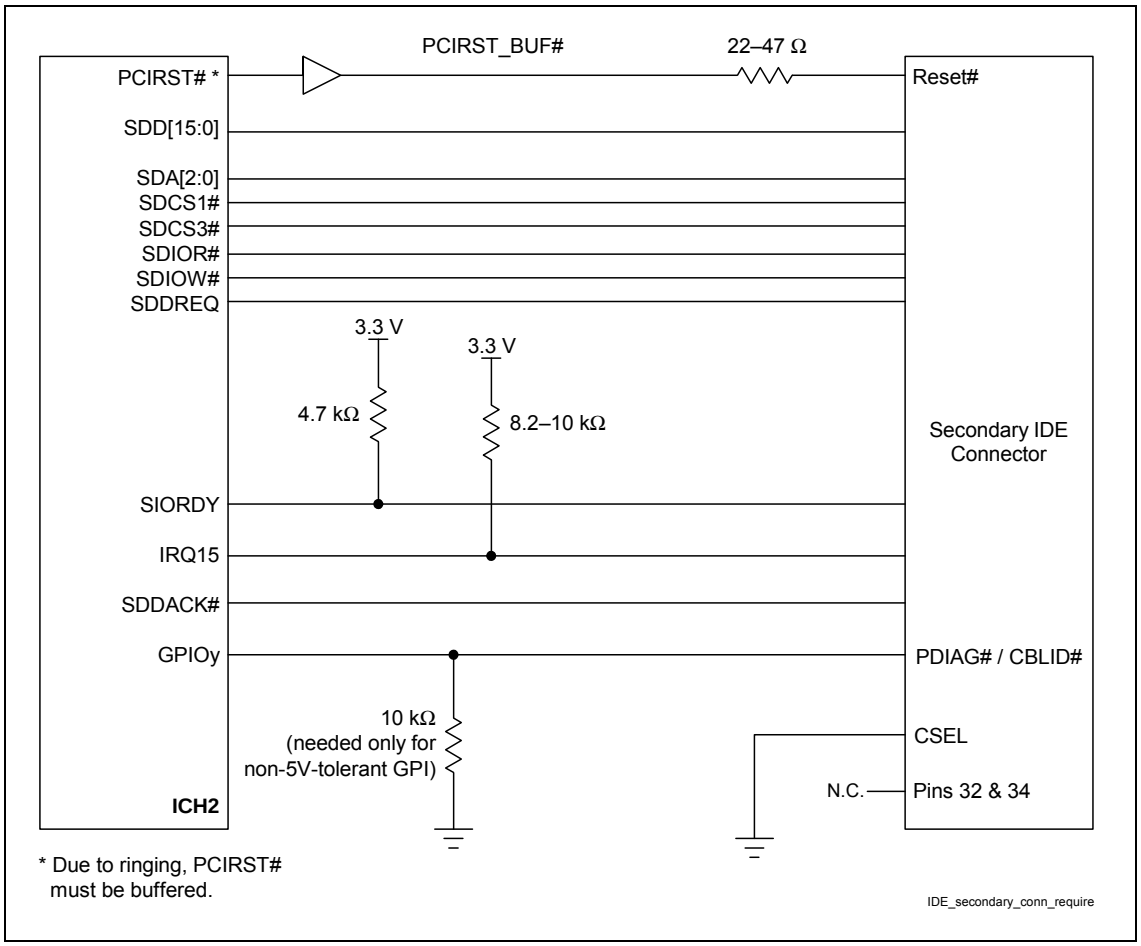



**NOTES:**

1. 22-Ω to 47-Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2-kΩ to 10-kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3.
3. A 4.7-kΩ pull-up resistor to VCC3 is required on PIORDY and SIORDY.
4. Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close as possible to the connector. Values are determined for each unique motherboard design.
5. The 10-kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

## 3.12.4. Secondary IDE Connector Requirements

**Figure 31. Connection Requirements for Secondary IDE Connector**




**NOTES:**

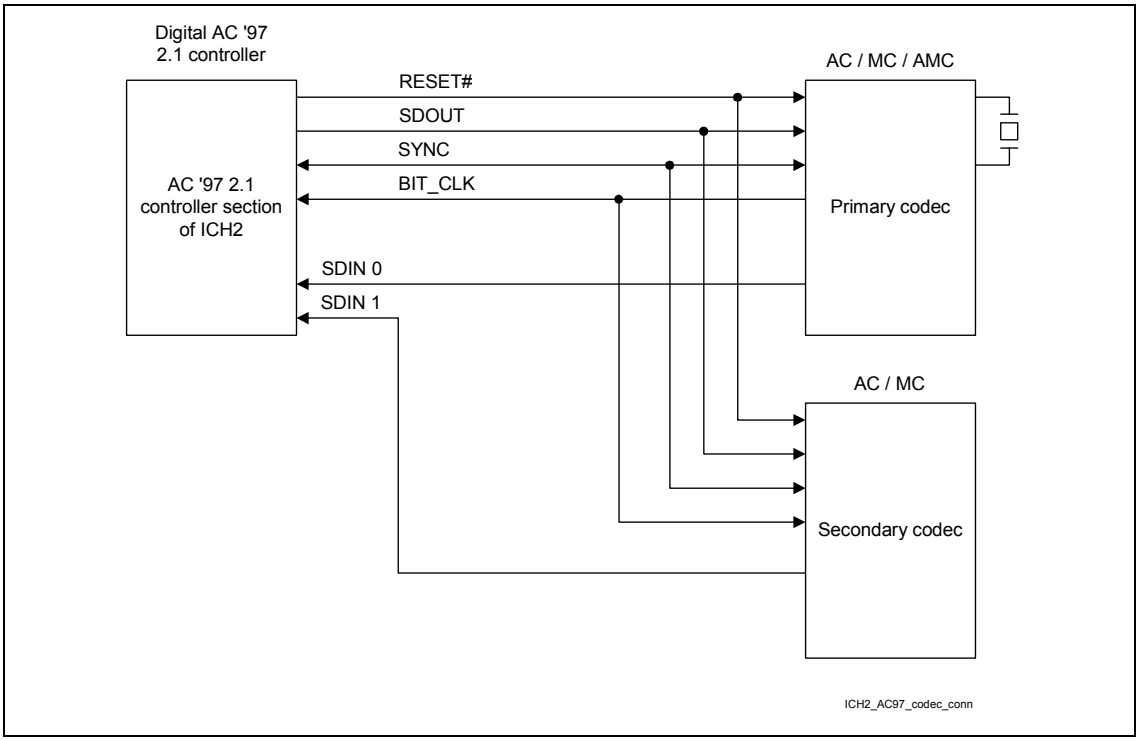
1. 22-Ω to 47-Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2-kΩ to 10-kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3.
3. A 4.7-kΩ pull-up resistor to VCC3 is required on PIORDY and SIORDY
4. Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close as possible to the connector. Values are determined for each unique motherboard design.
5. The 10-kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Secondary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

## 3.13. AC'97

The ICH2 implements an AC'97 2.1-compliant digital controller. Any codec attached to the ICH2 AC-link must be AC'97 2.1 compliant, as well. Contact your codec IHV for information on 2.1-compliant products. The AC'97 2.1 specification is available on the Intel website: http://developer.intel.com/pc-supp/platform/ac97/index.htm.

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, by employing a time-division-multiplexed (TDM) scheme. The AC-link architecture enables data transfer through individual frames transmitted serially. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH2 AC-link allows a maximum of two codecs to be connected. The following figure shows a two-codec topology of the AC-link for the ICH2.

**Figure 32. Intel® ICH2 AC'97– Codec Connection**




Intel has developed an advanced common connector for both AC'97 as well as networking options. This is known as the Communications and Network Riser (CNR). Refer to Section 3.14.

The AC'97 interface can be routed using 5 mil traces with 5 mil space between the traces. Maximum length between ICH2 to CODEC/CNR is 14" in a tee topology. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 4" for the AC-link. Trace impedance should be $Z_0 = 60\ \Omega \pm 15\%$.

Clocking is provided from the primary codec on the link via BITCLK, and it is derived from a 24.576-MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288-MHz clock driven by the primary codec to the digital controller (ICH2) and any other codec present. That clock is used as the timebase for latching and driving data.

The ICH2 supports wake-on-ring from S1–S5 via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

ICH2 has weak pull-downs/pull-ups that are enabled only when the AC-Link Shut-off bit in the ICH2 is set. This keeps the link from floating when the AC-link is off or when there are no codecs present.

If the Shut-off bit is not set, it means that there is a codec on the link. Therefore, BITCLK and AC_SDOUT will be driven by the codec and ICH2, respectively. However, AC_SDIN0 and AC_SDIN1 may not be driven. If the link is enabled, it may be assumed that there is at least one codec. If there only is an on-board codec (i.e., no AMR), then the unused SDIN pin should have a weak (10-kΩ) pull-down to keep it from floating. If an AMR is used, any SDIN signal could be Not Connected (e.g., with no codec, both can be NC), then both SDIN pins must have a 10-kΩ pull-down.

**Table 18. AC'97 SDIN Pull-down Resistors**

| System Solution | Pull-up Requirements |
|---|---|
| On-board codec only | Pull down the SDIN pin that is **not** connected to the codec. |
| AMR only | Pull down **both** SDIN pins. |
| BOTH AMR and on-board codec | Pull down any SDIN pin that could be NC*. |

*If the on-board codec can be disabled, both SDIN pins must have pull-downs. If the on-board codec cannot be disabled, only the SDIN not connected to the on-board codec requires a pull-down.

## 3.13.1. AC'97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. Refer to Intel's White Paper Recommendations for ICHx/AC'97 Audio (Motherboard and Communication and Network Riser) for Intel's recommended codec configurations.

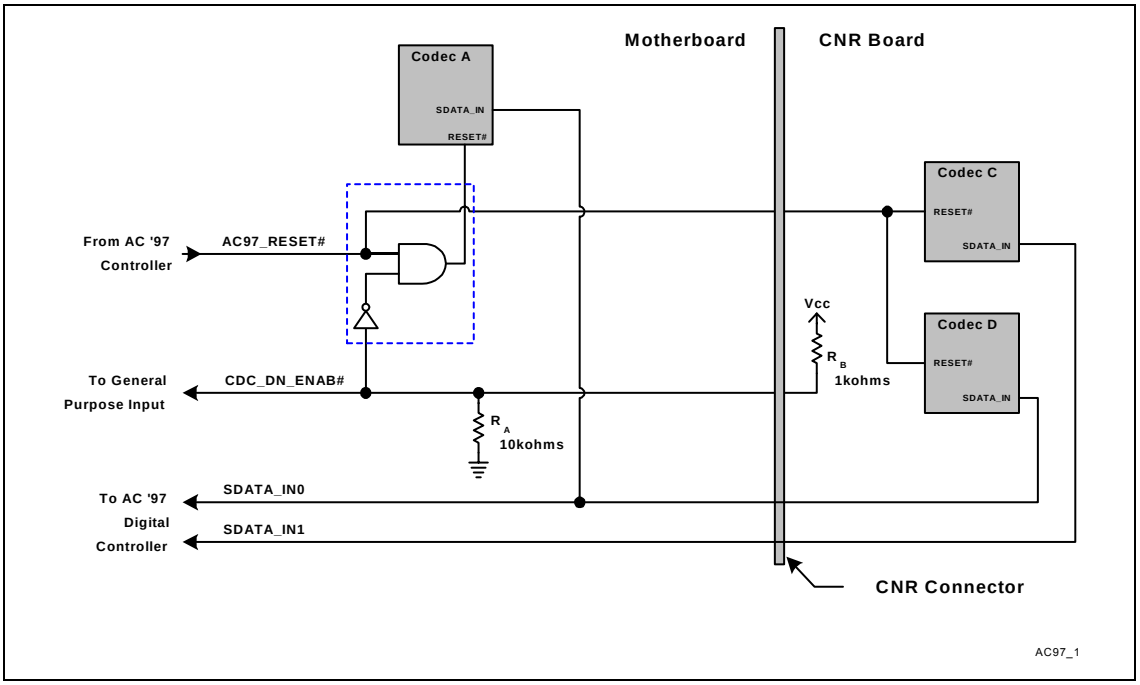
To support more than two channels of audio output, the ICH2 allows for a configuration where two audio codecs work concurrently to provide surround capabilities. To maintain data-on-demand capabilities, the ICH2 AC'97 controller, when configured for 4 or 6 channels, will wait for all the appropriate slot request bits to be set before sending data in the SDATA_OUT slots. This allows for simple FIFO synchronization of the attached codecs. It is assumed that both codecs will be programmed to the same sample rate, and that the codecs have identical (or at least compatible) FIFO depth requirements. It is recommended that the codecs be provided by the same vendor, upon the certification of their interoperability in an audio channel configuration.

The following four circuit figures (Figure 33 to Figure 36)show the adaptability of a system with the modification of $R_A$ and $R_B$ combined with some basic glue logic to support multiple codec configurations. This also provides a mechanism to make sure that only two codecs are enabled in a given configuration and allows the configuration of the link to be determined by BIOS so that the correct PnP IDs can be loaded.

As shown in the following figure, when a single codec is located on the motherboard, the resistor $R_A$ and the circuitry (AND and NOT gates) shown inside the dashed box must be implemented on the motherboard. This circuitry is required to disable the motherboard codec when a CNR is installed containing two AC ’97 codecs (or a single AC ’97 codec that must be the primary codec on the AC-Link).

By installing resistor $R_B$ (1 kΩ) on the CNR, the codec on the motherboard becomes disabled (held in reset) and the codec(s) on the CNR take control of the AC-Link. One possible example of using this architecture is a system integrator installing an audio plus modem CNR in a system already containing an audio codec on the motherboard. The audio codec on the motherboard would then be disabled, allowing all of the codecs on the CNR to be used.

**Figure 33. CDC_DN_ENAB# Support Circuitry for a Single Codec on Motherboard**




The architecture shown in Figure 34 has some unique features. These include the possibility of the CNR being used as an upgrade to the existing audio features of the motherboard (by simply changing the value of resistor $R_B$ on the CNR to 100 kΩ). An example of one such upgrade is increasing from two-channel to four or six-channel audio.

Both Figure 34 and Figure 35 show a switch on the CNR board. This is necessary to connect the CNR board codec to the proper SDATA_IN*n* line so there is not a conflict with the motherboard codec(s).

**Figure 34. CDC_DN_ENAB# Support Circuitry for Multi-Channel Audio Upgrade**

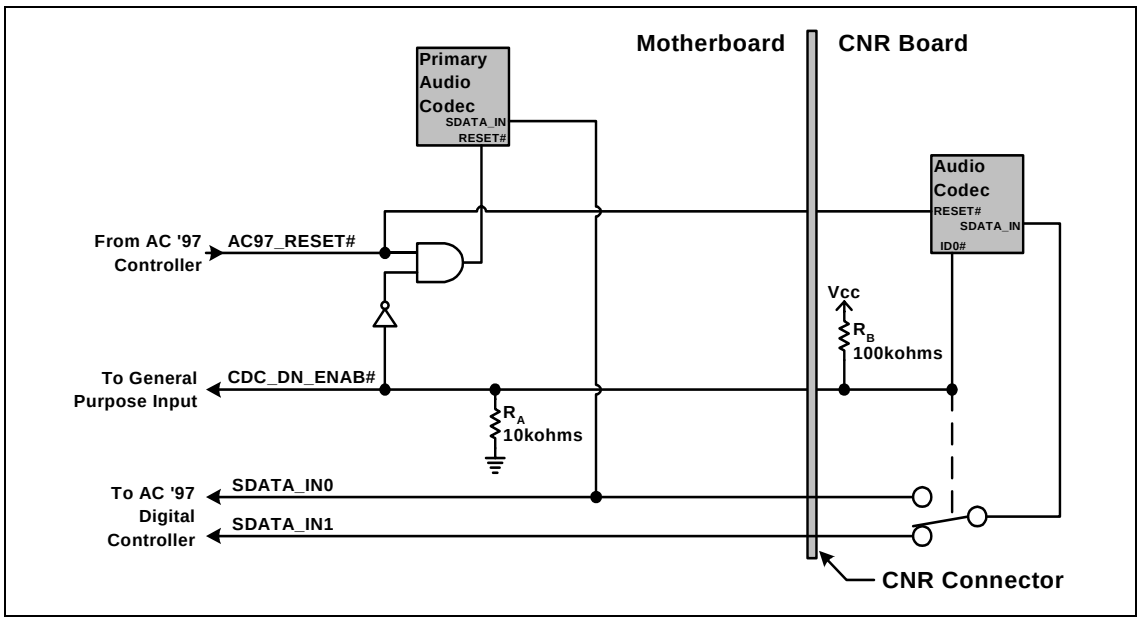
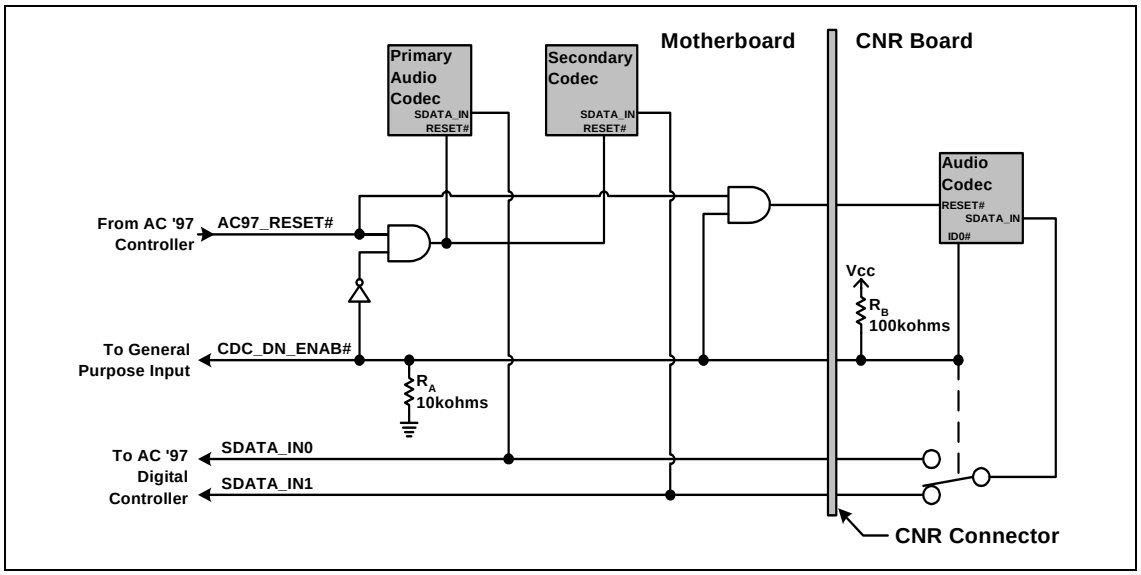


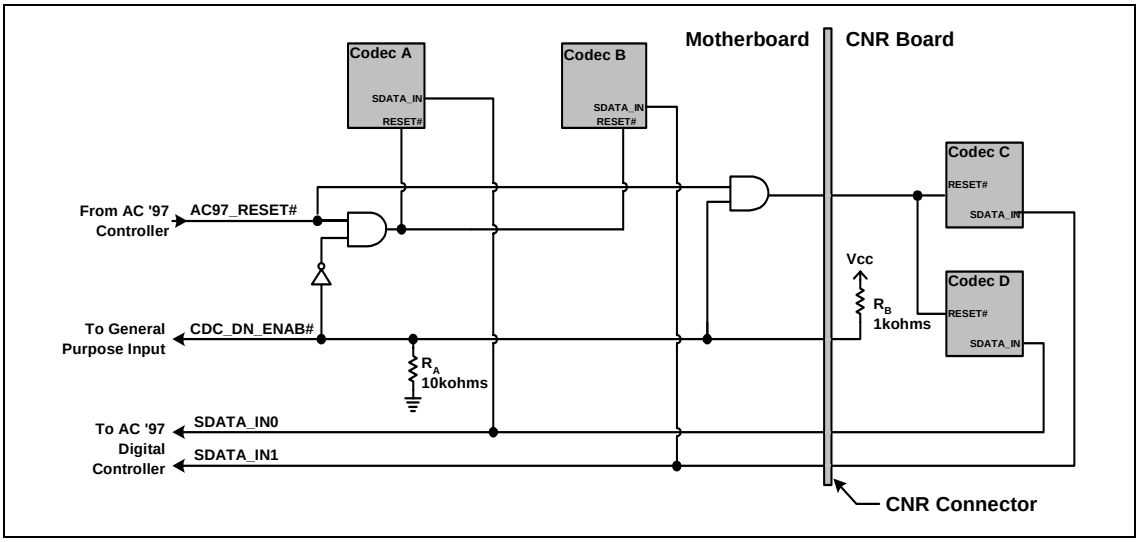

Figure 35 shows the circuitry required on the motherboard to support a two-codec down configuration. This circuitry disables the codec on a single codec CNR. Notice that in this configuration the resistor $R_B$ has been changed to 100 kΩ.

**Figure 35. CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard / One-Codec on CNR**



The following figure shows the case of two-codecs down and a dual-codec CNR. In this case, both codecs on the motherboard are disabled (while both on CNR are active) by $R_A$ being 10 kΩ and $R_B$ being 1 kΩ.

**Figure 36. CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard / Two-Codecs on CNR**




**Circuit Notes (Figure 33 to Figure 36)**

1. While it is possible to disable down codecs, as shown in Figure 33 and Figure 36, it is recommended against for reasons cited in the ICHx/AC'97 White Paper, including avoidance of shipping redundant and/or non-functional audio jacks.
2. All CNR designs include resistor $R_B$. The value of $R_B$ is either 1 kΩ or 100 kΩ, depending on the intended functionality of the CNR (whether or not it intends to be the primary/controlling codec).
3. Any CNR with two codecs must implement $R_B$ with value 1 kΩ. If there is one codec, use a 100 kΩ pull-up resistor. A CNR with zero codecs must not stuff $R_B$. If implemented, $R_B$ must be connected to the same power well as the codec so that it is valid when the codec has power.
4. A motherboard with one or more codecs down must implement $R_A$ with a value of 10 kΩ.
5. The CDC_DN_ENAB# signal must be run to a GPI so that the BIOS can sense the state of the signal. CDC_DN_ENAB# is *required* to be connected to a GPI; a connection to a GPIO is *strongly recommended* for testing purposes.

**Table 19. Signal Descriptions**

| Signal | Description |
|---|---|
| CDC_DN_ENAB# | When low, this signal indicates that the codec on the motherboard is enabled and primary on the AC97 Interface. When high, this signal indicates that the motherboard codec(s) must be removed from the AC '97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC '97 Interface. |
| AC97_RESET# | Reset signal from the AC '97 Digital Controller (ICH2). |
| SDATA_IN*n* | AC '97 serial data from an AC '97-compliant codec to an AC '97-compliant controller (i.e., the ICH2). |

#### 3.13.1.1. Valid Codec Configurations

**Table 20. Codec Configurations**

| Valid Codec Configurations |
|---|
| AC(Primary) |
| MC(Primary) |
| AMC(Primary) |
| AC(Primary) + MC(Secondary) |
| AC(Primary) + AC(Secondary) |
| AC(Primary) + AMC(Secondary) |

| Invalid Codec Configurations |
|---|
| MC(Primary) + X(any other type of codec) |
| AMC(Primary) + AMC(Secondary) |
| AMC(Primary) + MC(Secondary) |

## 3.13.2. SPKR Pin Considerations

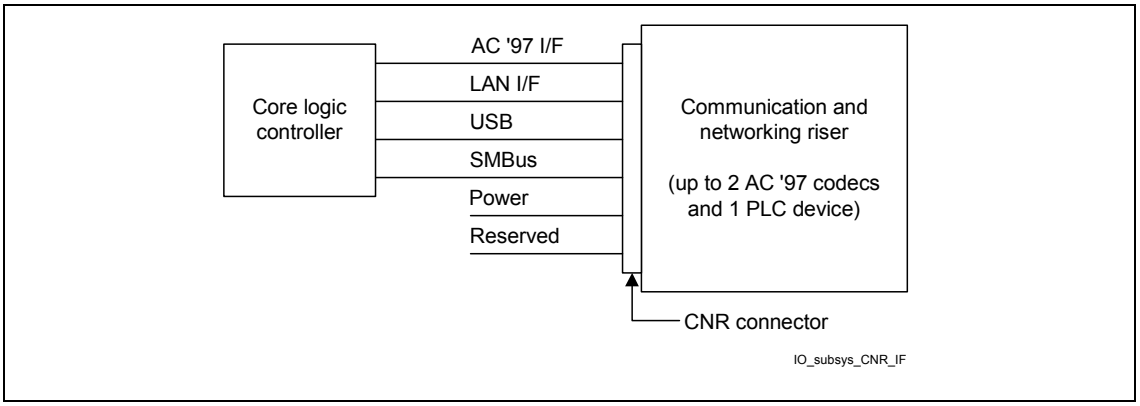
The effective impedance of the speaker and codec circuitry on the SPKR signal line must be greater than 50 kΩ. Failure to due so will cause the TCO Timer Reboot function to be erroneously disabled. SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the “TCO Timer Reboot function” based on the state of the SPKR pin on the rising edge of POWEROK. When enabled, the ICH2 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-up resistor (the resistor is only enabled during boot/reset). Therefore, it is default state when the pin is a “no connect” is a logical one or enabled. To disable the feature, a jumper can be populated to pull the signal line low (see figure). The value of the pull-down must be such that the voltage divider caused by the pull-down and integrated pull-up resistors will be read as logic low. When the jumper is not populated, a low can still be read on the signal line if the effective impedance due to the speaker and codec circuit is equal to or lower than the integrated pull-up resistor. It is therefore strongly recommended that the effective impedance be greater than 50 kΩ and the pull-down resistor be less than 7.3 kΩ.

## 3.14. CNR

The Communication and Networking Riser (CNR) Specification defines a hardware-scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. This interface supports multi-channel audio, a V.90 analog modem, phone-line based networking, and 10/100 Ethernet based networking. The CNR specification defines the interface that should be configured before system shipment. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot. Unlike in the case of the AMR, the system designer will not sacrifice a PCI slot after deciding not to include a CNR in a particular build.

The following figure indicates the interface for the CNR connector. Refer to the appropriate section of this document for the appropriate design and layout guidelines. The Platform LAN Connection (PLC) can either be a 82562EH or 82562ET component. Refer to the CNR specification for additional information.

**Figure 37. CNR Interface**




## 3.15. USB

The general guidelines for the USB interface are as follows:

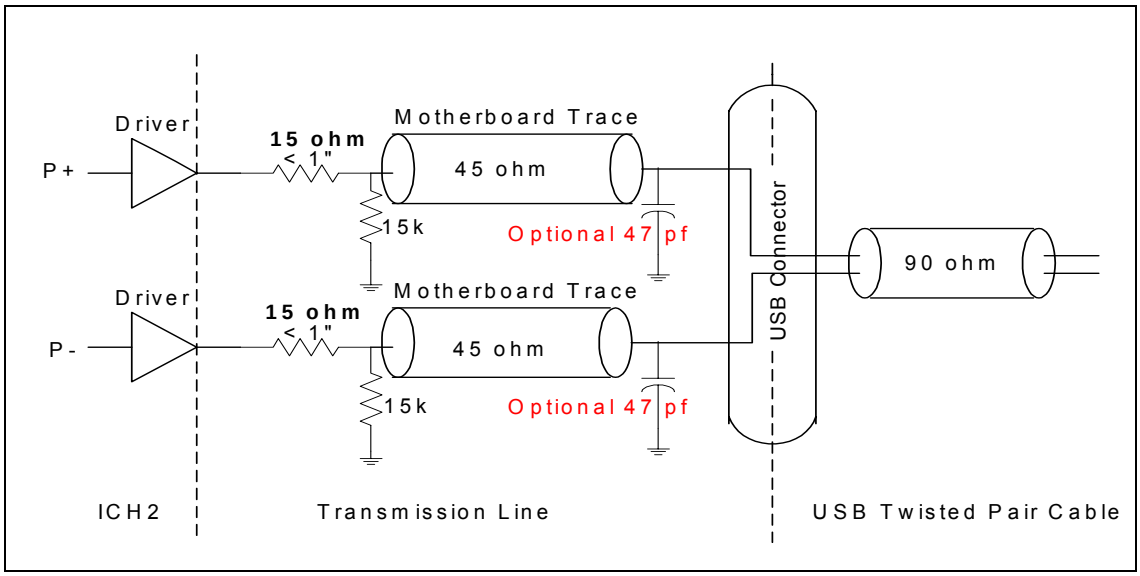
- Unused USB ports should be terminated with 15-kΩ pull-down resistors on both P+/P- data lines.
- 15-Ω series resistors should be placed as close as possible to the ICH2 (<1”). These series resistors are required for source termination of the reflected signal.
- An optional cap (0 pF – 47pF) may be placed as close to the USB connector side of the series resistors on the USB data lines (P0+/-, P1+/-, P2+/-, P3+/-). This cap should be sized to minimize EMI radiation while still maintaining signal quality (rise/fall time, Vcrs, etc).
- 15-kΩ ± 5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0± … P3±), and they are **Required** for signal termination by the USB specification. The stub should be as short as possible.
- The trace impedance for the P0±…P3± signals should be 45 Ω (to ground) for each USB signal P+ or P-. When the stack-up recommended in Figure 10 is used, the USB requires 9-mil traces. The impedance is 90 Ω between the differential signal pairs P+ and P-, to match the 90-Ω USB twisted-pair cable impedance. Note that the twisted-pair’s characteristic impedance of 90 Ω is the series

impedance of both wires, resulting in an individual wire presenting a 45-Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.

- USB data lines must be routed as critical signals. The P+/P- signal pair must be routed together, parallel to each other on the same layer, and not parallel with other non-USB signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI. Lastly, do not route over plane splits.

The following figure illustrates the recommended USB schematic.

**Figure 38. USB Data Signals**




The recommended USB trace characteristics are:

- Impedance ‘Z0’ = 45.4 Ω
- Line Delay = 160.2 ps
- Capacitance = 3.5 pF
- Inductance = 7.3 nH
- Res @ 20° C = 53.9 mΩ

## 3.15.1. Disabling the Native USB Interface of Intel® ICH2

The ICH2 native USB interface can be disabled. This can be done when an external PCI-based USB controller is being implemented in the platform. To disable the native USB Interface, ensure the differential pairs are pulled down thru 15 kΩ resistors, ensure the OC[3:0]# signals are deasserted by pulling them up weakly to VCC3SBY, and that both function 2 & 4 are disabled via the D31:F0;FUNC_DIS register. Ensure that the 48 MHz USB clock is connected to the ICH2 and is kept running. This clock must be maintained even though the internal USB functions are disabled.

## 3.16. ISA

Implementations that require ISA support can benefit from the enhancements of the ICH2, while "ISA-less" designs are not burdened with the complexity and cost of the ISA subsystem. For information regarding the implementation of an ISA design, contact external suppliers.

## 3.17. IOAPIC Design Recommendation

UP systems not using the IOAPIC should comply with the following recommendations:

- On the ICH2:
  - Tie PICCLK directly to ground.
  - Tie PICD0, PICD1 to ground through a 10-kΩ resistor.
- On the processor:
  - PICCLK must be connected from the clock generator to the PICCLK pin on the processor.
  - Tie PICD0 to 2.5 V through 10-kΩ resistors.
  - Tie PICD1 to 2.5 V through 10-kΩ resistors.

## 3.18. SMBus/SMLink Interface

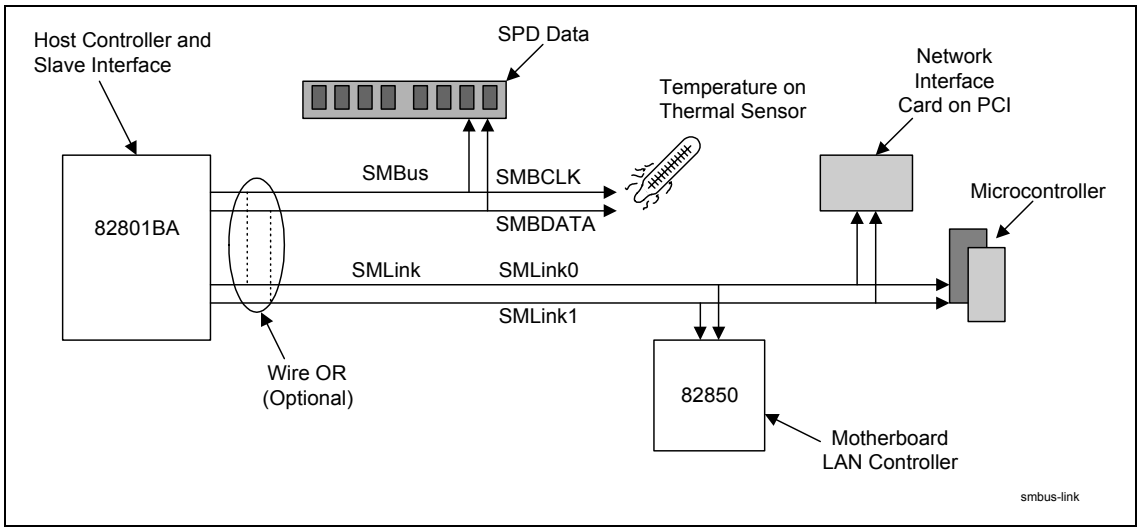
The SMBus interface on the ICH2 is the same as that on the ICH. It uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus host controller. The SMBus host controller resides inside the ICH2.

The ICH2 incorporates a new SMLink interface supporting AOL*, AOL2*, and slave functionality. It uses two signals, SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB slave interface.

For Alert on LAN (AOL) functionality, the ICH2 transmits heartbeat and event messages over the interface. When the 82562EM LAN connect component is used, the ICH2's integrated LAN controller claims the SMLink heartbeat and event messages and sends them out over the network. An external, AOL2-enabled LAN controller will connect to the SMLink signals, to receive heartbeat and event messages as well to as access the ICH2 SMBus slave interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus host controller and the SMBus slave interface obey the SMBus protocol, so the two interfaces can be externally wire-ORed together to allow an external management ASIC to access targets on the SMBus as well as the ICH2 slave interface. This is performed by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA, as shown in the following figure. Since the SMBus and SMLINK are pulled up to VCCSUS3_3, system designers must ensure that they implement proper isolation for any devices that may be powered down while VCCSUS3_3 is still active (i.e., thermal sensors).

### Figure 39. SMBus/SMLink Interface




***Note:*** Intel does not support external access to the ICH2's integrated LAN controller via the SMLink interface. Also, Intel does not support access to the ICH2's SMBus slave interface by the ICH2's SMBus host controller. The following table describes the pull-up requirements for different implementations of the SMBus and SMLink signals.

### Table 21. Pull-up Requirements for SMBus and SMLink

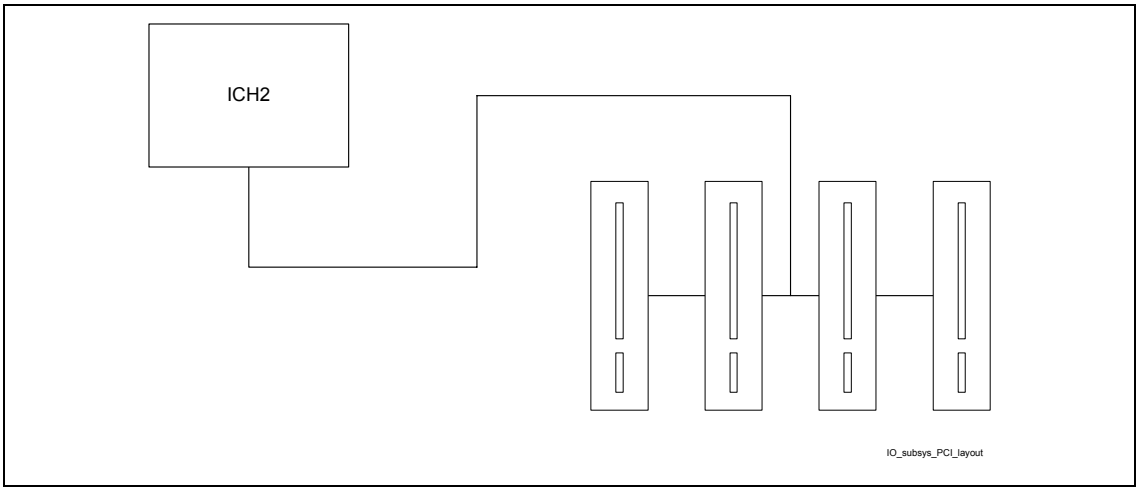
| SMBus / SMLink Use | Implementation |
|---|---|
| Alert-on-LAN* signals | 4.7-kΩ pull-up resistors to 3.3 VSB are required. |
| GPIOs | Pull-up resistors to 3.3 VSB and the signals must be allowed to change states on power-up. (For example, on power-up the ICH2 will drive *heartbeat* messages until the BIOS programs these signals as GPIOs.) The value of the pull-up resistors depends on the loading on the GPIO signal. |
| Not Used | 4.7-kΩ pull-up resistors to 3.3 VSB are required. |

## 3.19. PCI

The ICH2 provides a PCI Bus interface compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH2 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

The ICH2 supports six PCI Bus masters (excluding the ICH2), by providing six REQ#/GNT# pairs. In addition, the ICH2 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

**Figure 40. PCI Bus Layout Example**




## 3.20. RTC

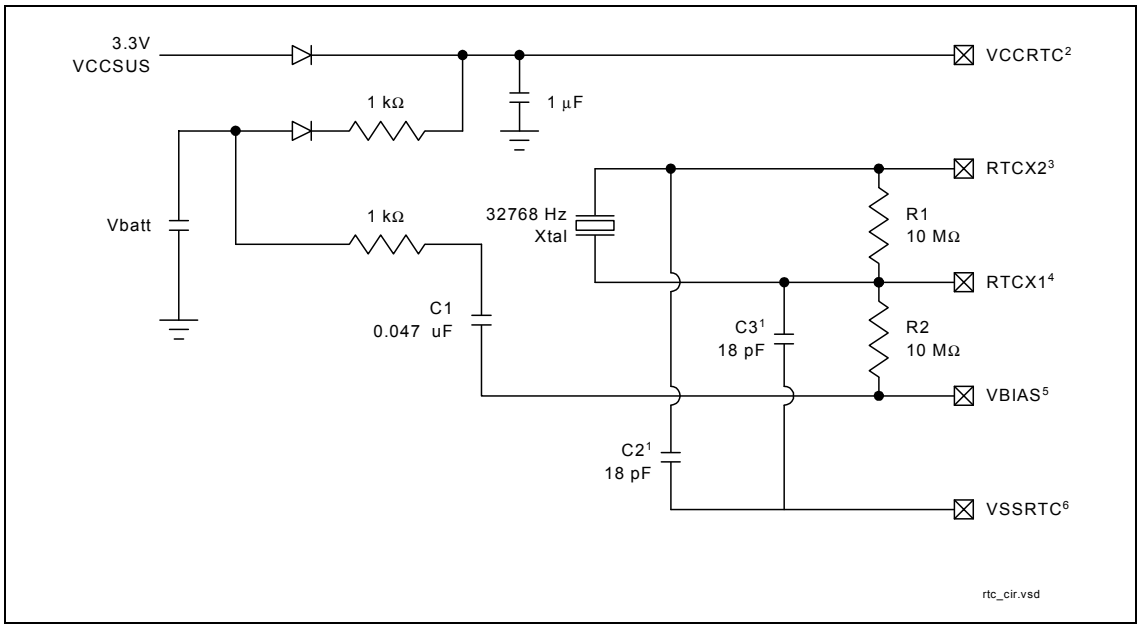
The ICH2 contains a real-time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping the date and time, and storing system data in its RAM when the system is powered down.

This section presents the recommended RTC circuit hook-up for ICH2.

## 3.20.1. RTC Crystal

The ICH2 RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 pins. The following figure documents the external circuitry that comprises the oscillator of the ICH2 RTC.

**Figure 41. External Circuitry for the Intel® ICH2 RTC**




**NOTES:**

1. The exact capacitor value must be based on the crystal maker's recommendation (Typical values for C2 and C3 are 18 pF for a crystal with CLOAD=12.5 pF)
2. VCCRTC: Power for RTC well
3. RTCX2: Crystal input 2 – Connected to the 32.768-kHz crystal.
4. RTCX1: Crystal input 1 – Connected to the 32.768-kHz crystal.
5. VBIAS: RTC BIAS voltage – This pin is used to provide a reference voltage. This DC voltage sets a current that is mirrored throughout the oscillator and buffer circuitry.
6. Vss: Ground

## 3.20.2. External Capacitors

To maintain RTC accuracy, the external capacitor C1 must be 0.047 µF, and the external capacitor values (C2 and C3) should be chosen to provide the manufacturer-specified load capacitance (Cload) for the crystal, when combined with the parasitic capacitance of the trace, socket (if used), and package. When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer the capacitor value can be matched to the actual load capacitance of the crystal used, the more accurate the RTC will be.

The following equation can be used to choose the external capacitance values (C2 and C3):

Cload = (C2 * C3) / (C2 + C3) + Cparasitic

C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain 32.768 kHz.

## 3.20.3. RTC Layout Considerations

- Keep the RTC lead lengths as short as possible. Approximately 0.25” is sufficient.
- Minimize the capacitance between Xin and Xout in the routing.
- Put a ground plane under the XTAL components.
- Do not route switching signals under the external components (unless on the other side of the board).
- The oscillator VCC should be clean. Use a filter (e.g., an RC low-pass or a ferrite inductor).

## 3.20.4. RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH2 is not powered by the system.

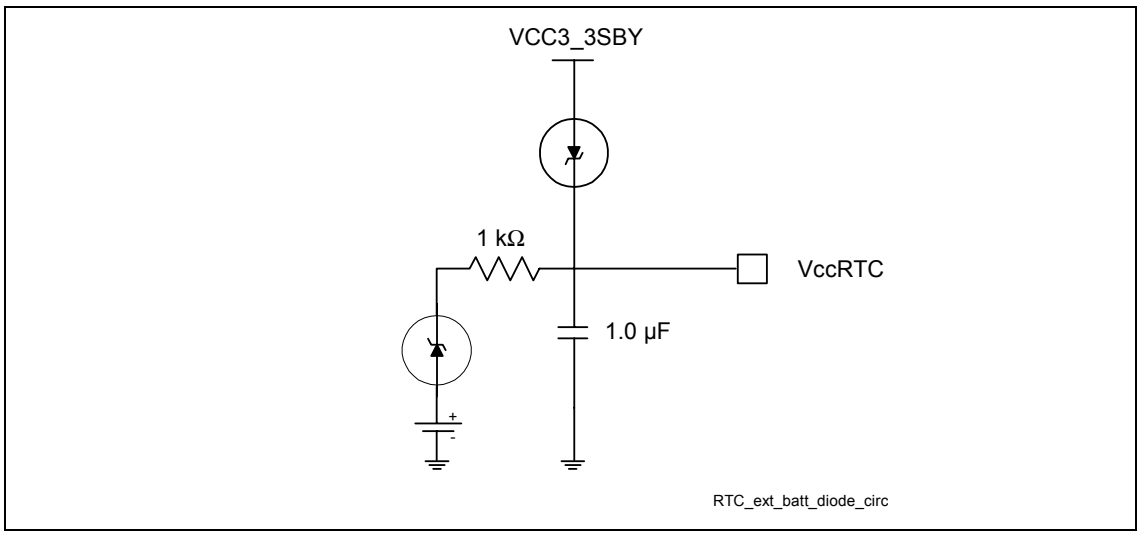
Example batteries include the Duracell* 2032, 2025 or 2016 (or equivalent), that give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 µA, the battery life will be at least:

170,000 µAh / 3 µA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is within the range 3.0 V to 3.3 V.

The battery must be connected to the ICH2 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH2 RTC well to be powered by the battery when system power is unavailable, but by system power when it is available. So, the diodes are set to be reverse-biased when system power is unavailable. The following figure shows an example of the used diode circuitry.

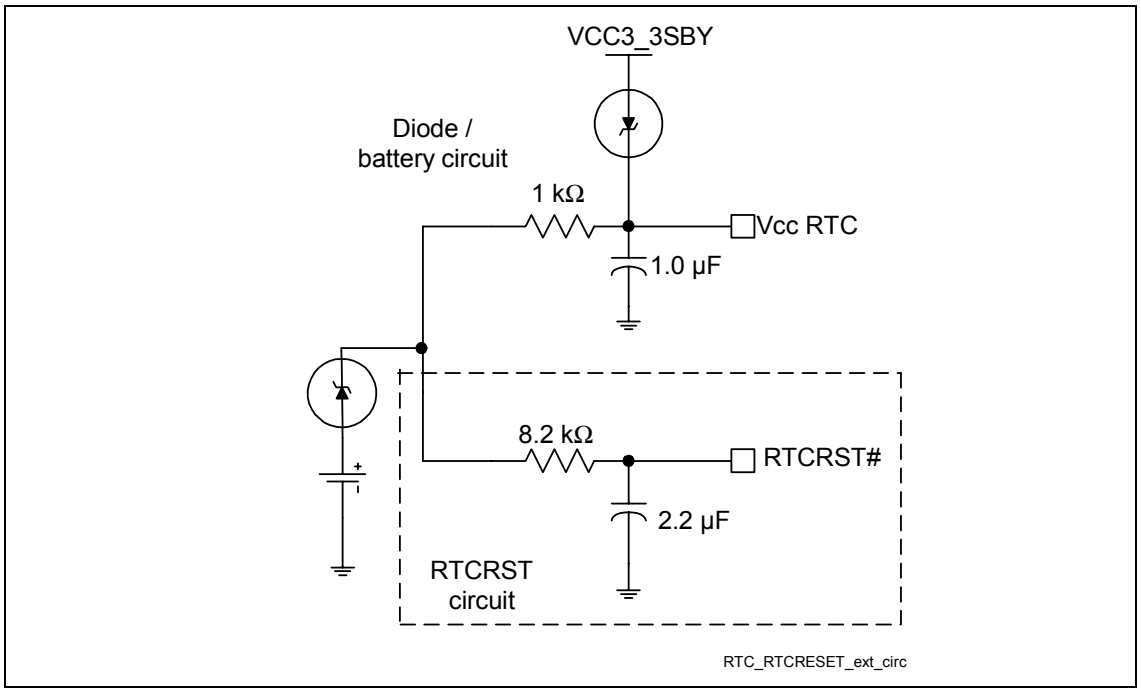
**Figure 42. Diode Circuit to Connect RTC External Battery**




A standby power supply should be used in a desktop system, to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

## 3.20.5. RTC External RTCRST Circuit

**Figure 43. RTCRST External Circuit for Intel® ICH2 RTC**



The ICH2 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create a RC time delay such that RTCRST# goes high some time after the battery voltage is valid. The RC time delay should be within the range of 10–20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1 and remains set until cleared by software. As a result, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (see previous figure) that allows the RTC well to be powered by the battery when system power is unavailable. The previous figure shows an example of this circuitry when used in conjunction with the external diode circuit.

## 3.20.6. RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths less than 1”. The shorter, the better.
- Minimize the capacitance between RTCX1 and RTCX2 in the routing. (Optimally, there would be a ground line between them.)
- Put a ground plane under all external RTC circuitry.
- Do not route any switching signals under the external components (unless on the other side of the ground plane).

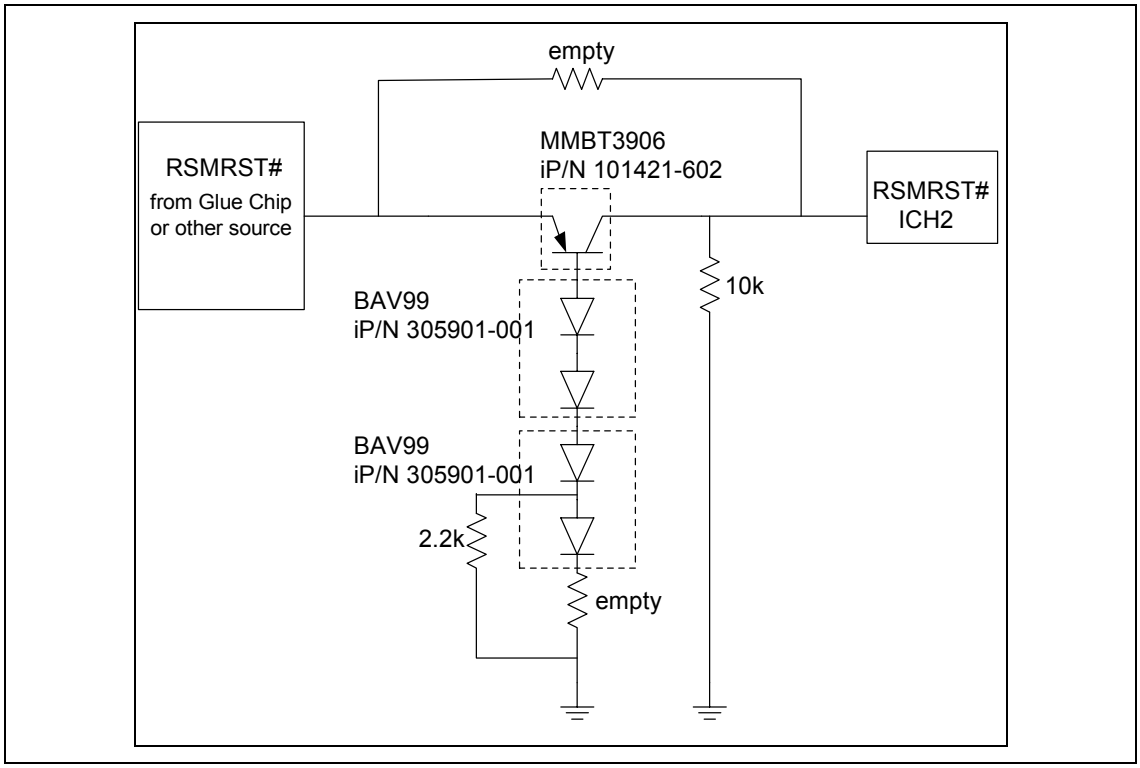
## 3.20.7. VBIAS DC Voltage and Noise Measurements

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths less than 1”. The shorter, the better.
- Steady-state VBIAS is a DC voltage of about 0.38 V ± 0.06 V.
- When the battery is inserted, VBIAS will be “kicked” to about 0.7–1.0 V, but it will return to its DC value within a few ms.
- Noise on VBIAS must be kept to a minimum (200 mV or less).
- VBIAS is very sensitive and cannot be directly probed, but it can be probed through a .01-µF capacitor.
- Excessive noise on VBIAS can cause the ICH2 internal oscillator to misbehave or even stop completely.
- To minimize VBIAS noise, it is necessary to implement the routing guidelines described previously as well as the required external RTC circuitry, as described in the *Intel® 82801BA I/O Controller Hub 2 (ICH2) Datasheet*.

## 3.20.8. Power-well Isolation Control

The circuit shown in the figure below should be implemented to control well isolation between the3.3V resume and RTC power-wells. Failure to implement this circuit may result in excessive droop on the VCCRTC node during Sx- to-G3 power state transitions (removal of AC power).

**Figure 44. RTC Power-well Isolation Control**



# 3.21. LAN Layout Guidelines

The ICH2 provides several options for integrated LAN capability. The platform supports several components depending on the target market. These guidelines use the 82562ET to refer to both the 82562ET and 82562EM. The 82562EM is specified in those cases where there is a difference.

| LAN Connect Component | Connection | Features |
|---|---|---|
| Intel® 82562EM | Advanced 10/100 Ethernet | AOL* & Ethernet 10/100 connection |
| Intel® 82562ET | 10/100 Ethernet | Ethernet 10/100 connection |
| Intel® 82562EH | 1-Mb HomePNA* LAN | 1-Mb HomePNA connection |

Intel developed a dual footprint for the 82562ET and 82562EH, to minimize the required number of board builds. A single layout with the specified dual footprint allows the OEM to install the appropriate LAN connect component to satisfy market demand. Design guidelines are provided for each required interface and connection. Refer to the following figure and table for the corresponding section of the design guide. Dual footprint guidelines are in Section 3.21.4.6.

**Figure 45. Intel® ICH2 / LAN Connect Section**

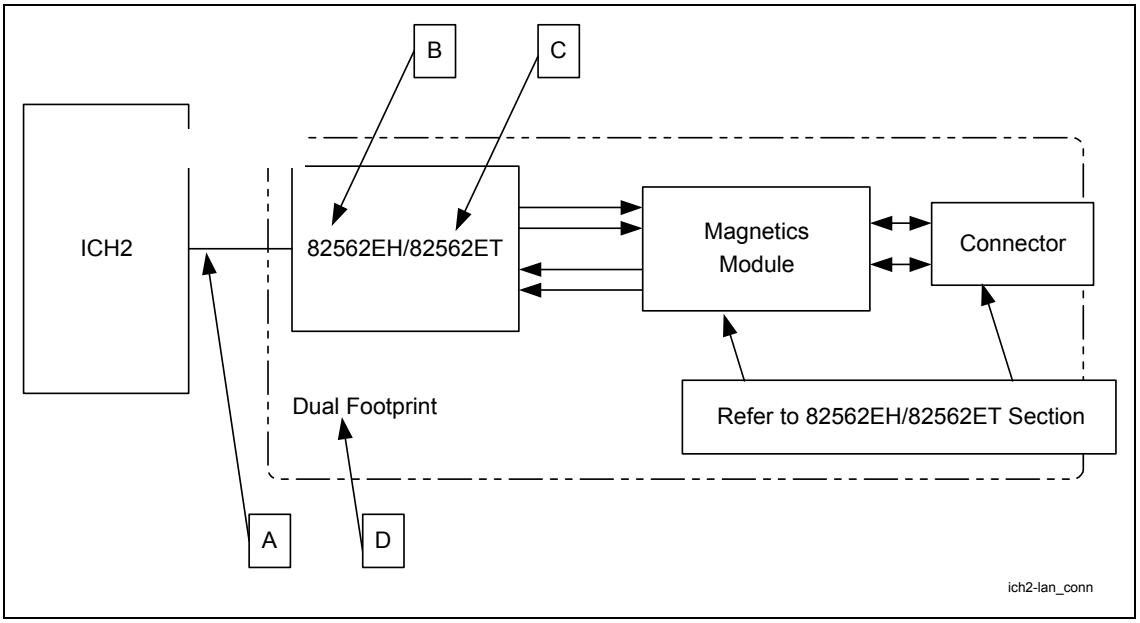


**Table 22. LAN Design Guide Section Reference**

| Layout Section | Figure Ref. | Design Guide Section |
|---|---|---|
| Intel® ICH2 – LAN interconnect | A | Section 3.21.1 Intel® ICH2 – LAN Interconnect Guidelines |
| General routing guidelines | B,C,D | Section 3.21.2 General LAN Routing Guidelines and Considerations |
| Intel® 82562EH | B | Section 3.21.3 Intel® 82562EH Home/PNA* Guidelines |
| Intel® 82562ET /82562EM | C | Section 3.21.4 Intel® 82562ET / 82562EM Guidelines |
| Dual layout footprint | D | Section Intel® 82562ET/EM Disable Guidelines 82562ET/EM Disable Guidelines |

## 3.21.1. Intel® ICH2 – LAN Interconnect Guidelines

This section contains the guidelines for the design of motherboards and riser cards that comply with LAN connect. It should not be considered a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be taken to match the **LAN_CLK** traces with those of the other signals, as follows. The following guidelines are for the ICH2-to-LAN component interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports both 82562EH and 82562ET/82562EM components. Both components share signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0]. Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected when 82562EH is installed.

### 3.21.1.1. Bus Topologies

The LAN connect interface can be configured in several topologies:

- Direct point-to-point connection between the ICH2 and the LAN component
- Dual footprint
- LOM/CNR implementation

### 3.21.1.2. Point-to-Point Interconnect

The following guidelines are for a single-solution motherboard. Either 82562EH, 82562ET or CNR is installed.

**Figure 46. Single-Solution Interconnect**

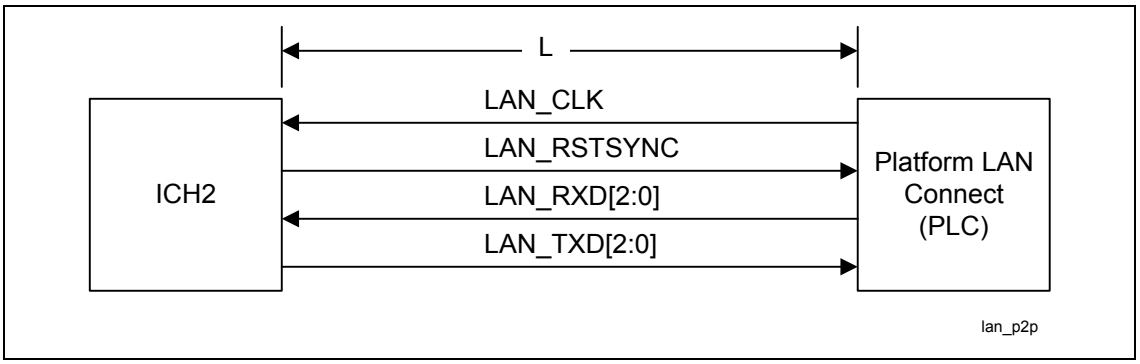



**Table 23. Single-Solution Interconnect Length Requirements**

| Configuration | L | Comment |
|---|---|---|
| Intel® 82562EH | 4.5” to 10” | Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected. |
| Intel® 82562ET | 3.5” to 10” | |
| CNR | 3” to 9” | The trace length from the connector to LOM should be 0.5” to 3.0” |

### 3.21.1.3. LOM/CNR Interconnect

The following guidelines allow for an all-inclusive motherboard solution. This layout combines the LOM, dual-footprint, and CNR solutions. The resistor pack ensures that either a CNR option or a LAN on Motherboard option can be implemented at one time, as shown in the following figure. This figure shows the recommended trace routing lengths.

**Figure 47. LOM/CNR Interconnect**

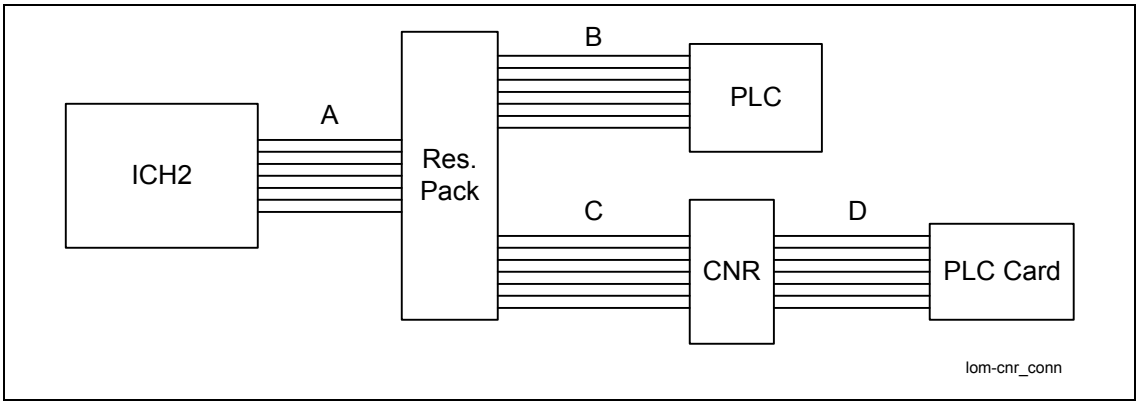


**Table 24. LOM/CNR Length Requirements**

| Configuration | A | B | C | D |
|---|---|---|---|---|
| Intel® 82562EH | 0.5” to 6.0” | 4.0” to (10.0” – A) | | |
| Intel® 82562ET | 0.5” to 7.0” | 3.0” to (10.0” – A) | | |
| Dual footprint | 0.5” to 6.5” | 3.5” to (10.0” – A) | | |
| Intel® 82562ET/EH card* | 0.5” to 6.5” | | 2.5” to (9” – A) | 0.5” to 3.0” |

**NOTES:**
1. The total trace length should not exceed 13”.

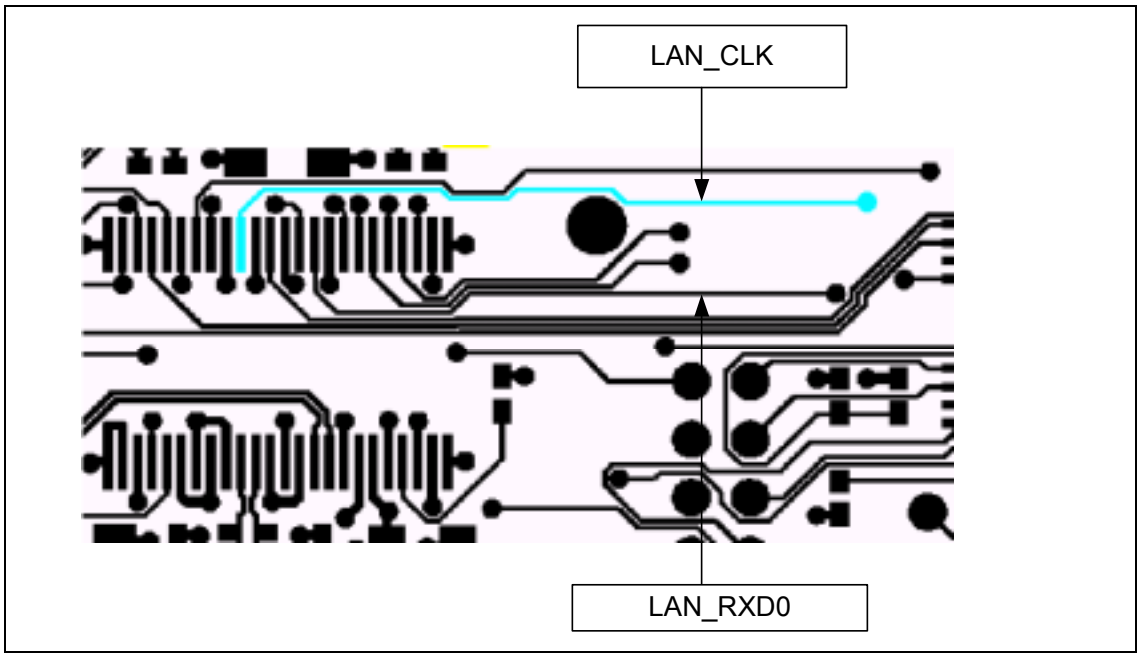
Additional guidelines for this configuration are as follows:

- Stubs due to the resistor pack should not be present on the interface.
- The resistor pack value can be 0 Ω or 22 Ω.
- LAN on Motherboard PLC can be a dual-footprint configuration.

### 3.21.1.4. Signal Routing and Layout

LAN connect signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some of the general guidelines that should be followed. It is recommended that the board designer simulate the board routing, to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard, the length of each data trace is either equal in length to the **LAN_CLK** trace or up to 0.5” shorter than the **LAN_CLK** trace. (**LAN_CLK** should always be the longest motherboard trace in each group.)

**Figure 48. LAN_CLK Routing Example**



#### 3.21.1.5. Crosstalk Consideration

Noise due to crosstalk must be carefully minimized. Crosstalk is the main cause of timing skews and is the largest part of the $t_{RMATCH}$ skew parameter.

#### 3.21.1.6. Impedances

Motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 Ω ± 15% is strongly recommended. Otherwise, signal integrity requirements may be violated.

#### 3.21.1.7. Line Termination

Line termination mechanisms are not specified for the LAN connect interface. Slew-rate-controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 33-Ω series resistor can be installed at the driver side of the interface, if the developer has concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

### 3.21.2. General LAN Routing Guidelines and Considerations

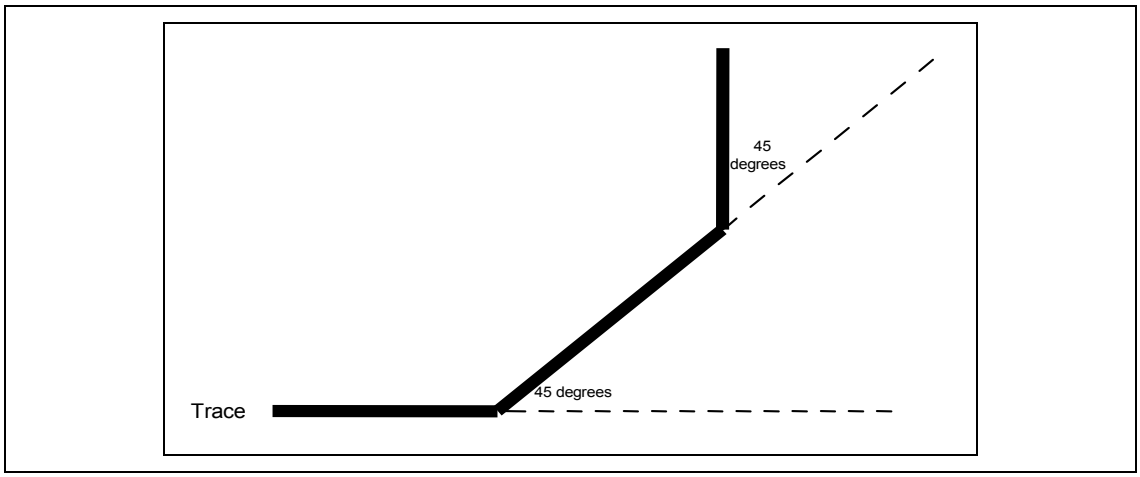
#### 3.21.2.1. General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance:

- The maximum mismatch between the clock trace length and the length of any data trace is 0.5”.
- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4”. (Many customer designs with differential traces longer than 5” have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER.)
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep to 7 mils the maximum separation between differential pairs.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. Refer to the following figure.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures, by a distance exceeding the largest aperture dimension.

**Figure 49. Trace Routing**




## Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace width to trace height above the ground plane. To minimize trace inductance, high-speed signals and signal layers close to a ground or power plane should be as short and wide as practical. Ideally, this ratio of trace width to height above the ground plane is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another, if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling. This can lower the differential impedance by 10 Ω when the traces within a pair are closer than 0.030” (edge-to-edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long-and-thin traces are more inductive and would reduce the intended effect of the decoupling capacitors. For similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should have diameters sufficiently large to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

## Signal Isolation

Comply with the following rules for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Phoneline and Ethernet) and other nets, but group associated differential pairs together.

***Note:*** Over the length of the trace run, each differential pair should be at least 0.3” away from any parallel signal trace.

- Physically group together all components associated with one clock trace, to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor or other similar device.

### 3.21.2.2. Power and Ground Connections

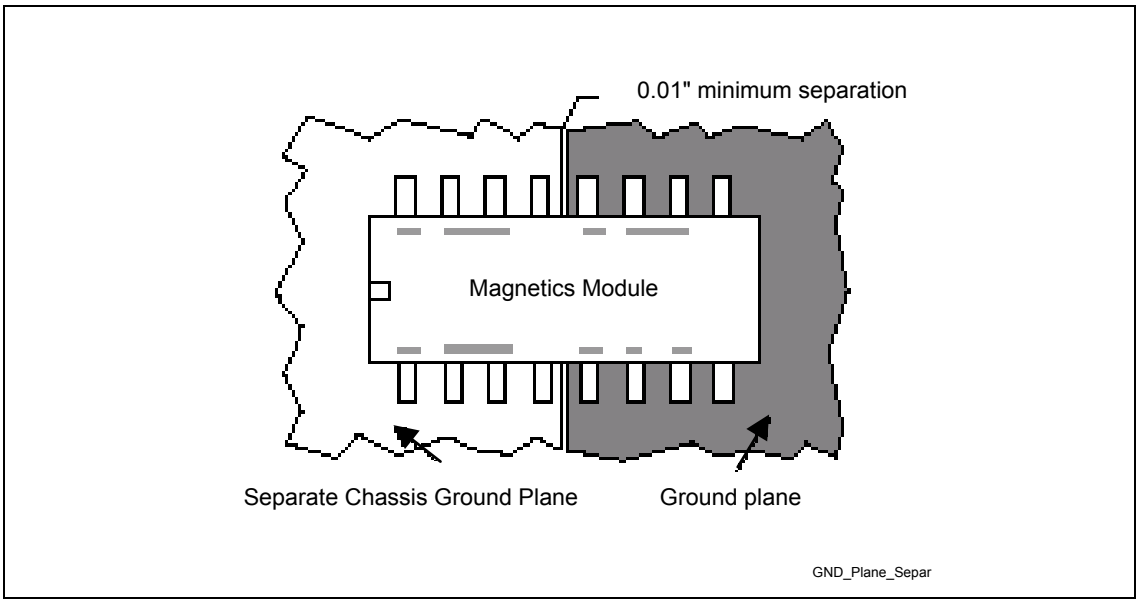
Comply with the following rules and guidelines for power and ground connections:

- All VCC pins should be connected to the same power supply.
- All VSS pins should be connected to the same ground plane.
- Use one decoupling capacitor per power pin for optimized performance.
- Place decoupling as close as possible to power pins.

#### General Power and Ground Plane Considerations

To properly implement the common-mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be physically separated from the digital or input ground (primary side) by at least 100 mils.

**Figure 50. Ground Plane Separation**




Good grounding requires minimizing inductance levels in the interconnections. Keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return will significantly reduce EMI radiation.

Comply with the following rules to help reduce circuit inductance in both backplanes and motherboards:

- *Route traces over a continuous plane with no interruptions (i.e., do not route over a split plane).* If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- To reduce coupling, separate noisy digital grounds from analog grounds.
- Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- *Physically locate grounds between a signal path and its return.* This minimizes the loop area.
- *Avoid fast rise/fall times as much as possible.* Signals with fast rise and fall times contain many high-frequency harmonics that can radiate EMI.
- *The ground plane beneath the filter/transformer module should be split. The RJ45 and/or RJ11 connector side of the transformer module should have chassis ground beneath it.* Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between adjacent coils in the transformer. There should not be a power plane under the magnetics module.
- *Create a spark gap between pins 2 through 5 of the Phoneline connector(s) and shield ground of 1.6mm (59.0 mil).* This is a ***critical*** requirement needed to past FCC part 68 testing for Phoneline connection.
  Note: For worldwide certification a trench of 2.5 mm is required. In North America, the spacing requirement is 1.6 mm. However, home networking can be used in other parts of the world, including Europe, where some Nordic countries require the 2.5 mm spacing.

### 3.21.2.3. A 4-Layer Board Design

#### Top-Layer Routing

Sensitive analog signals are routed completely on the top layer without the use of vias. This allows tight control of signal integrity and removes any impedance inconsistencies due to layer changes.

#### Ground Plane

A layout split (100 mils) of the ground plane under the magnetics module between the primary and secondary side of the module is recommended. It is also recommended to minimize the digital noise injected into the 82562 common ground plane. Suggestions include optimizing decoupling on neighboring noisy digital components, isolating the 82562 digital ground using a ground cutout, etc.

#### Power Plane

Physically separate digital and analog power planes must be provided to prevent digital switching noise from being coupled into the analog power supply planes VDD_A. Analog power may be a metal fill “island,” separated from digital power, and better filtered than digital power.

#### Bottom-Layer Routing

Digital high-speed signals, which include all LAN interconnect interface signals, are routed on the bottom layer.

### 3.21.2.4. Common Physical Layout Issues

Common physical layer design and layout mistakes in LAN on Motherboard designs are as follows:

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and distort transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. (For each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise, and distort the waveforms.
3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45/11 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a specification-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (≤1 inch).
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk on the receive channel will induce degraded long-cable BER. When crosstalk gets onto the transmit channel, it can cause excessive emissions (below the FCC standard) and can cause poor transmit BER on long cables. Other signals should be kept at least 0.3” from the differential traces.
5. Routing the transmit differential traces next to the receive differential traces. The transmit trace closest to one of the receive traces will put more crosstalk onto the closest receive trace; this can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3” or more away from the nearest receive trace. In the vicinities where the traces enter or exit the magnetics, the RJ-45/11 and the PLC are the only possible exceptions.
6. Use of an inferior magnetics module. The magnetics modules used by Intel have been fully tested for IEEE PLC conformance, long-cable BER problems, and emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto-transformer in the transmit channel.)
7. Another common mistake is using an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different, and there also are differences in the receive circuit. Use the appropriate reference schematic or application notes.
8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45/11 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and capacitor or termination plane. If these are not terminated properly, there can be emission (FCC) problems, IEEE conformance issues, and long-cable noise (BER) problems. The application notes contain schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they have designed for 100 Ω. (To calculate the differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close (see Note) to each other, the edge coupling can lower the effective differential impedance by 5 Ω to 20 Ω. A 10-Ω to 15-Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.
10. Another common problem is to use a too-large capacitor between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the 82562ET side of the magnetics)

to ground. Using capacitors with capacitances exceeding a few pF in either of these locations can slow the 100-Mbps rise and fall times so much that they fail the IEEE rise time and fall time specifications. This will cause the return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. (Reasonably good success has been achieved by using 6-pF to 12-pF values in past designs.) Unless there is some overshoot in the 100-Mbps mode, these caps are not necessary.

***Note:*** It is important to keep the two traces within a differential pair close to each other. Keeping them close helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces and better receive BER for the receive traces. Close should be considered to be less than 0.030 inches between the two traces within a differential pair (0.007 inch trace-to-trace spacing is recommended).

## 3.21.3. Intel® 82562EH Home/PNA* Guidelines

### Related Documents

| Title | Location |
|---|---|
| Intel® 82562EH HomePNA 1-Mb/s Physical Layer Interface Datasheet (Order number: 278313) | Intel's website for developers is at: http://developer.intel.com |
| Intel® 82562EH HomePNA 1-Mb/s Physical Layer Interface Brief Datasheet (Order number: 278314) | Intel's website for developers is at: http://developer.intel.com |

For correct LAN performance, designers must follow the general guidelines outlined in Section 3.21.2. Additional guidelines for implementing a 82562EH Home/PNA* LAN connect component are listed in the following sections.

### 3.21.3.1. Power and Ground Connections

Obey the following rule for power and ground connections:

- For best performance, place decoupling capacitors on the back side of the PCB, directly under the 82562EH, with equal distance from both pins of the capacitor to power/ground.

The analog power supply pins for 82562EH (VCCA, VSSA) should be isolated from the digital VCC and VSS through the use of ferrite beads. In addition, adequate filtering and decoupling capacitors should be provided between VCC and VSS as well as the VCCA and VSSA power supplies.

### 3.21.3.2. Guidelines for Intel® 82562EH Component Placement

Component placement can affect the signal quality, emissions, and temperature of a board design. This section discusses guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could result in failure to meet FCC specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

It is important to minimize the space needed for the HomePNA LAN interface, because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HomePNA LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

### 3.21.3.3. Crystals and Oscillators

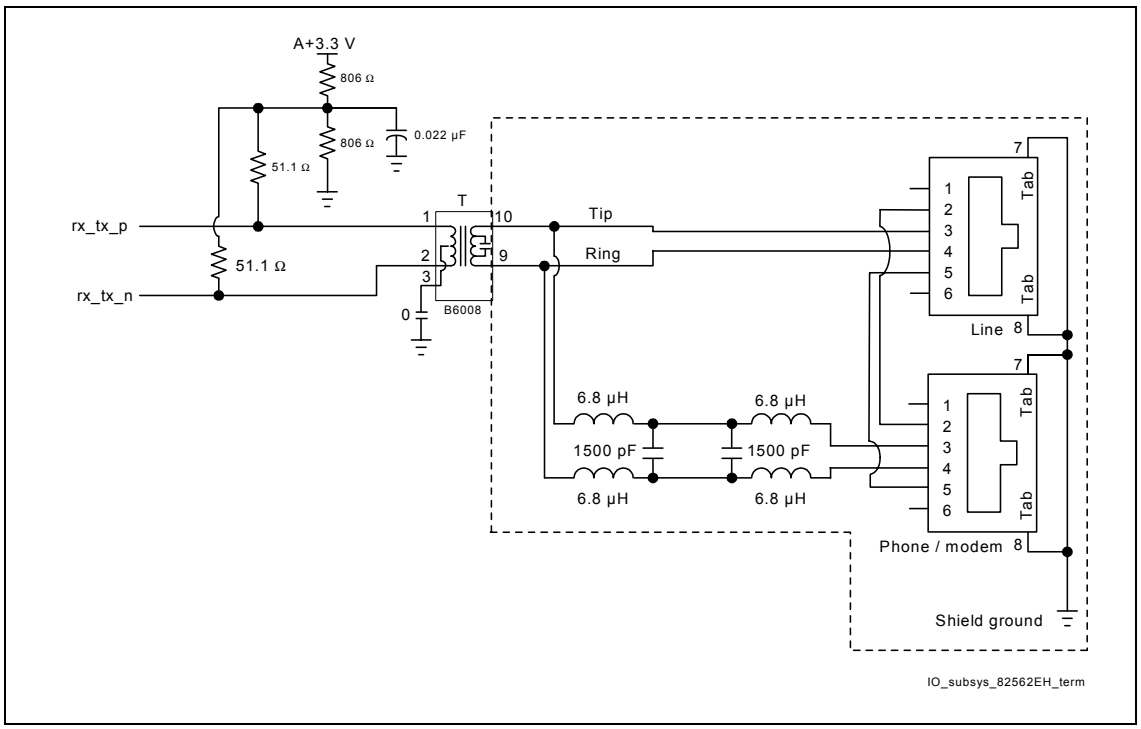
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the HomePNA magnetics module to prevent communication interference. If they exist, the crystal's retaining straps should be grounded to prevent the possibility of radiation from the crystal case, and the crystal should lie flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise-free and stable operation, place the crystal and associated discrete components as close as possible to the 82562EH. Minimize the length and do not route any noisy signals in this area.

### 3.21.3.4. Phoneline HPNA Termination

The transmit/receive differential signal pair is terminated with a pair of 51.1-Ω (1%) resistors. This parallel termination should be placed close to the 82562EH. The center, common point between the 51.1-Ω resistors is connected to a voltage-divider network. The termination is shown in the following figure.

### Figure 51. Intel® 82562EH Termination




The filter and magnetics component T1 integrates the required filter network, high-voltage impulse protection, and transformer to support the HomePNA LAN interface.

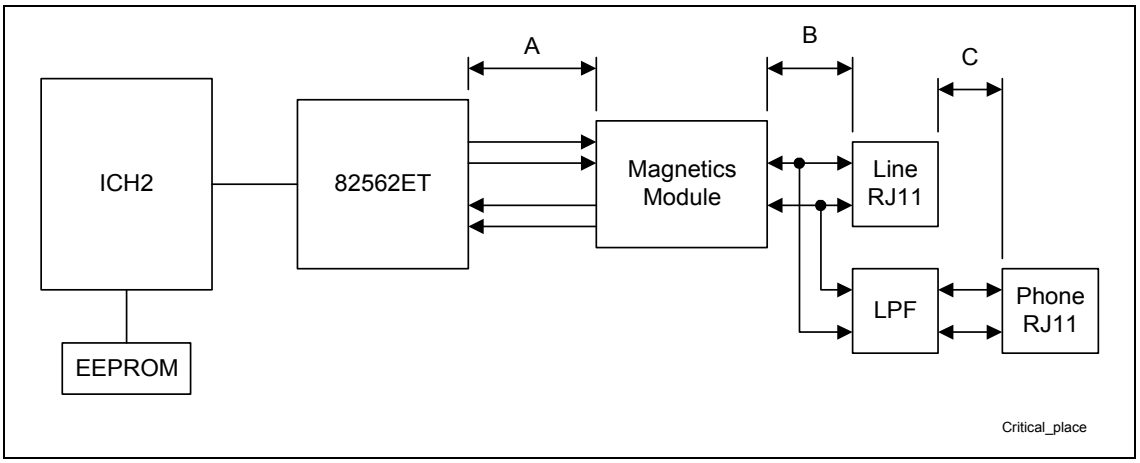
One RJ-11 jack (labeled “LINE” in the previous figure) allows the node to be connected to the Phoneline, and the second jack (labeled “PHONE” in the previous figure) allows other down-line devices to be connected at the same time. This second connector is not required by the HomePNA. However, typical PCI adapters and PC motherboard implementations are likely to include it for user convenience.

A low-pass filter, setup in-line with the second RJ-11 jack, also is recommended by the HomePNA to minimize interference between the HomeRun connection and a POTs voice or modem connection on the second jack. This restricts of the type of devices connected to the second jack as the pass-band of this filter is set approximately at 1.1 MHz. Refer to the HomePNA website (www.homepna.org) for up-to-date information and recommendations regarding the use of this low-pass filter to meet HomePNA certifications.

### 3.21.3.5. Critical Dimensions

There are three dimensions to consider during layout. Distance ‘B’ from the line RJ11 connector to the magnetics module, distance ‘C’ from the phone RJ11 to the LPF (if implemented), and distance ‘A’ from 82562EH to the magnetics module (see the following figure).

**Figure 52. Critical Dimensions for Component Placement**




| Distance | Priority | Guideline |
|---|---|---|
| B | 1 | < 1” |
| A | 2 | < 1” |
| C | 3 | < 1” |

#### Distance from Magnetics Module to Line RJ11

This distance ‘B’ should be given highest priority and should be less then 1”. Regarding trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequally long differential pairs contribute to common-mode noise. This can degrade receive circuit performance and contribute to emissions radiated from the transmit side.

### Distance from Intel® 82562EH to Magnetics Module

Due to the high speed of signals present, distance ‘A’ between the 82562EH and the magnetic should also be less than 1”, but should be second priority relative to distance from connects to the magnetic module.

Generally speaking, any section of trace intended for use with high-speed signals should be subject to proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between the device and trace route. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself.

### Distance from LPF to Phone RJ11

This distance ‘C’ should be less then 1”. Regarding trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequally long differential pairs contribute to common-mode noise. This can degrade the receive circuit performance and contribute to emissions radiated from the transmit side

## 3.21.4. Intel® 82562ET / 82562EM Guidelines

### Related Documents

- *82562ET Platform LAN Connect (PLC) Datasheet*
- *PCB Design for the 82562 ET/EM Platform LAN Connect*

For correct LAN performance, designers must follow the general guidelines outlined in Section 3.21.2. Additional guidelines for implementing a 82562ET or 82562EM LAN connect component are as follows.

### 3.21.4.1. Guidelines for Intel® 82562ET / 82562EM Component Placement

Component placement can affect the signal quality, emissions, and temperature of a board design. This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could result in failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

It is important to minimize the space needed for the Ethernet LAN interface, because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

### 3.21.4.2. Crystals and Oscillators

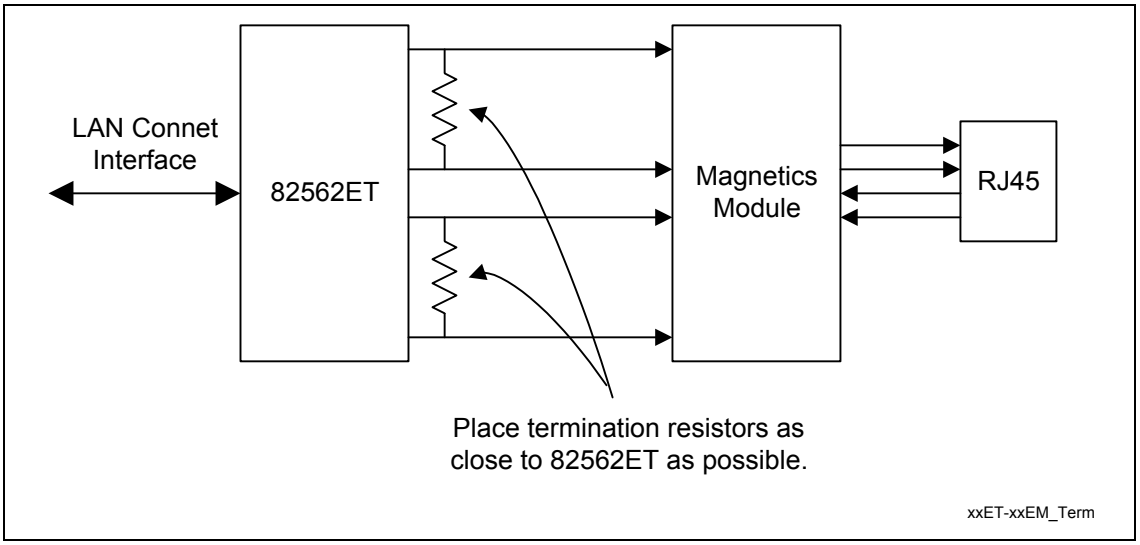
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference with communication. If they exist, the retaining straps of the crystal should be grounded to prevent possible radiation from the crystal case. Also, the crystal should lie flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise-free and stable operation, place the crystal and associated discrete components as close as possible to the 82562ET or 82562EM. Keep the trace length as short as possible and do not route any noisy signals in this area.

### 3.21.4.3. Intel® 82562ET / 82562EM Termination Resistors

The 100-Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 120-Ω (1%) receive differential pairs (RDP/RDN) should be placed as close as possible to the LAN connect component (82562ET or 82562EM). This is due to the fact that these resistors terminate the entire impedance seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

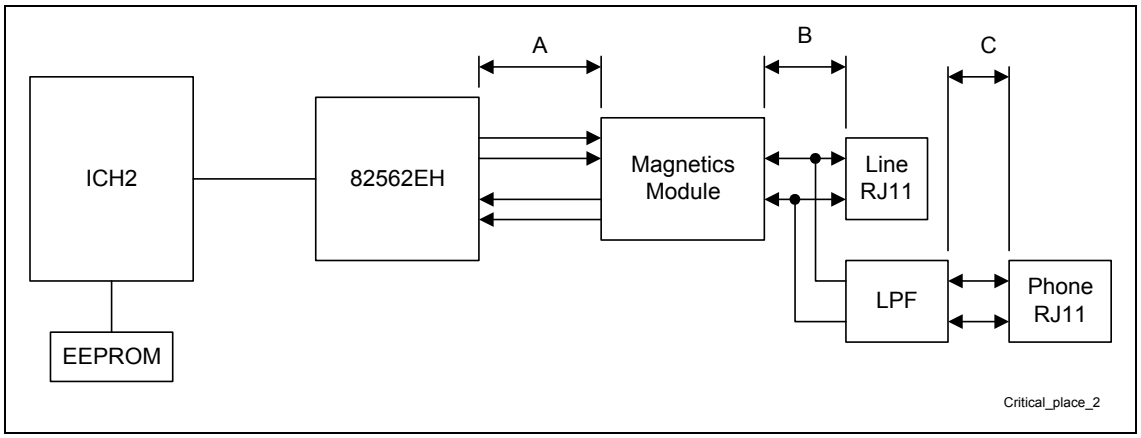
**Figure 53. Intel® 82562ET/82562EM Termination**



### 3.21.4.4. Critical Dimensions

There are two dimensions to consider during layout. Distance ‘B’ from the line RJ45 connector to the magnetics module and distance ‘A’ from the 82562ET or 82562EM to the magnetics module (see the following figure).

**Figure 54. Critical Dimensions for Component Placement**




| Distance | Priority | Guideline |
|---|---|---|
| A | 1 | < 1” |
| B | 2 | < 1” |

#### Distance from Magnetics Module to RJ45

The distance A in the previous figure should be given the highest priority in board layout. The separation between the magnetic module and the RJ45 connector should be kept less than 1”. The following trace characteristics are important and should be observed:

- Differential impedance: The differential impedance should be 100 Ω. The single-ended trace impedance will be approximately 50 Ω. However, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (e.g., TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (e.g., width).

***Caution:*** Asymmetric and unequal length traces in the differential pairs contribute to common-mode noise. This can degrade the receive circuit’s performance and contribute to emissions radiated from the transmit circuit. If the 82562ET must be placed farther than a couple of inches from the RJ45 connector, distance B can be sacrificed. It should be a priority to keep the total distance between the 82562ET and RJ45 as short as possible.

***Note:*** The measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layouts accordingly. If the actual impedance is consistently low, a target of 105–110 Ω should compensate for second-order effects.

### Distance from Intel® 82562ET to Magnetics Module

Distance B should also be designed to be less than 1” between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces intended for use with high-speed signals should be subject to proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that contributes more EMI than the original signal itself. For this reason, these traces should be designed to a 100-Ω differential value. These traces should also be symmetric and of equal length within each differential pair.

## 3.21.4.5. Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both backplanes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems, such as analog-to-digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane. Similarly, every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds so as to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Because signals with fast rise and fall times contain many high-frequency harmonics, they can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

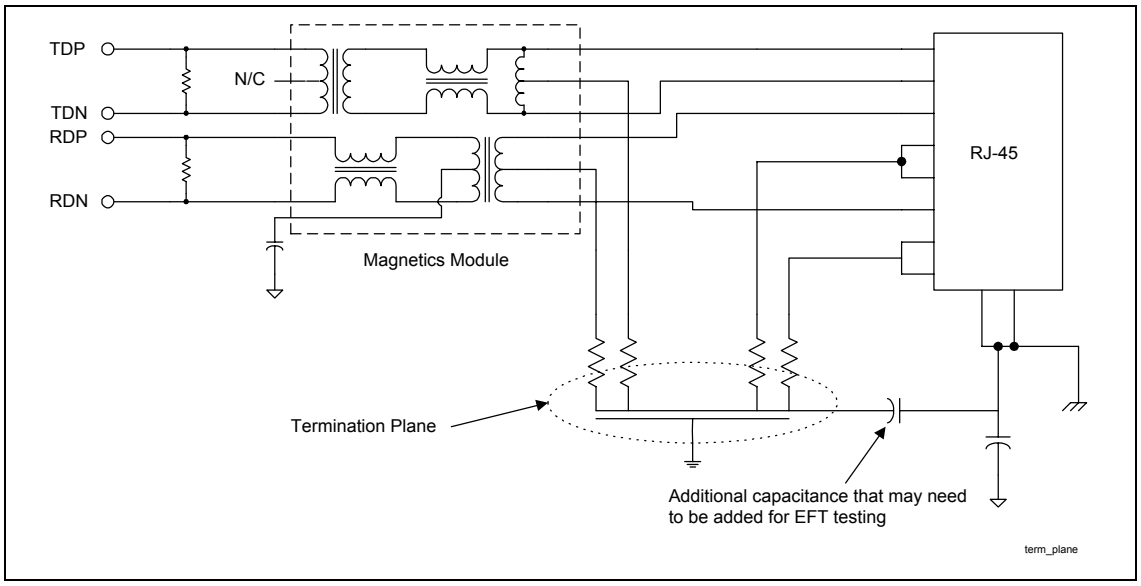
### Terminating Unused Connections

In Ethernet designs, it is common practice to terminate to ground both unused connections on the RJ45 connector and the magnetics module. Depending on the overall shielding and grounding design, this may be done to the chassis ground, signal ground or a termination plane. Care must be taken when using various grounding methods to ensure that emission requirements are met. The method most often implemented is called the “Bob Smith” termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75-Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

### Termination Plane Capacitance

The recommended minimum termination plane capacitance is 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (electrical fast transient) testing. If a discrete capacitor is used, it should be rated for at least 1000 Vac, to satisfy the EFT requirements.

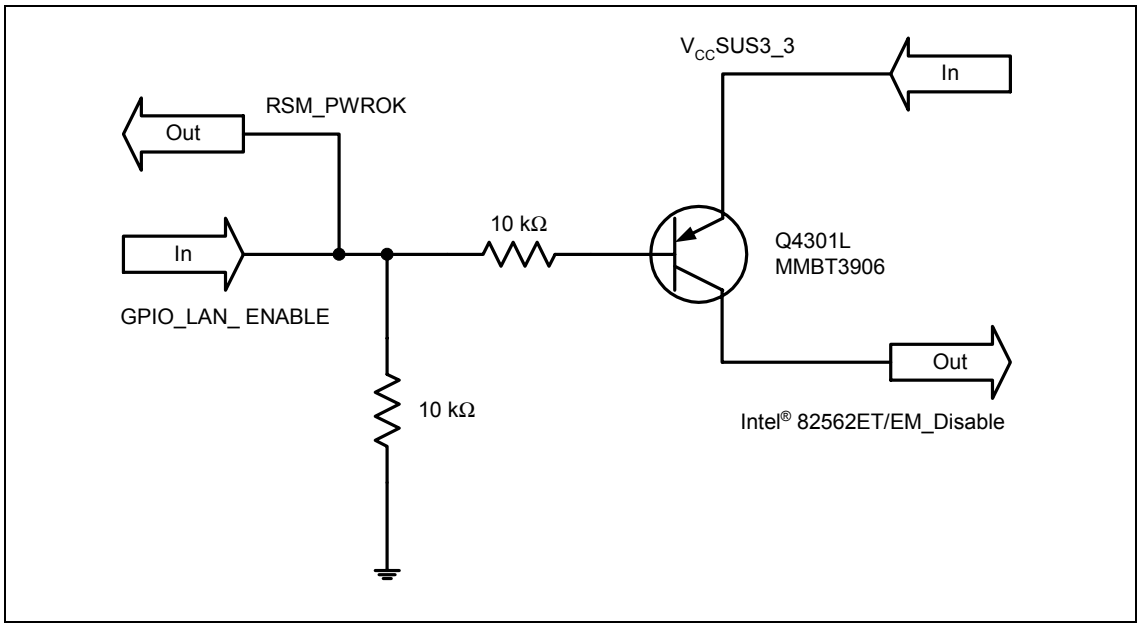
**Figure 55. Termination Plane**




## 3.21.4.6. Intel® 82562ET/EM Disable Guidelines

To disable the 82562ET/EM (82562ET/EM), the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. The BIOS, by controlling the GPIO, can disable the LAN microcontroller.

**Figure 56. Intel® 82562ET/EM Disable Circuit**



There are four pins which are used to put the 82562ET/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. The table below describes the operational/disable features for this design.

| Test_En | Isol_Tck | Isol_Ti | Isol_Tex | State |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Enabled |
| 0 | 1 | 1 | 1 | Disabled w/ Clock (low power) |
| 1 | 1 | 1 | 1 | Disabled w/out Clock (lowest power) |

The four control signals shown in the above table should be configured as follows: Test_En should be pulled-down through a 100 Ω resistor. The remaining 3 control signals should each be connected through 100 Ω series resistors to the common node “82562ET/EM_Disable” of the disable circuit.

## 3.21.5. Intel® 82562ET / 82562EH Dual Footprint Guidelines

These guidelines characterize the proper layout for a dual-footprint solution. This configuration enables the developer to install either the 82562EH or the 82562ET/82562EM components, while using only one motherboard design. The following guidelines are for the 82562ET/82562EH dual-footprint option. The guidelines called out in Sections 3.21.1 through 3.21.4 apply to this configuration. The dual footprint for this particular solution uses a SSOP footprint for 82562ET and a TQFP footprint for 82562EH. The combined footprint for this configuration is shown in the following two figures.

**Figure 57. Dual-Footprint LAN Connect Interface**

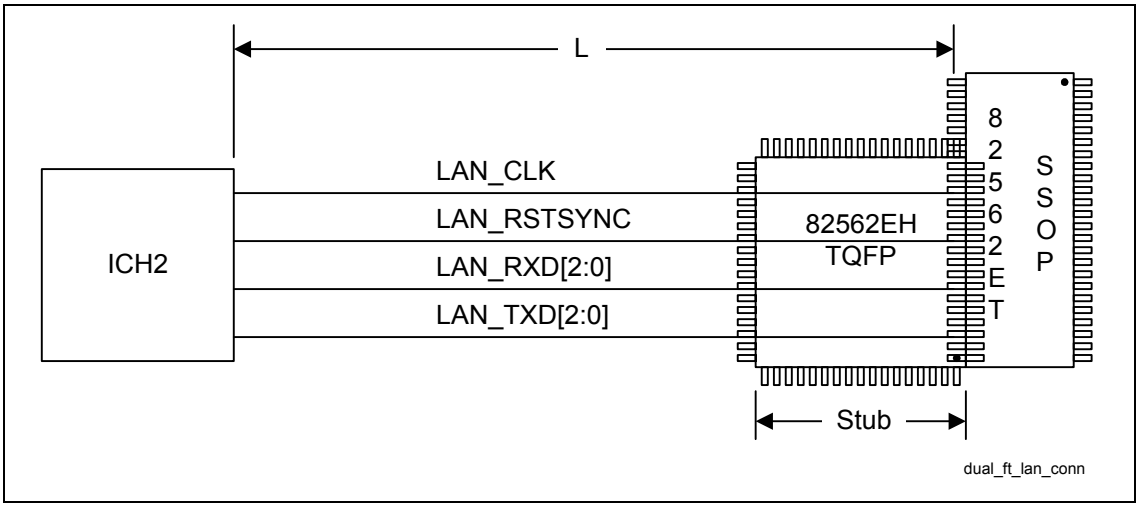
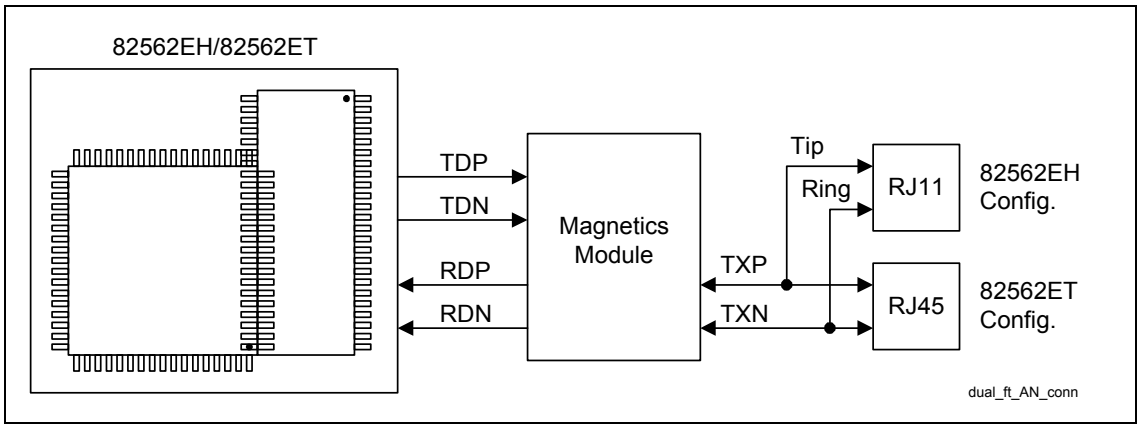


**Figure 58. Dual-Footprint Analog Interface**




The following are additional guidelines for this configuration:

- L = 3.5” to 10.0”
- Stub < 0.5”
- Either 82562EH or 82562ET/82562EM can be installed, but not both.
- 82562ET pins 28, 29, and 30 overlap with 82562EH pins 17, 18, and 19.
- Overlapping pins are tied to ground.
- No other signal pads should overlap or touch.
- Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], LAN_TXD[0], RDP, RDN, RXP/Ring, and RXN/Tip are shared by the 82562EH and 82562ET configurations.
- No stubs should be present when 82562ET is installed.
- Packages used for the dual footprint are TQFP for 82562EH and SSOP for 82562ET.
- A 22-Ω resistor can be placed at the driving side of the signal line to improve signal quality on the LAN connect interface.
- Resistor should be placed as close as possible to the component.
- Use components that can satisfy both the 82562ET and 82562EH configurations (i.e., magnetics module).
- Install components for either the 82562ET or the 82562EH configuration. Only one configuration can be installed at a time.
- Route shared signal lines such that stubs are not present or are kept to a minimum.
- Stubs may occur on shared signal lines (i.e., RDP and RDN). These stubs are due to traces routed to an uninstalled component.
- Use 0-Ω resistors to connect and disconnect circuitry not shared by both configurations. Place resistor pads along the signal line to reduce stub lengths.

# 3.22. LPC/FWH

The following provides general guidelines for compatibility and design recommendations for supporting the FWH flash BIOS device. The majority of the changes will be incorporated in the BIOS.

## 3.22.1. In-Circuit FWH Programming

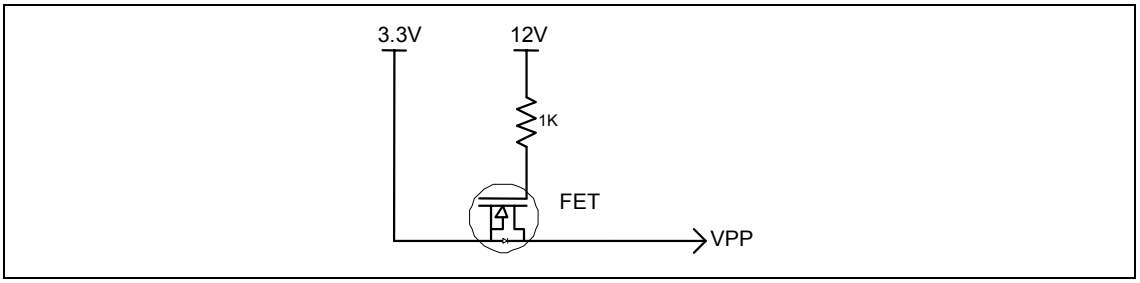
All cycles destined for the FWH will appear on the PCI. The ICH2 hub interface-to-PCI Bridge puts all processor boot cycles out on the PCI (before sending them out on the FWH interface). If the ICH2 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on PCI. This enables booting from a PCI card that positively decodes these memory cycles. To boot from a PCI card, it is necessary to keep the ICH2 in the subtractive decode mode. If a PCI boot card is inserted and the ICH2 is programmed for positive decode, two devices will positively decode the same cycle. In systems with the 82380AB (ISA bridge), it is also necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot from a ROM behind the 82380AB. Once you have booted from the PCI card, you potentially could program the FWH in circuit and program the ICH2 CMOS.

## 3.22.2. FWH Vpp Design Guidelines

The Vpp pin on the FWH is used for programming the flash cells. The FWH supports a Vpp of 3.3 V or 12 V. If Vpp is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12 Vpp for 80 hours. The 12 Vpp would be useful in a programmer environment that is typically an event that occurs very infrequently (much less than 80 hours). The VPP pin MUST be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the $V_{PP}$ pin. The following circuit will allow testers to put 12 V on the $V_{PP}$ pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

**Figure 59. FWH VPP Isolation Circuitry**



# 3.23. FWH Decoupling

A 0.1 µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the Vcc supply pins and the Vss ground pin to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the Vcc supply pins.

# 3.24. Processor PLL Filter Recommendation

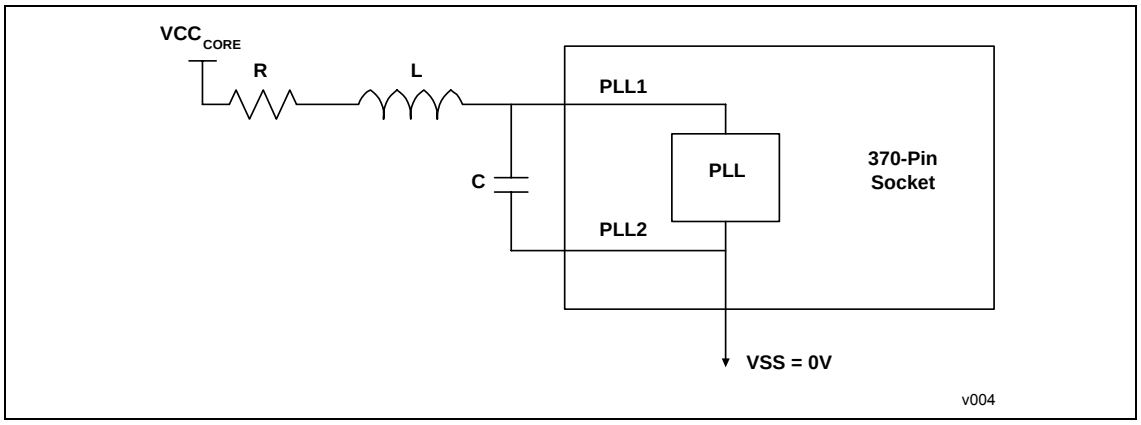
## 3.24.1. Processor PLL Filter Recommendation

All Celeron processors have internal PLL clock generators that are analog and require quiet power supplies to minimize jitter.

## 3.24.2. Topology

The general desired topology is shown in the following figure. Not shown are parasitic routing and local decoupling capacitors. Excluded from the external circuitry are parasitics associated with each component.

**Figure 60. Filter Topology**




## 3.24.3. Filter Specification

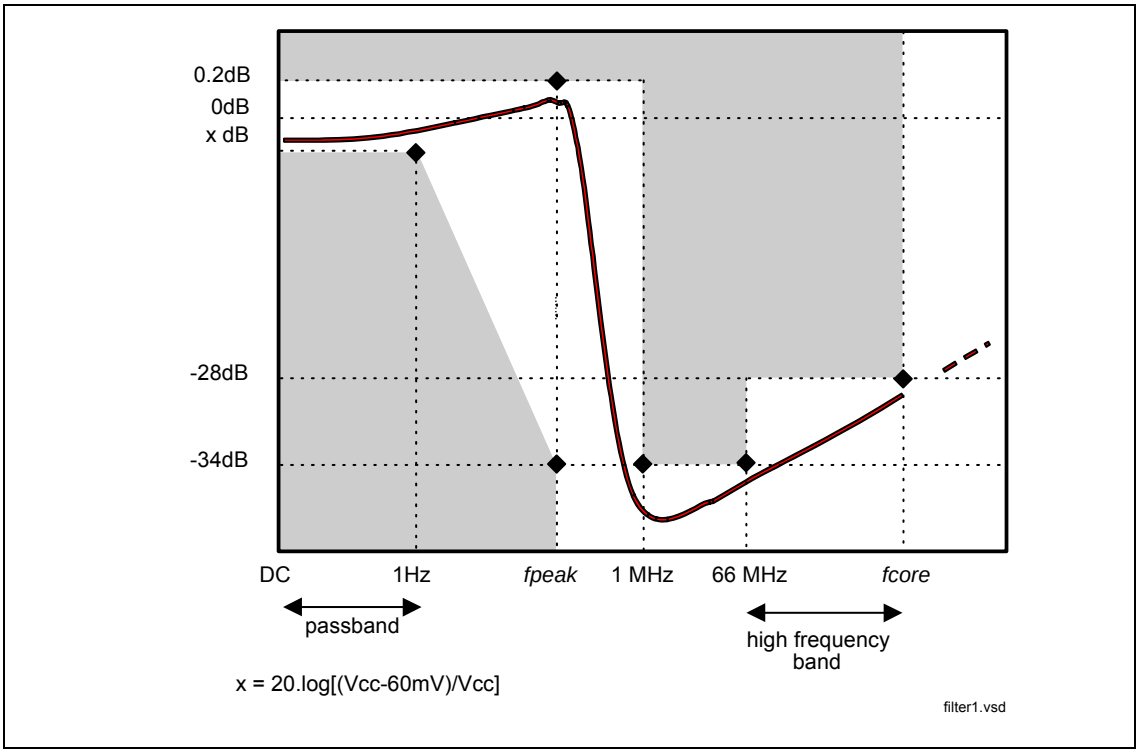
The function of the filter is to protect the PLL from external noise through low-pass attenuation. In general, the low-pass description forms an adequate description for the filter.

The low-pass specification, with input at $VCC_{CORE}$ and output measured across the capacitor, is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter specification is graphically shown in the following figure.

**Figure 61. Filter Specification**




**NOTES:**
1. Diagram not to scale.
2. No specification for frequencies beyond fcore.
3. fpeak, if it exists, should be less than 0.05 MHz.

Other requirements:

- Filter should support DC current > 30 mA.
- Shielded type inductor to minimize magnetic pickup.
- DC voltage drop from VCC to PLL1 should be < 60mV, which in practice implies series R < 2 Ω; also means pass band (from DC to 1Hz) attenuation < 0.5dB for VCC = 1.1V, and < 0.35dB for VCC = 1.5V.

## 3.24.4. Recommendation for Intel® Platforms

The following tables are examples of components that meet Intel's recommendations, when configured in the topology presented in Figure 60.

### Table 25. Inductor

| Part Number | Value | Tol | SRF | Rated I | DCR |
|---|---|---|---|---|---|
| TDK MLF2012A4R7KT | 4.7 µH | 10% | 35 MHz | 30 mA | 0.56 Ω (1 W max) |
| Murata LQG21N4R7K00T1 | 4.7 µH | 10% | 47 MHz | 30 mA | 0.7 Ω (±50%) |
| Murata LQG21C4R7N00 | 4.7 µH | 30% | 35 MHz | 30 mA | 0.3 Ω max |

### Table 26. Capacitor

| Part Number | Value | Tolerance | ESL | ESR |
|---|---|---|---|---|
| Kemet T495D336M016AS | 33 µF | 20% | 2.5 nH | 0.225 Ω |
| AVX TPSD336M020S0200 | 33 µF | 20% | 2.5 nH | 0.2 Ω |

### Table 27. Resistor

| Value | Tolerance | Power | Note |
|---|---|---|---|
| 1 Ω | 10% | 1/16W | Resistor may be implemented with trace resistance in which discrete R is not needed |

To satisfy damping requirements, total series resistance in the filter (from $VCC_{CORE}$ to the top plate of the capacitor) must be at least 0.35 Ω. This resistor can be in the form of a discrete component, or routing, or both. For example, if the picked inductor has a minimum DCR of 0.25 Ω, then a routing resistance of at least 0.10 Ω is required. Be careful not to exceed the maximum resistance rule (2 Ω). For example, if using discrete R1, the maximum DCR of the L should be less than 2.0 - 1.1 = 0.9 Ω, which precludes using some inductors.

Other routing requirements:

- C should be close to PLL1 and PLL2 pins, < 0.1 Ω per route. These routes do not count towards the minimum damping R requirement.
- PLL2 route should be parallel and next to PLL1 route (minimize loop area).
- L should be close to C; any routing resistance should be inserted between $VCC_{CORE}$ and L.
- Any discrete R should be inserted between $VCC_{CORE}$ and L.

**Figure 62. Using Discrete R**

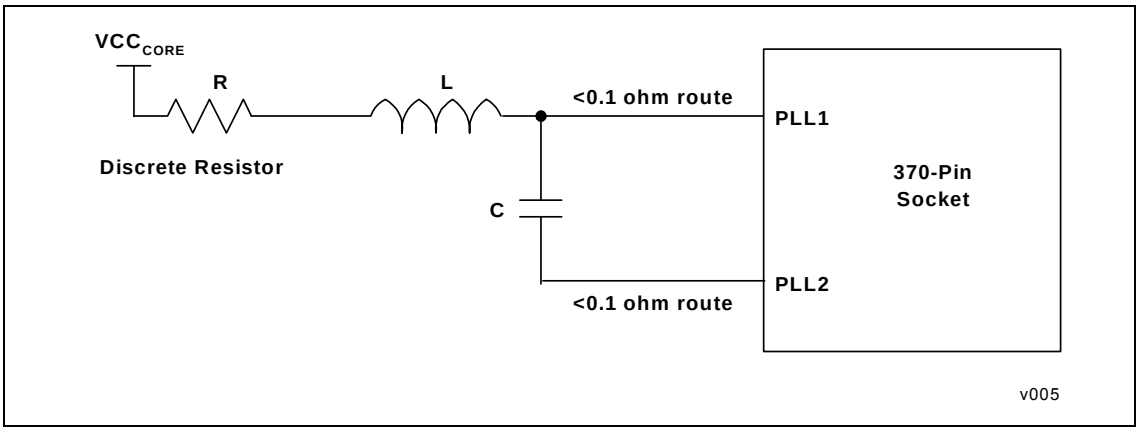
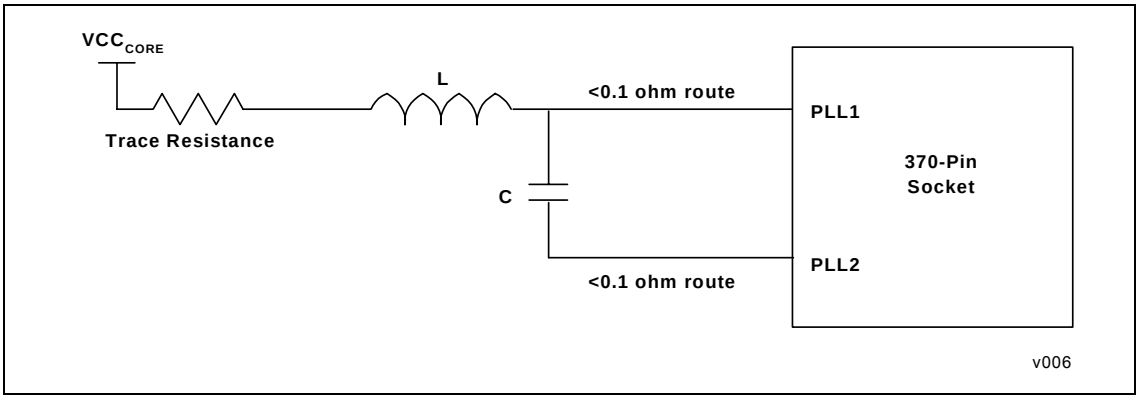


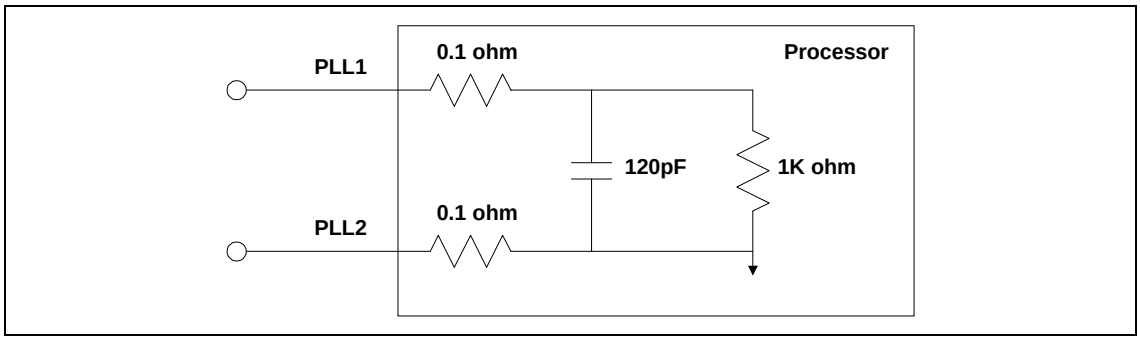

**Figure 63. No Discrete R**



## 3.24.5. Custom Solutions

As long as filter performance as specified in the previous “Filter Specification” figure and other requirements outlined in Section 3.24.1. are satisfied, other solutions are acceptable. Custom solutions should be simulated against a standard reference core model, which is shown in the figure below.

**Figure 64. Core Reference Model**




**NOTES:**

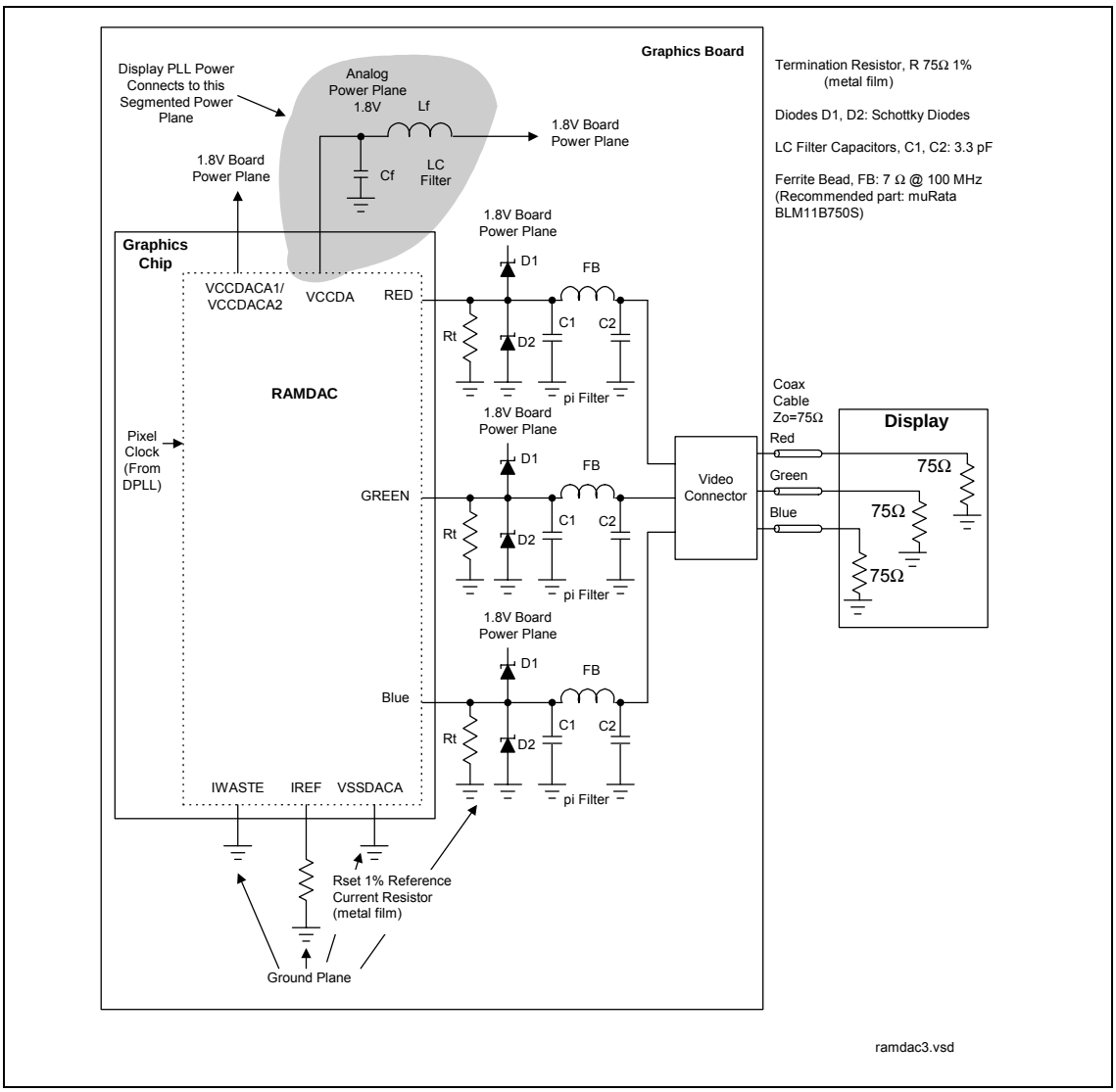
1. 0.1 Ω resistors represent package routing1.
2. 120 pF capacitor represents internal decoupling capacitor.
3. 1 kΩ resistor represents small signal PLL resistance.
4. Be sure to include all component and routing parasitics.
5. Please sweep across component/parasitic tolerances.
6. To observe IR drop, use DC current of 30 mA and minimum $VCC_{CORE}$ level.

1 For other modules (interposer, DMM, etc), adjust routing resistor if desired, but use minimum numbers.

# 3.25. RAMDAC/Display Interface

The following figure shows the interface of the RAMDAC analog current outputs with the display. Each DAC output is doubly-terminated with a 75-Ω resistance; one 75-Ω resistance from the DAC output to the board ground and the other termination resistance exists within the display. The equivalent DC resistance at the output of each DAC output is 37.5 Ω. The output current of each DAC flows into this equivalent resistive load to produce a video voltage without the need for external buffering. There is also an LC pi-filter that is used to reduce high-frequency glitches and noise, and reduce EMI. To maximize the performance, the filter impedance, cable impedance, and load impedance should be the same. The LC pi-filter consists of two 3.3 pF capacitors and a Ferrite bead with a 75-Ω impedance at 100 MHz. The LC pi-filter is designed to filter glitches produced by the RAMDAC while maintaining adequate edge rates to support high-end display resolutions.

**Figure 65. Schematic of RAMDAC Video Interface**




**NOTES:** Diodes $D_1$, $D_2$ are clamping diodes and may not be necessary to populate.

In addition to the termination resistance and LC pi-filter, there are protection diodes connected to the RAMDAC outputs to help prevent latch-up. The protection diodes must be connected to the same power supply rails as the RAMDAC. An LC filter is recommended to connect the segmented analog 1.8V power plane of the RAMDAC to the 1.8V board power plane. The LC filter is recommended to be designed for a cut-off frequency of 100 kHz.

## 3.25.1. Reference Resistor (Rset) Calculation

The full-swing video output is designed to be 0.7V according to the VESA video standard. With an equivalent DC resistance of 37.5 Ω (two 75 Ω in parallel - one 75 Ω termination on the board and one 75 Ω termination within the display), the full-scale output current of a RAMDAC channel is 0.7/37.5 Ω = 18.67 mA. Since the RAMDAC is an 8-bit current-steering DAC, this full-scale current is equivalent 255I, where I is a unit of current. Therefore, the unit current or LSB current of the DAC signals equals 73.2 µA. The reference circuitry generates a voltage across this $R_{set}$ resistor equal to a bandgap voltage divided-by-three (409 mV). The RAMDAC reference current generation circuitry is designed to generate a 32I reference current using the reference voltage and the $R_{set}$ value. To generate a 32I reference current for the RAMDAC, the reference current setting resistor, $R_{set}$, is calculated from the following equation:

$$R_{set} = V_{REF}/32I = 0.409V/32*73.2\mu A = 174\ \Omega$$

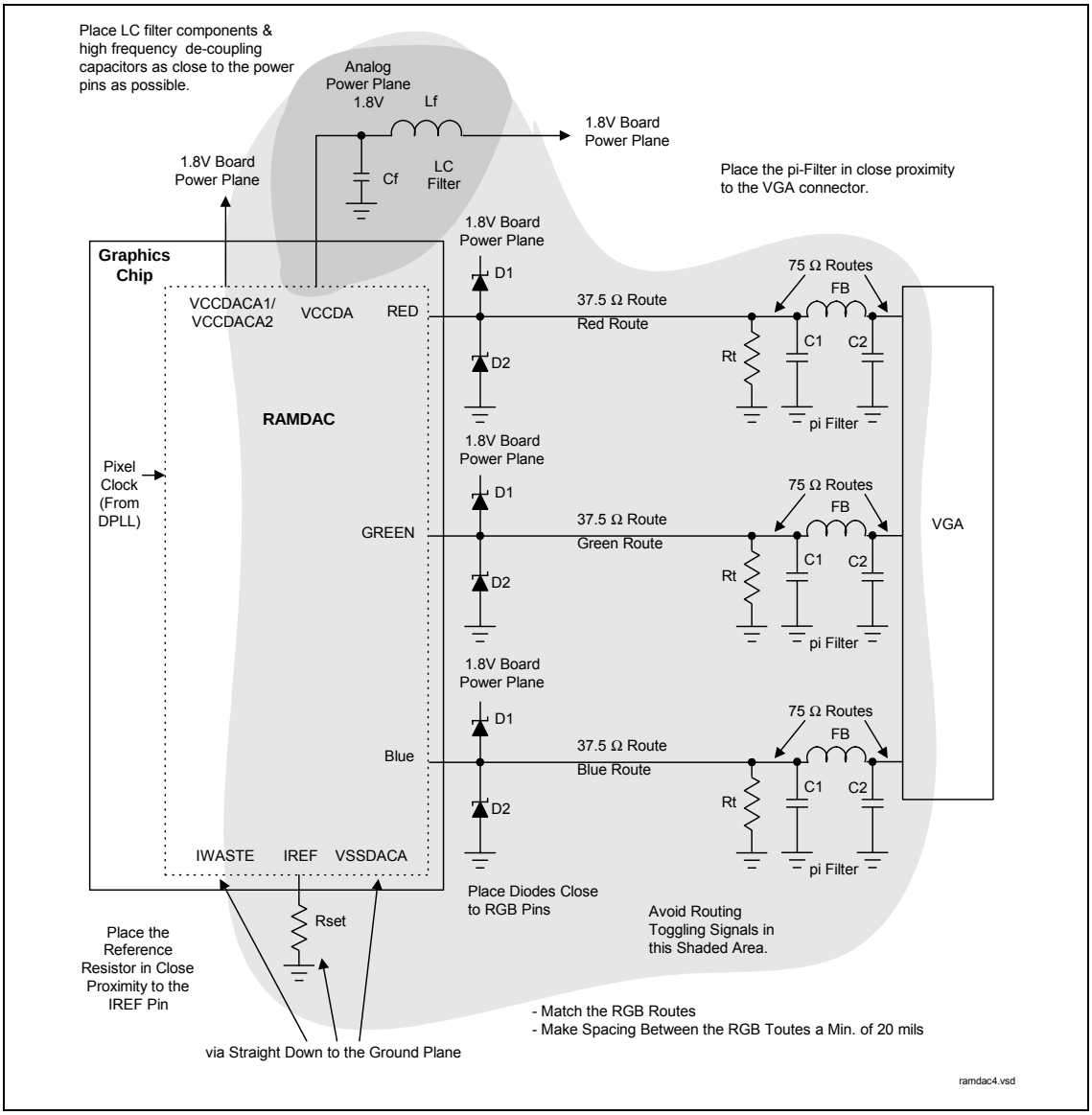
## 3.25.2. RAMDAC Board Design Guidelines

The RAMDAC layout is shown in the following three figures. An RLC network should be used between the board power plane and the board ground plane. The recommended RAMDAC routing for a four layer board is such that the red, green and blue video outputs be routed on the top (bottom) layer over (under) a solid ground plane to maximize noise rejection characteristics of the video outputs. It is essential to avoid toggling signals from being routed next to the video output signals to the VGA connector. A 20 mil spacing between any video route and any other routes is recommended.

Matching of the video routes (red, green, and blue) from the RAMDAC to the VGA connector is also essential. The routing for these signals should be as similar as possible (i.e., same routing layer(s), same number of vias, same routing length, same bends and jogs).

The following figure shows recommended RAMDAC component placement and routing. The termination resistance can be placed anywhere along the video route from the RAMDAC output to the VGA connector as long as the impedance of the traces are designed as indicated in the following figure. The pi- filters are recommended to be placed in close proximity to the VGA connector to maximize EMI filtering effectiveness. The LC filter components for the RAMDAC/PLL power plane, de-coupling capacitors, latch-up protection diodes, and the reference resistor are recommended to be placed in close proximity to the respective pins.

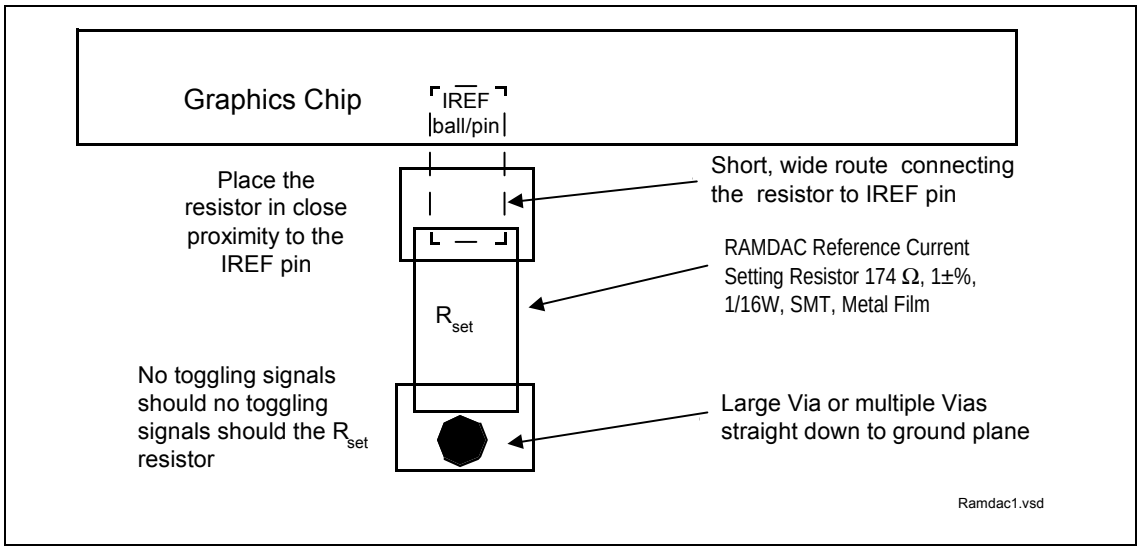
## Figure 66. RAMDAC Component and Routing Guidelines




**NOTES:** Diodes $D_1$, $D_2$ are clamping diodes and may not be necessary to populate.

The following figure shows the recommended reference resistor placement and connections.

**Figure 67. Recommended RAMDAC Reference Resistor Placement and Connections**



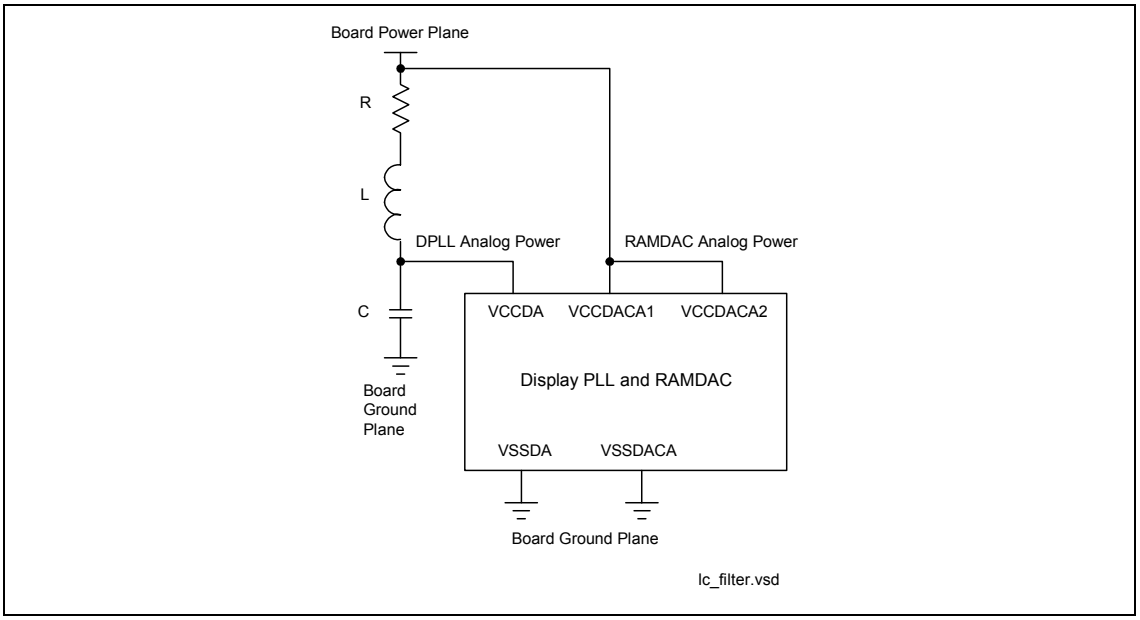

## 3.26. DPLL Filter Design Guidelines

The 810E2 chipset contains sensitive phase-locked loop circuitry, the DPLL, that can cause excessive dot clock jitter. Excessive jitter on the dot clock may result in a “jittery” image. An LC filter network connected to the DPLL analog power supply is recommended to reduce dot clock jitter.

The DPLL bandwidth varies with the resolution of the display and can be as low as 100 kHz. In addition, the DPLL jitter transfer function can exhibit jitter peaking effects in the range from 100 kHz to a few megahertz. A low-pass LC filter is recommended for the display PLL analog power supply designed to attenuate power supply noise with frequency content from 100 kHz and above so that jitter amplification is minimized.

The following figure is a block diagram showing the recommended topology of the filter connection (parasitics not shown). The display PLL analog power rail (VCCDA) is connected to the board power plane through an LC filter. The RAMDAC analog power rails (VCCDACA1 and VCCDACA2) are connected directly to the 1.8V board power plane.

**Figure 68. Recommended LC Filter Connection**




The resistance from the inductor to the board 1.8V power plane represents the total resistance from the board power plane to the filter capacitor. This resistance, which can be a physical resistor, routing/via resistance, parasitic resistance of the inductor or combinations of these, acts as a damping resistance for the filter and effects the response of the filter.

The LC filter topology shown in the above figure is the preferred choice since the RAMDAC minimum voltage level requirement does not place constraints on the LC filter for the DPLL. The maximum current flowing into the DPLL analog power is approximately 30 mA, much less than that of the RAMDAC, and therefore, a filter inductor with a higher DC resistance can be tolerated. With the topology in the above figure, the filter inductor DC current rating must be at least 30 mA and the maximum IR drop from the board power plane to the VCCDA ball should be 100 mV or less (corresponds to a series resistance equal to or less than 3.3 Ω. This larger dc resistance tolerance improves the damping and the filter response.

## 3.26.1. Filter Specification

The low-pass filter specification with the input being the board power plane and the output measured across the filter capacitor is defined as follows for the filter topology shown in the above figure.

- pass band gain < 0.2 dB
- DC IR drop from board power plane to the DPLL VCCDA ball < 100 mV (and a maximum DC resistance < 3.3 Ω)
- filter should support a DC current > 30 mA
- minimum attenuation from 100 kHz to 10 MHz = 10 dB (desired attenuation > 20 dB)
- a magnetically shielded inductor is recommended

The resistance from the board power plane to the filter capacitor node should be designed to meet the filter specifications outlined above. This resistance acts as a damping resistance for the filter and affects

the filter characteristics. This resistance includes the routing resistance from the board power plane connection to the filter inductor, the filter inductor parasitic resistance, the routing from the filter inductor to the filter capacitor, and resistance of the associated vias. Part of this resistance can be a physical resistor. A physical resistor may not be needed depending on the resistance of the inductor and the routing/via resistance.

The filter capacitance should be chosen with as low of an ESR (equivalent series resistance) and ESL (equivalent series inductance) as possible to achieve the best filter performance. The parasitics of the filter capacitor can alter the characteristics of the filter significantly and even cause the filter to be ineffective at the frequencies of interest. The LC filter must be simulated with all the parasitics of the inductor, capacitor, and associated routing parasitics along with tolerances.

## 3.26.2. Recommended Routing/Component Placement

- The filter capacitance should be placed as close to the VCCDA ball as possible so that the routing resistance from the filter capacitor lead to the package VCCDA ball is < 0.1 Ω.
- The VSSDA ball should via straight down to the board ground plane.
- The filter inductor should be placed in close proximity to the filter capacitor and any routing resistance should be inserted between the board power plane connection and the filter inductor.
- If a discrete resistor is used for the LC filter, the resistor should be placed between the board power plane connection and the filter inductor.

## 3.26.3. Example LC Filter Components

The following two tables show example LC components and resistance for the LC filter topology shown in the “Recommended LC Filter Connection” figure.

**Table 28. DPLL LC Filter Component Example**

| Component | Manufacturer | Part No. | Description |
|---|---|---|---|
| Capacitor | KEMET | T495D336MD16AS | 33 µF ±20%, 16VDC,<br>ESR=0.225 Ω @ 100 kHz, ESL=2.5 nH |
| Inductor | muRATA | LQG11A68NJ00 | 68 nH ±5%, 300 mA,<br>Max dc resistance = 0.8 Ω, size=0603 |
| Resistance | | | < 3.3 Ω |

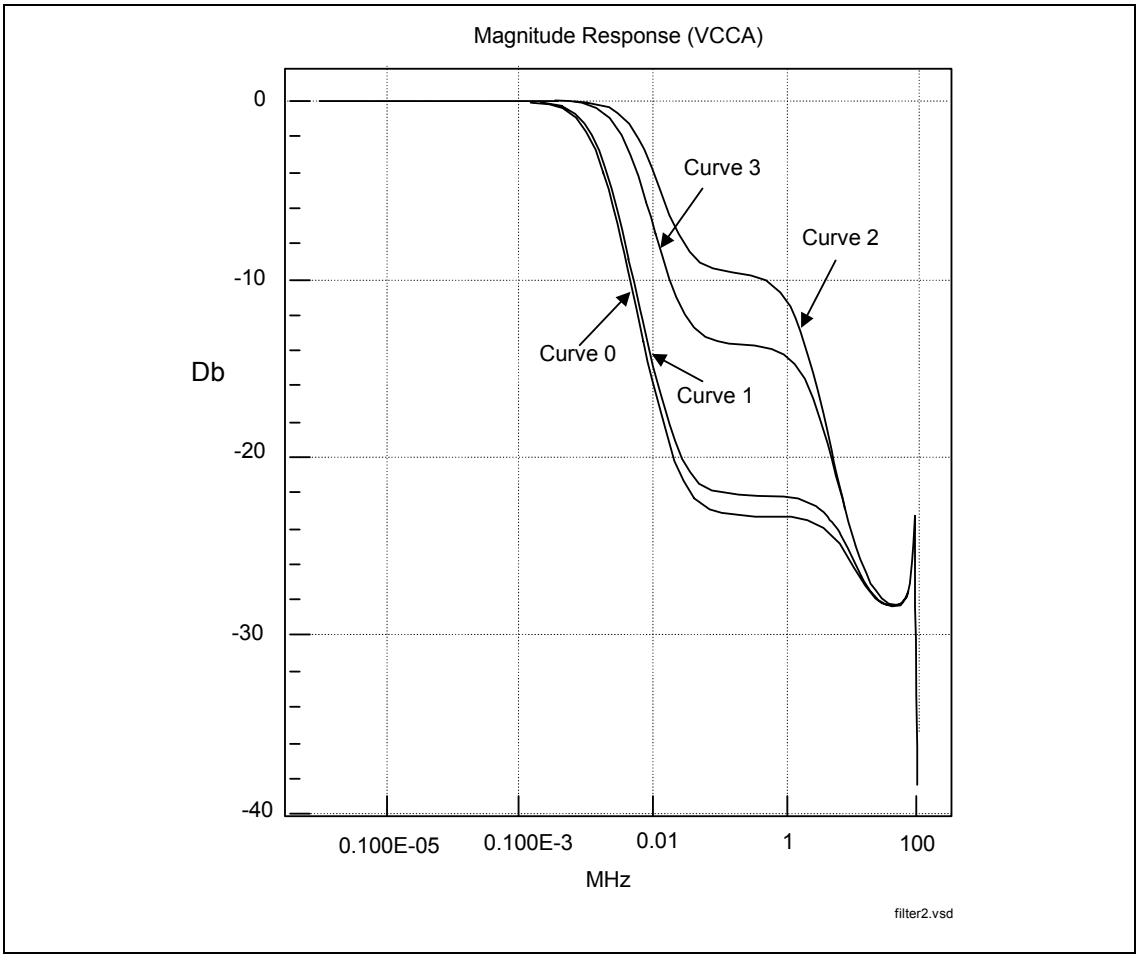
The resistance of the filter is defined as the total resistance from the board power plane to the filter inductor. If a discrete resistor is used as part of this resistance, the tolerance and temperature coefficient should be accounted for so that the maximum DC resistance in this path from the board power plane connection to the DPLL VCCDA ball is less than 3.3 Ω to meet the IR drop requirement.

### Table 29. Additional DPLL LC Filter Component Example

| Component | Manufacturer | Part No. | Description |
|---|---|---|---|
| Capacitor | KEMET | T495D336MD16AS | 33 µF ±20%, 16VDC,<br>ESR=0.225 Ω @ 100 kHz,<br>ESL=2.5 nH |
| Inductor | muRATA | LQG21NR10K10 | 100 nH ±10%, 250 mA,<br>Max dc resistance = 0.26 Ω,<br>size=0805,<br>magnetically shielded |

As an example, is a Bode plot showing the frequency response using the capacitor and inductor values shown in Table 30. The capacitor and inductor values were held constant while the resistance was swept for four different combinations of resistance (the resistance of the discrete/trace resistor and the resistance of the inductor), each resulting in a different series resistance. In addition, different values for the resistance of the inductor were assumed based on its max and typical DC resistance. This is summarized in Table 30. This yielded the four different frequency response curves shown in.

### Figure 69. Frequency Response (see Table 30)



### Table 30. Resistance Values for Frequency Response Curves

| Curve | RTRACE + RDISCRETE | RIND |
|---|---|---|
| 0 | 2.2 Ω | 0.8 Ω |
| 1 | 2.2 Ω | 0.4 Ω |
| 2 | 0 Ω | 0.4 Ω |
| 3 | 0 Ω | 0.8 Ω |

As series resistance ($R_{TRACE}$ + $R_{DISCRETE}$ + $R_{IND}$) increases, the filter response (i.e., attenuation in PLL bandwidth) improves. There is a limit of 3.3 Ω total series resistance of the filter to limit DC voltage drop.

# 4. Advanced System Bus Design

This chapter discusses more detail about the methodology used to develop the guidelines. Section 4.1 specific system guidelines. This is a step-by-step methodology that Intel has successfully used to design high performance desktop systems. Section 4.2 introduces the theories that are applicable to this layout guideline. Section 4.3 contains more details and insights. The items in Section 4.3 expand on some of the rationale for the recommendations in the step-by-step methodology. This section also includes equations that may be used for reference.

## 4.1. AGTL+ Design Guidelines

The following step-by-step guideline was developed for systems based on two processor loads and one Intel 82810E GMCH load. Systems using custom chipsets will require timing analysis and analog simulations specific to those components.

The guideline recommended in this section is based on experience developed at Intel while developing many different Intel® Pentium® Pro processor family and Pentium II processor- based systems. Begin with an initial timing analysis and topology definition. Perform pre-layout analog simulations for a detailed picture of a working “solution space” for the design. These pre-layout simulations help define routing rules prior to placement and routing. After routing, extract the interconnect database and perform post-layout simulations to refine the timing and signal integrity analysis. Validate the analog simulations when actual systems become available. The validation section describes a method for determining the flight time in the actual system.

Guideline Methodology:

- Initial Timing Analysis
- Determine General Topology, Layout, and Routing
- Pre-Layout Simulation
  - Sensitivity sweep
  - Monte Carlo Analysis
- Place and Route Board
  - Estimate Component to Component Spacing for AGTL+ Signals
  - Layout and Route Board
- Post-Layout Simulation
  - Interconnect Extraction
  - Inter-Symbol Interference (ISI), Crosstalk, and Monte Carlo Analysis
- Validation
  - Measurements
  - Determining Flight Time

## 4.1.1. Initial Timing Analysis

Perform an initial timing analysis of the system using the Setup Time and Hold Time equations shown below. These equations are the basis for timing analysis. To complete the initial timing analysis, values for clock skew and clock jitter are needed, along with the component specifications. These equations contain a multi-bit adjustment factor, $M_{ADJ}$, to account for multi-bit switching effects such as SSO push out or pull-in that are often hard to simulate. These equations **do not** take into consideration all signal integrity factors that affect timing. Additional timing margin should be budgeted to allow for these sources of noise.

### Setup Time

$$T_{CO\_MAX} + T_{SU\_MIN} + CLK_{SKEW} + CLK_{JITTER} + T_{FLT\_MAX} + M_{ADJ} \leq \text{Clock Period}$$

### Hold Time

$$T_{CO\_MIN} + T_{FLT\_MIN} - M_{ADJ} \geq T_{HOLD} + CLK_{SKEW}$$

Symbols used in Setup Time and Hold Time equations above:

- $T_{CO\_MAX}$ is the maximum clock to output specification[1].
- $T_{SU\_MIN}$ is the minimum required time specified to setup before the clock[1].
- $CLK_{JITTER}$ is the maximum clock edge-to-edge variation.
- $CLK_{SKEW}$ is the maximum variation between components receiving the same clock edge.
- $T_{FLT\_MAX}$ is the maximum flight time as defined in Chapter 1.
- $T_{FLT\_MIN}$ is the minimum flight time as defined in Chapter 1.
- $M_{ADJ}$ is the multi-bit adjustment factor to account for SSO pushout or pull-in.
- $T_{CO\_MIN}$ is the minimum clock to output specification[1].
- $T_{HOLD}$ is the minimum specified input hold time.

***Note:*** The Clock to Output ($T_{CO}$) and Setup to Clock ($T_{SU}$) timings are both measured from the signals last crossing of $V_{REF}$, with the requirement that the signal does not violate the ringback or edge rate limits. See the *Intel® Pentium® II Processor Developer's Manual* for more details.

Solving these equations for $T_{FLT}$ results in the following equations:

### Maximum Flight Time

$$T_{FLT\_MAX} \leq \text{Clock Period} - T_{CO\_MAX} - T_{SU\_MIN} - CLK_{SKEW} - CLK_{JITTER} - M_{ADJ}$$

### Minimum Flight Time

$$T_{FLT\_MIN} \geq T_{HOLD} + CLK_{SKEW} - T_{CO\_MIN} + M_{ADJ}$$

There are multiple cases to consider. Note that while the same trace connects two components, component A and component B, the minimum and maximum flight time requirements for component A driving component B as well as component B driving component A must be met. The cases to be considered are:

- Processor driving processor
- Processor driving chipset
- Chipset driving processor

A designer using components other than those listed above must evaluate additional combinations of driver and receiver.

**Table 31. AGTL+ Parameters for Example Calculations [1,2]**

| IC Parameters | Intel® Pentium® III processor core at 133 MHz Bus (ns) | Intel® 82810E GMCH (ns) | Notes |
|---|---|---|---|
| Clock to Output maximum ($T_{CO\_MAX}$) | 2.7 | 3.6 | 4 |
| Clock to Output minimum ($T_{CO\_MIN}$) | -0.1 | 0.5 | 4 |
| Setup time ($T_{SU\_MIN}$) | 1.2 | 2.27 | 3,4 |
| Hold time ($T_{HOLD}$) | 0.8 | 0.28 | 4 |

**NOTES:**
1. All times in nanoseconds.
2. **Numbers in table are for reference only.** These timing parameters are subject to change. Please check the appropriate component documentation for valid timing parameter values.
3. $T_{SU\_MIN}$ = 1.9 ns assumes the 82810E GMCH sees a minimum edge rate equal to 0.3 V/ns.
4. The Pentium III substrate nominal impedance is set to 65 Ω ±15%. Future Pentium III processor substrate may be set at 60 Ω ±15%

Table 31 lists the AGTL+ component timings of the processors and 82810E GMCH defined at the pins. These timings are for reference only.

Table 32 gives an example AGTL+ initial maximum flight time and Table 33 is an example minimum flight time calculation for a 133 MHz, 2-way Pentium III processor/Intel 810E2 chipset system bus. Note that assumed values for clock skew and clock jitter were used. Clock skew and clock jitter values are dependent on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.

Intel highly recommends adding margin as shown in the "$M_{ADJ}$" column to offset the degradation caused by SSO push-out and other multi-bit switching effects. The "Recommended $T_{FLT\_MAX}$" column contains the recommended maximum flight time after incorporating the $M_{ADJ}$ value. If edge rate, ringback, and monotonicity requirements are not met, flight time correction must first be performed as documented in the *Intel® Pentium® II Processor Developer's Manual* with the additional requirements noted in Section 4.1. The commonly used "textbook" equations used to calculate the expected signal propagation rate of a board are included in that section.

Simulation and control of baseboard design parameters can ensure that signal quality and maximum and minimum flight times are met. Baseboard propagation speed is highly dependent on transmission line geometry configuration (stripline vs. microstrip), dielectric constant, and loading. This layout guideline includes high-speed baseboard design practices that may improve the amount of timing and signal quality margin. The magnitude of $M_{ADJ}$ is highly dependent on baseboard design implementation (stackup, decoupling, layout, routing, reference planes, etc.) and needs to be characterized and budgeted appropriately for each design.

Table 32 and Table 33 are derived assuming:

- CLKSKEW = 0.2 ns (Note: Assumes clock driver pin-to-pin skew is reduced to 50 ps by tying two host clock outputs together ("ganging") at clock driver output pins, and the PCB clock routing skew is 150 ps. System timing budget must assume 0.175 ns of clock driver skew if outputs are not tied together and a clock driver that meets the CK98 clock driver specification is being used.)
- CLKJITTER = 0.250 ns

Some clock driver components may not support ganging the outputs together. Be sure to verify with your clock component vendor before ganging the outputs. See the appropriate Intel 810E chipset documentation and *CK98 Clock Synthesizer/Driver Specification* for details on clock skew and jitter specifications. Refer to the "Clocking" chapter for host clock routing details.

### Table 32. Example T Calculations for 133 MHz Bus[1]

| Driver | Receiver | Clk Period[2] | TCO_MAX | TSU_MIN | ClkSKEW | ClkJITTER | MADJ | Recommended TFLT_MAX[3] |
|---|---|---|---|---|---|---|---|---|
| Processor | Processor | 7.50 | 2.7 | 1.20 | 0.20 | 0.250 | 0.40 | 2.75 |
| Processor | 82810E GMCH | 7.50 | 2.7 | 2.27 | 0.20 | 0.250 | 0.40 | 1.68 |
| Intel® 82810E GMCH | Processor | 7.50 | 3.63 | 1.20 | 0.20 | 0.25 | 0.40 | 1.82 |

**NOTES:**

1. All times in nanoseconds.
2. BCLK period = 7.50 ns @ 133.33 MHz.
3. The flight times in this column include margin to account for the following phenomena that Intel has observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect flight time and signal quality and are sometimes not accounted for in simulation. Accordingly, maximum flight times depend on the baseboard design and additional adjustment factors or margins are recommended.
   - SSO push-out or pull-in.
   - Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay.
   - Crosstalk on the PCB and internal to the package can cause variation in the signals.

   There are additional effects that **may not** necessarily be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. Examples include:
   - The effective board propagation constant (SEFF ), which is a function of:
     - Dielectric constant (r ) of the PCB material.
     - The type of trace connecting the components (stripline or microstrip).
     - The length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time **but not necessarily equal to** the flight time.

### Table 33. Example TFLT_MIN Calculations (Frequency Independent)

| Driver | Receiver | THOLD | ClkSKEW | TCO_MIN | Recommended TFLT_MIN |
|---|---|---|---|---|---|
| Processor | Processor | 0.8 | 0.2 | -0.1 | 1.2 |
| Processor | 82810E GMCH | 0.28 | 0.2 | -0.1 | 0.58 |
| Intel® 82810E GMCH | Processor | 0.8 | 0.2 | 0.5 | 0.5 |

**NOTE:** All times in nanoseconds.

## 4.1.2. Determine General Topology, Layout, and Routing Desired

After calculating the timing budget, determine the approximate location of the processor and the chipset on the baseboard.

## 4.1.3. Pre-Layout Simulation

### 4.1.3.1. Methodology

Analog simulations are recommended for high-speed system bus designs. Start simulations prior to layout. Pre-layout simulations provide a detailed picture of the working “solution space” that meets flight time and signal quality requirements. The layout recommendations in the previous sections are based on pre-layout simulations conducted at Intel. By basing board layout guidelines on the solution space, the iterations between layout and post-layout simulation can be reduced.

Intel recommends running simulations at the **device pads** for signal quality and at the **device pins** for timing analysis. However, simulation results at the device pins may be used later to correlate simulation performance against actual system measurements.

### 4.1.3.2. Sensitivity Analysis

Pre-layout analysis includes a sensitivity analysis using parametric sweeps. Parametric sweep analysis involves varying one or two system parameters while all others such as driver strength, package, $Z_0$, and $S_0$ are held constant. This way, the sensitivity of the proposed bus topology to varying parameters can be analyzed systematically. Sensitivity of the bus to minimum flight time, maximum flight time, and signal quality should be covered. Suggested sweep parameters include trace lengths, termination resistor values, and any other factors that may affect flight time, signal quality, and feasibility of layout. Minimum flight time and worst signal quality are typically analyzed using fast I/O buffers and interconnect. Maximum flight time is typically analyzed using slow I/O buffers and slow interconnects.

Outputs from each sweep should be analyzed to determine which regions meet timing and signal quality specifications. To establish the working solution space, find the common space across all the sweeps that result in passing timing and signal quality. The solution space should allow enough design flexibility for a feasible, cost-effective layout.

### 4.1.3.3. Monte Carlo Analysis

Perform a Monte Carlo analysis to refine the passing solution space region. A Monte Carlo analysis involves randomly varying parameters (independent of one another) over their tolerance range. This analysis intends to ensure that no regions of failing flight time and signal quality exists between the extreme corner cases run in pre-layout simulations. For the example topology, vary the following parameters during Monte Carlo simulations:

- Lengths L1 through L3
- Termination resistance $R_{TT}$ on the processor cartridge #1
- Termination resistance $R_{TT}$ on the processor cartridge #2
- $Z_0$ of traces on processor substrate cartridge #1
- $Z_0$ of traces on processor substrate cartridge #2
- $S_0$ of traces on processor substrate cartridge #1
- $S_0$ of traces on processor substrate cartridge #1
- $Z_0$ of traces on baseboard
- $S_0$ of traces on baseboard
- Fast and slow corner processor I/O buffer models for processor cartridge #1
- Fast and slow corner processor I/O buffer models for processor cartridge #2
- Fast and slow package models for processor cartridge #1
- Fast and slow package models for processor cartridge #2
- Fast and slow corner Intel 82810E GMCH I/O buffer models
- Fast and slow Intel 82810E GMCH package models

### 4.1.3.4. Simulation Criteria

Accurate simulations require that the actual range of parameters be used in the simulations. Intel has consistently measured the cross-sectional resistivity of the PCB copper to be approximately 1 Ω *$mil^2$/inch, not the 0.662 Ω *$mil^2$/inch value for annealed copper that is published in reference material. Using the 1 Ω *$mil^2$/inch value may increase the accuracy of lossy simulations.

Positioning drivers with faster edges closer to the middle of the network typically results in more noise than positioning them towards the ends. However, Intel has shown that drivers located in all positions (given appropriate variations in the other network parameters) can generate the worst- case noise margin. Therefore, Intel recommends simulating the networks from all driver locations, and analyzing each receiver for each possible driver.

Analysis has shown that **both fast and slow corner conditions** must be run for both rising and falling edge transitions. The fast corner is needed because the fast edge rate creates the most noise. The slow corner is needed because the buffer's drive capability will be a minimum, causing the $V_{OL}$ to shift up, which may cause the noise from the slower edge to exceed the available budget. Slow corner models may produce minimum flight time violations on rising edges if the transition starts from a higher $V_{OL}$. So, Intel **highly recommends** checking for minimum and maximum flight time violations with both the fast and slow corner models.

The transmission line package models must be inserted between the output of the buffer and the net it is driving. Likewise, the package model must also be placed between a net and the input of a receiver model. Editing the simulator's net description or topology file generally does this.

Intel has found wide variation in noise margins when varying the stub impedance and the PCB's Z0 and S0. Intel, therefore, recommends that PCB parameters be controlled as tightly as possible, with a sampling of the allowable Z0 and S0 simulated. The Pentium III processor nominal effective line impedance is 65 Ω ±15%. Future Pentium III processor effective line impedance ($Z_{EFF}$) may be 60 Ω ±15%. Intel recommends the baseboard nominal effective line impedance to be at 60 Ω ±15% for the recommended layout guidelines to be effective. Intel also recommends running uncoupled simulations using the $Z_0$ of the package stubs and performing fully coupled simulations if increased accuracy is needed or desired. Accounting for crosstalk within the device package by varying the stub impedance was investigated and was not found to be sufficiently accurate. This lead to the development of full package models for the component packages.

## 4.1.4. Place and Route Board

### 4.1.4.1. Estimate Component to Component Spacing for AGTL+ Signals

Estimate the number of layers that will be required. Then determine the expected interconnect distances between each of the components on the AGTL+ bus. Using the estimated interconnect distances, verify that the placement can support the system timing requirements.

The required bus frequency and the maximum flight time propagation delay on the PCB determine the maximum network length between the bus agents. The minimum network length is independent of the required bus frequency. Table 32 and Table 33 assume values for $CLK_{SKEW}$ and $CLK_{JITTER}$ (parameters that are controlled by the system designer). To reduce system clock skew to a minimum, clock buffers that allow their outputs to be tied together are recommended. Intel strongly recommends running analog simulations to ensure that each design has adequate noise and timing margin.

### 4.1.4.2. Layout and Route Board

Route the board satisfying the estimated space and timing requirements. Also stay within the solution space set from the pre-layout sweeps. Estimate the printed circuit board parameters from the placement and other information including the following general guidelines:

- Distribute $V_{TT}$ with a power plane or a partial power plane. If this cannot be accomplished, use as wide a trace as possible and route the $V_{TT}$ trace with the same topology as the AGTL+ traces.
- Keep the overall length of the bus as short as possible (but do not forget minimum component- to-component distances to meet hold times).
- Plan to minimize crosstalk with the following guidelines developed for the example topology given (signal spacing recommendations were based on fully coupled simulations; spacing may be decreased based upon the amount of coupled length).
  - Use an intragroup AGTL+ spacing to line width to dielectric thickness ratio of at least 2:1:1 for microstrip geometry. If $e_r = 4.5$, this should limit coupling to 3.4%. For example, intragroup AGTL+ routing could use 10 mil spacing, 5 mil traces, and a 5 mil prepreg between the signal layer and the plane it references (assuming a 4-layer motherboard design).
  - Minimize the dielectric process variation used in the PCB fabrication.
  - Eliminate parallel traces between layers not separated by a power or ground plane.

Table 34 contains the trace width:space ratios assumed for this topology. The crosstalk cases considered in this guideline involve three types: Intragroup AGTL+, Intergroup AGTL+, and AGTL+ to non-AGTL+.

Intra-group AGTL+ crosstalk involves interference between AGTL+ signals within the same group (See Section 4.3). Intergroup AGTL+ crosstalk involves interference from AGTL+ signals in a particular group to AGTL+ signals in a different group. An example of AGTL+ to non-AGTL+ crosstalk is when CMOS and AGTL+ signals interfere with each other.

**Table 34. Trace Width Space Guidelines**

| Crosstalk Type | Trace Width:Space Ratio |
|---|---|
| Intragroup AGTL+ (same group AGTL+) | 5:10 or 6:12 |
| Intergroup AGTL+ (different group AGTL+) | 5:15 or 6:18 |
| AGTL+ to non-AGTL+ | 5:20 or 6:24 |

The spacing between the various bus agents causes variations in trunk impedance and stub locations. These variations cause reflections that can cause constructive or destructive interference at the receivers. A reduction of noise may be obtained by a minimum spacing between the agents. Unfortunately, tighter spacing results in reduced component placement options and lower hold margins. Therefore, adjusting the inter-agent spacing may be one way to change the network's noise margin, but mechanical constraints often limit the usefulness of this technique. Always be sure to validate signal quality after making any changes in agent locations or changes to inter-agent spacing.

There are six AGTL+ signals that can be driven by more than one agent simultaneously. These signals may require more attention during the layout and validation portions of the design. When a signal is asserted (driven low) by two or more agents on the same clock edge, the two falling edge wave fronts will meet at some point on the bus and can sum to form a negative voltage. The ring- back from this negative voltage can easily cross into the overdrive region. The signals are AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#.

This section addresses AGTL+ layout for both 1 and 2-way 133 MHz/100 MHz processor/Intel 810E2 chipset systems. Power distribution and chassis requirements for cooling, connector location, memory location, etc., may constrain the system topology and component placement location; therefore, constraining the board routing. These issues are not directly addressed in this document. Chapter 1 contains a listing of several documents that address some of these issues.

### 4.1.5. Post-Layout Simulation

Following layout, extract the interconnect information for the board from the CAD layout tools. Run simulations to verify that the layout meets timing and noise requirements. A small amount of "tuning" may be required; experience at Intel has shown that sensitivity analysis dramatically reduces the amount of tuning required. The post layout simulations should take into account the expected variation for all interconnect parameters.

Intel specifies signal integrity **at the device pads** and therefore recommends running simulations at the device pads for signal quality. However, Intel specifies core timings **at the device pins,** so simulation results at the device pins should be used later to correlate simulation performance against actual system measurements.

#### 4.1.5.1. Intersymbol Interference

Intersymbol Interference (ISI) refers to the distortion or change in the waveform shape caused by the voltage and transient energy on the network when the driver begins its next transition.

Intersymbol Interference (ISI) occurs when transitions in the current cycle interfere with transitions in subsequent cycles. ISI can occur when the line is driven high, low, and then high in consecutive cycles (the opposite case is also valid). When the driver drives high on the first cycle and low on the second cycle, the signal may not settle to the minimum $V_{OL}$ before the next rising edge is driven. This results in improved flight times in the third cycle. Intel performed ISI simulations for the topology given in this section by comparing flight times for the first and third cycle. ISI effects do not necessarily span only 3 cycles so it may be necessary to simulate beyond 3 cycles for certain designs. After simulating and quantifying ISI effects, adjust the timing budget accordingly to take these conditions into consideration.

#### 4.1.5.2. Crosstalk Analysis

AGTL+ crosstalk simulations can consider the processor core package, Intel 82810E2 GMCH package, and SC242 connectors as non-coupled. Treat the traces on the processor cartridge and baseboard as fully coupled for maximum crosstalk conditions. Simulate the traces as lossless for worst case crosstalk and lossy where more accuracy is needed. Evaluate both odd and even mode crosstalk conditions.

AGTL+ Crosstalk simulation involves the following cases:

- Intra-group AGTL+ crosstalk
- Inter-group AGTL+ crosstalk
- Non-AGTL+ to AGTL+ crosstalk

#### 4.1.5.3. Monte Carlo Analysis

Perform a Monte Carlo analysis on the extracted baseboard. Vary all parameters recommended for the pre-layout Monte Carlo analysis within the region that they are expected to vary. The range for some parameters will be reduced compared to the pre-layout simulations. For example, baseboard lengths L1 through L7 should no longer vary across the full min and max range on the final baseboard design. Instead, baseboard lengths should now have an actual route, with a length tolerance specified by the baseboard fabrication manufacturer.

### 4.1.6. Validation

Build systems and validate the design and simulation assumptions.

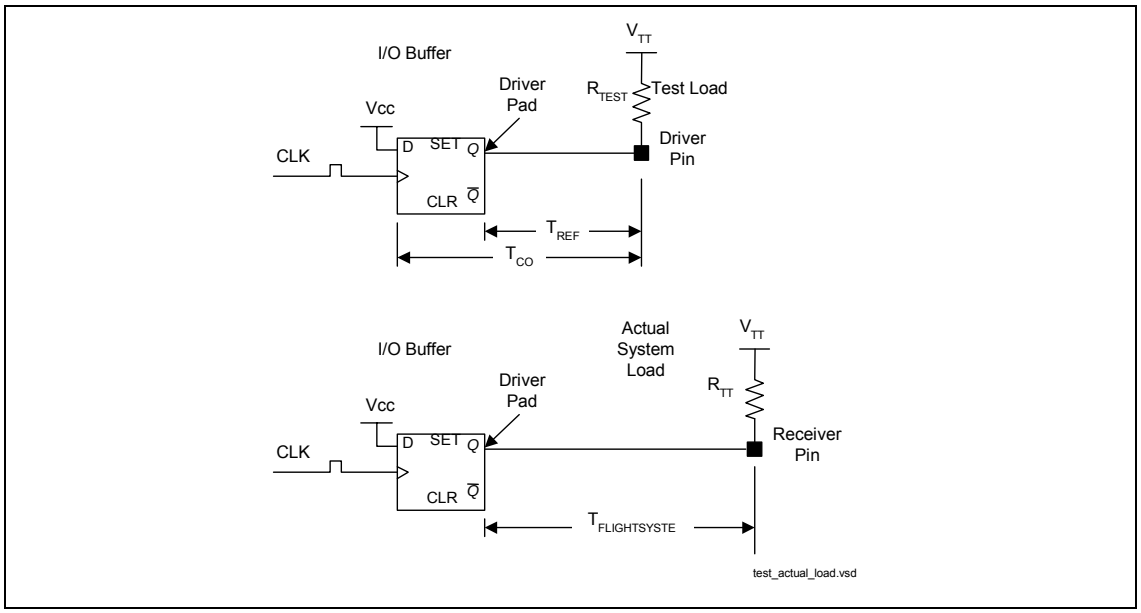
#### 4.1.6.1. Measurements

Note that the AGTL+ specification for signal quality is at the **pad** of the component. The expected method of determining the signal quality is to run analog simulations for the pin and the pad. Then correlate the simulations at the pin against actual system measurements at the pin. Good correlation at the pin leads to confidence that the simulation at the pad is accurate. Controlling the temperature and voltage to correspond to the I/O buffer model extremes should enhance the correlation between simulations and the actual system.

### 4.1.6.2. Flight Time Simulation

As defined in Chapter 1, flight time is the time difference between a signal crossing $V_{REF}$ at the input pin of the receiver, and the output pin of the driver crossing $V_{REF}$ were it driving a test load. The timings in the tables and topologies discussed in this guideline assume the actual system load is 50 Ω and is equal to the test load. While the DC loading of the AGTL+ bus in a DP mode is closer to 25 Ω, AC loading is approximately 29 Ω since the driver effectively "sees" a 56 Ω termination resistor in parallel with a 60 Ω transmission line on the cartridge.

**Figure 70. Test Load vs. Actual System Load**




The figure above shows the different configurations for $T_{CO}$ testing and flight time simulation. The flip-flop represents the logic input and driver stage of a typical AGTL+ I/O buffer. $T_{CO}$ timings are specified at the driver pin output. $T_{FLIGHT-SYSTEM}$ is usually reported by a simulation tool as the time from the driver pad starting its transition to the time when the receiver's input pin sees a valid data input. Since both timing numbers ($T_{CO}$ and $T_{FLIGHT-SYSTEM}$) include propagation time from the pad to the pin, it is necessary to subtract this time ($T_{REF}$) from the reported flight time to avoid double counting. $T_{REF}$ is defined as the time that it takes for the driver output pin to reach the measurement voltage, $V_{REF}$, starting from the beginning of the driver transition at the pad. $T_{REF}$ must be generated using the same test load for $T_{CO}$. Intel provides this timing value in the AGTL+ I/O buffer models.

In this manner, the following *valid delay* equation is satisfied:

#### Valid Delay Equation

$$\text{Valid Delay} = T_{CO} + T_{FLIGHT-SYS} - T_{REF} = T_{CO-MEASURED} + T_{FLIGHT-MEASURED}$$

This valid delay equation is the total time from when the driver sees a valid clock pulse to the time when the receiver sees a valid data input.

#### 4.1.6.3. Flight Time Hardware Validation

When a measurement is made on the actual system, $T_{CO}$ and flight time do not need $T_{REF}$ correction since these are the actual numbers. These measurements include all of the effects pertaining to the driver-system interface and the same is true for the $T_{CO}$. Therefore the addition of the measured $T_{CO}$ and the measured flight time must be equal to the valid delay calculated above.

- Changes in flight time due to crosstalk, noise, and other effects.

## 4.2. Theory

### 4.2.1. AGTL+

AGTL+ is the electrical bus technology used for the processor bus. This is an incident wave switching, open-drain bus with external pull-up resistors that provide both the high logic level and termination at each load. The processor AGTL+ drivers contain a full-cycle active pull-up device to improve system timings. The AGTL+ specification defines:

- Termination voltage ($V_{TT}$).
- Receiver reference voltage ($V_{REF}$) as a function of termination voltage ($V_{TT}$).
- processor termination resistance ($R_{TT}$).
- Input low voltage ($V_{IL}$).
- Input high voltage ($V_{IH}$).
- NMOS on resistance ($R_{ONN}$).
- PMOS on resistance ($R_{ONP}$).
- Edge rate specifications.
- Ringback specifications.
- Overshoot/Undershoot specifications.
- Settling Limit.

### 4.2.2. Timing Requirements

The system timing for AGTL+ is dependent on many things. Each of the following elements combine to determine the maximum and minimum frequency the AGTL+ bus can support:

- The range of timings for each of the agents in the system.
  - Clock to output ($T_{CO}$). (Note that the system load is likely to be different from the "specification" load therefore the $T_{CO}$ observed in the system might not be the same as the $T_{CO}$ from the specification.)
  - The minimum required setup time to clock ($T_{SU\_MIN}$) for each receiving agent.
- The range of flight time between each component. This includes:
  - The velocity of propagation for the loaded printed circuit board [$S_{EFF}$].
  - The board loading impact on the effective $T_{CO}$ in the system.
- The amount of skew and jitter in the system clock generation and distribution.
- Changes in flight time due to crosstalk, noise, and other effects.

## 4.2.3. Crosstalk Theory

AGTL+ signals swing across a smaller voltage range and have a correspondingly smaller noise margin than technologies that have traditionally been used in personal computer designs. This requires that designers using AGTL+ be more aware of crosstalk than they may have been in past designs.

Crosstalk is caused through capacitive and inductive coupling between networks. Crosstalk appears as both backward crosstalk and as forward crosstalk. Backward crosstalk creates an induced signal on a victim network that propagates in a direction opposite that of the aggressor's signal. Forward crosstalk creates a signal that propagates in the same direction as the aggressor's signal. On the AGTL+ bus, a driver on the aggressor network is not at the end of the network; therefore it sends signals in both directions on the aggressor's network. The figure below shows a driver on the aggressor network and a receiver on the victim network that are not at the ends of the network. The signal propagating in each direction causes crosstalk on the victim network.

**Figure 71. Aggressor and Victim Networks**

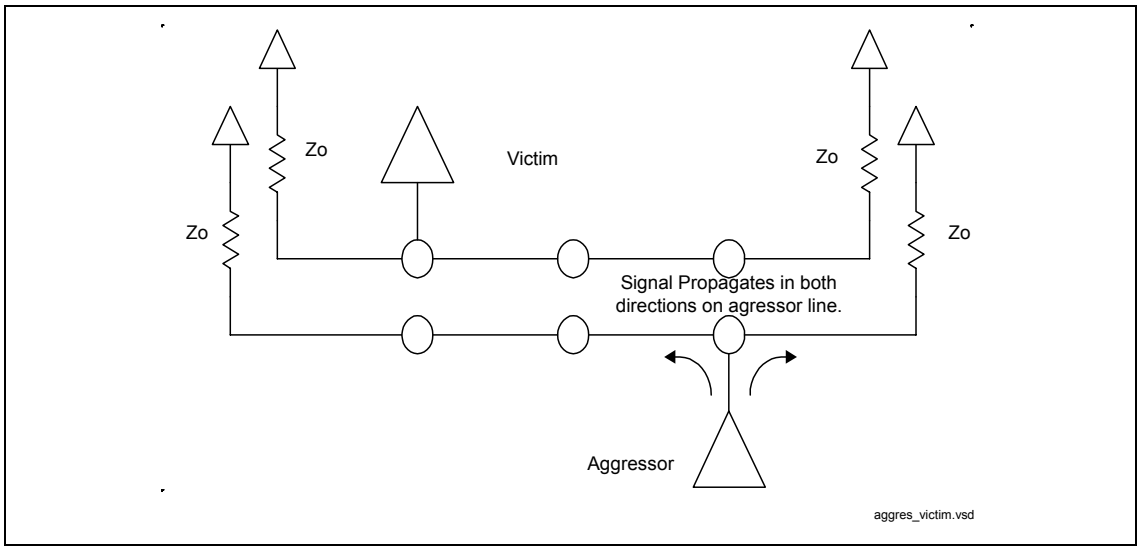
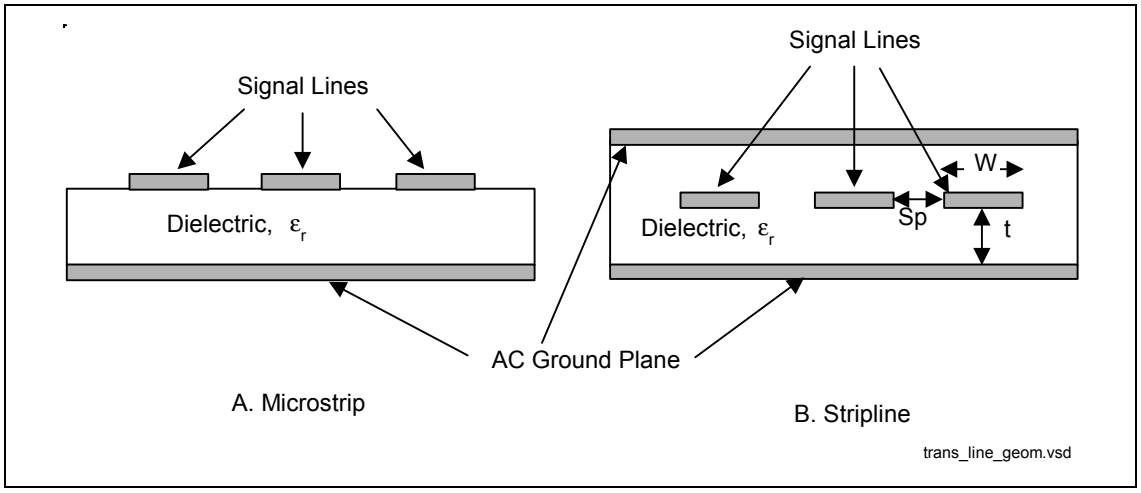



**Figure 72. Transmission Line Geometry: (A) Microstrip (B) Stripline**



Additional aggressors are possible in the z-direction, if adjacent signal layers are not routed in mutually perpendicular directions. Because crosstalk-coupling coefficients decrease rapidly with increasing separation, it is rarely necessary to consider aggressors that are at least five line widths separated from the victim. The maximum crosstalk occurs when all the aggressors are switching in the same direction at the same time.

There is crosstalk internal to the IC packages, which can also affect the signal quality.

Backward crosstalk is present in both stripline and microstrip geometry (see Figure 72). A way to remember which geometry is stripline and which is microstrip is that a stripline geometry requires **stripping** a layer away to see the signal lines. The backward-coupled amplitude is proportional to the backward crosstalk coefficient, the aggressor's signal amplitude, and the coupled length of the network up to a maximum that is dependent on the rise/fall time of the aggressor's signal. Backward crosstalk reaches a maximum (and remains constant) when the propagation time on the coupled network length exceeds one half of the rise time of the aggressor's signal. Assuming the ideal ramp on the aggressor from 0% to 100% voltage swing, and the fall time on an unloaded coupled network, then:

LengthforMaxBaxkwardCrosstalk = (½ x FallTime) / (BoardDelayPerUnitLength)

An example calculation follows when the fast corner fall time is 3 V/ns and board delay is 175 ps/inch (2.1 ns/foot):

Fall time = 1.5 V/3 V/ns = 0.5 ns

Length for Max Backward Crosstalk = ½ * 0.5 ns * 1000 ps/ns /175 ps/in = 1.43 inches

Agents on the AGTL+ bus drive signals in each direction on the network. This causes backward crosstalk from segments on two sides of a driver. The pulses from the backward crosstalk travel toward each other and meet and **add** at certain moments and positions on the bus. This can cause the voltage (noise) from crosstalk to double.

#### 4.2.3.1. Potential Termination Crosstalk Problems

The use of commonly used "pull-up" resistor networks for AGTL+ termination may not be suitable. These networks have a common power or ground pin at the extreme end of the package, shared by 13 to 19 resistors (for 14- and 20-pin components). These packages generally have too much inductance to maintain the voltage/current needed at each resistive load. Intel recommends using discrete resistors, resistor networks with separate power/ground pins for each resistor, or working with a resistor network vendor to obtain resistor networks that have acceptable characteristics.

## 4.3. More Details and Insight

### 4.3.1. Textbook Timing Equations

The following "textbook" equations used to calculate the propagation rate of a PCB are the basis for spreadsheet calculations for timing margin based on the component parameters.

### Intrinsic Impedance

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \ (\Omega)$$

### Stripline Intrinsic Propagation Speed

$$S_{0\_STRIPLINE} = 1.017 * \sqrt{\varepsilon_r} \ (\text{ns/ft})$$

### Microstrip Intrinsic Propagation Speed

$$S_{0\_MICROSTRIP} = 1.017 * \sqrt{0.475 * \varepsilon_r + 0.67} \ (\text{ns/ft})$$

### Effective Propagation Speed

$$S_{EFF} = S_0 * \sqrt{1 + \frac{C_D}{C_0}} \ (\text{ns/ft})$$

### Effective Impedance

$$Z_{EFF} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}} \ (\Omega)$$

### Distributed Trace Capacitance

$$C_0 = \frac{S_0}{Z_0} \ (\text{pF/ft})$$

### Distributed Trace Inductance

$$L_0 = 12 * Z_0 * S_0 \ (\text{nH/ft})$$

Symbols for the above equations are:

- $S_0$ is the speed of the signal on an unloaded PCB in ns/ft. This is referred to as the board propagation constant.
- $S_{0\ MICROSTRIP}$ and $S_{0\ STRIPLINE}$ refer to the speed of the signal on an unloaded microstrip or stripline trace on the PCB in ns/ft.
- $Z_0$ is the intrinsic impedance of the line in Ω and is a function of the dielectric constant ($\varepsilon_r$), the line width, line height and line space from the plane(s). The equations for $Z_0$ are not included in this document. See the *MECL System Design Handbook* by William R. Blood, Jr. for these equations.
- $C_0$ is the distributed trace capacitance of the network in pF/ft.
- $L_0$ is the distributed trace inductance of the network in nH/ft.
- $C_D$ is the sum of the capacitance of all devices and stubs divided by the length of the network's trunk, not including the portion connecting the end agents to the termination resistors in pF/ft.
- $S_{EFF}$ and $Z_{EFF}$ are the effective propagation constant and impedance of the PCB when the board is "loaded" with the components.

## 4.3.2. Effective Impedance and Tolerance/Variation

The impedance of the PCB needs to be controlled when the PCB is fabricated. The method of specifying control of the impedance needs to be determined to best suit each situation. Using stripline transmission lines (where the trace is between two reference planes) is likely to give better results than microstrip (where the trace is on an external layer using an adjacent plane for reference with solder mask and air on the other side of the trace). This is in part due to the difficulty of precise control of the dielectric constant of the solder mask, and the difficulty in limiting the plated thickness of microstrip conductors, which can substantially increase crosstalk.

The effective line impedance ($Z_{EFF}$) is recommended to be 60 Ω ±15%, where $Z_{EFF}$ is defined by "Effective Impedance" equation.

## 4.3.3. Power/Reference Planes, PCB Stackup, and High Frequency Decoupling

### 4.3.3.1. Power Distribution

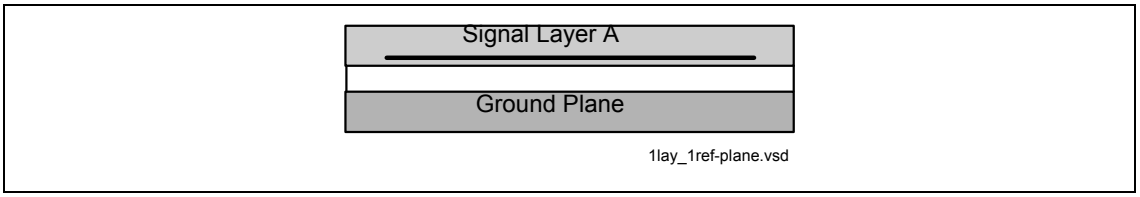
Designs using the Intel Pentium III processor require several different voltages. The following paragraphs describe some of the impact of two common methods used to distribute the required voltages. Refer to the *Flexible Motherboard Power Distribution Guidelines* for more information on power distribution.

The most conservative method of distributing these voltages is for each of them to have a dedicated plane. If any of these planes are used as an "AC ground" reference for traces to control trace impedance on the board, then the plane needs to be AC-coupled to the system ground plane. This method may require more total layers in the PCB than other methods. A 1 ounce/ft$^2$ thick copper is recommended for all power and reference planes.

A second method of power distribution is to use partial planes in the immediate area needing the power, and to place these planes on a routing layer on an as-needed basis. These planes still need to be decoupled to ground to ensure stable voltages for the components being supplied. This method has the disadvantage of reducing area that can be used to route traces. These partial planes may also change the impedance of adjacent trace layers. (For instance, the impedance calculations may have been done for microstrip geometry, and adding a partial plane on the other side of the trace layer may turn the microstrip into a stripline.)

It is **strongly recommended** that baseboard stackup be arranged such that AGTL+ signals are referenced to a ground (VSS) plane, and that the AGTL+ signals do not traverse multiple signal layers. Deviating from either guideline can create discontinuities in the signal's return path that can lead to large SSO effects that degrade timing and noise margin. Designing an AGTL+ platform incorporating discontinuities will expose the platform to a risk that is very hard to predict in pre-layout simulation. The figure below shows the ideal case where a particular signal is routed entirely within the same signal layer, with a ground layer as the single reference plane.

**Figure 73. One Signal Layer and One Reference Plane**



When it is not possible to route the entire AGTL+ signal on a single VSS referenced layer, there are methods to reduce the effects of layer switches. The best alternative is to allow the signals to change layers while staying referenced to the same plane (see Figure 74). Figure 75 shows another method of minimizing layer switch discontinuities, but may be less effective than Figure 74. In this case, the signal still references the same type of reference plane (ground). In such a case, it is important to stitch (i.e., connect) the two ground planes together with vias in the vicinity of the signal transition via.

**Figure 74. Layer Switch with One Reference Plane**

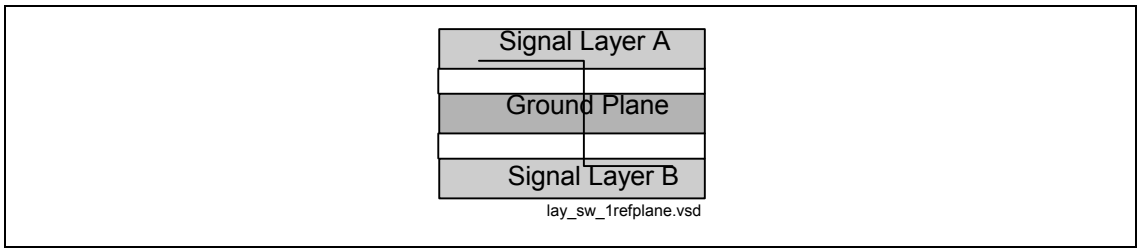
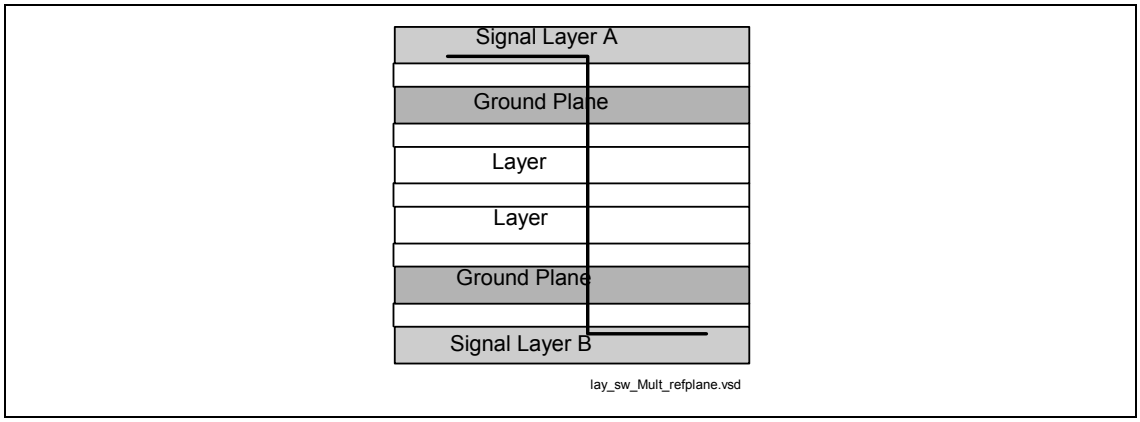



**Figure 75. Layer Switch with Multiple Reference Planes (same type)**




When routing and stackup constraints require that an AGTL+ signal reference VCC or multiple planes, special care must be given to minimize the SSO impact on timing and noise margin. The best method of reducing adverse effects is to add high-frequency decoupling wherever the transitions occur, as shown in Figure 76 and Figure 77. Such decoupling should, again, be in the vicinity of the signal transition via and use capacitors with minimal effective series resistance (ESR) and effective series inductance (ESL). When placing the caps, it is recommended to space the VSS and VCC vias as close as possible and/or use dual vias since the via inductance may sometimes be higher than the actual capacitor inductance.

**Figure 76. Layer Switch with Multiple Reference Planes**

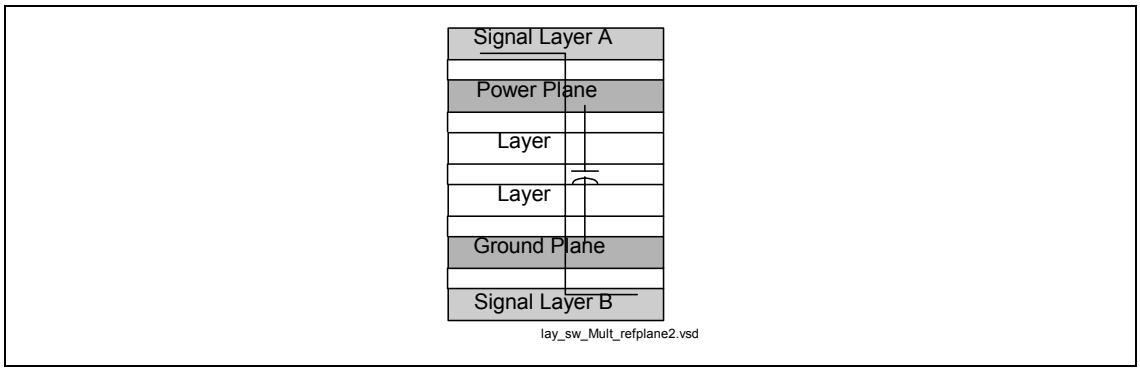
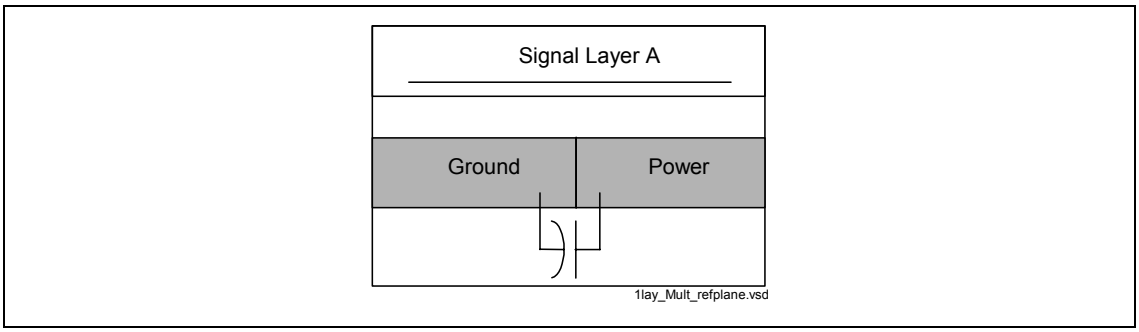


**Figure 77. One Layer with Multiple Reference Planes**




### 4.3.3.2. High Frequency Decoupling

This section contains several high frequency decoupling recommendations that will improve the return path for an AGTL+ signal. These design recommendations will likely reduce the amount of SSO effects.

Just as layer switching and multiple reference planes can create discontinuities in an AGTL+ signal return path, discontinuities may also occur when a signal transitions between the baseboard and cartridge. Therefore, providing adequate high-frequency decoupling across $VCC_{CORE}$ and ground at the SC242 connector interface on the baseboard will minimize the discontinuity in the signal's reference plane at this junction. Note that these additional high-frequency decoupling capacitors are in addition to the high-frequency decoupling already on the processor.

Transmission line geometry also influences the return path of the reference plane. The following are decoupling recommendations that take this into consideration:

- A signal that transitions from a stripline to another stripline should have close proximity decoupling between all four reference planes.
- A signal that transitions from a stripline to a microstrip (or vice versa) should have close proximity decoupling between the three reference planes.
- A signal that transitions from a stripline or microstrip through vias or pins to a component (Intel 82810E GMCH, etc.) should have close proximity decoupling across all involved reference planes to ground for the device.

### 4.3.4. Clock Routing

Analog simulations are required to ensure clock net signal quality and skew is acceptable. The system clock skew must be kept to a minimum (The calculations and simulations for the example topology given in this document have a total clock skew of 200 ps and 150 ps of clock jitter). For a given design, the clock distribution system, including the clock components, must be evaluated to ensure these same values are valid assumptions. Each processor's datasheet specifies the clock signal quality requirements. To help meet these specifications, follow these general guidelines:

- Tie clock driver outputs if clock buffer supports this mode of operation.
- Match the electrical length and type of traces on the PCB (microstrip and stripline may have different propagation velocities).
- Maintain consistent impedance for the clock traces.
  - Minimize the number of vias in each trace.
  - Minimize the number of different trace layers used to route the clocks.
  - Keep other traces away from clock traces.
- Lump the loads **at the end** of the trace if multiple components are to be supported by a single clock output.
- Have equal loads at the end of each network.

The **ideal** way to route each clock trace is on the same single inner layer, next to a ground plane, isolated from other traces, with the same total trace length, to the same type of single load, with an equal length ground trace parallel to it, and driven by a zero skew clock driver. When deviations from ideal are required, going from a single layer to a pair of layers adjacent to power/ground planes would be a good compromise. The fewer number of layers the clocks are routed on, the smaller the impedance difference between each trace is likely to be. Maintaining an equal length and parallel ground trace for the **total length of each** clock ensures a low inductance ground return and produces the minimum current path loop area. (The parallel ground trace will have lower inductance than the ground plane because of the mutual inductance of the current in the clock trace.)

## 4.4. Definitions of Flight Time Measurements/ Corrections and Signal Quality

Acceptable signal quality must be maintained over all operating conditions to ensure reliable operation. Signal Quality is defined by four parameters: Overshoot, Undershoot, Settling Limit, and Ringback. Timings are measured at the pins of the driver and receiver, while signal integrity is observed at the receiver chip pad. When signal integrity at the pad violates the following guidelines and adjustments need to be made to flight time, the adjusted flight time obtained at the chip pad can be assumed to have been observed at the package pin, usually with a small timing error penalty.

### 4.4.1. $V_{REF}$ Guardband

To account for noise sources that may affect the way an AGTL+ signal becomes valid at a receiver, $V_{REF}$ is shifted by $\Delta V_{REF}$ for measuring minimum and maximum flight times. The $V_{REF}$ Guardband region is bounded by $V_{REF}$ - $\Delta V_{REF}$ and $V_{REF}$ + $\Delta V_{REF}$. $\Delta V_{REF}$ has a value of 100 mV, which accounts for the following noise sources:

- Motherboard coupling
- VTT noise
- VREF noise

### 4.4.2. Ringback Levels

The example topology covered in this guideline assumes ringback tolerance allowed to within 200 mV of 2/3 VTT. Since VTT is specified with approximate total ±11% tolerance, this implies a 2/3 VTT (VREF) range from approximately 0.89 V to 1.11 V. This places the absolute ringback limits at:

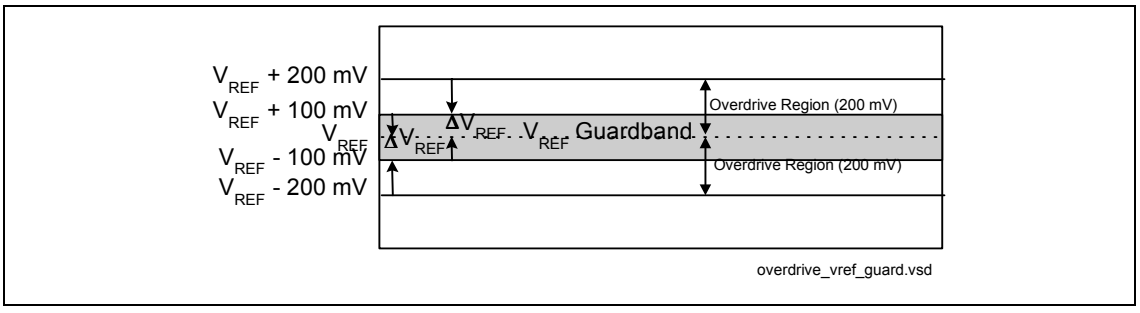
- 1.3 V (1.1 V + 200 mV) for rising edge ringback
- 0.69 V (0.89 V – 200 mV) for falling edge ringback

A violation of these ringback limits requires flight time correction as documented in the *Intel® Pentium® II Processor Developer's Manual*.

### 4.4.3. Overdrive Region

The overdrive region is the voltage range, at a receiver, from $V_{REF}$ to $V_{REF}$ + 200 mV for a low-to- high going signal and $V_{REF}$ to $V_{REF}$ - 200 mV for a high-to-low going signal. The overdrive regions encompass the $V_{REF}$ Guardband. So, when $V_{REF}$ is shifted by $\Delta V_{REF}$ for timing measurements, the overdrive region **does not** shift by $\Delta V_{REF}$. The figure below depicts this relationship. Corrections for edge rate and ringback are documented in the *Intel® Pentium® II Processor Developer's Manual*. However, there is an exception to the documented correction method. The *Intel® Pentium® II Processor Developer's Manual* states that extrapolations should be made from the last crossing of the overdrive region back to $V_{REF}$. Simulations performed on this topology should extrapolate back to the appropriate $V_{REF}$ Guardband boundary, and not $V_{REF}$. So, for maximum rising edge correction, extrapolate back to $V_{REF}$ + $\Delta V_{REF}$. For maximum falling edge corrections, extrapolate back to $V_{REF}$ - $\Delta V_{REF}$.

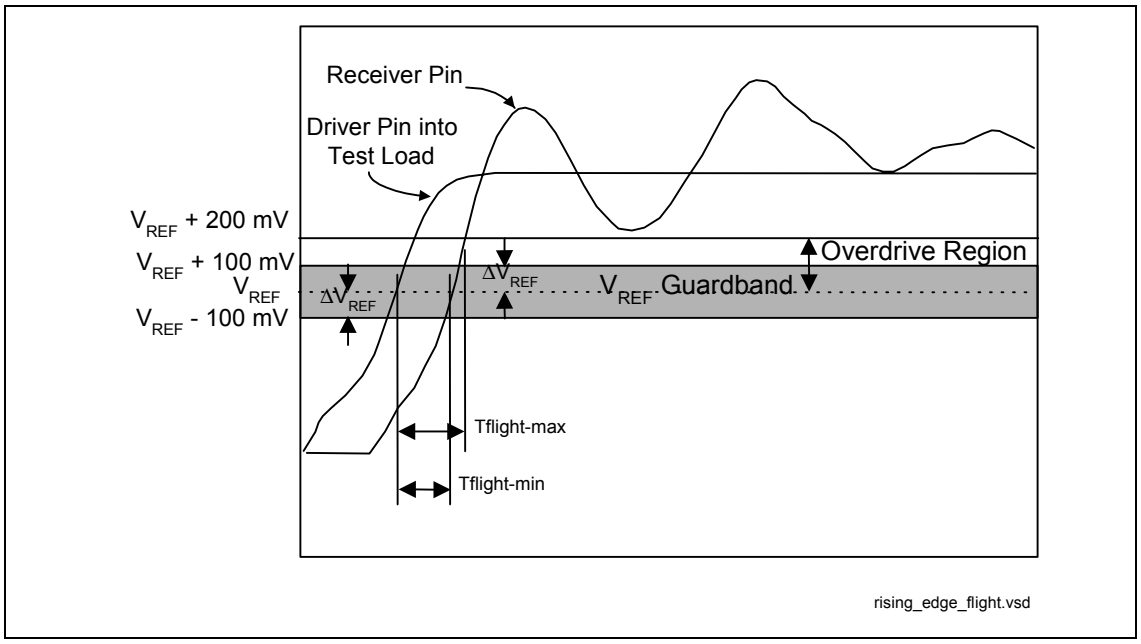
**Figure 78. Overdrive Region and $V_{REF}$ Guardband**



## 4.4.4. Flight Time Definition and Measurement

Timing measurements consist of minimum and maximum flight times to take into account that devices can turn on or off anywhere in a $V_{REF}$ Guardband region. This region is bounded by $V_{REF} - \Delta V_{REF}$ and $V_{REF} + \Delta V_{REF}$. The minimum flight time for a rising edge is measured from the time the driver crosses $V_{REF}$ when terminated to a test load, to the time when the signal first crosses $V_{REF} - \Delta V_{REF}$ at the receiver (see the figure below). Maximum flight time is measured to the point where the signal first crosses $V_{REF} + \Delta V_{REF}$, assuming that ringback, edge rate, and monotonicity criteria are met. Similarly, minimum flight time measurements for a falling edge are taken at the $V_{REF} + \Delta V_{REF}$ crossing and maximum flight time is taken at the $V_{REF} - \Delta V_{REF}$ crossing.

**Figure 79. Rising Edge Flight Time Measurement**




## 4.4.5. Conclusion

AGTL+ routing requires a significant amount of effort. Planning ahead and leaving the necessary time available for correctly designing a board layout will provide the designer with the best chance of avoiding the more difficult task of debugging inconsistent failures caused by poor signal integrity. Intel recommends planning a layout schedule that allows time for each of the tasks outlined in this document.

# 5. Clocking

## 5.1. Clock Generation

There is only one clock generator component required in an 810E2 chipset system. The CK810E clock chip is pin compatible with the CK810 clock chip, which comes in a single 56-pin SSOP package.

There is one pin function change in the CK810E relative to the CK810, the REFCLK Reset Strap:

**Table 35. REFCLK Reset Strap for CK810 vs. CK810E**

| At reset | APIC Clock Strap | System Bus Freq Select (SEL1) |
|---|---|---|
| After reset | 14 MHz Clock | 14 MHz Clock |
| Reset default | Internal Pull-up for 33 MHz APIC Clock<br>Populate External 10 kΩ Resistor to Ground for 16 MHz | Internal Pull-down for 66 MHz or 100 MHz Bus Freq Select (SEL0)<br>External Drive to 1 to Select 133 MHz System Bus |

The CK810E is a mixed voltage component. Some of the output clocks are 3.3V and some of the output clocks are 2.5V. As a result, the CK810E device requires both 3.3V and 2.5V. These power supplies should be as clean as possible. Noise in the power delivery system for the clock driver can cause noise on the clock lines. The CK810E provides the following clock frequencies.

**Table 36. Intel® 810E2 Chipset Clocks**

| Number | Clock | Frequency |
|---|---|---|
| 3 | Processor Clocks | 66/100/133 MHz |
| 9 | SDRAM Clocks | 100 MHz |
| 8 | PCI Clocks | 33 MHz |
| 2 | APIC Clocks | 16.67/33 MHz |
| 2 | 48 MHz Clocks | 48 MHz |
| 2 | 3V66 MHz Clocks | 66 MHz |
| 1 | REF Clock | 14.31818 MHz |

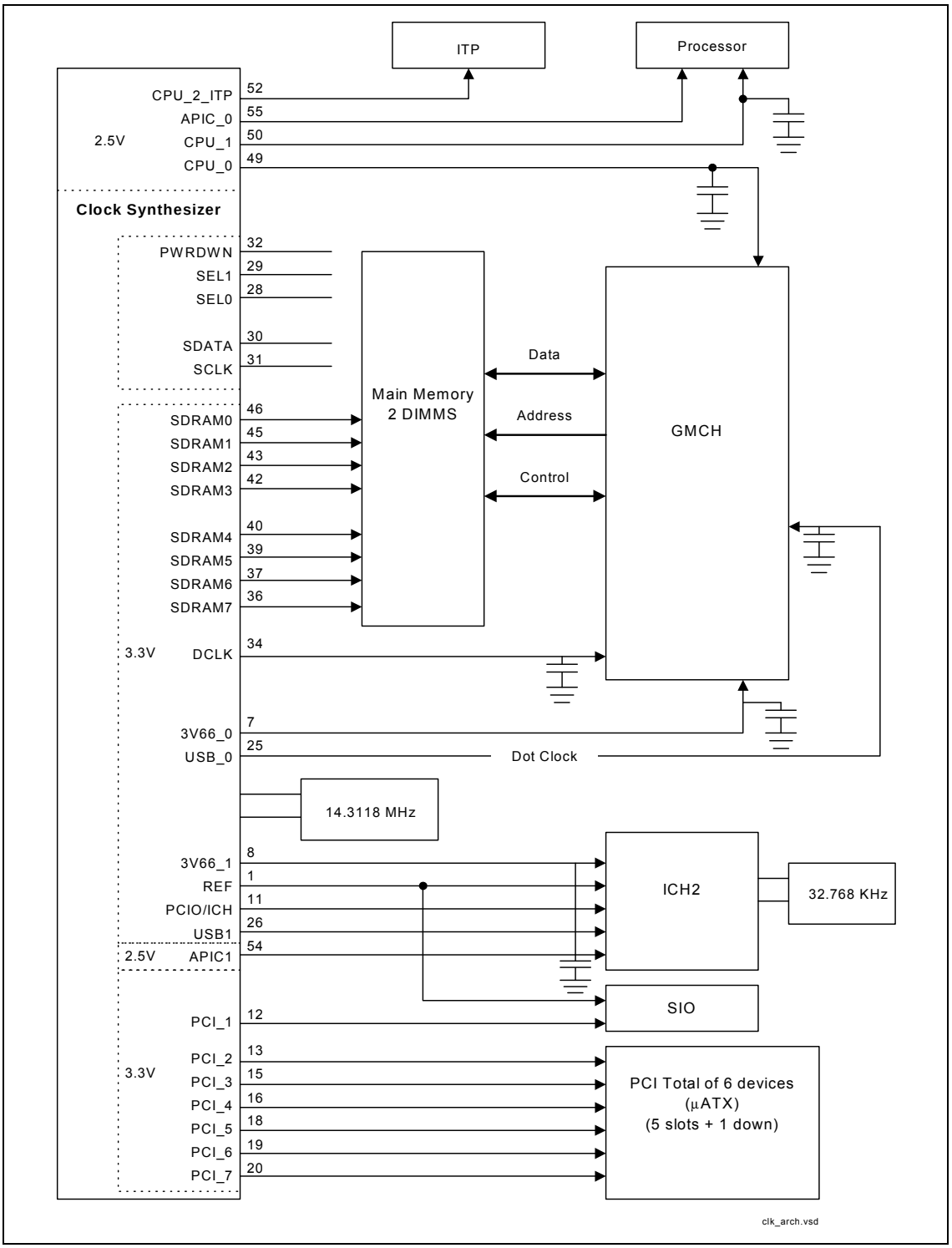
The DCLKREF signal from the external clock synthesizer to the GMCH is a 48 MHz signal. This signal has no length requirements, except those specified in the Design Guide. However, care in routing this signal relative to the DIMM slots is important. Future board designs should attempt to route the DCLKREF trace so that the trace is not parallel to the DIMM slots or does not pass underneath the DIMM slots. This prevents noise coupling of memory-related signals into the 48 MHz clock signal.

### Features (56 Pin SSOP Package)

- 3 copies of processor clock 66/100/133 MHz (2.5V) (Processor, GMCH, ITP)
- 9 copies of 100 MHz (all the time) SDRAM clock (3.3V) (SDRAM[0:7], DClk)
- 8 copies of PCI clock (33 MHz ) (3.3V)
- 2 copies of APIC clock @16.67 MHz or 33 MHz, synchronous to processor clock (2.5V)
- 2 copy of 48 MHz clock (3.3V) [Non SSC]
- 2 copies of 3V66 MHz clock (3.3V)
- 1 copy of REF clock @14.31818 MHz (3.3V) also used as input strap to determine APIC frequency
- 66/100/133 MHz processor operation (selectable at power up only)
- Ref. 14.31818 MHz Xtal oscillator input
- Power Down Pin
- Spread spectrum support
- $I^2C$ Support for turning off unused clocks

## 5.2. Clock Architecture

**Figure 80. Intel® 810E2 Chipset Clock Architecture**



## 5.3. Clock Routing Guidelines

The following table shows the group skew and jitter limits.

**Table 37. Group Skew and Jitter Limits at the Pins of the Clock Chip**

| Signal Group | Pin-Pin Skew | Cycle-Cycle Jitter | Nominal Vdd | Skew, Jitter Measure Point |
|---|---|---|---|---|
| Processor | 175 pS | 250 pS | 2.5V | 1.25V |
| SDRAM | 250 pS | 250 pS | 3.3V | 1.50V |
| APIC | 250 pS | 500 pS | 2.5V | 1.25V |
| 48 MHz | 250 pS | 500 pS | 3.3V | 1.50V |
| 3V66 | 175 pS | 500 pS | 3.3V | 1.50V |
| PCI | 500 pS | 500 pS | 3.3V | 1.50V |
| REF | N/A | 1000 pS | 3.3V | 1.50V |

The following table shows the signal group and resistor tolerance.

**Table 38. Signal Group and Resistor**

| Signal Group | Resistor |
|---|---|
| Processor | 33 Ω ± 5% |
| SDRAM | 22 Ω ± 5% |
| DCLK | 33 Ω ± 5% |
| 3V66 | 22 Ω ± 5% |
| PCI | 33 Ω ± 5% |
| TCLK | 22 Ω ± 5% |
| OCLK/RCLK | 33 Ω ± 5% |
| 48 MHz | 33 Ω ± 5% |
| APIC | 33 Ω ± 5% |
| REF | 10 Ω ± 5% |

The following table shows the layout dimensions for the clock routing.

***Note:*** All the clock signals must be routed on the same layer which reference to a ground plane.

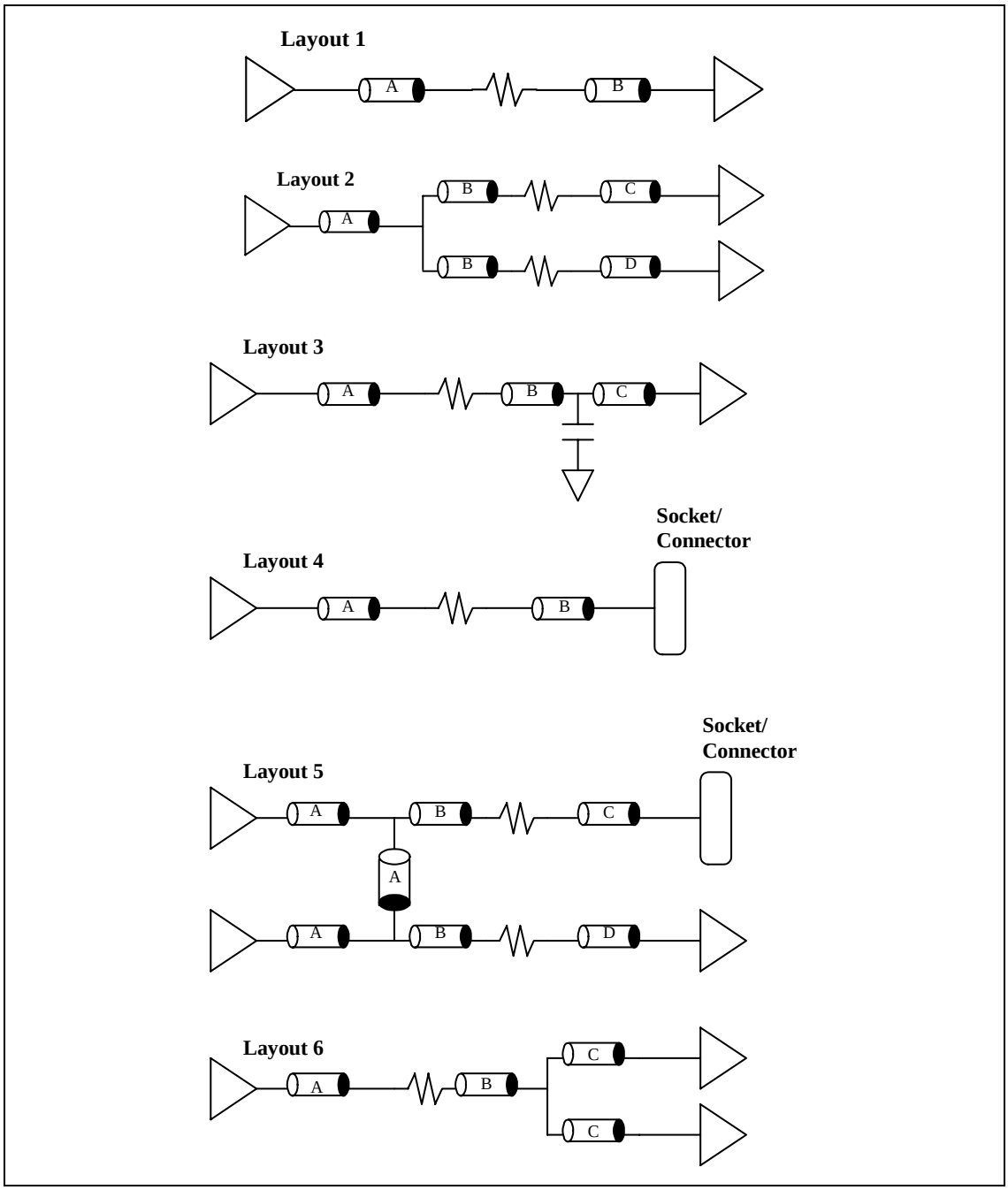
### Table 39. Layout Dimensions

| Group | Receiver | Resistor | Cap | Topology | A | B | C | D |
|---|---|---|---|---|---|---|---|---|
| MCLK | DIMM | 22 Ω | N/A | Layout 1 | 0.5” | X | N/A | N/A |
| Processor Intel® Pentium® III FC-PGA Processor 100/133 MHz | Segment C => Pentium III FC-PGA Processor<br>Segment D => GMCH | 33 Ω | N/A | Layout 5 | 0.1” | 0.5” | X+4.8" | X+7.1” |
| Processor Intel® Celeron® Processor 66/100 MHz | Segment C => Celeron Processor Socket<br>Segment D => GMCH | 33 Ω | N/A | Layout 5 | 0.1” | 0.5” | X+5.4" | X+7.1” |
| DCLK | GMCH | 33 Ω | 22 pF | Layout 3 | 0.5” | X+3.2” | 0.5” | N/A |
| 3V66 | GMCH | 22 Ω | 18 pF | Layout 3 | 0.5” | X+1.4” | 0.5” | N/A |
| 3V66 | ICH2 | 22 Ω | 18 pF | Layout 3 | 0.5” | X+1.4” | 0.5” | N/A |
| PCI | PCI device | 33 Ω | N/A | Layout 1 | 0.5” | X+3.0” to X+9.3” | N/A | N/A |
| PCI | PCI socket | 33 Ω | N/A | Layout 4 | 0.5” | X+0.0” to X+6.0” | N/A | N/A |
| PCI | ICH2 | 33 Ω | N/A | Layout 1 | 0.5” | X+4.4” | N/A | N/A |
| TCLK | SDRAM | 22 Ω | N/A | Layout 6 | 0.5” | 1.5” to 2.5” | 0.75” to 1.25” | N/A |
| OCLK/RCLK | GMCH | 33 Ω | N/A | Layout 1 | 0.5” | 3.25” to 3.75” | N/A | N/A |
| APIC | PPGA | 33 Ω | N/A | Layout 4 | 0.5” | Y | N/A | N/A |
| APIC | ICH2 | 33 Ω | N/A | Layout 1 | 0.5” | Y+2.4” | N/A | N/A |

**NOTES:**
1. W, X, Y and Z trace lengths are arbitrary. Below are some suggested values: X=5.0", Y=4.2".

The following figure shows the different topologies used for the clock routing guidelines.

**Figure 81. Different Topologies for the Clock Routing Guidelines**

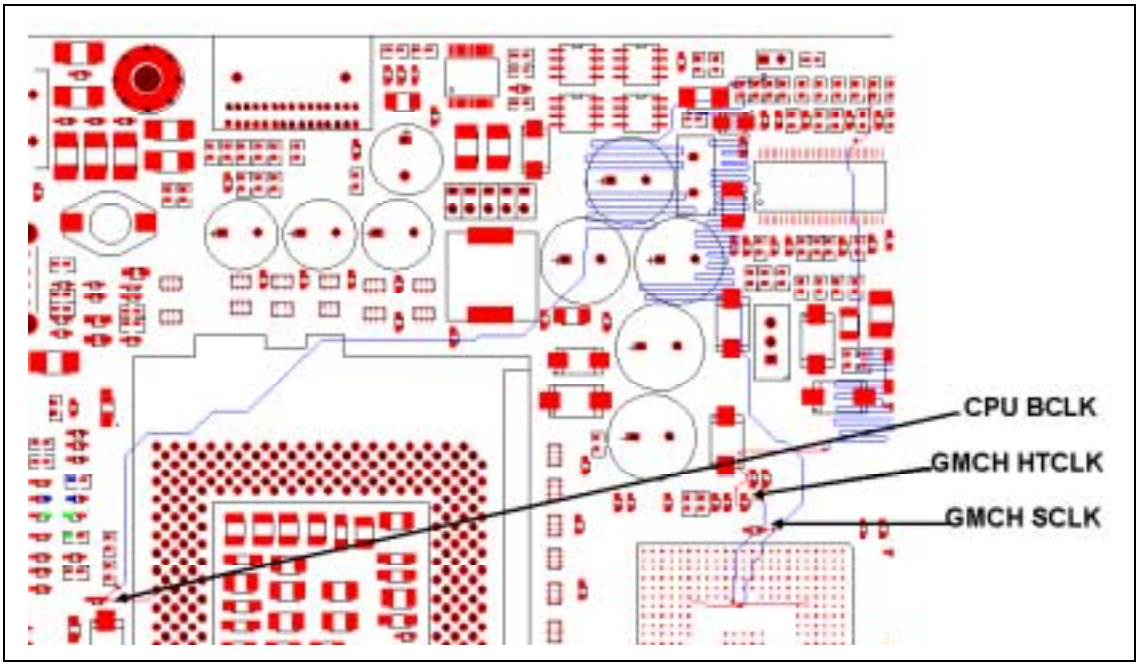


## 5.4. Capacitor Sites

Intel recommends 0603 package capacitor sites placed as close as possible to the clock input receivers for AC tuning for the following signal groups:

- GMCH
- Processor
- SDRAM/DCLK
- 3V66
- 3V66 to the ICH2

**Figure 82. Example of Capacitor Placement Near Clock Input Receiver**



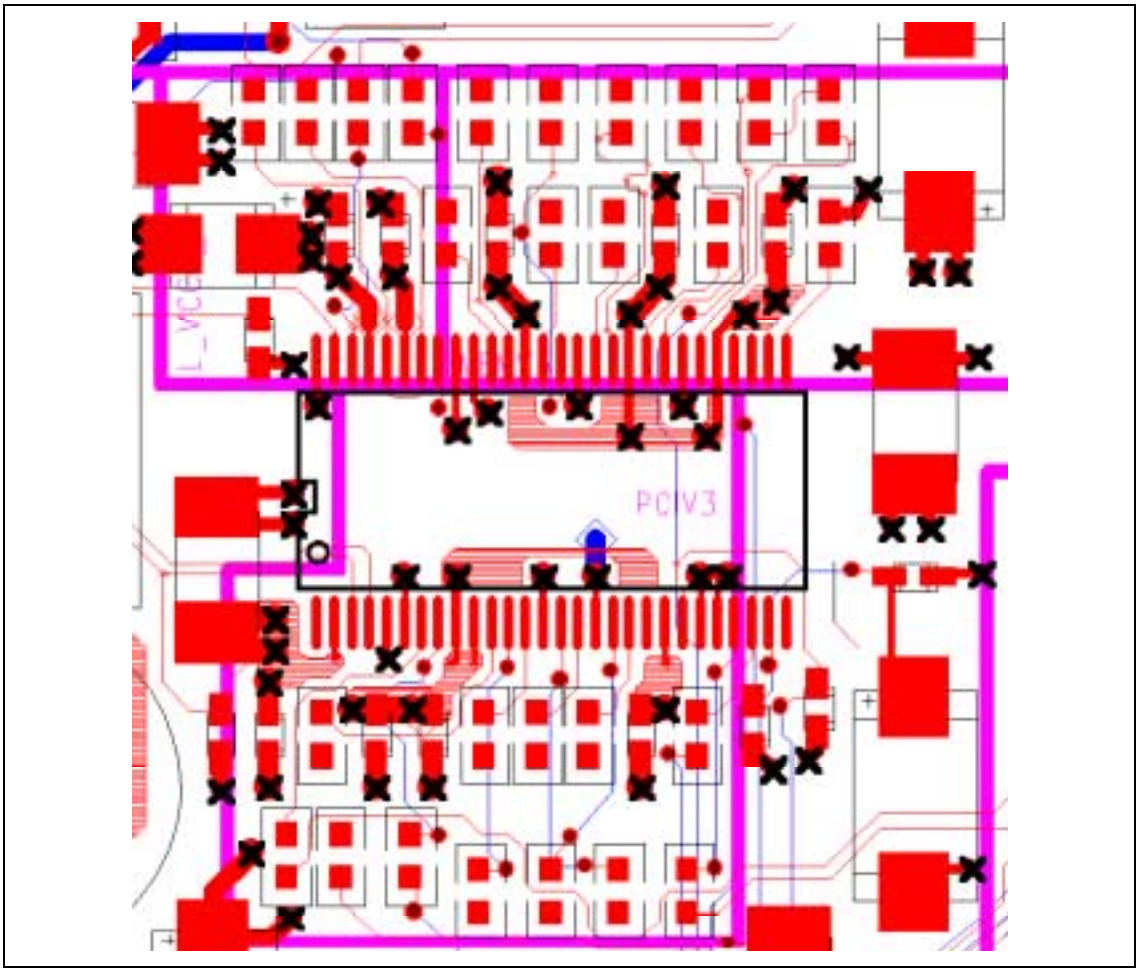
## 5.5. Clock Power Decoupling Guidelines

Several general layout guidelines should be followed when laying out the power planes for the CK810E clock generator.

- Isolate power planes to the each of the clock groups.
- Place local decoupling as close to power pins as possible and connect with short, wide traces and copper.
- Connect pins to appropriate power plane with power vias (larger than signal vias).
- Bulk decoupling should be connected to plane with 2 or more power vias.
- Minimize clock signal routing over plane splits.
- Do not route any signals underneath the clock generator on the component side of the board.
- An example signal via is a 14 mil finished hole with a 24–26 mil path. An example power via is an 18 mil finished hole with a 33–38 mil path. For large decoupling or power planes with large current transients it is recommended to use a larger power via.

An example of clock power layout is presented in the following figure.

**Figure 83. Example of Clock Power Plane Splits and Decoupling**



## 5.6. Clock Skew Requirements

To ensure correct system functionality, certain clocks must maintain a skew relationship to other clocks as summarized in the following section.

### 5.6.1. IntraGroup Skew Limits

Clocks within each group must maintain appropriate skew relationship to each other. These requirements are summarized in the following table.

**Table 40. Clock Skew Requirements**

| Group Pair | Skew Limit | Measurement Point of Receiver |
|---|---|---|
| Processor BCLK to GMCH HTCLK | 350 pS window | Pin on top of PPGA PKG GMCH Ball |
| GMCH SCLK to DIMM Clocks | ±630 pS Referenced to GMCH SCLK | GMCH Ball DRAM Component Pin on Module |
| GMCH HubCLK to ICH2 HubCLK | 575 pS window | GMCH Ball ICH Ball |

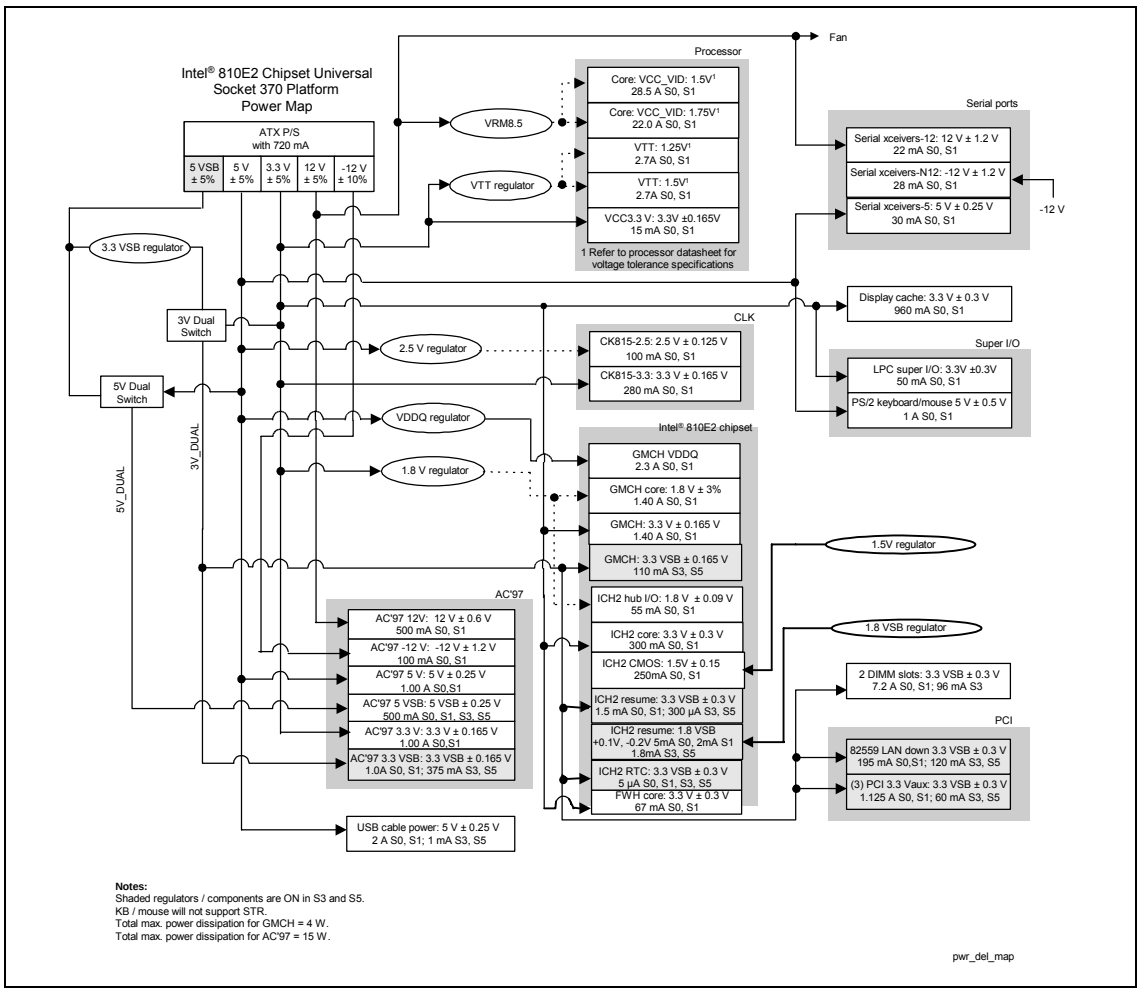
# 6. Power Delivery

The following figure shows the power delivery architecture for an example 810E2 chipset platform. This power delivery architecture supports the “Instantly Available PC Design Guidelines” via the *suspend-to-RAM* (STR) state.

During STR, only the necessary devices are powered. These devices include: main memory, the ICH2 resume well, PCI wake devices (via 3.3 Vaux), AC’97, and optionally USB. (USB can be powered only if sufficient standby power is available.) To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device’s power requirements, both in *suspend* and in *full-power*. The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a *dual* power rail.

The solutions in this Design Guide are only examples. Many power distribution methods achieve the similar results. When deviating from these examples, it is critical to consider the effect of a change.

**Figure 84. Power Delivery Map**




# 6.1. Thermal Design Power

Thermal Design power (TDP) is defined as the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus.

The TDP for the GMCH component is 4.0 W.

The TDP for the ICH2 is 1.5 W.

## 6.1.1. Power Sequencing

This section shows the timings between various signals during different power state transitions.

**Figure 85. G3-S0 Transistion**

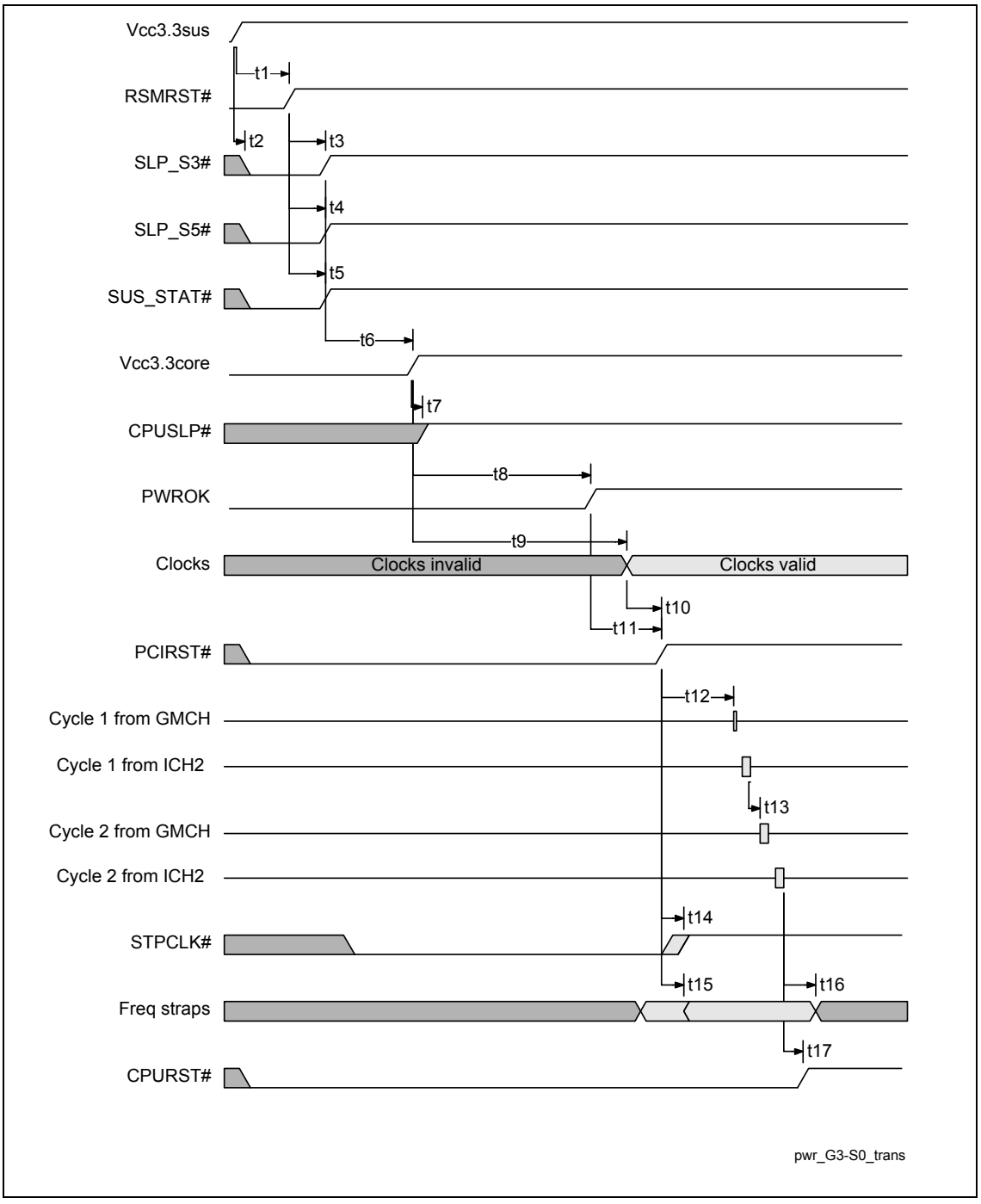


**Figure 86. S0-S3-S0 Transition**

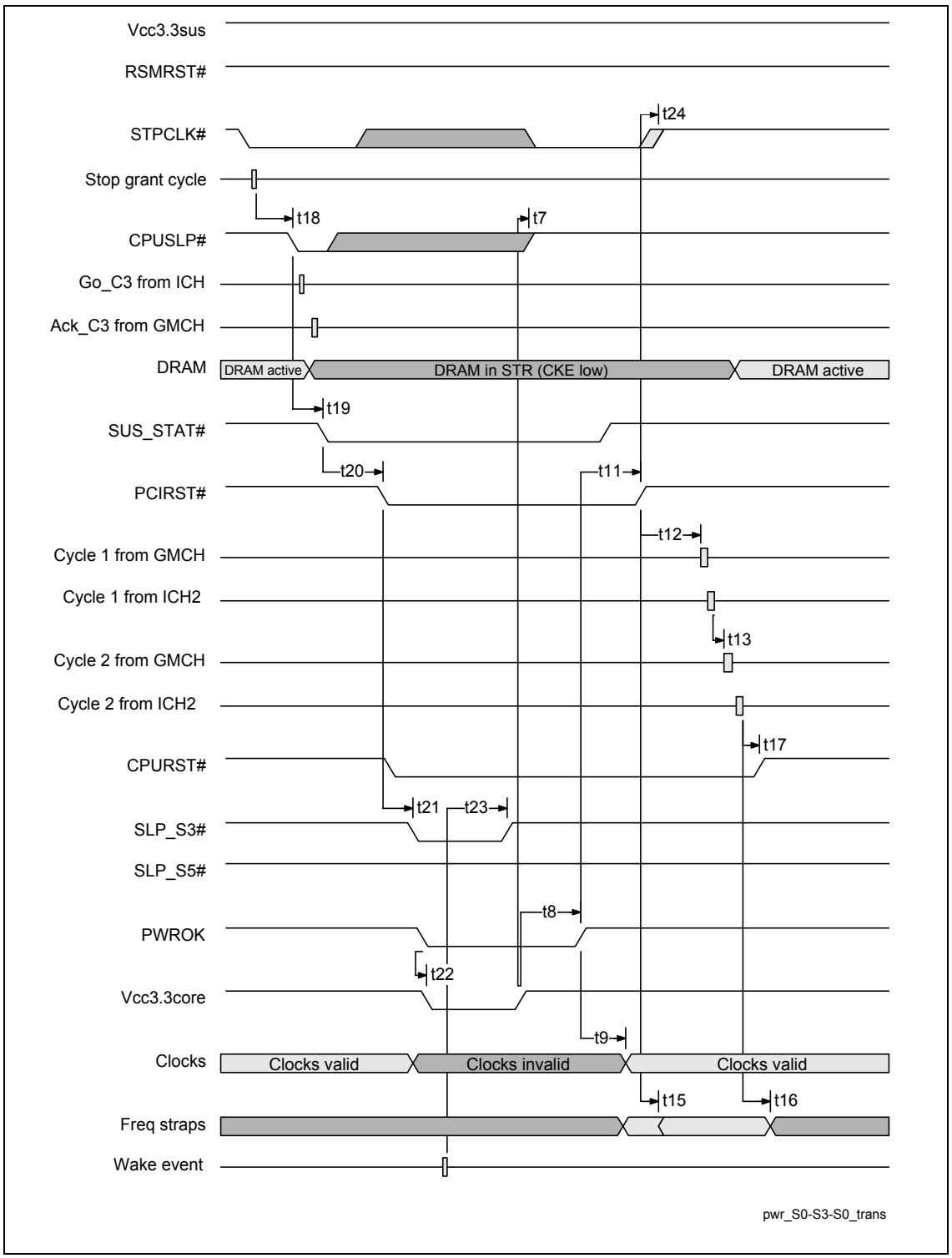
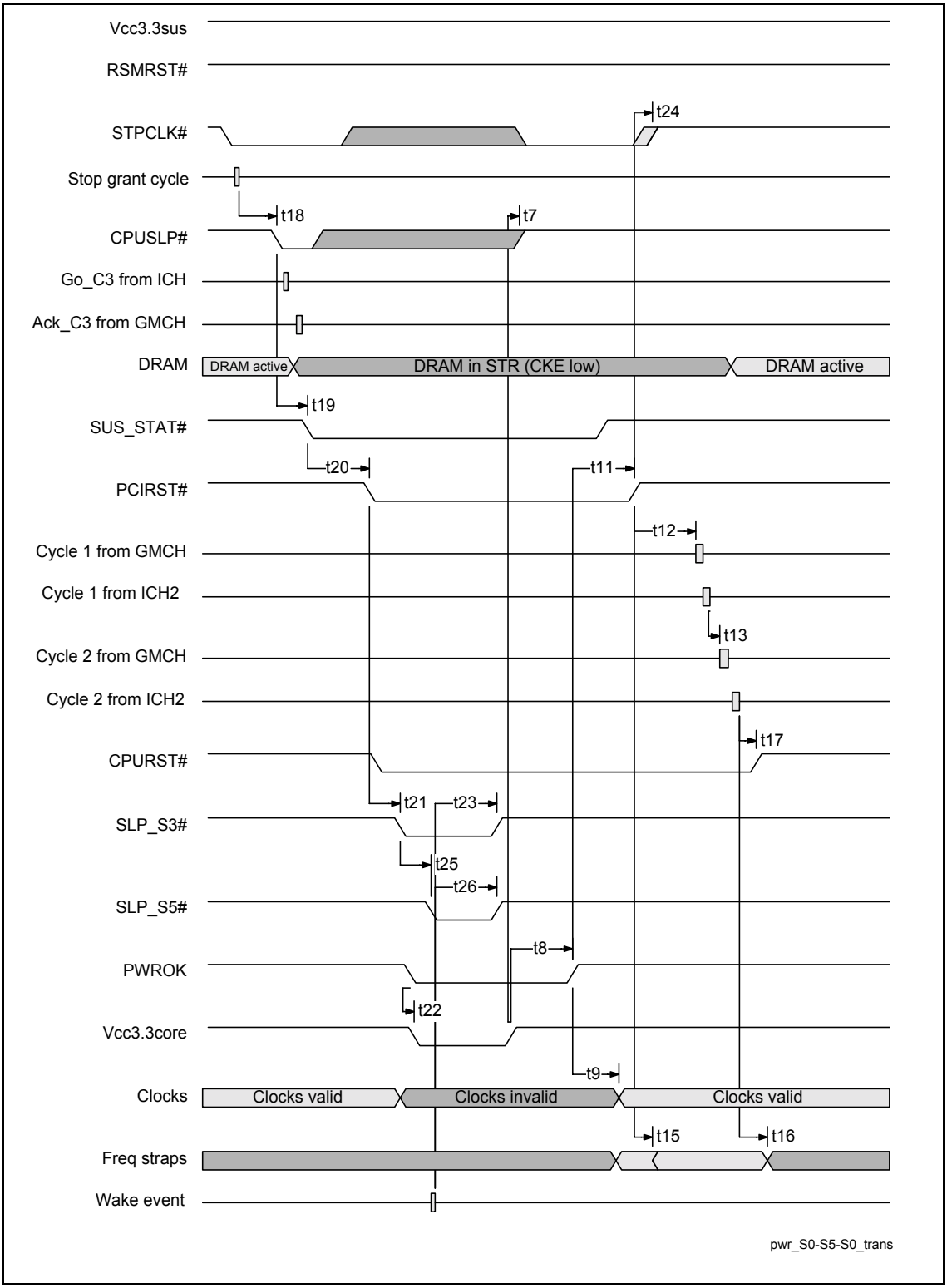


**Figure 87. S0-S5-S0 Transition**



### Table 41. Power Sequencing Timing Definitions

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| t1 | VccSUS good to RSMRST# inactive | 1 | 25 | ms |
| t2 | VccSUS good to SLP_S3#, SLP_S5#, and PCIRST# active | | 50 | ns |
| t3 | RSMRST# inactive to SLP_S3# inactive | 1 | 4 | RTC clocks |
| t4 | RSMRST# inactive to SLP_S5# inactive | 1 | 4 | RTC clocks |
| t5 | RSMRST# inactive to SUS_STAT# inactive | 1 | 4 | RTC clocks |
| t6 | SLP_S3#, SLP_S5#, SUS_STAT# inactive to Vcc3.3core good | * | * | |
| t7 | Vcc3.3core good to CPUSLP# inactive | | 50 | ns |
| t8 | Vcc3.3core good to PWROK active | * | * | |
| t9 | Vcc3.3core good to clocks valid | * | * | |
| t10 | Clocks valid to PCIRST# inactive | 500 | | µs |
| t11 | PWROK active to PCIRST# inactive | .9 | 1.1 | ms |
| t12 | PCIRST# inactive to cycle 1 from GMCH | | 1 | ms |
| t13 | Cycle 1 from ICH2 to cycle 2 from GMCH | | 60 | ns |
| t14 | PCIRST# inactive to STPCLK de-assertion | 1 | 4 | PCI clocks |
| t15 | PCIRST# to frequency straps valid | -4 | 4 | PCI clocks |
| t16 | Cycle 2 from ICH2 to frequency straps invalid | | 180 | ns |
| t17 | Cycle 2 from ICH2 to CPURST# inactive | | 110 | ns |
| t18 | Stop Grant Cycle to CPUSLP# active | | 8 | PCI clocks |
| t19 | CPUSLP# active to SUS_STAT# active | | 1 | RTC clock |
| t20 | SUS_STAT# active to PCIRST# active | 2 | 3 | RTC clocks |
| t21 | PCIRST# active to SLP_S3# active | 1 | 2 | RTC clocks |
| t22 | PWROK inactive to Vcc3.3core not good | 20 | | ns |
| t23 | Wake event to SLP_S3# inactive | 2 | 3 | RTC clocks |
| t24 | PCIRST# inactive to STPCLK# inactive | 1 | 4 | PCI clocks |
| t25 | SLP_S3# active to SLP_S5# active | 1 | 2 | RTC clocks |
| t26 | SLP_S5# inactive to SLP_S3# inactive | 2 | 3 | RTC clocks |

## 6.2. Pull-up and Pull-down Resistor Values

The pull-up and pull-down values are system dependent. The appropriate value for a system can be determined from an AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, the input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high-voltage/low-voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be performed to determine the minimum/maximum values usable on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications, and other considerations.

A simplistic DC calculation for a pull-up value is:

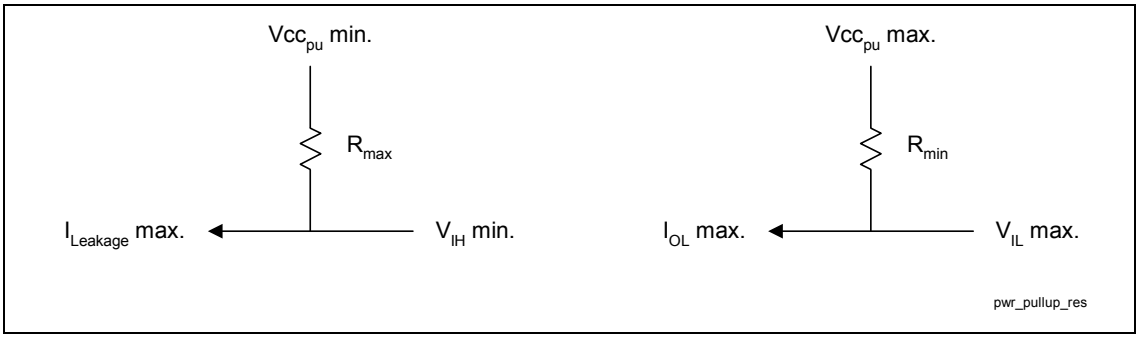
$$R_{MAX} = (Vcc_{PU}\ MIN - V_{IH}\ MIN) / I_{LEAKAGE}\ MAX$$

$$R_{MIN} = (Vcc_{PU}\ MAX - V_{IL}\ MAX) / I_{OL}\ MAX$$

Since $I_{LEAKAGE}$ MAX is normally very small, $R_{MAX}$ may not be meaningful. $R_{MAX}$ also is determined by the maximum allowable rise time. The following calculation allows for t, the maximum allowable rise time, and C, the total load capacitance in the circuit, including the input capacitance of the devices to be driven, the output capacitance of the driver, and the line capacitance. This calculation yields the largest pull-up resistor allowable to meet the rise time t.

$$R_{MAX} = -t / (C * \ln(1-(V_{IH}\ MIN / Vcc_{PU}\ MIN)))$$

**Figure 88. Pull-up Resistor Example**



## 6.3. ATX Power Supply PWRGOOD Requirements

The PWROK signal must be glitch free for proper power management operation. The ICH2 sets the PWROK_FLR bit (ICH2 GEN_PMCON_2, General PM Configuration 2 Register, PM-dev31: function 0, bit 0, at offset A2h). If this bit is set upon resume from S3 power-down, the system will reboot and control of the system will not be given to the program running when entering the S3 state. System designers should insure that PWROK signal designs are glitch free.

## 6.4. Power Management Signals

- A power button is required by the ACPI specification.
- PWRBTN# is connected to the front panel on/off power button. The ICH2 integrates 16-ms debouncing logic on this pin.
- AC power loss circuitry has been integrated into the ICH2 to detect power failure.
- It is recommended that the PS_POK signal from the power supply connector be routed through a Schmitt trigger to square-off and maintain its signal integrity. It should not be connected directly to logic on the board.
- PS_POK logic from the power supply connector can be powered from the core voltage supply.
- RSMRST# logic should be powered by a standby supply, while making sure that the input to the ICH2 is at the 3-Volt level. The RSMST# signal requires a minimum time delay of 1 ms from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1-ms delay should be placed before the Schmitt trigger circuit. The reference design implements a 20-ms delay at the input of the Schmitt trigger to ensure that the Schmitt trigger inverters have sufficiently powered up before switching the input. Also ensure that voltage on RSMRST# does not exceed VCC(RTC).
- It is recommended that 3.3-Volt logic be used to drive RSMRST# to alleviate rise time problems when using a resistor divider from VCC5.
- The PWROK signal to the chipset is a 3-Volt signal.
- The core well power valid to PWROK asserted at the chipset is a minimum of 1 ms.
- PWROK to the chipset must be deasserted after RSMRST#.
- PWRGOOD signal to processor is driven with an open-collector buffer pulled up to 2.5 V, using a 330-Ω resistor.
- RI# can be connected to the serial port if this feature is used. To implement ring indicate as a wake event, the RS232 transceiver driving the RI# signal must be powered when the ICH2 suspend well is powered. This can be achieved with a serial port transceiver powered from the standby well that implements a shutdown feature.
- SLP_S3# from the ICH2 must be inverted and then connected to PSON of the power supply connector to control the state of the core well during sleep states.
- For an ATX power supply, when PSON is low, the core wells are turned on. When PSON is high, the core wells from the power supply are turned off.

## 6.4.1. Power Button Implementation

The following items should be considered when implementing a power management model for a desktop system. The power states are as follows:

S1 – Stop Grant – (processor context not lost)

S3 – STR (Suspend to RAM)

S4 – STD (Suspend to Disk)

S5 – Soft-off

- Wake: Pressing the power button wakes the computer from S1–S5.
- Sleep: Pressing the power button signals software/firmware in the following manner:
- If SCI is enabled, the power button will generate an SCI to the OS.
  - The OS will implement the power button policy to allow orderly shutdowns.
  - Do not override this with additional hardware.
- If SCI is not enabled:
  - Enable the power button to generate an SMI and go directly to soft-off or a supported sleep state.
  - Poll the power button status bit during POST while SMIs are not loaded and go directly to soft-off if it gets set.
  - Always install an SMI handler for the power button that operates until ACPI is enabled.
- Emergency Override: Pressing the power button for 4 seconds goes directly to S5.
  - This is only to be used in EMERGENCIES when the system is not responding.
  - This will cause the user data to be lost in most cases.
- Do not promote pressing the power button for 4 seconds as the normal mechanism to power the machine off. This violates ACPI.
- To be compliant with the latest PC9x specification, machines must appear to the user to be off when in the S1–S4 sleeping states. This includes:
  - All lights, except a power state light, must be off.
  - The system must be inaudible: silent or stopped fan, drives off.
- Note: Contact Microsoft* for the latest information concerning PC9x and Microsoft* Logo programs.

## 6.4.2. 1.8V / 3.3V Power Sequencing

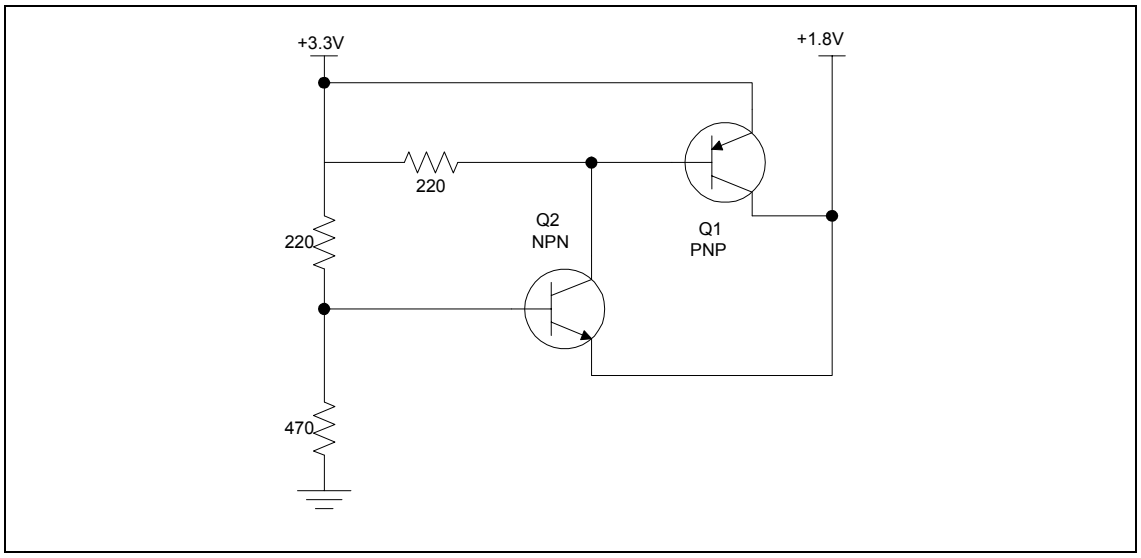
The ICH2 has two pairs of associated 1.8V and 3.3V supplies. These are (Vcc1_8, Vcc3_3) and (VccSus1_8, VccSus3_3). These pairs are assumed to power up and power down together. **The difference between the two associated supplies must never be greater than 2.0V.** The 1.8V supply may come up before the 3.3V supply without violating this rule (though this is generally not practical in a desktop environment, since the 1.8V supply is typically derived from the 3.3V supply by means of a linear regulator).

One serious consequence of violation of this "2V Rule" is electrical overstress of oxide layers, resulting in component damage.

The majority of the ICH2 I/O buffers are driven by the 3.3V supplies, but are controlled by logic that is powered by the 1.8V supplies. Thus, another consequence of faulty power sequencing arises if the 3.3V supply comes up first. In this case the I/O buffers will be in an undefined state until the 1.8V logic is powered up. Some signals that are defined as "Input-only" actually have output buffers that are normally disabled; the ICH2 may unexpectedly drive these signals if the 3.3V supply is active while the 1.8V supply is not.

The figure below shows an example power-on sequencing circuit that ensures the “2V Rule” is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.8V supply tracks the 3.3V supply. The NPN transistor controls the current through PNP from the 3.3V supply into the 1.8V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8V plane, current will not flow from the 3.3V supply into 1.8V plane when the 1.8V plane reaches 1.8V.

**Figure 89. Example 1.8V/3.3V Power Sequencing Circuit**




When analyzing systems that may be "marginally compliant" to the 2V Rule, please pay close attention to the behavior of the ICH2's RSMRST# and PWROK signals, since these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the Resume wells.
- PWROK controls isolation between the Resume wells and Main wells

If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

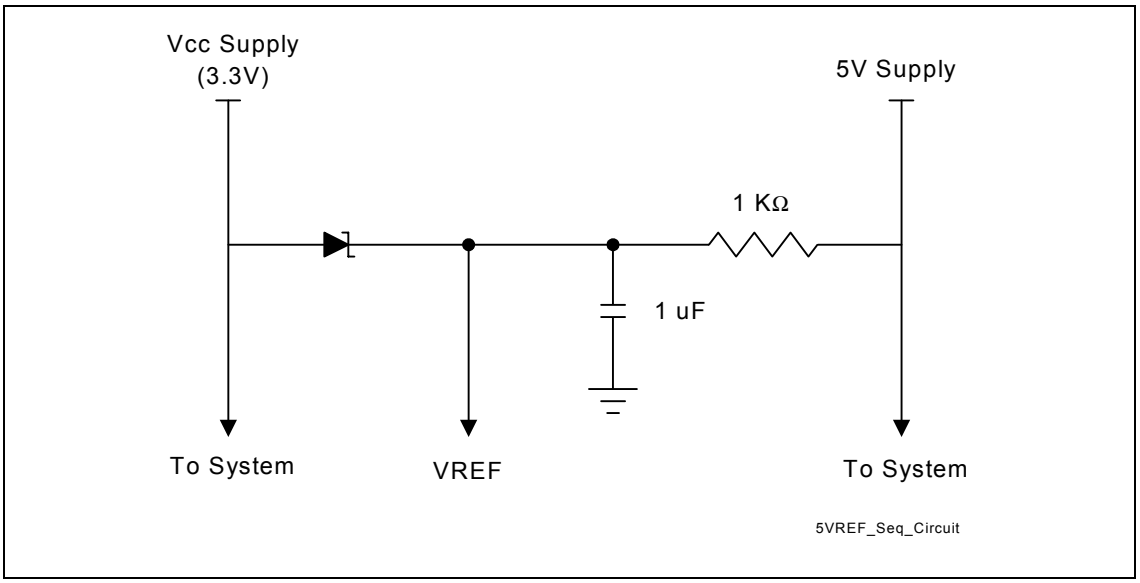
## 6.4.3. 3.3V / V5REF Sequencing

V5REF is the reference voltage for 5V tolerance on inputs to the ICH2. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within .7V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within .7V. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 87 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

This rule also applies to the stand-by rails. However, in most platforms the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend, the only signals that are 5V tolerant capable are USB OC:[3:0]#. If these signals are not needed during suspend, V5REF_SUS can be connected to either VccSus3_3 or 5V_Always/5V_AUX. If OC:[3:0]# is needed during suspend and 5V tolerance is required then V5REF_SUS should be connected to 5V_Always/5V_AUX, but if 5V tolerance is not needed in suspend, then V5REF_SUS can be connected to either VccSus3_3 or 5V_Always/5V_AUX rails.

**Figure 90. Example 3.3V/V5REF Sequencing Circuitry**



## 6.4.4. GMCH Decoupling Guidelines

### GMCH Vsus 3.3V (3.3V Standby) Power Plane Decoupling

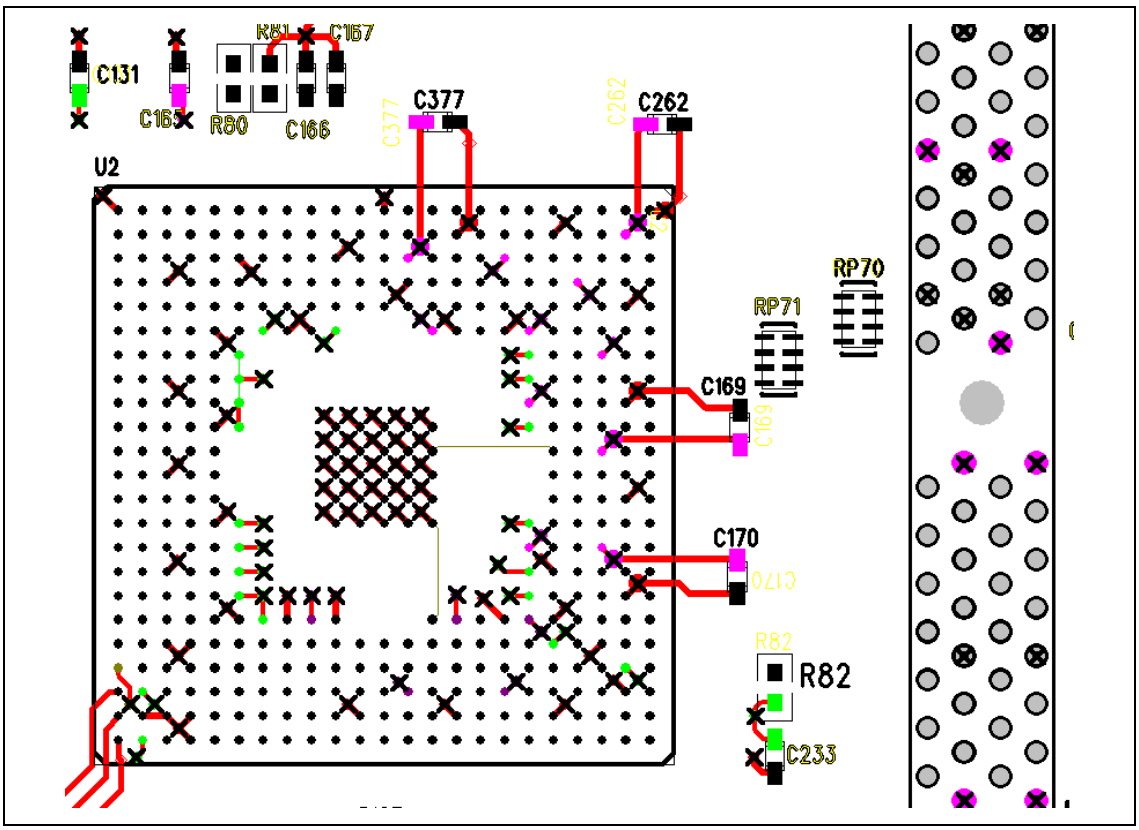
The use of top-side (component side) capacitors near the GMCH (as shown in the following "GMCH Power Plane Decoupling" figure) as the only means of decoupling the VSUS_3.3V power plane may be insufficient to meet the 3.3V droop specification or to attenuate noise. In some cases bottom-side (solder side) capacitors (connected at three to four of the VSUS_3.3V signal balls to the nearest VSS balls) may be required to comply with the droop specification and improve noise protection. This is important in platforms where 100 MHz or 133 MHz SDRAM interface is used.

- 3.3V Droop Specification
  - Worse case droop on 3.3V plane must not go below 2.5 V.
  - *Droop below the minimum Vcc of 3.135 V must not occur for a period greater than 2 ns.*
- Place four 0.01 µF decoupling capacitors as close as possible to the GMCH.
  - Trace from cap pad to via < 500 mils (Ideal = 300 mils).
  - Trace width at least 15 mils.
- Use power vias (multiple if possible).
  - Power via example: 18 mil drill, 33–38 mil width.
- Place capacitors orientation such that flight time will be minimized.
  - Vias between GMCH ball and cap pad (see following figure).

### Power Plane Layout

- Make the power planes as square as possible with no sharp corners.
- Avoid crossing traces over multiple power planes.

Figure 91. GMCH Power Plane Decoupling




## 6.4.5. Ground Flood Planes

To further decouple the 82810E GMCH and provide a solid current return path for the system memory interface signals, it is recommended that 4-layer boards (signal-power-ground-signal) be designed with a topside (device side) ground flood plane under the GMCH. This topside copper flood plane under the center of the GMCH creates a parallel plate capacitor between the power layer and GND. This topside ground flood plane reduces the inductive trace/via path to the ground layer by acting as a ground itself. The top-side ground flood plane adds board plane decoupling to the power layer (1.8V and 3.3V) directly underneath it. This added board plane decoupling is significant – typically 25 pF/sq.inch without the ground flood plane vs. 225 pF/sq.inch with the ground flood plane. The added board plane decoupling has a much wider frequency spectrum (100 MHz – 1 GHz+) with a sustained low series resistance in that range compared to power plane decoupling capacitors alone. Tying the pads of these power plane decoupling capacitors to the ground flood plane reduces trace inductance into these capacitors and provides improved decoupling.

## 6.5. Power_Supply PS_ON Considerations

If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10-100mS) such that PS_ON is driven active during the exponential decay of the power rails, a few power supplies may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

The platform designer must ensure that the power supply used with the platform is not affected by this issue.

# 7. Design Checklist

## 7.1. Design Review Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements an 810E2 chipset. This is not a complete list and does not guarantee that a design will function properly. Beyond the items contained in the following text, refer to the most recent version of the Design Guide for more detailed instructions on designing a motherboard.

### 7.1.1. Design Checklist Summary

The following tables provide design considerations for the various portions of a design. Each table describes one of those portions, and is titled accordingly. Contact your Intel Field Representative for questions or issues regarding interpretation of the information contained in these tables.

### Table 42. AGTL+ Connectivity Checklist for 370-Pin Socket Processors

| Processor Pin | I/O | Recommendations |
|---|---|---|
| A[35:3]# 1 | I/O | Connect A[31:3]# to GMCH. Leave A[35:32]# as No Connect (not supported by chipset). |
| ADS# 1 | I/O | Connect to GMCH. |
| AERR# | I/O | Leave as No Connect (not supported by chipset). |
| AP[1:0]# | I/O | Leave as No Connect (not supported by chipset). |
| BERR# | I/O | Leave as No Connect (not supported by chipset). |
| BINIT# | I/O | Leave as No Connect (not supported by chipset). |
| BNR# 1 | I/O | Connect to GMCH. |
| BP[3:2]# | I/O | Leave as No Connect. |
| BPM[1:0] | I/O | Leave as No Connect. |
| BPRI# 1 | I | Connect to GMCH. |
| BREQ[0]# (BR0#) | I/O | 10 Ω pull-down resistor to ground. |
| D[63:0]# 1 | I/O | Connect to GMCH. |
| DBSY# 1 | I/O | Connect to GMCH. |
| DEFER# 1 | I | Connect to GMCH. |
| DEP[7:0]# | I/O | Leave as No Connect (not supported by chipset). |
| DRDY# 1 | I/O | Connect to GMCH. |
| HIT# 1 | I/O | Connect to GMCH. |
| HITM# 1 | I/O | Connect to GMCH. |
| LOCK# 1 | I/O | Connect to GMCH. |
| REQ[4:0]# 1 | I/O | Connect to GMCH. |
| RESET# | I | 56 Ω pull-up resistor to Vtt, connect to GMCH, 240 Ω series resistor to ITP. |
| RESET2# 2 | I | Driven by same signal as RESET#. |
| RP# | I/O | Leave as No Connect (not supported by chipset). |
| RS[2:0]# | I | Connect to GMCH. |
| RSP# | I | Leave as No Connect (not supported by chipset). |
| TRDY# 1 | I | Connect to GMCH. |

**NOTES:**

1. For Celeron (PPGA package, CPUID=0665) processor electrical compatibility, the motherboard must include AGTL+ termination resistors. If the Celeron processor is not supported, AGTL+ termination is provided by the Pentium III processor (**except RESET**#).
2. If the Celeron processor is not supported by the motherboard, then RTTCTRL is pulled down with a 56 Ω resistor and RESET2# is grounded.

### Table 43. CMOS Connectivity Checklist for 370-Pin Socket Processors

| Processor Pin | I/O | Recommendations |
|---|---|---|
| A20M# | I | Connect to ICH2. |
| FERR# | O | 150 Ω pull-up resistor to $VCC_{CMOS}$ / Connect to ICH2. |
| FLUSH# | I | 150 Ω pull-up resistor to $VCC_{CMOS}$ (not used by chipset). |
| IERR# | O | 150 Ω pull-up resistor to $VCC_{CMOS}$ if tied to custom logic or leave as No Connect (not used by chipset). |
| IGNNE# | I | Connect to ICH2. |
| INIT# | I | Connect to ICH2 & FWH Flash BIOS. |
| LINT0/INTR | I | Connect to ICH2. |
| LINT1/NMI | I | Connect to ICH2. |
| PICD[1:0] | I/O | 150 Ω pull-up resistor to $VCC_{CMOS}$ / Connect to ICH2. |
| PREQ# | O | ~200–330 Ω pull-up resistor to $VCC_{CMOS}$ / Connect to ITP. |
| PWRGOOD | I | 150–330 Ω pull-up to 2.5V, output from the PWRGOOD logic. |
| SLP# | I | Connect to ICH2. |
| SMI# | I | Connect to ICH2. |
| STPCLK# | I | Connect to ICH2. |
| THERMTRIP# | O | 150 Ω pull-up resistor to $VCC_{CMOS}$ and connect to power off logic, or leave as No Connect. |

### Table 44. TAP Checklist for a 370-Pin Socket Processor

| Processor Pin | I/O | Recommendations |
|---|---|---|
| TCK | I | 1 kΩ pull-up resistor to $VCC_{CMOS}$ / 47 Ω series resistor to ITP. |
| TDI | I | ~200–330 Ω pull-up resistor to $VCC_{CMOS}$ / Connect to ITP. |
| TDO | O | 150 Ω pull-up resistor to $VCC_{CMOS}$ / Connect to ITP. |
| TMS | I | 1 kΩ pull-up resistor to $VCC_{CMOS}$ / 47 Ω series resistor to ITP. |
| TRST# | I | ~680 Ω pull-down resistor to ground / Connect to ITP. |
| PRDY# | I | 150 Ω pull-up resistor to Vtt / 240 Ω series resistor to ITP. |

**NOTES:**

1. The ITP connector is different than the one previously specified for other Intel IA-32 processors. It is the female counterpart to the previously specified connector and is specifically for use with processors utilizing 1.5V CMOS TAP I/O signals.
2. The Pentium® III processor requires an ITP with a 1.5V tolerant buffer board. Previous ITPs are designed to work higher voltages and may damage the processor if they are connected to an Pentium III processor.

### Table 45. Miscellaneous Checklist for 370-Pin Socket Processors

| Processor Pin | I/O | Recommendations |
|---|---|---|
| BCLK | I | Connect to clock generator / 22–33 Ω series resistor (though OEM needs to simulate based on driver characteristics). To reduce pin-to-pin skew, tie host clock outputs together at the clock driver then route to the GMCH and processor. |
| BSEL0 | I/O | **Case 1, 66/100/133 MHz support:** 1 kΩ pull-up resistor to 3.3V, connect to CK810E SEL0 input, connect to GMCH LMD29 pin via 10 kΩ series resistor.<br>**Case 2, 100/133 MHz support:** 1 kΩ pull-up resistor to 3.3V, connect to PWRGOOD logic such that a logic low on BSEL0 negates PWRGOOD. |
| BSEL1 | I/O | 1 kΩ pull-up resistor to 3.3V, connect to CK810E REF pin via 10 kΩ series resistor, connect to GMCH LMD13 pin via 10 kΩ series resistor. |
| CLKREF | I | Connect to divider on VCC_2.5 or VCC_3.3 to create 1.25V reference with a 4.7 µF decoupling capacitor. Resistor divider must be created from 1% tolerance resistors. **Do not use VTT as source voltage for this reference!** |
| CPUPRES# | | Tie to ground, leave as No Connect, or could be connected to PWRGOOD logic to gate system from powering on if no processor is present. If used, 1 kΩ–10 kΩ pull-up resistor to any voltage. |
| EDGCTRL | I | 51 Ω ±5% pull-up resistor to $VCC_{CORE}$. |
| PICCLK | I | Connect to clock generator / 22–33 Ω series resistor (though OEM needs to simulate based on driver characteristics). |
| PLL1, PLL2 | I | Low pass filter on $VCC_{CORE}$ provided on motherboard. Typically a 4.7 uH inductor in series with $VCC_{CORE}$ is connected to PLL1 then through a series 33 µF capacitor to PLL2. |
| RTTCTRL5 (S35) | | 110 Ω ±1% pull-down resistor to ground. |
| SLEWCTRL (E27) | | 110 Ω ±1% pull-down resistor to ground. |
| THERMDN | O | No Connect if not used; otherwise connect to thermal sensor using vendor guidelines. |
| THERMDP | I | No Connect if not used; otherwise connect to thermal sensor using vendor guidelines. |
| VCC_1.5 | I | Connected to same voltage source as $V_{TT}$. Must have some high and low frequency decoupling. |
| VCC_2.5 | I | Connected to 2.5V voltage source. Should have some high and low frequency decoupling. |
| $VCC_{CMOS}$ | O | Used as pull-up voltage source for CMOS signals between processor and chipset and for TAP signals between processor and ITP. Must have some decoupling (HF/ LF) present. |
| $VCC_{CORE}$ | I | 10 ea (min) 4.7 µF in 1206 package all placed within the PGA370 socket cavity.<br>8 ea (min) 1 µF in 0612 package placed in the PGA370 socket cavity. |
| $VCORE_{DET}$ (E21) | O | 220 Ω pull-up resistor to 3.3V, connect to GMCH LMD27 pin via 10 kΩ series resistor for the Celeron® processor and Pentium® II processor.<br>For the Celeron processor and Pentium® III processor VCOREdet must float. |
| VID[3:0] | O | Connect to on-board VR or VRM. For on-board VR, 10 kΩ pull-up resistor to power-solution compatible voltage required (usually pulled up to input voltage of the VR). Some of these solutions have internal pull-ups. Optional override (jumpers, ASIC, etc.) could be used. May also connect to system monitoring device. |
| VID[4] | N/A | Connect regulator controller pin to ground (not on processor). |

| Processor Pin | I/O | Recommendations |
|---|---|---|
| VREF[7:0] | I | Connect to Vref voltage divider made up of 75 and 150 Ω 1% resistors connected to Vtt.<br>Decoupling Guidelines:<br>4 ea. (min) 0.1 µF in 0603 package placed within 500 mils of VREF pins. |
| VTT | I | Connect AH20, AK16, AL13, AL21, AN11, AN15, and G35 to 1.5V regulator. Provide high and low frequency decoupling.<br>Decoupling Guidelines:<br>19 ea (min) 0.1 µF in 0603 package placed within 200 mils of AGTL+ termination resistor packs (r-paks). Use one capacitor for every two (r-paks).<br>4 ea (min) 0.47 µF in 0612 package |
| Additional VTT | I | AA33, AA35, AN21, E23, S33, S37, U35, U37 |
| GND | N/A | AJ3 |
| NO CONNECTS | N/A | The following pins must be left as no-connects: AK30, AM2, F10, G37, L33, N33, N35, N37, Q33, Q35, Q37, R2, W35, X2, Y1 |

**NOTES:**
1. If the Celeron processor (CPUID = 0665) is not supported by the motherboard, then RTTCTRL is pulled down with a 56 Ω resistor and RESET2# is grounded.

### Table 46. GMCH Checklist

| Checklist Line Items | Comments |
|---|---|
| VCCDA | VCCDA needs to be connected to an isolated power plane. |
| HCLK, SCLK | 22 pF cap to ground as close as possible to GMCH. |
| GTLREFA, GTLREFB | Refer to the latest design guide for the correct GTLREF generation circuit. |
| HUBREF | Refer to the latest design guide for the correct HUBREF generation circuit. Also, place a 0.1 µF cap as close as possible to GMCH to ground. |
| IWASTE | Tie to ground. |
| IREF | Place a resistor as close as possible to GMCH and via straight to VSS plane. A 174 Ω 1% resistor is recommended. |
| LTVCL, LTVDA | 10 kΩ (approximate) pull-up resistor to 3.3V if digital video out is not implemented. |
| LTCLK | Series resistor 22 Ω ± 2%. |
| OCLK/RCLK | Series resistor 33 Ω ± 2%. |

| Checklist Line Items | Comments |
|---|---|
| LMD[27:31]<br>Reset strapping options: | **Strapping options:** For a "1", use a 10 kΩ (approximate) pull-up resistor to 3.3V; a "0" is default (due to internal pull-down resistors).<br>LMD13: 0= LMD29 determines host bus frequency<br>1= host bus frequency is 133 MHz<br>LMD31: 0 = Normal operation<br>1 = XOR TREE for testing purposes<br>LMD30: 0 = Normal operation<br>1 = Tri-state mode for testing purposes (will tri-state all signals)<br>LMD29: 0 = System bus frequency = 66 MHz<br>1 = System bus frequency = 100 MHz<br>LMD28: The value on LMD28 sampled at the rising edge of CPURST# reflects if the IOQD (In-Order Queue Depth) is set to 1 or 4.<br>0 = IOQD = 4<br>1 = IOQD = 1<br>LMD27: PGA370: Connect to $V_{CORE_{DET}}$ on the processor (pin E21) through a 10 kΩ series resistor for the Celeron processor and Pentium II processor<br>For the Celeron processor and Pentium III processor, LMD27 should not be pulled up.<br>SC242: No Connect |
| HCOMP | **Option 1—RCOMP Method:** Tie the HCOMP pin to a 40 Ω 1% or 2% (or 39 Ω 1%) pull-up resistor to 1.8V via a 10 mil wide, very short (~0.5") trace.<br>**Option 2—ZCOMP Method:** The HCOMP pin must be tied to a 10 mil trace that is AT LEAST 18" long. This trace must be un-terminated and care should be taken when routing the signal to avoid crosstalk (1520 mil separation between this signal and any adjacent signals is recommended). This signal may not cross power plane splits. |

## Table 47. System Memory Checklist

| Checklist Line Items | Recommendations |
|---|---|
| Pin 147 | Connect to Ground (since Intel® 810E2 chipset does not support registered DIMMs). |
| WP (Pin 81 on the DIMMs) | Add a 4.7 kΩ pull-up resistor to 3.3V. This is a recommendation to write-protect the DIMM's EEPROM. |
| MAA[7:4], MAB[7:4] | Add 10 Ω series resistors to the MAA[7:4], MAB[7:4] as close as possible to GMCH for signal integrity. |

## Table 48. Display Cache Checklist

| Checklist Line Items | Recommendations |
|---|---|
| CKE | 4.7 kΩ pull-up resistor to VCC3. |

# 7.2. Intel® ICH2 Checklist

## 7.2.1. PCI Interface

| Checklist Items | Recommendations |
|---|---|
| All | All inputs to the ICH2 must not be left floating. Many GPIO signals are fixed inputs that must be pulled up to different sources. See GPIO section for recommendations. |
| PERR#, SERR# PLOCK#, STOP# DEVSEL#, TRDY# IRDY#, FRAME# REQ#[0:4], GPIO[0:1], THRM# | These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to VCC3.3 or a 2.7 kΩ pull-up resistor to VCC5. See PCI 2.2 Component Specification for pull-up recommendations for VCC3.3 and VCC5. |
| PCIRST# | The PCIRST# signal should be buffered to form the IDERST# signal.<br>33 Ω series resistor to IDE connectors. |
| PCIGNT# | No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented they must be pulled up to VCC3.3. |
| PME# | This signal has an integrated pull-up of 24K. |
| SERIRQ | External weak (8.2 kΩ) pull-up resistor to VCC3.3 is recommended. |
| GNT[A]# /GPIO[16], GNT[B]/ GNT[5]#/ GPIO[17] | No extra pull-up needed. These signals have integrated pull-ups of 24 kΩ.<br>GNT[A] has an added strap function of “top block swap”. The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull-down resistor can be added to manually enable the function. |

## 7.2.2. Hub Interface

| Checklist Items | Recommendations |
|---|---|
| HL[11] | No pull-up resistor required. Use a no-stuff or a test point to put the ICH2 into NAND chain mode testing |
| HL_COMP | Tie the COMP pin to a 40 Ω 1% or 2% (or 39 Ω - 1%) pull-up resistor (to VCC1.8) via a 10-mil wide, very short (~0.5 inch) trace. ZCOMP No longer supported. |

## 7.2.3. LAN Interface

| Checklist Items | Recommendations | Comments |
|---|---|---|
| 1 | Trace Spacing: 5 mils wide, 10 mil spacing | |
| 2 | LAN Max Trace Length Intel® ICH2 to CNR:<br>L = 3” to 9” (0.5” to 3” on card) | To meet timing requirements. |
| 3 | Stubs due to R-pak CNR/LOM stuffing option should not be present. | To minimize inductance. |
| 4 | Maximum Trace Lengths: ICH2 to Intel® 82562EH: L = 4.5 inches to 10 inches; 82562ET: L = 3.5 inches to 10 inches; 82562EM: L = 4.5 inches to 8.5 inches. | To meet timing requirements. |

| Checklist Items | Recommendations | Comments |
|---|---|---|
| 5 | Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inches (clock must be longest trace) | To meet timing and signal quality requirements. |
| 6 | Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN phy. | To meet timing and signal quality requirements. |
| 7 | Keep the total length of each differential pair under 4 inches. | Issues found with traces longer than 4 inches : IEEE phy conformance failures, excessive EMI and or degraded receive BER. |
| 8 | Do not route the transmit differential traces closer than 100 mils to the receive differential traces. | To minimize crosstalk. |
| 9 | Distance between differential traces and any other signal line is 100 mils. (300 mils recommended) | To minimize crosstalk. |
| 10 | Route 5 mils on 7 mils for differential pairs (out of LAN phy) | To meet timing and signal quality requirements. |
| 11 | Differential trace impedance should be controlled to be ~100 Ω. | To meet timing and signal quality requirements. |
| 12 | For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90 degree bend is required, it is recommended to use two 45 degree bends. | To meet timing and signal quality requirements. |
| 13 | Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. | This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards. |
| 14 | Do not route traces and vias under crystals or oscillators. | This will prevent coupling to or from the clock. |
| 15 | Trace width to height ratio above the ground plane should be between 1:1 and 3:1. | To control trace EMI radiation. |
| 16 | Traces between decoupling and I/O filter capacitors should be as short and wide as practical. | Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors. |
| 17 | Vias to decoupling capacitors should be sufficiently large in diameter. | To decrease series inductance. |
| 18 | Avoid routing high-speed LAN* or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices. | To minimize crosstalk. |
| 19 | Isolate I/O signals from high speed signals. | To minimize crosstalk. |
| 20 | Place the 82562ET/EM part more than 1.5 inches away from any board edge. | This minimizes the potential for EMI radiation problems. |
| 21 | Place at least one bulk capacitor (4.7 µF or greater) on each side of the 82562ET/EM. | Research and development has shown that this is a robust design requirement. |
| 22 | Place decoupling caps (0.1 µF) as close to the 82562ET/EM as possible. | |

| Checklist Items | Recommendations | Comments |
|---|---|---|
| 23<br>LAN_CLK | Connect to LAN_CLK on Platform LAN Connect Device. | |
| 24<br>LAN_RXD[2:0] | Connect to LAN_RXD on Platform LAN Connect Device. ICH2 contains integrated 9 kΩ pull-up resistors on interface. | |
| 25<br>LAN_TXD[2:0]<br>LAN_RSTSYNC | Connect to LAN_TXD on Platform LAN Connect Device. | |

**NOTES:**
1. LAN connect interface can be left NC if not used. Input buffers internally terminated.
2. In the event of EMI problems during emissions testing (FCC Classifications) you may need to place a decoupling capacitor (~470 pF) on each of the 4 LED pins. Reduces emissions attributed to LAN subsystem.

## 7.2.4. EEPROM Interface

| Checklist Items | Recommendations |
|---|---|
| EE_DOUT | Prototype Boards should include a placeholder for a pull-down resistor on this signal line, but do not populate the resistor. Connect to EE_DIN of EEPROM or CNR Connector.<br>Connected to EEPROM data input signal (input from EEPROM perspective and output from ICH2 perspective). |
| EE_DIN | No extra circuitry required. Connect to EE_DOUT of EEPROM or CNR Connector. ICH2 contains an integrated pull-up resistor for this signal.<br>Connected to EEPROM data output signal (output from EEPROM perspective and input from ICH2 perspective). |

## 7.2.5. FWH/LPC Interface

| Checklist Items | Recommendations |
|---|---|
| FWH[3:0]/ LAD[3:0]<br>LDRQ[1:0] | No extra pull-ups required. ICH2 Integrates 24 kΩ pull-up resistors on these signal lines. |

## 7.2.6. Interrupt Interface

| Checklist Items | Recommendations |
|---|---|
| PIRQ[D:A]# | These signals require a pull-up resistor. The recommendation is a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3.3.<br>In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register.<br>In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19. This frees the ISA interrupts. |

| Checklist Items | Recommendations |
|---|---|
| PIRQ[G:F]#/ GPIO[4:3] | These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3.3.<br>In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register.<br>In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the ISA interrupts. |
| PIRQ[H]#<br>PIRQ[E]# | These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3.3.<br>Since PIRQ[H]# and PIRQ[E]# are used internally for LAN and USB controllers, they cannot be used as GPIO(s) pin. |
| APIC | • **Intel Pentium® 4 processor based systems:**<br>— These processors do not have APIC pins so all platforms using this processor should both tie APICCLK to ground and tie APICD:[1:0] to ground via a 1k-10k pull-down resistor.<br>• **Non- Pentium 4 processor based systems:**<br>— If the APIC is used: 150Ω pull-up resistors on APICD[1:0]<br>— Connect APICCLK to CK133 with a 20-33Ω series termination resistor.<br>• **If the APIC is not used on up systems:**<br>— The APICCLK can either be tied to GND or connected to CK133, but not left floating.<br>— Pull APICD[1:0] to GND through 10kΩ pull-down resistors. |

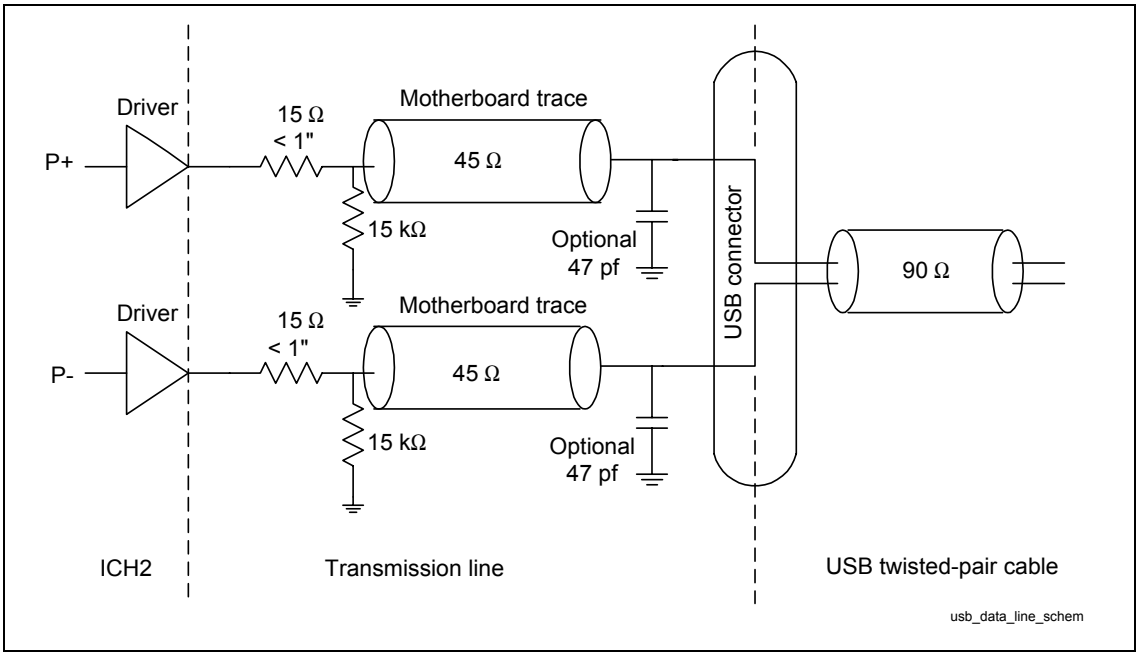
## 7.2.7. GPIO Checklist

| Checklist Items | Recommendations |
|---|---|
| All | Ensure ALL unconnected signals are OUTPUTS ONLY! |
| GPIO[7:0] | These pins are in the Main Power Well. Pull-ups must use the VCC3.3 plane. Unused **core** well inputs must either be pulled up to VCC3.3 or pulled down. Inputs must not be allowed to float. These signals are 5V tolerant.<br>GPIO[1:0] can be used as REQ[A:B]#. GPIO[1] can also used as PCI REQ[5]#. |
| [13:11], GPIO[8] | These pins are in the Resume Power Well. Pull-ups must use the VCCSUS3.3 plane. These are the only GPI signals in the resume well with associated status bits in the GPE1_STS register. Unused **resume** well inputs must be pulled up to VCCSUS3.3. These signals are not 5V tolerant.<br>These are the only GPIs that can be used as ACPI compliant wake events. |
| GPIO[23:16] | Fixed as output only. Can be left NC. In Main Power Well. GPIO22 is open drain. |
| GPIO[24,25,27,28] | These I/O pins can be NC. These pins are in the resume power well. |

## 7.2.8. USB

| Checklist Items | Recommendations |
|---|---|
| USBP[3:0]P<br>USBP[3:0]N | See Figure 92 for circuitry needed on each differential Pair. |
| VCC USB (Cable power) | It should be powered from the 5V core instead of the 5V standby, unless adequate standby power is available. |
| Voltage drop considerations | The resistive component of the fuses, ferrite beads and traces must be considered when choosing components, and power and GND trace widths. Minimize the resistance between the Vcc5 power supply and the USB ports to prevent voltage drop.<br>Sufficient bypass capacitance should be located near the USB receptacles to minimize the voltage drop that occurs during the hot plugging a new device. For more information, see the USB specification. |
| Fuse | A fuse larger than 1A can be chosen to minimize the voltage drop. |

**Figure 92. USB Data Line Schematic**



## 7.2.9. Power Management

| Checklist Items | Recommendations |
|---|---|
| THRM# | Connect to temperature Sensor. Pull-up if not used. |
| SLP_S3#<br>SLP_S5# | No pull-up/down resistors needed. Signals driven by ICH2. |
| PWROK | This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_8 have reached their nominal voltages |
| PWRBTN# | This signal has an integrated pull-up of 24K. |
| RI# | RI# does not have an internal pull-up. Recommend an 8.2 kΩ pull-up resistor to Resume well.<br>If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns, the RI_STS bit will be set and the system will interpret that as a wake event. |
| RSMRST# | Connect to power monitoring logic, and should go high no sooner than 10 ms after both VccSUS3_3 and VccSus1_8 have reached their nominal voltages. Requires weak pull-down. Also requires well isolation control as directed in section 3.20.8 |

## 7.2.10. Processor Signals

| Checklist Items | Recommendations |
|---|---|
| A20M#, CPUSLP#, IGNNE#, INIT#, INTR, NMI, SMI#, STPCLK# | Internal circuitry has been added to the ICH2, external pull-up resistors are not needed. |
| FERR# | Requires Weak external pull-up resistor to $VCC_{CMOS}$. |
| RCIN#<br>A20GATE | Pull-up signals to VCC3.3 through a 10 kΩ resistor. |
| CPUPWRGD | Connect to the processor's CPUPWRGD input. Requires weak external pull-up resistor. |

## 7.2.11. System Management

| Checklist Items | Recommendations |
|---|---|
| SMBDATA<br>SMBCLK | Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.)<br>Value of pull-up resistors determined by line load. Typical value used is 8.2 kΩ. |
| SMBALERT#/ GPIO[11] | See GPIO section if SMBALERT# not implemented |
| SMLINK[1:0] | Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.)<br>Value of pull-up resistors determined by line load. Typical value used is 8.2 kΩ. |
| INTRUDER# | Pull signal to VCCRTC (VBAT), if not needed. |

## 7.2.12. ISA Bridge Checklist

| Checklist Items | Recommendations |
|---|---|
| ICH2 GPO[21] / MISA NOGO input | Connect ICH2 GPO[21] to MISA NOGO input.<br>If GPO[21] is not available on the ICH2, any other GPO that defaults High in the system can be used. GPO[21] is the only ICH2 GPO that defaults high. |
| ICH2 AD22 / MISA IDSEL input | Connect ICH2 AD22 to the MISA IDSEL input. |

## 7.2.13. RTC

| Checklist Items | Recommendations |
|---|---|
| VBIAS | The VBIAS pin of the ICH2 is connected to a .047 µF cap. See Figure 86 |
| RTCX1<br>RTCX2 | Connect a 32.768 kHz Crystal Oscillator across these pins with a 10 MΩ resistor and use 18 pF decoupling caps (assuming crystal with CLOAD=12.5 pF) at each signal.<br>The ICH2 implements a new internal oscillator circuit as compared with the PIIX4 to reduce power consumption. The external circuitry shown in Figure 86 will be required to maintain the accuracy of the RTC.<br>The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.<br>RTCX1 may optionally be driven by an external oscillator instead of a crystal. These signals are 1.8V only, and must not be driven by a 3.3V source. |
| RTCRST# | Ensure 10 ms-20 ms RC delay (8.2 K & 2.2 µF) See Figure 43. RTCRST External Circuit for Intel® ICH2 RTC |
| SUSCLK | To assist in RTC circuit debug, route SUSCLK to a test point if it is unused. |

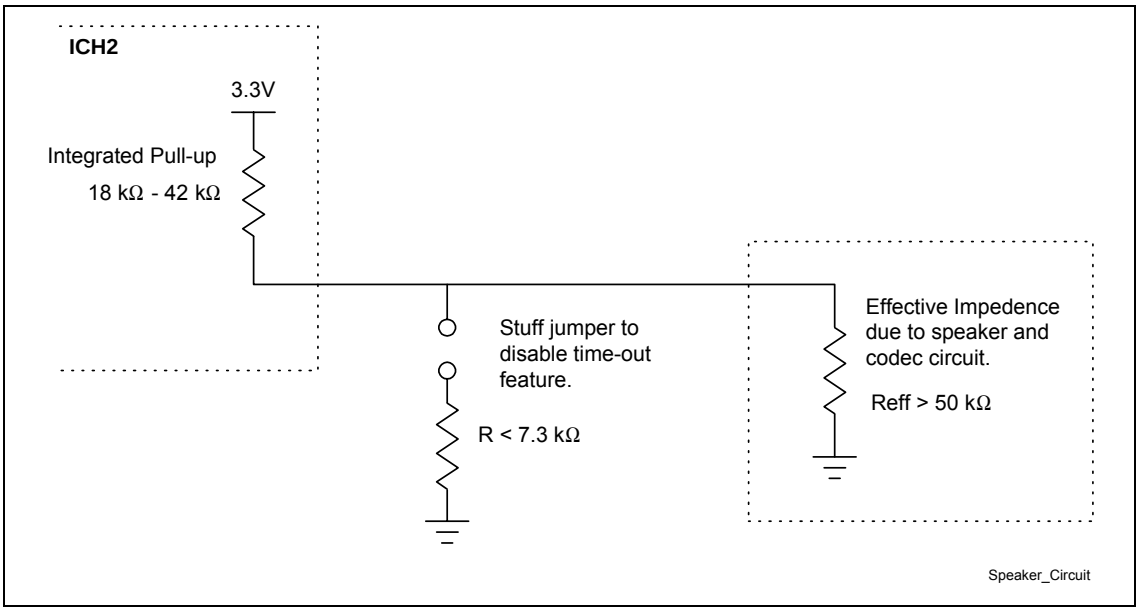
## 7.2.14. AC'97

| Checklist Items | Recommendations |
|---|---|
| AC_BITCLK | No extra pull-down resistors required.<br>When nothing is connected to the link, BIOS must set a shut off bit for the internal keeper resistors to be enabled. At that point, you do not need pull-ups/pull-downs on any of the link signals. |
| AC_SYNC | No extra pull-down resistors required. Some implementations add termination for signal integrity. Platform specific. |
| AC_SDOUT | Requires a jumper to 8.2 kΩ pull-up resistor. Should not be stuffed for default operation.<br>This pin has a weak internal pull-down. To properly detect a safe_mode condition a strong pull-up will be required to over-ride this internal pull-down. |
| AC_SDIN[1], AC_SDIN[0] | Requires pads for weak 10 kΩ pull-downs. Stuff resistor for unused AC_SDIN signal or AC_SDIN signal going to the CNR connector.<br>AC_SDIN[1:0] are inputs to an internal OR gate. If a pin is left floating, the output of the OR gate will be erroneous.<br>If there is no codec on the system board, then both AC_SDIN[1:0] should be pull-down externally with resisters to ground. |
| CDC_DN_ENAB# | If the primary codec is down on the motherboard, this signal must be low to indicate the motherboard codec is active and controlling the AC '97 interface. |
| | $Z_O$ AC97 = 60 Ω ± 15% |
| | 5 mil trace width, 5 mil spacing between traces |
| | Max Trace Length ICH2/Codec/CNR = 14" |

## 7.2.15. Miscellaneous Signals

| Checklist Items | Recommendations |
|---|---|
| SPKR | No extra pull-up resistors. Has integrated pull-up of between 18 kΩ and 42 kΩ. The integrated pull-up is only enabled at boot/reset for strapping functions; at all other times, the pull-up is disabled.<br>A low effective impedance may cause the TCO Timer Reboot function to be erroneously disabled.<br>Effective Impedance due speaker and codec circuitry must be greater than 50 kΩ or a means to isolate the resistive load from the signal while PWROK is low be found. see following figure. |
| TP[0] | Requires external pull-up resistor to VCCSUS3.3 |
| FS[0] | Rout to a testpoint. ICH2 contains an integrated pull-up for this signal. Testpoint used for manufacturing appears in XOR tree. |

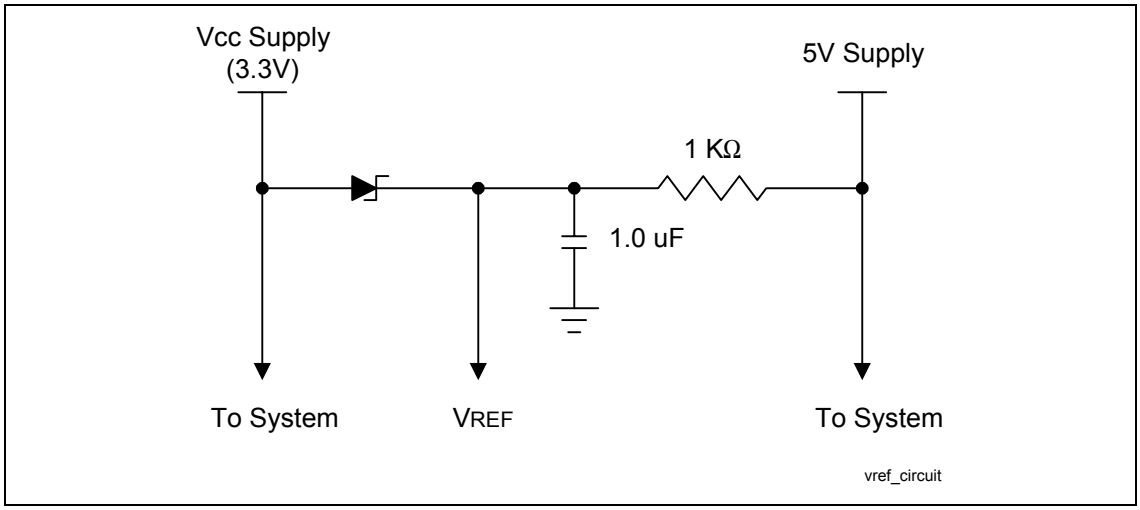
**Figure 93. SPKR Circuitry**



## 7.2.16. Power

| Checklist Items | Recommendations |
|---|---|
| V_CPU_IO[1:0] | The power pins should be connected to the proper power plane for the processor 's CMOS Compatibility Signals. Use one 0.1 µF decoupling cap. |
| VccRTC | No clear CMOS jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safemode strapping for Clear CMOS |
| Vcc3.3 | Requires six 0.1 µF decoupling capacitors |
| VccSus3.3 | Requires one 0.1 µF decoupling capacitor. |
| Vcc1.8 | Requires two 0.1 µF decoupling capacitors. |
| VccSus1.8 | Requires one 0.1 µF decoupling capacitor. |
| V5_REF SUS | Requires one 0.1 µF decoupling capacitor.<br>V5REF_SUS only affects 5V-tolerance for USB OC:[3:0]# pins and can be connected to either VccSUS3_3 or 5V_Always/5V_AUX if 5V tolerance on these OC:[3:0]# is not needed. If 5V tolerance on OC:[3:0]# is needed then V5REF_SUS USB must be connected to 5V_Always/5V_AUX which remains powered during S5. |
| 5V_REF | 5VREF is the reference voltage for 5V tolerant inputs in the ICH2. Tie to pins VREF[2:1]. 5VREF must power up before or simultaneous to Vcc3_3. It must power down after or simultaneous to Vcc3_3. Refer to the figure below for an example circuit schematic that may be used to ensure the proper 5VREF sequencing. |

**Figure 94. V5REF Circuitry**

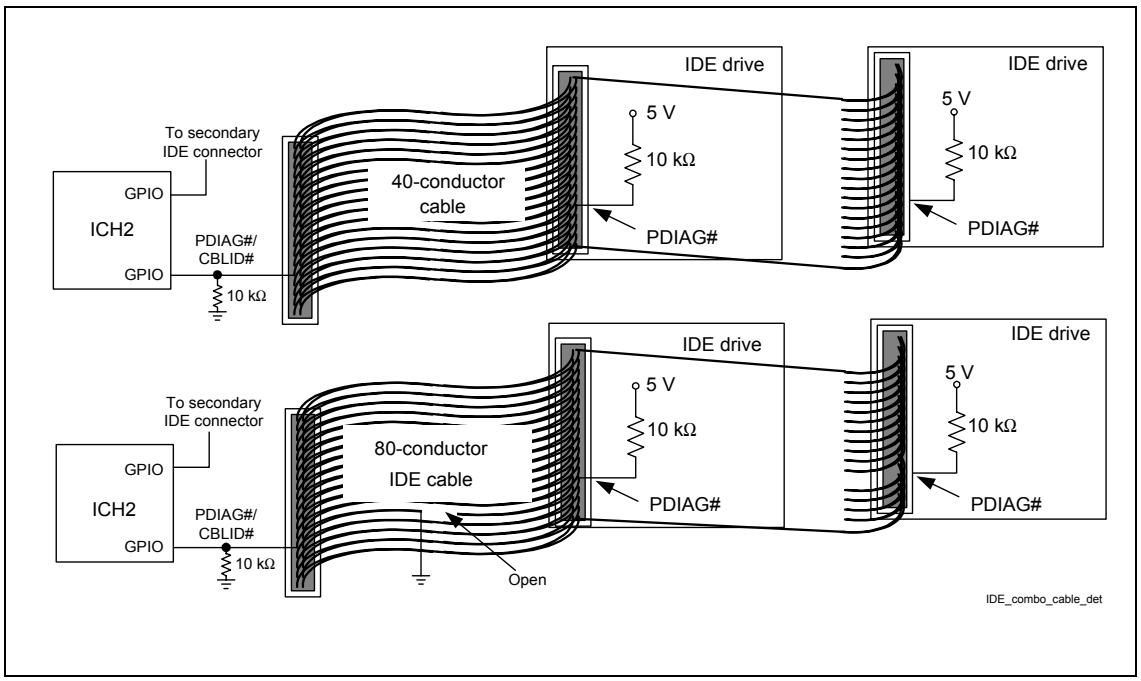


## 7.2.17. IDE Checklist

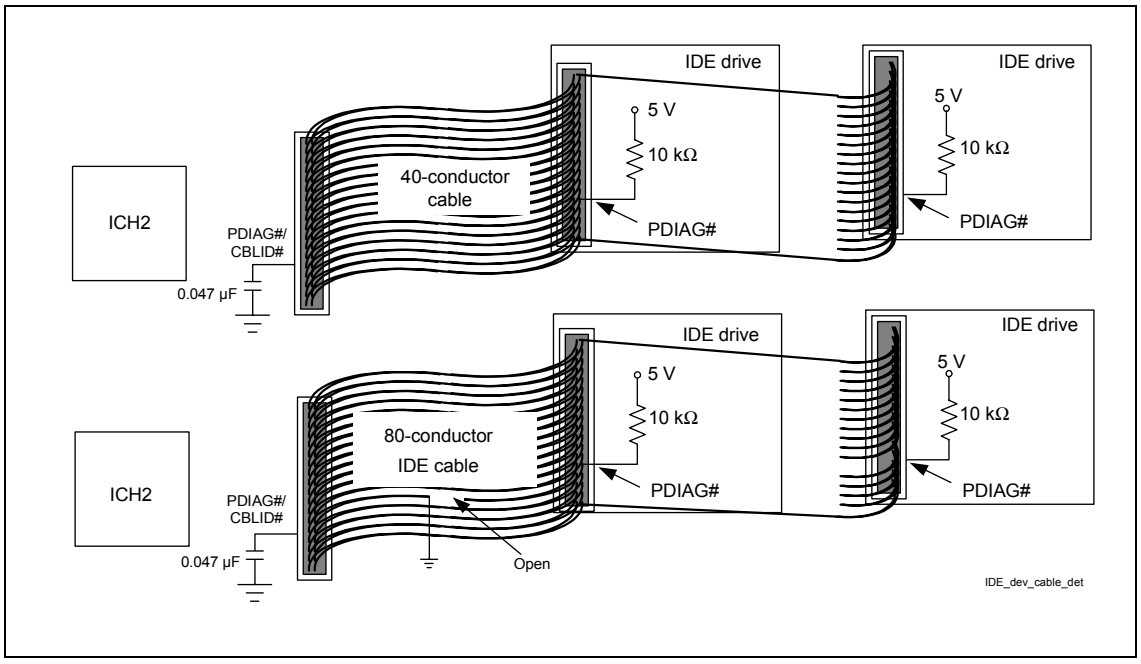
| Checklist Items | Recommendations |
|---|---|
| PDD[15:0], SDD[15:0] | No extra series termination resistors or other pull-ups/pull-downs are required. These signals have integrated series resistors.<br>NOTE: Simulation data indicates that the integrated series termination resistors can range from 31 Ω to 43 Ω.<br>PDD7/SDD7 does not require a 10 kΩ pull-down resistor. Refer to ATA ATAPI-4 specification. |
| PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3# | No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns. These signals have integrated series resistors.<br>NOTE: Simulation data indicates that the integrated series termination resistors can range from 31 Ω to 43 Ω. |
| PDREQ<br>SDREQ | No extra series termination resistors. No pull-down resistors needed.<br>These signals have integrated series resistors in the ICH2. These signals have integrated pull-down resistors in the ICH2. |
| PIORDY<br>SIORDY | No extra series termination resistors. These signals have integrated series resistors in the ICH2. Pull-up to VCC3.3 via a 4.7 kΩ resistor. |
| IRQ14, IRQ15 | Recommend 8.2 kΩ—10 kΩ pull-up resistors to VCC3.3.<br>No extra series termination resistors. |
| IDERST# | The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal. |
| Cable Detect: | **Host Side/Device Side Detection:** Connect IDE pin PDIAG/CBLID to an ICH2 GPIO pin. Connect a 10 kΩ resistor to GND on the signal line. The 10 kΩ resistor to GND prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3V and 5V tolerant GPIOs.<br>**Device Side Detection:** Connect a 0.047 µF capacitor from IDE pin PDIAG/CBLID to GND. No ICH2 connection.<br>NOTE: All ATA66/ATA100 drives will have the capability to detect cables |

Note: The maximum trace length from the ICH2 to the ATA connector is 8 inches.

### Figure 95. Host/Device Side Detection Circuitry




### Figure 96. Device Side Only Cable Detection



## 7.3. LPC Checklist

| Checklist Items | Recommendations |
|---|---|
| RCIN# | Pull up through 8.2-kΩ resistor to Vcc3_3. |
| LPC_PME# | Pull up through 8.2-kΩ resistor to Vcc3_3. Do not connect LPC PME# to PCI PME#. If the design requires the Super I/O to support wake from any suspend state, connect Super I/O LPC_PME# to a resume well GPI on the ICH2. |
| LPC_SMI# | Pull up through 8.2-kΩ resistor to Vcc3_3. This signal can be connected to any ICH2 GPI. The GPI_ROUTE register provides the ability to generate an SMI# from a GPI assertion. |
| TACH1, TACH2 | Pull up through 4.7-kΩ resistor to Vcc3_3.<br>Jumper for decoupling option (decouple with 0.1-µF capacitor) |
| J1BUTTON1, JPBUTTON2, J2BUTTON1, J2BUTTON2 | Pull up through 1-kΩ resistor to Vcc5. Decouple through 47-pF capacitor to GND. |
| LDRQ#1 | Pull up through 4.7-kΩ resistor to Vcc3SBY. |
| A20GATE | Pull up through 8.2-kΩ resistor to Vcc3_3. |
| MCLK, MDAT | Pull up through 4.7-kΩ resistor to PS2V5. |
| L_MCLK, L_MDAT | Decoupled using 470-pF capacitor to ground. |
| RI#1_C, CTS0_C, RXD#1_C, RXD0_C, RI0_C, DCD#1_C, DSR#1_C, DSR0_C, DTR#1_C, DTR0_C, DCD0_C, RTS#1_C, RTS0_C, CTS#1_C, TXD#1_C, TXD0_C | Decoupled using 100-pF capacitor to GND. |
| L_SMBD | Pass through 150-Ω resistor to Intel® 82559. |
| SLCT#, PE, BUSY, ACK#, ERROR# | Pull up through 2.2-kΩ resistor to Vcc5_DB25_DR.<br>Decouple through 180-pF capacitor to GND. |
| LFRAME# | No required pull-up resistor |
| LDRQ#0 | No required pull-up resistor |
| STROBE#, ALF#, SLCTIN#, PAR_INIT# | Signal passes through a 33-Ω resistor and is pulled up through a 2.2-kΩ resistor to Vcc5_DB25_CR. Decoupled using a 180-pF capacitor to GND. |
| PWM1, PWM2 | Pull up to 4.7 kΩ to Vcc3_3 and connected to jumper for decouple with 0.1-µF capacitor to GND. |
| INDEX#, TRK#0, RDATA#, DSKCHG#, WRTPRT# | Pull up through 1-kΩ resistor to Vcc5. |
| PDR0, PDR1, PDR2, PDR3, PDR4, PDR5, PDR6, PDR7 | Passes through 33-Ω resistor.<br>Pull up through 2.2 kΩ to Vcc5_DB5_CRD and couple through 180-pF capacitor to GND. |
| SYSOPT | Pull down with 4.7-kΩ resistor to GND or IO address of 02Eh. |

## 7.4. System Checklist

| Checklist Items | Recommendations |
|---|---|
| KEYLOCK# | Pull up through 10-kΩ resistor to Vcc3_3. |
| PBTN_IN | Connects to PBSwitch and PBin. |
| PWRLED | Pull up through a 220-Ω resistor to Vcc5. |
| R_IRTX | Signal IRTX after it is pulled down through 4.7-kΩ resistor to GND and passes through 82-Ω resistor. |
| IRRX | Pull up to 100-kΩ resistor to Vcc3_3.<br>When signal is input for SI/O decouple through 470-pF capacitor to GND |
| IRTX | Pull down through 4.7 kΩ to GND.<br>Signal passes through 82-Ω resistor.<br>When signal is input to SI/O decouple through 470-pF capacitor to GND |
| FP_PD | Decouple through a 470-pF capacitor to GND.<br>Pull up 470 Ω to Vcc5. |
| PWM1, PWM2 | Pull up through a 4.7-kΩ resistor to Vcc3_3. |

## 7.5. FWH Checklist

| Checklist Items | Recommendations |
|---|---|
| No floating inputs | Unused FGPI pins must be tied to a valid logic level. |
| WPROT, TBLK_LCK | Pull up through a 4.7-kΩ resistor to Vcc3_3. |
| R_VPP | Pulled up to Vcc3_3 and decoupled with two 0.1-µF capacitors to GND. |
| FGPI0_PD, FGPI1_PD, FGPI2_PD, FPGI3_PD, FPGI4_PD, IC_PD | Pull down through a 8.2-kΩ resistor to GND. |
| FWH_ID1, FWH_ID2, FWH_ID3 | Pull down to GND. |
| INIT# | FWH INIT# must be connected to processor INIT#. |
| RST# | FWH RST# must be connected to PCIRST#. |
| ID[3:0] | For a system with only one FWH device, tie ID[3:0] to ground. |

## 7.6. Clock Synthesizer Checklist

| Checklist Items | Recommendations |
|---|---|
| REFCLK | Connects to R-RefCLK, USB_CLK, SIO_CLK14, and ICHCLK14. |
| ICH_3V66/3V66_0, DOTCLK | Passes through 33-Ω resistor.<br>When signal is input for ICH2, it is pulled down through a 18-pF capacitor to GND. |
| DCLK/DCLK_WR | Passes through 33-Ω resistor.<br>When signal is input for GMCH, it is pulled down through a 22-pF capacitor to GND. |
| CPUHCLK/CPU_0_1 | Passes through 33-Ω resistor.<br>When signal is input for 370PGA, decouple through a 18-pF capacitor to GND. |
| R_REFCLK | REFCLK passed through 10-kΩ resistor.<br>When signal is input for 370PGA, pull up through 1-kΩ resistor to Vcc3_3 and pass through 10-kΩ resistor. |
| USB_CLK, ICH_CLK14 | REFCLK passed through 10-Ω resistor. |
| XTAL_IN, XTAL_OUT | Passes through 14.318-MHz oscillator.<br>Pulled down through 18-pF capacitor to GND. |
| SEL1_PU | Pulled up via MEMV3 circuitry through 8.2-kΩ resistor. |
| FREQSEL | Connected to clock frequency selection circuitry through 10-kΩ resistor. |
| L_VCC2_5 | Connects to VDD2_5[0…1] through ferrite bead to Vcc2_5. |
| GMCHHCLK/CPU_1, ITPCLK/CPU_2, PCI_0/PCLK_OICH, PCI_1/PCLK_1, PCI_2/PCLK_2, PCI_3/PCLK_3, PCI_4/PCLK_4, PCI_5/PCLK_5, PCI_6/PCLK_6, APICCLK_CPU/APIC_0, APICCLK)ICH/APIC_1, USBCLK/USB_0, GMCH_3V66/3V66_1, AGPCLK_CONN | Passes through 33-Ω resistor. |
| MEMCLK0/DRAM_0, MEMCLK1/DRAM_1, MEMCLK2/DRAM_2, MEMCLK3/DRAM_3, MEMCLK4/DRAM_4, MEMCLK5/DRAM_5, MEMCLK6/DRAM_6, MEMCLK7/DRAM_7, SCLK | Pass through 22-Ω resistor. |

## 7.7. ITP Probe Checklist

| Checklist Items | Recommendations |
|---|---|
| R_TCK, TCK R_TMS, TMS | Connect to 370-Pin socket through 47-Ω resistor and pull up to VCMOS. |
| ITPRDY#, R_ITPRDY# | Connect to 370-Pin socket through 243-Ω resistor. |
| TDI | Pull up through 330-Ω resistor to VCMOS. |
| TDO | Pull up through 150-Ω resistor to VCMOS. |
| PLL1 | See Design Guide. |
| PLL2 | See Design Guide. |

## 7.8. Power Delivery Checklist

| Checklist Items | Recommendations |
|---|---|
| All voltage regulator components meet maximum current requirements. | Consider all loads on a regulator, including other regulators. |
| All regulator components meet thermal requirements. | Ensure the voltage regulator components and dissipate the required amount of heat. |
| VCC1_8 | VCC1_8 power sources must supply 1.8 V and be between 1.71 V to 1.89 V. |
| If devices are powered directly from a dual rail (i.e., not behind a power regulator), then the RDSon of the FETs used to create the dual rail must be analyzed to ensure there is not too much voltage drop across the FET. | “Dual” voltage rails may not be at the expected voltage. |
| Dropout voltage | The minimum dropout for all voltage regulators must be considered. Take into account that the voltage on a dual rail may not be the expected voltage. |
| Voltage tolerance requirements are met. | See the individual component specifications for each voltage tolerance. |
| Total power consumption in S3 must be less than the rated standby supply current. | Adequate power must be supplied by power supply. |

# 8. Flexible Motherboard Guidelines

## 8.1. Flexible Processor Guidelines

### 8.1.1. Flexible System Design DC Guidelines

The processor DC guidelines for flexible system designed in this section is defined at the processor pin.

Table 49 lists the guidelines for future 1.5V processors and Table 50 lists the guidelines for future 2.0V processors. Specifications are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

**Table 49. Flexible Processor Voltage and Current Guidelines for 1.5V Processors**

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $Vcc_{CORE}$ | VCC for processor core | | 1.5 | | V | 1, 3 |
| Baseboard Tolerance, Static | processor core voltage static tolerance at processor pins | 0.070 | | 0.070 | V | 2, 3 |
| Baseboard Tolerance, Transient | processor core voltage transient tolerance level at processor pins | 0.110 | | 0.110 | V | 2, 3 |
| $I_{CCCORE}$ | ICC for processor core | | | 12.6 | A | 1, 4, 5, 7 |
| $I_{SGnt}$ | ICC Stop-Grant for processor core | | | 0.8 | A | 6 |
| $dI_{CCCORE}/dt$ | Power supply current slew rate | | | 240 | A/µS | 8, 9 |

**NOTES:**

1. $Vcc_{CORE}$ and $Icc_{CORE}$ supply the processor core.
2. Use the Typical Voltage specification with the Tolerance specifications to provide correct voltage regulation to the processor.
3. These are the tolerance requirements, across a 20 MHz bandwidth at the processor pin at the bottom side of the system platform. $Vcc_{CORE}$ must return to within the static voltage specification within 100 us after a transient event; see the VRM 8.4 DC-DC Converter Specification for further details.
4. Max ICC measurements are measured at Vcc maximum voltage, under maximum signal loading conditions.
5. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of $Vcc_{CORE}$ ($Vcc_{CORE\_TYP}$). In this case, the maximum current level for the regulator, $Icc_{CORE\_REG}$, can be reduced from the specified maximum current $Icc_{CORE\_MAX}$ and is calculated by the equation:

$$Icc_{CORE\_REG} = Icc_{CORE\_MAX} \times Vcc_{CORE\_TYP} / (Vcc_{CORE\_TYP} + Vcc_{CORE} \text{ Tolerance, Transient})$$

6. The current specified is also for AutoHALT state.
7. Maximum values are specified by design/characterization at maximum $Vcc_{CORE}$.
8. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
9. dICC/dt specifications are specified at the processor pins.

### Table 50. Flexible Processor Voltage and Current Guidelines for 2.0 V Processors [1]

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $Vcc_{CORE}$ | $V_{CC}$ for processor core | | 2.00 | | V | 1, 3 |
| Baseboard Tolerance, Static | processor core voltage static tolerance at processor pins | 0.089 | | 0.100 | V | 2, 3 |
| Baseboard Tolerance, Transient | processor core voltage transient tolerance level at processor pins | 0.144 | | 0.144 | V | 2, 3 |
| $I_{CCCORE}$ | $I_{CC}$ for processor core | | | 15.6 | A | 1, 4, 5, 7 |
| $I_{SGnt}$ | $I_{CC}$ Stop-Grant for processor core | | | 0.8 | A | 6 |
| $dI_{CCCORE}/dt$ | Power supply current slew rate | | | 240 | A/µS | 8, 9 |

**NOTES:**

1. $Vcc_{CORE}$ and $Icc_{CORE}$ supply the processor core.
2. Use the Typical Voltage specification with the Tolerance specifications to provide correct voltage regulation to the processor.
3. These are the tolerance requirements, across a 20 MHz bandwidth at the top of the PPGA package. $Vcc_{CORE}$ must return to within the static voltage specification within 100 us after a transient event; see the VRM 8.4 DC-DC Converter Specification for further details.
4. Max ICC measurements are measured at Vcc maximum voltage, under maximum signal loading conditions.
5. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of $Vcc_{CORE}$ ($Vcc_{CORE\_TYP}$). In this case, the maximum current level for the regulator, $Icc_{CORE\_REG}$, can be reduced from the specified maximum current $Icc_{CORE\_MAX}$ and is calculated by the equation:

   $$Icc_{CORE\_REG} = Icc_{CORE\_MAX} \text{ X } Vcc_{CORE\_TYP} / (Vcc_{CORE\_TYP} + Vcc_{CORE} \text{ Tolerance, Transient})$$

6. The current specified is also for AutoHALT state.
7. Maximum values are specified by design/characterization at maximum $Vcc_{CORE}$.
8. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
9. dICC/dt specifications are specified at the processor pins.

## 8.1.2. System Bus AC Guidelines

Table 51 and Table 52 contain 66 MHz and 100 MHz system bus AC Guidelines defined at the processor pins. For 133 MHz see the *Intel® Pentium® III processor PGA 370 Socket* datasheet.

Table 51 contains the BCLK guidelines and Table 52 contains the AGTL+ system bus guidelines. Processor System Bus AC Specifications for the AGTL+ Signal Group at the processor pins for 100 MHz are equivalent to 66 MHz. The 66 MHz specification is documented in the processor datasheet.

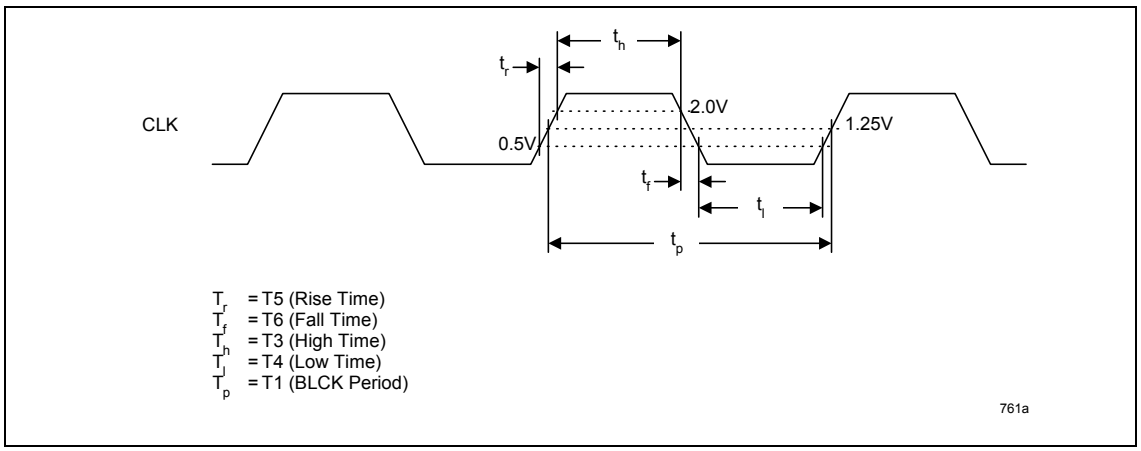
**Table 51. Flexible Motherboard Processor System Bus AC Guidelines (Clock) at the Processor Pins [1,2,3]**

| T# Parameter | Min | Nom | Max | Unit | Figure | Notes |
|---|---|---|---|---|---|---|
| System Bus Frequency | | | 66.67<br>100.00 | MHz<br>MHz | | All processor core frequencies |
| T1: BCLK Period | 15.0<br>10.0 | | | ns<br>ns | Figure 97<br>Figure 97 | 4, 5, 9 4, 6, 9 |
| T2: BCLK Period Stability | | | ±300<br>±250 | ps<br>ps | Figure 97<br>Figure 97 | 5, 7, 8, 9 6, 7, 8, 9 |
| T3: BCLK High Time | 4.94<br>2.5 | | | ns | Figure 97<br>Figure 97 | @>2.0V [5]<br>@>2.0V [6] |
| T4: BCLK Low Time | 4.94<br>2.4 | | | ns | Figure 97<br>Figure 97 | @<0.5V [5]<br>@<0.5V [6] |
| T5: BCLK Rise Time | 0.34<br>0.38 | | 1.5<br>1.36 | ns<br>ns | Figure 97<br>Figure 97 | (0.5V2.0V) [5, 11]<br>(0.5V2.0V) [6, 11] |
| T6: BCLK Fall Time | 0.34<br>0.38 | | 1.5<br>1.36 | ns<br>ns | Figure 97<br>Figure 97 | (2.0V0.5V) [5, 11]<br>(2.0V0.5V) [6, 11] |

**NOTES:**

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor core pin. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00V at the processor core pins.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25V at the processor core pins.
4. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
5. This specification applies to the processor when operating with a system bus frequency of 66 MHz.
6. This specification applies to the processor when operating with a system bus frequency of 100 MHz.
7. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25V at the processor core pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.
8. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer.
9. The average period over a 1 uS period of time must be greater than the minimum specified period.

### Figure 97. BCLK Waveform



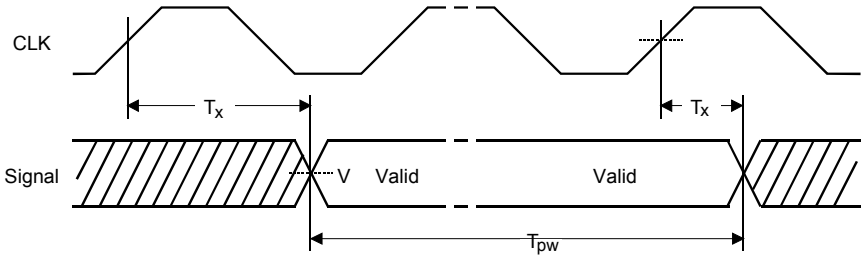

### Table 52. Processor System Bus AC Guidelines (AGTL+ Signal Group) at the Processor Pins [1, 2, 3, 4]

| T# Parameter | Min | Max | Unit | Figure | Notes |
|---|---|---|---|---|---|
| T7: AGTL+ Output Valid Delay | 0.30 | 4.43 | ns | Figure 98 | 5 |
| T8: AGTL+ Input Setup Time | 1.75 | | ns | Figure 99 | 5, 6, 7, 8 |
| T9: AGTL+ Input Hold Time | 0.85 | | ns | Figure 99 | 9 |
| T10: RESET# Pulse Width | 1.00 | | ms | Figure 100 | 7, 10 |

**NOTES:**

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor pin. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00V at the processor pins.
4. This specification applies to the processor operating with a 66 MHz or 100 MHz system bus.
5. Valid delay timings for these signals are specified into 25 Ω to 1.5V and with VREF at 1.0V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. Specification is for a minimum 0.40V swing.
9. Specification is for a maximum 1.0V swing.
10. After $Vcc_{CORE}$ and BCLK become stable.

### Figure 98. Processor System Bus Valid Delay Timings



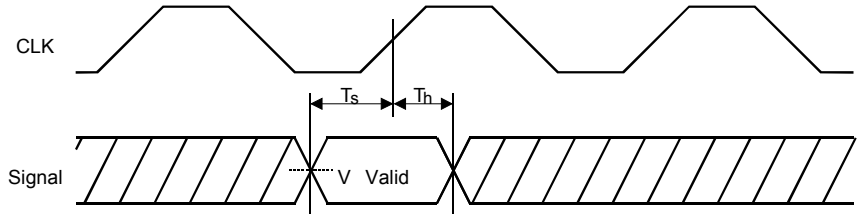

$T_x$ = T7, T11, T29 (Valid Delay)

$T_{pw}$ = T14, T15 (Pulse Wdith)

V = 1.0V for GTL+ signal group; 1.25V for CMOS, APIC and JTAG signal groups

000762b

### Figure 99. Processor System Bus Setup and Hold Timings

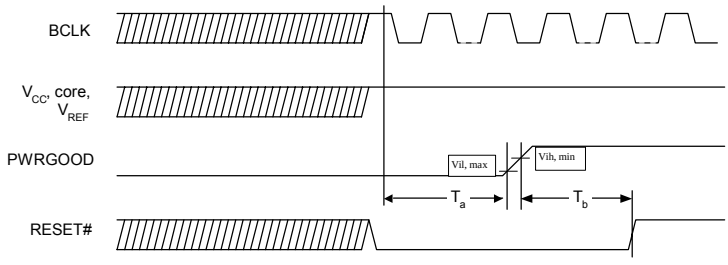



$T_s$ = T8, T12, T27 (Setup Time)

$T_h$ = T9, T13, T28 (Hold Time)

V = 1.0V for GTL+ signal group; 1.25V for CMOS, APIC and JTAG signal groups

### Figure 100. Power-On Reset and Configuration Timings




$T_a$ = T15 (PWRGOOD Inactive Pulse Width)

$T_b$ = T10 (RESET# Pulse Width)

## 8.1.3. Thermal Guidelines

The following table provides the recommended thermal design power dissipation for use in designing a flexible system board. The processor's heatslug is the attach location for all thermal solutions. The maximum and minimum case temperatures are specified in the following table. A thermal solution should be designed to ensure the temperature of the case never exceeds these specifications.

**Table 53. Intel® Celeron® Processor PPGA Flexible Thermal Design Power [1, 2]**

| Processor Power (W) | Minimum $T_{CASE}$ (°C) | Maximum $T_{CASE}$ (°C) |
|---|---|---|
| 30.02 | 0 | 70 |

**NOTES:**
1. These values are specified at nominal $Vcc_{CORE}$ for the processor core.
2. These values are preliminary.

# 9. Third-Party Vendor Information

This design guide has been compiled to give an overview of important design considerations while providing sources for additional information. This chapter includes information regarding various third-party vendors who provide products to support the 810E2 chipset. The list of vendors can be used as a starting point for the designer. Intel does not endorse any one vendor, nor guarantee the availability or functionality of outside components. Contact the manufacturer for specific information regarding performance, availability, pricing and compatibility.

### Table 54. Super I/O

| Vendors | Contact | Phone |
|---|---|---|
| SMC | Dave Jenoff | (909) 244-4937 |
| National | Robert Reneau | (408) 721-2981 |
| ITE | Don Gardenhire | (512)388-7880 |
| Winbond | James Chen | (02) 27190505 - Taipei office |

### Table 55. Clock Generation

| Vendors | Contact | Phone |
|---|---|---|
| Cypress | John Wunner | 206-821-9202 x325 |
| ICS | Raju Shah | 408-925-9493 |
| IC Works | Jeff Keip | 408-922-0202, x1185 |
| IMI | Elie Ayache | 408-263-6300, x235 |
| PERICOM | Ken Buntaran | 408-435-1000 |

### Table 56. Memory Vendors

| |
|---|
| http://developer.intel.com/design/motherbd/se/se_mem.htm |

### Table 57. Voltage Regulator Vendors

| Vendors | Contact | Phone |
|---|---|---|
| Linear Tech Corp. | Stuewart Washino | 408-432-6326 |
| Celestica | Dariusz Basarab | 416-448-5841 |
| Corsair Microsystems | John Beekley | 888-222-4346 |
| Delta Electronics | Colin Weng | 886-2-6988, x233(Taiwan) |
| N. America: Delta Products Corp. | Maurice Lee | 510-770-0660, x111 |

### Table 58. Flat Panel

| Vendors | Contact | Phone |
|---|---|---|
| Silicon Images Inc | John Nelson | 408-873-3111 |

### Table 59. AC'97

| Vendors | Contact | Phone |
|---|---|---|
| Analog Devices | Dave Babicz | 781-461-3237 |
| AKM | George Hill | 408-436-8580 |
| Cirrus Logic (Crystal) | David Crowell | 512-912-3587 |
| Creative Technologies Ltd./ Ensoniq Corp. | Steve Erickson | 408-428-6600 x6945 |
| Diamond Multimedia Systems | Theresa Leonard | 360-604-1478 |
| ESS Technology | Bill Windsor | 510-492-1708 |
| Euphonics, Inc. | David Taylor | 408-554-7201 |
| IC Ensemble Inc. | Steve Allen | 408-969-0888 x106 |
| Motorola | Pat Casey | 508-261-4649 |
| PCTel, Inc. | Steve Manuel | 410-965-2172 |
| Conexant (formerly Rockwell) | Tom Eichenberg | 949-221-4164 |
| SigmaTel | Spence Jackson<br>Arron Lyman | 512-343-6636<br>512-343-6636 x11 |
| Staccato Systems | Bob Starr | 650-853-7035 |
| Tritech Microelectronics, Inc. | Rod Maier | 408-941-1360 |
| Yamaha | Jose Villafuerte (US)<br>Kazunari Fukaya (Japan) | 408-467-2300<br>(0539) 62-6081 |

### Table 60. TMDS Transmitters

| Vendors | Component | Contact | Phone |
|---|---|---|---|
| Silicon Images | SII164 | John Nelson | (408) 873- 3111 |
| Texas Instrument | TFP420 | Greg Davis (gdavis@ti.com) | (214) 480-3662 |
| Chrontel | CH7301 | Chi Tai Hong (cthong@chrontel.com) | (408) 544-2150 |

### Table 61. TV Encoders

| Vendors | Component | Contact | Phone |
|---|---|---|---|
| Chrontel | CH7007 / CH7008 | Chi Tai Hong (cthong@chrontel.com) | (408)544-2150 |
| Chrontel | CH7010 / CH7011 | Chi Tai Hong (cthong@chrontel.com) | (408)544-2150 |
| Conexant | CN870 / CN871 | Eileen Carlson (eileen.carlson@conexant.com) | (858) 713-3203 |
| Focus | FS450 / FS451 | Bill Schillhammer (billhammer@focusinfo.com) | (978) 661-0146 |
| Philips | SAA7102A | Marcus Rosin (marcus.rosin@philips.com) | None |
| Texas Instrument | TFP6022/ TFP6024 | Greg Davis (gdavis@ti.com) | (214) 480-3662 |

### Table 62. Combo TMDS Transmitters/TV Encoders

| Vendors | Component | Contact | Phone |
|---|---|---|---|
| Chrontel | CH7009/ CH7010 | Chi Tai Hong (cthong@chrontel.com) | (408) 544-2150 |
| Texas Instrument | TFP6422/ TFP6424 | Greg Davis (gdavis@ti.com) | (214) 480-3662 |

### Table 63. LVDS Transmitter

| Vendors | Component | Contact | Phone |
|---|---|---|---|
| National Semiconductor | 387R | Jason Lu (Jason.Lu@nsc.com) | (408) 721-7540 |

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# Appendix A: Intel® 810E2 Chipset Platform Reference Schematics

This appendix provides a set of schematics for Intel's 810E2 chipset platform. The feature list is shown below:

### Intel® 810E2 Chipset Reference Schematics Feature Set

- 810E2 Chipset
  - Graphics and Memory Controller Hub (GMCH)
  - I/O Controller Hub (ICH)
  - FWH Flash BIOS
- Support for the Celeron or Pentium III processor (66/100/133 MHz System Bus Frequency)
- Debug Port
- Synchronous SDRAM Memory Interface
  - 100 MHz SDRAM Support
  - 2 DIMM Sockets
- 4 MB Display Cache (133 MHz)
- PCI 2.2 interface
  - 6 REQ#/GNT# pairs
- Integrated LAN controller
- Bus master IDE controller: supports Ultra ATA/100
- USB controller
- I/O APIC
- LPC Interface
- AC'97 2.1 Interface
- FWH interface
- Integrated System Management controller
- Intel On-board VRM (VRM 8.4, Rev 1.5 Compliant)
- 4-Layer Design

# INTEL® PENTIUM® III & INTEL® CELERON (TM) PROCESSOR (PGA370) / INTEL® 810E2 CHIPSET

## UNIPROCESSOR CUSTOMER REFERENCE SCHEMATICS

REVISION 1.0

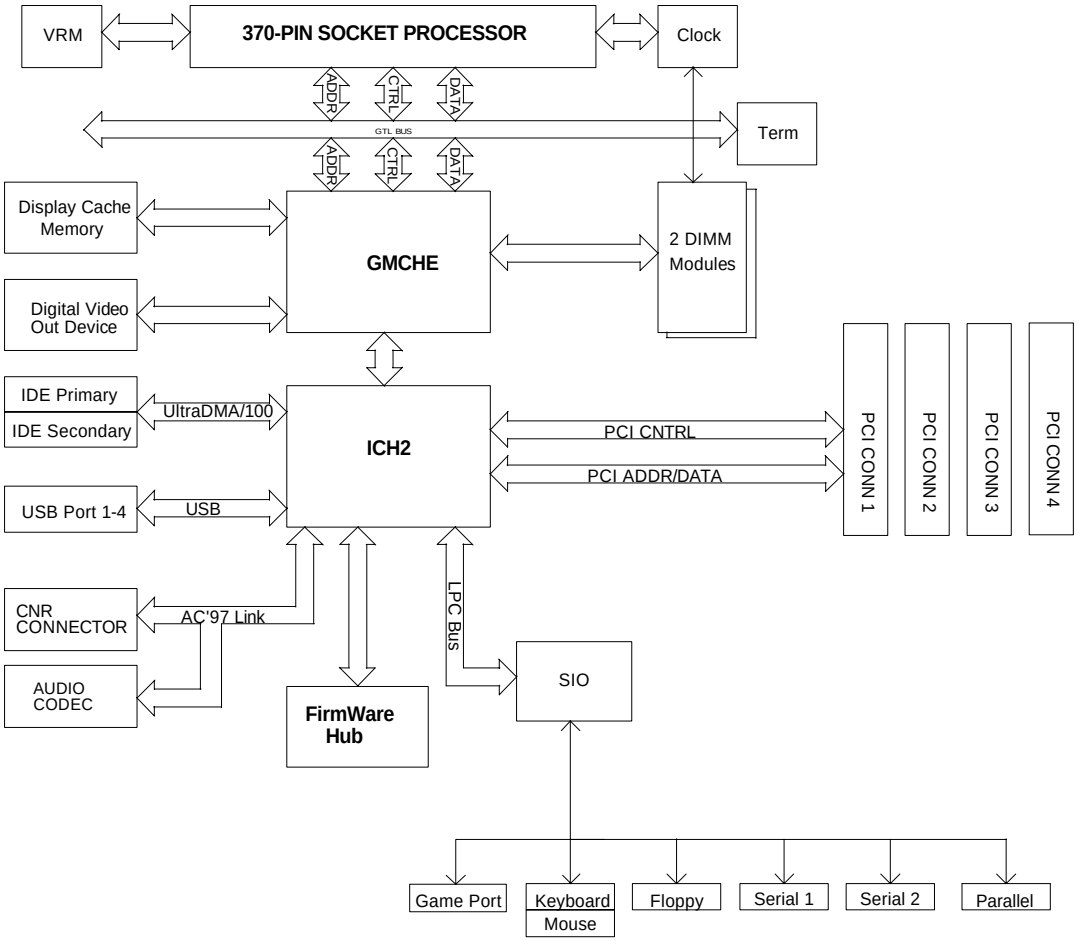


** Please note these schematics are subject to change.

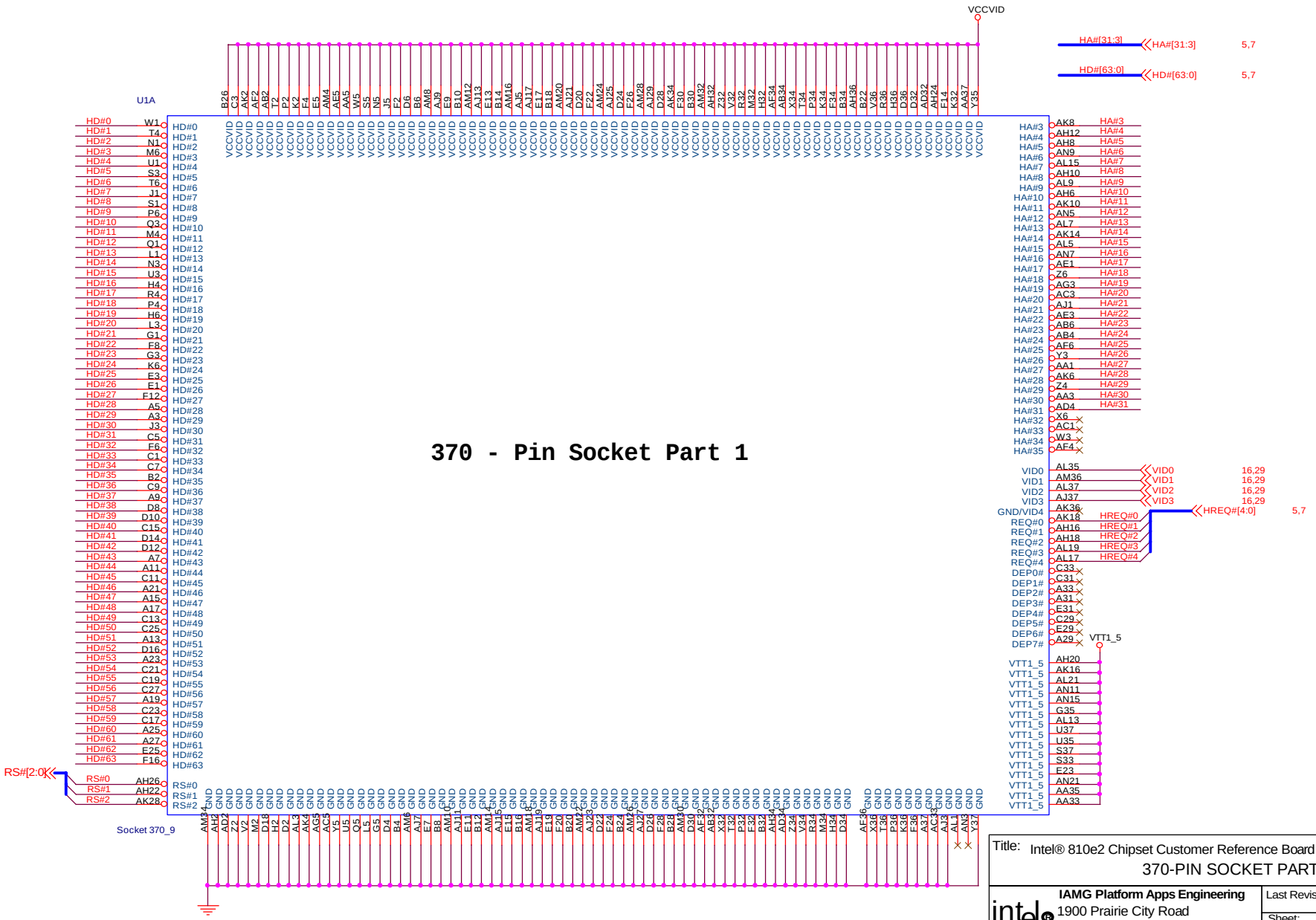


| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>Cover Sheet | | REV.<br>1.0 |
| IAMG Platform Apps Engineering<br>1900 Prairie City Road<br>Folsom, Ca. 95630 | Last Revision Date: 10/24/00<br>Sheet: 1 of 34 | |

# Block Diagram




| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board Block Diagram | | REV. 1.0 |
| IAMG Platform Apps Engineering<br>1900 Prairie City Road<br>Folsom, Ca. 95630 | Last Revision Date: 10/24/00 | Sheet: 2 of 34 |




| | |
|---|---|
| Title: | Intel® 810e2 Chipset Customer Reference Board<br>370-PIN SOCKET PART 1 |
| REV. | 1.0 |
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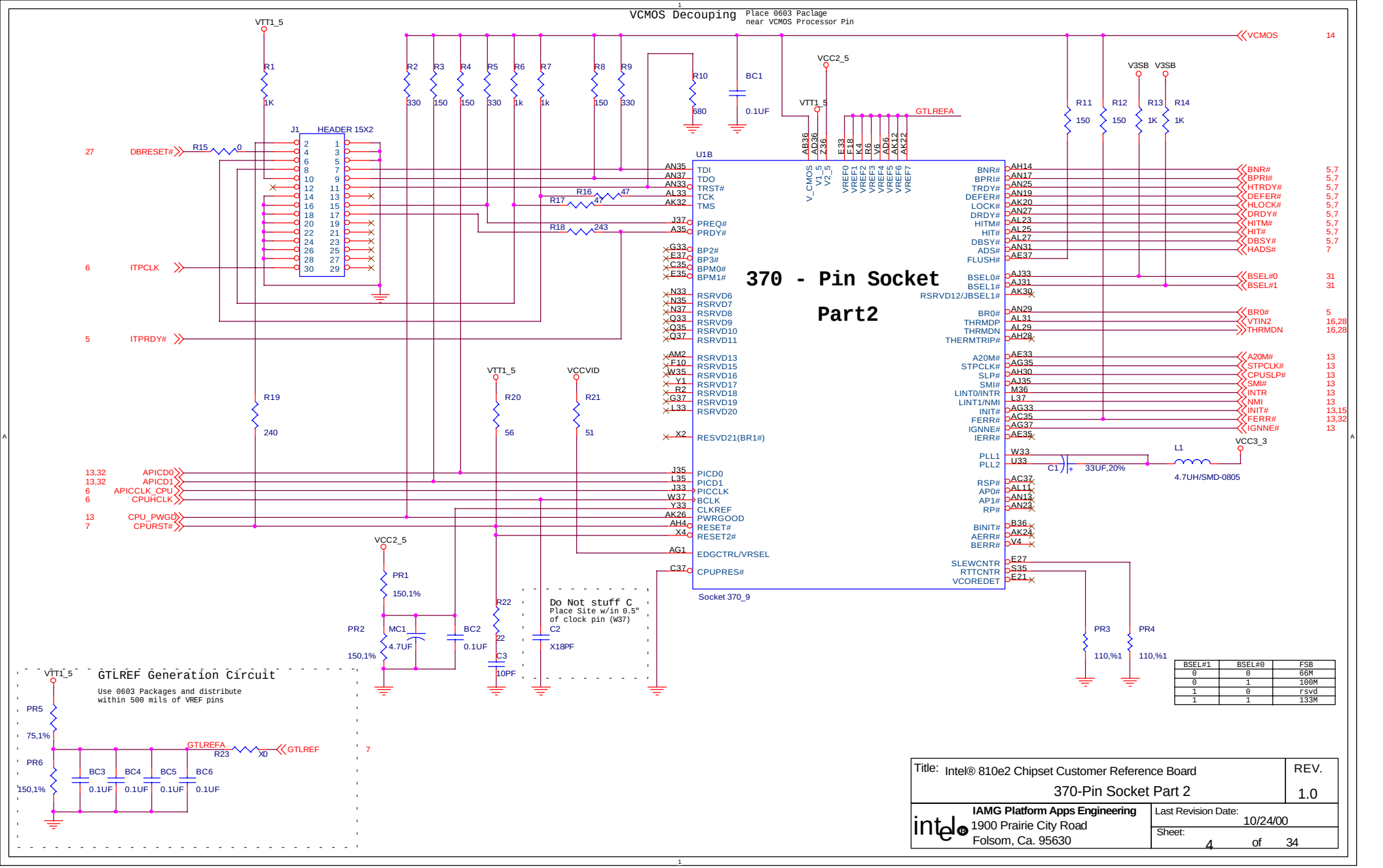
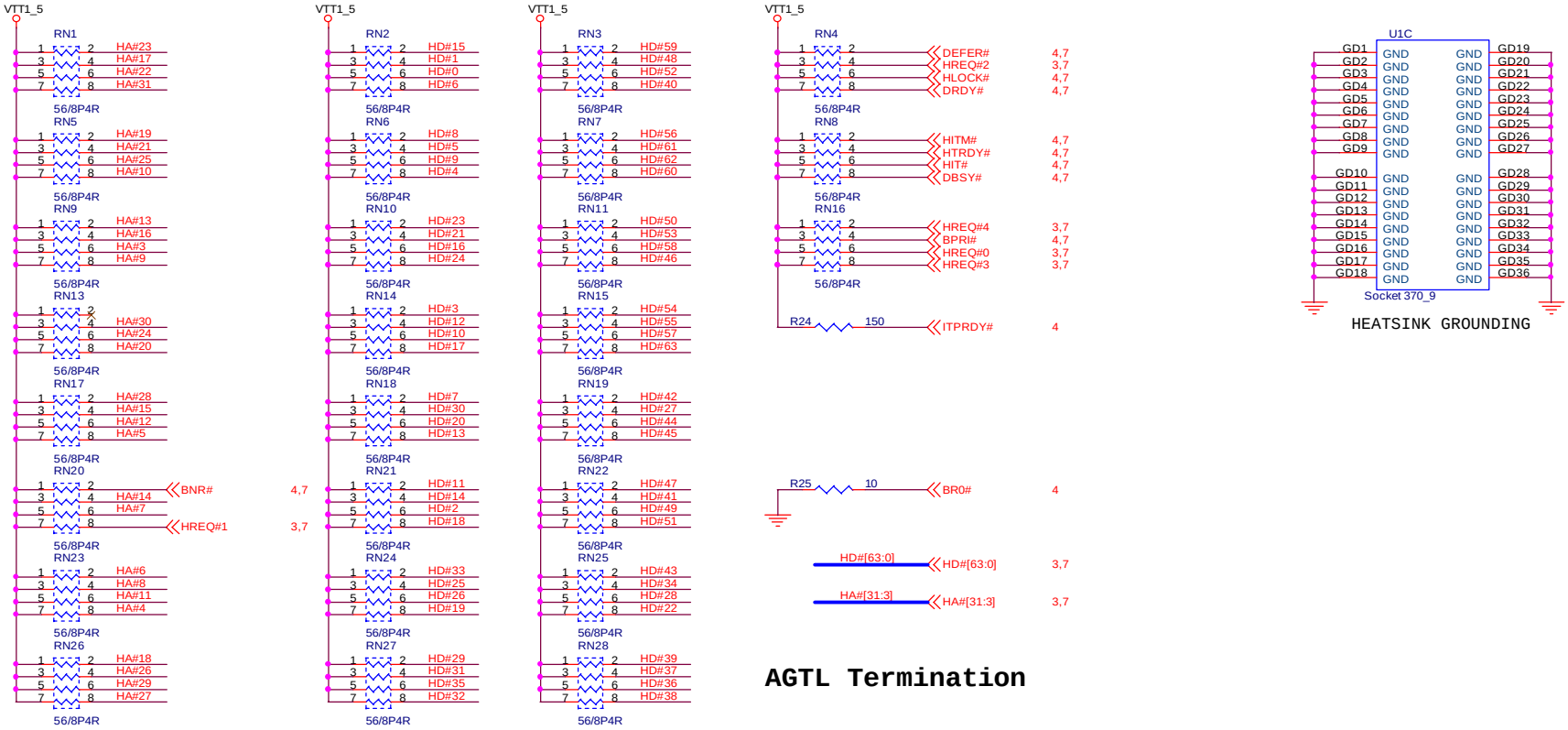



| | |
|---|---|
| Title: | Intel® 810e2 Chipset Customer Reference Board<br>370-Pin Socket Part 2 |
| REV. | 1.0 |
| IAMG Platform Apps Engineering<br>1900 Prairie City Road<br>Folsom, Ca. 95630 | Last Revision Date: 10/24/00<br>Sheet: 4 of 34 |




| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>AGTL TERMINATION | | REV. 1.0 |
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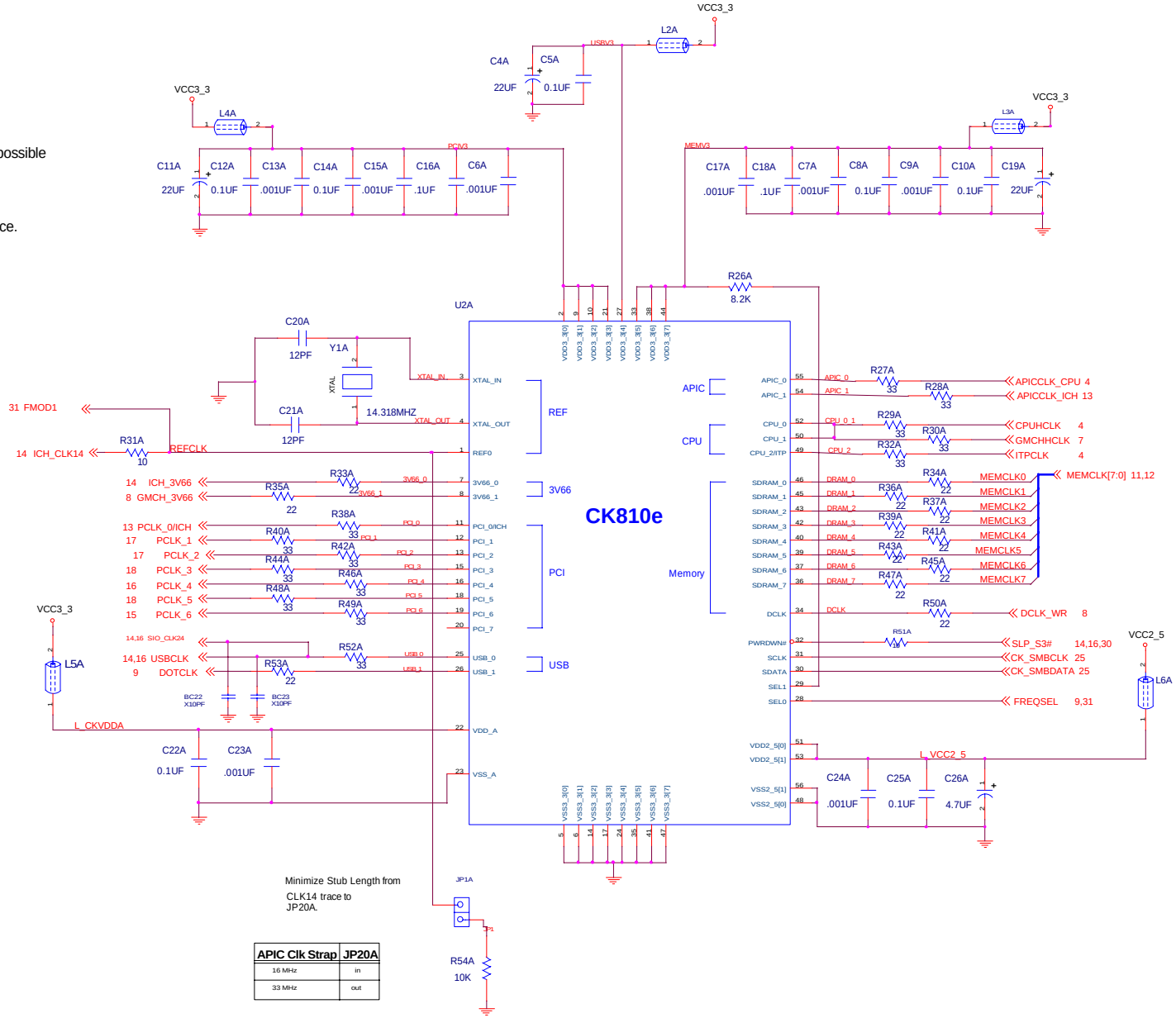
| | Sheet: 5 of 34 | |

# Clock Synthesizer

## Notes:

- Place all decoupling caps as close to VCC/GND pins as possible
- PCI_0/ICH pin has to go to the ICH.
  (This clock cannot be turned off through SMBus)
- CPU_ITP pin must go to the ITP. It is the only
  CPU CLK that can be shut off through the SMBUS interface.




| Title: Intel® 810e2 Chipset Customer Reference Board<br>Clock Synthesizer | REV. 1.0 |
|---|---|
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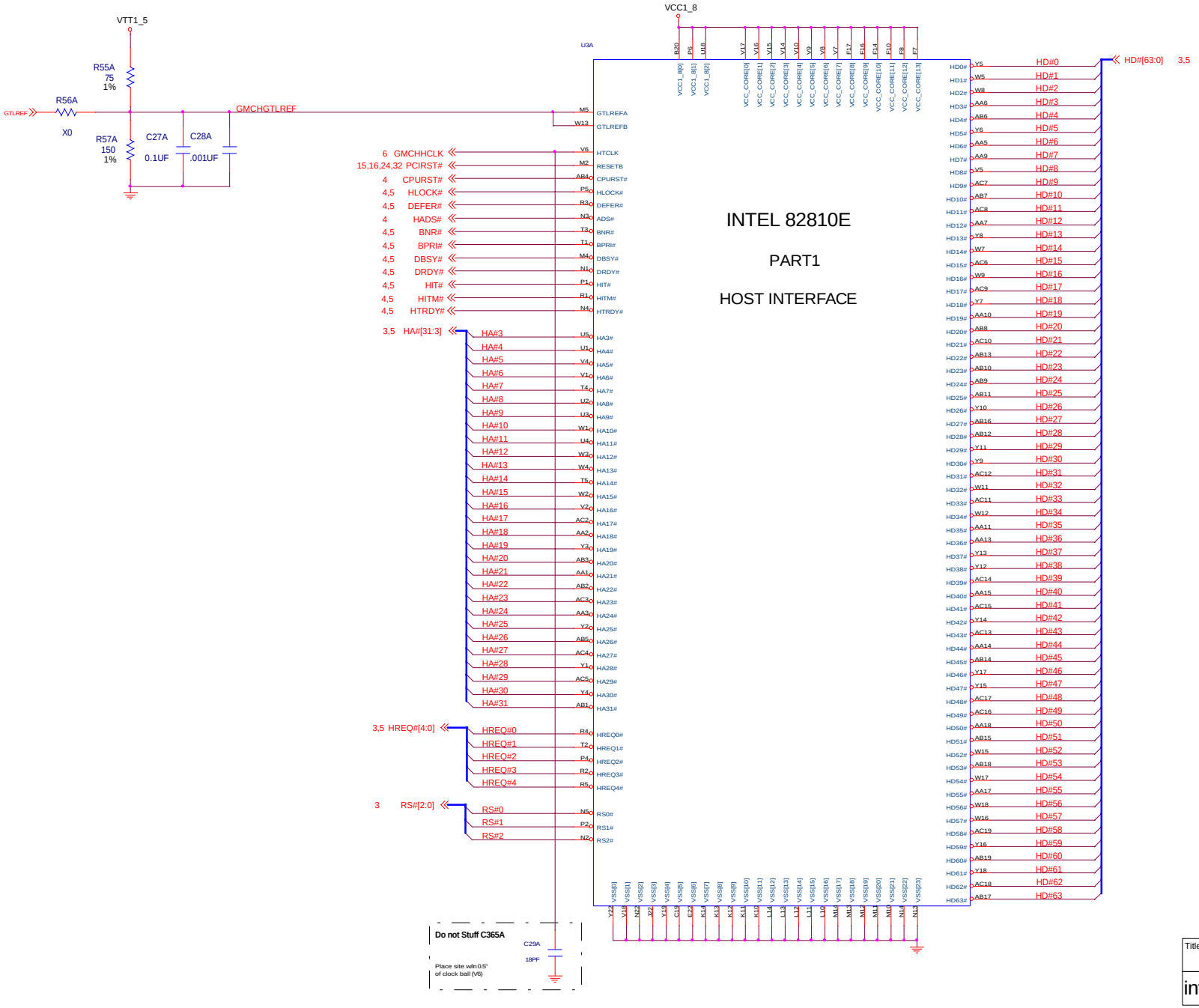
# 82810E, PART 1: HOST INTERFACE




| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>82810E, Part 1: Host Interface | | REV. 1.0 |
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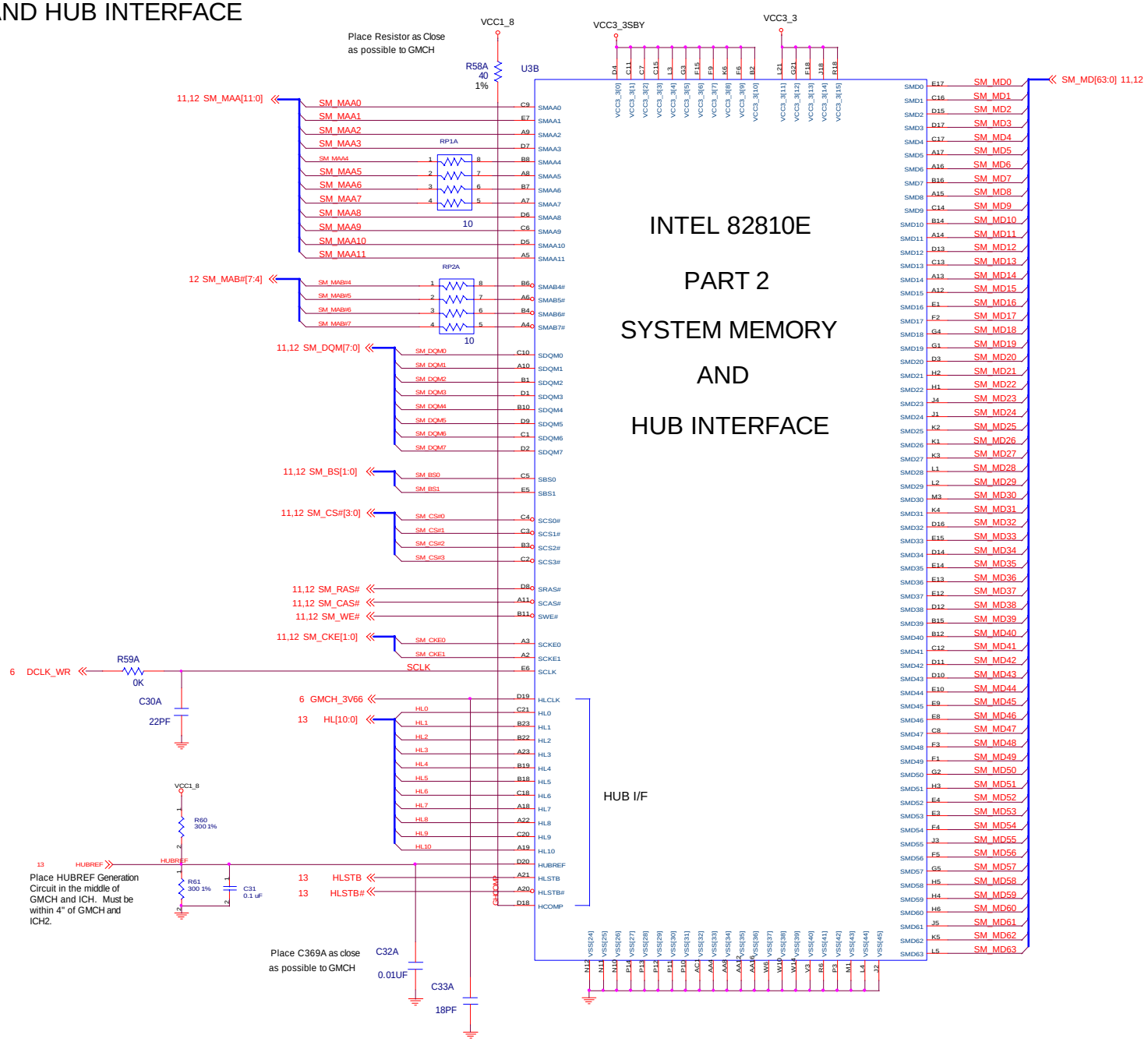
# 82810E, PART 2: SYSTEM MEMORY AND HUB INTERFACE




| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>82810E, Part 2: System Memory and Hub | | REV. 1.0 |
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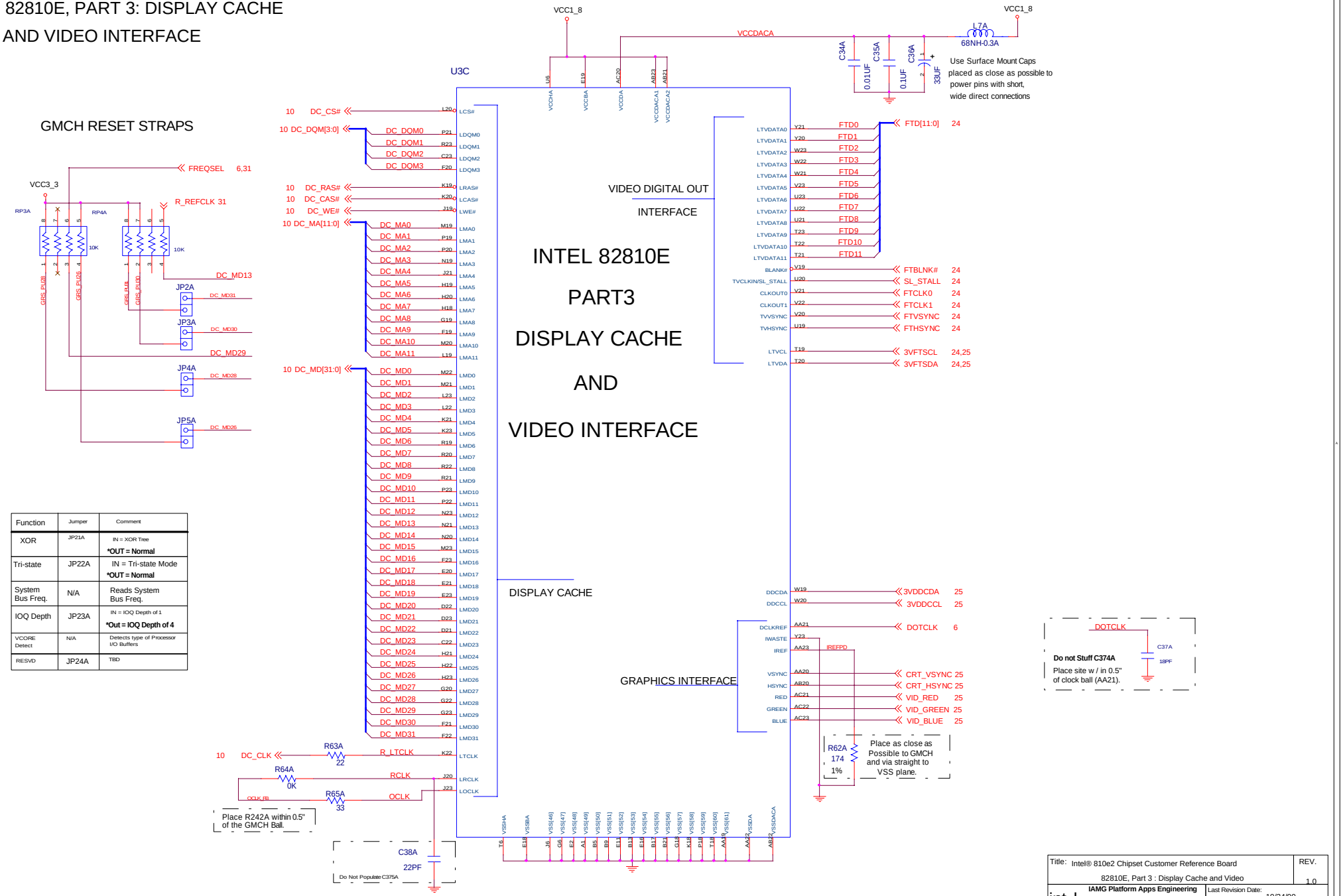
# 82810E, PART 3: DISPLAY CACHE AND VIDEO INTERFACE




| Function | Jumper | Comment |
|---|---|---|
| XOR | JP21A | IN = XOR Tree<br>*OUT = Normal |
| Tri-state | JP22A | IN = Tri-state Mode<br>*OUT = Normal |
| System Bus Freq. | N/A | Reads System Bus Freq. |
| IOQ Depth | JP23A | IN = IOQ Depth of 1<br>*Out = IOQ Depth of 4 |
| VCORE Detect | N/A | Detects type of Processor I/O Buffers |
| RESVD | JP24A | TBD |

| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>82810E, Part 3 : Display Cache and Video | | REV. 1.0 |
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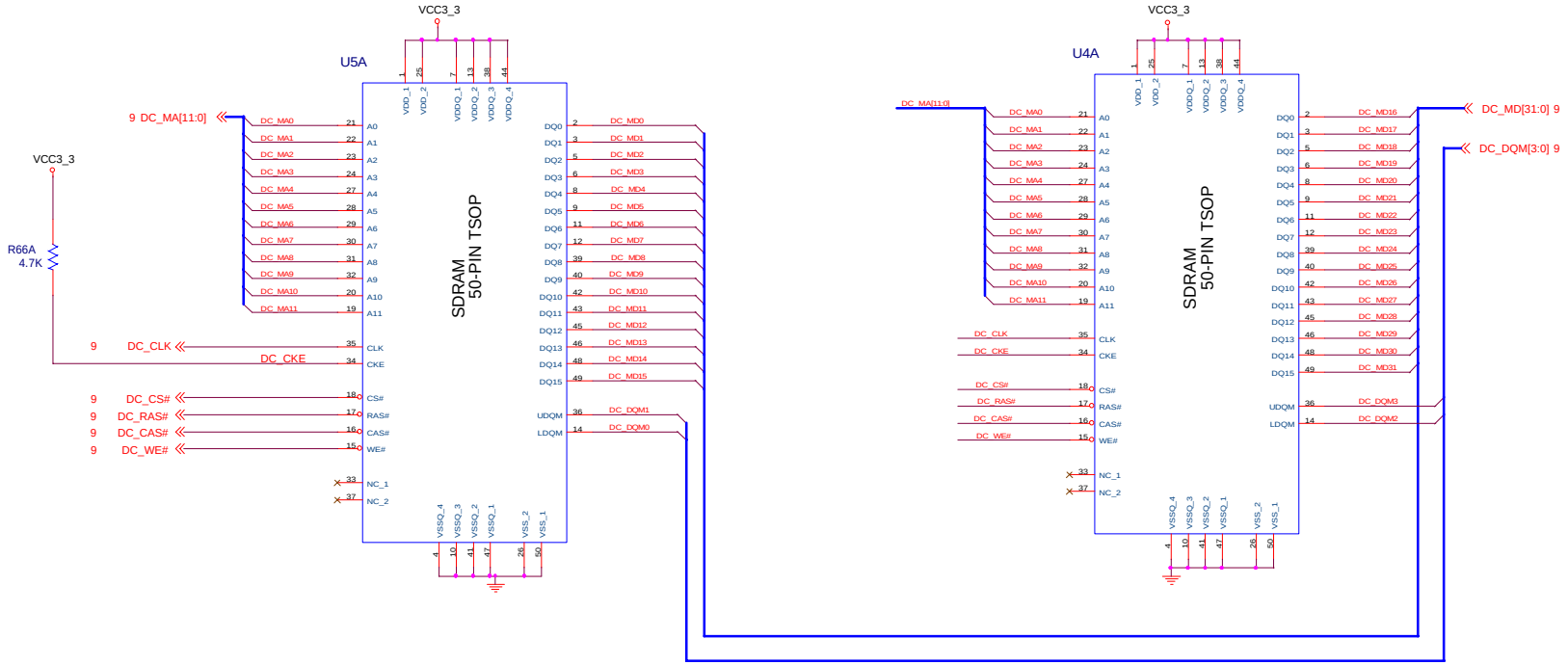
# 4MB Display Cache




| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>Display Cache | | REV. 1.0 |
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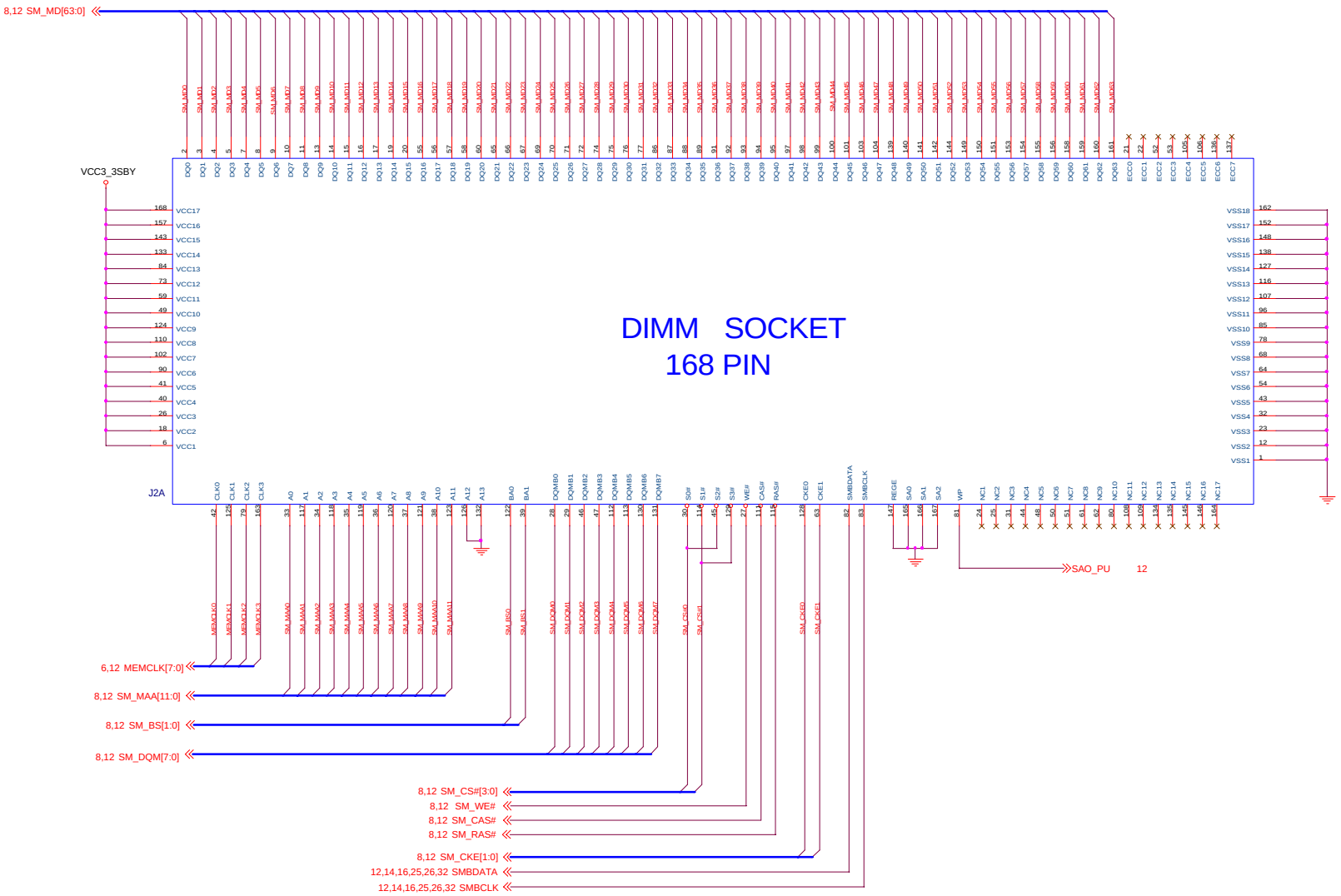
# SYSTEM MEMORY




| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board | | REV. |
| System Memory : DIMM0 | | 1.0 |
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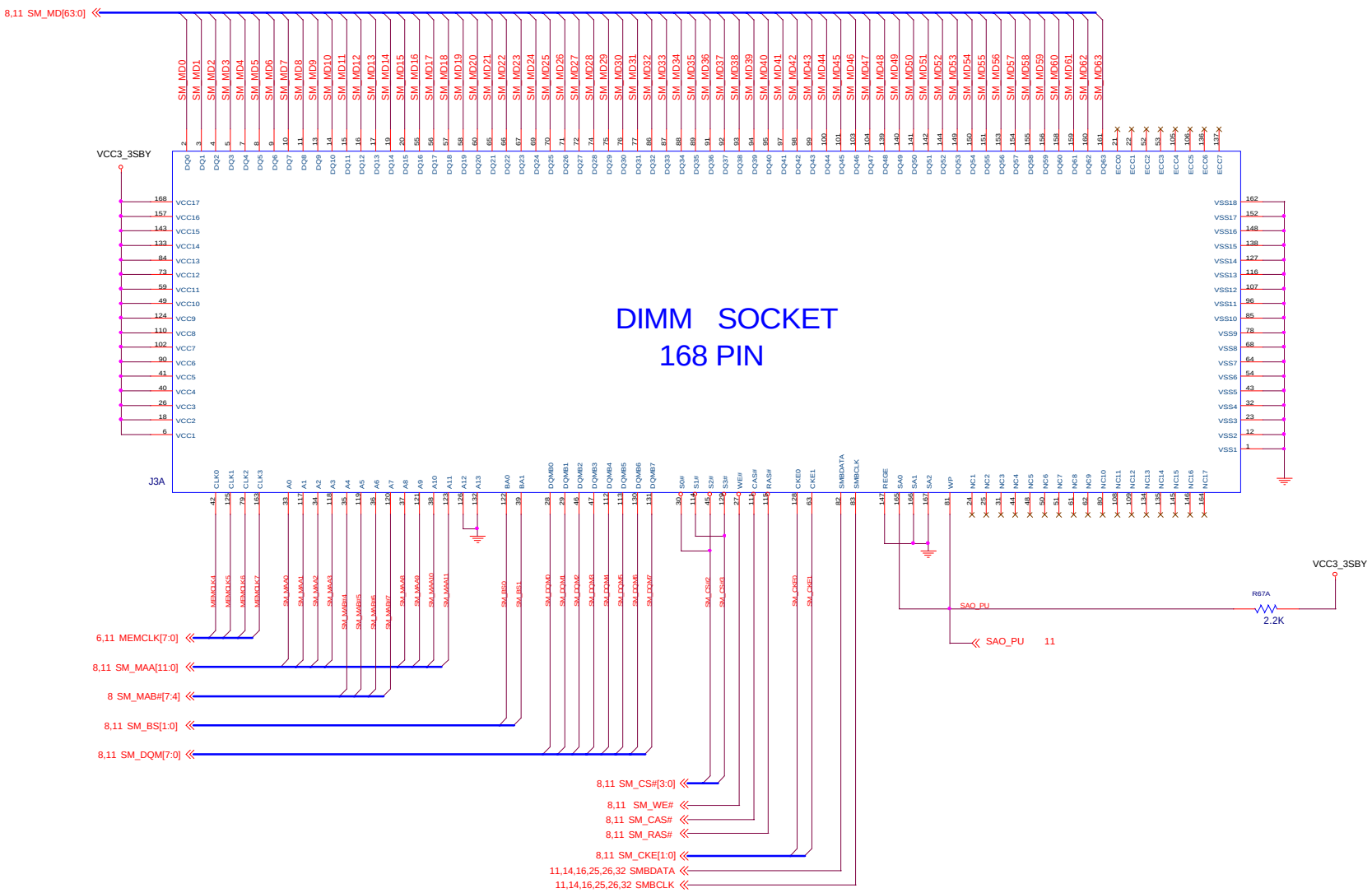
# SYSTEM MEMORY




| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>System Memory : DIMM1 | | REV. 1.0 |
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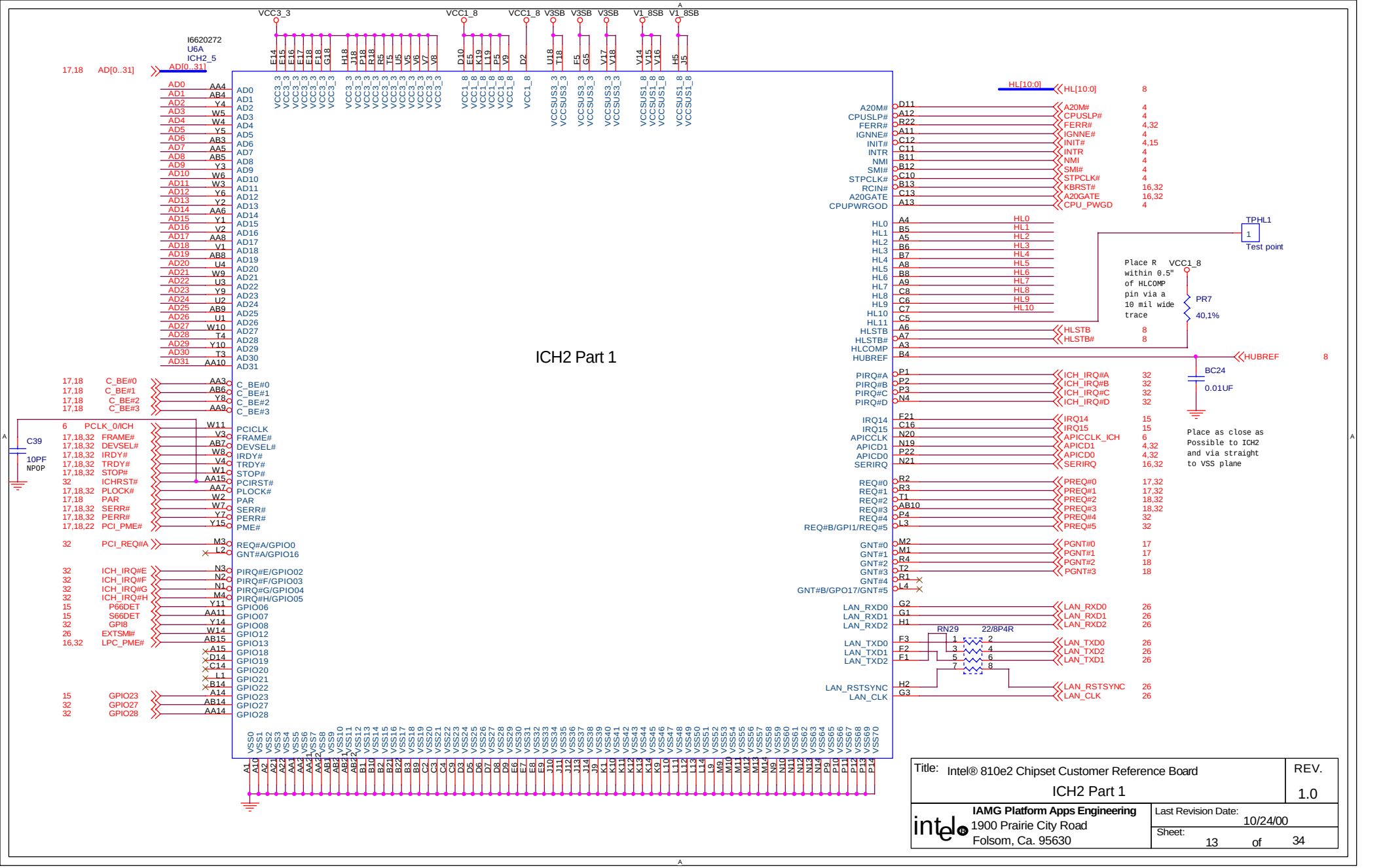
ICH2 Part 1
I6620272
U6A
ICH2_5
AD[0..31]
C39
10PF
NPOP
Place R within 0.5" of HLCOMP pin via a 10 mil wide trace
PR7
40,1%
TPHL1
Test point
BC24
0.01UF
Place as close as Possible to ICH2 and via straight to VSS plane
RN29
22/8P4R
Title: Intel® 810e2 Chipset Customer Reference Board
ICH2 Part 1
REV. 1.0
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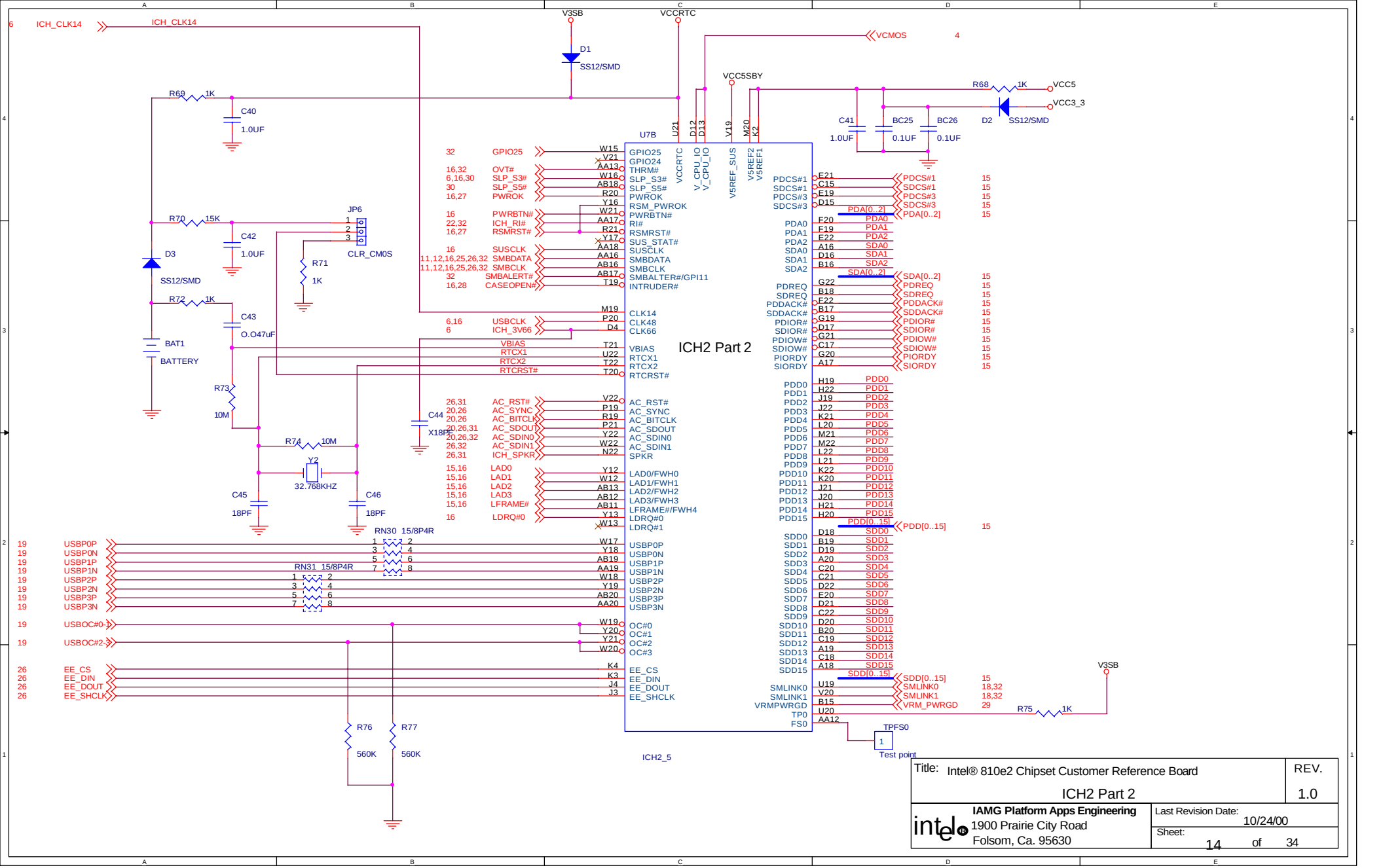
ICH_CLK14
V3SB
VCCRTC
D1
SS12/SMD
VCMOS
4
VCC5SBY
R68 1K
VCC5
VCC3_3
D2 SS12/SMD
C41 1.0UF
BC25 0.1UF
BC26 0.1UF
R69 1K
C40 1.0UF
U7B
ICH2 Part 2
R70 15K
C42 1.0UF
JP6
CLR_CM0S
R71 1K
D3 SS12/SMD
R72 1K
C43 O.O47uF
BAT1 BATTERY
R73 10M
R74 10M
Y2 32.768KHZ
C45 18PF
C46 18PF
C44 X18PF
RN30 15/8P4R
RN31 15/8P4R
USBP0P
USBP0N
USBP1P
USBP1N
USBP2P
USBP2N
USBP3P
USBP3N
USBOC#0-1
USBOC#2-3
EE_CS
EE_DIN
EE_DOUT
EE_SHCLK
R76 560K
R77 560K
R75 1K
TPFS0
Test point
ICH2_5
Title: Intel® 810e2 Chipset Customer Reference Board
ICH2 Part 2
REV. 1.0
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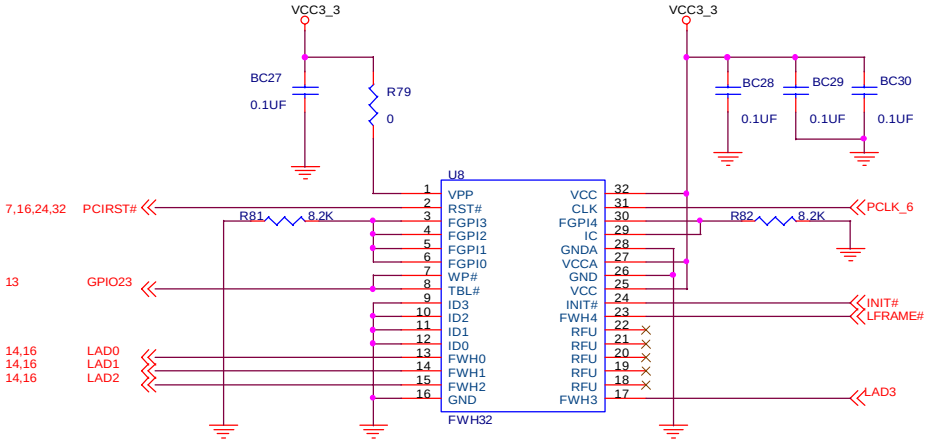
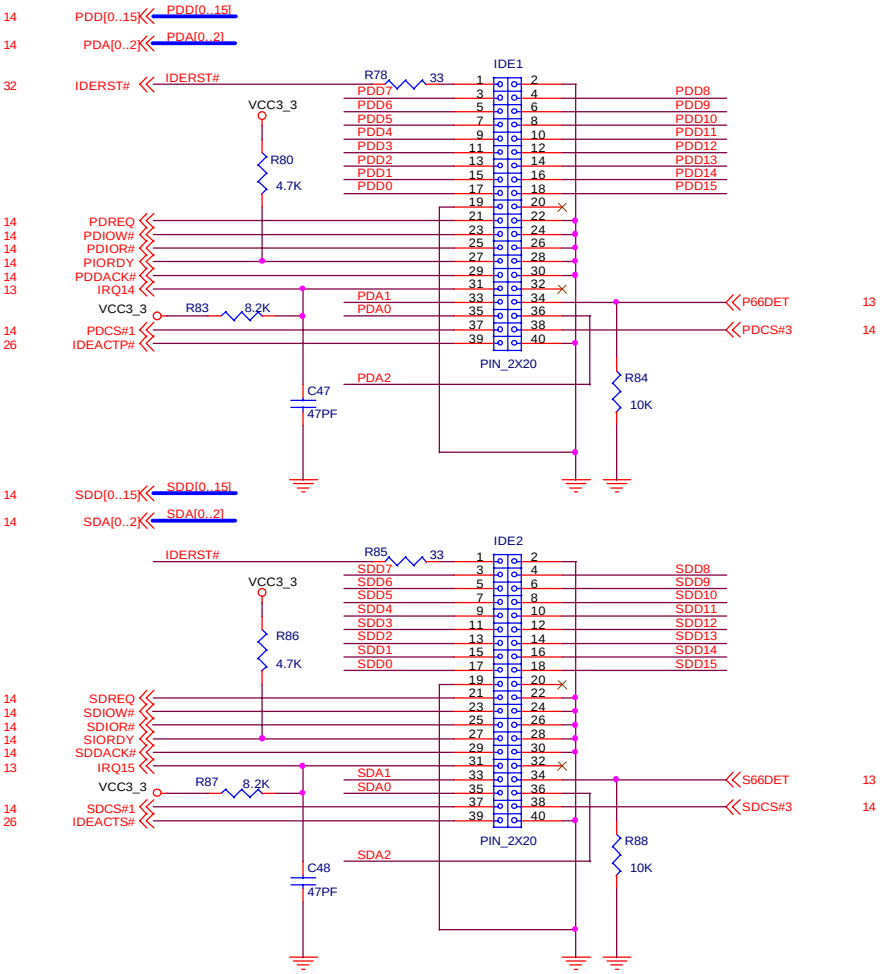
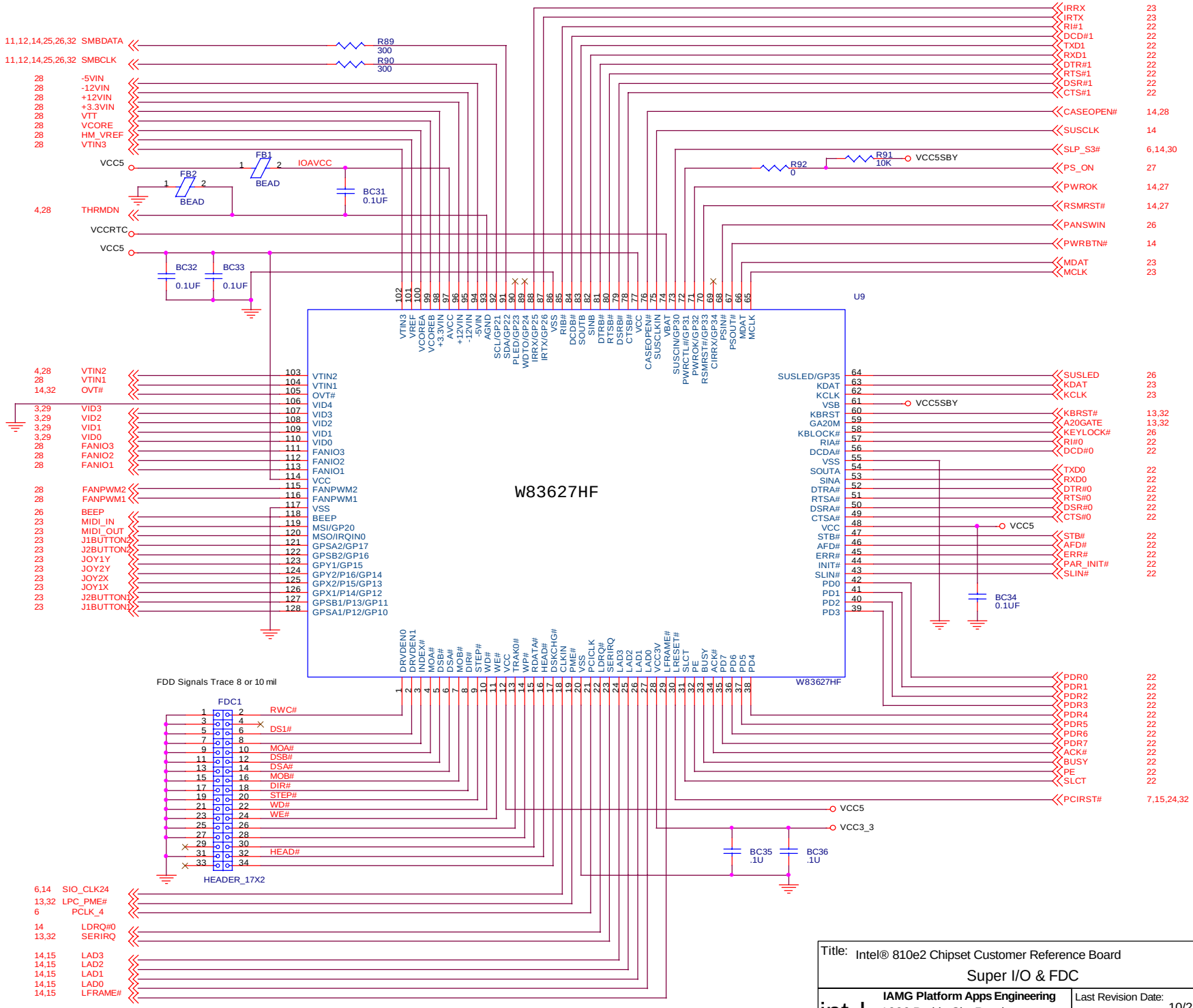
# FWH




# IDE




| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>FWH & ULTRA-ATA100 IDE connectors | | REV. 1.0 |
| intel<br>**IAMG Platform Apps Engineering**<br>1900 Prairie City Road<br>Folsom, Ca. 95630 | Last Revision Date: 10/24/00<br>Sheet: 15 of 34 | |


W83627HF
U9
R89 300
R90 300
R91 10K
R92 0
VCC5SBY
FB1 BEAD
FB2 BEAD
IOAVCC
BC31 0.1UF
BC32 0.1UF
BC33 0.1UF
BC34 0.1UF
BC35 .1U
BC36 .1U
VCC5
VCC3_3
FDD Signals Trace 8 or 10 mil
FDC1
HEADER_17X2
Title: Intel® 810e2 Chipset Customer Reference Board
Super I/O & FDC
REV. 1.0
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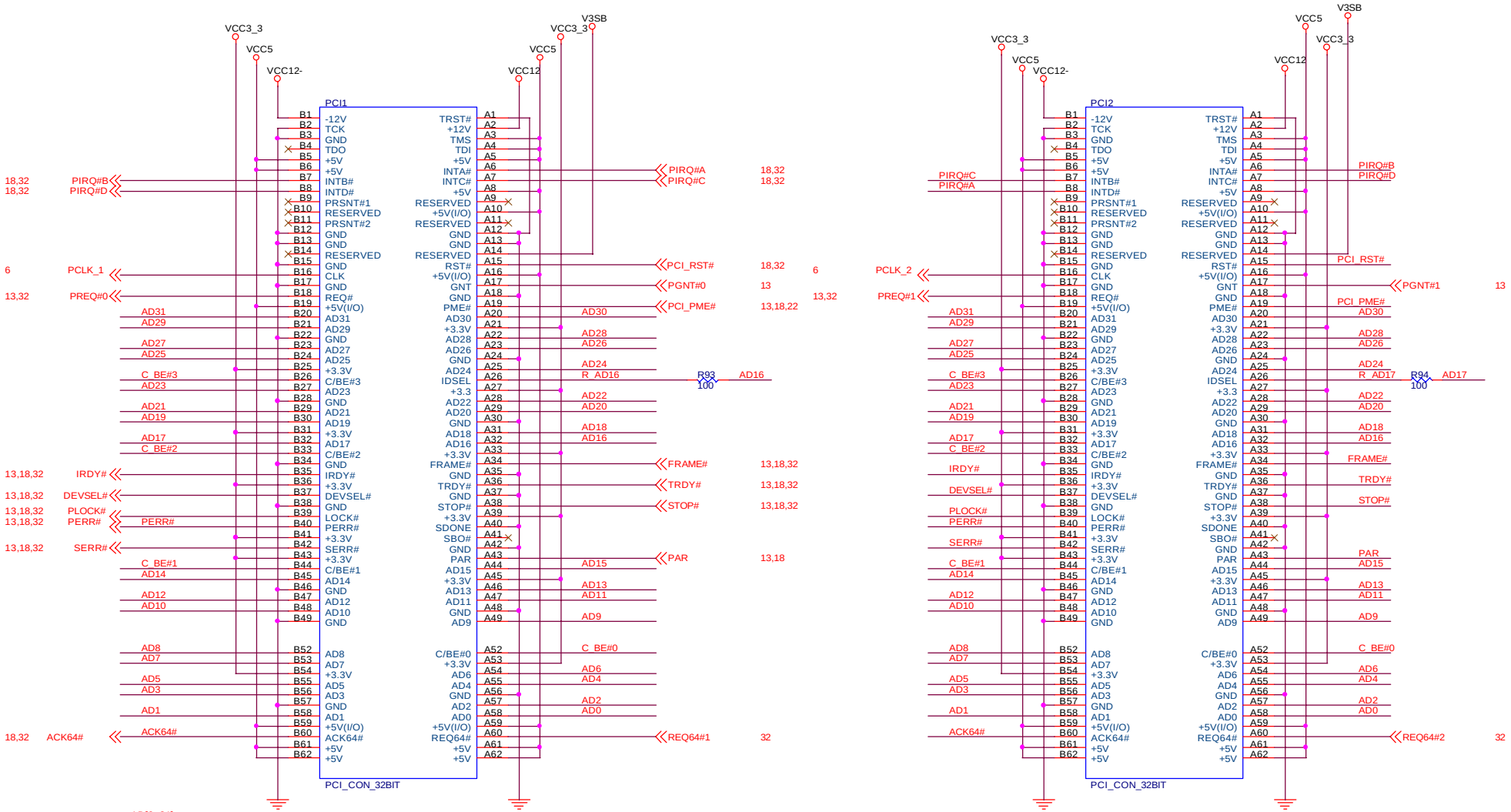


| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>PCI 1 & 2 | | REV. 1.0 |
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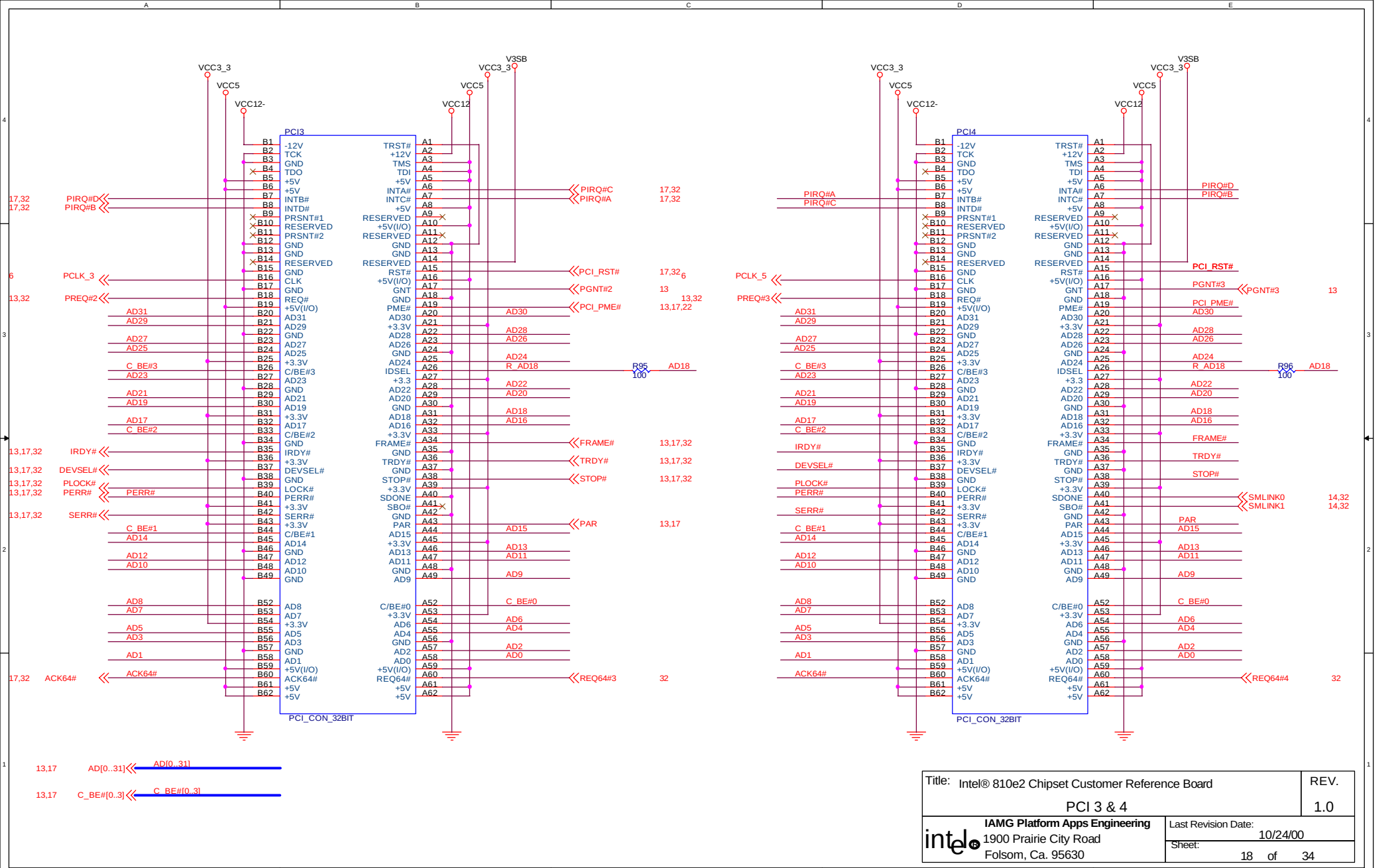
| | Sheet: 17 of 34 | |


PCI3
PCI4
PCI_CON_32BIT
VCC3_3
VCC5
VCC12-
VCC12
V3SB
PIRQ#D
PIRQ#B
PIRQ#C
PIRQ#A
PCLK_3
PCLK_5
PREQ#2
PREQ#3
PCI_RST#
PGNT#2
PGNT#3
PCI_PME#
R_AD18
R95
R96
100
IRDY#
DEVSEL#
PLOCK#
PERR#
SERR#
FRAME#
TRDY#
STOP#
PAR
SMLINK0
SMLINK1
ACK64#
REQ64#3
REQ64#4
AD[0..31]
C_BE#[0..3]
Title: Intel® 810e2 Chipset Customer Reference Board
PCI 3 & 4
REV.
1.0
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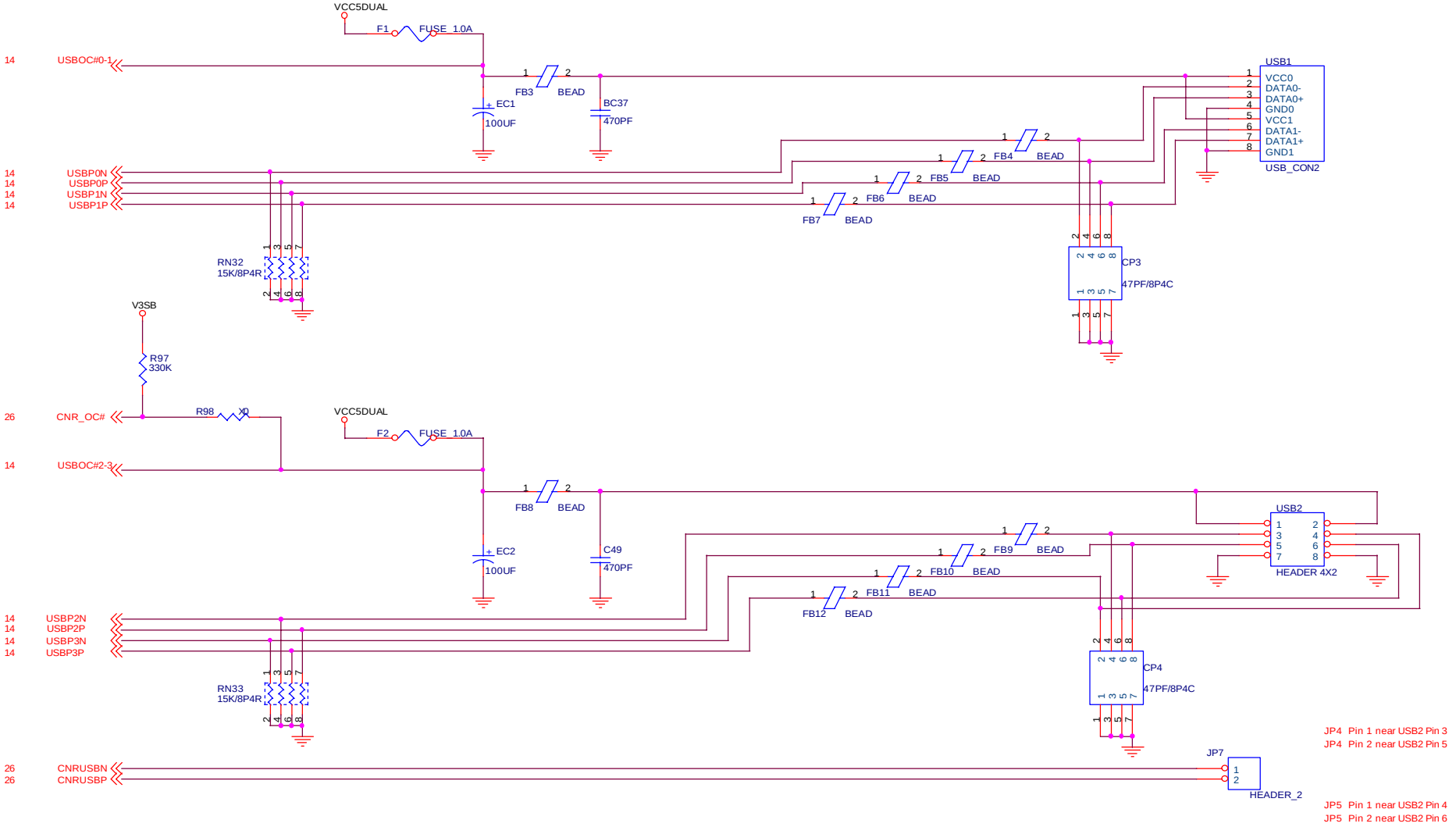
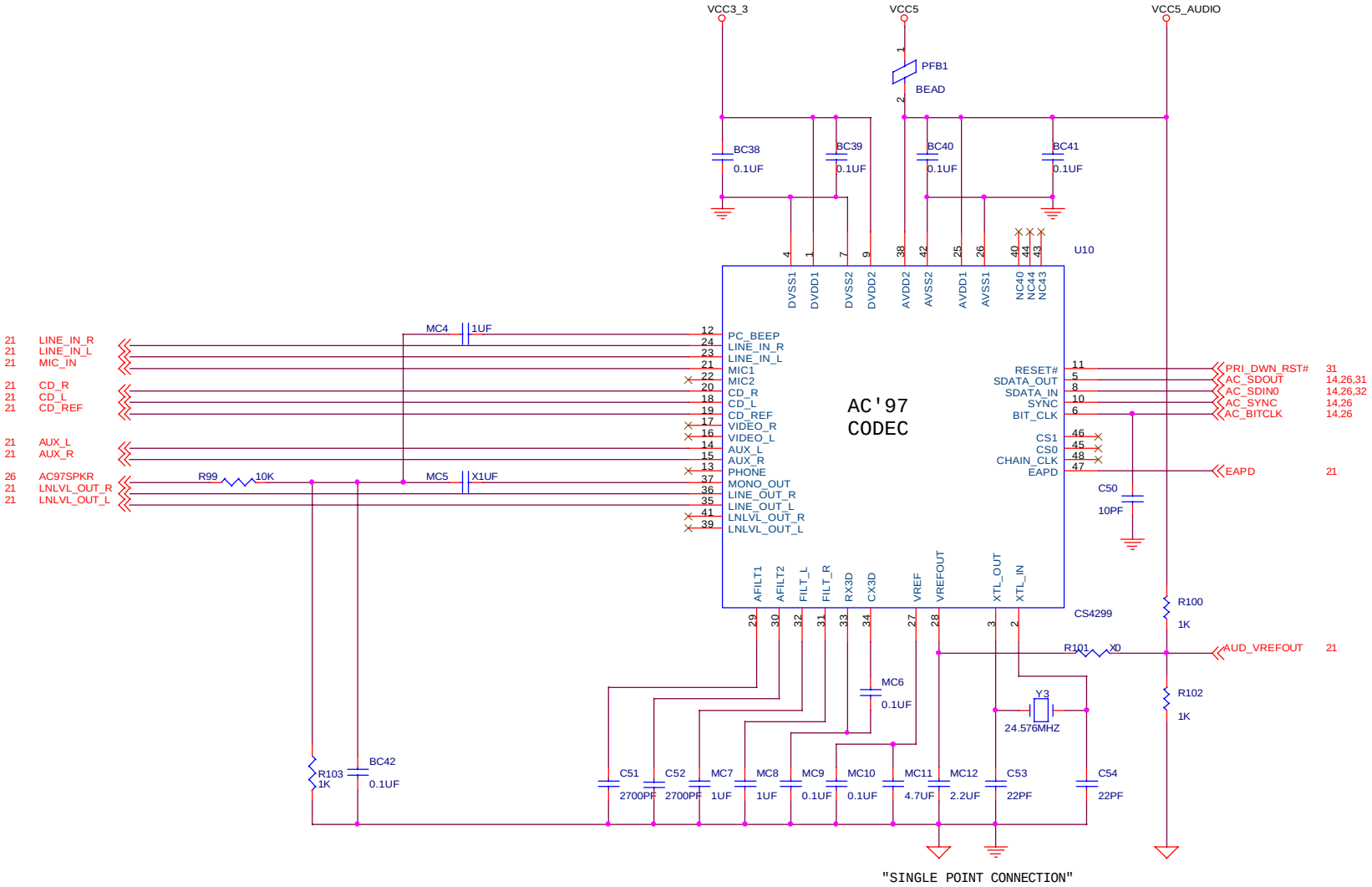
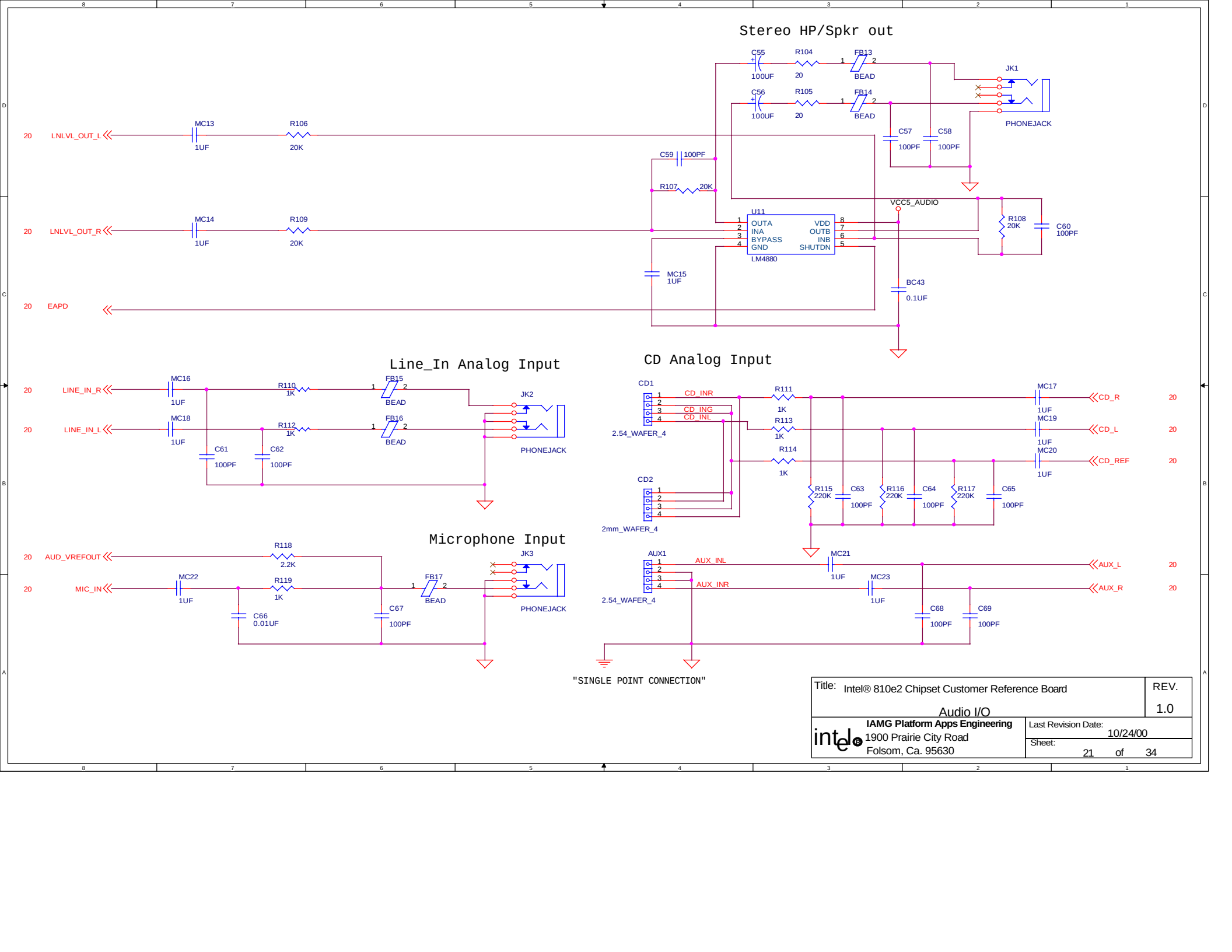



| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>USB 0-3 | | REV. 1.0 |
| intel<br>**IAMG Platform Apps Engineering**<br>1900 Prairie City Road<br>Folsom, Ca. 95630 | Last Revision Date: 10/24/00 | |
| | Sheet: 19 of 34 | |




| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>AC97 CODEC | | REV. 1.0 |
| intel<br>**IAMG Platform Apps Engineering**<br>1900 Prairie City Road<br>Folsom, Ca. 95630 | Last Revision Date: 10/24/00<br>Sheet: 20 of 34 | |


Stereo HP/Spkr out
LNLVL_OUT_L
LNLVL_OUT_R
EAPD
MC13
MC14
MC15
1UF
R106
R109
20K
C55
C56
100UF
R104
R105
20
FB13
FB14
BEAD
JK1
PHONEJACK
C57
C58
100PF
C59
R107
U11
OUTA
INA
BYPASS
GND
VDD
OUTB
INB
SHUTDN
LM4880
VCC5_AUDIO
R108
C60
BC43
0.1UF
Line_In Analog Input
LINE_IN_R
LINE_IN_L
MC16
MC18
R110
R112
1K
FB15
FB16
JK2
C61
C62
CD Analog Input
CD1
CD2
CD_INR
CD_ING
CD_INL
2.54_WAFER_4
2mm_WAFER_4
R111
R113
R114
MC17
MC19
MC20
CD_R
CD_L
CD_REF
R115
R116
R117
220K
C63
C64
C65
Microphone Input
AUD_VREFOUT
MIC_IN
R118
2.2K
R119
MC22
C66
0.01UF
C67
FB17
JK3
AUX1
AUX_INL
AUX_INR
MC21
MC23
AUX_L
AUX_R
C68
C69
"SINGLE POINT CONNECTION"
Title: Intel® 810e2 Chipset Customer Reference Board
Audio I/O
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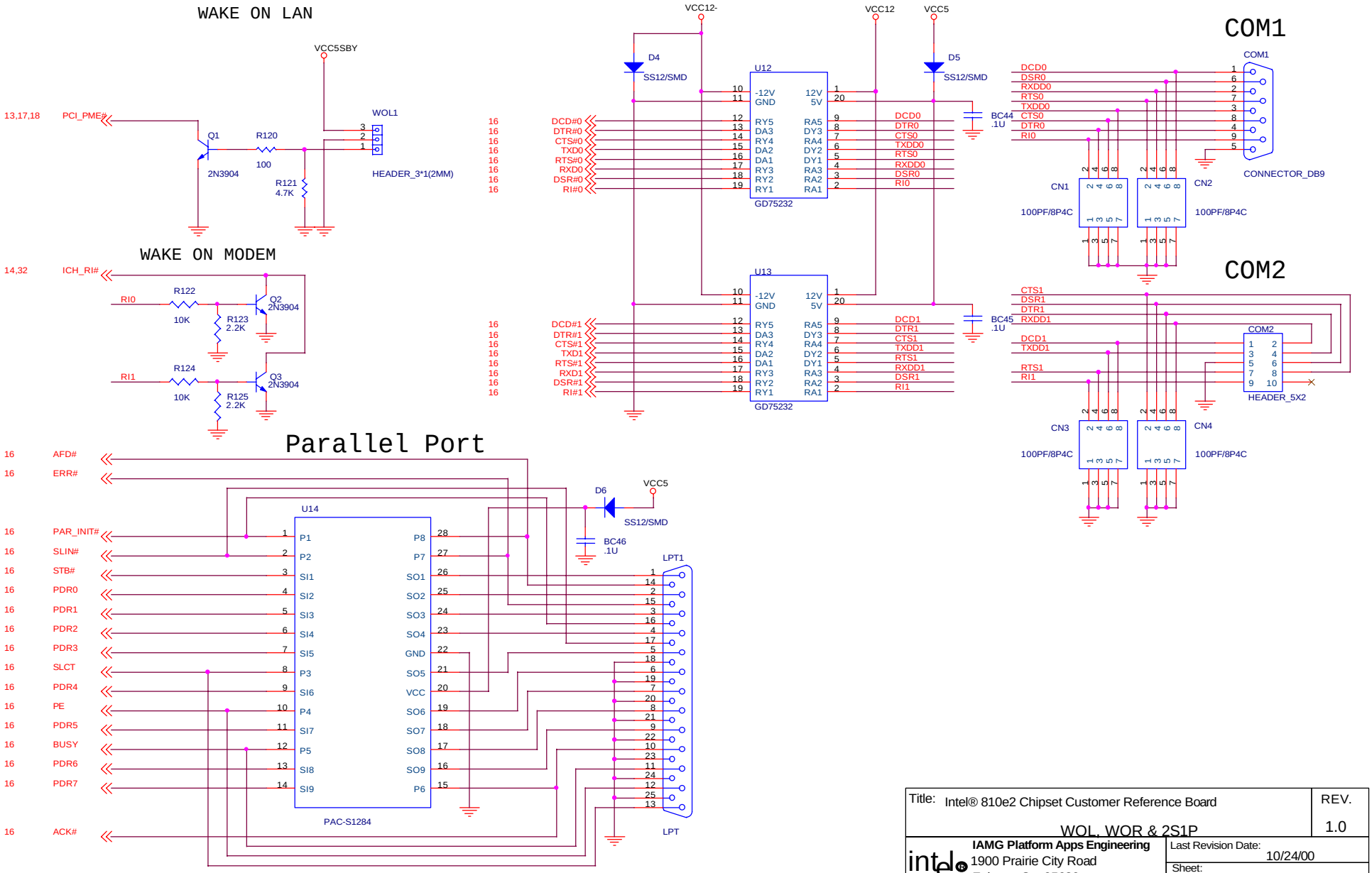
WAKE ON LAN
VCC5SBY
13,17,18
PCI_PME#
Q1
2N3904
R120
100
R121
4.7K
WOL1
HEADER_3*1(2MM)
WAKE ON MODEM
14,32
ICH_RI#
RI0
R122
10K
R123
2.2K
Q2
2N3904
RI1
R124
10K
R125
2.2K
Q3
2N3904
VCC12-
VCC12
VCC5
D4
SS12/SMD
D5
SS12/SMD
U12
-12V
GND
12V
5V
RY5
DA3
RY4
DA2
DA1
RY3
RY2
RY1
RA5
DY3
RA4
DY2
DY1
RA3
RA2
RA1
GD75232
DCD#0
DTR#0
CTS#0
TXD0
RTS#0
RXD0
DSR#0
RI#0
DCD0
DTR0
CTS0
TXDD0
RTS0
RXDD0
DSR0
RI0
BC44
.1U
U13
GD75232
DCD#1
DTR#1
CTS#1
TXD1
RTS#1
RXD1
DSR#1
RI#1
DCD1
DTR1
CTS1
TXDD1
RTS1
RXDD1
DSR1
RI1
BC45
.1U
COM1
CONNECTOR_DB9
CN1
CN2
100PF/8P4C
COM2
HEADER_5X2
CN3
CN4
100PF/8P4C
Parallel Port
16
AFD#
ERR#
PAR_INIT#
SLIN#
STB#
PDR0
PDR1
PDR2
PDR3
SLCT
PDR4
PE
PDR5
BUSY
PDR6
PDR7
ACK#
D6
SS12/SMD
VCC5
BC46
.1U
U14
P1
P2
SI1
SI2
SI3
SI4
SI5
P3
SI6
P4
SI7
P5
SI8
SI9
P8
P7
SO1
SO2
SO3
SO4
GND
SO5
VCC
SO6
SO7
SO8
SO9
P6
PAC-S1284
LPT1
LPT
Title:
Intel® 810e2 Chipset Customer Reference Board
WOL, WOR & 2S1P
REV.
1.0
IAMG Platform Apps Engineering
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Folsom, Ca. 95630
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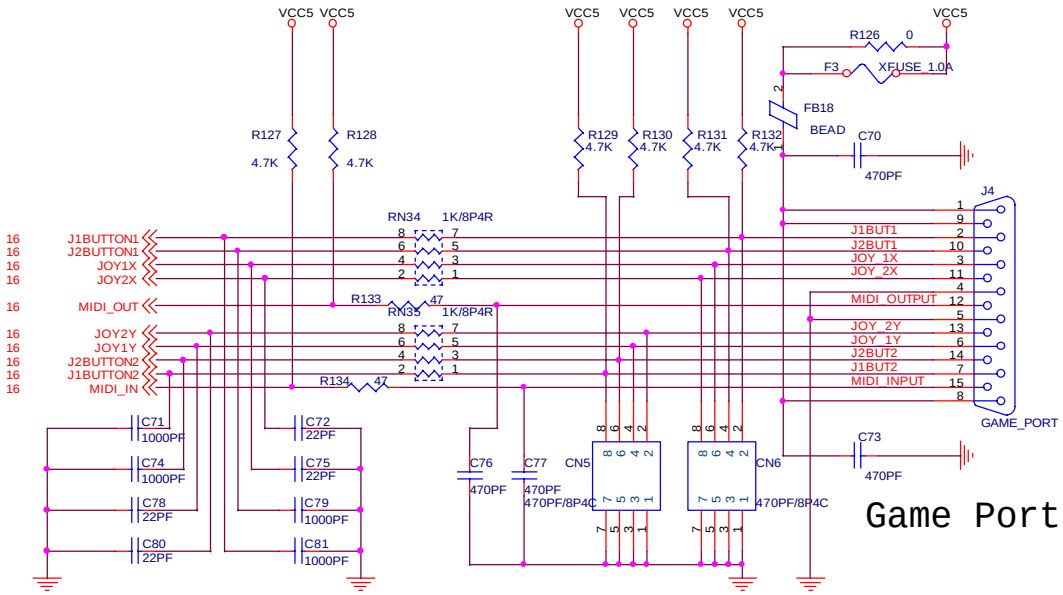


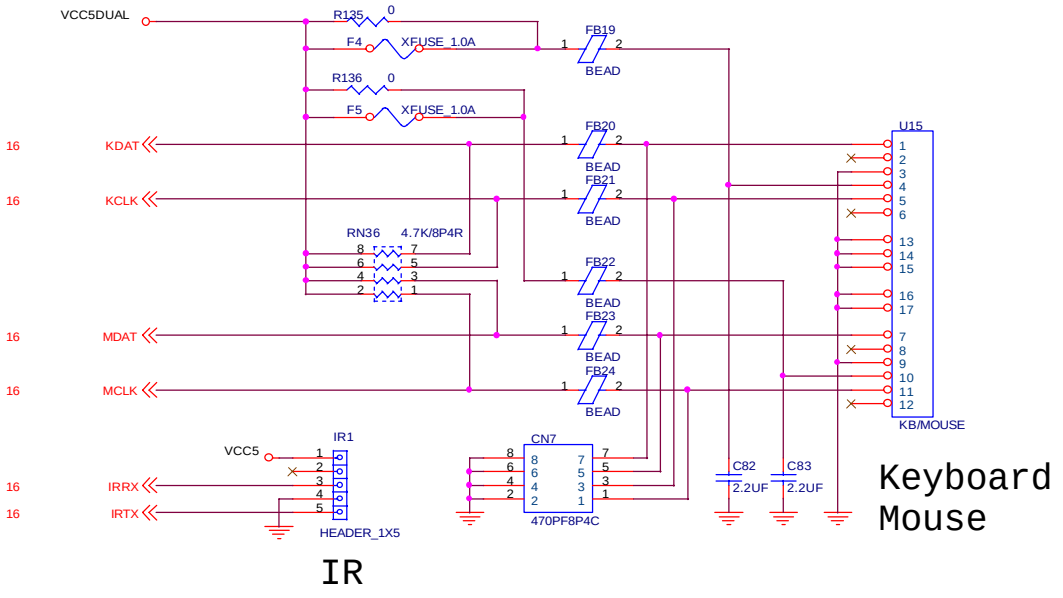


| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>Kybrd / Mse / F. Disk / Gme Connectors | | REV. 1.0 |
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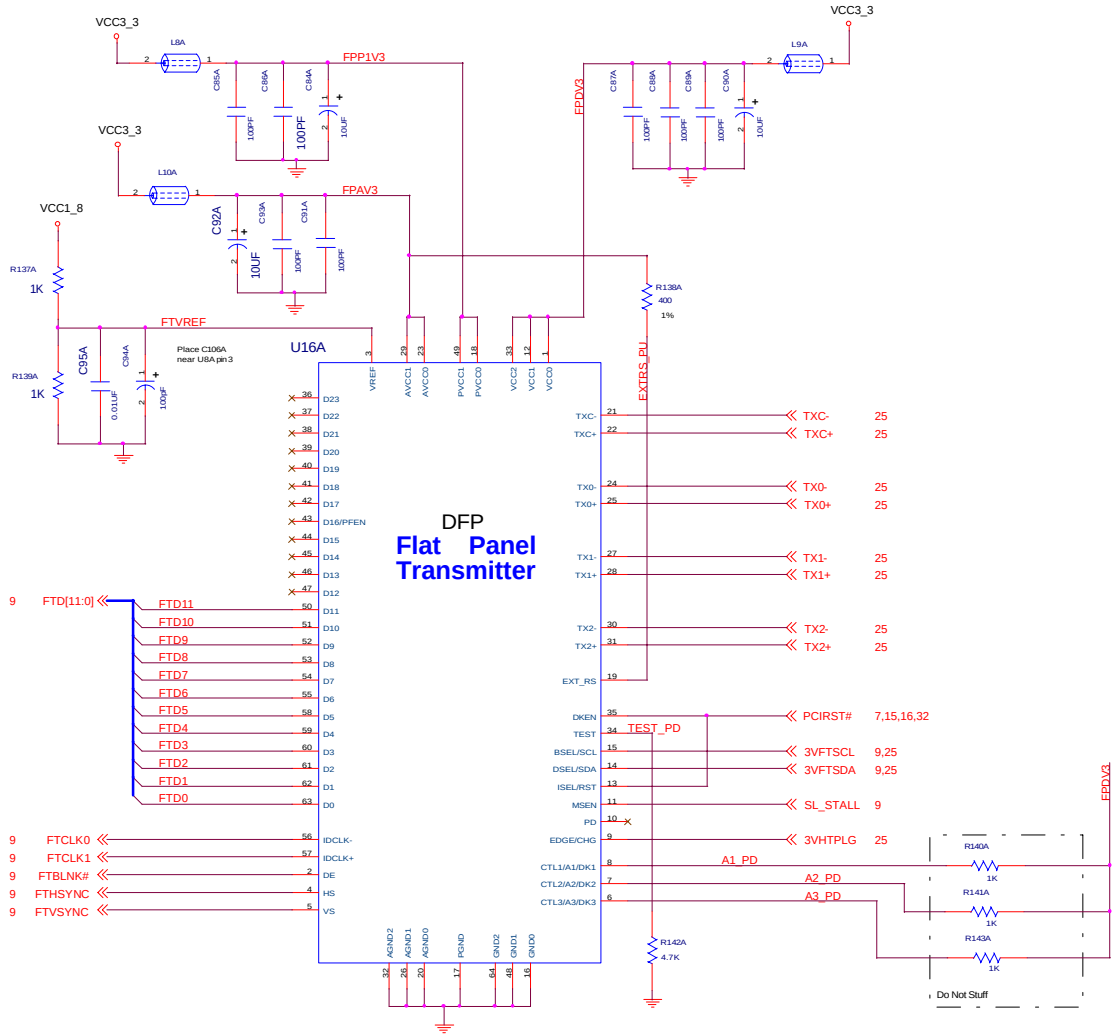
# Digital Video Out




| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>Digital Video Out | | REV. 1.0 |
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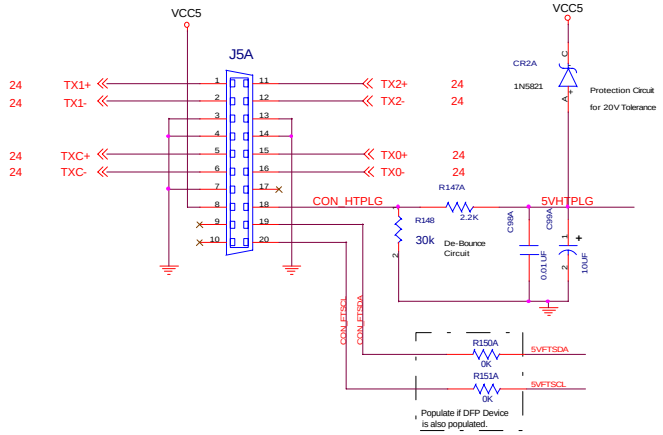
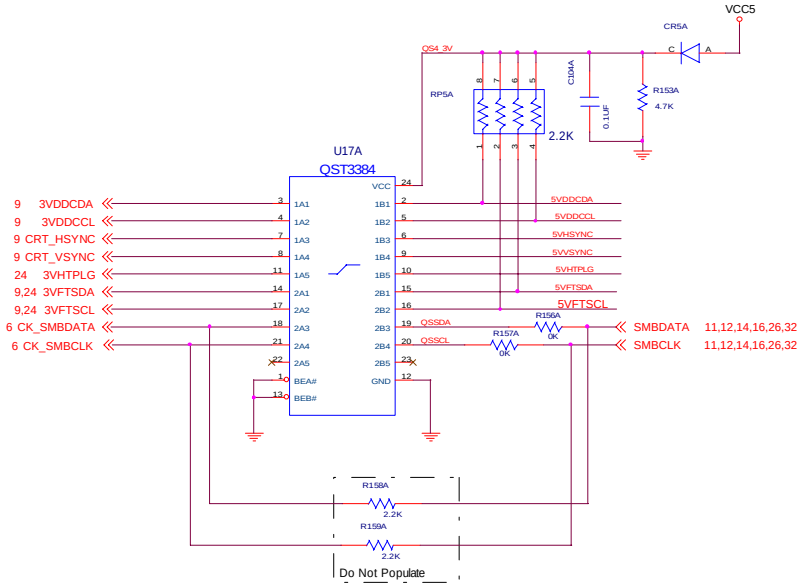
# Video Connectors

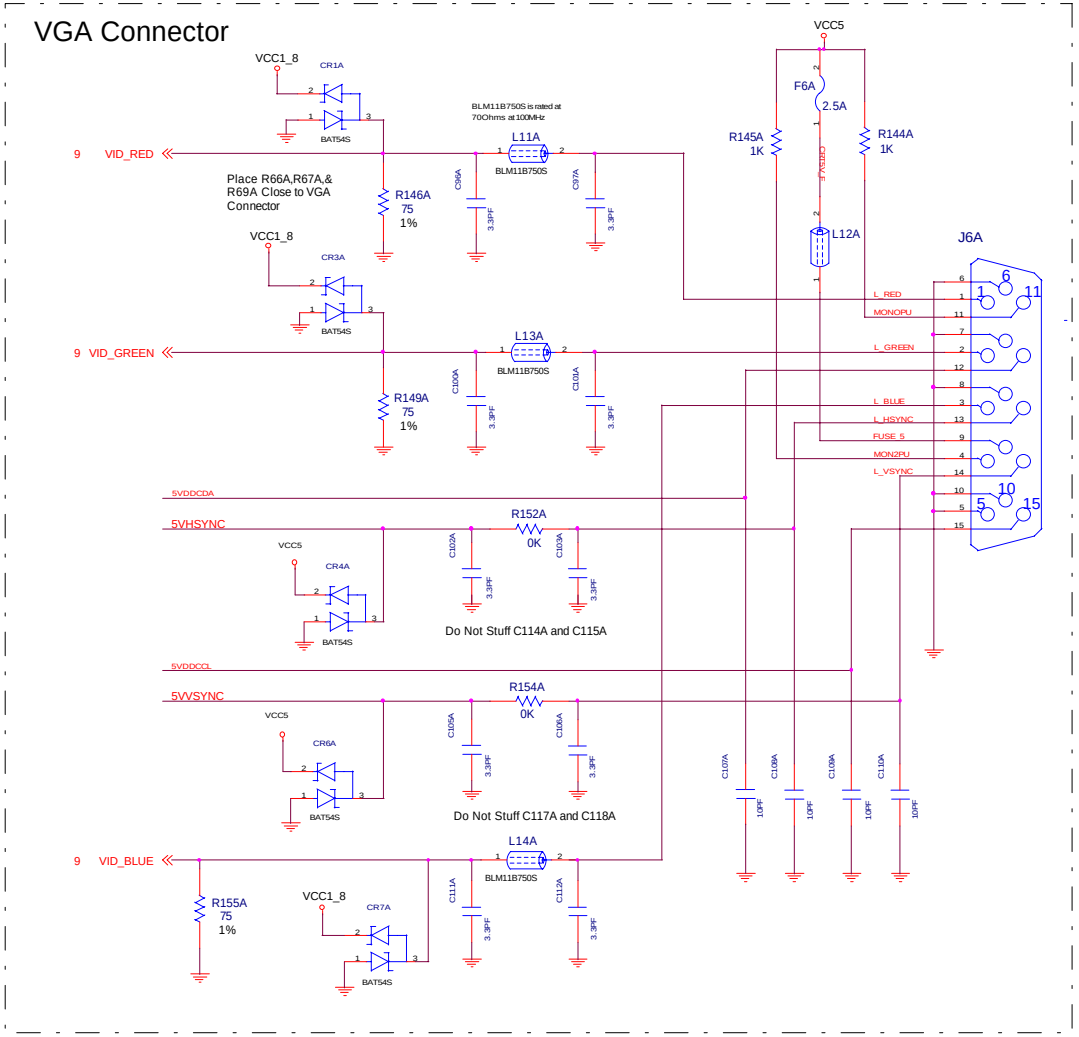
## 20 Pin Flat Panel Connector




## 5V to 3.3V Translation / Isolation




## VGA Connector




| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>Video Connectors | | REV. 1.0 |
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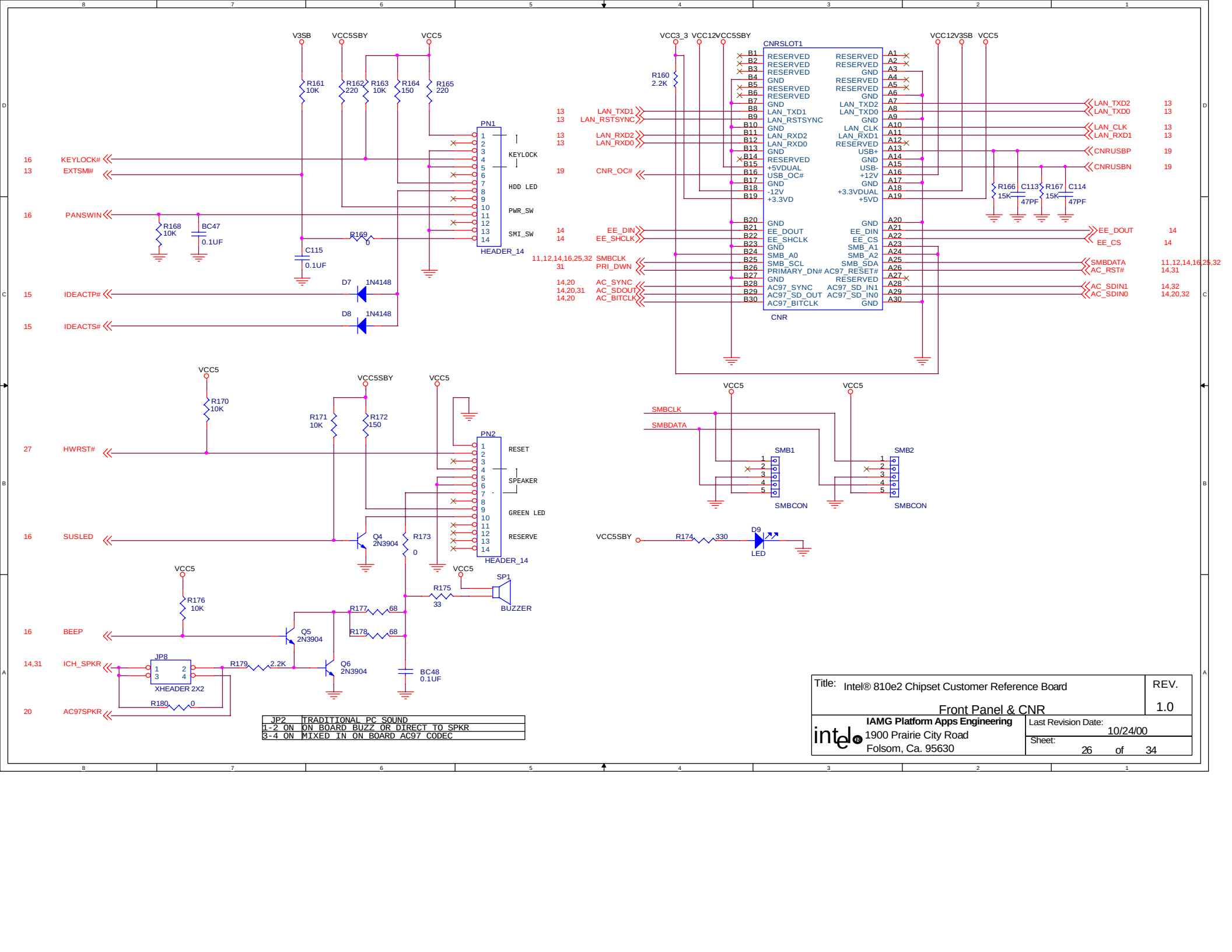
V3SB
VCC5SBY
VCC5
R161 10K
R162 220
R163 10K
R164 150
R165 220
PN1
KEYLOCK
HDD LED
PWR_SW
SMI_SW
HEADER_14
16 KEYLOCK#
13 EXTSMI#
16 PANSWIN
R168 10K
BC47 0.1UF
R169 0
C115 0.1UF
15 IDEACTP#
15 IDEACTS#
D7 1N4148
D8 1N4148
VCC3_3
VCC12
CNRSLOT1
R160 2.2K
13 LAN_TXD1
13 LAN_RSTSYNC
13 LAN_RXD2
13 LAN_RXD0
19 CNR_OC#
14 EE_DIN
14 EE_SHCLK
11,12,14,16,25,32 SMBCLK
31 PRI_DWN
14,20 AC_SYNC
14,20,31 AC_SDOUT
14,20 AC_BITCLK
CNR
VCC12V3SB
R166 15K
C113 47PF
R167 15K
C114 47PF
LAN_TXD2 13
LAN_TXD0 13
LAN_CLK 13
LAN_RXD1 13
CNRUSBP 19
CNRUSBN 19
EE_DOUT 14
EE_CS 14
SMBDATA 11,12,14,16,25,32
AC_RST# 14,31
AC_SDIN1 14,32
AC_SDIN0 14,20,32
SMBCLK
SMBDATA
SMB1
SMB2
SMBCON
VCC5SBY
R174 330
D9
LED
R170 10K
R171 10K
R172 150
27 HWRST#
16 SUSLED
Q4 2N3904
R173 0
RESET
SPEAKER
GREEN LED
RESERVE
R175 33
SP1
BUZZER
R176 10K
16 BEEP
Q5 2N3904
R177 68
R178 68
14,31 ICH_SPKR
JP8
XHEADER 2X2
R179 2.2K
Q6 2N3904
BC48 0.1UF
R180 0
20 AC97SPKR
JP2 TRADITIONAL PC SOUND
1-2 ON ON BOARD BUZZ OR DIRECT TO SPKR
3-4 ON MIXED IN ON BOARD AC97 CODEC
Title: Intel® 810e2 Chipset Customer Reference Board
Front Panel & CNR
REV. 1.0
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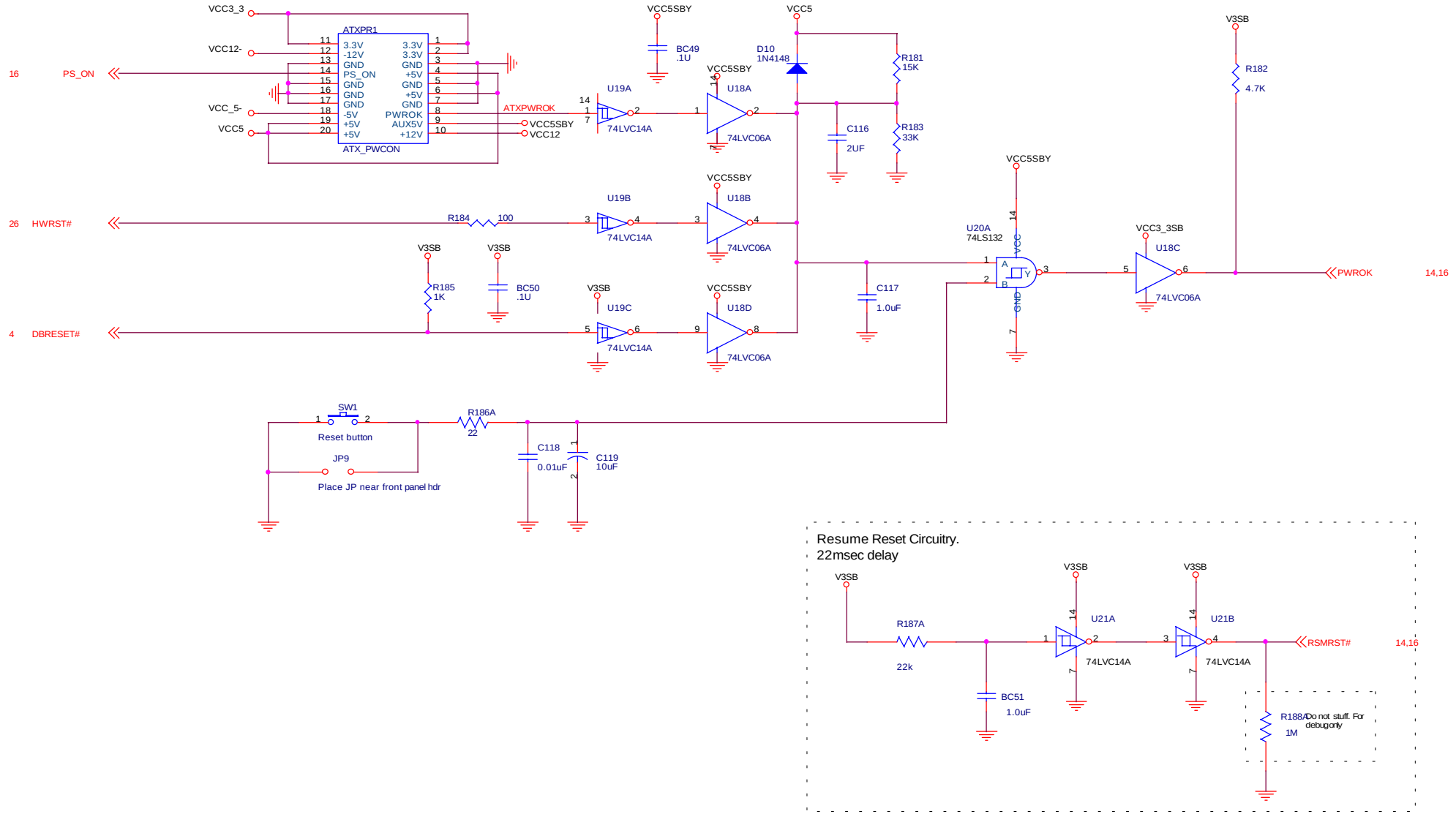


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|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>ATX Power | | REV. 1.0 |
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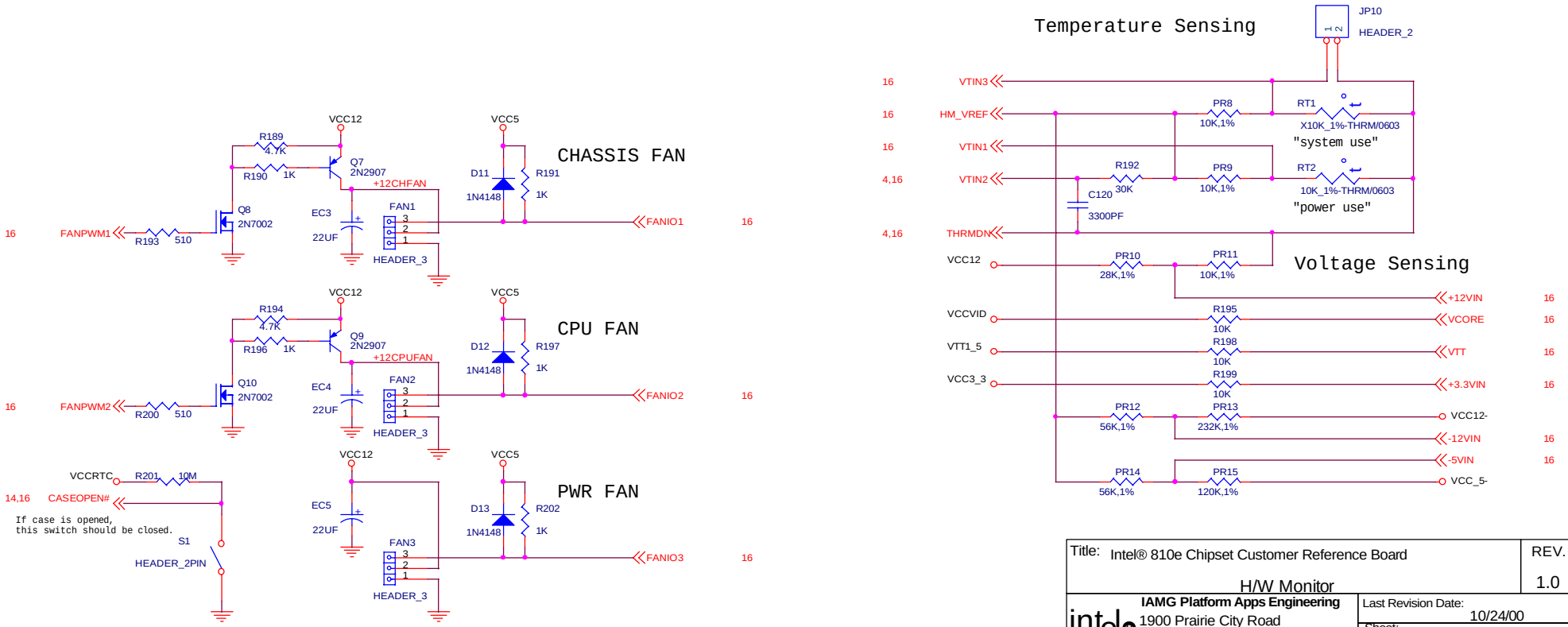





| | | |
|---|---|---|
| Title: Intel® 810e Chipset Customer Reference Board<br>H/W Monitor | | REV. 1.0 |
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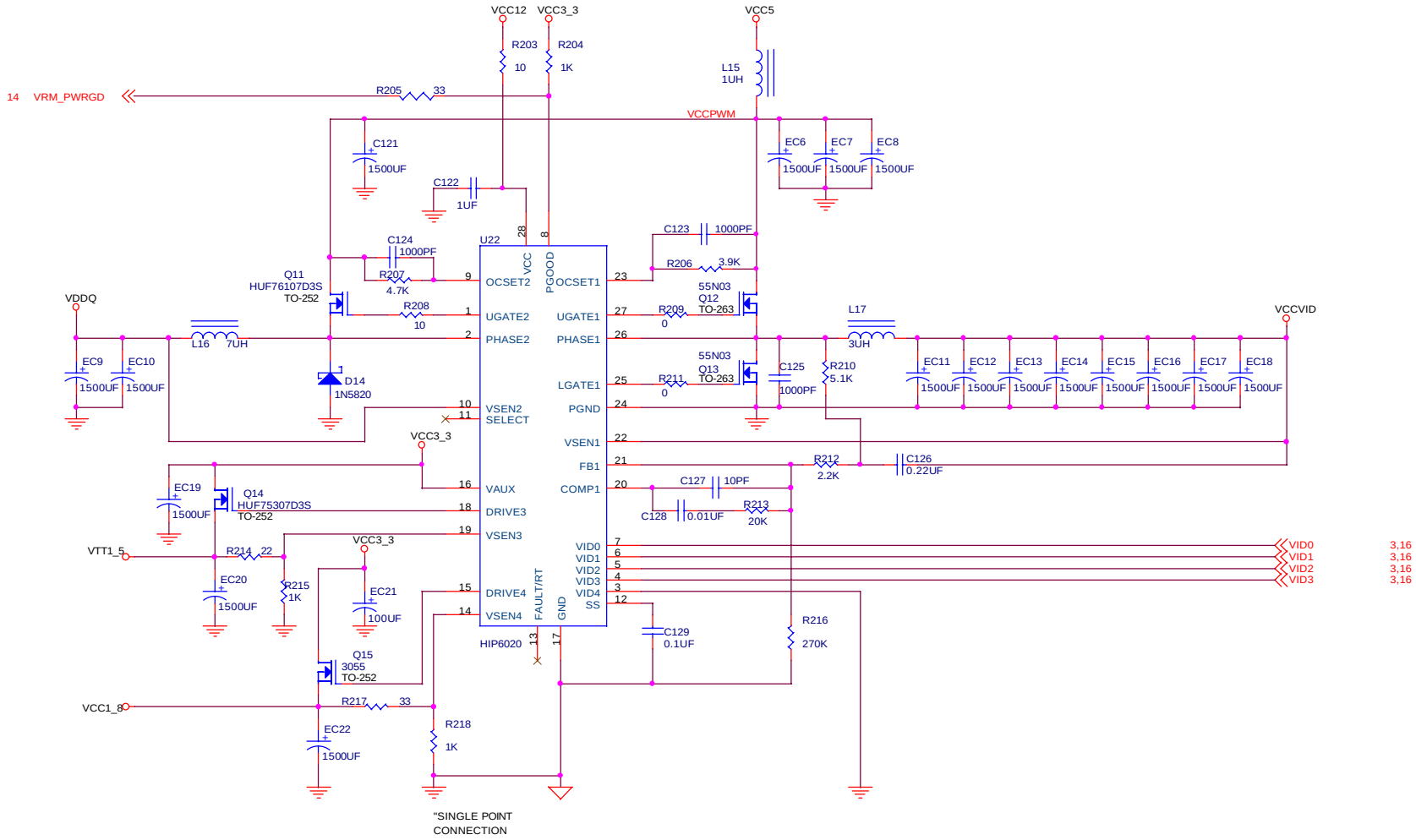


| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>Voltage Regulators Part 1 | | REV. 1.0 |
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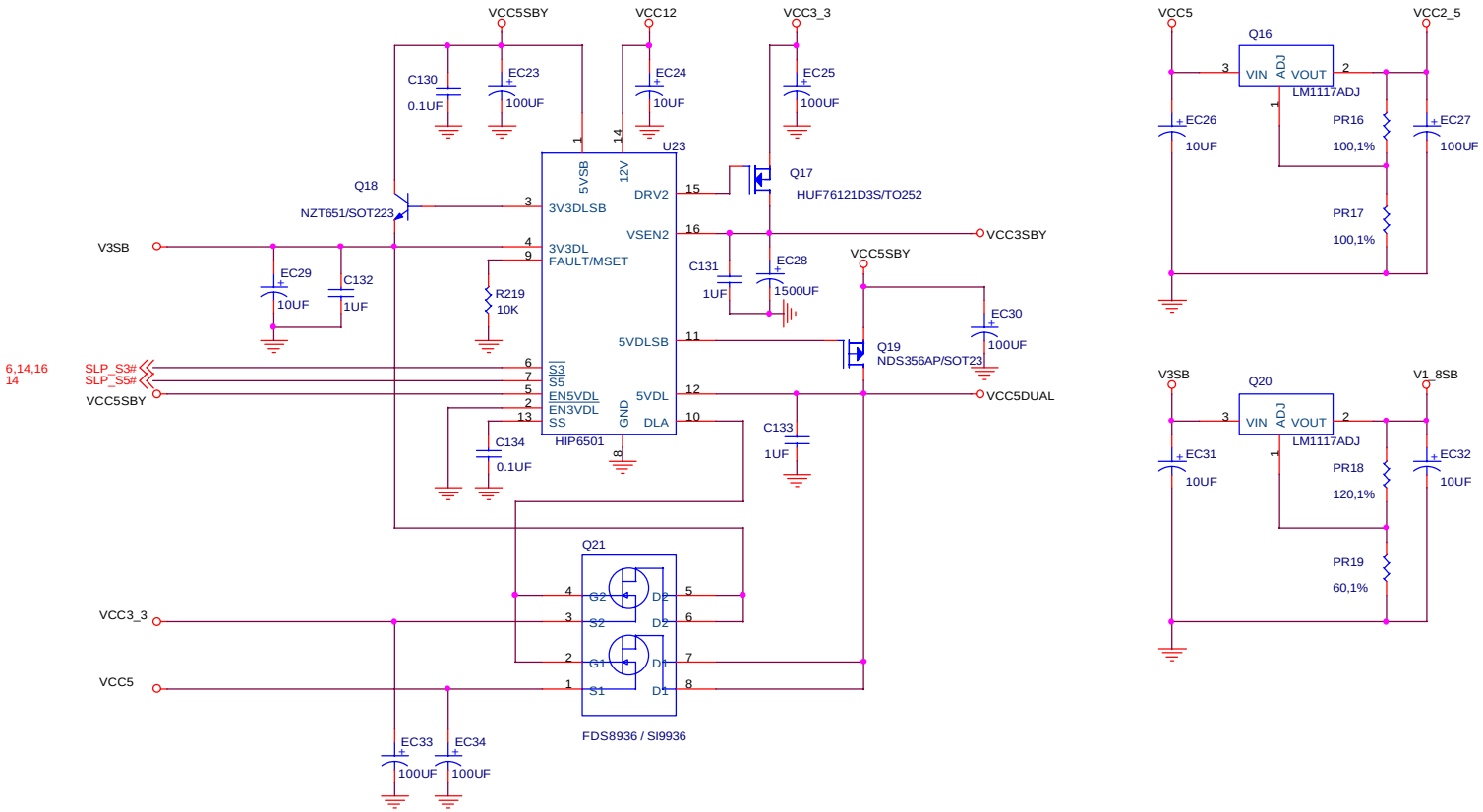





| | | |
|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>Voltage Regulators Part 2 | | REV. 1.0 |
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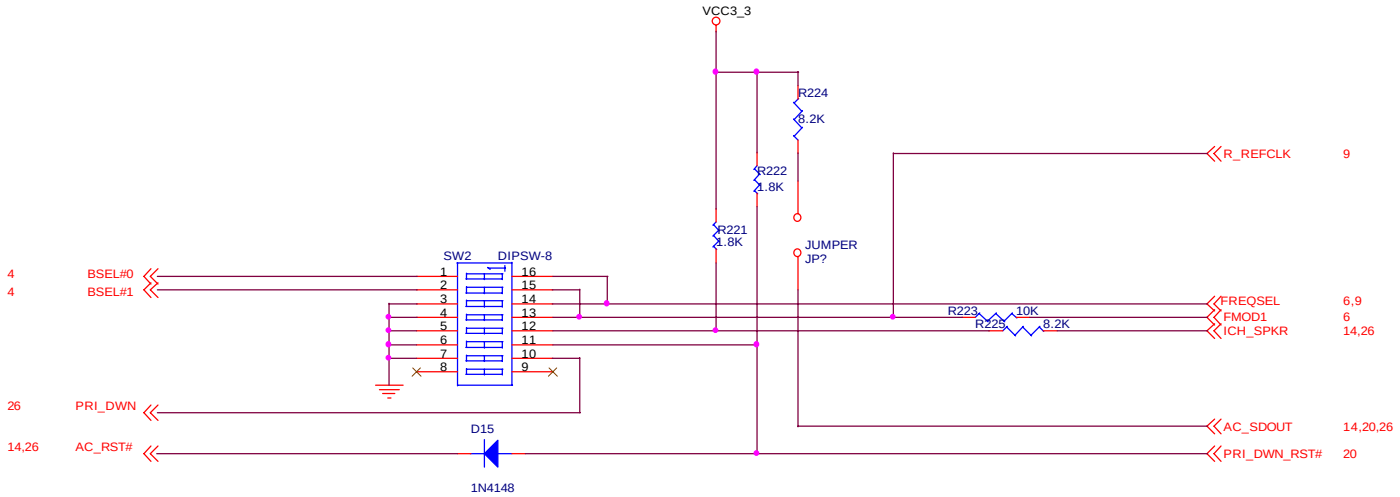


| SW1:7-8 | ON BOARD AC97 CODEC |
|---|---|
| ON 7 | PRIMARY CODEC |
| ON 8 | DISABLE |

| SW1:1-2 | FSB / SYSTEM MEMORY |
|---|---|
| ON1-2 | CPU DEFAULT |
| OFF 1-2 | BY SW2:3-4 |

| SW1:3-4 | FSB / SYSTEM MEMORY |
|---|---|
| ON ON | 66M/PC100 |
| OFF ON | 100M/PC100 |
| OFF OFF | 133M/PC100 OR PC133 |

| SW1:5 | AC_SDOUT |
|---|---|
| ON | USE CPU FREQ STRAP IN ICH REGISTER |
| OFF | FORCE CPU FREQ STRAP TO SAFE MODE(1111) |

| SW1:6 | STRAP(SPKR) |
|---|---|
| ON | NO REBOOT ON 2ND WATCHDOG TIMEOUT |
| OFF | REBOOT ON 2ND WATCHDOG TIMEOUT |

Title: Intel® 810e2 Chipset Customer Reference Board
System Configuration

REV. 1.0


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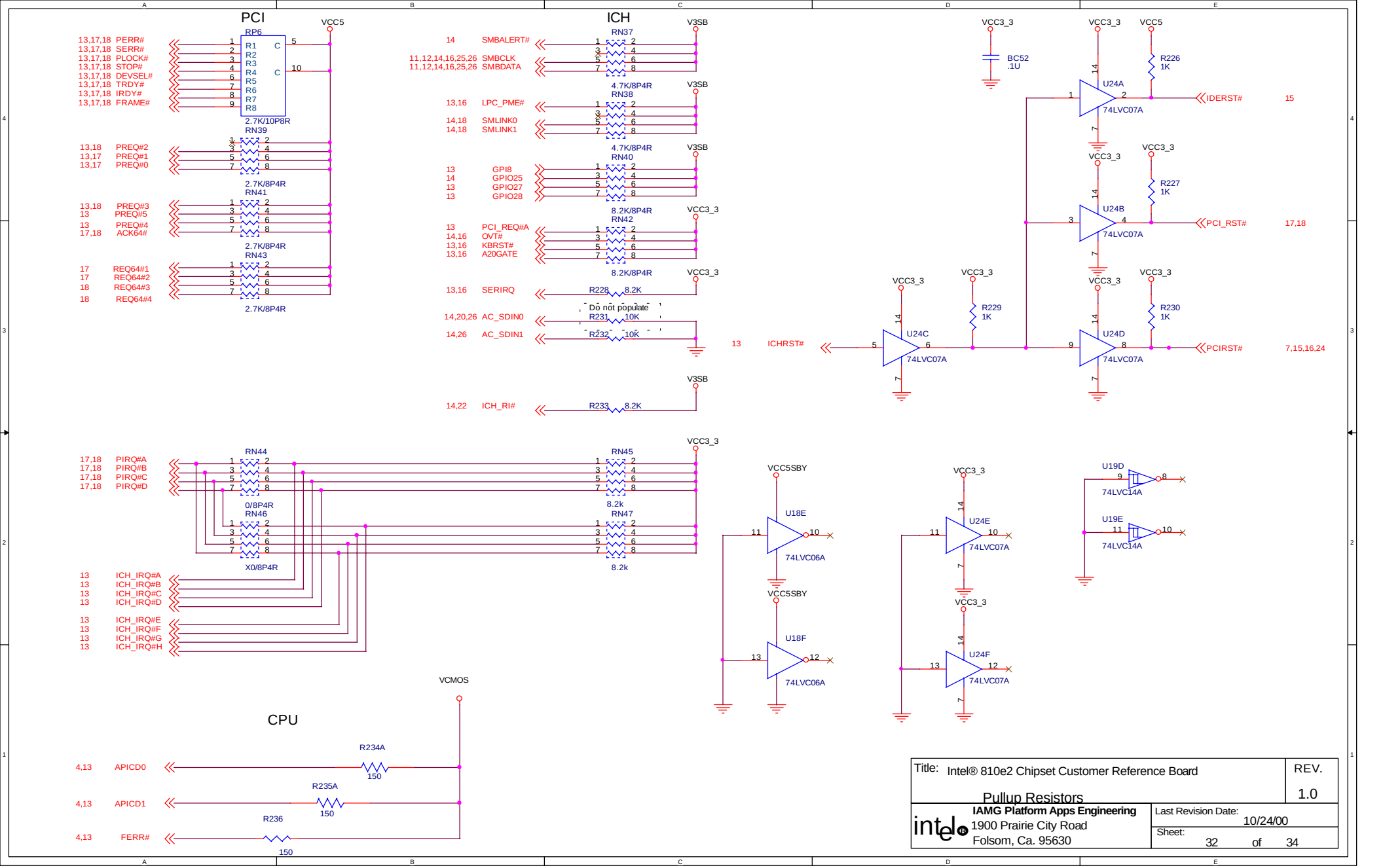
PCI
ICH
VCC5
V3SB
VCC3_3
RP6
2.7K/10P8R
RN37
RN38
RN39
RN40
RN41
RN42
RN43
4.7K/8P4R
8.2K/8P4R
2.7K/8P4R
13,17,18 PERR#
13,17,18 SERR#
13,17,18 PLOCK#
13,17,18 STOP#
13,17,18 DEVSEL#
13,17,18 TRDY#
13,17,18 IRDY#
13,17,18 FRAME#
13,18 PREQ#2
13,17 PREQ#1
13,17 PREQ#0
13,18 PREQ#3
13 PREQ#5
13 PREQ#4
17,18 ACK64#
17 REQ64#1
17 REQ64#2
18 REQ64#3
18 REQ64#4
14 SMBALERT#
11,12,14,16,25,26 SMBCLK
11,12,14,16,25,26 SMBDATA
13,16 LPC_PME#
14,18 SMLINK0
14,18 SMLINK1
13 GPI8
14 GPIO25
13 GPIO27
13 GPIO28
13 PCI_REQ#A
14,16 OVT#
13,16 KBRST#
13,16 A20GATE
13,16 SERIRQ
14,20,26 AC_SDIN0
14,26 AC_SDIN1
Do not populate
R231 10K
R232 10K
14,22 ICH_RI#
R233 8.2K
R228 8.2K
BC52 .1U
U24A
U24B
U24C
U24D
74LVC07A
R226 1K
R227 1K
R229 1K
R230 1K
IDERST# 15
PCI_RST# 17,18
13 ICHRST#
PCIRST# 7,15,16,24
RN44
RN45
RN46
RN47
0/8P4R
X0/8P4R
8.2k
17,18 PIRQ#A
17,18 PIRQ#B
17,18 PIRQ#C
17,18 PIRQ#D
13 ICH_IRQ#A
13 ICH_IRQ#B
13 ICH_IRQ#C
13 ICH_IRQ#D
13 ICH_IRQ#E
13 ICH_IRQ#F
13 ICH_IRQ#G
13 ICH_IRQ#H
VCC5SBY
U18E
U18F
74LVC06A
U19D
U19E
74LVC14A
CPU
VCMOS
R234A
R235A
R236
150
4,13 APICD0
4,13 APICD1
4,13 FERR#
Title: Intel® 810e2 Chipset Customer Reference Board
Pullup Resistors
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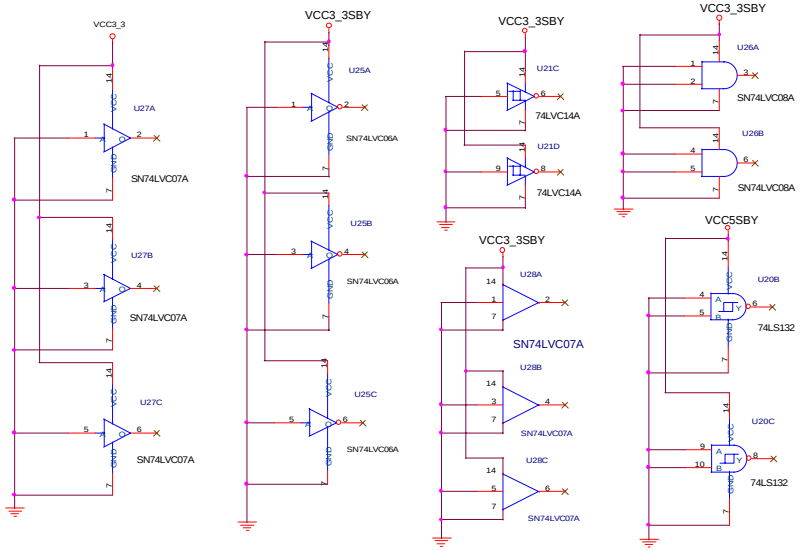
# UNUSED GATES

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|---|---|---|
| Title: Intel® 810e2 Chipset Customer Reference Board<br>Unused Gates | | REV.<br>1.0 |
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| | |
|---|---|
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