Intel® Xeon™ Processor and Intel® 860 Chipset Platform

Design Guide

Document Number: 298252-004

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Revision History

Revision Number	Description	Revision Date
-001	Initial Release.	May 2001
-002	2nd Release. Updated document references in Table 1 and throughout document. Added additional THERMTRIP# information to Section 5.4.2.1. Updated BR[3:0] routing recommendations in Section 5.4.2.5. Rotated and resized Figure 133, Figure 134, and Figure 135 to make more readable. Updated Table 50 and Table 51 with Intel Xeon processor at 2 GHz information. Updated TESTHI[6:0] and ODTEN recommendations in Sections 5.4.2.7 and 5.4.2.8, along with associated entries in processor schematic checklist in Section 17.1. Updated processor PLL filter, TESTHI[6:0], and ODTEN implementations in Customer Reference Board Schematics in Appendix A.	October 2001
-003	3rd release. Updated document with Intel® Xeon™ processor with 512 KB L2 cache content. Updated Section 12 with additional design details pertaining to processor decoupling, loadlines, voltage regulators, and power simulation/modeling. Replaced Figure 107 in Section 9.7.1, RTC Crystal Replaced Section 9.14, Power-Well Isolation Control Strap Requirements, and moved to Section 9.7.8, Power-well Isolation Control Added Section 9.7.9, Power Supply PS_ON Consideration Replaced Figure 114, Trace Routing in Section 9.8.2.1, General Trace Routing Considerations Added Section 9.8.5, Intel® 82562 ET/EM Disable Guidelines Added Section 9.9, FWH Guidelines Reordered the following sections: Glue Chip, SPKR Pin Considerations, and 1.8V and 3.3V Power Sequence Requirement Revised Section 13.5, ICH2 5VREF and VCC3.3 Sequencing Requirement Revised checklist item RSMRST# in Section 17.7.9, Power Management Revised checklist item RTCX1/RTCX2 in Section 17.7.12, RTC Added checklist item SUSCLK to RTC checklist in Section 17.7.12	January 2002

-004	Revised paragraph 3 in Section 9.14 ICH2 V5REF and VCC3_3 Sequencing Requirement Revised APIC in Section 17.7.6 Interrupt Interface in the Schematics Checklist Revised V5REF_SUS in Section 17.7.15 Power in the Schematics Checklist	March 2002

1 Introduction

This design guide documents Intel's design recommendations for systems based on the Intel® Xeon™ processor and/or Intel® Xeon™ processor with 512 KB L2 cache with the Intel® 860 chipset. In addition to providing motherboard design recommendations such as layout and routing guidelines, this document also addresses possible system design issues such as EMI design impacts and system bus decoupling. Thermal considerations are addressed by specific thermal documentation for the processor and the Intel 860 chipset listed in Section 1.1. Unless otherwise noted, references to "processor" throughout this document apply to both the Intel Xeon processor and Intel Xeon processor with 512 KB L2 cache.

Carefully follow the design information, board schematics, debug recommendations, and system checklist presented in this document. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into one of the two categories:

- *Design Recommendations* are items that are based on Intel's simulations and lab experience to date, and are strongly recommended, if not necessary, to meet the timing and signal quality specifications.
- *Design Considerations* are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel. They should be used as examples, and may not apply to your particular design.

Note: The guidelines recommended in this document are based on experience, simulation, and validation work completed at Intel during Intel Xeon processor and Intel Xeon processor with 512 KB L2 cache/Intel 860 chipset based systems development. This work is ongoing, and the recommendations are subject to change.

The platform schematics in Appendix A can be used as a reference for board designers. While the schematics may cover a specific design, the core schematics remain the same for most platforms. The schematic sets provide a reference schematic for each platform component, and common motherboard options. Additional flexibility is possible through permutations of these options and components.

1.1 Related Documentation

Table 1. Reference Documentation

Document	Document Number/Source
IA-32 Intel® Architecture Software Developer's Manual	
• Volume 1: Basic Architecture	245470
• Volume 2: Instruction Set Reference	245471
• Volume 3: System Programming Guide	245472
CK00 Clock Synthesizer/Driver Design Guidelines	http://developer.intel.com /design/pentium4/guides /249206.htm
VRM 9.0 DC-DC Converter Design Guidelines	http://developer.intel.com /design/pentium4/guides /249205.htm
Intel® 860 Chipset: 8260 Memory Controller Hub (MCH) Datasheet	290713
Intel® Xeon™ Processor Thermal Design Guidelines	http://developer.intel.com /design/Xeon/guides /298348.htm
603 Pin Socket Design Guidelines	http://developer.intel.com /design/Xeon/guides /249672.htm
Intel® Xeon™ Processor at 1.40 GHz, 1.50 GHz, 1.7 GHz and 2 GHz Datasheet	http://developer.intel.com /design/xeon/datashts /249665.htm
Intel® Xeon™ Processor with 512 KB L2 Cache at 1.8 GHz, 2 GHz and 2.2 GHz Datasheet	http://developer.intel.com
Intel® Xeon™ Processor with 512 KB L2 Cache Compatibility Guidelines for Intel® Xeon™ Processor-Based Platforms	http://developer.intel.com
Intel® Xeon™ Processor Thermal Solution Functional Specification	http://developer.intel.com /design/Xeon/applnots/24 9673.htm
Intel® Xeon™ Processor Signal Integrity Models (IBIS format)	http://developer.intel.com
Intel® Xeon™ Processor with 512 KB L2 Cache Signal Integrity Models (IBIS format)	http://developer.intel.com
Intel® Xeon™ Processor Overshoot Checker Tool	http://developer.intel.com
Intel® Xeon™ Processor with 512 KB L2 Cache Overshoot Checker Tool	http://developer.intel.com
Intel® Xeon™ Processor Enabled Components Models (ProE and IGES format)	http://developer.intel.com
Intel® Xeon™ Processor with 512 KB L2 Cache Mechanical Models (ProE and IGES format)	http://developer.intel.com
Intel® Xeon™ Processor Thermal Model (Flotherm and Icepak format)	http://developer.intel.com
Intel® Xeon™ Processor with 512 KB L2 Cache Thermal Models (Flotherm	http://developer.intel.com

Document	Document Number/Source
and Icepak format)	
Intel® Xeon™ Processor Core Boundary Scan Descriptive Language (BSDL) Model	http://developer.intel.com
Intel® Xeon™ Processor with 512 KB L2 Cache Boundary Scan Descriptive Language (BSDL) Model	http://developer.intel.com
Intel® Processor Identification and the CPUID Instruction (AP-485)	241618
System Management Bus Specification, Rev. 1.1	www.sbs-forum.org/specs
Wired for Management 2.0 Design Guide	http://developer.intel.com
Intel® 860 I/O Buffer Model Documentation	http://developer.intel.com
Intel® 860 Chipset Thermal Considerations Application Note	292269
Intel® 82801BA I/O Controller Hub 2 (ICH2) I/O and Intel® 82801 BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet	290687
AC '97 Component Specification Rev. 2.1	http://developer.intel.com/ial/scalableplatforms/audio/index.htm
Accelerated Graphics Port Interface Specification Rev. 2.0	www.agpforum.org
Low Pin Count Interface Specification Rev. 1.0	http://developer.intel.com
PCI Local Bus Specification Rev. 2.1	www.pcisig.com
PCI Local Bus Specification Rev. 2.2	www.pcisig.com
PCI-PCI Bridge Specification Rev. 1.0	www.pcisig.com
PCI Hot Plug Specification Rev. 1.0	www.pcisig.com
PCI Bus Power Management Interface Specification Rev. 1.0	www.pcisig.com
Universal Serial Bus Specification Rev. 1.0	http://developer.intel.com
Direct RDRAM* device documentation	http://developer.intel.com
Advanced Configuration and Power Interface Specification (ACPI) Rev. 1.0b	http://developer.intel.com
NT Hardware Design Guide	www.microsoft.com
PC 99/2001 Specification	www.microsoft.com
Intel® 860 Chipset Memory Expansion Card (MEC) Design Guide	298302
ITP700 Debug Port Design Guide	http://developer.intel.com/design/Xeon/guides/249679.htm
Intel® 82806AA PCI 64 Hub (P64H) Datasheet.	http://developer.intel.com

1.2 Conventions and Terminology

This section defines conventions and terminology that are used throughout this document.

Table 2. Platform Conventions and Terminology

Convention/ Terminology	Definition
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGTL+	The processor system bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors that provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Corner	Describes how a component performs when all parameters that could impact performance are adjusted simultaneously to have the best or worst impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. Performance of an electronic component may change as a result of (including, but not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the “slow” corner means a component operating at its slowest, weakest drive strength performance. Similar discussion of the “fast” corner means a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Crosstalk–coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal. • Forward Crosstalk–coupling that creates a signal in a victim network that travels in the same direction as the aggressor’s signal. • Even Mode Crosstalk–coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Crosstalk–coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.

Convention/ Terminology	Definition
Flight Time	Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, *flight time* is defined to be: • Time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; e.g., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings. • Maximum and Minimum Flight Time–Flight time variations can be caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects. • Maximum flight time is the largest acceptable network flight time under all conditions. • Minimum flight time is the smallest acceptable network flight time under all conditions.
GTL+	GTL+ is the bus technology used by the Intel® Pentium® Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) technology.
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Manageability Features	Circuits incorporated into the processor that allow system administrators to monitor processor status and information including temperature, stepping, cache size, and more. They are accessed through the System Management Bus.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	The distance between agent 0 pins and the corresponding agent pin at the far end of the bus.
Overshoot	Maximum voltage observed for a signal at the device pad. Measured with respect to VCC_CPU.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulation.
Pin	The contact point of a component package to the traces on a substrate such as the motherboard. Signal quality and timings can be measured at the pin.
Power-Good	*"Power-Good"* or "*PWRGOOD*" (an active high signal) indicates that all of the supplies and clocks within the system are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena.

Convention/ Terminology	Definition
System Bus	The system bus (also known as the Intel® NetBurst™ micro-architecture system bus) is the interconnect between the processor and Intel® 860 Chipset. The Intel® NetBurst™ micro-architecture system bus is not compatible with the P6 family processor system bus.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
SSO	Simultaneous Switching Output (SSO) Effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or “push-out”), or a decrease in propagation delay (or “pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	Minimum voltage observed for a signal to extend below VSS at the device pad.
VCC_CPU	VCC_CPU is the processor power supply. It is specified as Vcc in the processor datasheets, but for clarity it is referred to as VCC_CPU in this document. The system bus is terminated to VCC_CPU.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
V_{REF} Guardband	A guardband defined above and below V_{REF} to provide a more realistic model accounting for noise such as VTT and V_{REF} noise.
VRM 9.0	*“VRM 9.0”* refers to a specific revision of the VRM (Voltage Regulator Module) design guidelines recommended for this platform. It is a DC-DC converter module that supplies the required voltage and current to a single processor.

1.3 System Overview

The Intel Xeon processor and Intel Xeon processor with 512 KB L2 cache with the Intel 860 chipset deliver a high performance workstation platform solution.

1.3.1 Processor Overview

The Intel Xeon processor is the first generation Intel® IA-32 processor for workstations featuring the Intel® NetBurst™ micro-architecture. It has a number of features that increase its performance with respect to the previous generation of IA-32 processors. One change is a more efficient implementation of on-die cache. The Intel Xeon processor implements integrated on-die L1 and L2 caches. The L2 cache size is 256 KB and is 8-way set associative. The L1 and L2 caches on the Intel Xeon processor outperforms the L1 and L2 caches on Intel® Pentium® III processors.

The Intel Xeon processor with 512 KB L2 cache is the next generation Intel® IA-32 processor for workstations. In addition to increasing the L2 cache size, the Intel Xeon processor with 512 KB L2 cache operates at significantly higher clock speeds than the Intel Xeon processor. Table 3 summarizes the feature set of these two processors.

The System Bus is the link between the Intel 860 chipset memory controller hub (MCH) and the Intel Xeon processors. The System Bus utilizes a split-transaction, deferred reply protocol similar to that of the P6 bus, but the System Bus is not compatible with the P6 bus. The System Bus uses Source-Synchronous Transfer (SST) of address and data to improve performance by allowing data transfers at a frequency of 400 MHz, or 3.2 GB/sec data bandwidth. The control signals and bus phases are based on a 100 MHz system clock. This enhanced bus protocol and internal architecture increases performance beyond previous levels.

Table 3. Processor Feature Set Overview

Feature	Intel® Xeon™ Processor	Intel® Xeon™ Processor with 512 KB L2 Cache
L1 Cache	On-die	On-die
L2 Cache	256 KB on-die	256 KB on-die
Data Bus Frequency	400 MHz	400 MHz
Multi-Processor Support	1-2 way	1-2 way
Manageability Features	Intel and OEM EEPROMS and thermal sensor on package	Intel and OEM EEPROMS and thermal sensor on package
Package Configuration	603 pins, 0.05 inch spacing, micro-PGA	603 pins, 0.05 inch spacing, micro-PGA

1.3.2 Intel® 860 Chipset

The Intel 860 chipset consists of two main components, the Memory Controller Hub (MCH) and the I/O Controller Hub 2 (ICH2). Two optional components, the MRH-R and the P64H, provide expansion capability. These components are interconnected via an Intel proprietary interface called the "hub interface," which provides efficient communication between components.

Additional hardware platform features include AGP Pro, Direct RDRAM* device, Ultra ATA/100, Low Pin Count interface (LPC), integrated LAN, and the Universal Serial Bus (USB). The platform is also ACPI compliant and supports Full-on, Stop Grant, Suspend-to-RAM, Suspend-to-Disk, and Soft-off power management states. Through the use of an appropriate LAN connect, the platform supports Alert-on-LAN* for remote administration and troubleshooting.

1.3.2.1 Memory Controller Hub (MCH)

The MCH component provides the processor interface, DRAM interface, AGP interface, and hub interfaces in an Intel 860 chipset-based platform. The processor interface is optimized for the System Bus Protocol. The AGP interface supports AGP4X and high-end AGP Pro graphics cards. The hub interfaces may be used to connect to a P64H peripheral component.

The MCH is available in a 1012-ball OLGA package, and contains the following functionality:

- Supports a dual Intel Xeon processor or Intel Xeon processor with 512 KB L2 cache configuration with data transfer rates of 400 MHz
- AGTL+ host bus with integrated termination that supports 36-bit host addressing
- Dual Rambus* channels that support 300 MHz and 400 MHz Direct RDRAM* device operation **on RIMM* modules down solution**.
- Maximum 4GB of Direct RDRAM device memory support using 2 MRH-Rs with 256-Mbit technology
- 1.5 V AGP interface with 4X SBA/data transfer and 2X/4X fast write capability
- Two 16-bit, 66 MHz 4X hub interfaces that allow flexible I/O expansion
- 8-bit, 66 MHz 4X hub interface to ICH2

1.3.2.2 I/O Controller Hub 2 (Intel® ICH2)

The ICH2 provides the I/O subsystem access to the rest of the system. Additionally, it integrates many widely utilized I/O functions.

The ICH2 is available in a 360 ball EBGA package, and contains the following functionality:

- PCI bus interface at 33 MHz, 133 Mbit/s maximum throughput
- Supports up to 6 PCI master devices
- LAN controller with 10/100 Mbit/s Ethernet and 1 Mbit/s HomePDA® support
- Low pin count (LPC) interface
- Firmware Hub (FWH Flash BIOS) interface
- 82C54 based timer
- IDE controller with support for Ultra ATA 100/66/33
- Two USB controllers for a total of four ports
- Enhanced DMA controller with support for REQ#/GNT# pairs, LPC DMA, Type F DMA
- SMBus interface
- AC’97 link for external audio and telephony CODECs

1.3.2.3 Memory Repeater Hub for Direct RDRAM* Device (Intel® MRH-R)

The Intel® MRH-R component provides the capability to support multiple Rambus* Channels from the MCH "expansion channels." The expansion channel is the interconnection between the Intel 860 chipset MCH and the MRH-R component. It is referred to as the expansion channel because two extra RSL signals are required when interfacing with an MRH-R component (refer to the *Intel® 860 Chipset Memory Expansion Card (MEC) Design Guide* for more details). Each MRH-R can support up to two Rambus Channels also known as stick channels. The MRH-R acts as a pass-through logic with fixed delay for read and write accesses from expansion channels to Rambus Channels.

The MRH-R is available in a 324 MBGA package, and contains the following functionality:

- Maximum of 1 GB memory per stick channel
- Nap Entry/Exit, Power down Exit, Refresh and Precharge on a channel upon request from memory controller
- Core logic gating to minimize power consumption
- Reference clock generation for Direct Rambus* Clock Generator (DRCG device)
- Integrated SMBus controller to read/write data from/to SPD (serial presence detect) EEPROM on the RIMM modules.

1.3.2.4 PCI 64-Bit Hub (Intel® P64H)

The PCI 64-Bit Hub (P64H) is a peripheral chip that performs PCI bridging functions between the hub interface and the PCI Bus, and is used as an integral part of the Intel 860 chipset. The P64H has a 16-bit primary hub interface to the Memory Controller Hub (MCH) and a secondary 64-bit PCI Bus interface. The 64-bit interfaces inter-operate transparently with either 64-bit or 32-bit devices. The P64H is compliant with the *PCI Local Bus Specification, Revision 2.2*.

1.3.3 Bandwidth Summary

The following table describes the bandwidth for each bus.

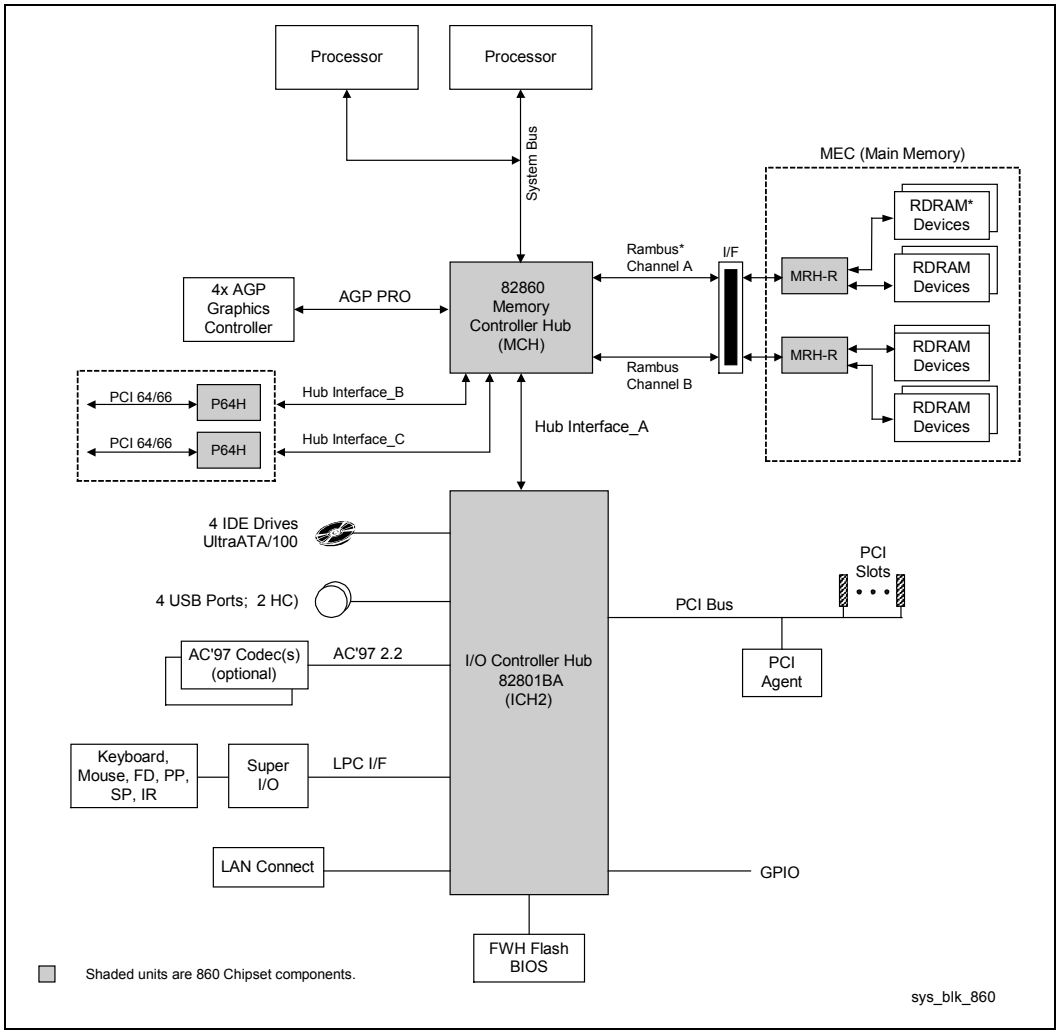
Table 4. Platform Bandwidth Summary

Interface	Maximum Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Maximum Bandwidth (Mbit/s)
System Bus (DP)	100	4	8	3200
AGP	66	4	4	1066
Hub interface A	66	4	1	266
Hub interface B/C	66	4	2	533
PCI	33	1	4	133
Direct RDRAM* device	400	2	4	3200
Ultra ATA/66	66			66
Ultra ATA/100	100			100

1.3.4 System Configurations

Figure 1 illustrates a typical Intel 860 chipset system configuration for workstation platforms. The workstation systems examples below use a Memory Expansion Card (MEC) to increase the amount of available system memory. An MEC can be designed with two MRH-Rs if a Direct RDRAM device is used. If memory expansion to 4 GB is not required, the memory slots can be placed directly on the motherboard.

Figure 1. Workstation System Configuration Using the Intel® Xeon™ Processor/Intel Xeon Processor with 512 KB L2 Cache and Intel® 860 Chipset



1.4 Platform Initiatives

This section documents the platform initiatives.

1.4.1 Memory Expansion Card (MEC) and Connector (MECC)

The MEC concept is intended to provide flexibility and scalability of memory to Intel 860 chipset-based workstation platforms. Specific design information for this memory expansion card and connector is described in the *Intel® 860 Chipset Memory Expansion Card (MEC) Design Guide*. This document presents design recommendations, board schematics, debug recommendations, and an MEC schematic and layout checklist.

1.4.2 Intel® 860 Chipset MCH

1.4.2.1 Direct RDRAM* Device Interface

The Direct RDRAM device interface provides the necessary memory bandwidth to obtain optimal performance from the Intel Xeon processor, as well as a high performance AGP graphics controller. The MCH Direct RDRAM device interface supports a maximum of 400 MHz operation, delivering 3.2 GB/s of theoretical memory bandwidth using two Rambus Channels operating in lock step. This is twice the memory bandwidth of 100 MHz SDRAM systems. Coupled with the greater bandwidth, the heavily pipelined Direct RDRAM device protocol provides a substantially more efficient data transfer. The Direct RDRAM device memory interface can achieve greater than 95% utilization of the 3.2 GB/s theoretical maximum bandwidth.

In addition to the Direct RDRAM device performance features, this new memory architecture provides enhanced power management capabilities. The powerdown mode of operation enables Intel 860 chipset-based systems to cost-effectively support Suspend-to-RAM.

The 128-/144-Mbit, and 256-/288-Mbit Direct RDRAM device technologies will be supported by Intel 860 chipset –based platforms.

1.4.2.2 Accelerated Graphics Port (AGP)

AGP is a high performance, component-level interconnect targeted at 3D graphical display applications. AGP is based on a set of performance extensions or enhancements to the PCI bus. The Intel 860 chipset employs an AGP interface that is optimized for a point-to-point topology using 1.5 V signaling in 4X mode. The 4X mode provides a peak bandwidth of 1066 Mbit/s.

For complete details at refer to the *AGP Interface Specification, Rev. 2.0* at

http://www.agpforum.org/specs_specs.htm.

1.4.2.2.1 AGP 2.0

The Accelerated Graphics Port (AGP) is a high performance, component-level interconnect targeted at 3D graphical display applications. AGP is based on a set of performance extensions or enhancements to the PCI bus. The AGP interface is optimized for a point-to-point topology using 1.5 V signaling. The baseline performance level utilizes a 66 MHz clock to provide a peak bandwidth of 266 Mbit/s. There are two options for higher performance levels- 2X mode and 4X mode. The 2X mode provides a peak bandwidth of 533 Mbit/s and 4X mode provides a peak bandwidth of 1066 Mbit/s.

Refer to the *Accelerated Graphics Port Interface Specification* Rev. 2.0, and *AGP Design Guide* (1X, 2X and 4X Modes & 1.5 V and 3.3 V Signaling), Rev 1.0 for complete details.

1.4.2.2.2 AGP Pro

AGP Pro specifies an extension to the AGP graphics bus connection for the high-performance workstation market segment. The AGP Pro specifications include electrical, mechanical and thermal requirements for the AGP Pro connector, card and chassis. It will also include examples of possible thermal solutions.

AGP Pro is expected to deliver up to four times the electrical power of the standard AGP interface through an extension to the AGP connector and provision of sufficient space to dissipate this increased power. It also allows for multiple slot implementations where an AGP Pro Card is coupled with one or more PCI cards. Finally, the specification allows for flexible utilization of the thermal space provided for cards that dissipate significantly less than the maximum power-envelope. AGP Pro will retain mechanical and functional compatibility with AGP so that an AGP Card can plug into an AGP Pro connector, although an AGP Pro card cannot plug into an AGP connector.

For complete details refer to the *AGP Pro Specification Rev 1.1* at

http://www.agpforum.org/specs_specs.htm.

1.4.3 Intel® ICH2

1.4.3.1 Integrated LAN Controller

The ICH2 incorporates an integrated LAN Controller. Its bus master capabilities enable the component to process high level commands and perform multiple operations that lowers processor utilization by off-loading communication tasks from the processor.

The ICH2 functions with several options of Platform LAN Connect Components to target the desired market segment. The Intel® 82562EH component provides a *HomePNA*® 1Mbit/sec connection. The Intel® 82562ET component provides a basic Ethernet 10/100 connection. The Intel® 82562EM component provides an Ethernet 10/100 connection with the added flexibility of *Alert on LAN**. More advanced LAN solutions can be implemented with the Intel® PRO/100 S Desktop Adapter or other PCI based product offerings.

1.4.3.2 Audio Codec ’97 (AC’97) 6-Channel Support

The *Audio Codec ‘97 Component Specification v2.2* defines a digital link that can be used to attach an audio codec (AC), a modem codec (MC), an audio/modem codec (AMC), or both an AC and an MC. The *Audio Codec ‘97 Component Specification v2.2* defines the interface between the system logic and the audio or modem codec known as the “AC’97 digital link.”

The ICH2 AC’97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC’97 digital link. Using the ICH2 integrated AC’97 digital link reduces cost and eases migration from ISA.

By using an audio codec, the AC’97 digital link allows for cost-effective, high-quality, integrated audio on the Intel 860 chipset platform. In addition, an AC’97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC’97. ICH2’s integrated digital link allows two external codecs to be connected to the ICH2 in several configurations. Refer to Table 5 for the various AC’97 codec implementations.

Table 5. Intel® ICH2 Codec Options

Primary:	Secondary:
Audio (AC)	None
Modem (MC)	None
Audio/Modem (AMC)	None
Audio (AC)	Modem (MC)
Audio (AC)	Audio (AC)
Audio (AC)	Audio/Modem (AMC)

Modem implementation for different countries must be considered because telephone systems may vary. By using a split design, the audio codec can be on-board, and the modem codec can be placed on a riser. Intel is developing a digital link connector. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

The digital link in the ICH2 is *Audio Codec ‘97 Component Specification v2.2* compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec. The Intel 860 chipset-based platform expands audio capability with support for up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center and Woofer for a complete surround sound effect.

For complete details, refer to the *Audio Codec ‘97 Component Specification v2.2* at

http://developer.intel.com/pc-supp/platform/ac97/.

1.4.3.3 Low Pin Count (LPC) Interface

In the platform, the super I/O component has migrated to the Low Pin Count (LPC) interface. Migration to the LPC interface allows for lower cost super I/O designs. The LPC super I/O component requires the same feature set as traditional super I/O components. It should include a keyboard and mouse controller, floppy disk controller and serial and parallel ports. In addition to the standard super I/O features, an integrated game port is recommended because the AC'97 interface does not provide support for a game port. In a system with ISA audio, the game port typically existed on the audio card. The fifteen-pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface.

For complete details, refer to the *Low Pin Count Interface Specification, Revision 1.0* at

http://developer.intel.com.

Consult your super I/O vendor for a comprehensive list of devices offered and features supported.

1.4.3.4 Ultra ATA

Ultra ATA "widens" the path to the hard drive by transferring twice as much data per clock cycle. The net effect is that the maximum burst data transfer rate from the disk drive increases from 16.6 Mbit/s to 100 Mbit/s. Hard disk drive manufacturers can now bring higher performance products to market that scale with the rest of the PC platform (faster hard drives to feed faster processors, memory and graphics).

The Ultra ATA protocol allows Intel 860 chipset-based systems to send and retrieve data faster, removing bottlenecks associated with data transfers, especially during sequential operations. Users of new Intel 860 chipset-based systems will need less time to boot their systems and open applications, a direct result of the improved throughput provided by Ultra ATA. Current disk drive technology has been optimized to perform within the limits of the legacy protocol (16.6 Mbit/s). Raising the data transfer headroom results in moderate performance gains with today's drive technology. Even greater performance improvements will emerge as drive manufacturers introduce products that generate a faster data stream.

The ICH2 supports the IDE controller with two sets of interface signals (Primary and Secondary) that can be independently enabled, tri-stated, or driven low. It supports the Ultra ATA/33, Ultra ATA/66, and Ultra ATA/100 protocols. Ultra ATA/66 and ATA/100 are similar to the Ultra ATA/33 scheme and are intended to be device driver compatible. The Ultra ATA/66 logic clocks at 66 MHz and can move 16-bit of data every two clocks (for a maximum of 66 Mbit/s), and the Ultra ATA/100 logic clocks at 100 MHz and can move 16-bit of data every two clocks (for a maximum of 100 Mbit/s).

1.4.3.5 Universal Serial Bus (USB)

Universal Serial Bus (USB) simplifies the peripheral attaching and accessing process to the computer. It also eases the system configuration process from an end-user's perspective. The USB specification outlines a single connector-type for all PC peripherals, automatic detection/configuration of the USB devices, and transfer types allowed on the bus.

In the Intel 860 chipset based platform, the ICH2 integrates two USB Host Controllers. The Host Controllers include the root hub with two separate USB ports, resulting in a total of four USB ports. The addition of a USB Host Controller expands functionality of the platform. The ICH2 Host Controller supports the standard *Universal Host Controller Interface (UHCI), rev. 1.0*.

For further information refer to the *USB Specification Rev. 1.0* at

http://www.usb.org.

1.4.4 Manageability

The Intel 860 chipset platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external micro-controller.

Interrupt Controller: The interrupt capabilities of the ICH2 in an Intel 860 chipset-based platform expands support for up to 8 PCI interrupt pins and PCI 2.2 Message-Based Interrupts. In addition, the ICH2 supports system bus interrupt delivery.

TCO Timer: The ICH2 integrates a programmable TCO timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI# which the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.

Processor Present Indicator: The ICH2 looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the ICH2 has the ability to blink a GPIO.

ECC Error Reporting: Upon detecting an ECC error, the MCH, has the ability to send one of several messages to the ICH2 via the Hub Interface. The MCH can tell the ICH2 to generate either an SMI#, SCI, or SERR# interrupt.

Function Disable: The ICH2 provides the ability to disable the following functions: AC'97 Modem, AC'97 Audio, IDE, USB or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disabled functions.

Intruder Detect: The ICH2 provides an input signal, INTRUDER#, that can be attached to a switch that is activated when the system case being opened. The ICH2 can be programmed to generate an SMI# or TCO interrupt due to an active INTRUDER# signal.

SMBus: The ICH2 integrates an SMBus controller. The SMBus provides an interface to manage peripherals such as serial presence detect (SPD) devices on the RIMM modules and thermal

probes. A slave interface is also provided to enable additional platform manageability. This interface allows an external microcontroller to access system resources, and external system devices the ability to check the system power state, watchdog timer, and system status bits, and generate a system reset and other platform messages.

Alert-On-LAN*: The ICH2 supports Alert-On-LAN. In response to a TCO event (intruder detect, thermal event, processor not booting) the ICH2 sends a hard-coded message over the SMLink. For complete details refer to the Wired for Management (WfM) Design Guide at

http://www.intel.com/ial/wfm/.

1.5 Platform Compliance

This section describes platform compliance with industry standards.

1.5.1 PC 99/2001

The PC 99/2001 is intended to provide guidelines for hardware design that result in the optimal user experience, particularly when the hardware is used with the Windows* family of operating systems. This document includes PC 99/2001 requirements and recommendations for basic consumer and office implementations such as desktop, mobile, and workstation systems, and Entertainment PCs. This document includes guidelines to address the following design issues:

- Design requirements for specific types of systems that run Windows 98*, Windows 2000*, or Windows Millennium* operating systems.
- Design requirements related to OnNow design initiative, including requirements related to ACPI, Plug and Play device configuration, and power management in PC systems.
- Manageability requirements that focus on improving Windows* operating systems with the end goal of reducing TCO.
- Clarification and additional design requirements for devices supported under Windows* operating systems including new graphics and video device capabilities, DVD, scanners and digital cameras, and other devices.

For complete details refer to the *PC 99/2001 System Design Guide* at

http://www.microsoft.com/windows/.

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2 Component Layout

The following processor layout figures do not show the exact component ball count, only the general quadrant information. Only the exact ball assignment should be used to conduct routing analysis. Reference the following documents for ball assignment information.

- *Intel® 860 Chipset: 8260 Memory Controller Hub (MCH) Datasheet*
- *Intel® Xeon™ Processor at 1.40 GHz, 1.50 GHz, 1.7 GHz and 2 GHz Datasheet*
- *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.8 GHz, 2 GHz and 2.2 GHz Datasheet*

2.1 Intel® Xeon™ Processor Component Quadrant Layout

Figure 2 and Figure 3 illustrate the quadrant layout of the Intel Xeon processor and Intel Xeon processor with 512 KB L2 cache, respectively. In the event that this layout conflicts with the processor datasheet, the datasheet supercedes all other data.

Note: All figures in this section are from the top view perspective.

Figure 2. TOP VIEW—Intel® Xeon™ Processor Socket Quadrant Layout

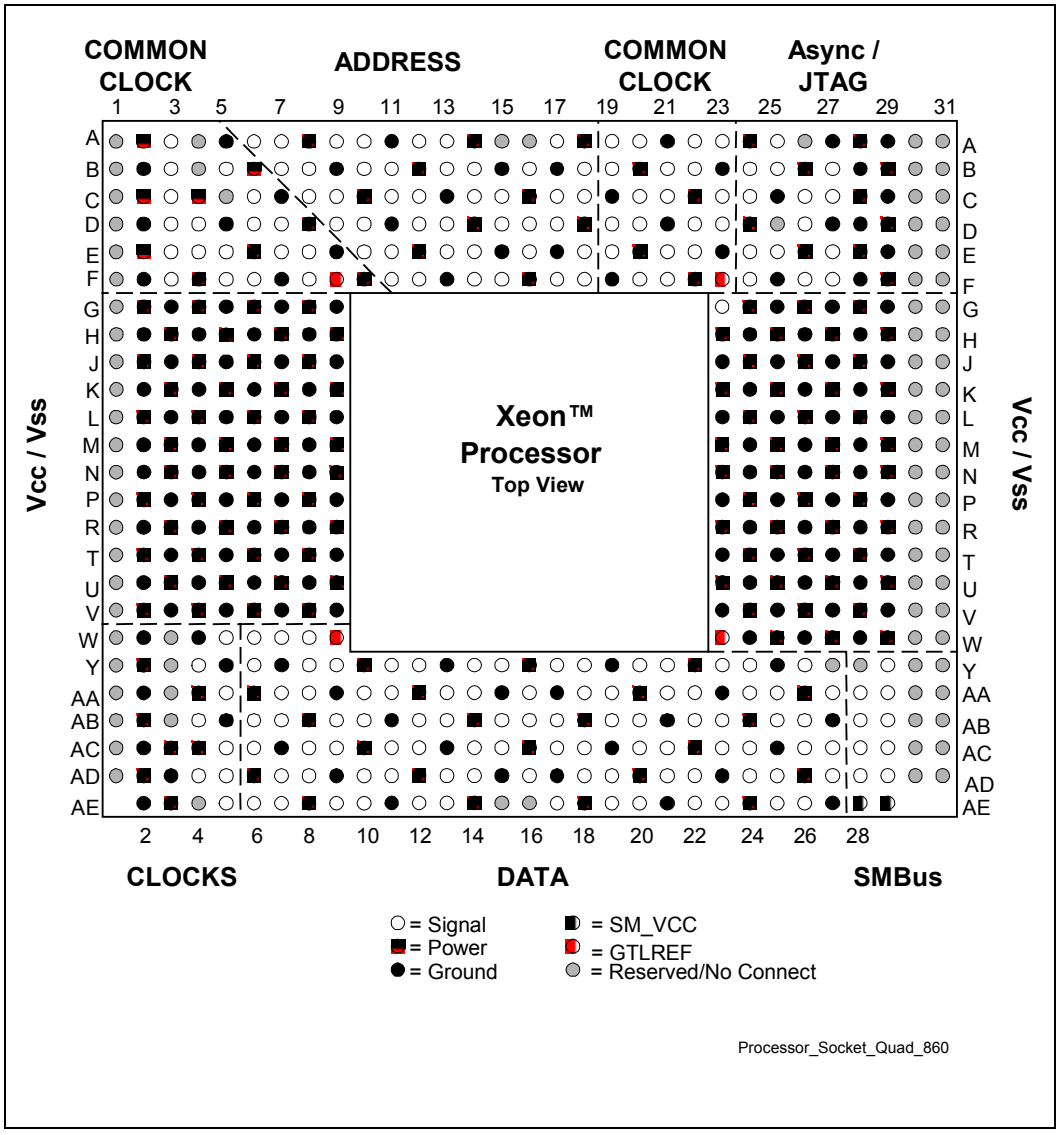
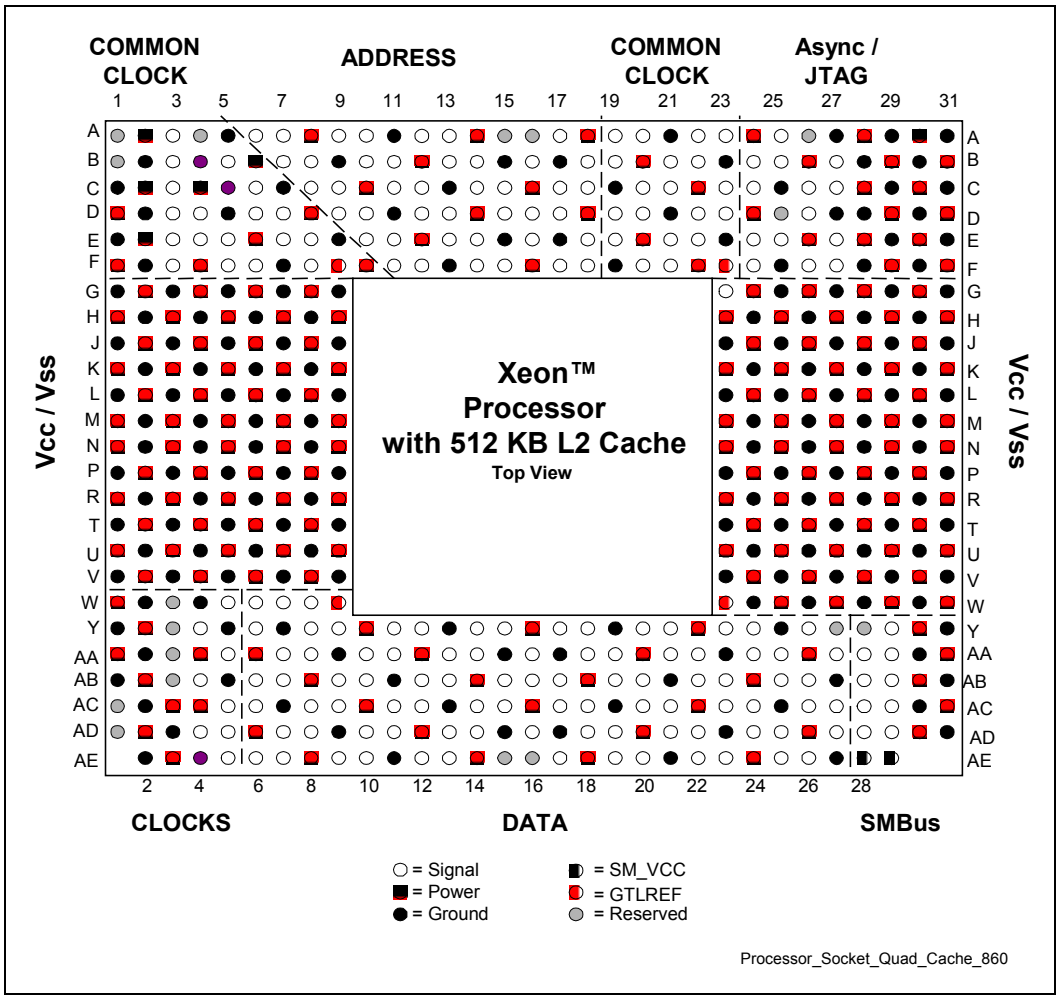


Figure 3. TOP VIEW—Intel® Xeon™ Processor with 512 KB L2 Cache Socket Quadrant Layout



2.2 Intel® 860 Chipset Component Quadrant Layout

Figure 4 through Figure 7 illustrate the quadrant layouts for the Intel 860 chipset components. In the event that information in a component datasheet and this information conflict, the information in the datasheet supercedes.

Figure 4. TOP VIEW—MCH Quadrant Layout

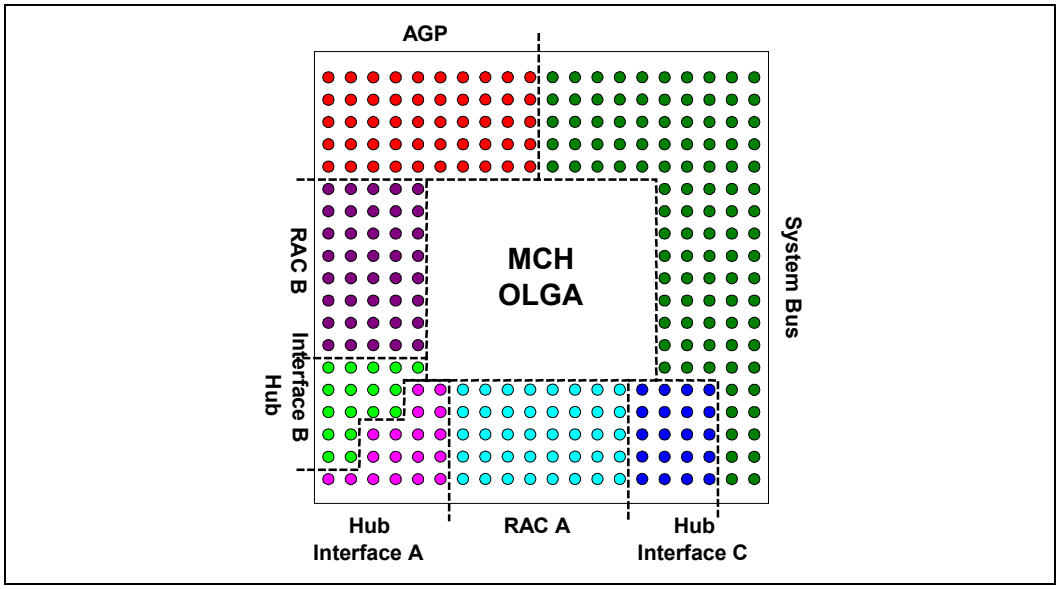


Figure 5. TOP VIEW—Intel® ICH2 Quadrant Layout

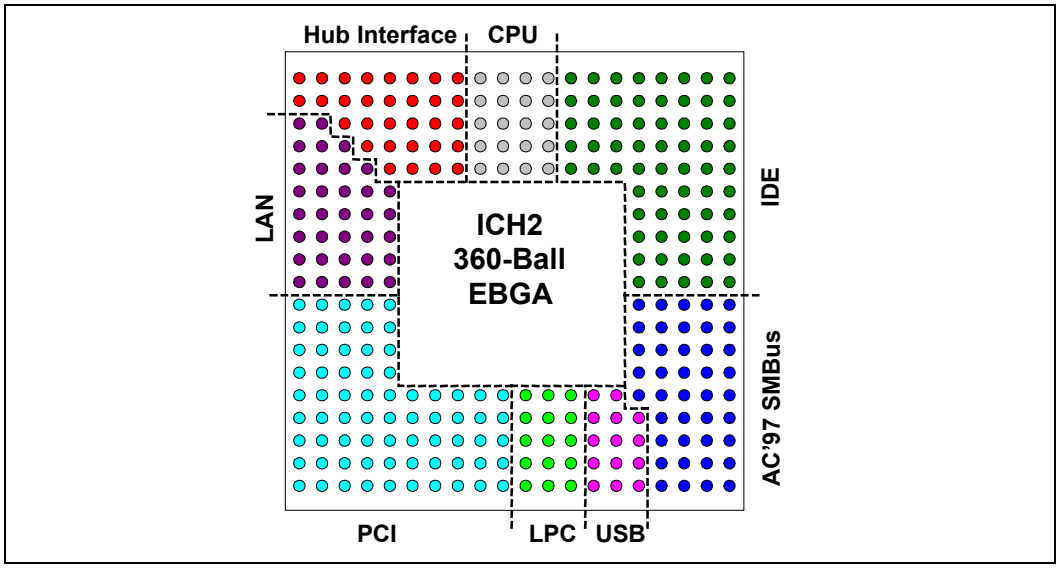


Figure 6. TOP VIEW—Intel® P64H Quadrant Layout

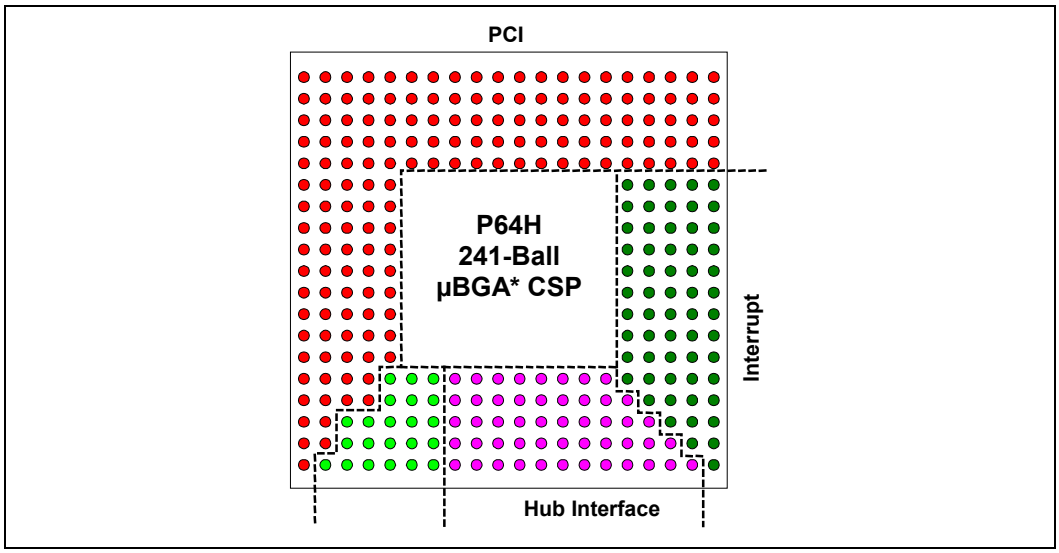
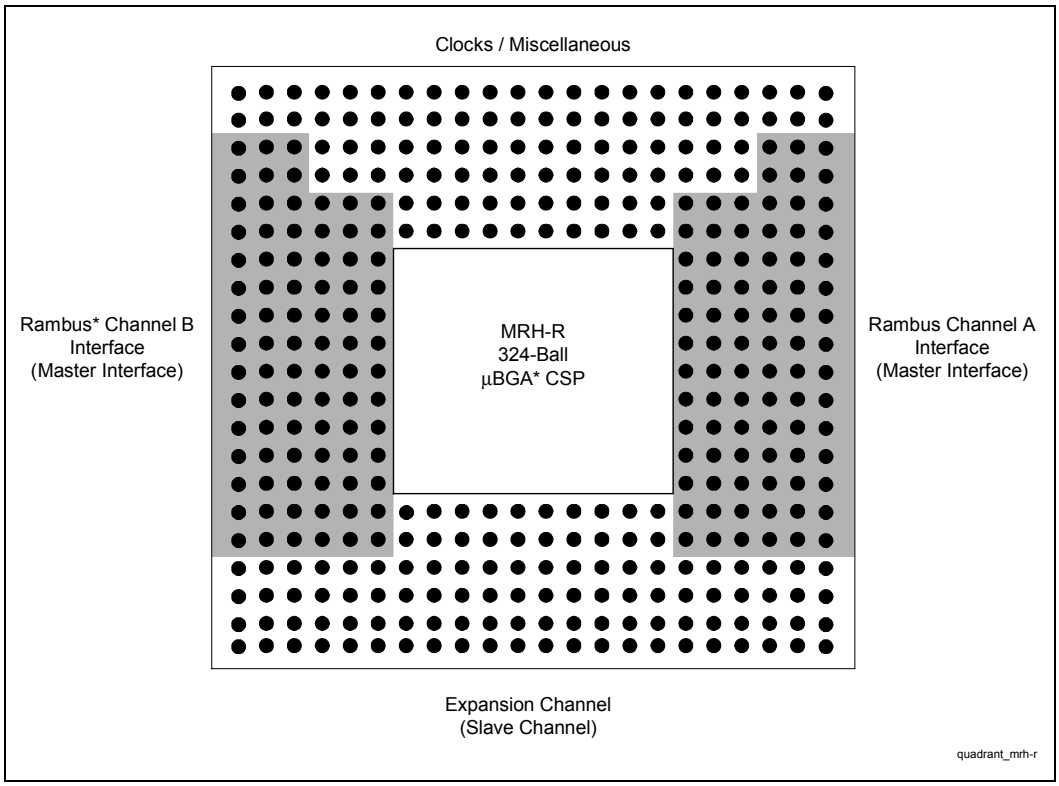


Figure 7. TOP VIEW— Intel® MRH-R Quadrant Layout



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3 Platform Stack-Up and Placement Overview

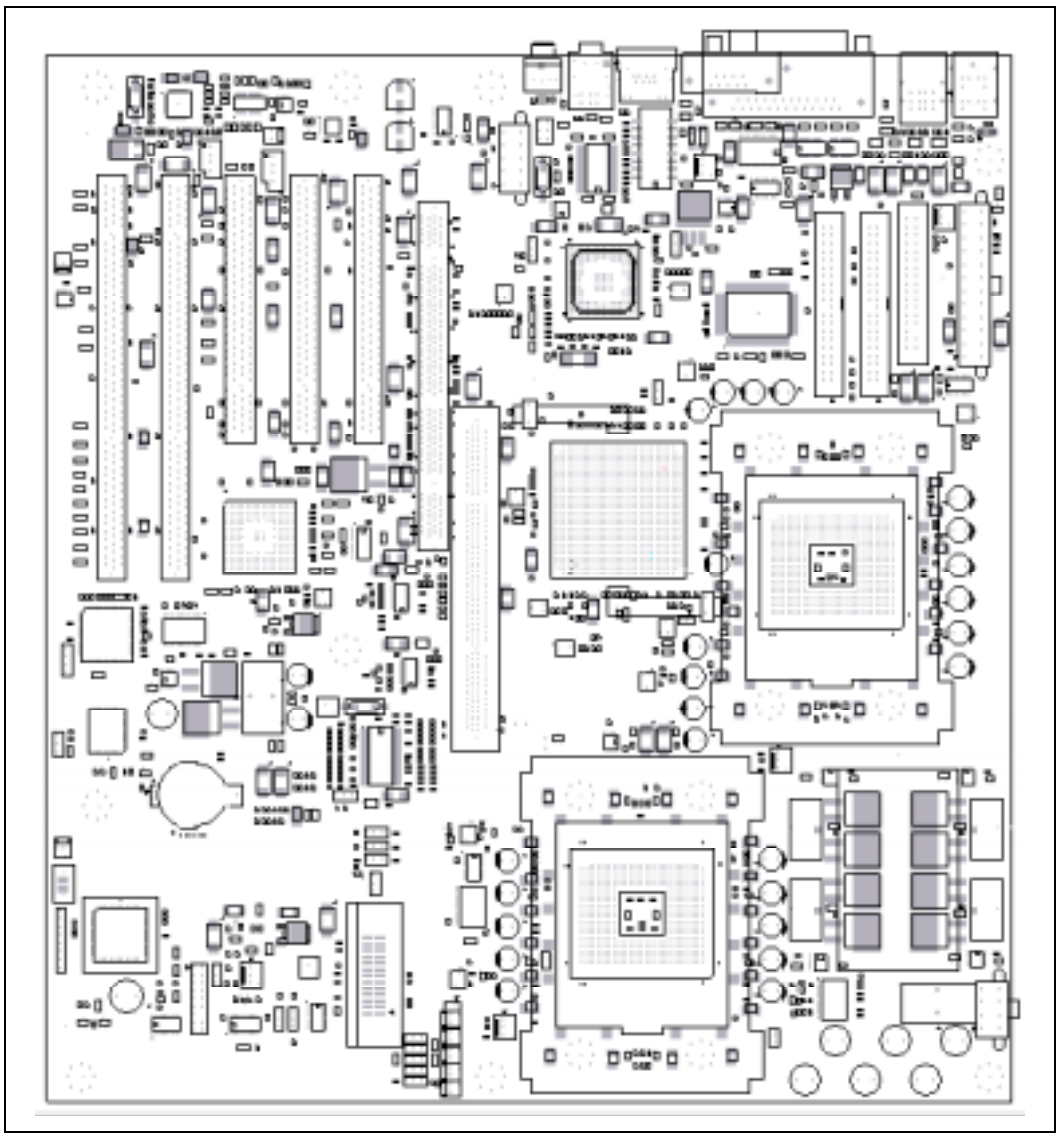
3.1 Platform Component Placement

The following figures illustrate general component placement for workstation systems. The assumptions used for the component placement are described in the following table.

Table 6. Placement Assumptions for Workstation Configurations

System Configuration	Assumptions		
	Form Factor	Number of Total PCB Layers	Assembly
Workstation (DP)	Extended-ATX/Entry SSI	8 Layers	Single Sided

Figure 8. DP Workstation Component Placement Example in an Extended ATX Form Factor



3.2 Two-Way System Stack-Up

Design recommendations are presented first in this section, followed by design considerations.

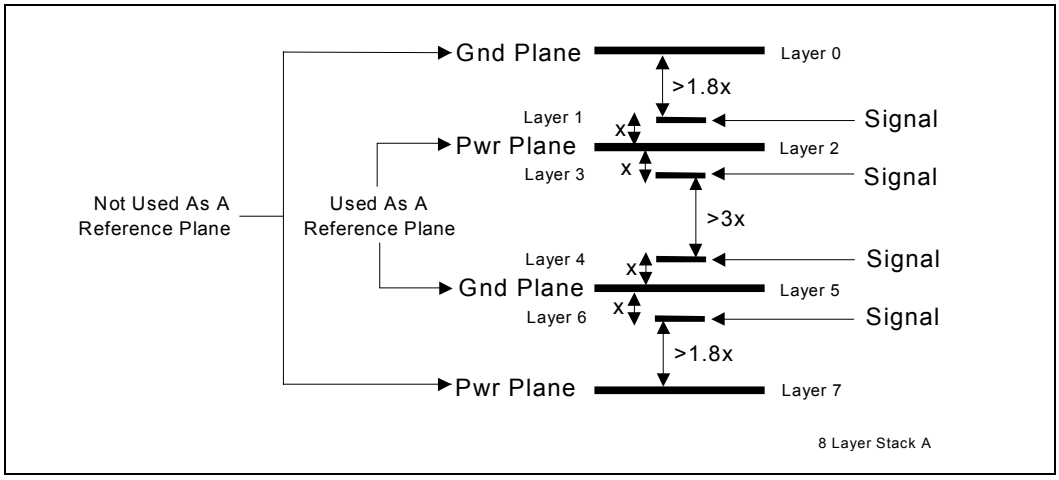
3.2.1 Design Recommendations

3.2.1.1 Stack-Up Option A

A dual processor motherboard stack-up option is shown in Figure 9. Signal layers should be routed as unbalanced stripline referencing layers 2 and 5 only. Stripline routing has fewer mode dependent velocity changes and results in less system timing skew than microstrip. For signals other than the system bus source-synchronous AGTL+ signals, layers 0 and 7 also provide routing room in the presence of surface mount devices, such as the processor sockets. Layers 0 and 7 should not act as reference planes for the system bus signals.

The separations between layers 0 and 1, layers 3 and 4, and layers 6 and 7 should be kept as large as possible. Therefore, the distance between the signal trace and the reference plane should be greater than 1.8x for layers 0 and 1 and layers 6 and 7 (where x is the distance between layers 1 and 2, 2 and 3, 4 and 5, 5 and 6). A distance greater than 3x should be kept between signals on layers 3 and 4. In addition, signals on layers 3 and 4 should be routed orthogonal to each other.

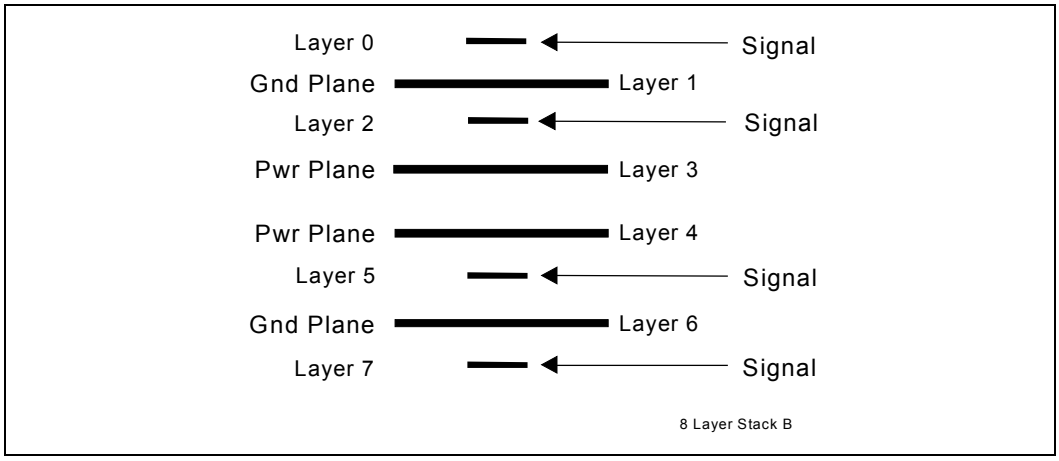
Figure 9. Eight Layer Stack-Up for DP Configurations—Option A



3.2.1.2 Stack-Up Option B

Stack-up option B shown in Figure 10 has the advantage of using symmetric stripline routing preferred for the system bus on layer 2 and layer 5. However, it uses microstrip routing on layer 0 and layer 7. Microstrip routing is worse than the stripline routing of Option A in that it is more susceptible to variations in fab manufacturing and crosstalk. Furthermore, microstrip has a different propagation delay, which must be accounted for in flight time simulations. If Option B is used, all 4X signals must be routed on layer 2 and layer 5. 2X signals should also be routed on the symmetric stripline layers (2 & 5), but may be routed on microstrip layers if necessary. Common clock signals can be routed as microstrip. It is important to prevent layer switching, particularly between stripline and microstrip layers. BCLK signals should be routed on stripline layers. Any signals routed as microstrip must account for the increased crosstalk coefficient, the difference in flight time, and the effect of greater fab variation on skew.

Figure 10. Eight Layer Stack-Up for DP Configurations—Option B



3.2.2 Design Considerations

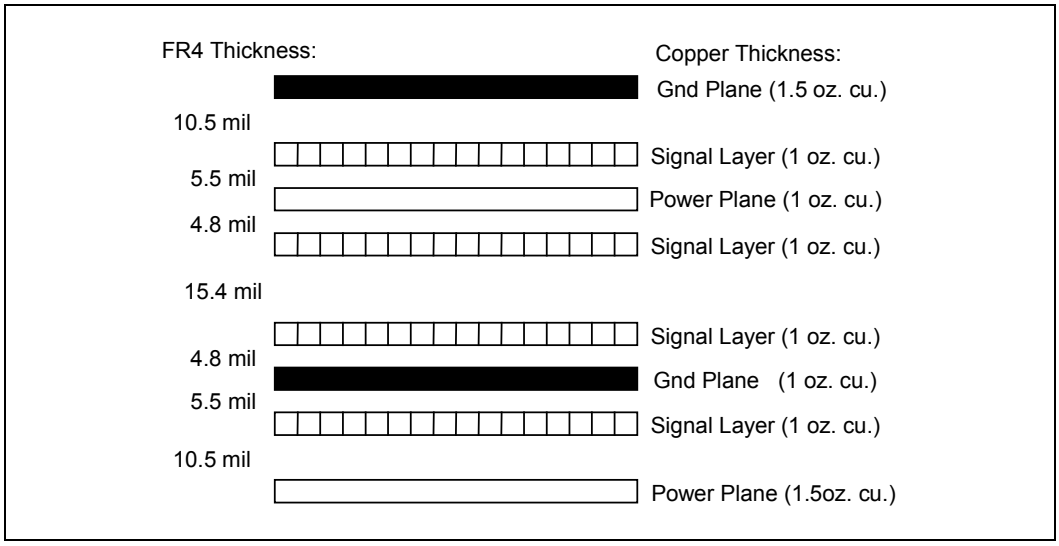
The following design considerations are based on Intel reference designs for the Intel Xeon processor and Intel Xeon processor with 512 KB L2 cache with the Intel 860 chipset. These designs are targeted to provide a high quality platform with optimized signal integrity, timing margins, and power distribution. These design considerations represent Intel's recommended platform design. However, excursions from these guidelines can be made to optimize for cost or system-specific designs without violating the specifications of either the processor or chipset. In any design it is up to the designers to ensure that the platform meets all the component specifications. Intel strongly recommends that a comprehensive simulation analysis be performed to ensure all such specifications will be met. This is particularly important for designs that deviate from the following design considerations.

3.2.2.1 Stack-Up Example A

Use the following items and the stack-up in Figure 11 as the design considerations for the dual processor system stack-up Example A.

- 1 oz. Copper in middle layers.
- There must be the equivalent total of at least 2 oz. Of copper on power planes for power delivery to the processor.
- Vias are 10 mil holes with 35 mil anti-pads (24 mil pads).
- Total board thickness is 0.0685 inches. (Slightly greater than the preferred standard 0.062 inch).

Figure 11. Dual Processor Stack-Up Example



3.2.2.2 Stack-Up Example B

Use the following items and the stack-up in Figure 12 as the design considerations for the dual processor system stack-up Example B. For detailed thickness information, refer to Figure 13.

- A system bus impedance of 50 Ω can be obtained with 5 mil traces for stripline and 7 mil traces for microstrip.
- There must be the aggregate total of at least 2 oz of copper on power and ground planes for power delivery to the processor.
- Vias are 10 mil hole with a 32 mil anti-pad (24 mil pad)
- Total board thickness is 0.062 inches.

Figure 12. Dual Processor Example Stack-Up B

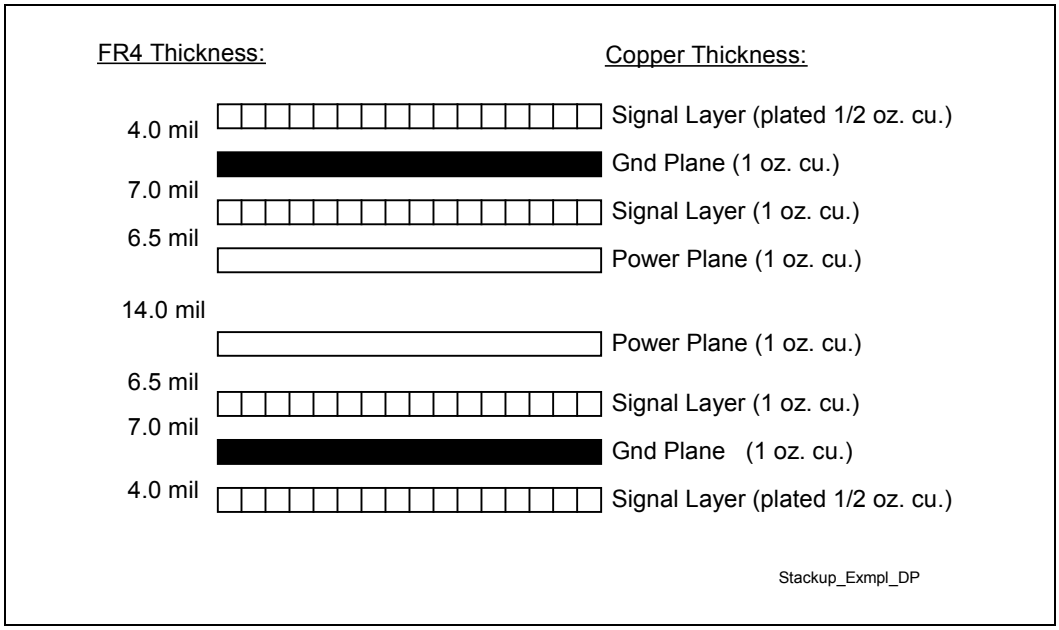
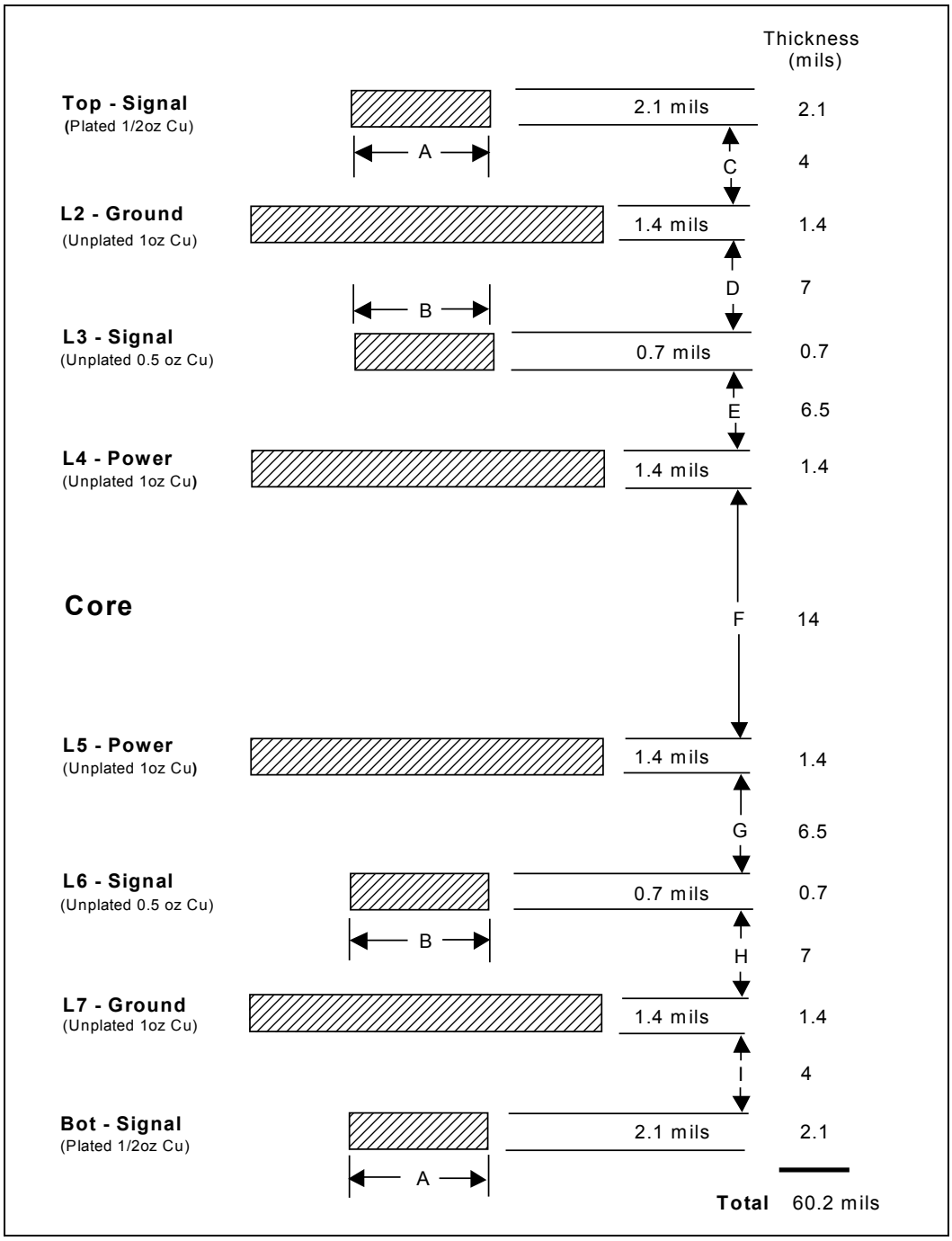


Figure 13. Stack-Up Example B Thickness Summary



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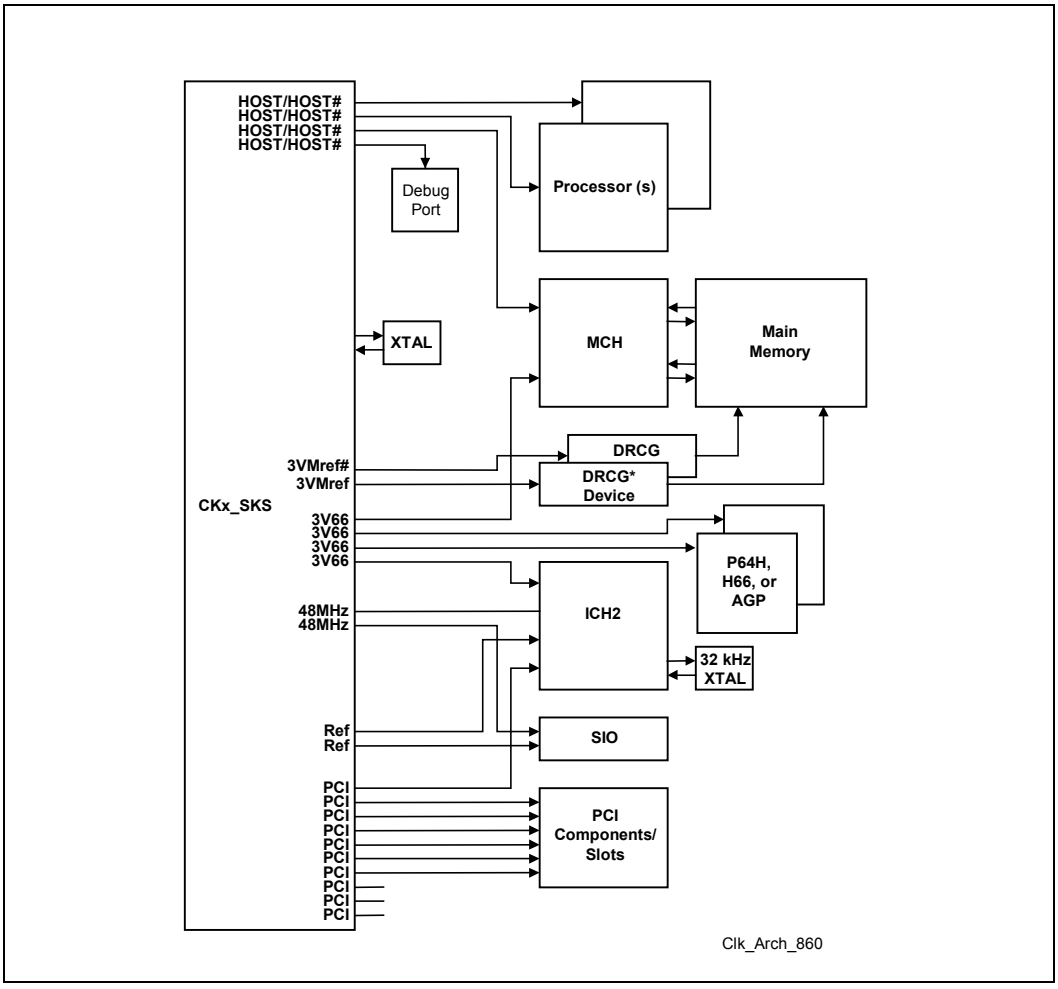
4 Platform Clock Routing Guidelines

Intel recommends CK00 compliant clock drivers for this platform. For more information on CK00 compliance, refer to the *CK00 Clock Synthesizer/Driver Design Guidelines*.

The CK00 design guidelines specify the following platform clocking solution that can be used with this Intel 860 chipset-based design.

The clock synthesizer solution is defined in the CK00 guidelines and is shown in the following figure.

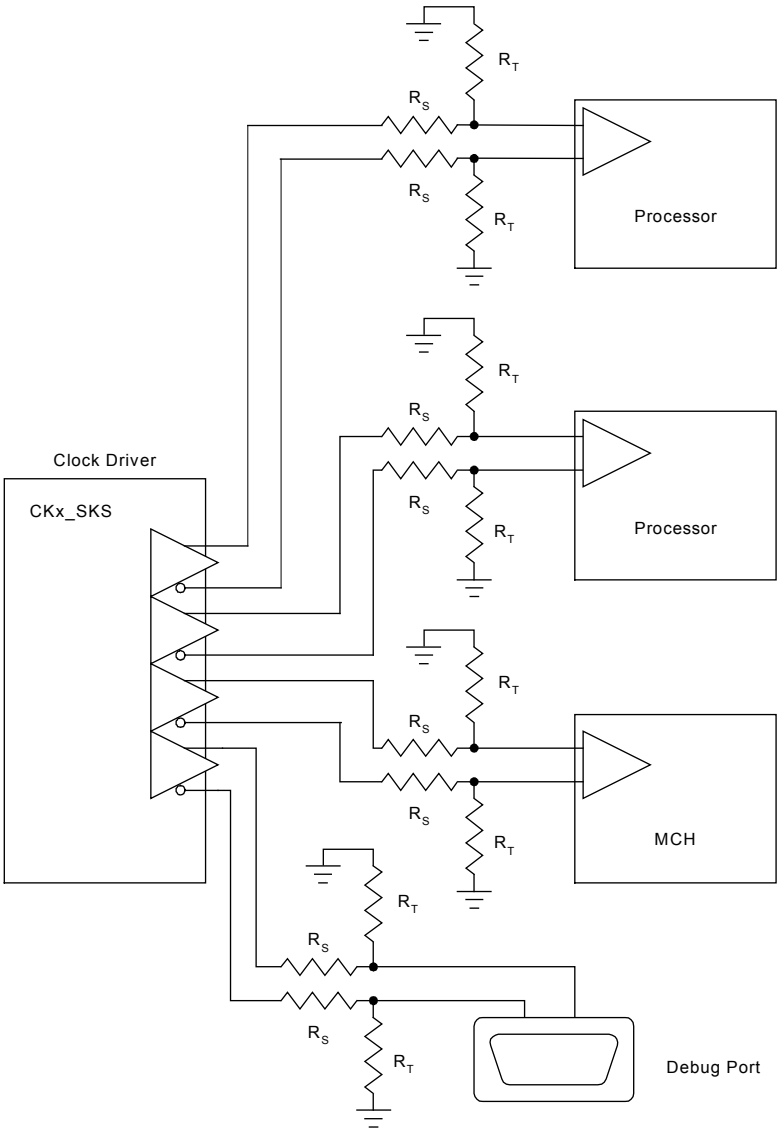
Figure 14. Platform Clocking Architecture Using the CKx_SKS



4.1 Routing Guidelines for Host Clocks

The CKx_SKS clock synthesizer provides four sets of 100 MHz differential clock outputs. The 100 MHz differential clocks are driven to the processors and MCH as shown in Figure 15.

Figure 15. Dual Processor BCLK Topology



NOTE: Connect the CK00 component's HOST pin to the BCLK0 pins on the processor and MCH. Additionally, connect the CK00 HOST_BAR pin to the BCLK1 pins. For production boards, the debug port can be removed and the unused host clocks can be terminated to GND via 10K Ohm resistors.

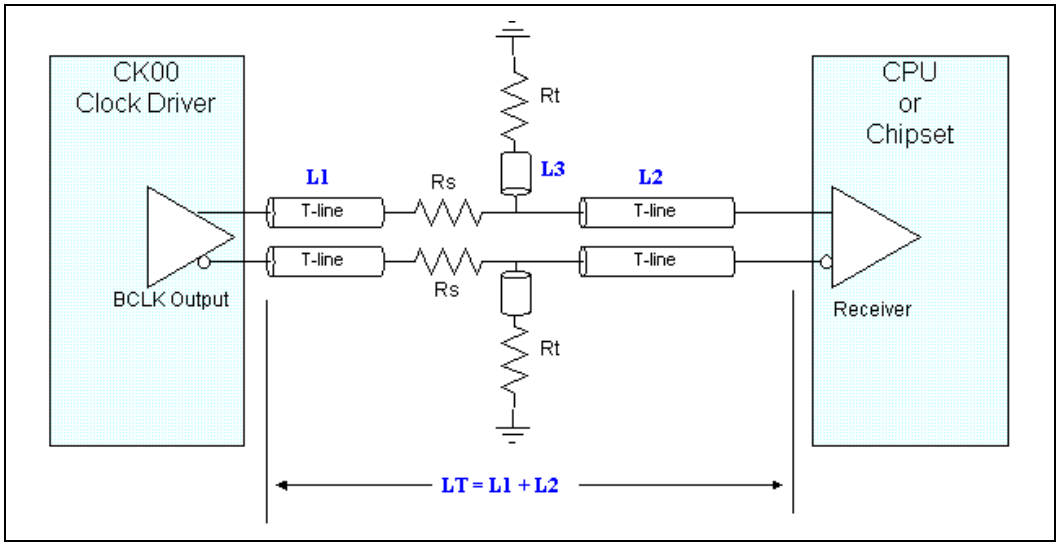
BCLK_Topo

The CK00 clock driver's differential bus output structure is a "Current Mode, Current Steering" output that develops a clock signal by alternately steering a programmable constant current to the external termination resistors R_T. The resulting amplitude is determined by multiplying I_{OUT} by R_T. The current I_{OUT} is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of R_T for impedance matching or to accommodate future load requirements. Refer to the *CK00 Clock Synthesizer/Driver Design Guidelines* for more detailed information.

The recommended termination for the CK00 differential bus clock is a "Shunt Source termination". Refer to Figure 16. Parallel resistors R_T perform a dual function: converting the current output of the CK00 to a voltage, and matching the driver output impedance to the transmission line. The series resistors R_S provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor R_T

The value of R_T should be selected to match the characteristic impedance of the motherboard, and R_S should be between 20 and 33 Ω. Simulations have shown that R_S values above 33 Ω provide no benefit to signal integrity, but do degrade the edge rate.

Figure 16. Source Shunt Termination



The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in ε_r, and the impedance variations due to physical tolerances of circuit board material. Routing on internal layers provides the least amount of ε_r and impedance variation.

- **Requirement:** Do not split up the two halves of a differential clock pair between layers.
- **Goal:** Route clocks to all agents on same physical routing layer.

General Routing Guidelines:

- If layer transition is required, make sure that skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Layer transitions should only be made between routing layers of the same configuration (i.e., stripline layer to stripline layer).
- Keep routes to all agents as short as possible to minimize the cumulative effects of ε_r variations on clock skew.
- Do not place Vias between adjacent complementary clock traces.
- Avoid differential Vias. A via that's placed in one half of a differential pair must be matched by a via in the other half. Can have differential vias within length L1, between clock driver and RS, if needed to shorten length L1.

EMI Constraints:

Clocks are a significant contributor to electro-magnetic interference (EMI) and should be treated with care. The following recommendations can aid in EMI reduction:

- Route clocks on inner layers.
- On internal signal layers maintain a minimum of 100 mils from the edge of the clock traces to the edge of the motherboard.
- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to the VSS reference plane only.

The following table describes the routing guidelines for the bus clock signals.

Table 7. BCLK[1:0]# Routing Guidelines Summary

Layout Guideline	Value	Figures	Notes
BCLK Skew between agents	200 ps total 150 ps for Clock driver 100 ps for interconnect	Figure 17	1, 2, 3
Differential pair spacing	4 x W min. to 5 x W max.	Figure 18	4, 5
Spacing to other traces	25 mils	Figure 18	
Serpentine spacing	Maintain a minimum S/h ratio of > 5/1 Keep parallel serpentine sections as short as possible Minimize 90° bends. Make 45° bends if possible.	Figure 18	
Line width	4.0 mil typical		6
Motherboard Impedance–Differential	100 Ω typical		7
Motherboard Impedance–single ended	50 Ω ± 10%		8
Processor routing length–L1: CK_WBY/CK_SKS to Rs	0.5 inch max	Figure 16	
Processor routing length–L2: Rs to Processor	0 inch–12 inches	Figure 16	
MCH routing length–L1: CK_WBY/CK_SKS to Rs	0.5 inch max	Figure 16	
MCH routing length–L2: Rs to Processor	0 inch–12 inches	Figure 16	
L3: Stub length to Rt	Stubless 10 mils max from via to pad	Figure 16	
Processor to CS length matching (LT)	0.3 inch ± 0.010 inch MCH LT must be 0.3 inch longer than Processor LT.	Figure 16	9
Processor to Processor length matching (LT)	± 10 mils	Figure 16	10
BCLK0–BCLK1 length matching	± 10 mils		
Rs Series termination value	33 Ω ± 5%	Figure 16	11
Rt Shunt termination value	49.9 Ω ± 1%	Figure 16	12

NOTES:
1. The skew budget includes clock driver output pair to output pair jitter (differential jitter), and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents. This number does not include clock driver common mode (cycle to cycle) jitter, or spread spectrum clocking.
2. This number assumes all BCLK pairs are routed on the same signal layer.
3. Skew measured at the load between any two bus agents. Measured at the crossing point.
4. Edge-to-edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.

5. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing because this will degrade the noise rejection of the network.
6. Set trace width to meet correct motherboard impedance. The value for trace width provided here is a recommendation on how to meet the proper trace impedance based on the recommended stack-up.
7. The differential impedance of each clock pair is approximately 2*Zsingle-ended*(1-2*Kb) where Kb is the backwards crosstalk coefficient. For the recommended trace spacing, the Kb is very small and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
8. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the BCLK traces vary within the tolerances specified, both traces of a differential pair must vary equally.
9. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor at die pad. Therefore, the motherboard trace length for the chipset will be longer than that for the processor.
10. Length of LT for one processor must match the LT of all other BCLK traces to other processors with specified tolerance.
11. Rs values of 20 Ω–33 Ω have been found to be effective. The value specified is the recommended value.
12. Rt values should match the motherboard trace impedance for BCLK.

Figure 17. Clock Skew as Measured from Agent-to-Agent

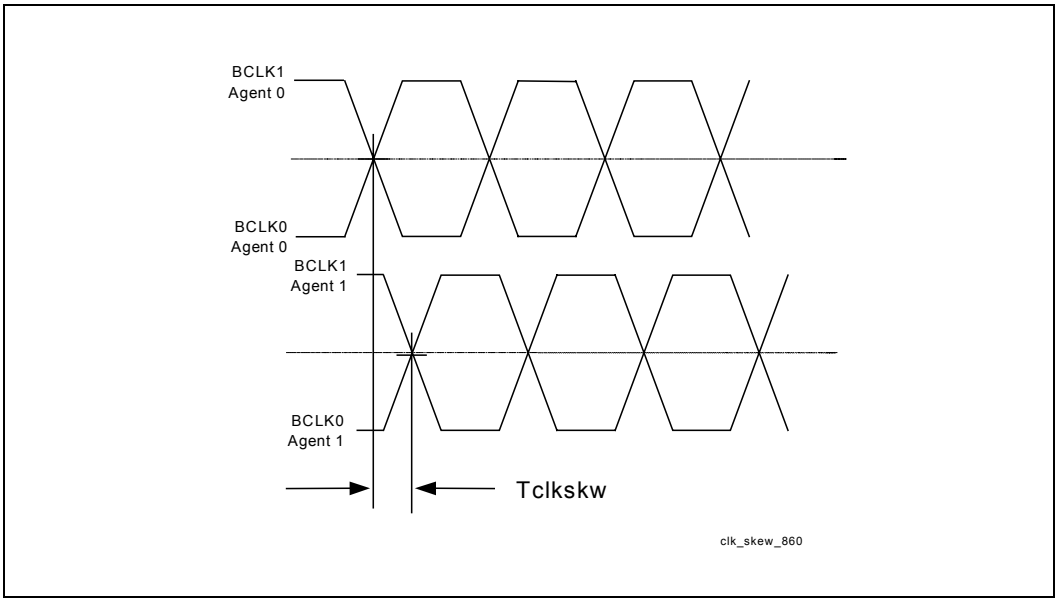
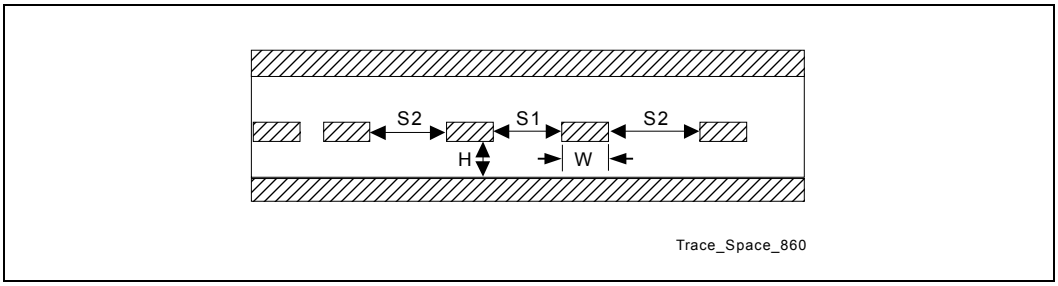


Figure 18. Trace Spacing



4.2 Routing Guidelines for Direct Rambus* Clock Generators (DRCG Devices)

The CKx_SKS clock synthesizer provides two 3.3 V clock reference outputs [3 Vmref and 3 Vmref#] that are used by the Direct Rambus Clock Generators (DRCG devices). Two DRCG devices are required in an Intel 860 chipset dual Rambus Channels interface.

These reference clocks operate at one-half the host clock frequency. They are inputs into the DRCG devices and are used to generate the Direct Rambus* Clock Generator "Clock-to-Master" differential pair (CTM, CTM#).

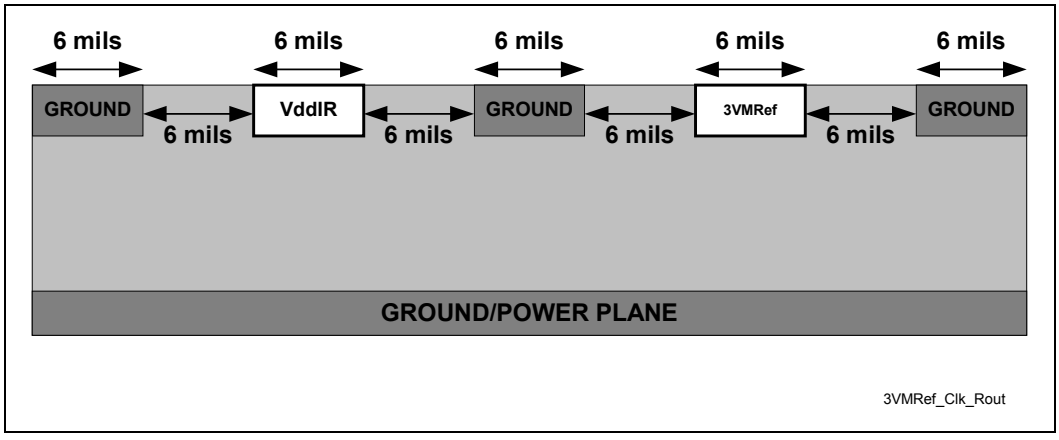
In addition, the DRCG device uses phase information provided by the MCH via the RCLKOUT and HCLKOUT phase aligning clock signals. This phase alignment information is sent to the DRCG SYNCLKN and PCLKM pins from MCH RCLK and HCLK.

4.2.1 CKx_SKS to DRCG: Reference Clocks

The 3VMRef clock output must be routed as shown in Figure 19. Note that the VddIR power pin on the DRCG device can be connected directly to 3.3 V near the DRCG device if the 3.3 V plane extends near the DRCG device. However, if a 3.3 V trace must be used, it should originate at the clock synthesizer and be routed as shown. The maximum length for the 3VMRef and 3VMRef# signals is 8 inches.

Note: The following recommendations assume routing of the reference clocks on microstrip.

Figure 19. VddIR and 3VMRef or 3VMRef# Routing



Note: 3VMRef# should be routed in a similar manner as 3 VMRef.

4.2.2 MCH to DRCG* Device: Phase Aligning Clocks

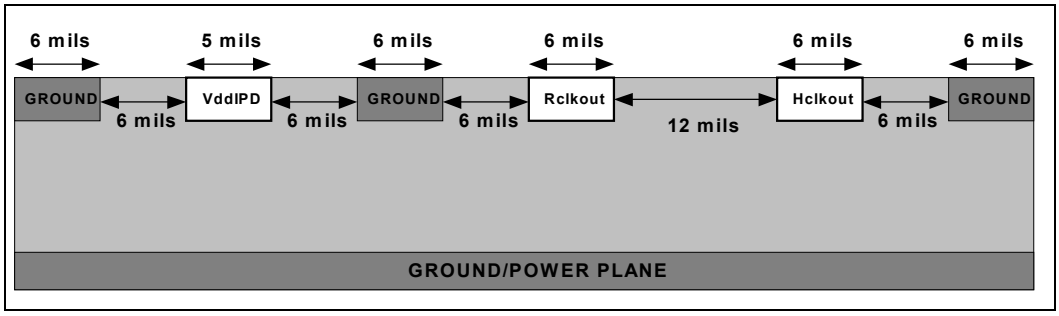
The RCLKOUT and HCLKOUT signals from the MCH should be routed to the SYNCLKN and PCLKM signals on the DRCG device, respectively, as shown in Figure 20. Note that the VddIPD power pin on the DRCG device can be connected directly to 1.8 V near the DRCG device if the 1.8 V plane extends near the DRCG device. However, if a 1.8 V trace must be run, it should originate at the MCH and be routed as shown with respect to RCLKOUT and HCLKOUT.

The maximum length for RCLKOUT and HCLKOUT is 6 inches. Additionally, these signals must be length matched within 50 mils. These signals should be routed on the same layer. If these signals must switch layers, then BOTH signals should change layers together.

If the VddIPD pin is connected to the 1.8 V plane using a via (i.e., trace is not run from the MCH), then HCLKOUT and RCLKOUT must still be routed as shown in Figure 20 and ground isolated.

Note: The following recommendations assume routing of the phase alignment clocks on microstrip.

Figure 20. MCH to DRCG* Device Routing Diagram



Note: The signals RCLKOUT and HCLKOUT are channel specific, and their exact names are CHx_RCLKOUT and CHx_HCLKOUT, where x is the channel (either A or B). Consult the *Intel® 860 Chipset: 82860 Memory Controller Hub (MCH) Datasheet* for more information.

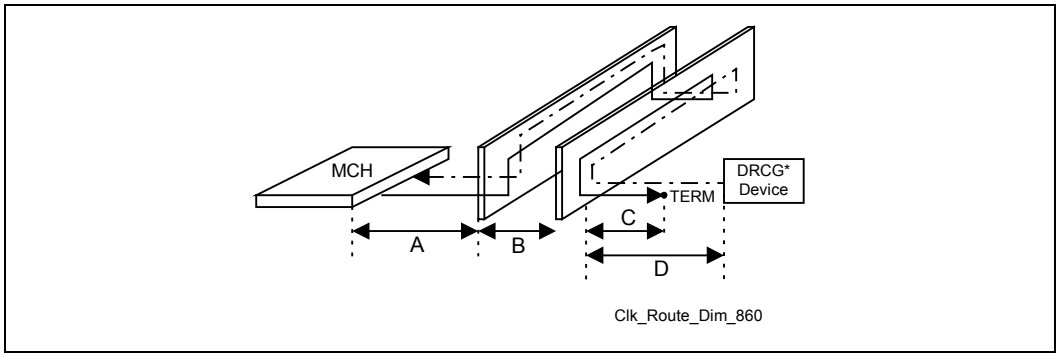
4.2.3 DRCG* Device Signals to Rambus* Channels (300 MHz/400 MHz Clocks)

The Direct Rambus* Clock Generator (DRCG device) signals (i.e., CTM/CTM# and CFM/CFM#) are high-speed, impedance matched transmission lines that require strict routing recommendations to insure that the memory timings are met. The following DRCG device recommendations should be strictly followed. Any deviations from the recommendations should be properly simulated.

4.2.3.1 Trace Length Recommendations

Figure 21 shows the critical Direct Rambus Clock Generator routing sections, with the routing lengths for each section defined in Table 8.

Figure 21. Direct Rambus* Clock Generator Routing Dimension



The following table shows the routing length recommendations for the CTM/CTM# and CFM/CFM# 400 MHz Direct Rambus Clock Generator. Note that the recommendations are shown for a single Rambus Channel and should be applied to both of the MCH Rambus Channels.

Table 8. Direct Rambus* Clock Generator Routing Guidelines

Clock	From	To	Length (inches)	Figure 21 Trace
CTM/CTM# (1)	DRCG* Device	2nd RIMM Connector	0.0–6.0	D
	RIMM Connector	RIMM Connector	0.4–1.0	B
	1st RIMM Connector	MCH	1.0–6.0	A
CFM/CFM# (2)	MCH	1st RIMM Connector	1.0–6.0	A
	RIMM Connector	RIMM Connector	0.4–1.0	B
	2nd RIMM Connector	Termination	0.0–2.0	C

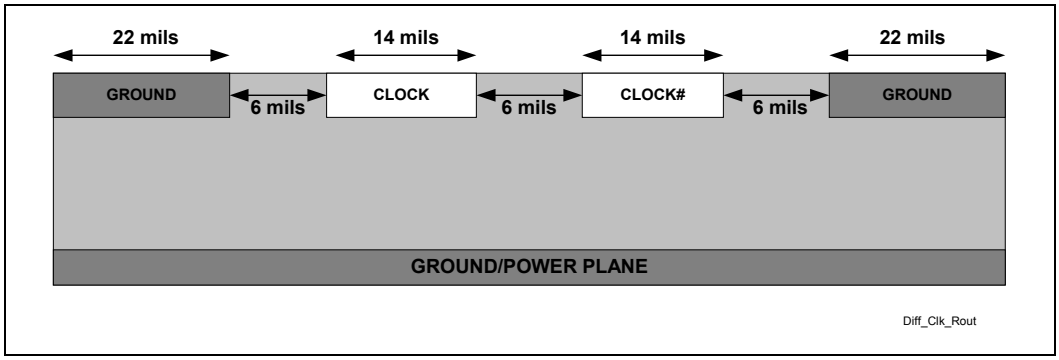
NOTES: .
1. First RIMM connector to MCH:
   Trace length must be compensated to match the RSL signals from MCH to first RIMM connector.
2. MCH to First RIMM connector:
   Trace length must be compensated to match the RSL signals from first RIMM connector to MCH.

In clock routing sections ‘A’ and ‘D’, the clock signals (CTM/CTM# and CFM/CFM#) should be routed differentially. An example recommended topology for microstrip differential clock routing is shown in Figure 22.

Note: Clock trace widths and spacing may change according to prepreg thickness.

The clock signals shown in the example topology are 14 mils wide and are routed differentially. There must be a 22 mil ground isolation trace routed around the clock differential pair signals. The 22 mil ground isolation traces must be connected to ground with a via per every 1 inch. Vias must be placed within 0.5 inch of the beginning and end of the ground isolation trace. A 6 mil gap is required between the clock signals, and between the clocks and ground isolation traces.

Figure 22. Differential Clock Routing Diagram



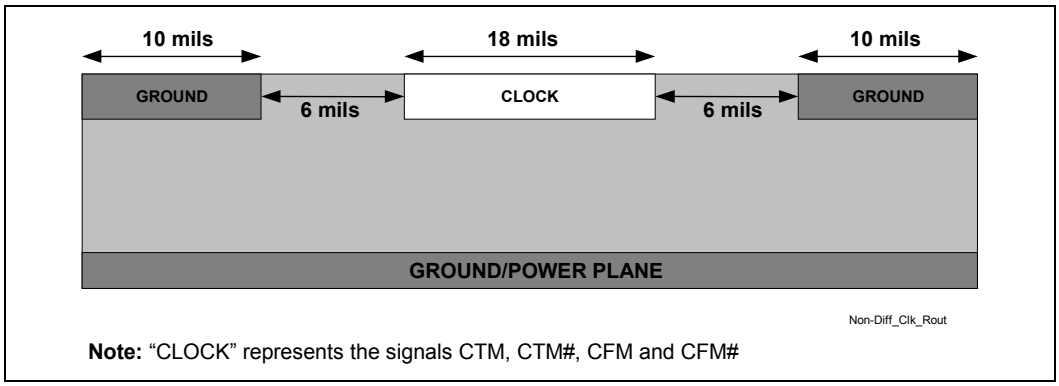
Note: "CLOCK" stands for the CTM and CFM signals, and "CLOCK#" stands for the CTM# and CFM# signals.

In clock routing section 'B', the CTM/CTM# and CFM/CFM# clock signals should be routed non-differentially because of the short routing lengths between RIMM connectors. An example recommended topology for microstrip non-differential clock routing is shown in Figure 23.

Note: Clock trace widths and spacing may change according to prepreg thickness.

The clock signals shown in the example topology are routed with 18 mil wide traces. When routing the clocks non-differentially, there must be a 10 mil ground isolation trace routed around the single-ended clock signals. The 10 mil ground isolation traces must be connected to ground with a via per every 1 inch. Vias must be placed within 0.5 inch of the beginning and end of the ground isolation trace. A 6 mil gap is required between the clock signals and the ground isolation traces.

Figure 23. Non-Differential Clock Routing Diagram



Note: The CTM/CTM# and CFM/CFM# clock signals must be ground referenced (with continuous ground island/plane) at all times.

4.2.3.2 Topology Considerations

Package trace compensation, via compensation, and RSL signal layer alteration must also be considered when routing the Direct Rambus Clock Generator. Additionally, when routing on microstrip layers, 0.021 inches of CLK per 1 inch of RSL trace length must be added to compensate for the clock's faster trace velocity.

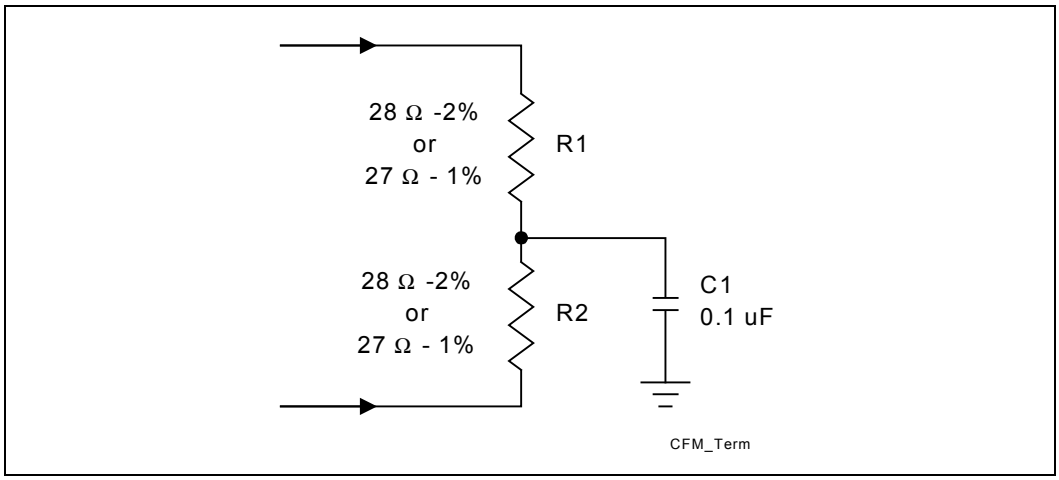
For clock routing sections 'A' and 'B', the CTM/CTM# and CFM/CFM# clocks must be length matched within ± 2 mils to the RSL channel trace length. Exact matching is preferred.

For trace sections 'C' and 'D', the CFM/CFM# clocks must be length matched within ± 2 mils to the RSL channel trace length. Exact matching is preferred.

4.2.3.3 Clock Termination

The CFM/CFM# differential pair signals require termination using either 27 Ω 1% or 28 Ω 2% resistors and a 0.1 µF capacitor as shown in the following figure.

Figure 24. CFM/CFM# Termination



4.2.4 DRCG* Device Impedance Matching Circuit

The external DRCG device impedance matching circuit is shown in the following figure.

Figure 25. DRCG* Device Impedance Matching Network

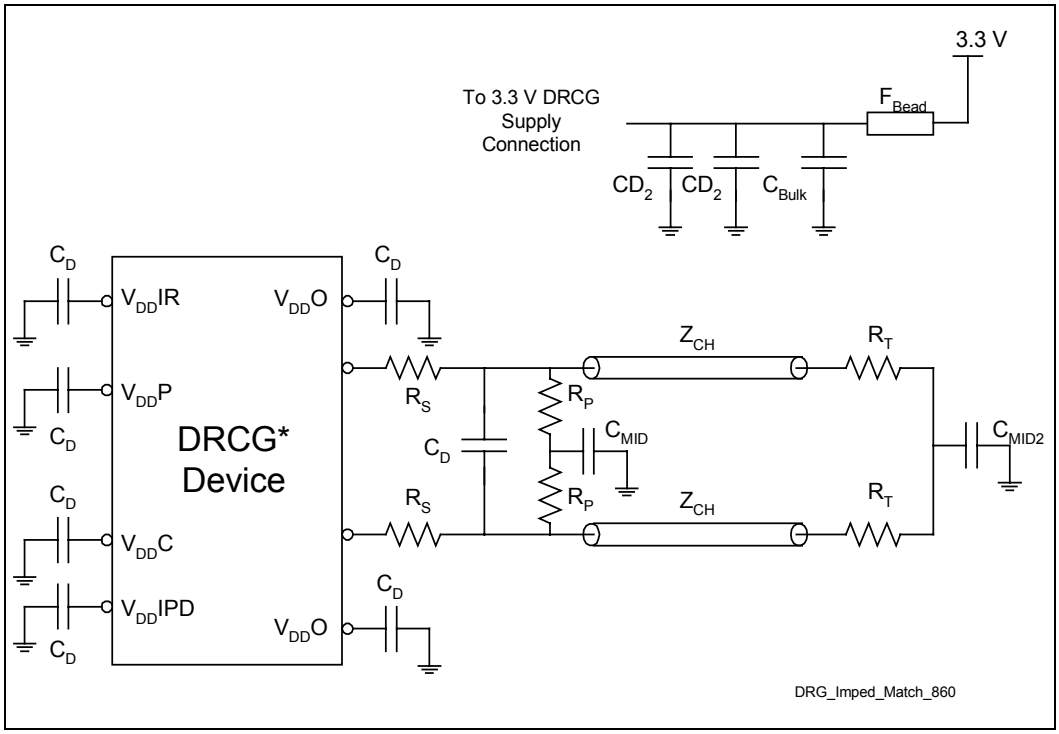


Table 9. DRCG* Device Impedance Matching Network Values

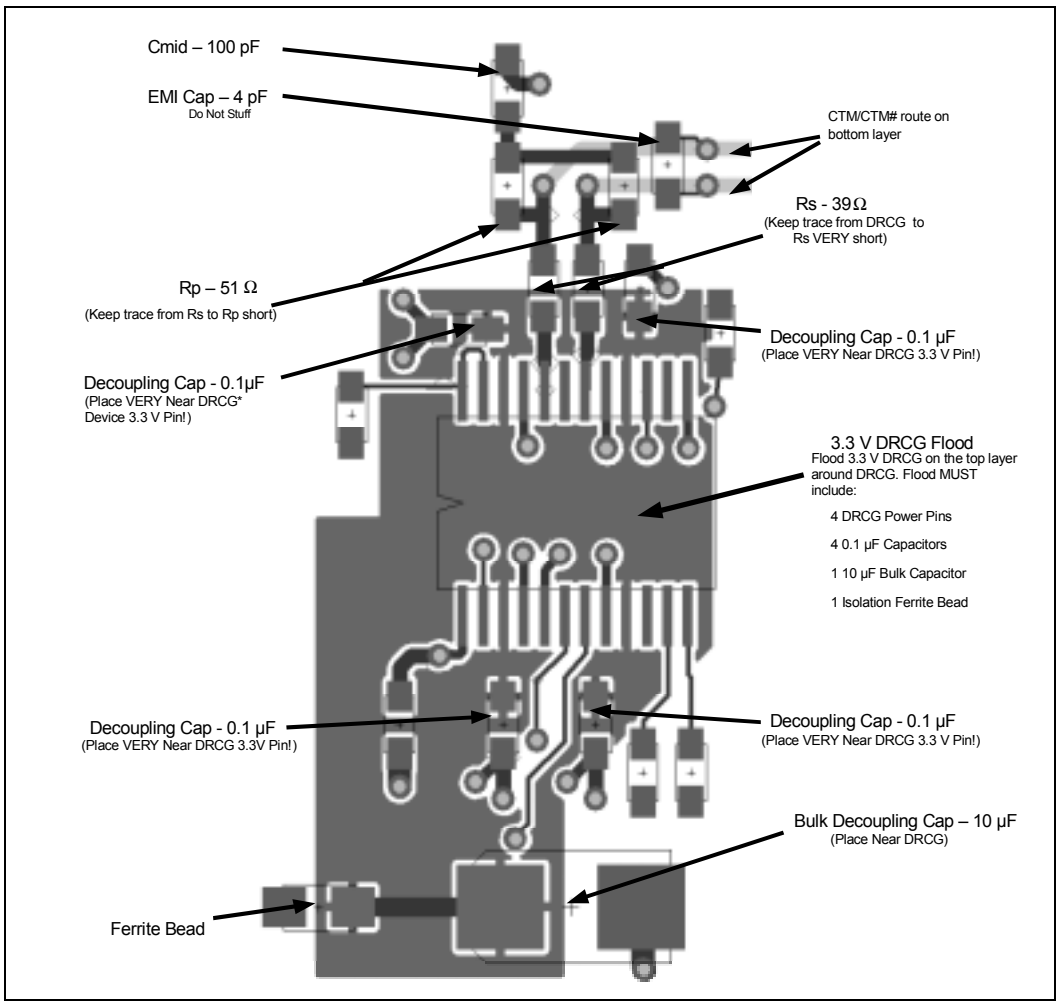
Component	Nominal Value	Notes
C_D	0.1 µF	Decoupling caps to GND
R_S	39 Ω	Series termination resistor
R_P	51 Ω	Parallel termination resistor
C_{MID1}, C_{MID2}	0.1 µF	Virtual GND caps
R_T	27 Ω	End of channel termination
C_F	4 pF–15 pF	Do Not Stuff, leave pads for future use
Fbead	50 Ω at 100 MHz	Ferrite bead
CD2	0.1 µF	Additional 3.3 V decoupling caps
Cbulk	10 µF	Bulk cap on device side of ferrite bead

NOTES:

1. Note the removal of the original EMI capacitors between the junctions of RS, RP and ground. These capacitors had minimal impact on EMI and increased DRCG device output jitter by approximately 2X.
2. The intent of component CF is to decouple CLK and CLKB outputs to each other, but data shows this actually increases device jitter. CF should not be stuffed at this time.
3. The ferrite bead and 10 µF bulk cap combination improves jitter and helps to keep the clock noise away from the rest of the system. The additional 3.3 V capacitors (CD2) have a minor positive impact, but the ideal values have not been extensively optimized.
4. 0.1 µF capacitors are better than 0.01 µF or 0.001 µF capacitors for DRCG device decoupling. Most decoupling experiments that replaced 0.1 µF capacitors with higher frequency caps ended up with the same or worse jitter. Replacing existing 0.1 µF capacitors with higher frequency capacitors is not advised.
5. Cmid at 0.1 µF has improved jitter versus Cmid at 100 pF. However, this will increase the latency coming out of a stop clock or tri-state mode.
6. RS, RP, RT were modified to improve channel signal integrity through increasing CTM/CTMN swing.
7. The circuit shown is required to match the impedance of the DRCG device to the 28 Ω channel impedance. More detailed information can be found in the Direct Rambus* Clock Generator Specification.
8. The previously recommended 15 pF capacitors on CTM/CTM# should be removed. The 4 pF capacitor shown in Figure 26 should not be stuffed.

4.2.5 DRCG* Device Layout Example

Figure 26. DRCG* Device Layout Example

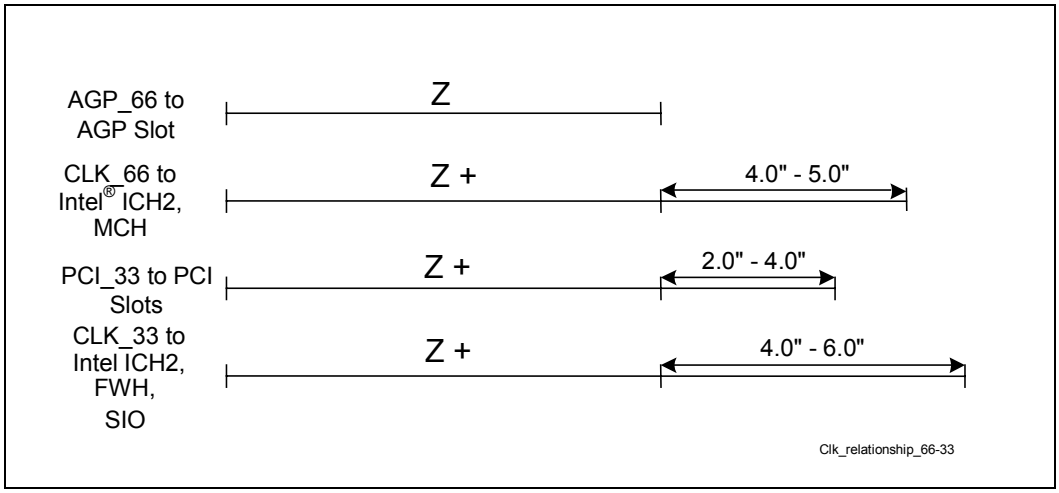


4.3 Routing Guidelines for 66 MHz and 33 MHz Clocks

4.3.1 66 MHz/33 MHz Clock Relationships

Figure 27 shows the clock routing relationships between the 66 MHz clocks and the 33 MHz clocks.

Figure 27. 66 MHz/33 MHz Clock Relationships



4.3.2 66 MHz Clock Routing Length Guidelines

Table 10 summarizes the layout recommendations between the CK00 clock synthesizer and the AGP connector, MCH and ICH2 components, which require a 66 MHz clock. Figure 28 and Figure 29 show traces A and B.

Table 10. 66 MHz Clock Routing Length Guidelines

Clock Group	Length of Trace A (inches)	Length of Trace B (inches)	R1 (Ω)
AGP_66	0 to 0.5	Z	33
CLK_66	0 to 0.5	Z + (4 to 5)	33

Note: The routing length value of Z is 5 to 9 inches.

Figure 28 and Figure 29 show the recommended clock routing topologies for the 66 MHz clocks.

Figure 28. AGP_66 Clock Routing Topology

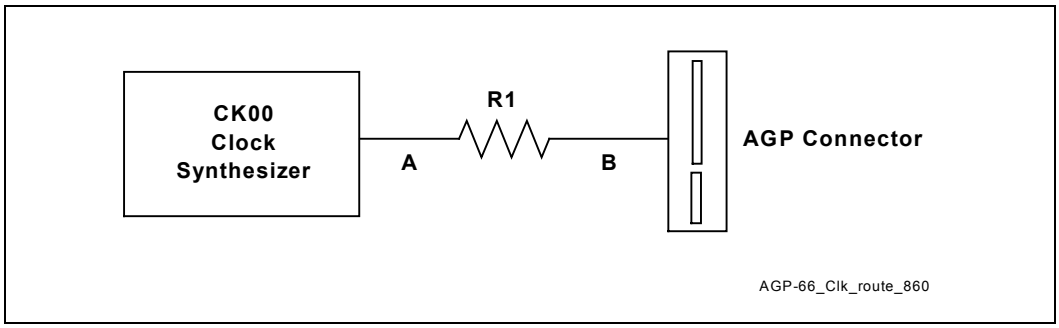
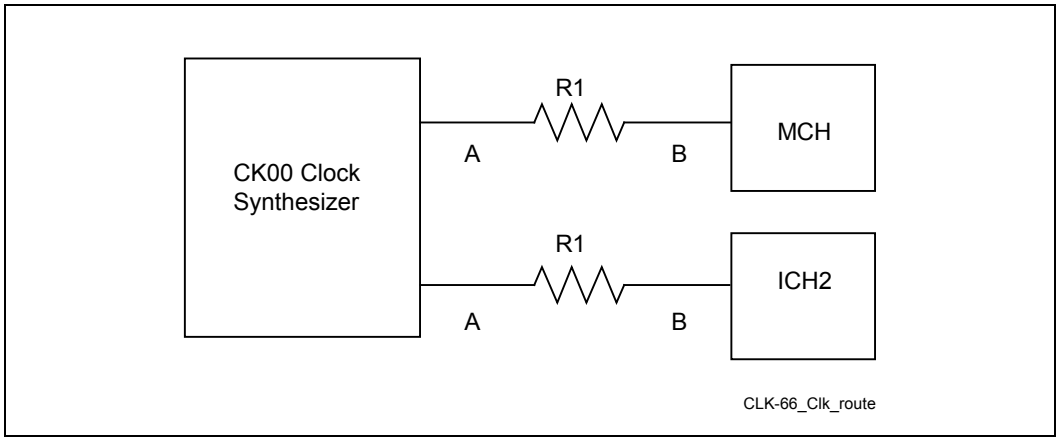


Figure 29. CLK_66 Clock Routing Topology



4.3.3 33 MHz Clock Routing Length Guidelines

Table 11 summarizes the layout recommendations between the CK00 clock synthesizer and PCI connectors, ICH2, FWH Flash BIOS and SIO components, which require a 33 MHz clock. Figure 30 and Figure 31 show segments A and B.

Table 11. 33 MHz Clock Routing Guidelines

Clock Group	Length of Trace A (inches)	Length of Trace B (inches)	R1 (Ω)
PCI_33	0 to 0.5	Z + (2 to 4)	33
CLK_33	0 to 0.5	Z + (4 to 6)	33

Note: The routing length value of Z is 5 to 9 inches.

Figure 30 and Figure 31 show the recommended clock routing topologies for the 33 MHz clocks.

Figure 30. PCI_33 Clock Routing Topology

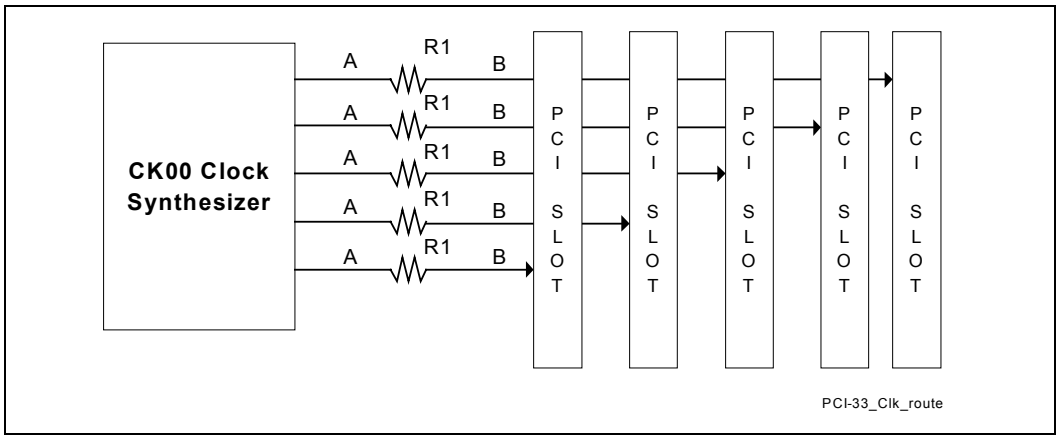
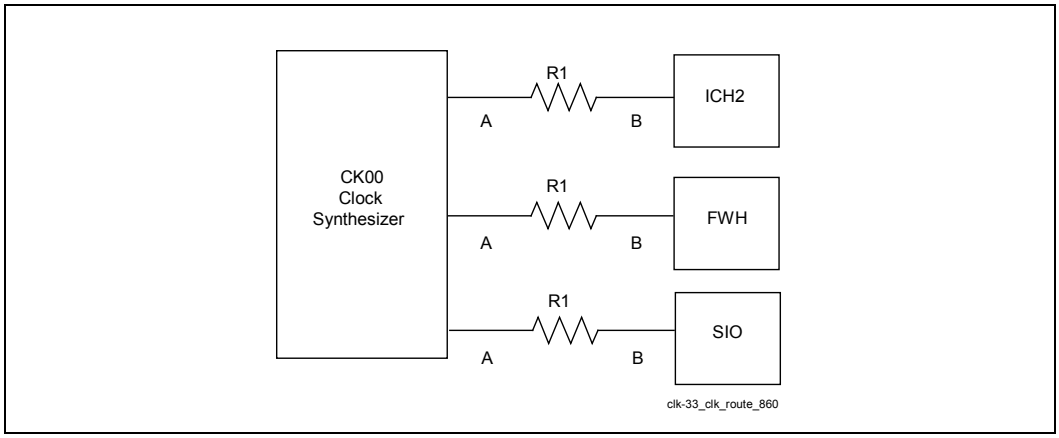


Figure 31. CLK_33 Clock Routing Topology



4.3.4 Intel® P64H PCI Clock Routing Guidelines

4.3.4.1 Intel® P64H PCI 33 MHz Clock Routing Guidelines

At 33 MHz, the P64H can support 4x33 MHz PCI slots. The P64H can provide 6 copies of the PCLKOUT to PCI devices on its primary PCI bus. PCLKFBOUT is used as the feedback clock and must be routed into PCLKFBIN of the P64H. The PCLKOUT routing guidelines are shown below:

Figure 32. Intel® P64H PCI 33 MHz Clock Routing

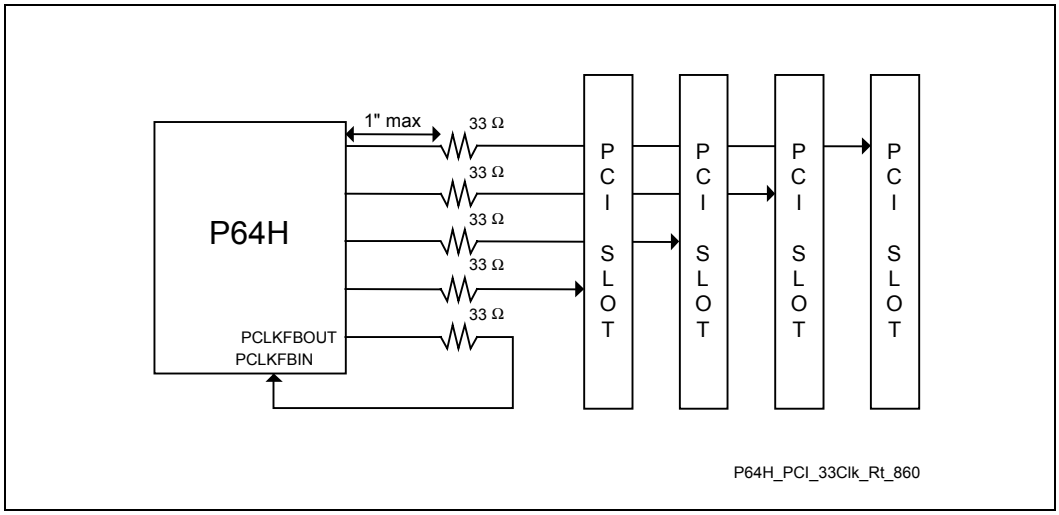
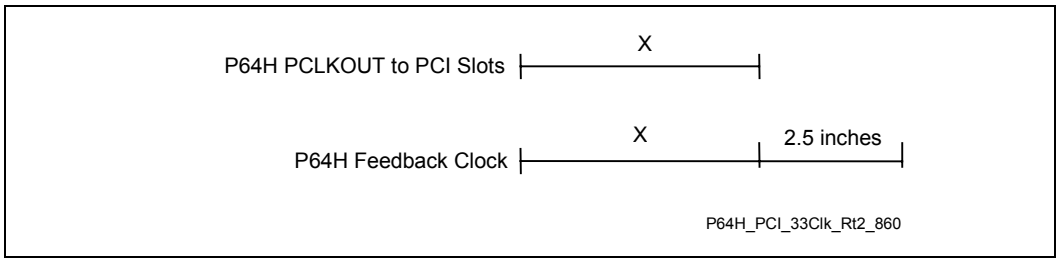


Figure 33. Intel® P64H PCI 33 MHz Clock Routing



As required by the PCI Specification, the PCI CLK signal length from the expansion board edge connector to the PCI device should be 2.5 inches ± 0.1 inches for 32-bit and 64-bit expansion boards.

4.3.4.2 Intel® P64H PCI 66 MHz Clock Routing Guidelines

At 66 MHz, the P64H can supports 2X66 MHz PCI slots and 1x66 MHz device down. The P64H can provide 3 copies of the PCLKOUT to PCI devices on its primary PCI bus. PCLKFBOUT is used as the feedback clock and must be routed into PCLKFBIN of the P64H. The PCLKOUT layout guidelines are shown in the following figures.

Figure 34. Intel® P64H PCI 66 MHz Clock Routing

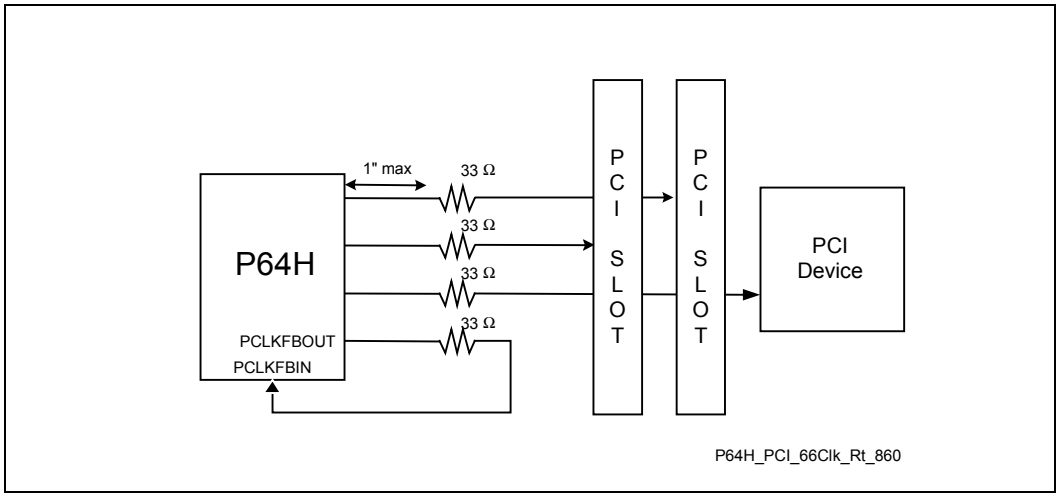
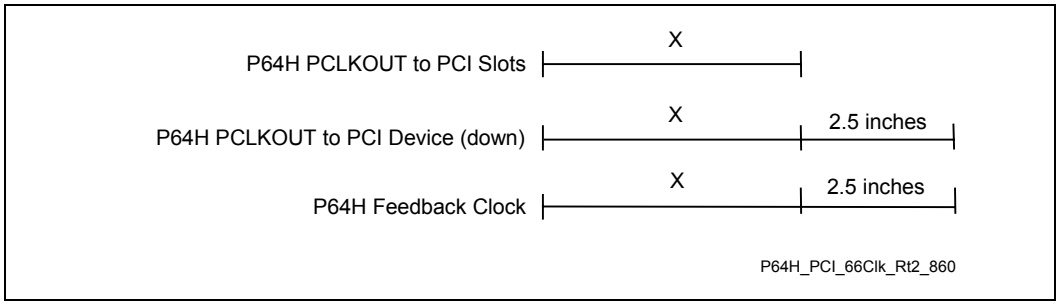


Figure 35. 66 MHz PCI Clock Routing



As required by the PCI Specification, the PCI CLK signal length from the expansion board edge connector to the PCI device should be 2.5 inches ± 0.1 inches for 32-bit and 64-bit expansion boards.

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5 System Bus Routing

Table 12 summarizes the layout recommendations for dual-processor based configurations. It should be used for quick reference only. The subsequent sections in this chapter provide more detailed information about various system configurations.

Table 12. System Bus Routing Summary

Parameter	Guidelines
Line to line spacing	• Greater than 3:1 edge-to-edge spacing vs. trace to reference plane height ratio.
Data line lengths (agent-to-agent spacing)	• 3.0 inches to 10.1 inches pin-to-pin. • Total bus length must not exceed 20.2 inches. • Data signals within a source synchronous strobe group should be routed within 25 mils of each other, pad to pad. • Length must be added to the motherboard trace between agents to compensate for the stub created by the processor package. See section 5.4.1 for details.
DSTBn/p[3:0]# line lengths	• DSTB# signals should follow the same routing rules at the data signals. In addition: • The lengths of each DSTBp# and DSTBn# pair should be routed within 25mils of each other, pad-to-pad, agent-to-agent and over the entire length of the bus. • A 25 mil spacing should be maintained around each strobe signal (between DSTBp# and DSTBn#, and any other signal).
Address line lengths	• Address signals should follow the same routing rules at the Data signals. • The lengths of Address signals within a group should be routed within 50 mils of each other, pad to pad.
ADSTB[1:0]# line lengths	• ADSTB# signals should follow the same routing rules at the DSTBn/p[3:0]# signals.
Common Clock signal line lengths	• Common Clock signals should follow the same routing rules as the Data signals, however no length compensation is necessary.
Topology	• Daisy chain with chipset at one end. The end processor must have on-die termination enabled. No stubs.
Routing priorities	• No motherboard contribution to stub length of middle processor (35 mil max trace via to pad). • Strobes and associated signals must be routed on same layer for entire length of bus.
Reference plane requirements	• Avoid changing layers when routing system bus signals. If a layer change must occur, use vias connecting the VCC_CPU planes and/or VSS planes to provide a low impedance path for the return current. Vias should be as close as possible to the signal via.
Serpentine spacing	• S/H greater than or equal to 5 (Figure 36). • Keep parallel sections as short as possible. • No 90° bends, use 45° bends whenever possible.
Motherboard Impedance	• 50 Ω ± 10%

5.1 Return Path

The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, or integrated circuits. The return path is based on electro-magnetic field effects. It is useful to think of the return path as the path of least impedance nearest the signal conductor. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths must be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, and then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance.

The following sets of return path rules apply to all designs:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near system bus signals.
- Do not make signal layer changes that force the return path to make a reference plane change, even if it is from one VSS layer to another VSS layer.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not route over via anti-pads or socket anti-pads

If reference plane changes must be made:

- Change from a VSS reference to a VSS reference and place a via that connects the two planes as close as possible to the signal via. This also applies when making a change from VCC_CPU to VCC_CPU.
- For symmetric stripline, return path vias for both VSS and VCC_CPU must be provided.
- Do not switch reference from VCC_CPU to VSS or vice versa.

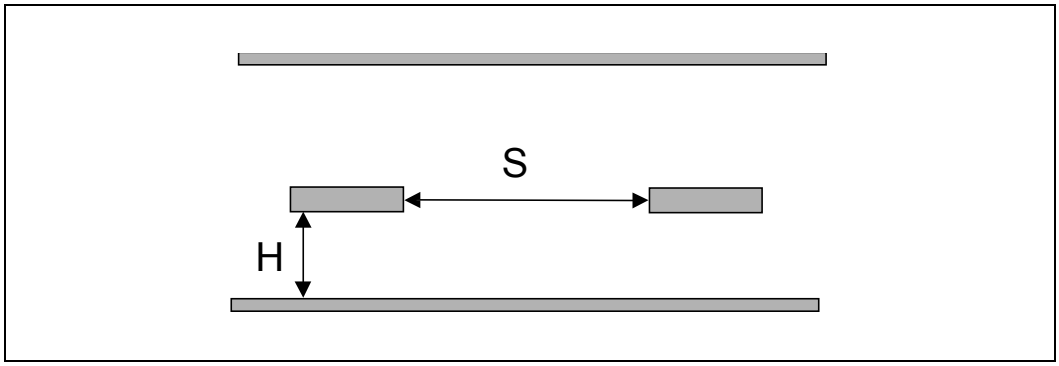
5.2 Serpentine Routing

A serpentine net is a transmission line that is routed in such a manner that sections of the net double back and couple to another segment of the same net. Serpentining a transmission line is sometimes necessary to properly match lengths between nets. It is important to properly control the serpentine to avoid signal integrity and timing problems. The primary impact of a serpentined trace is an observed decrease in the flight time when compared to a straight trace of equal length. This decrease in the flight time is a result of the crosstalk between parallel sections of the serpentined net. As the signal travels down the transmission line, a component of the signal follows the transmission line and behaves as though it were a straight line with no serpentine. However, another portion of the energy propagates perpendicular to the parallel routed portions of the serpentined net via the mutual capacitance and mutual inductance. This creates an extra mode that arrives at the receiver significantly earlier than the other component of the signal. If the coupling between parallel sections is high, significant timing skew can occur when attempting to match trace lengths on a bus. Furthermore, if the coupling is very high, significant signal integrity problems can result.

The serpentine guidelines included in this document were based on HSPICE* simulations with different spacing between parallel sections. The guidelines were chosen to significantly limit the effect of serpentining, while minimizing the impact to the application.

Serpentine spacing S/H should be greater than or equal to 5. The S/H ratio is shown in Figure 36.

Figure 36. Serpentine Spacing – Diagram of Spacing to Reference Plane Height Ratio



5.3 System Bus Decoupling Requirements

This section contains the motherboard decoupling recommendations to minimize return path discontinuities and provide necessary power delivery for the bus I/O buffers. These are decoupling requirements for the system bus I/O **only**. This decoupling is not adequate for power delivery. Refer to Section 12.16 for processor core power decoupling requirements.

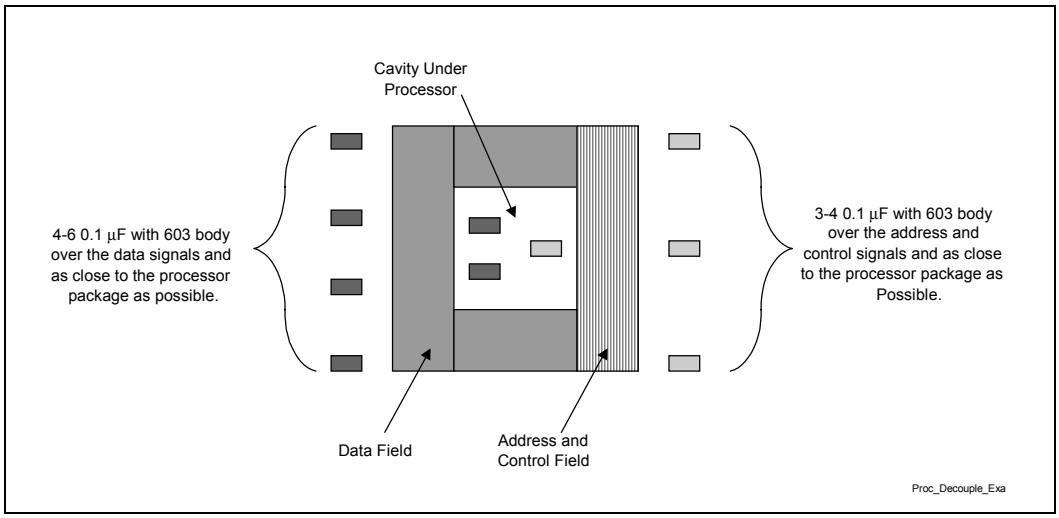
5.3.1 Processor I/O Decoupling Requirements

The primary objective of the processor decoupling guidelines is to minimize the impact of return path discontinuities. The processor power delivery guidelines for the help ensure that the I/O has adequate power decoupling. The worst-case return path discontinuity anticipated is for systems that use microstrip structures on the motherboard. The processor, from die to package pin, follows a symmetric stripline configuration with VCC_CPU as one reference plane, and VSS as the other reference plane. If the motherboard uses symmetric stripline with VCC_CPU and VSS references, then a discontinuity does not exist and additional decoupling is not necessary. If the motherboard routing references only a single reference plane (VCC_CPU **or** VSS), then a return path discontinuity exists between the processor and the motherboard, and I/O decoupling capacitors are required.

The following are decoupling recommendations for each processor (also refer to Figure 37):

- 4 minimum, 6 preferred 0.1 µF capacitors with 603 packages distributed evenly over the system bus data signals
- 3 minimum, 4 preferred 0.1 µF capacitors with 603 packages distributed evenly over the system bus address and Common Clock signals
- All capacitors placed as close to the processor package as keepout zones allow

Figure 37. I/O Decoupling Guidelines for the Processor



5.4 Dual Processor Configuration

This section provides more details for dual processor based systems. Both recommendations and considerations are presented.

For proper processor operation, it is necessary to meet the timing and voltage specifications of each component on the system bus. The most accurate way to understand the signal integrity and timing of the system bus on the platform is to perform a comprehensive simulation analysis. It is possible that adjustments to trace impedance, line length, termination impedance, board stack-up, and other parameters can be made that improve system performance. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation based on our reference platform. It is therefore strongly recommended that you perform a simulation analysis based on your platform

The following table lists all signals that interface with the processor. This table is a copy of the table from the processor datasheets referenced in Section 1.1. In the event that this layout conflicts with the datasheet, the datasheet data supercedes this data.

Table 13. System Bus Signals

Signal Group	Type	Signals
AGTL+ Common Clock Input	Synchronous to BCLK	BPRII#, BR[3:1]#[1,2], DEFER#, RESET#[1], RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK	ADS#, AP[1:0]#, BINIT#[3], BNR#[3], BPM[5:0]#[1], BR0#, DBSY#, DP[3:0]#, DRDY#, HIT#[3], HITM#[3], LOCK#, MCERR#[3]
AGTL+ Source Synchronous I/O: 4X Group	Synchronous to assoc. strobe	D[63:0]#, DBI[3:0]#
AGTL+ Source Synchronous I/O: 2X Group	Synchronous to assoc. strobe	A[35:3]#[4], REQ[4:0]#
AGTL+ Strobes	Synchronous to BCLK	ADSTB[1:0]#, DSTBN[3:0]#, DSTBP[3:0]#
Async GTL+ Input1	Asynchronous	A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK#
Async GTL+ Output1	Asynchronous	FERR#, IERR#, THERMTRIP#, PROCHOT#
System Bus Clock	Clock	BCLK0, BCLK1
TAP Input1	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output1	Synchronous to TCK	TDO
SMBus Interface1	Synchronous to SM_CLK	SM_EP_A[2:0], SM_TS_A[1:0], SM_DAT, SM_CLK, SM_ALERT#, SM_WP
Power/Other		BSEL[1:0] [5], GTLREF[3:0], COMP[1:0], OTDEN, RESERVED, SKTOCC#, TESTHI[6:0], VID[4:0], VCC_CPU, SM_VCC, VCCA, VSSA, VCCIOPLL, VSS, VCCSENSE, VSSSENSE

NOTES:

1. These signals do not have on-die termination on the processor. They must be terminated properly on the motherboard.
2. The Intel Xeon processor and Intel Xeon processor with 512 KB L2 cache only use BR0# and BR1#. BR2# and BR3# operation is not supported on these processors and these pins must be terminated to VCC_CPU. Refer to the routing guidelines in Section 5.4.2.5.
3. These signals are “wired-OR” signals and may be driven simultaneously by multiple agents. For further details on how to implement wired-OR signals, refer to the routing guidelines in Section 5.4.1.4.
4. The value of these pins during the active to inactive edge of RESET# determine processor configuration options .
5. Bus Select (BSEL)[1:0] are processor output signals that indicate the system bus frequency supported by the processor. Since this platform is only designed to operate with a 100 MHz system bus clock, use these output signals is not required. Refer to the *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.8 GHz, 2 GHz and 2.2 GHz Datasheet* for more details about BSEL[1:0] operation.

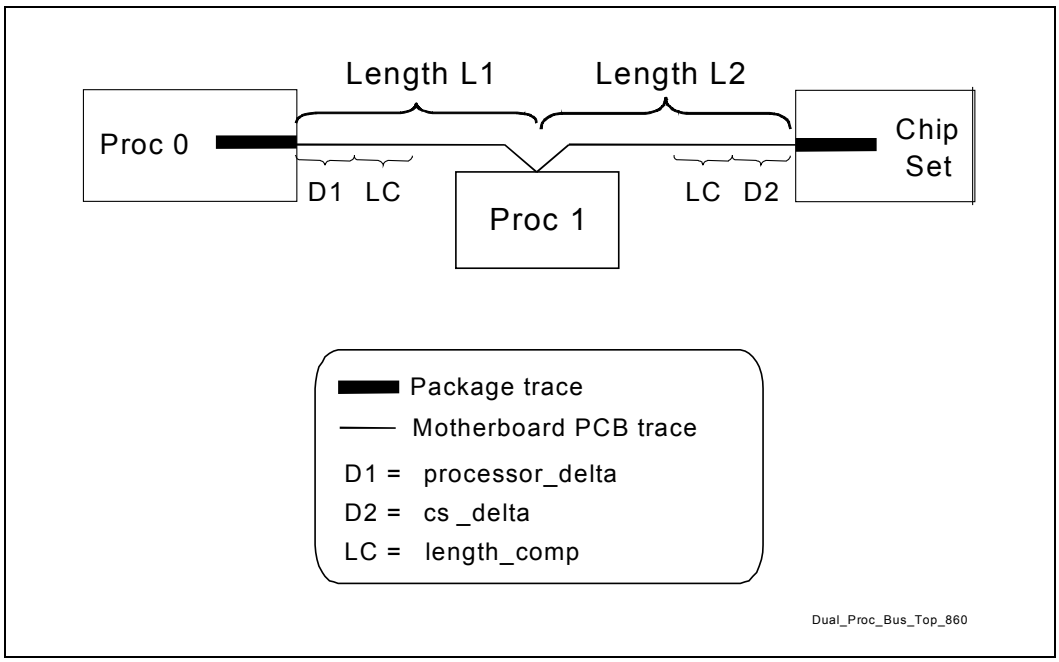
5.4.1 Routing Guidelines for Source Synchronous Signals

Design recommendations are presented first, followed by design considerations. The layout guidelines given in this section are based on specific chipset (I/O buffer, package, and loading) and motherboard properties. Complete simulation and hardware validation is necessary to ensure a robust design.

Design Recommendations

The dual processor topology requires that the chipset be at one end of the bus, and that no motherboard contribution to the stub length of the processor exists in the middle of the bus. A diagram of the dual processor daisy chain topology is shown in Figure 38.

Figure 38. Dual Processor System Bus Topology

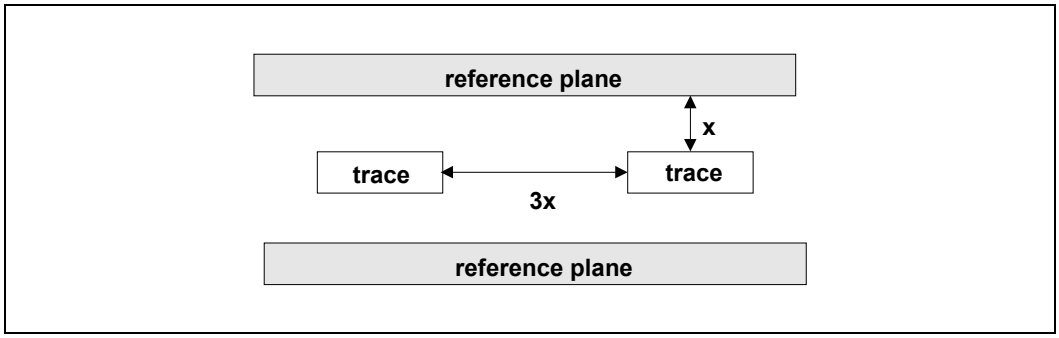


The motherboard trace impedance should be 50 Ω ± 10%. The traces should maintain a greater than three to one edge-to-edge spacing versus trace to reference plane height ratio (see Figure 39). As the traces pass through the pin fields of the 603-pin socket and the chipset, the 3:1 requirement may not be achievable. In these areas where the 3:1 ratio is not possible, the separation should be maximized and the distance of the violation should be minimized. Specifically, when routing through the 603-pin socket, expand to a 3:1 ratio whenever possible. Do not keep a tighter spacing ratio the entire length of the socket. However, do not route through the VCC_CPU and V_{SS} pin field because this also has a great potential for noise coupling. A trace spacing-to-height above reference plane ratio of 3 to 1 ensures a low crosstalk coefficient. All the effects of crosstalk are difficult and tedious to simulate. Intel has performed extensive simulation and experimentation on the effects of crosstalk to more accurately predict these effects. The timing and layout guidelines for the processor have been created with the assumption of a 3:1 trace spacing to height above reference plane ratio. A smaller ratio would have a negative impact on both timing and noise margins because of crosstalk.

In a dual processor configuration where the stack-up has two signal layers as the middle layers, the signals in the middle layers should be routed orthogonal to each other. If routing the signals in an orthogonal manner is not possible, then maximize the distance of separation between these two layers and route the signals such that they are not routed directly above each other. This configuration (signal layers with no reference plane separating them) provides the greatest coupling co-efficient, and thus a higher potential for detrimental crosstalk.

For partially populated systems, the end processor must be populated first. The end processor is that furthest from the chipset. This effectively leaves only the socket as a stub on the bus for the unpopulated agents.

Figure 39. Cross Sectional View of 3:1 Ratio for Stripline (Edge-to-Edge Trace Spacing vs. Trace to Reference Plane Height)



It is critical that additional stub length not be added on the motherboard to the middle processor.

Source synchronous groups and associated strobes should be routed on the same layer for the entire length of the bus. This results in a significant reduction of the flight time skew since the FR4 thickness, trace width, and velocity of the signals will be uniform across a single layer of the stack-up. There is no guarantee of a relationship of FR4 thickness, trace width, and velocity between two layers.

Additionally, changing layers may create a return path discontinuity that often leads to unpredictable delay push-outs or pull-ins and signal quality problems. Specifically, if via densities are large and most of the signals switch at the same time, the layer to layer bypass fails to provide an acceptably short signal return path to maintain timing and noise margins. Experience at Intel indicates that the magnitude of the uncertainty that occurs with shifting return paths is on the same order as the data bus cycle time. If layer changes must be made, it is best to change to a routing layer that references the same VCC_CPU or VSS plane.

To avoid return path discontinuities, traces must be routed with at least 50% of the trace width directly over a reference plane. This is particularly important when routing next to vias in the socket pin field.

Table 14. Source Synchronous Signals and the Associated Strobes

Signals	Associated Strobe
REQ[4:0]#, A[16:3]#	ADSTB0#
A[35:17]#	ADSTB1#
D[15:0]#, DBI0#	DDSTBP0##, DSTBN0#
D[31:16]#, DBI1#	DSTBP1#, DSTBN1#
D[47:32]#, DBI2#	DSTBP2#, DSTBN2#
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#

5.4.1.1 4X Group (DSTBN[3:0]#, DSTBP[3:0]#, D[63:0]#, DBI[3:0]#):

The distance from the pin of one agent to the pin of the next must be between 3.0 inches and 10.1 inches. Figure 38 illustrates the dual processor daisy chain topology with the chipset at the end. Total bus length must not exceed 20.2 inches.

5.4.1.1.1 Trace Length Balancing

Length must be added between each agent to compensate for package length differences that exist within a source synchronous data group. This length compensation results in minimizing the source synchronous skew that exists on the system bus. Without the length compensation, the flight times between a data signal and its strobe is different, which results in an inequity between the setup and hold times. Since the strobe typically has a shorter package length, there is favoritism toward hold time, and the setup requirement may not be met without length compensation on the motherboard. Note this will not make the pad-to-pad lengths between all agents equal in length, but it will balance the strobe-to-signal skew in the middle of the setup-and-hold window between all driver-receiver combinations.

Compensating for the processor package lengths on the motherboard is necessary. The amount that should be added can be calculated using Equation 1. This length should be added to motherboard trace segment L1.

Equation 1. Processor Package Compensation Length

$$D1 = cpu\_delta_{net,group} = \max\_cpu\_pkglen_{group} - cpu\_pkglen_{net}$$

Compensating for the chipset package lengths on the motherboard is also necessary. The amount that should be added can be calculated using Equation 2. This length should be added to motherboard trace segment L2.

Equation 2. Chipset Package Compensation Length

$$D2 = cs\_delta_{net,group} = \max\_cs\_pkglen_{group} - cs\_pkglen_{net}$$

A length of 0.78 times the processor package compensation length (D1) should be added between each agent. See Equation 3. The length should be added to motherboard trace segment lengths L1 and L2.

Equation 3. Additional Compensation Length for DP Systems

$$LC = length\_comp_{net,group} = 0.78 * (\max\_cpu\_pkglen_{group} - cpu\_pkglen_{net})$$

The routed motherboard lengths within a source synchronous group should match the results of the previous equations to ± 25 mils between agent-to-agent, and ± 50 mils over the entire length of the bus. This skew should be simulated to determine the length that best centers the strobe for a given system.

Example Using Hypothetical Numbers

Consider 2 signals, DSTBP0# and D1#, from the same group. Assume that L1 (motherboard trace from CPU1 to CPU2) for DSTBP0# and D1# is 4 inches. Similarly, assume that the package trace for DSTBP0# is 0.15 inches (cpu_pkglen) and D1# is 0.35 inch (max_cpu_pkglen). Using Equation 1, the delta will be 0.20 inches (0.35 – 0.15). Using Equation 3, length_comp for D0 is 0.156 inches 0.78*(0.20). The length-matching spreadsheet therefore requires that additional length of 0.356 inches (0.20 + 0.156) be added to signal DSTBP0#. Hence, the new length for DSTBP0# will be 4.356 inches (instead of the current 4 inches). The length matching spreadsheet requires the new length of DSTBP0# to be within ± 0.025 inches (25 mils) of 4.356 inches.

L2 requires delta from Equations 2 and 3 to determine the new length. Again, the spreadsheet requires that the new length for L2 be met within ± 0.025 inches (25 mils).

Refer to the processor signal integrity models and the length matching spreadsheet tool (referenced in Section 1.1) for the package line lengths and for assistance in matching the motherboard trace lengths.

This compensation makes up for the flight time difference caused by the difference in package lengths and counteracts the capacitive loading effects caused by stubs on the bus. The stub lengths of the processor package act as capacitive loads and thus degrade the edge rate as a signal travels from one agent to an agent that is not its nearest neighbor. The greatest degradation is seen when a signal propagates from one end agent to the other end agent. Because all stub lengths are not the same, different signals see varying degrees of degradation. The signals with longer stubs see more degradation than those with shorter stubs. For source synchronous signals, the goal is to reduce skew between a signal and its strobe. Since strobe signals typically have short package lengths, they do not see much edge rate degradation. However, since other signals can have stub lengths of up to 600 mils, their edge rate degradation can be dramatic, at least relative to that of the strobe. These large differences in the slope of the edges at the receiver can result in a very large skew between the data and the strobe. This could result in a bus error because the setup and hold times may not be met. To compensate for this edge rate degradation, length is added (between each

agent on the motherboard) to the signals that have shorter stub lengths in an attempt to achieve similar flight times for the data and its strobe at the receiver. Adding the length helps achieve a similar behavior of the signal along the length of the bus.

The 4X group signals of the same source synchronous group should be routed within 25 mils of the same length between each agent, and within 50mils of the same length over the entire distance of the bus. It is recommended that skew be simulated to determine the length that best centers the strobe for a given system. It is not necessary to match lengths of one 4X signal group to the signals other 4X groups. It is necessary that every signal meet its setup and hold timing requirements.

A strobe and its complement (DSTBN# & DSTBP#) should be routed within 25 mils of the same length. Keep all traces at least 25 mils away from the strobes. It is also advisable to keep 4X signals away from other signals, particularly the asynchronous signals.

5.4.1.2 2X Group (ADSTB[1:0]#, A[35:3]#, REQ[4:0]#)

The requirements for the 2X group signals are the same as for the 4X group signals.

5.4.1.3 Common Clock

Common Clock signals should follow the same routing rules at the 4X Group signals. However, no length compensation is necessary.

The distance from the package pin of one agent to the package pin of the next agent should be between 3.0 inches and 10.1 inches. Figure 38 illustrates the dual processor daisy chain topology with the chipset at the end. Total bus length must not exceed 20.2 inches. Simulation of these signals is strongly recommended to ensure that they meet the setup and hold times with respect to BCLK[1:0].

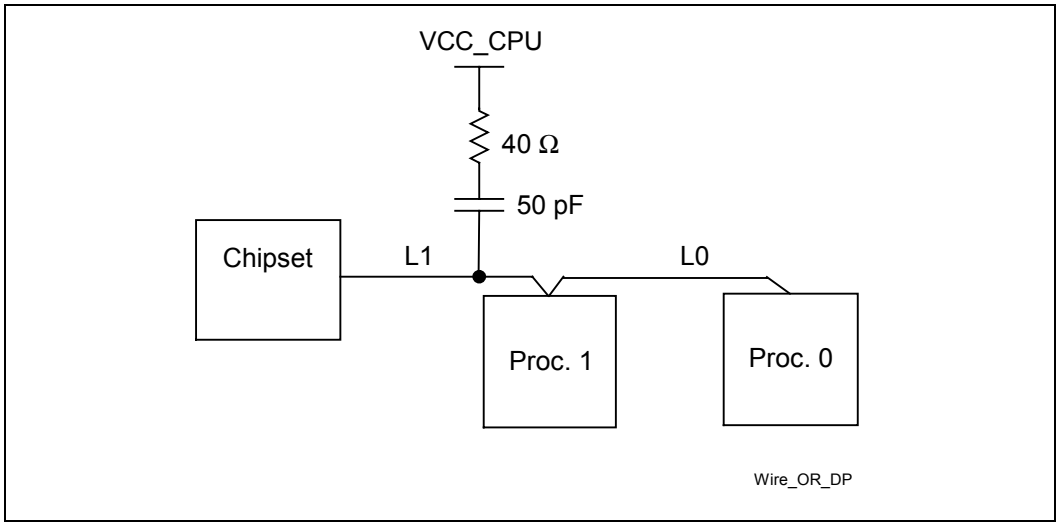
5.4.1.4 Wired-OR Signals (BINIT#, BNR#, HIT#, HITM#, MCERR#)

There are five “wired-OR” signals on the system bus. These signals are HIT#, HITM#, MCERR#, BINIT#, and BNR#. These signals differ from the other front-side bus signals in that more than one agent can drive the signal at one time. Therefore, timing and signal integrity must be met when one agent is driving, all agents are driving, and any combination of agents is driving. Specialized routing guidelines are therefore required to meet signal integrity and timing requirements.

The wired-OR signals should follow the same routing rules as the common clock signals except for the items specified in the following text. It is highly recommended that simulations for these signals be performed for each system.

The wired-OR signals BNR#, HIT#, and HITM# should have AC termination to VCC_CPU at the middle agents (see Figure 40). The termination should be located as close as possible to the processor pins (< 1 inch) with no stubs. A 40.2 Ω resistor and 47 pF capacitor should be used for the AC termination. The nominal impedance of the wired-OR signal traces should be 25Ω ± 10%. The L1 and L0 lengths between agents should be 3.0 inches to 6.2 inches. **Wired-OR signals BINIT# and MCERR# do not require any termination as only the processors are capable of driving these signals.** The resulting signal integrity is sufficient without AC termination for BINIT# and MCERR# signals.

Figure 40. Wired OR Topology for Dual Processor Based Systems



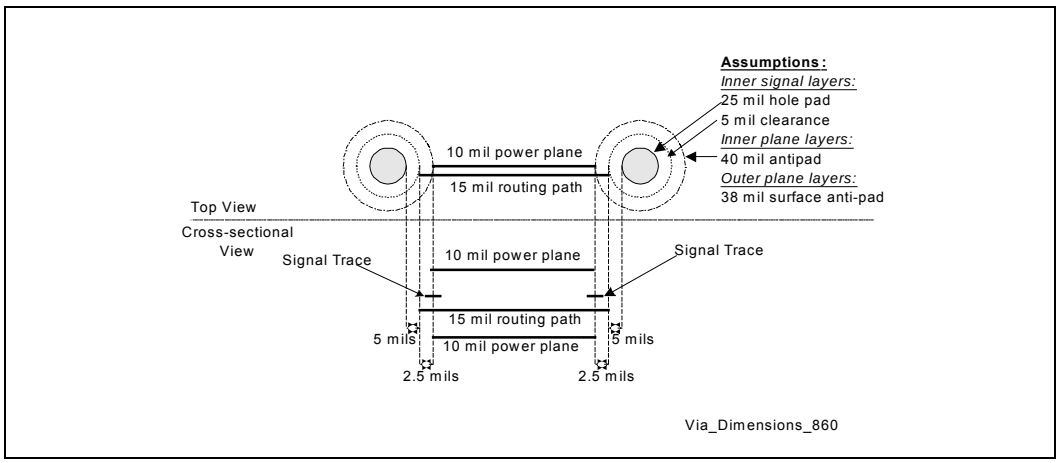
Design Considerations

Intel has found that the following recommendations aid in the routing of a processor platform. This is a baseline configuration only. Modify this baseline as needed while adhering to the preceding design recommendations.

- Trace width = 5.0 mil
- Trace to trace spacing = 15 mil (except in component breakout where spacing is constrained)
- 10 mil vias with a 35 mil pad
- ½ oz copper on signal layers, 1 oz on planes for power delivery

Using the recommendations for via size shown in Figure 41 allows two traces to be routed between vias, and the traces to overlap the reference plane by no more than 50%. The overlap should occur only for a short distance.

Figure 41. Via Dimensions and Routing Path



5.4.2 Routing Guidelines for Asynchronous GTL+ and Other System Bus Signals

This section describes layout recommendations for signals not covered in the previous section. Table 15 describes the signals covered in this section.

Table 15. Asynchronous GTL+ and Miscellaneous Signals

Signal Name	Type	Processor I/O Type	Topology Number	Driven by	Received by
A20M#	Async GTL+	I	2	ICH2	Processor
BINIT#	AGTL+	I/O	Refer to Section 5.4.1.4	Processor	Processor
BR[3:1]#	AGTL+	I	5	Processor	Processor
BR0#	AGTL+	I/O	5	Processor/ MCH	Processor/ MCH
COMP[1:0]	Analog	I	6	Pull-down	Processor
FERR#	Async GTL+	O	1	Processor	ICH2
IERR#	Async GTL+	O	1	Processor	External logic
IGNNE#	Async GTL+	I	2	ICH2	Processor
INIT#	Async GTL+	I	2	ICH2	Processor
LINT[1:0]	Async GTL+	I	2	ICH2	Processor
ODTEN	other	I	7	Pull-up / pull-down	Processor
PROCHOT#	Async GTL+	O	1	Processor	External logic
PWRGOOD	Async GTL+	I	2	External logic	Processor
RESET#	Common Clock	I	See note 2	MCH	Processor
SLP#	Async GTL+	I	2	ICH2	Processor
SM_ALERT#	SMBUS (3.3 V)	I/O	4	Processor/ ICH2	ICH2
SM_CLK	SMBUS (3.3 V)	I	4	Processor/ ICH2	Processor/ ICH2
SM_DAT	SMBUS (3.3 V)	I	4	Processor/ ICH2	Processor/ ICH2
SM_EP_A[2:0]	SMBUS (3.3 V)	I	4	Pull-up / pull-down	Processor
SM_TS_A[1:0]	SMBUS (3.3 V)	I	4	Pull-up / pull-down	Processor
SM_WP	SMBUS (3.3 V)	I	4	Pull-up / pull-down or external logic	Processor

Signal Name	Type	Processor I/O Type	Topology Number	Driven by	Received by
SMI#	Async GTL+	I	2	ICH2	Processor
STPCLK#	Async GTL+	I	2	ICH2	Processor
TAP signals	TAP		See Section 16		
THERMTRIP#	Async GTL+	O	Refer to Section 5.4.2.1	Processor	External logic
VCCA	Power	I	See Section 12.17.3		
VCCIOPLL	Power	I	See Section 12.17.3		
VCCSENSE	Other	O	See Section 12.12		
VID[4:0]	Other	O	3	Processor	Voltage regulator
GTLREF	Power	I	See Section 12.17.2		
VSSA	Power	I	See Section 12.17.3		
VSSSENSE	Other	O	See Section 12.12		

NOTES:
1. All signals must meet the AC and DC specifications listed in the Intel® Xeon™ Processor at 1.40 GHz, 1.50 GHz, 1.7 GHz and 2 GHz Datasheet.
2. The Reset# signal should be terminated to the processor VCC_CPU voltage on both ends of the transmission line similar to the system bus. The Intel Xeon processor and Intel Xeon processor with 512 KB L2 cache do not provide on-die termination for the Reset# signal and hence the platform must provide the termination. Refer to the ITP700 Debug Port Design Guide for implementation details affecting the debug port design.

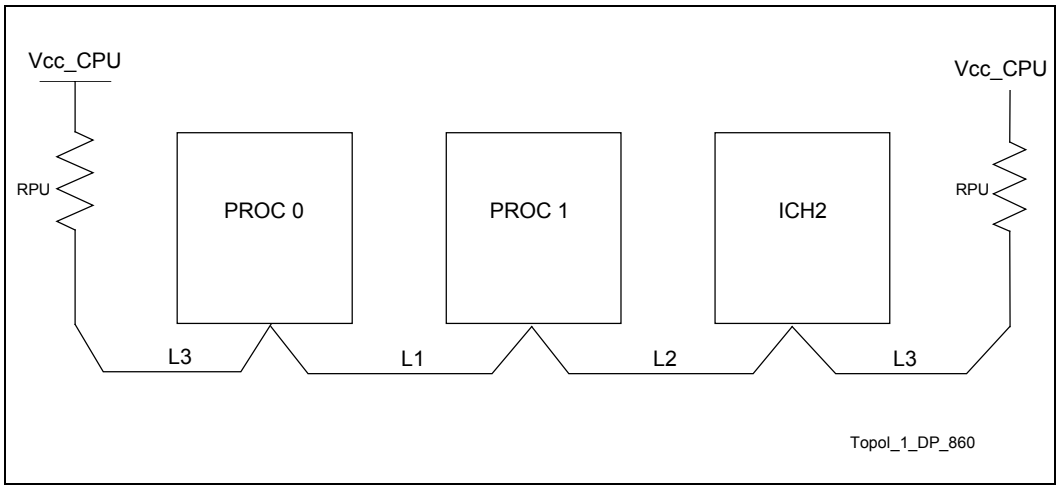
5.4.2.1 Topology 1: Asynchronous GTL+ Signals Driven by the Processor

These signals (FERR#, PROCHOT#, THERMTRIP#, and IERR#) should adhere to the following routing and layout recommendations. Figure 42 illustrates the recommended topology. When routing to middle agents connect in true daisy chain topology. Do not create a stub to connect to the socket pins. Note that FERR# is the only signal in this group that connects between the processor(s) and the ICH2. PROCHOT#, THERMTRIP# and IERR# are connected to other motherboard logic.

Because of excessive undershoot observed at the processors, use dual termination on all four signals for dual processor configurations. Each processor's signal can be routed to it's own receiver, or the signals can be wire-OR'd together. Each signal must be terminated if routed separately, but the signal can be terminated at the receiver end only. Figure 42 shows the recommended topology.

Trace Zo	Trace Spacing	L1	L2	L3	Rpu
50 Ω	10 mil	4–6 inches	1–12 inches	3 inches max	56 Ω ± 5%

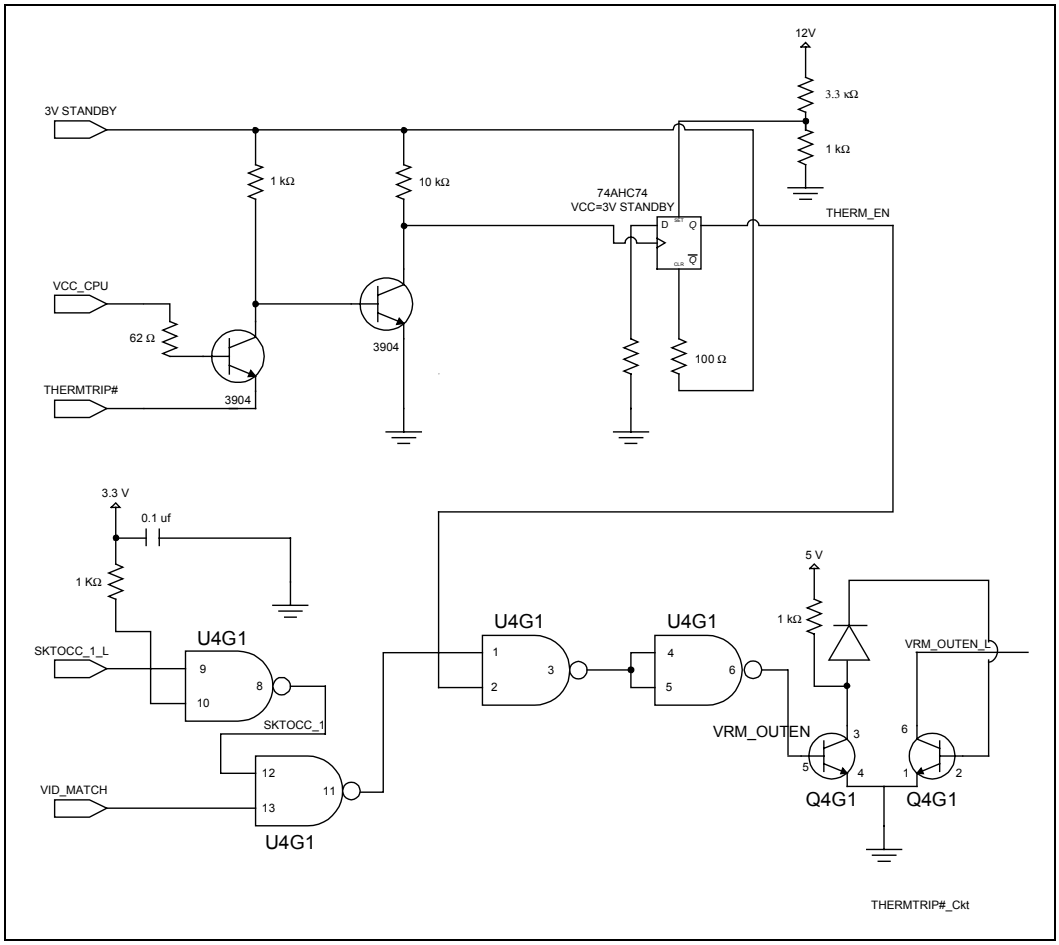
Figure 42. Topology 1 for DP Configuration



To help protect the processor from damage in over-temperature situations, motherboard logic must ensure that power to the processor core is removed within 0.5 seconds of the assertion of THERMTRIP#. If power is applied to a processor when no thermal solution is attached, normal leakage currents will cause the die temperature to rapidly rise to levels at which permanent silicon damage is possible. This high temperature will cause THERMTRIP# to go active. For details regarding the THERMTRIP# specification, refer to the processor datasheets referenced in Section 1.1.

Each processor's THERMTRIP# signal can be routed to its own receiver, or they can be wire-OR'd together. If routed separately, each signal should be terminated at the receiver end only instead of using dual termination. Because this platform utilizes a shared VCC_CPU power plane, all power supply sources to all processors must be disabled when any installed processor asserts THERMTRIP#. Figure 43 shows a recommended circuit for disabling power to the processor, along with related customer reference board logic that interfaces with this THERMTRIP# shutdown circuit. The 74AHC74 flip-flop latches the THERMTRIP# signal HIGH after a PWRGOOD assertion, and LOW after a THERMTRIP# assertion. The output of this latch is then used by the system logic that controls the enable and disable of the processors' VRD supply. Refer to the Customer Reference Board Schematics in Appendix A for complete details.

Figure 43. Recommended THERMTRIP# Circuit



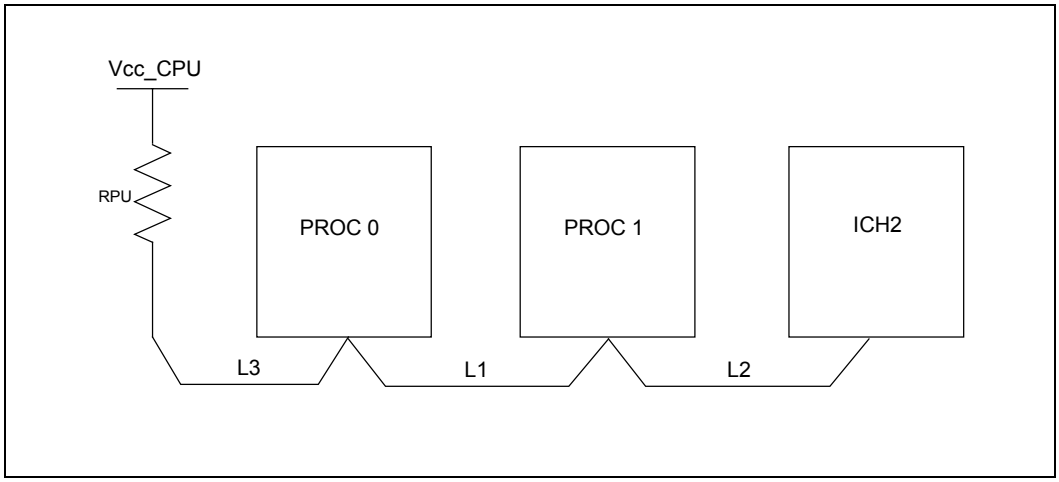
5.4.2.2 Topology 2: Asynchronous GTL+ Signals Driven by the Chipset

These signals (A20M#, IGNNE#, INIT#, LINT[1:0], PWRGOOD, SLP#, SMI#, and STPCLK#) should adhere to the following routing and layout recommendations. Figure 44 illustrates the recommended topology. When routing to middle agents, connect in true daisy chain topology. Do not create a stub to connect to the socket pins.

It may be desirable to isolate PWRGOOD for each voltage regulation module (VRM) and processor pair to allow recognition of individual VRM failures.

Trace Zo	Trace Spacing	L1	L2	L3	Rpu
50 Ω	10 mil	4–6 inches	1–12 inches	3 inches max	300 Ω ± 5%

Figure 44. Topology 2 for DP Configuration



5.4.2.3 Topology 3: VID[4:0]

The processor VID[4:0] signals should be routed to the voltage regulator. The voltage regulator controller should provide internal pull-up resistors for these signals. Refer to voltage regulator design guidelines referenced in Section 1.1 and the specification of the voltage controller specific to your design for further details.

Because all installed processors must operate at the same voltage (the power plane is shared between both CPUs), it is advisable to provide a way to check the VID[4:0] values from both processors are the same, otherwise power should not be output enabled from the VRMs.

5.4.2.4 Topology 4: SMBus Signals

The SMBus signals provide access to the manageability features on the Intel Xeon processor and Intel Xeon processor with 512 KB L2 cache. The signaling protocol adheres to the specification of the System Management Bus. Refer to the processor datasheet for details on the processor implementation and addressing scheme.

The SM_ALERT#, SM_CLK, and SM_DAT signals should be connected to an SMBus controller in adherence to the *System Management Bus Specification, rev2.0*. These signals can be connected to other processors on the same SMBus. Refer to the *SMBus and I^2C Bus Design* application note for additional design information.

The SM_EP_A[2:0] signals set the SMBus address for the memory device on the processor. These signals must be set at power on with a unique address per bus. They have an internal 10 kΩ pull-down. To pull a signal to a logic high level, connect it to a 100 Ω resistor tied to SM_VCC.

The SM_TS_A[1:0] signals set the SMBus address for the thermal device on the processor. These signals must be set at power on with a unique address per bus. The SM_TS_A[1:0] can be set to a logic high, a logic low, or a high impedance state giving nine possible combinations of addresses. The SM_TS_A[1:0] signals do not have internal pull-downs and must therefore be pulled to VSS or SM_VCC with a 1 kΩ or smaller resistor. Leaving the pins floating achieves a high-Z state.

The SM_WP signal is a write protect signal for the memory device. Pulling this signal to SM_VCC enables write protection. SM_WP has an internal 10 kΩ pull-down.

5.4.2.4.1 Considerations for Implementing Manageability Features of the Processor

The Intel Xeon processor and Intel Xeon processor with 512 KB L2 cache include three features that provide manageability needs beyond the processor core, an on-board thermal sensor, a Processor Information ROM (PIROM), and an OEM Scratch ROM. These features are accessible via the System Management Bus (SMBus) interface pins provided by the processor. The SMBus thermal sensor can be utilized to analyze long-term temperature trends of the processor. The PIROM contains 128 bytes of information regarding the features and configuration of the processor. The OEM Scratch ROM provides 128 bytes of space for data to be supplied by the OEM. Together, these features can be utilized to enhance system manageability, such as implementing portions of *the Intelligent Platform Management Interface (IPMI) Specification*.

General Design Considerations

Utilizing the SMBus devices of the processor is not required. While the Intel Xeon processor utilizes SM_VCC only for the SMBus devices, the Intel Xeon processor with 512 KB L2 cache requires a valid 3.3V source to SM_VCC because the VID[4:0] pins are driven by logic that is powered by the SM_VCC supply. Therefore, the SM_VCC supply must be valid before the VRM supplying VCC_CPU to the processor is enabled. Refer to the *Intel® Xeon™ Processor with 512 KB L2 Cache Compatibility Guidelines for Intel® Xeon™ Processor-Based Platforms* and *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.8 GHz, 2 GHz and 2.2 GHz Datasheet* for implementation details regarding VID and SM_VCC. When configuring the address space of the SMBus devices, Intel recommends using 1 kΩ pull-up or pull-down resistors.

SMBus Thermal Sensor Design Considerations

The SMBus thermal sensor is configured for its SMBus address space through the processor input signals SM_TS_A[1:0]. The thermal sensor supports nine unique addresses. This is accomplished by using three states of decode of the address pins: high, low, and high-Z. With no motherboard supplied pull up or pull down resistors, the address pins are configured for the high-Z state for address space determination.

For systems with more than nine thermal sensors utilizing the same address space that exceeds nine devices, the SMBus will need segmentation to avoid address conflicts. In addition, there may be cases where segmentation is required due to power availability in various zones of the design. For example, if some portions of the system can be powered off, it may not be necessary/desired to monitor thermal activity in that zone and thus power can be removed from the sensors as well. Segmentation of the SMBus would be necessary so that powered and unpowered devices do not occupy the same segment.

PIROM and OEM Scratch ROM Design Considerations

The PIROM and OEM Scratch ROM are both contained in the same EEPROM device, and as such are configured for their address space through a common set of address pins. Processor input signals SM_EP_A[2:0] configure the address space on the SMBus. Each of these inputs includes a 10 kΩ pull down on the processor interposer. There are eight address options for the ROMs and these addresses are the same as those found in memory Serial Presence Detect (SPD) devices. Thus, when implementing the PIROM and Scratch ROM, segmentation of the Smbus is necessary if there are more than eight SPD and PIROM/Scratch ROM devices in the system.

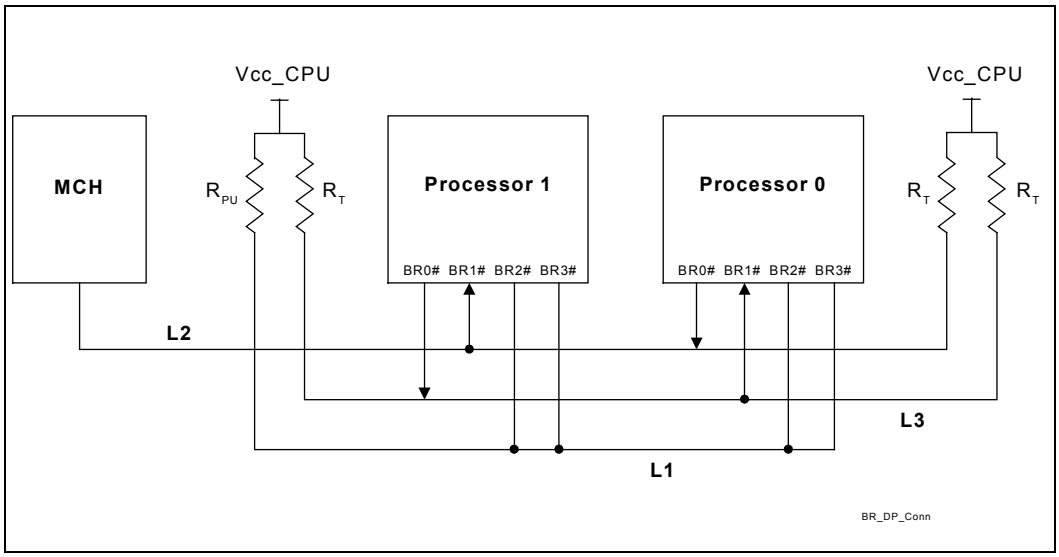
The PIROM is always write protected. The OEM Scratch ROM space is write protected via the SM_WP input signal. The processor provides a 10 kΩ pull down resistor on this signal. The platform may drive this signal with logic or use a pull up of 1 kΩ to enable the write protection of the Scratch ROM. As with the other SMBus signals, the SM_WP input is 3.3 V compatible.

5.4.2.5 Topology 5: BR[3:0]# Signals

Because the processor does not include on-die termination for the BR[3:0]# signals, it is necessary to terminate the signals using discrete components on the motherboard. Connect the BR[1:0]# signals, as in the past, by "swizzling" the lines between the processors as shown in Figure 45. Agent-to-agent signal length for the processors should be 4.5 inches. The total bus length can be no longer than 20.2 inches. Agent-to-agent lengths on BR[1:0]# should be matched within 0.5 inches. For other routing guidelines such as trace spacing and layer referencing, follow the guidelines for common clock signals in Figure 45. Either terminate BR[3:2]# individually at each processor, or connect the signals between processors and terminate at one end. Terminate to VCC_CPU.

Trace Zo	L1 Agent-to-agent	L2 (BR0#) Agent to Chipset	L3 Agent to Rpu stub	R_T	R_{PU}
50 Ω	3.0 to 10.1 inches	Up to 15.7 inches	Up to 1 inch	41Ω ± 5%	41 Ω ± 5%

Figure 45. BR[3:0]# Connection for DP Configuration



5.4.2.6 Topology 6: COMP[1:0] Signals

Terminate the COMP[1:0] pins to ground through a 43.2 Ω ± 1% resistor. Do not wire the COMP pins together—connect each pin to its own termination resistor.

5.4.2.7 Topology 7: ODTEN Signal

The end processor in a dual-processor system must have its on-die termination enabled. The middle agent must disable the on-die termination. To enable, pull the ODTEN pin to a high state by terminating it to VCC_CPU through a resistor. To disable, pull the ODTEN pin to a low state by terminating it to ground through a resistor. There are two options for choosing the pull-up and pull-down resistor values. While both options are suitable for this platform, Option 1 is preferred over Option 2. The two available options are:

- Option 1 (preferred): Enable ODT (on-die termination) on Processor 0 (end processor) by pulling up to VCC_CPU with a resistor that matches the motherboard trace impedance within ± 20%. Disable ODT on Processor 1 by pulling down to VSS with a resistor that matches the motherboard trace impedance within ± 20%. For example, since the recommended nominal trace impedance is 50 Ω, resistor values within the range of 50 Ω ± 20% should be used for the pull-up and pull-down.
- Option 2: Enable ODT on Processor 0 (end processor) by pulling up to VCC_CPU with a 1 kΩ resistor. Disable ODT on Processor 1 by pulling down to VSS with a 1 kΩ resistor.

5.4.2.8 Topology 8: TESTHI[6:0] Signals

For each processor, all TESTHI[6:0] pins must be connected to VCC_CPU via pull-up resistors. TESTHI[3:0] and TESTHI[6:5] may all be tied together at each processor and pulled up to VCC_CPU with a single resistor, if desired. However, boundary scan testing will not be functional if any TESTHI pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins regardless of the usage of boundary scan. The TESTHI[6:0] signal group must not be connected between processors. There are four options for choosing the pull-up and pull-down resistor values. While four options are suitable for this platform, Intel recommends new designs or designs undergoing design updates follow the trace impedance matching termination guidelines given in Option 1a or Option 2a. The four available options are:

- Option 1a (preferred): All TESTHI[6:0] pins may be individually pulled-up to VCC_CPU with resistors. For optimum noise margin, the pull-up resistor value should have a resistance value within ± 20% of the impedance of the board transmission line traces. Since the recommended nominal trace impedance is 50 Ω, use resistors that fall within the range of 50 Ω ± 20%.
- Option 1b: All TESTHI[6:0] pins may be individually pulled-up to VCC_CPU with 1 kΩ ± 5% resistors.
- Option 2a (preferred): TESTHI[3:0] and TESTHI[6:5] may all be tied together and pulled up to VCC_CPU with a single resistor. For optimum noise margin, the pull-up resistor value should have a resistance value within ± 20% of the impedance of the board transmission line traces. Since the recommended nominal trace impedance is 50 Ω, use resistors that fall within the range of 50 Ω ± 20%. However, utilization of boundary scan test will not be functional if these pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins.
- Options 2b: TESTHI[3:0] and TESTHI[6:5] may all be tied together and pulled up to VCC_CPU with a single 1 kΩ – 4.7 kΩ resistor if desired. However, utilization of boundary scan test will not be functional if these pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins.

5.4.2.9 Topology 9: SKTOCC# Signal

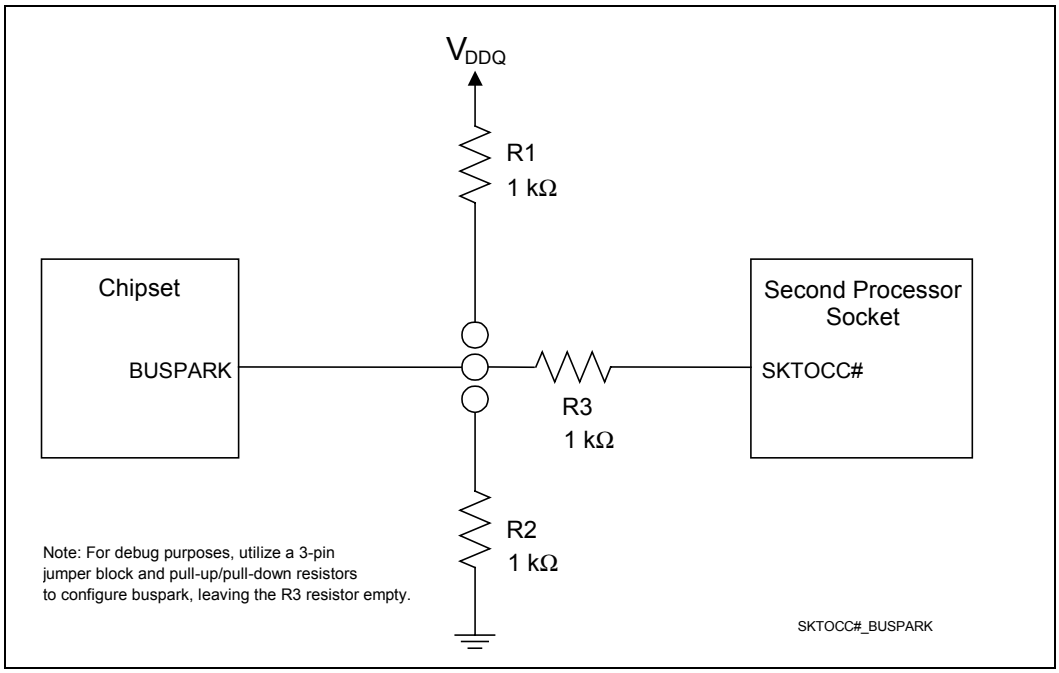
The SKTOCC# signal is an output from the processor used as an indication of whether a processor is installed or not. It will be connected to VSS when a processor is installed in the socket and will float when there is no processor present. SKTOCC# can be used to disable the VRM output for unpopulated processor sockets, the power supply output when no processors are installed, system bus parking in an dual processor system, and other features.

One possible implementation is to disable the bus parking feature of the processor when a second processor is installed in a dual-processor system. Bus parking allows the current bus owner to maintain bus ownership even if it currently does not have a pending transaction. If a transaction becomes pending before that bus owner relinquishes bus ownership, it can drive the transaction without having to arbitrate for the bus. The parked symmetric agent can then issue transactions 2 clocks sooner than if it had to participate in idle bus arbitration. As a result, enabling bus parking is strongly recommended for systems that have one processor installed.

For systems with two processors installed, bus parking will increase processor-to-processor bus ownership exchange by 2 clocks over the ownership-from-idle bus case. Bus parking could reduce transaction request bandwidth in multi-processor systems in the following cases. As a result, the ability to disable bus parking is recommend in multi-processor systems. Performance benchmarking is recommended to determine the optimum setting based on workload and application.

Connect the SKTOCC# of the second processor to the MCH's BUSPARK enable pin. Refer to the diagram in the following figure. The pull-up and pull-down resistors and the jumper block shown in the figure are optional.

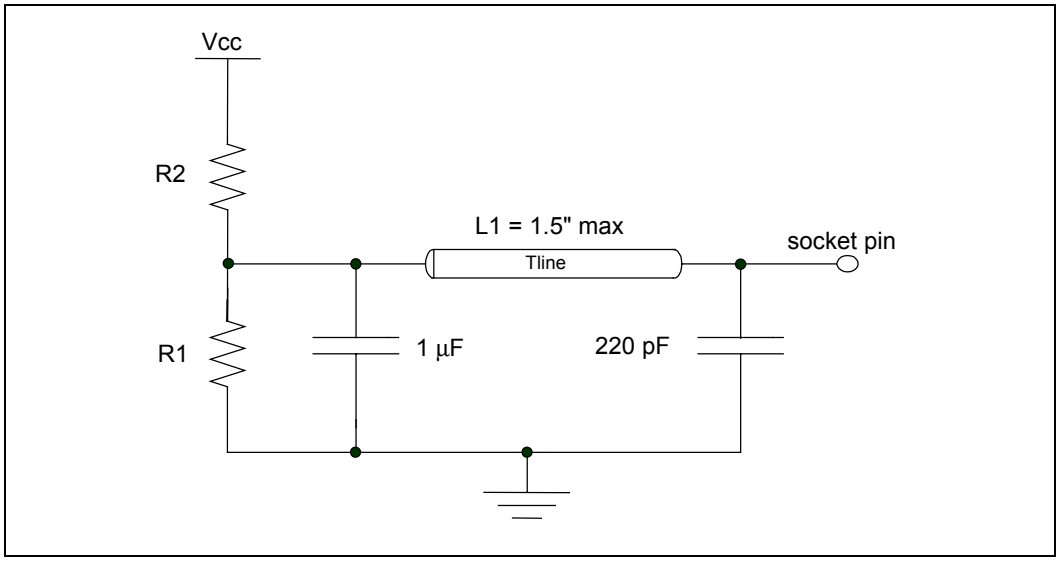
Figure 46. SKTOCC# Connection to Chipset BUSPARK Signal



5.5 MCH System Bus Interface

A voltage divider network should supply host interface reference voltages locally as shown in Figure 47 and Figure 48, as specified in Table 16.

Figure 47. Voltage Divider Network for Reference Voltage Generation



Note the following:

- The MCH must have only one dedicated voltage divider.
- Decouple the voltage divider with a 1 µF capacitor.
- Keep the voltage divider within 1.5 inches of the MCH V_{REF} ball.

Figure 48. Pull-Down Circuit

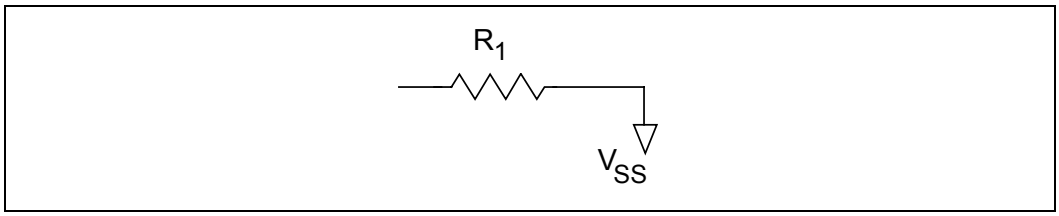


Table 16. Reference Voltage Network Values

Signal	R1	R2	Tolerance	Figure	Notes
HDVREF[3:0]	100 Ω	50 Ω	± 1%	Figure 47	1,2
HAVREF[1:0]	100 Ω	50 Ω	± 1%	Figure 47	1,2
CCVREF	100 Ω	50 Ω	± 1%	Figure 47	1,2
HRCOMP[1:0]	20.75 Ω	—	± 1%	Figure 48	3
HSWNG[1:0]	150 Ω	301 Ω	± 1%	Figure 47	4

NOTES:
1. 2/3 Vtt Resistor Network.
2. Single voltage divider for these signals.
3. Independent of board impedance.
4. 1/3 Vtt Resistor Network.

5.5.1 MCH System Bus I/O Decoupling Recommendations

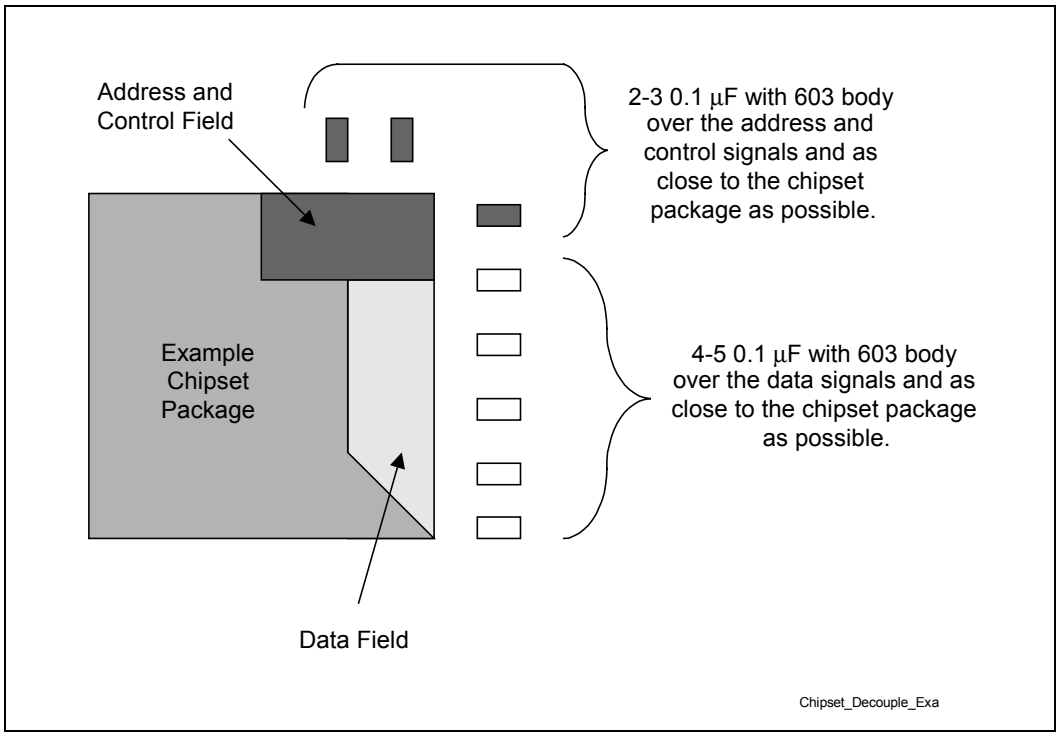
The primary objective of the decoupling recommendations for the chipset is to provide clean power delivery to the system bus I/O buffers. The split plane nature of chipsets creates power delivery concern.

The secondary objective of decoupling at the chipset is to minimize the impact of return path discontinuities that may occur between the chipset package and the motherboard. A return path discontinuity occurs in systems whose signals reference either power or ground, but not both (the chipset uses symmetric stripline interconnects that reference the signal to both Vcc and VSS). Systems that have this type of discontinuity (such as the recommended dual processor stack-up) should use the larger number of decoupling capacitors listed in the following guidelines for the chipset.

The following are decoupling recommendations for the MCH (see Figure 49):

- 4 minimum, 5 preferred 0.1 µF capacitors with 0603 packages distributed evenly over the system bus data lines
- 2 minimum, 3 preferred 0.1 µF capacitors with 0603 packages distributed evenly over the system bus address and control lines
- All capacitors placed as close as possible to the MCH package (within 150 mils).

Figure 49. I/O Decoupling Guidelines for the MCH



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6 Memory Interface Routing

6.1 Rambus* Channel Overview

The Rambus Channel is a multi-symbol interconnect. Because of the length of the interconnect and the frequency of operation, this bus is designed to allow multiple command and data packets to be present on a signal wire at any given instant. For example, the driving device can send the next data out before the previous data has left the bus.

The nature of the multi-symbol interconnect forces many requirements on the bus design and topology. First and foremost, a drastic reduction in reflected voltage levels is necessary. The interconnect transmission lines must be terminated at their characteristic impedance; otherwise the reflected voltage resulting from a mismatch in impedance will degrade signal quality. These reflections reduce noise, timing margins and the maximum operating frequency of the bus. Second, coupled noise can greatly affect the performance of high-speed interfaces. Just as in source synchronous designs, odd and even mode propagation velocity change can create skew between the clock and data or command lines which reduces the maximum operating frequency of the bus. Efforts must be made to significantly decrease crosstalk, as well as the other sources of skew.

To achieve these bus requirements, the Rambus Channel is designed to operate as a transmission line. All components, including the individual Direct RDRAM devices, are incorporated into the design to create a uniform bus structure that can support up to 33 devices (including the MCH) running at 800 MegaTransfers/second (MT/s).

The following sections describe the design guidelines that help ensure a robust Rambus Channel design.

For more information regarding Direct RDRAM device technology, refer to

http://www.rambus.com/developer/quickfind_documents.html.

The Intel 860 chipset supports the following types of memory configurations on its Direct RDRAM devices interface:

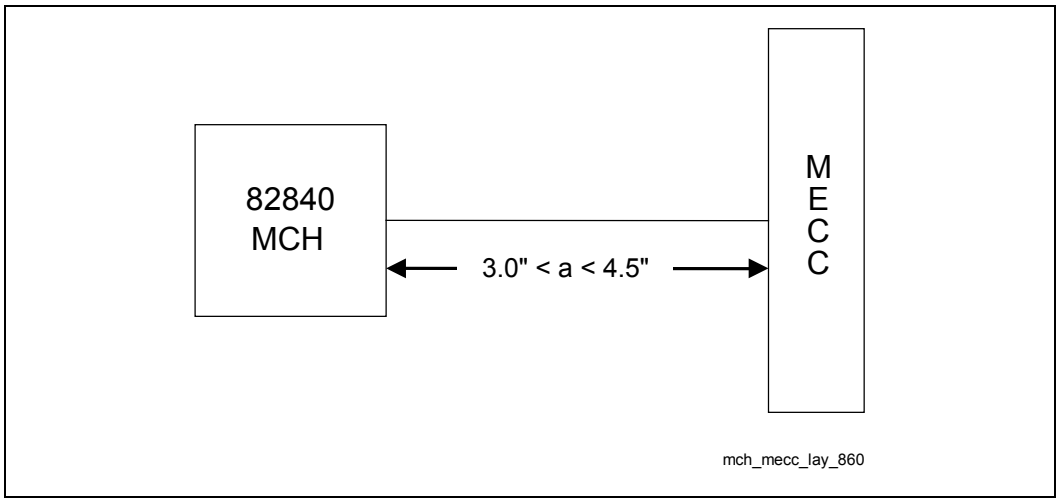
- The Memory Expansion Card (MEC).
- Direct RDRAM devices on the system board.

6.2 Memory Design with MEC/MECC (Inner Layer Routing)

The Memory Expansion Card (MEC) concept is intended to provide flexibility and scalability of memory to an Intel 860 chipset-based workstation platform. The Intel 860 chipset supports both RIMM modules down and MECC configurations. For routing guidelines for the Memory Expansion Card (MEC), refer to the *Intel® 860 Chipset Memory Expansion Card (MEC) Design Guide*.

The MCH-to-MECC routing guidelines are based on the usage of a Memory Expansion Card Connector (MECC) that meets the RIMM connector specification electrical characteristics.

Figure 50. Rambus* Channel Signal Groups



All Direct RDRAM device signals lengths between the MCH and the MECC should be between 3.0 inches (min) and 4.5 inches (max). Although channels A and B are not required to match one another, the difference between channels should be minimized and must meet MCH levelization requirements.

Refer to the *Intel® 860 Chipset Memory Expansion Card (MEC) Design Guide* for complete RSL and other signal routing guidelines to expansion devices (MRH-R).

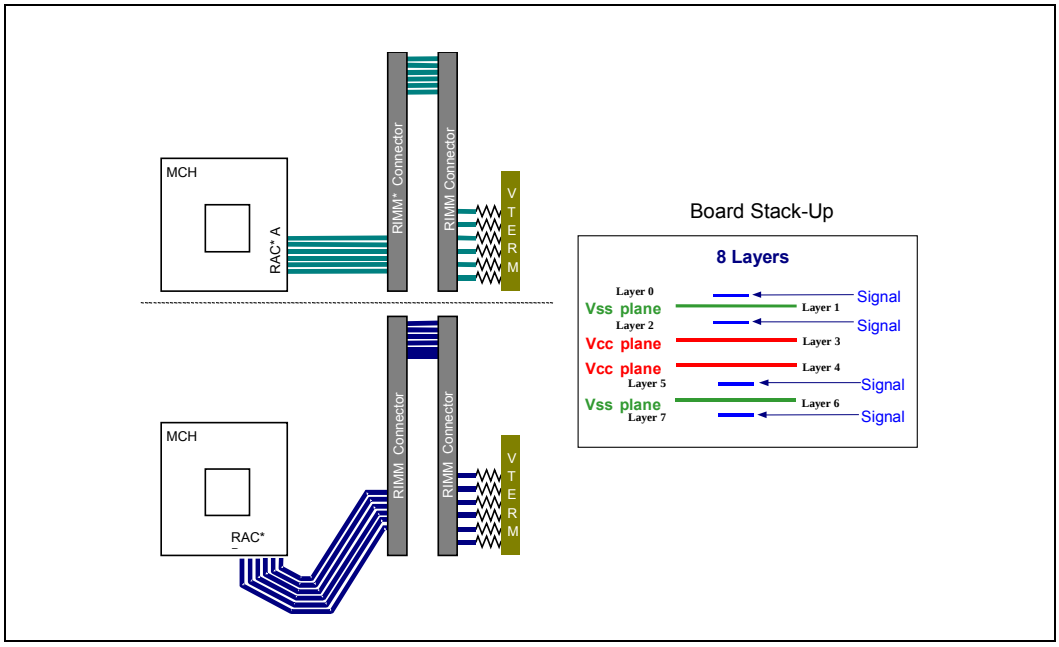
To maintain 28 Ω trace impedance, the RSL signals must be 18 mil wide. To control crosstalk and odd/even mode velocity deltas, there must be a 10 mil ground isolation trace between adjacent RSL signals. The 10 mil ground isolation traces must be connected to ground with a via every 1 inch. A 6 mil gap is required between the RSL signals and ground isolation traces. To ensure uniform traces, the trace width variation must be uniform on all RSL signals at every neck down. The RSL signals within each channel must be length matched to ± 10 mils in the line section between the MCH and first device (MRH-R) on the MEC using trace length matching methods.

Also, all RSL signals must have the same number of vias. It may be necessary to place additional vias (dummy vias) on RSL signals to meet the via-loading (equal number of vias) requirement, even if vias are not needed. Refer to the *Intel® 860 Chipset MEC Design Guide* for complete RSL and other signal routing guidelines to expansion devices (MRH-R).

6.3 Rambus* Channel Routing Guidelines

The MCH has two Rambus Channels. The following layout guidelines are applicable for each channel. Because of routing and timing margin, one channel should be routed entirely microstrip (outer layers) or stripline (inner layers). Figure 51 illustrates an example routing topology for the MCH.

Figure 51. Intel® 860 Chipset MCH Rambus* Channel Routing Example



The signals on the Rambus Channel are broken into three groups: Rambus Signaling Level (RSL) signals, CMOS signals, and clocking signals. The signal groups are described in Table 17.

Table 17. Rambus* Channel Signal Groups

Group	Signal
RSL Signals	DQA[8:0]
	DQB[8:0]
	RQ[7:0]
CMOS Signals	CMD(1)
	SCK*(1)
	SIO
Clocking Signals	CTM
	CTM#
	CFM
	CFM#

NOTE: These are high-speed CMOS signals

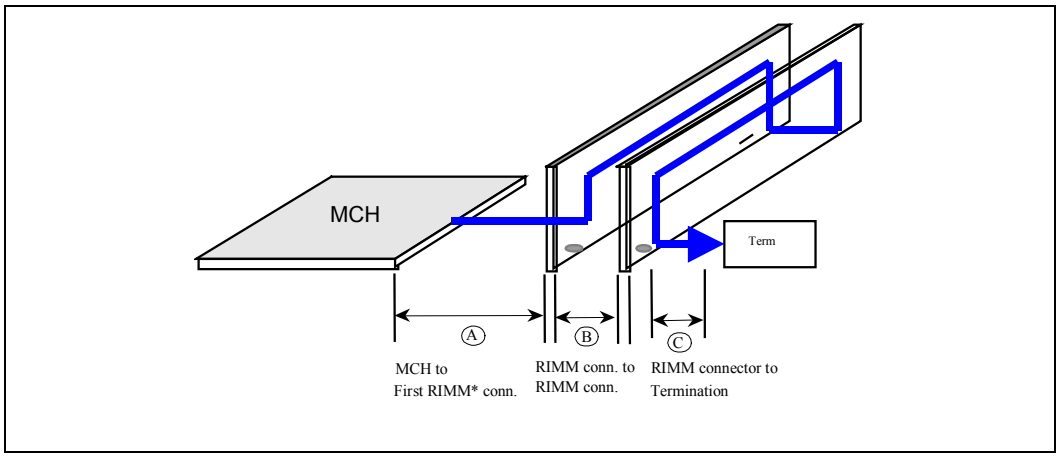
6.3.1 Rambus* Signaling Level (RSL) Signals

The Rambus Channel RSL signals are high-speed signals that transmit data between the MCH and RDRAM component at a maximum speed of 800 MHz. These signals start at the MCH, enter the first RIMM connector on either side, propagate through the RIMM connector, and then exit on the opposite side. The RSL signals continue through the second RIMM connector until they are terminated at Vterm. All unpopulated RIMM connector slots must have continuity modules in place to ensure that signals propagate to the termination at the end of the Rambus Channel.

The perfect matching of transmission line impedance and uniform trace length are essential for the Direct RDRAM device interface to work properly. Maintaining 28 Ω ± 10% loaded impedance for every RSL signal requires some changes to the standard trace width and board prepreg thickness. Typically, 28 Ω nominal impedance with 7 mil prepreg requires 28 mil wide traces. 28 mils wide traces are too wide to break out of the rows of RSL signals on the MCH. To reduce the trace width, a thinner prepreg is required. For example, a prepreg thickness of 4.0 mils to 4.5 mils allows 18 mil wide traces to meet the 28 Ω ± 10% nominal impedance requirement.

The following figure and table describe the Rambus Channel topology for a 28 Ω channel.

Figure 52. Example Rambus* Channel Routing



Note: This diagram only illustrates the routing of one Rambus Channel. However, the example routing shown can be applied to both channels.

Table 18. Rambus* Channel RSL Signal Lengths for RIMM* Connectors on Motherboard

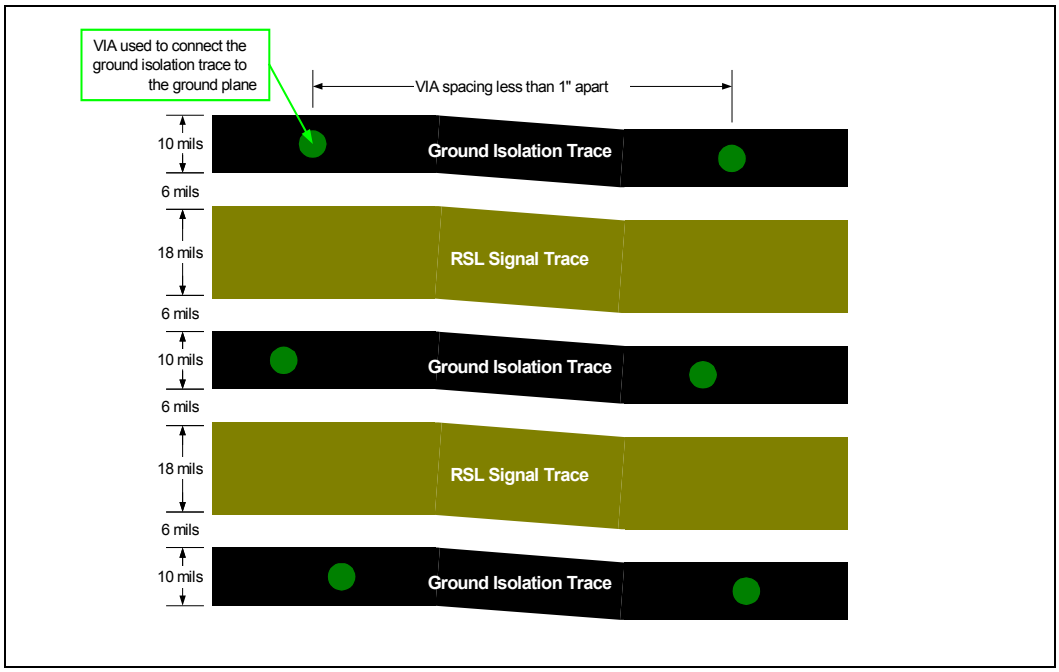
Reference Section	Trace Description	Trace Length
A	MCH to first RIMM connector for Rambus* Channel A or first RIMM for Rambus Channel B	1 inch to 6 inches
B	RIMM connector to RIMM connector for the same channel	0.4 inch to 1 inch
C	RIMM connector to Termination	0 inch to 2 inches(1)

NOTES:
1. Place termination resistors between RIMM connectors of the same channel, when possible, to reduce the trace length.

To ensure a solid memory subsystem design, the RSL signals routing rules must be followed. The following is a breakdown of the key areas to watch when you design your platform.

- To control crosstalk and odd/even mode velocity deltas, there must be a 10 mil ground isolation trace between adjacent RSL signals (see Figure 53). The 10 mil ground isolation traces must be connected to ground with vias distributed every 1 inch. Vias must be placed within 0.5 inch of the beginning and end of the ground isolation trace. A 6 mil gap is required between RSL signals and ground isolation traces.
- RSL signals must be length matched to ±10 mils in section "A" and ±2 mils in sections "B" using the trace length matching methods described in the following section. There is no trace length-matching requirement for traces in section 'C'. If signals are routed on inner and outer layers, the trace velocity differences must be accounted for to minimize channel skew.
- RSL signals must have the same number of vias. It may be necessary to place additional vias (dummy vias) on certain RSL signals, even if vias are not needed, to meet the via loading (equal number of vias) requirement.

Figure 53. RSL Routing Diagram Showing Ground Isolation Traces with Via Around Signals



Note: For the Intel 860 chipset Customer Reference Board (CRB), both inner and outer layer RSL trace width is 18 mils. Inner layer RSL trace width may vary depending on the board stack-up that is used. RSL signals should be no wider than 18 mils to prevent neck-down in the RIMM connector pin field.

Note: 10 mil ground isolation traces and 6 mil gaps are also considered effective for RSL signals less than 18 mils.

6.3.2 Rambus Signaling Level (RSL) Channel Compensation

The RSL and clocking signals requires special compensation for discontinuities introduced in the channel. Since the Rambus Channel only allows for 125 ps of interconnect skew, it is critical to minimize skew and to match the skew on RSL and clocking signals within a given channel. The next few sections describe how to compensate for skew due to package trace differences, vias, differential clock routing, and connectors.

When compensating a channel, the compensating techniques must be performed in the following layout order:

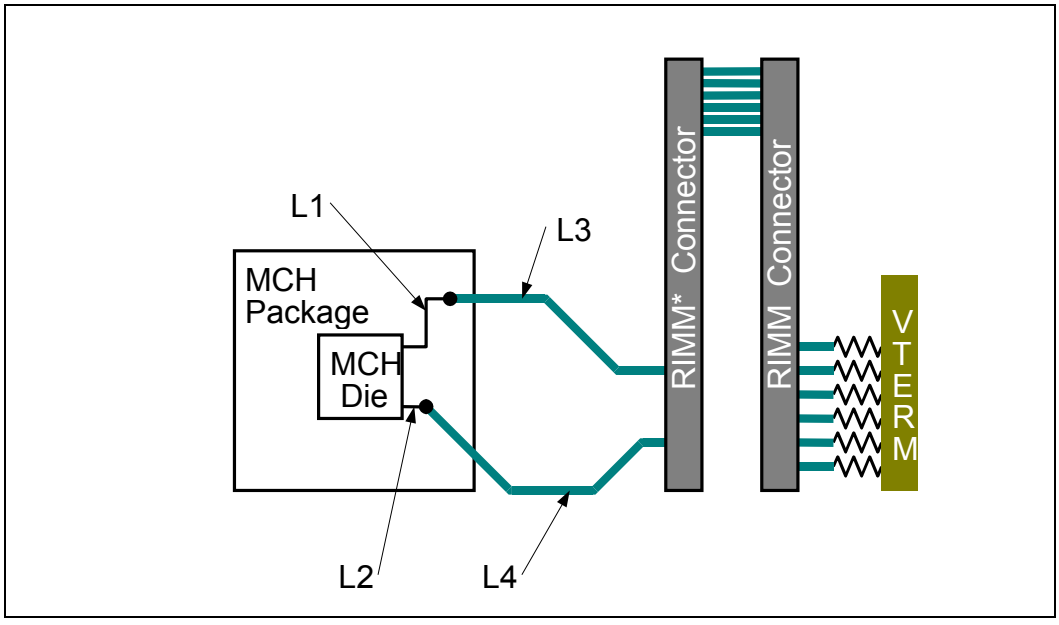
1. Package trace compensation
2. Via compensation
3. Differential clock compensation
4. Alternating signal layer for RIMM connector pin compensation
5. RIMM connector impedance compensation

6.3.2.1 Package Trace Compensation (RSL and Clocking Signals)

All RSL and clocking signals require pad-to-pin length matching between the MCH and the first RIMM connector to minimize skew. All RSL and clocking signals for a given channel require pad-to-pin trace matching within ± 10 mils.

The RIMM connector-to-RIMM connector trace length match requirement is ± 2 mils.

Figure 54. Rambus* Channel Trace Length Matching Example



Note: This diagram illustrates the routing of only one Rambus Channel. However, the example routing shown can be applied to both channels.

The following are a few definitions:

- Package Dimension (ΔL_{PKG}): a representation of the length from the pad to the ball.
- Board Trace Length (L_{MB}): the trace length on the board.
- Nominal Length: the length to which all signals are matched.

As Figure 54 shows, L1 plus L3 must be length matched to L2 plus L4 within ±10 mils.

Equation 4. Compensated Trace Length Calculation

$$\Delta L_{PCB} = (\Delta L_{PKG} * \text{Package}_{\text{TRACE VELOCITY}}) / PCB_{\text{TRACE VELOCITY}}$$

The PCB trace length for each signal is a calculated value, and may vary with designs. The nominal MCH package trace velocity is 167.64 ps/in. The $PCB_{\text{TRACE VELOCITY}}$ is board and layer dependent. $PCB_{\text{TRACE VELOCITY}}$ can change depending on the layer the board designer uses to route the RSL channel.

The following is the $PCB_{\text{TRACE VELOCITY}}$ for stripline and microstrip routing used on the Intel 860 chipset Customer Reference Board (CRB).

- Stripline velocity typically equals 172 ps/in
- Microstrip velocity typically equals 154 ps/in

The MCH package trace length information is contained in the *Intel® 860 Chipset: 82860 Memory Controller Hub (MCH) Datasheet*. The package trace length information presented in this document is normalized to the longest package trace length. The RSL and clocking signal lengths (ΔL_{PKG}) can be renormalized to any signal using Equation 5.

Equation 5. Normalized Trace Length Calculation

$$\text{New } \Delta L_{PKG} = \Delta L_{PKG} - \Delta L_{\text{NORMALIZED RSL}}$$

It is not necessary to account for CMOS signal package compensation. For PCB routing, the mismatch between the CMOS signals (CMD, SCK) and the RSL signals should be kept as small as possible.

6.3.2.2 Via Compensation

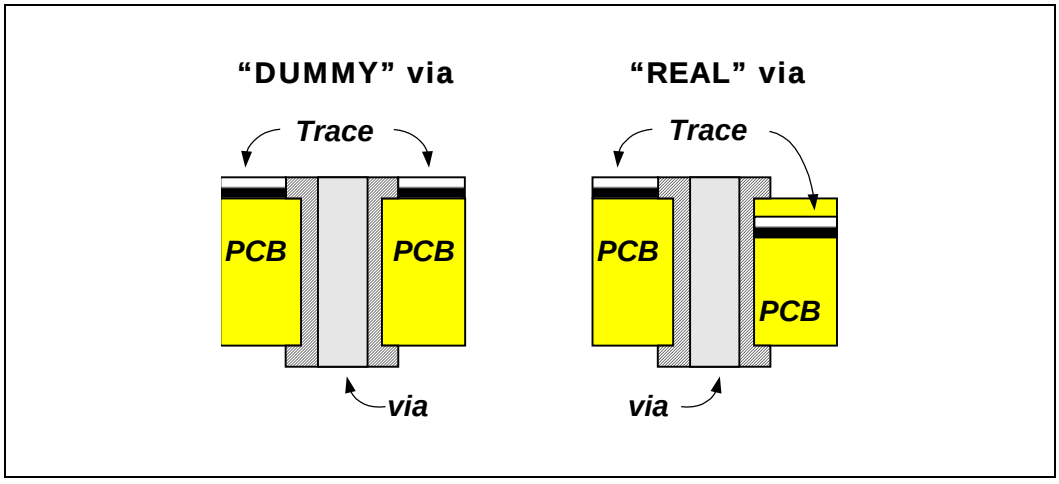
All RSL and clocking signals must have the same number of vias. As a result, each trace will have at least one via because some of the RSL signals must be routed on other layers of the motherboard. The via should be placed as close as possible to the MCH package ball. For the channel routed on outer layers (microstrip), it will be necessary to place a "dummy" via on all signals. The electrical characteristics between dummy and "real" vias are not exact, so additional compensation is needed on each signal that has dummy via.

Dummy vias are not required on the channel routed on the inner layers (stripline) because all signals require a real via.

Each signal with a dummy via must have 25 mils of additional trace length. The additional 25 mils trace length must be added to the signal routed on the top layer, after length matching.

"Real" via = "Dummy" via + 25 mils of trace length

Figure 55. "Dummy" vs. "Real" Vias



6.3.2.3 Differential Clock Compensation

If the Direct Rambus Clock Generators (CTM, CTM#, CFM and CFM#) are routed differentially, the clock signals must be longer than the RSL signals due to their increased trace velocity because they are routed as a differential pair. To calculate the length for each clock, use Equation 6 for microstrip and Equation 7 for stripline routing.

Equation 6. Clock Trace Length Calculation for Microstrip

$$\text{Clock Length} = \text{Nominal RSL Signal Length (package + board)} * 1.030^{(1)}$$

Note: This compensation factor is based on the Intel 860 chipset Customer Reference Board (CRB) stack-up.

Equation 7. Clock Trace Length Calculation for Stripline

$$\text{Clock Length} = \text{Nominal RSL Signal Length (package + board)} * 1.009^{(1)}$$

Note: This compensation factor is based on the Intel 860 chipset Customer Reference Board (CRB) stack-up.

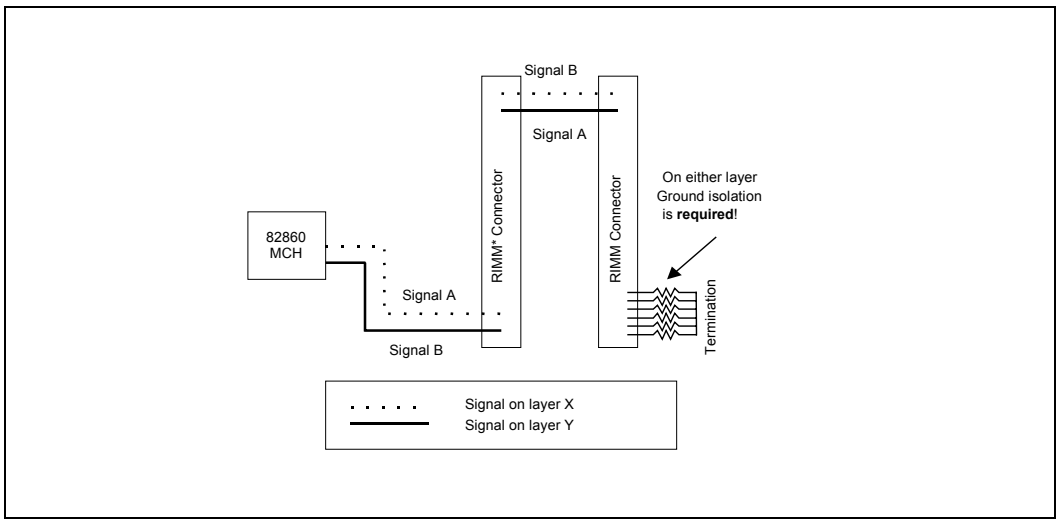
The lengthening of the clock signals to compensate for their trace velocity change applies only to routing between the MCH and first RIMM connector. The clock signals should be matched in length to the RSL signals between RIMM connectors.

6.3.2.4 Signal Layer Alteration for RIMM* Connector Pin Compensation

RSL and clocking signals must alternate layers because they are routed through the channel to compensate for signals on the bottom layer having to travel a longer distance through the pin connector. This is illustrated in Figure 56. For example if a signal is routed on the top layer from the MCH to the first RIMM connector, it must be routed on the bottom layer from the first RIMM connector to the second RIMM connector. This rule also holds true for inner layer routing. If a signal is routed on the top inner layer from the MCH to the first RIMM connector socket, it must be routed on the bottom inner layer from the first RIMM connector to the second RIMM connector.

All RSL and clocking signals from the second RIMM connector to the termination resistor should be routed on the top layer.

Figure 56. RSL and Clocking Signal Layer Alteration



6.3.2.5 RIMM* Connector Impedance Compensation

The RIMM connector inductance has been shown to cause an impedance discontinuity on the Rambus Channel. This can reduce voltage and timing margin. To compensate for the inductance of the connector, a compensating capacitance is required on each RSL and clocking connector pin. This compensating capacitance must be added to the following connector pins at each connector.

- LCTM
- LCTM#
- RCTM
- RCTM#
- CMD
- LCFM
- LCFM#
- RCFM
- RCFM#
- SCK
- LROW[2:0]
- RROW[2:0]
- LCOL[4:0]
- RCOL[4:0]
- RDQA[8:0]
- LDQA[8:0]
- RDQB[8:0]
- LDQB[8:0]

The amount of capacitance needed depends on the distance that the signals have to travel though the RIMM connector pin (i.e., a signal on the bottom layer has to travel though more of the RIMM connector pin than a signal on the top layer). This can be achieved on the motherboard by adding a copper tab to the specified RSL pins at each connector.

Table 19. RSL and Clocking Signal RIMM* Connector Capacitance Requirement

RSL and Clocking Signal Routing Layer	Capacitance (pF)[1]
Top	0.8
Inner 1	0.9
Inner 2	1.25
Bottom	1.36

NOTE: These numbers are based on Intel's Customer Reference Board (CRB) eight layer stack-up design.

The copper tab area for the recommended stack-up was determined through simulation. The amount of capacitance required is determined by the layer through which the RSL or clocking signal is routed. The placement of the copper tabs can be on any signal layer, independent of the layer on which the RSL signal is routed.

Capacitance for a different stack-up assuming a 62 mil board thickness can be computed by linear interpolation. Equation 8 is used to determine the amount of capacitance needed on any stripline layer.

Equation 8. Calculation for a Stripline C-Tab

$$Ctab_{LayerX} = 0.8\ pF + (1.36\ pF - .8\ pF)(X/62)$$

- X is the distance in mils from the top of the board to the stripline signal layer in which the RSL or clocking signals are routed.

Equation 9 is an approximation that can be used to calculate copper tab area on the outer layer.

Equation 9. Copper Tab Capacitance Calculation

$$Length * Width = Area = [C_{plate} * Thickness\ of\ prepreg] / [\varepsilon_0 * \varepsilon_r * 1.1]$$

- Cplate = Capacitance of the plates
- ε_0 = 2.25 x 10–16 Farads/mil
- ε_r = Relative dielectric constant of prepreg material
- Thickness of prepreg = Stack-up dependent
- Length, Width = Dimensions in mils of copper plate to be added
- Factor of 1.1 accounts for fringe capacitance

The following are example calculations for a board with $\varepsilon_r = 4.2$, and prepreg thickness 4.5. Note that these numbers will vary according to prepreg thickness.

Table 20. Copper Tab Area Calculation

Layer	Dielectric Thickness	Separation Between Signal Traces & Copper Tab	Minimum Ground Flood	Air Gap between Signal & GND Flood	Compensating Capacitance in Cplate (pF)(1)	CTAB Area in sq mils
Top	4.5	6	10	6	0.8	~3463
Inner 1	4.5	6	10	6	0.9	~3896
Inner 2	4.5	6	10	6	1.25	~5300
Bottom	4.5	6	10	6	1.36	~5887

NOTE: These numbers are based on Intel's Customer Reference Board eight-layer stack-up design.

Note that more than one copper tab shape may be used as shown in the following figure. The dimensions are based on copper area over the ground plane. The actual lengths and widths of the tabs may be different because of routing constraints (e.g., if a tab must extend to center of hole or anti-pad). The following figures show a routing example of tab compensation capacitors.

Note: The capacitor tabs must not interrupt ground floods around the RIMM connector pins, and they must be connected to avoid discontinuity in the ground plane as shown.

Figure 57. Top Layer CTAB with RSL Signal Routed on the Same Layer (Ceff = 0.8 pF)

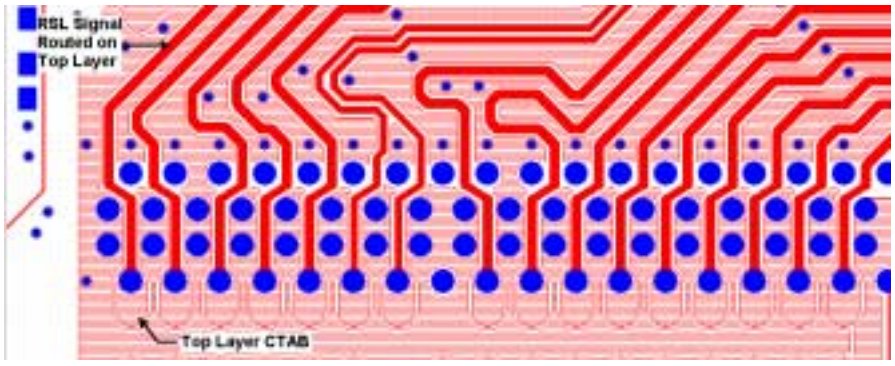
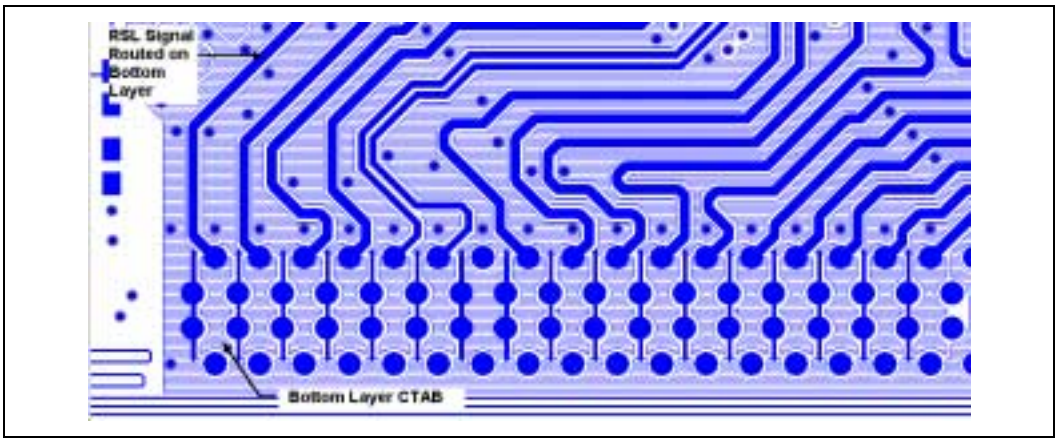
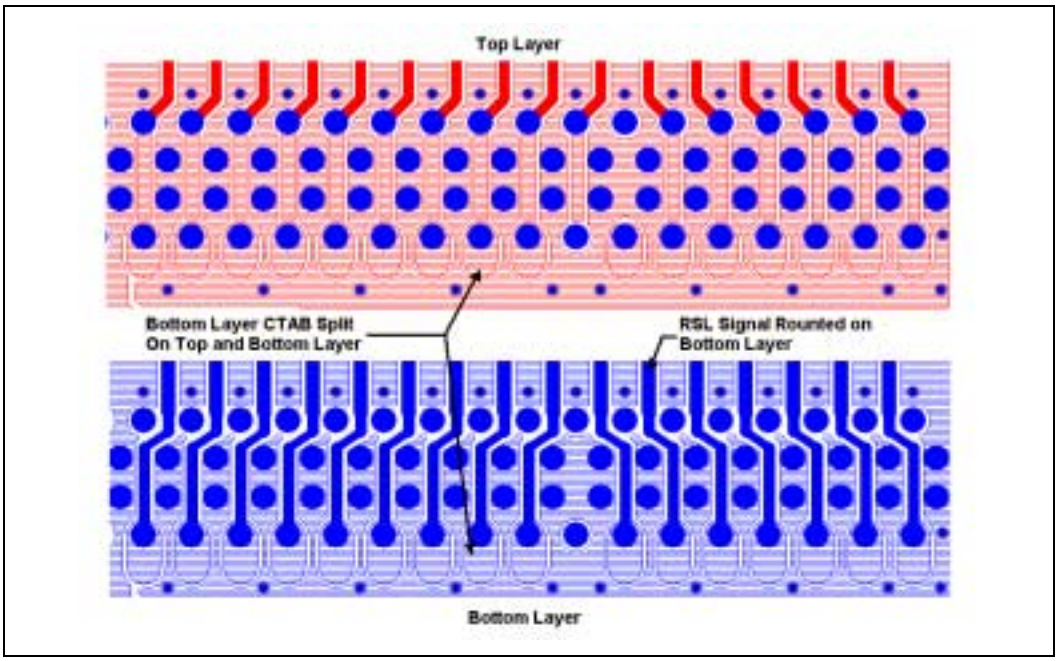


Figure 58. Bottom Layer CTAB with RSL Signal Routed on the Same Layer (Ceff = 1.35 pF)



The CTAB can be implemented on the multiple layers to minimize routing and space constrains. The following figure shows the use of CTABs on the top and bottom layer for bottom layer RSL and clocking signals routed between RIMM connectors.

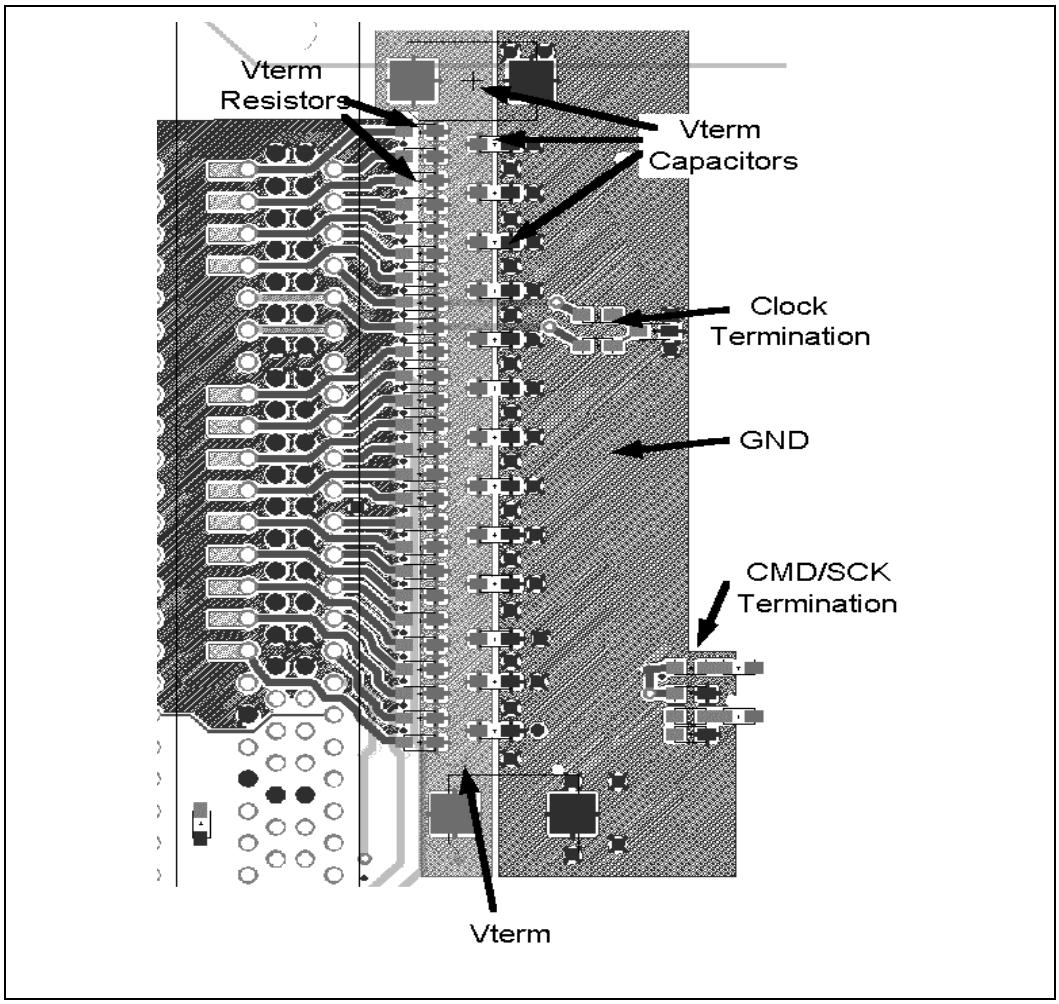
Figure 59. Bottom Layer CTABs Split Across the Top and Bottom Layer to Achieve Ceff ~1.35 pF



6.3.3 RSL Signal Termination

All RSL signals must be terminated to 1.8 V (Vterm) using 27 Ω ± 1% or 28 Ω ± 2% resistors at the end of the channel opposite the MCH. Resistor packs are acceptable. However, discrete resistors are recommended for increased margin and control. The RSL and clocking signals from the last RIMM connector to termination should be routed on the top layer. Vterm must be decoupled using high-speed bypass capacitors (one 0.1 µF ceramic chip capacitor per two RSL lines) near the terminating resistors. Additionally, bulk capacitance is required. Assuming a linear regulator with approximately 20 µs response time, two 100 µF tantalum capacitors are recommended. The trace length between the last RIMM connector and the termination resistors should be less than 2 inches. Length matching in this section of the channel is not required. The Vterm power island should be AT LEAST 50 mils wide. This voltage is not required during Suspend-to-RAM (STR).

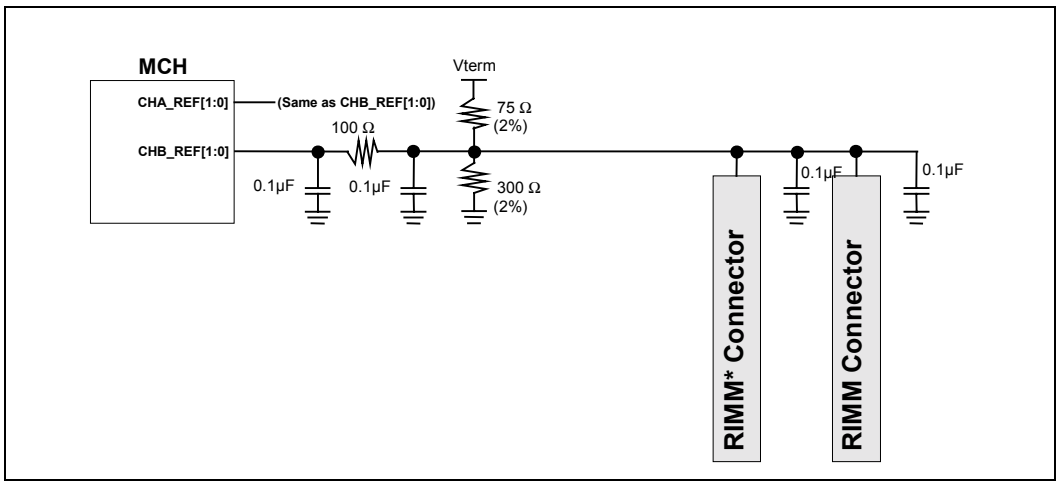
Figure 60. Direct RDRAM* Device Termination Example



6.3.4 Direct RDRAM* Device Reference Voltage

The Direct RDRAM device reference voltage (RAMREF) must be generated as shown in Figure 61. RAMREF should be generated from a typical resistor divider using 2% tolerant resistors. Additionally, RAMREF must be decoupled locally at each RIMM connector, at the resistor divider network, and at the MCH. Finally, a 100 Ω series resistor is required near the MCH. The RAMREF signal should be routed with 10 mils wide traces.

Figure 61. RAMREF Generation Example Circuit

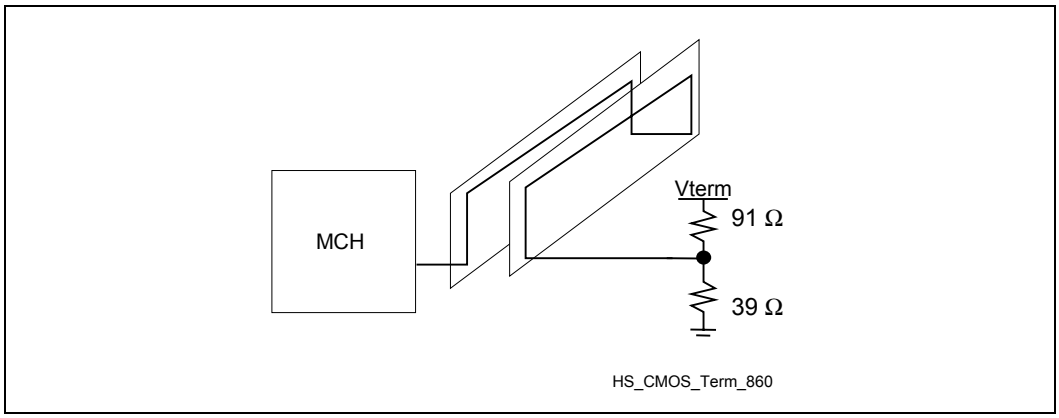


Note: The RAMREF Generation Circuit is not shown for Channel A in Figure 61, but the circuit is the same as the one shown for Channel B.

6.3.5 High Speed CMOS Routing

Because of the synchronous requirements between RSL signals and high-speed CMOS signals, the CMOS signals should be routed as part of the RSL channel. They must be impedance matched and properly terminated (using a different termination scheme than the RSL signals). It is not necessary to perform the length match calculation for high-speed CMOS signals. For PCB routing, the mismatch between the CMOS signals (CMD, SCK) and the RSL signals should be kept as small as possible.

Figure 62. High Speed CMOS RC Termination



A CMOS voltage must be supplied to each RIMM connector. This CMOS voltage is used by the Direct RDRAM device CMOS interface. This voltage (Vcmos) must be 1.8 V and the maximum load is 3 mA. Additionally, this voltage must be supplied during Suspend-to-RAM. Therefore, Vterm and Vcmos cannot be generated from the same source. Because of the low power requirements, Vcmos can be generated by a 36 / 100 Ω resistor divider from 2.5 V.

The high-speed CMOS signals require AC termination as shown Figure 62 with 91 Ω pull-up and 39 Ω pull-down resistors.

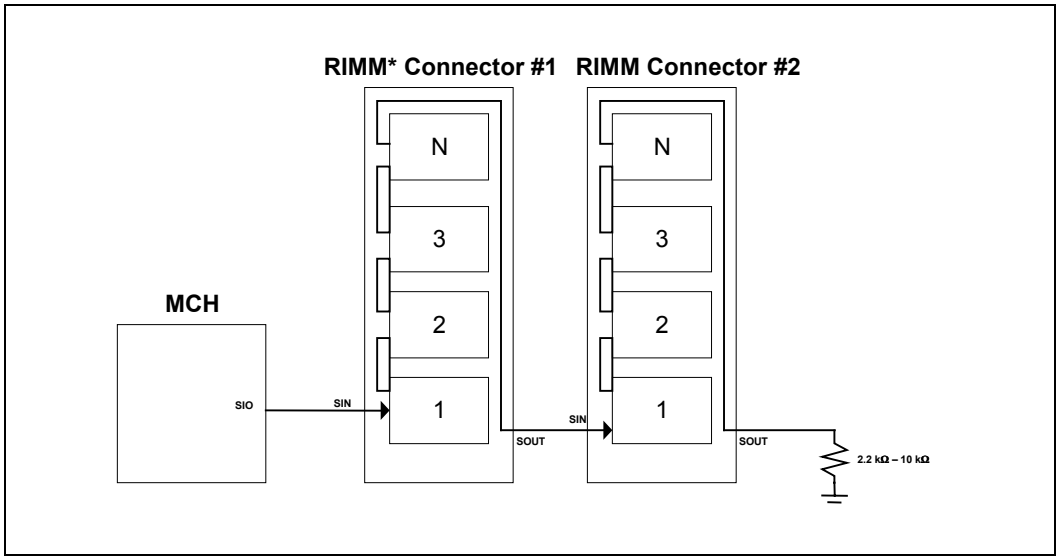
6.3.6 SIO Routing

The SIO signal is a bi-directional signal that operates at 1 MHz. This signal must be routed from MCH to RIMM connectors as follows (see Figure 63):

- MCH SIO ball to the first RIMM connector's SIN pin (RIMM #1–Pin B36)
- First RIMM connector's SOUT pin (RIMM #1–Pin A36) to the second RIMM connector's SIN pin (RIMM #2–Pin B36)
- Second RIMM connector's SOUT pin (RIMM #1–Pin A36) to terminating resistor that is tied to GND

The SIO signal enters the first RIMM connector, propagates through all the devices on the RIMM connector (this signal is buffered by each device), then exits the RIMM connector. A 2.2 kΩ–10 kΩ terminating resistor is required on the last RIMM connectors SOUT pin. This resistor must be tied to GND. The SIO is routed with a 5 mil wide, 60 Ω trace.

Figure 63. SIO Routing



6.3.7 Suspend-to-RAM Shunt Transistor

When the system enters or exits Suspend-to-RAM, power ramps to the MCH (i.e., it is powering-up or powering-down). When power is ramping, the state of the MCH outputs is not guaranteed. Therefore, the MCH may drive the CMOS signals and issue CMOS commands. The only command Direct RDRAM device would respond to is the Power-Down Exit command. To avoid the MCH inadvertently taking the Direct RDRAM device out of power-down due to the CMOS interface being driven during power ramp, the SCK (CMOS clock) signal should be shunted to ground when the MCH is entering and exiting Suspend-to-RAM. This shunting can be accomplished using the NPN transistor having a sinking capability of 300 mA at 400 mV. The transistor should also have a Cobo of 15 pF or less with a signal switching range of 0.1–1.5 V. Lastly, shunting transistors must not have their bases tied directly together. See Figure 64 for the SCK/CMD circuitry. Single and Dual Package sample transistors are listed in the following table.

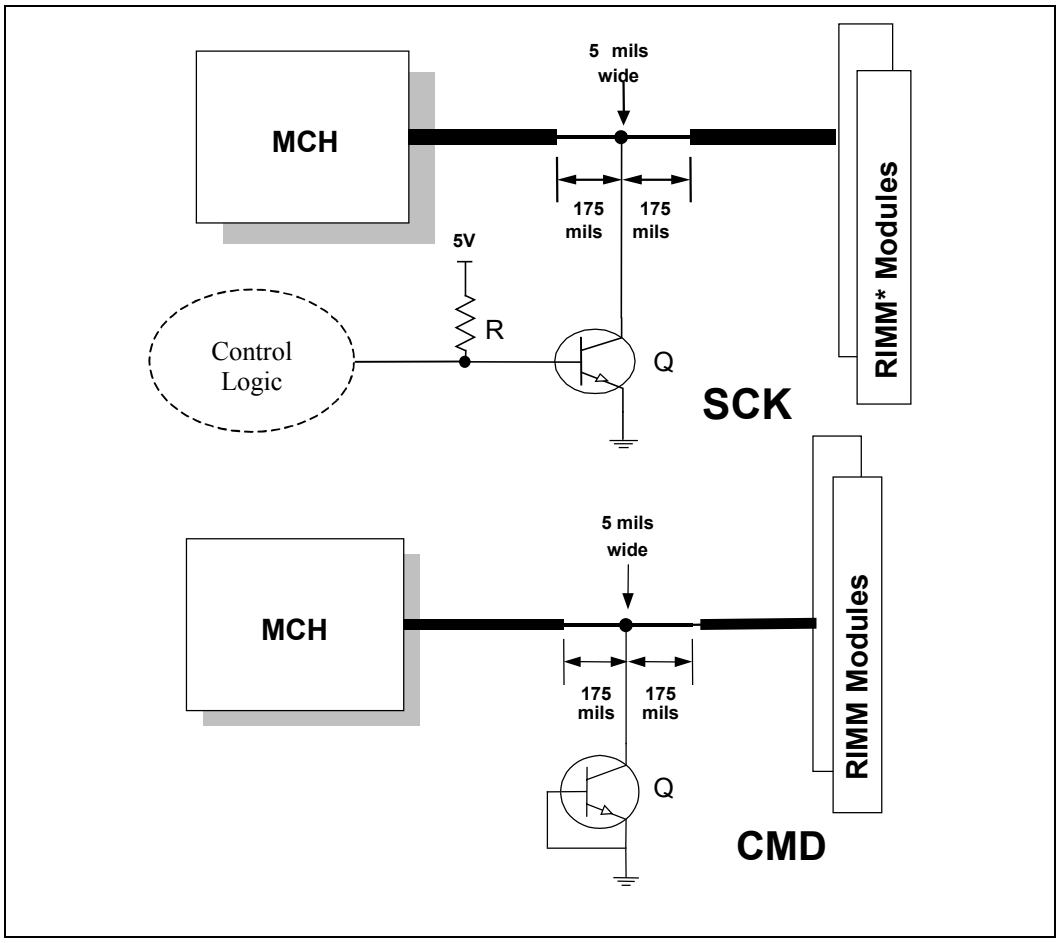
Note: The use of these transistors alone does not guarantee the preceding conditions will be met. Each design must ensure that the transistor can sink the appropriate amount of current by properly driving the base. Resistances should include source impedance driver.

To match the electrical characteristics on the SCK signal, the CMD signal needs a dummy transistor. This transistor's base should be tied to ground (i.e., always turned off). To minimize impedance discontinuities, the traces for CMD and SCK must have a neck down from 18 mil traces to 5 mil traces for 175 mils on either side of the SCK/CMD attach point as shown in the following figure.

Table 21. Single and Dual Package Sample Transistors

Package	Series Resistor I	Power
Single (Q)		
MMBT2222LT1D	1 kΩ	5 V
MMBT100A	300 Ω	5 V
Dual		
MMDT2222A	1 kΩ	5 V

Figure 64. Direct RDRAM* Device CMOS Shunt Transistor

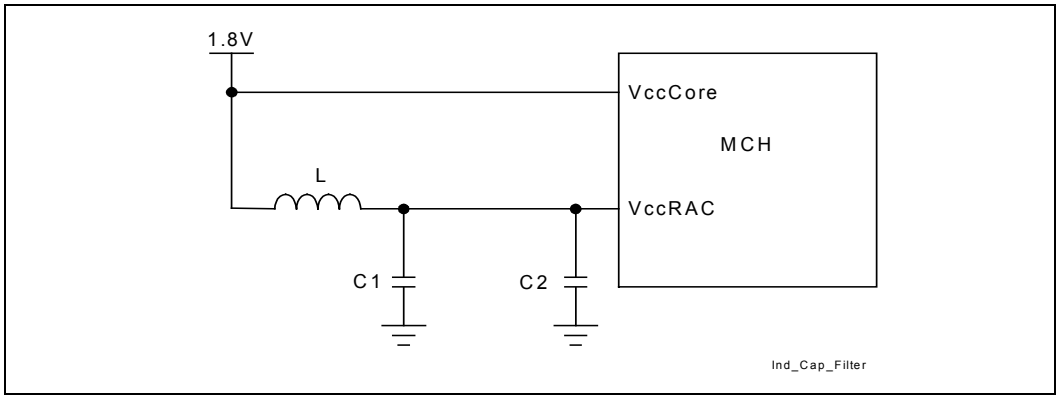


NOTE: This implementation is applicable for RIMM modules down solution only and is not needed on the repeater channels. Also, this implementation is not necessary if Suspend-to-RAM is not supported within the system

6.4 1.8 V RAC Isolation Solution

The 82860 MCH requires a low-pass filter on the V_{CC}RAC pins to meet clock jitter specifications. The filter may be configured as either an inductor-capacitor (LC) filter, or a ferrite bead-capacitor filter. For more details, see the following two figures. The inductor or ferrite bead must have a minimum current capacity of 500 mA, and a maximum DC resistance of 100 mΩ. DC drop is a concern because of the series element between the RAC and 1.8 V supply. The V_{CC}RAC pins for the 82860 MCH are listed in Table 22.

Figure 65. Inductor-Capacitor Filter Circuit

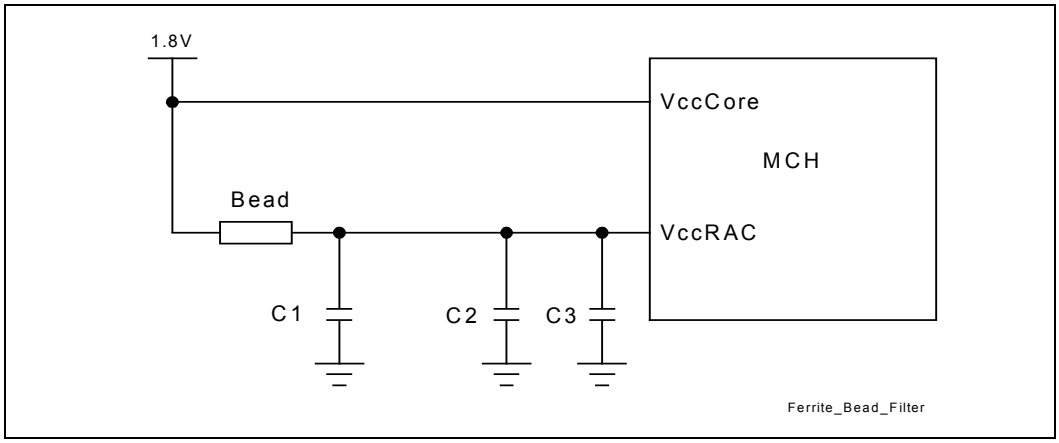


Simulations and validations indicate that L = 3.3 nH and C1 = 3.3 µF forms an adequate inductor-capacitor filter. The filter must be located within 2 inches of the device, and the layout of V_{CC}RAC connections should follow high-speed design practices.

In addition to the low-pass filter, the RAC requires local decoupling capacitors. These decoupling capacitors should be located close to the RAC pins to control self-induced RAC noise. For the inductor-capacitor filter, two to three 0.1 µF capacitors (C2) for both RACs should provide adequate decoupling between V_{CC}RAC and VSS.

The inductor-capacitor filter and its associated decoupling capacitors can be implemented using 0805 size components.

Figure 66. Ferrite Bead Filter Circuit



As an alternate solution, a 10 Ω (@ 100 MHz) ferrite bead and a 10 µF capacitor (C1) forms an adequate ferrite bead-capacitor filter. The filter must be located within 2 inches of the device, and the layout of V_{CC}RAC connections should follow high-speed design practices.

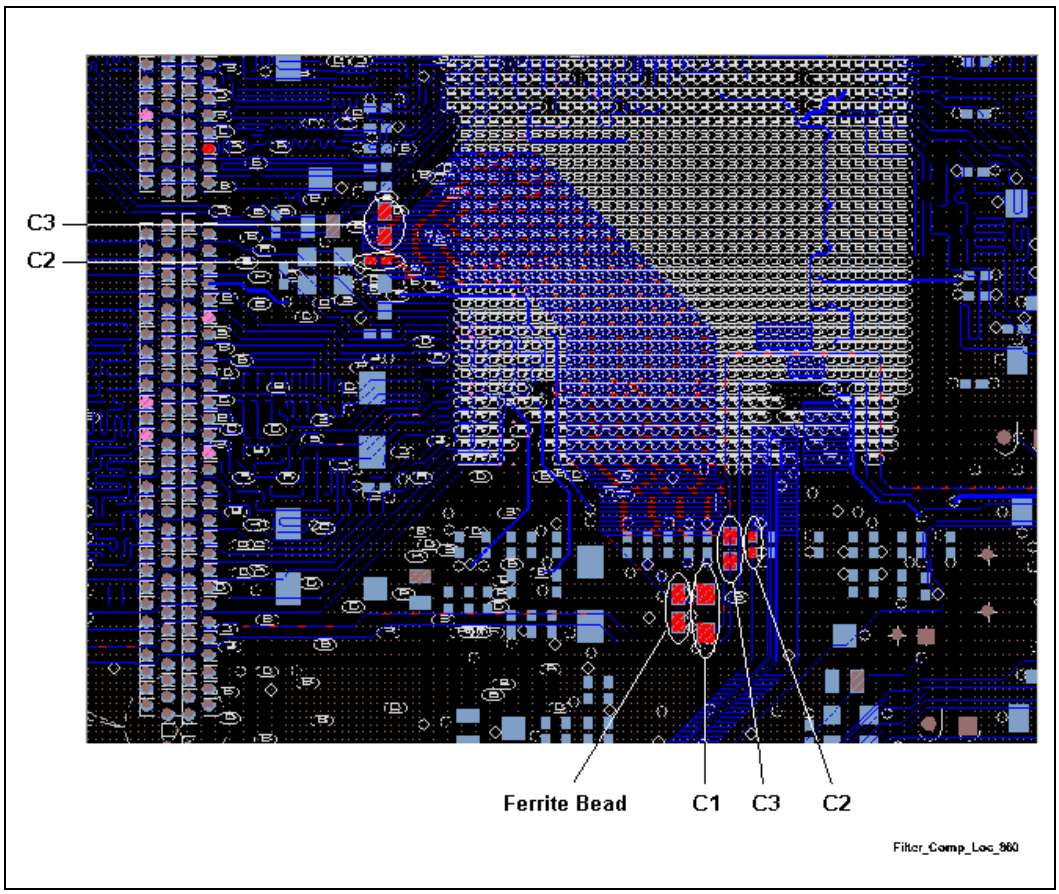
In addition to the ferrite bead filter, the RAC requires local decoupling capacitors. These decoupling capacitors should be located close to the RAC pins to control self-induced RAC noise. For the ferrite bead filter, use a minimum number of two 0.1 µF capacitors (C2) per RAC, and a minimum of one 1.0 µF capacitor (C3) for both RACs. The layout of the capacitor connections should follow high-speed design practices.

The ferrite bead filter and its associated decoupling capacitors can also be implemented using 0805 components except for the 10 µF capacitor, which is a 1206 size component.

Table 22. 82860 MCH 1.8 V RAC Pinout

82860 MCH 1.8 V RAC Pinout Location	Channel A	Channel B
Ball	AB30	F25
	W30	C22
	R30	F21
	AA27	F20
	Y27	C19
	R27	F15
		C15

Figure 67. RAC Isolation Filter Component Locations on Customer Reference Board



7 AGP Interface Routing

For detailed AGP Interface functionality (protocols, rules and signaling mechanisms, etc.) refer to the *AGP Interface Specification, rev. 2.0*, which can be obtained from

http://www.agpforum.org.

This design guide focuses only on specific Intel 860 chipset-based platform recommendations.

The latest *AGP Interface Specification* enhances the functionality of the original *AGP Interface Specification, rev. 1.0* by allowing 4X data transfers and 1.5 V operation. In addition to these enhancements, additional performance enhancement and clarifications, such as fast write capability, are included in the *AGP Interface Specification, rev. 2.0*. The 82860 MCH supports these enhanced features and 1.5 V signaling only.

The 4X mode of operation on the AGP interface provides for "quad-sampling" of the AGP AD (Address/Data) and SBA (Side-Band Addressing) buses. This means data is sampled four times during each 66 MHz AGP clock cycle, or each data cycle is ¼ of 15 ns or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time, not the clock cycle time. During 2X mode, data is sampled twice during a 66 MHz clock cycle; therefore, the data cycle time is 7.5 ns. These high-speed data transfers are accomplished using source synchronous data strobing for 2X mode, and differential source synchronous data strobing for 4X mode.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, it is important to minimize noise and propagation delay mismatch. Noise on the data lines cause the settling time to be large. If the mismatch between a data line and the associated strobe is too great or if there is noise on the interface, incorrect data will be sampled.

The AGP signals are broken into three groups: 1x timing domain, and 2X/4X timing domain signals. In addition, the 2X/4X timing domain signals are divided into three sets of signals (#1–#3). All signals must meet the minimum and maximum trace length, width and spacing requirements. The trace length matching requirements are applicable only between the 2X/4X timing domain signal sets.

Table 23. AGP 2.0 Signal Groups

1x Timing Domain	2X/4X Timing Domain		Miscellaneous Signals
CLK	SET #1	AD[15:0]	USB+
RBF#		C/BE[1:0]#	USB-
WBF#		AD_STB0	OVRCNT#
ST[2:0]		AD_STB0#	PME#
PIPE#	SET #2	AD[31:16]	TYPDET#
REQ#		C/BE[3:2]#	PERR#
GNT#		AD_STB1	SERR#
PAR		AD_STB1#	INTA#
FRAME#	SET #3	SBA[7:0]	INTB#
IRDY#		SB_STB	
TRDY#		SB_STB#	
STOP#			
DEVSEL#			

Strobe signals are not used in the 1x AGP mode. In 2X AGP mode, AD[15:0] and C/BE[1:0]# are associated with AD_STB0, AD[31:16] and C/BE[3:2]# are associated with AD_STB1, and SBA[7:0] is associated with SB_STB. In 4X AGP mode, AD[15:0] and C/BE[1:0]# are associated with AD_STB0 and AD_STB0#, AD[31:16] and C/BE[3:2]# are associated with AD_STB1 and AD_STB1#, and SBA[7:0] is associated with SB_STB and SB_STB#.

7.1 AGP Routing Guidelines

The following section documents the recommended routing guidelines for Intel 860 chipset-based designs. All aspects of the interface are covered from signal trace length to decoupling. These trace length guidelines apply to ALL of the signals listed as 2X/4X timing domain signals. These signals should be routed using 5 mil (60 Ω) traces.

Note: These guidelines are not intended to replace thorough system simulations and validation.

7.1.1 1X Timing Domain Signal Routing Guidelines

1x signals should adhere to the follow routing guidelines:

- The maximum trace length is 7.5 inches for all 1X timing domain signals
- 1X timing domain signals can be routed with 5 mil minimum trace separation
- There are no trace length matching requirements for 1X timing domain signals

7.1.2 2X/4X Timing Domain Signal Routing Guidelines

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. The maximum length of the AGP interface defines which set of routing guidelines must be used. Guidelines for short AGP interfaces (e.g., < 6 inches) and the long AGP interfaces (e.g., > 6 inches and < 7.25 inches) are documented separately. The maximum length allowed for the AGP interface is 7.25 inches.

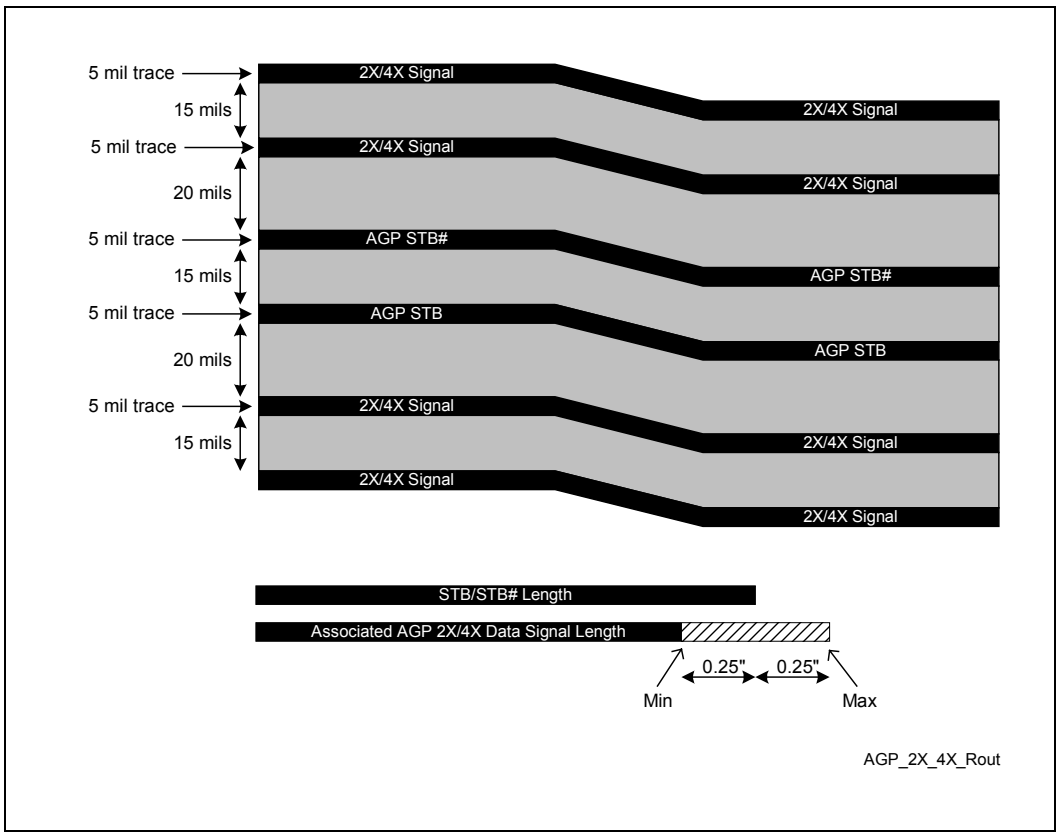
7.1.2.1 Trace Lengths Less Than 6 Inches

If the AGP interface is less than 6 inches with 60 Ω ± 10% board impedance, at least 5 mil traces with at least 15 mils of space (1:3) between signals is required for 2X/4X lines (data and strobes). These 2X/4X signals must be matched to their associated strobe within ± 0.25 inch. For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 5.3 inches long, the data signals associated to those strobe signals (e.g., AD[15:0] and C/BE#[2:0]), can be 5.05 inches to 5.55 inches long. While another strobe set (e.g., SB_STB and SB_STB#) could be 4.2 inches long and the data signals associated to those strobe signals (e.g., SBA[7:0]) can be 3.95 inches to 4.45 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface; therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length matched to less than ± 0.1 inch (that is, a strobe and its compliment must be the same length within 0.1 inch).

If the board impedance is 15%, the trace spacing increases to 20 mils. See the AGP interfaces trace length summary section for detailed information regarding 15% tolerance signals.

Figure 68. AGP 2X/4X Routing Example for Interfaces < 6 Inches



7.1.2.2 Trace Lengths Greater Than 6 Inches and Less Than 7.25 Inches

Longer lines have more crosstalk. Therefore, to reduce skew, longer line lengths require a greater amount of spacing between traces. For line lengths greater than 6 inches and less than 7.25 inches, 1:4 routing is required for all data lines and strobes with a 10% tolerance impedance. For these designs, the line length mismatch must be less than ± 0.125 inch within each signal group (between all data signals and the strobe signals).

For example, if a set of strobe signals (e.g., AD_STB0 & AD_STB0#) is 6.5 inches long, the data signals that are associated to those strobe signals (e.g., AD[15:0] & C/BE#[2:0]), can be 6.475 inches to 6.625 inches long. Another strobe set (e.g., SB_STB & SB_STB#) could be 6.2 inches long, and the data signals that are associated to those strobe signals (e.g., SBA[7:0]), can be 6.075 inches to 6.325 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface; therefore special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 20 mils of space (1:4) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length matched to less than ± 0.1 inch (i.e., a strobe and its complement must be the same length within 0.1 inch).

7.1.3 AGP Interfaces Trace Length Summary

The 2X/4X Timing Domain Signals can be routed with 5 mil spacing when breaking out of the MCH. The routing must widen to the documented requirements within 0.3 inch of the MCH package.

When matching trace length for the AGP 4X interface, all traces should be matched from the ball of the MCH to the pin on the AGP connector. It is not necessary to compensate for the length of the AGP signals on the MCH package.

Reduce line length mismatch to insure added margin. To reduce trace-to-trace coupling (crosstalk), separate the traces as much as possible. All signals in a signal group should be routed on the same layer. The trace length and trace spacing requirements must not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to zero as possible to provide timing margin.

Table 24. AGP 2.0 Routing Summary

Signal	Maximum Length (Inches)	Trace Spacing (5 mil traces)	Length Mismatch (Inches)	Relative To
1X Timing Domain	7.5”	5 mils	No requirement	N/A
2X/4X Timing Domain Set #1	7.25”	20 mils [3]	± 0.125” [2]	AD_STB0 and AD_STB0#
2X/4X Timing Domain Set #2	7.25”	20 mils [3]	± 0.125” [2]	AD_STB1 and AD_STB1#
2X/4X Timing Domain Set #3	7.25”	20 mils [3]	± 0.125” [2]	SB_STB and SB_STB#
2X/4X Timing Domain Set #1	6”	15 mils [1,3]	± 0.25” [2]	AD_STB0 and AD_STB0#
2X/4X Timing Domain Set #2	6”	15 mils [1,3]	± 0.25” [2]	AD_STB1 and AD_STB1#
2X/4X Timing Domain Set #3	6”	15 mils [1,3]	± 0.25” [2]	SB_STB and SB_STB#
2X/4X Timing Domain Set #1	6”	20 mils [1,4]	± 0.25” [2]	AD_STB0 and AD_STB0#
2X/4X Timing Domain Set #2	6”	20 mils [1,4]	± 0.25” [2]	AD_STB1 and AD_STB1#
2X/4X Timing Domain Set #3	6”	20 mils [1,4]	± 0.25” [2]	SB_STB and SB_STB#

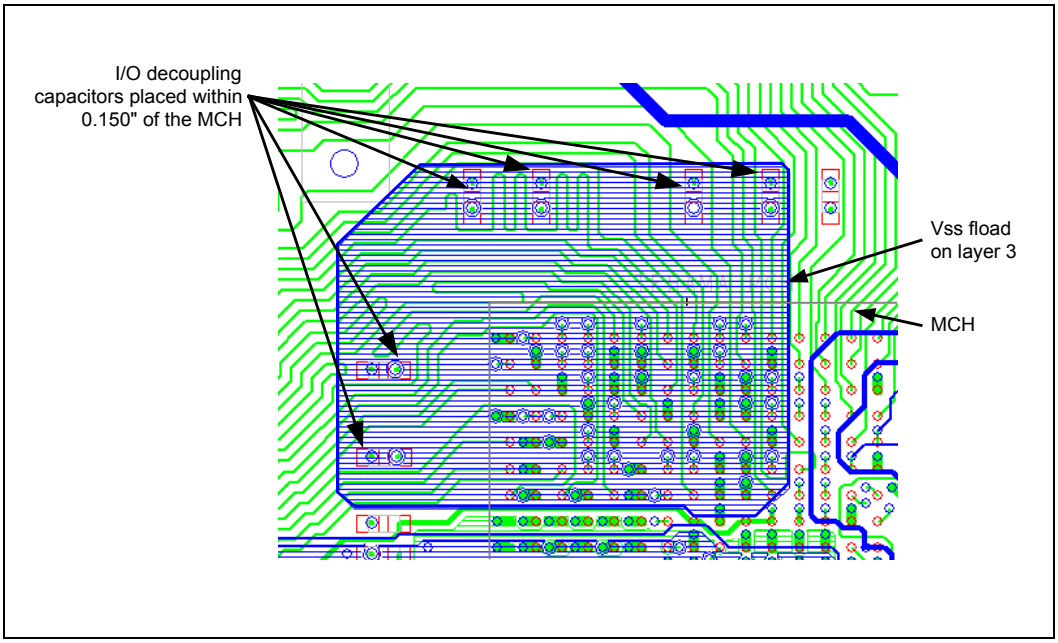
NOTES:
1. Each strobe pair must be separated from other signals by at least 20 mils.
2. Each strobe pair must be the same length.
3. These guidelines apply to board stack-ups with 10% impedance tolerance.
4. These guidelines apply to board stack-ups with 15% impedance tolerance

7.1.4 I/O Decoupling Guidelines

A minimum of six, 0.01 µF capacitors are required for I/O decoupling. The designer should evenly distribute placement of decoupling capacitors among the AGP interface signal field and should place them as close to the MCH as possible (no further than 0.15 inch from the edge of the MCH package). It is recommended that the designer use a low ESL ceramic capacitor, such as a 0603 body type, X7R dielectric.

To help lower the inductive path from the decoupling capacitor, pour a solid VSS plane under the VDDQ plane on layer 3 from the decoupling capacitors to the MCH. Figure 69 illustrates an example AGP decoupling layout with a VSS flood. This VSS flood that is referenced to VDDQ optimizes the mutual inductance between the two planes. The mutual inductance helps cancel out the self inductance from the power balls on the package to the decoupling caps.

Figure 69. AGP I/O Decoupling Example with a VSS Flood to Improve Power Delivery to the MCH



In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition AGP signal from one reference signal plane to another. One extra 0.01 µF capacitor is required per 10 vias. The capacitor should be placed as close to the center of the via field as possible.

The designer should ensure that the AGP connector is well decoupled as described in the *AGP Design Guide*, Revision 1.0.

7.1.5 Signal Power/Ground Referencing Recommendations

It is strongly recommended that, at a minimum, the following critical signals be referenced to ground from the MCH to an AGP connector utilizing a minimum number of vias on each net; AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_GTRY#, G_IRDY#, G_GNT#, and ST[2:0].

In addition to the preceding minimum signal set, it is strongly recommended that half of all the AGP signals be referenced to ground, depending on board layout. An ideal design would have the complete AGP interface signal field referenced to ground.

These recommendations are not specific to any particular PCB stack-up, but are applicable to all Intel chipset designs.

7.1.6 VDDQ and TYPEDET#

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller and is always 3.3 V. VDDQ is the interface voltage. The 82860 MCH supports only an interface voltage of 1.5 V.

The AGP 2.0 specification requires that VCC and VDDQ to be tied to separate power planes, and implements a TYPEDET# (type detect) signal on the AGP connector that determines the interface operating voltage (VDDQ). However, a motherboard based on the Intel 860 chipset supports only 1.5 V add-in cards. The 3 V add-in cards are not supported. Therefore, TYPEDET# detection on the motherboard is not required.

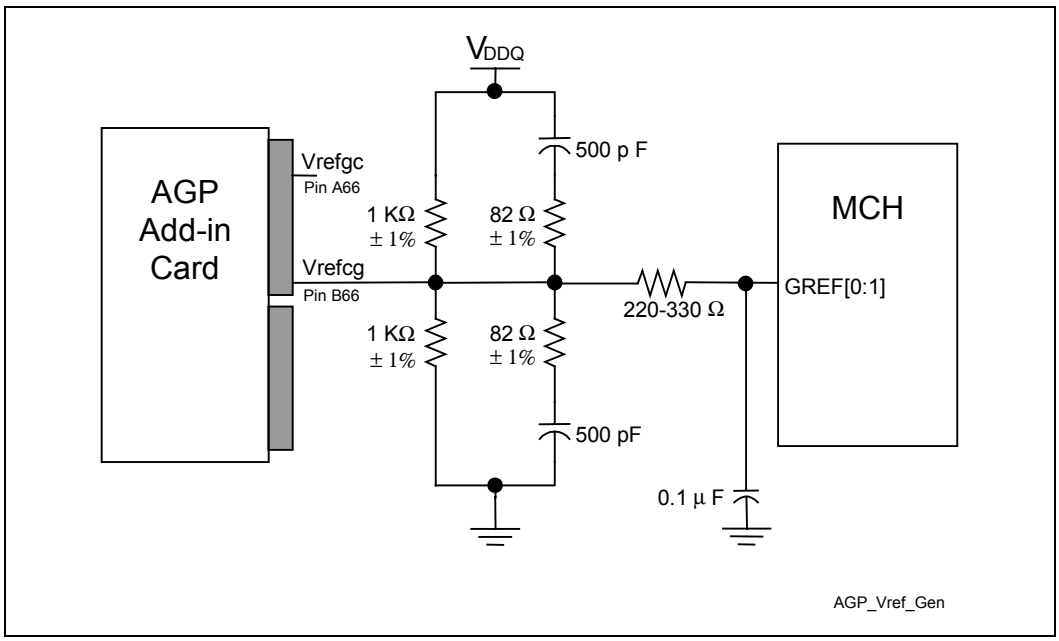
7.1.7 V_{REF} Generation

For 1.5 V add-in cards, both the graphics controller and MCH are required to generate V_{REF} and distribute it through the connector. Two signals have been defined on the 1.5 V connector to allow V_{REF} delivery:

- VREFGC – V_{REF} from the graphics controller to the chipset
- VREFCG – V_{REF} from the chipset to the graphics controller

However, use of the source generated V_{REF} at the MCH is not required by the *AGP Interface Specification*, Revision 2.0. Given this and the fact that the MCH requires the presence of V_{REF} when an AGP add-in card is either present or not present, the circuit in the following figure is recommended for V_{REF} generation.

Figure 70. AGP 2.0 V_{REF} Generation and Distribution for 1.5 V Cards



The V_{REF} divider network should be placed near the AGP interface. The minimum trace spacing around the V_{REF} signal must be 25 mils to reduce crosstalk and maintain signal integrity. Also, a 0.1µF bypass capacitor should be placed within 150 mils of the MCH GREF pins. The two GREF pins on the MCH (GREF[0:1]) should be tied together before connecting to the bypass capacitor. V_{REF} voltage must be 0.5 x VDDQ for 1.5 V operation.

7.1.8 MCH AGP Interface Buffer Compensation

The MCH AGP interface supports resistive buffer compensation (GRCOMP[1:0]). The GRCOMP[1:0] signals must be tied through a 40 Ω ± 2% or 39 Ω ± 1% pull-down resistor to ground. This trace should be 10 mils wide and less than 0.5 inch long.

7.1.9 AGP Pull-Ups/Pull-Downs on AGP Signals

Some of the AGP signals may require either a pull-up resistor to VDDQ (not VCC3.3), or a pull-down resistor to GND. This is to ensure that stable values are maintained when agents are not actively driving the bus. The recommended AGP pull-up/pull-down resistor value is 8.2 kΩ with 10% tolerance (4 kΩ ≤ R_{value} ≤ 16 kΩ). The AGP interface does not require external termination.

The trace stub length to the pull-up/pull-down resistor should be kept to a minimum to avoid signal reflection. This trace length is different for 1x and 2X/4X modes.

The following are the recommended stub lengths for 1x and 2X/4X modes.

- **1X mode:** trace stub to pull-up resistor should be less than 0.5 inch
- **2X/4X mode:** trace stub to pull-up resistor should be less than 0.1 inch

Short stub lengths help minimize signal reflections from the stub. The strobe signals require pull-ups/pull-downs on the motherboard to ensure stable values when there are no agents driving the bus.

Note: The G_GNT# and G_PAR signals require pull-ups to VDDQ.

The MCH G_GNT# output signal is tri-stated during RSTIN# assertion. This signal must have an external pull-up resistor to keep it from floating during the RSTIN# assertion. The recommended value is that same as for other AGP common clock signals.

The MCH G_PAR signal also requires an external pull-up resistor. This signal must have an external pull-up resistor to ensure that G_PAR remains at a valid logic level during AGP protocol transactions.

Table 25. AGP Pull-Up/Pull-Down Resistors

Signals	PU/PD Requirement
1x Timing Domain	
FRAME#	Pull-up resistor to VDDQ
TRDY#	Pull-up resistor to VDDQ
IRDY#	Pull-up resistor to VDDQ
DEVSEL#	Pull-up resistor to VDDQ
STOP#	Pull-up resistor to VDDQ
SERR#	Pull-up resistor to VDDQ
PERR#	Pull-up resistor to VDDQ
RBF#	Pull-up resistor to VDDQ
PIPE#	Pull-up resistor to VDDQ
REQ#	Pull-up resistor to VDDQ
GNT#	Pull-up resistor to VDDQ
WBF#	Pull-up resistor to VDDQ
PAR	Pull-up resistor to VDDQ
INTA#	Pull-up resistor to 3.3 V
INTB#	Pull-up resistor to 3.3 V
2X/4X Timing Domain	
AD_STB[1:0]	Pull-up resistor to VDDQ
SB_STB	Pull-up resistor to VDDQ
AD_STB[1:0]#	Pull-down resistor to GND
SB_STB#	Pull-down resistor to GND

7.1.10 AGP Signal Voltage Tolerance List

The following table describes 3.3 V tolerant signals and 5 V tolerant signals on the AGP interface (refer to the AGP Specification for more details). No other signals in the VDDQ group are 3.3 V tolerant during 1.5 V AGP operation.

Table 26. 3.3 V and 5 V Tolerant Signals During 1.5 V Operation

3.3 V Tolerant Signals	5 V Tolerant Signals
PME#	USB+
INTA#	USB-
INTB#	OVRCNT#
PERR#	
SERR#	
CLK	
RST	

7.1.11 AGP Connector

Only 1.5 V add-in cards are supported. The 1.5 V uses the AGP 3 V connector and rotates it 180 degrees on the planar. Therefore, the key of the connector moves to the opposite side of the planar away from the I/O panel and does not allow 3 V add-in cards.

The designer should ensure that the AGP connector is well decoupled as described in the *AGP Design Guide Revision 1.0* (i.e., use a 0.01 µF capacitor for each power pin and a bulk 10 µF tantalum capacitor on VDDQ and 20 µF tantalum capacitor on VCC3.3 plane near the connector.).

7.2 AGP Universal Retention Mechanism (RM)

Environmental testing and field reports indicate that AGP cards and AGP In Line Memory Module (AIMM) cards may become unseated during system shipping and handling without proper retention. To avoid disengaged AGP cards and AIMM modules, Intel recommends that AGP based platforms use the AGP retention mechanism (RM).

The AGP RM is a mounting bracket that is used to properly locate the card with respect to the chassis, and to assist with card retention. The AGP RM is available in two different handle orientations — left-handed and right-handed (see Figure 71). Most system boards accommodate the left-handed AGP RM. The manufacturing capacity of the left-handed RM currently exceeds the right-handed capacity, and as a result Intel recommends that customers design their systems to insure they can use the left-handed version of the AGP RM (see Figure 72). The right-handed AGP RM is identical to the left-handed AGP RM except for the position of the actuation handle. This handle is located on the same end as the primary design, but extends from the opposite side (mirrored about the center axis running parallel to the length of the part). Figure 72 contains keepout information for the left hand AGP retention mechanism. Use this information to make sure that your motherboard design leaves adequate space to install the retention mechanism.

The AGP interconnect design requires that the AGP card must be retained to the extent that the card not back out more than 0.99 mm (0.039 in) within the AGP connector. To accomplish this it is recommended that new cards implement an additional notch feature in the mechanical keying tab to allow an anchor point on the AGP card for interfacing with an AGP RM. The retention mechanism's round peg engages with the AGP or AIMM card's retention tab and prevents the card from disengaging during dynamic loading. The additional notch feature in the mechanical keying tab is required for 1.5 V AGP cards and is recommended for the new 3.3 V AGP cards.

Figure 71. AGP Left-Handed Retention Mechanism Drawing

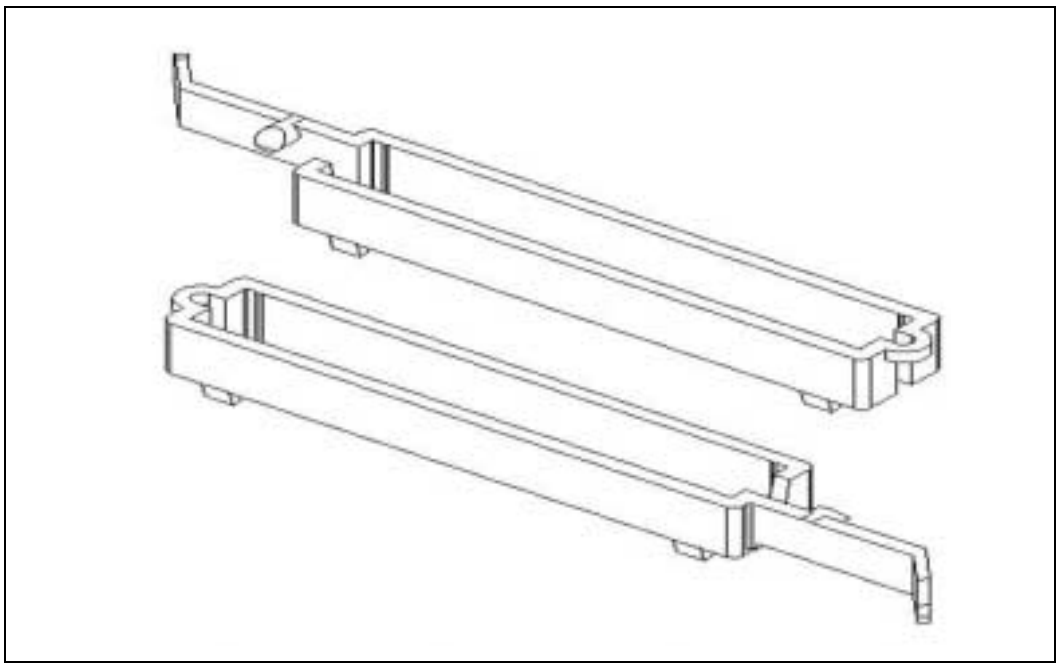
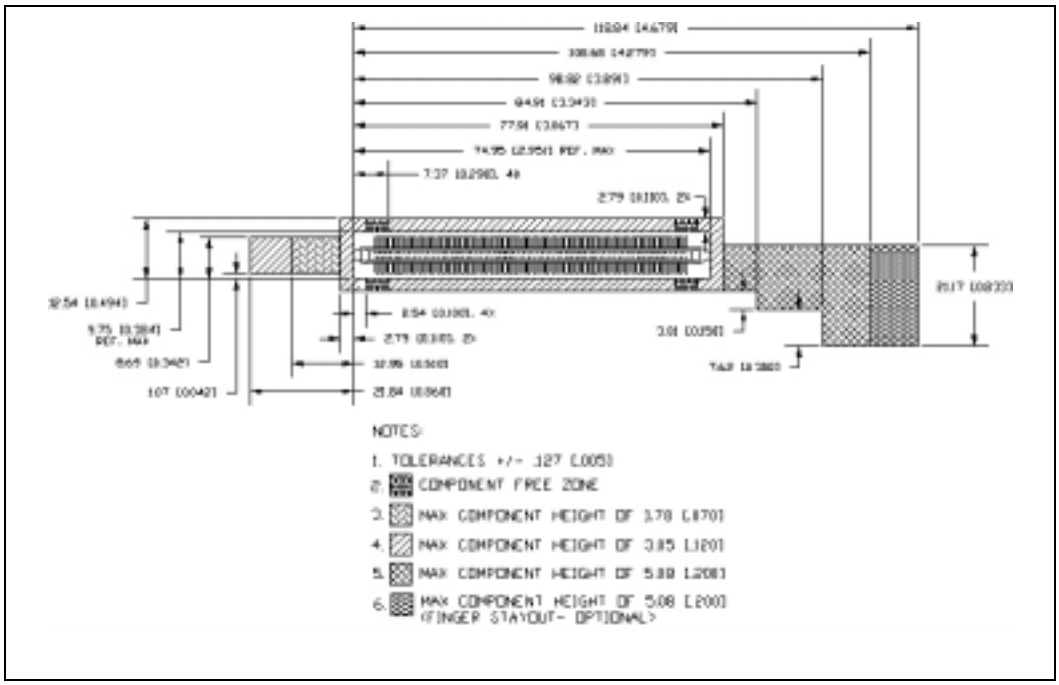


Figure 72. AGP Left-Handed Retention Mechanism Keepout Information



Engineering Change Request number 48 (ECR #48) of the AGP specification details the AGP RM, which is recommended for all AGP cards. These are approved changes to the *Accelerated Graphics Port (AGP) Interface Specification*, Revision 2.0. Intel intends to incorporate the AGP RM changes into later revisions of the AGP Interface Specification. In addition, Intel has defined a reference design of a mechanical device to utilize the features defined in ECR #48.

ECR #48 can be viewed at the Intel Web site

http://developer.intel.com/technology/agp/ecr.htm.

More information regarding this component (AGP RM) is available from the vendors listed in the following table.

Table 27. List of Vendors for Retention Mechanism

Resin Color	Supplier Part Number	"Left Handed" Orientation (Preferred)	"Right Handed" Orientation (Alternate)
Black	AMP P/N	136427-1	136427-2
	Foxconn P/N	006-0002-939	006-0001-939
Green	Foxconn P/N	009-0004-008	009-0003-008

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8 Hub Interface

The MCH, ICH2, and P64H ballout assignments have been optimized to simplify the hub interface routing between these devices. It is recommended that the hub interface signals be routed directly from the MCH to the ICH2, and from the MCH to the P64H with all signals referenced to VSS. Layer transition should be kept to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signal on the same layer.

The hub interface signals are divided into two groups: data signals (HL) and strobe signals (HL_STB). For the 8-bit hub interface, HL[0:7] is associated with HL_STB and HL_STB#. For the 16-bit hub interface, HL[0:7] is associated with HL_STB0 and HL_STB0#, and HL[8:15] are associated with HL_STB1 and HL_STB1#.

Figure 73. 8-Bit Hub Interface Routing Example

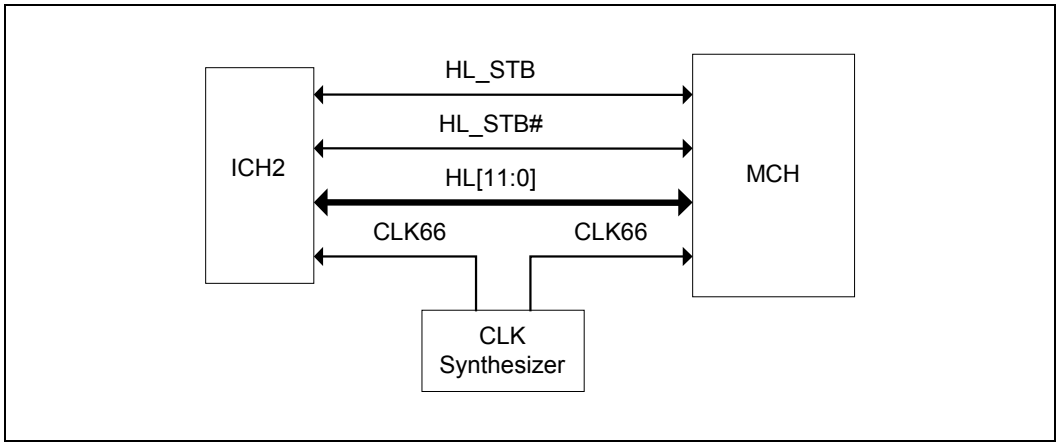
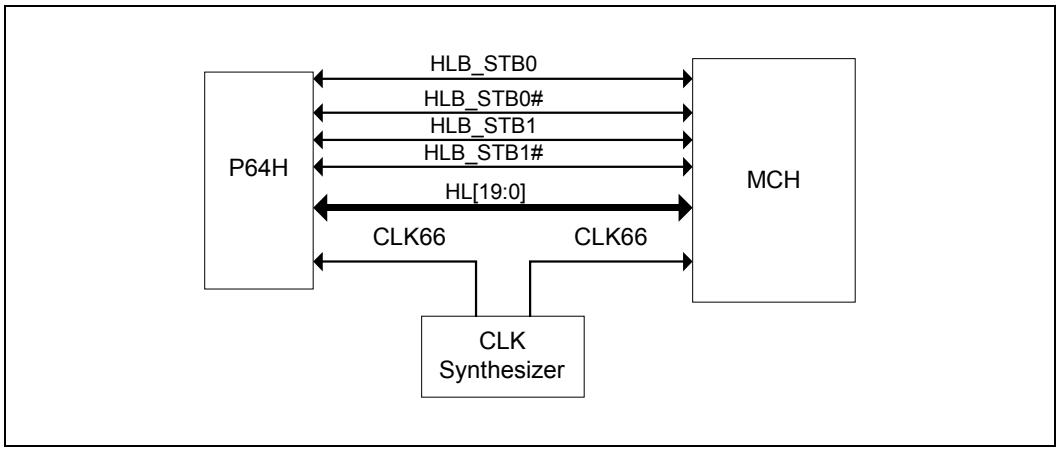


Figure 74. 16-Bit Hub Interface Routing Example

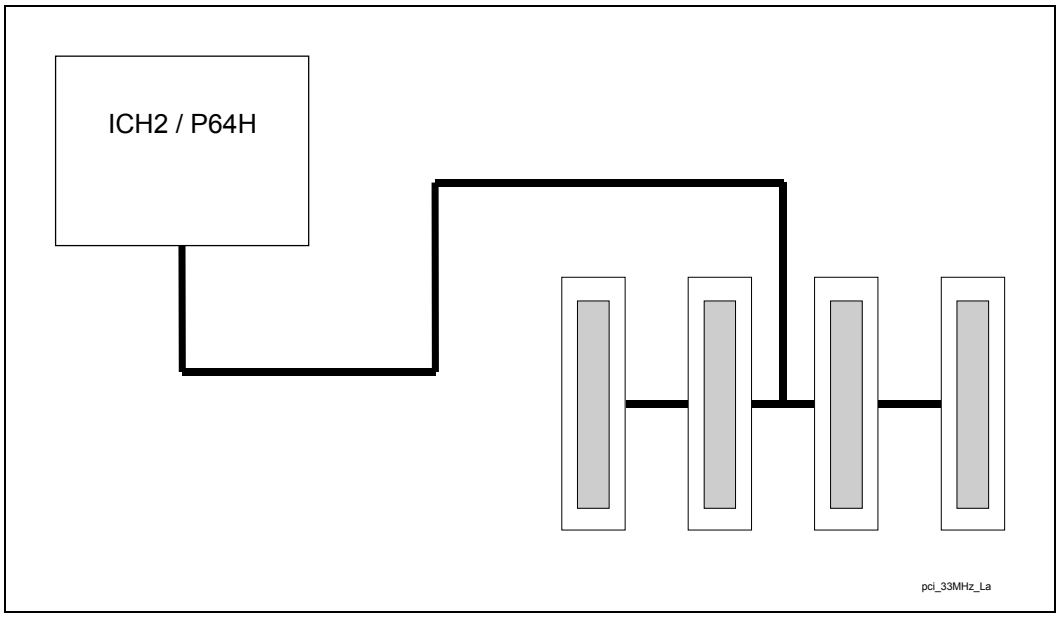


The Intel 860 chipset offers support for both 33 MHz and 66 MHz PCI operations. The ICH2 supports 33 MHz, while the P64H supports both 33 MHz and 66 MHz PCI operations. The ICH2 and P64H each provide 6 pairs of REQ#/GNT# signals that support 6 PCI masters. In addition, the ICH2 supports 2 PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

8.1 PCI 33 MHz Guidelines

The ICH2 and P64H both provide PCI Bus interfaces that are compliant with the *PCI Local Bus Specification, Revision 2.2*. Their implementation is optimized for high-performance data streaming when either ICH2 or P64H is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

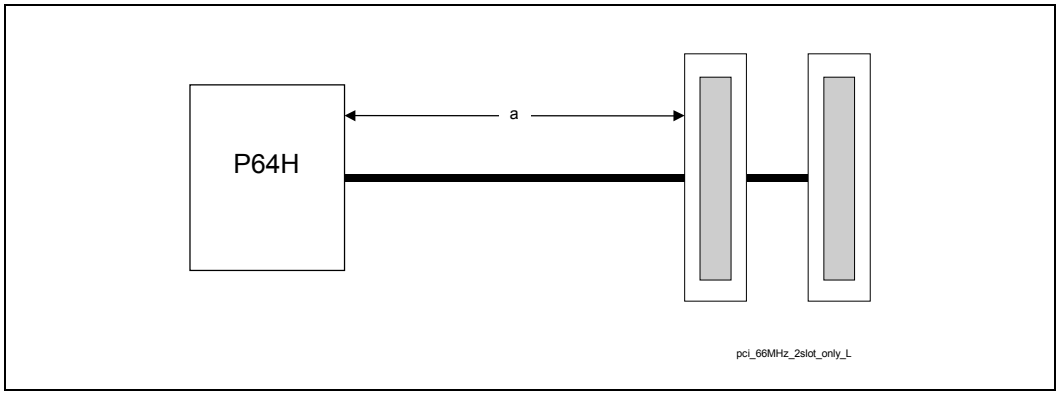
Figure 75. PCI 33 MHz Bus Layout Example



8.2 PCI 66 MHz Guidelines

The P64H provides a PCI Bus interface that is compliant with *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the P64H is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

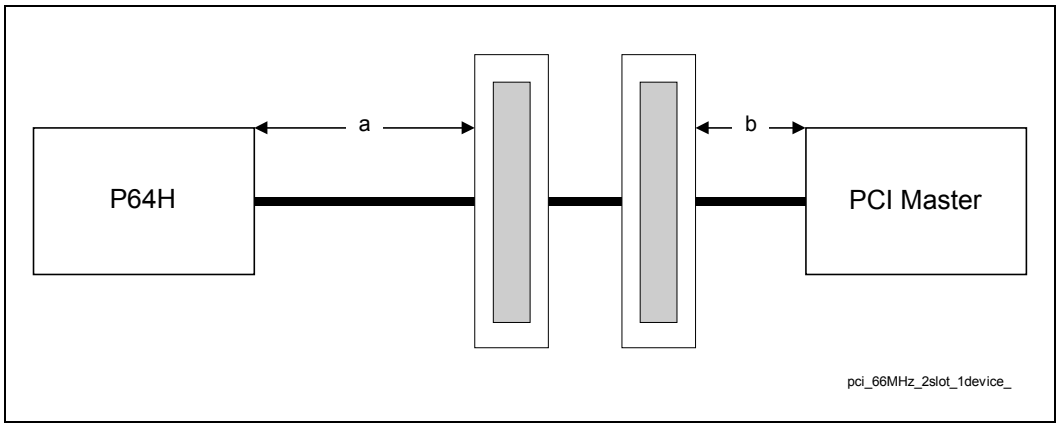
Figure 76. PCI 66 MHz — 2 Slots Only



All of the PCI 66 MHz signals can be routed using 5 mil traces with 7 mil spacing between the traces. The following guidelines apply to the previous figure:

- (a) P64H to 1st 66 MHz slot connector length: a ≤ 13 inches
- The typical spacing between PCI connectors is 0.8 inch

Figure 77. PCI 66 MHz—2 Slots with 1 Device Down



All of the PCI 66 MHz signals can be routed using 5 mil traces with 7 mil spacing between the traces. The following guidelines apply to the previous figure:

- (a) P64H to 1st 66 MHz slot connector length: 0 inch ≤ a ≤ 6 inches
- (b) 2nd 66 MHz slot to PCI device down length: 1 inch ≤ b ≤ 5 inches
- The typical spacing between PCI connectors is 0.8 inch

8.3 8-Bit Hub Interface Routing Guidelines

This section documents the routing guidelines for the 8-bit hub interface. This hub interface connects the ICH2 to the MCH. This interface supports two buffer modes: normal and enhanced. The ICH2 uses its HLCOMP pin to set the buffer mode, and the MCH uses its HLA_ENH# pin to configure its 8-bit hub interface buffers. Both devices must be configured for the same buffer mode.

When the buffers are configured for normal mode, the trace impedance must equal 60 Ω ± 15%. In the enhanced buffer mode, the trace impedance can be 50 Ω ± 10%, or 60 Ω ± 15%.

Table 28. 8-Bit Hub Interface Buffer Configuration Setting

Component	Hub Interface Buffer Mode	Trace Impedance	Strap
ICH2	Normal	60 Ω	HLCOMP pulled to VCC1.8(1)
	Enhanced	50 or 60 Ω	HLCOMP pulled to GND(1)
MCH	Normal	60 Ω	Default
	Enhanced	50 or 60 Ω	HLA_ENH# pulled to GND via a 100 Ω resistor

NOTE: [1]Refer to Section 8.3.4 for the specific resistor value.

8.3.1 8-Bit Hub Interface Data Signals

The 8-bit hub interface data signal traces should be routed 5 mils wide with 20 mils trace spacing (5 on 20). These signals can be routed 5 on 15 for navigation around components or mounting holes. To break out of the MCH and ICH2 package, the hub interface data signals can be routed 5 on 5. The signal must be separated to 5 on 20 within 300 mils of the package.

The maximum hub interface data signal trace length is 6 inches in normal buffer mode, and 14 inches in enhanced mode. Each data signal must be matched within ±0.1 inch of the HL_STB differential pair. There is no explicit matching requirement between the individual data signals.

8.3.2 8-Bit Hub Interface Strobe Signals

The hub interface strobe signals should be routed 5 mils wide with 20 mils trace spacing (5 on 20). This strobe pair should have a minimum of 20 mils spacing from any adjacent signals. The maximum length for the strobe signal in normal mode is 6 inches, and 14 inches in enhanced mode. Each strobe signal must be the same length, and each data signal must be matched within ±0.1 inch of the strobe signals.

8.3.3 8-Bit Hub Interface HIREF Generation/Distribution

HIREF is the hub interface reference voltage. Depending on the buffer mode (i.e., normal or enhanced buffer mode), the HIREF voltage requirement must be set appropriately for proper operation. See the following table for the HIREF voltage specifications for normal and enhanced buffer modes, and for the associated resistor recommendations for the voltage divider circuit.

Table 29. 8-Bit Hub Interface HIREF Generation Circuit Specifications

Buffer Mode	HIREF Voltage Specification (V)	Recommend Resistor Values for the HIREF Divider Circuit (Ohms)
Normal	1/2 VCC1.8 ± 2%	R1 = R2 = 150 ± 1%
Enhanced	2/3 VCC1.8 ± 2%	R1 = 150 ± 1%, R2 = 301 ± 1%

The single HIREF divider should not be located more than 3.5 inches away from either MCH or ICH2. If the single HIREF divider is located more than 3.5 inches away, the locally generated hub interface reference dividers should be used instead. The reference voltage generated by a single HIREF divider should be bypassed to ground at each component with a 0.01 µF capacitor (C2) located close to the component HUBREF pin. If the reference voltage is generated locally, the bypass capacitor must be close to the component HUBREF pin. See the following figures for example HIREF divider circuits.

Figure 78. 8-Bit Hub Interface with a Single Reference Divider Circuit (Normal Mode)

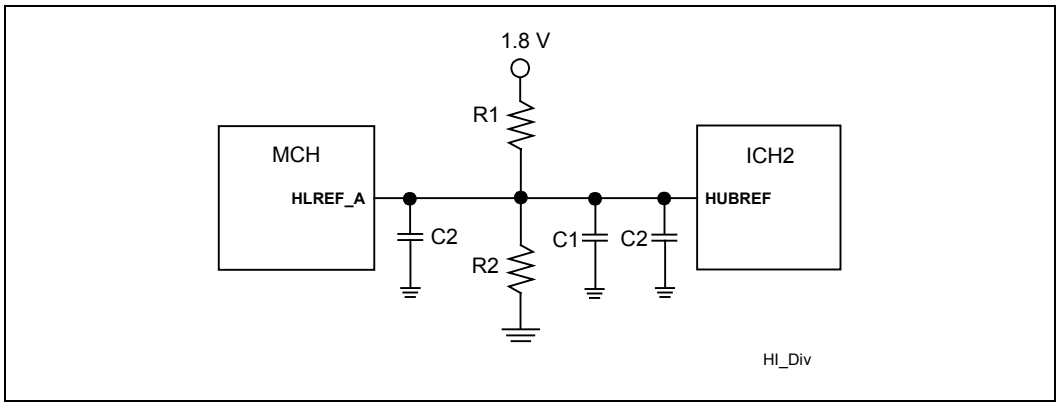


Figure 79. 8-Bit Hub Interface with Locally Generated Reference Divider Circuits (Normal)

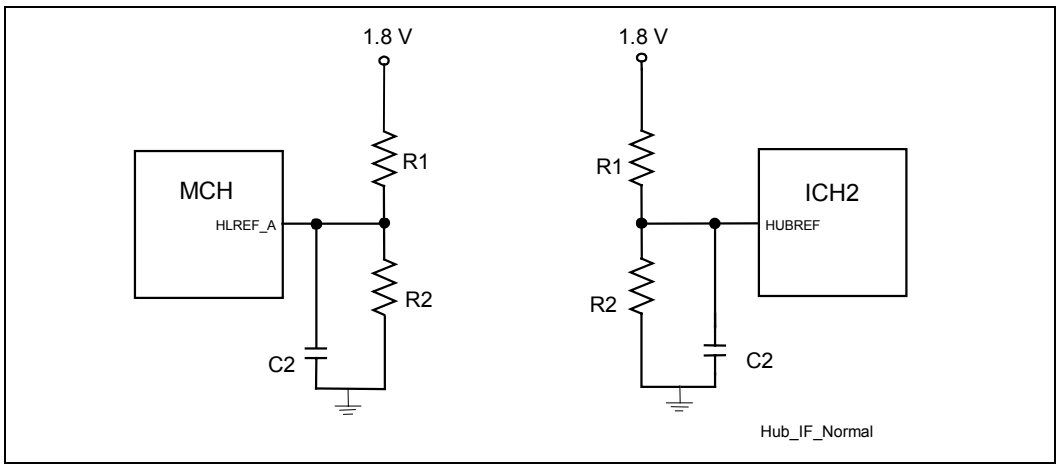
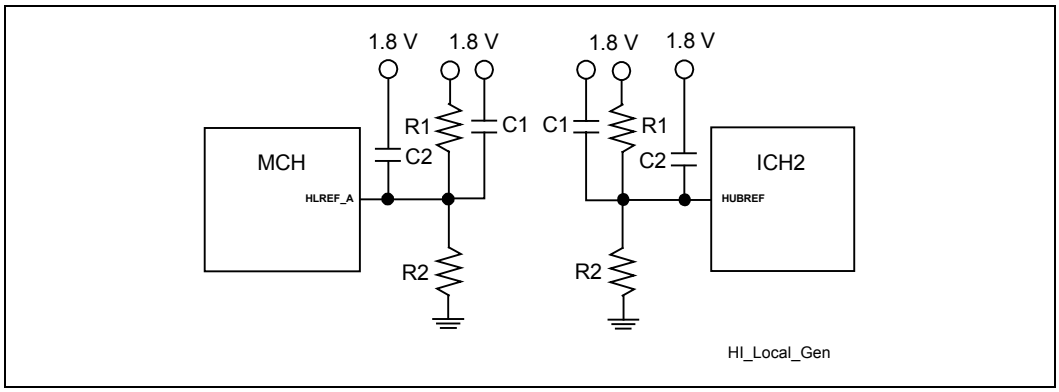


Figure 80. 8-Bit Hub Interface with Locally Generated Reference Divider Circuits (Enhanced Mode)



The resistor values, R1 & R2, must be rated at 1% tolerance. These selected resistor values must ensure that the reference voltage tolerance is maintained over the input leakage specification. A 0.1 µF capacitor (C1 in the previous figure) should be placed close to R1 and R2. Also, a 0.01 µF bypass capacitor (C2 in the previous figure) should be placed near each HUBREF pin. The trace length from the divider circuit to the HLREF pin must be no longer than 3.5 inches.

8.3.4 8-Bit Hub Interface Compensation

The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The hub interface requires Resistive Compensation (RCOMP).

Table 30. 8-Bit Hub Interface RCOMP Resistor Values

Component	Hub Interface Buffer Mode	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Connection
ICH2	Normal	60 Ω ± 15%	40 Ω ± 2% or 39 Ω ± 1%	VCC1.8
	Enhanced	60 Ω ± 15%	30 Ω ± 1%	VSS
		50 Ω ± 10%	25 Ω ± 1%	VSS
MCH	Normal	60 Ω ± 15%	40 Ω ± 2% or 39 Ω ± 1%	VSS
	Enhanced	60 Ω ± 15%	30 Ω ± 1%	VSS
		50 Ω ± 10%	25 Ω ± 1%	VSS

8.3.5 8-Bit Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1 µF capacitors for each component (i.e., the ICH2 and MCH). These capacitors should be placed within 150 mils from each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1.8 side of the capacitors to the VCC1.8 power pins. Similarly, if layout allows, metal fingers running on the VCC1.8 side of the board should connect the ground side of the capacitors to the VSS power pins.

8.4 16-Bit Hub Interface Routing Guidelines

This section describes the routing guidelines for the 16-bit hub interface. This hub interface connects the P64H to the MCH. This interface only supports the enhanced buffer mode. Trace impedance can be 50 Ω ± 10% or 60 Ω ± 15%. Both the HUBREF and HSWING signals should be routed 20–25 mils from all other signals.

8.4.1 16-Bit Hub Interface Data Signals

The 16-bit hub interface data signal traces should be routed 5 mil wide with 20 mil trace spacing (5-on-20). These signals can be routed 5-on-15 for navigation around components or mounting holes. To break out of the MCH and P64H package, the hub interface data signals can be routed 5-on-5. The signal must be separated to 5-on-20 within 300 mil of the package.

The 16-bit hub interface has minimum and maximum requirements. The maximum hub interface signals trace length is 14 inches. Each data signal must be matched within ±0.1 inch of the HL_STB[1:0] differential pairs. There is no length match requirement between the data signals.

8.4.2 16-Bit Hub Interface Strobe Signals

The hub interface strobe signals should be routed 5 mil wide with 20 mil trace spacing (5 on 20). This strobe pair should have a minimum of 20 mil spacing from any adjacent signals. The maximum length for the strobe signals is 14 inches, and all of the strobe signals must be the same length. Each data signal must be matched within ±0.1 inch of the HL_STB[1:0] differential pairs.

8.4.3 16-Bit Hub Interface HIREF Generation/Distribution

HIREF is the hub interface reference voltage and should be 2/3 VCC1.8 ± 2%. This reference voltage can be generated locally or with a single HIREF divider circuit. Example HIREF divider circuits are shown in the following figures.

Table 31. 16-Bit Hub Interface HUBREF Generation Circuit Specifications

Buffer Mode	HIREF Voltage Specification (V)	Recommend Resistor Values for the HIREF Divider Circuit (Ohms)
Enhanced	2/3 VCC1.8 ± 2%	R1 = 150 Ω ± 1%, R2 = 301 Ω ± 1%

Figure 81. 16-Bit Hub Interface with a Shared Reference Divider Circuit

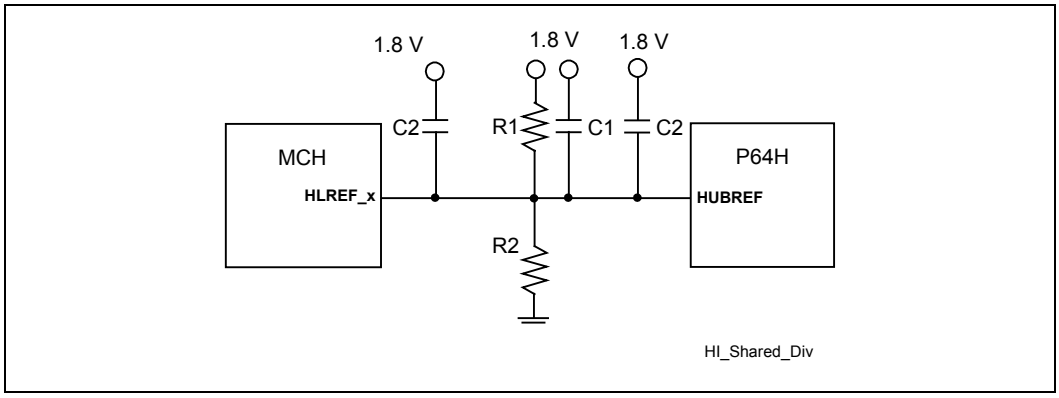
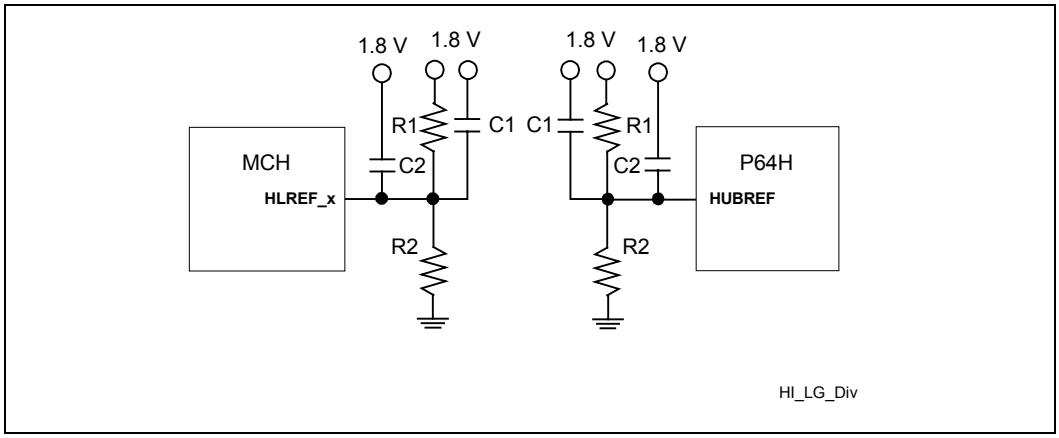


Figure 82. 16-Bit Hub Interface with Locally Generated Reference Divider Circuits



The resistor values, R1 & R2, must be rated at 1% tolerance. These selected resistor values must also ensure that the reference voltage tolerance is maintained over the input leakage specification. A 0.1 µF capacitor (C1 in the previous figures) should be placed close to R1 and R2. Also, a 0.01 µF bypass capacitor (C2 in the previous figures) should be placed near each HUBREF pin. If the length of the trace from voltage divider to the HUBREF pin is greater than 1 inch, place more than one 0.01 µF capacitor near the HUBREF pin. The trace length from the divider circuit to the HLREF pin must be no longer than 3.5 inches.

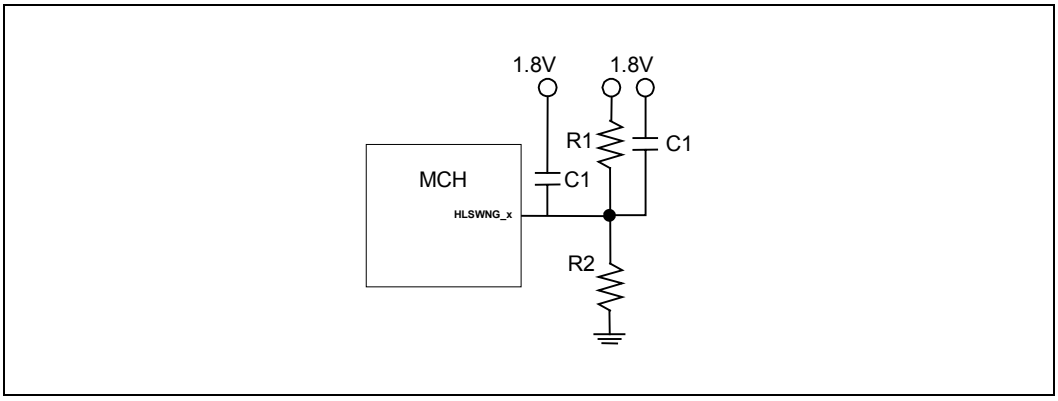
8.4.4 16-Bit Hub Interface Compensation Reference Voltage Generation/Distribution

The MCH 16-bit hub interfaces use a compensation voltage to control the buffer voltage characteristics. Each 16-bit hub interface on the MCH has a dedicated HLSWNG pin. This reference voltage can be implemented using a simple voltage divider circuit.

Table 32. 16-Bit Hub Interface HLSWNG Generation Circuit Specifications

HLSWNG Voltage Specification (V)	Recommend Resistor Value for the HUBREF Divider Circuit
1/3 VCC1.8 ± 2%	R1 = 301 Ω ± 1%, R2 = 150 Ω ± 1%

Figure 83. MCH 16-Bit Hub Interface HLSWNG Generated Reference Divider Circuit



The resistor values, R1 & R2, must be rated at 1% tolerance. The selected resistor values that the reference voltage tolerance is maintained over the input leakage specification. A 0.1 µF capacitor (C1 in the previous figure) should be placed close to R1 and R2. Also, a 0.01 µF bypass capacitor (C2 in the previous figure) should be placed within 0.5 inches each HLSWNG pin. The trace length from the divider circuit to the HLSWNG pin must be no longer than 3.5 inches.

If multiple 16-bit hub interfaces are used, a HLSWNG divider circuit can be shared among the interfaces as long as the trace length from the divider circuit is less than 3.5 inches.

8.4.5 16-Bit Hub Interface Resistive Compensation

The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The hub interface requires Resistive Compensation (RCOMP).

Table 33. 16-Bit Hub Interface RCOMP Resistor Values

Component	Hub Interface Buffer Mode	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Connection
P64H	Enhanced	60 Ω ± 15%	30 Ω ± 1%	VSS
		50 Ω ± 10%	25 Ω ± 1%	VSS
MCH	Enhanced	60 Ω ± 15%	30 Ω ± 1%	VSS
		50 Ω ± 10%	25 Ω ± 1%	VSS

8.4.6 16-Bit Hub Interface Decoupling Guidelines

To improve I/O power delivery, use three 0.1 µF capacitors per each component (i.e., the P64H and MCH). These capacitors should be placed as close as possible to each package, within a maximum of 150 mils, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1.8 side of the capacitors to the VCC1.8 power pins. Similarly, if layout allows, metal fingers running on the VCC1.8 side of the board should connect the ground side of the capacitors to the VSS power pins.

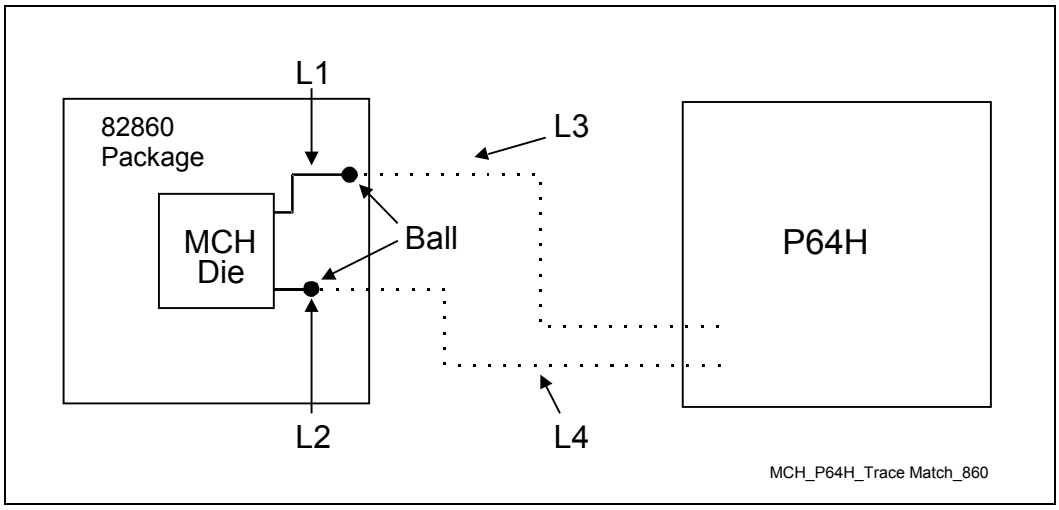
8.4.7 16-Bit Trace Length Compensation

To allow for greater routing flexibility, the 16-bit hub interface signals require trace length matching between the MCH pads and the P64H balls:

1. Match the trace lengths between the MCH balls and the P64H balls.
2. Match the trace lengths between the MCH balls and pads.

All 16-bit interface signals are required to have matching trace lengths from pad-to-pin within ±10 mils.

Figure 84. Trace Length Matching Example from MCH to Intel® P64H



Listed below are a few definitions.

- Package Dimension (ΔL_{PKG}): a representation of the length from the pad to the ball.
- Board Trace Length (L_{MB}): the trace length on the board.
- Nominal 16–bit Hub Interface Length: the length to which all signals are matched. The Nominal 16–bit Hub Interface Length is an arbitrary length to which all the 16–bit signals will be matched (within 10 mils).

As Figure 84 shows, L1 and L3 must be length matched to L2 and L4 within ±10 mils.

Equation 10. Compensated Trace Length Calculation

$$\Delta L_{PCB} = (\Delta L_{PKG} * \text{Package}_{\text{TRACE VELOCITY}}) / PCB_{\text{TRACE VELOCITY}}$$

The PCB trace length for each signal is a calculated value, and may vary with designs. The actual package trace velocity is between 177 ps/in and 183 ps/in. The nominal trace velocity of 180 ps/in can be used when calculating the compensated PCB trace length. The $PCB_{\text{TRACE VELOCITY}}$ is board dependent.

8.4.8 Unused 16-Bit Hub Interfaces

The recommended termination for unused 16-bit hub interfaces is as follows:

- All hub interface data and strobe signals can be left as no connects. The MCH has integrated detection logic that detects un-populated 16-bit interfaces without external pull-ups or pull-downs.
- HLREF must remain connected to the HUBREF voltage divider as shown in Figure 82
- HLSWNG must be connected to VCC1.8.

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9 I/O Controller Hub 2 (Intel® ICH2)

9.1 IDE Interface

This section contains guidelines for connecting and routing the ICH2 IDE interface. The ICH2 has two independent IDE channels. This section provides guidelines for IDE connector cabling and system board design, including component and resistor placement, and signal termination for both IDE channels. The ICH2 has integrated series resistors that have been typically required on the IDE data signals (PDD [15:0] and SDD [15:0]) running to the two ATA connectors. We do not anticipate requiring additional series termination, but OEMs should verify system board signal integrity through simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the system board. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface must be routed with 5 mil traces on 10 mil spaces, and with a maximum trace length of 8 inches long (from ICH2 to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 0.5 inch shorter than the longest IDE signal (on that channel).

9.1.1 IDE Cable

The IDE cabling specifications and requirements are as follows:

- Length of cable: Each IDE cable must be equal to or less than 18 inches.
- Capacitance: Less than 30 pF.
- Placement: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).
- Grounding: Provide a direct low impedance chassis path between the system board ground and hard disk drives.
- ICH2 Placement: The maximum trace length from the ICH2 to the ATA connector(s) is 8 inches.
- PC ’99 requirement: Support Cable Select for master-slave configuration is a system design requirement for Microsoft PC99. The CSEL signal of each ATA connector must be grounded at the host side.

9.1.2 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH2 IDE Controller supports PIO, Multi-word (8237 style) DMA, and Ultra DMA modes 0 through 5. The ICH2 needs to determine the type of cable that is present, in order to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra ATA/66 and Ultra ATA/100. This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

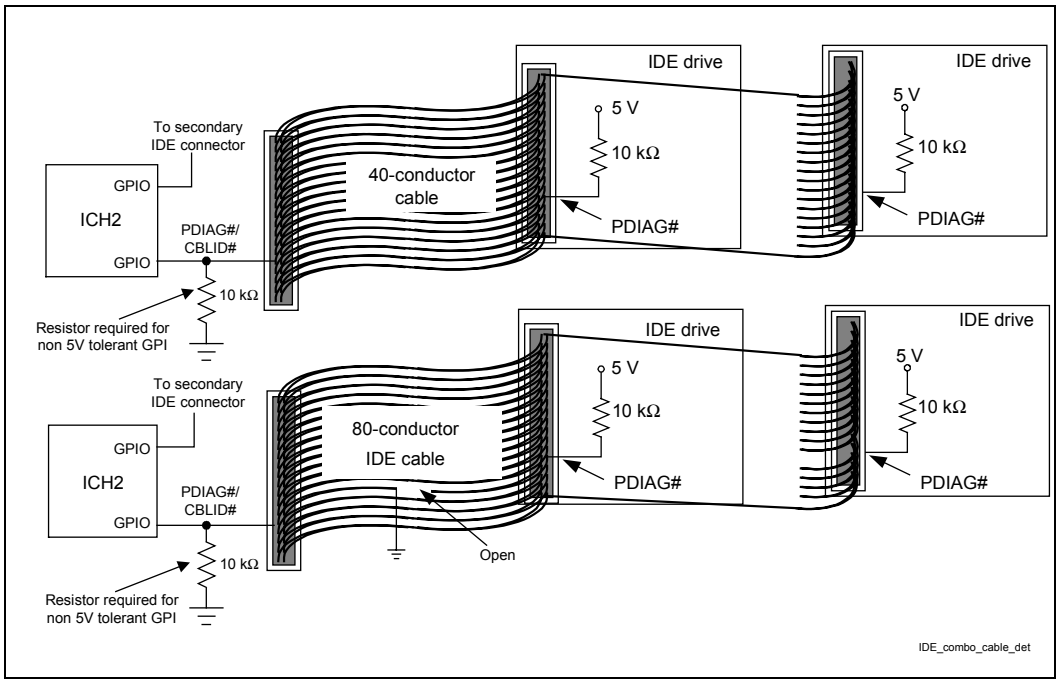
To determine if ATA/66 or ATA/100 mode can be enabled, the ICH2 requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be done using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system, since this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side detection mechanism only.

9.1.2.1 Host/Device-Side Detection

Host-Side detection requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 85. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. Not all of the GPI and GPIO pins on the ICH2 are 5 V tolerant. If non-5 V tolerant inputs are used, a resistor divider is required to prevent 5 V on the ICH2 or FWH pins. The proper value of the divider resistor is 10 kΩ (as shown in Figure 85).

Figure 85. Host/Device-Side Detection Layout



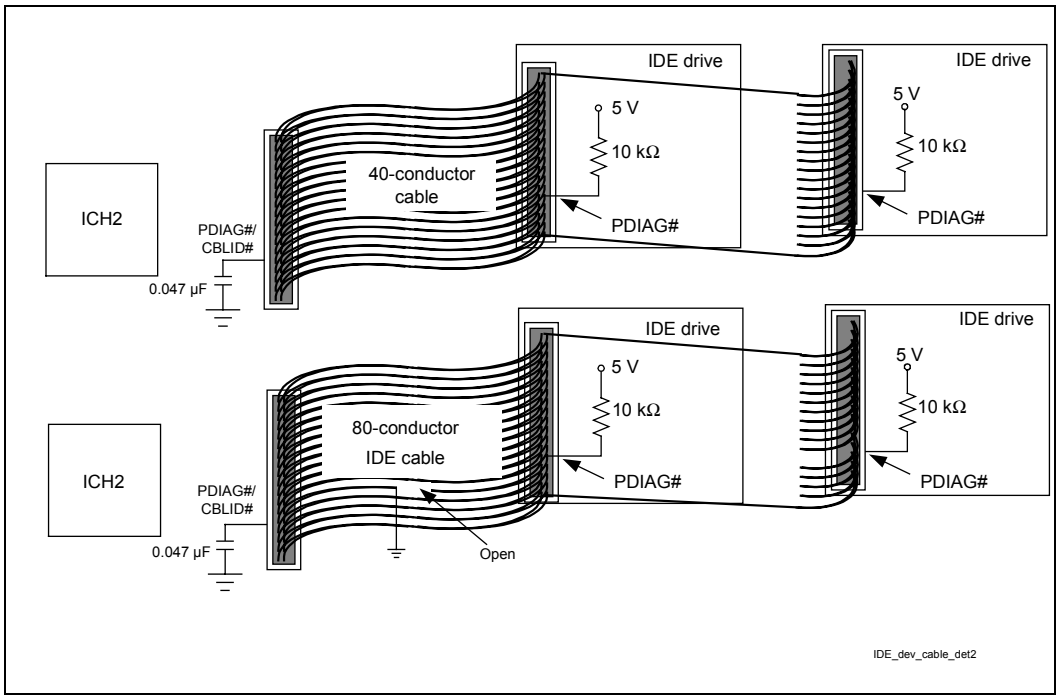
This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high then there is 40-conductor cable in the system and ATA modes 3, 4 and 5 must not be enabled.

If PDIAG#/CBLID# is detected low, then there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-4 standard. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13 is 1, then an 80-conductor cable is present. If this bit is 0, then a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present, and notify the user of the problem.

9.1.2.2 Device-Side Cable Detection

For platforms that must implement Device-Side detection **only** (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in Figure 86. This capacitor **should not** be populated when implementing the recommended combination Host-Side/Device-Side cable detection mechanism described above.

Figure 86. Device-Side Only Cable Detection

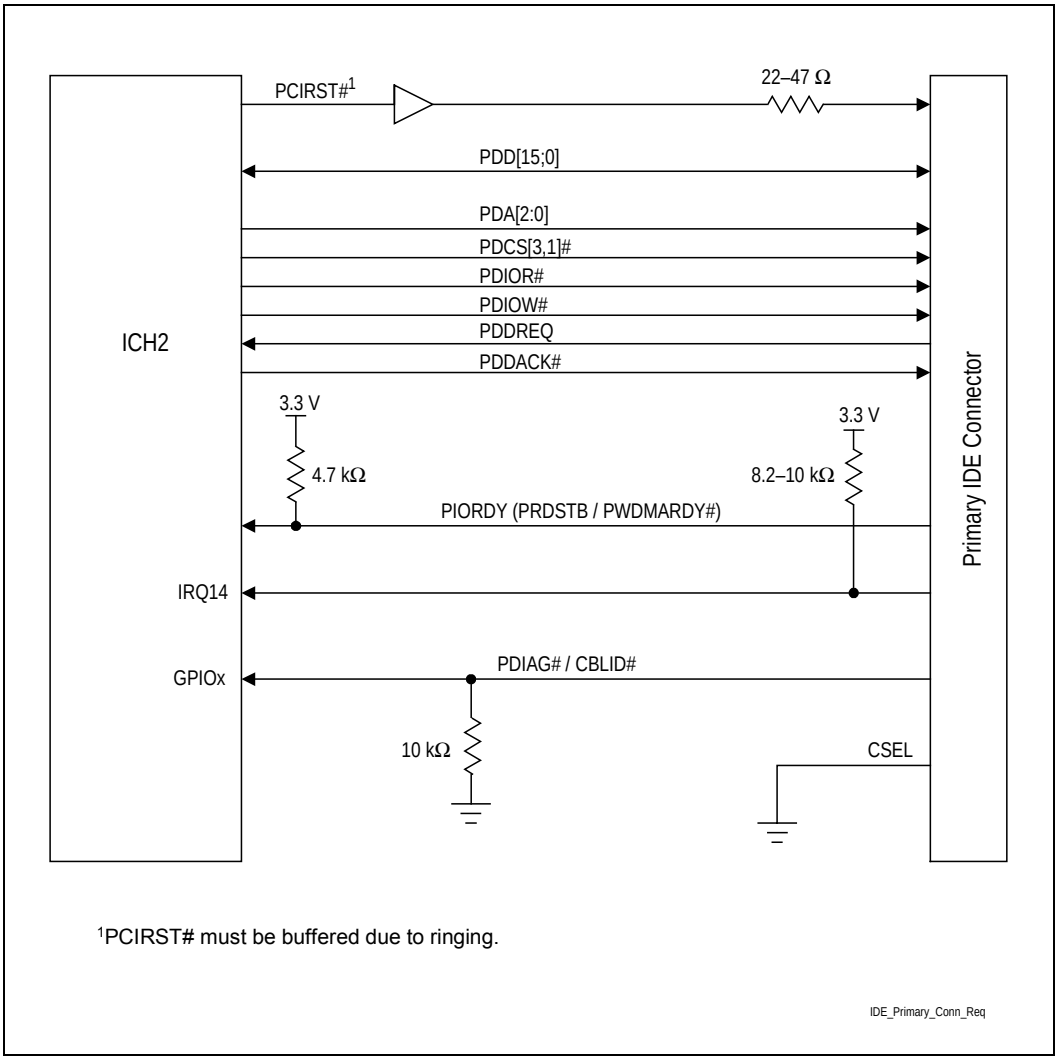


This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3, 4, or 5 drive will drive PDIAG#/CBLID# low and then release it (pulled up through a 10 kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host; therefore, the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host. Therefore, the signal will rise more slowly, as the capacitor charges. The drive can detect the difference in rise times and it will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the *ATA/66 Specification*.

9.1.3 Primary IDE Connector Requirements

The 10 kΩ resistor to ground on the PDIAG/CBLID signal is now required on both the primary and secondary connectors. This change is to prevent the GPI pin from floating if a device is not present on either IDE interface.

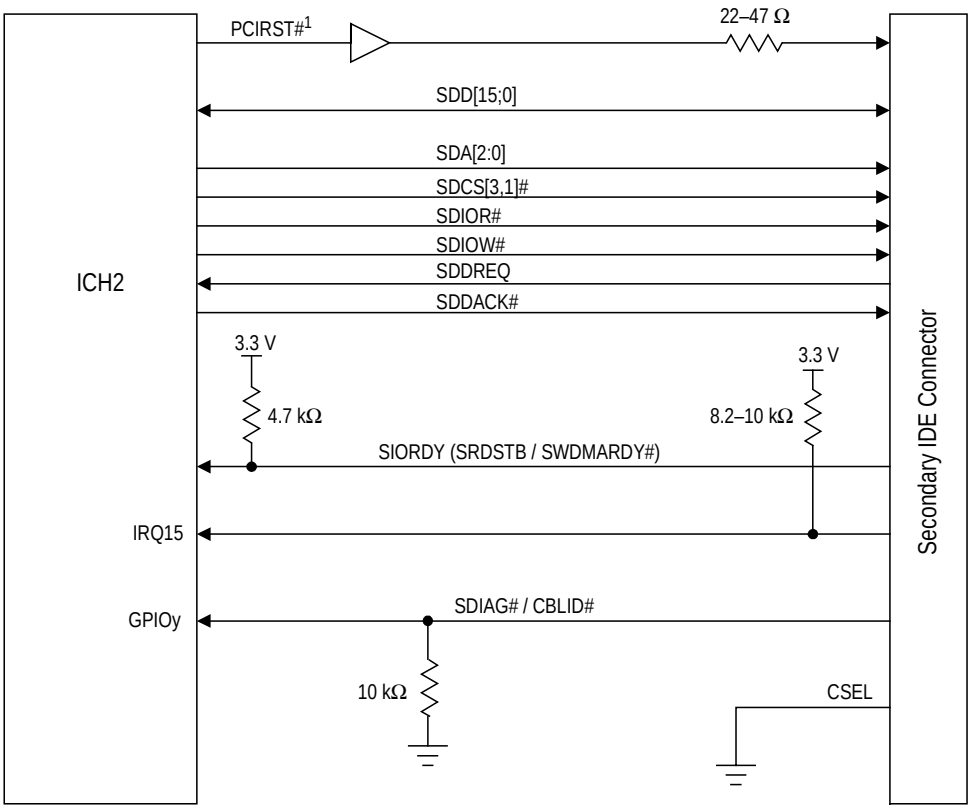
Figure 87. Connection Requirements for Primary IDE Connector



- 22 Ω–47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3.3.
- A 4.7 kΩ pull-up resistor to VCC3.3 is required on PIORDY and SIORDY.
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.

9.1.4 Secondary IDE Connector Requirements

Figure 88. Connection Requirements for Secondary IDE Connector



- 22 Ω–47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3.3.
- A 4.7 kΩ pull-up resistor to VCC3.3 is required on PIORDY and SIORDY
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.

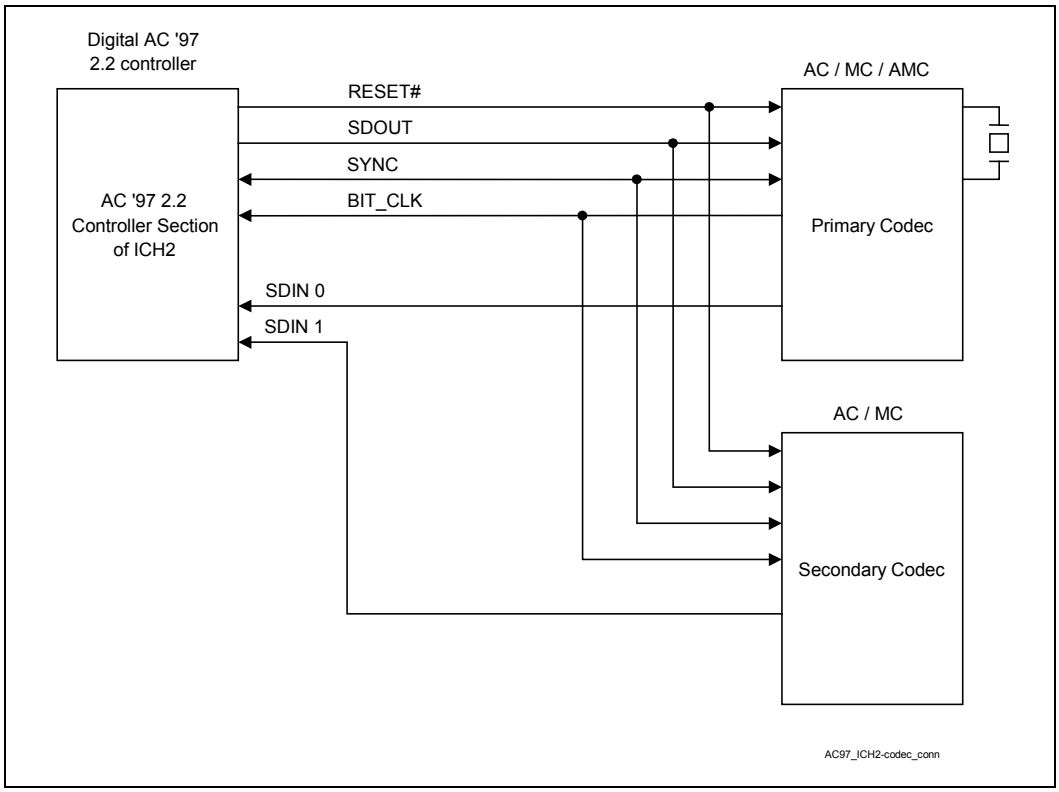
9.2 Audio Codec ’97 (AC’97)

The ICH2 implements an *Audio Cod‘c '97 Component Specification v2.2*-compliant digital controller. Any codec attached to the ICH2 AC-link must be *Audio Cod‘c '97 Component Specification v2.2*-compliant as well. Contact your codec IHV for information on *Audio Cod‘c '97 Component Specification v2.2*-compliant products. The *Audio Cod‘c '97 Component Specification v2.2* is on the Intel website at

http://developer.intel.com/ial/scalableplatforms/audio/index.htm.

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH2 AC-link allows a maximum of two codecs to be connected. Figure 89 shows a two-codec topology of the AC-link for the ICH2.

Figure 89. Intel® ICH2 AC’97–Codec Connection



In a lightly loaded system (e.g., single codec down), AC'97 signal integrity should be evaluated to confirm that the signal quality on the link is acceptable to the codec used in the design. A series resistor at the driver and a capacitor at the codec can be implemented in order to compensate for any signal integrity issues. The values used will be design dependent and should be verified for correct timings. The ICH2 AC-link output buffers are designed to meet the AC'97 2.1 specification with the specified load of 50 pF.

The ICH2 supports the following combinations of codecs:

Figure 90. Audio Codec

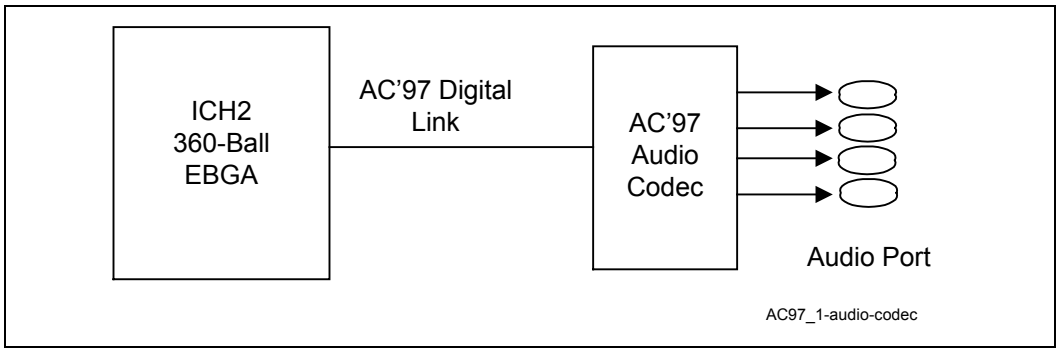


Figure 91. Modem Codec

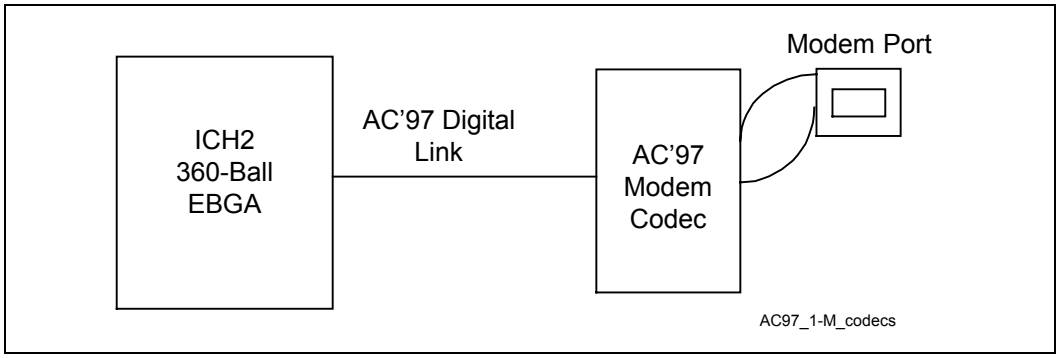


Figure 92. Audio/Modem Codec

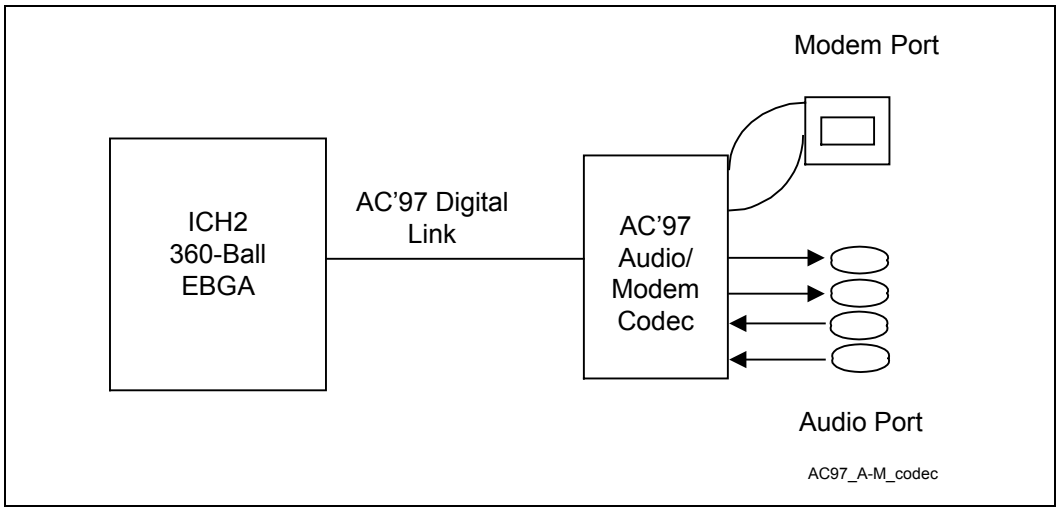


Figure 93. Modem Codecs

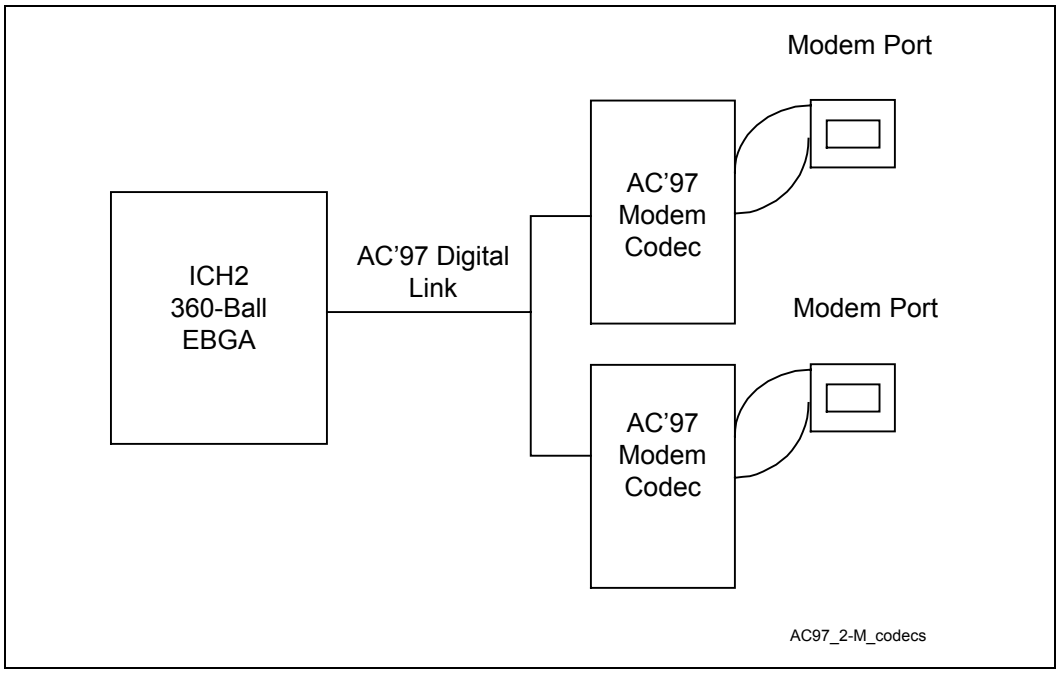


Figure 94. Audio and Modem Codecs

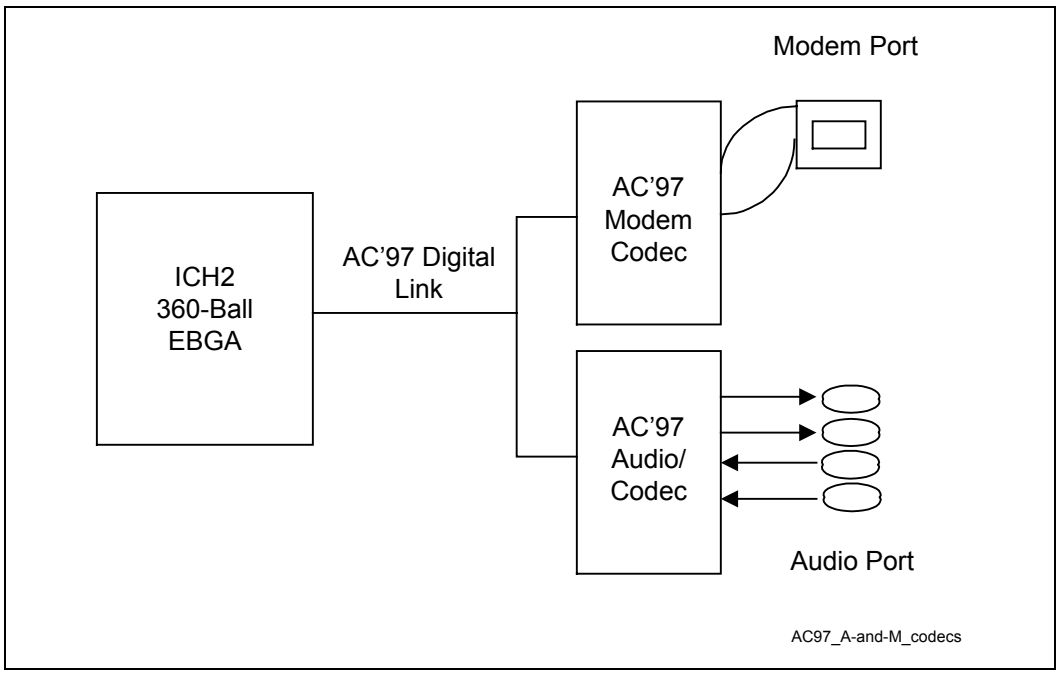


Figure 95. Audio Codecs

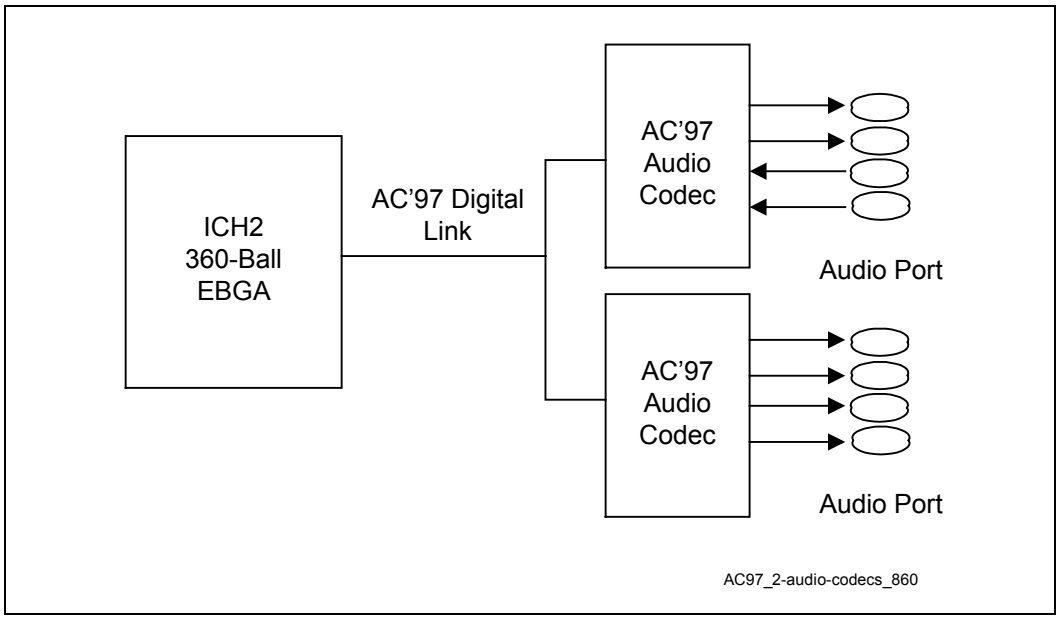
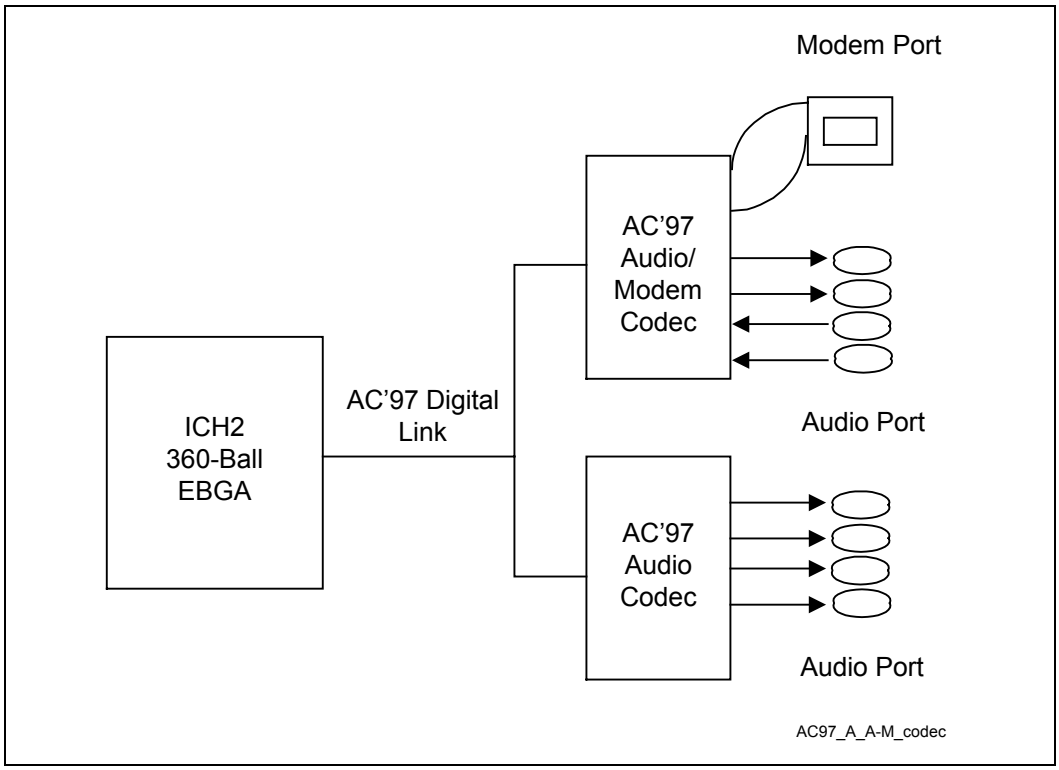


Figure 96. Audio and Audio/Modem Codecs



The AC'97 interface can be routed using 5 mil traces with 5 mil space between the traces. Maximum length between ICH2 to CODEC/CNR is 14 inches in a tee topology. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 4 inches for the AC'LINK. Trace impedance should be $Z_0 = 60\ \Omega \pm 15\%$.

Intel has developed an advanced common connector for both AC'97 and networking options. This is known as the Communication Network Riser (CNR).

Clocking is provided from the primary codec on the link via BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH2), and any other codec present. That clock is used as the time base for latching and driving data.

The ICH2 supports wake on ring from S1–S5 via the AC'97-link. The codec asserts SDATA_IN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH2 has weak pull-downs/pull-ups that are only enabled when the AC-link shut-off bit in the ICH2 is set. This keeps the link from floating when the AC-link is off, and when there are no codecs present.

If the shut-off bit is not set, it implies that there is a codec on the link. Therefore, BITCLK and AC_SDOUT will be driven by the codec and ICH2 respectively. However, AC_SDIN0 and AC_SDIN1 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec. If there is one or no CODEC onboard, then the unused AC_SDINx pin(s) should have a weak (10 kΩ) pull-down to keep it from floating.

Table 34. AC'97 SDIN Pull-Down Resistors

System Solution	Pull-Up Requirements
On-Board Codec Only	Pull-down the SDIN pin that is **not** connected to the codec
AMR Only	Pull-down **both** SDIN pins
Both AMR and On-Board Codec	Pull-down any SDIN pin that could be NC(1)

Note: (1)If the on-board codec can be disabled, both SDIN pins must have pull-downs. If the on-board codec cannot be disabled, only the SDIN not connected to the on-board codec requires a pull-down.

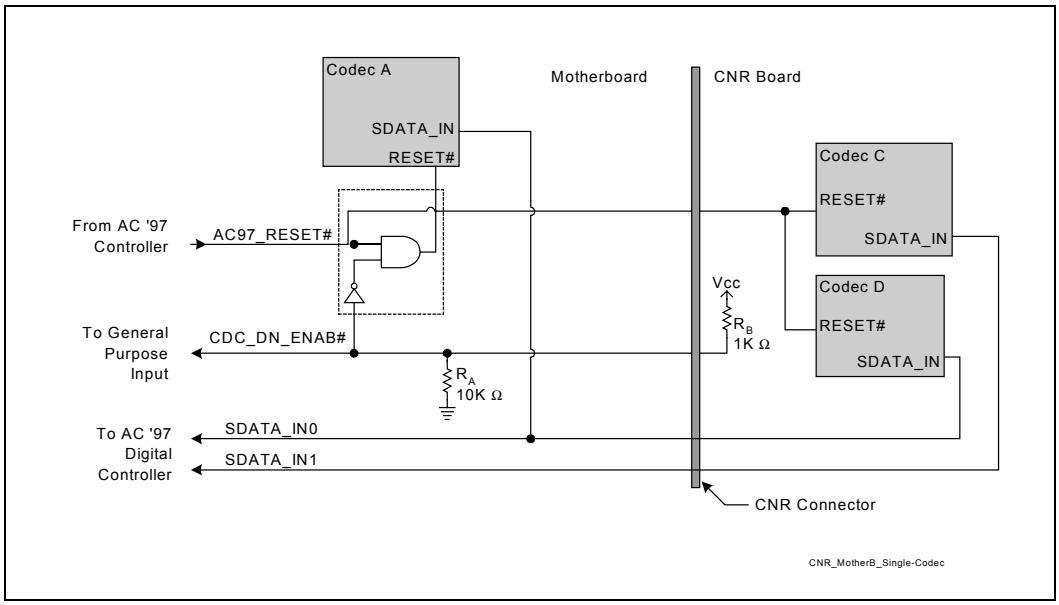
9.2.1 AC'97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. Refer to Intel's White Paper, *Recommendations for ICHx/A'97 Audio (Motherboard and Communication and Network Riser)*, for Intel's recommended codec configurations.

To support more than two channels of audio output, the ICH2 allows for a configuration where two audio codecs work concurrently to provide surround capabilities. To maintain data-on-demand capabilities, the ICH2 AC'97 controller, when configured for 4 or 6 channels, waits for all the appropriate slot request bits to be set before sending data in the SDATA_OUT slots. This allows for simple FIFO synchronization of the attached codecs. It is assumed that both codecs are programmed to the same sample rate, and that the codecs have identical (or at least compatible) FIFO depth requirements. It is recommended that the codecs be provided by the same vendor, upon the certification of their interoperability in an audio channel configuration.

The following circuits (Figure 97 through Figure 100) show the adaptability of a system with the modification of R_A and R_B combined with some basic glue logic to support multiple codec configurations. This also provides a mechanism to make sure that only two codecs are enabled in a given configuration and allows the configuration of the link to be determined by the BIOS so that the correct Pnp IDs can be loaded.

Figure 97. CDC_DN_ENAB# Support Circuitry for a Single Codec Motherboard



As shown in Figure 97, when a single codec is located on the motherboard, the resistor R_A and the circuitry (AND and NOT gates) shown inside the dashed box must be implemented on the motherboard. This circuitry is required in order to disable the motherboard codec when a CNR is installed which contains two AC ’97 codecs (or a single AC ’97 codec which must be the primary codec on the AC-link).

By installing resistor R_B (1 kΩ) on the CNR, the codec on the motherboard becomes disabled (held in reset) and the codec(s) on the CNR take control of the AC-link. One possible example of using this architecture is a system integrator installing an audio plus modem CNR in a system already containing an audio codec on the motherboard. The audio codec on the motherboard would then be disabled, allowing all of the codecs on the CNR to be used.

The architecture shown in Figure 98 has some unique features. These include the possibility of the CNR being used as an upgrade to the existing audio features of the motherboard (by simply changing the value of resistor R_B on the CNR to 100 kΩ). An example of one such upgrade is increasing from two-channel to four- or six-channel audio.

Both Figure 98 and Figure 99 show a switch on the CNR board. This is necessary to connect the CNR board codec to the proper SDATA_IN line to prevent conflicts with the motherboard codec(s).

Figure 98. CDC_DN_ENAB# Support Circuitry for Multi-Channel Audio Upgrade

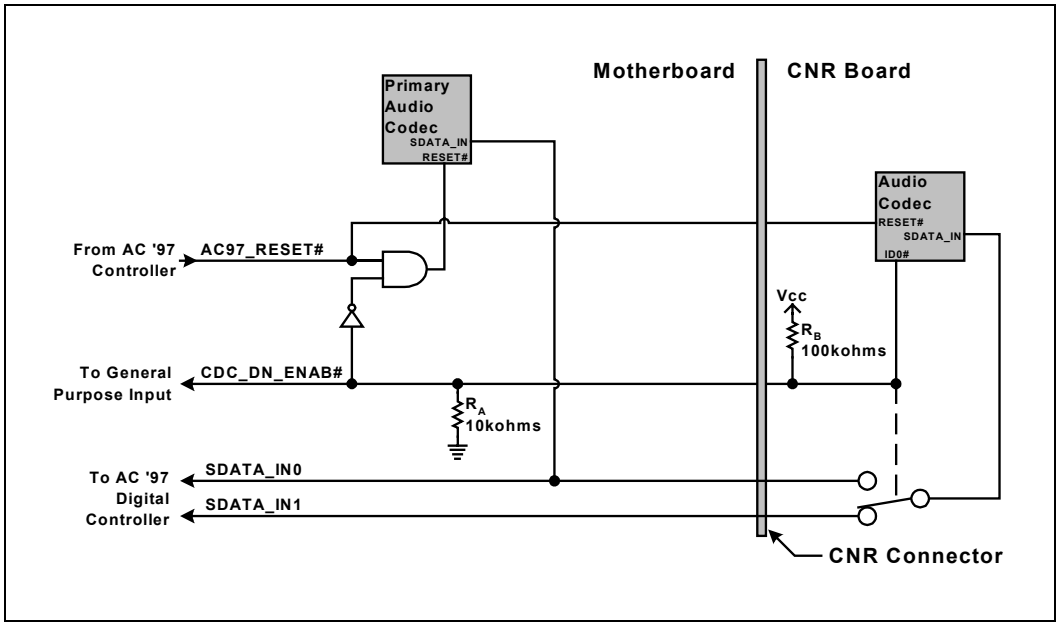


Figure 99 shows the circuitry required on the motherboard to support a two-codec down configuration. This circuitry disables the codec on a single codec CNR. Notice that in this configuration the resistor, R_B, has been changed to 100 kΩ.

Figure 99. CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard / One-Codec on CNR

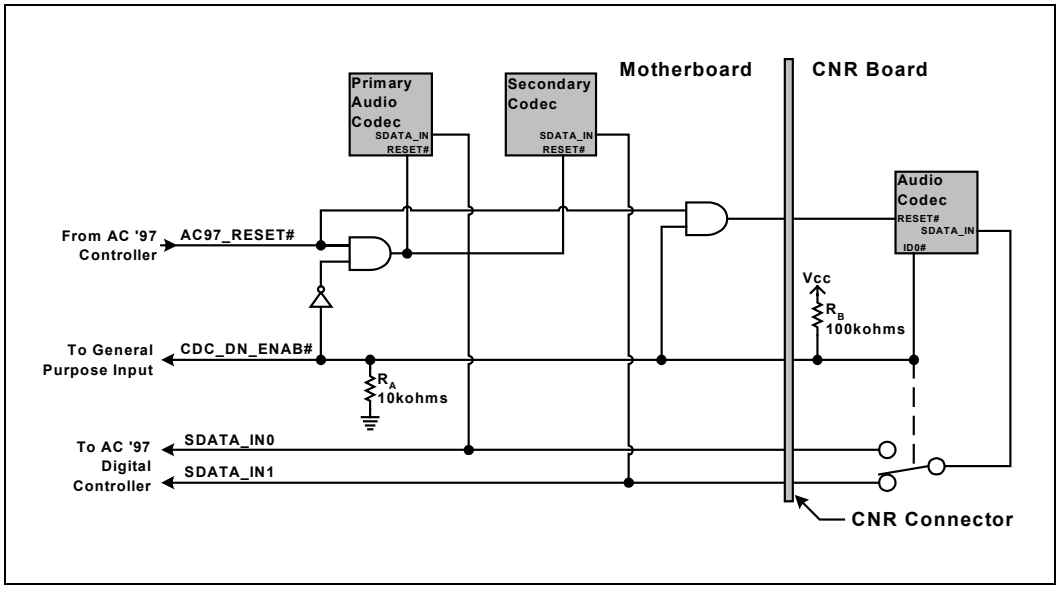
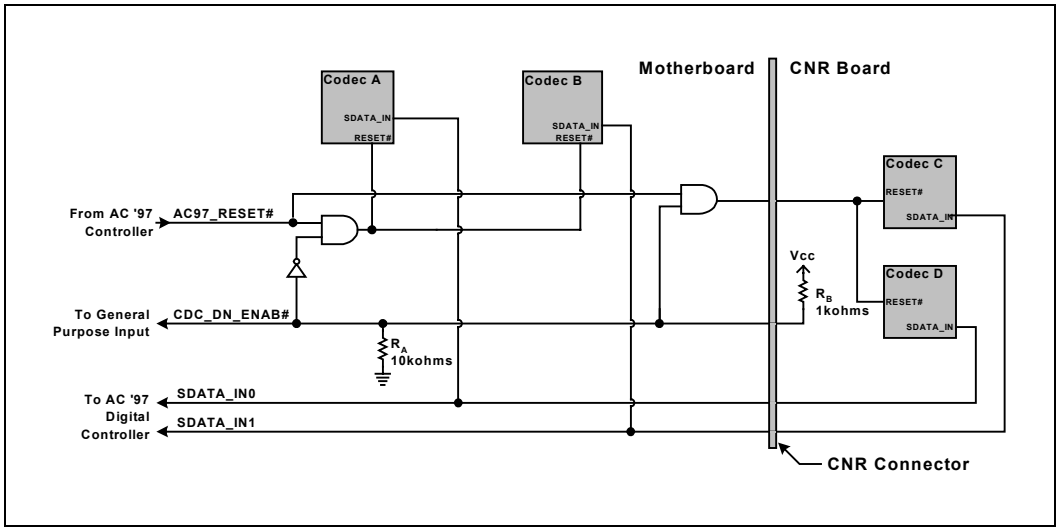


Figure 100 shows the case of two-codecs down and a dual-codec CNR. In this case, both codecs on the motherboard are disabled (while both on CNR are active) by R_A being 10 kΩ, and R_B being 1 kΩ.

Figure 100. CDC_DN_ENAB# Support for Two-Codecs on Motherboard / Two-Codecs on CNR



Circuit Notes:

1. All CNR designs include resistor R_B. The value of R_B is either 1 kΩ or 100 kΩ, depending on the intended functionality of the CNR (whether or not it intends to be the primary/controlling codec).
2. Any CNR with two codecs must implement R_B with value 1 kΩ. If there is one Codec, use a 100 kΩ pull-up resistor. A CNR with zero codecs must not stuff R_B. If implemented, R_B must be connected to the same power well as the codec so that it is valid whenever the codec has power.
3. A motherboard with one or more codecs down must implement R_A with a value of 10 kΩ.
4. The CDC_DN_ENAB# signal must be run to a GPI so that the BIOS can sense the state of the signal. CDC_DN_ENAB# is *required* to be connected to a GPI; a connection to a GPIO is *strongly recommended* for testing purposes.

Table 35. Signal Descriptions

CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC'97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC'97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC '97 Interface.
AC97_RESET#	Reset signal from the AC'97 Digital Controller (ICH2).
SDATA_IN0 **SDATA_IN1**	AC'97 serial data from an AC'97-compliant codec to an AC '97-compliant controller (i.e., the ICH2).

9.2.2 Valid Codec Configurations

Table 36. Codec Configurations

Valid Codec Configurations
AC(Primary)
MC(Primary)
AMC(Primary)
AC(Primary) + MC(Secondary)
AC(Primary) + AC(Secondary)
AC(Primary) + AMC(Secondary)

Invalid Codec Configurations
MC(Primary) + X(any other type of codec)
AMC(Primary) + AMC(Secondary)
AMC(Primary) + MC(Secondary)

9.3 USB Guidelines

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15 kΩ pull-down resistors on both P+/P- data lines.
- 15 Ω series resistors should be placed as close as possible to the ICH2 (<1 inch). These series resistors are required for source termination of the reflected signal.
- Optional 47 pF capacitors may be placed as close to the USB connector as possible and on the ICH2 side of the series resistors on the USB data lines (P0±, P1±, P2±, P3±). These capacitors are used to improve signal quality (rise/fall time), and to help minimize EMI radiation.
- 15 kΩ ± 5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0±… P3±), and are REQUIRED for signal termination by USB specification. The length of the stub should be as short as possible.
- The trace impedance for the P0±… P3 ±signals should be 45 Ω (to ground) for each USB signal P+ or P-. The impedance is 90 Ω between the differential signal pairs P+ and P- to match the 90 Ω USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting 45 Ω impedance. The trace impedance can be controlled by carefully selecting the line width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as critical signals. The P+/P- signal pair must be routed together parallel to each other on the same layer, and not parallel with other non-USB signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces helps prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This minimizes the effect of common mode current on EMI. Lastly, do not route over plane splits.

The following figure illustrates the recommended USB schematic.

Figure 101. USB Data Line Schematic

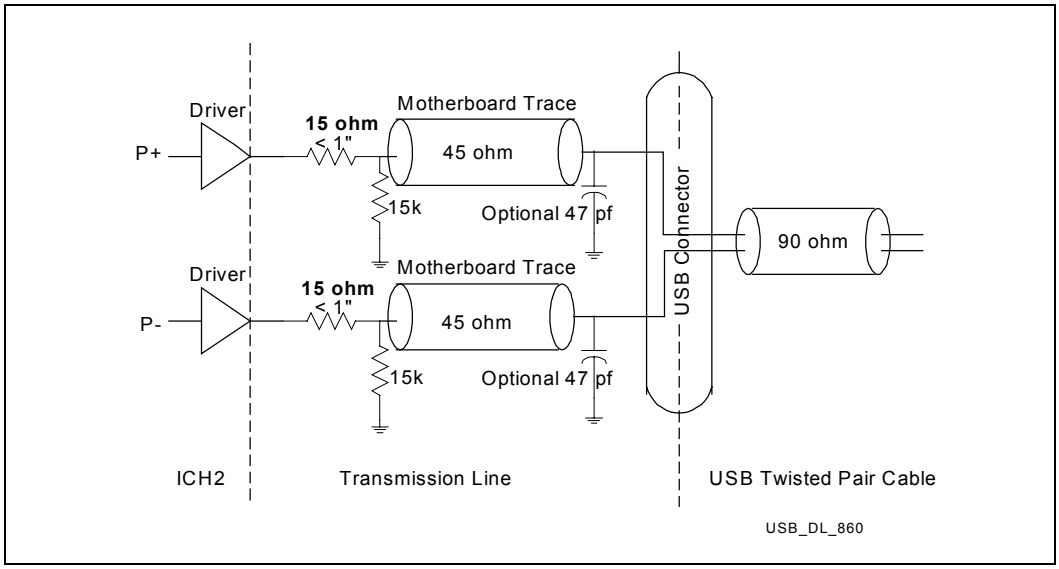


Table 37. Recommended USB Trace Characteristics

Impedance 'Z0'	Line Delay	Capacitance	Inductance	Resistance @ 20° C
45.4 Ω	160.2 ps	3.5 pF	= 7.3 nH	53.9 mΩ

9.4 I/O APIC Design Recommendations

For the Intel Xeon processor and Intel Xeon processor with 512 KB L2 cache:

- These processors do not have I/O APIC pins defined. These processors receive interrupts for servicing via the system bus. Refer to the *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet*, document 290687, for more details.

On the ICH2:

- Tie PICCLK directly to ground
- Tie PICD0, PICD1 to ground via 1 kΩ to 10 kΩ resistors

9.5 SMBus/SMLink Interface

The SMBus interface on the ICH2 is the same as that on the ICH. It uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus. The SMBus Host Controller uses these signals. The SMBus Host Controller resides inside the ICH2. If the SMBus is used only for the Rambus* SPD EPROM's (one on each RIMM connector), both signals should be pulled up with a 4.7 kΩ resistor to 3.3 V.

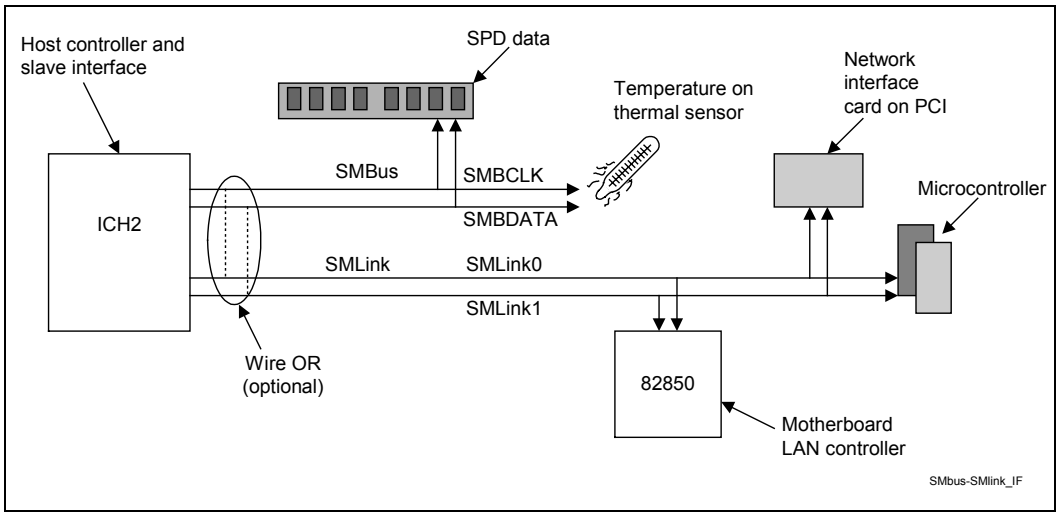
The ICH2 incorporates a new SMLink interface supporting AOL, AOL2 and a slave functionality. It uses two signals, SMLink[1:0]. SMLink[0] corresponds to an SMBus clock signal and SMLink[1] corresponds to an SMBus data signal. Internally the SMLink signals are connected to the following:

- ICH2 Slave Interface
- ICH2 TCO Host Controller
- ICH2 Integrated LAN Slave Interface

For Alert On LAN* (AOL®) functionality, TCO Host Controller transmits heartbeat and event messages over the interface. When using the Intel 82562EM Platform LAN Connect Component, the ICH2's integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert-on-Lan2*-enabled LAN Controller (i.e., Intel PRO/100 S Desktop Adapter) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH2 SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, and the watchdog timer status and system status bits.

Both the SMBus Host Controller and the TCO Host Controller obey the SMBus protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (e.g., Intel PRO/100 S Desktop Adapter) to access targets on the SMBus as well as the ICH2 Slave interface. This is done by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA. See Figure 102.

Figure 102. SMBUS/SMLink Interface



Note: Intel does not support external access of the ICH2's Integrated LAN Controller via the SMLink interface. Also, Intel does not support access of the ICH2's SMBus Slave Interface by the ICH2's SMBUS Host Controller.

Refer to *the Intel® 82801BA I/O Controller Hub 2 (ICH2) I/O and Intel® 82801 BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

Table 38. SMBus/SMLink Requirements

SMBus / SMLink Use	Implementation
Alert-on-LAN* signals	4.7 kΩ pull-up resistors to 3.3 VSB are required.
GPIOs	Pull-up resistors to 3.3 VSB and the signals must be allowed. To change states on power-up (e.g., on power-up, the ICH2 drives *heartbeat* messages until the BIOS programs these signals as GPIOs). The value of the pull-up resistors depends on the loading on the GPIO signal.
Not Used	4.7 kΩ pull-up resistors to 3.3 VSB are required.

9.5.1 SMBus Architecture and Design Considerations

9.5.1.1 SMBus Design Considerations

There are several possibilities for designing an SMBus using the ICH2. Designs can be grouped into three major categories based on the power supply source for the SMBus microcontrollers. This includes two unified designs in which all devices are powered by either VCC_CPU or VCC_Suspend, and a mixed design in which some devices are powered by each of the two supplies.

Primary considerations in choosing a design are based on:

- Are there devices that must run in STR?
- Amount of VCC_Suspend current available (i.e., minimizing load of VCC_Suspend)
- Are there enough unique address configuration settings for all devices on a particular SMBus segment?

Refer to Section 5.4.2.4.1 for additional design considerations when implementing the processor manageability features via the SMBus.

9.5.1.1.1 General Design Issues and Notes

Regardless of the architecture used, there are some general considerations.

The pull-up resistor size for the SMBus data and clock signals is dependent on the number of devices present on the bus. A typical value is 8.2 kΩ. This should prevent the SMBus signals from floating, which could cause leakage in the ICH2 and other devices.

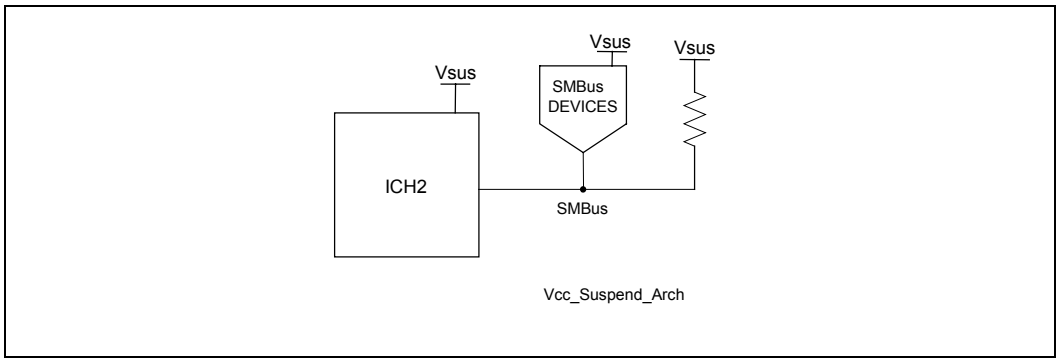
RIMM connector memory modules have a separate power source from the Direct RDRAM device array for the SPD device. If this SPD device must operate in STR, it should be connected to the VCC_Suspend supply.

The ICH2 does not run SMBus cycles while in STR. SMBus devices that can operate in STR must be powered by the VCC_Suspend supply.

9.5.1.1.2 The Unified VCC_Suspend Architecture

In this design all SMBus devices are powered by the VCC_Suspend supply. Consideration must be made to provide enough VCC_Suspend current while in STR.

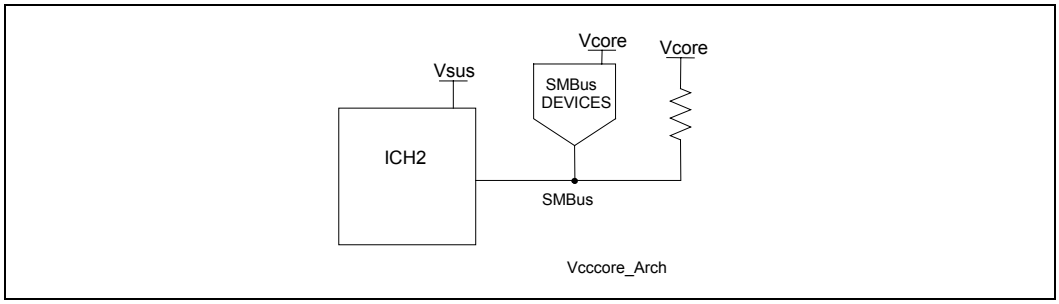
Figure 103. Unified VCC_Suspend Architecture



9.5.1.1.3 The Unified VCC_CPU Architecture

In this design, all SMBUS devices are powered by the VCC_CPU supply. This architecture allows none of the devices to operate in STR, but minimizes the load on VCC_Suspend. See Figure 104.

Figure 104. Unified VCC_CPU Architecture



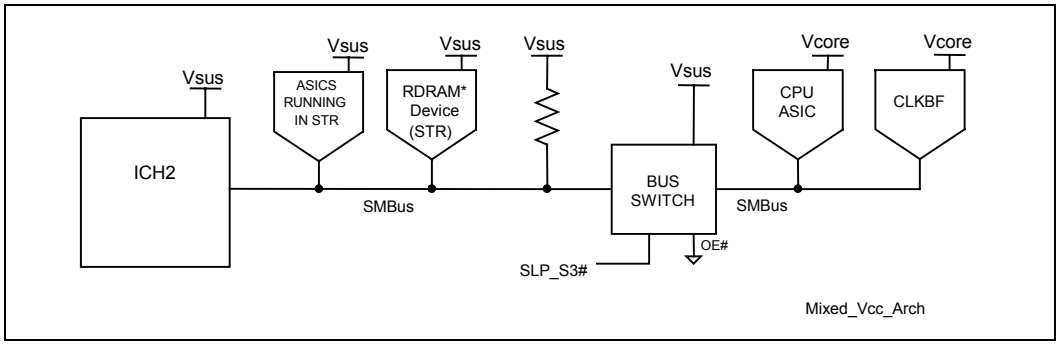
Note: The SMBus device must be back-drive safe while its supply (Vcore) is off and VCC_Suspend is still powered.

Note: In suspended modes where VCC_CPU is OFF & VCC_Suspend is on, the VCC_CPU node will be very near ground. In this case the input leakage of the ICH2 will be approximately 10 µA.

9.5.1.1.4 Mixed Architecture

This design allows for SMBus devices to communicate while in STR, yet minimizes VCC_Suspend leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a “bus switch” to isolate the devices powered by the core and suspend supplies. See Figure 105.

Figure 105. Mixed VCC_Suspend/ VCC_CPU Architecture



Added Considerations for Mixed Architecture

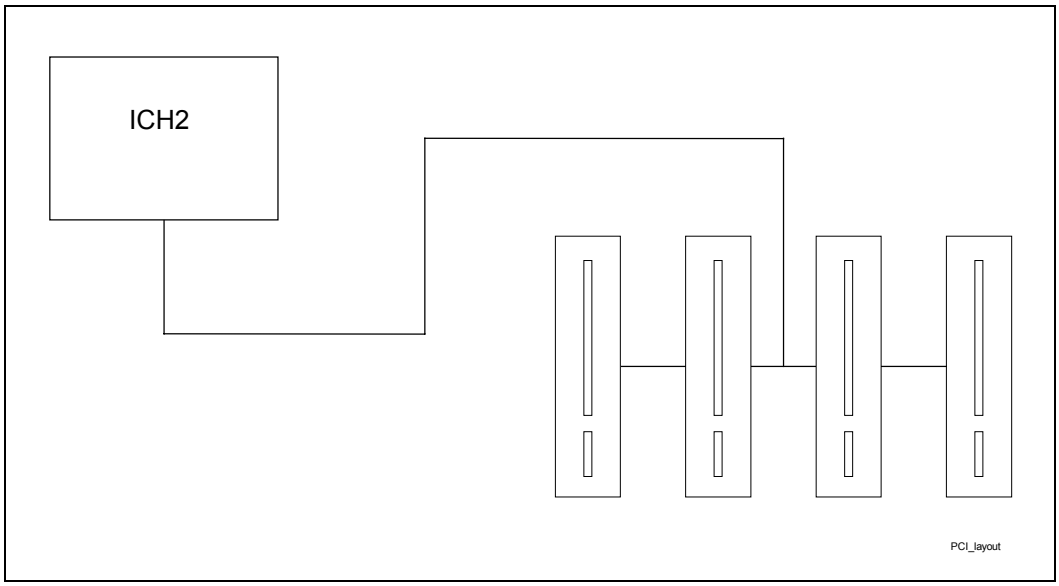
- The bus switch must be powered by VCC_Suspend.
- If there are 5 V SMBus devices used, then an added level translator must be used to separate those devices driving 5 V from those driving 3 V signal levels.
- Devices that are powered by the VCC_Suspend well must not drive into other devices that are powered off. This is accomplished with the “bus switch”.

9.6 PCI

The ICH2 provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification*, Revision 2.2. The implementation is optimized for high-performance data streaming when the ICH2 is acting as either the target or the initiator on the PCI bus. For more information about the PCI Bus interface, refer to the *PCI Local Bus Specification*, Revision 2.2.

The ICH2 supports six PCI Bus masters (excluding the ICH2), by providing six REQ#/GNT# pairs. In addition, the ICH2 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 106. PCI Bus Layout Example



9.7 RTC

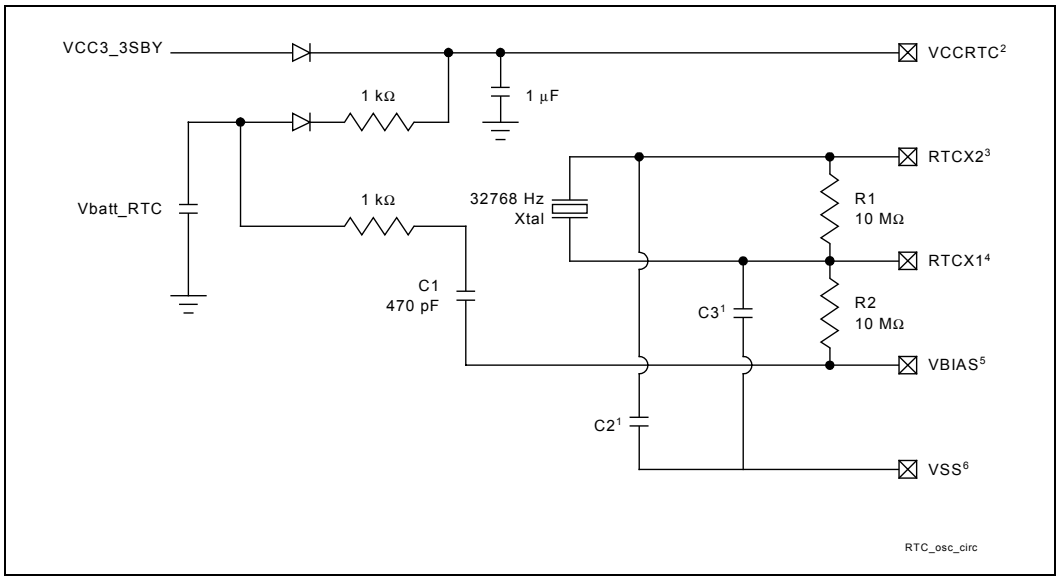
The ICH2 contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

This section will present the recommended hookup for the RTC circuit for the ICH2. **This circuit is not the same as the circuit used for the PIIX4.**

9.7.1 RTC Crystal

The ICH2 RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 pins. Figure 107 documents the external circuitry that comprises the oscillator of the ICH2 RTC.

Figure 107. Intel® ICH2 Oscillator Circuitry



NOTES:

1. The exact capacitor value must be based on the crystal manufacturer's recommendation (Typical values for C2 and C3 are 18 pF for a crystal with CLOAD=12.5 pF)
2. VCC RTC: Power for RTC Well
3. RTCX2: Crystal Input 2–Connected to the 32.768 kHz crystal.
4. RTCX1: Crystal Input 1–Connected to the 32.768 kHz crystal.
5. VBIAS: RTC BIAS Voltage–This pin is used to provide a reference voltage, and this DC voltage sets a current that is mirrored throughout the oscillator and buffer circuitry.
6. VSS: Ground.

9.7.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C1 must be 0.047 µF, and the external capacitor values (C2 and C3) should be chosen to provide the manufacturer's specified load capacitance (C_{LOAD}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer the capacitor value can be matched to the actual load capacitance of the crystal used, the more accurate the RTC will be.

Equation 11 can be used to choose the external capacitance values (C2 and C3):

Equation 11. External Capacitance Values

$$C_{LOAD} = (C_2 * C_3)/(C_2+C_3) + C_{PARASITIC}$$

Note: C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain the 32.768 kHz.

9.7.3 RTC Layout Considerations

- Keep the RTC lead lengths as short as possible; around ¼ inch is sufficient.
- Minimize the capacitance between XIN and XOUT in the routing.
- Put a ground plane under the XTAL components.
- Do not route switching signals under the external components (unless on the other side of the board).
- The oscillator VCC should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

9.7.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH2 is not powered by the system.

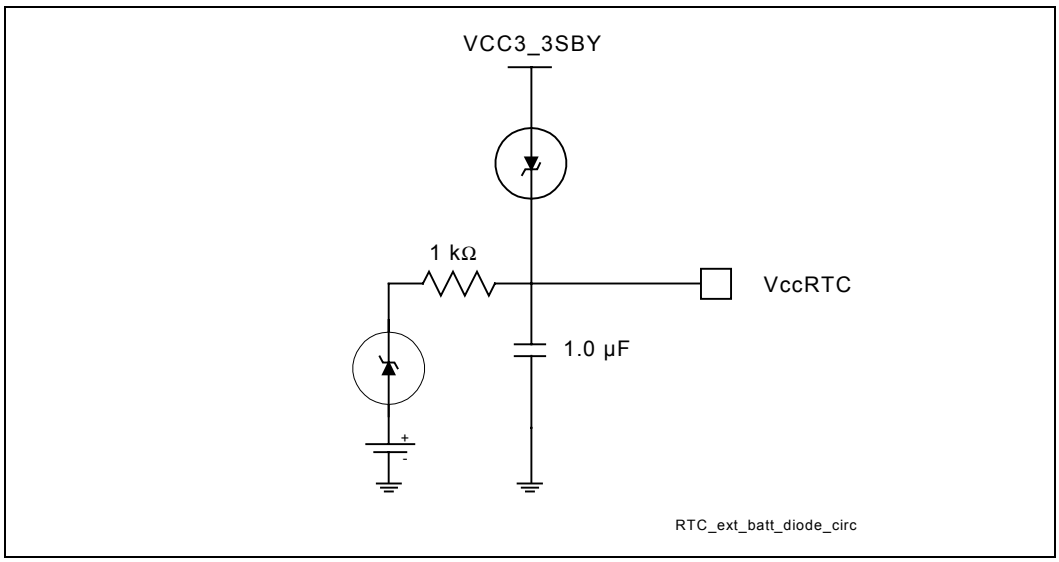
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 uA, the battery life will be at least:

170,000 µAh / 3 µA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH2 through an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH2 RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 108 is an example of a diode circuitry that is used.

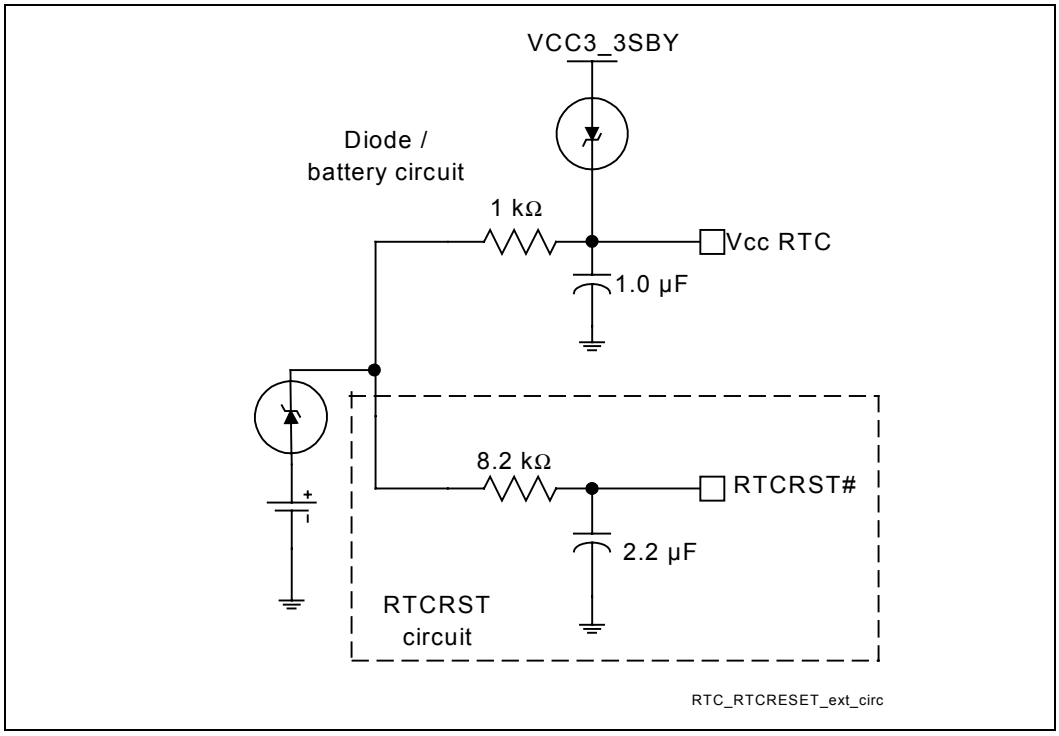
Figure 108. Diode Circuit to Connect RTC External Battery



A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and, thereby, the RTC accuracy.

9.7.5 RTC External RTCRST Circuit

Figure 109. RTCRST External Circuit for the Intel® ICH2 RTC



The ICH2 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10–20ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (Figure 108) which allows the RTC well to be powered by the battery when the system power is not available. Figure 109 is an example of this circuitry that is used in conjunction with the external diode circuit.

9.7.6 RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths of less than 1 inch, the shorter the better.
- Minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them).
- Put a ground plane under all of the external RTC circuitry.
- Do not route any switching signals under the external components (unless on the other side of the ground plane).

9.7.7 VBIAS DC Voltage and Noise Measurements

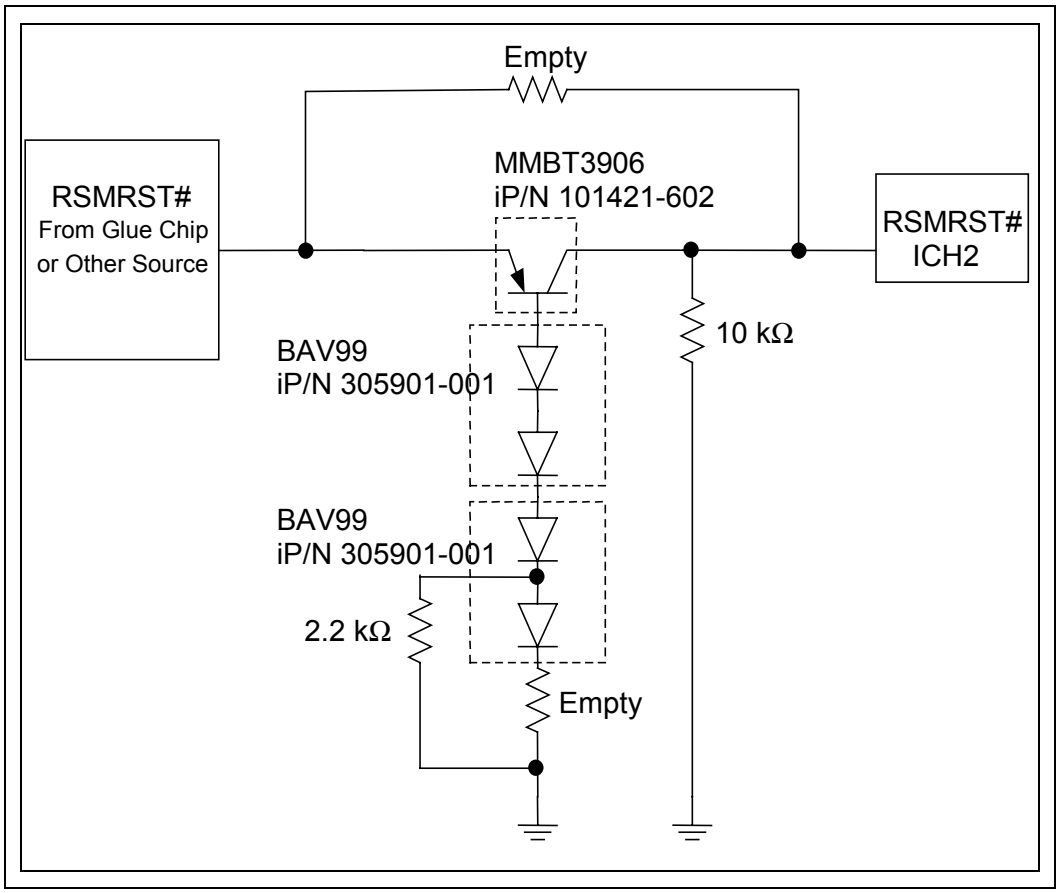
- Steady state VBIAS will be a DC voltage of about 0.38 V ± 0.06V.
- VBIAS will be "kicked" when the battery is inserted to about 0.7–1.0V, but it will come back to its DC value within a few ms.
- Noise on VBIAS must be kept to a minimum, 200 mV or less.
- VBIAS is very sensitive and cannot be directly probed. It can be probed through a 0.01 µF capacitor.
- Excess noise on VBIAS can cause the ICH2 internal oscillator to misbehave or even stop completely.
- To minimize noise of VBIAS It is necessary to implement the routing guidelines described above and the required external RTC circuitry as described in the *Intel® 82801BA I/O Controller Hub 2 (ICH2) I/O Buffer Model Documentation and Intel® 82801 BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet*.

9.7.8 Power-Well Isolation Control

The RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in Figure 107 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VCCRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

- The circuit shown in Figure 110 below should be implemented to control well isolation between the 3.3 V resume and RTC power-wells. Failure to implement this circuit may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power).

Figure 110, RTC Power-Well Isolation Control



9.8.9 Power Supply PS_ON Considerations

- If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10-100mS) such that PS_ON is driven active during the exponential decay of the power rails, a few power supplies may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.
- The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).
- The platform designer must ensure that the power supply used with the platform is not affected by this issue.

9.8 LAN Layout Guidelines

The ICH2 provides several options for integrated LAN capability. The platform supports several components depending on the target market. These guidelines use the 82562ET to refer to both the 82562ET and 82562EM. The 82562EM is specified in those cases where there is a difference.

Table 39. Integrated LAN Options

Platform LAN Connect Component	Connection	Features
82562EM	Advanced 10/100 Ethernet	Alert-on-LAN* and Ethernet 10/100 Connection
82562ET	10/100 Ethernet	Ethernet 10/100 Connection
82562EH	1-Mb HomePNA* LAN	1-Mb HomePNA* connection

Intel developed a dual footprint for 82562ET and 82562EH to minimize the required number of board builds. A single layout with the specified dual footprint will allow the OEM to install the appropriate Platform LAN Connect Component to meet the market need. Design guidelines are provided for each required interface and connection. Refer to Figure 111 and Table 40 for the corresponding section of the design guide.

Figure 111. Intel® ICH2 / LAN Connect Section

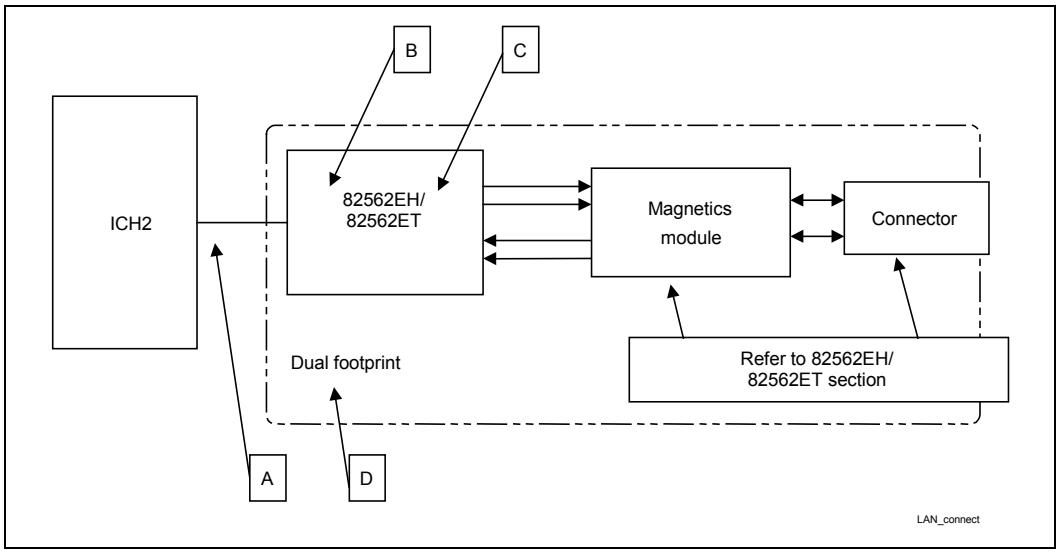


Table 40. LAN Design Guide Section Reference

Layout Section	Figure 107 Reference	Design Guide Section
ICH2–LAN Interconnect	A	9.8.1, Intel® ICH2–LAN Interconnect Guidelines
General Routing Guidelines	B, C, D	9.8.2, General LAN Routing Guidelines and Considerations
82562EH	B	9.8.3, Intel® 82562EH Home/PNA Guidelines
82562ET/EM	C	9.8.4, Intel® 82562ET/EM Guidelines
Dual Layout Footprint	D	9.8.5, Intel® 82562ET / Intel® 82562EH Dual Footprint Guidelines

9.8.1 Intel® ICH2—LAN Interconnect Guidelines

This section contains guidelines to the design of motherboards and riser cards to comply with LAN Connect. It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH2 to LAN component interface. The following signal lines are used on this interface:

LAN_CLK
LAN_RSTSYNC
LAN_RXD[2:0]
LAN_TXD[2:0]

This interface supports both 82562EH and 82562ET/EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by both components. Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected when 82562EH is installed Dual footprint guidelines are found in Section 9.8.5.

9.8.1.1 Bus Topologies

The LAN Connect Interface can be configured in several topologies:

- Direct point-to-point connection between the ICH2 and the LAN component
- Dual Footprint

9.8.1.2 Point-to-Point Interconnect

The following are guidelines for a single solution motherboard. Either 82562EH or 82562ET are installed.

Figure 112. Single Solution Interconnect

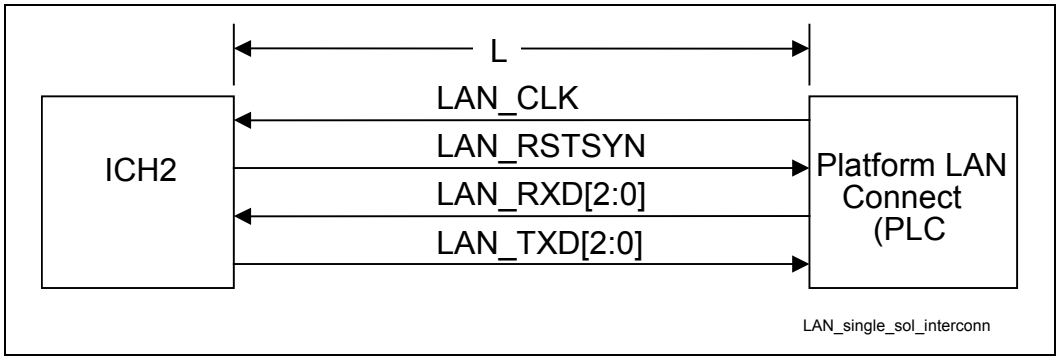


Table 41. Length Requirements for Single Solution Interconnect

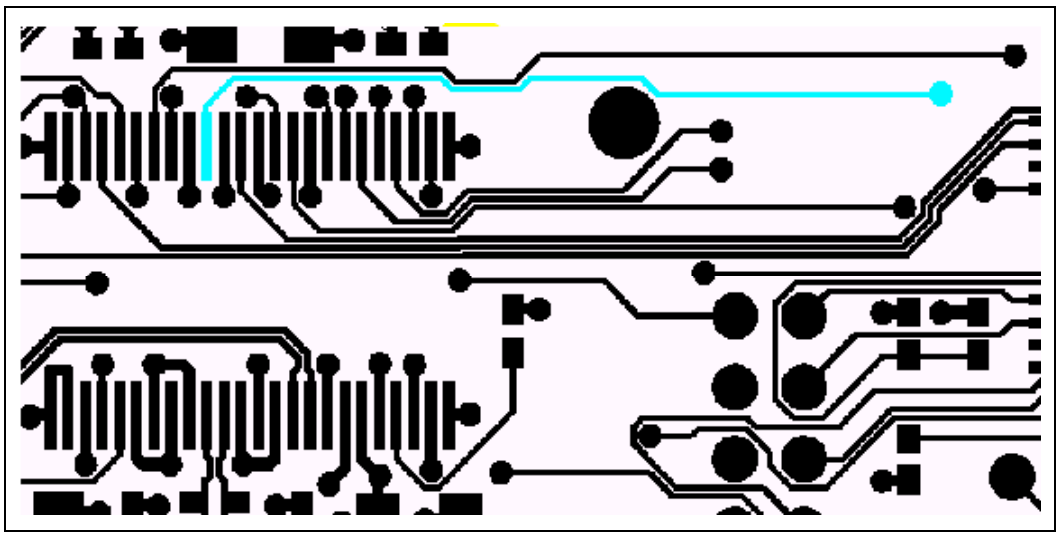
Component	Minimum (inches)	Maximum (inches)	Notes
82562EH	L=4.5	L=10	Signal Lines LAN_RXD[2:1] and LAN_TXD[2:1] Not Connected.
82562ET	L=3.5	L=10	

Note: Length of trace from connector to LOM should be 0.5 to 3 inches.

9.8.1.3 Signal Routing and Layout

LAN Connect signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 113. LAN_CLK Routing Example



9.8.1.4 Crosstalk Consideration

Crosstalk noise must be carefully controlled to a minimum. Crosstalk is the primary cause of timing skews and is the largest part of the t_{RMATCH} skew parameter.

9.8.1.5 Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 Ω ±15% is strongly recommended; otherwise, signal integrity requirements may be violated.

9.8.1.6 Line Termination

Line termination mechanisms are not specified for the LAN Connect interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 33 Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

9.8.2 General LAN Routing Guidelines and Considerations

9.8.2.1 General Trace Routing Considerations

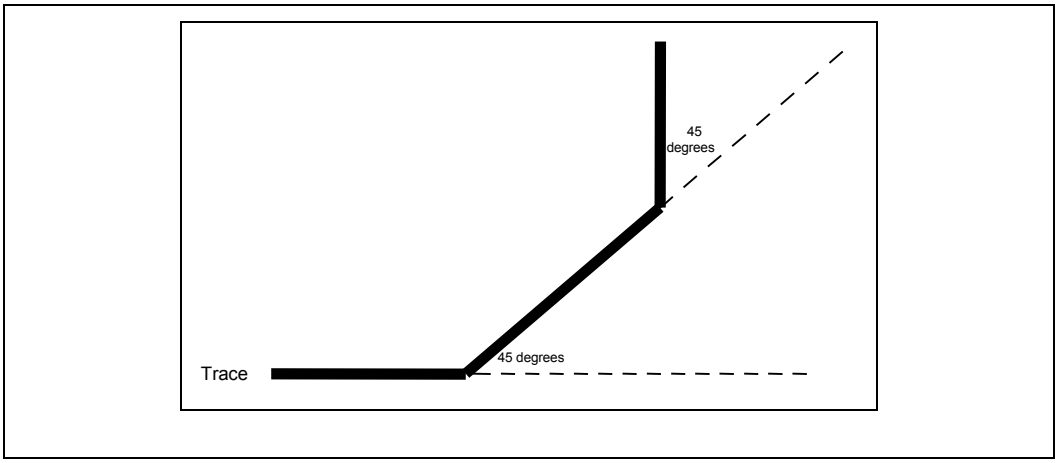
Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance:

Note: Some suggestions are specific to a 4.5 mil stack-up.

- Maximum mismatch between the length of the clock trace and the length of any data trace is 0.5 inch.
- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER.]
- Do not route the transmit differential traces closer than 70 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 70 mils to the differential traces.
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. Refer to Figure 114.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. As a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 114. Trace Routing



9.8.2.2 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by 10 Ω, when the traces within a pair are closer than 0.030 inches (edge-to-edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

9.8.2.2.1 Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 70 mils between all differential pairs (Phoneline and Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

9.8.2.3 Power and Ground Connections

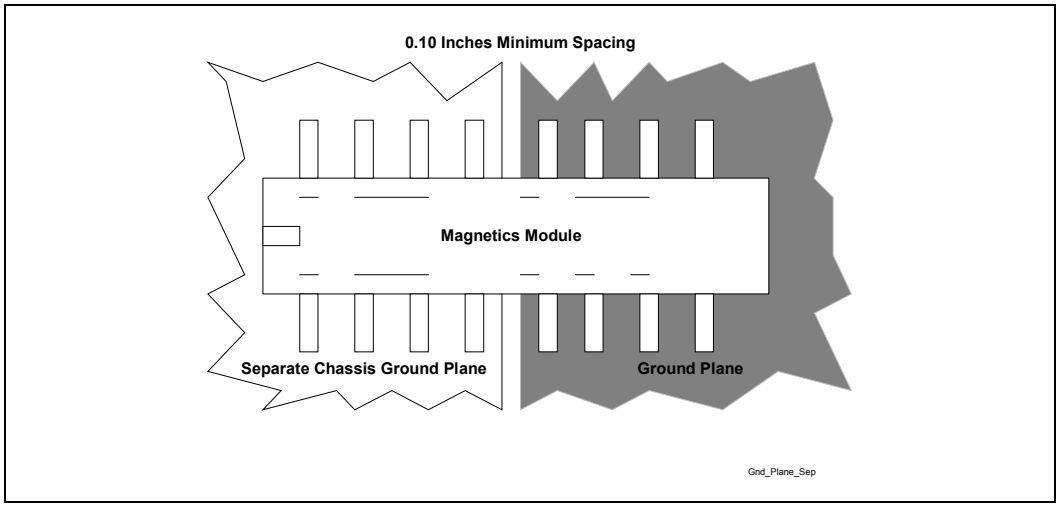
Some rules and guidelines to follow for power and ground connections:

- All VCC pins should be connected to the same power supply.
- All VSS pins should be connected to the same ground plane.
- Use one decoupling capacitor per power pin for optimized performance
- Place decoupling as close as possible to power pins.

9.8.2.3.1 General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 115. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both backplanes and motherboards.

- *Route traces over a continuous plane with no interruptions (do not route over a split plane).* If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling.
- Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.

- *Avoid fast rise/fall times as much as possible.* Signals with fast rise and fall times contain many high-frequency harmonics that can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 and/or RJ11 connector side of the transformer module should have chassis ground beneath. By splitting ground planes beneath the transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.
- *Create a spark gap between pins 2 through 5 of the Phoneline connector(s) and shield ground of 1.5 mm (59.0 mil).* This is a ***critical*** requirement needed to pass FCC part 68 testing for phoneline connection.

Note: For worldwide certifications, a trench of 2.5 mm is required.

9.8.2.4 Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

1. *Unequal length of the two traces within a differential pair.* Inequalities create common-mode noise and distort the transmit or receive waveforms.
2. *Lack of symmetry between the two traces within a differential pair.* [Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.] Asymmetry can create common-mode noise, and distort the waveforms.
3. *Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45/11 connector.* Beyond a total distance of about 4 inches, it can become extremely difficult to design a specification-compliant LAN product. If they are long, traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (less than or equal to one inch).
4. *Routing any other trace parallel to and close to one of the differential traces.* Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
5. *Routing the transmit differential traces next to the receive differential traces.* The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace, and can greatly degrade the recei'er's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. In the vicinities where the traces enter or exit the magnetics, the RJ-45/11, and the PLC are the only possible exceptions.
6. *Use of an inferior magnetics module.* The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no autotransformer in the transmit channel.)
7. *Another common mistake is using an 82555 or 82558 physical layer schematic in a PLC design.* The transmit terminations and decoupling are different, and there are also differences in the receive circuit. Follow the appropriate reference schematic or application notes.

8. *Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45/11 and for the wire-side center-taps of the magnetics modules.* These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The application notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. *Incorrect differential trace impedances.* It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they have designed for 100 Ω. (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by 5 Ω to 20 Ω. A 10 Ω to 15 Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.
10. *Another common problem is to use a capacitor that's too large between the transmit traces and/or too much capacitance from the magne'ic's transmit center-tap (on the 82562ET side of the magnetics) to ground.* Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs, and will cause return loss to fail at higher frequencies, and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) Unless there is some overshoot in
100 Mbps mode, these caps are not necessary.

Note: Keep the two traces within a differential pair close to each other. Keeping them close helps to make them more immune to crosstalk and other sources of common-mode noise. Keeping them close means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces. Close should be considered to be less than 0.030 inches between the two traces within a differential pair. A range of 0.008 inch to 0.012 inch trace-to-trace spacing is recommended.

9.8.3 Intel® 82562EH Home/PNA Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in section 9.8.2, *General LAN Routing Guidelines and Considerations*. Additional guidelines for implementing an 82562EH Home/PNA Platform LAN Connect Component are provided below.

9.8.3.1 Power and Ground Connections

Some rules to follow for power and ground connections:

- For best performance place decoupling capacitors on the backside of the PCB directly under the 82562EH with equal distance from both pins of the capacitor to power/ground.
- The analog power supply pins for 82562EH (VCCA, VSSA) should be isolated from the digital VCC and VSS through the use of ferrite beads. In addition, adequate filtering and decoupling capacitors should be provided between VCC and VSS, and VCCA and VSSA power supplies.

9.8.3.2 Guidelines for Intel® 82562EH Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the HomePNA* LAN interfaces is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HomePNA* LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.8.3.3 Crystals and Oscillators

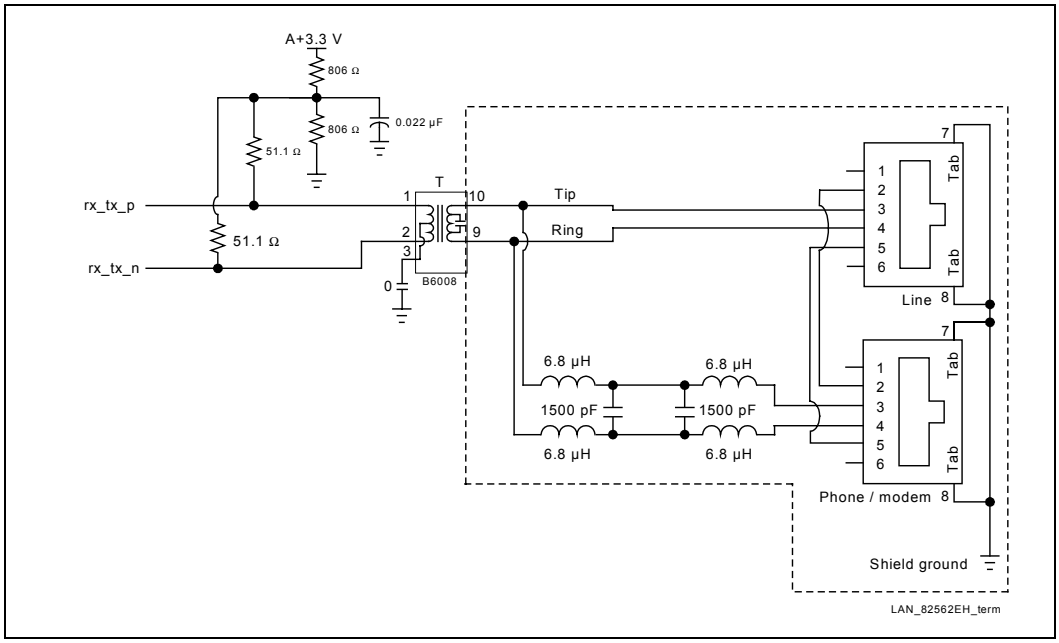
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the HomePNA* magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent radiation from the crystal case, and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise free and stable operation, place the crystal and associated discretes as close as possible to 82562EH, keeping the length as short as possible and do not route any noisy signals in this area.

9.8.3.4 Phoneline HPNA Termination

The transmit/receive differential signal pair is terminated with a pair of 51.1 Ω 1% resistors. This parallel termination should be placed close to the 82562EH. The center, common point between the 51.1 Ω resistors is connected to a pair of 806 Ω resistors and a single 0.022 µF capacitor. The opposite end of one 806 Ω resistor is tied to VCCA (3.3 V), and the opposite end of the other 806 Ω resistor and the cap are connected to ground. The termination is shown in Figure 116.

Figure 116. Intel® 82562EH Termination



The filter and magnetics component T1, integrates the required filter network, high-voltage impulse protection, and transformer to support the HomePNA* LAN interface.

One RJ-11 jack (labeled “LINE” in Figure 116) allows the node to be connected to the phoneline, and the second jack (labeled “PHONE” in Figure 116) allows other downline devices to be connected at the same time. The HomePNA* does not require the second connector. However, typical PCI adapters and PC motherboard implementations are likely to include it for user convenience.

A low-pass filter, setup in-line with the second RJ-11 jack is also recommended by the HomePNA* to minimize interference between the HomeRun connection and a POTS voice or modem connection on the second jack. This places a restriction of the type of devices connected to the second jack as the pass-band of this filter is set approximately at 1.1 MHz. Refer to the HomePNA* website: www.HomePNA.org for up-to-date information and recommendations regarding the use of this low-pass filter to meet HomePNA* certifications.

9.8.3.5 Critical Dimensions

There are three dimensions to consider during layout. Distance ‘B’ from the line RJ11 connector to the magnetics module, distance ‘C’ from the phone RJ11 to the LPF (if implemented), and distance ‘A’ from 82562EH to the magnetics module (See Figure 117).

Figure 117. Critical Dimensions for Component Placement

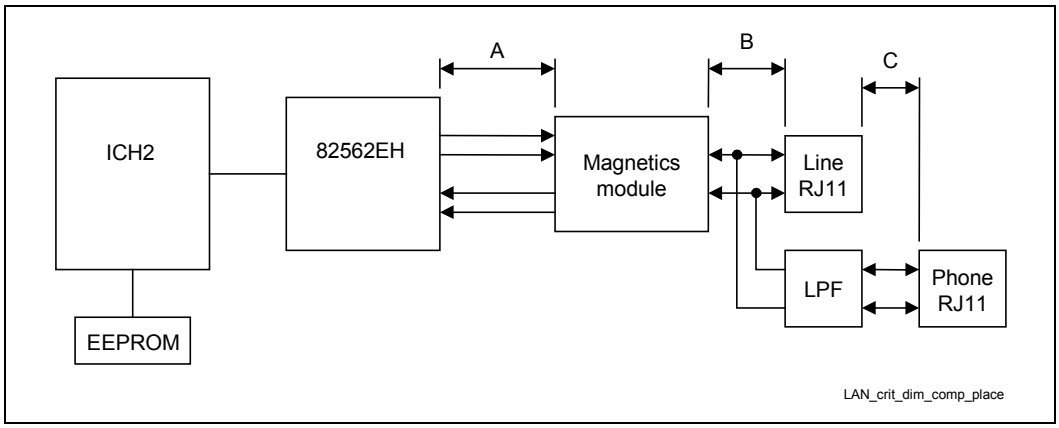


Table 42. Critical Dimension Values

Distance	Priority	Guideline
B	1	< 1 inch
A	2	< 1 inch
C	3	< 1 inch

9.8.3.5.1 Distance from Magnetics Module to Line RJ11

This distance ‘B’ should be given highest priority and should be less than 1 inch. In regards to trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side.

9.8.3.5.2 Distance from Intel® 82562EH to Magnetics Module

Because of the high-speed of signals present, distance ‘A’ between the 82562EH and the magnetics should also be less than 1 inch, but should be second priority relative to distance from connects to the magnetics module.

In general, any section of trace that is intended for use with high-speed signals should observe proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between devices and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself.

9.8.3.5.3 Distance from LPF to Phone RJ11

This distance ‘C’ should be less than 1 inch. In regards to trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side

9.8.4 Intel® 82562ET/EM Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in section 9.8.2, *General LAN Routing Guidelines and Considerations*. Additional guidelines for implementing an 82562ET or 82562EM Platform LAN Connect Components are provided in the following section.

9.8.4.1 Guidelines for Intel® 82562ET/EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.8.4.2 Crystals and Oscillators

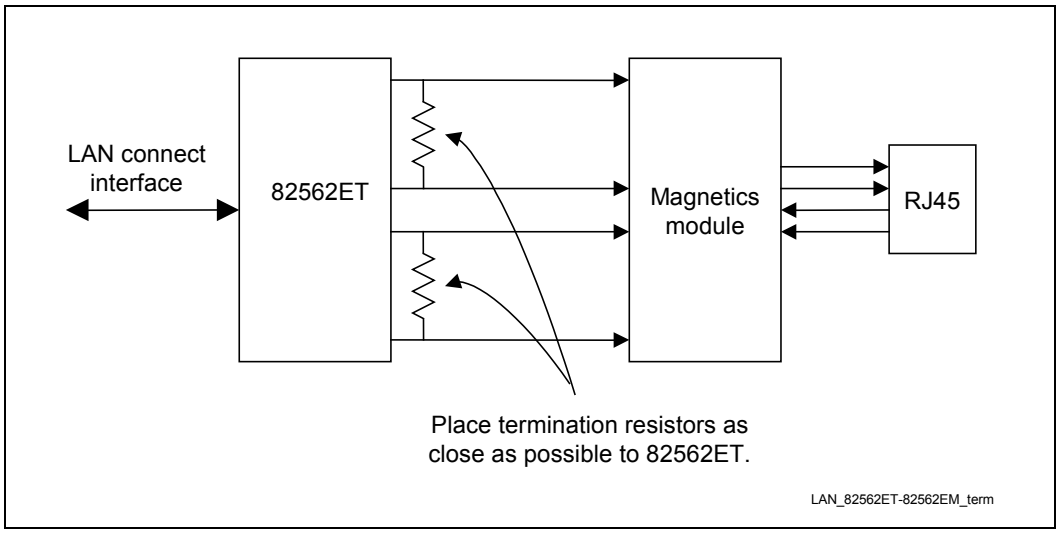
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent radiation from the crystal case, and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562ET or 82562EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

9.8.4.3 Intel® 82562ET/EM Termination Resistors

The 100 Ω 1% resistor used to terminate the differential transmit pairs (TDP/TDN) and the 120 Ω 1% receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN Connect Component (82562ET or 82562EM) as possible. This is because these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

Figure 118. Intel® 82562ET/EM Termination



9.8.4.4 Critical Dimensions

There are two dimensions to consider during layout. Distance ‘B’ from the line RJ45 connector to the magnetics module and distance ‘A’ from the 82562ET or 82562EM to the magnetics module. (See Figure 119)

Figure 119. Critical Dimensions for Component Placement

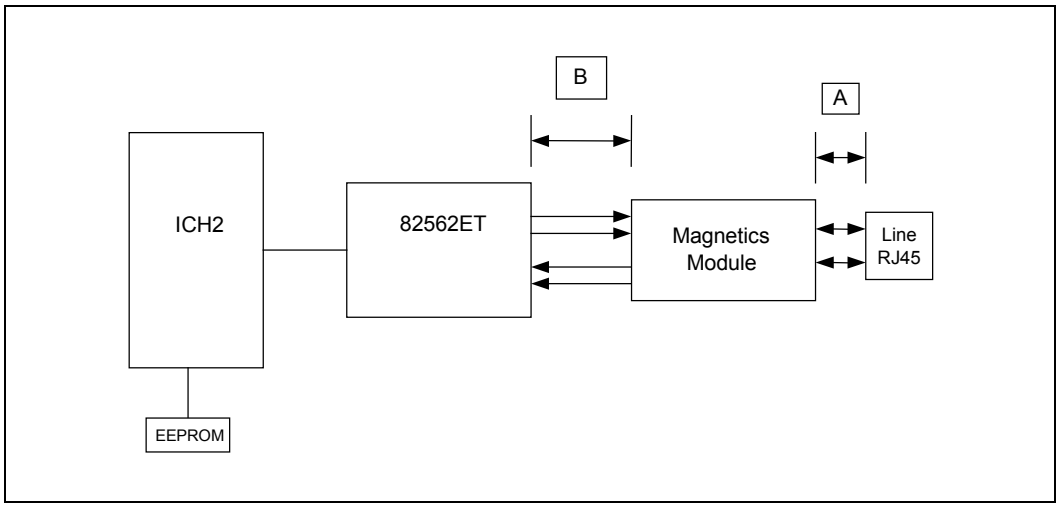


Table 43. Critical Dimension Values

Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

9.8.4.4.1 Distance from Magnetics Module to RJ45

The distance 'A' in Figure 119 should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation.

The following trace characteristics are important and should be observed:

- *Differential Impedance:* The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- *Trace Symmetry:* Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the 82562ET must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562ET and RJ-45 as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 Ω–110 Ω should compensate for second order effects.

9.8.4.4.2 Distance from Intel® 82562ET to Magnetics Module

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and equal length within each differential pair.

9.8.4.5 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems (e.g., analog-to-digital conversion, operational amplifiers, etc). All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Because signals with fast rise and fall times contain many high frequency harmonics, they can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

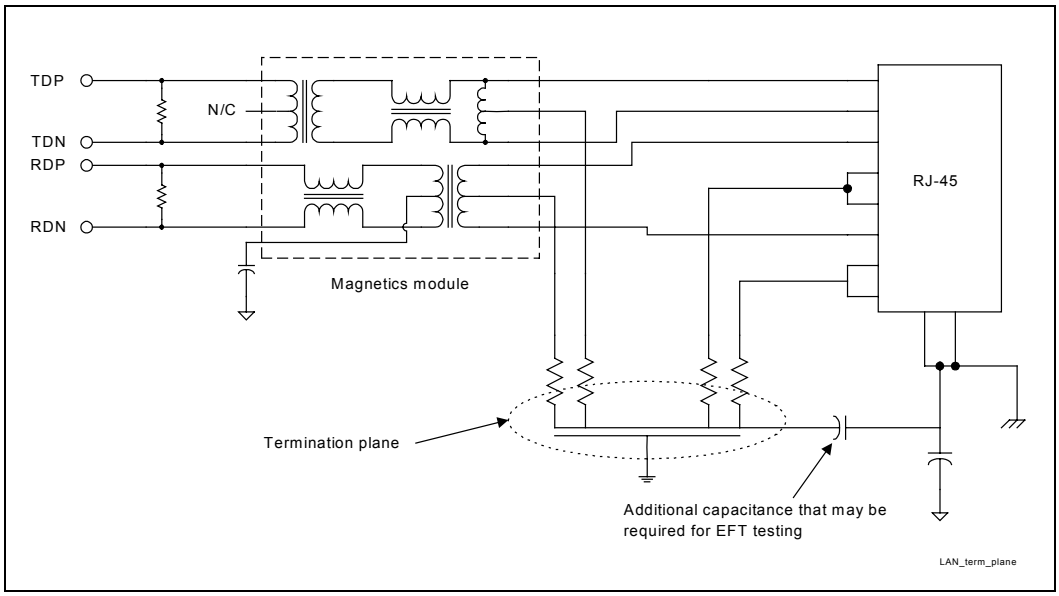
9.8.4.6 Terminating Unused Connections

In Ethernet designs it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

9.8.4.6.1 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 V AC.

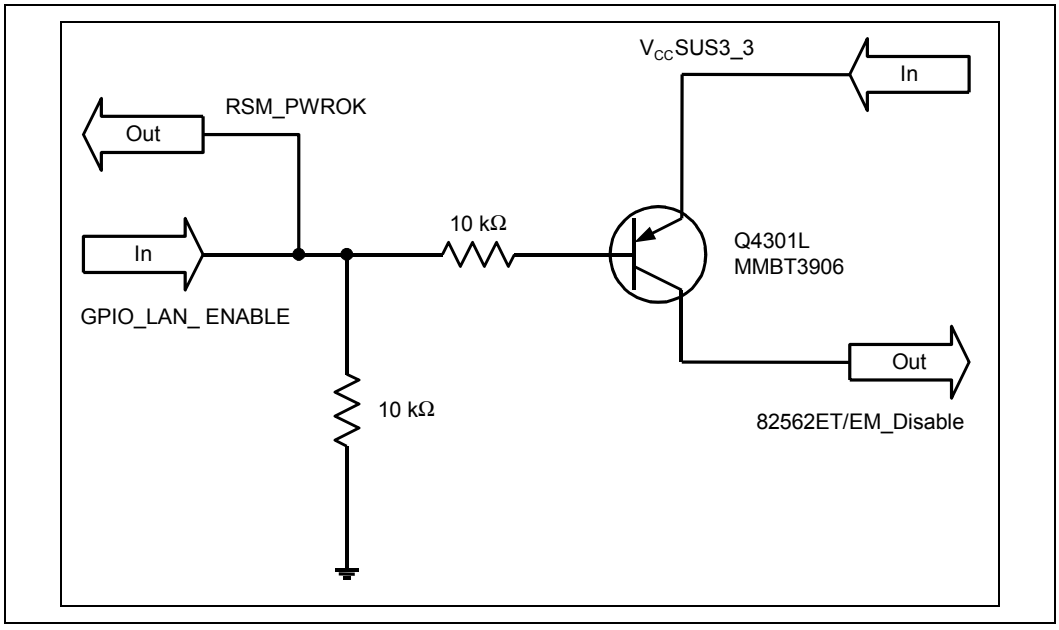
Figure 120. Termination Plane



9.8.5 Intel® 82562 ET/EM Disable Guidelines

To disable the 82562ET/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. BIOS by controlling the GPIO can disable the LAN microcontroller.

Figure 121, Intel® 82562ET/EM Disable Circuit



9.8.6 Intel® 82562ET / Intel® 82562EH Dual Footprint Guidelines

These guidelines characterize the proper layout for a dual footprint solution. This configuration enables the developer to install either the 82562EH or the 82562ET/EM components while having only one motherboard design. The following are guidelines for the 82562ET/ 82562EH Dual Footprint option. The dual footprint for this particular solution uses a SSOP footprint for 82562ET and a TQFP footprint for 82562EH. The combined footprint for this configuration is shown in and Figure 122 and Figure 123.

Figure 122. Dual Footprint LAN Connect Interface

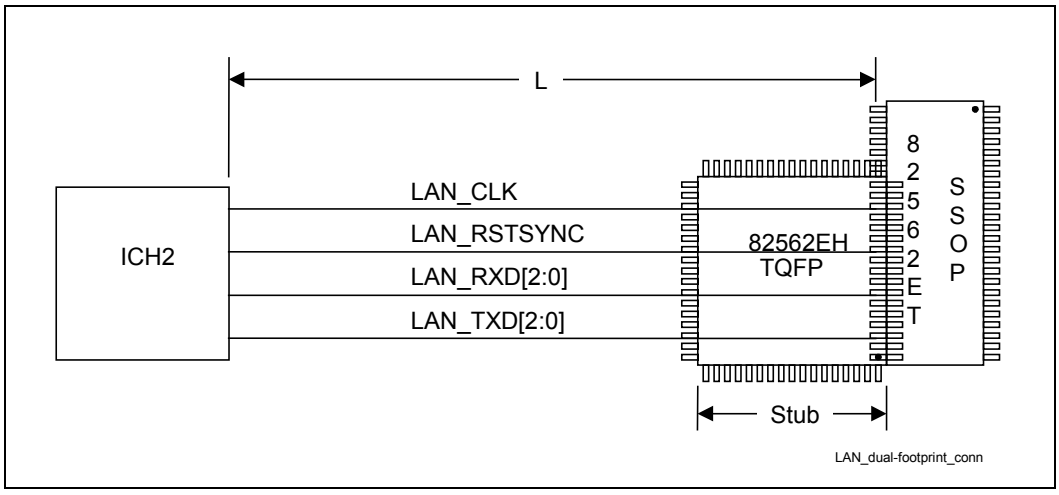
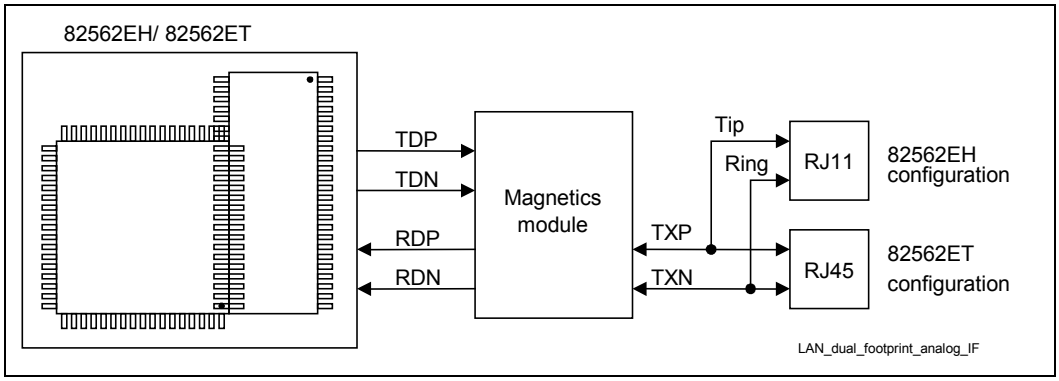


Figure 123. Dual Footprint Analog Interface



The following are additional guidelines for this configuration:

- L = 1.5 inches to 4.5 inches
- Stub < 0.5 inch
- Either 82562EH or 82562ET/EM can be installed. Not both
- The 82562ET pins 28,29, and 30 overlap with 82562EH pins 17,18, and 19.
- Overlapping pins are tied to ground.
- No other signal pads should overlap or touch.
- Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], LAN_TXD[0], RDP, RDN, RXP/Ring, and RXN/Tip are shared by the 82562EH and 82562ET configurations.
- No stubs should be present when 82562ET is installed.
- Packages used for the Dual Footprint are TQFP for 82562EH and SSOP for 82562ET.
- A 22 Ω resistor can be placed at the driving side of the signal line to improve signal quality on the LAN connect interface.
- Resistor should be placed as close as possible to the component.
- Use components that can satisfy both the 82562ET and 82562EH configurations (i.e., magnetics module).
- Install components for either the 82562ET or the 82562EH configuration. Only one configuration can be installed at a time.
- Route shared signal lines such that stubs are not present or are kept to a minimum.
- Stubs may occur on shared signal lines (i.e., RDP and RDN). These stubs are due to traces routed to an uninstalled component. In an optimal layout, there should be no stubs.
- Use 0 Ω resistors to connect and disconnect circuitry not shared by both configurations. Place resistor pads along the signal line to reduce stub lengths.
- Traces from magnetics to connector must be shared and not be stubbed. An RJ-11 connector that fits into the RJ-45 slot is available. Any amount of stubbing will destroy both HomePNA* and Ethernet performance.

9.9 FWH Guidelines

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the FWH BIOS Specification or equivalent.

9.9.1 FWH Decoupling

A 0.1 µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the Vcc supply pins.

9.9.2 In Circuit FWH Programming

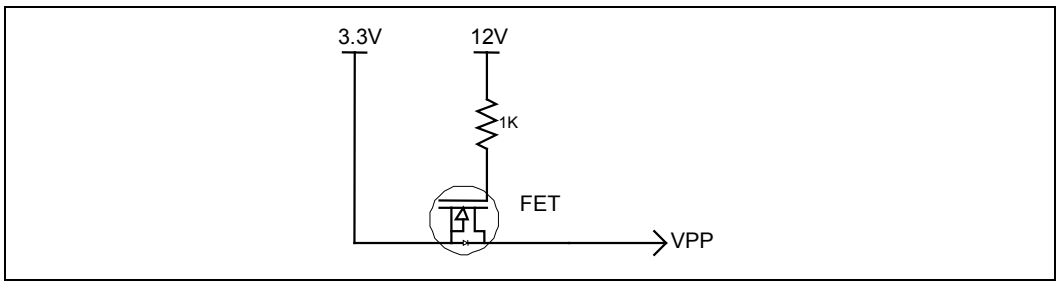
All cycles destined for the FWH will appear on PCI. The ICH2 hub interface to PCI Bridge will put all CPU boot cycles out on PCI (before sending them out on the FWH interface). If the ICH2 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from of a PCI card that positively decodes these memory cycles. In order to boot off a PCI card, it is necessary to keep the ICH2 in subtractive decode mode. If a PCI boot card is inserted and the ICH2 is programmed for positive decode, there will be two devices positively decoding the same cycle. In systems with the 82380AB (ISA bridge), it is also necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot off a ROM behind the 82380AB. Once you have booted from the PCI card, you could potentially program the FWH in circuit and program the ICH2 CMOS.

9.9.3 FWH Vpp Design Guidelines

The Vpp pin on the FWH is used for programming the flash cells. The FWH supports Vpp of 3.3V or 12V. If Vpp is 12V the flash cells will program about 50% faster than at 3.3V. However, the FWH only supports 12V Vpp for 80 hours. The 12V Vpp would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The VPP pin MUST be tied to 3.3V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 124, FWH VPP Isolation Circuitry



9.10 Intel® ICH2 Decoupling Recommendations

The ICH2 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in the table below to ensure the components maintain stable supply voltages. Also the capacitors should be placed as close to the package as possible. Maximum distance allowed is 400 mils. It is recommended that the motherboard designer include pads for extra decoupling caps should the recommendation not work on their board.

Table 44. Decoupling Capacitor Recommendation

Power Plane	# Decoupling Capacitors	Capacitor Value
3.3 V Core	6	0.1 µF
3.3 V Stand By	1	0.1 µF
VCC_CPU	1	0.1 µF
1.8 V Core	2	0.1 µF
1.8 V Stand By	1	0.1 µF
5 V Reference	2	0.1 µF and 1 µF
5 V Reference Stand By	1	0.1 µF

9.11 Glue Chip 3 (Intel® ICH2 Glue Chip)

To reduce the component count and bill of material (BOM) cost of the Intel 860 chipset based-platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The Glue Chip 3 is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Glue Chip 3 Features:

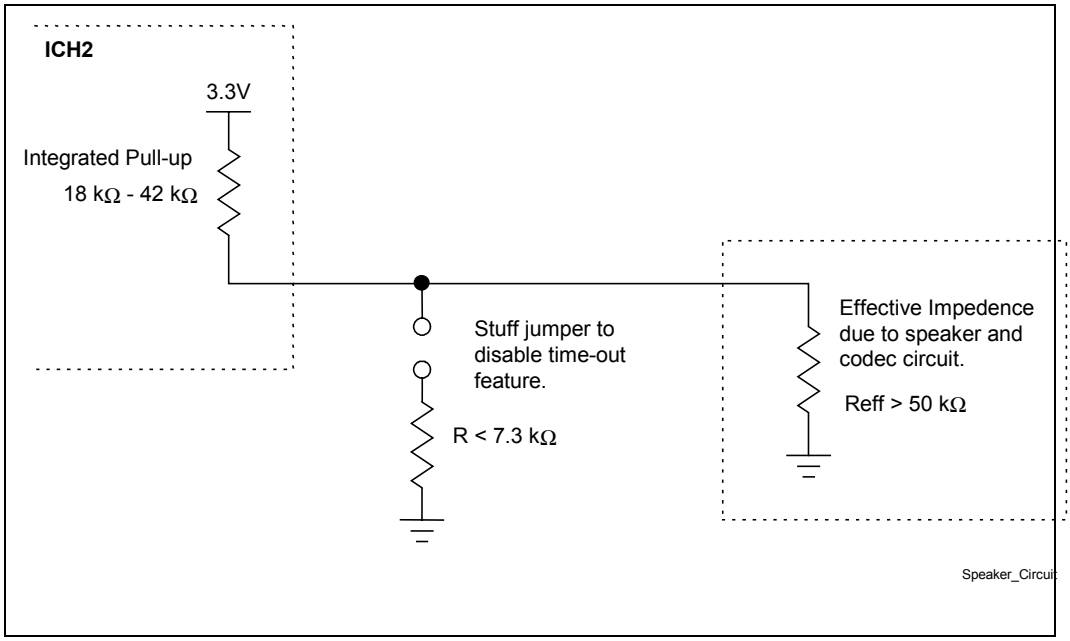
- PWROK signal generation
- Control circuitry for *Suspend To RAM*
- Power Supply power up circuitry
- RSMRST# generation
- Backfeed cutoff circuit for *Suspend-to-RAM*
- 5 V reference generation
- Flash FLUSH# / INIT# circuit
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- Voltage translation for Audio MIDI signal
- Audio-disable circuit
- Voltage translation for DDC to monitor
- Tri-state buffers for test.

Note: Contact your local Intel representative to obtain the necessary documents for the discrete solution of the Glue Chip 3.

9.12 SPKR Pin Consideration

The effective impedance of the speaker and codec circuitry on the SPKR signal line must be greater than 50 kΩ. Failure to due so will cause the TCO Timer Reboot function to be erroneously disabled. SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of POWEROK. When enabled, the ICH2 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-up resistor (the resistor is only enabled during boot/reset). Therefore, it's default state when the pin is a "no connect" is a logical one, or enabled. To disable the feature, a jumper can be populated to pull the signal line low (see the following figure). The value of the pull-down must be such that the voltage divider caused by the pull-down and integrated pull-up resistors will be read as logic low. When the jumper is not populated, a low can still be read on the signal line if the effective impedance due to the speaker and codec circuit is equal to or lower than the integrated pull-up resistor. It is therefore strongly recommended that the effective impedance be greater than 50 kΩ and the pull-down resistor be less than 7.3 kΩ.

Figure 125, SPKR Circuit



9.13 1.8 V and 3.3 V Power Sequence Requirement

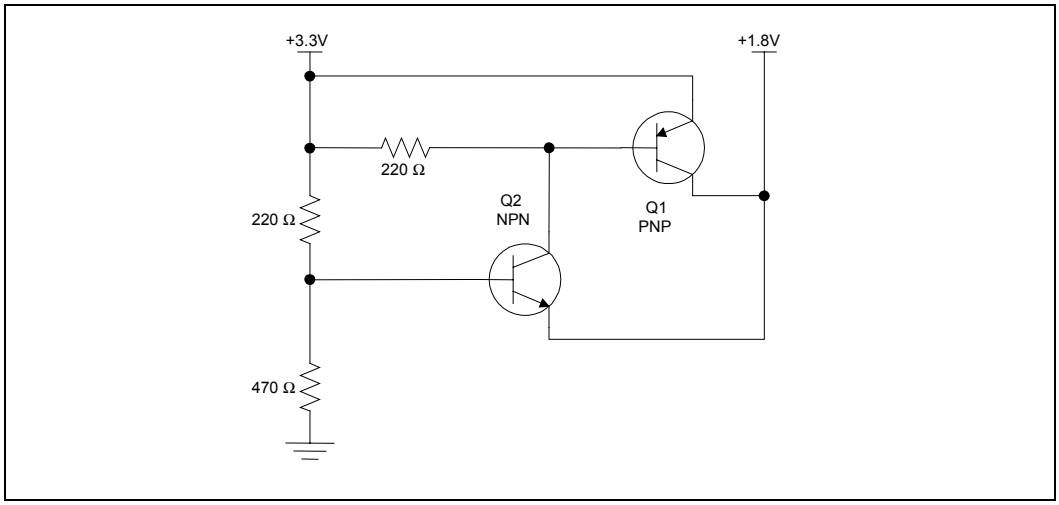
The ICH2 has two pairs of associated 1.8 V and 3.3 V supplies. These supplies are Vcc1.8 and Vcc3.3, and VccSus1.8 and VccSus3.3. These pairs are assumed to power up and power down together. The difference between the two associated supplies must never be greater than 2.0V. The 1.8 V supply may come up before the 3.3 V supply without violating this rule (though this is generally not practical in a desktop environment, since the 1.8 V supply is typically derived from the 3.3 V supply by means of a linear regulator).

One serious consequence of violation of this "2V Rule" is electrical overstress of oxide layers, possibly resulting in component damage.

The majority of the ICH2 I/O buffers are driven by the 3.3 V supplies, but are controlled by logic that is powered by the 1.8 V supplies. If the 3.3 V supply powers up first, the I/O buffers will be in an undefined state until the 1.8 V logic is powered up. Some signals that are defined as "Input-only" actually have output buffers that are normally disabled, and the ICH2 may unexpectedly drive these signals if the 3.3 V supply is active while the 1.8 V supply is not.

The following figure is an example power-on sequencing circuit that ensures the 2V Rule is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.8 V supply tracks the 3.3 V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.8 V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8 V plane, current will not flow from the 3.3 V supply into 1.8 V plane when the 1.8 V plane reaches 1.8 V.

Figure 126, Example Power-On 3.3 V / 1.8 V Sequencing Circuit



When analyzing systems that may be “marginally compliant” to the 2 V Rule, pay close attention to the behavior of the I’H2's RSMRST# and PWROK signals, since these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the Resume wells.
- PWROK controls isolation between the Resume wells and Main wells
- LAN_PWROK controls isolation between the LAN wells and the Resume wells

If one of these signals goes high while one of its associated power planes is active and the other is inactive, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging internal currents.

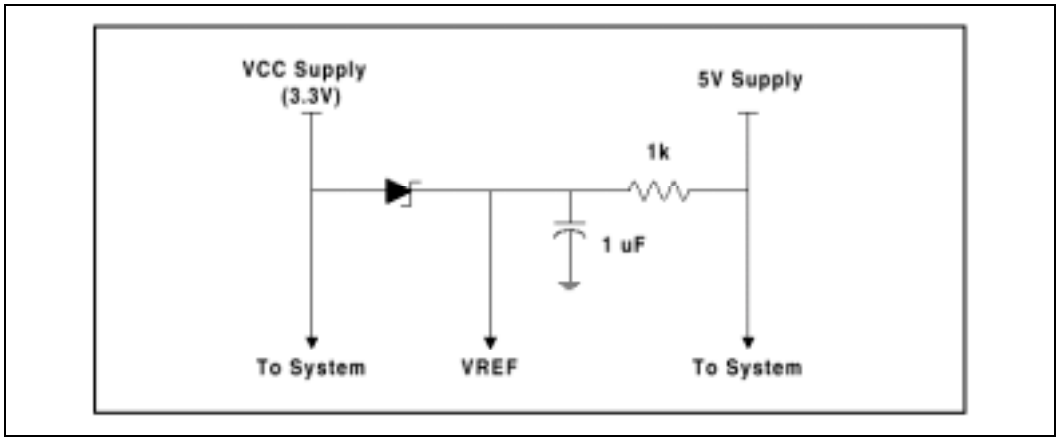
9.14 ICH2 V5REF and VCC3_3 Sequencing Requirement

V5REF is the reference voltage for 5V tolerance on inputs to the ICH2. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within .7V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within .7V. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 127 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend, the only signals that are 5V tolerant capable are USB OC:[3:0]#. If these signals are not needed during suspend, V5REF_SUS can be connected to either VccSus3_3 or 5V_Always/5V_AUX. If OC:[3:0]# is needed during suspend and 5V tolerance is required then V5REF_SUS should be connected to 5V_Always/5V_AUX, but if 5V tolerance is not needed in suspend, then V5REF_SUS can be connected to either VccSus3_3 or 5V_Always/5V_AUX rails.

Figure 127. Example 3.3V/V5REF Sequencing Circuitry



9.15 PIRQ Routing

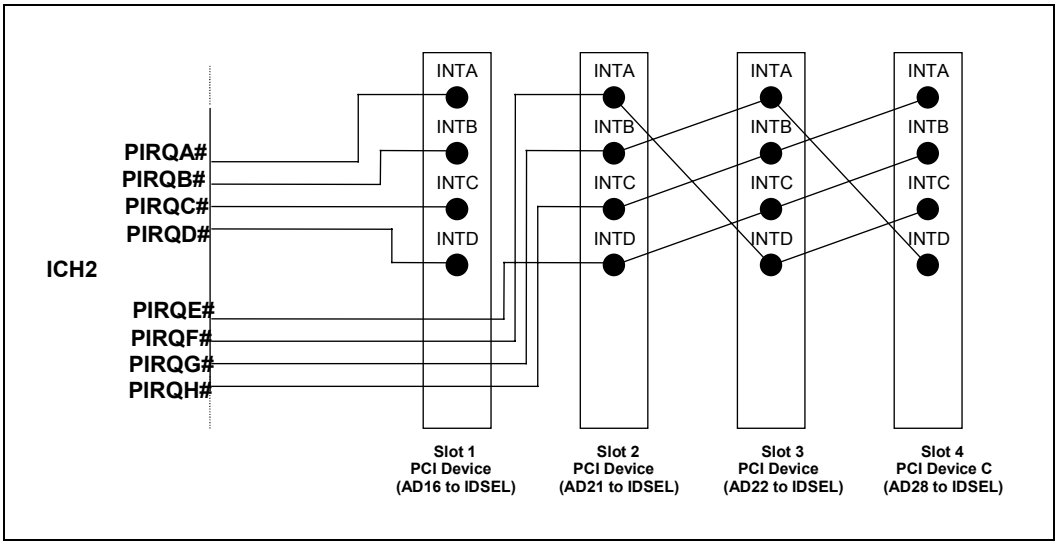
PCI interrupt request signals E–H are new to the ICH2. These signals have been added to lower the latency caused by having multiple devices on one interrupt line. With these new signals, each PCI slot can have an individual PCI interrupt request line (assuming that the system has four PCI slots). Table 45 shows how the ICH2 uses the PCI IRQ when the I/O APIC is active.

Table 45. IOAPIC Interrupt Inputs 16 Through 23 Usage

No	IOAPIC INTIN PIN	Function in ICH2 using the PCI IRQ in IOAPIC
1	IOAPIC INTIN PIN 16 (PIRQA)	
2	IOAPIC INTIN PIN 17 (PIRQB)	AC'97, Modem and SMBUS
3	IOAPIC INTIN PIN 18 (PIRQC)	
4	IOAPIC INTIN PIN 19 (PIRQD)	USB Controller #1
5	IOAPIC INTIN PIN 20 (PIRQE)	Internal LAN Device
6	IOAPIC INTIN PIN 21 (PIRQF)	
7	IOAPIC INTIN PIN 22 (PIRQG)	
8	IOAPIC INTIN PIN 23 (PIRQH)	USB Controller #2 (starting from ICH2 B0 silicon)

Interrupts B, D, E, and H service devices internal to the ICH2. Interrupts A, C, F, and G are not used and can be used by PCI slots. The figure below shows an example of IRQ line routing to the PCI slots.

Figure 128. Example PCI IRQ Routing



The PCI IRQ Routing shown in the previous figure allows the ICH2 internal functions to have a dedicated IRQ (Assuming add-in cards are single function devices and use INTA). If a P2P bridge card or a multifunction device uses more than one INTn# pin on the ICH2 PCI Bus, the ICH2 internal functions will start sharing IRQs.

The previous figure is an example. It is up to the board designer to route these signals in a way that is the most efficient for their particular system. A PCI slot can be routed to share interrupts with any of the ICH2's internal device/functions.

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10 EMI Design Guidelines

As microprocessor amperage and speeds increase, the ability to contain electromagnetic radiation becomes more difficult. Frequencies generated by the processor are in the gigahertz (GHz) range, which impacts both the system design, and electromagnetic interference (EMI) test methodology.

This chapter provides information that is intended to help electrical and mechanical design engineers develop Intel Xeon based systems that meet government EMI regulations. The chapter describes heat sink grounding, processor shielding, differential and spread spectrum clocking and the test methodology impact on FCC Class B requirements.

Designers should be aware that implementation of recommendations in this guideline does not guarantee compliance to EMI regulations. These guidelines may help reduce the emissions from processors and motherboards, and may make chassis design easier.

10.1 Terminology

Electromagnetic Interference (EM–) - electromagnetic radiation from an electrical source that interrupts the normal function of an electronic device.

Electromagnetic Compatibility (EM–) - the successful operation of electronic equipment in its intended electromagnetic environment.

10.2 Basic EMI Theory

Electromagnetic energy transfer can be viewed in four ways:

- Radiated emissions
- Radiated susceptibility
- Conducted emissions
- Conducted susceptibility.

For PC systems, designers achieve EMC compliance by reducing radiated and conducted emissions. Susceptibility is typically not a major concern in the desktop PC environment, but may be more important in an industrial environment.

The main component of EMI is a radiated electromagnetic wave that consists of both electric (E-field) and magnetic (H-field) waves traveling together and oriented perpendicular to each other. Although E and H fields are intimately tied together, they are generated by different sources.

The following are characteristics of E and H fields:

- E-fields are created by voltage potentials
- H-fields are created by current flow.
- In a steady state environment (where voltage and current is unchanging), E and H fields are static and do not generate EMI.
- Changing voltages and currents do generate EMI.
- If a dynamic E-field is present, there must be a corresponding dynamic H-field, and vice versa.
- Motherboards with fast processors generate high frequency E and H fields from currents and voltages present in the component silicon and in signal traces.

Two methods exist for minimizing E and H field emissions from a system: prevention, and containment.

Prevention is achieved by implementing design techniques that minimize generation of EMI fields. Containment is used in a chassis environment to contain radiated energy within the chassis. Proper board layout, trace routing and grounding may significantly reduce motherboard radiated emissions and make the chassis design easier.

10.3 EMI Regulations and Certifications

Personal Computer Original Equipment Manufacturers (PC OEMs) ensure EMC compliance by meeting EMI regulatory requirements. PC designers must ensure that their computer systems do not exceed the emission limit standards set by applicable regulatory agencies. Regulatory requirements referenced in this document include:

- United States Federal Communication Commission (FCC) Part 15 Class B
- International Electrotechnical Commiss'on's International Special Committee on Radio Interference (CISPR) Publication 22 class B limits

The FCC rules are interpreted to require any PC OEM that sells an "off-the-shelf" motherboard in the United States to pass an open chassis test. The purpose of this regulation is to ensure that system boards have reasonable emission levels since they are one of the main contributors to EMI. Open chassis testing is defined as removing the chassis cover (or top and 2 sides) and testing for EMI compliance (although permitted emission levels are allowed to be higher). Removing the cover greatly reduces the shielding provided by the chassis, and increases the amount of EMI radiation.

10.4 EMI Design Considerations

The following sections describe design techniques that can be used to minimize EMI emissions. Some ideas have been incorporated into Intel® enabled designs (differential clock drivers, selective clock gating, etc.), and some must be implemented by motherboard designers (trace routing, clocking schemes, etc.).

10.4.1 Spread Spectrum Clocking (SSC)

Spread Spectrum Clocking (SSC) is defined as continuously ramping (or modulating) the processor clock frequency over a predefined range (see Figure 129). SSC reduces radiated emissions by spreading the radiated energy over a wider frequency band (see Figure 130). Thus, instead of maintaining a constant clock frequency, SSC modulates the clock frequency along a predetermined path (or modulating profile) with a predetermined modulation frequency. The modulation frequency is usually selected to be higher than 30 kHz (above the audio band), but low enough to avoid violating the PC system timing requirements (less than 0.8% of the nominal clock frequency). SSC has been demonstrated to effectively reduce peak radiation levels, making EMC compliance easier to achieve.

To conserve the minimum period requirement for bus timing, the SSC clock is modulated between *fnom* and *(1-d) fnom*, where *fnom* is the nominal frequency for a constant frequency clock. *d* specifies the total amount of spreading as a relative percentage of *fnom*. The modulation percentage is always a function of *1-d* and not *1+d* because increasing the clock frequency above the rated speed of the processor causes unpredictable operation.

Figure 129. Spread Spectrum Modulation Profile

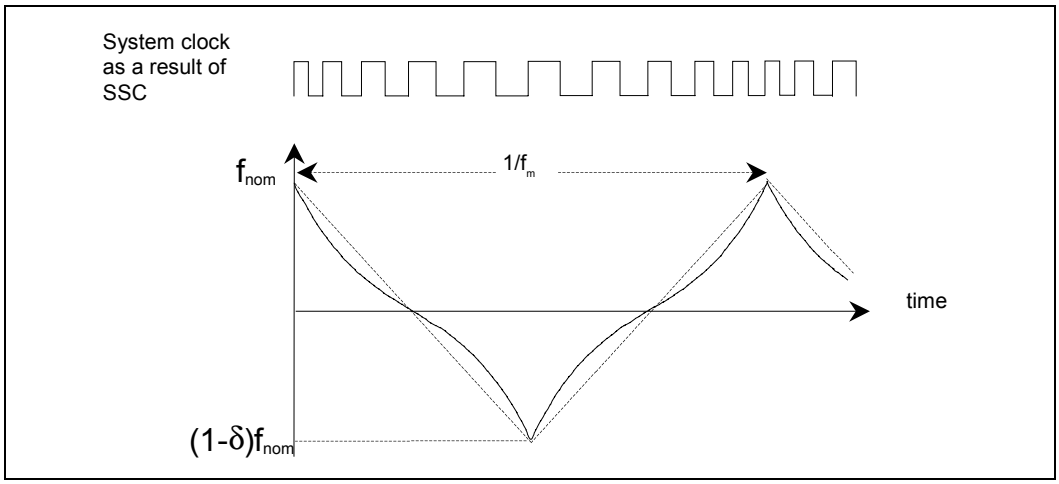
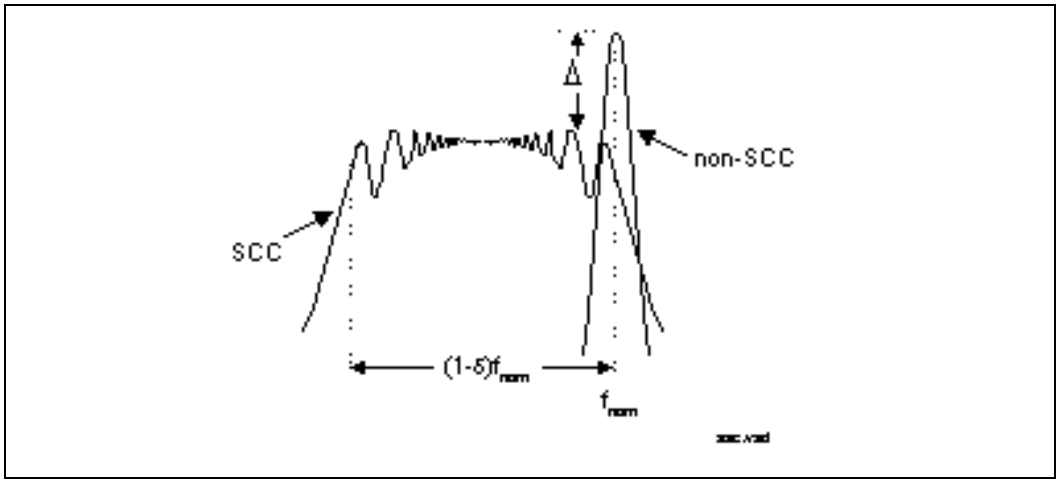


Figure 130. Impact of Spread Spectrum Clocking on Radiated Emissions

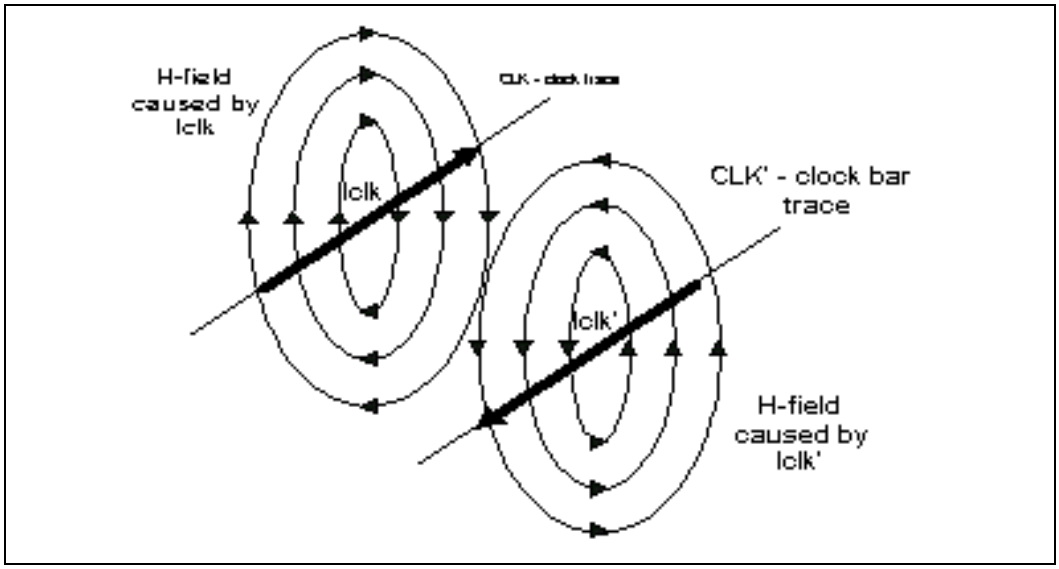


10.4.2 Differential Clocking

Differential clocking requires that the clock generator supply both clock and clock-bar traces. Clock-bar has equal and opposite current as the primary clock, and is 180° out of phase with the primary clock. To maximize the benefit of differential clocking, both clock lines must be routed parallel to each other for their entire length. Devices connected to the clock must also be designed to accept both the clock, and clock-bar signals.

Differential clocking reduces EMI because of H-field cancellation. Since H-field orientation is generated by and depends on current flow, the H fields of two equal currents flowing in opposite directions and 180 degrees out of phase are cancelled (see Figure 131), and lower H-fields reduce EMI radiation.

Figure 131. Cancellation of H-fields Through Inverse Currents



Differential clocking can also reduce the amount of noise coupled to other traces, which improves signal quality and reduces EMI. I/O signals are particularly important because they often leave the system chassis (serial and parallel ports, keyboards, mouse, etc.) and radiate noise that has been induced onto them.

A single-ended cl'ck's return path is usually a reference plane, which is shared by other signals/traces. When noise is created on a single-ended clock, the noise appears on the reference plane and may be coupled to I/O traces. A differential cl'ck's return path is the clock-bar signal/trace, which is more isolated than the reference plane and minimizes potential I/O trace coupling.

For best results, the trace lengths and routing of the clock lines must be closely matched, and spacing between the two traces should be kept as small as possible. This minimizes loop area and maximizes H-field cancellation. In addition, the real and parasitic terminations of each signal of a differential pair should be the same, and the skew between the signal level transitions on the two lines must be small compared to the rise time of the level transitions.

Placing ground traces on the outside of the differential pair may further reduce emissions. Intermediate vias to ground may be needed to reduce re-radiation from the ground traces themselves. The distance between vias should be less than ¼ of a wavelength of th^{e} 5th harmonic of the processor core frequency.

10.4.3 PCI Bus Clock Control

Experimental data indicates that a reduction in EMI may be possible by disabling the clocks to unused (and therefore unterminated) PCI slots. CK00, the clock chip that has been specified and designed for this platform, supports individual control of the various PCI clocks. Designers have the option of enabling or disabling individual PCI clocks depending on specific system configuration requirements. Refer to the *CK00 Clock Synthesizer Design Guidelines* for details on how to configure the PCI clocks.

10.4.4 Heat Sink Effects

Heat sink grounding may be an effective way to reduce system EMI emissions. Noise coupled from the processor package to the heat sink may cause the heat sink to act as an antenna and re-radiate the noise. Heat sink size, shape, fin pattern, orientation, and material may all affect the heat sink's noise re-radiation. Designers must experimentally investigate the behavior of a particular heat sink to determine its EMC performance.

Grounding of the heat sink through the Intel processor package is not possible with the current package implementation, but may be an option at some time in the future. Therefore, OEMs must design their own heat sink grounding solutions.

When designing a grounding mechanism for the heat sink, care must be taken to minimize the impedance and distance between the ground paths. Typical guidelines suggest that ground points should be separated by less than ¼ wavelength of th^{e} 3rd harmonic of the processor core frequency.

Grounding materials should be selected to eliminate galvanic action between the various metals with which they will be in contact. Oxidation of the various materials should also be considered because some oxides are non-conductive (for example, aluminum oxide) and degrade EMC performance over time. Manufacturing process residue or coatings that prevent oxidation should also be checked for conductivity, especially at high frequencies.

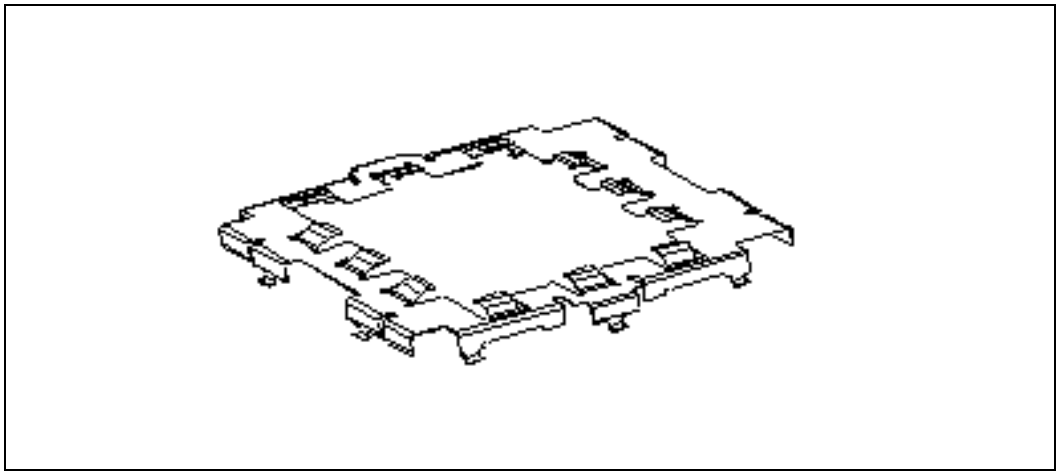
10.4.5 Faraday Cages

Grounding of heat sinks may reduce EMI, but that alone may not be sufficient to pass the required EMI tests. Additional shielding of the processor itself may be necessary. A Faraday cage placed around the processor may provide a reduction in radiated noise and make chassis design easier.

A true Faraday cage completely surrounds the source of radiation and contains all radiated energy. Because of limitations of processor packaging and motherboard assembly, it is not possible to create a true Faraday cage around the processor. A reasonable approximation of a Faraday cage around the processor can be achieved by using the heat sink and motherboard ground plane as two sides of the cage, and using a metal frame that encloses the remaining four sides.

Intel has designed‘a 'picture fr’me' type of grounding device that fits between the processor and heat sink (see Figure 132). With this implementation, it is unnecessary to design a separate heat sink grounding mechanism because the frame provides this capability. OEMs that choose to use the Intel-designed grounding frame must provide ground pads on the top layer of the motherboard around the processor socket. These pads provide the necessary ground continuity to complete the Faraday cage. The required motherboard ground pad descriptions are provided in Chapter 11.

Figure 132. Intel® Xeon™ Processor Ground Frame



10.4.6 EMI Test Capabilities

FCC regulations in the United States specify that the maximum test frequency for products with clocks with frequencies higher than 1 GHz is either 5 times the highest clock frequency or 40 GHz, which ever is lower. OEMs are advised to enquire into the capabilities of their preferred EMC test lab to ensure that they are able to scan to the required frequency.

History indicates that processor performance and frequency double approximately every 2 years. With this in mind, it is advisable to be prepared for the frequencies that must be scanned in the next few years.

Since the FCC Rules ultimately require testing to 40 GHz, commercial test equipment has been developed that is capable of making measurements at that frequency. Although it will be some time before processors require testing at this frequency, it may be cheaper to upgrade to 40 GHz now, rather than upgrading in several intermediate steps.

It is also possible to upgrade various parts of the test equipment at different times. For example, the spectrum analyzer may be upgraded to 40 GHz today while using only the antennas necessary to support the initial processor frequencies. Antennas and cables can then be purchased when necessary as processor speed increases. Cost flexibility in antenna selection is probably the greatest because different antenna designs are necessary for different frequency ranges.

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11 Mechanical and EMI Design Considerations

11.1 Retention Mechanism Placement and Keepouts

The retention mechanism (RM) (illustrated in Figure 133) requires two keepout zones: one for the EMI ground pads and another for a limited component height area under the RM as shown in Figure 134 shows the relationship between the RM mounting holes and pin one of the socket. In addition it also documents the ground pads and keepouts. Figure 135 details the ground pad locations and the associated limited height areas due to the ground frame.

The EMI ground pads under the retention mechanism should have a minimum of 8 vias connecting the pad to the baseboard ground plane. The retention holes should be a non-plated hole.

The ground pads for the EMI ground frame should have a minimum of 6 vias each connecting the pads to the ground plane. The suggested via size is 0.012 inches. This should allow sufficient clearance to route traces between the vias on the secondary side of the PB or on internal layers.

In the event of conflict, information in the *Intel® Xeon™ Processor at 1.40 GHz, 1.50 GHz, 1.7 GHz and 2 GHz Datasheet* supercedes this information.

Figure 133. Retention Mechanism Keepout Outline

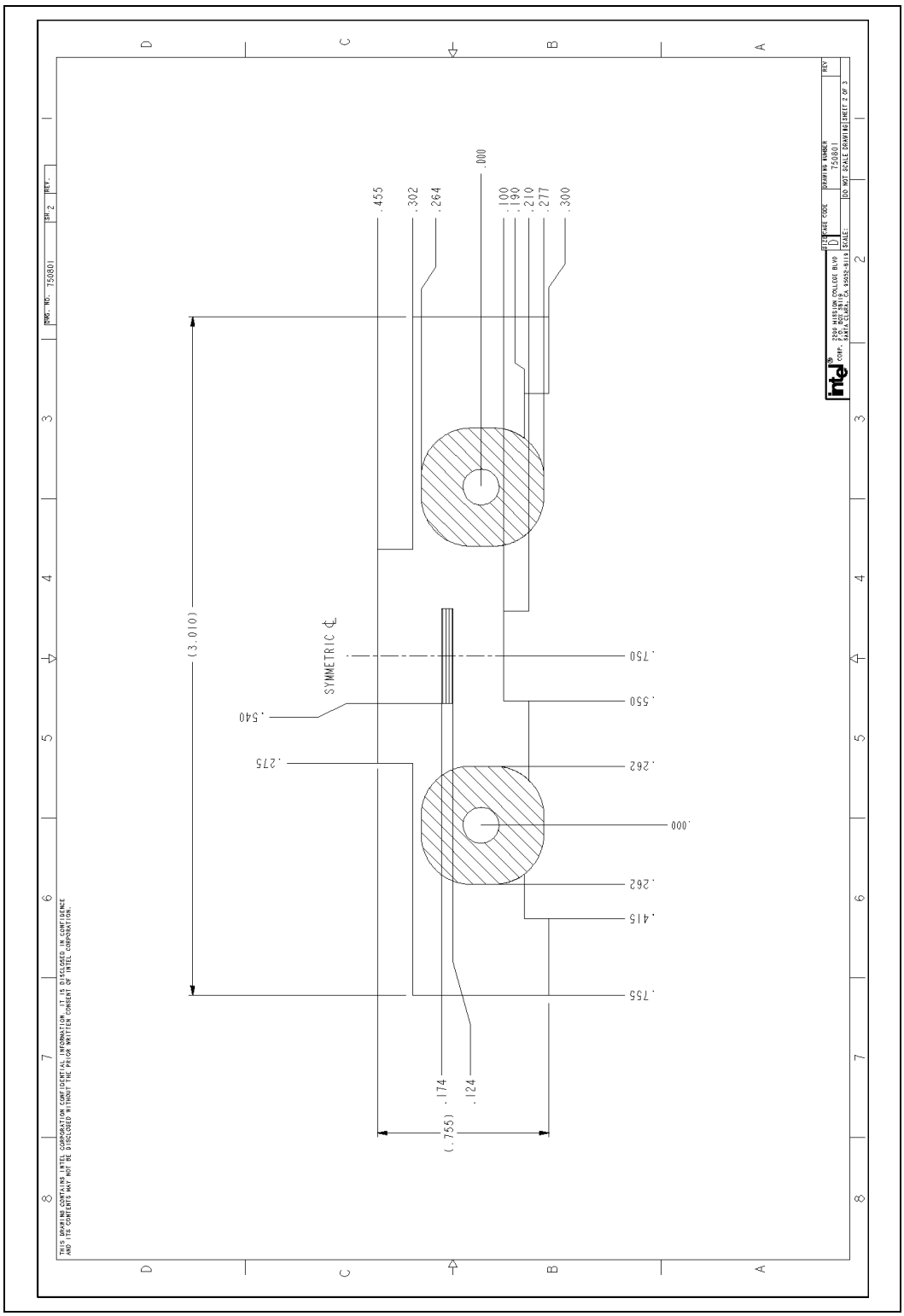
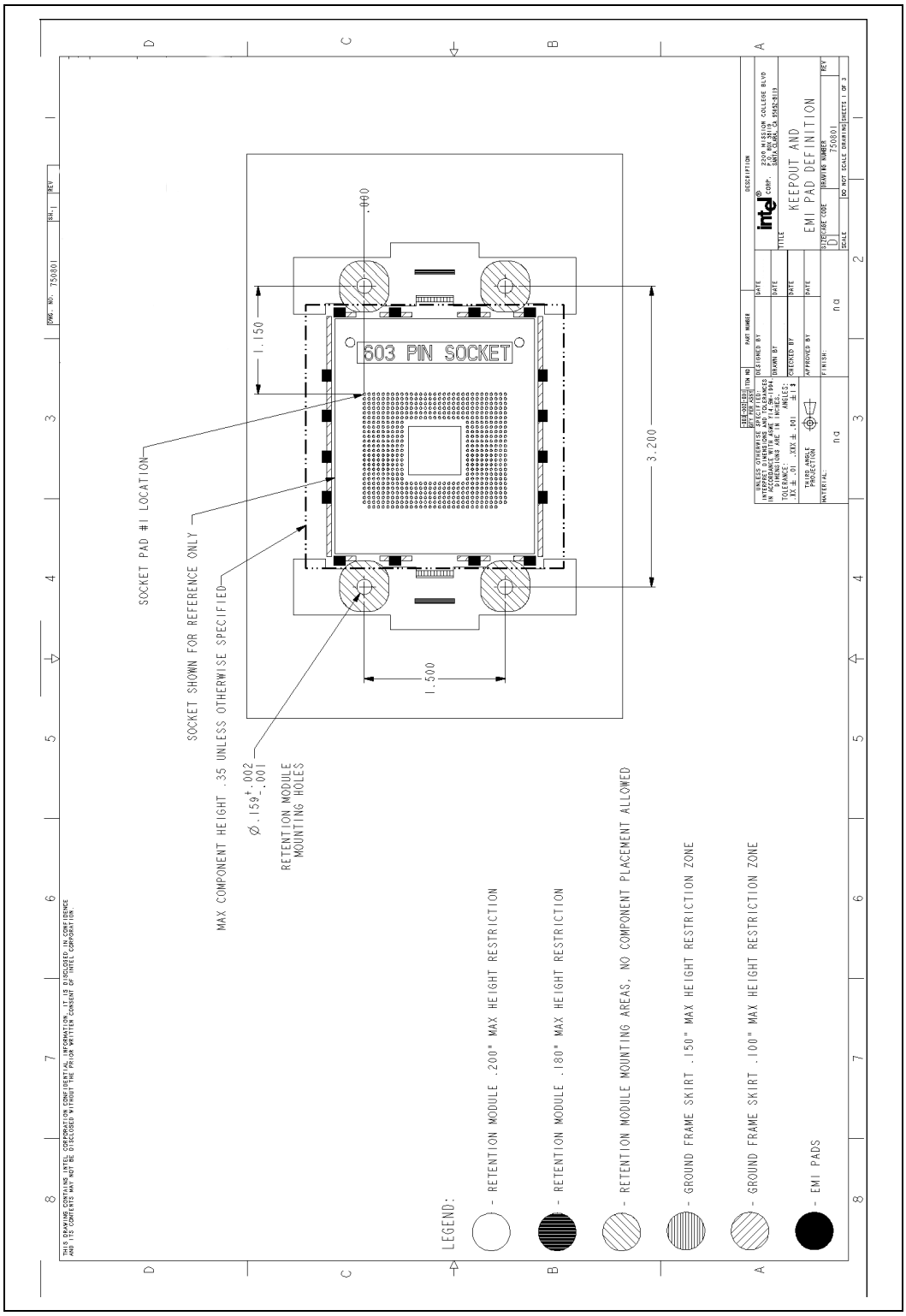


Figure 134. Retention Mechanism Placement and Keepout Overview



11.2 Electromagnetic Interference Considerations

In an effort to be proactive regarding electromagnetic interference (EMI) reduction, Intel has a reference design for a processor EMI ground frame for this platform. The solution is a metal grounding frame that contacts the heatsink on two sides and provides grounding to the motherboard. See the *Intel Xeon Processor Enabled Components ProE Files* or the *Intel® Xeon™ Processor Enabled Components IGES Files* for details.

The processor EMI ground frame is meant to provide grounding of AC currents seen on the heatsink and has been shown to be the most effective design in EMI reduction for the processor. The metal frame will be installed after the processor and retention mechanisms have been inserted. It fits around the processor and inside of the retention mechanisms. Fingers on the top of the metal frame will provide contact to the heatsink, and fingers along the bottom will contact the ground pads on the motherboard. The grounding frame will require the placement of a series of ground pads surrounding the processor, as shown in Figure 135. Anodizing or any form of insulated coating on the heat sink is strongly discouraged when implementing the EMI ground frame.

If ground pads for the retention mechanism are desired, the following is a set of recommendations for their implementation:

- All four RM mounting holes should have ground pad rings.
- Ground pad annular ring should be no less than 125 mil wide. Try to cover the entire keep out zone, if possible. See the following illustration for better dimensions.
- Place 8-12 vias in the annular ring, which connects the pad to internal ground planes.

Refer to Figure 136 for specific details regarding the ground pads that are required to utilize this reduction technique.

Figure 135. EMI Ground Pad Size and Locations

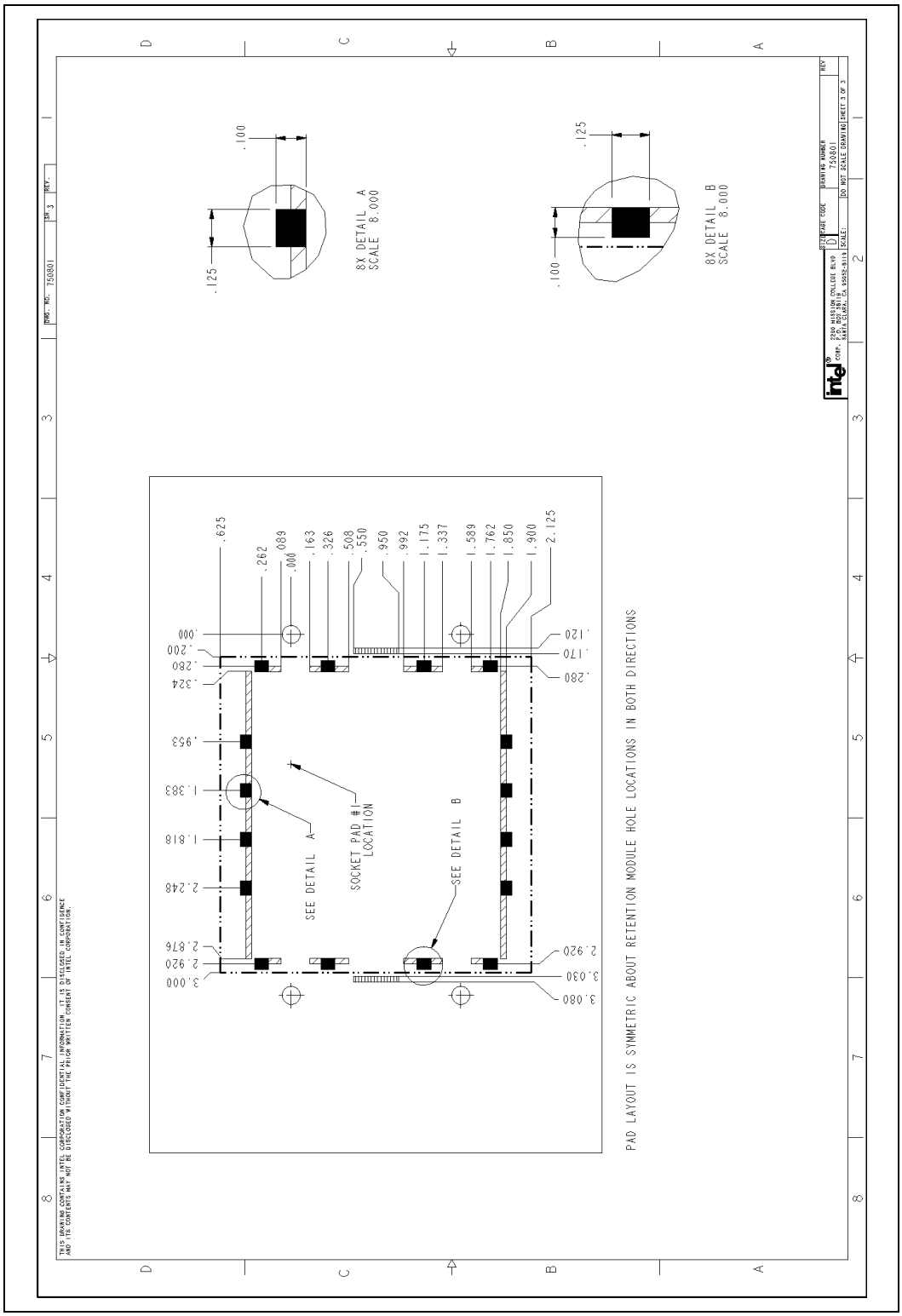
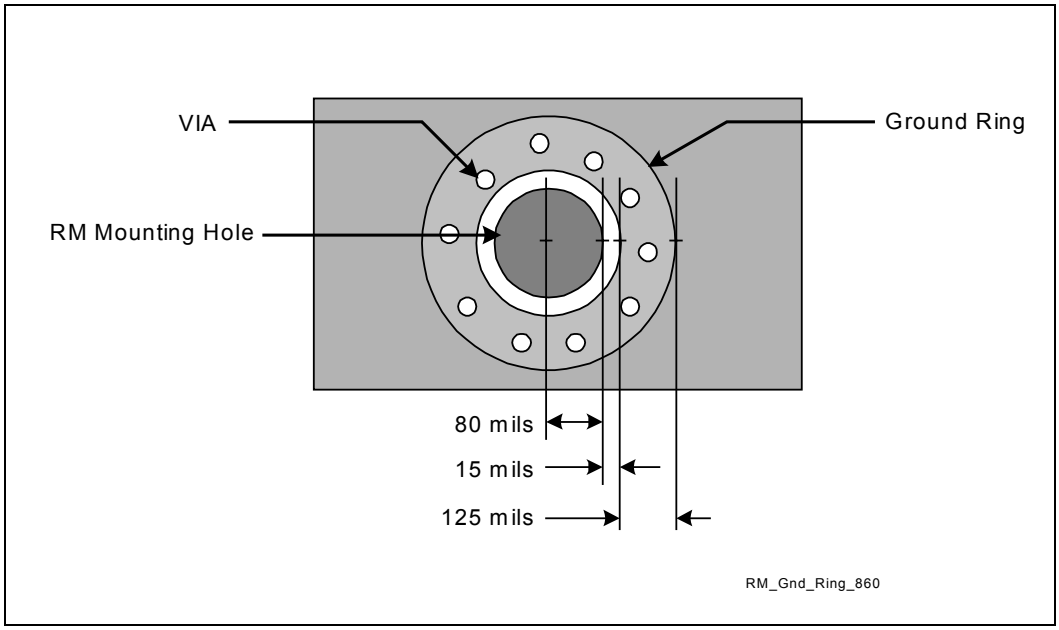


Figure 136. Retention Mechanism Ground Ring (Optional)



12 Intel® Xeon™ Processor Power Distribution Guidelines

Note: Intel recommends systems utilize modules based on VRM 9.1 DC-DC Converter Design Guidelines for any new Intel® Xeon™ processor with 512 KB L2 cache-based designs. Only existing Intel Xeon processor designs intending to support the Intel Xeon processor with 512 KB L2 cache should continue using VRM 9.0.

12.1 Introduction

As computer performance demands increase, new, higher speed logic with increased density is developed to fulfill these needs. To reduce their overall power dissipation, modern microprocessors are being designed with lower voltage implementations. This in turn requires power supplies to provide lower voltages with higher current capability. Because of this, processor power is now becoming a significant portion of the system design and demands special attention. Now more than ever, power distribution requires careful design practices. The processors that operate in this platform have unique requirements for voltages supplied to them. The processor system bus implementation (based on AGTL+ technology), core, and cache are being powered from the same voltage supply. The demand on the supply current and transient specification has increased drastically by the processor core. As the differences in processor current between the low power state and the high power state increase, the cost of the power distribution system becomes significant enough to merit careful calculation. Centralized distribution of power, for example, is no longer the effective solution to power distribution.

The intent of this chapter is to familiarize the reader with the processor power requirements. In addition, the chapter discusses simulation and power implementation techniques. It is assumed the reader is familiar with power distribution issues of the Pentium® III, Pentium® II Xeon™ and Pentium® III Xeon™ processors.

12.2 Terminology

"Power-Good" or "*PWRGOOD*" (an active high signal) indicates that all of the supplies and clocks within the system are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.

"VCC" in this chapter refers to the appropriate processor core V_{CC}, cache supply voltage and Assisted Gunning Transceiver Logic + (AGTL+) supply voltage. The processor core and cache are on the same silicon and are powered from the same power plane, unlike Pentium II Xeon and Pentium III Xeon processors which required different power planes.

"VRD" refers to a Voltage Regulator Down for the processor. It is an embedded voltage regulator that supplies the required voltage and current for one or more processors.

"VRM 9.0" refers to the Voltage Regulator Module (VRM) intended for use with this platform. It is a DC-DC converter module that supplies the required voltage and current to a single processor.

"VRM 9.1" refers to the next version of the Voltage Regulator Module for the processor, which is based on VRM 9.0. It is a DC-DC converter module that supplies the required voltage and current to a single processor.

12.3 Power Delivery Overview

Power distribution is generally thought of as supplying power to the components that require it. Most digital designers typically assume that an ideal supply will be provided. The printed circuit board (PCB) designers attempt to create this ideal supply with two power planes in the PCB or by using large width traces to distribute power. High-frequency noise created when logic gates switch is typically controlled with high-frequency ceramic capacitors, which are recharged from lower frequency bulk capacitors. Various rule of thumb methods exist for determining the amount of each type of capacitance that is required. For this platform, the system designer needs to design beyond the rule of thumb and architect a power distribution system that meets appropriate processor specifications.

This platform supports dual processor operation. The processor core and all of the caches are operating at the same voltage level, i.e., V_{CC}. On-die termination is used to pull the AGTL+ bus up to V_{CC} to control reflections on the transmission line. Intel chipsets will also provide on-die termination thus eliminating the need to terminate the bus on the system board. The data bus must route over a uniform power plane because of signal quality constraints. Consequently in a multiprocessor system design a single power plane should be used for power delivery to all processors. Hence, the mixing of processors operating at different voltages is not supported and will not be validated by Intel.

12.4 Processor Power Delivery Ingredients

This section describes the issues related to supplying power to the processor. For detailed electrical specifications, refer to the processor datasheets.. Discussion of processor power delivery may be broken down as follows:

- System Design
- Processor Load
- Voltage Regulator
- Power Planes
- Decoupling Capacitors
- Component Placement and Modeling
- Validation Testing

12.5 System Design

12.5.1 Multiple Voltages

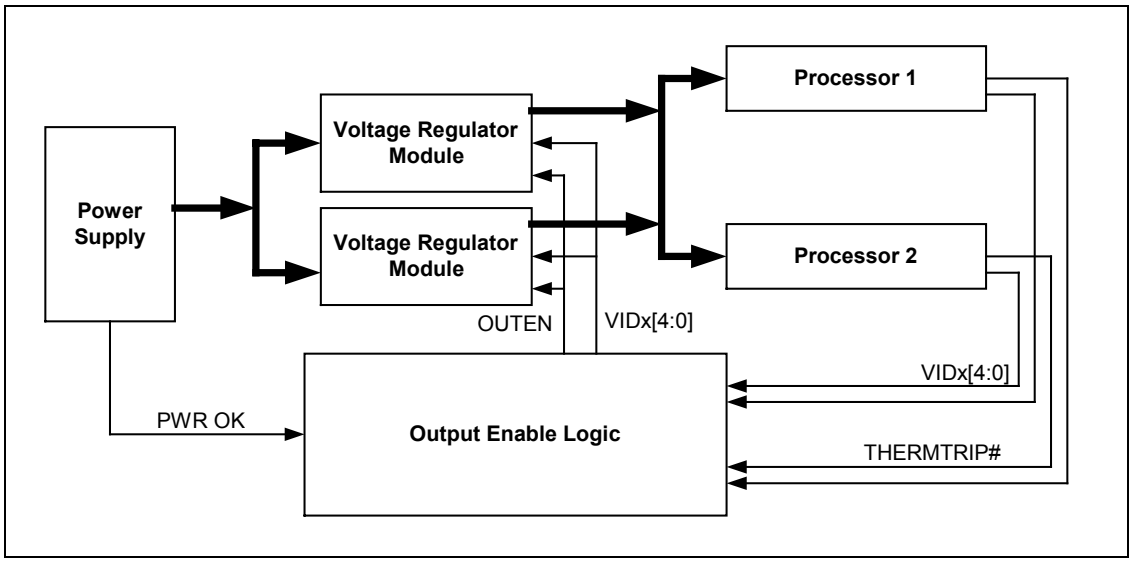
The voltage regulator or voltage regulator modules that provide V_{CC} supply to processor and have the capability of supplying voltages from +1.1 V to +1.85 V. The V_{CCA} supplies power to the processor core and on-die termination used for AGTL+ bus. The voltage regulator is only recommended for dual processor systems. Refer to *VRM 9.1 DC-DC Converter Design Guidelines* or *Dual Intel®* Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines for available voltage details.

Multiple voltages required for the processor are SM_V_{CC} and V_{CC}, which differs for the Intel Xeon processor and Intel Xeon processor with 512 KB L2 cache. $V_{CCIOPLL}$, V_{CCA}, and V_{SSA} are the power supplies to the processor's internal PLL and must be connected to V_{CC} through a discrete RLC filter as described in Section 12.17.3. Refer to the processor datasheet for the pin location of these voltage supplies and specifications for all processor voltage supplies.

12.5.2 Voltage Sequencing

When designing a system with multiple voltages, there is always the issue of ensuring that no damage occurs to the system during voltage sequencing. Voltage sequencing is the timing relationship between two or more voltages, such as VCC and SM_VCC. Sequencing applies to the power voltage levels and the levels of certain other crucial signals when the user turns on or off the power supply, or the system enters a failure condition. VCC from the voltage regulators should be enabled after assertion of the Power Supply Power Good signal and disabled upon de-assertion of the Power Supply Power Good signal. In addition, in the event of any processor asserting its THERMTRIP# signal, VCC must be disabled within 0.5 s. Please contact the chipset vendor for the recommended circuit to disable power to the processor.

Figure 137. Power Distribution Block Diagram for Dual Processor System Motherboard with Voltage Regulator Modules



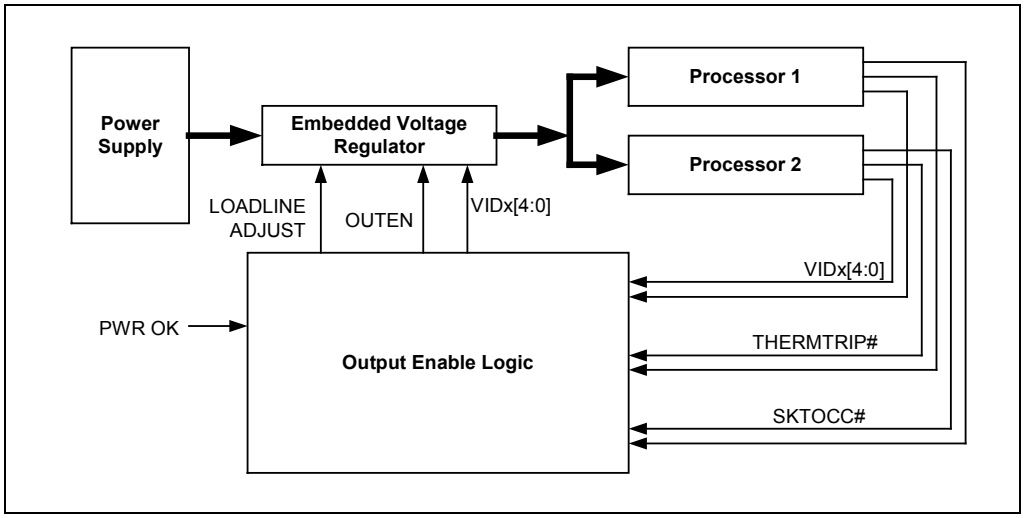
12.5.3 Block Diagrams with Voltage Regulator Modules

Figure 137 depicts the recommended dual processor system baseboard solution involving local voltage regulator modules (VRMs). The block diagrams also recommend the implementation of logic for monitoring the VID [4:0] of all processors. This logic should determine that all of the installed processors are requesting the same VCC. If mixed voltage processors are detected the output enable signal (OUTEN) of all voltage regulators must be disabled. Note that if a processor is not installed the VID [4:0] of that processor are high, and this should not cause disabling of the output of other VRMs.

12.5.4 Block Diagram with Embedded Voltage Regulator

Figure 138 depicts the recommended dual processor system baseboard solution involving a local embedded voltage regulator (often referred to as a V–D - voltage regulator down). The block diagram recommends the implementation of logic for monitoring the VID [4:0] of both processors. This logic should determine that both of the installed processors are requesting the same VCC. If mixed voltage processors are detected the output enable signal (OUTEN) of the voltage regulator must be disabled. Note that if a processor is not installed, the VID [4:0] of that processor are high, and this should cause the load line of the voltage regulator to adjust. The socket occupied pin, SKTOCC#, may also be used to detect the presence of a processor. See Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines.

Figure 138. Power Distribution Block Diagram for Dual Processor System Motherboard with Single Embedded Voltage Regulator



12.6 Processor Load

12.6.1 Processor Current Requirements

This section describes the issues related to supplying power to the processor. For detailed electrical specifications, please refer to the appropriate processor datasheet. The processor allows the use of low power state to reduce power consumption by stopping the clock to specific internal sections of the processor and the BCLK depending on each particular state. This can create load-change transients as high as 450 amps per microsecond on VCC at the socket pins. The shape of the current through the processor socket during a transient usually does not have a constant slope due to the high-frequency filtering by the package decoupling. The historical method of specifying a value for the maximum rate of current change for the processor does not give adequate information in describing the transient current profile. Specifying one value exaggerates the speed of the current transient and can lead to over-design. Intel now provides piecewise-linear (PWL) approximations to specify the transient current allowing the baseboard and voltage regulator designer to optimize their decoupling solutions. Table 46, Table 47, and Figure 139 provide a tabulation and graphical representation of the PWL approximations for each processor type. Note that the processor can also cause load changes of this magnitude while executing regular code. In this document, a load-change transient is a change from one current requirement (averaged over many clocks) to another.

Table 46. Processor Current Step Parameters

Processor		Maximum Step Size Per Processor	Maximum Current Per Processor
Intel® Xeon™ Processor	1.5 GHz	34.5 A	45.7 A
	1.7 GHz	39.0 A	50.3 A
	2.0 GHz	45.7 A	57.2 A
Intel® Xeon™ Processor with 512 KB L2 cache	1.8 GHz	26.5 A	41.9 A
	2.0 GHz	29.3 A	44.7 A
	2.2 GHz	32.1 A	47.6 A

Figure 139. Current Load Step Shape at Socket

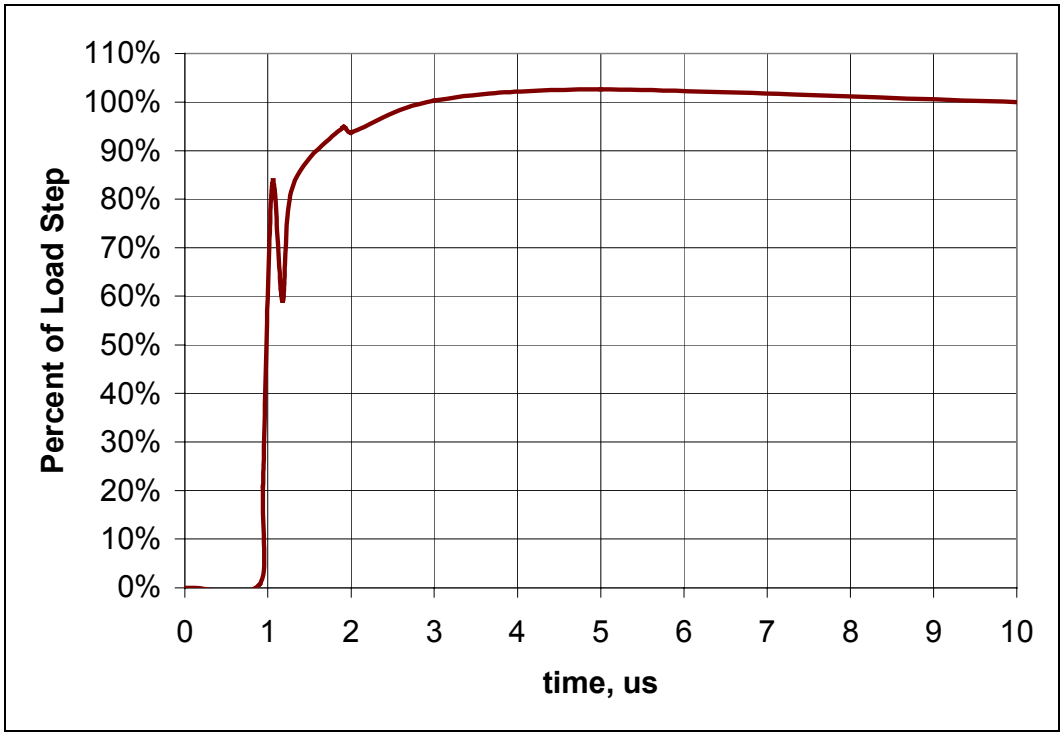


Table 47. Piecewise Linear Tabulation of Load Step at Socket by Percentage

Time (µs)	Percent of Load Step
0.00	0.0 %
0.90	0.7 %
0.94	20.8 %
1.05	83.0 %
1.17	59.1 %
1.30	82.8 %
1.90	94.8 %
2.00	93.8 %
3.00	100.3 %
5.00	102.6 %
10.00	100.0 %

Table 48. Piecewise Linear Tabulation of Load Step at Socket Composite

Time (µs)	Intel® Xeon™ Processor			Intel® Xeon™ Processor with 512 KB L2 Cache		
	1.5 GHz (A)	1.7 GHz (A)	2.0 GHz (A)	1.8 GHz (A)	2.0 GHz (A)	2.2 GHz (A)
0.00	11.2	11.3	11.5	15.4	15.4	15.5
0.90	11.4	11.6	11.8	15.6	15.6	15.7
0.94	18.4	19.4	21.0	20.9	21.5	22.2
1.05	39.8	43.7	49.4	37.4	39.7	42.1
1.17	31.6	34.4	38.5	31.1	32.7	34.5
1.30	39.8	43.6	49.3	37.3	39.7	42.1
1.90	43.9	48.3	54.8	40.5	43.2	45.9
2.00	43.5	47.9	54.3	40.2	42.9	45.6
3.00	45.8	50.4	57.3	42.0	44.8	47.7
5.00	46.6	51.3	58.4	42.6	45.5	48.4
10.00	45.7	50.3	57.2	41.9	44.7	47.6

Figure 140. Piecewise Linear Tabulation of Load Step at Socket Composite

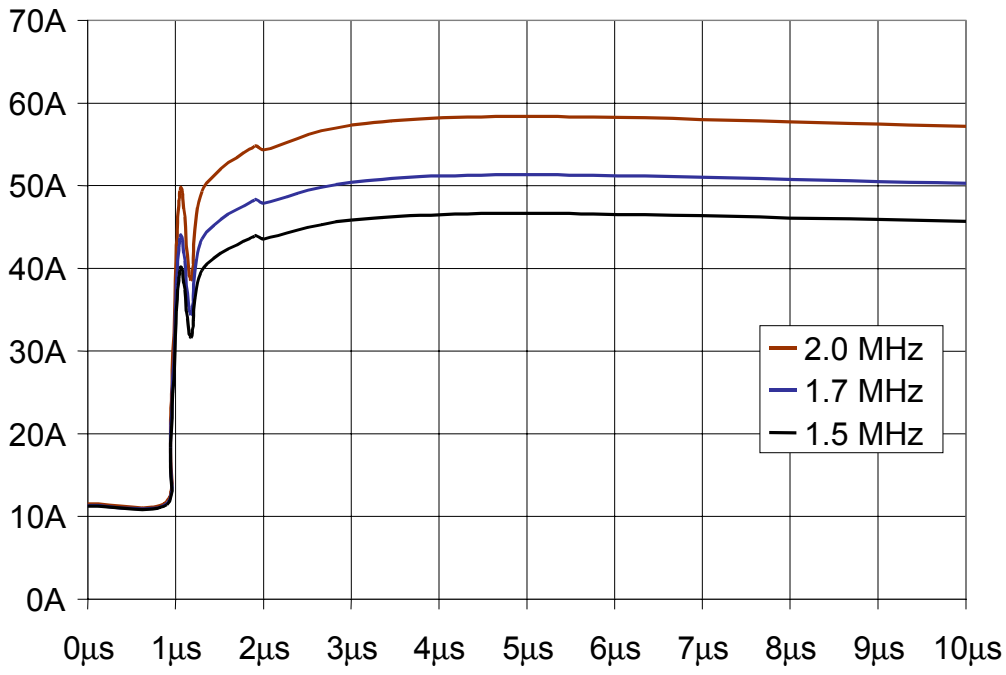
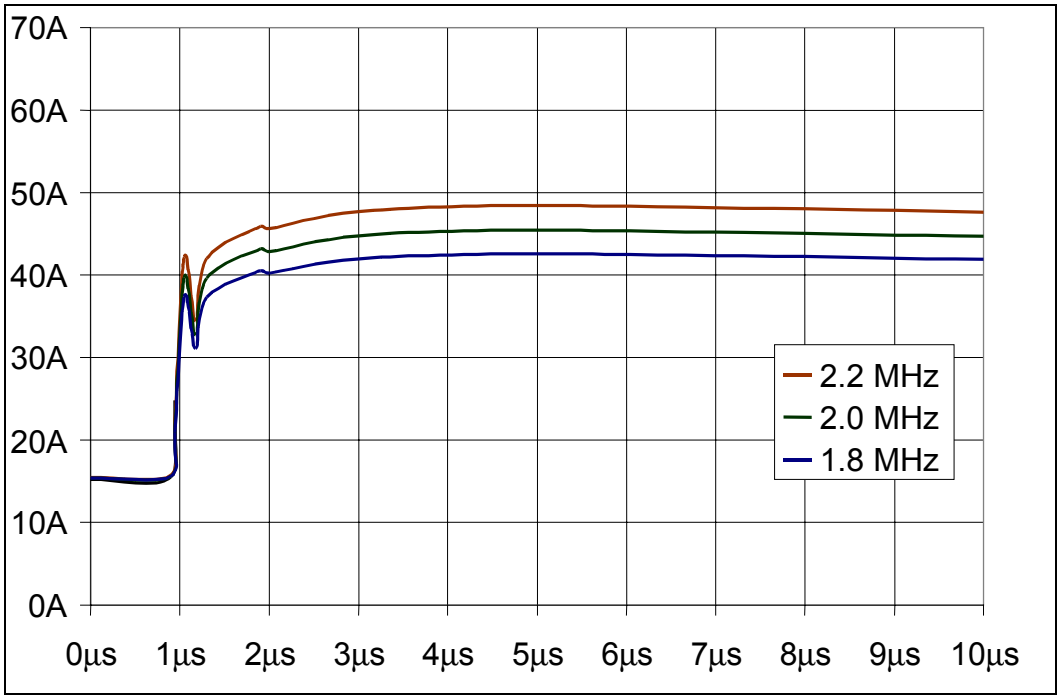


Figure 141. Intel® Xeon Processor with 512 KB L2 Cache Piecewise Linear Socket Current



12.6.2 Processor Voltage Tolerance

Refer to the appropriate processor datasheet for die voltage tolerance specifications. Failure to meet these specifications on the low-end tolerance can result in system error or lock up. Not meeting these specifications on the high-end tolerance can cause damage or reduce the life of the processor.

Refer to either Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines or VRM 9.1 DC-DC Converter Design Guidelines for voltage regulator tolerance specifications (regulation requirements at the voltage regulator remote sense point located at the geometric center of the processors). The voltage tolerance at the voltage regulator remote sense point and the processor socket power pins is depicted in Figure 143 and Table 52 for dual processor Intel Xeon processor platforms; Figure 144 and Table 53 for dual processor Intel Xeon processor with 512 KB L2 cache platforms.

12.6.3 Voltage Regulation Load Lines

The Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines or VRM 9.1 DC-DC Converter Design Guidelines, henceforth referred to in this section as Regulator Guidelines, require that the combination of voltage regulator set-point accuracy and ripple be less than 2% of the VID value. For VID's of 1.7 V and 1.5 V this would be a total budget of 34 mV and 30 mV, respectively. In addition, the voltage regulator should decrease its output voltage as its output current increases. The Regulator Guidelines voltage requirements at the voltage regulator remote sense point and the expected resulting voltage at the processor socket are depicted in Figure 143/Figure 144, and enumerated in Table 52/Table 53, for the Intel Xeon processor and Intel Xeon processor with 512 KB L2 cache respectively. These load lines represent DC and transient requirements. During a current load step, the delivered voltage should stay within the boundaries set by the minimum and maximum voltage requirements of the beginning and ending current values. This is depicted in Figure 142 for the regulator remote sense voltage. Upon a regulator current load step from current A to current B, the voltage at the regulator remote sense point should stay within the bounds set by VMAX for current A and VMIN for current B. Table 50, Table 51, Table 52, and Table 53 provide "current A," "current B," "VMAX for current A" and "VMIN for current B" values. For reference, the socket voltage limits and processor VCCSENSE to VSSSENSE limits are also listed. Socket voltage measurements should be made at the socket pins closest to the voltage regulator for maximum limits and at the socket pins farthest from the voltage regulator for minimum limits.

12.6.4 Voltage Regulation Load Line Equations

The regulator remote sense voltage limits (VSENSE) as a function of regulator current (IVR) are calculated by Equation 12. The socket voltage limits (VSKT) as a function of regulator current (IVR) are calculated by Equation 13 and Equation 14. The values for the equation variables are given in Table 49. The negative values in the RMB column of Table 49 reflect the fact that the socket voltage can be slightly higher than the RVR voltage due to socket being between the regulator output and the SENSE to power plane connection.

Equation 12. Regulator Remote Sense Voltage Limit versus Regulator Current

VSENSE = VTOL X VVID – IVR X RVR

Equation 13. Socket Voltage Limit versus Regulator Current, IVR Less Than IMAX

VSKT = VSENSE – IVR X RMB for IVR less than IMAX

Equation 14. Socket Voltage Limit versus Regulator Current, IVR Greater Than IMAX

VSKT = VSENSE – IMAX X RMB for IVR greater than IMAX

Table 49. Load Line Equation Parameters

		VTOL (%)	VVID (V)	RVR (µΩ)	RMB (µΩ)	IMAX (A)
Intel® Xeon™ Processor	Maximum	1.00	1.7	475	- 100	65
	Minimum	0.98	1.7	475	200	65
Intel® Xeon™ Processor with 512 KB L2 Cache	Maximum	1.00	1.5	475	- 100	65
	Minimum	0.98	1.5	475	200	65

Figure 142. Load Step Transient Voltage

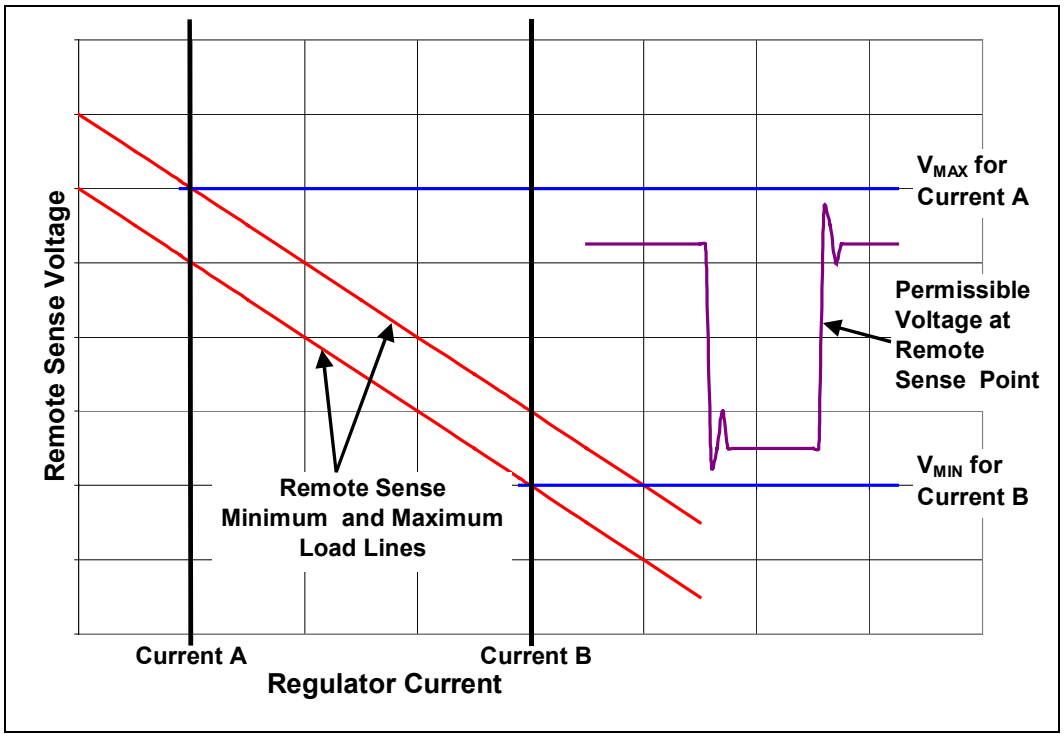


Table 50. Intel® Xeon™ Processor Dual Processor Load Step Transient Requirements

Parameter		1.5 GHz	1.7 GHz	2.0 GHz
Step Size per Processor from Table 46		34.5 A	39 A	45.7 A
Current per Processor from Table 46		45.7 A	50.3 A	57.2 A
Total VR Current Step Size		69 A	78 A	91.4 A
Total VR Average Current Slew Rate		24 A/m	31 A/m	42 A/m
Regulator Increasing Current: Current A to B	Figure 142 Current A	22.4 A	22.6 A	23 A
	Figure 142 Current B	91.4 A	100.6 A	114.4 A
	Figure 142 VMAX	1.689 V	1.689 V	1.689 V
	Figure 142 VMIN	1.623 V	1.618 V	1.612 V
	VMAX Socket	1.692 V	1.692 V	1.691 V
	VMIN Socket	1.610 V	1.605 V	1.599 V
	VMAX proc sense	1.700 V	1.700 V	1.700 V
	VMIN proc sense	1.585 V	1.575 V	1.560 V
Regulator Decreasing Current: Current B to A	Figure 142 Current A	4 A	4 A	4 A
	Figure 142 Current B	69 A	78 A	91.4 A
	Figure 142 VMAX	1.698 V	1.698 V	1.698 V
	Figure 142 VMIN	1.633 V	1.629 V	1.623 V
	VMAX Socket	1.699 V	1.699 V	1.699 V
	VMIN Socket	1.620 V	1.616 V	1.610 V
	VMAX proc sense	1.700 V	1.700 V	1.700 V
	VMIN proc sense	1.585 V	1.575 V	1.560 V

Table 51. Intel® Xeon™ Processor with 512 KB L2 Cache Dual Processor Load Step Transient Requirements

Parameter		1.5 GHz	1.7 GHz	2.0 GHz
Step Size per Processor from Table 46		26.5 A	29.3 A	32.1 A
Current per Processor from Table 46		41.9 A	44.7 A	47.6 A
Total VR Current Step Size		53.0 A	58.6 A	64.2 A
Total VR Average Current Slew Rate		14.2 A/m	17.4 A/m	20.8 A/m
Regulator Increasing Current: Current A to B	Figure 142 Current A	30.8 A	30.8 A	31.0 A
	Figure 142 Current B	83.8 A	89.4 A	95.2 A
	Figure 142 VMAX	1.485 V	1.485 V	1.485 V
	Figure 142 VMIN	1.430 V	1.428 V	1.425 V
	VMAX Socket	1.488 V	1.488 V	1.488 V
	VMIN Socket	1.417 V	1.415 V	1.412 V
	VMAX proc sense	1.500 V	1.500 V	1.500 V
	VMIN proc sense	1.372 V	1.363 V	1.358 V
Regulator Decreasing Current: Current B to A	Figure 142 Current A	4.0 A	4.0 A	4.0 A
	Figure 142 Current B	53.0 A	58.6 A	64.2 A
	Figure 142 VMAX	1.498 V	1.498 V	1.498 V
	Figure 142 VMIN	1.445 V	1.442 V	1.440 V
	VMAX Socket	1.499 V	1.499 V	1.499 V
	VMIN Socket	1.434 V	1.430 V	1.427 V
	VMAX proc sense	1.500 V	1.500 V	1.500 V
	VMIN proc sense	1.372 V	1.363 V	1.358 V

Figure 143. Intel® Xeon™ Processor Socket and Regulator Voltage Limits

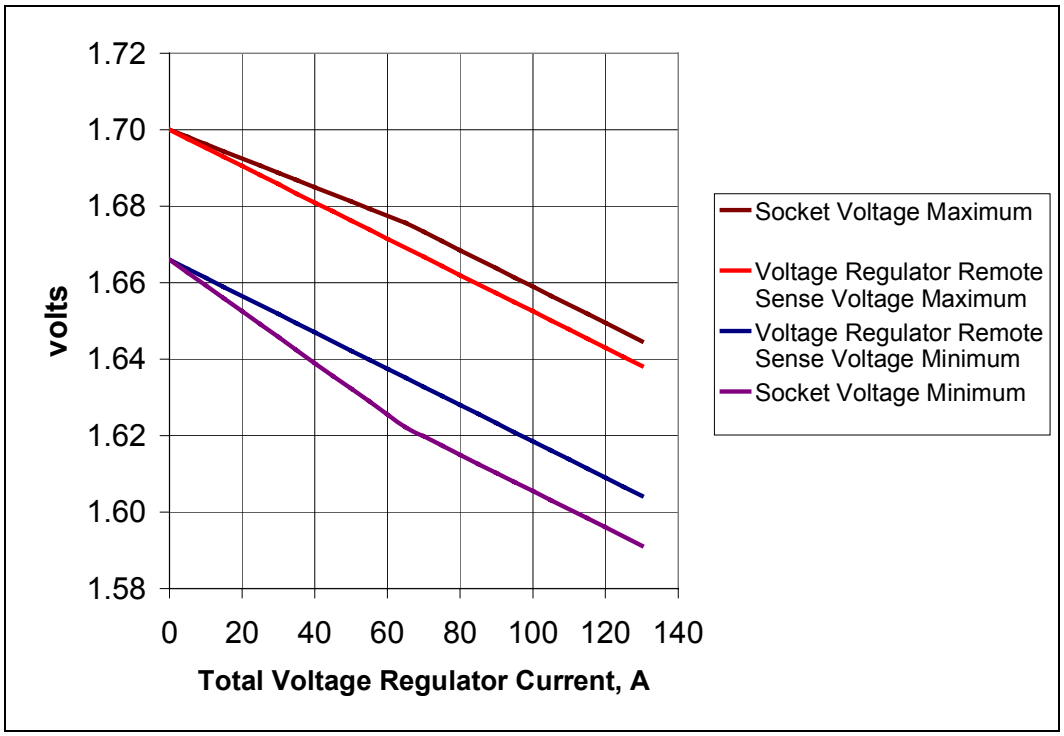


Table 52. Intel® Xeon™ Processor Socket and Regulator Voltage Limits

Total Voltage Regulator Current	Socket Voltage		Voltage Regulator Remote Sense Voltage	
	Maximum	Minimum	Maximum	Minimum
0 A	1.700 V	1.666 V	1.700 V	1.666 V
5 A	1.698 V	1.663 V	1.698 V	1.664 V
10 A	1.696 V	1.659 V	1.695 V	1.661 V
15 A	1.694 V	1.656 V	1.693 V	1.659 V
20 A	1.693 V	1.653 V	1.691 V	1.657 V
25 A	1.691 V	1.649 V	1.688 V	1.654 V
30 A	1.689 V	1.646 V	1.686 V	1.652 V
35 A	1.687 V	1.642 V	1.683 V	1.649 V
40 A	1.685 V	1.639 V	1.681 V	1.647 V
45 A	1.683 V	1.636 V	1.679 V	1.645 V
50 A	1.681 V	1.632 V	1.676 V	1.642 V
55 A	1.679 V	1.629 V	1.674 V	1.640 V
60 A	1.678 V	1.626 V	1.672 V	1.638 V
65 A	1.676 V	1.622 V	1.669 V	1.635 V
70 A	1.673 V	1.620 V	1.667 V	1.633 V
75 A	1.671 V	1.617 V	1.664 V	1.630 V
80 A	1.669 V	1.615 V	1.662 V	1.628 V
85 A	1.666 V	1.613 V	1.660 V	1.626 V
90 A	1.664 V	1.610 V	1.657 V	1.623 V
95 A	1.661 V	1.608 V	1.655 V	1.621 V
100 A	1.659 V	1.606 V	1.653 V	1.619 V
105 A	1.657 V	1.603 V	1.650 V	1.616 V
110 A	1.654 V	1.601 V	1.648 V	1.614 V
115 A	1.652 V	1.598 V	1.645 V	1.611 V
120 A	1.650 V	1.596 V	1.643 V	1.609 V
125 A	1.647 V	1.594 V	1.641 V	1.607 V
130 A	1.645 V	1.591 V	1.638 V	1.604 V

Figure 144. Intel® Xeon™ Processor with 512 KB L2 Cache Socket and Regulator Voltage Limits

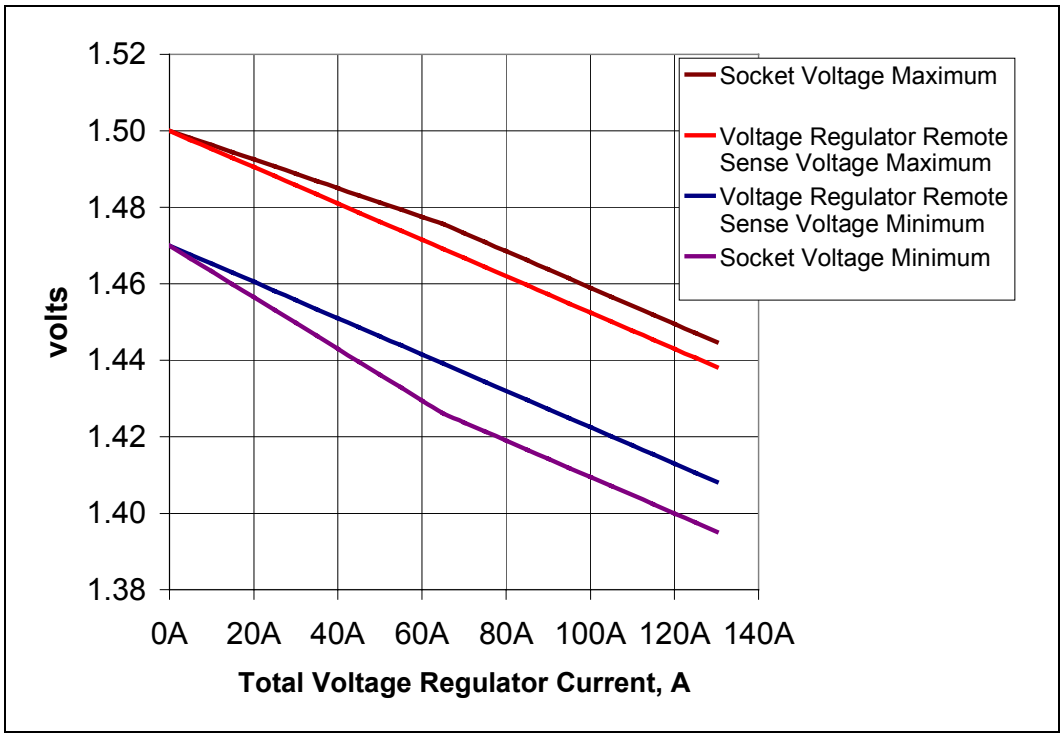


Table 53. Intel® Xeon™ Processor with 512 KB L2 Cache Socket and Regulator Voltage Limits

Total Voltage Regulator Current	Socket Voltage		Voltage Regulator Remote Sense Voltage	
	Maximum	Minimum	Maximum	Minimum
0 A	1.500 V	1.470 V	1.500 V	1.470 V
5 A	1.498 V	1.467 V	1.498 V	1.468 V
10 A	1.496 V	1.463 V	1.495 V	1.465 V
15 A	1.494 V	1.460 V	1.493 V	1.463 V
20 A	1.493 V	1.457 V	1.491 V	1.461 V
25 A	1.491 V	1.453 V	1.488 V	1.458 V
30 A	1.489 V	1.450 V	1.486 V	1.456 V
35 A	1.487 V	1.446 V	1.483 V	1.453 V
40 A	1.485 V	1.443 V	1.481 V	1.451 V
45 A	1.483 V	1.440 V	1.479 V	1.449 V
50 A	1.481 V	1.436 V	1.476 V	1.446 V
55 A	1.479 V	1.433 V	1.474 V	1.444 V
60 A	1.478 V	1.430 V	1.472 V	1.442 V
65 A	1.476 V	1.426 V	1.469 V	1.439 V
70 A	1.473 V	1.424 V	1.467 V	1.437 V
75 A	1.471 V	1.421 V	1.464 V	1.434 V
80 A	1.469 V	1.419 V	1.462 V	1.432 V
85 A	1.466 V	1.417 V	1.460 V	1.430 V
90 A	1.464 V	1.414 V	1.457 V	1.427 V
95 A	1.461 V	1.412 V	1.455 V	1.425 V
100 A	1.459 V	1.410 V	1.453 V	1.423 V
105 A	1.457 V	1.407 V	1.450 V	1.420 V
110 A	1.454 V	1.405 V	1.448 V	1.418 V
115 A	1.452 V	1.402 V	1.445 V	1.415 V
120 A	1.450 V	1.400 V	1.443 V	1.413 V
125 A	1.447 V	1.398 V	1.441 V	1.411 V
130 A	1.445 V	1.395 V	1.438 V	1.408 V

12.7 Voltage Regulator

Intel recommends that the processor power if provided by an embedded voltage regulator meets the specifications described in Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines or voltage regulator modules (one per processor) as described by either VRM *9.0 DC-DC Converter Design Guidelines* or *VRM 9.1 DC-DC Converter Design Guidelines*. The voltage regulator definition includes Remote-Sense, Current Share and Output Enable features. Voltage regulator designers must provide these features as well as meeting voltage and current requirements set forth in the regulator design guidelines. The voltage regulator output slew rate is generally less than 50 A/µs. The slew rate at the processor socket pins can be as high as 450 A/µs. The system designer needs to provide adequate bulk and high-frequency decoupling on the baseboard to meet the processor required slew rate. Generally, the main power source for the voltage regulator is 12 V +5%, -8%. This voltage is supplied by a conventional computer power supply through a cable to the baseboard.

12.8 Voltage Regulator Design

It is outside the scope of this document to provide all the nuances involved in creating a high performance voltage regulator. Intel provides a list of enabled VRM suppliers and provides customer reference designs with embedded voltage regulators. Also, manufacturers of voltage regulator IC controllers provide application notes, demo modules, design reviews and other forms of customer support including on site design assistance.

12.9 Voltage Regulator System Matching

12.9.1 Voltage Regulator Output

Some voltage regulator modules may be purchased with output capacitance included although many voltage regulator modules available today rely entirely on the baseboard for their output filtering capacitance. Regardless, the transient response or bandwidth of the voltage regulator must complement the combined output decoupling and storage capacitors so that the DC to 10 MHz impedance seen by the processor socket is less than 1 mΩ for a single processor system, 0.5 mΩ for a dual processor system, and 0.25 mΩ for a four processor system.

12.10 Voltage Regulator Input

Some voltage regulator modules may be purchased with input power filtering included although many voltage regulator modules available today rely entirely on the baseboard for their input power filtering. Input filtering requirements are dependant upon the power source and transient tolerance of common loads. However, for a typical 12 V power source, the voltage regulator input filter must limit its power sou’ce's current rate of change to less than 100 mA/µs. Other peripheral 12 V components should be powered separately from the voltage regulators.

12.11 Voltage Regulator Cooling

High performance voltage regulators generally operate at less than 85% efficiency. Careful attention must be given to providing adequate cooling air or thermal conduction paths. If using voltage regulator modules, the temperature of the module board must not exceed 90 °C at the connector interface. Specifically, to maintain the connector within its operating temperature range, the VRM board must not exceed 90 °C at any point within 2.54 mm of the top of the connector.

12.12 Voltage Regulator Remote Sense Connection

The system board is to include a positive and a negative SENSE input for the embedded voltage regulator or for each voltage regulator module. The round trip trace resistance should not be greater than one ohm. These voltage sense lines draw little current and there should be only a minute voltage drop from the remote sense connection and the voltage regulators.

In a multiprocessor system the SENSE lines from the embedded voltage or voltage regulator modules should be routed to a point in the middle of and equidistant from all processors. At this remote sense point all positive SENSE lines should be tied together and connected to VCC_CPU and all negative SENSE lines should be tied together and connected to VSS_CPU.

All SENSE lines should be routed directly between the remote sense point and the voltage regulator and should not exceed 5 inches in trace length. If the SENSE lines are routed parallel to signal lines, the SENSE lines should be shielded.

12.13 Voltage Regulator Module ISHARE Connection

If voltage regulator modules are used it is necessary that the ISHARE lines of the modules be connected. The round trip resistance of this connection should be less than 1 W. The ISHARE connection traces should be shielded from or separated from noisy signal traces.

12.14 Voltage Regulator Module OUTEN Connection

The voltage regulat’rs' OUTEN input is used to disable the regulat’rs' output voltage. The system designer should disable the output of the voltage regulator in a multiprocessor system when processors with different voltage settings are installed. The block diagrams in Figure 137 and Figure 138 show this implementation based on VID [4:0] signals. Note that the VID lines are pulled up internal to the voltage regulators. No pull-ups are allowed on the baseboard. If the designer adds pull-ups on the baseboards, voltage-sequencing problems can occur with unpredictable results.

12.15 Power Planes

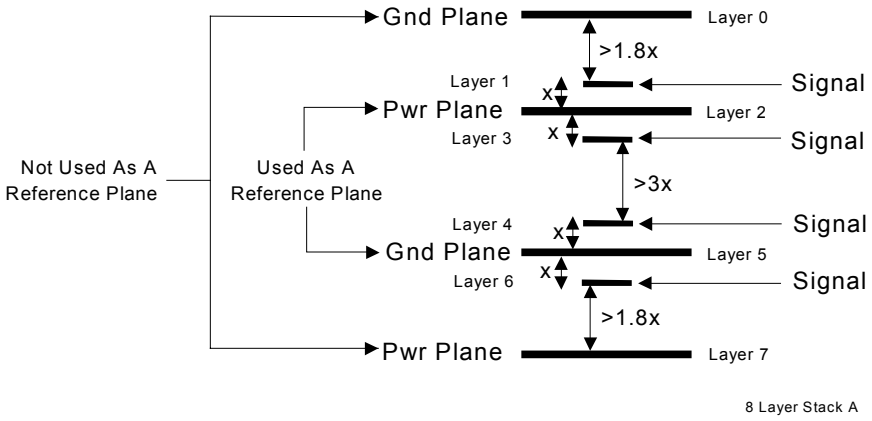
VCC static and transient tolerances of the processor, and the corresponding voltage regulator tolerances assume power distribution paths with round trip resistances no greater than 300 mΩ and inductances any greater than 100 pH. Power must be distributed as a plane. This plane can be constructed as an island on a layer used for other signals, on a supply plane with other power islands, or as a dedicated layer of the PCB. Processor power should never be distributed by traces alone.

Due to the fact that processor voltage is unique to most system designs, a voltage island will probably be the most cost-effective means of distributing power to the processors. This island from the source of power to the load should not have any breaks, so as to minimize inductance in the plane. It should also completely surround all of the pins of the source and all of the pins of the load.

12.15.1 Layer Stack-Up

Intel recommends an absolute minimum of two ounce copper power plane for both VCC and VSS. The goal for dual processor systems should be at 2.5 ounces or more and 3.5 ounces or more for four processor systems. This can be implemented using multiple layers as shown in the example given in Figure 145b.

Figure 145. Suggested Eight Layer Stack-Up for Dual Processor Systems



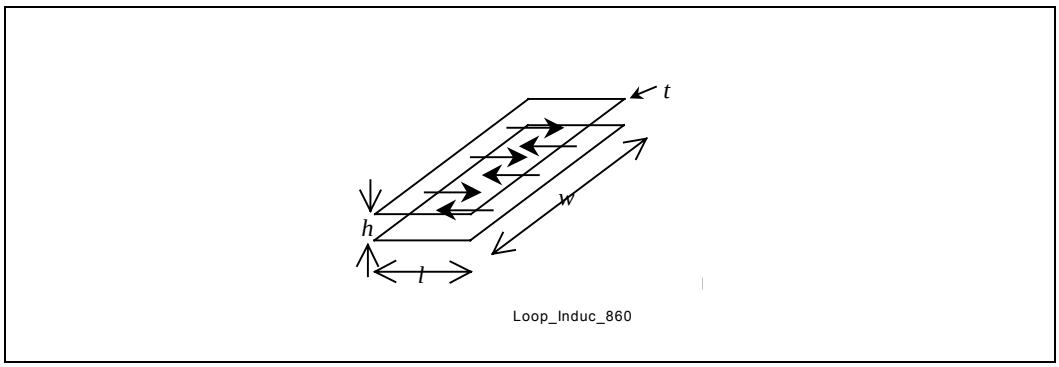
12.15.2 Sheet Inductance/Resistance and Emission Effects of Power Plane

The imperfections of the power plane themselves may introduce unwanted resistance and inductance into the power distribution system. Assuming layer thickness is smaller than skin depth, the metal layer resistance can be calculated as:

$$R = \rho \cdot \frac{l}{w \cdot t},$$

where ρ is the copper resistivity (ρ = 0.667 mΩ·mil), l, w, and t are the length, width and thickness of the metal layer, respectively.

Figure 146. Loop Inductance



The loop inductance can be calculated as:

$$L = 31.9 \frac{\text{pH}}{\text{mil}} \cdot \frac{l \cdot h}{w \cdot (N-1)}$$

where N is the number of VCC_CPU/V_{SS} planes. To minimize parasitic layer inductance, it is important to reduce the distance from decoupling capacitors to the processor socket (reducing l) and to use islands for power distribution (increasing w). To reduce h, it is recommended to select the VCC_CPU/V_{SS} planes in the layer stack up that are interleaved and have small spacing in between. As a practical matter it is impossible to get the requisite L_{mb1} and L_{mb2} without locally dedicating at least 4 planes to carry power from the baseboard capacitors to the power pins of the processor.

There are impedance consequences for signals that cross over or under the edges of the power island that exists on another layer. While neither of these may be necessary for most designs, there are two reasonable options to consider which can protect a system from these consequences.

Processor power islands can be isolated from signals by one of the solid power plane layers such as the ground layer. This forces a particular stack-up model.

Another option that helps, but does not completely eliminate radiation effects, is to decouple the edges of the processor power islands to ground on regular intervals of about 1 inch using good high frequency decoupling capacitors (1206 packages). This requires more components but does not require any particular board stack-up.

In either event, for controlling emissions, all planes and islands should be well decoupled. The exact board layout, and the chassis design will determine the amount of decoupling required for controlling emissions. One should plan ahead by allowing additional pads for capacitors to be added in case they are found to be necessary during EMI testing.

Signals routed over power islands or islands in the ground plane create a discontinuity in the return path of that signal. This discontinuity can have detrimental effects on the timing and signal quality of that signal and other signals referencing the same planes. Avoid routing signals over splits in power planes or ground planes at all times.

Example:

Given power bussing area from the regulator to the socket approximated as a rectangle, with the following dimensions for the power and ground plane: l = 0.279 inch; w = 2.09 inches; t = 1.24 mils (1 oz. copper):

$$R = 0.677\ \text{m}\Omega \cdot \text{mil} \cdot \frac{0.279''}{2.09 \cdot 1.24\ \text{mil}} = 0.073\ \text{m}\Omega\ .$$

The total resistance of the round trip is:

$$R = 2 \cdot 0.073\ \text{m}\Omega = 0.15\ \text{m}\Omega\ .$$

With the VCC_CPU/VSS separated by 4.5 mils, the loop inductance is:

$$L = 31.9\frac{\text{pH}}{\text{mil}} \cdot \frac{0.279\ \text{mil} \cdot 4.5\ \text{mil}}{2.09\ \text{mil} \cdot (2 - 1)} = 19.2\ \text{pH}\ .$$

12.16 Decoupling Capacitors

12.16.1 Decoupling Technology and Transient Response

The inductance of the system due to cables and power planes slows the power sup'ly's ability to respond quickly to a current transient. Decoupling a power plane can be broken into several independent parts. The closer to the load the capacitor is placed, the more inductance that is bypassed. By bypassing the inductance of leads, power planes, etc., less capacitance is required. However, closer to the load there is less room for capacitance. Therefore tradeoffs must be made.

The processor can cause very large switching transients. These sharp surges of current occur at the transition between low power mode and high power mode. It is the responsibility of the system designer to provide adequate high-frequency decoupling to manage the highest frequency components of the current transients. To lower total board inductance and resistance, the Intel Xeon processor is designed with approximately 141 VCC and 141 VSS (ground) pins. The Intel Xeon processor with 512 KB L2 cache is designed with 188 VCC and 189 VSS (ground) pins. The designer needs to support a current slew rate of 450 A/µs at the socket pins. Larger bulk storage such as OSCON capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition.

All of this power bypassing is required due to the relatively slow speed at which a DC-to-DC converter can react. A typical voltage converter has a reaction time on the order of 1 µs to 10 µs while the proces'or's current steps are on the order of 100 ns to 200 ns. Bulk capacitance supplies energy from the time the high-frequency decoupling capacitors are drained until the power supply can react to the demand. More correctly, the bulk capacitors in the system slow the transient requirement seen by the power source to a rate that it is able to supply, while the high-frequency capacitors slow the transient requirement seen by the bulk capacitors to a rate that they can supply.

A load-change transient occurs when coming out of or entering a low power mode. This load-change transient can be on the order of 55 amps. These are not only quick changes in current demand, but also long lasting average current requirements. This occurs when the processor enters or leaves a low power state. Please refer to the processor datasheet for more information on the low power states. Note that even during normal operation, the processor current requirements can change by as much as 70% (± 10%) of the max current very quickly.

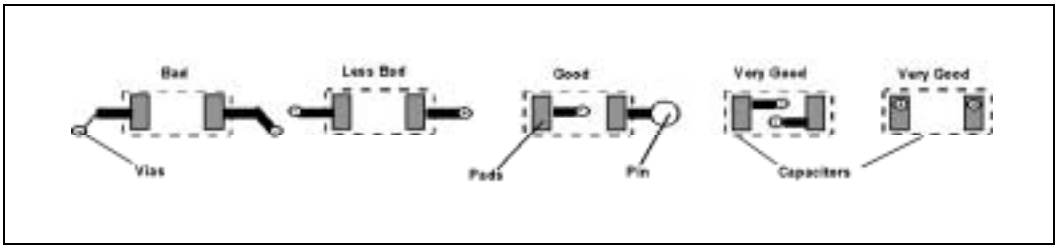
Maintaining voltage tolerance, during these changes in current, requires high-density bulk capacitors with low Effective Series Resistance (ESR) and low Effective Series Inductance (ESL). Use thorough analysis when choosing these components.

12.16.2 Location of High-Frequency Decoupling

A system designer should properly design for the high-frequency decoupling. High-frequency decoupling should be placed as close to the power pins of the processor as physically possible. Use both sides of the board if necessary for placing components in order to achieve the optimum proximity to the power pins. This is vital as the inductance of the bo'rd's metal plane layers could cancel the usefulness of these low inductance components.

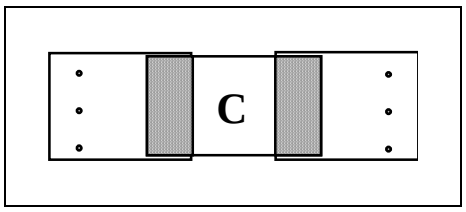
Another method to lower the inductance that should be considered is to shorten the path from the capacitor pads to the pins that it is decoupling. If possible, place the vias connecting to the planes within the pad of the capacitor. If this is not possible, keep the traces as short and wide as is feasible. Possibly one or both ends of the capacitor can be connected directly to the pin of the processor without the use of via. Even if simulation results look good, these practical suggestions can be used to create an even better decoupling situation where they can be applied in layout. Figure 147 illustrates these concepts.

Figure 147. 1206 Capacitor Pad and Via Layouts



If polymer capacitors or large ceramics are being used, avoid the loss of the low ESL characteristic by connecting via patterns as wide as the capacitor with multiple via holes per connection, as shown in Figure 148b.

Figure 148. Connections to Via Patterns



12.16.3 Location of Bulk Decoupling

The location of bulk capacitance is not as critical as the high-frequency decoupling since more inductance is already expected for these components. However, to achieve better performance, good placement of these components will affect the transient response of the system for the better, as shown in simulation. In addition to the bulk capacitors on the voltage converter module, which are electrically behind the inductance of the converter pins, several bulk capacitors need to be placed close to the processor socket.

12.16.4 Decoupling Recommendation

Intel recommends that the baseboard design incorporates at least nine 560 µF OSCON bulk capacitors and twenty 22 µF ceramic capacitors per processor. The bulk capacitors should be placed, half on one side of the processor and half on the other as close to the processor package as the keep-out zone allows. One quarter of the ceramic capacitors should be placed on one side of the processor, one quarter on the other side, and half in the processor cavity using both sides of the board. See Section 12.16.5 for placement options. Check with the voltage regulator designer for optimal choice of bulk capacitors. Some very high switching regulators are better served by replacing the OSCON bulk capacitors with additional high-frequency ceramics. Table 54 provides parameters for bulk and high-frequency capacitors.

12.16.5 Component Placement and Modeling

Intel recommends using simulation to design and verify this platform. The models in the following sections can be used to piece together a complete base board spice circuit. The PWL data from Table 46 and Table 47 or Table 48 can be used to create the current waveform of the processor load.

The maximum distance between each processor and its voltage regulator module or the output inductors of an embedded voltage regulator should not be greater than 1.5 inches. To be more specific, the distance between the facing edges of the VRM connector (or the output terminal of the output inductor of an embedded voltage regulator) and the socket should be no more than 0.5 inch. The bulk capacitors can be placed close to and the high-frequency capacitors should be placed next to the processors. Distribute the bulk and high-frequency capacitors equally on both sides of the socket where the power/ground pins are located (the east and west side).

The 603-pin socket use on this platform has 603-pins with 50-mil pitch. The routing of the signals, power and ground pins will require creation of lots of vias. These vias cause a “Swiss cheese” effect in the power and ground planes beneath the processor resulting in increased inductance of these planes. It is recommended to place as many high-frequency capacitors as possible inside the cut out of the processor socket. The remaining high-frequency capacitors should be placed next to the processor, specifically the power/ground pins.

Processors should be placed with respect to the voltage regulator or voltage regulator modules and bulk decoupling capacitors such that current to one processor does not flow in the same path as that of any other processor.

12.16.6 Component Models

Acquire component models from their respective manufacturers. Intel cannot guarantee the specifications of another manufactu'er's components. This section contains some of the models developed by Intel for internal simulations.

Table 54. Various Component Models Used at Intel (Not Vendor Specifications)

Component of Simulation	ESR (Ω)	ESL (nH)
0.1 µF Ceramic 0603 package	0.006	0.63
1 µF Ceramic 0805 package	0.080	0.702
10.0 µF Ceramic 1206 package	0.010	0.880
22.0 µF Ceramic 1210 package	0.010	0.880
560 µF OSCONS	0.012	2.7

12.16.7 Processor Socket-Package Lump Model

Figure 149 shows the lump electrical model for the high-frequency baseboard capacitors, the processor socket, and the processor package. Figure 150 shows a physical pictorial of the model. This model serves as a sub-circuit for the following baseboard models. Table 55 lists the mo'el's component values. L2 and L6 refer to the inductance and resistance of the power plane next to the processor socket area, i.e., "before Swiss cheese" area. L3 and L5 refer to the inductance and resistance of the power plane within the processor socket area, i.e., "after Swiss cheese" area. The inductance and resistance of the power plane between voltage regulator and bulk capacitors and the processor is shown as L1 and L7. A current step from 0 A to 55 A should be applied with a rise time of 308 ns or use the PWL values.

Figure 149. Processor Lump Model Schematic

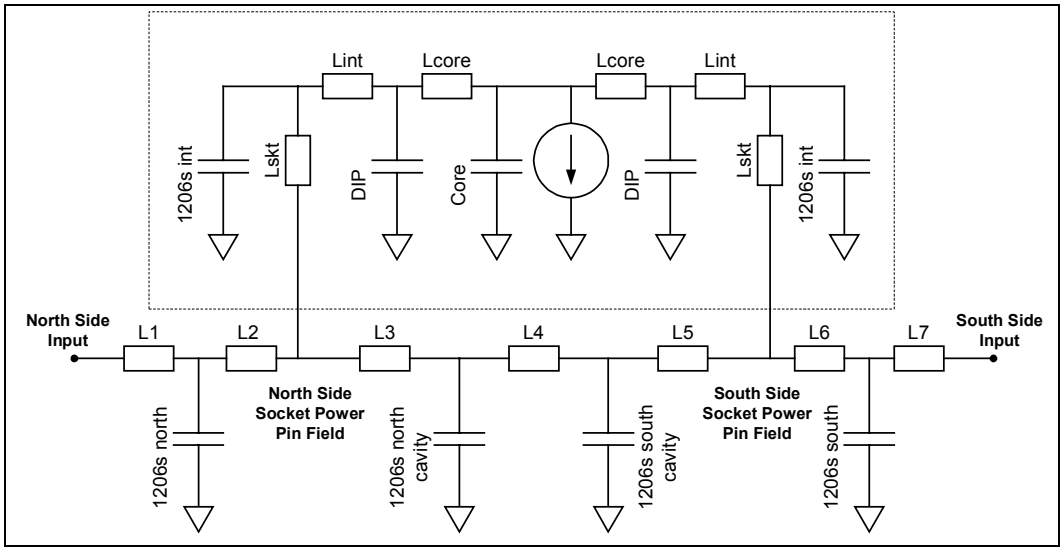


Table 55. Processor Lump Model Component Values

Component	Description	Value		
		Resistance	Inductance	Capacitance
1206's North/South	Five 22 mF MLCC	10 mΩ / 5	1.1 nH / 5	5 * 22 µF
1206's North/South Cavity	Five 22 mF MLCC	10 mΩ / 5	1.1 nH / 5	5 * 22 µF
1206's Interposer	Interposer MLCC	833 µΩ	45 pH	120 µF
DIP Capacitors	Package Capacitors	270 µΩ	2.35 pH	36 µF
Core Capacitors	Die Capacitance	146 µΩ	0	541 nF
L1	North Side Input	17 0µΩ	23 nH	-
L2	North Side Pin Field Input	150 µΩ	23 nH	-
L3	North Side Cavity Input	120 µΩ	18 nH	-
L4	Cavity	130 µΩ	20 nH	-
L5	South Side Cavity Input	120 µΩ	18 nH	-
L6	South Side Pin Field Input	150 µΩ	23 nH	
L7	South Side Input	170 µΩ	23 nH	
Lskt	Socket Impedance	326 µΩ	24 pH	
Lint	Interposer Impedance	125 µΩ	12 pH	
Lcore	Package Impedance	25 µΩ	1 pH	

Figure 150. Processor Lump Model Drawing

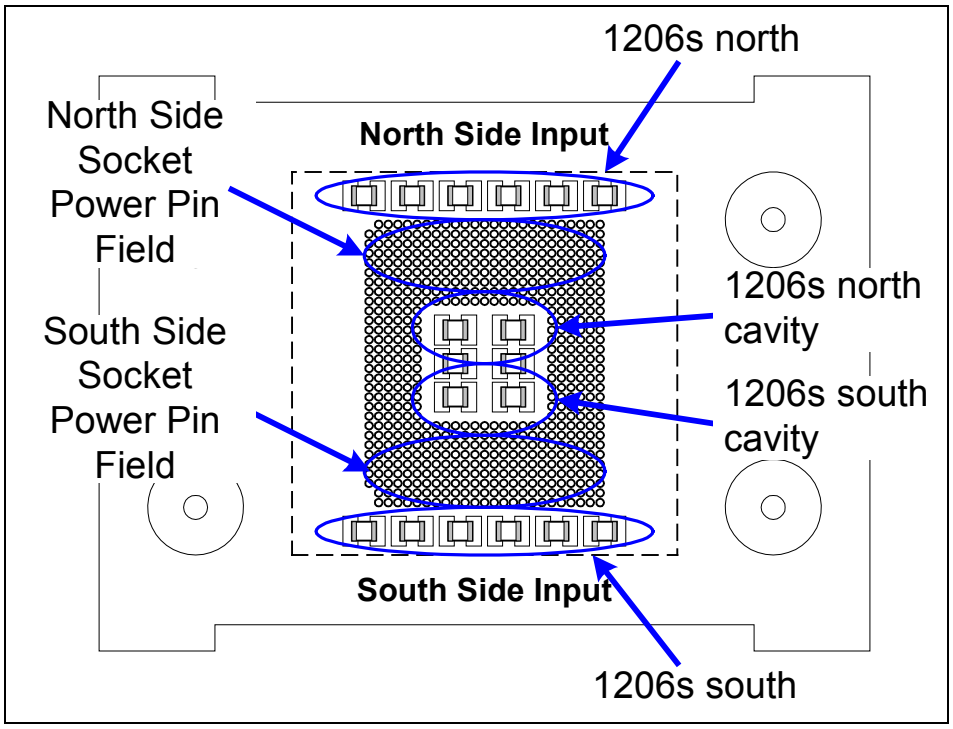


Figure 151. “L” Pattern with Embedded Voltage Regulator

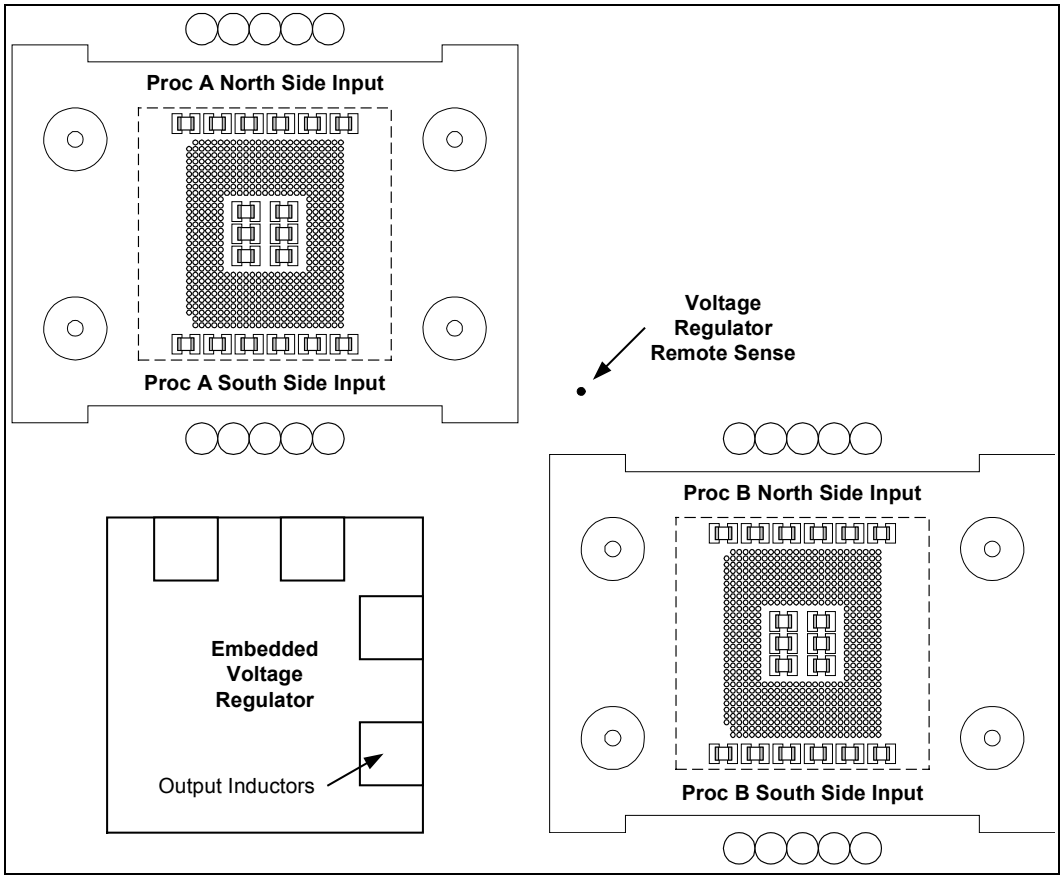


Figure 152. “L” Pattern with Embedded Voltage Regulator Schematic

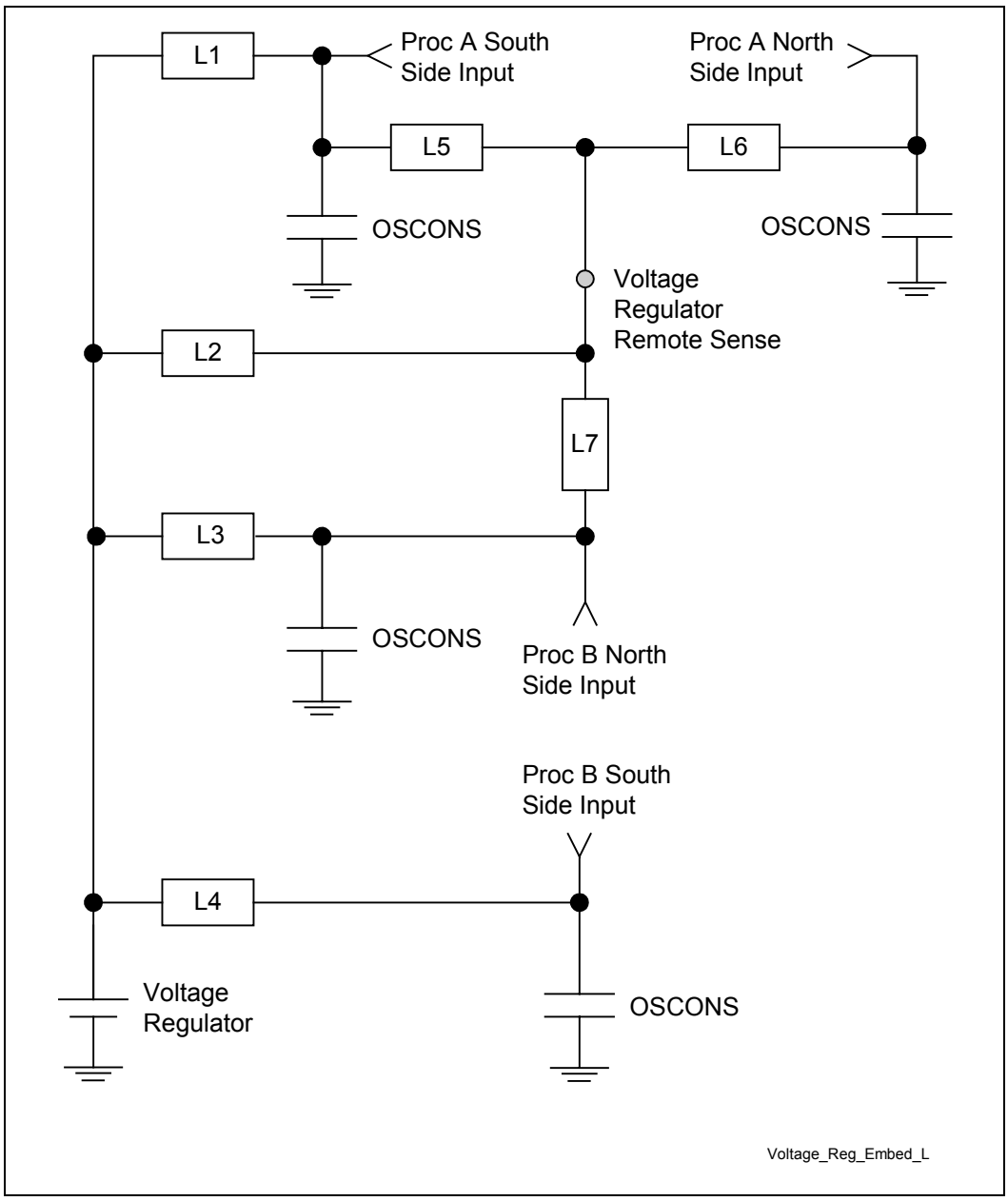


Table 56. "L" Pattern with Embedded Voltage Regulator Schematic Values

Component	Description	Values		
		Resistance	Inductance	Capacitance
OSCONs	Bulk Capacitors	12 mΩ / 5	3.1 nH / 5	5 ¥ 560 µF
L1	VR – Proc A south	150 µΩ	40 pH	-
L2	VR –Sense	600 µΩ	160 pH	-
L3	VR – Proc B north	600 µΩ	160 pH	-
L4	VR – Proc B south	600 µΩ	160 pH	-
L5	Proc A south – Sense	600 µΩ	160 pH	-
L6	Proc A north – Sense	1.5 mΩ	400 pH	-
L7	Proc B north – Sense	300 µΩ	80 pH	

Figure 153. "Row" Pattern with Voltage Regulator Module

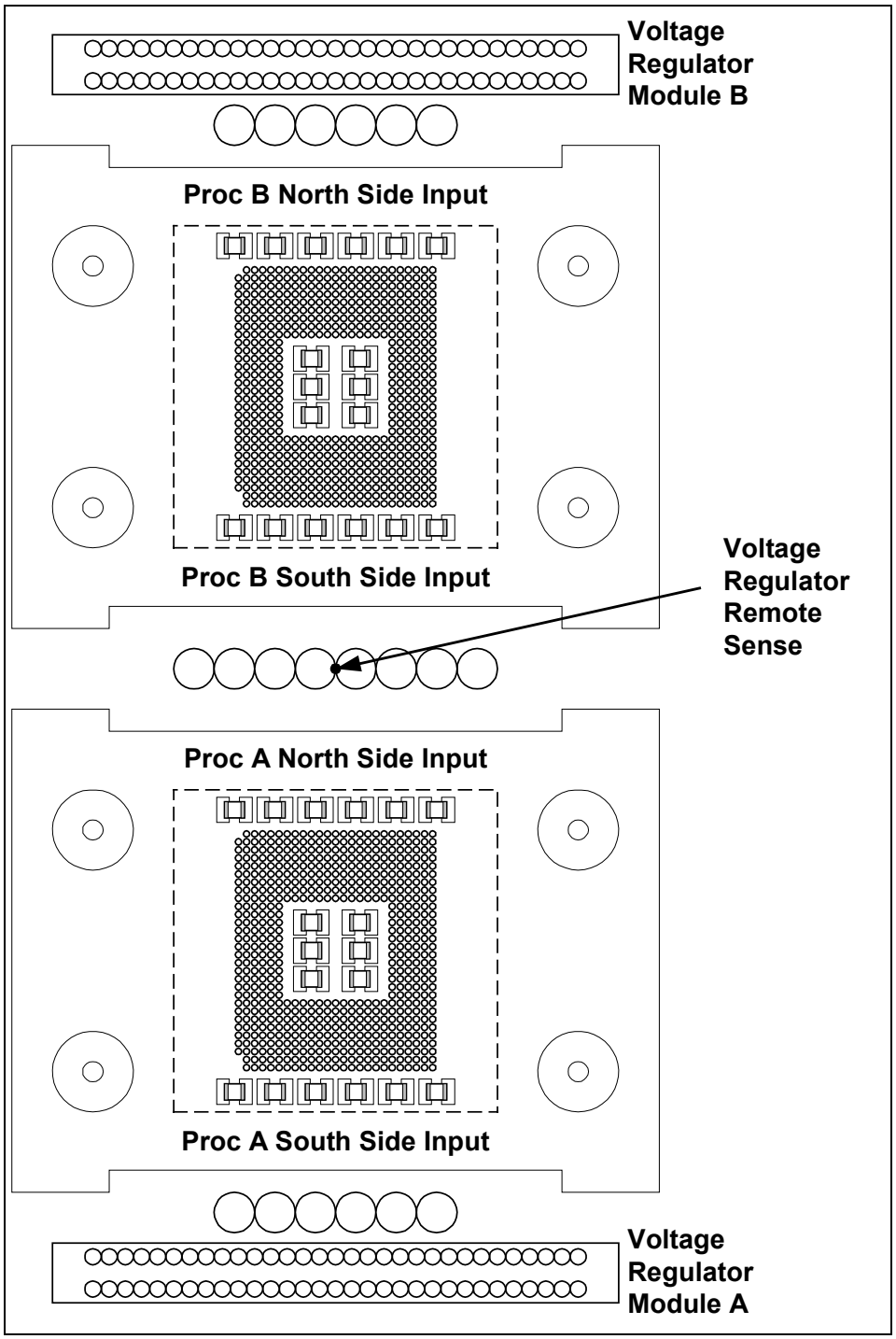


Figure 154. "Row" Pattern with Voltage Regulator Module Schematic

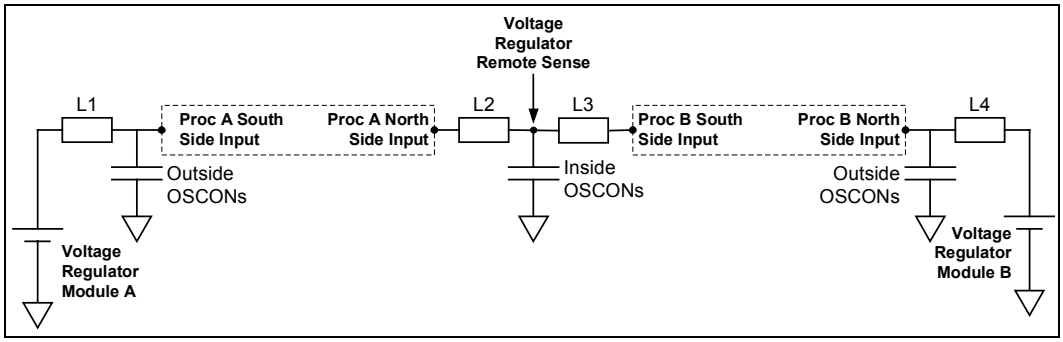


Table 57. "Row" Pattern with Voltage Regulator Module Schematic Values

Component	Description	Vales		
		Resistance	Inductance	Capacitance
Outside OSCONs	Bulk Capacitors	12 mΩ / 6	3.1 nH / 6	6 X 560 µF
Inside OSCONs	Bulk Capacitors	12 mΩ / 8	3.1 nH / 8	8 X 560 µF
L1	VRM A – Proc A south	75 µΩ	20 pH	-
L2	Proc A nor–h - sense	75 µΩ	20 pH	-
L3	Proc B sou–h - sense	75 µΩ	20 pH	-
L4	VRM B – Proc B north	75 µΩ	20 pH	-

Figure 155. “Row” Pattern with Embedded Voltage Regulator

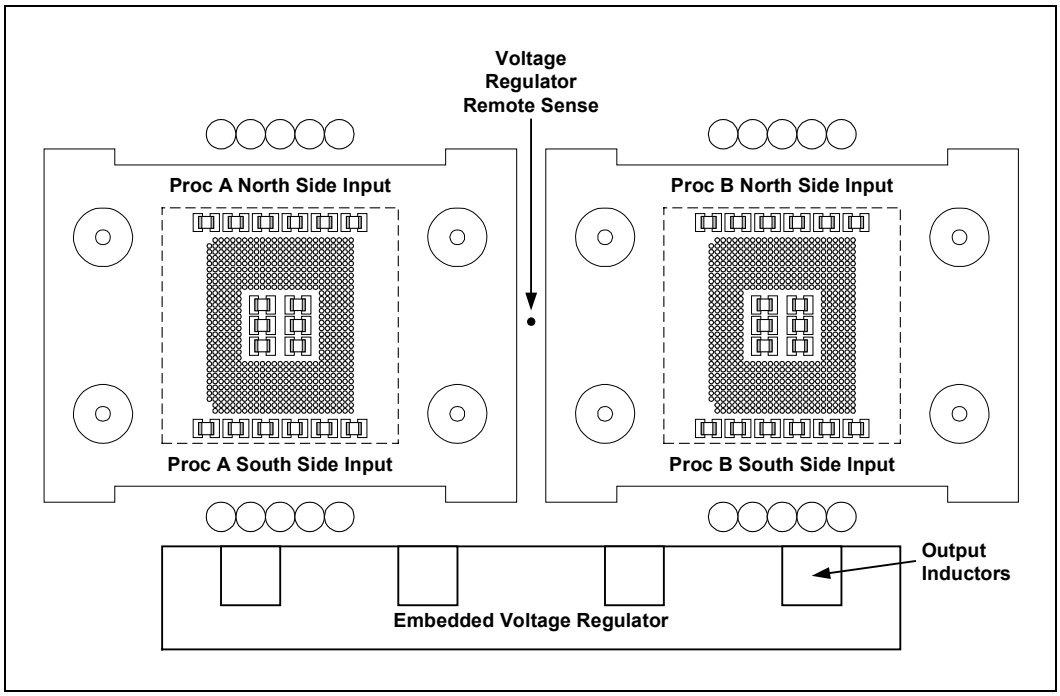


Figure 156. "Row" Pattern with Embedded Voltage Regulator Schematic

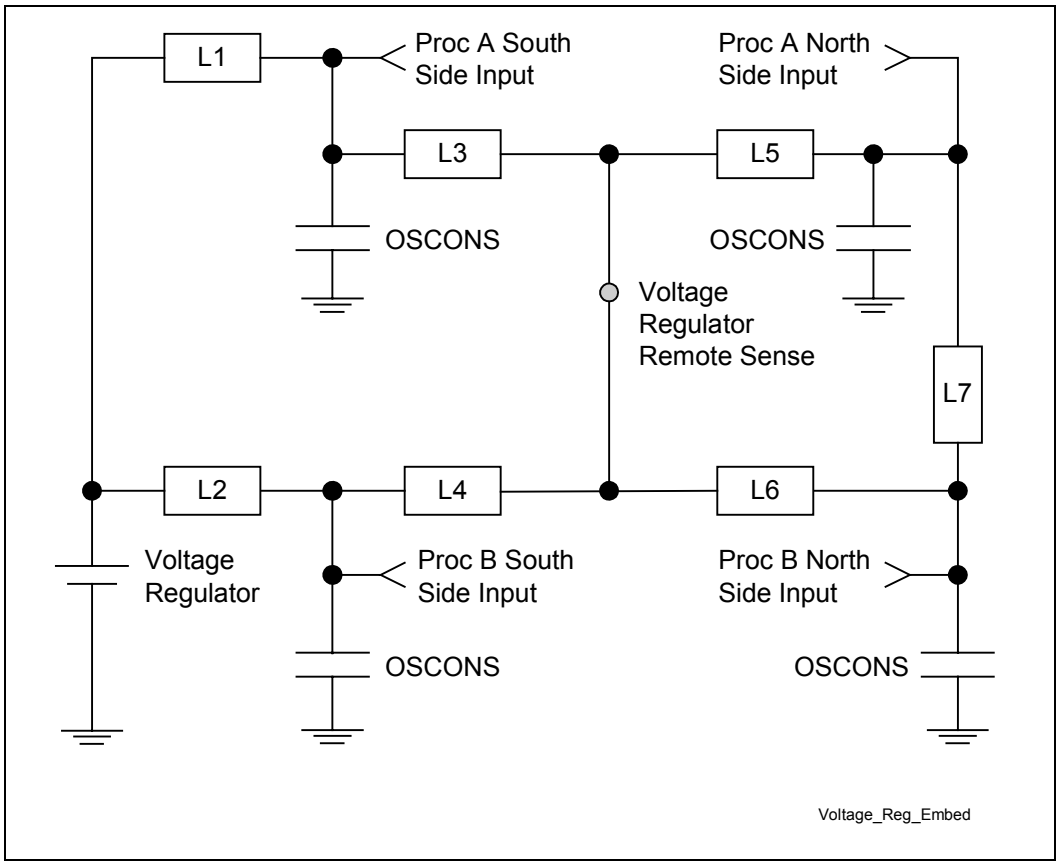


Table 58. "Row" Pattern with Embedded Voltage Regulator Schematic Values

Component	Description	Vales		
		Resistance	Inductance	Capacitance
OSCONs	Bulk Capacitors	12 mΩ / 5	3.1 nH / 5	5 X 560 µF
L1	VRM A – Proc A south	75 µΩ	20 pH	
L2	VRM A – Proc B south	75 µΩ	20 pH	
L3	Proc A sou–h - sense	600 µΩ	160 pH	
L4	Proc B sou–h - sense	600 µΩ	160 pH	
L5	Proc A nor–h - sense	600 µΩ	160 pH	
L6	Proc B nor–h - sense	600 µΩ	160 pH	
L7	Proc A nor–h - Proc B north	1.2 µΩ	320 pH	

12.17 Validation Testing

The processor VCCSENSE and VSSSENSE pins should be routed to vias. The vias should be as close to the socket pins as possible and should be connected with a low impedance trace. As these signals provide measurement points to verify adherence to the proces'or's VCC specifications, the vias need to be accessible to measurement equipment.

Intel recommends the following guideline when measuring the transients on the processor VCC. The measurement should be done across the VCC and VSS pins on processor socket. Use an oscilloscope with 100 MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 mΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe. Some probes have a very significant level of inherent noise. Attempt to minimize noise by investigating different probes. Use a differential probe to make the voltage measurements. The bandwidth of the probe should be no less than the oscilloscope. Ensure all connections from oscilloscope to motherboard pin are good and have a very low contact resistance.

12.17.1 Generating and Distributing GTLREF[3:0]

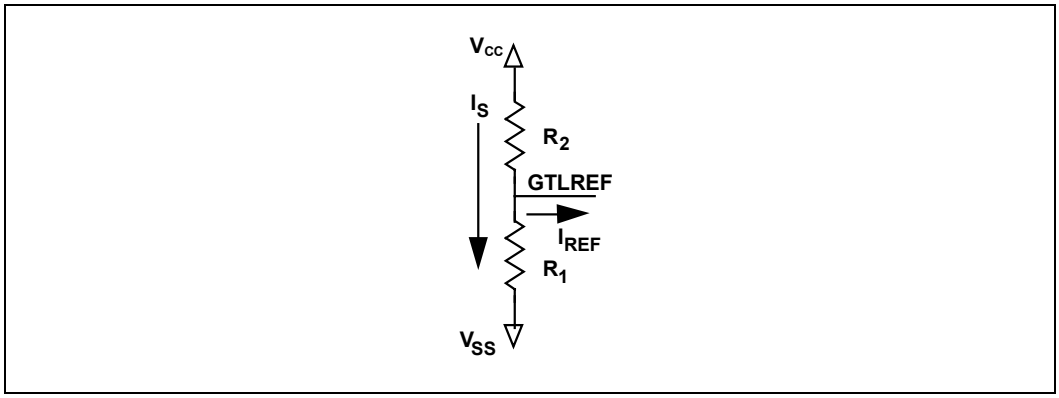
The GTLREF[3:0] pins are low current inputs (less than 15 µA each) to the differential receivers within each of the components on the AGTL+ bus. A simple voltage divider can generate GTLREF[3:0]. The GTLREF[3:0] inputs must meet the ± 2% specification.

Equation 15 uses $R_1 = 2 \times R_2$ to generate a GTLREF set at a nominal value of 2/3 VCC_CPU. The following figure illustrates using 1% resistors to generate the GTLREF specification of 2/3 VCC_CPU ± 2%.

Equation 15. Creating GTLREF of 2/3 VCC_CPU

$$V_{REF} = V_{CC} \times \frac{R_1}{R_1 + R_2} = V_{CC} \times \frac{2 \times R_2}{2 \times R_2 + R_2} = \tfrac{2}{3} V_{CC}$$

Figure 157. GTLREF Divider



R_1 and R_2 should be small enough values that the current drawn by the GTLREF inputs (I_{REF}) is negligible versus the current caused by R_2 and R_1.

A complete analysis of this circuit's currents into and out of the center node, as in Equation 16, will provide the final GTLREF of the circuit. *n* is the number of I_{REF} inputs supplied by the divider.

Equation 16. Node Analysis

$$I(R_2) = I(R_1) + n \times I_{REF}$$

Plugging in for the currents and rearranging gives:

Equation 17. Node Analysis in Terms of Voltage

$$\frac{V_{CC} - GTLREF}{R_2} - \frac{GTLREF}{R_1} = n \times I_{REF}$$

Which leads to:

Equation 18. Solving for GTLREF

$$GTLREF = \frac{V_{CC}/R_2 - n \times I_{REF}}{1/R_2 + 1/R_1}$$

The worst-case GTLREF should be analyzed with I_{REF} at the maximum and minimum values determined for the number of loads being supplied. If the number of loads can change from model to model because of upgrades, this should be taken into account as well. Analyze Equation 18 with R_1 and R_2 at the extremes of their tolerance specifications.

12.17.2 GTLREF [3:0]

Intel recommends two voltage dividers for each processor and one for chip-set component. Assume a maximum of 15µA of leakage current per load. Note that these leakage currents can be positive or negative.

The following discussion illustrates using a single voltage divider to support two GTLREF Loads assuming VCC_CPU of 1.7 V. Using 1% resistors for the voltage divider in Figure 157, make R_1 a 100 Ω resistor, and use 49.9 Ω for R_2. This creates a static usage of 10.7 mA (1.7V/149.9 Ω) per voltage divider. After looking at all combinations of R_1 and R_2 (above and below tolerance) and I_{REF} (±30 µA), the worst-case solution for Equation 18 can be found with I_{REF} at 30 µA, R_1 at the low end of its tolerance specification (99 Ω), and R_2 at the high end of its tolerance specification (50.4 Ω). This yields:

Equation 19. Resistor Tolerance Analysis

$$V_{REF} = \frac{1.7/50.4 - .000030}{1/50.4 + 1/99} = 1.1256V$$

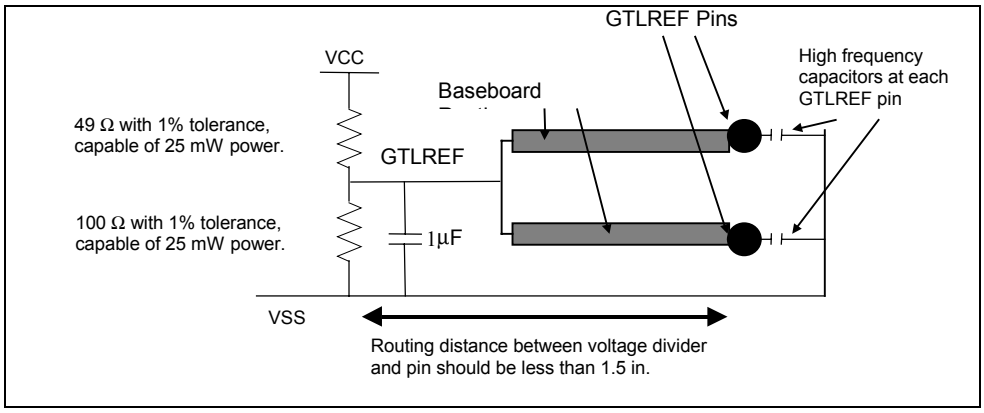
Since the target of 2/3 of VCC_CPU is 1.133 V, this setting is within 0.7% of the 2/3 point and satisfies the 2% specification. A spreadsheet program allows the reader to easily verify the other corners. Varying over its tolerance range has minimal effect.

These values chosen for R_1 and R_2 have additional benefits: The parallel combination terminates the GTLREF line to 33 Ω. These generally available resistance values reduce resistor cost.

Decouple GTLREF[3:0] at each pin with a 220 pF capacitor to V_{SS}. Decoupling GTLREF to V_{SS} at the voltage dividers with a 1 µF capacitor may further enhance the ability for GTLREF to track VCC_CPU.

When routing GTLREF to the pins, use a 30 mil–50 mil trace (the wider the better) and keep it as short as possible (less than 1.5 inches). Also, keep all other signals at least 20 mils away from the GTLREF trace. This provides a low impedance line without the cost of an additional plane or island. Because of the placement of the GTLREF pins on the processor, it may not be possible or convenient to route all four pins from one voltage divider. It is acceptable to use more than one voltage divider with decoupling at each voltage divider and each pin.

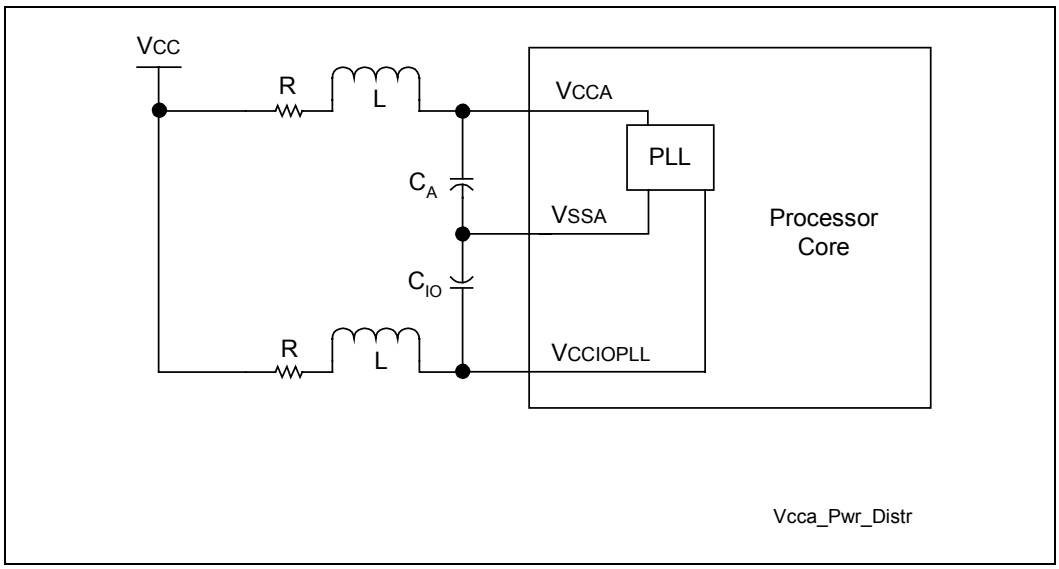
Figure 158. Suggested Processor GTLREF Design



12.17.3 Filter Specifications for VCCA, VCCIOPLL, and VSSA

VCCA and $V_{CCIOPLL}$ are power sources for processor internal PLL's. These supplies are enhanced with low pass filters generated for the processor's VCC_CPU. Intel Xeon processors have internal PLL clock generators that are analog in nature and require quiet power supplies for minimal jitter. Jitter is detrimental to a system; it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). The general desired topology is shown in Figure 159. Not shown in the figure is the parasitics of connecting traces, circuits, and components.

Figure 159. Processor PLL Filter Topology



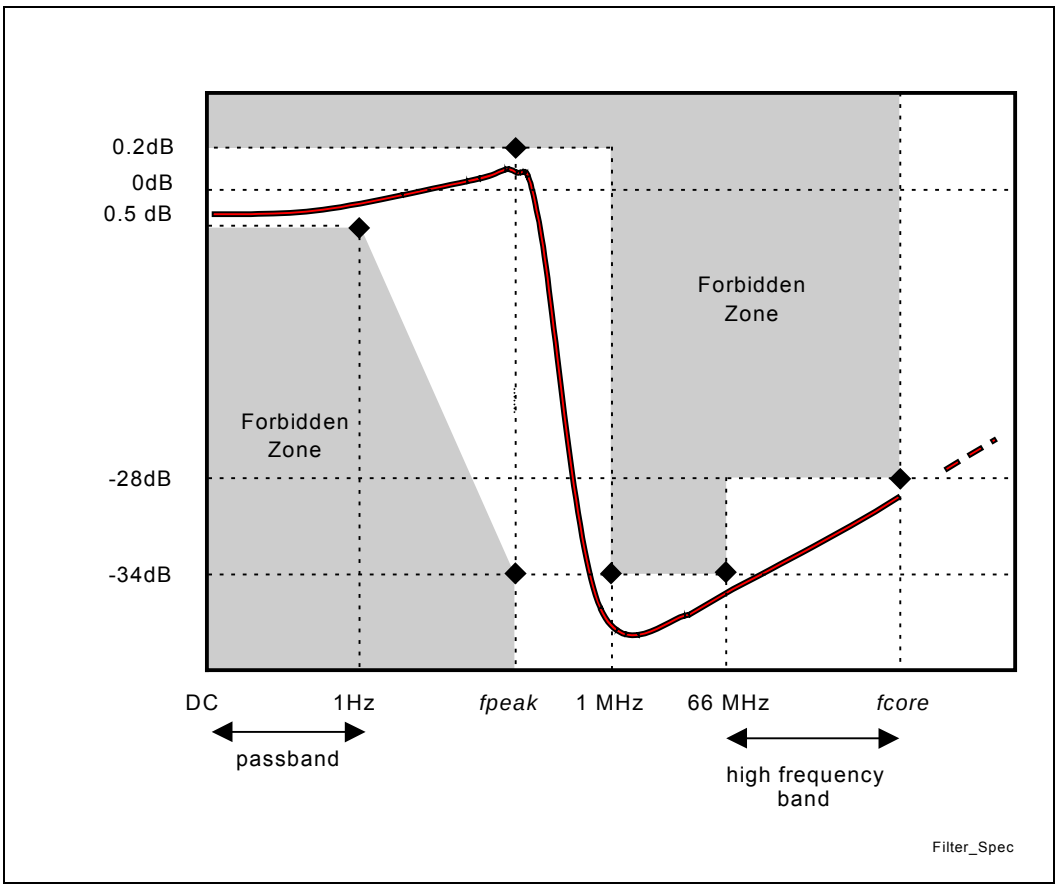
The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity we are addressing the recommendation for VCCA filter design. The same characteristics and design approach is applicable for $V_{CCIOPLL}$ filter design.

The AC low-pass specification, with input at VCC_CPU and output measured across the capacitor, is as follows:

- < 0.2dB gain in pass band
- < 0.5dB attenuation in pass band < 1Hz (see DC drop in next set of requirements)
- >34dB attenuation from 1 MHz to 66 MHz
- >28dB attenuation from 66 MHz to core frequency

The filter specification (AC) is graphically shown in Figure 160.

Figure 160. Processor PLL Filter Specification



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond *fcore*.
3. *fpeak*, if it exists, should be less than 0.05 MHz.

Other requirements

- Use shielded type inductor to minimize magnetic pickup.
- Filter should support at least 30 mA of DC current.
- DC voltage drop from VCC_CPU to the processor interposer pin VCCA should be < 33 mV, which in practice implies series R < 1.1 Ω; also means pass band (from DC to 1Hz) attenuation < 0.5 dB for VCC_CPU = 1.1V, and <0.35dB for VCC_CPU = 1.7V.

The following tables list some recommended components for the filter. Values in table are for reference only. Refer to vendor documentation for valid specifications.

Table 59. Component Recommendation — Inductor

Part Number (Ref Designator)	Value	Tol.	SRF	Rated I	DCR
TDK MLF2012A4R7KT (L1)	4.7uH	10%	35MHz	30mA	0.56Ω (1Ω max)
Murata LQG21N4R7K10 (L2)	4.7uH	10%	47MHz	30mA	0.7Ω (± 50%)

Table 60. Component Recommendation — Capacitor

Part Number	Value	Tolerance	ESL	ESR
Kemet T495D336M016AS	33uF	20%	2.5nH	0.225Ω
AVX TPSD336M020S0200	33uF	20%	see note	0.2Ω

NOTE: Refer to the vendor datasheet for the AVX TPSD336M020S0200 component ESL value.

To satisfy damping requirements, total series resistance in the filter (from VCC_CPU to the top plate of the capacitor) must be at least 0.35 Ω. It includes the minimum DCR of the inductor, and any resistance (routing or discrete components) between VCC_CPU and capacitor top plate. Keep the routing short and wide. If the total is less than 0.35 Ω, add a discrete resistor to make up the difference. For example, if the selected filter inductor has a minimum of 0.1 Ω DCR and a negligible routing resistance (less than 10 mΩ), add a discrete resistor R1 of approximately 0.3 Ω.

The total maximum resistance in each routing cannot be greater than 1.1 Ω as measured from VCC_CPU (more specifically, the baseboard via that connects the PLL filter to the VCC_CPU plane) to the processor interposer pin. (Refer to Figure 161 and Figure 162 for recommended filter circuits.) This path includes the total trace resistance (denoted “R-TRACE” in the following figures), discrete resistor (if needed), inductor DCR, and Socket 603 resistance (0.025 Ω). It is important to note that “R-TRACE” includes the total trace resistance between VCC_CPU and the processor socket pin, but is represented in the figures as a single resistor to simplify the circuit representation.

Other routing requirements:

- C should be as close as possible to VCCA and VSSA pins in the socket (typically < 0.02 Ω per route).
- Route away from clocks and fast switching signals.
- VCCA route should be parallel and next to VSSA route (to minimize loop area).
- VCCIOPLL route should be parallel and next to VSSA route (to minimize loop area).
- L should be close to C; any routing resistance should be inserted between VCC_CPU and L.
- Any discrete R (if needed to meet minimum resistance) should be inserted between VCC_CPU and L.

Figure 161. Filter Circuit with Discrete Resistors

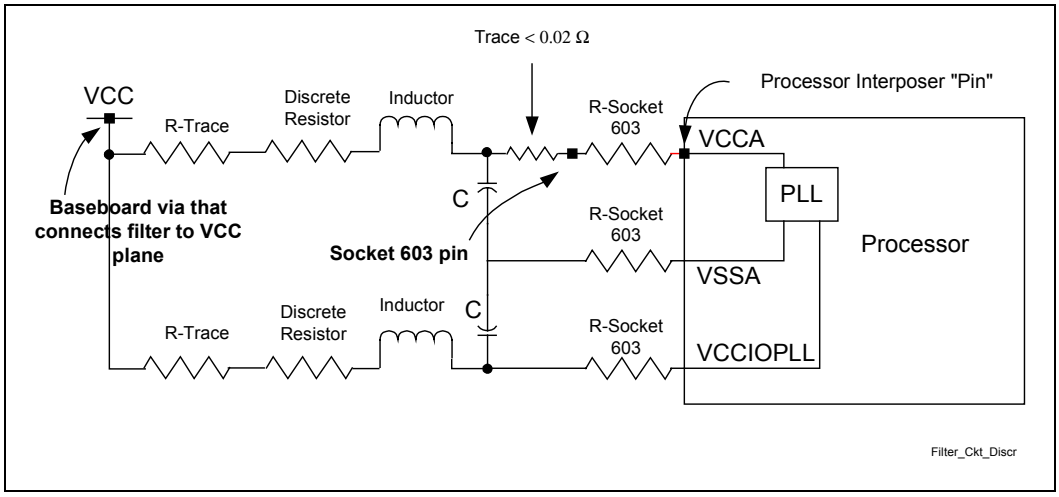
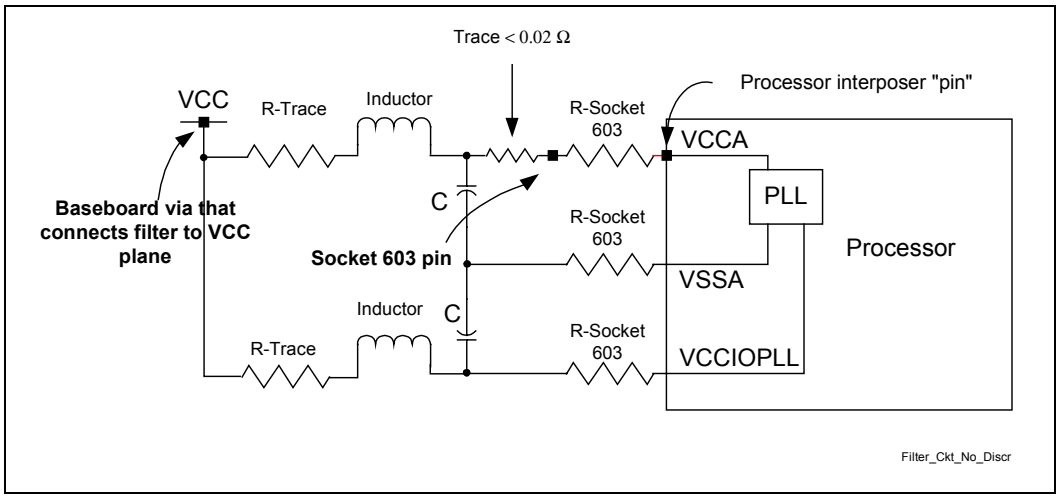


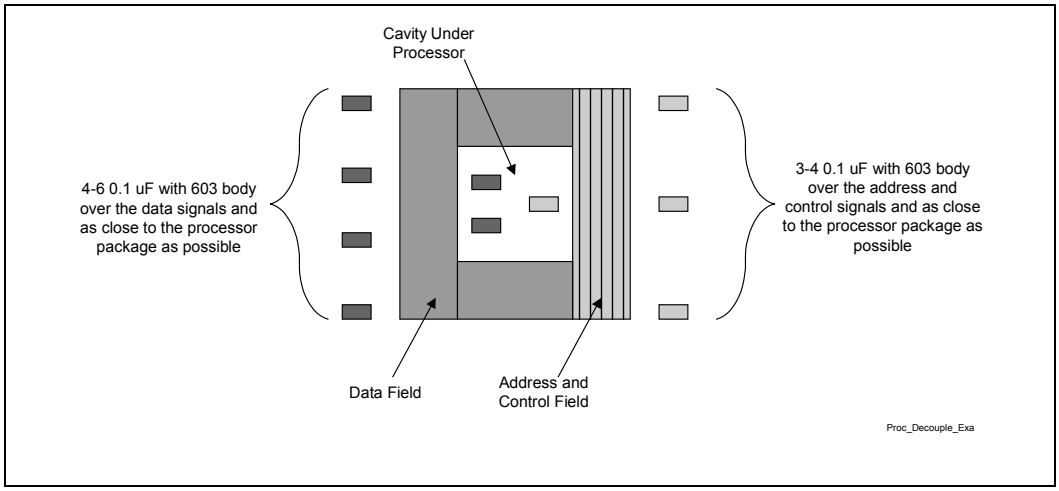
Figure 162. Filter Circuit without Discrete Resistors



In addition high frequency decoupling may be required for signal integrity. System boards designed using striplines with VCC_CPU and V_{SS} references should not require high frequency decoupling beyond that recommended above. In systems using microstrip configurations, a return path discontinuity will exist between the processor and the baseboard because the baseboard traces have only one reference plane. These systems should distribute decoupling capacitors as shown in Figure 163 and described as follows:

- 4 minimum, 6 preferred 1 µF capacitors with 0805 packages distributed evenly over the data lines.
- 3 minimum, 4 preferred 1 µF capacitors with 0805 packages distributed evenly over the address and control lines.
- All capacitors placed as close to the processor package as the keepout zone allows.

Figure 163. Example of Decoupling for a Microstrip Baseboard Design



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13 Chipset Power Distribution Guidelines

13.1 Definitions

Term	Definition
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered.
Full-power operation	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state and the S1 (CPU Stop-Grant state) state.
Suspend operation	During suspend operation, power is removed from some components on the motherboard. The Customer Reference Board supports two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).
Core power rail	A power rail that is only on during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply.
Standby power rail	A power rail that in on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is: 3.3 VSB. There are other standby rails that are created with voltage regulators on the motherboard.
Derived power rail	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 1.8 VSB is usually derived (on the motherboard) from 5 VSB using a voltage regulator.
Dual power rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during suspend operation and derived from a core supply during full-power operation. Note that the voltage on a dual power rail may be misleading.

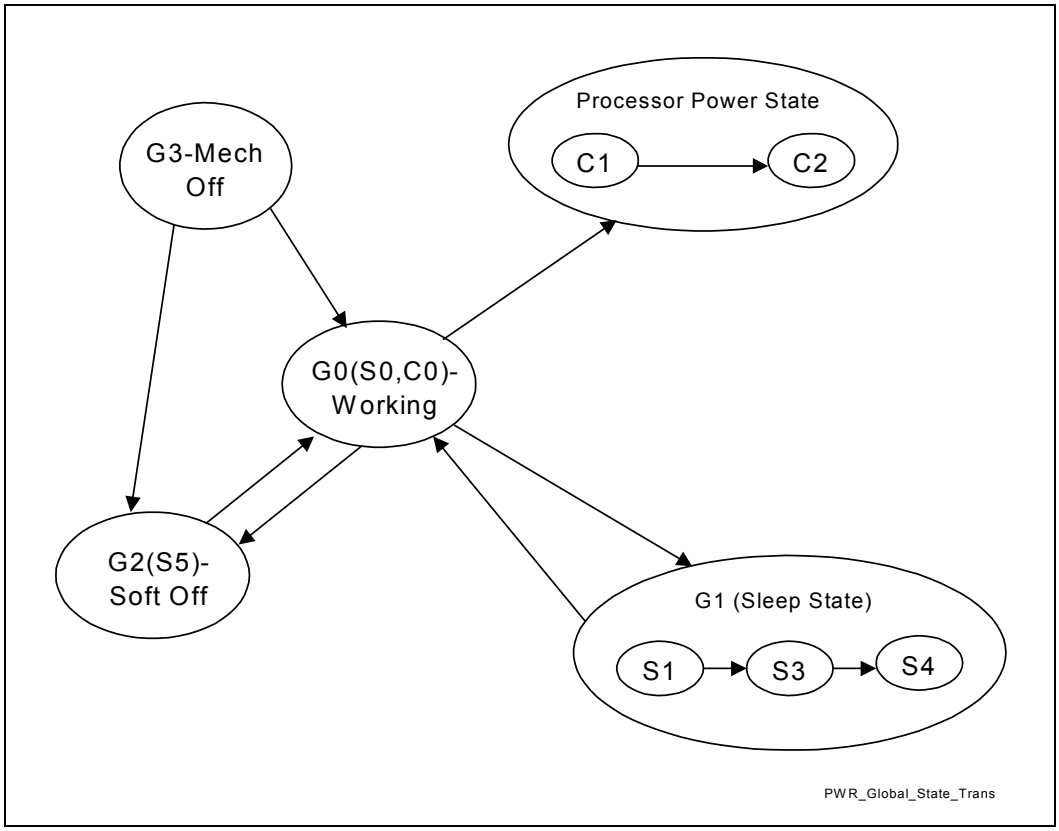
13.2 Power Management

The Intel 860 chipset-based platform implements the ACPI mechanism software and hardware that enable the system to minimize system power consumption, manage system thermal limits, and maximize the battery life. This implementation involves tradeoffs among system speed and noise.

13.2.1 ACPI Hardware Model

The Intel 860 chipset-based desktop supports both legacy and ACPI operations which involves sequencing the platform between the various global system states (G0-G3). The following figure depicts global states and the transitions. For complete detail of the mechanisms involved in transition from any of the global states refer to the Advanced Configuration and Power Interface Specification (ACPI).

Figure 164. Global System Power States and Transition



13.2.2 Thermal Design Power

The thermal design power numbers are an estimation of the maximum expected power generated by a component in a realistic application. It is based on extrapolations in both hardware and software technology over the product life. It does not represent the expected power generated by a power virus. The ICC max-sustained (WCRA) numbers are an estimation of the maximum expected current generated within a die section in a realistic application such as an application that executes extensive memory reads/writes.

Refer to the *Intel 860 chipset: 82860 Memory Controller Hub (MCH) Datasheet* and the *Intel® 860 Chipset Thermal Considerations Application Note* for additional thermal package characteristics.

Table 61. Intel® 860 Chipset MCH and Intel® ICH2 Thermal Design Power

Parameter	Icc Max Sustained Current (A)
MCH • MCH (UP) Typical Thermal Design Power = 6.5 W • MCH (UP) Maximum Thermal Design Power = 8.6 W	
1.8 V Core	3.9
1.5 V VDDQ AGP I/O	.37
1.8 V VDD HL 16 B&C	0.79
1.6V VTT	2.2
ICH2 • ICH2 Max Thermal Design Power = 1.6W ± 15%	
1.8 V Main Logic	0.30
1.8 V (Stand By) Resume Logic + 1.8 V LAN	0.040
3.3 V Main I/O	0.41
3.3 V (Stand By) Resume Logic	0.062
Processor I/F (1.3 ~ 2.5)	200 µA

NOTE: It is important to understand that values stated for the maximum sustainable current (Icc) of ICH2 are subject to change.

13.3 Intel® 860 Chipset MCH Power Sequencing Requirement

The Intel 860 chipset MCH requires VCC1.8, VDDQ, and VTT power supplies for operation. To avoid forward-biasing ESD protection-diodes from the IO to Core power supplies, it is necessary that the VCC1.8 power supply ramp up ahead (see Figure 165) of the VDDQ and VTT power supplies. For the same reason, it is necessary to have the VCC1.8 power supply ramp down later than the VDDQ and VTT power supplies. If this cannot be provided, it is important that the VCC1.8 supply lag (see Figure 166) the IO supplies by no greater than 1.0V. There are no dependencies between VDDQ and VTT supplies.

Figure 165. Desired Mode of Power Sequencing

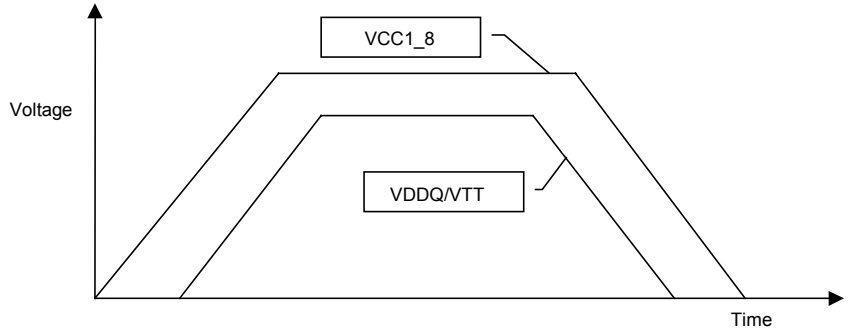
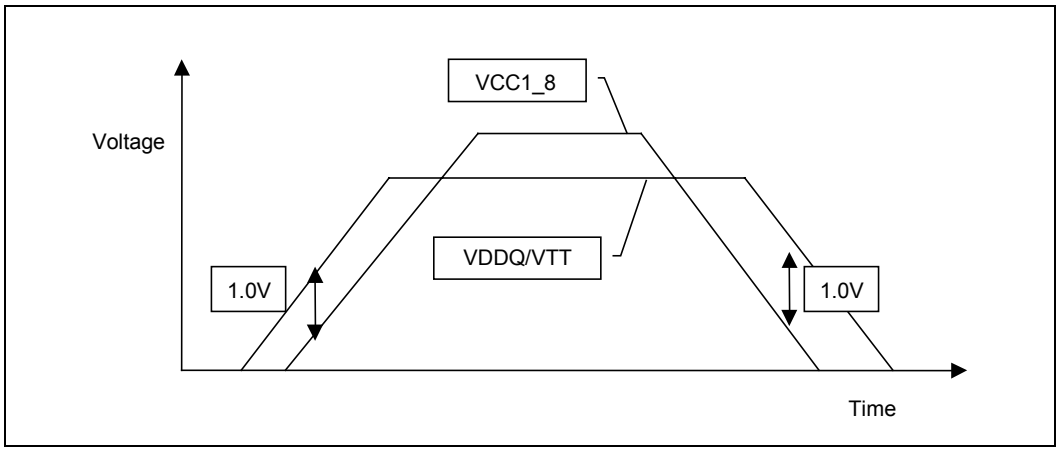


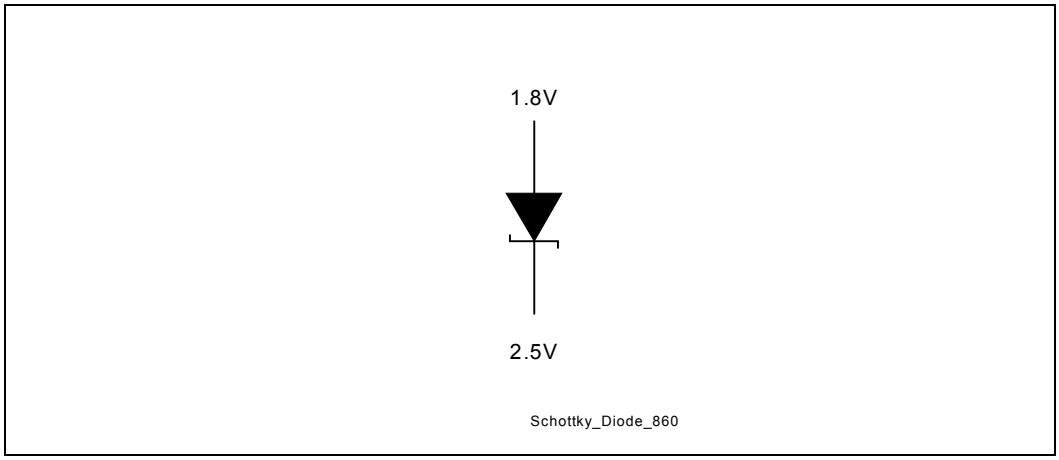
Figure 166. Optional Mode of Power Sequencing



13.4 Vterm/Vdd Power Sequencing Requirement

Power to the Direct RDRAM device termination resistors (Vterm) must follow the power to the Direct RDRAM device Core. A Schottky Diode can be placed between the 1.8 V and 2.5 V to ensure this power-up sequence.

Figure 167. 1.8 V and 2.5 V Power Sequence (Schottky Diode)



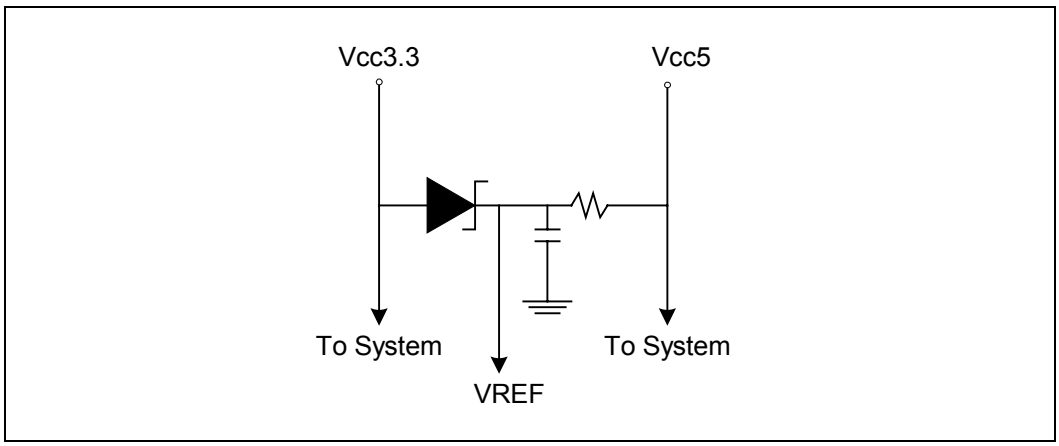
13.5 ICH2 5VREF and VCC3.3 Sequencing Requirement

V5REF is the reference voltage for 5V tolerance on inputs to the ICH2. V5REF must be powered up before or simultaneously to Vcc3_3. It must also power down after or simultaneous to Vcc3_3. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 143 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend the only signals that are 5V tolerant are USB pins (both over-current and data lines). If USB is not implemented in the system then V5REF_SUS can be connected to the VccSus3_3 rail. Otherwise when USB is supported, V5REF_SUS must be connected to 5V_AUX which remains powered during S5.

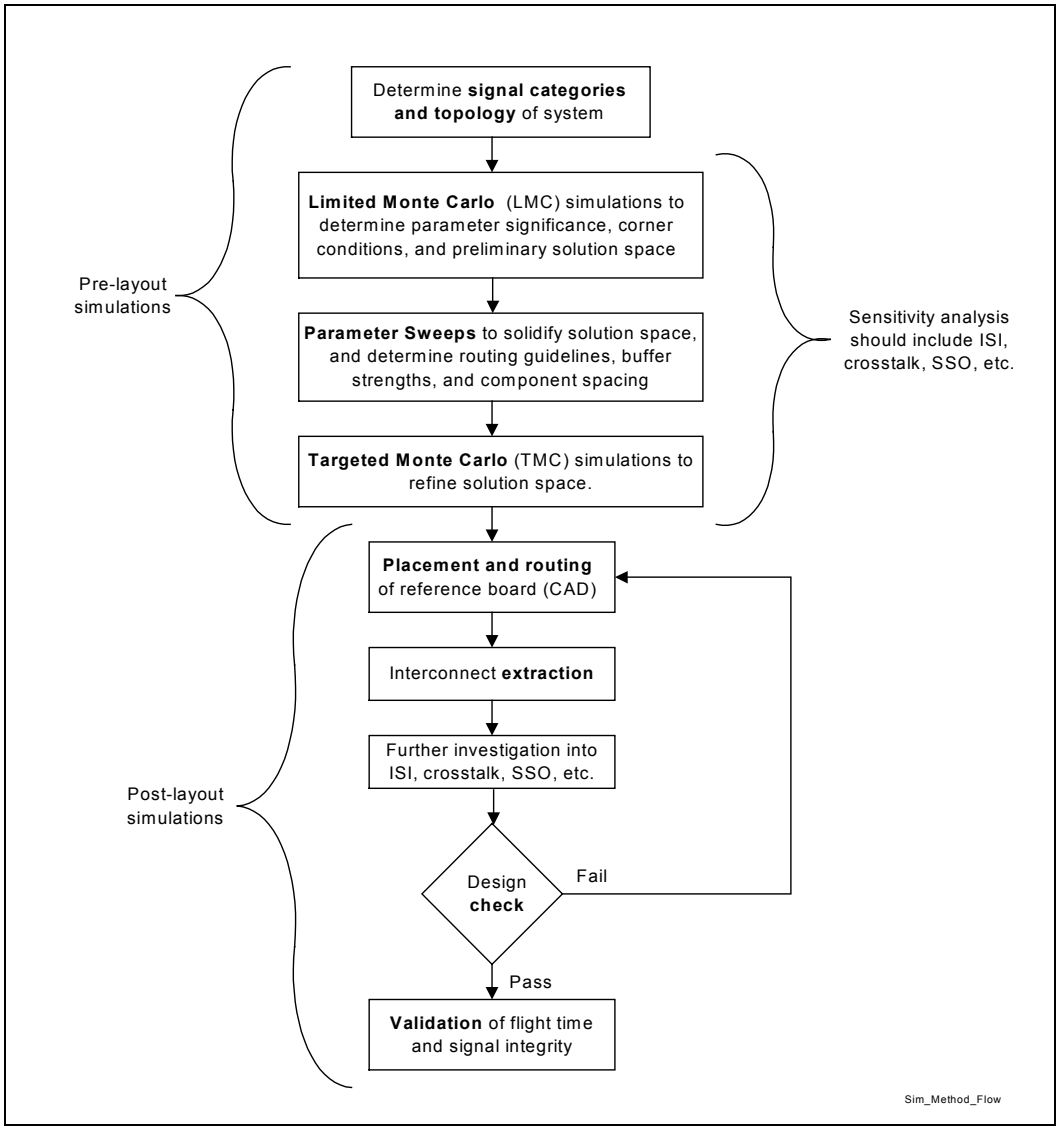
Figure 168. 5VREF Sequencing Circuit



14 Methodology for Determining Topology and Routing Guidelines

This section documents the simulation methodology that was used to derive the topology and routing guidelines presented in this design guide.

Figure 169. Simulation Methodology Flowchart



The design process should begin with an initial timing analysis and topology definition. Pre-layout analog simulations should be performed. These pre-layout simulations will help define routing rules prior to placement and routing. After routing, the interconnect database can be extracted and post-layout simulations can be performed to refine the timing and signal integrity analysis. The analog simulations should be validated when actual systems become available.

Pre-layout simulations provide a detailed picture of the working solution space that meets flight time and signal quality requirements. By basing board layout guidelines on the solution space, the iterations between layout and post-layout simulation can be reduced.

Intel recommends running simulations at the device pads for signal quality and for timing analysis. However, simulation results at the device pins may be used later to correlate simulation performance against actual system measurements.

Pre-layout analysis includes a sensitivity analysis using parametric sweeps. Parametric sweep analysis involves varying one or two system parameters while all others such as driver strength, package Z0, and S0 are held constant. This way, the sensitivity of the proposed bus topology to varying parameters can be analyzed systematically. Sensitivity of the bus to flight time and signal quality should be covered. Suggested sweep parameters include trace lengths, termination resistor values, and any other factors that may affect flight time, signal quality, and feasibility of layout. Minimum flight time and worst signal quality are typically analyzed using fast I/O buffers and interconnect. Maximum flight time is typically analyzed using slow I/O buffers and slow interconnects. However, fast I/O buffers and various baseboard and package combinations have been found to have violating signal quality. It is advisable to perform some level of Monte Carlo analysis, which includes all possible parameters.

Outputs from each sweep should be analyzed to determine which regions meet timing and signal quality specifications. To establish the working solution space, find the common space across all the sweeps that result in passing timing and signal quality. The solution space should allow enough design flexibility for a feasible, cost-effective layout.

The effects of ISI and return path irregularities are difficult and tedious to simulate with 100% accuracy. Intel has found through experimentation and targeted simulations that these effects can have a significant impact on the primary signal. Because of this work, Intel has been able to more accurately predict the effects. Given the complexity of a quad-pumped source synchronous bus architecture, it was necessary for Intel to tighten the component timings and bus requirements in order to provide a viable routing solution space. Because of this, Intel strongly recommends adhering to the design guideline requirements and component specifications.

14.1 Timing Methodology

The timing equations used for both source synchronous and common clock parameters are derived in the following sections.

14.1.1 Source Synchronous

In a source synchronous bus the clock (or strobe) is driven from the same source as the signal it will sample. The strobe and the signal both propagate to the receiver via the PCB. The receiver then uses the strobe to sample the signal. This eliminates the need to account for worst-case flight times and, in theory, will significantly increase the maximum bus speed.

14.1.1.1 Setup Time

Figure 170 shows the setup timing diagram for a source synchronous bus design. Equation 20 gives the total loop equation derived from the timing diagram.

Equation 20. Source synchronous setup time

$$T_{co}(strobe) + T_{flight}(strobe) - T_{setup} - T_{margin\_setup} - T_{co}(data) - T_{flight}(data) = 0$$

- T_{co}(strobe)[(data)] is the driver delay of the strobe [data]
- T_{flight}(strobe)[(data)] is the flight time of the strobe [data] interconnect
- T_{setup} is the recei'er's setup requirement
- T_{margin} is the available timing margin for the setup time

The loop equation can be simplified and solved for T_{margin_setup}. The equation can be broken into two parts, valid before and interconnect skew. Then, the setup margin can be determined.

Equation 21. Source Synchronous, Valid Before

$$T_{vb} = T_{co}(data)_{\max} - T_{co}(strobe)_{\min}$$

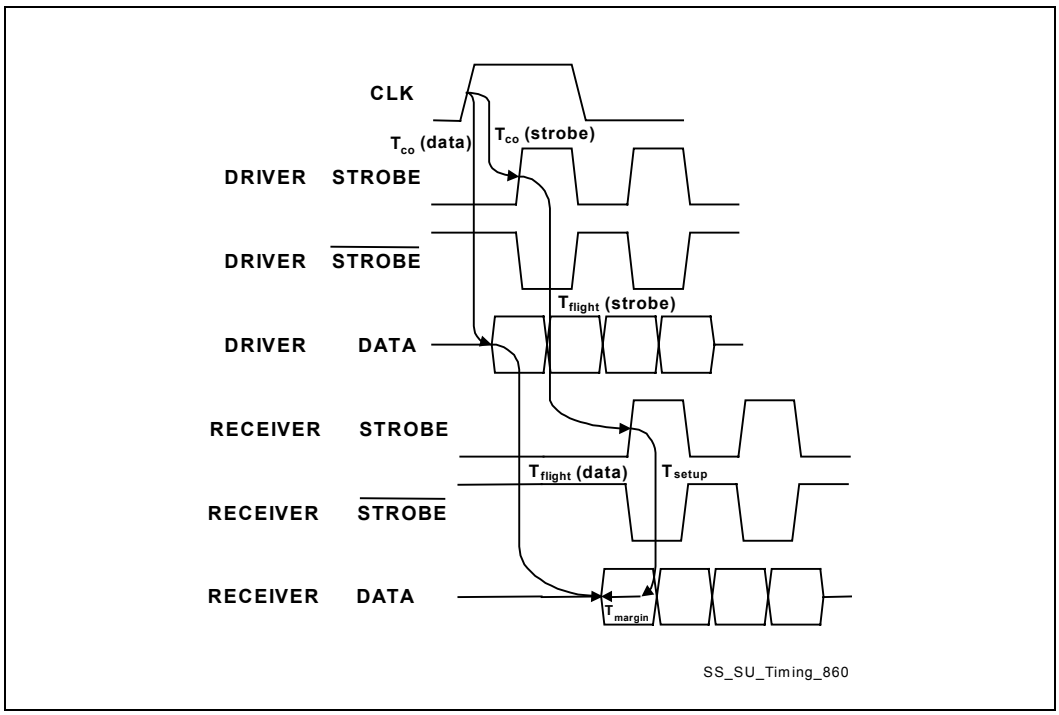
Equation 22. Source Synchronous, Interconnect Skew

$$T_{skew,\max} = T_{flight}(data)_{\max} - T_{flight}(strobe)_{\min}$$

Equation 23. Source Synchronous Setup Margin

$$T_{margin\_setup} = -T_{vb,\min} - T_{skew,\max} - T_{setup}$$

Figure 170. Source Synchronous Timing Diagram for Setup Time



14.1.1.2 Hold Time

The hold timing diagram for a source synchronous bus design is shown in Figure 171. The total loop equation is derived from the hold timing diagram.

Equation 24. Source synchronous loop equation for hold timing diagram

$$T_{co}(data) + T_{flight}(data) - T_{margin\_hold} - T_{hold} - T_{flight}(strobe) - T_{co}(strobe) = 0$$

- T_{co}(strobe)[(data)] is the driver delay of the strobe [data]
- T_{flight}(strobe)[(data)] is the flight time of the strobe [data] interconnect
- T_{hold} is the receiver setup requirement
- T_{margin} is the available timing margin for the setup time

The loop equation can be simplified and solved for T_{margin_hold}. The equation can be broken into two parts, valid before and interconnect skew. Then, the hold margin can be determined.

Equation 25. Source Synchronous, Valid After

$$T_{va} = T_{co}(data)_{\min} - T_{co}(strobe)_{\max}$$

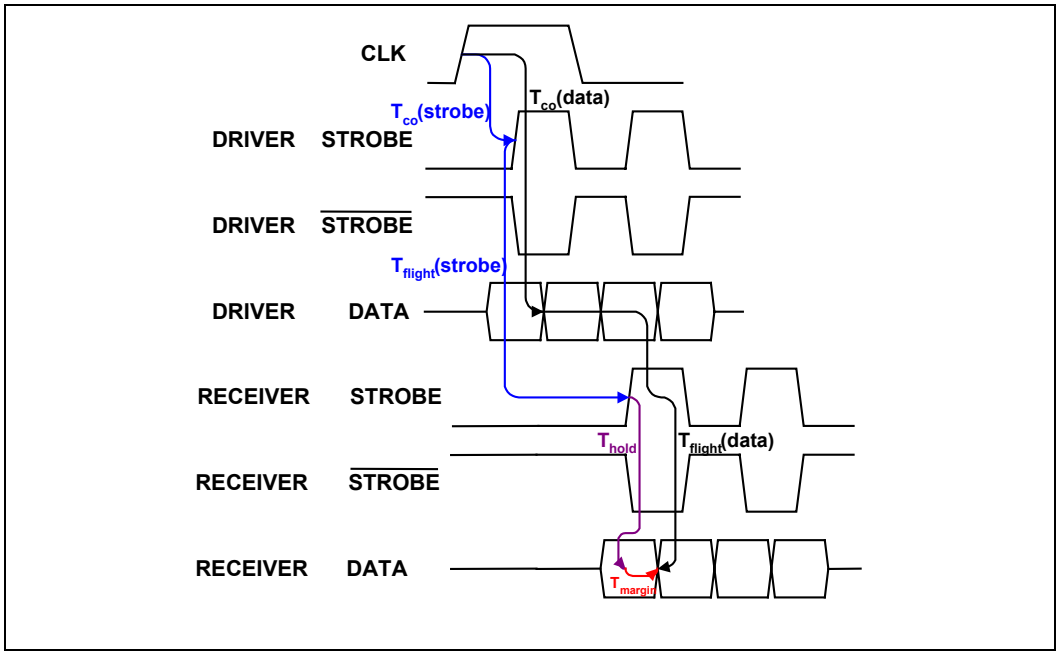
Equation 26. Source Synchronous, Interconnect Skew

$$T_{skew,\min} = T_{flight}(data)_{\min} - T_{flight}(strobe)_{\max}$$

Equation 27. Source Synchronous, Hold Margin

$$T_{margin\_hold} = T_{va,\min} + T_{skew,\min} - T_{hold}$$

Figure 171. Source Synchronous Timing Diagram for Hold Time



14.1.2 Common clock

A block diagram of a circuit that was used to develop the basic timing equations is shown in Figure 172.

14.1.2.1 Setup Margin

Figure 173 shows the setup timing diagram that was used to develop the final timing equations for the setup margin.

Equation 28. Common Clock Loop Equation

$$T_{cyvle} + T_{drv\_clk}(B) + T_{prop\_clk}(B) - T_{jitter} - T_{setup} - T_{m\,arg\,in} - T_{prop} - T_{drv} - T_{prop\_clk}(A) - T_{drv\_clk}(A) = 0$$

- T_{cycle} is the cycle time
- T_{drv_clk}(A)[(B)] is the delay of the clock buffer circuit connected to device A [B]
- T_{prop_clk}(A)[(B)] is the delay of the interconnect between the clock buffer and device A [B]
- T_{drv} is the delay of the output buffer for the data signal on device A (T_{CO})
- T_{prop} is the interconnect delay between device A and B
- T_{setup} is the setup time required by the buffer
- T_{jitter} is the clock cycle-to-cycle jitter

Figure 172. Circuit Used to Develop the Common Clock Timing Equations

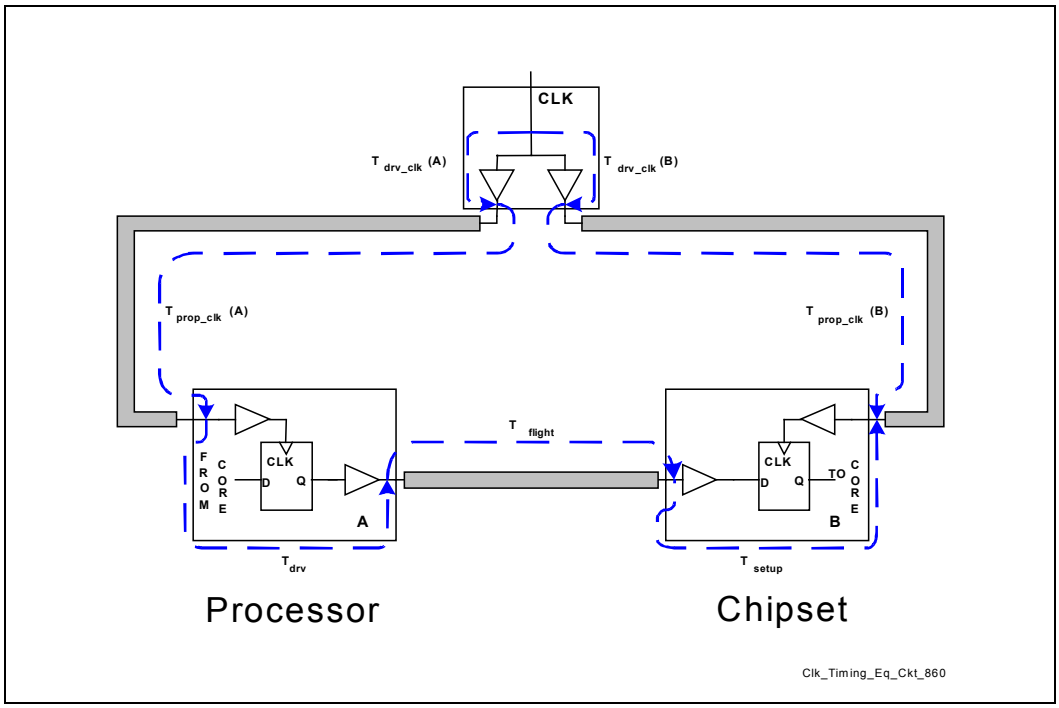
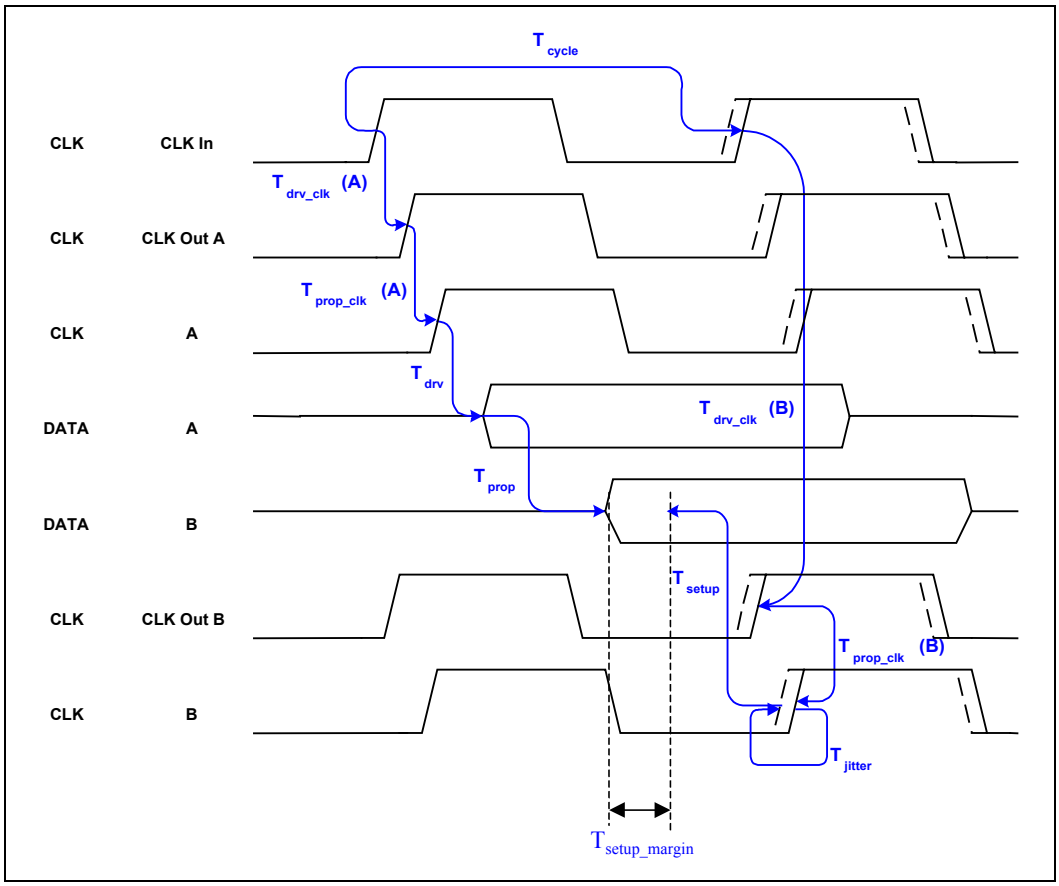


Figure 173. Timing Diagram Used to Determine the Common Clock Setup Timing Equations



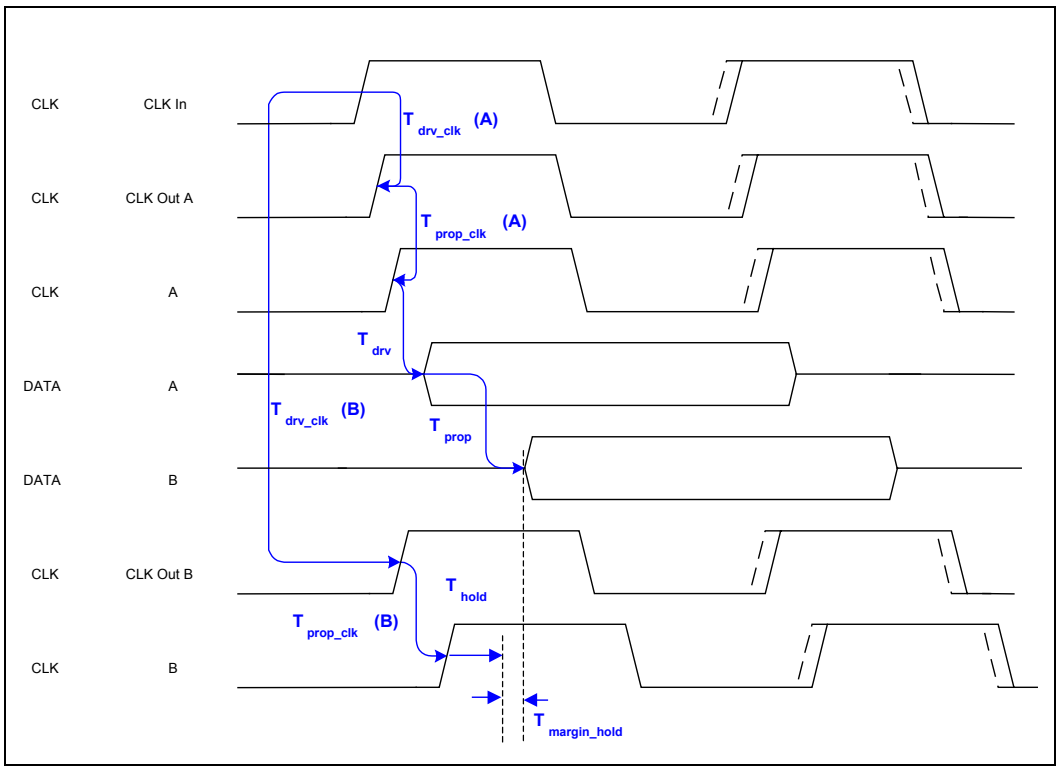
14.1.2.2 Hold Margin

Figure 174 illustrates the timing diagram that was used to develop the final timing equations.

Equation 29. Common Clock Hold Margin

$$T_{margin\_hold} = T_{drv} + T_{prop} - T_{hold} - T_{skew\_hold}$$

Figure 174. Timing Diagram Used to Determine the Common Clock Hold Timing Equations



14.1.3 Timing Spreadsheet

A timing spreadsheet should be created to keep track of each sig'al's timing margins.

To effectively manage the timing spreadsheet the following recommendations should be adhered to.

- All assumptions should be stated in the spreadsheet file
- Simulated and measured timings should be tracked separately
- Each timing component has an owner and revision date
- Rising and falling edges should be tracked separately

14.2 Simulation Methodology

This sections outlines the simulation methodology used to determine the topology and routing guidelines.

14.2.1 Design Optimization

The layout for a high-speed bus design can be complex. High-frequency phenomena that previously had second or third order effects on system level performance are becoming first order as bus speeds continue to increase. It should be noted that for a high-speed bus, fixing a problem in one area of the board might create another problem in a different area.

The design recommendations of this design guide have been written to provide enough detail to allow a platform designer to go right into layout designs and only perform post-route simulations. If any of the recommendations are not followed, then it is advisable to follow the complete simulation process described below in order to accurately quantify your solution space.

14.2.2 Signal Categories and Topology Options

The first task of the bus design process is to identify all signal categories that are contained within the design. Categories should be defined by signal buffer type, timing requirements, and topology similarities. The bus or component specification should provide help in this categorization.

Once signals have been categorized, all possible interconnect topologies for each signal group must be determined. This requires significant collaboration with the layout engineer and will be the direct result of a layout study. The optimum part placement and all possible interconnect solutions should be determined. The layout study should produce a solution space that lists all possible interconnect topology options including line lengths, widths and spacing. Extensive simulations during the sensitivity analysis will be used to limit the solution space determined from the layout study. This limited solution space becomes a final design solution that meets all timing and signal quality specifications.

14.2.3 Sensitivity Analysis

A sensitivity analysis is used to determine the solution space for all aspects of the design. Every parameter in the system bus should be varied in simulations. The performance metrics, such as flight time, flight skew, and signal integrity are observed while each one of the variables is swept. The performance as a function of each variable is compared to the timing and signal quality specifications. As a result, limits are placed on each of the components. This produces a solution space that places strict limits on the system variables such as trace lengths, spacing, impedance, etc. The solution space will lead to design guidelines for the PCB and routing. Table 62 lists the primary system variables that should be considered in the system bus sensitivity analysis. The following table indicates the relative effect of each variable on system performance.

Table 62. System Variables to Consider for Sensitivity Analysis

System Variable	Impact on Timings and/or Signal Integrity
Trace/stub lengths	High
Trace impedance variations	High
ε_r variations	Low (variation is usually small)
Pattern dependency	Low to High (high for long lines)
Ground return path discontinuities	Unknown (presumed high)
Trace to trace spacing	High
AC losses	Moderate
Termination resistor variations	Low (if high tolerance resistors are used)
Layer to layer Zo and ε_r variations	Moderate
Serpentine spacing	Moderate
Simultaneous Switching Outputs (SSO)	Moderate
Inter-Symbol Interference (ISI)	Moderate

14.2.4 Signal Quality Metrics

The tight timing and low voltage characteristics of the system bus require clean reception of all signals. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swing will adversely affect system timings. Excessive ringback, and signal non-monotinicity cannot be tolerated because these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Additionally, over/undershoot can cause timing degradation due to the build up of inter-symbol interference (ISI) effects.

For these reasons, it is important that the designer work to achieve a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines.

14.2.4.1 Noise Margin

The receiver buffers are designed to switch at the threshold voltage. Because of several variables such as processor variations and system noise, the threshold voltage may change. This variation in the threshold voltage is known as the noise margin. For the processor the noise margin is assumed to be 100 mV above and 100 mV below the reference voltage, GTLREF.

Signal quality is measured by observing the linearity of the signal as it passes through the transition region (GTLREF ± 100 mV) and by observing any signal ringing into the noise margin region. The upper and lower noise margin levels are referred to as V_{IH} and V_{IL} respectively.

An edge is defined to be linear if it exhibits a linear shape between V_{IH} and V_{IL}. Figure 175 depicts a linear edge. Figure 177 depicts a nonlinear edge. For non-clock and non-strobe signals, the signal seen at the receiver should be linear between V_{IH} and V_{IL}. On a case-by-case basis where it can be shown that the timing can be met with no potential data corruption, it may not be necessary for the signal to be linear between V_{IH} and V_{IL}.

14.2.4.2 Ringback

Ringback is defined as the amount of voltage that 'rings' back towards the threshold voltage and is measured at the receiver. For non-clock and non-strobe signals, the signal at the receiver should not ringback into the noise margin region unless it can be shown that the timing can be met with no potential data corruption.

14.2.5 Timing Metrics

The timing metrics consists of flight time and flight time skew. Flight time is defined as the amount of time between the point where the signal on the unloaded driver (or loaded with a test load) crosses a certain threshold and the time where the signal crosses the threshold at the receiver. Flight time skew is the difference in flight times between two nets. Figure 175 illustrates the definition of flight time (assuming a linear edge from V_{IL} through V_{IH}). The flight time should be evaluated at V_{IL}, $V_{threshold}$, and V_{IH}. The methodology is to measure flight time at these three points and record the worst case. This is valid as long as the edge rate seen at the receiver is equal to the edge rate at which it was characterized (the tester edge rate). If the device was characterized at a different edge rate than the system edge rate, then the following procedures for setup and hold time calculations should be used.

14.2.5.1 Setup Flight Time

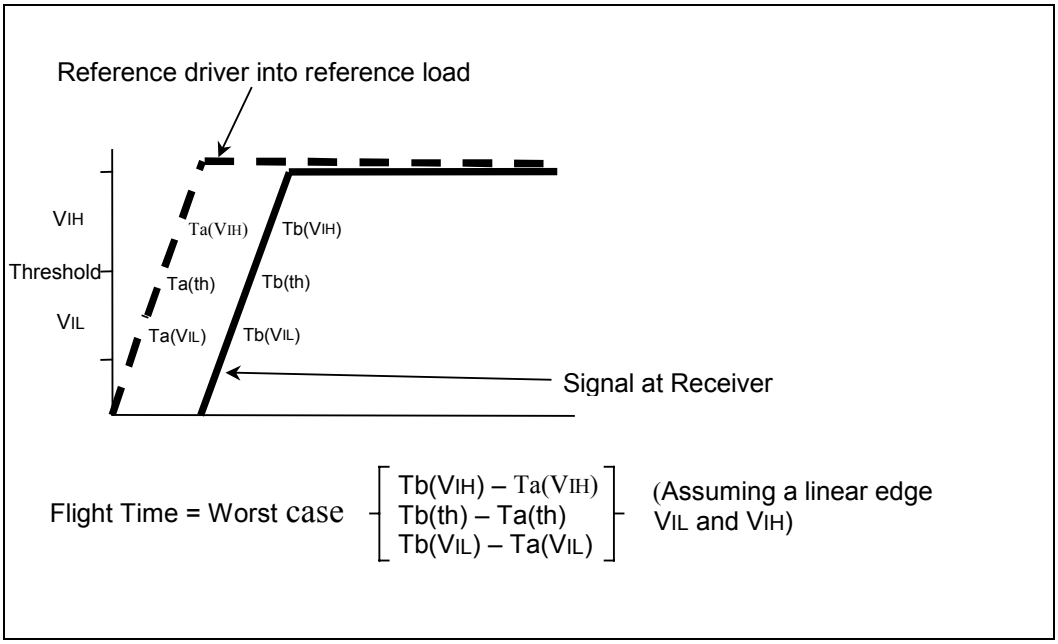
If the edge rate seen at the receiver is faster than the specified edge rate, then the traditional method should be used. If the edge rate seen at the receiver is slower than the specified edge rate, then the flight time must be extrapolated from V_{IL} or V_{IH} to $V_{threshold}$ at the specified edge rate. See Figure 176 for more details.

14.2.5.2 Calculating Flight Time for Signals with Corrupt Signal Quality

If non-linearity or ringback occurs between V_{IL} and V_{IH}, then the last crossing should be extrapolated back at the specified minimum edge rate to $V_{threshold}$. See Figure 177 and Figure 178.

The following figure shows the traditional method of calculating rising edge to rising edge flight time, assuming a linear edge from V_{IL} through V_{IH} at the receiver

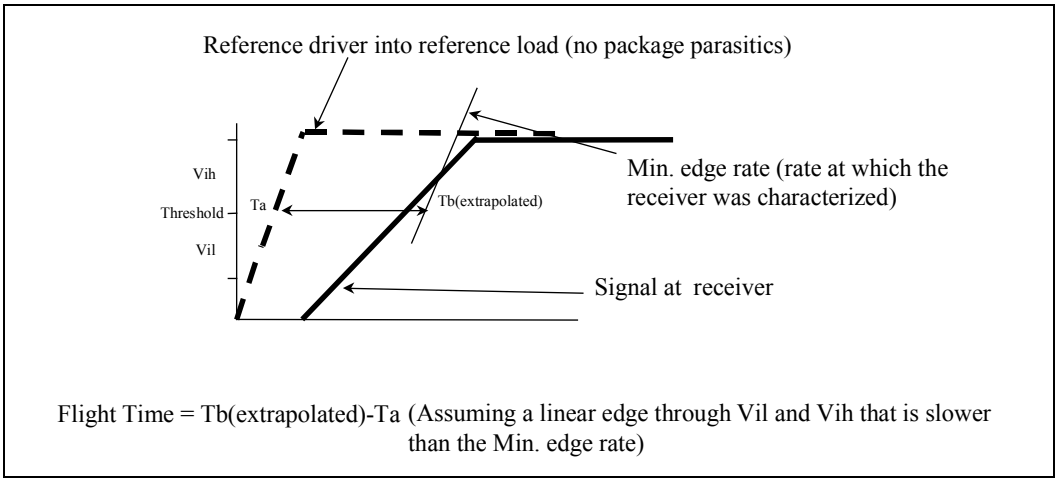
Figure 175. Calculating Rising Edge to Rising Edge Flight Time (Traditional Method)



NOTES:
1. Flight time skew is the difference in flight time between two nets.
2. Assuming a Linear Edge from V_{IL} through V_{IH} at the receiver.

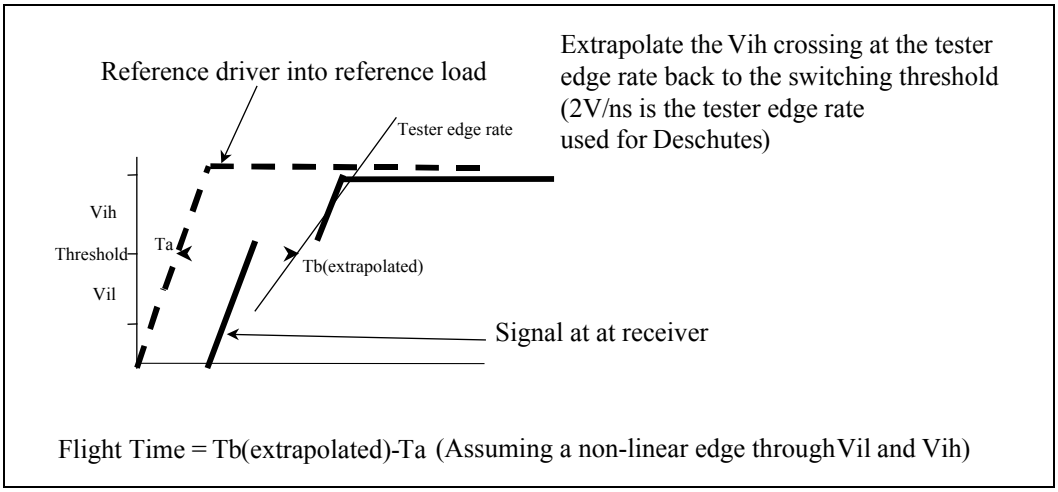
The following figure shows a method of calculating setup flight time when the edge rate seen at the receiver is slower than the specified edge rate.

Figure 176. Calculating Setup Flight Time (Receiver Edge Rate is Slower than Specified Edge Rate)



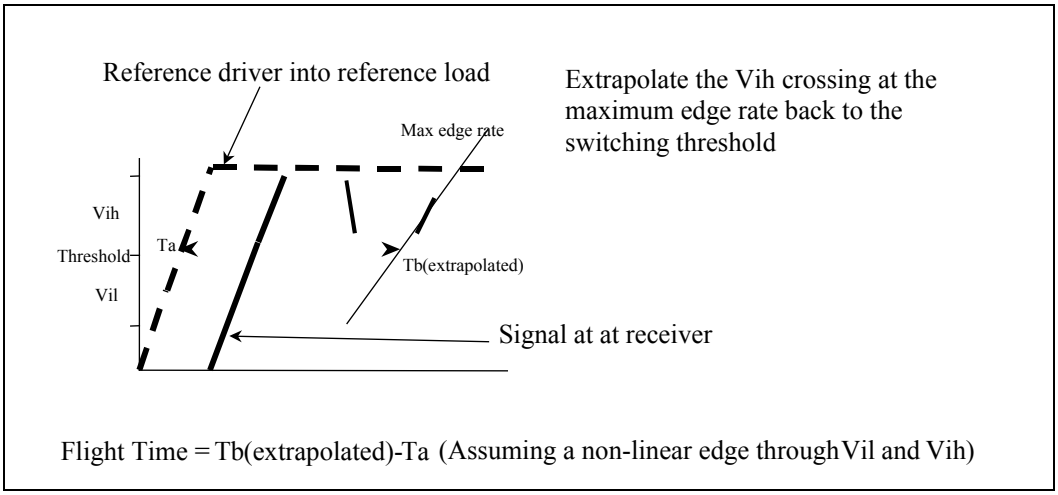
The following figure shows a traditional method of calculating flight time assuming a nonlinear edge from VIL Through VIH at the receiver.

Figure 177. Calculating Flight Time (Nonlinear Edge from V_{IL} through V_{IH} at the Receiver)



The following figure shows a traditional method of calculating flight time assuming a ringback violation from V_{IL} through V_{IH} at the receiver.

Figure 178. Calculating Flight Time (Ringback Violation from V_{IL} through V_{IH} at the Receiver)



14.2.5.3 Incorporating Package Effects into the Flight Time

Flight time should be simulated beginning and ending at the pad of the silicon, not at the package pin. This allows the skew due to the package trace length differences to be accounted for. Additionally, the traces on the motherboard should be skewed appropriately to cancel any skews built into the package.

14.2.6 Parameter Sweeps and Monte Carlo Analysis

This part of the sensitivity analysis constitutes the bulk of the pre-route design. In this section of the design phase, all system variables shown in Table 62 are varied, and the solution space for the design is determined.

14.2.6.1 Parameter Sweeps

The bulk of the sensitivity analysis consists of parameter sweeps. During a parameter sweep, all parameters are held constant except for one or two. The system performance is then observed as the specific variables are being swept. Surface plots can be generated from the results of the parameter sweep. Then the timing and signal quality specifications can be superimposed onto the surface and design limits (e.g., line length, buffer strength, line impedance, etc.) can be determined. Figure 179 shows an example of surface plots based on simulated flight times and undershoot. The upper and lower left surface plots show flight time as a function of line lengths L2 and L3. Additional planes are incorporated into the plots that represent the upper and lower flight time specifications. The upper right plot depicts a signal quality metric as a function of L2 and L3 line length. The surfaces of all three of these plots are intersected with the specifications and the resultant solution space for these variables under the conditions of the simulation is shown in the lower right hand side of Figure 179.

It should be noted that the sweeps should be performed using different switching speeds to capture the majority of ISI noise. If *N* is the fastest switching speed for a given bus, then simulations should be performed at a frequency of *N*, *½N*, and *¼N*. The difference between the timings at the different switching frequencies is a good approximation of the ISI noise. Final checks on fully coupled models with long worst-case bit patterns should be performed in order to find any ISI effects not captured in this analysis. This sweeping technique can be used extensively to get initial bounds on all variables in the system. The resultant solution space will be known as the "Phase 1 solution space."

The drawback of this method is that the sweeps are only good for evaluating two variables at a time. While the two parameters of interest are being varied, the other parameters in the system are held constant at a value that may not yield worst-case performance. For example, if the line lengths are being swept, all line and buffer impedances, package parasitics, receiver capacitance, etc., are held at fixed values. Every effort should be made to set these parameters so that the performance will approach worst case. Use Intel's recommendations as a baseline, and work from there to refine corner conditions specific to your environment. In order to ensure that the worst-case performance is captured, all system variables must be varied simultaneously. This can be accomplished using a targeted Monte Carlo analysis.

14.2.6.1.1 Targeted Monte Carlo Analysis

Targeted Monte Carlo (TMC) analysis can be used to further refine the phase 1 solution space and ensure that the worst-case performance has been captured. Performing a full Monte Carlo analysis over all system variables is inefficient because a large number of simulations must be performed to statistically guarantee that all worst-case conditions are captured. If a TMC analysis is performed on the boundaries of the phase 1 solution space determined by the parametric sweeps, the number of simulations required will decrease dramatically and the solution space can be refined by changing the variables that were held constant during the sweep.

Figure 180 shows the area where the TMC analysis was performed to refine the phase 1 solution space illustrated in Figure 179. Figure 181 shows the results of the TMC analysis and shows the final solution space. This final solution space will be referred to as the "Phase 2 solution space." It should be noted that the worst-case bit pattern should be included in the TMC analysis.

Figure 179. Example of Sweeps Used to Evaluate the Length Limits of Trace L2 and L3

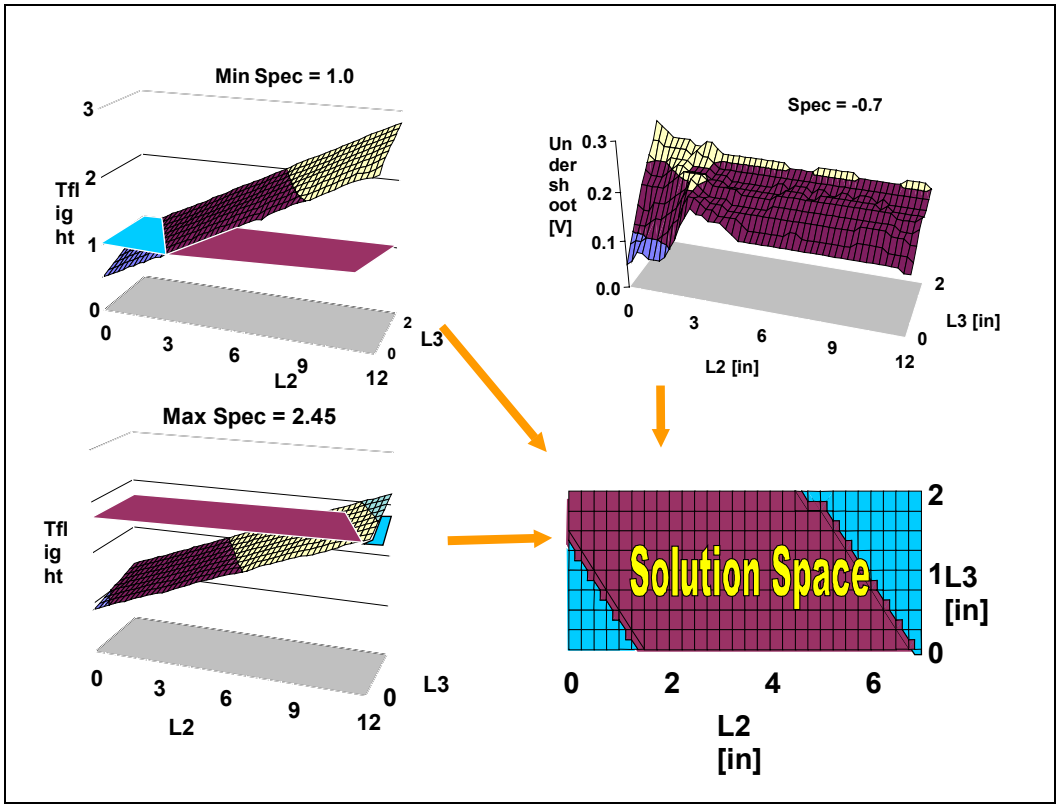
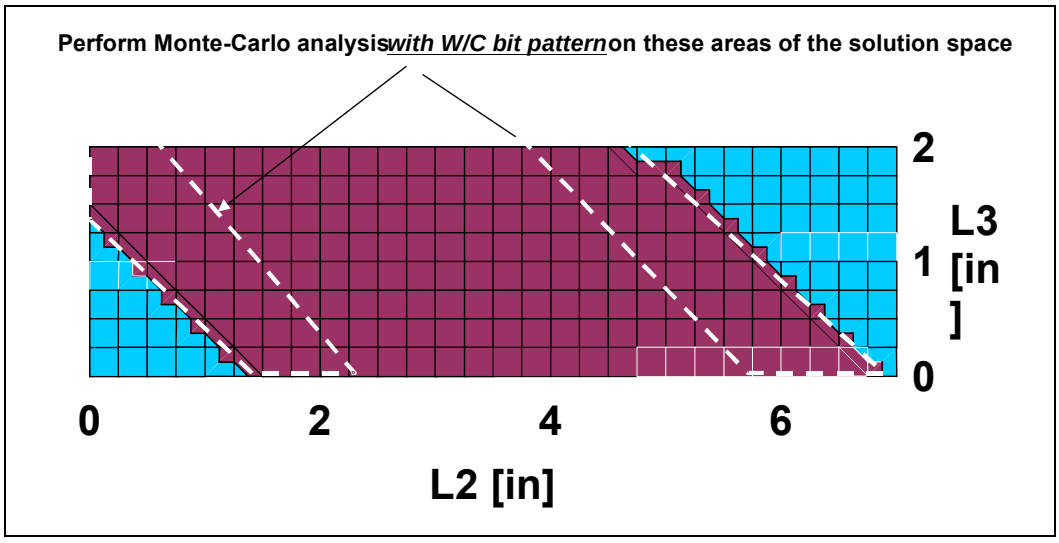
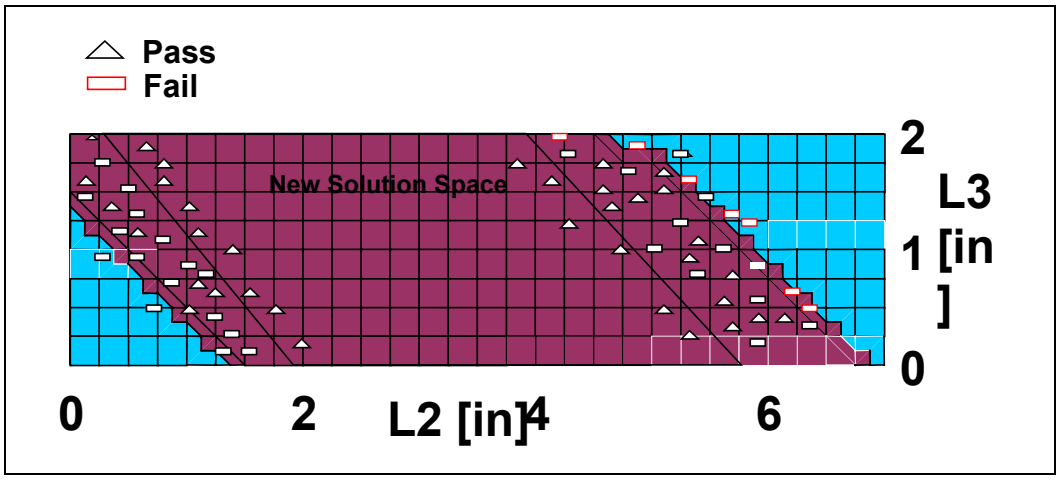


Figure 180. Monte Carlo Analysis



The following figure shows the results of targeted Monte Carlo (TMC) analysis and the resultant phase 2 solution space for variables L2 and L3

Figure 181. Targeted Monte Carlo (TMC) Analysis (Phase 2 Solution Space for Variables L2 and L3)



14.2.6.2 Final Solution Space

The final solution space will be referred to as t‘e 'phase 3 solution spa’e.' This phase incorporates effects that are too computationally demanding to easily include in the phase 1 or phase 2 solution spaces. A final check on the worst-case nets under fast and slow conditions should be performed. The sweeps and the Monte Carlo analysis already performed should allow the worst-case conditions to easily be chosen. These simulations should be performed using a fully coupled crosstalk model. The results of the final check should be used to further narrow the solution space.

The routing guidelines should incorporate the entire solution space determined during the sensitivity analysis in order to provide the maximum amount of flexibility. When some portions of the routing guidelines cannot be met because of physical real estate limitations or manufacturing concerns, new solutions must be determined.

15 System Theory

This section provides in-depth information about signal technology and system signal interference.

15.1 AGTL+

AGTL+ is the electrical system bus technology. It is an incident wave switching, open-drain bus with integrated pull-up resistors (p-channel FETs) that provide both the high logic level and the termination.

The end agents on the system bus will always have their termination on. Middle agents' pull-ups will turn on only when needed to drive a signal to its high state. The ODTEN pin on the Intel Xeon processor will be used to determine whether a processor is an end agent and thus needs to enable its termination. It is up to the baseboard designer to pull this pin to the appropriate logic level (high to enable).

15.2 Inter-Symbol Interference

Inter-symbol interference (ISI) is the effect of a previous signal (or transition) on the interconnect delay. When a signal is transmitted down a transmission line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI can impact both the timing and the signal integrity. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. Thus, ISI is a major concern in any high-speed design where the period is smaller than the delay of the transmission line. Figure 182 shows an example of how ISI can affect timing. In this example the starting voltage of the driver is different from the idle state starting voltage. This figure illustrates the ISI effect on both timing and signal integrity.

One method of capturing most of the timing impact due to ISI is to perform parameter sweeps at the fastest bus period, and then at 2x and 3x multiples of the fastest bus period. For example, if the fastest frequency at which the bus will operate is 400 MHz, then the pulse duration of a single bit is 2.5 ns (5 ns period). The data pattern should be repeated with pulse durations of 5 ns and 7.5 ns (10 ns and 15 ns periods). This represents the following data patterns transitioning at the highest bus rate.

- 01010101010101
- 00110011001100
- 00011100011100

The worst-case results of these patterns can be used to produce the phase 1 solution space. The maximum difference in flight time between these patterns produces a first order approximation of the ISI impact.

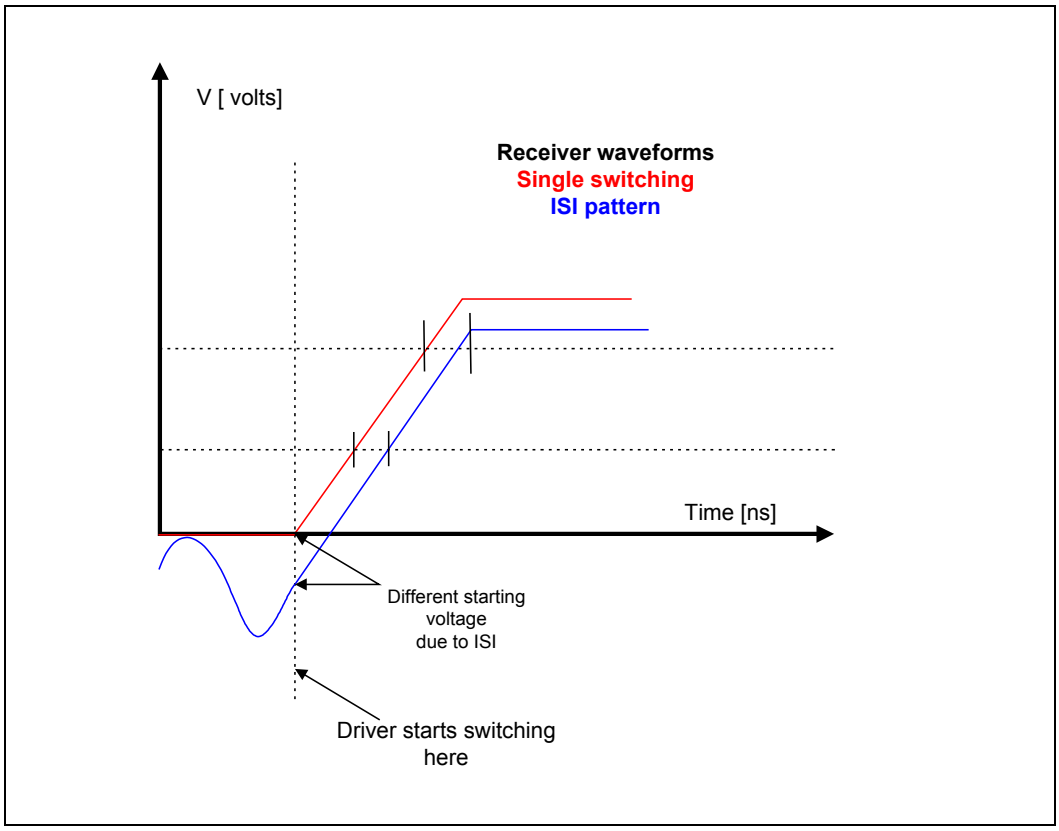
The final solution space must account for the full ISI variations. This can be done by performing targeted simulations at the edges of the phase 2 solution space using a long pseudo-random pulse

train. If the timing impact due to ISI does not violate any timing or signal integrity specifications, then the phase 2 solution space is acceptable. If timing violations do occur then steps should be taken to minimize reflections on the bus, which will reduce the ISI. Typically, the best way to limit reflections is to reduce impedance variations and minimize discontinuities (e.g., by shortening stubs and connectors, matching impedance between packages and motherboard traces, etc.).

The worst-case ISI can be evaluated using the following procedure:

- Simulate the longest net on the bus using a long pseudo-random bit pattern for both the fast and slow cases.
- Take the first transition of the ISI simulation as the baseline.
- Determine the rising and falling delays for each bus transition.
- Subtract the minimum and maximum delays from the baseline delays, and find the worst-case difference.
- Take the smallest negative and the greatest positive difference. This should be the worst-case ISI impact on timing.

Figure 182. Example of ISI Impact on Timing and Signal Integrity



15.3 Crosstalk

Crosstalk is caused through capacitive and inductive coupling between networks. Crosstalk can be backward or forward. Backward crosstalk creates an induced signal on a victim network that travels in a direction opposite that of the aggres'or's signal. Forward crosstalk creates a signal that travels in the same direction as the aggres'or's signal. On an AGTL+ bus a driver on the aggressor network is not necessarily at the end of the network. Therefore, it sends signals in both directions on the aggres'or's network. The signal propagating in each direction causes crosstalk on the victim network. This effect is illustrated in Figure 183, which shows a driver on the aggressor network and a receiver on the victim network. Figure 184 shows two aggressors on each side of the victim. Additional aggressors are possible in the z-direction if adjacent signal layers are not routed in mutually perpendicular directions. Because coupling coefficients decrease rapidly with increasing separation, it is rarely necessary to consider aggressors that are at least five line widths separated from the victim. Additionally, there is crosstalk internal to the IC packages, which can also affect the signal quality.

Figure 183. Propagation on Aggressor Network

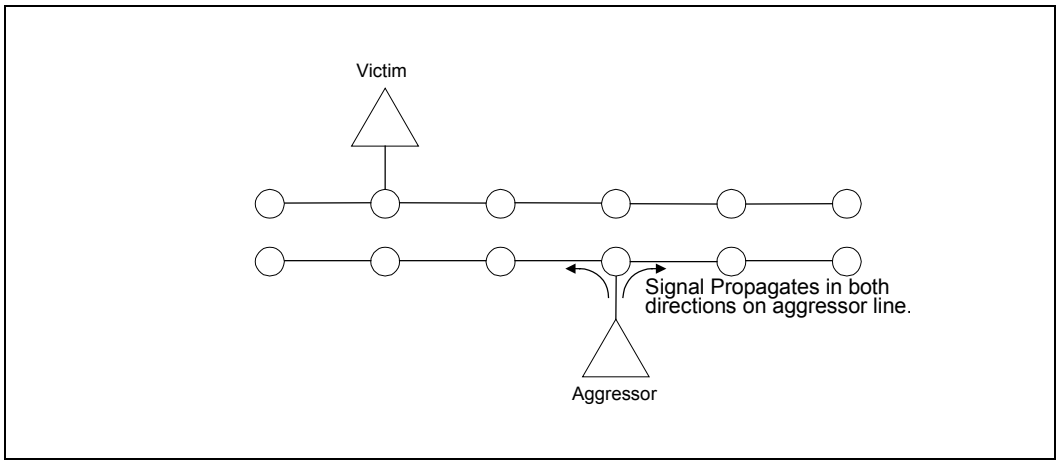


Figure 184. Aggressor and Victim Networks

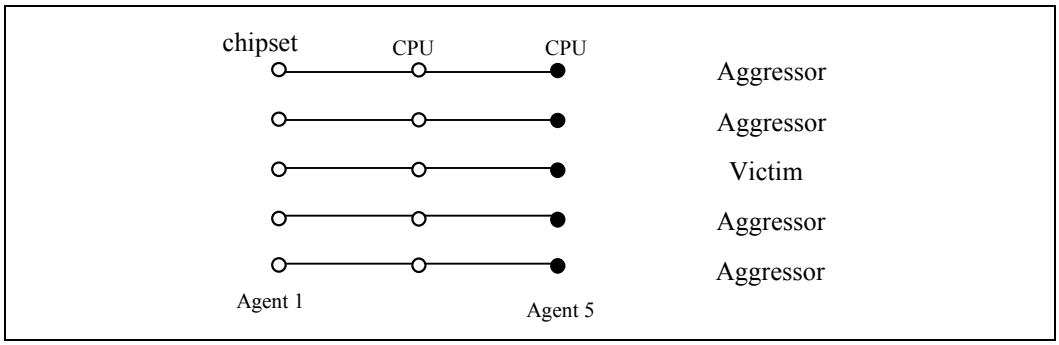
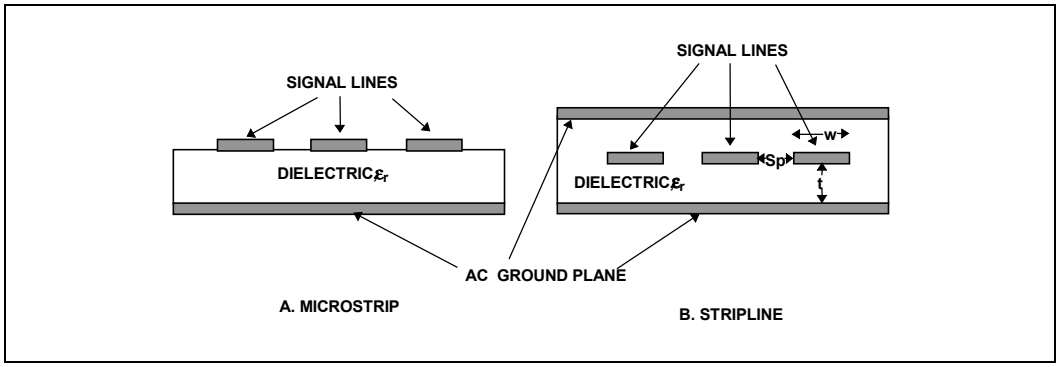


Figure 185. Transmission Line Geometry of Microstrip and Stripline



Backward crosstalk is present in both stripline and microstrip geometry. The backward-coupled amplitude is proportional to the backward crosstalk coefficient, the aggres'or's signal amplitude, and the coupled length of the network. Backward crosstalk reaches a maximum (and remains constant) when the propagation time on the coupled network length exceeds one half of the rise time of the aggres'or's signal. Assuming the ideal ramp on the aggressor from 0% to 100% voltage swing and the rise time on an unloaded coupled network, then the following equation applies.

Equation 30. Length for Maximum Backward Crosstalk

$$Length\ for\ Max\ Backward\ Crosstalk = \frac{½ \times Rise\ Time}{Board\ Delay\ Per\ Unit\ Length}$$

An example calculation if fast corner fall time is 1.5 V/ns and board delay is 175 ps/inch (2.1 ns/foot) follows:

Fall time = 1.5 V/1.5 V/ns = 1 ns

Length of maximum backward crosstalk
= ½ * 1 ns * 1000 ps/ns /175 ps/in = 2.86 inches

Agents on the AGTL+ bus drive signals in each direction on the network. This will cause backward crosstalk from segments on two sides of a driver. The pulses from the backward crosstalk travel toward each other and will meet and *add* at certain moments and positions on the bus. This can cause the voltage (noise) from crosstalk to double. Table 63 provides example coupling factors for various stripline space to width to dielectric thickness ratios (see Figure 185) with dielectric constant $\varepsilon_r = 4.5$, $V_{OH\_MAX} = 1.5$ V, and $Z0 = 65\ \Omega$. Note that the fast edge rates of falling edges place limits on the maximum coupled length allowed. Also, it should be noted that multiple parallel coupled lines increase the impact on the noise budget.

Forward crosstalk is absent in stripline topologies, but present in microstrip. This is for the ideal case with a *uniform* dielectric constant. In actual boards, forward crosstalk is *nearly* absent in stripline topologies, but *abundant* in microstrip. The forward coupled amplitude is proportional to the forward crosstalk coefficient, the aggressor's signal edge rate (*dv/dt*), and the coupled network's electrical length. The forward crosstalk coefficient is also a function of the geometry. Unlike backward crosstalk, forward crosstalk can grow with coupled section length, and may transition in a direction similar to or opposite to that of the aggressor's edge. Unlike backward

crosstalk, forward crosstalk on the victim signal will continue to grow as it passes through more coupled length before the aggressor's wave front is absorbed by the termination.

To minimize crosstalk:

- Route adjacent trace layers in different directions (orthogonal preferred) to minimize the forward and backward crosstalk that can occur from parallel traces on adjacent layers. This reduces the source of crosstalk.
- Maximize the spacing between traces. Where traces have to be close and parallel to each other, minimize the distance that they are close together, and maximize the distance between sections that have close spacing. Routing close together could occur where multiple signals have to route between a pair of pins. When this happens, the signals should be spread apart where possible. Also note that routing multiple layers in the same direction between reference planes can result in parallel traces that are close enough to each other to have significant crosstalk.
- Minimize the variation in board impedance (Z_0). For the example topologies covered in this guideline, 60 Ω ±15% and 52.5 Ω ±10% were assumed for uni-processor and dual-processor based designs respectively.
- Minimize the nominal board impedance within the AGTL+ specification while maintaining the same trace width/spacing ratio. For a given dielectric constant, this reduces the trace width/trace height ratio, which reduces the backward and forward crosstalk coefficients. Having reduced crosstalk coefficients reduces the magnitude of the crosstalk.
- Minimize the dielectric constant used in the PCB fabrication. As above, all else being equal, this puts the traces closer to their reference planes and reduces the magnitude of the crosstalk.
- Watch out for voltage doubling at a receiving agent, caused by the adding of the backward crosstalk on either side of a driver. Minimize the total network length of signals that have coupled sections. If there has to be closely spaced/coupled lines, place them near the center of the net. This will cause the point in time that voltage doubling occurs to be before the setup window.
- Route synchronous signals that could be driven by different components in separate groups to minimize crosstalk between these groups. The Intel Xeon processor uses a split transaction bus with five independent sub buses (arbitration, request, snoop, response, and data). This implies that in a given clock cycle, each sub bus could be driven by a different agent. If these two agents are at the opposite process corner (one fast and one slow), then separating the bus types will reduce the impact of crosstalk.

Table 63. Example Backward Crosstalk Coupling Factors with ε_r = 4.5, V_{OH_MAX} = 1.5 V, and Z_0 = 65 Ω

Space: Width:Thickness	Coupling Factor	Maximum Crosstalk
24:4:8	0.65%	9.8 mV
20:4:8	1.3%	19.5 mV
16:4:8	1.75%	26.2 mV
14:4:8	2.5%	37.5 mV
12:4:8	3.4%	51.0 mV
8:4:8	6.55%	98.2 mV
4:4:8	13.5%	202.5 mV

16 Debug Port Routing Guidelines

Please refer to the latest version of the *ITP700 Debug Port Design Guide* for details on the implementation of the Debug Port. This document is available at http://developer.intel.com.

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17 Schematic Checklist

17.1 Intel® Xeon™ Processor and Intel Xeon Processor with 512 KB L2 Cache Checklist

Checklist Items	Recommendations	Reason/Impact/Documentation
A20M#	• Recommend 300 Ω ± 5% pull-up to VCC_CPU.	• Sampling the value of this signal along with IGNNE#, and LINT[1:0] determines the ratio of the core clock frequency to bus clock frequency. • Async GTL+ Input Signal • Refer to Section 5.4.2.2.
A[35:3]#	• Signal must be connected to the appropriate pins on all processor system bus agents. Balance signal lengths within strobe group.	• Refer to Section 5.4.1.2. • AGTL+ Source Synchronous I/O
ADS#	• Connect to the appropriate pins on all processor system bus agents.	• Asserted to indicate the validity of the transaction address on the A[35:3]# pins. • AGTL+ Common Clock I/O • Refer to Table 13.
ADSTB[1:0]#	• Connect to all system bus agents. Balance signal lengths within strobe group. Refer to the length balancing spreadsheet in the Intel® Xeon™ Processor Signal Integrity Models.	• Address strobes used to latch A[35:3}# on rising and falling edge. • AGTL+ Strobes • Refer to Section 5.4.1.2.
AP[1:0]#	• Connect to all system bus agents.	• Refer to Section 5.4 and Table 13.
BCLK[1:0]	• Connect to CK_SKS clock driver. BCLK's to all processors should be length matched, and the BCLK to the MCH should be offset accordingly.	• All processor system bus agents must receive these signals to drive their outputs and latch their inputs. • Refer to Section 5.4.1 and Table 13.
BINIT#	• Wired-OR signal: Route as common clock signal. No AC termination is required because the signal is driven only by the processor.	• AGTL+ Common Clock I/O • Refer to Section 5.4.1.4 and Table 13.
BNR#	• Connect to all system bus agents. Wired-OR signal: • For DP design, route as common clock signal. • Must be terminated to VCC_CPU using a 40.2Ω resistor and series 47 pF cap.	• Used to assert a bus stall by any bus agent who is unable to accept new bus transactions. • AGTL+ Common Clock I/O • Refer to Section 5.4.1.4 and Table 13.

Checklist Items	Recommendations	Reason/Impact/Documentation
BPM[5:0]#	• Recommend 41 Ω ± 5% pull-up to VCC_CPU.	• Indicates status of breakpoints and programmable counters used for monitoring processor performance. • AGTL+ Common Clock I/O • Refer to the *ITP700 Debug Port Design Guide*
BPRI#	• Connect to all system bus agents.	• Used to arbitrate for ownership of the processor system bus. • AGTL+ Common Clock Input • Refer to Section 5.4 and Table 13.
BR[3:0]#	• Either terminate BR[3:2]# individually at each processor, or connect the signals between processors and terminate at one end using 40.2 Ω resistors. Terminate to VCC_CPU.	• Refer to Section 5.4.2.5 and Table 64.
COMP[1:0]	• Recommend 43.2 Ω ± 1% pull-down to GND for each COMP pin. Place as close as possible to the pin.	• Refer to Section 5.4.2.6.
D[63:0]#	• Connect to all system bus agents. Balance signal lengths within strobe group. Refer to the length balancing spreadsheet in the processor signal Integrity models.	• AGTL+ Source Synchronous I/O • Refer to Section 5.4.1.1, Table 13 and Table 14.
DBI[3:0]#	• Connect to all system bus agents. Balance signal lengths within strobe group. Refer to the length balancing spreadsheet in the processor signal integrity models.	• Source synchronous indicating the polarity of the D[63:0]# signals. • AGTL+ Source Synchronous I/O • Refer to Section 5.4.1.1.
DBSY#	• Connect to all system bus agents.	• Asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. • AGTL+ Common Clock I/O • Refer to Section 5.4.
DEFER#	• Connect to all system bus agents.	• Asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. • AGTL+ Common Clock Input • Refer to Section 5.4.
DP[3:0]#	• Connect to all system bus agents.	• AGTL+ Common Clock I/O • Refer to Section 5.4.
DRDY#	• Connect to all system bus agents.	• AGTL+ Common Clock I/O • Refer to Section 5.4.

Checklist Items	Recommendations	Reason/Impact/Documentation
DSTBN[3:0]#	• Connect to all system bus agents • Balance signal lengths within strobe group. Refer to the length balancing spreadsheet in the processor signal integrity models. Maintain a 25 mil spacing from other signals	• AGTL+ Strobes • Refer to Section 5.4.1.1.
DSTBP[3:0]#	• Connect to all system bus agents. • Balance signal lengths within strobe group. Refer to the length balancing spreadsheet in the processor signal integrity models.	• AGTL+ Strobes • Refer to Section 5.4.1.1.
FERR#	• Connect to ICH2. Pull-up at both ends of the signal with 56 Ω resistors.	• CMOS output • Refer to Section 5.4.2.1.
HIT#	• Connect to all system bus agents. Wired-OR signal: • For DP design, route as common clock signal. • Must be terminated to VCC_CPU using a 40.2Ω resistor and series 47 pF cap.	• AGTL+ Common Clock I/O • Refer to Section 5.4.1.4.
HITM#	• Connect to all system bus agents. Wired-OR signal: • For DP design, route as common clock signal. • Must be terminated to VCC_CPU using a 40.2Ω resistor and series 47 pF cap.	• Convey transaction snoop operation results. • AGTL+ Common Clock I/O • Refer to Section 5.4.1.4.
HLOCK# (LOCK#)	• Connect to all system bus agents.	• AGTL+ Common Clock I/O • Refer to Section 5.4.
IERR#	• If supported, connect to all system bus agents and terminate at both ends with 56 Ω pull-up. If not supported, leave as no-connect.	• AGTL+ Common Clock Output • Refer to Section 5.4.
IGNNE#	• Recommend 300 Ω ± 5% pull-up to VCC_CPU.	• Refer to Section 5.4.2.2.
INIT#	• Recommend 300 Ω ± 5% pull-up to VCC_CPU.	• Refer to Section 5.4.2.2.
LINT[1:0]	• Recommend 300 Ω ± 5% pull-up to VCC_CPU.	• Refer to Section 5.4.2.2.
MCERR#	• Wired-OR signal: Route as common clock signal. No AC termination is required because the signal is driven only by the processor. • MCERR# must be connected to BERR# on the MCH.	• Asserted to indicate an unrecoverable error without a bus protocol violation. • AGTL+ Common Clock I/O • Refer to Section 5.4.1.4.

Checklist Items	Recommendations	Reason/Impact/Documentation
ODTEN	• Option 1 (preferred): Enable ODT (on-die termination) on Processor 0 (end processor) by pulling up to VCC_CPU with a resistor that falls within the range of 50 Ω ± 20%. Disable ODT for Processor 1 by pulling down to VSS with a resistor that that falls in the range of 50 Ω ± 20%. • Option 2: Enable ODT on Processor 0 (end processor) by pulling up to VCC_CPU with a 1 kΩ resistor. Disable ODT for Processor 1 by pulling down to VSS with a 1 kΩ resistor.	• Refer to Section 5.4.2.7.
PROCHOT#	• Recommend 56 Ω ± 5% pull-up to VCC_CPU • Connect to ICH2 GPIO or external logic.	• Refer to Section 5.4.2.1.
PWRGOOD	• Recommend 300 Ω ± 5% pull-up to VCC_CPU	• Refer to Section 5.4.2.2.
REQ[4:0]#	• Connect to all system bus agents • AGTL+ Source Synchronous I/O: 2X Group	• Refer to Section 5.4.1.2.
Reserved	• Reserved signals must remain as a No Connect (NC)	
RESET#	• Recommend 41 Ω ± 5% pull-up to VCC_CPU. Connect to MCH.	• AGTL+ Common Clock Input • Refer to Section 5.4.
RS[2:0]#	• Connect to all system bus agents.	• AGTL+ Common Clock Input • Refer to Section 5.4.
RSP#	• Connect to all system bus agents.	• AGTL+ Common Clock Input • Refer to Section 5.4.
SKTOCC#	• Connect to glue logic if pin is used. Refer to Section 5.4.2.9.	• Output of this signal indicates whether a processor is installed or not.
SLP#	• Recommend 300 Ω ± 5% pull-up to VCC_CPU.	• Refer to Section 5.4.2.2.
SM_ALERT#	• Should be connected to an SMBUS controller in adherence to the SMBus Specification	• Refer to Section 5.4.2.4.
SM_CLK	• Recommend a pull-up resistor to SM_VCC. Resistor value is based on the number of devices on the SMBus.	• Refer to Section 5.4.2.4.

Checklist Items	Recommendations	Reason/Impact/Documentation
SM_DAT	• Recommend a pull-up resistor to SM_VCC. Resistor value is based on the number of devices on the SMBus.	• Refer to Section 5.4.2.4.
SM_EP_A[2:0]	• Leave as no connect or recommend <1 kΩ ± 5% pull-up to SM_VCC.	• Sets the SMBus address for the memory device on the processor. These signals must be set at power up with unique address per bus. • Refer to Section 5.4.2.4.
SM_TS_A[1:0]	• Recommend 1 kΩ ± 5% pulled down to VSS or SM_VCC with 1 kΩ ± 5% or smaller.	• Leaving the pins floating achieves a high impedance state. • Refer to Section 5.4.2.4.
SM_WP	• Pull to SM_VCC.	• Pulling this signal to SM_VCC will enable write protection. • Refer to Section 5.4.2.4.
SMI#	• Recommend 300 Ω ± 5% pull-up to VCC_CPU.	• Asserted asynchronously by system logic. • Refer to Section 5.4.2.2.
STPCLK#	• Recommend 300 Ω ± 5% pull-up to VCC_CPU.	• Causes processors to enter a low power Stop-Grant state. • Refer to Section 5.4.2.2.

Checklist Items	Recommendations	Reason/Impact/Documentation
TESTHI[6:0]	• Option 1a (preferred): All TESTHI[6:0] pins may be individually pulled-up to VCC_CPU with resistors that fall within the range of 50 Ω ± 20%. • Option 1b: All TESTHI[6:0] pins may be individually pulled-up to VCC_CPU with 1 kΩ ± 5% resistors. **or,** • Option 2a (preferred): TESTHI[3:0] and TESTHI[6:5] may all be tied together and pulled up to VCC_CPU with a single resistor that falls within the range of 50 Ω ± 20%. However, utilization of boundary scan test will not be functional if these pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins. • Options 2b: TESTHI[3:0] and TESTHI[6:5] may all be tied together and pulled up to VCC_CPU with a single 1 kΩ–4.7 kΩ resistor if desired. However, utilization of boundary scan test will not be functional if these pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins.	• For proper operation, note the following: • Range: 50 Ω ± 20% and 1 kΩ–10 kΩ • Refer to Section 5.4.2.8. • Refer to the *Intel® Xeon™ Processor at 1.40 GHz, 1.50 GHz, 1.7 GHz and 2 GHz Datasheet* for TESTHI[6:0] specification details.
THERMTRIP#	• Recommend 56 Ω ± 5% pull-up to VCC_CPU • Connect to motherboard logic that will remove processor power within 0.5 seconds of a THERMTRIP# assertion.	• Asynchronous GTL+ Output Signal • Refer to Section 5.4.2.1.
TRDY#	• Connect to MCH • All bus agents must connect to this signal.	• AGTL+ Common Clock Input • All bus agents must connect to this signal. • Refer to Section 5.4.
VCCA	• Use discrete RLC filter to provide clean power	• An isolated power for internal PLL • Refer to Section 12.17.3.
VCCIOPLL	• Use discrete RLC filter to provide clean power	• An isolated power for internal PLL • Refer to Section 12.17.3.
VCCSENSE	• Place via next to the processor pad for measurement of VCC_CPU.	• Isolated low impedance connection to processor core VSS. • Refer to Section 12.12.

Checklist Items	Recommendations	Reason/Impact/Documentation
VID[4:0]	• Should be routed to the voltage regulator. Refer to VRM 9.0 DC-DC Converter Design Guidelines • Compare VID's from both processors with logic and disable VR/VRM if they are not equal.	• Refer to Section 5.4.2.3.
VSSA	• Use discrete RLC filter to provide clean ground.	• Isolated ground for internal PLL's • Refer to Section 12.17.3.
VSSSENSE	• Place via next to the processor pad for measurement of VCC_CPU/VSS	• An isolated low impedance connection to processor core VSS • Refer to Section 12.12.

Table 64. BR0# (I/O) and BR1# Signals Rotating Interconnect

Bus Signal	Processor 0 Pins	Processor 1 Pins
BREQ0#	BR0#	BR1#
BREQ1#	BR1#	BR0#

17.2 CKx_SKS(DP)/Direct Rambus* Clock Generator Checklist

NOTES:

1. Processor Clock output blocks should utilize the same series termination resistor value on all signal lines (CPUCLK0, CPUCLK1, CPUCLK2, CPUCLK3).
2. Different Clock output blocks can utilize different series termination resistor values (CPUCLK [0:3] can differ from 3 V66[0:3]).
3. If Rpacks are used for series termination, then each resistor pack should only carry clock signals of the same frequency. Recommend simulation. Also note that with Rpacks, the clock signals cannot be easily adjusted by altering their series termination resistor.
4. Unused clock outputs require pull-down resistors to eliminate EMI radiation. CPU, CPU_Div2 and IOAPIC are required to be pulled-down with 30 Ω resistors. 48 MHz and REF are required to be pulled-down with 40 Ω resistors. PCI, 3 V33, and 3 V66 are required to be pulled-down with 33 Ω resistors.

Checklist Items	Recommendations	Reason/Impact/Documentation
Frequency Combinations:	• The following combinations are supported by the MCH: FSB Frequency / Direct RDRAM* Device Frequency 100 MHz / 300 MHz[1] 100 MHz / 400 MHz [1]RIMM modules down only	
REF/MultSel [0:1]	• Use 20 Ω or 33 Ω series termination resistor. Connect to ICH2 and SIO.	• MultSel0 and MultSel1 inputs are sensed on power up and then internally latched prior to the pin being used for output of 3 V 14.318 MHz clocks. • Refer to the CK00 Clock Synthesizer/Driver Design Guide (OR-1979).
PCICLK[0:9]	• Use 33 Ω series termination resistor for each signal. • Connect to PCI slots 0 through 4 • Connect to ICH2, FWH Flash BIOS, SIO, and AUDIO logic device	• Refer to the schematics in Appendix A.
3 V66[0:3]	• 20 Ω to 33 Ω series termination resistor. • Recommend tying the MCH and AGP clock signals together at the CK133WW output to eliminate pin to pin skew. Connect to ICH2.	• Tying the clocks together is only a recommendation. The OEM may want to simulate a design that does not tie these pins together. • Refer to the CK00 Clock Synthesizer/Driver Design Guide (OR-1979).
3 VMref 3 Vmref_b	• Use 33 Ω series termination resistor for each signal. Connect 3 VMref to DRCG1. Connect 3 VMref_b to DRCG2	• 3 VMref_b is 180° out of phase with 3 VMref. • Refer to the schematics in Appendix A.

Checklist Items	Recommendations	Reason/Impact/Documentation
vSEL133/100#	• Connect this signal to 10 kΩ ± 5% resistor to GND.	• Refer to the CK00 Clock Synthesizer/Driver Design Guide (OR-1979).
48 MHz/SelA 48 MHz/SelB	• Add a 10 kΩ ± 5% series termination resistor to GND. Connect to ICH2.	• Sensed on power-up and then internally latched prior to the pin being used for output of 3 V 48 MHz clocks.
SPREAD#	• If SSC is DISABLED: Use 4.7 kΩ–10 kΩ pull-up resistors to VCC3.3	• Invokes Spread Spectrum functionality on the Differential Host Clocks
PWRDWN#	• Pull-up to 3.3 V through a 10 kΩ resistor	• Invokes powerdown mode • Refer to the CK00 Clock Synthesizer/Driver Design Guide (OR-1979).
3.3 V(VCC)	• Connect to 3.3 V power plane	• Refer to the schematics in Appendix A.
GND	• Connect to GND plane.	• Refer to the schematics in Appendix A.
XTAL_in XTAL_out	• Connect a 10 pF cap from each signal to GND. Connect to 14.318 MHz crystal oscillator.	• Capacitor values may vary slightly from manufacturer to manufacturer. • Refer to the schematics in Appendix A.
VddIR	• Connect to 3.3 V	• Provides the voltage reference for the Refclk clock output from CK_SKS clock generator • Refer to the schematics in Appendix A.
Refclk	• Connect Refclk pin of DRCG1 and DRCG2 to 3 VMREF and 3 VMREF_B outputs from the CK_SKS clock generator.	• Refer to the schematics in Appendix A.
VddP, VddC, VddO,	• These are all 3.3 V voltage pins. Tie directly to VCC3.3 supply. Place a 0.1 µF cap between each pin and the VSS plane.	• Refer to the schematics in Appendix A.
GndP, GndI, GndC, GndO	• Connect to GND.	• These are all Ground pins. • Refer to the schematics in Appendix A.
PCLKM	• Connect to HCLKOUT of MCH.	• This is a host clock feedback input. • Refer to the schematics in Appendix A.
SYNCLKN	• Connect to RCLKOUT of MCH.	• This is a Rambus* clock feedback input. • Refer to the schematics in Appendix A.

Checklist Items	Recommendations	Reason/Impact/Documentation
VddIPD	• Connect to 1.8 V power plane.	• This is a voltage reference for PCLKM and SYNCLKN signals. • Refer to the schematics in Appendix A.
STOPB#	• Terminate to 1.8 V power plane with a 4.7 kΩ resistor.	• Refer to the schematics in Appendix A.
PWRDN#	• Terminate to 3.3 V through a 4.7 kΩ resistor. Connect to CK_SKS PWRDN# signal.	• Refer to the schematics in Appendix A.
S1, S0	• Connect 1 kΩ ± 5% series resistors to S0 and S1 and connect signals together. Connect joined signals through a 4.7 kΩ ± 5% pull-up resistor to Vcc and a series resistor to a GPIO	• The GPIO allows software adjustable mode control over CLK and CLKB • Refer to the schematics in Appendix A.
Mult[1:0]	• Connect to GPIO.	• These pins determine the internal PLL divider ratio in the DRCG device. Connection to GPIO allows software adjustable PLLCLK and REFCLK multipliers. • Refer to the schematics in Appendix A.
CLKB/CLK	• Connect a 39 Ω ± 5% series resistor near the pins. Connect 51 Ω ± 5% parallel resistors after the series resistors through a 0.1 µF capacitor to ground. Connect to RIMM connector. • This signal should be terminated with 28 Ω ± 2% or 27Ω ± 1% resistors to ground through a 0.1 µF capacitor.	• This is the main clock (CTM/CTM#) for the Direct Rambus* channel. • Refer to the schematics in Appendix A.
Global Decoupling:	• It is recommended that a ferrite filter with 2 caps (10 µF and 0.1 µF) be placed near the part for both the 2.5 V and the 3.3 V planes. • Discrete caps are recommended for all the aforementioned decoupling. • Cpacks are not recommended.	• To reduce jitter and voltage supply noise for the part. Cpacks will increase the parasitic inductance of the capacitors, and may require more capacitors than specified above.

17.3 Intel® 860 Chipset MCH Checklist

Checklist Items	Recommendations	Reason/Impact
BUSPARK	• Connect to SKTOCC# signal from second processor socket through a 100 Ω resistor.	• Hardware strapping option to disable system bus parking when two CPUs are installed.
HLA_STB HLA_STB#	• Connect to ICH2 • Must NOT have pull-up, pull-down, or series resistors	• The length of each data signal must be matched within ± 0.1 of the HB_STB differential pair • Refer to Section 8.
HDVREF[3:0] HAVREF[1:0] CCVREF	• Use one dedicated voltage divider for all these signals. Decouple the voltage divider with 1 µF capacitor	• To provide constant and clean power delivery to the data, address and common clock signals of the host AGTL+ interface. • Refer to Figure 47, Section 5.5.
HLREF_A HLREF_B HLREF_C	• Connect to HUBREF of ICH2 • Depending on the buffer mode i.e., normal or enhanced mode the HUBREF voltage requirements must be set appropriately for proper operation. Normal Mode: R1 = R2 =150 Ω ±1% Hub reference voltage = ½ Vcc1.8 ±2% C1= 0.1 µF and C2 = 0.01 µF For HUBREF only Enhanced Mode: R1 =150 Ω ±1% R2 =301 Ω ±1% Hub reference voltage = 2/3 Vcc1.8 ± 2% For HLREF_A, HLREF_B, and HLREF_C only	• HLx_REF (x = A or B) is the hub interface reference voltage. It is 0.5*1.8 V=0.9V±2%. It can be generated locally, or HLx_REF divider can be used. The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. • Refer to Figure 79 through Figure 81 of Section 8.3.3 and Section 8.4.3 in this document. • Dual reference dividers (1 for the MCH and 1 for the ICH2) should be configured the same as the single reference divider.
HLSWNG_B HLSWNG_C	• Each 16-bit hub interface on MCH has a dedicated HLSWNG PIN. The reference voltage can be implemented using a simple voltage divider circuit. • R1 =150 Ω ±1% and R2 =301 Ω ± 1% • C1= 0.1 µF and C2 = 0.01 µF	• The MCH 16-bit hub interfaces use a compensation voltage to control the buffer voltage characteristics. If a multiple 16-bit hub interfaces are used, a HLSWNG divider circuit can be shared among the interfaces as long as the trace length from the divider circuit is less than 3.5 inches. • Refer to Figure 83 and Section 8.4.4.
HSWNG[1:0]	• The host compensation reference voltage can be implemented using a simple voltage divider circuit. • R1 =150 Ω ± 1% and R2 =301 Ω ± 1% • C1= 0.1 µF and C2 = 0.01µF	• The HSWNG inputs of MCH are used provide reference voltage for the compensation logic. • Refer to Section 5.5, Table 16, and Figure 47

Checklist Items	Recommendations	Reason/Impact
HLRCOMP_A	• Normal Mode: Tie the COMP pin to a 40 Ω ± 2% or 39 Ω ± 1% Pull-up to VCC1.8 (For Trace Impedance= 60 ± 10%) • Enhanced Mode: Tie the COMP pin to a 30 Ω ± 1% pull-down to VSS (For Trace Impedance= 60 ± 15%) • Tie the COMP pin to a 25 Ω ± 1% pull-down to VSS (For Trace Impedance= 50 ± 10%)	• Resistive compensation is used by the ICH2 and MCH to adjust the buffer characteristics to specific board characteristic. Same compensation must be used on both ICH2 and MCH side. • Refer to Table 33 and Section 8.3.4.
HLRCOMP_B HLRCOMP_C	• Enhanced Mode: Tie the COMP pin to a 30 Ω ± 1% pull-down to VSS (For Trace Impedance= 60 ± 10%) • Tie the COMP pin to a 25 Ω ± 1% pull-down to VSS (For Trace Impedance= 50Ω ±10%) • Leave HLRCOMP_C no connect if Hub Interface C is not used	• Resistive compensation is used by the P64H and MCH to adjust the buffer characteristics to specific board characteristics. Same compensation must be used on both P64H and MCH side. • Refer to Table 33 and Section 8.4.5.
HRCOMP[1:0]	• Tie the COMP pin to a 20.0 Ω ±1% pull-down resistor to ground.	• This signal is used to calibrate the Host AGTL+ I/O buffers characteristics to specific board characteristic. • Refer to Table 16 and Section 5.5.
GRCOMP	• Tie the COMP pin to a 40 Ω ± 2% or 39 Ω ± 1% pull-down resistor to ground.	• Resistive compensation is used by the AGP to adjust the buffer characteristics to specific board characteristics. • Refer to Table 33 and Section 7.1.8.
SCK/CMD Circuitry	• This implementation is applicable for RIMM modules down solution only. Also, this implementation is not necessary if Suspend-to-RAM is not supported within the system. • The transistor should have a Cobo of 4 pF or less.	• This circuitry is needed to avoid the MCH inadvertently taking the Direct RDRAM* device out of power-down due to the CMOS interface being driven during power ramp, the SCK signal should be shunted to ground when the MCH is entering and exiting Suspend-to-RAM. • Refer to Figure 64 and Section 6.3.7.
Unused 16 bit interfaces	• All data and strobe signals can be left as no connect • HLREF must be connected to the HUBREF voltage divider circuit. • HLSWNG must be connected to VCC1.8	• The MCH has integration detection logic that will detect unpopulated 16-bit interfaces without external pull-ups and pull-downs. • Refer to Section 8.4.8.
TESTIN#	• Requires 10 kΩ pull-up to VDDQ	• This pin is used for manufacturing and board level test purposes. • Refer to CRB schematics

17.4 AGP Checklist

Checklist Items	Recommendations	Reason/Impact
G_FRAME# G_IRDY# G_TRDY# G_DEVSEL# G_STOP# G_SERR# G_RBF# G_PIPE# G_REQ# G_WBF# G_PAR# G_GNT# G_PERR AD_STB[0:1] SB_STB	• These signals require pull-up resistors to Vddq. • Acceptable values are between 4 kΩ & 16 kΩ. 8.2 kΩ at 10% tolerance is the recommended value.	• The Intel® 860 Chipset MCH supports 1.5 V AGP signals only • Vddq = 1.5 V for 1X, 2X and 4X mode • Pull-up to VDDQ ensures that stable values are maintained when agents are not actively driving the bus. • Refer to Table 25 and Section 7.1.9.
AD_STB#[0:1] SB_STB#	• These signals require pull-down resistors. • Acceptable values are between 4 kΩ & 16 kΩ. 8.2 kΩ is the recommended value.	• Pull-down to GND ensures that stable values are maintained when agents are not actively driving the bus. • Refer to Table 25 and Section 7.1.9.
PME#	• Connect to PCI PME#	• This is a open drain signal and does not require pull-up resistor to VCC3.3 if connected to ICH2
INTA# INTB#	• 8.2 kΩ pull-up resistor to 3.3 V • Range is 4 kΩ–16 kΩ	• Note: These signals should be pulled up only once (for both PCI and AGP). They should be pulled to 3.3 V and MUST NOT be pulled to 5 V. • Note: INTB# is for a two function device and may not be seen with AGP down • Refer to Table 25 and Section 7.1.9.
VREFCG[B66] VREFGC[A66]	• VREFGC should be left as No Connect. • VREFCG should be tied to a V_{REF} divider network near the AGP interface to achieve the common mode power supply effect.	• Refer to Figure 70 and Section 7.1.7.

Checklist Items	Recommendations	Reason/Impact
TYPEDET# [A2]	• This signal must be no connect. The Intel 860 chipset only supports 1.5 V add-in card.	• TYPEDET# is a special AGP signal for detecting Vddq voltage level. It is either GROUNDED (1.5 V) or NO CONNECTED (3.3 V) on an AGP card. • Refer to Section 7.1.6.
3.3_Vaux1 [B24]	• Connect to 3.3 VSB	• Note: May not be seen with AGP down • Refer to schematics in Appendix A.
SBA[7:0]	• No extra pull-up resistors.	• In the MCH, weak pull-ups are integrated for SBA[7:0] signals. There is no need for external pull-ups for SBA[7:0]. • Refer to schematics in Appendix A.
Decoupling Capacitors]	• Use 0.01 µF capacitors for each power pins, bulk 10 µF tantalum capacitors on VDDQ, and 20 µF tantalum capacitors on VCC3.3 plane near the connector.	• To provide the clean power to AGP power pins. • Refer to Figure 69 and Section 7.1.4.

17.5 Intel® P64H Checklist

Checklist Items	Recommendations	Reason/Impact
P64H	Decoupled to VCC3.3 rail.	
AD[63:32] IRQ[23:0] REQ[5:0] PERR# SERR# LOCK# STOP# DEVSEL# TRDY# IRDY# FRAME# REQ64# ACK64# C/BE#[7:4] PAR64	• These pins require 8.2 kΩ pull-up resistors to VCC3.3	• See PCI 2.2 Component Specification • Pull-ups to VCC3.3 recommendations
GNT [5:0]	• These pins require 8.2 kΩ pull-up resistor to VCC3.3	• Note: Unused pins are left as no connect.
VCC5REF	• Decoupled to VCC3.3 at ball P7 & H17. • Alternative: Recommended 1K pull-up to VCC5 and a Schottky diode to VCC3.3.	• Reference voltage for IRQ. • Used for IRQs, TEST#, and BT_INT# at ball H17. • Used for RSTIN#
PVCC5REF	• Decoupled to VCC3.3 at ball F4. • Alternative: Recommended 1K pull-up to VCC5 and a Schottky diode to VCC3.3	• Reference for 5 Volt tolerance on input for PCI.
RSTIN#	• This pin should be connected to PCIRST of the ICH2. It should have a synchronizer and Schmitt trigger.	• Used to reset the P64H logic. Assists in avoiding spurious interrupts.
TEST#	• Must be pulled up to VCC3.3 (10 kΩ resistor)	• This pin is used for manufacturing testing only.
BT_INTR	• Connect directly to ICH2. Pull-up resistors are not required.	• To support boot devices on the P64H PCI segment

Checklist Items	Recommendations	Reason/Impact
PCLKOUT	• Clocks must connect through 33 Ω resistors to slots/down devices. Unused clocks should be no connects.	• These are 66 MHz clock outputs for PCI 64 slots
M66EN	• Indicates bus speed (high = 66 MHz) • Recommend 5 kΩ pull-up resistor to 3.3 V	• Referring to PCI Specification 2.2, M66EN pin is bused between all connectors within the single logical bus segment that is 66 MHz capable, and this is pulled up with a 5 kΩ resistor to VCC.
HLBRCOMP	• Requires 25 Ω ± 1% pull-down to ground • For 50 Ω enhanced mode	• The HLBRCOMP is used by the P64H to adjust the buffer characteristics to specific board characteristics. The P64H supports RCOMP method only
RSV1,3,5,7,8,9	• These pins require 8.2 kΩ pull-down resistors to GND	• These are hot plug signals need terminations.
RSV2,4,6,10, 11,12,13,14, 15	• No connect	• These are hot plug signals do not require terminations.

17.6 RIMM* Modules Down/ Intel® MRH-R Checklist

NOTES:
1. S3 (Suspend To RAM):
   - Direct RDRAM device support
   - 2.5 V (ON), 1.8 V (ON), 3.3 V (N/A)
2. S5–2.5 V (OFF), 1.8 V (OFF), 3.3 V (OFF)

Checklist Items	Recommendations	Reason/Impact/Documentation
LCTM LCTM# RCTM RCTM# LCFM LCFM# RCFM RCFM# LROW[2:0] RROW[2:0] LCOL[4:0] RCOL[4:0] RDQA[8:0] LDQA[8:0] RDQB[8:0] LDQB[8:0]	• RSL and Clocking Signal Routing Layer Capacitance (pF)(1) — Top: 0.8 — Inner 1: 0.9 — Inner 2: 1.25 — Bottom: 1.36	• The RIMM connector inductance has been shown to cause an impedance discontinuity on the Rambus* Channel. This may reduce voltage and timing margin. • Refer to Section 6.3.2.5.
RSL Signal Termination	• It is recommended that 27 Ω 1% or 28 Ω 2% tolerance resistors be used at the end of the channel opposite the MCH.	• In order to avoid reflections, proper terminations are required to match output trace impedance. Terminator Rpacks are OK • Refer to Figure 60 and Section 6.3.3.
RC Termination	• Because of the buffer strengths in the MCH, the high-speed CMOS signals require DC termination.	• The MCH tri-states SCK during STR entry causing a glitch on SCK. Terminate with 91/39 Ω ± 2% ensures proper resuming form S3. • Refer to Figure 62 and Section 6.3.5.
RESET	• For the 168-pin RIMM connector: This is a reserved pin.	• The connector pad is reserved for future use for the 168-pin RIMM connector. • Refer to the Rambus datasheets at http://www.rambus.com

Checklist Items	Recommendations	Reason/Impact/Documentation
SVDD (A56 and B56)	• Should be tied to 3.3 V for EEPROM (SPD) on RIMM connector. • If the SMBus is tied to 3.3 VSB, then either provide proper isolation on SCL /SDA and pull SVDD to 3.3 V–OR- tie SVDD to 3.3 VSB.	• Ensure proper isolation if some SMBUS devices are powered by 3.3 VSB. • Refer to the Rambus datasheets at http://www.rambus.com
SA Pins	• Should be connected to VCC3.3 or GND to set the SMBus address for that RIMM connector's EEPROM. • If the SMBus is tied to 3.3 VSB, then either provide proper isolation on SCL /SDA and pull the HIGH SA pins to 3.3 V –OR- tie the HIGH SA pins to 3.3 VSB.	• This sets the SMBus address. Each device on the SMBus must have an address to distinguish it from another device of the same type. i.e., each RIMM connector EEPROM must be strapped to a different address or they will all respond on an access. • Refer to the Rambus datasheets at http://www.rambus.com
SIN & SOUT	• Should be daisy chained between RIMM connectors: • MCH SIO pin connects to 1st RIMM connector's SIN [B36] • SOUT [A36] on 1st RIMM connector connects to 2nd RIMM connector's SIN [B36]	• Refer to the most recent version of the Design Guide for more information. • Refer to the Rambus datasheets at http://www.rambus.com
SWE (A57)	• If an OEM needs to write to the SPD devices, it is recommended that this signal be tied to a GPO pin from either the ICH2 or the SIO. • If an OEM does not have to write to the SPD devices, it is recommended that this signal be tied to 3.3 V via a weak pull-up resistor (4.7 kΩ).	• If SWE = 1: write protected. • If SWE = 0: not write protected. • These signals must be driven, do not leave floating. • Refer to the Rambus datasheets at http://www.rambus.com
VDD	• This is connected to 2.5 V (or 2.5 VSB) • It is **required** that the voltage regulator to the Direct RDRAM device (2.5 V Direct RDRAM device Core) is turned **off** in S5. This can be accomplished by connecting the SLP_S5# signal to the 2.5 V Direct RDRAM device Core voltage regulator.	• It supplies the core voltage for the Direct RDRAM device and interface logic. • Refer to the schematics in Appendix A.
VCMOS	• This is connected to 1.8 VSB for Direct RDRAM device • VCMOS can be generated by a 36/100 resistor divider from 2.5 V • VCMOS must be **off** in S5.	• S5 is a suspend state and power is removed from some components on the motherboard. Therefore, VCMOS should be off while in suspend state. • Refer to Section 6.3.5.

Checklist Items	Recommendations	Reason/Impact/Documentation
2.5 V (VDD) decoupling	• Low frequency decoupling: • This must be done on motherboard with bulk capacitors. • Linear regulator design: 8x 100 µF • Switching regulator: 5x 47 –F -OR- 6x 20 µF	• Note: These are examples. The **exact** decoupling requirements are dependent on the voltage regulator design. Refer to the Direct RDRAM device specification for the power delivery requirements. • Refer to Section 6.3.2.5.
1.8 V (Vterm) decoupling	• High frequency decoupling: • One 0.1µF ceramic cap per 2 RSL signals. These should be placed near the termination resistor pack. • Low frequency decoupling: • 2 x 100 µF tantalum caps.	• RSL termination voltage decoupling is required on motherboard. Both high and low frequency decoupling must be added on the motherboard. • Note: These are examples. The **exact** decoupling requirements are dependent on the voltage regulator design. Refer to the Direct RDRAM device specification for the power delivery requirements. • Refer to Section 6.3.2.5.
1.4V (RAMREF) decoupling	• This plane must be decoupled in the following manner: • Each RIMM connector: Locally–A value of 0.1 µF is required for local decoupling. • RAMREF Generation Circuit: At resistor divider using 75 Ω +/-2% pull-up resistor and 300 Ω +/-2% pull-down resistor to Vterm and GND respectively. A 100 Ω series resistor is required near the MCH– The RAMREF generation circuitry should be placed near the MCH. • MCH: Locally–A value of 0.1 µF is required for local decoupling.	• This will decrease the effects of voltage differences between the MEC card and baseboard. • Refer to Section 6.3.4.

17.7 I/O Controller Hub 2 (Intel® ICH2)

17.7.1 PCI Interface

Checklist Items	Recommendations	Reason/Impact/Documentation
FYI	• No inputs to the ICH2 may be left floating.	• Many GPIO signals are fixed inputs that must be pulled up to different sources. See section 17.7.7 for recommendations
PERR# SERR# PLOCK# STOP# DEVSEL# TRDY# IRDY# FRAME# REQ#[0:4] GPIO[0:1] RCIN# A20GATE# THRM#	• These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to VCC3.3 or a 2.7 kΩ pull-up resistor to VCC5.	• See PCI 2.2 Component Specification • Pull-up recommendations for VCC3.3 and VCC5.
PCIRST#	• The PCIRST# signal should be buffered to form the IDERST# signal • 33 Ω series resistor to IDE connectors.	• Improves Signal Integrity
PCIGNT#	• No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented they must be pulled up to 3.3 V	• These signals are actively driven by the ICH2
PME#	• No extra pull-up resistors	• This signal has an integrated pull-up of 24 kΩ.
SERIRQ	• External weak (8.2 kΩ) pull-up resistor to VCC3.3 is recommended.	• Open drain signal
GNT[A]# /GPIO[16], GNT[B]/ GNT[5]#/ GPIO[17]	• No extra pull-up needed	• These signals have integrated pull-ups of 24 kΩ. • GNT[A] has an added strap function of “top block swap”. The signal is sampled on the rising edge of PWROK. Default value is high or enabled due to pull-up. A Jumper to a pull-down resistor can be added to manually disable the function.

17.7.2 Hub Interface

Checklist Items	Recommendations	Reason/Impact/Documentation
HL[11]	• No pull-up resistor required	• Use a no-stuff or a test point to put the ICH2 into NAND chain mode testing
HL_COMP	• Tie the COMP pin to a 40 Ω 1% or 2% (or 39 Ω 1%) pull-up resistor (to 1.8 V) via a 10 mil wide, very short (~0.5 inch) trace.	• ZCOMP No longer supported.

17.7.3 LAN Interface

Checklist Items	Recommendations	Reason/Impact/Documentation
LAN_CLK	• Connect to LAN_CLK to Platform LAN Connect Device.	
LAN_RXD[2:0]	• Connect to LAN_CLK to Platform LAN Connect Device.	• ICH2 contains integrated 9K pull-up resistors on interface
LAN_TXD[2:0] LAN_RSTSYNC	• Connect to LAN_CLK to Platform LAN Connect Device.	
	• LAN connect interface can be left NC if not used.	• Input buffers internally terminated
	• In the event of EMI problems during emissions testing (FCC Classifications) you may have to place a decoupling cap (~470 pF) on each of the 4 LED pins.	• Reduces emissions attributed to LAN subsystem.

17.7.4 EEPROM Interface

Checklist Items	Recommendations	Reason/Impact/Documentation
EE_DOUT	• Prototype Boards should include a placeholder for a pull-down resistor on this signal line but do not populate the resistor. Connect to EE_DIN of EEPROM or CNR Connector.	• Connected to EEPROM data input signal (Input from EEPROM perspective and output from ICH2 perspective)
EE_DIN	• No extra circuitry required. Connect to EE_DOUT of EEPROM or CNR Connector.	• ICH2 contains integrated pull-up resistor for this Signal. • Connected to EEPROM data output signal (Output from EEPROM perspective and input from ICH2 perspective)

17.7.5 FWH/LPC Interface

Checklist Items	Recommendations	Reason/Impact/Documentation
FWH[3:0]/ LAD[3:0] LDRQ[1:0]	• No extra pull-ups required. Connect straight to FWH/LPC.	• ICH2 Integrates 24 kΩ pull-up resistors on these signal lines.

17.7.6 Interrupt Interface

Checklist Items	Recommendations	Reason/Impact/Documentation
PIRQ#[D:A]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3.3.	• In Non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control register. • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19. This frees the ISA interrupts.
PIRQ#[F:G]/ GPIO[4:3]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5.	• In Non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the ISA interrupts. If not needed for interrupts, these signals can be used as GPIO.
PIRQ#[H] PIRQ#[E]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3.3.	• Since PIRQ[H]# and PIRQ[E]# are used internally for LAN and USB controllers, they cannot be used as GPIO(s) pin.

Checklist Items	Recommendations	Reason/Impact/Documentation
APIC	***Pentium® 4 processor based systems:*** • These processors do not have APIC pins so all platforms using this processor should both tie APICCLK to ground and tie APICD:[1:0] to ground via a 1K-10K pull-down resistor. ***Non-Pentium® 4 processor based systems:*** *If the APIC is used:* • 150Ω pull-up resistors on APICD[1:0] • Connect APICCLK to CK133 with a 20-33Ω series termination resistor. *If the APIC is not used on UP systems:* • The APICCLK can either be tied to GND or connected to CK133, but not left floating. • Pull APICD[1:0] to GND through 10kΩ pull-down resistors.	If the APIC is not used on UP systems: • Use pull downs for each APIC signal. Do not share resistor to pull signals up.

17.7.7 GPIO

Checklist Items	Recommendations	Reason/Impact/Documentation
GPIO Pins	*GPIO[0:7]:* • These pins are in the Main Power Well. Pull-ups must use the VCC3.3 plane. • Unused **core** well inputs must be pulled up to VCC3.3. • GPIO[1:0] can be used as REQ[A:B]#. • GPIO[1] can also be used as PCI REQ[5]#. • These signals are 5 V tolerant *GPIO[8] & [11:13]:* • These pins are in the Resume Power Well. Pull-ups must use the VCCSUS3.3 plane. • Unused **resume** well inputs must be pulled up to VCCSUS3.3. • These are the only GPIs that can be used as ACPI compliant wake events. • These signals are not 5 V tolerant *GPIO[16:23]:* • Fixed as output only. Can be left NC. • In Main Power Well. • GPIO22 is open drain. *GPIO[24,25,27,28]:* • I/O pins. Can be left NC. • From resume power well.	• Ensure that **all** unconnected signals are **outputs only**! These are the only GPI signals in the resume well with associated status bits in the GPE1_STS register.

17.7.8 USB

Checklist Items	Recommendations	Reason/Impact/Documentation
USBP[3:0]P USBP[3:0]N	Refer to Figure 101.	

17.7.9 Power Management

Checklist Items	Recommendations	Reason/Impact/Documentation
THRM#	• Connect to temperature Sensor. • Pull-up if not used.	• Input to ICH2 cannot float. THRM# polarity bit defaults THRM# to active low, so pull-up.
SLP_S3# SLP_S5#	• No pull-up/down resistors needed. Signals driven by ICH2.	• Signal driven by ICH2
PWROK	• This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCC3.3 and Vcc1.8 have reached their nominal voltages	• Timing Requirement
PWRBTN#	• No extra pull-up resistors	• This signal has an integrated pull-up of 24 kΩ.
RI#	• RI# does not have an internal pull-up. Recommend an 8.2 kΩ pull-up resistor to Resume well	• If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.
RSMRST#	• This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3.3 and VccSus1.8 have reached their nominal voltages. Requires a weak pull-down. Also requires well isolation control as directed in Section 9.7.8	• Timing Requirement

17.7.10 Processor Signals

Checklist Items	Recommendations	Reason/Impact/Documentation
A20M#, CPUSLP#, IGNNE#, INIT#, INTR, NMI, SMI#, STPCLK#	• Internal circuitry has been added to the ICH2, external pull-up resistors are not needed.	• Push/pull buffers now drive the output signals.
FERR#	• Requires Weak External pull-up resistor.	• Refer to platform processor documentation for specific values.
RCIN# A20GATE	• Pull-up signals to VCC3.3 through a 10 kΩ resistor.	• Typically driven by Open Drain External Micro-controller
CPUPWRGD	• Connect to the processor PWRGOOD input. Requires weak external pull-up resistor.	• Refer to platform processor documentation for specific values.

17.7.11 System Management

Checklist Items	Recommendations	Reason/Impact/Documentation
SMBDATA SMBCLK	• Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.)	• Value of pull-ups resistors determined by line load. • Typical value used is 8.2 kΩ.
SMBALERT#/ GPIO[11]	• See GPIO section if SMBALERT# not implemented	
SMLink[1:0]	• Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.)	• Value of pull-ups resistors determined by line load. • Typical value used is 8.2 kΩ.
INTRUDER#	• Pull signal to VCCRTC(Vbat) if not needed	• Signal in VCCRTC (VBAT) well

17.7.12 RTC

Checklist Items	Recommendations	Reason/Impact/Documentation
VBIAS	• The VBIAS pin of the ICH2 is connected to a 0.047 µF cap.	• For noise immunity on VBIAS signal
RTCX1 RTCX2	• Connect a 32.768 kHz Crystal Oscillator across these pins with a 10 MΩ resistor and use 18 pF decoupling capacitors at each signal (assuming crystal with C_{LOAD} = 12.5 pF). • RTCX1 may be optionally driven by an external oscillator instead of a crystal. These signals are 1.8 V only, and must not be driven by a 3.3 V source.	• The ICH2 implements new internal oscillator circuit as compared with the PIIX4 to reduce power consumption. The external circuitry shown in Figure 107 will be required to maintain the accuracy of the RTC. • The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.
RTCRST#	• Ensure 10 ms–20 ms RC delay (8.2 kΩ and 2.2 µF). See Figure 109	
SUSCLK	• Route to Test Point if SUSCLK is unused	• To assist in RTC debug

17.7.13 AC'97

Checklist Items	Recommendations	Reason/Impact/Documentation
AC_SDOUT	• Requires a jumper to 8.2 kΩ Pull-up resistor. Should not be stuffed for default operation.	• This pin has a weak internal pull-down. To properly detect a safe_mode condition a strong pull-up will be required to over-ride this internal pull-down.
AC_SDIN[1]/ GPIO[9], AC_SDIN[0]	• Requires pads for weak 10 kΩ pull-downs. Stuff resistor for unused AC_SDIN signal or AC_SDIN signal going to the CNR connector. • If there is no codec on the system board, then both AC_SDIN[1:0] should be pulled down externally with resisters to ground.	• AC_SDIN[1:0] are inputs to an internal OR gate. If a pin is left floating, the output of the OR gate will be erroneous.
AC_BITCLK,	• No extra pull-down resistors required.	• When nothing is connected to the link, BIOS must set a shut off bit for the internal keeper resistors to be enabled. At that point, you do not need pull-ups/pull-downs on any of the link signals.
AC_SYNC	• No extra pull-down resistors required.	• Some implementations add termination for signal integrity. Platform specific.

17.7.14 Miscellaneous Signals

Checklist Items	Recommendations	Reason/Impact/Documentation
SPKR	• No extra pull-up resistors • Effective Impedance due Speaker and Codec circuitry must be greater than 50 kΩ or a means to isolate the resistive load from the signal while PWROK is low be found.	• Has integrated pull-up of between 18 kΩ and 42 kΩ. The integrated pull-up is only enabled at boot/reset for strapping functions; at all other times, the pull-up is disabled. • A low effective impedance may cause the TCO Timer Reboot function to be erroneously disabled. • Refer to Figure 125 (*SPKR Circuit*)
TP[0]	• Requires external pull-up resistor to VCCSUS3.3.	• This signal is used for BATLOW in Mobile. • Not required for Desktop.
FS[0]	• Route to a test point.	• ICH2 contains an integrated pull-up for this signal. Test point used for manufacturing appears in XOR tree.

17.7.15 Power

Checklist Items	Recommendations	Reason/Impact/Documentation
V_CPU_IO[1:0]	• The power pins should be connected to the proper power plane for the processor's CMOS Compatibility Signals. Use one 0.1 µF decoupling cap.	• Used to pull up all processor I/F signals.
VccRTC	• No clear CMOS jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safemode strapping for Clear CMOS	
Vcc3.3 V	• Requires six 0.1 µF decoupling caps	
VccSus3.3 V	• Requires one 0.1 µF decoupling cap.	
Vcc1.8 V	• Requires two 0.1 µF decoupling caps.	
VccSus1.8 V	• Requires one 0.1 µF decoupling cap.	

Checklist Items	Recommendations	Reason/Impact/Documentation
5 V_REF SUS	• Requires one 0.1 µF decoupling cap. • V5REF_SUS only affects 5 V tolerance for USB OC[3:0]# pins and can be connected to VccSUS3.3 or 5V_Always/5V_AUX if 5 V tolerance on OC[3:0]# is not required. If 5V tolerance on OC[3:0]# is needed then V5REF_SUS USB must be connected to 5V_Always/5V_AUX which remains powered during S5.	
5 V_REF	• 5VREF is the reference voltage for 5 V tolerant inputs in the ICH2. Tied to pins V_{REF} [2:1] 5VREF must power up before or simultaneous to Vcc3.3. It must power down after or simultaneous to Vcc3.3.	Refer to “5VREF Sequencing Circuit” for an example circuit that may be used to ensure the proper 5VREF sequencing

17.7.16 IDE Checklist

Checklist Items	Recommendations	Reason/Impact/Documentation
PDD[15:0], SDD[15:0]	• No extra series termination resistors or other pull-ups/pull-downs are required. • PDD7/SDD7 does not require a 10 kΩ pull-down resistor. • Refer to ATA ATAPI-4 specification.	• These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	• No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	• These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.
PDREQ SDREQ	• No extra series termination resistors. • No pull-down resistors needed.	• These signals have integrated series resistors in the ICH2. • These signals have integrated pull-down resistors in the ICH2.

Checklist Items	Recommendations	Reason/Impact/Documentation
PIORDY SIORDY	• No extra series termination resistors. • Pull-up to 3.3 V via a 4.7 kΩ resistor.	• These signals have integrated series resistors in the ICH2.
IRQ14, IRQ15	• Recommend 8.2 kΩ—10 kΩ pull-up resistors to 3.3 V. • No extra series termination resistors.	• Open drain outputs from drive.
IDERST#	• The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal.	
Cable Detect:	• Host Side/Device Side Detection: • Connect IDE pin PDIAG/CBLID to an ICH2 GPIO pin. Connect a 10 kΩ resistor to GND on the signal line. • Device Side Detection: • Connect a 0.047µF capacitor from IDE pin PDIAG/CBLID to GND. No ICH2 connection.	• The 10 kΩ resistor to GND prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. • **NOTE:** All ATA66/ATA100 drives will have the capability to detect cables

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18 Layout Checklist

18.1 Processor and System Bus

18.1.1 AGTL+ Signals

This section covers the address, Data, DSTBn/p#, ADSTBn/p# and common clock signals. Refer to the *Intel® Xeon™ Processor at 1.40 GHz, 1.50 GHz, 1.7 GHz and 2 GHz Datasheet* for a System Bus list, signal types and definitions.

√	Recommendations	Reason/Impact/Documentation
	• Traces should maintain a greater than 3:1 edge to edge spacing versus trace to reference plane height ratio. Trace impedance should be 50 Ω ± 10%.	• This recommendation has been simulated and ensures a low crosstalk coefficient. A smaller ratio would have an unpredictable impact because of crosstalk. • If 3:1 ratio is requirement cannot be achieved, the separation should be maximized and the distance of the violation should be minimized. • Refer to Section 5.4.1, Table 12, and Figure 39.
	• Trace width recommendation is 5.0 mils with 15 mils edge-to-edge spacing for all signals.	• Intel has simulated these recommendations for normal conditions. • Refer to Section 5.4 and Section 5.4.1.
	• Data signal length should be 3 inches–10.1 inches pin-to-pin. Data signals of the same source synchronous group should be routed within 25 mils.	• The length compensation will result in minimizing the source synchronous skew that exists on the system bus. • Without trace matching and length compensation flight times between the data signals and the strobes will result in inequity between the setup and hold times. • Refer to Section 5.4.1 and Table 12.
	• DSTBn/p[3:0]# should be routed approximately 0.4 inch greater than the length of the corresponding data set between each agent. A strobe and its complement (DSTBp/n#) should be routed within ± 25 mils of the same pad-to-pad length.	• The impact of this recommendation causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. • It is recommended to simulate skew in order to determine the length that best centers the strobe for a given system. • Refer to Section 5.4.1 and Table 12.

√	Recommendations	Reason/Impact/Documentation
	• The requirements for the address signals are currently the same as for data. • In addition, address signals within a group should be routed within 50 mils of each other, pad to pad. • Refer to the length balancing spreadsheet in the processor signal integrity models.	• The length compensation will result in minimizing the source synchronous skew that exists on the system bus. • Without trace matching and length compensation flight times between the data signals and the strobes will result in inequity between the setup and hold times. • Address signals may change layers if reference plane remains the same. • VCC_CPU and VSS vias are placed as close to the signal via as possible to provide the shortest possible path for return current. • Refer to Section 5.4.1 and Table 12.
	• Source Synchronous groups and associated strobes should be routed on the same layer for the entire length of the bus. Thus, • REQ[4:0]#, A[16:3]# and ADSTB0# should be routed on the same layer • A[32:17]# and ADSTB1# should be routed on the same layer • D[15:0]#,DBI0# and DDSTBP0##, DSTBN0# should be routed on the same layer • D[31:16]#, DBI1# and DSTBP1#, DSTBN1# should be routed on the same layer • D[47:32]#, DBI2# and DSTBP2#, DSTBN2# should be routed on the same layer • D[63:48]#, DBI3# and DSTBP3#, DSTBN3# should be routed on the same layer	• These recommendations result in a significant reduction of flight time skew since the FR4 thickness, trace width, and velocity of the signals will be uniform across a single layer of the stack-up. • Changing layers may create a return path discontinuity, which can lead to unpredictable push-outs or push-ins and signal integrity problems. • Refer to Section 5.4.1, Table 12 and Table 14.
	• ADSTBn/p[3:0]# should be routed that is approximately 0.4 inch greater than the length of the corresponding data set between each agent. A strobe and its complement (ADSTBp/n) should be routed within ± 25 mils of the same pad-to-pad length. Refer to the length balancing spreadsheet in the processor signal integrity models.	• The impact of this routing recommendation causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. • Refer to Section 5.4.1 and Table 12.
	• Common clock signals should follow the same routing rules as the Data signals.	• Refer to Section 5.4.1 and Table 12.
	• The serpentine height (height to reference plane) to serpentine width between the serpentine bends) ratio should be greater than or equal to 5. No 90° serpentine bends. Utilize 45° serpentine bends as much as possible. Keep parallel sections as short as possible.	• This recommendation helps to control the serpentine in order to avoid signal integrity and timing problems that could occur from the coupling of the serpentine net. If coupling between serpentine parallel sections is high, this will cause significant timing skew when attempting to match trace lengths. • Refer to Section 5.2, Table 12 and Figure 36.
	• 25 mils spacing should be maintained around all clock and strobe traces	• Refer to Section 5.4.1 and Table 12.

18.1.2 Asynchronous GTL+ and Other Signals

√	Recommendations	Reason/Impact/Documentation
	• FERR#, PROCHOT#, and THERMTRIP# connects with the Topology 1 and should use dual termination • CPU0 to T-junction and T-junction to ICH2 should be 1 inch max. CPU0 to CPU1 should be 4 inches–6 inches max. CPU1 to ICH2 should be 1 inch–12 inches max. Pull-up resistor recommended value is 56 Ω ± 5%. • When routing to middle agents connect in true daisy chain topology. Trace impedance should be 50 Ω. Trace spacing should be 10 mils.	• Dual termination of the THERMTRIP# minimizes the effects of excessive undershoots that are seen at the processor. • Refer to Section 5.4.2.1 and Figure 41.
	• A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI# and STPCLK# connect in Topology 2 setup. • CPU0 to T-junction should be 0.25 inch–1 inch max. CPU0 to CPU1 should be 4 inches–6 inches max. CPU1 to ICH2 should be 1 inch–12 inches max. Pull-up resistor recommended value is 300 Ω ± 5%. • When routing to middle agents connect in true daisy chain topology. Trace impedance should be 50 Ω. Trace spacing should be 10 mils.	• Refer to Section 5.4.2.2 and Figure 42.
	• PWRGOOD connects in Topology 2. CPU0 to T-junction should be 0.25 inch–1 inch max. CPU0 to CPU1 should be 4 inches–6 inches max. CPU1 to ICH2 should be 1 inch–12 inches max. Pull-up resistor recommended value is 300 Ω ± 5%. • When routing to middle agents connect in true daisy chain topology. Trace impedance should be 50 Ω. Trace spacing should be 10 mils.	• Refer to Section 5.4.2.2 and Figure 44.
	• BR0# should be connected to the MCH. Terminate using a 41 Ω ± 5% pull-up resistor at the processor end. • BR1# should be connected to both processors and dual terminate using a 41 Ω ± 5% pull-up resistor. • BR[3:2] should be terminated individually at each processor, or should be connected between processors and terminated at one end using a 41 Ω ± 5% pull-up resistor.	• Refer to Section 5.4.2.5 and Figure 45.
	• Place 43.2Ω ± 1% resistors as close to COMP[1:0] as possible.	• Refer to Section 5.4.2.6.
	• End processor should have ODTEN enabled whereas middle agents should have ODTEN disabled.	• Refer to Section 5.4.2.7.

18.1.3 CK-SKS Clocking

√	Recommendations	Reason/Impact/Documentation
	• 25 mil spacing required around all 100 MHz differential clocks	• Refer to Section 5, Section 4.1, Table 7 and Table 12.
	• Differential Clocks should be routed on same layer. If vias are required, dummy vias must be placed on other differential Clock signals.	• This recommendation is to minimize clock skew due to clock pair to clock pair inconsistencies. • Refer to Section 4.1.
	• Route 100 MHz differential clocks to all agents on the same physical layer.	• Constraining all bus clocks to one physical layer minimizes the impact on skew due to variations in ε_r (dielectric constant), and impedance due to physical tolerances of circuit board material. Routing on internal layers reduces impedance variations and ε_r. • Refer to Section 4.1.
	• Connect individual differential clock signal from the CK_SKS to the MCH, ITP port and the processor. • CK_SKS to series resistor should be 0.5 inch max. • Series resistor to termination resistor node should be 0.2 inch max. Termination resistor node to actual termination resistor should be 0.2 inch max. Termination resistor node to processor socket should be 12 inches max for Host_CPU and Host_ITP clocks. • Termination resistor node to MCH should be 12 inches for Host_MCH clocks. Add 0.30 inch ± 10% for length matching to Host_MCH clock to compensate for processor socket and package delay.	• Refer to Section 4.1, Table 7 and Figure 15.
	• Traces must be 50O Ω ± 10% single ended and 100 Ω differential.	• Refer to Section 4.1.
	• Trace width for clocks is 4 mils and spacing between each end of the differential clock should be 16 mils min and 20 mils max. Uniform spacing should be maintained through the entire length of the trace.	• Degradation in noise rejection will occur if spacing is not uniform. • Refer to Section 4.1 and Table 7.
	• All Host Clocks must be Ground Referenced.	• This ensures that proper current return path is available. • Refer to Section 4.1.
	• Connect individual 33 MHz clock signals to ICH2, FWH, and SIO. Trace length from CK_SKS chip to series resistor should be 0 inch –0.5 inch and from series resistor to receiver should be Z + (4 inches–6 inches). Route signals on a single layer. • Z = 5 inches to 9 inches	• This recommendation insures setup and hold times in relation to the other clock signals are maintained. Clock length routing relationships between clock signals should be observed. Refer to Section 4.3.1. • Refer to Section 4.3, Section 4.3.3, Table 11, Figure 31 and Figure 27.

√	Recommendations	Reason/Impact/Documentation
	• Connect individual PCI 33 MHz clock signals to PCI slots. Trace length from CK_SKS chip to series resistor should be 0 inch–0.5 inch and from series resistor to receiver should be Z + (2 inches–4 inches). Route signals on a single layer. • Z = 5 inches to 9 inches	• This recommendation insures setup and hold times in relation to the other clock signals are maintained. Clock length routing relationships between clock signals should be observed. Refer to Section 4.3.1. • Refer to Section 4.3, Section 4.3.3, Table 11, Figure 30 and Figure 27.
	• Connect individual 66 MHz clock signals to ICH2 and MCH. • Trace length from CK_SKS to series resistor should be 0 inch–0.5 inch and from series resistor to receiver should be Z + (4 inches–5 inches). Route signals on a single layer. • Z = 5 inches to 9 inches.	• This recommendation insures setup and hold times in relation to the other clock signals are maintained. Clock length routing relationships between clock signals should be observed. Refer to Section 4.3.1. • Refer to Section 4.3, Table 10 and Figure 29.
	• Connect 66 MHz clock signal to AGP connector. • Trace length from the CK_SKS to series resistor should be 0 inch– 0.5 inch and from series resistor to receiver should be equal to Z (5 inches to 9 inches Route signals on a single layer.	• This recommendation insures setup and hold times in relation to the other clock signals are maintained. Clock length routing relationships between clock signals should be observed. Refer to Section 4.3.1. • Refer to Section 4.3, Table 10 and Figure 28.

18.1.4 Processor Decoupling

√	Recommendations	Reason/Impact/Documentation
	• Place 4–6 high frequency 0.1 µF caps with 0603 package distributed evenly over the system bus data lines.	• This recommendation reduces return path discontinuities that result from system board traces having only one reference plane (microstrip). • Refer to Section 5.3.1 and Figure 37.
	• Place 3–4 high frequency 0.1 µF caps with 0603 packages distributed evenly over the system bus address and control lines.	• This recommendation reduces return path discontinuities that result from system board traces having only one reference plane (microstrip). • Refer to Section 5.3.1 and Figure 37.
	• Place 24 1206 package 10 µF capacitors as close to processor ground and power pins as possible. • All capacitors should be placed as close to the processor package as the processor keep-out zone allows.	• These high frequency decoupling capacitors are needed to meet voltage transients.

18.1.5 Chipset Decoupling

√	Recommendations	Reason/Impact/Documentation
	• 4–5, 0.1 µF caps with 0603 packages distributed evenly over the system bus data lines. Place as close as possible to the MCH package.	• This recommendation reduces return path discontinuities that result from system board traces having only one reference plane (microstrip). • Refer to Section 5.5.1 and Figure 49.
	• 2–3, 0.1 µF caps with 0603 packages distributed evenly over the system bus address and control lines. Place as close as possible (within 150 mils) to the MCH package.	• This recommendation reduces return path discontinuities that result from system board traces having only one reference plane. These recommendations are only used for designs containing microstrip configurations. • Refer to Section 5.5.1 and Figure 49.

18.1.6 AGTL+ (V_{REF}, HDVREF [3:0], HAVREF [1:0], and CCVREF)

√	Recommendations	Reason/Impact/Documentation
	• Processor must have at least two dedicated voltage dividers. There are 4 GTLREF signals on the processor.	• Refer to Section 12.17.2.
	• Intel® 860 Chipset MCH requires one dedicated voltage divider. Voltage divider must be within 1.5 inches of MCH V_{REF} ball.	• Refer to Section 5.5 and Figure 47.
	• Decouple each voltage divider with a 1 µF cap and each V_{REF} pin with a 220 pF cap as close to the pin as possible.	• This recommendation provides a low impedance line without the cost of additional plane or island. • Refer to Section 5.3.

18.2 Rambus* Routing Guidelines

18.2.1 RSL Signals

√	Recommendations	Reason/Impact
	• MCH to 1st RIMM of Channel A or 1st RIMM connector of Channel B 1 inch–6 inches	• Refer to Section 6.3.1, Table 18, and Figure 52.
	• RIMM connector to RIMM connector of the same channel 0.4 inch to 1 inch.	• Refer to Section 6.3.1, Table 18, and Figure 52.
	• RIMM connector to termination < 2 inches. The trace length between the last RIMM connector and the termination resistors should be less than 2 inches.	• Length matching in this section is not required. • Refer to Section 6.3.1, Table 18, and Figure 52.
	• RSL traces 18 mils trace width, 6 mil space, and 10 mil ground flood, 6 mil space.	• Refer to Section 6.3.1 and Figure 53.
	• All signals must be length matched within ± 10 mils of the Nominal RSL Length as described in this design guide. Ensure that signals with a dummy via are compensated correctly.	• Refer to Section 6.3.1.
	• ALL RSL signals must have 1 via near the MCH BGA pad. Signals routed on the secondary side of the motherboard will have a “real via” while signals routed on the top layer will have a “dummy via”. Additionally, all signals with a dummy via must have an additional trace length of 25 mils.	• Refer to Section 6.3.1.
	• Signals must “alternate” layers.	• Refer to Section 6.3.2.4.
	• At least 10 mils ground flood isolation required around ALL RSL signals (ground isolation must be exactly 6 mils from RSL signals). Ground flood recommended for isolation. This ground flood should be as close to the MCH (and the 1st RIMM connector) as possible. If possible, connect the flood to the ground balls/pins on the MCH/connector. • To control crosstalk and odd/even mode velocity deltas.	• Refer to Section 6.3.1.
	• When RSL traces neckdown to exit the MCH BGA, the minimum width is 15 mils and the neckdown is no longer than 25 mils in length	• To minimize impedance discontinuities
	• Uniform ground isolation flood is exactly 6 mils from the RSL signals at all times	• Refer to Section 6.3.1 and Figure 53.
	• RSL traces Do NOT neckdown when routing into the RIMM connector	• To minimize impedance discontinuities

√	Recommendations	Reason/Impact
	• If tight serpentining is necessary, 10 mil ground isolation MUST be between serpentine segments	• I.e. an RSL signal CANNOT serpentine so tightly that the signal is adjacent to itself with no ground isolation between the serpentines.
	• ALL RSL, CMD/SCK and CTM/CTM#/CFM/CFM# signals have CTABs on each RIMM connector pin.	• Compensation for the inductance of the connector. Voltage and timing margins may be reduced with CTABs. • Refer to Section 6.3.2.5.
	• CTABs must not cross (or be on top of) power plane splits. They must be ENTIRELY referenced to ground.	• Refer to Section 6.3.2.5.
	• All RSL signals are routed adjacent to a ground reference plane.	• This includes all signals from the 2nd RIMM connector to the termination. If signals are routed referenced to ground from the 2nd RIMM connector to the termination, the ground reference plane **must** extend under these signals **and** include the ground side of the Vterm decoupling capacitors.
	• The traces for CMD and SCK must have a neck down from 18 mil traces to 5 mil traces for 175 mil s on either side of the SCK/CMD attach point.	• To minimize impedance discontinuities. • Refer to Section 6.3.7 and Figure 64.
	• Voltage divider network for reference voltage generation should be within 1.5 inches of the MCH V_{REF} ball.	• Refer to Section 5.5 and Figure 47.
	• RSL traces do not cross power plane splits. RSL signals must also not be routed *next to* a power plane split	• To maintain signal integrity.

18.2.2 Ground Isolation:

√	Recommendations	Reason/Impact
	• Via to ground every ½ inch around edge of isolation island, between RIMM connectors and between RSL signals (from MCH to 1St RIMM connector)	• Refer to Section 6.3.
	• Via between every signal within 100 mils of the MCH edge and the connector edge.	• Refer to Section 6.3.
	• No unconnected ground floods	• To avoid discontinuity in ground planes.
	• Ground isolation fills between serpentines	• To avoid crosstalk.
	• Ground isolation not broken by C-tabs	• To avoid discontinuity in the ground plane. • Refer to Section 6.3.2.5 and Figure 57 through Figure 59.
	• Ground isolation connects to the ground pins in the middle of the RIMM connector.	
	• Ground isolation vias connect on all layers and should NOT have thermal relieves.	
	• Ground pins in RIMM connector should connect on all layers.	

18.2.3 Vterm Layout

√	Recommendations	Reason/Impact
	• Solid Vterm island is on top routing layer; do not split this plane	
	• Ground island(for ground side of Vterm caps) is on top routing layer	
	• Termination resistors connect directly to the Vterm island on the top routing layer(without vias)	• Refer to Section 6.3.3 for further details.
	• Decoupling caps connect to top layer Vterm island and top routing layer ground island directly.	
	• Use at least 2 vias per decoupling caps in the top layer ground island.	
	• Use 2X100 µF Tantalum caps to decouple Vterm.	• Refer to Section 6.3.3 for further details.
	• Hi-frequency decoupling caps must be spread-out across the termination island so that all termination resistors are near high frequency caps.	• Refer to Section 6.3.3 for further details.
	• 100 µF Tantalum cap should be at each end of the Vterm island.	• Refer to Section 6.3.3 for further details.
	• 100 µF Tantalum caps must be connected to the Vterm island directly	• Refer to Section 6.3.3 for further details.
	• 100 µF Tantalum caps must have at least 2 vias/cap to ground.	
	• Vterm island should be 50 mils wide	• Refer to Section 6.3.3 for further details.
	• The trace length between the last RIMM connector and the termination resistors should be less than 3 inches.	• Refer to Section 6.3.3 for further details.

18.2.4 Direct Rambus* Clock Generation (DRCG* Device) Recommendations

√	Recommendations	Reason/Impact/Documentation
	• 3VMRef trace routed from CKx-SKS must be 6 mils wide and separated by 6 mil space on both sides. 6 mil wide ground isolation trace should be placed after 6 mil space. Max trace length is 8 inches.	• This recommendation is for micro strip applications. • Refer to Section 4.2.1 and Figure 19.
	• VddIR pin on the DRCG device can be connected to 3.3 V plane near the DRCG device if the plane extends near the DRCG device. However, if a 3.3 V trace must be used, it should originate at the clock synthesizer and routed 6 mil wide with 6 mil spacing with 6 mil wide ground trace following.	• Refer to Section 4.2.1 and Figure 19.
	• RCLKOUT and HCLKOUT from MCH must be routed to SYNCLKN and PCLKM on the DRCG device. • Signals must be routed together about 12 mils apart with 6 mil wide traces. 6 mil wide ground trace located on each side of the pair. 6 mil spacing between the ground trace and RCLKOUT and HCLKOUT signals. Max trace length is 6 inches and must be length matched within 50 mils	• If signals must switch layers then they should switch layers together. • Refer to Section 4.2.2 and Figure 20.
	• VddIPD pin on the DRCG device can be connected to 1.8 V plane near the DRCG device if the plane extends near the DRCG device. However, if a 1.8 V trace must be used, it should originate at the CK00 clock synthesizer and routed 6 mil wide with 6 mil spacing with 6 mil wide ground trace.	• Refer to Section 4.2.2 and Figure 20.
	• Series resistors (39) should be mounted very near CTM/CTM# pins. Parallel resistors (51) should be very near series resistors.	• Refer to Section 4.2.3 and Figure 21.
	• CFM pair trace length: MCH to 1st RIMM connector 1 inch–6 inches. RIMM connector to RIMM connector 0.4 inch–1.0 inch. 2nd RIMM connector to termination 0 inch–2 inches	• Refer to Section 4.2.3.1 and Figure 15.
	• CTM pair trace length: DRCG device to 2nd RIMM connector 0 inch–6 inches. RIMM connector to RIMM connector 0.4 inch–1.0 inch. 1st RIMM connector to MCH 1 inch–6 inches	• Refer to Section 4.2.3.1 and Figure 15.
	• CTM & CFM pairs routed differentially should be routed –22 mil ground trace—6 mil spacing—14 mil trace width (clock) —6 mil spacing—14 mil trace width (clock#)—6 mil spacing—22 mil ground trace.	• Refer to Section 4.2.3.1 and Figure 15.

√	Recommendations	Reason/Impact/Documentation
	• If CTM & CFM pairs routed single ended route 10 mil ground trace, 6 mil spacing, 18 mil wide clock trace, 6 mil wide spacing and then use 10 mil ground trace.	• Refer to Section 4.2.3.1 and Figure 22.
	• CFM and CTM pairs must be Ground Referenced at all time.	• This recommendation ensures a proper return current path. • Refer to Section 4.2.3.1 and Figure 22.
	• CFM and CTM pairs must have additional 0.021 inches of trace for every 1inch of RSL trace.	• This added length is to compensate for the clocks faster velocity. • Refer to Section 4.2.3.2 for further details.
	• Ensure that each clock pair is length matched within ± 2 mils of the RSL channel length. Exact matching is preferred.	• Refer to Section 4.2.3.2 for further details.
	• Vias are placed in ground isolation traces and ground reference every 1 inch	• Refer to Section 4.2.3.2 for further details.
	• When CTM/CTM# serpentine together, they MUST maintain EXACT mils spacing	• Refer to Section 4.2.3.2 for further details.

18.2.5 DRCG* Device Layout- Clean Power Supply

√	Recommendations	Reason/Impact
	• 3.3 V DRCG device power flood on the top layer. This should connect to each high frequency (0.1µF) capacitors are near the DRCG device power pins. One capacitor next to each power pin.	• Refer to Section 4.2.5 and Figure 26 for further details.
	• 10 µF bulk *tantalum* capacitor near DRCG device connected directly to the 3.3 V DRCG device power flood on the top layer	• Refer to Section 4.2.5 and Figure 26 for further details.
	• Ferrite bead isolating DRCG device power flood from 3.3 V main power.	• Refer to Section 4.2.5 and Figure 26 for further details.

18.2.6 DRCG - CTM/CTM# Output Network Layout

√	Recommendations	Reason/Impact
	• Series resistors (39 Ω) should be mounted very near CTM/CTM# pins. Parallel resistors (51Ω) should be very near series resistors.	• Refer to Section 4.2.5 and Figure 26 for further details.
	• CTM/CTM# should be 18 mils wide from the CTM/CTM# pins to the resistors	
	• CTM/CTM# should be 14 on 6 routed differential as soon as possible after the resistor network. When not 14 on 6, the clocks should be 18 mils wide	
	• Ensure CTM/CTM# are ground referenced and the ground reference is connected to the ground plane every ½ inch to 1 inch	
	• Ensure CTM/CTM# are ground isolated and the ground isolation is connected to the ground plane every ½ inch to 1 inch	

18.2.7 RAMREF Routing

√	Recommendations	Reason/Impact
	• Ensure 1 x 0.1 µF capacitor on V_{REF} at each RIMM connector	• Refer to Section 6.3.4 and Figure 61 for further details.
	• Use 10 mil wide trace.	
	• Do not route V_{REF} near high-speed signals	
	• V_{REF} minimum trace spacing should be 25 mils.	• To reduce crosstalk and maintain signal integrity.

18.3 AGP Guidelines

18.3.1 All 1X Signals

The 1X signals are: CLK, RBF#, WBF#, ST [2:0], PIPE, REQ#, GNT#, PAR, FRAME#, IRDY#, TRDY, STOP# and DEVSEL#.

√	Recommendations	Reason/Impact
	• Max trace length 7.5 inches	• Refer to Section 7.1.1 for further details.
	• 5 mil trace width, 5 mil trace separation	• Refer to Section 7.1.1 for further details.
	• No trace matching requirements for 1X signals.	• Refer to Section 7.1.1 for further details.

18.3.2 2X/4X Signals

The 2X/4X signals are: AD [31:0], C/BE [3:0]#, ADSTB [1:0]#, SBA [7:0], SB_STB, SB_STB#

If AGP is less than 6 inches		
√	Recommendations	Reason/Impact
	• 5 mil trace width 15 mil separation between data to data for 60 Ω ± 10%, for ± 15% its 20 mils	• Refer to Section 7.1.2.1 for further details.
	• 5 mil trace width 20 mil separation between data to strobes for 60 Ω ± 10% and 15%	• Refer to Section 7.1.2.1 for further details.
	• 5 mil trace width 15 mil separation between strobe to strobe for 60 Ω ± 10%, for ± 15 Ω its 20 mils	• Refer to Section 7.1.2.1 for further details.
	• If AGP Interface is <6 inches long, DATA and C/BE#s must be length-matched within ± 0.25 inch of strobes.	• Refer to Section 7.1.2.1 for further details.
	• Strobe pairs must be length matched ± 0.1 inch	• Refer to Section 7.1.3 and Table 24 for further details.
	• Route AD [15:0], C/BE [1:0]#, AD_STB0, and AD_STB0# together. (Good recommendation, but not in the AGP specification)	• Signals to be kept on same stripline. Microstrip to microstrip and stripline to stripline.
	• Route AD [31:16], C/BE [3:2]#, AD_STB1, and AD_STB1# together. (Good recommendation, but not in the AGP specification)	• Signals to be kept on same stripline. Microstrip to microstrip and stripline to stripline.
	• Route SBA [7:0], SB_STB, SB_STB# together. (Good recommendation, but not in the AGP specification)	• Signals to be kept on same stripline. Microstrip to microstrip and stripline to stripline.

If AGP is less than 6 inches		
√	**Recommendations**	**Reason/Impact**
	• Recommended that all strobes be ground referenced as well as TRDY#, IRDY#, GNT#.	• Refer to Section 7.1.5 for further details.
	• Recommended that ½ the AGP signals are ground referenced.	• Refer to Section 7.1.5 for further details.
	• For signals that require a pull-up or pull-down, keep stub less than 0.5 inch for 1X signals and 0.1 for 2X/4X signals.	• This is to minimize signal reflections from the stub. • Refer to Section 7.1.9 for further details.
	• Pour a Ground flood under the VDDq plane	• Optimizes the mutual inductance between two planes. • Refer to Section 7.1.9 for further details.

If AGP Interface is greater than 6 inches but less than 7.25 inches		
√	**Recommendations**	**Reason/Impact**
	• Board impedance must be 60 Ω ± 10%	• Refer to Section 7.1.2.2 for further details.
	• 5 mil trace width 20 mil separation between data to data	• Refer to Section 7.1.2.2 for further details.
	• 5 mil trace width 20 mil separation between data to strobes	• Refer to Section 7.1.2.2 for further details.
	• 5 mil trace width 20 mil separation between strobe to strobe	• Refer to Section 7.1.2.2 for further details.
	• DATA and C/BE#s must be length-matched within ± 0.125 inch of strobes.	• Refer to Section 7.1.2.2 for further details.
	• Strobe pairs must be length matched ± 0.1 inch	• Refer to Section 7.1.3 and Table 24 for further details.
	• Route AD [15:0], C/BE [1:0]#, AD_STB0, and AD_STB0# together. (Good recommendation, but not in the AGP specification)	• Signals to be kept on same stripline. Microstrip to microstrip and stripline to stripline.
	• Route AD [31:16], C/BE [3:2]#, AD_STB1, and AD_STB1# together. (Good recommendation, but not in the AGP specification)	• Signals to be kept on same stripline. Microstrip to microstrip and stripline to stripline.
	• Route SBA [7:0], SB_STB, SB_STB# together. (Good recommendation, but not in the AGP specification)	• Signals to be kept on same stripline. Microstrip to microstrip and stripline to stripline.
	• Recommended that all strobes be ground referenced as well as TRDY#, IRDY#, GNT#.	• Refer to Section 7.1.5 for further details.
	• Recommended that ½ the AGP signals are ground referenced.	• Refer to Section 7.1.5 for further details.
	• For signals that require pull-up or pull-down, keep stub less than 0.5 inch for 1X signals and 0.1 for 2X/4X signals.	• This is to minimize signal reflections from the stub. • Refer to Section 7.1.9 for further details.
	• Pour a VSS flood under Vddq plane	• Optimizes the mutual inductance between two planes. • Refer to Section 7.1.9 for further details.

18.3.3 MCH AGP Decoupling

√	Recommendations	Reason/Impact
	Min of six, 0.01 µF caps spread evenly around the MCH AGP interface.	It is recommended that a low ESL ceramic capacitor, such as a 0603 body type, X7R dielectric. Refer to Section 7.1.4 for further details.
	Must be within 0.15 inch from package	Refer to Section 7.1.4 for further details.
	Pour a VSS flood under VDDQ plane to decouple AGP.	To help lower inductive path from the power balls on the package to the decoupling capacitor Refer to Section 7.1.4 for further details.

18.3.4 AGP Connector Decoupling

√	Recommendations	Reason/Impact
	• Place one, 0.01 µF cap next to each power pin i.e., Vcc1.5, Vddq, +5, +12, and 3.3 VAUX on connector.	• Refer to Section 7.1.11 for further details.
	• For Bulk decoupling, place one 10 µF tantalum cap to VDDQ and a 20 µF tantalum cap on Vcc3.3 plane near connector.	• Refer to Section 7.1.11 for further details.

18.4 8-Bit Hub Interface

√	Recommendations	Reason/Impact
	• Board impedance must be 60 Ω ± 15%	• Use when operating in normal mode. • Refer to Section 8.3 for further details.
	• Board impedance can be 50 Ω ± 10% or 60 Ω ± 15 Ω.	• Use when operating in enhanced mode. • Refer to Section 8.3 for further details.
	• Traces must be routed 5 mils wide with 20 mils spacing	• Refer to Section 8.3.1 for further details.
	• In order to breakout of the MCH and ICH2 package the hub interface signals can be routed 5 on 5. Signals must be separated to 5 on 20 within 300 mils of the package.	• Refer to Section 8.3.1 for further details.
	• Max trace length is 6 inches for normal buffer mode	• Refer to Section 8.3.1 for further details.
	• Max trace length is 14 inches for enhanced buffer mode.	• Refer to Section 8.3.1 for further details.
	• Data signals must be matched within ± 0.1 inch of the HL_STB diff pair.	• Refer to Section 8.3.1 for further details.
	• Each strobe signal must be the same length.	• Refer to Section 8.3.2 for further details.
	• HIREF divider should be placed no more than 1 inch away from ICH2. If so, place more than one 0.01 µF capacitor placed near the HUBREF pin.	• Refer to Section 8.3.3 for further details.
	• HIREF divider should be placed no more than 3.5 inches away from MCH. If so, then need separate resistor divider placed locally.	• Refer to Section 8.3.3 for further details.

18.4.1 Hub Decoupling

√	Recommendations	Reason/Impact
	• Two, 0.01 µF caps per each component (MCH and ICH2) spread over the Hub Interface.	• Implemented to improve power delivery. • Refer to Section 8.3.5 for further details.
	• Place within 150 mils of each package.	• Implemented to improve power delivery. • Refer to Section 8.3.5 for further details.

18.5 16-Bit Hub Interface

√	Recommendations	Reason/Impact
	• Board impedance must be 50 Ω ± 10% or 60 Ω ± 15% in enhanced buffer mode.	• Interface only support enhanced buffer mode. • Refer to Section 8.4.1 for further details.
	• Both HUBREF and HSWING must be routed 20–25 mils from all other signals.	• Refer to Section 8.4.1 for further details.
	• Traces must be routed 5 mils wide with 20 mils spacing	• Refer to Section 8.4.1 for further details.
	• In order to breakout of the MCH and P64H package the hub interface signals can be routed 5 on 5. Signals must be separated to 5 on 20 within 300 mils of the package.	• Refer to Section 8.4.1 for further details.
	• Max trace length for hub interface signals is 14 inches	• Refer to Section 8.4.1 for further details.
	• Data signals must be matched within ± 0.1 inch of the HL_STB[1:0] diff pair.	• Refer to Section 8.4.1 for further details.
	• Each strobe signal must be the same length.	• Refer to Section 8.4.2 for further details.
	• HUBREF divider should be placed no more than 3.5 inches of away from MCH. If so, then it needs separate resistor divider placed locally.	• Refer to Section 8.4.2 for further details.
	• HUBREF divider should be placed no more than 1 inch of away from P64H. If so, then place more than one 0.1 µF capacitor placed near the HUBREF pin.	• Refer to Section 8.4.2 and Figure 80 for further details.

18.5.1 Hub Decoupling

√	Recommendations	Reason/Impact
	• Three, 0.01 µF caps per each component (MCH and ICH2) spread over the Hub Interface.	• Refer to Section 8.4.6 for further details.
	• Place within 150 mils of each package.	• Implemented to improve power delivery. • Refer to Section 8.4.6 for further details.

18.6 IDE Interface

√	Recommendations	Reason/Impact
	• 5 mil wide and 10 mil spaces	• Refer to Section 9.1 for further details.
	• Max trace length is 8 inches in length	• Refer to Section 9.1 for further details.
	• Shortest trace length must be 0.5 inch shorter than the longest trace length.	• Refer to Section 9.1 for further details.

18.7 AC'97

√	Recommendations	Reason/Impact
	• Z_O AC97 = 60 Ω ±15%	• Refer to Section 9.2 for further details.
	• 5 mil trace width, 5 mil spacing between traces	• Refer to Section 9.2 for further details.
	• Max Trace Length ICH2/Codec/CNR = 12 inches	• Refer to Section 9.2 for further details.

18.8 USB

√	Recommendations	Reason/Impact
	• Characteristic impedance of individual signal lines P+, P- Zo = 45 Ω (90Ω Differential)	• Refer to Section 9.3 and Figure 101 for further details.
	• Stack-up: 9 mils wide, 25 mil spacing between Differential pairs	• Refer to Section 9.3 and Figure 101 for further details.
	• Trace Characteristics: — Line Delay = 160.2 ps — Capacitance = 3.5 pF — Inductance = 7.3 nH — Res @ 20° C = 53.9 mΩ	• Refer to Section 9.3 and Table 37 for further details.
	• 15 Ω series resistor to be placed < 1 inch from ICH2	• This is required for source termination of the reflected signal. • Refer to Section 9.3 and Figure 101 for further details.
	• 47 pF parallel caps should be placed as close to the ICH2 as possible	• Refer to Section 9.3 and Figure 101 for further details.
	• 15K ±5% pull-down resistors should be placed as close to the ICH2 as possible.	• Refer to Section 9.3 and Figure 101 for further details.
	• Stub length due to 15K pull-downs should be as short as possible.	• Refer to Section 9.3 and Figure 101 for further details.

18.9 Intel® ICH2 Decoupling

√	Recommendations	Reason/Impact
	• 3.3 V Core: six 0.1 µF caps	• To prevent large current swings when switching from logic high and logic low. • Refer to Section 9.10 and Table 44.
	• 3.3 V Stand By: one 0.1 µF cap	• To prevent large current swings when switching from logic high and logic low. • Refer to Section 9.10 and Table 44.
	• CPU I/F(Vcc core): one 0.1 µF cap	• To prevent large current swings when switching from logic high and logic low. • Refer to Section 9.10 and Table 44.
	• 1.8 V Core: two 0.1 µF cap–already included in Hub decoupling	• To prevent large current swings when switching from logic high and logic low. • Refer to Section 9.10 and Table 44.
	• 1.8 V Stand By: one 0.1 µF cap	• To prevent large current swings when switching from logic high and logic low. • Refer to Section 9.10 and Table 44.
	• 5 V Reference: one 0.1 µF cap and one 1.0 µF	• To prevent large current swings when switching from logic high and logic low. • Refer to Section 9.10 and Table 44.
	• 5 V Reference Stand By: one 0. 1 µF cap	• To prevent large current swings when switching from logic high and logic low. • Refer to Section 9.10 and Table 44.

18.10 RTC

√	Recommendations	Reason/Impact
	• RTC LEAD length <= 0.25 inch Max	• Refer to Section 9.7.3.
	• Minimize capacitance between Xin and Xout	• Refer to Section 9.7.3.
	• Put GND plane underneath Crystal components	• Refer to Section 9.7.3.
	• Do not route switching signals under the external components (unless on other side of board)	• Refer to Section 9.7.3.

18.11 LAN Connect I/F

√	Recommendations	Reason/Impact
	• Stack-up: 5 mils wide, 10 mil spacing	
	• Z_O = 60 Ω ± 15%	• Signal integrity requirement.
	• LAN Max Trace Length ICH2 to CNR: L = 3 inches to 9 inches (0.5 inch to 3 inches on card)	• To meet timing requirements.
	• Stubs due to R-pak CNR/LOM stuffing option should not be present.	• To minimize inductance.
	• Maximum Trace Lengths: ICH2 to 82562EH/ET/EM : L = 4.5 inches to 8.5 inches	• To meet timing requirements.
	• Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inch	• To meet timing and signal quality requirements.
	• Maintain constant symmetry and spacing between the traces within a differential pair.	• To meet timing and signal quality requirements.
	• Keep the total length of each differential pair under 4 inches.	• Issues found with traces longer than 4 inches: IEEE phy conformance failures, excessive EMI and or degraded receive BER.
	• Do not route transmit differential traces closer than 70 mils to the receive differential traces.	• To minimize crosstalk.
	• Distance between differential traces and any other signal line is 70 mils.	• To minimize crosstalk.
	• Keep Max separation between differential pairs to 7 mils.	• To meet timing and signal quality requirements.
	• Differential trace impedance should be controlled to be ~100 Ω.	• To meet timing and signal quality requirements.
	• For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two, 45° bends.	• To meet timing and signal quality requirements.
	• Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	• This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
	• Do not route traces and vias under crystals or oscillators.	• This will prevent coupling to or from the clock.
	• Trace width to height ratio above the ground plane should be between 1:1 and 3:1.	• To control trace EMI radiation.
	• Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	• Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.
	• Vias to decoupling capacitors should be sufficiently large in diameter.	• To decrease series inductance.

√	Recommendations	Reason/Impact
	• Avoid routing high-speed LAN or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.	• To minimize crosstalk.
	• Isolate I/O signals from high speed signals.	• To minimize crosstalk.
	• Place the 82562ET/EM part more than 1.5 inches away from any board edge.	• This minimizes the potential for EMI radiation problems.
	• Verify proper EEPROM size: — 82562ET–64 word — 82562EM–256 word	• The 82562EM requires a larger EEPROM to store the alert envelope and other configuration information.
	• Place at least one bulk capacitor (4.7 µF or greater OK) on each side of the 82562ET/EM.	• Research and development has shown that this is a robust design recommendation.
	• Place decoupling caps (0.1 µF) as close to the 82562ET/EM as possible.	
	• RBIAS10 and RBIAS100 resistors should be 1% values	• These are biasing resistors that require 1% accuracy. Keep mind that the values shown on the reference schematic are recommended starting values. Fine tuning (with IEEE conformance testing) is required for every new design.

18.12 Miscellaneous Routing Guidelines

√	Recommendations	Reason/Impact
	• IDE Interface routed on one layer	
	• CNR and on board Codec	

Appendix A: Customer Reference Board Schematics

This appendix provides a set of schematics for the Intel® Xeon™ processor /Intel® 860 chipset Platform Customer Reference Board (CRB).

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INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD

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INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Fri May 18 13:49:12 2001	SHEET: 1

DRAWING

CR-2

VOLTAGE TABLE

SYMBOL	NETNAME		PAGE
+12V :	+12V	:POWER SUPPLY OUTPUT	: P.52
+3.3V:	+3_3V	:POWER SUPPLY OUTPUT	: P.52
-12V :	-12V	:POWER SUPPLY OUTPUT	: P.52
N\A :	AGP_VDDQ	:VOLTAGE REGULATOR OUTPUT FROM +3.3V	: P.52
N\A :	GND	:SYSTEM DC GROUND	
N\A :	P12V_CPU	:POWER SUPPLY OUTPUT	: P.52
N\A :	COIL_P12V_CPU	:POWER SUPPLY OUTPUT	: P.53
+1.8V:	P1_8V	:VOLTAGE REGULATOR OUTPUT FROM +12V	: P.54
+5V :	P5V	:POWER SUPPLY OUTPUT	: P.52
N\A :	SB1_8V	:VOLTAGE REGULATOR OUTPUT FROM SB5V	: P.54
SB5V :	SB5V	:POWER SUPPLY OUTPUT	: P.52
N\A :	SB2.5V	:VOLTAGE REGULATOR OUTPUT FROM SB5V ON MEC	: P.20
SB3V :	STANDBY3V	:POWER SUPPLY OUTPUT	: P.52
N\A :	VCC_CORE	:VR OUTPUT FROM P12V_CPU	: P.53
N\A :	VCC3_CLK	:CK00 FILTERED POWER FROM +3.3V	: P19
N\A :	DRCGA_3_3V	:DRCGA FILTERED POWER FROM +3.3V	: P21
N\A :	DRCGB_3_3V	:DRCGB FILTERED POWER FROM +3.3V	: P21
N\A :	AGND	:FILTERED GND FOR SERIAL,PARALLEL,USB,KEYBRD,MOUSE	: P38
N\A :	AUD_GND	:FILTERED GND ISLAND FOR AUDIO	: P48
N\A :	AUD_VCC	:+5V VOLTAGE REGULATOR OUTPUT FROM +12V	: P47
N\A :	CHGND	:CHASSIS GND	: P50

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VOLTAGE TABLE

SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: VOLTAGE TABLE

REV: 1.0

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED:
Thu May 17 14:04:38 2001

SHEET: 2

DEVICE TABLE

DEVICE	POWER	PINS
MCH U6D1 PAGES 16-18	+1.8V	A6 A9 AA12 AA13 AA14 AA15 AA18 AA19 AA20 AA21 AA27 AB8 AB9 AB10 AB11 AB16 AB17 AB22 AB23 AB24 AB25 AB30 AC8 AC9 AC10 AC11 AC16 AC17 AC22 AC23 AC24 AC25 AD8 AD9 AD10 AD11 AD16 AD17 AD22 AD23 AD24 AD25 AE8 AE9 AE10 AE11 AE16 AE17 AE22 AE23 AE24 AE25 AF22 B29 B31 C5 C8 C15 C19 C22 D11 D26 D27 E7 E10 E31 F15 F20 F21 F25 G7 G8 G9 G11 G29 G32 H5 H8 H9 H10 H11 H16 H17 H22 H23 H24 H25 H26 J8 J9 J10 J11 J16 J17 J22 J23 J24 J25 J27 J30 K5 K7 K8 K9 K10 K11 K16 K17 K22 K23 K24 K25 L8 L9 L10 L11 L16 L17 L22 L23 L24 L25 L27 L29 M12 M13 M14 M15 M18 M19 M20 M21 N12 N13 N14 N15 N18 N19 N20 N21 P12 P13 P14 P15 P18 P19 P20 P21 R12 R13 R14 R15 R18 R19 R20 R21 R27 R30 T8 T9 T10 T11 T16 T17 T22 T23 T24 T25 U8 U9 U10 U11 U16 U17 U22 U23 U24 U25 V12 V13 V14 V15 V18 V19 V20 V21 W12 W13 W14 W15 W18 W19 W20 W21 W30 Y12 Y13 Y14 Y15 Y18 Y19 Y20 Y21 Y27
	VCC_CORE	AB2 AB5 AB7 AD1 AD4 AD7 AF3 AF6 AF9 AF11 AG5 AG10 AG12 AG14 AH2 AH5 AJ9 AJ11 AK1 AK4 AK7 AL14 AM3 AM6 AM9 B3 D2 F1 F4 H3 K2 M1 M4 M7 P3 P6 T2 T5 T7 V1 V4 V7 Y3 Y6 Y7
	AGP_VDDQ	AG30 AJ32 AK27 AL19 AL25 AM23 AM29
	GND	A12 A13 A14 A16 A18 A19 A22 A23 A25 AA1 AA4 AA7 AA8 AA9 AA10 AA11 AA16 AA17 AA22 AA23 AA24 AA25 AA26 AA28 AA30 AB12 AB13 AB14 AB15 AB18 AB19 AB20 AB21 AB26 AB27 AB29 AB31 AB32 AC3 AC6 AC7 AC12 AC13 AC14 AC15 AC18 AC19 AC20 AC21 AC26 AC28 AC30 AC32 AD12 AD13 AD14 AD15 AD18 AD19 AD20 AD21 AD26 AD27 AD29 AD31 AD32 AE2 AE5 AE7 AE12 AE13 AE14 AE15 AE18 AE19 AE20 AE21 AE26 AE28 AE30 AE32 AF10 AF14 AF15 AF16 AF23 AF29 AF31 AG1 AG4 AG8 AG15 AG16 AG24 AH8 AH14 AH22 AH28 AH31 AJ3 AJ6 AJ13 AJ20 AJ26 AK10 AK18 AK24 AK30 AL5 AL8 AL12 AL22 AL28 AM20 AM26 B4 B7 B11 B13 B15 B17 B19 B22 B24 B26 C1 C3 C12 C14 C16 C18 C20 C21 C23 C25 C28 C30 D6 D9 D13 D15 D17 D19 D22 D24 D32 E3 E11 E12 E14 E15 E16 E18 E20 E21 E23 E25 E28 F11 F13 F17 F19 F22 F24 F30 G2 G5 G10 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G23 G24 G25 G26 H7 H12 H13 H14 H15 H18 H19 H20 H21 H28 H31 J1 J4 J7 J12 J13 J14 J15 J18 J19 J20 J21 J26 K12 K13 K14 K15 K18 K19 K20 K21 K29 L3 L6 L7 L12 L13 L14 L15 L18 L19 L20 L21 L26 L28 L31 M8 M9 M10 M11 M16 M17 M22 M23 M24 M25 M26 M28 M30 M32 N2 N5 N8 N9 N10 N11 N16 N17 N22 N23 N24 N25 N26 N27 N29 N31 N32 P8 P9 P10 P11 P16 P17 P22 P23 P24 P25 P26 P28 P30 P32 R1 R4 R7 R8 R9 R10 R11 R16 R17 R22 R23 R24 R25 R26 R28 R29 P31 T12 T13 T14 T15 T18 T19 T20 T21 T26 T28 T30 T32 U3 U6 U7 U12 U13 U14 U15 U18 U19 U20 U21 U26 U27 U29 U31 V8 V9 V10 V11 V16 V17 V22 V23 V24 V25 V26 V28 V30 V32 W2 W5 W7 W8 W9 W10 W11 W16 W17 W22 W23 W24 W25 W26 W27 W29 W31 W32 Y8 Y9 Y10 Y11 Y16 Y17 Y22 Y23 Y24 Y25 Y26 Y28 Y30
PROCESSORS U7H1 U8E1 PAGES 10-13	+3.3V	AE28, AE29
	GND	A11, A21, A27, A29, A5, AA15, AA17, AA2, AA23, AA30, AB1, AB31, AC30, AD31AA9, AB11, AB21, AB27, AB5, AC13, AC19, AC2, AC25, AC7, AD15, AD17, AD23 AD3, AD9, AE11, AE2, AE21, AE27, B15, B17, B2, B23, B28, B9, B30, C1, C31, C13, C19, C25, C29, C7, D11, D30, D2, D21, D27, D28, D5, E1, E15, E17 E23, E29, E9, F13, F19, F2, F25, F28, F7, G1, G31, G25, G27, G29, G3, G5, G7, G9, H2, H24, H26, H28, H4, H6, H8, H30, J1, J31J23, J25, J27, J29 J3, J5, J7, J9, K2, K24, K26, K28, K4, K6, K8, K30, L1, L31, L23, L25, L27, L29, L3, L5, L7, L9, M2, M24, M26, M28, M4, M6, M8, M30, N30, N2, N24, N26 N28, N4, N6, N8, P23, P25, P27, P29, P3, P5, P7, P9, P1, P31, R30, R2, R24, R26, R28, R4, R6, R8, T23, T25, T27, T29, T3, T5, T7, T9, U2, U24 U26, U28, U4, U6, U8, V23, V25, V27, V29, V3, V5, V7, V9, V1, V31, W30, W2, W24, W26, W28, W4, Y13, Y19, Y25, Y5, Y7
	VCC_CORE	A30, AD30, AC31, AB30, AA31, AA1, A14, A18, A2, A24, A28, A8, AA12, AA20, AA26, AAV4, AA6, AB14, AB18, AB2, AB24, AB8, AC10, AC16, AC22, AC3, AC4, AD12, AD2 AD20, AD26, AD6, AE14, AE18, AE24, AE3, AE8, B4, B31, C30, D1, D31B12, B20, B26, B29, B6, C10, C16, C2, C22, C28, C4, D14, D18, D24, D29, D8, E12 E30, F1, F31, G30, H1, H31, E2, E20, E26, E28, E6, E31, F30, F10, F16, F22, F29, F4, G2, G24, G26, G28, G4, G6, G8, H23, H25, H27, H29, H3, H5, H7, H9, J2, J24, J26 J30, K1, K31, L30, M1, M31, J28, J4, J6, J8, K23, K25, K27, K29, K3, K5, K7, K9, L2, L24, L26, L28, L4, L6, L8, M23, M25, M27, M29, M3, M5, M7, M9, N23, N25 N1, N31, P30, R1, R31, T30, N27, N29, N3, N5, N7, N9, P2, P24, P26, P28, P4, P6, P8, R23, R25, R27, R29, R3, R5, R7, R9, T2, T24, T26, T28, T4, T6, T8, T1, T31, U30, U23 U1, U31, V30, W1, W31, Y30, U25, U27, U29, U3, U5, U7, U9, V2, V24, V26, V28, V4, V6, V8, W25, W27, W29, Y1, Y31, Y10, Y16, Y2, Y22
ICH2 U6B3 PAGES 23-24	+3.3V(vcc3_CLK)	E14, E15, E16, E17, E18, F18, G18, H18, J18, P18, R18, R5, T5, U5, V5, V6, V7, V8
	GND	A1, A10, A2, A21, A22, AA1, AA2, AA21, AA22, AB1, AB2, AB21, AB22, B1, B10, B2, B21, B22, B3, B9, C2, C3, C4 C9, D3, D5, D6, D7, D8, D9, E6, E7, E8, E9, J10, J11, J12, J13, J14, J9, K1, K10, K11, K12, K13, K14, K9, L10, L11 L12, L13, L14, L9, M10, M11, M12, M13, M14, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9
	+1.8V	D10, D2, E5, K19, L19, P5, V9
	SB1_8V	H5, J5, V14, V15, V16
	SB5V	V19
	VCC_CORE	D12, D13
P64H U3D1 PAGE 30	+3.3V	E11, E13, E5, E7, E9, F14, F4, H17, J13, J5, L13, M13, M5, N12, N6, P7
	+1.8V	N11, N7, N9, P10, P8
	GND	A1, A17, B12, B6, B9, C3, D16, E12, E14, F13, F16, F2, F5, G13, H10, H8, H9, J10, J8, J9, K10, K2, K8, K9, L5 M16, N13, P12, P2, P6, P9, R15, R16, T10, T13, T7, U1, U17
CKX_SKS U4F2 PAGE 19	+3.3V	4, 10, 16, 22, 27, 29, 36, 38, 43, 49, 56
	GND	1, 7, 13, 19, 24, 32, 33, 37, 40, 46, 53
DRCG'S U4E2 U4F1 PAGE 21	+3.3V	3, 9, 16, 22
	+1.8V	10
	+3.3V(vcc3_CLK)	1
	GND	4, 5, 8, 13, 17, 21
HECETA4 U7B2 PAGE 34	+3.3V	4, 13
	+5V	12
	SB2.5V	14
	VCC_CORE	15
	GND	3
74HCT4051 U3J2 PAGE 55	+5V	16
	GND	7
HCT4052 U4E2 PAGE 56	+5V	16
	GND	8
74F08 U9C1 PAGE 41-43	+5V	14
	GND	7
SIO LPC47B27X U7C1 PAGE 37	+3.3V	53, 65, 93
	+5V	44
	STANDBY3V	18
	GND	7, 31, 40, 60, 76
AD1881 U2A1 PAGE 44	+3.3V	1, 9
	AUD_VCC	25, 38
	GND	4, 7, 26, 42
GLUECHIP3 U1E1 PAGE 35	SB5V	2
	STANDBY3V	3
	GND	42 17
74HC682 U5H1 PAGE 56	+3.3V	20
	GND	10
82562EM U6B1 PAGE 50	STANDBY3V	1, 7, 25, 2, 9, 12, 14, 17, 19, 23, 36, 40
	GND	3, 6, 8, 13, 18, 20, 22, 24, 33, 38, 48
FWH U1F1 PAGE 36	+3.3V	25, 27, 32
	GND	16, 26, 28
QS3126 U1C1 PAGE49	+5V	16
	GND	8
74F07 U3J1 PAGE 49	SB5V	14
	GND	7
HIP6601 U2F1 PAGE 54	+12V	7
	GND	4
HIP6301 U2E1 PAGE 54	+5V	20
	GND	9
AT24C08 U6F1 PAGE 56	+3.3V	8
	GND	4
74LVC00 U5G1 PAGE 56	+3.3V	14
	GND	7
74LVC08 U5A1 PAGE 34	+3.3V	7
	GND	14

DEVICE TABLE

DRAWING

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: DEVICE TABLE

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INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

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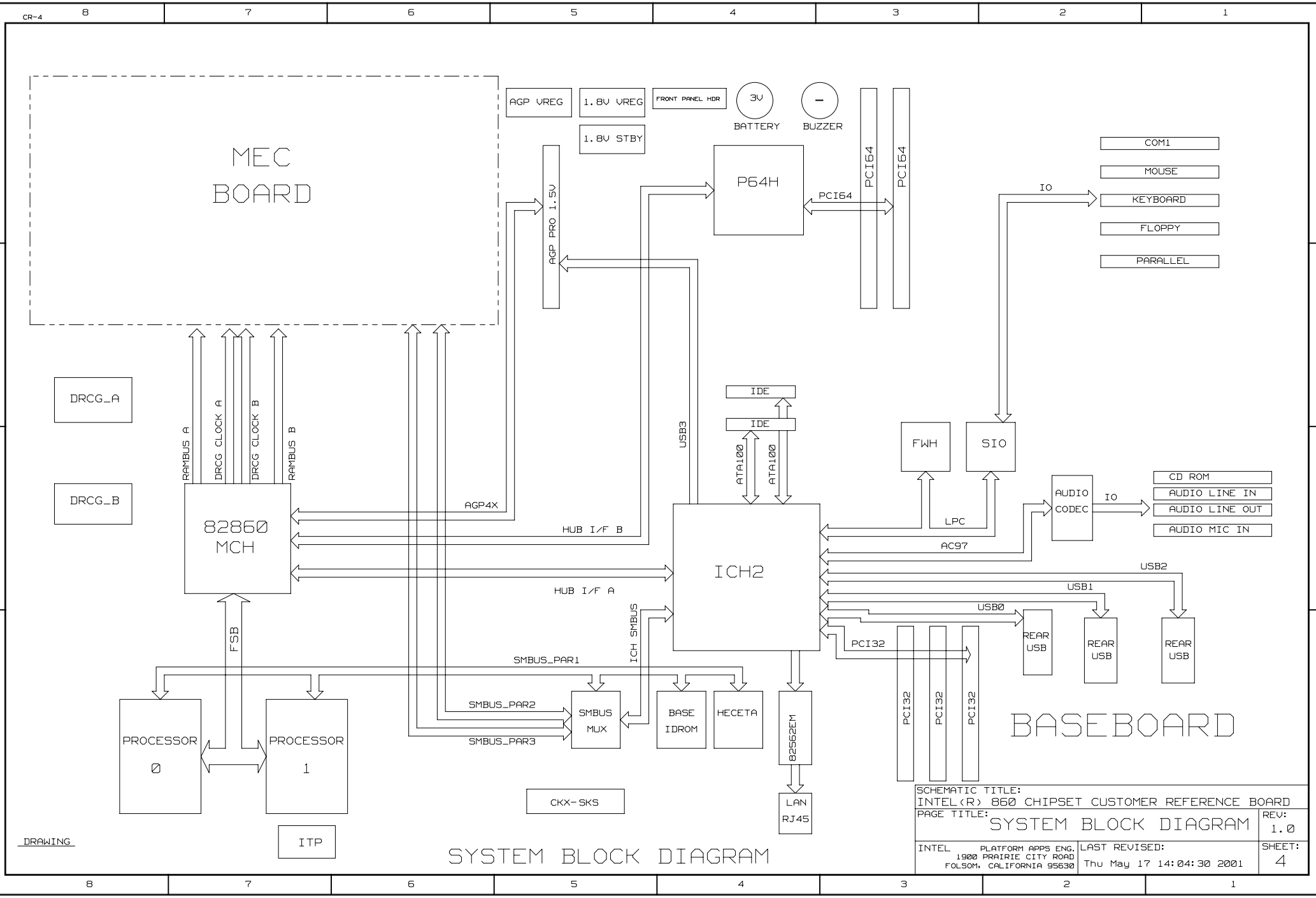
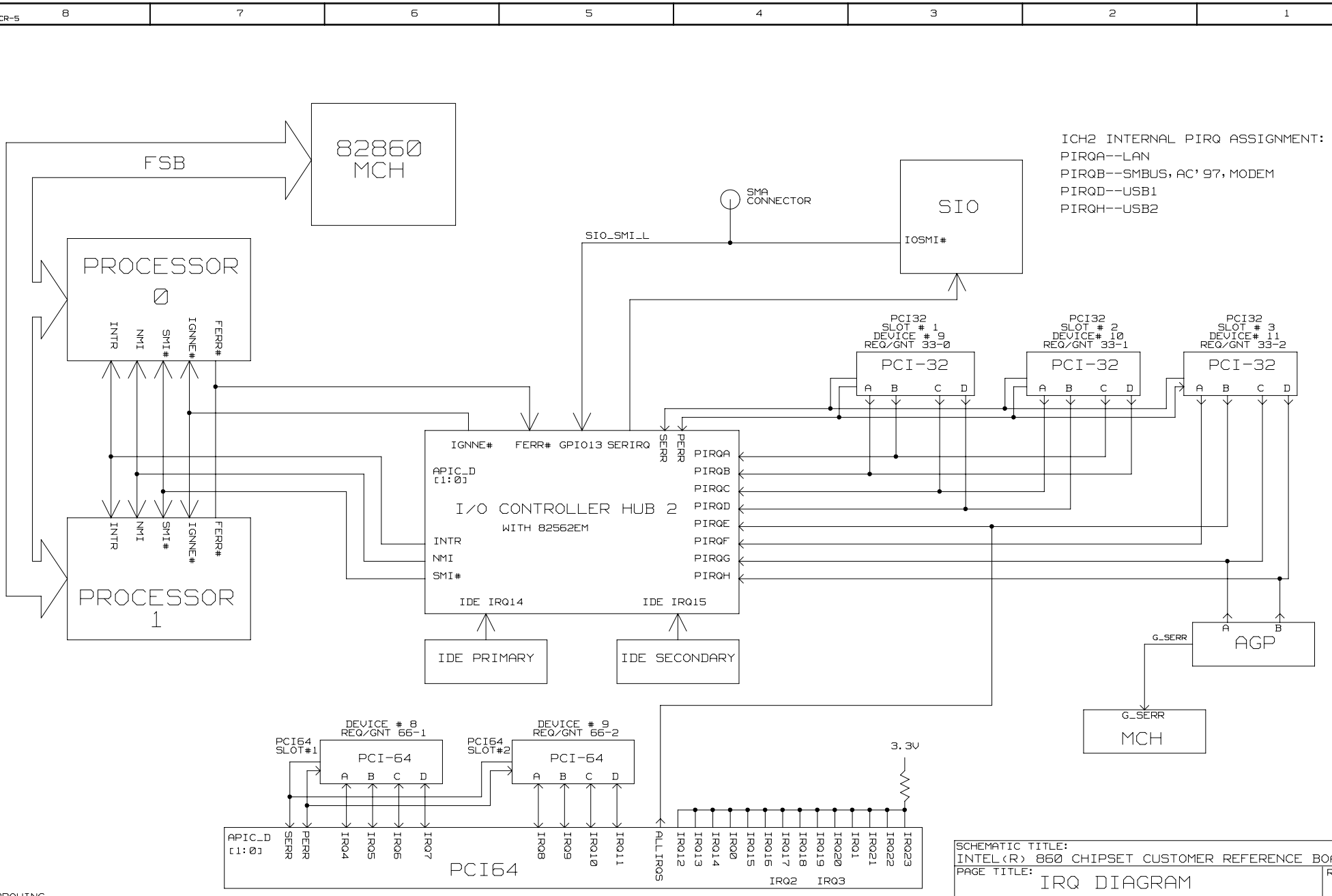

CR-4
MEC BOARD
AGP VREG
1.8V VREG
1.8V STBY
FRONT PANEL HDR
3V
BATTERY
BUZZER
P64H
PCI64
PCI64
PCI64
AGP PRO 1.5V
COM1
MOUSE
KEYBOARD
FLOPPY
PARALLEL
IO
DRCG_A
DRCG_B
RAMBUS A
DRCG CLOCK A
DRCG CLOCK B
RAMBUS B
82860 MCH
AGP4X
HUB I/F B
HUB I/F A
USB3
IDE
IDE
ATA100
ATA100
FWH
SIO
LPC
AUDIO CODEC
IO
CD ROM
AUDIO LINE IN
AUDIO LINE OUT
AUDIO MIC IN
AC97
ICH2
USB2
USB1
USB0
REAR USB
REAR USB
REAR USB
PCI32
PCI32
PCI32
PCI32
FSB
ICH SMBUS
SMBUS_PAR1
SMBUS_PAR2
SMBUS_PAR3
SMBUS MUX
BASE IDROM
HECETA
82562EM
LAN RJ45
PROCESSOR 0
PROCESSOR 1
ITP
CKX-SKS
BASEBOARD
DRAWING
SYSTEM BLOCK DIAGRAM
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
SYSTEM BLOCK DIAGRAM
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:04:30 2001
SHEET:
4

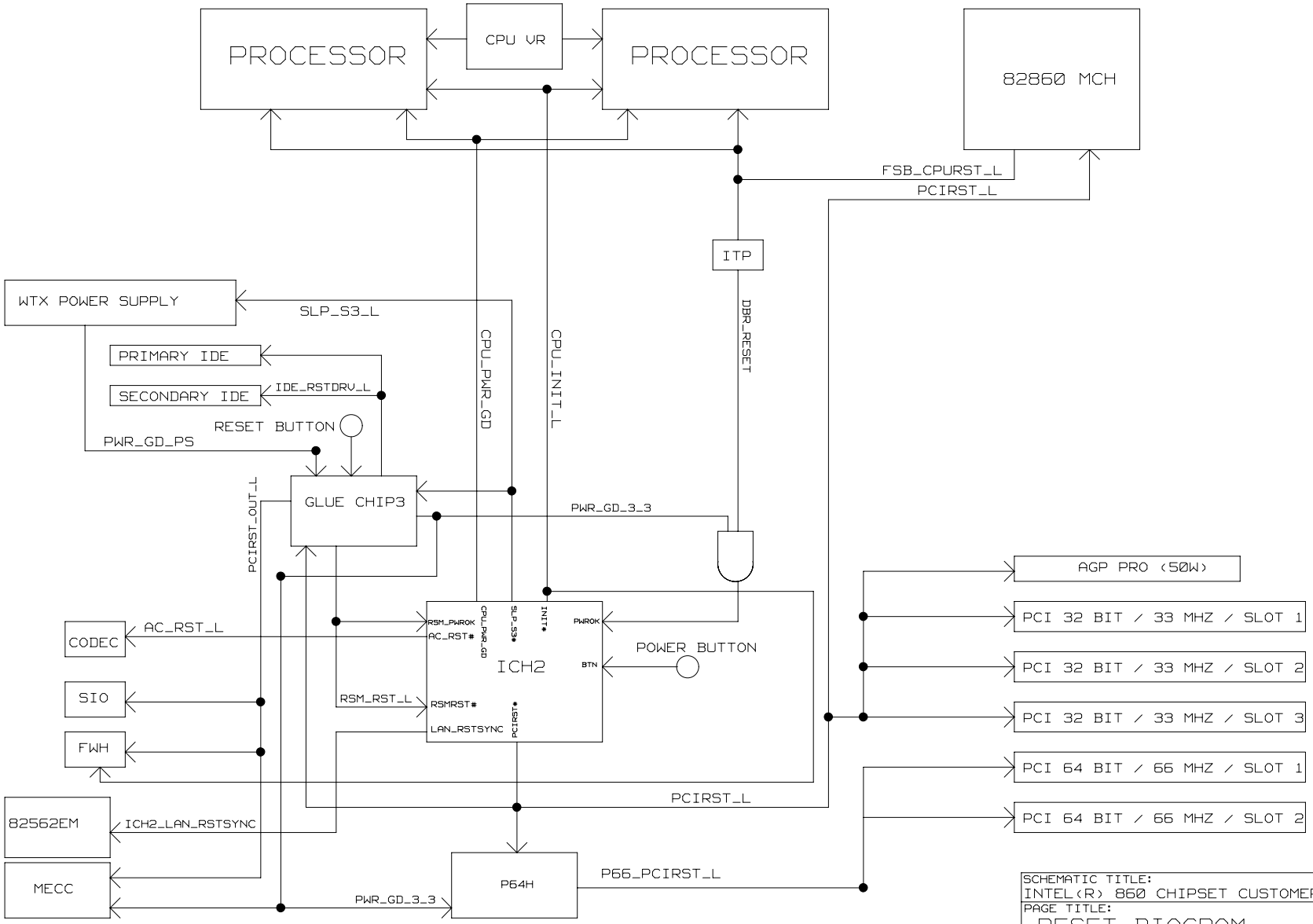


IRQ DIAGRAM

DRAWING

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: IRQ DIAGRAM	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:04:26 2001
	SHEET: 5

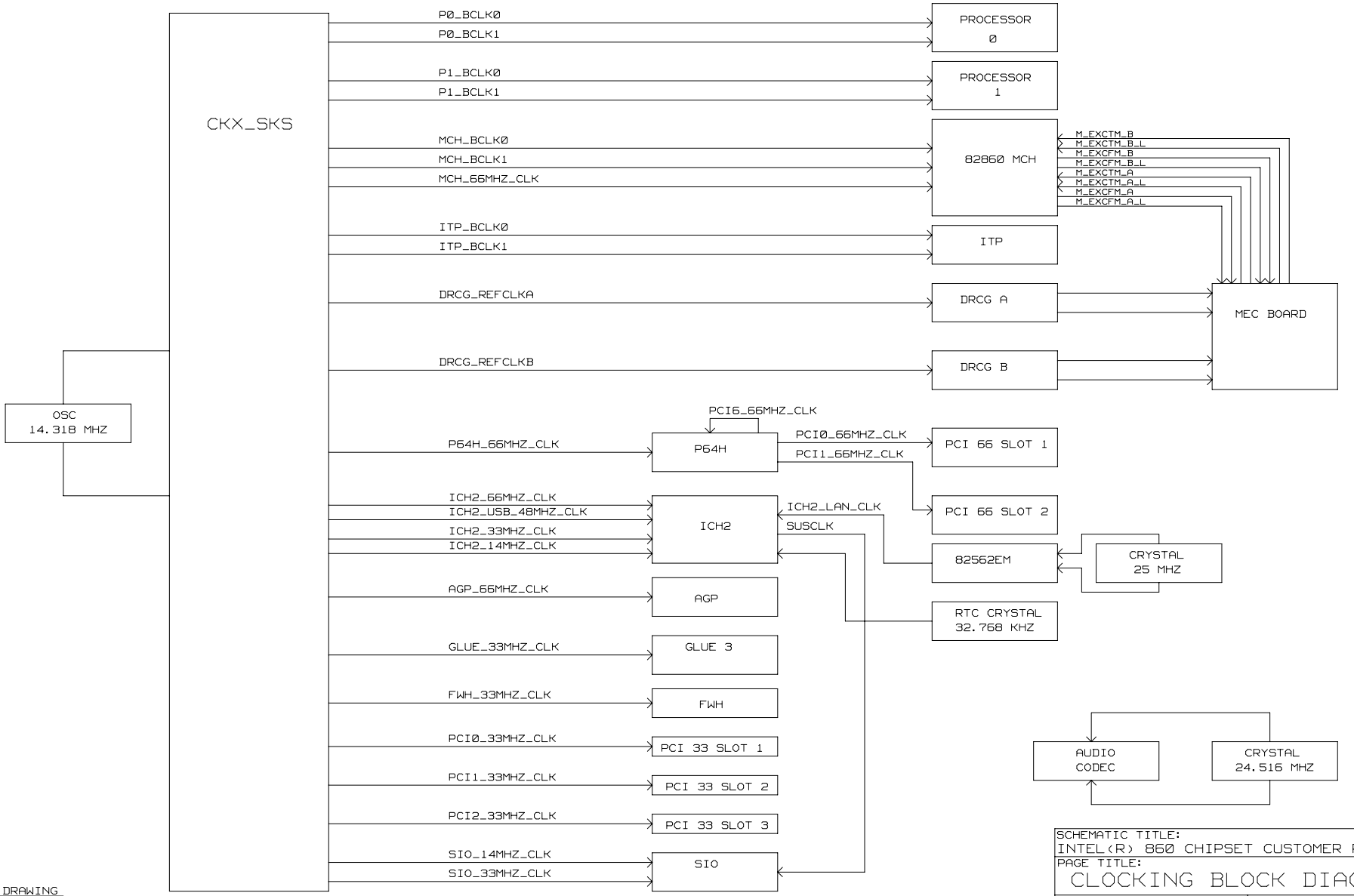
CR-6



DRAWING

RESET DIAGRAM

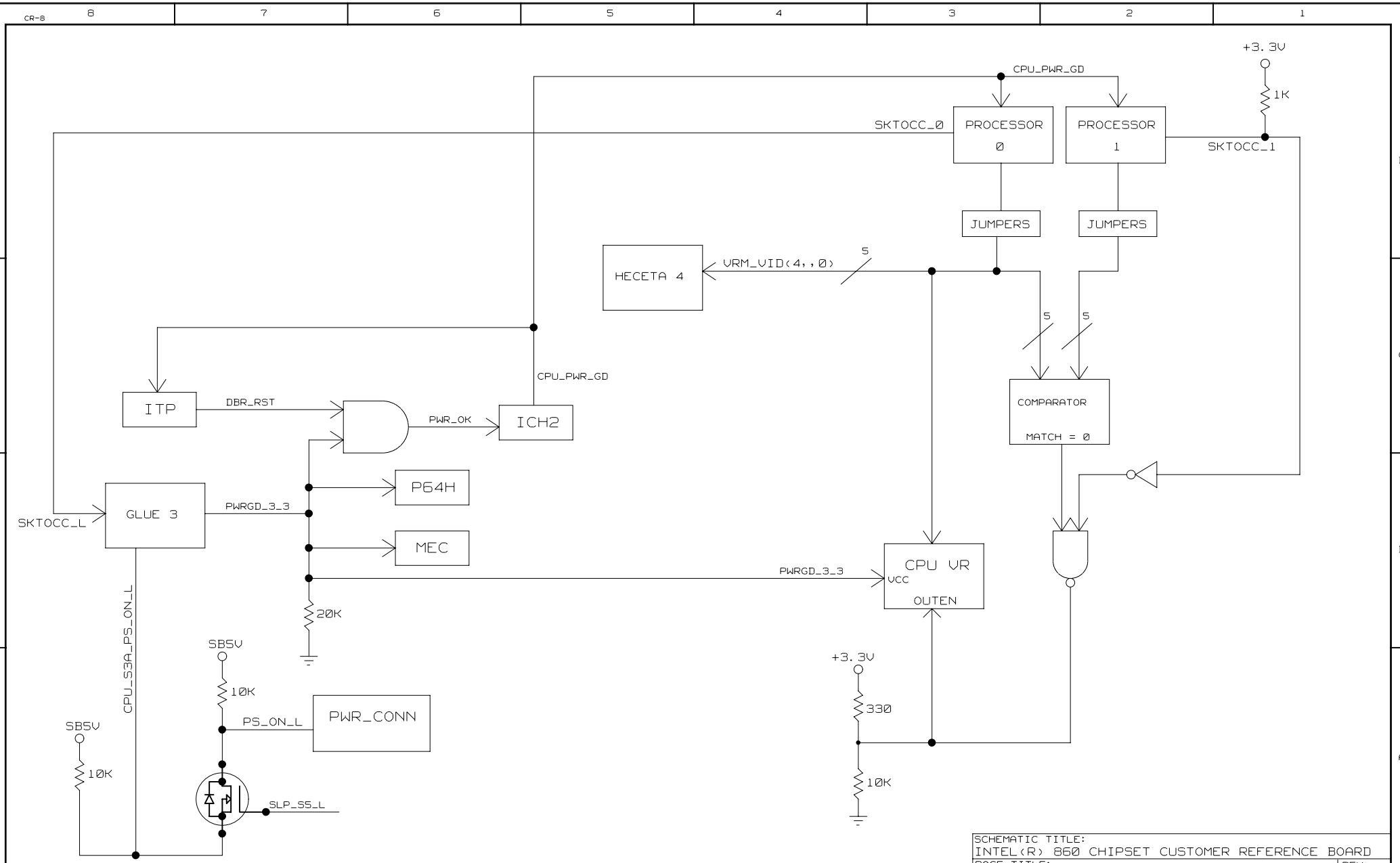
SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: RESET DIAGRAM	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:04:22 2001
	SHEET: 6



DRAWING

CLOCKING BLOCK DIAGRAM

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: CLOCKING BLOCK DIAGRAM	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Fri May 18 13:50:54 2001
	SHEET: 7



DRAWING

POWER GOOD AND CPU VR BLOCK DIAGRAM

SCHEMATIC TITLE:	INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:	PWR GD AND CPU VR BLOCK DIAGRAM
REV:	1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	
LAST REVISED:	Thu May 17 14:04:13 2001
SHEET:	8

CR-9

SMBUS PARTITION1

PARTITION SELECT = 10, 11

CPU0

THERMAL SENSOR: 30
IDROM SMB_ADDR: A0

CPU1

THERMAL SENSOR: 32
IDROM SMB_ADDR: A2

HECETA 4

SMB_ADDR: 5A

BASEBOARD IDROM

SMB_ADDR: A8-AE

ICH2

WITH 82562EM

ICH2 LAN
SMB_ADDR: C8

ICH_SMBUS

SMBUS_CTRL_0

SMBUS_CTRL_1

MUX

SMBUS_PAR1

SMBUS_PAR2

SMBUS PARTITION2

PARTITION SELECT = 00

RIMM* 1

SMB_ADDR: A0

RIMM* 2

SMB_ADDR: A2

RIMM* 3

SMB_ADDR: A4

RIMM* 4

SMB_ADDR: A6

RIMM* 5

SMB_ADDR: A8

RIMM* 6

SMB_ADDR: AA

RIMM* 7

SMB_ADDR: AC

RIMM* 8

SMB_ADDR: AE

S0	S1	SMBUS PARTITION
0	0	PAR2
0	1	PAR3
1	X	PAR1

DRAWING

SMBUS ADDRESS PARTITION

SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD

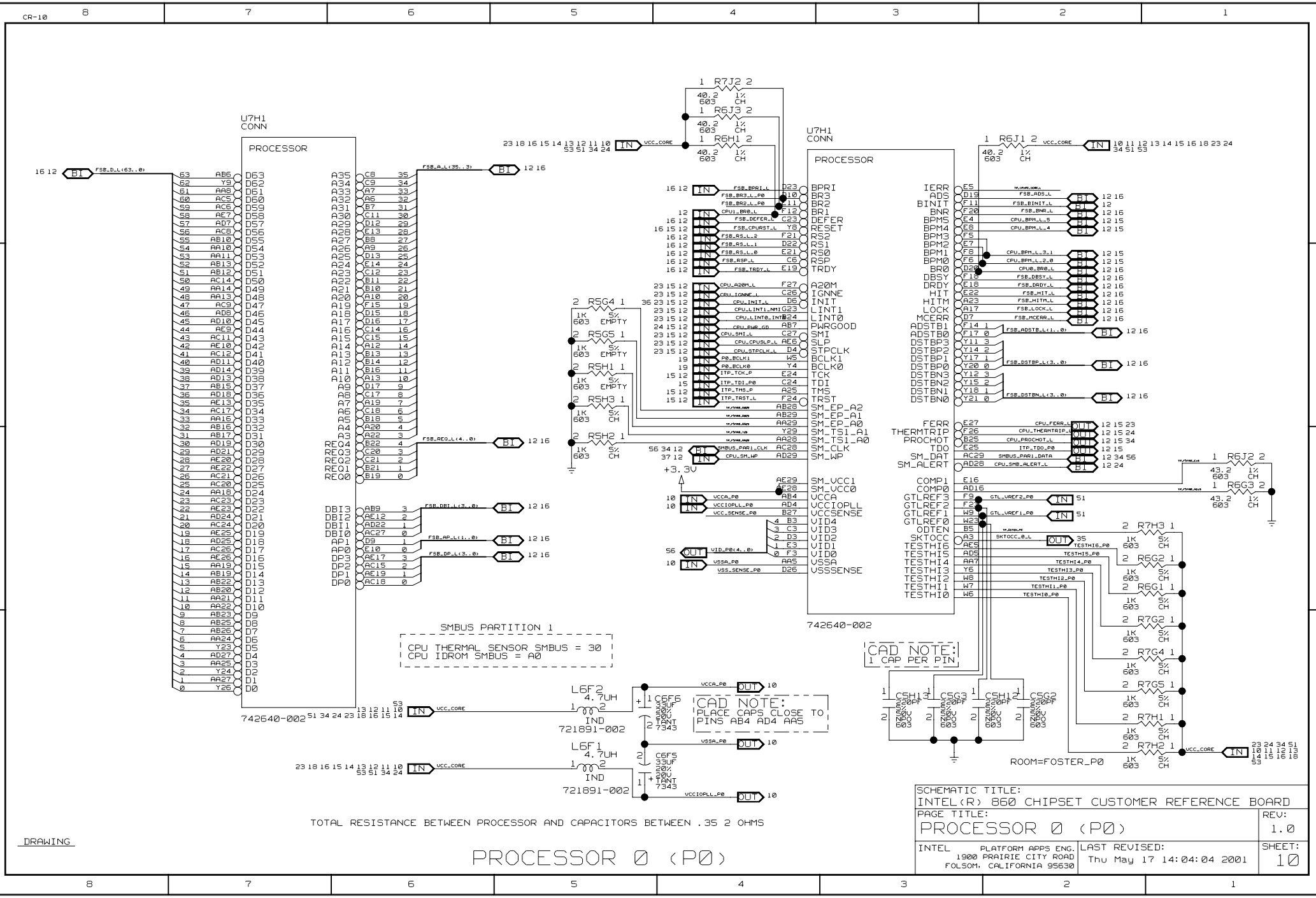
PAGE TITLE:
SMBUS ADDRESS PARTITION

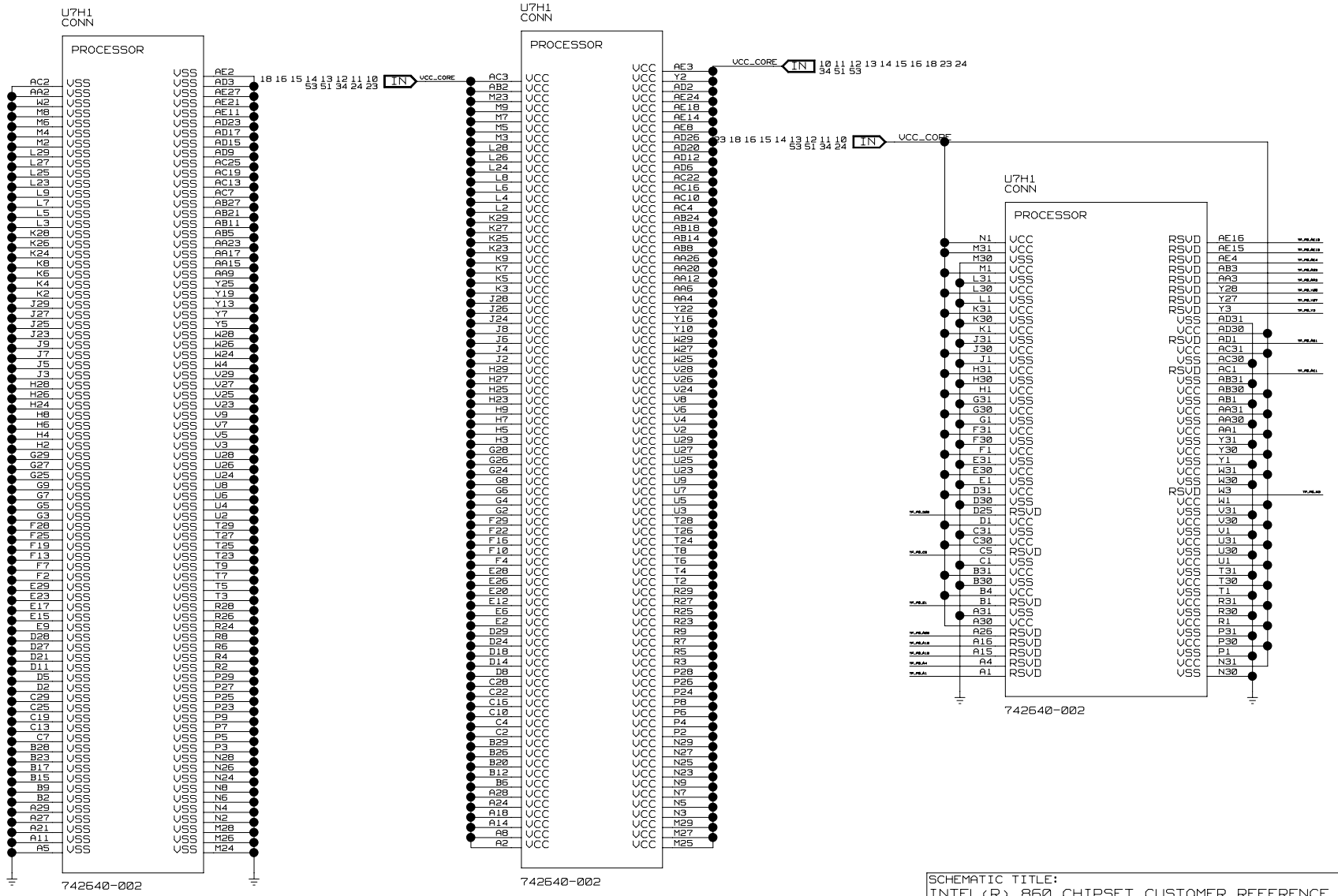
REV: 1.0

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED:
Fri May 18 13:54:44 2001

SHEET: 9

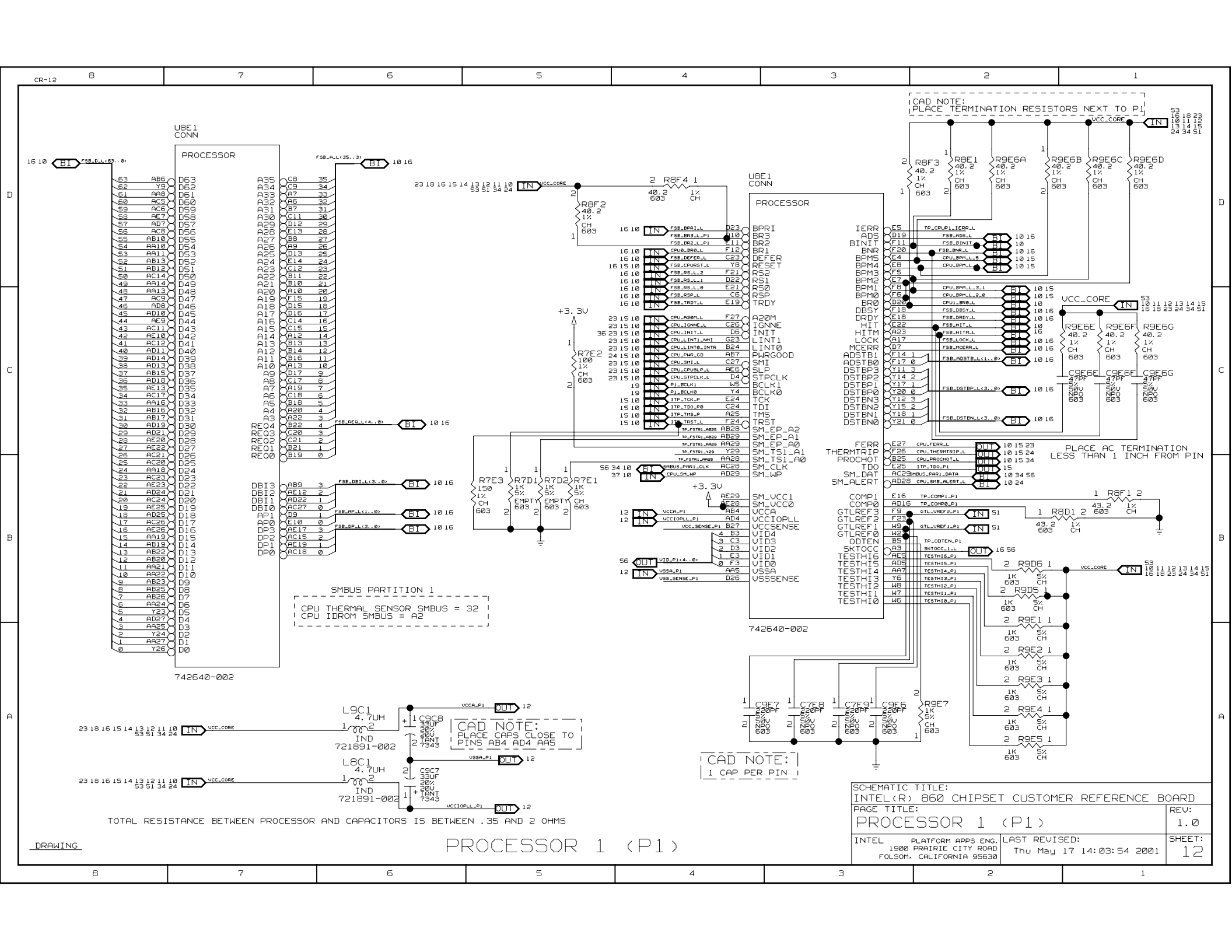

U7H1
CONN
PROCESSOR
742640-002
SMBUS PARTITION 1
CPU THERMAL SENSOR SMBUS = 30
CPU IDROM SMBUS = A0
CAD NOTE:
PLACE CAPS CLOSE TO
PINS AB4 AD4 AA5
CAD NOTE:
1 CAP PER PIN
ROOM=FOSTER_P0
TOTAL RESISTANCE BETWEEN PROCESSOR AND CAPACITORS BETWEEN .35 2 OHMS
DRAWING
PROCESSOR 0 (P0)
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
PROCESSOR 0 (P0)
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:04:04 2001
SHEET:
10

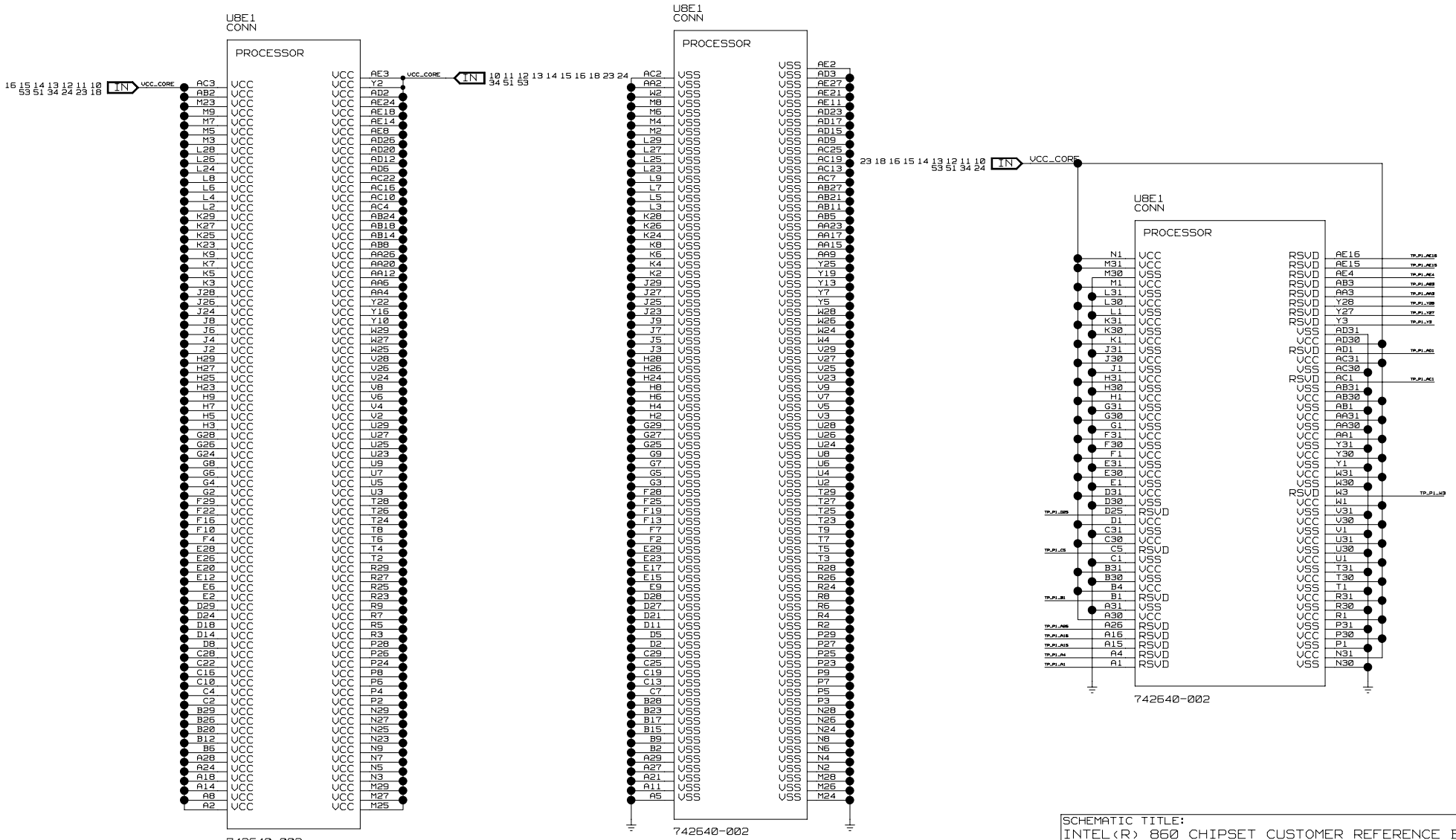


DRAWING

PROCESSOR 0 / POWER GROUND & RESERVED

SCHEMATIC TITLE:	INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:	PROCESSOR 0
REV:	1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	
LAST REVISED:	Thu May 17 14:03:59 2001
SHEET:	11

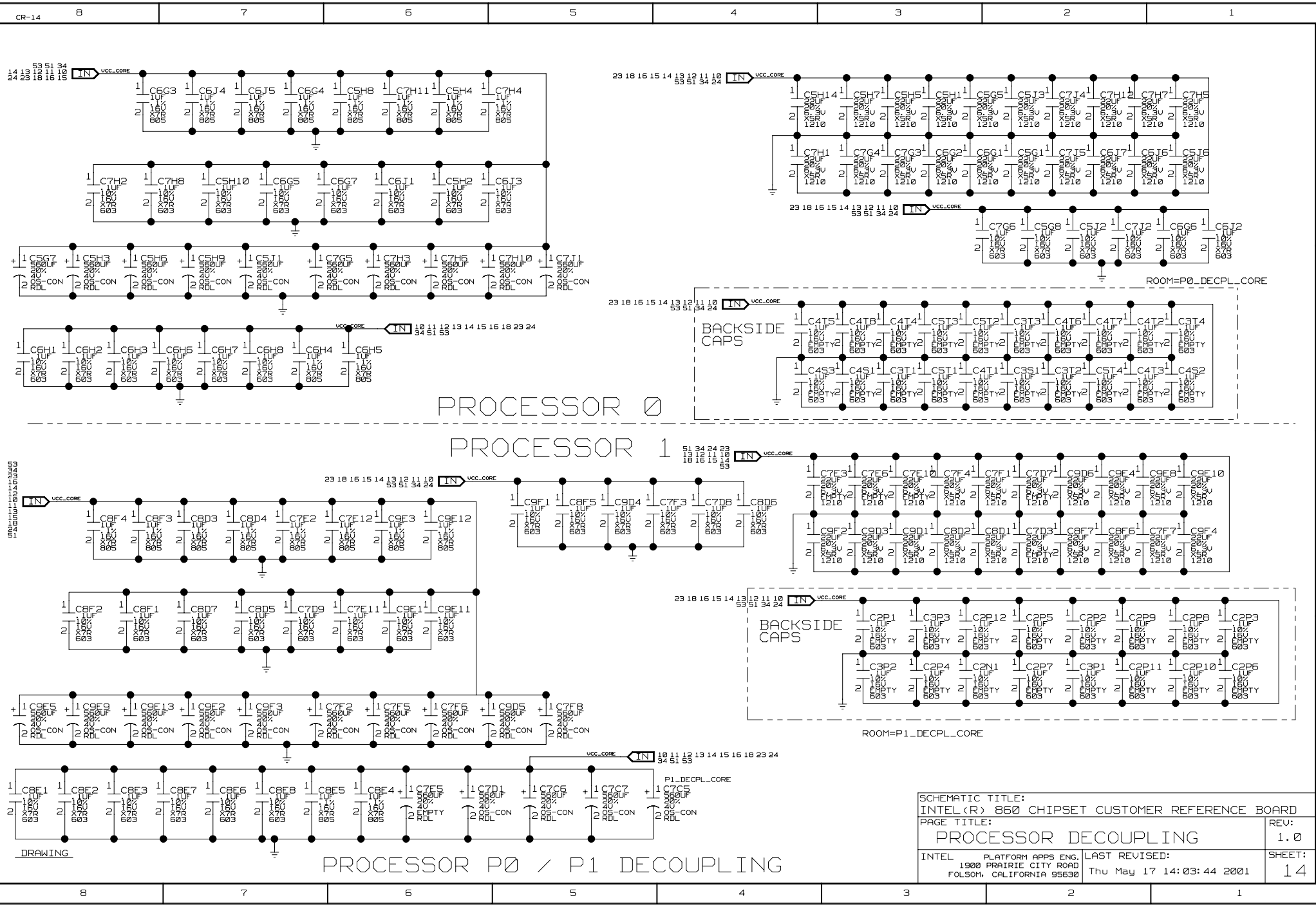

U8E1
CONN
PROCESSOR
742640-002
SMBUS PARTITION 1
CPU THERMAL SENSOR SMBUS = 32
CPU IDROM SMBUS = A2
CAD NOTE:
PLACE TERMINATION RESISTORS NEXT TO P1
PLACE AC TERMINATION
LESS THAN 1 INCH FROM PIN
CAD NOTE:
PLACE CAPS CLOSE TO
PINS AB4 AD4 AA5
CAD NOTE:
1 CAP PER PIN
TOTAL RESISTANCE BETWEEN PROCESSOR AND CAPACITORS IS BETWEEN .35 AND 2 OHMS
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
PROCESSOR 1 (P1)
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:03:54 2001
SHEET:
12
DRAWING
PROCESSOR 1 (P1)



DRAWING

PROCESSOR 1 / POWER GROUND & RESERVED

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PROCESSOR 1		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:03:49 2001	SHEET: 13



SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD

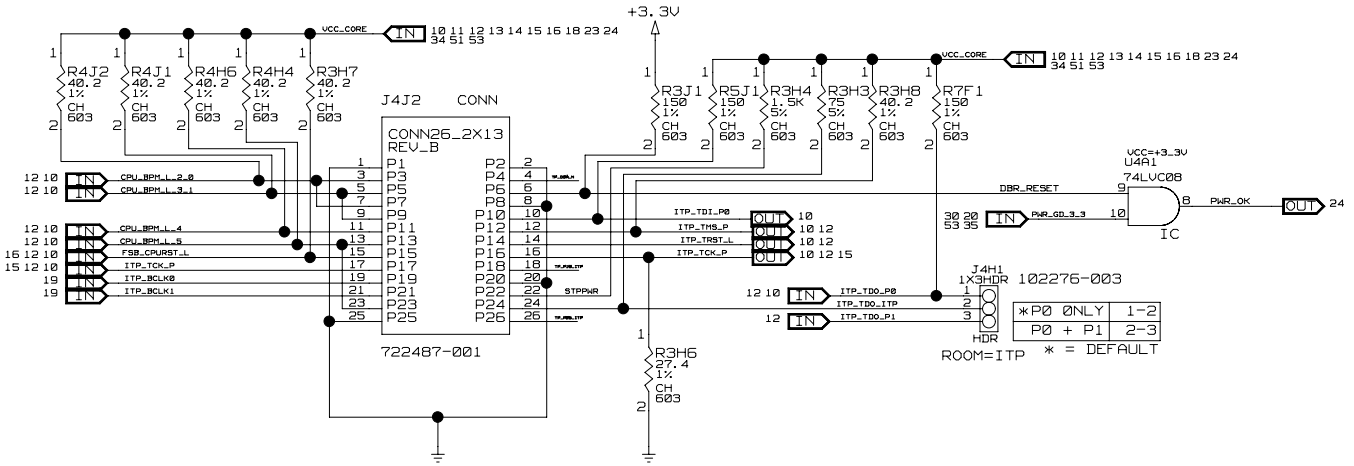
PAGE TITLE:
PROCESSOR DECOUPLING

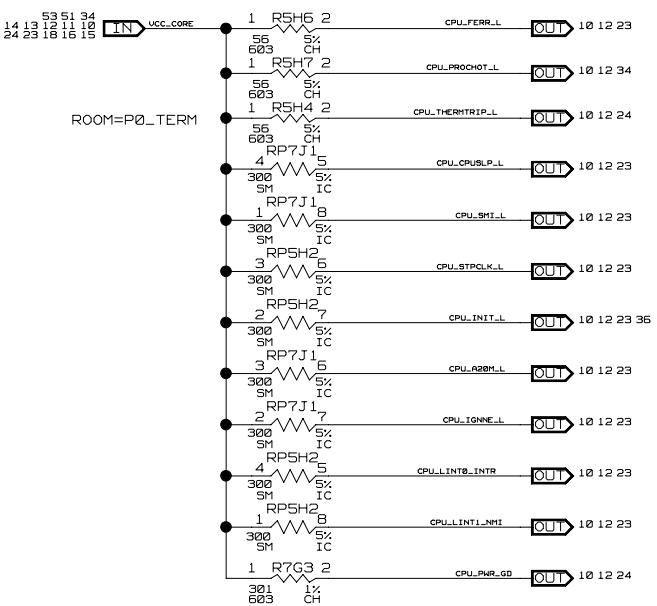
REV:
1.0

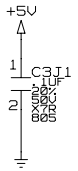
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

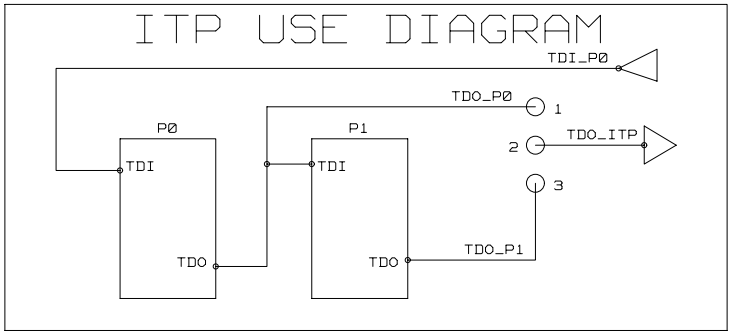
LAST REVISED:
Thu May 17 14:03:44 2001

SHEET:
14







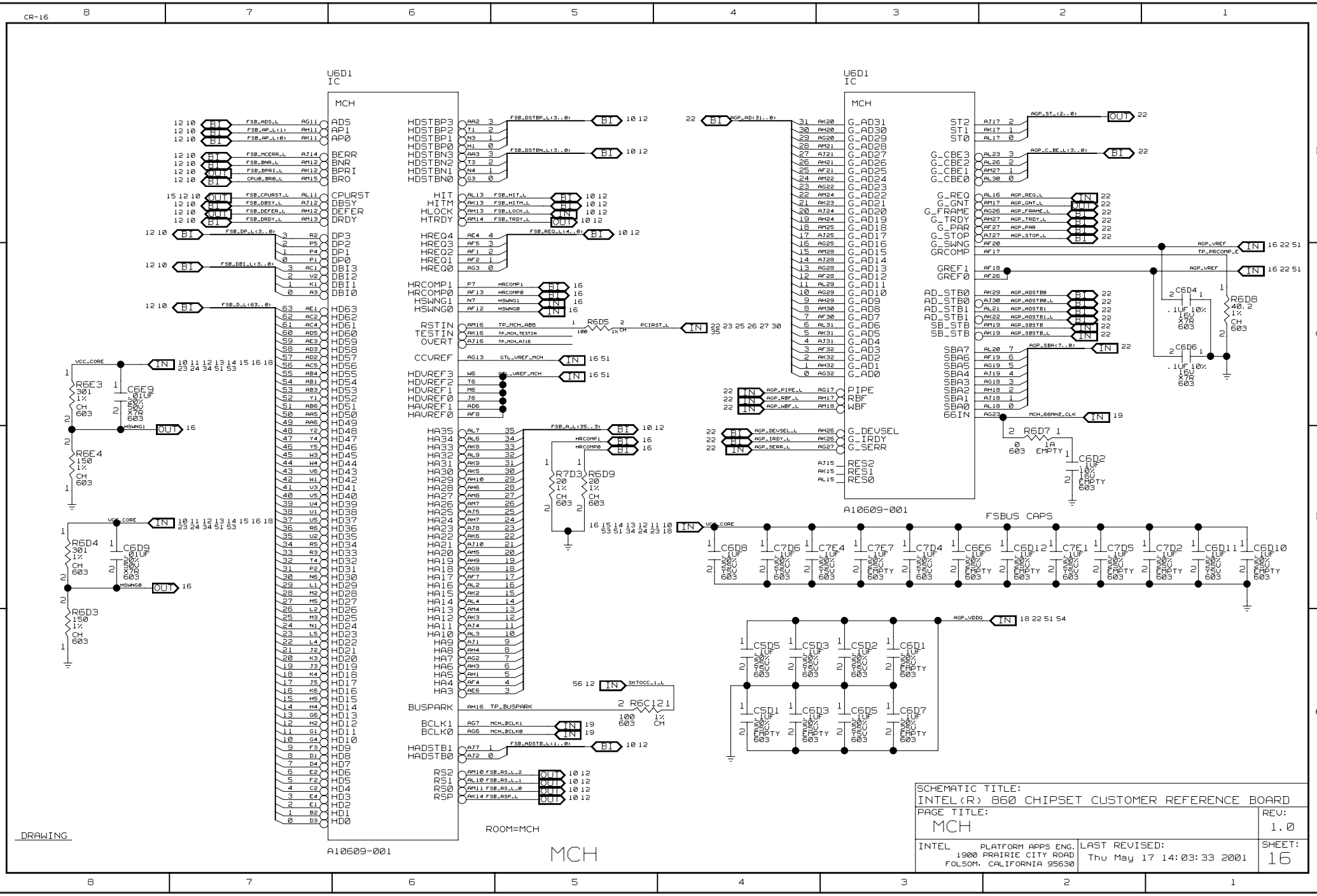


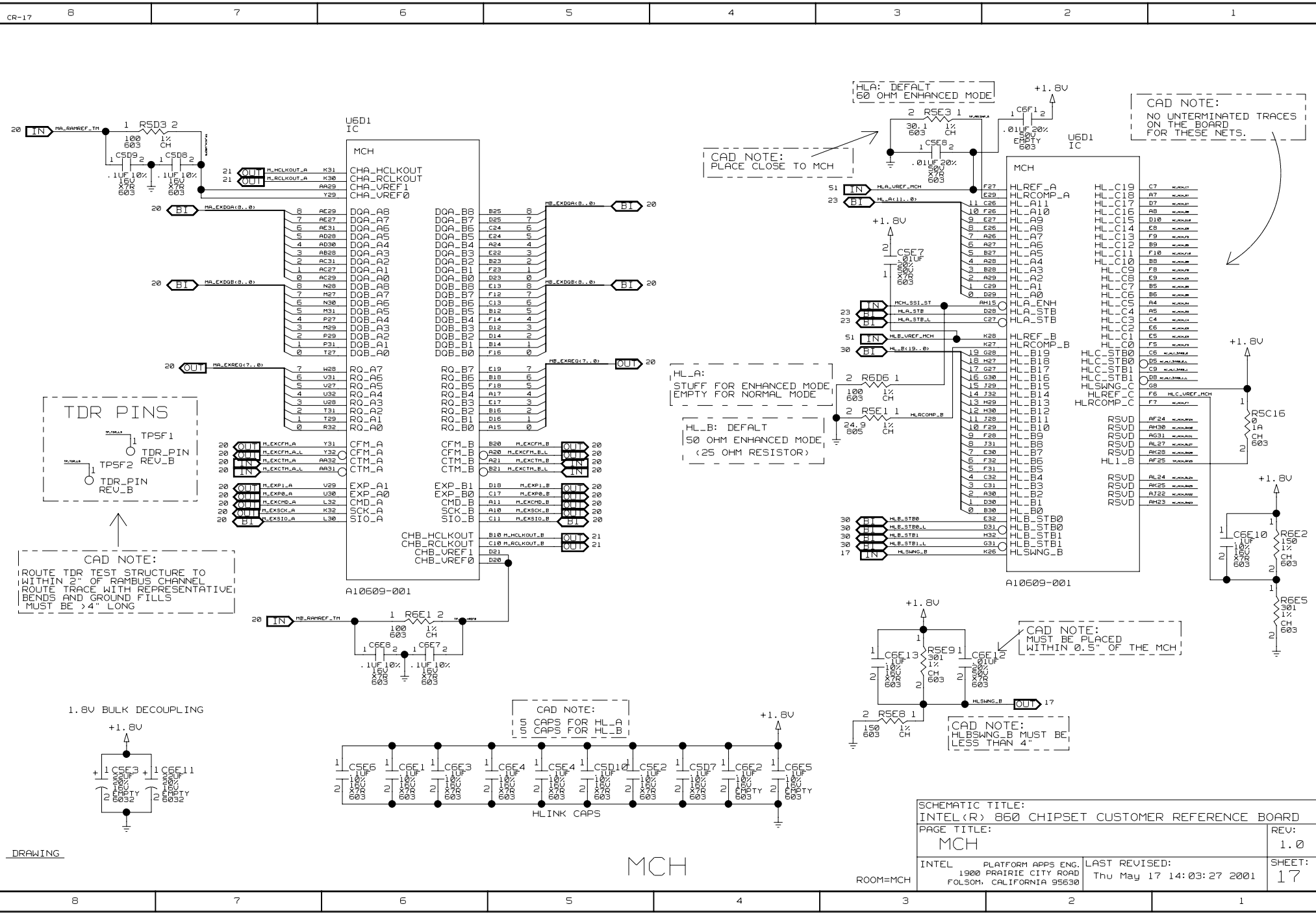
DRAWING

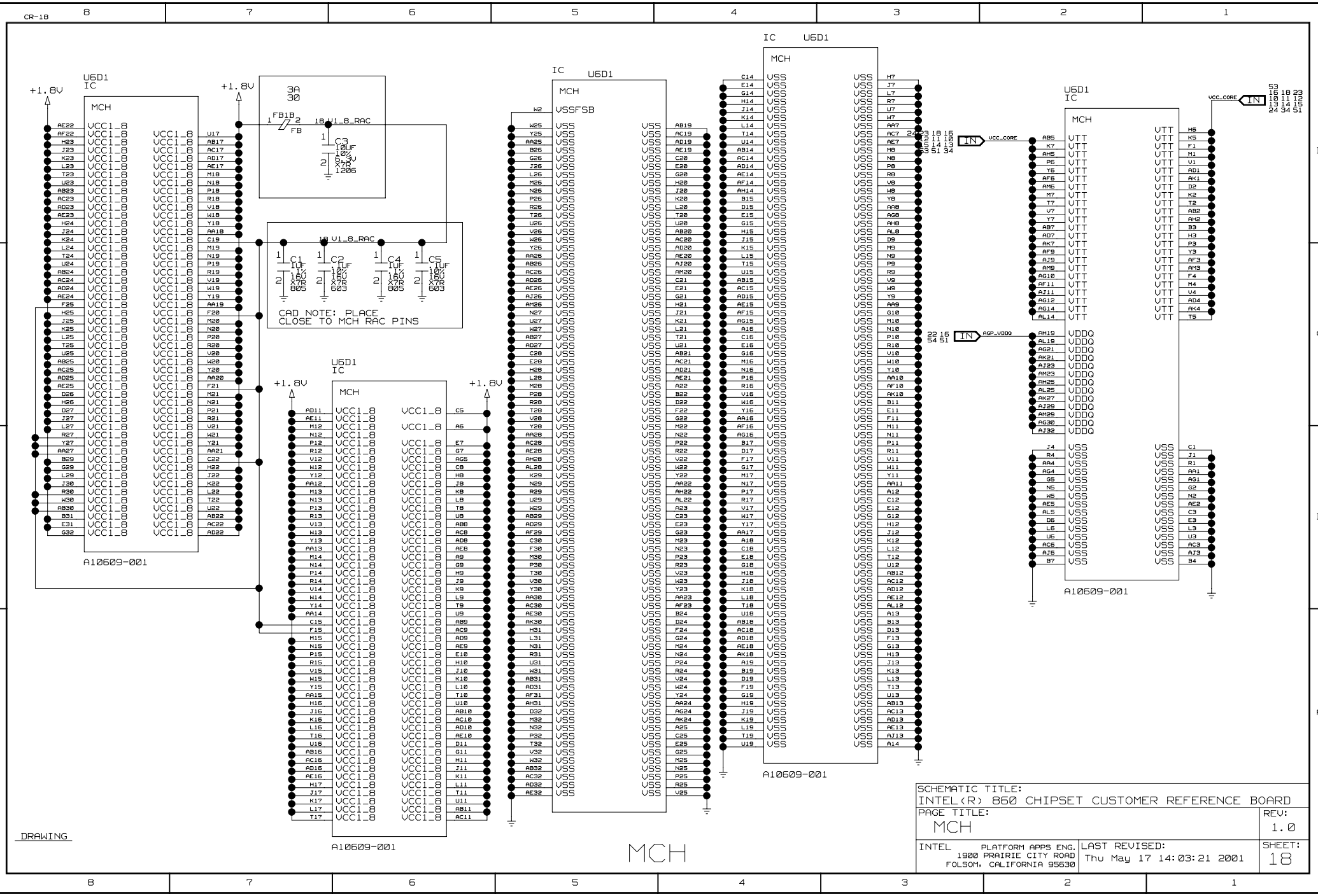
ITP

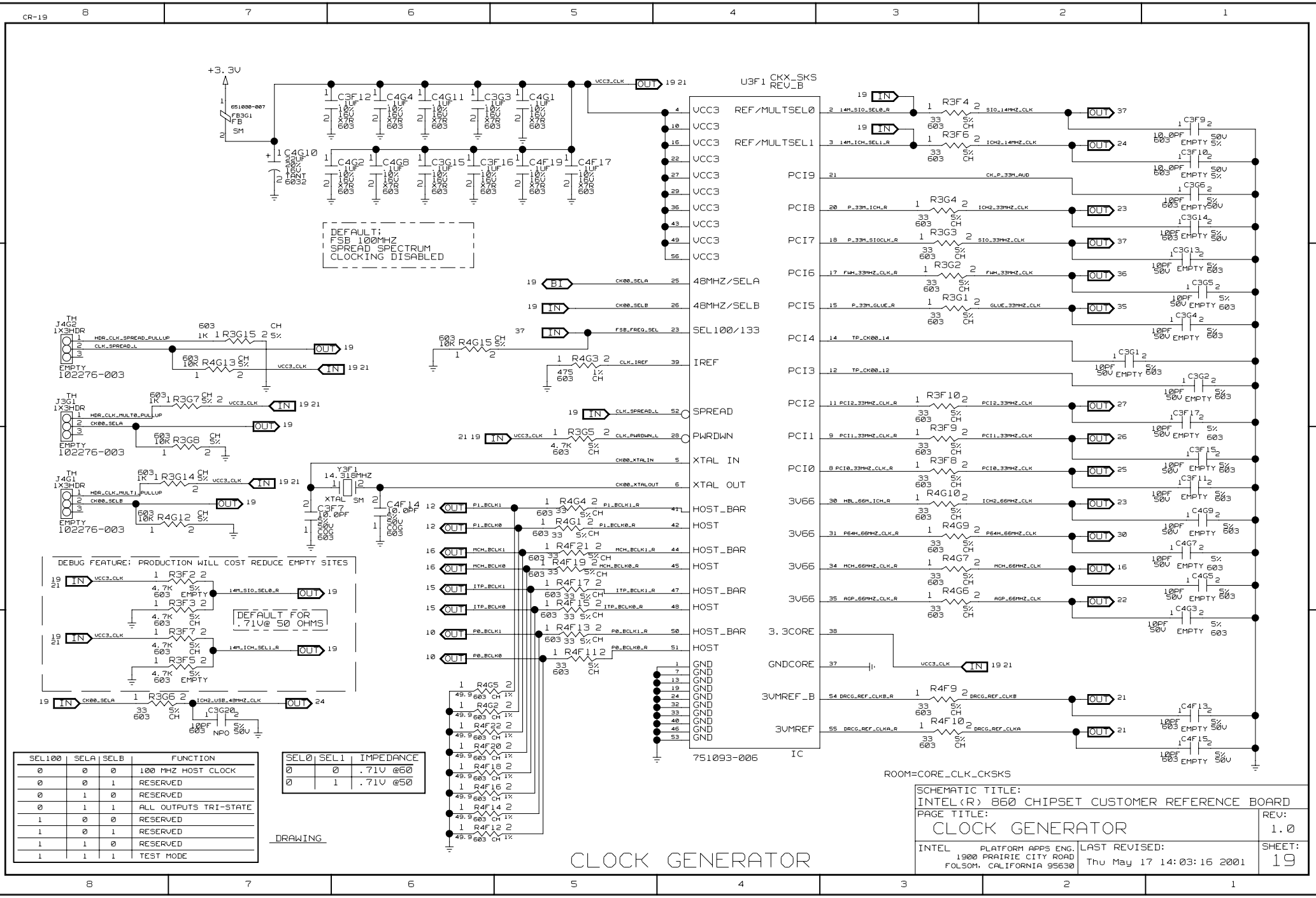
ROOM=ITP

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: ITP	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:03:39 2001
	SHEET: 15


U6D1
IC
MCH
A10609-001
ROOM=MCH
MCH
DRAWING
FSBUS CAPS
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
MCH
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:03:33 2001
SHEET:
16

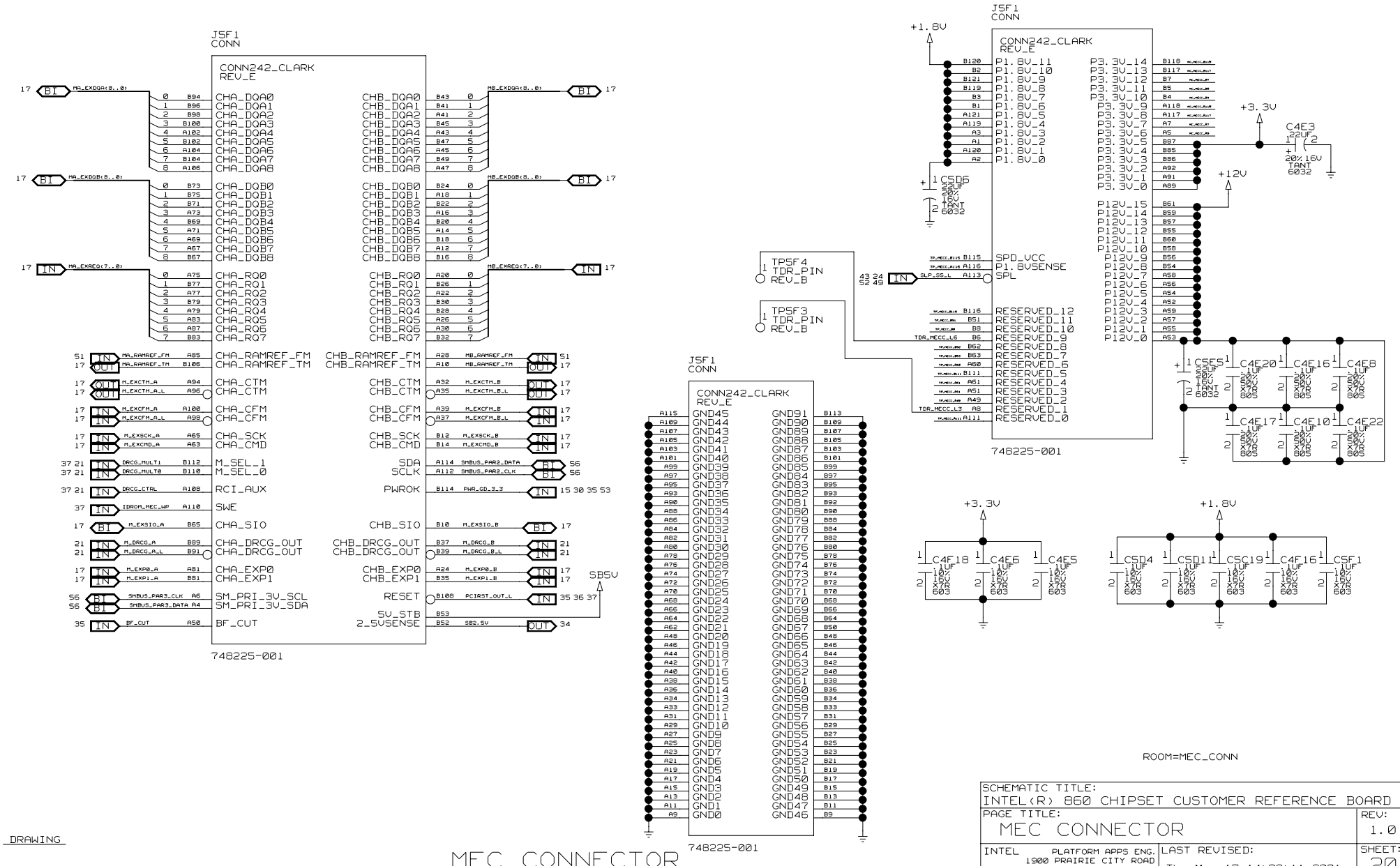

CR-17
U6D1
IC
MCH
A10609-001
TDR PINS
TPSF1
TDR_PIN
REV_B
TPSF2
TDR_PIN
REV_B
CAD NOTE:
ROUTE TDR TEST STRUCTURE TO WITHIN 2" OF RAMBUS CHANNEL
ROUTE TRACE WITH REPRESENTATIVE BENDS AND GROUND FILLS
MUST BE >4" LONG
HLA: DEFALT
60 OHM ENHANCED MODE
CAD NOTE:
PLACE CLOSE TO MCH
CAD NOTE:
NO UNTERMINATED TRACES
ON THE BOARD
FOR THESE NETS.
HL_A:
STUFF FOR ENHANCED MODE
EMPTY FOR NORMAL MODE
HL_B: DEFALT
50 OHM ENHANCED MODE
(25 OHM RESISTOR)
CAD NOTE:
MUST BE PLACED
WITHIN 0.5" OF THE MCH
CAD NOTE:
HLBSWNG_B MUST BE
LESS THAN 4"
CAD NOTE:
5 CAPS FOR HL_A
5 CAPS FOR HL_B
HLINK CAPS
1.8V BULK DECOUPLING
+1.8V
DRAWING
MCH
ROOM=MCH
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
MCH
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:03:27 2001
SHEET:
17


CR-1B
U6D1
IC
MCH
+1.8V
3A
30
FB1B
FB
1B_V1_8_RAC
C3
10UF
10%
6.3V
X7R
1206
C1
1UF
16V
X5R
805
C2
10UF
10%
6.3V
X5R
603
C4
1UF
16V
X5R
805
C5
10UF
10%
6.3V
X5R
603
CAD NOTE: PLACE
CLOSE TO MCH RAC PINS
A10609-001
VSSFSB
VSS
VCC1_8
VTT
VDDQ
VCC_CORE
AGP_VDDQ
IN
MCH
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
MCH
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:03:21 2001
SHEET:
18
DRAWING



SEL100	SELA	SELB	FUNCTION
0	0	0	100 MHZ HOST CLOCK
0	0	1	RESERVED
0	1	0	RESERVED
0	1	1	ALL OUTPUTS TRI-STATE
1	0	0	RESERVED
1	0	1	RESERVED
1	1	0	RESERVED
1	1	1	TEST MODE

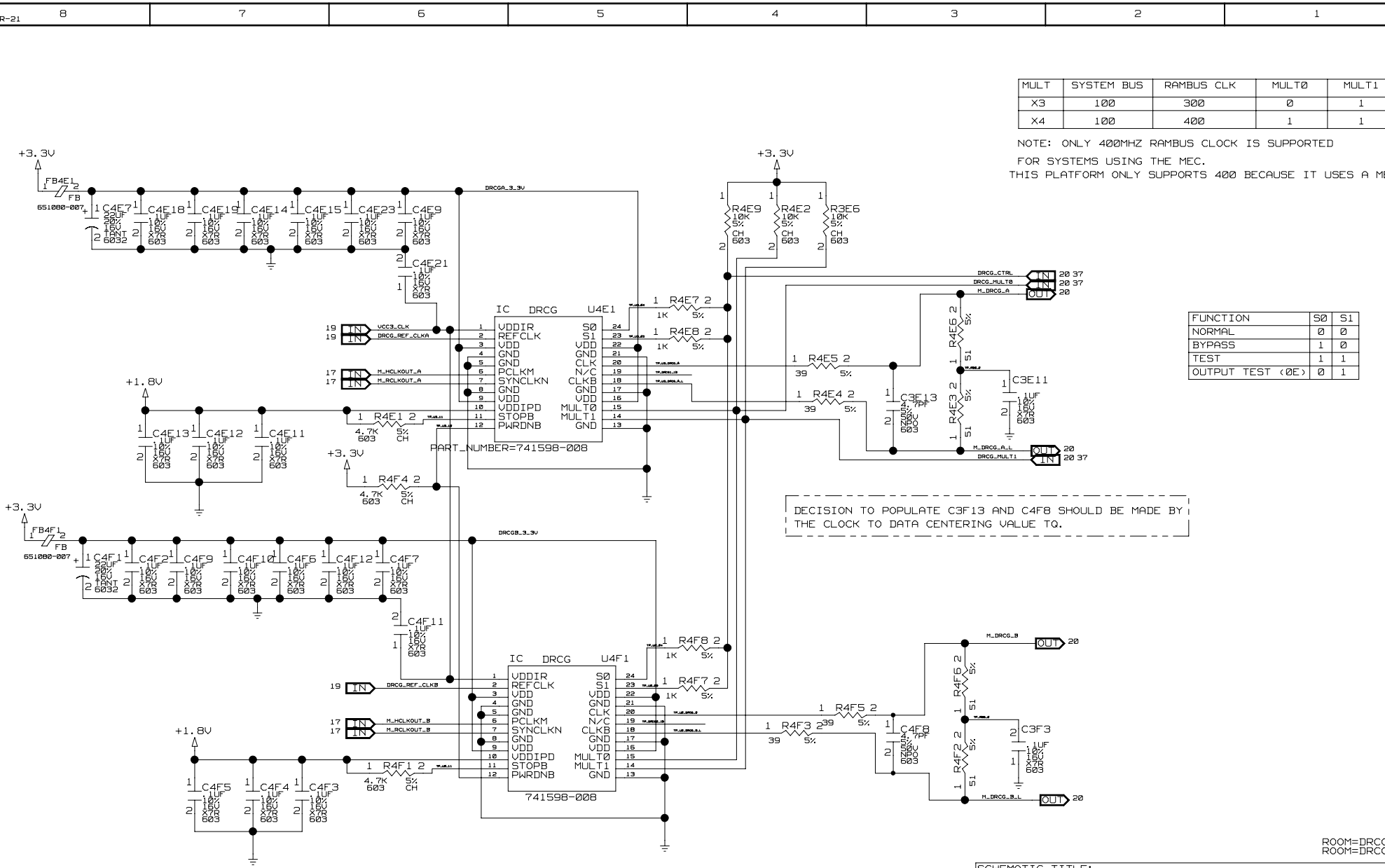
SEL0	SEL1	IMPEDANCE
0	0	.71V @60
0	1	.71V @50

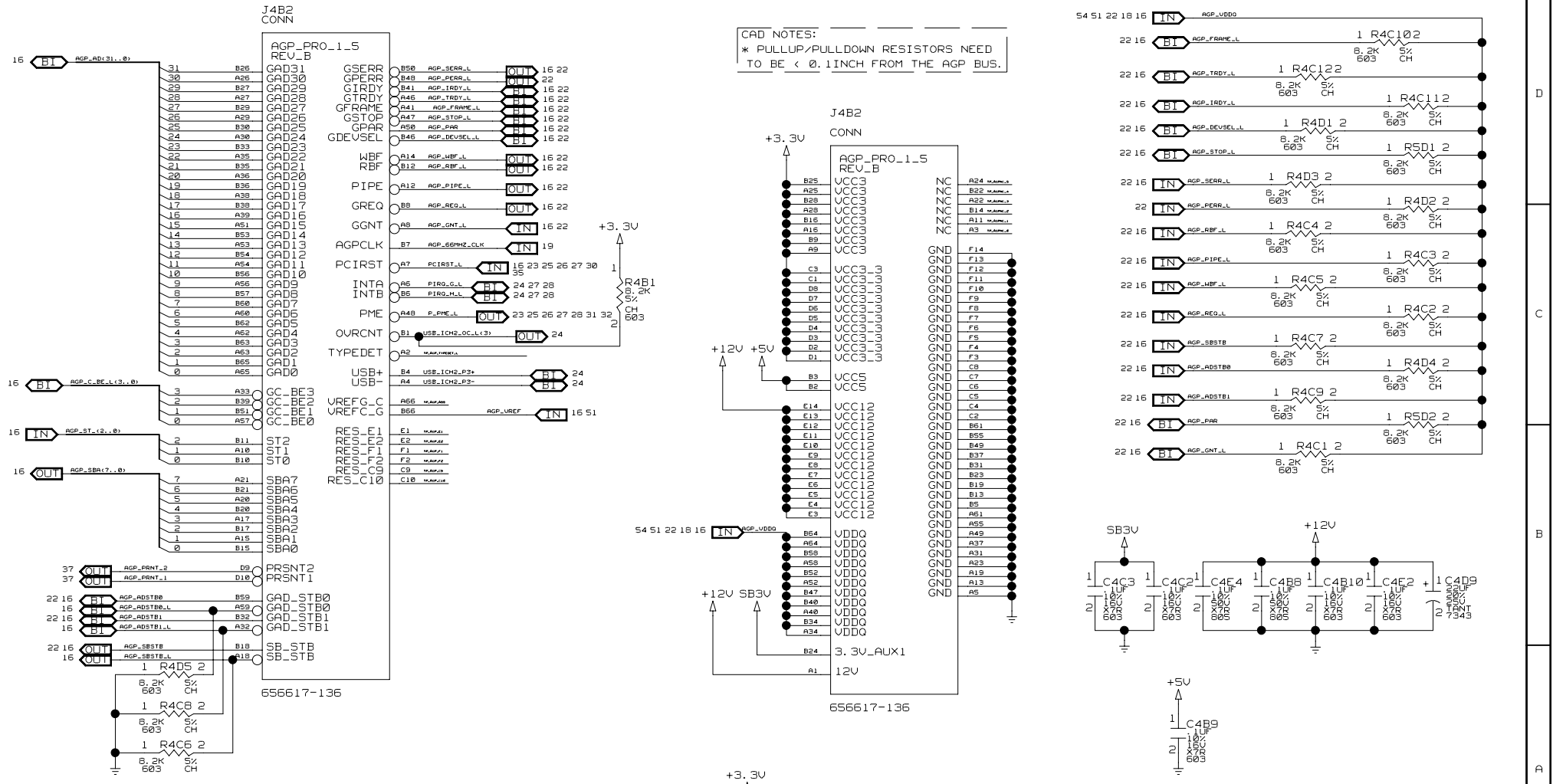


DRAWING

MEC CONNECTOR

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: MEC CONNECTOR	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:03:11 2001
	SHEET: 20

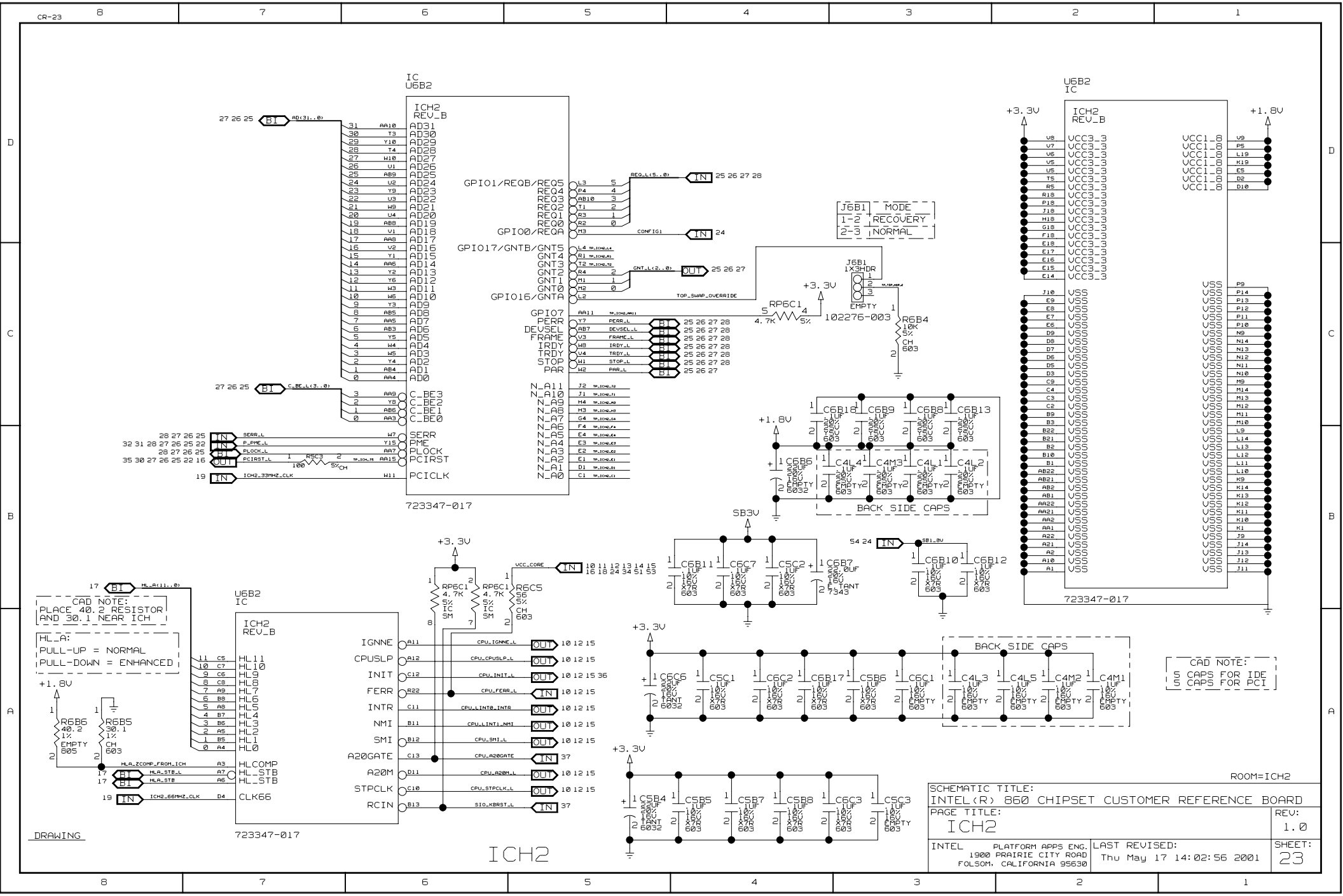

CR-21
8
7
6
5
4
3
2
1
D
C
B
A
MULT | SYSTEM BUS | RAMBUS CLK | MULT0 | MULT1
X3 | 100 | 300 | 0 | 1
X4 | 100 | 400 | 1 | 1
NOTE: ONLY 400MHZ RAMBUS CLOCK IS SUPPORTED
FOR SYSTEMS USING THE MEC.
THIS PLATFORM ONLY SUPPORTS 400 BECAUSE IT USES A MEC.
FUNCTION | S0 | S1
NORMAL | 0 | 0
BYPASS | 1 | 0
TEST | 1 | 1
OUTPUT TEST (0E) | 0 | 1
+3.3V
+1.8V
FB4E1
FB4F1
651000-007
IC DRCG U4E1
IC DRCG U4F1
VDDIR
REFCLK
VDD
GND
PCLKM
SYNCLKN
VDDIPD
STOPB
PWRDNB
S0
S1
N/C
CLKB
MULT0
MULT1
PART_NUMBER=741598-008
741598-008
DRCGA_3_3V
DRCGB_3_3V
VCC3_CLK
DRCG_REF_CLKA
DRCG_REF_CLKB
M_HCLKOUT_A
M_RCLKOUT_A
M_HCLKOUT_B
M_RCLKOUT_B
DRCG_CTRL
DRCG_MULT0
DRCG_MULT1
M_DRCG_A
M_DRCG_A_L
M_DRCG_B
M_DRCG_B_L
R4E9 10K 5% CH 603
R4E2 10K 5% CH 603
R3E6 10K 5% CH 603
R4E7 2 1K 5%
R4E8 2 1K 5%
R4E5 2 39 5%
R4E4 2 39 5%
R4E3 2 51 5%
R4E6 2 51 5%
R4E1 2 4.7K 603 5% CH
R4F8 2 1K 5%
R4F7 2 1K 5%
R4F5 2 39 5%
R4F3 2 39 5%
R4F6 2 51 5%
R4F2 2 51 5%
R4F4 2 4.7K 603 5% CH
R4F1 2 4.7K 603 5% CH
C4E7 22UF 20% 16V TANT 6032
C4E18 C4E19 C4E14 C4E15 C4E23 C4E9 C4E21 C4E13 C4E12 C4E11
C4F1 C4F2 C4F9 C4F10 C4F6 C4F12 C4F7 C4F11 C4F5 C4F4 C4F3
C3E11 C3F3
C4E8 C4F8 4.7PF 50V COG 603
DECISION TO POPULATE C3F13 AND C4F8 SHOULD BE MADE BY
THE CLOCK TO DATA CENTERING VALUE TQ.
ROOM=DRCG0
ROOM=DRCG1
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
DRCG* (RAMBUS CLOCK)
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Fri May 18 14:01:20 2001
SHEET:
21
DRAWING
DRCG* (RAMBUS CLOCK)

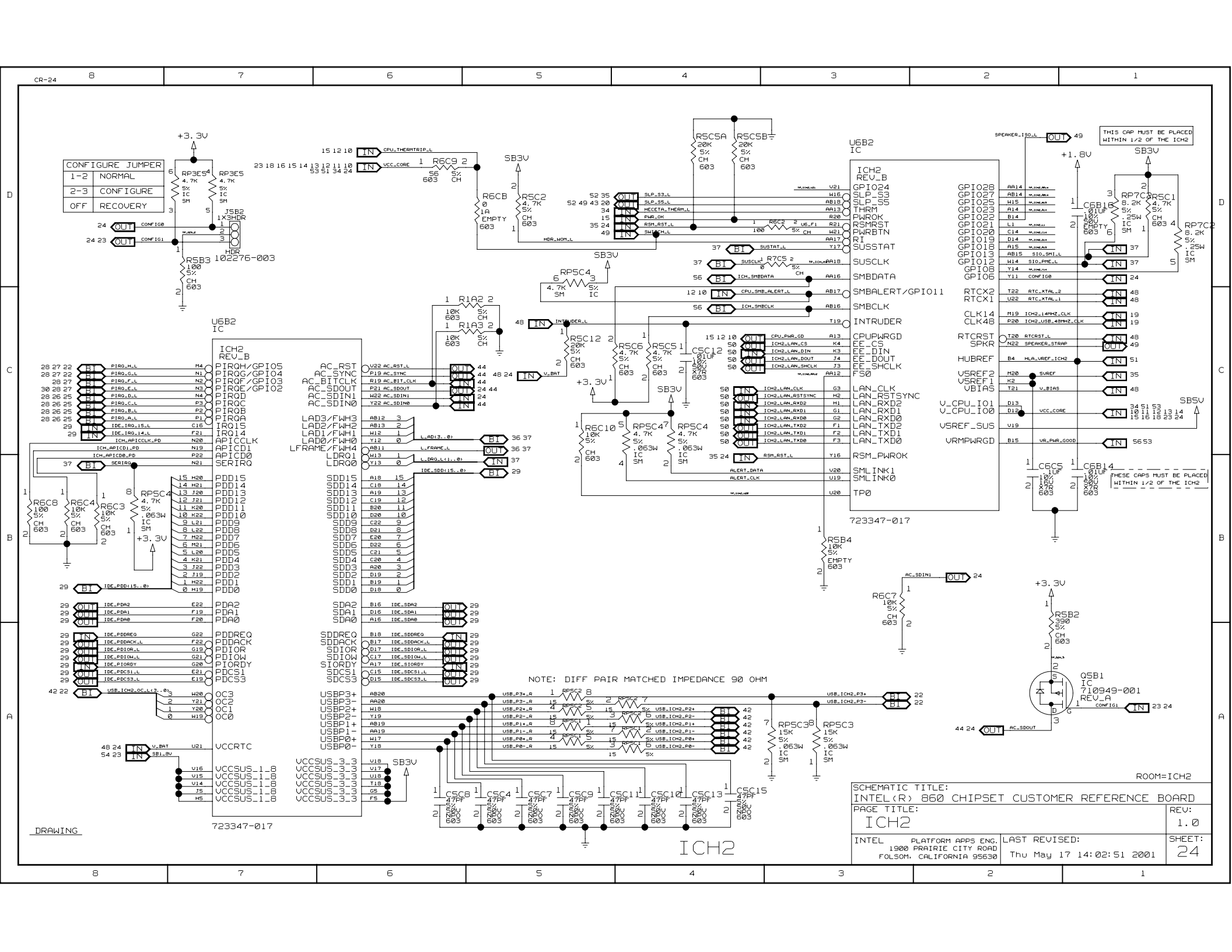


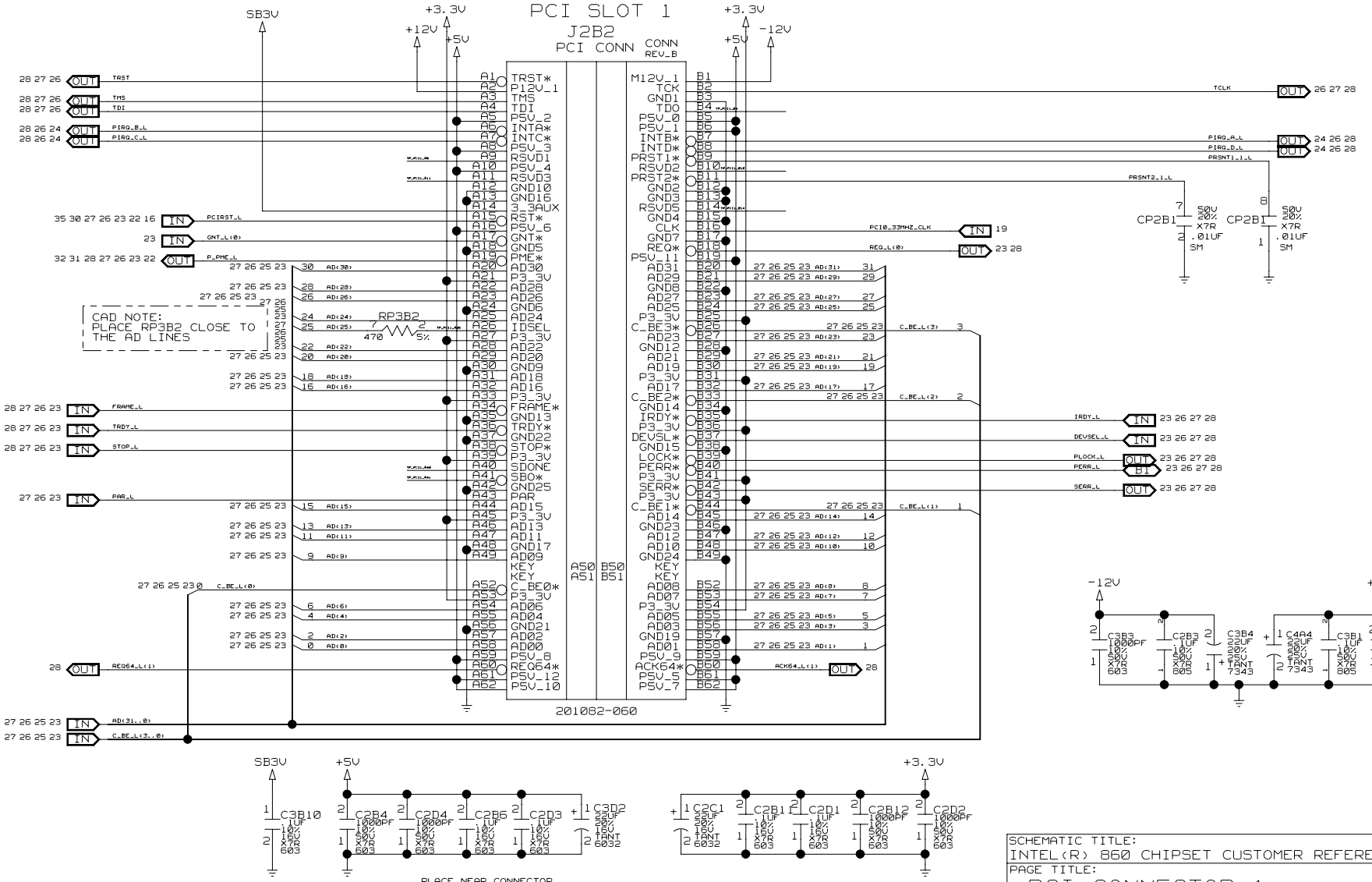
AGP CONNECTOR

ROOM=AGP

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: AGP CONNECTOR	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:03:01 2001
	SHEET: 22


IC
U6B2
ICH2
REV_B
723347-017
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
C_BE3
C_BE2
C_BE1
C_BE0
SERR
PME
PLOCK
PCIRST
PCICLK
GPIO1/REQB/REQ5
REQ4
REQ3
REQ2
REQ1
REQ0
GPIO0/REQA
GPIO17/GNTB/GNT5
GNT4
GNT3
GNT2
GNT1
GNT0
GPIO16/GNTA
GPIO7
PERR
DEVSEL
FRAME
IRDY
TRDY
STOP
PAR
N_A11
N_A10
N_A9
N_A8
N_A7
N_A6
N_A5
N_A4
N_A3
N_A2
N_A1
N_A0
REQ_L(5..0)
CONFIG1
GNT_L(2..0)
TOP_SWAP_OVERRIDE
J6B1
MODE
1-2 RECOVERY
2-3 NORMAL
J6B1
1X3HDR
EMPTY
102276-003
RP6C1
4.7K
R6B4
10K
CH
603
+3.3V
+1.8V
SB3V
BACK SIDE CAPS
CAD NOTE:
PLACE 40.2 RESISTOR
AND 30.1 NEAR ICH
HL_A:
PULL-UP = NORMAL
PULL-DOWN = ENHANCED
R6B6
40.2
EMPTY
805
R6B5
30.1
CH
603
HL11
HL10
HL9
HL8
HL7
HL6
HL5
HL4
HL3
HL2
HL1
HL0
HLCOMP
HL_STB
HL_STB
CLK66
IGNNE
CPUSLP
INIT
FERR
INTR
NMI
SMI
A20GATE
A20M
STPCLK
RCIN
R6C5
56
CAD NOTE:
5 CAPS FOR IDE
5 CAPS FOR PCI
DRAWING
ICH2
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
ICH2
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:02:56 2001
SHEET:
23
ROOM=ICH2


CR-24
CONFIGURE JUMPER
1-2 NORMAL
2-3 CONFIGURE
OFF RECOVERY
J5B2 1X3HDR
HDR 102276-003
U6B2 IC
ICH2 REV_B
723347-017
THIS CAP MUST BE PLACED WITHIN 1/2 OF THE ICH2
THESE CAPS MUST BE PLACED WITHIN 1/2 OF THE ICH2
NOTE: DIFF PAIR MATCHED IMPEDANCE 90 OHM
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
ICH2
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:02:51 2001
SHEET:
24
ROOM=ICH2
DRAWING
ICH2

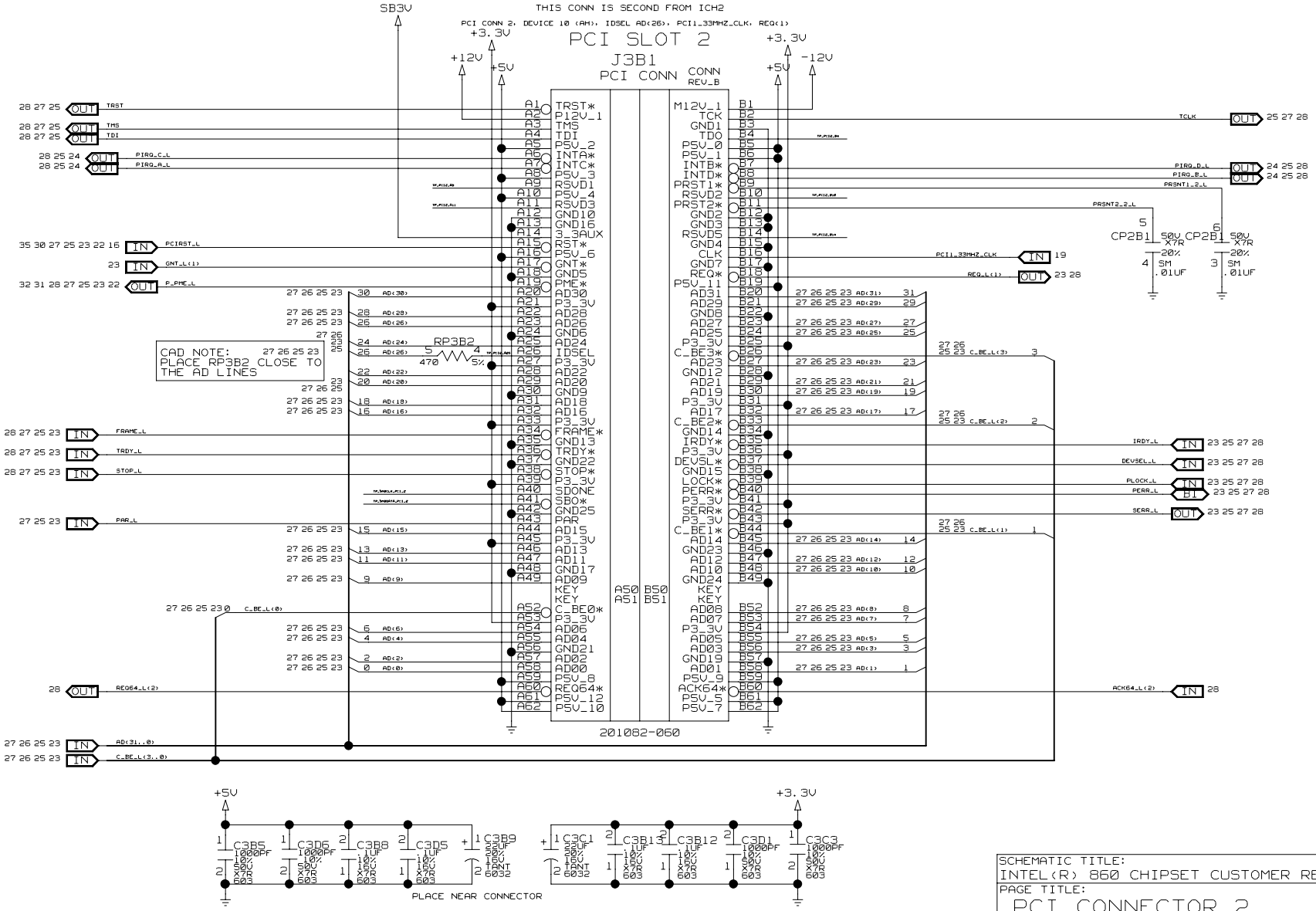


DRAWING

PCI CONNECTOR 1 AND DECOUPLING

ROOM=PCI1

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: PCI CONNECTOR 1	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:46 2001
	SHEET: 25

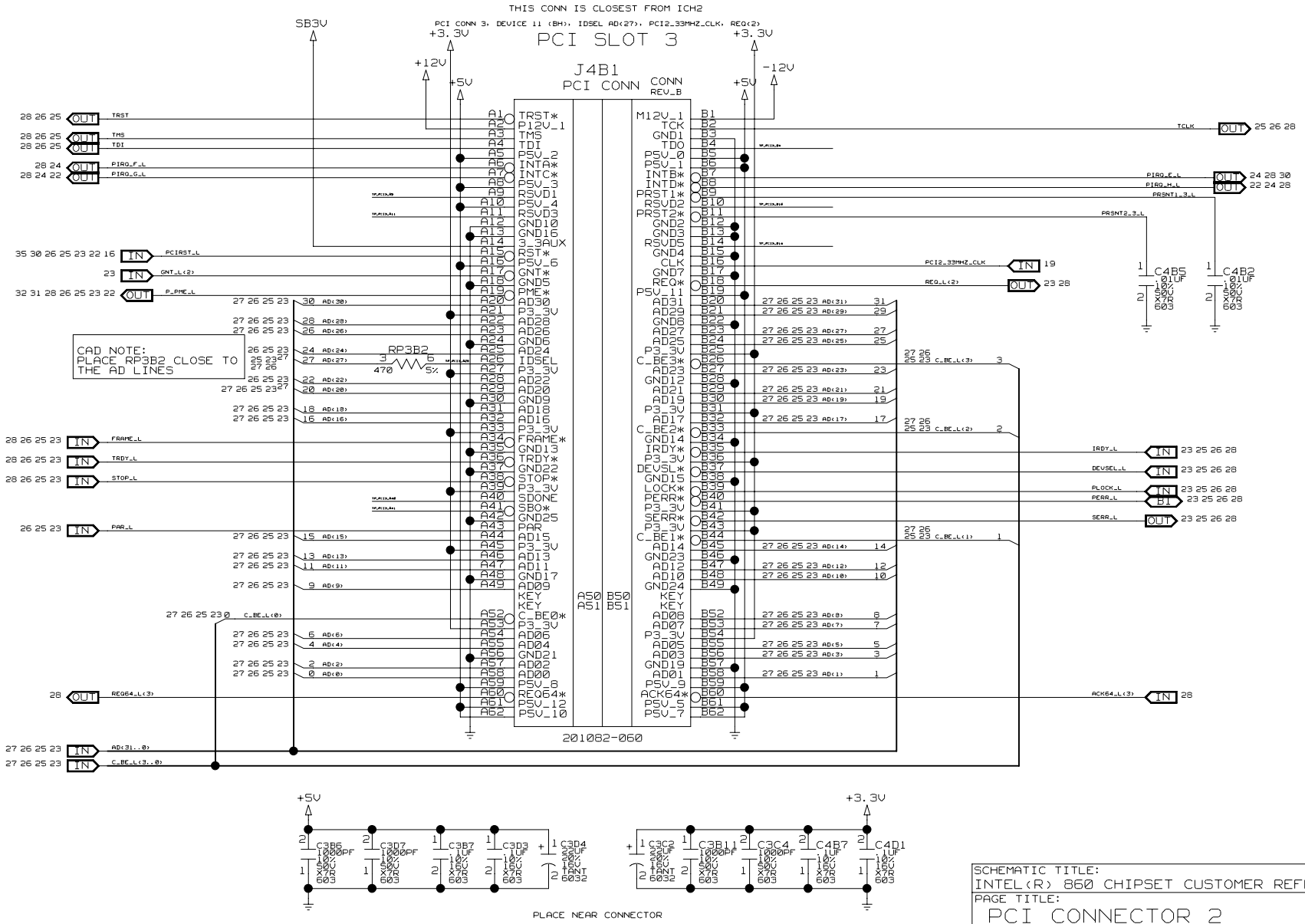


DRAWING

PCI CONNECTOR 2 AND DECOUPLING

ROOM=PCI2

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: PCI CONNECTOR 2	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:41 2001
	SHEET: 26

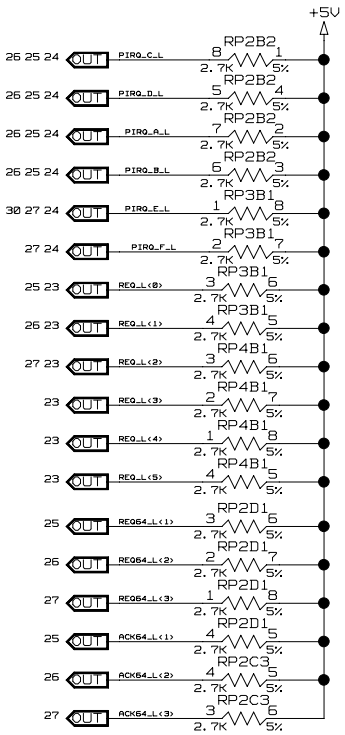


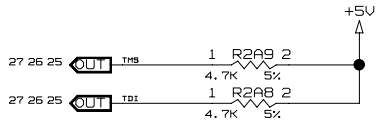
PCI CONNECTOR 3 AND DECOUPLING

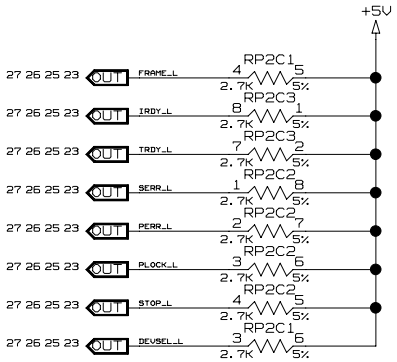
DRAWING

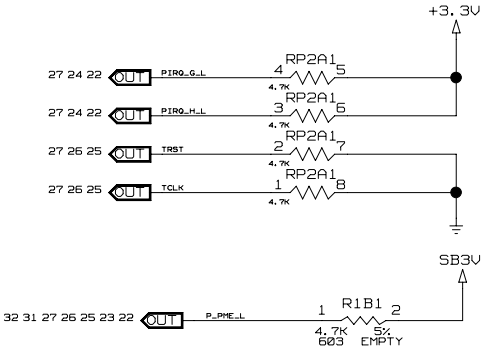
ROOM=PCI3

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: PCI CONNECTOR 2	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:36 2001
	SHEET: 27









DRAWING

PCI33 TERMINATION

ROOM=PCI33_TERM

SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD

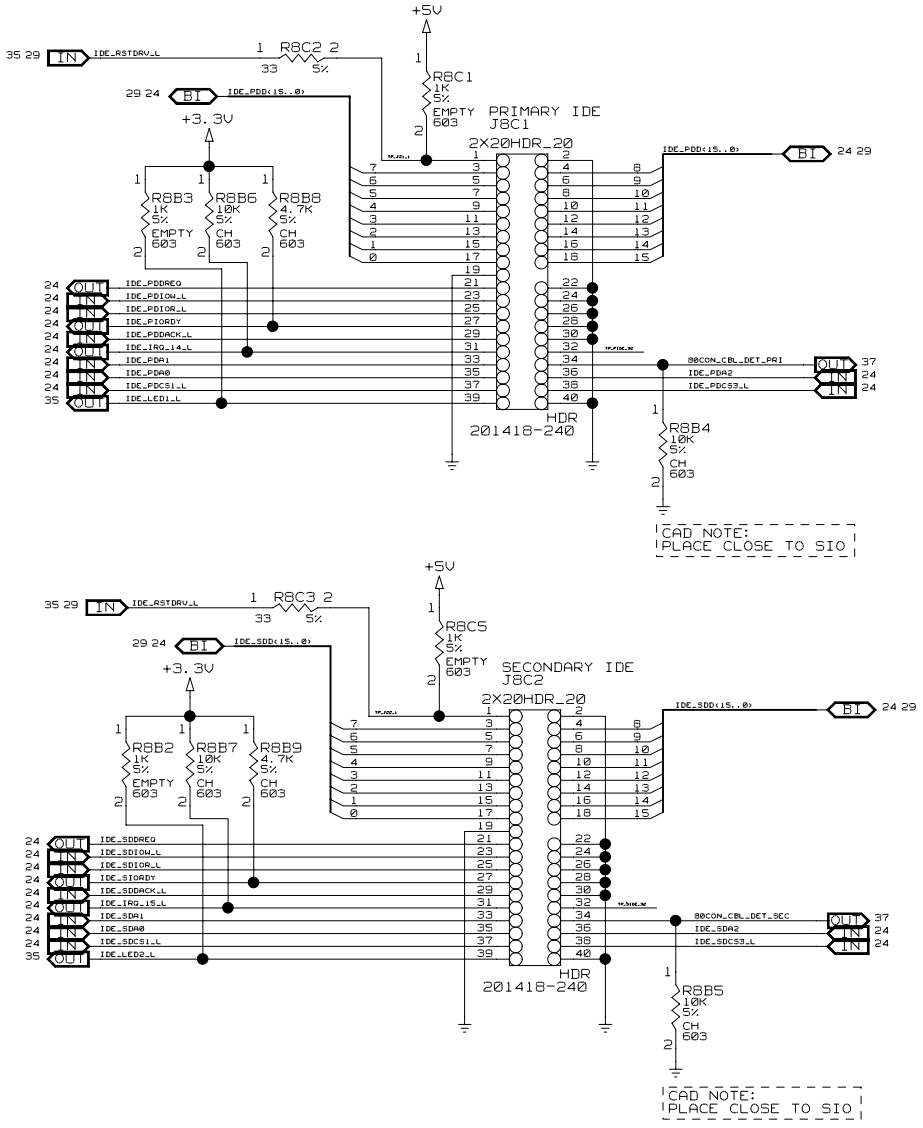
PAGE TITLE:
PCI33 TERMINATION

REV: 1.0

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED:
Thu May 17 14:02:31 2001

SHEET: 28



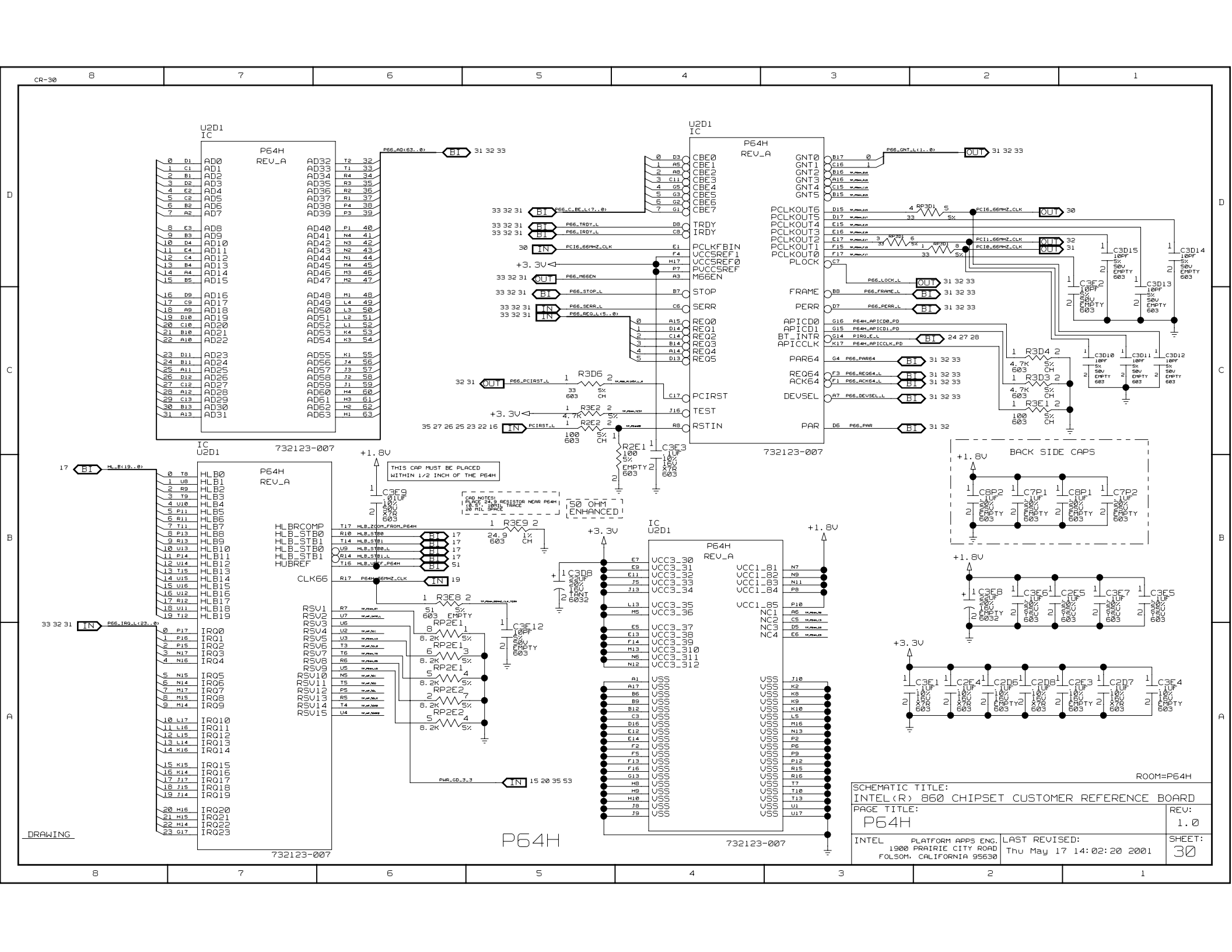
ROOM=IDEPRI

ROOM=IDESEC

DRAWING

IDE PRIMARY / SECONDARY

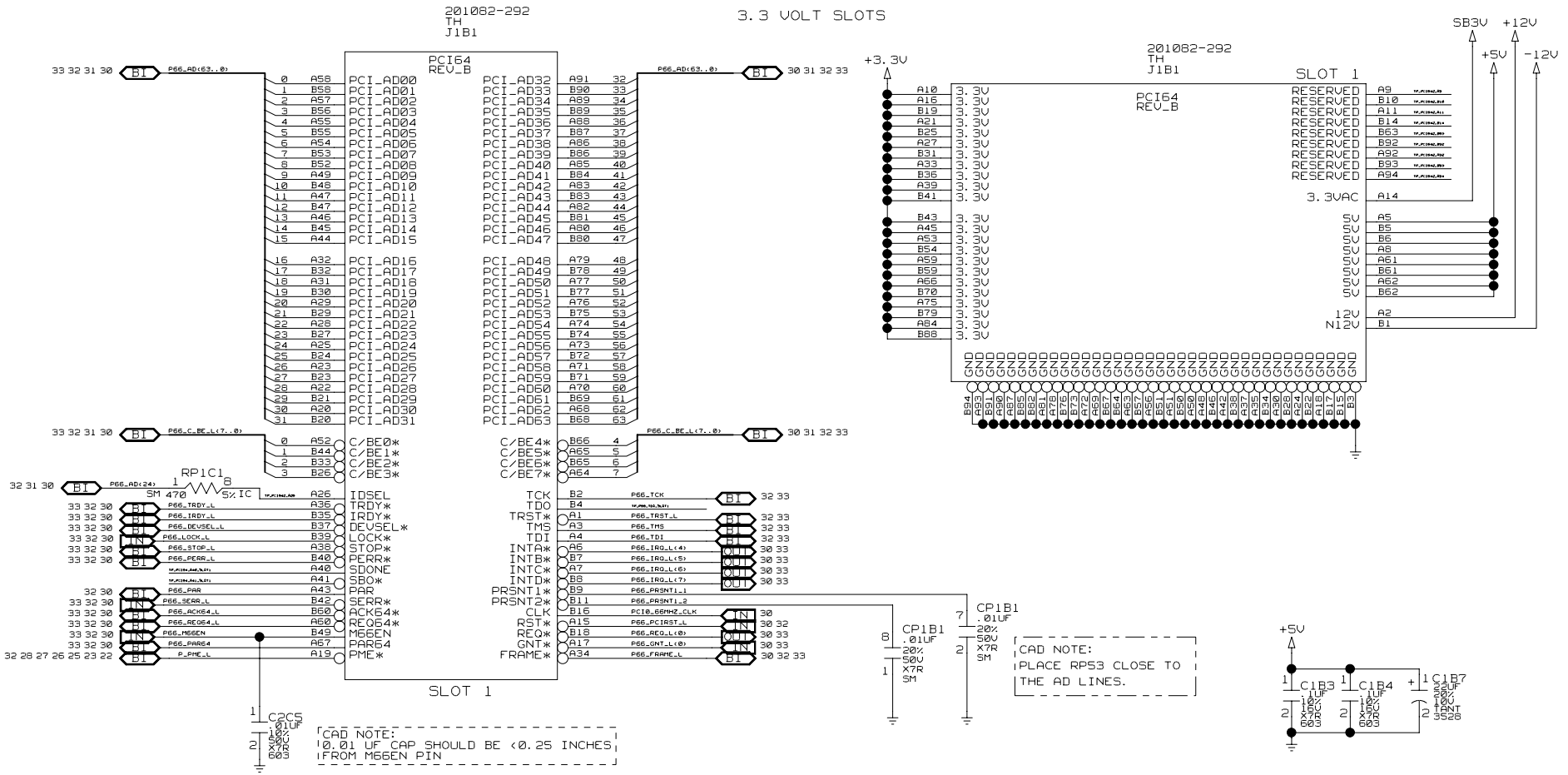
SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: IDE PRIMARY / SECONDARY		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:26 2001	SHEET: 29

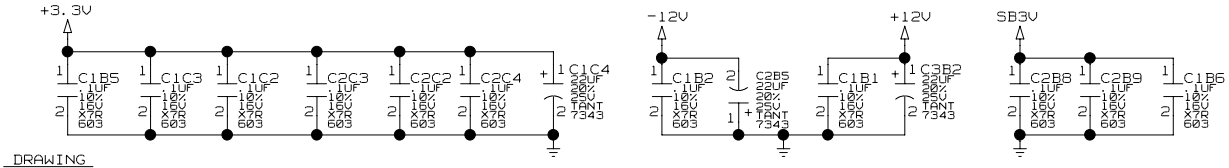

U2D1
IC
P64H
REV_A
732123-007
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
AD32
AD33
AD34
AD35
AD36
AD37
AD38
AD39
AD40
AD41
AD42
AD43
AD44
AD45
AD46
AD47
AD48
AD49
AD50
AD51
AD52
AD53
AD54
AD55
AD56
AD57
AD58
AD59
AD60
AD61
AD62
AD63
P66_AD<63..0>
CBE0
CBE1
CBE2
CBE3
CBE4
CBE5
CBE6
CBE7
P66_C_BE_L<7..0>
TRDY
IRDY
P66_TRDY_L
P66_IRDY_L
PCLKFBIN
VCC5REF1
VCC5REF0
PUCC5REF
M66EN
P66_M66EN
STOP
P66_STOP_L
SERR
P66_SERR_L
P66_REQ_L<5..0>
REQ0
REQ1
REQ2
REQ3
REQ4
REQ5
PCIRST
TEST
RSTIN
PCIRST_L
R3D6
R3E2
R2E2
R2E1
C3E3
GNT0
GNT1
GNT2
GNT3
GNT4
GNT5
P66_GNT_L<1..0>
PCLKOUT6
PCLKOUT5
PCLKOUT4
PCLKOUT3
PCLKOUT2
PCLKOUT1
PCLKOUT0
PLOCK
P66_LOCK_L
FRAME
P66_FRAME_L
PERR
P66_PERR_L
APICD0
APICD1
BT_INTR
APICCLK
P64H_APICD0_PD
P64H_APICD1_PD
P1RQ_E_L
P64H_APICCLK_PD
PAR64
P66_PAR64
REQ64
P66_REQ64_L
ACK64
P66_ACK64_L
DEVSEL
P66_DEVSEL_L
PAR
P66_PAR
RP3D1
R3D4
R3D3
R3E1
C3D15
C3D14
C3E2
C3D13
C3D10
C3D11
C3D12
PCI6_66MHZ_CLK
PCI1_66MHZ_CLK
BACK SIDE CAPS
C8P2
C7P1
C8P1
C7P2
HLB_B<19..0>
HLB0
HLB1
HLB2
HLB3
HLB4
HLB5
HLB6
HLB7
HLB8
HLB9
HLB10
HLB11
HLB12
HLB13
HLB14
HLB15
HLB16
HLB17
HLB18
HLB19
HLBRCOMP
HLB_STB0
HLB_STB1
HLB_STB0_L
HLB_STB1_L
HUBREF
CLK66
P64H_66MHZ_CLK
P66_IRQ_L<23..0>
IRQ0
IRQ1
IRQ2
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8
IRQ9
IRQ10
IRQ11
IRQ12
IRQ13
IRQ14
IRQ15
IRQ16
IRQ17
IRQ18
IRQ19
IRQ20
IRQ21
IRQ22
IRQ23
RSV1
RSV2
RSV3
RSV4
RSV5
RSV6
RSV7
RSV8
RSV9
RSV10
RSV11
RSV12
RSV13
RSV14
RSV15
RP2E1
RP2E2
C3E12
R3E8
R3E9
C3E9
THIS CAP MUST BE PLACED
WITHIN 1/2 INCH OF THE P64H
CAD NOTES:
PLACE 24.9 RESISTOR NEAR P64H
(@ 5", 10MIL TRACE
20 MIL SPACE
50 OHM
ENHANCED
PWR_GD_3_3
C3D8
C3E1
C2E4
C2D6
C2D8
C2E3
C2D7
C3E4
C3E6
C2E5
C3E7
C3E5
C3E8
+1.8V
+3.3V
ROOM=P64H
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
P64H
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:02:20 2001
SHEET:
30
DRAWING
P64H

THIS CONN IS FIFTH FROM ICH2
PCI64 CONN 1, DEVICE 8 (8H), IDSEL P66_AD(24), PCI0_66MHZ_CLK, REQ(0)

PCI64 SLOT 1

3.3 VOLT SLOTS





DRAWING

PCI64 SLOT1

ROOM=PCI66_1

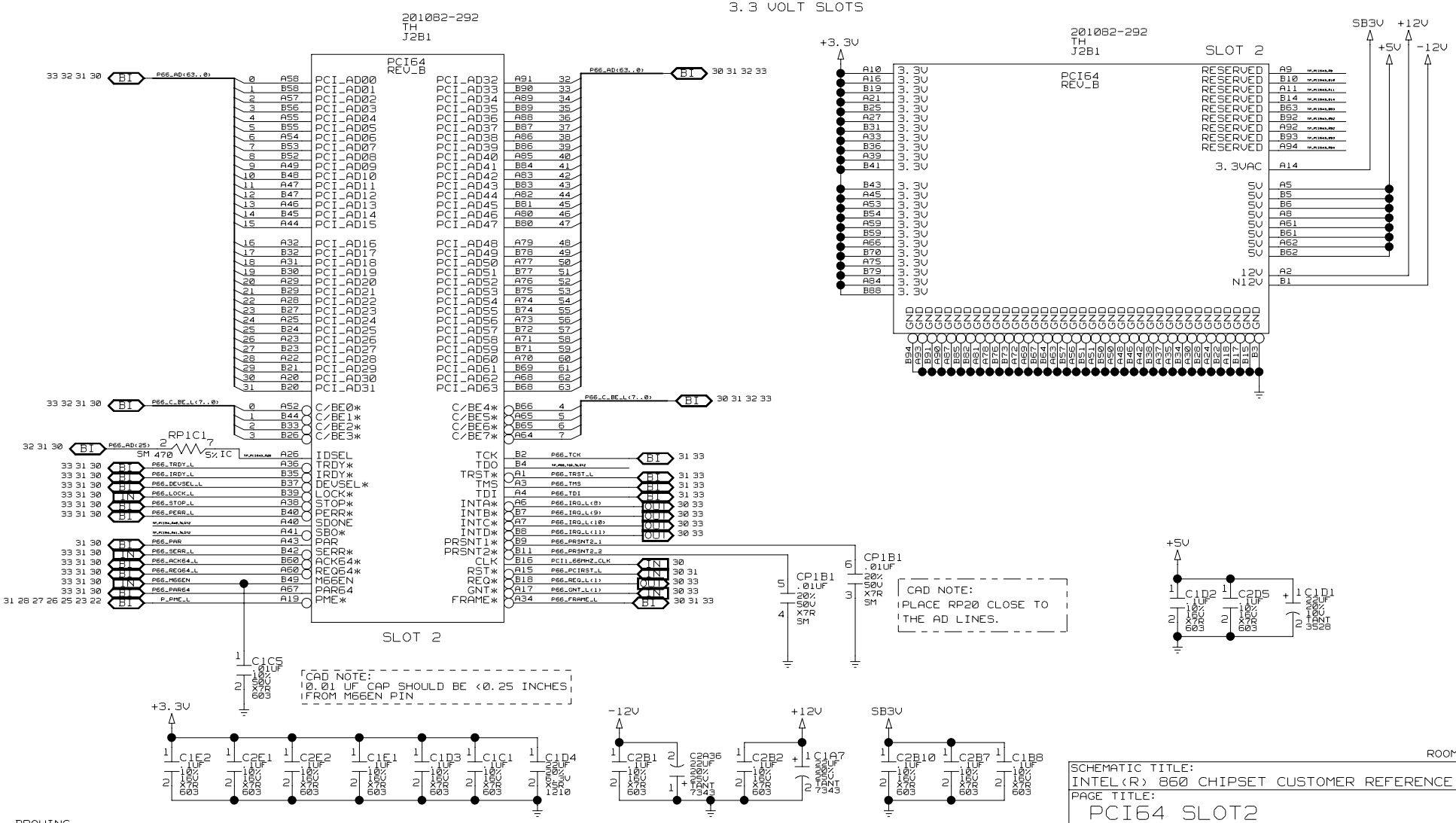
SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: PCI64 SLOT1	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:15 2001
	SHEET: 31

THIS CONN IS FOURTH FROM ICH2

PCI64 CONN21, DEVICE 9 (9H), IDSEL P66_AD(25), PCI1_66MHZ_CLK, REQ(1)

PCI64 SLOT 2

3.3 VOLT SLOTS

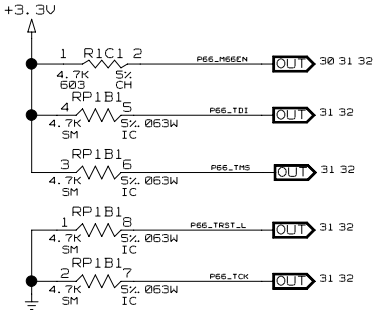


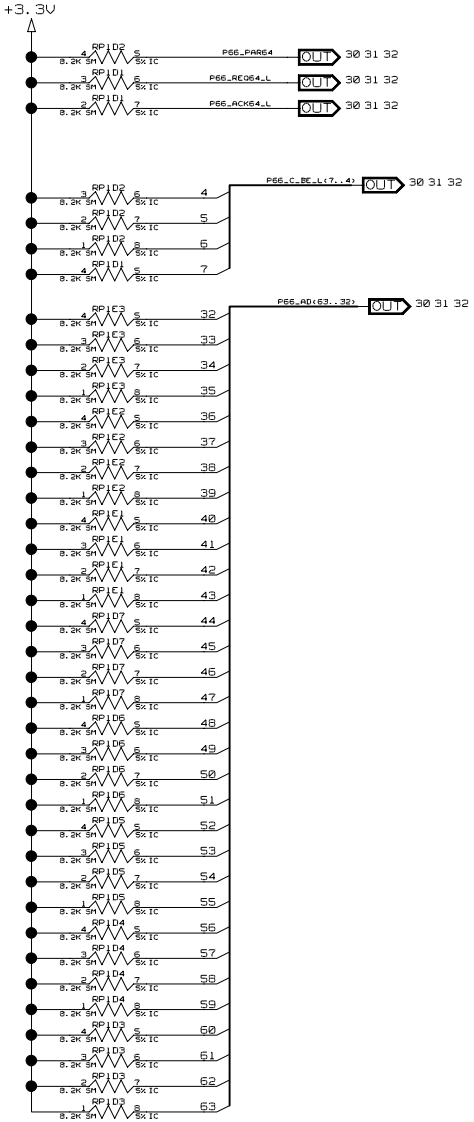
DRAWING

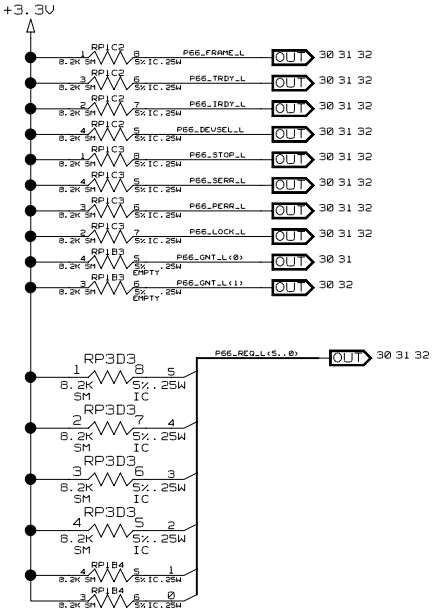
PCI64 SLOT2

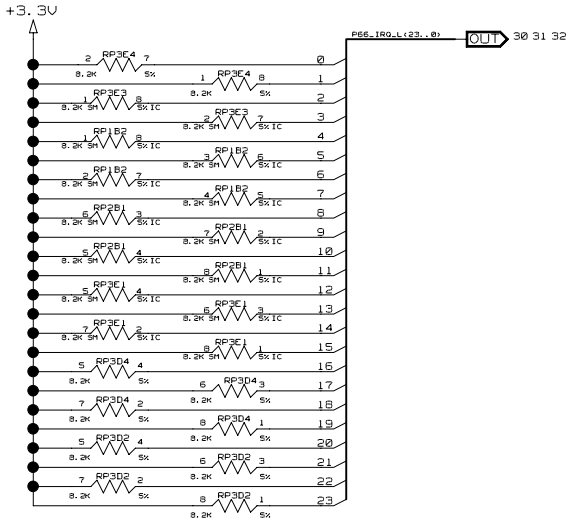
ROOM=PCI66_2

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI64 SLOT2		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:11 2001	SHEET: 32







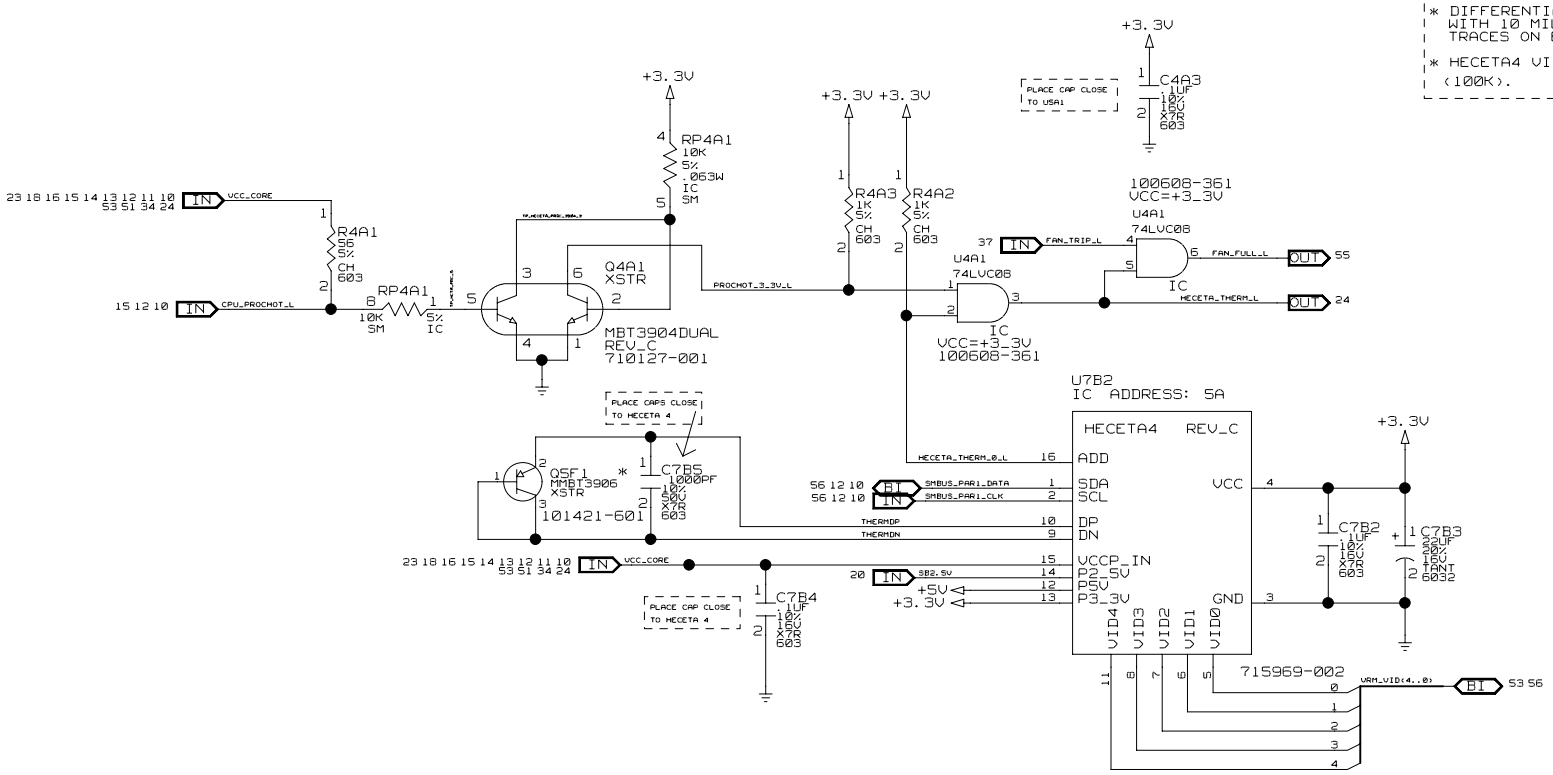


DRAWING

PCI66 TERMINATION

ROOM=PCI66_TERM

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI66 TERMINATION		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:06 2001	SHEET: 33

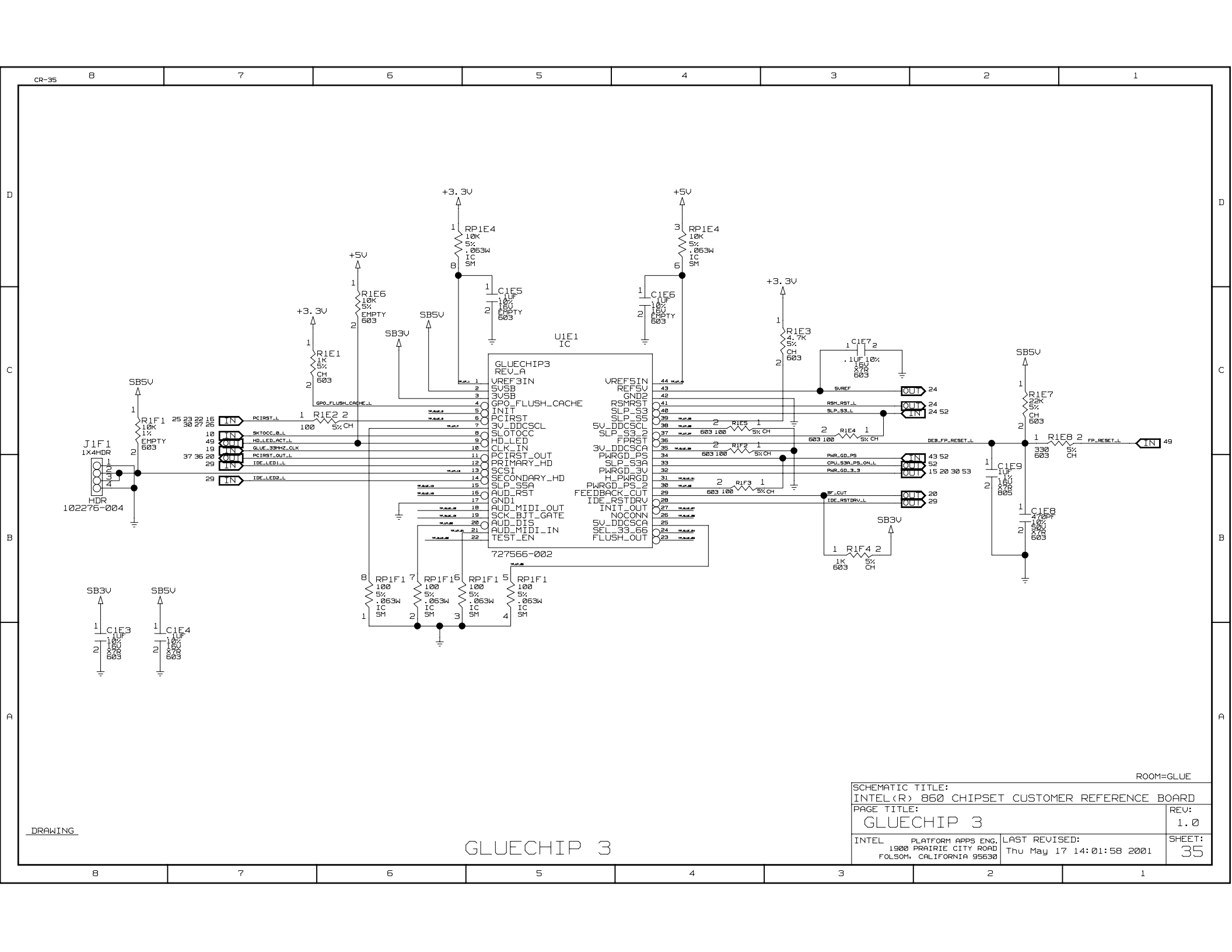


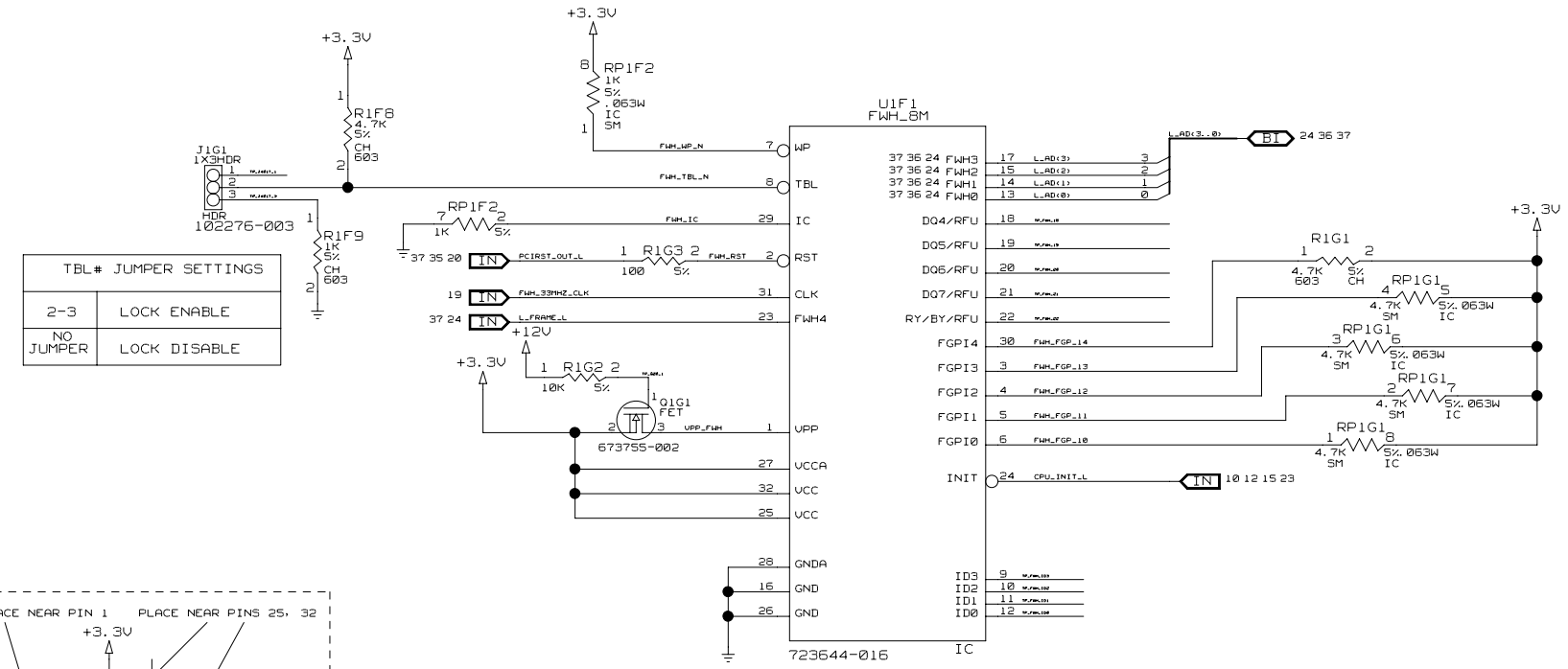
ROOM=HECETA

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: HECETA 4	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:02 2001
	SHEET: 34

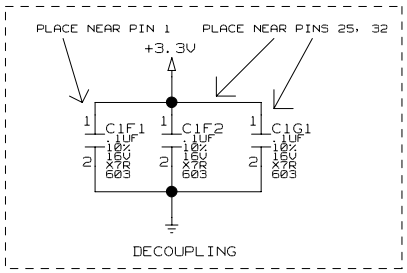
DRAWING

HECETA 4


CR-35
GLUECHIP3
REV_A
U1E1
IC
727566-002
VREF3IN
5VSB
3VSB
GPO_FLUSH_CACHE
INIT
PCIRST
3V_DDCSCL
SLOTOCC
HD_LED
CLK_IN
PCIRST_OUT
PRIMARY_HD
SCSI
SECONDARY_HD
SLP_S5A
AUD_RST
GND1
AUD_MIDI_OUT
SCK_BJT_GATE
AUD_DIS
AUD_MIDI_IN
TEST_EN
VREF5IN
REF5V
GND2
RSMRST
SLP_S3
SLP_S5
5V_DDCSCL
SLP_S3_2
FPRST
3V_DDCSCA
PWRGD_PS
SLP_S3A
PWRGD_3V
H_PWRGD
PWRGD_PS_2
FEEDBACK_CUT
IDE_RSTDRV
INIT_OUT
NOCONN
5V_DDCSCA
SEL_33_66
FLUSH_OUT
J1F1
1X4HDR
HDR
102276-004
+3.3V
+5V
SB5V
SB3V
DRAWING
GLUECHIP 3
ROOM=GLUE
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
GLUECHIP 3
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:01:58 2001
SHEET:
35



TBL# JUMPER SETTINGS	
2-3	LOCK ENABLE
NO JUMPER	LOCK DISABLE



NEED SPACE FOR SOCKET 201138-032

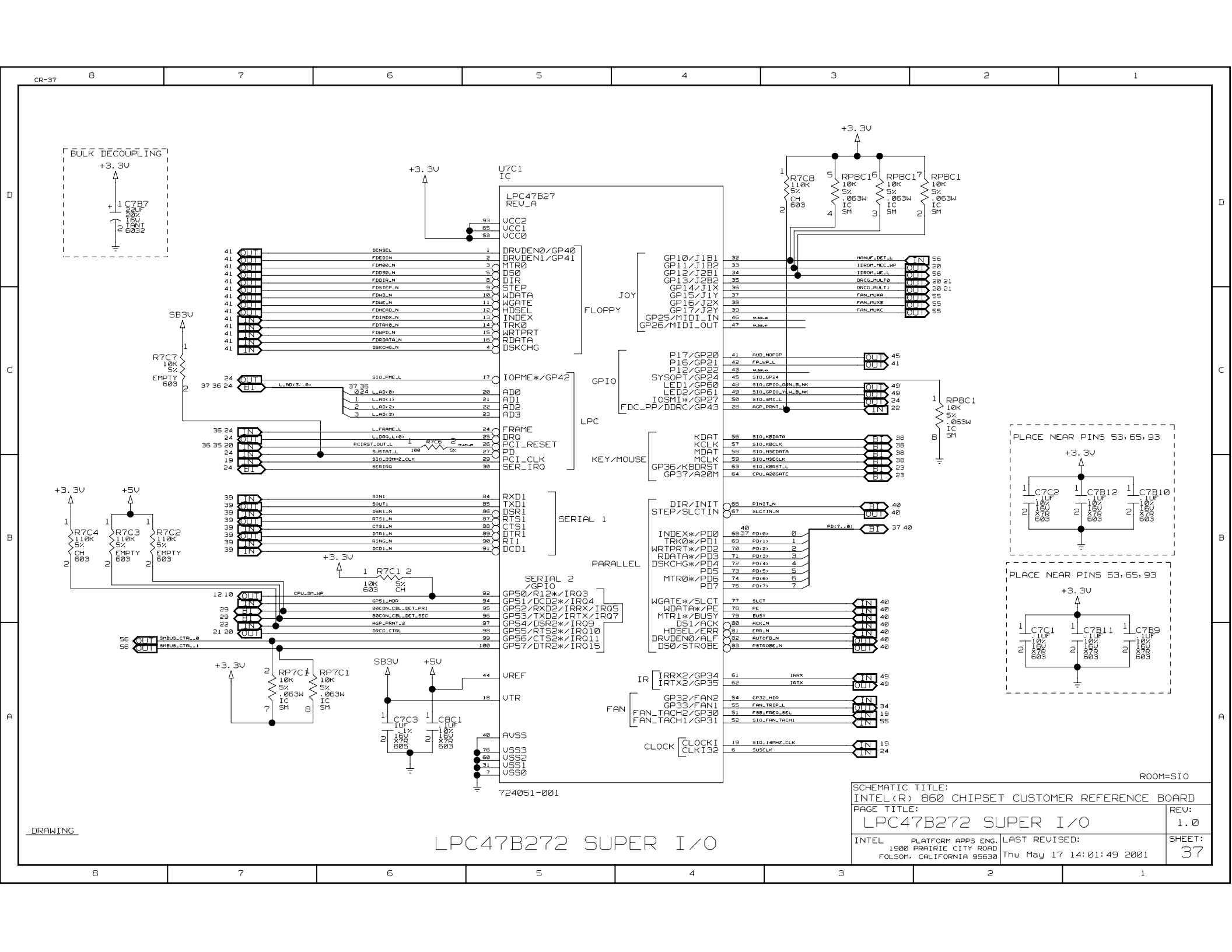
CAD/DESIGN NOTE: ALL PINS MUST HAVE TP'S TO SUPPORT FLASH PROGRAMMING

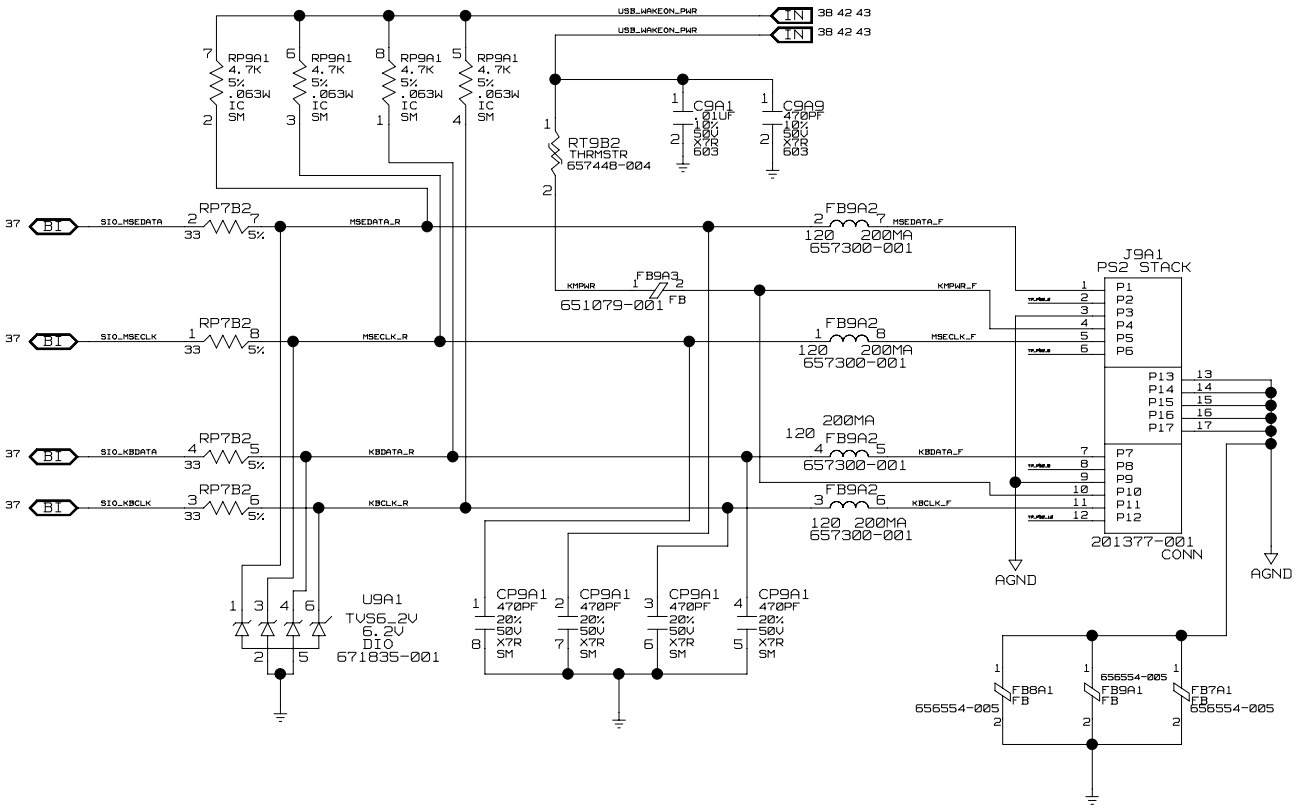
DRAWING

FIRMWARE HUB

ROOM=FWH

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: FIRMWARE HUB		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:53 2001	SHEET: 36


BULK DECOUPLING
+3.3V
C7B7
22UF
20%
16V
TANT
6032
U7C1
IC
LPC47B27
REV_A
VCC2
VCC1
VCC0
DRVDEN0/GP40
DRVDEN1/GP41
MTR0
DS0
DIR
STEP
WDATA
WGATE
HDSEL
INDEX
TRK0
WRTPRT
RDATA
DSKCHG
FLOPPY
IOPME*/GP42
AD0
AD1
AD2
AD3
LPC
FRAME
DRQ
PCI_RESET
PD
PCI_CLK
SER_IRQ
RXD1
TXD1
DSR1
RTS1
CTS1
DTR1
RI1
DCD1
SERIAL 1
SERIAL 2
/GPIO
GP50/R12*/IRQ3
GP51/DCD2*/IRQ4
GP52/RXD2/IRRX/IRQ5
GP53/TXD2/IRTX/IRQ7
GP54/DSR2*/IRQ9
GP55/RTS2*/IRQ10
GP56/CTS2*/IRQ11
GP57/DTR2*/IRQ15
VREF
VTR
AVSS
VSS3
VSS2
VSS1
VSS0
724051-001
GP10/J1B1
GP11/J1B2
GP12/J2B1
GP13/J2B2
GP14/J1X
GP15/J1Y
GP16/J2X
GP17/J2Y
GP25/MIDI_IN
GP26/MIDI_OUT
JOY
P17/GP20
P16/GP21
P12/GP22
SYSOPT/GP24
LED1/GP60
LED2/GP61
IOSMI*/GP27
FDC_PP/DDRC/GP43
GPIO
KDAT
KCLK
MDAT
MCLK
GP36/KBDRST
GP37/A20M
KEY/MOUSE
DIR/INIT
STEP/SLCTIN
INDEX*/PD0
TRK0*/PD1
WRTPRT*/PD2
RDATA*/PD3
DSKCHG*/PD4
PD5
MTR0*/PD6
PD7
WGATE*/SLCT
WDATA*/PE
MTR1*/BUSY
DS1/ACK
HDSEL/ERR
DRVDEN0/ALF
DS0/STROBE
PARALLEL
IRRX2/GP34
IRTX2/GP35
IR
GP32/FAN2
GP33/FAN1
FAN_TACH2/GP30
FAN_TACH1/GP31
FAN
CLOCKI
CLKI32
CLOCK
R7C8
110K
5%
CH
603
RP8C1
10K
5%
.063W
IC
SM
R7C7
10K
5%
EMPTY
603
SB3V
+5V
R7C4
110K
5%
CH
603
R7C3
110K
5%
EMPTY
603
R7C2
110K
5%
EMPTY
603
R7C1
10K
5%
CH
603
RP7C1
10K
5%
.063W
IC
SM
C7C3
1UF
10%
16V
X7R
805
C8C1
1UF
10%
16V
X7R
603
PLACE NEAR PINS 53,65,93
C7C2
C7B12
C7B10
C7C1
C7B11
C7B9
1UF
10%
16V
X7R
603
ROOM=SIO
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
LPC47B272 SUPER I/O
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:01:49 2001
SHEET:
37
DRAWING
LPC47B272 SUPER I/O

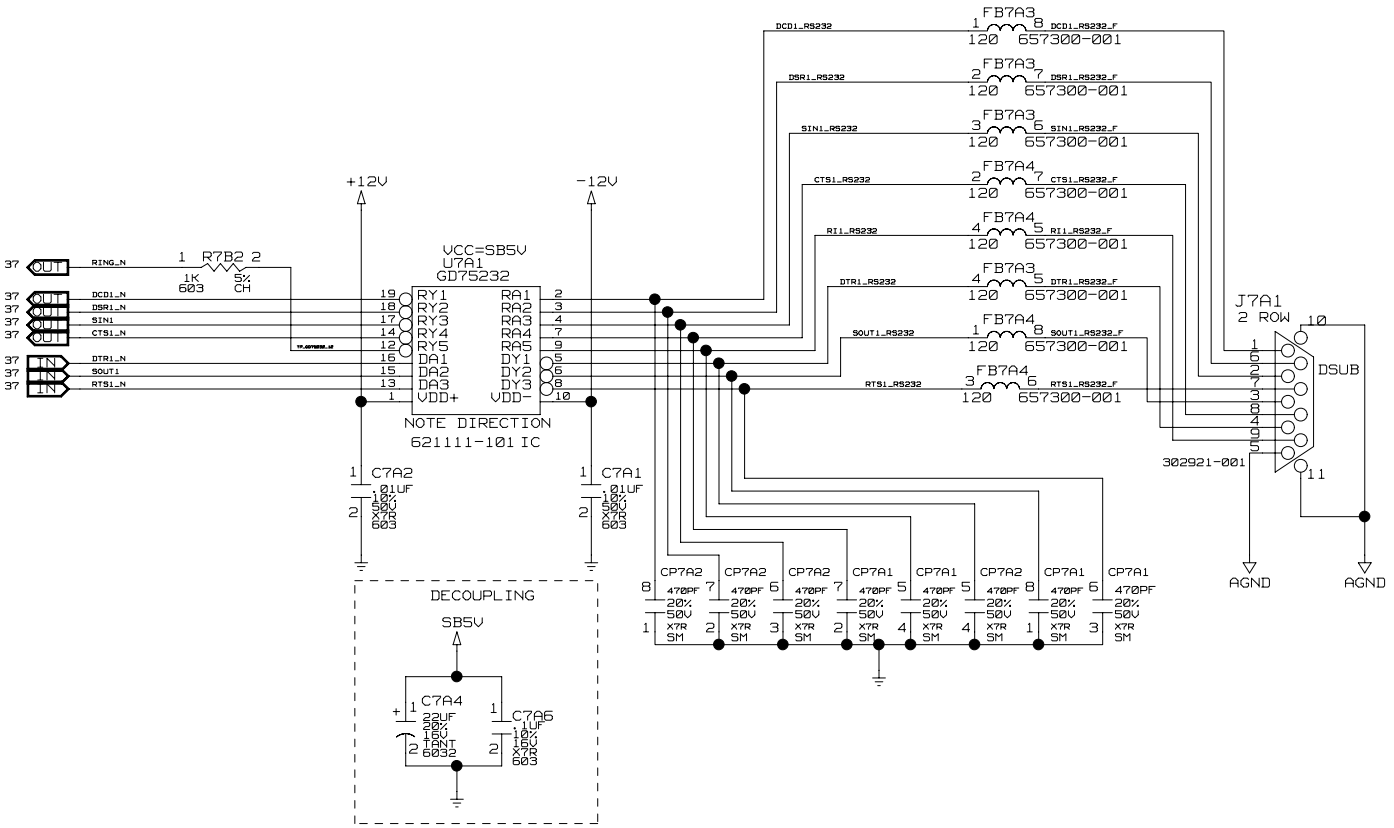


DRAWING

PS2 KEYBOARD AND MOUSE

ROOM=PS2_MOUSE

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: PS2 KEYBOARD AND MOUSE	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:45 2001
	SHEET: 38

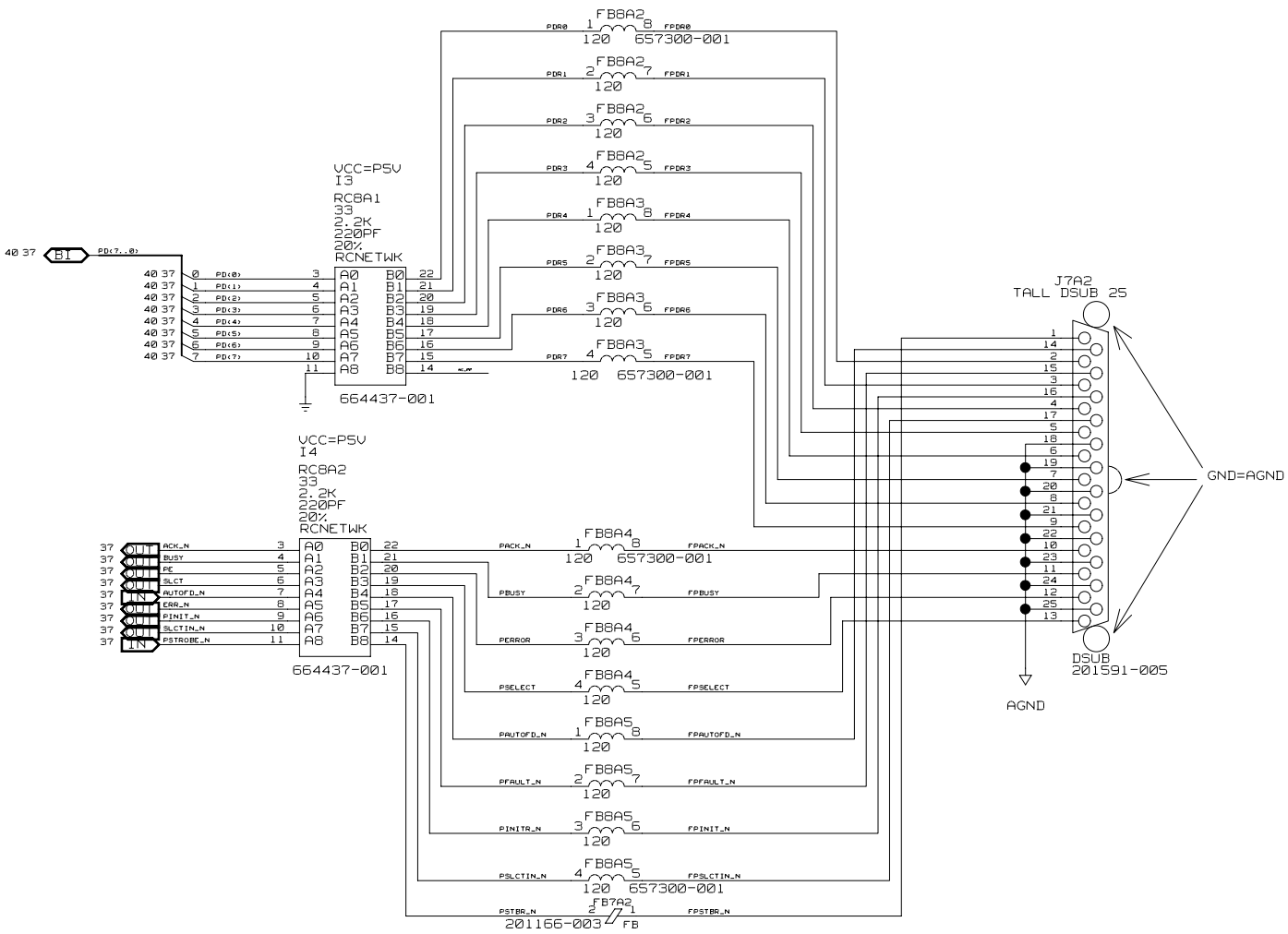


SERIAL PORT

DRAWING

ROOM=SERIAL

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: SERIAL PORT	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:41 2001
	SHEET: 39

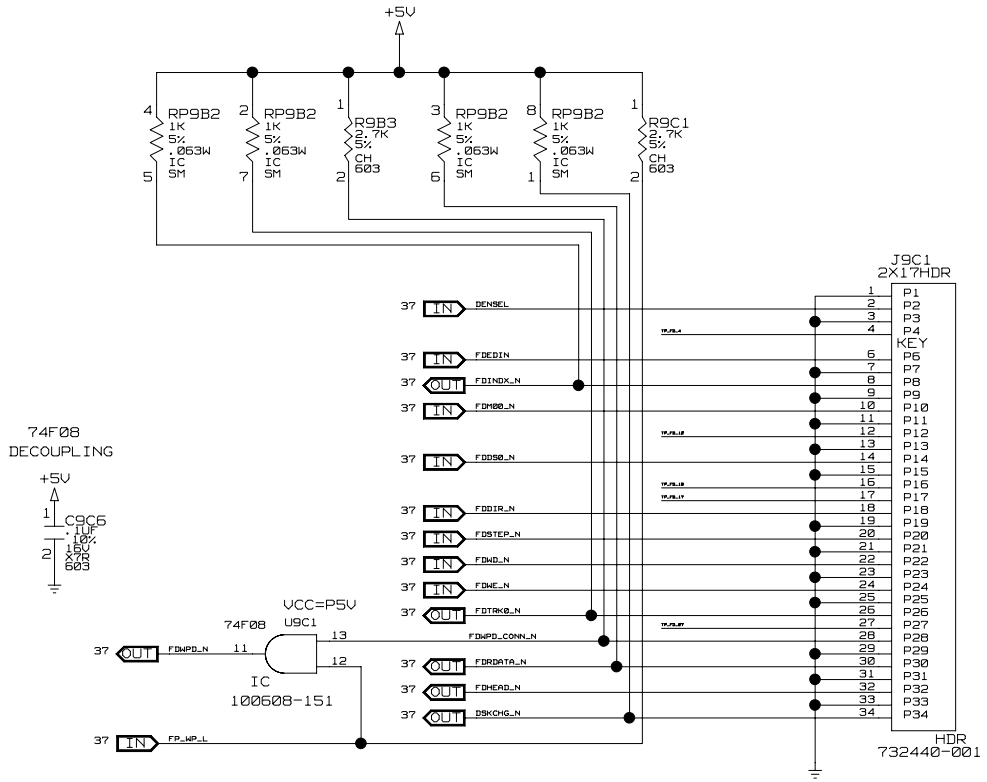


DRAWING

PARALLEL PORT

ROOM=PARALLEL

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: PARALLEL PORT	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:37 2001
	SHEET: 40

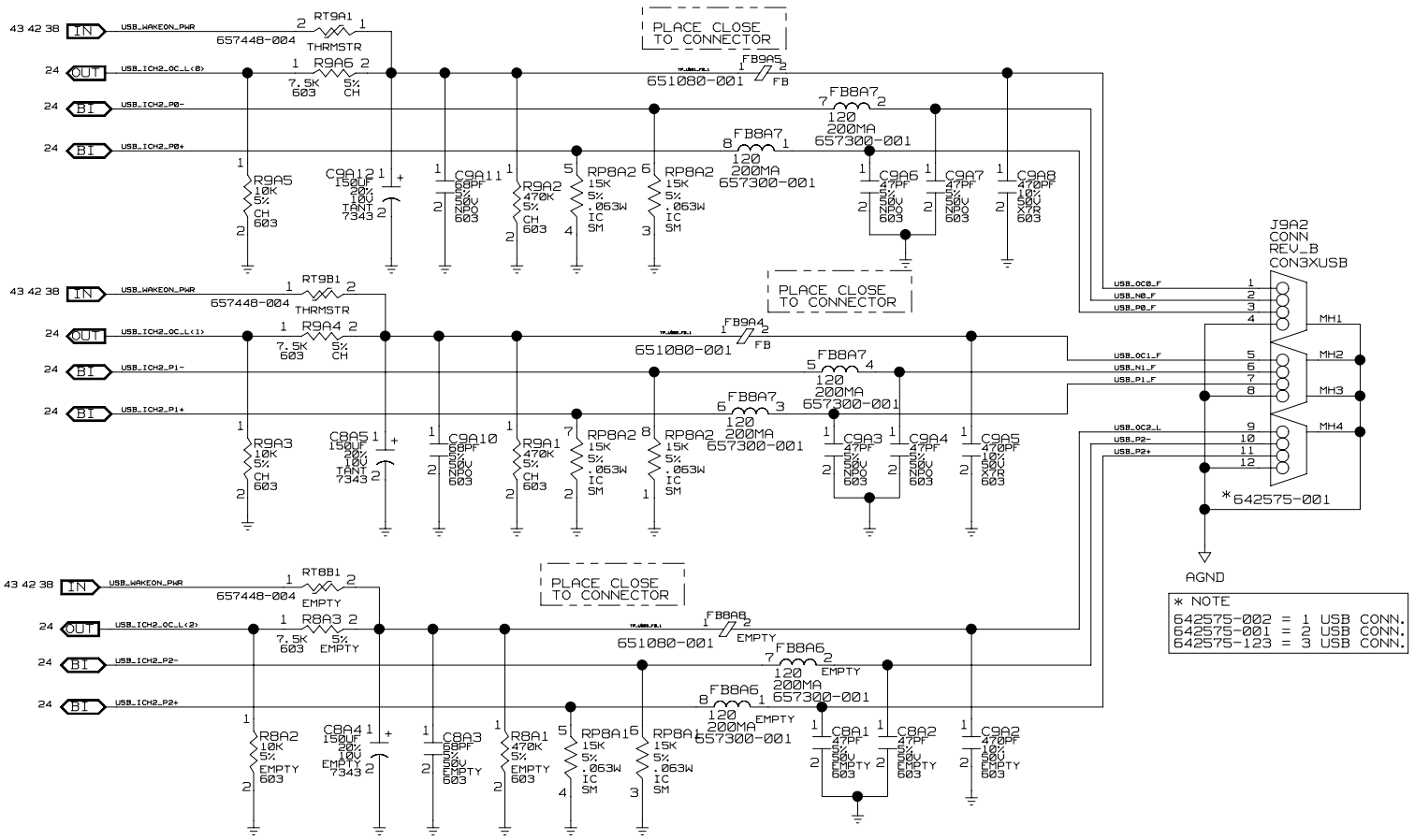


DRAWING

FLOPPY DRIVE PORT

ROOM=FLOPPY

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: FLOPPY DRIVE PORT	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:32 2001
	SHEET: 41



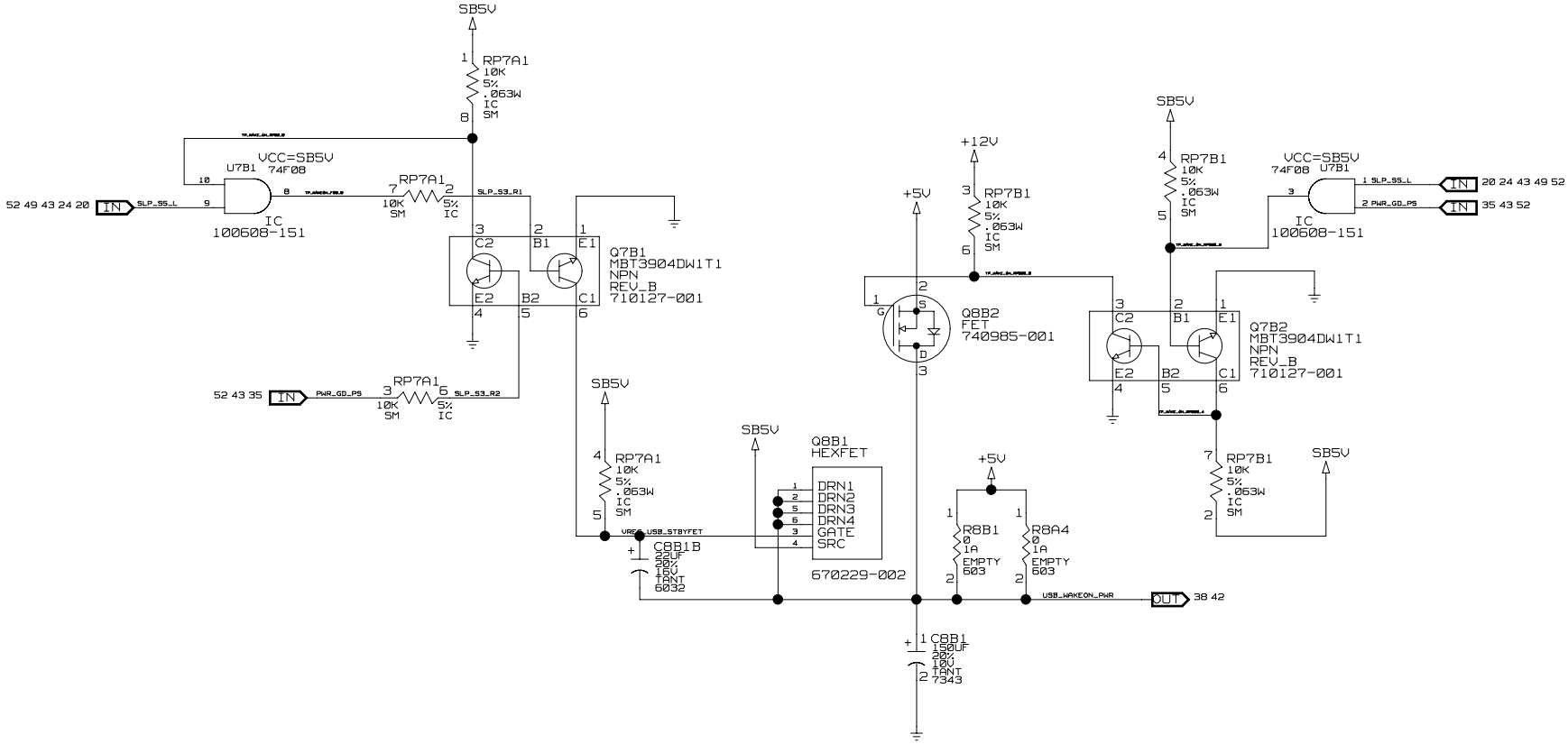
* NOTE
642575-002 = 1 USB CONN.
642575-001 = 2 USB CONN.
642575-123 = 3 USB CONN.

ROOM=USB

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: USB CONNECTORS	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:25 2001
	SHEET: 42

DRAWING

USB CONNECTORS

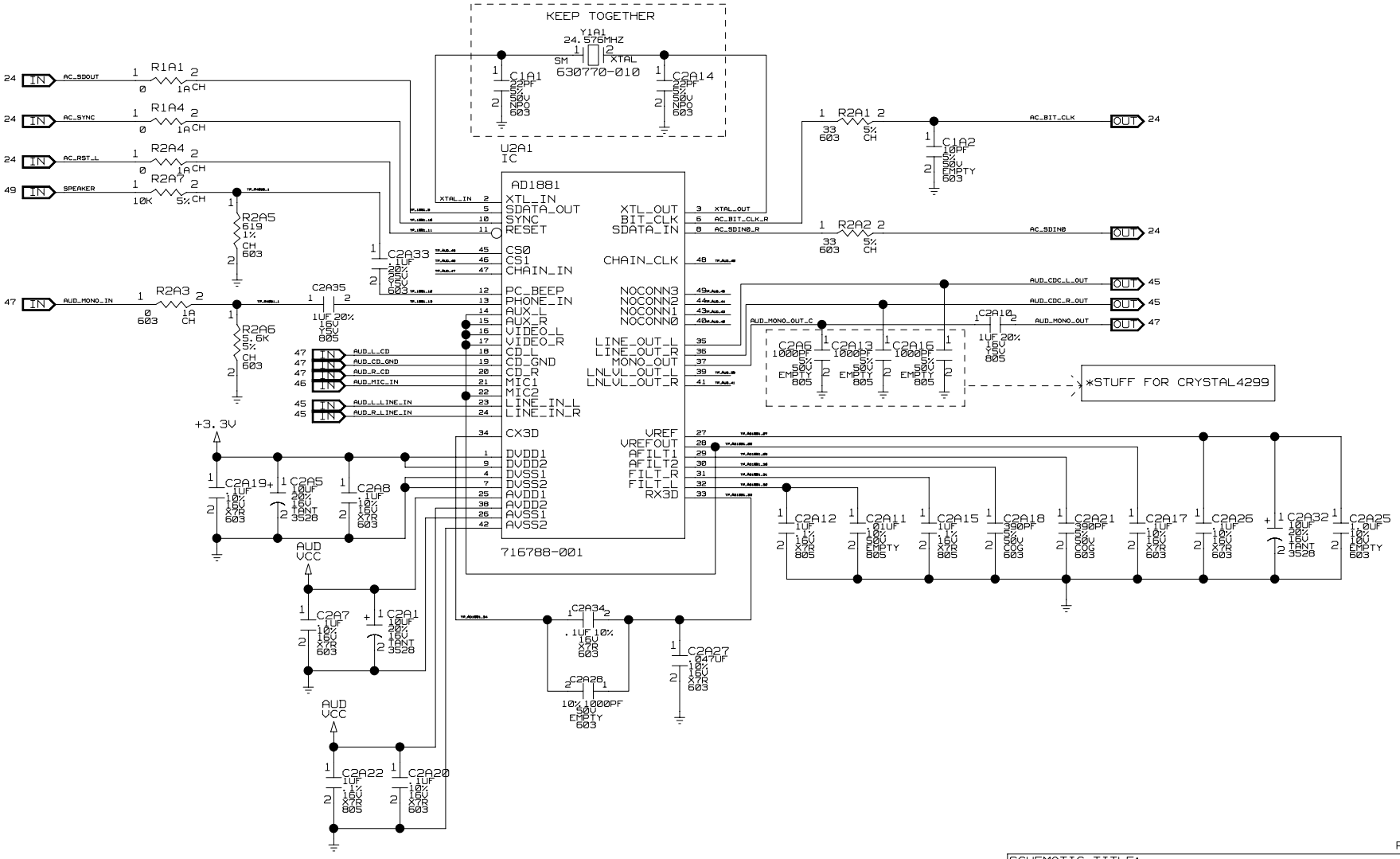


ROOM=USB_WAKE

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: WAKE ON USB	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:21 2001
	SHEET: 43

DRAWING

WAKE ON USB

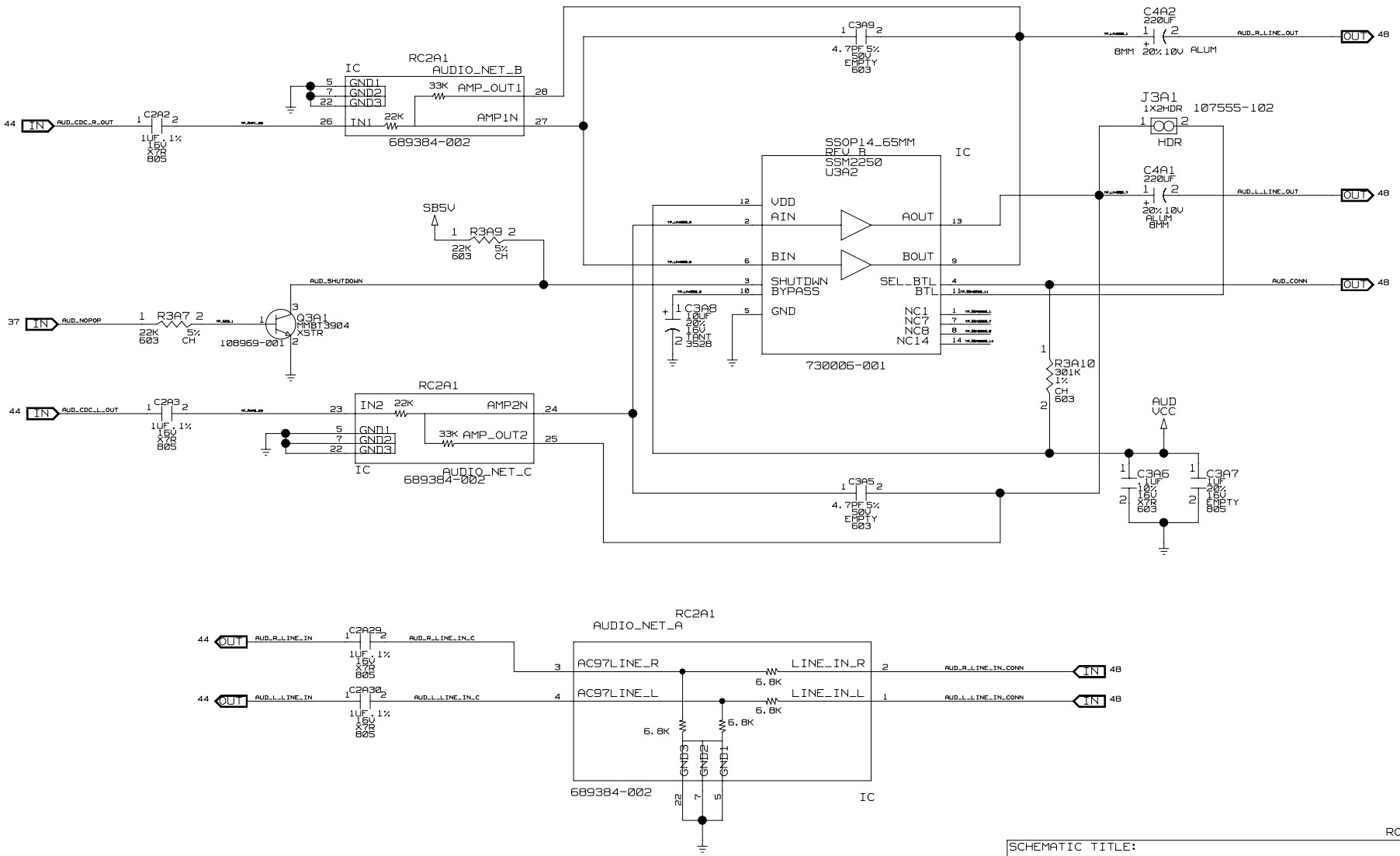


AD1881 AUDIO CODEC

DRAWING

ROOM=AUDIO

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: AD1881 AUDIO CODEC	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:18 2001
	SHEET: 44

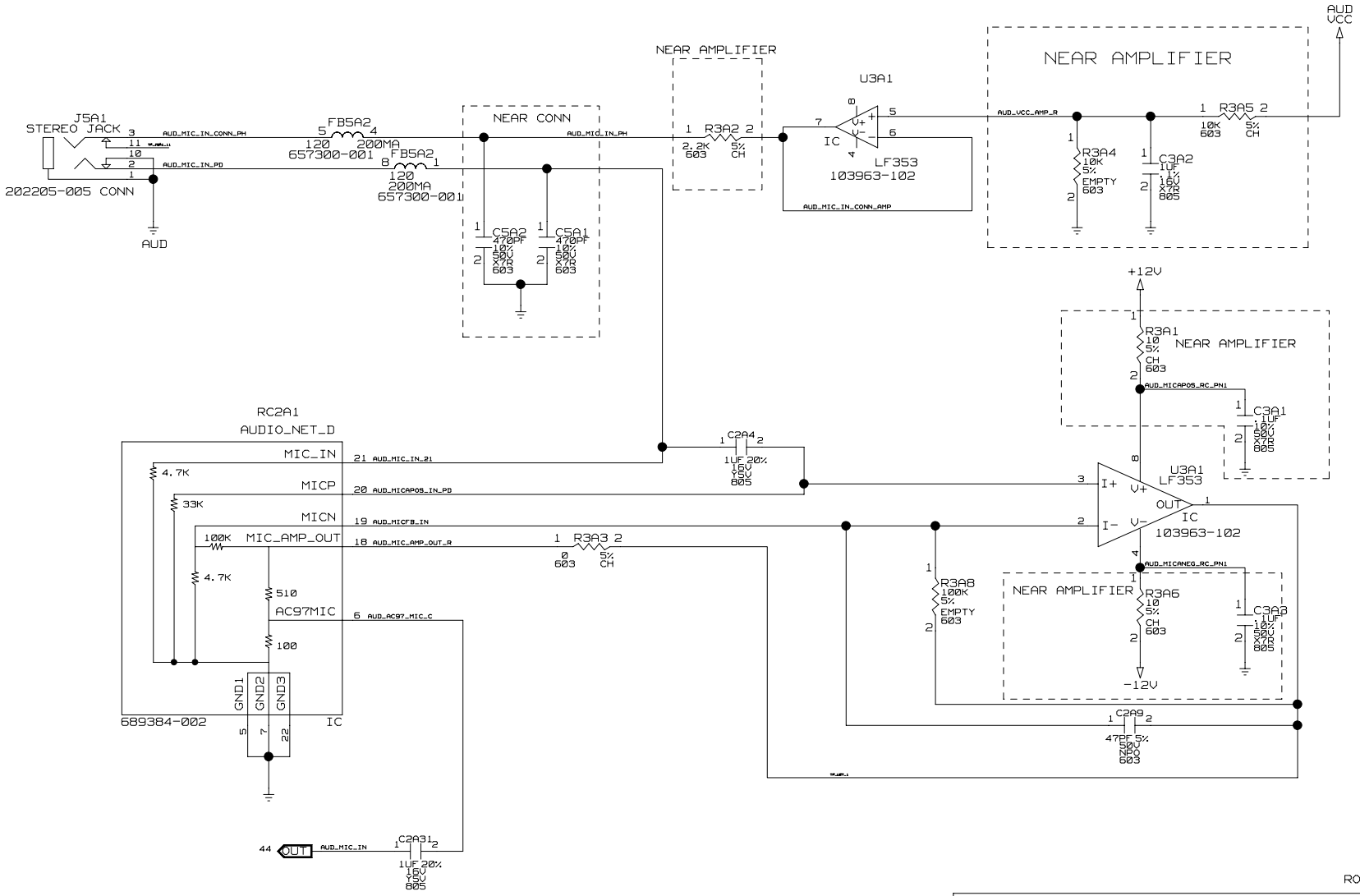


ROOM=AUDIO

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: LINE IN / OUT		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:12 2001	SHEET: 45

DRAWING

LINE IN / OUT

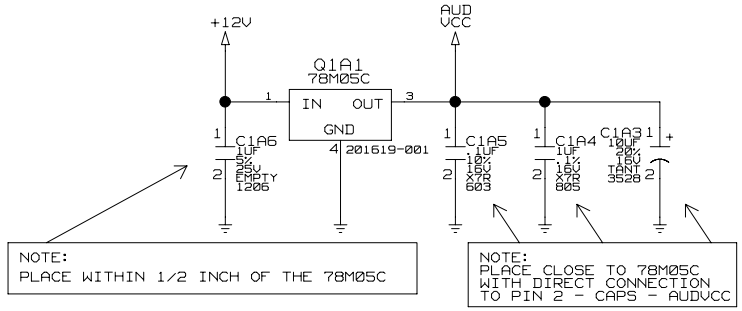


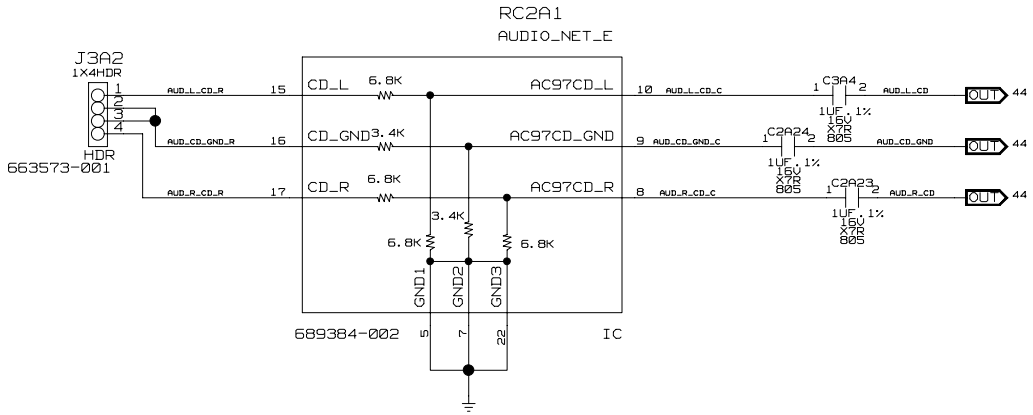
ROOM=AUDIO

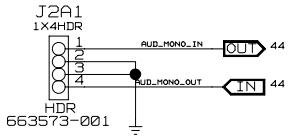
DRAWING

MICROPHONE IN

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: MICROPHONE IN	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:08 2001
	SHEET: 46





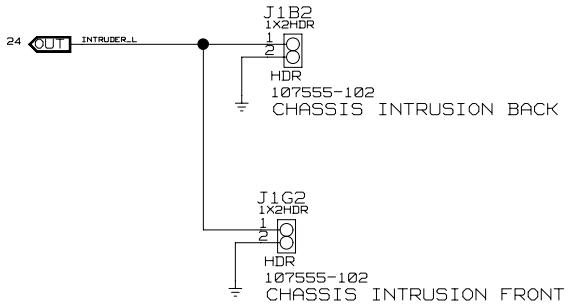


ROOM=AUDIO

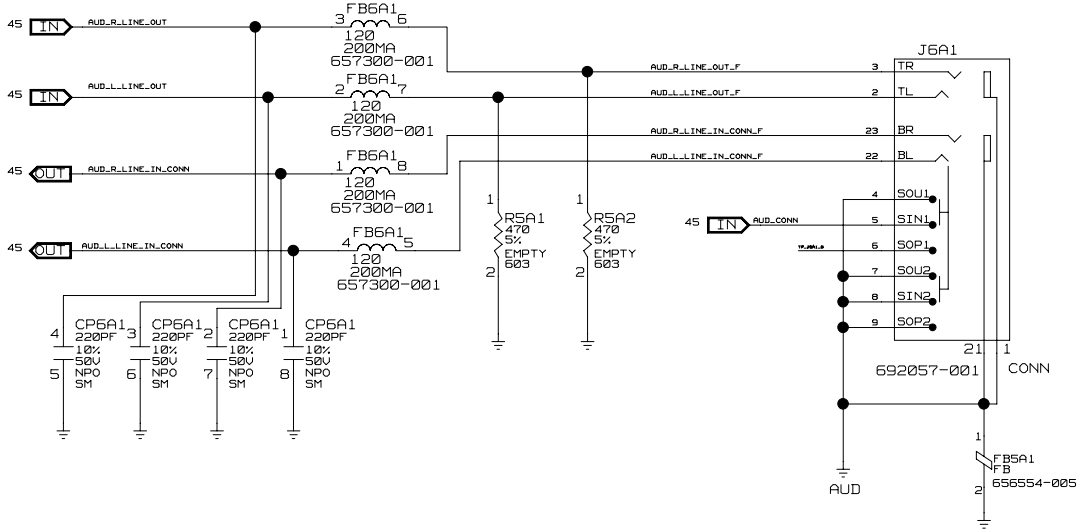
SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: AUDIO NET & VREG	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:03 2001
	SHEET: 47

DRAWING

AUDIO NET & VREG

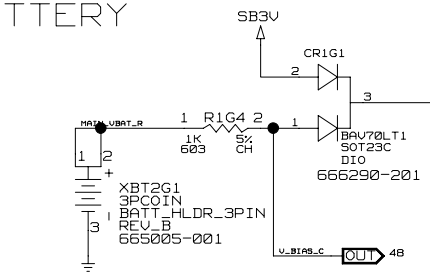


CHASSIS INTRUSION



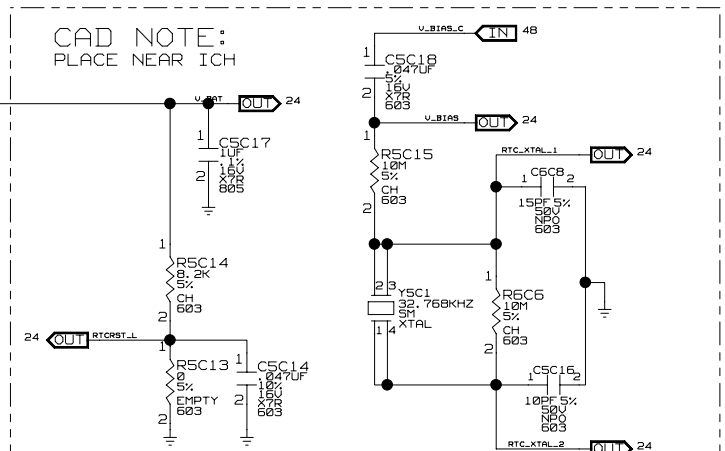
AUDIO CONNECTOR

BATTERY



CAD NOTE: DO NOT PLACE BATTERY NEAR MOUNTING HOLES, GROUND OR VIAS

ROOM=BATTERY



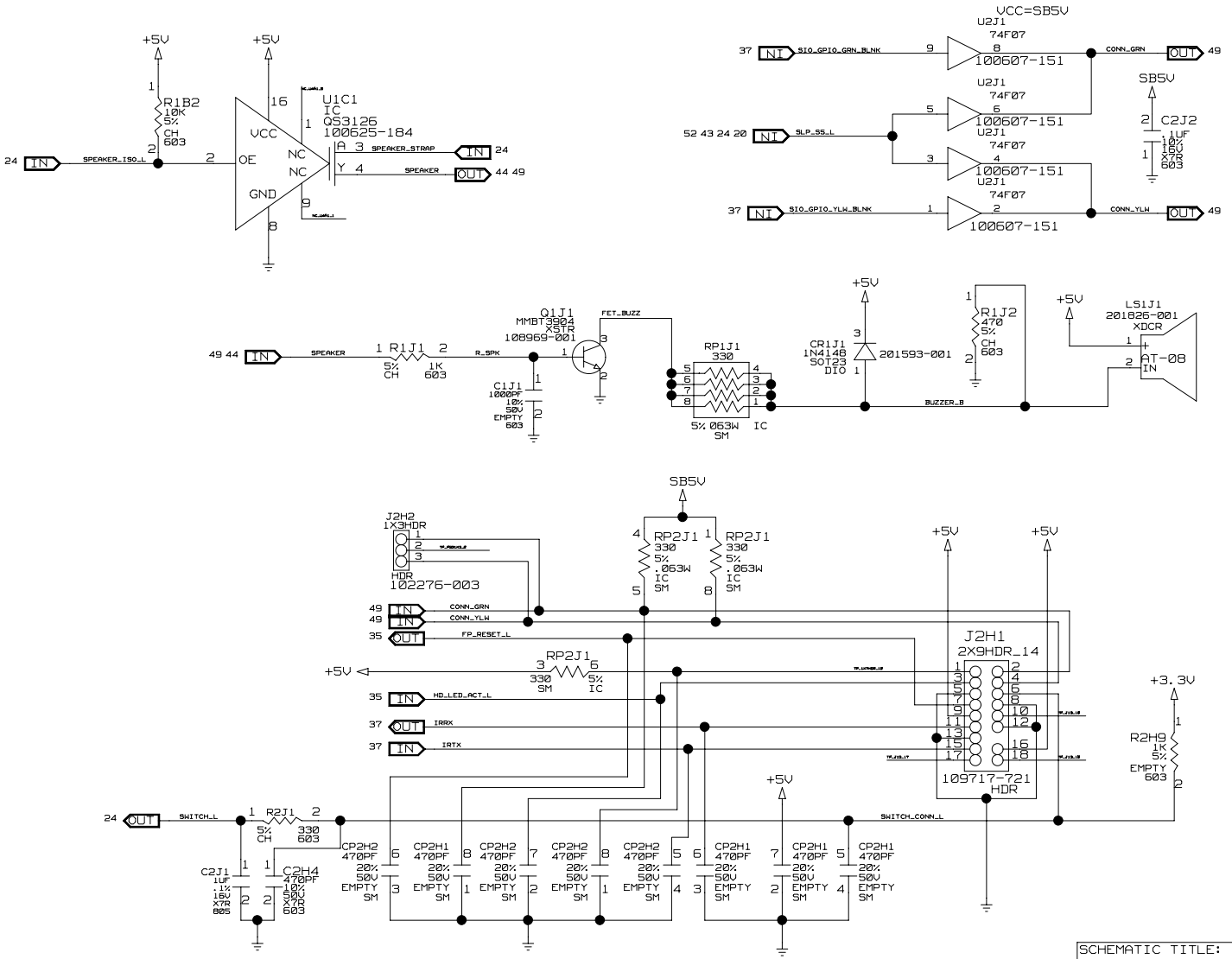
ROOM=STACKED AUDIO

ROOM=INTRUSION

DRAWING

CHASSIS INTRUSION, AUDIO AND BATTERY

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: CHASSIS INTRUSION & AUDIO	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:58 2001
	SHEET: 48



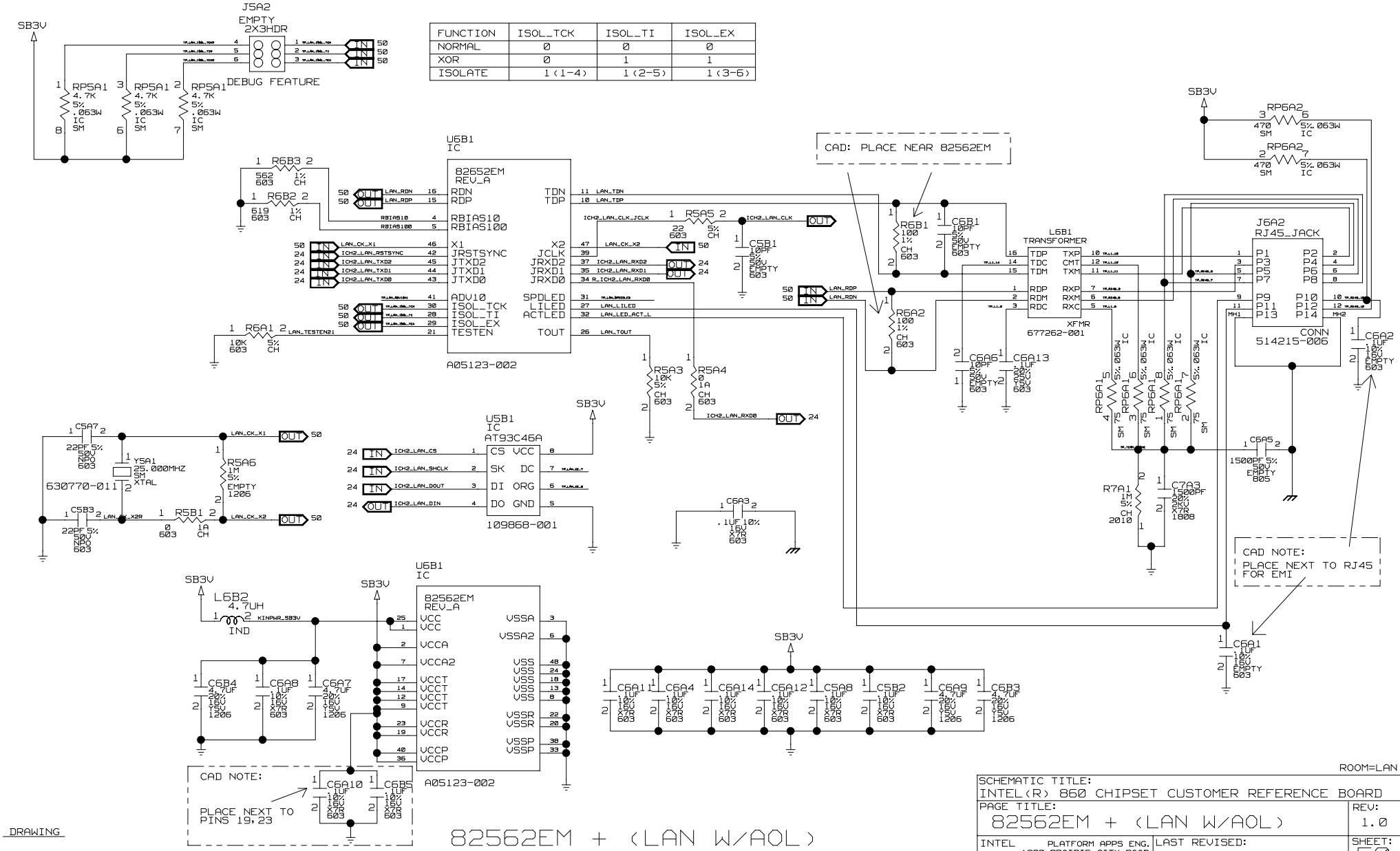
DRAWING

FRONT PANEL HEADERS / SPEAKER

ROOM=FRNT_PNL

ROOM=SPEAKER

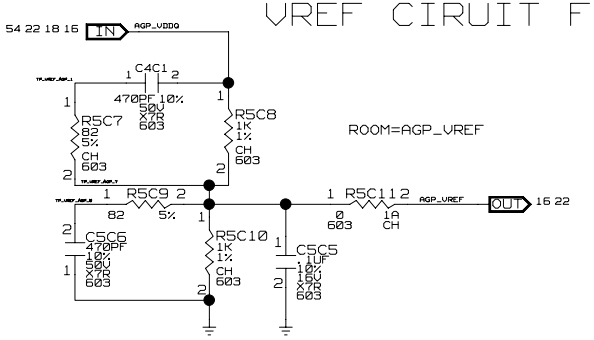
SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: FRONT PANEL HEADERS	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:53 2001
	SHEET: 49



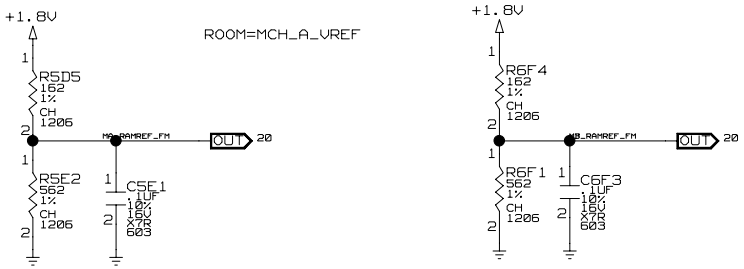
FUNCTION	ISOL_TCK	ISOL_TI	ISOL_EX
NORMAL	0	0	0
XOR	0	1	1
ISOLATE	1(1-4)	1(2-5)	1(3-6)

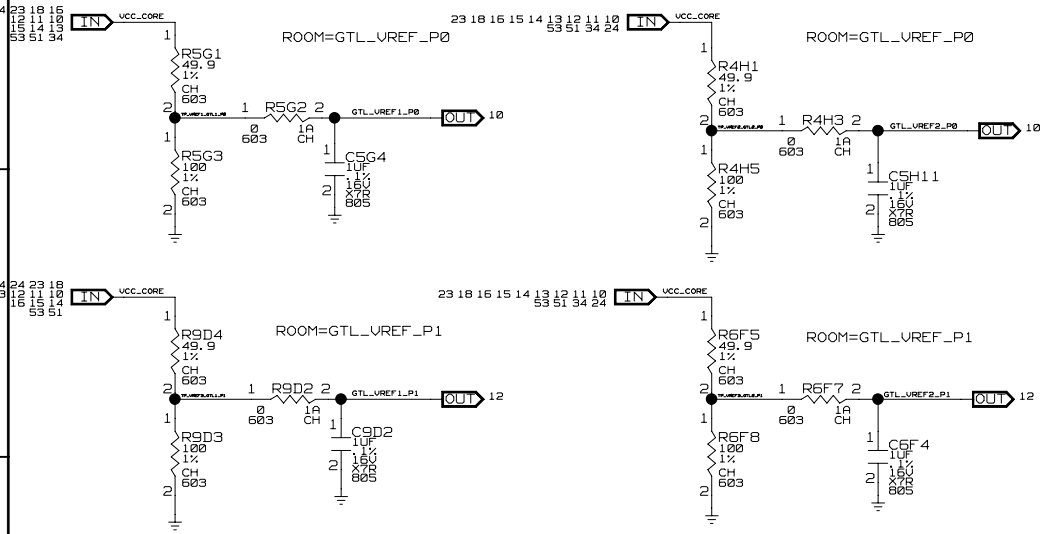
CR-51

VREF CIRUIT FOR AGP 4X



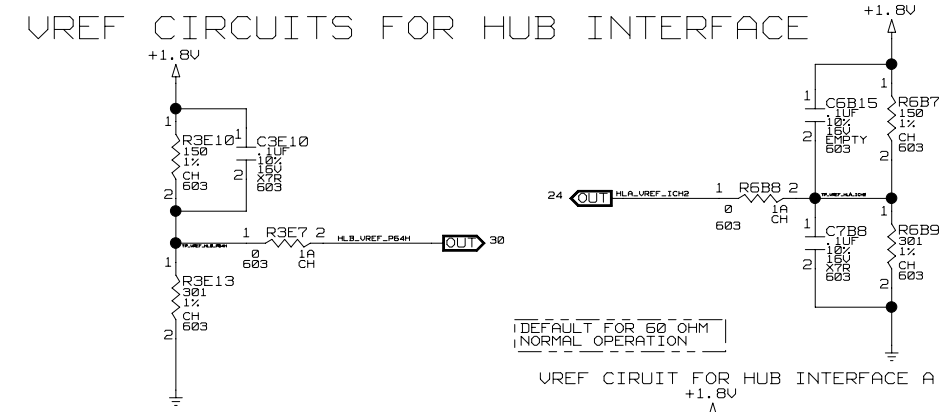
VREF CIRCUITS FOR RAMBUS





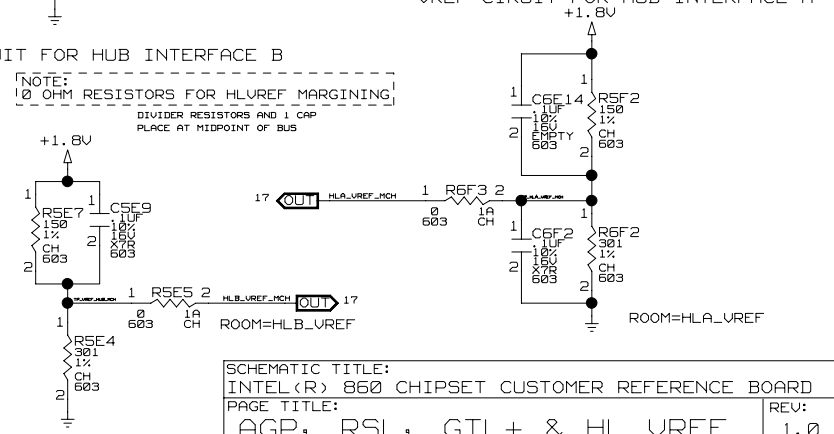
VREF CIRCUIT FOR GTL+

VREF CIRCUITS FOR HUB INTERFACE



VREF CIRUIT FOR HUB INTERFACE A

VREF CIRUIT FOR HUB INTERFACE B



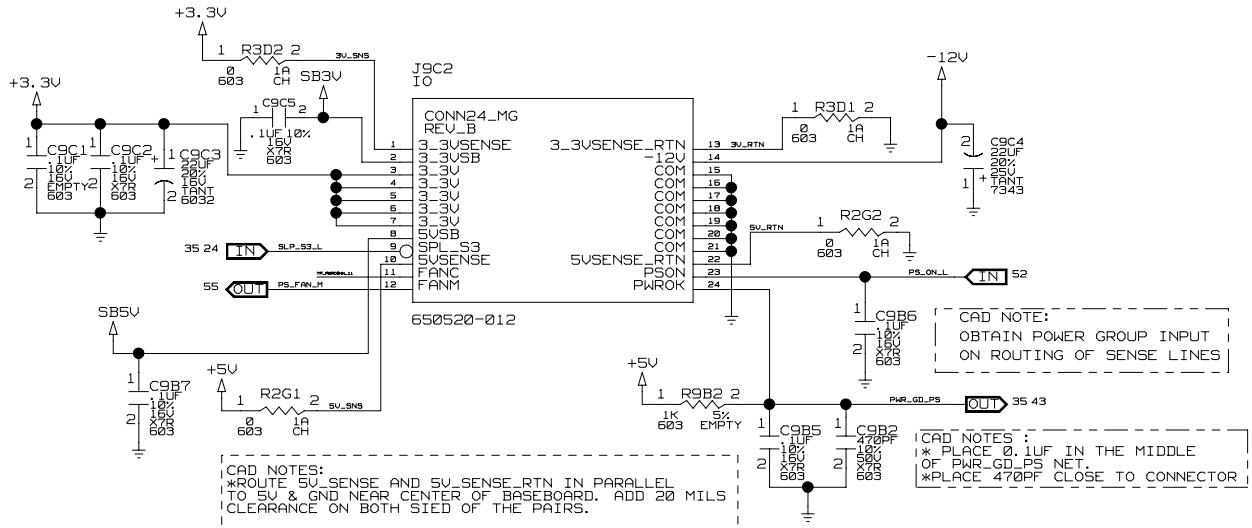
DRAWING

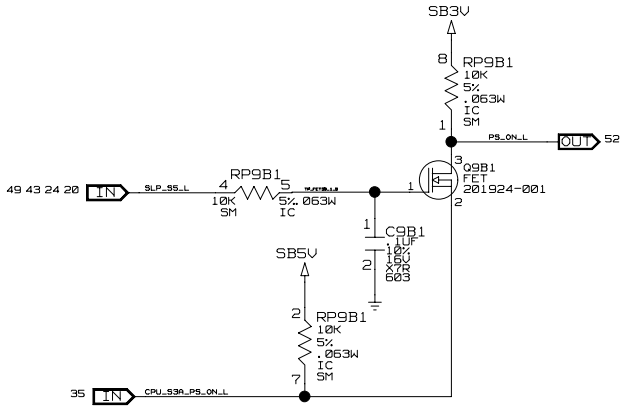
AGP, RSL, GTL+ & HUB LINK VREF CIRCUITS

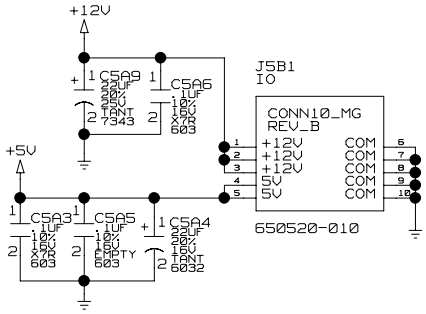
SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: AGP, RSL, GTL+ & HL VREF		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:42 2001	SHEET: 51

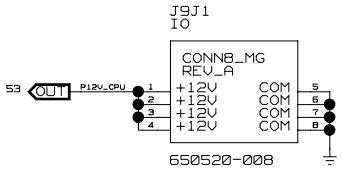
WTX PSU SIGNAL TABLE

PS_ON = 10K PULL UP TO 5VSB INTERNAL TO PSU
FAN_C = 10K PULL UP TO 5V INTERNAL TO PSU
SLEEP = 10 PULL UP TO 3.3V AUX INTERNAL TO PSU
PS_OK = 10K PULLUP TO 5V INTERNAL TO PSU









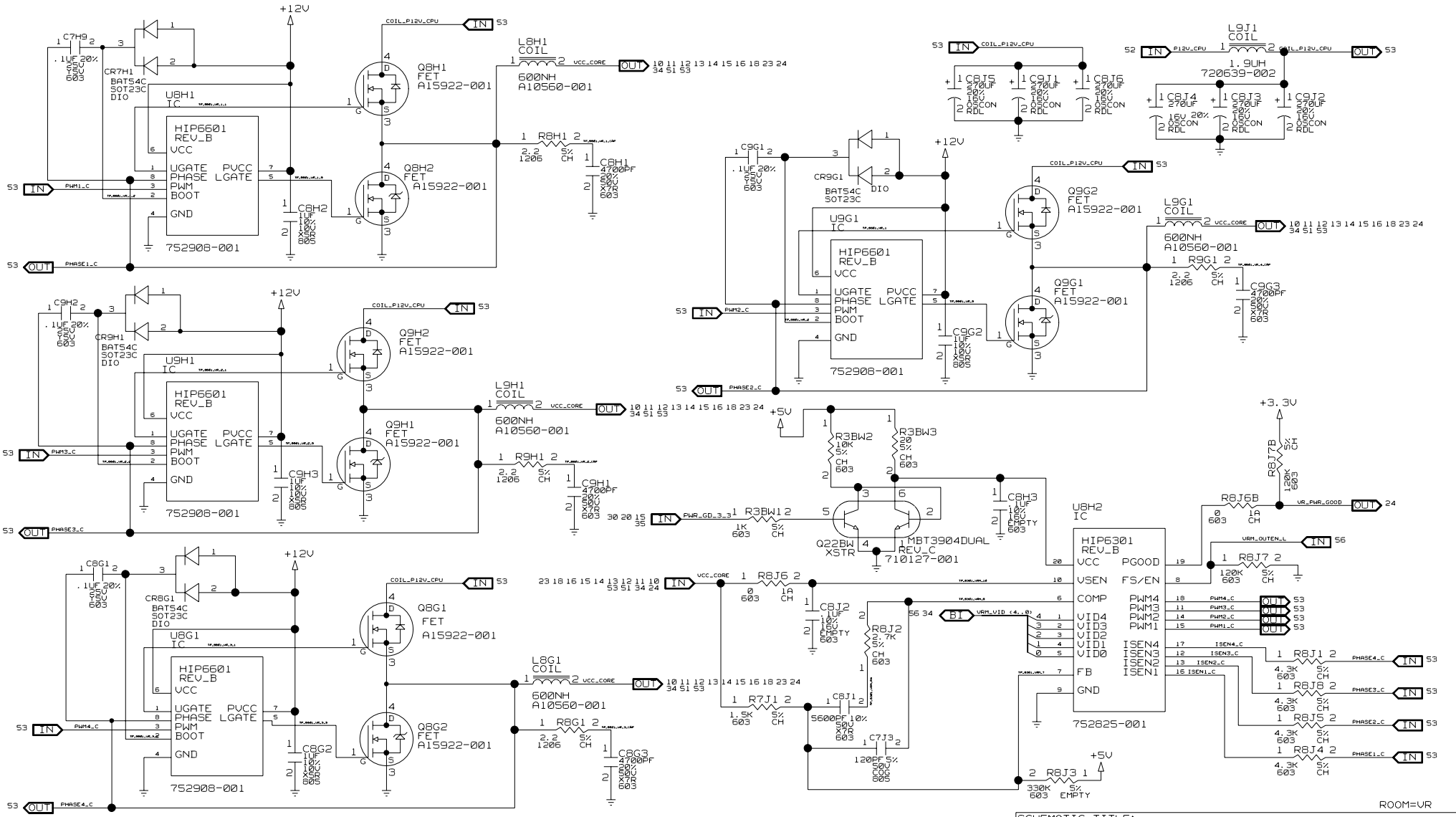
ROOM=POWER_HDR

ROOM=PWRCONN_BASE

DRAWING

POWER SUPPLY CONNECTORS

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: POWER SUPPLY CONNECTORS		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:37 2001	SHEET: 52



NOTE:
HEAT-SINK FOR VR IS IPN 701073-001
HEAT-SINK CLIP IS IPN XXXXXX-XXX

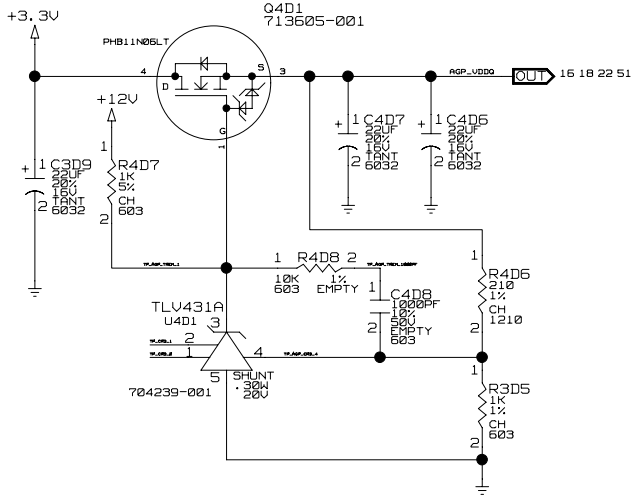
DRAWING

CPU VOLTAGE REGULATORS

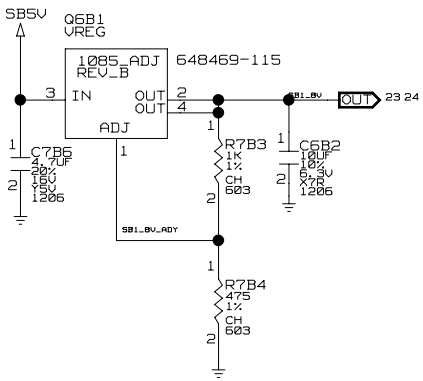
ROOM=VR

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: CPU VOLTAGE REGULATORS	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:31 2001
	SHEET: 53

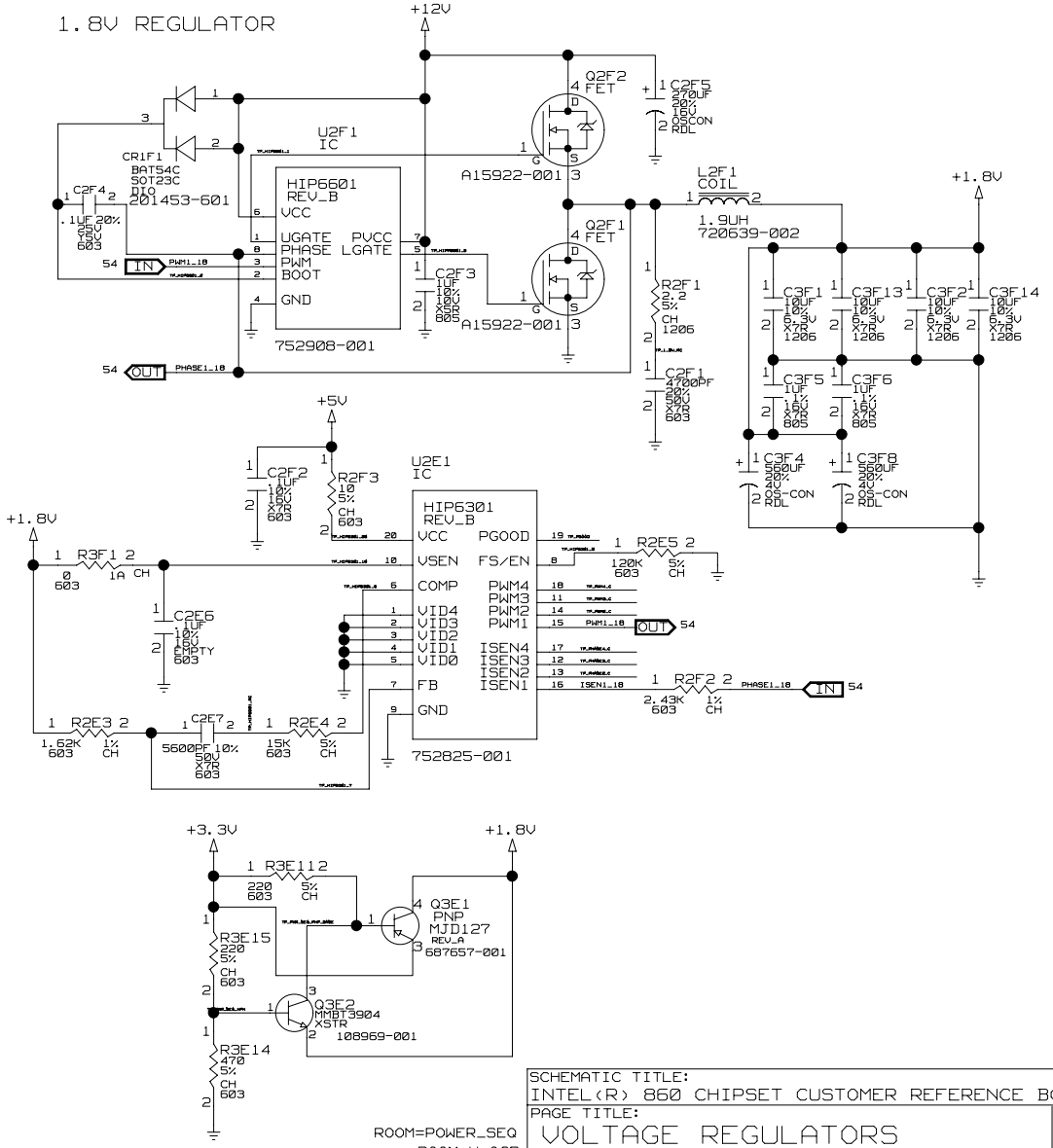
AGP PRO TERMINATION



STANDBY 1.8 V REGULATOR



1.8V REGULATOR



DRAWING

VOLTAGE REGULATORS

ROOM=POWER_SEQ
ROOM=V_AGP
ROOM=1_8VREG
ROOM=VREG_SB1.8V

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: VOLTAGE REGULATORS	REV: 1.0
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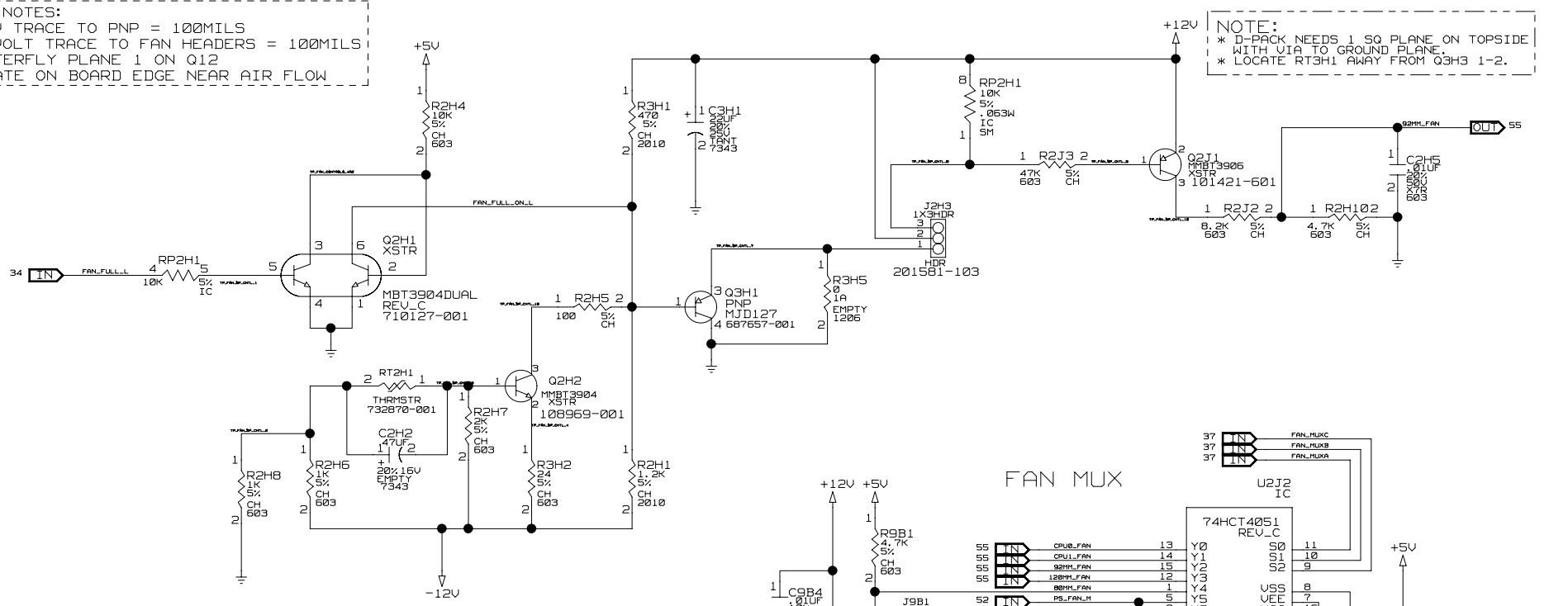
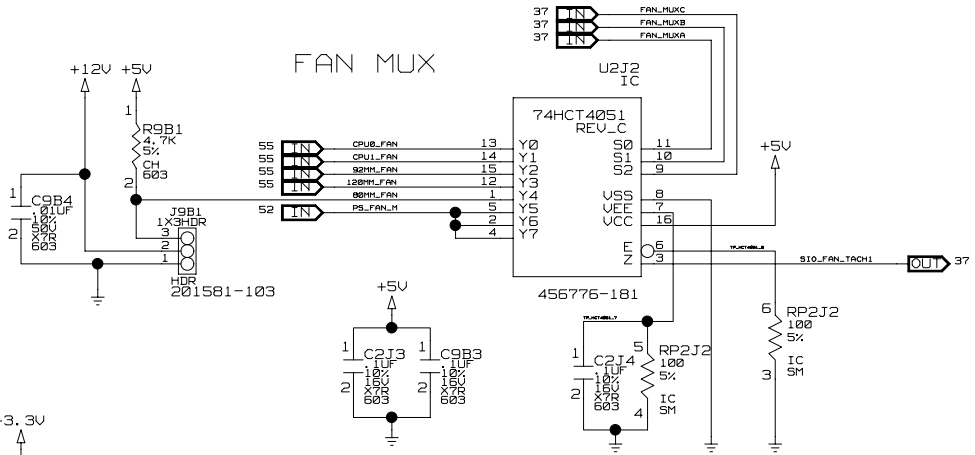
CR-55

CAD NOTES:
+12V TRACE TO PNP = 100MILS
12 VOLT TRACE TO FAN HEADERS = 100MILS
BUTTERFLY PLANE 1 ON Q12
LOCATE ON BOARD EDGE NEAR AIR FLOW

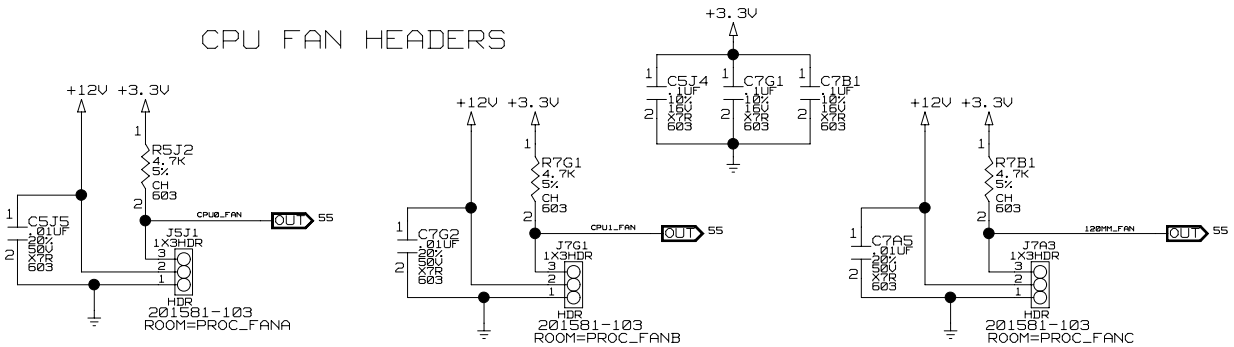
NOTE:
* D-PACK NEEDS 1 SQ PLANE ON TOPSIDE WITH VIA TO GROUND PLANE.
* LOCATE RT3H1 AWAY FROM Q3H3 1-2.



FAN MUX



CPU FAN HEADERS



DRAWING

FAN CONTROL

ROOM=FAN_CONTROL

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PAGE TITLE: FAN CONTROL	REV: 1.0
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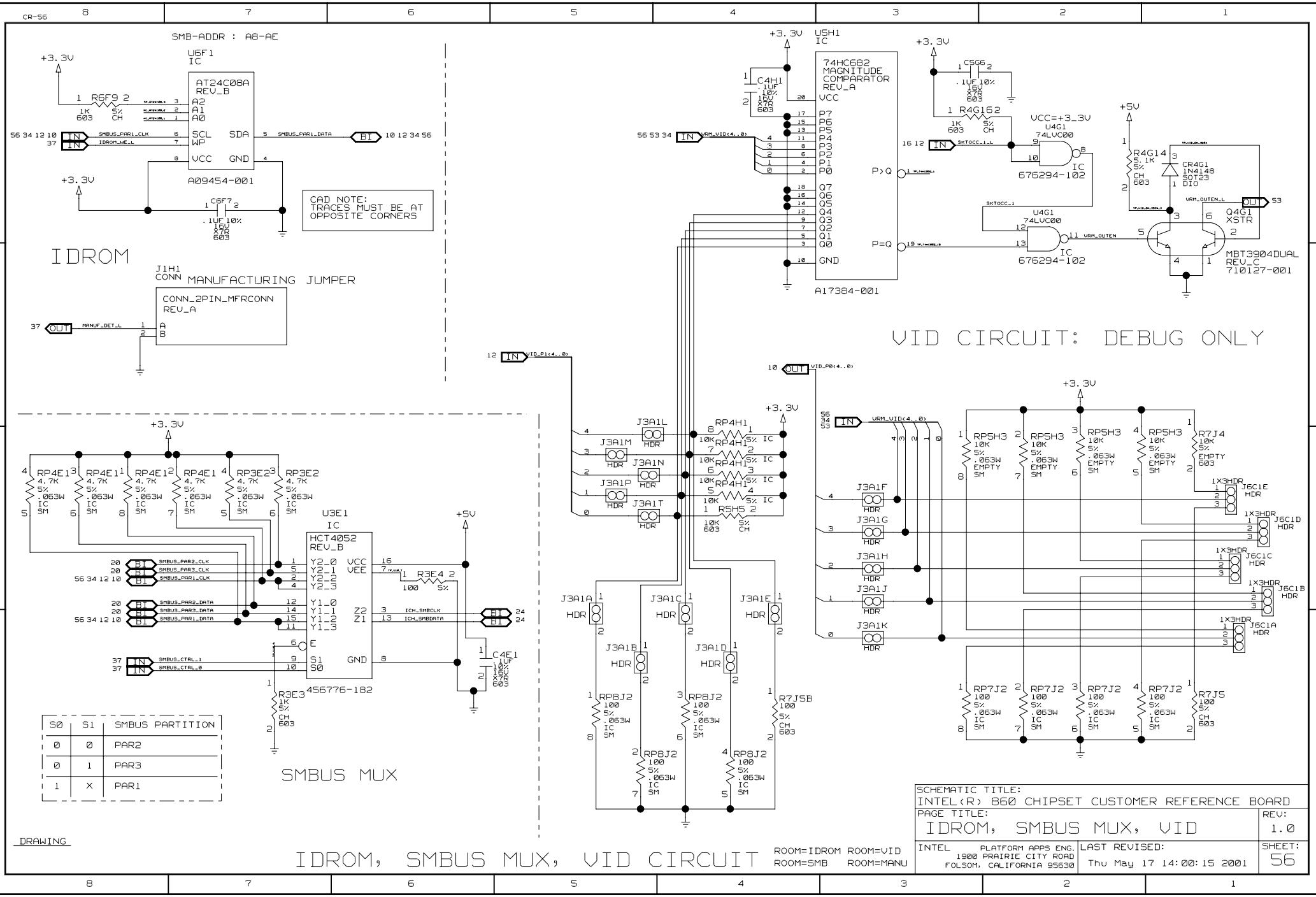
SMB-ADDR : A8-AE
U6F1
IC
AT24C08A
REV_B
A09454-001
IDROM
CAD NOTE:
TRACES MUST BE AT
OPPOSITE CORNERS
J1H1
CONN
MANUFACTURING JUMPER
CONN_2PIN_MFRCONN
REV_A
U5H1
IC
74HC682
MAGNITUDE
COMPARATOR
REV_A
A17384-001
VID CIRCUIT: DEBUG ONLY
MBT3904DUAL
REV_C
710127-001
SMBUS MUX
HCT4052
REV_B
456776-182
SMBUS_PAR1_CLK
SMBUS_PAR2_CLK
SMBUS_PAR3_CLK
SMBUS_PAR1_DATA
SMBUS_PAR2_DATA
SMBUS_PAR3_DATA
SMBUS_CTRL_1
SMBUS_CTRL_0
ICH_SMBCLK
ICH_SMBDATA
S0 S1 SMBUS PARTITION
0 0 PAR2
0 1 PAR3
1 X PAR1
IDROM, SMBUS MUX, VID CIRCUIT
ROOM=IDROM ROOM=VID
ROOM=SMB ROOM=MANU
DRAWING
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
IDROM, SMBUS MUX, VID
REV:
1.0
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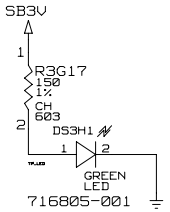
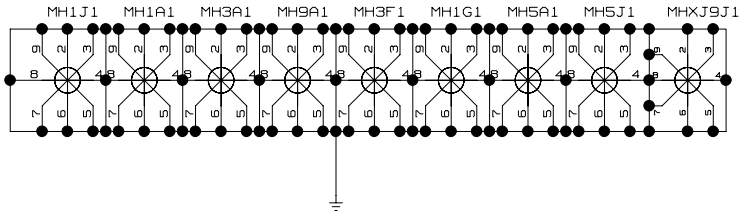
STANDBY LED



ROOM=LED



MOUNTING HOLES

DRAWING

VID JMPR'S MOUNTING HOLES, SB LED

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PAGE TITLE: VID JMPR MNT HOLE, SB LED		REV: 1.0
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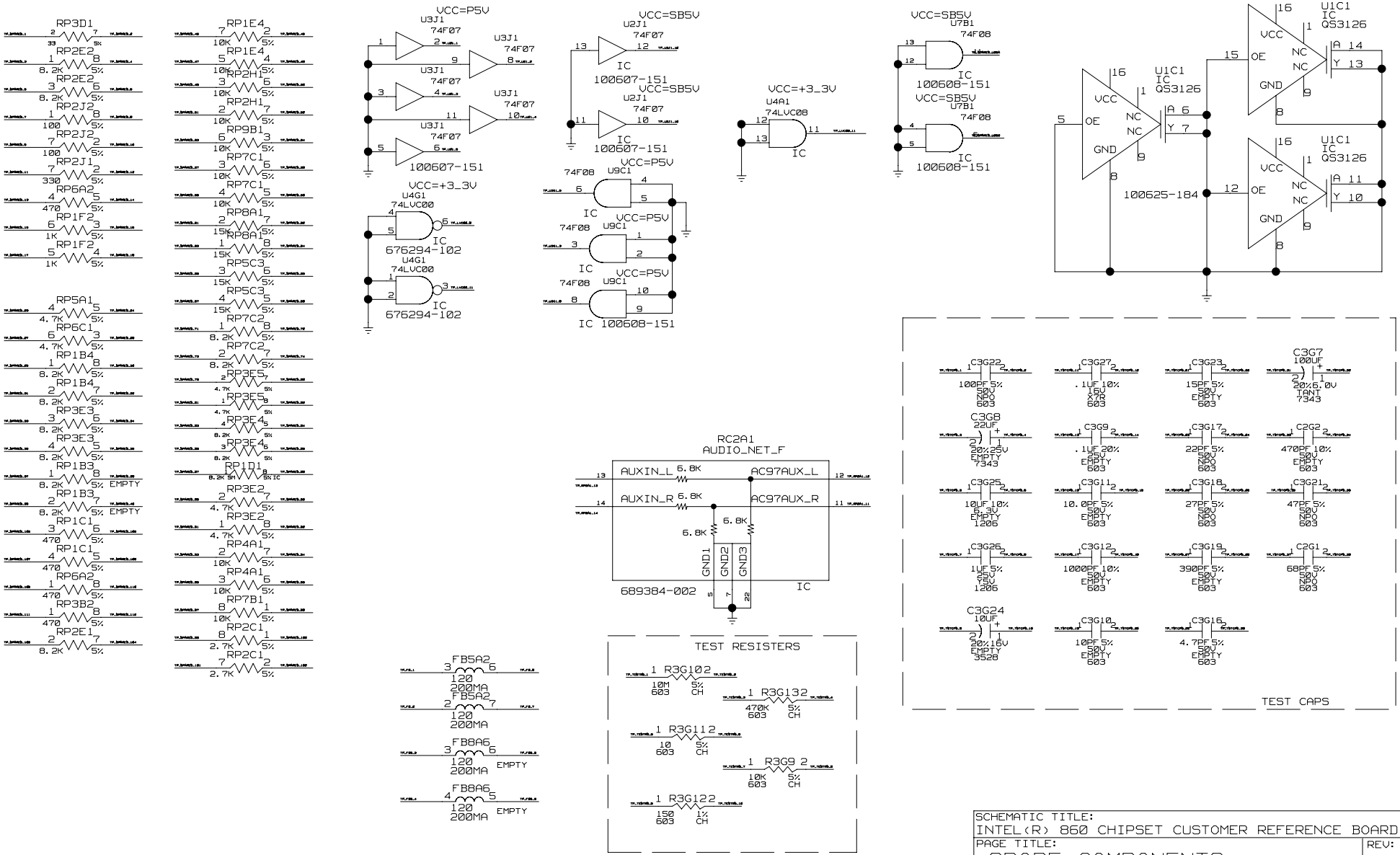

DRAWING

SPARE COMPONENTS

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