



Intel[®] Pentium[®] 4 Processor in 478-pin Package and Intel[®] 845G/845GL/845GV Chipset

Platform Design Guide

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Revision History

Rev. No.	Description	Date
-001	Initial Release.	May 2002
-002	Added 845GV chipset information. Minor edits throughout for clarity.	October 2002
-003	Updated section 14.3.1.1 to state that the 1.5 V rail must power up before or simultaneously with the 3.3 V rail.	September 2006

1 Introduction

This design guide has Intel design recommendations for systems based on the Intel® Pentium® 4 Processor in the 478-pin package, the Intel® 82845G/82845GL/82845GV GMCH, and the Intel® ICH4. Design issues such as thermal considerations should be addressed using specific design guides or application notes for the processor, the GMCH, and the 82801DB ICH4.

These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into two categories:

- **Design Recommendations:** items based on Intel’s simulations and lab experience to date and are strongly recommended, if not necessary, to meet the timing and signal quality specifications.
- **Design Considerations:** suggestions for platform design that provide one way to meet the design recommendations. Design considerations are based on the reference platforms designed by Intel. They should be used as an example, but may not be applicable to particular designs.

Chapters 1 through 18 provide design guidelines for the 845G chipset platform. Chapter 19 provides design guidelines for the 845GL and 845GV chipset platforms.

Note: In this document “processor” and “Intel® Pentium® 4 processor” refer to the Intel® Pentium® 4 Processor in the 478-pin package.

Note: The guidelines recommended in this document are based on experience and simulation work completed by Intel while developing systems with the Intel® Pentium® 4 Processor in the 478-pin package, and 845G, 845GL, 845GV chipsets. This work is ongoing, and the recommendations and considerations are subject to change.

Platform schematics are provided in Appendix A as a reference for board designers. While the schematics may cover a specific design, the core schematics remain the same for most platforms. The schematic set provides a reference schematic for each platform component, and common system board options. Additional flexibility is possible through other permutations of these options and components.

1.1 Terminology

This section defines conventions and terminology that will be used throughout this document.

Table 1. Platform Conventions and Terminology

Convention/ Terminology	Definition
ADD Card	AGP Digital Display Card provides digital display options for 82845G/82845GL/82845GV GMCH when plugged into an AGP connector.
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGP	Accelerated Graphics Port. Refers to the AGP/PCI interface that is in the GMCH. It supports a 1.5 V 66/266 MHz component.
AGTL+	The Processor System Bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors that provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Corner	This term describes how a component performs when all parameters that could impact performance are adjusted simultaneously to have the best or worst impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. Performance of an electronic component may change as a result of (including, but not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the “slow” corner means having a component operating at its slowest, weakest drive strength performance. Similar discussion of the “fast” corner means having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bind the extremes between slowest, weakest performance and fastest, strongest performance.
Crosstalk	<p>The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks.</p> <p>Backward Crosstalk – coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal.</p> <p>Forward Crosstalk – coupling that creates a signal in a victim network that travels in the same direction as the aggressor’s signal.</p> <p>Even Mode Crosstalk – coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching.</p> <p>Odd Mode Crosstalk – coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.</p>
DDR	Double Data Rate SDRAM
DVO	Digital Video Out port. This port is used for the GMCH digital display channel. The GMCH chipset has two DVO ports that are multiplexed with AGP.

Convention/ Terminology	Definition
Flight Time	<p>Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, <i>flight time</i> is defined to be:</p> <p>Time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; e.g., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings.</p> <p>Maximum and Minimum Flight Time – Flight time variations can be caused by many different variables. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects.</p> <p>Maximum flight time is the largest acceptable flight time a network will experience under all variations of conditions.</p> <p>Minimum flight time is the smallest acceptable flight time a network will experience under all variations of conditions.</p>
FWH	Firmware Hub
GMCH	The Graphics-Memory Controller Hub component that contains the processor interface, DRAM controller, AGP interface and an integrated 3D/2D display core. It communicates with the ICH4 through the hub interface
GTL+	GTL+ is the bus technology used by the Intel® Pentium® Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) bus technology.
Hub Interface	Proprietary Hub interconnect that ties the GMCH to the ICH4.
ICH4	The I/O Controller Hub component that contains various I/O functions. It communicates with the GMCH through the hub interface.
IGD	Internal/Integrated Graphics Device. Graphics device integrated into the GMCH
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
LPC	Low Pin Count interface.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	The distance between one agent pin and the corresponding agent pin at the far end of the bus.
Overshoot	Maximum voltage observed for a signal at the device pad.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulation.
PSB	Processor System Bus. This bus is the connection between the GMCH and the processor.

Convention/ Terminology	Definition
Pin	The contact point of a component package to the traces on a substrate, like the system board. Signal quality and timings can be measured at the pin.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena.
SDR	Single Data Rate SDRAM
SDRAM	Synchronous Dynamic Random Access Memory
System Bus	The System Bus is the microprocessor bus of the Intel® Pentium® 4 Processor in the 478 Pin Package. It may also be termed “system bus” in implementations where the System Bus is routed to other components. The P6 bus was the microprocessor bus of the Intel® Pentium® Pro, Intel® Pentium II, and Intel® Pentium III processors. The system bus is not compatible with the P6 bus.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
SSO	Simultaneous Switching Output (SSO) effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or “push-out”), or a decrease in propagation delay (or “pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Test Load	Intel uses a 50 Ω test load for specifying its components.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	Minimum voltage observed for a signal to extend below VSS at the device pad.
USB	Universal Serial Bus
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
VREF Guardband	A guardband defined above and below VREF to provide a more realistic model accounting for noise such as VTT and VREF variation.

1.2 Related Documentation

Reference the following documents or models for more information. All Intel issued documentation revision numbers are subject to change, and the latest revision should be used. The specific revision numbers referenced should be used for all documents not released by Intel. Contact your field representative for information on how to obtain Intel issued documentation.

Document	Document Number/Source
<i>Intel® 845G/845GL/845GV Chipset Datasheet</i>	290746
<i>AGP Design Guide Revision 1.5</i>	http://developer.intel.com/technology/agp/downloads/DesignGuide062601.htm
<i>Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet</i>	249887
<i>Intel® Pentium® 4 Processor with 512 KB L2 Cache on .13 Micron Process Datasheet</i>	http://developer.intel.com/design/Pentium4/datashts/
<i>Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines</i>	http://developer.intel.com/design/pentium4/guides/249889.htm
<i>Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet</i>	290744
<i>Intel® 82801DB I/O Controller Hub 4 (ICH4): Thermal and Mechanical Design Guidelines</i>	298651
<i>Intel® 845G/845GL/845GV Chipset Thermal and Mechanical Design Guidelines</i>	298655
<i>Intel® Pentium® 4 Processor in the 478 pin package Processor Signal Integrity Models</i>	Contact Intel Field Representative
<i>Intel® Pentium® 4 Processor VR Down Design Guidelines</i>	249891
<i>mPGA478 Socket Design Guidelines</i>	249890
<i>Intel® PC SDRAM Unbuffered DIMM Specification</i>	http://developer.intel.com/technology/memory/pcsdram/spec/index.htm
<i>Intel® PC SDRAM Specification</i>	http://developer.intel.com/technology/memory/pcsdram/spec/index.htm
<i>Accelerated Graphics Port Interface Specification</i>	http://www.agpforum.org/
<i>Low Pin Count Interface Specification</i>	http://www.intel.com/design/chipsets/industry/lpc.htm
<i>PCI Local Bus Specification</i>	www.pcisig.com
<i>PCI-PCI Bridge Specification</i>	www.pcisig.com
<i>PCI Bus Power Management Interface Specification</i>	www.pcisig.com
<i>Universal Serial Bus Revision 2.0, Specification</i>	http://www.usb.org/developers/docs.html
<i>Advanced Configuration and Power Interface Specification (ACPI), Revision 1.0b</i>	http://www.teleport.com/~acpi/
<i>Communication and Networking Riser (CNR) Specification Revision 1.2</i>	http://developer.intel.com/technology/cnr/index.htm

Document	Document Number/Source
<i>82562ET 10/100 Mbps Platform LAN Connect (PLC) Product Datasheet</i>	Contact Intel Field Representative
<i>ITP700 Debug Port Design Guide</i>	http://developer.intel.com/design/Xeon/guides/249679.htm
<i>82562ET LAN on Motherboard Design Guide</i>	AP 414
<i>82562ET/EM PCB Design Platform LAN Connect</i>	AP-412
<i>CNR Reference Design Application Note</i>	AP-418
<i>82540EM Gigabit Ethernet Controller Preliminary Datasheet and Hardware Design Guide</i>	10441
<i>Intel® 82562EX/EZ 10/100 Mbps Platform LAN Connect (PLC) Networking Silicon Datasheet</i>	10522
<i>AC '97 Specification, Revision 2.2</i>	http://developer.intel.com/ial/scalableplatforms/audio/index.htm#97spec/
<i>Intel® Pentium® 4 Processor VR-Down Design Guidelines</i>	http://developer.intel.com/design/Pentium4/guides/249891.htm
<i>JEDEC® 184-Pin Unbuffered DDR DIMM Specification</i>	
<i>JEDEC® Double Data Rate (DDR) SDRAM Specification</i>	
<i>Intel® JEDEC® DDR 200 Registered DIMM Specification Addendum</i>	http://www.intel.com/technology/memory/pcsdram/spec/ddr200_dimm_rev09.htm
<i>ATA/ATAPI-6 Standard</i>	
<i>Real Time Clock (RTC) Accuracy and Considerations Under Test</i>	Application Note AP-728
<i>CK-408 Clock Synthesizer/Driver Specification</i>	Contact Intel Field Representative
<i>Advanced Configuration and Power Interface Specification (ACPI) Revision 2.0a</i>	http://www.acpi.info/spec.htm
<i>845G Chipset Platform DDR System Memory Trace Length Calculator</i>	Contact Intel Field Representative
<i>SMBus Interface Power Management, Revision 1.1</i>	Contact Intel Field Representative

1.3 System Overview

The Intel® Pentium® 4 Processor in the 478-pin package with the GMCH and the ICH4 delivers a stable mainstream desktop platform solution. The processor and the chipset support the System Bus Protocol.

The GMCH component provides the processor interface, system memory interface, Hub Interface, AGP interface, and an integrated graphics device with analog and digital display ports. This product provides flexibility and scalability in graphics subsystem performance. Competitive internal graphics may be scaled with the addition of an AGP interface card or an ADD card.

The ICH4 integrates a Universal Serial Bus 2.0 controller, Ultra ATA/100 controller, Low Pin Count interface, Firmware Hub Flash BIOS interface controller, PCI interface controller, integrated LAN, AC'97 digital controller, and a Hub Interface for communication with the GMCH.

An ACPI compliant 845G platform can support the *Full-On (S0)*, *Stop Grant (S1)*, *Suspend to RAM (S3)*, *Suspend to Disk (S4)*, and *Soft-Off (S5)* power management states. Through the use of an appropriate LAN connect, the chipset also supports *Wake-On LAN** for remote administration and troubleshooting. The use of AC'97 allows the OEM to use *software configurable AC'97* audio and modem coder/decoders (codecs).

The chipset architecture also enables a security and manageability infrastructure through the Firmware Hub (FWH) component.

1.3.1 Intel® 845G Chipset

The 845G chipset contains two *core* components designed for the desktop platform: the 82845G GMCH and the 82801DB Intel® I/O Controller Hub 4 (ICH4). These components are interconnected via an Intel proprietary interface called Hub Interface. The Hub Interface is designed into the 845G chipset to provide an efficient, high bandwidth communication channel between the GMCH and the ICH4.

1.3.2 Intel® Graphics Memory Controller Hub (GMCH)

The GMCH is available in a 760 ball FCBGA package, and has the following functionality:

- Supports 2 DIMMS of either SDR-SDRAM (PC133) or DDR-SDRAM (DDR200/266)
- AGTL+ host bus with integrated termination supporting 32-bit host addressing
- 1.5 V AGP interface with 4x SBA/data transfer and 2x/4x fast write capability – multiplexed with DVO ports
- 8-bit, 66 MHz 4x Hub Interface to the ICH4
- IGD with analog and digital display ports

1.3.2.1 Packaging/Power

- 37.5 mm x 37.5 mm 760 ball FCBGA package with 1mm ball pitch
- 1.5 Vcore with 1.5 V, 2.5 V, 3.3 V and AGTL+ I/O

1.3.2.2 Processor System Bus

- Supports single processor
- Processor packaging: mPGA 478 package
- Supports 400/533 MHz System Bus
- System Bus interrupt delivery
- Supports 32-bit addressing for access to 4 GB memory
- Supports AGTL+ on-die termination

1.3.2.3 System Memory Interface

- Supports one 64-bit wide SDR SDRAM or DDR SDRAM data channel
- Available bandwidth up to 1 GB/s (SDR), and 2.1 GB/s (DDR266)
- Configurable to support either an SDR board or a DDR board
- Supports 64 Mb, 128 Mb, 256 Mb, and 512 Mb SDRAM technologies
- Supports only x8 and x16 SDRAM devices with 4-banks
- Does not support ECC functionality
- Registered DIMMs not supported
- Supports unbuffered non-ECC DIMMs only
- Up to 16 simultaneously open pages (4 per row, 4 rows maximum)
- SPD (Serial Presence Detect) scheme for DIMM detection
- Suspend-to-RAM support using CKE

Double Data Rate (DDR) SDRAM Configuration

- Up to 2.0 GB of 200 MHz or 266 MHz DDR SDRAM
- Supports up to 2 DDR DIMMs, single-sided and/or double-sided
- Supports DDR 200/266 unregistered 184-pin non-ECC DDR SDRAM DIMMs
- Supports configurations defined in the JEDEC[®] DDR DIMM specification only
- Does not support double-sided x16 DDR DIMMs
- Supports Selective Command-Per-Clock (selective CPC) Accesses

Single Data Rate (SDR) SDRAM Configuration

- Up to 2.0 GB of 133 MHz SDR SDRAM
- Supports up to 2 SDR DIMMs, single-sided and/or double-sided
- Supports PC133 unregistered 168-pin non-ECC SDR SDRAM DIMMs
- Does not support PC100
- Does not support mixed-mode / uneven double-sided SDR DIMMs
- Supports 3.3 V SDR DIMM configurations only

1.3.2.4 Graphics Interface

Integrated Graphics Controller

- Integrated 2D/3D graphics accelerator
- 256 bit graphics core
- Texture mapped 3D with point sampled, Bilinear, Trilinear, and Anisotropic filtering
- Hardware setup with support for strips and fans
- Hardware motion compensation assist for software MPEG/DVD decode
- Digital Video Out (DVO) ports add support for digital displays and TV-out
- Integrated 350 MHz RAMDAC

Accelerated Graphics Port (AGP) Interface

- Supports a single, 1.5 V only, AGP 2.0 compliant device
- High priority access support
- Delayed transaction support for AGP reads that cannot be serviced immediately
- AGP semantic traffic to the DRAM is not snooped on the PSB and is therefore not coherent with the CPU caches
- AGP interface multiplexed with 2 DVO ports
- Supports ADD cards

1.3.2.5 Hub Interface

- 1.5 V operation; 266 MB/s point-to-point 8-bit Hub Interface to the ICH4
- 66 MHz base clock

1.3.3 Intel® 82801DB I/O Controller Hub 4 (ICH4)

The ICH4 provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many I/O functions. The ICH4 integrates:

- Upstream Hub Interface for access to the GMCH
- 2 channel Ultra ATA/100 Bus Master IDE controller
- 6 USB 2/1.1 ports
- I/O APIC
- SMBus 2.0 controller
- FWH interface
- LPC interface
- AC'97 2.2 interface
- PCI 2.2 interface
- Integrated System Management Controller
- Integrated LAN Controller

The ICH4 also contains the arbitration and buffering necessary to ensure efficient utilization of these interfaces.

1.3.3.1 Packaging/Power

- 31 mm x 31 mm 421 BGA package
- 1.5 V core, 1.5 V standby, and 3.3 V standby with 1.5 V and 3.3 V I/O

1.3.3.2 Expanded USB Support

- 3 UHCI Host Controllers that includes a root hub with two separate USB ports each, for a total of six legacy USB ports
- 1 EHCI Host Controller that includes a root hub that supports up to six USB 2.0 ports
- Supports a maximum of 6 USB ports at any given time. The connection to either a UCHI or the EHCI is dynamic and dependent on the USB device capability.

1.3.3.3 Integrated LAN Controller

- WfM 2.0 Compliant
- Interface to discrete platform LAN connect component
- 10/100 Mbit/sec Ethernet support

1.3.3.4 Ultra ATA/100 Support

- Ultra ATA/100/66/33, BMIDE and PIO modes
- Independent timing of up to 4 drives, with separate IDE connections for Primary and Secondary cables
- Supports “Native Mode” Register and Interrupt support

1.3.3.5 AC'97 6-Channel Support

- Supports AC'97 2.3.
- 20 bit/16 bit audio capability with support for up to six channels of PCM audio output (full AC3 decode)
- Supports 3 codecs with independent PCI functions for audio and modem
- Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center and Woofer for a complete surround sound effect
- Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution.
- Integrated digital link allows several external codecs to be connected
- Third SDATA_IN line
- S/PDIF directed output
- Supports wake-up events (Wake on ring from suspend is supported with an appropriate modem codec)

Note: Modem implementation for different countries must be considered because telephone systems may vary.

1.3.3.6 Manageability and Other Enhancements

- Integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system.
- System management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

1.3.3.7 SMBus 2.0

- Provides an interface to manage peripherals such as serial presence detection (SPD) on DIMMs.
- 32 byte buffer
- Hardware Packet Error Checking
- Host interface allows the processor to communicate via SMBus
- Slave interface allows an external Microcontroller to access system resources
- Compatible with most 2-Wire components that are also I²C compatible.



1.3.3.8 Interrupt Controller

- Support for up to 8 PCI interrupt pins
- Supports PCI 2.2 Message Signaled Interrupts
- Two cascaded 82C59 with 15 interrupts
- Integrated I/O APIC capability with 24 interrupts
- Supports Serial Interrupt Protocol
- Supports Front-Side Bus interrupt delivery

1.3.4 Bandwidth Summary

Table 2 describes the bandwidth of critical 845G chipset platform interfaces.

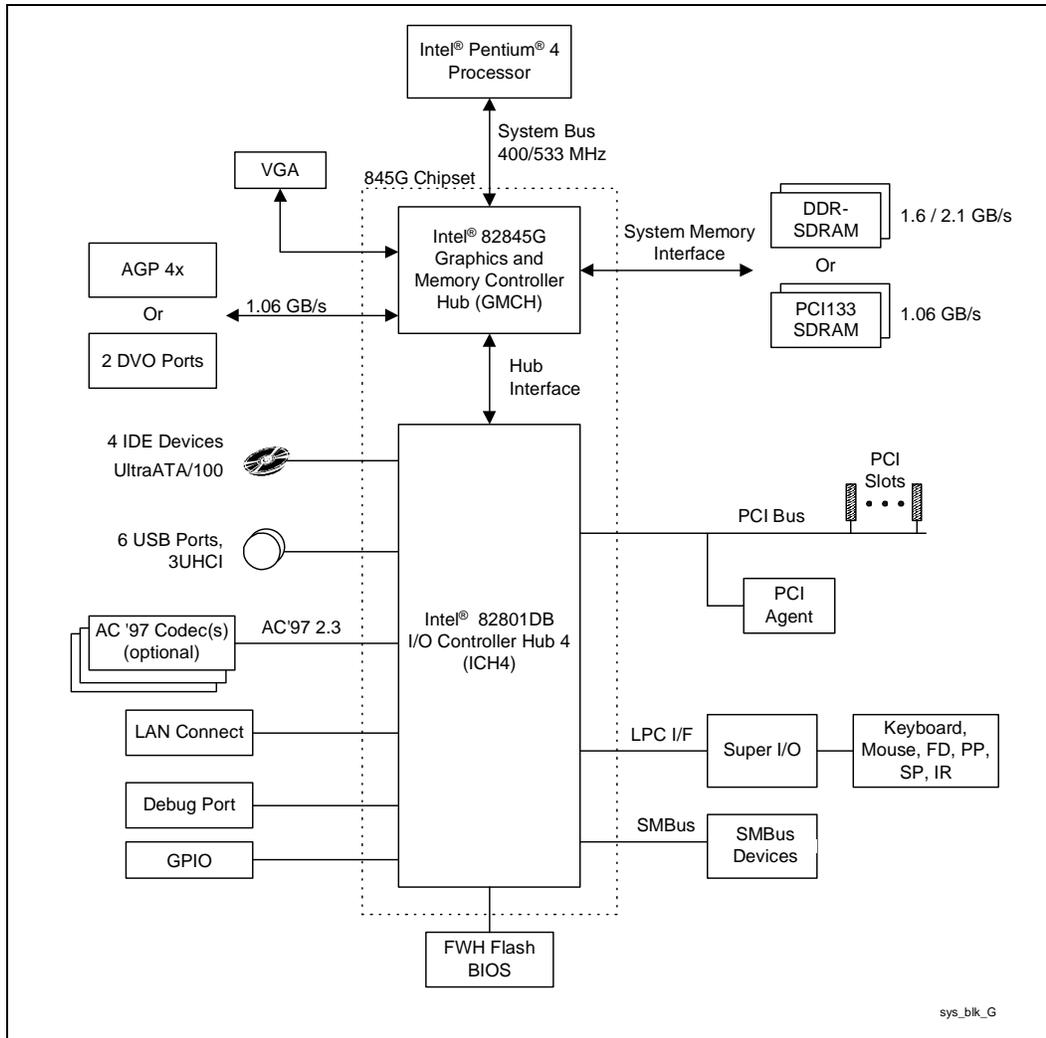
Table 2. Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth
System Bus	100/133	4	8	3.2 GB/s / 4.2 GB/s
AGP	66	4	4	1.06 GB/s
DVO	Up to 165	2	1.5/3	165 Mpixel/s / 330 Mpixel/s
DAC	Up to 350	N/A	N/A	Up to 350 Mpixel/s
Hub Interface	66	4	1	266 MB/s
PCI 2.2	33	1	4	133 MB/s
DDR-SDRAM	100/133	2	8	1.6 GB/s / 2.1 GB/s
SDR-SDRAM	133	1	8	1.06 GB/s

1.3.5 System Configuration

Figure 1 illustrates a typical Intel® Pentium® 4 Processor in the 478-pin package and 845G chipset based system configuration for mainstream desktop segments.

Figure 1. Typical System Configuration





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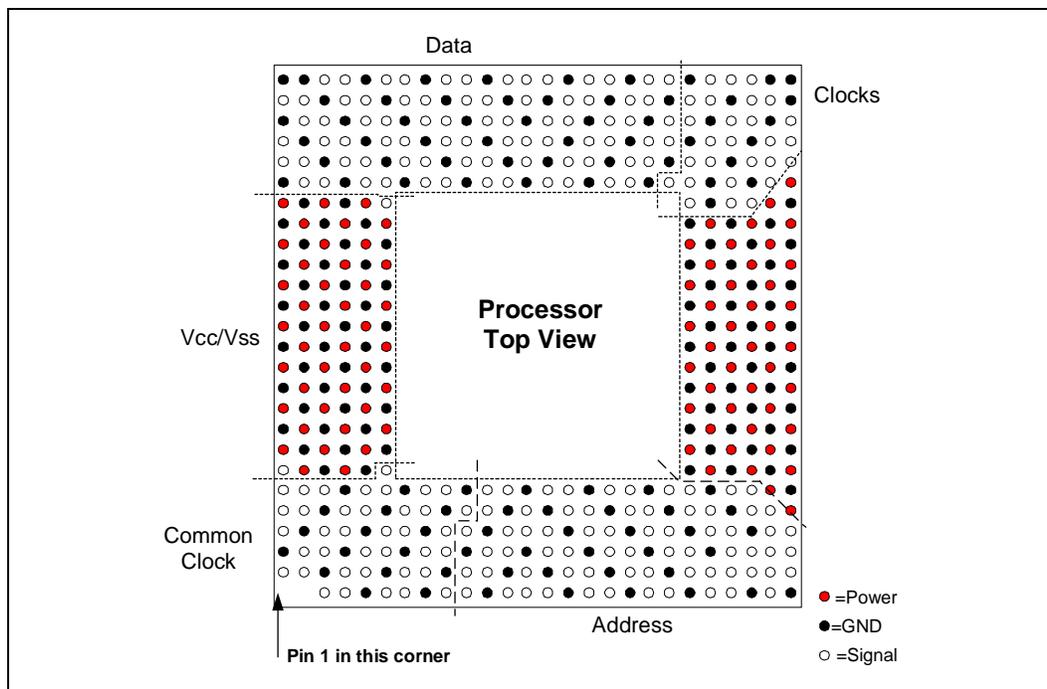
2 Component Quadrant Layout

The quadrant layouts shown are approximations. The quadrant layout figures do not show the exact component ball count; only general quadrant information is presented and is intended for reference while using this document. Only the exact pin or ball assignment should be used to conduct routing analysis. Refer to the following documents for pin or ball assignment information.

- *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*
- *Intel® Pentium® 4 Processor with 512 KB L2 Cache on .13 Micron Process Datasheet*
- *Intel® 845G/845GL/845GV Chipset Datasheet*
- *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*

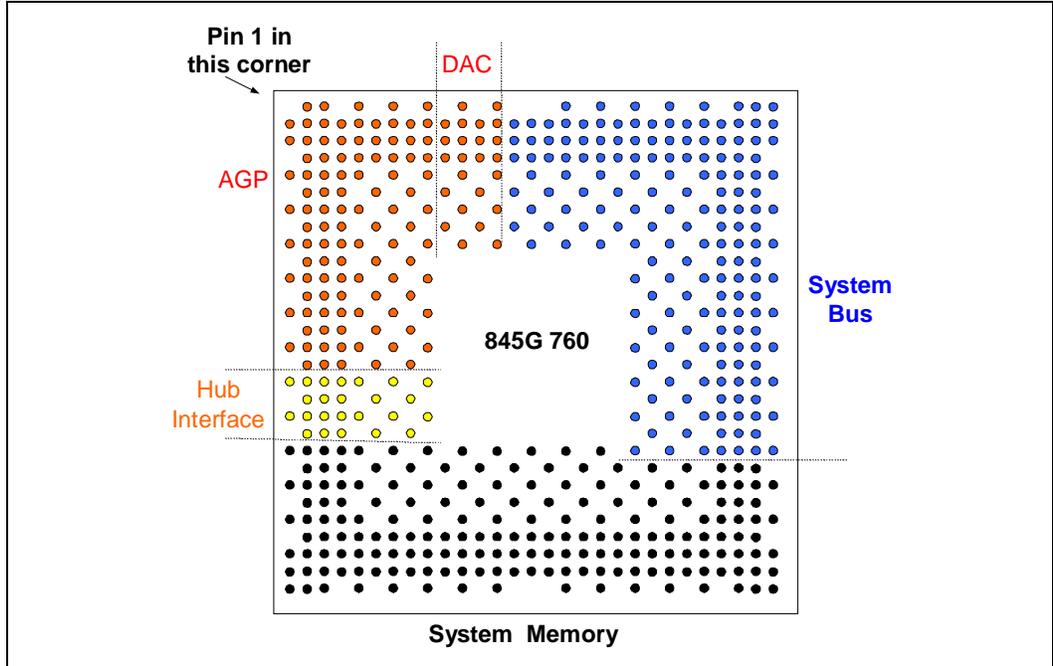
2.1 Intel® Pentium® 4 Processor Component Quadrant Layout

Figure 2. Intel® Pentium® 4 Processor in the 478-Pin Package Component Quadrant Layout (Top View)



2.2 Intel® 845G GMCH Component Quadrant Layout

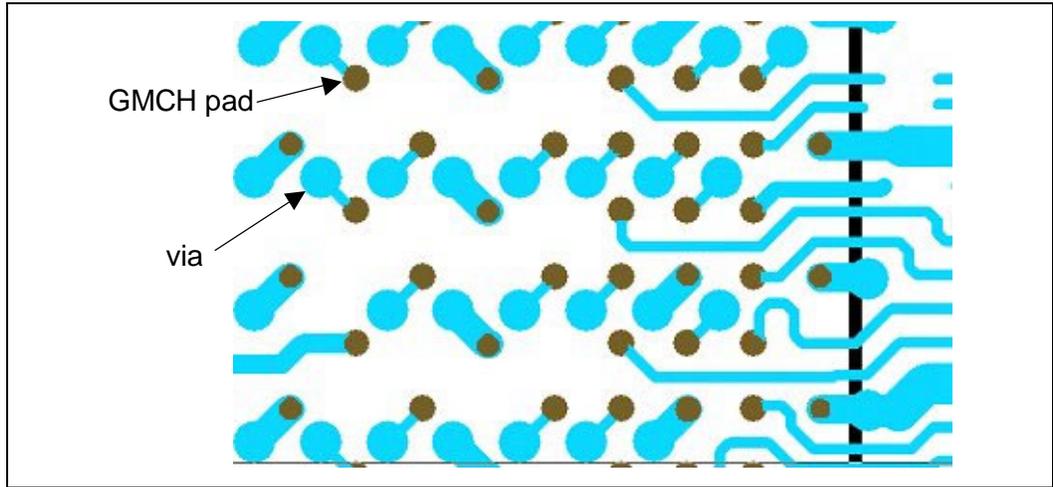
Figure 3. Intel® GMCH Component Quadrant Layout (Top View)



2.2.1 Offset-Ballout Advantages

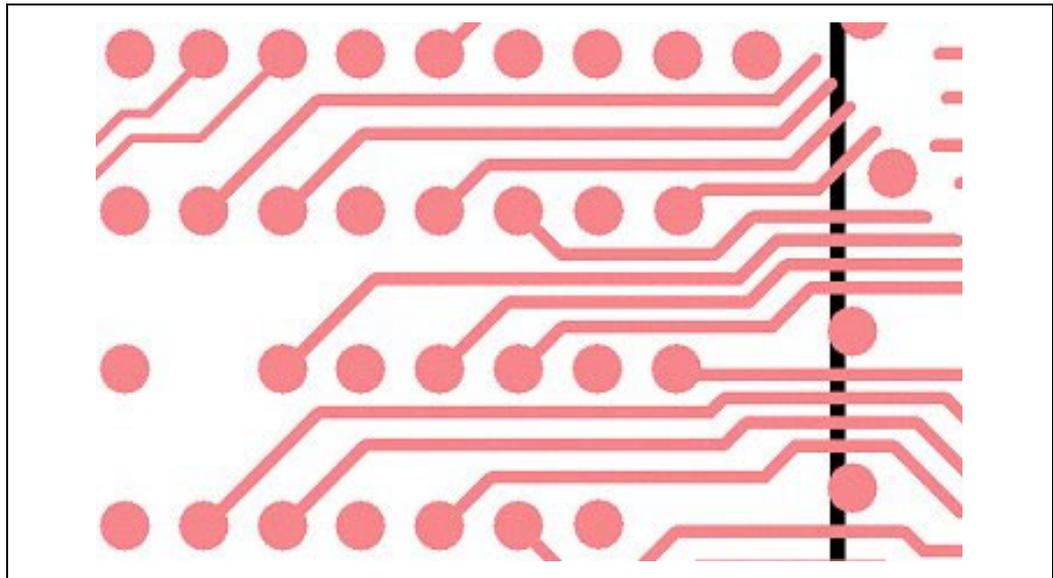
The GMCH utilizes an offset ballout pattern to allow for robust power delivery while utilizing the traditional vias discussed in Section 3.2.1. It is strongly recommended that the following breakout and via strategies be used with the 82845G GMCH. The following two figures show layer one and layer four and illustrate the breakout on the top layer and the breakout for the bottom layer. Notice the vias are arranged in rows, with the rows occurring between every other row of balls. Also, notice that the breakout is clean, both on the top layer and on the bottom layer.

Figure 4. Layer One Breakout



NOTE: Large circles are vias, and small circles are pads.

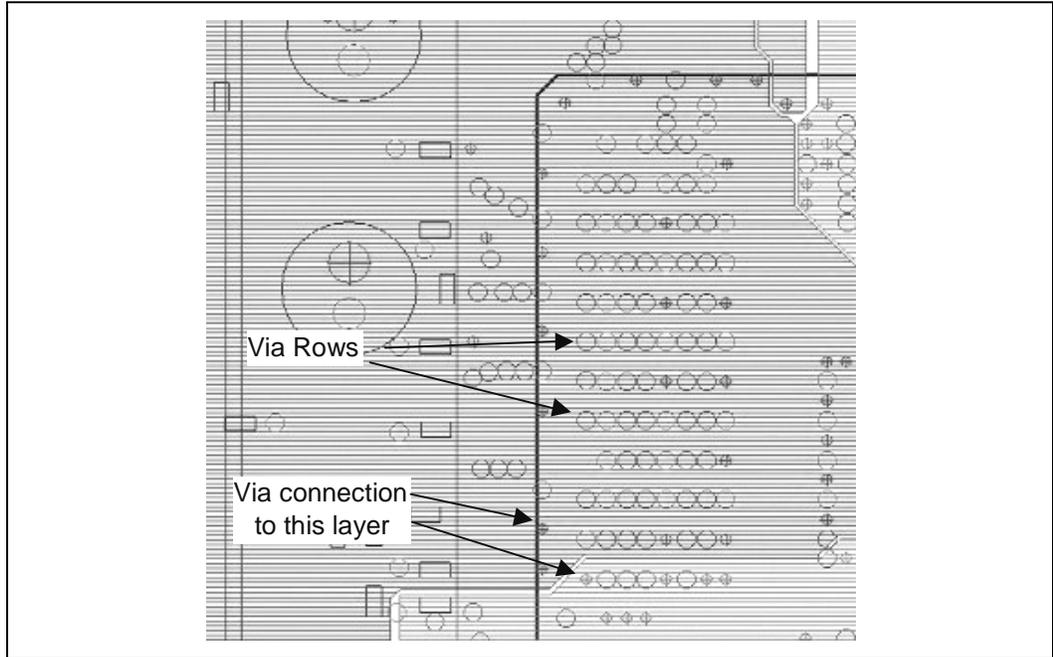
Figure 5. Layer Four Breakout



NOTE: Large circles are vias.

Figure 6 shows the results of the via rows on layer two (layer two has a ground shape and a power shape underneath the GMCH – see Section 14 for implementation).

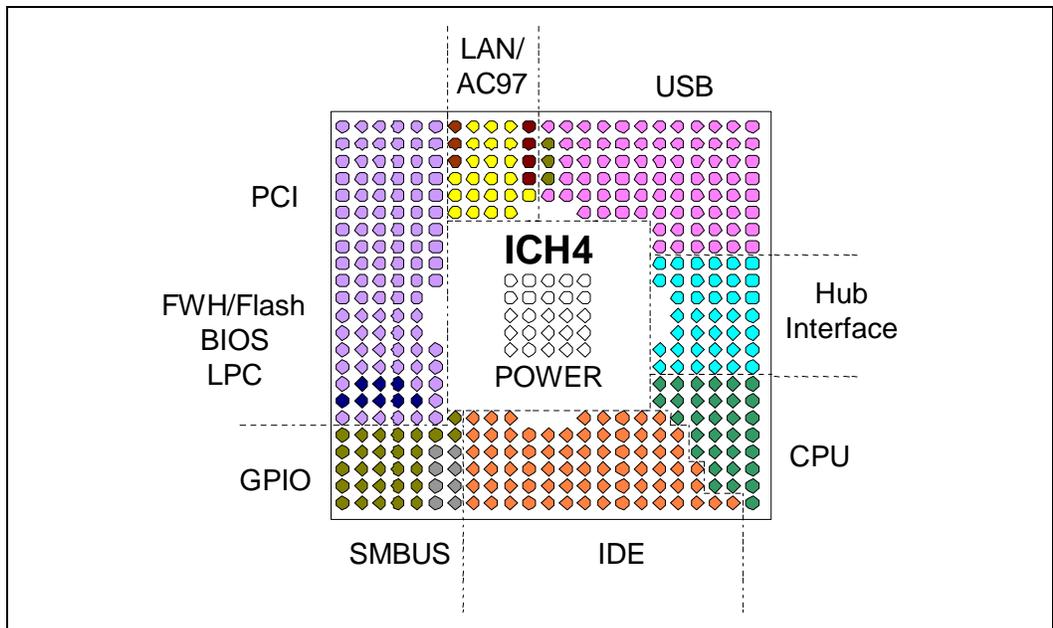
Figure 6. Layer Two Vias



The resulting rows of vias allow wide copper paths for power and ground. This fosters good power delivery and low impedance return paths for current to follow.

2.3 Intel® ICH4 Component Quadrant Layout

Figure 7. Intel® ICH4 Quadrant Layout (Top View)



3 Platform Stackup and Placement Overview

In this section, an example of an 845G chipset platform component placement and stackup is presented for a desktop system in uATX board form factor for PC133 or DDR200/266 SDRAM.

3.1 General Design Considerations

This section describes motherboard layout and routing guidelines for 845G platforms. This section does not describe the functional aspects of any bus, or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e., $60 \Omega \pm 15\%$) is the “nominal” trace impedance for a 5-mil wide trace. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

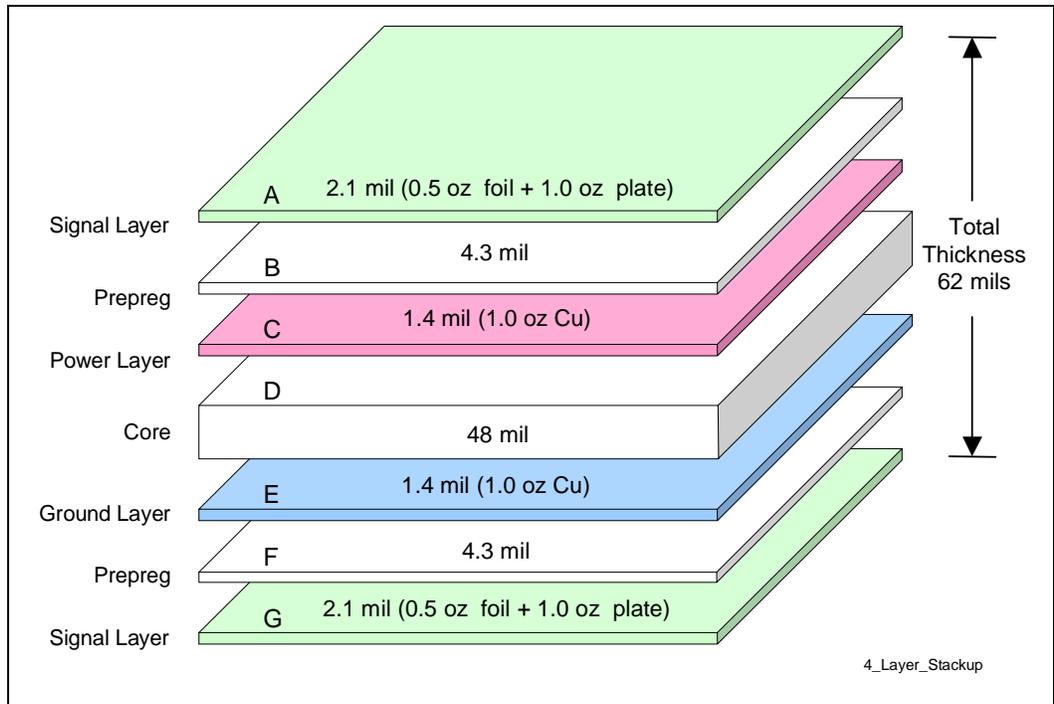
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

Additionally, these routing guidelines are created using a PCB stackup similar to that illustrated in Figure 8.

3.2 Nominal 4-Layer Board Stackup

The 845G chipset platform requires a board stackup yielding a target board impedance of $60 \Omega \pm 15\%$. Recommendations in this design guide are based on the following a 4-layer board stackup:

Figure 8. 4-layer PCB Stackup

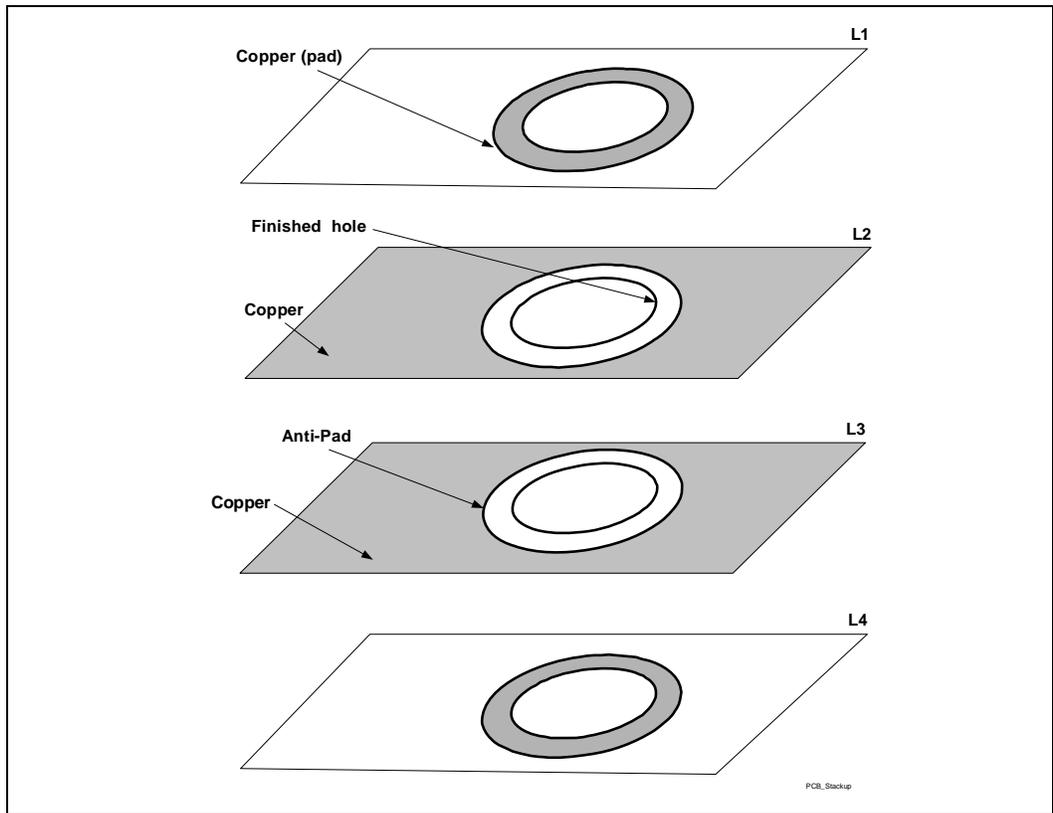


Description	Nominal Value	Tolerance	Comments
Board Impedance Z_0	60 Ω	$\pm 15\%$	With nominal 5 mil trace width
Dielectric Thickness	4.3 mils	± 0.5 mils	1 x 2116 Pre-Preg
Micro-stripline E_r	4.1	± 0.4	@ 100 MHz
Trace Width	5.0 mils	± 0.5 mils	Standard trace
Trace Thickness	2.1 mils	± 0.5 mils	0.5 oz foil + 1.0 oz plate
Soldermask E_r	4.0	± 0.5	@ 100 MHz
Soldermask Thickness	1.0 mils	± 0.5 mils	From top of trace

3.2.1 PCB Technology Considerations

Intel has found that the following recommendation aids in the design of an 845G chipset based platform. Simulations and reference platform are based on the following technology, and Intel recommends that designers adhere to these guidelines.

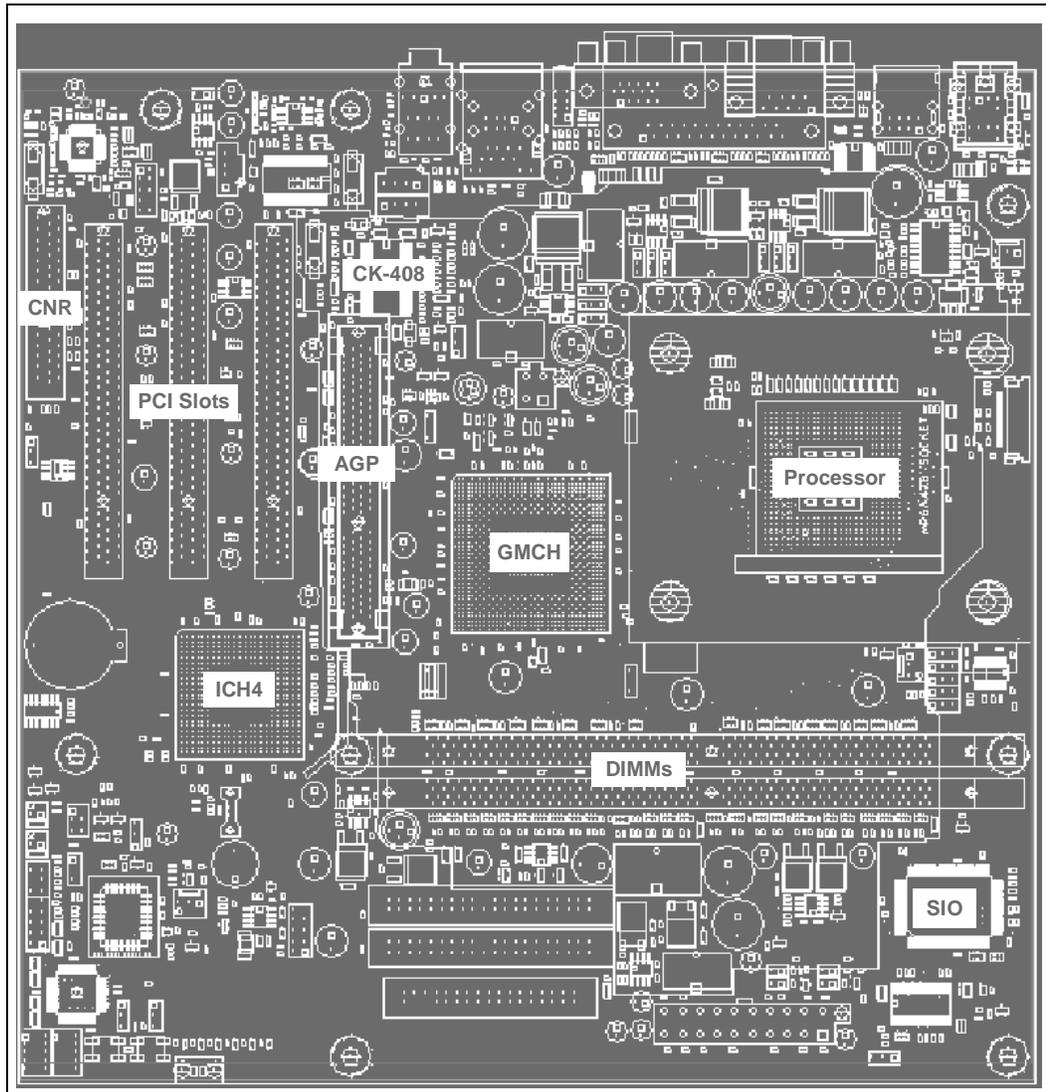
Figure 9. PCB Technologies – Stackup



Number of Layers	
Stack Up	4 Layer
Cu Thickness	0.5 oz Outer (before plating); 1oz inner
Final Board Thickness	62 mils (- 5mils / +8mils)
Material	Fiberglass made of FR4
Signal and Power Via Stack	
Via Pad	26 mils
Via Anti-Pad	40 mils
Via Finished Hole	14 mils

3.3 Platform Component Placement

Figure 10. Component Placement Example using DDR DIMMs



NOTE: SDR DRAM component placement is similar to the DDR DRAM placement shown in the figure.

4 Processor System Bus Guidelines

This section addresses layout recommendations for an Intel® Pentium® 4 Processor in the 478-pin package with a 400/533 MHz PSB configuration.

4.1 Processor System Bus Design Guidelines

Table 3 summarizes the layout recommendations for an Intel® Pentium® 4 Processor in the 478-pin package with a 400/533 MHz PSB configuration, and expands on specific design issues and recommendations.

Table 3. System Bus Routing Summary for the Processor

Parameter	Processor Routing Guidelines
Line to line spacing	Data and common clock system bus must be routed at 7 mil wide traces and with 13 mils spacing.
Breakout Guidelines (processor and GMCH)	7 mil wide with 5 mil spacing for a maximum of 250 mils from the component ball.
Group Spacing	Non Clock Spacing = 20 mils to any other signal
Data Line lengths (agent to agent spacing)	2" – 8" from pin-to-pin Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Signals should be referenced to VSS.
DSTBN/P[3:0]#	DSTBN/P# should be routed to the same length as their corresponding data signals' mean pad-to-pad length ± 25 mils. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (VSS) and the layers are all of the same configuration (all stripline or all microstrip). A data strobe and its complement should be routed within ± 25 mils of the same pad-to-pad length. If one strobe switches layers, its complement must switch layers in the same manner. DSTBN/P# should be referenced to VSS.
Address line lengths (agent to agent spacing) ADSTB[1:0]#	2" – 10" from pin-to-pin Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (VSS) and the layers are all of the same configuration (all stripline or all microstrip).



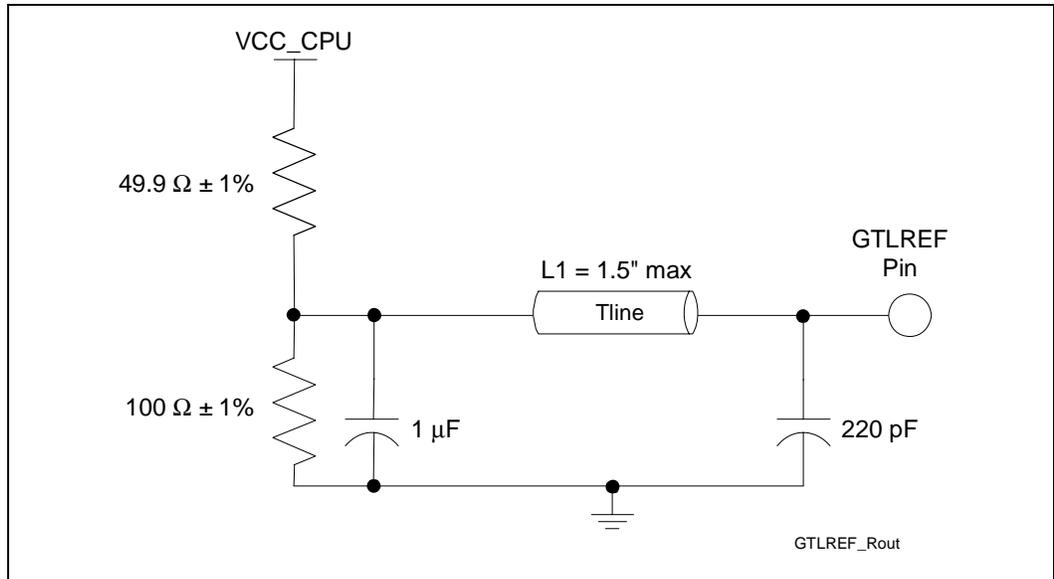
Parameter	Processor Routing Guidelines
Common Clock Trace Lengths	<ul style="list-style-type: none"> • 3.0" - 10" from pin-to-pin <p>Note: No length compensation is necessary.</p>
Topology	Point to point (chipset to processor).
Routing priorities	<p>All signals should be referenced to VSS.</p> <p>Ideally, layer changes should not occur for any signals. If a layer change must occur, reference plane must be VSS and the layers must all be of the same configuration (all stripline or all microstrip for example).</p> <p>The Data Bus must be routed first, then the address bus and then common clock.</p>
Clock keep-out zones	Refer to Table 89 Host Clock Routing Guidelines
Trace Impedance	50 Ω \pm 15%
Maximum via count per signal	<p>4 (Avoid layer change as much as possible.)</p> <p>No layer change is recommended.</p>

Note: Refer to the *Intel® 845G/845GL/GV Chipset Datasheet* for GMCH package dimensions, and refer to *Intel® Pentium® 4 Processor in the 478-pin package Signal Integrity Models* for Processor package dimensions.

4.1.1 GTLREF Layout and Routing Recommendations

There are four AGTL+ GTLREF pins on the processor that are used to set the reference voltage level for the AGTL+ signals (GTLREF). Because all of these pins are connected inside the processor package, the GTLREF voltage must be supplied to only one of the four pins.

Figure 11. GTLREF Routing



- The processor must have one dedicated voltage divider.
- Decouple the voltage divider with a 1 μF capacitor.
- Keep the voltage divider within 1.5 inches of the GTLREF pin.
- Decouple the pin with a high frequency capacitor (such as a 220 pF 603) as close to the pin as possible.
- Keep signal routing at least 10 mils separated from the GTLREF routes. Use a minimum 7 mil trace for routing.
- Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the front side bus signals.)

4.1.2 HVREF, HSWNG, HRCOMP Layout and Routing Recommendations at the Intel[®] GMCH

The HVREF signals must be tied to a resistor divider network that supplies $2/3 * VCC_CPU$. Use one 49.9Ω 1% resistor to the VCC_CPU plane, and one 100Ω 1% resistor to ground for the divider. Decouple with one $0.1 \mu F$ capacitor at the GMCH. The trace to the voltage divider should be routed at a maximum of 3" at 12 mils width. Keep this trace at a minimum of 10 mils away from other signals.

The HSWNG signals must be tied to a resistor divider network that supplies $1/3 * VCC_CPU$. Use one $300 \Omega \pm 1\%$ resistor to the VCC_CPU plane, and one $150 \Omega \pm 1\%$ resistor to ground for the divider. Decouple with one $0.01 \mu F$ capacitor at the GMCH. The trace to the voltage divider should be routed at a maximum of 3" with 12 mils width. Keep this trace at a minimum of 10 mils away from other signals.

Each HRCOMP signal must be tied to ground through a 24.9Ω 1% resistor. The trace to each resistor should be routed a maximum of 0.5" with 10 mils width. Keep each trace a minimum of 7 mils away from other signals.

4.2 Processor Configuration

4.2.1 Intel[®] Pentium[®] 4 Processor Configuration

This section provides more details for routing Intel[®] Pentium[®] 4 Processor based systems. Both recommendations and considerations are discussed.

For proper operation of the processor and the 845G chipset, it is necessary that the system designer meet the timing and voltage specifications of each component. The following recommendations are Intel guidelines based on extensive simulation and experimentation that make design assumptions that may be different than an OEM's assumptions. The most accurate way to understand the signal integrity and timing of the system bus in a platform is by performing a comprehensive simulation analysis. It is conceivable that adjustments to trace impedance, line length, termination impedance, board stackup, and other parameters can be made that improve system performance.

Refer to the *Intel[®] Pentium[®] 4 Processor in the 478-pin package Datasheet* for a system bus signal list, signal types, and definitions.

4.2.2 Topology and Routing

Table 4. Source Synchronous Signal Groups and the Associated Strobes

Signals	Associated Strobe
REQ[4:0]#, A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#, DINV_0#	DSTBP0#, DSTBN0#
D[31:16]#, DINV_1#	DSTBP1#, DSTBN1#
D[47:32]#, DINV_2#	DSTBP2#, DSTBN2#
D[63:48]#, DINV_3#	DSTBP3#, DSTBN3#

Note: DINV_[3:0] pins on the GMCH are referred to as DBI[3:0] on the processor.

Design recommendations are discussed first, followed by design considerations.

4.2.2.1 Design Recommendations

The following are the design recommendations for the data, address, strobes, and common clock signals. Based on the illustration shown in Figure 12, the data, address, strobe and common clock should be routed 7 mils with a 13-mil spacing. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate.

Data

The pin-to-pin distance for the data signals from the processor to the chipset should be between 2.0" and 8" (i.e., $2.0 < L1 < 8$ "). Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. As a result, additional trace is added to some data nets on the system board for all trace lengths within the same data group to be the same length (± 100 mils) from the pad of the processor to the pad of the chipset. This length compensation minimizes the source synchronous skew that exists on the system bus. Without the length compensation, the flight times between a data signal and its strobe will be different, which results in an inequity between the setup and hold times. Data signals may change layers if the reference plane remains VSS.

Equation 1. Calculation to Determine Package Delta Addition to Motherboard Length

$$\text{delta}_{\text{net,stroke}} = (\text{cpu_pkglen}_{\text{net}} - \text{cpu_pkglen}_{\text{stroke}^*}) + (\text{cs_pkglen}_{\text{net}} - \text{cs_pkglen}_{\text{stroke}})$$

NOTE: Strobe package length is the average of the strobe pair.

Refer to Section 4.7 in this Design Guide for package lengths.

Address

Address signals follow the same rules as data signals, except they should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. Address signals may change layers if the reference plane remains VSS.

Data Strobes

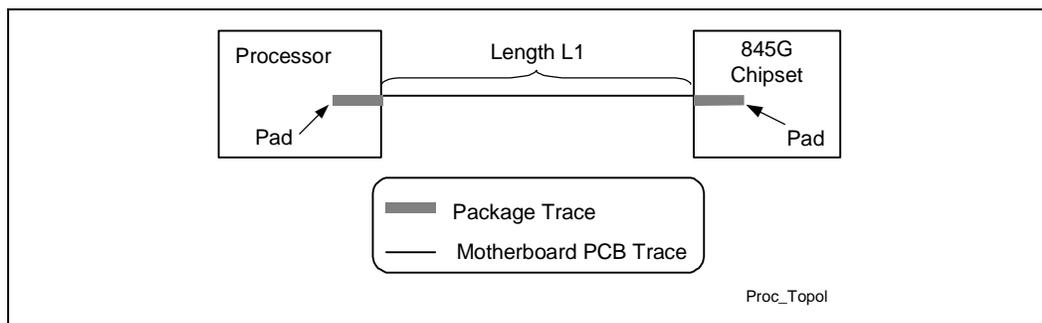
A strobe and its complement should be routed to a length equal to their corresponding data group's mean pad-to-pad length ± 25 mils. This causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. A strobe and its complement (xSTBp/n#) should be routed so that the difference in their lengths is less than

25 mils. It is recommended that skew be simulated to determine the length that best centers the strobe for a given system.

Common Clock

Common clock signals should be routed to a minimum pin-to-pin motherboard length of 3 inches, and a maximum motherboard length of 10 inches.

Figure 12. Processor Topology



4.3 Routing Guidelines for Asynchronous GTL+ and Other Signals

This section describes layout recommendations for signals other than data, strobe and address. Table 5 lists the signals described in this section.

Table 5 Miscellaneous Signals (Signals that are not Data, Address, or Strobe)

Signal Name	Type	Direction	Topology	Driven by
A20M#	Asynchronous GTL+	I	2A	ICH4
BREQ0#	AGTL+	I/O	4	Processor
COMP[1:0]	Analog	I	5	
FERR#	Asynchronous GTL+ Open Drain	O	1A	Processor
IGNNE#	Asynchronous GTL+	I	2A	ICH4
INIT#	Asynchronous GTL+	I	2B	ICH4
LINT0/INTR LINT1/NMI	Asynchronous GTL+	I	2A	ICH4
PROCHOT#	Asynchronous GTL+ Open Drain	O	1B	Processor
PWRGOOD	Other	I	2C	ICH4
RESET#	AGTL+ Open Drain	I	4	GMCH
SLP#	Asynchronous GTL+	I	2A	ICH 4
SMI#	Asynchronous GTL+	I	2A	ICH4
STPCLK#	Asynchronous GTL+	I	2A	ICH4
THERMTRIP#	Asynchronous GTL+ Open Drain	O	1C	Processor
VCCA	Power	I	3	External logic
VCCIOPLL	Power	I	3	External logic
VCC_SENSE	Other	O		Processor
VID[4:0]	Open Drain 3.3 V Tolerant	O	8	Processor
VSSA	Power	I	3	Ground
VSS_SENSE	Other	O		Processor
THERMDA/THERMDC	Other	I/O	6	External logic
TESTHI	Other	I/O	7	External logic

All signals must meet the AC and DC specifications as documented in the *Intel® Pentium® 4 Processor in the 478-pin package Datasheet*.

4.3.1 Topologies

The following sections describe the topologies and layout recommendations for the miscellaneous signals.

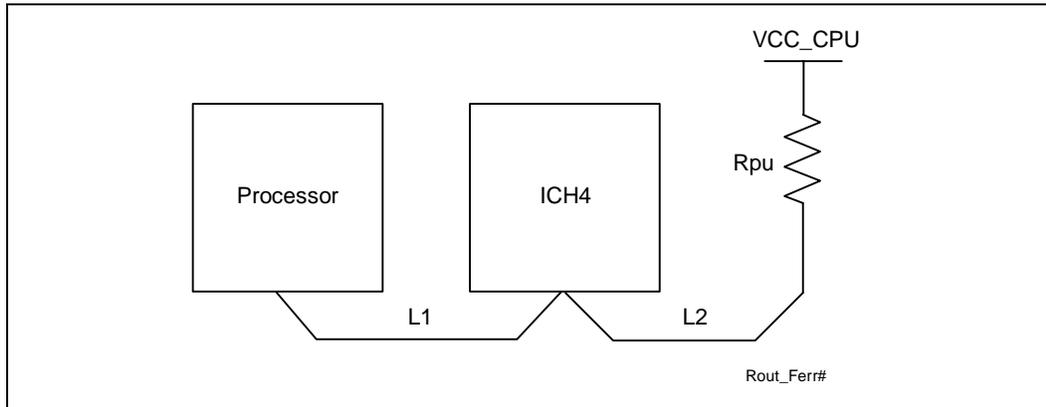
4.3.1.1 Topology 1A: Asynchronous GTL+ Signals Driven by Processor

Topology 1A is for the asynchronous GTL+ signals driven by the processor (FERR#). FERR# should adhere to the following routing and layout recommendations.

Table 6. Layout Recommendations for FERR# Signal — Topology 1A

Trace Zo	Trace Spacing	L1	L2	Rpu
60 Ω	7 mil	1"-12"	3" max	62 ± 5% Ω

Figure 13. Routing Illustration for FERR#



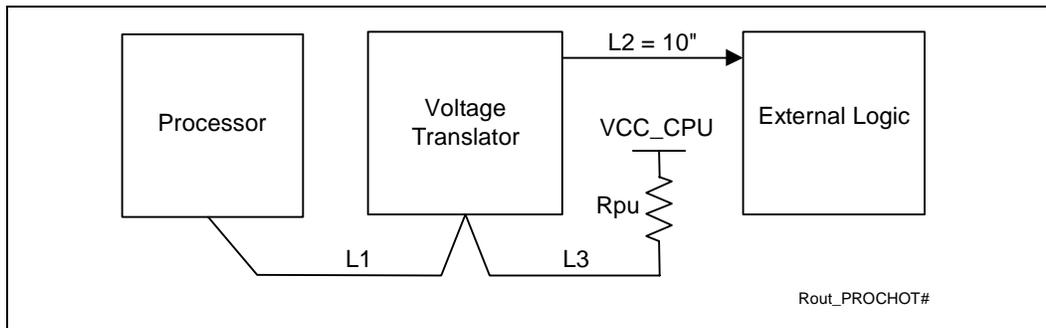
4.3.1.2 Topology 1B: Asynchronous GTL+ Signals Driven by Processor (PROCHOT#)

Topology 1B is for the asynchronous GTL+ signals driven by the processor (PROCHOT#). PROCHOT# should adhere to the following routing and layout recommendations. If PROCHOT# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

Table 7. Layout Recommendations for PROCHOT# Signal — Topology 1B

Trace Zo	Trace Spacing	L1	L2	L3	Rpu
60 Ω	7 mil	1" – 17"	10" max	3" max	62 Ω ± 5%

Figure 14. Routing Illustration for PROCHOT#



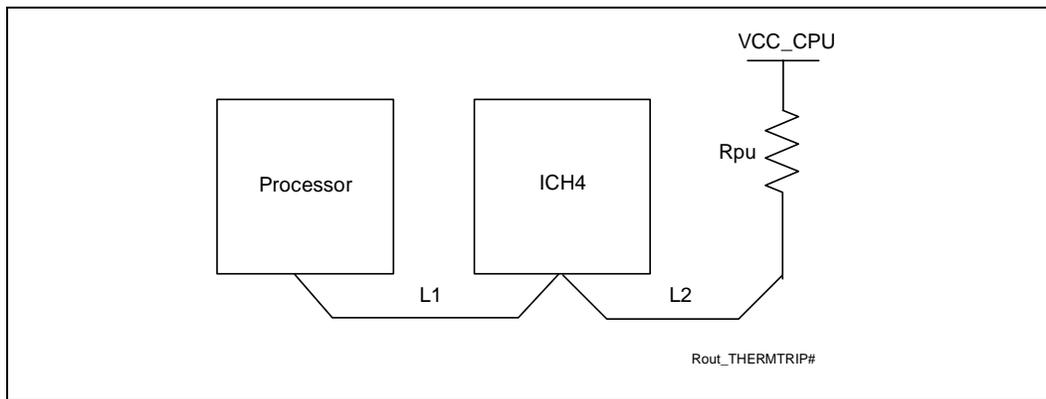
4.3.1.3 Topology 1C: Asynchronous GTL+ Signals Driven by Processor (THERMTRIP#)

Topology 1C is for the asynchronous GTL+ signals driven by the processor (THERMTRIP#). THERMTRIP# should adhere to the following routing and layout recommendations. If THERMTRIP# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor, and to meet input thresholds for the external logic.

Table 8. Layout Recommendations for THERMTRIP# Signal — Topology 1C

Trace Zo	Trace Spacing	L1	L2	Rpu
60 Ω	7 mil	1" – 12"	3" max	62 Ω ± 5%

Figure 15. Routing Illustration for THERMTRIP#



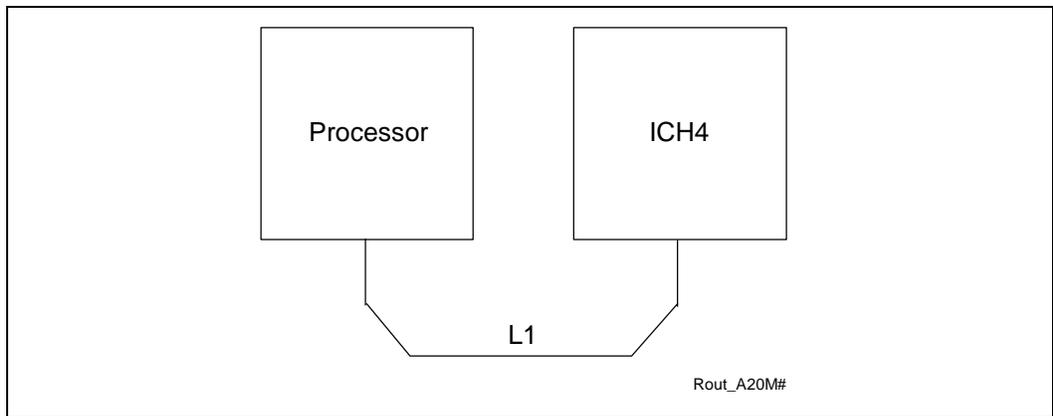
4.3.1.4 Topology 2A: Asynchronous GTL+ Signals Driven by ICH4

Topology 2A is for the asynchronous GTL+ signals driven by the Intel® ICH4 (A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#). These signals should adhere to the following routing and layout recommendations. Figure 16 shows the recommended topology.

Table 9. Layout recommendations for Miscellaneous Signals — Topology 2A

Trace Zo	Trace Spacing	L1	Rpu
60 Ω	7 mil	17" max	None

Figure 16. Routing Illustration for A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#



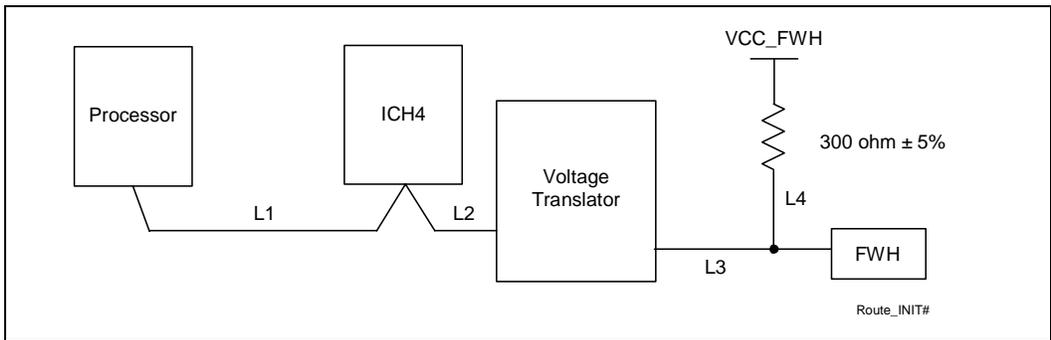
4.3.1.5 Topology 2B

Topology 2B is for the INIT# signal.

Table 10: Layout Recommendations for INIT# — Topology 2B

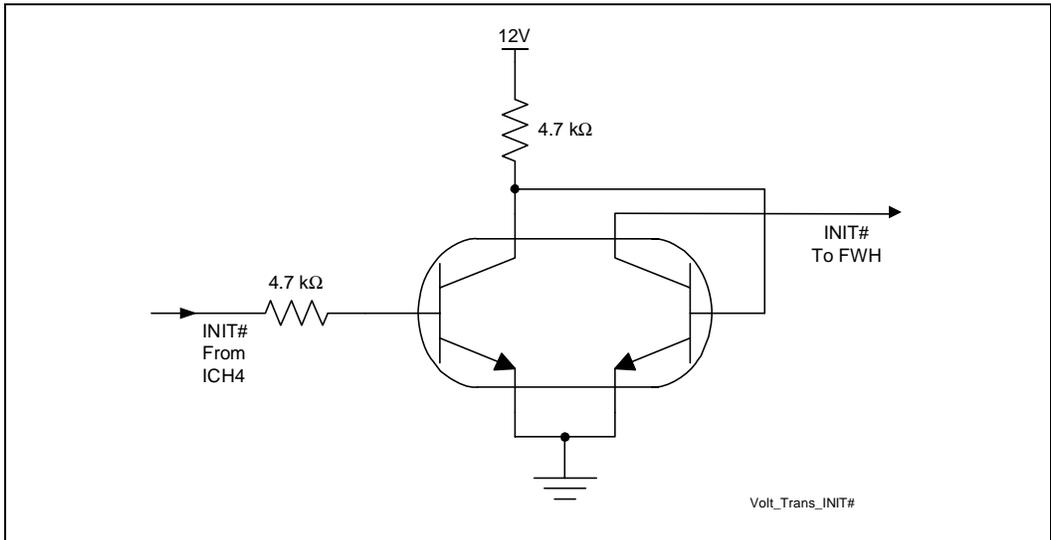
Trace Zo	Trace Spacing	L1	L2	L3	L4	Rpu
60 Ω	7mil	17" max	2" max	10" max	3" max	None

Figure 17: Routing Illustration for INIT#



Level shifting is required for the INIT# signal to the FWH to meet the input logic levels of the FWH. Figure 18 shows one method of implementing level shifting.

Figure 18: Voltage Translation of INIT#



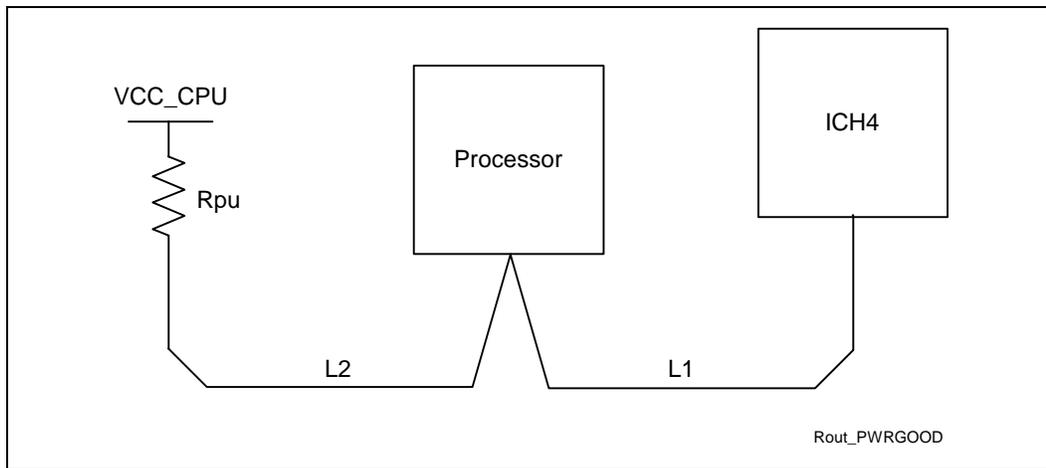
4.3.1.6 Topology 2C: Miscellaneous Signals Driven by ICH4 (PWRGOOD)

Topology 2C is for the miscellaneous signals driven by the Intel® ICH4 Open Drain (PWRGOOD). This signal should adhere to the following routing and layout recommendations. Figure 19 illustrates the recommended topology.

Table 11. Layout Recommendations for Miscellaneous Signals — Topology 2B

Trace Zo	Trace Spacing	L1	L2	Rpu
60 Ω	7 mil	1" – 12"	3" max	300 Ω ± 5%

Figure 19. Routing Illustration for PWRGOOD



4.3.1.7 Topology 3

Topology 3 is for the VCCIOPLL, VCCA and VSSA signals. Refer to Section 4.6.5.1 (Filter Specifications For VCCA, VCCIOPLL, and VSSA) for VCCIOPLL, VCCA, and VSSA information.

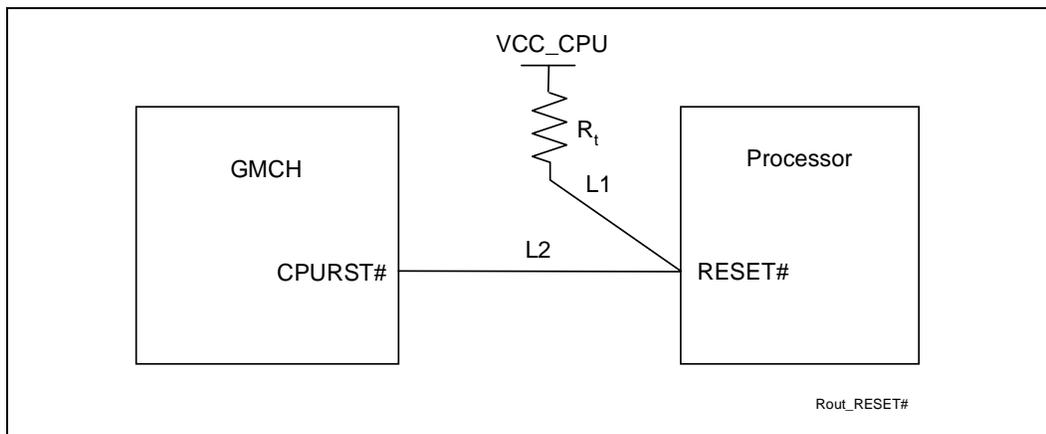
4.3.1.8 Topology 4: BREQ0# and RESET#

Topology 4 is for the BREQ0# and RESET# signals. Because the processor does not have on-die termination on the BREQ0# and RESET# signals, it is necessary to terminate using discrete components on the system board. Connect the signals between the components as shown in Figure 20. The 845G chipset has on-die termination; therefore it is necessary to terminate only at the processor end. The value of R_t should be $51\ \Omega \pm 5\%$ for RESET#. The value of R_t should be $150\ \Omega - 220\ \Omega \pm 5\%$ for BREQ0#.

Table 12. Layout Recommendations for BREQ0# and RESET# — Topology 4

Signal	R_t	L1	L2
BREQ0#	150 Ω to 220 Ω	$\leq 1'' - 2''$	3'' - 10''
RESET#	51 Ω	$\leq 1'' - 2''$	3'' - 10''

Figure 20. Routing Illustration for RESET#



NOTE: BREQ0# is similarly terminated.

4.3.1.9 Topology 5: COMP[1:0] Signals

Topology 5 is for the COMP[1:0] signals. Terminate the COMP[1:0] pins to ground through a $51\ \Omega \pm 1\%$ resistor as close as possible to the pin. Do not wire COMP pins together — connect each pin to its own termination resistor. RCOMP value can be adjusted to set external drive strength of I/O, and to control the edge rate.



4.3.1.10 Topology 6: THERMDA/THERMDC

Topology 6 is for the THERMDA/THERMDC routing guidelines. The processor incorporates an on-die thermal diode. THERMDA (diode anode) and THERMDC (diode cathode) pins on the processor can be connected to a thermal sensor located on the system board to monitor the die temperature of the processor for thermal management and long term die temperature change monitoring purpose. This thermal diode is separate from the thermal monitor's thermal sensor, and cannot be used to predict the behavior of the thermal monitor.

Because the thermal diode is used to measure a very small voltage from the remote sensor, care must be taken to minimize noise induced at the sensor inputs. The following are some guidelines:

- The remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4 to 8 inches away, as long as the worst noise sources such as clock generators, data buses, address buses, etc., are avoided.
- Route the THERMDA and THERMDC lines in parallel and close together with ground guards enclosed.
- Use wide tracks to reduce inductance and noise pickup that may be introduced by narrow ones. A width of 10 mils and spacing of 10 mils is recommended.

4.3.1.11 Topology 7: TESTHI and RESERVED Pins

Topology 7 is for the TESTHI and RESERVED Pins. The TESTHI pins should be tied to the processor VCC using a matched resistor, where a matched resistor has a resistance value within $\pm 20\%$ of the impedance of the board transmission line traces. For example, if the trace impedance is 50 Ω , then a value between 40 Ω and 60 Ω is required.

The TESTHI pins may use individual pull-up resistors or may be grouped together as follows:

- TESTHI[1:0]
- TESTHI[5:2]
- TESTHI[10:8]
- TESTHI[12:11]

A matched resistor should be used for each group.

Additionally, if the ITPCLKOUT[1:0] pins are not used, they may be connected individually to VCC using matched resistors, or may be grouped with TESTHI[5:2] with a single matched resistor. If they are being used, individual termination with 1 k Ω resistors is acceptable. Tying ITPCLKOUT[1:0] directly to VCC or sharing a pull-up resistor to VCC, will prevent use of debug interposers. This implementation is strongly discouraged for system boards that do not implement an onboard debug port.

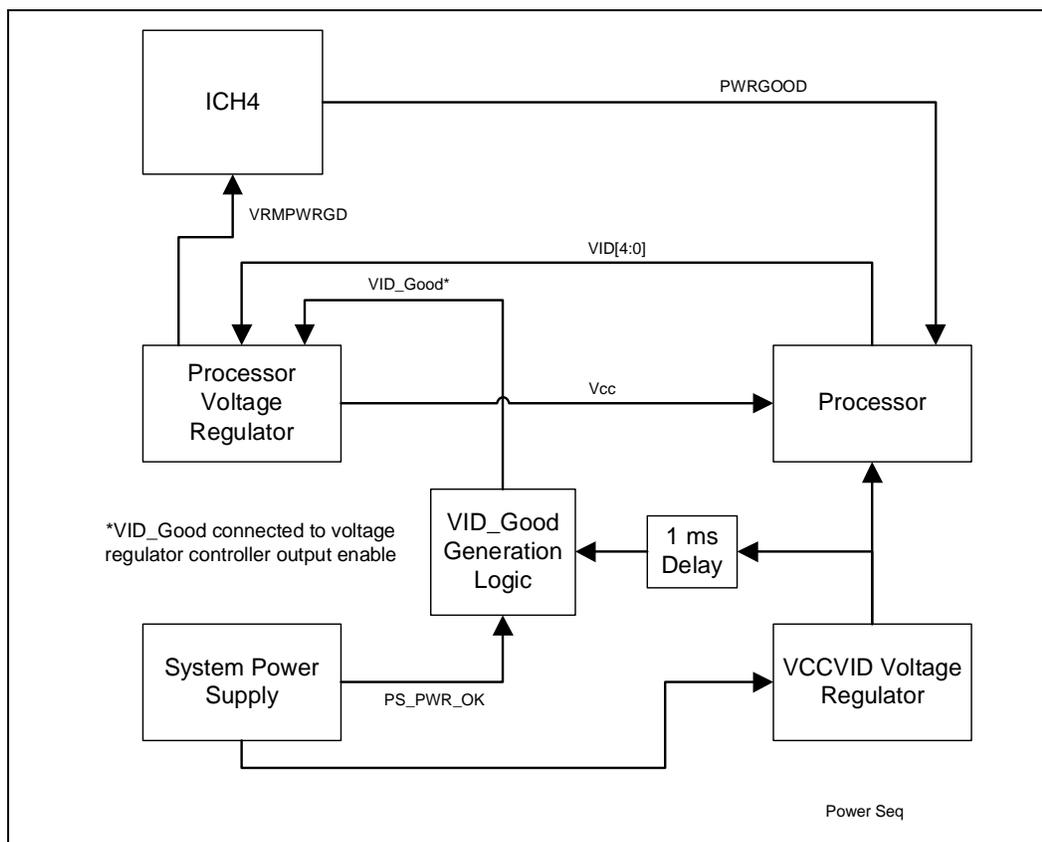
As an alternative, group 2 (TESTHI[5:2]), and the ITPCLKOUT[1:0] pins may be tied directly to the processor VCC. This has no impact on system functionality. TESTHI0 and TESTHI12 may also be tied directly to processor VCC if resistor termination is a problem, but matched resistor termination is recommended. In the case of the ITPCLKOUT1:0, direct tie to VCC is strongly discouraged for system boards that do not implement an onboard debug port.

Reserved pins on the GMCH and on the CPU should be left as No Connect unless otherwise specified.

4.3.1.12 Topology 8: Processor Voltage Regulator Sequencing Requirements

Topology 8 is for the processor voltage regulator sequencing requirements. The processor requires a 1.2 V supply to the VCCVID pins to support the on-die VID generation circuitry. A linear regulator is recommended to generate this voltage. The on-die VID generation circuitry has some power sequencing requirements. Figure 21 shows a block diagram of a power sequencing implementation.

Figure 21. Power Sequencing Block Diagram



4.3.1.13 Topology 9: PSB Frequency Select

The BSEL circuit determines the PSB frequency, and should be implemented as shown in Figure 22.

Figure 22. PSB Frequency Select Circuitry

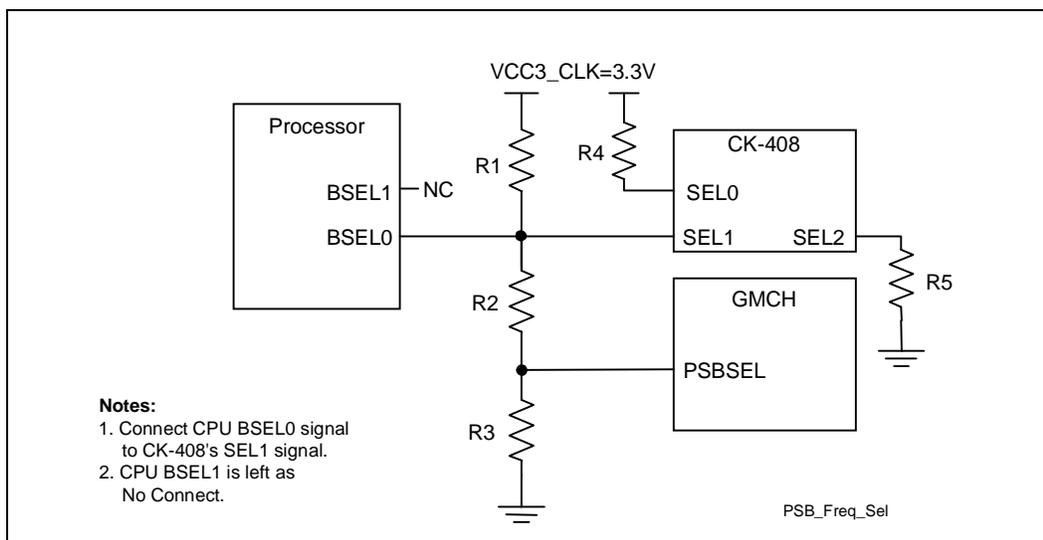


Table 13. PSB Frequency Select Circuit Resistor Values

Resistor	Value
R1	1.5 kΩ
R2	8.2 kΩ
R3	8.2 kΩ
R4	1 kΩ
R5	> 470 Ω

Table 14. Frequency Select Settings

SEL [2:0]	CK-408 Speed	BSEL0	CPU
001	100 MHz	L	400 MHz
011	133 MHz	Hi-Z	533 MHz

Do not exceed the max current rating for the BSEL. Refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet* for the max current specifications.



4.4 Additional Processor Design Considerations

This section describes system design considerations not addressed in previous sections.

4.4.1 Retention Mechanism Placement and Keep-Outs

The retention mechanism requires a keep-out zone, for a limited component height area under the retention mechanism as shown in the following figures. The figures show the relationship between the retention mechanism mounting holes and pin one of the socket, and show the keep-outs.

The retention holes should be non-plated holes, and should have a primary and secondary side route keep-out area of 0.409 inches diameter.

For heat sink volumetric information, refer to the *Intel® Pentium® 4 Processor in the 478-pin package Thermal Design Guidelines*.

Figure 23. Retention Mechanism Keep-Out Drawing 1

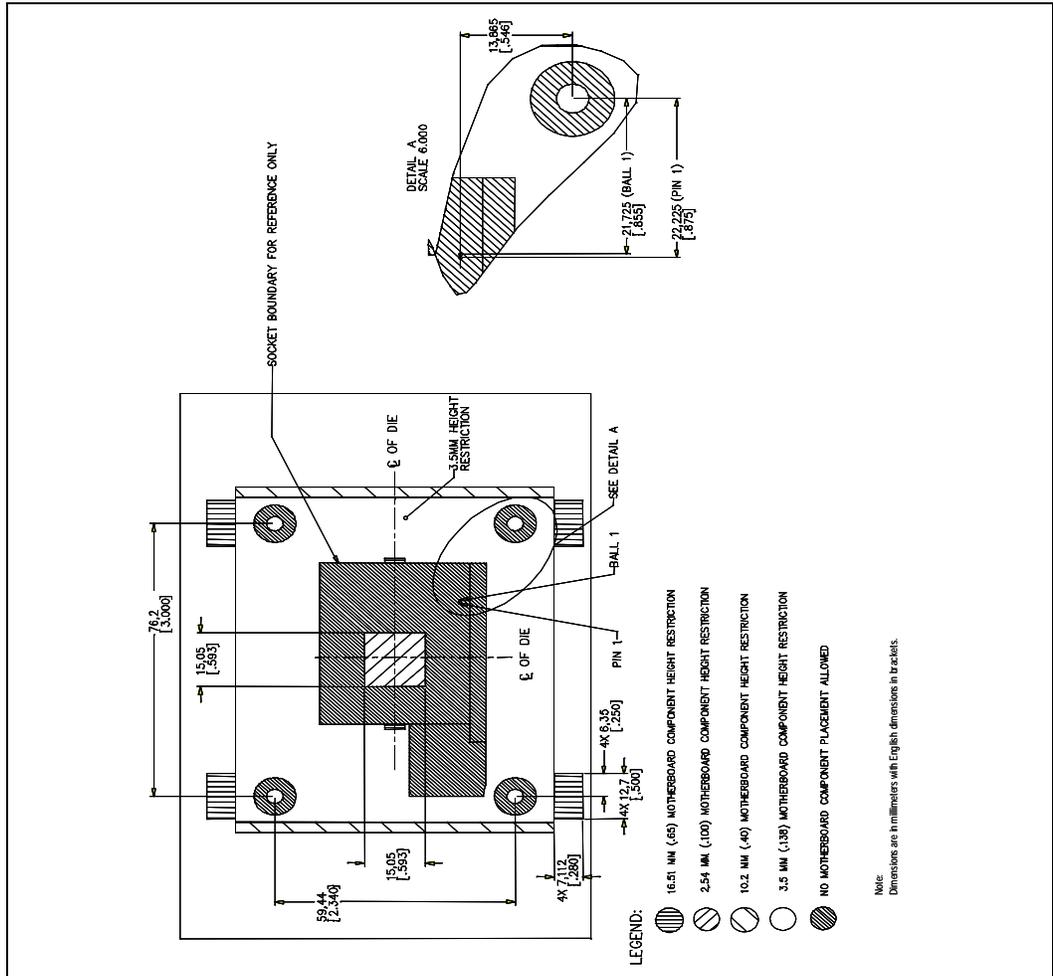
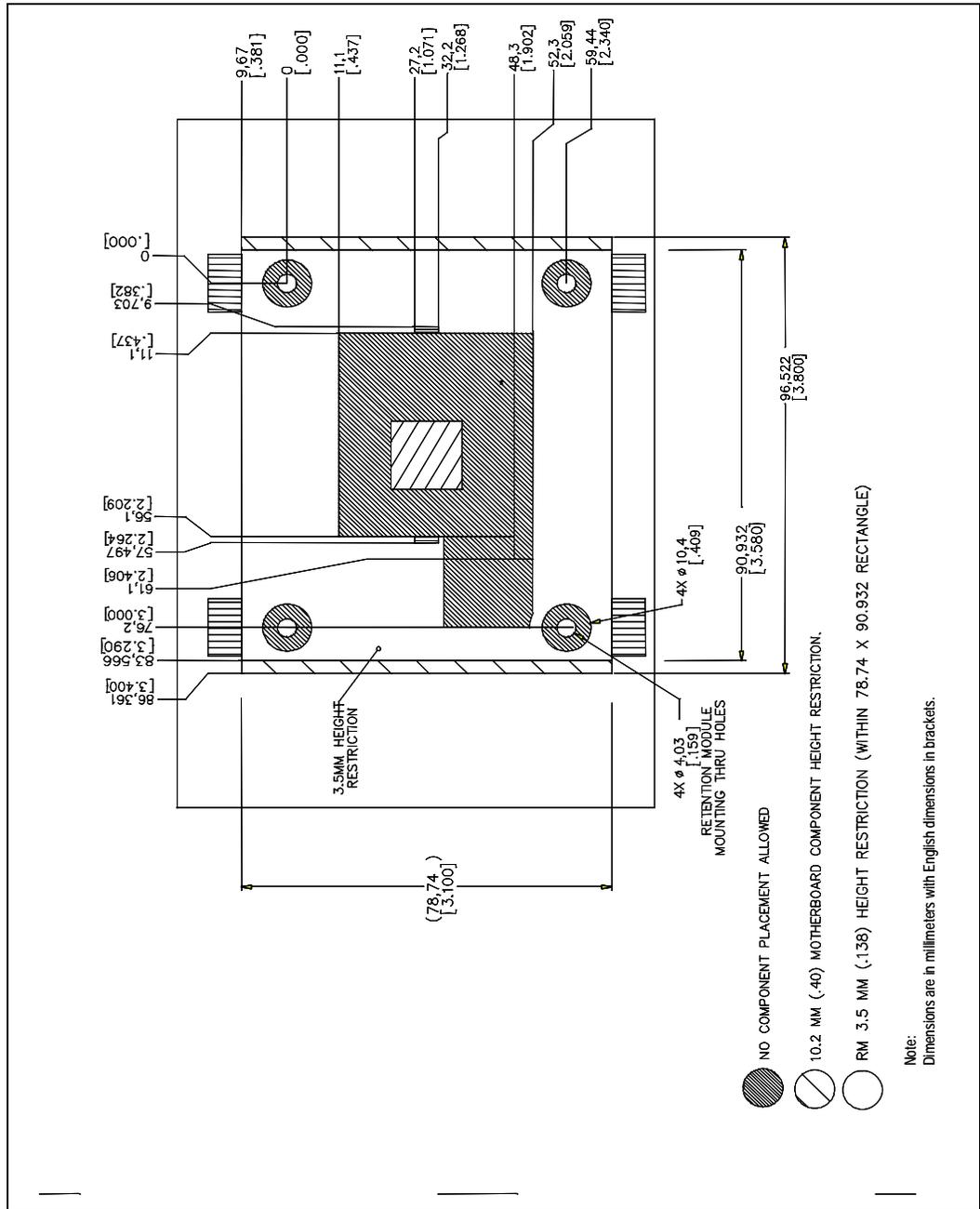


Figure 24. Retention Mechanism Keep-Out Drawing 2



4.4.2 Power Header for Active Cooling Solutions

The reference-design heat sink includes an integrated fan. The recommended connector for the active cooling solution is a Walden* /Molex* 22-01-3037, AMP* 643815-3 or equivalent. The integrated fan requires the system board to supply a minimum of 740mA at 12 V for proper operation. The fan connector pinout is described in Table 15.

Table 15. Reference Solution Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	No Connect

The Intel boxed processor heat sink includes an integrated fan. The recommended connector for the active cooling solution is a Walden* /Molex* 22-23-2037, AMP* 640456-3 or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. The fan connector pinout is described in Table 16.

Table 16. Boxed Processor Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	SENSE

The fan heat sink outputs a SENSE signal, which is an open-collector output that pulses at a rate of two pulses per fan revolution. The system board requires a pull-up resistor to provide the appropriate Voh level to match the fan speed monitor. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 should be tied to GND.

For more information on boxed processor requirements, refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*.

4.5 ITP Debug Port Routing Guidelines

Refer to the latest revision of the *ITP700 Debug Port Design Guide* for details on the implementation of the debug port.

4.5.1 Debug Tools Specifications

4.5.1.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the Intel® Pentium® 4 Processor in the 478-pin package system. Tektronix* and Agilent* should be contacted for specific information about their logic analyzer interfaces. The following information is general in nature.

Due to the complexity of Intel® Pentium® 4 Processor in the 478-pin package system, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing an Intel® Pentium® 4 Processor in the 478-pin package system that can make use of an LAI: mechanical and electrical.

4.5.1.2 Mechanical Considerations

The LAI is installed between the processor socket and the Intel® Pentium® 4 Processor in the 478-pin package. The LAI pins plug into the socket, and the Intel® Pentium® 4 Processor in the 478-pin package pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Intel® Pentium® 4 Processor in the 478-pin package and a logic analyzer. The maximum volume occupied by the LAI, known as the keep-out volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keep-out volume remains unobstructed inside the system. Note that it is possible that the keep-out volume reserved for the LAI may include space normally occupied by the Intel® Pentium® 4 Processor in the 478-pin package heat sink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

4.5.1.3 Electrical Considerations

The LAI will also affect the electrical performance of the system bus. Therefore, it is critical to obtain electrical load models for each of the logic analyzers to allow running of system level simulations that prove that the tool will work in the system. Contact the logic analyzer vendor for LAI electrical specifications and load models.



4.6 Intel® Pentium® 4 Processor in the 478-pin Package Power Distribution Guidelines

See Section 14 for general platform power delivery guidelines.

4.6.1 Power Requirements

Intel recommends using an Intel® Pentium® 4 Processor VR Down Design Guidelines-compliant regulator for processor system board designs. An Intel® Pentium® 4 Processor VR Down Design Guidelines-compliant regulator may be integrated as part of the system board, or on a module. The system board designer should properly place high frequency and bulk-decoupling capacitors as needed between the voltage regulator and the processor to ensure voltage fluctuations remain within the specifications listed in the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*. See Section 4.6.2 for recommendations on the amount of decoupling that is required.

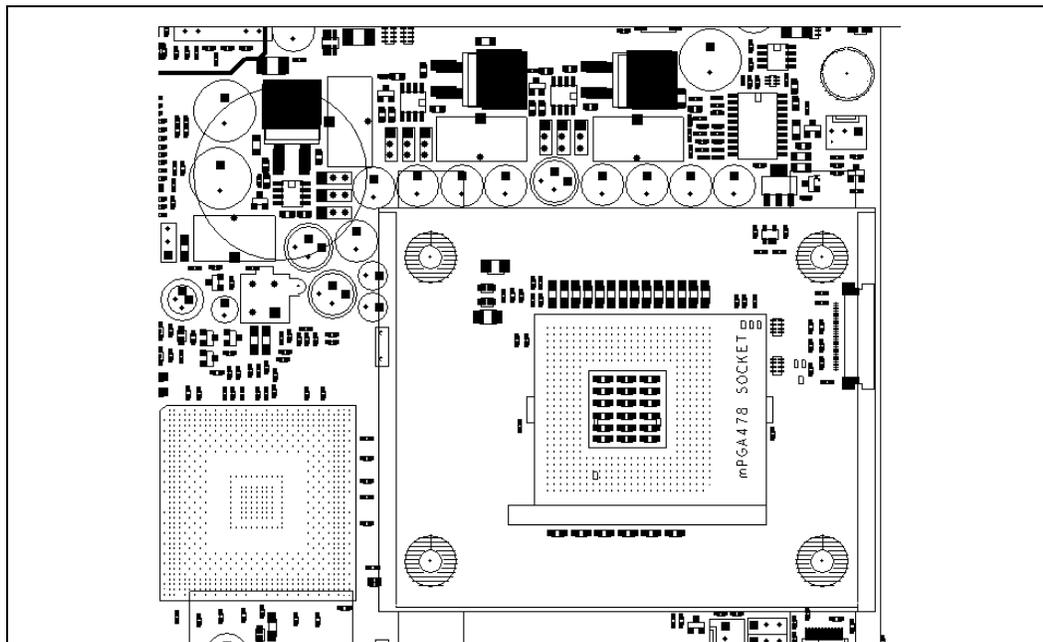
Specifications for the processor voltage are contained in the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*. These specifications are for the processor die. For guidance on correlating the die specifications to socket level measurements, refer to the socket loadlines in the *Intel® Pentium® 4 Processor VR Down Design Guidelines*.

The voltage tolerance of the loadlines contained in the referenced documents help the system designer to achieve a flexible motherboard design solution for many different frequencies of the processor. Failure to meet the load line requirements when modeling the system power delivery may result in a system that is not upgradeable.

The processor requires local regulation because of its higher current requirements, and to maintain power supply tolerance. For example, an on-board DC-to-DC converter converts a higher DC voltage to a lower level using either a linear or a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses ($I \times R$). More important, a discrete regulator regulates the voltage locally, which minimizes DC line losses by reducing motherboard resistance on the processor voltage. Figure 25 shows an example of the placement of the local voltage regulation circuitry.

In this section, North and South are used to describe a specific side of the socket based on the placement of the customer reference board shown in Figure 10. North refers to the side of the processor closest to the back panel, and South refers to the side of the processor closest to the system memory.

Figure 25. VR Component Placement



4.6.2 Decoupling Requirements

Proper bulk and high frequency decoupling is required for the processor voltage regulator circuitry to meet the transient specifications of the processor. The decoupling requirements for the processor power delivery are described in Table 17:

Table 17. Decoupling Requirements

Capacitance	ESR (Each)	ESL (Each)	Ripple Current Rating (Each)	Notes
9 OSCONs*, 560 μ F	9.28 m Ω , max	6.4 nH, max	4.080 A	1
3 Al Electrolytic, 3300 μ F	12 m Ω	5 nH		1
24 0805 package, 10 μ F				1,2
14 1206 package, 10 μ F	3.5 m Ω , typ	1.15 nH, typ		1,2

NOTES:

1. The ESR, ESL and ripple current values in this table are based on the values used in power delivery simulation by Intel, and are not vendor specifications.
2. If only 1206s are used, 38 are required.

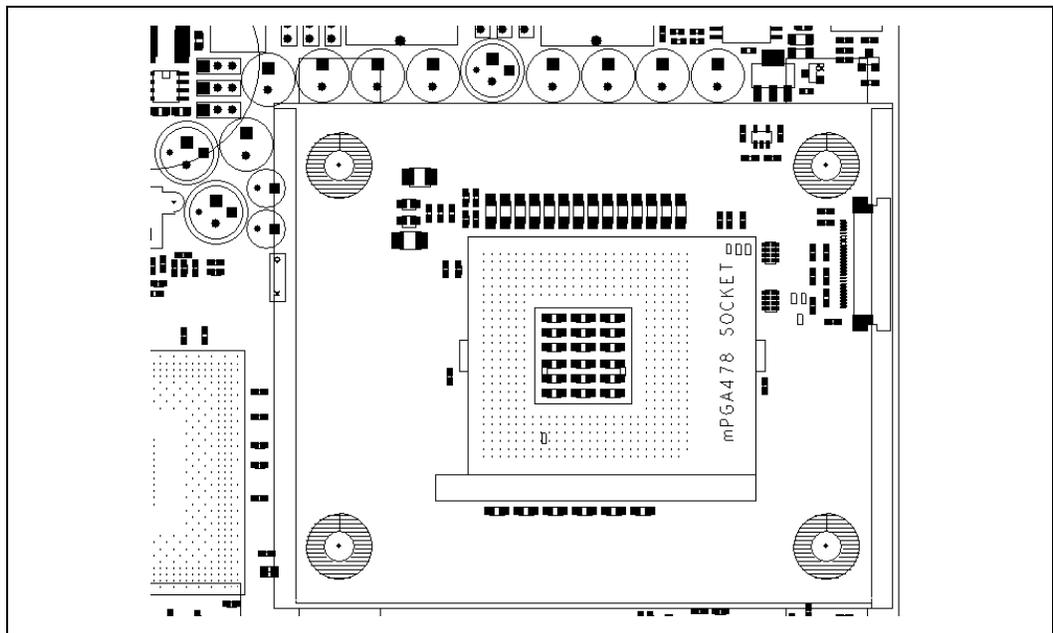
The decoupling should be placed as close as possible to the processor power pins. Table 18 and Figure 26 describe the recommended placement.

Table 18. Decoupling Locations

Type	Number	Location
560 μ F OSCONs*	9	North side of the processor as close as possible to the keep-out area for the retention mechanism.
Al Electrolytic, 3300 μ F	3	North side of the processor as close as possible to the keep-out area for the retention mechanism.
1206 package, 10 μ F	14	North side of the processor as close as possible to the processor socket.
0805 package, 10 μ F	18	Inside the processor socket cavity.
0805 package, 10 μ F	6	South side of the processor as close as possible to the processor socket.

NOTE: If (38) 1206s are used, place 14 north, 10 inside, and 14 south of the socket.

Figure 26. Decoupling Placement



4.6.3 Layout

All four layers in the processor area should be used for power delivery. Two layers should be used for VCC_CPU, and two layers should be used for ground. Traces are not sufficient for supplying power to the processor because of the high current and low resistance required to meet the processor voltage specifications. To satisfy these requirements, shapes that encompass the power delivery part of the processor pin field are required. The following figures show examples of how to use shapes to deliver power to the processor.

Figure 27. Top Layer Power Delivery Shape (VCC_CPU)

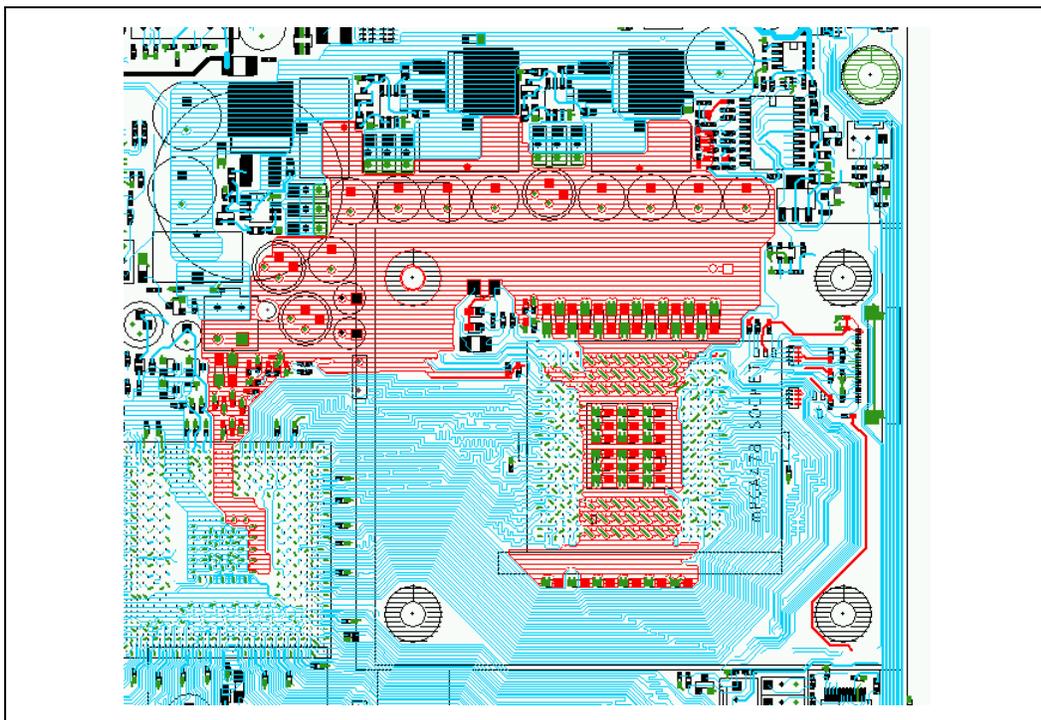


Figure 28. Layer 2 Power Delivery Shape (VSS)

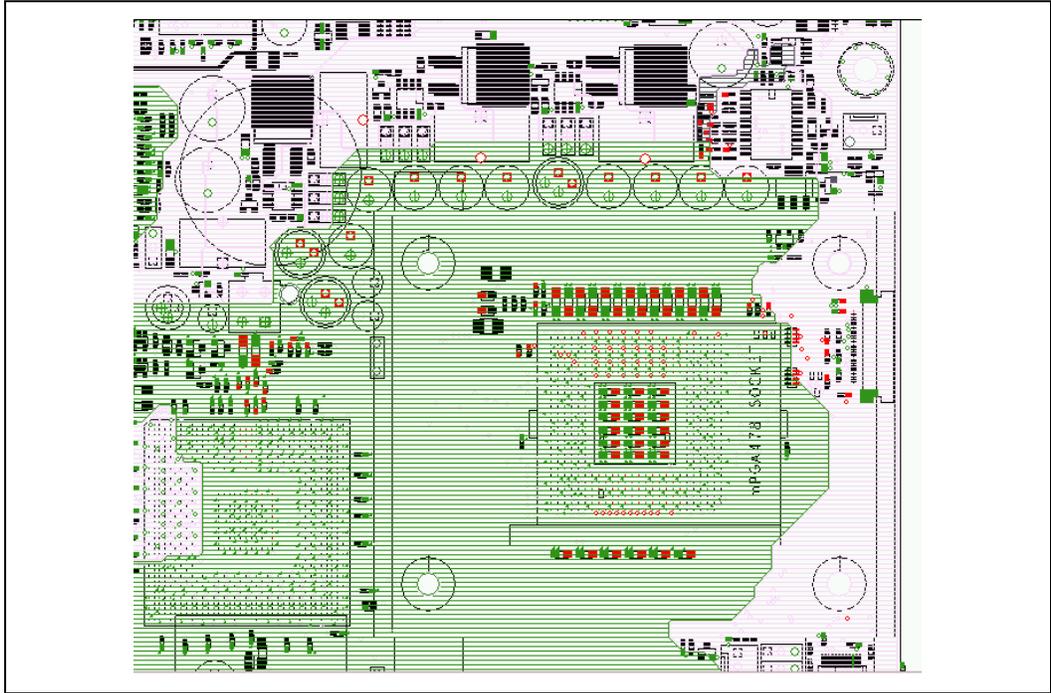


Figure 29. Layer 3 Power Delivery Shape (VSS)

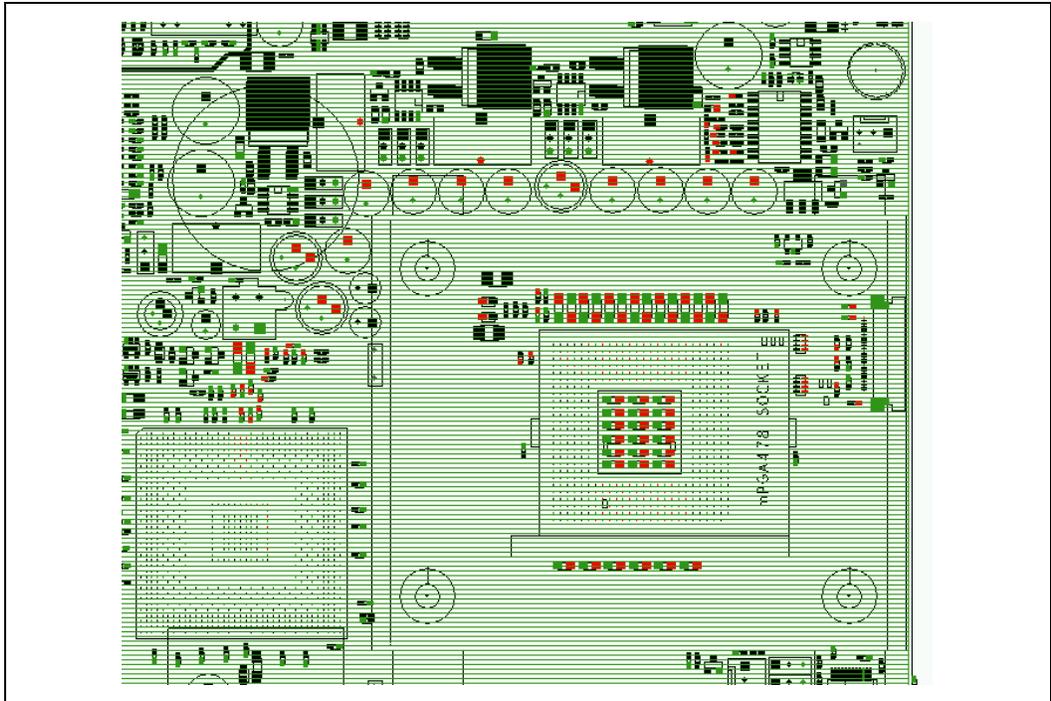
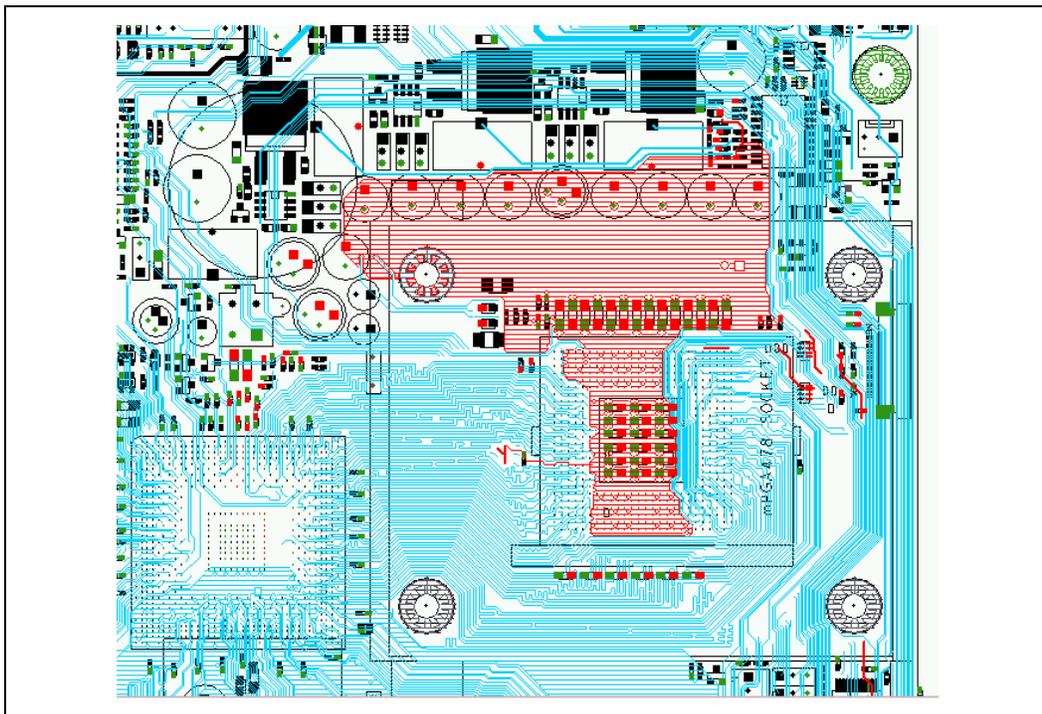
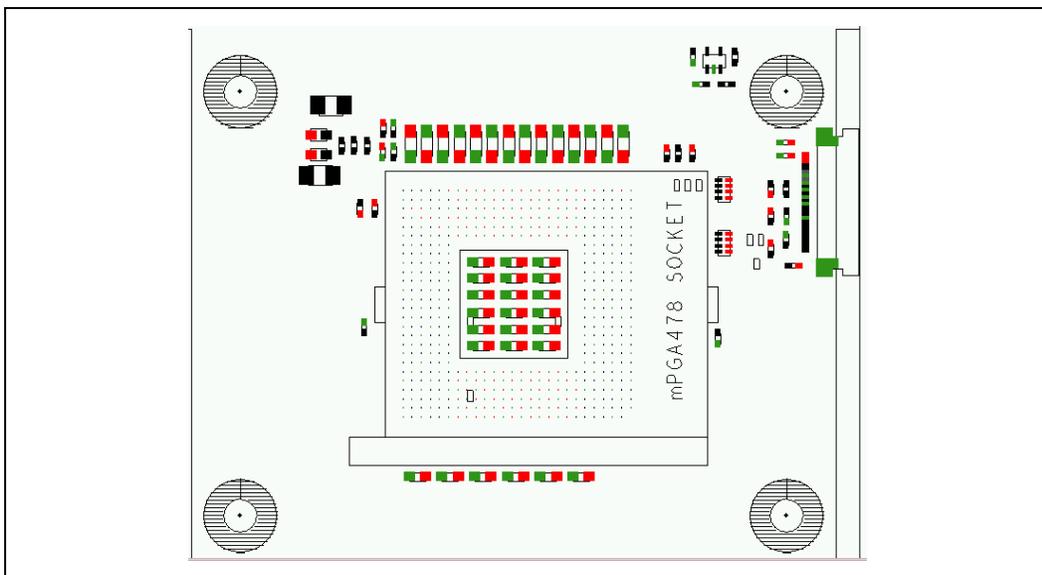


Figure 30. Bottom Layer Power Delivery Shape (VCC_CPU)



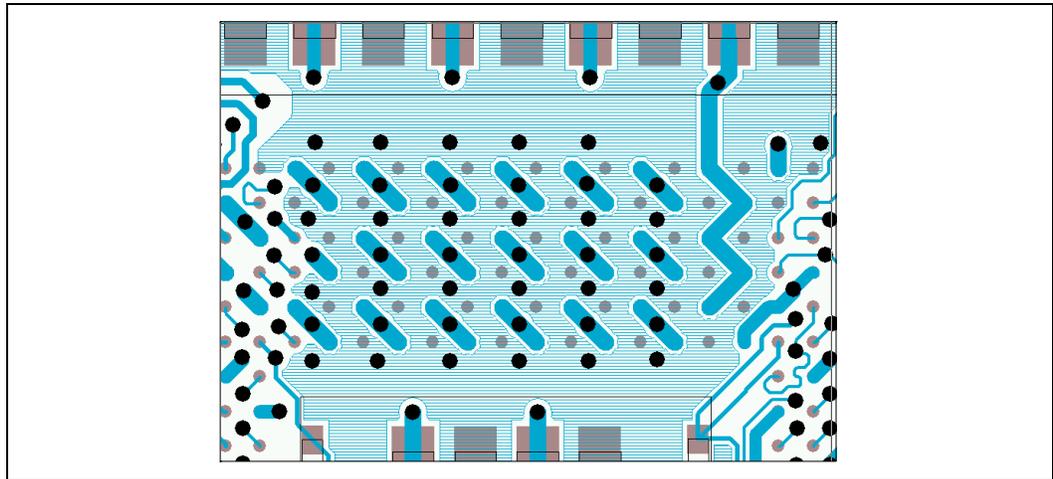
The high frequency decoupling capacitors on the North side and within the socket cavity should be placed with alternating VCC_CPU and VSS to provide a better path for power delivery through the capacitor field. An example of this placement is shown in Figure 31.

Figure 31. Alternating VCC_CPU/VSS Capacitor Placement

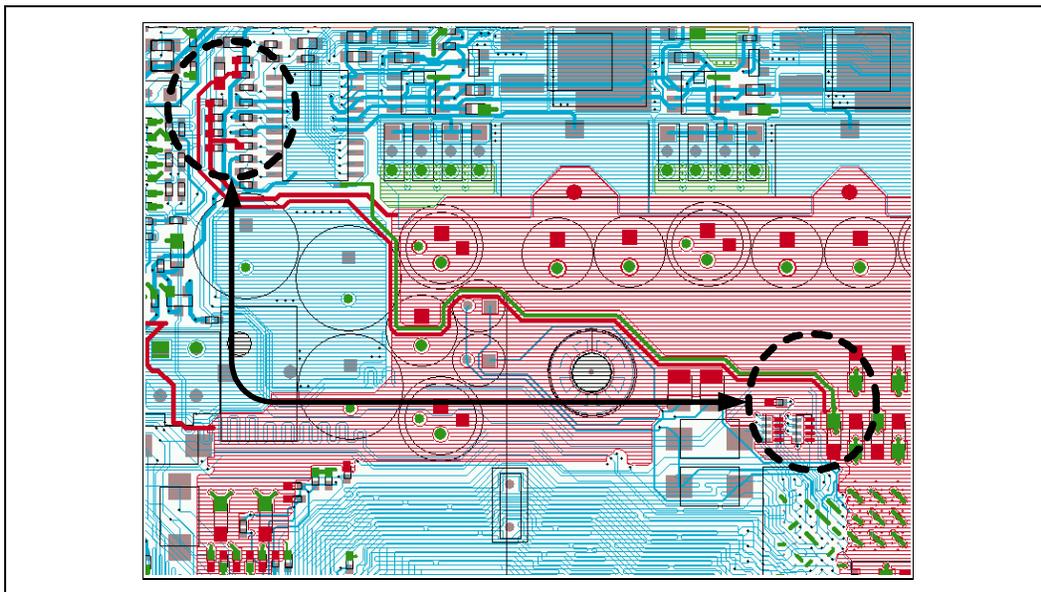


The processor socket has 478 pins with 50-mil pitch. The routing of the signals, power and ground pins require creation of many vias. These vias cut up the power and ground planes beneath the processor, resulting in increased inductance of these planes. To provide the best path through the via field, it is recommended that vias be shared for every two processor ground pins, and for every two processor power pins. Figure 32 shows this via sharing.

Figure 32. Shared Power and Ground Vias



The switching voltage regulators typically used for processor power delivery require the use of a feedback signal for output error correction. The VCC_SENSE and VSS_SENSE pins on the processor should not be used for generating this feedback. These pins should be used as measurement points for lab measurements only. They can be routed to a test point or via on the back of the motherboard with a trace that is a maximum length of 100 mils for this purpose. The socket loadline defined in the Intel® Pentium® 4 Processor VR Down Design Guidelines is defined from pins AC14 (VCC_CPU) and AC15 (VSS), and should be validated from these pins as well. These pins are located approximately in the center of the pin field on the North side of the processor. Feedback for the voltage regulator controller should therefore be taken close to this area of the power delivery shape. Figure 33 shows an example routing of the feedback signal. It is routed as a trace from the 1206 capacitor in the Northwest corner of the processor back to the voltage regulator controller. Because the feedback in this case is not taken from the exact point that defines the socket loadline (pins AC14/AC15), it is important to consider any voltage drop from the feedback point to these pins in the design.

Figure 33. Routing of VR Feedback Signal

4.6.4 Thermal Considerations

For a power delivery solution to meet the flexible motherboard (FMB) requirements, it must be able to deliver a high current. This high current also requires that the solution be able to dissipate the associated heat generated by the components, and keeps all of the components and the PCB within their thermal specifications. OEMs should evaluate their component configurations, system airflow, and layout to ensure adequate thermal performance of the processor power delivery solution.

4.6.5 Simulation

To completely model the system board, one must include the inductance and resistance that exists in the cables, connectors, PCB planes, pins and body of components (such as resistors and capacitors), processor socket, and the voltage regulator module. More detailed models showing these effects are shown in Figure 34.

Figure 34. Detailed Power Distribution Model for Processor with Voltage Regulator on System Board

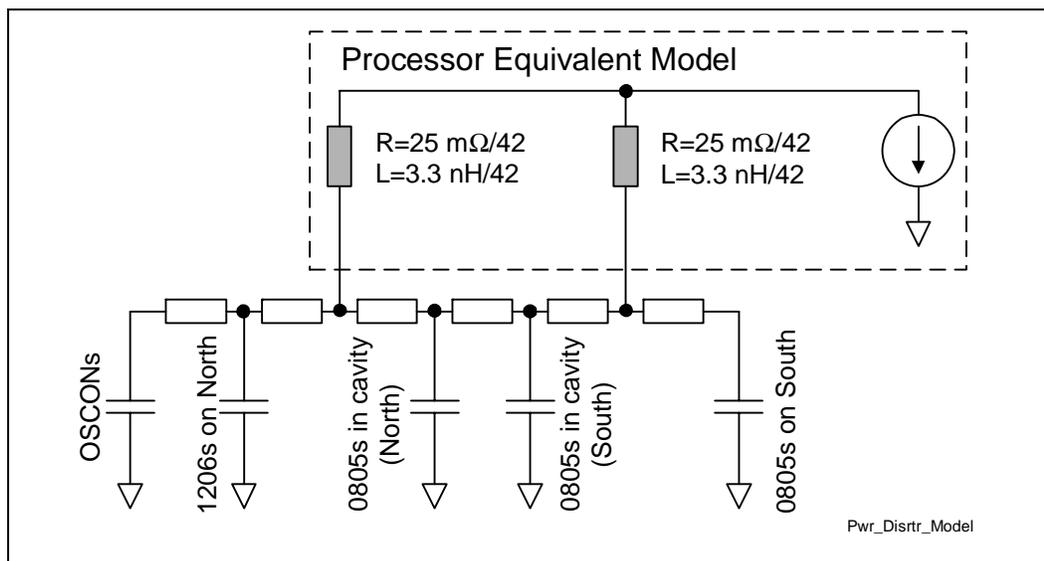


Table 19 lists model parameters for the system board shown in Figure 10. The values listed may be different, depending on board layout.

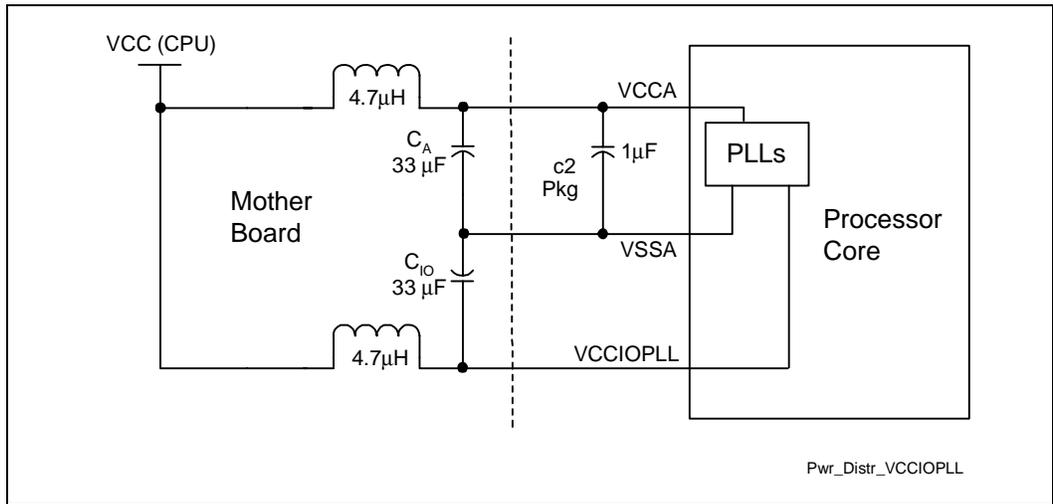
Table 19. Intel® Pentium® 4 Processor Power Delivery Model Parameters

Segment	Resistance	Inductance
L1	0.27 mΩ	80 pH
L2	0.33 mΩ	11.3 pH
L3	0.392 mΩ	104 pH
L4	0.196 mΩ	52 pH
L5	0.392 mΩ	104 pH
L6	0.64 mΩ	200 pH

4.6.5.1 Filter Specifications For VCCA, VCCIOPLL, and VSSA

VCCA and VCCIOPLL are power sources required by the PLL clock generators on the processor silicon. Because these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from VCC. The general desired filter topology is shown in Figure 35. Not shown in the core is parasitic routing. Excluded from the external circuitry are parasitics associated with each component.

Figure 35. Typical VCCIOPLL, VCCA, and VSSA Power Distribution



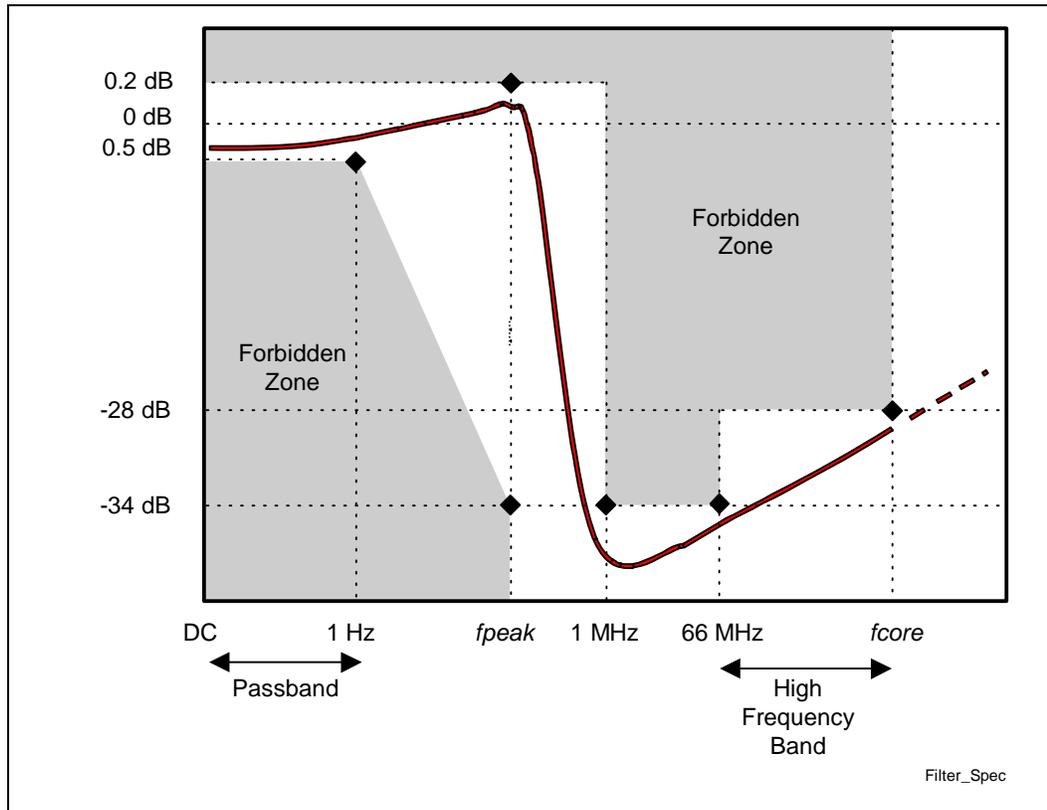
The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity, this document addresses the recommendation for the VCCA filter design. The same characteristics and design approach is applicable for the VCCIOPLL filter design.

The AC low-pass recommendation, with input at VCC and output measured across the capacitor (C_A or C_{IO} in Figure 35), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter recommendation (AC) is graphically shown in Figure 36.

Figure 36. Filter Recommendation



NOTES:

1. Diagram not to scale.
2. No specification for frequencies beyond f_{core} (core frequency).
3. f_{peak} , if existent, should be less than 0.05 MHz.

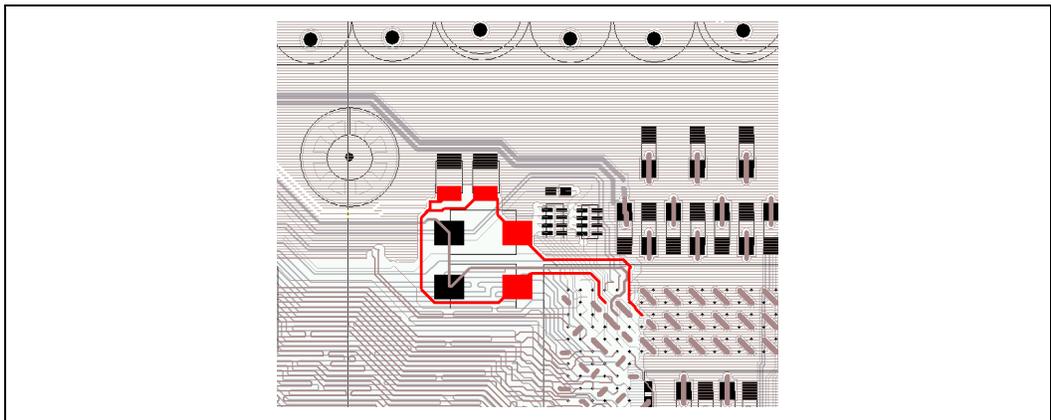
Other recommendations:

- Use shielded type inductors to minimize magnetic pickup
- Capacitors for the filter can be any value between 22 μF and 100 μF as long as components with $\text{ESL} \leq 5 \text{ nH}$ and $\text{ESR} < 0.3 \Omega$ are used.
- Values of either 4.7 μH or 10 μH may be used for the inductor.
- The filter should support DC current $> 60 \text{ mA}$.
- The DC voltage drop from VCC to VCCA should be $< 60 \text{ mV}$.
- To maintain a DC drop of less than 60 mV, the total DC resistance of the filter from VCC_CPU to the processor socket should be a maximum of 1 Ω .

Other routing requirements:

- C should be within 600 mils of the VCCA and VSSA pins. An example of the component placement is shown in Figure 37.
- VCCA route should be parallel and next to VSSA route (minimize loop area).
- A minimum of a 12mil trace should be used to route from the filter to the processor pins.
- L should be close to C.

Figure 37. Example Component Placement for PLL Filter



4.6.6 Electrostatic Discharge Platform Recommendations

Electrostatic discharge (ESD) into a system can lead to system instability and can cause functional failures when a system is in use. There are system level design methodologies that when followed can lead to higher ESD immunity. Electromagnetic fields due to ESD are introduced into a system through chassis openings such as the I/O back panel and PCI slots. These fields can introduce noise into signals and can cause the system to malfunction. One can reduce the potential for issues at the I/O area by adding more ground plane on the motherboard around the I/O area. This can lead to a higher ESD immunity.

Intel recommends that the I/O area on the top and bottom signal layers of a 4-layer motherboard near the I/O back panel be filled with a ground fill as shown in the following figures. In addition, a ground fill cutout should be placed on the VCC layer in the area where the ground fill is placed on the top and bottom layers. Intel recommends filling the I/O area as much as possible without effecting the signal routing. The board designer should fill the entire I/O area along the board edge.

The spacing from the ground fill to other shapes/traces should be at least 20 mils. It is recommended that these ground fill areas be connected to two chassis mounting holes (as shown in Figure 39). This will allow ESD current to travel to the chassis instead of the board. Ground stitching vias should be placed throughout the entire ground fill if possible. It is important that the vias are placed along the board edge. Ground stitching vias for the ground fill should be 100–150 mils apart or less.

Intel recommends the following:

- Fill the I/O area with the ground fill in all layers including signal layers whenever possible.
- Extend the ground fill along the entire back I/O area.
- Connect the ground fill to mounting holes.
- Place stitching vias 100 – 150 mils apart in the entire ground fill.

Figure 38. Top Signal Layer Before the Ground Fill Near the I/O Area

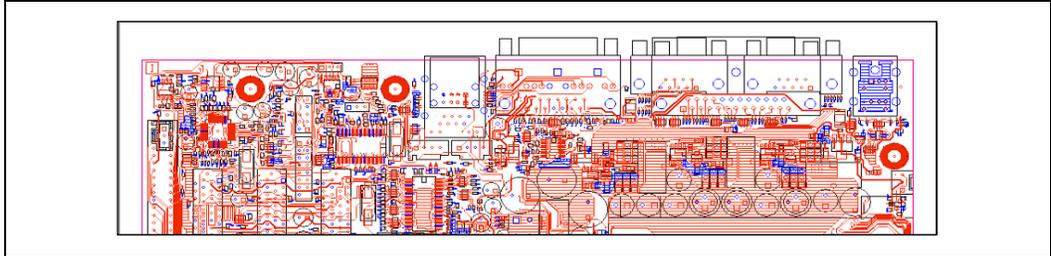


Figure 39. Top Signal Layer After the Ground Fill Near the I/O Area

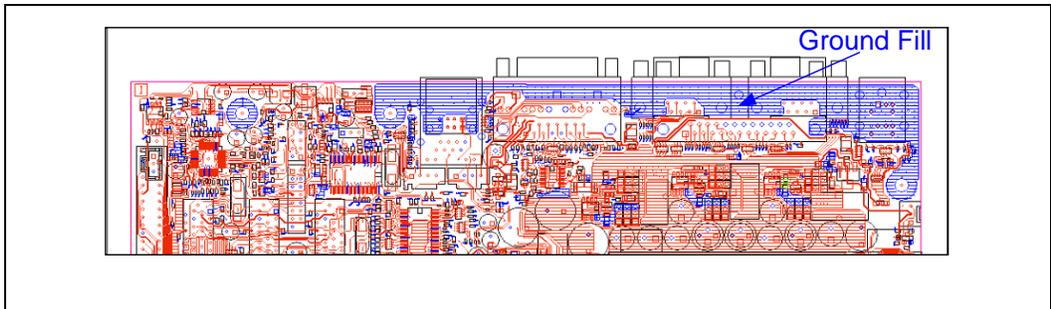


Figure 40. Bottom Signal Layer Before the Ground Fill Near the I/O Area

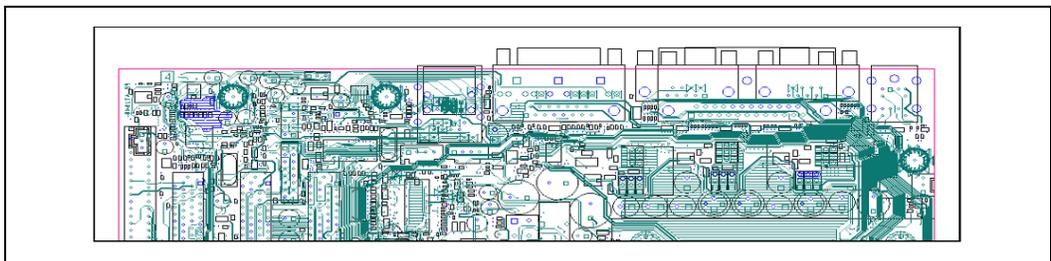
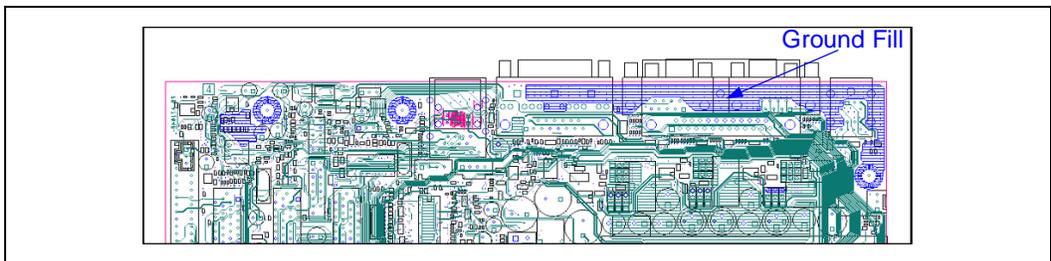


Figure 41. Bottom Signal Layer After the Ground Fill Near the I/O Area





4.7 Intel® Pentium® 4 Processor and Intel® GMCH PSB Package Lengths

Table 20. Processor / Intel® GMCH PSB Package Lengths

Processor Lengths			Intel® GMCH Lengths		
Signal	Processor Ball	Length (inches)	Signal	GMCH Ball	Length (inches)
Address Group 0					
ADSTB0#	L5	0.210	HADSTB_0#	AB35	0.569
A3#	K2	0.368	HA_3#	W31	0.362
A4#	K4	0.265	HA_4#	AA33	0.468
A5#	L6	0.155	HA_5#	AB30	0.353
A6#	K1	0.415	HA_6#	V34	0.520
A7#	L3	0.304	HA_7#	Y36	0.597
A8#	M6	0.144	HA_8#	AC33	0.497
A9#	L2	0.372	HA_9#	Y35	0.575
A10#	M3	0.327	HA_10#	AA36	0.636
A11#	M4	0.246	HA_11#	AC34	0.521
A12#	N1	0.394	HA_12#	AB34	0.566
A13#	M1	0.408	HA_13#	Y34	0.516
A14#	N2	0.349	HA_14#	AB36	0.612
A15#	N4	0.241	HA_15#	AC36	0.604
A16#	N5	0.198	HA_16#	AC31	0.465
REQ0#	J1	0.427	HREQ_0#	V36	0.594
REQ1#	K5	0.207	HREQ_1#	AA31	0.413
REQ2#	J4	0.270	HREQ_2#	W33	0.443
REQ3#	J3	0.337	HREQ_3#	AA34	0.535
REQ4#	H3	0.356	HREQ_4#	W35	0.555
Address Group 1					
ADSTB1#	R5	0.214	HADSTB_1#	AF30	0.442
A17#	T1	0.470	HA_17#	AF35	0.631
A18#	R2	0.404	HA_18#	AD36	0.617
A19#	P3	0.303	HA_19#	AD35	0.598
A20#	P4	0.246	HA_20#	AE34	0.558
A21#	R3	0.334	HA_21#	AD34	0.566



Processor Lengths			Intel® GMCH Lengths		
Signal	Processor Ball	Length (inches)	Signal	GMCH Ball	Length (inches)
A22#	T2	0.388	HA_22#	AE36	0.623
A23#	U1	0.458	HA_23#	AF36	0.663
A24#	P6	0.156	HA_24#	AE33	0.508
A25#	U3	0.379	HA_25#	AF34	0.553
A26#	T4	0.281	HA_26#	AG34	0.634
A27#	V2	0.417	HA_27#	AG36	0.663
A28#	R6	0.166	HA_28#	AE31	0.531
A29#	W1	0.493	HA_29#	AH35	0.658
A30#	T5	0.217	HA_30#	AG33	0.557
A31#	U4	0.285	HA_31#	AG31	0.494
Data Group 0					
DSTBN0#	E22	0.338	HDSTB_N0#	N31	0.520
DSTBP0#	F21	0.326	HDSTB_P0#	L31	0.528
D0#	B21	0.414	HD_0#	T30	0.385
D1#	B22	0.475	HD_1#	R33	0.465
D2#	A23	0.538	HD_2#	R34	0.544
D3#	A25	0.608	HD_3#	N34	0.578
D4#	C21	0.386	HD_4#	R31	0.400
D5#	D22	0.386	HD_5#	L33	0.540
D6#	B24	0.535	HD_6#	L36	0.632
D7#	C23	0.464	HD_7#	P35	0.575
D8#	C24	0.515	HD_8#	J36	0.691
D9#	B25	0.590	HD_9#	K34	0.561
D10#	G22	0.274	HD_10#	K36	0.652
D11#	H21	0.203	HD_11#	M30	0.383
D12#	C26	0.589	HD_12#	M35	0.612
D13#	D23	0.462	HD_13#	L34	0.588
D14#	J21	0.183	HD_14#	K35	0.620
D15#	D25	0.550	HD_15#	H36	0.695
DBI0#	E21	0.309	DINV_0#	N33	0.560
Data Group 1					
DSTBN1#	K22	0.301	HDSTB_N1#	G33	0.646
DSTBP1#	J23	0.306	HDSTB_P1#	J34	0.777



Processor Lengths			Intel® GMCH Lengths		
Signal	Processor Ball	Length (inches)	Signal	GMCH Ball	Length (inches)
D16#	H22	0.272	HD_16#	G34	0.660
D17#	E24	0.480	HD_17#	G36	0.728
D18#	G23	0.358	HD_18#	J33	0.526
D19#	F23	0.418	HD_19#	D35	0.787
D20#	F24	0.443	HD_20#	F36	0.747
D21#	E25	0.508	HD_21#	F34	0.696
D22#	F26	0.513	HD_22#	E36	0.793
D23#	D26	0.597	HD_23#	H34	0.644
D24#	L21	0.176	HD_24#	F35	0.696
D25#	G26	0.524	HD_25#	D36	0.818
D26#	H24	0.412	HD_26#	H35	0.645
D27#	M21	0.171	HD_27#	E33	0.687
D28#	L22	0.245	HD_28#	E34	0.739
D29#	J24	0.401	HD_29#	B35	0.846
D30#	K23	0.313	HD_30#	G31	0.548
D31#	H25	0.473	HD_31#	C36	0.876
DBI1#	G25	0.458	DINV_1#	C35	0.786
Data Group 2					
DSTBN2#	K22	0.252	HDSTB_N2#	C30	0.694
DSTBP2#	J23	0.266	HDSTB_P2#	E29	0.616
D32#	M23	0.300	HD_32#	D33	0.750
D33#	N22	0.226	HD_33#	D30	0.672
D34#	P21	0.178	HD_34#	D29	0.621
D35#	M24	0.371	HD_35#	E31	0.627
D36#	N23	0.271	HD_36#	D32	0.694
D37#	M26	0.454	HD_37#	C34	0.802
D38#	N26	0.437	HD_38#	B34	0.878
D39#	N25	0.383	HD_39#	D31	0.661
D40#	R21	0.165	HD_40#	G29	0.514
D41#	P24	0.343	HD_41#	C32	0.762
D42#	R25	0.381	HD_42#	B31	0.751
D43#	R24	0.329	HD_43#	B32	0.800
D44#	T26	0.420	HD_44#	B30	0.754



Processor Lengths			Intel® GMCH Lengths		
Signal	Processor Ball	Length (inches)	Signal	GMCH Ball	Length (inches)
D45#	T25	0.380	HD_45#	B29	0.716
D46#	T22	0.221	HD_46#	E27	0.570
D47#	T23	0.279	HD_47#	C28	0.718
DBI2#	P26	0.441	DINV_2#	B33	0.825
Data Group 3					
DSTBN3#	W22	0.298	HDSTB_N3#	D25	0.596
DSTBP3#	W23	0.300	HDSTB_P3#	E25	0.606
D48#	U26	0.419	HD_48#	B27	0.718
D49#	U24	0.324	HD_49#	D26	0.633
D50#	U23	0.270	HD_50#	D28	0.663
D51#	V25	0.384	HD_51#	B26	0.692
D52#	U21	0.167	HD_52#	G27	0.599
D53#	V22	0.252	HD_53#	H26	0.577
D54#	V24	0.341	HD_54#	B25	0.666
D55#	W26	0.447	HD_55#	C24	0.591
D56#	Y26	0.454	HD_56#	B23	0.645
D57#	W25	0.426	HD_57#	B24	0.715
D58#	Y23	0.336	HD_58#	E23	0.482
D59#	Y24	0.386	HD_59#	C22	0.586
D60#	Y21	0.222	HD_60#	G25	0.459
D61#	AA25	0.426	HD_61#	B22	0.632
D62#	AA22	0.268	HD_62#	D24	0.583
D63#	AA24	0.394	HD_63#	G23	0.399
DBI3#	V21	0.202	DINV_3#	C26	0.689

5 DDR System Memory Design Guidelines

The 845G chipset Double Data Rate (DDR) SDRAM system memory interface provides support for DDR200 or DDR266 memory.

The first two sections in this chapter provide information about the DDR reference stack-up. The third section describes the DDR topologies, layout, and routing guidelines organized by signal group:

Note: The recommended routing order is listed in the beginning of Section 5.2.

Table 21. Intel® 845G Chipset DDR Signal Groups

Section	Group	Signal Name	Description
5.2.1	Data	SDQ_[63:0]	Data Bus
		SDM_[7:0]	Data Masks
		SDQS_[7:0]	Data Strobes
5.2.2	Control	SCKE_[3:0]	Clock Enable
		SCS_[3:0]#	Chip Select
5.2.3	Address / Command	SMAA_[12:6, 3, 0]	Memory Address Bus
		SBA_[1:0]	Bank Address (Bank Select)
		SRAS#	Row Address Select
		SCAS#	Column Address Select
		SWE#	Write Enable
5.2.4	CPC Address	SMAA_[5,4,2,1]	Memory Address Bus CPC signals
		SMAB_[5,4,2,1]	Memory Address Bus CPC signals
5.2.5	Clocks**	SCMDCLK_[5:0]	DDR-SDRAM Differential Clocks
		SCMDCLK_[5:0]#	DDR-SDRAM Inverted Differential Clocks
5.2.6	Feedback	SRCVEN_OUT#	Output Feedback Signal
		SRCVEN_IN#	Input Feedback Signal

The remaining two sections contain information and details on the system memory bypass capacitor guidelines and DDR power delivery requirements. Together, these design guidelines provide for a robust DDR solution for an 845G chipset-based design.

The DDR SDRAM system memory interface is multiplexed with SDR. For DDR board designs, the MEMSEL strap has an internal pull-up and is left as a No Connect (refer to the *Intel® 845G/845GL/845GV Chipset Datasheet* for additional information). The DDR guidelines should be used for designing a DDR system board. Although the GMCH directly supports SDR or DDR SDRAM channel, **the DDR guidelines must not be used for SDR designs.**

The 845G chipset does not support Error Checking and Correction (ECC). Refer to the *Intel® 845G/845GL/845GV Chipset Datasheet* for more signal details.

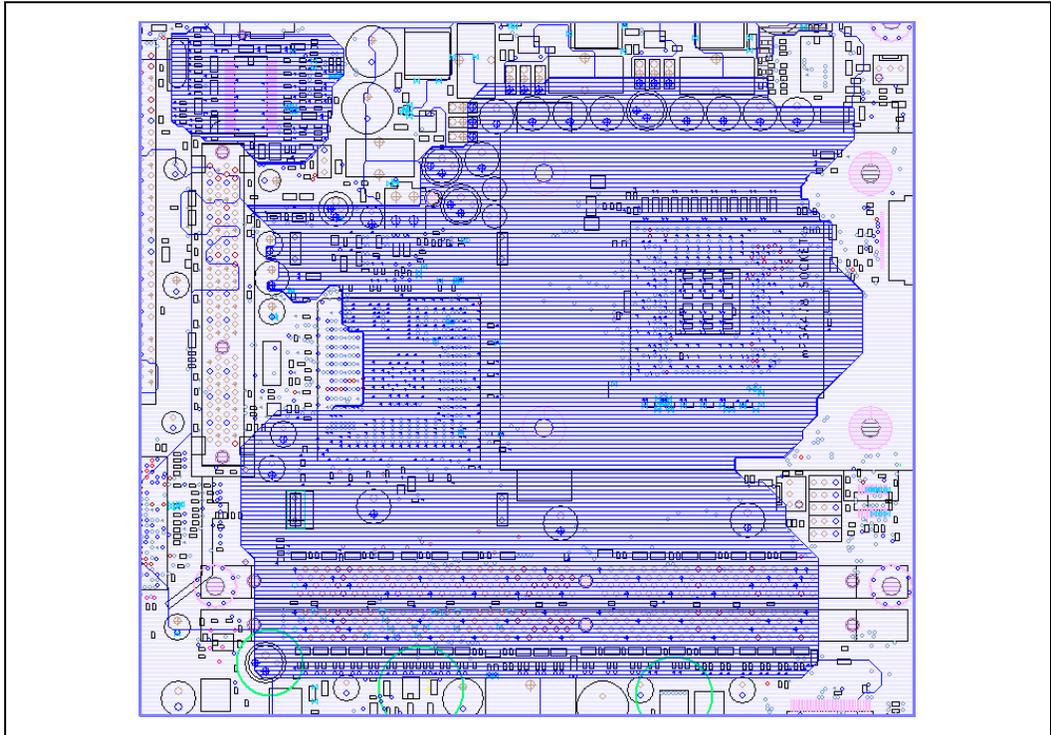
5.1 DDR-SDRAM Stack-up and Referencing Guidelines

The 845G chipset platform designs using the DDR-SDRAM memory sub-system requires continuous ground referencing for all DDR signals. Based on the four-layer stack-up in Section 3.2, the DDR channel requires the following referencing stack-up to ground reference all of the DDR signals from the GMCH to the parallel termination at the end of the channel. Note that the DDR channel stack-up applies to the DDR channel only.

Table 22. DDR Channel Referencing Stack-up

Motherboard Layer	Description
Layer 1	Signal / Power
Layer 2	Ground Flood
Layer 3	Ground
Layer 4	Signal / Power

A solid continuous ground flood must be placed under the DDR channel on layer two from the GMCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel to provide an optimal current return path. Any split in the ground flood will provide a sub-optimal return path. The DDR and the processor ground flood must be connected to together, as shown in Figure 42.

Figure 42. Layer Two Preliminary Ground Flood Picture

Ground Stitching

The ground flood must be well stitched to the ground plane on layer three to ensure the same potential between the two layers. Any ground pin or ground via that is placed in the DDR routing area must connect to both the ground flood, and the ground plane:

- DIMM Connector ground pins.
- GMCH DDR ground pins in the DDR interface section.
- Ground ends of the DDR-DIMM high-frequency bypass capacitors.
- Ground vias for the GMCH 2.5 V high frequency decoupling capacitors.
- Ground ends connecting to the VTT termination decoupling capacitors.
- Ground vias wherever possible around the edge of the ground flood.
- Ground vias along the edge where the DDR and PSB ground floods connect on layer two.

5.2 DDR System Memory Topology and Layout Design Guidelines

The 845G chipset Double Data Rate (DDR) SDRAM system memory interface implements SSTL_2 topology. This section is organized by signal group.

- Section 5.2.1 – Data
- Section 5.2.2 – Control
- Section 5.2.3 – Address / Command
- Section 5.2.4 – CPC Address
- Section 5.2.5 – Clock
- Section 5.2.6 – Feedback

Routing Order

To help maximize routing efficiency, the following routing order, which has been developed and optimized for the guidelines, is highly recommended.

1. CPC Address
2. Control (SCS#, SCKE)
3. Clocks¹
4. Address/command
5. Data (includes mask and strobes)

Note: ¹Clock lengths in the following sections refer to the total clock lengths, which are measured from GMCH die to DIMM connector.

The CPC address and control (SCS#, SCKE) signals should be routed first on layer 4 because these signals can help determine the system clock length. A portion of the address/command signal group will likely have to be routed at the same time as the CPC address signals because the address/command signals are intermixed with the CPC address signal routing. Be mindful of the 2.5 V power delivery to the GMCH, which is flooded on Layer 4 in between the various signals on Layer 4 (see Section 5.4)

As an example, after routing the CPC address, take the longest routed CPC address length for each associated DIMM and use the CPC address length matching guidelines to help determine the minimum total target clock length (versus routed length) based on CPC address routing. If the minimum total target clock length for 2nd DIMM is over 0.5" greater than for the 1st DIMM, use the 2nd DIMM target clock length as your base target and subtract 0.5" to get the 1st DIMM target clock length. Do the same for Control signals, and determine whether the CPC address signals or the Control signals are your limiting factor.

Once the total target clock length has been determined, use the DIMM clock matching guidelines (Section 5.2.5) to match all total target clock lengths to each associated DIMM. The difference between the total target clock length for the 1st DIMM and the 2nd DIMM should be 0.5". The remaining address/command and data signals can then be routed.

The following DDR guidelines should be followed based on the 4-layer stack-up (Section 3.2), the GMCH ball field, and the requirement that all DDR signals must be referenced to ground.

5.2.1 Data Signals — SDQ_[63:0], SDQS_[7:0], SDM_[7:0]

The GMCH data signals are source synchronous signals that include the 64-bit wide data bus, 8 data masks (SDM), and 8 data strobe signals (SDQS). There is an associated data strobe (SDQS) for each data (SDQ) and data mask (SDM) group. Table 23 summarizes the SDQ/SDM to SDQS mapping. SDQ/SDM are tuned to SDQS, and SDQS are tuned to SCMD_CLK.

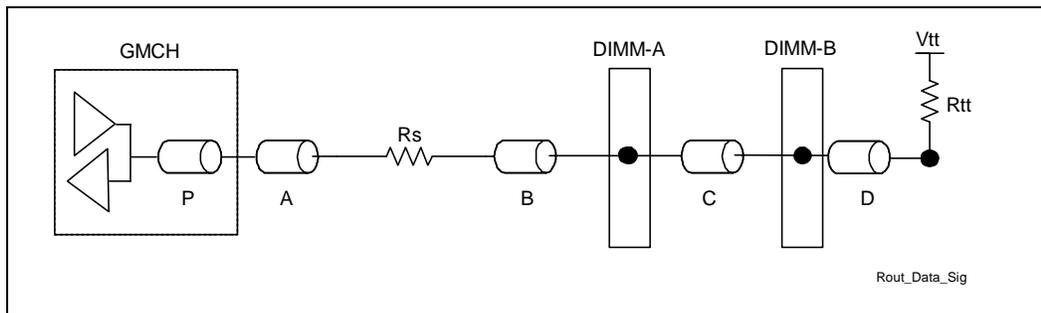
Table 23. SDQ/SDM to SDQS Mapping

SDQ/SDM	SDQS
SDQ_[7:0] / SDM_0	SDQS_0
SDQ_[15:8] / SDM_1	SDQS_1
SDQ_[23:16] / SDM_2	SDQS_2
SDQ_[31:24] / SDM_3	SDQS_3
SDQ_[39:32] / SDM_4	SDQS_4
SDQ_[47:40] / SDM_5	SDQS_5
SDQ_[55:48] / SDM_6	SDQS_6
SDQ_[63:56] / SDM_7	SDQS_7

All data and strobe signals **must** be routed on layer one. The GMCH system memory pinout has been optimized to breakout all the data and strobe signals on the top signal layer. The data signals should break out of the GMCH and route entirely on the top signal layer referenced to ground, from the GMCH to the series termination resistor, from the series termination resistor to the first DIMM, from DIMM to DIMM, and from the second DIMM to the parallel termination.

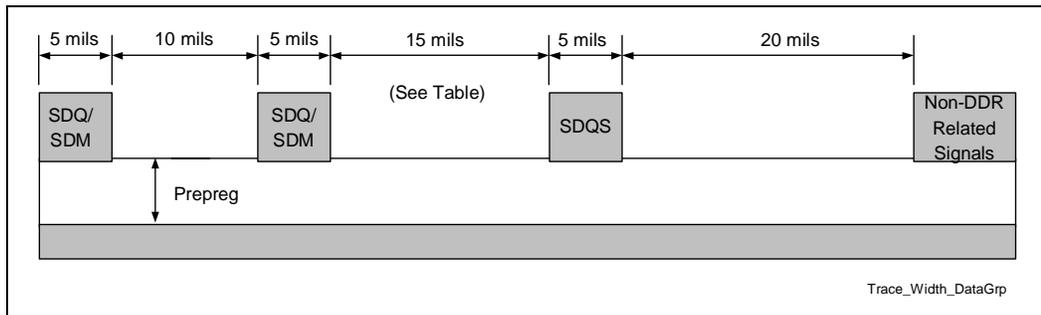
Resistor packs are acceptable for the series (R_s) and parallel (R_{tt}) data and data strobe termination resistors, but data and strobe signals **cannot** be routed to the same resistor pack (RPACK) used by address/command, CPC address, or control signals. Termination resistor packs for the data group must remain dedicated to data group signals, and cannot be used for any other signal groups.

The following figures and table describe the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Figure 43. Data Signal Routing Topology

Table 24. Data Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	Data – SDQ_[63:0], SDQS_[7:0], SDM_[7:0]
Topology	Daisy Chain
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	$60\Omega \pm 15\%$
Nominal Trace Width	5 mils
Nominal Trace Spacing	<ul style="list-style-type: none"> • SDQS to SDQ/SDM = 15 mils • SDQ/SDM to SDQ/SDM = 10 mils • Within DIMM Pin Field = 7 mils minimum • From DIMM to DIMM = 12 mils • 2nd DIMM to Rtt = 7 mils minimum
Group Spacing	Isolation from non-DDR related signals = 20 mils minimum
GMCH Breakout Guidelines	5 mil width with 6 mil spacing for a max of 350 mils. Note: Use of breakout guidelines should be minimized.
Total Trace Length $P + A + B$ – GMCH signal Pad to First DIMM Pin	Max = 5.8" Note: See Section 5.2.7 for package length P.
Trace Length B – Series Termination Resistor Pad to First DIMM Pin	Max = 500 mils The resistor should be placed within 500 mils of the 1st DIMM.
Trace Length C – DIMM Pin to DIMM Pin	Min = 400 mils Max = 600 mils
Trace Length D – Last DIMM Pin to Parallel termination Resistor Pad	Max = 800 mils
Series Resistor (R_s)	$10\Omega \pm 5\%$
Termination Resistor (R_{tt})	$56\Omega \pm 5\%$
Maximum via Count per signal	0 (all signals are routed on the top layer)
Length Tuning Method	<ul style="list-style-type: none"> • SDQ_[63:0] / SDM_[7:0] to associated SDQS_[7:0] • SDQS_[7:0] to SCMDCLK/SCMDCLK_[5:0]# per DIMM See Section 5.2.1.1.1 and Section 5.2.1.1.2 for details

Figure 44. Data Group Signal Trace Width/Spacing Routing



5.2.1.1 Data Group Signal Length Matching Requirements

5.2.1.1.1 Data to Strobe Length Matching Requirements

Data/data mask (SDQ_[63:0], SDM_[7:0]) and data strobe (SDQS_[7:0]) signals **require** tuning from GMCH internal pads to the first DIMM **and** from GMCH internal pads to the second DIMM connector pins for data/data mask to the associated data strobe within each byte group.

SDQS Total Length = X

Associated SDQ/SDM Byte Group Total Length = Y, where $(X - 25 \text{ mils}) \leq Y \leq (X + 25 \text{ mils})$

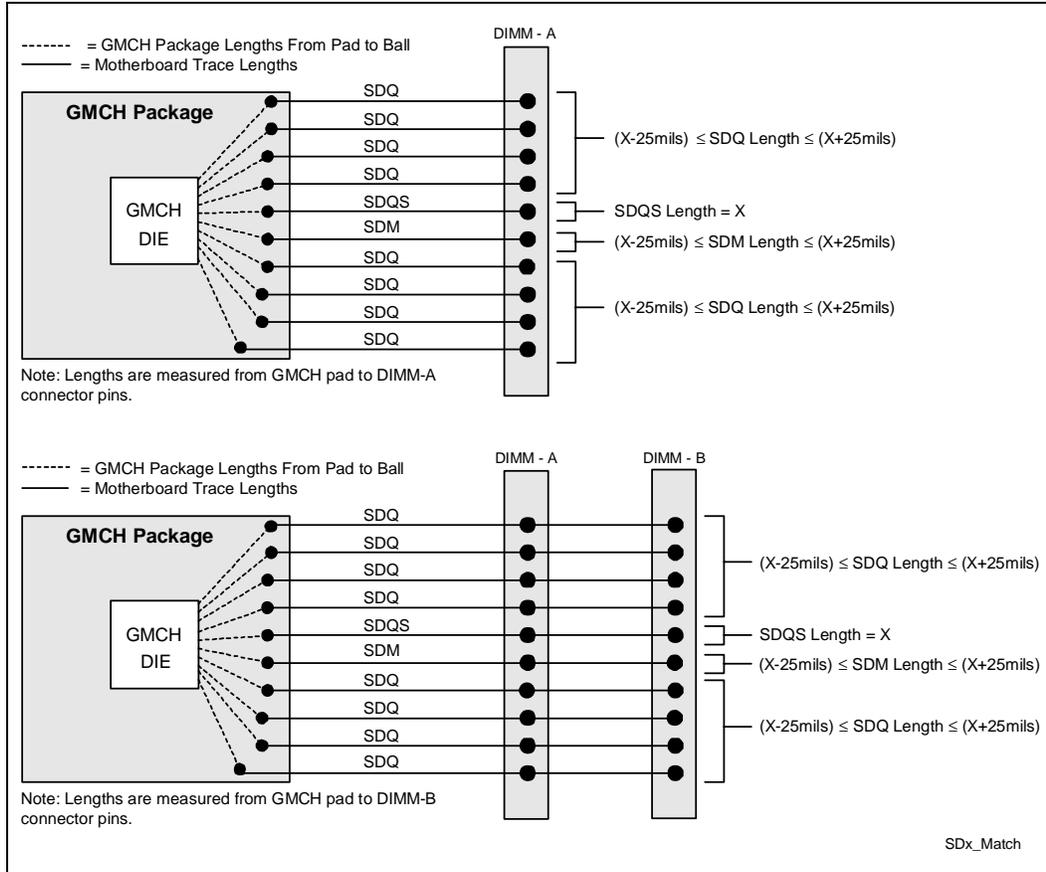
Length X and Y to 1st DIMM includes the GMCH Package Length P + Motherboard Trace Length A + B.

Length X and Y to 2nd DIMM includes the GMCH Package Length P + Motherboard Trace Lengths A + B + C.

SDQS_[7:0] motherboard trace length guidelines A, B and C are described in Table 24. No length matching is required from the second DIMM to the parallel termination resistors. Refer to Section 5.2.7 for GMCH data and strobe package length data.

Figure 45 shows the length matching requirements between the SDQ, SDM, and SDQS signals.

Figure 45. SDQ/SDM to SDQS Trace Length Matching Requirements



5.2.1.1.2 Strobe to Command Clock Length Matching Requirements

Tuning is required from GMCH internal pad to the pins of the DIMM connector for strobe to the differential clock signals.

- On an 845G chipset based DDR platform, the total target data strobe lengths must be longer than the total target differential clock minus 4.4" for the associated DIMM.

$$\text{SCMD_CLK/SCMD_CLK\# Total Length} = X$$

$$\text{SDQS Total Length} = Y, \text{ where } (X - 4.4") \leq Y$$

Length X to 1st and 2nd DIMM includes the GMCH Package Length P + Motherboard Trace Length A.

Length Y to 1st DIMM includes the GMCH Package Length P + Motherboard Trace Lengths A + B.

Length Y to 2nd DIMM includes the GMCH Package Length P + Motherboard Trace Lengths A + B + C

SDQS_[7:0] motherboard trace length guidelines A, B and C are listed in Table 24. No length matching is required from the second DIMM to the parallel termination resistors. Refer to Section 5.2.7 for GMCH data and strobe package length data.

Figure 46 shows the length matching requirements between the SDQS and clock signals.

Figure 46. SDQS to SCMD_CLK/SCMD_CLK# Trace Length Matching Requirements

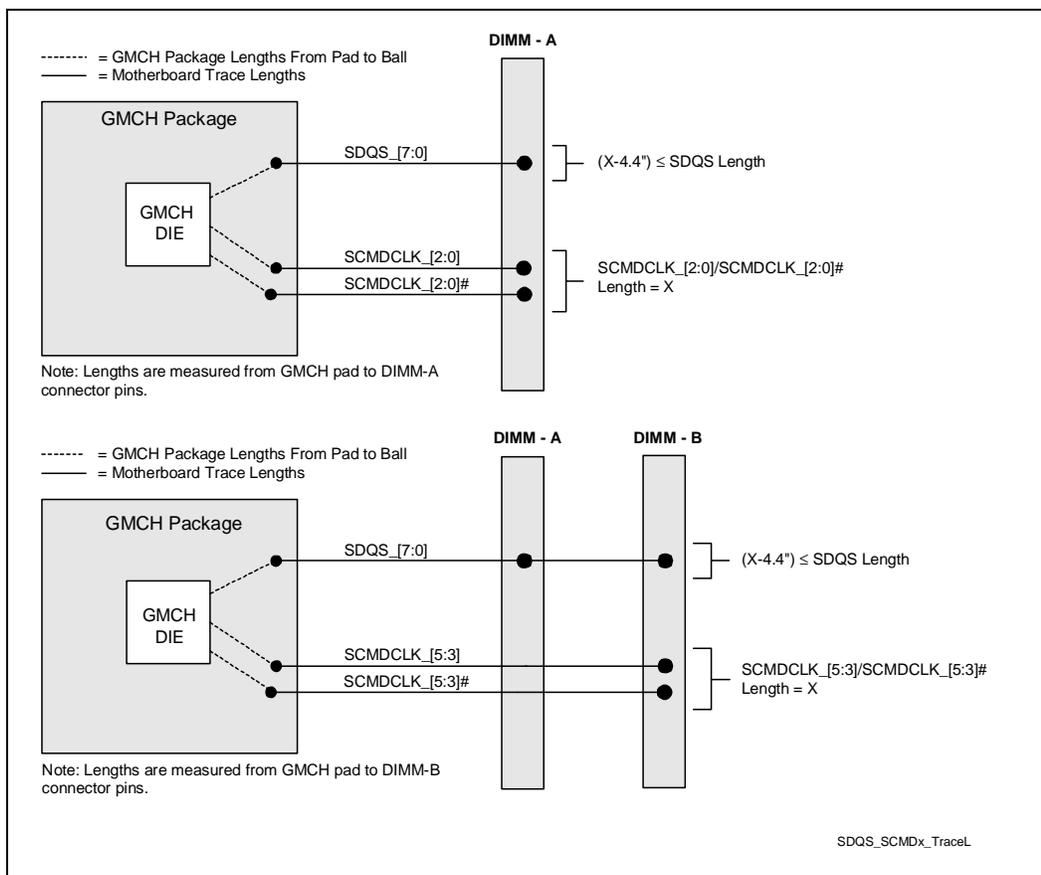
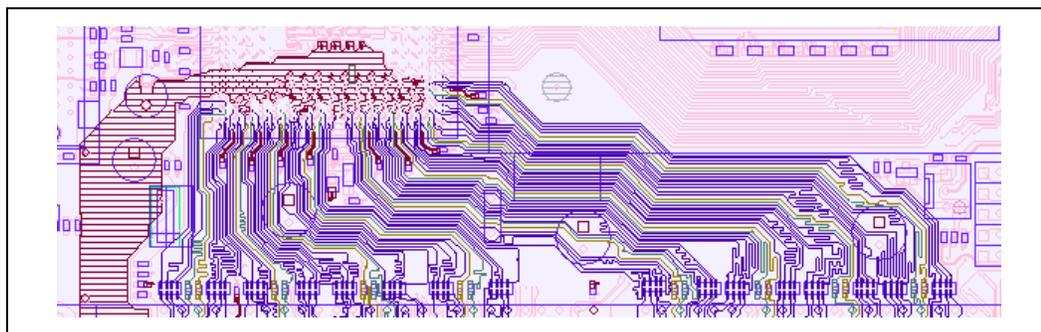


Figure 47. Data Group Top Layer to First DIMM Routing Example



5.2.2 Control Signals — SCKE_[3:0], SCS_[3:0]#

The GMCH control signals that include the enable (SCKE) and chip select (SCS#) are source-clocked signals. One chip select (SCS#) and one clock enable (SCKE) signals are needed per row. SCKE and SCS# are tuned to SCMD_CLK. Table 25 summarizes the SCKE/SCS# to DIMM and DIMM pin mapping.

Table 25. Control Signal DIMM Mapping

Signal	Relative To	DIMM Pin
SCS_0#	DIMMA	157
SCS_1#	DIMMA	158
SCS_2#	DIMMB	157
SCS_3#	DIMMB	158
SCKE_0	DIMMA	21
SCKE_1	DIMMA	111
SCKE_2	DIMMB	21
SCKE_3	DIMMB	111

The GMCH system memory pinout has been optimized to breakout the control signals on the **bottom** signal layer, and all control signals must be routed on the same layer. They should transition from the top signal layer to the bottom signal layer under the GMCH. They should be routed on the bottom signal layer until the first DIMM, or until they transition to the top signal layer within 500 mils before the first DIMM connector. Finally, they should route from the DIMM connector pins to the parallel termination resistors at the end of the memory channel on the top signal layer.

Because the control signals are routed on the bottom signal layer between the GMCH and the first DIMM, 2.5 V flooding on the bottom signal layer is reduced, and the control signals should be kept as short as possible. Also, because the control signals transition signal layers near the first DIMM, a via connecting the ground flood and ground plane on layer two and three should be placed as close as possible to each control signal transition via.

Resistor packs are acceptable for the parallel (R_{tt}) control termination resistors, but the control signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, address/command, or CPC address signals. Termination resistor packs for the control group must remain dedicated to control group signals, and cannot be used for any other signal groups.

The following figures and tables describe the recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

Figure 48. DIMM-A Control Signal Routing Topology (SCS_[1:0]#, SCKE_[1:0])

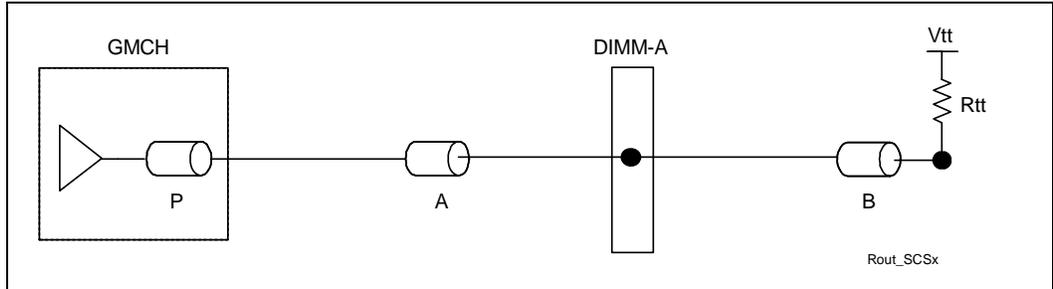


Figure 49. DIMM-B Control Signal Routing Topology (SCS_[3:2]#, SCKE_[3:2])

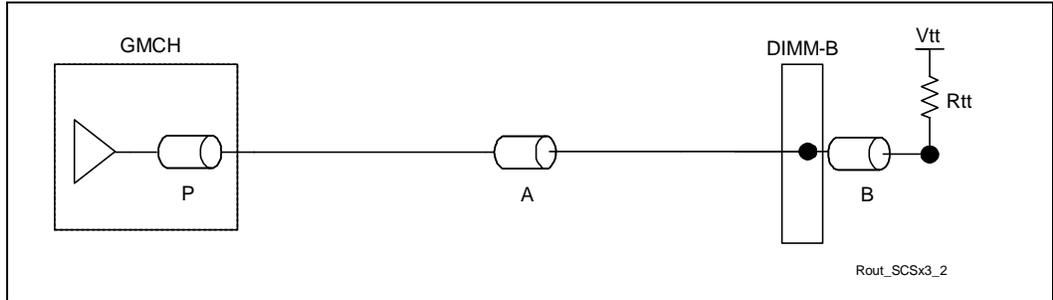
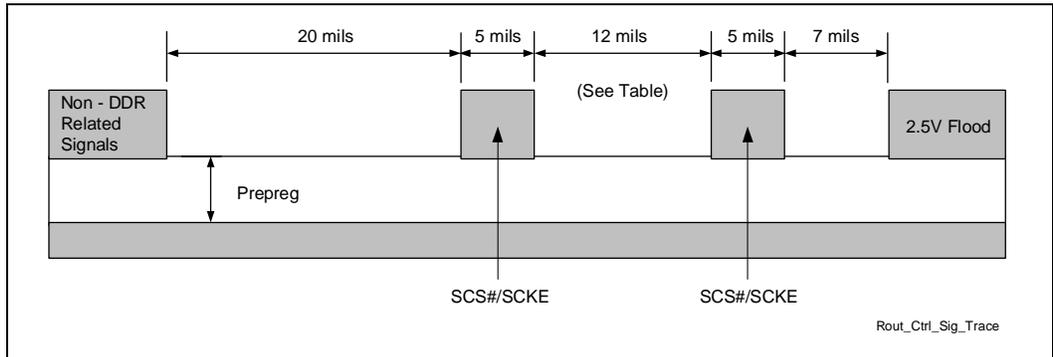


Table 26. Control Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	Control – SCS_[3:0]#, SCKE_[3:0]
Topology	Point to Point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	60 $\Omega \pm 15\%$
Nominal Trace Width	5 mils
Nominal Trace Spacing	<ul style="list-style-type: none"> GMCH to 1st DIMM = 12 mils Within DIMM Pin Field = 7 mils minimum From DIMM to DIMM = 12 mils 2nd DIMM to Rtt = 7 mils minimum
Group Spacing	Isolation spacing from non-DDR related signals = 20 mils
2.5 V Flood Spacing	Isolation from the 2.5 V flood on layer four = 7 mils minimum
GMCH Breakout Guidelines	5 mils width with 6 mil spacing for a max of 350 mils. Note: Use of breakout guidelines should be minimized.
Trace Length A – (SCS#/SCKE_[1:0]) – GMCH Signal Ball to DIMM Pins on 1 st DIMM	Max = 3.5" The trace length from ball to 1st via should be within 50 mils. The trace length from the 2nd via to the 1st DIMM should be within 500 mils.
Trace Length A – (SCS#/SCKE_[3:2]) – GMCH Signal Ball to DIMM Pins on 2 nd DIMM	Max = 4.0" The trace length from ball to 1st via should be within 50 mils. The trace length from the 2nd via to the 2nd DIMM should be within 1".
Trace Length B – (SCS#/SCKE_[1:0]) – DIMM pins on 1 st DIMM to Rtt Pad	Max = 1.4"
Trace Length B – (SCS#/SCKE_[3:2]) – DIMM pins on 2 nd DIMM to Rtt Pad	Max = 800 mils
Termination Resistor (Rtt)	56 $\Omega \pm 5\%$
Maximum via Count per signal	4 vias (The number of vias over 2 should be minimized)
Length Tuning Method	SCS#/SCKE_[3:0] to SCMD_CLK/SCMD_CLK[5:0]# See Section 5.2.2.1

Figure 50. Control Signal Trace Width/Spacing Routing



5.2.2.1 Control Group Signal Length Matching Requirements

Tuning is required from GMCH ball to DIMM pin for control signals, and from GMCH pad to DIMM pin for clock signals. Clock Total Length includes clock package length.

- On a 845G chipset based DDR platform, the total target differential clock length must be at least 3.4" longer than the longest routed control signal length for the associated DIMM.

$$\text{SCMD_CLK/SCMD_CLK\# Total Length} = X$$

$$\text{Associated SCS\#/SCKE Max Length} = Y, \text{ where } Y \leq (X - 3.4")$$

where Max Length = Longest (Motherboard trace length) for each associated DIMM

Length X to 1st and 2nd DIMM include the GMCH Package Length P + Motherboard Trace Length A.

Length Y to 1st and 2nd DIMM includes the Motherboard Trace Length A.

SCS#/SCKE motherboard trace length guideline A is described in Table 26. No length matching is required from the DIMM to the parallel termination resistors. Refer to Section 5.2.7 for GMCH clock package length data.

Figure 51 shows the length matching requirements between the control signals and the clock signals.

Figure 51. Control Signal to SCMDCLK/SCMDCLK# Trace Length Matching Requirements

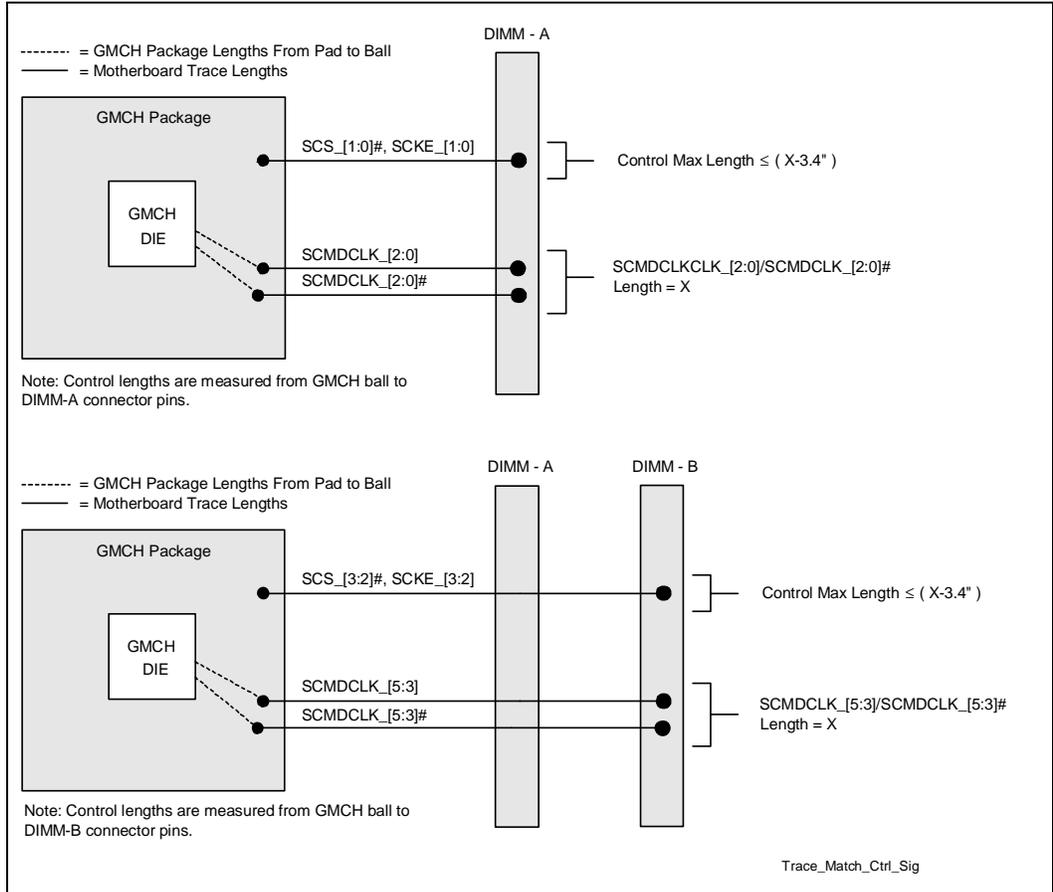




Figure 52. Control Group Bottom Layer to First DIMM Routing Example

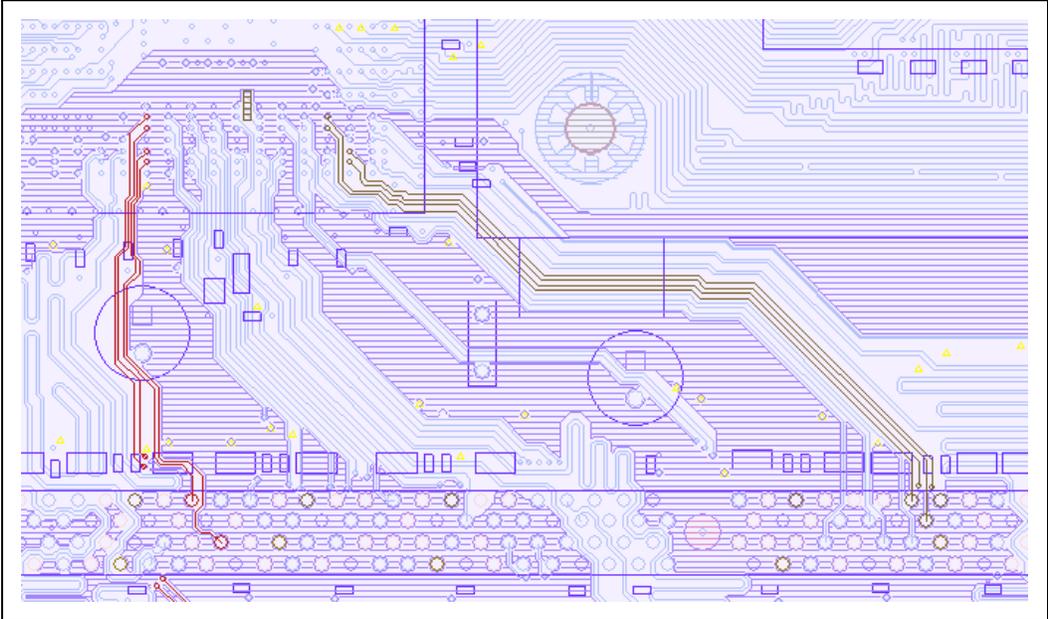


Figure 53. Control Group Bottom Layer Second DIMM Routing Example

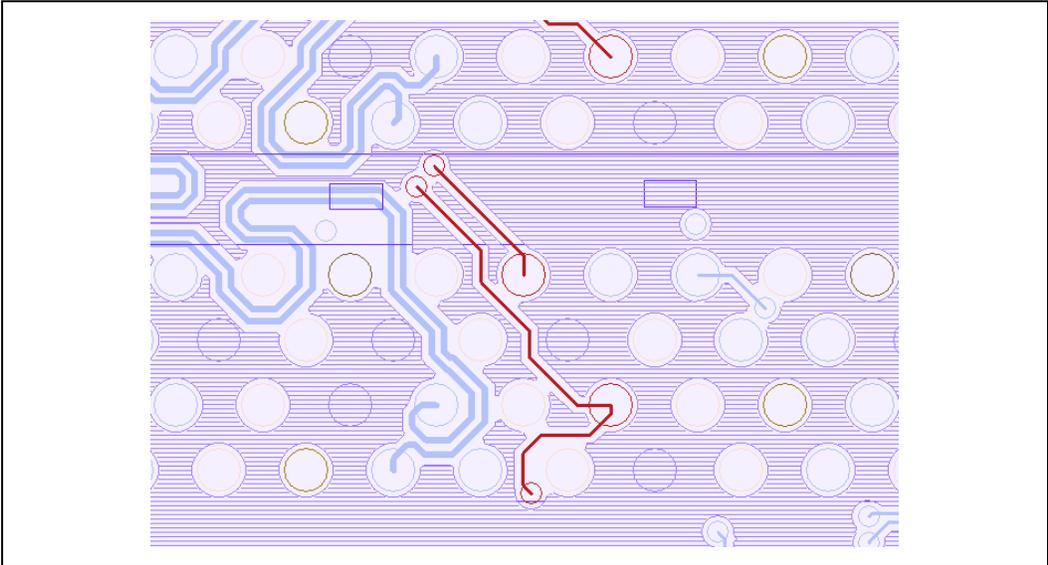
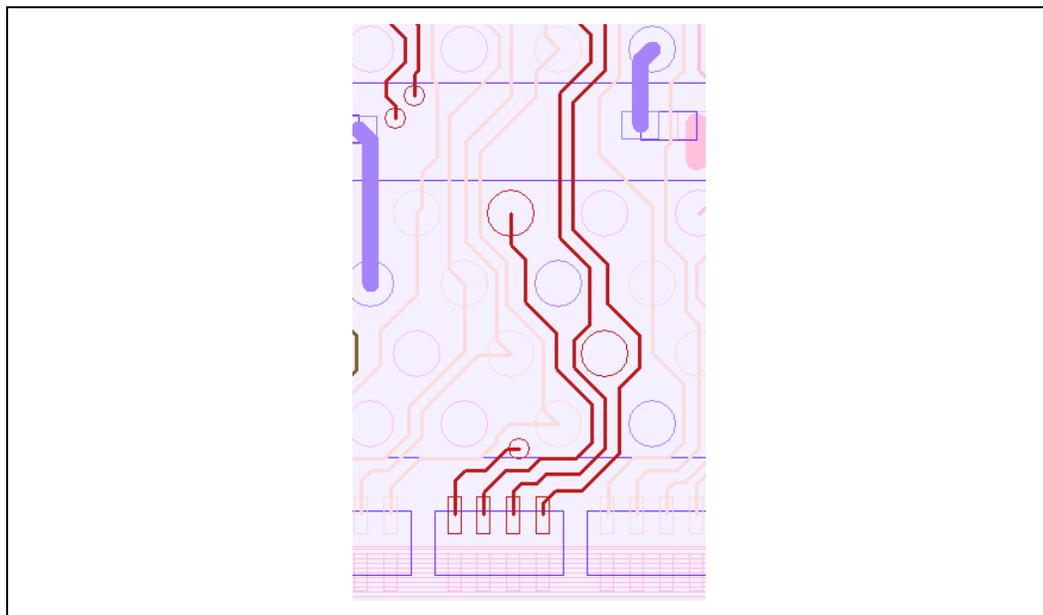


Figure 54. Control Group Top Layer Second DIMM to Termination Routing Example



5.2.3 Address/Command Signals — SMAA_[12:6, 3, 0], SBA_[1:0], SRAS#, SCAS#, SWE#

The GMCH address/command signals are source-clocked signals that include memory address signals SMAA_[12:6, 3, 0], SBA, SRAS#, SCAS#, and SWE#. The address signals (SMAA_[5,4,2,1] /SMAB_[5,4,2,1]) are described in the next section. The address/command signals are tuned to SCMD_CLK.

The GMCH system memory pin out has been optimized to breakout the address/command signals on the **bottom** signal layer, and all address/command signals must be routed on the same layer. They should transition from the top signal layer to the bottom signal layer under the GMCH. They should be routed on the bottom signal layer until the first DIMM, or until they transition to the top signal layer within 500 mils before the first DIMM connector. Finally, they should route from the DIMM connector pins to the parallel termination resistors at the end of the memory channel on the top signal layer.

Because the address/command signals are routed on the bottom signal layer between the GMCH and the first DIMM, 2.5 V flooding on the bottom signal layer is reduced, and the address/command signals should be kept as short as possible. Also, because the address/command signals transition signal layers near the first DIMM, a via connecting the ground flood and ground plane on layer two and three should be placed as close as possible to each control signal transition via.

Resistor packs are acceptable for the parallel (R_{tt}) address/command termination resistors, but address/command signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, control, or CPC address signals. Termination resistor packs for the address/command group must remain dedicated to address/command group signals, and cannot be used for any other signal groups.

The following figures and table describe the recommended topology and layout routing guidelines for the DDR-SDRAM address/command signals.

Figure 55. Address/Command Signal Routing Topology

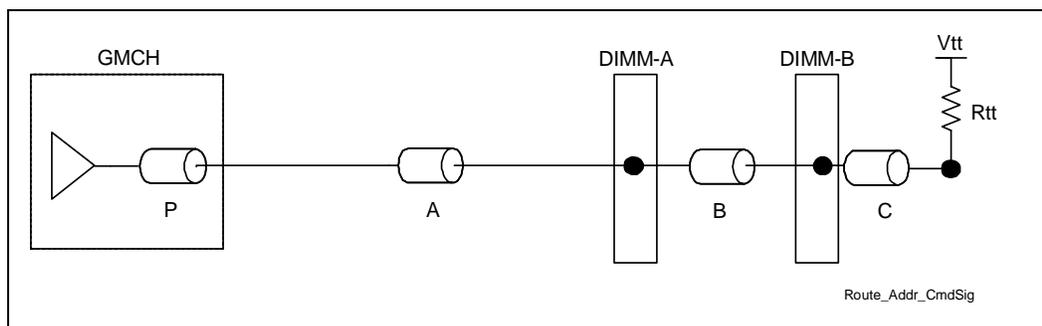
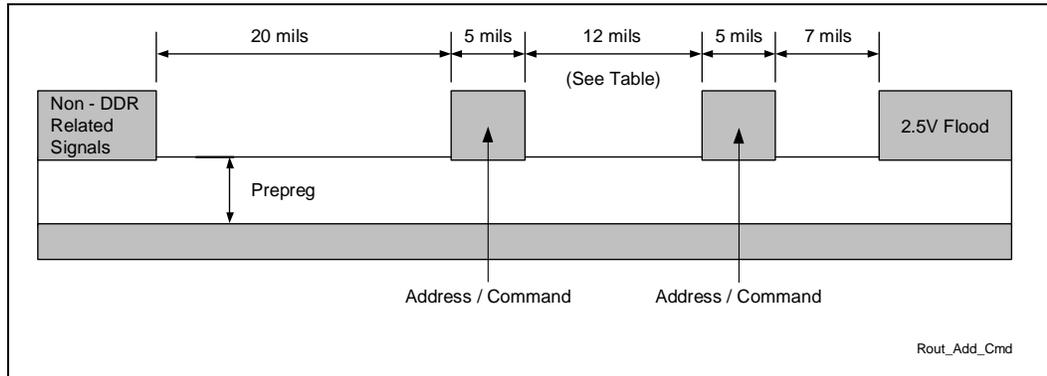


Table 27. Address/Command Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	Address/command – SMAA_[12:6, 3, 0], SBA_[1:0], SRAS#, SCAS#, SWE#
Topology	Daisy Chain
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_0)	$60 \Omega \pm 15\%$
Nominal Trace Width	5 mils
Nominal Trace Spacing from GMCH	<ul style="list-style-type: none"> • GMCH to 1st DIMM = 12 mils • Within DIMM Pin Field = 7 mils minimum • From DIMM to DIMM = 12 mils • 2nd DIMM to Rtt = 7 mils minimum
Group Spacing	Isolation spacing from non-DDR related signals = 20 mils
2.5 V Flood Spacing	Isolation from the 2.5 V flood on layer four = 7 mils minimum
GMCH Breakout Guidelines	5 mils width with 6 mil spacing for a max of 350 mils. Note: Use of breakout guidelines should be minimized.
Trace Length A – GMCH Signal Ball to 1st DIMM Pin	Max = 4.0" The trace length from ball to 1st via should be within 50 mils.
Trace Length B – DIMM Pin to DIMM Pin	Min = 400 mils Max = 600 mils
Trace Length C – Last DIMM Pin to Parallel Termination Resistor Pad	Max = 800 mils
Termination Resistor (Rtt)	$56\Omega \pm 5\%$
Maximum via Count per signal	4 vias (The number of vias over 2 should be minimized.)
Length Tuning Method	SMAA_[12:6,3,0], SBA_[1:0], SRAS#, SCAS#, SWE# to SCMD_CLK/ SCMD_CLK [5:0]# per DIMM See Section 5.2.3.1

Figure 56. Address/Command Signal Trace Width/Spacing Routing



5.2.3.1 Address/Command Group Signal Length Matching Requirements

SMAA_[12:6,3,0], SBA_[1:0], SRAS#, SCAS#, SWE# require tuning to differential clock signals from GMCH ball to DIMM pin for address/command signals, and from GMCH pad to DIMM pin for clock signals. Clock Total Length includes clock package length.

On an 845G chipset based DDR platform, the longest routed address/command signals must shorter than the total target differential clock for the associated DIMM by at least 1.9".

$$\text{SCMD_CLK/SCMD_CLK\# Total Length} = X$$

$$\text{Associated Address/Command Max Length} = Y, \text{ where } Y \leq (X - 1.9")$$

where Max Length = Longest (Motherboard trace length) for each associated DIMM

Length X to 1st and 2nd DIMM include the GMCH Package Length P + Motherboard Trace Length A.

Length Y to 1st DIMM includes the Motherboard Trace Length A.

Length Y to 2nd DIMM include the Motherboard Trace Lengths A + B.

Address/command motherboard trace length guidelines A and B are described in Table 27. No length matching is required from the DIMM to the parallel termination resistors. Refer to Section 5.2.7 for GMCH clock package length data.

Figure 57 shows the length matching requirements between the address/command signals and the clock signals.

Figure 57. Address/Command Signal to SCMD_CLK/SCMD_CLK# Trace Length Matching Requirements

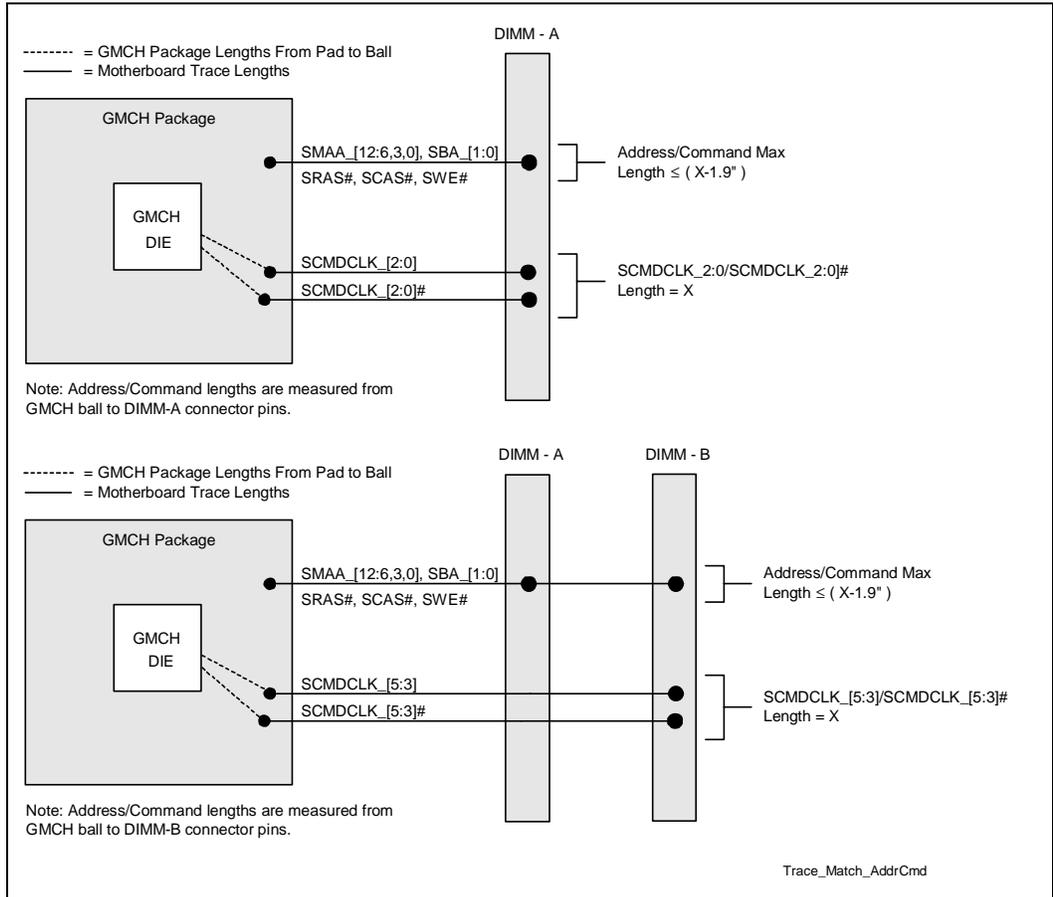




Figure 58. Address/Command Group Bottom Layer to First DIMM Routing Example

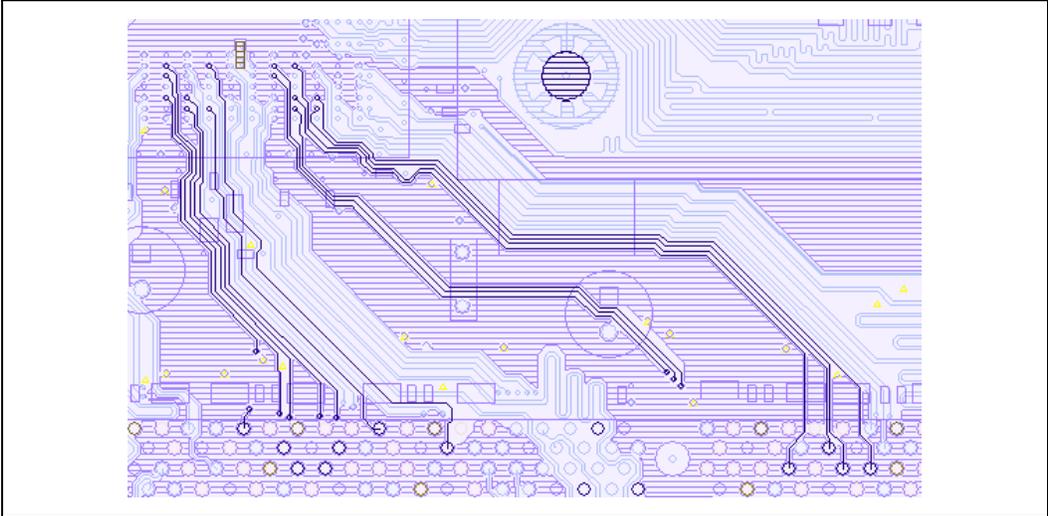
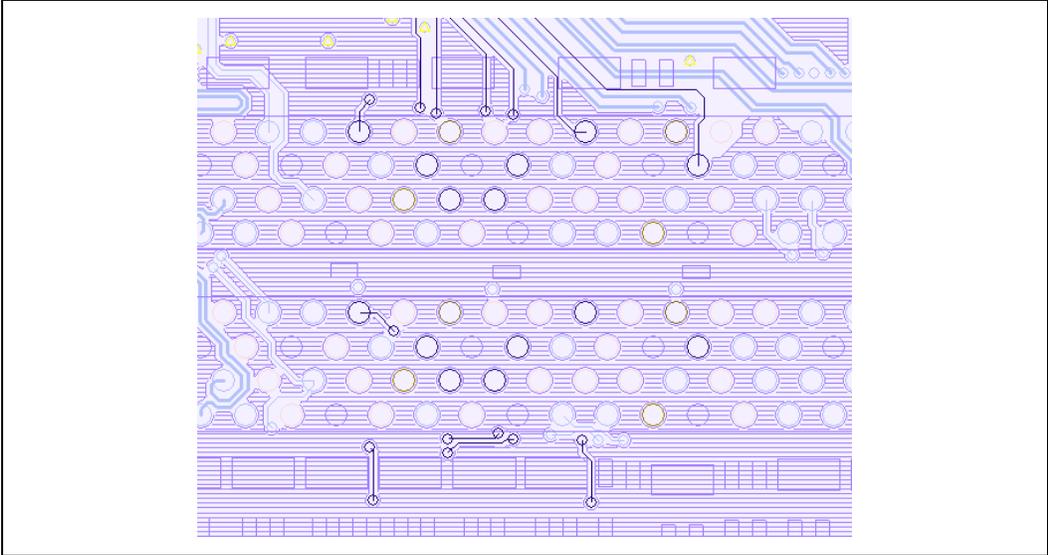


Figure 59. Address/Command Group Bottom Layer Routing Example



5.2.4 CPC Address Signals — SMAA_[5,4,2,1] and SMAB_[5,4,2,1]

The GMCH CPC address signals are source-clocked signals that include SMAA_[5,4,2,1] and SMAB_[5,4,2,1].

It is recommended to route CPC address signals before routing the differential clock signals. For more information, see the beginning of Section 5.2. The CPC address signals should be kept as short as possible, and must be tuned to SCMD_CLK.

The GMCH system memory pin out has been optimized to breakout the CPC address signals on the **bottom** signal layer, and all CPC address signals must be routed on the same layer. Table 28 lists the correct SMAA_[5,4,2,1]/SMAB_[5,4,2,1] signal to DIMM mapping.

Table 28. CPC Address to DIMM Mapping

SMAA/SMAB	DIMM
SMAA_[5,4,2,1]	DIMM-A
SMAB_[5,4,2,1]	DIMM-B

Because CPC address signals are routed on the bottom signal layer, they should be kept as short as possible. A via connecting the ground flood and ground plane on layers two and three should be placed as close as possible to each control signal transition via.

Resistor packs are acceptable for the parallel (R_{tt}) CPC address termination resistors, but CPC address signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, control, or address/command signals. Termination resistor packs for the CPC address group must remain dedicated to CPC address group signals, and cannot be used for other signal groups.

The following figures and table describe the recommended topology and layout routing guidelines for the DDR-SDRAM CPC address signals.

Figure 60. DIMM-A CPC Address Signal Routing Topology

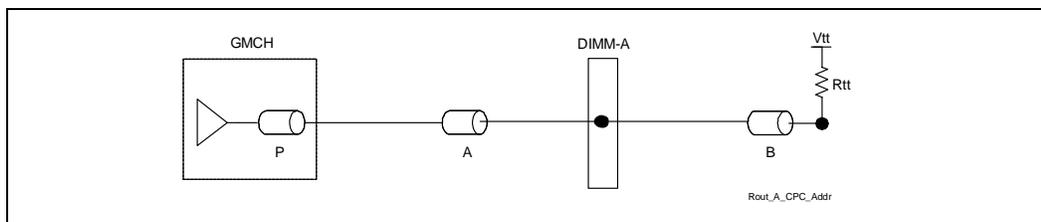




Figure 61. DIMM-B CPC Address Signal Routing Topology

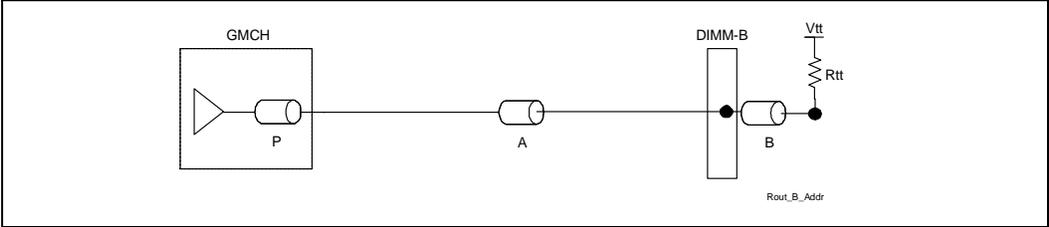
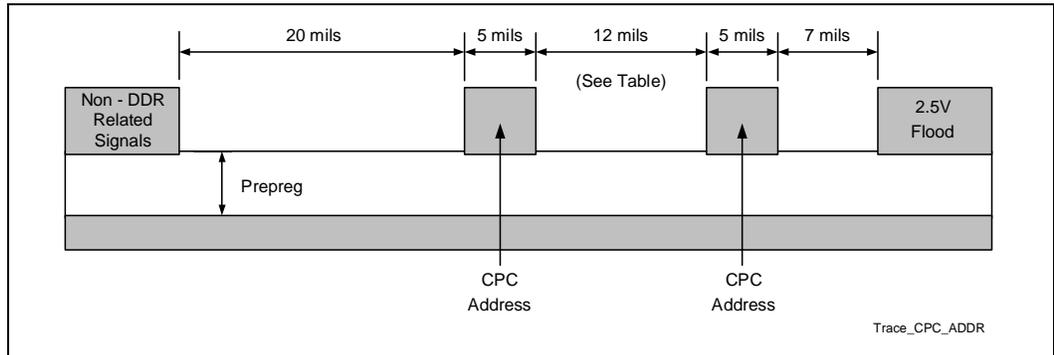


Table 29. CPC Address Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	CPC Address – SMAA_[5,4,2,1] and SMAB_[5,4,2,1]
Topology	Point to Point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Nominal Trace Width	5 mils
Nominal Trace Spacing	<ul style="list-style-type: none"> • GMCH to DIMM = 12 mils • Within DIMM Pin Field = 8 mils minimum • DIMM to Rtt = 8 mils minimum
Group Spacing	<p>Isolation spacing from non-DDR related signals = 20 mils</p> <p>A maximum of 1 address/command signal can be routed adjacent to a CPC Address signal.</p>
2.5 V Flood Spacing	Isolation from the 2.5 V flood on layer four = 7 mils minimum
GMCH Breakout Guidelines	<p>5 mil width on 6 mil spacing up to the first 200 mils from ball.</p> <p>5 mil width on 8 mil spacing up to an additional 550 mils after the first 200 mils from ball.</p> <p>Note: Use of breakout guidelines should be minimized.</p>
Trace Lengths A – (SMAA_[5,4,2,1]) – GMCH Signal Ball to 1st DIMM	<p>Max = 2.5"</p> <p>The trace length from ball to 1st via should be within 50 mils.</p>
Trace Lengths A – (SMAB_[5,4,2,1]) – GMCH Signal Ball to 2nd DIMM	<p>Max = 3.0"</p> <p>The trace length from ball to 1st via should be within 50 mils.</p>
Trace Length B – (SMAA_[5,4,2,1]) – 1st DIMM Pin to Parallel Termination Resistor Pad	Max = 1.4"
Trace Length B – (SMAB_[5,4,2,1]) – 2nd DIMM Pin to Parallel Termination Resistor Pad	Max = 800 mils
Termination Resistor (Rtt)	33Ω ± 5%
Maximum via Count per signal	4 vias (The number of vias over 2 should be minimized)
Length Tuning Method	<p>SMAA_[5,4,2,1], SMAB_[5,4,2,1] to SCMDCLK/SCMDCLK_[5:0]# for corresponding DIMM</p> <p>See Section 5.2.4.1 for details</p>

Figure 62. CPC Address Signal Trace Width/Spacing Routing



5.2.4.1 CPC Address Group Signal Length Matching Requirements

Tuning is required from GMCH ball to DIMM pin for CPC address signals, and from GMCH pad to DIMM pin for clock signals. Clock Total Length includes clock package length.

- The total target differential clock must be at least 4.4" longer than the longest routed CPC address signal SMAA_[5,4,2,1] and SMAB_[5,4,2,1] for the associated DIMM.

SCMDCLK/SCMDCLK# Total Length = X

Associated CPC address Max Length = Y, where $Y \leq (X - 4.4")$

where Max Length = Longest (Motherboard trace length) for each associated DIMM*

Length X to 1st and 2nd DIMM include the GMCH Package Length P + Motherboard Trace Length A.

Length Y to 1st and 2nd DIMM includes the Motherboard Trace Length A.

SMAA_[5,4,2,1] and SMAB_[5,4,2,1] motherboard trace length guidelines A are listed in Table 29. No length matching is required from the DIMM to the parallel termination resistors. Refer to Section 5.2.7 for GMCH clock package length data.

Note: It is recommended to route CPC address before routing the clocks. This tuning is applied to the longest 1st-DIMM signal, and is also applied to the longest 2nd-DIMM signal.

Figure 63 shows the length matching requirements between the CPC address signals, and the clock signals.

Figure 63. CPC Address Signal to SCMD_CLK/SCMD_CLK# Trace Length Matching Requirements

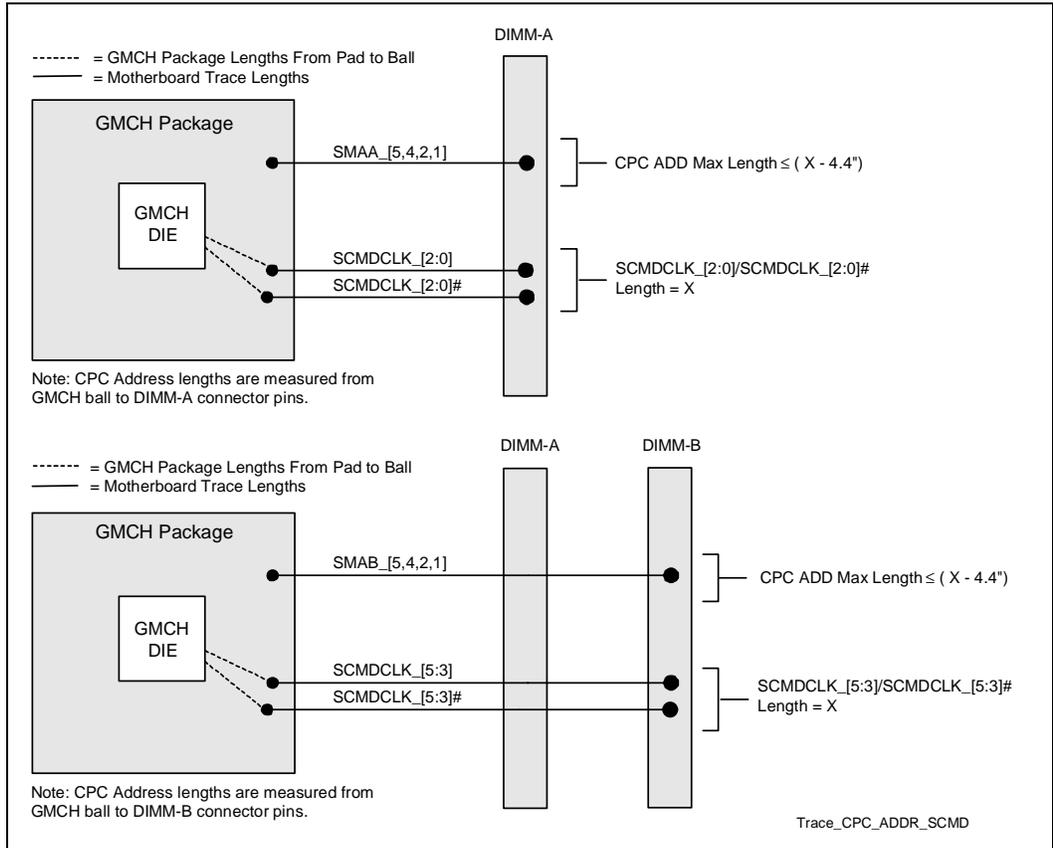




Figure 64. CPC Address Group Bottom Layer to First DIMM Routing Example

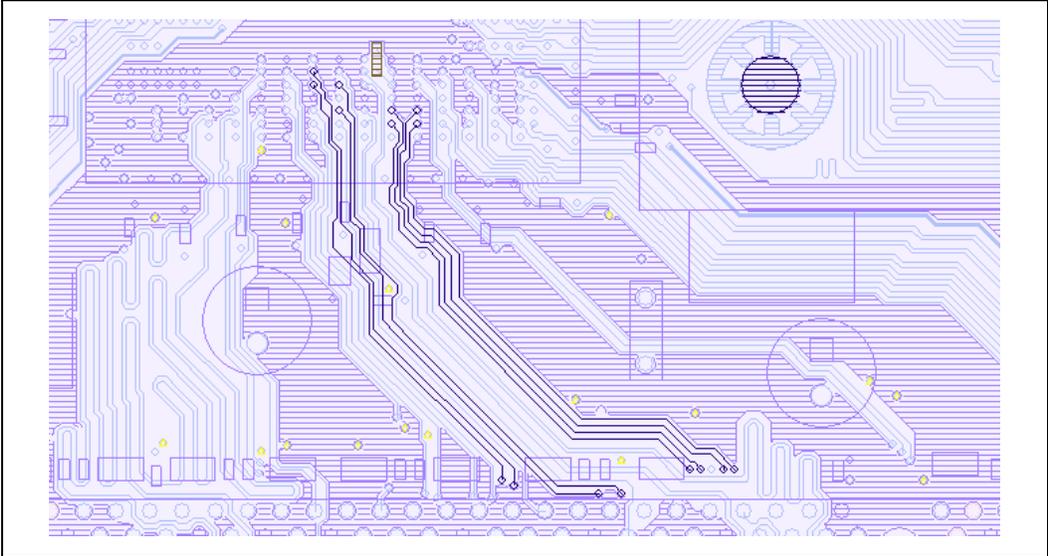
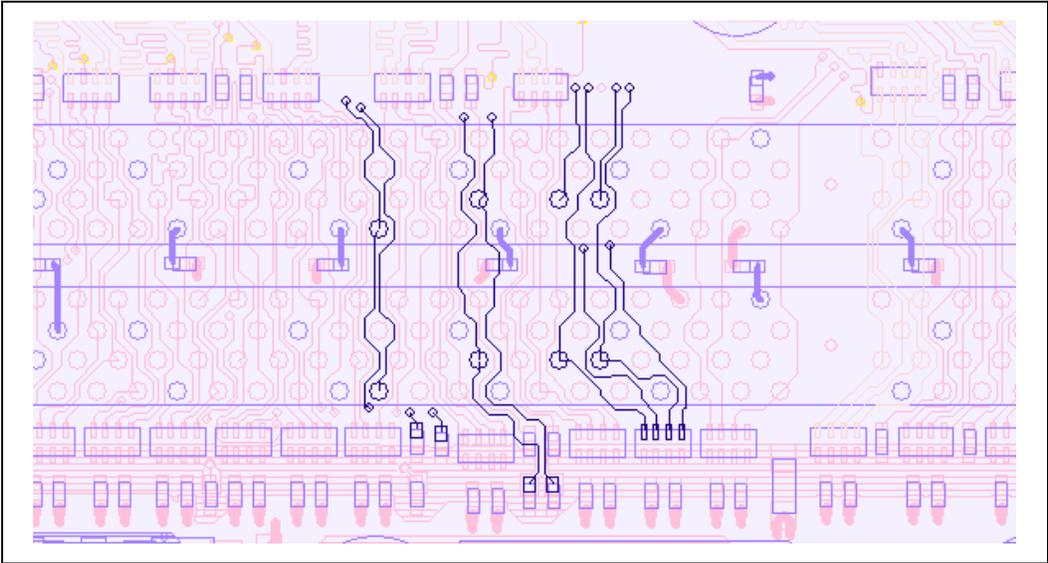


Figure 65. CPC Address Group Top Layer DIMM to Termination Routing Example



5.2.5 Clock Signals — SCMDCLK_[5:0], SCMDCLK_[5:0]#

The GMCH clock signals include 6 differential clock pairs SCMDCLK_[5:0] and SCMDCLK_[5:0]#. The GMCH generates and drives these differential clock signals required by the DDR interface. Therefore, no external clock driver is required for the DDR interface. Because the GMCH only supports unbuffered DDR DIMMs, three differential clock pairs are routed to each DIMM connector.

Before routing the clocks, refer to the beginning of Section 5.2 for the recommended routing order. This will help determine your target total clock length. Table 30 summarizes the clock signal mapping.

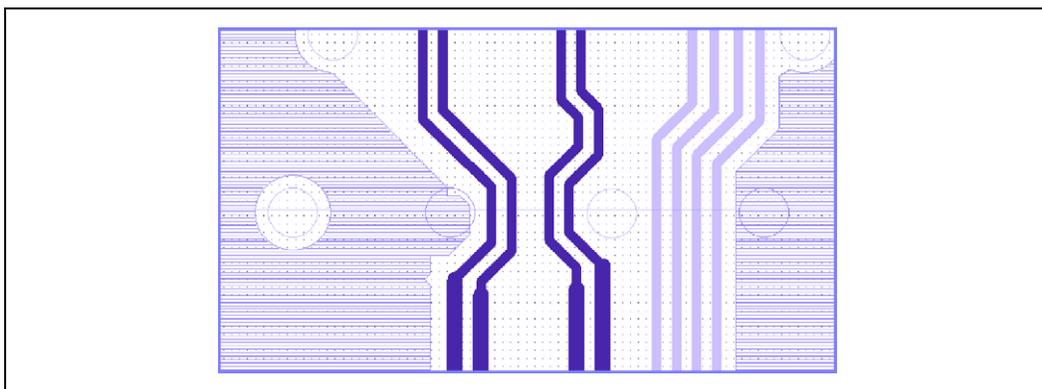
Table 30. Clock Signal DIMM Mapping

Signal	Relative To
SCMDCLK_[2:0], SCMDCLK_[2:0]#	DIMMA
SCMDCLK_[5:3], SCMDCLK_[5:3]#	DIMMB

All differential clock signals **must** be routed on the same layer. The GMCH system memory pinout has been optimized to breakout the clock signals on the **bottom** signal layer. The clock signals should transition from the top signal layer to the bottom signal layer under the GMCH, and be route referenced to ground on the bottom signal layer for the entire length to their associated DIMM pins.

DDR clocks can breakout of the GMCH with a reduced width for a maximum of 350 mil length, but use should be minimized where possible. Figure 66 shows an example of clock neck down in the GMCH region.

Figure 66. Clock Breakout Neck Down Example



The differential clock pairs must be routed differentially from the GMCH to their associated DIMM pins. They must maintain correct spacing of 5 mils **between** themselves to remain differential. In addition, they must maintain an isolation spacing of 20 mils **away** from other signals and themselves (in serpentines). See Figure 67.

Figure 67. Differential Clock Spacing Example

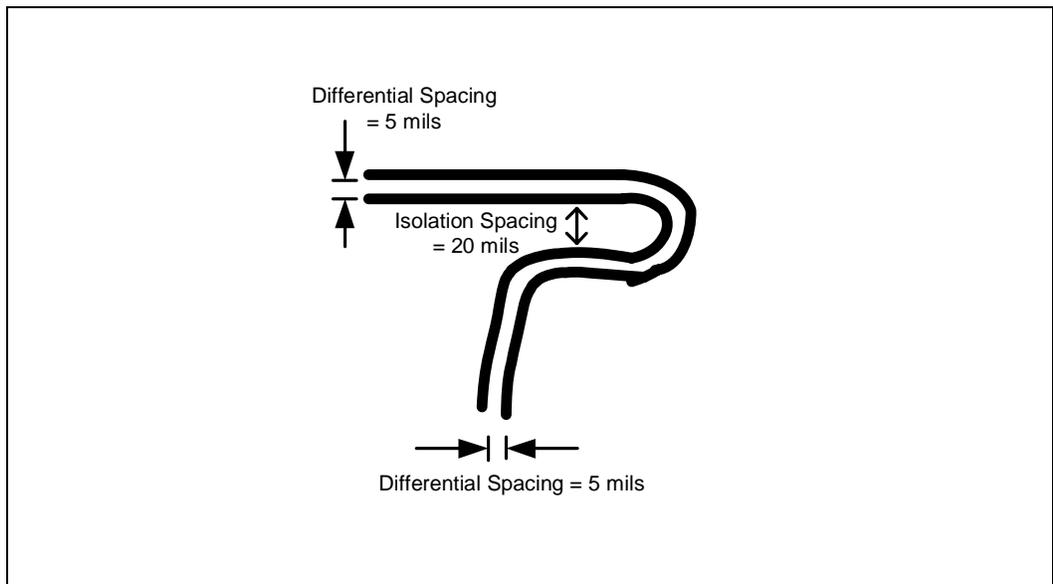


Table 31 summarizes a clock-signal-to-DIMM-pin mapping.

Table 31. DDR Clock Signal DIMM Pin Mapping

Signal	Relative To	DIMM Pin
SCMDCLK_0	DIMMA	137
SCMDCLK_0#	DIMMA	138
SCMDCLK_1	DIMMA	16
SCMDCLK_1#	DIMMA	17
SCMDCLK_2	DIMMA	76
SCMDCLK_2#	DIMMA	75
SCMDCLK_3	DIMMB	137
SCMDCLK_3#	DIMMB	138
SCMDCLK_4	DIMMB	16
SCMDCLK_4#	DIMMB	17
SCMDCLK_5	DIMMB	76
SCMDCLK_5#	DIMMB	75

System memory signal lengths must be tuned to the total target length of the clock pairs SCMDCLK/SCMDCLK#. Refer to the individual group signal length matching requirements found in the corresponding chapter section for each system memory group. In addition, SCMDCLK must be tuned to SCMDCLK#.

Special attention must be paid to how the clock signals would affect the 2.5 V flood to any of the 2.5 V DIMM pins because the clock signals are routed on the bottom signal. This is especially important in the area where the clocks must serpentine in or near the DIMM connector area. For an example of the clock routing on the bottom signal layer, see Figure 71 and Figure 72 (DDR Clock Bottom Signal Layer Routing Example 1 and 2).

There are no external termination resistors needed for SCMDCLK#/SCMDCLK. The following figures and table describe the recommended topology and layout routing guidelines for the DDR-SDRAM differential clocks.

Figure 68. DDR Clock Routing Topology (SCMDCLK/SCMDCLK_[2:0]#)

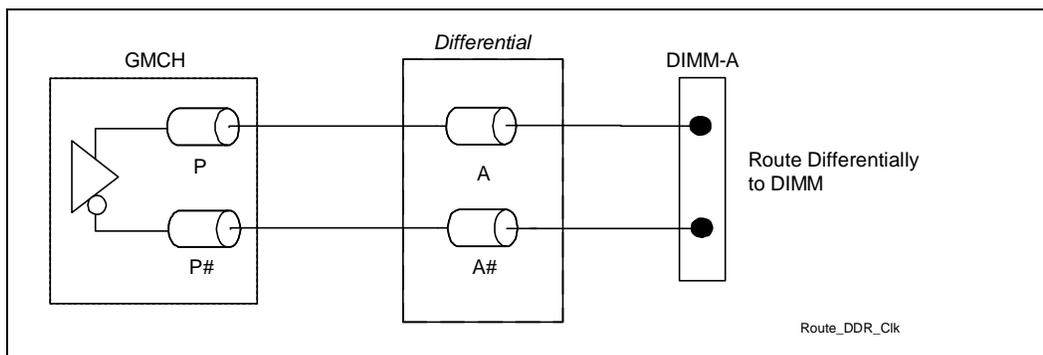


Figure 69. DDR Clock Routing Topology (SCMDCLK/SCMDCLK_[5:3]#)

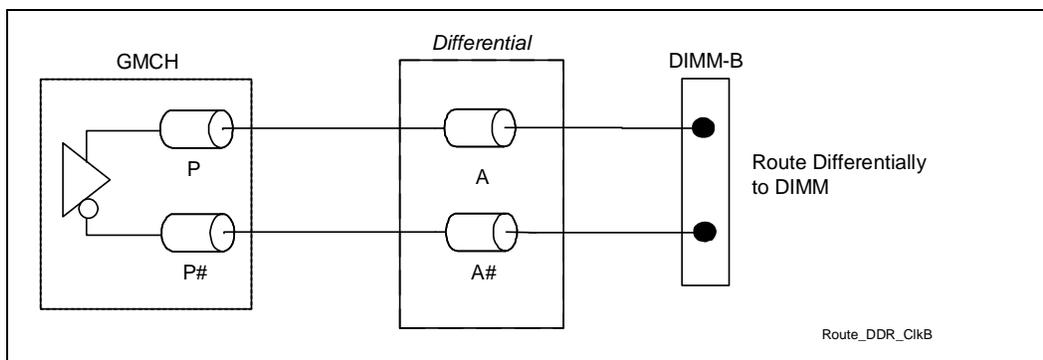


Table 32. Clock Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	Clocks – SCMDCLK_[5:0], SCMDCLK_[5:0]#
Topology	Point to Point
Reference Plane	Ground Referenced
Nominal Characteristic Trace Impedance (Zo)	Differential (odd-mode) = 70 Ω
Nominal Trace Width	8 mils
Differential Trace Spacing - spacing between SCMDCLK and its SCMDCLK#	5 mils
Group Spacing	Isolation spacing from another DDR signal group = 20 mils Isolation spacing from non-DDR related signals = 20 mils
Serpentine Spacing	Isolation spacing from itself when serpentine = 20 mils
2.5 V Flood Spacing	Isolation from the 2.5 V flood on layer four = 10 mils minimum
GMCH Breakout Guidelines	5 mil width with 5 mil differential spacing with a minimum of 5 mil isolation from any other signals for a max length of 350 mils Note: Use of breakout guidelines should be minimized.
Total Trace Length P + A - SCMDCLK_[2:0] - GMCH Signal Pad to 1st DIMM	Max = 7.4" The trace length from ball to via should be within 50 mils. See Section 5.2.7 for package length P.
Total Trace Length P + A - SCMDCLK_[5:3] - GMCH Signal Pad to 2 nd DIMM	Max = 7.9" The trace length from ball to via should be within 50 mils. See Section 5.2.7 for package length P.
Total Clock Length Relationship - between 1st DIMM and 2nd DIMM	$(P + Y) = ((P + X) + 0.5")$ where (P+X) = Total target clock length to 1st DIMM where (P+Y) = Total target clock length to 2nd DIMM
Maximum via Count per signal	1 via (for breakout to bottom layer)
Length Tuning Method	<ul style="list-style-type: none"> SCMD_CLK length to SCMD_CLK# length, within ± 10 mils All 3 clock pairs to each DIMM are equal in length, within ± 10 mils where length includes package length compensation (P + A) See Section 5.2.5.1 for details

Figure 70. Clock Signal Trace Width/Spacing Routing

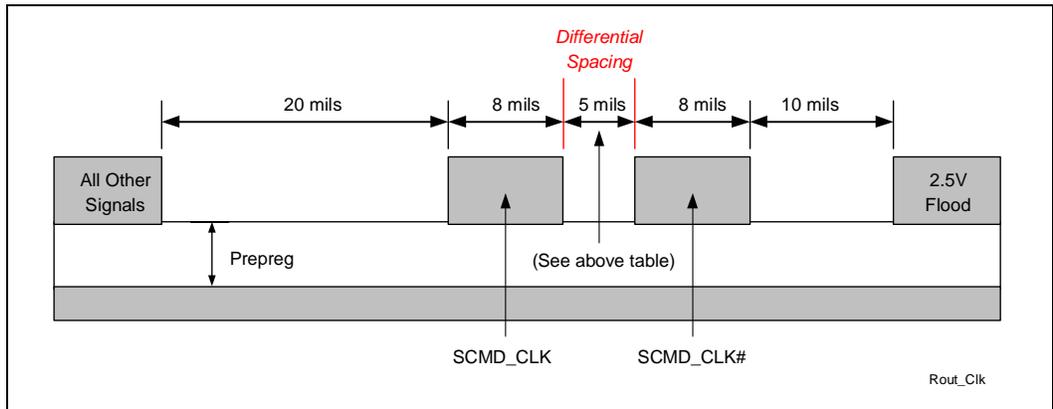


Figure 71. DDR Clock Bottom Signal Layer Routing Example 1

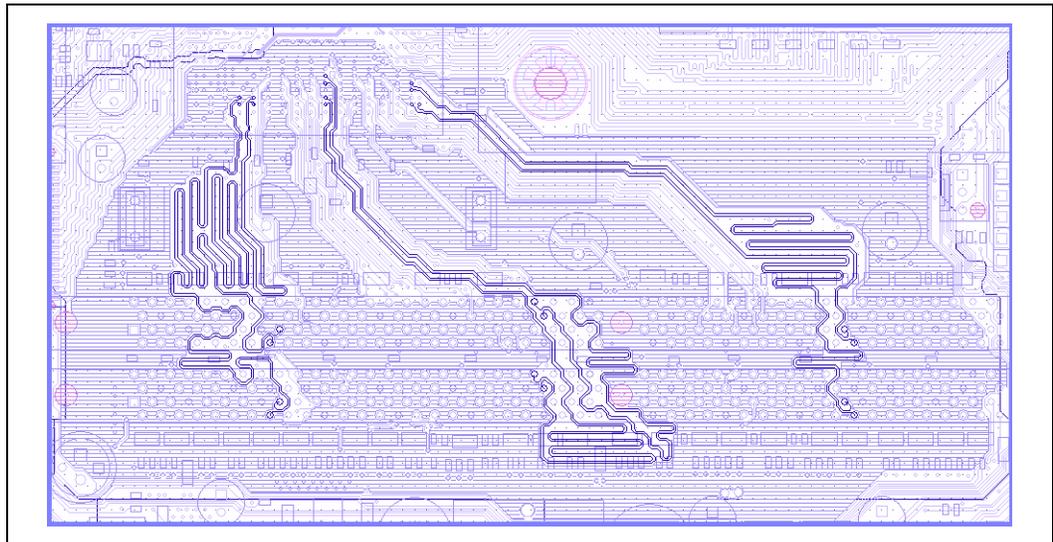




Figure 72. DDR Clock Bottom Signal Layer Routing Example 2

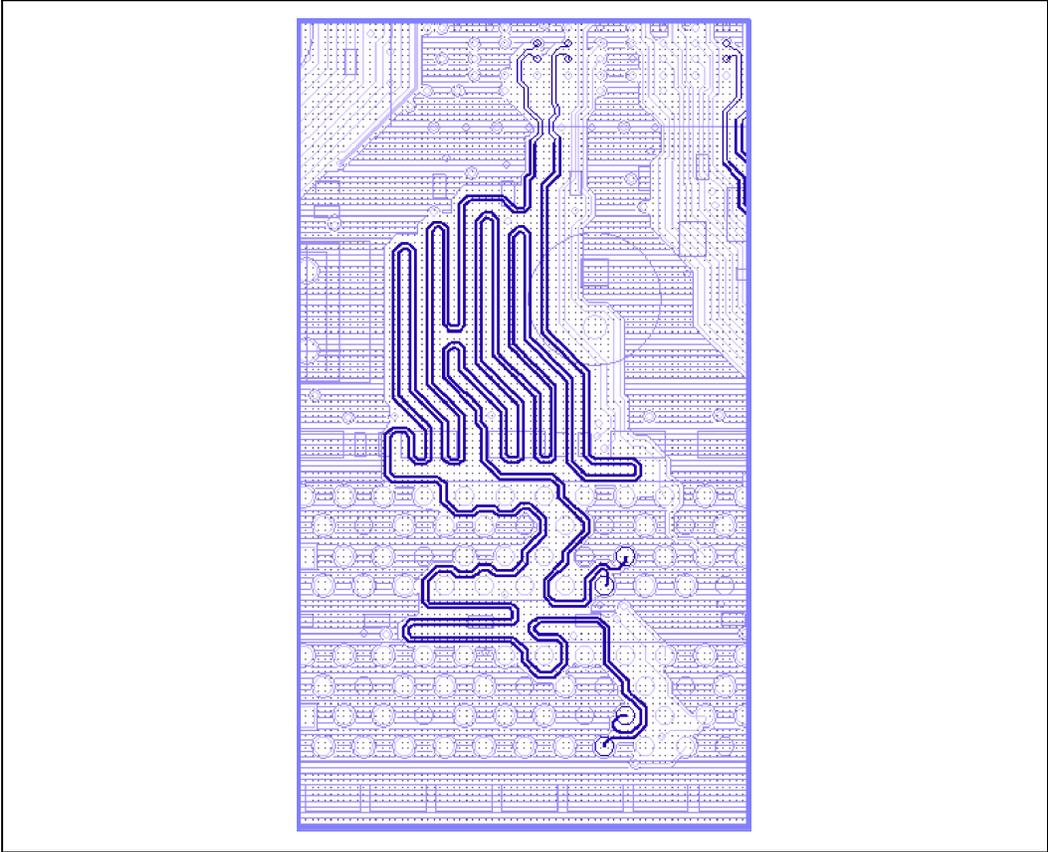


Figure 73. DDR Clock Bottom Signal Layer Routing Example 3

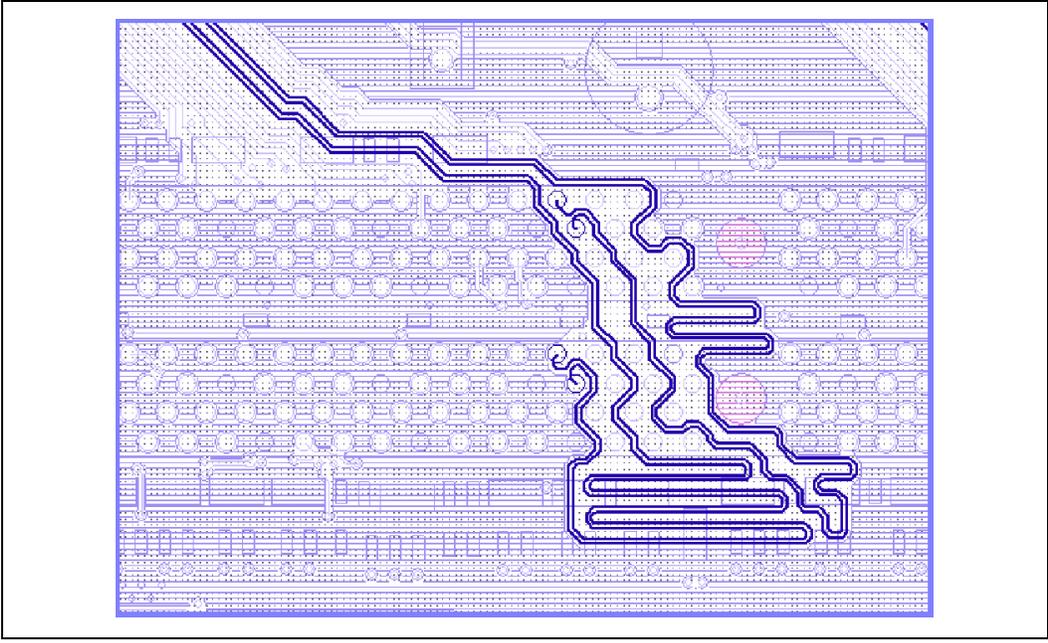
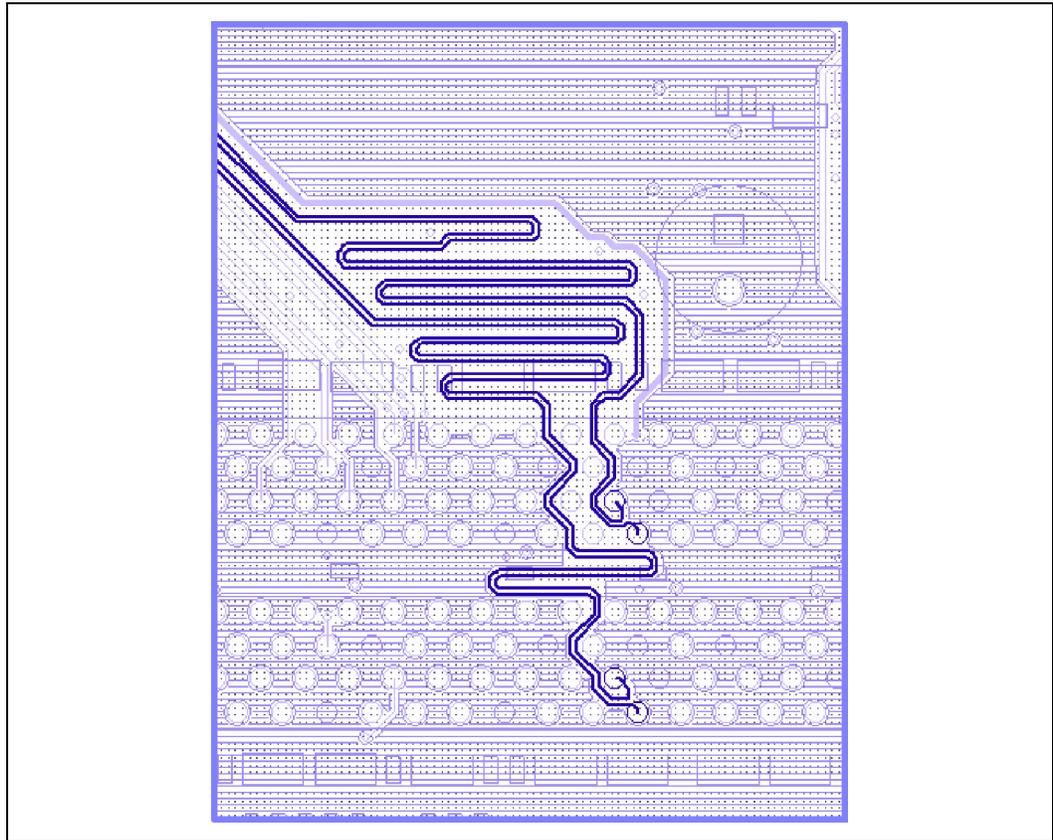


Figure 74. DDR Clock Bottom Signal Layer Routing Example 4


5.2.5.1 Clock Group Signal Length Matching Requirements

Clock length matching is required for every clock and its complement, and between clock pairs associated to the same DIMM. See Figure 75.

- Every SCMDCLK must be length matched to its complement SCMDCLK# from GMCH pad to the pins of the DIMM connector. ($P + A = P\# + A\#$).
- All clock pairs to the 1st DIMM (SCMDCLK_[2:0]/SCMDCLK_[2:0]#) are matched to each other from GMCH internal pad to the pin of the 1st DIMM connector.
- All clock pairs to the 2nd DIMM (SCMDCLK_[5:3]/SCMDCLK_[5:3]#) are matched to each other from the GMCH internal pad to the pin of the 2nd DIMM connector.
- The total target clock length to 2nd DIMM is 0.5" longer than the total target clock length to 1st DIMM.

**Table 33. Clock Group Signal Length Matching Requirements**

First DIMM:	Second DIMM:
SCMDCLK_0 = SCMDCLK_0# = SCMDCLK_1 = SCMDCLK_1# = SCMDCLK_2 = SCMDCLK_2#	SCMDCLK_3 = SCMDCLK_3# = SCMDCLK_4 = SCMDCLK_4# = SCMDCLK_5 = SCMDCLK_5#

Length SCMDCLK to 1st and 2nd DIMM include the GMCH Package Length P + Motherboard Trace Length A.

Length SCMDCLK# to 1st and 2nd DIMM include the GMCH Package Length P# + Motherboard Trace Length A#.

SCMDCLK and SCMDCLK# GMCH internal package trace lengths can be found in Section 5.2.7.

Clock pairs can be matched within ± 10 mils, and associated DIMM clocks can be matched within ± 10 mils.

Note that the total target differential clock lengths must also be tuned with the data strobes, address/command, CPC address, and control signals lengths. For more information, see their corresponding length matching chapter sections. Figure 75 shows the length matching requirements for the differential clock signals.

Figure 75. SCMDCLK_x to SCMDCLK_x# Trace Length Matching Requirements

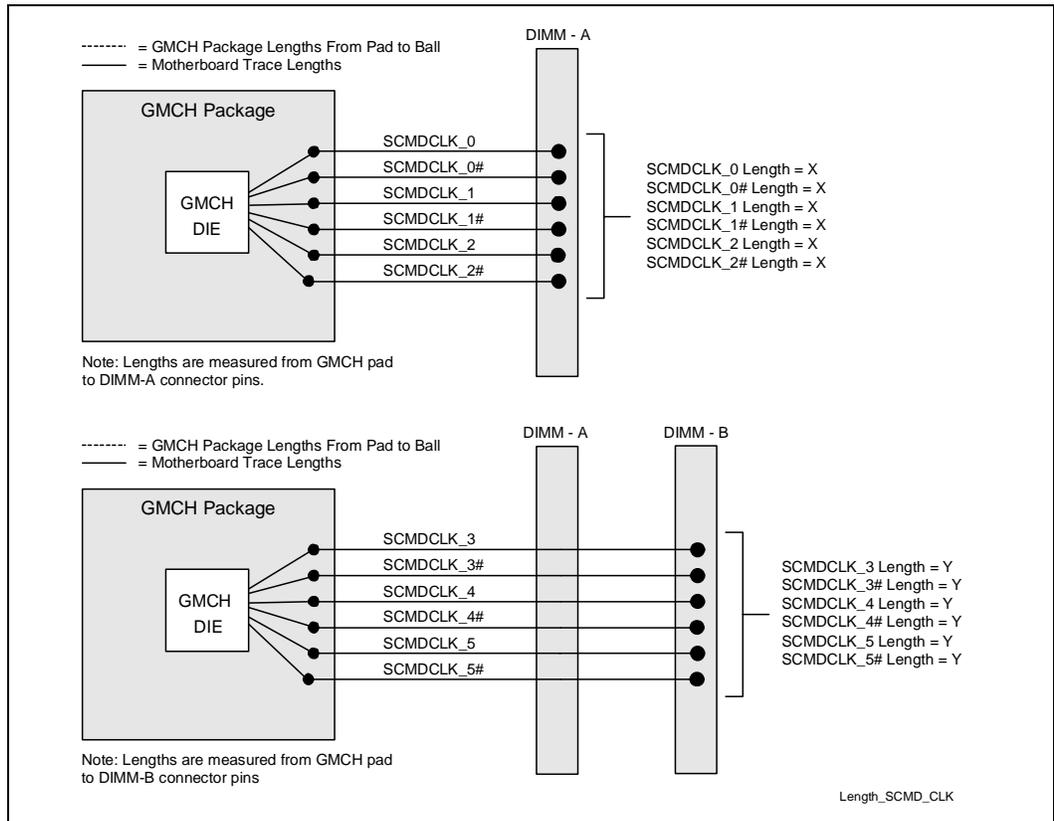
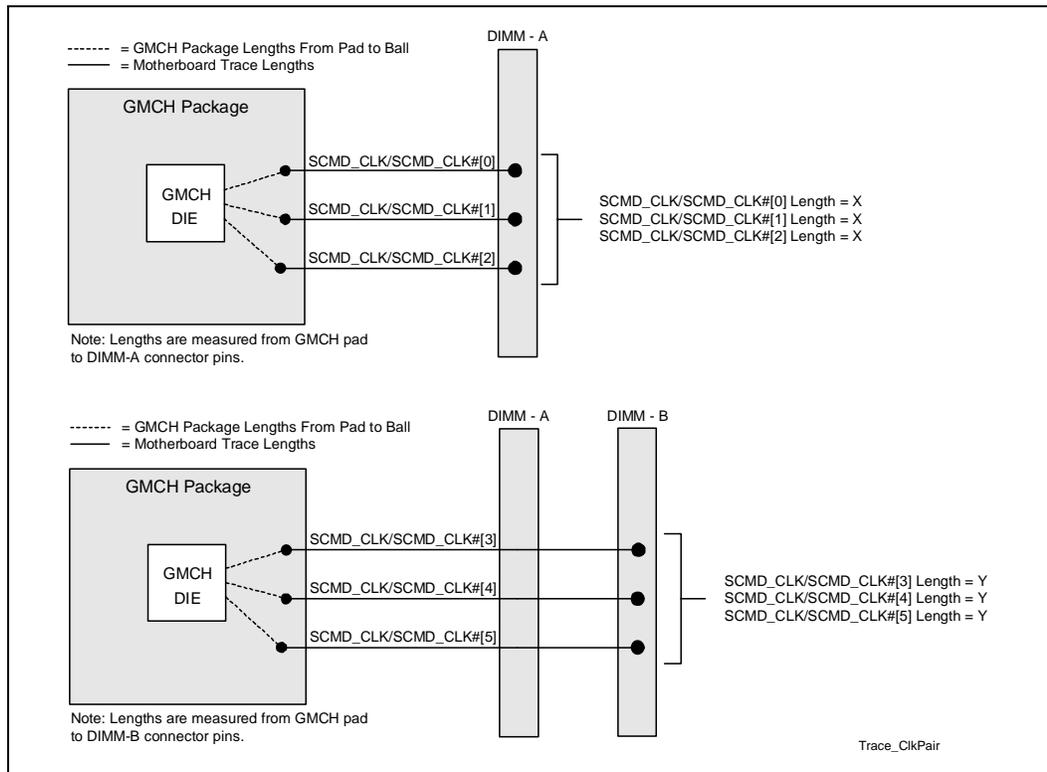


Figure 76. Clock Pair Trace Length Matching Requirements



5.2.6 Feedback – SRCVEN_OUT#, SRCVEN_IN#

On the 845G chipset platform, two signals on the GMCH facilitate testing of “receive enable”. A very short trace on the motherboard to each end of the resistor site can be routed from each of the two balls. The resistor site can be located on the bottom side, routed directly from layer one to layer four through 2 vias.

The implementation of the receive enable resistor site is optional. If a resistor site is implemented, the resistor site must not be populated connecting SRCVEN_OUT# to SRCVEN_IN#. The resistor site should be left unpopulated.

The following figures and table describe the recommended topology and layout routing guidelines for the DDR-SDRAM feedback signal.

Figure 77. DDR Feedback (SRCVEN_OUT# / SRCVEN_IN#) Routing Topology

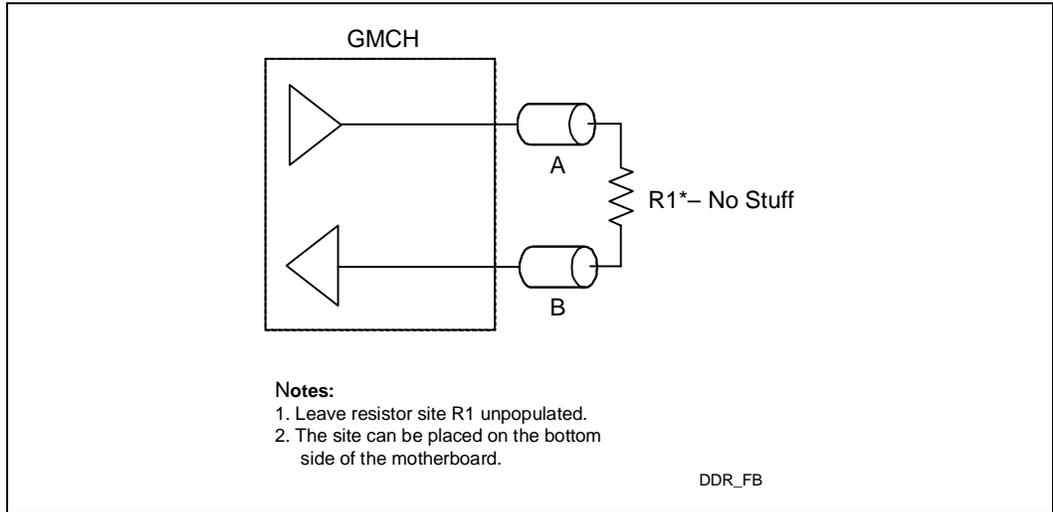


Table 34. Feedback SRCVEN_OUT# and SRCVEN_IN#

Parameter	Routing Guidelines
Signal Group	Feedback – SRCVEN_OUT# and SRCVEN_IN#
Topology	Point to Point, w/ resistor site
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Nominal Trace Width	5 mils
Group Spacing	Isolation from another DDR signal group = 10 mils minimum Isolation from non-DDR related signal = 10 mils minimum
Trace Length Limits – A	Max = 100 mils
Trace Length Limits – B	Max = 100 mils
Maximum via Count per signal	2
Resistor - R1	Not populated

5.2.7 Intel® GMCH DDR Signal Package Lengths

Signal	Intel® GMCH Ball	Package Length (Inches)	Signal	Intel® GMCH Ball	Package Length (Inches)
Data Signals					
SDQ_0	AN4	0.652	SDQ_32	AR22	0.575
SDQ_1	AP2	0.758	SDQ_33	AP22	0.578
SDQ_2	AT3	0.802	SDQ_34	AP24	0.508
SDQ_3	AP5	0.680	SDQ_35	AT26	0.614
SDQ_4	AN2	0.754	SDQ_36	AT22	0.638
SDQ_5	AP3	0.747	SDQ_37	AT23	0.616
SDQ_6	AR4	0.710	SDQ_38	AT25	0.619
SDQ_7	AT4	0.815	SDQ_39	AR26	0.638
SDQ_8	AT5	0.728	SDQ_40	AP26	0.621
SDQ_9	AR6	0.665	SDQ_41	AT28	0.657
SDQ_10	AT9	0.650	SDQ_42	AR30	0.743
SDQ_11	AR10	0.646	SDQ_43	AP30	0.630
SDQ_12	AT6	0.780	SDQ_44	AT27	0.645
SDQ_13	AP6	0.642	SDQ_45	AR28	0.588
SDQ_14	AT8	0.684	SDQ_46	AT30	0.707
SDQ_15	AP8	0.603	SDQ_47	AT31	0.783
SDQ_16	AP10	0.576	SDQ_48	AR32	0.725
SDQ_17	AT11	0.628	SDQ_49	AT32	0.752
SDQ_18	AT13	0.723	SDQ_50	AR36	0.830
SDQ_19	AT14	0.621	SDQ_51	AP35	0.762
SDQ_20	AT10	0.662	SDQ_52	AP32	0.652
SDQ_21	AR12	0.610	SDQ_53	AT33	0.801
SDQ_22	AR14	0.561	SDQ_54	AP34	0.712
SDQ_23	AP14	0.591	SDQ_55	AT35	0.804
SDQ_24	AT15	0.589	SDQ_56	AN36	0.762
SDQ_25	AP16	0.479	SDQ_57	AM36	0.825
SDQ_26	AT18	0.563	SDQ_58	AK36	0.759
SDQ_27	AT19	0.613	SDQ_59	AJ36	0.736
SDQ_28	AR16	0.556	SDQ_60	AP36	0.794
SDQ_29	AT16	0.588	SDQ_61	AM35	0.736
SDQ_30	AP18	0.472	SDQ_62	AK35	0.681
SDQ_31	AR20	0.578	SDQ_63	AK34	0.667

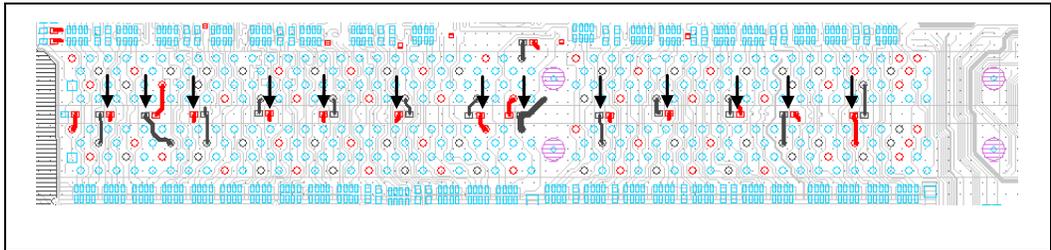


Signal	Intel® GMCH Ball	Package Length (Inches)	Signal	Intel® GMCH Ball	Package Length (Inches)
Data Mask Signals					
SDM_0	AP4	0.681	SDM_4	AT24	0.631
SDM_1	AR8	0.660	SDM_5	AP28	0.561
SDM_2	AP12	0.541	SDM_6	AR34	0.766
SDM_3	AR18	0.529	SDM_7	AL34	0.662
Data Strobe Signals					
SDQS_0	AR2	0.780	SDQS_4	AR24	0.564
SDQS_1	AT7	0.704	SDQS_5	AT29	0.670
SDQS_2	AT12	0.628	SDQS_6	AT34	0.823
SDQS_3	AT17	0.579	SDQS_7	AL36	0.744
Clock Signals					
SCMDCLK_0	AL21	0.387	SCMDCLK_0#	AK22	0.387
SCMDCLK_1	AN11	0.722	SCMDCLK_1#	AP11	0.720
SCMDCLK_2	AM34	0.826	SCMDCLK_2#	AL33	0.827
SCMDCLK_3	AP21	0.520	SCMDCLK_3#	AN21	0.523
SCMDCLK_4	AP9	0.793	SCMDCLK_4#	AN9	0.779
SCMDCLK_5	AP33	0.899	SCMDCLK_5#	AN34	0.898

5.3 System Memory Bypass Capacitor Guidelines

Discontinuities in the DDR signal return paths occur when the signals transition between the motherboard and the DIMMs. To account for this ground to 2.5 V discontinuity, a minimum of nine 0603 0.1 μF high-frequency bypass capacitors are required between the DIMMs to help minimize any anticipated return path discontinuities that may be created. The bypass capacitors connect to 2.5 V and ground. A wide trace should connect to a via that transitions to the ground cutout on layer two, and to the ground plane on layer three. The ground via should be placed as close to the ground pad as possible. A wide trace should connect the 2.5 V side of the capacitor to a via that transitions to the 2.5 V plane on layer four, then to the closest 2.5 V DIMM pin on either DIMM. These 2.5 V traces should be distributed evenly between the two DIMMs as shown in Figure 78. Finally, the 2.5 V via should be placed as close to the 2.5 V pad as possible.

Figure 78. DDR-DIMM Bypass Capacitor Placement



5.4 Power Delivery

The following guidelines are recommended for an 845G chipset DDR system memory design. The main focus of these GMCH guidelines is to minimize signal integrity problems and improve the power delivery of the GMCH system memory interface and the DDR-DIMMs.

5.4.1 2.5 V Power Delivery Guidelines

The 2.5 V power for the GMCH system memory interface and the DDR-DIMMs is delivered on layer one and on layer four around the DDR signals. Special attention must be paid to the 2.5 V copper flooding to ensure proper GMCH and DIMM power delivery. This 2.5 V flood must extend from the GMCH 2.5 V power vias all the way to the 2.5 V DDR voltage regulator and its bulk capacitors. The 2.5 V DDR voltage regulator must connect to the 2.5 V flood with a minimum of six vias, and the DIMM connector 2.5 V pins as well as the GMCH 2.5 V power vias must connect to the 2.5 V copper flood on layer four.

The copper flooding to the GMCH should include at least one finger on layer 1 and five fingers on layer 4 to allow for the routing of the DDR signals, and for optimal GMCH power delivery. The copper fingers must be kept as wide as possible to keep the loop inductance path from the 2.5 V voltage regulator to the GMCH at a minimum. In the areas where the copper flooding necks down under the GMCH, make sure to keep these neck down lengths as short and wide as possible.

Table 35 lists the minimum width requirements for the copper fingers going from the DIMM high frequency capacitors to the GMCH high frequency capacitors. It also describes the minimum neck down width requirements that the copper fingers can be reduced to for short distances from the GMCH high frequency capacitors through the GMCH ball field. **These neck down lengths must be kept as short as possible.** The width requirements listed in the table must be met at a minimum by the copper fingers to have good 2.5 V power delivery to the GMCH. Table 35 references Figure 81, which has a total of five copper fingers for GMCH 2.5 V power delivery. The copper finger numbering starts from the far left, and moves to the right.

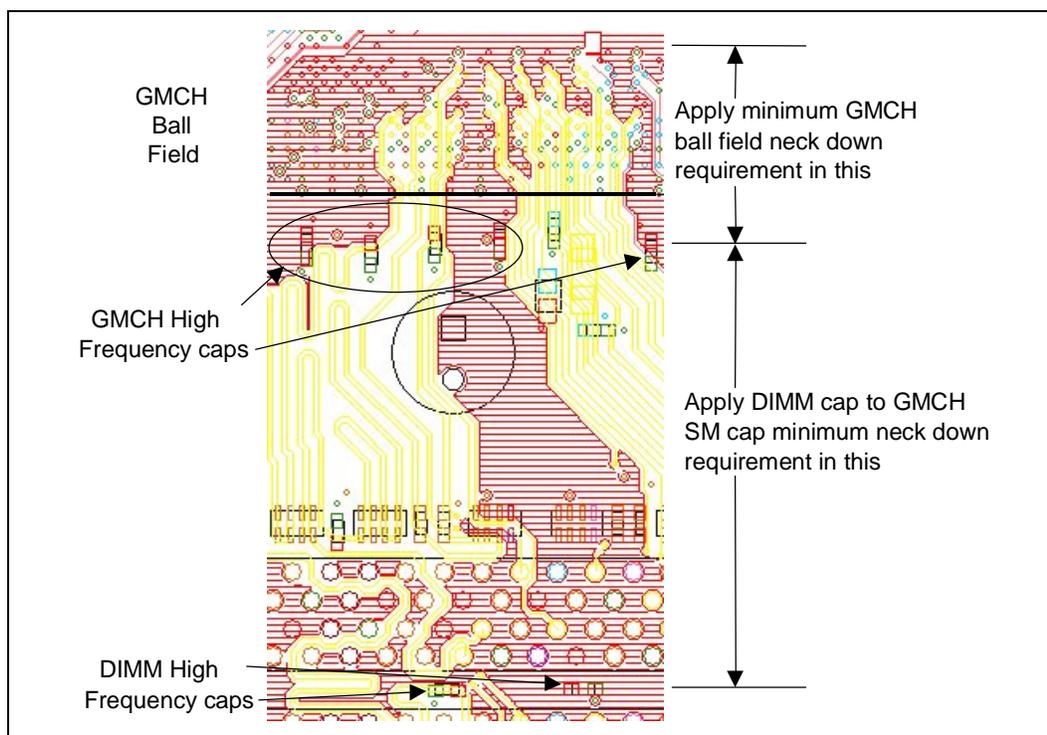
Table 35. Minimum 2.5 V Copper Finger Width Requirements

Cu Finger	Min Width (From DIMM Caps to GMCH SM Caps)	Min Neck Down Widths (Within GMCH Ball Field)
Layer 1	130 mils	100 mils
Layer 4 Number 1 (Left most finger)	150 mils	115 mils
Layer 4 Number 2	135 mils	40 mils
Layer 4 Number 3	90 mils	60 mils
Layer 4 Number 4	100 mils	50 mils
Layer 4 Number 5 (Right most finger)	80 mils	30 mils

To meet DC power delivery requirements to the GMCH, the layer one shape must connect to the following VCCSM balls: all in row AL (except AL37), all in row AK (except AK33), all in row AJ, all in row AH, all in row AG, and all in row AD. To meet the DC requirements, the left most finger on layer 4 (finger 1) must have vias placed by the following VCCSM balls (vias may be shared between balls): AU5, AU9, AP7, AL2, AL3, AL4, AL5, AL7, AL9, AK2, AK3, AK4, AK6, AK8, AJ3, AJ4, AJ5, AJ7, AJ9, AJ15, AJ19, AJ23, AJ27, and all in row AD.

To meet AC power delivery requirements, fingers that have capacitors placed in them (see recommendations later in this section) should meet the minimum width as stated, but the width should be maximized as much as possible

Figure 79. Example Implementation of Finger Width Requirement



The 2.5 V copper flooding must encompass all the DIMM 2.5 V pins. Figure 81 is an example of the layer four 2.5 V power delivery to the DIMMs.

Because the DDR control, address/command, CPC address, and clock signals are routed on the bottom signal layer between the GMCH and the first DIMM, the 2.5 V copper flooding on layer four is limited. To maximize the copper flooding, these signals should be kept as short as possible.

Finally, the eight GMCH 2.5 V high frequency decoupling capacitors located on the top signal layer should have their 2.5 V via placed directly over and connected to a 2.5 V copper finger. For guidelines on the GMCH 2.5 V high frequency decoupling capacitors refer to Section 5.4.2.1.

The following figures show examples of the 2.5 V power delivery copper flood for the GMCH and the DIMMs.

Figure 80. Layer One 2.5 V Power Delivery

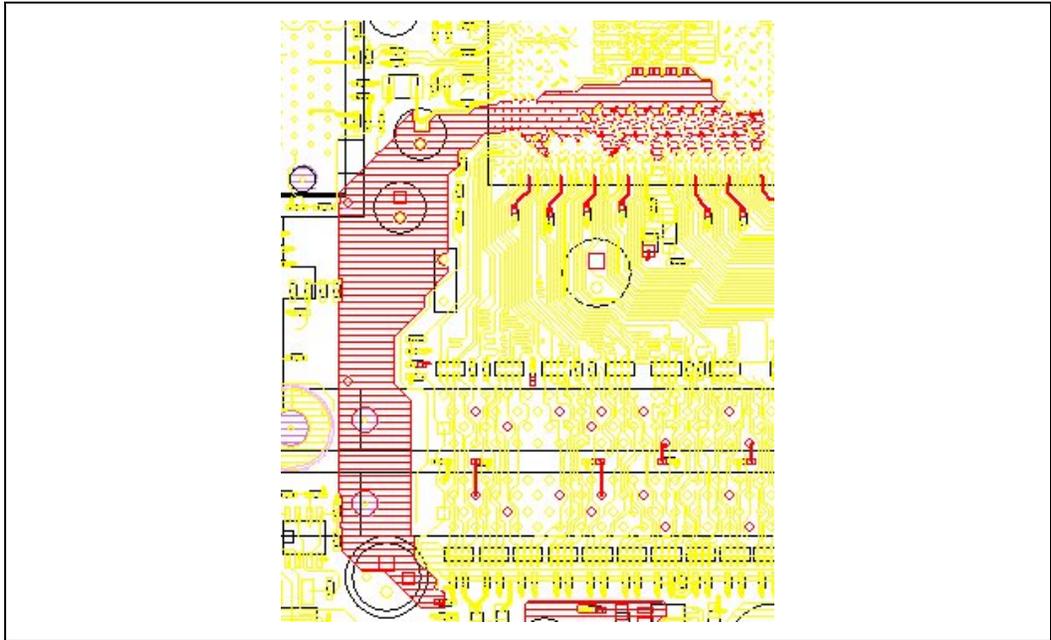
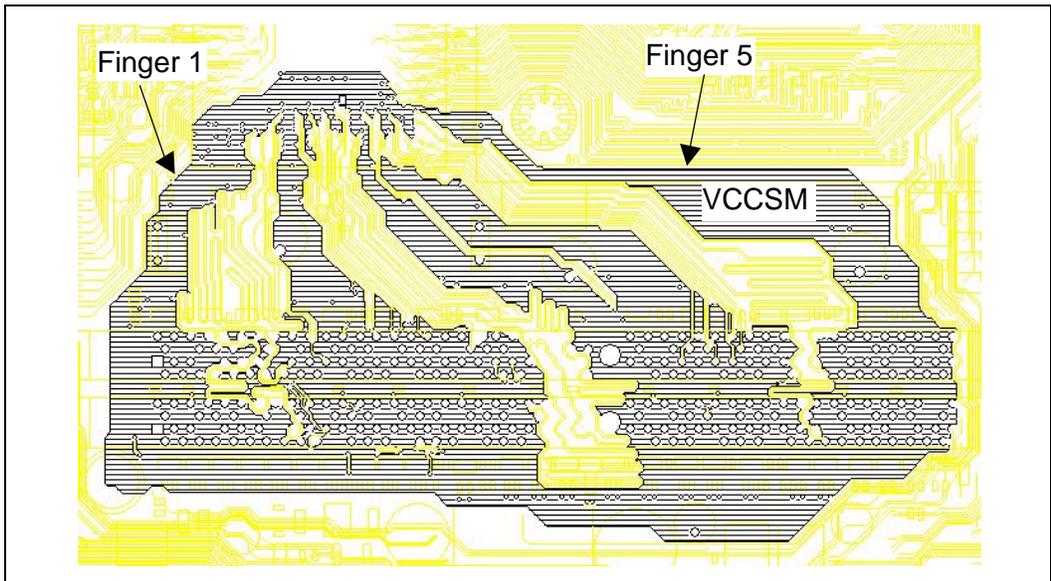


Figure 81. Layer Four 2.5 V Power Delivery



Maximize the amount of copper that is flooded on layer one and layer four from the 2.5 V Vreg through the DIMMs and to the GMCH. Care must be taken to ensure that enough copper is poured after the tuning of the DDR clocks and other signals.

5.4.2 Intel® GMCH System Memory Interface Decoupling Requirements

5.4.2.1 Intel® GMCH System Memory High Frequency Decoupling

Every GMCH ground and power ball in the system memory interface should have its own via where possible. For 2.5 V high frequency decoupling, a minimum of eight 0603 0.1 μ F high frequency capacitors are required, and must be within 100 mils of the GMCH package. These capacitors must be placed perpendicular to the GMCH, when appropriate, with the 2.5 V side of the capacitors facing the GMCH. The trace from the power end of the capacitor should be as wide as possible, and must connect to a 2.5 V power ball on the outer row of balls on the GMCH. The power balls that require a capacitor are AL37, AU5, AU9, AU13, AU17, AU25, AU29, and AU33. Each capacitor should have two vias placed directly over a 2.5 V copper finger that is located on layer four. One via should be placed within 25 mils of the capacitor pads, and the other via should be placed within 25 mils of the power ball. If the trace from the solder ball to the capacitor is less than 100 mils, one of the vias may be omitted. The ground end of the capacitors must connect to the ground cutout on layer two and to the ground plane on layer three through a via that is placed within 25 mils of the capacitor pad. The trace from the ground via to the capacitor pad must be as wide as possible. The following figures represent the GMCH DDR 2.5 V high frequency decoupling requirements.

Figure 82. Intel® GMCH DDR 2.5 V Decoupling Picture

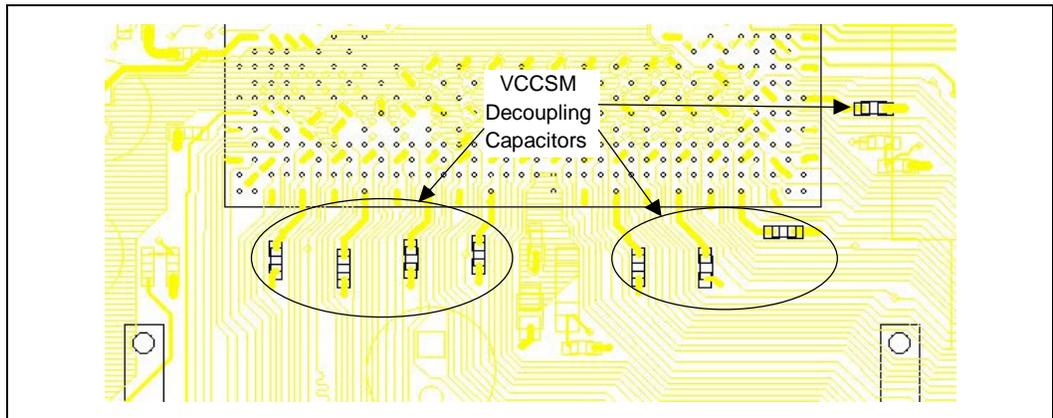


Figure 83. Intel® GMCH DDR 2.5 V Decoupling Capacitor Routing Alignment

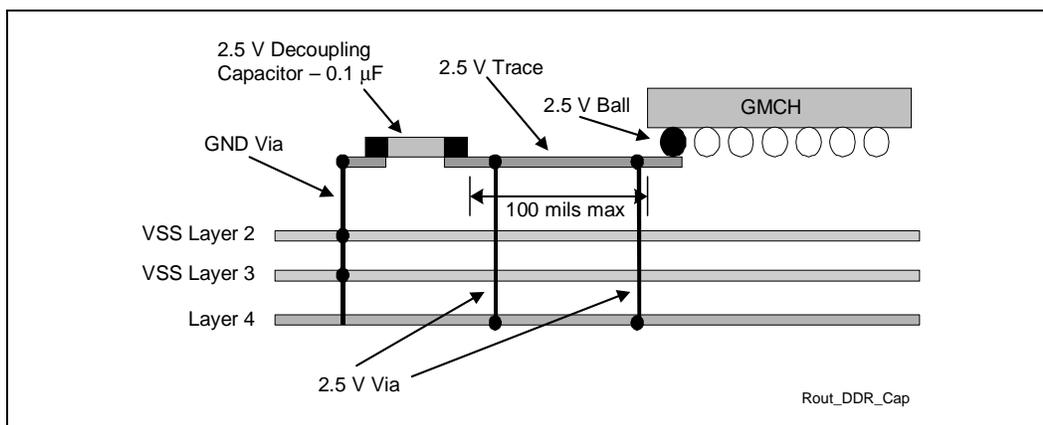


Table 36. Intel® GMCH System Memory Decoupling Capacitor Requirements

Parameter	Guideline
Capacitor number	Eight 0603 0.1 μF MLC capacitors – placed with trace leading to the following balls: AL37, AU5, AU9, AU13, AU17, AU25, AU29, and AU33
Capacitor placement	Within 100 mils of the GMCH
Capacitor pad to power ball trace width	Route as wide as possible minimum width of 18 mils
Power vias	Two vias, one placed within 25 mils of the capacitor pad and one placed within 25 mils of the power ball
Capacitor pad to ground via trace width	Route as wide as possible with a minimum width of 18 mils
Ground via	Placed within 25 mils of the capacitor pad

Note: If the trace from the power ball to the capacitor pad is less than 100 mils, one of the vias may be omitted.

5.4.2.2 Intel® GMCH System Memory Low Frequency Bulk Decoupling

The GMCH system memory interface requires low frequency bulk decoupling. Place four 100 μF electrolytic capacitors between the GMCH and the first DIMM connector. The power end of the capacitors must connect to 2.5 V on layer one or layer four, and the ground end of the capacitors must connect to ground on layer two and three. These capacitors are in addition to the bulk decoupling required by the 2.5 V regulator (regulator bulk decoupling is design specific).

Figure 84. Shared Intel® GMCH/DIMM 2.5 V Bulk Decoupling Example

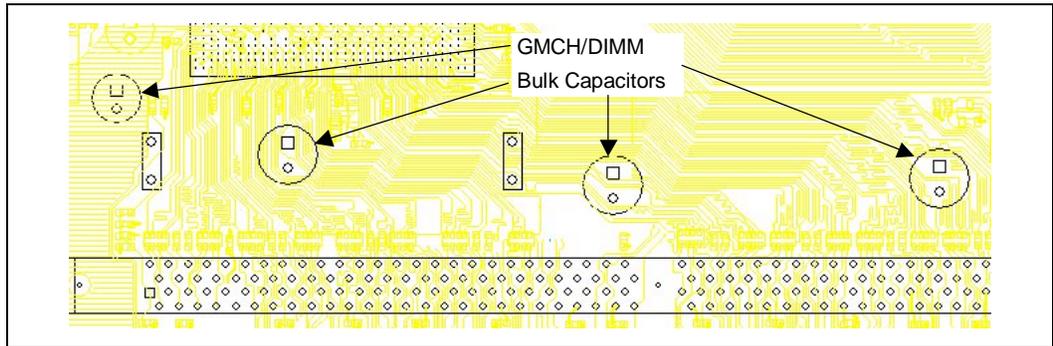


Table 37. Intel® GMCH System Memory Bulk Capacitor Requirements

Parameter	Guideline
Capacitor number	Four 100 μ F capacitors
Capacitor placement	Evenly placed between the GMCH and the DIMMs, with one of the 100 μ F capacitors connecting to the top layer copper flood.

5.4.3 DDR-DIMM Decoupling Requirements

The DDR DIMMs require bulk decoupling in addition to what is required by the GMCH. Place three more 100 μ F capacitors near the DIMM connectors as shown in Figure 85. The power end of the capacitors must connect to 2.5 V on layer one and layer four, and the ground end of the capacitors must connect to ground on layer two and three.

Figure 85. DDR DIMM 2.5 V Bulk Decoupling Example

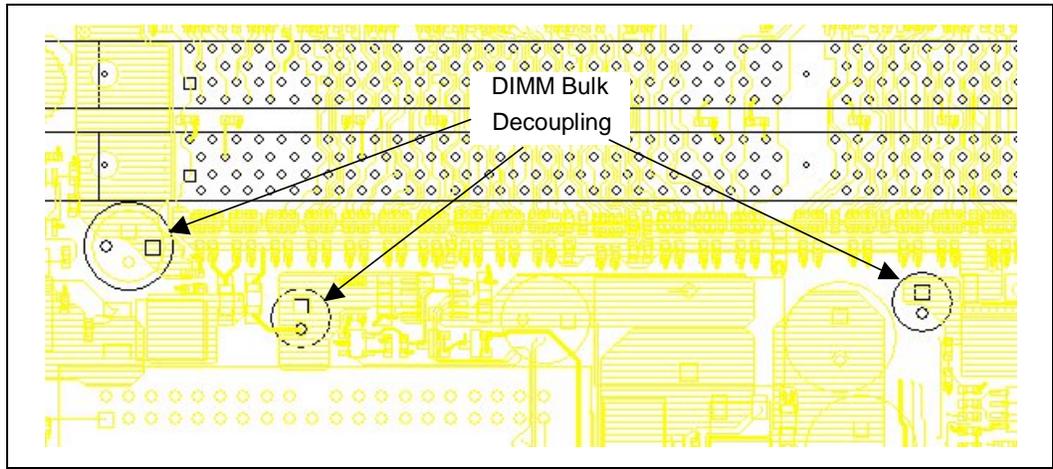


Table 38. Intel® GMCH System Memory Bulk Capacitor Requirements

Parameter	Guideline
Capacitor number	Three 100 μ F capacitors.
Capacitor placement	Place along bottom side of the DIMMs as shown in Figure 85.

5.4.4 DDR Reference Voltage

The DDR system memory reference voltage (VREF) is used by the DDR-SDRAM devices to compare the input signal levels of the data, command, and control signals, and is also used by the GMCH to compare the input data signal levels. VREF must be generated as shown in Figure 86. It should be generated from a typical resistor divider using 1%-tolerance resistors. The VREF resistor divider should be placed no further than 1.0” from the DIMMs. Additionally, VREF must be decoupled locally at each DIMM connector and at the GMCH. Finally, the VREF signal should be routed with as wide a trace as possible (12 mils minimum width) and should be isolated from other signals with a minimum of 12 mils spacing (during breakout from the GMCH, a minimum of 7 mil spacing can be maintained for a maximum length of 350 mils).

Figure 86. DDR VREF Generation Example Circuit

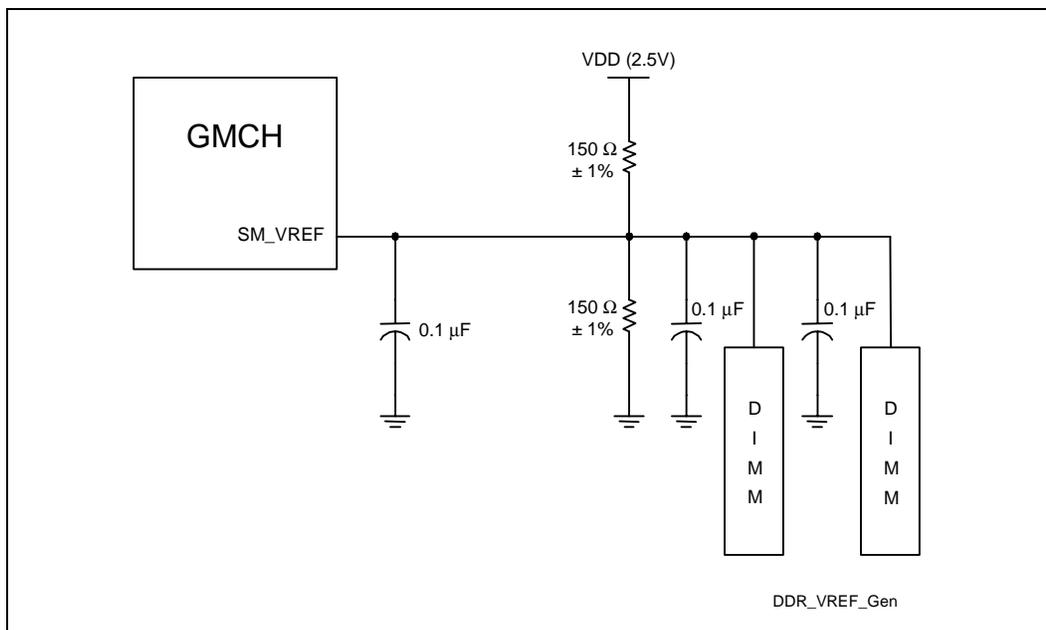


Table 39. DDR VREF Generation Requirements

Parameter	Guideline
VREF Routing	Minimum 12 mils wide and separated from other traces with a minimum 12 mils spacing, except during breakout, which is allowed 7 mil spacing to other signals for no more than 350 mils
Voltage Divider	Place resistor divider consisting of two resistors (50 Ω – 150 Ω, 1%) within 1.0” of the DIMM sockets. Note: Both resistors must be the same, have the same resistance value, and be 1%.
Decoupling requirements	Three 0603 0.1 μF capacitors
Decoupling placement	Place one decoupling cap at each of the DIMM sockets and one decoupling cap at the GMCH

5.4.5 DDR SMRCOMP Resistive Compensation

The GMCH uses a compensation signal to adjust the system memory buffer characteristics over temperature, process, and voltage variations. The DDR system memory (SMRCOMP) must be connected to the DDR voltage (2.5 V) through a $60.4 \Omega \pm 1\%$ resistor, and connected to ground through a $60.4 \Omega \pm 1\%$ resistor. A 0603 0.1 μF decoupling capacitor connected to 2.5 V and to ground should be used as shown in Figure 87. Do not connect any capacitor to the SMRCOMP signals. Place the capacitors within 1.0" of the GMCH package. The compensation signal and the power trace should be routed with a minimum of 12 mils wide, and should be isolated from other signals with a minimum of 10mils spacing.

Figure 87. DDR SMRCOMP Resistive Compensation

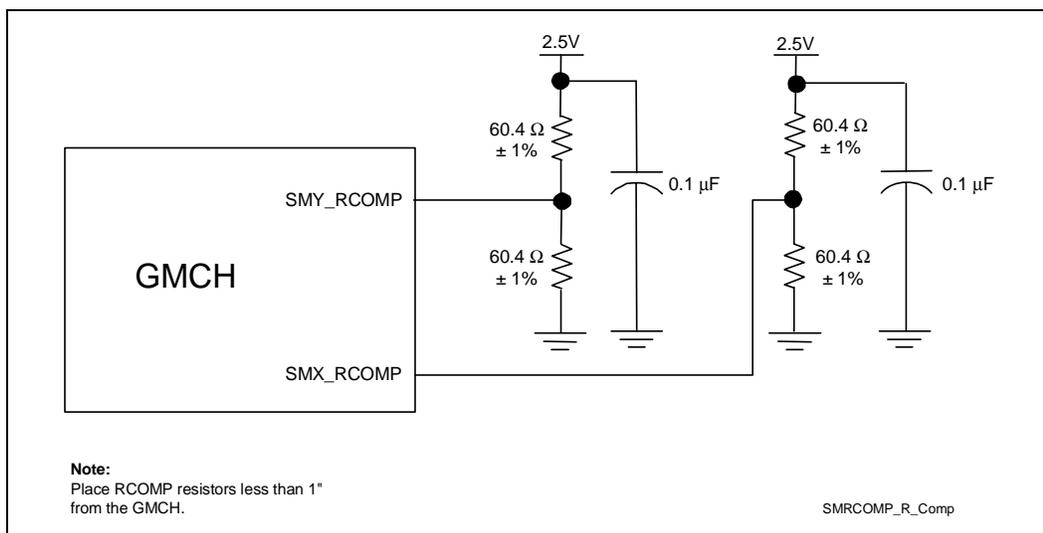


Table 40. DDR SMRCOMP Requirements

Parameter	Guideline
RCOMP Resistors	$60.4 \Omega \pm 1\%$ pulled to DDR 2.5 V, and $60.4 \Omega \pm 1\%$ tied to ground.
RCOMP Routing	Minimum width of 12 mils and isolated from other signals by 10 mils spacing.
Decoupling	Decouple each divider as shown in Figure 87.

5.4.6 DDR VTT Termination

All DDR signals except the command clocks must be terminated to 1.25 V (VTT) using 5% resistors at the end of the channel opposite the GMCH. Place a solid 1.25 V (VTT) termination island on the top signal layer just beyond the last DIMM connector, as shown in the following figures. The VTT Termination Island must be at least 50 mils wide. Use this termination island to terminate all DDR signals using one resistor per signal. Resistor packs are acceptable, with the understanding that the signals within an RPACK must be from the same DDR signal group. Termination resistor packs for each group must remain dedicated to that group, and must not be shared with any other signal groups. No mixing of signals from different DDR signal groups is allowed within an RPACK. The parallel termination resistors connect directly to the VTT Island on the top signal layer.

Figure 88. DDR VTT Termination Island Example

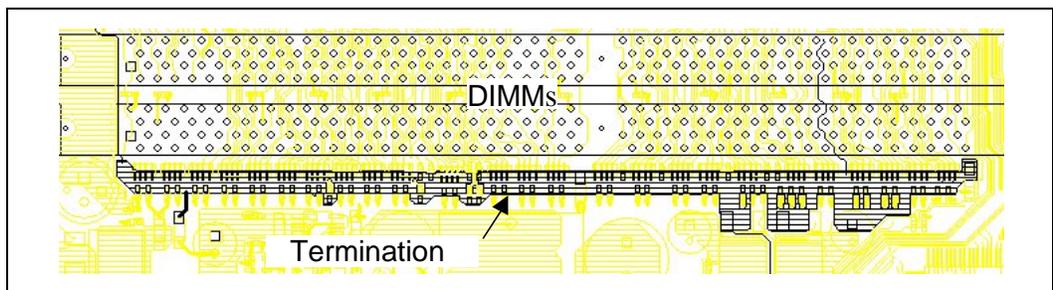


Table 41. DDR VTT Termination Island Requirements

Parameter	Guideline
Island Width	50 mils minimum
Resistor and capacitor connectivity	Connect termination resistors and decoupling capacitors directly to the termination island

5.4.6.1 VTT Termination Island High Frequency Decoupling Requirements

The VTT Island must be decoupled using high-speed bypass capacitors, one 0603 0.1- μ F capacitor per two DDR signals (or two capacitors per RPACK). These decoupling capacitors connect directly to the VTT Island and to ground, and must be spread-out across the Termination Island so that all the parallel termination resistors are near high-frequency capacitors. The capacitor ground via connecting the ground cutout on layer two and the ground plane on layer three should be within 25 mils of the capacitor pad, and the via and the pad should be connected with as wide a trace as possible. The distance from any DDR termination resistor pin to a 0.1 μ F VTT capacitor pin must not exceed more than 100 mils.

Finally, place one 4.7 μ F ceramic capacitor on each end of the termination island, and place one 4.7 μ F ceramic capacitor near the center of the termination island. The power end of these capacitors must connect to the VTT termination island directly, and the ground end of the capacitors must connect to ground on layer two and three.

Figure 89. DDR VTT Termination 0.1 μ F High Frequency Capacitor Example 1

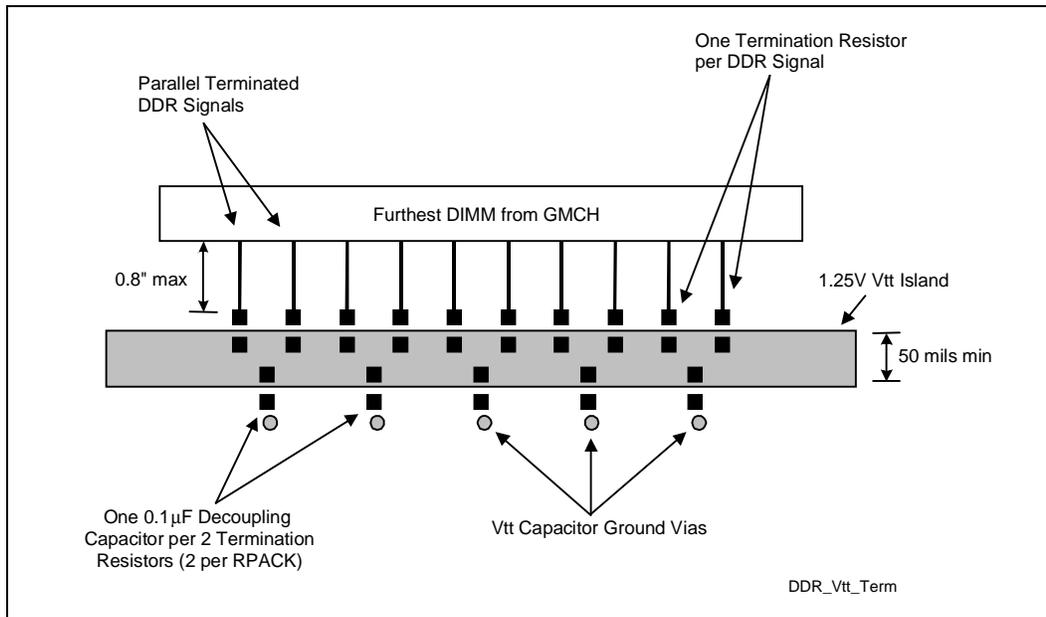


Figure 90. DDR VTT Termination 0.1 μ F High Frequency Capacitor Example 2

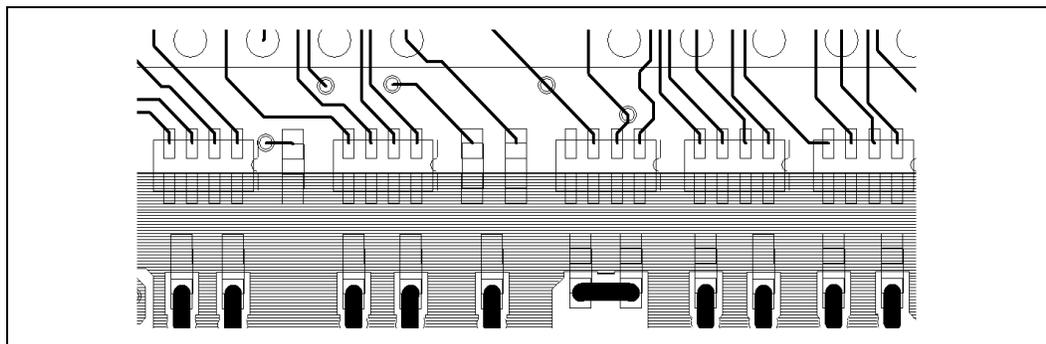


Figure 91. DDR VTT Termination 4.7 μ F High Frequency Capacitor Example

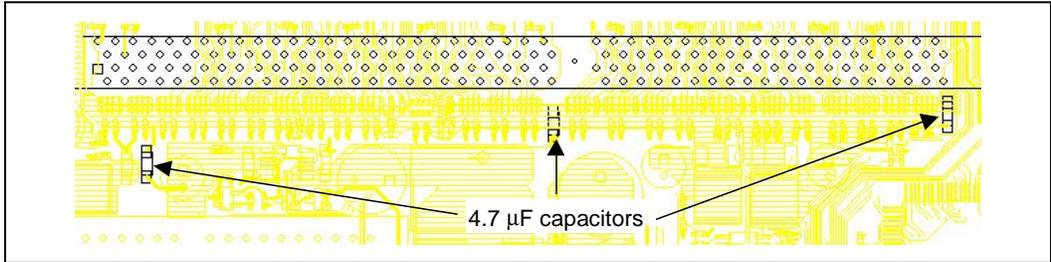


Table 42. DDR VTT Termination Island High Frequency Decoupling Requirements

Parameter	Guideline
0.1 μ F capacitors	Place one decoupling cap for every two DDR signals/termination resistors (or two caps for every RPACK). The distance from any termination resistor to decoupling capacitor should not exceed 100 mils.
4.7 μ F capacitors	Three capacitors needed. Place one capacitor each at the middle, left, and right sides of the termination island as shown in Figure 91.

5.4.6.2 VTT Termination Island Low Frequency Bulk Decoupling Requirements

The VTT Termination Island requires low frequency bulk decoupling. Ensure adequate decoupling of the DDRVTT rail to meet the DC and AC electrical requirements found in Section 5.4.7.7. Different VTT regulator designs may require different bulk decoupling requirements (refer to the latest version of the Customer Reference Board (CRB) schematics for an implementation example). Also, the output of the 1.25 V regulator must have enough bulk decoupling to ensure the stability of the regulator. The amount of bulk decoupling required at the output of the 1.25 V regulator will vary according to the OEM design targets.

Figure 92. DDR VTT Termination Low Frequency Capacitor Example

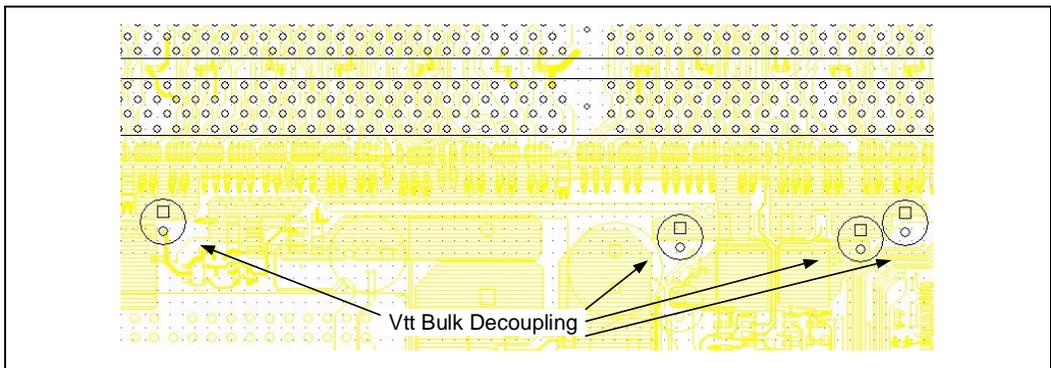


Table 43. DDR VTT Termination Island Low Frequency Capacitor Example (As Seen on CRB)

Parameter	Guideline
Capacitor number	Four 470 μ F capacitors (One 470 μ F capacitor is empty site only)
Capacitor placement	Place one capacitor at each end of the termination island.

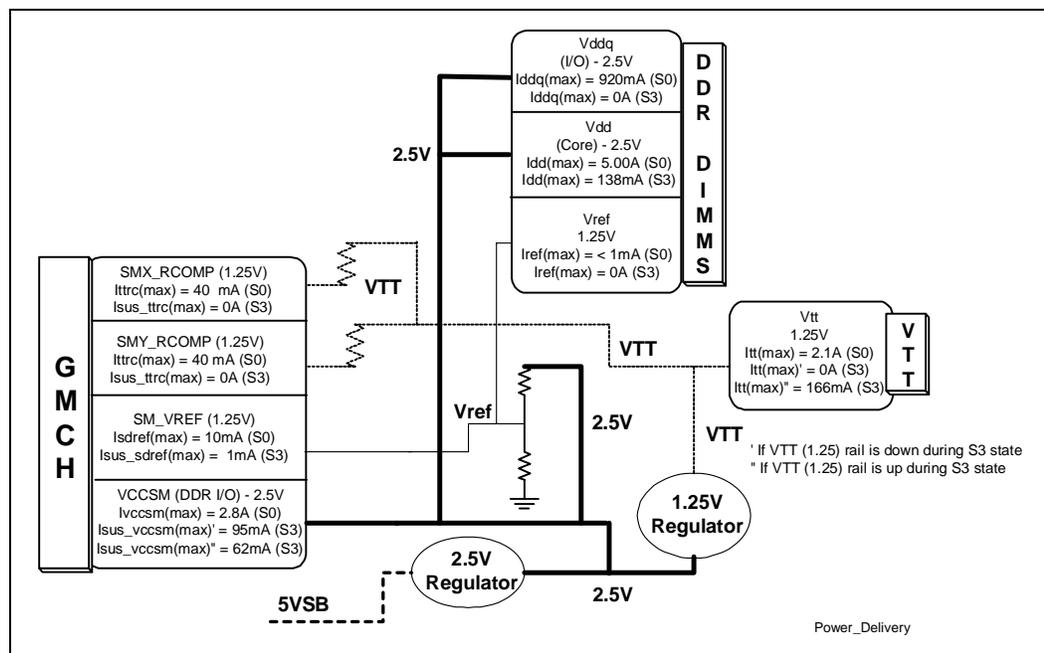
5.4.7 DDR Voltage Regulator Guidelines

The 845G chipset designs using the DDR-SDRAM memory sub-system require several voltages: Vdd/VddQ, VTT, and VREF. To generate these voltages, a 2.5 V and a 1.25 V regulator are required and must be designed to supply the required voltage and current levels to meet both the GMCH and DDR-SDRAM device requirements. The following sections define the range of DC and AC operating Voltage and Current conditions the 2.5 V and 1.25 V voltage regulators should meet for a two DIMM DDR-SDRAM based system with the 845G chipset. It does not attempt to define a specific voltage regulator implementation. DDR voltage regulation will be governed by either an on-motherboard regulator circuitry or a module with the necessary complement of external capacitance, and will vary according to the needs of OEM design targets.

5.4.7.1 Intel® 845G Chipset DDR Reference Board Power Delivery

Figure 93 shows the power delivery architecture for the 845G chipset DDR memory subsystem. This power delivery example provides support for the suspend-to-RAM (STR) and the full Power-on State.

Figure 93. Intel® 845G Chipset DDR Power Delivery Example



5.4.7.2 DDR 2.5 V Power Plane

The 2.5 V power plane, which is generated by the 2.5 V regulator, is used to supply power to the GMCH 2.5 V I/O Ring, the DDR-SDRAM 2.5 V Core, and the DDR-SDRAM 2.5 V I/O Ring. The 2.5 V regulator should be placed at the end of the DDR channel near the VTT Termination Island.

5.4.7.3 DDR 1.25 V Power Plane

The 1.25 V power plane, which is generated by the 1.25 V regulator, is used to supply the DDR termination voltage (VTT) and the GMCH SMRCOMP pull-up voltage (VTT). Special considerations must be taken for the 1.25 V regulator design because it must be able to source and sink a significant amount of current. The 1.25 V regulator should be placed at the end of the DDR channel near the VTT Termination Island.

5.4.7.4 DDR Reference Voltage (VREF)

The GMCH and DDR-DIMM reference voltage (VREF) is generated from a typical resistor divider circuit off the 2.5 V power plane. For guidelines on the VREF resistor divider, refer to the previous DDR VREF generation section.

5.4.7.5 DC and AC Electrical Characteristics (DIMM Supply Rails)

The DDR 2.5 V voltage regulator supplies the required voltages, Vdd/VddQ, and VREF, and current for up to two DDR-DIMMs, as shown in the following tables. The following DRAM Device specifications were determined at the DIMM connectors.

5.4.7.5.1 DDR-SDRAM DIMM Core and I/O Voltage (Vdd, VddQ)

The following conditions apply to the specifications listed below:

- Idd and IddQ are measured at maximum Vdd/VddQ and under maximum signal loading conditions.
- Note that these worst case values are for reference only and are based on current and future expected DRAM vendor specific specifications for maximum current.
- The worst-case Idd current draw was determined with the following criteria:
 - Both DIMM slots are populated with double-sided non-ECC x8 device DDR-DIMMs
 - Continuous back-to-back burst reads, with a burst length of 4, to one single bank in the same physical DIMM device row.
 - All other banks are in the active standby state where a row in each bank is activated/open.

Table 44. DDR-SDRAM DIMM Core and I/O Voltage and Current Requirements (Measured at the DIMM Connectors)

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
Core Supply Voltage, Static	Vdd	V	2.3	2.5	2.7
I/O Supply Voltage, Static	VddQ	V	2.3	2.5	2.7
Core Supply Current, Static	Idd	A			5.0
I/O Supply Current, Static	IddQ	A			0.920

5.4.7.5.2 DDR-SDRAM DIMM Reference Voltage (VREF)

The following conditions apply to the specifications listed below:

- IREF is measured at maximum VREF under maximum signal loading conditions.

Table 45. DDR-SDRAM DIMM Reference Voltage and Current Requirements (Measured at the DIMM Connectors)

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
Absolute I/O Reference Supply Voltage, Static	VREF	V	Vdd/2 – 0.05	Vdd/2	Vdd/2 + 0.05
I/O Reference Supply Current, Static	Iref	A			< 0.001

5.4.7.6 DC and AC Electrical Characteristics (Intel® GMCH Supply Rails)

The 2.5 V DDR voltage regulator supplies the required GMCH voltages, VCCSM and SDREF, and current as shown in the following tables. The following GMCH specifications were determined at the GMCH supply pins.

5.4.7.6.1 Intel® GMCH DDR Supply Voltage (VCCSM)

The following conditions apply to the specifications:

- Ivccsm is measured at maximum VCCSM under maximum signal loading conditions.

Note: These values are for reference only. Refer to the *Intel® 845G/845GL/845GV Chipset Datasheet*.

Table 46. Intel® GMCH DDR Supply Voltage and Current Requirements (Measured at the GMCH)

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
GMCH DDR Supply Voltage, Static	VCCSM	V	2.375	2.5	2.625
GMCH DDR Supply Current, Static	Ivccsm	A			2.8

5.4.7.6.2 Intel® GMCH Reference Voltage (VREF)

The following conditions apply to the specifications:

- Isdref is measured at maximum Vsdref under maximum signal loading conditions.

Note: These values are for reference only. Refer to the *Intel® 845G/845GL/845GV Chipset Datasheet*.

Table 47. Intel® GMCH DDR Reference Voltage and Current Requirements (Measured at the GMCH)

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
GMCH Reference Supply Voltage, Static	SDREF	V	VCCSM/2 – 2%	VCCSM/2	VCCSM/2 + 2%
GMCH Reference Supply Current, Static	Isdref	A			0.01

5.4.7.7 DC and AC Electrical Characteristics (VTT Supply Rail)

The 1.25 V DDR voltage regulator supplies the required DDR Termination Voltage (VTT) and current (Itt), and supplies the GMCH system memory resistive compensation pull-up voltage (VTT), and current (IttRC) as shown in the following tables.

5.4.7.7.1 DDR Termination Voltage (VTT)

The following conditions apply to the specifications:

- Itt is measured at maximum VTT under maximum signal loading conditions by looking at all the DDR signals, excluding the command clocks, with their specified series and parallel termination resistors.

Table 48. DDR Termination Voltage and Current Requirements

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
Termination Supply Voltage, Static	VTT	V	SM_VREF – 0.04	SM_VREF	SM_VREF + 0.04
Termination Supply Current, Static	Itt	A			2.1

5.4.7.7.2 DDR SMRCOMP Pull-up Voltage (VTT)

The following conditions apply to the specifications:

- Ittrc is measured at maximum VTT under maximum signal loading conditions.

Table 49. DDR Termination Voltage and Current Requirements

Parameter	Symbol	Unit	Minimum	Nominal	Maximum
SMRCOMP Termination Supply Voltage, Static	VTT	V	SM_VREF – 0.04	SM_VREF	SM_VREF + 0.04
SMRCOMP Termination Supply Current, Static	Ittrc	A			25 mA

5.4.7.8 DDR Voltage Regulator Reference Design Example

Refer to the Customer Reference Board schematic in Appendix A.

5.4.8 Power Sequencing Requirements

5.4.8.1 Intel® GMCH Power Sequencing Requirements

There is no GMCH power sequencing requirements. All GMCH power rails should be stable before deasserting reset, but the power rails can be brought up in any order desired. Good design practice has all GMCH power rails come up as close in time as practical, with the core voltage (1.5 V) coming up first.



5.4.8.2 DDR-SDRAM Power Sequencing Requirements

No DDR-SDRAM power sequencing requirements are specified during power up or power down if the following criteria are met:

- Vdd and VddQ are driven from a single power converter output.
- VTT is limited to 1.44 V (reflecting $V_{ddQ(max)}/2 + 50 \text{ mV}$ VREF variation + 40 mV VTT variation)
- VREF tracks $V_{ddQ}/2$
- A minimum resistance of 42 Ω (22 Ω series resistor + 22 Ω parallel resistor, 5% tolerance) limits the input current from the VTT supply into any pin.

If the above criteria cannot be met by the system design, the information in Table 50 must be adhered to during power up:

Table 50. Power-up Initialization Sequence

Voltage Description	Sequencing	Voltage Relationship to Avoid Latch-up
VddQ	After or with Vdd	$< V_{dd} + 0.3 \text{ V}$
VTT	After or with VddQ	$< V_{ddQ} + 0.3 \text{ V}$
VREF	After or with VddQ	$< V_{ddQ} + 0.3 \text{ V}$

NOTE: The information in the table applies if the previously-listed requirements are not met.

6 SDR (PC133) System Memory Design Guidelines

6.1 SDRAM Signal Groups

The 82845G GMCH SDR (PC133) Synchronous DRAM (SDRAM) memory interface consists of CMOS signals. These CMOS signals can be divided into five signal routing group categories: Data, Control, Address / Command, Clock, and Feedback.

The SDR SDRAM system memory interface is multiplexed with DDR. For SDR board designs, the MEMSEL strap should be pulled-down through a 200 Ω resistor (refer to the *Intel® 845G/845GL/845GV Chipset Datasheet* for additional information). The SDR guidelines should be used for designing a SDR system board. Although the GMCH directly supports SDR and DDR SDRAM channels, the SDR guidelines should not be used for DDR designs.

Table 51. Intel® 82845G GMCH SDR Signal Routing Groups

Data	Control	Address / Command	Clock	Feedback
SDQ_[63:0] SDM_[7:0]	SCS_[7:0]# SCKE_[3:0]	SMAA_[12:0] SBA_[1:0] SRAS# SCAS# SWE#	SCK_[7:0]	SRDCLK_OUT SRDCLK_IN

NOTE: The SDR pins are multiplexed onto DDR pins.

6.2 PC133 System Memory Topology and Layout Design Guidelines for Two DIMMs

To provide a good current return path and limit noise on system memory signals, all system memory signals should be referenced to a single contiguous plane from the GMCH to the DIMM connectors, and from DIMM connector to DIMM connector. The following PC133 system memory guidelines should be followed in an 845G chipset platform based on the four-layer stack-up example in Section 3.2, the GMCH system memory signal ball field, and the GMCH system memory package referencing.

6.2.1 PC133 DIMM Topology and Layout Guidelines

6.2.1.1 Data — SDQ_[63:0], SDM_[7:0]

The GMCH provides one pin per data bus signal. This signal group includes the 64-bit data bus and the 8 bits for the Data Mask (SDM) bus signals. Each data mask signals corresponds to a data bus group. The SDM signals are routed by zones. These signals should break out of the GMCH and be routed to the DIMMs on the top layer in a daisy chain topology.

The following figures and table describe the recommended topology and layout routing guidelines for the SDR SDRAM data signals.

Figure 94. DIMM Routing Topology for Data Signals

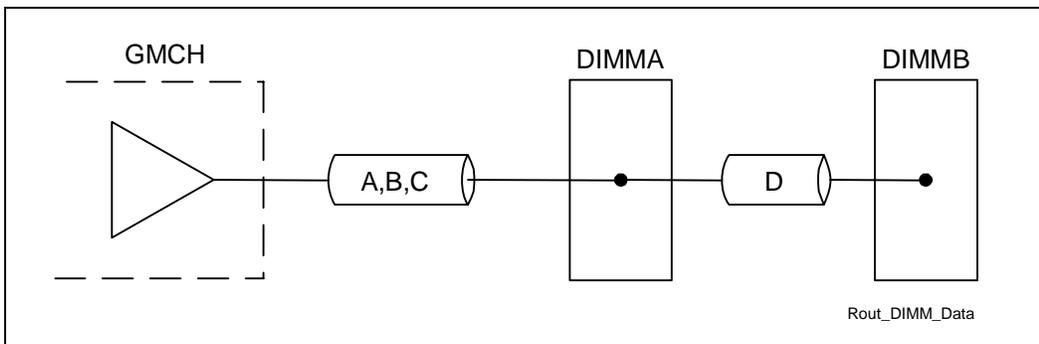


Table 52. DIMM Routing Guidelines for SDQ_[63:0], SDM_[7:0] Data Signals

Parameter	Routing Guidelines
Topology	Daisy Chain
Reference Plane	Single plane referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Minimum Trace Spacing	12 mils
Minimum Group Spacing (spacing from other signal groups)	12 mils
Trace Length to first DIMM for SDM – A	2.0" to 4.0"
Trace Length to first DIMM for SDQ Zone 2 – B ¹	2.0" to 4.0"
Trace Length to first DIMM for SDQ Zone 1 – C ¹	2.0" to 4.4"
Trace Length – D	0.4" to 0.6"
Breakout Guidelines	5 mil width with 5 mil min spacing for a max of 0.50"

NOTES:

1. As defined in the Intel SDRAM Unbuffered DIMM Specification, Revision 1.
2. Data Zone 1: SDQ_[63:56, 39:24, 7:0]
3. Data Zone 2: SDQ_[55:40, 23:8]

6.2.1.2 Control — SCS_[7:0]#, SCKE_[3:0]

The GMCH provides two chip select outputs and one clock enable output signal per PC133 DIMM device row. These signals are single plane referenced and should transition from the top signal layer to the bottom signal layer under the GMCH, and should be routed to the DIMMs. The trace lengths from these signal balls to their signal vias, under the GMCH should be kept as short as possible. Table 53 summarizes the SDR control signal mapping.

Table 53. SDR Control Signal DIMM Mapping

Signal	Relative To	DIMM Pin
SCS_0#	DIMM A	30
SCS_1#	DIMM A	114
SCS_2#	DIMM A	45
SCS_3#	DIMM A	129
SCS_4#	DIMM B	30
SCS_5#	DIMM B	114
SCS_6#	DIMM B	45
SCS_7#	DIMM B	129
SCKE_0	DIMM A	128
SCKE_1	DIMM A	63
SCKE_2	DIMM B	128
SCKE_3	DIMM B	63

The following figures and tables describe the recommended topology and layout routing guidelines for a single PC133 DIMM socket. This topology and layout routing guidelines should be repeated for both PC133 DIMM slots.

Figure 95. Routing Topology For SCS# Signals

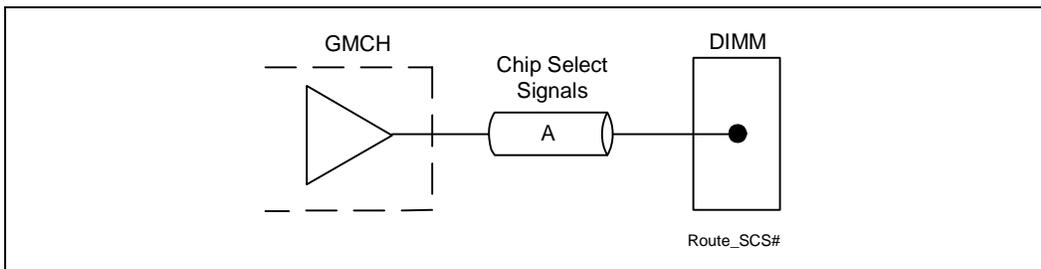
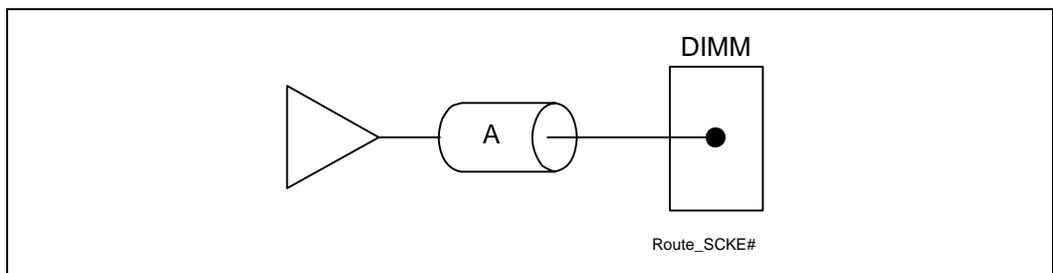


Table 54. Routing Guidelines for SCS_[7:0]# Signals

Parameter	Routing Guidelines
Topology	Point to point
Reference Plane	Single plane referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Z_0)	$60 \Omega \pm 15\%$
Trace Width	5 mils
Minimum Trace Spacing	12 mils
Minimum Group Spacing (spacing from other signal groups)	12 mils
Trace Length – A	3.0" to 4.0"
Breakout Guidelines	5 mil width with 5 mil spacing for a max of 0.50"

Figure 96. Routing Topology For SCKE# Signals**Table 55. Routing Guidelines for SCKE_[3:0]# Signals**

Parameter	Routing Guidelines
Topology	Point to point
Reference Plane	Single plane referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Z_0)	$45 \Omega \pm 15\%$
Trace Width	8 mils
Minimum Trace Spacing	12 mils
Minimum Group Spacing (spacing from other signal groups)	12 mils
Trace Length – A	3.0" to 4.0"
Breakout Guidelines	5 mil width with 5 mil spacing for a max of 0.50"

6.2.1.3 Address / Command — SMAA_[12:0], SBA_[1:0], SRAS#, SCAS#, SWE#

The GMCH provides one pin per address signal, one pin for SRAS#, one pin for SCAS#, one pin for SWE#, and one pin per bank address signal. These signals are single plane referenced. They should transition from the top signal layer to the bottom signal layer under the GMCH, and should be routed to the first DIMM, then to the second DIMM in a daisy chain topology. The trace lengths from the signal balls to their signal vias, under the GMCH should be kept as short as possible.

The following figures and table describe the recommended topology and layout routing guidelines for the SDR SDRAM address/command signals.

Figure 97. Routing Topology For Address / Command Signals

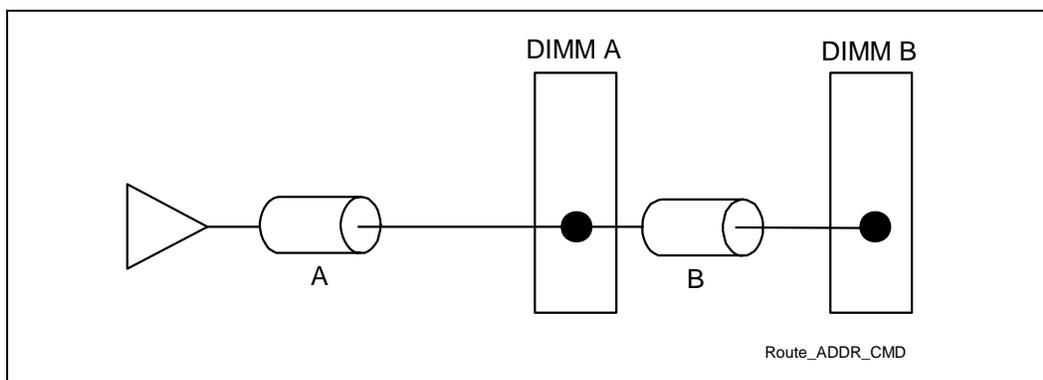


Table 56. Routing Guidelines for SMAA_[12:0], SBA_[1:0], SRAS#, SCAS#, SWE# Signals

PARAMETER	ROUTING GUIDELINES
Topology	Daisy Chain
Reference Plane	Single plane referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	60 Ω ± 15%
Trace Width	5 mils
Minimum Trace Spacing	12 mils
Minimum Group Spacing (spacing from other signal groups)	12 mils
Trace Length – A	2.0" to 3.5"
Trace Length – B	0.4" to 0.6"
Breakout Guidelines	5 mil width with 5 mil min spacing for a max of 0.50"

6.2.1.4 Clocks — SCK_[7:0]

The GMCH provides eight total clocks (four per SDRAM DIMM). Two clocks are routed to each SDRAM device row. The clock signals should transition from the top signal layer to the bottom signal layer, and should be routed to the DIMMs on the bottom signal layer. The clocks should be length matched from GMCH die pad to DIMM pin. Refer to Table 57 for package trace length data.

The following tables list both the necessary package trace lengths and the signal mapping for the SCK, SCS#, and SCKE signals.

Table 57. SCK_[7:0] DIMM Mapping and Intel® GMCH Package Trace Lengths

CLOCK	DIMM	DIMM PIN	Intel® GMCH Ball	Package Trace Length (inches)
SCK_0	A	42	AP9	0.793
SCK_1	A	125	AN9	0.779
SCK_2	A	79	AP33	0.899
SCK_3	A	163	AN34	0.898
SCK_4	B	42	AN11	0.722
SCK_5	B	125	AP11	0.720
SCK_6	B	79	AM34	0.826
SCK_7	B	163	AL33	0.827

DIMMA is closest to the GMCH, and DIMMB is furthest from the GMCH.

The following figures and table describe the recommended topology and layout routing guidelines for the PC133 clocks. This topology and layout routing guidelines should be repeated for both PC133 DIMM slots.

Figure 98. Routing Topology For Clock Signals

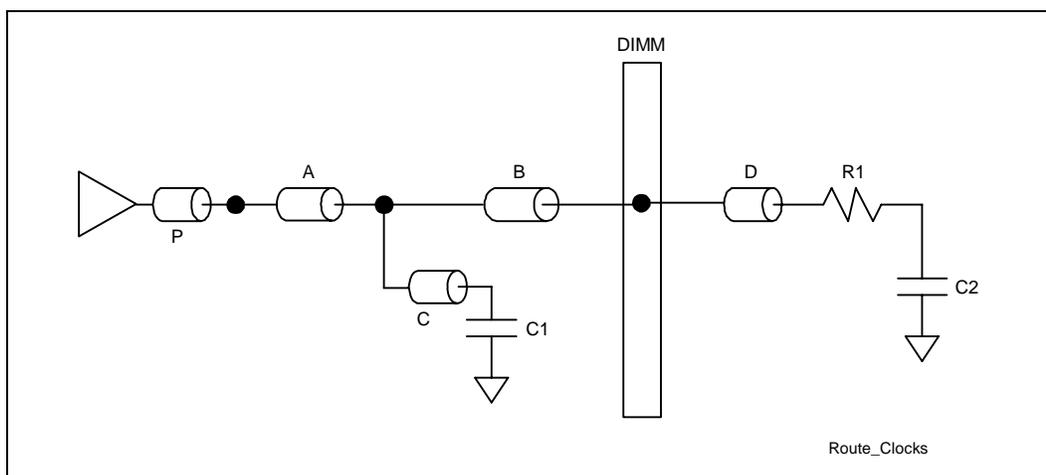


Table 58. Routing Guidelines for SCK_[7:0] Clock Signals

Parameter	Routing Guidelines
Topology	Point to Point, w/ AC Termination
Reference Plane	Ground referenced
Characteristic Trace Impedance (Z_0)	$50 \Omega \pm 15\%$
Trace Width	7 mils
Minimum Trace Spacing	15 mils
Minimum Group Spacing (spacing from other signal groups)	15 mils
Trace Length – P (package trace length)	Refer to Table 57 for package trace lengths
Trace Length – A	0.0" to 0.5" from GMCH ball to EMI capacitor stub
Trace Length – B	4.3" to 5.2"
Trace Length – C	0.0" to 0.25" (stub to component pad)
Trace Length – D	0.5" to 1.5"
Total Length Limits (P+A+B)	$5.7" \pm 0.02"$ from GMCH die pad to DIMM pin
Breakout Guidelines	5 mil width with 5 mil min spacing for a max of 0.50"

NOTES:

1. The value of the AC termination network, R1 and C2, is 51Ω and $270 \text{ pF} \pm 5\%$.
2. The value of the EMI filter capacitor C1 is $22 \text{ pF} \pm 5\%$.

6.2.1.5 Feedback — SRDCLK_OUT, SRDCLK_IN

The GMCH provides a feedback reference clock output (SRDCLK_OUT) and reference clock input (SRDCLK_IN) that are used during SDRAM reads. The SRDCLK_OUT ball is connected directly to the SRDCLK_IN ball through a very short trace on the motherboard through a resistor. A test point should be added to this net for probing. **The resistor serves as a configuration jumper, and serves no termination function. It should not be stuffed.** The resistor site can be located on the bottom side of the board if necessary.

The following figures and table describe the recommended topology and layout routing guidelines for the SDRAM feedback signal.

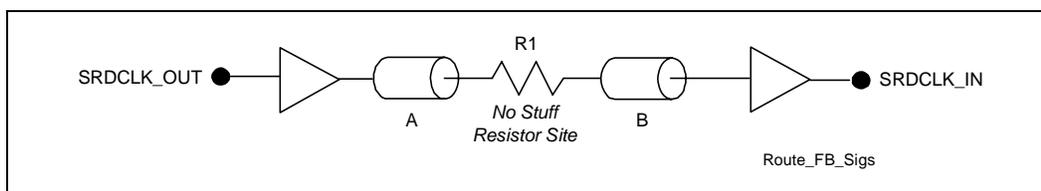
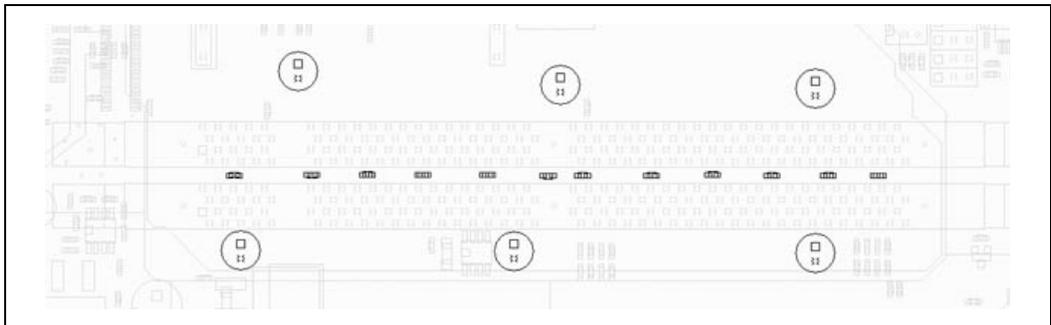
Figure 99. Routing Topology for Feedback Signals


Table 59. 2-DIMM Routing Guidelines for SRDCLK_OUT, SRDCLK_IN Feedback Signals

Parameter	Routing Guidelines
Topology	Point to Point, w/ Resistor Jumper
Reference Plane	Ground referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Z_0)	$60 \Omega \pm 15\%$
Minimum Trace Width	5 mils
Minimum Group Spacing (spacing from other signal groups)	5 mils
Trace Length pad to resistor – A	0 to 100 mils
Trace Length pad to resistor – B	0 to 100 mils

6.3 DIMM Decoupling Guidelines

Bypass capacitors should be added between the VCCSM voltage rail and ground, where VCCSM is the 3.3 V power plane. Place nine evenly spaced 0.1 μF capacitors between the DIMMs. This should ensure a clean current return path. For bulk decoupling, place six 100 μF bulk capacitors around the DIMMs. See Figure 100.

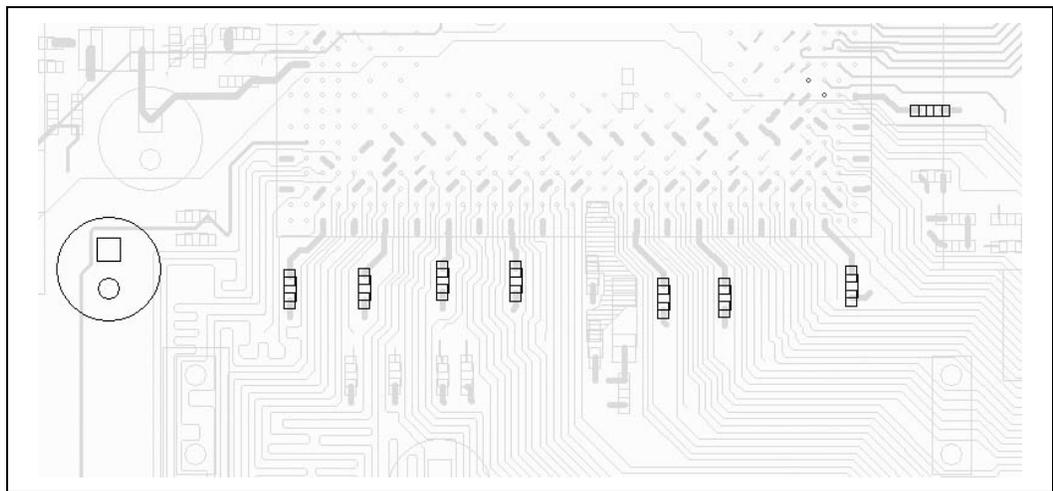
Figure 100. DIMM Decoupling Example


6.4 Intel® GMCH VCCSM Decoupling Guidelines

The GMCH requires both high frequency and bulk decoupling for VCCSM. Where possible, every GMCH power and ground ball in the system memory interface should have its own via. For 3.3 V high frequency decoupling, a minimum of six 0603 0.1 μ F capacitors are required. These capacitors should be evenly distributed along the GMCH SDR interface as shown in Figure 101. The trace from the ground end of the capacitor should be as wide as possible, and must connect to an outer row ground ball on the on the GMCH. The power ball of the capacitor should via down directly to the 3.3 V power plane. The via should be within 25 mils of the capacitor pad, and the trace from the via to the pad should be as thick as possible with a minimum width of 18 mils.

For low frequency decoupling, one 100 μ F capacitor at the GMCH is recommended. See Figure 101 for a placement example.

Figure 101. Intel® GMCH VCCSM Decoupling Example



6.5 Compensation

A system memory compensation resistor, SMRCOMP is used by the GMCH to adjust buffer characteristics to specific board and operation environment characteristics. This is a 20 Ω \pm 1% resistor to ground that is placed near the GMCH. This trace should be routed a maximum of 1.25", with a minimum width of 10 mils. Keep this trace a minimum of 7 mils away from other signals.

6.6 System Memory Reference Voltage

The SDREF signals are to be tied to a resistor divider network capable of supplying at least 10 mA of current. The output of this voltage divider is $\frac{1}{2}$ VCCSM. Use 1% resistors and decouple with one 0.1 μ F capacitor at the GMCH. The trace to the voltage divider should be



routed at a maximum of 3" in length, with a minimum width of 12 mils. Keep this trace a minimum of 10 mils away from other signals.



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7 AGP / Multiplexed DVO Design Guidelines

For detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms), refer to *AGP Interface Specification, Revision 2.0*, which can be obtained from <http://www.agpforum.org>. This design guide focuses only on specific 845G chipset platform recommendations.

7.1 AGP Interface

The GMCH multiplexes the AGP signal interface with two Digital Video Out (DVO) ports. When an external AGP device is utilized, the multiplexed DVO ports are not available, and the GMCH IGD is disabled. For flexible motherboard designs that make use of a 1.5 V AGP connector, the multiplexed DVO ports can be utilized only via an AGP Digital Display (ADD) card.

The guidelines for AGP card support and ADD card support are the same. There are **no** separate guidelines for systems that only support AGP cards.

The Intel® 815 chipset multiplexes a display cache interface with its AGP interface. A Graphics Performance Accelerator (GPA) card was required to make use of that display cache interface. Because the GMCH has a multiplexed digital display interface and not a multiplexed display cache interface, the GPA will not function in an 845G chipset system. Because GPAs are keyed for a 3.3 V AGP connector, they are not compatible with the 1.5 V AGP connector used with the GMCH.

A single AGP connector is supported by the GMCH AGP interface. SERR# and PERR# from the AGP connector are not supported. The AGP buffers operate in only one mode:

- 1.5 V drive, not 3.3 V safe. This mode is compliant with the AGP 2.0 Specification. The 845G chipset can make use of a 1.5 V only AGP connector.

AGP 4X, 2X and 1X must operate at 1.5 V. The AGP interface supports up to 4X AGP signaling. AGP semantic cycles to DRAM are not snooped on the host bus.

The GMCH supports PIPE# or SBA_[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA_[7:0] mechanism must be selected during system initialization

The AGP interface is clocked from a 66-MHz clock. The AGP interface is asynchronous to the host bus, system memory, and internal graphics device. The AGP interface is synchronous to the Hub Interface with a clock ratio of 1:1 (66 MHz : 66 MHz).

7.1.1 AGP Digital Display (ADD) Card

The GMCH multiplexes the AGP signal interface with two DVO ports. These DVO ports are capable of supporting a variety of digital display devices such as TMDS transmitters and TV-Out encoders. It is possible to use the DVO ports in dual-channel mode to support higher resolutions and refresh rates (single channel mode is limited to a 165 MHz pixel clock rate).

Flexible motherboard designs may make use of a 1.5 V AGP connector. In this scenario, an ADD card is required to make use of the multiplexed DVO ports. The ADD card is designed to plug into a 1.5 V AGP connector. When an ADD card is populated, the GMCH cannot support an external AGP device. When an external 1.5 V AGP device is populated, the GMCH cannot support the ADD card.

7.2 AGP 2.0

The *AGP Interface Specification*, Revision 2.0, enhances the functionality of the original *AGP Interface Specification*, Revision 1.0, by allowing 4X data transfers (i.e., 4 data samples per clock), and 1.5-volt operation. The 4X operation of the AGP interface provides for "quad-pumping" of the AGP AD (address/data) and SBA (side-band addressing) buses. That is, data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is $\frac{1}{4}$ of a 15-ns (66-MHz) clock or 3.75 ns. It is important to understand that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, data is sampled twice during a 66-MHz clock cycle. Therefore, the data cycle time is 7.5 ns. To allow for these high-speed data transfers, the 2X mode of AGP operation uses source-synchronous data strobing. During 4X operation, the AGP interface uses differential source-synchronous strobing.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be long. If the mismatch between a data line and the associated strobe is too great, or if there is noise on the interface, incorrect data will be sampled. The low-voltage operation on AGP (1.5 V) requires even more noise immunity.



7.2.1 AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: 1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals. Each group has different routing requirements. In addition, within the 2X/4X timing domain signals, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements, as well as trace width and spacing requirements. Because of the multiplexed AGP/DVO interface, there are trace length matching requirements within each set of 2X/4X signals, as well as between sets of 2X/4X signals. The signal groups are listed in Table 60.

Table 60. AGP 2.0 Signal Groups

1X Timing Domain	2X / 4X Timing Domain	Miscellaneous, Async
CLK (3.3 V) GRBF# GWBF# GST_[2:0] GPIPE# GREQ# GGNT# GPAR GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL#	Set #1 GAD_[15:0] GC/BE_[1:0]# GADSTB_0 GADSTB_0# ¹ Set #2 GAD_[31:16] GC/BE_[3:2]# GADSTB_1 GADSTB_1# ¹ Set #3 GSBA_[7:0] GSBSTB GSBSTB# ¹	USB+ USB- OVRCNT# PME# TYPDET# PERR# SERR# INTA# INTB#

Note: ¹These signals are used in 4X AGP mode ONLY.

Table 61. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobe in 2X	Associated Strobes in 4X
GAD_[15:0] and GC/BE_[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	GADSTB_0	GADSTB_0, GADSTB_0#
GAD_[31:16] and GC/BE_[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	GADSTB_1	GADSTB_1, GADSTB_1#
GSBA_[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	GSBSTB	GSBSTB, GSBSTB#

Throughout this section, the term *data* refers to GAD_[31:0], GC/BE_[3:0]#, and GSBA_[7:0]. The term *strobe* refers to GADSTB_[1:0], GADSTB_[1:0]#, GSBSTB, and GSBSTB#. When the term *data* is used, it refers to one of the three sets of data signals, as in Table 60. When the term *strobe* is used, it refers to one of the strobes as it relates to the data in its associated group.

The routing guidelines for each group of signals (1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals) are addressed separately.

7.3 AGP Routing Guidelines

7.3.1 1X Timing Domain Routing Guidelines

- The AGP 1X timing domain signals (refer to Table 60) have a maximum trace length of 6". This maximum applies to ALL signals listed as 1X timing domain signals in the table.
- AGP 1X timing domain signals can be routed with 5 on 7 trace separation.
- Trace length matching requirements for 1X timing domain signals apply only to 1X signals multiplexed with DVO signals. GIRDY# and GDEVSEL# should be matched (± 250 mils), as should GTRDY# with GFRAME#, and GSTOP# with GAD_15.

7.3.2 2X/4X Timing Domain Routing Guidelines

These trace length guidelines apply to ALL signals listed in Table 60 as 2X/4X timing domain signals. These signals should be routed using 5-mil (60 Ω) traces.

For motherboards that utilize an AGP connector, the maximum length of AGP 2X/4X timing domain signals is 6".

- 1:3 trace width-to-spacing is required for AGP 2X/4X signal traces.
- AGP 2X/4X signals must be matched with their associated strobe (as described in Table 61) from GMCH pad to AGP pin within ± 0.125 ". Refer to Table 62 for GMCH AGP nominalized package lengths.
- Strokes should match their complement to ± 50 mils.
- GADSTB_0 should match GADSTB_1 to ± 0.125 ".

For example, if GADSTB_0 is 2.6" long, GADSTB_0# should also be 2.6". The data signals associated with those strobe signals (e.g., GAD_[15:0] and GC/BE_[1:0]#) must be no more than 0.125" different in length than *either* of their associated strobes. This means that if GADSTB_0 is 2.6" long and GADSTB_0# is 2.65" long, then GAD_[15:0] and GC/BE_[1:0]# must be between 2.525" and 2.725" long. The GADSTB_1 pair should also be matched to 2.6 ± 0.125 ", their associated data signals then matched to ± 0.125 " of the GADSTB_1 pair. The GSBSTBs are not directly related to the GADSTBs.

The strobe signals (GADSTB_0, GADSTB_0#, GADSTB_1, GADSTB_1#, GSBSTB, and GSBSTB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Because AGP 4X uses a differential clocking scheme, the pair should be routed together and on the same layer (e.g., GADSTB_0 and GADSTB_0# should

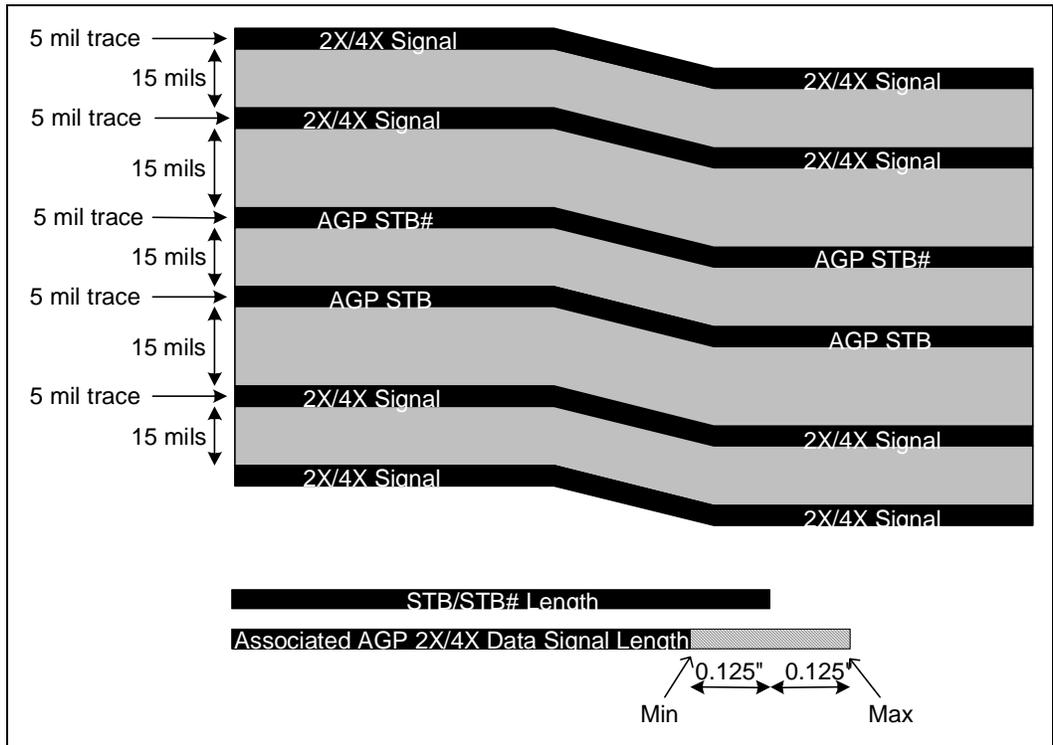


be routed next to each other). The two strobes in a strobe pair should be routed using 5-mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals, and all other signals, by at least 20 mils (1:4). The strobe pair must be length-matched to less than ± 50 mils.

Table 62. Intel® GMCH AGP Nominalized Package Lengths

Data Signal	Intel® GMCH Ball	Package Length (Inches)	Data Signal	Intel® GMCH Ball	Package Length (Inches)
GSBSTB	F4	0.662	GADSTB_1	M8	0.443
GSBSTB#	E5	0.671	GADSTB_1#	L7	0.458
GSBA_7	F2	0.763	GAD_31	G4	0.628
GSBA_6	F3	0.688	GAD_30	K8	0.437
GSBA_5	E2	0.760	GAD_29	H3	0.679
GSBA_4	E4	0.716	GAD_28	J7	0.505
GSBA_3	D2	0.769	GAD_27	J5	0.580
GSBA_2	D3	0.767	GAD_26	J4	0.616
GSBA_1	C2	0.832	GAD_25	K3	0.640
GSBA_0	C3	0.812	GAD_24	G2	0.742
			GAD_23	H4	0.623
GADSTB_0	V8	0.384	GAD_22	L4	0.605
GADSTB_0#	U7	0.395	GAD_21	L5	0.549
GAD_15	P3	0.573	GAD_20	M3	0.641
GAD_14	T8	0.367	GAD_19	J2	0.676
GAD_13	R7	0.410	GAD_18	K2	0.663
GAD_12	R5	0.493	GAD_17	K4	0.575
GAD_11	R2	0.638	GAD_16	P8	0.364
GAD_10	T4	0.524			
GAD_9	T3	0.586			
GAD_8	T2	0.635	GCBE3#	H2	0.754
GAD_7	V3	0.574	GCBE2#	M2	0.675
GAD_6	U2	0.602	GCBE1#	N4	0.581
GAD_5	U4	0.514	GCBE0#	R4	0.557
GAD_4	U5	0.494			
GAD_3	W5	0.461			
GAD_2	W4	0.529			
GAD_1	V2	0.607			
GAD_0	V4	0.492			

Figure 102 2X/4X Routing Example





7.3.3 AGP Routing Guideline Considerations and Summary

- The 2X/4X timing domain signals can be routed with 5-mil spacing when breaking out of the GMCH. It is recommended that the routing widen to the documented requirements < 0.3" from the GMCH package.
- Reduce line length mismatch to ensure added margin. Trace length mismatch for all signals within a signal group should be as close to zero as possible to provide timing margin.
- To reduce trace-to-trace coupling (cross-talk), separate the traces as much as possible.
- Ideally, all signals in a signal group should be routed on the same layer. Data and associated strobe signals must not be routed on a separate layer for more than 3".

The trace length and trace spacing requirements must not be violated by any signal.

Table 63. AGP 2.0 Routing Summary

Signal	Max. Length	Trace Spacing (5-mil Traces)	Length Mismatch	Relative To	Notes
1X Timing Domain	6 "	7 mils	No requirement	N/A	None
2X/4X Timing Domain Set 1	6 "	15 mils ¹	± 0.125"	GADSTB_0 and GADSTB_0#	GADSTB_0, GADSTB_0# must be the same length (± 50 mils); match GADSTB_0 to GADSTB_1 within 0.125"
2X/4X Timing Domain Set 2	6 "	15 mils ¹	± 0.125"	GADSTB_1 and GADSTB_1#	GADSTB_1, GADSTB_1# must be the same length (± 50 mils); match GADSTB_1 to GADSTB_0 within 0.125"
2X/4X Timing Domain Set 3	6 "	15 mils ¹	± 0.125"	GSBSTB and GSBSTB#	GSBSTB, GSBSTB# must be the same length (± 50 mils)

NOTES:

1. These guidelines apply to board stack-ups with 15% impedance tolerance.

7.3.4 AGP Clock Routing

The maximum total AGP clock skew between the GMCH and the graphics component is 1 ns for all data transfer modes. This 1 ns includes skew and jitter that originates on the motherboard, add-in card, and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but also at all points on the clock edge that fall within the switching range. The 1 ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew. (The motherboard designer determines how the 0.9 ns is allocated between the board and the synthesizer.)

For the 845G chipset platform AGP clock routing guidelines, refer to the clocking guidelines in Section 13.2.4.

7.3.5 AGP Signal Noise Decoupling Guidelines

The following routing guidelines are recommended for the optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the GMCH. The following guidelines are not intended to replace thorough system validation on 845G chipset-based products.

- Five 0.1 μ F capacitors are required and must be as close as possible to the GMCH. These should be placed within 100 mils of the outer row of balls on the GMCH for VDDQ decoupling. The closer the placement, the better.
- The designer should evenly distribute placement of decoupling capacitors in the AGP interface signal field.
- It is recommended that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.
- To add the decoupling capacitors within 100 mils of the GMCH and/or close to the vias, the trace spacing for AGP signals may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal, and for as short a distance as possible.
- In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. On a typical four layer PCB design, the signals transition from one side of the board to the other. One 0.01 μ F capacitor is required per 5 vias. The capacitor should be placed as close as possible to the center of the via field.

7.3.5.1 1.5 V AGP Connector Decoupling

The designer should ensure that the AGP connector is well decoupled. The following recommendations are derived from the *AGP Design Guide Revision 1.0*, Section 1.5.3.3 Connector AC Signal Decoupling Requirements:

The decoupling capacitor recommendations for the AGP connector are intended to address AC signaling issues and not power delivery issues. The main reason for not addressing power delivery issues with the motherboard connector decoupling is because of the connector inductance and the distance the capacitors are from the graphics device. These two factors negate much of the usefulness of the connector decoupling on the motherboard for power delivery purposes. The following are recommendations for decoupling at the AGP connector on the motherboard:

- VCC3_3: Three 0.01 μ F or larger, low ESL capacitors. Each capacitor should be placed as close as possible to a VCC3_3 pair of pins on the connector.
- Vddq: Six 0.01 μ F or larger, low ESL capacitors. Each capacitor should be placed as close as possible to a Vddq pair of pins on the connector.
- +5 V: One 0.01 μ F or larger, low ESL capacitor placed as close as possible to the +5 V connector pins.
- +12 V: One 0.01 μ F or larger, low ESL capacitor placed as close as possible to the +12 V connector pin.
- 3.3VAUX: One 0.01 μ F or larger, low ESL capacitors placed as close as possible to the 3.3VAUX connector pin(s).

7.3.6 AGP Routing Ground Reference

It is strongly recommended that the following critical signals be referenced to ground from the GMCH to an AGP connector (or to an AGP video controller, if implemented as a "down" solution on the motherboard), using a minimum number of vias on each net: GADSTB_0, GADSTB_0#, GADSTB_1, GADSTB_1#, GSBSTB, GSBSTB#, GTRDY#, GIRDY#, GGNT#, and GST_[2:0].

For DVO support on the AGP interface, it is strongly recommended that all the AD/CBE signals be referenced to ground. In an ideal design, the complete AGP interface signal field would be referenced to ground. This recommendation is not specific to any particular PCB stack-up, but should be applied to all 845G chipset designs.

7.4 AGP 2.0 Power Delivery Guidelines

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller (or the DVO device in an ADD scenario). This voltage is always 3.3 V. If the graphics controller (or DVO device) needs a lower voltage, the add-in card must regulate the 3.3 V VCC voltage to the device's requirements. The graphics controller may ONLY power AGP I/O buffers with the 1.5 V VDDQ power pins. In the ADD card scenario, any output signal from the card must not exceed 1.5 V. This means that I²C (normally 3.3 V) and DDC (normally 5 V) signals must have a level-shifting device *on the ADD card* to ensure that 1.5 V is not exceeded.

Because the GMCH supports only 1.5 V signaling, flexible VDDQ (1.5 V or 3.3 V) voltage regulation and TYPEDET# circuitry should not be implemented. TYPEDET# does not have to be routed from the AGP connector because it is not used to set VDDQ on 845G chipset-based platforms.

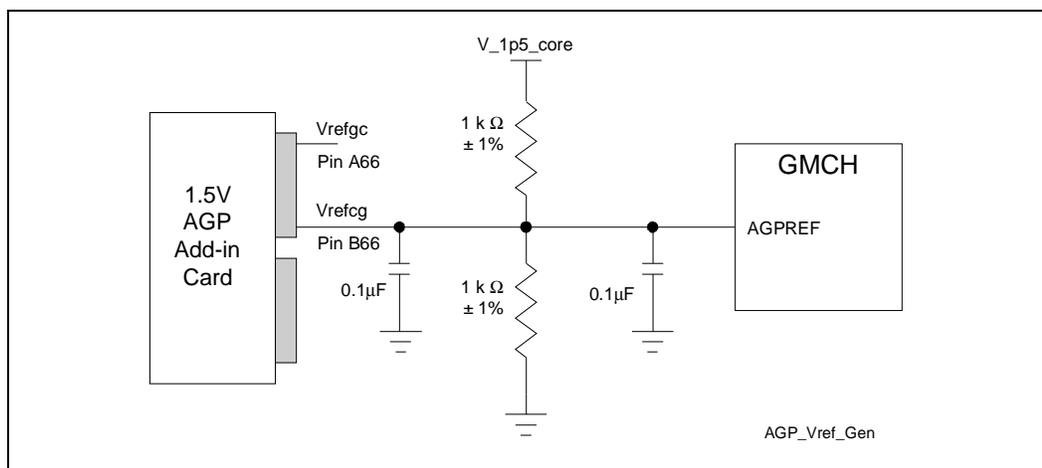
7.4.1 VREF Generation for AGP 2.0

Both the graphics controller and the GMCH are required to generate VREF and distribute it through the connector. The following two pins are defined on the AGP 2.0 universal connector to allow this VREF passing:

- VREFGC — VREF from the graphics controller to the chipset.
- VREFCG — VREF from the chipset to the graphics controller.

The GMCH does not make use of the VREFGC, but 845G chipset systems are still required to supply a voltage ($\frac{1}{2}$ of VDDQ) through VREFCG. Regardless of whether or not the platform uses AGP, VREF must always be supplied to the GMCH. See Figure 103 for an example circuit.

Figure 103. AGP VREF Generation



7.5 Additional AGP Design Guidelines

7.5.1 Compensation

The GMCH AGP interface supports resistive buffer compensation (RCOMP). Tie the AGP_RCOMP pin to a 40 Ω , 1% pull-down resistor to ground through a very short (<0.5") trace.

7.5.2 AGP Pull-Ups

AGP control signals require resistors that pull up to VDDQ on the motherboard to ensure that they contain stable values when no agent is actively driving the bus. The GMCH has integrated the following pull-up resistors. However, the signals may still require pull-up resistors:

1X Timing Domain Signals

- GFRAME#
- GSTOP#
- GWBF#
- GTRDY#
- GRBF#
- GGNT#
- GIRDY#
- GPIPE#
- GST_[2:0]
- GDEVSEL#
- GREQ#
- GPAR¹

NOTES:

1. To assure that ADD vs. AGP detection occurs properly, 845G chipset systems must have a pull-up resistor on the GPAR line.

It is critical that these signals be pulled up to 1.5 V.

SERR#/PERR# should be pulled up to Vddq at the AGP connector.

The trace stub to the pull-up resistor on 1X timing domain signals should be kept at less than 0.5", to avoid signal reflections from the stub.

Note: The strobe signals require pull-ups/pull-downs on the motherboard to ensure that they contain stable values when no agent is driving the bus.

2X/4X Timing Domain Signals

- GADSTB_[1:0] (pull up to 1.5 V).
- GSBSTB (pull up to 1.5 V)
- GADSTB_[1:0]# (pull down to ground)
- GSBSTB# (pull down to ground)

The trace stub to the pull-up/pull-down resistor on 2X/4X timing domain signals should be kept to less than 0.1" to avoid signal reflections from the stub.

The pull-up/pull-down resistor value requirements are $R_{min} = 4 \text{ k}\Omega$, and $R_{max} = 16 \text{ k}\Omega$. The recommended AGP pull-up/pull-down resistor value is 8.2 k Ω .

7.5.2.1 AGP Signal Voltage Tolerance List

The following signals on the AGP interface are 3.3 V tolerant during 1.5 V operation:

- PME#
- INTA#
- INTB#
- CLK
- RST

The following signals on the AGP interface are 5 V tolerant (refer to the USB 2.0 specification):

- USB+
- USB-
- OVRCNT#

The following special AGP signal is either GROUNDED or NOT CONNECTED on an AGP card.

- TYPEDET#

Note: All other signals on the AGP interface are in the VDDQ group. For an 82845G GMCH, they are only 1.5 V tolerant!

Note: INTA# and INTB# should be pulled to 3.3 V, not to VDDQ.

7.6 Motherboard/Add-In Card Interoperability

There are three AGP connectors: *3.3 V AGP connector*, *1.5 V AGP connector* and *Universal AGP connector*. The **GMCH supports only the 1.5 V AGP connector**.

The GMCH can support either an external 1.5 V capable AGP device, or an ADD card. The GMCH cannot support both devices simultaneously.

The GPA card that provides a display cache for the Intel® 815 chipset will not function in an 845G chipset platform. Because GPAs are keyed for a 3.3 V AGP connector, they are not compatible with the 1.5 V AGP connector that is used with 845G chipsets.

All assumptions relating to AGP routing include 2" of trace on the AGP card. If an AGP device is used down on the board, 2" can be added to trace lengths. All other guidelines still apply.

7.7 AGP/ DVO Shared Interface

As described previously, the AGP interface of the 845G chipset is multiplexed or shared with a digital display interface. In other words, the same component pins (balls) are used for both interfaces, although obviously only one interface can be supported at any given time. As a result, DVO signals are mapped onto the AGP interface. This interface can be configured in either AGP mode, or Digital Video Out (DVO) mode. Additionally, if an AGP connector is used, DVO down cannot be implemented. In the AGP mode, the interface supports a full AGP 4X interface. In DVO mode, the interface becomes a digital display interface.

7.7.1 AGP Digital Display (ADD) Card Considerations

To support the fullest display flexibility, a digital display device may reside on an ADD card that complies with the 1.5 V AGP connector form factor. If the motherboard designer follows the routing guidelines for the AGP interface detailed in previous sections, the customer has a wide variety of options. A 1.5 V AGP connector on an 845G chipset platform can utilize either an AGP Graphics card or an ADD card, or can be left unpopulated to obtain the lowest-cost solution. Some ADD/845G chipset interfacing implications are as follows.

- A pull-up resistor is required on GPAR/ADD_DETECT# to allow the GMCH to determine whether an ADD card or AGP card is populated. The GMCH has integrated a pull-up for this function, but an external site may still be required on the motherboard. The ADD card pulls this signal down stronger than the on-board pull-up to indicate to the 845G chipset that it should operate in DVO mode.
- Any I/O signals on the ADD card that exceed the 1.5 V signaling level (e.g., I²C and DDC), must have a level shifting device on the ADD card. No output signal from the ADD card to the GMCH may exceed 1.5 V.

7.7.2 ADD Clocking

The digital display interface is clocked source synchronously by the GMCH. The digital display interface clocking scheme uses four output clock signals: DVOB_CLK and DVOB_CLK#, and DVOC_CLK and DVOC_CLK #; and a single clock input: DVOBC_CLKINT#. The four output clocks are muxed with the AD strobes and should be routed according to the AGP strobe guidelines described in previous sections. DVOBC_CLKINT# is only an input clock when the DVO device on the ADD card is running in TV-Out mode. This input clock is multiplexed with the AD13 line.

7.7.3 Multiplexed Intel® DVO Down

If an external AGP device\connector is not implemented, it is possible to solder DVO devices down on the motherboard. GMCH multiplexed DVO ports (DVOB and DVOC) are 1.5 V interfaces that can each support transactions up to 165 MHz. The DVO ports are capable of interfacing with a wide variety of DVO port compliant devices (e.g., discrete TV encoder, discrete TMDS transmitter, combination TV encoder and TMDS transmitter or LVDS transmitters).

All assumptions relating to DVO routing include 1.5" of trace on the ADD card. If a DVO device is used down on the board, 1.5" can be added to trace lengths from the previous section.

In a DVO device down scenario, a 330 Ω pull-down to GND is required on GPAR/ADD_DETECT#, as well as on SBA_7/ADD_ID7.

The GMCH controls the video front-end devices via the multiplexed I²C interfaces. The MI2C_DATA and MI2C_CLK pins should be used to communicate with I²C compliant DVO devices. I²C is a two-wire communications bus/protocol. The protocol and bus are used to configure registers in the DVO device. GMCH also utilizes the MDVI_CLK and MDVI_DATA to collect EDID (Extended Display Identification) from a digital display panel.

Do not interchange or modify the functionality of MI2C and MDVI signals. Each of these signals require a 4.7 k Ω pull-up to 1.5 V (or pull-up with the appropriate value derived from simulation). These signals are 1.5 V tolerant. If higher signaling voltages are needed (3.3 V for MI2C and 5 V for MDVI), level-shifting devices are required on the motherboard.

7.7.4 Intel[®] DVO Interface Routing Guidelines

Route data signals (DVOxData[11:0]) with a trace width of 5 mils, and a trace spacing of 15 mils. To break out of the GMCH, the DVO data signals can be routed with a trace width of 5 mils, and a trace spacing of 5 mils. The signals should be separated to a trace width of 5, and a trace spacing of 15 mils within 0.3" of the GMCH component. The maximum trace length for the DVO data signals is 7.5 ". These signals should each be matched within ± 0.125 " of their associated Clk(#) signals.

Route the DVOx_Clk (#) signals 5 mils wide and 15 mils apart. This signal pair should be a minimum of 20 mils from any adjacent signals. The maximum length for DVOx_Clk(#) is 7.5 ", and the two signals should be the same length.

DVOx_CLK is the primary clock of the differential pair. Care should be taken to ensure that DVOx_CLK is connected to the primary clock receiver on the DVO device. If the DVO device supports differential clocking mode (highly recommended), DVOx_CLK# should be connected to the complementary clock receiver of the DVO device.

7.8 Leaving the Intel[®] 845G Chipset AGP / DVO Port Unconnected

If the motherboard does not implement any of the possible graphics/display devices with the AGP/DVO port, the following is recommended on the motherboard:

- Voltages, including AGP_VREF, must still be supplied to the GMCH.
- Signals can be left as NCs – initial boards may want to have empty back up sites for the pull-up resistors outlined in Section 7.5.2
- AGP_RCOMP should still be connected to a 40 Ω 1% pull down to ground.

8 **Analog Display Port**

8.1 **Analog RGB/CRT**

8.1.1 **RAMDAC/Display Interface**

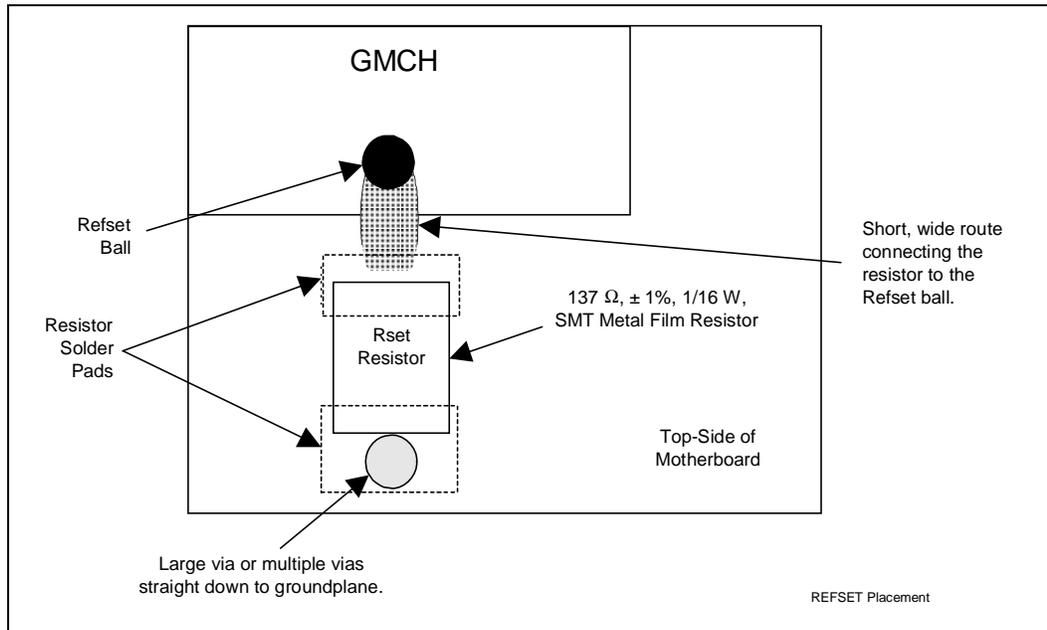
The integrated graphics in the GMCH interfaces to an analog display via a RAMDAC. The RAMDAC is a subsection of the graphics controller display engine and consists of three identical 8-bit digital-to-analog converter (DAC) channels: one for each red, green, and blue display electron gun.

Each RGB output is doubly terminated with a 75 Ω resistance: One 75 Ω resistance is connected from the DAC output to the board ground, and the other termination resistance exists within the display. The equivalent DC resistance at the output of each DAC is 37.5 Ω . The current output from each DAC flows into this equivalent resistive load to produce a video voltage without the need for external buffering. There is also a CLC pi-filter on each channel that is used to reduce high-frequency noise and to reduce EMI. To maximize the performance, the filter impedance, cable impedance, and load impedance should be matched.

Because the GMCH DAC runs at speeds up to 350 MHz, special attention should be paid to signal integrity and EMI. RGB routing, component placement, component selection, and cable and load impedance (monitor) all play a large role in the analog display's quality and robustness. This holds true for all resolutions, but especially for those at 1600x1200 or higher.

8.1.2 **Reference Resistor (REFSET)**

A reference resistor of 137 Ω is used to set the reference current for the RAMDAC. This resistor is an external resistor with a $\pm 1\%$ tolerance that is placed on the circuit board.

Figure 104. REFSET Placement


8.1.3 RAMDAC Board Design Guidelines

For the DAC to successfully run at speeds up to 350 MHz, care should be taken when routing the analog RAMDAC signals. A variety of routing options are available. Be sure to thoroughly validate any DAC routing design you choose. If routed differentially, each analog RGB signal should be routed differentially with its complement R#, G#, or B# signal. A pair (i.e., red and red#) should be routed 75 Ω odd-mode differential. For the assumed stack-up, this equates to ~8 mil trace for both traces with as little space (~5 mils) between the pair as possible. Spacing between pairs and to other signals should be maximized, – 20 mil spacing is recommended. The RGB signals should utilize pi filters placed near the VGA connector. An example pi-filter consists of two 3.3 pF capacitors with a 75 Ω @ 100 MHz FB between them. Prior to hitting this filter, the RGB signals should have a 75 Ω 1% terminating pull-down resistor. If routed differentially, the complement signals (R#, G# and B#) do not require a pi filter, and should be terminated with a ~37.5 Ω ± 1% resistor to ground.

If routed differentially, each analog signal should be matched to its complement as closely as possible. This includes the routing channel for each signal, as well as the loading on that signal. To have the complements' loading and edge rates more closely resemble that of the RGB signals, the complements may have a capacitor across their terminating resistors to mimic the pi filter. Also, the three pairs (R/R# combined) should closely resemble each other. If possible, try to match bends in one pair to the other two.

If routed differentially, signals within a pair should be routed with 5 mil spacing for as long a length as possible. To accomplish this, it is recommended that the pi filter and terminating resistors be placed as close as possible to the VGA connector. The complement signals should terminate through their 37.5 Ω resistors at the same location that the RGB signals hit their 75 Ω terminating resistors. After hitting their 75 Ω terminating resistors, the RGB signals should

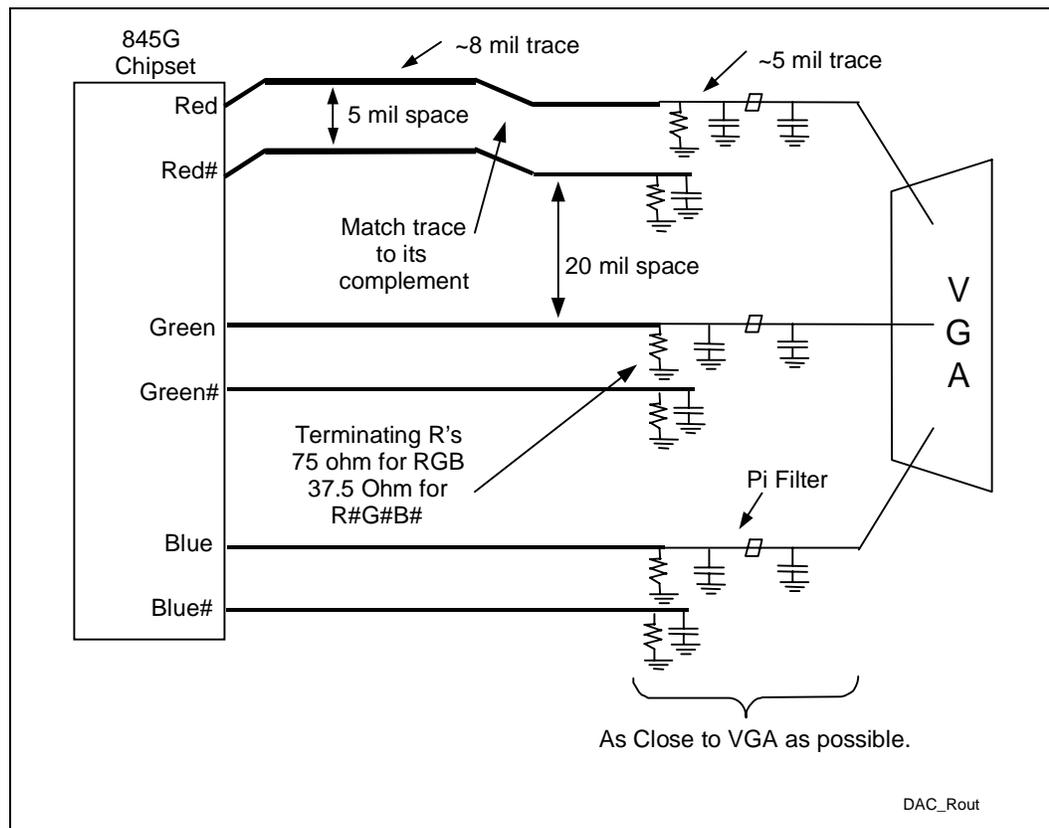
continue on to their pi filters and the VGA connector, *but should now ideally be routed with 75 Ω impedance (~ 5 mil traces).*

If single-ended routing is desired, the RGB traces should be routed 5 mils wide all the way from the GMCH, through the pi-filter, to the VGA connector. The complement signals (R#, G#, and B#) should be terminated to ground with as little trace as possible. Terminating resistors are not needed on the #'s if routing the RGB single-ended. In this scenario, the RGB signals should be routed 5 mils wide with at least 20 mil spacing. Termination and pi-filter recommendations for the RGB signals are identical to those mentioned above. Namely, they should have a 75 $\Omega \pm 1\%$ termination resistor, followed by the pi-filter as close as possible.

Regardless of routing preference, the RGB signals also require protection diodes between 1.5 V and ground. These diodes should have low C ratings (~5 pF max) and small leakage current (~ 10 μ A @ 120 $^{\circ}$ C), and should be properly decoupled with a 0.1 μ F cap. These diodes and decoupling should be placed to minimize power rail inductance. To have the complements' loading more closely resemble that of the RGB signals, the complements may have similar diodes. The choice between diodes (or diode packs) should be based on the recommended electrical characteristics and cost.

The RGB signals should be length matched as closely as possible (from GMCH to VGA connector), and should not exceed 200 mils of mismatch.

Figure 105. Generic DAC Routing — Differential Style



NOTE: This figure does not show the recommended diodes.

8.1.4 DAC Power Requirements

The DAC requires a 1.5 V supply through its two VCCA_DAC balls. The two may share a set of capacitors, 0.1 μF and 0.01 μF , but this connection should have low inductance. This supply should be connected directly to the main 1.5 V plane – it should **not** be connected to 1.5 V through an LC filter (like DPLL). Separate analog power or ground planes are not required for the DAC.

However, because the DAC is an analog circuit, it is particularly sensitive to AC noise seen on its power rail. Designs should provide as clean and quiet a supply as possible to the VCCA_DAC. Additional filtering and/or separate voltage rail may be needed to do so. Refer to the *Intel[®] 845G/845GL Chipset Datasheet* for AC and DC specifications for this supply.

8.1.5 Sync and DDCA Considerations

HSYNC and VSYNC should have $\sim 50 \Omega$ 5% series resistors on them. These are 3.3 V outputs from the GMCH. If higher signaling voltages are needed (5 V), level-shifting devices are required. DDCA_Data and DDCA_Clk should be connected to the analog display attached to the DAC.

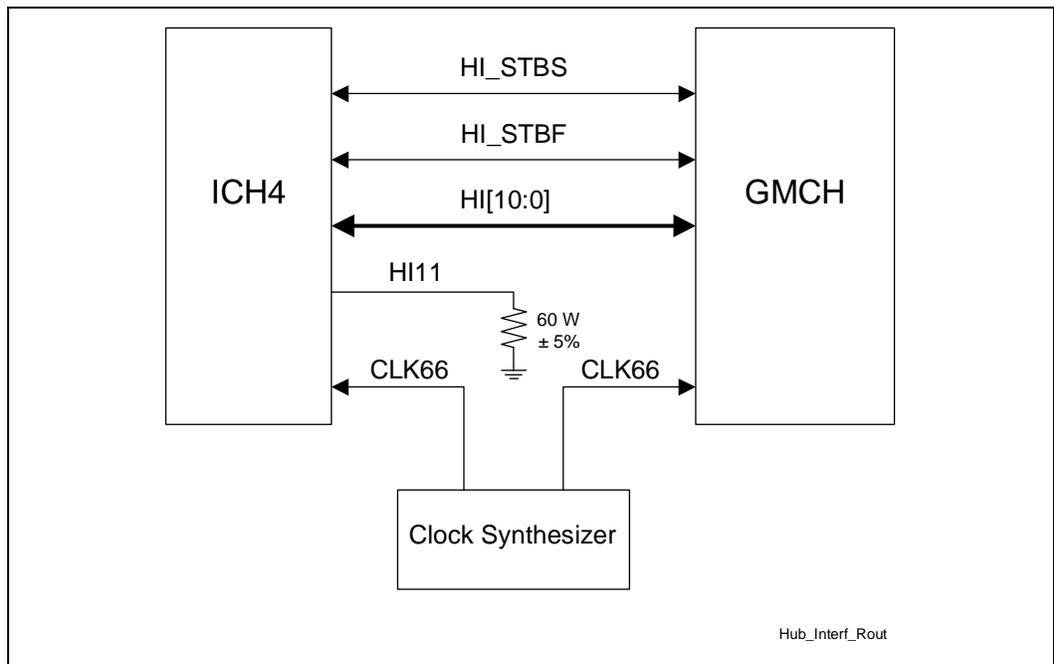
4.7 k Ω pull-ups (or pull-ups with the appropriate value derived from simulation) are required on each of these signals. These signals are 3.3 V tolerant. If higher signaling voltages are needed (5 V), level-shifting devices are required.

9 Hub Interface

The GMCH and ICH4 ballout assignments have been optimized to simplify the Hub Interface routing between these devices. It is recommended that the Hub Interface signals be routed directly from the GMCH to ICH4, with all signals referenced to VSS. Layer transition should be kept to a minimum. If a layer change is required, use only two vias per net, and keep all data signals and associated strobe signal on the same layer.

The Hub Interface signals are broken into two groups: data signals (HI), and strobe signals (HI_STB). For the 8-bit hub interface, HI[10:0] are associated with HI_STBS and HI_STBF.

Figure 106. Hub Interface Routing Example



9.1 Hub Interface Routing Guidelines

This section documents the routing guidelines for the Hub Interface. This Hub Interface connects the ICH4 to the GMCH. The ICH4 should strap its HICOMP pin to $V_{CCHI}=1.5\text{ V}$. The trace impedance must equal $60\ \Omega \pm 15\%$.

9.1.1 Hub Interface Strobe Signals

The Hub Interface strobe signals should be routed 5 mils wide with 15 mils trace spacing (5 on 15). This strobe pair should have a minimum of 20 mils spacing from any adjacent signals. The maximum length for the strobe signals is 2" to 8". The length between two strobes must be matched within ± 100 mil. Additionally, each data signal must be matched within ± 100 mils of the strobe signals. To break out of the GMCH and ICH4 package, the Hub Interface strobe signals can be routed 5 on 5 within 300 mils of the package.

9.1.2 Hub Interface Data Signals

The Hub Interface data signal traces should be routed 5 mils wide with 15 mils trace spacing (5 on 15). To break out of the GMCH and ICH4 package, the Hub Interface data signals can be routed 5 on 5 within 300 mils of the package.

The maximum Hub Interface data signal trace length is 2" to 8". Each data signal must be matched within ± 100 mils of the HI_STBF/HI_STBS pair.

9.1.3 Hub Interface Signal Referencing

The hub interface signal traces (HI[10:0]) and the two hub interface strobe signals (HI_STBS and HI_STBF) must all be referenced to ground to insure proper noise immunity.

9.1.4 Hub Interface HI_REF/HI_SWING Generation/Distribution

HI_REF is the Hub Interface reference voltage. The ICH4 uses HI_SWING to control voltage swing and impedance strength of the hub interface buffers. The HI_REF and HI_SWING voltage requirement and associated resistor/capacitor recommendations for the voltage divider circuit are listed in Table 64.

Table 64. Hub Interface HI_REF/HI_SWING Generation Circuit Specifications

HI_REF Voltage Specification	HI_SWING Voltage Specification	Recommended Values for the HI_REF / HI_SWING Divider Circuit
350mV \pm 2% at 1.5 V nominal	700mV \pm 2% at 1.5 V nominal	R1 = 226 Ω \pm 1%, R2 = R3 = 100 Ω \pm 1% C2 and C5 = 0.1 μ F C1, C3, C4, and C6 = 0.01 μ F

The resistor values, R1, R2, and R3, must be rated at 1% tolerance. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. Two 0.1 μ F capacitors (C2, C5) should be placed close the divider. In addition, the 0.01 μ F bypass capacitors (C1, C3, C4, C6) should be placed within 0.25" of the component HI_REF/VREF pin (for C3 and C4) and HI_SWING pin (for C1 and C6). The max distance from divider to device is 4" (less is better). Normal care must be taken to minimize crosstalk to other signals (< 10–15 mV). If the single HI_REF/HI_SWING divider circuit is located more than 4 inches away, the locally generated reference divider should be used.

Figure 107 shows an example of the HI_REF/HI_SWING divider circuit.

Figure 107. Hub Interface Single HI_REF/HI_SWING Generation Circuit

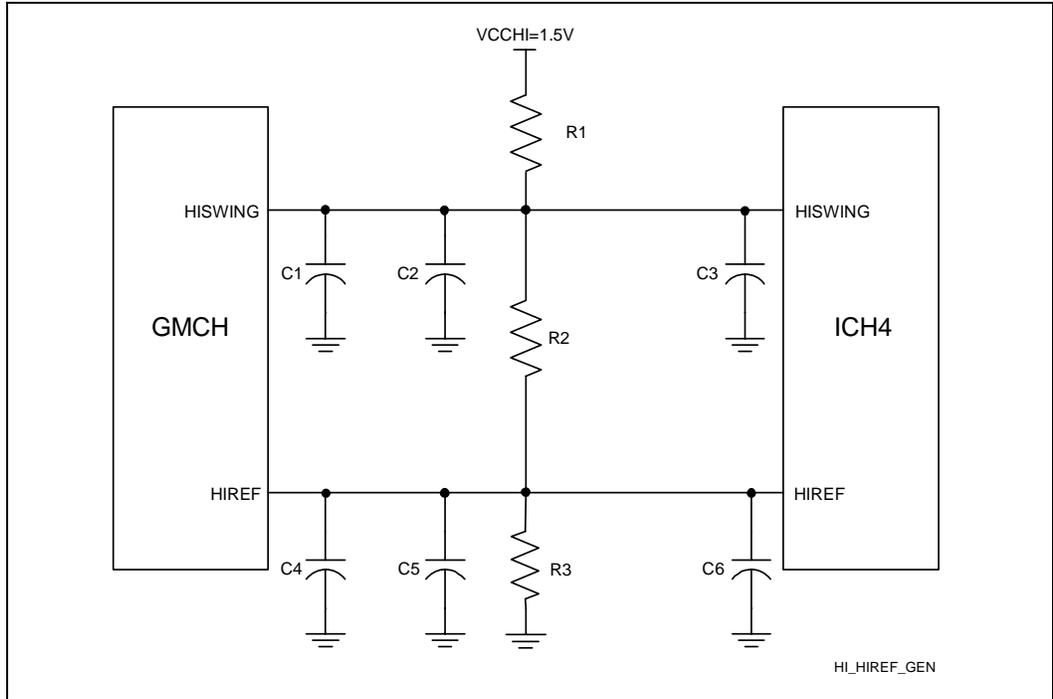
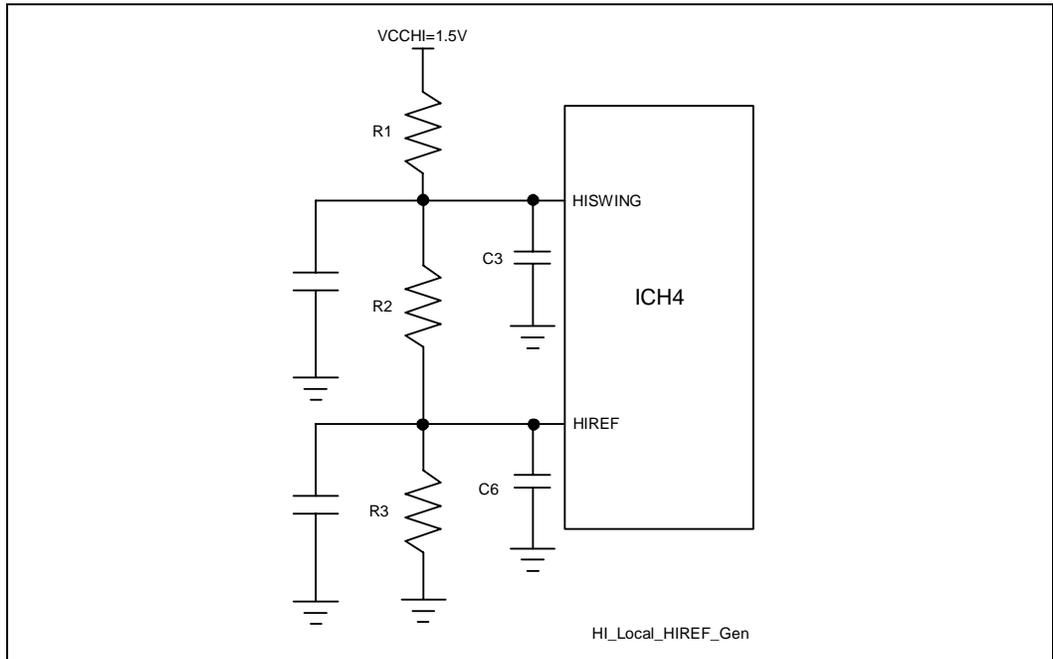


Figure 108. Hub Interface Local HI_REF/HI_SWING Generation Circuit (Intel® ICH4 side)



9.1.5 Hub Interface Compensation

The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The hub interface requires Resistive Compensation (HICOMP).

Table 65. Hub Interface HICOMP Resistor Values

Trace Impedance	HICOMP Calculation	HICOMP Resistor Value	HICOMP Resistor Tied To
60 Ω ± 15%	$[(1.5 - 0.7) / (0.7)] * 60$	68.1 Ω ± 1%	VCCHI = 1.5 V

9.1.6 Hub Interface Decoupling Guidelines

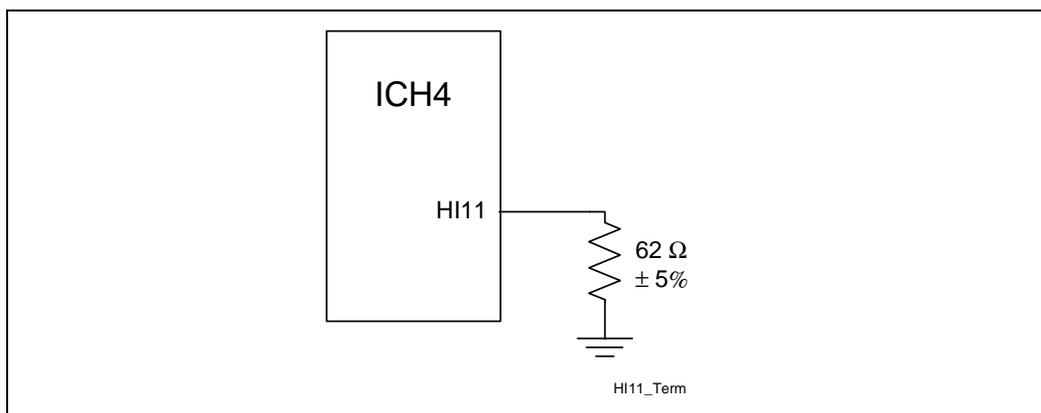
To improve I/O power delivery, use two 0.1 μF capacitors per each component (i.e., the ICH4 and GMCH). These capacitors should be placed within 100 mils from each package, adjacent to the rows that contain the Hub Interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCCHI=1.5 V side of the capacitors to the VCCHI=1.5 V power pins. Similarly, if layout allows, metal fingers running on the VCCHI=1.5 V side of the board should connect the ground side of the capacitors to the VSS power pins.

9.2 Additional Considerations

9.2.1 Hub Interface Intel® ICH4 Signals

The hub interface signal HI[11] is an ICH4 only signal and does not exist on the GMCH. This ICH4 signal should be terminated to VSS through a 62 Ω ± 5% resistor.

Figure 109. Intel® ICH4 HI11 Termination



10 Intel® ICH4

10.1 IDE Interface

This section contains guidelines for connecting and routing the ICH4 IDE interface. The ICH4 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH4 has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors may be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5 mil traces on 7 mil spaces and must be less than 8 inches long (from ICH4 to IDE connector). Additionally, the maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inches.

Table 66. IDE Routing Summary

Trace Impedance	IDE Routing Requirements	Maximum Trace Length	IDE Signal Length Matching
51 Ω to 69 Ω , 60 Ω Target	5 on 7	8"	No more than 0.5" (500 mils) between the shortest data signal and the longest strobe signal of a channel.

10.1.1 Cabling

Length of cable: Each IDE cable must be equal to or less than 18 inches.

Capacitance: Less than 35 pF.

Placement: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (6" away from the end of the cable).

Grounding: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

10.1.1.1 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH4 IDE Controller supports PIO, Multi-word (8237 style) DMA, and Ultra DMA modes 0 through 5, and Native Mode IDE. Note that there are no motherboard hardware requirements for supporting Native Mode IDE. Native Mode IDE is supported through the operating system and system driver. The ICH4 must determine the type of cable that is present to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra ATA/66 and Ultra ATA/100. This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector).

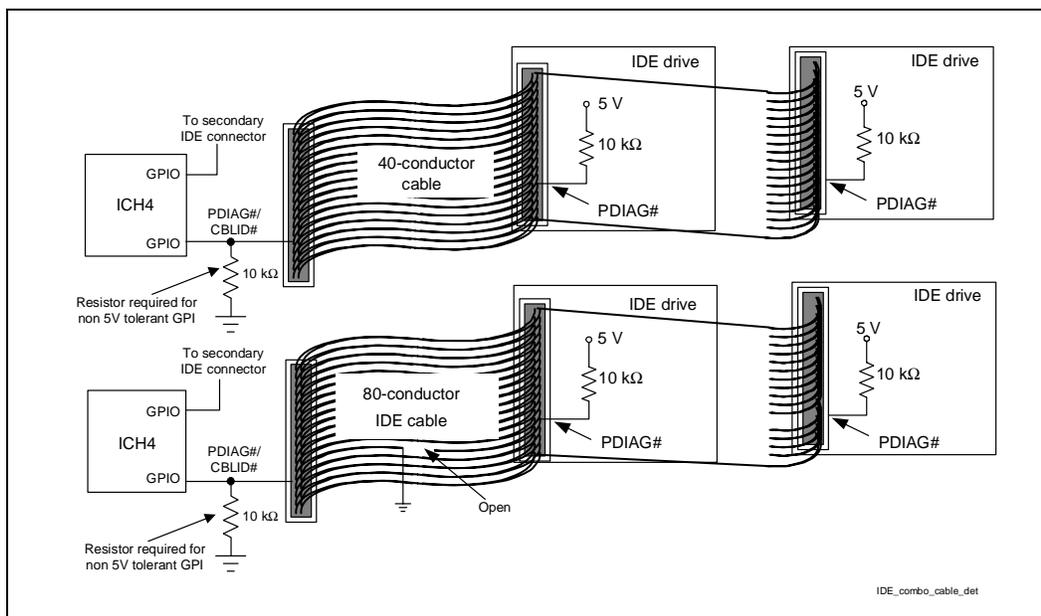
To determine if Ultra DMA modes greater than 2 (Ultra ATA/33) can be enabled, the ICH4 requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be done using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system because this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side Detection mechanism only.

10.1.1.2 Combination Host-Side/Device-Side Cable Detection

Host side detection (described in the *ATA/ATAPI-6 Standard*) requires the use of two GPIO pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 110. All IDE devices have a 10 K Ω pull-up resistor to 5 V on this signal. A 10 K Ω pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present, and allows for use of a non-5 V tolerant GPIO.

Figure 110. Combination Host-Side/Device-Side IDE Cable Detection



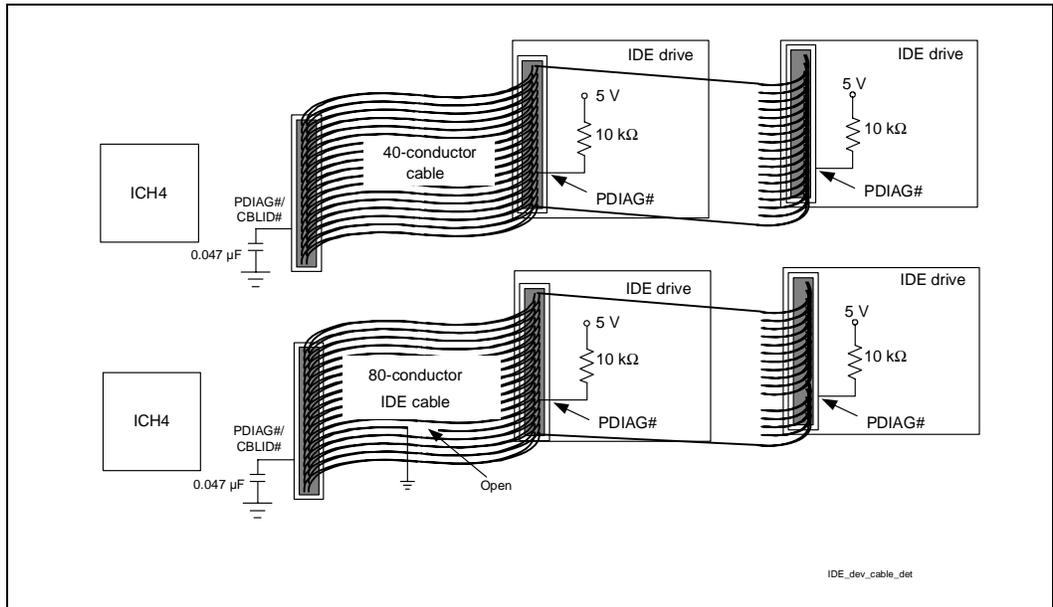
This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high, there is 40-conductor cable in the system, and Ultra DMA modes greater than 2 must not be enabled.

If PDIAG#/CBLID# is detected low, there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the *ATA/ATAPI-6 Standard*. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13 is a 1, an 80-conductor cable is present. If this bit is 0, a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present and should notify the user of the problem.

10.1.1.3 Device-Side Cable Detection

For platforms that must implement Device-Side detection only (e.g., NLX platforms), a 0.047 μF capacitor is required on the motherboard as shown in Figure 111. This capacitor should not be populated when implementing the previously-described recommended combination Host-Side/Device-Side cable detection mechanism. Note that some drives may not support device-side cable detection.

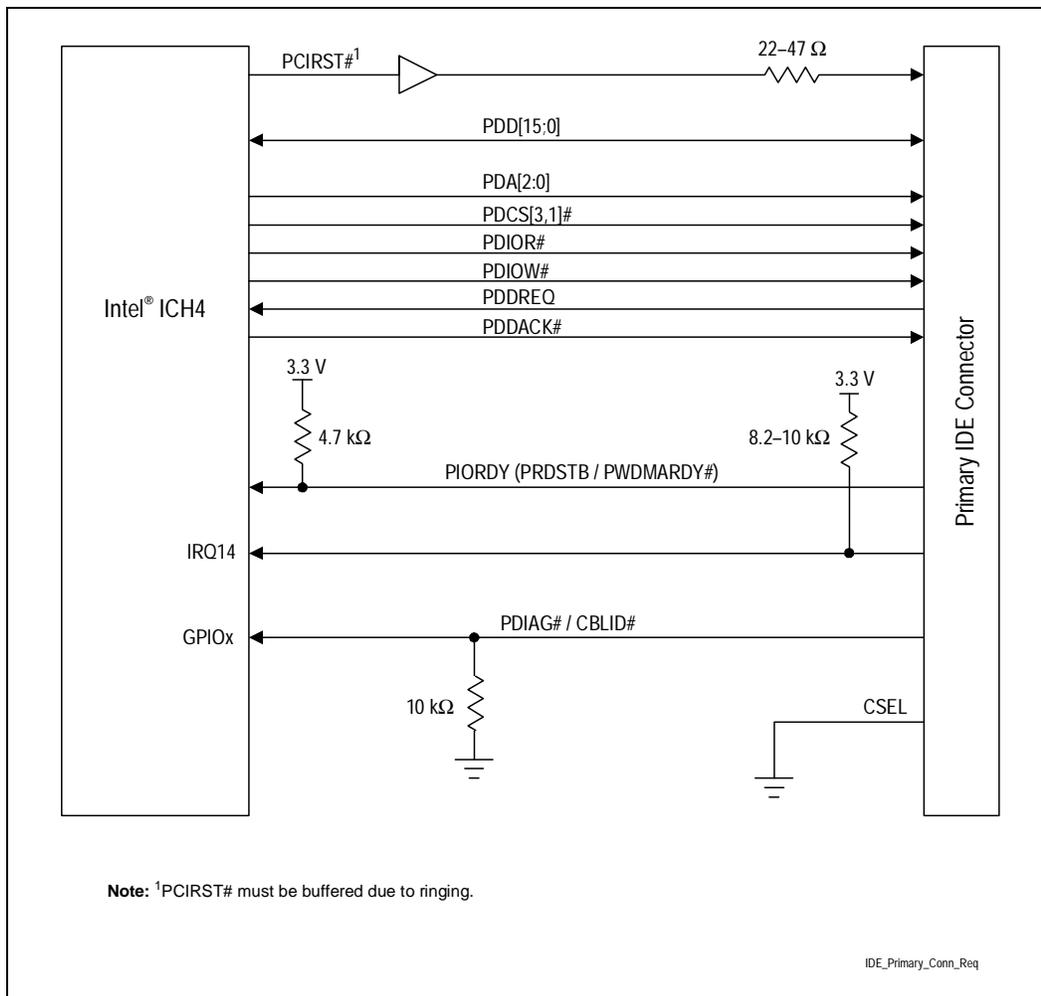
Figure 111. Device Side IDE Cable Detection



This mechanism creates a resistor-capacitor (RC) time constant. Drives supporting Ultra DMA modes greater than 2 (Ultra DMA/33) will drive PDIAG#/CBLID# low then release it (pulled up through a 10 k Ω resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host. Therefore, the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host. Therefore, the signal will rise more slowly as the capacitor charges. The drive can detect the difference in rise times, and will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot, as described in the *ATA/ATAPI-6 Standard*.

10.1.2 Primary IDE Connector Requirements

Figure 112. Connection Requirements for Primary IDE Connector

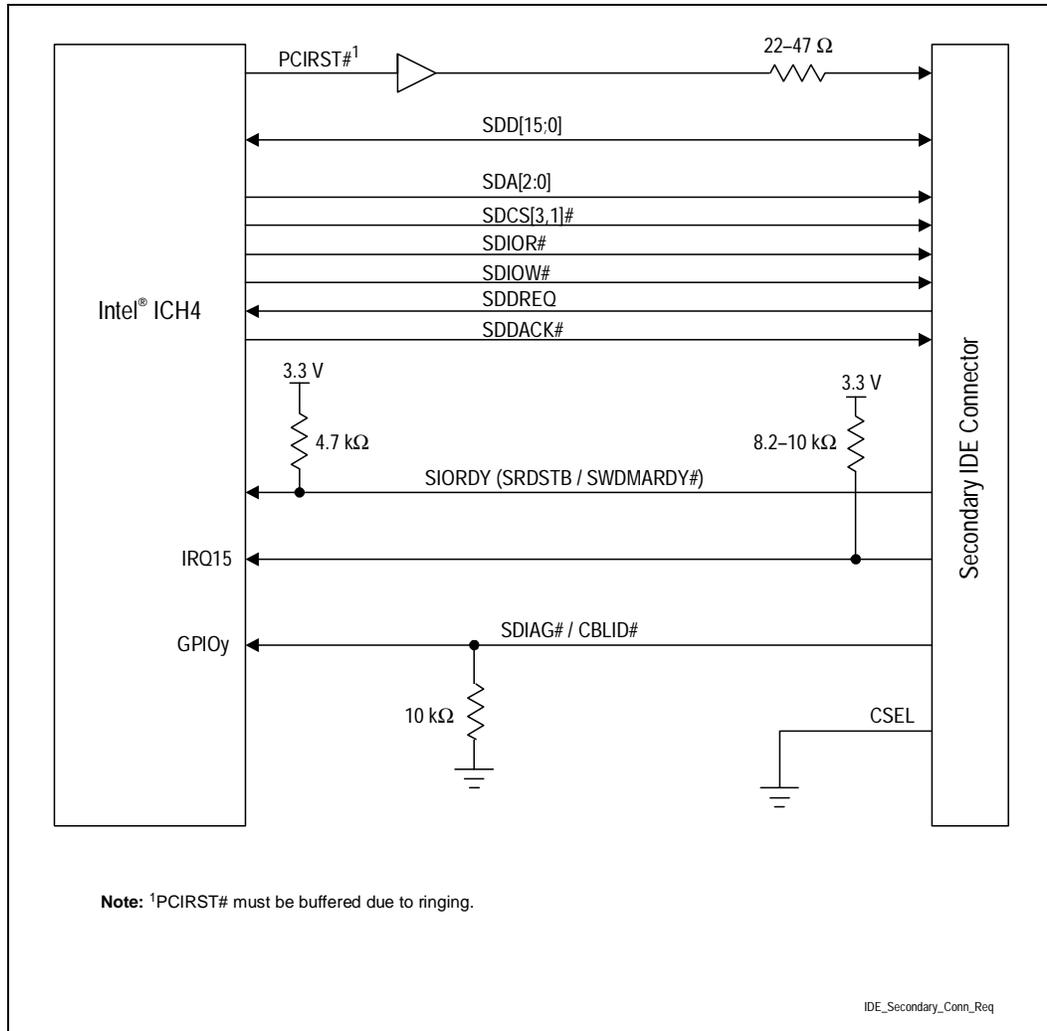


NOTES:

1. 22 kΩ – 47 kΩ series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2 kΩ – 10 kΩ pull-up resistor is required on IRQ14 to VCC3_3.
3. A 4.7 kΩ pull-up resistor to VCC3_3 is required on PIORDY.
4. Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
5. The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is required on the primary connector. This change is to prevent the GPIO pin from floating if a device is not present on the IDE interface.

10.1.3 Secondary IDE Connector Requirements

Figure 113. Connection Requirements for Secondary IDE Connector



NOTES:

1. 22 kΩ – 47 kΩ series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2 kΩ – 10 kΩ pull-up resistor is required on IRQ15 to VCC3_3.
3. A 4.7 kΩ pull-up resistor to VCC3_3 is required on SIORDY.
4. Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
5. The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is required on the secondary connector. This change is to prevent the GPIO pin from floating if a device is not present on the IDE interface.

10.2 AC'97

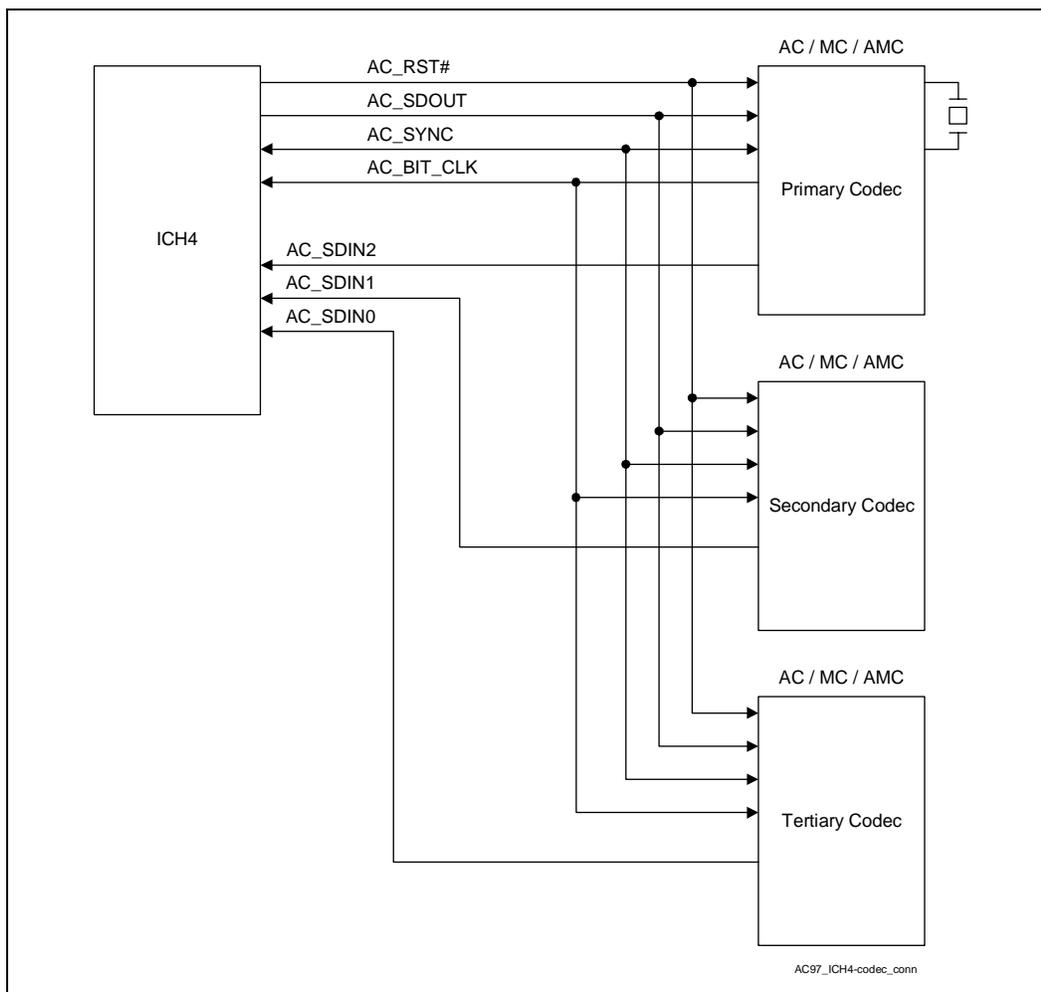
The ICH4 implements an AC'97 2.3 compatible digital controller. Contact your codec IHV (Independent Hardware Vendor) for information on AC'97 2.3 compliant products. The AC'97 2.3 specification is on the Intel website:

<http://developer.intel.com/ial/scalableplatforms/audio/index.htm#97spec>

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH4 AC-link allows a maximum of three codecs to be connected.

Figure 114 shows a three-codec topology of the AC-link for the ICH4.

Figure 114. Intel® ICH4 AC'97 — Codec Connection



NOTE: If a modem codec is configured as the primary AC-link Codec, there should not be any Audio Codecs residing on the AC-link. The primary codec must be connected to AC_SDIN2 if also routing to CNR. If no CNR exists on the platform, the primary codec may be connected to AC_SDIN0 as documented in the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*.

Using the assumed 4-layer stack-up, the AC'97 interface can be routed using 5 mil traces with 5 mil spacing between the traces. Maximum length between ICH4 to down CODEC is 14". Maximum length between ICH4 to CNR is 14". This assumes that a CNR riser card implements its audio solution with a maximum trace length of 6" for the AC-link. Trace impedance should

be

$$Z_0 = 60 \Omega \pm 15\%.$$

Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH4), and to any other codec present. That clock is used as the time base for latching and driving data. **Clocking AC_BIT_CLK directly from the CK408 14.31818 MHz clock is not supported.**

The ICH4 supports wake on ring from S1–S5 via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH4 has weak pull-downs/pull-ups that are always enabled. This will keep the link from floating when the AC-link is off, and when there are no codecs present.

The Shut-off bit not set it implies that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOOUT will be driven by the codec and ICH4 respectively. However, AC_SDIN0, AC_SDIN1, and AC_SDIN2 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

Figure 115. Intel® ICH4 AC'97 — AC_BIT_CLK Topology

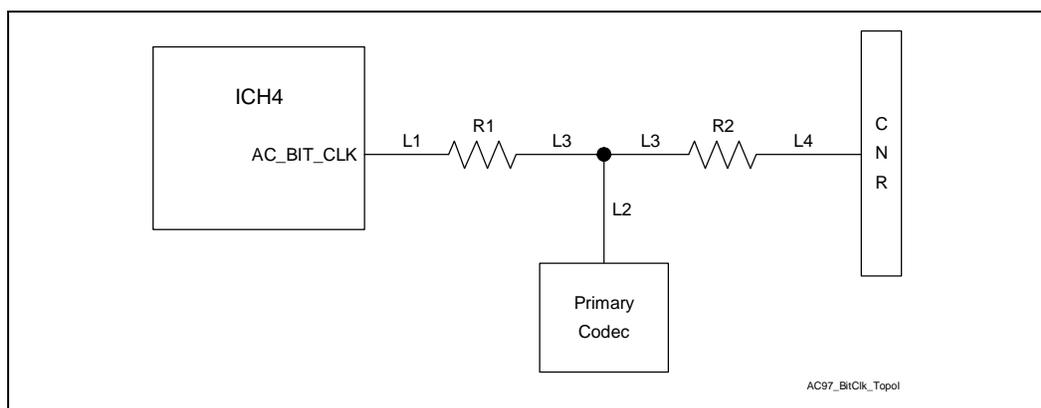


Table 67. AC'97 AC_BIT_CLK Clock Routing Summary

Trace Impedance	AC'97 Routing Requirements	Maximum Trace Length	Series Termination Resistance	AC_BIT_CLK Signal Length Matching
51 Ω to 69 Ω , 60 Ω Target	5 on 5	L1 = (1 to 8) – L3 inches L2 = (0.1 to 6) inches L3 = (0.1 to 0.4) inches L4 = (1 to 6) – L3 inches	R1 = 33 Ω - 47 Ω R2 = Optional 0 Ω resistor for debug purposes	N/A

NOTES:

1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec is used, a 33 Ω resistor is best for R1; and if the CS4205b codec is used, a 47 Ω resistor for R1 is best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel 9750 codec

Figure 116. Intel® ICH4 AC'97 — AC_SDOOUT/AC_SYNC Topology

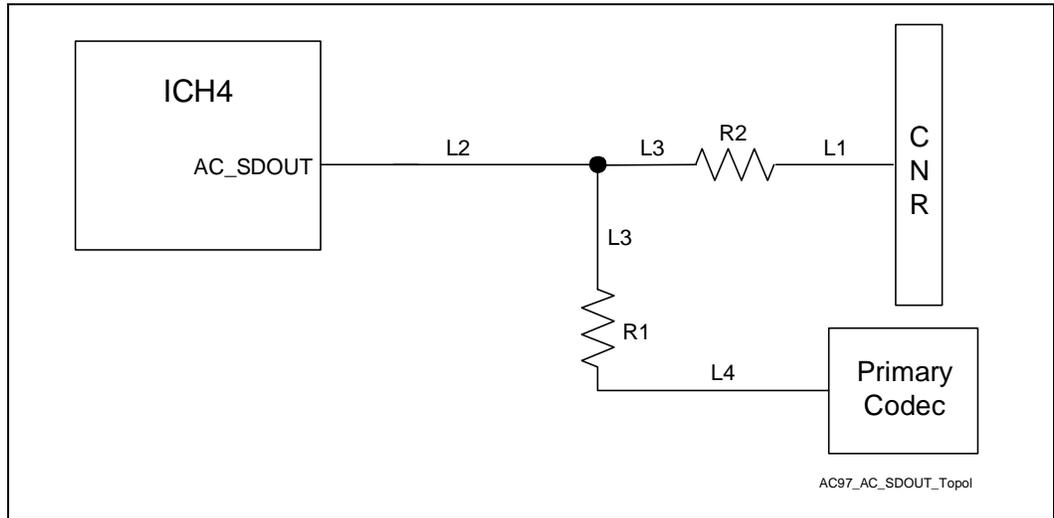


Table 68. AC'97 AC_SDOOUT/AC_SYNC Routing Summary

Trace Impedance	AC'97 Routing Requirements	Maximum Trace Length	Series Termination Resistance	AC_SDOOUT/AC_SYNC Signal Length Matching
51 Ω – 69 Ω , 60 Ω Target	5 on 5	L1 = (1 to 6) – L3 inches L2 = (1 to 8) inches L3 = (0.1 to 0.4) inches L4 = (0.1 to 6) – L3 inches	R1 = 33 Ω – 47 Ω R2 = R1 if the CNR card that will be used with the platform does not have a series termination resistor on the card. Otherwise, R2 = 0 Ω	N/A

NOTES:

1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec is used, a 33 Ω resistor is best for R1; and if the CS4205b codec is used, a 47 Ω resistor for R1 is best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel 9750 codec

Figure 117. Intel® ICH4 AC'97 — AC_SDIN Topology

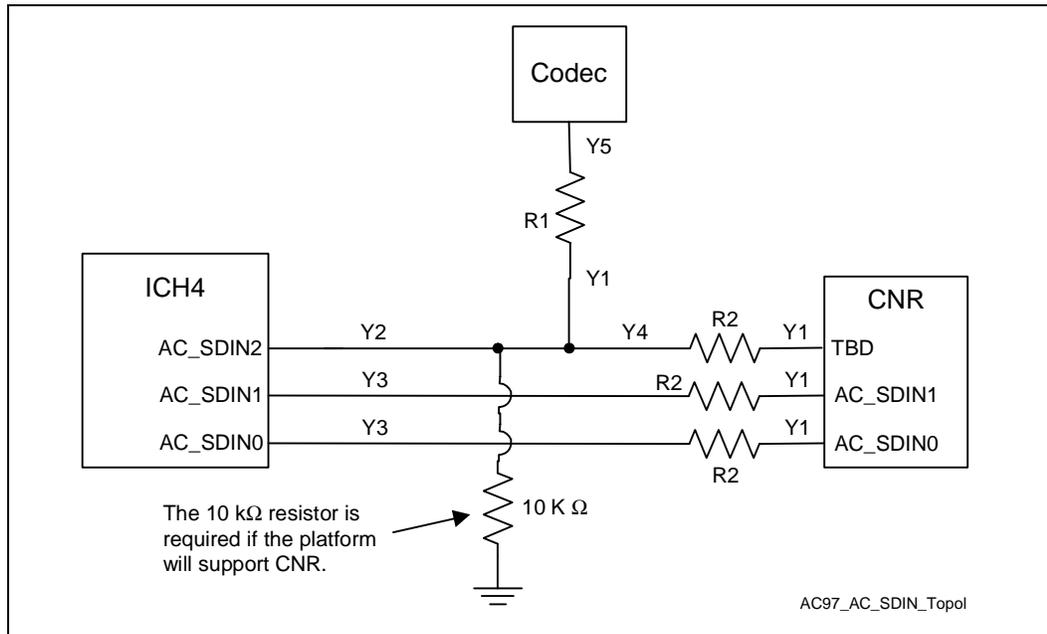


Table 69. AC'97 AC_SDIN Routing Summary

Trace Impedance	AC'97 Routing Requirements	Maximum Trace Length	Series Termination Resistance	AC_SDIN Signal Length Matching
50 Ω – 69 Ω, 60 Ω Target	5 on 5	Y1 = (0.1 to 0.4) inches Y2 = (1 to 8) – Y1 inches Y3 = (1 to 14) – Y1 inches Y4 = (1 to 6) – Y1 inches Y5 = (0.1 to 6) – Y1 inches	R1 = 33 Ω – 47 Ω R2 = R1 if the CNR card that will be used with the platform does not have a series termination resistor on the card. Otherwise, R2 = 0 Ω	N/A

NOTES:

1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec is used, a 33 Ω resistor is best for R1; and if the CS4205b codec is used, a 47 Ω resistor for R1 is best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel 9750 codec

10.2.1 AC'97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area, and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

10.2.2 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH4 platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but are based on the ICH4 platform.

- Active Components such as FET switches, buffers and logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so potentially interferes with timing margins and signal integrity.
- The ICH4 supports wake-on-ring from S1–S5 states via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

10.2.2.1 Valid Codec Configurations

Table 70. Codec Configurations

Option	Primary Codec	Secondary Codec	Tertiary Codec
1	Audio	Audio	Audio
2	Audio	Audio	Modem
3	Audio	Audio	Audio / Modem
4	Audio	Modem	Audio
5	Audio	Audio / Modem	Audio
6	Audio / Modem	Audio	Audio

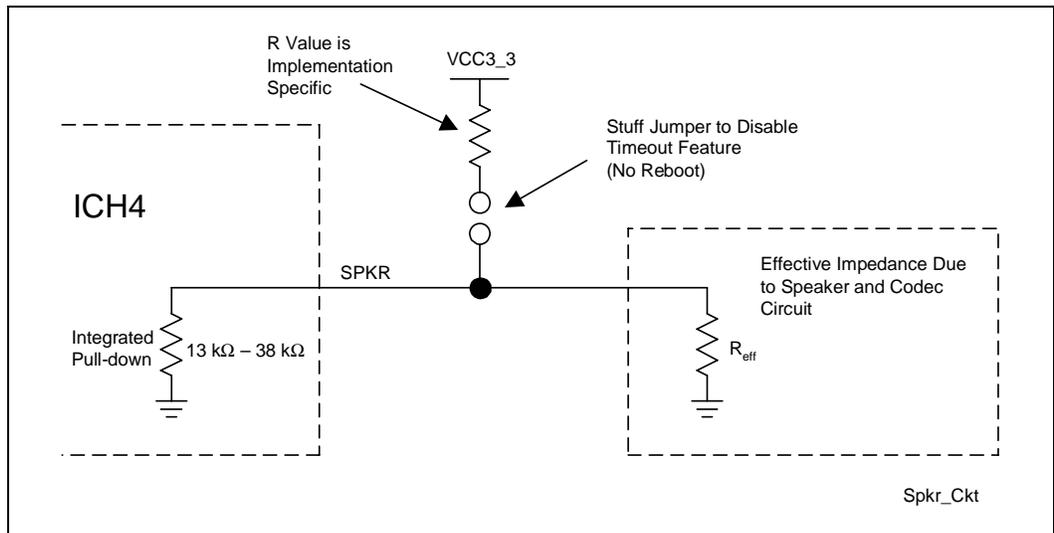
NOTES:

1. For power management reasons, codec power management registers are in audio space. As a result, if there is an audio codec in the system, it must be Primary.
2. There cannot be two modems in a system because there is only one set of modem DMA channels.
3. The ICH4 supports a modem codec on any of the AC_SDIN lines. However, the Modem Codec ID must be either 00 or 01.

10.2.3 SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker, and as a functional strap. The strap function enables or disables the “TCO Timer Reboot function” based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH4 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero, or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see Figure 118). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{eff}), and the ICH4 integrated pull-down resistor is read as logic high ($0.5 V_{CC3_3}$ to $V_{CC3_3} + 0.5 V$).

Figure 118. Example Speaker Circuit



10.3 CNR

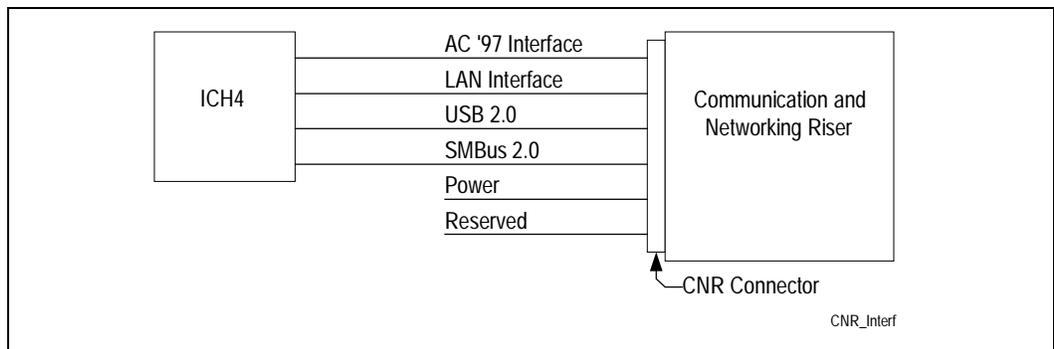
The Communication and Networking Riser (CNR) Specification defines a hardware scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. A related documents for CNR is:

- *Communication Network Riser Specification Revision 1.2*; Available at <http://developer.intel.com/technology/cnr>

This interface supports multi-channel audio, V.90 analog modem, phone-line based networking, 10/100 Ethernet based networking, *SMBus Interface Power Management Revision 1.1*, and USB 2.0. The CNR specification defines the interface, which should be configured prior to shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot. Therefore, the system designer will not sacrifice a PCI slot if he decides not to include a CNR in a particular build.

Figure 119 indicates the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. The Platform LAN connection (PLC) can be either an 82562ET/EZ or an 82562EM/EX component. Refer to the CNR specification for additional information.

Figure 119. CNR Interface



10.3.1 AC'97 Audio Codec Detect Circuit and Configuration Options

This section provides general circuits to implement a number of different codec configurations. Refer to the *Communication Network Riser Specification, Revision 1.2* for Intel's recommended codec configurations

Table 71. Signal Descriptions

CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC'97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC '97 Interface (held in reset) because the CNR codec(s) will be the primary device(s) on the AC '97 Interface.
AC_RST#	Reset signal from the AC '97 Digital Controller (ICH4).
AC_SDIN_n	AC '97 serial data from an AC '97-compatible t codec to an AC '97-compatible controller (i.e., the ICH4).

10.3.1.1 CNR 1.2 AC'97 Disable and Demotion Rules for the Motherboard

The following are the CNR1.1/1.2 AC '97 disable and demotion rules for the motherboard.

- All AC '97 Rev. 2.2 *non-chaining* Codecs on the motherboard **must always** disable themselves when the CDC_DWN_ENAB# signal is in a high state.
- A motherboard AC '97 Codec **must never** change its address or AC_SDIN line used, regardless of the state of the CDC_DWN_ENAB# signal.
- A motherboard containing an AC '97 Controller supporting three AC '97 Codecs, the AC '97 Rev. 2.2 or the AC'97 Rev. 2.3 Codec on the motherboard **must be** connected to the AC_SDIN2 signal of the CNR connector.
- A motherboard should not contain any more than a single AC '97 Codec.

These rules allow for forward and backward compatibility between CNR Version 1.1/1.2 cards. For more information on chaining, consult the *Communication Network Riser Specification Revision 1.2*.

Figure 120. Motherboard AC'97 CNR Implementation with a Single Codec Down On Board

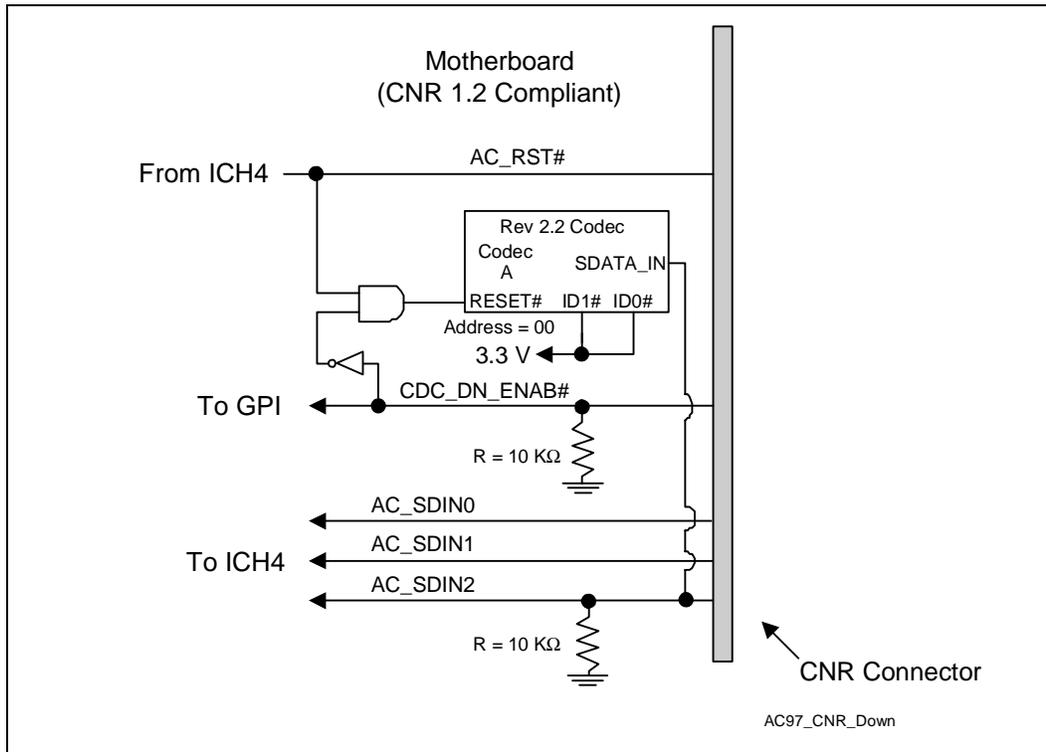
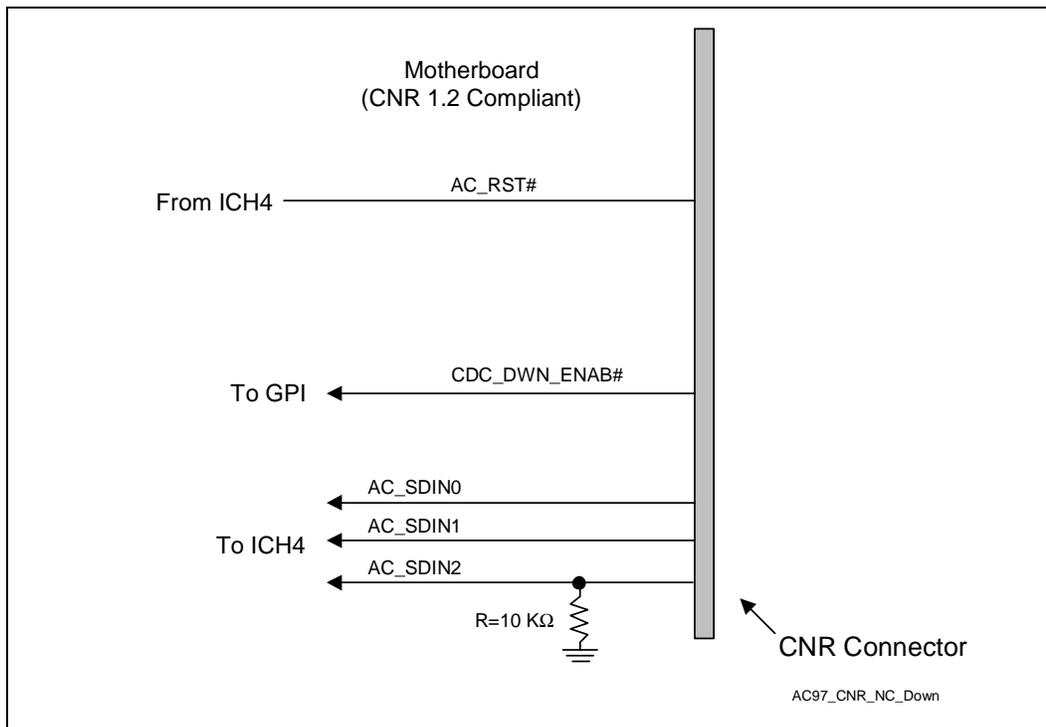


Figure 121. Motherboard AC'97 CNR Implementation with no Codec Down On Board



10.3.2 CNR Routing Summary

Table 72 is a summary of the various interfaces routing requirements to the CNR Riser.

Table 72. CNR Routing Summary

Trace Impedance	CNR Routing Requirements	Maximum Trace Length to CNR Connector	Signal Length Matching	Signal Referencing
77 Ω to 103 Ω Differential, 90 Ω Differential Target	USB (7.5 on 7.5) Data pair must be at least 20 mils from nearest neighbor	10"	No more than 150 mils trace mismatch	Ground
51 Ω to 69 Ω , 60 Ω Target	AC'97 (5 on 5)	AC_BIT_CLK (See Table 67) AC_SDOOUT (See Table 68) AC_SDIN (See Table 69)	N/A	Ground
51 Ω to 69 Ω , 60 Ω Target	LAN (5 on 10)	9.5" (See Table 84)	Equal to or up to 500 mils shorter than the LAN_CLK trace	Ground

10.4 USB 2.0

10.4.1 Layout Guidelines

10.4.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines help minimize signal quality and EMI problems. The USB 2.0 validation efforts focused on a four-layer motherboard in which the first plane is a signal layer, the second plane is power, the third plane is ground, and the fourth plane is a signal layer. This results in placing most of the routing on the fourth plane closest to the ground plane, allowing a higher component density on the first plane.

- Place the ICH4 and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs, and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
- USB 2.0 signals should be *ground referenced*.
- Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities. (See Figure 150.)
- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or IC's that use and/or duplicate clocks.
- Stubs on high speed USB signals should be avoided because stubs cause signal reflection and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils.
- Route all traces over continuous planes (VCC or GND) with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 10.4.2.
- Separate signal traces into similar categories, and route similar signal traces together (for example, rout differential pairs together).
- Keep USB 2.0 signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
- Follow the 20*h thumb rule by keeping traces at least 20* (height above the plane) away from the edge of the plane (VCC or GND, depending on which plane the trace is over. For the suggested stackup, the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the

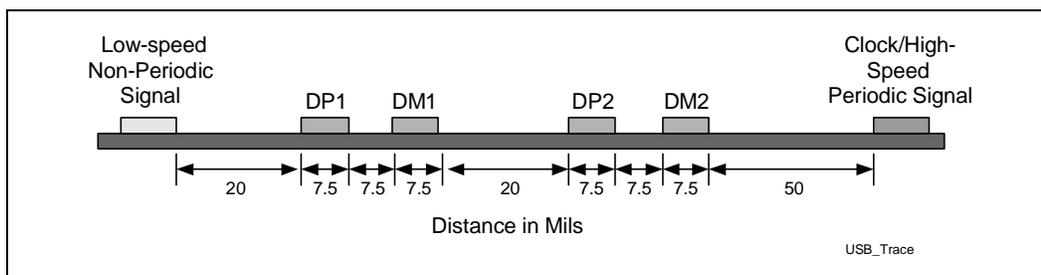
signal onto adjacent wires, and helps prevent free radiation of the signal from the edge of the PCB.

10.4.1.2 USB 2.0 Trace Separation

Use the following separation guidelines. Figure 122 shows the recommended trace spacing.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve $90\ \Omega$ differential impedance. Deviations normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.
- Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used. For the board stackup parameters referred to in Section 3.2, 7.5 mil traces with 7.5 mil spacing results in approximately $90\ \Omega$ differential trace impedance.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

Figure 122. Recommended USB Trace Spacing



10.4.1.3 USBRBIAS Connection

The USBRBIAS pin and the USBRBIAS# pin can be shorted and routed 5 on 5 to one end of a $22.6\ \Omega \pm 1\%$ resistor to ground. Place the resistor within 500 mils of the ICH4 and avoid routing next to clock pins.

Figure 123. USBRBIAS Connection

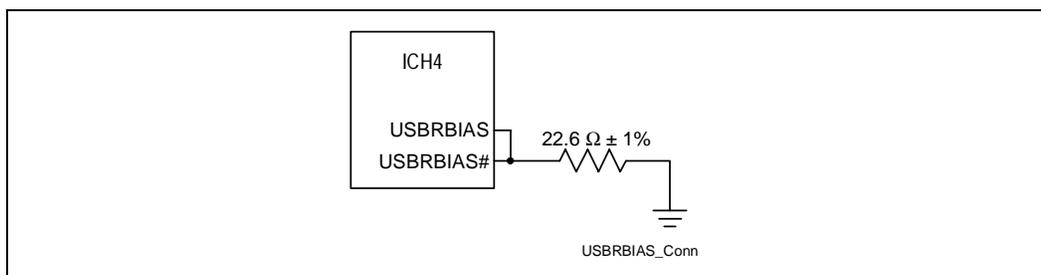


Table 73. USBRBIAS/USBRBIAS# Routing Summary

Trace Impedance	USBRBIAS/ USBRBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
51 Ω to 69 Ω , 60 Ω Target	5 on 5	500 mils	N/A	N/A

10.4.1.4 USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See Section 10.4.4 for common-mode choke details.

10.4.1.5 USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pair should be no greater that 150 mils.

10.4.1.6 USB 2.0 Trace Length Guidelines

Use the following trace length guidelines.

Table 74. USB 2.0 Trace Length Preliminary Guidelines (With Common-mode Choke)

Trace Imped.	USB 2.0 Routing Req.	Topology	Signal Ref.	Signal Matching	Motherboard Trace Length	Card Trace Length	Maximum Total Length																								
77 Ω to 103 Ω differential,	7.5 on 7.5	Back Panel	Ground	The max mismatch between data pairs should not be greater than 150 mils	17 inches	N/A	17 inches																								
		CNR			8 inches	6 inches	14 inches																								
90 Ω Differential Target		Front Panel			<table border="1"> <thead> <tr> <th>Cable Length</th> <th>Motherboard Trace Length</th> <th>Daughter Card Trace Length</th> <th>Max. Total Length</th> </tr> </thead> <tbody> <tr> <td>9</td> <td>6</td> <td>2</td> <td>17</td> </tr> <tr> <td>10.5</td> <td>5</td> <td>2</td> <td>17.5</td> </tr> <tr> <td>12</td> <td>4</td> <td>2</td> <td>18</td> </tr> <tr> <td>13.5</td> <td>3</td> <td>2</td> <td>18.5</td> </tr> <tr> <td>15</td> <td>2</td> <td>2</td> <td>19</td> </tr> </tbody> </table>	Cable Length	Motherboard Trace Length	Daughter Card Trace Length	Max. Total Length	9	6	2	17	10.5	5	2	17.5	12	4	2	18	13.5	3	2	18.5	15	2	2	19		
Cable Length	Motherboard Trace Length	Daughter Card Trace Length	Max. Total Length																												
9	6	2	17																												
10.5	5	2	17.5																												
12	4	2	18																												
13.5	3	2	18.5																												
15	2	2	19																												

NOTES:

- These lengths are based upon simulation results and may be updated in the future.
- All lengths are based upon using a common-mode choke (see Section 10.4.4.1 for details on common-mode choke).
- Numbers in this table are based on the following simulation assumptions:
CNR configuration — max 6 inches trace on add-on card.
- An Approximate 1:1 trade-off can be assumed from Motherboard Trace Length vs. Daughter card Trace Length (e.g., trade 1 inch of Daughter card for 1 inch of Motherboard Trace Lengths).
- Routing guidelines are based on the stackup assumptions in Section 3.2
- Numbers in this table are based on the following simulation assumptions
 - Trace length on front panel connector card assumed a max of 2 inches.
 - USB twisted-pair shielded cable as specified in USB 2.0 specification was used.
- For front panel solutions, signal matching is considered from the ICH4 to the front panel header.

10.4.2 Plane Splits, Voids and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cutouts.

10.4.2.1 VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the VCC plane.

- Traces should not cross anti-etch because this greatly increases the return path for the signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces, as well as slower signal traces that may be coupling to them. USB signaling is not purely differential in all speeds (i.e. the Full-speed Single Ended Zero is common mode).
- Avoid routing of USB 2.0 signals within 25-mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages, it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboards that use several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one and the other.

If crossing a plane split is completely unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 μ F or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates VCC5 and VCC3_3 planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to VCC5, and the other side should tie to VCC3_3. Stitching caps provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

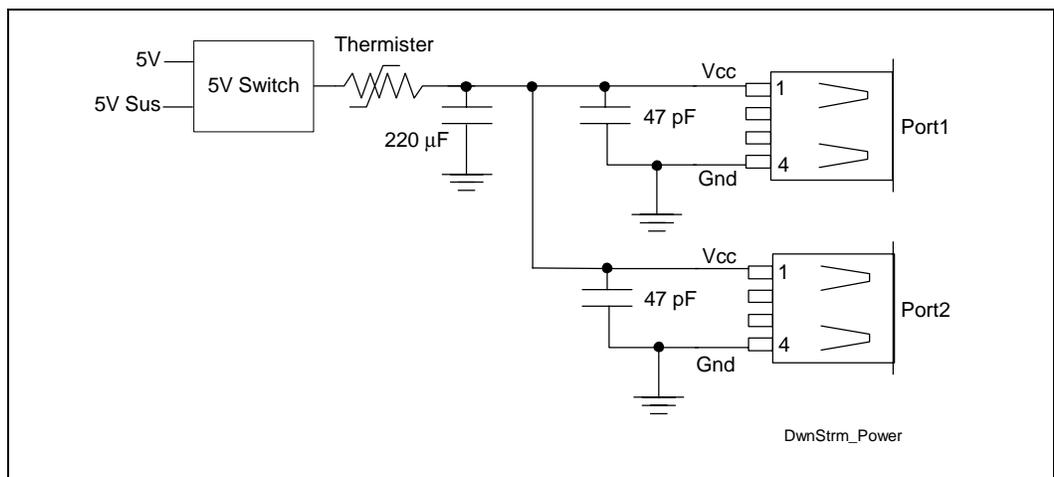
10.4.2.2 GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

10.4.3 USB Power Line Layout Topologies

The following is a suggested topology for power distribution of Vbus to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop), and dynamic detach flyback protection. These two different situations require both bulk capacitance (droop), and filtering capacitance (for dynamic detach flyback voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port, and the power-carrying traces should be as wide as possible, preferably a plane. A good “rule-of-thumb” is to make the power-carrying traces wide enough that the system fuse will blow during an over current event. If the system fuse is rated at 1 amps, the power-carrying traces should be wide enough to carry at least 1.5 amps.

Figure 124. Good Downstream Power Connection



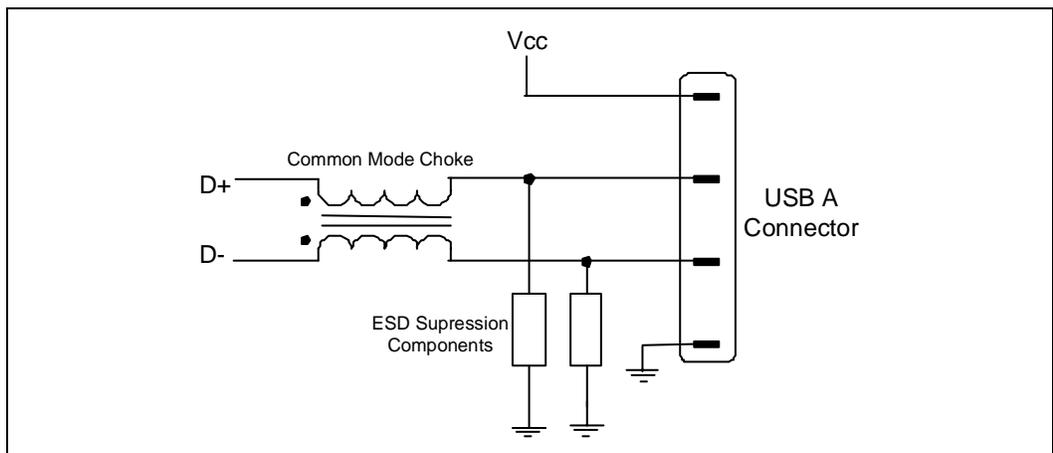
10.4.4 EMI Considerations

The following guidelines apply to the selection and placement of common chokes and ESD protection devices.

10.4.4.1 Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design should include a common mode choke footprint to provide a stuffing option *in the event* that the choke is needed to pass EMI testing. Figure 125 shows the schematic of a typical common mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins. In systems that route USB to a front panel header, the choke should be placed on the front panel card.

Figure 125. A Common-Mode Choke



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion increases, so the effects of the common mode choke on full-speed and high-speed signal quality should be tested. Common Mode Chokes with a target impedance of 80 to 90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process.

- A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen, and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
- Once you have a part that gives passing EMI results, test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for Low-speed, Full-speed and High-speed USB operation.

10.4.5 ESD

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 because of the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common mode choke and the USB connector data pins as shown in Figure 125. Other types of low-capacitance ESD protection devices may work as well, but were not investigated. As with the common mode choke solution, it is recommended that footprints for some type of ESD protection device be included as a stuffing option in case it is needed to pass ESD testing.

10.4.6 Front Panel Solutions

10.4.6.1 Internal USB Cables

The front panel internal cable solution chosen must meet all the requirements of Chapter 6 of the *USB 2.0 Specification* for high-/full-speed cabling for each port, with the exceptions described in the following Cable Option 2.

10.4.6.1.1 Internal Cable Option 1

Use standard High-Speed/Full-Speed compatible USB cables. These must meet all cabling requirements called out in Chapter 6 of the *USB 2.0 Specification*. Recommended motherboard mating connector pin-out is covered in detail later in this document.

10.4.6.1.2 Internal Cable Option 2

Use custom cables that meet all of the requirements of Chapter 6 of *the USB 2.0 Specification* with the following additions/exceptions:

- They can share a common jacket, shield, and drain wire.
- Two ports with signal pairs that share a common jacket may combine Vbus and ground wires into a single wire, provided the following conditions are met:
 - A.1 The bypass capacitance required by Section 7.2.4.1 of the USB 2.0 Specification is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughter card). Refer to the front panel daughter card referenced later for details.
 - A.2 Selecting proper wire size: A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the USB 2.0 Specification that has $\leq \frac{1}{2}$ the resistance of either of the two wires being combined. The data is provided for reference in Table 75.

Table 75. Conductor Resistance

American Wire Gauge (AWG)	Ohm (Ω) / 100 Meters Maximum
28	23.20
26	14.60
24	9.09
22	5.74
20	3.58

Example: 2 – 24 gauge (AWG) power or ground wires can be replaced with one 20-gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the USB 2.0 specification at the USB connectors, and at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure that the system passes droop requirements. Cables that provide individual power and ground conductors for each port can usually meet droop requirements by providing adequate capacitance near the motherboard mating connector because droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case, all transients will be seen/dampened by the capacitance at the motherboard mating connector before they can cause problems with the adjacent port sharing the same cable. See section 7.2.2 and 7.2.4.1 of *the USB 2.0 Specification* for more details.

Cables that contain more than two signal pairs are not recommended because of unpredictable impedance characteristics.

10.4.6.2 Motherboard/PCB Mating Connector

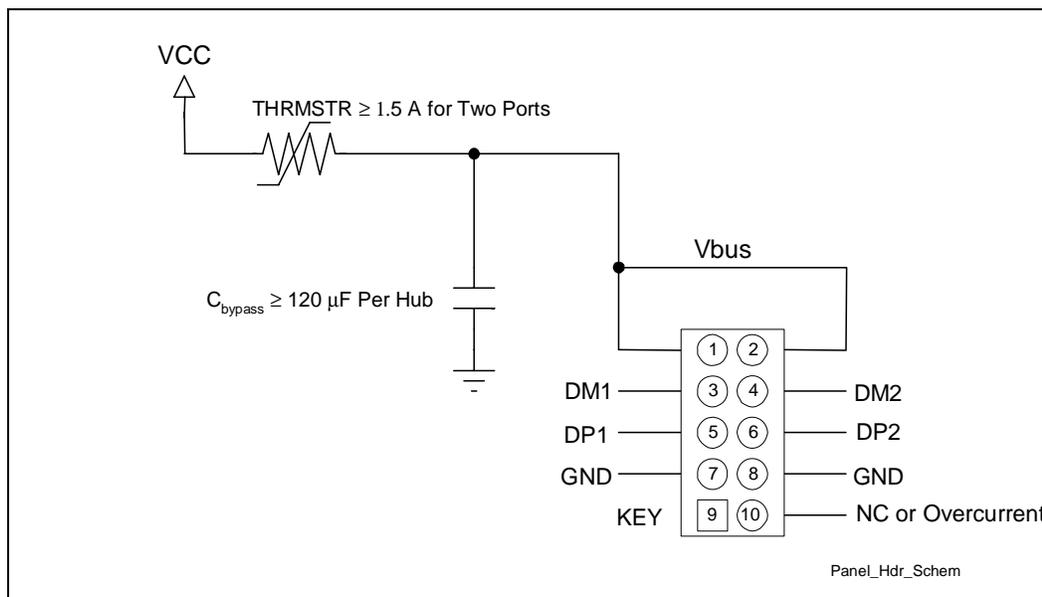
Proper selection of a motherboard mating connector for front panel USB support is important to ensure that signal quality is not adversely affected because of a poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the *USB 2.0 Specification*.

10.4.6.2.1 Pin-out

A ten pin, 0.1-inch pitch stake pin assembly is recommended with the pin-out listed in Table 76 and in the following schematic.

Table 76. Front Panel Header Pin-Out

Pin	Description
1	VCC
2	VCC
3	dm1
4	dm2
5	dp1
6	dp2
7	Gnd
8	Gnd
9	key
10	No connect or over-current sense.

Figure 126. Front Panel Header Schematic


It is **highly** recommended that the fuse element (thermistor) for the front panel header be included on the motherboard to protect the motherboard from damage.

- This protects the motherboard from damage in the case where an un-fused front panel cable solution is used.
- It also provides protection from damage if an un-keyed cable is inadvertently plugged onto the front panel USB connector.
- It provides protection to the motherboard in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between Vbus and ground.

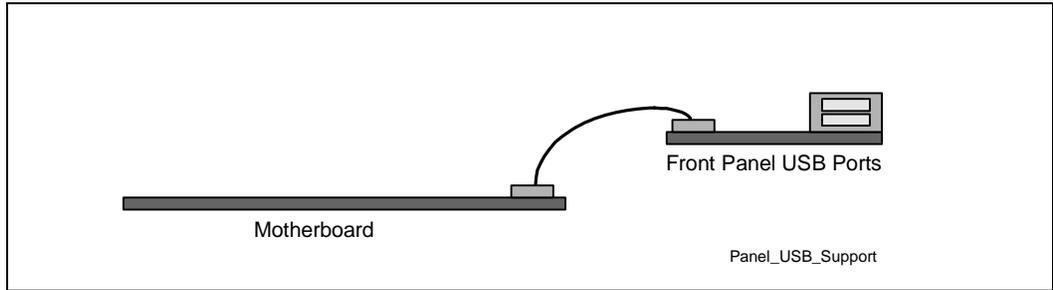
10.4.6.2.2 Routing Considerations

- Traces or surface shapes from VCC to the thermistor, to C_{bypass} , and to the connector power and ground pins, should be at least 50 mils wide to ensure adequate current carrying capability.
- There should be double vias on power and ground nets, and the trace lengths should be kept as short as possible.

10.4.6.3 Front Panel Connector Card

The best way to provide front or side panel support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. Figure 127 shows the major components associated with a typical front/side panel USB solution that uses a front panel connector card.

Figure 127. Motherboard Front Panel USB Support



Note: The terms “connector card” and “daughter card” are used interchangeably.

When designing the motherboard with front/side panel support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a connector card, ensure that there aren't duplicate EMI/ESD/thermistor components placed on the motherboard because this will usually cause drop/droop, and signal quality degradation or failure.

10.4.6.3.1 Front Panel Daughter Card Design Guidelines

- Place the Vbus bypass capacitance, Common Mode Choke, and ESD suppression components on the daughter card as close as possible to the connector pins.
- Follow the same layout, routing and impedance control guidelines as specified for motherboards.
- Minimize the trace length on the front panel connector card. Less than 2-inch trace length is recommended.
- Use the same mating connector pin-out as outlined for the motherboard in Section 10.4.6.2.1.
- Use the same routing guidelines as described in Section 10.4.1.
- Trace length guidelines are given in Table 74.

10.5 IOAPIC Design Recommendation

UP systems not using the IOAPIC Bus should follow these recommendations:

On the ICH4:

- Tie APICCLK directly to ground.
- Tie APICD [1:0] to ground through a 10 k Ω resistor (Separate pull-downs are required if using XOR chain testing.).

On the processor:

- Consult processor documentation.

10.5.1 PIRQ Routing Example

Table 77 describes how the ICH4 uses the PCI IRQ when the IOAPIC is active.

Table 77. IOAPIC Interrupt Inputs 16 – 23 Usage

No	IOAPIC INTIN PIN	Function in Intel® ICH4 Using the PCI IRQ in IOAPIC
1	IOAPIC INTIN PIN 16 (PIRQA)	USB1 UHCI Controller #1
2	IOAPIC INTIN PIN 17 (PIRQB)	AC'97 Audio and Modem; option for SMBus
3	IOAPIC INTIN PIN 18 (PIRQC)	USB1 UHCI Controller #3; Native IDE
4	IOAPIC INTIN PIN 19 (PIRQD)	USB1 UHCI Controller #2
5	IOAPIC INTIN PIN 20 (PIRQE)	Internal LAN; option for SCI, TCO, MMT #0,1,2
6	IOAPIC INTIN PIN 21 (PIRQF)	Option for SCI, TCO, MMT #0,1,2
7	IOAPIC INTIN PIN 22 (PIRQG)	Option for SCI, TCO, MMT #0,1,2
8	IOAPIC INTIN PIN 23 (PIRQH)	USB2 EHCI Controller, Option for SCI, TCO, MMT #0,1,2

Due to different system configurations, IRQ line routing to the PCI slots (“swizzling”) should be made to minimize the sharing of interrupts between both internal ICH4 functions and PCI functions. Figure 128 shows an example of IRQ line routing to the PCI slots (note: it is not necessarily an optimal routing scheme; an optimal scheme depends on individual system PCI IRQ usage).

Figure 128. Example PIRQ Routing

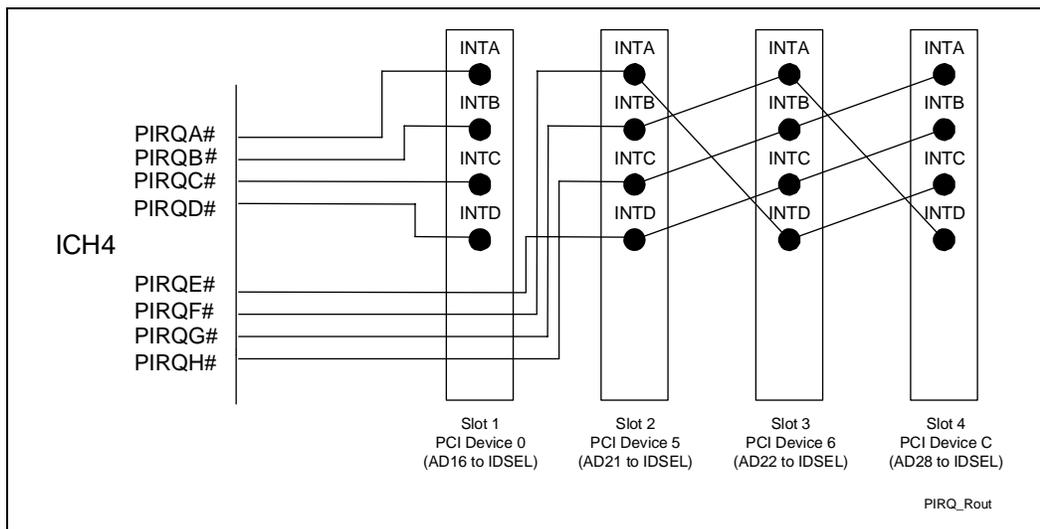


Figure 128 is an example. It is up to the board designer to route these signals in a way that will prove the most efficient for their particular system. A PCI slot can be routed to share interrupts with any of the ICH4 internal device/functions (but at a higher latency cost).

10.6 SMBus 2.0/SMLink Interface

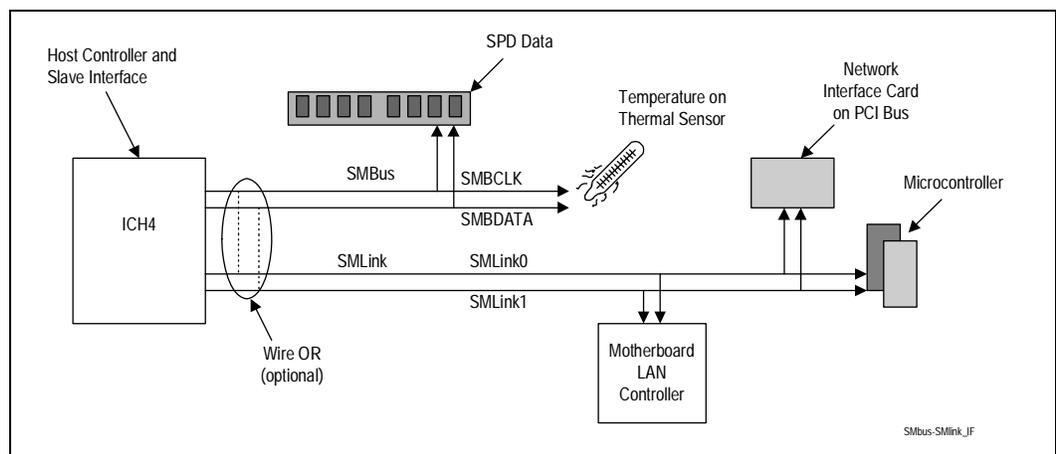
The SMBus interface on the ICH4 uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH4.

The ICH4 incorporates an SMLink interface supporting Alert on LAN*, Alert on LAN2* and a slave functionality. It uses two signals, SMLINK[1:0]. SMLINK0 corresponds to an SMBus clock signal and SMLINK1 corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert on LAN* functionality, the ICH4 transmits heartbeat and event messages over the interface. When using the 82562EM/82562EX platform LAN connect component, the ICH4 integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert on LAN2*-enabled LAN Controller (i.e., 82562EM/82562EX 10/100 Mbps platform LAN connect) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH4 SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, the watchdog timer status, and the system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (e.g., 82562EM/82562EX 10/100 Mbps platform LAN connect) to access targets on the SMBus as well as the ICH4 Slave interface. Additionally, the ICH4 supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, to be fully compliant with the SMBus 2.0 specification (which requires the Host Notify cycle), the SMLink and SMBus signals **must** be tied together externally. This is done by connecting SMLink0 to SMBCLK and SMLink1 to SMBDATA.

Figure 129 SMBUS 2.0/SMLink Interface



Note: Intel does not support external access of the ICH4 Integrated LAN Controller via the SMLink interface. Also, Intel does not support access of the ICH4 SMBus Slave Interface by the ICH4 SMBus Host Controller. Refer to the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

10.6.1 SMBus Architecture and Design Considerations

SMBus Design Considerations

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging because they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in choosing a design are based on:

- Devices that must run in S3
- Amount of VCC_Suspend current available (i.e., minimizing load of VCC_Suspend)
- Device class: High power/Low power. Most designs use primarily High Power Devices.

General Design Issues / Notes

Regardless of the architecture used, there are some general considerations.

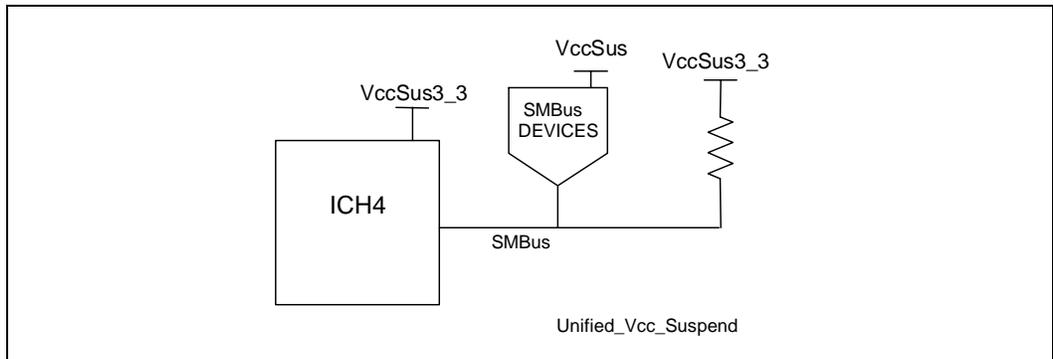
- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and fall time specification.
- The maximum bus capacitance that a physical segment can reach is 400 pF.
- The ICH4 does not run SMBus cycles while in S3
- SMBus devices that can operate in S3 must be powered by the VCC_Suspend supply.
- If SMBus is to be connected to PCI, it must be connected to all PCI slots.

10.6.1.1 Power Supply Considerations

The Unified VCC_Suspend Architecture

In this design all SMBus devices are powered by the VCC_Suspend supply. Consideration must be made to provide enough VCC_Suspend current while in S3.

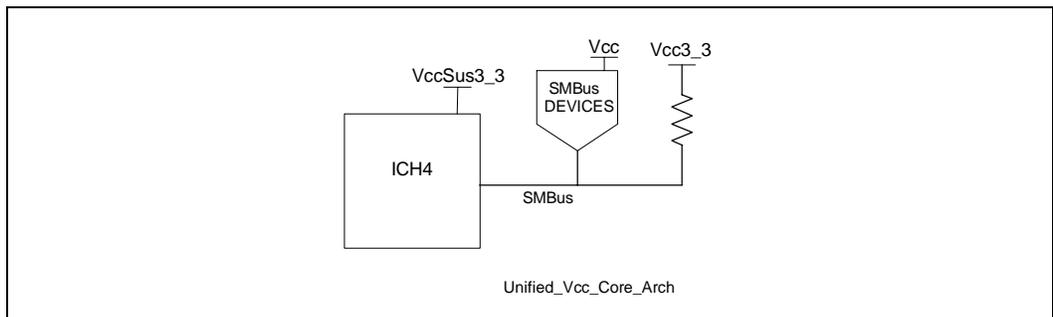
Figure 130. Unified VCC_Suspend Architecture



The Unified VCC_CORE Architecture

In this design, all SMBUS devices are powered by the VCC_CORE supply. This architecture allows none of the devices to operate in S3, but minimizes the load on VCC_Suspend.

Figure 131. Unified VCC_CORE Architecture



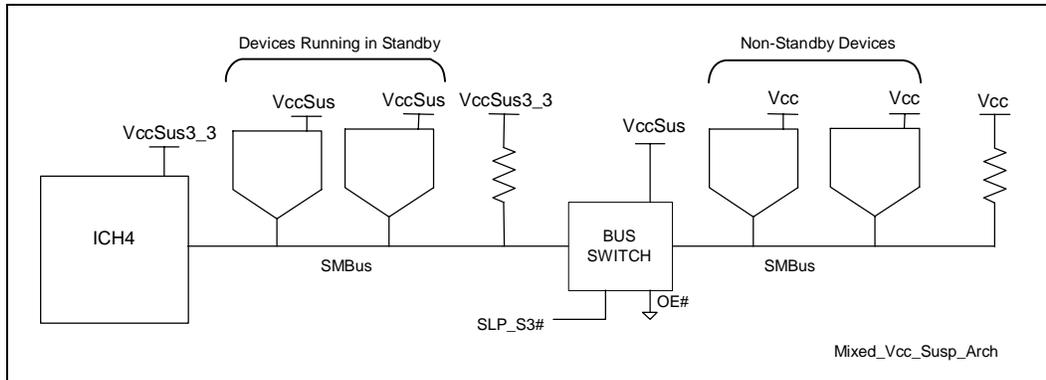
NOTES:

1. The SMBus device must be back-drive safe while its supply (Vcore) is off and VCC_Suspend is still powered.
2. In suspended modes where VCC_CORE is OFF and VCC_Suspend is on, the VCC_CORE node will be very near ground. In this case the input leakage of the ICH4 will be approximately 10 uA.

Mixed Power Supply Architecture

This design allows for SMBus devices to communicate while in S3, yet minimizes VCC_Suspend leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a “bus switch” to isolate the devices powered by the core and suspend supplies. See Figure 132.

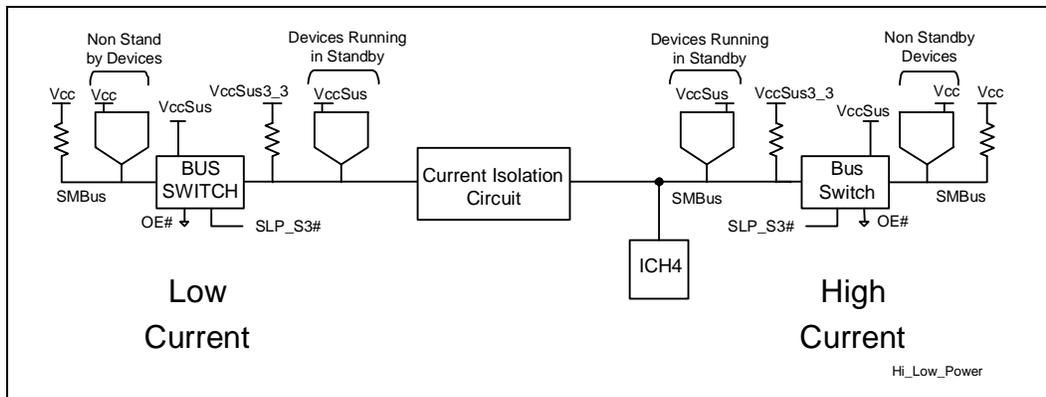
Figure 132. Mixed VCC_Suspend/VCC_CORE Architecture



10.6.1.2 Device Class Considerations:

In addition to the previously-described power supply considerations, system designers should take into consideration the SMBus device class (high power/low power) used on the bus. If the design supports both high power and low power devices on the bus, current isolation of high power segment and low power segment of the bus is needed as shown in Figure 133.

Figure 133. High Power/Low Power Mixed VCC_SUSPEND/VCC_CORE Architecture



10.7 PCI

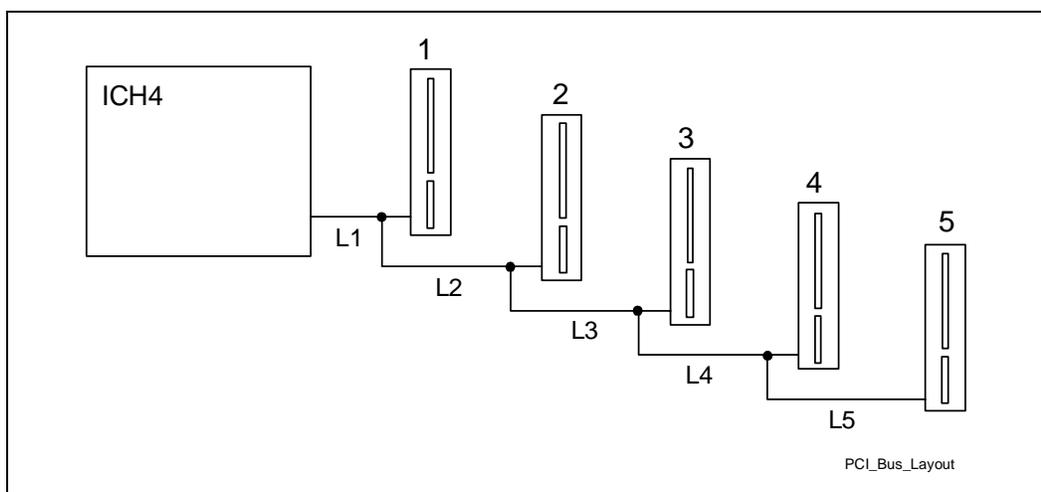
The ICH4 provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH4 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

The ICH4 supports six PCI Bus masters (excluding the ICH4), by providing six REQ#/GNT# pairs. In addition, the ICH4 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

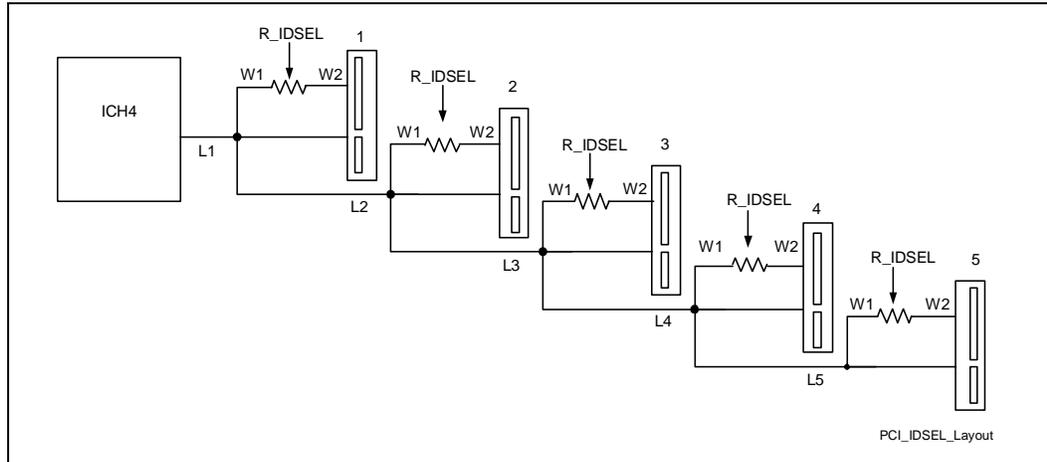
10.7.1 PCI Routing Summary

The following represents a summary of the routing guidelines for the PCI Slots. Simulations assume that PCI cards follow the *PCI Local Bus Specification, Revision 2.2* trace length guidelines.

Figure 134. PCI Bus Layout Example

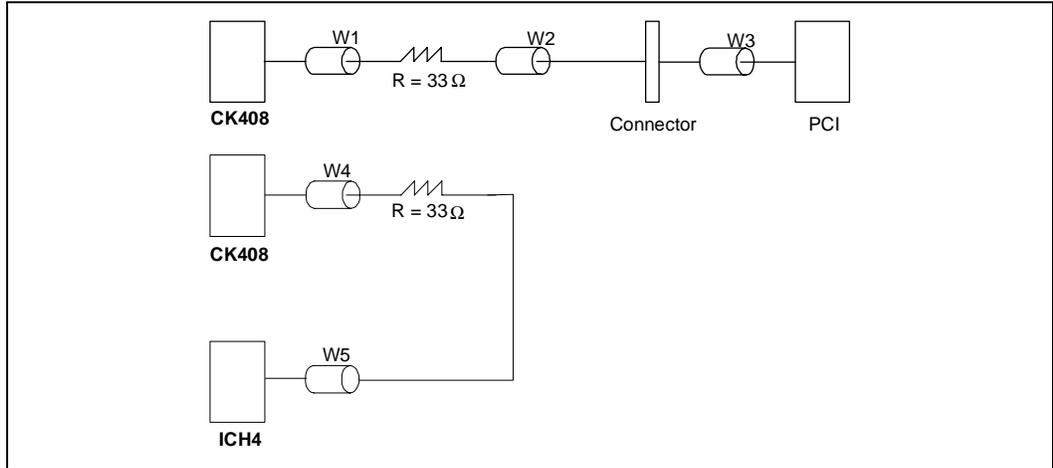


Note: Note that if a CNR connector is placed on the platform, it will share a slot space with one of the PCI slots. However, it will not take away from the slot functionality unless a CNR card occupies the CNR slot.

Figure 135. PCI Bus Layout Example with IDSEL

Table 78. PCI Data Signals Routing Summary

PCI Routing Req.	Trace Impedance	Topology	Maximum Trace Length (Inches)					
			L1	L2	L3	L4	L5	L6
5 on 7	47 Ω to 69 Ω 60 Ω target	2 Slots W1=W2=0.5" R_IDSEL = 300 Ω to 900 Ω	5 to 10	1.5	N/A	N/A	N/A	N/A
		2 Slots with 1 down device W1=W2=0.5" R_IDSEL = 300 Ω to 900 Ω	5 to 10	1.0	3.0	N/A	N/A	N/A
		3 Slots W1=W2=0.5" R_IDSEL = 300 Ω to 900 Ω	5 to 10	1.5	1.5	N/A	N/A	N/A
		3 Slots with 1 down device W1=W2=0.5" R_IDSEL = 300 Ω to 900 Ω	5 to 10	1.0	1.0	3.0	N/A	N/A
		4 Slots W1=W2=0.5" R_IDSEL = 300 Ω to 900 Ω	5 to 10	1.0	1.0	1.0	N/A	N/A
		4 Slots with 1 down device W1=W2=0.5" R_IDSEL = 300 Ω to 900 Ω	5 to 10	1.0	1.0	1.0	3.0	N/A
	5 Slots W1=W2=0.5" R_IDSEL = 300 Ω to 900 Ω	5 to 8	1.0	1.0	1.0	1.0	N/A	
	6 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	5 to 7	1.0	1.0	1.0	1.0	1.0	

Figure 136. PCI Clock Layout Example



NOTE: Clocks should be routed first

Table 79. PCI Clock Signals Routing Summary

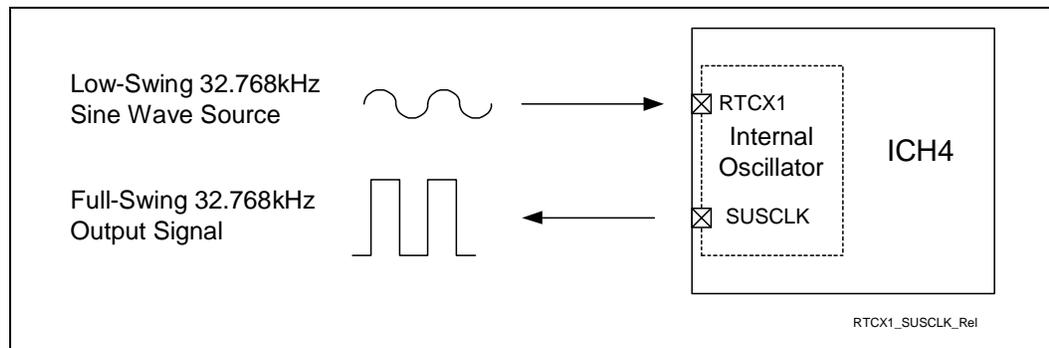
Trace Impedance	PCI Routing Requirements	Topology	Maximum Trace Length				
			W1	W2	W3	W4	W5
51 Ω to 69 Ω, 60 Ω Target	5 on 7	2 – 5 Slots	0.5"	W5 – 4.5"	2.5 inches (Shown as a reference only)	0.5"	Can be as long as needed (as long as W2 is scaled accordingly)

10.8 RTC

The ICH4 contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH4 uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH4, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use. This output ball of the ICH4 is called SUSCLK. This is shown in Figure 137.

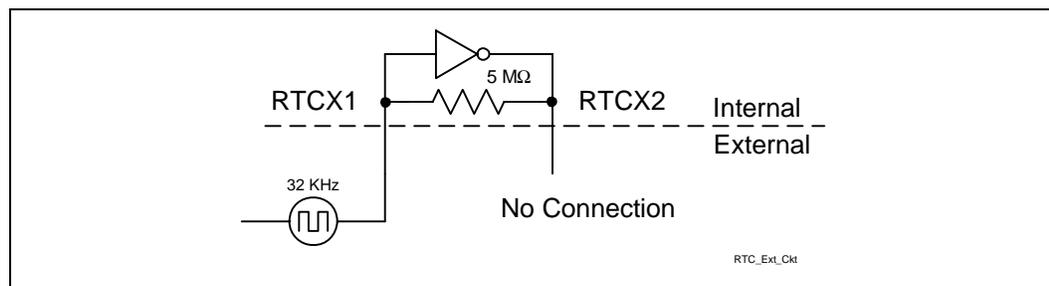
Figure 137. RTCX1 and SUSCLK Relationship in the Intel® ICH4



For further information on the RTC, consult Application Note AP-728 “ICH/ICH2/ICH2M/ICH3S/ICH3M Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions”. This application note is valid for ICH4.

Even if the ICH4 internal RTC is not used, it’s still necessary to supply a clock input to RTCX1 of the ICH4 because other signals are gated off that clock in suspend modes. However, in this case, the frequency accuracy (32.768 kHz) of the clock inputs is not critical. A crystal can be used or a single clock input can be driven into RTCX1 with RTCX2 left as no connect. Figure 138 shows the connection. This is not a validated feature on ICH4. Note that the peak-to-peak swing on RTCX1 cannot exceed 1.0V.

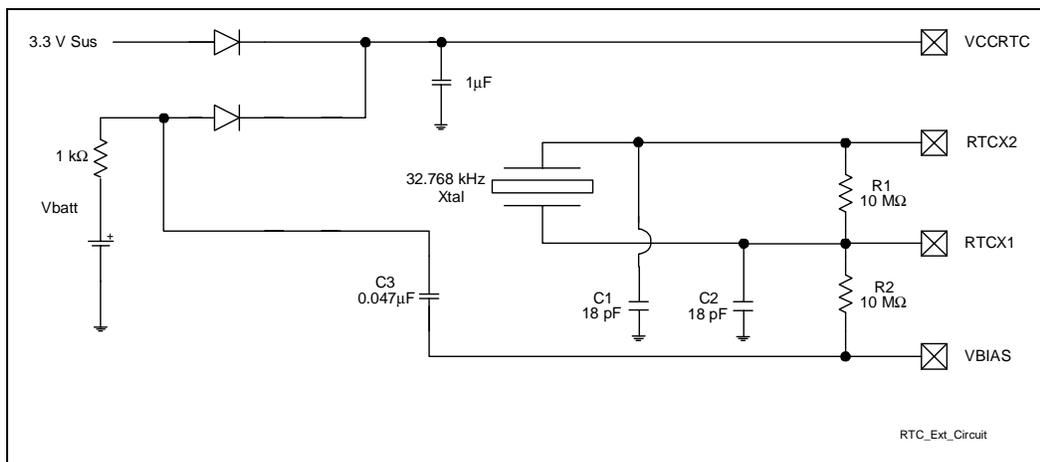
Figure 138. External Circuitry for the Intel® ICH4 Where the Internal RTC Is Not Used



10.8.1 RTC Crystal

The ICH4 RTC module requires an external oscillating source of 32.768 KHz connected on the RTCX1 and RTCX2 balls. Figure 139 shows the external circuitry that comprises the oscillator of the ICH4 RTC.

Figure 139. External Circuitry for the Intel® ICH4 RTC



NOTES:

1. Typical values for C1 and C2 are 18 pF (based on a crystal load of 12.5 pF).
2. Reference designators are arbitrarily assigned.
3. 3.3 V Sus is active whenever the system is plugged in.
4. Vbatt is voltage provided by the battery.
5. VCCRTC, RTCX2, RTCX1, and VBIAS are ICH4 pins.
6. VCCRTC: Power for RTC Well.
7. RTCX2: Crystal Input 2 – Connected to the 32.768 kHz crystal.
8. RTCX1: Crystal Input 1 – Connected to the 32.768 kHz crystal.
9. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.
10. VSS: Ground.

Table 80. RTC Routing Summary

Trace Impedance	RTC Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R1, R2, C1, and C2 Tolerances	Signal Referencing
45 Ω to 69 Ω, 60 Ω Target	5 mil trace width (results in ~2 pF per inch)	1 inch	NA	R1 = R2 = 10 MΩ ± 5% C1 = C2 = (NPO class) See Section 10.8.2 for calculating a specific capacitance value for C1 and C2	Ground

10.8.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C_3 must be 0.047 μF and capacitor values C_1 and C_2 should be chosen to provide the manufacturer's specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{\text{load}} = [(C_1 + C_{\text{in1}} + C_{\text{trace1}}) * (C_2 + C_{\text{in2}} + C_{\text{trace2}})] / [(C_1 + C_{\text{in1}} + C_{\text{trace1}} + C_2 + C_{\text{in2}} + C_{\text{trace2}})] + C_{\text{parasitic}}$$

Where:

- C_{load} = Crystal's load capacitance. This value can be obtained from Crystal's specification.
- $C_{\text{in1}}, C_{\text{in2}}$ = input capacitances at RTCX1, RTCX2 balls of the ICH4. These values can be obtained in the ICH4 data sheet.
- $C_{\text{trace1}}, C_{\text{trace2}}$ = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. Typical value, based on a 5 mil wide trace and a 1/2 ounce copper pour, is approximately equal to:

$$C_{\text{trace}} = \text{trace length} * 2 \text{ pF/inc}$$

- $C_{\text{parasitic}}$ = Crystal's parasitic capacitance. This capacitance is created by the existence of 2 electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C_1, C_2 can be chosen such that $C_1 = C_2$. Using the equation of C_{load} above, the value of C_1, C_2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C_2 can be chosen such that $C_2 > C_1$. Then C_1 can be trimmed to obtain the 32.768 kHz.

In certain conditions, both C_1, C_2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C_1, C_2 values are smaller than the theoretical values, the RTC oscillation frequency will be higher.

The following example will illustrate the use of the practical values C_1, C_2 in the case that theoretical values can not guarantee the accuracy of the RTC in low temperature condition:

Example

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH4, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25 °C) to yield a 32.768 kHz oscillation.

At 0 °C the frequency stability of crystal gives –23 ppm (assumed that the circuit has 0 ppm at 25 °C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C_1, C_2 are chosen to be 6.8 pF instead of 10 pF, this will make the RTC oscillate at higher frequency at room temperature (+23 ppm) but this configuration of C_1 / C_2 makes the circuit oscillate closer to 32.768 kHz at 0 °C. The 6.8 pF value of C_1 and 2 is the **practical value**.

Note that the temperature dependency of crystal frequency is parabolic relationship (ppm / degree square). The effect of changing crystal's frequency when operating at 0 °C (25 degrees below room temperature) is the same when operating at 50 °C (25 °C above room temperature).

10.8.3 RTC Layout Considerations

Because the RTC circuit is very sensitive and requires high accurate oscillation, reasonable care must be taken during layout and routing RTC circuit. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. ICH4 requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of board's material. On FR-4, a 5-mil trace has approximately 2 pF per inch.
- Trace signal coupling must be importantly reduced, by avoiding routing of adjacent PCI signals close to RTCX1 and RTCX1, VBIAS.
- Ground guard plane is highly recommended.
- The oscillator VCC should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

10.8.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH4 is not powered by the system.

Example batteries are: Duracell® 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is

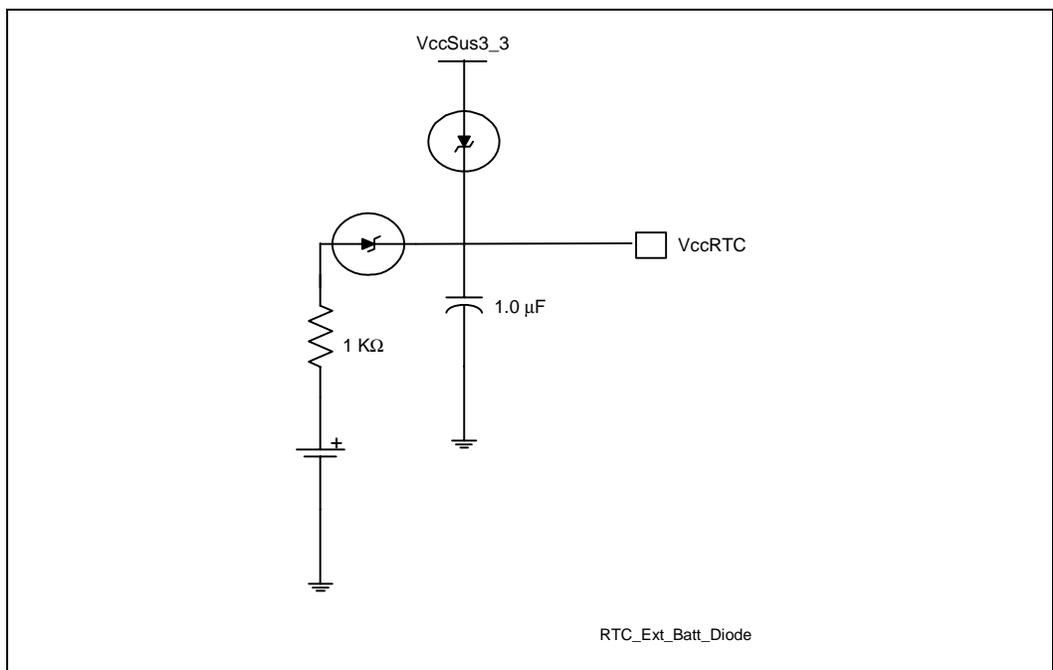
170 mAh (assumed usable) and the average current required is 5 µA, the battery life will be at least:

$$170,000 \mu\text{Ah} / 5 \mu\text{A} = 34,000 \text{ h} = 3.9 \text{ years}$$

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH4 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH4 RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 140 is an example of a diode circuit that is used.

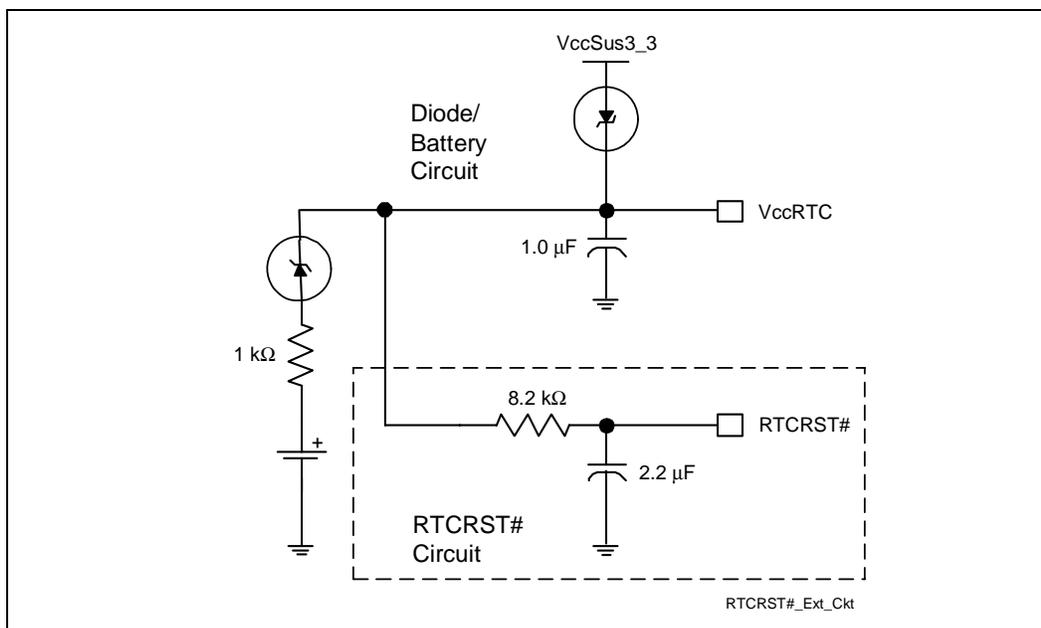
Figure 140. A Diode Circuit to Connect the RTC External Battery



A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

10.8.5 RTC External RTCRST# Circuit

Figure 141. RTCRST# External Circuit for the Intel® ICH4 RTC



The ICH4 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18 ms – 25 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed

This RTCRST# circuit is combined with the diode circuit (shown in Figure 140) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 141 is an example of this circuitry that is used in conjunction with the external diode circuit.

10.8.6 VBIAS DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC Network of R2 and C3 (see Figure 139) therefore it is self-adjusted voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

- VBIAS should be at least 200 mV DC. The RC network of R2 and C3 will filter out most of AC signal that exist on this ball, however, the noise on this ball should be kept minimal to guarantee the stability of the RTC oscillation.
- Probing VBIAS requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). See Application Note AP-728 for further details on measuring techniques.
- Note that VBIAS is also very sensitive to environmental conditions.

10.8.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30 – 70%. If the SUSCLK duty cycle is beyond 30 – 70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50Ω input impedance probe) and it is an appropriated signal to check the RTC frequency to determine the accuracy of the ICH4's RTC Clock (see Application Note AP-728 for further details).

10.8.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRRTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in the previous figure meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VCCRRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

10.9 Internal LAN Layout Guidelines

The ICH4 provides several options for integrated LAN capability. The platform supports several components depending on the target market. Available LAN components include the 82540EM Gigabit Ethernet Controller, 82551QM Fast Ethernet Controller, 82562EZ/82562ET and 82562EX/82562EM platform LAN connect components.

Table 81. LAN Component Connections/Features

LAN Component	Interface To Intel® ICH4	Connection	Features
82540EM (196 BGA)	PCI	Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting	Gigabit Ethernet, ASF 1.0 alerting, PCI 2.2 compatible
82551QM (196 BGA)	PCI	Performance 10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible
82562EM (48 Pin SSOP) 82562EX (196 BGA)	LCI	10/100 Ethernet with Alert on LAN (AoL) alerting	Ethernet 10/100 connection, Alert on LAN (AoL)
82562ET (48 Pin SSOP) 82562EZ (196 BGA)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

Which LAN component to use on the ICH4 platform will depend on the end user's need for connection speed, manageability needs, and bus connection type. In addition, footprint compatible packages make it possible to design a platform that can use any of the LAN components without the need for a motherboard redesign.

10.9.1 Footprint Compatibility

The 82540EM Gigabit Ethernet Controller, 82551QM Fast Ethernet Controller, and the 82562EX/82562EZ platform LAN connect devices are all manufactured in a footprint compatible 15mm x 15mm (1 mm pitch), 196-ball grid array package. Many of the critical signal pin locations on the 82540EM, 82551QM, and 82562EX/82562EZ are identical, allowing designers to create a single design that accommodates any one of these parts. Because the usage of some pins on the 82540EM differ from the usage on the 82551QM or the 82562EX/82562EZ, the parts are not referred to as “pin compatible”. The term “footprint compatible” refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design. Therefore, it is easy to populate a single board design with either part to maximize value while matching your customers’ performance needs.

Design guidelines are provided for each required interface and connection. Refer to the following figures and table for the corresponding section of the design guide. The guidelines use the 82546EZ to refer to both the 82562EZ and 82562EX. The 82562EX is specified in those cases where there is a difference.

Figure 142. Intel® ICH4/Platform LAN Connect Section

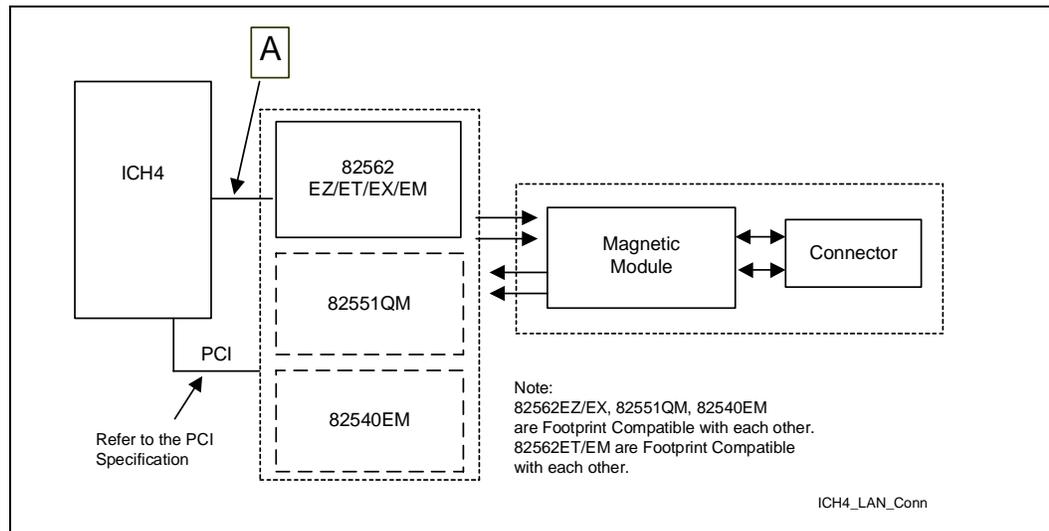


Table 82. LAN Design Guide Section Reference

Layout Section	Figure 142 Reference	Design Guide Section
ICH4 – LAN Connect Interface (LCI)	A	10.9.2 - LAN Connect Interface Guidelines
82562EZ/EX 82562ET / 82562EM	A	10.9.3 Design and Layout Considerations for 82562EZ/EX and 82551QM
82551QM	PCI	10.9.3 Design and Layout Considerations for 82562EZ/EX and 82551QM

82540EM	PCI	10.10.2 Design and Layout Considerations for 82540EM
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10.9.2 Intel® ICH4 — LAN Connect Interface Guidelines

This section contains guidelines on how to implement a Platform LAN connect device on a system motherboard or on a CNR riser card. It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH4 to LAN connect interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports 82562EZ/ET and 82562EX/EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD0, and LAN_TXD0 are shared by all components. The AC characteristics for this interface are found in the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*.

10.9.2.1 Bus Topologies

The platform LAN connect interface can be configured in several topologies:

- Direct point-to-point connection between the ICH4 and the LAN component
- LOM/CNR Implementation

10.9.2.1.1 LOM (LAN on Motherboard) or CNR Point-to-Point Interconnect

The following are guidelines for a single solution motherboard. Either 82562EZ/ET, 82562EX/EM, or CNR are uniquely installed.

Figure 143. Single Solution Interconnect

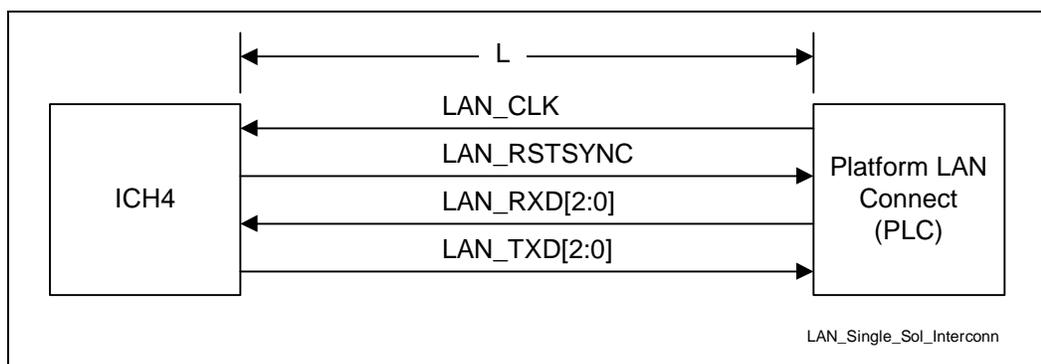


Table 83. LAN LOM or CNR Routing Summary

Trace Impedance	LAN Routing Requirements	Maximum Trace Length		Signal Ref.	LAN Signal Length Matching
51 Ω to 69 Ω, 60 Ω Target	5 on 10	82562EZ/ET/EX/EM	4.5" to 12"	Ground	Data signals must be equal to no more than 0.5 inches (500 mils) shorter than the LAN clock trace.
		82562EZ/ET/EX/EM on CNR	2" to 9.5"		

10.9.2.1.2 LOM (LAN on Motherboard) and CNR Interconnect

The following guidelines apply to an all-inclusive configuration of PLC design. This layout combines LAN on motherboard and the CNR solutions. The resistor pack ensures that either a CNR option or a LAN on motherboard option can be implemented at one time.

Figure 144. LOM/CNR Interconnect

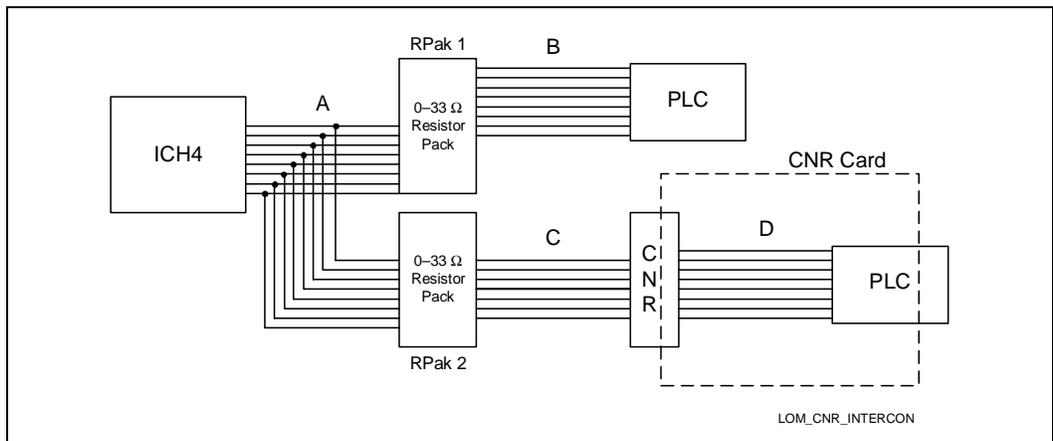


Table 84. LOM/CNR Dual Routing Summary

Trace Impedance	LAN Routing Req.	Maximum Trace Length				Sig. Ref.	LAN Signal Length Matching
51 Ω to 69 Ω, 60 Ω Target	5 on 10	82562EZ /ET/EX/EM				Gnd.	Data signals must be equal to or no more than 0.5 inches (500 mils) shorter than the LAN clock trace.
		A	B	C	D		
		0.5" to 7.5"	4" to (11.5 – A) "	NA	NA		
		82562EZ /ET/EX/EM on CNR¹					
		A	B	C	D		
		0.5" to 7.5"	NA	1.5" to (9.0 – A) "	0.5" to 3"		

NOTE: ¹Total motherboard trace length should not exceed 9.0"

The following are additional guidelines:

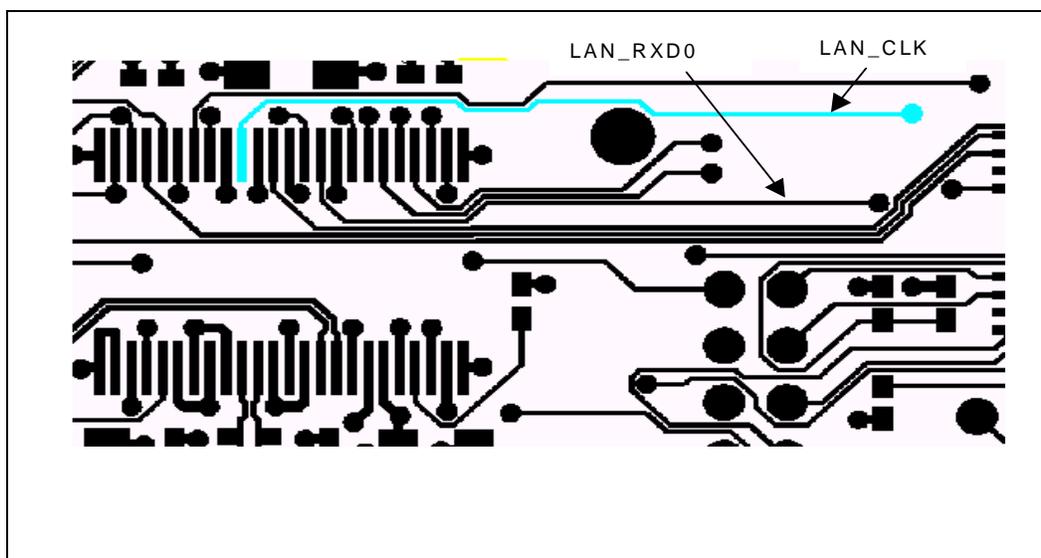
- Stubs due to the resistor pack should not be present on the interface.

- The resistor pack value can be 0 Ω to 33 Ω (See Section 10.9.2.5).

10.9.2.2 Signal Routing and Layout

Platform LAN connect Interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 145. LAN_CLK Routing Example



10.9.2.3 Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the tRMATCH skew parameter. tRMATCH is the sum of the trace length mismatch between LAN_CLK and LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inches shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-PLC signals.

10.9.2.4 Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 $\Omega \pm 15\%$ is strongly recommended; otherwise, signal integrity requirements may be violated.

10.9.2.5 Line Termination

Line termination mechanisms are not specified for the LAN connect interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 0 to 33 Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

10.9.2.6 Terminating Unused LAN Connect Interface Signals

The LAN connect interface on the ICH4 can be left as a no-connect if it is not used.

10.9.3 Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM and Intel® 82551QM

For correct LAN performance, designers must follow the general guidelines outlined in Section 10.9.2 (General LAN Routing Guidelines and Considerations). Additional guidelines for implementing an 82562EZ/ET/EX/EM or 82551QM platform LAN connect component are provided below.

10.9.3.1 Guidelines for Intel® 82562EZ/ET/EX/EM / Intel® 82551QM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

10.9.3.2 Crystals and Oscillators

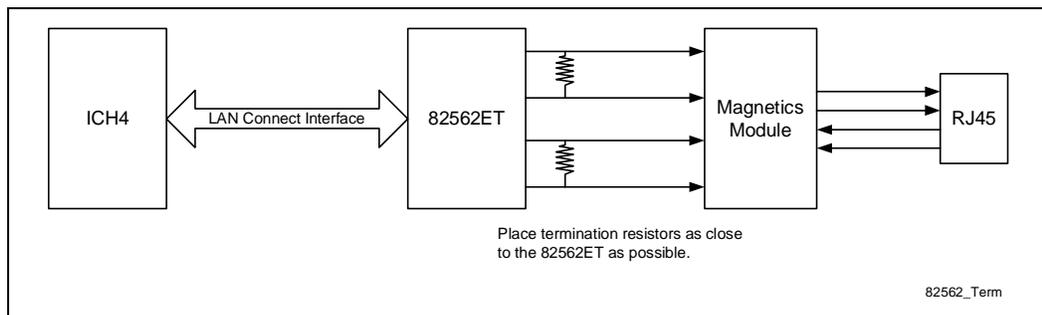
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562EZ/ET/EX/EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

10.9.3.3 Intel® 82562EZ/ET/EX/EM / Intel® 82551QM Termination Resistors

The 100 Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 121 Ω ($\pm 1\%$) receive differential pairs (RDP/RDN) should be placed as close to the platform LAN connect component (82562EZ/ET/EX/EM and 82551QM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

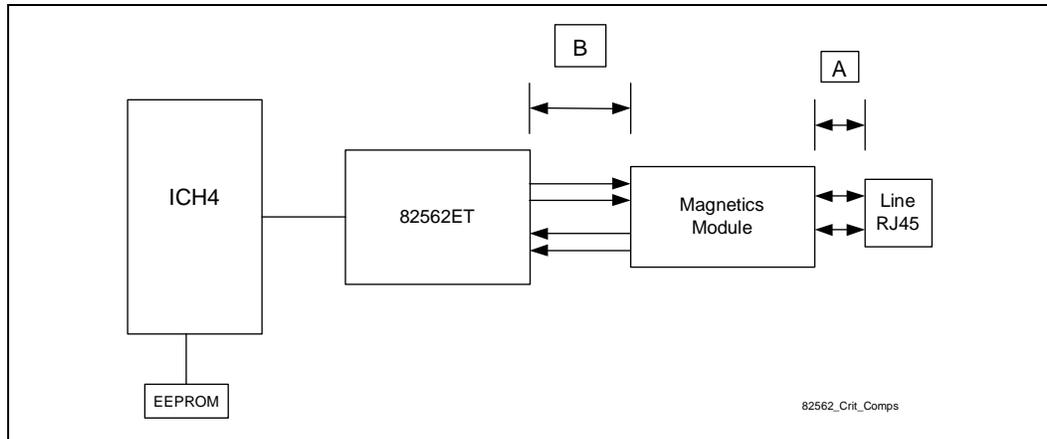
Figure 146. Intel® 82562ET/82562EM Termination



10.9.3.4 Critical Dimensions

There are two dimensions to consider during layout. Distance ‘A’ from the line RJ45 connector to the magnetics module and distance ‘B’ from the 82562EZ/ET/EX/EM or 82551QM to the magnetics module. The combined total distances of A and B must not exceed 4 inches (preferably, less than 2 inches — see Figure 147).

Figure 147. Critical Dimensions for Component Placement



Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

10.9.3.4.1 Distance from Magnetics Module to RJ45 (Distance A)

The distance A in the preceding figure should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- Differential Impedance:** The differential impedance should be 100 Ω . The single ended trace impedance will be approximately 60 Ω ; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry:** Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit’s performance and contribute to radiated emissions from the transmit circuit. If the 82562EZ/ET/EX/EM or 82551QM must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562EZ/ET/EX/EM or 82551QM and RJ45 as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If

the actual impedance is consistently low, a target of 105–110 Ω should compensate for second order effects.

10.9.3.4.2 Distance from Intel® 82562EZ/ET/EX/EM / Intel® 82551QM to Magnetics Module (Distance B)

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and equal length within each differential pair.

10.9.3.5 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of cross talk. The effect of different configurations on the amount of cross talk can be studied using electronics modeling software.

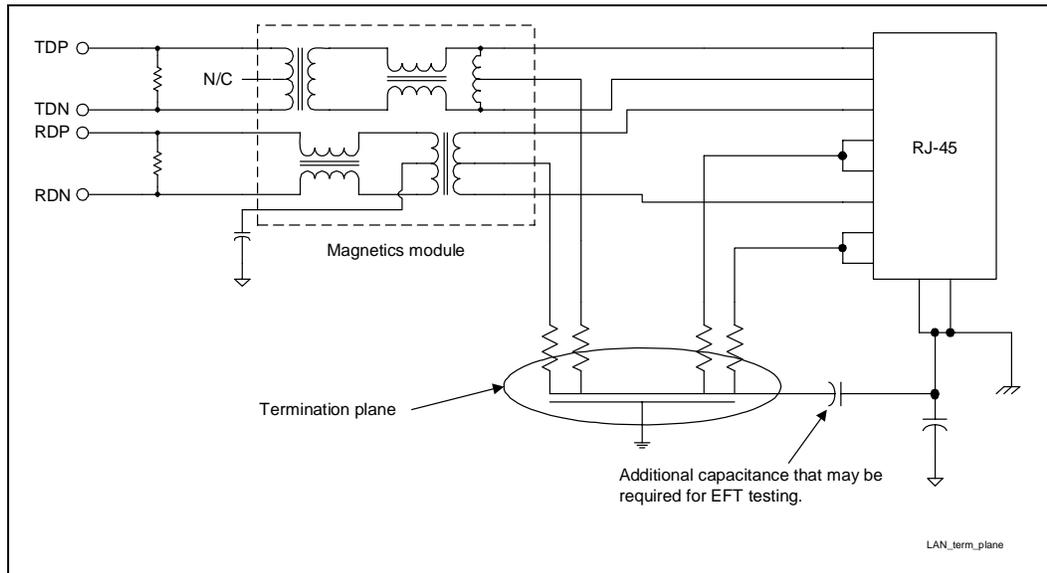
10.9.3.5.1 Terminating Unused Connections

In Ethernet designs it is common practice to terminate unused connections on the RJ45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

10.9.3.5.2 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

Figure 148. Termination Plane

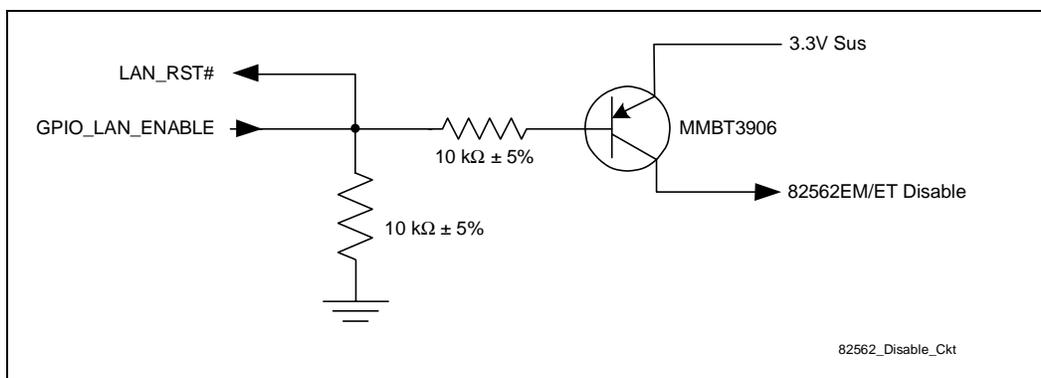


10.10 Intel® 82562EZ/ET/EX/EM Disable Guidelines

10.10.1 Intel® 82562EZ/ET/EX/EM Disable Guidelines

To disable the 82562EZ/ET/EX/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. The BIOS controlling the GPIO can disable the LAN microcontroller.

Figure 149. Intel® 82562EZ/ET/EX/EM Disable Circuitry



There are 4 pins, which are used to put the 82562EZ/ET/EX/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 85 describes the operational/disable features for this design.

The four control signals shown in Table 85 should be configured as follows: Test_En should be pulled-down thru a 100 Ω resistor. The remaining 3 control signals should each be connected thru 100 Ω series resistors to the common node “82562EZ/ET/EX/EM _Disable” of the disable circuit.

Table 85. Intel® 82562EZ/ET/EX/EM Control Signals

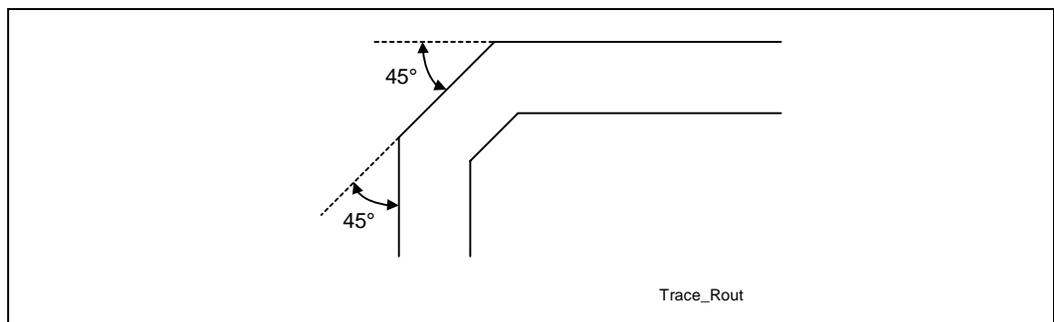
Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

10.10.1.1 General Intel® 82562ET/82562EM Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of cross talk and propagation delays on sections of the board where high speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance: (Note: Some suggestions are specific to a 4.3 mil stackup.)

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).]
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces. (300 mils recommended)
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. Refer to Figure 150.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 150. Trace Routing



10.10.1.1.1 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be $\sim 100 \Omega$. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by 10Ω , when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

10.10.1.1.2 Signal Isolation

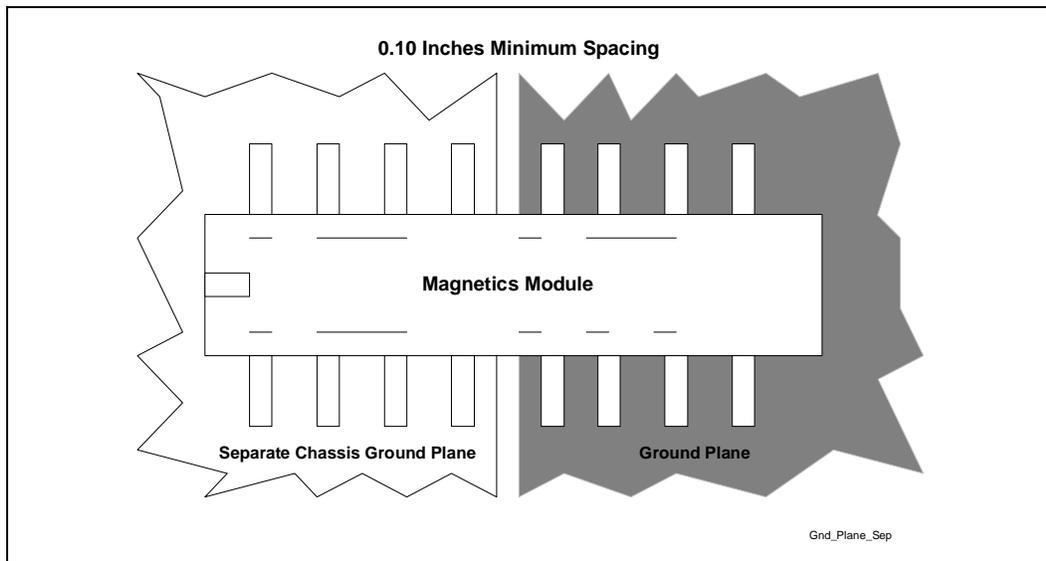
Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize cross talk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, Processor, or other similar devices.

10.10.1.1.3 Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 151. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both back planes and motherboards.

- Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics that can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

10.10.1.2 Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

- Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
- Lack of symmetry between the two traces within a differential pair. [Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.] Asymmetry can create common-mode noise and distort the waveforms.
- Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer. The magnetics should be as close to the connector as possible (less than or equal to one inch).
- Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
- Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45, and the PLC.
- Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
- Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or App.-Note.
- Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or term plane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The AP-Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.

- Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω , even when the designers think they've designed for 100 Ω . [To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close† to each other the edge coupling can lower the effective differential impedance by 5 to 20 Ω . A 10 to 15 Ω drop in impedance is common.] Short traces will have fewer problems if the differential impedance is a little off.
- Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetics transmit center-tap (on the 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. [6 pF to 12 pF values have been used on past designs with reasonably good success.] These caps are not necessary, unless there is some overshoot in 100 Mbps mode.

Note: It is important to keep the two traces within a differential pair close† to each other. Keeping them close† helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces.

Note: † Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

10.10.2 Design and Layout Considerations for 82540EM

For specific design and layout considerations for the 82540EM refer to:

82540EM Gigabit Ethernet Controller Preliminary Datasheet and Hardware Design Guide

10.11 Intel® ICH4 Usage Models and Isolation Strap Requirements

This section provides ICH4 SYS_RESET# and PWRBTN# usage models and power-well isolation Control Strap Requirements.

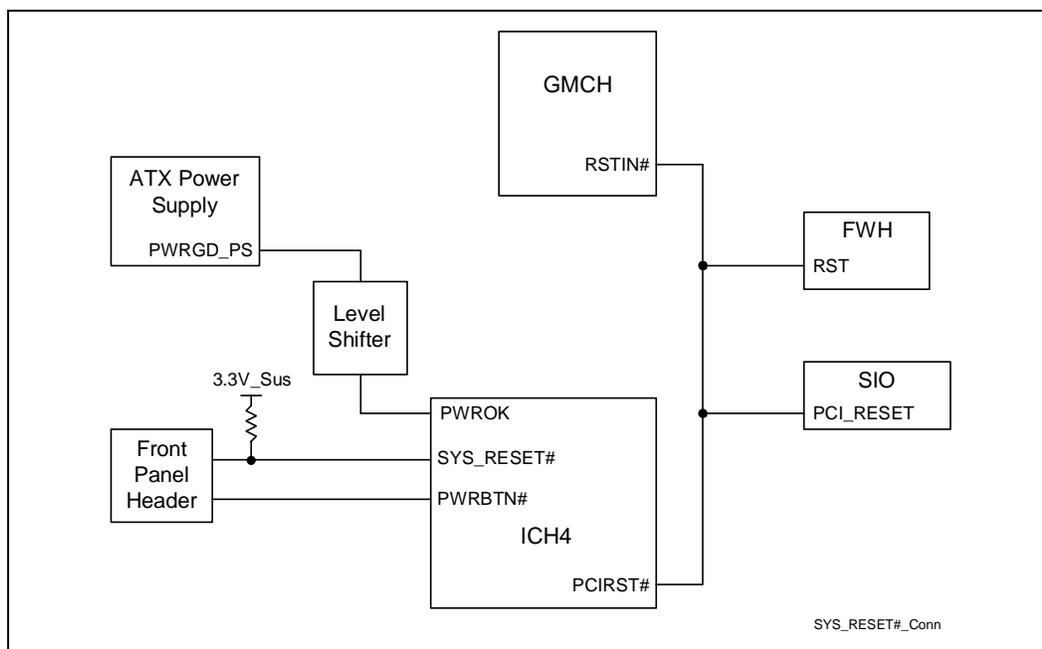
10.11.1 SYS_RESET# Usage Model

The System Reset ball (SYS_RESET#) on the ICH4 can be connected directly to the reset button on the systems front panel provided that the front panel header pulls this signal up to 3.3 V standby through a weak pull-up resistor. The ICH4 will debounce signals on this pin (16 ms) and allow the SMBus to go idle before resetting the system; thus helping prevent a slave device on the SMBus from “hanging” by resetting in the middle of a cycle.

10.11.2 PWRBTN# Usage Model

The Power Button ball (PWRBTN#) on the ICH4 can be connected directly to the power button on the systems front panel. This signal is internally pulled-up in the ICH4 to 3.3 V standby through a weak pull-up resistor (24 K Ω nominal). The ICH4 has 16 ms of internal debounce logic on this pin.

Figure 152. SYS_RESET# and PWRBTN# Connection

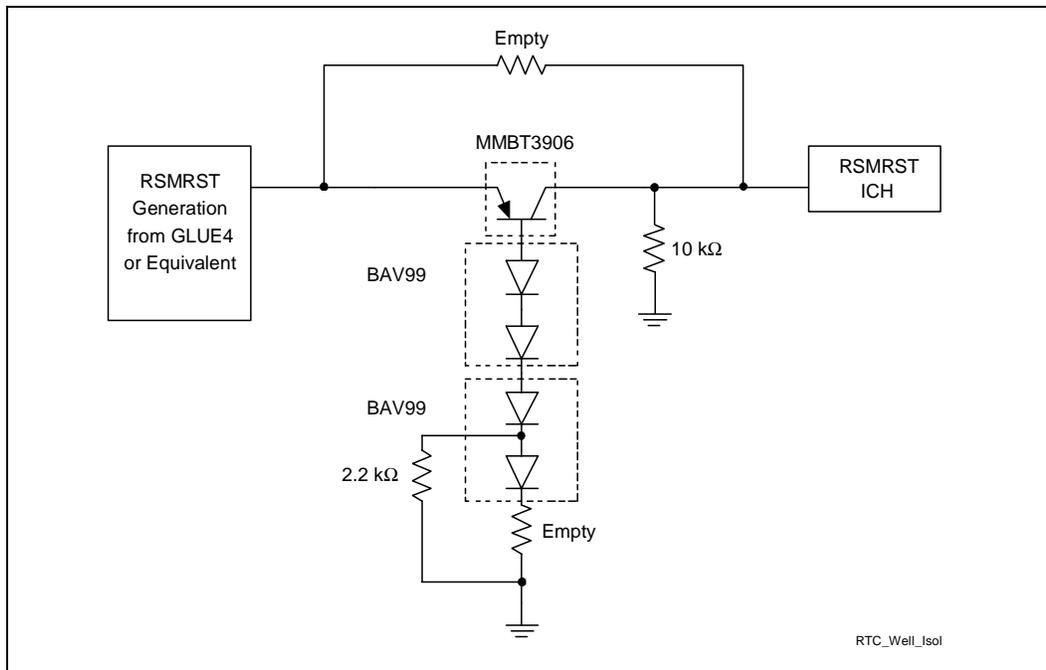


10.11.3 Power-Well Isolation Control Requirement

The RSMRST# signal of the ICH4 must transition from 20 % signal level to 80 % signal level and vice-versa in 50 us. Slower transitions may result in excessive droop on the VCCRRTC node during Sx-to-G3 power state transitions (removal of AC power). Droop on this node can potentially cause the CMOS to be cleared or corrupted, the RTC to loose time after several AC power cycles, or the intruder bit might assert erroneously.

The circuit shown in Figure 153 can be implemented to control well isolation between the VccSus3_3 and RTC power-wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail or does not meet the above rise/fall time.

Figure 153. RTC Power Well Isolation Control



10.12 General Purpose I/O

10.12.1 GPIO summary

The ICH4 has 12 general purpose inputs, 8 general purpose outputs, and 16 general purpose inputs/outputs.

Table 86. GPIO Summary

GPIO #	Power Well	Input, Output, I/O	Tolerance	Note
0	Core	Input	5 V	2
1	Core	Input	5 V	2
2	Core	Input	5 V	2
3	Core	Input	5 V	2
4	Core	Input	5 V	2
5	Core	Input	5 V	2
6	Core	Input	5 V	
7	Core	Input	5 V	
8	Resume	Input	3.3 V	
11	Resume	Input	3.3 V	2
12	Resume	Input	3.3 V	
13	Resume	Input	3.3 V	
16	Core	Output	3.3 V	2
17	Core	Output	3.3 V	2
18	Core	Output	3.3 V	
19	Core	Output	3.3 V	
20	Core	Output	3.3 V	
21	Core	Output	3.3 V	
22	Core	Output (Open Drain)	3.3 V	
23	Core	Output	3.3 V	
24	Resume	I/O	3.3 V	1
25	Resume	I/O	3.3 V	1
27	Resume	I/O	3.3 V	1
28	Resume	I/O	3.3 V	1
32	Core	I/O	3.3 V	1
33	Core	I/O	3.3 V	1
34	Core	I/O	3.3 V	1
35	Core	I/O	3.3 V	1
36	Core	I/O	3.3 V	1
37	Core	I/O	3.3 V	1
38	Core	I/O	3.3 V	1
39	Core	I/O	3.3 V	1
40	Core	I/O	3.3 V	1
41	Core	I/O	3.3 V	1
42	Core	I/O	3.3 V	1
43	Core	I/O	3.3 V	1

NOTES:

1. Defaults as an output.
2. Can be used as a GPIO if the native function is not needed. ICH4 defaults these signals to native functionality.

11 FWH Guidelines

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the FWH BIOS Specification or equivalent.

11.1 FWH Vendors

The following vendors manufacture firmware hubs, which conform to the *Intel® FWH Specification*. Contact the vendor directly for information on packaging and density.

SST <http://www.ssti.com/>

STM <http://us.st.com/stonline/index.shtml>

ATMEL <http://www.atmel.com/>

11.2 FWH Decoupling

A 0.1 μF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple high frequency noise, which may affect the programmability of the device.

Additionally, a 4.7 μF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the VCC supply pins.

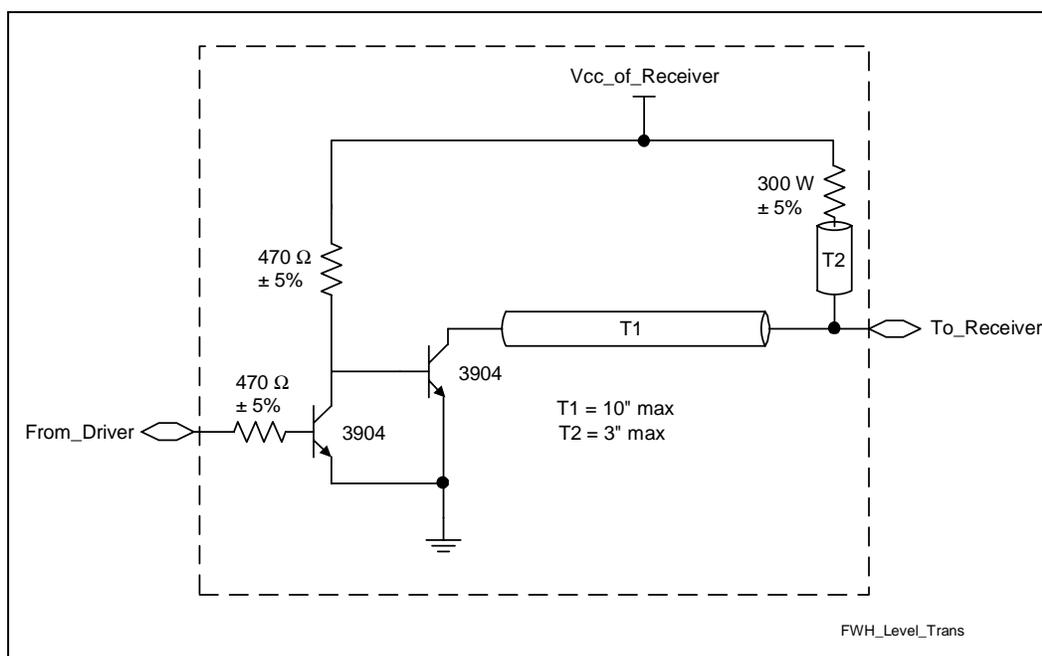
11.3 In Circuit FWH Programming

All cycles destined for the FWH will appear on PCI. The ICH4 Hub Interface to PCI Bridge will put all processor boot cycles out on PCI (before sending them out on the FWH interface). If the ICH4 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. To boot off a PCI card it is necessary to keep the ICH4 in subtractive decode mode. If a PCI boot card is inserted and the ICH4 is programmed for positive decode, there will be two devices positively decoding the same cycle.

11.4 FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the ICH4 INIT# signal must be at a value slightly higher than the V_{IH} min FWH INIT# pin specification. The ICH4 inactive state of this signal is typically governed by the formula $V_{CPU_IOmin} - \text{noise margin}$. Therefore if the V_{CPU_IOmin} of the processor is 1.6 V, the noise margin is 200 mV and the V_{IH} min spec of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because $1.6 \text{ V} - 0.2 \text{ V} = 1.40 \text{ V}$ which is greater than the 1.35 V minimum of the FWH. If the V_{IH} min of the FWH was 1.45 V, then there would be an incompatibility and logic translation would need to be used. Note that these examples do not take into consideration actual noise that may be encountered on INIT#. Care must be taken to ensure that the V_{IH} min specification is met with ample noise margin. In applications where it is necessary to use translation logic, refer to the circuit in Figure 154.

Figure 154 FWH Level Translation Circuitry



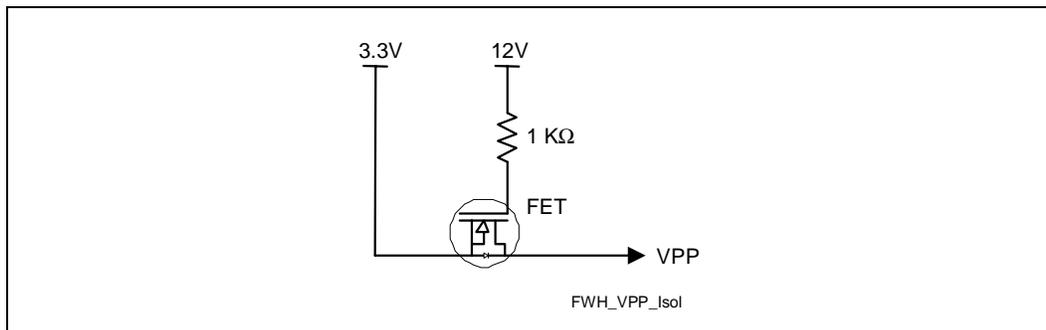
Note: This translation circuit is optimized to function with low voltage processors that the ICH4 supports.

11.5 FWH VPP Design Guidelines

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports V_{PP} of 3.3 V or 12 V. If V_{PP} is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12 V V_{PP} for 80 hours (3.3 V on V_{PP} does not affect the life of the device). The 12 V V_{PP} would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The V_{PP} pin **MUST** be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. To decrease programming time, it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 155. FWH VPP Isolation Circuitry





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12 Miscellaneous Logic

The ICH4 requires additional external circuitry to function properly. Some of these functionalities include meeting timing specifications, buffering signals, and switching between power wells. This logic may be implemented through the use of the Glue Chip or discrete logic.

12.1 Glue Chip 4

To reduce the component count and BOM (Bill of Materials) cost of the ICH4 platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The ICH4 Glue Chip is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Features

- Dual, Strapping, Selectable Feature Sets
- Audio-disable circuit
- Mute Audio Circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK (PWRGD_3V) signal generation
- Power Sequencing / BACKFEED_CUT
- Power Supply turn on circuitry
- RSMRST# generation
- Voltage Translation for DDC to VGA monitor
- HSYNC / VSYNC voltage translation to VGA monitor
- Tri-state buffers for test
- Extra GP Logic Gates
- Power LED Drivers
- Flash FLUSH# / INIT# circuit

More information regarding this component is available from the vendors listed in the following table.

Vendor	Contact Information	Part Number
Philips Semiconductors	http://www.semiconductors.philips.com	PCA9504A



Fujitsu Microelectronics	http://www.fujitsumicro.com/	MB87B302ABPD-G-ER
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12.2 Discrete Logic

As an alternative solution, discrete circuitry may be implemented into a design instead of using the Glue Chip.

13 Platform Clock Routing Guidelines

The following information details platform clock and routing layout guidelines for an 845G chipset based platform.

13.1 Clock Generation

Only one clock generator component is required in an 845G chipset based platform. Clock synthesizers that meet the *Intel® CK-408 Clock Synthesizer/Driver Specification* are suitable for an 845G chipset based platform. For more information on CK-408 compliance, refer to the *Intel® CK-408 Clock Synthesizer/Driver Specification* document. The following tables and figure list and describe the 845G chipset clock groups, the platform system clock cross-reference, and the platform clock distribution:

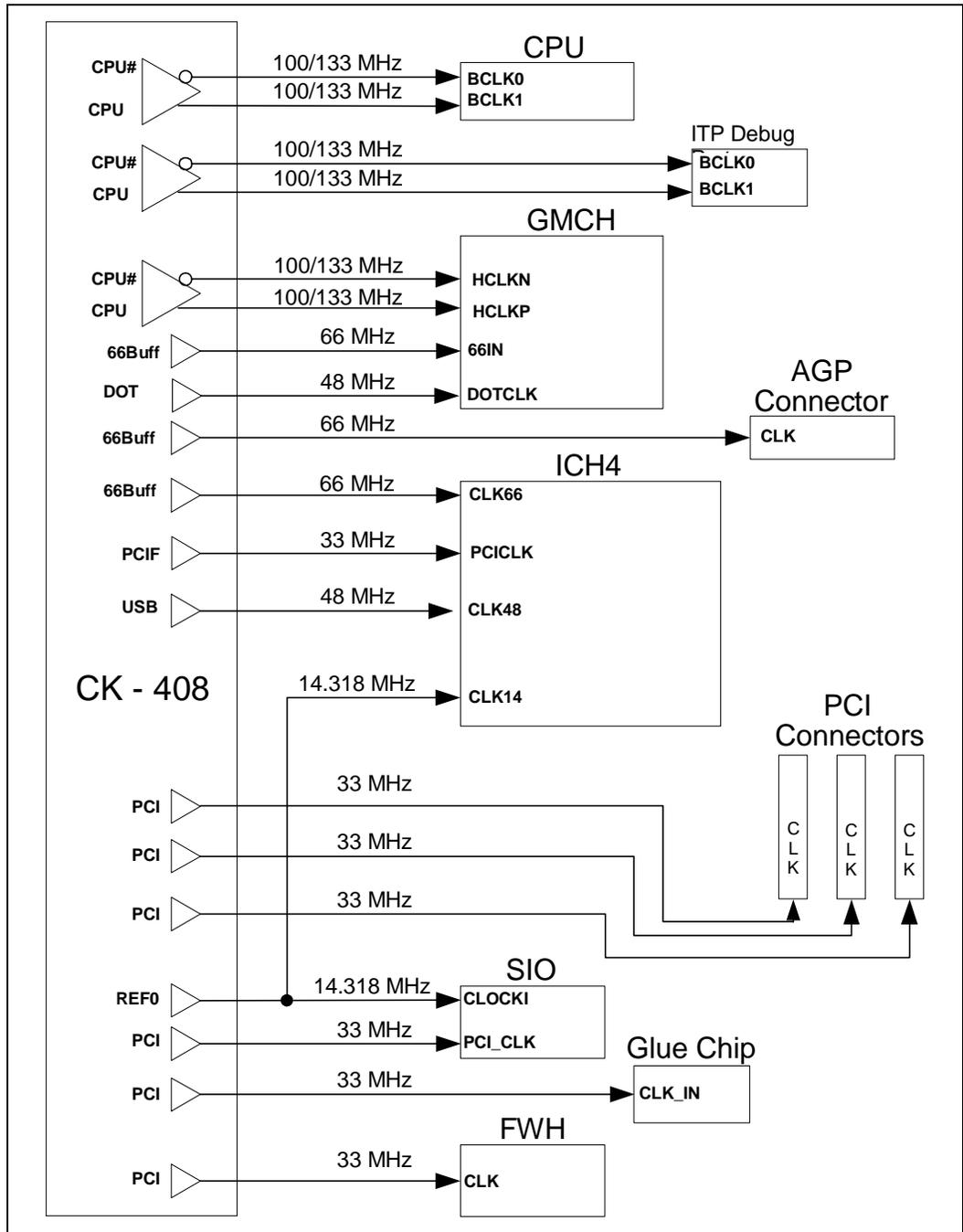
Table 87. Intel® 845G Chipset Clock Groups

Clock Name	Frequency	Receiver
Host_CLK	100/133 MHz	CPU, ITP Debug Port, and GMCH
DOT_CLK	48 MHz	GMCH
CLK66	66 MHz	GMCH and ICH4
AGPCLK	66 MHz	AGP Connector or AGP Device
CLK33	33 MHz	ICH4, SIO, Glue Chip, and FWH/Flash BIOS
CLK14	14.318 MHz	ICH4 and SIO
PCICLK	33 MHz	PCI Connector
USBCLK	48 MHz	ICH4

Table 88. Platform System Clock Cross-Reference

Clock Group	CK-408 Pin	Component	Component Pin Name
HOST_CLK	CPU	CPU	BCLK0
	CPU#	CPU	BCLK1
	CPU	ITP Debug Port	BCK
	CPU#	ITP Debug Port	BCK#
	CPU#	GMCH	HCLKN
	CPU	GMCH	HCLKP
DOT_CLK	DOT_48 MHz	GMCH	DREFCLK
CLK66	3V66	GMCH	GCLKIN
		ICH4	CLK66
AGPCLK	3V66	AGP Connector or AGP Device	AGPCLK
CLK33	PCIF	ICH4	PCICLK
	PCI	SIO	PCI_CLK
	3V66	Glue Chip	CLK_IN
	PCI	FWH/Flash BIOS	CLK
CLK14	REF0	ICH4	CLK14
		SIO	CLOCKI
PCICLK	PCI	PCI Connector #1	CLK
		PCI Connector #2	CLK
		PCI Connector #3	CLK
USBCLK	USB_48MHz	ICH4	CLK48

Figure 156. Platform Clocking Block Diagram



13.2 Clock Group Topology and Layout Routing Guidelines

13.2.1 HOST_CLK Clock Group

The clock synthesizer provides four sets of differential clock outputs. The differential clocks are driven to the processor, the 845G chipset, and the processor debug port as shown in Figure 156.

The clock driver differential bus output structure is a “Current Mode Current Steering” output which develops a clock signal by alternately steering a programmable constant current to the external termination resistors R_t . The resulting amplitude is determined by multiplying I_{OUT} by the value of R_t . The current I_{OUT} is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of R_t to match impedances or to accommodate future load requirements.

The recommended termination for the differential bus clock is a “Shunt Source termination.” Refer to Figure 157 for this termination scheme. Parallel R_t resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors R_s provide isolation from the clock driver’s output parasitics, which would otherwise appear in parallel with the termination resistor R_t .

The value of R_t should be selected to match the characteristic impedance of the system board and R_s should be between 20 and 33 Ω . Simulations have shown that R_s values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

- Mult0 pin (pin # 43) connected to HIGH – making the multiplication factor as 6.
- Iref pin (pin # 42) is connected to ground through a 475 $\Omega \pm 1\%$ resistor, making the Iref 2.32 mA.

Figure 157. Processor BCLK Topology and Source Shunt Termination

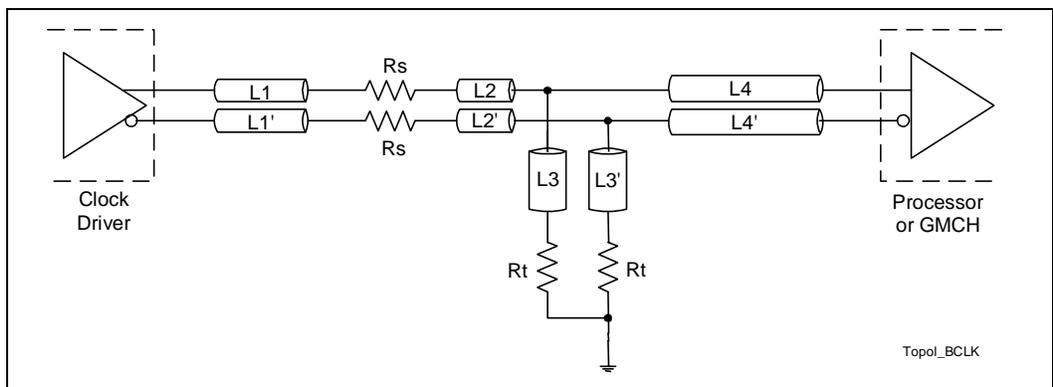


Table 89. Host Clock Routing Guidelines (BCLK [1:0]#, HCLKP, HCLKN)

Layout Guideline	Value	Notes
Host Clock Skew between agents	400 ps total Budget: 150 ps for Clock driver 250 ps for interconnect	2, 3, 4,5
Reference Plane	Ground Referenced (Contiguous over entire length)	
Differential pair spacing = S	8 mils	6, 7
Spacing to other traces	3S to 4S	
Nominal trace width = W	7.0 mils	8
System board Impedance – Differential	100 Ω \pm 15%	9
System board Impedance – odd mode	50 Ω \pm 15%	10
Processor routing length – L1, L1': Clock driver to Rs	0.5" max	13
Processor routing length – L2, L2': Rs to Rs-Rt node	0 – 0.2"	13
Processor routing length – L3, L3': RS-RT node to Rt	0 – 0.2"	13
Processor routing length – L4, L4': RS-RT Node to Load	2 – 12"	
GMCH routing length – L1, L1': Clock Driver to RS	0.5" max	13
GMCH routing length – L2, L2': Rs to Rs-Rt node	0 – 0.2"	13
GMCH routing length – L3, L3': RS-RT node to Rt	0 – 0.2"	13
GMCH routing length – L4, L4': RS-RT Node to Load	2 – 12"	
Clock driver to Processor and clock driver to chipset length matching (L1+L2+L4)	Clock pair to GMCH must be 100 mils longer than clock pair to processor socket	10
HCLKP – HCLKN, BCLK0 – BCLK1 length matching	\pm 10 mils	
Rs Series termination value	27 Ω \pm 1%	11
Rt Shunt termination value	49.9 Ω \pm 1% (for 50 Ω MB impedance)	12
Maximum Via Count Per Signal	3	

NOTES:

1. The skew budget includes clock driver output pair to output pair jitter (differential jitter), and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes clock pairs are routed on multiple routing layers and routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two bus agents. Measured at the crossing point.
5. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network.
7. Set line width to meet correct system board impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stackup.



8. The differential impedance of each clock pair is approximately $2 \cdot Z_{\text{single-ended}} \cdot (1 - 2 \cdot K_b)$ where K_b is the backwards crosstalk coefficient. For the recommended trace spacing, K_b is very small and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
9. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the BCLK traces vary within the tolerances specified, both traces of a differential pair must vary equally.
10. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the system board trace length for the chipset will be longer than that for the processor. Details of this additional length will be included in a future revision of the processor package files.
11. Rt shunt termination value should match the system board impedance.
12. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ring back.
13. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in ϵ_r and the impedance variations due to physical tolerances of circuit board material.

Host Clock Routing Guidelines

- When routing the 100/133 MHz differential clocks do not split up the two halves of a differential clock pair between layers and route to all agents on the same physical routing layer referenced to ground.
- If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Do not place Vias between adjacent complementary clock traces, and avoid differential Vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential Vias can be placed within length L1, between clock driver and RS, if needed to shorten length L1.

Differential Routing

- The host clock pairs must be routed differentially and on the same physical routing layer.
- DO NOT split the two halves of a differential clock pair. Route them referenced to ground for the entire length.

EMI Constraints

- Clocks are a significant contributor to EMI and should be treated with care. Following recommendations can aid in EMI reduction:
- Maintain uniform spacing between the two halves of differential clocks
- Route clocks on physical layer adjacent to the VSS reference plane only

Figure 158. Clock Skew as Measured from Agent to Agent

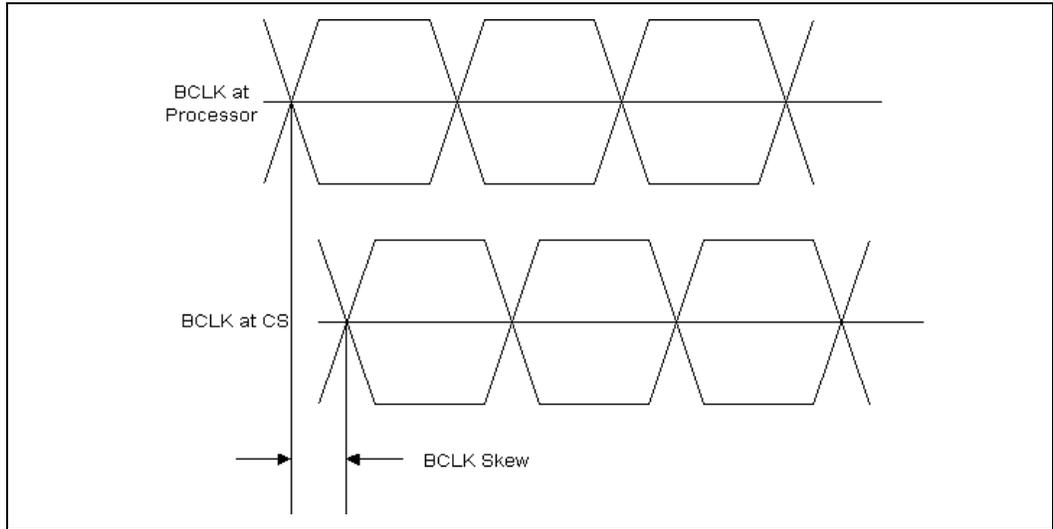
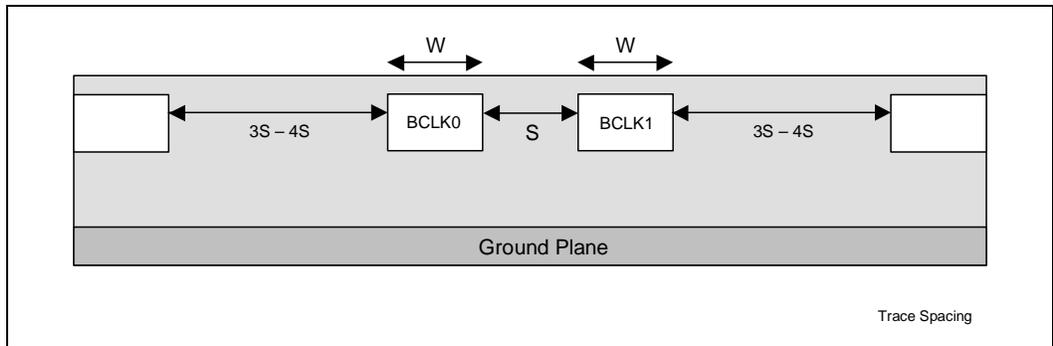


Figure 159. Trace Spacing



13.2.2 DOT_CLK Clock Group

The driver is the clock synthesizer 48 MHz clock output buffer and the receiver is the 48 MHz clock input buffer at the GMCH. Note that this clock is asynchronous to any other clock on the board.

Figure 160. Topology for DOT_CLK

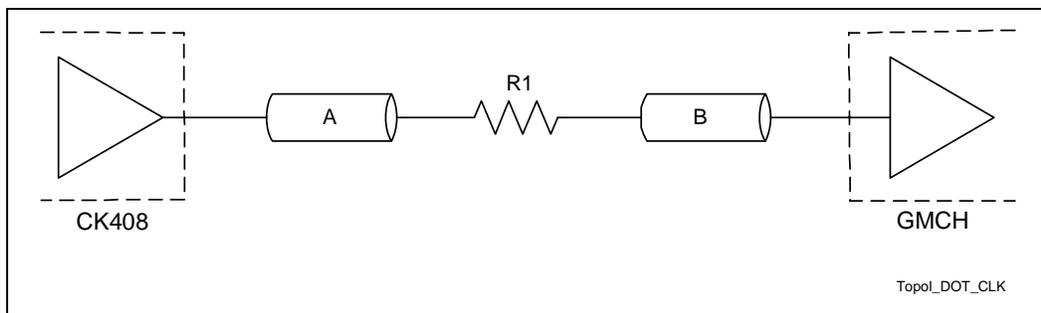


Table 90. DOT_CLK Routing Guidelines

Parameter	Routing Guidelines
Clock Group	DOT_CLK
Topology	Point to point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Z_0)	$60 \Omega \pm 15\%$
Trace Width	5 mils
Spacing to other traces	20 mils
Trace Length – A	0.00" to 0.50"
Trace Length – B	2.0" to 9.0"
Resistor	$R1 = 27 \Omega \pm 1\%$
Maximum Via Count Per Signal	3

13.2.3 CLK66 Clock Group

The driver is the clock synthesizer 66 MHz clock output buffer and the receiver is the 66 MHz clock input buffer at the Glue 4, GMCH and the ICH4. Note that the goal is to have as little skew between the clocks within this group. The 66 MHz clock to the Glue 4 chip has no trace length matching requirements with the rest of the clocks in this group.

Figure 161. Topology for CLK66

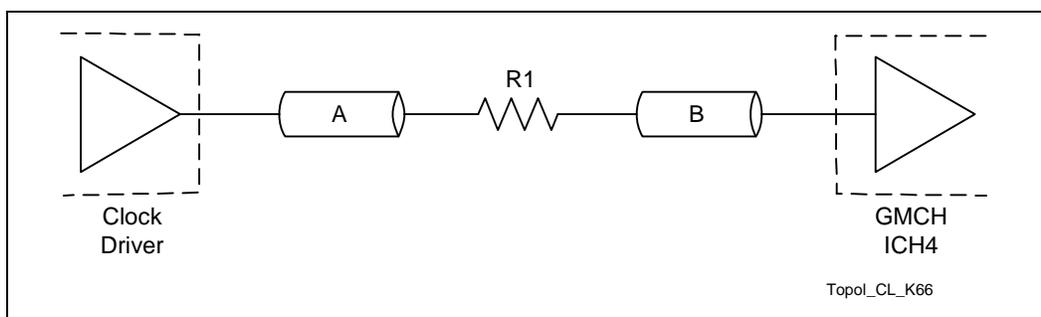


Table 91. CLK66 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK66
Topology	Point to point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Z_0)	$60 \Omega \pm 15\%$
Trace Width	5 mils
Trace Spacing	20 mils
Spacing to other traces	20 mils
Trace Length – A	0.00" to 0.50"
Trace Length – B	4.00" to 8.50"
Resistor	$R1 = 33 \Omega \pm 1\%$
Skew Requirements	All the clocks in the CLK66 group should have minimal skew (~ 0) between each other.
Clock Driver to GMCH	X
Clock Driver to ICH	$X \pm 100$ mils
Maximum Via Count Per Signal	3

NOTE: If the trace length from the clock driver to the GMCH is X the trace length from clock to ICH4 must be $X \pm 100$ mils.

13.2.4 AGPCLK Clock Group

The driver is the clock synthesizer 66 MHz clock output buffer and the receiver is the 66 MHz clock input buffer at the AGP device. Note that the goal is to have minimal (~ 0) skew between this clock and the clocks in the clock group CLK66.

Figure 162. Topology for AGPCLK to AGP Connector

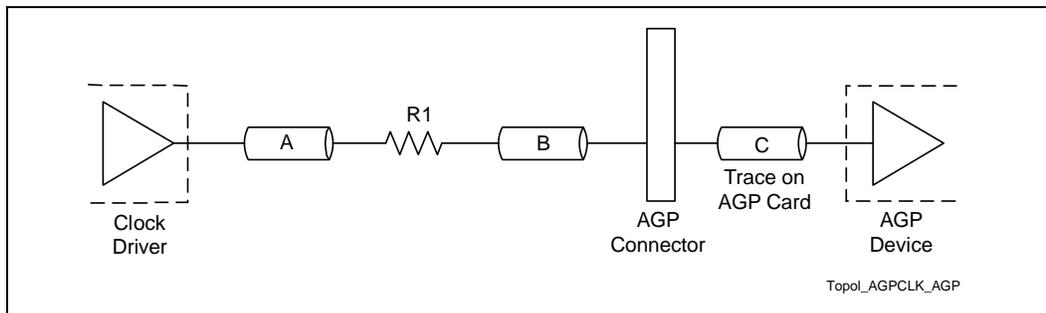


Figure 163. Topology for AGPCLK to AGP Device Down

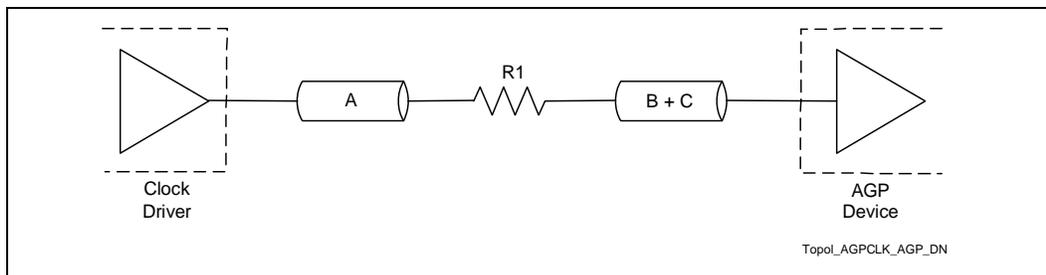


Table 92. AGPCLK Routing Guidelines

Parameter	Routing Guidelines
Clock Group	AGPCLK
Topology	Point to point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Z_0)	$60 \Omega \pm 15\%$
Trace Width	5 mils
Trace Spacing	15 mils
Spacing to other traces	15 mils
Trace Length – A	0.00" to 0.50"
Trace Length – B	(CLK66 Trace B) – 4"
Trace Length – C	Routed 4" per the AGP Specification
Resistor	$R1 = 33 \Omega \pm 1\%$
Skew Requirements	Should have minimal (~ 0) skew between the AGPCLK and the clocks in the CLK66 clock group.

Parameter	Routing Guidelines
Maximum Via Count Per Signal	3

13.2.5 CLK33 Clock Group

The driver is the clock synthesizer 33 MHz clock output buffer and the receiver is the 33 MHz clock input buffer at the ICH4, FWH, Glue Chip, and SIO. Note that the goal is to have minimal (~ 0) skew between the clocks within this group, and also minimal (~ 0) skew between the clocks of this group and that of group CLK66.

Figure 164. Topology for CLK33

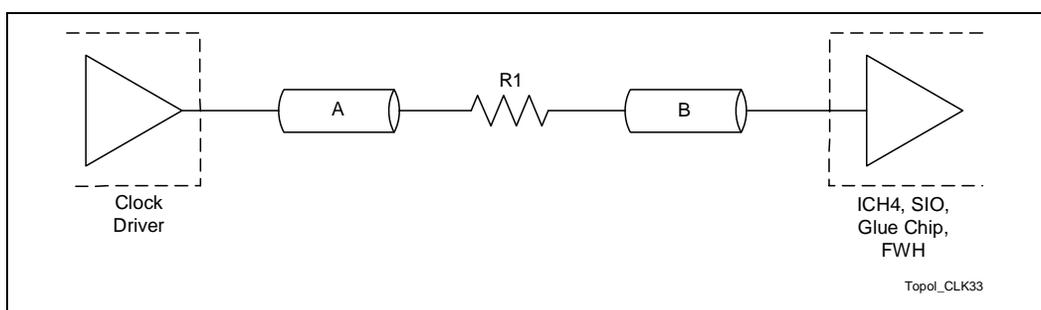


Table 93. CLK33 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point to point
Characteristic Trace Impedance (Z_0)	$60 \Omega \pm 15\%$
Trace Width	5 mils
Trace Spacing	15 mils
Spacing to other traces	15 mils
Trace Length – A	0.5" max
Trace Length – B	4.0" to 8.5"
Total Trace Length – A + B	$(\text{CLK66}) \pm 100$ mils
Resistor	$R1 = 33 \Omega \pm 5\%$
Skew Requirements	Should have minimal (~ 0) skew between the clocks within this group, and also minimal (~ 0) skew between the clocks of this group and that of group CLK66.
Maximum Via Count Per Signal	4

13.2.6 CLK14 Clock Group

The driver is the clock synthesizer 14.318 MHz clock output buffer and the receiver is the 14.318 MHz clock input buffer at the ICH4 and SIO. Note that the clocks within this group should have minimal skew (~ 0) between each other. However, each of the clocks in this group is asynchronous to clocks in other groups.

Figure 165. Topology for CLK14

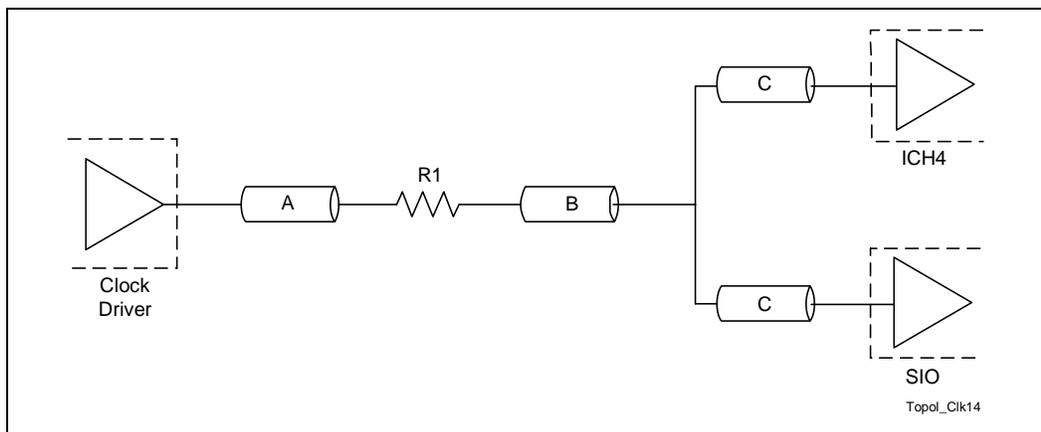


Table 94. CLK14 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK14
Topology	Balanced Topology
Characteristic Trace Impedance (Z_0)	$60 \Omega \pm 15\%$
Trace Width	5 mils
Trace Spacing	10 mils
Spacing to other traces	10 mils
Trace Length – A	0.00" to 0.50"
Trace Length – B	0.00" to 12"
Trace Length – C	0.00" to 6"
CLK14 Total Length (A+B+C)	Matched to ± 0.5 " of each other
Resistor	$R1 = 33 \Omega \pm 5\%$

13.2.7 PCICLK Clock Group

The driver is the clock synthesizer 33 MHz clock output buffer and the receiver is the 33 MHz clock input buffer at the PCI devices. Note that the goal is to have a maximum of ± 1 ns skew between the clocks within this group, and also a maximum of ± 1 ns skew between the clocks of this group and that of group CLK33.

Figure 166. Topology for PCICLK to PCI Device Down

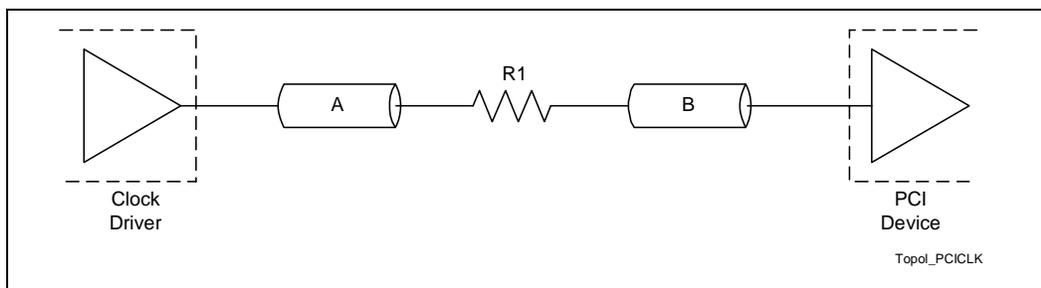


Table 95. PCICLK Routing Guidelines for PCI Device Down

Parameter	Routing Guidelines
Clock Group	PCICLK
Topology	Point to point
Characteristic Trace Impedance (Z_0)	$60 \Omega \pm 15\%$
Trace Width	5 mils
Trace Spacing	15 mils
Spacing to other traces	15 mils
Trace Length – A	0.50" max
Trace Length – B	Not Specified
Total Trace Length – A + B	$(\text{CLK33}) \pm 500$ mils
Resistor	$R1 = 33 \Omega \pm 5\%$
Maximum Via Count Per Signal	4

Figure 167. Topology for PCICLK to PCI Slot

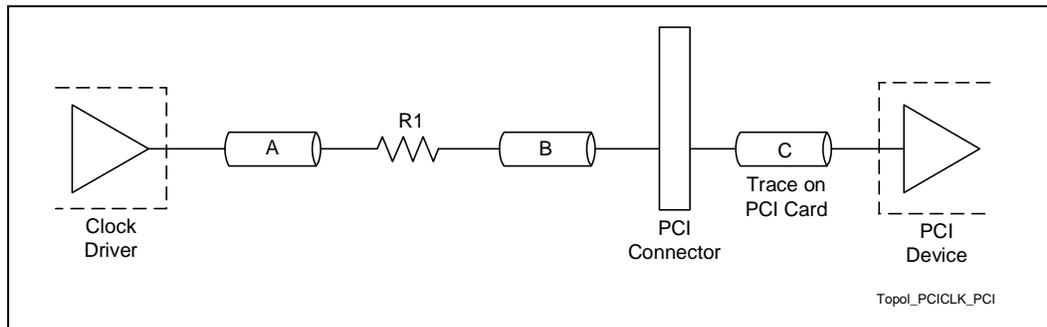


Table 96. PCICLK Routing Guidelines for Devices on PCI Cards

Parameter	Routing Guidelines
Clock Group	PCICLK
Topology	Point to point
Characteristic Trace Impedance (Z_0)	$60 \Omega \pm 15\%$
Trace Width	5 mils
Trace Spacing	15 mils
Spacing to other traces	15 mils
Trace Length – A	0.5" max
Trace Length – B	Not Specified Trace Length B constraints are indicated in the Total MB Trace Length – A + B parameters in this table.
Trace Length – C	2.50", As per the PCI Specification
Total MB Trace Length – A + B	$(\text{CLK33} - 2.5") \pm 500$ mils
Resistor	$R1 = 33 \Omega \pm 5\%$
Skew Requirements	Should have a maximum of ± 1 ns skew between the clocks within this group, and also a maximum of ± 1 ns skew between the clocks of this group and that of group CLK33.
Maximum via Count per signal	4

13.2.8 USBCLK Clock Group

The driver is the clock synthesizer USB clock output buffer and the receiver is the USB clock input buffer at the ICH4. Note that this clock is asynchronous to any other clock on the board.

Figure 168. Topology for USB_CLOCK

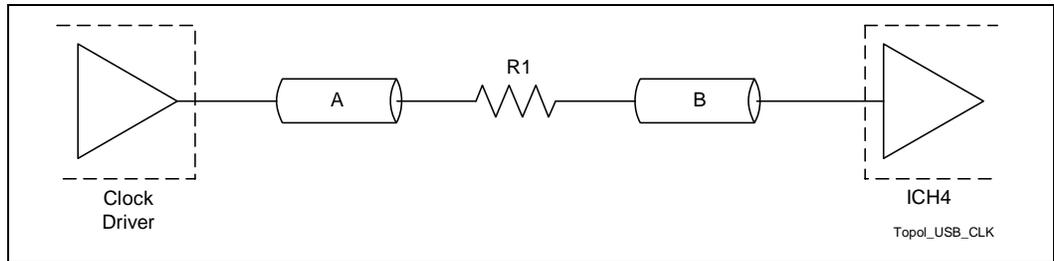


Table 97. USBCLK Routing Guidelines

Parameter	Routing Guidelines
Clock Group	USBCLK
Topology	Point to point
Reference Plane	Ground Referenced (Contiguous over entire Length)
Characteristic Trace Impedance (Zo)	60 $\Omega \pm 15\%$
Trace Width	5 mils
Spacing to other traces	20 mils
Trace Length – A	0.00" – 0.50"
Trace Length – B	3.00" – 12.00"
Resistor	R1 = 27 $\Omega \pm 5\%$
Skew Requirements	None – USBCLK is asynchronous to any other clock on the board
Maximum via Count per signal	3



13.3 CK-408 Power Delivery

13.3.1 Power Plane Isolation

- Special care must be taken to provide quiet supplies to Vdd, VddA and 48 MHz Vdd.
- The VddA signal is especially sensitive to switching noise induced by the other Vdd signals on the clock chip
 - The VddA signal is also sensitive to switching noise generated elsewhere in the system such as CPU VRM. The LC Pie filter should be designed to provide the best reasonable isolation.

13.3.2 Referencing

- Ground referencing is strongly recommended on all Host, 66 MHz, 48 MHz platform clocks.
- Motherboard layer transitions and power plane split crossing must be kept at a minimum.

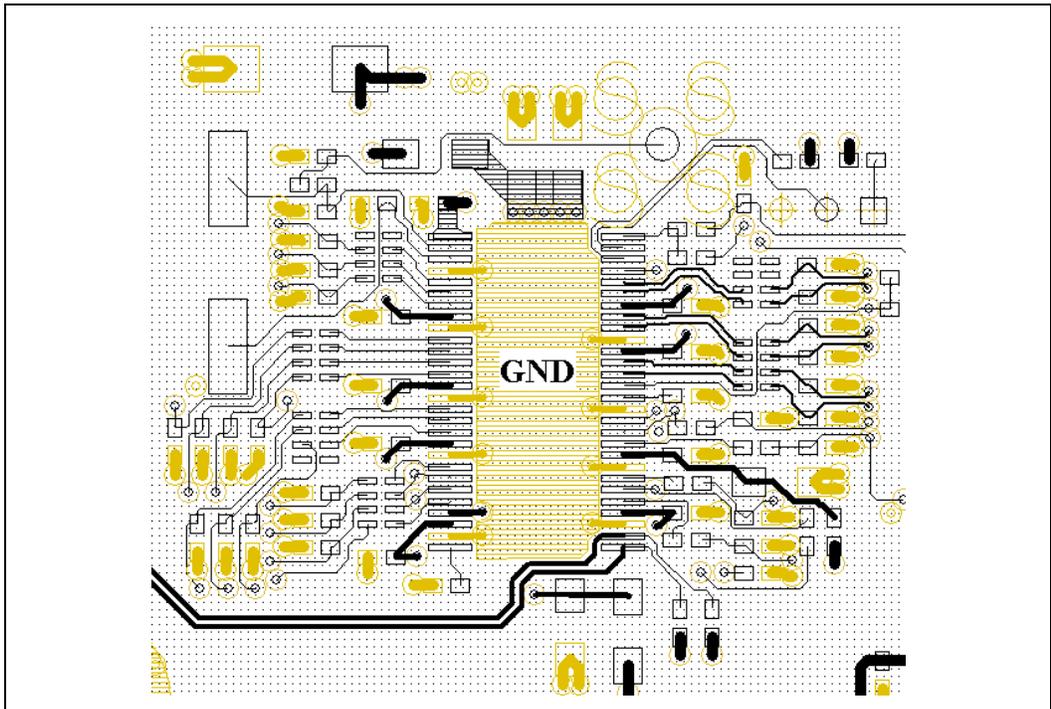
13.3.3 Flooding

13.3.3.1 Option 1. (Signal-Power-Ground-Signal)

For a Signal-Power-Ground-Signal stack up, it is **strongly recommended** that:

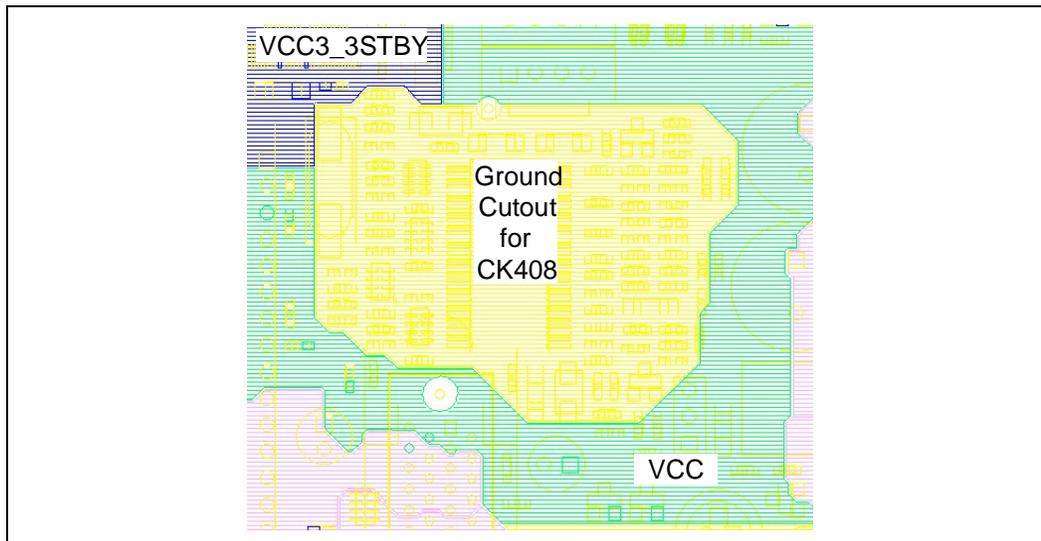
- A solid ground flood be placed on layer 1 (signal layer) inside the part pads

Figure 169. Layer 1 — Ground Flood on Signal Layer



NOTE: A solid ground flood must be placed on layer 2 (power layer) to maintain ground referencing for critical signals.

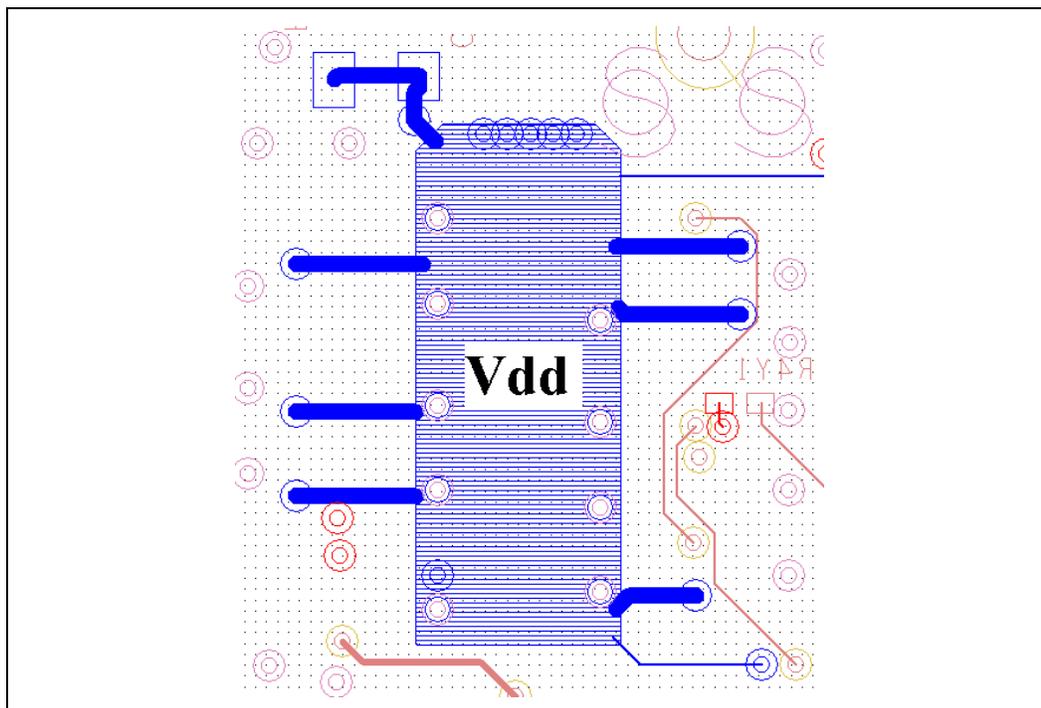
Figure 170. Layer 2 — Ground Flood on Power Layer



NOTES:

1. A solid ground plane must be present on layer 3 (ground layer).
2. A solid 3.3 V power flood must be present on layer 4 (signal layer) inside the part pads.

Figure 171. Layer 4 — Power Flood on Signal Layer



NOTE: Signals after termination should via to the backside to be ground referenced on layer 4.

13.3.3.2 Option 2. (Signal-Ground-Power-Signal)

For a Signal-Ground-Power-Signal stack up, it is **strongly recommended** that:

- A ground flood should be present on layer 1 (signal layer) inside the part pads.
- A solid ground plane be present on layer 2 (ground layer).
- A solid 3.3 V Power plane be present on layer 3 (power layer).
- Signals after termination remain on the top layer to be ground referenced. (via to the front side).

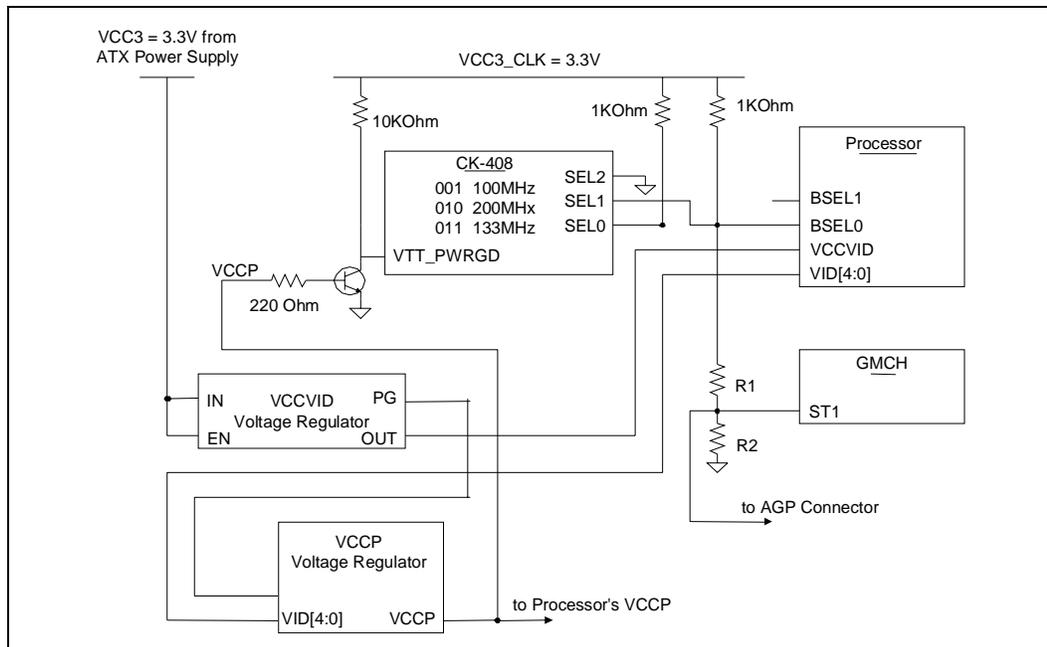
13.3.4 Clock Chip Decoupling

- For ALL power connections to planes, decoupling caps and vias, the MAXIMUM trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance.
- The VSS pins should not be connected directly to the VSS side of the caps. They should be connected to the ground flood under the part which is via'd to the ground plane to avoid Vdd glitches propagating out, getting coupled through the decoupling caps to the VSS pins. This method has been shown to provide the best clock performance.
- The ground flood should be via'd through to the ground plane with no less than 12 – 16 vias under the part. It should be well connected.
- For all power connections, heavy duty and/or dual vias should be used.
- It is imperative that the standard signal vias and small traces not be used for connecting decoupling caps and ground floods to the power and ground planes.

13.3.5 CK-408 Power Sequencing

Platforms need proper power sequencing of the CK-408 with respect to the voltage regulators, processor, and GMCH. Figure 172 is a schematic showing the relationship between the VCCVID voltage regulator, the VCCP voltage regulator, CK-408, processor, and GMCH

Figure 172. CK-408, VREG, Intel® GMCH and Processor Interconnectivity



13.3.6 CK-408 Power Plane Filtering

13.3.6.1 Vdd Plane Filtering

The Vdd decoupling requirements for a CK-408 compliant clock synthesizer are as follows:

- One 300 Ω (@ 100 MHz) Ferrite Bead is recommended for the Vdd plane.
- 10 μF of bulk decoupling in a 1206 package, placed close to the Vdd generation circuitry, is recommended for the Vdd plane. Although a 10 μF capacitor is recommended, (2) 4.7 μF capacitors can be used in place of a single 10 μF capacitor. It is also recommended that the capacitor be placed as close to the Vdd generation circuitry as possible.
- Seven 0.1 μF high frequency decoupling caps in 0603 packages are recommended for the Vdd plane. It is recommended that one capacitor be placed as close to each Vdd pin as possible.

13.3.6.2 VddA Plane Filtering

The VddA decoupling requirements for a CK-408 compliant clock synthesizer are as follows:

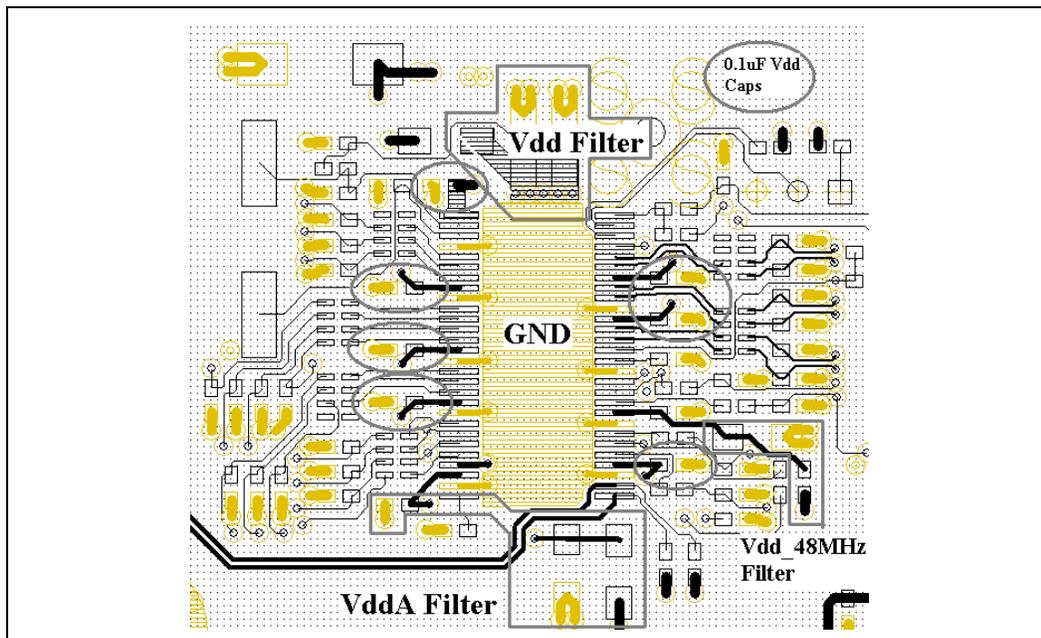
- (1) 300 Ω (@ 100 MHz) Ferrite Bead is recommended for the VddA plane.
- 10 μF of bulk decoupling in a 1206 package, placed close to the VddA generation circuitry, is recommended for the VddA plane. Although a 10 μF capacitor is recommended, (2) 4.7 μF capacitors can be used in place of a single 10 μF capacitor. It is also recommended that the capacitor be placed as close to the VddA generation circuitry as possible.
- (1) 0.1 μF high frequency decoupling caps in 0603 packages are recommended for the Vdd plane. It is recommended that one capacitor be placed as close to each Vdd pin as possible.

13.3.6.3 Vdd_48MHz Plane Filtering

The Vdd_48MHz decoupling requirements for a CK-408 compliant clock synthesizer are as follows:

- (1) 10 Ω (5%) series resistor is recommended for the Vdd_48MHz plane.
- (1) 4.7 μF bulk-decoupling cap in a 1206 package is recommended for the Vdd_48MHz plane. It is also recommended that the capacitor be placed as close to the Vdd_48MHz generation circuitry as possible.
- (1) 0.1 μF high frequency decoupling caps in 0603 packages are recommended for the Vdd_48MHz plane. It is recommended that one capacitor be placed as close to each Vdd_48MHz pin as possible.

Figure 173. Decoupling Capacitors Placement and Connectivity





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14 Platform Power Guidelines

This chapter presents the power guidelines for an 845G chipset platform. Power delivery architecture, power supply decoupling, power sequencing and power management are covered. Table 98 defines some of the terms used in this chapter.

Table 98. Power Terms and Definitions

Term	Definition
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered.
Full-power operation	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state and the S1 (processor stop-grant state) state.
Suspend operation	During suspend operation, power is removed from some components on the motherboard. The customer reference board supports three suspend states: Suspend-to-RAM (S3), Suspend-to- Disk (S4), and Soft-off (S5).
Power rails	An ATX power supply has 6 power rails: +5 V, -5 V, +12 V, -12 V, +3.3 V, 5 Vsb. In addition to these power rails, several other power rails are created with voltage regulators.
Core power rail	A power rail that is only on during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX 12 V power supply are +5 V, -5 V, +12 V, -12 V, +3.3 V.
Standby power rail	A power rail that in on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is: 5Vsb (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived power rail	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3Vsb is usually derived (on the motherboard) from 5Vsb using a voltage regulator.
Dual power rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during suspend operation and derived from a core supply during full-power operation. Note that the voltage on a dual power rail may be misleading.

14.1 Power Delivery Map

Figure 174 shows the power delivery architecture for an example 845G chipset platform. This power delivery architecture supports the “Instantly Available PC Design Guidelines”.

During STR, only the necessary devices are powered. These devices include: main memory, the ICH4 resume well, PCI wake devices (via 3.3 Vaux), AC’97, and USB. To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device power requirements, both in *suspend* and in *full-power*. The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create *dual* power rails.

The solutions in this Design Guide are only examples. Many power distribution methods achieve the similar results. When deviating from these examples, it is critical to consider the effect of a change.

Figure 174. Intel® 845G Chipset DDR Platform Power Delivery Map

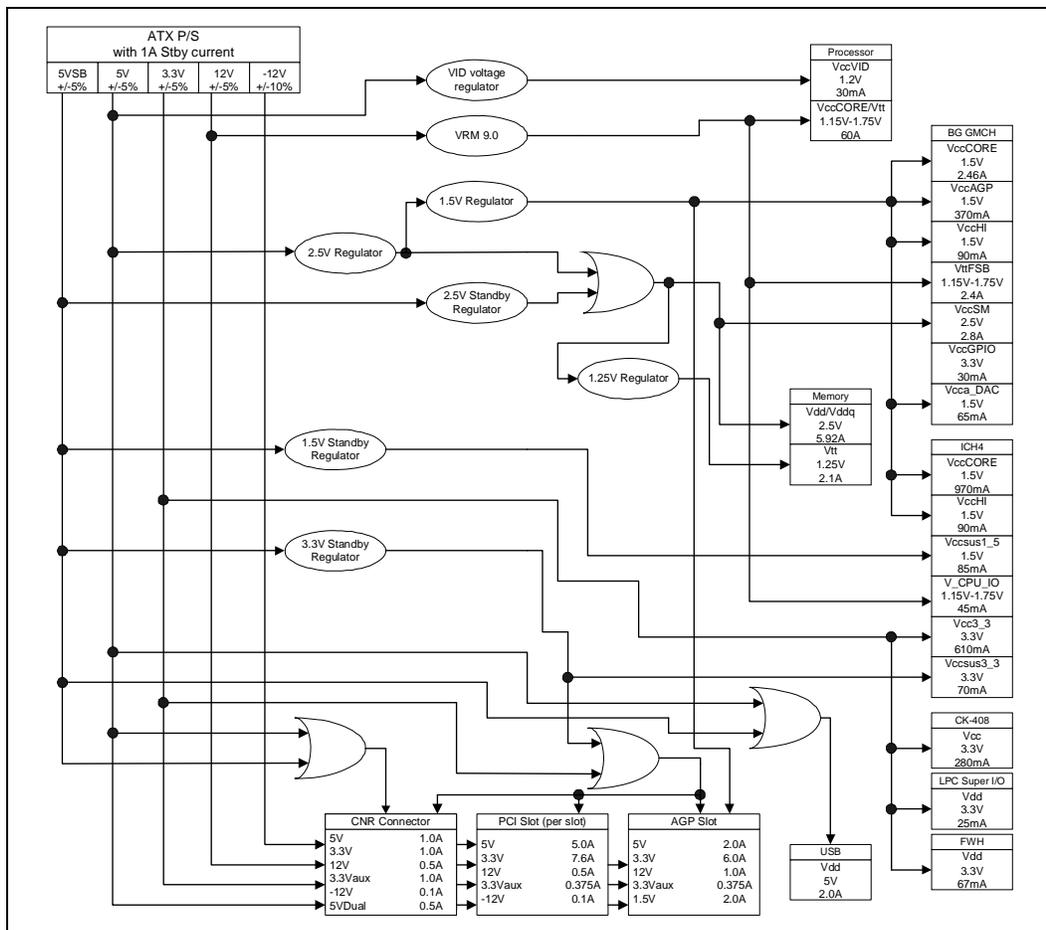
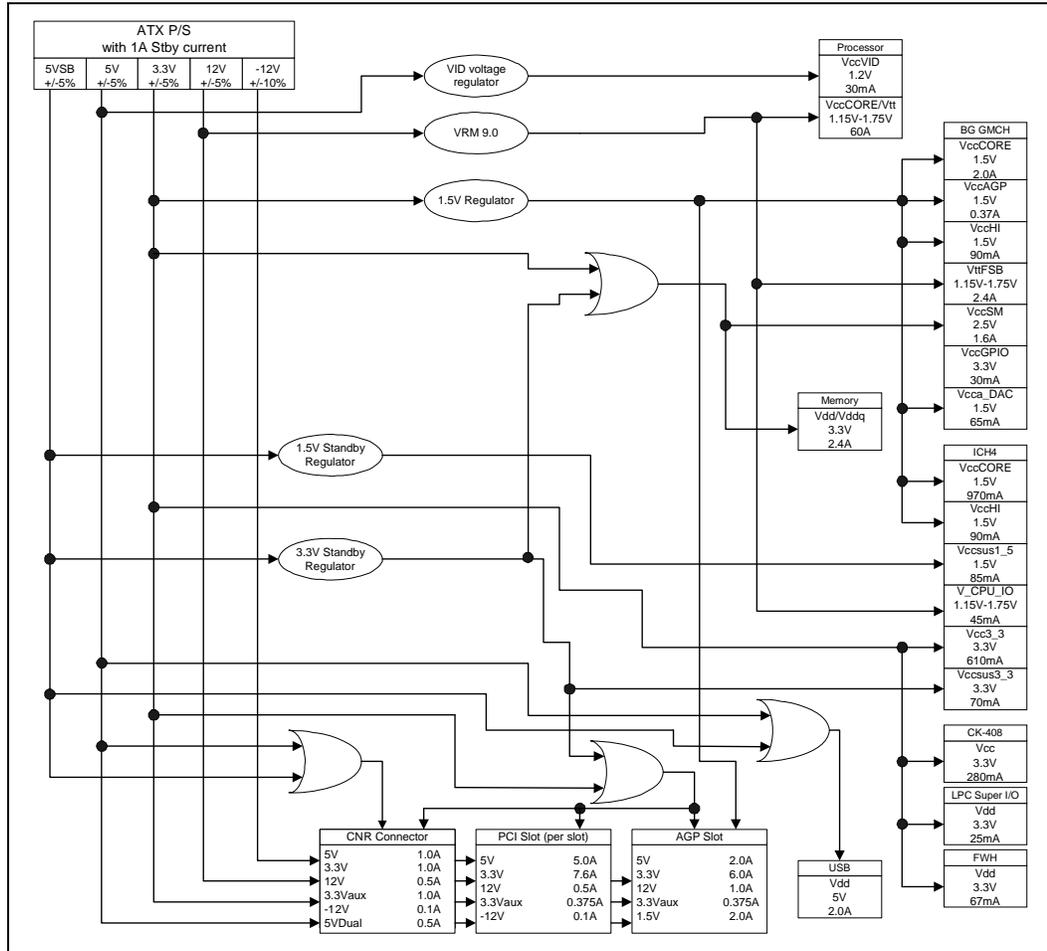


Figure 175. Intel® 845G Chipset SDR Platform Power Delivery Map



14.2 Intel® GMCH Power Delivery and Decoupling

14.2.1 Power Sequencing

There are no GMCH power sequencing requirements; however, the following must be observed:

- GCLKIN must be valid at least 10 us prior to the rising edge of PWROK
- HCLKN/HCLKP must be valid at least 10 us prior to the rising of RSTIN#

Good design practice would have all power rails come up as close in time as practical.



14.2.2 Intel® GMCH Analog Power Delivery

There are five analog circuits that require filtered supplies on the GMCH. They are: VCCQSM, VCCASM, VCCA_DAC, VCCA_DPLL, and VCCA_FSB. VCCQSM and VCCASM have different requirements when the GMCH is in DDR mode versus SDR mode. VCCA_DAC does not require an LC filter. It must be connected directly to the 1.5 V power plane through a trace. Its decoupling requirements are listed in Table 101.

Figure 176. Example Analog Supply Filter for VCCQSM, VCCASM, VCCA_DPLL, and VCCA_FSB

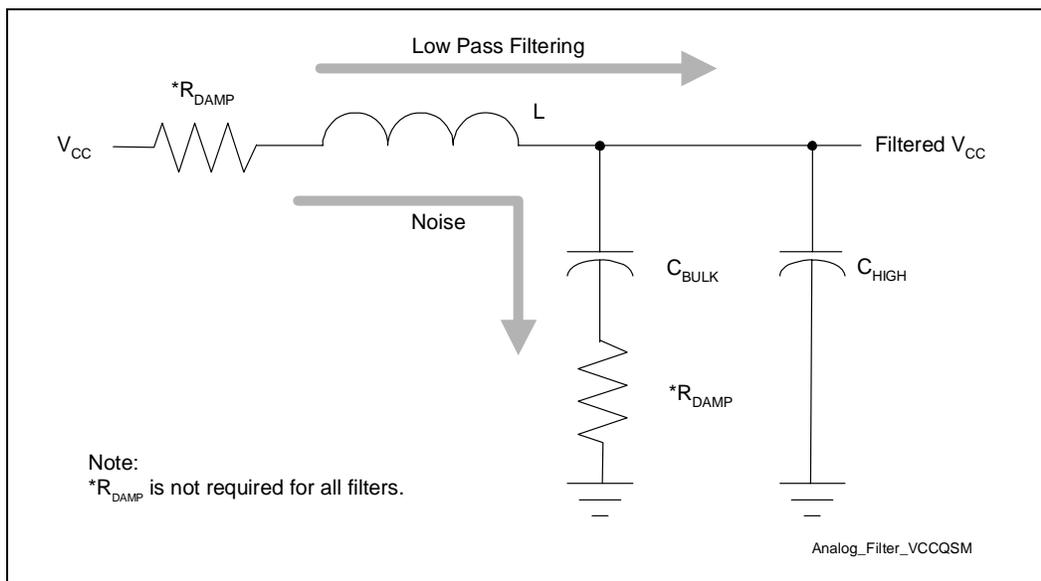


Figure 177. Filter Characteristics

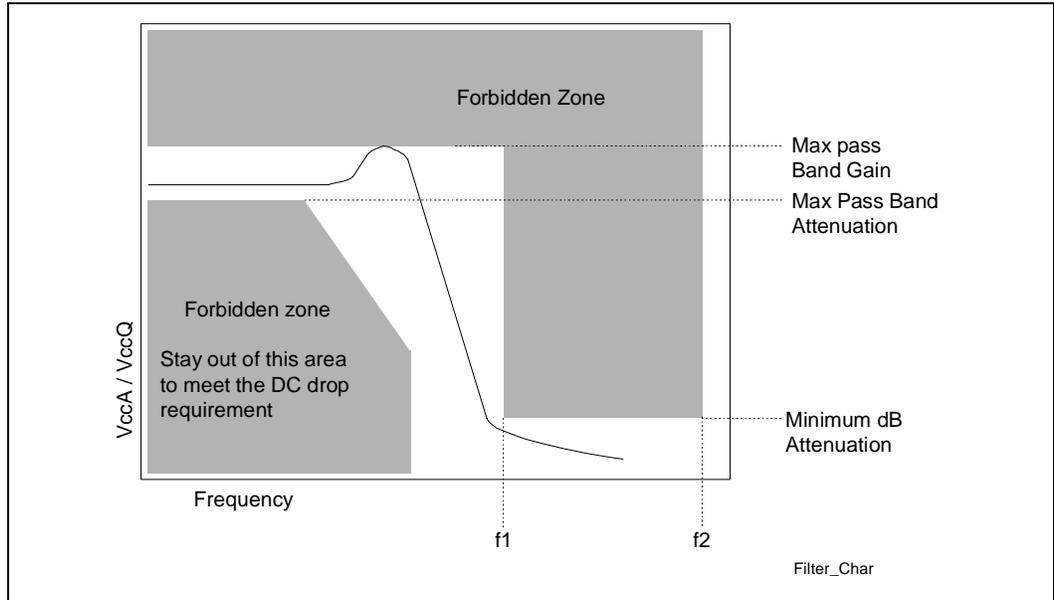


Table 99. Filter Requirements

Required Intel® 845G Chipset Filters	Filter Current Capability (mA)	Filter DC Resistance (Ohms) ¹	Max DC Drop (mV) ²	Pass Band Gain (dB)	f1	f2	Attenuation From f1 to f2 (dB)
VCCA_DPLL	35	2	70	<+0.2, >-0.5	10 kHz	1 MHz	-20
VCCQSM – SDR	50	3.2	160	<+0.2, >-0.5	50 MHz	133 MHz	-30
VCCASM – SDR	200	0.35	70	<+0.2, >-0.5	50 MHz	133 MHz	-30
VCCQSM – DDR	150	0.8	120	<+0.2, >-0.5	50 MHz	133 MHz	-30
VCCASM – DDR	500	0.14	70	<+0.2, >-0.5	50 MHz	266 MHz	-30
VCCA_FSB	30	2.3	70	<+0.2, >-0.5	50 MHz	533 MHz	-30

NOTES:

1. Filter DC resistance is the inductor resistance + MB routing resistance
2. DC drop across filter includes voltage drop across the inductor and across the MB trace

Table 100. Recommended Filter Components

Required Intel® 845G chipset Filters	Rdamp	Rdamp Location	L	Cbulk	Chigh
VCCA_DPLL	1 Ω	In series with inductor	0805 10uH	680 μF	0603 0.1 μF X5R (empty)



VCCQSM – SDR	1 Ω	In series with capacitor	0603 0.27uH	1206 4.7 μ F X5R	0603 0.1 μ F X5R
VCCASM – SDR	none	N/A	1210 4.7 uH DCRmax 0.169 Ω s	100 μ F AIEI	0603 0.1 μ F X5R
VCCQSM – DDR	1 Ω	In series with capacitor	0805 0.68 uH DCRmax 0.80 Ω s	1206 4.7 μ F X5R	0603 0.1 μ F X5R
VCCASM – DDR	none	N/A	1210 1uH DCRmax 0.078 Ω s	100 μ F AIEI	0603 0.1 μ F X5R
VCCA_FSB	none	N/A	0603 0.82uH	22 μ F AIEI	0603 0.1 μ F X5R

14.2.3 Intel® GMCH Power Delivery

Power is delivered to the GMCH through three different layers: layer 1, layer 2, and layer 4.

Figure 178. Intel® GMCH DDR Layer 1 Power Delivery

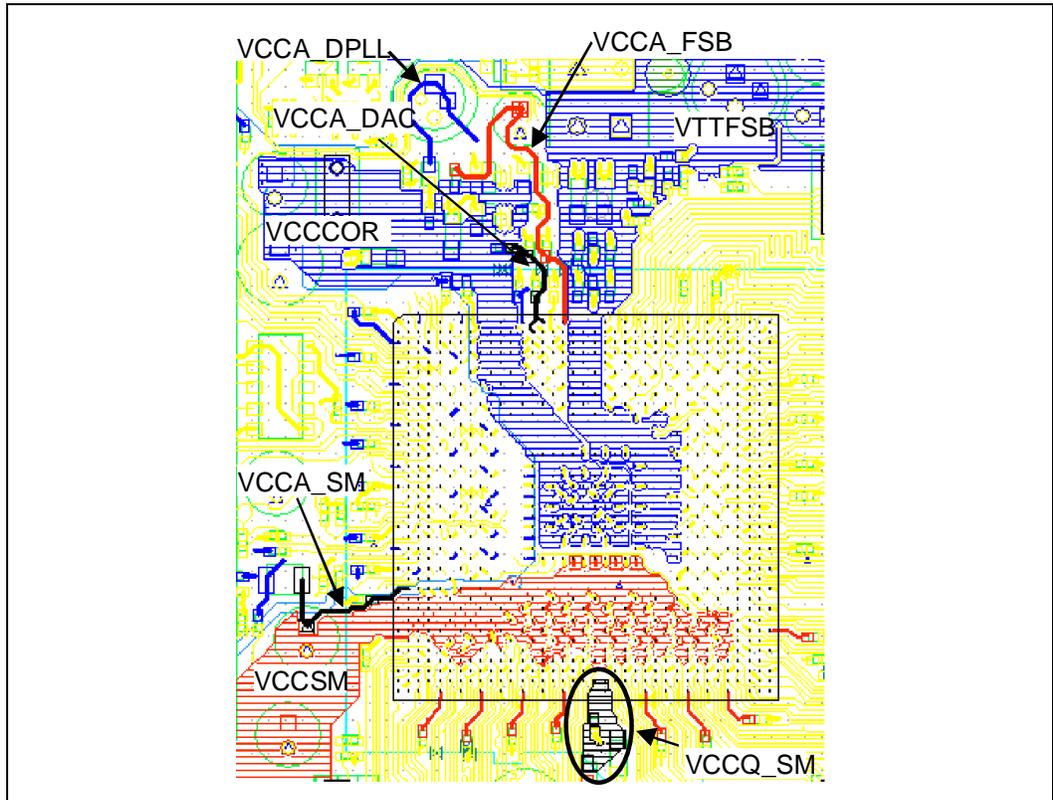




Figure 179. Intel® GMCH DDR Layer 2 Power Delivery

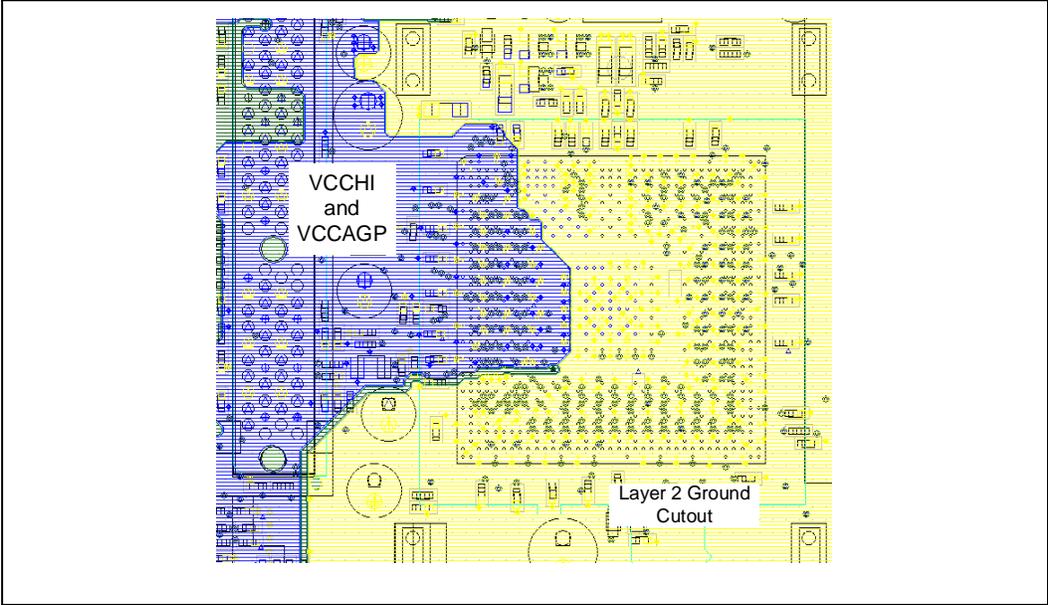


Figure 180. Intel® GMCH DDR Layer 4 Power Delivery

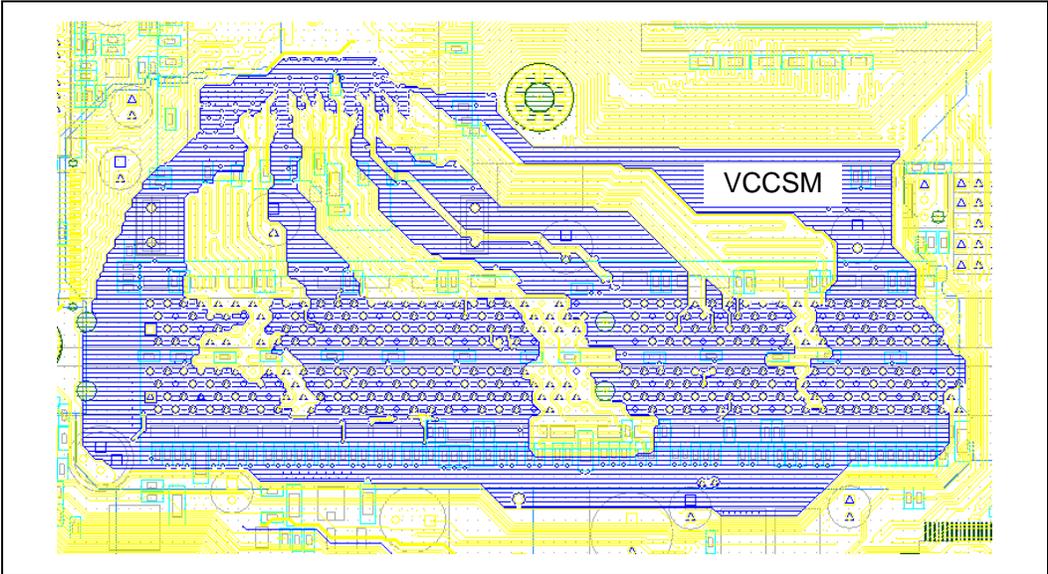


Figure 181. Intel® GMCH SDR Layer 1 Power Delivery

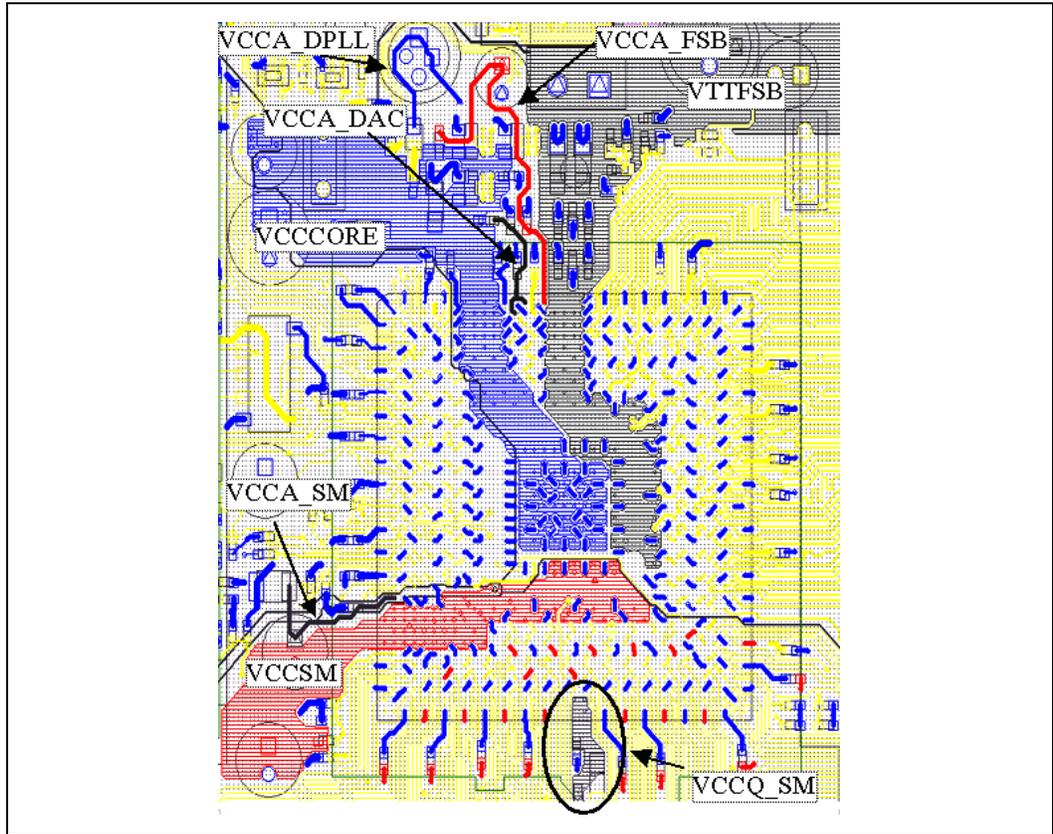


Figure 182. Intel® GMCH SDR Layer 2 Power Delivery

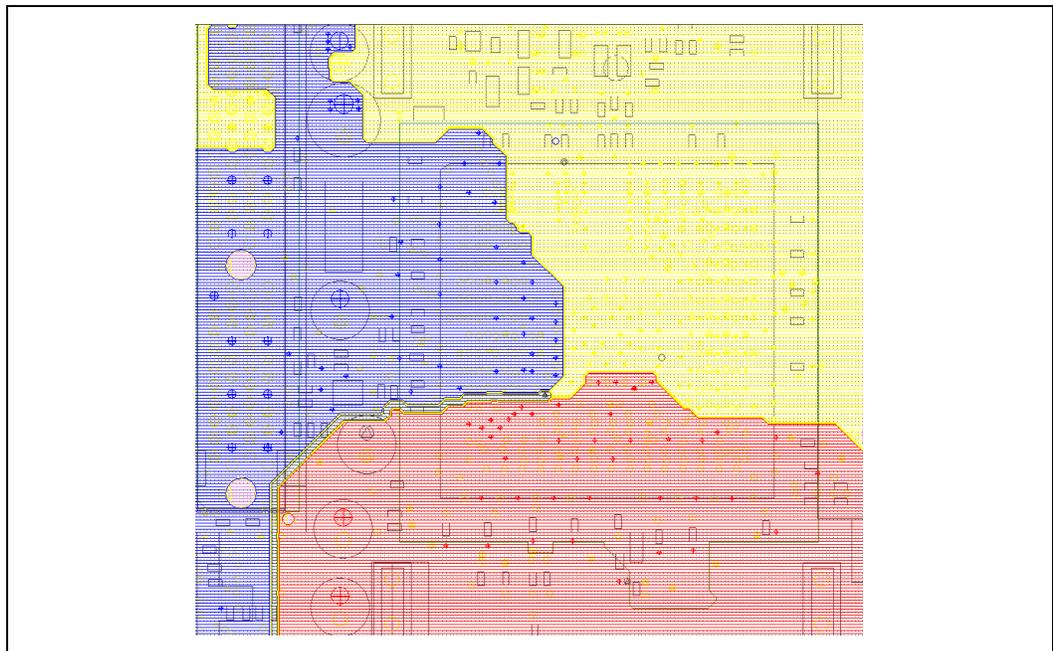
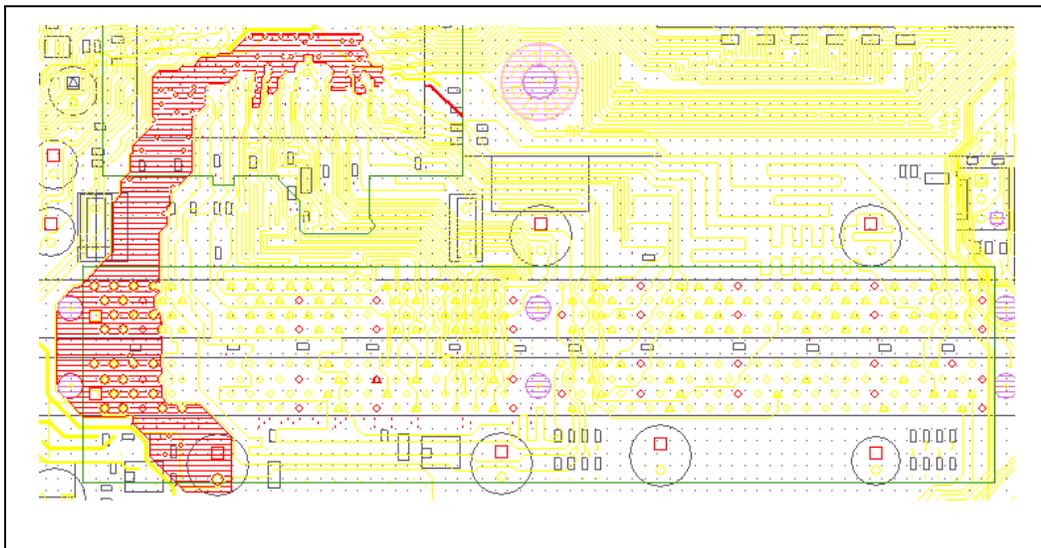
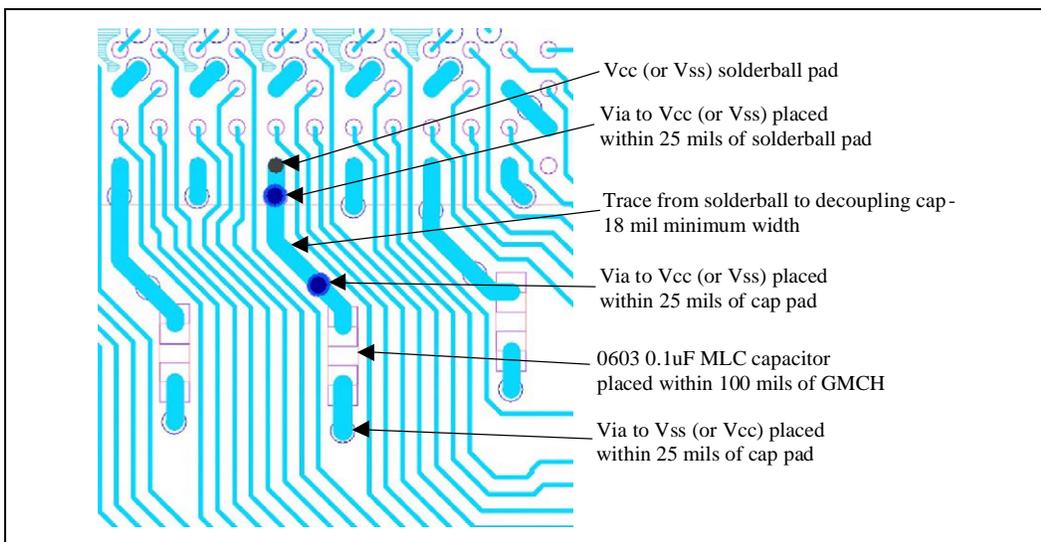


Figure 183. Intel® GMCH SDR Layer 4 Power Delivery



14.2.4 Intel® GMCH Decoupling

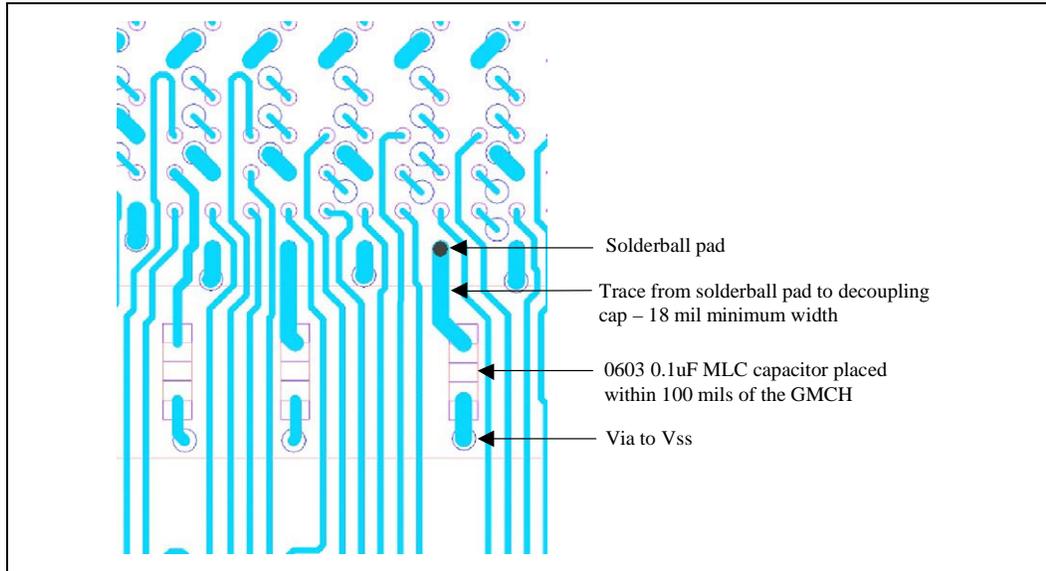
Figure 184. Example Decoupling Capacitor



NOTES:

1. Decoupling capacitors placed in/by a power corridor do not require the vias between the solder ball and the capacitor pad all other decoupling capacitors require the vias to the appropriate power or ground plane.
2. If the trace from the solder ball to the capacitor is less than 100 mils, one of the two vias may be omitted.

Figure 185. Example Edge Cap



NOTE: There **must not** be any vias placed in the trace leading from the solder ball pad to an edge capacitor.

Table 101. High Frequency Decoupling Requirements for Intel® 82845G GMCH

Pin	Decoupling Requirements	Decoupling Type (Ball Type)	Decoupling Placement ¹
VTT_DECAP	(5) 0.1 μ F	Edge Cap ²	Place near balls: AC37, R37, L37, G37, and A31
VTTFSB	(5) 0.1 μ F	Decoupling Cap (VTT)	Place within 250 mils of the package in the VTT corridor
VCC	(1) 0.1 μ F	Decoupling Cap (VCC)	Place within 100 mils of the package in or near the VCC corridor
VCCAGP	(5) 0.1 μ F	Decoupling Cap (VSS)	Place near balls: A5, E1, J1, N1, and U1
VCCHI	(2) 0.1 μ F	Decoupling Cap (VSS)	Place near balls: AA1 and AE1
VCCSM	(8) 0.1 μ F	Decoupling Cap (VCC)	Place near balls: AL37, AU5, AU9, AU13, AU17, AU25, AU29, and AU33
VCCA_DAC	(1) 0.1 μ F (1) 0.01 μ F	Decoupling Cap (VCC)	Place near balls: B14 and A15

NOTES:

1. Unless otherwise noted, capacitors should be placed less than 100 mils from the package.
2. Edge Caps **must not** have vias in the trace from the cap to the GMCH solder ball. They also **must not** connect to the motherboard VTT plane.

Figure 186. Intel® GMCH High Frequency Decoupling Capacitor Placement

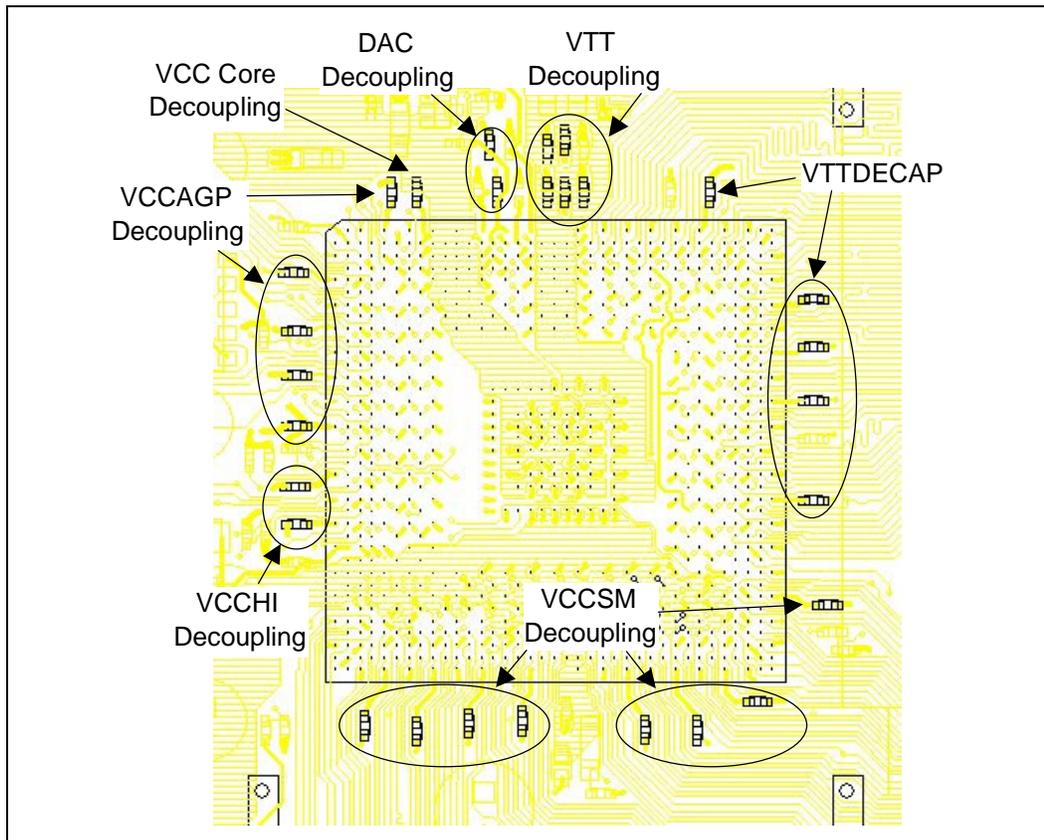


Figure 187. Intel® GMCH Bulk Decoupling Capacitor Placement

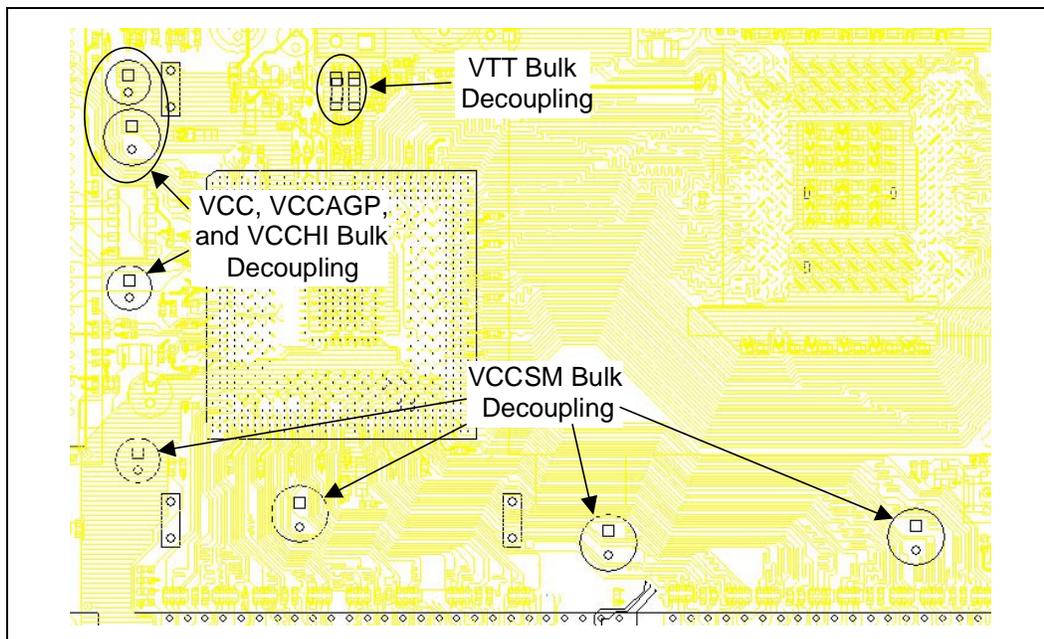


Table 102. Bulk Decoupling requirements for Intel® 82845G GMCH

Plane	Decoupling Requirements	Decoupling Placement
VTTFSB	(2) 10 μ F	Place in VTT power corridor as shown in the above finger
VCC/VCCAGP/VCCHI	(2) 100 μ F (1) 220 μ F	Place between the AGP connector and the GMCH as shown in Figure 187. The 220 μ F and one 100 μ F cap must be placed in the VCC_CORE plane.
VCCSM	(4) 100 μ F	Placed between the GMCH and DIMMs as shown in Figure 187 (one of the capacitors must be placed in the layer one shape)

14.3 Intel® ICH4 Power Delivery and Decoupling

14.3.1 Power Sequencing

14.3.1.1 1.5 V / 3.3 V Power Sequencing

The ICH4 has power sequencing requirements for the 3.3 V and 1.5 V rails in respect to each other. This requirement is as follows: The 1.5 V rail must power up before or simultaneously with the 3.3 V rail. The 3.3 V and 1.5 V rails must power down simultaneously.

The majority of the ICH4 I/O buffers are driven by the 3.3 V supplies but are controlled by logic powered by the 1.5 V supplies. Therefore, another consequence of faulty power sequencing arises when the 3.3 V supply comes up first. In this case, the I/O buffers may be in an undefined state until the 1.5 V logic is powered up. Some signals that are defined as 'Input-only' actually have output buffers that are normally disabled, and the Intel ICH4 may unexpectedly drive these signals when the 3.3 V supply is active while the 1.5 V supply is not.

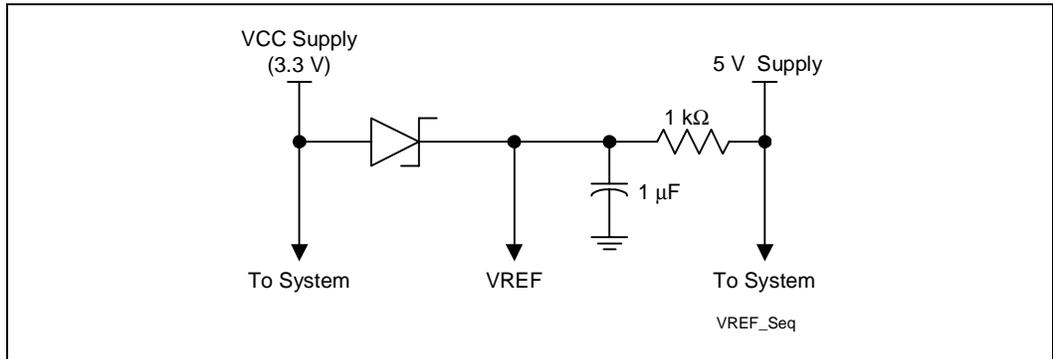
14.3.1.2 3.3 V / V5REF Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH4. V5REF must be powered up before VCC3_3, or after VCC3_3 within 0.7 V. Also, V5REF must power down after VCC3_3, or before VCC3_3 within 0.7 V. This rule must be followed to ensure the safety of the ICH4. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 188 shows a sample implementation of how to satisfy the V5REF/3.3 V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the VccSus3_3 rail is derived from the VccSus5 rail and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

Additionally, the ICH4 requires the V5REF_Sus rail to be hooked to a 5 V sustained source.

Figure 188. Example 3.3 V/V5REF Sequencing Circuitry



14.3.1.3 Power Supply PS_ON Consideration

If a pulse on SLP_S3# or SLP5# is short enough (~ 10 – 100 ms) such that PS_ON is driven active during the exponential decay of the power rails, a few power supply designs may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

The ATX spec does not specify a minimum pulse width on PS_ON deassertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

The platform designer must ensure that this issue does not affect the power supply used with the platform.

14.3.2 Intel® ICH4 Analog Power Delivery

There are no analog ICH4 circuits requiring filters.

14.3.3 Intel® ICH4 Power Delivery

ICH4 Power Delivery is accomplished through layer 1, layer 2, and layer 4.

Figure 189. Intel® ICH4 Layer 1 Power Delivery

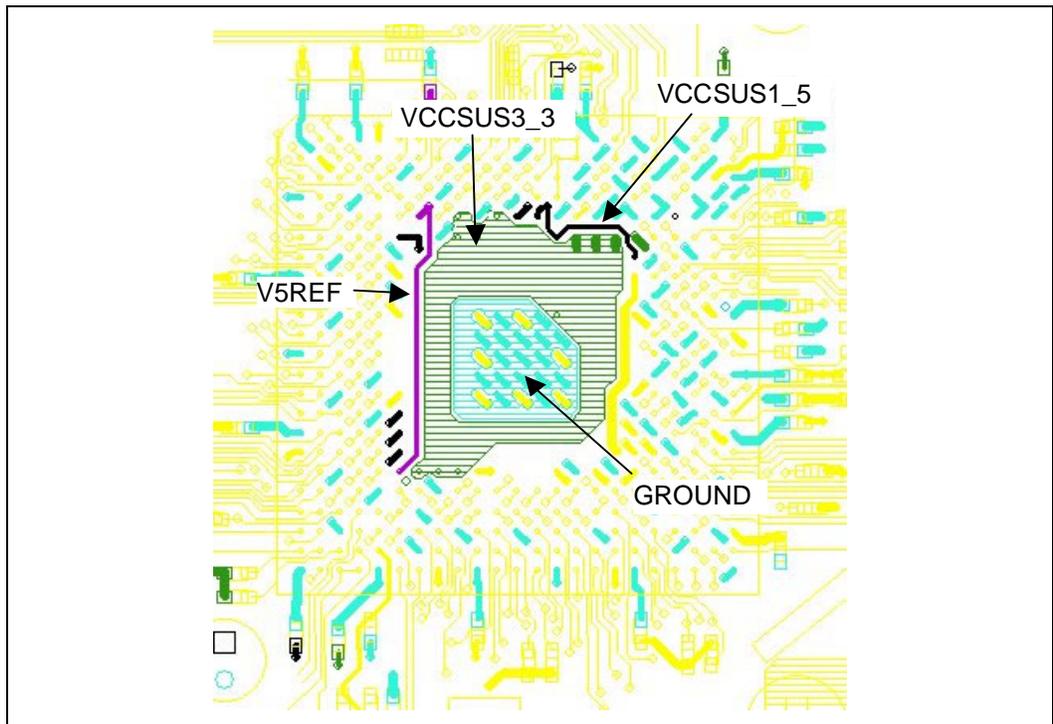




Figure 190. Intel® ICH4 Layer 2 Power Delivery

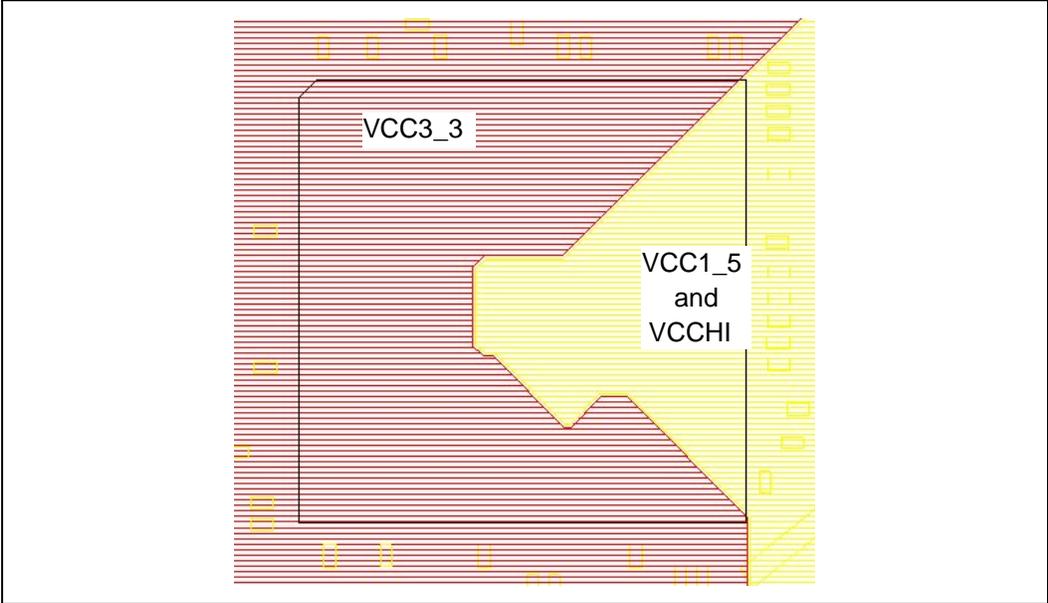
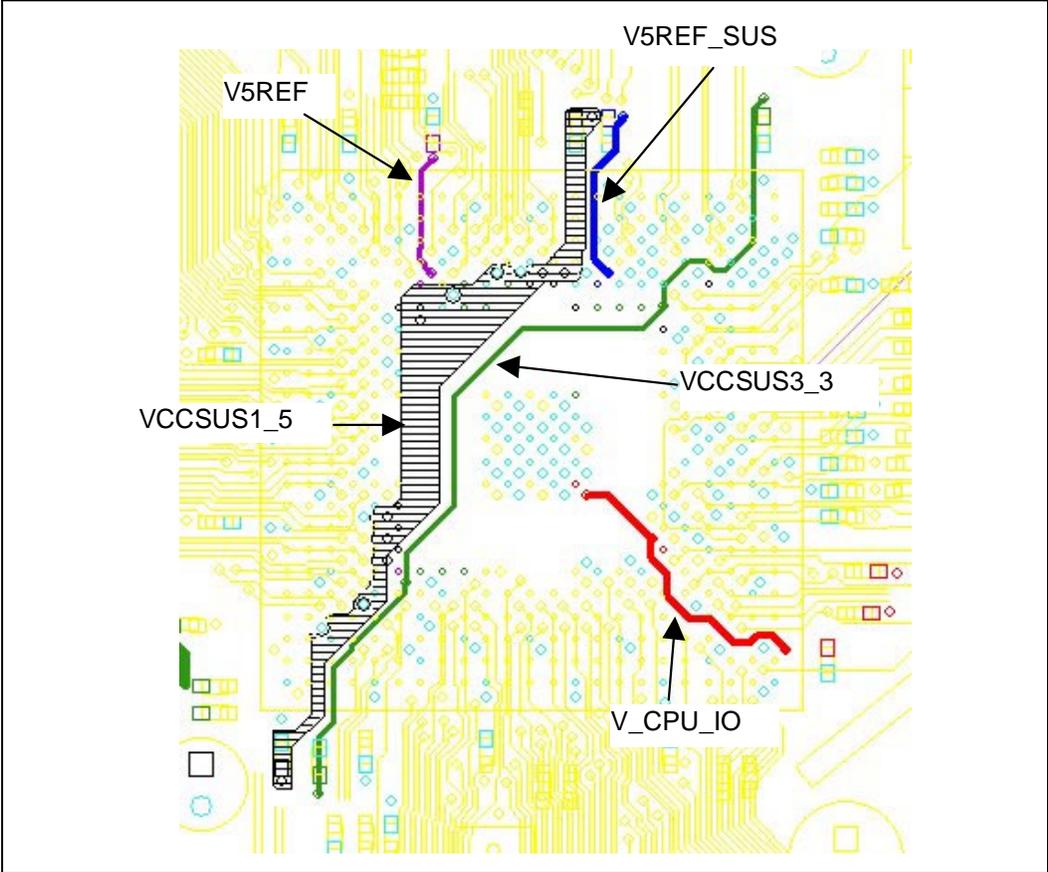


Figure 191. Intel® ICH4 Layer 4 Power Delivery



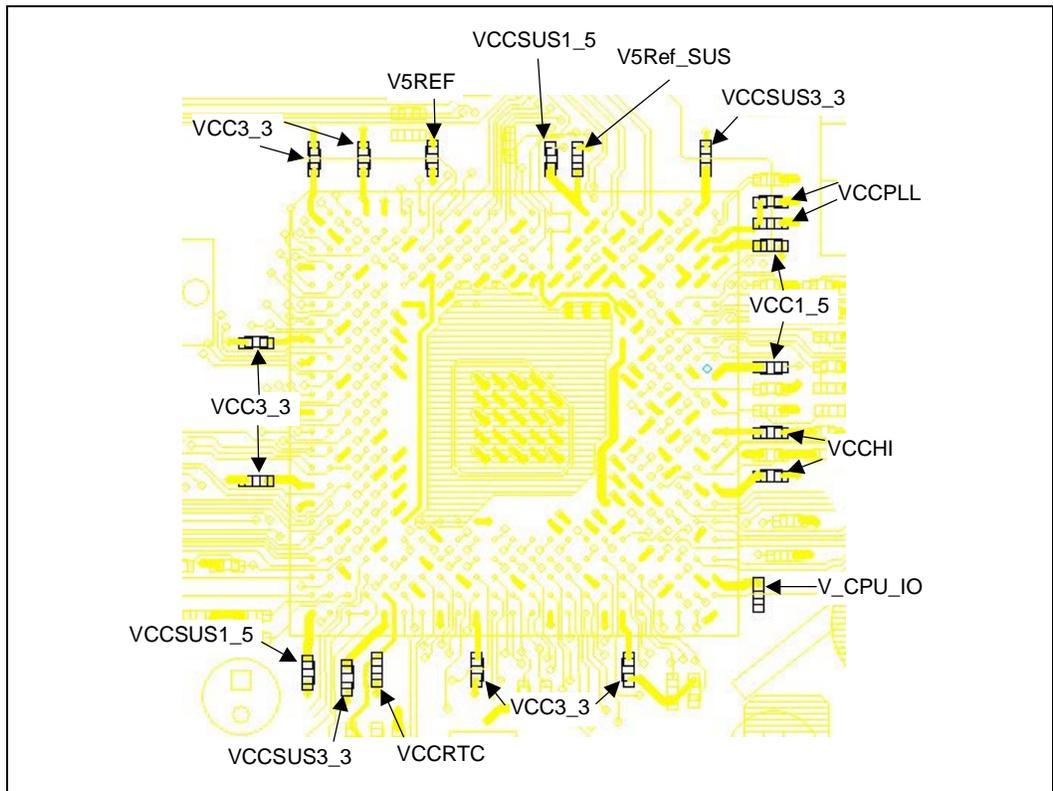
14.3.4 Intel® ICH4 Decoupling

Table 103. Decoupling Requirements for Intel® ICH4

Pin	Decoupling Requirements	Decoupling Type (Ball Type)	Decoupling Placement
VCC3_3	(6) 0.1 μ F	Decoupling Cap (VSS)	Place near balls: A4, A1, H1, T1, AC10, and AC18
VccSus3_3	(2) 0.1 μ F	Decoupling Cap (VSS)	Place near balls: A22 and AC5
V_CPU_IO	(1) 0.1 μ F	Decoupling Cap (VCC)	Place near ball: AA23
VCC1_5	(2) 0.1 μ F	Decoupling Cap (VSS)	Place near balls: K23 and C23
VccSus1_5	(2) 0.1 μ F	Decoupling Cap (VSS)	Place near balls: A16 and AC1
V5REF	(1) 0.1 μ F	Decoupling Cap (VCC)	Place near ball: E7
V5_REF_SUS	(1) 0.1 μ F	Decoupling Cap (VSS)	Place near ball: A16
VCCRTC	(1) 0.1 μ F	Decoupling Cap (VCC)	Place near ball: AB5
VCCHI	(2) 0.1 μ F	Decoupling Cap (VSS)	Place near balls: T23 and N23
VCCPLL	(1) 0.1 μ F (1) 0.01 μ F	Decoupling Cap (VCC)	Place near ball: C22

NOTE: Capacitors should be placed less than 100 mils from the package.

Figure 192. Intel® ICH4 Decoupling Capacitor Placement



14.4 Thermal Design Power

The thermal design power is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus. For 845G chipset package thermal characteristics, refer to the following:

- *Intel® 82801DB I/O Controller Hub 4 (ICH4): Thermal and Mechanical Design Guidelines*
- *Intel® 845G/845GL/845GV Chipset: Intel® 82845G/82845GL/82845GV Graphics and Memory Controller Hub (GMCH) Thermal and Mechanical Design Guidelines*



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15 Platform Mechanical Guidelines

15.1 Intel® GMCH Retention Mechanism and Keep-Outs

Figure 193 shows the motherboard keep-out dimensions intended for the reference thermal/mechanical components for the 845G chipset.

Figure 193. Intel® GMCH Retention Mechanism and Keep-Out Drawing

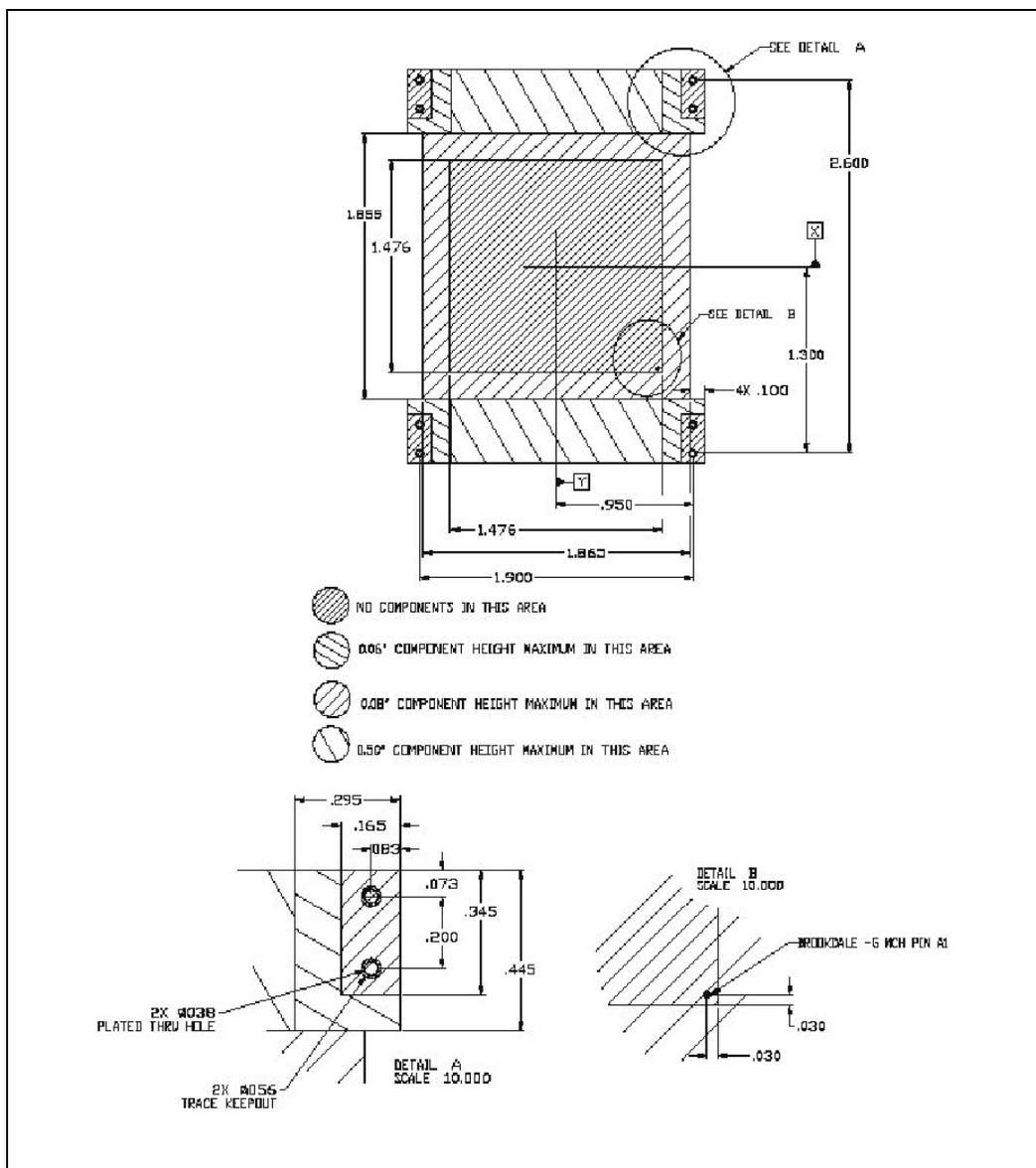
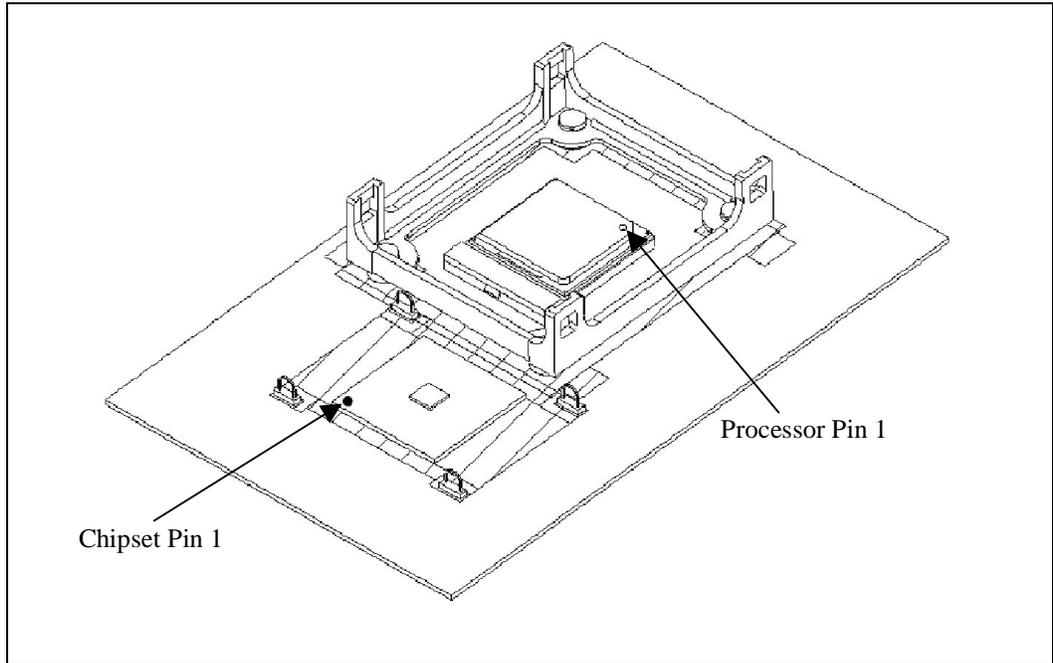


Figure 194. Typical Orientation of the Chipset Relative to the Processor



15.2 Intel® 82845G GMCH Package

Figure 195. Intel® GMCH Package (Bottom View)

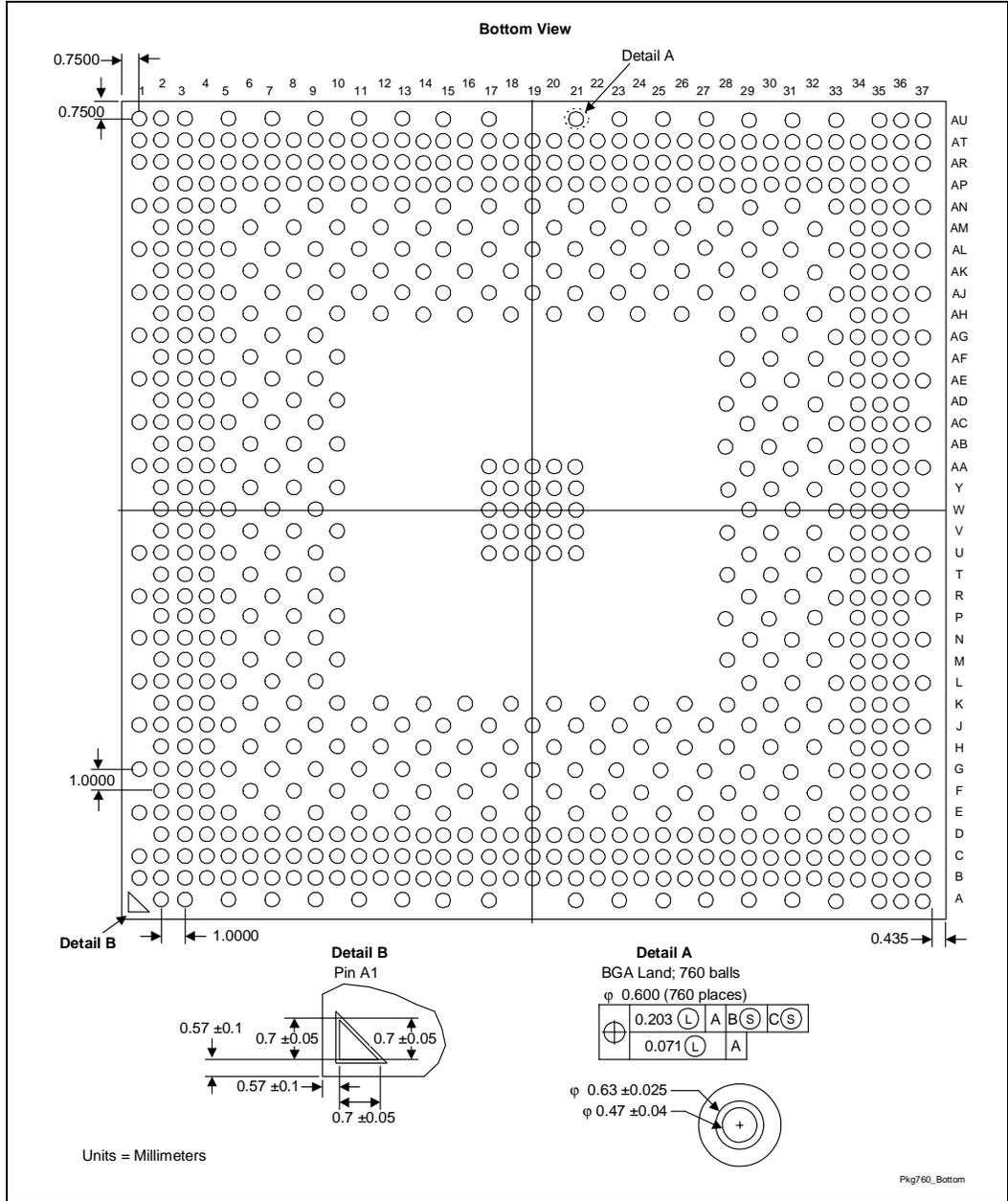
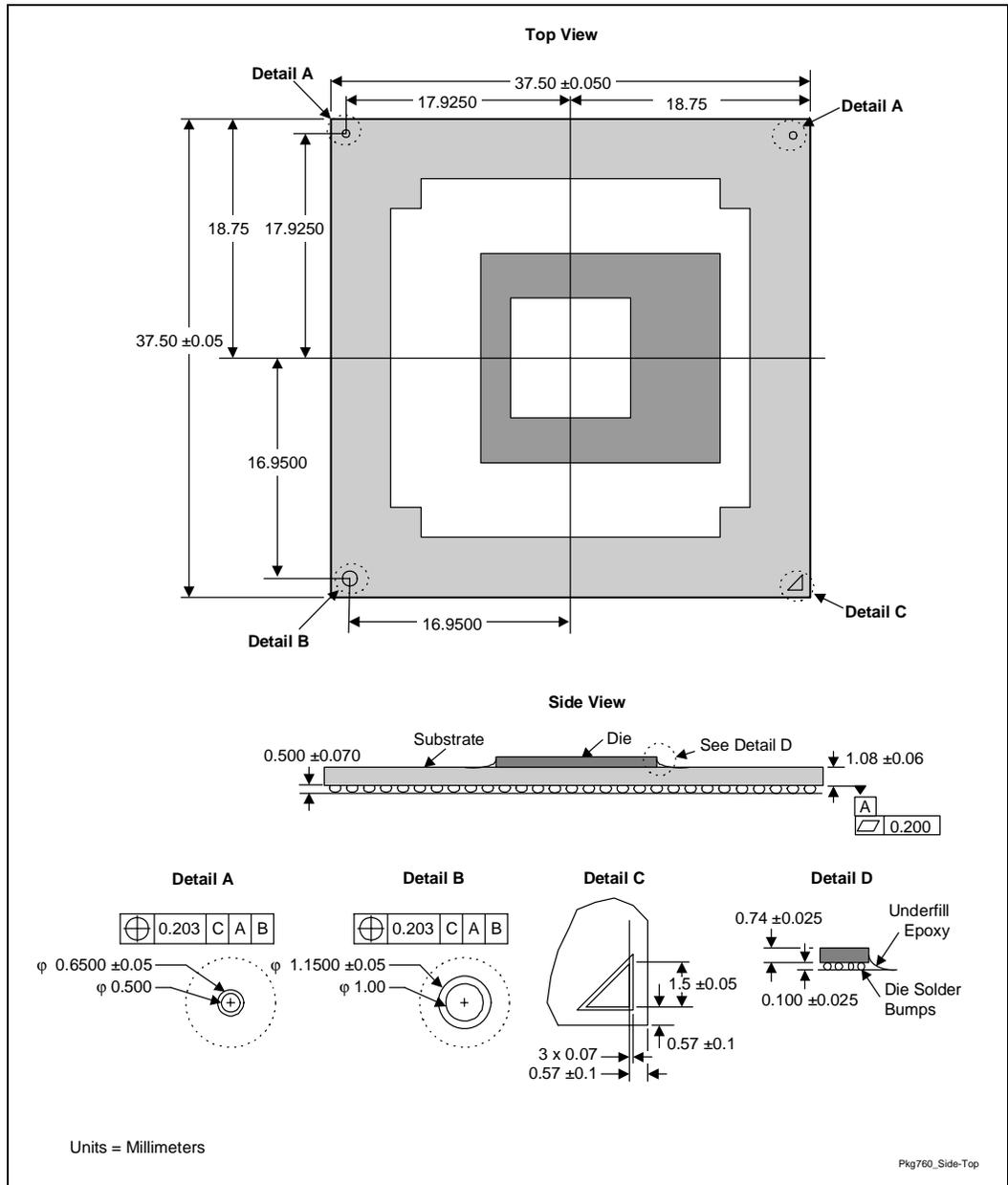


Figure 196. Intel® GMCH Package (Top and Side Views)



16 Signal Routing Reference

This chapter describes routing for the Processor System Bus, System Memory Interface, AGP, Display Interface, Hub Interface, and clocking signals.

16.1 Processor System Bus

Table 104. Processor System Bus Routing

Intel® GMCH	I/O	Type	Plane Ref	Net Width (mils)	Net Spacing (Same Signal Group)	Spacing to other signals (mils)	Min MB length	Max MB length	Associated Strobe	Matching	Topology	Termination	Reference Section							
HA_[16:3]#	I/O	AGTL+	VSS	7	Breakout for a maximum of 250 mils from the component ball with 5 mils spacing. After that, spacing of 13 mils.	20	2"	10"	HADSTB_0#	Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes.	P to P	On Die	4.2.2.1							
HREQ_[4:0]#	I/O	AGTL+	VSS	7					—											
HA_[31:17]#	I/O	AGTL+	VSS	7					HADSTB_1#											
HADSTB_[1:0]#	I/O	AGTL+	VSS	7					—											
HD_[15:0]#	I/O	AGTL+	VSS	7		20	2"	8"	HDSTB_P0#	Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes.	P to P	On Die	4.2.2.1							
DINV_0#	I/O	AGTL+	VSS	7					HDSTB_N0#											
HD_[31:16]#	I/O	AGTL+	VSS	7					HDSTB_P1#											
DINV_1#	I/O	AGTL+	VSS	7					HDSTB_N1#											
HD_[47:32]#	I/O	AGTL+	VSS	7					HDSTB_P2#											
DINV_2#	I/O	AGTL+	VSS	7					HDSTB_N2#											
HD_[63:48]#	I/O	AGTL+	VSS	7					HDSTB_P3#											
DINV_3#	I/O	AGTL+	VSS	7					HDSTB_N3#											
HDSTB_P[3:0]#	I/O	AGTL+	VSS	7					—					20	2"	8"	DSTBN/P# routed to the same length as corresponding data signal mean pad-to-pad length ± 25 mils	P to P	On Die	4.2.2.1
HDSTB_N[3:0]#	I/O	AGTL+	VSS	7					—											
ADS#	I/O	AGTL+	VSS	7		20	3"	10"	—	—	P to P	On Die	—							
BNR#	I/O	AGTL+	VSS	7																
BPRI#	O	AGTL+	VSS	7																
CPURST#	O	AGTL+	VSS	7																
DBSY#	I/O	AGTL+	VSS	7																
DEFER#	O	AGTL+	VSS	7																
DRDY#	I/O	AGTL+	VSS	7																
HIT#	I/O	AGTL+	VSS	7																
HITM#	I/O	AGTL+	VSS	7																
HLOCK#	I	AGTL+	VSS	7																
HTRDY#	O	AGTL+	VSS	7																

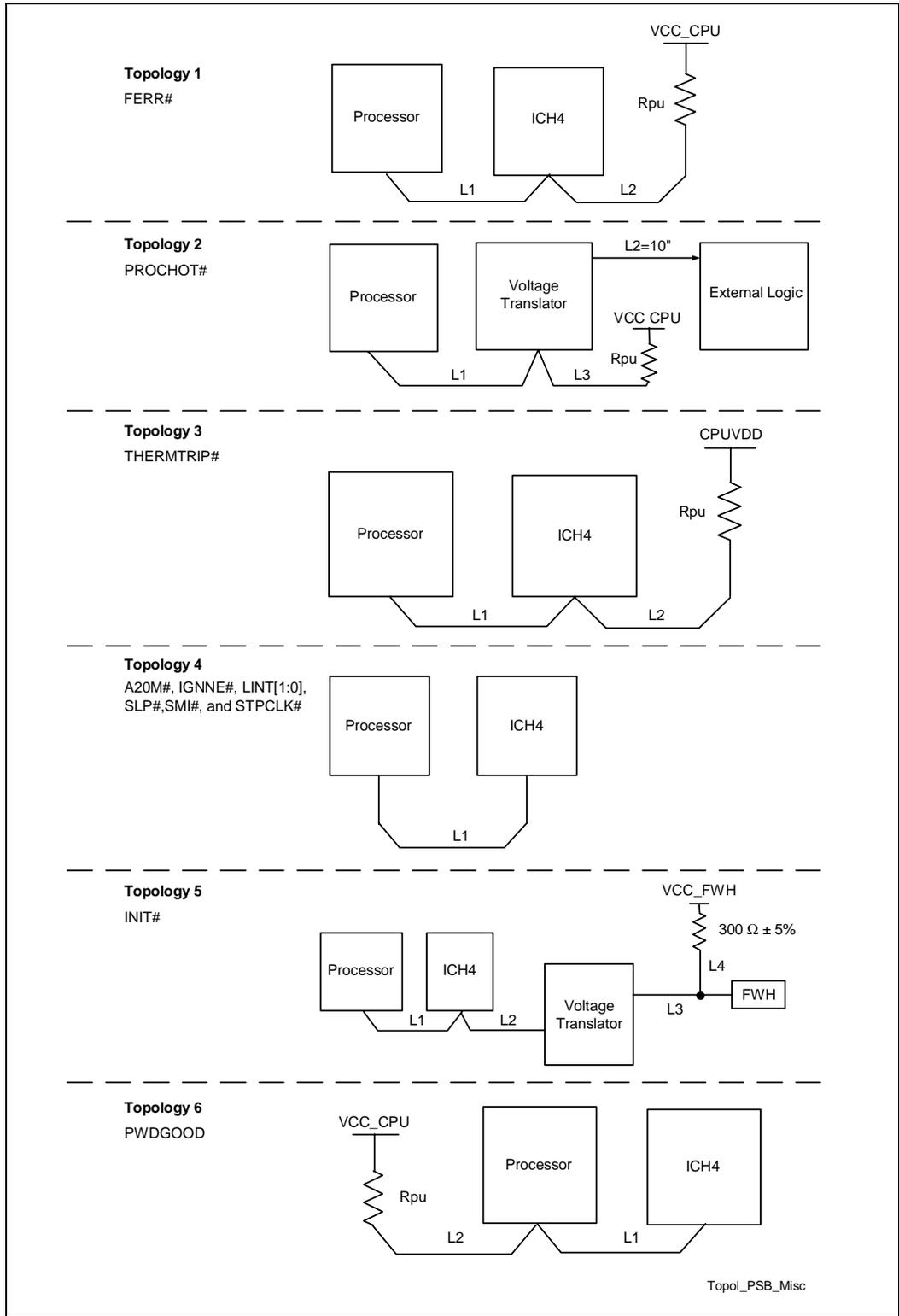


Intel® GMCH	I/O	Type	Plane Ref	Net Width (mils)	Net Spacing (Same Signal Group)	Spacing to other signals (mils)	Min MB length	Max MB length	Associated Strobe	Matching	Topology	Termination	Reference Section
RS[2:0]#	O	AGTL+	VSS	7									

Table 105. Processor System Bus Miscellaneous Signals Routing

Intel® GMCH	I/O	Type	Plane Reference	Net Width (mils)	Spacing to other signals (mils)	Topology	L1		L2	L3	L4	Termination	Reference Section
							Min	Max	Max	Max	Max		
FERR#	O	Asyn GTL+	VSS	7	20	1	1"	12"	3"	—	—	62 Ohm series to VCC_CPU	4.3.1.1
PROCHOT#	O	Asyn GTL+	VSS	7	20	2	1"	17"	10"	3"	—	62 Ohm series to VCC_CPU	4.3.1.2
THERMTRIP#	O	Asyn GTL+	VSS	7	20	3	1"	12"	3"	—	—	62 Ohm series to VCC_CPU	4.3.1.3
A20M#	I	Asyn GTL+	VSS	7	20	4	—	17"	—	—	—	—	4.3.1.4
IGNNE#	I	Asyn GTL+	VSS	7	20		—		—	—	—	—	
LINT0 / INTR	I	Asyn GTL+	VSS	7	20		—		—	—	—	—	
LINT1 / NM		Asyn GTL+	VSS	7	20		—		—	—	—	—	
SLP#	I	Asyn GTL+	VSS	7	20		—		—	—	—	—	
SMI#	I	Asyn GTL+	VSS	7	20		—		—	—	—	—	
STPCLK#	I	Asyn GTL+	VSS	7	20		—		—	—	—	—	
INT#	I	Asyn GTL+	VSS	7	20	—	—	17"	2"	10"	3"	—	4.3.1.5
PWRGOOD	I	Asyn GTL+	VSS	7	20	5	1"	12"	3"	—	—	300 Ohm series to VCC_CPU	4.3.1.6

Figure 197. PSB Miscellaneous Signals Routing Topologies





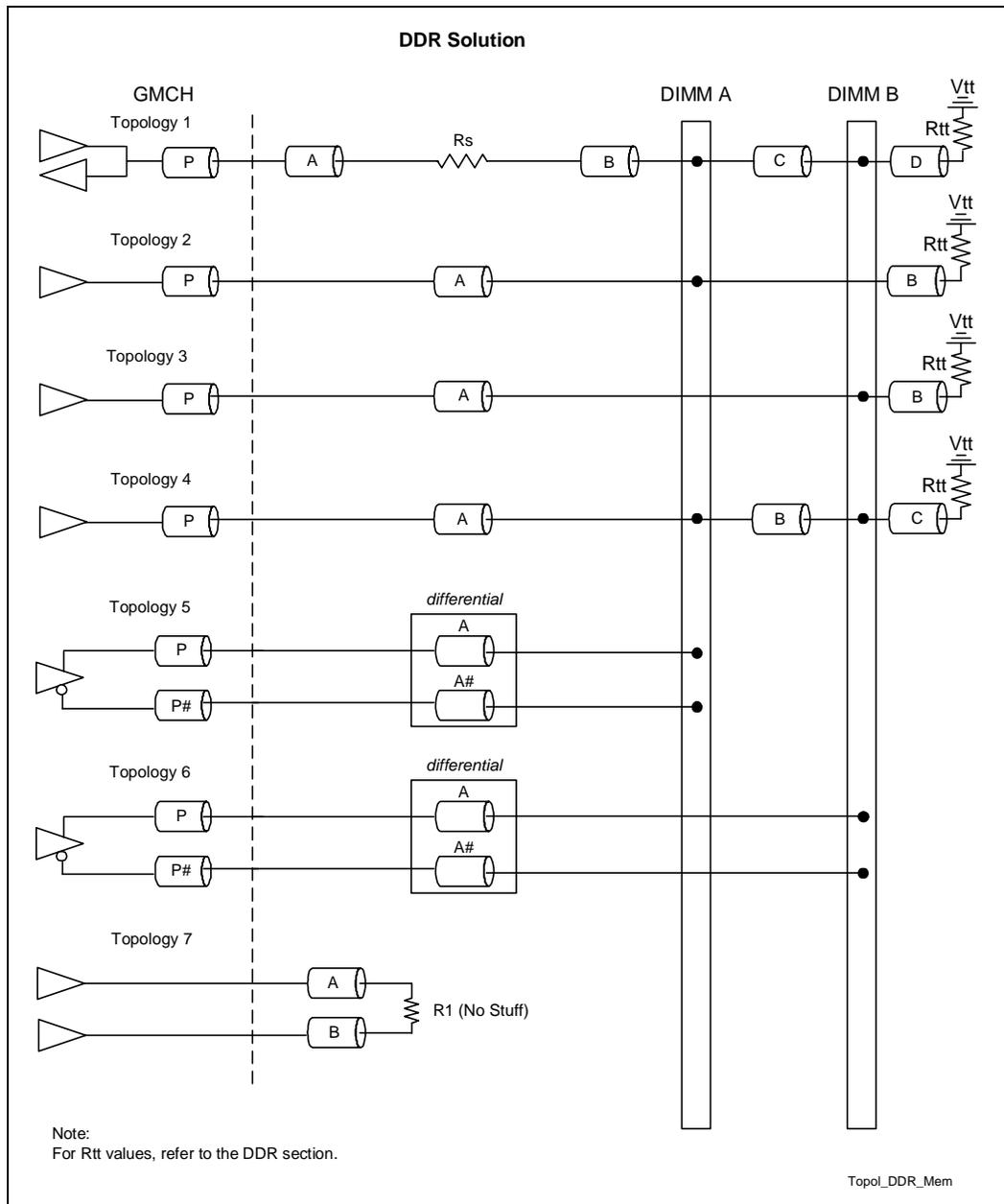
16.2 System Memory Interface

16.2.1 DDR – SDRAM

Table 106. DDR System Memory Interface Routing

Intel® GMCH	I/O	Type	Signal Group	Plane Reference	Layer Target	Nominal Width	Net Spacing (Same Signal Group)	Spacing to other signals (mils)	Topology	A		B		C		D	P	P+A+B	P+A	Intel® GMCH Breakout Guidelines	Length Tuning Method Section	Reference Section						
										Max	Min	Max	Min	Max	Min								Max					
SDQ_[63:0]	I/O	SSTL2	Data	GND	1	5	Table 24	20	1	—	—	0.5"	0.4"	0.6"	0.8"	—	5.8"	—	5 mil width with 6 mil spacing for max of 350 mils	5.2.1.1	5.2.1							
SDQS_[7:0]	I/O									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
SDM_[7:0]	O									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SCS_[1:0]#	O	SSTL2	Control	GND	4	5	Table 26	20	2	3.5"	—	1.4"	—	—	—	—	—	—	—	5 mil width with 6 mil spacing for max of 350 mils	5.2.2.1	5.2.2						
SCKE_[1:0] #	O									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
SCS_[3:2]#	O									3	4.0"	—	0.8"	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SCKE_[3:2]	O									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SMAA_ [12:6,3,0]	O	SSTL2	Addr/ Cmd	GND	4	5	Table 27	20	4	4.0"	0.4"	0.6"	—	0.8"	—	—	—	—	—	5 mil width with 6 mil spacing for max of 350 mils	5.2.3.1	5.2.3						
SBA_[1:0]	O									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
SRAS#	O									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SCAS#	O									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SWE#	O									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SMAA_ [5,4,2,1]	O	SSTL2	CPC Addr	GND	4	5	Table 29	20	2	2.5"	—	1.4"	—	—	—	—	—	—	—	5 mil on 6 mil to the first 200 mils from ball. 5 mil on 8 mil to an additional 550 mils after the first 200 mils from ball	5.2.4.1	5.2.4						
SMAB_ [5,4,2,1]	O									3	3.0"	—	0.8"	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
SCMD CLK[2:0]	O	SSTL2	Clock	GND	4	8	Table 33	20	5	—	—	—	—	—	—	—	—	—	7.4"	5 mil width with 5 mil differential spacing with a min of 5 mils isolation from any other signal for max of 350 mils	5.2.5.1	5.2.5						
SCMD CLK[2:0]#	O									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
SCMD CLK[5:3]	O									6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	7.9"	—	—
SCMD CLK[5:3]#	O									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SRCVEN_ IN#	I	SSTL2	Feed back	GND	4	5	Table 34	10	7	0.1"	—	0.1"	—	—	—	—	—	—	—	N/A	N/A	5.2.6						
SRCVEN_ OUT#	O									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Figure 198. DDR System Memory Routing Topologies



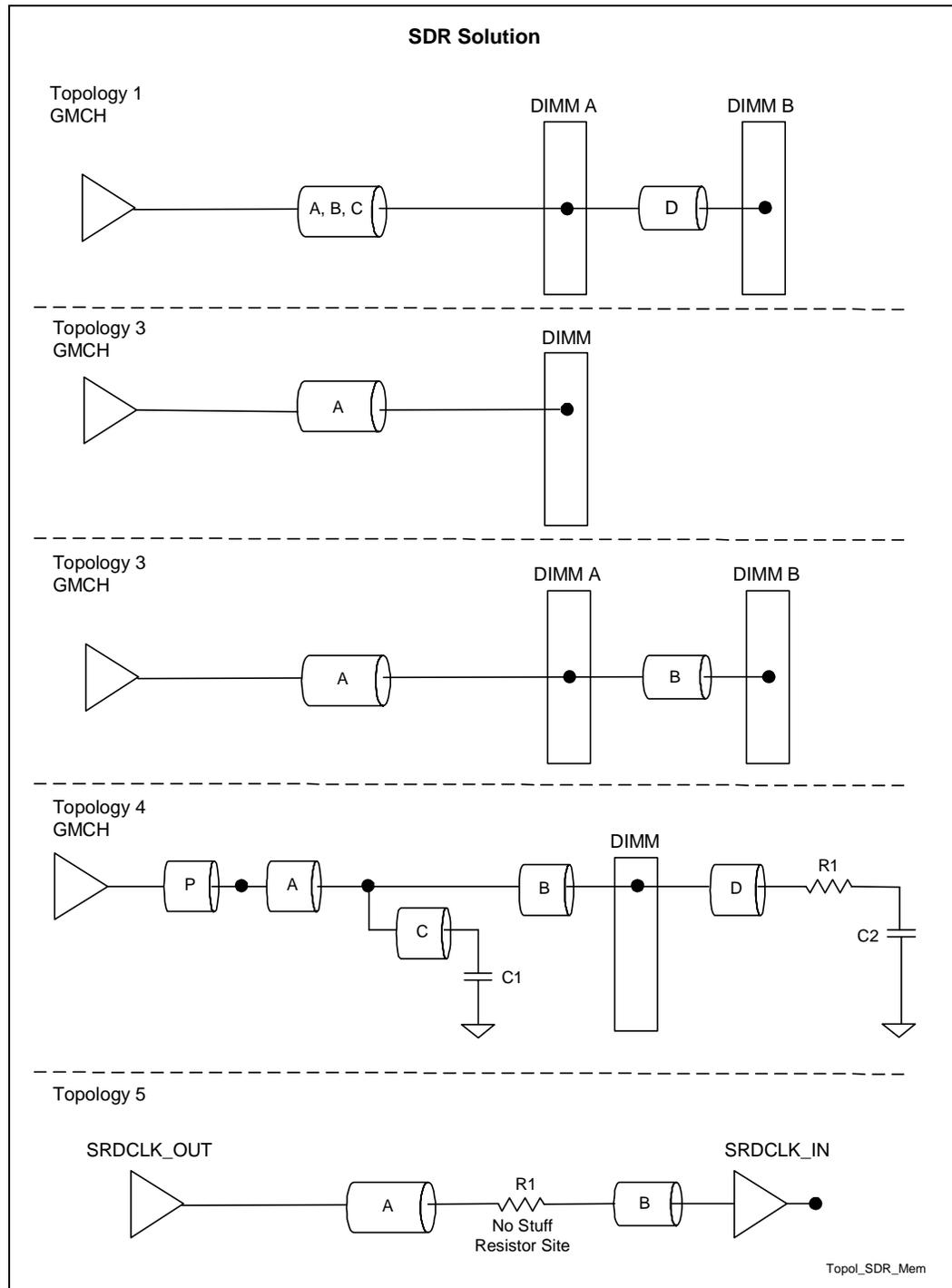


16.2.2 SDR (PC133)

Table 107. SDR System Memory Interface Routing

Intel® GMCH	I/O	Type	Signal Group	Plane Reference	Layer Target	Nominal Width	Net Spacing (Same Signal Group)	Spacing to other signals (mils)	Topology	A		B		C		D		P	P+A+B	Intel® GMCH Breakout Guidelines	Reference Section
										Min	Max	Min	Max	Min	Max	Min	Max				
SDM_[7:0]	I/O	LVTTTL	Data	Single	1	5	12	12	1	2"	4"					0.4"	0.6"	—	—	5 on 5 for max of 0.5"	6.2.1.1
SDQ_[55:40,23:8]	O											2"	4"								
SDQ_[63:56,39:24,7:0]	O											2"	4.4"								
SCS_[7:0]#	O	LVTTTL	Control	Single	1,4	5	12	12	2	3"	4"	—	—	—	—	—	—	—	5 on 5 for a max of 0.5"	6.2.1.2	
SCKE_[3:0]	O					8	12	12													
SMAA_[12:0]	O	LVTTTL	Addr/Cmd	Single	1,4	5	12	12	3	2"	3.5"	0.4"	0.6"	—	—	—	—	—	—	5 on 5 for a max of 0.5"	6.2.1.3
SBA_[1:0]	O																				
SRAS#	O																				
SCAS#	O																				
SWE#	O																				
SCK_[7:0]	O	LVTTTL	Clock	GND	1,4	7	15	15	4	0"	0.5"	4.3"	5.2"	0"	0.25"	0.5"	1.5"	Table 6-7	5.7" ±0.02" from GMCH die pad to DIMM pin	5 on 5 for a max of 0.5"	6.2.1.4
SRDCLK_OUT	O	LVTTTL	Feed back	GND	NA	5	15	5	5	0"	0.1"	0"	0.1"	—	—	—	—	—	—	N/A	6.2.1.5
SRDCLK_IN	I																				

Figure 199. SDR System Memory Routing Topologies





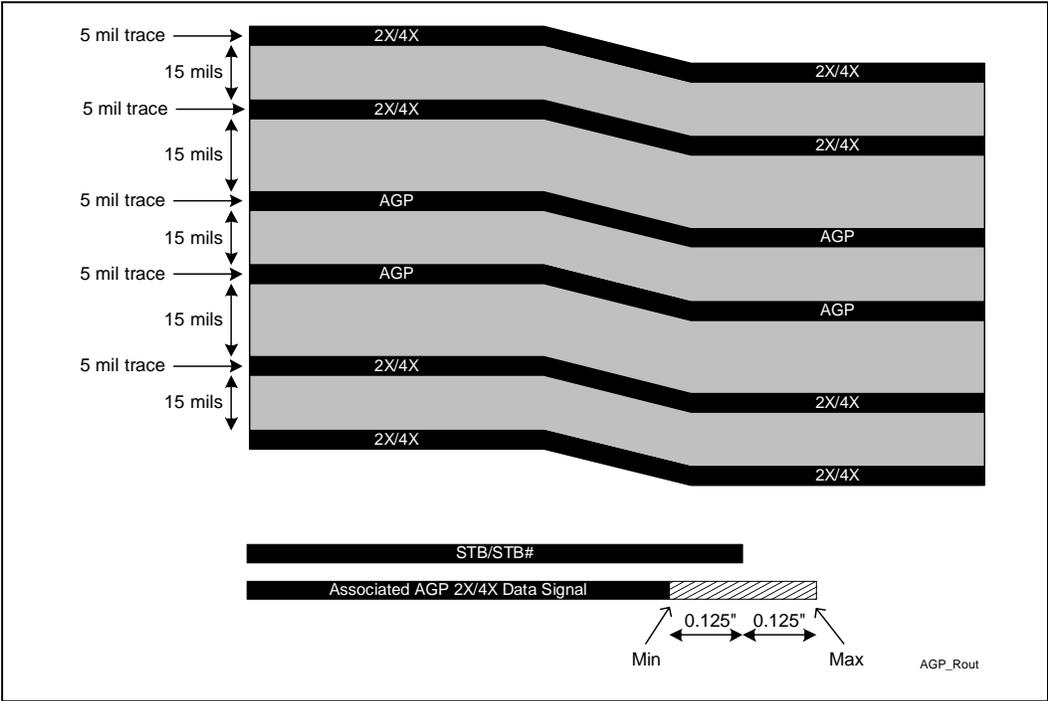
16.3 AGP Signals

Table 108. AGP Interface Routing

Intel® GMCH	I/O	Timing Domain	Plane Reference	Layer Target	Net Width (mils)	Net Spacing (Same Signal Group)	Max MB Length	Matching	Intel® GMCH Breakout Guidelines	Reference Section
GFRAME#	I/O	1X	—	—	5	7	6"	Match GTRDY# ±250 mils	—	7.3.1
GTRDY#	I/O		GND	4				Match GFRAME# ±250 mils		
GSTOP#	I/O		—	—				Match GAD_15# ±250 mils		
GIRDY#	I/O		GND	4				Match DEVSEL# ±250 mils		
GDEVSEL#	I/O		—	—				Match GIRDY# ±250 mils		
GRBF#	I		—	—						
GPIPE#	I		—	—						
GREQ#	I		—	—						
GWBF#	I		—	—						
GGNT#	O		GND	4						
GST_[2:0]	O		GND	4						
GPAR / ADD_DETECT	I/O		—	—						
GADSTB_[1:0]	I/O	2X/4X	—	—	15			Strobe should match complement to ±50 mils GADSTB_0 should match GADSTB_1 to ±125 mils (Note Strobes are not used for 1X mode)	5 mil spacing allowed. <0.3" from the GMCH package	7.3.2
GADSTB_[1:0]#	I/O		—	—						
GSBSTB	I		—	—						
GSBSTB#	I		—	—						
GAD_[15:0]	I/O		GND	4				Match with GAD_STB0 and GAD_STB0# from GMCH pad to AGP pin within ±125 mils		
GC/BE_[1:0]#	I/O		—	—				Match with GAD_STB1 and GAD_STB1# from GMCH pad to AGP pin within ±125 mils		
GAD_[31:16]	I/O		—	—				Match with GAD_STB and GAD_STB# from GMCH pad to AGP pin within ±125 mils		
GC/BE_[3:2]#	I/O		—	—						
GSBA_[7:0]	I	—	—							



Figure 200. AGP 2X, 4X Routing Example





16.4 Display Interface Signals

Table 109. Display Interface (DVO Down Signal Routing)

Intel® GMCH	I/O	Plane Reference	Layer Target	Net Width	Net Spacing (Same Signal Group)	Spacing to other signals (mils)	Maximum MB Length	Matching	Intel® GMCH Breakout Guidelines	Reference Section		
DVOB_CLK / DVOB_CLK#	O	GND	4	5	15	20	7.5"	Match complement ±50 mils	—	—		
DVOB_D[11:0]	O	GND	4	5	15	15	7.5"	Match to DVOB_CLK / DVOB_CLK# within ±0.1"	Width and Space 5 mils on 5 mils. 5 mils spacing allowed <0.3" from GMCH package	7.7		
DVOB_HSYNC	O	GND	4	5	15	15	7.5"					
DVOB_VSYNC	O	GND	4	5	15	15	7.5"					
DVOB_BLANK#	O	GND	4	5	15	15	7.5"					
DVOBC_CLKINT	I	GND	4	5	15	15	7.5"	—				
DVOB_FLDSTL	I	GND	4	5	15	15	7.5"	—				
DVOC_CLK / DVOC_CLK#	O	GND	4	5	15	20	7.5"	Match complement ±50 mils				
DVOC_D[11:0]	O	GND	4	5	15	15	7.5"	Match to DVOC_CLK / DVOC_CLK# within 0.1"				
DVOC_HSYNC	O	GND	4	5	15	15	7.5"					
DVOC_VSYNC	O	GND	4	5	15	15	7.5"					
DVOC_BLANK#	O	GND	4	5	15	15	7.5"					
DVOBC_INTR#	I	GND	4	5	15	15	7.5"	—				
DVOC_FLDSTL	I	GND	4	5	15	15	7.5"	—				
MI2C_CLK	I/O	GND	4	5	15	15	7.5"	—				
MI2C_DATA	I/O	GND	4	5	15	15	7.5"	—				
MDVI_CLK	I/O	GND	4	5	15	15	7.5"	—				
MDVI_DATA	I/O	GND	4	5	15	15	7.5"	—				
MDDC_CLK	I/O	GND	4	5	15	15	7.5"	—				
MDDC_DATA	I/O	GND	4	5	15	15	7.5"	—				

Table 110. Display Interface (Analog Display Routing Signal)

Intel® GMCH	I/O	Type	Type	Net Width	Net Spacing (Same Signal Group)	Spacing to other signals (mils)	Matching	Reference Section
VSYNC	O	3.3 V	GPIO	—	—	—	—	8.1
HSYNC	O	3.3 V	GPIO	—	—	—	—	
RED	O	NA	Analog	8	5	20	*Routing parallel complement (i.e., RED and RED#) to terminating resistor *Match RGB signals ± 200 mils to VGA connector	
RED#	O	NA	Analog	8	5	20		
GREEN	O	NA	Analog	8	5	20		
GREEN#	O	NA	Analog	8	5	20		
BLUE	O	NA	Analog	8	5	20		
BLUE#	O	NA	Analog	8	5	20		
REFSET	I	NA	Analog	8	5	20		
DDCA_CLK	I/O	3.3 V	GPIO	—	—	—	—	
DDCA_DATA	I/O	3.3 V	GPIO	—	—	—	—	

16.5 Hub Interface Signals

Table 111. Hub Interface Routing

Intel® GMCH	I/O	Type	Plane Reference	Layer Target	Net Width (mils)	Net Spacing (Same Signal Group)	Spacing to other signals	Min MB Length	Max MB Length	Matching	Reference Section
HSTRS	I/O	H	GND	4	5	15	20	2"	8"	Length between two strobes match within ± 100 mils	9.1
HSTRF	I/O	H	GND	4	5	15	20	2"	8"		
H[7:0]	I/O	H	GND	4	5	15	20	2"	8"	Each data signal match within ± 100 mils of the strobe pair	
H8	O	H	GND	4	5	15	—	2"	8"		
H9	I	H	GND	4	5	15	—	2"	8"		
H10	I/O	H	GND	4	5	15	—	2"	8"		



16.6 Clocking Signals

Table 112. Clocking Signals Routing

Intel® GMCH	I/O	Type	Freq.	Plane Ref	Net Width (mils)	Net Spacing (same signal group - mils)	Spacing to other signals (mils)	Topology	A		B		C		A + B	A + B + C	Reference Section
									Max	Min	Max	Min	Max				
HOST_CLK	O	CMOS	100/133	GND	7	—	—	1	—	—	—	—	—	—	—	—	13.2.2
DOT_CLK	O	LVTTTL	48	GND	5	NA	20	2	0.5"	2.0"	9.0"	—	—	—	—	—	13.2.3
CLK66	O	LVTTTL	66	GND	5	20	20	3	0.5"	4.0"	8.5"	—	—	—	—	—	13.2.4
AGPCLK	O	—	66	GND	5	15	15	4	0.5"	(CLK66 Trace B) - 4	—	Route per the AGP Spec		—	—	—	13.2.5
CLK33	O	—	33	GND	5	15	15	5	0.5"	4"	8.5"	—	—	CLK66 ±100 mils	—	—	13.2.6
CLK14	O	—	14.318	GND	5	10	10	6	0.5"	0"	12"	0"	6"	CLK33 ±500 mils	Match to ±5" of each other	—	13.2.7
PCICLK	O	—	33	GND	5	15	15	7	0.5"	—	—	—	—	PCI device down: (CLK33) ±500 mils. Devices on PCI cards: (CLK33 - 2.5") ±500 mils	—	—	13.2.8
USBCLK	O	—	48	GND	5	NA	20	8	0.5"	3"	12"	—	—	—	—	—	—



Figure 201. Clocking Signals Routing Topologies

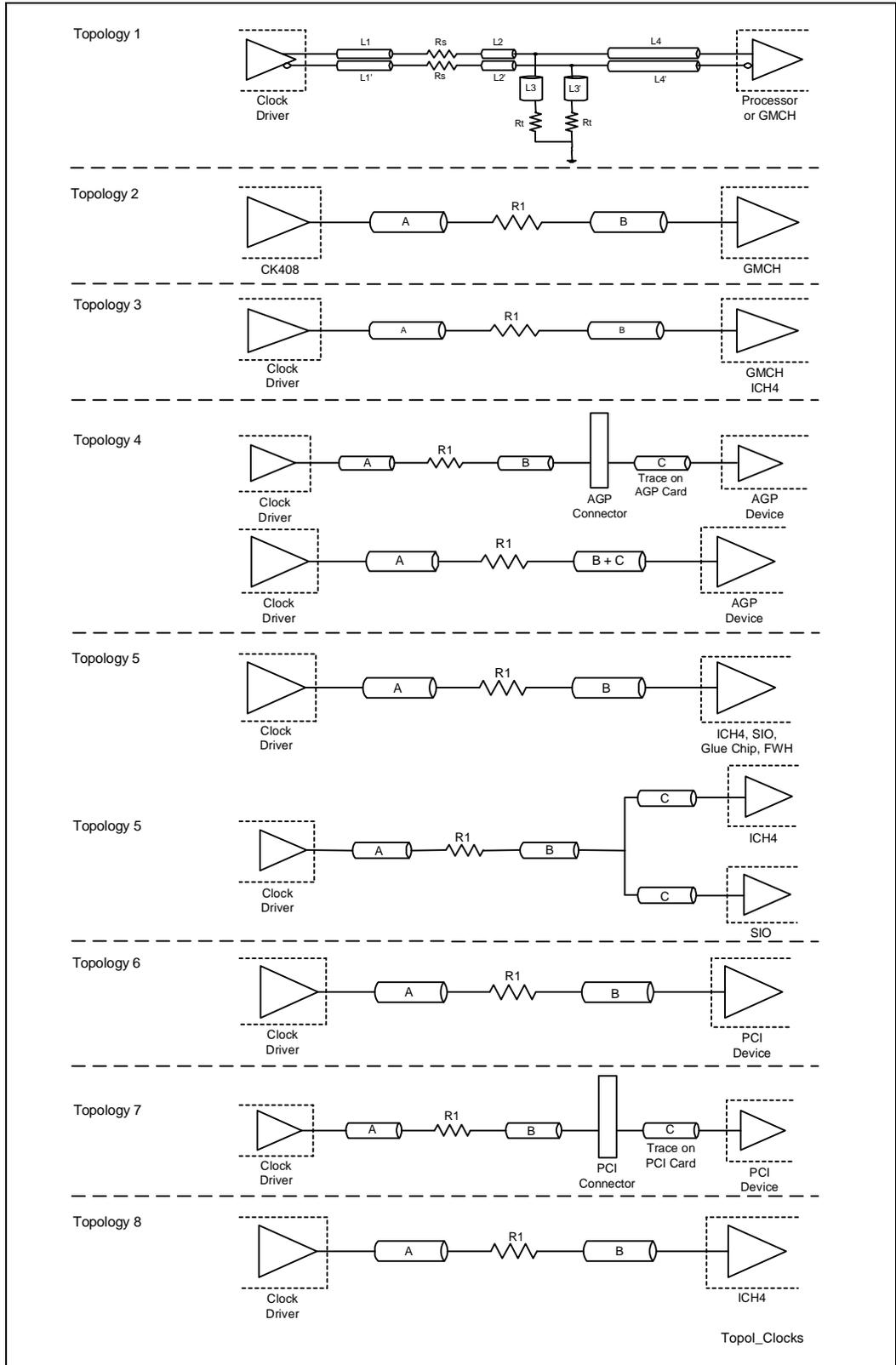


Figure 202. Host Clocking Signals Routing Topologies

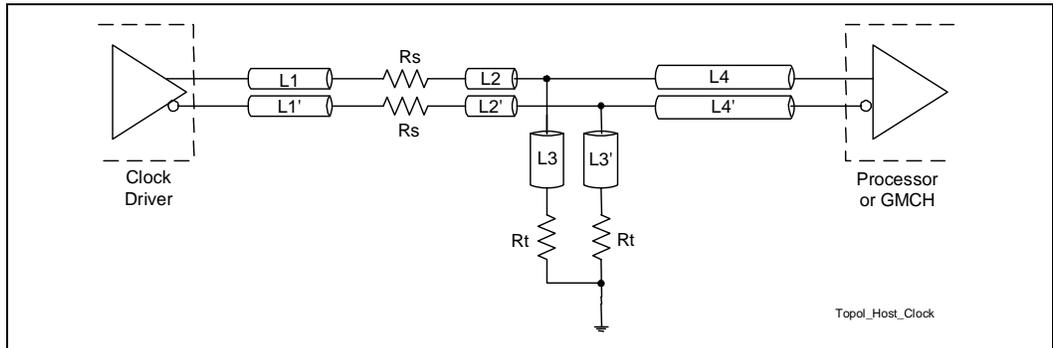


Table 113. Host Clock Routing Guidelines (BCLK[1:0]#, HCLKP, HCLKN)

Layout Guideline	Value	Notes
Host Clock Skew between agents	400 ps total Budget: 150 ps for Clock driver 250 ps for interconnect	2, 3, 4,5
Reference Plane	Ground Referenced (Contiguous over entire length)	—
Differential pair spacing = S	8 mils	6, 7
Spacing to other traces	3S to 4S	—
Nominal trace width = W	7.0 mils	8
System board Impedance – Differential	100 $\Omega \pm 15\%$	9
System board Impedance – odd mode	50 $\Omega \pm 15\%$	10
Processor routing length – L1, L1': Clock driver to Rs	0.5" max	13
Processor routing length – L2, L2': Rs to Rs-Rt node	0 – 0.2"	13
Processor routing length – L3, L3': RS-RT node to Rt	0 - 0.2"	13
Processor routing length – L4, L4': RS-RT Node to Load	2 – 12"	
GMCH routing length – L1, L1': Clock Driver to RS	0.5" max	13
GMCH routing length – L2, L2': Rs to Rs-Rt node	0 – 0.2"	13
GMCH routing length – L3, L3': RS-RT node to Rt	0 – 0.2"	13
GMCH routing length – L4, L4': RS-RT Node to Load	2 – 12"	
Clock driver to Processor and clock driver to chipset length matching (L1 + L2 + L4)	Clock pair to GMCH must be 100 mils longer than clock pair to processor socket	10
HCLKP – HCLKN, BCLK0 – BCLK1 length matching	± 10 mils	—
Rs Series termination value	27 $\Omega \pm 1\%$	11
Rt Shunt termination value	49.9 $\Omega \pm 1\%$ (for 50 Ω MB impedance)	12
Maximum Via Count Per Signal	3	

17 Intel® 845G Chipset Schematic Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements the 845G chipset. The items contained in this checklist attempt to address important connections to these devices and critical supporting circuitry. **This is not a complete list, and it does not guarantee that a design will function properly.** Beyond the items contained in the checklist, refer to the Customer Reference Board schematics in Appendix A for more detailed instructions on designing a motherboard. This work is ongoing, and the recommendations and considerations herein are subject to change.

17.1 Host Interface

17.1.1 Processor / Intel® GMCH Items

Checklist Item	Recommendation	Reason/Impact/Documentation
A[31:3]#	<ul style="list-style-type: none"> Connect to HA_[31:3] pins on GMCH Leave A[35:32]# as No Connect. 	Chipset does not support extended addressing over 4 GB, leave A[35:32]# unconnected. AGTL+ Source Synch I/O Signal
ADS#	<ul style="list-style-type: none"> Connect to the same pin name on the GMCH 	AGTL+ Common Clock I/O Signal
ADSTB[1:0]#	<ul style="list-style-type: none"> Connect to HADSTB_[1:0]# pins on GMCH 	AGTL+ Source Synch I/O Signal
BNR#	<ul style="list-style-type: none"> Connect to the same pin name on the GMCH 	AGTL+ Common Clock I/O Signal
BPRI#	<ul style="list-style-type: none"> Connect to the same pin name on the GMCH 	AGTL+ Common Clock Input Signal
BREQ0#	<ul style="list-style-type: none"> Connect to BREQ0# on the GMCH Terminate to VCCP through a 150 Ω – 220 Ω ±5% resistor near the processor 	The chipset contains on die termination for the BREQ0# signal. The Intel® Pentium 4 processor does not contain on die termination for this particular AGTL+ signal thus external termination is required only on the processor end. BR0# termination should equal the resistance value of on die AGTL+ termination resistance (Rtt) value. AGTL+ Common Clock I/O Signal Refer to Section 4.3.1.8 and Figure 20
D[63:0]#	<ul style="list-style-type: none"> Connect to HD_[63:0]# pins on GMCH 	AGTL+ Source Synch I/O Signal.
DBI[3:0]#	<ul style="list-style-type: none"> Connect to DINV_[3:0]# pin on the GMCH 	AGTL+ Source Synch I/O Signal.
DBSY#	<ul style="list-style-type: none"> Connect to the same pin name on the GMCH 	AGTL+ Common Clock I/O Signal.



Checklist Item	Recommendation	Reason/Impact/Documentation
DEFER#	<ul style="list-style-type: none"> Connect to the same pin name on the GMCH 	AGTL+ Common Clock Input Signal.
DRDY#	<ul style="list-style-type: none"> Connect to the same pin name on the GMCH 	AGTL+ Common Clock I/O Signal.
DSTBN[3:0]#	<ul style="list-style-type: none"> Connect to HDSTB_N[3:0]# pins on GMCH 	AGTL+ Source Synch I/O Signal.
DSTBP[3:0]#	<ul style="list-style-type: none"> Connect to HDSTB_P[3:0]# pins on GMCH 	AGTL+ Source Synch I/O Signal.
HIT#	<ul style="list-style-type: none"> Connect to the same pin name on the GMCH 	AGTL+ Common Clock I/O Signal.
HITM#	<ul style="list-style-type: none"> Connect to the same pin name on the GMCH 	AGTL+ Common Clock I/O Signal.
LOCK#	<ul style="list-style-type: none"> Connect to HLOCK# pin on GMCH 	AGTL+ Common Clock I/O Signal.
REQ[4:0]#	<ul style="list-style-type: none"> Connect to HREQ_[4:0]# pins on GMCH 	AGTL+ Source Synch I/O Signals.
RESET#	<ul style="list-style-type: none"> Connect to the CPURST# on the GMCH Terminate to VCCP through a 51 Ω $\pm 5\%$ resistor near the processor 	<p>The chipset contains on die termination for the CPURST# signal. The Intel® Pentium 4 processor does not contain on die termination for this particular AGTL+ signal thus external termination is required only on the processor end. RESET# termination should equal the resistance value of on die AGTL+ termination resistance (R_{tt}) value.</p> <p>AGTL+ Common Clock I/O Signal</p> <p>Refer to Section 4.3.1.8 and Figure 20</p>
RS[2:0]#	<ul style="list-style-type: none"> Connect to the same pin name on the GMCH 	AGTL+ Common Clock Input Signal.
TRDY#	<ul style="list-style-type: none"> Connect to HTRDY# pin on GMCH 	AGTL+ Common Clock Input Signal.

17.1.2 Intel® GMCH Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
HA_VREF HCC_VREF HDVREF_[2:0]	<ul style="list-style-type: none"> Connect voltage divider circuit to VCCP through a $49.9 \Omega \pm 1\%$ pull-up resistor and to GND through a $100 \Omega \pm 1\%$ pull-down resistor Decouple the voltage divider with a $0.1 \mu\text{F} \pm 10\%$ capacitor. 	Refer to DG Section 4.1.1
HCLKN	<ul style="list-style-type: none"> Connect to CPU2 in CK408 Connect to a series $27.4 \Omega \pm 1\%$ resistor and terminate to GND through a $49.9 \Omega \pm 1\%$ resistor 	
HCLKP	<ul style="list-style-type: none"> Connect to CPU2# in CK408 Connect to a series $27.4 \Omega \pm 1\%$ resistor and terminate to GND through a $49.9 \Omega \pm 1\%$ resistor 	
HX_RCOMP HY_RCOMP	<ul style="list-style-type: none"> Pull-down to GND through a $24.9 \Omega \pm 1\%$ resistor 	
HX_SWING HY_SWING	<ul style="list-style-type: none"> Connect voltage divider circuit to VCCP through a $301 \Omega \pm 1\%$ pull-up resistor and to GND through a $150 \Omega \pm 1\%$ pull-down resistor Decouple the voltage divider with a $0.01 \mu\text{F} \pm 10\%$ capacitor to VCCP 	
VTTDECAP	<ul style="list-style-type: none"> GND through a $0.1 \mu\text{F} \pm 10\%$ capacitor 	
VTTFSB	<ul style="list-style-type: none"> Connect to Processor Vreg (2) $10 \mu\text{F}$ and (5) $0.1 \mu\text{F}$ capacitor 	Refer to Section 14.2.4



17.1.3 Processor/Intel® ICH4 Items

Checklist Item	Recommendation	Reason/Impact/Documentation
A20M# IGNNE# SMI# STPCLK#	<ul style="list-style-type: none"> Connect to the same pin name on the ICH4. (No extra pull-up resistors required) 	Asynch GTL+ Input Signal Refer to Section 4.3.1.4
FERR#	<ul style="list-style-type: none"> Connect to the same pin name on the ICH4 Terminate to VCCP through a $62\ \Omega \pm 5\%$ resistor 	This output signal is not terminated on the processor. Termination is required on system board. Asynch GTL+ Output Signal Refer to DG Section 4.3.1.1
INIT#	<ul style="list-style-type: none"> Connect to the same pin name on the ICH4 (No extra pull-up resistors required) Level shifting required to connect to Firmware Hub From FWH tie to VCC_FWH through a $300\ \Omega \pm 5\%$ resistor 	Termination not required. Asynch GTL+ Input Signal. Refer to DG Section 4.3.1.5
LINT[1:0]	<ul style="list-style-type: none"> LINT0 connects to INTR on ICH4. (No extra pull-up resistors required) LINT1 connects to NMI on ICH4. (No extra pull-up resistors required) 	Asynch GTL+ Input Signal Refer to Section 4.3.1.4
PWRGOOD	<ul style="list-style-type: none"> Connects to CPUPWRGD on ICH4. (Weak external pull-up resistor required) Terminate to VCCP through a $300\ \Omega \pm 5\%$ resistor 	Miscellaneous Signal Refer to Section 4.3.1.6
SLP#	<ul style="list-style-type: none"> Connect to CPUSLP# on the ICH4 through a $60\ \Omega - 80\ \Omega$ series resistor (No extra pull-up resistors required) 	

17.1.4 Processor Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
A[35:32]#	<ul style="list-style-type: none"> No Connect 	Chipset does not support extended addressing over 4 GB, leave A[35:32]# unconnected.
AP[1:0]#	<ul style="list-style-type: none"> No Connect 	Chipset does not support parity protection on the address bus. AGTL+ Common Clock I/O Signal.
BCLK[1:0]	<ul style="list-style-type: none"> BLCK0 connects to CPU0 in CK-408 thru a $27.4 \Omega \pm 1\%$ resistor BLCK1 connects to CPU0# in CK-408 thru a $27.4 \Omega \pm 1\%$ resistor 	Rt resistors should be selected to match the characteristic impedance of the board. System Bus Clock Signal Refer to Section 13.2.1
BPM[5:0]#	<ul style="list-style-type: none"> These signals should be terminated with a $51 \Omega \pm 5\%$ resistor to VCCP near the processor. If a debug port is implemented termination is required near the debug port as well. Refer to the processor <i>ITP700 Debug Port Design Guide</i> for further information. 	
BINIT#	<ul style="list-style-type: none"> No Connect 	Chipset does not support this signal. AGTL+ Common Clock I/O Signal
BSEL[1:0]	<ul style="list-style-type: none"> BSEL1 – No Connect BSEL0 - Connect to GMCH PSBSEL Terminate to GMCH 3.3 V supply through a $1.5 \text{ k}\Omega \pm 5\%$ resistor 	
COMP[1:0]	<ul style="list-style-type: none"> Terminate to GND through a $51.1\Omega \pm 1\%$ resistor Minimize the distance from termination resistor and processor pin 	Each COMP pin requires a separate resistor for each pin. RCOMP value can be adjusted to set external drive strength of I/O and to control edge rate. Refer to Section 4.3.1.8
DBR#	<ul style="list-style-type: none"> Connect to SYS_RST# in ICH4 Refer to the processor <i>ITP700 Debug Port Design Guide</i> for further information. 	
DP[3:0]#	<ul style="list-style-type: none"> No Connect 	Not supported by chipset
IERR#	<ul style="list-style-type: none"> No Connect Ok to test point 	Not supported by chipset Asynch GTL+ Output Signal.
GTLREF[3:0]	<ul style="list-style-type: none"> GTLREF[3:1] – No Connect GTLREF0 - Terminate to VCCP through a $49.9 \Omega \pm 1\%$ resistor Terminate to GND through a $100 \Omega \pm 1\%$ resistor Should be 2/3 VCCP 	Correct settings are critical. This signal controls the signal reference of the AGTL+ input pins. Refer to Section 4.1.1



Checklist Item	Recommendation	Reason/Impact/Documentation
ITP_CLK0	<ul style="list-style-type: none"> Connect to CPU1 in CK_408 through a 27.4 Ω \pm1% resistor Refer to the processor <i>ITP700 Debug Port Design Guide</i> for further information. 	
ITP_CLK1	<ul style="list-style-type: none"> Connect to CPU1# in CK_408 through a 27.4 Ω \pm1% resistor Refer to the processor <i>ITP700 Debug Port Design Guide</i> for further information. 	
MCERR#	<ul style="list-style-type: none"> No Connect 	Chipset does not support this signal. AGTL+ Common Clock I/O Signal.
PROCHOT#	<ul style="list-style-type: none"> No connect 	Asynch GTL+ Output Signal Refer to Section 4.3.1.2
RSP#	<ul style="list-style-type: none"> No Connect 	Chipset does not support this signal. AGTL+ Common Clock Input Signal
SKTOCC#	<ul style="list-style-type: none"> Connect to CPU_Present on Glue Chip thru 33 Ω \pm 5% resistor or to Discrete Logic (If pin is used) 	Processor pulls this signal to GND. System board designers may use this pin to determine if the processor is present in the socket.
TCK	<ul style="list-style-type: none"> Refer to the processor <i>ITP700 Debug Port Design Guide</i> for further information. 	
TDI	<ul style="list-style-type: none"> Refer to the processor <i>ITP700 Debug Port Design Guide</i> for further information 	
TDO	<ul style="list-style-type: none"> Refer to the processor <i>ITP700 Debug Port Design Guide</i> for further information. 	
TESTHI[12:0]	<ul style="list-style-type: none"> The TESTHI pins should be tied to the VCC_CPU via a matched resistor that has a resistance value within \pm 20% of the impedance of the board transmission line traces. See DG Section 4.3.1.11 for further details. 	Tying any of the TESTHI pins together will prevent the ability to perform boundary scan testing. Refer to the processor datasheet
THERMTRIP#	<ul style="list-style-type: none"> Terminate to VCCP through a 62 Ω \pm5% resistor near the processor 	Asynch GTL+ Output Signal Refer to Section 4.3.1.3
THERMDA	<ul style="list-style-type: none"> Connect to thermal monitor circuitry if used Connect to REMOTE1+ in HECETA 	Refer to Section 4.3.1.10.
THERMDC	<ul style="list-style-type: none"> Connect to thermal monitor circuitry if used Connect to REMOTE1-/NTESTIN in HECETA 	Refer to Section 4.3.1.10.
TMS	<ul style="list-style-type: none"> Refer to the processor <i>ITP700 Debug Port Design Guide</i> for further information. Connect to the same name in ITP port 	
TRST#	<ul style="list-style-type: none"> Refer to the processor <i>ITP700 Debug Port Design Guide</i> for further information. Terminate to ground through a 680 Ω \pm 5 resistor 	



Checklist Item	Recommendation	Reason/Impact/Documentation
VCCA	<ul style="list-style-type: none"> Connect with isolated power circuitry to VCCP 	Isolated power for internal processor system bus PLLs Refer to Sections 4.3.1.7 and 4.6.5.1.
VCCIOPLL	<ul style="list-style-type: none"> Connect with isolated power circuitry to VCCP 	Isolated power for internal processor system bus PLLs Refer to Sections 4.3.1.7 and 4.6.5.1.
VCC_SENSE	<ul style="list-style-type: none"> Connect through test point header to VSS_SENSE 	Isolated low impedance connection to processor core power (VCC) Refer to the processor datasheet.
VCCVID	<ul style="list-style-type: none"> Connect to 1.2 V linear regulator 	Refer to Section 4.3.1.12
VID[4:0]	<ul style="list-style-type: none"> Connect to VR or VRM. These signals need to be pulled up to 3.3 V through either 1 kΩ pull-ups on the motherboard or with internal pull-ups in the VR or VRM. 	Refer to the <i>VRM9.0 DC-DC Converter Design Guidelines</i>
VSSA	<ul style="list-style-type: none"> Connect with isolated power circuitry to VCCP 	Isolated GND for internal PLLs Refer to Sections 4.3.1.7 and 4.6.5.1.
VSS_SENSE	<ul style="list-style-type: none"> Connect through test point header to VCC_SENSE 	Isolated low impedance connection to core VSS. Refer to the processor datasheet.

17.2 Memory Interface

17.2.1 DDR SDRAM

17.2.1.1 Intel® GMCH / DIMM Connector Items (DDR)

Checklist Item	Recommendation	Reason/Impact/Documentation
SBA_[1:0]	<ul style="list-style-type: none"> Connect to BA[1:0] pin on both DIMMA and DIMMB Terminate to VTT through a 56 Ω \pm5% resistor 	<p>Follow DDR Address/Command Signal routing topology guidelines.</p> <p>Refer to Section 5.2.3.</p>
SCAS#	<ul style="list-style-type: none"> Connect to CAS# pin on both DIMMA and DIMMB Terminate to VTT through 56 Ω \pm5% resistor 	<p>Follow DDR Address/Command Signal routing topology guidelines.</p> <p>Refer to Section 5.2.3.</p>
SDM_[7:0]	<ul style="list-style-type: none"> Connect to DM[7:0] on both DIMMA and DIMMB connect through a series 10 Ω \pm 5% resistor and terminate to VTT through a 56 Ω \pm 5% resistor. 	<p>Follow DDR Data Signal routing topology guidelines.</p> <p>Refer to Section 5.2.1.</p>
SCMDCLK_[2:0]	<ul style="list-style-type: none"> Connect to CK[2:0] in DIMMA 	Refer to DG Section 5.2.5.
SCMDCLK_[5:3]	<ul style="list-style-type: none"> Connect to CK[2:0] in DIMMB 	Refer to DG Section 5.2.5.
SCMDCLK_[2:0]#	<ul style="list-style-type: none"> Connect to CK[2:0]# in DIMMA 	Refer to DG Section 5.2.5.
SCMDCLK_[5:3]#	<ul style="list-style-type: none"> Connect to CK[2:0]# in DIMMB 	Refer to DG Section 5.2.5.
SCKE_[1:0]	<ul style="list-style-type: none"> Connect to CKE[1:0] on DIMMA Terminate to VTT through a 56 Ω \pm5% resistor 	Refer to DG Section 5.2.2.
SCKE_[3:2]	<ul style="list-style-type: none"> Connect to CKE[1:0] on DIMMB Terminate to VTT through a 56 Ω \pm5% resistor 	Refer to DG Section 5.2.2.
SCS_[1:0]#	<ul style="list-style-type: none"> Connect to CS[1:0]# on DIMMA Terminate to VTT through a 56 Ω \pm5% resistor 	Refer to DG Section 5.2.2.
SCS_[3:2]#	<ul style="list-style-type: none"> Connect to CS[1:0]# on DIMMB Terminate to VTT through a 56 Ω \pm5% resistor 	Refer to DG Section 5.2.2.
SDQ_[63:0]	Connect to DQ[63:0] on both DIMMA and DIMMB through a series 10 Ω \pm 5% resistor and terminate to VTT through a 56 Ω \pm 5% resistor	<p>Follow DDR Data Signal routing topology guidelines.</p> <p>Refer to Section 5.2.1.</p>
SDQS_[7:0]	<ul style="list-style-type: none"> Connect to DQS[7:0] pins on both DIMMA and DIMMB Connect to a series 10 Ω \pm5% resistors and terminate to VTT through a 56 Ω \pm5% resistor 	<p>Follow DDR Data Signal routing topology guidelines.</p> <p>Refer to Section 5.2.1.</p>

Checklist Item	Recommendation	Reason/Impact/Documentation
SMAA_[12:6,3,0]	<ul style="list-style-type: none"> Connect to A[12:6,3,0] pins on DIMMA and DIMMB Terminate to VTT through a 56 Ω \pm5% resistor 	Follow DDR Address/Command Signal routing topology guidelines. Refer to Section 5.2.3.
SMAA_[5,4,2,1]	<ul style="list-style-type: none"> Connect to A[5,4,2,1] on DIMMA Terminate to VTT through a 33 Ω \pm5% resistor 	Refer to Section 5.2.4.
SMAB_[5,4,2,1]	<ul style="list-style-type: none"> Connect to A[5,4,2,1] on DIMMB Terminate to VTT through a 33 Ω \pm 5% resistor. 	Refer to Section 5.2.4.
SRAS#	<ul style="list-style-type: none"> Connect to RAS# pin on both DIMMA and DIMMB Terminate to VTT through a 56 Ω \pm5% resistor 	Follow DDR Address/Command Signal routing topology guidelines. Refer to Section 5.2.3.
SWE#	<ul style="list-style-type: none"> Connect to WE# pin on each DIMMA and DIMMB Terminate to VTT through a 56 Ω \pm5% resistor 	Follow DDR Address/Command Signal routing topology guidelines. Refer to Section 5.2.3.

17.2.1.2 Intel® GMCH Only Items (DDR)

Checklist Item	Recommendation	Reason/Impact/Documentation
SRCVEN_OUT#	<ul style="list-style-type: none"> Connect directly to GMCH SRCVEN_IN# pin through an un-populated resistor site. 	Refer to Section 5.2.6.
SRCVEN_IN#	<ul style="list-style-type: none"> Connect directly to GMCH SRCVEN_OUT# pin through an un-populated resistor site. 	Refer to Section 5.2.6.
SM_VREF	<ul style="list-style-type: none"> Connect to DDR Reference Voltage (VREF) 1.25 V Resistor divider consists of two identical resistors (50 Ω – 150 Ω, 1%) Terminate to ground through a 0.1 μF 10% capacitor 	Refer to Section 5.4.4.
SMX_RCOMP SMY_RCOMP	<ul style="list-style-type: none"> 60.4 Ω 1% resistor pulled to DDR 2.5 V, and 60.4 Ω \pm 1% resistor tied to ground The 0.1 μF 20% cap connected to 2.5 V and GND should be used as illustrated in Figure 87 of this DG. 	Refer to Section 5.4.5.
VCCSM	<ul style="list-style-type: none"> Connect to 2.5 V 	



17.2.1.3 DIMM Connector Only Items (DDR)

Checklist Item	Recommendation	Reason/Impact/Documentation
A13 / NC	<ul style="list-style-type: none"> No Connect both DIMMA and DIMMB 	
DM8/DQS17	<ul style="list-style-type: none"> No Connect both DIMMA and DIMMB 	
SDQS_8	<ul style="list-style-type: none"> No Connect both DIMMA and DIMMB 	
CB[7:0]	<ul style="list-style-type: none"> No Connect both DIMMA and DIMMB 	
BA2	<ul style="list-style-type: none"> No Connect both DIMMA and DIMMB 	
SA[2:0]	<ul style="list-style-type: none"> DIMMA: Connect to GND DIMMB: Connect SA[2:1] to GND, and Connect SA0 to 2.5 V 	
WP	<ul style="list-style-type: none"> No Connect both DIMMA and DIMMB 	
RESET#	<ul style="list-style-type: none"> No Connect both DIMMA and DIMMB 	
FETEN	<ul style="list-style-type: none"> No Connect both DIMMA and DIMMB 	
SDA	<ul style="list-style-type: none"> Connect to SMBDATA and SMLINK1 in ICH4 through SMBUS isolation circuitry. 	
SCL	<ul style="list-style-type: none"> Connect to SMBCLK and SMLINK0 in ICH4 through SMBUS isolation circuitry. 	
VREF	<ul style="list-style-type: none"> Connect to DDR Reference Voltage (VREF) Terminate to ground through a 0.1 μF 10% capacitor 	
VDDSPD	<ul style="list-style-type: none"> Connect to power (from a minimum of 2.3 V to a maximum of 3.6 V) Strongly recommend connecting to 2.5 V core 	
VDDID	<ul style="list-style-type: none"> No Connect 	
VDD	<ul style="list-style-type: none"> Connect to 2.5 V both DIMMA and DIMMB 	
VDDQ	<ul style="list-style-type: none"> Connect to 2.5 V both DIMMA and DIMMB 	
VSS	<ul style="list-style-type: none"> Connect to GND 	
NC	<ul style="list-style-type: none"> No Connect both DIMMA and DIMMB 	
CS[3:2]#	<ul style="list-style-type: none"> No Connect both DIMMA and DIMMB 	



17.2.2 PC133 SDR SDRAM

17.2.2.1 Intel® GMCH / DIMM Items (SDR)

Checklist Item	Recommendation	Reason/Impact/Documentation
SCAS#	<ul style="list-style-type: none"> Connect to CAS# pin on each DIMM Connector 	Refer to Section 6.2.1.3.
SDM_[7:0]	<ul style="list-style-type: none"> Connect to DQMB[7:0] pin on each DIMM Connector 	Refer to Section 6.2.1.1.
SCK_[7:0]	<ul style="list-style-type: none"> Connect to CK[3:0] pins on each DIMM Connector according to Table 58 Terminate each to GND at the GMCH through a 22 pF ± 5% EMI capacitor Terminate each to GND through a 51 Ω ± 5% resistor and a 270 pF ± 5% capacitor after the DIMMs 	Refer to Section 6.2.1.4.
SCKE_[3:0]	<ul style="list-style-type: none"> Connect to CKE[1:0] pins on each DIMM Connector according to Table 53 	Refer to Section 6.2.1.2.
SCS_[7:0]#	<ul style="list-style-type: none"> Connect S[3:0] pins on each DIMM Connector according to Table 53 	Refer to Section 6.2.1.2.
SDQ_[63:0]	<ul style="list-style-type: none"> Connect to DQ[63:0] pins on each DIMM Connector 	Refer to Section 6.2.1.1.
SMAA_[12:0]	<ul style="list-style-type: none"> Connect to MA[12:0] pins on each DIMM Connector 	Refer to Section 6.2.1.3.
SBA_[1:0]	<ul style="list-style-type: none"> Connect to BA[1:0] pins on each DIMM Connector 	Refer to Section 6.2.1.3.
SRAS#	<ul style="list-style-type: none"> Connect to RAS pin on each DIMM Connector 	Refer to Section 6.2.1.3.
SWE#	<ul style="list-style-type: none"> Connect to WE# pin on each DIMM Connector 	Refer to Section 6.2.1.3.
VCCSM	<ul style="list-style-type: none"> Connect to 3.3 V system memory power plane 	

17.2.2.2 Intel® GMCH Signals Items (SDR)

Checklist Item	Recommendation	Reason/Impact/Documentation
SRDCLK_OUT#	<ul style="list-style-type: none"> Connect directly to GMCH SRDCLK_IN# pin through an un-populated resistor site 	
SRDCLK_IN#	<ul style="list-style-type: none"> Connect to GMCH SRDCLK_OUT# pin through an un-populated resistor site 	
SM_VREF		Refer to Section 5.4.4.
VCCSM	<ul style="list-style-type: none"> Connect to 3.3 V system memory power plane 	
RSVD	<ul style="list-style-type: none"> No Connect 	

17.2.2.3 DIMM Signals Items (SDR)

Checklist Item	Recommendation	Reason/Impact/Documentation
CB[7:0]	<ul style="list-style-type: none"> No Connect 	



Checklist Item	Recommendation	Reason/Impact/Documentation
MA13	<ul style="list-style-type: none">• Connect to GND	
SA[2:0]	<ul style="list-style-type: none">• DIMM0: Connect to GND• DIMM1: Connect SA[2:1] to GND, and Connect SA0 to 3.3 V	
SDA	<ul style="list-style-type: none">• Connect to I²C DATA	
SCL	<ul style="list-style-type: none">• Connect to I²C CLOCK	
VDD	<ul style="list-style-type: none">• Connect to VCCSM	
WP	<ul style="list-style-type: none">• No Connect	
VSS	<ul style="list-style-type: none">• Connect to GND	

17.3 AGP Interface

17.3.1 AGP Connector / Intel® GMCH Items

Checklist Item	Recommendation	Reason/Impact/Documentation
GADSTB_[1:0]	<ul style="list-style-type: none"> Connect to GADSTB__[1:0] in GMCH Recommend site for a pull up resistor to 1.5 V (4 kΩ to 16 kΩ if populated) 	The GMCH has integrated pull-ups for these signals, but external resistors may still be required. Refer to Section 7.5.2.
GADSTB_[1:0]#	<ul style="list-style-type: none"> Connect to GADSTB_[1:0]# in GMCH Recommend site for a pull-down resistor to GND (4 kΩ to 16 kΩ if populated) 	The GMCH has integrated pull-downs for these signals, but external resistors may still be required. Refer to Section 7.5.2.
GAD_[31:0]	<ul style="list-style-type: none"> Connect to GAD_[31:0] in GMCH 	
GC/BE_#[3:0]	<ul style="list-style-type: none"> Connect to GC/BE_[3:0]# in GMCH 	
GDEVSEL#	<ul style="list-style-type: none"> Connect to GDEVSEL# in GMCH Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated) 	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 7.5.2.
GFRAME#	<ul style="list-style-type: none"> Connect to GFRAME# in GMCH Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated) 	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 7.5.2.
GGNT#	<ul style="list-style-type: none"> Connect to GGNT# in GMCH Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ) 	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 7.5.2.
GIRDY#	<ul style="list-style-type: none"> Connect to GIRDY# in GMCH Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated) 	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 7.5.2.
GPAR	<ul style="list-style-type: none"> Connect to GPAR in GMCH Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated) 	Chipset has integrated pull-ups, but signal may still require
PIPE#	<ul style="list-style-type: none"> Connect to GPIPE in GMCH Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated) 	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 7.5.2.
GREQ#	<ul style="list-style-type: none"> Connect to GREQ# in GMCH Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated) 	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 7.5.2.



Checklist Item	Recommendation	Reason/Impact/Documentation
GSTOP#	<ul style="list-style-type: none"> Connect to GSTOP# in GMCH Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated) 	<p>Chipset has integrated pull-ups, but signal may still require external pull-up resistors.</p> <p>Refer to Section 7.5.2.</p>
GTRDY#	<ul style="list-style-type: none"> Connect to GTRDY# in GMCH Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated) 	<p>Chipset has integrated pull-ups, but signal may still require external pull-up resistors.</p> <p>Refer to Section 7.5.2.</p>
RBF#	<ul style="list-style-type: none"> Connect in GRBF in GMCH Recommend site for a pull-up resistor to VDDQ (4 kΩ to 16 kΩ if populated) 	<p>Chipset has integrated pull-ups, but signal may still require external pull-up resistors.</p> <p>Refer to Section 7.5.2.</p>
SBA_[7:0]	<ul style="list-style-type: none"> Connect to GSBA_[7:0] in GMCH 	<p>Chipset has integrated pull-ups for these signals.</p>
SBSTB	<ul style="list-style-type: none"> Connect to GSBSTB in GMCH Recommend site for a pull-up resistor to 1.5 V (4 kΩ to 16 kΩ if populated) 	<p>The GMCH has integrated pull-ups for these signals, but external resistors may still be required.</p> <p>Refer to Section 7.5.2.</p>
SBSTB#	<ul style="list-style-type: none"> Connect to GSBSTB# GMCH Recommend site for a pull-down resistor to GND (4 kΩ to 16 kΩ if populated) 	<p>The GMCH has integrated pull-downs for these signals, but external resistors may still be required.</p> <p>Refer to Section 7.5.2.</p>
ST[2:0]	<ul style="list-style-type: none"> Connect to GST_[2:0] in GMCH <p>Recommend site for a pull up resistor to 1.5 V (4 kΩ to 16 kΩ if populated)</p>	<p>Refer to Section 7.5.2.</p>
WBF	<ul style="list-style-type: none"> Connect GWBF in GMCH Recommend site for a pull up resistor to VDDQ (4 kΩ to 16 kΩ if populated) 	<p>Chipset has integrated pull-ups, but signal may still require external pull-up resistors.</p> <p>Refer to Section 7.5.2.</p>
VREFCG	<ul style="list-style-type: none"> Should be connected to a resistor divider network. This net should be connected to both Vddq and VSS through 1 KΩ, 1% resistors. In addition to this, a 0.1 μF capacitor should be on this net at both GMCH and the AGP connector. 	

17.3.2 AGP Connector Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
INTA	<ul style="list-style-type: none"> Connect PIRQA# in ICH4 Terminate to 3.3 V through a $8.2\text{ k}\Omega \pm 5\%$ resistor 	
INTB	<ul style="list-style-type: none"> Connect PIRQB# in ICH4 Terminate to 3.3 V through a $8.2\text{ k}\Omega \pm 5\%$ resistor 	
3.3VAUX	<ul style="list-style-type: none"> Connect to PCI 3.3 in VAUX 	
VCC3	<ul style="list-style-type: none"> Connect to 3.3 V 	
12 V	<ul style="list-style-type: none"> Connect to 12 V 	
VCC	<ul style="list-style-type: none"> Connect to 5 V 	
VDDQ	<ul style="list-style-type: none"> Connect to V_1P5_CORE 	
AGPCLK	<ul style="list-style-type: none"> Connect through a $33\ \Omega \pm 5\%$ resistor to 3V66_4 in CK-408 	
GPERR#	<ul style="list-style-type: none"> Recommend site for a Pull-up resistor to VDDQ (4 kΩ to 16 k, $6.8\text{ k}\Omega \pm 5\%$ resistor value recommended) 	
GSERR#	<ul style="list-style-type: none"> Recommend site for a Pull-up resistor to VDDQ (4 kΩ to 16 k, $6.8\text{ k}\Omega \pm 5\%$ resistor value recommended) 	
OVRcnt	<ul style="list-style-type: none"> No Connect 	
PCIRST	<ul style="list-style-type: none"> Connect to RST# slot PCI 1, 2, 3 	
PME#	<ul style="list-style-type: none"> Connect to PME in PCI 1, 2, 3 	
TYPEDET#	<ul style="list-style-type: none"> No Connect 	Signal should either be GROUNDED or NOT CONNECTED on an AGP card. Refer to Section 7.5.2.1.
USB+	<ul style="list-style-type: none"> No Connect 	5 V tolerant
USB-	<ul style="list-style-type: none"> No Connect 	5 V tolerant
RSVD	<ul style="list-style-type: none"> No Connect 	
VREFGC	<ul style="list-style-type: none"> No Connect 	

17.3.3 AGP Intel® GMCH Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
AGP_RCOMP	<ul style="list-style-type: none"> Pull-down to GND through a $40.2\ \Omega \pm 1\%$ resistor 	
VCCAGP	<ul style="list-style-type: none"> Connect to 1.5 V power plane 	Refer to Section 14.2.4



17.4 DVO Down / GMCH Items

Checklist Item	Recommendation	Reason/Impact/Documentation
DVOB_CLK	<ul style="list-style-type: none"> Connect to GADSTB_0 on GMCH 	Refer to Section 19.4.
DVOB_CLK#	<ul style="list-style-type: none"> Connect to GADSTB_0# on GMCH 	Refer to Section 19.4.
DVOC_CLK	<ul style="list-style-type: none"> Connect to GADSTB_1 in GMCH 	Refer to Section 19.4.
DVOC_CLK#	<ul style="list-style-type: none"> Connect to GADSTB_1# in GMCH 	Refer to Section 19.4.
DVOB_D0	<ul style="list-style-type: none"> Connect to GAD_3 on GMCH 	
DVOB_D1	<ul style="list-style-type: none"> Connect to GAD_2 on GMCH 	
DVOB_D2	<ul style="list-style-type: none"> Connect to GAD_5 on GMCH 	
DVOB_D3	<ul style="list-style-type: none"> Connect to GAD_4 on GMCH 	
DVOB_D4	<ul style="list-style-type: none"> Connect to GAD_7 on GMCH 	
DVOB_D5	<ul style="list-style-type: none"> Connect to GAD_6 on GMCH 	
DVOB_D6	<ul style="list-style-type: none"> Connect to GAD_8 on GMCH 	
DVOB_D7	<ul style="list-style-type: none"> Connect to GC/BE_0# on GMCH 	
DVOB_D8	<ul style="list-style-type: none"> Connect to GAD_10 on GMCH 	
DVOB_D9	<ul style="list-style-type: none"> Connect to GAD_9 on GMCH 	
DVOB_D10	<ul style="list-style-type: none"> Connect to GAD_12 on GMCH 	
DVOB_D11	<ul style="list-style-type: none"> Connect to GAD_11 on GMCH 	
DVOB_HSYNC	<ul style="list-style-type: none"> Connect to GAD_0 on GMCH 	
DVOB_VSYNC	<ul style="list-style-type: none"> Connect to GAD_1 on GMCH 	
DVOB_BLANK#	<ul style="list-style-type: none"> Connect to GC/BE_1# on GMCH 	
DV0BCCLKINT	<ul style="list-style-type: none"> Connect to GAD_13 on GMCH 	
DVOB_FLDSTL	<ul style="list-style-type: none"> Connect to GAD_14 on GMCH 	
DVOBCRCOMP	<ul style="list-style-type: none"> Pull down through a 40.2 Ω 1% resistor connect to AGP_RCOMP on GMCH 	
DVOC_D5	<ul style="list-style-type: none"> Connect to GC/BE_3# in GMCH 	
MI2C_DATA	<ul style="list-style-type: none"> Connect to GDEVSEL# in GMCH Pull-up resistor to VDDQ May require level shifting 	Refer to Section 19.4.
MDVI_DATA	<ul style="list-style-type: none"> Connect to GFRAME# in GMCH Pull-up resistor to VDDQ May require level shifting 	Refer to Section 19.4.
MI2C_CLK	<ul style="list-style-type: none"> Connect to GIRDY# in GMCH Pull-up resistor to VDDQ May require level shifting 	Refer to Section 19.4.



Checklist Item	Recommendation	Reason/Impact/Documentation
MDDC_CLK	<ul style="list-style-type: none"> Connect to GAD_15 in GMCH Pull-up resistor to VDDQ May require level shifting 	
DVOC_D0	<ul style="list-style-type: none"> Connect to GAD_19 on GMCH 	
DVOC_D1	<ul style="list-style-type: none"> Connect to GAD_20 on GMCH 	
DVOC_D2	<ul style="list-style-type: none"> Connect to GAD_21 on GMCH 	
DVOC_D3	<ul style="list-style-type: none"> Connect to GAD_22 on GMCH 	
DVOC_D4	<ul style="list-style-type: none"> Connect to GAD_23 on GMCH 	
DVOC_D6	<ul style="list-style-type: none"> Connect to GAD_25 on GMCH 	
DVOC_D7	<ul style="list-style-type: none"> Connect to GAD_24 on GMCH 	
DVOC_D8	<ul style="list-style-type: none"> Connect to GAD_27 on GMCH 	
DVOC_D9	<ul style="list-style-type: none"> Connect to GAD_26 on GMCH 	
DVOC_D10	<ul style="list-style-type: none"> Connect to GAD_29 on GMCH 	
DVOC_D11	<ul style="list-style-type: none"> Connect to GAD_28 on GMCH 	
DVOC_HSYNC	<ul style="list-style-type: none"> Connect to GAD_17 on GMCH 	
DVOC_VSYNC	<ul style="list-style-type: none"> Connect to GAD_16 on GMCH 	
DVOC_BLANK	<ul style="list-style-type: none"> Connect to GAD_18 on GMCH 	
DVOBC_INTR#	<ul style="list-style-type: none"> Connect to GAD_30 on GMCH 	
DVOC_FLDSTL	<ul style="list-style-type: none"> Connect to GAD_31 on GMCH 	
MDDC_DATA	<ul style="list-style-type: none"> Connect to GSTOP# in GMCH May require level shifting 	Refer to Section 19.4.
MDVI_CLK	<ul style="list-style-type: none"> Connect to GTRDY# in GMCH May require level shifting 	<p>Chipset has integrated pull-ups, but signal may still require external pull-up resistors.</p> <p>Refer to Section 19.4</p>
ADDID[7:0]	<ul style="list-style-type: none"> Connect to GSBA[7:0] in GMCH 	Chipset has integrated pull-ups for these signals.



17.5 Intel® GMCH / DAC Items

Checklist Item	Recommendation	Reason/Impact/Documentation
HSYNC	<ul style="list-style-type: none"> Output to VGA connector through a $47 \Omega \pm 5\%$ resistor 	
VSYNC	<ul style="list-style-type: none"> Output to VGA connector through a $47 \Omega \pm 5\%$ resistor 	
RED	<ul style="list-style-type: none"> Output through pi filter to VGA connector. Terminate to GND through a $75 \Omega \pm 1\%$ resistor. 	
RED#	<ul style="list-style-type: none"> Terminate to GND through a $37.4 \Omega \pm 1\%$ resistor 	
GREEN	<ul style="list-style-type: none"> Output through pi filter to VGA connector. Terminate to GND through a $75 \Omega \pm 1\%$ resistor. 	
GREEN#	<ul style="list-style-type: none"> Terminate to GND through a $37.4 \Omega \pm 1\%$ resistor 	
BLUE	<ul style="list-style-type: none"> Output through pi filter to VGA connector. Terminate to GND through a $75 \Omega \pm 1\%$ resistor. 	
BLUE#	<ul style="list-style-type: none"> Terminate to GND through a $37.4 \Omega \pm 1\%$ resistor 	
REFSET	<ul style="list-style-type: none"> Terminate to GND through a $137 \Omega \pm 1\%$ resistor 	
DREFCLK	<ul style="list-style-type: none"> Connect to DOT_48 MHZ in CK_408 through a $33 \Omega \pm 5\%$ resistor 	
DDCA_CLK	<ul style="list-style-type: none"> Pull-up to 3.3 V through 2.7 KΩ resistor Level shift (example: through glue 4) they output to VGA Connector. 	
DDCA_DATA	<ul style="list-style-type: none"> Pull-up to 3.3 V through 2.7 kΩ resistor Level shift (example: through glue 4) they output to VGA Connector. 	

17.5.1 DAC Intel® GMCH Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
VCCA_DPLL	<ul style="list-style-type: none"> Connect to 1.5 V through appropriate LC filter 	
VCCA_DAC	<ul style="list-style-type: none"> Connect 1.5 V with a 0.1 μF and 0.01 μF capacitor 	Refer to Section 8.1.4.
VSSA_DAC	<ul style="list-style-type: none"> Connect directly to ground 	



17.6 Hub Interface

17.6.1 Hub Interface Intel® GMCH / ICH4 Items

Checklist Item	Recommendation	Reason/Impact/Documentation
HI[10:0]	<ul style="list-style-type: none"> Connect to HI[10:0] in ICH4 	Refer to Section 9.1.2.
HI_STBS	<ul style="list-style-type: none"> Connect to HI_STBS in ICH4 	Refer to Section 9.1.1.
HI_STBF	<ul style="list-style-type: none"> Connect to HI_STBF in ICH4 	Refer to Section 9.1.1.
HI_REF	<ul style="list-style-type: none"> Connect to voltage divider circuit 	Refer to Section 9.1.4.
HI_SWING	<ul style="list-style-type: none"> Connect to voltage divider circuit 	Refer to Section 9.1.4.

17.6.2 Hub Interface Intel® GMCH Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
HI_RCOMP	<ul style="list-style-type: none"> Pull-up to VCC1.5 through a 68.1 Ω \pm1% resistor 	
VCCHI	<ul style="list-style-type: none"> Connect to 1.5 V through (2) 0.1 μF decoupling capacitor. Place near balls: AA1 and AE1 	Refer to Section 9.1.

17.6.3 Hub Interface Intel® ICH4 Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
HICOMP	<ul style="list-style-type: none"> Terminate to VCC1.5 through a 68.1 Ω \pm1% resistor 	
HI11	<ul style="list-style-type: none"> Terminate to VSS through a 60 Ω \pm 5% resistor 	

17.7 Miscellaneous Intel® GMCH Items

Checklist Item	Recommendation	Reason/Impact/Documentation
PWR0K	<ul style="list-style-type: none"> Connect to PWRGD_3V in Glue4 	Refer to Section 10.
RSTIN#	<ul style="list-style-type: none"> Connect to PCIRST# on the ICH4 through a 0 Ω resistor and tie to GND through a 10 pF 5% cap 	
RSVD	<ul style="list-style-type: none"> No Connect 	
VCCGPIO	<ul style="list-style-type: none"> Connect to 3.3 V and termination to GND with a 0.1 μF decoupling capacitor 	
VCC	<ul style="list-style-type: none"> Connect to 1.5 V power plane 	Refer to Section 14.2.

17.8 Clock Interface CK_408 Items

Checklist Item	Recommendation	Reason/Impact/Documentation
3V66_0	<ul style="list-style-type: none"> Connect to CLKIN in GLUECHIP4 Connect to a series $33\ \Omega \pm 5\%$ resistor 	
3V66_1	<ul style="list-style-type: none"> No Connect 	
3V66_2	<ul style="list-style-type: none"> Connect to GCLKIN in GMCH Connect to a series $33\ \Omega \pm 5\%$ resistor 	CLK66 Clock Group Refer to Section 13.1.
3V66_3	<ul style="list-style-type: none"> Connect to CLK66 in ICH4 Connect to a series $33\ \Omega \pm 5\%$ resistor 	CLK66 Clock Group Refer to Section 13.1.
3V66_4	<ul style="list-style-type: none"> Connect to AGPCLK in AGP Connect to a series $33\ \Omega \pm 5\%$ resistor 	CLK66 Clock Group Refer to Section 13.1.
66_IO	<ul style="list-style-type: none"> No Connect 	
CPU0	<ul style="list-style-type: none"> Connect to BCLK0 in CPU Connect to a series $27.4\ \Omega \pm 1\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor 	Host Clock Group Refer to Section 13.2.1.
CPU0#	<ul style="list-style-type: none"> Connect BCLK1 in CPU Connect to a series $27.4\ \Omega \pm 1\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor 	
CPU1	<ul style="list-style-type: none"> Connect to ITP_CLK0 in CPU Connect to BCLKP on ITP Connect to a series $27.4\ \Omega \pm 1\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor 	Host Clock Group Refer to Section 13.2.1.
CPU1#	<ul style="list-style-type: none"> Connect to ITP_CLK1 in CPU Connect to BCLKN on ITP Connect to a series $27.4\ \Omega \pm 1\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor 	
CPU2	<ul style="list-style-type: none"> Connect to HCLKN in GMCH Connect to a series $27.4\ \Omega \pm 1\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor 	Host Clock Group Refer to Section 13.2.1.
CPU2#	<ul style="list-style-type: none"> Connect to HCLKP in GMCH Connect to a series $27.4\ \Omega \pm 1\%$ resistor and terminate to GND through a $49.9\ \Omega \pm 1\%$ resistor 	Host Clock Group Refer to Section 13.2.1.
CPU_STOP#	<ul style="list-style-type: none"> Connect to VCC3_CLK through a $1\ \text{k}\Omega \pm 5\%$ resistor 	Host Clock Group Refer to Section 13.2.1.
DOT_48MHz	<ul style="list-style-type: none"> Connect to DREFCLK in GMCH Connect to a series $33\ \Omega \pm 5\%$ resistor 	Refer to Section 13.2.2



Checklist Item	Recommendation	Reason/Impact/Documentation
REF0	<ul style="list-style-type: none"> Connect to CLK14 in ICH4 through a series 33 Ω ±5% resistor Connect to CLK14 in SIO through a series 33 Ω ±5% resistor 	Refer to Section 13.2.6.
IREF	<ul style="list-style-type: none"> Terminate to GND through a 475 Ω ±1% resistor 	Refer to Section 13.2.1.
VSS_IREF	<ul style="list-style-type: none"> Terminate to GND 	
MULT0	<ul style="list-style-type: none"> Connect to VCC3_CLK through a series 10 kΩ ±5% resistor and terminate to GND through a 1 kΩ ±1% resistor 	Refer to Section 13.2.1.
PCI0	<ul style="list-style-type: none"> Connect to PCICLK on ICH4 Connect through a series 33 Ω ±5% resistor 	PCICLK Group Refer to Section 13.2.7.
PCI1	<ul style="list-style-type: none"> Connect to PCI_CLK on SIO Connect through a series 33 Ω ±5% resistor 	
PCI2	<ul style="list-style-type: none"> Connect to CLK in FWH Connect through a series 33 Ω ±5% resistor 	
PCI3	No connect	
PCI4	<ul style="list-style-type: none"> No connect or slot 4 for ATX MB Connect through a series 33 Ω ±5% resistor 	
PCI5	<ul style="list-style-type: none"> No connect or slot 5 for ATX MB Connect through a series 33 Ω ±5% resistor 	
PCI6	<ul style="list-style-type: none"> No connect or slot 6 for ATX MB Connect through a series 33 Ω ±5% resistor 	
PCIF[2:0]	<ul style="list-style-type: none"> Connect to a series 33 Ω ±5% resistor 	PCICLK Group Refer to Section 13.2.7.
PCI_STOP#	<ul style="list-style-type: none"> Terminate to VCC3_CLK through a 1 kΩ ±5% resistor 	PCICLK Group Refer to Section 13.2.7.
PWRDWN#	<ul style="list-style-type: none"> Terminate to VCC3_CLK through a 1 kΩ ±5% resistor 	
SEL_[1:0]	<ul style="list-style-type: none"> SEL0 terminate to VCC3_CLK through a 1 KΩ ± 5% resistor and terminate to GND through a series 0 Ω resistor. SEL1 connect to GMCH 	
SEL_2	<ul style="list-style-type: none"> Terminate to GND through a 1 kΩ ±5% resistor 	
SCLK	<ul style="list-style-type: none"> Connect to SCL in DIMMs 	
SDATA	<ul style="list-style-type: none"> Connect to SDA in DIMMs 	
USB_48Mhz	<ul style="list-style-type: none"> Connect to CLK48 in ICH4 through a series 33 Ω ±5% resistor 	
VDD	<ul style="list-style-type: none"> Terminate to VCC3_CLK 	
VDD_48MHz	<ul style="list-style-type: none"> Terminate to VCC3 through a 10 Ω ±5% resistor and terminate to GND through two parallel capacitor 	



Checklist Item	Recommendation	Reason/Impact/Documentation
VDDA	<ul style="list-style-type: none"> • Terminate to VCC3 and terminate to GND through two parallel capacitor 	
VSS	<ul style="list-style-type: none"> • Terminate to GND 	
VSS_48MHz	<ul style="list-style-type: none"> • Terminate to GND 	
VSSA	<ul style="list-style-type: none"> • Terminate to GND 	
VTT_PWRGD#	<ul style="list-style-type: none"> • Refer to DDR CRB for example 	
XTAL_IN	<ul style="list-style-type: none"> • Terminate to GND through a 10 pF $\pm 5\%$ capacitor 	Capacitor values may vary slightly from manufacturer to manufacturer.
XTAL_OUT	<ul style="list-style-type: none"> • Terminate to GND through a 10 pF $\pm 5\%$ capacitor 	Capacitor values may vary slightly from manufacturer to manufacturer.



17.9 Intel® ICH4 Interface

17.9.1 Intel® ICH4 IDE Items

Checklist Item	Recommendation	Reason/Impact/Documentation
IDERST#	<ul style="list-style-type: none"> The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal. 	
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	<ul style="list-style-type: none"> No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns. 	<p>These signals have integrated series resistors.</p> <p>NOTE: Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.</p>
PDD[15:0], SDD[15:0]	<p>No extra series termination resistors or other pull-ups/pull-downs are required.</p> <ul style="list-style-type: none"> PDD7/SDD7 does not require a 10 kΩ pull-down resistor. <p>Refer to ATA ATAPI-6 specification.</p>	<p>These signals have integrated series resistors.</p> <p>NOTE: Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.</p>
PDDREQ, SDREQ	<ul style="list-style-type: none"> No extra series termination resistors. No pull down resistors needed. 	<p>These signals have integrated series resistors in the ICH4.</p> <p>These signals have integrated pull down resistors in the ICH4.</p>
PIORDY, SIORDY	<ul style="list-style-type: none"> No extra series termination resistors. Pull-up to VCC3_3 via a 4.7 kΩ resistor. 	<p>These signals have integrated series resistors in the ICH4.</p>
IRQ14, IRQ15	<ul style="list-style-type: none"> Recommend 8.2 kΩ—10 kΩ pull-up resistors to VCC3_3. No extra series termination resistors. 	<p>Open drain outputs from drive.</p>
Cable Detect:	<ul style="list-style-type: none"> Host Side/Device Side Detection (recommended method): Connect IDE pin PDIAG#/CBLID to an ICH4 GPIO pin. Connect a 10 kΩ resistor to terminate to GND on the signal line. Device side detection: Connect a 0.047 μF capacitor from IDE pin PDIAG#/CBLID to terminate to GND. No ICH4 connection. 	<p>The 10 kΩ resistor to GND prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs.</p> <p>NOTE: All Ultra DMA drives supporting modes greater than Mode 2 will have the capability to detect cables</p>



17.9.2 Intel® ICH4 AC '97 Items

Checklist Item	Recommendation	Reason/Impact/Documentation
AC_SDOUT	<ul style="list-style-type: none"> Requires a jumper to 8.2 kΩ Pull Up resistor. Should not be stuffed for default operation. Series termination resistor 0 Ω to 47 Ω to on board codec and to the CNR 	This pin has a weak internal 20 k Ω nominal pull down. To properly detect a safe_mode condition a strong pull up will be required to over-ride this internal pull down.
AC_SDIN1, AC_SDIN0	<ul style="list-style-type: none"> Internal pull-downs in ICH4; no external pull-downs required. Series termination resistor 0 Ω to 47 Ω from the AC_SDIN lines to the ICH4 	These pins have a weak internal 20 k Ω nominal pull-down.
AC_SDIN2	<ul style="list-style-type: none"> Requires a 10 kΩ pull-down to ground if a CNR card is used on the platform. Series termination resistor 33 Ω to 47Ω from the AC_SDIN lines to the ICH4. 	<p>This pin has a weak internal 20 kΩ nominal pull-down. For platforms routing AC_SDIN2 to CNR the additional 10 kΩ pull-down is required to set the proper DC level for CNR card switching circuitry.</p> <p>Used for a codec detection/addressing mechanism on the CNR card.</p>
AC_BITCLK	<ul style="list-style-type: none"> No extra pull-down resistors required. Series termination resistor 33 Ω to 47 Ω from the motherboard codec to the ICH4 and also to the CNR 	This pin has a weak internal 20 k Ω nominal pull-down.
AC_SYNC	<ul style="list-style-type: none"> No extra pull-down resistors required. 	Some implementations add termination for signal integrity. Design specific.

17.9.3 Intel® ICH4 USB Items

Checklist Item	Recommendation	Reason/Impact/Documentation
USBRBIAS	<ul style="list-style-type: none"> 22.6 Ω \pm1% connected to ground 	
USBRBIAS#	<ul style="list-style-type: none"> Connected to the same 22.6 Ω \pm1% resistor to ground as USBRBIAS 	
USBP[5:0]P, USBP[5:0]N	<ul style="list-style-type: none"> No external resistors are required. 	Effective output driver impedance of 45 Ω provided
OC[5:0]#	<ul style="list-style-type: none"> If not used, use 10 kΩ \pm5% to VccSus3_3 	Inputs must not float
Unconnected USB data signals	<ul style="list-style-type: none"> Unconnected USB data signals can be left as no-connects 	

17.9.4 Intel® ICH4 Interrupt Interface Items

Checklist Item	Recommendation	Reason/Impact/Documentation
PIRQ[D:A]#	<ul style="list-style-type: none"> These signals require a pull-up resistor. Recommend a 2.7 kΩ pull up resistor to VCC5 or 8.2 kΩ ±5% to VCC3_3. 	<p>In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering Section. Each PIRQx# line has a separate Route Control Register.</p> <p>In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the ISA interrupts.</p>
PIRQ[H:E]#/GPIO[5:2]	<ul style="list-style-type: none"> These signals require a pull-up resistor. Recommend a 2.7 kΩ pull up resistor to VCC5 or 8.2 kΩ ±5% to VCC3_3. 	<p>In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering Section. Each PIRQx# line has a separate Route Control Register.</p> <p>In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees the ISA interrupts.</p>
SERIRQ	<ul style="list-style-type: none"> External weak (8.2 kΩ) pull up resistor to VCC3_3 is recommended. 	Open drain signal
APIC	<ul style="list-style-type: none"> If the APIC is used: 150 Ω pull-up resistors on APICD[1:0] Connect APICCLK to clock generator with a 20 Ω – 33 Ω series termination resistor. If the APIC is not used on up systems The APICCLK should be tied directly to GND. Pull APICD[1:0] to GND through a 10 kΩ pull-down resistor. If using XOR chain testing, a pull-down for each APIC signal is required (i.e., two 10 kΩ pull-down resistors). 	



17.9.5 Intel® ICH4 System Bus / SMLink Interface Items

Checklist Item	Recommendation	Reason/Impact/Documentation
SMBDATA, SMBCLK	<ul style="list-style-type: none"> Require external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.) Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. Required to be tied to SMLink signals for SMBus 2.0 compliance. SMBCLK should be tied to SMLINK0 and SMBDATA should be tied to SMLINK1 	Value of pull-ups resistors determined by line load.
SMBALERT#/ GPIO11	<ul style="list-style-type: none"> See GPIO section if SMBALERT# not implemented. 	
SMLINK[1:0]	<ul style="list-style-type: none"> Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.) Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. Required to be tied to SMLink signals for SMBus 2.0 compliance. SMBCLK should be tied to SMLINK0 and SMBDATA should be tied to SMLINK1 	Value of pull-ups resistors determined by line load.
INTRUDER#	<ul style="list-style-type: none"> Pull signal to VCCRTC (VBAT) through 10 kΩ resistor. 	Signal in VCCRTC (VBAT) well.

17.9.6 Intel® ICH4 PCI Interface Items

Checklist Item	Recommendation	Reason/Impact/Documentation
FYI	All inputs to the ICH4 must not be left floating	Many GPIO signals are fixed inputs that must be pulled up to different sources. See GPIO section for recommendations.
PERR#, SERR#, PLOCK#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#, REQ[4:0]#, GPIO0/REQA#, GPIO1/REQB#/REQ5	<ul style="list-style-type: none"> These signals require a pull up resistor. Recommend an 8.2 KΩ pull up resistor to VCC3_3 or a 2.7 KΩ pull up resistor to VCC5. 	See PCI 2.2 Component Specification pull-up recommendations for VCC3_3 and VCC5.
PCIGNT#[4:0]	<ul style="list-style-type: none"> No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented they must be pulled up to VCC3_3. 	These signals are actively driven by the ICH4
GNTA# /GPIO16, GNTB/ GNT5#/ GPIO17	<ul style="list-style-type: none"> No extra pull-up needed 	<p>These signals have integrated pull-ups of 24 kΩ.</p> <p>GNTA has an added strap function of "top block swap". The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull down resistor can be added to manually enable the function.</p>
PCIRST#	<ul style="list-style-type: none"> The PCIRST# signal should be buffered to form the IDERST# signal 33 Ω series resistor to IDE connectors. 	Improves Signal Integrity
PME#	<ul style="list-style-type: none"> No extra pull-up needed 	This signal has integrated pull-up of 18 k Ω to 42 k Ω .
IDSEL (on PCI Connector)	<ul style="list-style-type: none"> If connected must have a 300 Ω to 900 Ω series termination resistor 	



17.9.7 Intel® ICH4 RTC Items

Checklist Item	Recommendation	Reason/Impact/Documentation
VBIAS	<ul style="list-style-type: none"> The VBIAS pin of the ICH4 is connected to a 0.047 μF cap. 	For noise immunity on VBIAS signal
RTCX1, RTCX2	<ul style="list-style-type: none"> Connect a 32.768 kHz Crystal Oscillator across these pins with a 10M Ω resistor and use 18 pF decoupling caps at each signal (based on a crystal load of 12.5 pF). 	<p>The ICH4 implements new internal oscillator circuit as compared with the PIIX4 to reduce power consumption. The external circuitry shown in the DG will be required to maintain the accuracy of the RTC.</p> <p>The circuitry is required because the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.</p>
RTCRST#	<ul style="list-style-type: none"> Time constant due to RC filter on this line should be 18–25 ms. Recommended value for Resistor = 180 KΩ and Capacitor is 0.1 μF 	Timing Requirement

17.9.8 Intel® ICH4 LAN Items

Checklist Item	Recommendation	Reason/Impact/Documentation
LANCLK	<ul style="list-style-type: none"> Connect to LAN_CLK on platform LAN connect device. 	ICH4 contains integrated 100 k Ω nominal pull-down resistor on signal.
LANRXD[2:0]	<ul style="list-style-type: none"> Connect to LAN_RXD on platform LAN connect device. 	ICH4 contains integrated 10 k Ω pull-up resistors on interface.
LANTXD[2:0], LANRSTSYNC	<ul style="list-style-type: none"> Connect to LAN_TXD on platform LAN connect device. 	
If the LAN connect Interface is not used	<ul style="list-style-type: none"> platform LAN connect interface can be left NC if not used. 	Input buffers internally terminated
82540EM and 1000Base-T designs if applicable		Refer to DG Section 10.10.2.

17.9.9 Intel® ICH4 FWH/LPC Interface Items

Checklist Item	Recommendation	Reason/Impact/Documentation
FWH[3:0]/ LAD[3:0], LDRQ[1:0]	<ul style="list-style-type: none"> No extra pull-ups required. Connect straight to FWH/LPC 	ICH4 Integrates 20 kΩ nominal pull-up resistors on these signal lines.
FWH Decoupling	<ul style="list-style-type: none"> Follow Vendor recommendation 	

17.9.10 Intel® ICH4 EEPROM Interface Items

Checklist Item	Recommendation	Reason/Impact/Documentation
EE_DIN	<ul style="list-style-type: none"> No extra circuitry required. Connect to EE_DOUT of EEPROM or CNR Connector 	<p>ICH4 contains integrated 20 kΩ nominal pull-up resistor for this Signal.</p> <p>Connected to EEPROM data output signal.</p> <p>(Output from EEPROM perspective and input from ICH4 perspective.)</p>
EE_DOUT	<ul style="list-style-type: none"> Prototype Boards using internal LAN should include a placeholder for a pull-down resistor on this signal line, but do not populate the resistor. Connect to EEDIN of EEPROM or CNR Connector. 	<p>ICH4 contains integrated 20 kΩ nominal pull-up resistor for this Signal.</p> <p>Connected to EEPROM data input signal</p> <p>(Input from EEPROM perspective and output from ICH4 perspective.)</p>



17.9.11 Intel® ICH4 Power Management Items

Checklist Item	Recommendation	Reason/Impact/Documentation
LAN_RST#	<ul style="list-style-type: none"> Recommend a 10 kΩ pull-down to ground. This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Can be tied to RSMRST#. 	Timing Requirement
PWRBTN#	<ul style="list-style-type: none"> No extra pull-up resistors 	This signal has an integrated pull-up of 18 kΩ – 42 kΩ. This signal is internally debounced inside the ICH4
PWROK	<ul style="list-style-type: none"> Recommend a 10 kΩ pull-down to ground. This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCC3_3 and VCC1_5 have reached their nominal voltages 	Timing Requirement
RI#	<ul style="list-style-type: none"> RI# does not have an internal pull-up. Recommend an 8.2 kΩ pull-up resistor to Resume well 	If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.
RSMRST#	<ul style="list-style-type: none"> Recommend a 10 kΩ pull-down to ground. This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Can be tied to LAN_RST#. 	Timing Requirement
SLP_S3#, SLP_S4#, SLP_S5#	<ul style="list-style-type: none"> No pull up/down resistors needed. Signals driven by ICH4. 	Signals driven by ICH4
SYS_RESET#	<ul style="list-style-type: none"> Recommend an 8.2 kΩ pull-up resistor to VccSus3_3. Also, a (100 Ω to 8.2 kΩ) pull-down resistor isolated from SYS_RESET# by means of a normally open switch 	Input to ICH4 cannot float. This pin forces an internal reset to the ICH4 after the signal is internally debounced.
THRM#	<ul style="list-style-type: none"> Connect to temperature Sensor. Pull up if not used (an 8.2 kΩ pull up resistor to VCC3_3). 	Input to ICH4 cannot float. THRM# polarity bit defaults THRM# to active low, so pull up.
THRMTRIP#	<ul style="list-style-type: none"> A weak (62Ω ±5%) pull-up resistor to the V_CPU_IO well. See Processor Design Guide for specific pull-up value 	Input to ICH4 cannot float.
GPIO24	<ul style="list-style-type: none"> No pull-up required. 	



17.9.12 Processor Items

Checklist Item	Recommendation	Reason/Impact/Documentation
A20M#, CPU_SLP#, IGNNE#, INTR, NMI, SMI#, STPCLK#	<ul style="list-style-type: none">• Pull-up resistor to VCCCPU required if input to V_CPU_IO $\leq 0.8V$.	Push/pull buffers now drive the output signals.
INIT#		See Section 4.3.1.5.
FERR#	<ul style="list-style-type: none">• Requires weak ($62\Omega \pm 5\%$) external pull-up resistor to V_CPU_IO.	
RCIN#, A20GATE	<ul style="list-style-type: none">• Pull up signals to VCC3_3 through a 10K Ω resistor.	Typically driven by Open Drain External Micro-controller
CPUPWRGD	<ul style="list-style-type: none">• Connect to the CPU's CPUPWRGD input. Requires weak external pull-up resistor.	Refer to CPU Documentation of the processor for specific values. This signal represents a logical AND of the ICH4's PWROK and VRMPWRGD signals.

17.9.13 Intel® ICH4 GPIO Items

Checklist Item	Recommendation	Reason/Impact/Documentation
GPIO Pins	<p>GPIO[7:0]:</p> <ul style="list-style-type: none"> • These pins are in the Main Power Well. Pull-ups must use the VCC3_3 plane. • Unused core well inputs must be pulled up to VCC3_3. • GPIO[1:0] can be used as REQ[B:A]#. • GPIO1 can be used as PCI REQ5#. • GPIO[5:2] can be used as PIRQ[H:E]#. • GPIO6 • These signals are 5 V tolerant • These pins are inputs <p>GPIO8 & [13:11]:</p> <ul style="list-style-type: none"> • These pins are in the Resume Power Well. Pull-ups go to VccSus3_3 plane. • Unused resume well inputs must be pulled up to VccSus3_3. • These signals are NOT 5 V tolerant. • GPIO11 can be used as SMBALERT#. • These pins are inputs <p>GPIO[23:16]:</p> <ul style="list-style-type: none"> • Fixed as output only. Can be left NC. • GPIO22 is open drain. • GPIO[17:16] can be used as GNT[B:A]#. • GPIO17 can be used as PCI GNT5#. • GPIO18 • GPIO19 • GPIO20 • GPIO21 • GPIO22 • GPIO23 • These signals are NOT 5 V tolerant <p>GPIO[28, 27, 25, 24]:</p> <ul style="list-style-type: none"> • I/O pins. Default as outputs so can be left as NC • These pins are in the Resume Power Well • GPIO[28:27, 25] From resume power well. (Note: use pull-up to VccSus3_3 if these signals are pulled up) • GPIO24: No pull-up required • These signals are NOT 5 V tolerant <p>GPIO[43:32]:</p> <ul style="list-style-type: none"> • I/O pins. From main power well. • Default as outputs. • These signals are NOT 5 V tolerant. 	<p><i>Ensure ALL unconnected signals are OUTPUTS ONLY!</i></p>

17.9.14 Intel® ICH4 Miscellaneous Items

Checklist Item	Recommendation	Reason/Impact/Documentation
SPKR	<ul style="list-style-type: none"> Refer to Section 10.2.3 	Has integrated pull-down. The integrated pull-down is only enabled at boot/reset for strapping functions; at all other times, the pull-down is disabled.
TP0	<ul style="list-style-type: none"> Requires external pull-up resistor to VccSus3_3 	

17.10 Platform Power and Ground

17.10.1 Intel® ICH4 Power and Ground Items

Checklist Item	Recommendation	Reason/Impact/Documentation
HI_REF	<ul style="list-style-type: none"> 350 mV (See voltage divider recommendations in the HI section of this DG) 	
VCC3_3	<ul style="list-style-type: none"> Use six 0.1 μF decoupling cap 	
VCC1_5	<ul style="list-style-type: none"> Use two 0.1 μF decoupling caps 	
V5_REF	<ul style="list-style-type: none"> Use one 0.1 μF decoupling cap V5_REF is the reference voltage for 5 V tolerant inputs in the ICH4. V5_REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3. 	
VccSus3_3	<ul style="list-style-type: none"> Use two 0.1 μF decoupling caps 	
VccSus1_5	<ul style="list-style-type: none"> Use two 0.1 μF decoupling caps 	
V5_REF_SUS	<ul style="list-style-type: none"> Use one 0.1 μF decoupling cap V5REF is the reference voltage for 5 V tolerant inputs in the ICH4. V5_REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3. For most platforms this is not an issue because VccSus3_3 is usually derived from V5_REF_Sus. 	
V_CPU_IO[2:0]	<ul style="list-style-type: none"> Connect to the proper power plane for the CPU's CMOS compatibility signals Connect one 0.1 μF decoupling capacitor 	Used to pull up all CPU I/F signals
VccPLL	<ul style="list-style-type: none"> Use one 0.1 μF decoupling cap and one 0.01 μF decoupling cap 	
VccHI	<ul style="list-style-type: none"> Use two 0.1 μF decoupling caps 	
VccRTC	<ul style="list-style-type: none"> No clear CMOS jumper on VccRTC Use a jumper on RTCRST# or a GPI, or use a safe mode strapping for Clear CMOS Use one 0.1 μF decoupling cap 	
VSS	<ul style="list-style-type: none"> Connect to GND 	



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18 Intel® 845G Chipset Design Layout Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements the 845G chipset. The items contained within this checklist attempt to address important connections to these devices and any critical supporting circuitry. **This is not a complete list, and it does not guarantee that a design will function properly.** Beyond the items contained in list, refer to Customer Reference Board schematics in Appendix A for more detailed instructions on designing a motherboard. This work is ongoing, and the recommendations and considerations herein are subject to change.

18.1 Processor and System Bus

18.1.1 AGTL+ Signals

Data Signals: HD [63:0]#, DINV [3:0]# Data Strobes: HDSTB_P[3:0]#, HDSTB_N[3:0]# Address Signals: HA [31:3]#, HREQ [4:0]# Address Strobes: HADSTB_[1:0]#	
Recommendation	Reason/Impact/Documentation
General Guidelines	
<ul style="list-style-type: none"> Point to Point Topology 	Refer to Table 3
<ul style="list-style-type: none"> Referenced to VSS 	Layer changes should not occur for any signals. If a layer change must occur, reference plane must be VSS and the layers must all be of the same configuration Refer to Table 3
<ul style="list-style-type: none"> Route Data bus first Route Address bus second (after the Data bus) Route Common clock third 	Refer to Table 3
<ul style="list-style-type: none"> Breakout Guidelines (processor and GMCH): 7 mil wide with 5 mil spacing for a max of 250 mils from component ball 	Refer to Table 3
<ul style="list-style-type: none"> Data and common clock traces should be 7mils wide with 13 mil spacing 	Intel has simulated these recommendations for normal conditions. Refer to Section 4.2.2.1.
Group Spacing: Non Clock Spacing = 20 mils to any other signal	Refer to Table 3



Data Signals: HD_[63:0]#, DINV_[3:0]# Data Strobes: HDSTB_P[3:0]#, HDSTB_N[3:0]# Address Signals: HA_[31:3]#, HREQ_[4:0]# Address Strobes: HADSTB_[1:0]#	
Recommendation	Reason/Impact/Documentation
Data Signals / Data Strobes	
<ul style="list-style-type: none"> Data line 2.0" to 8" pin to pin data signal lengths Length compensation required 	The length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without trace matching and length compensation flight times between the data signals and the strobes will result in inequity between the setup and hold times. Refer to Section 4.2.2.1.
<ul style="list-style-type: none"> Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Signals should be referenced to VSS. 	The length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without trace matching and length compensation flight times between the data signals and the strobes will result in inequity between the setup and hold times. Refer to Section 4.2.2.1.
<ul style="list-style-type: none"> Data strobe and its complement should be routed to the same length as their corresponding data signals; mean pad-to-pad length should be ± 25 mils. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (VSS), and the layers are of the same configuration (all stripline or all microstrip). DSTBN/P[3:0]# 	The impact of this recommendation causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. It is recommended to simulate skew to determine the length that best centers the strobe for a given system. Refer to Section 4.2.2.1.
<ul style="list-style-type: none"> Data strobes and their complements should be routed within ± 25 mils of the same pad to pad length If one strobe switches layers, its complement must switch layers in the same manner 	The impact of this recommendation causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. It is recommended to simulate skew to determine the length that best centers the strobe for a given system. Refer to Section 4.2.



Data Signals: HD_[63:0]#, DINV_[3:0]# Data Strobes: HDSTB_P[3:0]#, HDSTB_N[3:0]# Address Signals: HA_[31:3]#, HREQ_[4:0]# Address Strobes: HADSTB_[1:0]#	
Recommendation	Reason/Impact/Documentation
Address Signals / Address Strobes	
<ul style="list-style-type: none"> Address line 2.0" to 10.0" pin to pin data signal lengths Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (VSS), and the layers are of the same configuration (all stripline or all microstrip). Length compensation required 	<p>The length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without trace matching and length compensation flight times between the data signals and the strobes will result in inequity between the setup and hold times.</p> <p>Refer to Section 4.2.2.1..</p>
<ul style="list-style-type: none"> Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes Length compensation required Address signals may change layers if reference plane remains the same (VSS), and the layers are of the same configuration. 	<p>The length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without trace matching and length compensation flight times between the Address signals and the strobes will result in inequity between the setup and hold times.</p> <p>Refer to Section 4.2.</p>
<ul style="list-style-type: none"> Address Strobes (HADSTB_[1:0]#) should be routed to the same length as their corresponding address signals, mean pad to pad length should be ± 25 mils Length compensation required Address strobes may change layers if reference plane remains the same (VSS), and the layers are of the same configuration. 	<p>The impact of this routing recommendation causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times.</p> <p>Refer to Section 4.1.</p>
<ul style="list-style-type: none"> ADSTB0 and ADSTB1 should be routed within ± 25 mils of the same pad-to-pad length 	Refer to Table 3
Common Clock BCLK[1:0]	
<ul style="list-style-type: none"> 3.0" to 10.0" pin-to-pin common clock lengths. No length compensation necessary 	Refer to Table 3
<ul style="list-style-type: none"> Common clock should be 7 mils wide and 13 mils spacing. 	Refer to Section 4.2.2.1.
Trace Impedance	50 $\Omega \pm 15\%$
Maximum via count per signal	<p>4</p> <p>Avoid layer change as much as possible.</p> <p>No layer change is recommendation.</p> <p>Refer to Section 4.1.</p>



18.1.2 Asynchronous GTL+ and Miscellaneous AGTL+ Signals

Processor:	FERR#, PROCHOT#, THERMTRIP#
Intel® ICH4:	A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI#, STPCLK#, PWRGOOD
Miscellaneous AGTL+:	BREQ0#, RESET#
Recommendation	Reason/Impact/Documentation
General Guidelines	
<ul style="list-style-type: none"> Point to Point Topology 	
<ul style="list-style-type: none"> Referenced to VSS 	
<ul style="list-style-type: none"> 5 mils wide with 7 mil spacing 	
<ul style="list-style-type: none"> Breakout Guidelines: None 	
FERR#, THERMTRIP# <ul style="list-style-type: none"> 1"–12" from processor to ICH4 3" max from ICH4 to VDD 	Refer to Sections 4.3.1.1 and 4.3.1.3
PROCHOT# <ul style="list-style-type: none"> 1" – 17" from processor to voltage translator 3" max from Voltage translator to VDD 10" max from Voltage translator to external logic 	Refer to Section 4.3.1.2.
A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, STPCLK# <ul style="list-style-type: none"> 17.0" max from Processor to Rs 2.0" max from Rs to ICH4 	Refer to Section 4.3.1.4.
INIT# <ul style="list-style-type: none"> 3" max from VCC_CPU to Processor 17" max from Processor to ICH4. 2.0" max from ICH4 to Voltage Translator. 10" max from voltage translator to FWH. 3" max from VCC_FWH to FWH Level shifting is required from the INIT# pin to FWH. 	Refer to Section 4.3.1.5.
PWRGOOD <ul style="list-style-type: none"> 1.0" to 12.0" max from processor to Rs 2" max from Rs to ICH4 3.0" max from processor to VDD 	Refer to Section 4.3.1.6.



Processor: FERR#, PROCHOT#, THERMTRIP# Intel® ICH4: A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI#, STPCLK#, PWRGOOD Miscellaneous AGTL+: BREQ0#, RESET#	
Recommendation	Reason/Impact/Documentation
BREQ0#, Reset# <ul style="list-style-type: none"> • Terminate using discrete components on the system board • Connect the signals between these components • ≤ 1" – 2" max from processor to Rt. • BREQ0#: Rt = 150 Ω to 220 Ω ± 5% • RESET#: Rt = 51 Ω ± 5% • ≤ 3" – 10" max from processor to GMCH 	Refer to Section 4.3.1.8.

18.1.3 Miscellaneous Signals

Miscellaneous: COMP[1:0], THERMDA, THERMDC	
Recommendation	Reason/Impact/Documentation
COMP[1:0] <ul style="list-style-type: none"> • Terminate to ground through a 51 Ω ± 1% resistor as close as possible to the pin. • Do not wire COMP pins together. Connect each pin to its own termination resistor. • RCOMP value can be adjusted to set external drive strength of I/O and to control the edge rate. • Minimize the distance from terminating resistor 	Refer to Section 4.3.1.9
THERMDA, THERMDC <ul style="list-style-type: none"> • 10 mils wide by 10 mil spacing • Remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4.0" to 8.0" away as long as the worst noise sources such as clock generators, data, buses and address buses, etc are avoided • Route in parallel and close together with ground guards enclosed 	Refer to Section 4.3.1.10.
TESTHI Pins <ul style="list-style-type: none"> • The TESTHI pins should be tied to the VCC_CPU via a matched resistor that has a resistance value within ± 20% of the impedance of the board transmission line traces. 	Refer to Section 4.3.1.11.
Reserved Pins <ul style="list-style-type: none"> • Leave as No Connects 	



18.1.4 Decoupling, VREF, and Filtering

Recommendation	Reason/Impact/Documentation
<p>VCC_CPU Decoupling</p> <p>Recommended Bulk and High Frequency Decoupling devices:</p> <ul style="list-style-type: none"> • (9) OSCONs*, 560μF caps <ul style="list-style-type: none"> —ESR 9.28 mΩ, max —ESL 6.4 nH, max —Ripple Current Rating 4.080 Arms • (3) Al Electrolytic, 3300 μF <ul style="list-style-type: none"> —ESR 12 mΩ —ESL 5 nH • (24) 0805 package, 10 μF caps • (14) 1206 package, 10 μF caps <ul style="list-style-type: none"> —ESR 3.5 m , typ —ESL 1.15 nH, typ • The decoupling should be placed as close as possible to the processor power pins • If (38) 1206s are used, place 14 north, 10 inside, and 14 south of the socket. 	<p>Refer to Table 17</p>
<p>Processor GTLREF</p> <ul style="list-style-type: none"> • The processor must have one dedicated voltage divider • Keep the voltage divider within 1.5" of the GTLREF pin • Keep signal routing at least 10 mils separated from the GTLREF routes. Use a minimum of a 7 mil trace for routing • Do not allow signal lines to use the GTLREF routing as part of their return path <p>GTLREF Decoupling:</p> <ul style="list-style-type: none"> • Decouple voltage divider with a 1μF capacitor • Decouple pin with a high frequency capacitor (such as a 220 pF 603) • Place cap as close to pin as possible 	<p>Refer to Section 4.1.1.</p>
<p>VCCA, VCCIOPLL, and VSSA Filtering for Processor</p> <ul style="list-style-type: none"> • Use shielded type inductors • Minimize the distance between VCCA, VSSA pins and capacitors • VCCA should be routed parallel and next to VSSA route • Filter capacitors and inductors should be routed next to each other 	<p>Refer to Section 4.6.5.1.</p>



Recommendation	Reason/Impact/Documentation
GMCH HVREF <ul style="list-style-type: none">• 12mils wide, 3.0" max length• 10mil group spacing• Place 0.1 μF decoupling capacitor at the GMCH• Minimize the distance between the voltage divider, decoupling capacitors and GMCH	Refer to Section 4.1.2.
GMCH HSWNG <ul style="list-style-type: none">• Trace to voltage divider 12 mils wide, 3.0" max length• 10mil group spacing• Place 0.01 μF decoupling capacitor at the GMCH• Minimize the distance between the voltage divider, decoupling capacitors and GMCH	Refer to Section 4.1.2.
GMCH HRCOMP <ul style="list-style-type: none">• Trace to each resistor 10 mils wide, 0.5" max length• 7 mils group spacing• Minimize the distance between HRCOMP and the GMCH	Refer to Section 4.1.2.



18.2 System Memory (DDR)

18.2.1 DDR-SDRAM

Data Signals: SDQ_[63:0], SDM_[7:0], SDQS_[7:0]	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Daisy Chain Topology 	Refer to Section 5.2.1.
<ul style="list-style-type: none"> Resistor packs for Data signals are not shared with any other signal groups 	
<ul style="list-style-type: none"> Ground Referenced 	<p>To provide an optimal current return path. The ground flood should be solid and continuous from the GMCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel.</p> <p>Refer to Section 5.2.1.</p>
<ul style="list-style-type: none"> Data and strobe signals should be routed entirely on the top signal layer 	<p>The GMCH pinout has been optimized to breakout all data and strobe signals on the top signal layer.</p> <p>Refer to Section 5.2.1.</p>
<ul style="list-style-type: none"> 5 mils wide 	Refer to Section 5.2.1.
<p>Trace Spacing</p> <ul style="list-style-type: none"> 15 mil spacing SDQS to SDQ/SDM 10 mil spacing SDQ/SDM to SDQ/SDM 7 mil min spacing within DIMM Pin Field 12 mil spacing from DIMM to DIMM 7 mil min spacing from 2nd DIMM to Rtt 	Refer to Section 5.2.1.
<ul style="list-style-type: none"> 20 mil min Isolation Spacing from Non-DDR Related Signals 	Refer to Section 5.2.1.
<p>Breakout guideline:</p> <ul style="list-style-type: none"> 5 mils wide by 6 mil spacing for a max of 350 mils This breakout spacing should be minimized 	Refer to Section 5.2.1.
<ul style="list-style-type: none"> 5.8" max total trace length from GMCH signal Pad to First DIMM Pin 	<p>Refer to Section 5.2.7.</p> <p>Max value includes package length.</p>
<ul style="list-style-type: none"> 500 mils max trace length from series termination resistor ($10 \Omega \pm 5\%$) pad to 1st DIMM pin 	Refer to Section 5.2.1.
<ul style="list-style-type: none"> 400 mils to 600 mils trace length from DIMM pin to DIMM pin 	Refer to Section 5.2.1.
<ul style="list-style-type: none"> 800 mils max trace length from last DIMM pin to parallel termination resistor ($56 \Omega \pm 5\%$) pad 	Refer to Section 5.2.1.
<ul style="list-style-type: none"> 0 vias max (all signals are routed on the top layer) 	



Data Signals: SDQ_[63:0], SDM_[7:0], SDQS_[7:0]	
Recommendation	Reason/Impact/Documentation
Required length matching: <ul style="list-style-type: none"> • SDQ_[63:0] / SDM_[7:0] to associated SDQS_[7:0] • SDQS_[7:0] to SCMD_CLK/SCMDCLK_[5:0]# for corresponding DIMM 	Refer to Section 5.2.1.1.1 and 5.2.1.1.2.

Control Signals: SCKE_[3:0], SCS_[3:0]#	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> • Point-to-Point Topology 	Refer to Section 5.2.2.
<ul style="list-style-type: none"> • Ground Referenced 	To provide an optimal current return path. The ground flood should be solid and continuous from the GMCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel. Refer to Section 5.2.2.
<ul style="list-style-type: none"> • Control signals should be routed on the bottom signal layer or until they transition to the top signal layer, within 500 mils before the first DIMM connector. • Control signals need to be routed on the same layer 	The GMCH pinout has been optimized to breakout the control signals onto the bottom signal layer. Refer to Section 5.2.2.
<ul style="list-style-type: none"> • Control signals should be as short as possible 	Because the control signals are routed on the bottom signal layer, the 2.5 V copper flooding on the bottom layer is reduced. This flooding should be maximized for better 2.5 V power delivery to the GMCH and DIMMs. Refer to Section 5.2.2.
<ul style="list-style-type: none"> • Resistor packs for Control signals must not be shared with any other signal groups. 	
<ul style="list-style-type: none"> • 5 mils wide 	Refer to Section 5.2.2.
Trace Spacing <ul style="list-style-type: none"> • 12 mil spacing from GMCH to 1st DIMM • 7 mil min spacing within DIMM Pin Field • 12 mil spacing from DIMM to DIMM • 7 mil min spacing from 2nd DIMM to Rtt 	Refer to Section 5.2.2.
<ul style="list-style-type: none"> • 20 mil min Isolation Spacing from Non-DDR Related Signals 	Refer to Section 5.2.2.
<ul style="list-style-type: none"> • 7 mil minimum Isolation Spacing from the 2.5 V Copper Flood on Layer Four 	Refer to Section 5.2.2.



Control Signals: SCKE_[3:0], SCS_[3:0]#	
Recommendation	Reason/Impact/Documentation
Breakout Guidelines <ul style="list-style-type: none"> • 5 mils wide with 6 mils spacing for a max of 350 mils • Breakout spacing should be minimized 	Refer to Section 5.2.2.1.
<ul style="list-style-type: none"> • 3.5" max from GMCH signal ball to DIMM Pins on 1st DIMM (SCS#/SCKE_[1:0]) <ul style="list-style-type: none"> —50 mil max from GMCH signal ball to 1st DIMM —500 mil max from 2nd Via to 1st DIMM 	Refer to Section 5.2.2.
<ul style="list-style-type: none"> • 4.0" max from GMCH signal ball to DIMM Pins on 2nd DIMM (SCS#/SCKE_[3:2]) <ul style="list-style-type: none"> —50 mil max from GMCH signal ball to 1st DIMM —1" max from 2nd Via to 2nd DIMM 	Refer to Section 5.2.2.
<ul style="list-style-type: none"> • 1.4" max from DIMM pins on 1st DIMM to Rtt (56Ω ± 5%) Pad (SCS#/SCKE_[1:0]) 	Refer to Section 5.2.2.
<ul style="list-style-type: none"> • 800 mils max from DIMM pins on 2nd DIMM to Rtt Pad (56 Ω±5%) 	Refer to Section 5.2.2.
<ul style="list-style-type: none"> • 4 via max (minimize number of vias over 2) 	
Length Tuning Method <ul style="list-style-type: none"> • SCS#/SCKE_[3:0] TO SCMDCLK/SCMDCLK_[5:0]# 	Refer to Section 5.2.2.1.

Address/Command Signals: SMAA_[12:6,3,0], SBA_[1:0], SRAS#, SCAS#, SWE#	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> • Daisy Chain Topology 	Refer to Section 5.2.3.
<ul style="list-style-type: none"> • Ground Referenced 	To provide an optimal current return path. The ground flood should be solid and continuous from the GMCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel. Refer to Section 5.2.3.
<ul style="list-style-type: none"> • Address/Command signals are routed on the bottom signal layer. • All Address/Command need to be routed on the same layer. 	The GMCH pinout has been optimized to breakout the address/ command signals onto the bottom signal layer. Refer to Section 5.2.3.
<ul style="list-style-type: none"> • Address/Command signals should be as short as possible. 	Because the control signals are routed on the bottom signal layer, the 2.5 V copper flooding on the bottom layer is reduced. This flooding should be maximized for better 2.5 V power delivery to the GMCH and DIMMs. Refer to Section 5.2.3.
<ul style="list-style-type: none"> • Resistor packs for Address/Command signals are not shared with any other signal groups. 	



Address/Command Signals: SMAA_[12:6,3,0], SBA_[1:0], SRAS#, SCAS#, SWE#	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> • 5 mils wide 	Refer to Section 5.2.3.
Trace Spacing <ul style="list-style-type: none"> • 12 mil spacing from GMCH to 1st DIMM • 7 mil min spacing within DIMM Pin Field • 12 mil spacing from DIMM to DIMM • 7 mil min spacing from 2nd DIMM to Rtt 	Refer to Section 5.2.3.
<ul style="list-style-type: none"> • 20 mil minimum Isolation Spacing from Non-DDR Related Signals 	Refer to Section 5.2.3.
<ul style="list-style-type: none"> • 7 mil min Isolation Spacing from the 2.5 V Copper Flood on Layer Four 	Refer to Section 5.2.3.
Breakout Guideline <ul style="list-style-type: none"> • 5 mils wide with 6 mil spacing for a max of 350 mils. • This breakout spacing should be minimized. 	Refer to Section 5.2.3.
<ul style="list-style-type: none"> • 4.0" max from GMCH signal ball to 1st DIMM pin —50 mil max from GMCH signal ball to 1st via 	Refer to Section 5.2.3.
<ul style="list-style-type: none"> • 400 mils to 600 mils from DIMM pin to DIMM pin 	Refer to Section 5.2.3.
<ul style="list-style-type: none"> • 800 mils max from Last DIMM Pin to Parallel Termination Resistor (56 Ω ± 5%) Pad 	Refer to Section 5.2.3.
<ul style="list-style-type: none"> • 4 vias max (Minimize number of vias over 2) 	
Length Tuning Required <ul style="list-style-type: none"> • SMAA_[12:6,3,0], SBA_[1:0], SRAS#, SCAS#, SWE# to SCMDCLK/SCMDCLK_[5:0]# for corresponding DIMM. 	Refer to Section 5.2.3.1.

CPC Address Signals: SMAA_[5,4,2,1] and SMAB_[5,4,2,1]	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Point to Point Topology 	Refer to Section 5.2.4.
<ul style="list-style-type: none"> Ground Referenced 	<p>To provide an optimal current return path. The ground flood should be solid and continuous from the GMCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel.</p> <p>Refer to Section 5.2.4.</p>
<ul style="list-style-type: none"> Resistor packs for CPC Address signals are not shared with any other signal groups. 	
<ul style="list-style-type: none"> CPC Address signals are routed on the bottom signal layer All CPC Address signals need to be routed on the same layer 	<p>The GMCH pinout has been optimized to breakout the CPC Address signals onto the bottom signal layer.</p> <p>Refer to Section 5.2.4.</p>
<ul style="list-style-type: none"> 5 mils wide SMAA_[5,4,2,1] to 1st DIMM 	Refer to Section 5.2.4.
<ul style="list-style-type: none"> 5 mils wide SMAB_[5,4,2,1] to 2nd DIMM 	Refer to Section 5.2.4.
<p>Trace Spacing</p> <ul style="list-style-type: none"> 12 mil spacing from GMCH to DIMM 8 mil min spacing within DIMM Pin Field 8 mil min spacing from DIMM to Rtt 	Refer to Section 5.2.4.
<ul style="list-style-type: none"> 20 mil minimum Isolation Spacing from Non-DDR Related Signals Max of 1 Address/Command signal can be routed next to a CPC signal. 	Refer to Section 5.2.4.
<ul style="list-style-type: none"> 7 mil min Isolation Spacing from the 2.5 V Copper Flood on Layer Four 	Refer to Section 5.2.4.
<p>Breakout Guideline</p> <ul style="list-style-type: none"> 5 mils wide with 6 mil spacing for up to the first 200 mils from ball 5 mils wide with 8 mil spacing for up to an additional 550 mils after the first 200 mils from the ball Use of breakout spacing should be minimized 	Refer to Section 5.2.4.
<ul style="list-style-type: none"> 2.5" max from GMCH signal ball to 1st DIMM (SMAA_[5,4,2,1]) —50 mil max from GMCH signal ball to 1st via 	Refer to Section 5.2.4.
<ul style="list-style-type: none"> 3.0" max from GMCH signal ball to 2nd DIMM (SMAB_[5,4,2,1]) —50 mil max from GMCH signal ball to 1st via 	Refer to Section 5.2.4.
<ul style="list-style-type: none"> 1.4" max from 1st DIMM pin to Parallel Termination resistor (33 Ω ± 5%) pad (SMAA_[5,4,2,1]) 	Refer to Section 5.2.4.
<ul style="list-style-type: none"> 800 mils max from 2nd DIMM Pin to Parallel Termination Resistor (33 Ω ± 5%) Pad (SMAB_[5,4,2,1]) 	Refer to Section 5.2.4.

CPC Address Signals: SMAA_[5,4,2,1] and SMAB_[5,4,2,1]	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> 4 vias max (minimize number of vias over 2) 	
<ul style="list-style-type: none"> Termination Resistor (Rtt) $33 \Omega \pm 5\%$ 	
Length Tuning Required <ul style="list-style-type: none"> SMAA_[5,4,2,1], SMAB_[5,4,2,1] to SCMDCLK/SCMDCLK_[5:0]# for corresponding DIMM 	Refer to Section 5.2.4.1.

Clock Signals: SCMDCLK_[5:0], SCMDCLK_[5:0]#	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Point to Point Topology 	Refer to Section 5.2.5.
<ul style="list-style-type: none"> Ground Referenced 	To provide an optimal current return path. The ground flood should be solid and continuous from the GMCH DDR signal pins all the way beyond the VTT termination capacitors at the end of the channel. Refer to Section 5.2.5.
<ul style="list-style-type: none"> Clock signals should be routed on the bottom signal layer 	The GMCH pinout has been optimized to breakout the CPC Address signals onto the bottom signal layer. Refer to Section 5.2.5.
<ul style="list-style-type: none"> All different clocks must be routed on the same layer. 	
<ul style="list-style-type: none"> Differential clock pairs must be routed differentially from the GMCH to their associated DIMM pins and must maintain the correct isolation spacing from other signals. 	Refer to Section 5.2.5.
<ul style="list-style-type: none"> Clocks must remain isolation spacing from itself during serpentines. 	Refer to Section 5.2.5.
<ul style="list-style-type: none"> 8 mils wide 	Refer to Section 5.2.5.
<ul style="list-style-type: none"> 5 mil Differential Trace Spacing between SCMDCLK and its corresponding SCMDCLK# 	Refer to Section 5.2.5.
<ul style="list-style-type: none"> Isolation spacing from another DDR signal group = 20 mils Isolation spacing from non-DDR related signals = 20 mils 	Refer to Section 5.2.5.
<ul style="list-style-type: none"> 10 mil minimum Isolation Spacing from the 2.5 V Copper Flood on Layer Four 	Refer to Section 5.2.5.
<ul style="list-style-type: none"> 20 mil min spacing from itself when serpentining 	Refer to Section 5.2.5.
Breakout Guideline <ul style="list-style-type: none"> 5 mils wide with 5 mils differential spacing with a minimum of 5 mils isolation spacing from another signal for a max of 350 mils. 	Refer to Section 5.2.5.



Clock Signals: SCMDCLK_[5:0], SCMDCLK_[5:0]#	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Total trace length of 7.4" max from GMCH signal pad to 1st DIMM (SCMDCLK_[2:0]) 50 mils max length from GMCH signal ball to via 	Refer to DG Section 5.2.5. See Section 5.2.7 for package length
<ul style="list-style-type: none"> Total trace length of 7.9" max from GMCH signal pad to 2nd DIMM (SCMDCLK_[5:3]) 50 mils max length from GMCH signal ball to via 	Refer to DG Section 5.2.5. See Section 5.2.7 for package length
Total Clock length relationship between 1 st DIMM and 2 nd DIMM: <ul style="list-style-type: none"> $(P+Y) = ((P+X)+0.5")$ $(P+X) =$ Total target clock length to 1st DIMM $(P+Y) =$ Total target clock length to 2nd DIMM 	
<ul style="list-style-type: none"> 1 via max (for breakout to bottom layer) 	
<ul style="list-style-type: none"> System memory signal lengths must be tuned to the total target length of the clock pairs SCMDSCK/SCMDCLK#. 	
Length Tuning Required <ul style="list-style-type: none"> SCMDCLK length to SCMDCLK# length, within ± 10 mils All 3 clock pairs to each DIMM are equal in length, within ± 10 mils where length includes package length compensation (P + A)	Refer to DG Section 5.2.5.1



Feedback Signals: SRCVEN_OUT#, SRCVEN_IN#	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none">Point to Point Topology with resistor site (unpopulated)	Refer to Section 5.2.6.
<ul style="list-style-type: none">Ground Referenced	Refer to Section 5.2.6.
<ul style="list-style-type: none">5 mils wide	Refer to Section 5.2.6.
<ul style="list-style-type: none">10 mil minimum Isolation Spacing from another DDR Signal Group or from Non-DDR Related Signals	
<ul style="list-style-type: none">100 mils max from GMCH SRCVEN_OUT# to series resistor	Refer to Section 5.2.6.
<ul style="list-style-type: none">100 mils max from series resistor to GMCH SRCVEN_IN#	Refer to Section 5.2.6.
<ul style="list-style-type: none">2 vias max	

18.2.2 DDR-SDRAM Decoupling, Compensation, and VREF

Recommendation	Reason/Impact/Documentation
<p>System Memory Bypass Caps</p> <ul style="list-style-type: none"> Place 9 evenly spaced 0.1µF 0603 capacitors between the DIMMs A wide trace should connect to a via that transitions to the ground cutout on layer two, and to the ground plane on layer three. The ground via should be placed as close to the ground pad as possible. A wide trace should connect the 2.5 V side of the cap to a via that transitions to the 2.5 V plane on layer four and then to the closest 2.5 V DIMM pin on either DIMM The 2.5 V traces should be distributed evenly between the two DIMMs The 2.5 V via should be placed as close to the 2.5 V pad as possible 	<p>Helps minimize return path discontinuities</p> <p>Refer to Section 5.3.</p>
<p>2.5 V Power Delivery Guidelines</p>	<p>Refer to Section 5.4.1.</p>
<p>GMCH System Memory High Frequency Decoupling</p> <ul style="list-style-type: none"> Place (8) 0.1 µF 0603 caps within 100 mils of the GMCH package Caps must be placed perpendicular to the GMCH, when appropriate, with the 2.5 V side of the caps facing the GMCH. The trace from the power end of the cap should be as wide as possible and it must connect to a 2.5 V power ball on the outer row of balls on the GMCH. Each capacitor should have two vias placed directly over a 2.5 V copper finger that is located on layer four. One via should be placed within 25 mils of the cap pad, while the other via should be placed within 25 mils of the power ball. If the trace from the solder ball to the capacitor is less than 100 mils, one of the vias may be omitted. The cap ground end must connect to the ground cutout on layer two and to the ground plane on layer three through a via that is placed within 25 mils of the cap pad. The trace from the ground via to the cap pad must be as wide as possible. 	<p>Refer to Section 5.4.2.1.</p>
<p>GMCH System Memory Low Frequency Bulk Decoupling</p> <ul style="list-style-type: none"> Place (4) 100 µF electrolytic evenly between the GMCH and the first DIMM connector. Place (1) 22 µF cap between the GMCH and the first DIMM connector on the top layer copper flood Power end of caps must connect to the 2.5 V on layer one or layer four. Ground end of caps must connect to ground on layer two and three. 	<p>Refer to Section 5.4.2.1.</p>

Recommendation	Reason/Impact/Documentation
<p>DDR DIMM Decoupling</p> <ul style="list-style-type: none"> • Place (3) 100 μF caps • One placed at the upper left, one at the bottom left, and one at the bottom right of the DIMM connectors • Power end of caps must connect to the 2.5 V on layer one and layer four. • Ground end of caps must connect to ground on layer two and three. 	<p>Refer to Section 5.4.3</p>
<p>DDR VREF</p> <ul style="list-style-type: none"> • Place VREF divider within 1.0" from the DIMMs (Two identical resistors 50 Ω – 150 Ω, 1%) • Place 0.1 μF decoupling cap at the GMCH and one 0.1 μF cap at each of the DIMM sockets • 12 mils wide min • 12 mil group spacing • Breakout: 7 mil spacing, 350 mils max. 	<p>Refer to Section 5.4.4</p>
<p>DDR SMRCOMP</p> <ul style="list-style-type: none"> • RCOMP Resistors – 60.4 $\Omega \pm 1\%$ pulled to DDR 2.5 V, and 60.4 $\Omega \pm 1\%$ tied to ground • 12 mils wide minimum • 10 mil group spacing 	<p>Refer to Section 5.4.5 for figure.</p>
<p>DDR VTT Termination</p> <ul style="list-style-type: none"> • All DDR signals, except the command clocks, must be terminated to 1.25 V (VTT) using 5% resistors at the end of the channel opposite the GMCH. • Place a solid 1.25 V (VTT) termination island on the top signal layer, just beyond the last DIMM connector. The VTT Termination Island must be at least 50 mils wide. • Use this termination island to terminate all DDR signals, using one resistor per signal. Resistor packs are acceptable, with the understanding that the signals within an RPACK must be from the same DDR signal group. • Termination resistor packs for each group must remain dedicated to that group, and not be shared with any other signal groups. • No mixing of signals from different DDR signal groups is allowed within an RPACK. The parallel termination resistors connect directly to the VTT Island on the top signal layer. 	<p>Refer to Section 5.4.6.</p>

18.3 System Memory (SDR)

18.3.1 2 DIMM SDR-SDRAM (PC133)

Data Signals: SDQ_[63:0], SDM_[7:0]	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Daisy Chain Topology 	Refer to Section 6.2.1.1.
<ul style="list-style-type: none"> 5 mils wide by 12 mil spacing 	Refer to Section 6.2.1.1.
<ul style="list-style-type: none"> 12 mil group spacing 	Refer to Section 6.2.1.1.
<ul style="list-style-type: none"> 2.0" to 4.0" from GMCH to first DIMM for SDM 	Refer to Section 6.2.1.1.
<ul style="list-style-type: none"> 2.0" to 4.4" from GMCH to first DIMM for SDQ – Zone 1 	Refer to Section 6.2.1.1.
<ul style="list-style-type: none"> 2.0" to 4.0" from GMCH to first DIMM for SDQ – Zone 2 	Refer to Section 6.2.1.1.
<ul style="list-style-type: none"> 0.4" to 0.6" from first DIMM to second DIMM 	Refer to Section 6.2.1.1.
Breakout guideline: <ul style="list-style-type: none"> 5 mils wide by 5 mil min spacing, 0.5" max length 	Refer to Section 6.2.1.1.

Control Signals Chip Select Signals: SCS_[7:0]# Clock Enable Signals: SCKE_[3:0]	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Point to Point Topology 	Refer to Section 6.2.1.2.
<ul style="list-style-type: none"> 5 mils trace width for SCS_[7:0]# 8 mils trace width for SCKE_[3:0] 12 mils minimum spacing 	Refer to Section 6.2.1.2.
<ul style="list-style-type: none"> 12 mils group spacing 	Refer to Section 6.2.1.2.
<ul style="list-style-type: none"> 3.0" to 4.0" from GMCH to DIMM 	Refer to Section 6.2.1.2.
Breakout guideline: <ul style="list-style-type: none"> 5 mils wide by 5 mil spacing, 0.5" max length 	Refer to Section 6.2.1.2.

Address/Command Signals: SMA[12:0], SBA_[1:0], SRAS#, SCAS#, SWE#	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Daisy Chain Topology 	Refer to Section 6.2.1.3.
<ul style="list-style-type: none"> 5 mils wide by 12 mil spacing 	Refer to Section 6.2.1.3.
<ul style="list-style-type: none"> 12 mil group spacing 	Refer to Section 6.2.1.3.



Address/Command Signals: SMA[12:0], SBA_[1:0], SRAS#, SCAS#, SWE#	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> • 2.0" to 3.5" from GMCH to first DIMM 	Refer to Section 6.2.1.3.
<ul style="list-style-type: none"> • 0.4" to 0.6" from first DIMM to second DIMM 	Refer to Section 6.2.1.3.
Breakout guideline: 5 mils wide by 5 mil spacing, 0.5" max length	Refer to Section 6.2.1.3.

Clock Signals: SCK_[7:0]	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> • Point to Point Topology w/AC Termination 	Refer to Section 6.2.1.4.
<ul style="list-style-type: none"> • 7 mils wide by 15 mil spacing 	Refer to Section 6.2.1.4.
<ul style="list-style-type: none"> • 15 mil group spacing 	Refer to Section 6.2.1.4.
<ul style="list-style-type: none"> • Clocks should be length matched from GMCH die pad to DIMM pin 	Refer to Section 6.2.1.4.
<ul style="list-style-type: none"> • 0.0" to 0.5" from GMCH ball to EMI capacitor stub 	Refer to Section 6.2.1.4.
<ul style="list-style-type: none"> • 0.0" to 0.25" from stub to component pad 	Refer to Section 6.2.1.4.
<ul style="list-style-type: none"> • 4.3" to 5.2" from cap stub to DIMM pin 	Refer to Section 6.2.1.4.
<ul style="list-style-type: none"> • 0.5" to 1.5" from DIMM to AC Termination 	Refer to Section 6.2.1.4.
<ul style="list-style-type: none"> • 5.7 ± 0.02" from GMCH die pad to DIMM pin 	Refer to Section 6.2.1.4.
Breakout guideline: 5 mils wide by 5 mil spacing, 0.5" max length	Refer to Section 6.2.1.4.

Feedback Signals: SRDCLK_OUT, SRDCLK_IN	
Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> • Point to Point Topology w/Resistor Jumper (Not populated) 	Refer to Section 6.2.1.5.
<ul style="list-style-type: none"> • 5 mils wide 	Refer to Section 6.2.1.5.
<ul style="list-style-type: none"> • 5 mil group spacing 	Refer to Section 6.2.1.5.
<ul style="list-style-type: none"> • 0 to 100 mils length from pad to resistor 	Refer to Section 6.2.1.5.
<ul style="list-style-type: none"> • 0 to 100 mils length from resistor to pad 	Refer to Section 6.2.1.5.



18.3.2 SDR-SDRAM Decoupling, Compensation, and VREF

Recommendation	Reason/Impact/Documentation
DIMM Decoupling <ul style="list-style-type: none"> • Place 9 evenly spaced 0.1 μF 0603 capacitors between the DIMMs • Place 6 100 μF bulk capacitors around the DIMMs 	Refer to Section 6.3.
VCCSM Decoupling <ul style="list-style-type: none"> • Place 6 evenly spaced 0.1μF 0603 capacitors • The via should be within 25 mils of the capacitor pad, and the trace from the via to the pad should be as thick as possible with a minimum width of 18 mils. • Place one 100 μF capacitor at the GMCH 	Refer to Section 6.4.
SMRCOMP <ul style="list-style-type: none"> • 10 mils wide minimum, 0.5" max length • 7 mil group spacing • Minimize the distance between SMRCOMP resistor and the GMCH 	Refer to Section 6.5.
SDREF <ul style="list-style-type: none"> • 12 mils wide, 3.0" max length • 10 mil group spacing • Place 0.1 μF decoupling capacitor at the GMCH • Minimize the distance between the voltage divider, decoupling capacitors and GMCH 	Refer to Section 6.6.

18.4 AGP

18.4.1 1X Signals

1X Signals: CLK(3.3 V), GRBF#, GWBF#, GST_[2:0], GPIPE, GREQ#, GGNT#, GPAR, GFRAME#, GIRDY#, GTRDY#, GSTOP#, GDEVSEL#	
1X Timing Domain Routing Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> • 6" max trace length 	Refer to Section 7.3.1.
<ul style="list-style-type: none"> • 5 mils wide with 7 mil trace separation. 	Refer to Section 7.3.1.
<ul style="list-style-type: none"> • GIRDY# and GDEVSEL# should be matched (± 250 mils) • GTRDY# with GFRAME# should be matched (± 250 mils) • GSTOP# with GAD_15 should be matched (± 250 mils) 	Refer to Section 7.3.1.

18.4.2 2X/4X Signals

2X/4X Signals: GAD_[15:0], GC/BE_[1:0]#, GAD_STB0, GAD_STB#1, GAD_[31:16], GC/BE_[3:2]#, GADSTB_1, GADSTB_1#1, GSBA_[7:0], GSBSTB, GSBSTB#1	
2X/4X Timing Domain Routing Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> • 6" max trace length 	Refer to Section 7.3.2.
<ul style="list-style-type: none"> • 1:3 trace width-to-spacing 	Refer to Section 7.3.2.
<ul style="list-style-type: none"> • Breakout Guidelines: 5 mil spacing, 0.3" max length 	Refer to Section 7.3.2.
<ul style="list-style-type: none"> • Strobes should match their complement to ± 50 mils 	Refer to Section 7.3.2.
<ul style="list-style-type: none"> • Data to Strobe length mismatch ± 0.125" from GMCH pad to AGP pin 	Refer to Section 7.3.2 and Table 63.
<ul style="list-style-type: none"> • GAD_STB0 should match GADSTB_1 to ± 0.125" 	Refer to Section 7.3.2.

18.4.3 AGP 1X and 2X/4X Common Routing

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Trace length mismatch for all signals within a signal group should be as close to zero as possible 	To provide timing margin Refer to Table 63
<ul style="list-style-type: none"> Separate the traces as much as possible 	Reduce trace-to-trace coupling Refer to Table 63
<ul style="list-style-type: none"> Data and associated strobe signals must not be routed on a separate layer for more than 3". 	Refer to Table 63
<ul style="list-style-type: none"> These guidelines apply to board stack-ups with 15% impedance tolerance. 	Refer to Table 63

18.4.4 AGP Clock Routing, Decoupling, VREF

Recommendation	Reason/Impact/Documentation
<p>Clock</p> <ul style="list-style-type: none"> Max 1 ns clock skew for all data transfer modes between the GMCH and the graphic component. 	Refer to Section 7.3.4.
<p>Decoupling</p> <ul style="list-style-type: none"> (5) 0.1 μF capacitors required Must be as close as possible to the GMCH, within 100 mils of the GMCH outer row of balls. AGP signal trace spacing may be reduced as the traces go around each cap. This space reduction should be minimal and for as short a distance as possible. Evenly distribute placement of decoupling caps in the AGP interface signal field. Use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric. Place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. 	Refer to Section 7.3.5 and 7.3.5.1.
<p>AGP Connector Decoupling</p> <ul style="list-style-type: none"> VCC3_3: (3) 0.01 μF or larger, low ESL caps. Place as close as possible to a VCC3_3 pair of pins on the connector Vddq: (6) 0.01 μF or larger, low ESL caps. Place as close as possible to a Vddq pair of pins on the connector +5 V: (1) 0.01 μF or larger, low ESL cap placed as close as possible to the +5 V connector pins +12 V: (1) 0.01 μF or larger, low ESL cap placed as close as possible to the +12 V connector pins 3.3VAUX: (1) 0.01 μF or larger, low ESL cap placed as close as possible to the 3.3VAUX connector pin(s) 	To address AC signaling issues. Refer to Section 7.3.5.1.

Recommendation	Reason/Impact/Documentation
AGP VREF <ul style="list-style-type: none"> Voltage divider with 1 kΩ 1% to produce 0.75 V – connected to both AGP_ref on GMCH and VrefCG on AGP connector. 0.1 μF Cap on net at both AGP connector and GMCH. 	Refer to Section 7.4.1.
AGP RCOMP <ul style="list-style-type: none"> 0.5" max length 40 Ω ± 1% down to ground 	Refer to Section 7.5.1.

18.5 Analog Display Port

18.5.1 Analog RGB/CRT

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> RED, GREEN, BLUE and RED#, GREEN#, BLUE# should be routed differentially 	Refer to Section 8.1.3.
<ul style="list-style-type: none"> 10 mil width with 5 mil spacing (Targeting 75 Ω odd mode differential impedance) 	Refer to Section 8.1.3.
<ul style="list-style-type: none"> 20 mil group spacing 	Refer to Section 8.1.3.
<ul style="list-style-type: none"> Each analog signal should be matched to its complement as closely as possible. 	Refer to Section 8.1.3.
<ul style="list-style-type: none"> RGB signals should be length matched as closely as possible from the GMCH to the VGA connector within ± 200 mils 	Refer to Section 8.1.3.
<ul style="list-style-type: none"> Terminate Rs (75 Ω for RED, GREEN, BLUE, 37.5 Ω for RED#, GREEN#, BLUE#) close to each other and the VGA connector. 	Refer to Section 8.1.3.



18.6 Hub Interface

18.6.1 Interface Signals

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> It is recommended that all signals be referenced to VSS 	Refer to Section 9.
<ul style="list-style-type: none"> The trace impedance must equal $60 \Omega \pm 15\%$. 	Refer to Section 9.1.
HI Strobe Signal: HI_STBS, HI_STBF	
<ul style="list-style-type: none"> Strobe signals need to be routed 5 mils wide with 15 mils spacing 	Refer to Section 9.1.1.
<ul style="list-style-type: none"> Strobe pair should have a minimum of 20 mils spacing from any adjacent signals. 	Refer to Section 9.1.1.
<ul style="list-style-type: none"> 2" to 8" max trace length 	Refer to Section 9.1.1.
<ul style="list-style-type: none"> Strobe length mismatch ± 100 mils max 	Refer to Section 9.1.1.
<ul style="list-style-type: none"> For breakout, strobe signals can be routed to 5 on 5 within 300 mils of the package 	Refer to Section 9.1.1.
HI Data Signals: HI[10:0]	
<ul style="list-style-type: none"> Data signals need to be routed 5 mils wide with 15 mils spacing 	Refer to DG Section 9.1.2.
<ul style="list-style-type: none"> Data signals must be matched within ± 100 mils of the HI_STBF/ HI_STBS differential pair 	Refer to DG Section 9.1.2.
<ul style="list-style-type: none"> For breakout, data signals can be routed to 5 on 5 within 300 mils of the package 	Refer to DG Section 9.1.2.
<ul style="list-style-type: none"> 2" to 8" max trace length 	Refer to DG Section 9.1.2.

18.6.2 Hub Interface Decoupling, Compensation, and VREF

Recommendation	Reason/Impact/Documentation
<p>HI_REF/HI_SWING generation circuit</p> <ul style="list-style-type: none"> • Should be placed no more than 4" away from GMCH or ICH4. • If more than 4" is needed, locally generated divider should be used. • Place (2) 0.1 μF caps close to the divider • Place the 0.01 μF bypass caps within 0.25" of the component's pin (HI_REF/VREF/HI_SWING). 	<p>Refer to Section 9.1.4.</p>
<p>HICOMP</p> <ul style="list-style-type: none"> • Trace must be as short as possible. 	<p>Refer to Section 9.1.5.</p>
<p>VCCHI1_5 Decoupling</p> <ul style="list-style-type: none"> • Decouple each component, the GMCH and the ICH4, with two 0.1 μF capacitors within 100 mils from each package. • Capacitors should be adjacent to hub interface rows 	<p>Refer to DG Section 9.1.6.</p>



18.7 Intel® ICH4

18.7.1 IDE Interface

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> 5 mil wide and 7 mil 	Refer to Section 10.1.
<ul style="list-style-type: none"> 8.0" max trace length from ICH4 to IDE connector 	Refer to Section 10.1.
<ul style="list-style-type: none"> The Maximum length difference between the data and strobe lengths is 0.5 inches. 	Refer to Section 10.1.

18.7.2 AC'97

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Trace impedance Z_0 AC97 = $60 \Omega \pm 15\%$ 	Refer to Section 10.2.
<ul style="list-style-type: none"> 5 mil trace wide, 5 mil spacing 	Refer to Section 10.2.
<ul style="list-style-type: none"> 14" max length from ICH4 to Codec/CNR connector 6" max length from primary codec and CNR 	Refer to Section 10.2.
AC_SDIN Max Trace Length ICH4 to: <ul style="list-style-type: none"> Primary Codec: L = 14 inches From Primary Codec T junction to CNR: L = 6 inches CNR: L = 14 inches. 	
AC_SDOOUT Max trace length ICH4 to: <ul style="list-style-type: none"> Primary Codec: L = 14 inches CNR: L = 14 inches. 	
AC_BIT_CLK Max trace length ICH4 to: <ul style="list-style-type: none"> Primary Codec: L = 13.6 inches CNR: L = 13.6 inches. 	
<ul style="list-style-type: none"> Series termination resistor on AC_BIT_CLK line should be no more than 0.9 to 7.6 inches from the ICH4 	
<ul style="list-style-type: none"> Series termination resistors on AC_SDIN lines if needed should be no more than 100 to 400 mils from the CNR card or the on board codec. 	

18.7.3 USB 2.0

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> 7.5 mils wide, 7.5 mil spacing 	Refer to Section 10.4.1.2.
<ul style="list-style-type: none"> 20 mil min spacing between USB signal pair and other traces 	This helps to minimize crosstalk. Refer to Section 10.4.1.2.
<ul style="list-style-type: none"> 150 mil max trace length mismatch between USB signal pair 	Refer to Section 10.4.1.5.
<ul style="list-style-type: none"> With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first 	Refer to Section 10.4.1.1.
<ul style="list-style-type: none"> Route USB signals ground referenced. 	Refer to Section 10.4.1.1.
<ul style="list-style-type: none"> Route USB signals using a minimum of vias and corners 	This reduces signal reflections and impedance changes. Refer to Section 10.4.1.1.
<ul style="list-style-type: none"> When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. 	This reduces reflections on the signal by minimizing impedance discontinuities Refer to Section 10.4.1.1.
<ul style="list-style-type: none"> Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or IC's that use and/or duplicate clocks. 	Refer to Section 10.4.1.1.
<ul style="list-style-type: none"> Stubs on USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs on a given data line should not be greater than 200 mils. 	Refer to Section 10.4.1.1.
<ul style="list-style-type: none"> Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.) 	Refer to Section 10.4.1.1.
<ul style="list-style-type: none"> Keep USB signals clear of the core logic set. 	High current transients are produced during internal state transitions, which can be very difficult to filter out. Refer to Section 10.4.1.1.
<ul style="list-style-type: none"> Keep traces at least 50 mils away from the edge of the plane (VCC or GND depending on which plane to which the trace is routed) 	Helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB. Refer to Section 10.4.1.1.
<ul style="list-style-type: none"> Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90Ω differential impedance. 	Refer to Section 10.4.1.2.
<ul style="list-style-type: none"> Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines. The minimum recommended spacing to clock signals is 20 mils 	Minimize crosstalk Refer to Section 10.4.1.2.



Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Use 20 mils minimum spacing between USB signal pairs and other signal traces. 	This helps to prevent crosstalk.
<ul style="list-style-type: none"> USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pair (such as DM1 and DP1) should be no greater than 150 mils. 	Refer to Section 10.4.1.5.
<ul style="list-style-type: none"> No termination resistors needed for USB. 	
<ul style="list-style-type: none"> USBRBIAS (ball A23) and USBRBIAS# (ball B23) should be routed 5 on 5 with a single trace 500 mils or less to the 22.6 Ω 1% resistor to ground. 	
<ul style="list-style-type: none"> 17" max trace length from ICH4 to the backpanel. 8" max trace length from ICH4 to CNR connector. Refer to Table 74 for front panel trace lengths. 	

18.7.4 PCI Guidelines

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Data Lines – See specific topology guidelines 	Refer to Table 78
<ul style="list-style-type: none"> Clock Lines 	Refer to Table 79
<ul style="list-style-type: none"> IDSEL 	See related figure in ICH4 PCI section

18.7.5 RTC

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> 5 mil trace width (results in ~2 pF per inch) 	
<ul style="list-style-type: none"> 1" max trace length to crystal 	
<ul style="list-style-type: none"> RTC LEAD length \leq 1.0 inches Max 	
<ul style="list-style-type: none"> Minimize capacitance between RTCX1 and RTCX2 	
<ul style="list-style-type: none"> Put GND plane underneath Crystal components 	
<ul style="list-style-type: none"> Do not route switching signals under the external components (unless on other side of board) 	
<ul style="list-style-type: none"> If SUSCLK is not used in the platform it should be routed to a test point. 	The ability to probe this signal can decrease the resolution time for RTC related issues

18.7.6 Platform LAN Connect Interface

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> • 5 mils wide, 10 mil spacing 	
LOM to PLC <ul style="list-style-type: none"> • 0.5" to 7.5" max trace length (A) from ICH4 to RPAK • 4" to (11.5 – A)" from RPAK to PLC LOM to CNR <ul style="list-style-type: none"> • 0.5" to 7.5" max trace length (A) from ICH4 to RPAK • 1.5" to (9 – A)" max trace length from ICH4 to CNR • (0.5" to 3" on card) 	To meet timing requirements. Refer to Section 10.9.2.1.2.
<ul style="list-style-type: none"> • Stubs due to R-pak CNR/LOM stuffing option should not be present. 	To minimize inductance.
Point-to- Point Single Solution Maximum Trace Lengths: <ul style="list-style-type: none"> • ICH4 to: 82562EZ/ET/EX/EM: L = 4.5 to 12 inches • CNR: L = 2 to 9.5 inches 	To meet timing requirements. Refer to Section 10.9.2.1.1.
<ul style="list-style-type: none"> • Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inches (clock must be longest trace) 	To meet timing and signal quality requirements. Refer to Section 10.9.2.2.
<ul style="list-style-type: none"> • Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN PHY. 	To meet timing and signal quality requirements. Refer to Section 10.10.1.1.
<ul style="list-style-type: none"> • Keep the total length of each differential pair under 4 inches. • (Preferably less than 2 inches) 	Issues found with traces longer than 4 inches: IEEE phy conformance failures, excessive EMI and or degraded receive BER. Refer to Section 10.10.1.1
<ul style="list-style-type: none"> • Do not route the transmit differential traces closer than 100 mils to the receive differential traces. 	To minimize crosstalk. Refer to Section 10.10.1.1
<ul style="list-style-type: none"> • Signal traces and differential traces not route in parallel and closer than 100 mil (300 mils recommended) 	To minimize crosstalk. Refer to Section 10.10.1.1
<ul style="list-style-type: none"> • Route 5 mils on 10 mils for differential pairs (out of LAN phy) 	To meet timing and signal quality requirements.
<ul style="list-style-type: none"> • Differential trace impedance should be controlled to be ~100 Ω . 	To meet timing and signal quality requirements. Refer to Section 10.10.1.1.1.
<ul style="list-style-type: none"> • For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, it is recommended to use two 45-degree bends. 	To meet timing and signal quality requirements. Refer to Section 10.10.1.1.



Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. 	<p>This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.</p> <p>Refer to Section 10.10.1.1.</p>
<ul style="list-style-type: none"> Do not route traces and vias under crystals or oscillators. 	<p>This will prevent coupling to or from the clock.</p> <p>Refer to Section 10.10.1.1.</p>
<ul style="list-style-type: none"> Trace width to height ratio above the ground plane ratio is between 1:1 and 3:1. 	<p>To control trace EMI radiation.</p> <p>Refer to Section 10.10.1.1.1.</p>
<ul style="list-style-type: none"> Traces between decoupling and I/O filter capacitors should be as short and wide as practical. 	<p>Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.</p> <p>Refer to Section 10.10.1.1.1.</p>
<ul style="list-style-type: none"> Vias to decoupling capacitors should be sufficiently large in diameter. 	<p>To decrease series inductance.</p> <p>Refer to Section 10.10.1.1.1.</p>
<ul style="list-style-type: none"> Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices. 	<p>To minimize crosstalk.</p> <p>Refer to Section 10.10.1.1.2.</p>
<ul style="list-style-type: none"> Isolate I/O signals from high-speed signals. 	<p>To minimize crosstalk.</p> <p>Refer to Section 10.10.1.1.2.</p>
<ul style="list-style-type: none"> Place the 82562EZ/ET/EX/EM part more than 1.5 inches away from any board edge. 	<p>This minimizes the potential for EMI radiation problems.</p>
<ul style="list-style-type: none"> Place at least one bulk capacitor (4.7 μF or greater OK) on each side of the 82562EZ/ET/EX/EM. 	<p>Research and development has shown that this is a robust design recommendation.</p>
<ul style="list-style-type: none"> Place decoupling caps (0.1 μF) as close to 82562EZ/ET/EX/EM as possible. 	
<ul style="list-style-type: none"> Design and Layout Guidelines for the 82540EM and 1000BASE-T Designs 	<p>Refer to DG Section 10.10.2</p>

18.8 FWH Decoupling

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> 0.1 μF capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins. 	
<ul style="list-style-type: none"> 4.7 μF capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins. 	

18.9 Platform Clocks

18.9.1 Host Clock (CPU#, CPU)

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Ground referenced 	Refer to Section 13.2.1.
<ul style="list-style-type: none"> 7 mils wide with 8 mil differential pair spacing 	Refer to Section 13.2.1.
<ul style="list-style-type: none"> Spacing to other traces should be 3 to 4 times greater than distance from BCLK1 to BCKL0 	Refer to Section 13.2.1.
<ul style="list-style-type: none"> Processor routing length- Clock driver to Rs should be 0.5" max 	Minimize the impact on skew and impedance variation Refer to Section 13.2.1.
<ul style="list-style-type: none"> Processor routing length- Rs to Rs-Rt should be 0" to 0.2" 	Minimize the impact on skew and impedance variation Refer to Section 13.2.1.
<ul style="list-style-type: none"> Processor routing length- Rs-Rt node to Rt should be 0" to 0.2" 	Minimize the impact on skew and impedance variation Refer to Section 13.2.1.
<ul style="list-style-type: none"> Processor routing length- Rs-Rt node to load should be 2" to 12" 	Refer to Section 13.2.1.
<ul style="list-style-type: none"> GMCH routing length- Clock driver to Rs should be 0.5" max 	Minimize the impact on skew and impedance variation Refer to Section 13.2.1.
<ul style="list-style-type: none"> GMCH routing length- Rs to Rs-Rt should be 0" to 0.2" 	Minimize the impact on skew and impedance variation Refer to Section 13.2.1.
<ul style="list-style-type: none"> GMCH routing length- Rs-Rt node to Rt should be 0" to 0.2" max 	Minimize the impact on skew and impedance variation Refer to Section 13.2.1.
<ul style="list-style-type: none"> GMCH routing length- Rs-Rt node to load should be 2.0" to 12" max 	Refer to Section 13.2.1.
<ul style="list-style-type: none"> Clock pair to GMCH must be 100 mils longer than clock pair to CPU socket 	Rs values between 20 – 33 Ω have been shown to be effective Refer to Section 13.2.1.
<ul style="list-style-type: none"> \pm10 mil length matching between BCLK0 to BCLK1 	Refer to Section 13.2.1.



Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Host clock pairs must be routed differentially and on the same physical routing layer. 	Refer to Section 13.2.1.
<ul style="list-style-type: none"> Route all agents on the same physical routing layer referenced to ground of the differential clock 	Refer to Section 13.2.1.
<ul style="list-style-type: none"> Make sure that the skew induced by the vias is compensated in the traces to other agents 	Refer to Section 13.2.1.
<ul style="list-style-type: none"> Do not place vias between adjacent complementary clock traces 	Refer to Section 13.2.1.
<ul style="list-style-type: none"> Maintain uniform spacing between the two halves of differential clocks 	EMI Constraints. Refer to Section 13.2.1.
<ul style="list-style-type: none"> Route clocks on physical layers adjacent to the VSS reference plane only 	EMI Constraints. Refer to Section 13.2.1.

18.9.2 DOT_CLK Clock Group

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Point to Point Topology 	Refer to Section 13.2.2.
<ul style="list-style-type: none"> 5 mils wide with 20 mil spacing 	Refer to Section 13.2.2.
<ul style="list-style-type: none"> 0.0" to 0.5" max from driver to series termination 	Refer to Section 13.2.2.
<ul style="list-style-type: none"> 2" to 9" max from series termination to GMCH 	Refer to Section 13.2.2.

18.9.3 66 MHz Clock Group

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Point to Point Topology 	Refer to Section 13.2.3.
<ul style="list-style-type: none"> 5 mils wide and 20 mil spacing 	Refer to Section 13.2.3.
<ul style="list-style-type: none"> 20 mil group spacing 	Refer to Section 13.2.3.
<ul style="list-style-type: none"> 0.0" to 0.5" max trace length from clock driver to series termination 	Refer to Section 13.2.3.
<ul style="list-style-type: none"> 4.0" and 8.5" max trace length from series termination to receiver on the motherboard 	Refer to Section 13.2.3.
<ul style="list-style-type: none"> X Trace length from the clock driver to the GMCH 	Refer to Section 13.2.3.
<ul style="list-style-type: none"> $X \pm 100$ mils max trace length from the clock driver to ICH4 	<p>If the trace length from the clock driver to the GMCH is X, the trace length from the clock drive to the ICH4 must be $X \pm 100$.</p> <p>Refer to Section 13.2.3.</p>
<ul style="list-style-type: none"> Minimal (~0) skew between CLK33 group and CLK66 group 	Refer to Sections 13.2.3 and 13.2.5.

18.9.4 AGPCLK (When Routing to an AGP Connector)

Recommendation	Reason/Impact/Documentation
AGPCLK to AGP Connector	
<ul style="list-style-type: none"> Point to Point Topology 	Refer to Section 13.2.4.
<ul style="list-style-type: none"> 5 mils wide and 15 mil spacing 	Refer to Section 13.2.4.
<ul style="list-style-type: none"> 15 mil group spacing 	Refer to Section 13.2.4.
<ul style="list-style-type: none"> Series termination within 0.5" of the driver 	Refer to Section 13.2.4.
<ul style="list-style-type: none"> The total trace length must be 4.0" less than the CLK66 total trace length ± 100mils. 	Refer to Section 13.2.4.
AGPCLK to AGP Down	
<ul style="list-style-type: none"> Point to Point Topology 	Refer to Section 13.2.4.
<ul style="list-style-type: none"> 5 mils wide and 15 mil spacing 	Refer to Section 13.2.4.
<ul style="list-style-type: none"> 15 mil group spacing 	Refer to Section 13.2.4.
<ul style="list-style-type: none"> Series termination within 0.5" of the driver 	Refer to Section 13.2.4.
<ul style="list-style-type: none"> The total trace length must be the CLK66 total trace lengths ± 100mils. 	Refer to Section 13.2.4.



18.9.5 33 MHZ Clock Group

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Point to Point Topology 	Refer to Section 13.2.5.
<ul style="list-style-type: none"> 5 mils wide and 15 mil spacing 	Refer to Section 13.2.5.
<ul style="list-style-type: none"> 15 mil group spacing 	Refer to Section 13.2.5.
<ul style="list-style-type: none"> Series termination within 0.5" of the driver 	Refer to Section 13.2.5.
<ul style="list-style-type: none"> 4.0" and 8.5" max trace length from series termination to receiver on the motherboard 	Refer to Section 13.2.5.
<ul style="list-style-type: none"> The 33 MHz clock to the receiver must be matched to ± 100 mils of the CLK66 	Refer to Section 13.2.5 and 13.2.3.
<ul style="list-style-type: none"> Clocks in 33 MHz and 66 MHz clock group should have minimal (~0) skew. 	Refer to Section 13.2.5 and 13.2.3.

18.9.6 14 MHz Clock Group

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Balanced Topology 	Refer to Section 13.2.6.
<ul style="list-style-type: none"> 5 mils wide and 10 mils spacing 	Refer to Section 13.2.6.
<ul style="list-style-type: none"> 10 mils group spacing 	Refer to Section 13.2.6.
<ul style="list-style-type: none"> Series termination within 0.5" of the driver 	Refer to Section 13.2.6.
<ul style="list-style-type: none"> Signal must T within 12" of the series termination 	Refer to Section 13.2.6.
<ul style="list-style-type: none"> Max trace length of stubs is 6" 	Refer to Section 13.2.6.
<ul style="list-style-type: none"> Total trace length matched to ± 0.5" of each other 	Refer to Section 13.2.6.



18.9.7 PCICLK Clock Group

Recommendation	Reason/Impact/Documentation
PCICLK to PCI Device Down	
• Point to Point Topology	Refer to Section 13.2.7.
• 5 mils wide and 15 mils spacing	Refer to Section 13.2.7.
• 15 mils group spacing	Refer to Section 13.2.7.
• Series termination within 0.5" of the driver	Refer to Section 13.2.7.
• Total trace length matched to $CLK33 \pm 500$ mils	Refer to Section 13.2.7.
PCICLK to Devices on PCI Cards	
• Point to Point Topology	Refer to Section 13.2.7.
• 5 mils wide and 15 mils spacing	Refer to Section 13.2.7.
• 15 mils group spacing	Refer to Section 13.2.7.
• Series termination within 0.5" of the driver	Refer to Section 13.2.7.
• Length from series resistor to PCI Slot is not specified: It is dependent on total motherboard trace length.	Refer to Section 13.2.7.
• 2.5" from PCI Slot to PCI device.	Refer to Section 13.2.7.
• Total trace length from driver to PCI Connector matched to $(CLK33 - 2.5") \pm 500$ mils	Refer to Section 13.2.7.

18.9.8 USBCLK

Recommendation	Reason/Impact/Documentation
• Point to Point Topology	Refer to Section 13.2.8.
• 5 mils wide	Refer to Section 13.2.8.
• 20 mils group spacing	Refer to Section 13.2.8.
• Series termination within 0.5" of the driver	Refer to Section 13.2.8.
• Trace length from series termination to receiver on the motherboard between 3.0" and 12"	Refer to Section 13.2.8.



18.9.9 Clock Decoupling: VddA/Vdd Decoupling

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Place (1) 10 μF bulk decoupling cap in a 1206 package close to the Vdd generation circuitry 	Refer to Section 13.3.
<ul style="list-style-type: none"> Place (6) 0.1 μF caps in a 0603 package close to the Vdd pins on the clock driver 	Refer to Section 13.3.
<ul style="list-style-type: none"> Place (3) 0.01μF high frequency decoupling caps in 0603 package close to the VddA pins on the clock driver 	Refer to Section 13.3.
<ul style="list-style-type: none"> Place (1) 10 μF bulk decoupling cap in 1206 package close to the VddA generation circuitry 	Refer to Section 13.3.

18.10 Platform Power

18.10.1 Intel® GMCH High-Frequency Decoupling

Recommendation	Reason/Impact/Documentation
<p>VTT_DECAP</p> <ul style="list-style-type: none"> (5) 0.1 μF Caps (Edge Cap - VTT) Edge Caps must not have vias in the trace from the cap to the GMCH solder ball. They also must not connect to the motherboard VTT plane. Place near balls: AC37, R37, L37, G37, and A31 Unless otherwise noted, capacitors should be placed less than 100 mils from the package. 	Refer to Section 14.2.4
<p>VTTFSB</p> <ul style="list-style-type: none"> (5) 0.1 μF Caps (Decoupling Cap - VTT) Place within 250 mils of the package within the VTT corridor Unless otherwise noted, capacitors should be placed less than 100 mils from the package. 	Refer to 14.2.4
<p>VCC</p> <ul style="list-style-type: none"> (1) 0.1 μF Caps (Decoupling Cap - VCC) Place within 100 mils of the package in or near the VCC corridor Unless otherwise noted, capacitors should be placed less than 100 mils from the package. 	Refer to Section 14.2.4.
<p>VCCAGP</p> <ul style="list-style-type: none"> (5) 0.1 μF Caps (Decoupling Cap - VSS) Place near balls: A5, E1, J1, N1, and U1 Unless otherwise noted, capacitors should be placed less than 100 mils from the package. 	Refer to Section 14.2.4

Recommendation	Reason/Impact/Documentation
VCCHI <ul style="list-style-type: none"> • (2) 0.1 μF Caps (Decoupling Cap - VSS) • Place near balls: AA1 and AE1 • Unless otherwise noted, capacitors should be placed less than 100 mils from the package. 	Refer to Section 14.2.4.
VCCSM <ul style="list-style-type: none"> • (8) 0.1 μF Caps (Decoupling Cap - VCC) • Place near balls: AL37, AU5, AU9, AU13, AU17, AU25, AU29, and AU33 • Unless otherwise noted, capacitors should be placed less than 100 mils from the package. 	Refer to Section 14.2.4
VCCA_DAC <ul style="list-style-type: none"> • (1) 0.1 μF Caps; (1) 0.01 μF Caps (Decoupling Cap - VCC) • Place near balls: B14 and A15 	Refer to 14.2.4.
<ul style="list-style-type: none"> • Unless otherwise noted, caps should be placed less than 100 mils from the package. 	Refer to Section 14.2.4
<ul style="list-style-type: none"> • Edge caps must not have vias in the trace from the cap to the GMCH solder ball 	Refer to Section 14.2.4.

18.10.2 Intel® GMCH Bulk Decoupling

Recommendation	Reason/Impact/Documentation
VTTFSB <ul style="list-style-type: none"> • (2) 10 μF caps • Place in VTT power corridor as shown in the above finger 	Refer to Section 14.2.4
VCC/VCCAGP/VCCHI <ul style="list-style-type: none"> • (2) 100 μF caps • (1) 220 μF caps • Place between the AGP connector and the GMCH. The 220 μF and one 100 μF cap must be placed in the VCC_CORE plane. 	Refer to Section 14.2.4.
VCCSM <ul style="list-style-type: none"> • (4) 100 μF caps • Placed between the GMCH and DIMMs (One of the capacitors must be placed in the layer one shape)	Refer to Section 14.2.4.
<ul style="list-style-type: none"> • Unless otherwise noted, caps should be placed less than 100 mils from the package. 	Refer to Section 14.2.4.
<ul style="list-style-type: none"> • Edge caps must not have vias in the trace from the cap to the GMCH solder ball 	Refer to Section 14.2.4.



18.10.3 Intel® ICH4 Decoupling

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> Place caps within 100 mils from the package 	Refer to Section 14.3.4.
VCC3_3 <ul style="list-style-type: none"> (6) 0.1 μF caps - Decoupling Cap (VSS) Place cap near A4, A1, H1, T1, AC10, and AC18 	Refer to Section 14.3.4.
VccSus3_3 <ul style="list-style-type: none"> (2) 0.1 μF caps - Decoupling Cap (VSS) Place cap near balls: A22 and AC5 	Refer to Section 14.3.4.
V_CPU_IO <ul style="list-style-type: none"> (1) 0.1 μF cap - Decoupling Cap (VCC) Place cap near ball: AA23 	Refer to Section 14.3.4.
VCC1_5 <ul style="list-style-type: none"> (2) 0.1 μF caps - Decoupling Cap (VSS) Place cap near balls: K23 and C23 	Refer to Section 14.3.4.
VccSus1_5 <ul style="list-style-type: none"> (2) 0.1 μF caps - Decoupling Cap (VSS) Place cap near balls: A16 and AC1 	Refer to Section 14.3.4.
V5REF <ul style="list-style-type: none"> (1) 0.1 μF cap - Decoupling Cap (VCC) Place cap near ball: E7 V5REF is the reference voltage for 5 V tolerant inputs in the ICH4. Tie to pins V5REF[2:1]. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3 	Refer to Section 14.3.4.
V5_REF_SUS <ul style="list-style-type: none"> (1) 0.1 μF cap - Decoupling Cap (VSS) Place cap near ball: A16 V5_REF_Sus only affects 5 V tolerance for USB OC[5:0]# pins and can be connected to VccSus3_3 if 5 V tolerance on these signals are not required. 	Refer to Section 14.3.4.
VCCRTC <ul style="list-style-type: none"> (1) 0.1 μF cap - Decoupling Cap (VCC) Place cap near ball: AB5 	Refer to Section 14.3.4.



Recommendation	Reason/Impact/Documentation
VCCHI <ul style="list-style-type: none">• (2) 0.1 μF cap – Decoupling Cap (VSS)• Place cap near balls: T23 and N23	Refer to Section 14.3.4.
VCCPLL <ul style="list-style-type: none">• (1) 0.1 μF and (1) 0.01 μF cap – Decoupling Cap (VCC)• Place cap near balls: C22	Refer to Section 14.3.4.

18.11 Platform Mechanical

18.11.1 Processor Keep-Out

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none">• Verify during system board layout that Intel's Boxed Processor mechanical keep-outs are marked and visible, and that they are considered during chassis selection.	



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19 Intel® 845GL/845GV Chipsets

The 845GL and 845GV chipsets are very similar to the 845G chipset, and most of the information in the preceding chapters (Chapter 1 through 18) apply to the 845GL and 845GV chipsets. This chapter provides 845GL/845GV chipset information that differs from the preceding 845G chipset information, and that applies only to 845GL/845GV designs.

The information in this chapter applies to both the 845GL chipset and 845GV chipset, unless otherwise noted. Also, unless otherwise noted in this chapter, the term GMCH applies to both the 845GL chipset and 845GV chipset.

Note: The only difference between the 845GL and 845GV chipsets is the supported Processor System Bus (PSB) frequencies. The 845GL chipset supports 400 MHz. The 845GV chipset supports both 400 MHz and 533 MHz.

19.1 Intel® 845GL/845GV Chipset System Overview

19.1.1 Intel® Graphics Memory Controller Hub (GMCH)

The GMCH is in a 760 ball FCBGA package and has the following functionality:

- Supports 2 DIMMS of either SDR-SDRAM (PC133) or DDR-SDRAM (DDR200/266)
- AGTL+ host bus with integrated termination supporting 32-bit host addressing
- Dedicated DVO ports
- 8-bit, 66 MHz 4x Hub Interface to the ICH4
- IGD with analog and digital display ports

19.1.2 Processor System Bus

Information in this section replaces information in Section 1.3.2.2 when designing with the 845GL/845GV chipsets.

- Supports single processor
- Processor packaging: mPGA 478 package
- Supports 400 MHz PSB. The 845GV chipset also supports 533 MHz PSB.
- System Bus interrupt delivery
- Supports 32-bit addressing for access to 4 GB memory
- Supports AGTL+ on-die termination



19.1.3 Accelerated Graphics Port (AGP) Interface

Section 1.3.2, Intel® Graphics Memory Controller Hub (GMCH), **does not apply** to the 845GL/845GV chipsets.

19.1.4 Bandwidth Summary

Information in this section replaces information in *Section 1.3.4* when designing with the 845GL/845GV chipset. Table 114 describes the bandwidth of critical 845GL/845GV chipset platform interfaces.

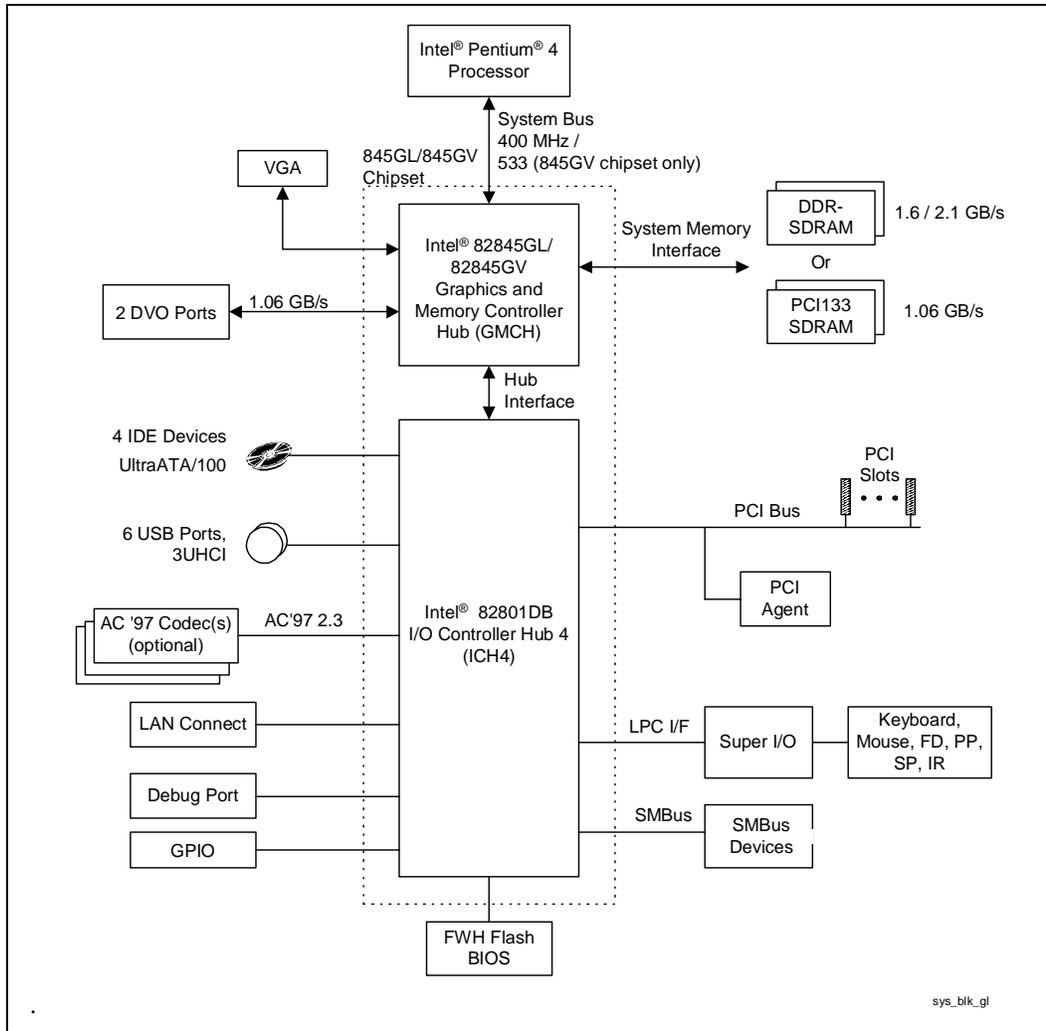
Table 114 Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth
System Bus	100 133 (845GV chipset only)	4	8	3.2 GB/s 4.2 GB/s (845GV chipset only)
DVO	Up to 165	2	1.5\3	165 Mpixel/s / 330 Mpixel/s
DAC	Up to 350	N/A	N/A	Up to 350 Mpixel/s
Hub Interface	66	4	1	266 MB/s
PCI 2.2	33	1	4	133 MB/s
DDR-SDRAM	100/133	2	8	1.6 GB/s / 2.1 GB/s
SDR-SDRAM	133	1	8	1.06 GB/s

19.1.5 Intel® 845GL/845GV Chipset System Configuration

Information in this section replaces information in *Section 1.3.5* when designing with the 845GL/845GV chipset. Figure 203 shows a typical Intel® Pentium® Processor in the 478 pin package and 845GL/845GV chipset based system configuration.

Figure 203. Typical System Configuration





19.2 Processor System Bus (PSB) Guidelines

19.2.1 PSB Guidelines for the Intel® 845GL Chipset

Information in this section replaces information in Chapter 4 when designing with the 845GL chipset. This section addresses layout recommendations for an Intel® Pentium® 4 Processor in the 478-pin package with a 400 MHz PSB configuration for the 845GL chipset platform.

Note: The Processor System Bus guidelines for the 845GL chipset are the same as for the 845G chipset unless otherwise noted; therefore, all references to 845G chipset for this section apply to 845GL, unless otherwise noted.

19.2.2 PSB Guidelines for the Intel® 845GV Chipset

When designing an 845GV chipset-based system, follow the 845G chipset guidelines described in Chapter 4.

19.2.3 Topology 9 — PSB Frequency Select (Intel® 845GL chipset only)

Table 115 replaces Table 14 when designing with the 845GL chipset.

Table 115. Frequency Select Settings

SEL [2:0]	CK-408 Speed	BSEL0	Processor	Notes
001	100 MHz	L	400 MHz	
011	133 MHz	Hi-Z	533 MHz	1, 2

NOTES:

1. A PSB clock speed of 133 MHz is not supported on the 845GL chipset platform
2. A 533 MHz capable CPU is not supported on the 845GL chipset platform

19.3 DDR System Memory Design Guidelines

The following note is added immediately before Section 5.1 when designing with the 845GL/845GV chipset.

Note: The DDR System Memory Design Guidelines for the 845GL/845GV apply to the 845G unless otherwise noted; therefore, all references to the 845G in the Design Guide for this section apply to 845GL/845GV, unless otherwise noted.

19.4 Intel® 845GL/845GV Chipset DVO Design Guidelines

The information in this section replaces information in *Chapter 7* when designing with the 845GL/845GV chipset.

Note: This section of the design guide focuses only on specific 845GL/845GV chipset platform recommendations. The design guidelines specified in *Chapter 7* of the Design Guide for 845G AGP/Multiplexed DVO designs do not apply to the 845GL/845GV chipset platform, and are not supported on the 845GL/845GV chipset platform.

19.4.1 DVO Interface Overview

The GMCH supports two DVO ports. These DVO ports (DVOB and DVOC) are 1.5 V interfaces that can each support transactions up to 165MHz. The DVO ports are capable of interfacing with a wide variety of DVO port compliant devices (e.g., discrete TV encoder, discrete TMDS transmitter, combination TV encoder and TMDS transmitter or LVDS transmitters). It is possible to use the DVO ports in dual-channel mode to support higher resolutions and refresh rates (single channel mode is limited to a 165MHz pixel clock rate).

Note: Even if the DVO ports are not utilized, certain DVO related signals must still be connected properly for GMCH to function properly. Refer to Section 19.4.5 for details.

19.4.2 DVO Interface Routing Guidelines

Route data signals (DVOxData[11:0]) with a trace width of 5 mils and a trace spacing of 15 mils. To break out of the GMCH, the DVO data signals can be routed with a trace width of 5 and a trace spacing of 5. The signals should be separated to a trace width of 5 and a trace spacing of 15 within 0.3" of the GMCH component. The maximum trace length for the DVO data signals is 7.5 ". These signals should each be matched within ± 0.125 " of their associated Clk(#) signals.

Route the DVOx_Clk(#) signals 5 mils wide and 15 mils apart. This signal pair should be a minimum of 20 mils from any adjacent signals. The maximum length for DVOx_Clk(#) is 7.5 ", and the two signals should be the same length.

DVOx_CLK is the primary clock of the differential pair. Care should be taken to ensure that DVOx_CLK is connected to the primary clock receiver on the DVO device. If the DVO device supports differential clocking mode (highly recommended), then DVOx_CLK# should be connected to the complementary clock receiver of the DVO device.



19.4.2.1 DVO Down

When the DVO ports are implemented, the DVO devices are soldered down on the motherboard. A 330 Ω pull-down to GND is required on ADD_DETECT# as well as ADD_ID7.

The GMCH controls the video front-end devices via the I²C interfaces. The MI2C_DATA and MI2C_CLK pins should be used to communicate with I²C compliant DVO devices. I²C is a two-wire communications bus/protocol. The protocol and bus are used to configure registers in the DVO device. GMCH also utilizes the MDVI_CLK and MDVI_DATA to collect EDID (Extended Display Identification) from a digital display panel. GMCH also has a third set of control signals, MDDC_CLK and MDDC_DATA that can be used for various purposes if multiple DVO devices are utilized.

Do not interchange or modify the functionality of MI2C and MDVI signals. Pull-up resistors of 4.7 k Ω pulled to 1.5 V (or pull-ups with the appropriate value derived from simulation) are required on each of these signals. These signals are 1.5 V tolerant. If higher signaling voltages are needed (3.3 V for MI2C and 5 V for MDVI), then level-shifting devices will be required on the motherboard.

19.4.2.2 DVO Interface Signal Groups

All signals must meet minimum and maximum trace length requirements as well as trace width and spacing requirements. The signal groups are listed in Table 116.

Table 116. DVO Signal Groups

DVO timing domain	Miscellaneous
Set #1	ADDID[7:0]
DVOB_D[11:0]	ADD_Detect#
DVOB_HSYNC	
DVOB_VSYNC	
DVOB_CLK	DVOBC_CLKINT#
DVOB_CLK#	DVOBC_INTR#
DVOB_BLANK#	
DVOB_FLDSTL	
	MDVI_CLK
Set #2	MDVI_DATA
DVOC_D[11:0]	MDVI_CLK
DVOC_HSYNC	MDDC_DATA
DVOC_VSYNC	MI2C_CLK
DVOC_CLK	MI2C_DATA
DVOC_CLK#	
DVOC_BLANK#	
DVOC_FLDSTL	

Throughout this section, the term data refers to DVOB_D[11:0], DVOC_D[11:0], DVOB_HYSNC, DVOB_VSYNC, DVOC_HYSNC, DVOC_VSYNC, DVOB_BLANK, DVOC_BLANK, DVOB_FLDSTL, and DVOC_FLDSTL. The term clock refers to DVOB_CLK, DVOB_CLK#, DVOC_CLK, and DVOC_CLK#. When the term data is used, it refers to one of the two sets of data signals, as in Table 116. When the term clock is used, it refers to one of the clocks as it relates to the data in its associated group.

19.4.3 DVO Routing Guidelines

19.4.3.1 DVO Timing Domain Routing Guidelines

These trace length guidelines apply to ALL signals listed in Table 116 as DVO timing domain signals. These signals should be routed using 5-mil (60 Ω) traces.

For motherboards that use DVO down, the maximum length of DVO timing domain signals is 7.5".

- 1:3 trace width-to-spacing is required for DVO signal traces.
- DVO signals must be matched with their associated clock from GMCH pad to DVO device within ± 0.125 ". Refer to Table 117 for GMCH DVO nominalized package lengths.
- Clocks should match their complement to ± 50 mils.
- If running in dual channel mode, DVOB_CLK should match DVOC_CLK to ± 0.125 ".

For example, if DVOB_CLK is 2.6" long, DVOB_CLK# should also be 2.6". The data signals associated with those clock signals (e.g., DVOB_D[11:0], DVOB_HYSNC, DVOB_VSYNC, DVOB_BLANK#, and DVOB_FLDSTL) must be no more than 0.125" different in length from either of their associated clocks. This means that if DVOB_CLK is 2.6" long and DVOB_CLK# is 2.65" long, then DVOB_D[11:0] must be between 2.525" and 2.725" long. If using dual channel mode, then the DVOC_CLK pair should also be matched to 2.6" ± 0.125 ", their associated data signals then matched to ± 0.125 " of the DVOC_CLK pair.

The signals (DVOB_CLK, DVOB_CLK#, DVOC_CLK, DVOC_CLK#) are clocks; therefore, special care must be taken when routing these signals. Because DVO uses a differential clocking scheme, the pair should be routed together and on the same layer (e.g., DVOB_CLK and DVOB_CLK# should be routed next to each other). The two clocks in a clock pair should be routed using 5-mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the DVO signals – and all other signals – by at least 20 mils (1:4). The clock pair must be length-matched to less than ± 50 mils.



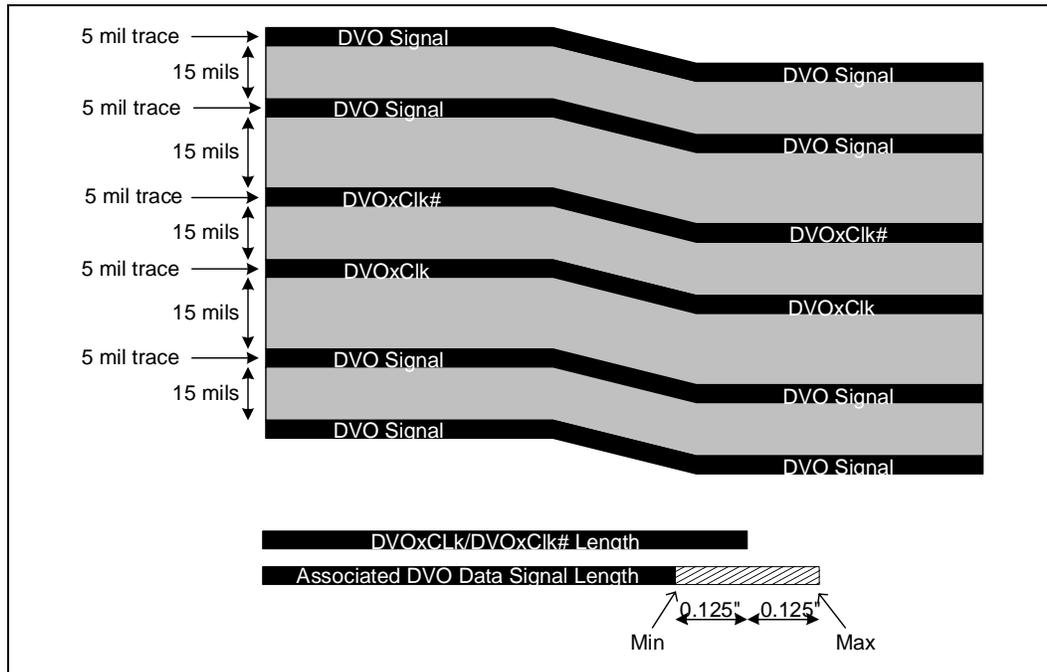
19.4.3.2 Miscellaneous Timing Domain Routing Guidelines

- The DVO Miscellaneous Timing domain signals (refer to Table 116) have a maximum trace length of 7.5". This maximum applies to ALL signals listed as Miscellaneous timing domain signals in that table.
- DVO Miscellaneous timing domain signals can be routed with 5 on 7 trace separation.
- MI2C_CLK and MI2C_DATA should be matched (± 250 mils), as should MDVI_CLK with MDVI_DATA and MDVI_DATA with MDVI_CLK.

Table 117. DVO Intel® GMCH Nominalized Package Lengths

Data Signal	Intel® GMCH Ball	Package Length (Inches)	Data Signal	Intel® GMCH Ball	Package Length (Inches)
DVOB_CLK	V8	0.384	DVOC_CLK	M8	0.443
DVOB_CLK#	U7	0.395	DVOC_CLK#	L7	0.458
DVOB_FLDSTL	T8	0.367	DVOC_FLDSTL	G4	0.628
DVOBC_CLKINT#	R7	0.410	DVOBC_INTR#	K8	0.437
DVOB_D10	R5	0.493	DVOC_D10	H3	0.679
DVOB_D11	R2	0.638	DVOC_D11	J7	0.505
DVOB_D8	T4	0.524	DVOC_D8	J5	0.580
DVOB_D9	T3	0.586	DVOC_D9	J4	0.616
DVOB_D6	T2	0.635	DVOC_D6	K3	0.640
DVOB_D4	V3	0.574	DVOC_D7	G2	0.742
DVOB_D5	U2	0.602	DVOC_D4	H4	0.623
DVOB_D2	U4	0.514	DVOC_D3	L4	0.605
DVOB_D3	U5	0.494	DVOC_D2	L5	0.549
DVOB_D0	W5	0.461	DVOC_D1	M3	0.641
DVOB_D1	W4	0.529	DVOC_D0	J2	0.676
DVOB_VSYNC	V2	0.607	DVOC_BLANK#	K2	0.663
DVOB_HSYNC	V4	0.492	DVOC_HSYNC	K4	0.575
DVOB_D7	R4	0.557	DVOC_VSYNC	P8	0.364
DVOB_BLANK#	N4	0.581	DVOC_D5	H2	0.754

Figure 204 DVO Routing Example



19.4.3.3 DVO Routing Guideline Considerations and Summary

- The DVO timing domain signals can be routed with 5-mil spacing when breaking out of the GMCH. It is recommended that the routing widen to the documented requirements < 0.3” from the GMCH package.
- Reduce line length mismatch to ensure added margin. Trace length mismatch for all signals within a signal group should be as close to zero as possible, to provide timing margin.
- To reduce trace-to-trace coupling (cross-talk), separate the traces as much as possible.
- Ideally, all signals in a signal group should be routed on the same layer. Data and associated clock signals must not be routed on a separate layer for more than 3”.
- The trace length and trace spacing requirements must not be violated by any signal.

Table 118. DVO Routing Summary

Signal	Max. Length	Trace Spacing (5-mil Traces)	Length Mismatch	Relative to	Notes
DVO Timing Domain Set 1 – DVOB	7.5 “	15 mils ¹	±0.125”	DVOB_CLK and DVOB_CLK#	DVOB_CLK, DVOB_CLK# must be the same length (± 50 mils); if dual channel mode, match DVOB_CLK to DVOC_CLK within 0.125”
DVO Timing Domain Set 2 – DVOC	7.5 “	15 mils ¹	±0.125”	DVOC_CLK and DVOC_CLK #	DVOC_CLK, DVOC_CLK # must be the same length (± 50 mils); if dual channel mode, match DVOC_CLK to DVOC_CLK within 0.125”
Misc Timing Domain	7.5 “	15 mils ¹			Control pair (I2CClk and I ² C data) should match its partner as closely as possible.

NOTE: ¹These guidelines apply to board stack-ups with 15% impedance tolerance.

19.4.3.4 DVO Signal Noise Decoupling Guidelines

The following routing guidelines are recommended for the optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the DVO interface of the 845GL/845GV chipset GMCH. The following guidelines are not intended to replace thorough system validation on 845GL/845GV chipset-based products.

- Five 0.1 µF capacitors are required and must be as close as possible to the GMCH. These should be placed within 100 mils of the outer row of balls on the GMCH for VDDQ decoupling. The closer the placement, the better.
- The designer should evenly distribute placement of decoupling capacitors in the DVO interface signal field.
- It is recommended that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.
- To add the decoupling capacitors within 100 mils of the GMCH and/or close to the vias, the trace spacing for DVO signals may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible.
- In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the DVO signal from one reference signal plane to another. On a typical four layer PCB design, the signals transition from one side of the board to the other. One 0.01 µF capacitor is required per 5 vias. The capacitor should be placed as close as possible to the center of the via field.

19.4.3.4.1 DVO Device Decoupling

Consult with the DVO device vendor for appropriate DVO device decoupling and power delivery.

19.4.3.5 DVO Routing Plane Reference

It is strongly recommended that each DVO timing group be continuously plane referenced from the GMCH to the DVO device using a minimum number of vias on each net.

In an ideal design, the complete DVO interface signal field would be referenced to ground. This recommendation is not specific to any particular PCB stack-up, but should be applied to all 845GL/845GV chipset designs.

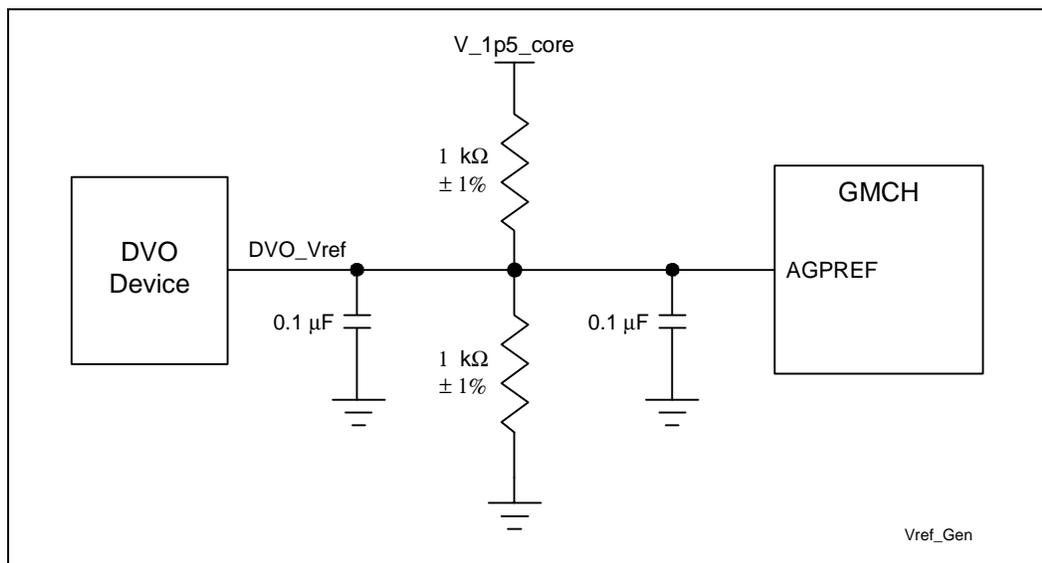
19.4.4 DVO Power Delivery Guidelines

The GMCH supports only 1.5 V signaling for the DVO ports. Because the 845GL/845GV chipset has other interfaces that utilize 1.5 V, a separate 1.5 V supply for the DVO interface is not required, as long as appropriate decoupling and power delivery guidelines are followed.

19.4.4.1 VREF Generation

Regardless if the DVO interfaces are being used, the GMCH always requires AGP_VREF to be supplied. When utilizing the DVO ports, the DVO device can also use this reference supply. See Figure 205 for an example circuit.

Figure 205. VREF Generation





19.4.4.2 Compensation

The GMCH DVO interface supports resistive buffer compensation (RCOMP). Tie the AGP_RCOMP pin to a 40 Ω , 1% pull-down resistor (to ground) through a very short (<0.5”) trace. This should be done whether or not the DVO ports are being utilized.

19.4.4.3 DVO Pull-Ups

DVO control signals require resistors that pull up to VDDQ on the motherboard, to ensure that they contain stable values when no agent is actively driving the bus.

Control signals (MI2C, MDVI and MDDC pairs) should have 4.7 k Ω pull-ups to 1.5 V (or pull-ups with the appropriate value derived from simulation). In addition to this, the Fld/Stall signals should have weak pull downs (8 k Ω – 10 k Ω) while the DVOBC_CLKINT# and DVOBC_INTR# signals should have weak pull-ups (8 k Ω – 10 k Ω).

19.4.4.3.1 DVO Signal Voltage Tolerance List

All DVO related signals discussed in this section are 1.5 V tolerant. If higher signaling voltages are needed (e.g., 3.3 V for MI2C and 5 V for MDVI), then level-shifting devices will be required on the motherboard.

19.4.4.4 DVO Clocking

The digital display interface is clocked source synchronously by the GMCH. The digital display interface clocking scheme uses four output clock signals: DVOB_CLK and DVOB_CLK#, and DVOC_CLK and DVOC_CLK #, and a single clock input: DVOBC_CLKINT#. The four output clocks should be routed according to the DVO guidelines detailed in previous sections. DVOBC_CLKINT# is only an input clock when the DVO device is running in TV-Out mode.

DVOx_CLK is the primary clock of the differential pair. Care should be taken to ensure that DVOx_CLK is connected to the primary clock receiver on the DVO device. If the DVO device supports differential clocking mode (highly recommended), then DVOx_CLK# should be connected to the complementary clock receiver of the DVO device.

19.4.5 Leaving the Intel® 845GL/845GV Chipset DVO Port Unconnected

If the motherboard does not implement any of the possible graphics/display devices with the DVO port, the following is recommended on the motherboard:

- Voltages, including AGP_VREF, must still be supplied to the GMCH.
- Signals can be left as NCs — boards may want to have back up sites for the pull-up resistors outlined in Section 19.4.4.3.
- AGP_RCOMP should still be connected to a 40 Ω 1% pull down to ground.



19.5 Intel® 845GL/845GV Chipset Design Layout Checklist

This section describes specific changes to the 845G Chipset Layout Checklist in Chapter 18 that pertain to the 845GL/845GV chipset design. These changes should be used in conjunction the checklist in Chapter 18. The specific items in this section are to be used instead of those in Chapter 18.

This checklists highlight design considerations that should be reviewed prior to manufacturing a motherboard that implements the 845GL/845GV chipset. The items in the checklists attempt to address important connections to devices and critical supporting circuitry. **These are not a complete lists, and they do not guarantee that a design will function properly.** Beyond the items contained in the checklists, refer to the Customer Reference Board schematics in Appendix A for more detailed instructions on designing a motherboard. This work is ongoing, and the recommendations and considerations herein are subject to change.

19.5.1 Dedicated DVO

The information in the following sections replaces information in *Section 18.4* when designing with the 845GL/845GV chipset.

19.5.1.1 Miscellaneous Timing Domain Signals

Miscellaneous Signals: ADDID[7:0], ADD_DETECT#, DVOBC_CLKINT#, DVOBC_INTR#, MDVI_CLK, MDVI_DATA, MDDC_CLK, MDDC_DATA, MI2C_CLK, MI2C_DATA	
Miscellaneous Timing Domain Routing Recommendation	Reason/Impact/Documentation
• 7.5" max trace length	Refer to Section 19.4.3.2.
• 5 mils wide with 7 mil trace separation.	Refer to Section 19.4.3.2.
• MI2C_CLK and MI2C_DATA should be matched (\pm 250 mils) • MDVI_CLK and MDVI_DATA should be matched (\pm 250 mils) • MDVI_CLK and MDVI_DATA should be matched (\pm 250 mils)	Refer to Section 19.4.3.2.



19.5.1.2 DVO Timing Domain Signals

DVO Timing Domain Signals: DVOB_D[11:0], DVOB_HSYNC, DVOB_VSYNC, DVOB_CLK, DVOB_CLK#, DVOB_BLANK#, DVOB_FLDSTL, DVOC_D[11:0], DVOC_HSYNC, DVOC_VSYNC, DVOC_CLK, DVOC_CLK#, DVOC_BLANK#, DVOC_FLDSTL	
DVO Timing Domain Routing Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> • 7.5" max trace length 	Refer to DG Section 19.4.3.
<ul style="list-style-type: none"> • 1:3 trace width-to-spacing 	Refer to DG Section 19.4.3.
<ul style="list-style-type: none"> • Breakout Guidelines: 5 mil spacing, 0.3" max length 	Refer to DG Section 19.4.3.
<ul style="list-style-type: none"> • Clocks should match their complement to ± 50 mils 	Refer to DG Section 19.4.3.
<ul style="list-style-type: none"> • Data to Clock length mismatch ± 0.125" from GMCH pad to DVO Device pin 	Refer to DG Section 19.4.3.
<ul style="list-style-type: none"> • DVOB_CLK should match DVOC_CLK to ± 0.125" 	Refer to DG Section 19.4.3.

19.5.1.3 DVO Miscellaneous and DVO Timing Domain Common Routing

Recommendation	Reason/Impact/Documentation
<ul style="list-style-type: none"> • Trace length mismatch for all signals within a signal group should be as close to zero as possible 	To provide timing margin Refer to Table 118.
<ul style="list-style-type: none"> • Separate the traces as much as possible 	Reduce trace-to-trace coupling Refer to Table 118.
<ul style="list-style-type: none"> • Data and associated clock signals must not be routed on a separate layer for more than 3". 	Refer to Table 118.
<ul style="list-style-type: none"> • These guidelines apply to board stack-ups with 15% impedance tolerance. 	Refer to Table 118.

19.5.1.4 DVO Clock Routing, Decoupling, VREF

Recommendation	Reason/Impact/Documentation
<p>Clock</p> <ul style="list-style-type: none"> • DVOx_CLK is the primary clock of the differential pair. • DVOx_CLK is connected to the primary clock receiver on the DVO device. • If the DVO Device supports differential clocking mode, DVOx_CLK# should be connected to the complementary clock receiver on the DVO device. 	<p>Refer to Section 19.4.4.</p>
<p>Decoupling</p> <ul style="list-style-type: none"> • Five 0.1 μF capacitors required • Evenly distribute placement of decoupling capacitors in the DVO interface signal field. • Must be as close as possible to the GMCH, within 100 mils of the GMCH outer row of balls. • DVO signal trace spacing may be reduced as the traces go around each cap. This space reduction should be minimal and for as short a • Use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric. • Place bypass capacitors at vias that transition the DVO signal from one reference signal plane to another. 	<p>Refer to Section 19.4.3.4.</p>
<p>DVO Device Decoupling</p> <ul style="list-style-type: none"> • Consult with the DVO device vendor for appropriate DVO device decoupling and power delivery. 	<p>To address AC signaling issues. Refer to Section 19.4.3.4.</p>
<p>VREF</p> <ul style="list-style-type: none"> • Voltage divider with 1 kΩ 1% to produce 0.75 V – connected to both AGP_ref on GMCH and VREF on DVO Device. 0.1 μF Cap on net at both DVO Device and GMCH. 	<p>Refer to DG Section 19.4.4</p>
<p>RCOMP</p> <ul style="list-style-type: none"> • 0.5" max length • 40 Ω \pm 1% down to ground 	<p>Refer to Section 19.4.4.</p>



19.6 Intel® 845GL/845GV Chipset Schematic Checklist

This section describes specific changes to the 845G Chipset Schematic Checklist in Chapter 17 that pertain to the 845GL/845GV chipset design. These changes should be used in conjunction the checklist in Chapter 17. The specific items in this section are to be used instead of those in Chapter 17.

This checklists highlight design considerations that should be reviewed prior to manufacturing a motherboard that implements the 845GL chipset. The items in the checklists attempt to address important connections to devices and critical supporting circuitry. **These are not a complete lists, and they do not guarantee that a design will function properly.** Beyond the items contained in the checklists, refer to the Customer Reference Board schematics in Appendix A for more detailed instructions on designing a motherboard. This work is ongoing, and the recommendations and considerations herein are subject to change.

19.6.1 Dedicated DVO Interface

The following replaces Sections 17.3 – 17.4 of the Design Guide.

19.6.1.1 DVO Intel® GMCH Only Items

Checklist Item	Recommendation	Reason/Impact/Documentation
AGP_RCOMP	<ul style="list-style-type: none"> Pull-down to GND through a 40.2 Ω \pm1% resistor 	
VCCAGP	<ul style="list-style-type: none"> Connect to 1.5 V power plane 	

19.6.2 DVO Down / Intel® GMCH Items

Checklist Item	Recommendation	Reason/Impact/Documentation
DVOB_CLK	<ul style="list-style-type: none"> Connect to GMCH 	Refer to Section 19.4
DVOB_CLK#	<ul style="list-style-type: none"> Connect to GMCH 	Refer to Section 19.4
DVOC_CLK	<ul style="list-style-type: none"> Connect to GMCH 	Refer to Section 19.4.
DVOC_CLK#	<ul style="list-style-type: none"> Connect to GMCH 	Refer to Section 19.4.
DVOB_D[11:0]	<ul style="list-style-type: none"> Connect to GMCH 	Refer to Section 19.4.
DVOB_HSYNC	<ul style="list-style-type: none"> Connect to GMCH 	Refer to Section 19.4.
DVOB_VSYNC	<ul style="list-style-type: none"> Connect to GMCH 	Refer to Section 19.4.
DVOB_BLANK#	<ul style="list-style-type: none"> Connect to GMCH 	Refer to Section 19.4
DV0BCCLKINT	<ul style="list-style-type: none"> Connect to GMCH 	Refer to Section 19.4.
DVOB_FLDSTL	<ul style="list-style-type: none"> Connect to GMCH 	Refer to Section 19.4.
DVOBCRCOMP	<ul style="list-style-type: none"> Pull down through a 40.2Ω 1% resistor connect to AGP_RCOMP on GMCH 	Refer to Section 19.4.

Checklist Item	Recommendation	Reason/Impact/Documentation
MDVI_DATA	<ul style="list-style-type: none"> • Connect to GMCH • Pull-up resistor to VDDQ • May require level shifting 	Refer to Section 19.4
MDVI_CLK	<ul style="list-style-type: none"> • Connect to GMCH • May require level shifting 	Chipset has integrated pull-ups, but signal may still require external pull-up resistors. Refer to Section 19.4
MDDC_CLK	<ul style="list-style-type: none"> • Connect to GMCH • Pull-up resistor to VDDQ • May require level shifting 	
MDDC_DATA	<ul style="list-style-type: none"> • Connect to GMCH • May require level shifting 	Refer to Section 19.4
MI2C_DATA	<ul style="list-style-type: none"> • Connect to GMCH • Pull-up resistor to VDDQ • May require level shifting 	Refer to Section 19.4
MI2C_CLK	<ul style="list-style-type: none"> • Connect to GMCH • Pull-up resistor to VDDQ • May require level shifting 	Refer to Section 19.4
DVOC_D[11:0]	<ul style="list-style-type: none"> • Connect to GMCH 	Refer to Section 19.4
DVOC_HSYNC	<ul style="list-style-type: none"> • Connect to GMCH 	Refer to Section 19.4
DVOC_VSYNC	<ul style="list-style-type: none"> • Connect to GMCH 	Refer to Section 19.4
DVOC_BLANK	<ul style="list-style-type: none"> • Connect to GMCH 	Refer to Section 19.4
DVOBC_INTR#	<ul style="list-style-type: none"> • Connect to GMCH 	Refer to Section 19.4
DVOC_FLDSTL	<ul style="list-style-type: none"> • Connect to GMCH 	Refer to Section 19.4
ADDID[7:0]	<ul style="list-style-type: none"> • Connect to GMCH 	Chipset has integrated pull-ups for these signals.



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Appendix B Customer Reference Board Schematics

This appendix provides a set of schematics for the Intel® Pentium 4 processor in 478-pin Package and Intel 845G chipset platform Customer Reference Board (CRB).

B.1 Intel® 845G Chipset DDR Schematics

Refer to the following pages for the 845G chipset DDR Schematics.

B.2 Intel® 845G Chipset SDR Schematics

The 845G chipset SDR Schematics follow the 845G chipset DDR schematics.



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1	COVER PAGE.
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3	TABLES: RESET MAP
4	TABLES: CLOCK DISTRIBUTION
5	TABLES: GPIO/IDSEL MAPPING
6	TABLES: VOLTAGE DISTRIBUTION
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8	CORE: CPU CONNECTOR
9	CORE: CPU PULLUPS & PULLDOWNS /VCCPVID, VCC_VIDGG
10	CORE: CPU ANALOG FILTER
11-13	CORE: INTEL(R) 845G GMCH
14	BLANK
15	CORE: INTEL(R) 845G DECOUPLING & REFERENCE VOLTAGES
16	CORE: DDR SERIES TERMINATION
17	CORE: DIMM CONNECTORS
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20	CORE: DDR VTERM CAPS
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22	CORE: VGA CONNECTOR
23-24	ICH: 82801DB I/O CONTROLLER HUB
25	ICH: ICH PULL-UP/PULL-DOWNS
26	ICH: LAN LINK
27	ICH: IDE PRIMARY & SECONDARY
28	ICH: USB BACK PANEL CONNECTORS
29	BLANK
30	ICH: USB FRONT PANEL/CNR UREG & OC#.
31-33	ICH: PCI SLOTS 3 - 1
34	ICH: PCI PULL-UPS
35	SMBUS ISOLATION
36	CNR CONNECTOR
37	BLANK
38	AUDIO: CODEC (AD1885 OR CS4201)
39	AUDIO: CODEC FILTERING CAPS
40	AUDIO: AUX-IN, CD-IN, LINE-IN: ATAPI HEADERS
41	AUDIO: MIC-IN
42	AUDIO: LINE-OUT
43	AUDIO: FRONT PANEL AUDIO HEADER
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PAGE # COMPONENT/FUNCTION

49	SIO: PARALLEL PORT
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62	UREG: USB BACK PANEL, PS/2
63	UREG: 1.5V STBY & 3.3V STBY
64	UREG: BULK DECOUPLING
65	UREG: 2.5V STR DECOUPLING
66	UREG: CORE 1.5V
67	UREG: CPU MAIN REGULATOR (VCCP)
68	UREG: CPU DECOUPLING, 12V CONN/FILTER INDUCTOR
69	DCL TRACK SPLITTERS
70	BLANK
71	DEBUG: ITP PORT AND PULL-UPS
72	MOON ISA RESISTORS
73-74	BLANK
75	DEBUG: PORT80 DECODER

INTEL(R) 845G
DDR SCHEMATICS
REV 2.0

POWER SYMBOLS USED:

VCC3
VCC
+12V
-12V

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPL'S FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5 VOLTS UNLESS OTHERWISE SPECIFIED.
4. VCC3 = +3.3 VOLTS UNLESS OTHERWISE SPECIFIED.
5. * SUFFIX INDICATES ACTIVE LOW SIGNAL.

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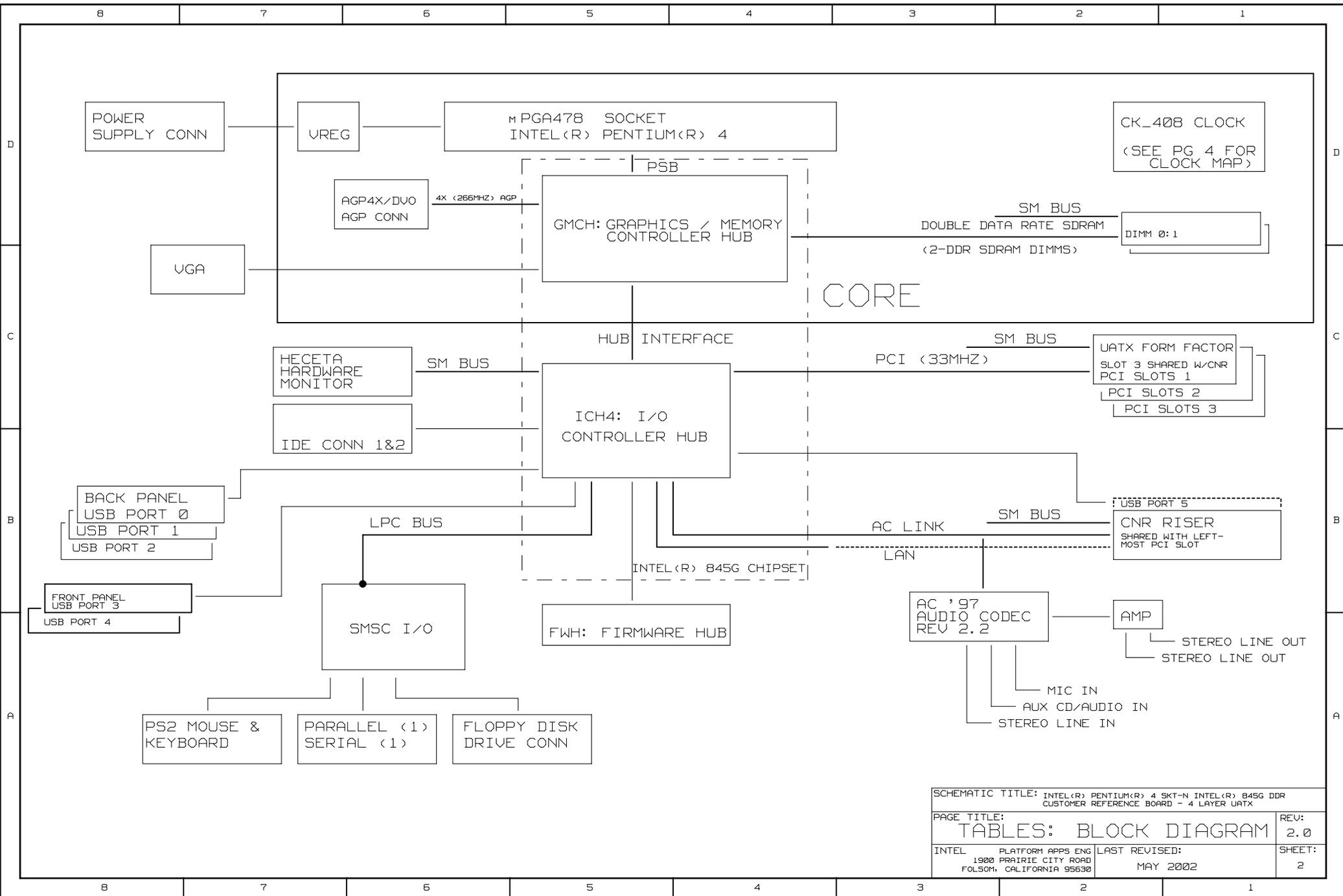
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CUSTOMER REFERENCE BOARD (CRB)
2-DDR SDRAM, 4 LAYER, UATX

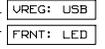
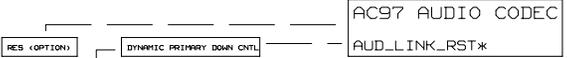
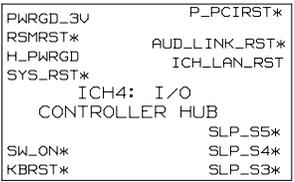
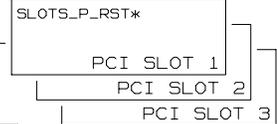
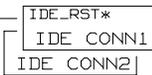
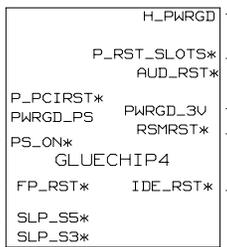
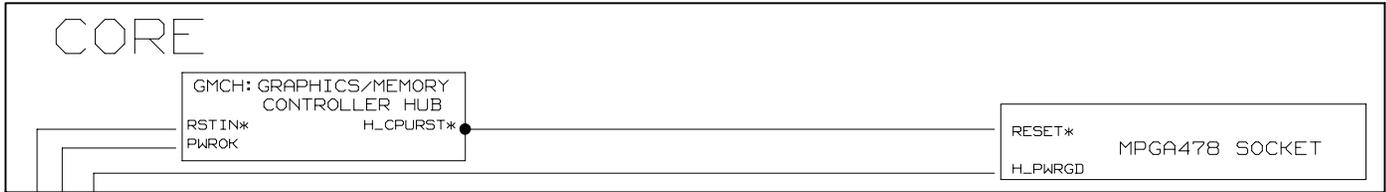
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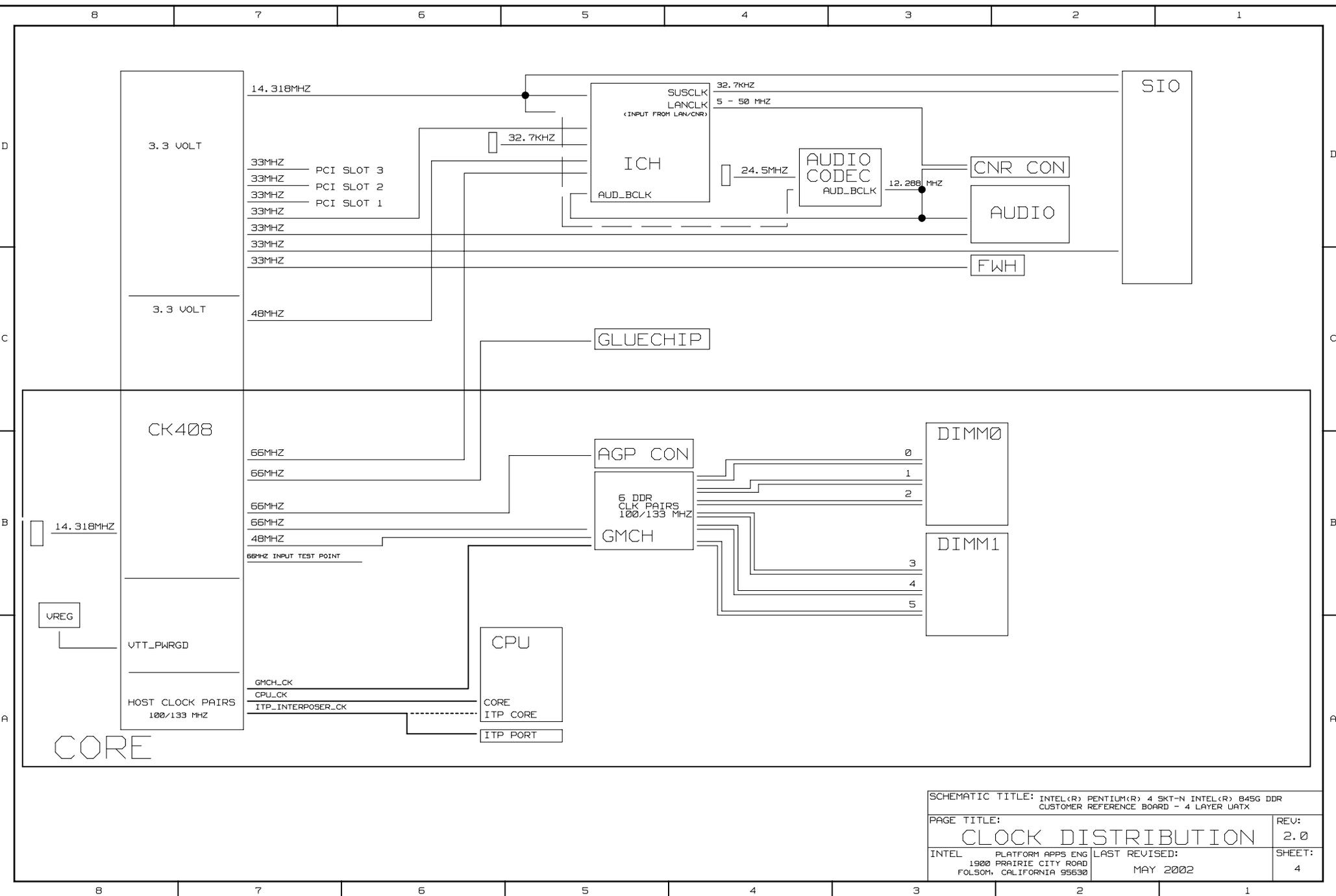
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RESET MAP

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PAGE TITLE: CLOCK DISTRIBUTION	REV: 2.0
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ICH4

PIN NAME	PWR WELL	USAGE	DURING RESET	S3/S4/S5	INTERNAL PULL-UP	NOTES
GPI<0>	CORE	P_REQA#	---	---		
GPI<1>	CORE	P_REQB#	---	---		
GPI<2>	CORE	P_IRQE#	---	---		
GPI<3>	CORE	P_IRQF#	---	---		
GPI<4>	CORE	P_IRQG#	---	---		
GPI<5>	CORE	P_IRQH#	---	---		
GPI<6>	CORE	UNUSED	---	---		
GPI<7>	CORE	UNUSED	---	---		
GPI<8>	RESUME	UNUSED	---	---		
GPI<11>	RESUME	SMB_ALERT#	---	---		
GPI<12>	RESUME	LPC_SIO_SMI#	---	---		
GPI<13>	RESUME	LPC_SIO_PME#	---	---		
GPO<16>	CORE	P_GNTA#	HIGH	OFF	24K	
GPO<17>	CORE	P_GNTS#	HIGH	OFF	24K	
GPO<18>	CORE	UNUSED	HIGH	OFF		
GPO<19>	CORE	UNUSED	HIGH	OFF		
GPO<20>	CORE	UNUSED	HIGH	OFF		
GPO<21>	CORE	ISA_GO_NOGO	HIGH	OFF		
GPO<22>	CORE	UNUSED	HIGH-Z	OFF		
GPO<23>	CORE	UNUSED	LOW	OFF		
GPIO<24>	RESUME	UNUSED	LOW	DEFINED		
GPIO<25>	RESUME	GPO_GRN_BLNK	HIGH	DEFINED		
GPIO<27>	RESUME	GPO_YEL_BLNK	HIGH	DEFINED		
GPIO<28>	RESUME	GPO_LAN_DISABLE	HIGH	DEFINED		
GPIO<32>	CORE	NO_POP*	HIGH	OFF		
GPIO<33>	CORE	UNUSED	HIGH	OFF		
GPIO<34>	CORE	UNUSED	HIGH	OFF		
GPIO<35>	CORE	UNUSED	HIGH	OFF		
GPIO<36>	CORE	UNUSED	HIGH	OFF		
GPIO<37>	CORE	<BOARD1>	HIGH	OFF		
GPIO<38>	CORE	<BOARD2>	HIGH	OFF		
GPIO<39>	CORE	<BOARD3>	HIGH	OFF		
GPIO<40>	CORE	<BOARD4>	HIGH	OFF		
GPIO<41>	CORE	UNUSED	HIGH	OFF		
GPIO<42>	CORE	UNUSED	HIGH	OFF		
GPIO<43>	CORE	CDC_DWN_ENAB*	HIGH	OFF		
RI*	RESUME					
THERM*	CORE					

IRQ ROUTING TABLE

	AGP	SLOT1	SLOT2	SLOT3	AC97/SMBUS	LAN
INT A	A			D		
INT B	B			C	A	
INT C				A		
INT D				B		
INT E		D	C			A
INT F		A	B			
INT G		B	A			
INT H		C	D			
REG /GNT						
IDSEL		16	17	18		24

ICH4

FWH

GPI4	CONFIG JUMPER	INPUT	DEFINED	CONFIG JUMPER
GPI3	MANUF MODE	INPUT	DEFINED	MANUF MODE
GPI2	HI/LOW BIOS CONFIG	INPUT	DEFINED	SPARE HI/LOW BIOS CONFIG STRAP
GPI1	GPIO_DMA66_DETECT_SEC	INPUT	DEFINED	ATA66 CABLE DETECT - SECONDARY
GPI0	GPIO_DMA66_DETECT_PRI	INPUT	DEFINED	ATA66 CABLE DETECT - PRIMARY

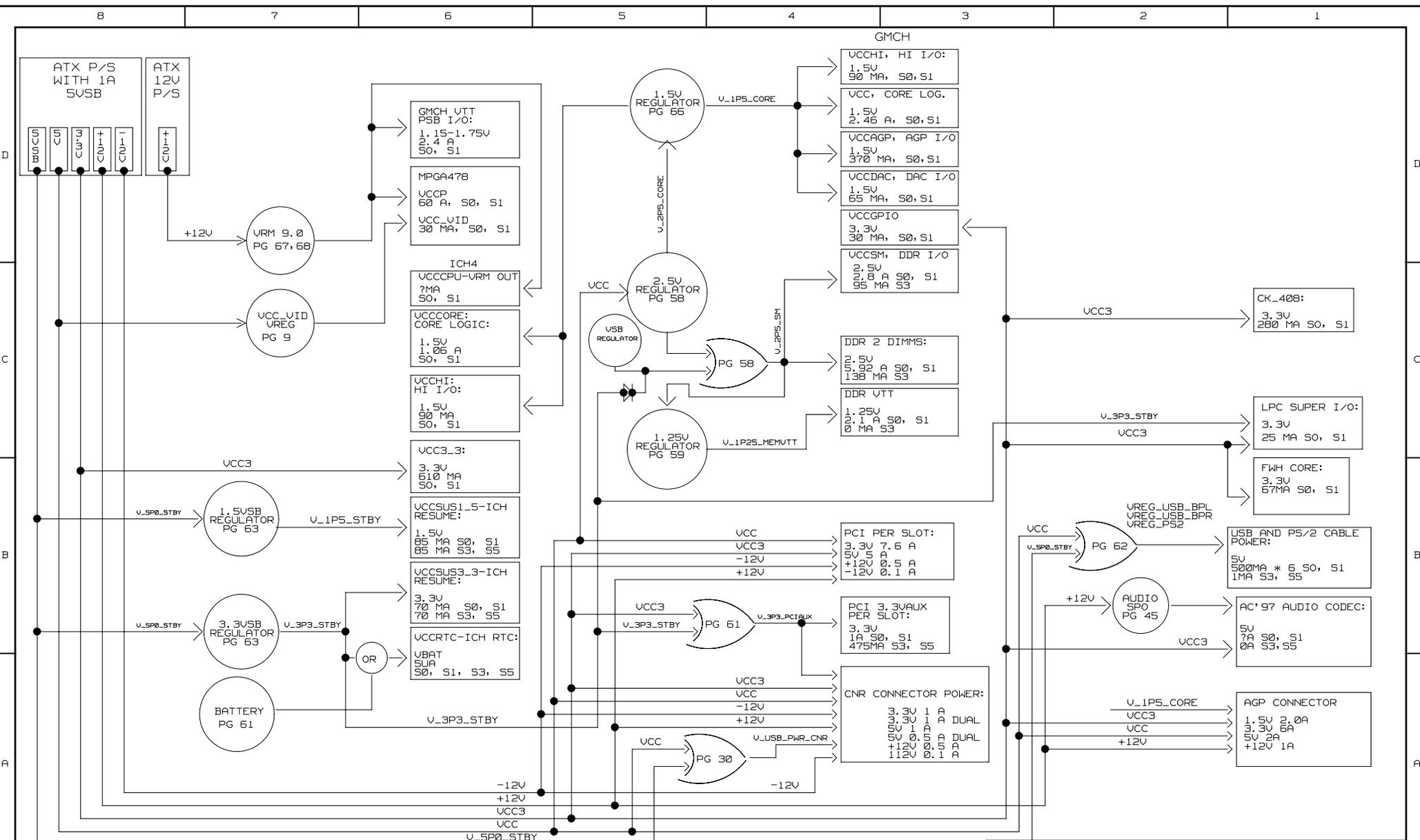
SIO

GPI020	RESISTOR STRAP OPTION	INPUT	DEFINED	DESIGN FEATURE WITH RESISTOR STRAPPING
GPI021	RESISTOR STRAP OPTION	INPUT	DEFINED	DESIGN FEATURE WITH RESISTOR STRAPPING
GP027/IOSMI*	IO_SMI*	INPUT	DEFINED	SENDS IO SMI REQUEST TO ICH2

MULTI-PLEXED GPIO PINS ON SIO USED FOR SPECIFIC FUNCTIONS (NOT AS GPIO) ARE NOT IDENTIFIED HERE
 UN-USED GPIO PINS ON SIO ARE NOT IDENTIFIED HERE

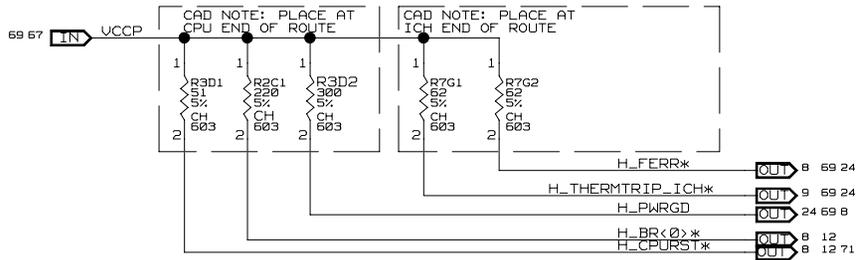
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INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 5

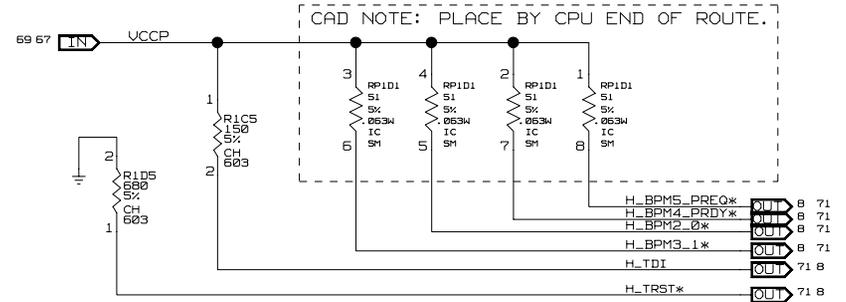


SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR
 CUSTOMER REFERENCE BOARD - 4 LAYER UATX
 PAGE TITLE: VOLTAGE DISTRIBUTION
 REV: 2.0
 INTEL PLATFORM APPS ENG LAST REVISED: SHEET: 6
 1900 PRAIRIE CITY ROAD MAY 2002 FOLSOM, CALIFORNIA 95630

CPU SIGNAL TERMINATION

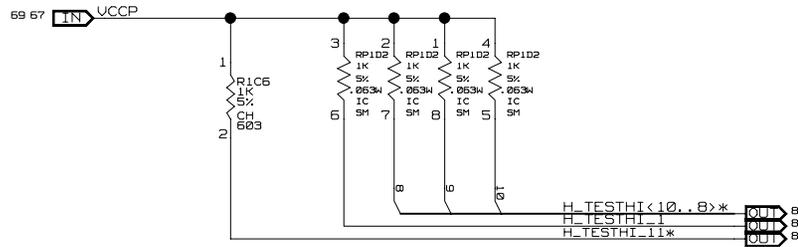


I/TAP TERMINATION

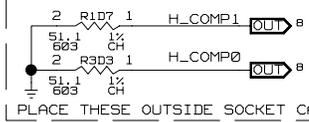


CAD NOTE: PLACE THESE RESISTORS CLOSE TO THE CPU SOCKET

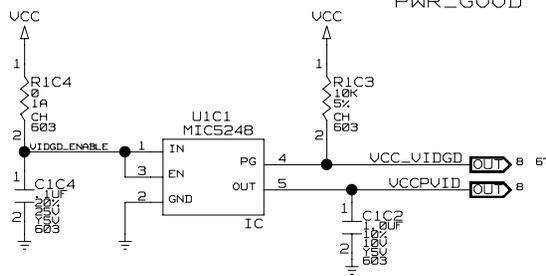
TESTHI PULLUPS



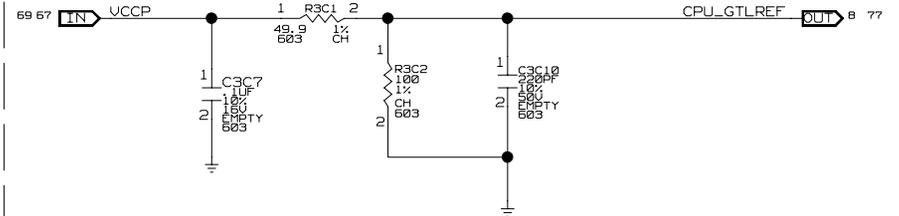
PRECISION FSB COMPENSATION RESISTORS



PWR_GOOD

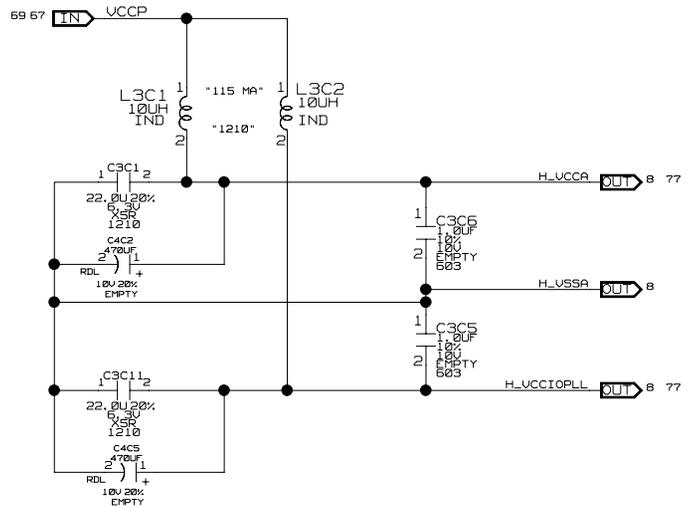


GTLREF GENERATION CIRCUITS



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: CPU PULLUPS/PULLDNS/TERMINATION	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 9

PLL SUPPLY FILTER

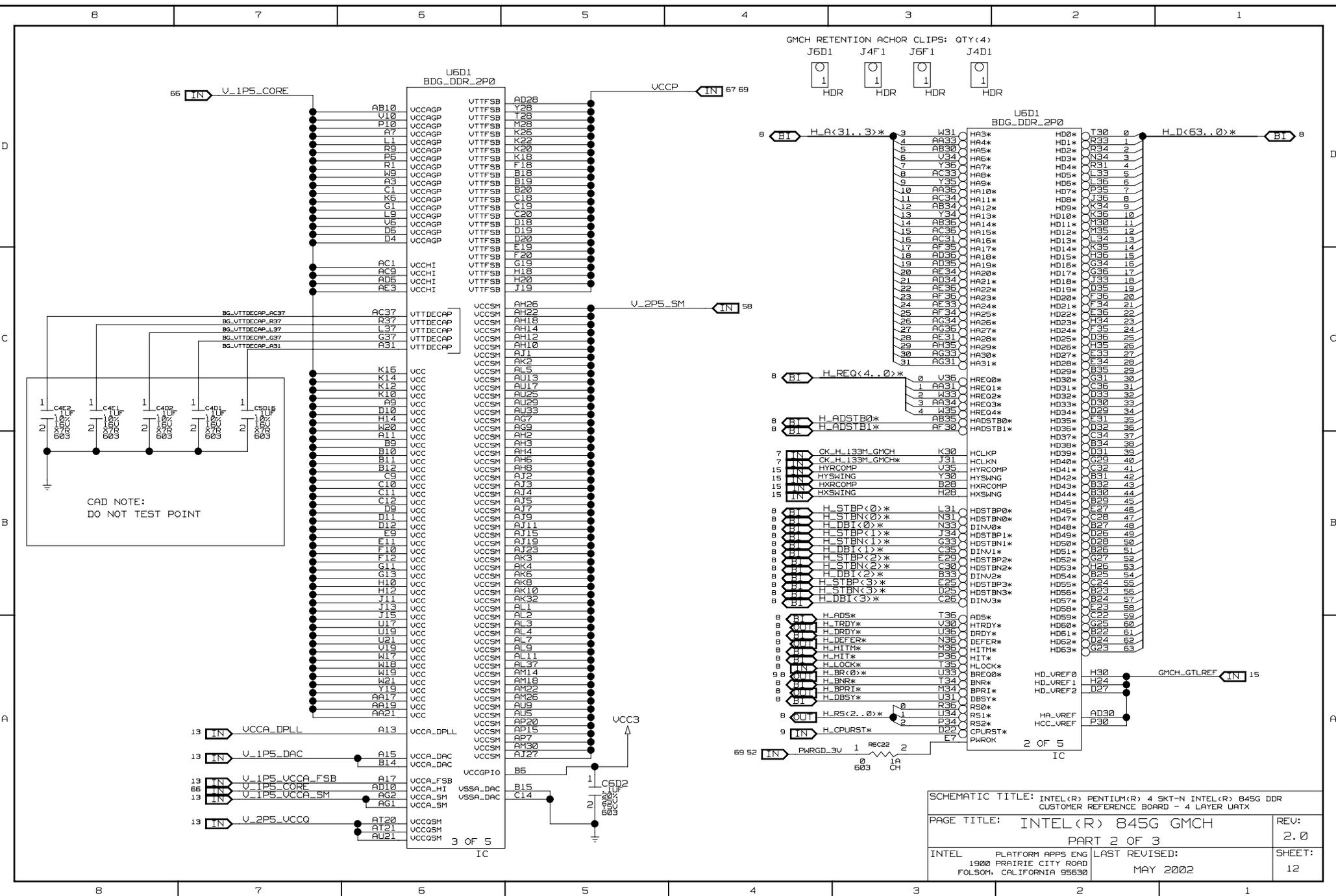


CAD NOTE:

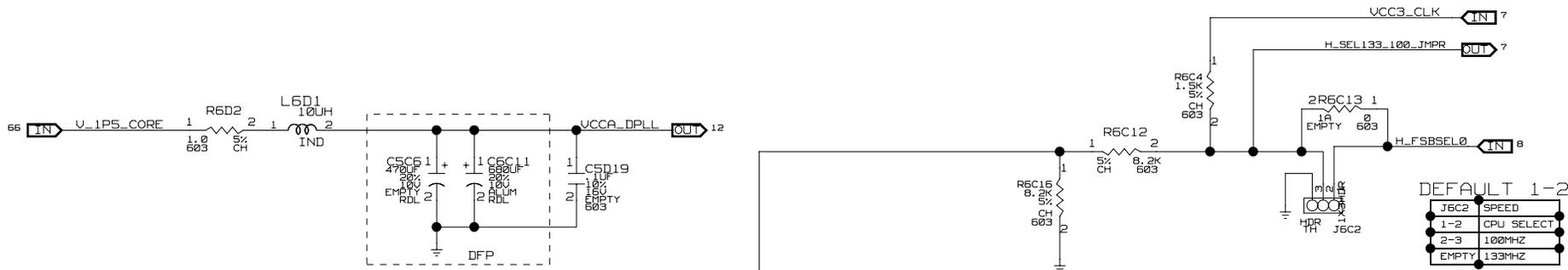
PLACE THMT CAPS OUTSIDE RM BOUNDARY.
 TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MIL
 CAD NOTE: PLACE COMPONENTS AS CLOSE AS POSSIBLE TO
 PROCESSOR SOCKET

FILTERED ANALOG SUPPLY

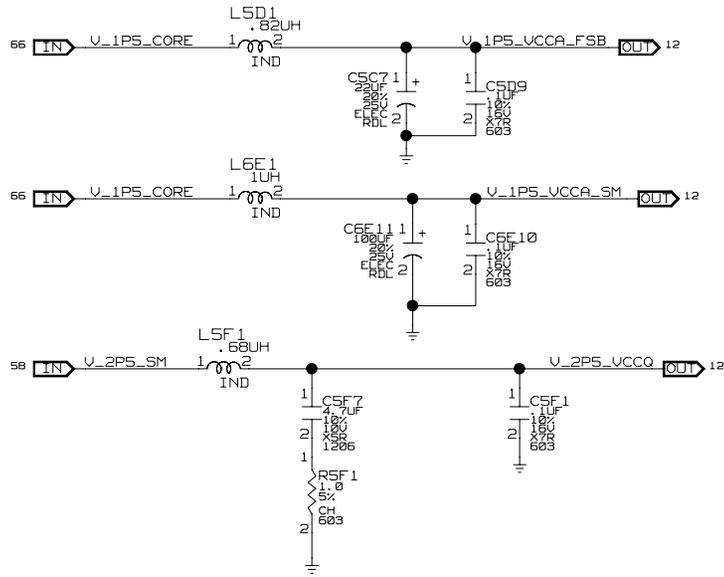
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: FILTERED ANALOG SUPPLY	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 10



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR
 CUSTOMER REFERENCE BOARD - 4 LAYER UATX
 PAGE TITLE: INTEL(R) 845G GMCH
 PART 2 OF 3
 INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
 LAST REVISED: MAY 2002
 REV: 2.0
 SHEET: 12



ANALOG FILTERS



SCHMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: INTEL(R) 845G GMCH
PART 3 OF 3

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002

1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

REV: 2.0

SHEET: 13

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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: BLANK
REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002
1900 PRAIRIE CITY ROAD SHEET: 14
FOLSOM, CALIFORNIA 95630

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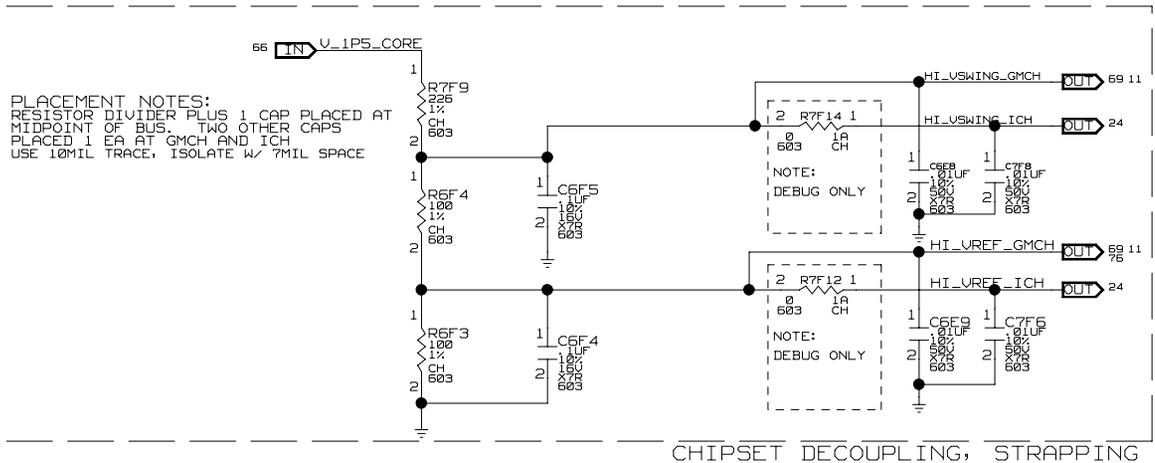
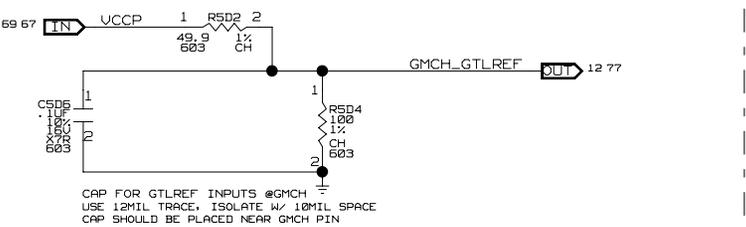
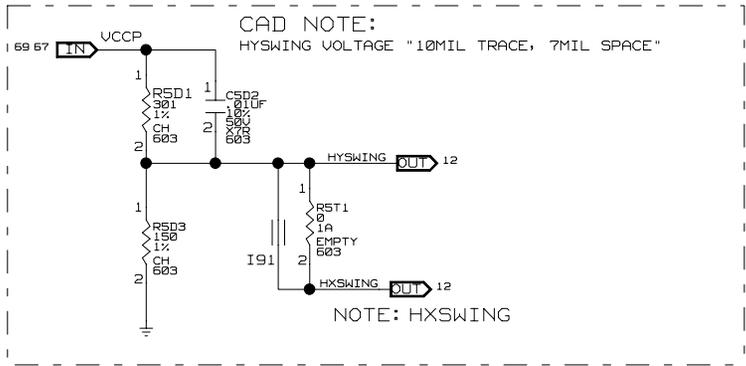
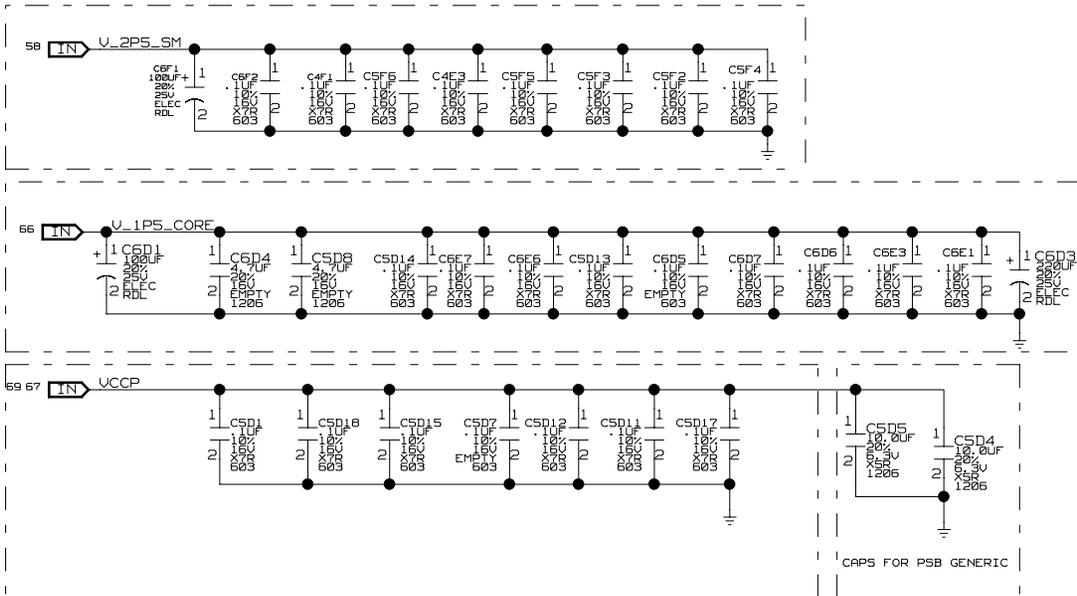
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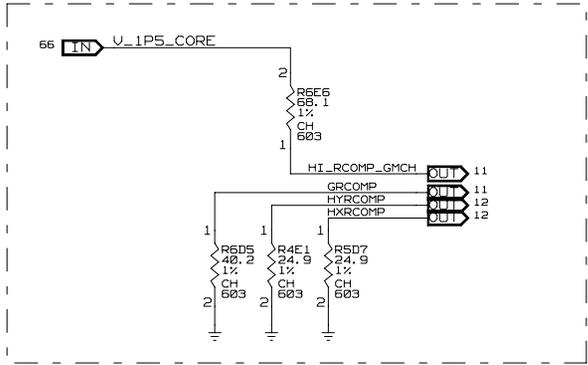
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SYSTEM MEMORY DECOUPLING

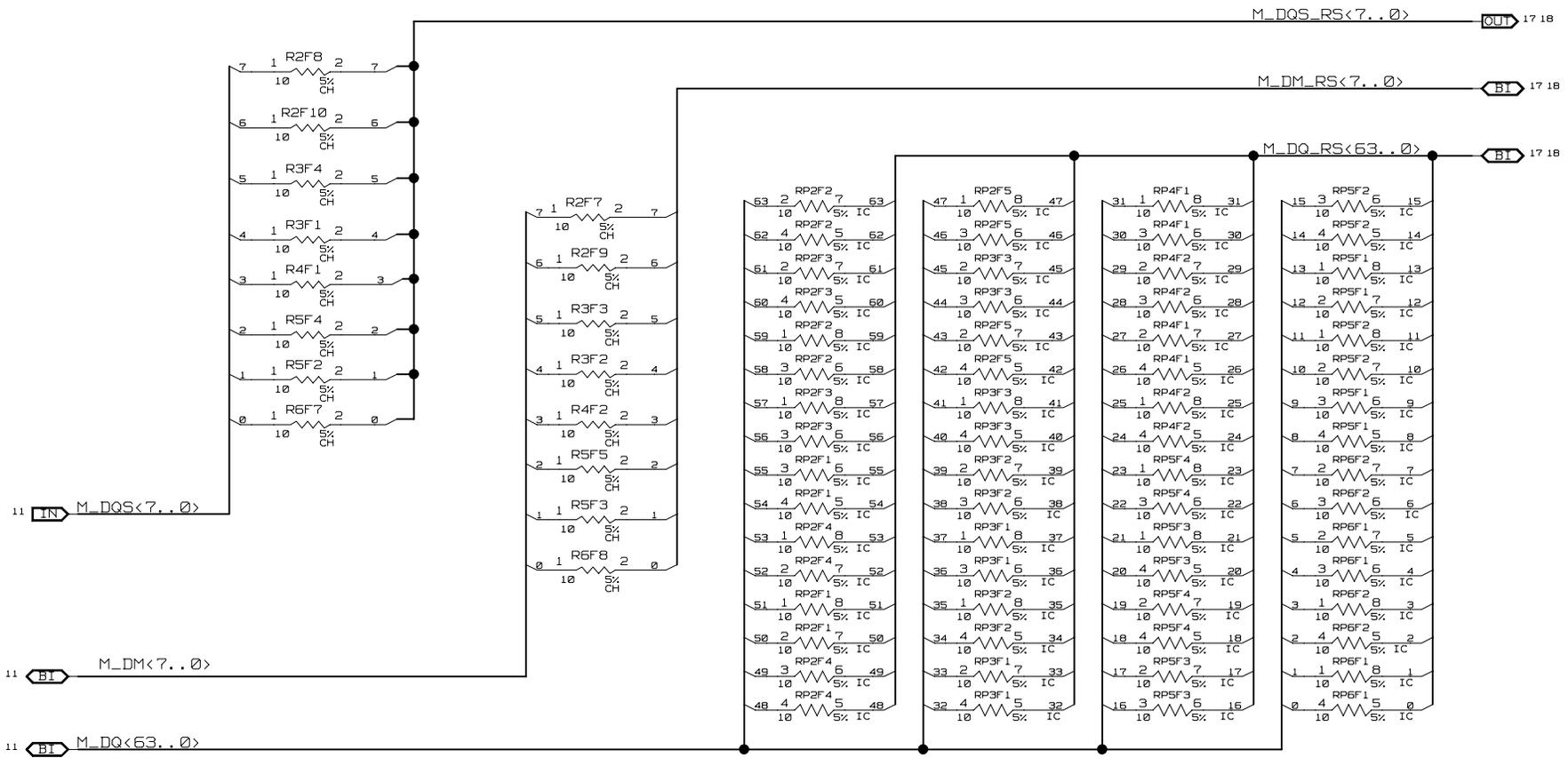


CHIPSET DECOUPLING, STRAPPING

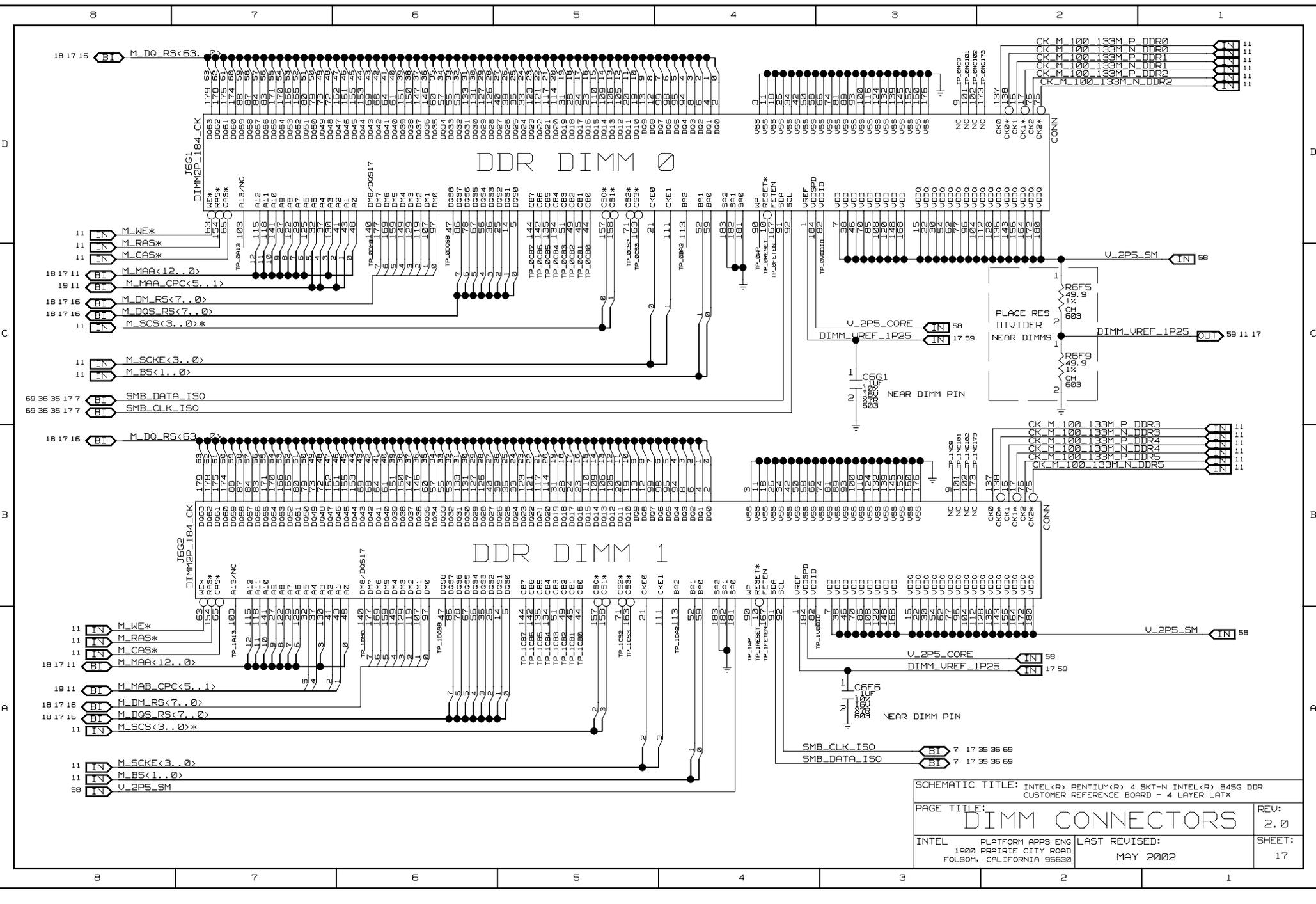


SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: DECOUPLING & REFERENCE VOLTAGES	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 15

DDR SERIES RESISTORS



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: DDR SERIES RESISTORS		REV: 2.0
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG LAST REVISED: MAY 2002	SHEET: 16



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR
 CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: DIMM CONNECTORS

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002

1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630

REV: 2.0

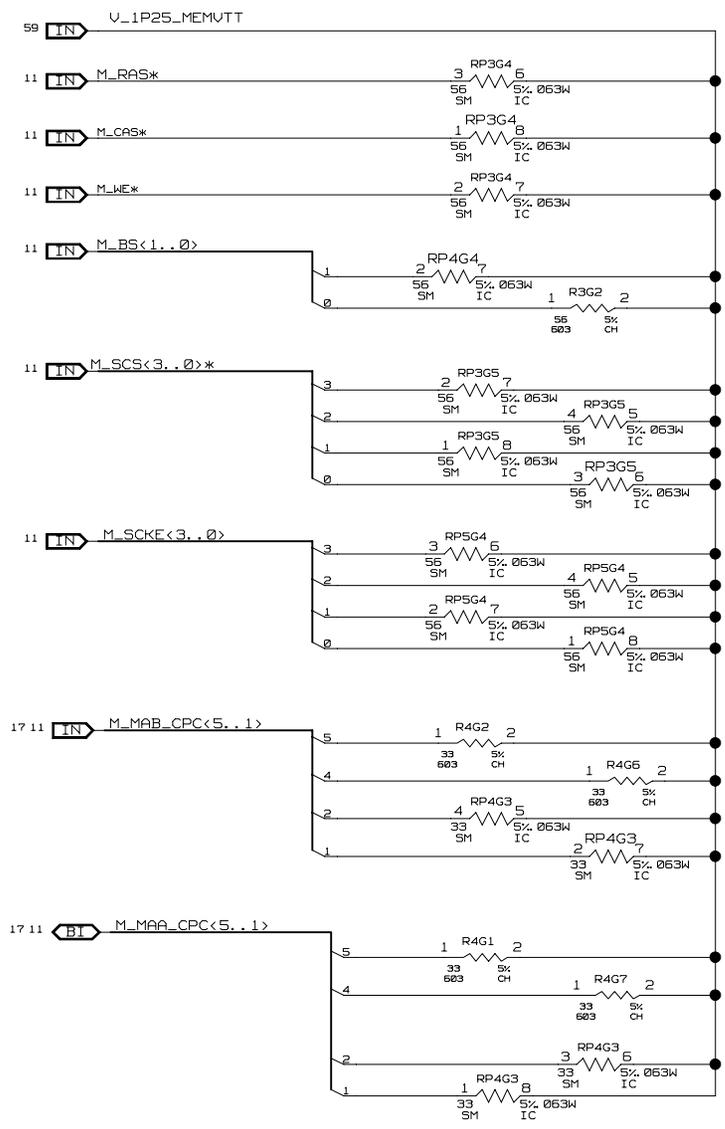
SHEET: 17

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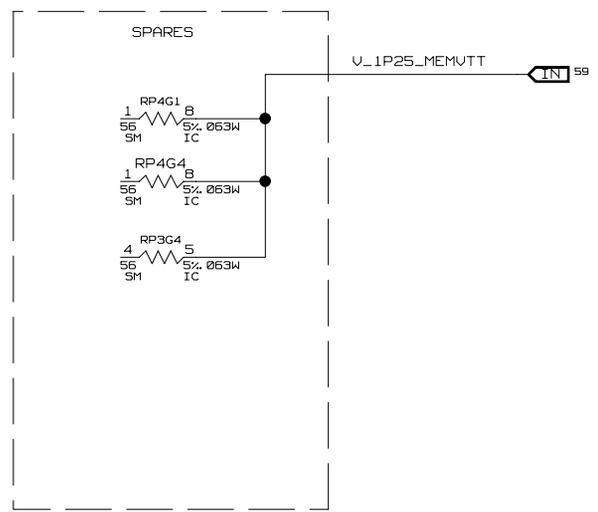
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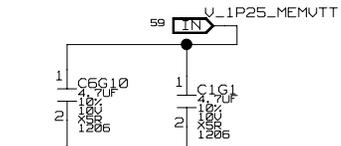


DDR TERMINATION RESISTORS



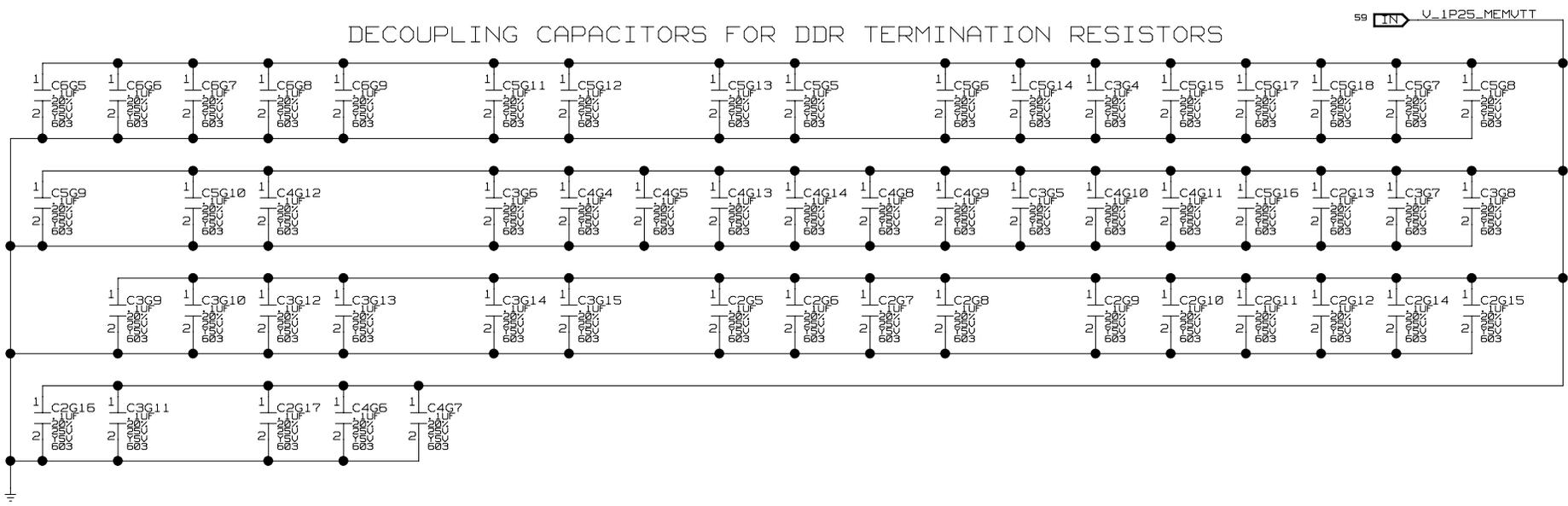
NOTE:
 CS SIGNALS MUST HAVE IT'S OWN RES/RPACK
 CKE SIGNALS MUST HAVE IT'S OWN RES/RPACK
 CPC SIGNALS MUST HAVE IT'S OWN RES/RPACK

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: DDR TERMINATION RESISTORS	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002 SHEET: 19



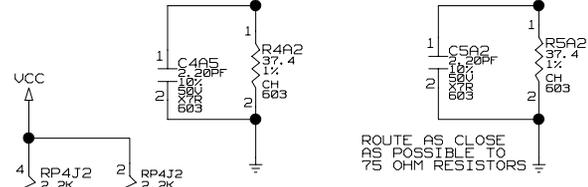
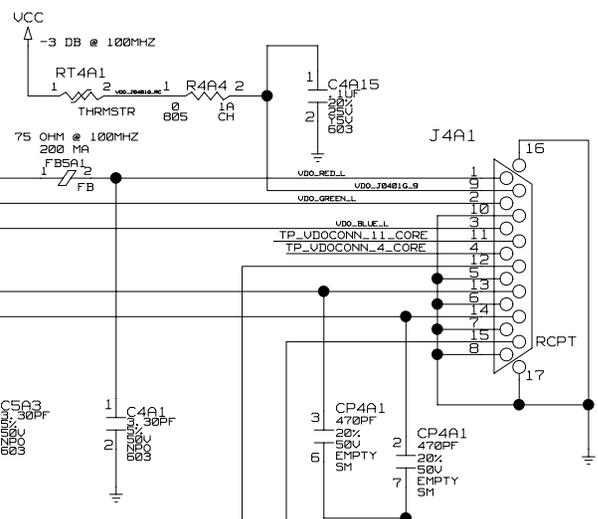
PLACED AT LEFT AND RIGHT ENDS
OF VTT ISLAND

DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 20

69 13 [IN] UGA_RED
 69 13 [IN] UGA_RED*
 69 13 [IN] UGA_GREEN
 69 13 [IN] UGA_GREEN*
 69 13 [IN] UGA_BLUE
 69 13 [IN] UGA_BLUE*
 69 13 [IN] HSYNC_5V
 69 13 [IN] VSYNC_5V



COMP PINS WANT RESISTOR
 CLOSEST TO 37.5 OHMS 1%

ROUTE AS CLOSE
 AS POSSIBLE TO
 75 OHM RESISTORS

52 [BI] GLUE4_DDCSDA_5V

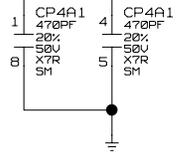
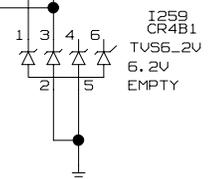
52 [BI] GLUE4_DDCSCL_5V

VDO_MONID1_R

VDO_MONID2_R

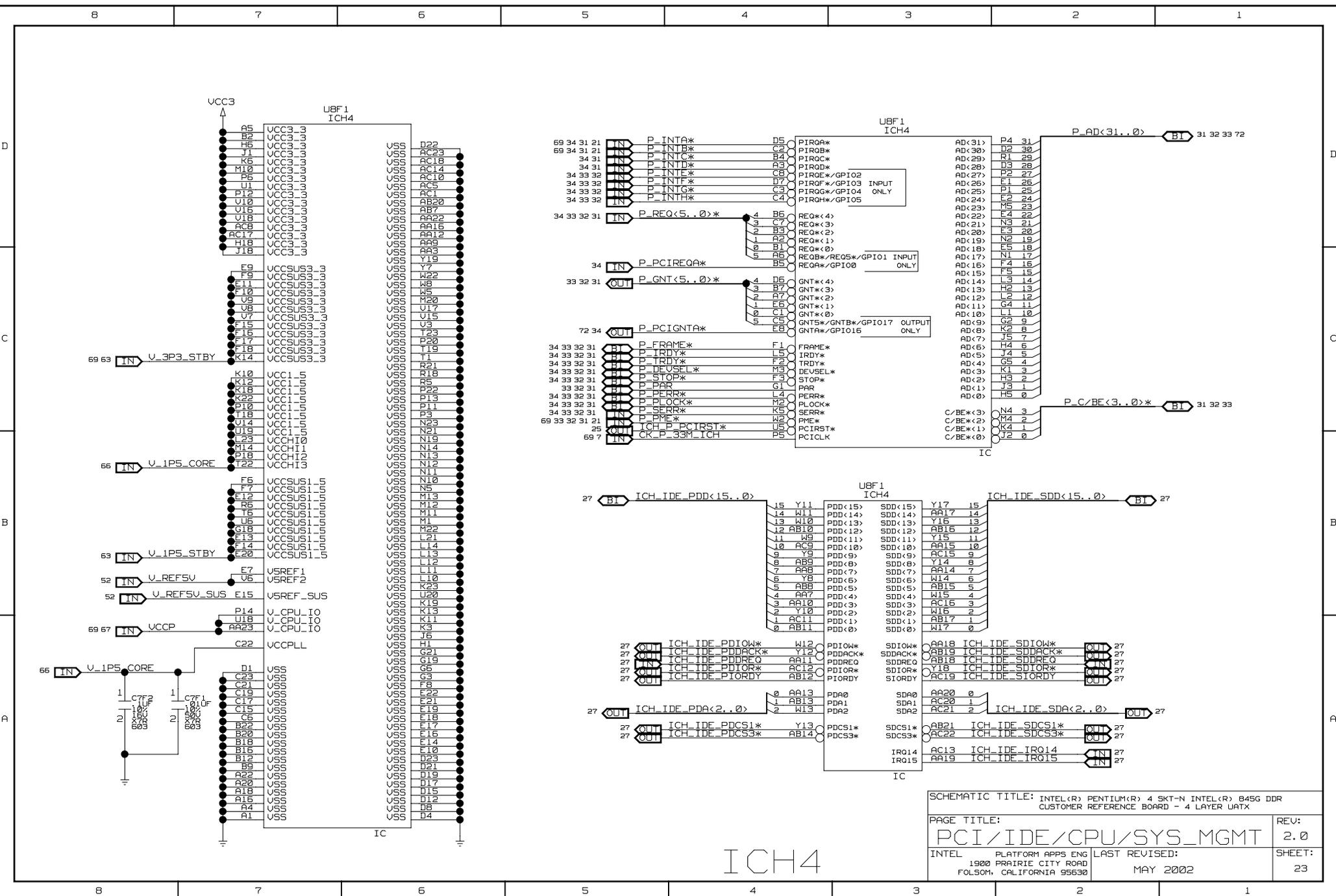
SPARES

1 RP4J2 2.2K 5% .063W 1C SM	3 RP4J2 2.2K 5% .063W 1C SM
----------------------------------------------	----------------------------------------------



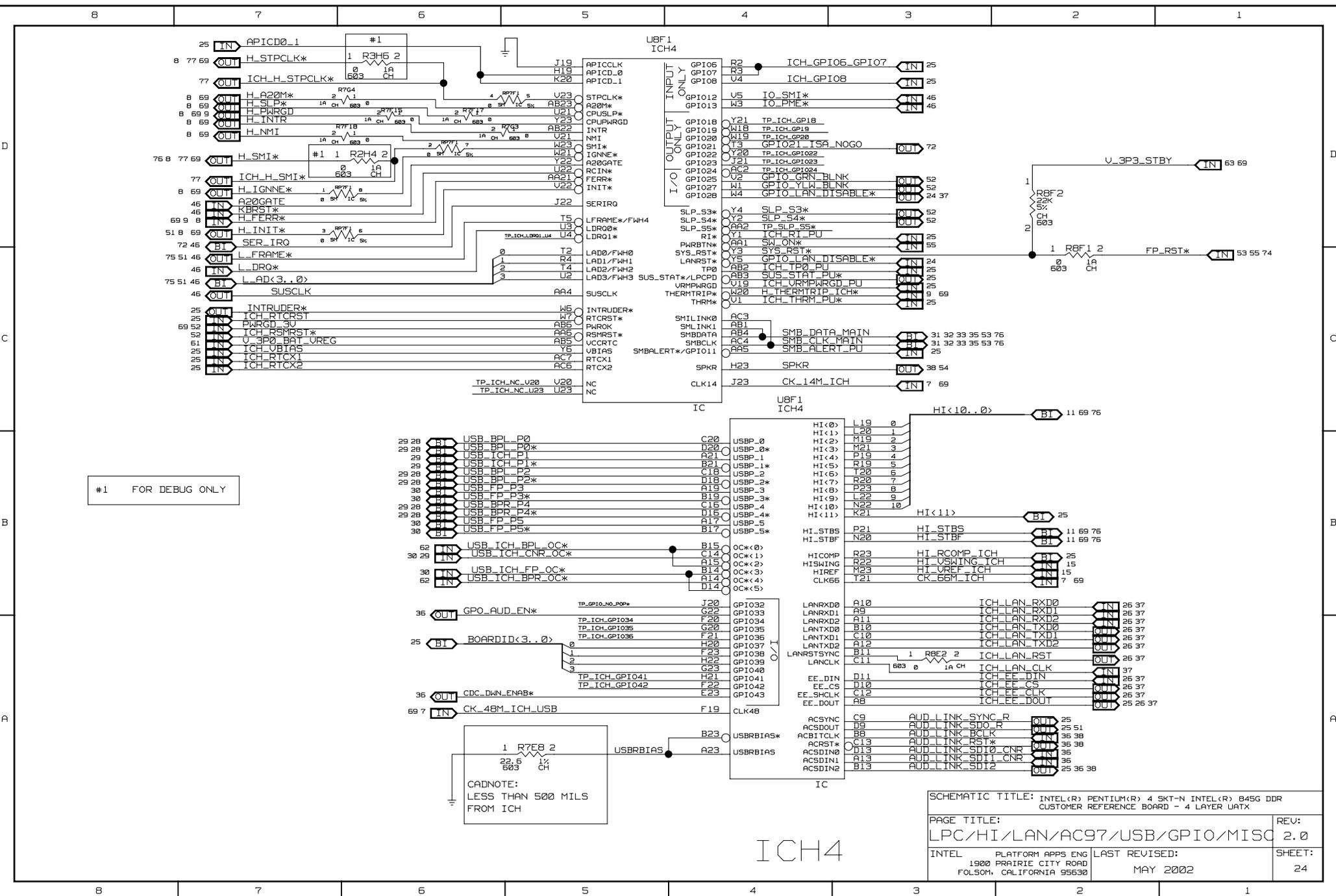
VGA CONNECTOR

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: VGA CONNECTOR	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002
	SHEET: 22

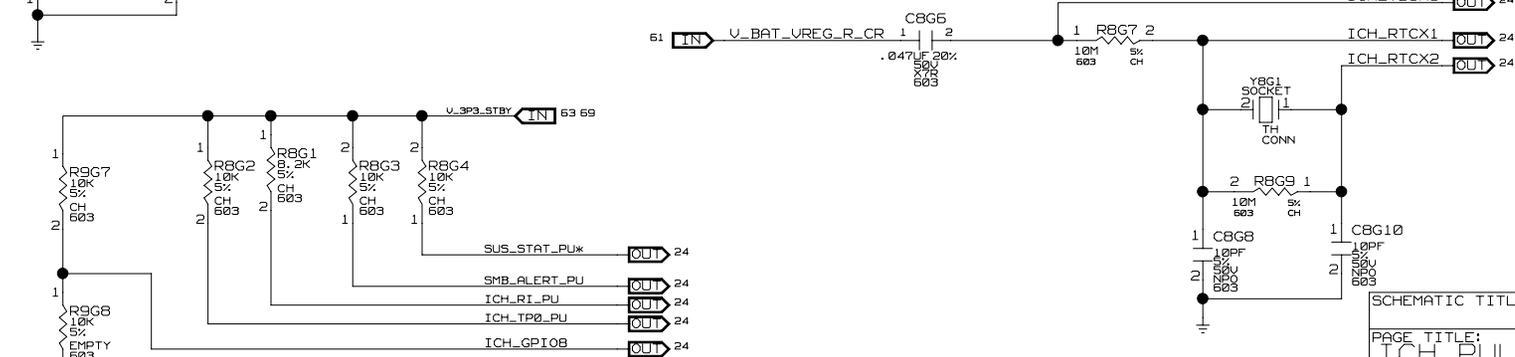
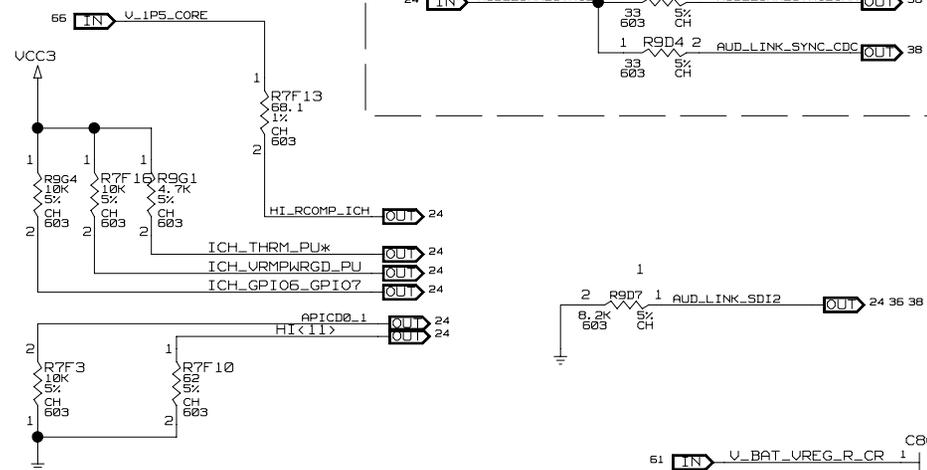
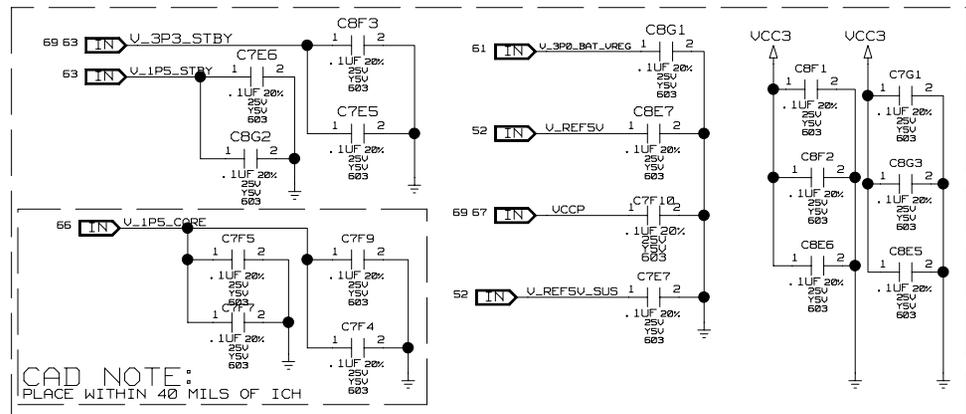
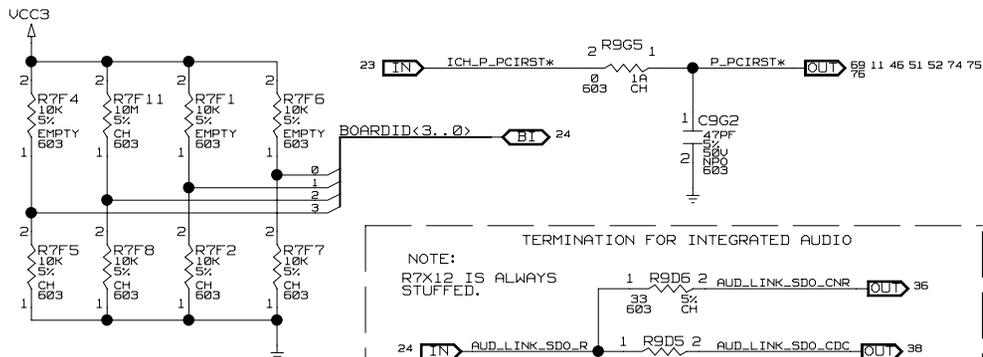


ICH4

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: PCI/IDE/CPU/SYS_MGMT		REV: 2.0
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 23



ICH4



ICH4

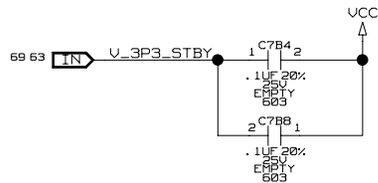
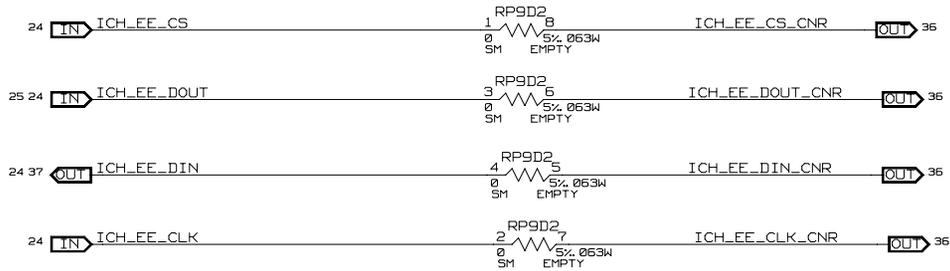
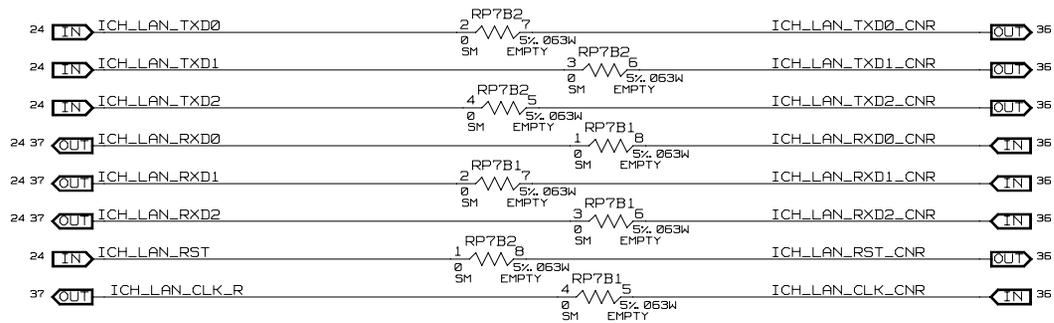
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		REV: 2.0
PAGE TITLE: ICH PULLUPS & DECOUPLING		SHEET: 25
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	

ICH AND CNR LINK

CAD NOTE:

PLACE THESE R-PACKS UNDERNEATH
THE LAN CHIP, RIGHT BY THE PINS TO
MINIMIZE STUB FROM PIN TO R-PACK

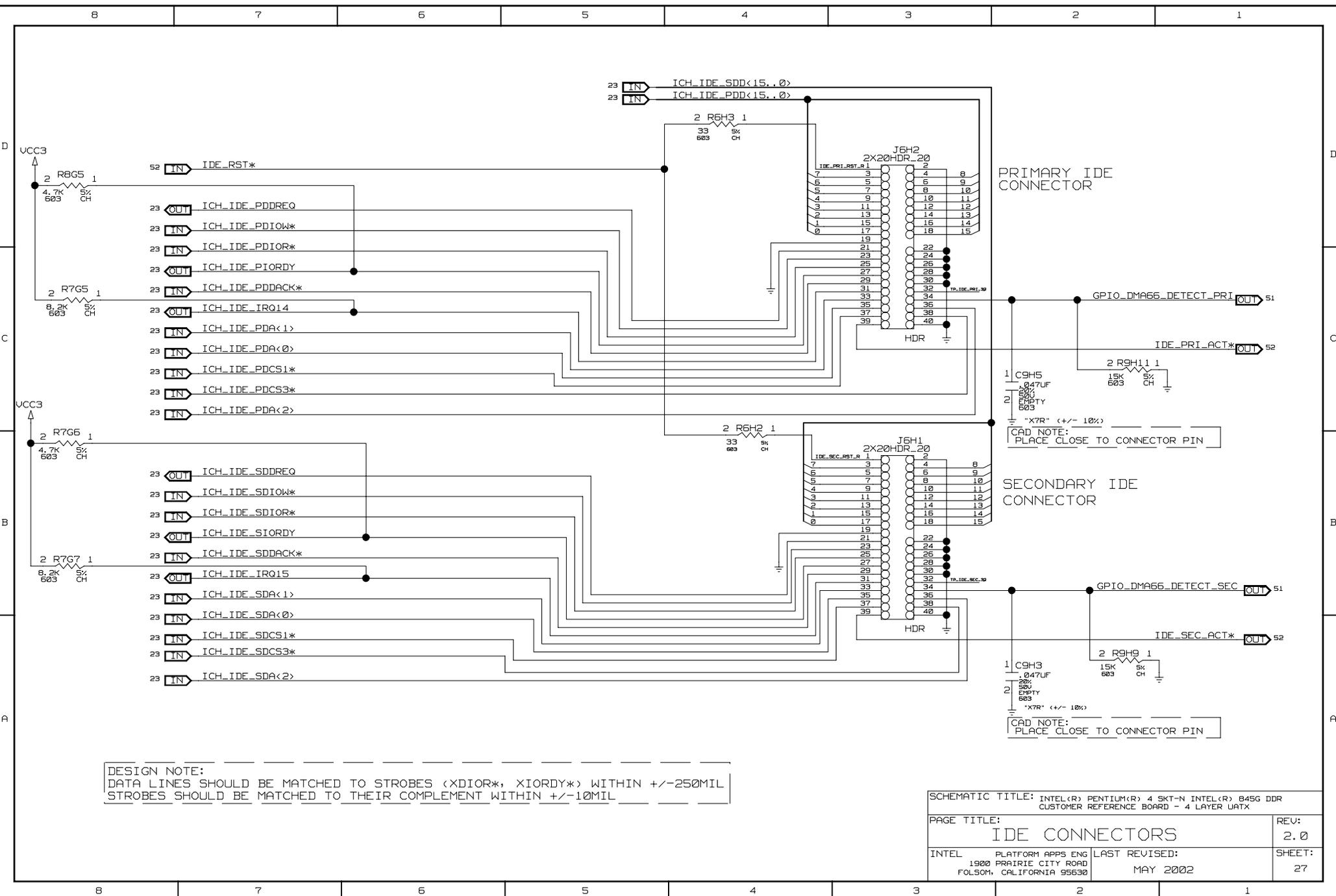
CNR OPTION FOR LAN-UP SOLUTION



0-OHMS ARE PROVIDED
TO MINIMIZE STUBS
ON LAN INTERFACE

ICH_360

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: ICH: CNR LAN LINK		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 25



DESIGN NOTE:
 DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR*, XIORDY*) WITHIN +/-250MIL
 STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/-10MIL

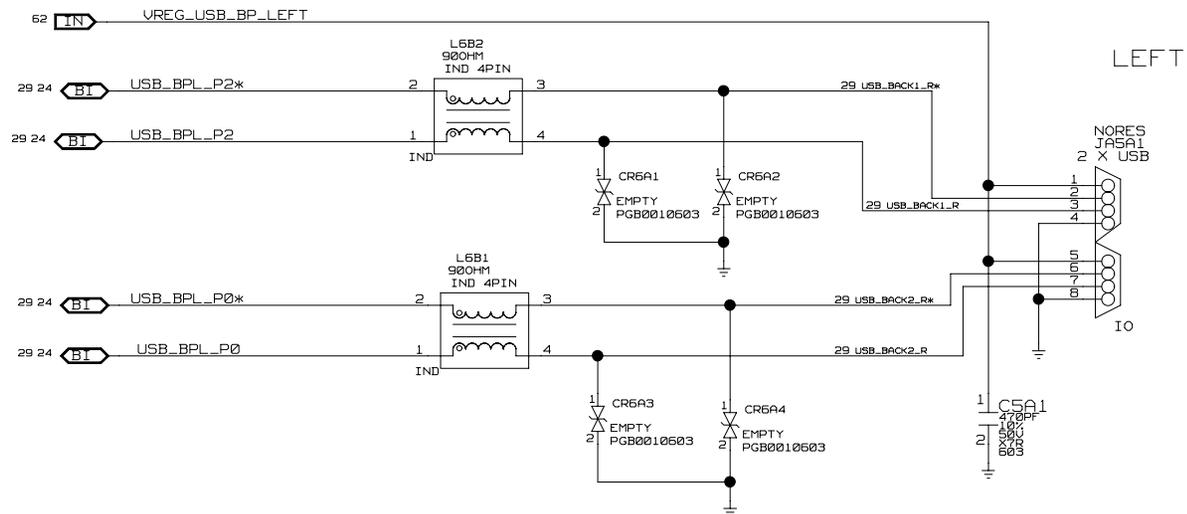
PRIMARY IDE CONNECTOR

SECONDARY IDE CONNECTOR

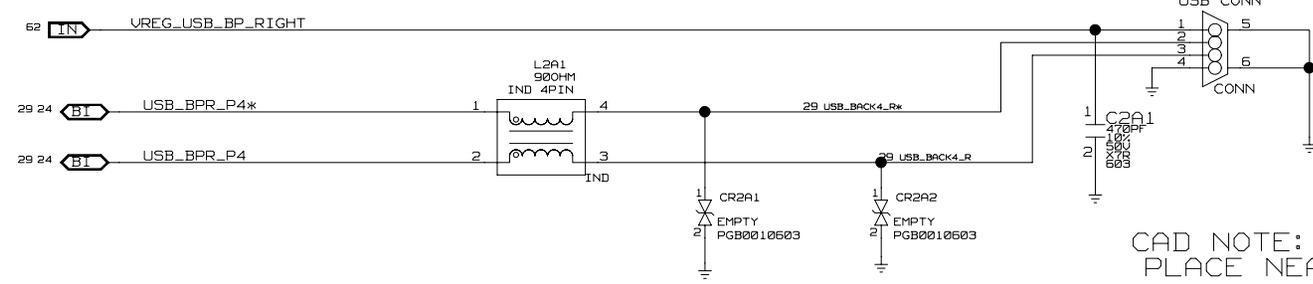
CAD NOTE:
 PLACE CLOSE TO CONNECTOR PIN

CAD NOTE:
 PLACE CLOSE TO CONNECTOR PIN

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX			
PAGE TITLE: IDE CONNECTORS			REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002		SHEET: 27



LEFT



RIGHT

CAD NOTE:
PLACE NEAR USB CONN

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: USB BACKPANEL		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 28

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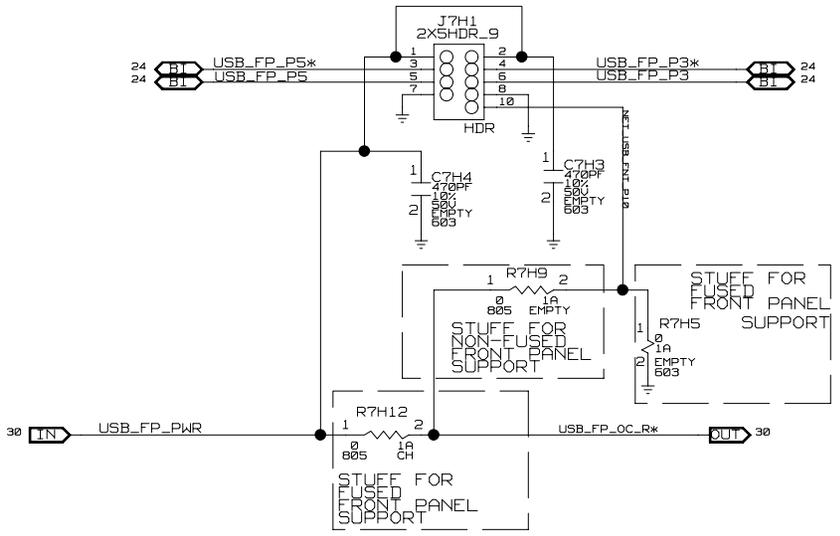
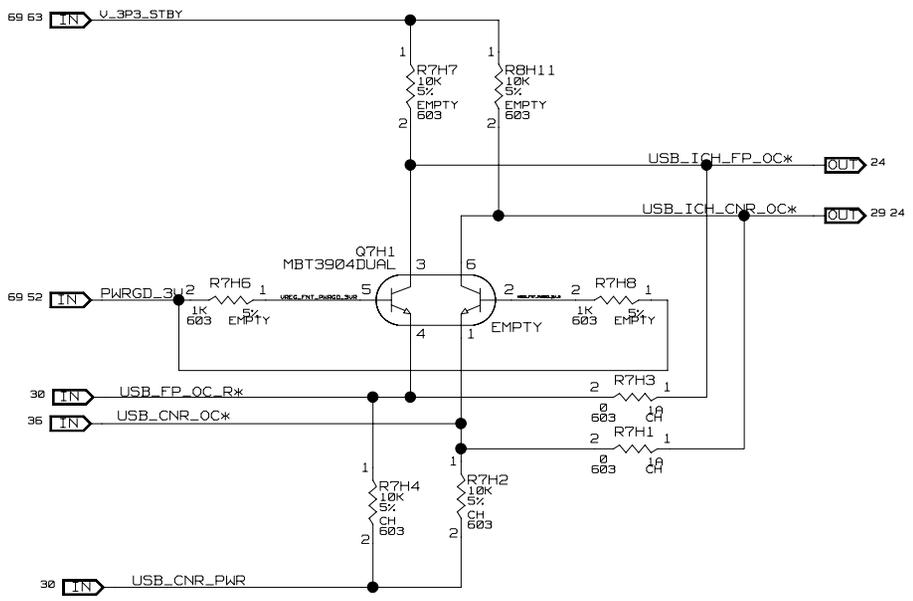
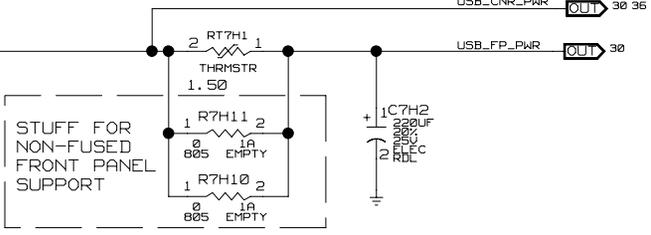
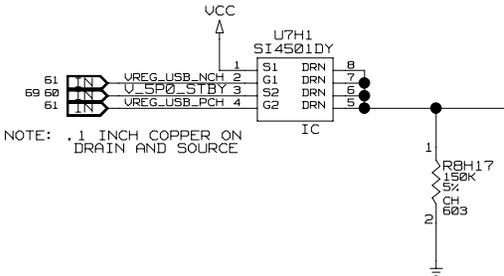
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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: BLANK		REV: 2.0
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG LAST REVISED: MAY 2002	SHEET: 29

8 7 6 5 4 3 2 1

CAD NOTE:
TRACE ROUTING IS 7.5 MIL, 7.5 MIL SPACING

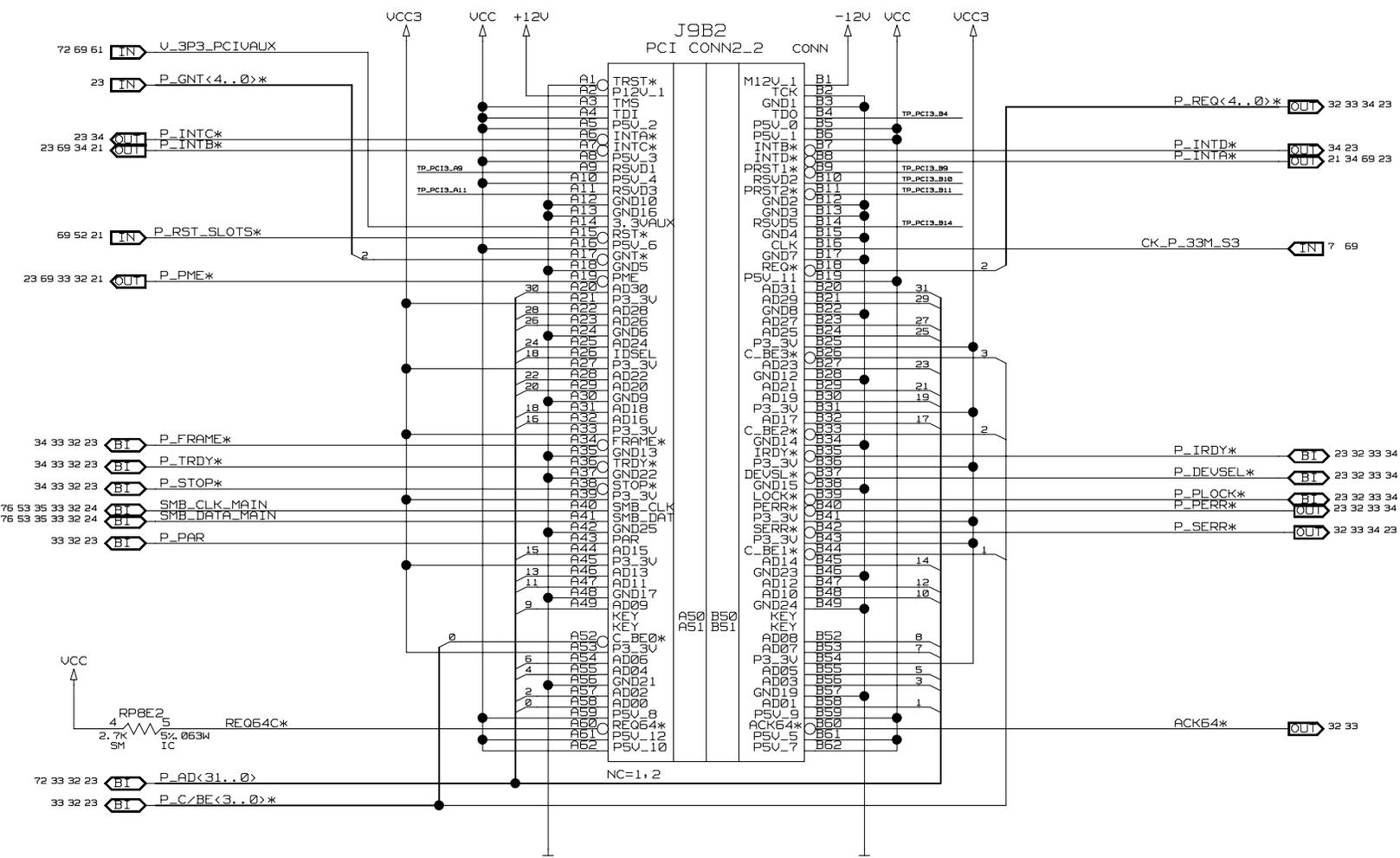
CAD NOTE: PLACE MIDWAY BETWEEN THE FPANEL (2X5) & CNR
RUN MUST HAVE 50 MIL POWER TO BOTH LOCATIONS.



USB FNT PANEL POWER

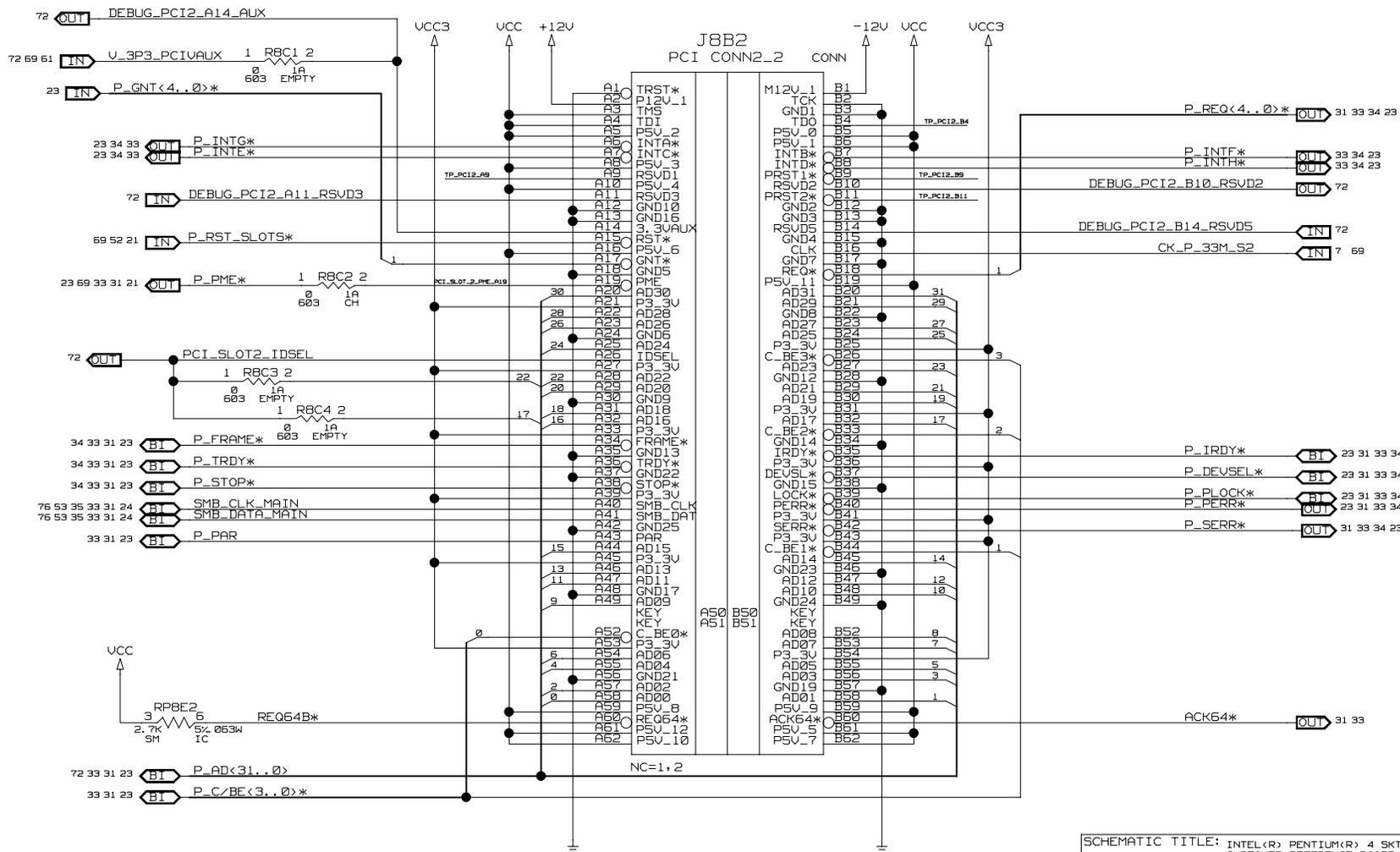
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: USB FRONT PANEL	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 30

PCI SLOT 3



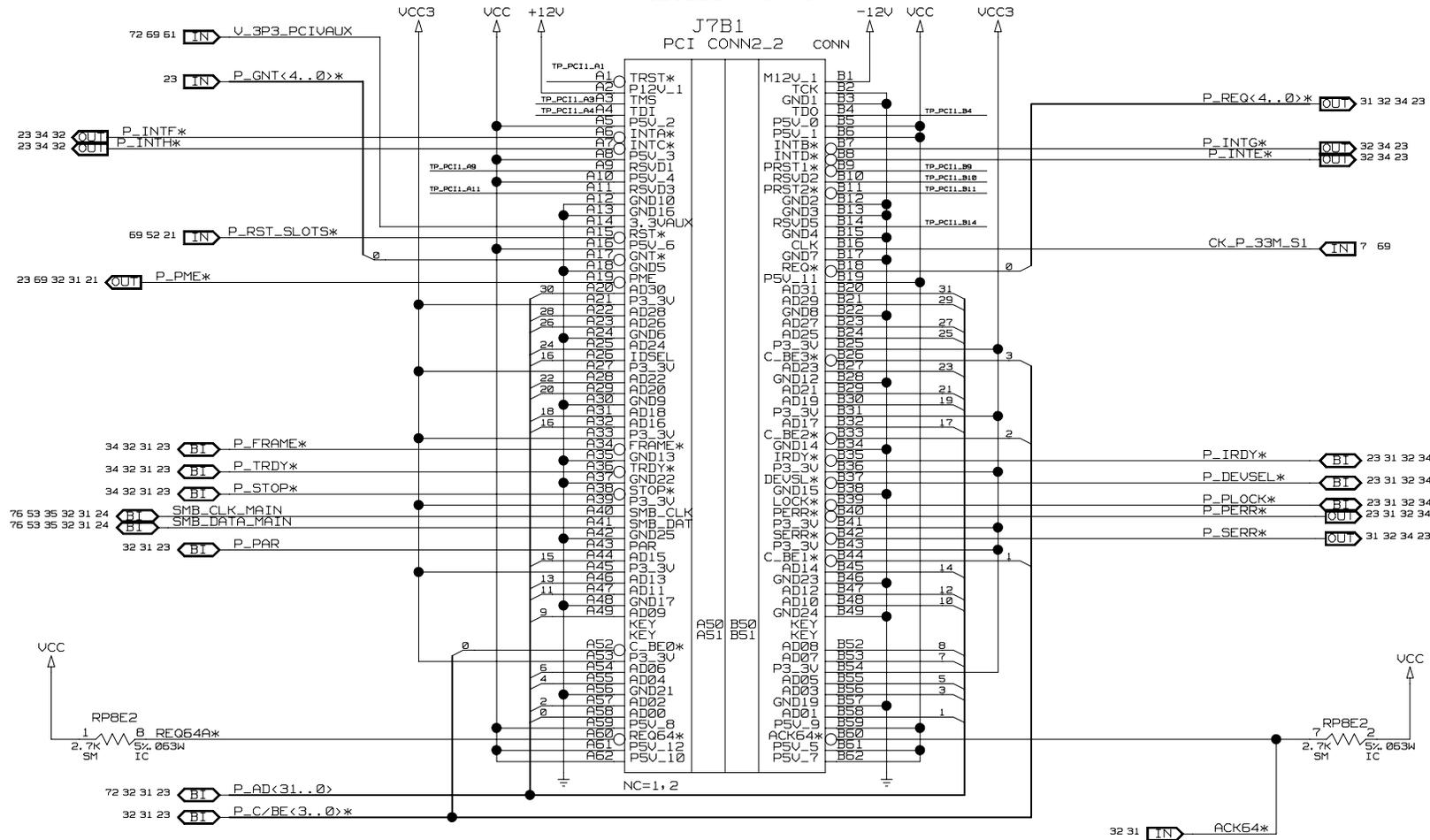
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: PCI SLOT 3	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002 SHEET: 31

PCI SLOT 2



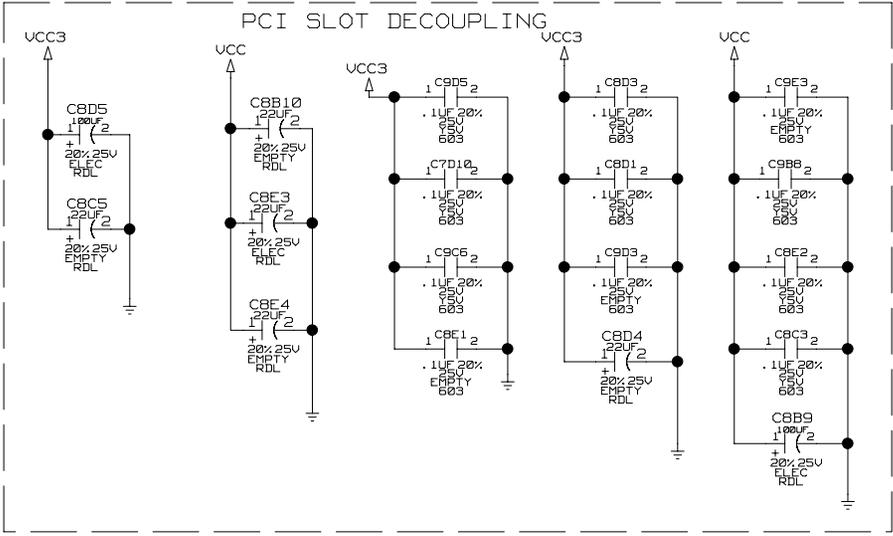
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: PCI SLOT 2	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002
	SHEET: 32

PCI SLOT 1
CLOSEST TO AGP

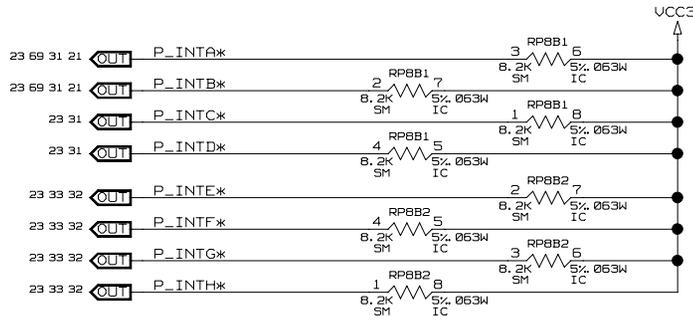
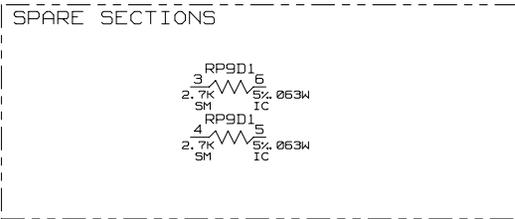
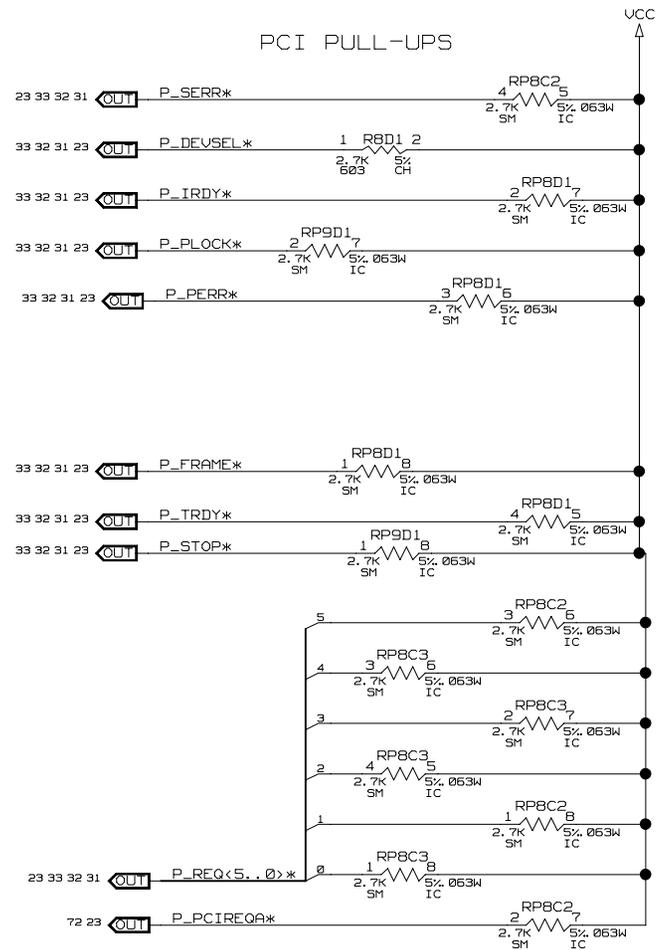


SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX			
PAGE TITLE: PCI SLOT 1			REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: MAY 2002	SHEET: 33

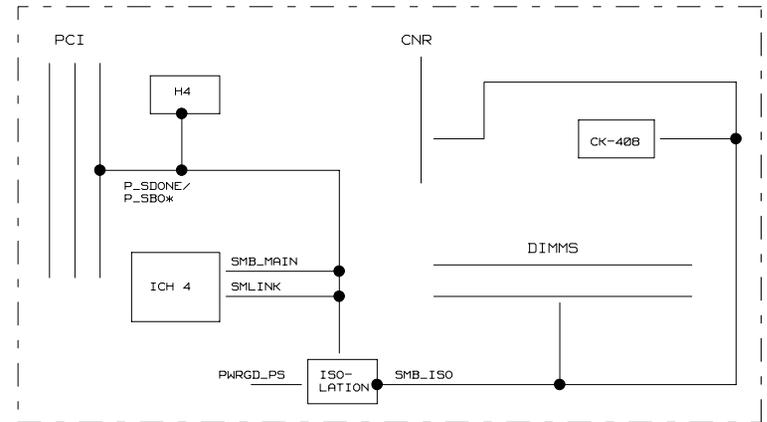
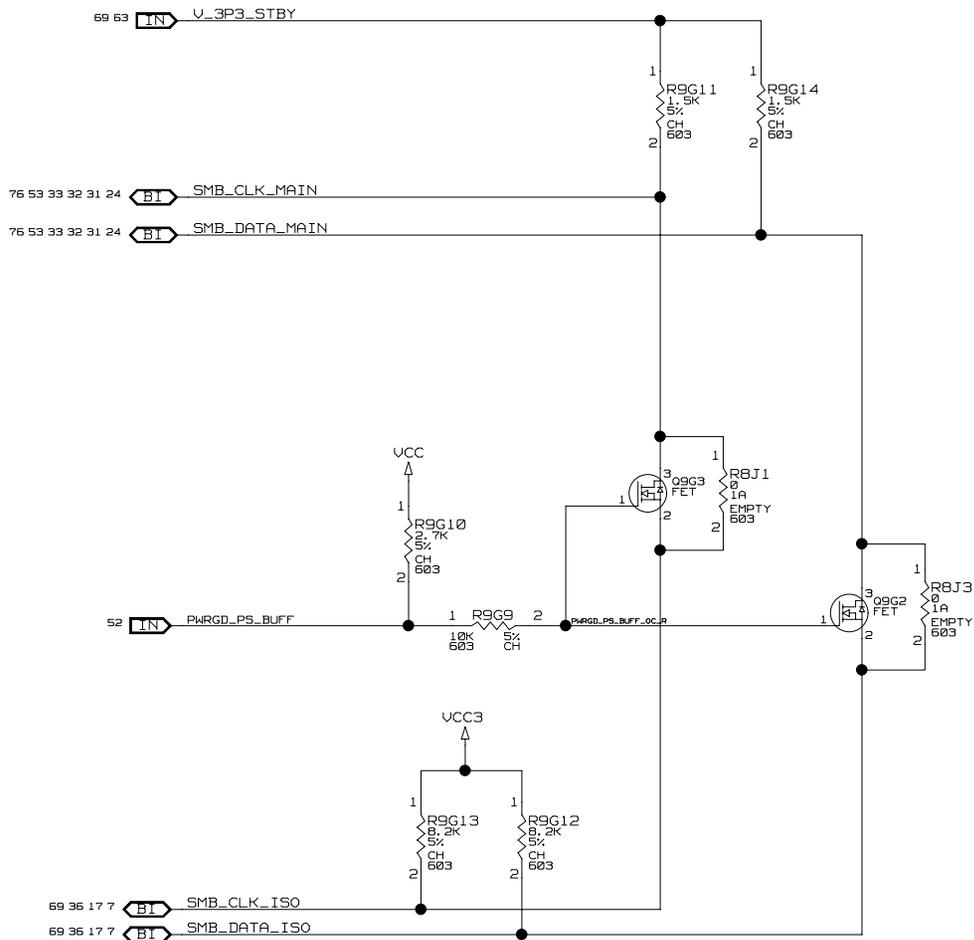
PCI SLOT DECOUPLING



PCI PULL-UPS



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: ICH PCI TERMINATION		REV: 2.0
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 34



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	SMBUS_ISOLATION	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 35

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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: BLANK
REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002
1900 PRAIRIE CITY ROAD SHEET: 37
FOLSOM, CALIFORNIA 95630

8

7

6

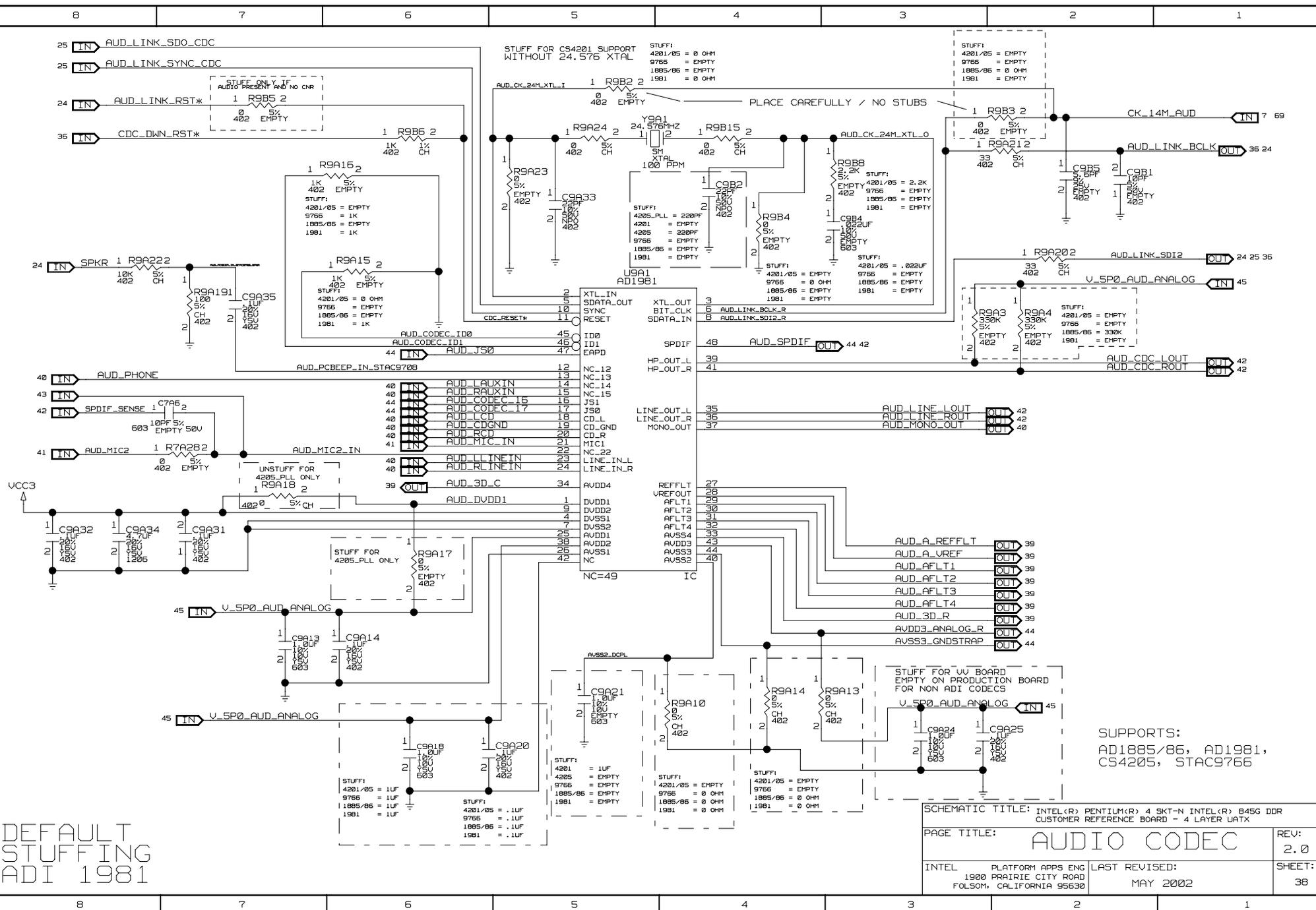
5

4

3

2

1

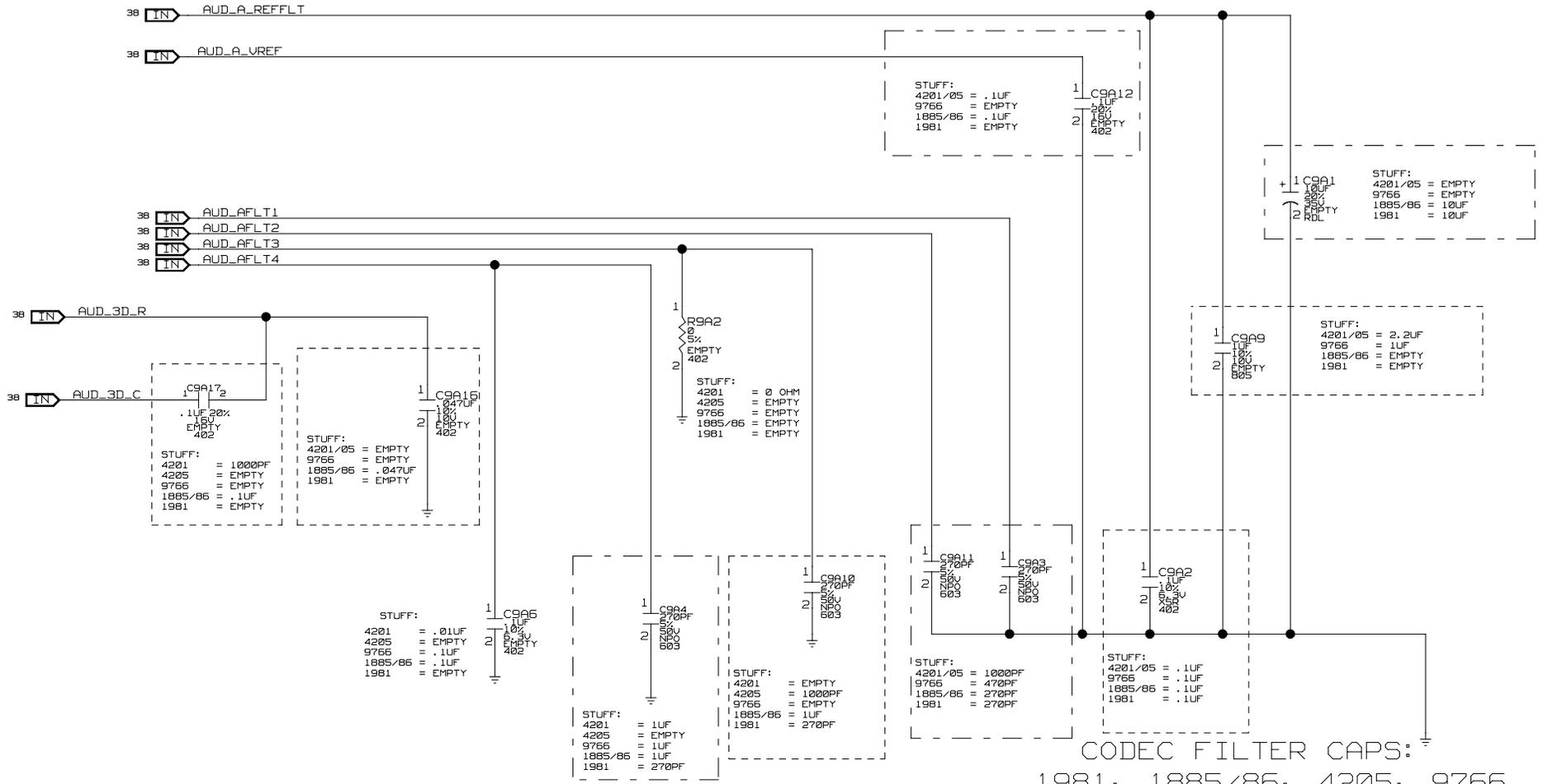


DEFAULT
STUFFING
ADI 1981

SUPPORTS:
AD1885/86, AD1981,
CS4205, STAC9766

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		REV: 2.0
PAGE TITLE: AUDIO CODEC	LAST REVISED: MAY 2002	SHEET: 38
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		

KEEP CAPS AS CLOSE
AS POSSIBLE TO AC97
CODEC.

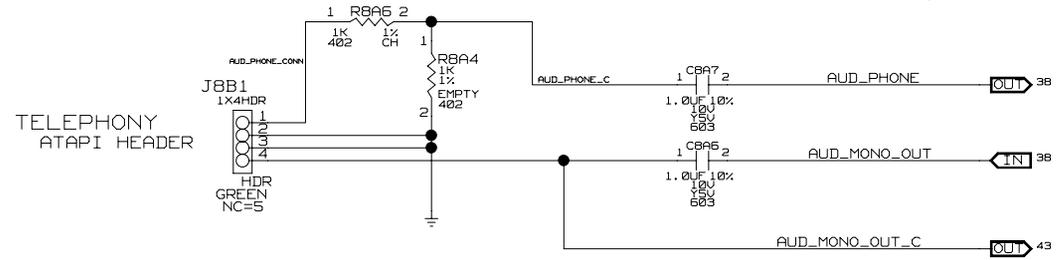
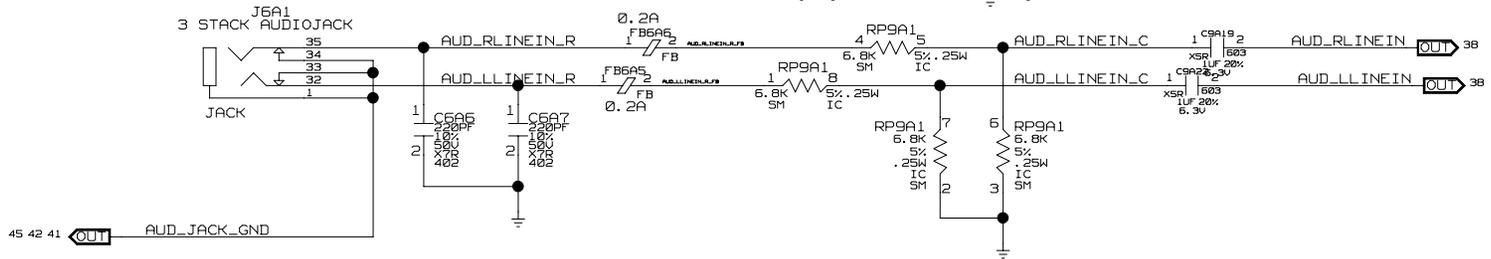
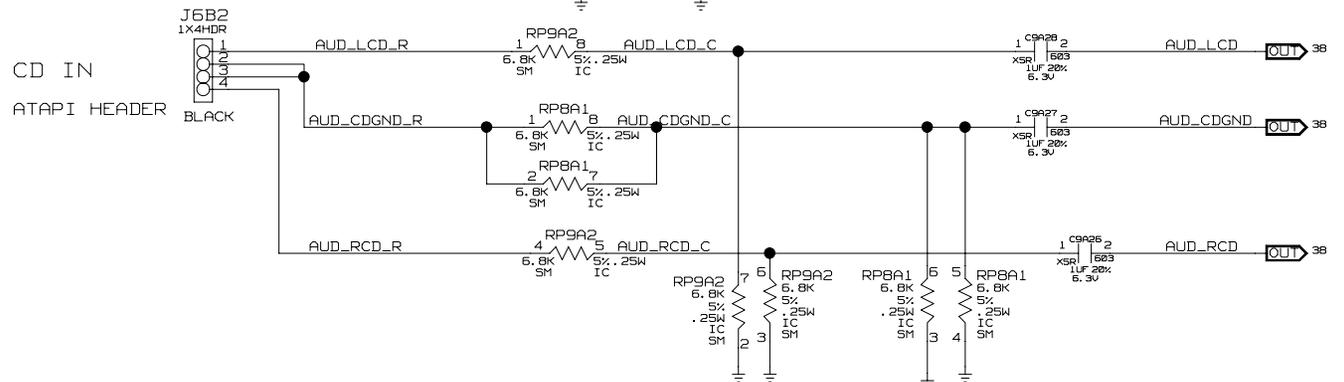
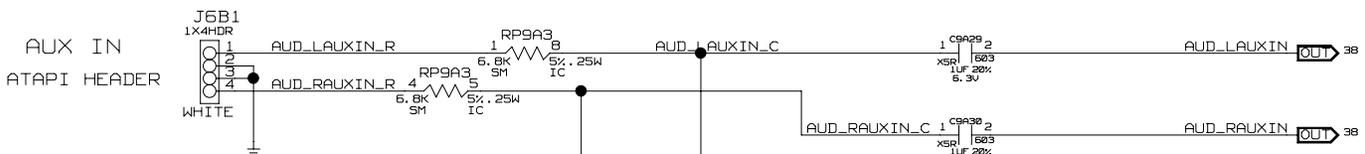


CODEC FILTER CAPS:
1981, 1885/86, 4205, 9766

DEFAULT
STUFFING
ADI 1981

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: AUDIO CODEC FILTERING CAPS	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002
	SHEET: 39

8 7 6 5 4 3 2 1



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: **AUDIO ATAPI HEADERS** REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002 SHEET: 40

1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

D

C

B

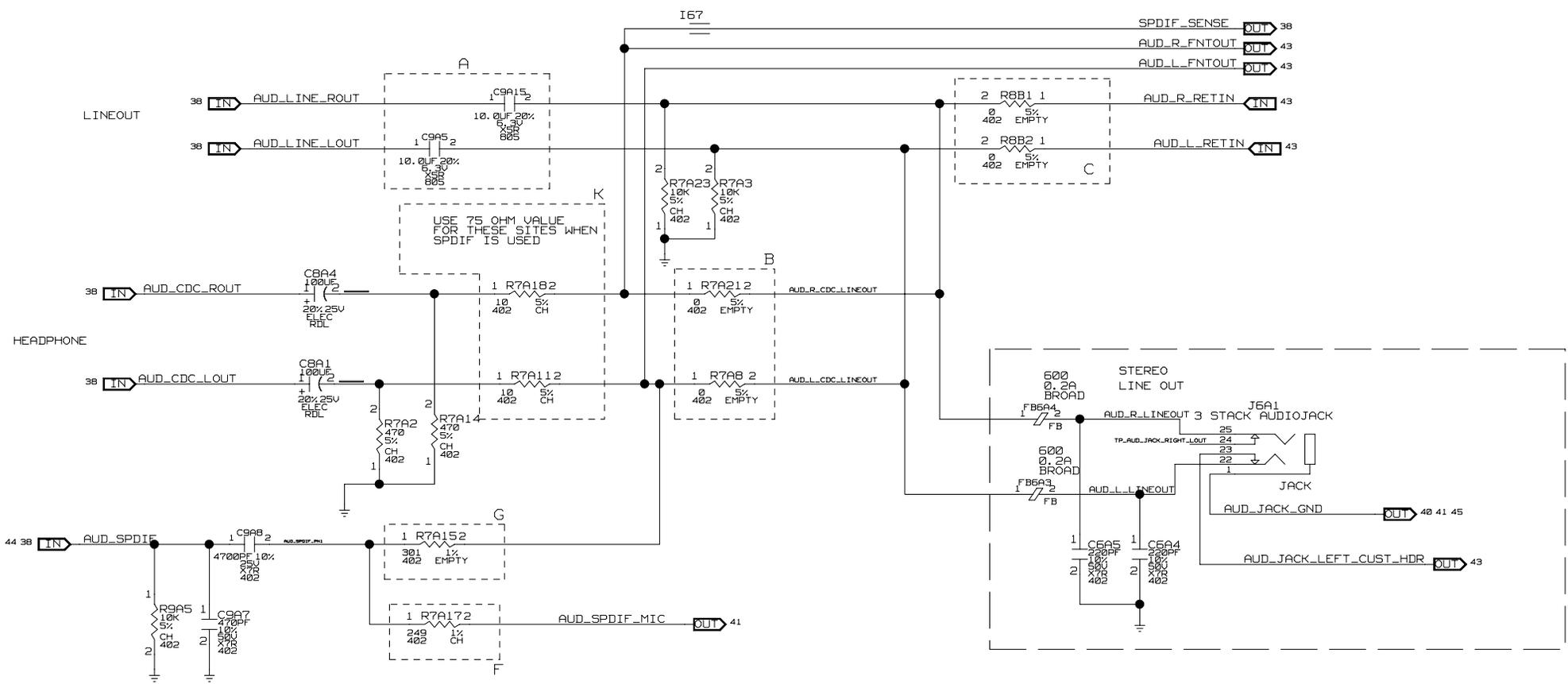
A

D

C

B

A



	BP ONLY	FP-->BP	SPDIF	BP LO	BP MIC
HEADPHONE	STUFF B	STUFF C	F	EMPTY	STUFF
	EMPTY A, C	EMPTY A, B	G	STUFF	EMPTY
LINEOUT	STUFF A	N/A	H	EMPTY	110 OHM
	EMPTY B, C		J	STUFF	EMPTY
			K	75 OHM	10 OHM

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: AUDIO: LINE-OUT

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002

1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

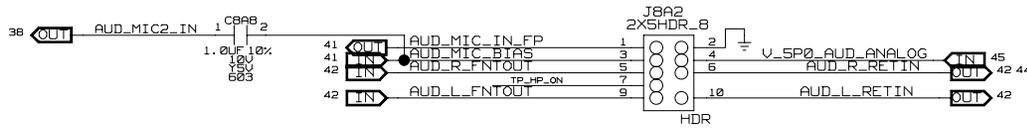
REV: 2.0

SHEET: 42

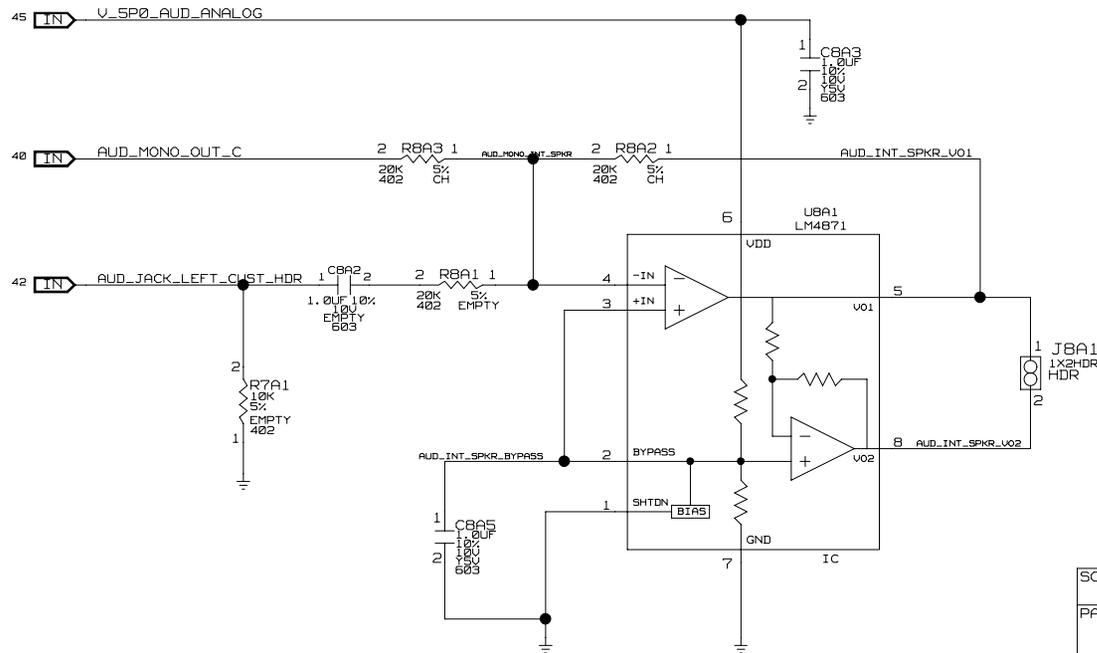
8 7 6 5 4 3 2 1

NOTE:
 FP DONGLE MUST HAVE
 MIC JACK RING SHUNT SPRING
 TERMINAL CONNECTED
 TO GND FOR PROPER
 MIC SENSING OPERATION

AUDIO FRONT PANEL
 PLACE NEAR AUDIO CIRCUIT



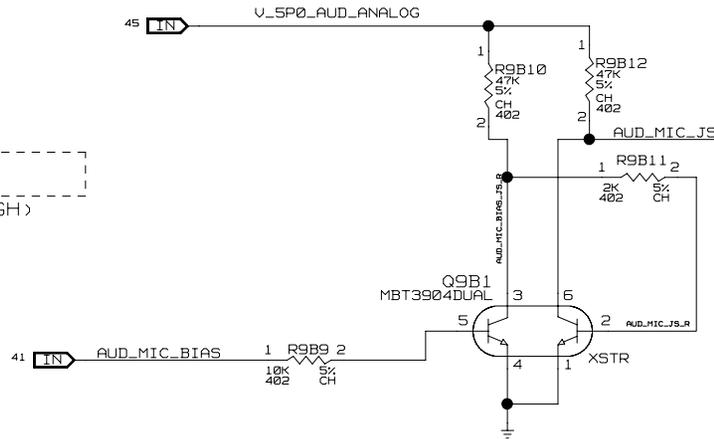
INTERNAL SPEAKER CIRCUIT



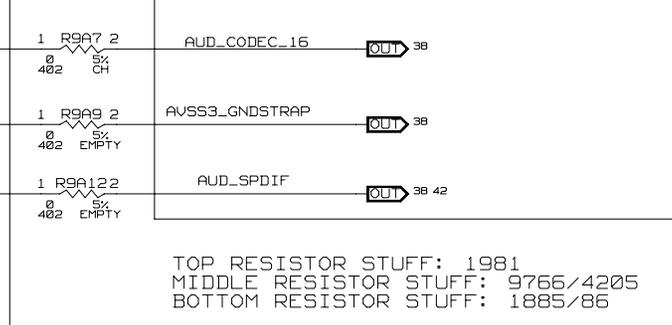
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PAGE TITLE: AUDIO_FRONT_PANEL		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 43

MIC JACK SENSE

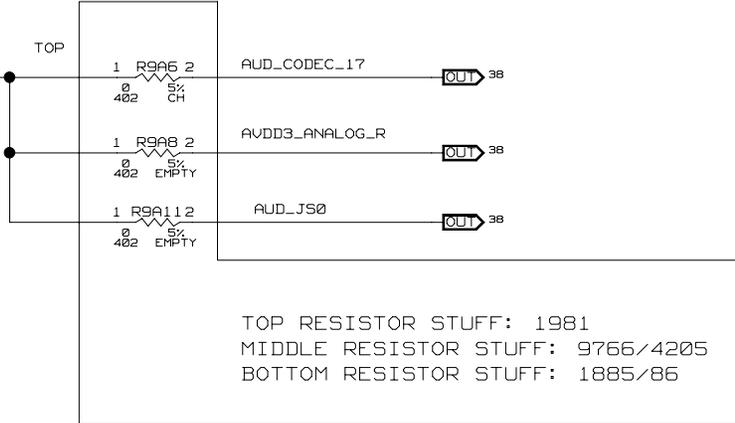
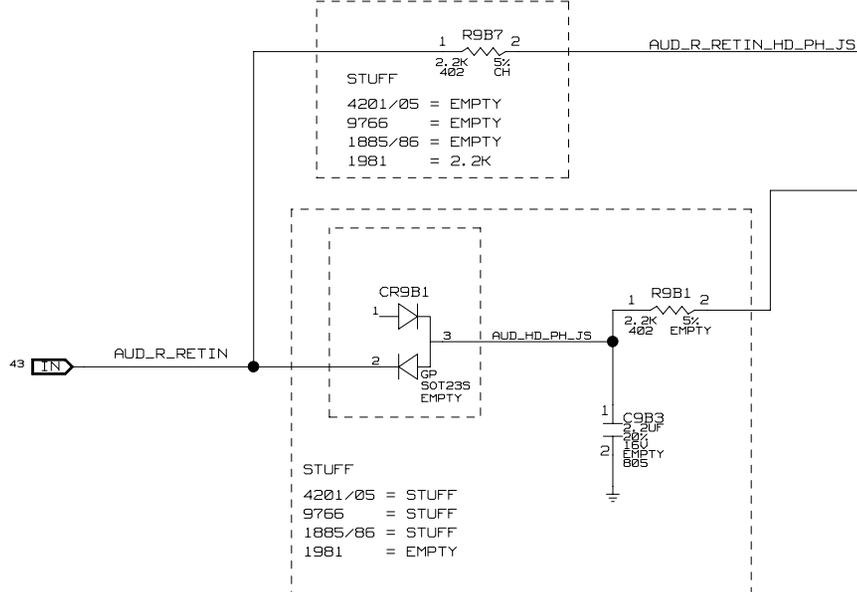
FP DONGLE MUST HAVE
MIC JACK RING SHUNT SPRING
TERMINAL CONNECTED
TO GND FOR PROPER
MIC SENSING OPERATION



NOT CONNECTED
4205: 43, 44, 41, 40, 39
1981: 16, 17 (ACTIVE HIGH)
9766: 43, 44
4291: NONE
1885/86: 47, 48



HEADPHONE JACK SENSE

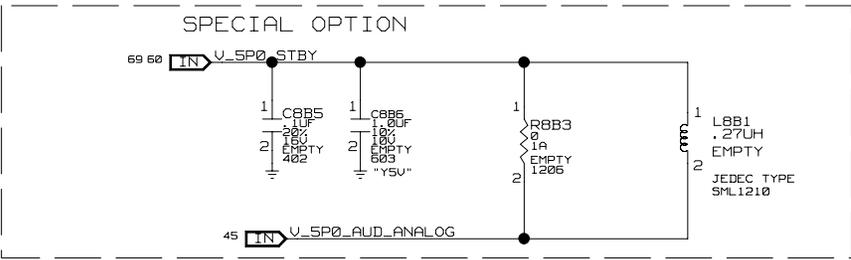


DEFAULT
STUFFING
ADI 1981

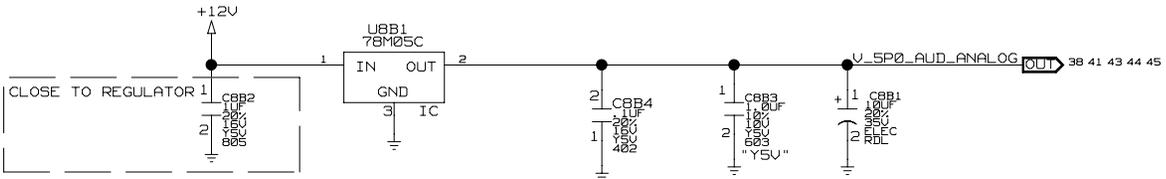
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: JACK SENSE REV: 2.0

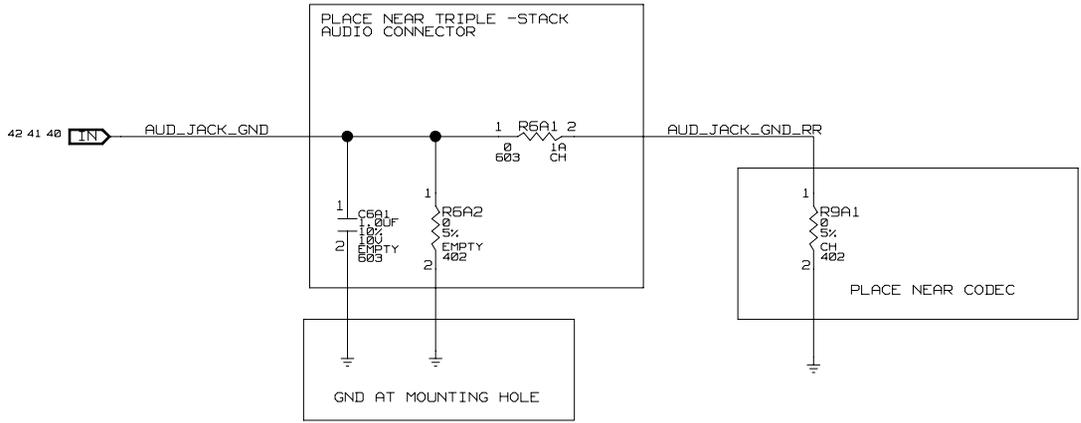
INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002 SHEET: 44
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630



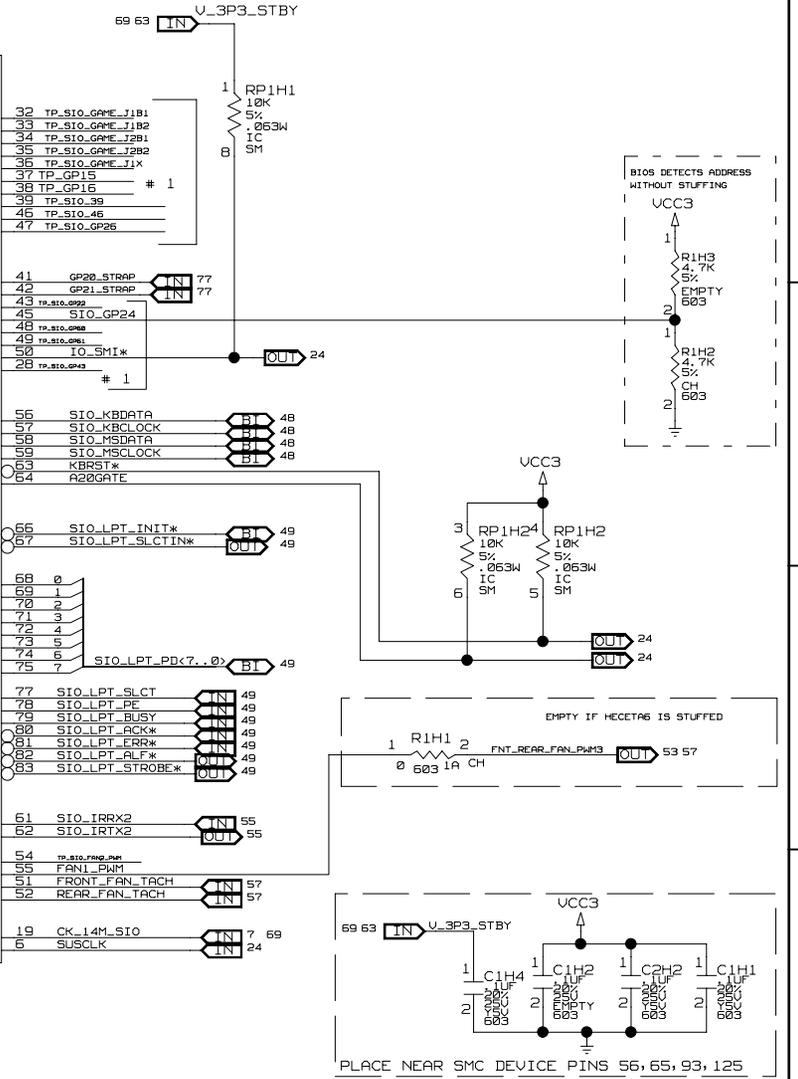
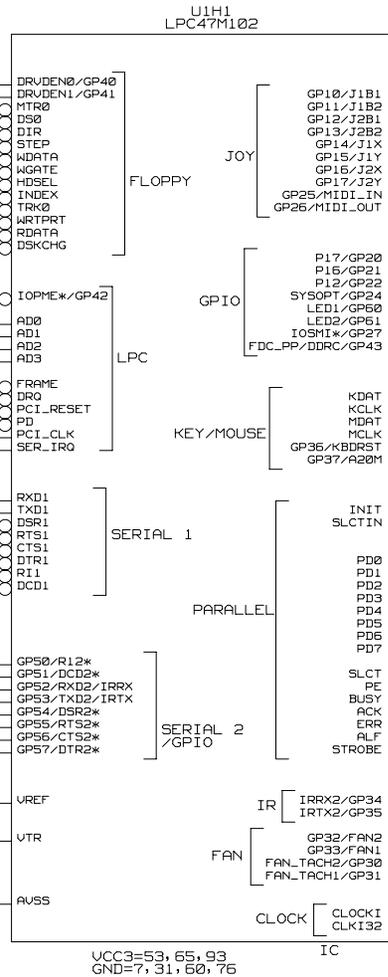
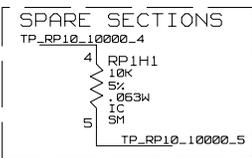
REGULATOR THERMAL TAB SHOULD BE SOLDERED TO A COPPER PAD THAT IS LARGE ENOUGH TO ALLOW 5 TO 10 GROUND VIAS AROUND THE COMPONENT FOR COOLING



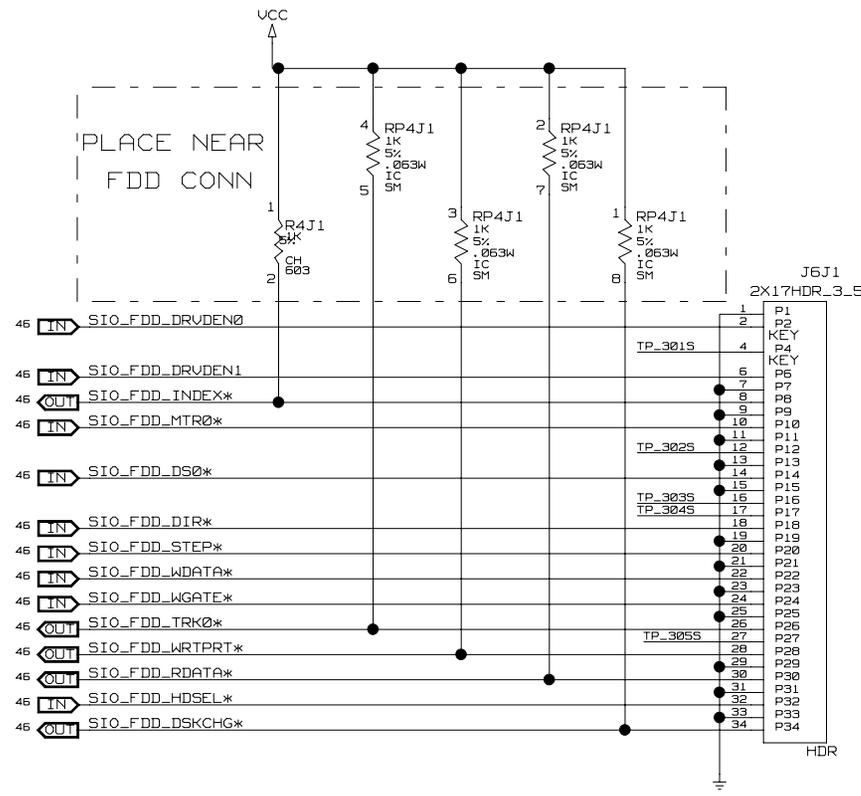
NOTE:
LAYOUT SHOULD GO FROM PIN 2 TO CAPS AND THEN THROUGH SEVERAL VIAS TO U_SP0_AUD_ANALOG



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: AUDIO VREG	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002
	SHEET: 45



NOTE: #1
 BIOS TO PROGRAM THESE
 GPIO'S AS OUTPUTS



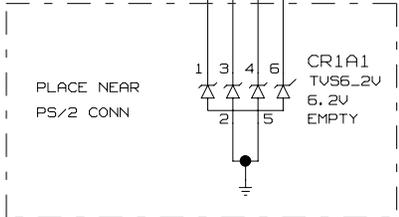
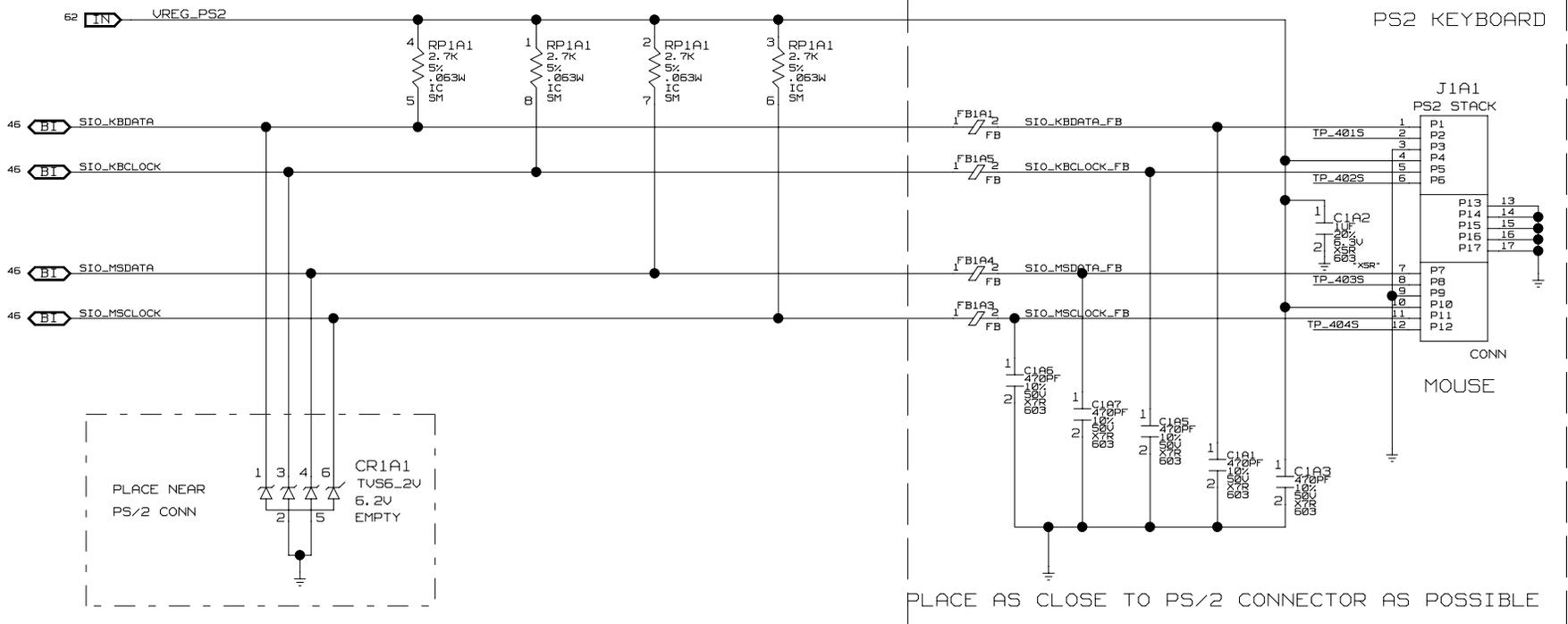
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: FLOPPY CONNECTOR

REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002 SHEET: 47

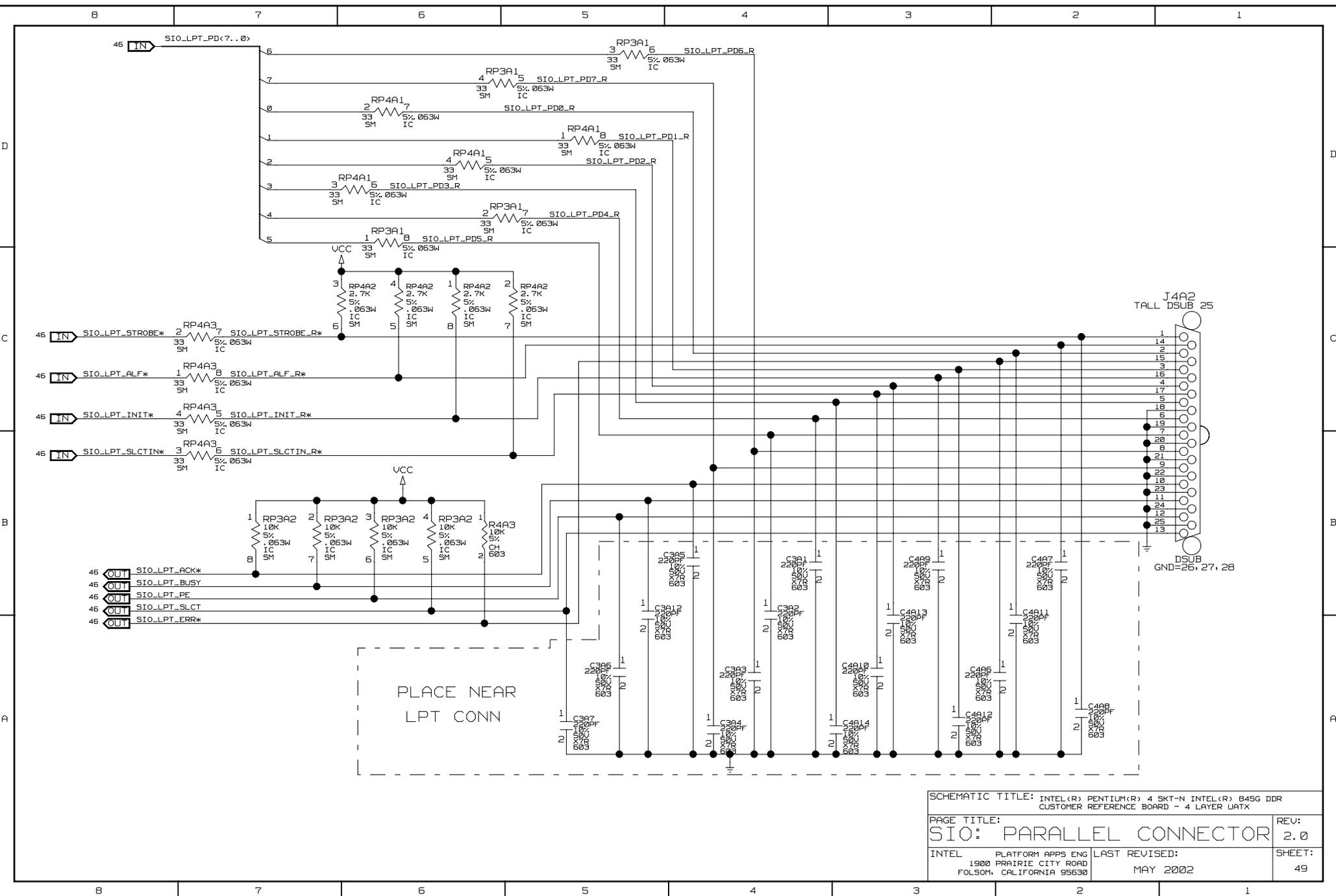
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630



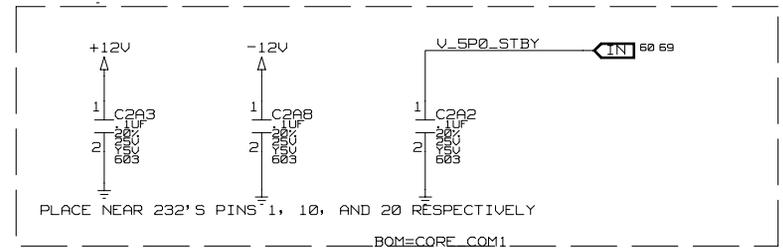
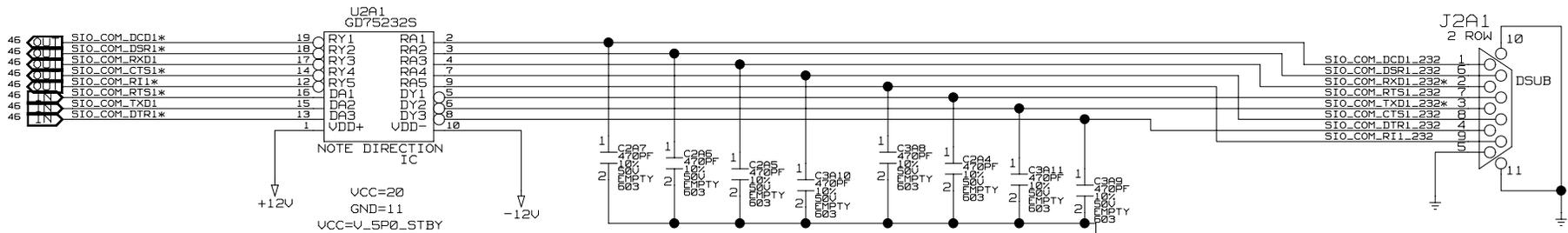
PLACE AS CLOSE TO PS/2 CONNECTOR AS POSSIBLE

ATX DOUBLE-STACKED

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: SIO: KEYBOARD/MOUSE		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 48



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR
 CUSTOMER REFERENCE BOARD - 4 LAYER UATX
 PAGE TITLE: SIO: PARALLEL CONNECTOR
 REV: 2.0
 INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002 SHEET: 49
 1900 PRAIRIE CITY ROAD
 FOLSOM, CALIFORNIA 95630



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: SERIAL CONNECTOR REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: SHEET: 50
1900 PRAIRIE CITY ROAD MAY 2002

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

CONFIGURE= SAFE MODE

8 7 6 5 4 3 2 1

D

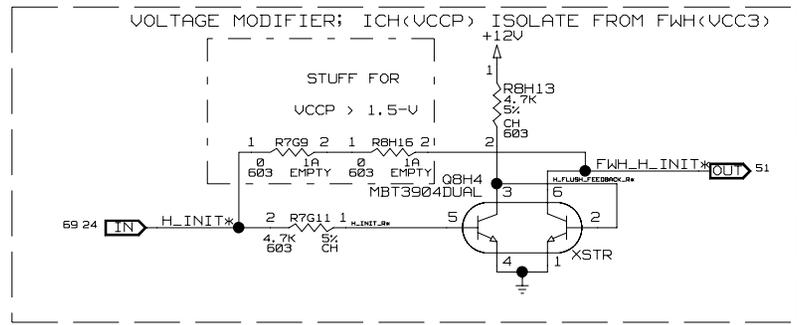
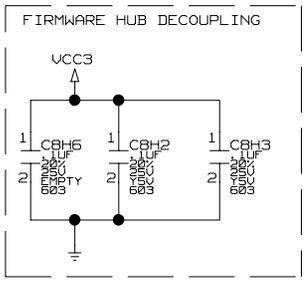
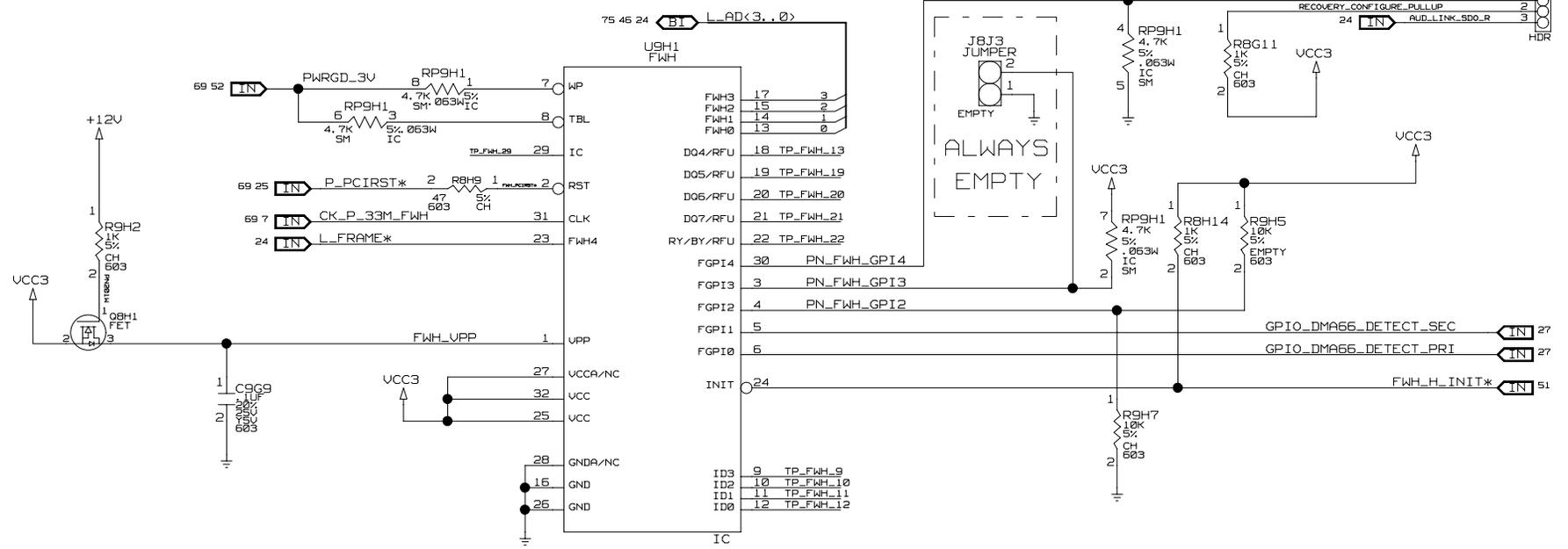
C

B

A

8 7 6 5 4 3 2 1

D C B A

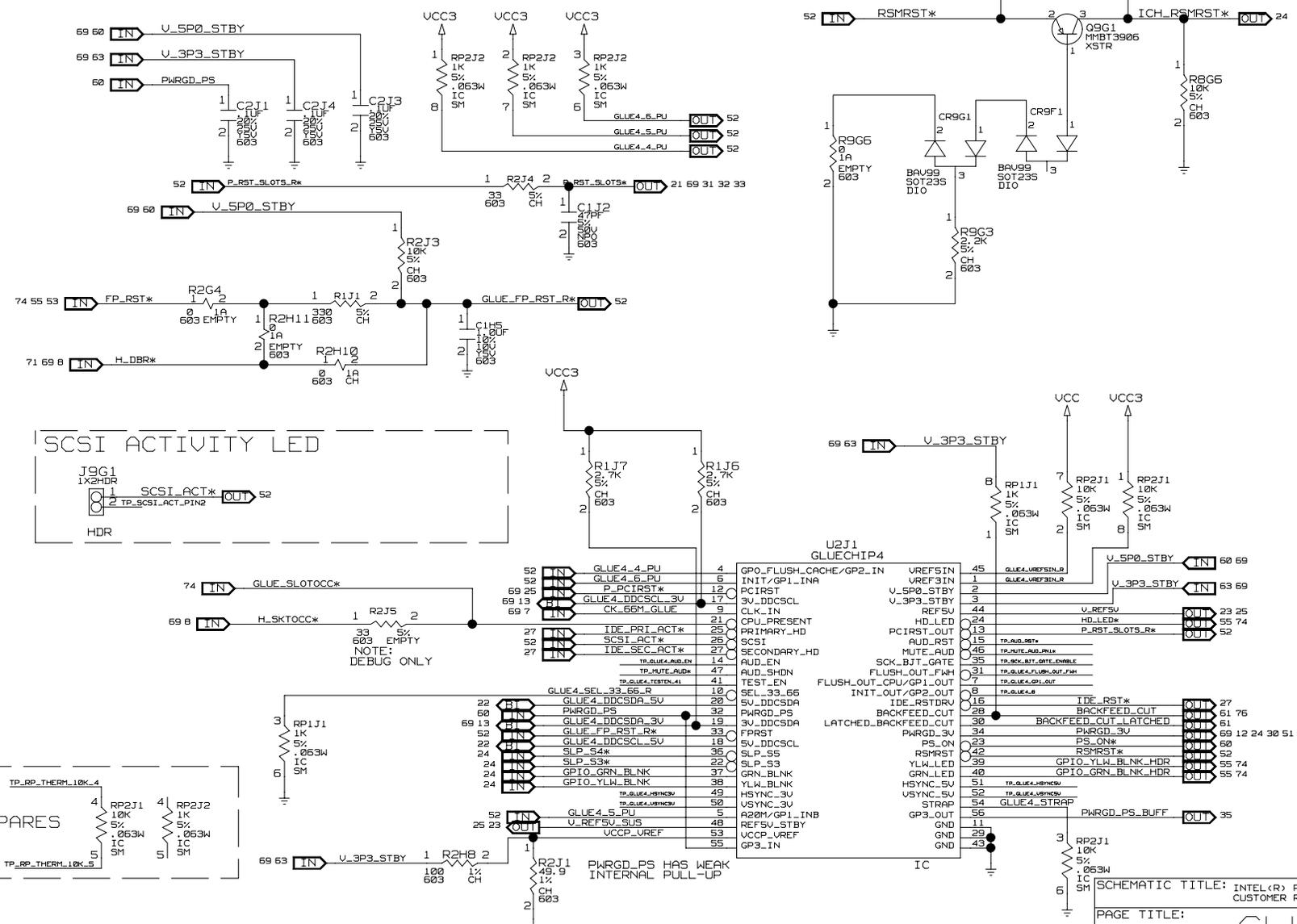


SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	FIRMWARE HUB	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 51

GLUECHIP4

GLUE4 INPUTS

PIN	FUNCTION	TYPE
1	VREF3IN	3I
2	5VSB	PI
3	3VSB	PI
4	GP2_IN	3IU
5	GP1_INB	UCCP REF
6	GP1_INA	UCCP REF
9	CLK_IN	3I
10	SEL_33_66	3IU
12	PCIRST*	3I
14	AUD_EN	3IU
17	3V_DDCSCL	3IOD
18	5V_DDCSCL	3IOD
19	3V_DDCSDA	3IOD
20	5V_DDCSDA	3IOD
21	CPU_PRESENT*	3IU
22	SLP_S3*	3I
25	PRIMARY_HDM*	5IU
26	SCSI*	5IU
27	SECONDARY_HDM*	5IU
32	PWRGD_PS	5IU
33	FPRST*	5IU
36	SLP_S5*	3I
37	GRN_BLNK	3IU
38	YLW_BLNK	3IU
41	TEST_EN	5ID
45	VREF5IN	5I
46	MUTE_AUD*	3IU
49	HSYNCH_3V	3I
50	VSYNCH_3V	3I
53	UCCP_VREF	AI
54	STRAP	3IU
55	GP3_IN	5I



U2J1 GLUECHIP4

45	GLUE4_VREF3IN_B	45	UREF5IN
1	GLUE4_VREF3IN_L	1	UREF3IN
2		2	V_5P0_STBY
3		3	V_3P3_STBY
44		44	REF5V
24		24	HD_LED
13		13	HD_LED*
15		15	AUD_RST
46		46	MUTE_AUD
35		35	SKC_BTT_GATE
31		31	TP_GLUE4_FLUSH_OUT_PWRH
7		7	TP_GLUE4_OUT_07
8		8	TP_GLUE4_8
16		16	IDE_RST*
28		28	BACKFEED_CUT
30		30	BACKFEED_CUT_LATCHED
34		34	PWRGD_3V
23		23	PS_ON*
42		42	RSMRST*
39		39	YLN_LED
40		40	GRN_LED
51		51	TP_GLUE4_HSYNCSU
52		52	TP_GLUE4_VSYNCSU
54		54	GLUE4_STRAP
11		11	GP3_OUT
29		29	GND
43		43	GND

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: **GLUE4**

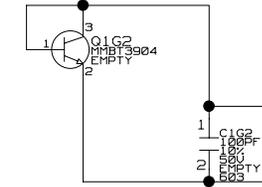
REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002 SHEET: 52

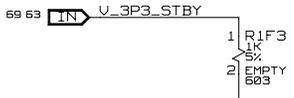
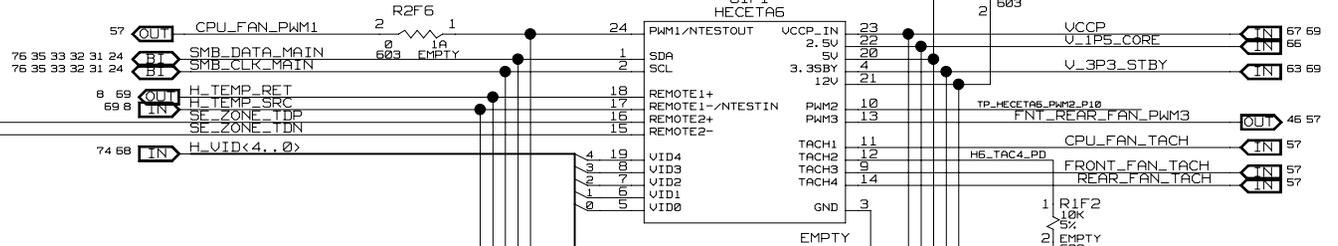
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

CAD NOTE:
SOUTHEAST THERMAL ZONE SENSOR
PLACE BELOW DIMMS

CAD NOTE:
10MIL TRACE ON SE_ZONE_TDN AND _TDP



ALL STUFFED IF HECETA6
ALL EMPTY IF HECETA4

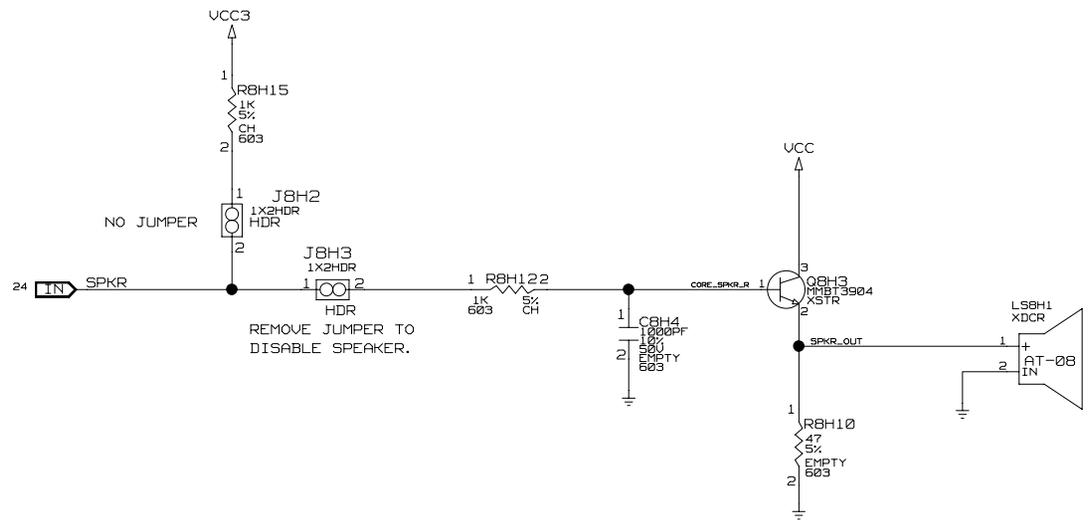


ALL STUFFED IF HECETA4
ALL EMPTY IF HECETA6

HARDWARE MANAGEMENT: HECETA

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: HW MANAGEMENT: HECETA		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 53



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: **SPEAKER** REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: SHEET: 54
1900 PRAIRIE CITY ROAD MAY 2002

8 7 6 5 4 3 2 1

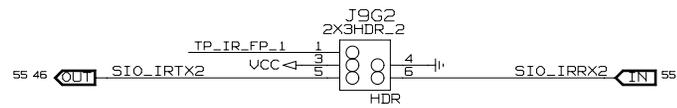
D

C

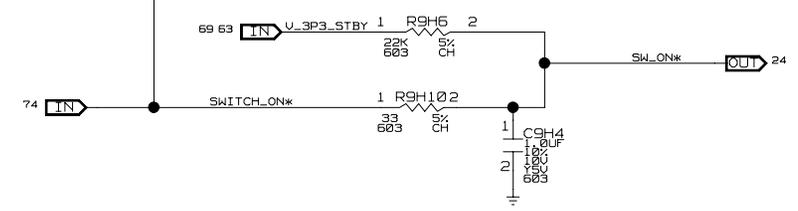
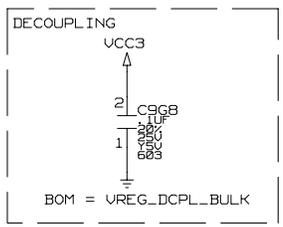
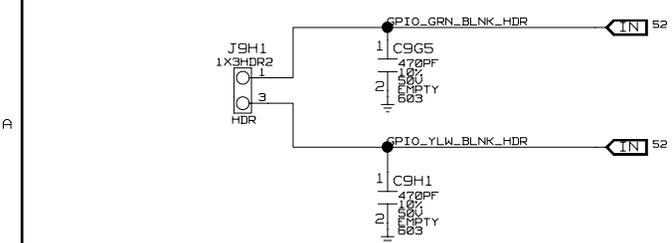
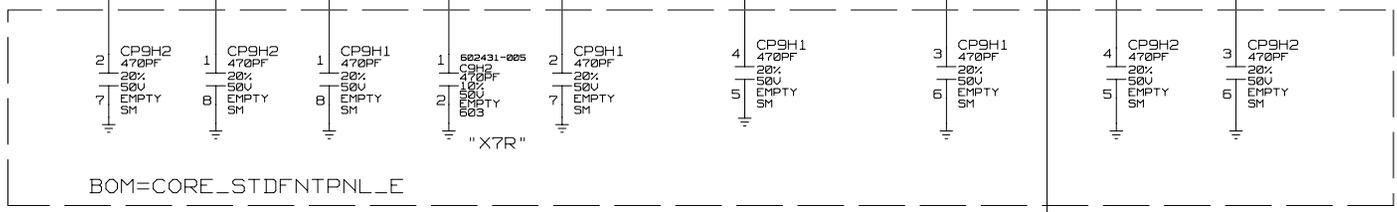
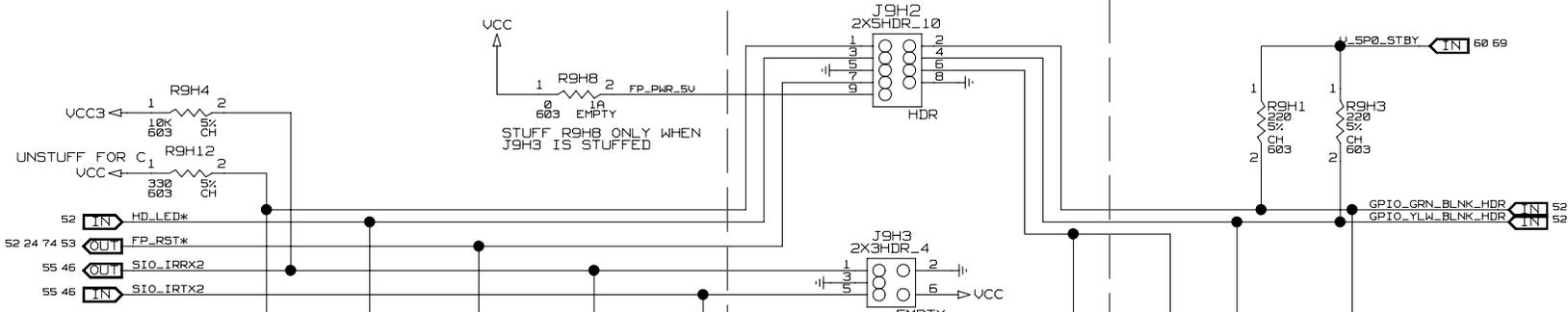
B

A

8 7 6 5 4 3 2 1



CAD NOTE: OVERLAY SO PINS
1-9 MATCH UP (DUAL FP).
J9G2 DOES NOT NEED TO BE DUAL FP'D



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	STD FRONT PANEL HDR	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 55

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C

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B

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THIS PAGE IS INTENTIONALLY LEFT BLANK

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: BLANK
REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002
1900 PRAIRIE CITY ROAD SHEET: 56
FOLSOM, CALIFORNIA 95630

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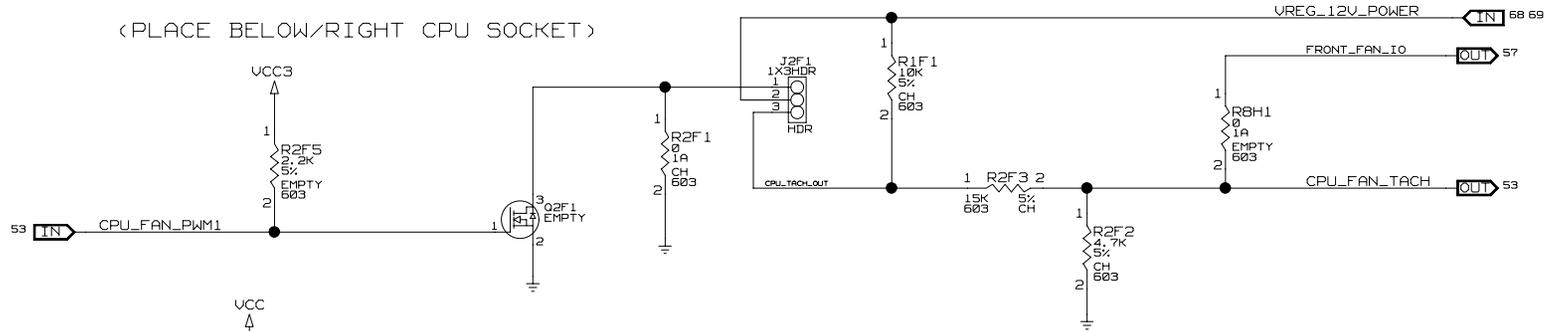
3

2

1

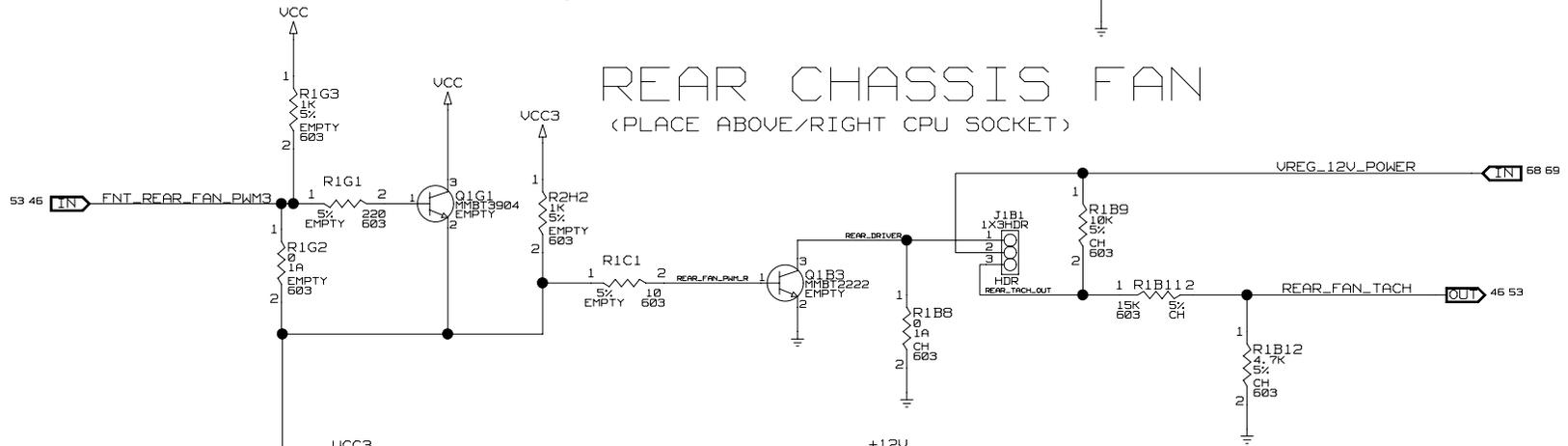
CPU ALWAYS-ON FAN

(PLACE BELOW/RIGHT CPU SOCKET)



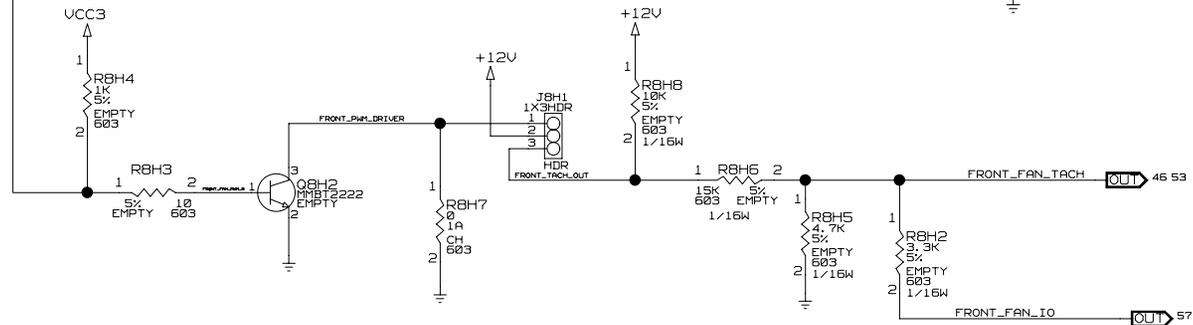
REAR CHASSIS FAN

(PLACE ABOVE/RIGHT CPU SOCKET)



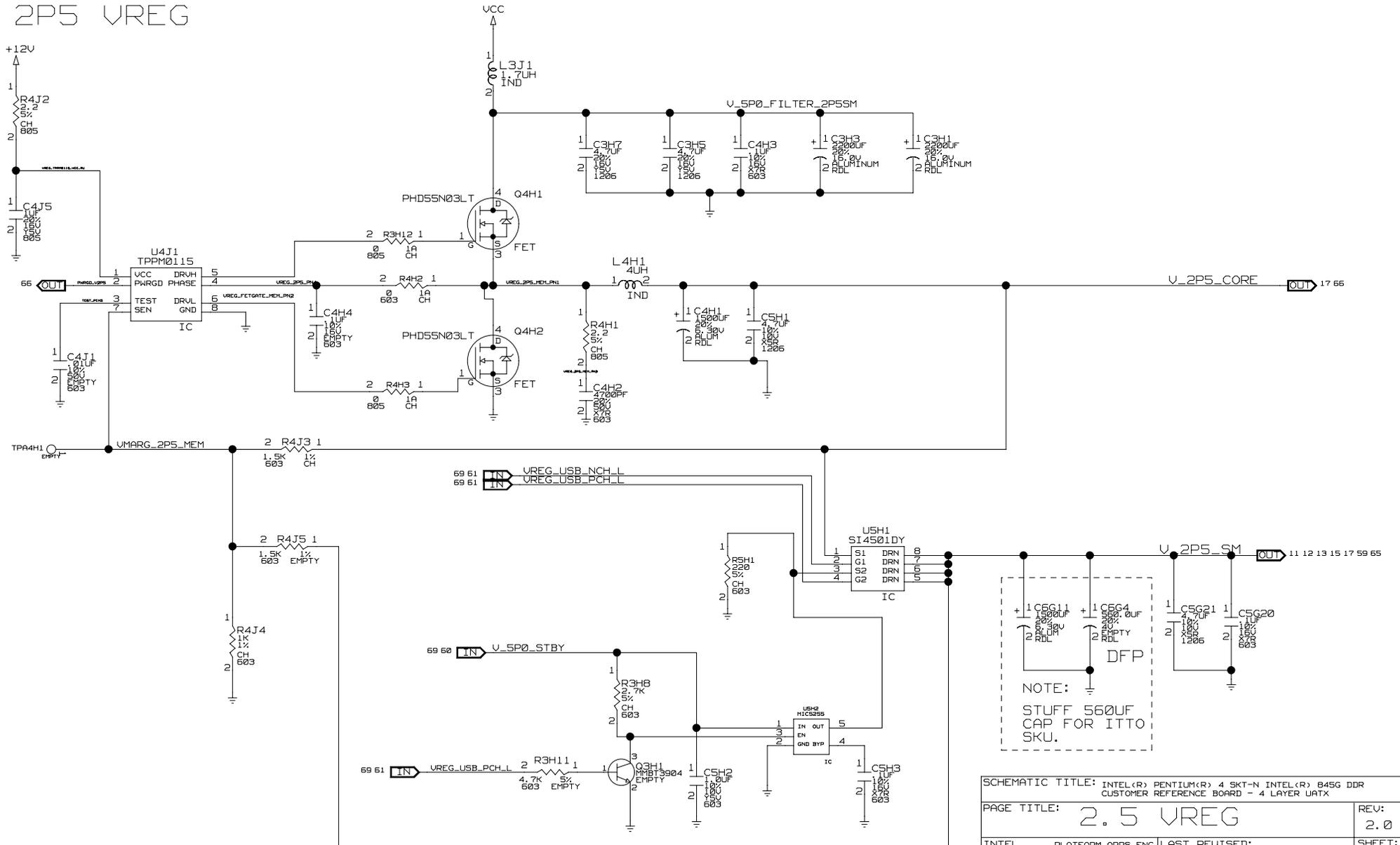
FRONT CHASSIS FAN

(PLACE LOWER LEFT CORNER OF PLATFORM)



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	FAN HEADERS	REV: 2.0
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 57

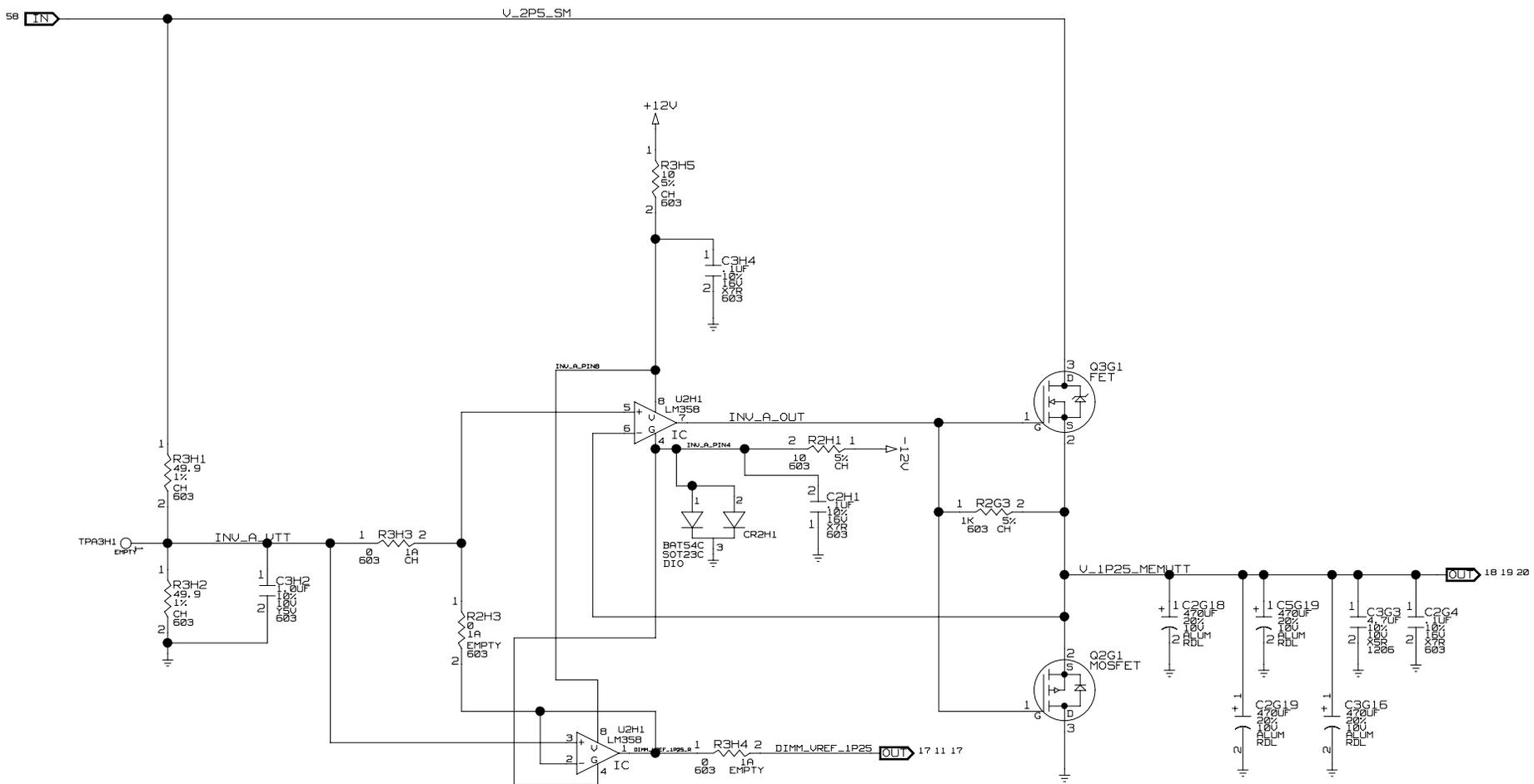
2P5 VREG



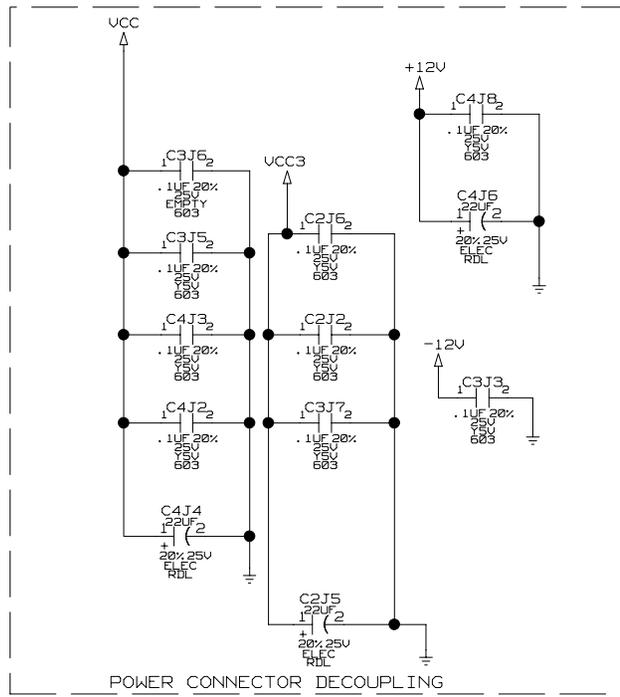
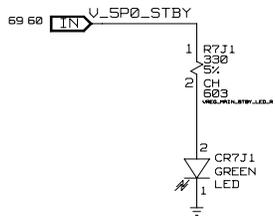
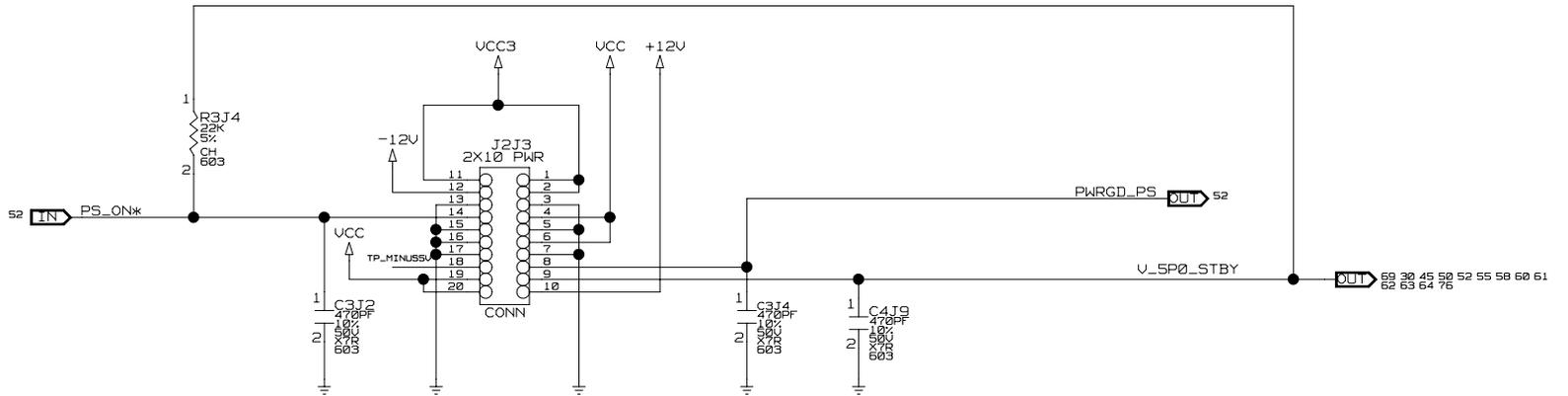
NOTE:
STUFF 560UF
CAP FOR ITTO
SKU.

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	2.5 VREG	REV: 2.0
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 58

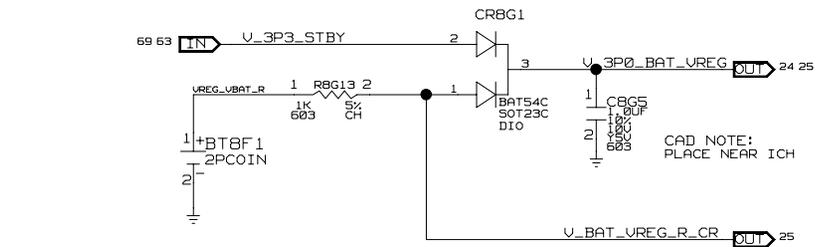
1.25V DDR



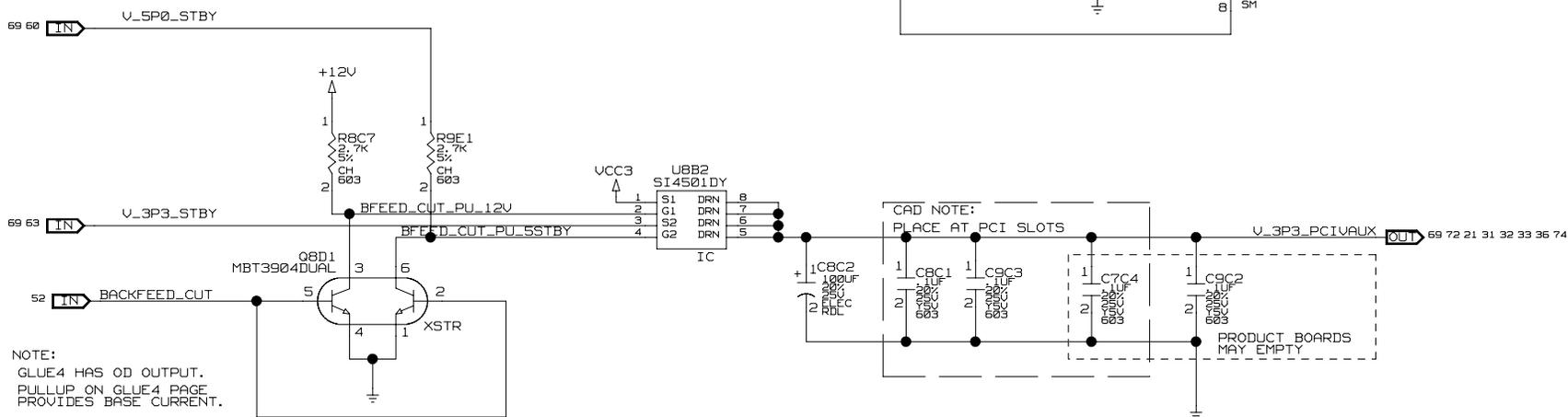
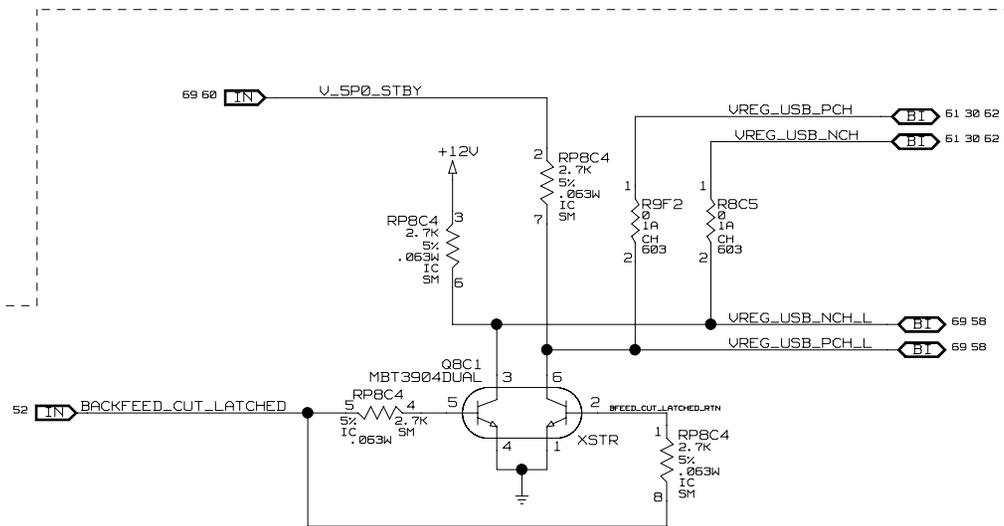
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	1P25 VREG	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 59



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: STANDARD POWER CONNECTOR		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 60



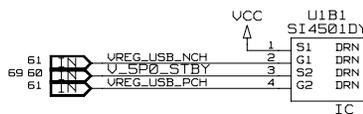
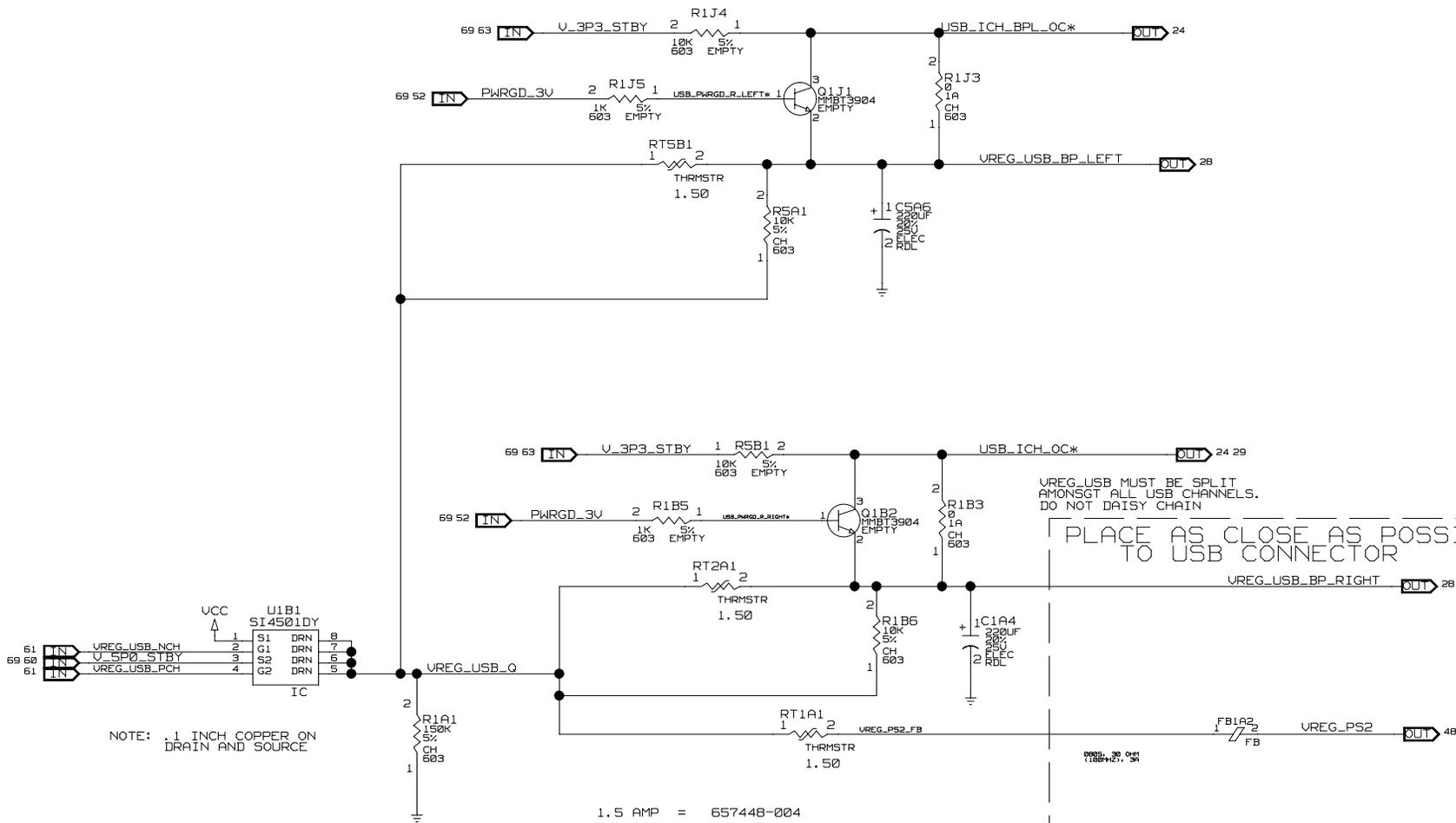
THROUGH-HOLE
CAD NOTE: DO NOT PLACE BATTERY NEAR
MOUNTING HOLES, GROUND OR VIAS



PCI VAUX

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE:	PCI VAUX	REV:	2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET:	61



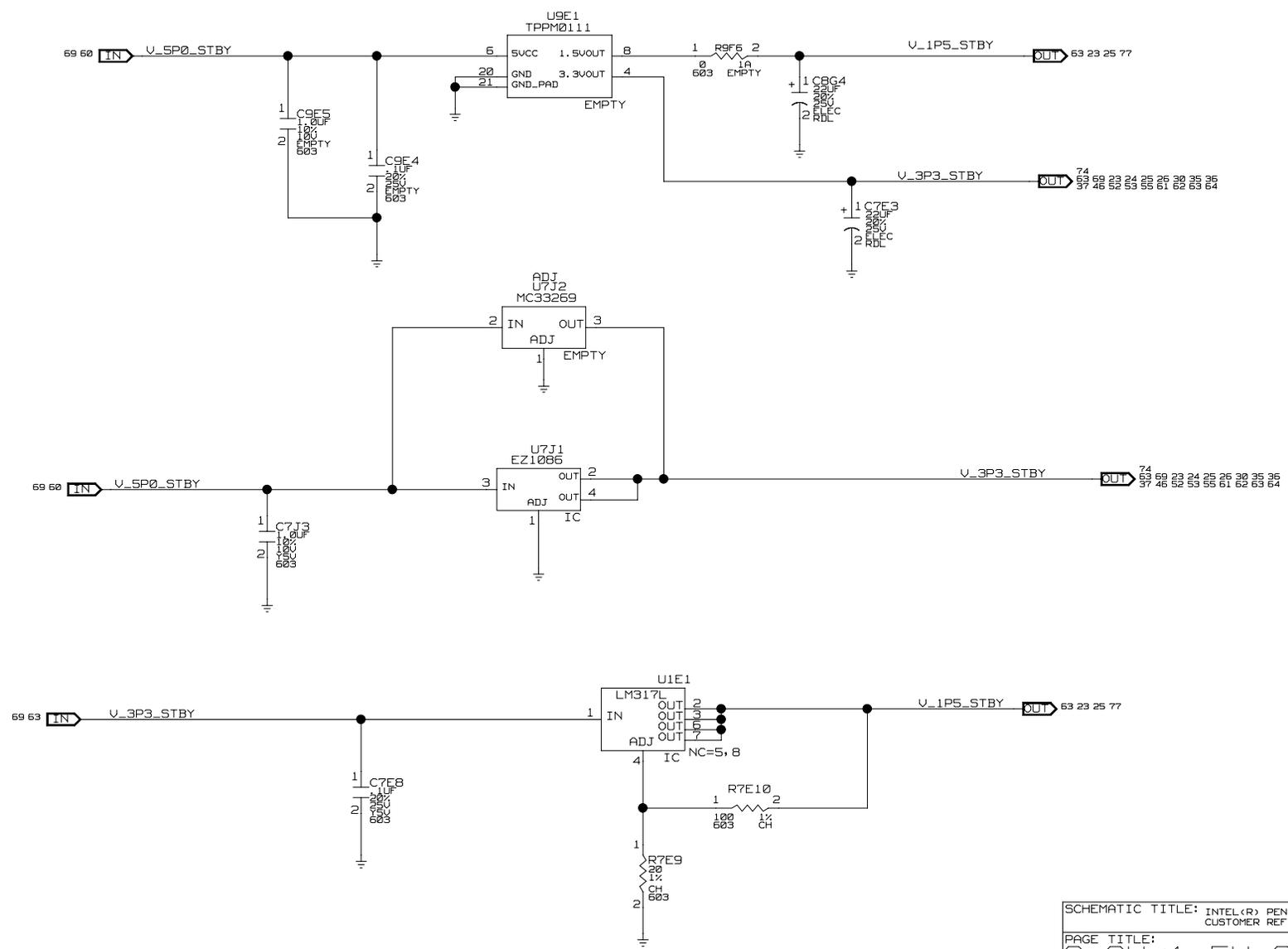
NOTE: .1 INCH COPPER ON DRAIN AND SOURCE

1.5 AMP = 65744B-004
 0.75 AMP = 65744B-001

VREG_USB MUST BE SPLIT AMONGST ALL USB CHANNELS. DO NOT DAISY CHAIN

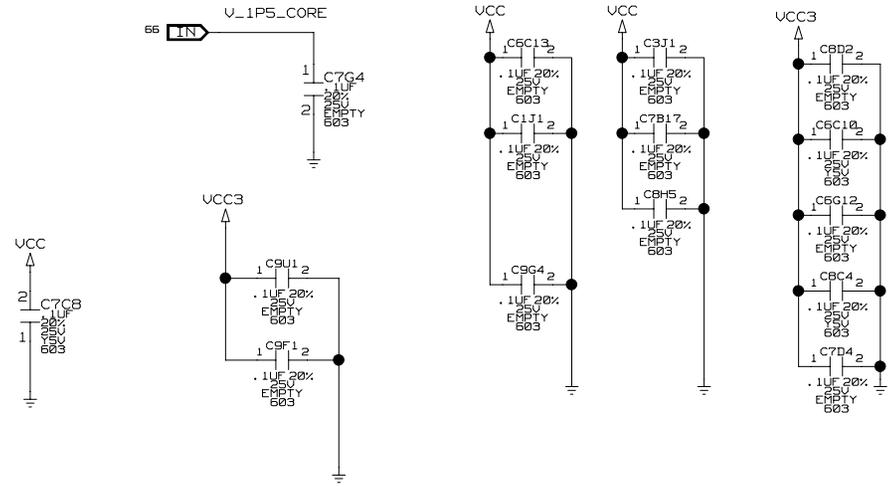
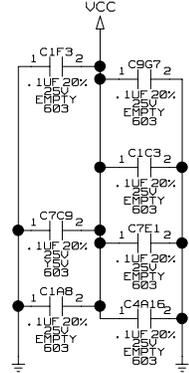
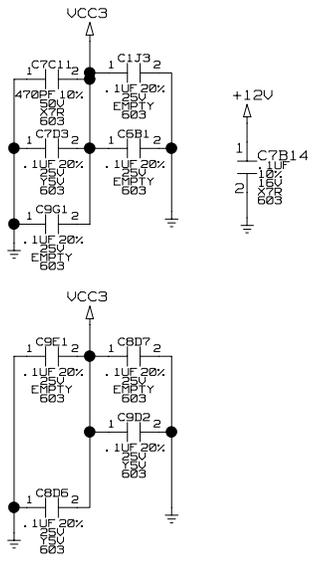
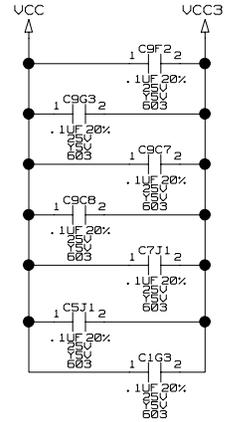
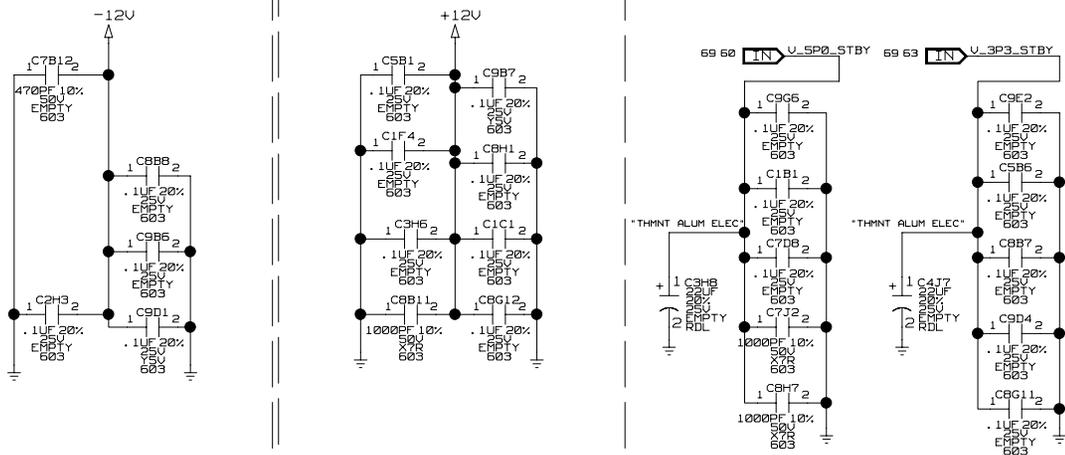
PLACE AS CLOSE AS POSSIBLE TO USB CONNECTOR

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: WAKE ON USB & PS2	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002 SHEET: 62

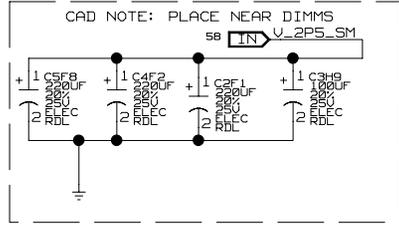
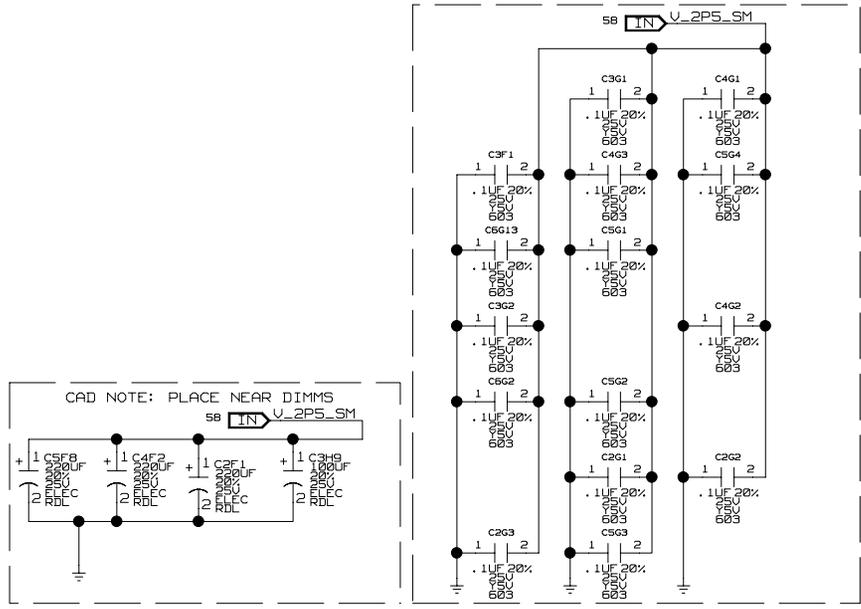


SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: 3.3V/1.5V STANDBY	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002 SHEET: 63

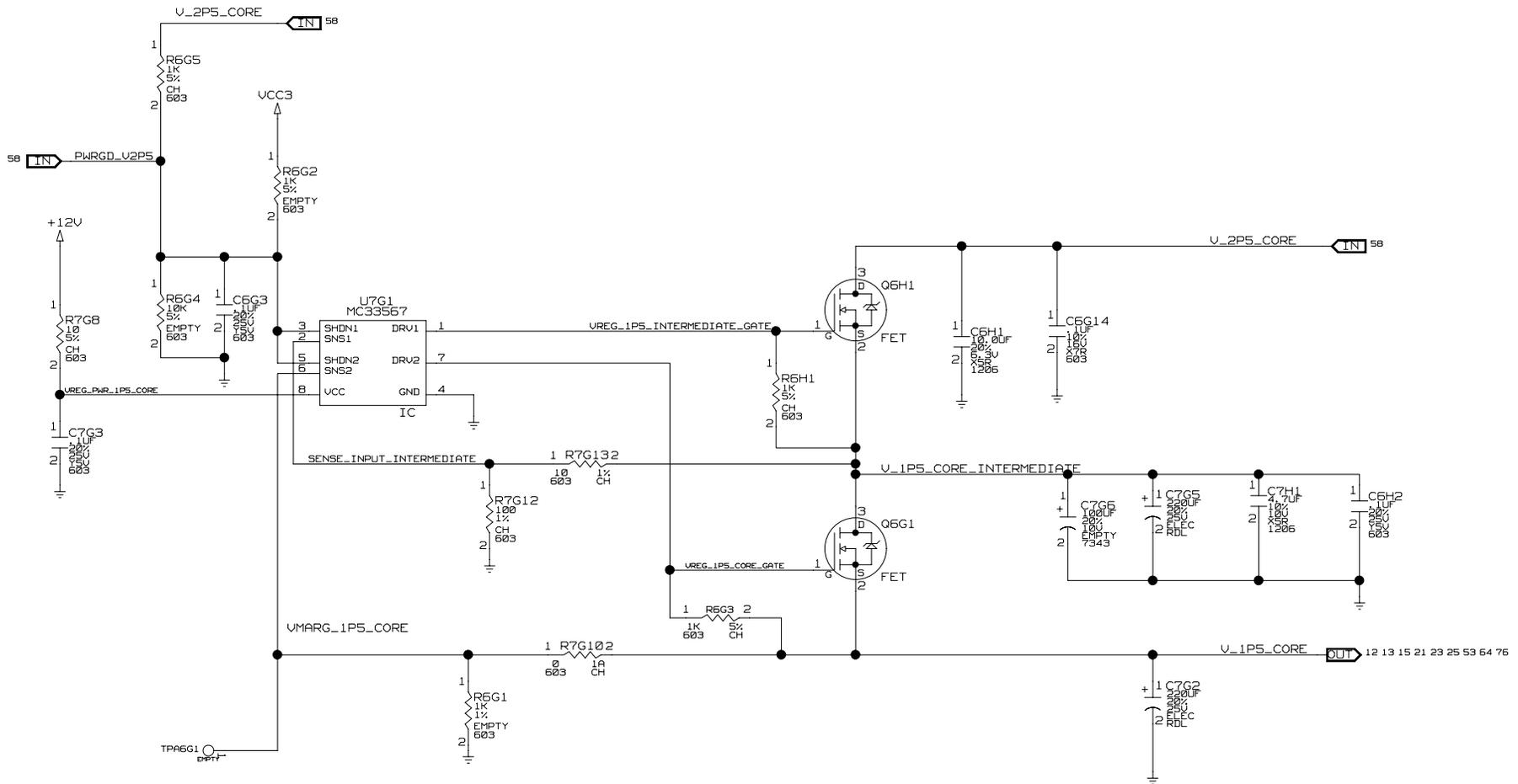
VREG_DCPL_BULK



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: VREG BULK DECOUPLING		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 64



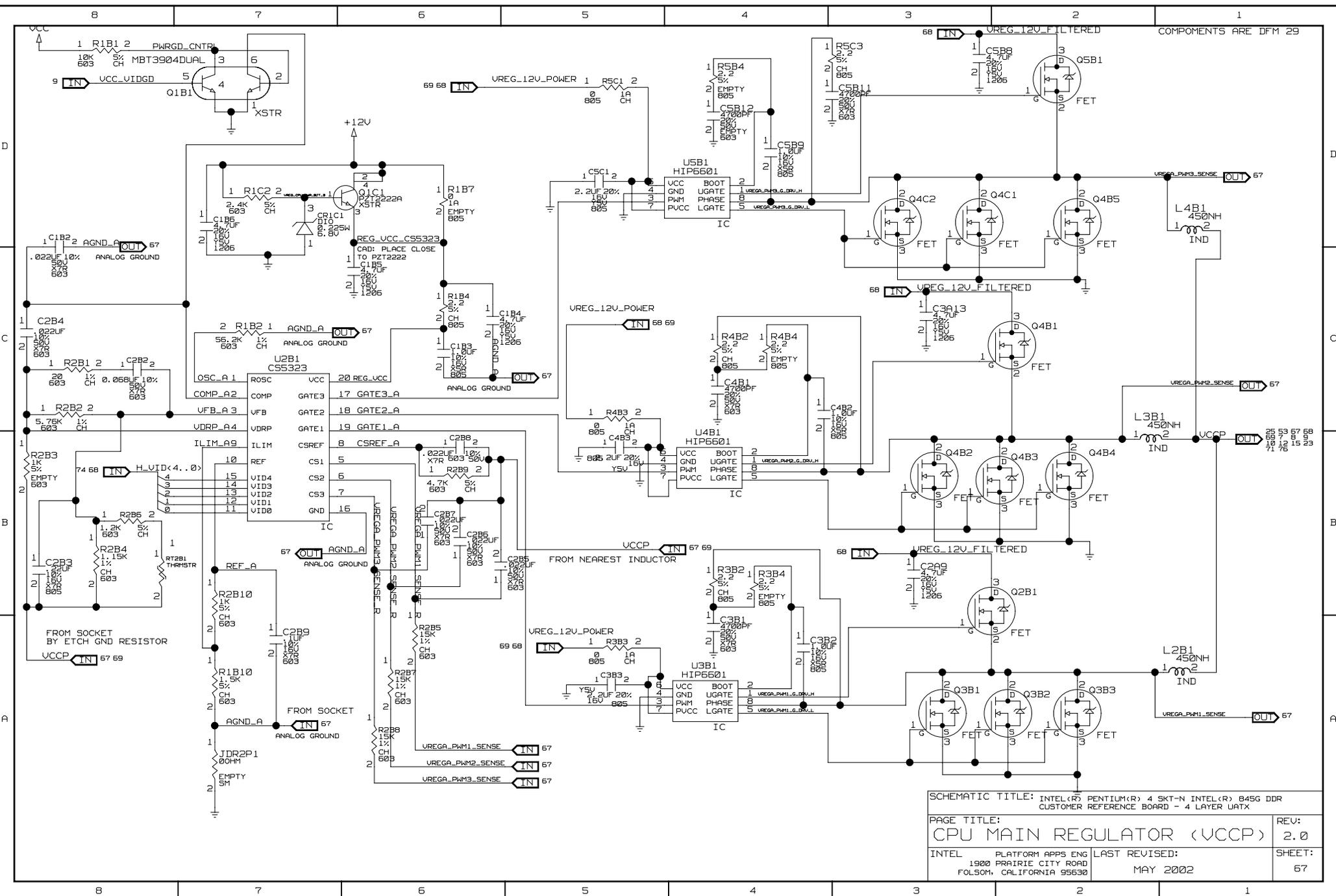
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: DDR 2P5_SM DECOUPLING	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002 SHEET: 65



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: 1P5 VREG REV: 2.0

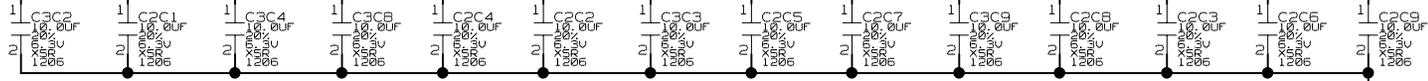
INTEL PLATFORM APPS ENG LAST REVISED: SHEET: 66
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630 MAY 2002



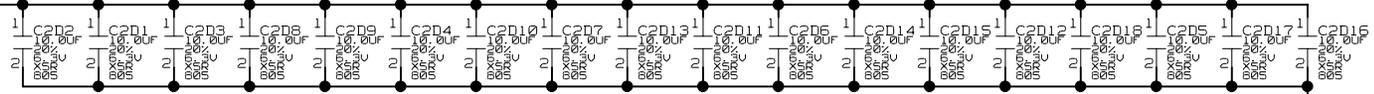
COMPONENTS ARE DFM 29

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: CPU MAIN REGULATOR (VCCP)	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002
	SHEET: 67

69 67 IN UCCP



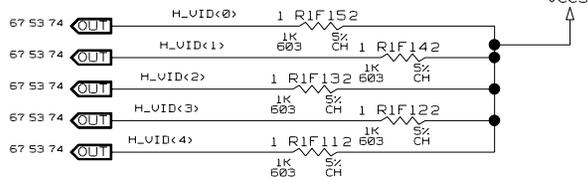
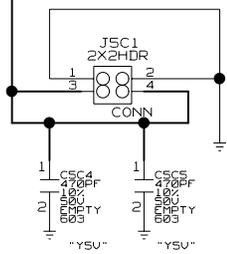
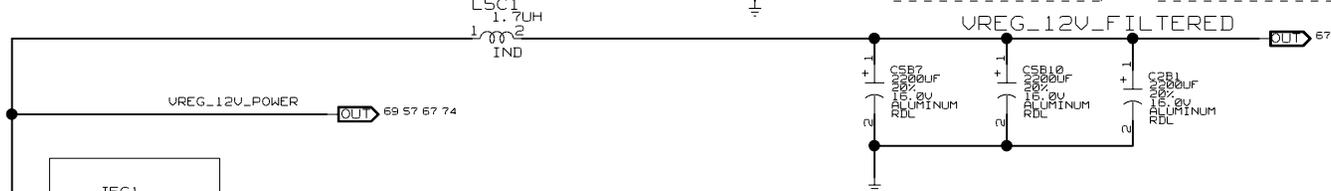
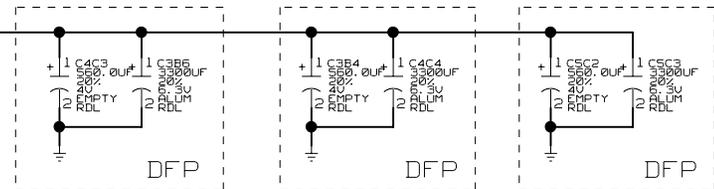
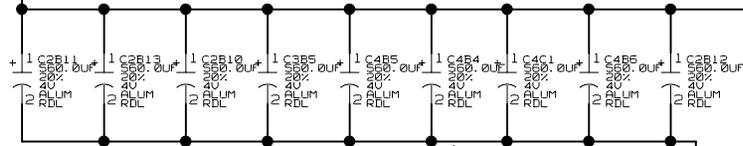
NOTE: PLACE THESE NORTH OF THE CPU SOCKET



NOTE: PLACE THESE IN THE CAVITY OF THE CPU SOCKET

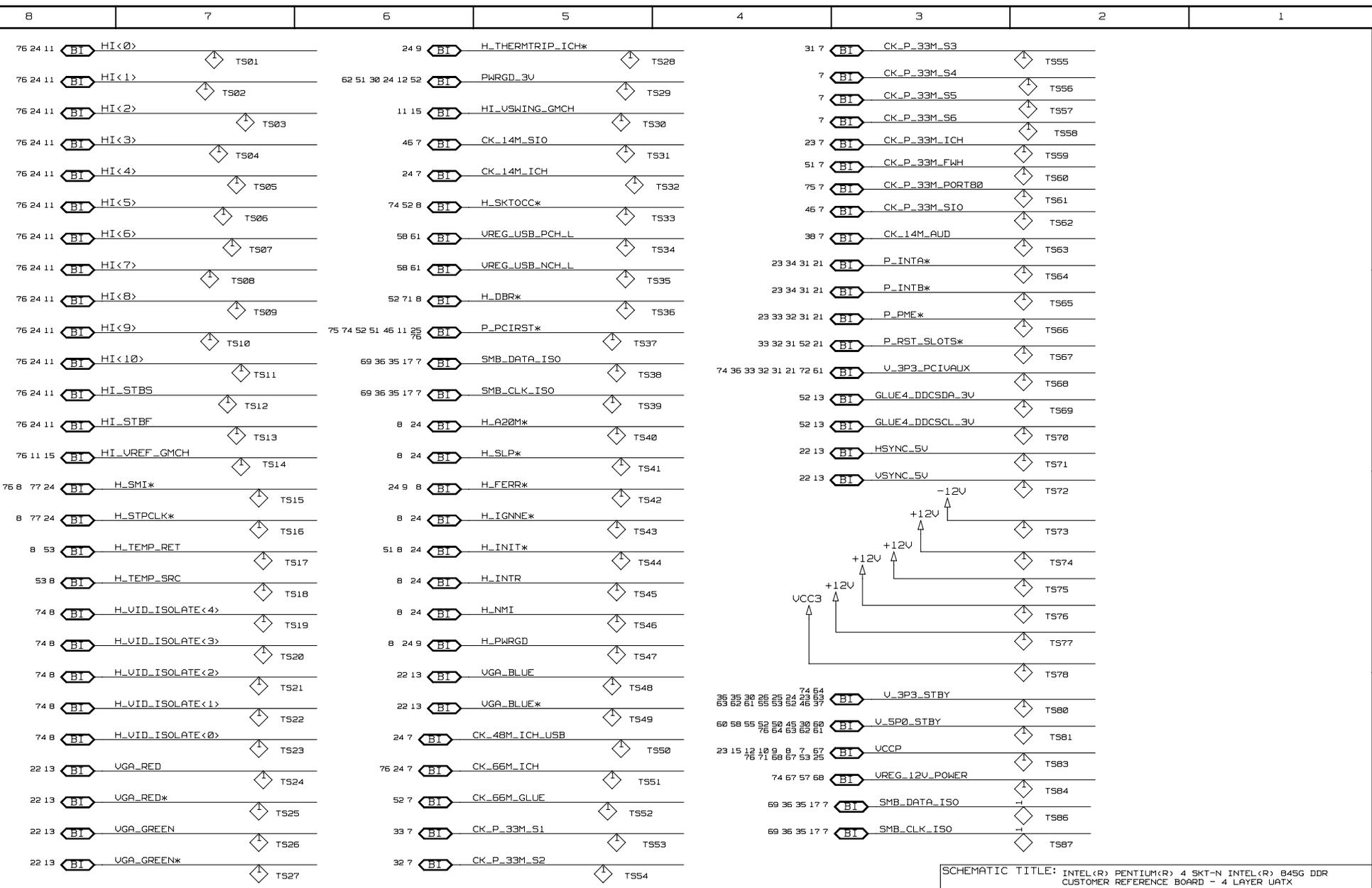


NOTE: PLACE THESE SOUTH OF THE CPU SOCKET



CAPACITORS

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 645G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: CPU DECOUPLING	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002
	SHEET: 68



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: DCL TRACK SPLITTERS	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002
	SHEET: 69

8

7

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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE:	BLANK	REV:	2.0
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INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG	LAST REVISED:	MAY 2002	SHEET:	70
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8

7

6

5

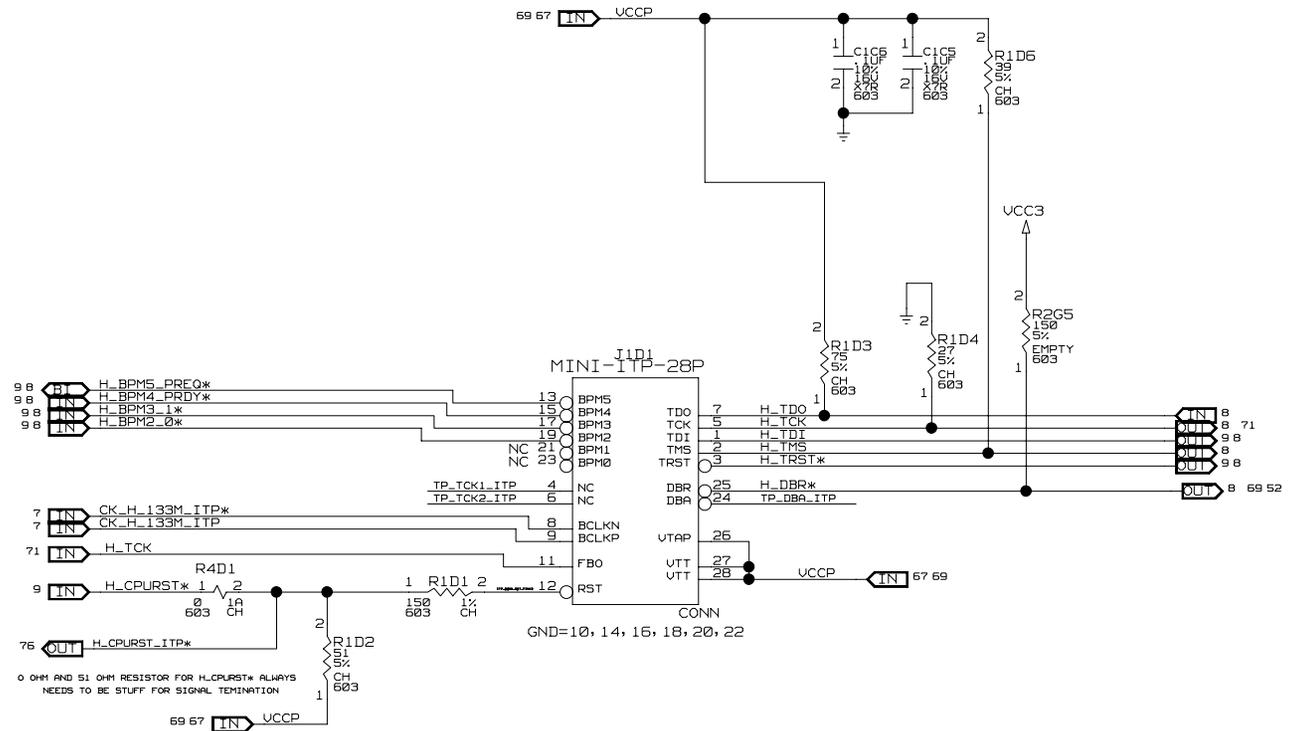
4

3

2

1

ITP 700FLEX CONNECTOR



CAD NOTE: ROUTE H_TCK FROM THE TCK PIN OF THE CONNECTOR
TO THE PROCESSOR PIN. FBO LENGTH = TCK + BPM LENGTHS TO CPU.
SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

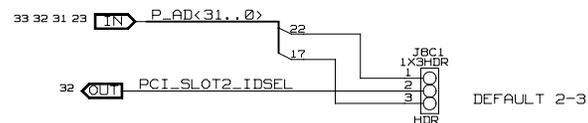
PAGE TITLE:
ITP 700FLEX CONNECTOR REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: SHEET: 71
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630 MAY 2002

DEBUG HOOKS MOON ISA



J8B3/J8C1	PCI SLOT 2 MODE
1-2	MOON ISA
2-3	PCI <DEFAULT>



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	MOON ISA	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 72

8 7 6 5 4 3 2 1

D

D

C

C

B

B

A

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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	BLANK	REV: 2.0
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG LAST REVISED: MAY 2002	SHEET: 73

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

D

D

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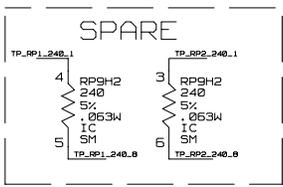
A

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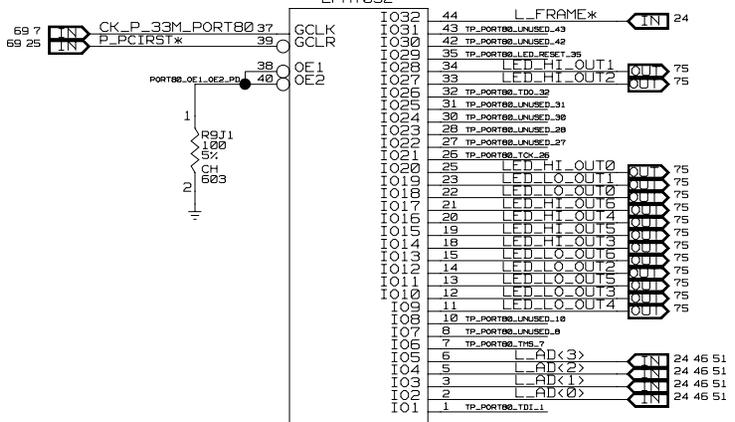
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: BLANK		REV: 2.0
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG	LAST REVISED: MAY 2002
		SHEET: 74

8 7 6 5 4 3 2 1



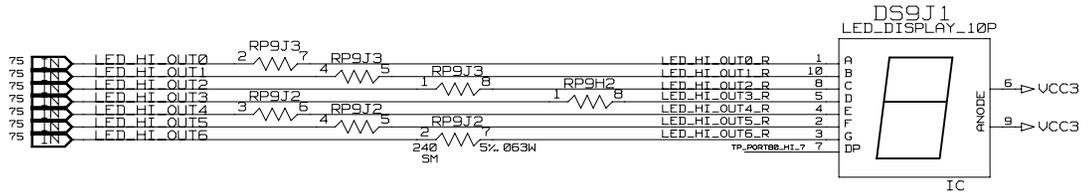
EPM7032AETC44-10
44 PIN TQFP

U9J1
EPM7032



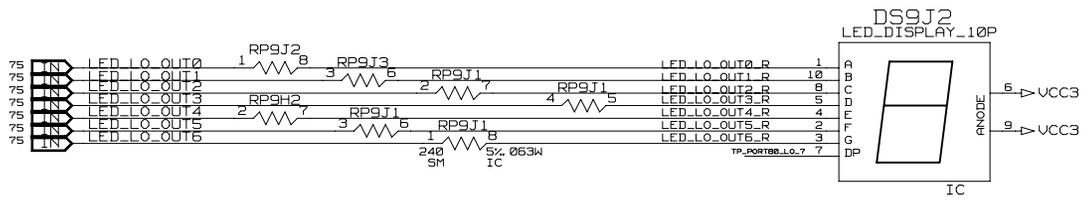
IC
UCC(PQFP)=9, 17, 29, 41
GND(PQFP)=4, 16, 24, 36
NC(PQFP)=45
UCC=UCC3(<~PORTB0DEC)

CAD NOTE: ORIENT TO LEFT

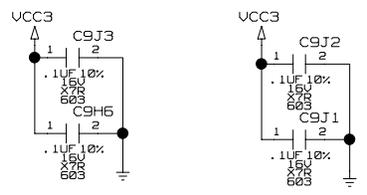


ALL RPACKS 240 OHMS

CAD NOTE: ORIENT TO RIGHT



CAD NOTE: PLACE 1 EACH ON PINS 6 & 9 OF EACH DISPLAY



DEBUG/EV FEATURE: PORT 80 DECODER & DISPLAY

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G DDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: PORT 80 DECODER & DISPLAY	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 75

PAGE # COMPONENT/FUNCTION

*1	COVER PAGE.
#2	TABLES: BLOCK DIAGRAM
3	TABLES: RESET MAP
#4	TABLES: CLOCK DISTRIBUTION
5	TABLES: GPIO/IDSEL MAPPING
#6	TABLES: VOLTAGE DISTRIBUTION
7	CORE: CK_408 (MAIN CLOCK GENERATOR)
8	CORE: CPU CONNECTOR
9	CORE: CPU PULL-UPS & PULL-DOWNS
10	CORE: CPU ANALOG FILTER
*11-13	CORE: INTEL(R) 845G GMCH
*14	CORE: INTEL(R) 845G GMCH PWR #1
#15	CORE: INTEL(R) 845G DECOUPLING & REFERENCE VOLTAGES
*16	DIMM TERMINATION/DECOUPLING
#17	CORE: DIMM CONNECTORS
*18-19	BLANK
*20	BLANK
21	CORE: AGP SLOT & AGP PULL-UPS/PULL-DOWNS
22	CORE: VGA CONNECTOR (DFM29)
23-24	ICH: 82801A I/O CONTROLLER HUB
25	ICH: ICH PULL-UP/PULL-DOWNS
26	ICH: LAN LINK
27	ICH: IDE PRIMARY & SECONDARY
28	ICH: USB BACK PANEL CONNECTORS
29	BLANK
30	ICH: USB FRONT PANEL/CNR VREG & OC#
31-33	ICH: PCI SLOTS 3 - 1
34	ICH: PCI PULL-UPS
35	SMBUS ISOLATION
36	CNR CONNECTOR
37	BLANK
38	AUDIO: CODEC (AD1885 OR CS4201)
39	AUDIO: CODEC FILTERING CAPS
40	AUDIO: AUX-IN, CD-IN, LINE-IN: ATA/PI HEADERS
41	AUDIO: MIC-IN
42	AUDIO: LINE-OUT
43	AUDIO: FRONT PANEL AUDIO HEADER
44	AUDIO: TRANSIENT CONTROL
45	AUDIO: ANALOG VREG
46	SIO: LPC47M102
47	SIO: FLOPPY
48	SIO: KEYBOARD & MOUSE PORTS (PS/2) (DFM29)

PAGE # COMPONENT/FUNCTION

49	SIO: PARALLEL PORT (DFM29)
50	SIO: COM1 (DFM29)
51	FWH: MFG MODE AND RECOVERY JUMPERS
52	GLUE4
53	HECETA4 & HECETA6
54	PC SPEAKER
55	FRONT PANEL HEADER
56	BLANK
57	FAN: FAN HEADERS (3)
*58	VREG: 3.3V SYSTEM MEMORY
*59	VREG: BLANK
60	VREG: POWER CONNECTOR
61	VREG: BATTERY, PCI VAUX, USB_NCH & USB_PCH
62	VREG: USB BACK PANEL, PS/2
63	VREG: 1.5V STBY & 3.3V STBY
64	VREG: BULK DECOUPLING
*65	VREG: 3.3V SM DECOUPLING
*66	VREG: CORE 1.5V
67	VREG: CPU MAIN REGULATOR (VCCP)
68	VREG: CPU DECOUPLING, 12V FILTER INDUCTOR
69	DCL TRACK SPLITTERS
70	BLANK
71	DEBUG: ITP PORT AND PULL-UPS
72	MOON ISA RESISTORS
73-74	BLANK
75	DEBUG: PORT80 DECODER

NOTE:

- * = CHANGED OR MODIFIED FROM DDR SCHEMATIC
- # = COPIED FROM PREVIOUS SDR SCHEMATIC
- #1 = SCHEMATIC SUPPORTS GMCH REV 1.5 FOOTPRINT PAGE 14 ONLY FOR BALLOUT 1.0 COMPATIBILITY

POWER SYMBOLS USED:

VCC3
VCC
+12V
-12V

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPL'S FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5 VOLTS UNLESS OTHERWISE SPECIFIED.
4. VCC3 = +3.3 VOLTS UNLESS OTHERWISE SPECIFIED.
5. * SUFFIX INDICATES ACTIVE LOW SIGNAL.

INTEL(R) 845G SDR SCHEMATICS REV 2.0

CAUTION:

THIS VERSION OF THE SDR SCHEMATICS CONTAINS AN OLD GMCH BALLOUT, BALLOUT 1.5. BOARD DESIGNERS SHOULD OPTIMIZE FOR THE BALLOUT 2.0. ADDITIONAL BALLOUT INFORMATION CAN BE FOUND IN THE LATEST REVISION OF THE INTEL(R) 845G/845GL GMCH DATASHEET. NO PLANS CURRENTLY EXIST TO UPDATE THE SDR SCHEMATICS WITH THE GMCH BALLOUT 2.0.

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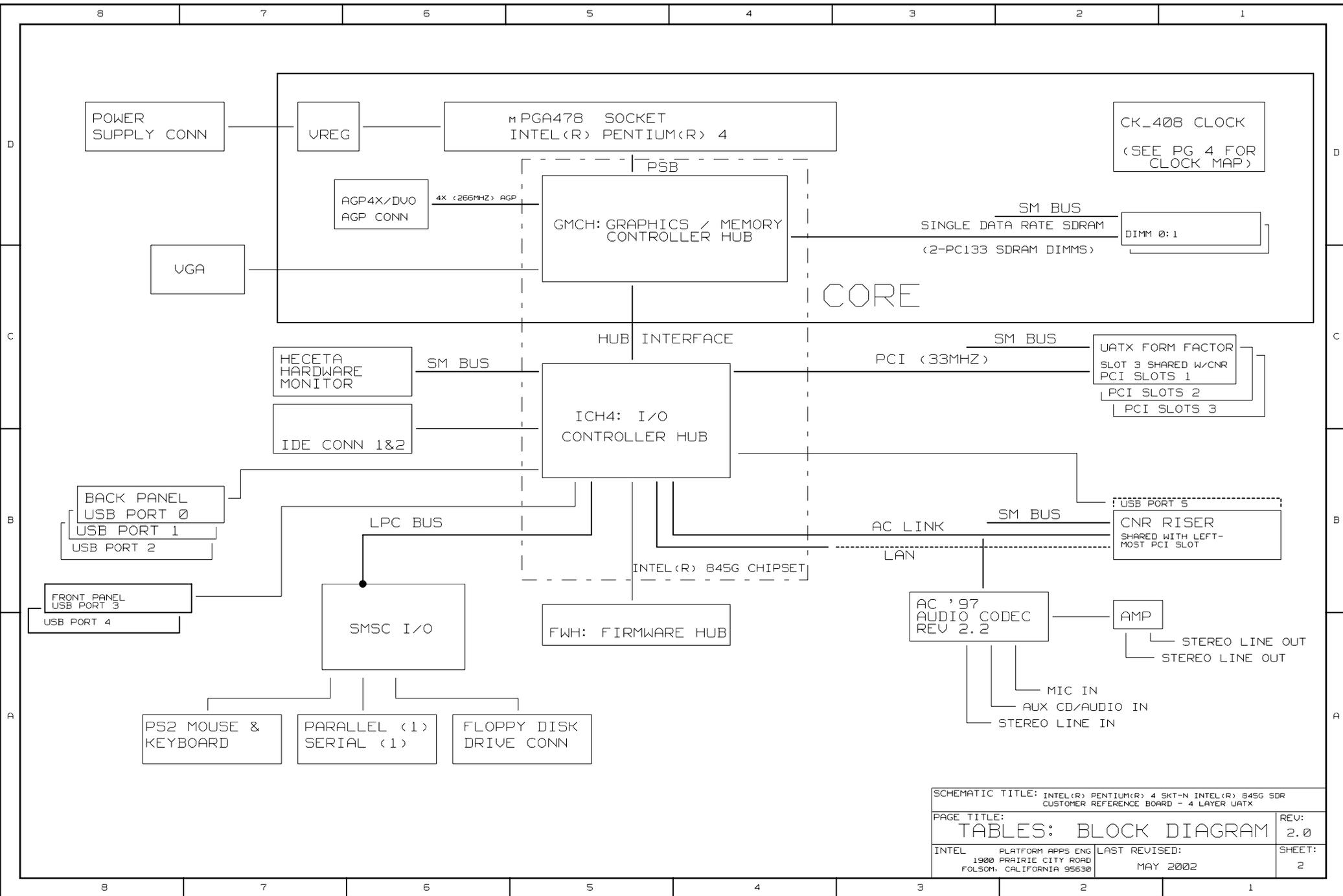
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INTEL CORPORATION
WWW.INTEL.COM
OR CALL 1-800-548-4725

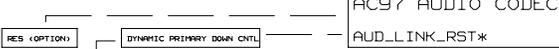
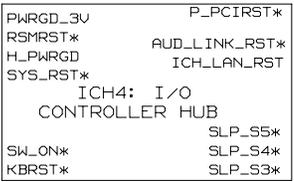
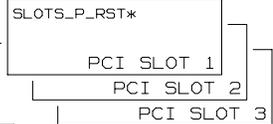
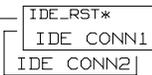
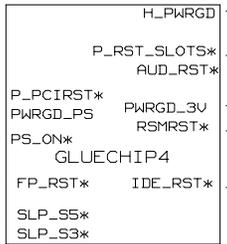
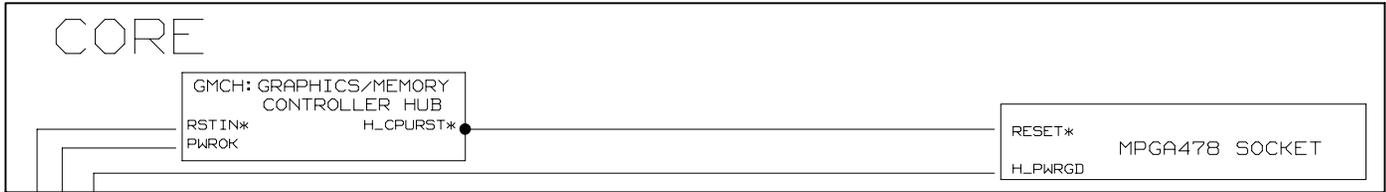
*OTHER NAMES AND BRANDS MAY BE CLAIMED AS THE PROPERTY OF OTHERS.

INTEL(R) PENTIUM(R) 4 SKT-N/INTEL(R) 845G CUSTOMER REFERENCE BOARD (CRB) 2-SDR SDRAM, 4 LAYER, UATX

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: COVER PAGE	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 1

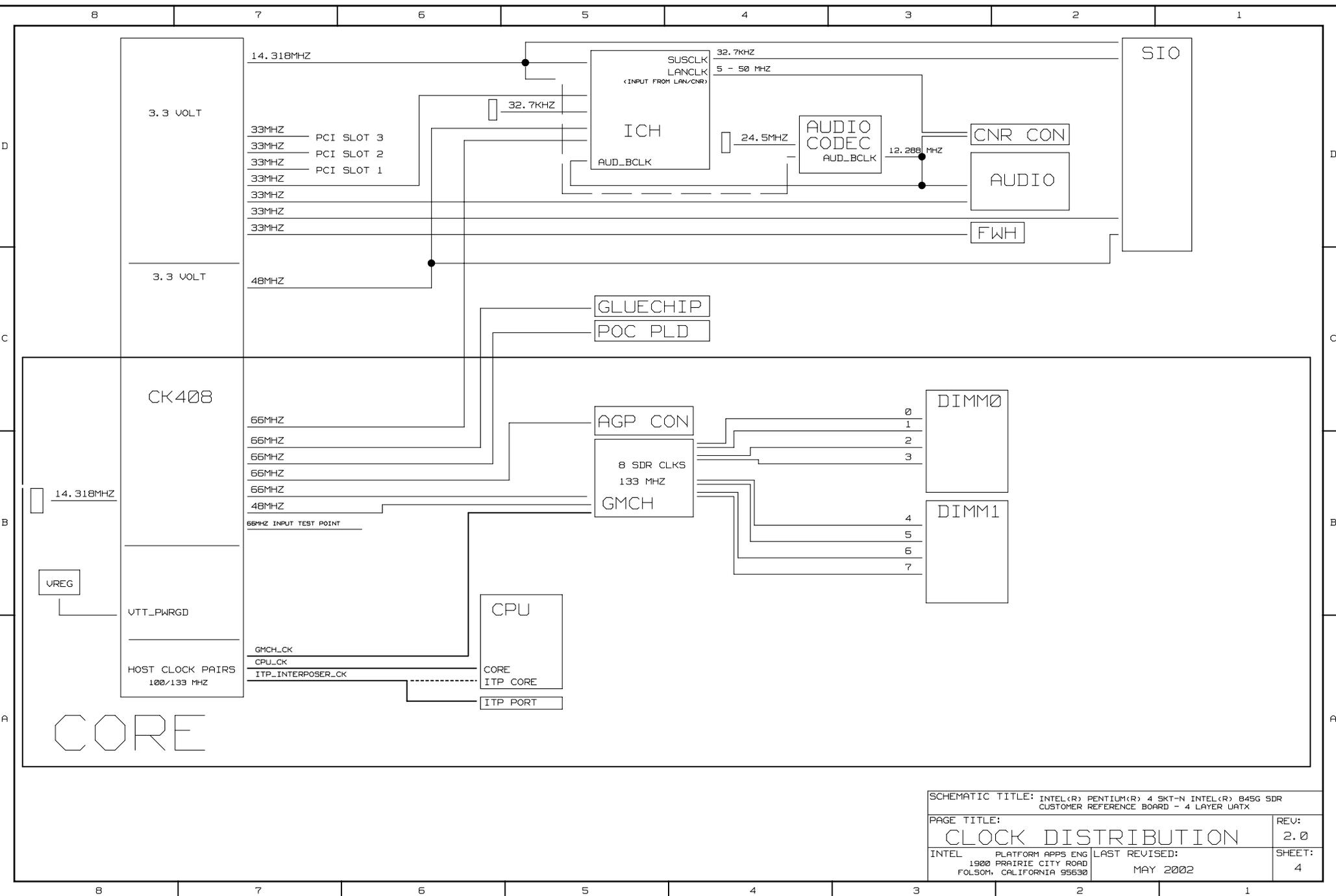


SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: TABLES: BLOCK DIAGRAM	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 2



RESET MAP

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX			
PAGE TITLE: RESET MAP			REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: MAY 2002	SHEET: 3



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: CLOCK DISTRIBUTION		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 4

ICH4

PIN NAME	PWR WELL	USAGE	DURING RESET	S3/S4/S5	INTERNAL PULL-UP	NOTES
GPI<0>	CORE	P_REQA#	---	---		
GPI<1>	CORE	P_REQB#	---	---		
GPI<2>	CORE	P_IRQE#	---	---		
GPI<3>	CORE	P_IRQF#	---	---		
GPI<4>	CORE	P_IRQG#	---	---		
GPI<5>	CORE	P_IRQH#	---	---		
GPI<6>	CORE	UNUSED	---	---		
GPI<7>	CORE	UNUSED	---	---		
GPI<8>	RESUME	UNUSED	---	---		
GPI<11>	RESUME	SMB_ALERT#	---	---		
GPI<12>	RESUME	LPC_SIO_SMI#	---	---		
GPI<13>	RESUME	LPC_SIO_PME#	---	---		
GPO<16>	CORE	P_GNTA#	HIGH	OFF	24K	
GPO<17>	CORE	P_GNTS#	HIGH	OFF	24K	
GPO<18>	CORE	UNUSED	HIGH	OFF		
GPO<19>	CORE	UNUSED	HIGH	OFF		
GPO<20>	CORE	UNUSED	HIGH	OFF		
GPO<21>	CORE	ISA_GO_NOGO	HIGH	OFF		
GPO<22>	CORE	UNUSED	HIGH-Z	OFF		
GPO<23>	CORE	UNUSED	LOW	OFF		
GPIO<24>	RESUME	UNUSED	LOW	DEFINED		
GPIO<25>	RESUME	GPO_GRN_BLNK	HIGH	DEFINED		
GPIO<27>	RESUME	GPO_YEL_BLNK	HIGH	DEFINED		
GPIO<28>	RESUME	GPO_LAN_DISABLE	HIGH	DEFINED		
GPIO<32>	CORE	NO_POP*	HIGH	OFF		
GPIO<33>	CORE	UNUSED	HIGH	OFF		
GPIO<34>	CORE	UNUSED	HIGH	OFF		
GPIO<35>	CORE	UNUSED	HIGH	OFF		
GPIO<36>	CORE	UNUSED	HIGH	OFF		
GPIO<37>	CORE	<BOARD1>	HIGH	OFF		
GPIO<38>	CORE	<BOARD2>	HIGH	OFF		
GPIO<39>	CORE	<BOARD3>	HIGH	OFF		
GPIO<40>	CORE	<BOARD4>	HIGH	OFF		
GPIO<41>	CORE	UNUSED	HIGH	OFF		
GPIO<42>	CORE	UNUSED	HIGH	OFF		
GPIO<43>	CORE	CDC_DWN_ENAB*	HIGH	OFF		
RI*	RESUME					
THERM*	CORE					

IRQ ROUTING TABLE

	AGP	SLOT1	SLOT2	SLOT3	AC97/SMBUS	LAN
INT A	A			D		
INT B	B			C	A	
INT C				A		
INT D				B		
INT E		D	C			A
INT F		A	B			
INT G		B	A			
INT H		C	D			
REG /GNT						
IDSEL		16	17	18		24

ICH4

FWH

GPI4	CONFIG JUMPER	INPUT	DEFINED	CONFIG JUMPER
GPI3	MANUF MODE	INPUT	DEFINED	MANUF MODE
GPI2	HI/LOW BIOS CONFIG	INPUT	DEFINED	SPARE HI/LOW BIOS CONFIG STRAP
GPI1	GPIO_DMA66_DETECT_SEC	INPUT	DEFINED	ATA66 CABLE DETECT - SECONDARY
GPI0	GPIO_DMA66_DETECT_PRI	INPUT	DEFINED	ATA66 CABLE DETECT - PRIMARY

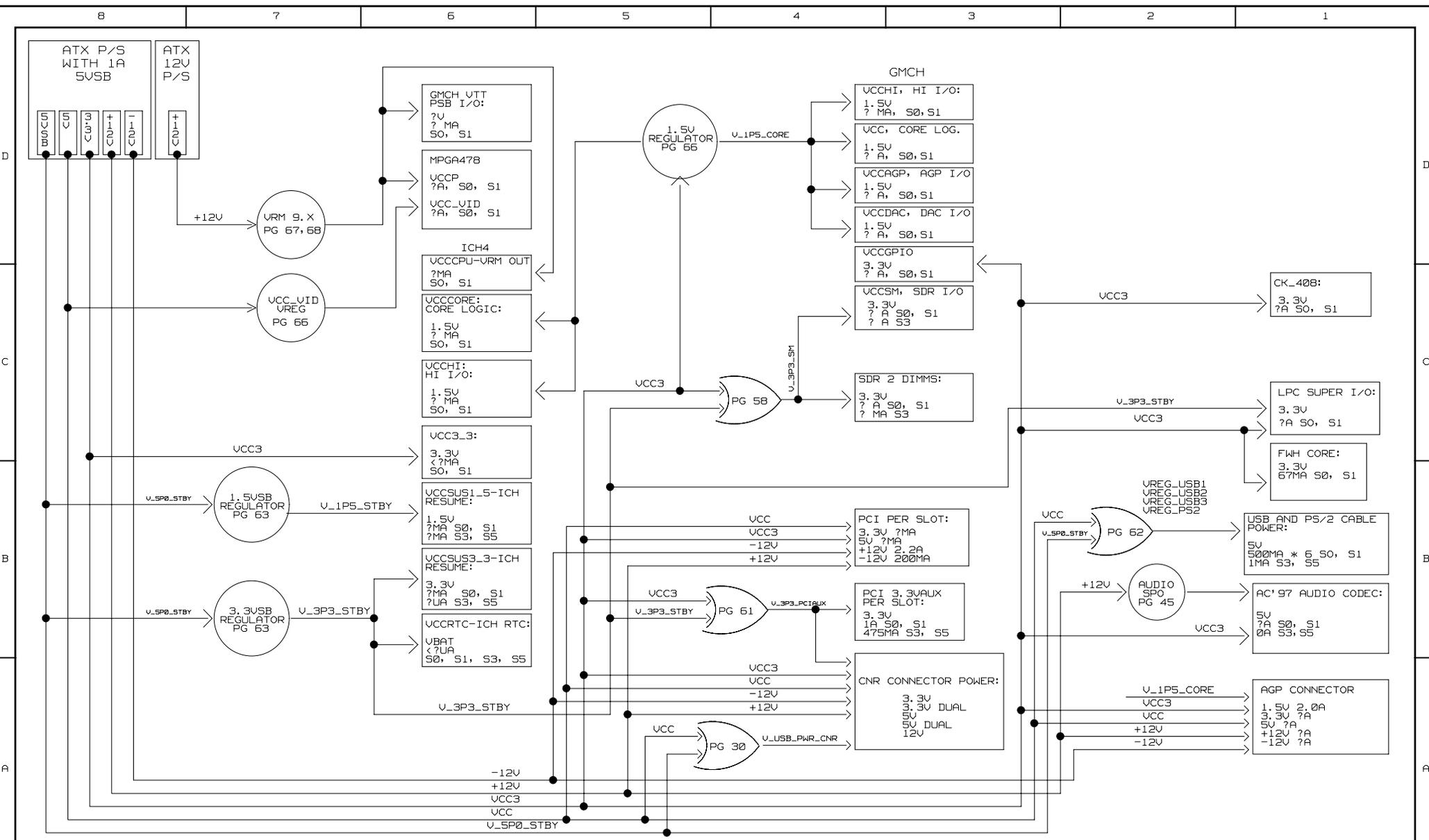
SIO

GPI020	RESISTOR STRAP OPTION	INPUT	DEFINED	DESIGN FEATURE WITH RESISTOR STRAPPING
GPI021	RESISTOR STRAP OPTION	INPUT	DEFINED	DESIGN FEATURE WITH RESISTOR STRAPPING
GP027/IOSMI*	IO_SMI*	INPUT	DEFINED	SENDS IO SMI REQUEST TO ICH2

MULTI-PLEXED GPIO PINS ON SIO USED FOR SPECIFIC FUNCTIONS (NOT AS GPIO) ARE NOT IDENTIFIED HERE
 UN-USED GPIO PINS ON SIO ARE NOT IDENTIFIED HERE

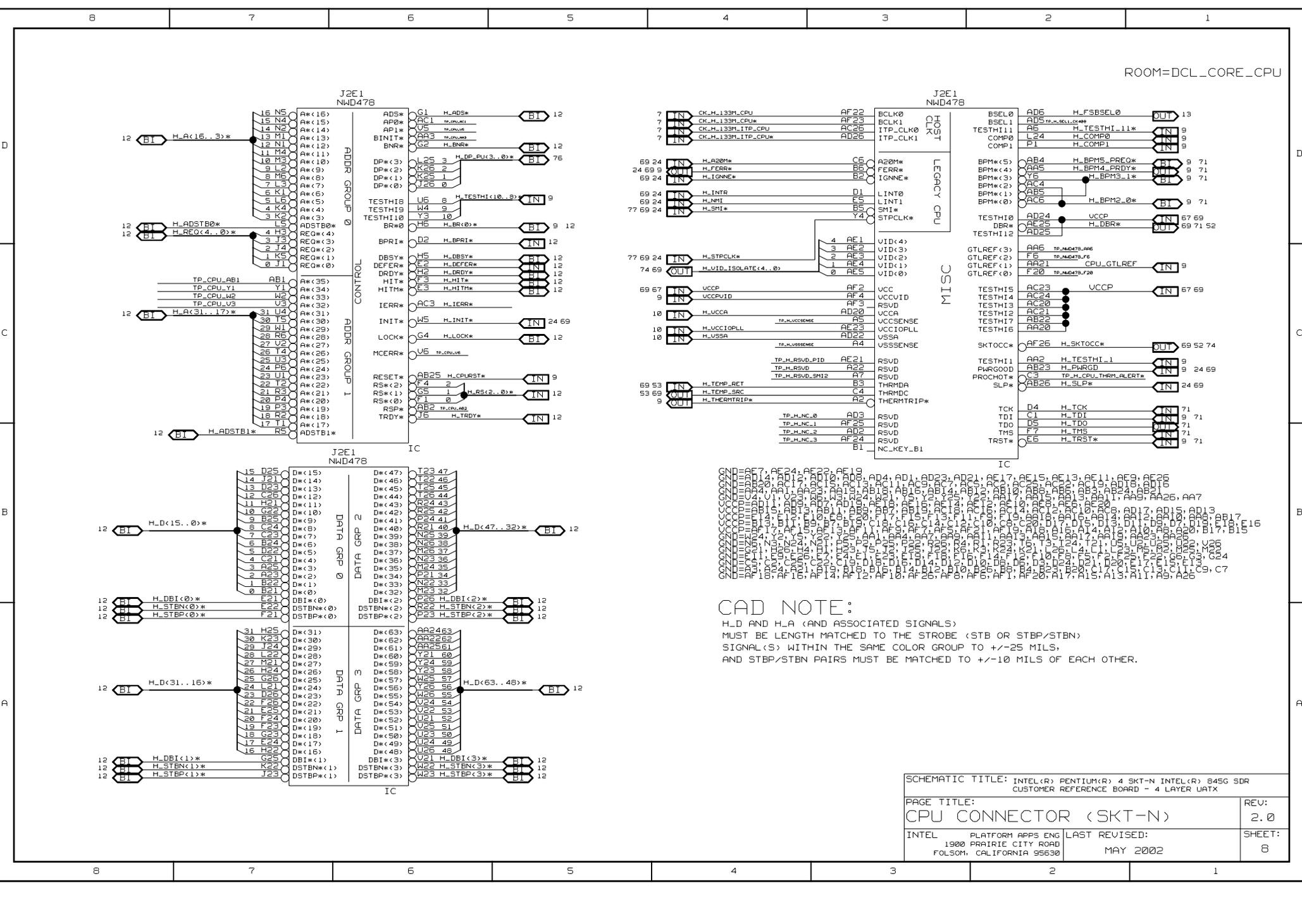
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR
 CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: GPIO, IRQ, IDSEL MAPS		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 5



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

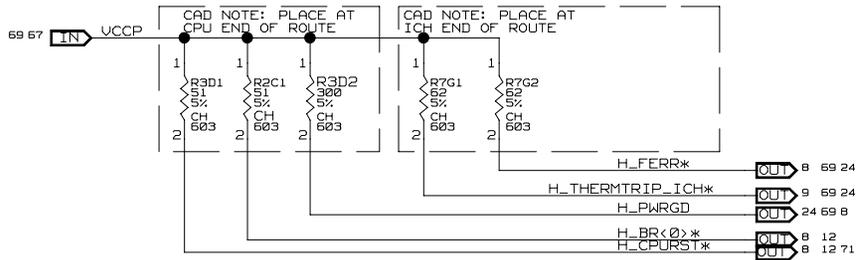
PAGE TITLE: VOLTAGE DISTRIBUTION	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002
	SHEET: 6



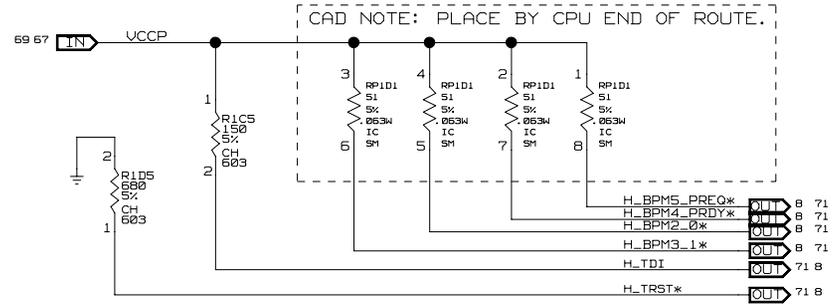
CAD NOTE:
 H_LD AND H_LA (AND ASSOCIATED SIGNALS)
 MUST BE LENGTH MATCHED TO THE STROBE (STB OR STBP/STBN)
 SIGNAL(S) WITHIN THE SAME COLOR GROUP TO +/-25 MILS,
 AND STBP/STBN PAIRS MUST BE MATCHED TO +/-10 MILS OF EACH OTHER.

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: CPU CONNECTOR (SKT-N)	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002
	SHEET: 8

CPU SIGNAL TERMINATION

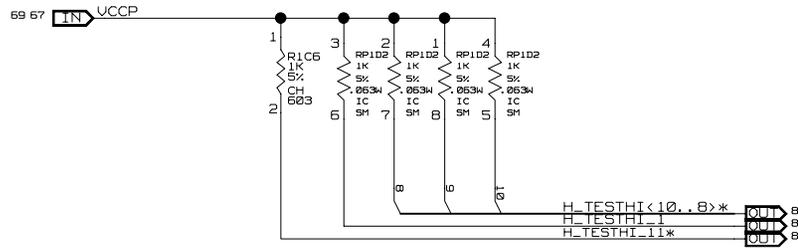


I/P/TAP TERMINATION

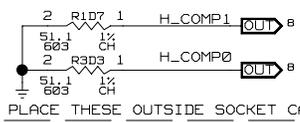


CAD NOTE: PLACE THESE RESISTORS CLOSE TO THE CPU SOCKET

TESTHI PULLUPS

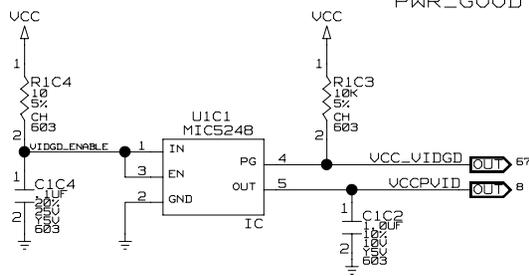


PRECISION FSB COMPENSATION RESISTORS



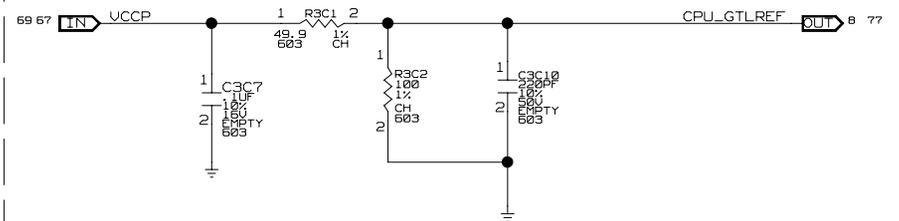
PLACE THESE OUTSIDE SOCKET CAVITY

PWR_GOOD



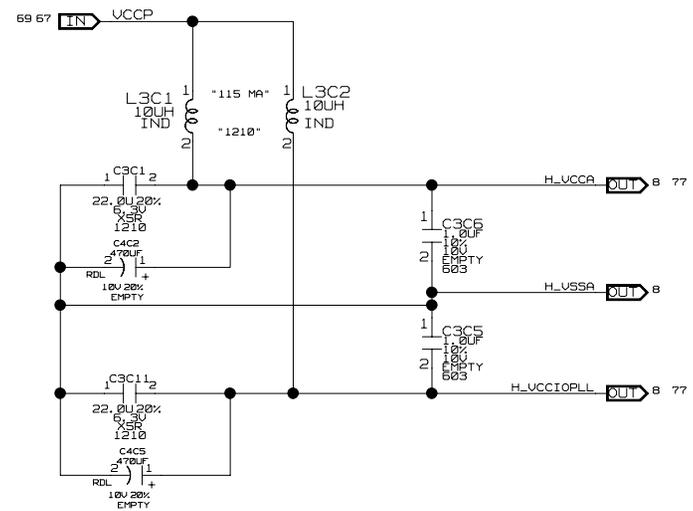
PLACE NEAR PIN 5

GTLREF GENERATION CIRCUITS



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: CPU PULLUPS/PULLDNS/TERMINATION	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 9

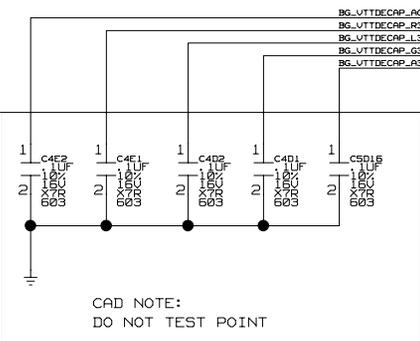
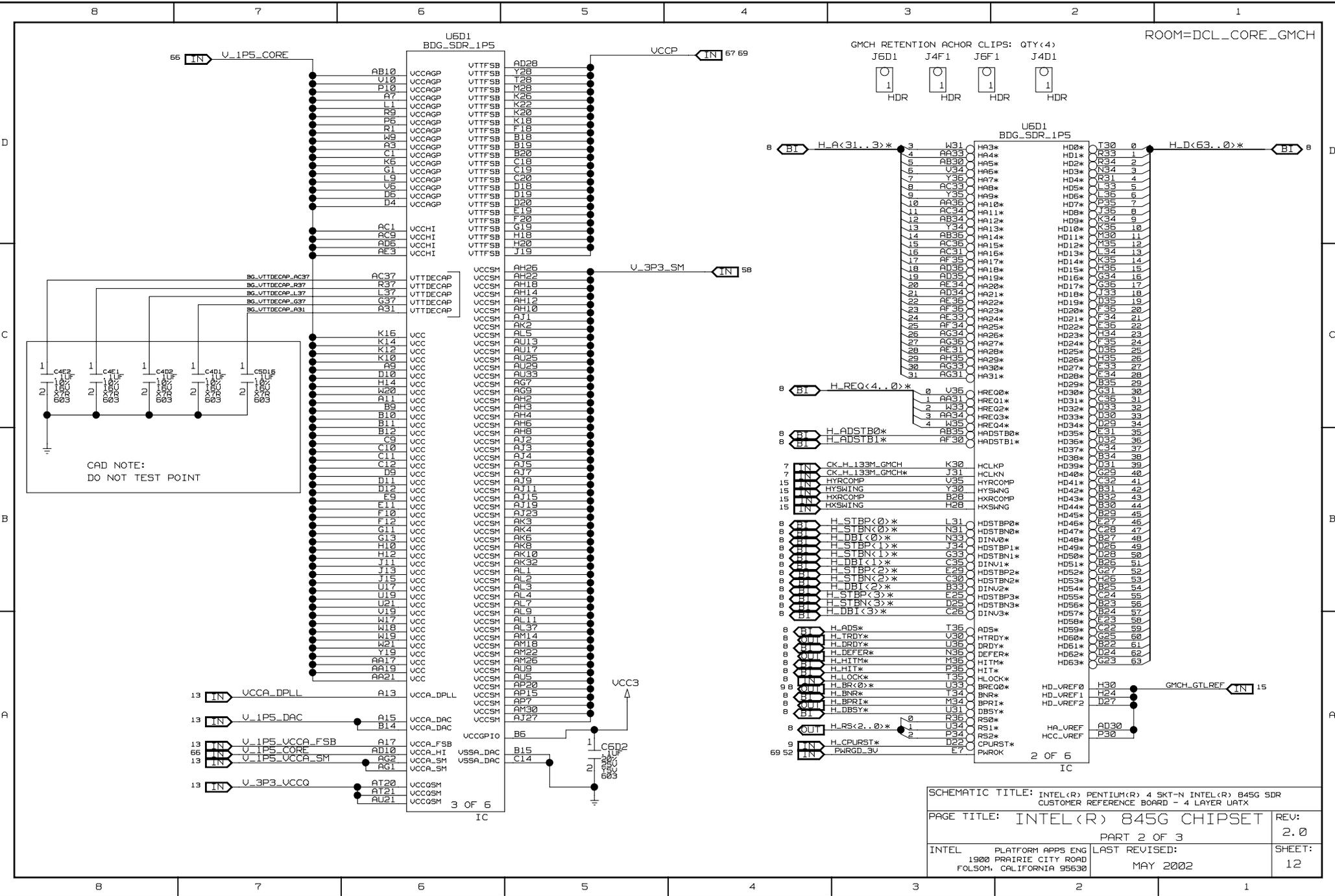
PLL SUPPLY FILTER



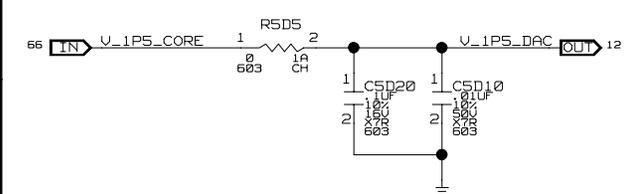
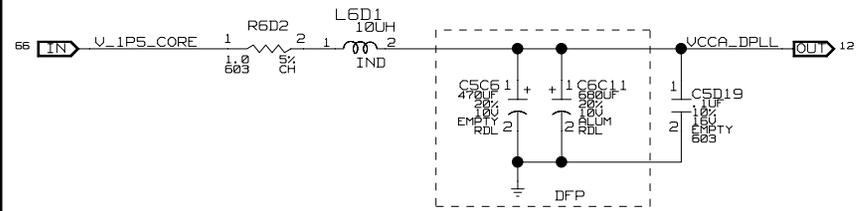
CAD NOTE:
 PLACE THMT CAPS OUTSIDE RM BOUNDARY.
 TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MIL
 CAD NOTE: PLACE COMPONENTS AS CLOSE AS POSSIBLE TO
 PROCESSOR SOCKET

FILTERED ANALOG SUPPLY

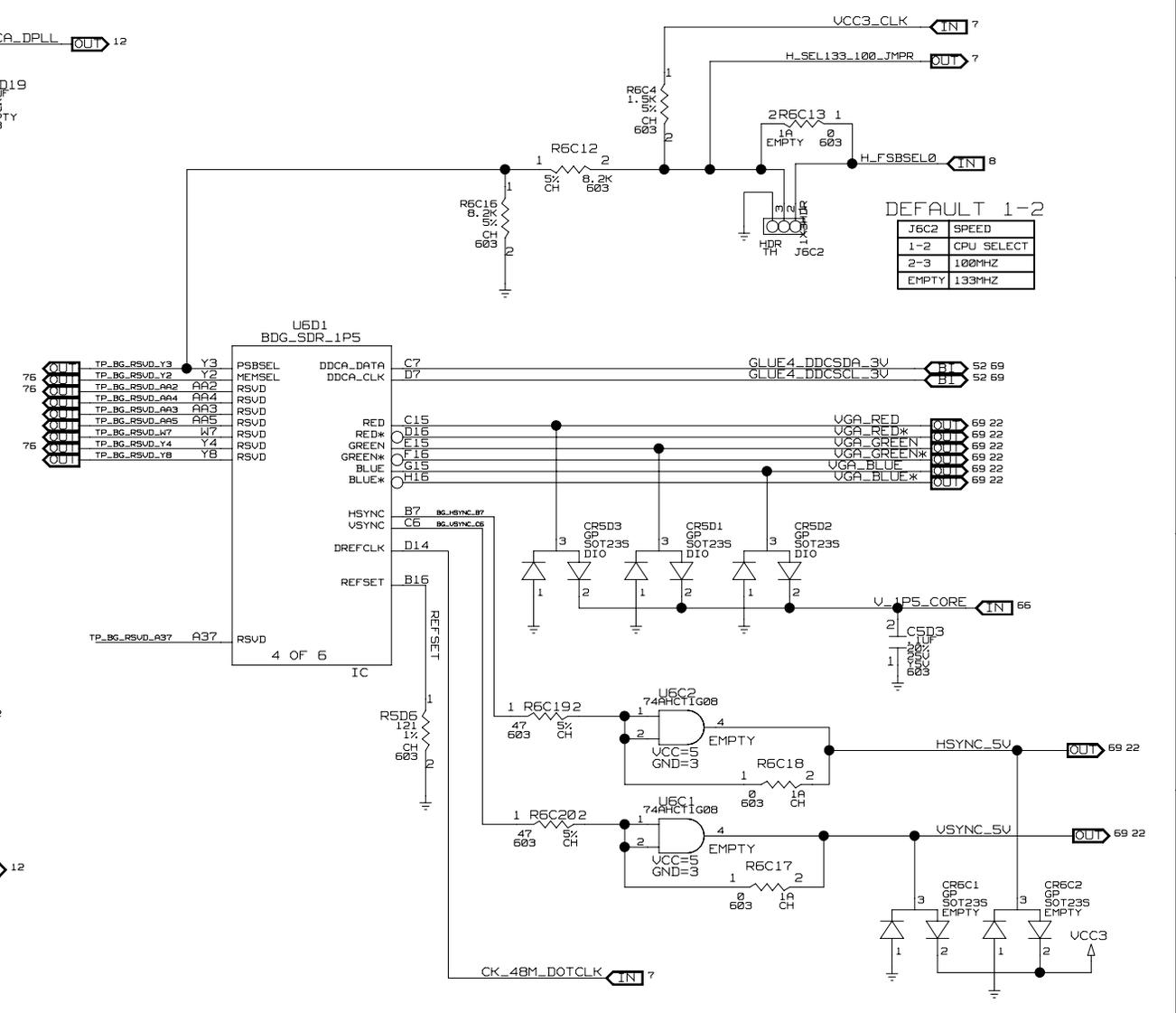
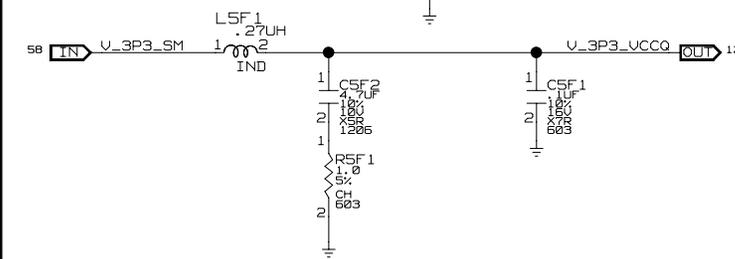
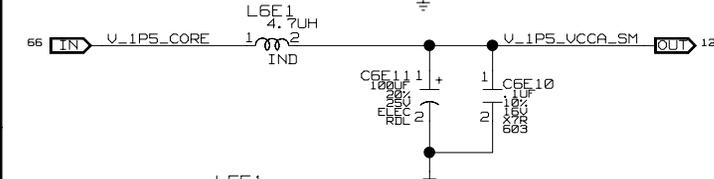
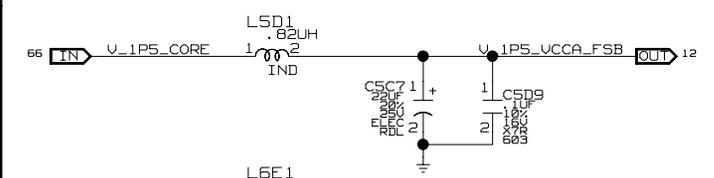
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	FILTERED ANALOG SUPPLY	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 10



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR
 CUSTOMER REFERENCE BOARD - 4 LAYER UATX
 PAGE TITLE: INTEL(R) 845G CHIPSET
 PART 2 OF 3
 INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
 LAST REVISED: MAY 2002
 REV: 2.0
 SHEET: 12



ANALOG FILTERS



DEFAULT 1-2

J6C2	SPEED
1-2	CPU SELECT
2-3	100MHZ
EMPTY	133MHZ



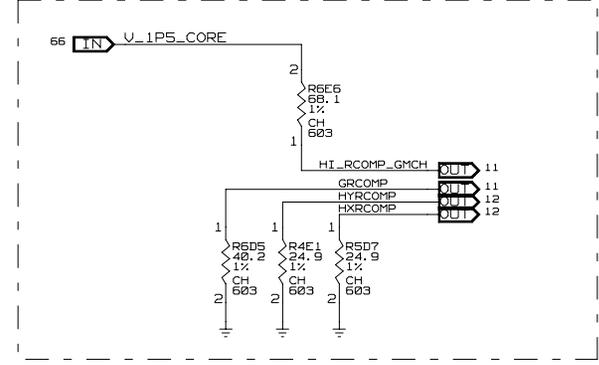
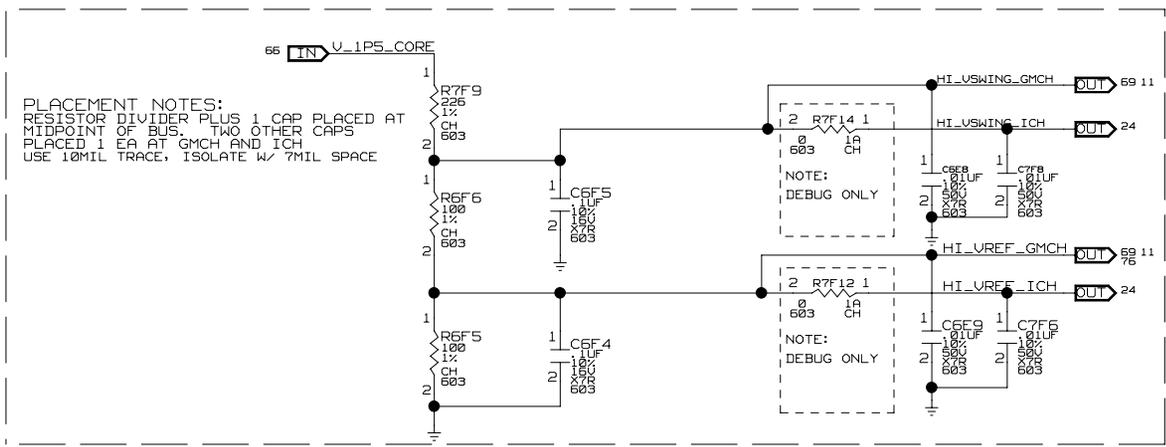
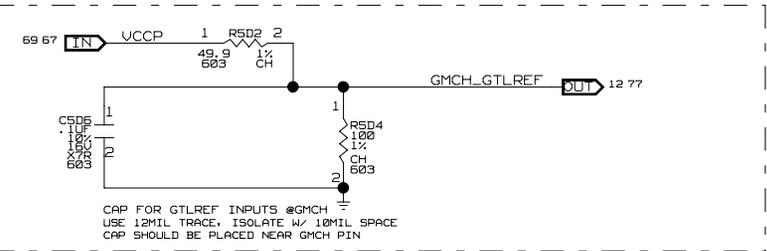
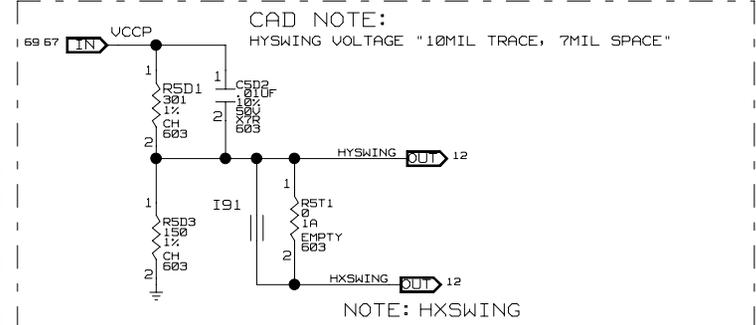
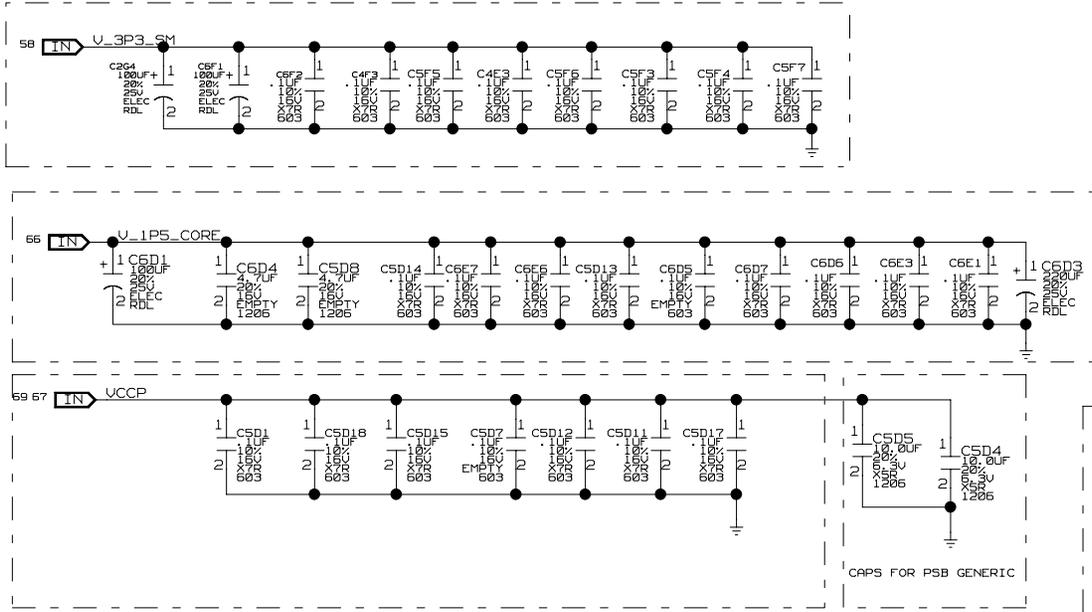
NOTE:
 THIS PAGE IS ONLY FOR FOOTPRINT
 COMPATIBILITY WITH THE REV 1.0
 BALLOUT. ALL CONNECTIONS HAVE
 BEEN REMOVED IN THE REV 2.0 BALLOUT

GND=K24, K28, M10, P28, T10, V28, Y10, AB28, AF28, AH16, AH20, AH24, AH28, AU35, AU31, AU27, AU23, AU15
 GND=AU11, AU7, AU3, AT36, AT2, AR37, AR35, AR33, AR31, AR29, AR27, AR25, AR23, AR21, AR19, AR17, AR15, AR13, AR9, AR7
 GND=AR5, AR3, AR1, AN37, AN35, AN33, AN7, AN5, AN3, AN1, AM32, AM28, AM24, AM20, AM16, AM12, AM10, AM6, AM5, AM4, AM3, AL35
 GND=AL31, AL27, AK12, AJ37, AJ33, AJ29, AJ25, AJ21, AJ17, AJ13, AH36, AH32, AH30, AG37, AG35, AG29, AG5, AG4, AG3, AF32
 GND=AF8, AF6, AE37, AE35, AE29, AE9, AE1, AD32, AC35, AC29, AC3, AB32, AB6, AB4, AA37, AA35, AA29, AA20, AA18, AA9, AA1
 GND=Y32, Y21, Y20, Y18, Y17, Y6, W36, W34, W29, W3, U32, V21, V20, V18, V17, U37, U35, U29, U20, U18, U9, U3, U1, T32, T6, R35
 GND=R29, R9, P32, N37, N35, N29, N9, N3, N1, M32, M6, L35, L29, L3, K32, J37, J35, J29, J27, J25, J23, J21, J17, J9, J3, J1, H32
 GND=H22, H6, G35, G21, G17, G8, G3, F32, F30, F28, F25, F24, F22, F14, F8, F6, E37, E35, E21, E17, E13, E3, E1, D34, D23, D21
 GND=D17, D15, D13, D8, C37, C33, C31, C29, C27, C25, C23, C21, C17, C16, C13, C8, C5, B36, B17, B21, B13, B8, B2, A35, A33, A29, A27, A25, A23, A21, A5

CAUTION: .
 THIS VERSION OF THE SDR SCHEMATICS CONTAINS AN OLD GMCH BALLOUT, BALLOUT 1.5.
 BOARD DESIGNERS SHOULD OPTIMIZE FOR THE BALLOUT 2.0.
 ADDITIONAL BALLOUT INFORMATION CAN BE FOUND IN THE LATEST REVISION OF THE
 INTEL(R) 845G/845GL GMCH DATASHEET.
 NO PLANS CURRENTLY EXIST TO UPDATE THE SDR SCHEMATICS WITH THE GMCH BALLOUT 2.0.

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX			
PAGE TITLE: 1.5 GMCH BALLOUT			REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: MAY 2002	SHEET: 14

SYSTEM MEMORY DECOUPLING

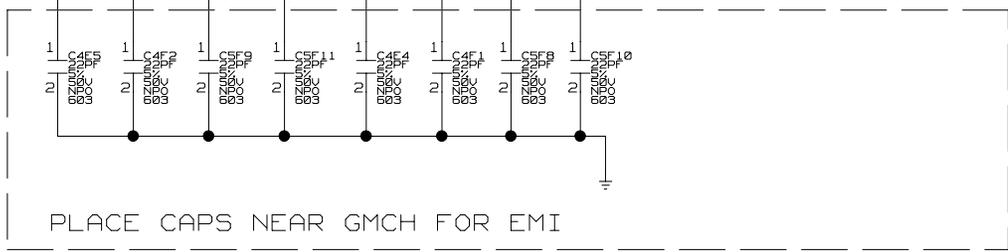


CHIPSET DECOUPLING, STRAPPING

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G 5DR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: DECOUPLING AND REF VOLTAGES	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 15

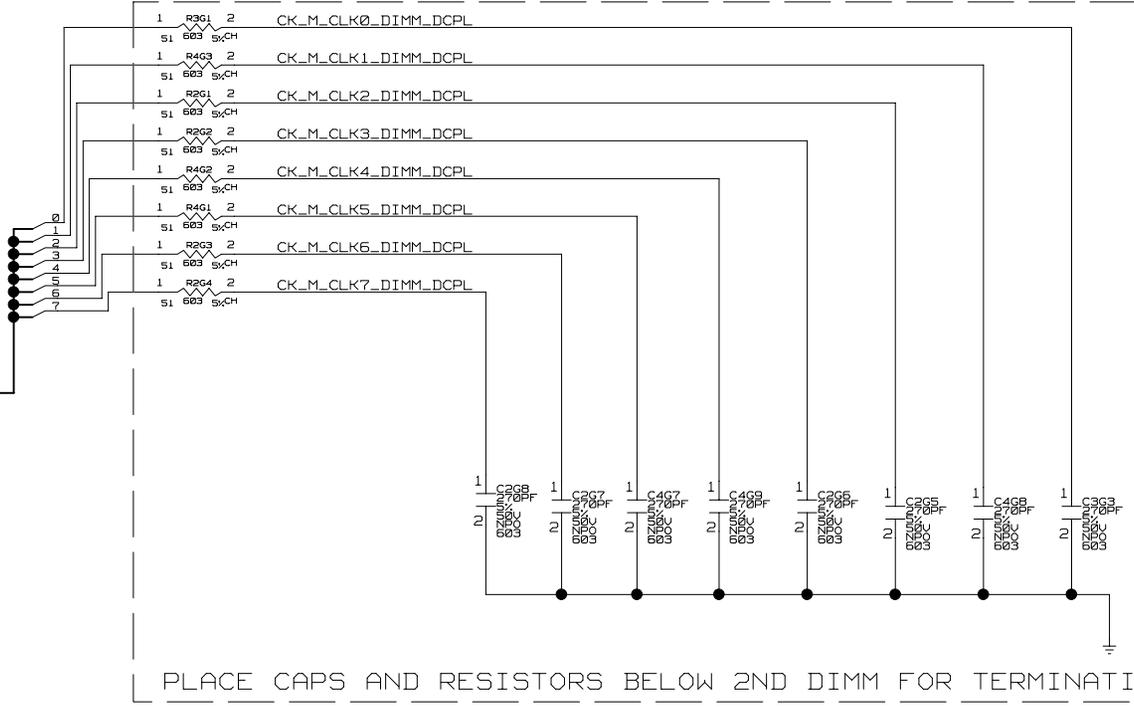
8 7 6 5 4 3 2 1

11 IN CK_M_133M_SDR<7..0>



PLACE CAPS NEAR GMCH FOR EMI

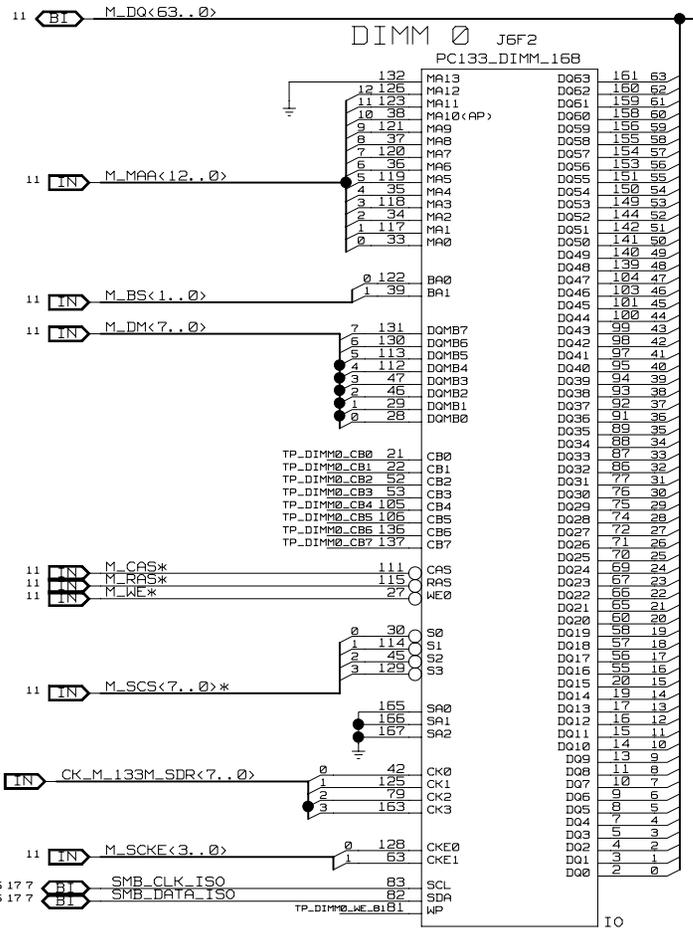
11 IN CK_M_133M_SDR<7..0>



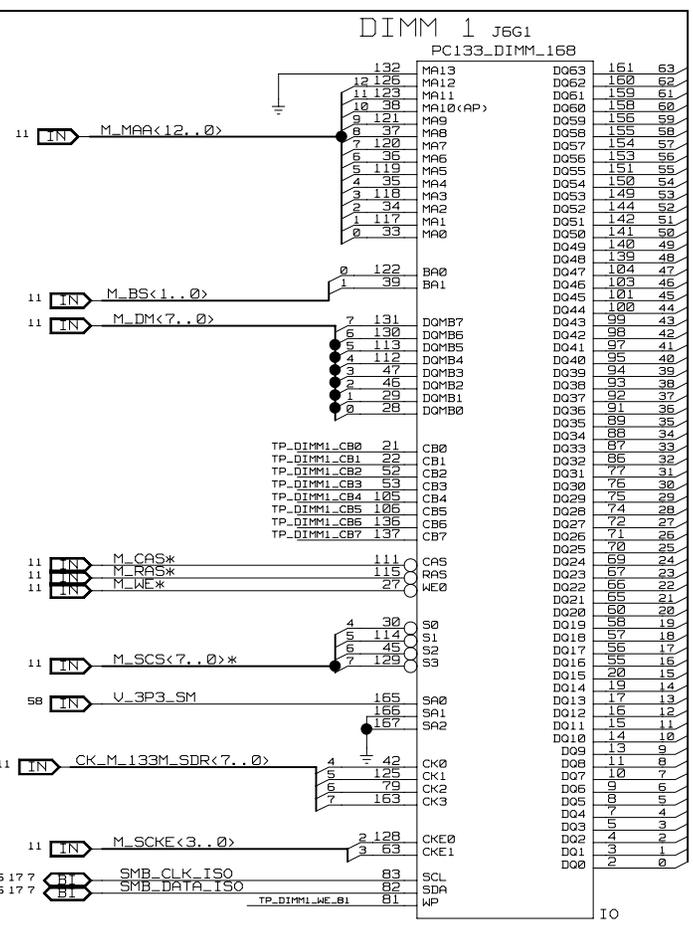
PLACE CAPS AND RESISTORS BELOW 2ND DIMM FOR TERMINATION

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: DIMM TERMINATION/DECOUPLING		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 16

8 7 6 5 4 3 2 1



UCC=V_3P3_SM
SMB ADDR = 0000000



UCC=6, 18, 26, 40, 41, 49, 59, 73, 84, 90
UCC=102, 110, 124, 133, 143, 157, 168
GND=1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96
NC=24, 25, 31, 44, 48, 50, 51, 61, 62, 80, 108, 109, 134, 135, 145, 146, 147, 164, 169, 170, 171
SMB ADDR = 0000001

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: DIMM CONNECTORS		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 17

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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE:	BLANK	REV:	2.0
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INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG	LAST REVISED: MAY 2002	SHEET: 18
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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE:	BLANK	REV:	2.0
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INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG	LAST REVISED:	MAY 2002	SHEET:	19
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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: BLANK
REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002
1900 PRAIRIE CITY ROAD SHEET: 20
FOLSOM, CALIFORNIA 95630

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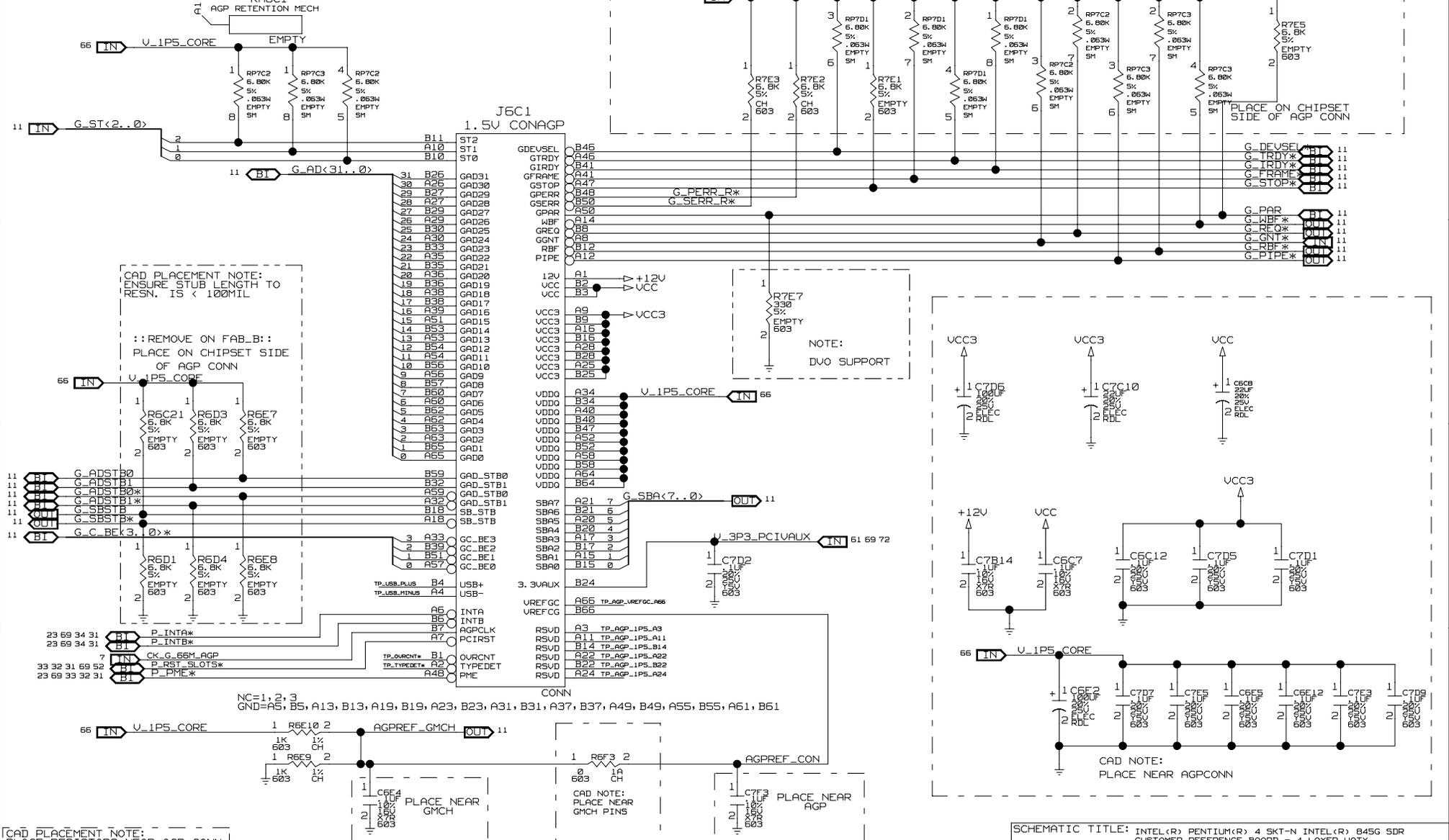
4

3

2

1

ROOM=DCL_CORE_AGP OPTION TO STUFF AT ALTERED ASSEMBLY LEVEL



CAD PLACEMENT NOTE:
ENSURE STUB LENGTH TO
RESN. IS < 100MIL

:: REMOVE ON FAB.B ::
PLACE ON CHIPSET SIDE
OF AGP CONN

CAD PLACEMENT NOTE:
PLACE RESISTORS NEAR AGP CONN

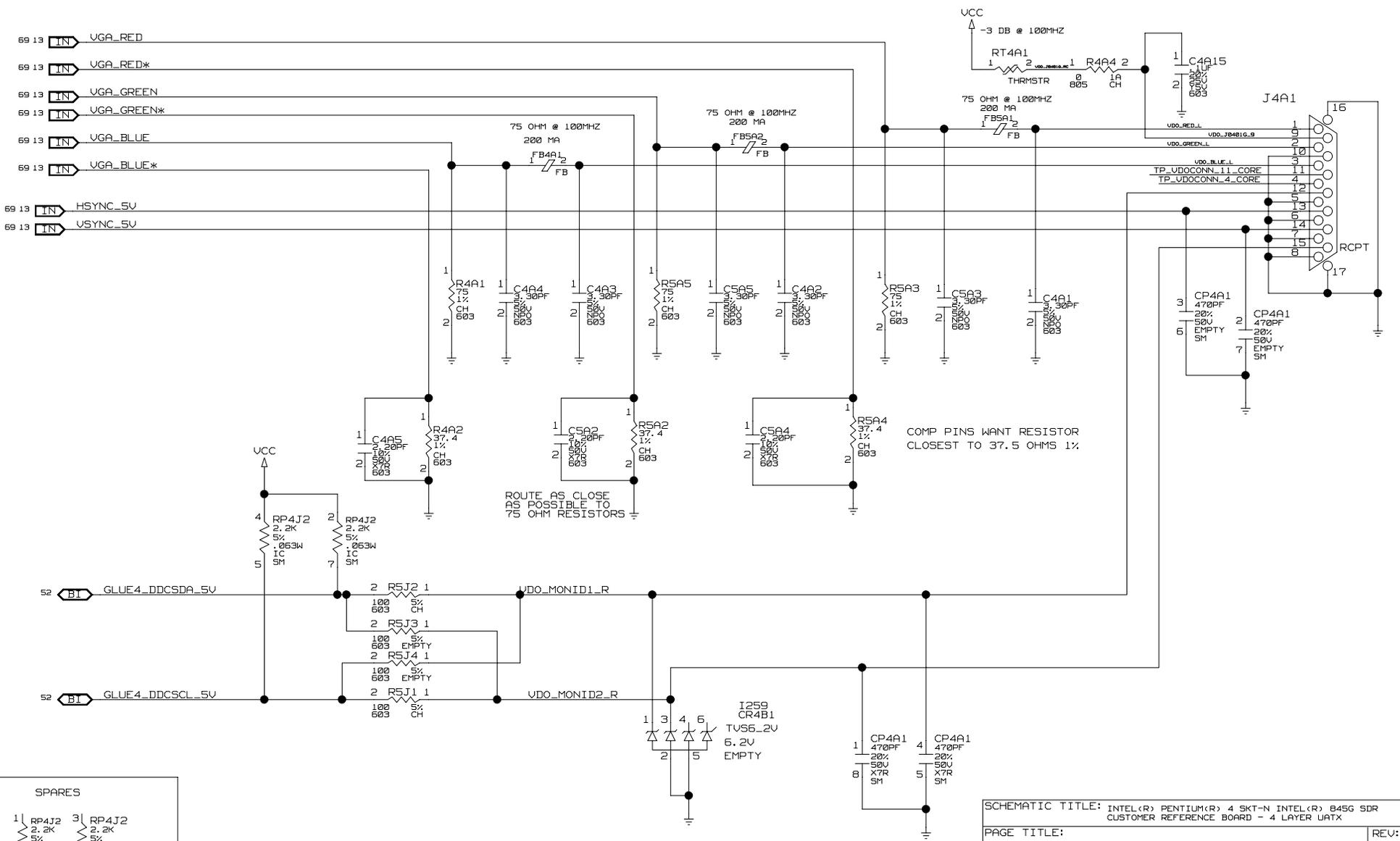
NOTE:
DVO SUPPORT

CAD NOTE:
PLACE NEAR AGP CONN

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: AGP REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002 SHEET: 21
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630



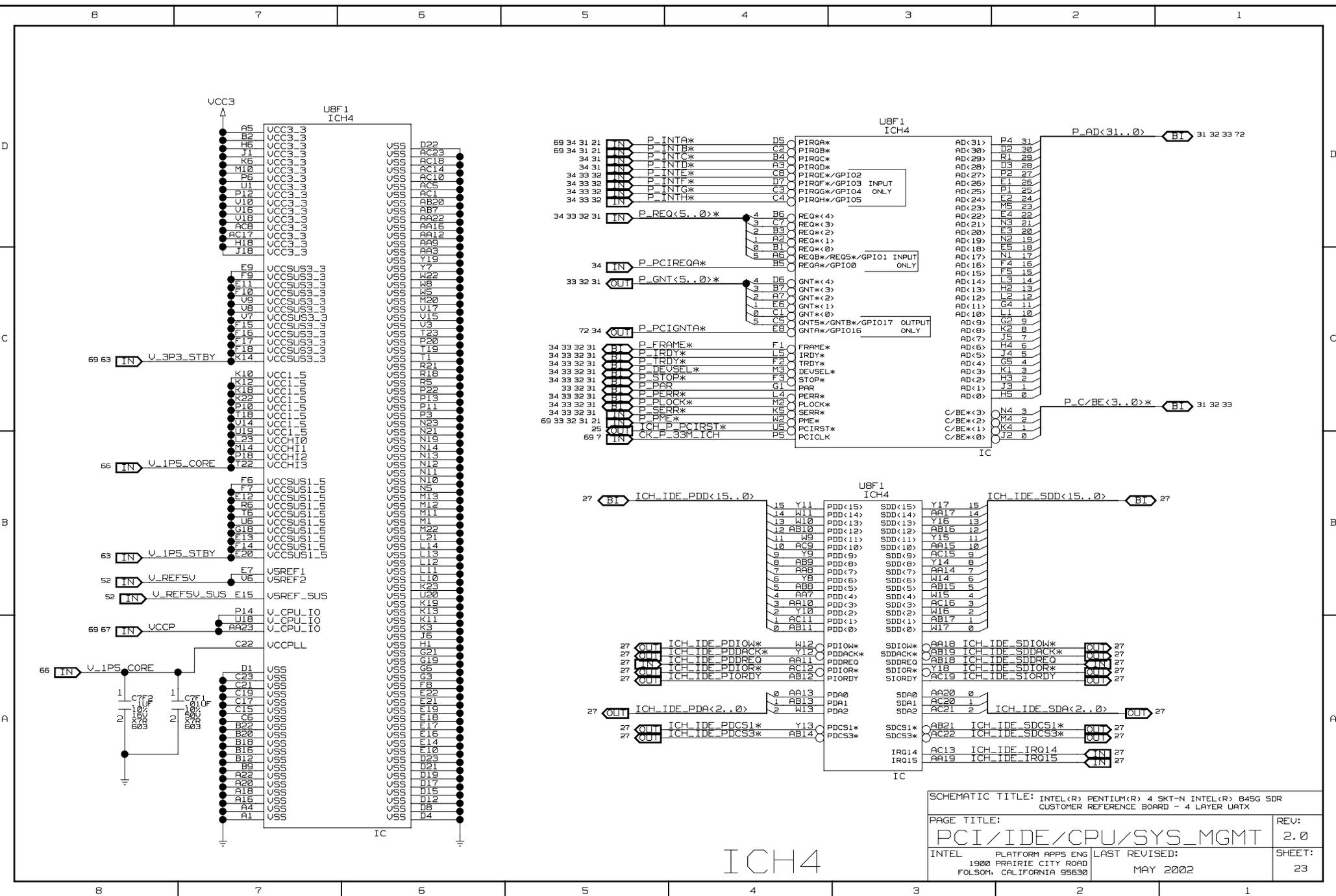
SPARES

1	RP4J2	3	RP4J2
	2.2K		2.2K
	5%		5%
	.063W		.063W
	1C		1C
B1	SM	B1	SM

COMP PINS WANT RESISTOR
CLOSEST TO 37.5 OHMS 1%

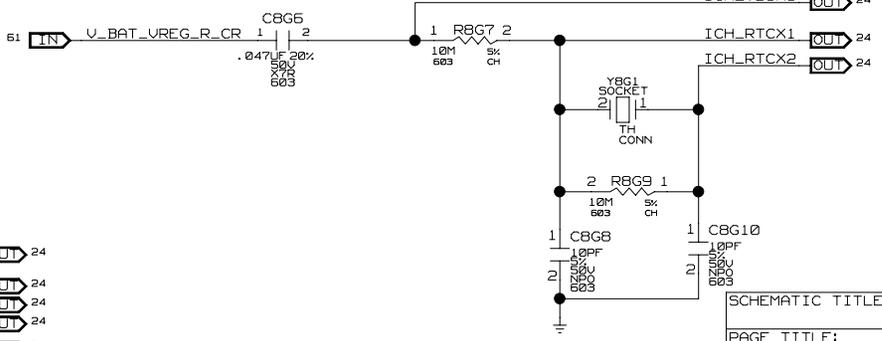
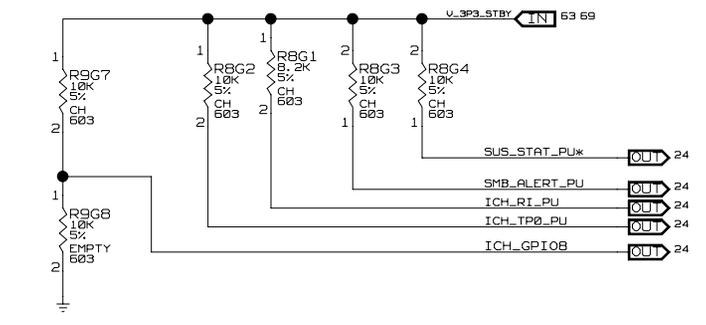
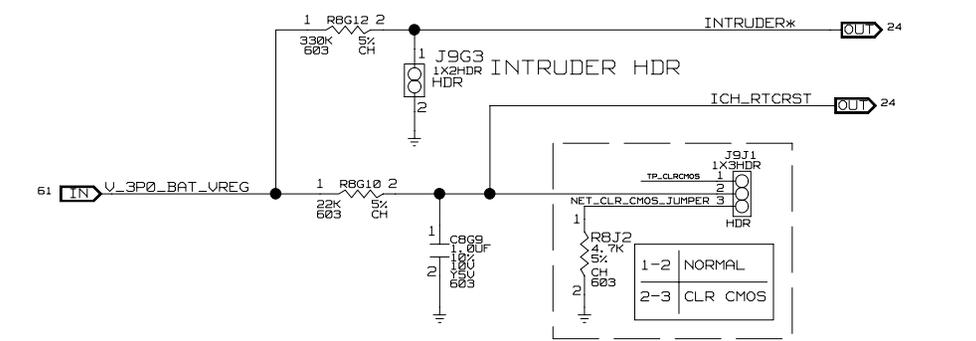
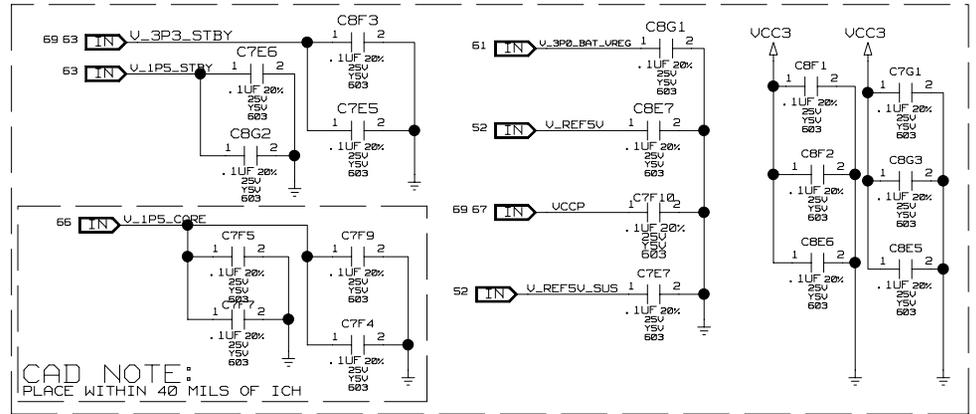
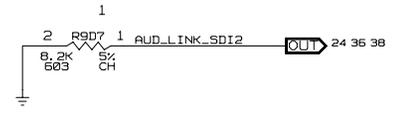
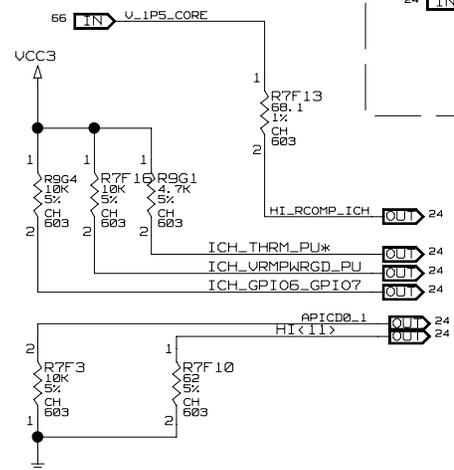
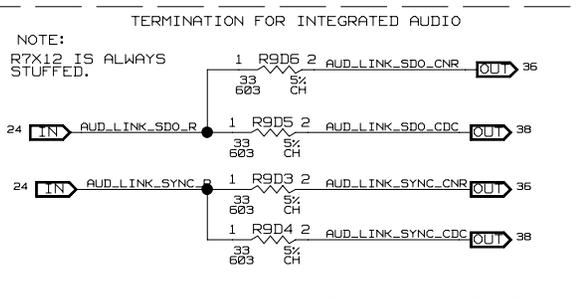
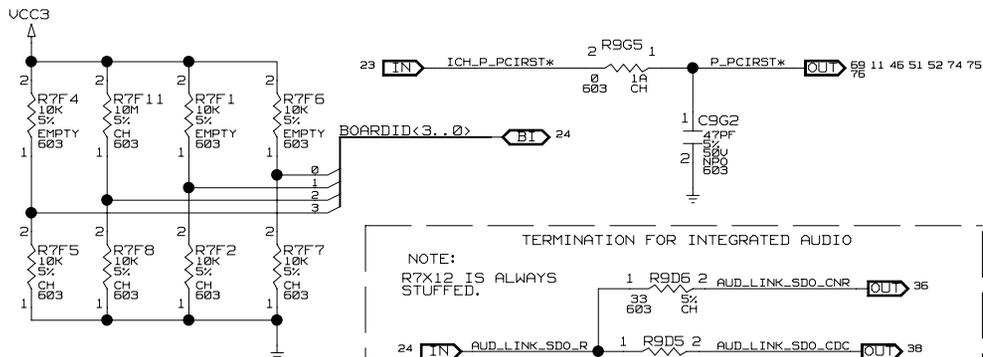
ROUTE AS CLOSE
AS POSSIBLE TO
75 OHM RESISTORS

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: VGA CONNECTOR	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002 SHEET: 22



ICH4

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: PCI/IDE/CPU/SYS_MGMT		REV: 2.0
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 23



SCHMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: ICH PULLUPS & DECOUPLING

REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002 SHEET: 25

1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

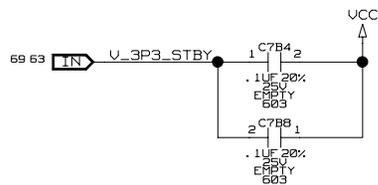
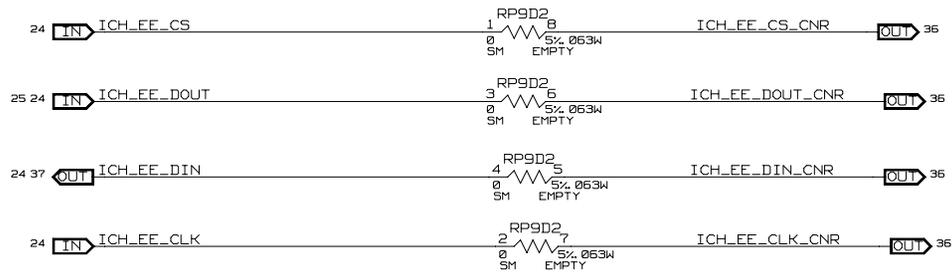
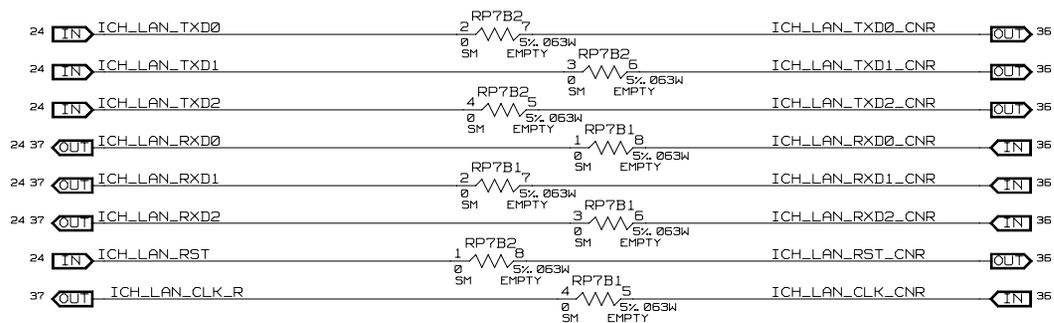
ICH4

ICH AND CNR LINK

CAD NOTE:

PLACE THESE R-PACKS UNDERNEATH
THE LAN CHIP, RIGHT BY THE PINS TO
MINIMIZE STUB FROM PIN TO R-PACK

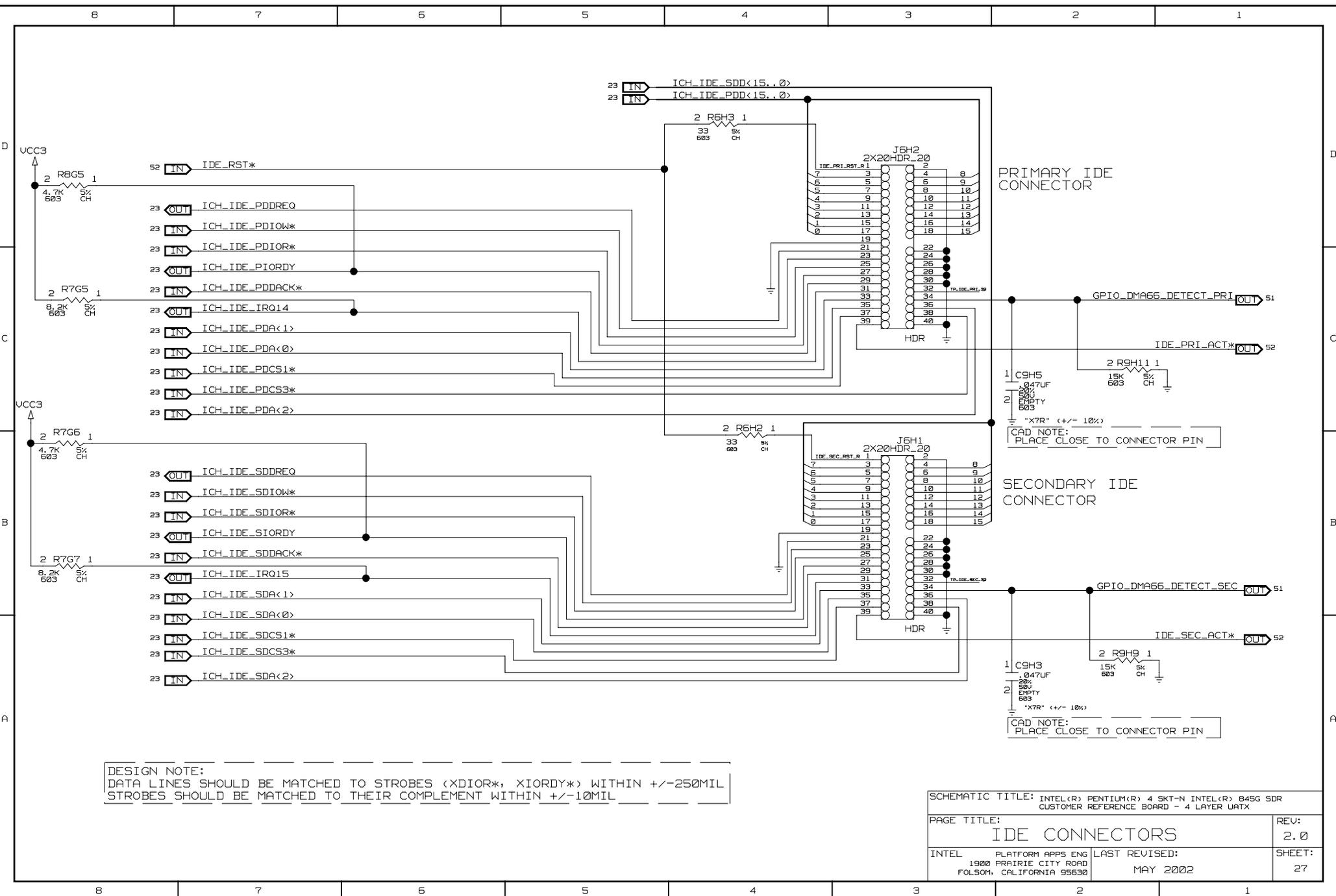
CNR OPTION FOR LAN-UP SOLUTION



0-OHMS ARE PROVIDED
TO MINIMIZE STUBS
ON LAN INTERFACE

ICH_360

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: ICH: CNR LAN LINK		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 25



PRIMARY IDE CONNECTOR

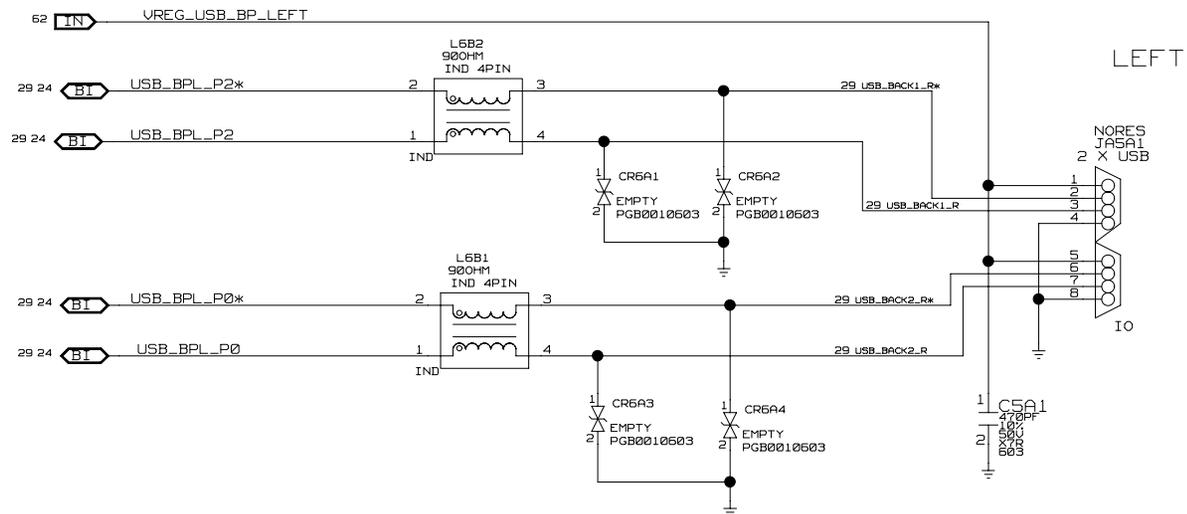
SECONDARY IDE CONNECTOR

CAD NOTE:
PLACE_CLOSE_TO_CONNECTOR_PIN

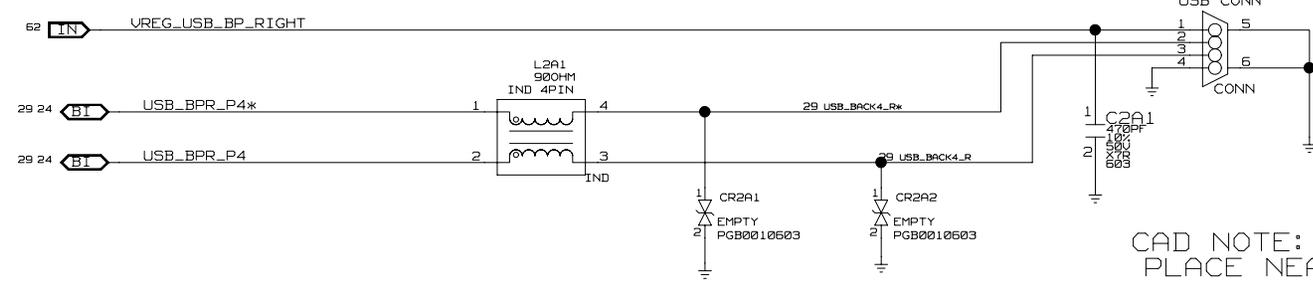
CAD NOTE:
PLACE_CLOSE_TO_CONNECTOR_PIN

DESIGN NOTE:
DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR*, XIORDY*) WITHIN +/-250MIL
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/-10MIL

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX			
PAGE TITLE: IDE CONNECTORS			REV: 2.0
INTEL	PLATFORM APPS ENG	LAST REVISED: MAY 2002	SHEET: 27



LEFT



RIGHT

CAD NOTE:
PLACE NEAR USB CONN

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: USB BACKPANEL		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 28

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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE:	BLANK	REV:	2.0
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INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG	LAST REVISED:	MAY 2002	SHEET:	29
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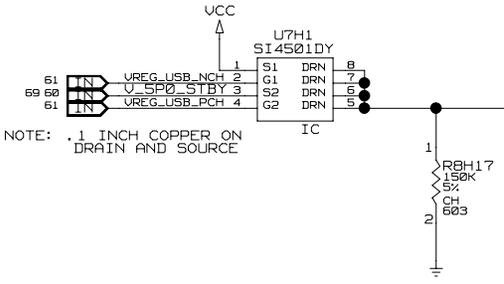
3

2

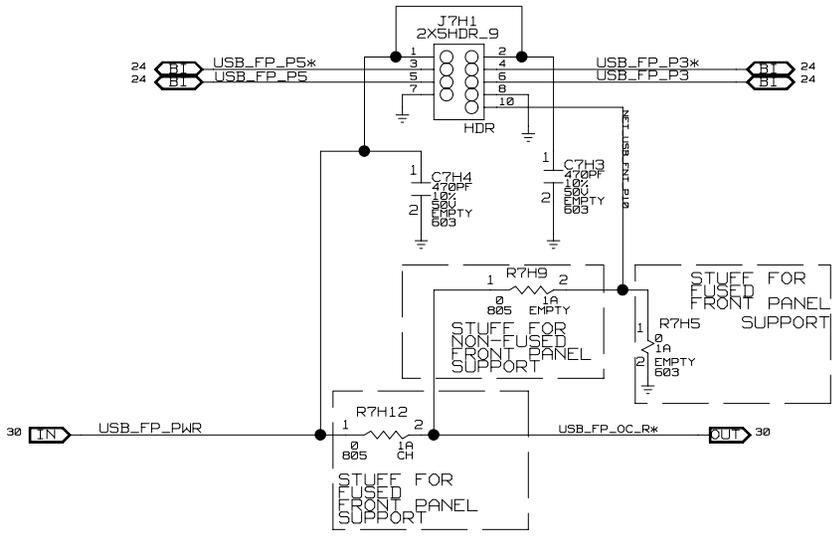
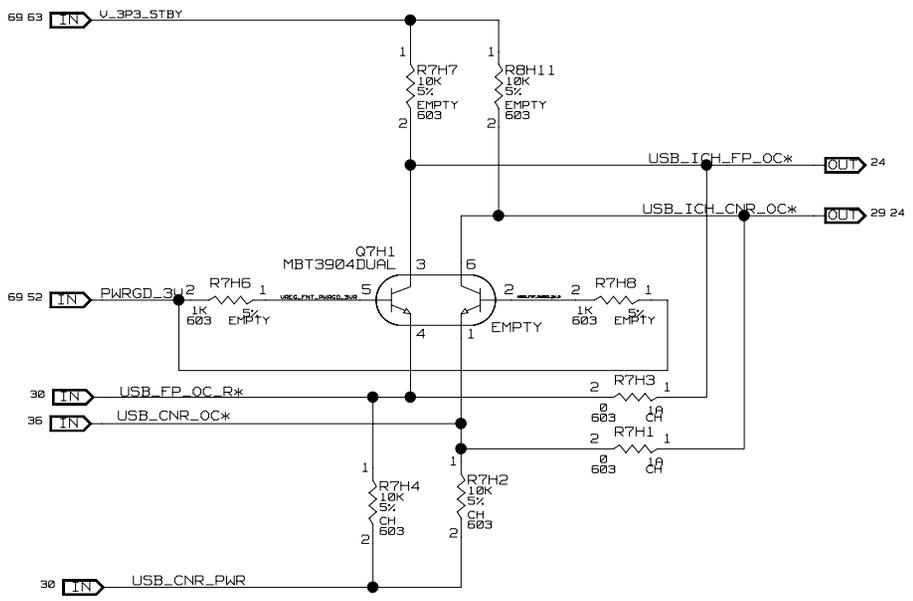
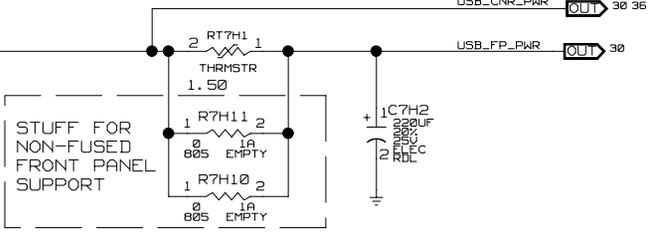
1

CAD NOTE:
TRACE ROUTING IS 7.5 MIL, 7.5 MIL SPACING

CAD NOTE: PLACE MIDWAY BETWEEN THE FPANEL (2X5) & CNR
RUN MUST HAVE 50 MIL POWER TO BOTH LOCATIONS.



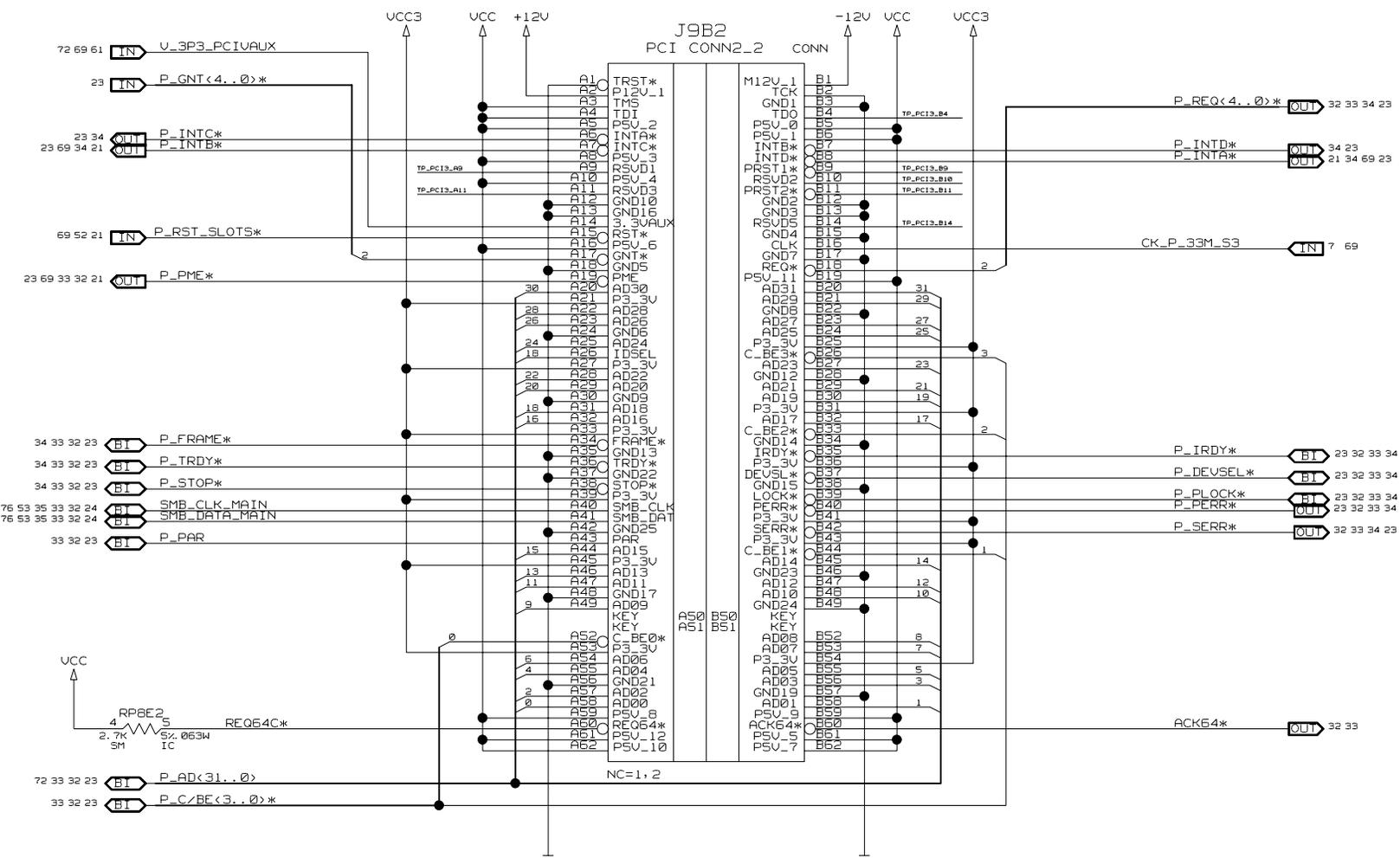
NOTE: .1 INCH COPPER ON DRAIN AND SOURCE



USB FNT PANEL POWER

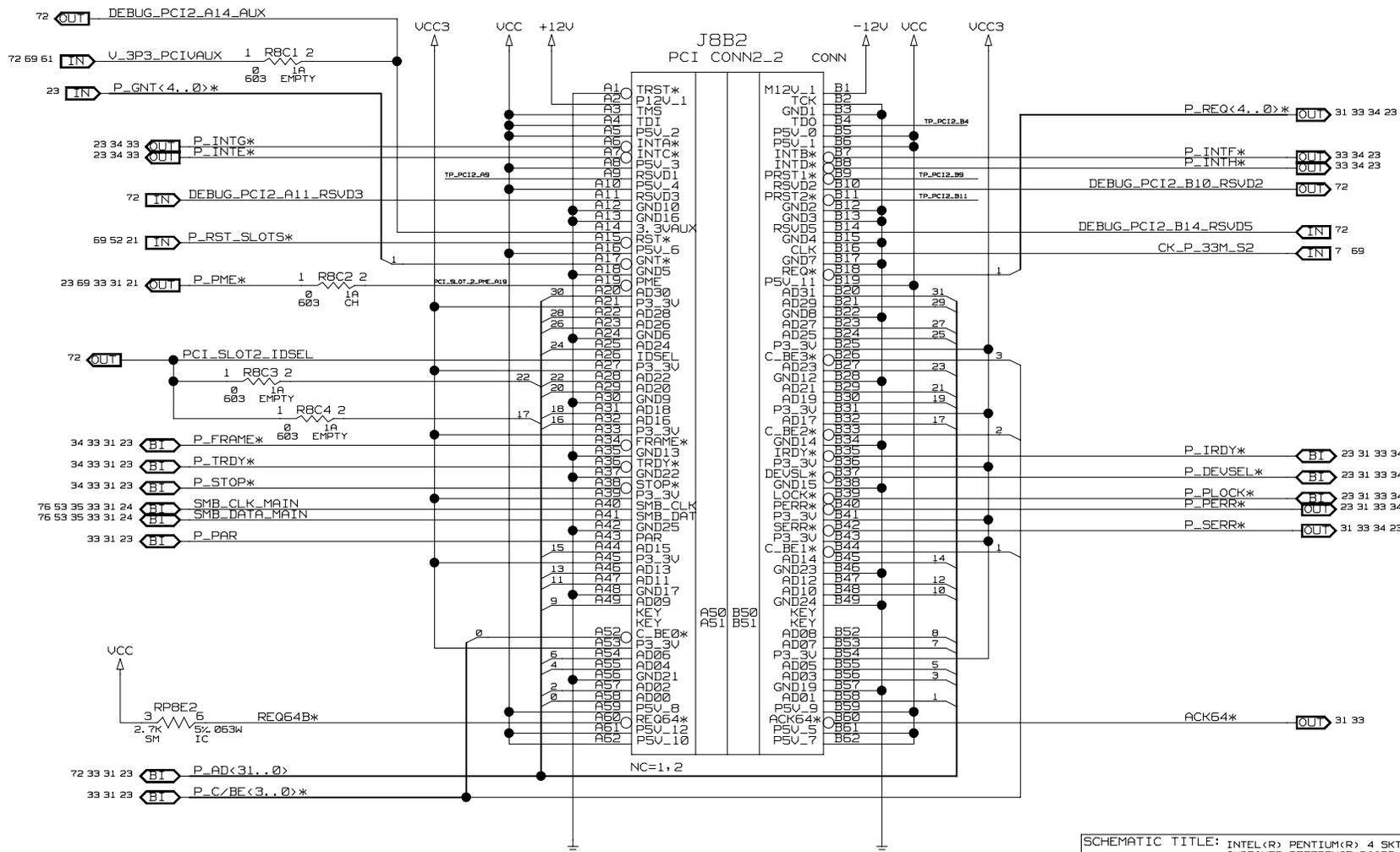
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: USB FRONT PANEL	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 30

PCI SLOT 3



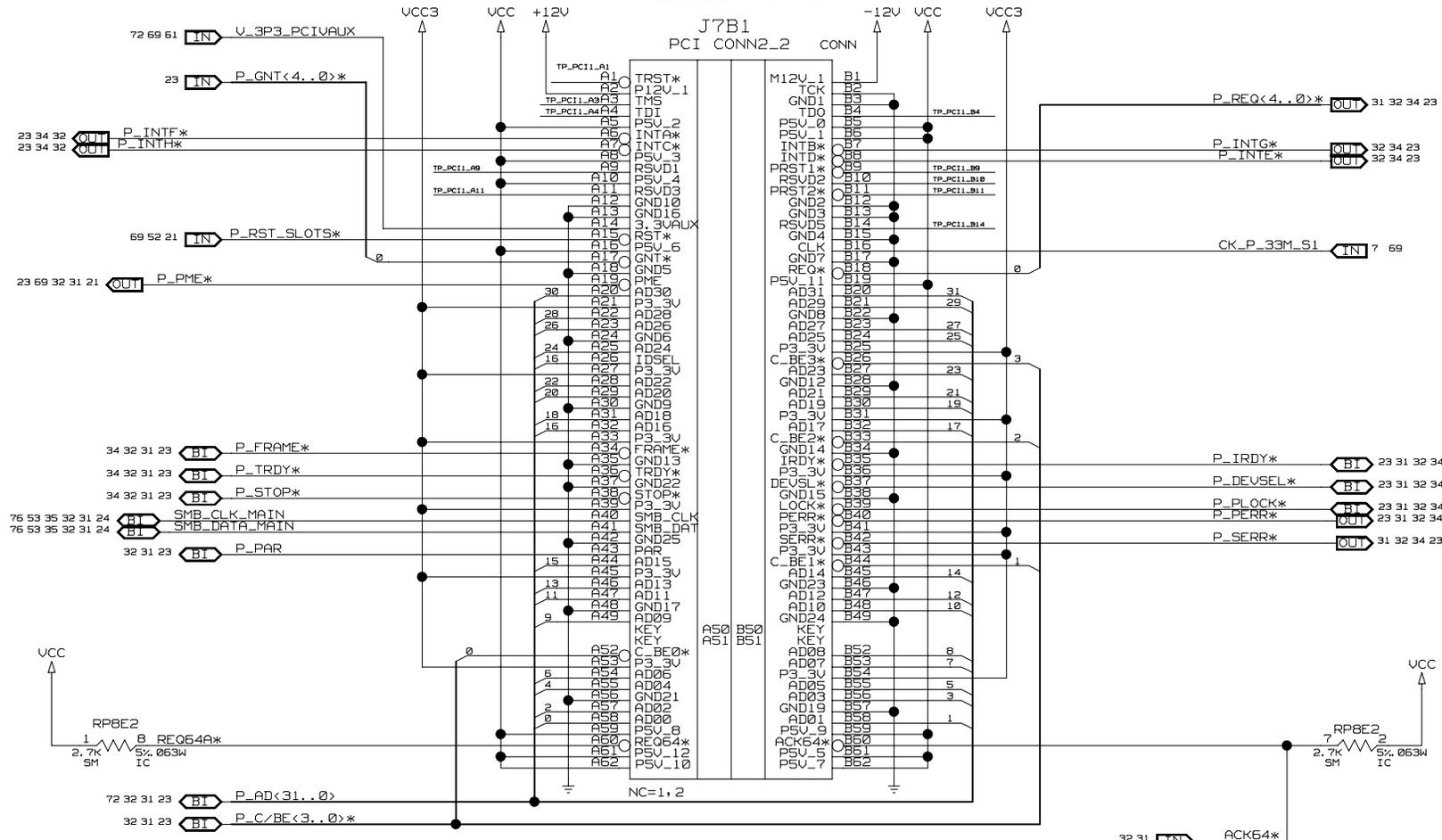
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PAGE TITLE: <b style="font-size: 1.5em;">PCI SLOT3		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 31

PCI SLOT 2

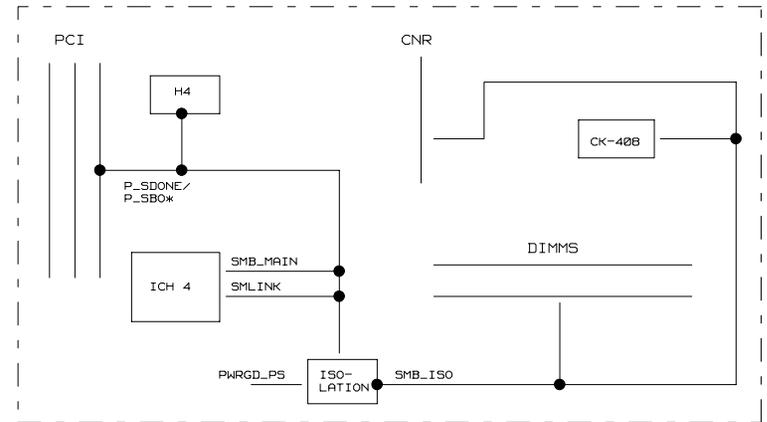
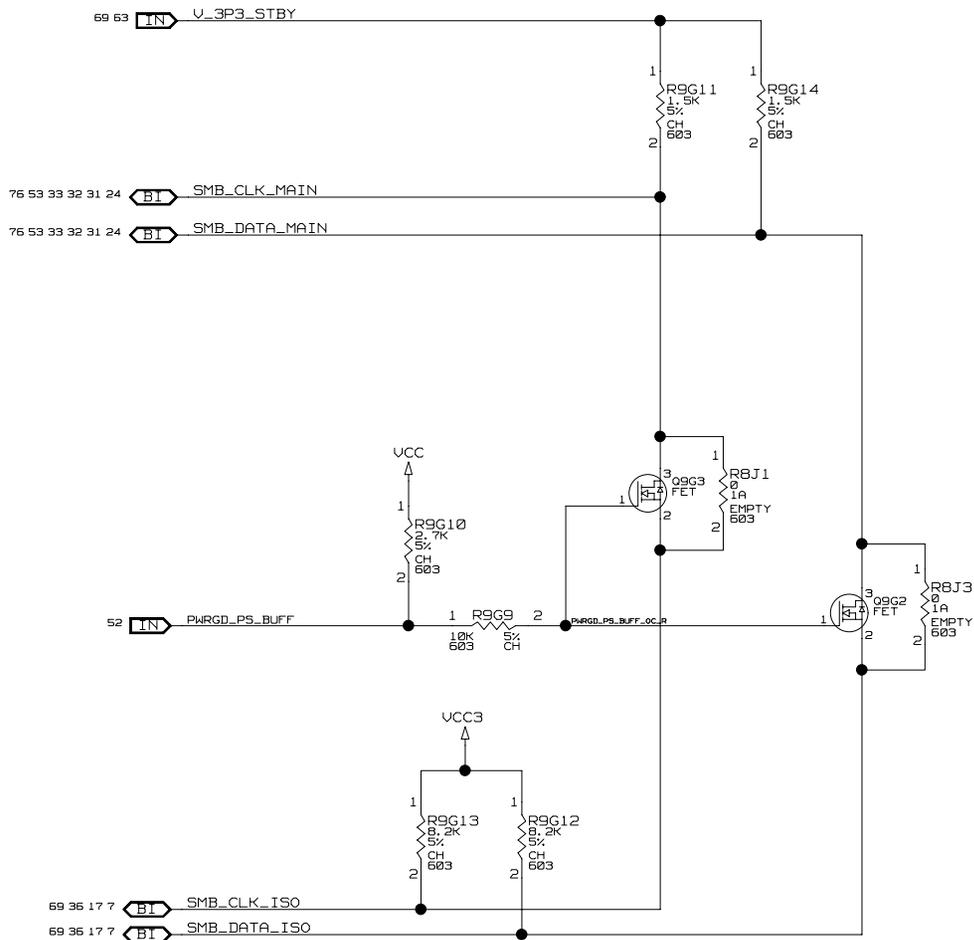


SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: PCI SLOT 2	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002 SHEET: 32

PCI SLOT 1
CLOSEST TO AGP



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX			
PAGE TITLE: PCI SLOT 1			REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: MAY 2002	SHEET: 33



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR
 CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: SMBUS_ISOLATION

REV:
2.0

INTEL PLATFORM APPS ENG
 1900 PRAIRIE CITY ROAD
 FOLSOM, CALIFORNIA 95630

LAST REVISED:
MAY 2002

SHEET:
35

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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX			
PAGE TITLE: BLANK		REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: MAY 2002	
		SHEET: 37	

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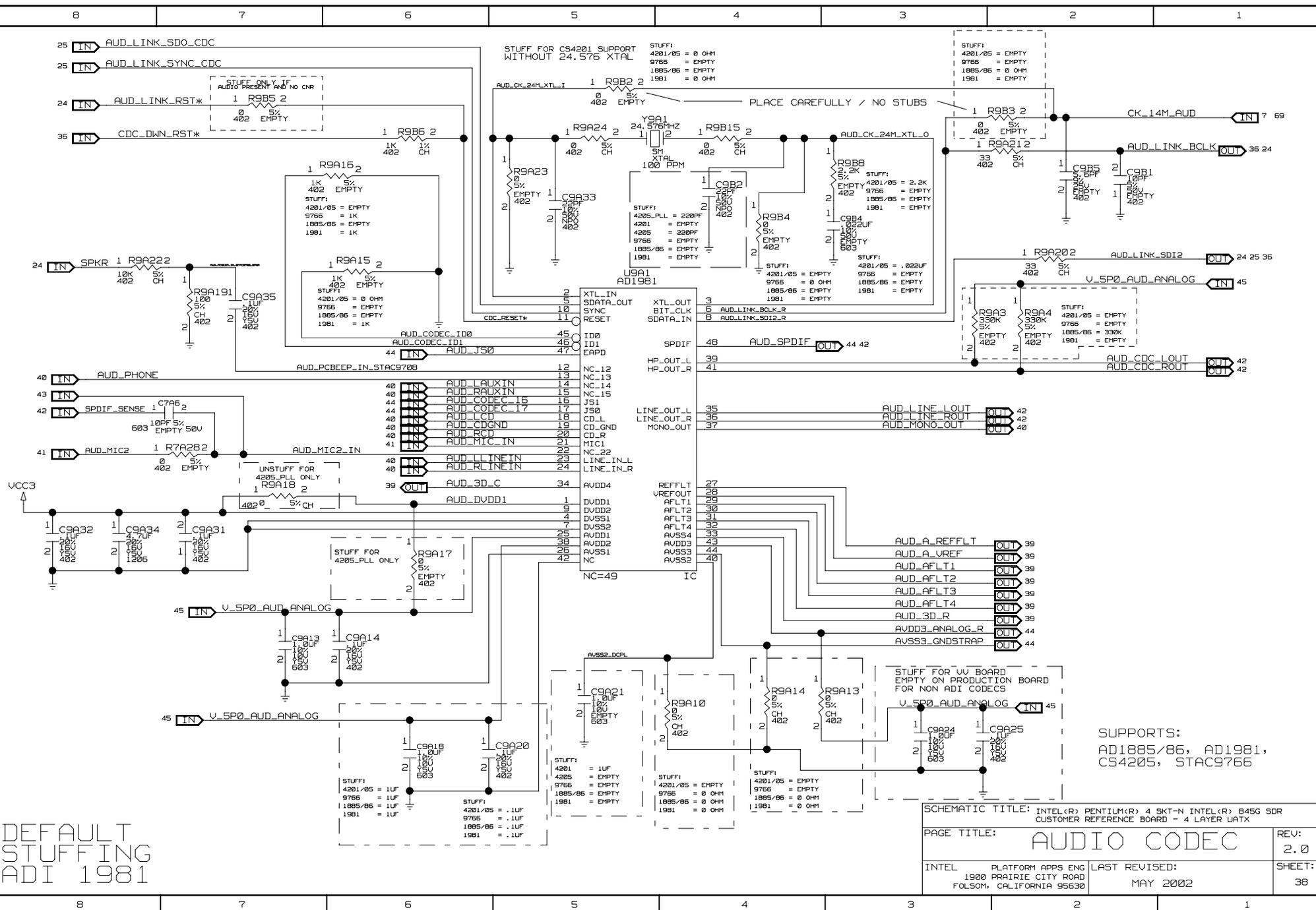
5

4

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2

1



DEFAULT
STUFFING
ADI 1981

STUFF1
4201/05 = .1UF
9766 = .1UF
1885/86 = .1UF
1981 = .1UF

STUFF1
4201/05 = .1UF
9766 = .1UF
1885/86 = .1UF
1981 = .1UF

STUFF1
4201/05 = 1UF
9766 = EMPTY
1885/86 = EMPTY
1981 = EMPTY

STUFF1
4201/05 = EMPTY
9766 = EMPTY
1885/86 = 0 OHM
1981 = EMPTY

STUFF1
4201/05 = EMPTY
9766 = EMPTY
1885/86 = 0 OHM
1981 = 0 OHM

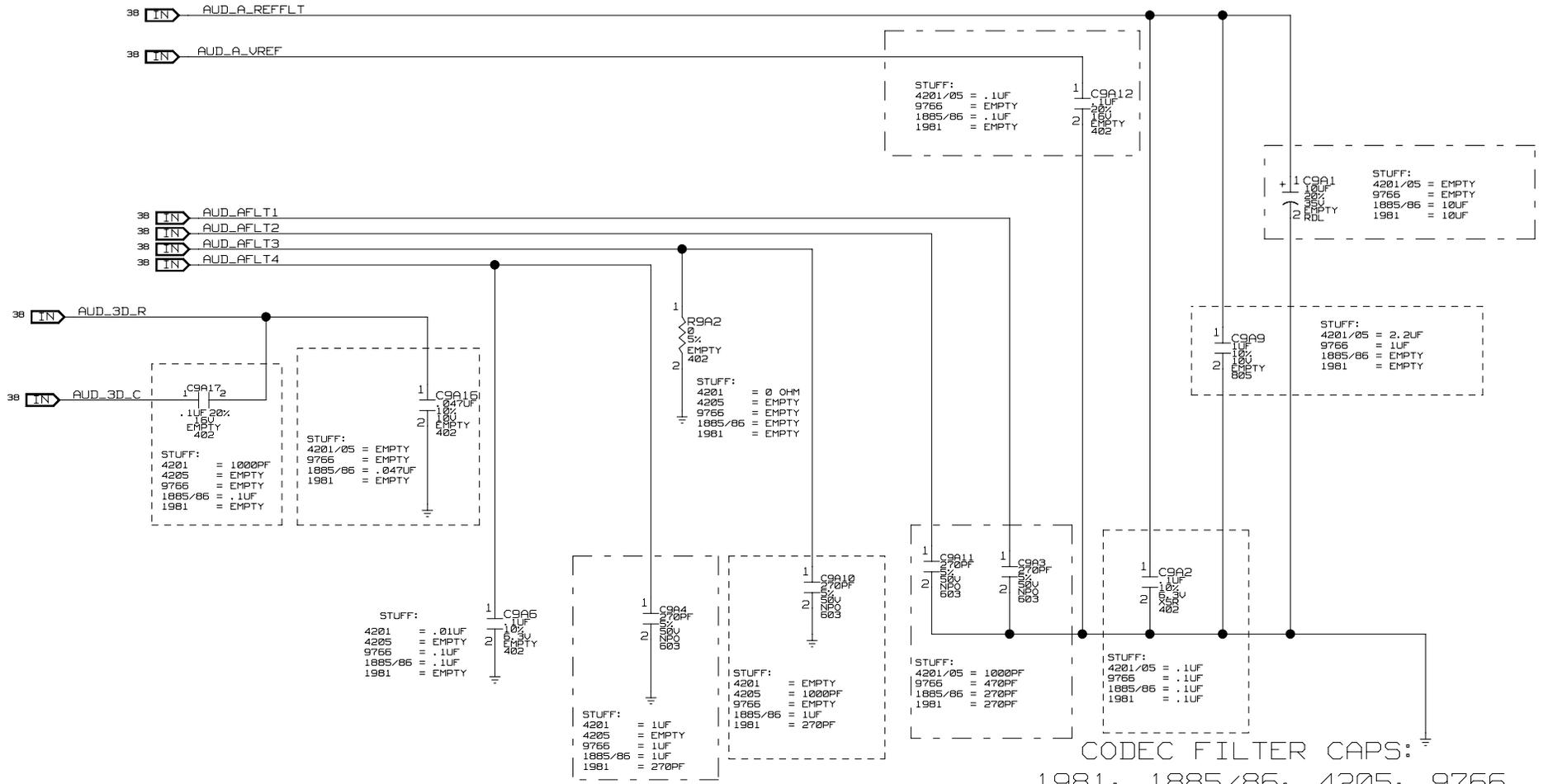
STUFF1
4201/05 = EMPTY
9766 = EMPTY
1885/86 = 0 OHM
1981 = 0 OHM

SCHMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: **AUDIO CODEC** REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002 SHEET: 38
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

KEEP CAPS AS CLOSE
AS POSSIBLE TO AC97
CODEC.

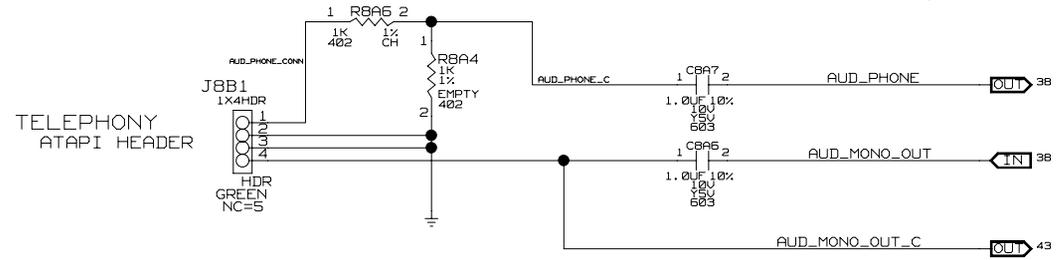
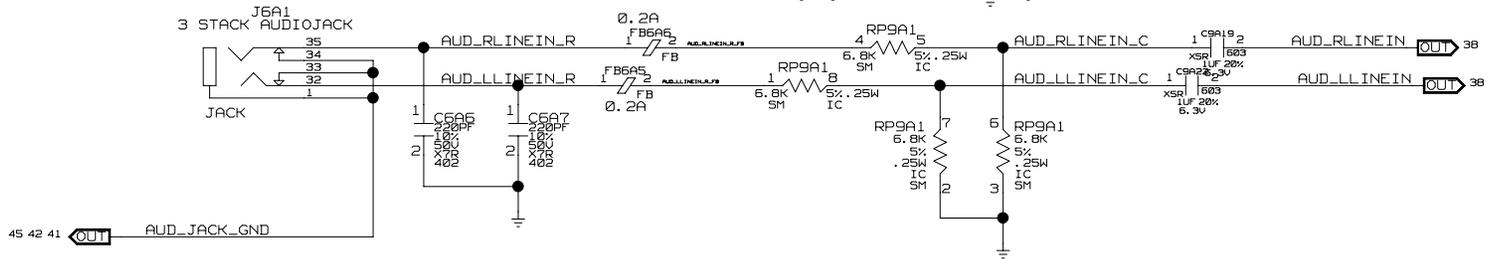
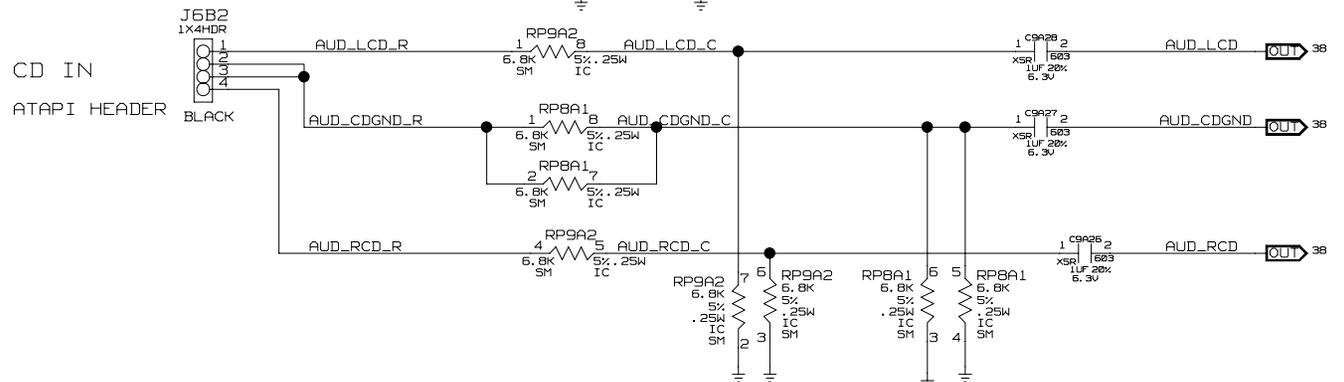
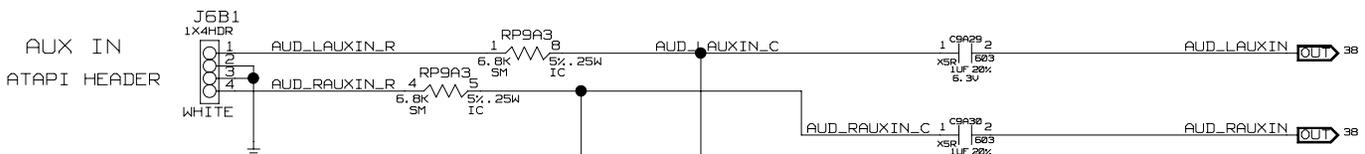


CODEC FILTER CAPS:
1981, 1885/86, 4205, 9766

DEFAULT
STUFFING
ADI 1981

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: AUDIO CODEC FILTERING CAPS		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 39

8 7 6 5 4 3 2 1



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: AUDIO ATAPI HEADERS

REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002 SHEET: 40

1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

D

C

B

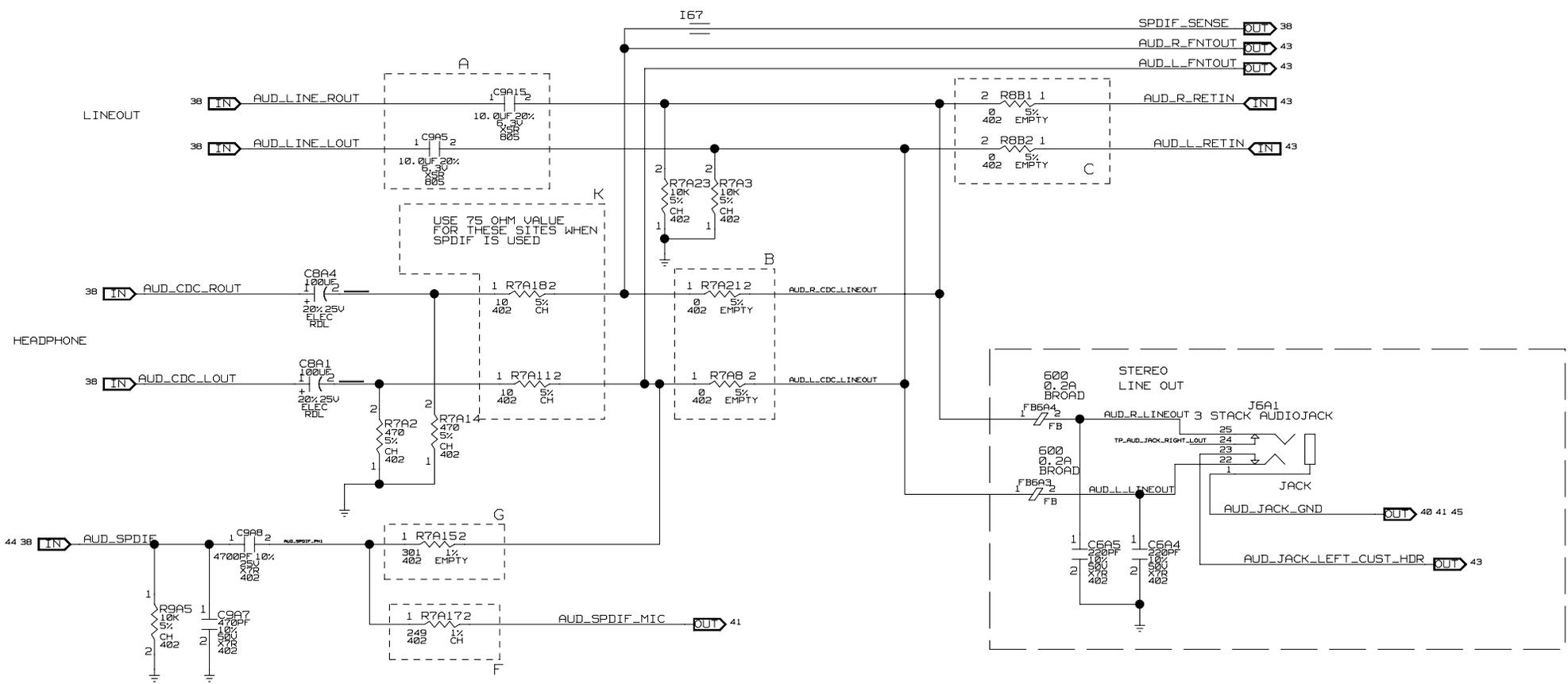
A

D

C

B

A



	BP ONLY	FP-->BP	SPDIF	BP LO	BP MIC
HEADPHONE	STUFF B	STUFF C	F	EMPTY	STUFF
	EMPTY A, C	EMPTY A, B	G	STUFF	EMPTY
LINEOUT	STUFF A	N/A	H	EMPTY	110 OHM
	EMPTY B, C		J	STUFF	EMPTY
			K	75 OHM	10 OHM

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: AUDIO: LINE-OUT

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002

1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630

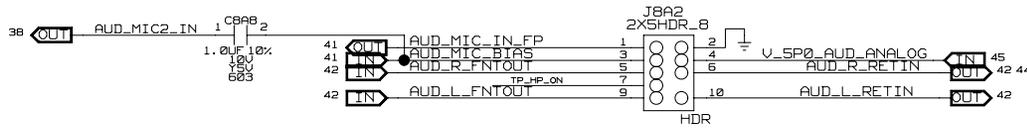
REV: 2.0

SHEET: 42

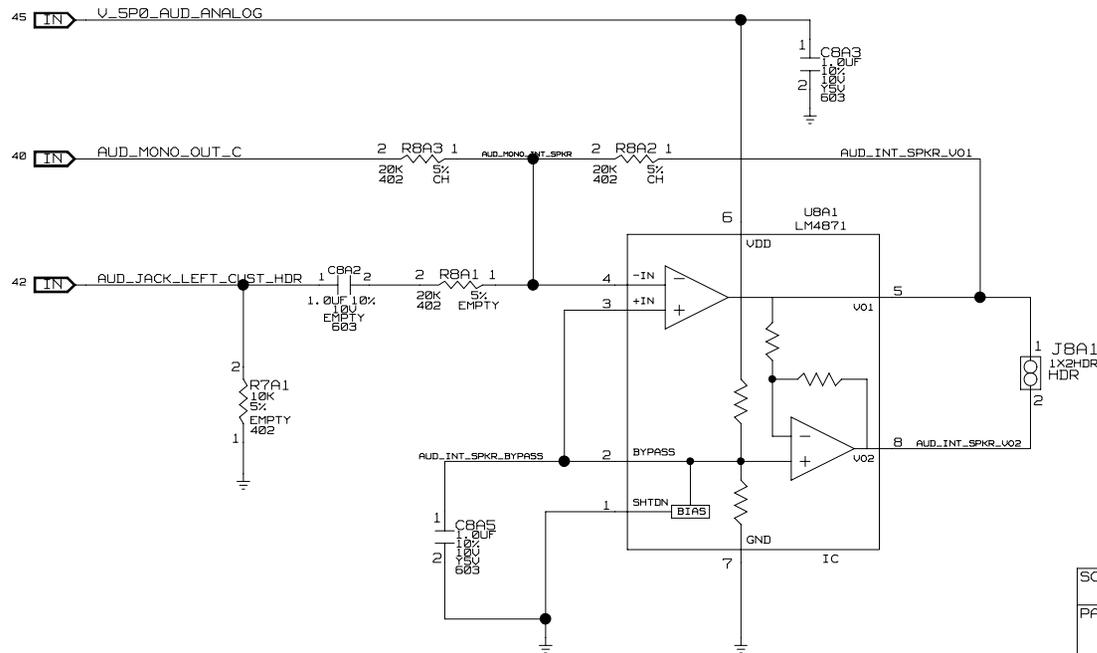
8 7 6 5 4 3 2 1

NOTE:
 FP DONGLE MUST HAVE
 MIC JACK RING SHUNT SPRING
 TERMINAL CONNECTED
 TO GND FOR PROPER
 MIC SENSING OPERATION

AUDIO FRONT PANEL
 PLACE NEAR AUDIO CIRCUIT



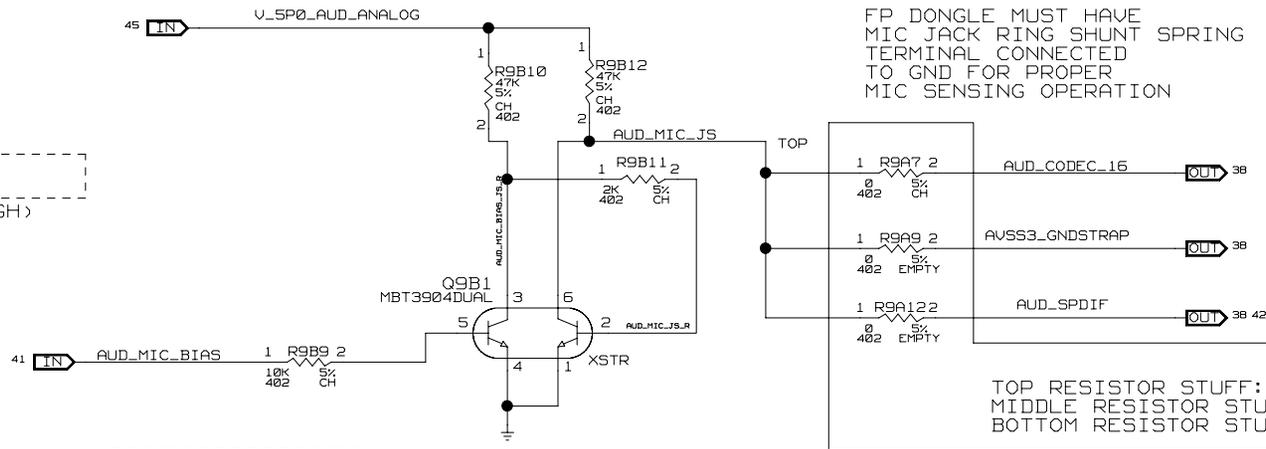
INTERNAL SPEAKER CIRCUIT



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: AUDIO_FRONT_PANEL		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 43

MIC JACK SENSE

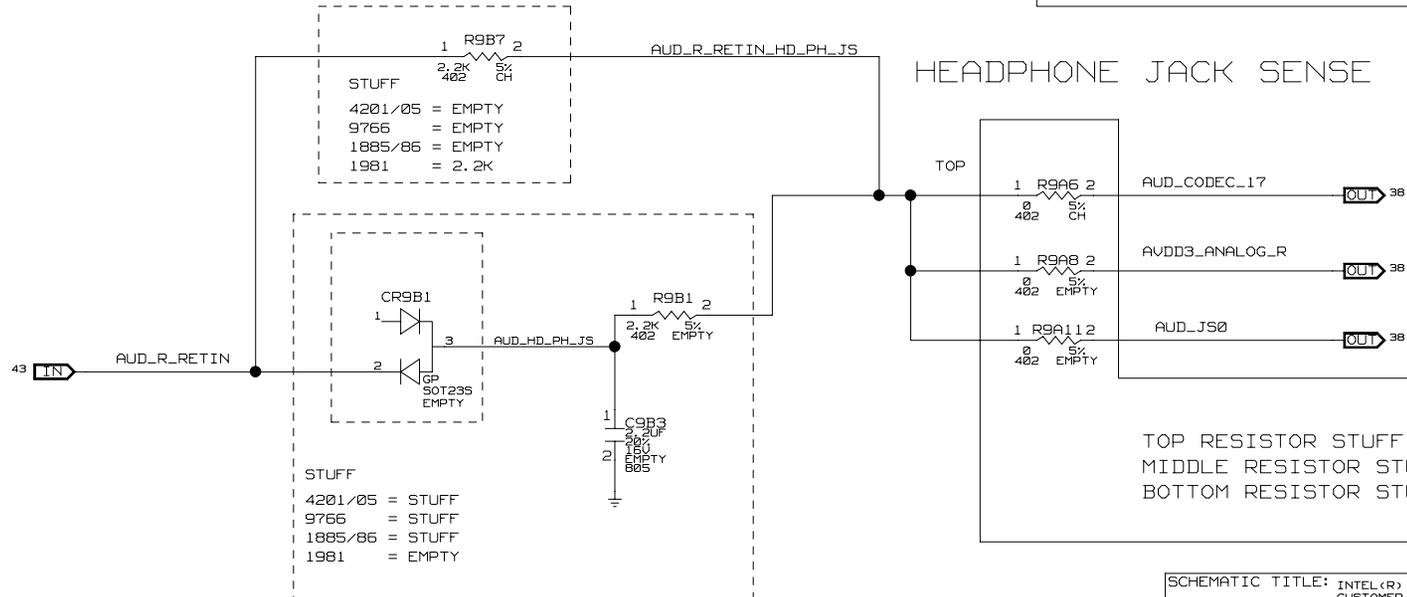
FP DONGLE MUST HAVE
MIC JACK RING SHUNT SPRING
TERMINAL CONNECTED
TO GND FOR PROPER
MIC SENSING OPERATION



NOT CONNECTED
4205: 43, 44, 41, 40, 39
1981: 16, 17 (ACTIVE HIGH)
9766: 43, 44
4291: NONE
1885/86: 47, 48

TOP RESISTOR STUFF: 1981
MIDDLE RESISTOR STUFF: 9766/4205
BOTTOM RESISTOR STUFF: 1885/86

HEADPHONE JACK SENSE



STUFF
4201/05 = EMPTY
9766 = EMPTY
1885/86 = EMPTY
1981 = 2.2K

STUFF
4201/05 = STUFF
9766 = STUFF
1885/86 = STUFF
1981 = EMPTY

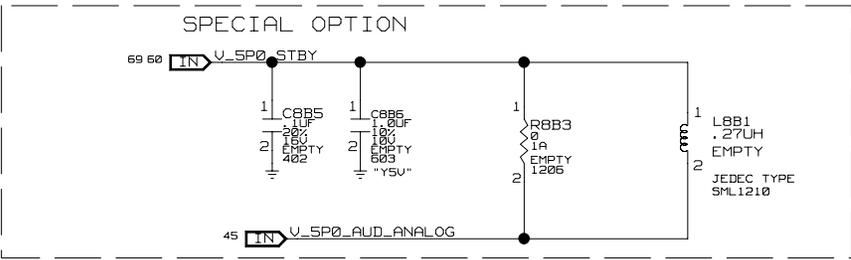
TOP RESISTOR STUFF: 1981
MIDDLE RESISTOR STUFF: 9766/4205
BOTTOM RESISTOR STUFF: 1885/86

DEFAULT
STUFFING
ADI 1981

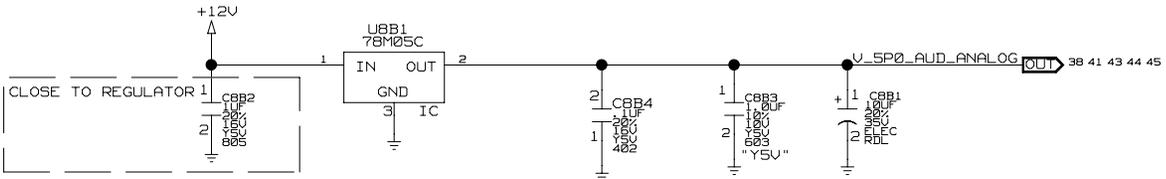
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: JACK SENSE REV: 2.0

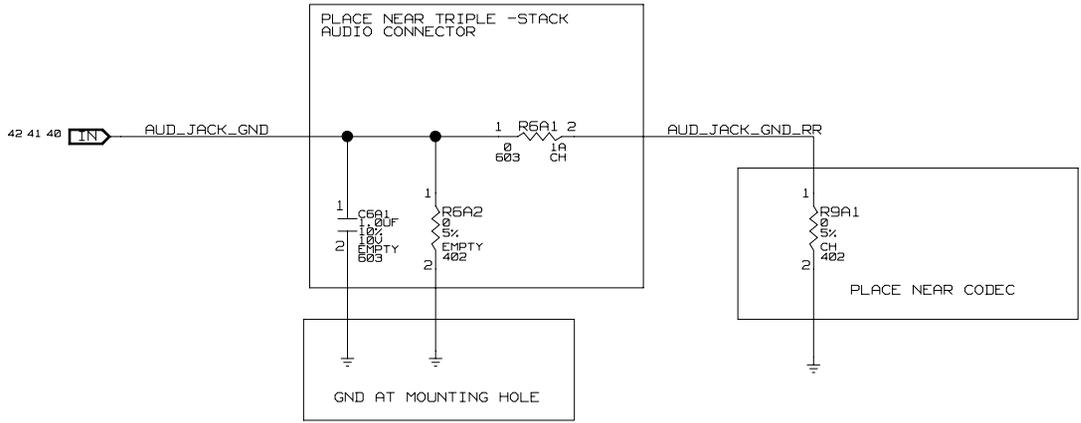
INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002 SHEET: 44
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630



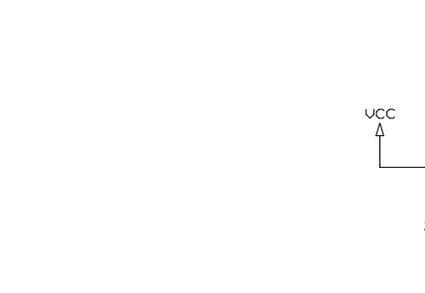
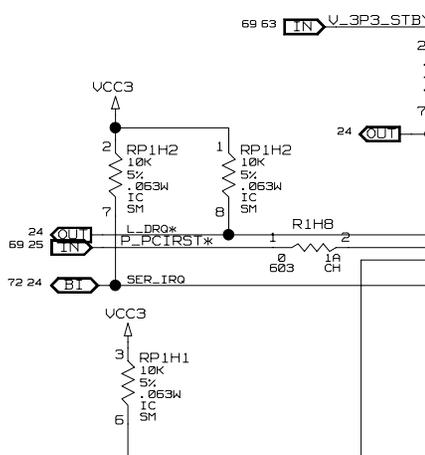
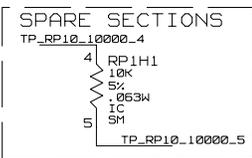
REGULATOR THERMAL TAB SHOULD BE SOLDERED TO A COPPER PAD THAT IS LARGE ENOUGH TO ALLOW 5 TO 10 GROUND VIAS AROUND THE COMPONENT FOR COOLING



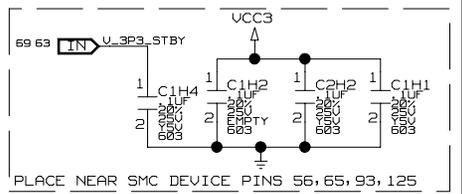
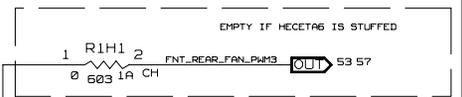
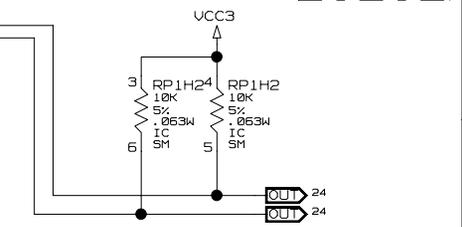
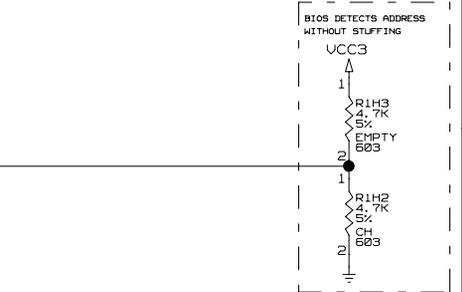
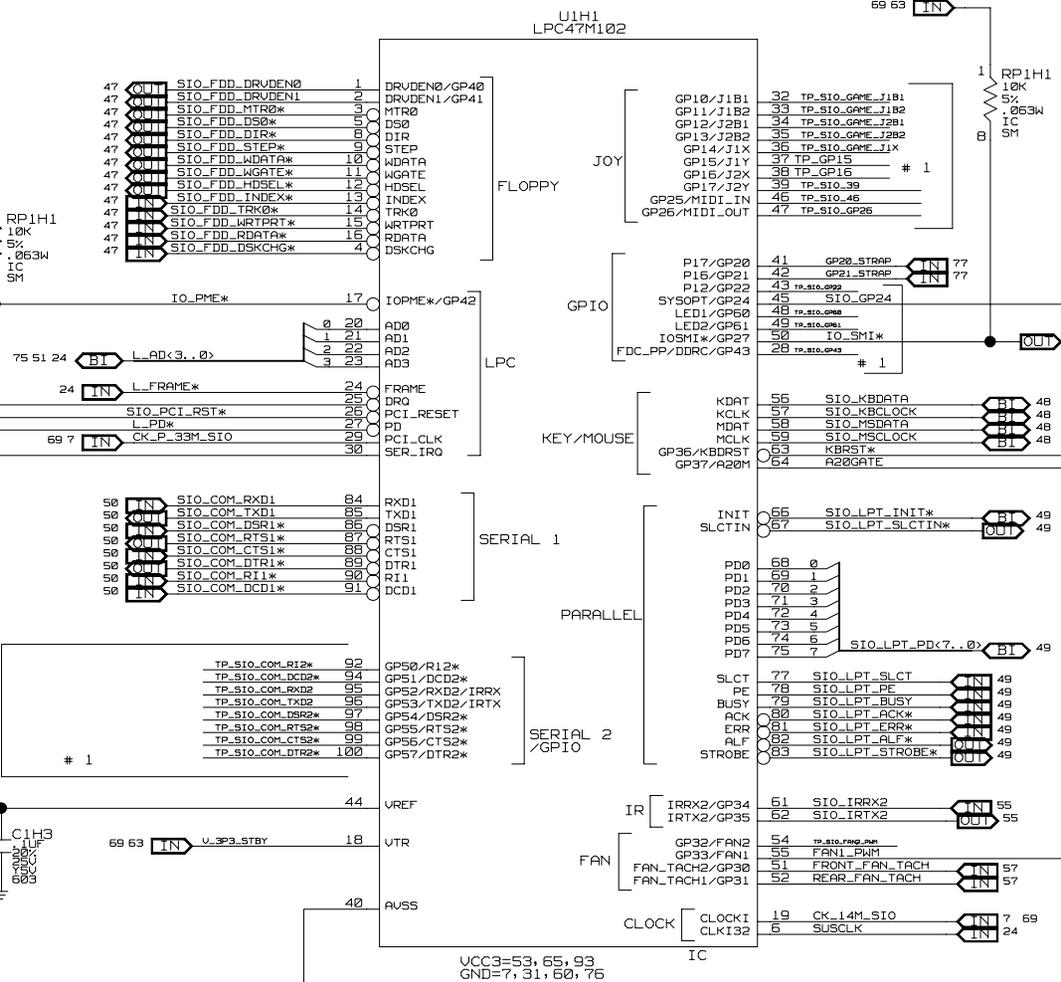
NOTE:
LAYOUT SHOULD GO FROM PIN 2 TO CAPS AND THEN THROUGH SEVERAL VIAS TO U_SP0_AUD_ANALOG



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	AUDIO VREG	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 45



NOTE: #1
BIOS TO PROGRAM THESE
GPIO'S AS OUTPUTS



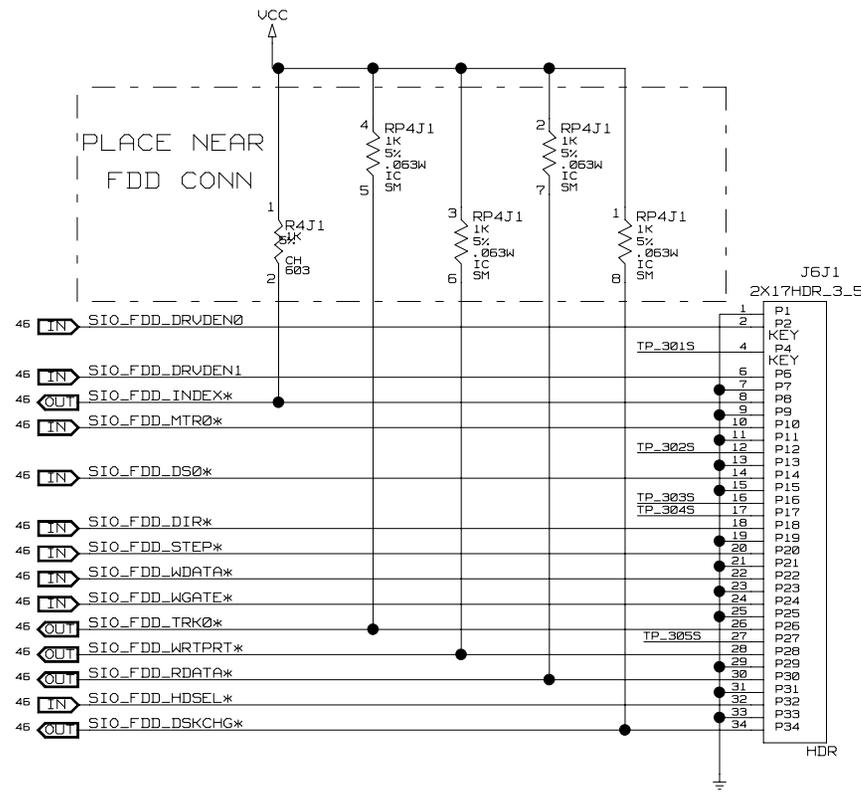
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

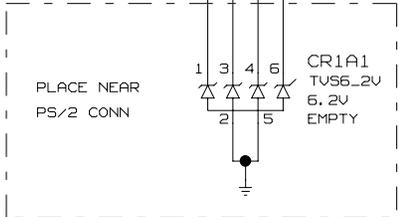
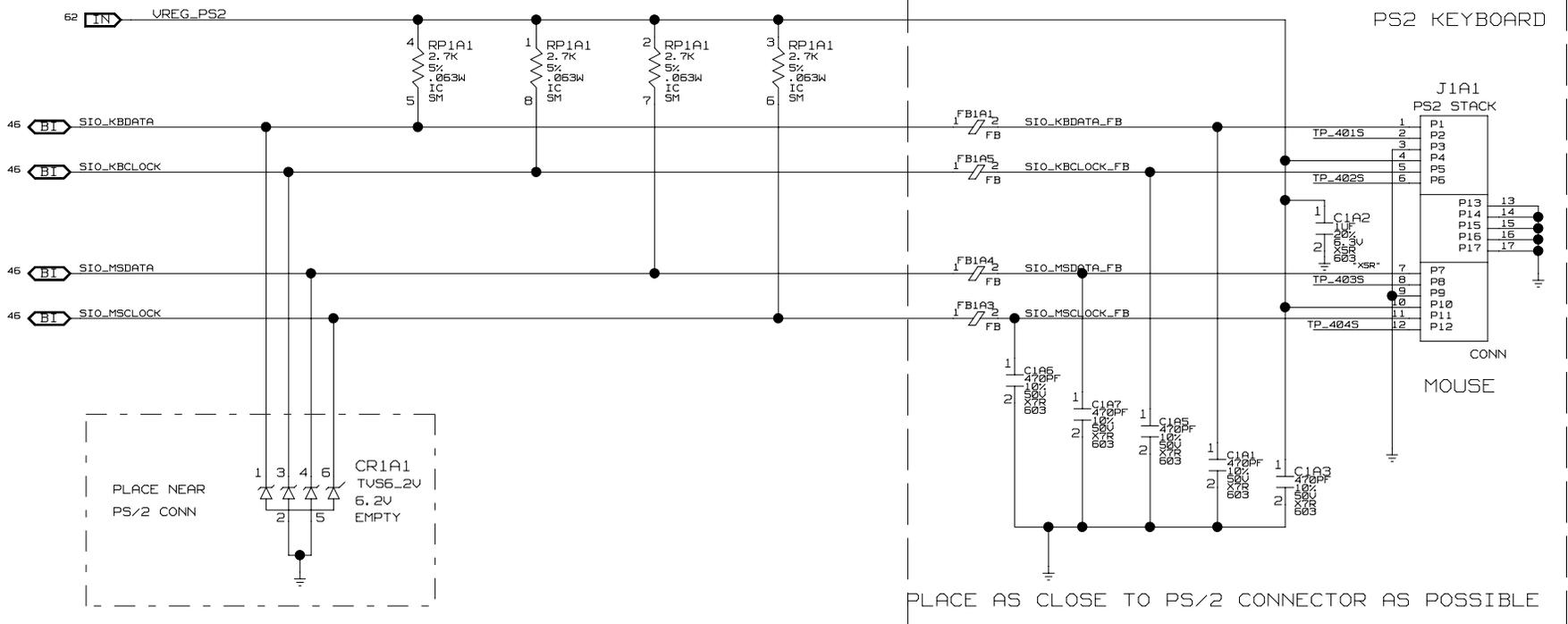
PAGE TITLE: SIO : LPC

REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002 **SHEET:** 46

1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

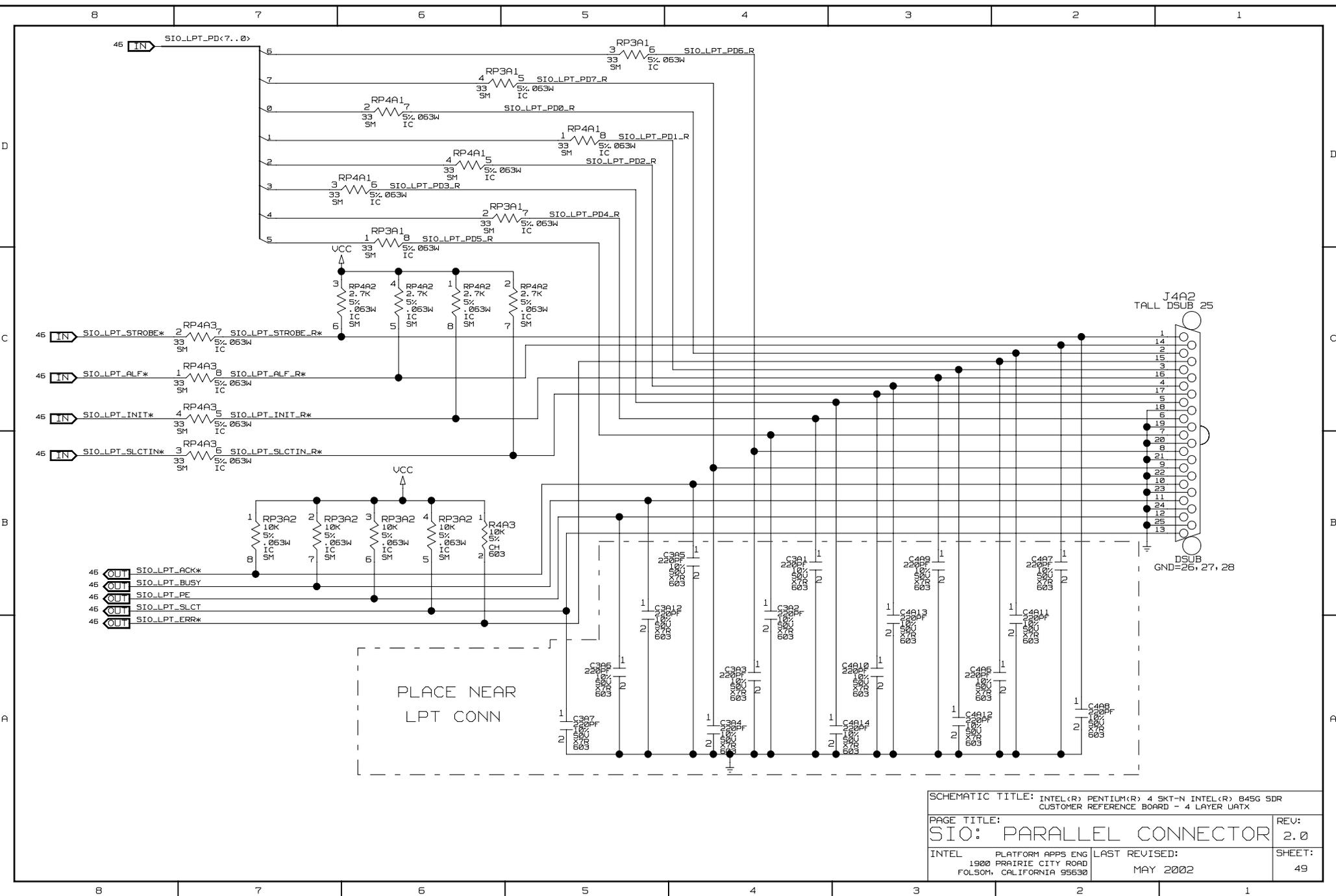




PLACE AS CLOSE TO PS/2 CONNECTOR AS POSSIBLE

ATX DOUBLE-STACKED

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: SIO: KEYBOARD/MOUSE		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 48

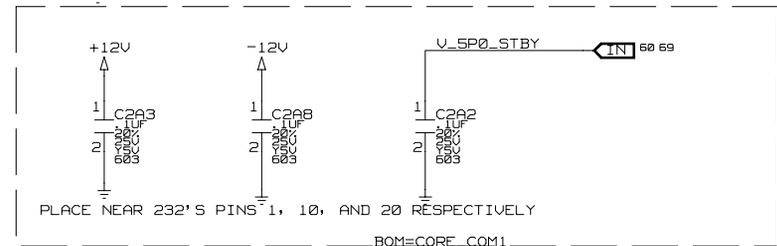
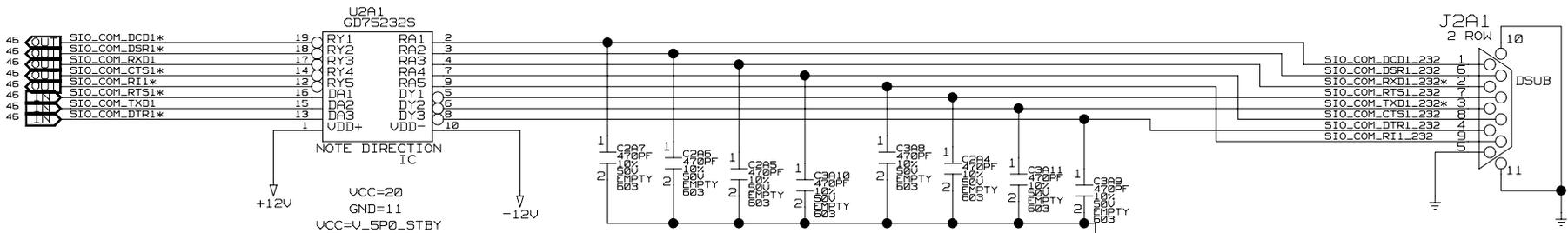


SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR
 CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE:
SIO: PARALLEL CONNECTOR

REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: MAY 2002 SHEET: 49
 1900 PRAIRIE CITY ROAD
 FOLSOM, CALIFORNIA 95630



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	SERIAL CONNECTOR	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 50

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

CONFIGURE= SAFE MODE

8 7 6 5 4 3 2 1

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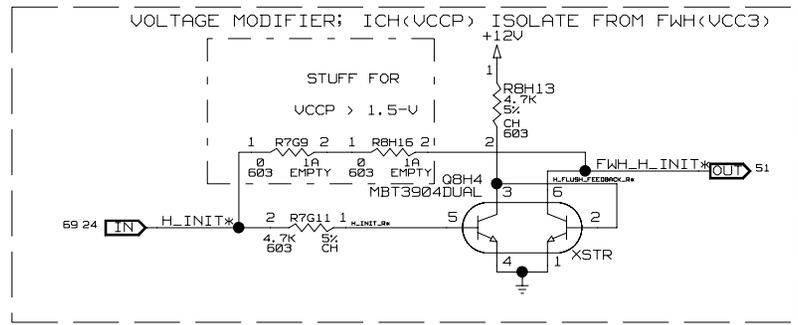
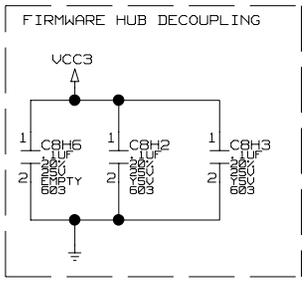
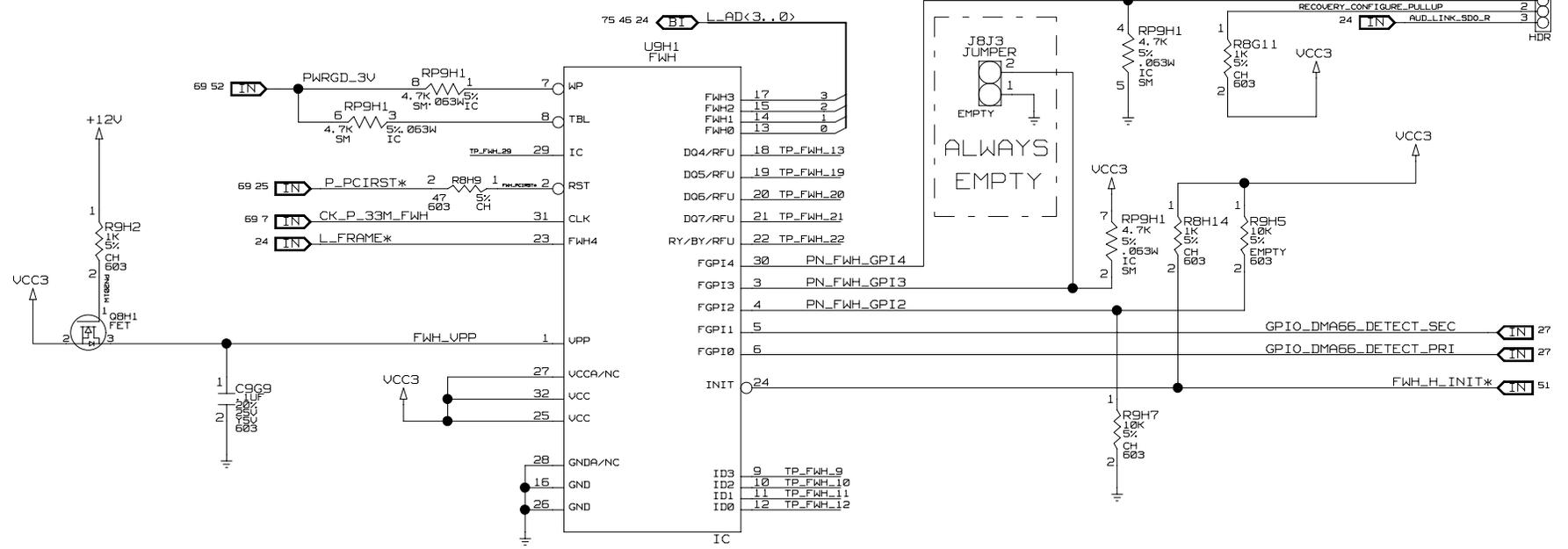
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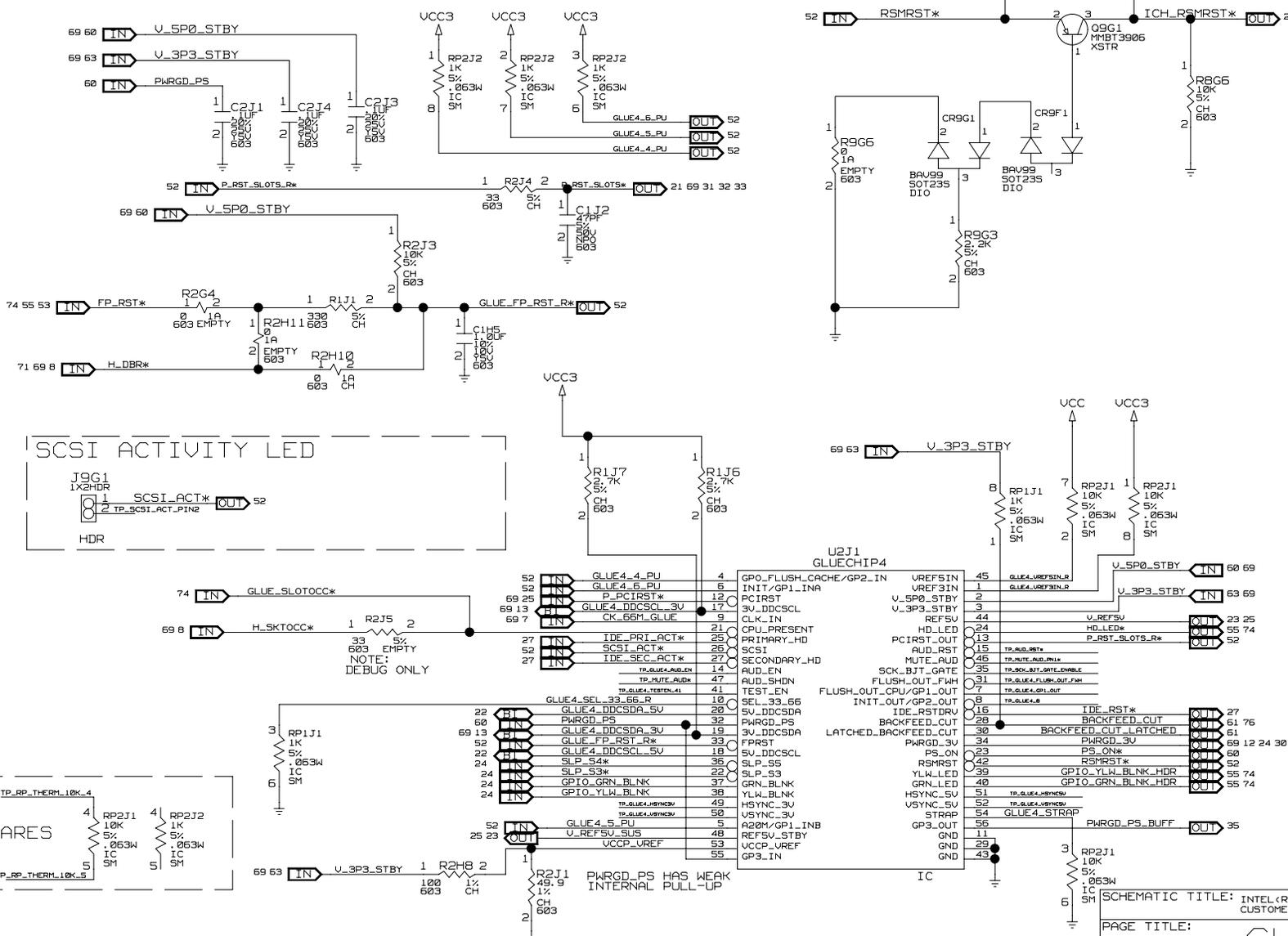
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PAGE TITLE:	FIRMWARE HUB	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		SHEET: 51
LAST REVISED: MAY 2002		

8 7 6 5 4 3 2 1

GLUECHIP4

GLUE4 INPUTS

PIN	FUNCTION	TYPE
1	VREF3IN	3I
2	5VSB	PI
3	3VSB	PI
4	GP2_IN	3IU
5	GP1_INB	UCCP REF
6	GP1_INA	UCCP REF
9	CLK_IN	3I
10	SEL_33_66	3IU
12	PCIRST*	3I
14	AUD_EN	3IU
17	3V_DDCSCL	3IOD
18	5V_DDCSCL	3IOD
19	3V_DDCSDA	3IOD
20	5V_DDCSDA	3IOD
21	CPU_PRESENT*	3IU
22	SLP_S3*	3I
25	PRIMARY_HDM*	5IU
26	SCSI*	5IU
27	SECONDARY_HDM*	5IU
32	PWRGD_PS	5IU
33	FPRST*	5IU
36	SLP_S5*	3I
37	GRN_BLNK	3IU
38	YLW_BLNK	3IU
41	TEST_EN	5ID
45	VREF5IN	5I
46	MUTE_AUD*	3IU
49	HSYNCH_3V	3I
50	VSYNCH_3V	3I
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54	STRAP	3IU
55	GP3_IN	5I

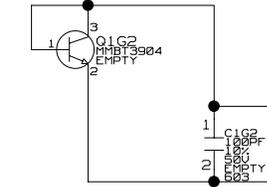


U2J1 GLUECHIP4

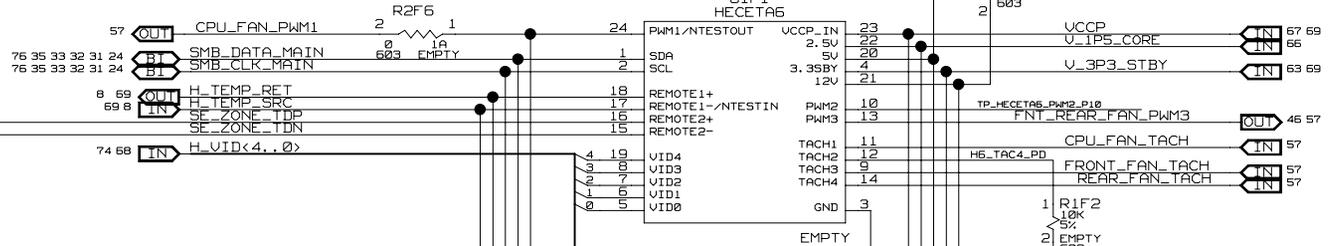
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CAD NOTE:
SOUTHEAST THERMAL ZONE SENSOR
PLACE BELOW DIMMS

CAD NOTE:
10MIL TRACE ON SE_ZONE_TDN AND _TDP



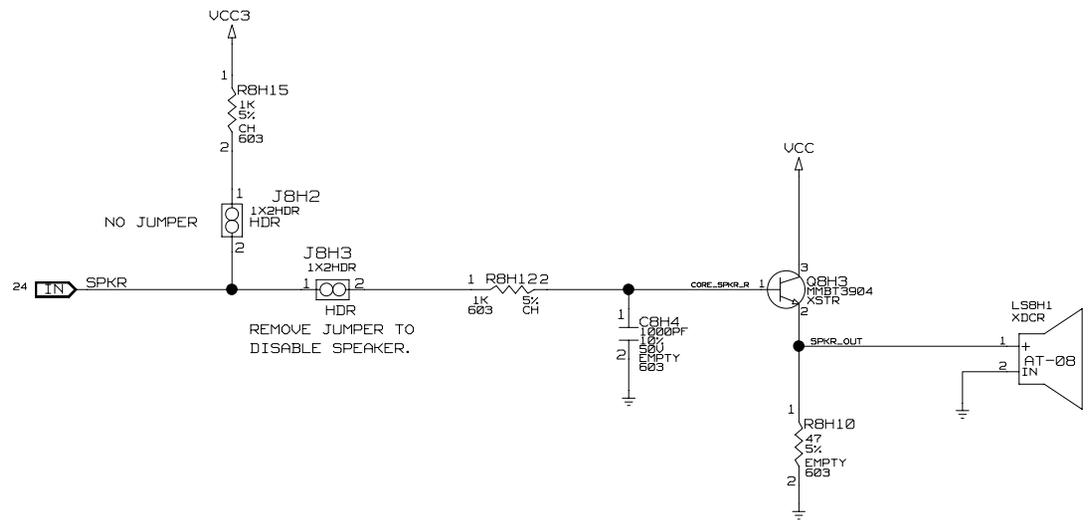
ALL STUFFED IF HECETA6
ALL EMPTY IF HECETA4



ALL STUFFED IF HECETA4
ALL EMPTY IF HECETA6

HARDWARE MANAGEMENT: HECETA

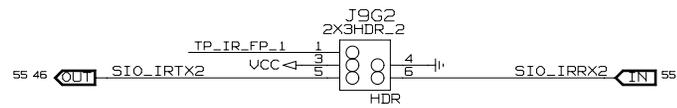
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PAGE TITLE: HW MANAGEMENT: HECETA	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 53



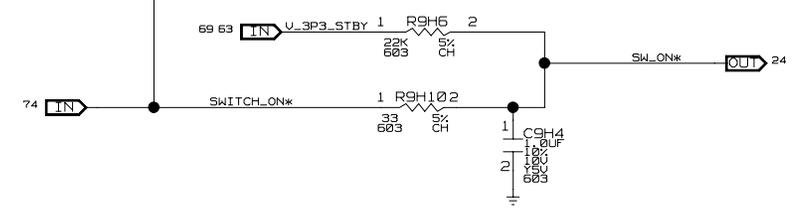
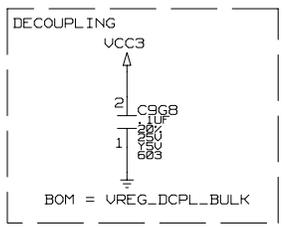
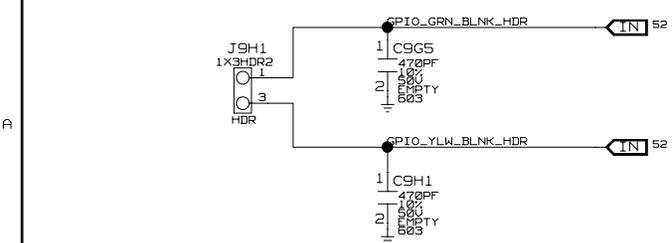
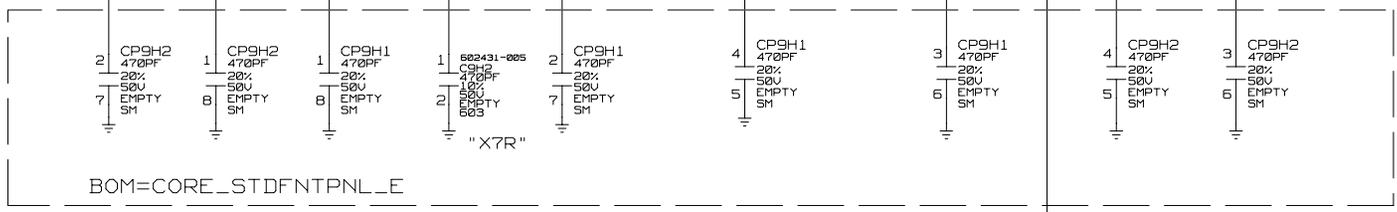
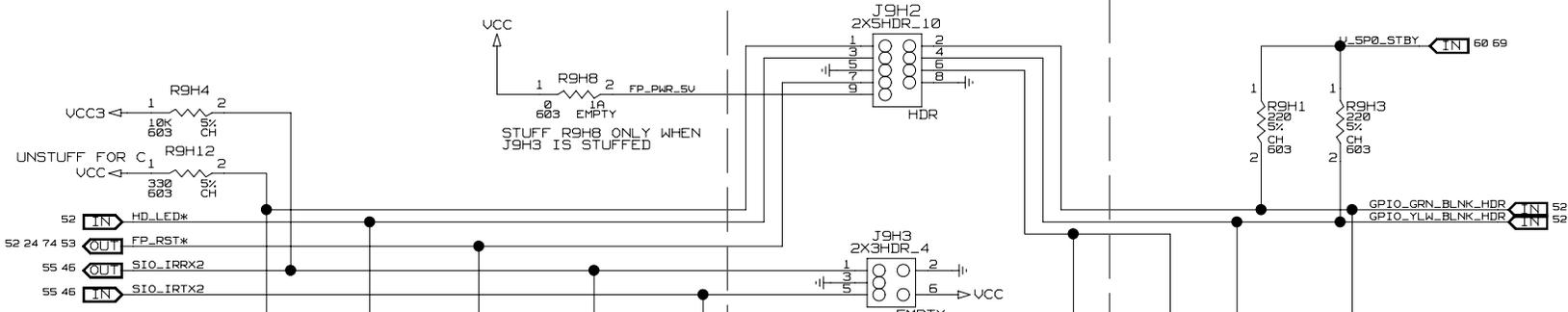
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CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: **SPEAKER** REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: SHEET: 54
1900 PRAIRIE CITY ROAD MAY 2002



CAD NOTE: OVERLAY SO PINS
 1-9 MATCH UP (DUAL FP).
 J9G2 DOES NOT NEED TO BE DUAL FP'D



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	STD FRONT PANEL HDR	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 55

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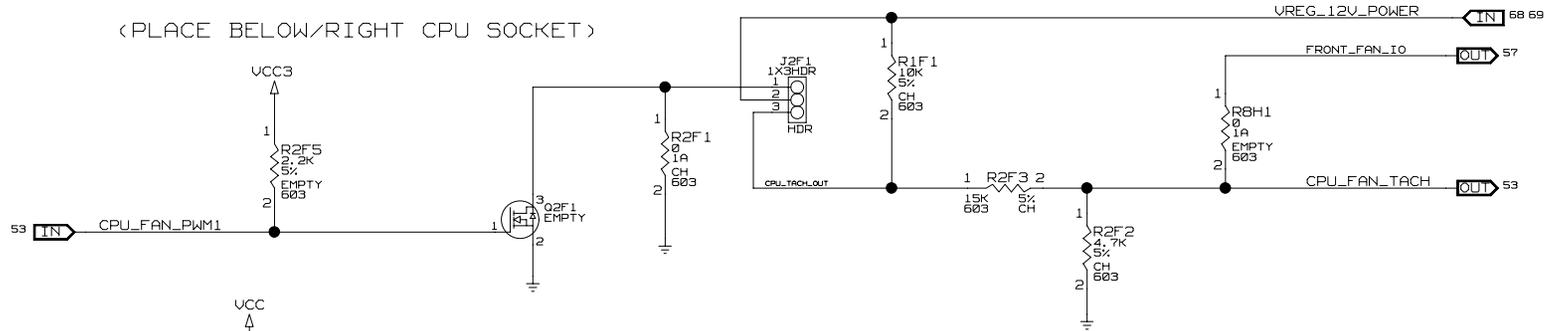
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INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG LAST REVISED: MAY 2002	SHEET: 56

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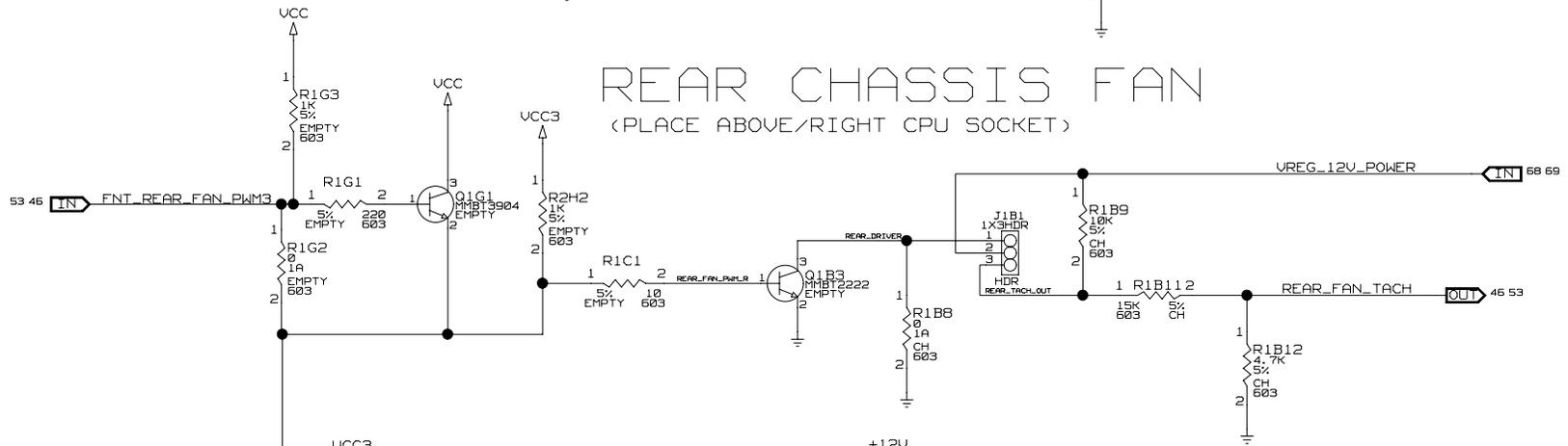
CPU ALWAYS-ON FAN

(PLACE BELOW/RIGHT CPU SOCKET)



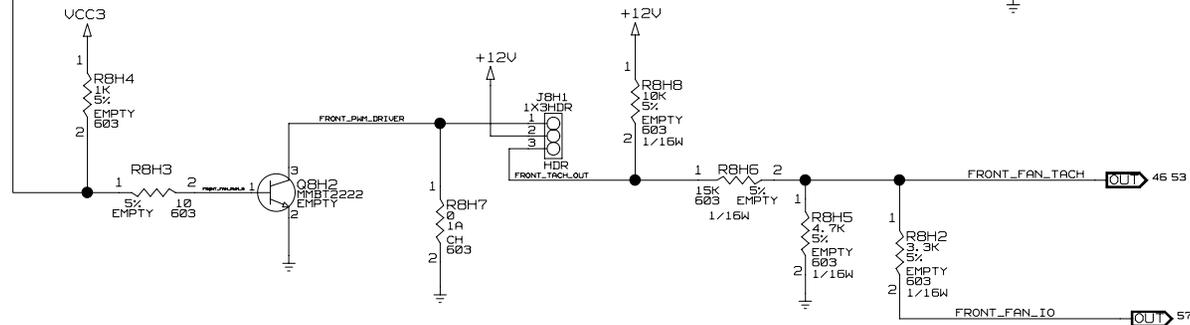
REAR CHASSIS FAN

(PLACE ABOVE/RIGHT CPU SOCKET)



FRONT CHASSIS FAN

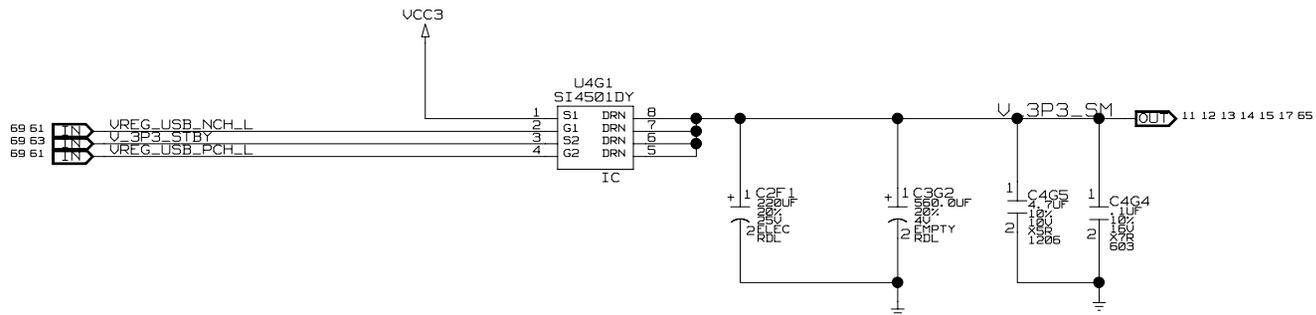
(PLACE LOWER LEFT CORNER OF PLATFORM)



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: FAN HEADERS	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 57

3P3 VREG

ROOM=DCL_DDR_VR



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: 3.3V SYSTEM MEMORY VREG		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 58

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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

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INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG LAST REVISED: MAY 2002	SHEET:	59
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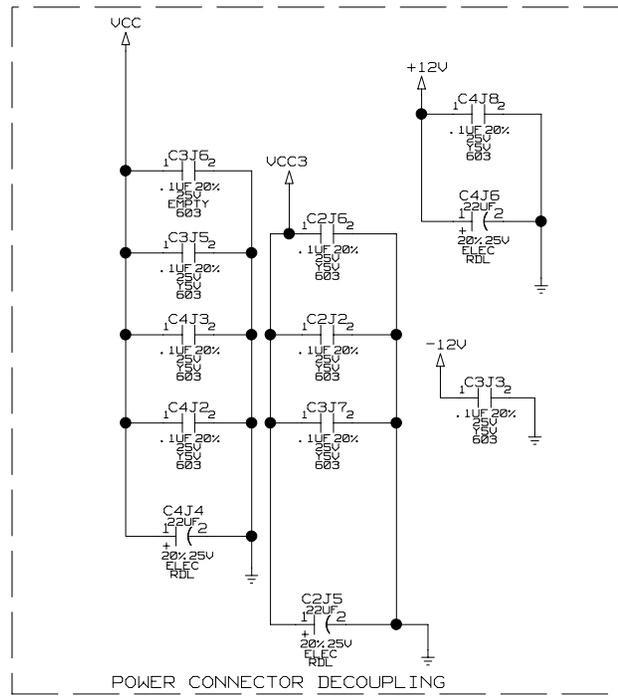
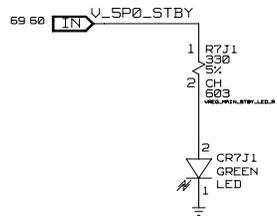
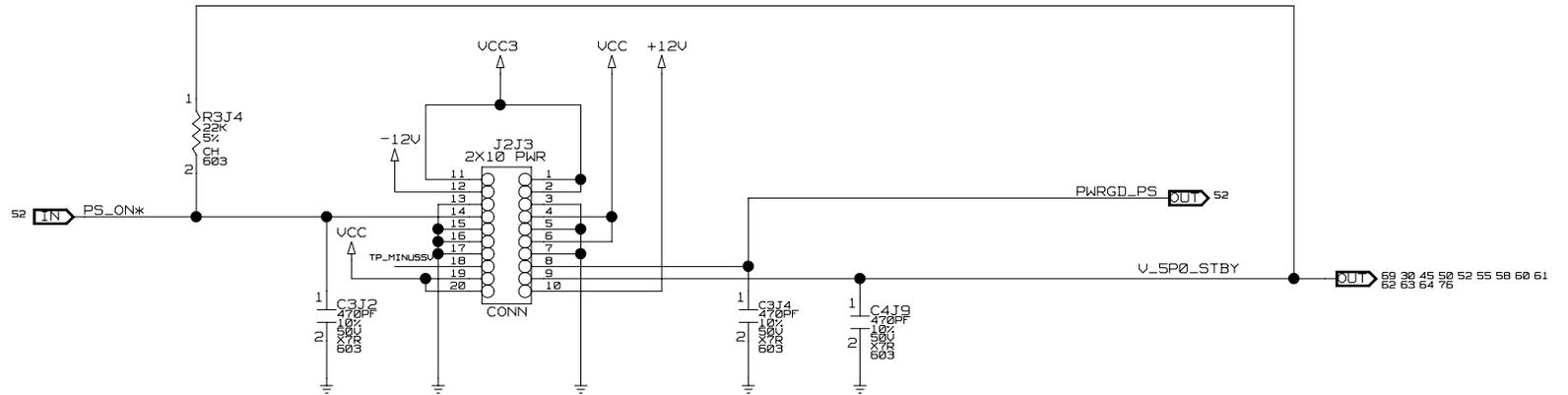
5

4

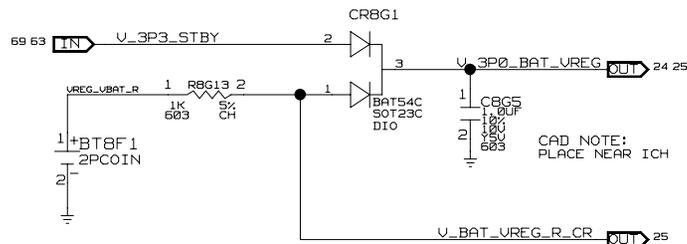
3

2

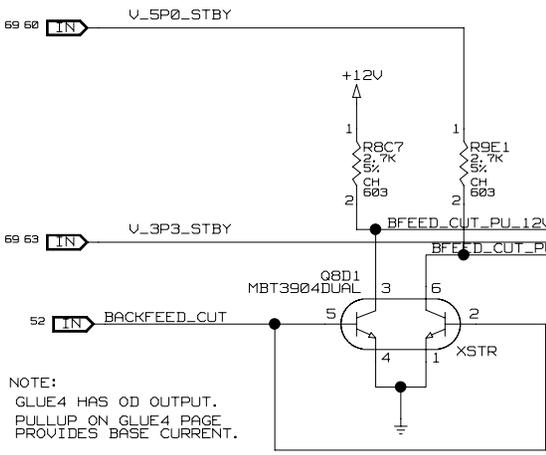
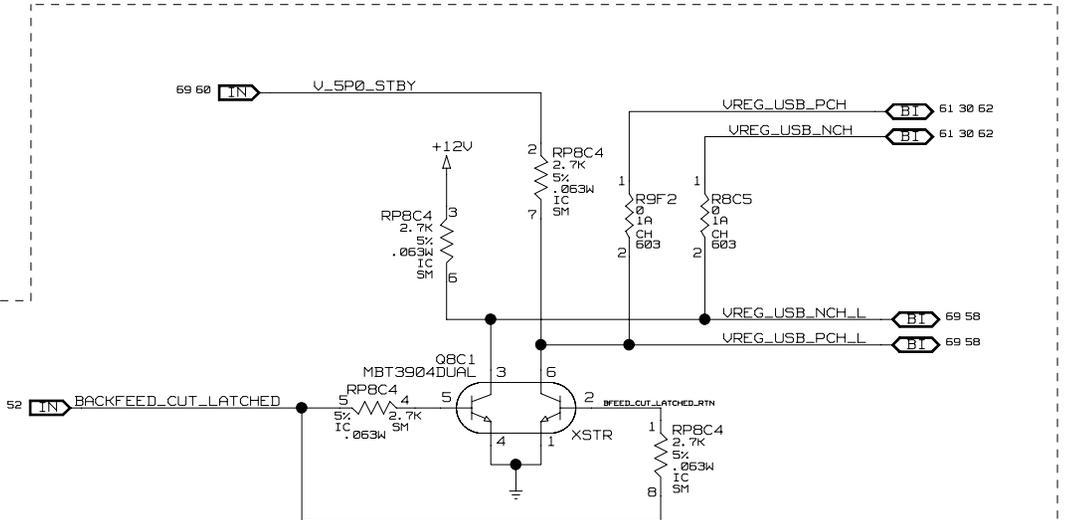
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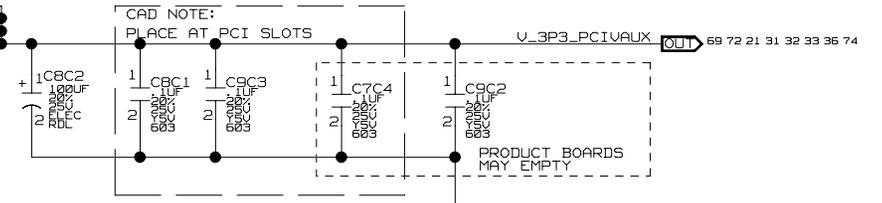
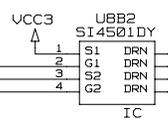
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		REV: 2.0
PAGE TITLE: STANDARD POWER CONNECTOR		SHEET: 60
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	



THROUGH-HOLE
 CAD NOTE: DO NOT PLACE BATTERY NEAR
 MOUNTING HOLES, GROUND OR VIAS

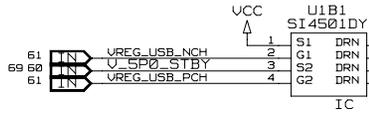
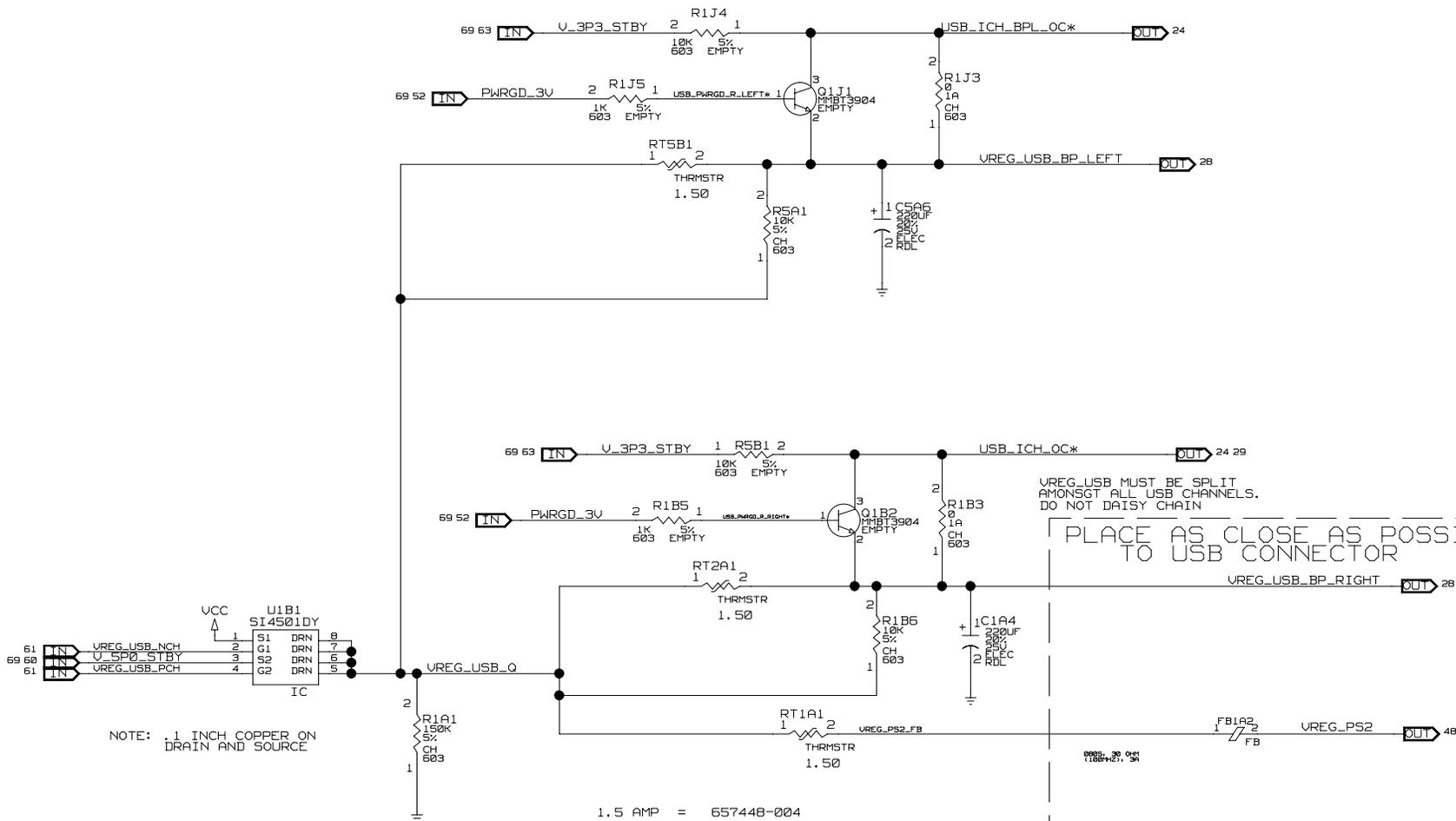


NOTE:
 GLUE4 HAS OD OUTPUT.
 PULLUP ON GLUE4 PAGE
 PROVIDES BASE CURRENT.



PCI VAUX

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: PCI VAUX		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 61



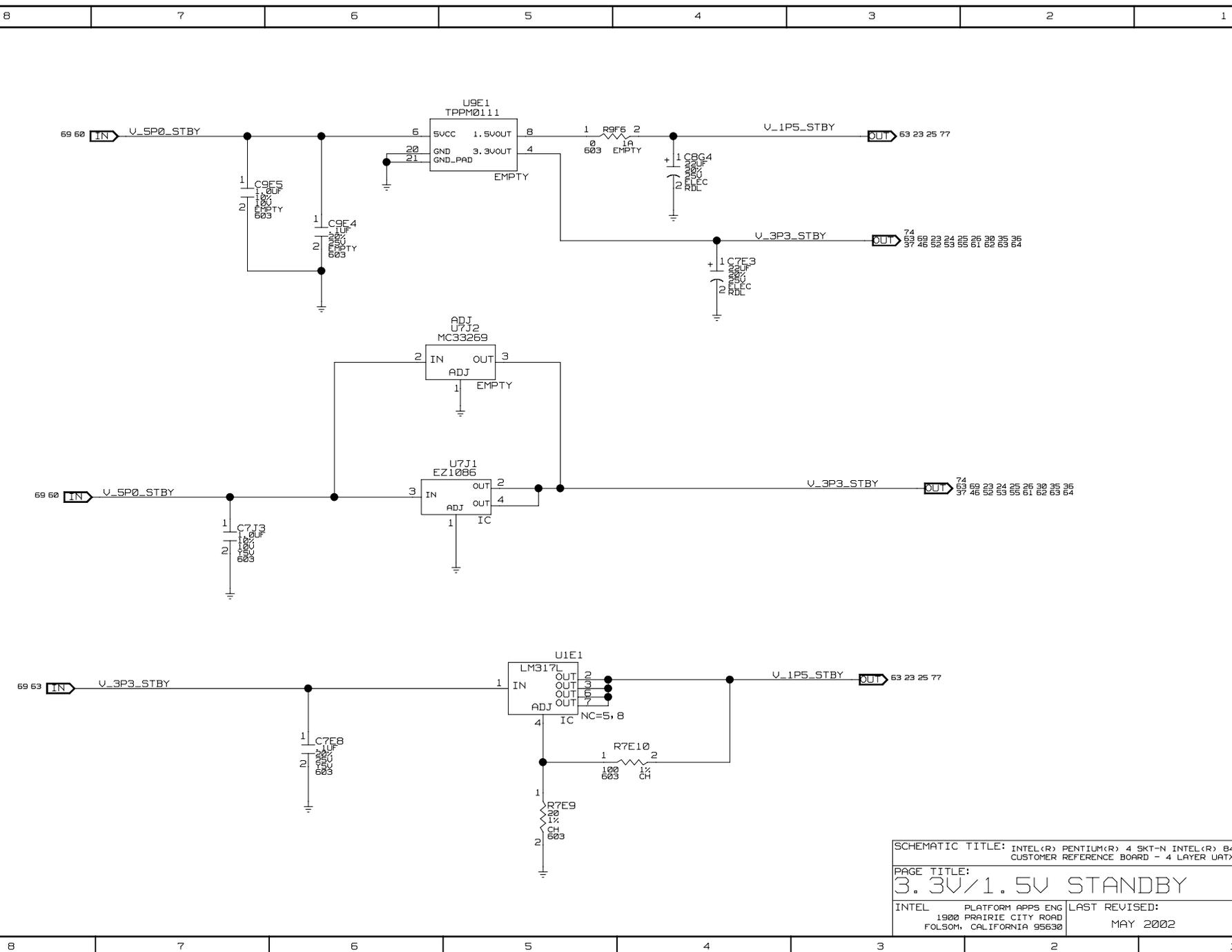
NOTE: .1 INCH COPPER ON DRAIN AND SOURCE

1.5 AMP = 65744B-004
 0.75 AMP = 65744B-001

VREG_USB MUST BE SPLIT AMONGST ALL USB CHANNELS. DO NOT DAISY CHAIN

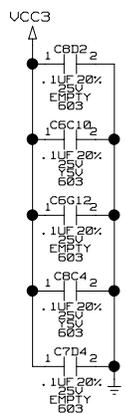
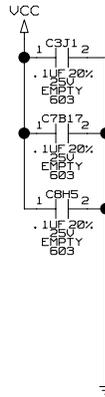
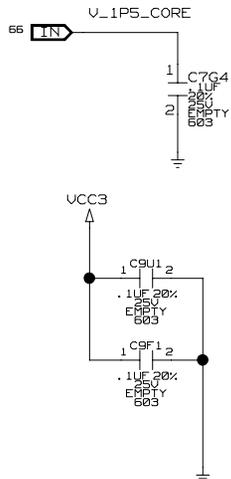
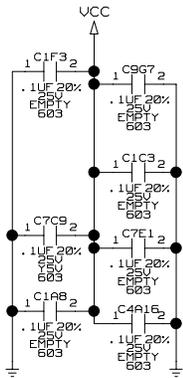
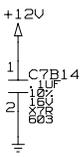
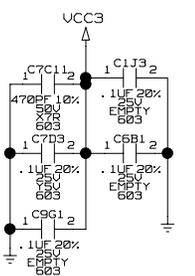
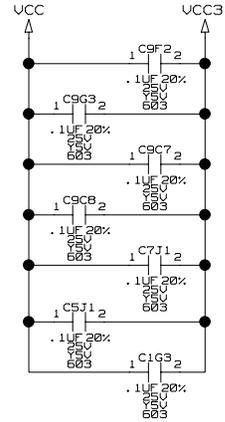
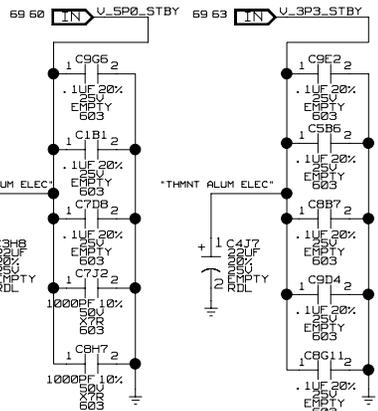
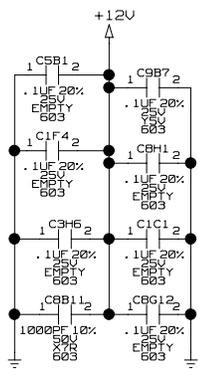
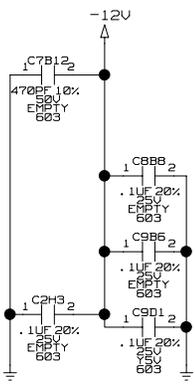
PLACE AS CLOSE AS POSSIBLE TO USB CONNECTOR

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: WAKE ON USB & PS2	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002 SHEET: 62



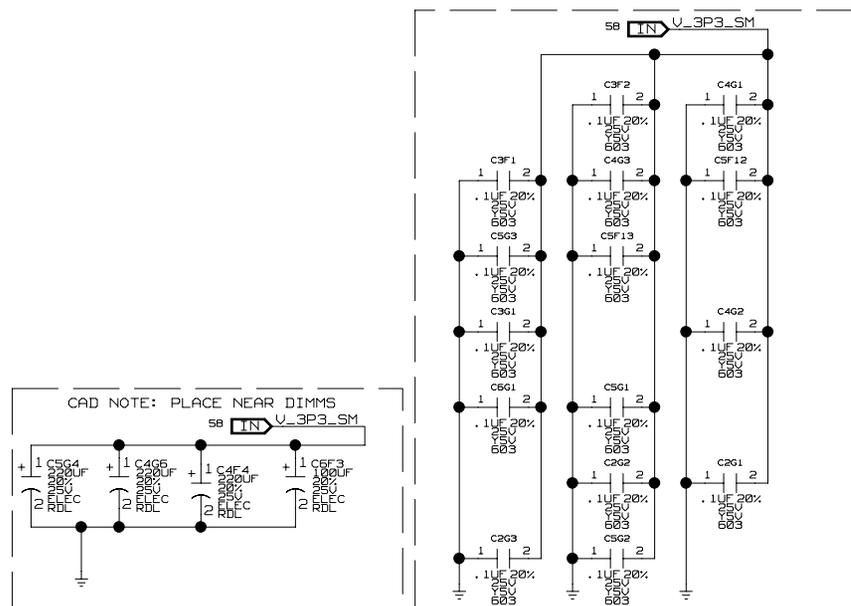
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: 3.3V/1.5V STANDBY	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002 SHEET: 63

VREG_DCPL_BULK



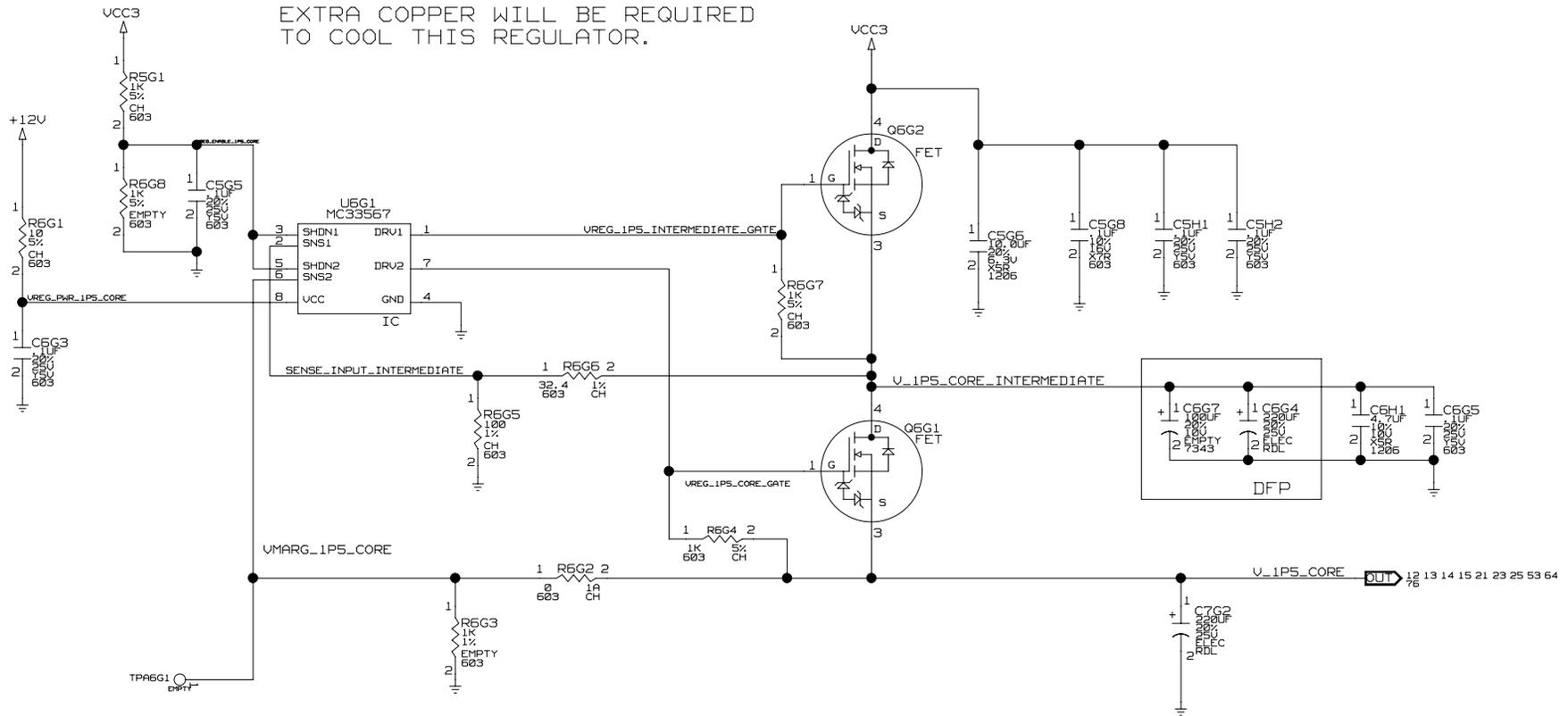
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: VREG BULK DECOUPLING		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 64

SDR 3P3_SM DECOUPLING

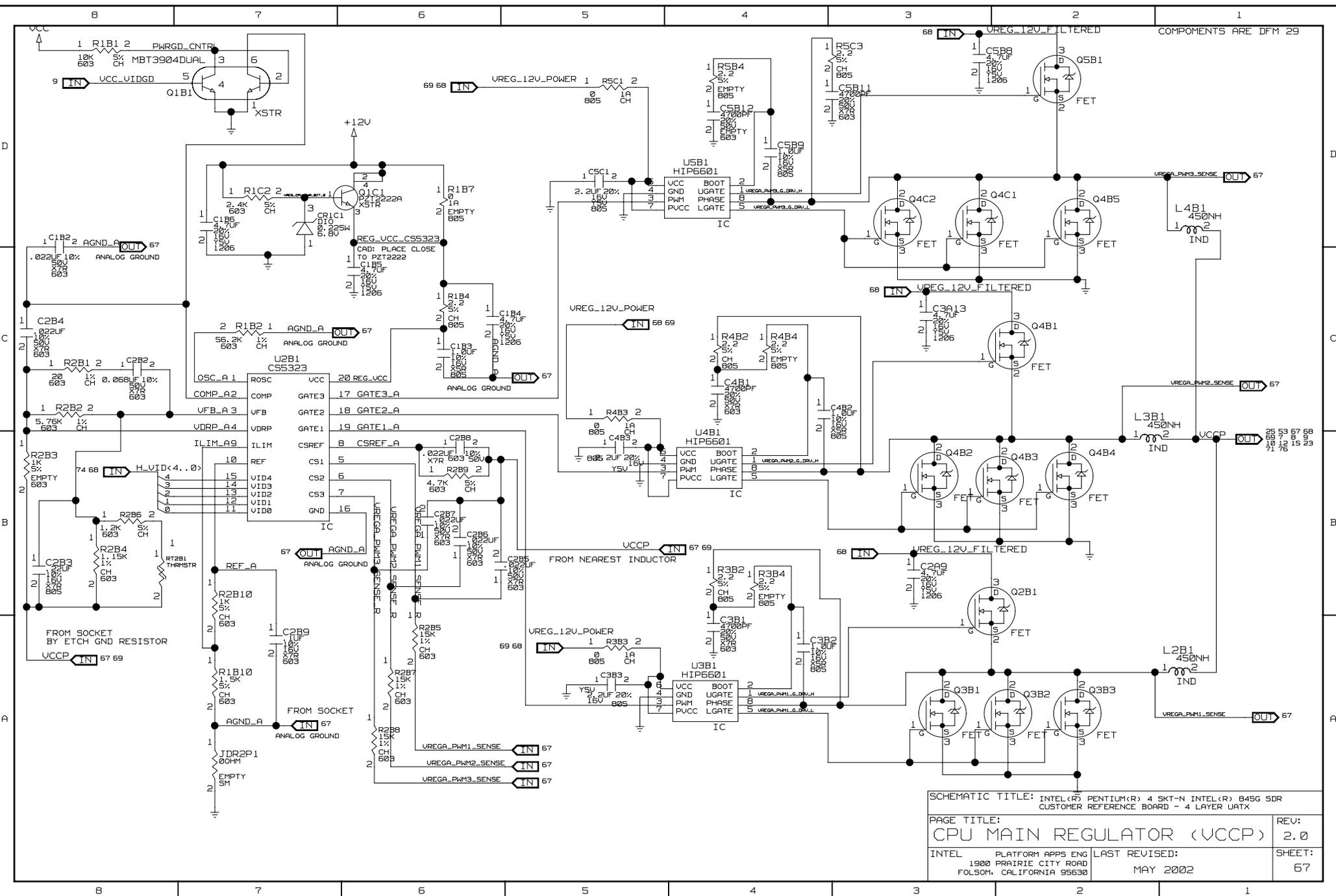


SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: VREG: 3.3V SM DECOUPLING		REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 65

CAD NOTE:
EXTRA COPPER WILL BE REQUIRED
TO COOL THIS REGULATOR.



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	VREG: CORE 1.5V	REV: 2.0
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 66



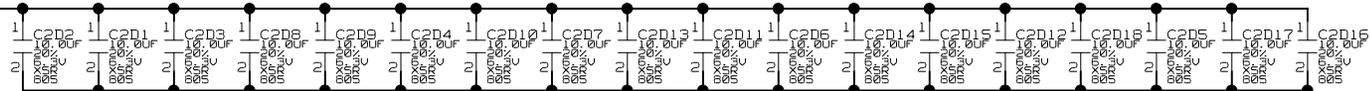
COMPONENTS ARE DFM 29

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		REV: 2.0
PAGE TITLE: CPU MAIN REGULATOR (VCCP)		SHEET: 67
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	

69 57 IN UCCP



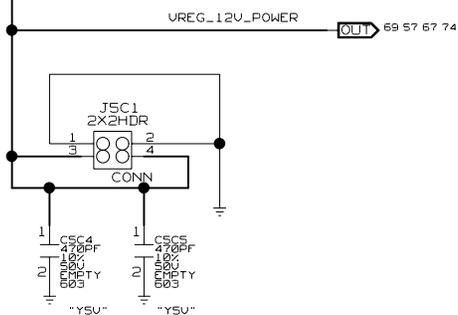
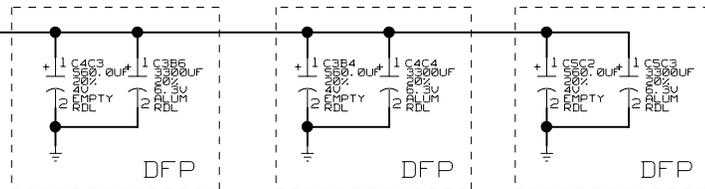
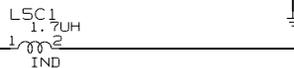
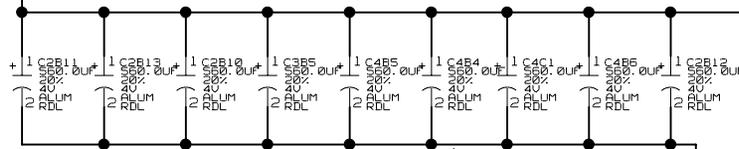
NOTE: PLACE THESE NORTH OF THE CPU SOCKET



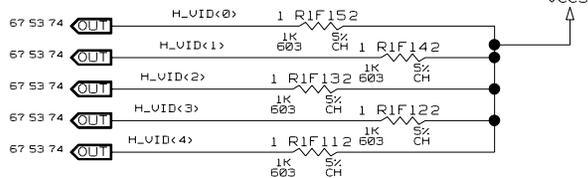
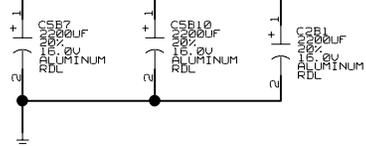
NOTE: PLACE THESE IN THE CAVITY OF THE CPU SOCKET



NOTE: PLACE THESE SOUTH OF THE CPU SOCKET

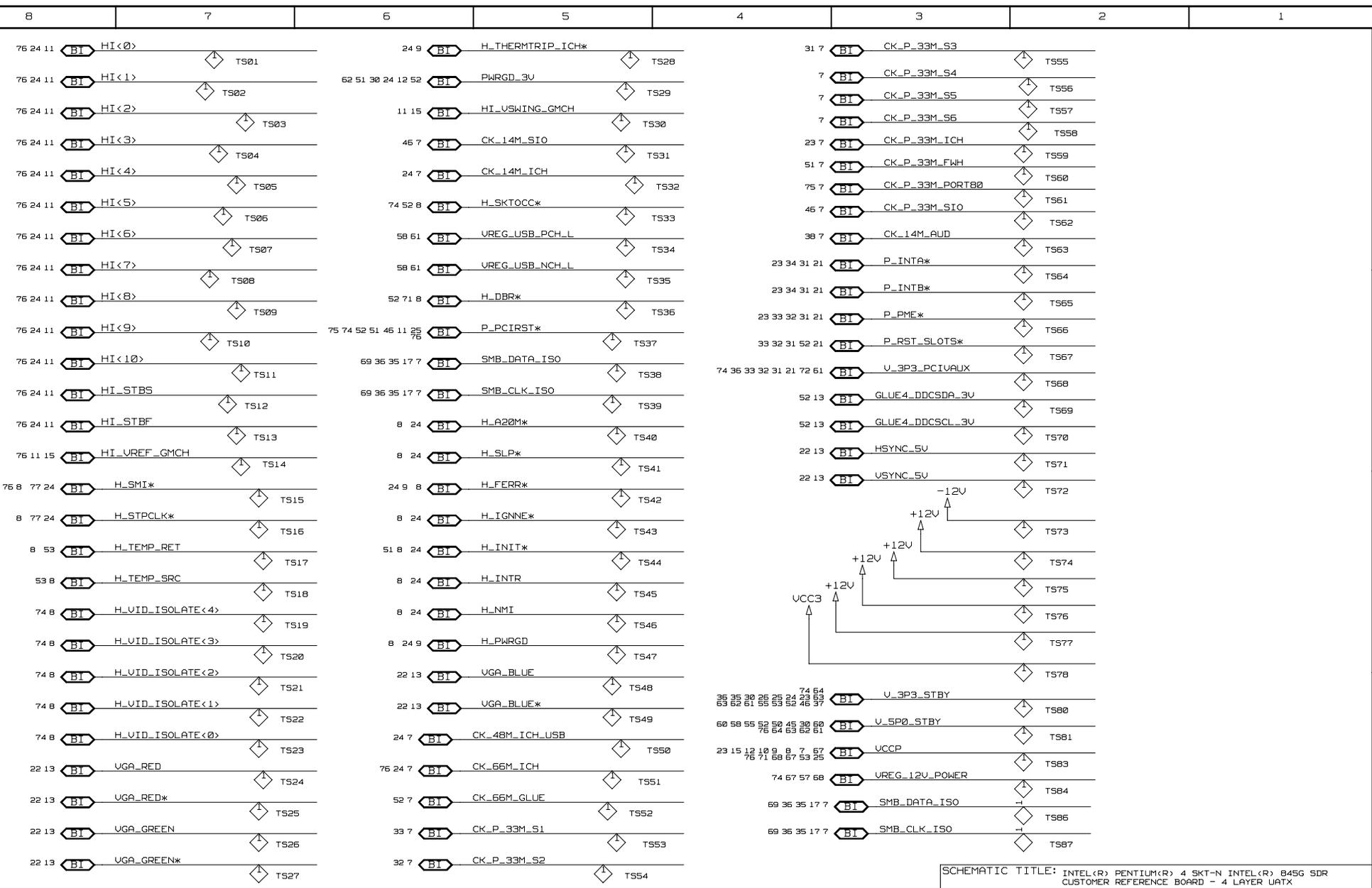


VREG_12V_FILTERED



CAPACITORS

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 645G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX	
PAGE TITLE: CPU DECOUPLING	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002 SHEET: 68



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE: DCL TRACK SPLITTERS	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002
	SHEET: 69

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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) 845G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE:	BLANK	REV:	2.0
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INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG	LAST REVISED:	MAY 2002	SHEET:	70
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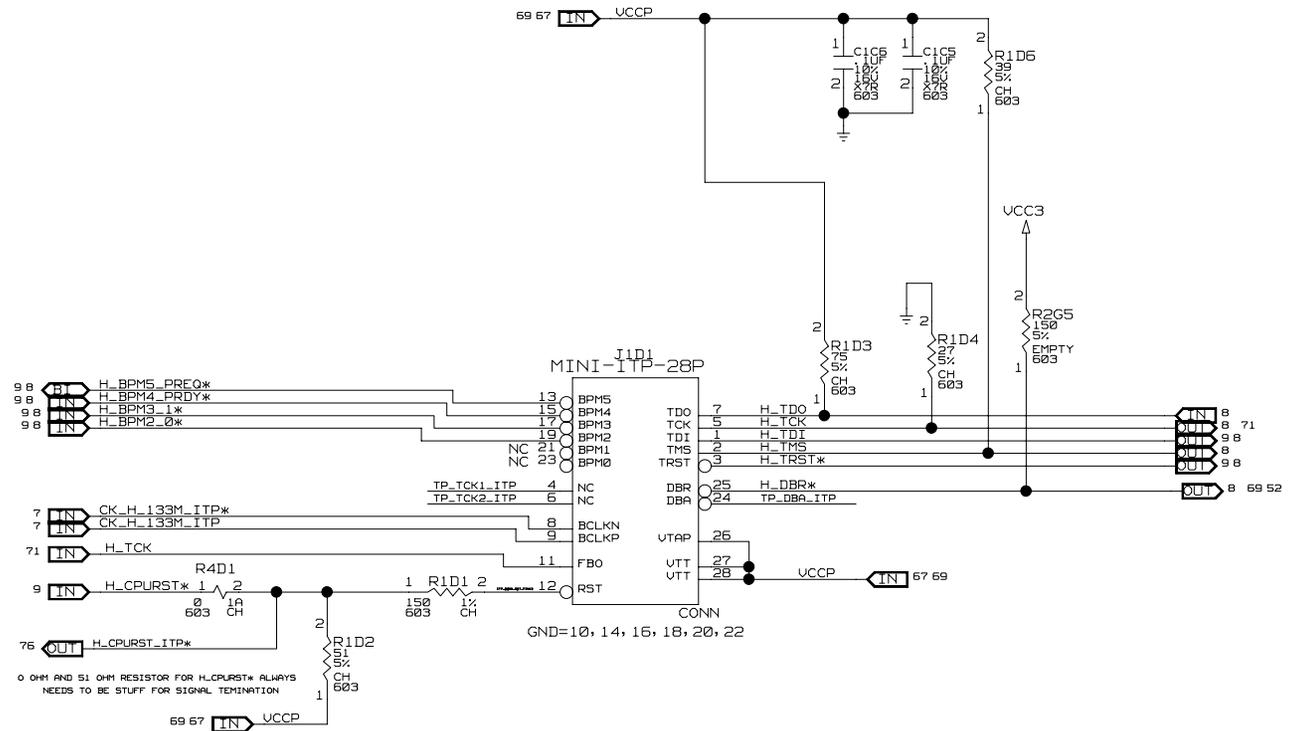
4

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1

ITP 700FLEX CONNECTOR



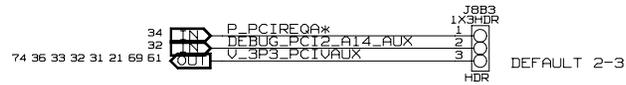
CAD NOTE: ROUTE H_TCK FROM THE TCK PIN OF THE CONNECTOR
TO THE PROCESSOR PIN. FBO LENGTH = TCK + BPM LENGTHS TO CPU.
SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

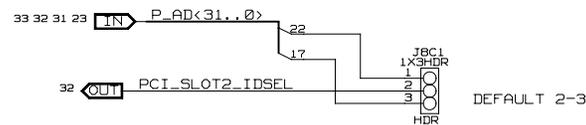
PAGE TITLE:
ITP 700FLEX CONNECTOR REV: 2.0

INTEL PLATFORM APPS ENG LAST REVISED: SHEET: 71
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630 MAY 2002

DEBUG HOOKS MOON ISA



J8B3/J8C1	PCI SLOT 2 MODE
1-2	MOON ISA
2-3	PCI <DEFAULT>



SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	MOON ISA	REV: 2.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 72

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SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR
CUSTOMER REFERENCE BOARD - 4 LAYER UATX

PAGE TITLE:	BLANK	REV:	2.0
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INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG	LAST REVISED: MAY 2002	SHEET: 73
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8 7 6 5 4 3 2 1

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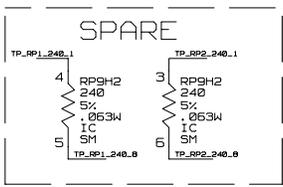
A

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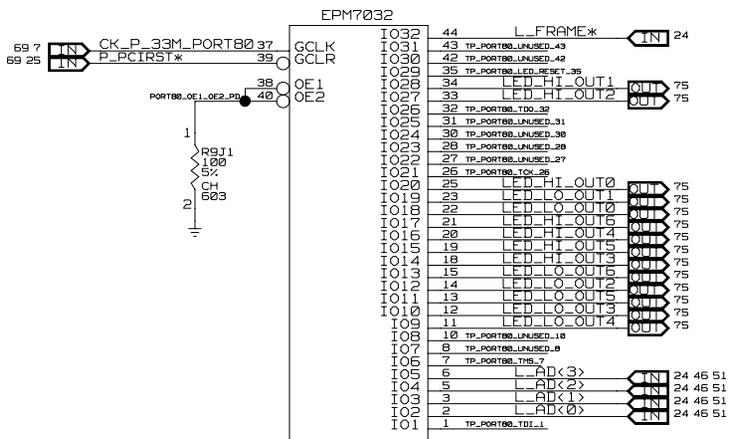
SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE:	BLANK	REV: 2.0
INTEL 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	PLATFORM APPS ENG LAST REVISED: MAY 2002	SHEET: 74

8 7 6 5 4 3 2 1



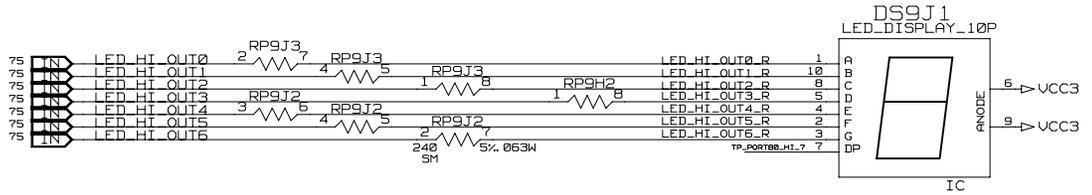
EPM7032AETC44-10
44 PIN TQFP

U9J1



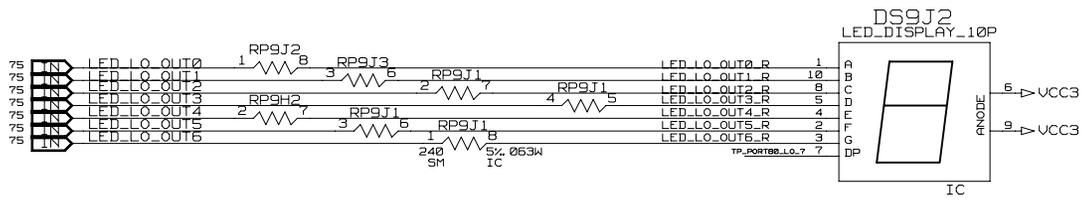
IC
UCC(PQFP)=9, 17, 29, 41
GND(PQFP)=4, 16, 24, 36
NC(PQFP)=45
UCC=UCC3(~PORTB0DEC)

CAD NOTE: ORIENT TO LEFT

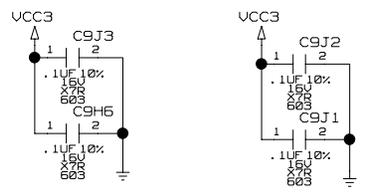


ALL RPACKS 240 OHMS

CAD NOTE: ORIENT TO RIGHT



CAD NOTE: PLACE 1 EACH ON PINS 6 & 9 OF EACH DISPLAY



DEBUG/EV FEATURE: PORT 80 DECODER & DISPLAY

SCHEMATIC TITLE: INTEL(R) PENTIUM(R) 4 SKT-N INTEL(R) B45G SDR CUSTOMER REFERENCE BOARD - 4 LAYER UATX		
PAGE TITLE: PORT 80 DECODER & DISPLAY	REV: 2.0	
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: MAY 2002	SHEET: 75