Intel® High Definition Audio Specification
Document Change Notification

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Change Identification:	**DCN No: HDA042-A**
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Document Revision:	Intel® High Definition Audio 1.0

Title: Errata on Traffic Priority and Immediate Response Read

Brief description of the functional changes:

The current definition in the HD Audio specification has defined the Traffic Priority and Immediate Response Read register field as RW attributes, but some existing HD-Audio Controller has implemented as RO. This DCN spells out the errata for that specification.

Definition Text Formatting:

xxx Original text in existing specification or DCN released earlier.
yyy New text inserted by this new DCN.
~~zzz~~ Deleted text introduced by this new DCN.

New Definitions:

3.3.35 Offset 80: {IOB}SDnCTL – Input/Output/Bidirectional Stream Descriptor *n* Control

Length: 3 bytes

Table 34. Stream Descriptor *n* Control

Bit	Type	Reset	Description
23:20	RW	0h	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal. When an input stream is detected on any of the SDATA_INx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDAT_INx input may contain data from more than one stream number, two different SDATA_INx inputs may not be configured with the same stream number. Although the controller hardware is capable of transmitting any stream number, by convention stream 0 is reserved as unused by software, so that converters whose stream numbers have been reset to 0 do not unintentionally decode data not intended for them. 0000 = *Reserved* (Indicates Unused) 0001 = Stream 1 … 1110 = Stream 14 1111 = Stream 15
19	RW	0's	**Bidirectional Direction Control (DIR):** (Bidirectional engines only. Read-only 0 for engines which are not bidirectional.) For a bidirectional engine, this bit determines the direction in which the bidirectional engine should operate. This bit can only be changed after stream reset (SRST) has been asserted and cleared and before any other stream registers have been programmed. Because setting this bit changes the fundamental behavior of the stream and the meaning of some bits, changing this bit after any other register in the stream descriptor has been written to may lead to undetermined results. 0 = Bidirectional engine is configured as an Input Engine. 1 = Bidirectional engine is configured as an Output Engine.
18	RW or RO	~~0h~~ Imp.Dep	**Traffic Priority (TP):** If set to a 1, the stream will be treated as preferred traffic if the underlying bus supports it. If set to a 0, the traffic will be handled on a "best effort" basis. The actual meaning of this bit is specific to the hardware implementation. Depending on the hardware implementation, there may be additional restrictions on the traffic, and software should assume that the buffers associated with this stream will not be snooped or cached. On PCI Express*, for example, setting the TP bit to a 1 might cause the controller to generate non-snooped isochronous traffic, while a PCI implementation may ignore this bit. It is permitted to implement this bit as RO if there is no controllability available.

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3.4.2 Offset 64h: Immediate Response Input Interface

Length: 4 bytes

Table 46. Immediate Command Input Interface

Bit	Type	Reset	Description
31:0	RO or R/W	0's	**Immediate Response Read (IRR):** The value in this register latches the last response to come in over the link. If multiple codecs responded in the same frame, which one of the responses that will be saved is indeterminate. The codec's address for the response that was latched is indicated in the ICRADD field of the Immediate Command Status register if the ICRADD field is implemented. Note that there is no defined usage for SW to write to this register, and therefore it is recommended to be implemented as RO attribute. RW attribute is kept as an option for compatible with earlier specification definition.

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