Intel® 865G/865GV/865PE/865P Chipset Customer Reference Board Schematics

For use with the Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide

September 2003

Document Number: 252813-002

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Revision History

Rev. No.	Description	Rev. Date
-001	Initial Release.	May 2003
-002	Added 865GV to document title	September 2003

Document Contents

This document contains a set of Customer Board Reference (CRB) schematics for the 865G, 865GV, 865PE, and 865P chipsets. Note that the schematic diagrams for the AGP interface are only for the 865G, 865PE, and 865P chipsets.

CR-1

INTEL(R) 865G/865PE/865P CUSTOMER REFERENCE BOARD SCHEMATICS

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PAGE #	COMPONENT/FUNCTION
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55	AUDIO: AUDIO VREG
56	TPM
57	SATA: SATA HEADERS
58	FWH: MFG MODE AND RECOVERY JUMPERS
59-60	SIO: 82801EB/82801ER
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63	SIO: PARALLEL PORT
64	SIO: COM1
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66	PC SPEAKER
67	2X8 FRONT PANEL HEADER
68	FAN: FAN HEADERS (3)
69	VREG: POWER CONNECTOR: 2X10 AND 2X2
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71	VREG: 1.25V MEMORY VTT
72	VREG: BATTERY, PCIV AUX, TURN-ON SEQUENCER
73	VREG: WAKE ON PS2 AND USB
74	VREG: WAKE ON USB, MAGJACK CONN
75	VREG: 3.3V/1.5V STBY, 1.7V DAC
76	VREG: BULK DECOUPLING
77	VREG: PROCESSOR SELECT/ LAN VREG
78	VREG: CORE 1.5V
79	CORE: CPU MAIN REGULATOR (VCCP); CONTROLLER
80	CORE: CPU MAIN REGULATOR (VCCP); 1 & 2 PHASES
81	CORE: CPU MAIN REGULATOR (VCCP); 3RD PHASE
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83	CORE: VID SELECT/PASSIVE BLEED/FRONT PANEL
84	CORE: BACKSIDE & CUB DECOUPLING
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86	CORE: ITP (SMT)

DRAWING

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SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
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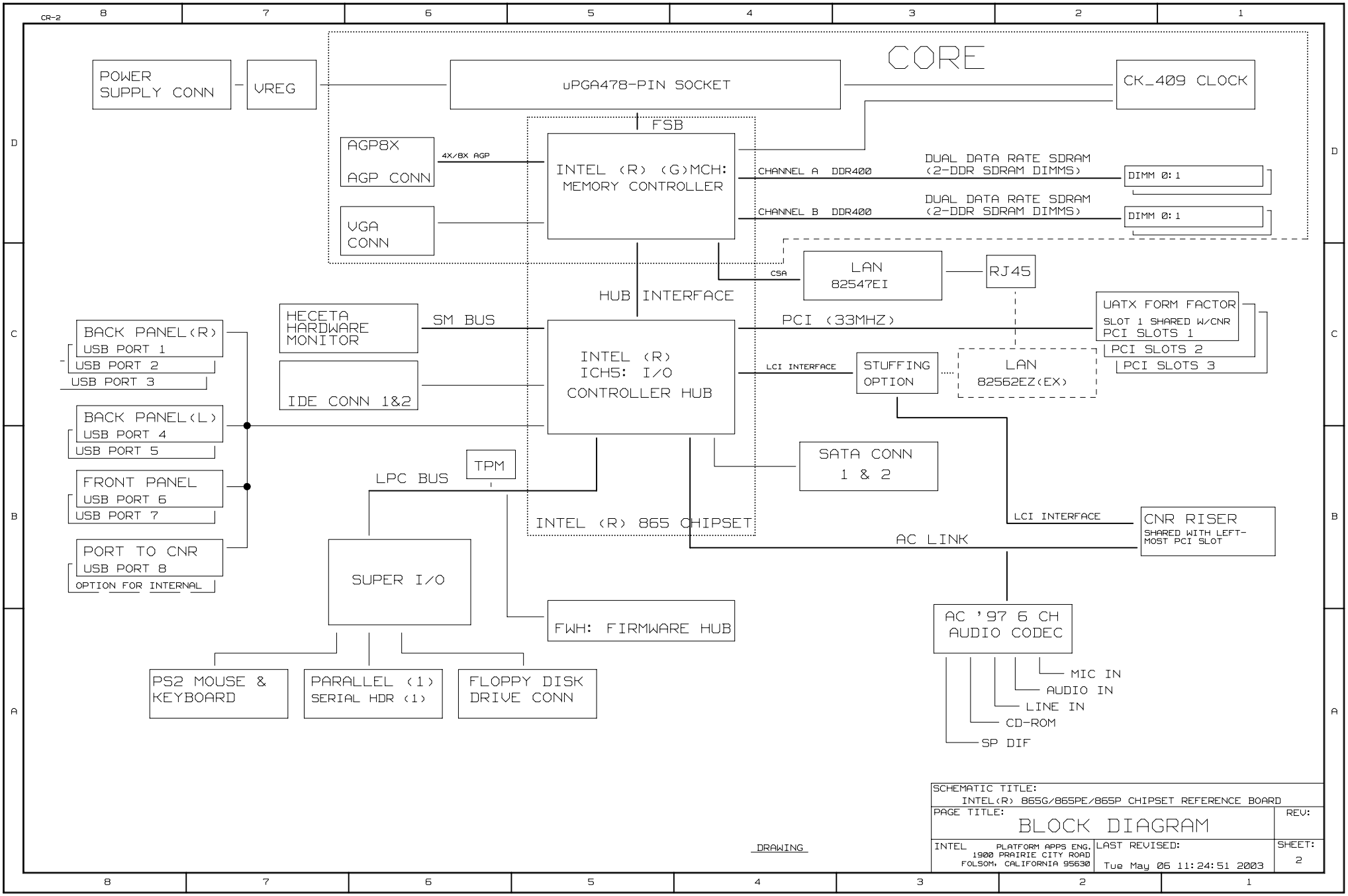
CR-2
8
7
6
5
4
3
2
1
CORE
POWER SUPPLY CONN
VREG
uPGA478-PIN SOCKET
CK_409 CLOCK
FSB
AGP8X
AGP CONN
4X/8X AGP
INTEL (R) (G)MCH: MEMORY CONTROLLER
CHANNEL A DDR400
DUAL DATA RATE SDRAM (2-DDR SDRAM DIMMS)
DIMM 0:1
CHANNEL B DDR400
DUAL DATA RATE SDRAM (2-DDR SDRAM DIMMS)
DIMM 0:1
VGA CONN
CSA
LAN 82547EI
RJ45
HUB INTERFACE
HECETA HARDWARE MONITOR
SM BUS
PCI (33MHZ)
UATX FORM FACTOR
SLOT 1 SHARED W/CNR PCI SLOTS 1
PCI SLOTS 2
PCI SLOTS 3
BACK PANEL(R)
USB PORT 1
USB PORT 2
USB PORT 3
INTEL (R) ICH5: I/O CONTROLLER HUB
LCI INTERFACE
STUFFING OPTION
LAN 82562EZ(EX)
IDE CONN 1&2
BACK PANEL(L)
USB PORT 4
USB PORT 5
SATA CONN 1 & 2
TPM
LPC BUS
FRONT PANEL
USB PORT 6
USB PORT 7
INTEL (R) 865 CHIPSET
LCI INTERFACE
CNR RISER
SHARED WITH LEFT-MOST PCI SLOT
AC LINK
PORT TO CNR
USB PORT 8
OPTION FOR INTERNAL
SUPER I/O
AC '97 6 CH AUDIO CODEC
MIC IN
AUDIO IN
LINE IN
CD-ROM
SP DIF
FWH: FIRMWARE HUB
PS2 MOUSE & KEYBOARD
PARALLEL (1) SERIAL HDR (1)
FLOPPY DISK DRIVE CONN
DRAWING
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
BLOCK DIAGRAM
REV:
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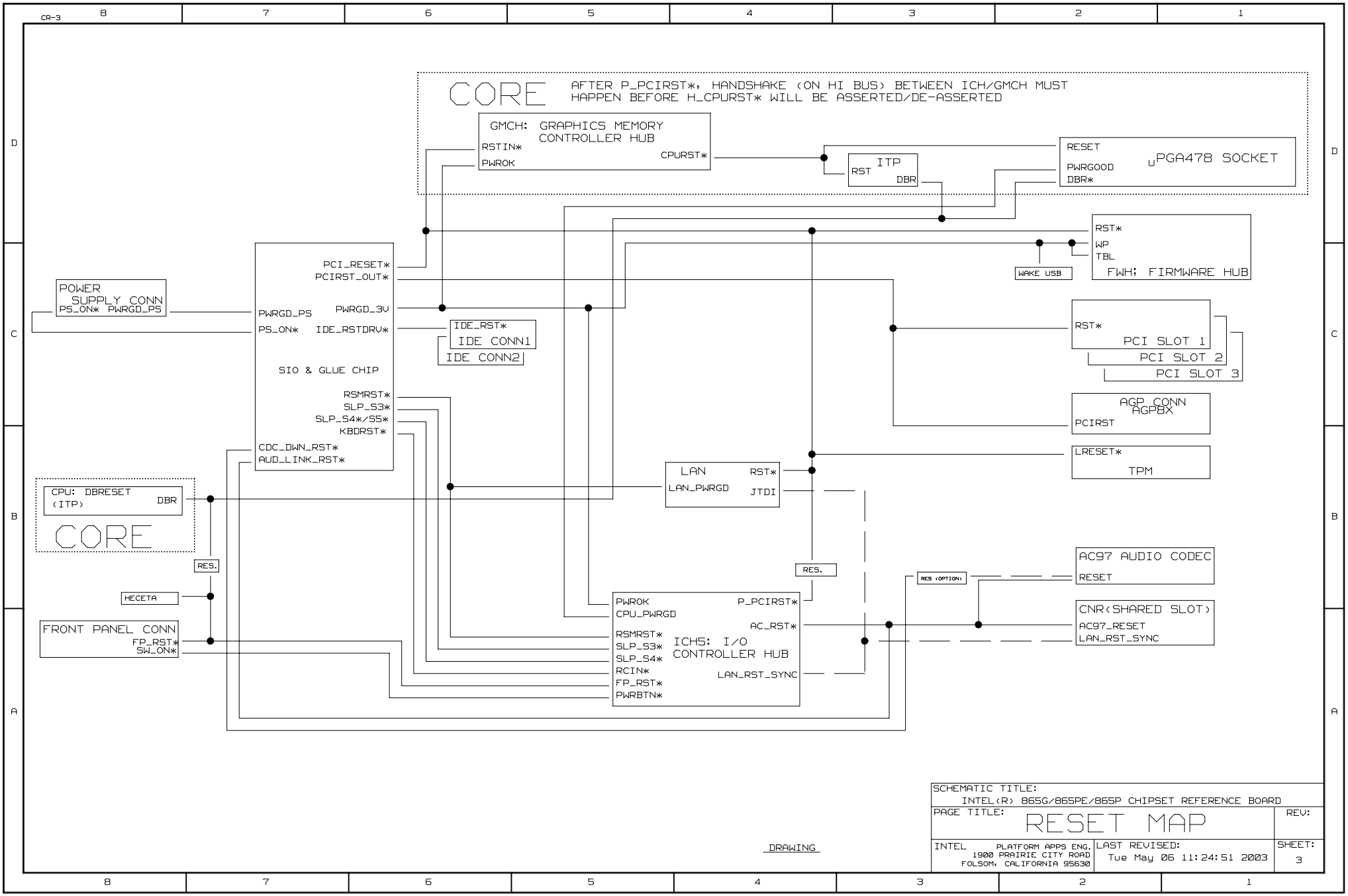
CR-3
CORE
AFTER P_PCIRST*, HANDSHAKE (ON HI BUS) BETWEEN ICH/GMCH MUST HAPPEN BEFORE H_CPURST* WILL BE ASSERTED/DE-ASSERTED
GMCH: GRAPHICS MEMORY CONTROLLER HUB
RSTIN*
PWROK
CPURST*
ITP
RST
DBR
RESET
PWRGOOD
DBR*
uPGA478 SOCKET
RST*
WP
TBL
FWH; FIRMWARE HUB
WAKE USB
POWER SUPPLY CONN
PS_ON* PWRGD_PS
PCI_RESET*
PCIRST_OUT*
PWRGD_PS
PWRGD_3V
PS_ON*
IDE_RSTDRV*
IDE_RST*
IDE CONN1
IDE CONN2
SIO & GLUE CHIP
RSMRST*
SLP_S3*
SLP_S4*/S5*
KBDRST*
CDC_DWN_RST*
AUD_LINK_RST*
RST*
PCI SLOT 1
PCI SLOT 2
PCI SLOT 3
AGP CONN
AGP8X
PCIRST
LRESET*
TPM
LAN
LAN_PWRGD
RST*
JTDI
CPU: DBRESET (ITP)
DBR
CORE
RES.
HECETA
FRONT PANEL CONN
FP_RST*
SW_ON*
PWROK
CPU_PWRGD
P_PCIRST*
AC_RST*
RSMRST*
SLP_S3*
SLP_S4*
RCIN*
FP_RST*
PWRBTN*
ICH5: I/O CONTROLLER HUB
LAN_RST_SYNC
RES. (OPTION)
AC97 AUDIO CODEC
RESET
CNR (SHARED SLOT)
AC97_RESET
LAN_RST_SYNC
DRAWING
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
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RESET MAP
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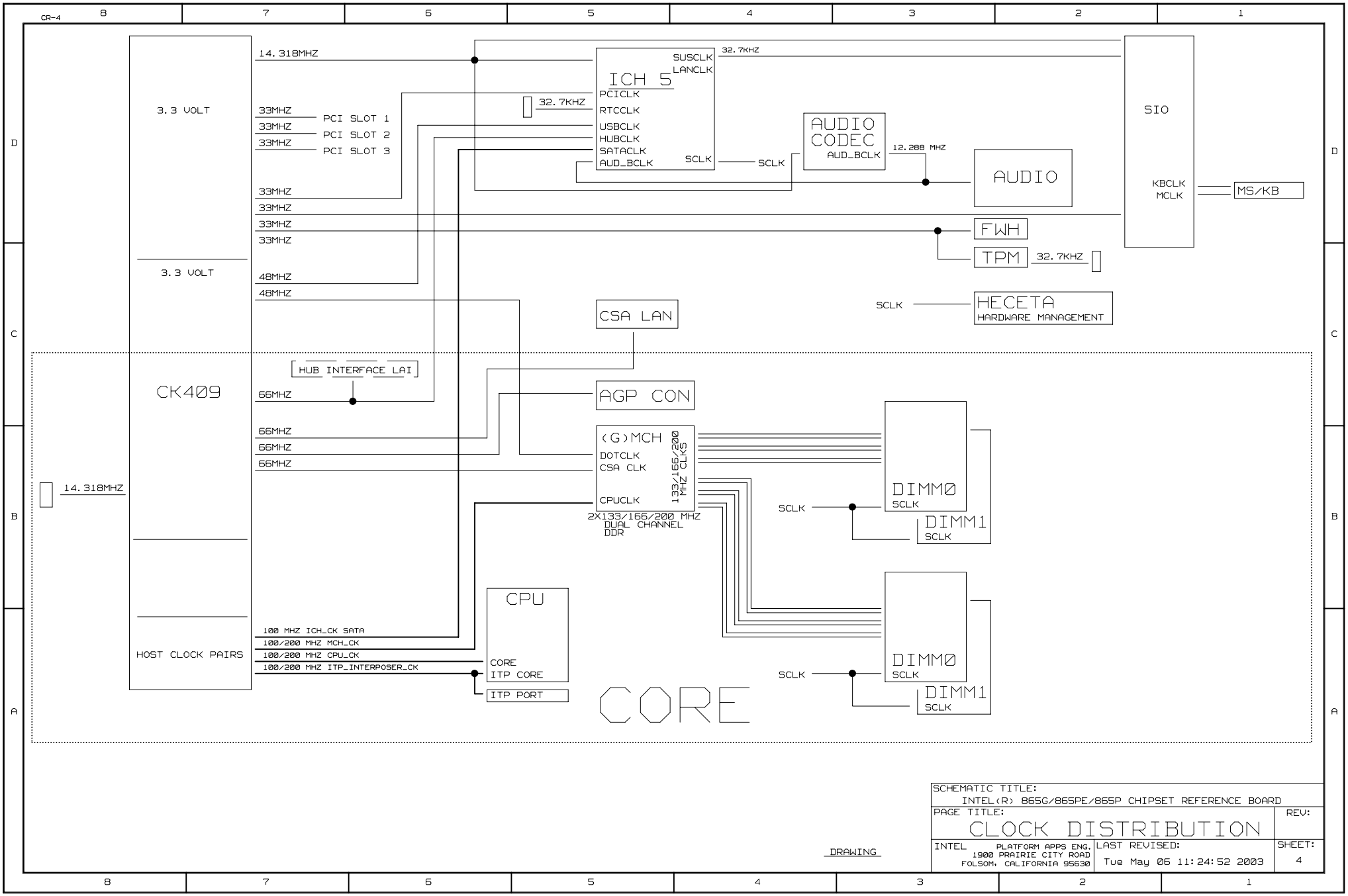

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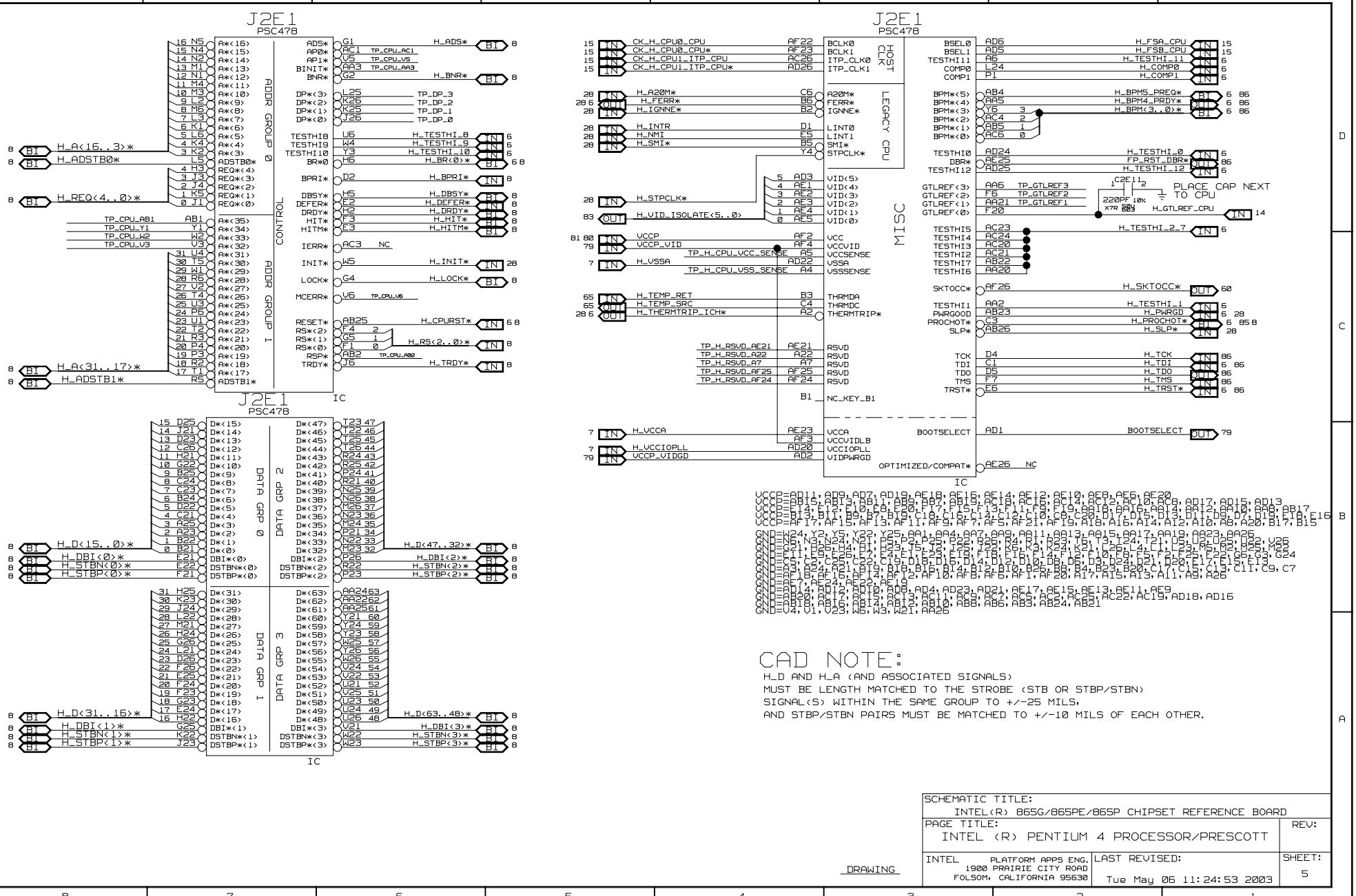

VCCP=AD11,AD9,AD7,AD19,AE18,AE16,AE14,AE12,AE10,AE8,AE6,AE20
VCCP=AB15,AB13,AB11,AB9,AB7,AB19,AC18,AC16,AC14,AC12,AC10,AC8,AD17,AD15,AD13
VCCP=T14,T12,T10,T8,T20,T17,T15,T13,T11,T9,T19,AD18,AA16,AB14,AA12,AB10,AA8,AB17
VCCP=B13,B11,B9,B7,B19,C18,C16,C14,C12,C10,C8,C20,D17,D15,D13,D11,D9,D7,D18,E16
VCCP=AF17,AF15,AF13,AF11,AF9,AF7,AF5,AF21,AF19,AF18,AF16,AF14,AF12,AF10,AF8,AF20,B17,B15

GND=W24,Y2,Y5,Y22,Y25,AA1,AA4,AA7,AA9,AA11,AA13,AA15,AA17,AA19,AA23,AA26
GND=W6,N3,N24,N21,D5,P2,P25,P22,R26,R4,R1,R23,T6,T3,T24,T21,U5,U2,U25,U22,V
GND=G21,D20,L4,J1,L23,J5,J2,J25,L22,K6,K3,K24,K21,L26,L4,L1,L23,M5,M2,M25,M22
GND=C11,C9,C26,C3,C23,C20,C17,C15,C13,D4,D1,D24,D21,E2,E25,E23,F4,F1,F26,F23
GND=A3,A24,A21,B10,B16,B14,B12,B10,B26,B8,B6,B4,B25,B20,C17,C15,C13,C11,C9,C7
GND=AF18,AF16,AF14,AF12,AF10,AF8,AF6,AF1,AF20,A17,A15,A13,A11,A9,A26
GND=AF2,AF24,AF23,AF19
GND=AD14,AD12,AD10,AD8,AD4,AD23,AD21,AE17,AE15,AE13,AE11,AE9
GND=AB20,AC17,AC15,AC13,AC11,AC9,AC7,AC5,AC2,AC25,AC22,AC19,AD18,AD16
GND=AB16,AB14,AB12,AB10,AB8,AB6,AB3,AB24,AB21
GND=V4,V1,V23,W5,W3,W21,AA25

CAD NOTE:

H_D AND H_A (AND ASSOCIATED SIGNALS)
MUST BE LENGTH MATCHED TO THE STROBE (STB OR STBP/STBN)
SIGNAL(S) WITHIN THE SAME GROUP TO +/-25 MILS,
AND STBP/STBN PAIRS MUST BE MATCHED TO +/-10 MILS OF EACH OTHER.

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SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD

PAGE TITLE:
INTEL (R) PENTIUM 4 PROCESSOR/PRESCOTT

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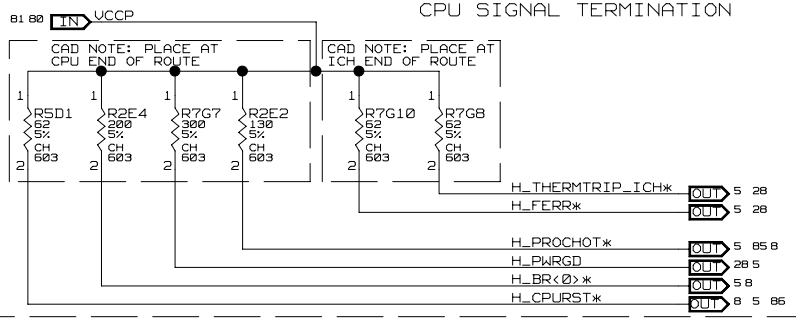
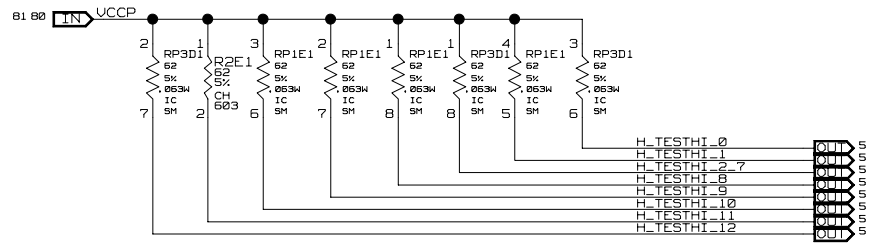
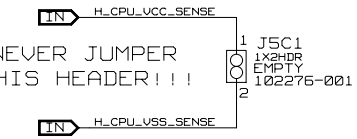
CPU SIGNAL TERMINATION



TESTHI PULLUPS

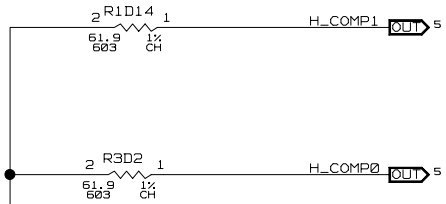




DESIGN NOTE: NO JUMPER SHOULD BE USED HERE
THE PINS WILL BE USED AS TEST/PROBE POINTS ONLY.

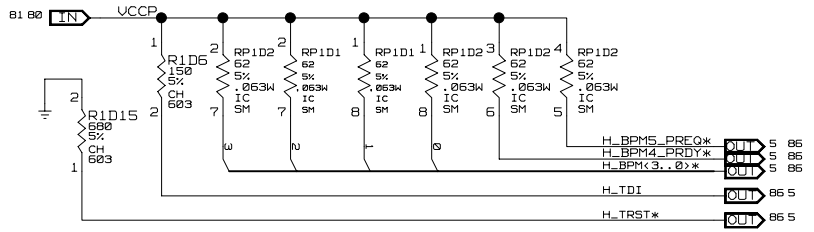
CAD NOTE:
PLACE HEADER AS CLOSE TO CPU PINS AS POSSIBLE

PRECISION FSB COMPENSATION RESISTORS



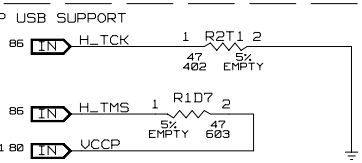
PLACE RESISTORS OUTSIDE SOCKET CAVITY
IF NO ROOM FOR VARIABLE RESISTOR DO NOT PLACE.

ITP/TAP TERMINATION



CAD NOTE: PLACE THESE RESISTORS CLOSE TO THE CPU SOCKET

ITP USB SUPPORT



PLACE R751 OUTSIDE SOCKET CAVITY

STUFF FOR USB ITP

CAD NOTE:
PLACE R750 ON BACK SIDE
OF BOARD NEXT TO CPU PIN

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SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE: CPU PULLUPS/PULLDNS/TERMINATION	REV:
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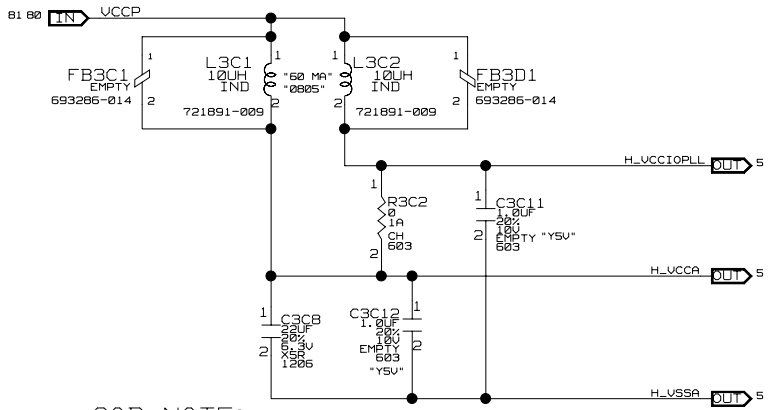
PLL SUPPLY FILTER



CAD NOTE:

PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET

TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MIL

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SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: PLL SUPPLY FILTER		REV:
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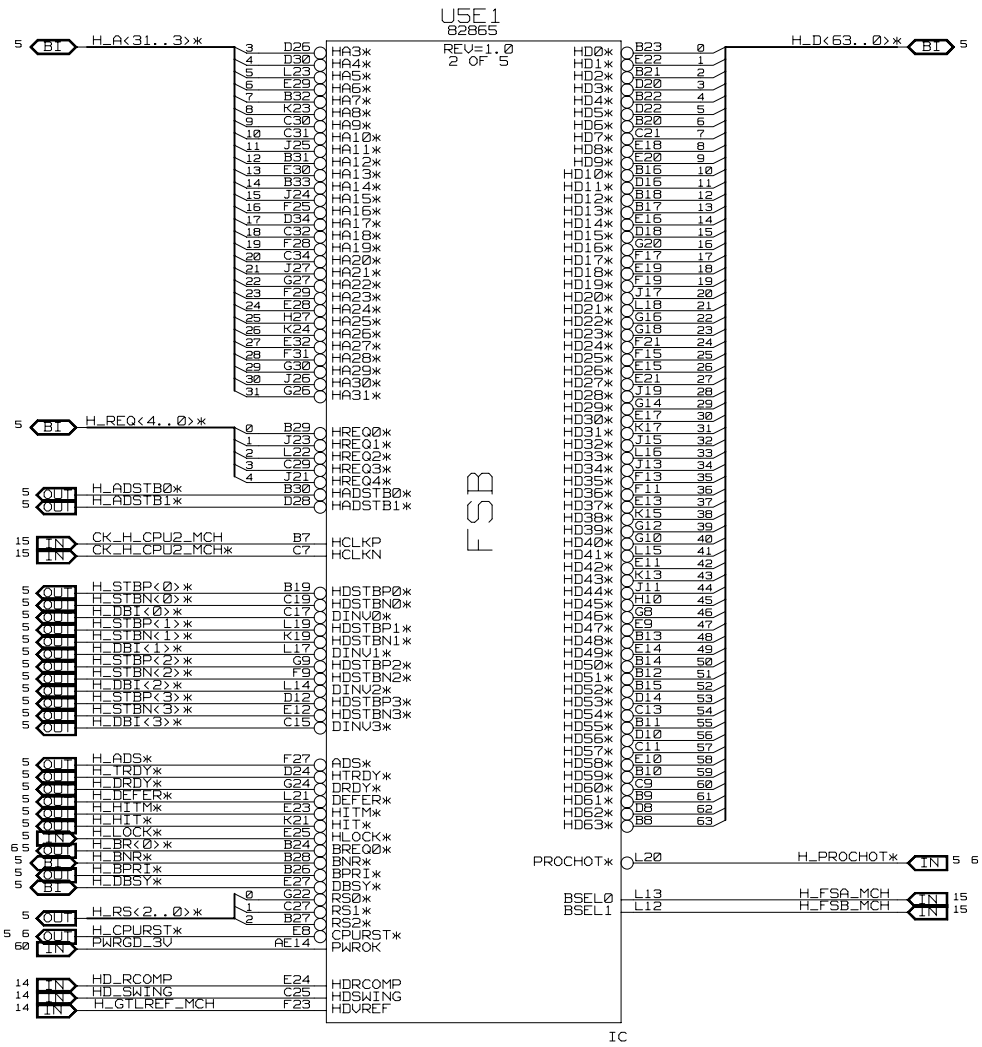

SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD

PAGE TITLE:
INTEL(R) 865G/865PE/865P CHIPSET(G)MCH
PART 1 OF 5

REV:

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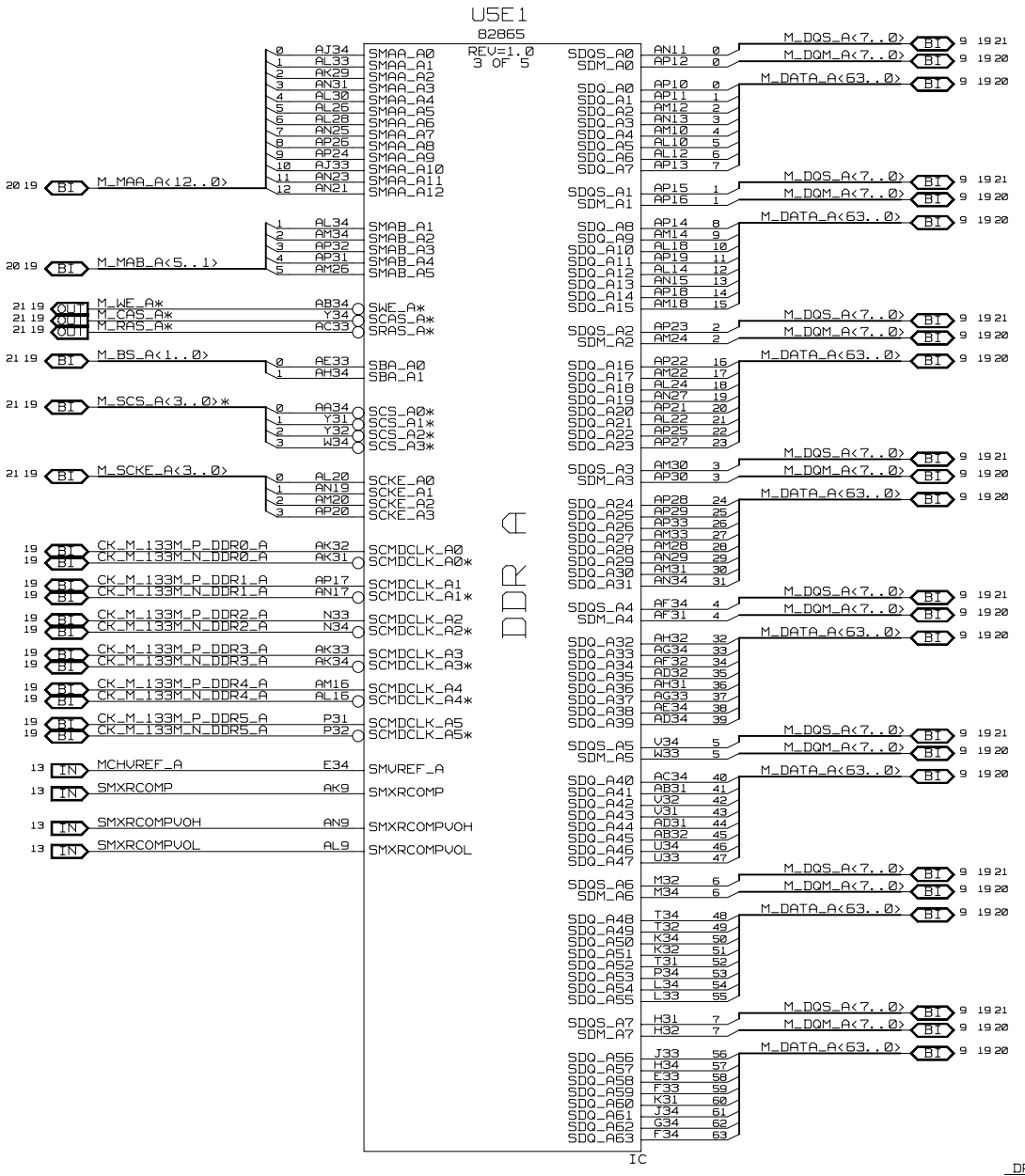

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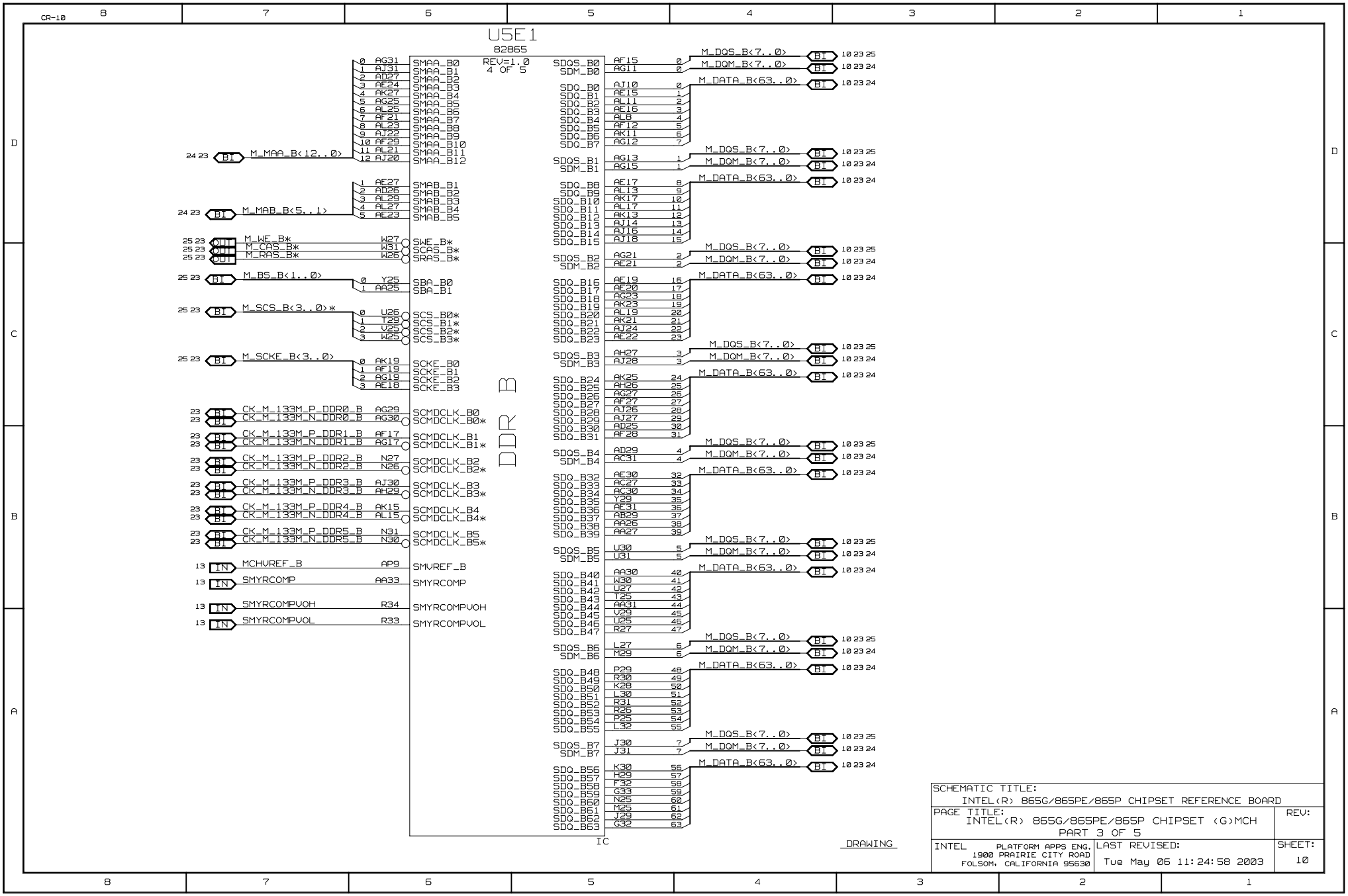
CR-10
8
7
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5
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1
U5E1
82865
REV=1.0
4 OF 5
DDR B
IC
M_MAA_B<12..0>
M_MAB_B<5..1>
M_WE_B*
M_CAS_B*
M_RAS_B*
M_BS_B<1..0>
M_SCS_B<3..0>*
M_SCKE_B<3..0>
CK_M_133M_P_DDR0_B
CK_M_133M_N_DDR0_B
CK_M_133M_P_DDR1_B
CK_M_133M_N_DDR1_B
CK_M_133M_P_DDR2_B
CK_M_133M_N_DDR2_B
CK_M_133M_P_DDR3_B
CK_M_133M_N_DDR3_B
CK_M_133M_P_DDR4_B
CK_M_133M_N_DDR4_B
CK_M_133M_P_DDR5_B
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MCHVREF_B
SMYRCOMP
SMYRCOMPVOH
SMYRCOMPVOL
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M_DQM_B<7..0>
M_DATA_B<63..0>
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SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
INTEL(R) 865G/865PE/865P CHIPSET (G)MCH
PART 3 OF 5
REV:
INTEL
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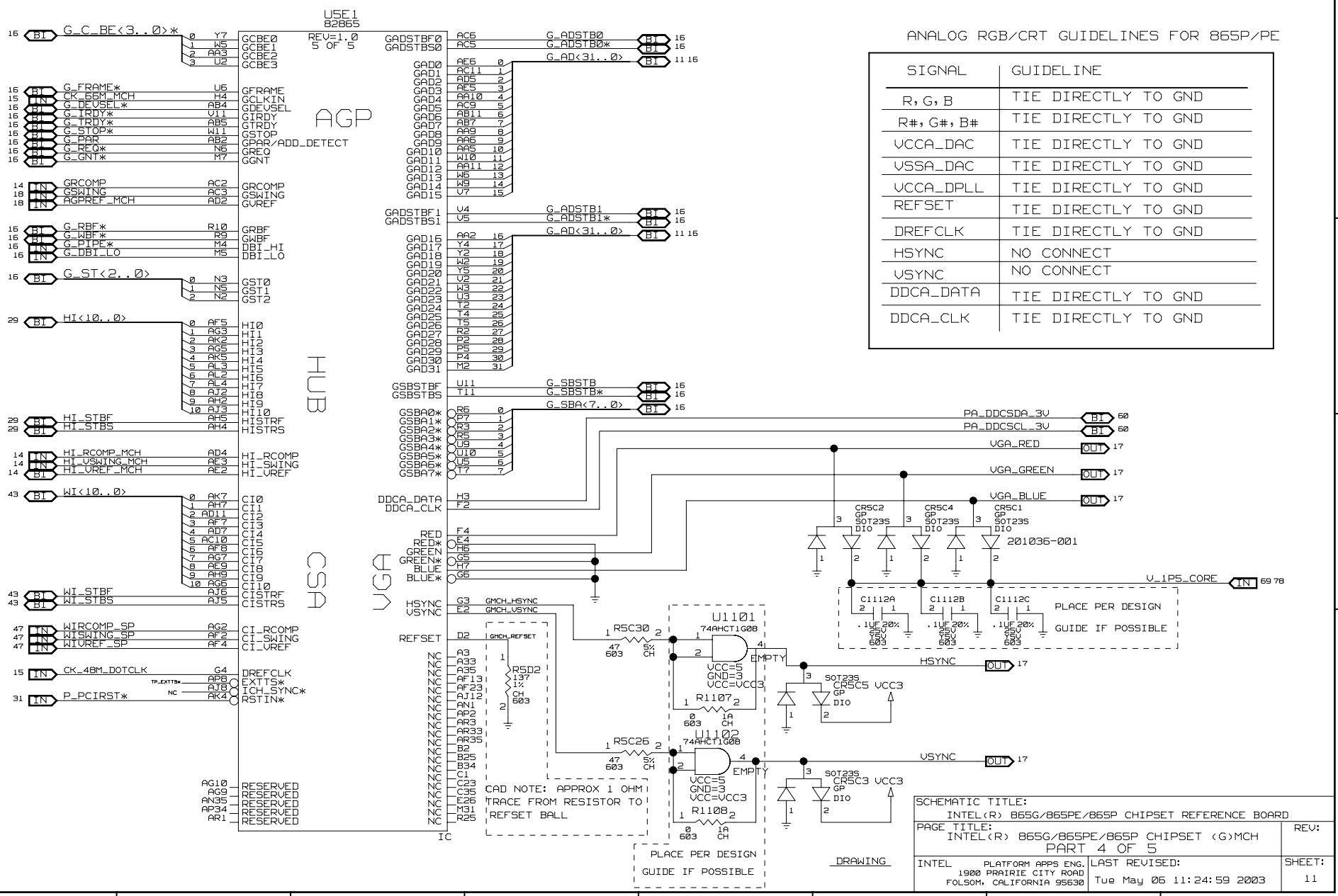
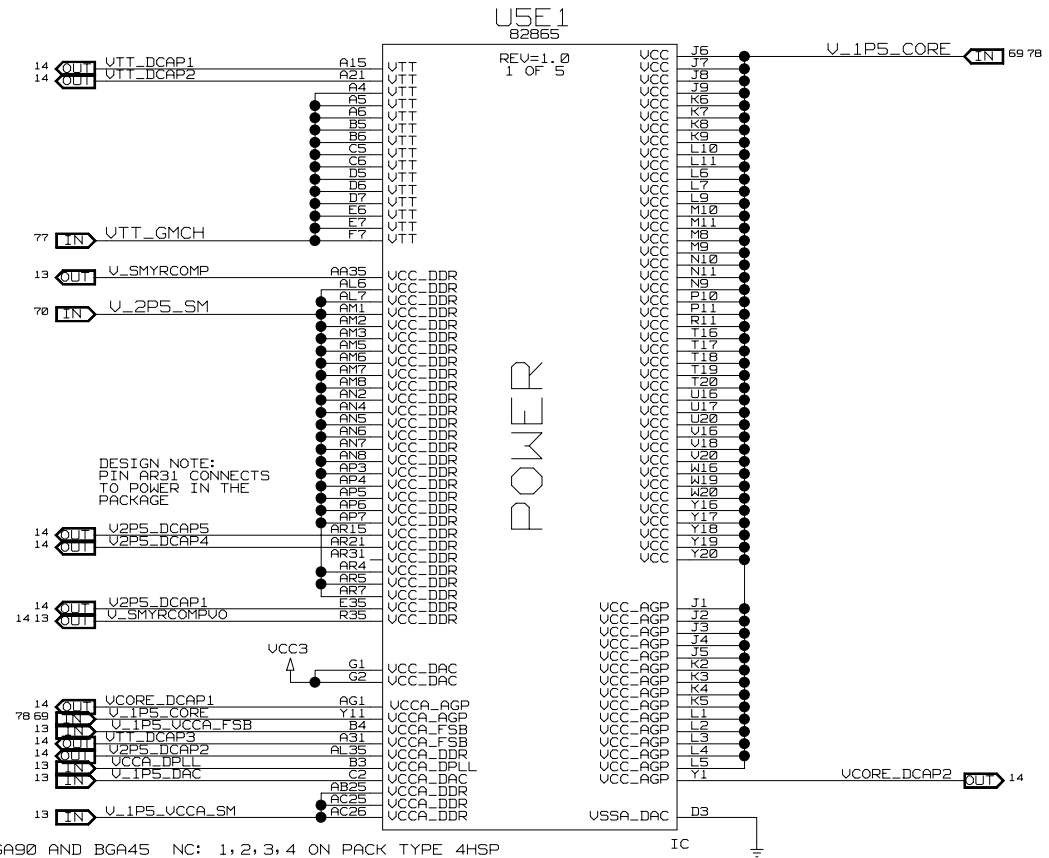
SHEET:
10


U5E1
82865
REV=1.0
5 OF 5
AGP
HUB
HSD
VGA
IC
ANALOG RGB/CRT GUIDELINES FOR 865P/PE
SIGNAL | GUIDELINE
R, G, B | TIE DIRECTLY TO GND
R#, G#, B# | TIE DIRECTLY TO GND
VCCA_DAC | TIE DIRECTLY TO GND
VSSA_DAC | TIE DIRECTLY TO GND
VCCA_DPLL | TIE DIRECTLY TO GND
REFSET | TIE DIRECTLY TO GND
DREFCLK | TIE DIRECTLY TO GND
HSYNC | NO CONNECT
VSYNC | NO CONNECT
DDCA_DATA | TIE DIRECTLY TO GND
DDCA_CLK | TIE DIRECTLY TO GND
G_C_BE<3..0>#
G_FRAME#
CK_66M_MCH
G_DEVSEL#
G_IRDY#
G_TRDY#
G_STOP#
G_PAR
G_REQ#
G_GNT#
GRCOMP
GSWING
AGPREF_MCH
G_RBF#
G_WBF#
G_PIPE#
G_DBI_LO
G_ST<2..0>
HI<10..0>
HI_STBF
HI_STBS
HI_RCOMP_MCH
HI_VSWING_MCH
HI_VREF_MCH
WI<10..0>
WI_STBF
WI_STBS
WIRCOMP_SP
WISWING_SP
WIVREF_SP
CK_48M_DOTCLK
P_PCIRST#
G_ADSTB0
G_ADSTB0#
G_AD<31..0>
G_ADSTB1
G_ADSTB1#
G_SBSTB
G_SBSTB#
G_SBA<7..0>
PA_DDCSDA_3V
PA_DDCSCL_3V
VGA_RED
VGA_GREEN
VGA_BLUE
CR5C2
CR5C4
CR5C1
SOT23S
GP
DIO
201036-001
V_1P5_CORE
C1112A
C1112B
C1112C
.1UF 20% 25V Y5V 603
PLACE PER DESIGN
GUIDE IF POSSIBLE
DDCA_DATA
DDCA_CLK
RED
RED#
GREEN
GREEN#
BLUE
BLUE#
HSYNC
VSYNC
REFSET
GMCH_HSYNC
GMCH_VSYNC
GMCH_REFSET
R5C30
R5C26
R5D2
47 603 5% CH
137 1% CH 603
U1101
U1102
74AHCT1G08
VCC=5
GND=3
VCC=VCC3
EMPTY
R1107
R1108
0 603 1A CH
CR5C5 VCC3
CR5C3 VCC3
CAD NOTE: APPROX 1 OHM TRACE FROM RESISTOR TO REFSET BALL
PLACE PER DESIGN
GUIDE IF POSSIBLE
DRAWING
RESERVED
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
INTEL(R) 865G/865PE/865P CHIPSET (G)MCH
PART 4 OF 5
REV:
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue May 06 11:24:59 2003
SHEET:
11

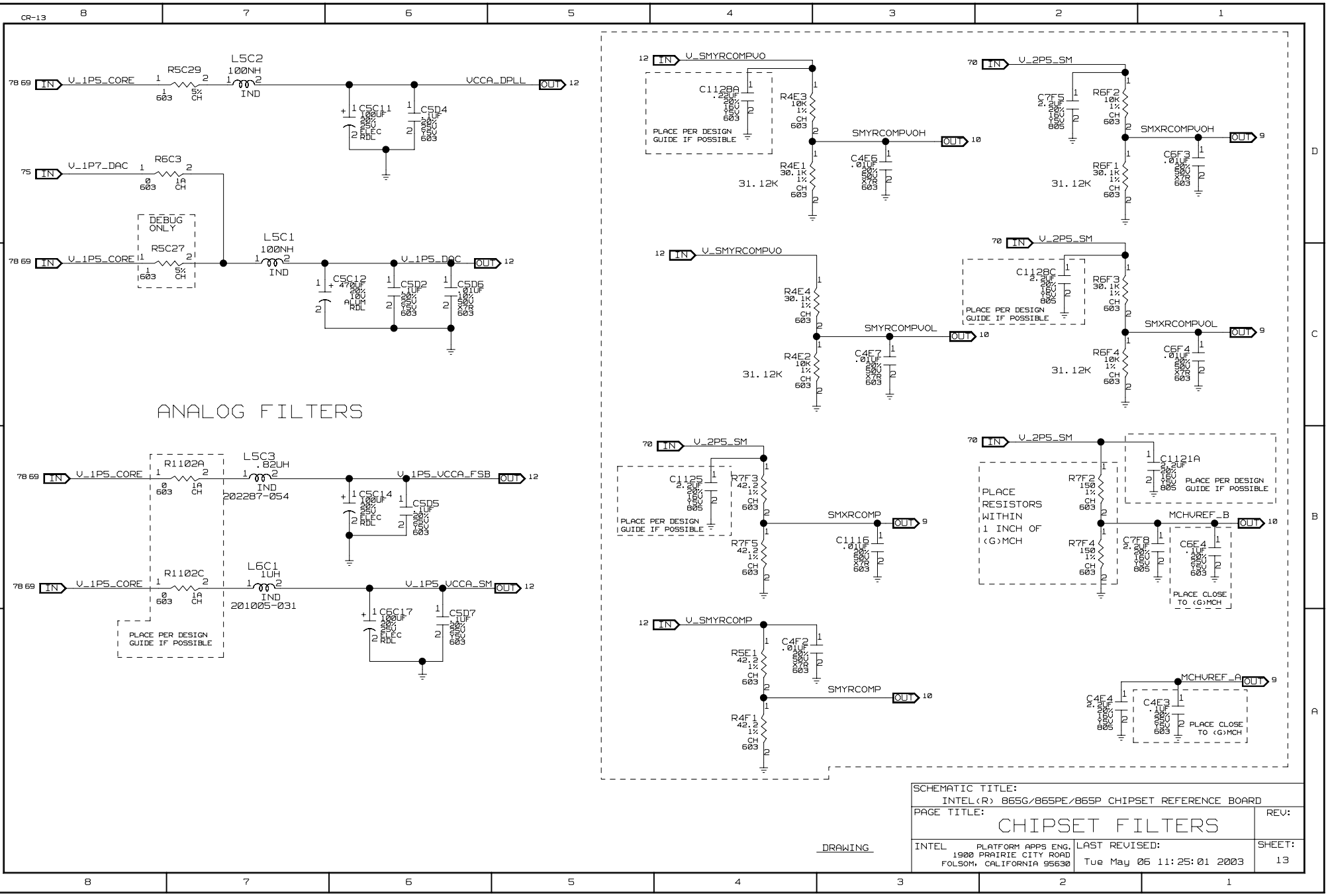


NC: 1, 2, 3, 4, 5, 6, 7, 8 ON PACK TYPE BGA90 AND BGA45 NC: 1, 2, 3, 4 ON PACK TYPE 4HSP

GND: A11, A13, A16, A20, A23, A25, A27, A29, A32, A7, A9, AA1, AA32, AA4, AB10, AB26, AB27, AB28, AB3, AB30, AB33, AB6, AB8, AB9, AC1, AC32, AC35, AC4, AD10, AD28, AD3, AD30, AD33, AD6, AD8, AD9, AE1, AE10 AE11, AE12, AE13, AE25, AE26, AE32, AE35, AE4, AF11, AF14, AF16, AF18, AF20, AF22, AF24, AF25, AF3, AF30, AF33, AF6, AF9, AG14, AG16, AG18, AG20, AG22, AG24, AG26, AG28, AG32, AG35, AG4, AG8, AH10, AH12 AH14, AH16, AH18, AH20, AH22, AH24, AH3, AH30, AH33, AH6, AJ1, AJ32, AJ35, AJ4, AJ9, AK10, AK12, AK14, AK16, AK18, AK20, AK22, AK24, AK26, AK28, AK3, AK8, AL1, AL32, AM11, AM13, AM15, AM17, AM19, AM21 AM23, AM25, AM27, AM29, AM35, AM9, AN10, AN12, AN14, AN16, AN18, AN20, AN22, AN24, AN26, AN28, AN30, AN32, AR11, AR13, AR16, AR20, AR23, AR25, AR27, AR29, AR32, AR9, C10, C12, C14, C16, C18, C20, C22 C24, C26, C28, C4, C8, D1, D11, D13, D15, D17, D19, D21, D23, D25, D27, D29, D31, D33, D35, D9, E1, E3, F1, F10, F12, F14, F16, F18, F20, F22, F24, F26, F3, F5, F8, G28, G31, G35, H12, H14, H16, H18, H2, H20, H22 N4, P26, P27, P28, P3, P30, P33, P6, P8, P9, R1, R32, R4, T1, T10, T26, T27, T28, T3, T30, T33, T35, T6, T8, T9, U18, U19, U32, U4, V10, V17, V19, V26, V27, V28, V3, V30, V33, V6, V8, V9, W17, W18, W32, W4, Y10 H24, H26, H30, H33, H5, H8, H9, J10, J12, J14, J16, J18, J20, J22, J28, J32, J35, K11, K12, K14, K16, K18, K20, K22, K25, K27, K29, K33, L24, L25, L26, L31, L35, M26, M27, M28, M3, M30, M33, M6, N1, N32, N35 Y26, Y27, Y28, Y3, Y30, Y33, Y35, Y6, Y8, Y9

SCHEMATIC TITLE:	INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:	INTEL(R) 865G/865PE/865P CHIPSET (G)MCH PART 5 OF 5
REV:	
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	
LAST REVISED:	Tue May 06 11:25:00 2003
SHEET:	12

DRAWING



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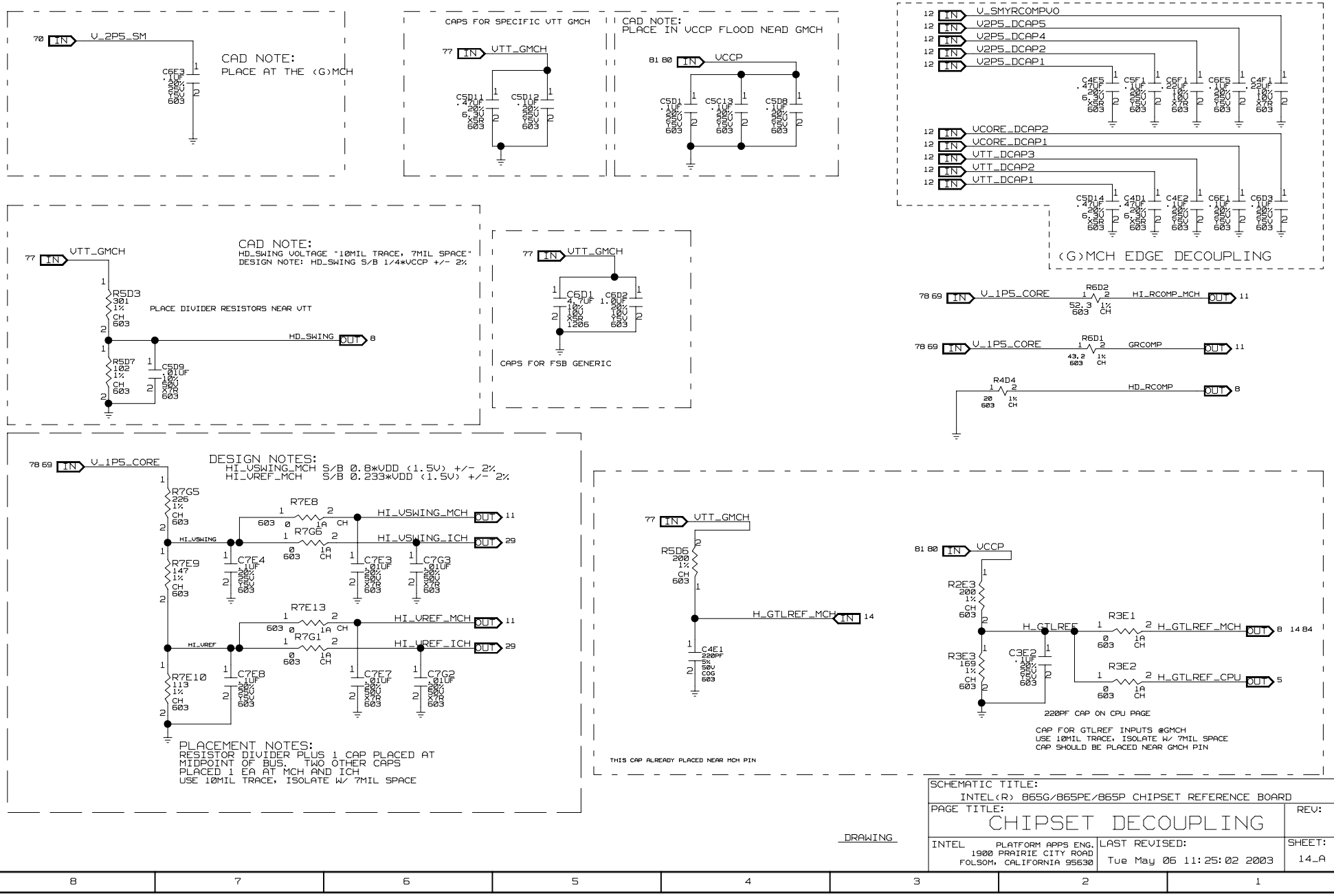
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: CHIPSET FILTERS		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:01 2003	SHEET: 13



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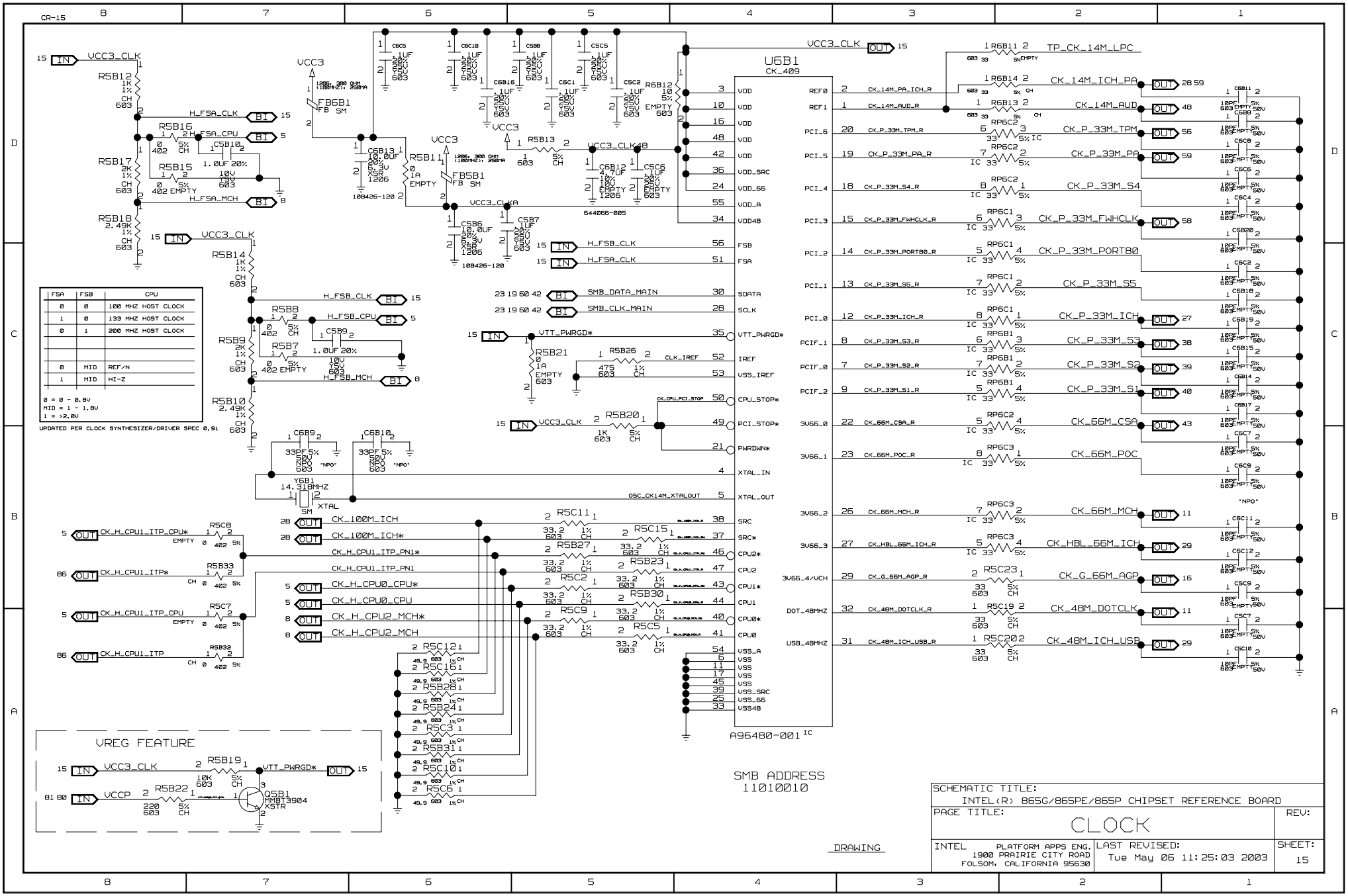
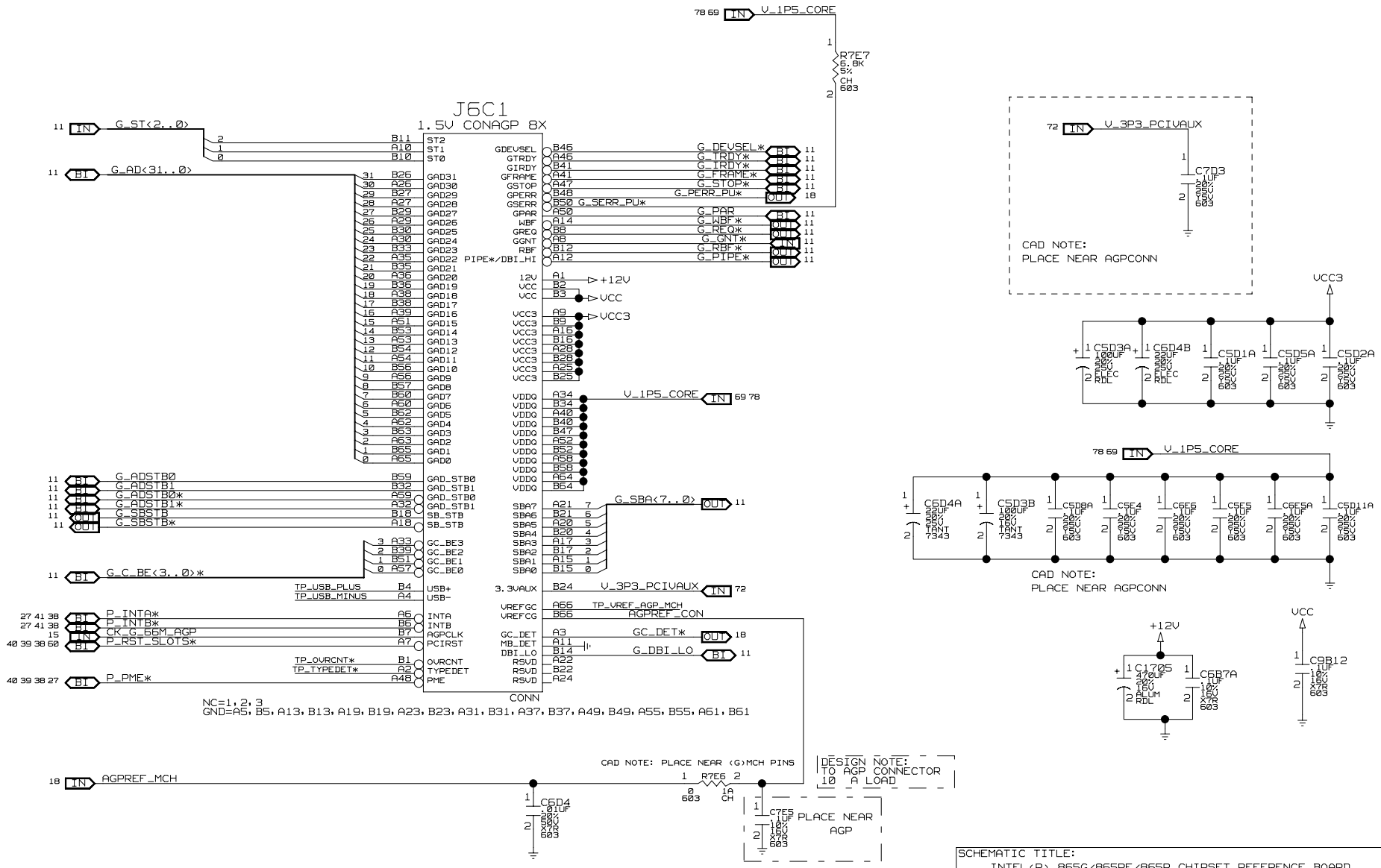
PAGE TITLE:	CHIPSET DECOUPLING
REV:	
DRAWING	
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED:	Tue May 06 11:25:02 2003
SHEET:	14_A

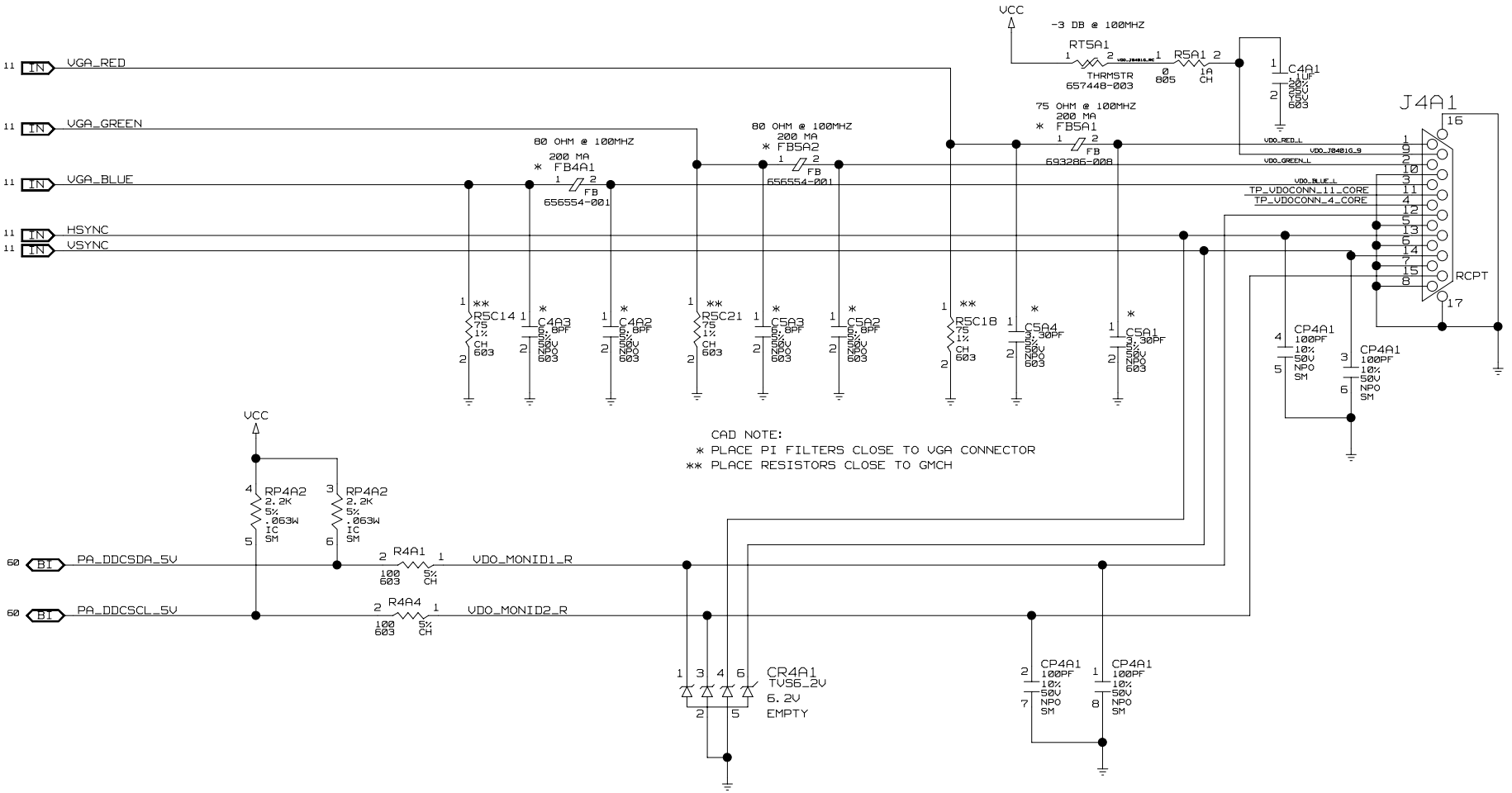


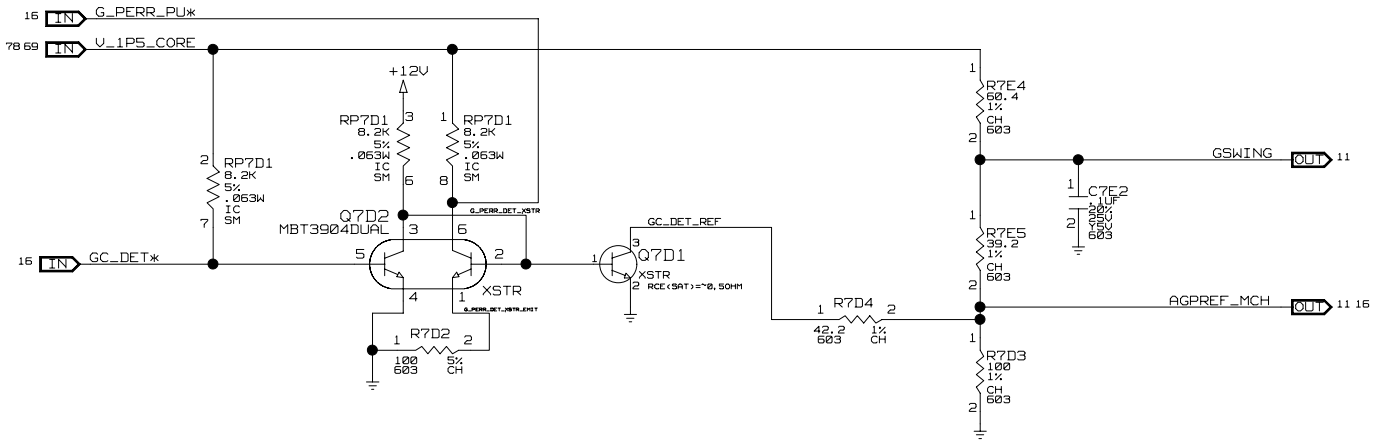
FSA	FSB	CPU
0	0	100 MHZ HOST CLOCK
1	0	133 MHZ HOST CLOCK
0	1	200 MHZ HOST CLOCK
0	MID	REF/N
1	MID	HI-Z

0 = 0 - 0.8V
MID = 1 - 1.8V
1 = >2.0V

UPDATED PER CLOCK SYNTHESIZER/DRIVER SPEC 0.91


J6C1
1.5V CONAGP 8X
CONN
V_1P5_CORE
R7E7 6.8K 5% CH 603
G_ST<2..0>
G_AD<31..0>
G_ADSTB0
G_ADSTB1
G_ADSTB0*
G_ADSTB1*
G_SBSTB
G_SBSTB*
G_C_BE<3..0>*
P_INTA*
P_INTB*
CK_G_66M_AGP
P_RST_SLOTS*
P_PME*
G_DEVSEL*
G_TRDY*
G_IRDY*
G_FRAME*
G_STOP*
G_PERR_PU*
G_SERR_PU*
G_PAR
G_WBF*
G_REQ*
G_GNT*
G_RBF*
G_PIPE*
+12V
VCC
VCC3
G_SBA<7..0>
V_3P3_PCIVAUX
TP_VREF_AGP_MCH
AGPREF_CON
GC_DET*
G_DBI_LO
TP_USB_PLUS
TP_USB_MINUS
TP_OVRCNT*
TP_TYPEDET*
NC=1, 2, 3
GND=A5, B5, A13, B13, A19, B19, A23, B23, A31, B31, A37, B37, A49, B49, A55, B55, A61, B61
AGPREF_MCH
C6D4 .01UF 20% 50V X7R 603
R7E6 0 603 1A CH
C7E5 1UF 10% 16V X7R 603
PLACE NEAR AGP
CAD NOTE: PLACE NEAR (G)MCH PINS
DESIGN NOTE:
TO AGP CONNECTOR
10 A LOAD
CAD NOTE:
PLACE NEAR AGPCONN
C7D3 .1UF 20% 25V Y5V 603
C5D3A 100UF 20% 25V ELEC RDL
C6D4B 22UF 20% 25V ELEC RDL
C5D1A .1UF 20% 25V Y5V 603
C5D5A .1UF 20% 25V Y5V 603
C5D2A .1UF 20% 25V Y5V 603
C5D4A 22UF 20% 25V TANT 7343
C5D3B 100UF 20% 16V TANT 7343
C5D8A .1UF 20% 25V Y5V 603
C5E4 .1UF 20% 25V Y5V 603
C6E6 .1UF 20% 25V Y5V 603
C5E5 .1UF 20% 25V Y5V 603
C6E5A .1UF 20% 25V Y5V 603
C5D11A .1UF 20% 25V Y5V 603
C1705 470UF 20% 16V ALUM RDL
C6B7A .1UF 10% 16V X7R 603
C9B12 .1UF 10% 16V X7R 603
AGP 4X / 8X ONLY
DRAWING
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
AGP CONNECTOR
REV:
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue May 06 11:25:05 2003
SHEET:
16


VGA_RED
VGA_GREEN
VGA_BLUE
HSYNC
VSYNC
VCC
-3 DB @ 100MHZ
RT5A1
THRMSTR
657448-003
R5A1
C4A1
1UF
J4A1
RCPT
75 OHM @ 100MHZ
200 MA
FB5A1
693286-008
80 OHM @ 100MHZ
FB4A1
656554-001
FB5A2
R5C14
R5C21
R5C18
C4A3
C5A3
C5A2
C5A4
C5A1
CP4A1
100PF
TP_VDOCONN_11_CORE
TP_VDOCONN_4_CORE
CAD NOTE:
* PLACE PI FILTERS CLOSE TO VGA CONNECTOR
** PLACE RESISTORS CLOSE TO GMCH
RP4A2
2.2K
PA_DDCSDA_5V
PA_DDCSCL_5V
R4A1
R4A4
VDO_MONID1_R
VDO_MONID2_R
CR4A1
TVS6_2V
6.2V
EMPTY
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
VGA CONNECTOR
REV:
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue May 06 11:25:06 2003
SHEET:
17
DRAWING



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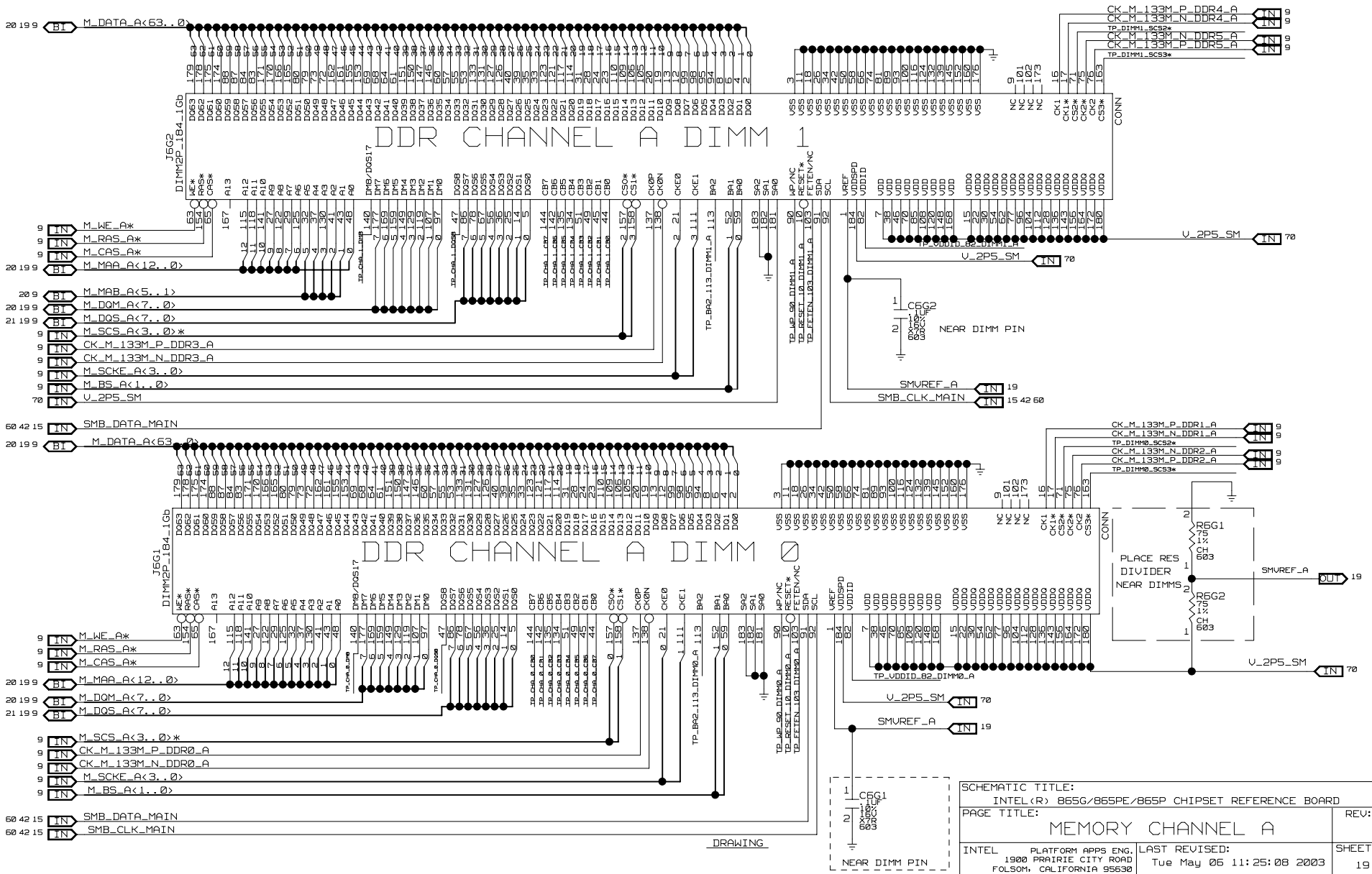
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: AGP SWING/VREF		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:07 2003	SHEET: 18


DDR CHANNEL A DIMM 1
J5G2
DIMM2P_184_1Gb
DDR CHANNEL A DIMM 0
J5G1
DIMM2P_184_1Gb
M_DATA_A<63..0>
M_MAA_A<12..0>
M_MAB_A<5..1>
M_DQM_A<7..0>
M_DQS_A<7..0>
M_SCS_A<3..0>#
M_WE_A#
M_RAS_A#
M_CAS_A#
M_SCKE_A<3..0>
M_BS_A<1..0>
CK_M_133M_P_DDR3_A
CK_M_133M_N_DDR3_A
CK_M_133M_P_DDR4_A
CK_M_133M_N_DDR4_A
CK_M_133M_N_DDR5_A
CK_M_133M_P_DDR5_A
CK_M_133M_P_DDR1_A
CK_M_133M_N_DDR1_A
CK_M_133M_N_DDR2_A
CK_M_133M_P_DDR2_A
TP_DIMM1_SCS2#
TP_DIMM1_SCS3#
TP_DIMM0_SCS2#
TP_DIMM0_SCS3#
V_2P5_SM
SMVREF_A
SMB_DATA_MAIN
SMB_CLK_MAIN
TP_VDDID_B2_DIMM1_A
TP_VDDID_B2_DIMM0_A
TP_WP_SO_DIMM1_A
TP_RESET_10_DIMM1_A
TP_FETEN_103_DIMM1_A
TP_WP_SO_DIMM0_A
TP_RESET_10_DIMM0_A
TP_FETEN_103_DIMM0_A
TP_BA2_113_DIMM1_A
TP_BA2_113_DIMM0_A
C6G2
C6G1
.1UF
10V
X5R
0603
NEAR DIMM PIN
PLACE RES DIVIDER NEAR DIMMS
R6G1
R6G2
75
1%
CONN
DRAWING
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
MEMORY CHANNEL A
REV:
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue May 06 11:25:08 2003
SHEET:
19

DDR CHANNEL A

70 IN V_1P25_MEMVTT

SPARE SECTIONS

70 IN V_1P25_MEMVTT

SPARE RPACKS

TP_RP20D2_1 — RP3G1 — 47 SM — 5% .063W IC

TP_RP2105_1 — RP3G5 — 56 SM — 5% .063W IC

199 BI M_MAB_A<5..1>

199 BI M_DQM_A<7..0>

199 BI M_DATA_A<63..0>

199 BI M_MAA_A<12..0>

RP4G6 — 47 SM — 5% .063W IC

RP4G6 — 47 SM — 5% .063W IC

RP4G4 — 47 SM — 5% .063W IC

RP4G4 — 47 SM — 5% .063W IC

RP4G1 — 47 SM — 5% .063W IC

RP6G3 — 56 SM — 5% .063W IC

RP5G1 — 56 SM — 5% .063W IC

RP5G5 — 56 SM — 5% .063W IC

RP4G3 — 56 SM — 5% .063W IC

RP3G3 — 56 SM — 5% .063W IC

R2G1 — 56 603 — 5% CH

RP2G4 — 56 SM — 5% .063W IC

RP2G6 — 56 SM — 5% .063W IC

RP1G1 — 56 SM — 5% .063W IC

RP1G1 — 56 SM — 5% .063W IC

RP2G5 — 56 SM — 5% .063W IC

RP2G5 — 56 SM — 5% .063W IC

RP1G1 — 56 SM — 5% .063W IC

RP2G6 — 56 SM — 5% .063W IC

RP2G6 — 56 SM — 5% .063W IC

RP2G4 — 56 SM — 5% .063W IC

RP2G4 — 56 SM — 5% .063W IC

RP2G3 — 56 SM — 5% .063W IC

RP2G3 — 56 SM — 5% .063W IC

RP2G5 — 56 SM — 5% .063W IC

RP2G5 — 56 SM — 5% .063W IC

RP2G3 — 56 SM — 5% .063W IC

RP2G3 — 56 SM — 5% .063W IC

RP2G2 — 56 SM — 5% .063W IC

RP2G2 — 56 SM — 5% .063W IC

RP3G5 — 56 SM — 5% .063W IC

RP3G4 — 56 SM — 5% .063W IC

RP2G2 — 56 SM — 5% .063W IC

RP2G2 — 56 SM — 5% .063W IC

RP3G5 — 56 SM — 5% .063W IC

RP3G4 — 56 SM — 5% .063W IC

RP3G4 — 56 SM — 5% .063W IC

RP3G4 — 56 SM — 5% .063W IC

RP3G3 — 56 SM — 5% .063W IC

RP3G2 — 56 SM — 5% .063W IC

RP3G2 — 56 SM — 5% .063W IC

RP3G4 — 56 SM — 5% .063W IC

RP3G3 — 56 SM — 5% .063W IC

RP3G2 — 56 SM — 5% .063W IC

RP3G2 — 56 SM — 5% .063W IC

RP4G5 — 56 SM — 5% .063W IC

RP4G5 — 56 SM — 5% .063W IC

RP4G3 — 56 SM — 5% .063W IC

RP4G2 — 56 SM — 5% .063W IC

RP4G5 — 56 SM — 5% .063W IC

RP4G5 — 56 SM — 5% .063W IC

RP4G3 — 56 SM — 5% .063W IC

RP4G2 — 56 SM — 5% .063W IC

RP4G2 — 56 SM — 5% .063W IC

RP5G5 — 56 SM — 5% .063W IC

RP5G4 — 56 SM — 5% .063W IC

RP4G2 — 56 SM — 5% .063W IC

RP5G5 — 56 SM — 5% .063W IC

RP5G4 — 56 SM — 5% .063W IC

RP5G4 — 56 SM — 5% .063W IC

RP5G2 — 56 SM — 5% .063W IC

RP5G2 — 56 SM — 5% .063W IC

RP5G1 — 56 SM — 5% .063W IC

RP5G1 — 56 SM — 5% .063W IC

RP5G2 — 56 SM — 5% .063W IC

RP5G2 — 56 SM — 5% .063W IC

RP6G1 — 56 SM — 5% .063W IC

RP6G1 — 56 SM — 5% .063W IC

RP6G1 — 56 SM — 5% .063W IC

RP6G3 — 56 SM — 5% .063W IC

RP6G2 — 56 SM — 5% .063W IC

RP6G2 — 56 SM — 5% .063W IC

RP6G1 — 56 SM — 5% .063W IC

RP6G3 — 56 SM — 5% .063W IC

RP6G2 — 56 SM — 5% .063W IC

RP6G2 — 56 SM — 5% .063W IC

R5G1 — 47 603 — 5% CH

R5G2 — 47 603 — 5% CH

RP3G1 — 47 SM — 5% .063W IC

R5G3 — 47 603 — 5% CH

RP4G1 — 47 SM — 5% .063W IC

RP4G1 — 47 SM — 5% .063W IC

R4G1 — 47 603 — 5% CH

RP4G1 — 47 SM — 5% .063W IC

RP4G4 — 47 SM — 5% .063W IC

RP4G4 — 47 SM — 5% .063W IC

RP4G6 — 47 SM — 5% .063W IC

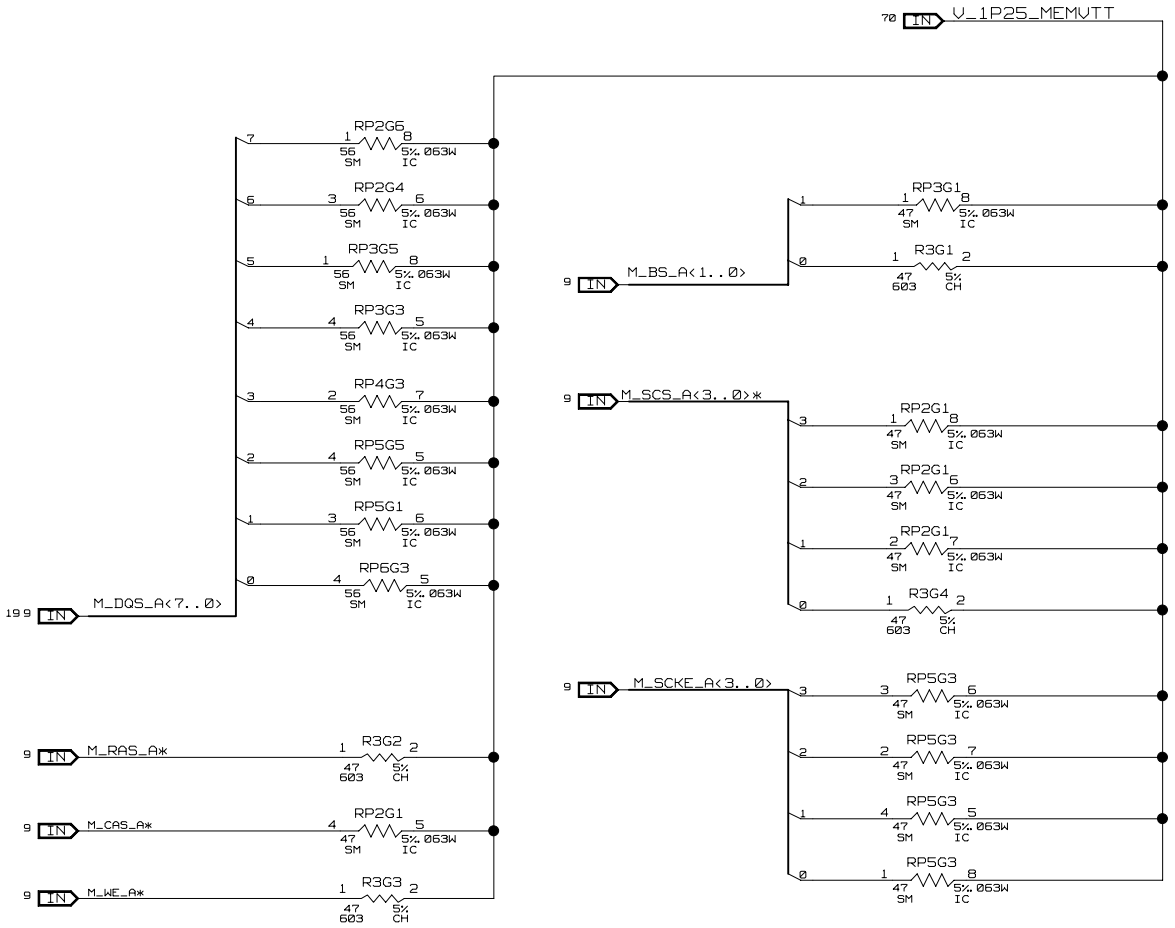
RP4G6 — 47 SM — 5% .063W IC

RP3G1 — 47 SM — 5% .063W IC

DRAWING

SCHEMATIC TITLE:	INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:	DDR RESISTOR TERMINATION
REV:	
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED:	Tue May 06 11:25:09 2003
SHEET:	20

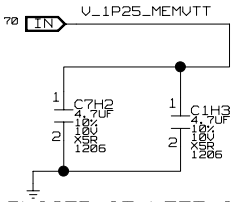
DDR CHANNEL A



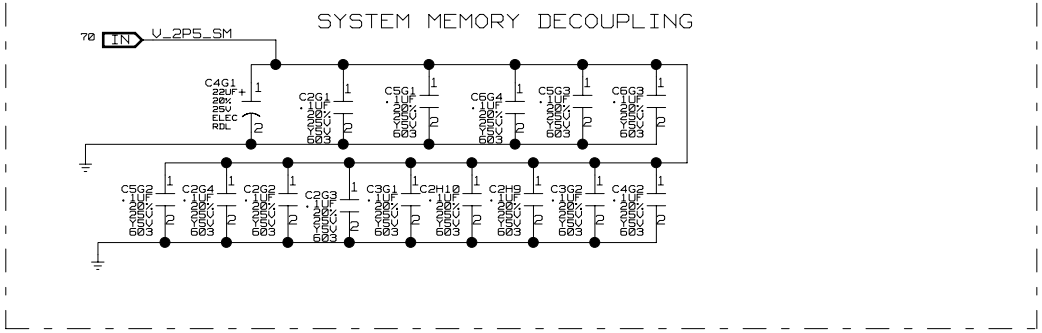
DRAWING

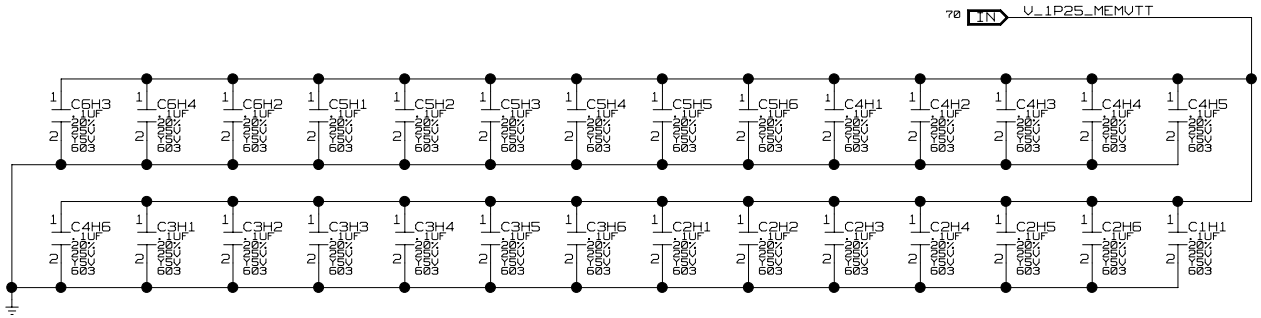
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: DDR RESISTOR TERMINATION		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:11 2003	SHEET: 21

DDR CHANNEL A



PLACED AT LEFT AND RIGHT ENDS OF VTT ISLAND

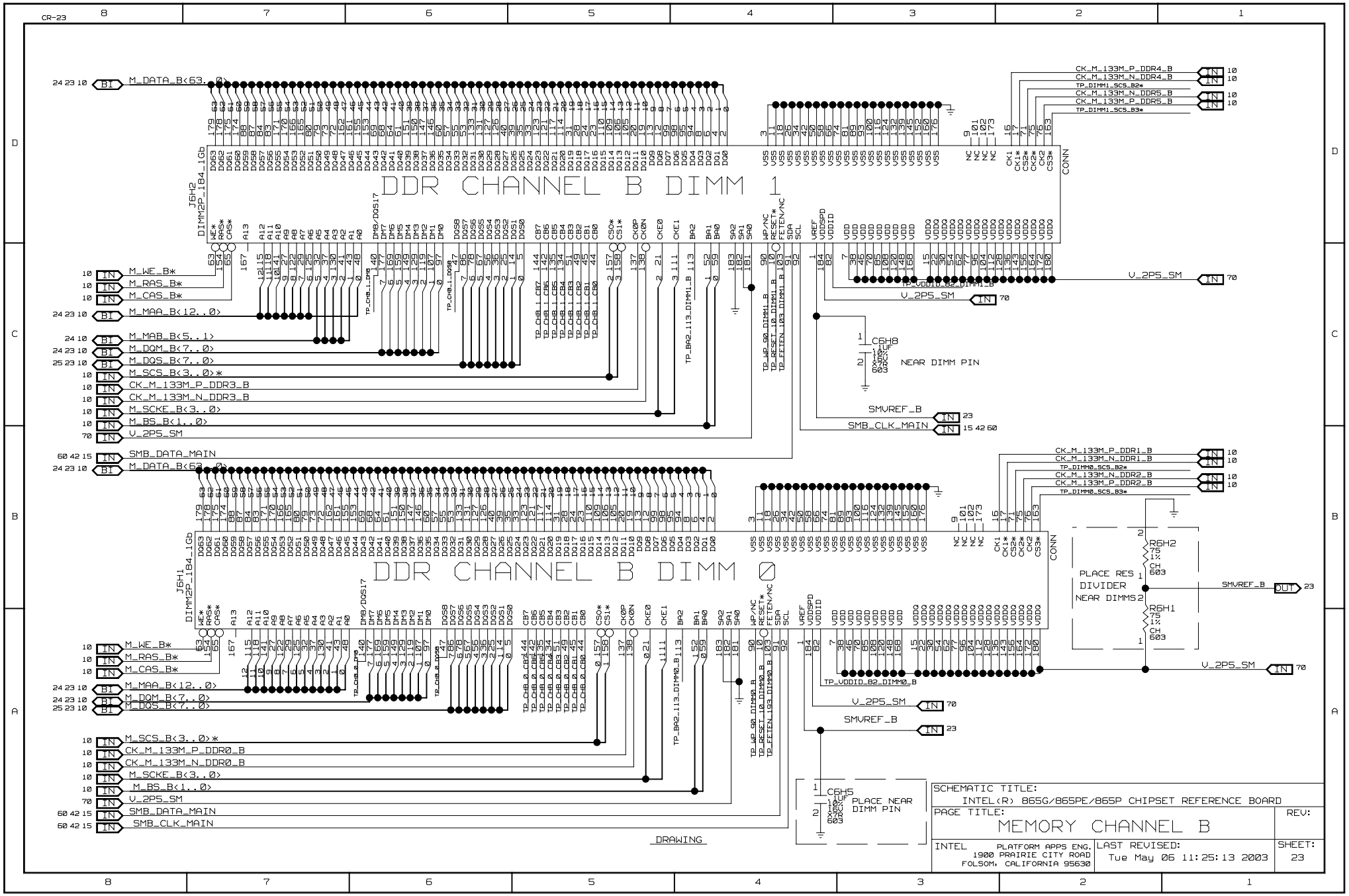




DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

DRAWING

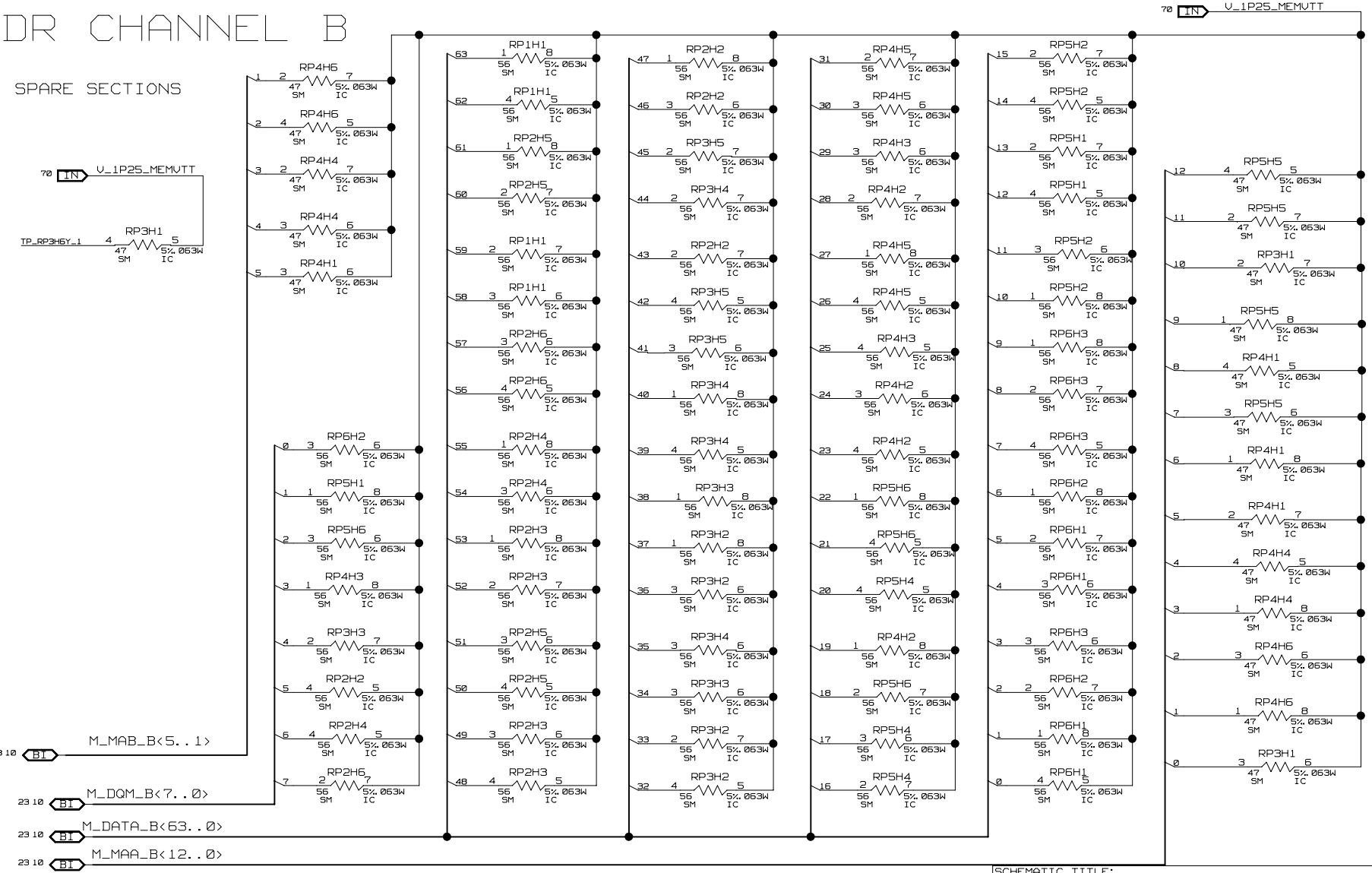
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: DECOUPLING CAPACITORS		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:12 2003	SHEET: 22



DDR CHANNEL B DIMM 1
DDR CHANNEL B DIMM 0
J6H2
DIMM2P_184_1Gb
J6H1
DIMM2P_184_1Gb
CONN
M_DATA_B<63..0>
M_WE_B*
M_RAS_B*
M_CAS_B*
M_MAA_B<12..0>
M_MAB_B<5..1>
M_DQM_B<7..0>
M_DQS_B<7..0>
M_SCS_B<3..0>*
CK_M_133M_P_DDR3_B
CK_M_133M_N_DDR3_B
M_SCKE_B<3..0>
M_BS_B<1..0>
V_2P5_SM
SMB_DATA_MAIN
SMB_CLK_MAIN
CK_M_133M_P_DDR4_B
CK_M_133M_N_DDR4_B
TP_DIMM1_SCS_B2*
CK_M_133M_N_DDR5_B
CK_M_133M_P_DDR5_B
TP_DIMM1_SCS_B3*
TP_VDDID_82_DIMM1_B
C6H8
.1UF
10%
16V
X7R
603
NEAR DIMM PIN
SMVREF_B
SMB_CLK_MAIN
CK_M_133M_P_DDR1_B
CK_M_133M_N_DDR1_B
TP_DIMM0_SCS_B2*
CK_M_133M_N_DDR2_B
CK_M_133M_P_DDR2_B
TP_DIMM0_SCS_B3*
R6H2
75
1%
CH
603
R6H1
75
1%
CH
603
PLACE RES
DIVIDER
NEAR DIMMS
TP_VDDID_82_DIMM0_B
C6H5
.1UF
10%
16V
X7R
603
PLACE NEAR
DIMM PIN
DRAWING
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
MEMORY CHANNEL B
REV:
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue May 06 11:25:13 2003
SHEET:
23

DDR CHANNEL B

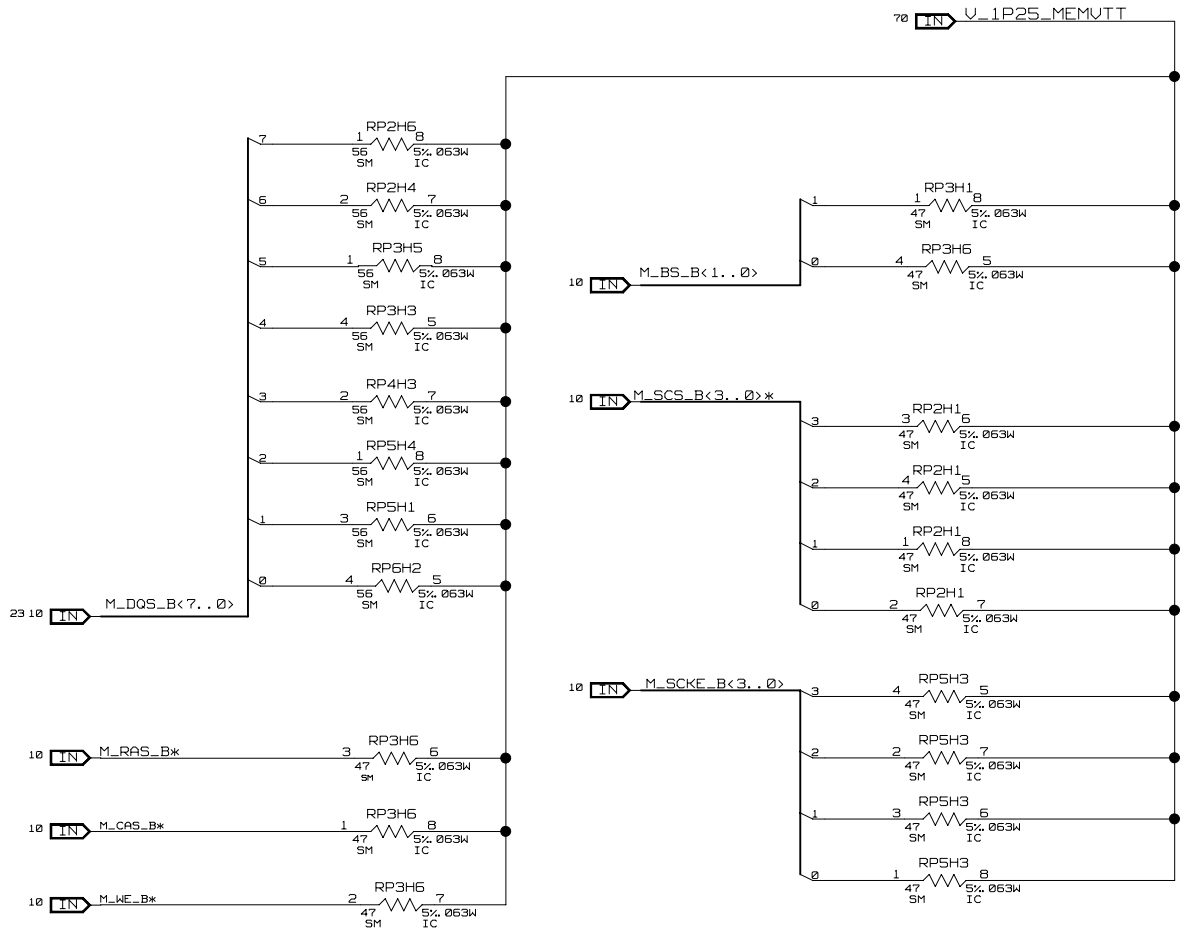
SPARE SECTIONS



DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: DDR RESISTOR TERMINATION		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:14 2003	SHEET: 24

DDR CHANNEL B



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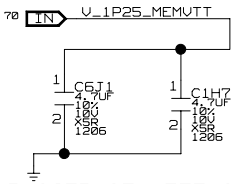
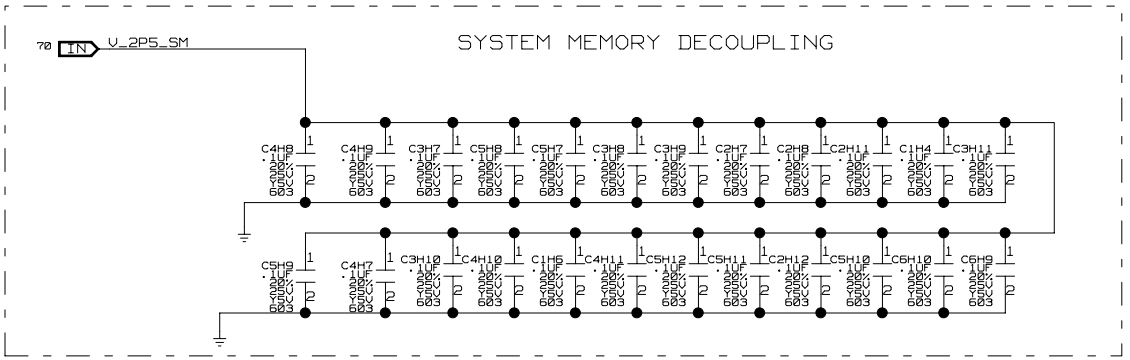
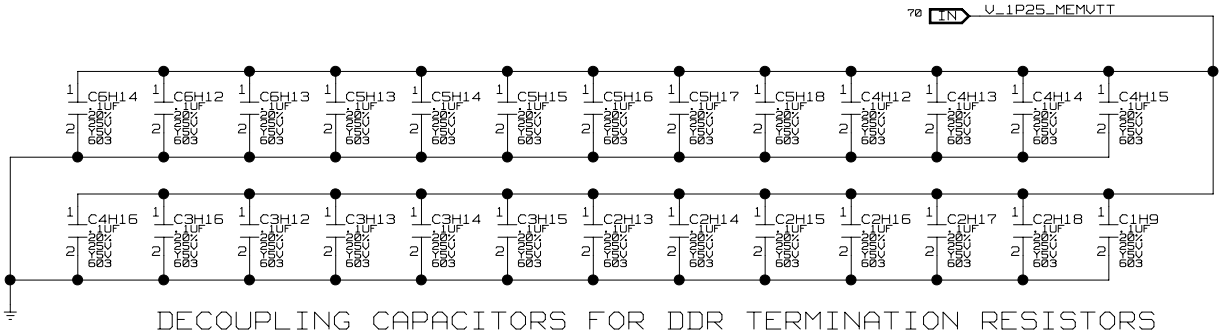
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: DDR RESISTOR TERMINATION		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:16 2003	SHEET: 25

DDR CHANNEL B



PLACED AT LEFT AND RIGHT ENDS OF VTT ISLAND

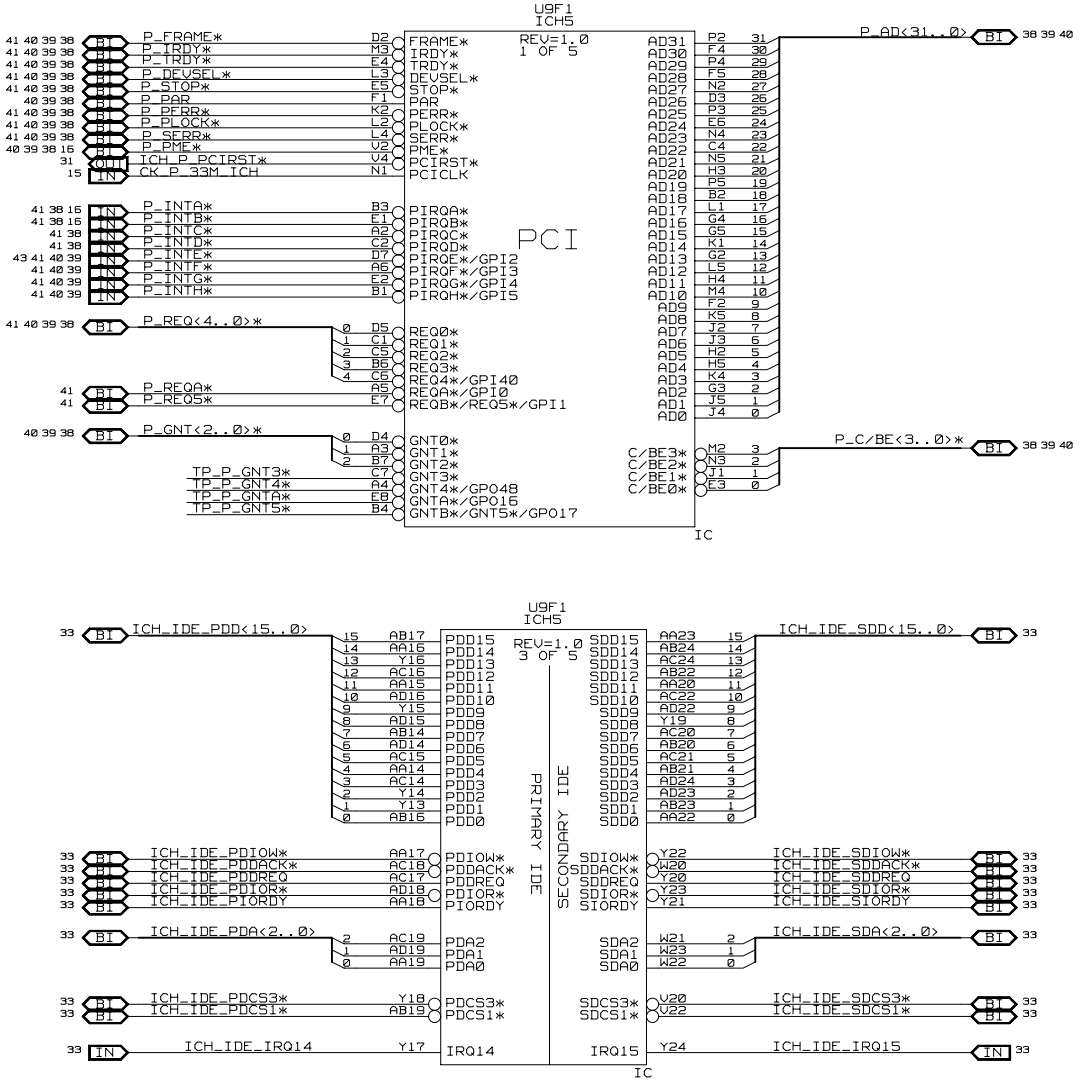




DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: DECOUPLING CAPACITORS		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:17 2003	SHEET: 26



DRAWING

SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD

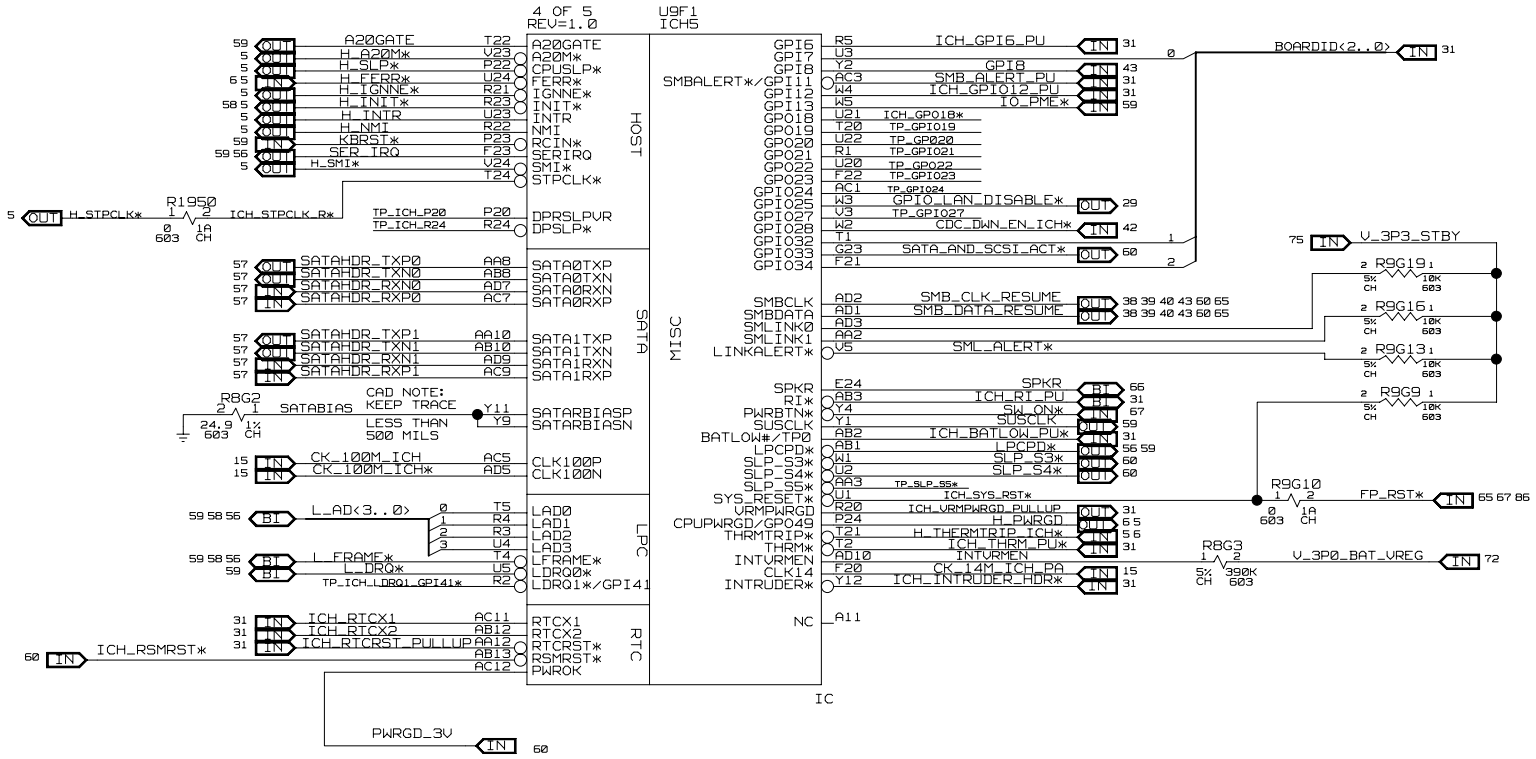
PAGE TITLE: INTEL(R) ICH5 1 OF 4

REV:

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

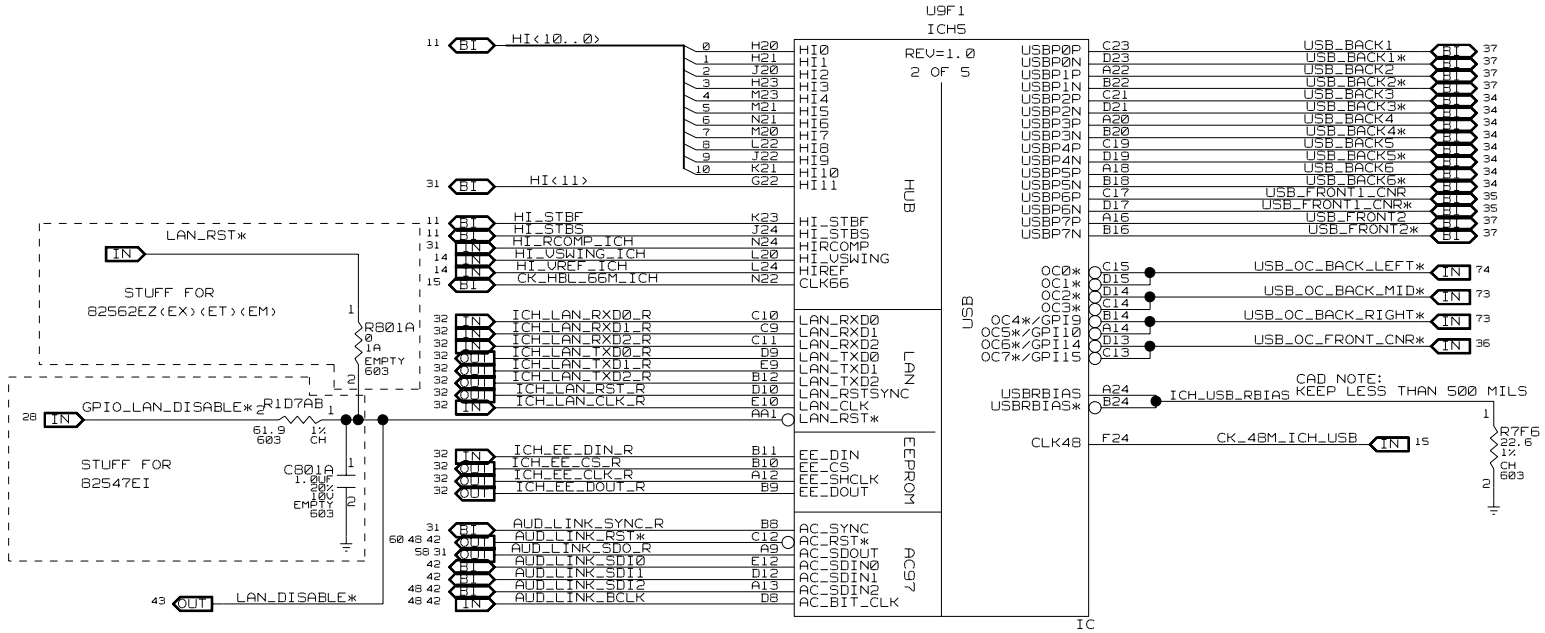
LAST REVISED: Tue May 06 11:25:18 2003

SHEET: 27



DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: INTEL(R) ICH5 2 OF 4		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:19 2003	SHEET: 28



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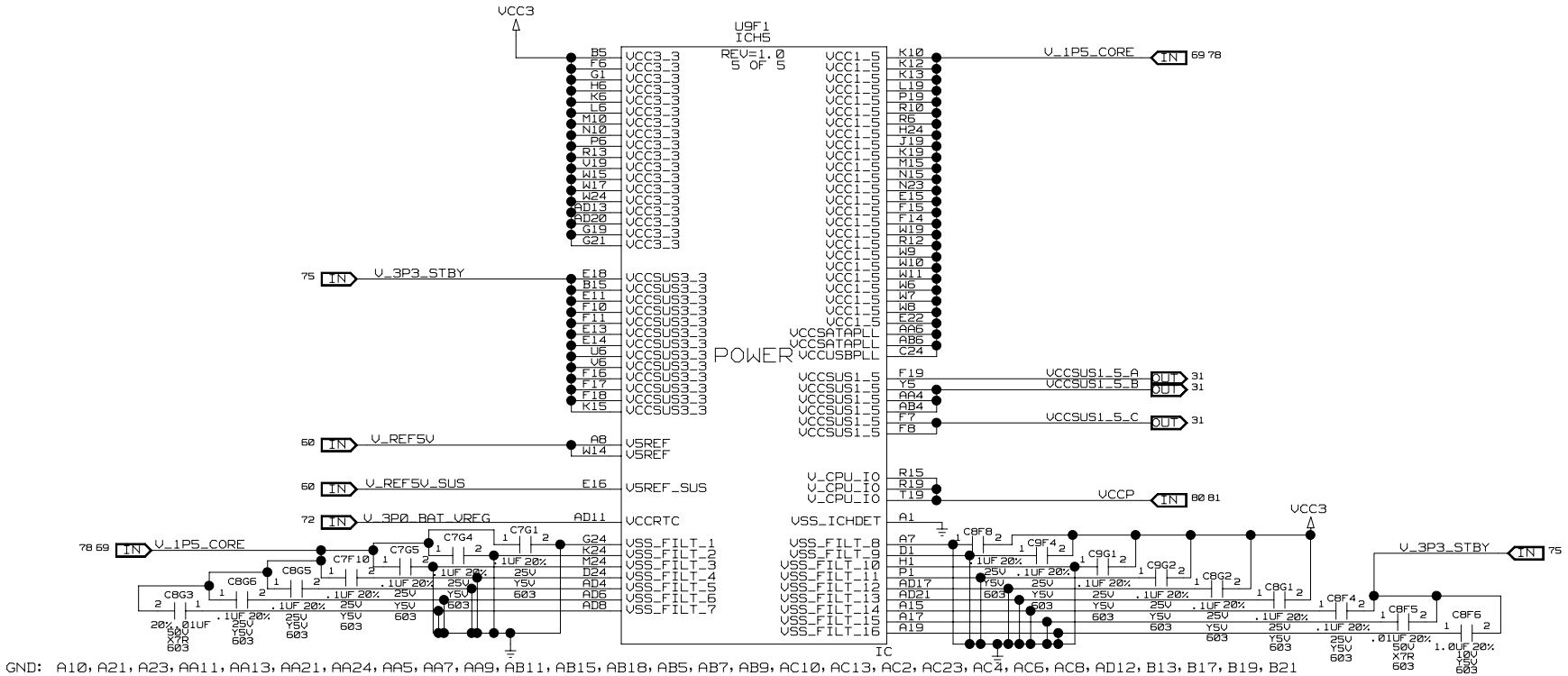
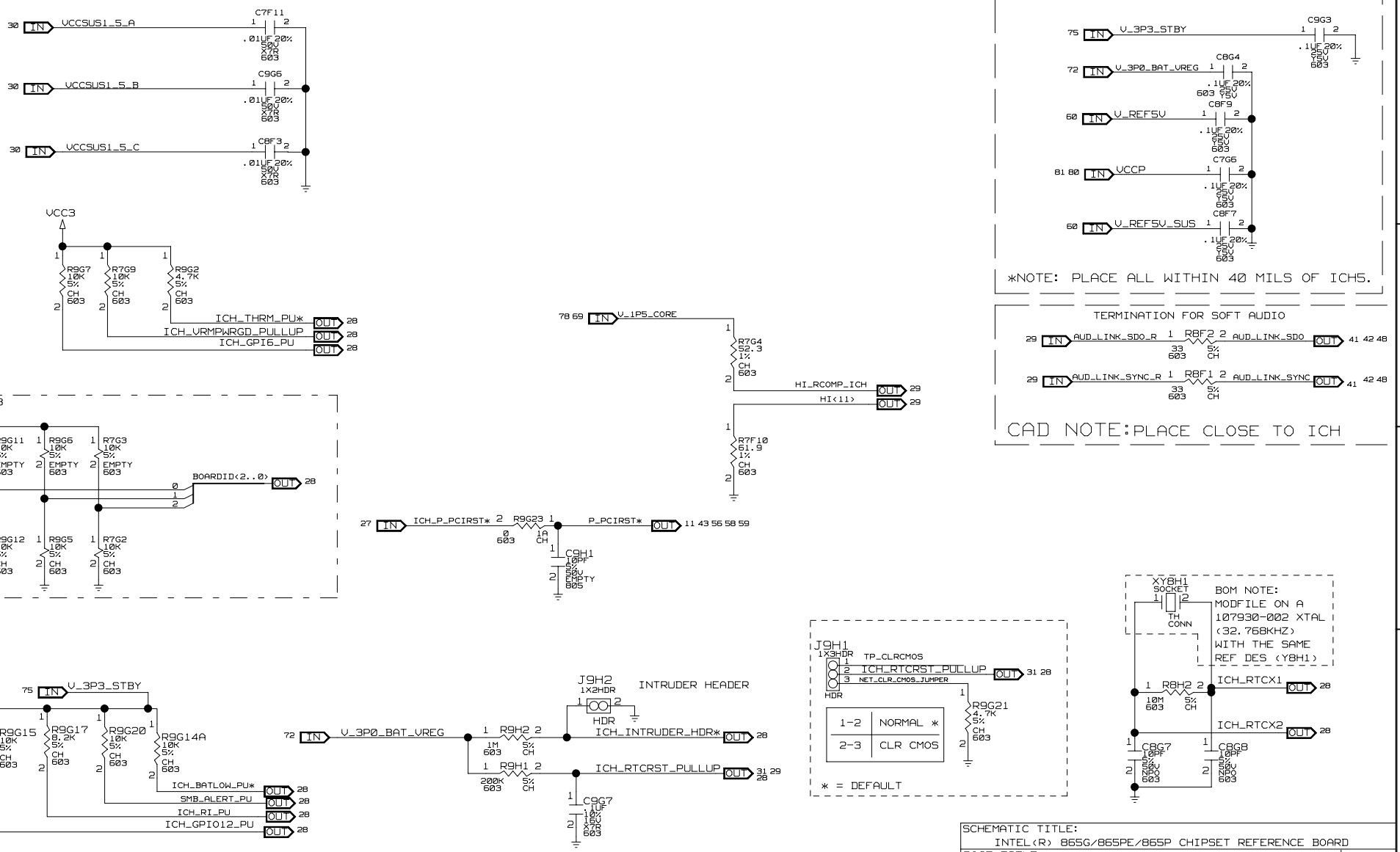
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: INTEL(R) ICH5 3 OF 4		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:20 2003	SHEET: 29



GND: A10, A21, A23, AA11, AA13, AA21, AA24, AA5, AA7, AA9, AB11, AB15, AB18, AB5, AB7, AB9, AC10, AC13, AC2, AC23, AC4, AC6, AC8, AD12, B13, B17, B19, B21 B23, C16, C18, C20, C22, C3, C8, D11, D16, D18, D20, D22, D6, E17, E19, E20, E21, E23, F3, F9, G20, G6, H19, H22, J21, J23, J6, K11, K14, K20, K22, K3, L10, L11, L12, L13, L14, L15, L21 L23, M1, M11, M12, M13, M14, M22, M5, N11, N12, N13, N14, N20, P10, P11, P12, P13, P14, P15, P21, R11, R14, T23, T3, T6, U19, V1, V21, W16, W18, Y10, Y3, Y6, Y7, Y8

DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: INTEL(R) ICH5 4 OF 4		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:20 2003	SHEET: 30

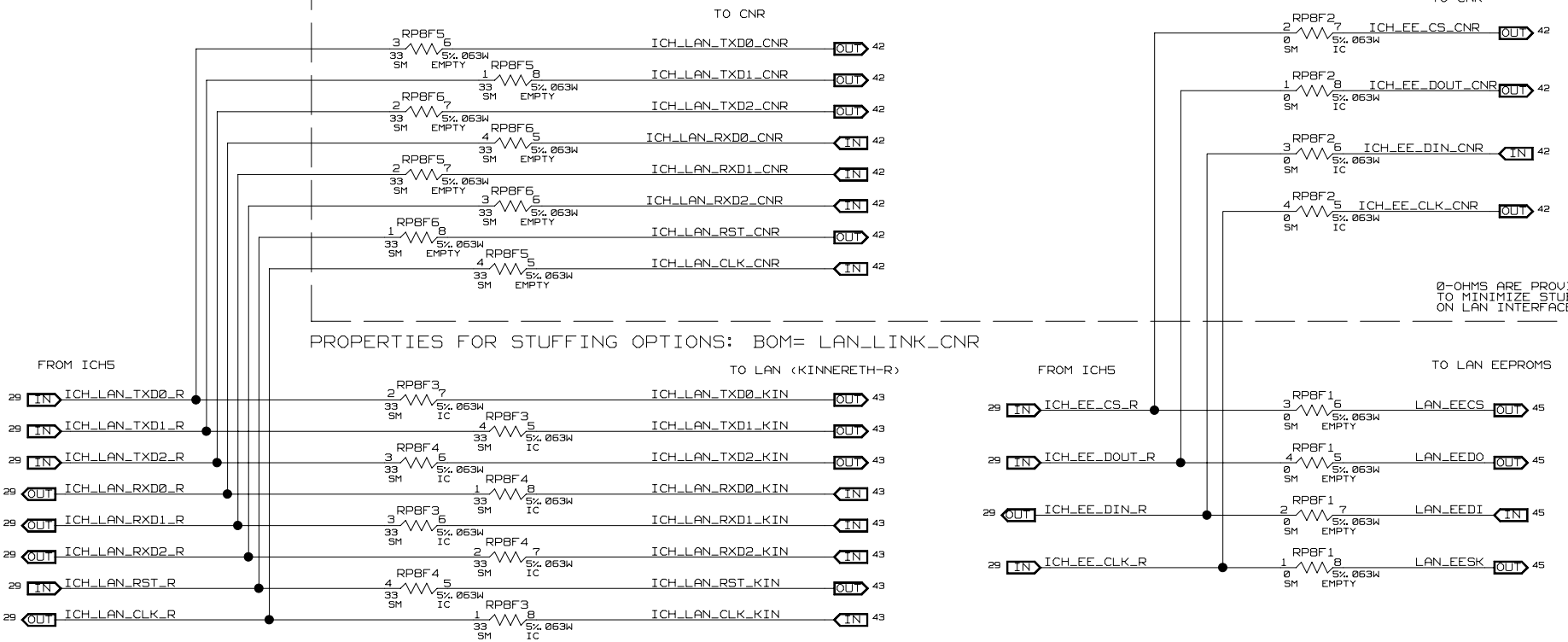


DRAWING

SCHEMATIC TITLE:	INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:	INTEL(R) ICH5 PULLUPS & DECOUPLING
REV:	
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED:	Tue May 06 11:25:21 2003
SHEET:	31

CR-32

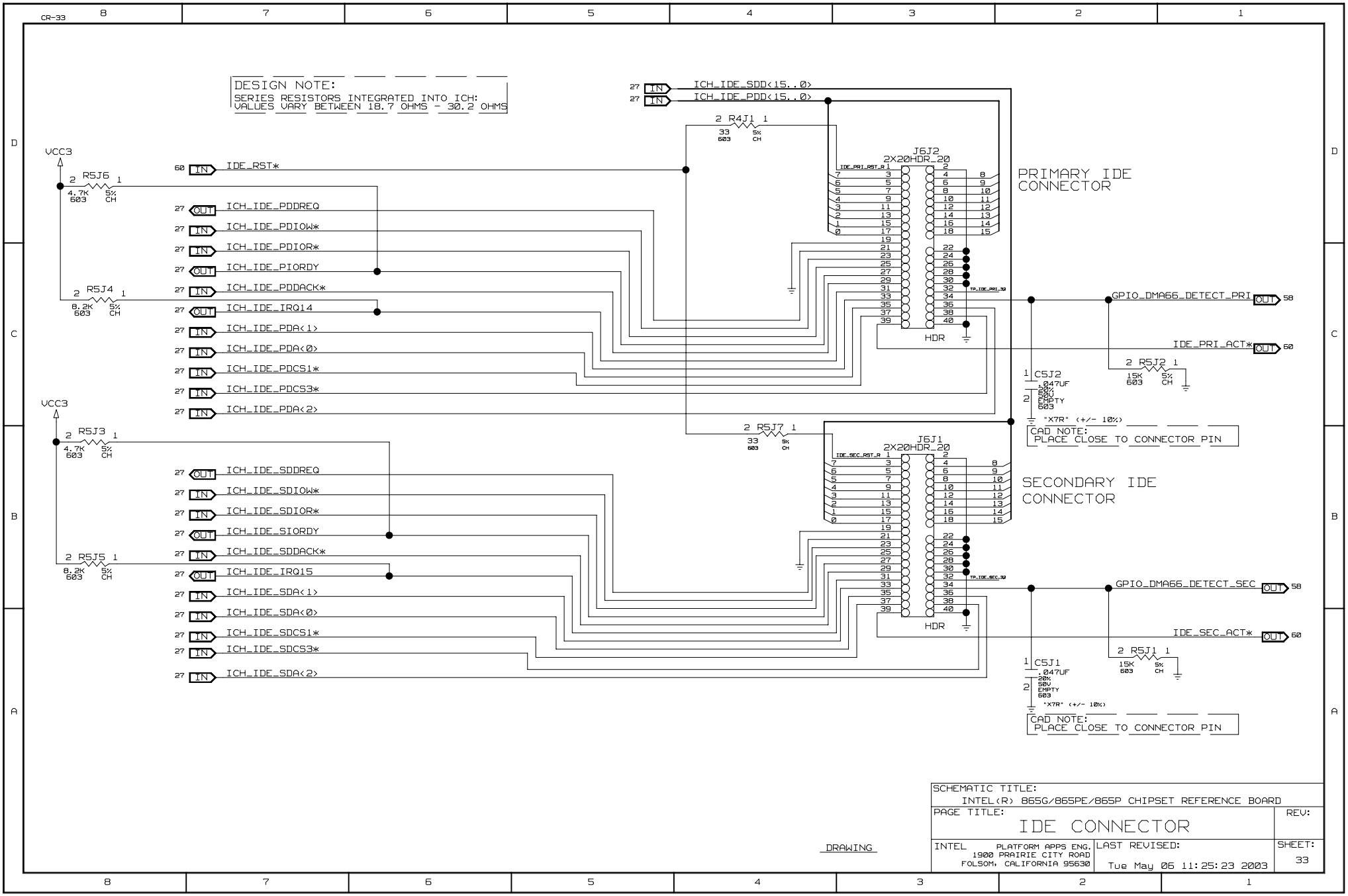
PROPERTIES FOR STUFFING OPTIONS: BOM= CNR_LINK_LAN
CNR STUFFING OPTION FOR LAN-UP SOLUTION

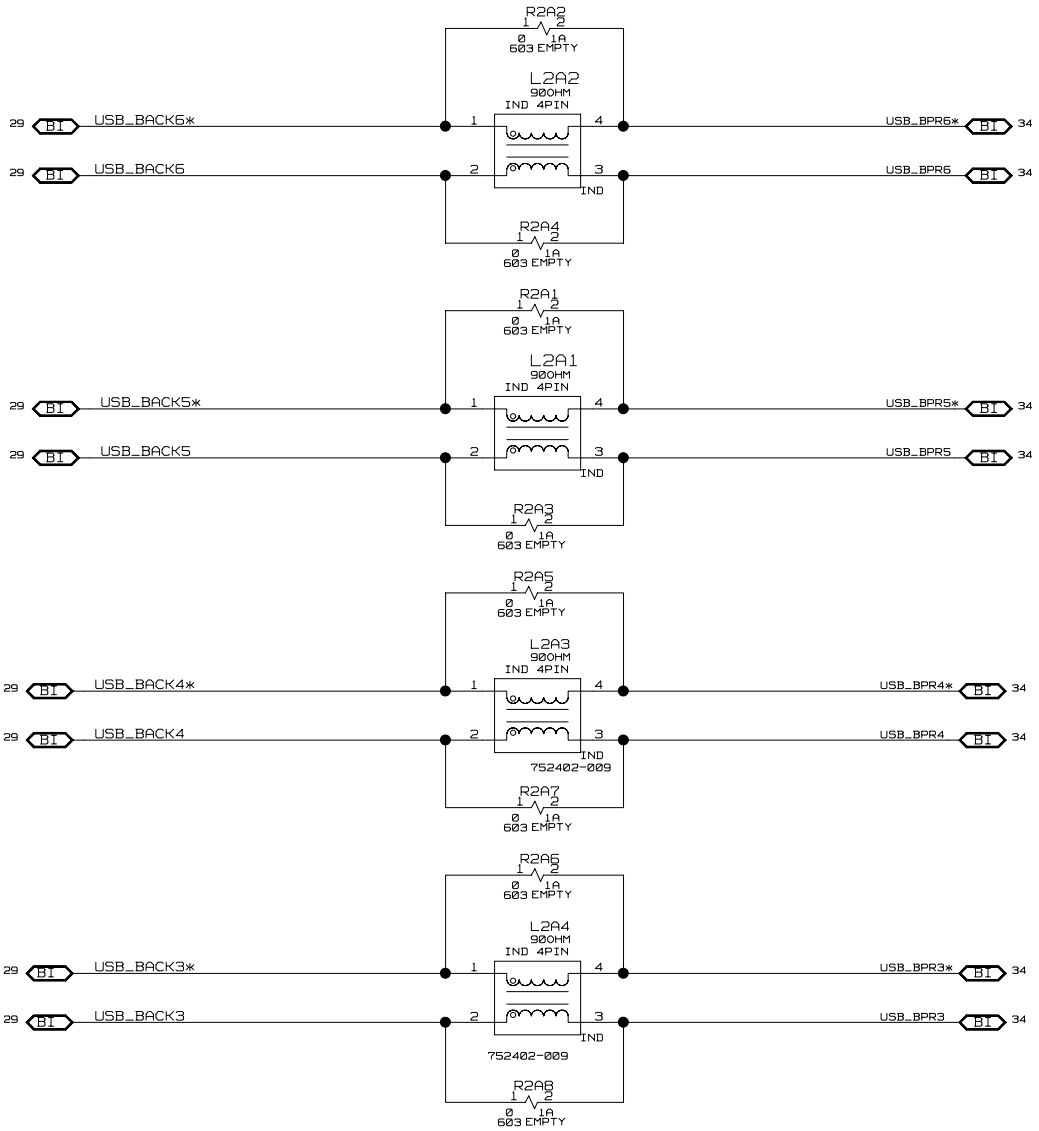


PROPERTIES FOR STUFFING OPTIONS: BOM= LAN_LINK_CNR

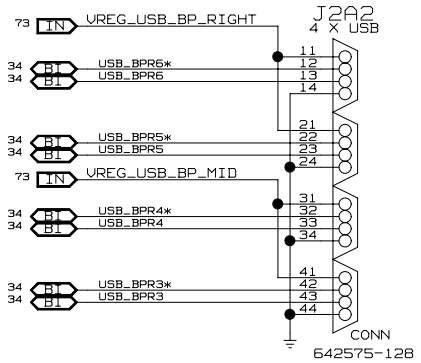
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: LAN STUFFING OPTION		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:22 2003	SHEET: 32


CR-33
DESIGN NOTE:
SERIES RESISTORS INTEGRATED INTO ICH:
VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS
ICH_IDE_SDD<15..0>
ICH_IDE_PDD<15..0>
R4J1
R5J6
R5J4
R5J3
R5J5
R5J7
R5J2
R5J1
C5J2
C5J1
J6J2
J6J1
2X20HDR_20
HDR
PRIMARY IDE CONNECTOR
SECONDARY IDE CONNECTOR
IDE_RST*
ICH_IDE_PDDREQ
ICH_IDE_PDIOW*
ICH_IDE_PDIOR*
ICH_IDE_PIORDY
ICH_IDE_PDDACK*
ICH_IDE_IRQ14
ICH_IDE_PDA<1>
ICH_IDE_PDA<0>
ICH_IDE_PDCS1*
ICH_IDE_PDCS3*
ICH_IDE_PDA<2>
ICH_IDE_SDDREQ
ICH_IDE_SDIOW*
ICH_IDE_SDIOR*
ICH_IDE_SIORDY
ICH_IDE_SDDACK*
ICH_IDE_IRQ15
ICH_IDE_SDA<1>
ICH_IDE_SDA<0>
ICH_IDE_SDCS1*
ICH_IDE_SDCS3*
ICH_IDE_SDA<2>
GPIO_DMA66_DETECT_PRI
IDE_PRI_ACT*
GPIO_DMA66_DETECT_SEC
IDE_SEC_ACT*
"X7R" (+/- 10%)
CAD NOTE:
PLACE CLOSE TO CONNECTOR PIN
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
IDE CONNECTOR
REV:
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue May 06 11:25:23 2003
SHEET:
33
DRAWING



QUAD STACK USB



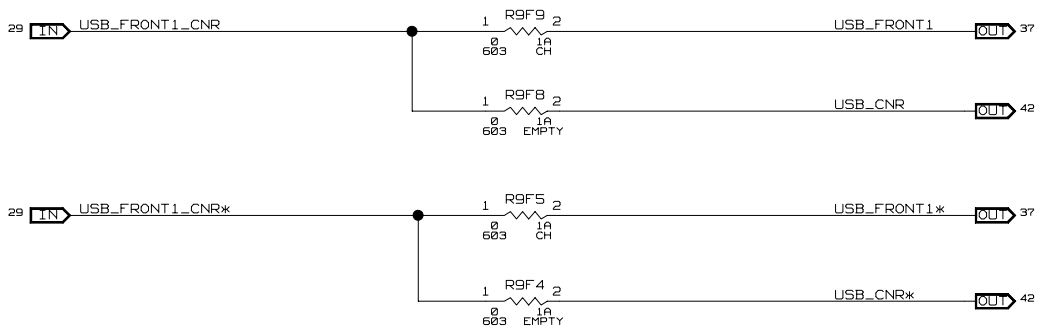
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: BACKPANEL_USB_RIGHT AND MID		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:24 2003	SHEET: 34

CR-35

USB SWITCH

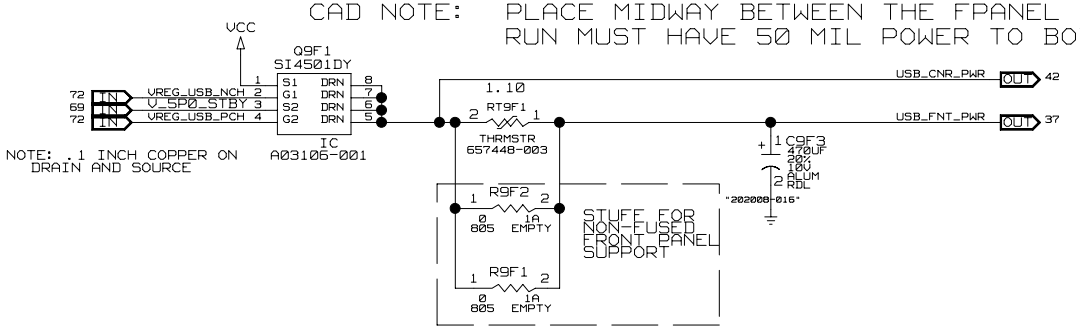
USB OPTION FOR FRONT PANEL OR CNR



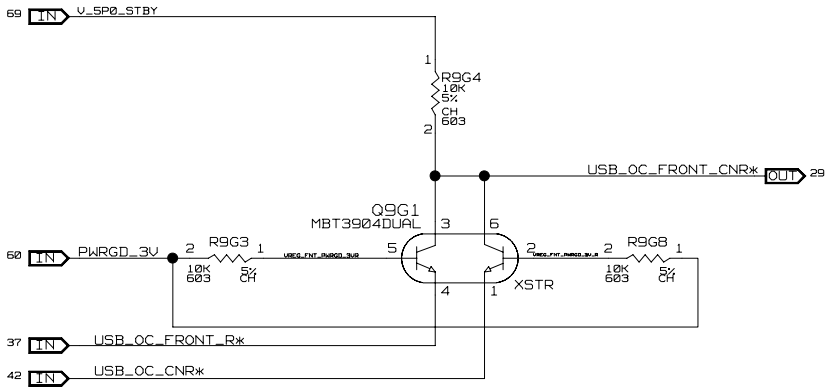
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: USB ROUTING OPTION		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:25 2003	SHEET: 35

CAD NOTE: PLACE MIDWAY BETWEEN THE FPANEL (2X5) & INTERNAL HEADERS RUN MUST HAVE 50 MIL POWER TO BOTH LOCATIONS.

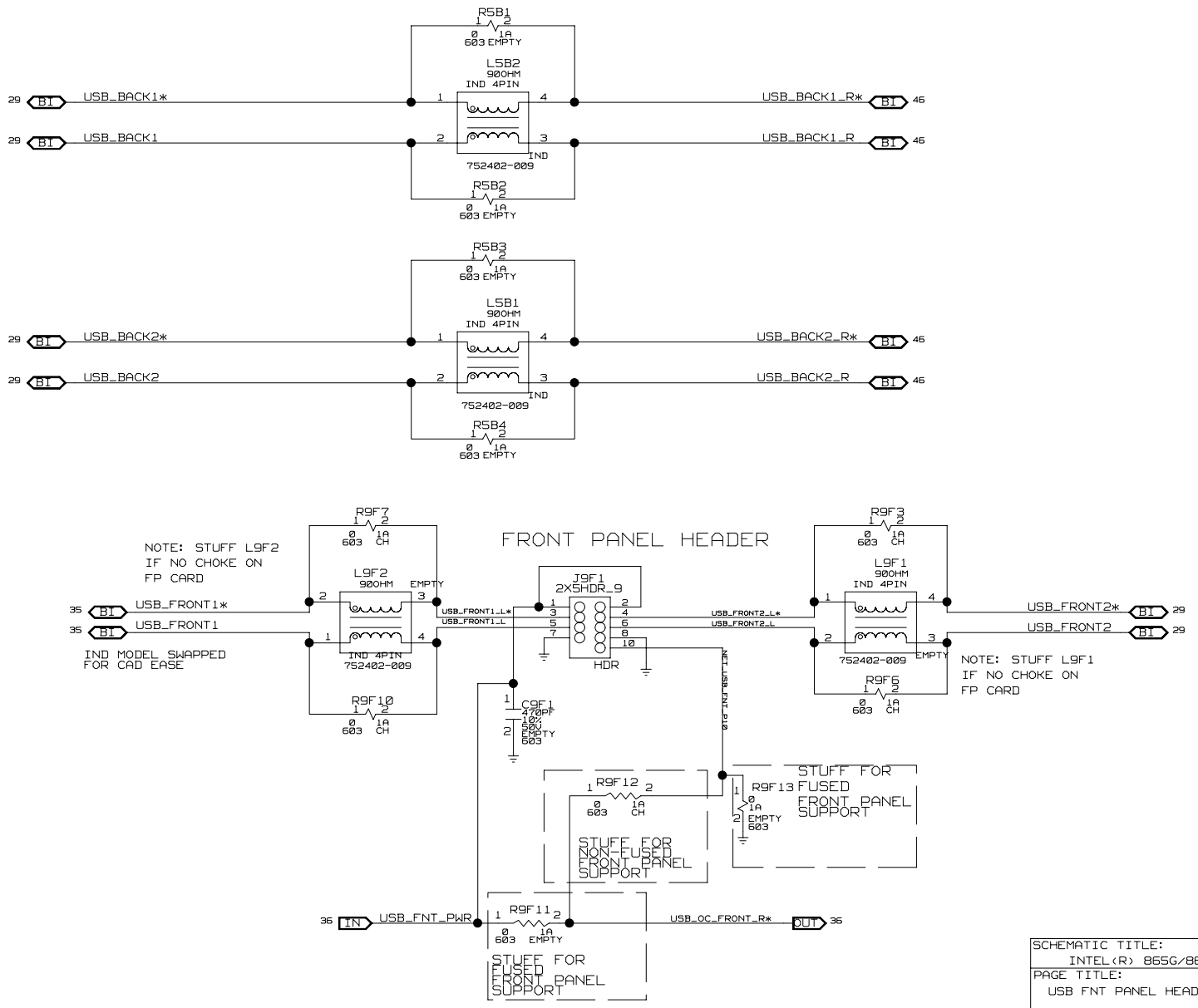


NOTE:
RPD ASSUMES FPANEL CARD HAS THERM & PROVIDES OC#



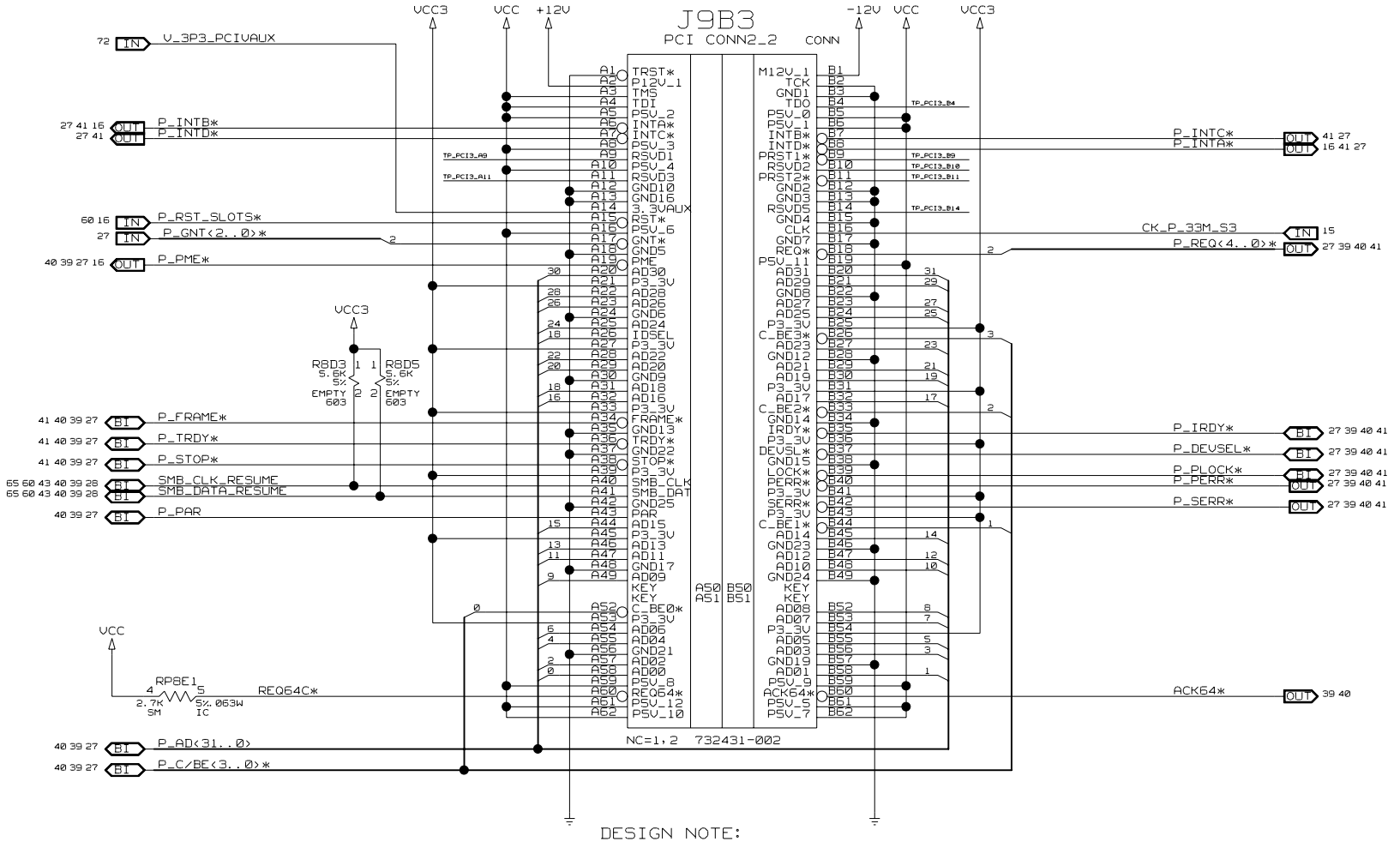
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: USB FNT PANEL POWER		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:25 2003	SHEET: 36



SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD			
PAGE TITLE: USB FNT PANEL HEADER & BACK PANEL RIGHT CONN			REV:
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:26 2003	SHEET: 37

PCI SLOT 3



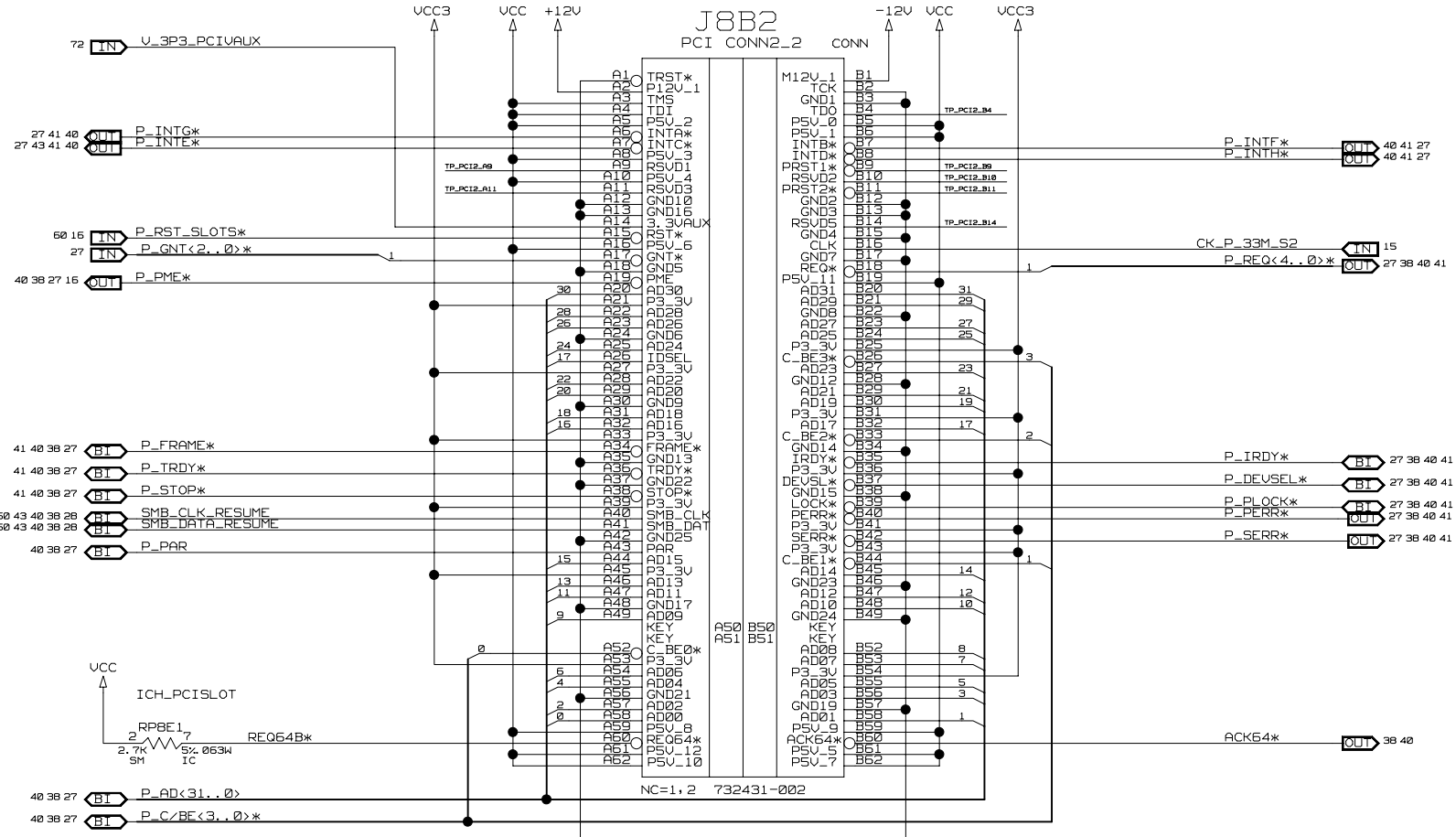
DESIGN NOTE:

PCI SLOT3 = PCI DEVICE FUNCTION 10H
= PCI DEVICE NUMBER 2H
= IDSEL VALUE AD18

DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE: PCI SLOT 3	REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:27 2003
	SHEET: 38

PCI SLOT 2



DESIGN NOTE:

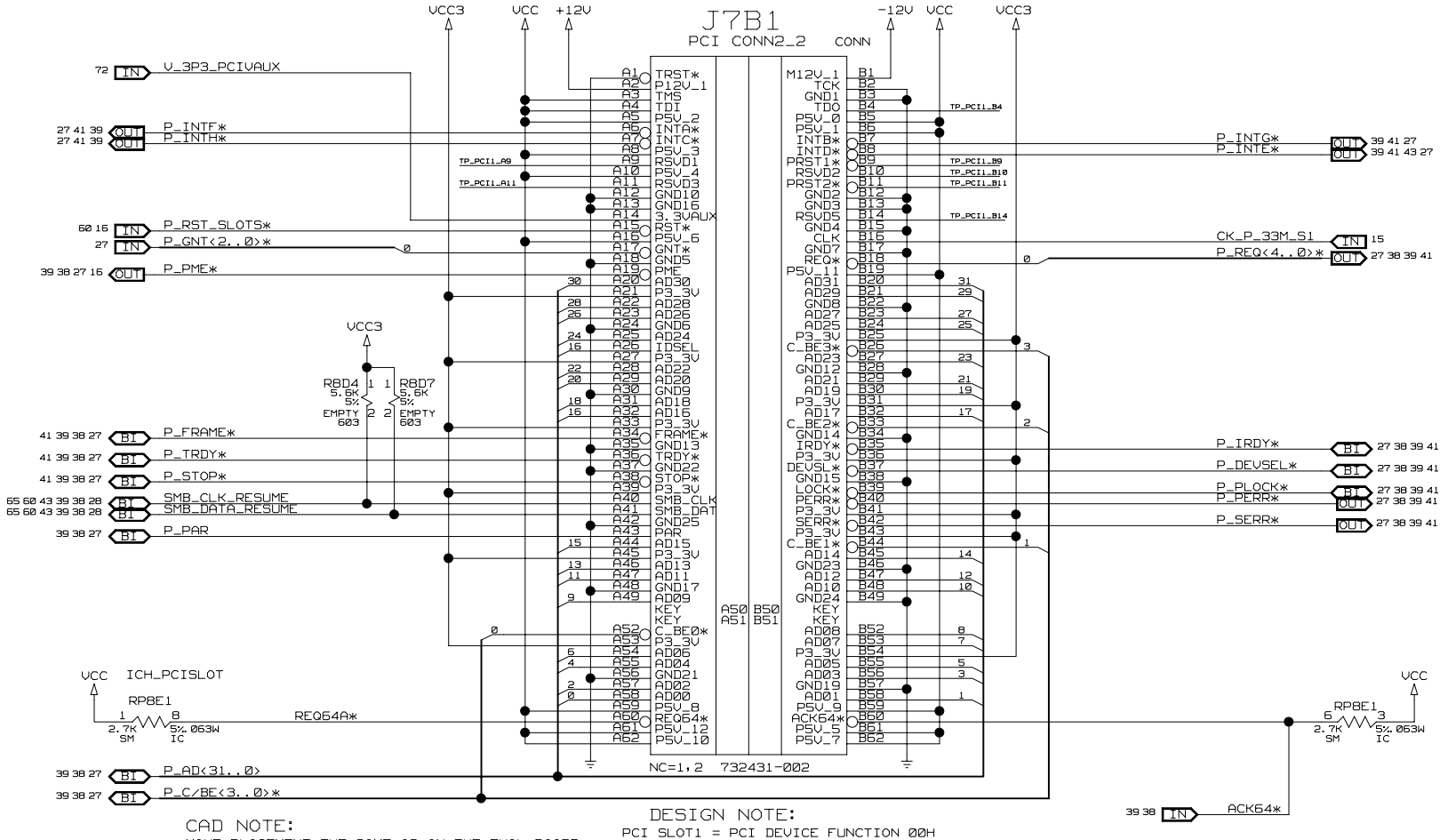
PCI SLOT2 = PCI DEVICE FUNCTION 08H
= PCI DEVICE NUMBER 1H
= IDSEL VALUE AD17

DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE: PCI SLOT 2	REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:28 2003
	SHEET: 39

PCI SLOT 1

CLOSEST PCI SLOT TO CPU



DESIGN NOTE:

PCI SLOT1 = PCI DEVICE FUNCTION 00H
= PCI DEVICE NUMBER 0H
= IDSEL VALUE AD16

CAD NOTE:

MAKE PLACEMENT THE SAME AS ON THE EVAL BOARD
FOR TEST-POINTED, EMPTY RESISTOR SITES

PCI SLOT 1

DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE: PCI SLOT 1	REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:28 2003
	SHEET: 40

SPARE SECTIONS

TP_RP6F2_4 — RP8C2 4 5 — 2.7K SM, 5% .063W IC — TP_RP6F2_5

TP_RP6D2_4 — RP8D3 4 5 — 2.7K SM, 5% .063W IC — TP_RP6D2_5

PCI PULL-UPS

VCC

40 39 38 27	P_SERR#	RP8D1 3 6	2.7K SM, 5% .063W IC
40 39 38 27	P_DEVSEL#	R9G1 1 2	2.7K 603, 5% CH
40 39 38 27	P_IRDY#	RP8D1 2 7	2.7K SM, 5% .063W IC
40 39 38 27	P_PLOCK#	RP8D3 2 7	2.7K SM, 5% .063W IC
40 39 38 27	P_PERR#	RP8D1 4 5	2.7K SM, 5% .063W IC
40 39 38 27	P_FRAME#	RP8D1 1 8	2.7K SM, 5% .063W IC
40 39 38 27	P_TRDY#	RP8D3 3 6	2.7K SM, 5% .063W IC
40 39 38 27	P_STOP#	RP8D3 1 8	2.7K SM, 5% .063W IC
40 39 38 27	P_REQ<4..0>#	RP8E2 4 2 7	2.7K SM, 5% .063W IC
		RP8E2 3 3 6	2.7K SM, 5% .063W IC
		RP8C2 2 2 7	2.7K SM, 5% .063W IC
		RP8C2 1 3 6	2.7K SM, 5% .063W IC
		RP8C2 0 1 8	2.7K SM, 5% .063W IC
27	P_REQA#	RP8E2 1 8	2.7K SM, 5% .063W IC
27	P_REQ5#	RP8E2 4 5	2.7K SM, 5% .063W IC

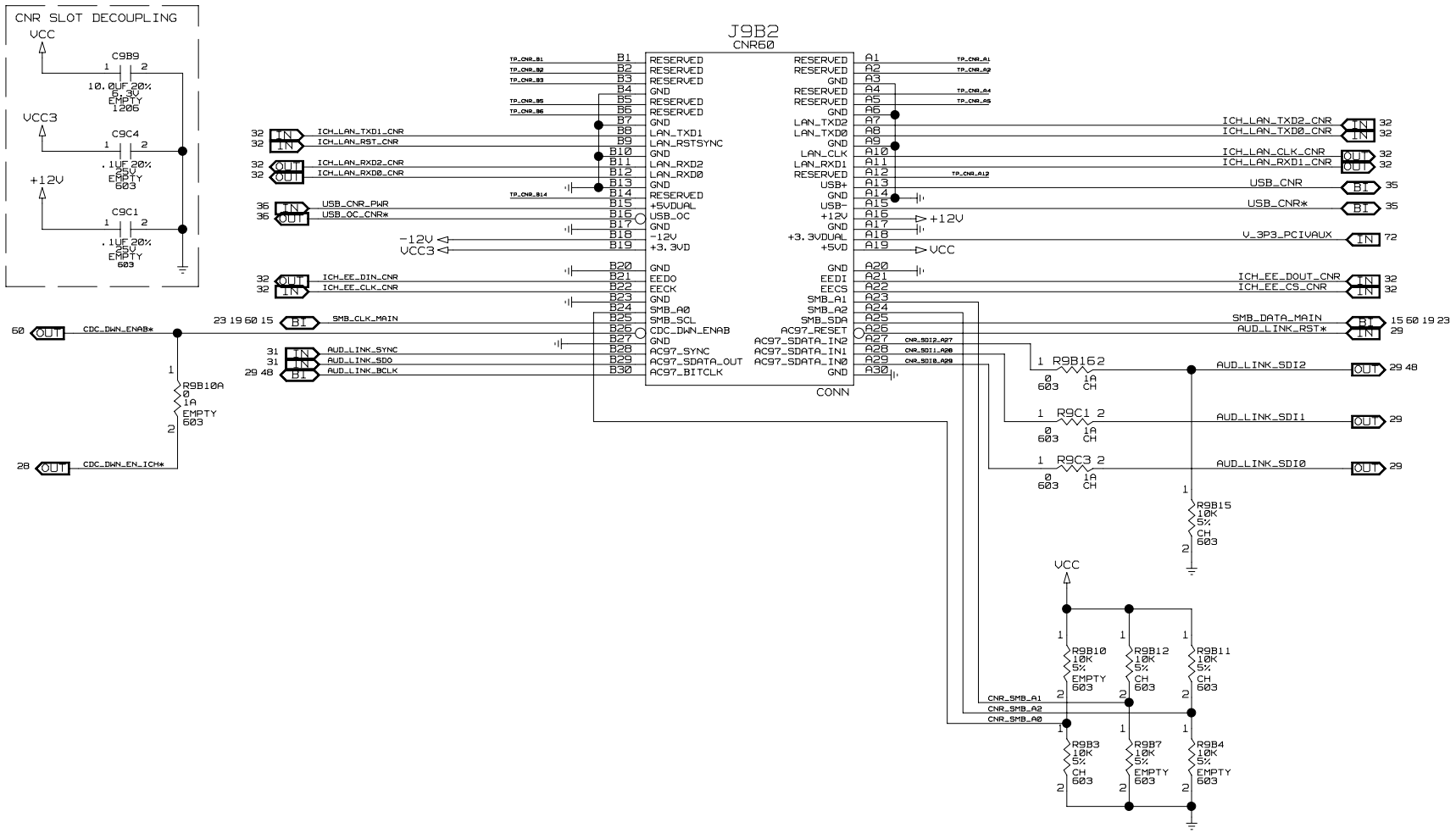
VCC3

27 38 16	P_INTA#	RP9B1 5 4	8.2K SM, 5% .063W IC
27 38 16	P_INTB#	RP9B1 6 3	8.2K SM, 5% .063W IC
27 38	P_INTC#	RP9B1 8 1	8.2K SM, 5% .063W IC
27 38	P_INTD#	RP9B1 7 2	8.2K SM, 5% .063W IC
27 43 40 39	P_INTE#	RP7B1 2 7	8.2K SM, 5% .063W IC
27 40 39	P_INTF#	RP7B1 1 8	8.2K SM, 5% .063W IC
27 40 39	P_INTG#	RP7B1 3 6	8.2K SM, 5% .063W IC
27 40 39	P_INTH#	RP7B1 4 5	8.2K SM, 5% .063W IC

DRAWING

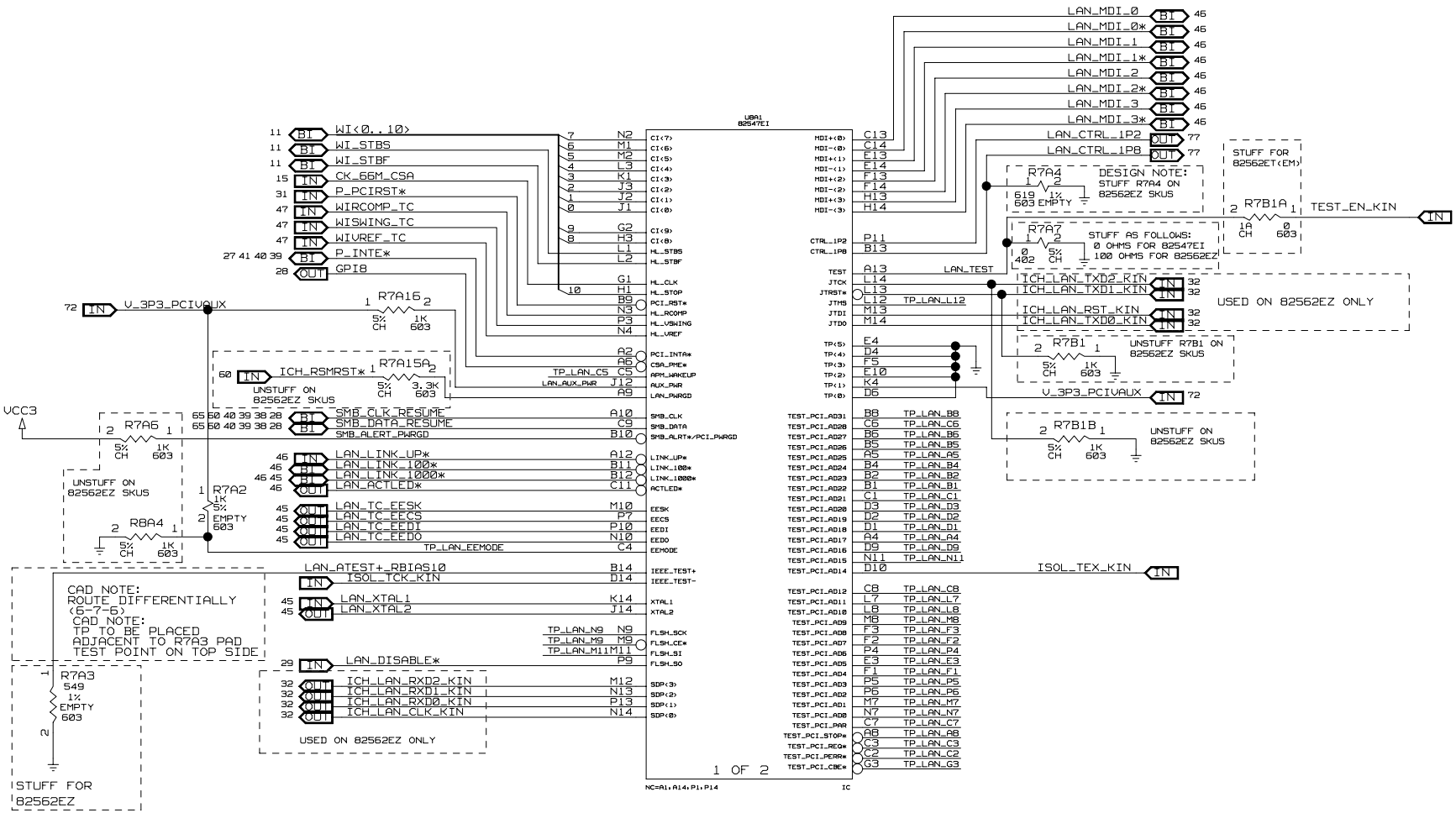
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: PCI TERMINATION		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:29 2003	SHEET: 41

SMB ADDRESS: 110
WRITE AC
READ AD



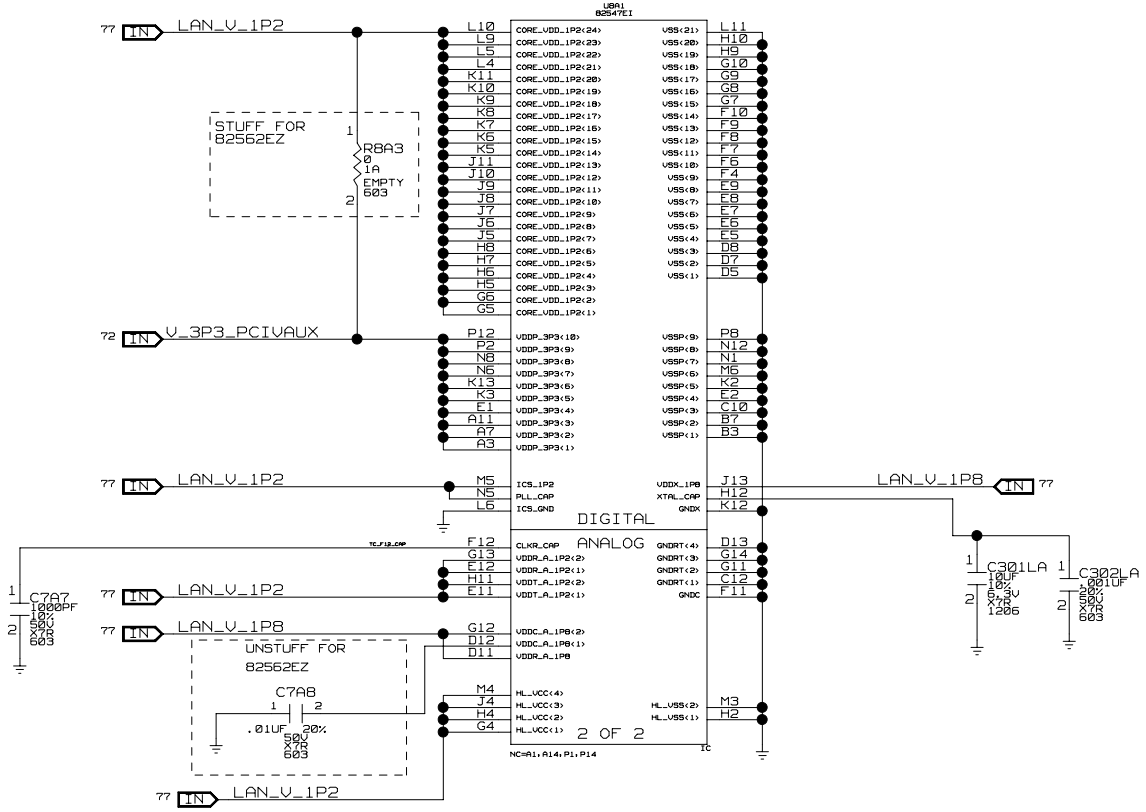
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: CNR		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:30 2003	SHEET: 42



SCHEMATIC TITLE:	INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:	82547EI/82562EZ(EX)(ET)(EM)
REV:	
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED:	Tue May 06 11:25:30 2003
SHEET:	43

DRAWING

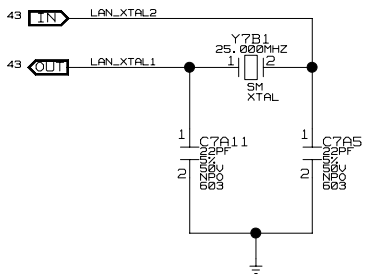


SCHEMATIC TITLE:	INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:	82547EI/82562EZ(EX)(ET)(EM) POWER CONNECTIONS
REV:	
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED:	Tue May 06 11:25:31 2003
SHEET:	44

DRAWING

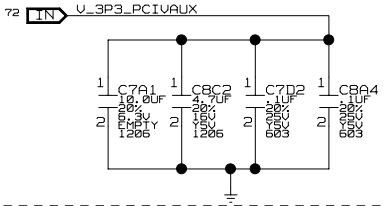
LAN CRYSTAL

CAD NOTE:
MINIMIZE XTAL TRACES
DO NOT PLACE OR ROUTE NEAR PLANE SPLIT



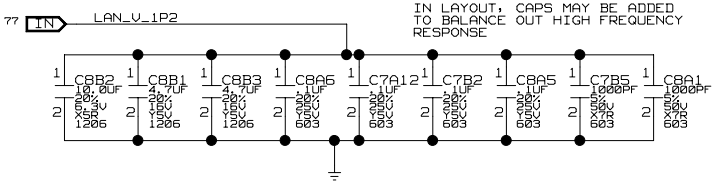
LAN DECOUPLING

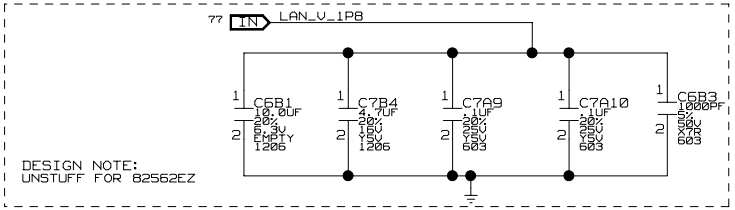
DESIGN NOTE:
DECOUPLING CAPS SHARE BETWEEN 82562EZ & 82547EI VOLTAGE NETS



DESIGN NOTE:

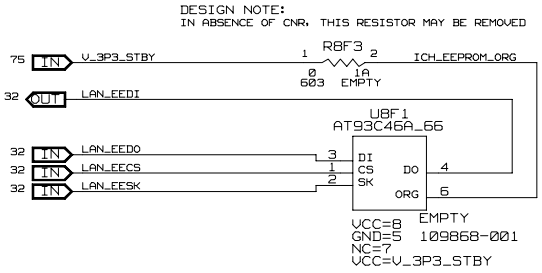
DEPENDING ON POWER DELIVERY IN LAYOUT, CAPS MAY BE ADDED TO BALANCE OUT HIGH FREQUENCY RESPONSE





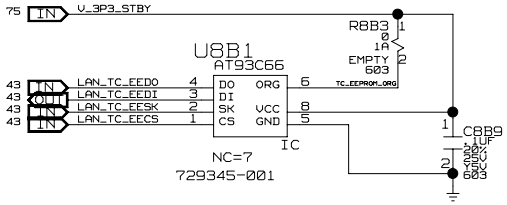
82562EZ EEPROM

STUFF THIS EEPROM ONLY WITH 82562EZ.
SKUS. PLACE NEAR ICH

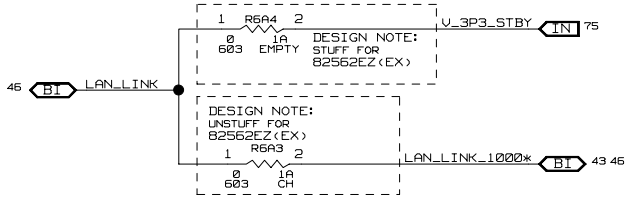


82547EI EEPROM

CAD NOTE:
PLACE EEPROM NEAR LAN CONTROLLER.



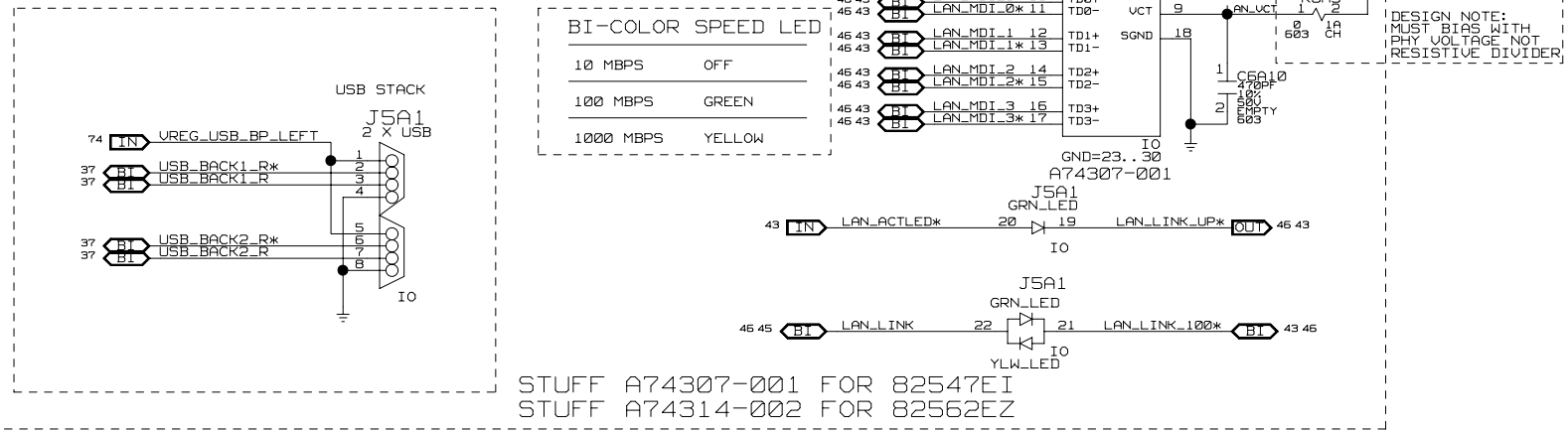
STUFFING OPTIONS FOR LED ENABLING



DRAWING

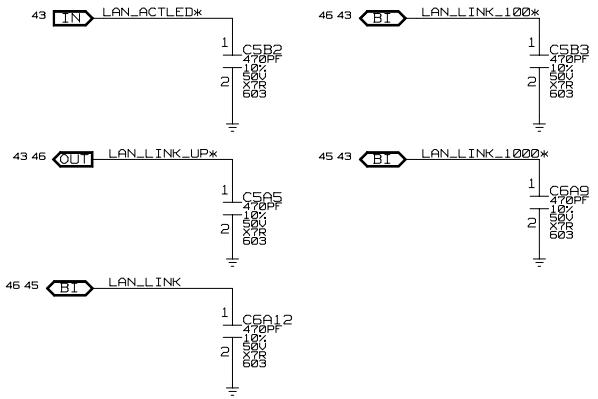
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE: LAN EEPROMS/DECOUPLING/LED	REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:32 2003
	SHEET: 45

LAN CONNECTOR



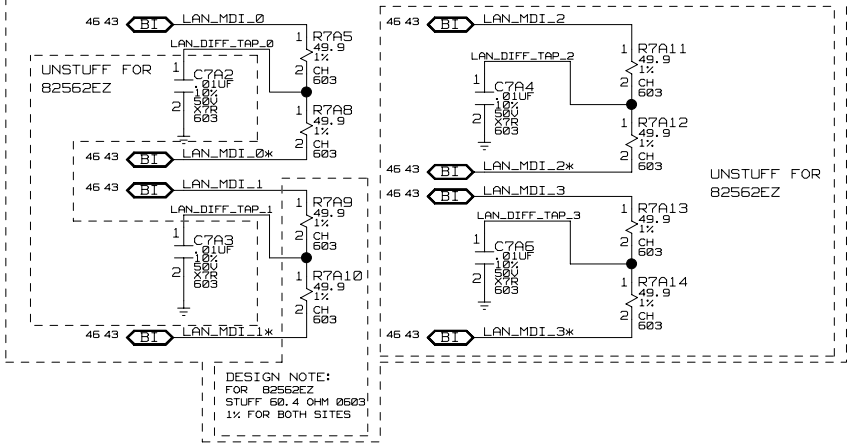
LED DECOUPLING

CAD NOTE:
LED CAPS SHOULD BE PLACED NEXT TO CONNECTOR



DIFFERENTIAL PAIR TERMINATONS

CAD NOTE:
PLACE NEXT TO CONTROLLER

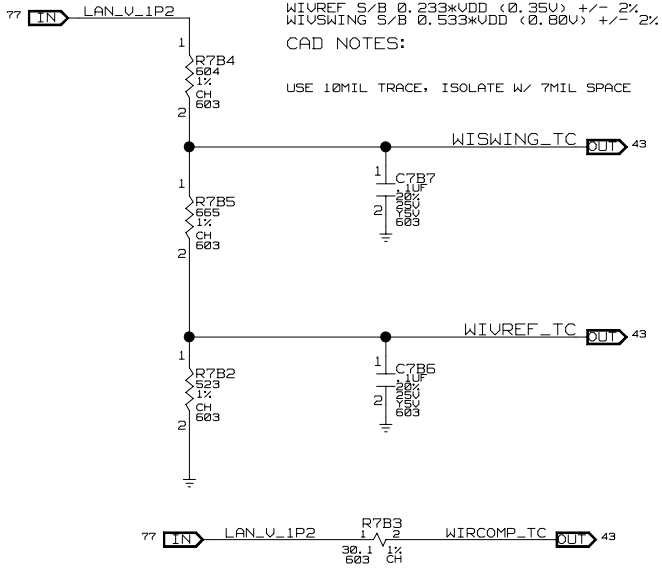


DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: LAN CONNECTOR/DECOUPLING		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:32 2003	SHEET: 46

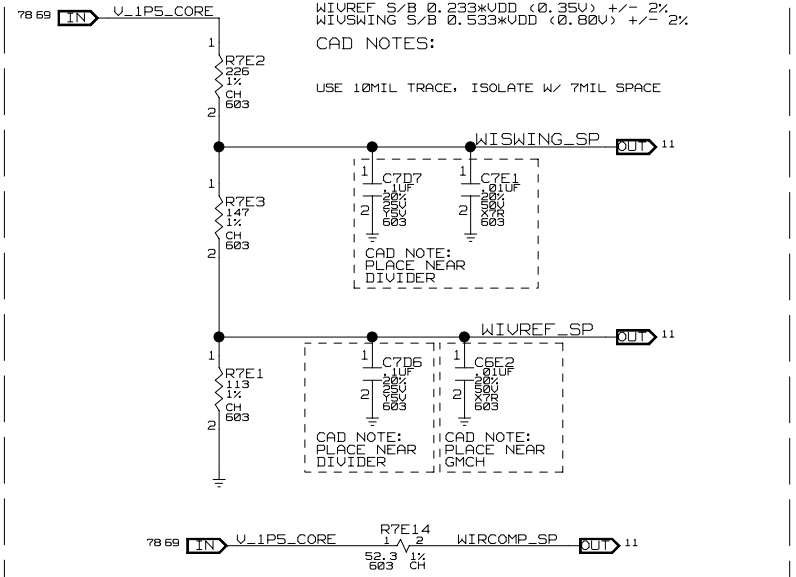
LAN
CSA INTERFACE REFERENCE

DESIGN NOTES:
WIVREF S/B 0.233*VDD (0.35V) +/- 2%
WIVSWING S/B 0.533*VDD (0.80V) +/- 2%
CAD NOTES:
USE 10MIL TRACE, ISOLATE W/ 7MIL SPACE



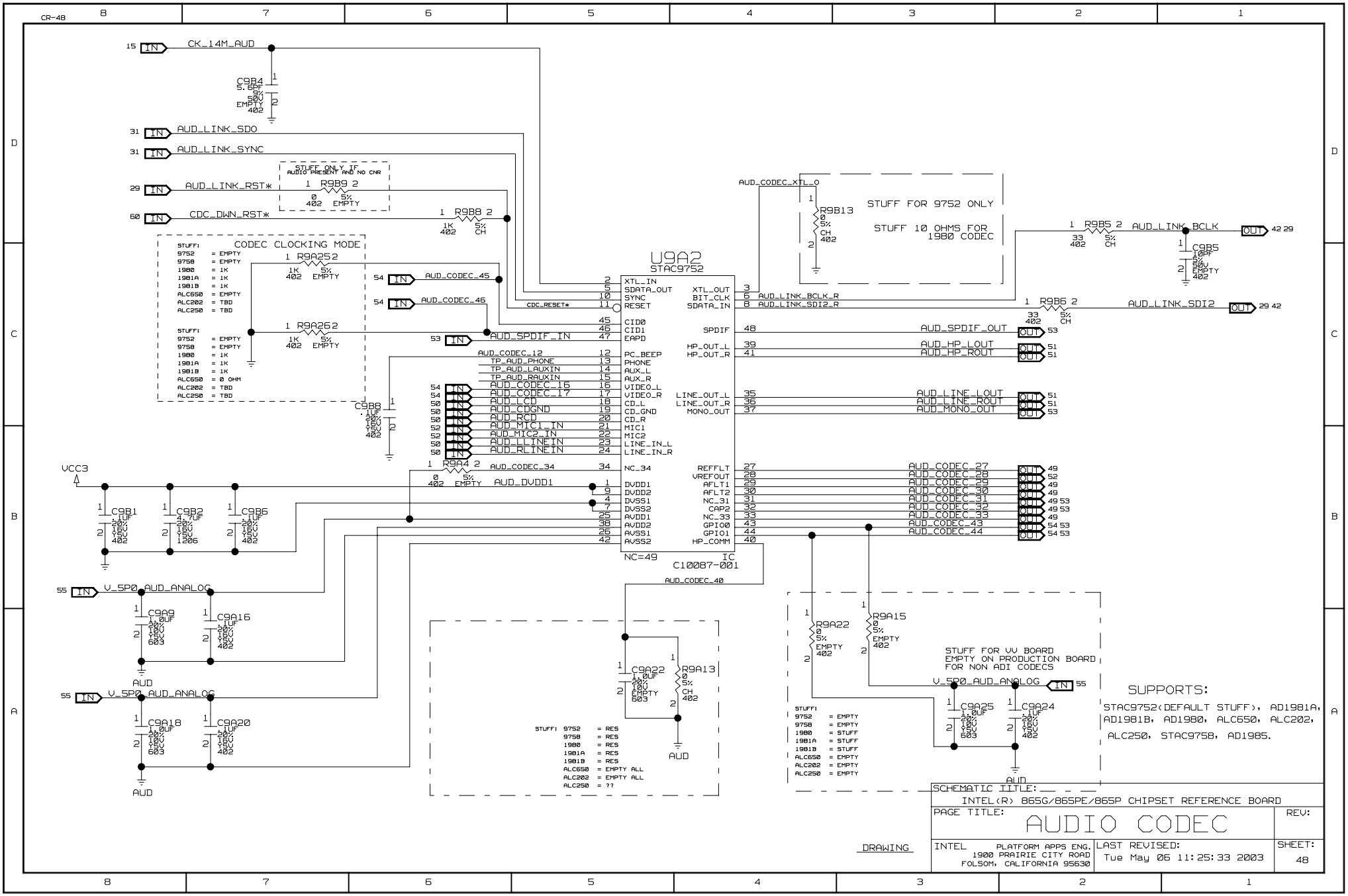
GMCH
CSA INTERFACE REFERENCE

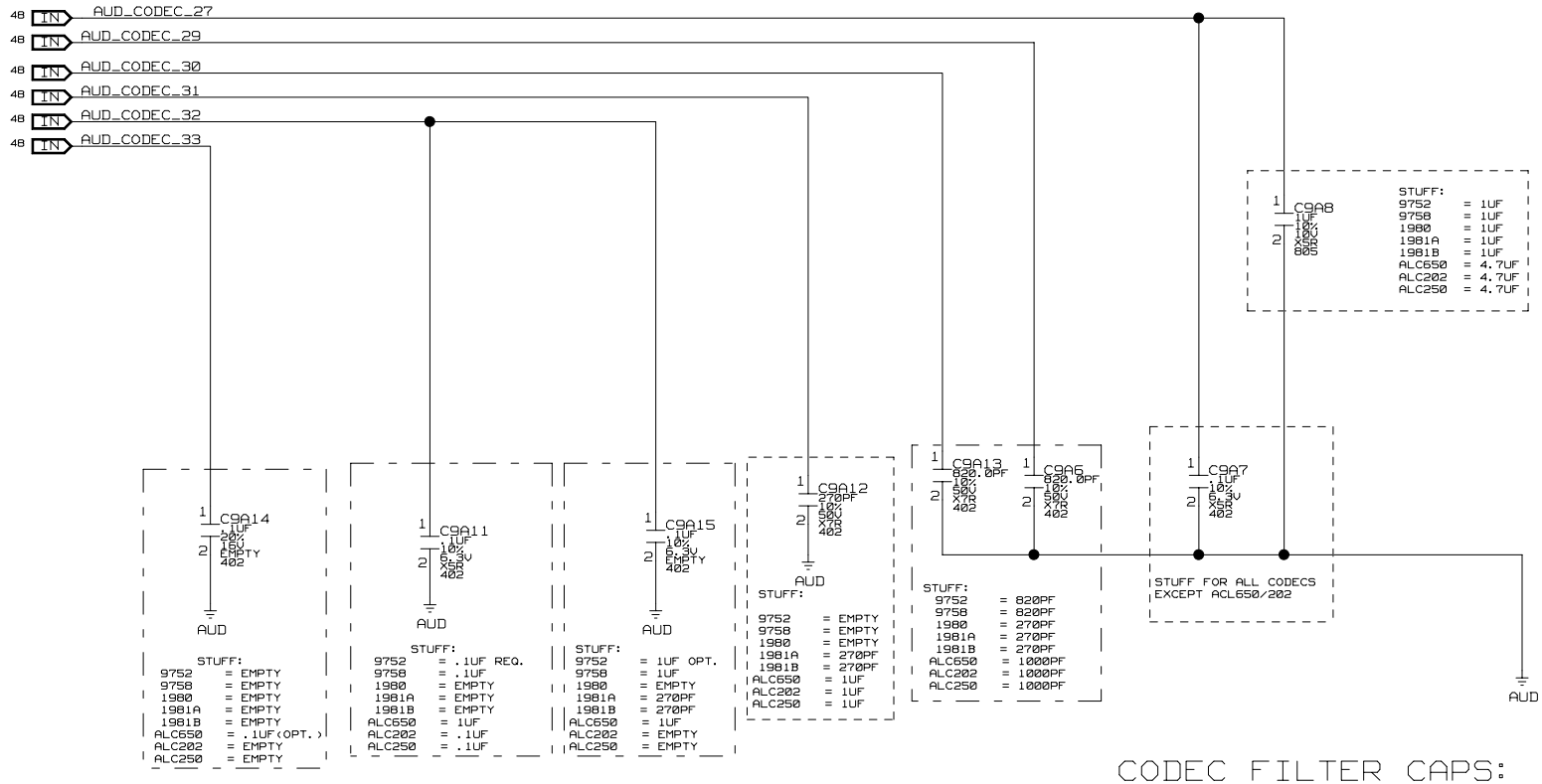
DESIGN NOTES:
WIVREF S/B 0.233*VDD (0.35V) +/- 2%
WIVSWING S/B 0.533*VDD (0.80V) +/- 2%
CAD NOTES:
USE 10MIL TRACE, ISOLATE W/ 7MIL SPACE



DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: CSA INTERFACE REFERENCE		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:33 2003	SHEET: 47


CR-4B
CK_14M_AUD
AUD_LINK_SDO
AUD_LINK_SYNC
AUD_LINK_RST*
CDC_DWN_RST*
STUFF ONLY IF AUDIO PRESENT AND NO CNR
CODEC CLOCKING MODE
AUD_CODEC_45
AUD_CODEC_46
AUD_SPDIF_IN
U9A2
STAC9752
XTL_IN
SDATA_OUT
SYNC
RESET
CDC_RESET*
CID0
CID1
EAPD
PC_BEEP
PHONE
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_GND
CD_R
MIC1
MIC2
LINE_IN_L
LINE_IN_R
NC_34
DVDD1
DVDD2
DVSS1
DVSS2
AVDD1
AVDD2
AVSS1
AVSS2
XTL_OUT
BIT_CLK
SDATA_IN
SPDIF
HP_OUT_L
HP_OUT_R
LINE_OUT_L
LINE_OUT_R
MONO_OUT
REFFLT
VREFOUT
AFLT1
AFLT2
NC_31
CAP2
NC_33
GPIO0
GPIO1
HP_COMM
NC=49
IC
C10087-001
AUD_CODEC_40
AUD_CODEC_XTL_O
STUFF FOR 9752 ONLY
STUFF 10 OHMS FOR 1980 CODEC
AUD_LINK_BCLK
AUD_LINK_SDI2
AUD_SPDIF_OUT
AUD_HP_LOUT
AUD_HP_ROUT
AUD_LINE_LOUT
AUD_LINE_ROUT
AUD_MONO_OUT
AUD_CODEC_27
AUD_CODEC_28
AUD_CODEC_29
AUD_CODEC_30
AUD_CODEC_31
AUD_CODEC_32
AUD_CODEC_33
AUD_CODEC_43
AUD_CODEC_44
VCC3
AUD_DVDD1
V_5P0_AUDIO_ANALOG
STUFF FOR VV BOARD
EMPTY ON PRODUCTION BOARD
FOR NON ADI CODECS
V_5P0_AUD_ANALOG
SUPPORTS:
STAC9752(DEFAULT STUFF), AD1981A, AD1981B, AD1980, ALC650, ALC202, ALC250, STAC9758, AD1985.
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
AUDIO CODEC
REV:
DRAWING
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue May 06 11:25:33 2003
SHEET:
48

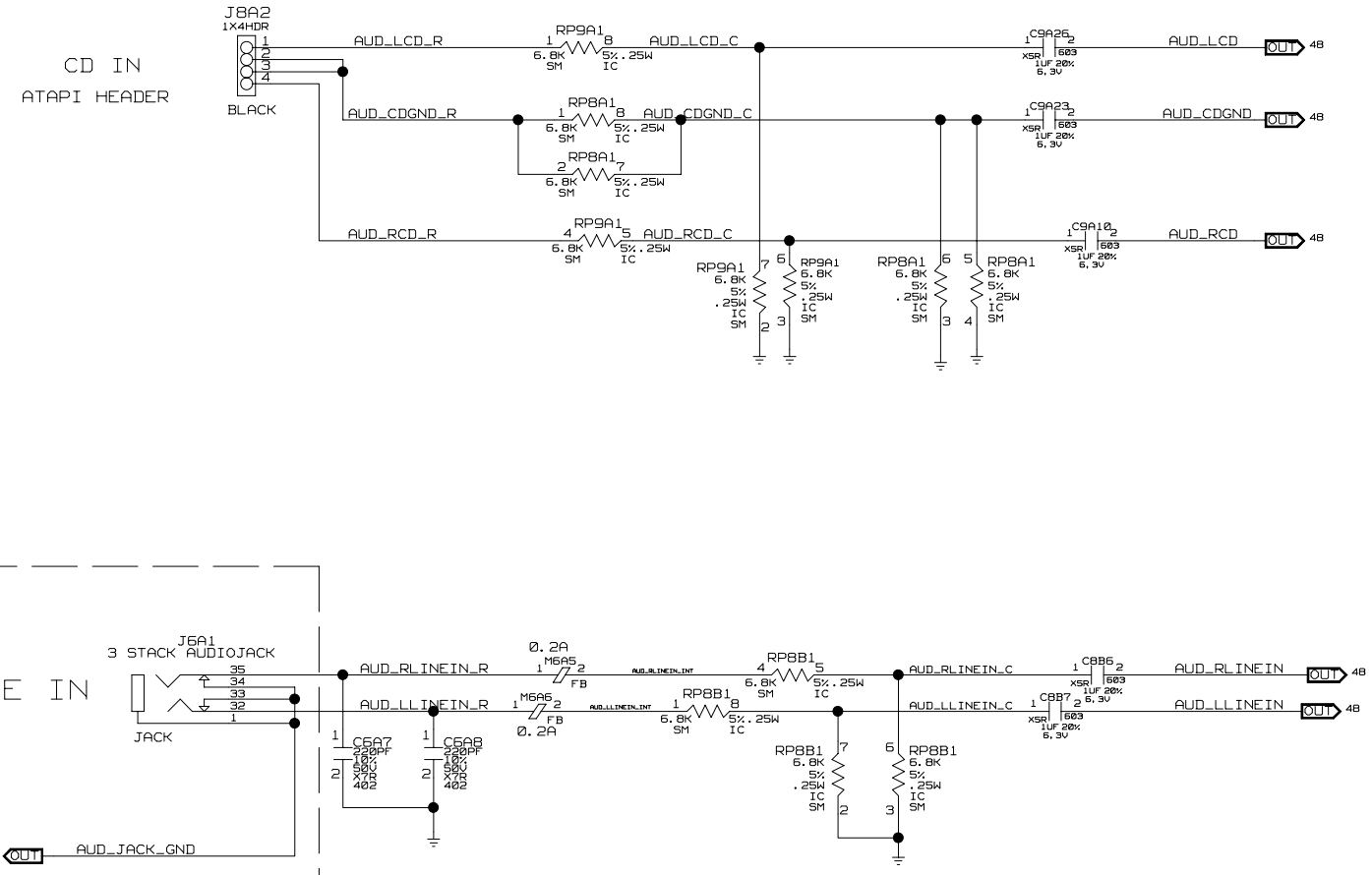


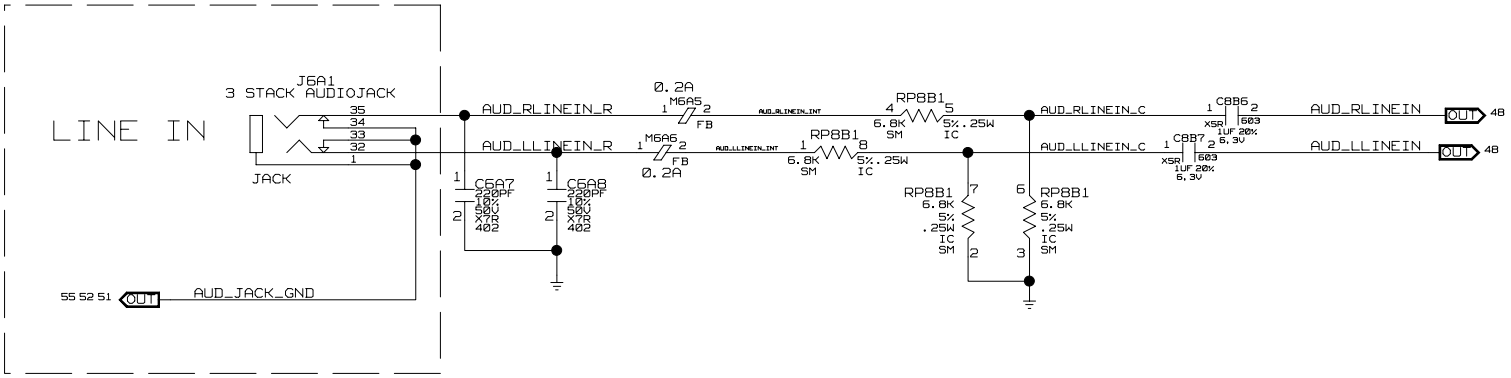
CODEC FILTER CAPS:
9752, 9758, 1980, 1981A, 1981B,
ALC650, ALC202, ALC250

KEEP CAPS AS CLOSE
AS POSSIBLE TO AC97
CODEC

DRAWING

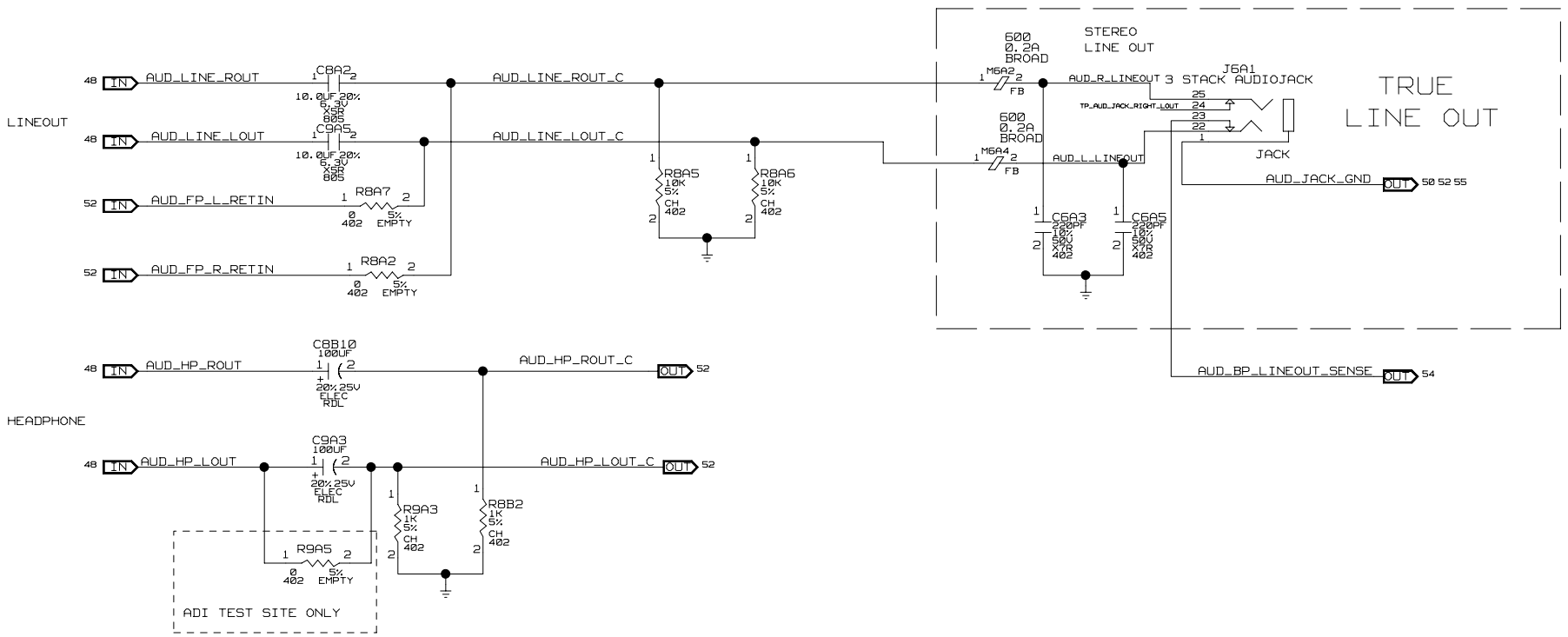
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE: CODEC FILTERING CAPS	REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:34 2003
	SHEET: 49





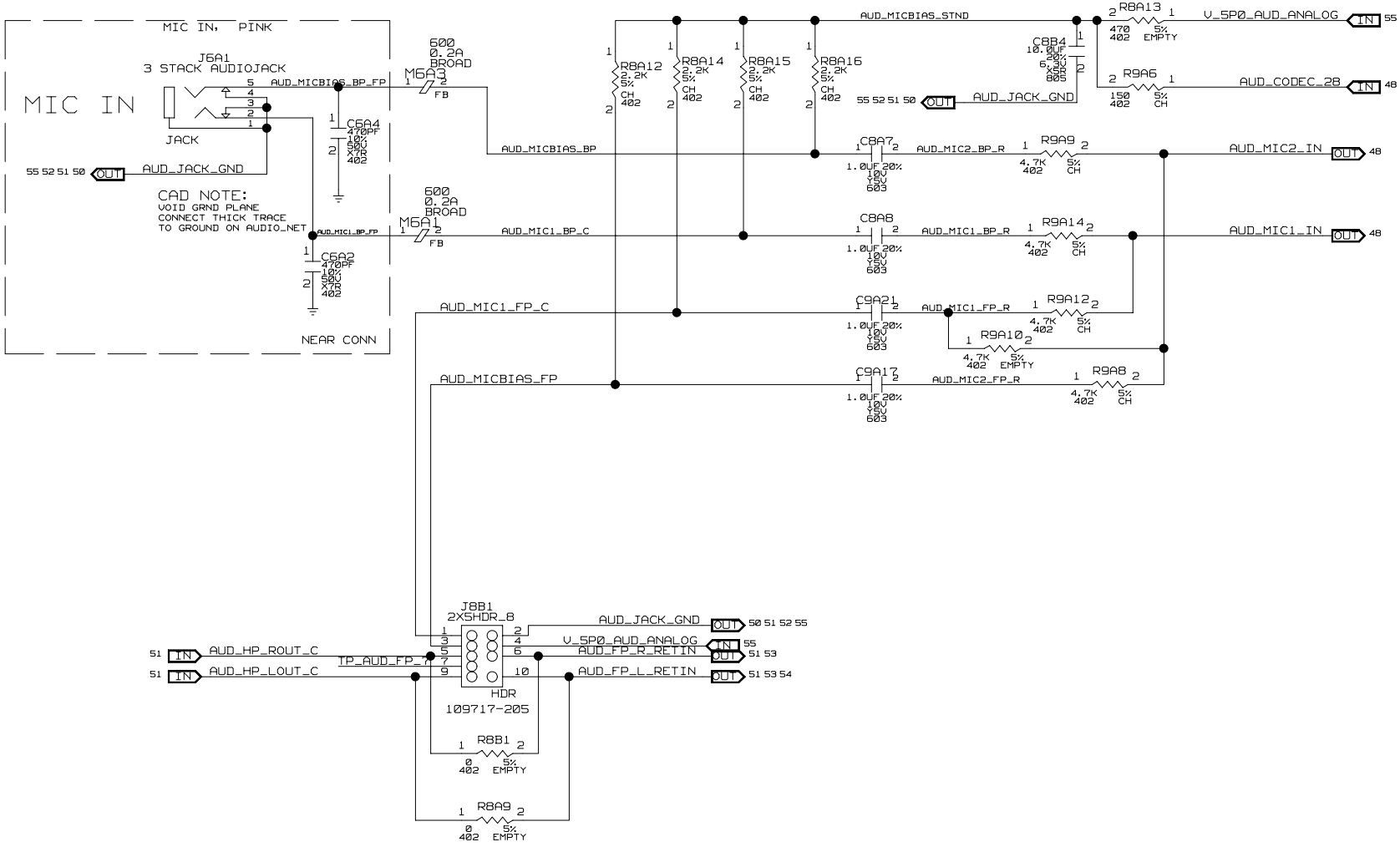
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: LINE IN & ATAPI HEADER		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:35 2003	SHEET: 50



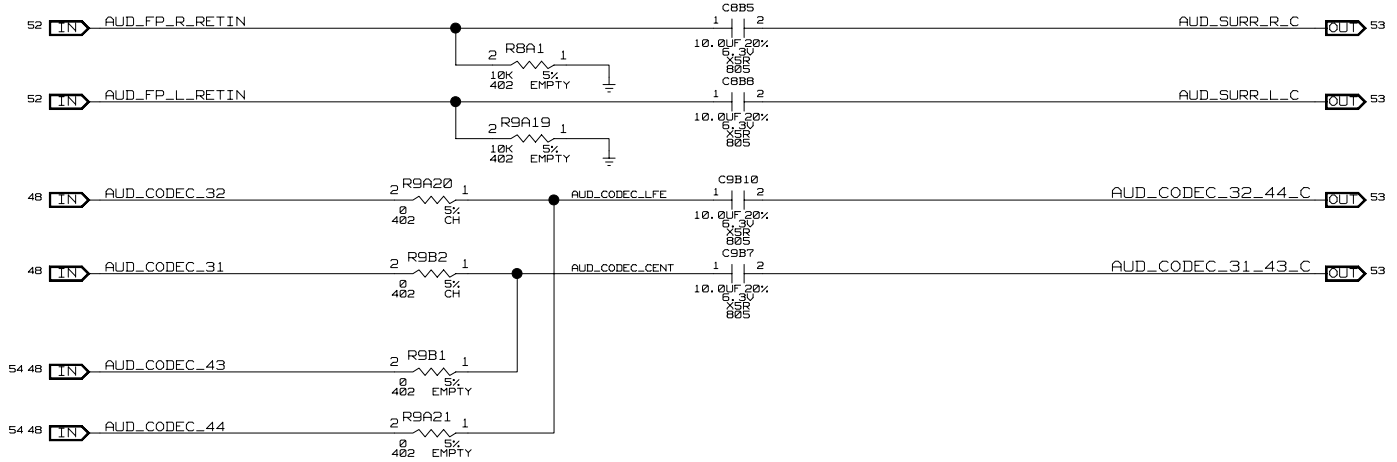
DRAWING

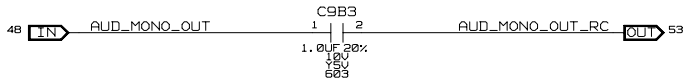
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: TRUE LINE OUT		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:35 2003	SHEET: 51



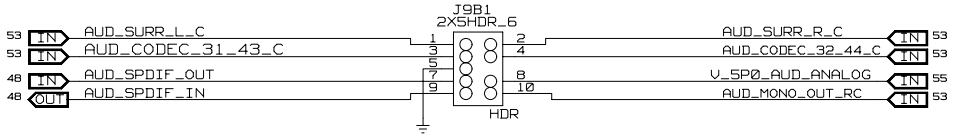
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: FP AUDIO HEADER AND MIC IN		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:36 2003	SHEET: 52





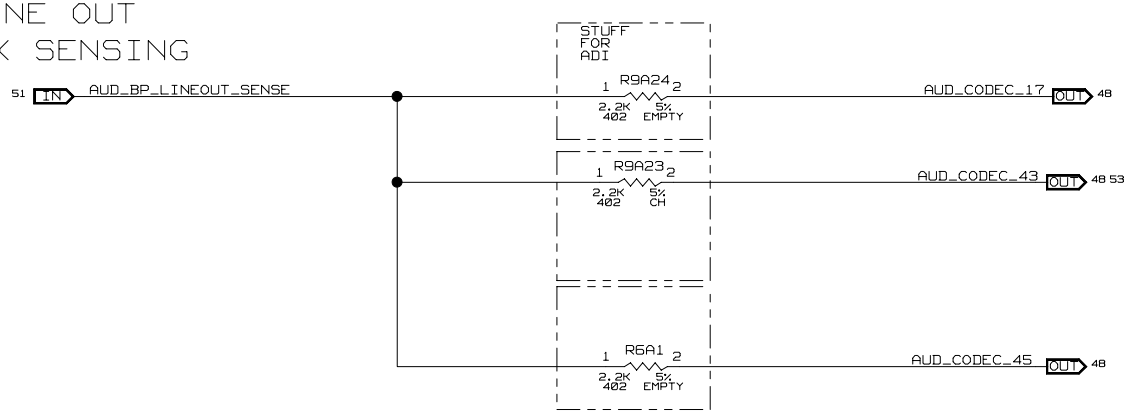
6 CHANNEL AUDIO HEADER



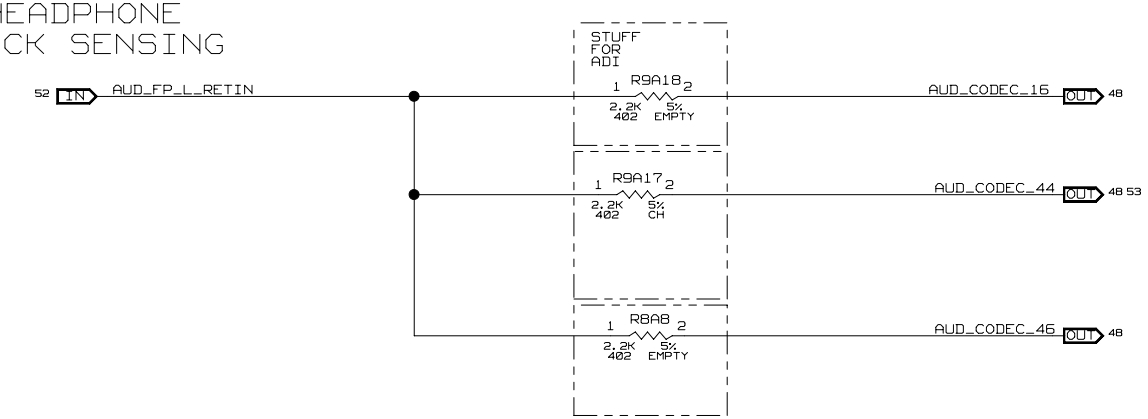
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: AUDIO OUTPUTS/6 CHANNEL HEADER		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:37 2003	SHEET: 53

LINE OUT JACK SENSING



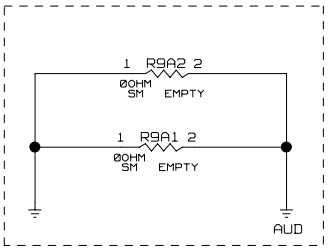
HEADPHONE JACK SENSING



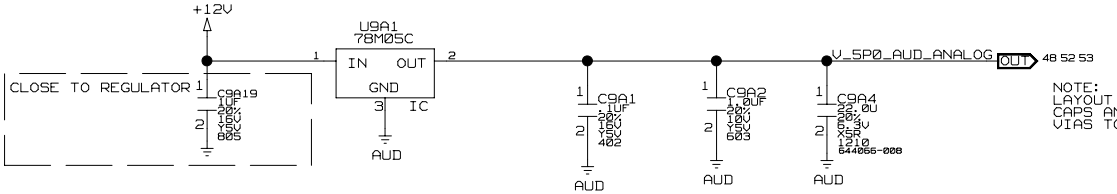
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: AUDIO JACK SENSING		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:37 2003	SHEET: 54

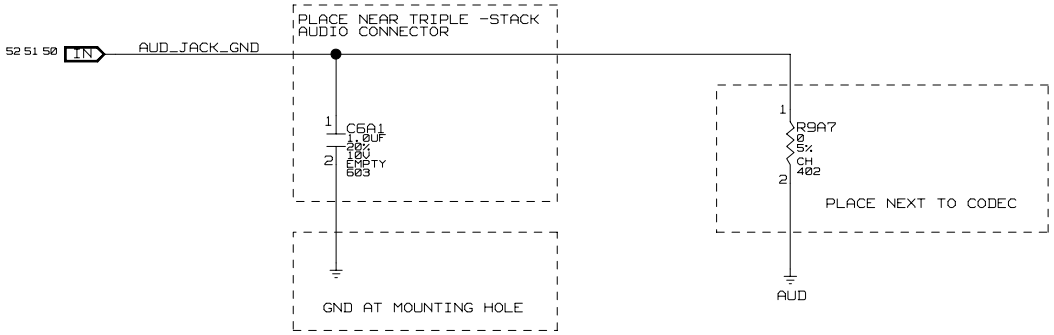
PLACE IN TOP LEFT CORNER OF BOARD



REGULATOR THERMAL TAB SHOULD BE SOLDERED
TO A COPPER PAD THAT IS LARGE ENOUGH
TO ALLOW 5 TO 10 GROUND VIAS AROUND
THE COMPONENT FOR COOLING



NOTE:
LAYOUT SHOULD GO FROM PIN 2 TO
CAPS AND THEN THROUGH SEVERAL
VIAS TO V_5P0_AUD_ANALOG

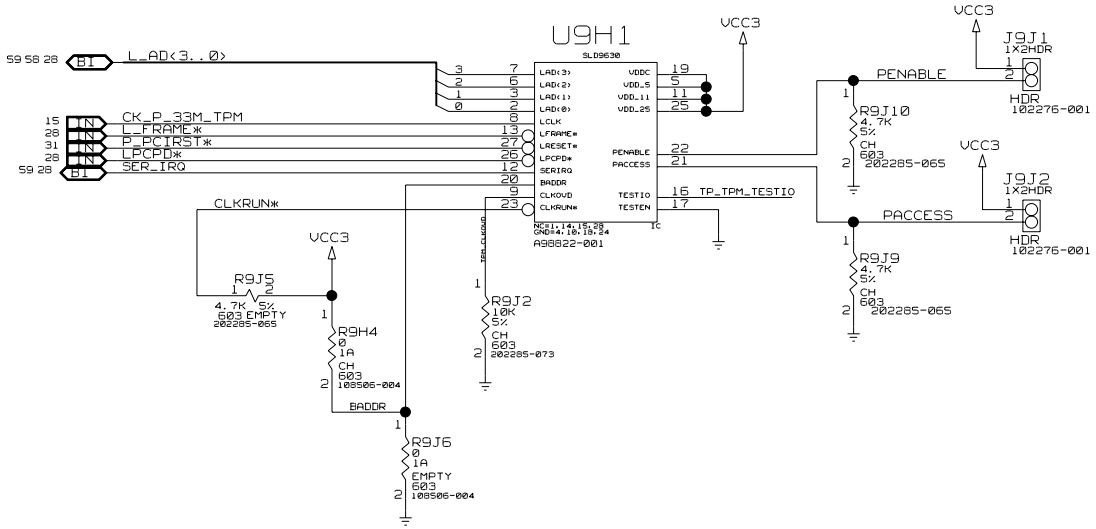


DRAWING

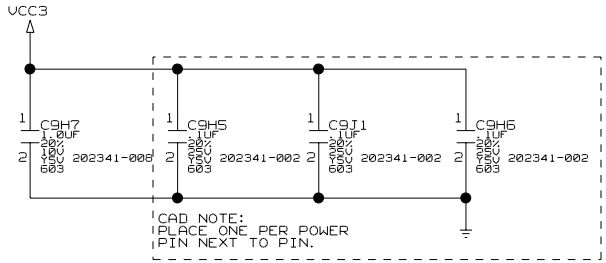
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: AUDIO VREG		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:38 2003	SHEET: 55

CR-S6

SECURITY: TPM (TRUSTED PLATFORM MODULE)

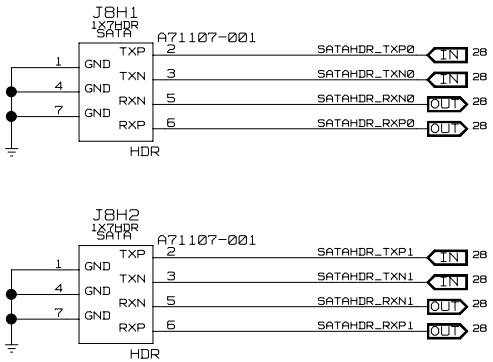


CAD NOTE:
CK_P_33M_TPM SHOULD HAVE 20MIL SPACING
P_PCIRST* SHOULD HAVE 20 MIL SPACING
LAD<3..0> HAS 5 MIL SPACING BETWEEN OTHER LAD SIGNALS, BUT 10 MILS TO ALL OTHER SIGNALS.



SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: TPM (TRUSTED PLATFORM MODULE)		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:38 2003	SHEET: 56

DRAWING



DRAWING

SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD

PAGE TITLE: SATA CONNECTORS

REV:

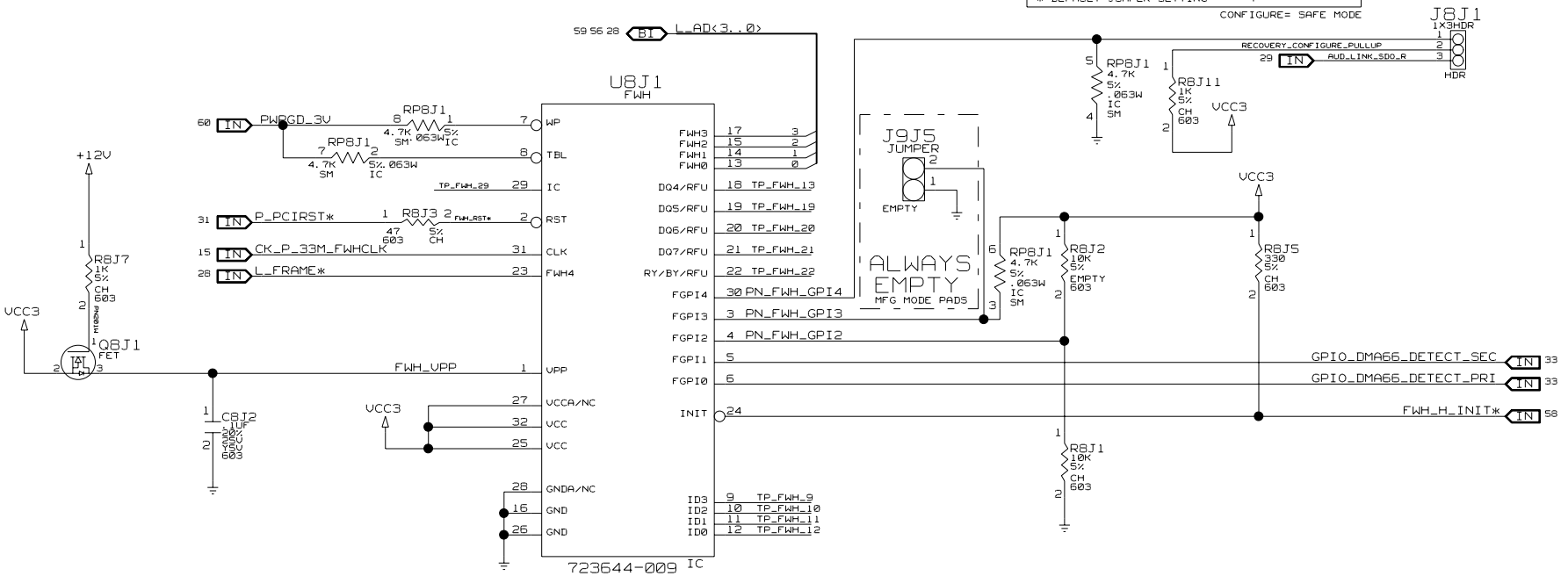
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

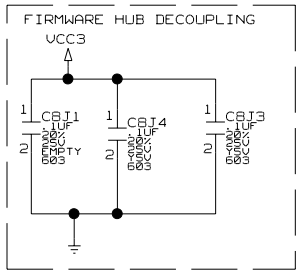
LAST REVISED:
Tue May 06 11:25:39 2003

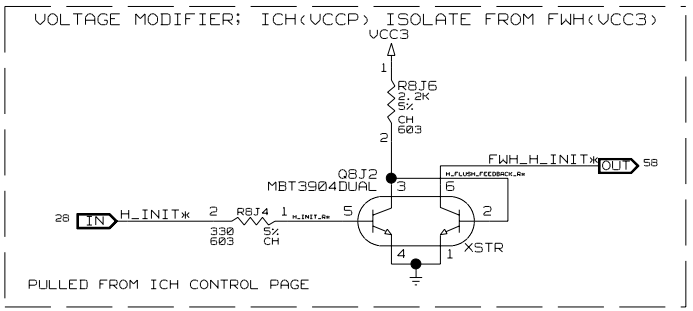
SHEET: 57

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

CONFIGURE= SAFE MODE

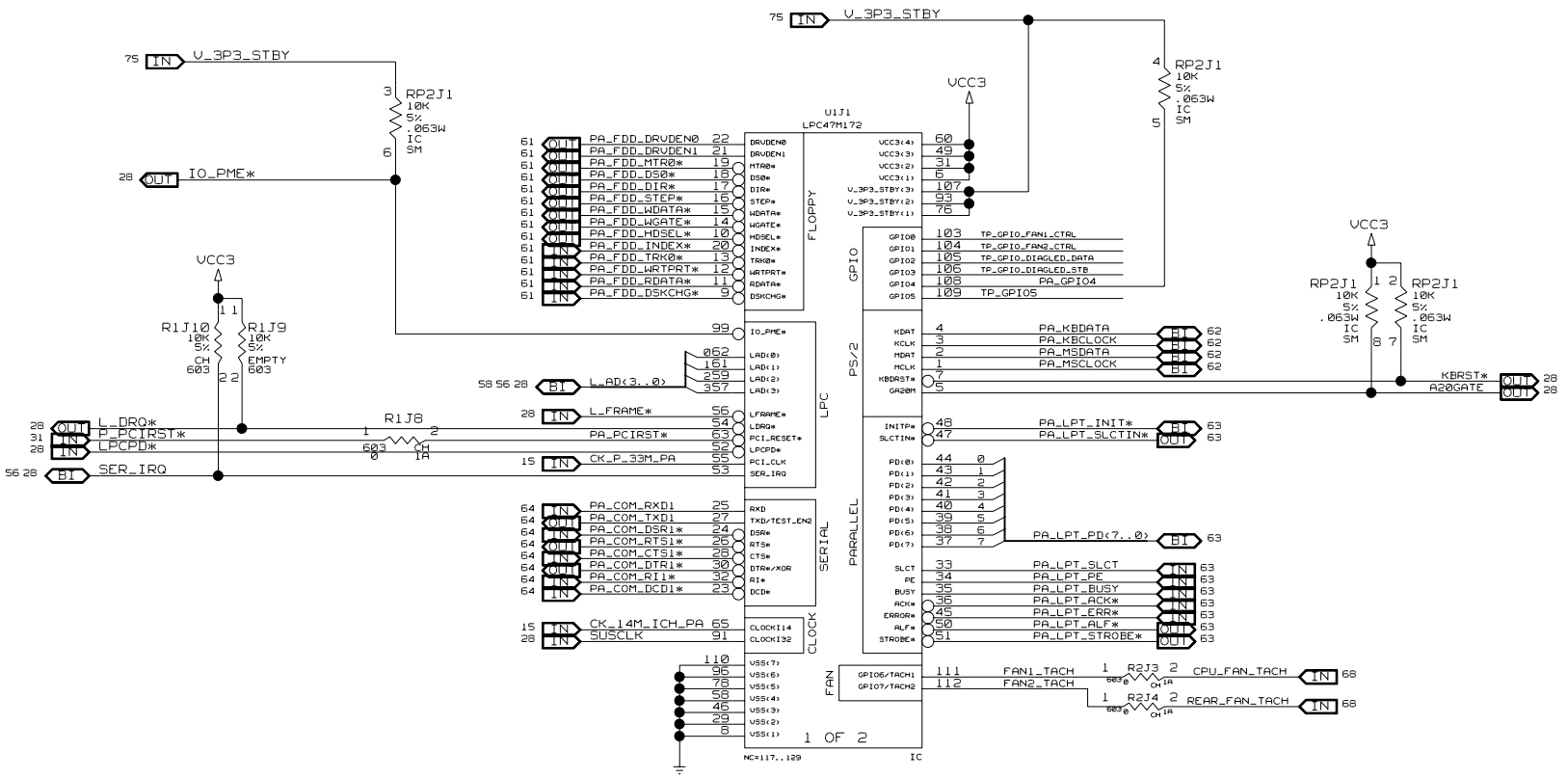






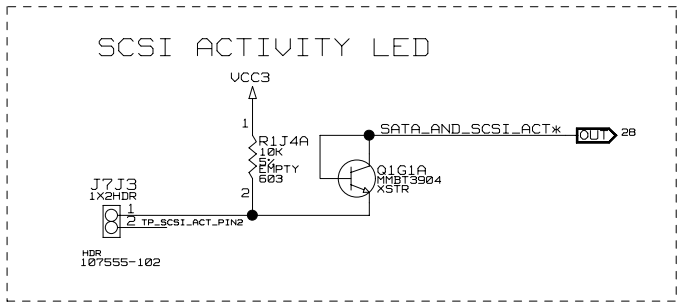
DRAWING

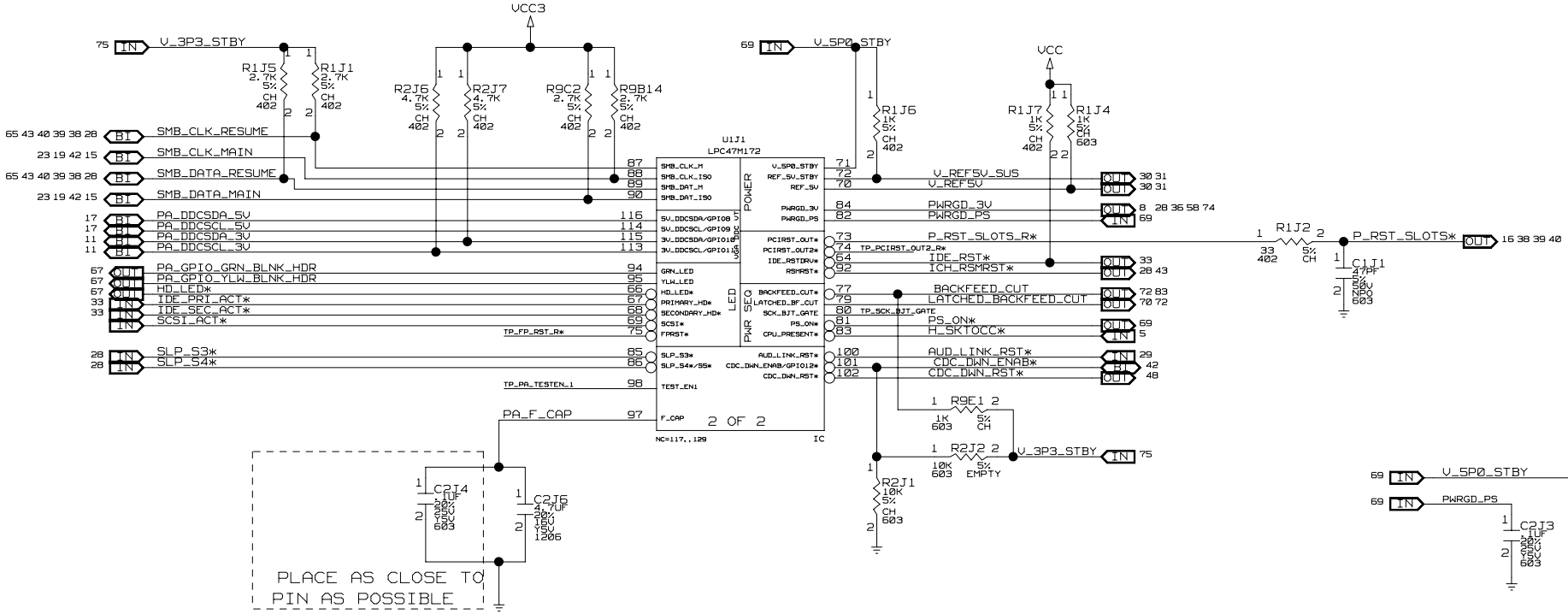
SCHEMATIC TITLE: INTEL<R> 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE: FIRMWARE HUB	REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:39 2003
	SHEET: 58



DRAWING

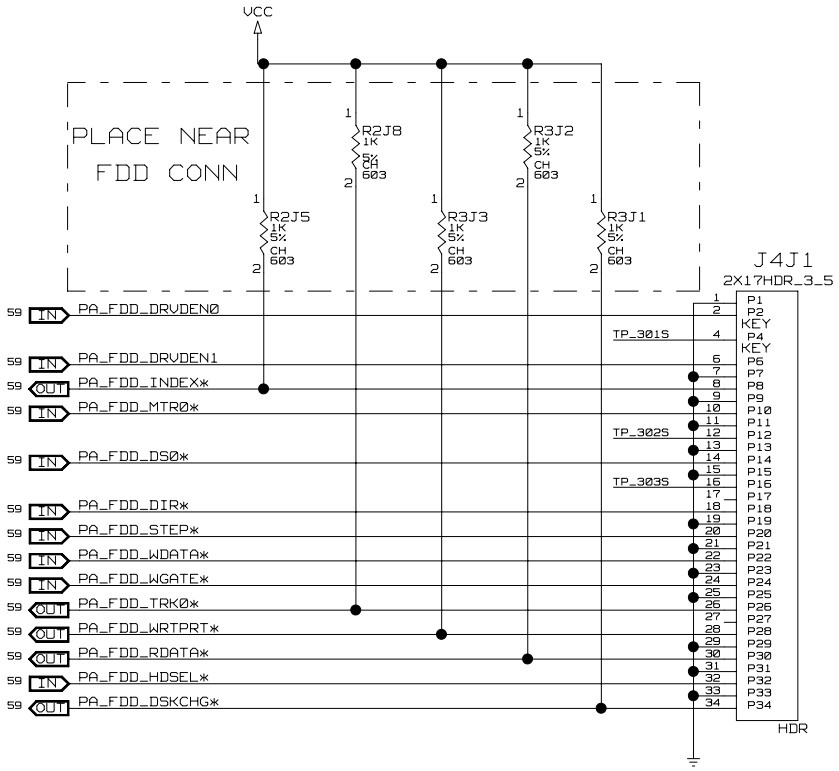
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: SIO (1 OF 2)		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:40 2003	SHEET: 59





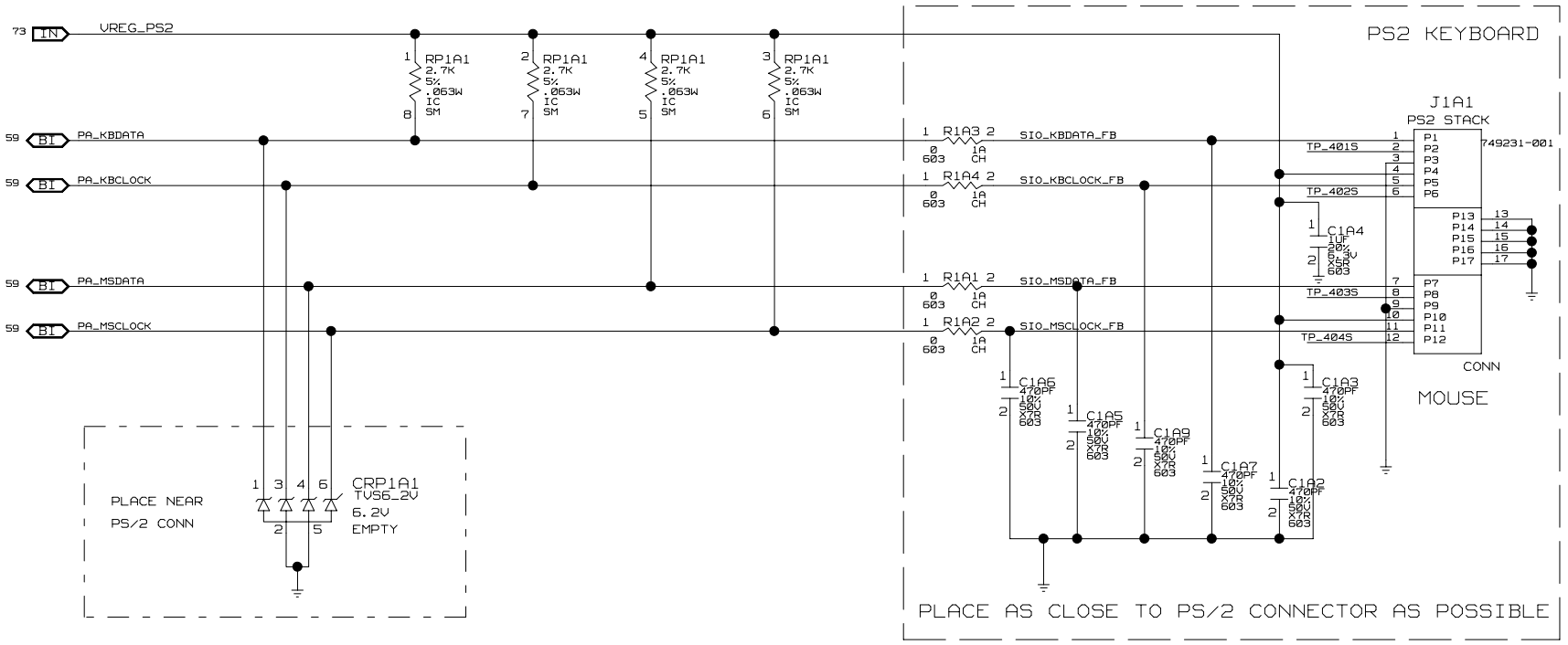
SCHEMATIC TITLE:	INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:	SIO (2 OF 2)
REV:	
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED:	Tue May 06 11:25:40 2003
SHEET:	60

DRAWING



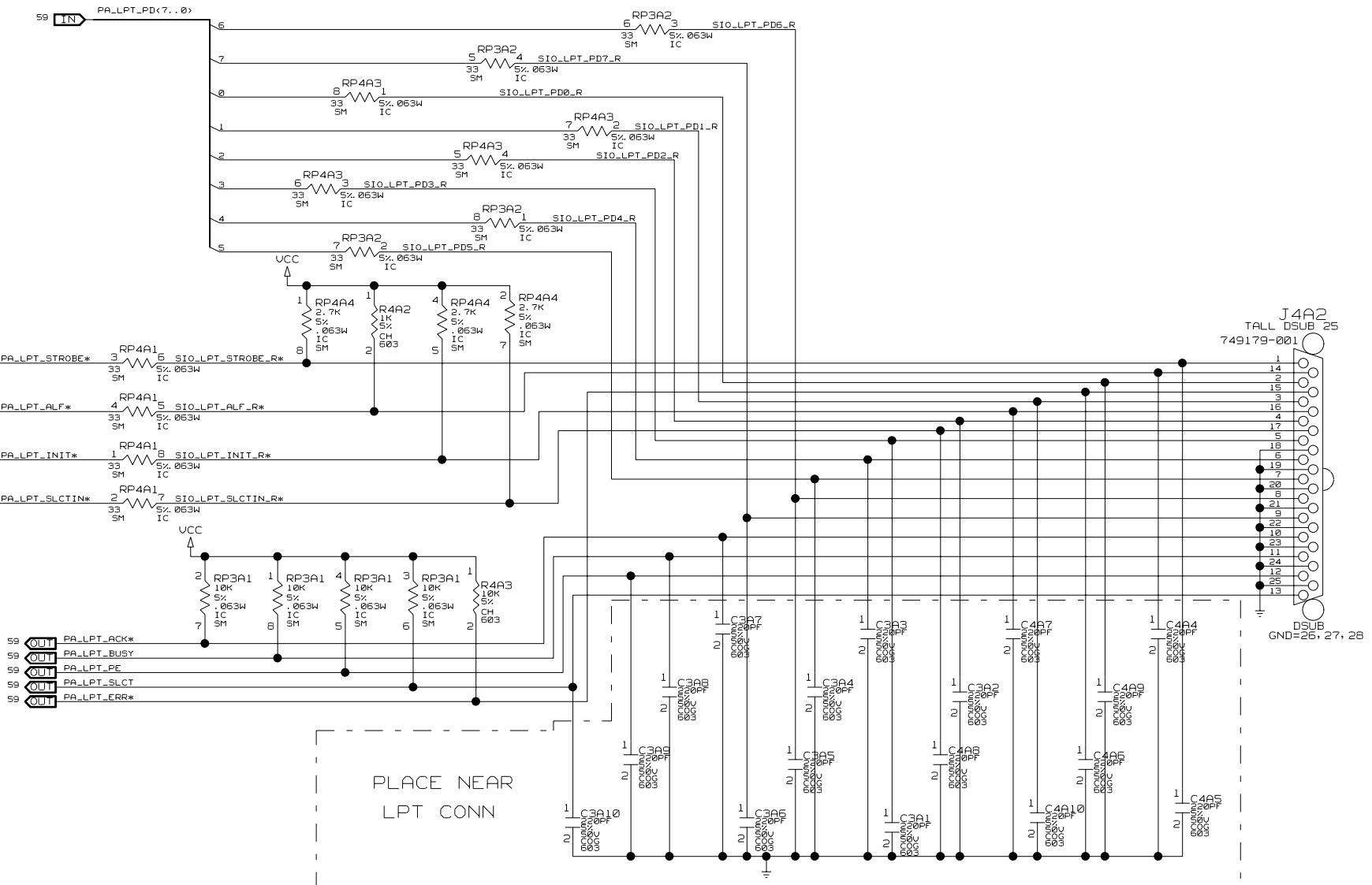
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: FLOPPY CONNECTOR		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:41 2003	SHEET: 61



DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: ATX DOUBLE-STACKED		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:42 2003	SHEET: 62



SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD

PAGE TITLE: PARALLEL PORT

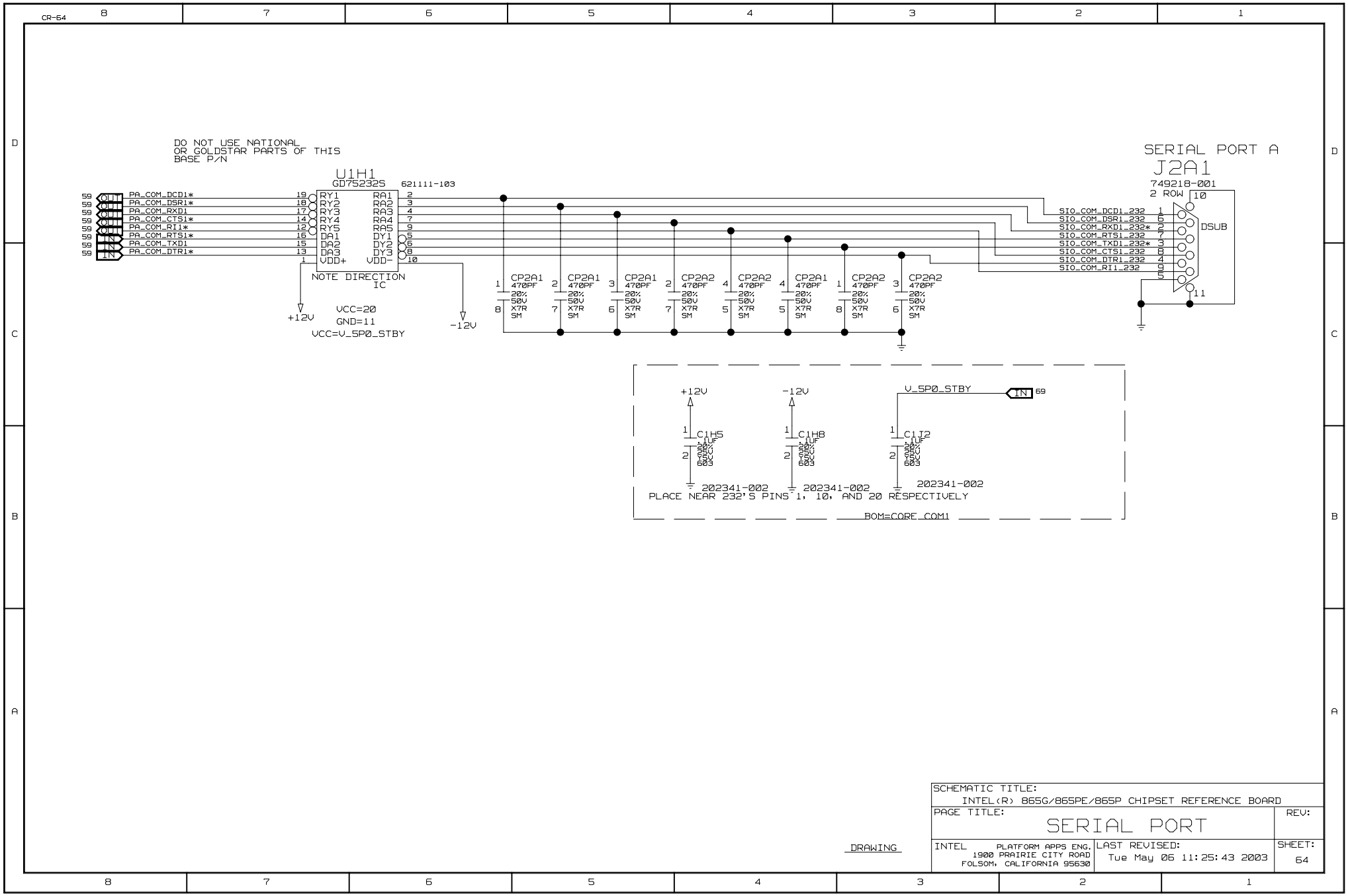
REV:

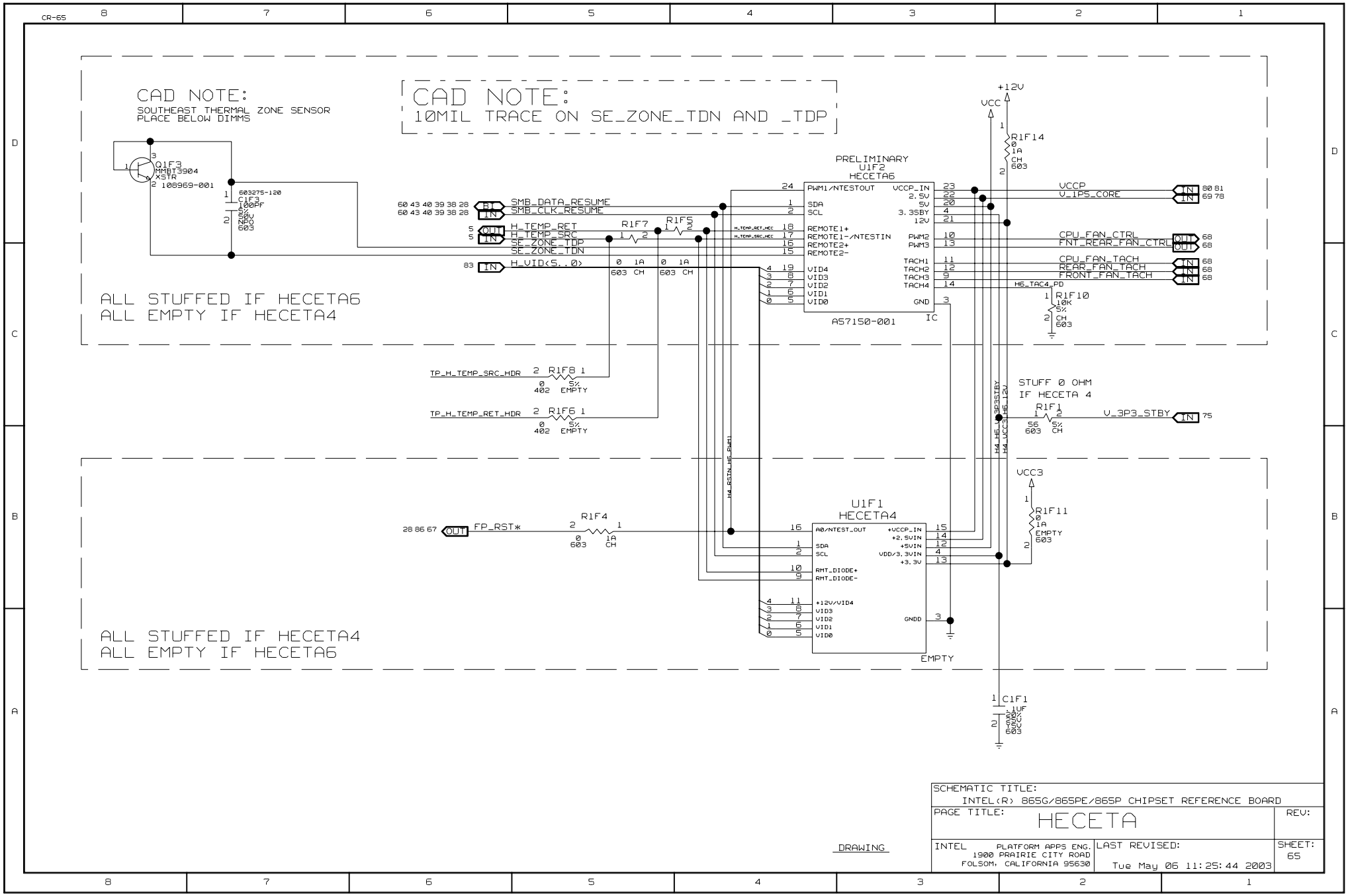
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

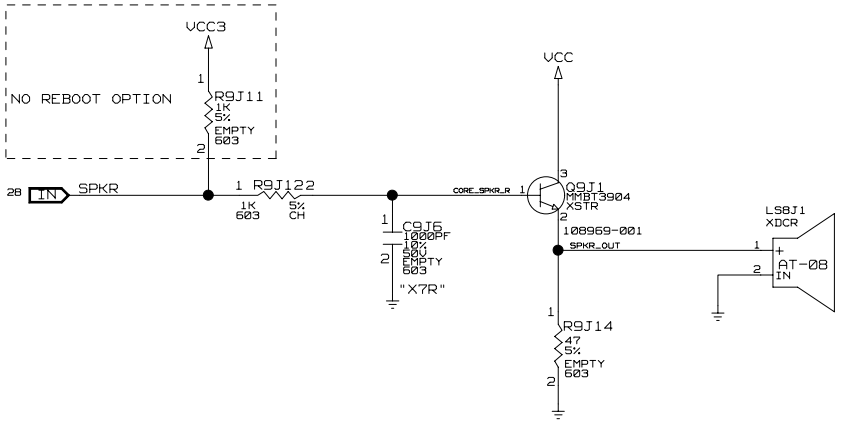
LAST REVISED:
Tue May 06 11:25:42 2003

SHEET: 63

DRAWING

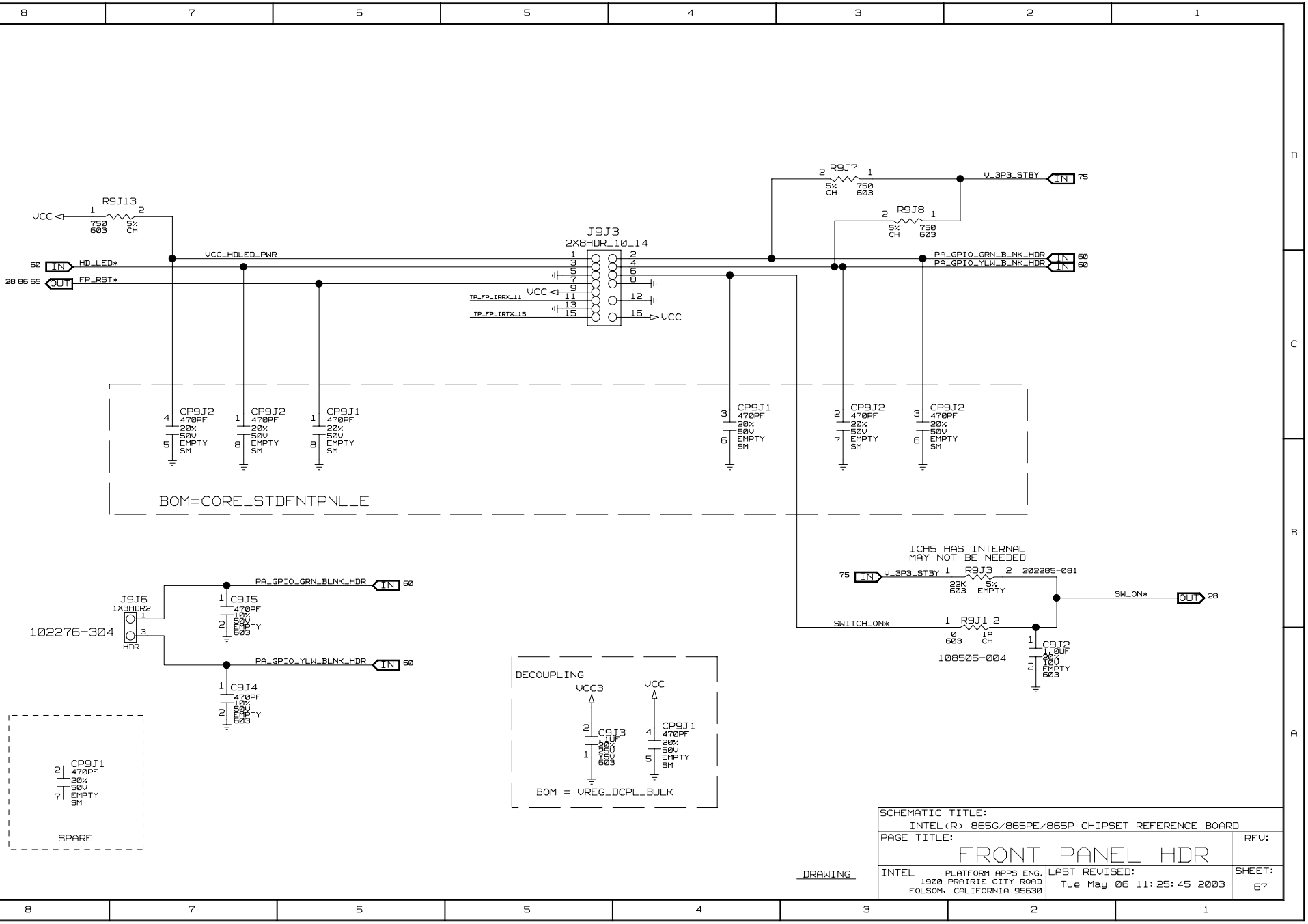

CR-64
DO NOT USE NATIONAL
OR GOLDSTAR PARTS OF THIS
BASE P/N
U1H1
GD75232S
621111-103
PA_COM_DCD1*
PA_COM_DSR1*
PA_COM_RXD1
PA_COM_CTS1*
PA_COM_RI1*
PA_COM_RTS1*
PA_COM_TXD1
PA_COM_DTR1*
RY1
RY2
RY3
RY4
RY5
DA1
DA2
DA3
VDD+
RA1
RA2
RA3
RA4
RA5
DY1
DY2
DY3
VDD-
NOTE DIRECTION
IC
+12V
VCC=20
GND=11
VCC=V_5P0_STBY
-12V
CP2A1
CP2A2
470PF
20%
50V
X7R
SM
SERIAL PORT A
J2A1
749218-001
2 ROW
DSUB
SIO_COM_DCD1_232
SIO_COM_DSR1_232
SIO_COM_RXD1_232*
SIO_COM_RTS1_232
SIO_COM_TXD1_232*
SIO_COM_CTS1_232
SIO_COM_DTR1_232
SIO_COM_RI1_232
V_5P0_STBY
C1H5
C1H8
C1J2
.1UF
202341-002
PLACE NEAR 232'S PINS 1, 10, AND 20 RESPECTIVELY
BOM=CORE_COM1
DRAWING
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
SERIAL PORT
REV:
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue May 06 11:25:43 2003
SHEET:
64


CR-65
CAD NOTE:
SOUTHEAST THERMAL ZONE SENSOR
PLACE BELOW DIMMS
CAD NOTE:
10MIL TRACE ON SE_ZONE_TDN AND _TDP
Q1F3
MMBT3904
XSTR
108969-001
603275-120
C1F3
100PF
5%
50V
NPO
603
SMB_DATA_RESUME
SMB_CLK_RESUME
H_TEMP_RET
H_TEMP_SRC
SE_ZONE_TDP
SE_ZONE_TDN
H_VID<5..0>
R1F7
R1F5
PRELIMINARY
U1F2
HECETA6
PWM1/NTESTOUT
SDA
SCL
REMOTE1+
REMOTE1-/NTESTIN
REMOTE2+
REMOTE2-
VID4
VID3
VID2
VID1
VID0
VCCP_IN
2.5V
5V
3.3SBY
12V
PWM2
PWM3
TACH1
TACH2
TACH3
TACH4
GND
A57150-001
IC
+12V
VCC
R1F14
VCCP
V_1P5_CORE
CPU_FAN_CTRL
FNT_REAR_FAN_CTRL
CPU_FAN_TACH
REAR_FAN_TACH
FRONT_FAN_TACH
H6_TAC4_PD
R1F10
10K
5%
CH
603
ALL STUFFED IF HECETA6
ALL EMPTY IF HECETA4
TP_H_TEMP_SRC_HDR
R1F8
402
EMPTY
TP_H_TEMP_RET_HDR
R1F6
STUFF 0 OHM
IF HECETA 4
R1F1
56
V_3P3_STBY
H4_RSTN_H5_PWM1
H4_H5_V_3P3STBY
H4_VCC3_H5_12V
VCC3
R1F11
EMPTY
FP_RST*
R1F4
U1F1
HECETA4
A0/NTEST_OUT
RMT_DIODE+
RMT_DIODE-
+12V/VID4
+VCCP_IN
+2.5VIN
+5VIN
VDD/3.3VIN
+3.3V
GNDD
EMPTY
ALL STUFFED IF HECETA4
ALL EMPTY IF HECETA6
C1F1
.1UF
DRAWING
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
HECETA
REV:
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue May 06 11:25:44 2003
SHEET:
65



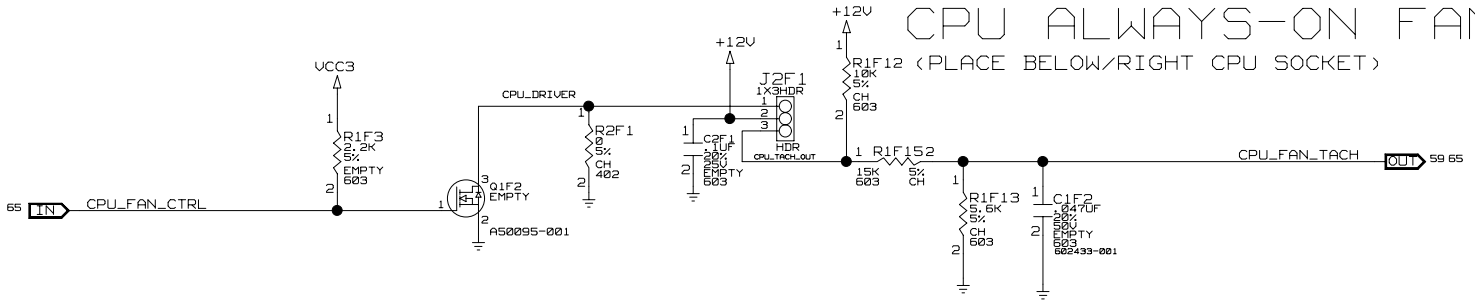
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: SPEAKER		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:44 2003	SHEET: 66


CR-67
R9J13
VCC
750
603
5%
CH
60 IN HD_LED*
28 86 65 OUT FP_RST*
VCC_HDLED_PWR
J9J3
2X8HDR_10_14
TP_FP_IRRX_11
TP_FP_IRTX_15
VCC
R9J7
V_3P3_STBY IN 75
R9J8
PA_GPIO_GRN_BLNK_HDR IN 60
PA_GPIO_YLW_BLNK_HDR IN 60
CP9J2 470PF 20% 50V EMPTY SM
CP9J1 470PF 20% 50V EMPTY SM
BOM=CORE_STDFNTPNL_E
ICH5 HAS INTERNAL
MAY NOT BE NEEDED
75 IN V_3P3_STBY
R9J3
22K
202285-081
SW_ON* OUT 28
SWITCH_ON*
R9J1
0
1A
108506-004
C9J2
1.0UF
10V
J9J6
1X3HDR2
102276-304
HDR
C9J5
C9J4
DECOUPLING
VCC3
C9J3
1UF
BOM = VREG_DCPL_BULK
SPARE
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
FRONT PANEL HDR
REV:
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue May 06 11:25:45 2003
SHEET:
67
DRAWING

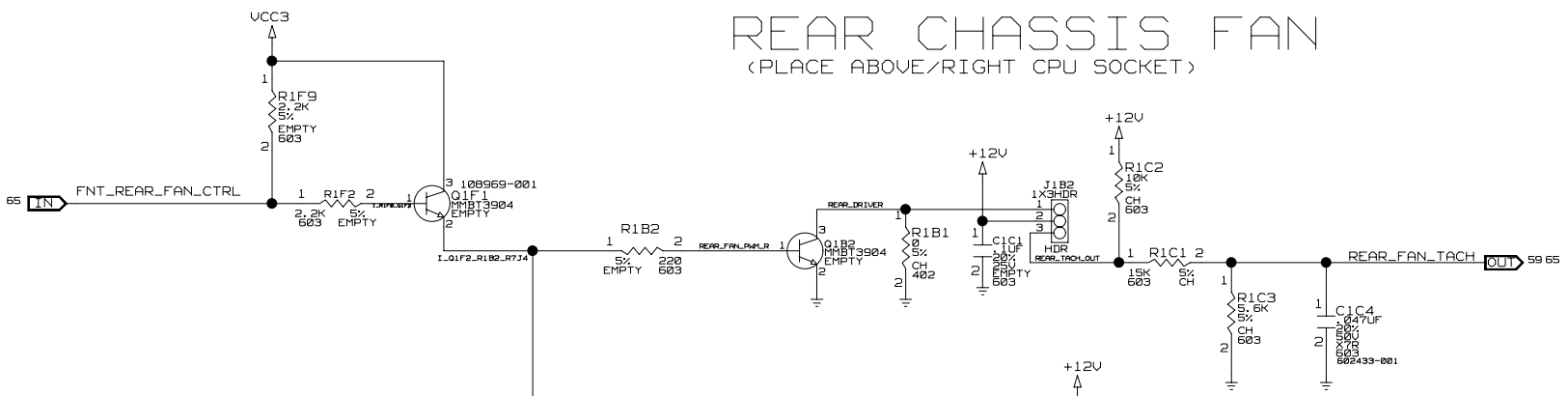
CPU ALWAYS-ON FAN

(PLACE BELOW/RIGHT CPU SOCKET)



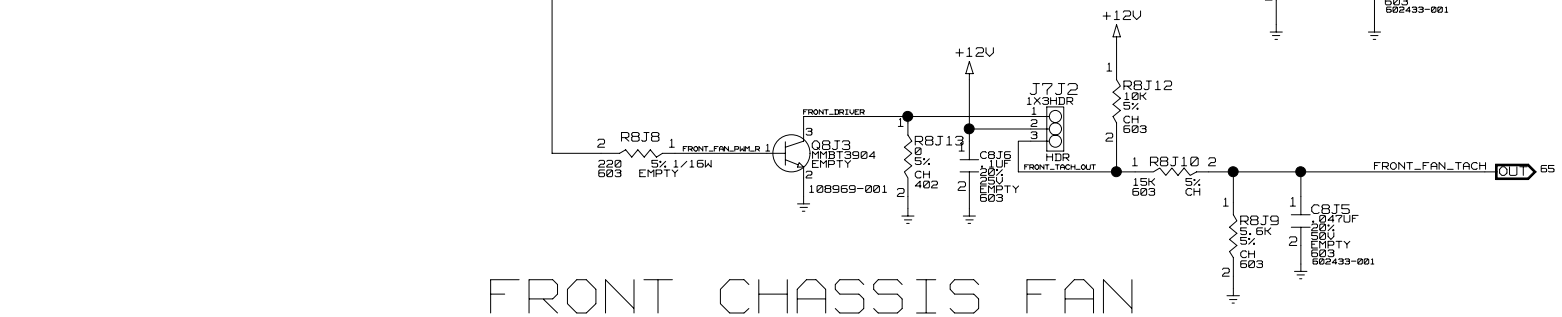
REAR CHASSIS FAN

(PLACE ABOVE/RIGHT CPU SOCKET)



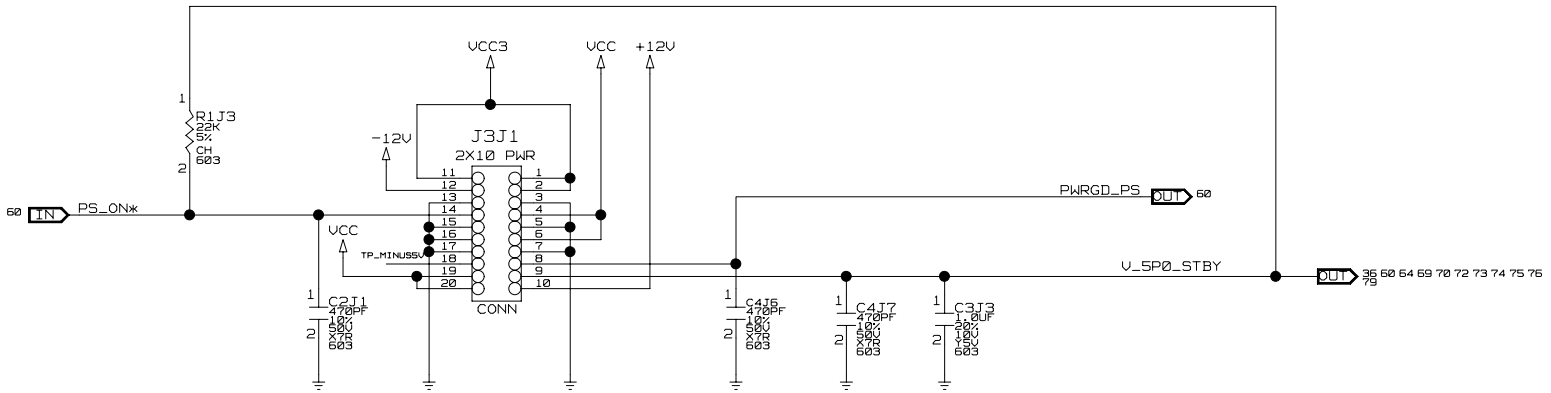
FRONT CHASSIS FAN

(PLACE LOWER LEFT CORNER OF PLATFORM)

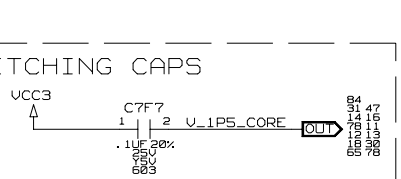


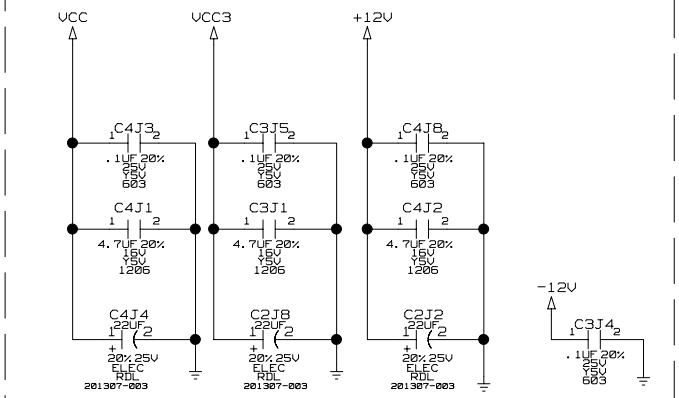
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: FAN CONTROL		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:45 2003	SHEET: 68

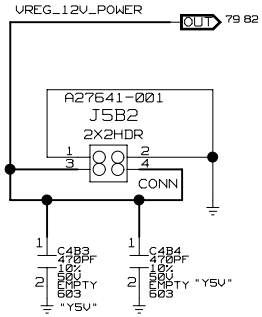


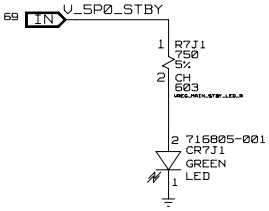
STITCHING CAPS





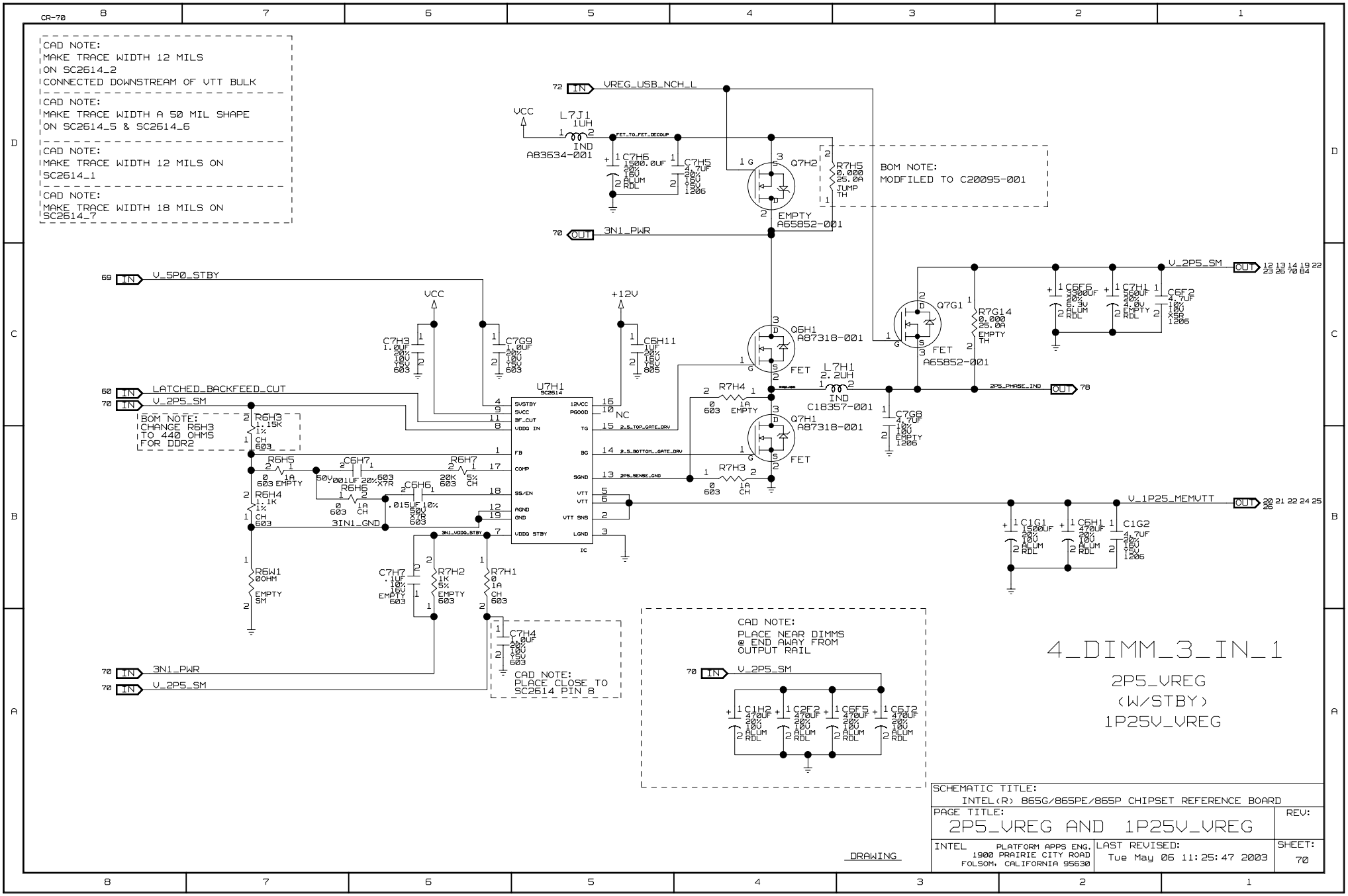
POWER CONNECTOR DECOUPLING





SCHEMATIC TITLE:	INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:	STANDARD POWER CONNECTOR
REV:	
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED:	Tue May 06 11:25:46 2003
SHEET:	69

DRAWING


CR-70
CAD NOTE:
MAKE TRACE WIDTH 12 MILS
ON SC2614_2
CONNECTED DOWNSTREAM OF VTT BULK
CAD NOTE:
MAKE TRACE WIDTH A 50 MIL SHAPE
ON SC2614_5 & SC2614_6
CAD NOTE:
MAKE TRACE WIDTH 12 MILS ON
SC2614_1
CAD NOTE:
MAKE TRACE WIDTH 18 MILS ON
SC2614_7
72 IN VREG_USB_NCH_L
VCC
L7J1
1UH
IND
A83634-001
FET_TO_FET_DECOUP
C7H6
1500.0UF
20%
16V
ALUM
RDL
C7H5
4.7UF
20%
16V
X5R
1206
Q7H2
R7H5
0.000
25.0A
JUMP
TH
EMPTY
A65852-001
BOM NOTE:
MODFILED TO C20095-001
70 OUT 3N1_PWR
69 IN V_5P0_STBY
VCC
C7H3
1.0UF
20%
10V
X5R
603
C7G9
1.0UF
20%
10V
X5R
603
+12V
C6H11
1UF
20%
16V
X7R
805
U7H1
SC2614
SVSTBY
SVCC
BF_CUT
VDDQ IN
FB
COMP
SS/EN
AGND
GND
VDDQ STBY
12VCC
PGOOD
NC
TG
2_5_TOP_GATE_DRV
BG
2_5_BOTTOM_GATE_DRV
SGND
2P5_SENSE_GND
VTT
VTT
VTT SNS
LGND
IC
Q6H1
A87318-001
FET
Q7H1
A87318-001
FET
Q7G1
FET
A65852-001
R7G14
0.000
25.0A
EMPTY
TH
L7H1
2.2UH
IND
C18357-001
2P5_PHASE_IND
OUT 78
C7G8
4.7UF
10%
10V
EMPTY
1206
R7H4
0
1A
EMPTY
603
R7H3
0
1A
CH
603
C5F6
3300UF
20%
2.5V
ALUM
RDL
C7H1
560UF
20%
2.0V
EMPTY
RDL
C5F2
4.7UF
10%
10V
X5R
1206
V_2P5_SM
OUT 12 13 14 19 22 23 26 70 84
60 IN LATCHED_BACKFEED_CUT
70 IN V_2P5_SM
BOM NOTE:
CHANGE R6H3
TO 440 OHMS
FOR DDR2
R6H3
1.15K
1%
CH
603
R6H5
0
1A
EMPTY
603
C6H7
.001UF
50V
20%
X7R
603
R6H7
20K
5%
CH
603
R6H4
1.1K
1%
CH
603
R6H8
0
1A
CH
603
C6H5
.015UF
10%
50V
X7R
603
3IN1_GND
R6W1
0OHM
EMPTY
SM
C7H7
.1UF
10%
16V
EMPTY
603
R7H2
1K
5%
EMPTY
603
R7H1
0
1A
CH
603
3N1_VDDQ_STBY
C7H4
1.0UF
20%
10V
X5R
603
CAD NOTE:
PLACE CLOSE TO
SC2614 PIN 8
70 IN 3N1_PWR
70 IN V_2P5_SM
V_1P25_MEMVTT
OUT 20 21 22 24 25 26
C1G1
1500UF
20%
10V
ALUM
RDL
C6H1
470UF
20%
10V
ALUM
RDL
C1G2
4.7UF
20%
16V
X5R
1206
CAD NOTE:
PLACE NEAR DIMMS
@ END AWAY FROM
OUTPUT RAIL
70 IN V_2P5_SM
C1H2
470UF
20%
10V
ALUM
RDL
C2F2
470UF
20%
10V
ALUM
RDL
C5F5
470UF
20%
10V
ALUM
RDL
C5J2
470UF
20%
10V
ALUM
RDL
4_DIMM_3_IN_1
2P5_VREG
(W/STBY)
1P25V_VREG
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
2P5_VREG AND 1P25V_VREG
REV:
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
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DRAWING

CR-71

PB MOUNTING HOLES

J1G1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J9G1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J7G1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J7J1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J1B1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J7A1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J1J1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J8A1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

DRAWING

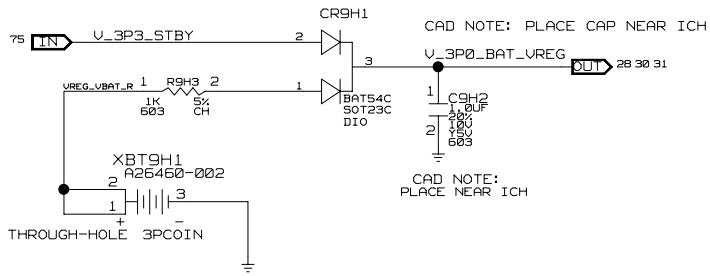
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: PB MOUNTING HOLES		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:47 2003	SHEET: 71

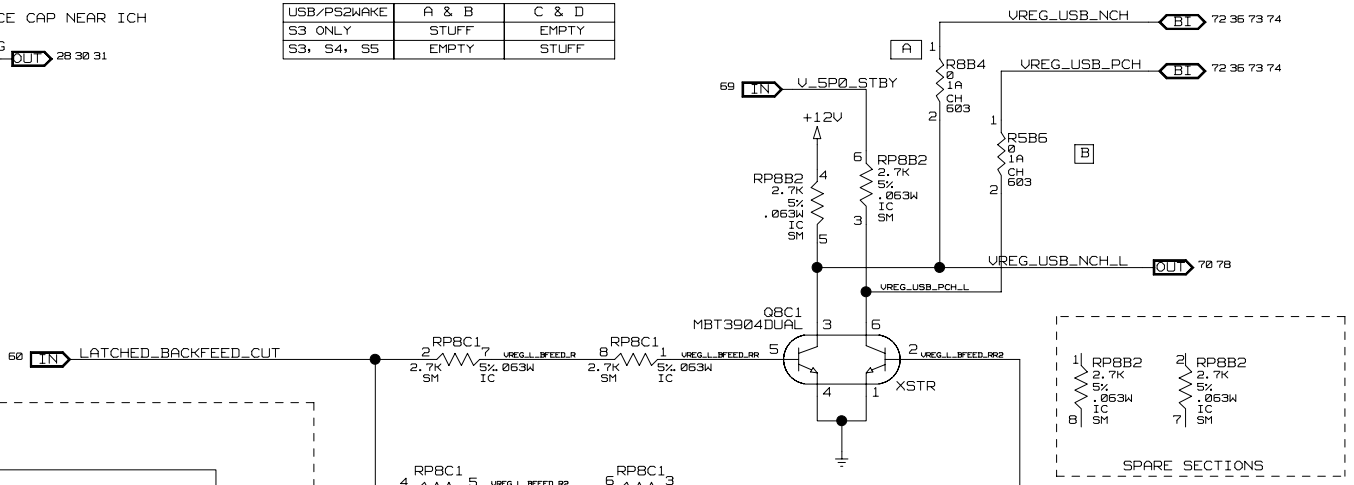
BATTERY

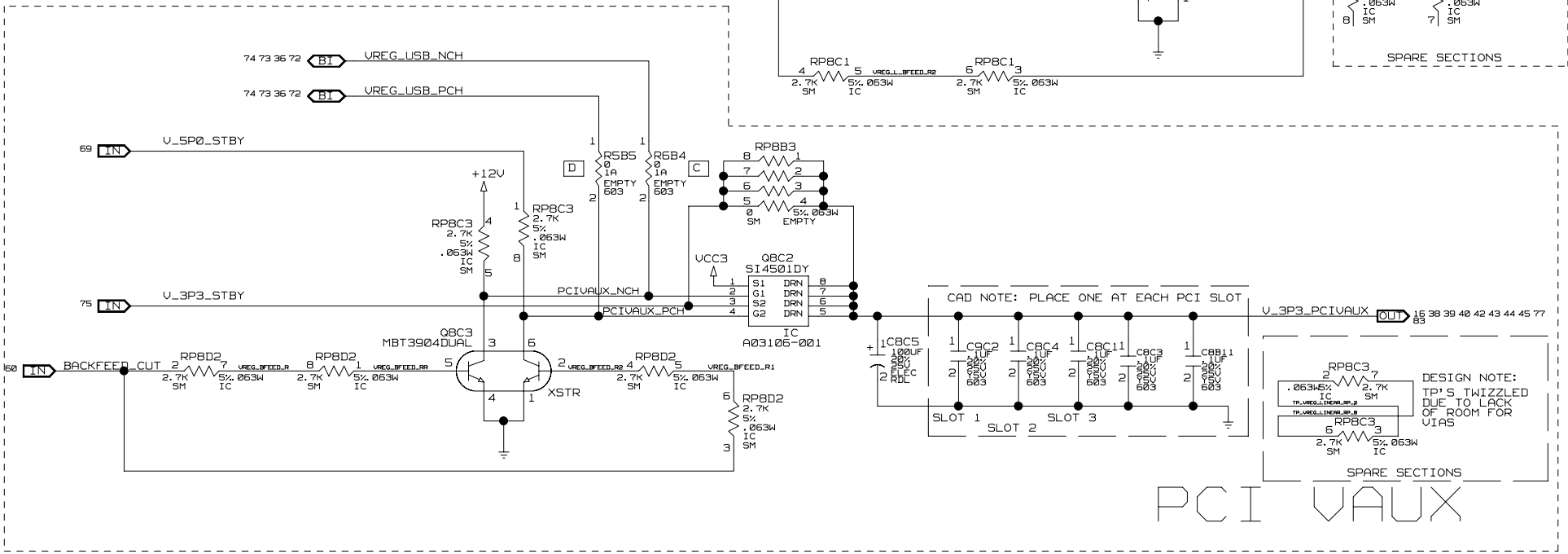
BOM=VREG
ROOM = VREG UNLESS SPECIFIED

NOTES:

USB/PS2WAKE	A & B	C & D
S3 ONLY	STUFF	EMPTY
S3, S4, S5	EMPTY	STUFF



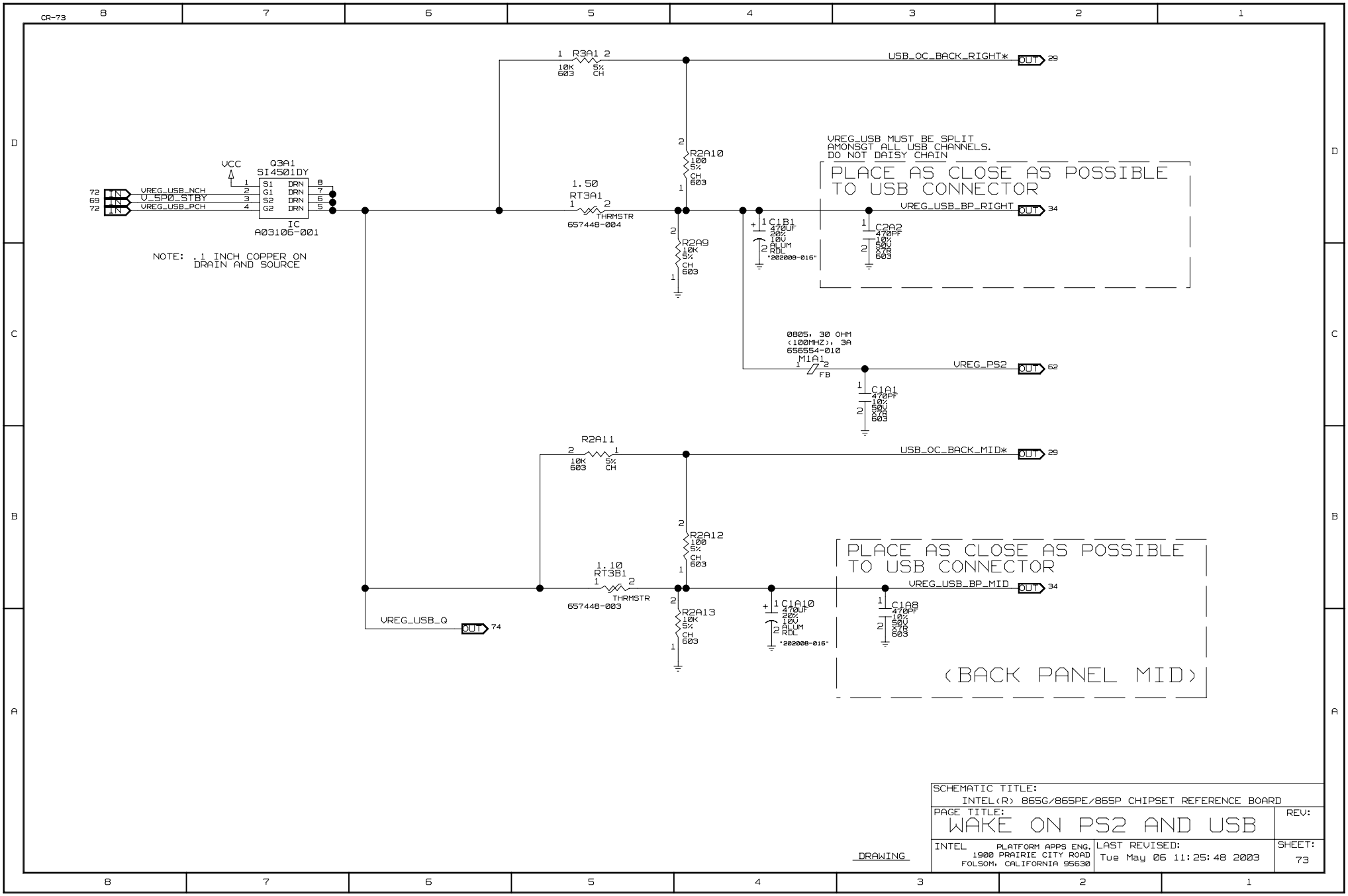


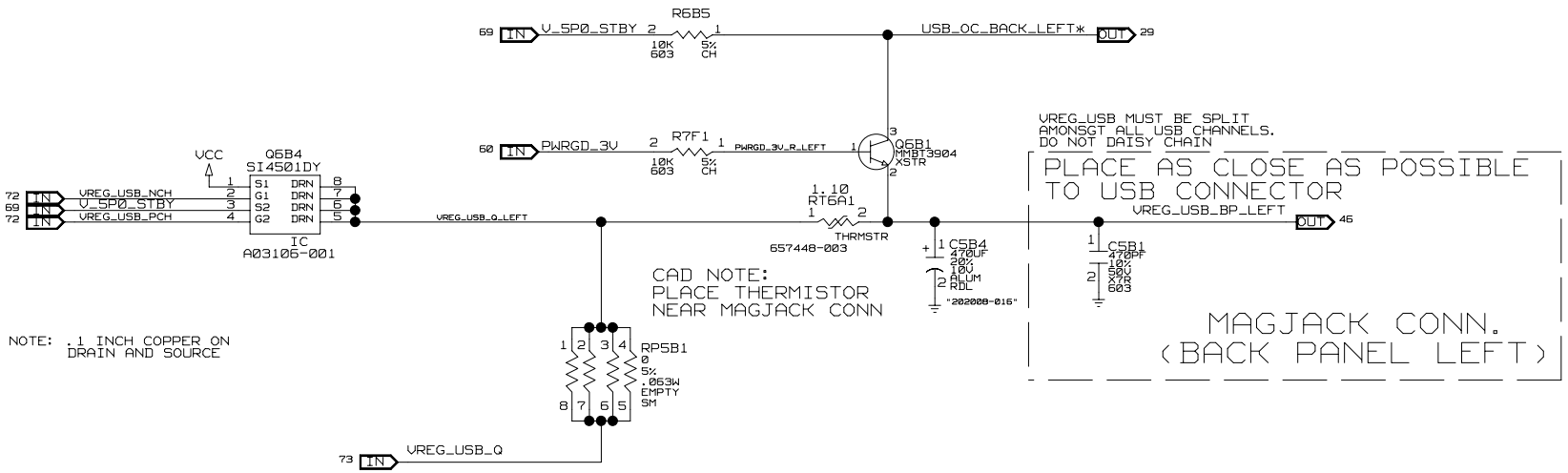


PCI VAUX

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: WAKE ON PS2 & USB (BACK PANEL RIGHT)		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:48 2003	SHEET: 72

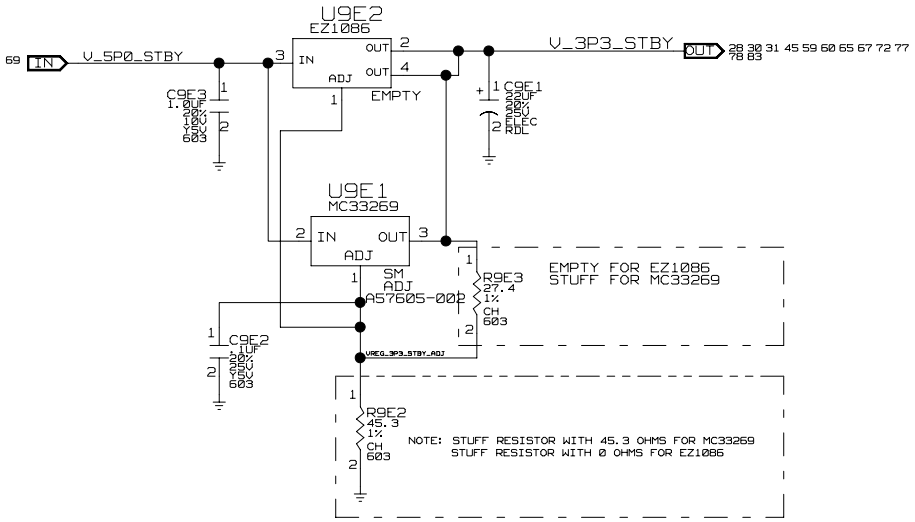
DRAWING

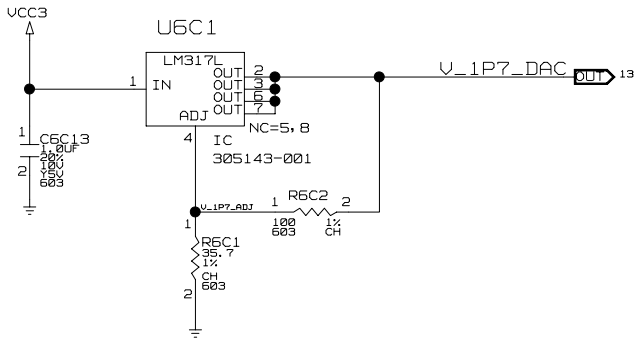

CR-73
8
7
6
5
4
3
2
1
D
C
B
A
R3A1
10K
603
5%
CH
USB_OC_BACK_RIGHT*
OUT 29
R2A10
100
5%
CH
603
VREG_USB MUST BE SPLIT
AMONSGT ALL USB CHANNELS.
DO NOT DAISY CHAIN
PLACE AS CLOSE AS POSSIBLE
TO USB CONNECTOR
VCC
Q3A1
SI4501DY
72 IN VREG_USB_NCH
69 IN V_5P0_STBY
72 IN VREG_USB_PCH
S1 S2 G1 G2 DRN DRN DRN DRN
IC
A03106-001
NOTE: .1 INCH COPPER ON
DRAIN AND SOURCE
1.5Ω
RT3A1
THRMSTR
657448-004
R2A9
10K
5%
CH
603
C1B1
470UF
20%
16V
ALUM
RDL
"202008-016"
VREG_USB_BP_RIGHT
OUT 34
C2A2
470PF
10%
50V
X7R
603
0805, 30 OHM
(100MHZ), 3A
656554-010
M1A1
FB
VREG_PS2
OUT 52
C1A1
470PF
10%
50V
X7R
603
R2A11
10K
603
5%
CH
USB_OC_BACK_MID*
OUT 29
R2A12
100
5%
CH
603
1.1Ω
RT3B1
THRMSTR
657448-003
R2A13
10K
5%
CH
603
C1A10
470UF
20%
16V
ALUM
RDL
"202008-016"
VREG_USB_BP_MID
OUT 34
C1A8
470PF
10%
50V
X7R
603
PLACE AS CLOSE AS POSSIBLE
TO USB CONNECTOR
(BACK PANEL MID)
VREG_USB_Q
OUT 74
DRAWING
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
WAKE ON PS2 AND USB
REV:
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue May 06 11:25:48 2003
SHEET:
73



DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: WAKE ON USB AND MAGNETICS JACK		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:49 2003	SHEET: 74





SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: 3.3V STANDBY & 1.7V DAC		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:50 2003	SHEET: 75

DRAWING

CR-75

-12V

C7B9 .1UF 20% 25V Y5V EMPTY 603

C9B11 .1UF 20% 25V Y5V EMPTY 603

CAD NOTE:
ONE FOR EACH PCI SLOT

+12V

C8E6 .1UF 20% 25V Y5V 603

C9F2 .1UF 20% 25V Y5V 603

C9H3 .1UF 20% 25V Y5V 603

CAD NOTE:
ONE FOR EACH PCI SLOT
ONE FOR AGP CONN

69 IN V_5P0_STBY

C3J2 .1UF 20% 25V Y5V 603

C9G4 .1UF 20% 25V Y5V 603

C9H4 1000UF 20% 10V ELEC RDL "THMNT ALUM ELEC"

PCI SLOT DECOUPLING

VCC3 C8D2 22UF 20% 25V EMPTY RDL

VCC3 C8D1 100UF 20% 25V EMPTY RDL

VCC C8E1 22UF 20% 25V EMPTY RDL

VCC3 C8C7 22UF 20% 25V EMPTY RDL

VCC C8E4 100UF 20% 25V ELEC RDL

VCC3

C9D1 .1UF 20% 25V Y5V 603

C7G7 .1UF 20% 25V Y5V 603

C7D4 .1UF 20% 25V Y5V 603

CAD NOTE:
PLACE @
AGP CONN

CAD NOTE:
ONE FOR EACH PCI SLOT
ONE FOR AGP CONN

VCC

C9D2 100UF 20% 25V ELEC RDL

C2A1 .1UF 20% 25V EMPTY 603

C3J6 .1UF 20% 25V EMPTY 603

C9C3 .1UF 20% 25V EMPTY 603

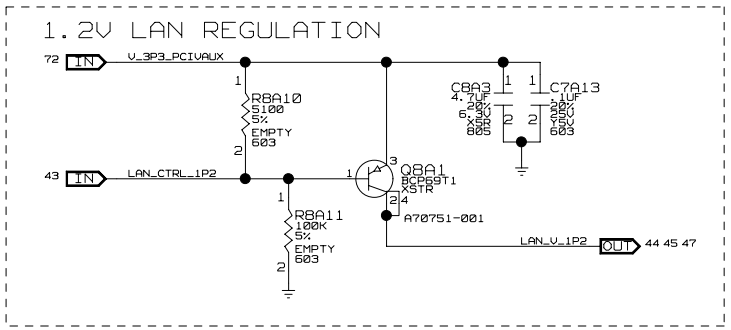
C3J7 .1UF 20% 25V EMPTY 603

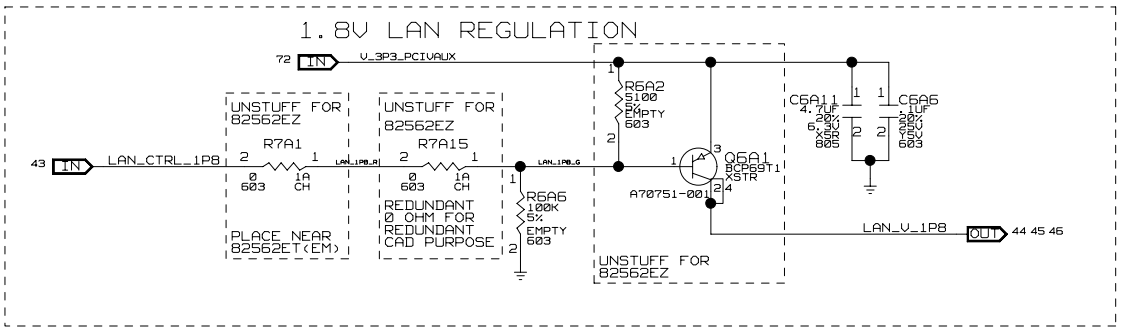
C4J5 .1UF 20% 25V EMPTY 603

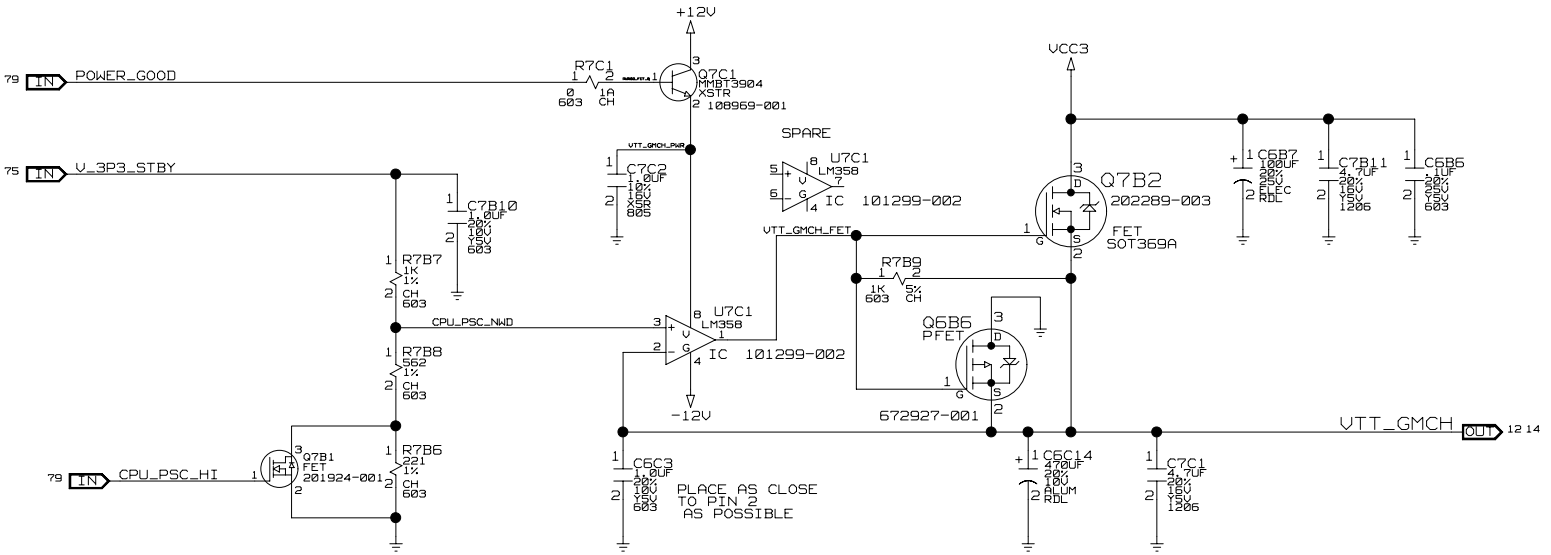
CAD NOTE:
ONE FOR EACH PCI SLOT

DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: VREG BULK DECOUPLING		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:50 2003	SHEET: 76

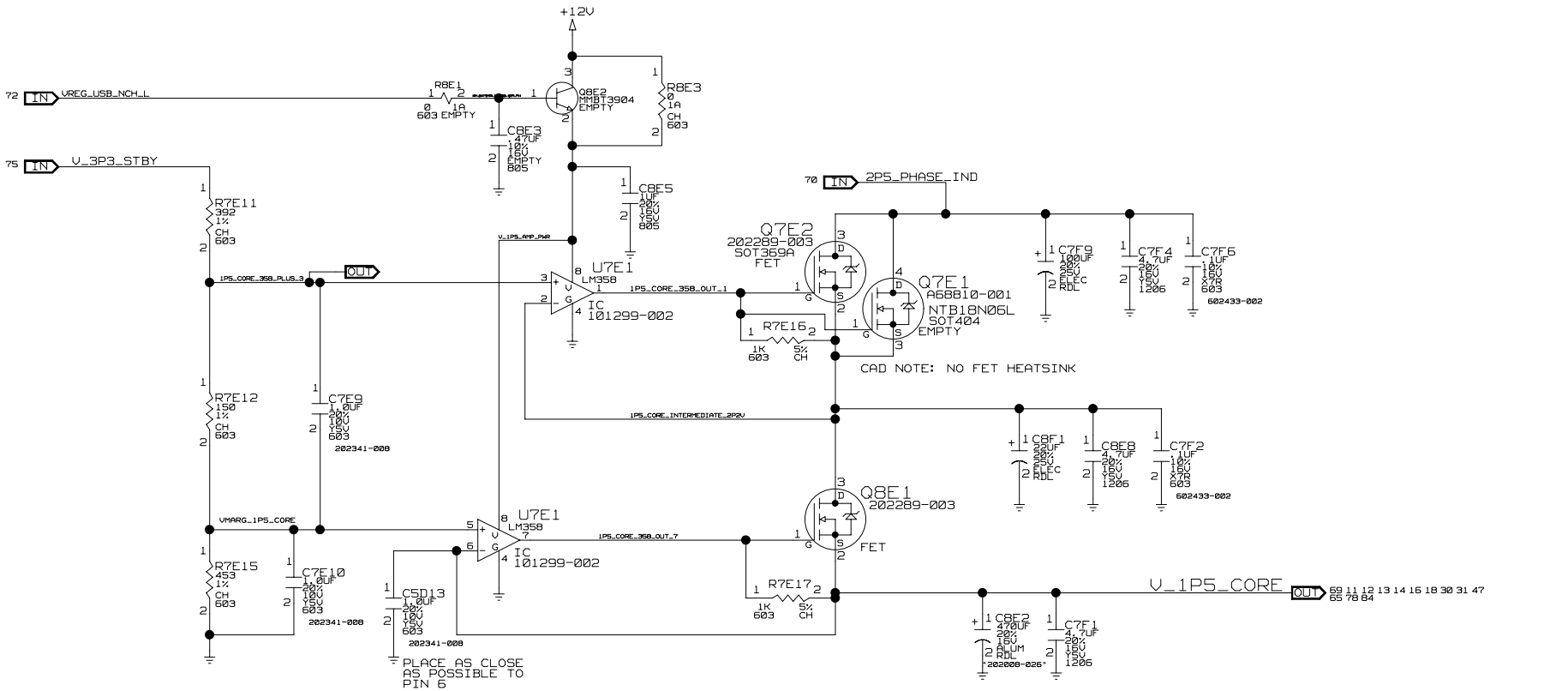






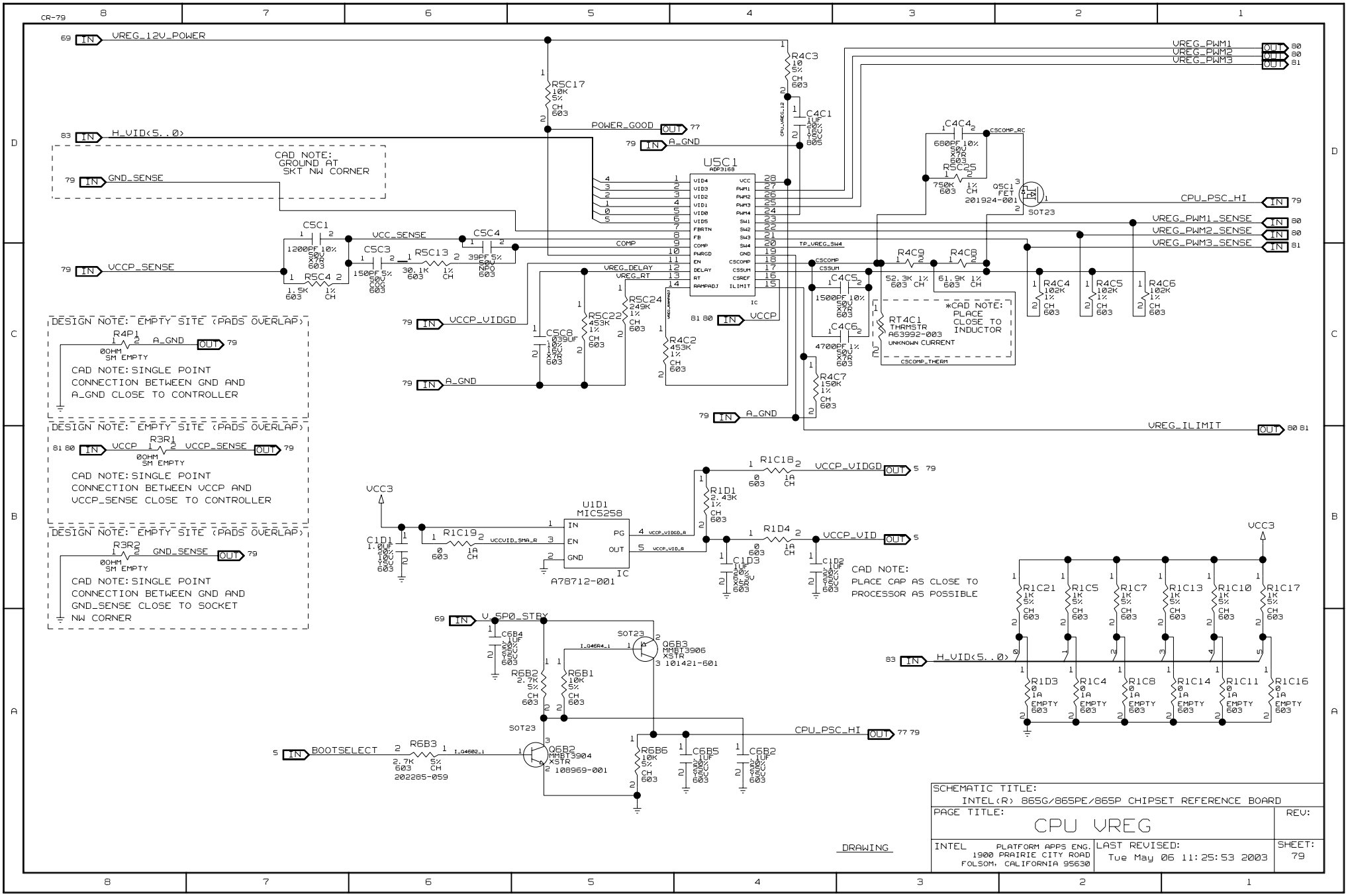
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD	
PAGE TITLE: LAN VREG/PROCESSOR SELECT	REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:51 2003
	SHEET: 77



DRAWING

SCHEMATIC TITLE:	INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:	1.5V CORE
REV:	
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:52 2003
SHEET:	78


VREG_12V_POWER
H_VID<5..0>
GND_SENSE
VCCP_SENSE
POWER_GOOD
A_GND
VREG_PWM1
VREG_PWM2
VREG_PWM3
CPU_PSC_HI
VREG_PWM1_SENSE
VREG_PWM2_SENSE
VREG_PWM3_SENSE
VREG_ILIMIT
VCCP_VIDGD
VCCP
VCCP_VID
VCC3
V_5P0_STBY
BOOTSELECT
U5C1
ADP3168
U1D1
MIC5258
A78712-001
Q5C1
FET
201924-001
Q6B3
MMBT3906
Q6B2
MMBT3904
RT4C1
THRMSTR
A63992-003
UNKNOWN CURRENT
CAD NOTE:
GROUND AT
SKT NW CORNER
DESIGN NOTE: EMPTY SITE (PADS OVERLAP)
CAD NOTE: SINGLE POINT
CONNECTION BETWEEN GND AND
A_GND CLOSE TO CONTROLLER
CAD NOTE: SINGLE POINT
CONNECTION BETWEEN VCCP AND
VCCP_SENSE CLOSE TO CONTROLLER
CAD NOTE: SINGLE POINT
CONNECTION BETWEEN GND AND
GND_SENSE CLOSE TO SOCKET
NW CORNER
*CAD NOTE:
PLACE
CLOSE TO
INDUCTOR
CAD NOTE:
PLACE CAP AS CLOSE TO
PROCESSOR AS POSSIBLE
DRAWING
SCHEMATIC TITLE:
INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD
PAGE TITLE:
CPU VREG
REV:
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
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SHEET:
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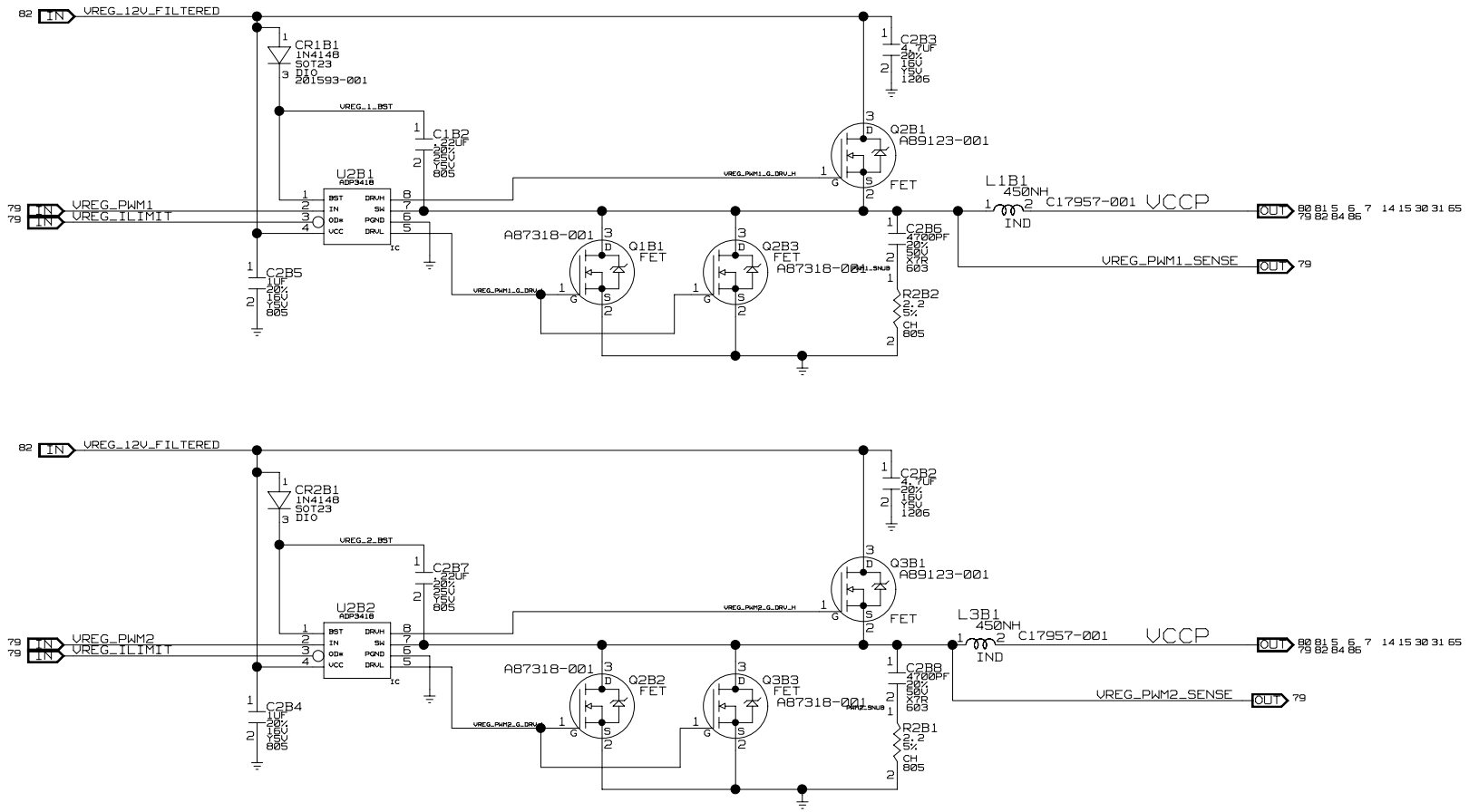
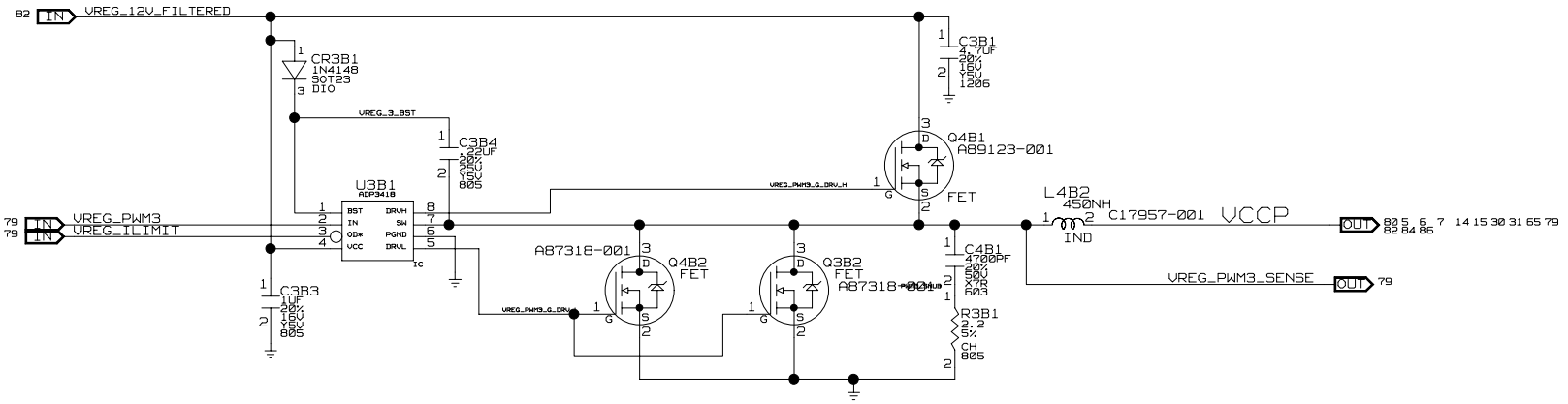


DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: CPU VREG		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:53 2003	SHEET: 80



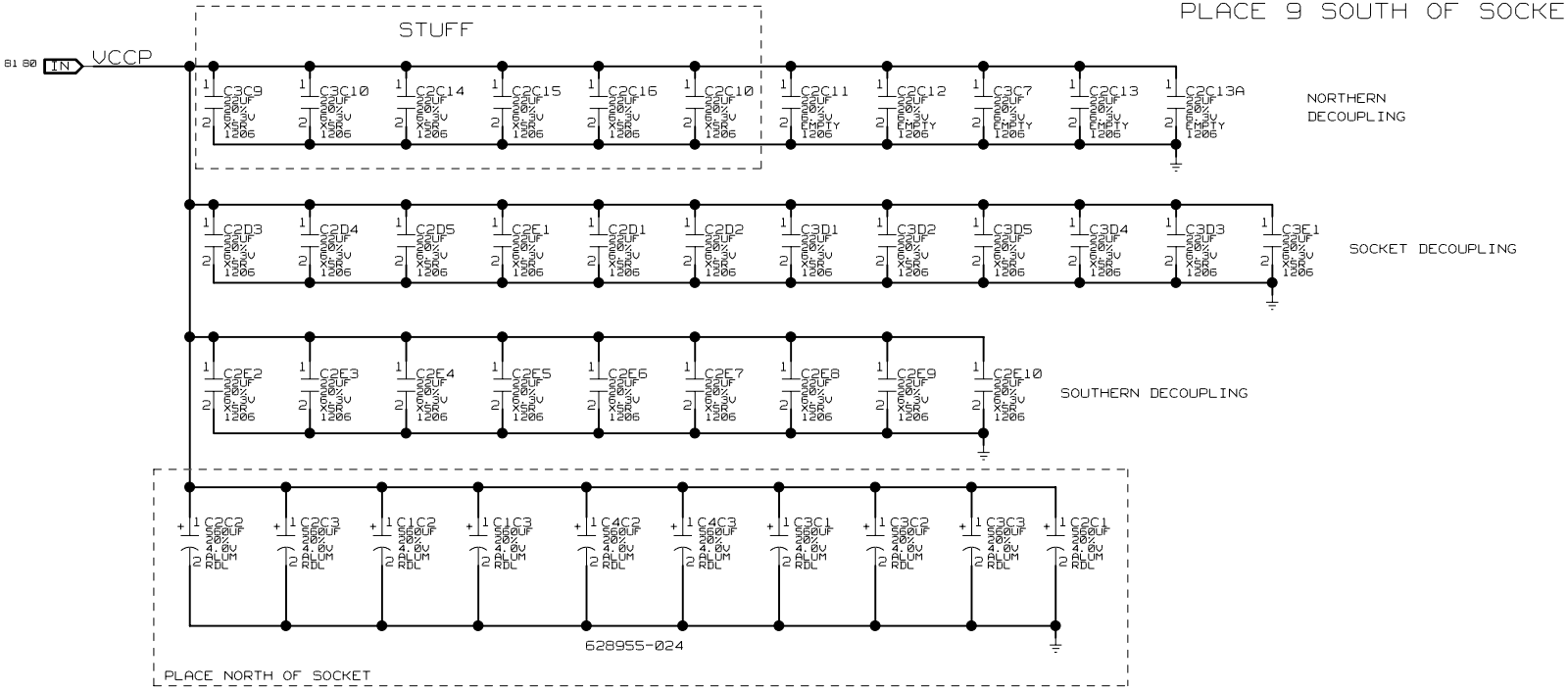
DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: CPU VREG		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:54 2003	SHEET: 81

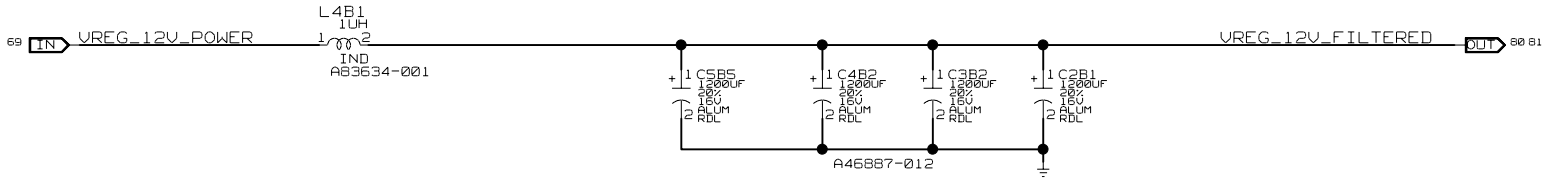
CR-82

CAD NOTE: PLACE AS MANY 1206 CAPACITORS AS POSSIBLE WITHIN CPU CAVITY

PLACEMENT NOTE FOR 1206:
PLACE 11 NORTH OF SOCKET (STUFF 6)
PLACE 12 INSIDE CPU SOCKET (STUFF ALL)
PLACE 9 SOUTH OF SOCKET (UNSTUFF ALL)



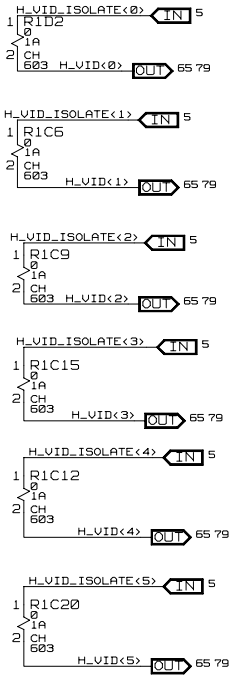
MODFILED TO -027 UNTIL SPEC AND MODEL AVAILABLE



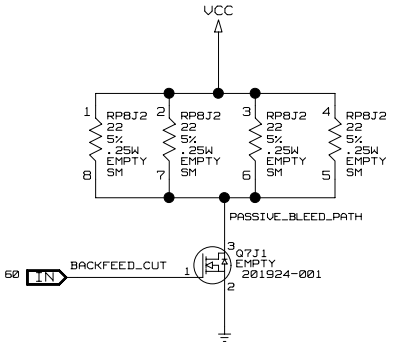
SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: CPU DECOUPLING		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:54 2003	SHEET: 82

DRAWING

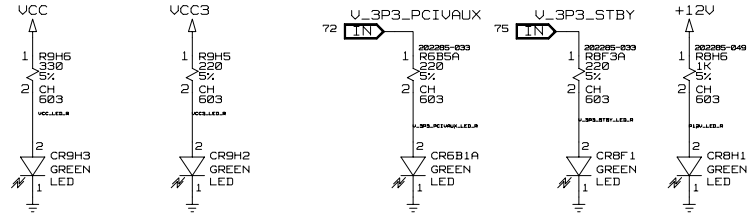
VID JUMPER RESISTORS



PASSIVE BLEED CIRCUIT



POWER RAIL STATUS LED'S

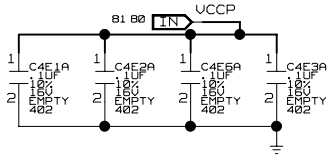


DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: PASSIVE BLEED CRKT/STATUS LEDS/FRNT PANEL SWITCHES/VID JMPRS		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:55 2003	SHEET: 83

CR-84

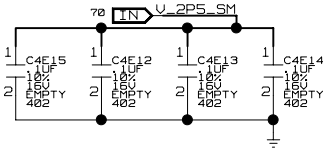
402



(G)MCH CUB DECOUPLING

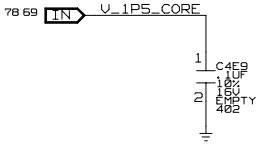
(G)MCH BACK DECOUPLING

402



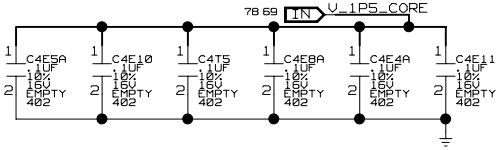
(G)MCH CUB DECOUPLING

402



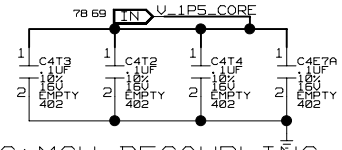
(G)MCH CUB DECOUPLING

402



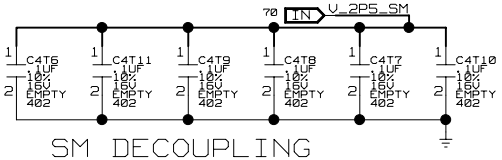
(G)MCH CUB DECOUPLING

402



(G)MCH DECOUPLING

402



SM DECOUPLING

DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: BACKSIDE CAPS		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:56 2003	SHEET: 84

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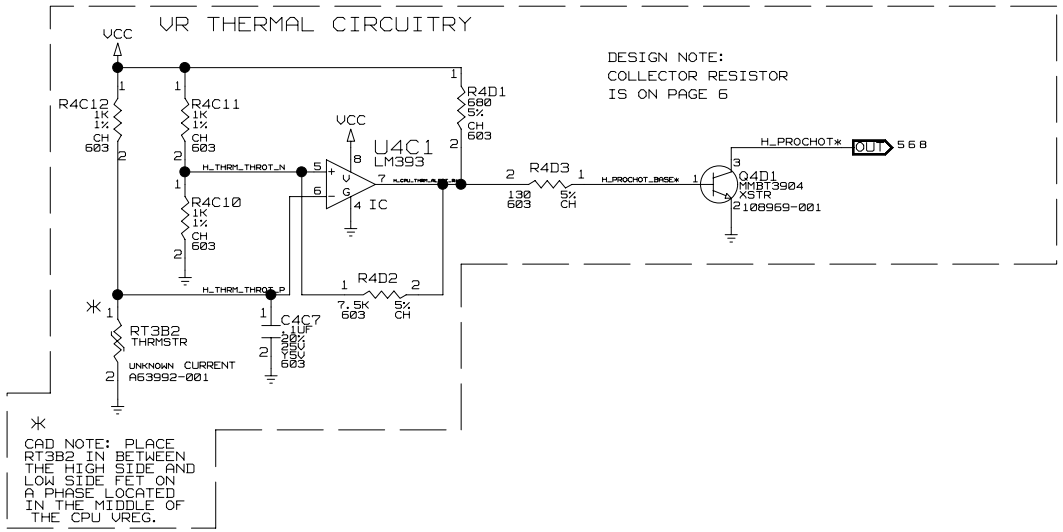
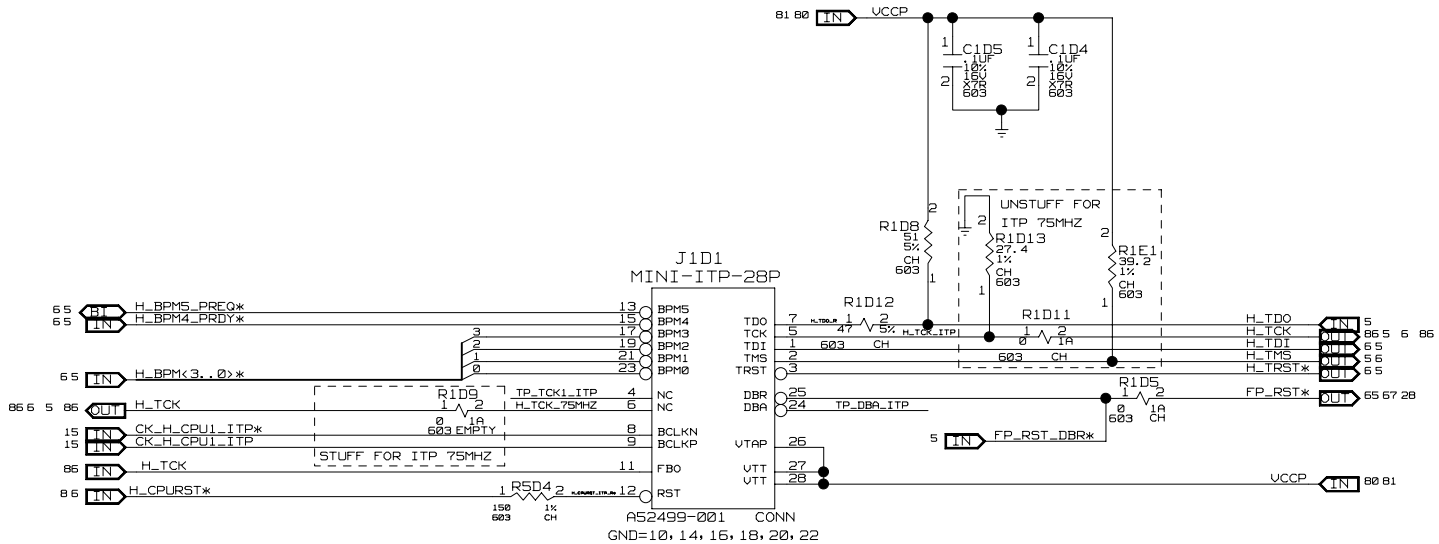


DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: VR THERMAL CIRCUITRY		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:56 2003	SHEET: 85

ITP/DPFLEX CONNECTOR



DESIGN NOTE:

INCLUDES STUFFING OPTIONS FOR 75MHZ ITP.

CAD NOTE:

ROUTE H_TCK FROM THE TCK PIN OF THE CONNECTOR TO THE PROCESSOR PIN.
FBO TAPS INTO THE H_TCK SIGNAL (CLOSE TO THE TCK PIN OF THE CONNECTOR).
SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS.

DRAWING

SCHEMATIC TITLE: INTEL(R) 865G/865PE/865P CHIPSET REFERENCE BOARD		
PAGE TITLE: ITP		REV:
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue May 06 11:25:57 2003	SHEET: 86