



# Intel<sup>®</sup> 848P Chipset Customer Reference Board Schematics

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*For use with the Intel<sup>®</sup> 848P Chipset Platform Design Guide*

*September 2003*



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## Revision History

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Rev. No.	Description	Rev. Date
-001	Initial Release.	August 2003
-002	<ul style="list-style-type: none"><li>Renamed pins labeled TestPxxx to final pin name</li><li>Changes to test points TestP2 &amp; TestP3</li></ul>	September 2003

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# INTEL(R) 848P CHIPSET CUSTOMER REFERENCE SCHEMATICS

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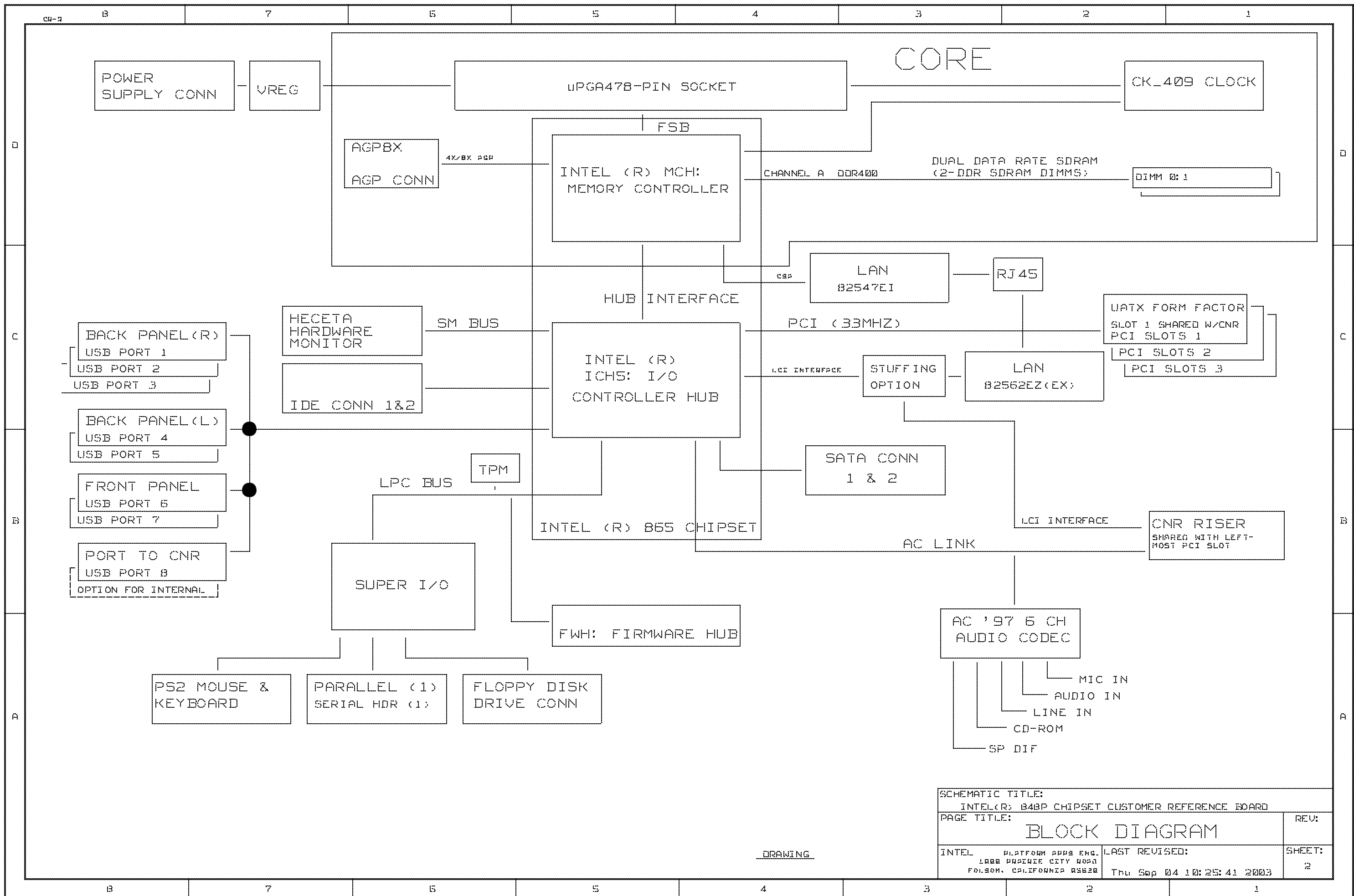
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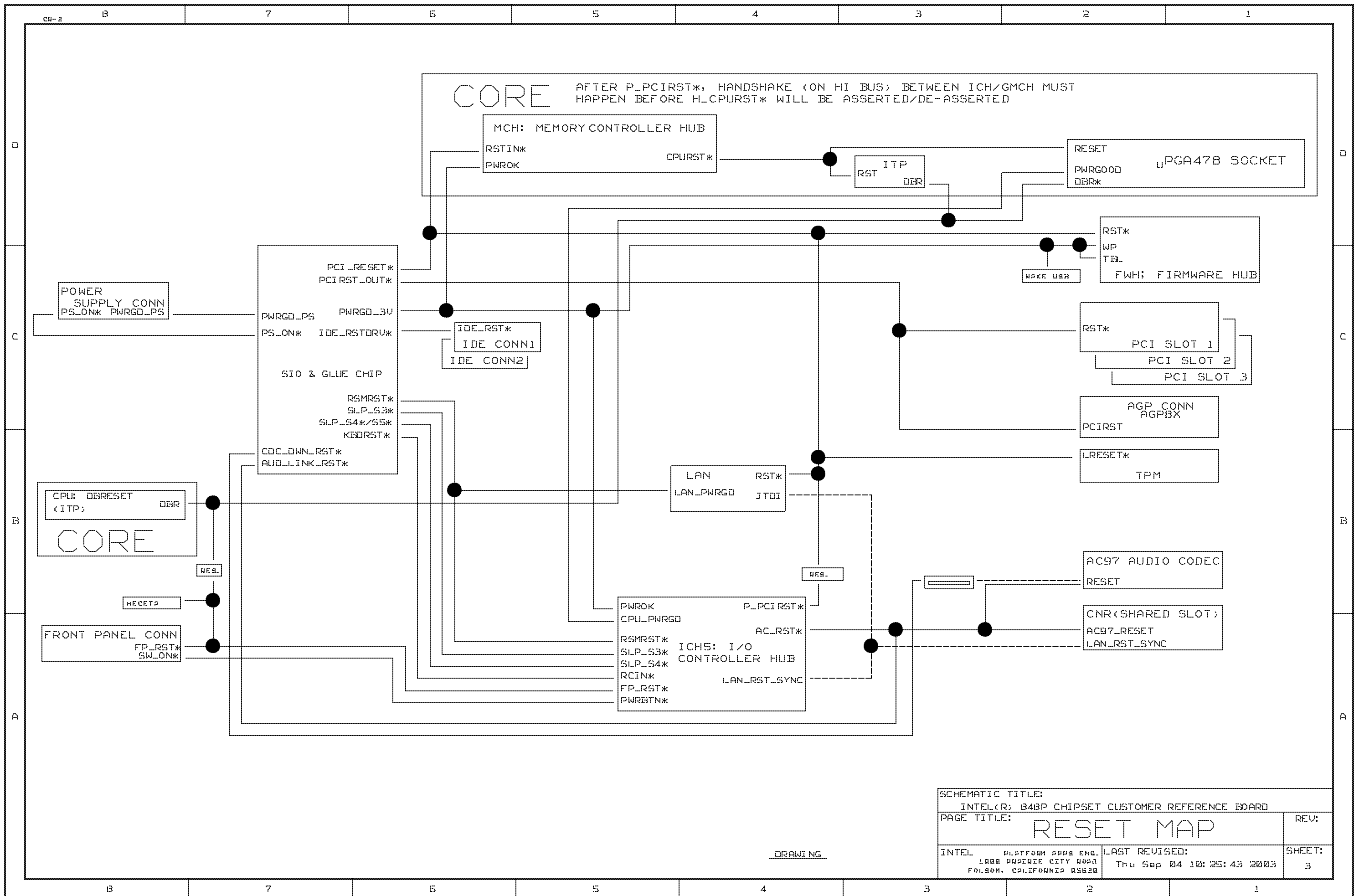
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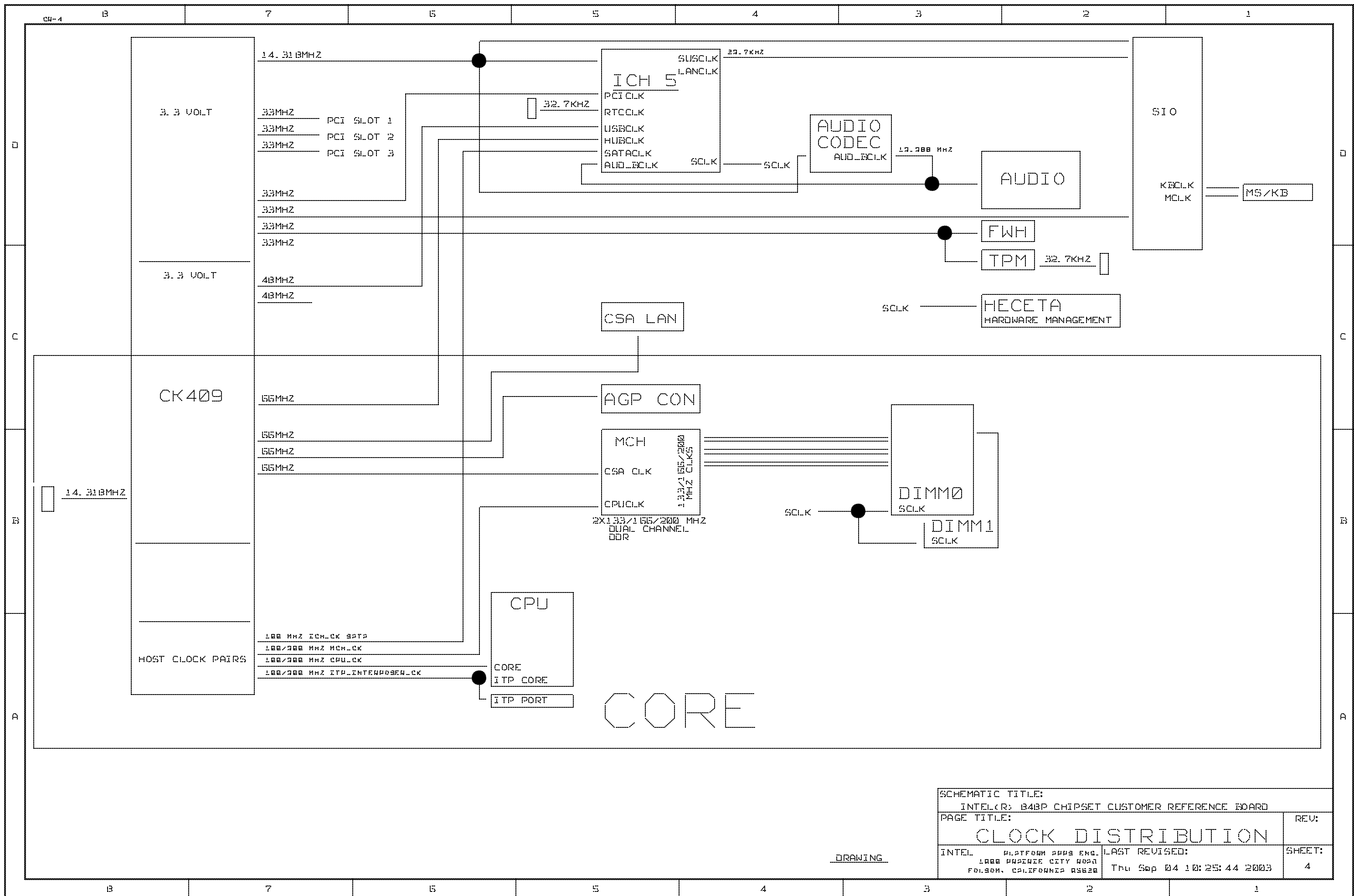
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PAGE TITLE:		RESET MAP	
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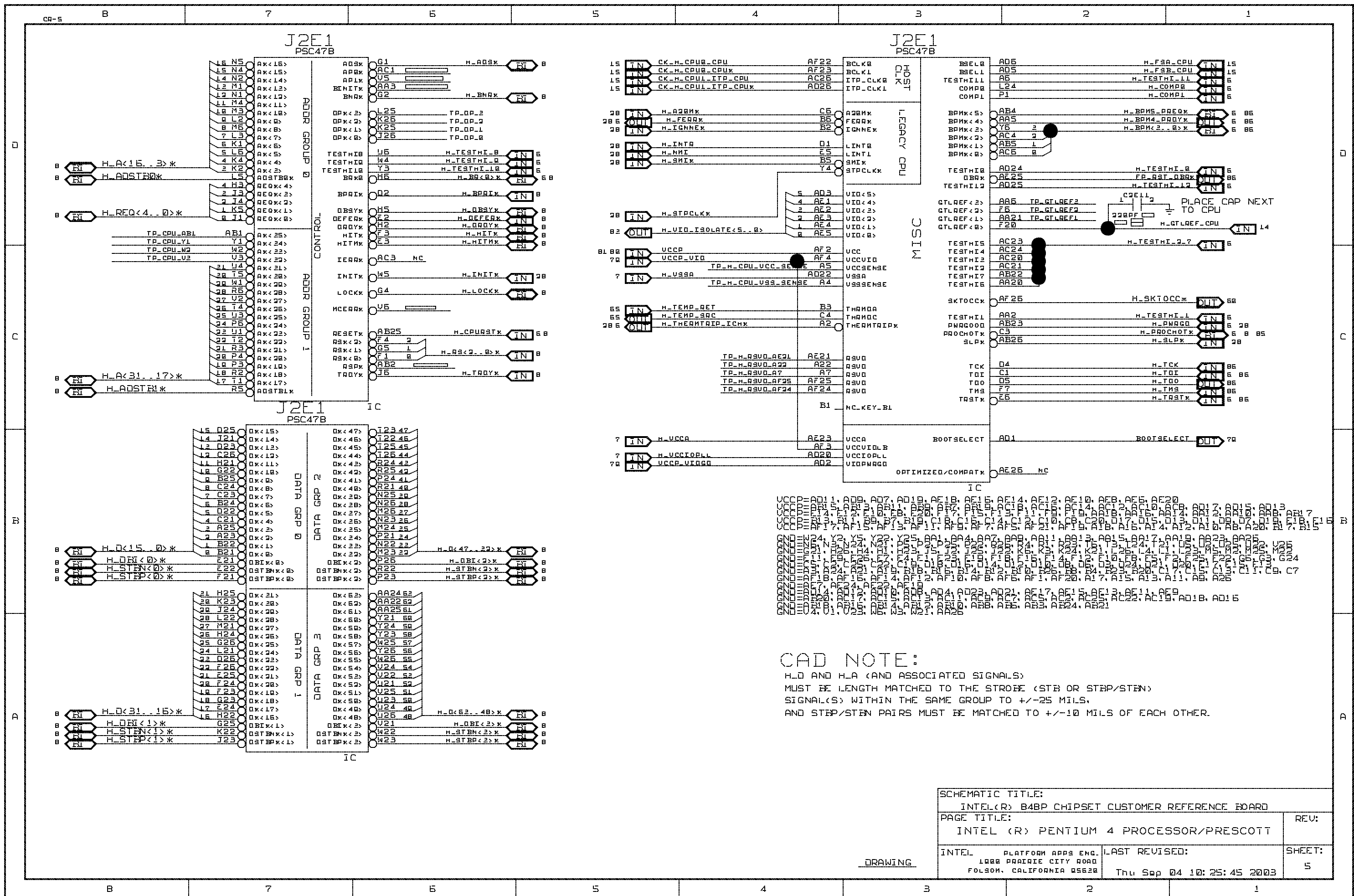


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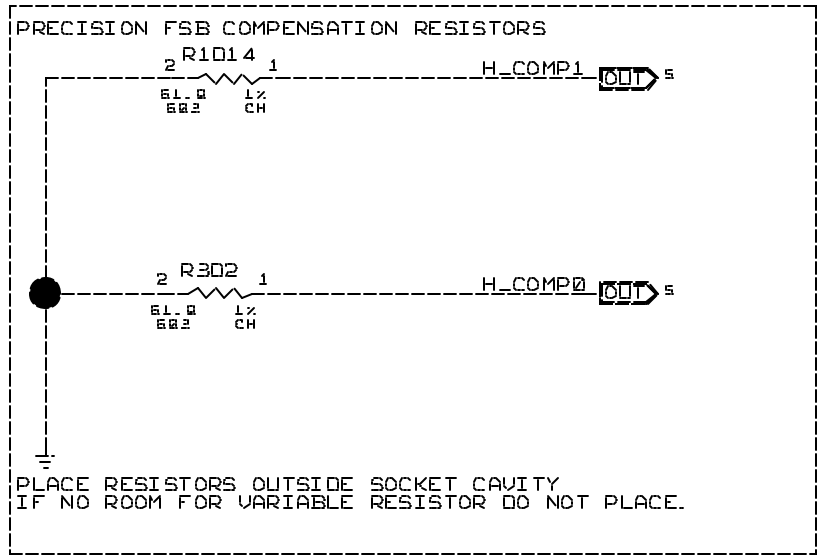
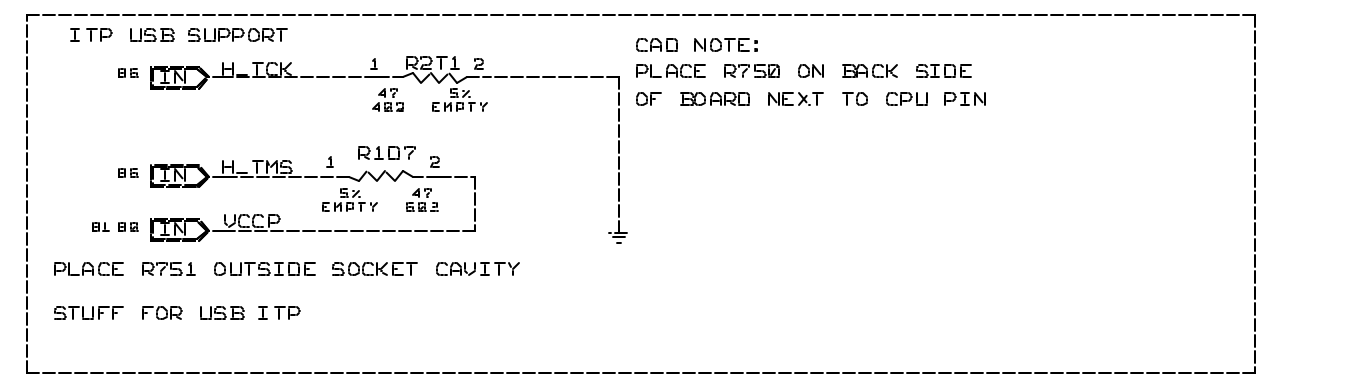
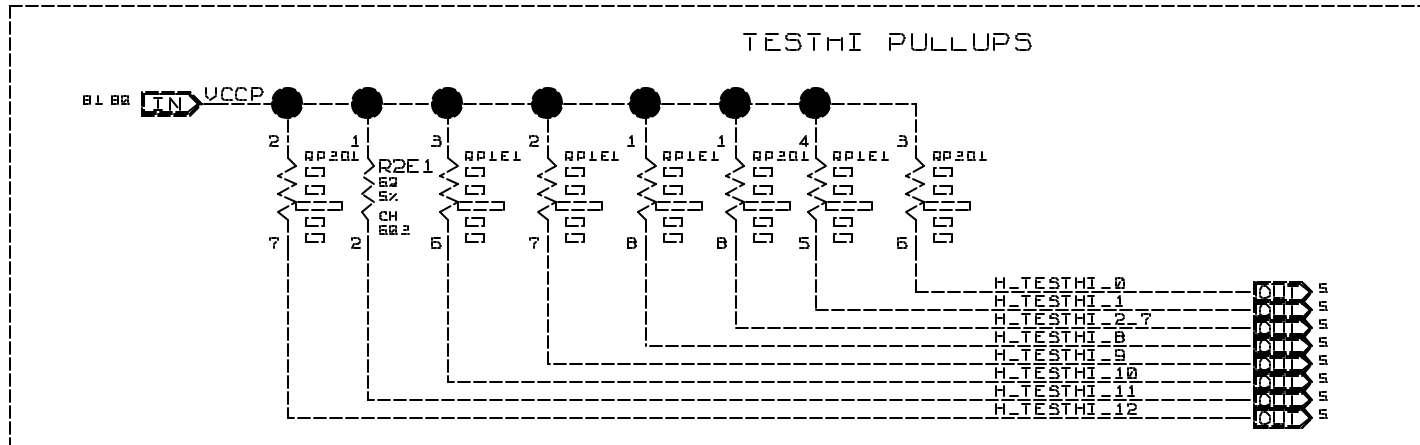
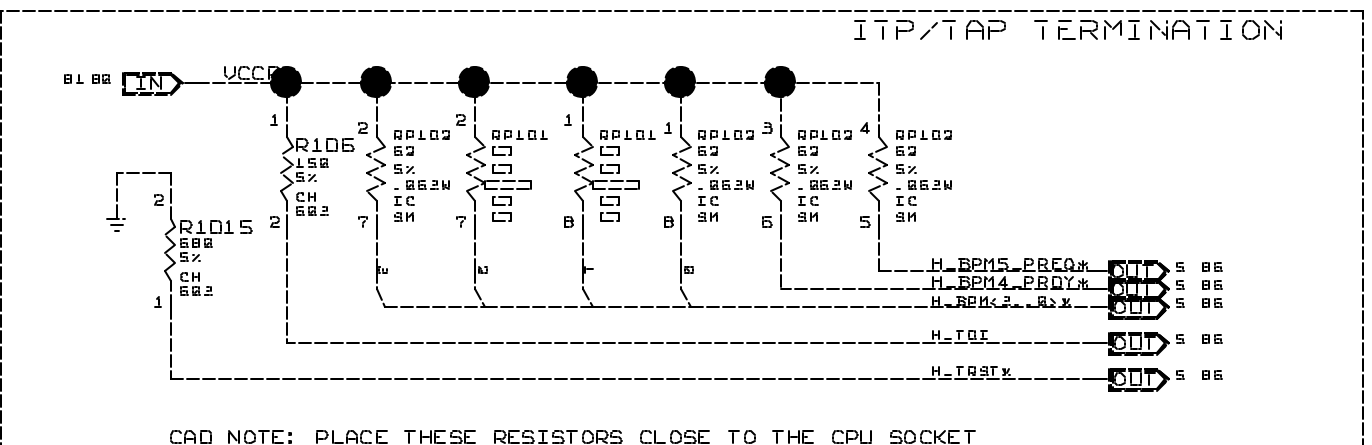
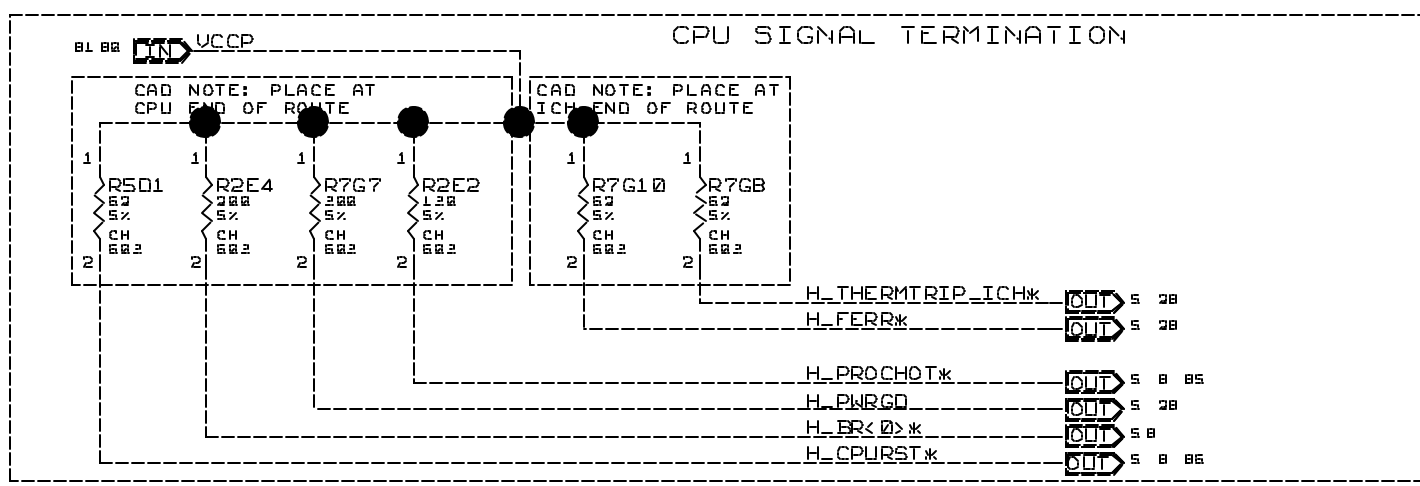
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CORE





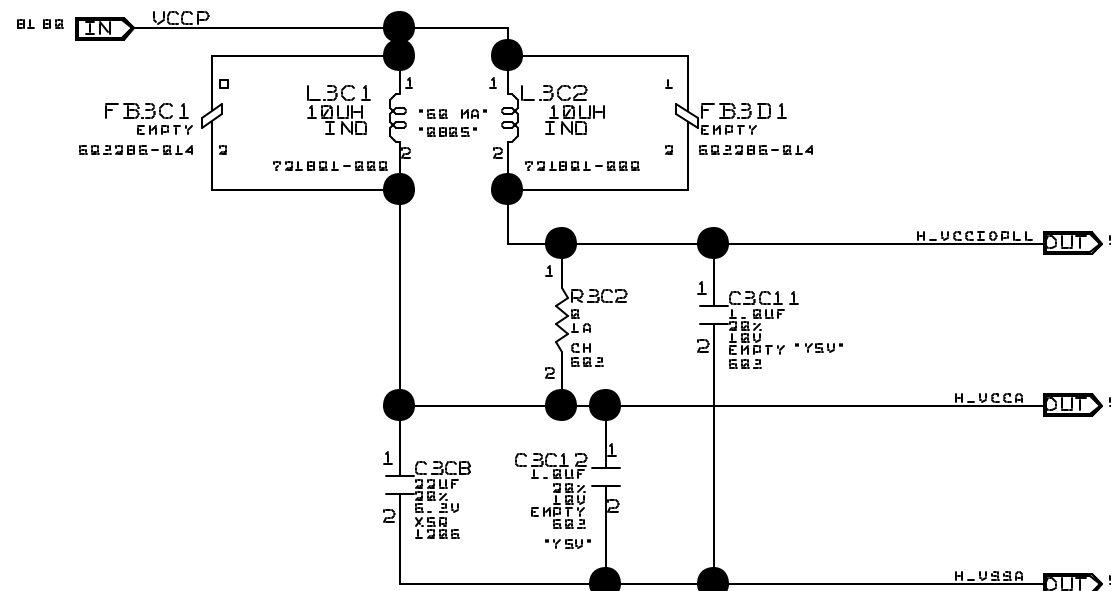
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PAGE TITLE:		CPU PULLUPS/PULLDOWNS/TERMINATION	
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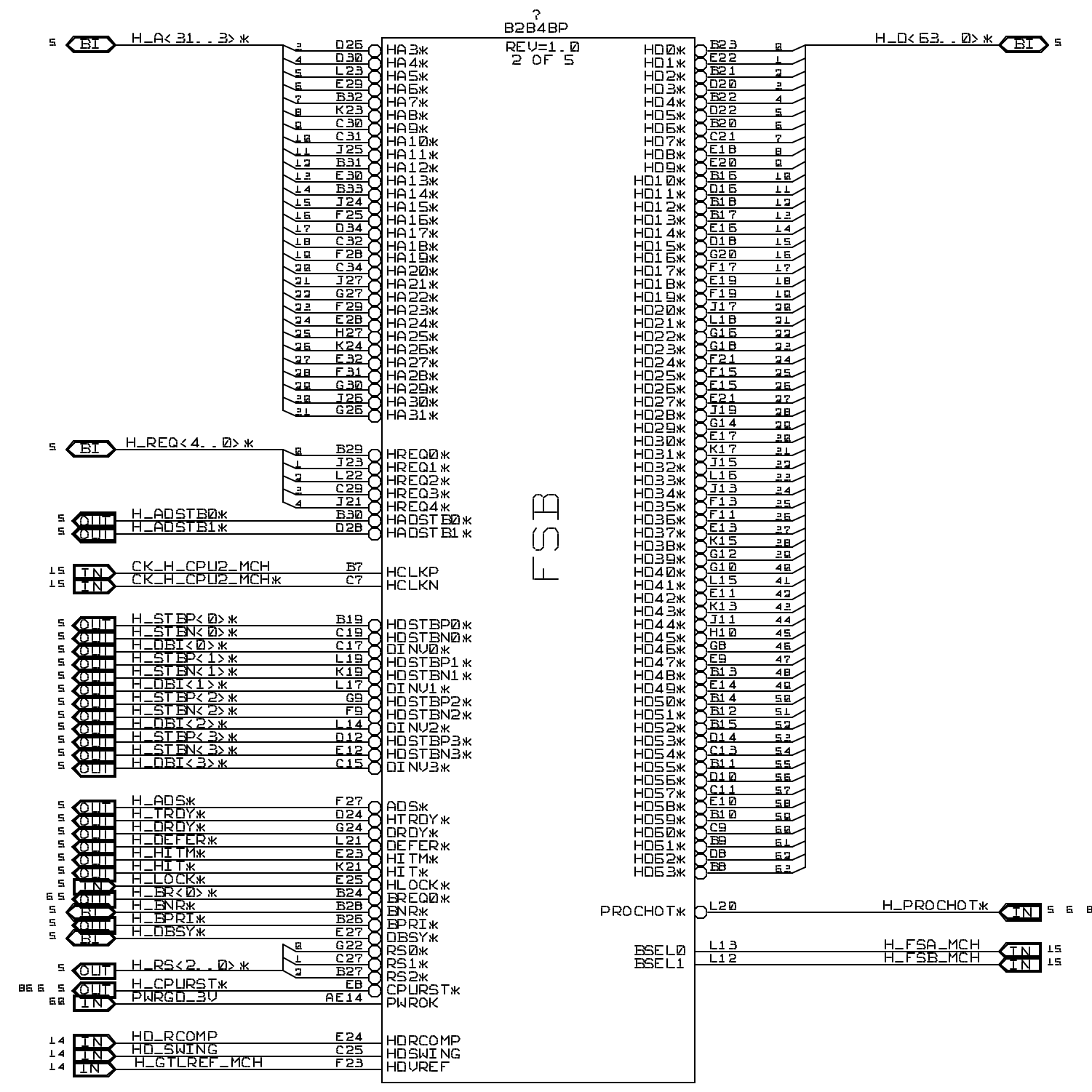
# PLL SUPPLY FILTER



CAD NOTE:  
 PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET  
 TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MIL

DRAWING

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
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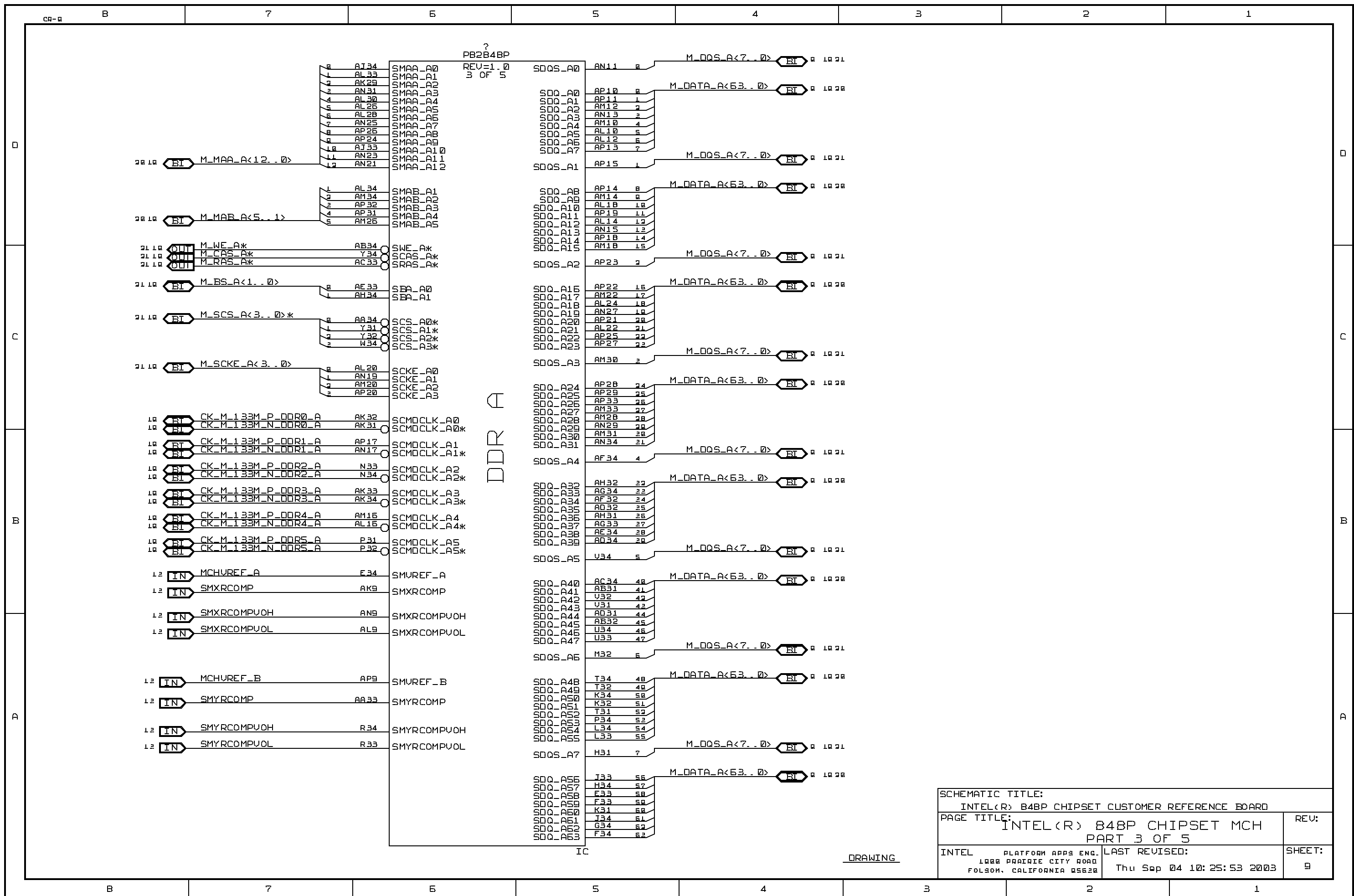


FSB

IC

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		PART 2 OF 5	
INTEL	PLATFORM APPS ENG.	LAST REVISED:	SHEET:
1000 PRAIRIE CITY ROAD		Thu Sep 04 10:25:51 2003	B
FOLSOM, CALIFORNIA 95630			



?  
PB2B4BP  
REV=1.0  
3 OF 5

DDR A

IC

DRAWING

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: INTEL(R) B4BP CHIPSET MCH PART 3 OF 5		SHEET: 9
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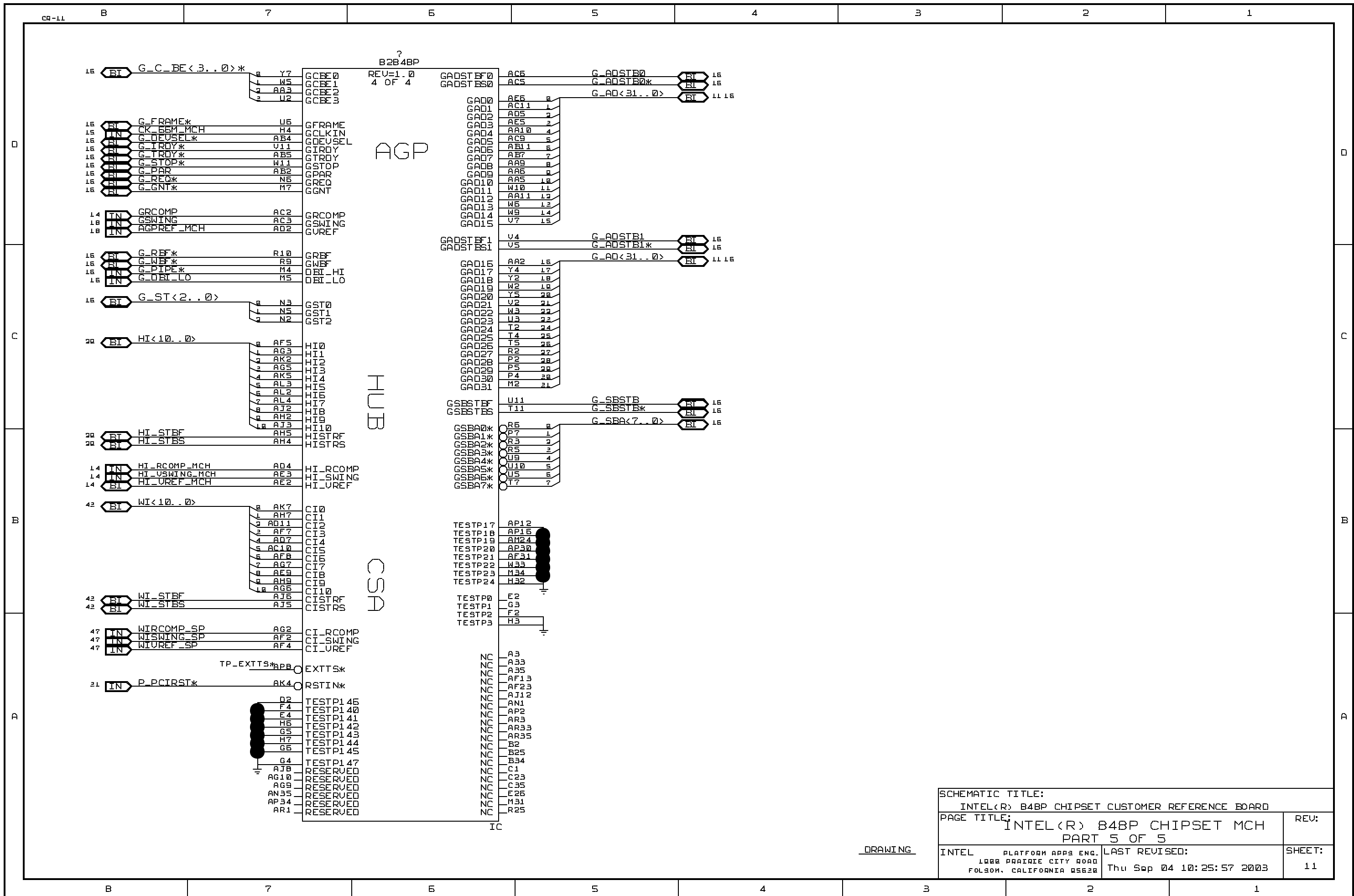
?  
B2B4BP

AG31	TESTP46	REV=1.0	TESTP128	AF15
AJ31	TESTP47	4 OF 5	TESTP4	AG11
AD27	TESTP48			
AE24	TESTP49		TESTP64	AJ10
AK27	TESTP50		TESTP65	AE15
AG25	TESTP51		TESTP66	AL11
AL25	TESTP52		TESTP67	AE16
AF21	TESTP53		TESTP68	AL8
AL23	TESTP54		TESTP69	AF12
AJ22	TESTP55		TESTP70	AK11
AF29	TESTP56		TESTP71	AG12
AL21	TESTP57			
AJ20	TESTP58		TESTP129	AG13
			TESTP5	AG15
AE27	TESTP12		TESTP72	AE17
AD26	TESTP13		TESTP73	AL13
AL29	TESTP14		TESTP74	AK17
AL27	TESTP15		TESTP75	AL17
AE23	TESTP16		TESTP76	AK13
			TESTP77	AJ14
			TESTP78	AJ16
			TESTP79	AJ18
W27	TESTP63			
W31	TESTP62		TESTP130	AG21
W26	TESTP61		TESTP6	AE21
Y25	TESTP59		TESTP80	AE19
AA25	TESTP60		TESTP81	AE20
			TESTP82	AG23
			TESTP83	AK23
U26	TESTP42		TESTP84	AL19
T29	TESTP43		TESTP85	AK21
V25	TESTP44		TESTP86	AJ24
W25	TESTP45		TESTP87	AE22
			TESTP131	AH27
			TESTP7	AJ28
AK19	TESTP136			
AF19	TESTP137		TESTP88	AK25
AG19	TESTP138		TESTP89	AH26
AE18	TESTP139		TESTP90	AG27
			TESTP91	AF27
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AG30	TESTP35		TESTP93	AJ27
			TESTP94	AD25
AF17	TESTP31		TESTP95	AF28
AG17	TESTP37			
			TESTP132	AD29
N27	TESTP32		TESTP8	AC31
N26	TESTP38			
			TESTP96	AE30
AJ30	TESTP33		TESTP97	AC27
AH29	TESTP39		TESTP98	AC30
			TESTP99	Y29
AK15	TESTP34		TESTP100	AE31
AL15	TESTP40		TESTP101	AB29
			TESTP102	AA26
N31	TESTP35		TESTP103	AA27
N30	TESTP41			
			TESTP133	U30
			TESTP9	U31
			TESTP104	AA30
			TESTP105	W30
			TESTP106	U27
			TESTP107	T25
			TESTP108	AA31
			TESTP109	V29
			TESTP110	U25
			TESTP111	R27
			TESTP134	L27
			TESTP10	M29
			TESTP112	P29
			TESTP113	R30
			TESTP114	K28
			TESTP115	L30
			TESTP116	R31
			TESTP117	R26
			TESTP118	P25
			TESTP119	L32
			TESTP135	J30
			TESTP11	J31
			TESTP120	K30
			TESTP121	H29
			TESTP122	F32
			TESTP123	G33
			TESTP124	N25
			TESTP125	M25
			TESTP126	J29
			TESTP127	G32

MCH

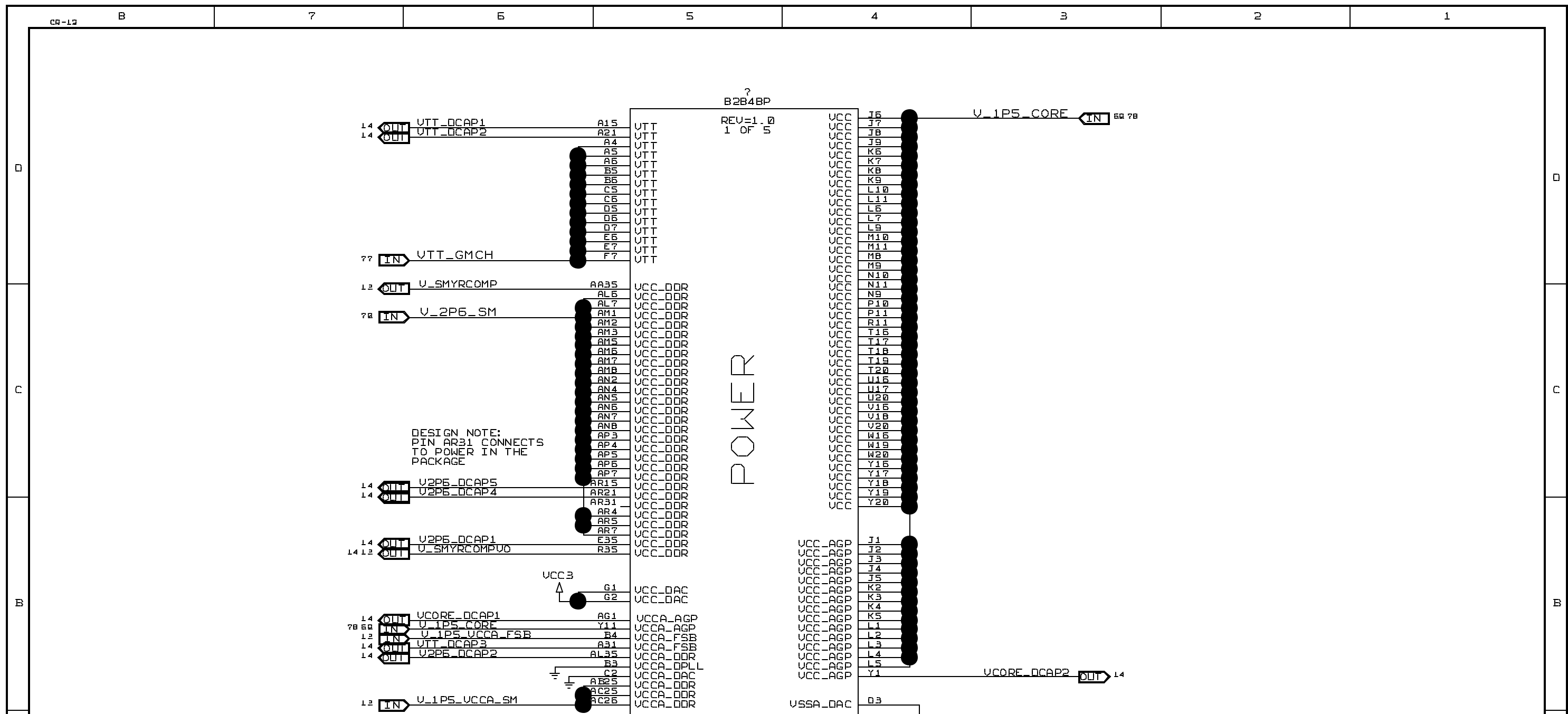
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INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: Thu Sep 04 10:25:57 2003	SHEET: 11

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DESIGN NOTE:  
PIN AR31 CONNECTS  
TO POWER IN THE  
PACKAGE

POWER

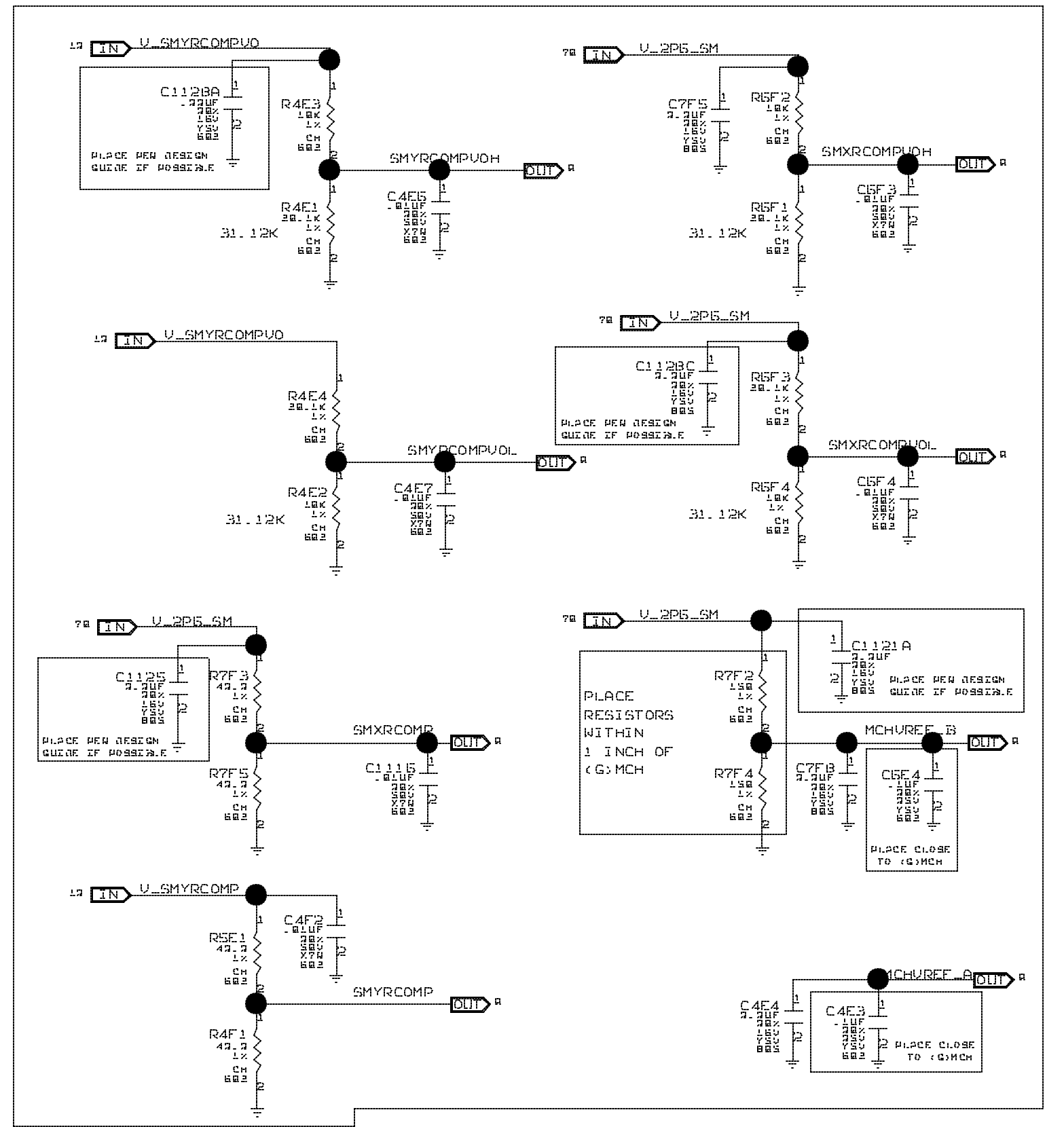
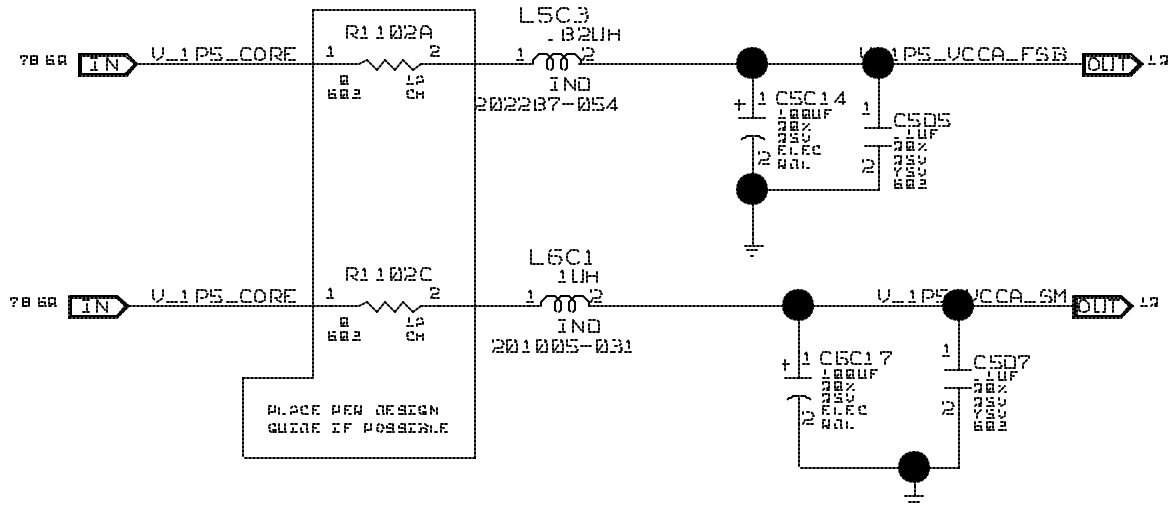
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SCHEMATIC TITLE: INTEL(R) B48P CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: INTEL(R) B48P CHIPSET MCH		SHEET:
PART 1 OF 5		12
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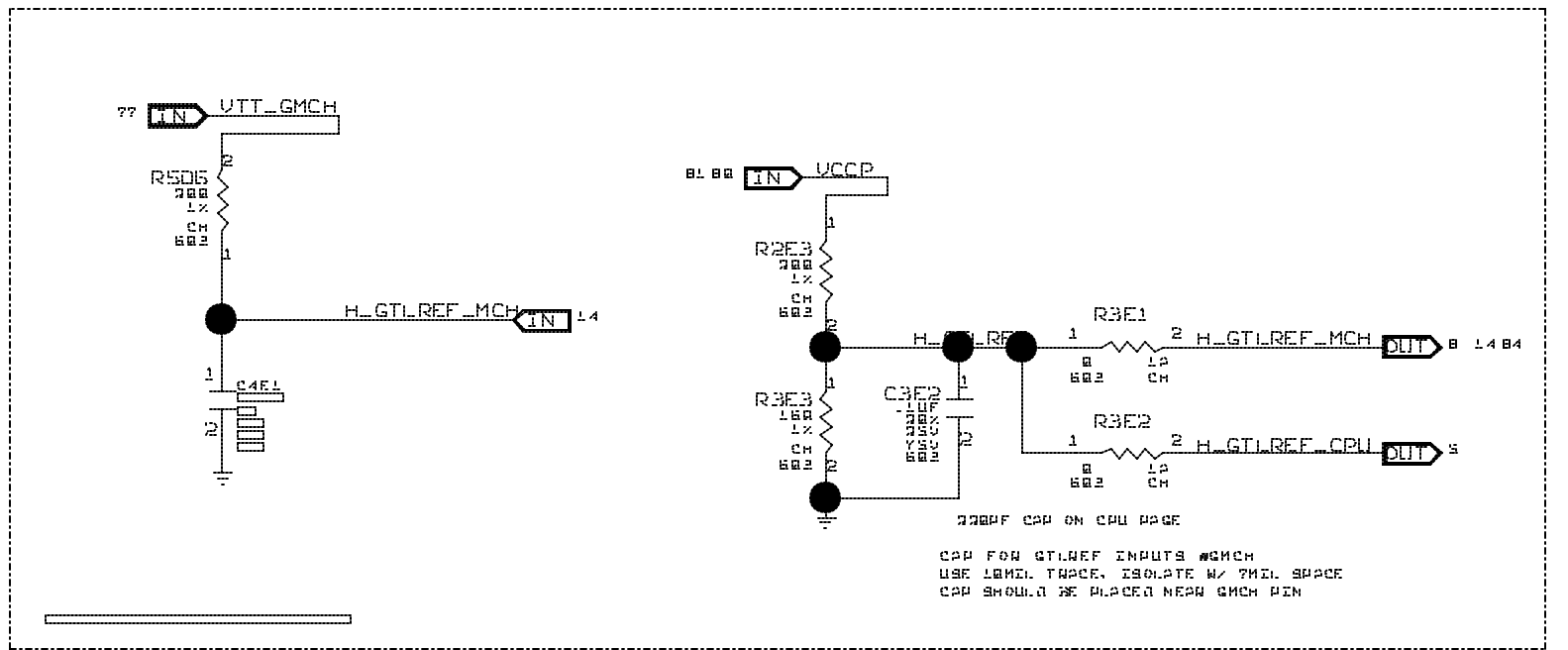
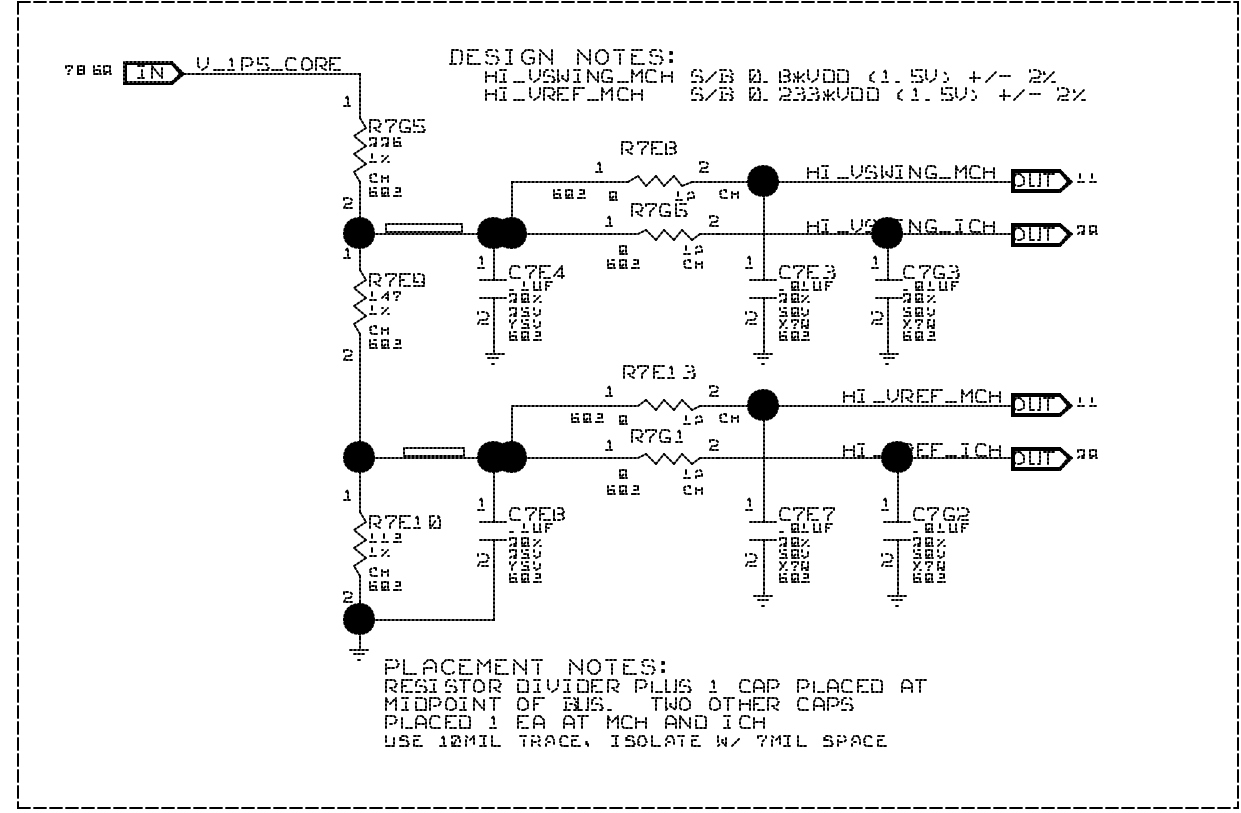
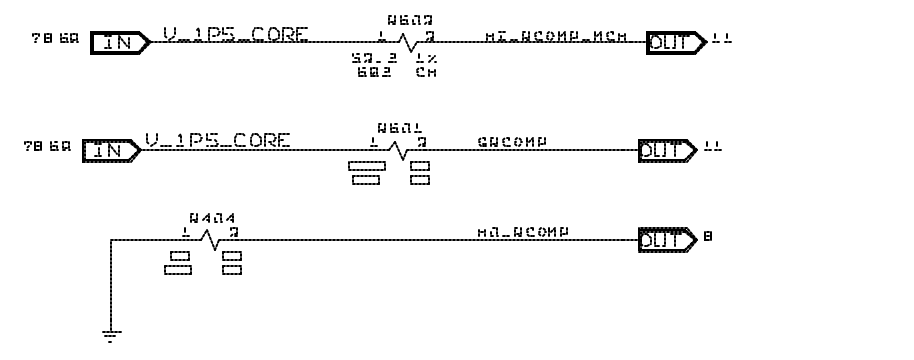
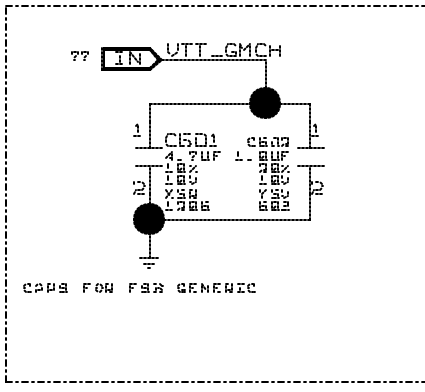
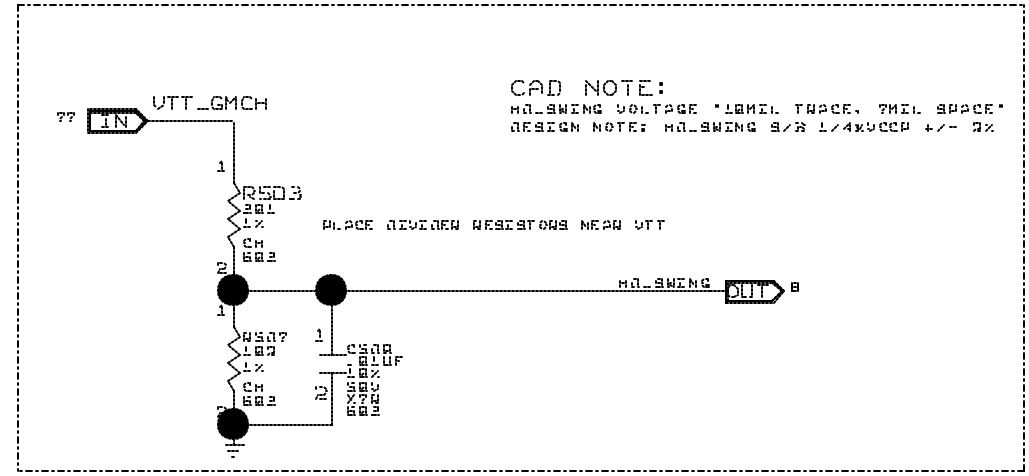
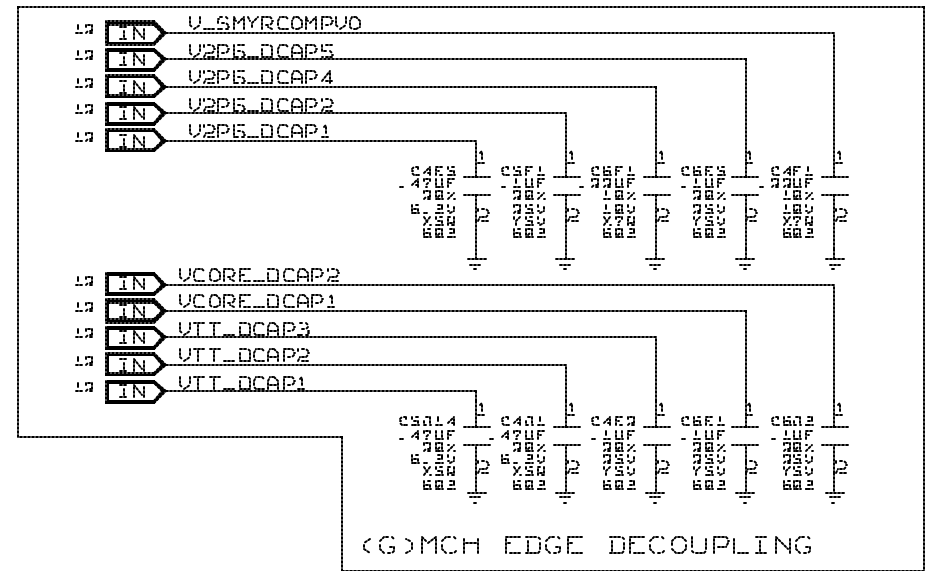
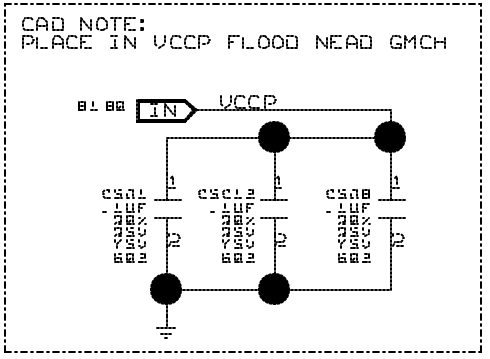
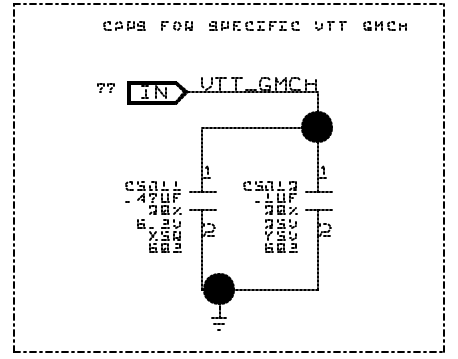
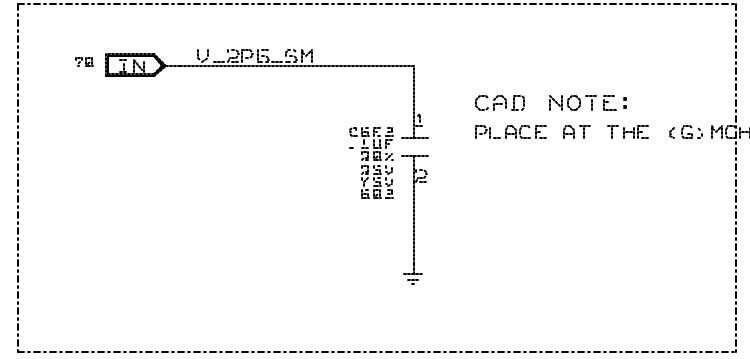


ANALOG FILTERS



SCHEMATIC TITLE: INTEL(R) B48P CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: <b>CHIPSET FILTERS</b>		SHEET:
INTEL PLATFORM APPS ENG. 1800 MANLINE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:25:01 2003	13

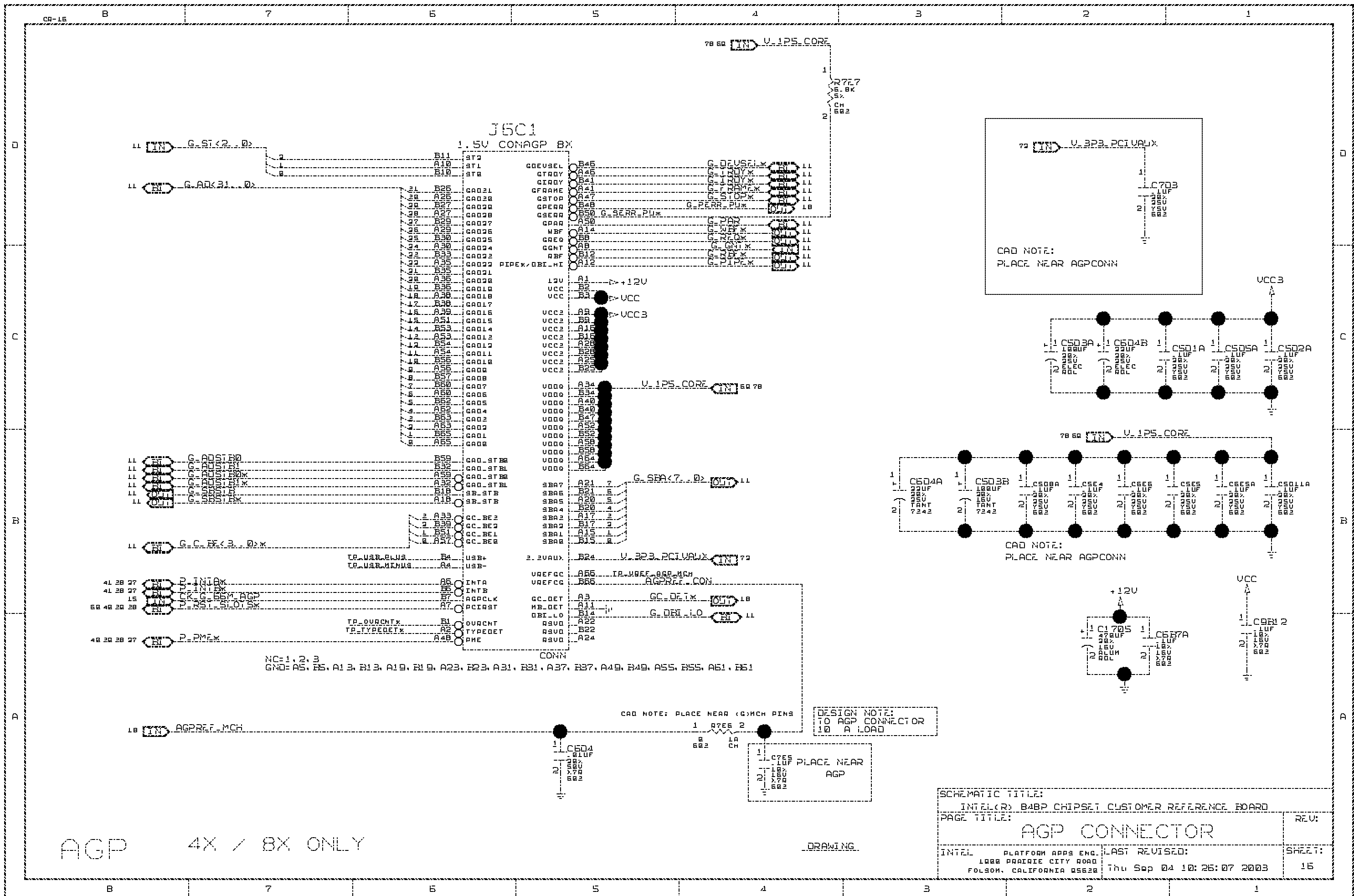
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SCHEMATIC TITLE: INTEL(R) 848P CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: <b>CHIPSET DECOUPLING</b>		SHEET: 14_A
INTEL PLATFORM APPS ENG. 1800 MANHATTAN CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:25:03 2003	

DRAWING





J5C1

1.5V CONAGP BX

CAD NOTE:  
PLACE NEAR AGPCONN

CAD NOTE:  
PLACE NEAR AGPCONN

DESIGN NOTE:  
TO AGP CONNECTOR  
10 A LOAD

AGP 4X / 8X ONLY

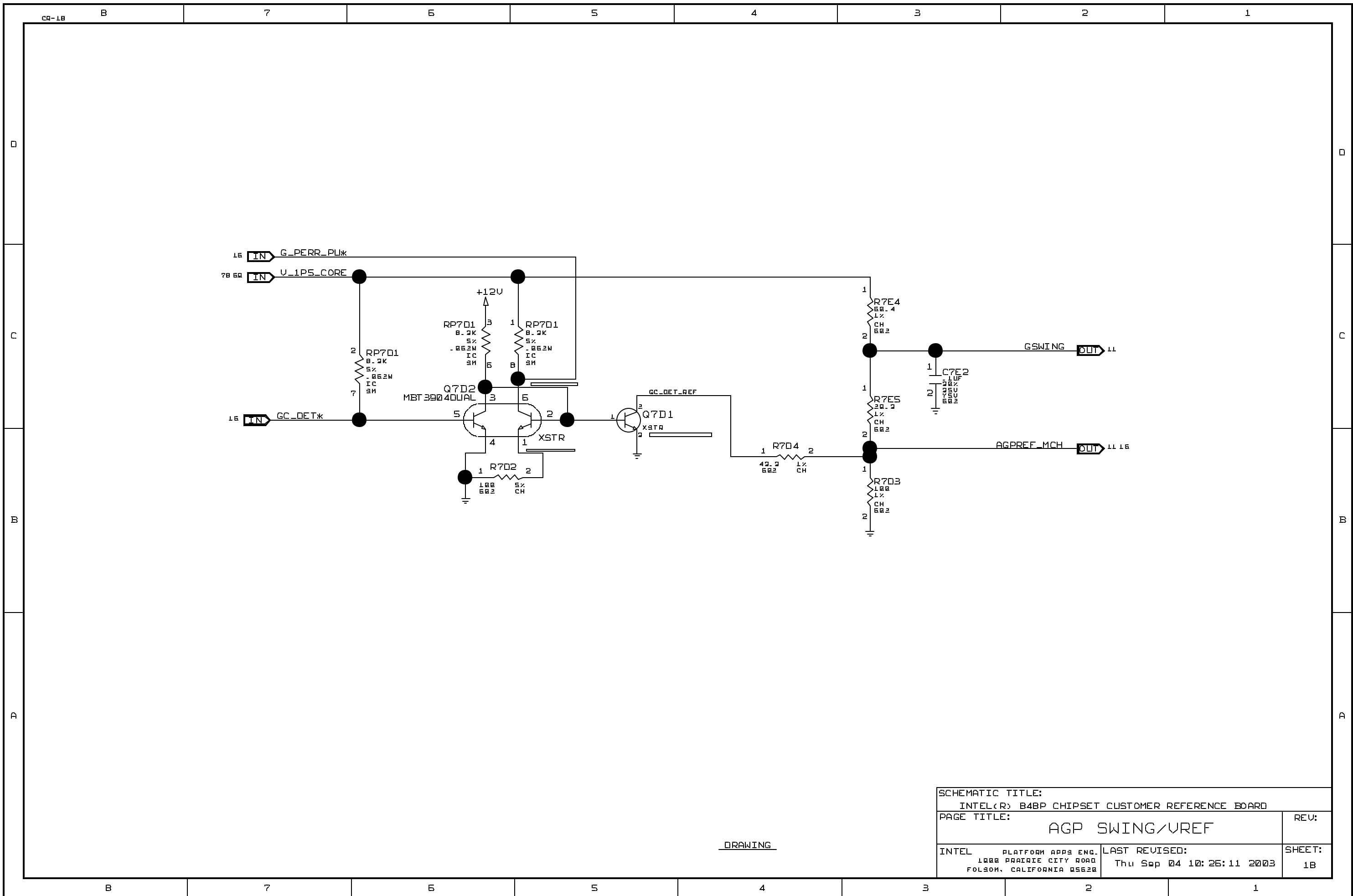
SCHEMATIC TITLE:		INTEL(R) BABP CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:		AGP CONNECTOR
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: Thu Sep 04 10:26:07 2003
SHEET:		15

DRAWING

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DRAWING

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:26:09 2003
SHEET: 17	



DRAWING

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: AGP SWING/VREF	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:26:11 2003
SHEET: 1B	



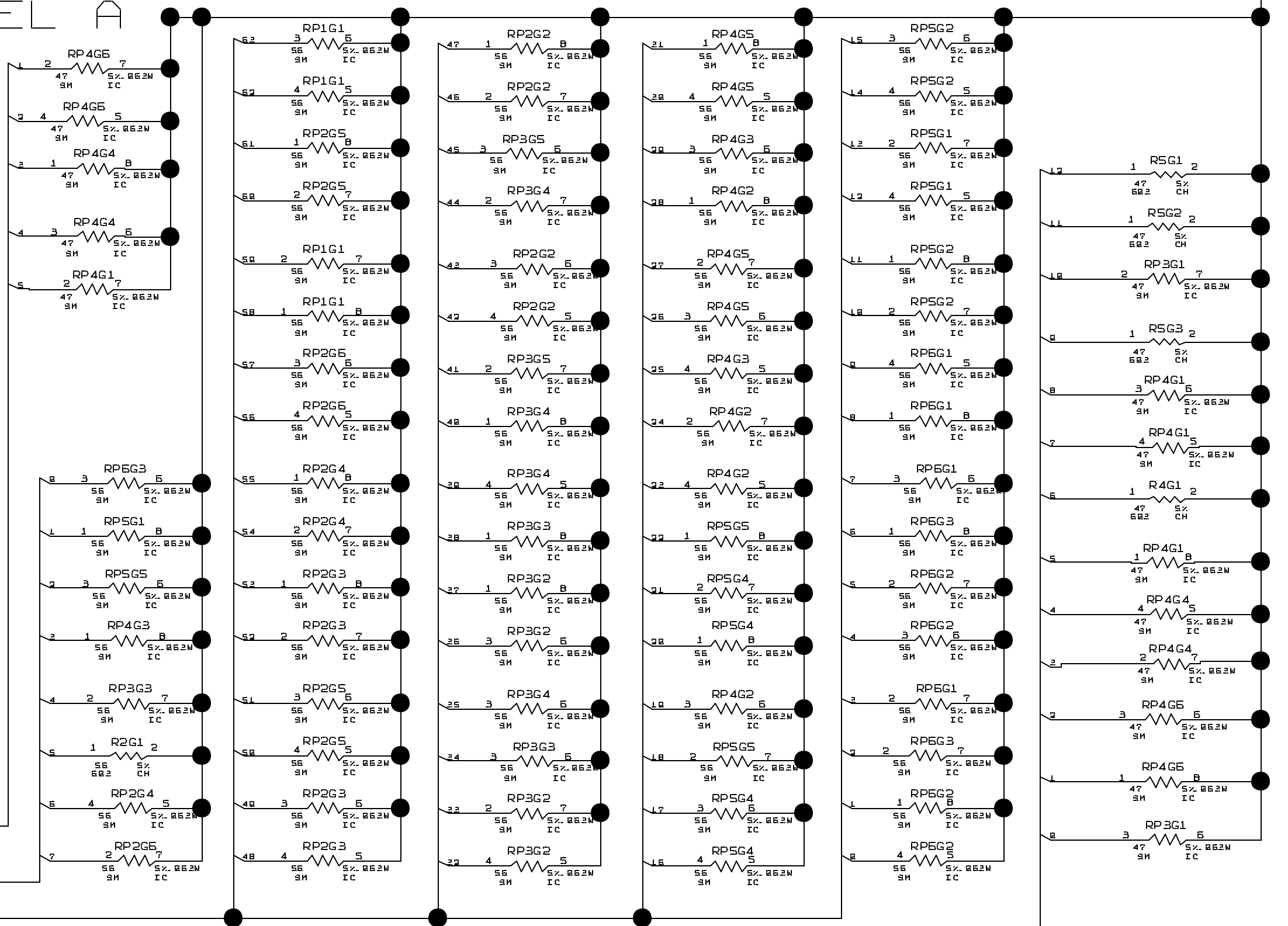
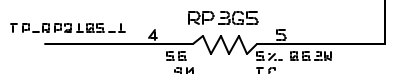
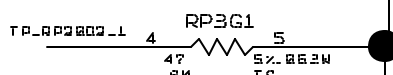
# DDR CHANNEL A

78 IN U\_1P3\_MEMUTT

## SPARE SECTIONS

78 IN U\_1P3\_MEMUTT

## SPARE RPACKS



M\_MAB\_A<5..1>

M\_DQM\_A<7..0>

M\_DATA\_A<63..0>

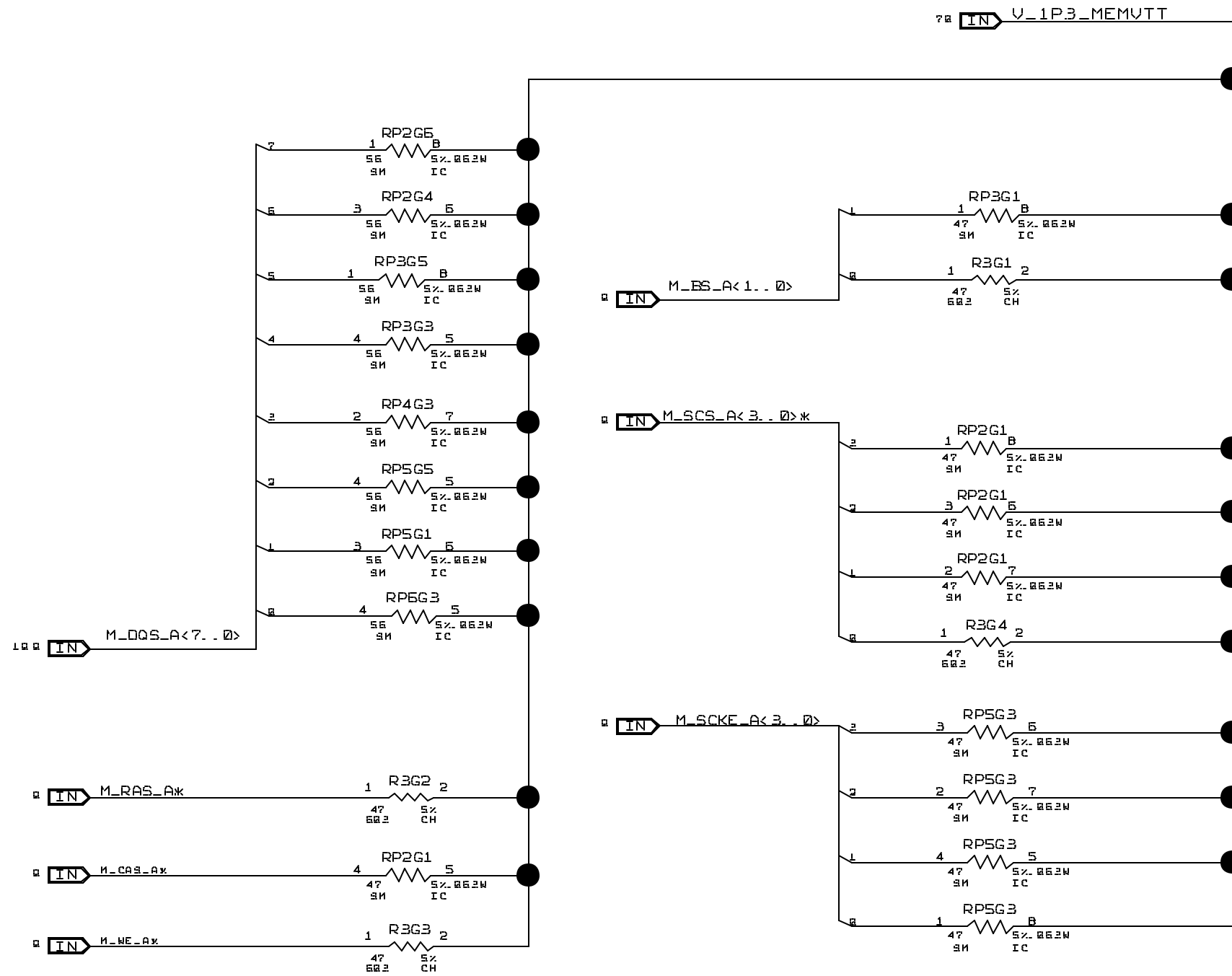
M\_MAA\_A<12..0>

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: DDR RESISTOR TERMINATION		SHEET: 20
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:26:17 2003	

DRAWING



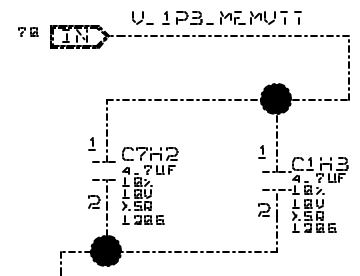
# DDR CHANNEL A



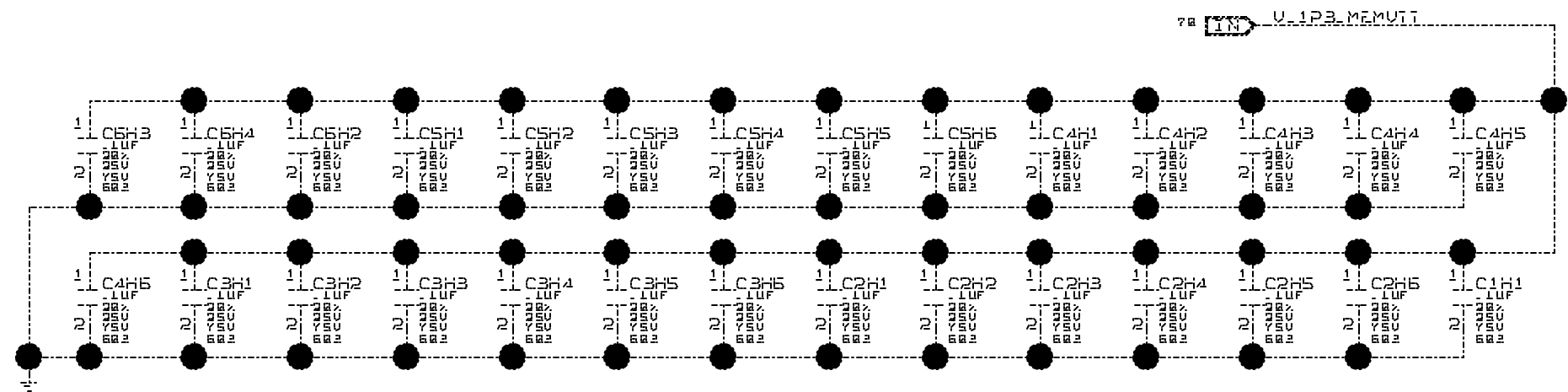
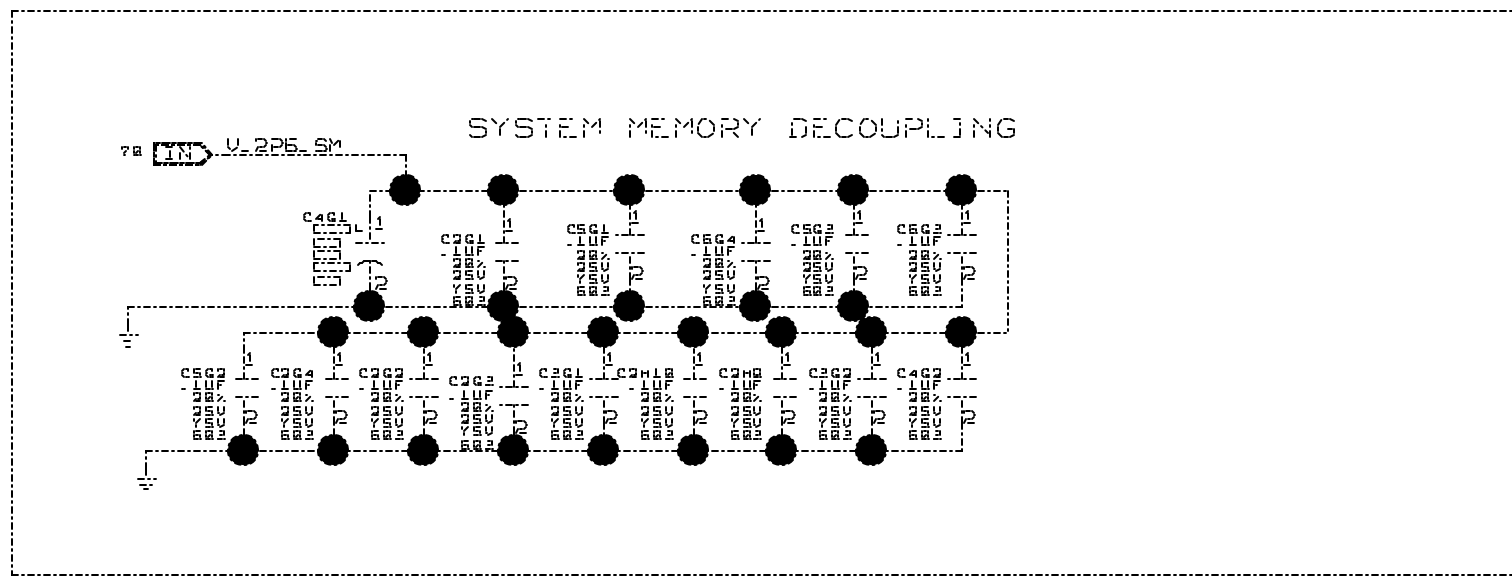
DRAWING

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: DDR RESISTOR TERMINATION		SHEET: 21
INTEL 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:26:19 2003	

# DDR CHANNEL A



PLACED AT LEFT AND RIGHT ENDS OF VTT ISLAND



## DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

SCHEMATIC TITLE:		INTEL(R) BABP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		DECOUPLING CAPACITORS	
DRAWING:		LAST REVISED:	
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620		Thu Sep 04 10:26:21 2003	
REV:	SHEET:	22	

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SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE:		SHEET: 23
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED:	

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SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: SHEET: 24

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SCHEMATIC TITLE:	
INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED:
	SHEET: 25

D

D

C

C

B

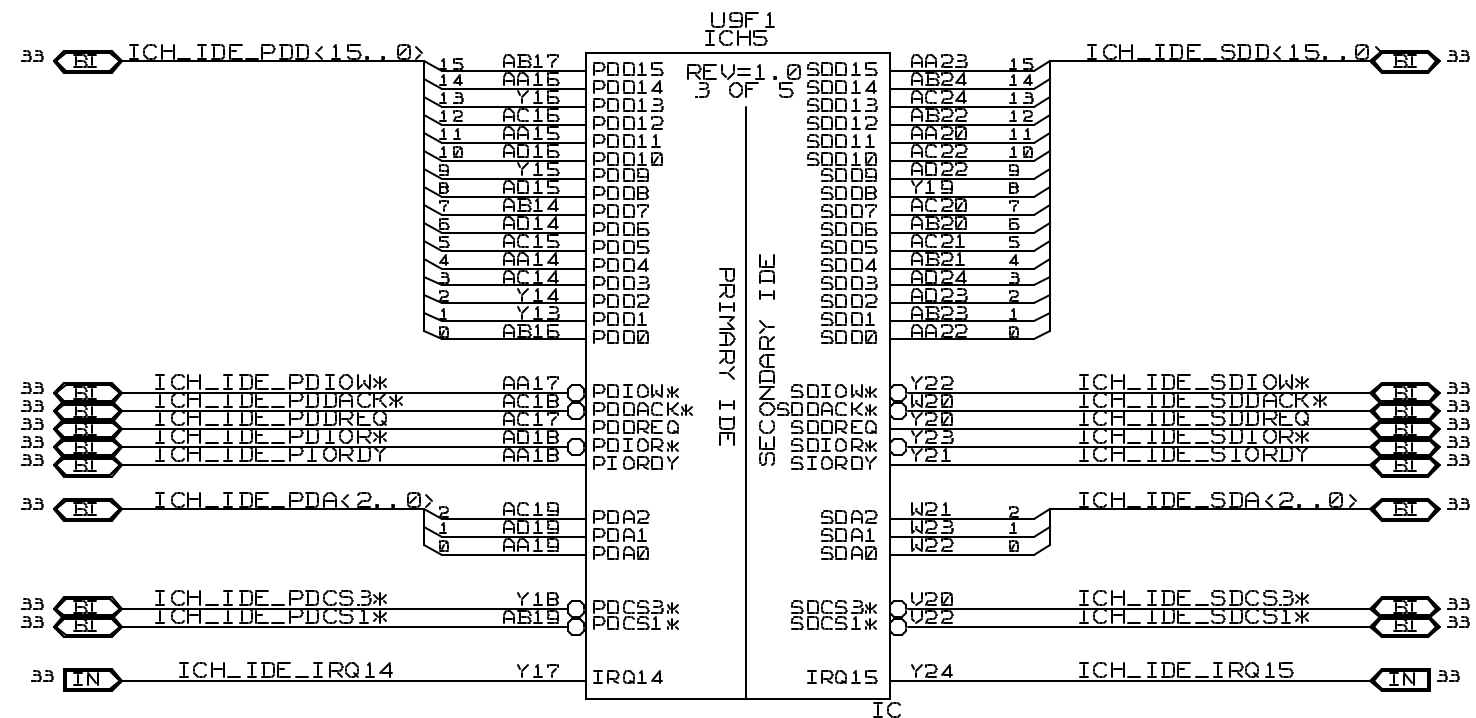
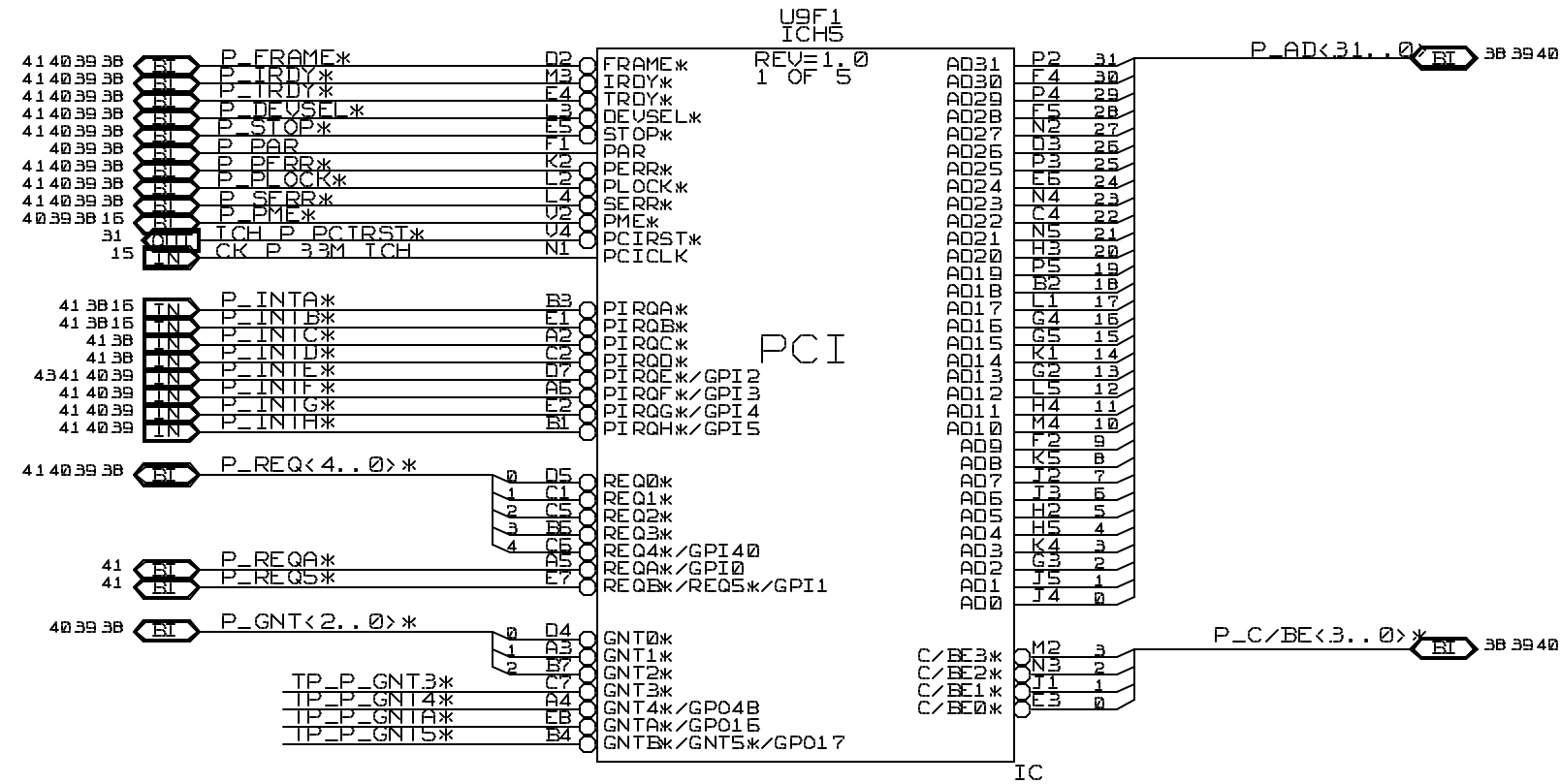
B

A

A

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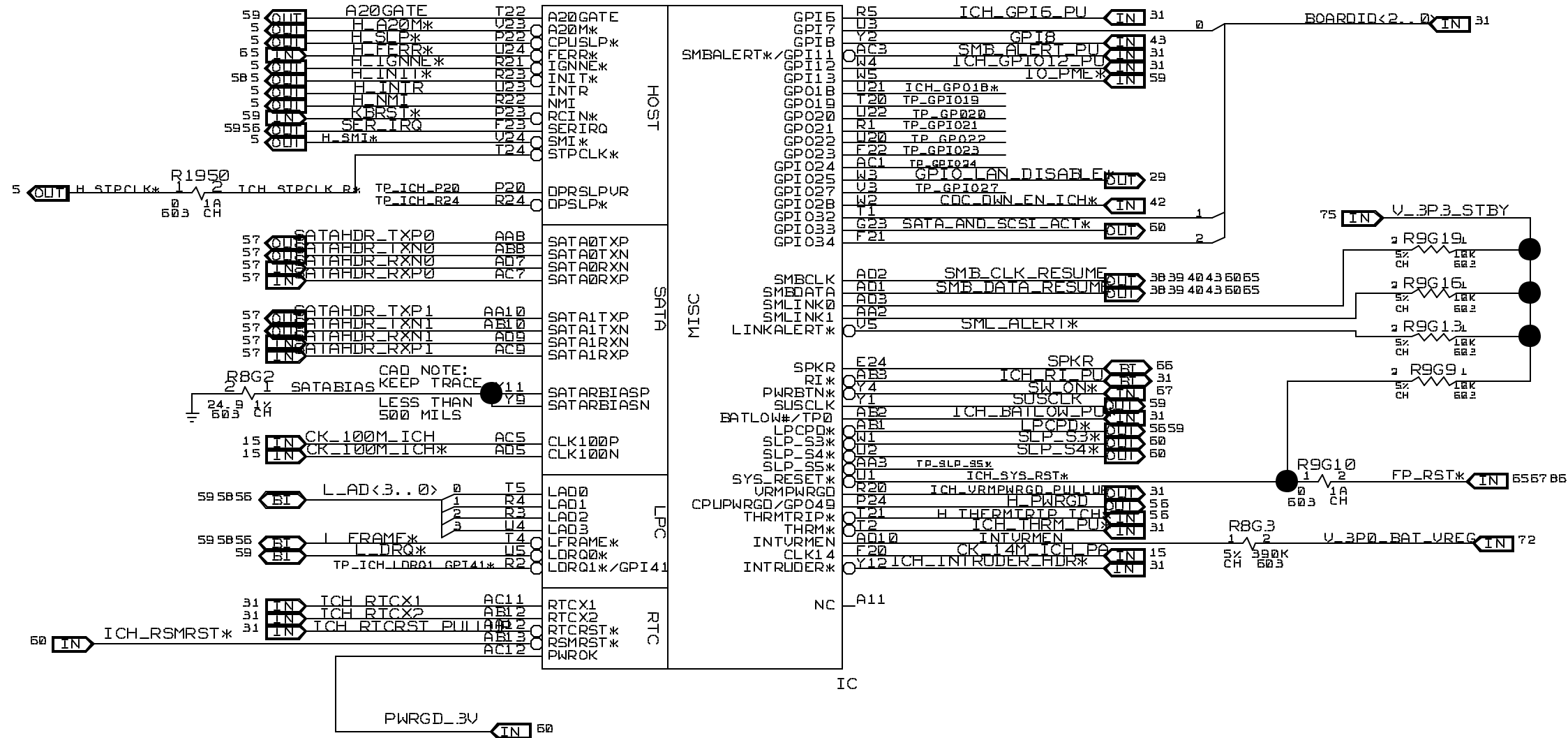
SCHEMATIC TITLE:	
INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED:
	SHEET: 25



SCHEMATIC TITLE:  
 INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD  
 PAGE TITLE: INTEL(R) ICH5 1 OF 4  
 REV: 1.0  
 INTEL PLATFORM APPS ENG. LAST REVISED: Thu Sep 04 10:26:27 2003  
 1000 PRAIRIE CITY ROAD SHEET: 27  
 FOLSOM, CALIFORNIA 95628

DRAWING

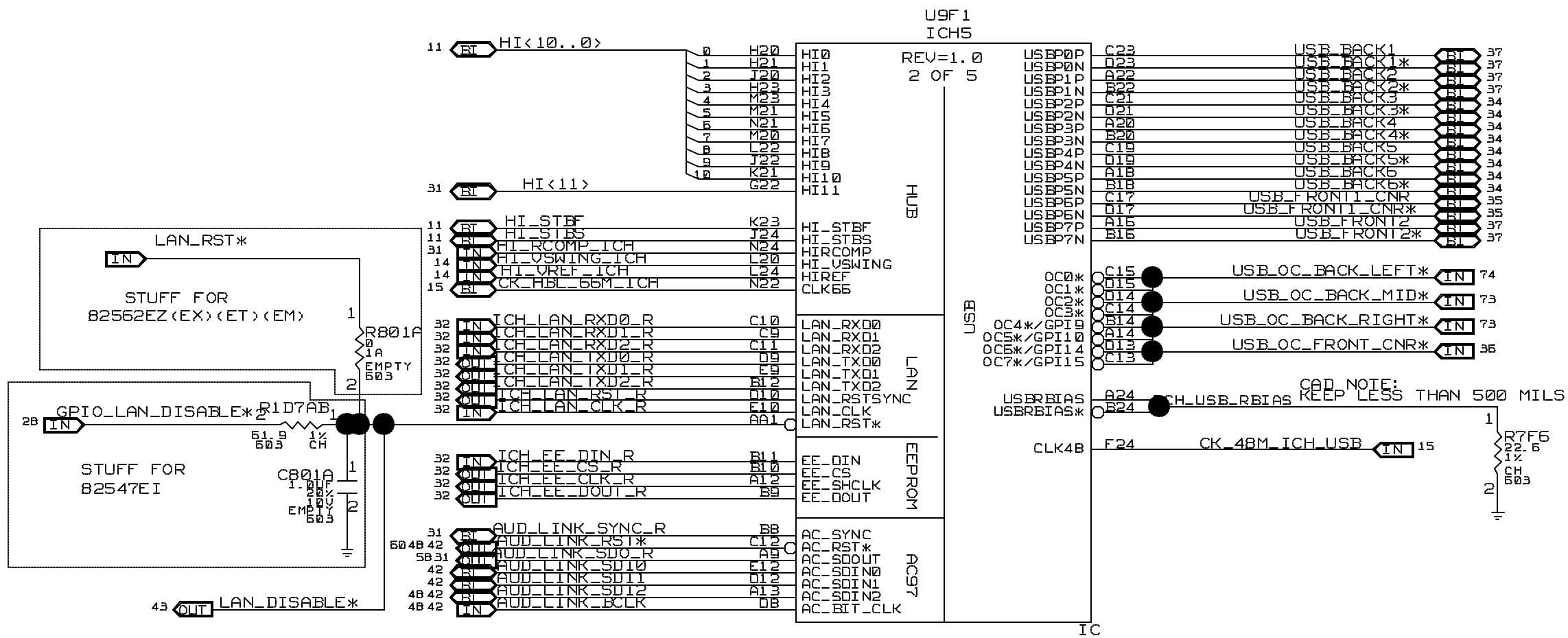
4 OF 5  
REV=1.0  
U9F1  
ICH5



SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		INTEL(R) ICH5 2 OF 4	REV: 4
INTEL	PLATFORM APPS ENG.	LAST REVISED:	SHEET:
1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		Thu Sep 04 10:26:29 2003 28	

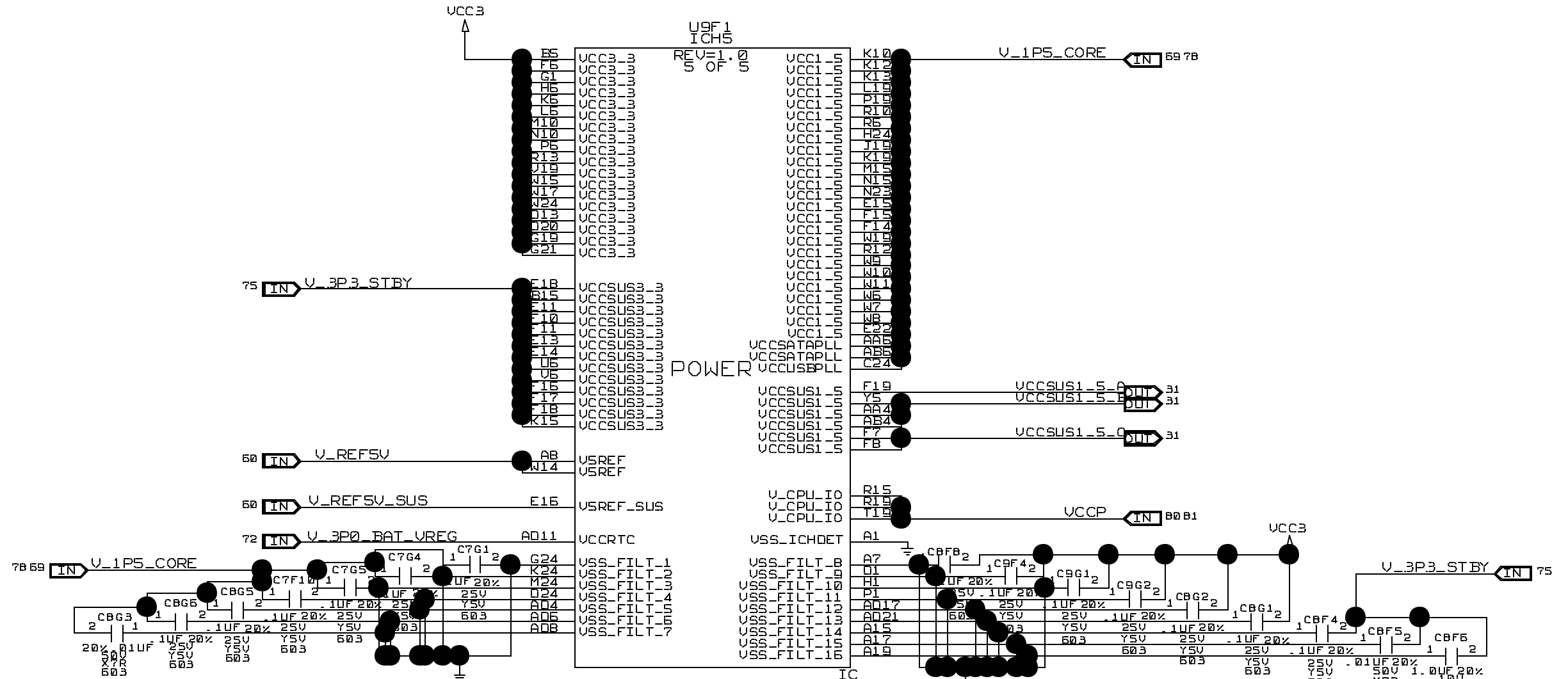
DRAWING





SCHEMATIC TITLE:		
INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE:	INTEL(R) ICH5 3 OF 4	REV: 4
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:26:31 2003	SHEET: 29

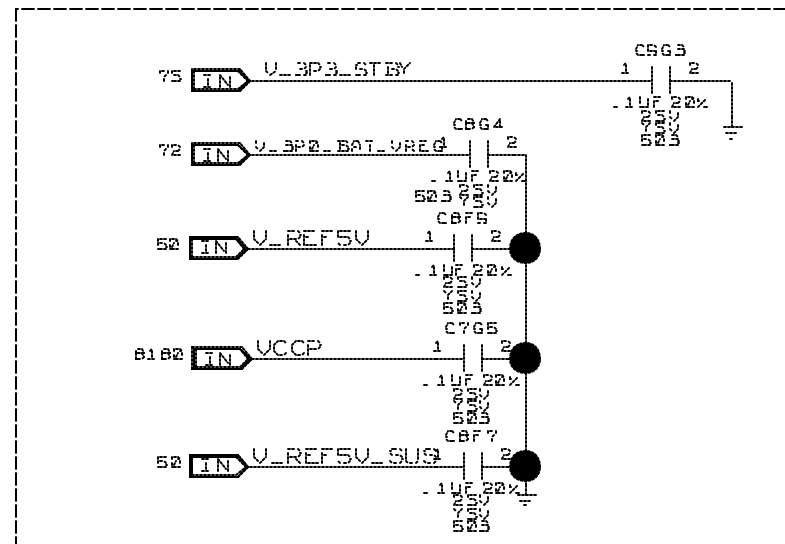
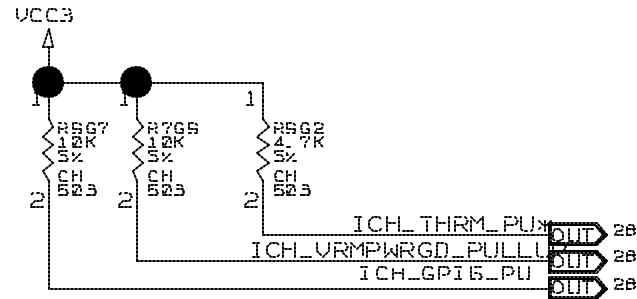
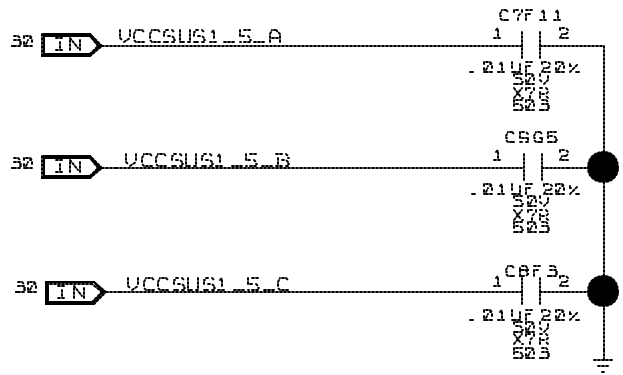
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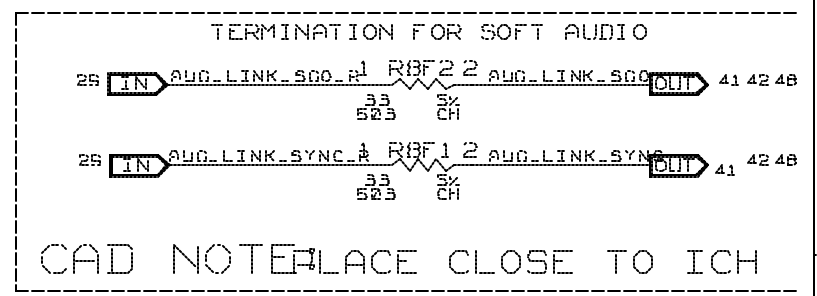
GND: A10, A21, A23, AA11, AA13, AA21, AA24, AA5, AA7, AA9, AB11, AB15, AB18, AB5, AB7, AB9, AC10, AC13, AC2, AC23, AC4, AC6, AC8, AD12, B13, B17, B19, B21, B23, C16, C18, C20, C22, C3, C8, D11, D16, D18, D20, D22, D6, E17, E19, E20, E21, E23, F3, F9, G20, G6, H19, H22, J21, J23, J6, K11, K14, K20, K22, K3, L10, L11, L12, L13, L14, L15, L21, L23, M1, M11, M12, M13, M14, M22, M5, N11, N12, N13, N14, N20, P10, P11, P12, P13, P14, P15, P21, R11, R14, T23, T3, T6, U19, V1, V21, W16, W18, Y10, Y3, Y6, Y7, Y8

DRAWING

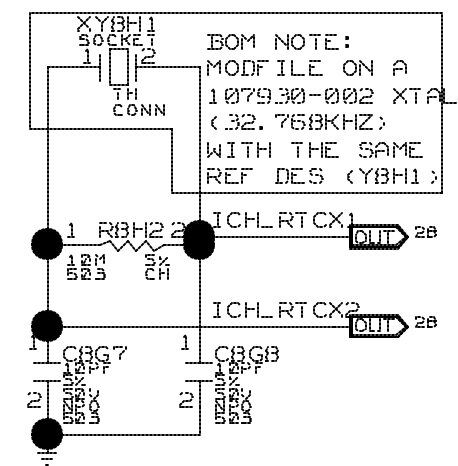
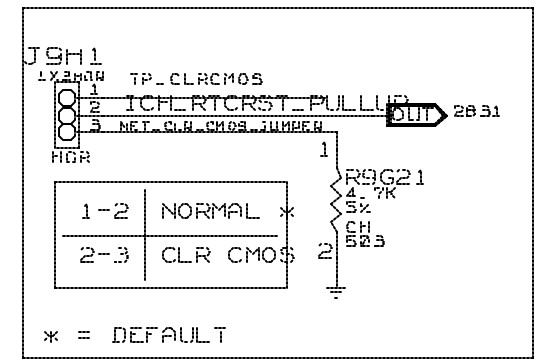
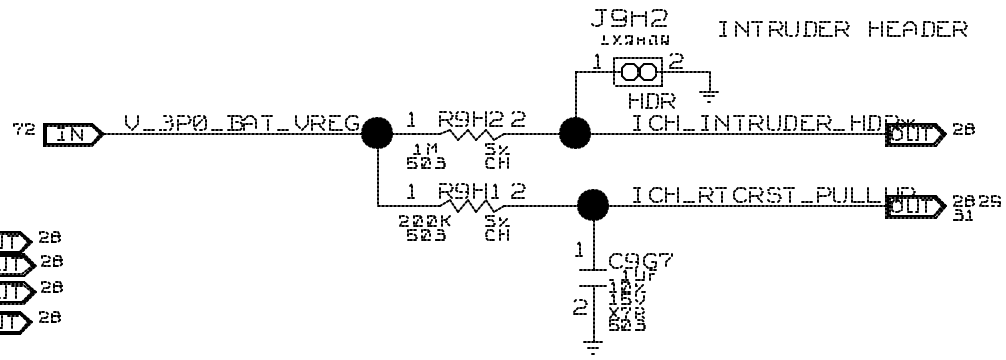
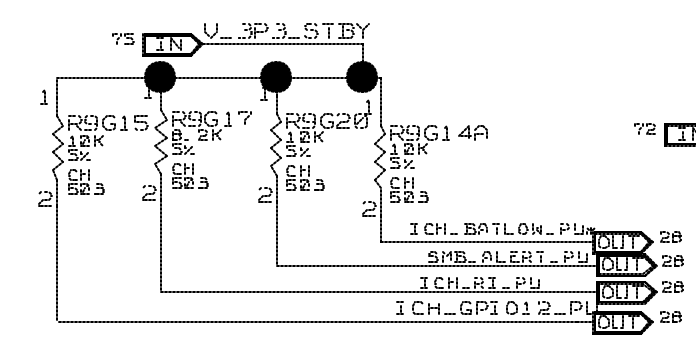
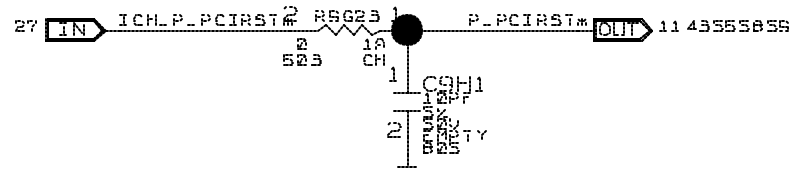
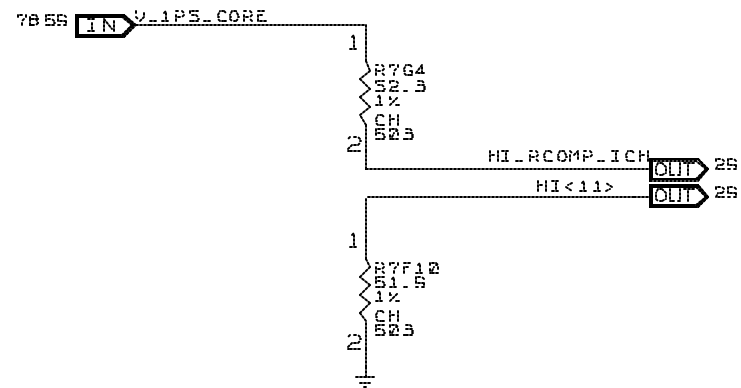
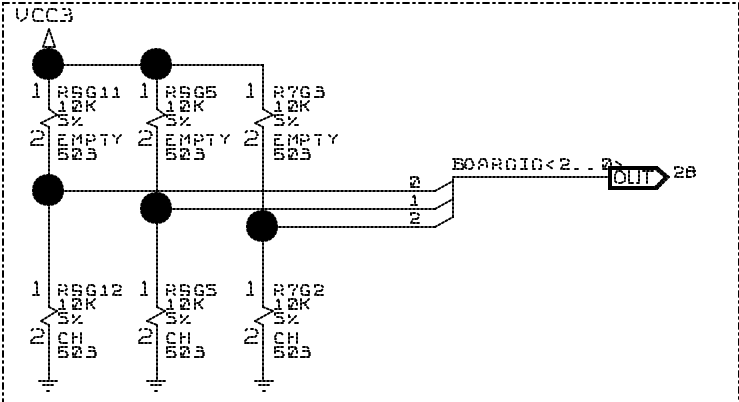
SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: INTEL(R) ICH5 4 OF 4		REV: 4
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:26:33 2003	SHEET: 03 30



\*NOTE: PLACE ALL WITHIN 40 MILS OF ICH5



CAD NOTE: PLACE CLOSE TO ICH



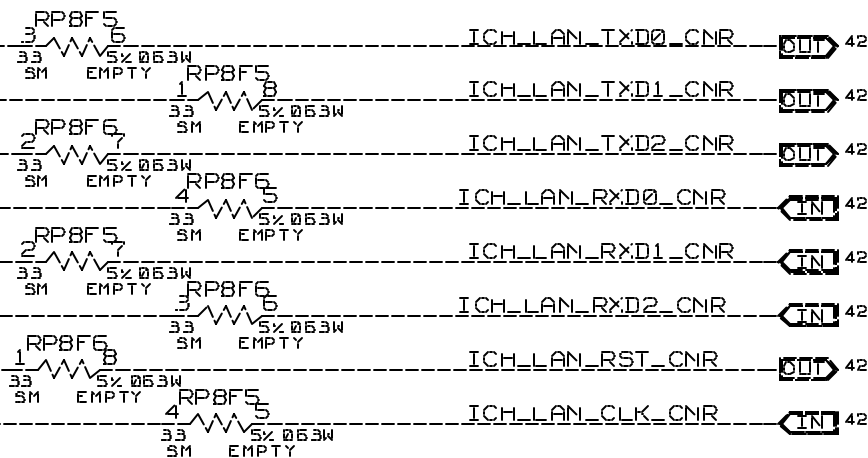
BOM NOTE:  
MODFILE ON A  
107930-002 XTA  
(32.768KHZ)  
WITH THE SAME  
REF DES (Y8H1)

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: INTEL(R) ICH5 PULLUPS & DECOUPLING		REV:
INTEL PLATFORM APPS ENG. 1000 BARRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:26:34 2003	SHEET: 31

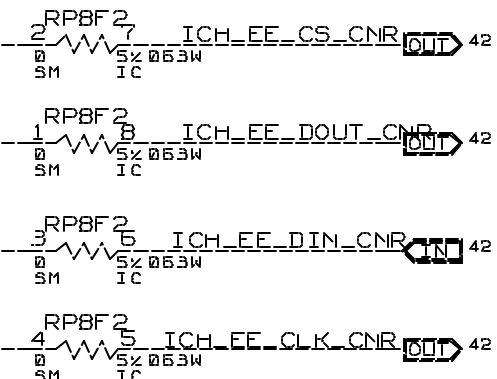
DRAWING

PROPERTIES FOR STUFFING OPTIONS: BOM= CNR\_LINK\_LAN  
CNR STUFFING OPTION FOR LAN-UP SOLUTION

TO CNR



TO CNR



0-OHMS ARE PROVIDED TO MINIMIZE STUBS ON LAN INTERFACE

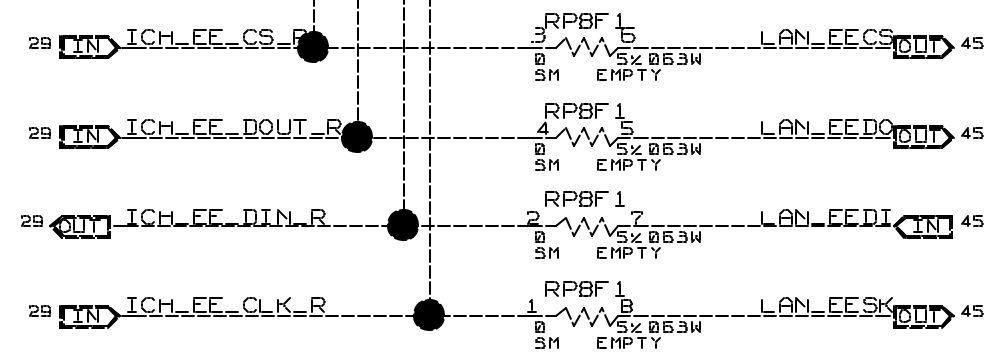
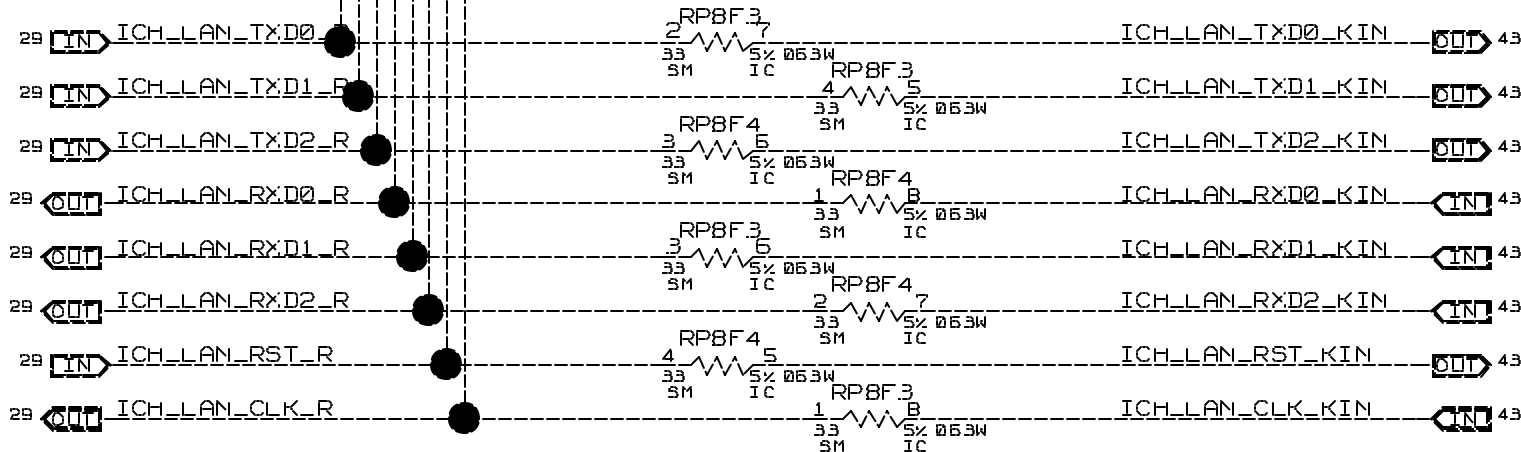
PROPERTIES FOR STUFFING OPTIONS: BOM= LAN\_LINK\_CNR

FROM ICH5

TO LAN (KINNERETH-R)

FROM ICH5

TO LAN EEPROMS

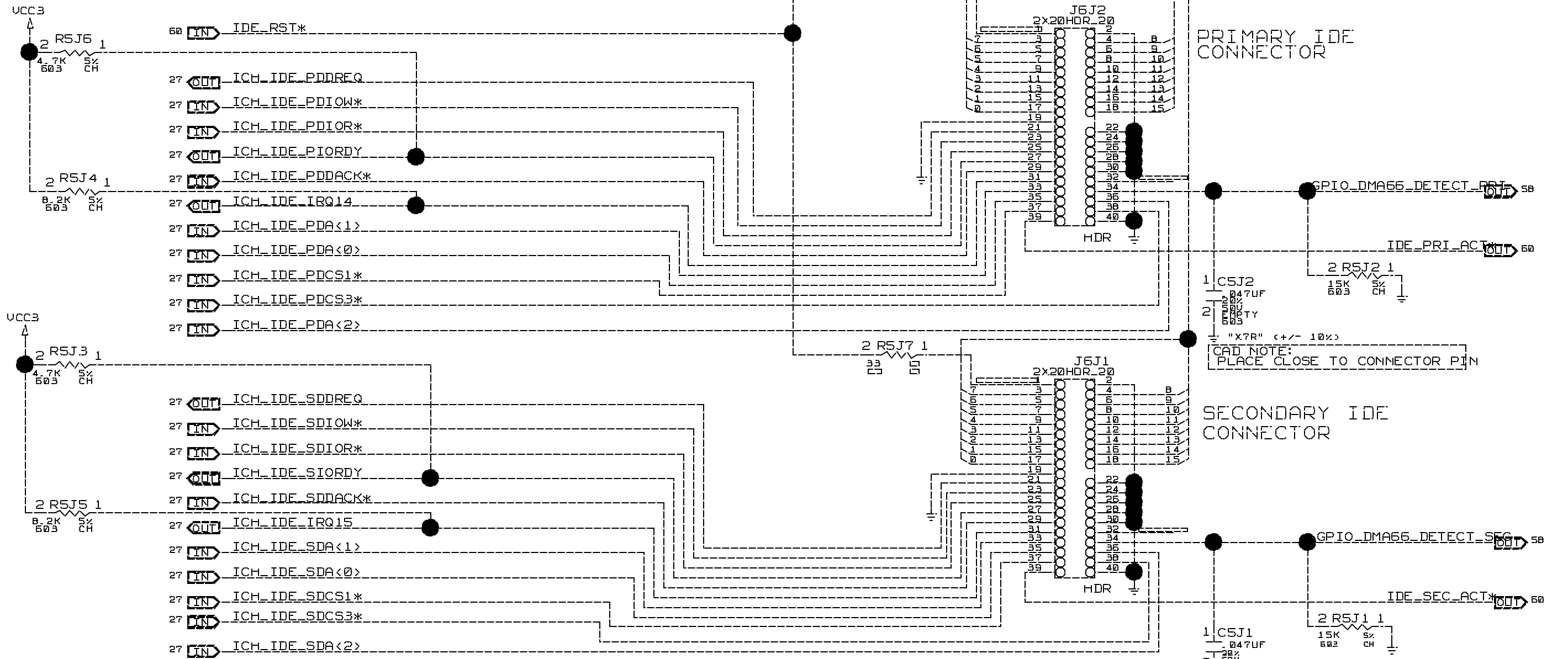


DRAWING

SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		LAN STUFFING OPTION	
INTEL PLATFORM APPS ENG.		LAST REVISED:	
1000 PRAIRIE CITY ROAD		Thu Sep 04 10:26:36 2003	
FOLSOM, CALIFORNIA 95630		SHEET: 32	

DESIGN NOTE:  
 SERIES RESISTORS INTEGRATED INTO ICH:  
 VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS

27 IN ICH\_IDE\_SDD<15..0>  
 27 IN ICH\_IDE\_PDD<15..0>



PRIMARY IDE CONNECTOR

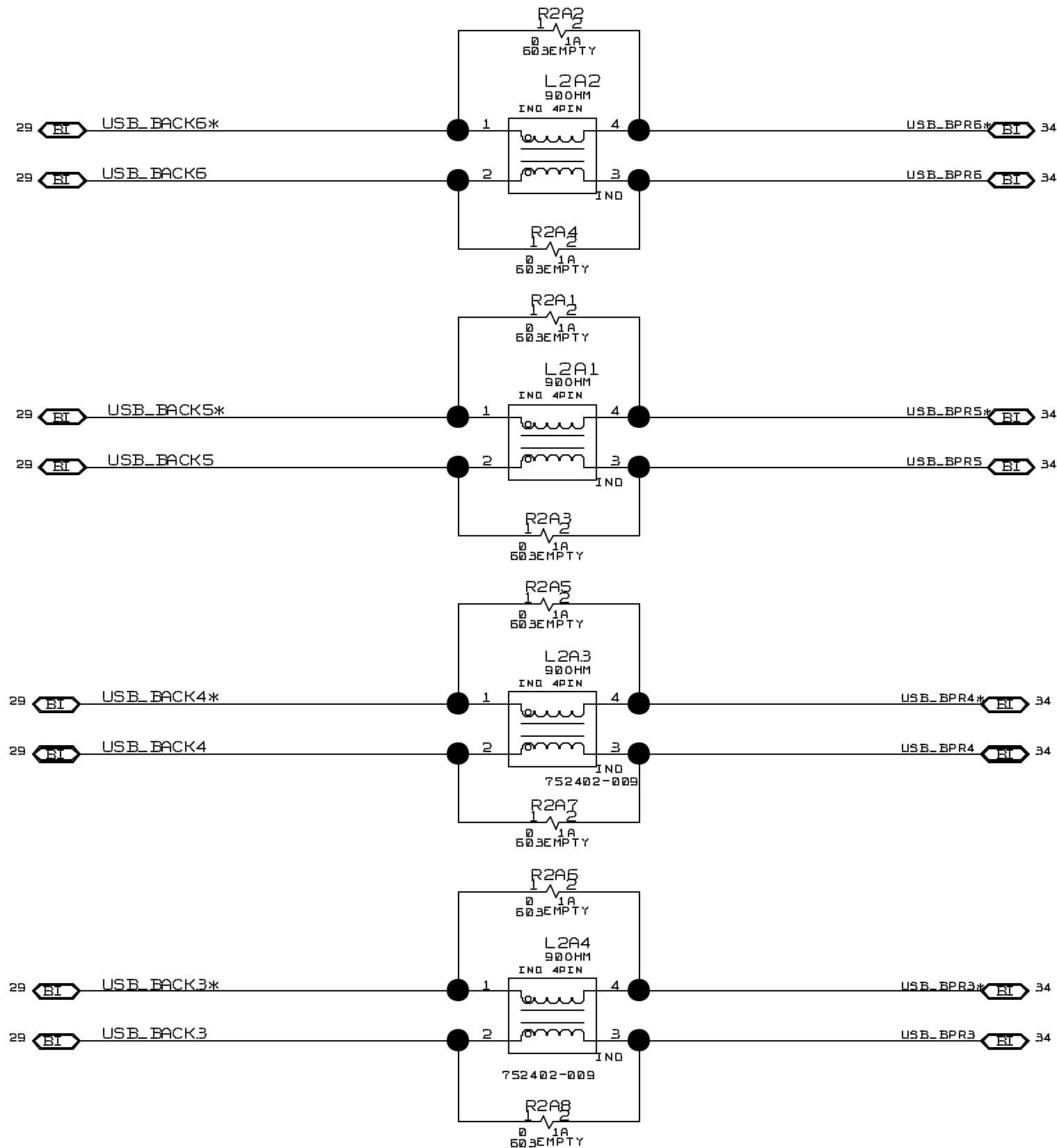
SECONDARY IDE CONNECTOR

CAD NOTE:  
 PLACE CLOSE TO CONNECTOR P1N

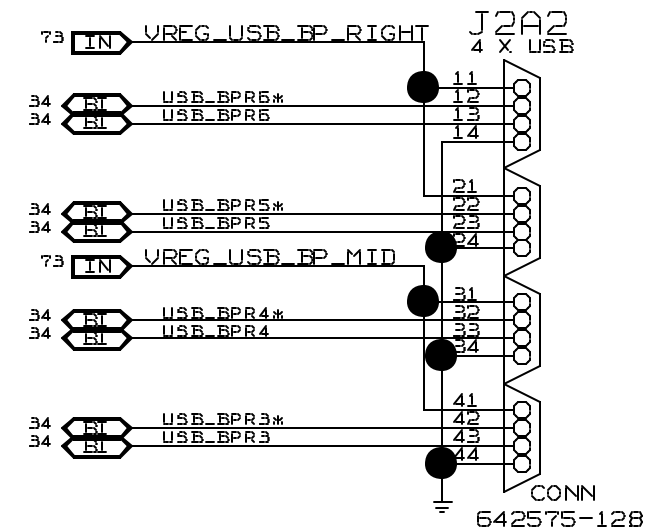
CAD NOTE:  
 PLACE CLOSE TO CONNECTOR P1N

SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		IDE CONNECTOR	
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620		LAST REVISED: Thu Sep 04 10:26:38 2003	REV: SHEET: 33

DRAWING



### QUAD STACK USB

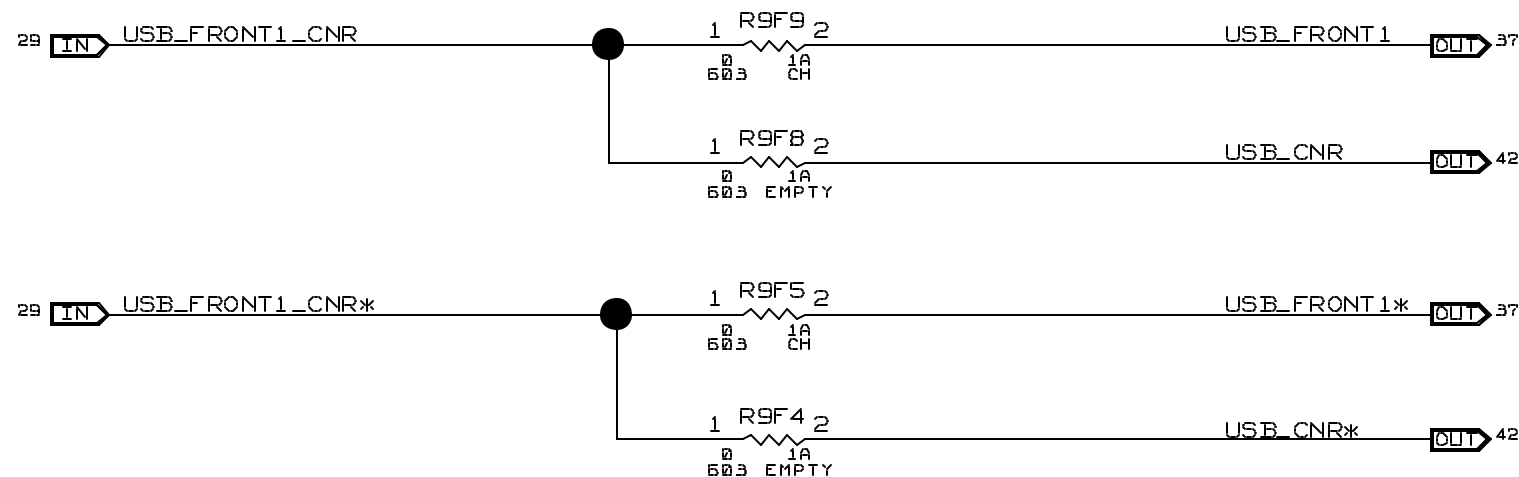


DRAWING

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: BACKPANEL_USB_RIGHT AND MID		SHEET:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:26:40 2003	20034

# USB SWITCH

## USB OPTION FOR FRONT PANEL OR CNR

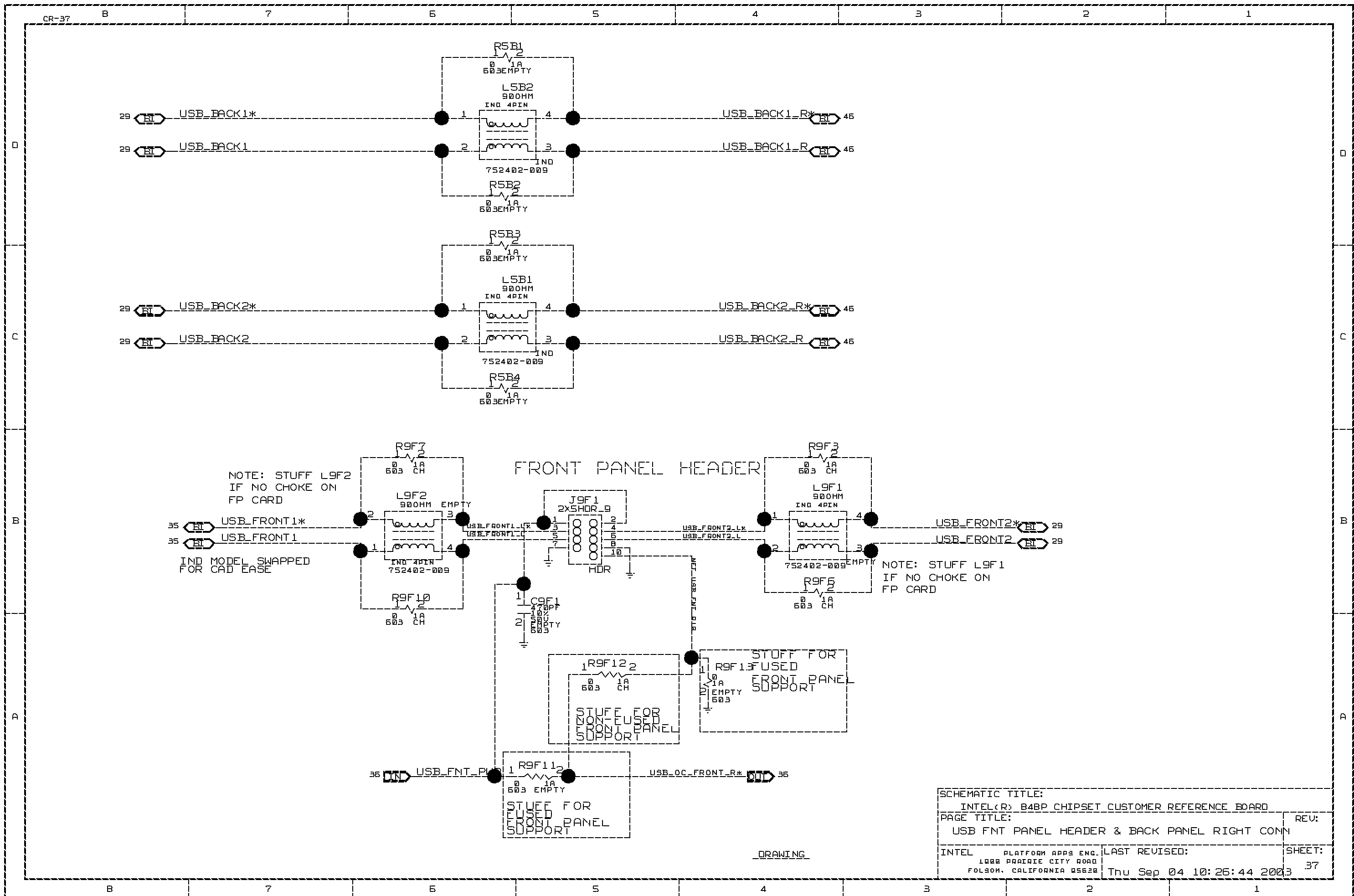


DRAWING

SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		USB ROUTING OPTION	
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620		LAST REVISED: Thu Sep 04 10:26:41 2003	REV: SHEET: 035



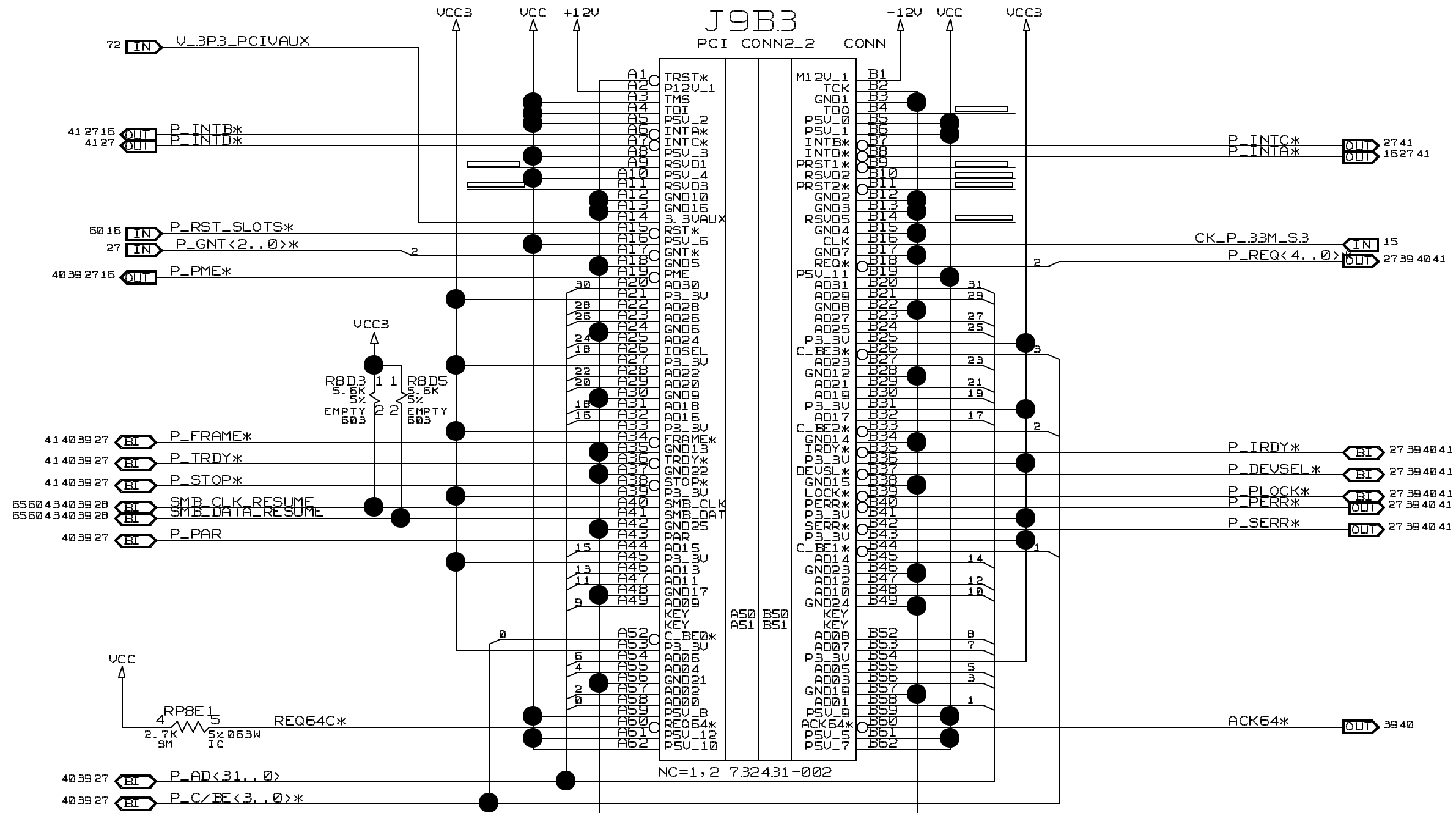




SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		USB FNT PANEL HEADER & BACK PANEL RIGHT CONN	
INTEL PLATFORM APPS ENG.		LAST REVISED:	
1000 PRAIRIE CITY ROAD		Thu Sep 04 10:26:44 2003	
FOLSOM, CALIFORNIA 95620		SHEET: 37	

DRAWING

# PCI SLOT 3



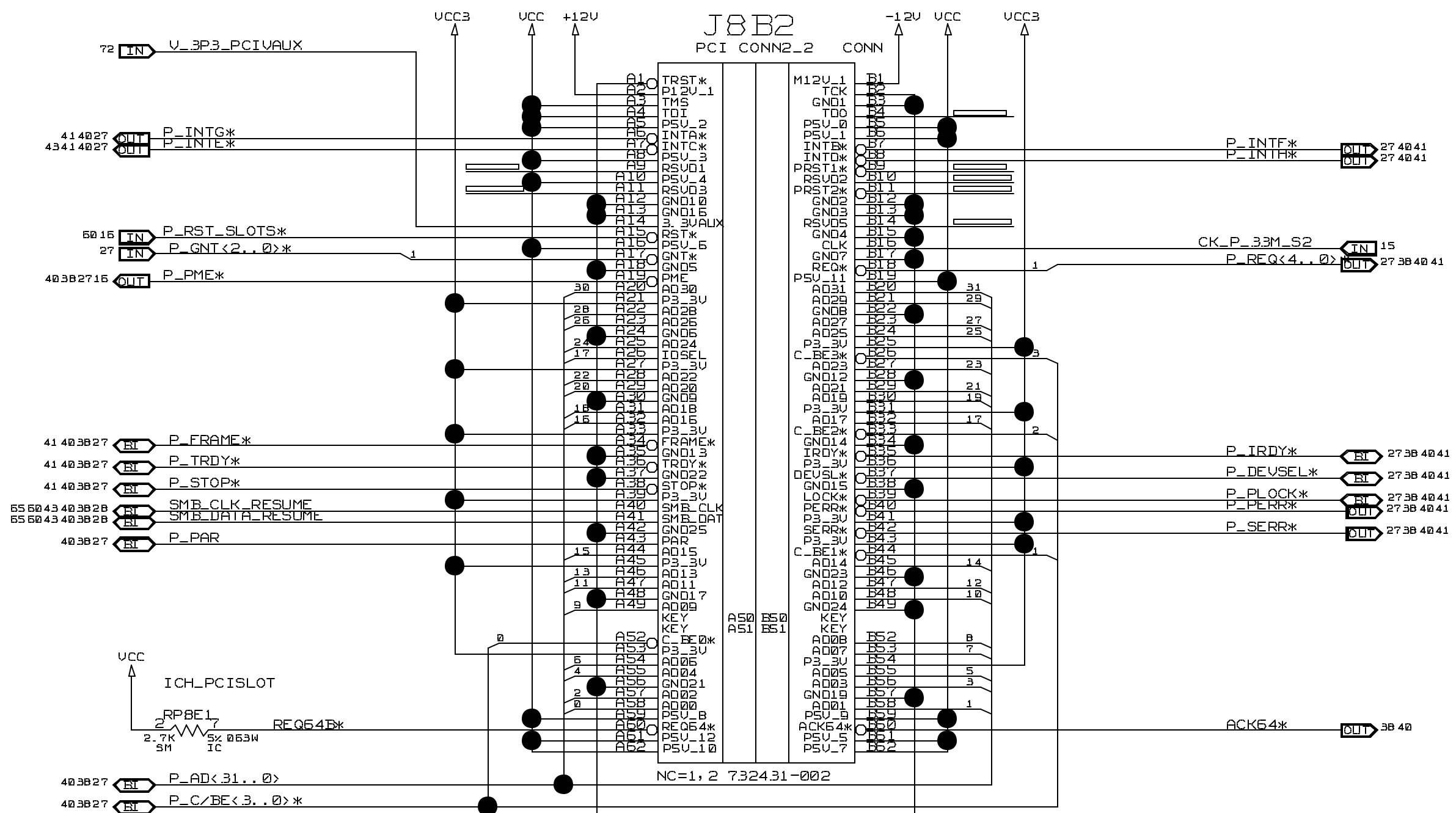
DESIGN NOTE:  
 PCI SLOT3 = PCI DEVICE FUNCTION 10H  
 = PCI DEVICE NUMBER 2H  
 = IDSEL VALUE AD18

DRAWING

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: <b>PCI SLOT 3</b>	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:26:46 2003
SHEET: 03 38	

# PCI SLOT 2

## J8B2 PCI CONN2\_2 CONN



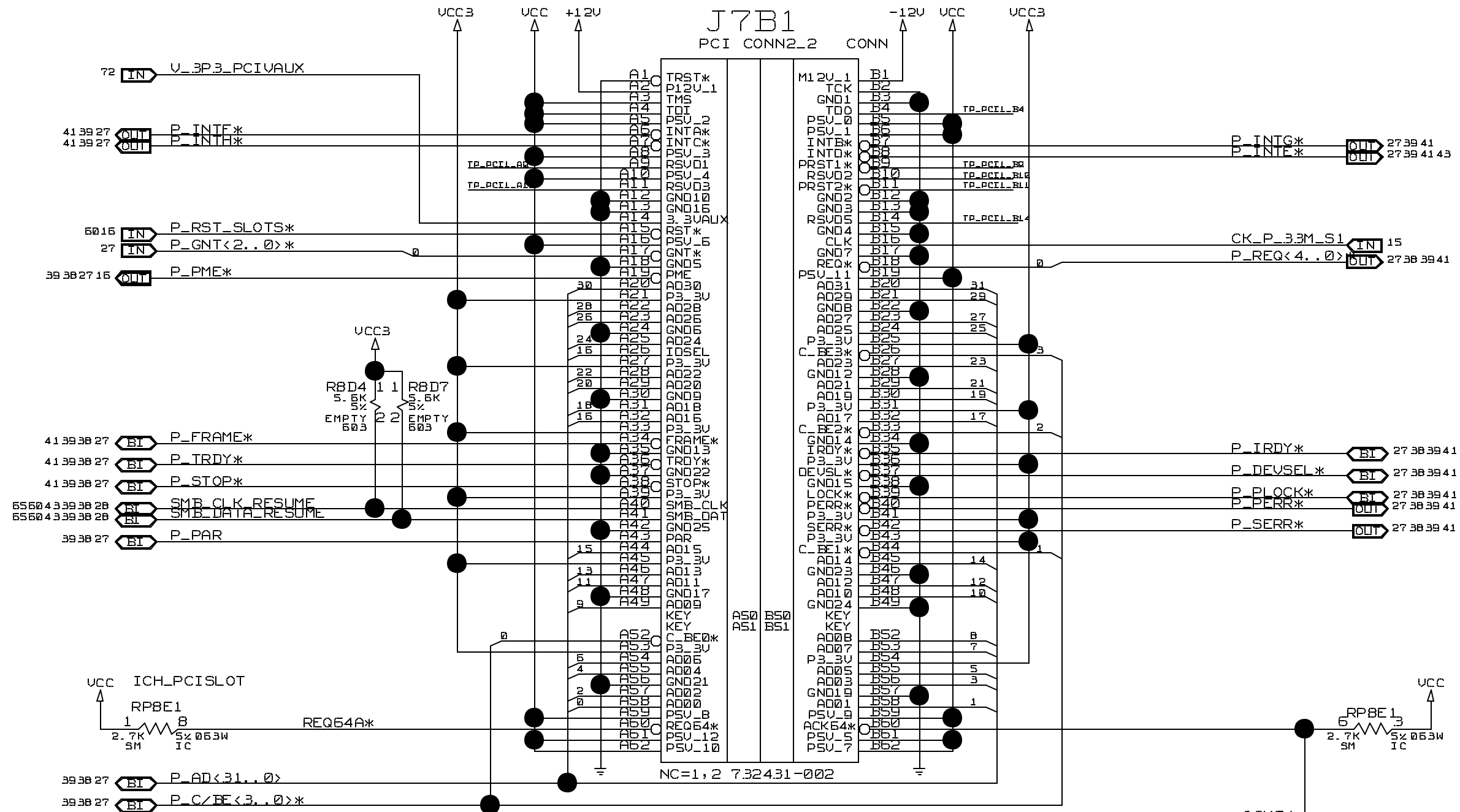
DESIGN NOTE:  
 PCI SLOT2 = PCI DEVICE FUNCTION 08H  
 = PCI DEVICE NUMBER 1H  
 = IDSEL VALUE AD17

DRAWING

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: <b>PCI SLOT 2</b>	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:26:47 2003
SHEET: 39	

# PCI SLOT 1 CLOSEST PCI SLOT TO CPU

## J7B1 PCI CONN2\_2 CONN



**CAD NOTE:**  
 MAKE PLACEMENT THE SAME AS ON THE EVAL BOARD  
 FOR TEST-POINTED, EMPTY RESISTOR SITES

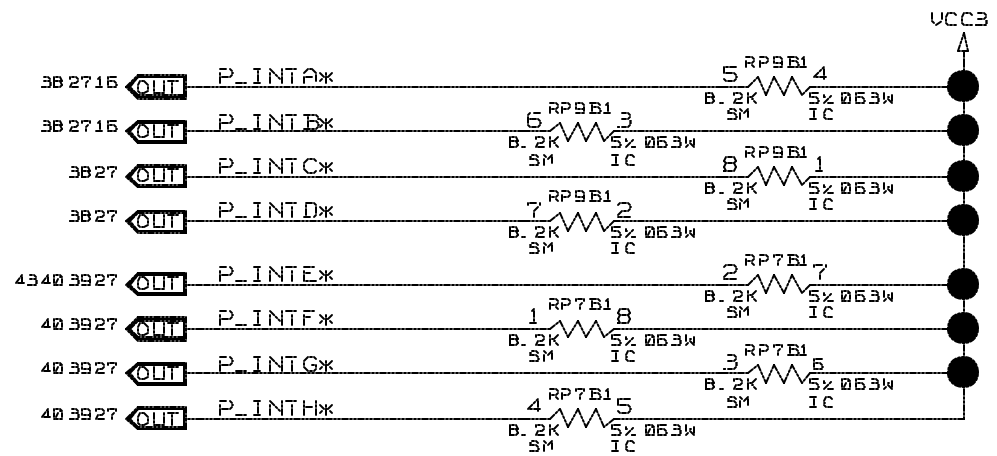
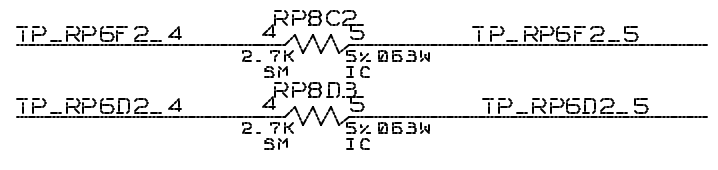
**DESIGN NOTE:**  
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 = PCI DEVICE NUMBER 0H  
 = IDSEL VALUE AD16

39 38 **IN** ACK64\*

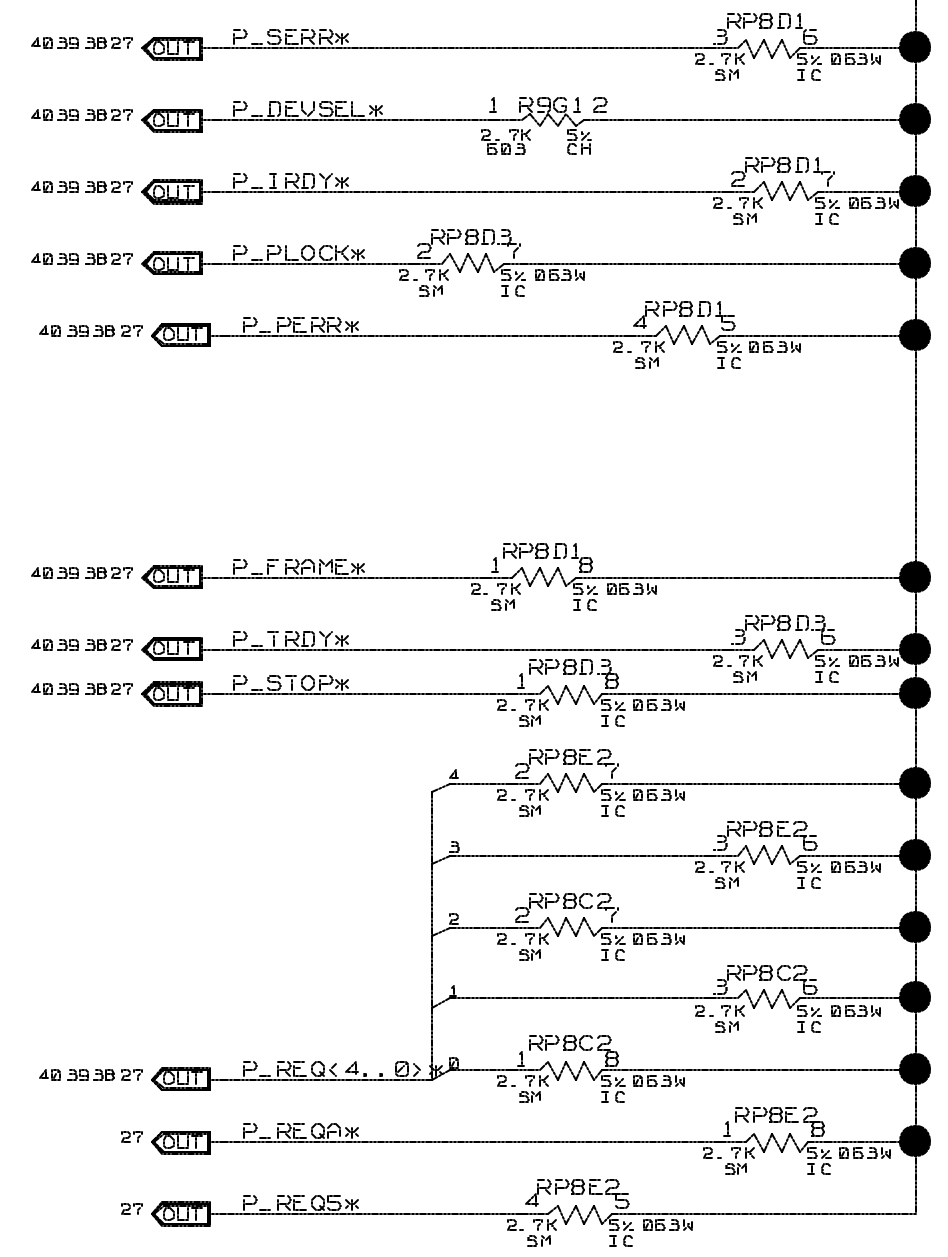
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SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: <b>PCI SLOT 1</b>	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:26:49 2003
SHEET: 40	

SPARE SECTIONS



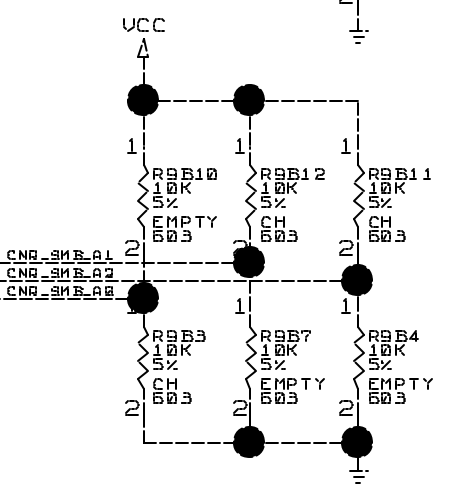
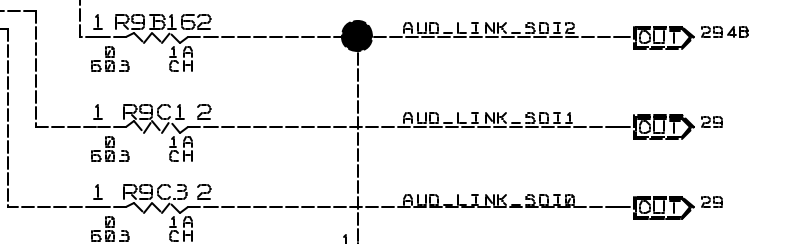
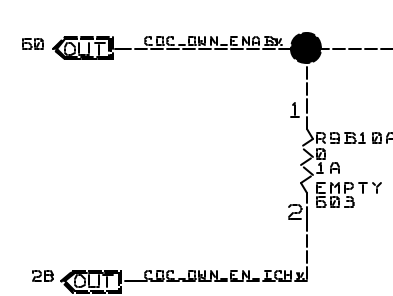
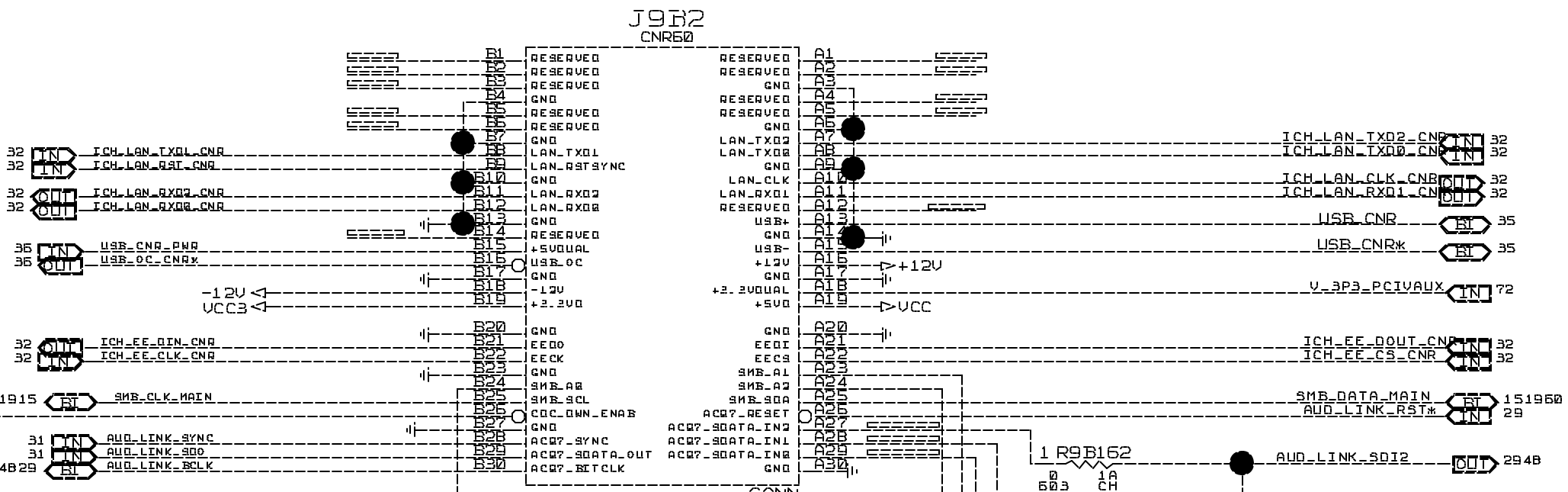
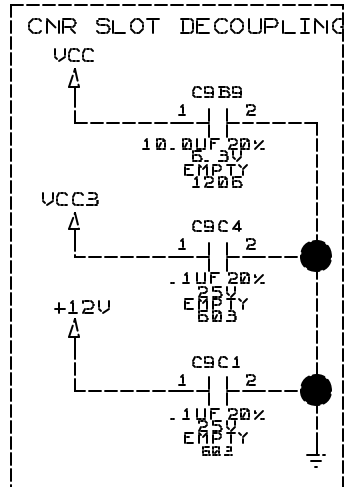
PCI PULL-UPS



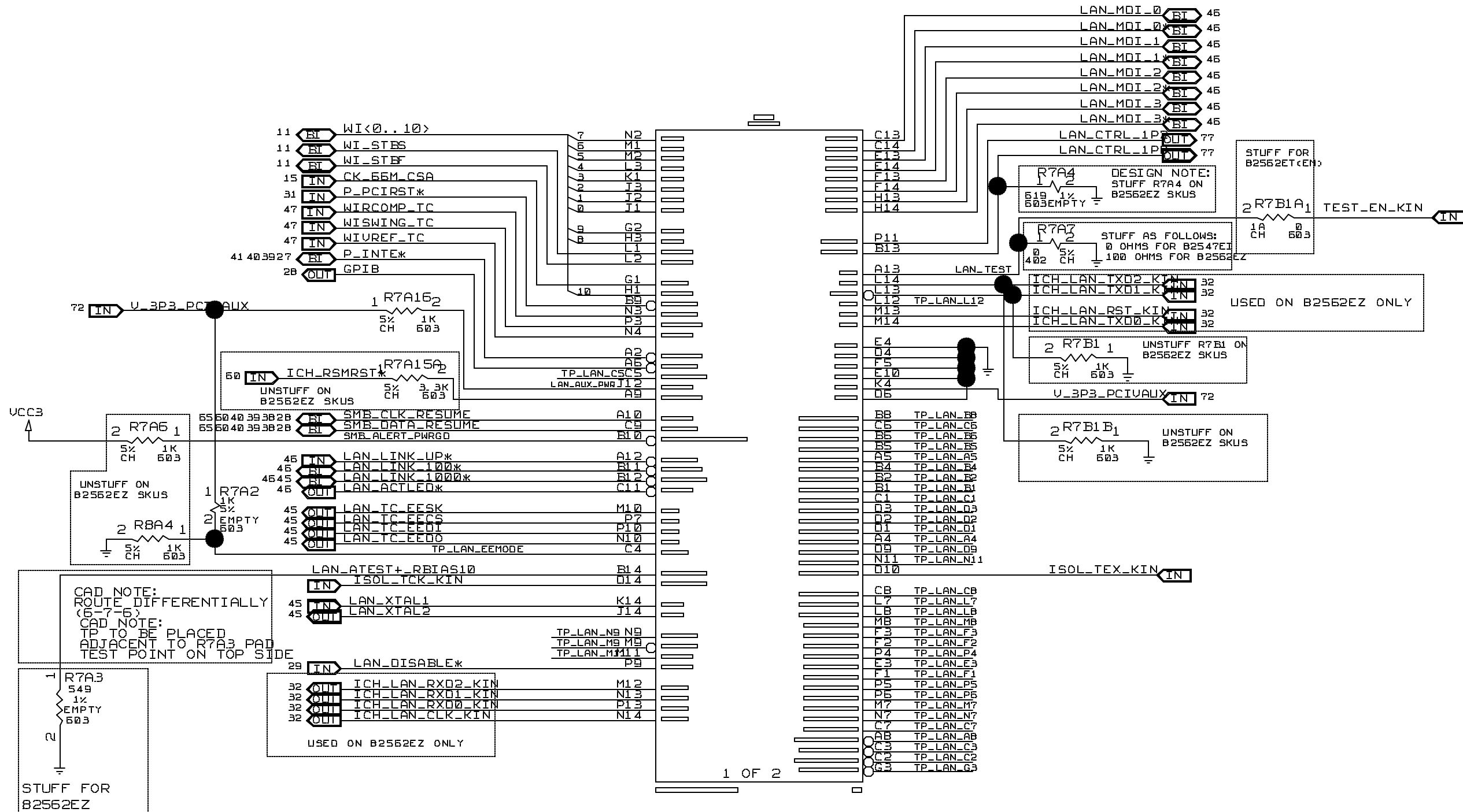
DRAWING

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: PCI TERMINATION		SHEET:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:26:51 2003	41

SMB ADDRESS: 110  
WRITE AC  
READ AD



SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		CNR	
DRAWING		REV:	SHEET:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: Thu Sep 04 10:26:53 2003	42



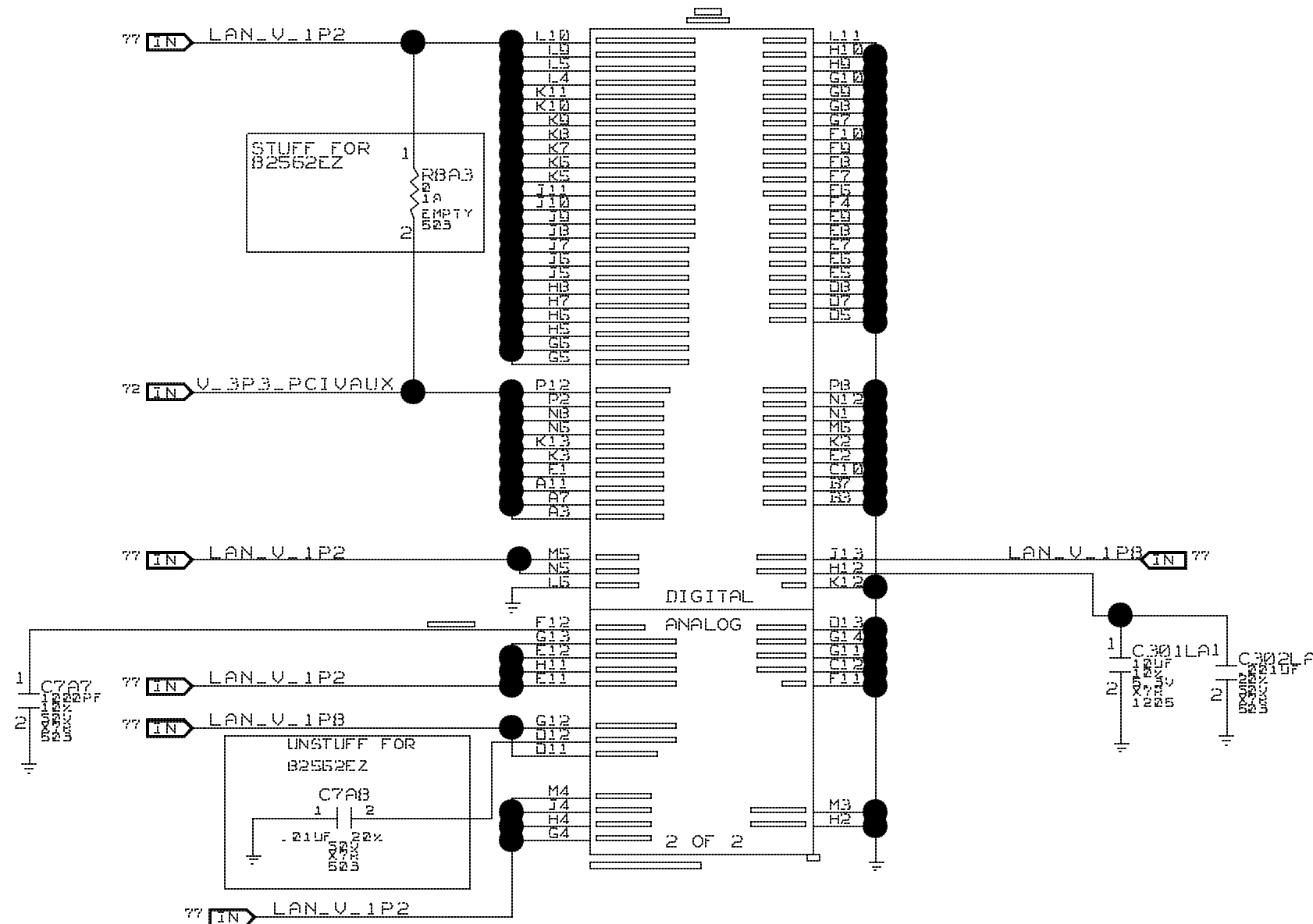
CAD NOTE:  
ROUTE DIFFERENTIALLY  
(5-7-5)  
CAD NOTE:  
TP TO BE PLACED  
ADJACENT TO R7A3 PAD  
TEST POINT ON TOP SIDE

R7A3  
549  
1x  
EMPTY  
503  
STUFF FOR  
B2562EZ

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: B2547EI/B2562EZ(EX)(ET)(EM)	REV: 0.3
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:26:55 2003
SHEET: 03 43	

DRAWING

1 OF 2



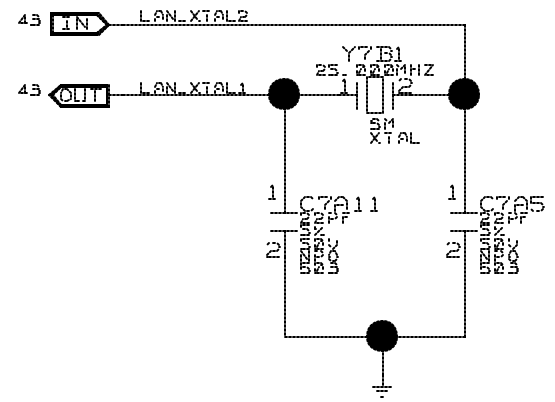
DRAWING

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: B2547EI/B2562EZ(EX)(ET)(EM) POWER CONNECTIONS	REV:
INTEL PLATFORM APPS ENG. 1800 BRANNE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:26:56 2003
SHEET: 44	



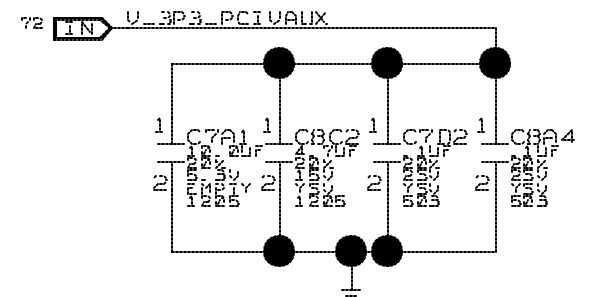
### LAN CRYSTAL

CAD NOTE:  
MINIMIZE XTAL TRACES  
DO NOT PLACE OR ROUTE NEAR PLANE SPLIT



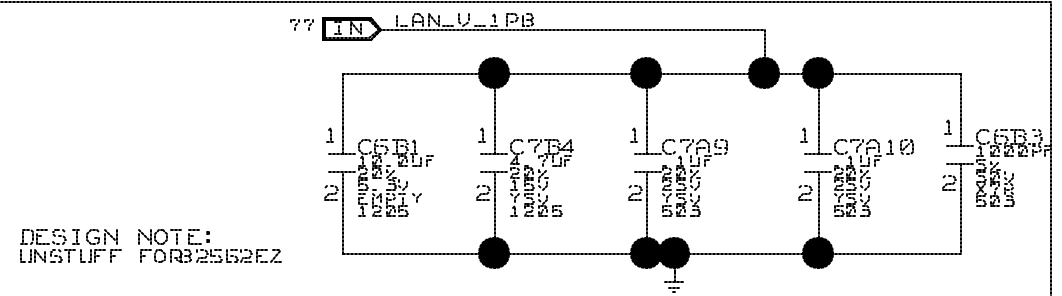
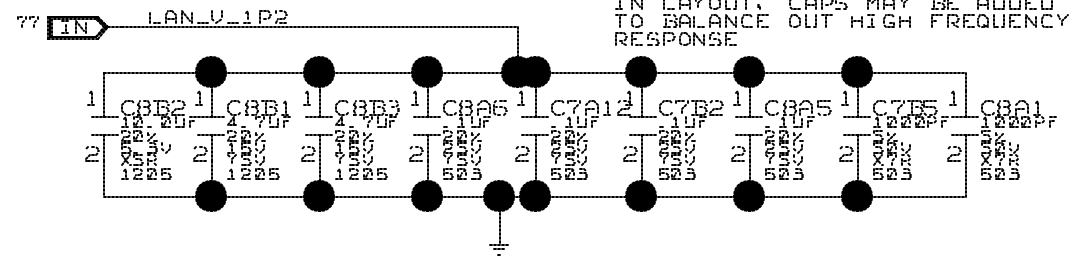
### LAN DECOUPLING

DESIGN NOTE:  
DECOUPLING CAPS SHARE BETWEEN  
B2552EZ & B2547EI  
VOLTAGE NETS



### DESIGN NOTE:

DEPENDING ON POWER DELIVERY  
IN LAYOUT, CAPS MAY BE ADDED  
TO BALANCE OUT HIGH FREQUENCY  
RESPONSE

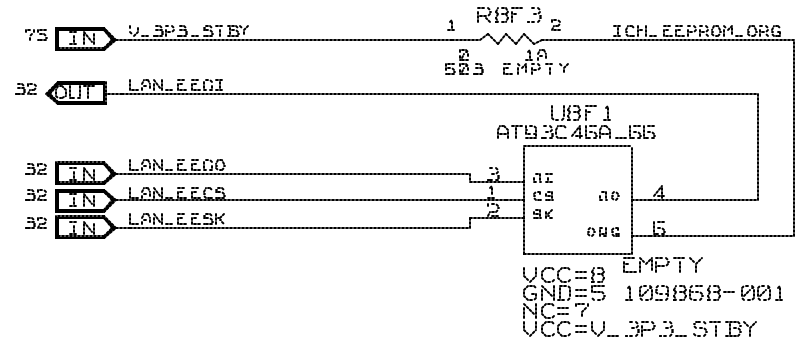


DESIGN NOTE:  
UNSTUFF FOR B2552EZ

### B2552EZ EEPROM

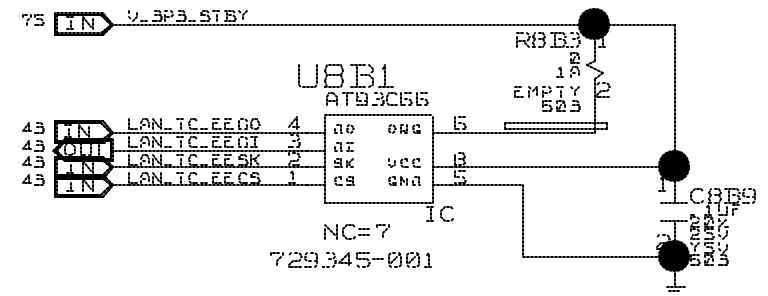
STUFF THIS EEPROM ONLY WITH B2552EZ.  
SKUS. PLACE NEAR ICH

DESIGN NOTE:  
IN ABSENCE OF CNR, THIS RESISTOR MAY BE REMOVED

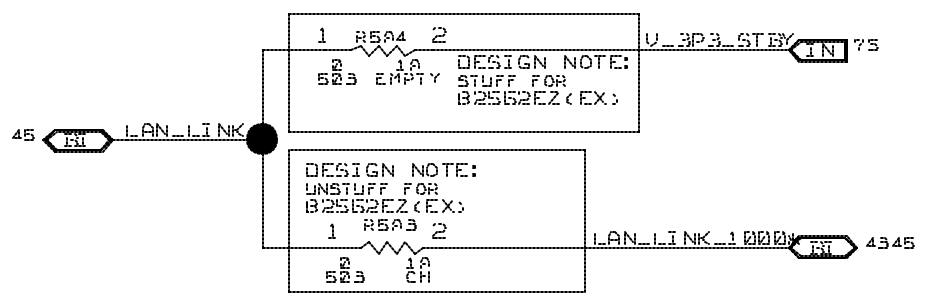


### B2547EI EEPROM

CAD NOTE:  
PLACE EEPROM NEAR LAN CONTROLLER.



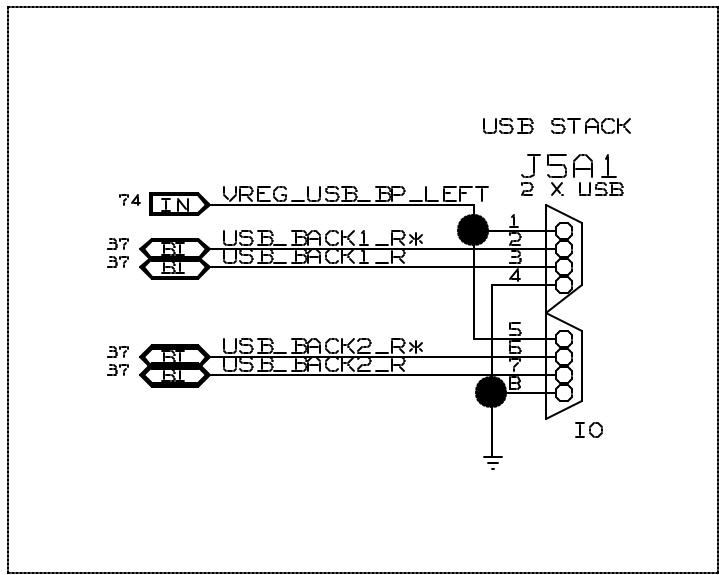
### STUFFING OPTIONS FOR LED ENABLING



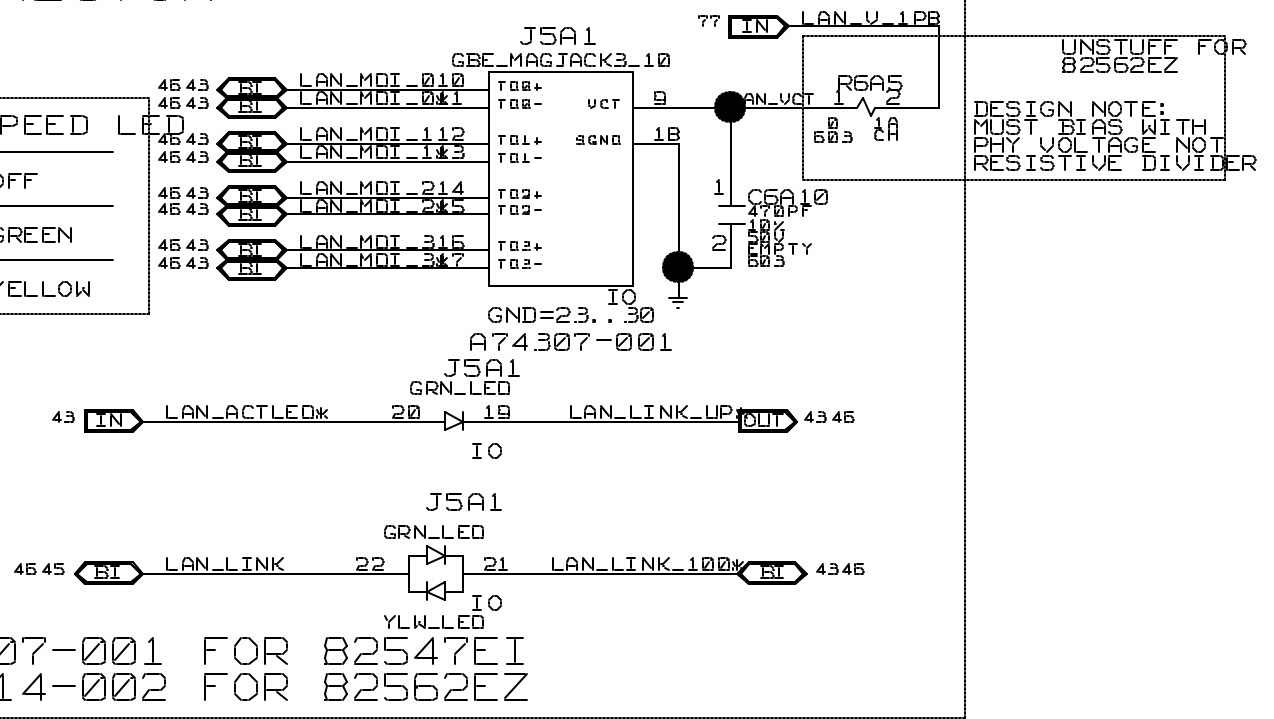
SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: LAN EEPROMS/DECOUPLING/LED	REV: 
INTEL PLATFORM APPS ENG. 1800 AMARIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:26:58 2003
SHEET: 	

DRAWING

### LAN CONNECTOR

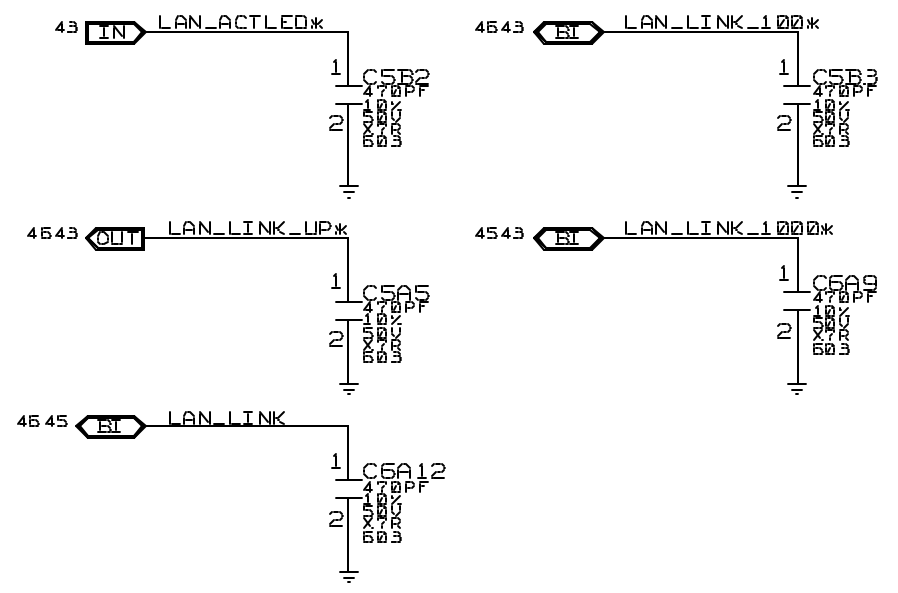


BI-COLOR SPEED LED	
10 MBPS	OFF
100 MBPS	GREEN
1000 MBPS	YELLOW



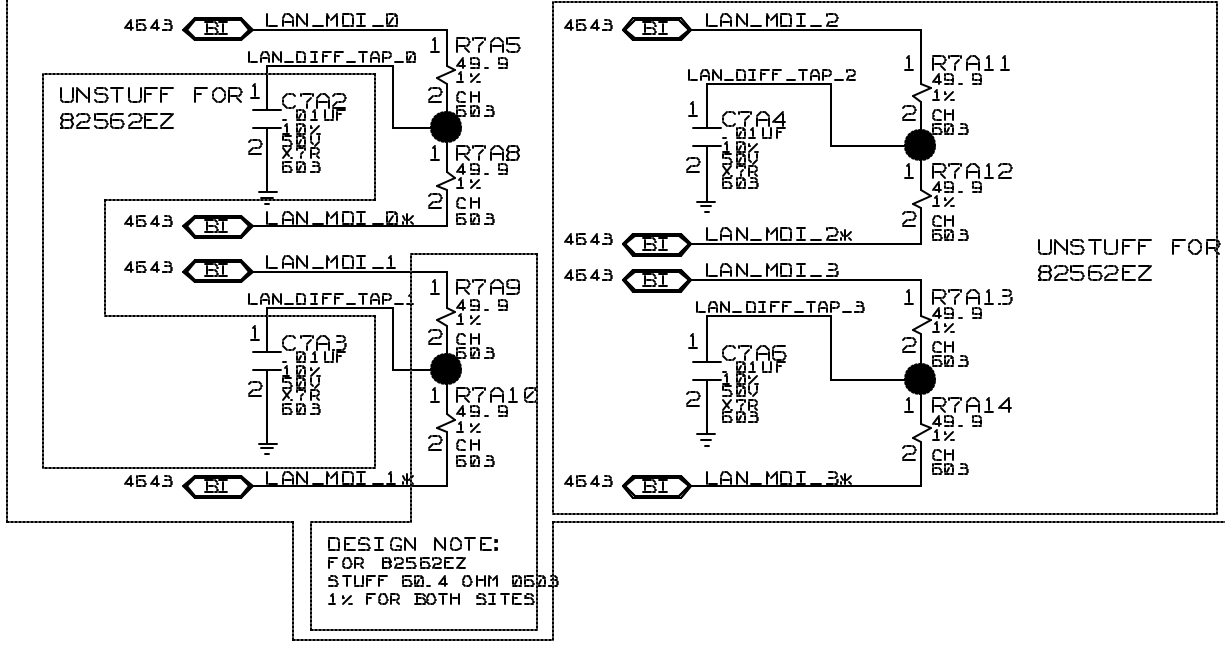
### LED DECOUPLING

CAD NOTE:  
LED CAPS SHOULD BE PLACED NEXT TO CONNECTOR



### DIFFERENTIAL PAIR TERMINATIONS

CAD NOTE:  
PLACE NEXT TO CONTROLLER

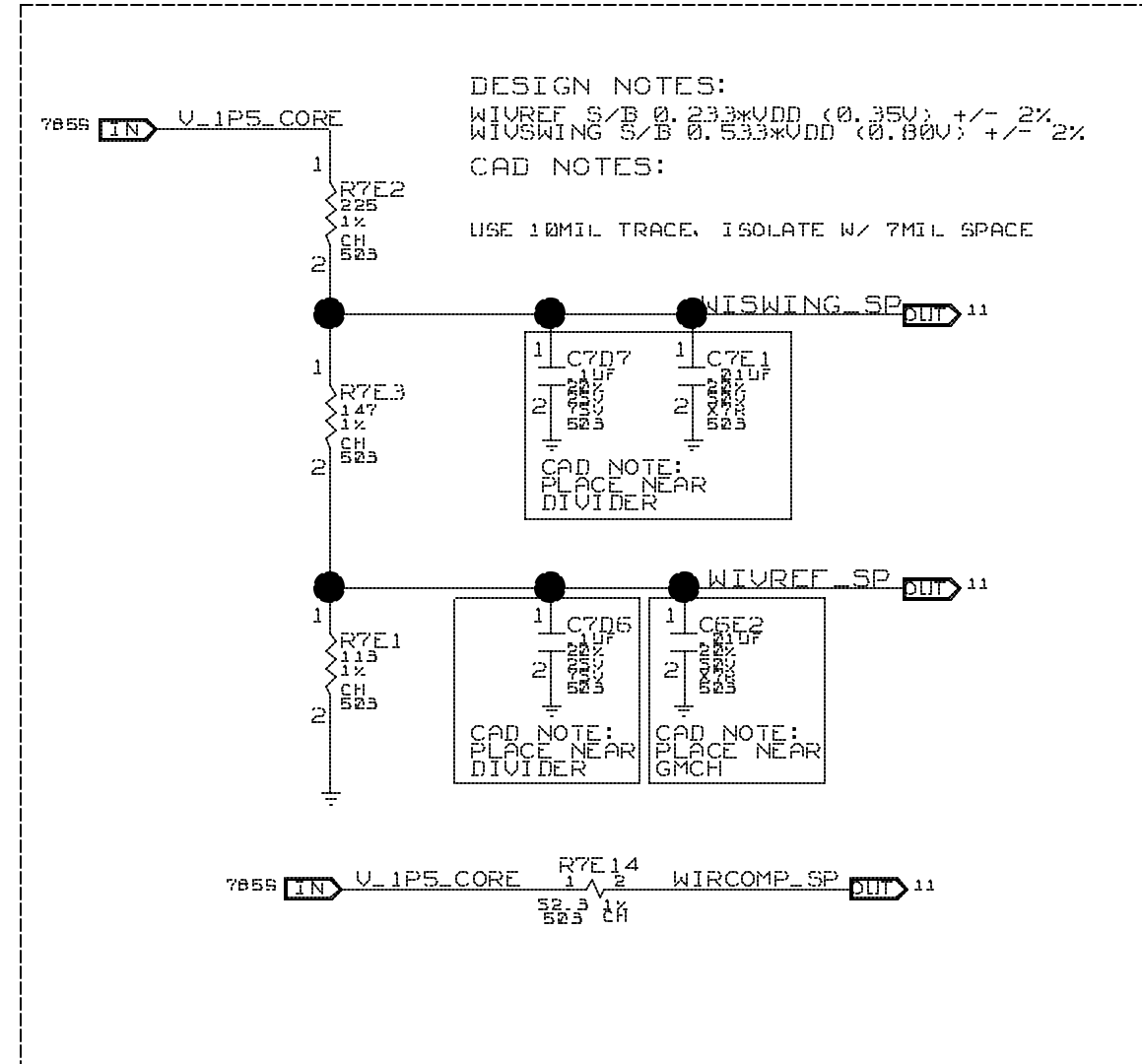
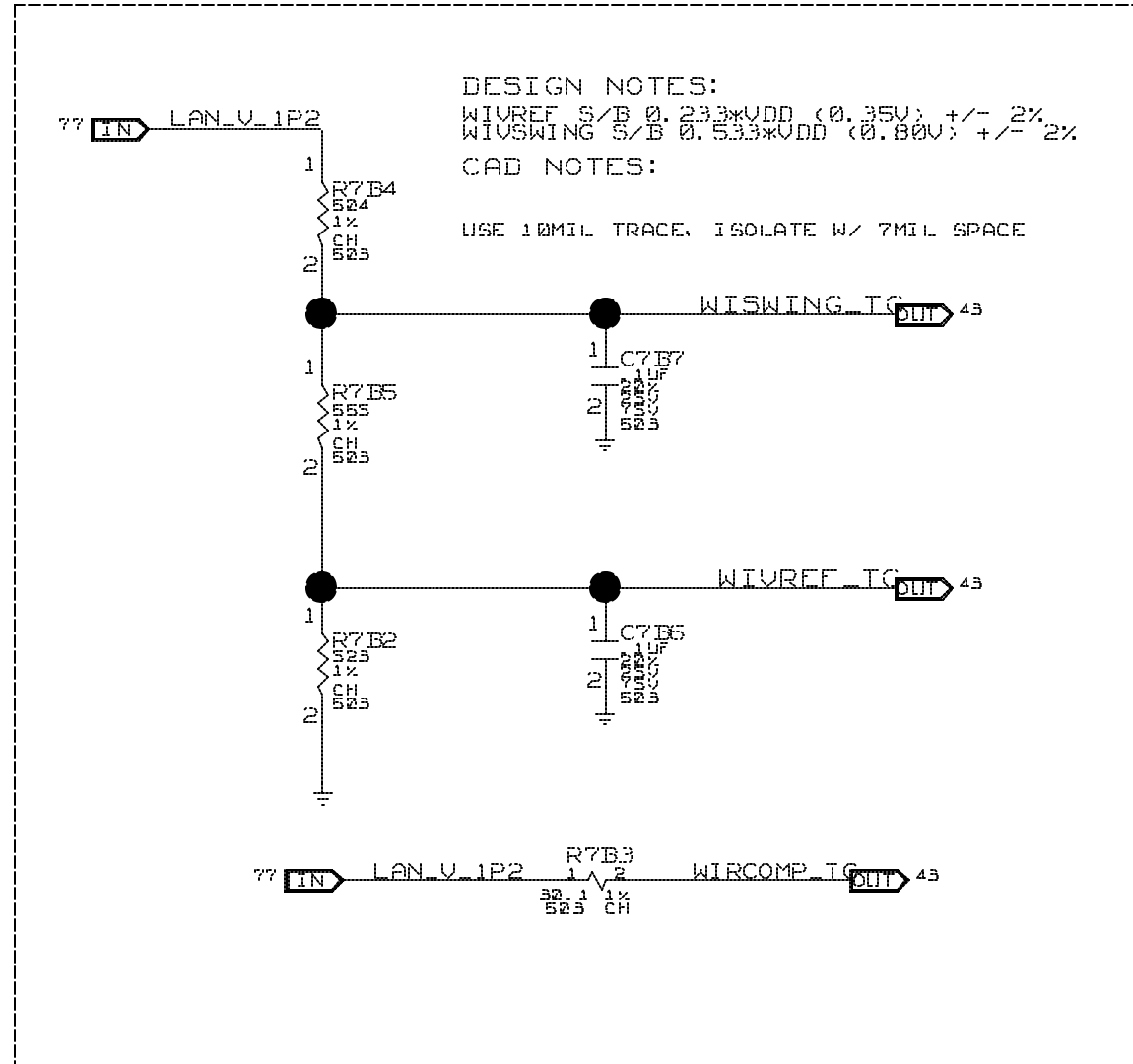


SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: LAN CONNECTOR/DECOUPLING		SHEET:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:27:00 2003	46

DRAWING

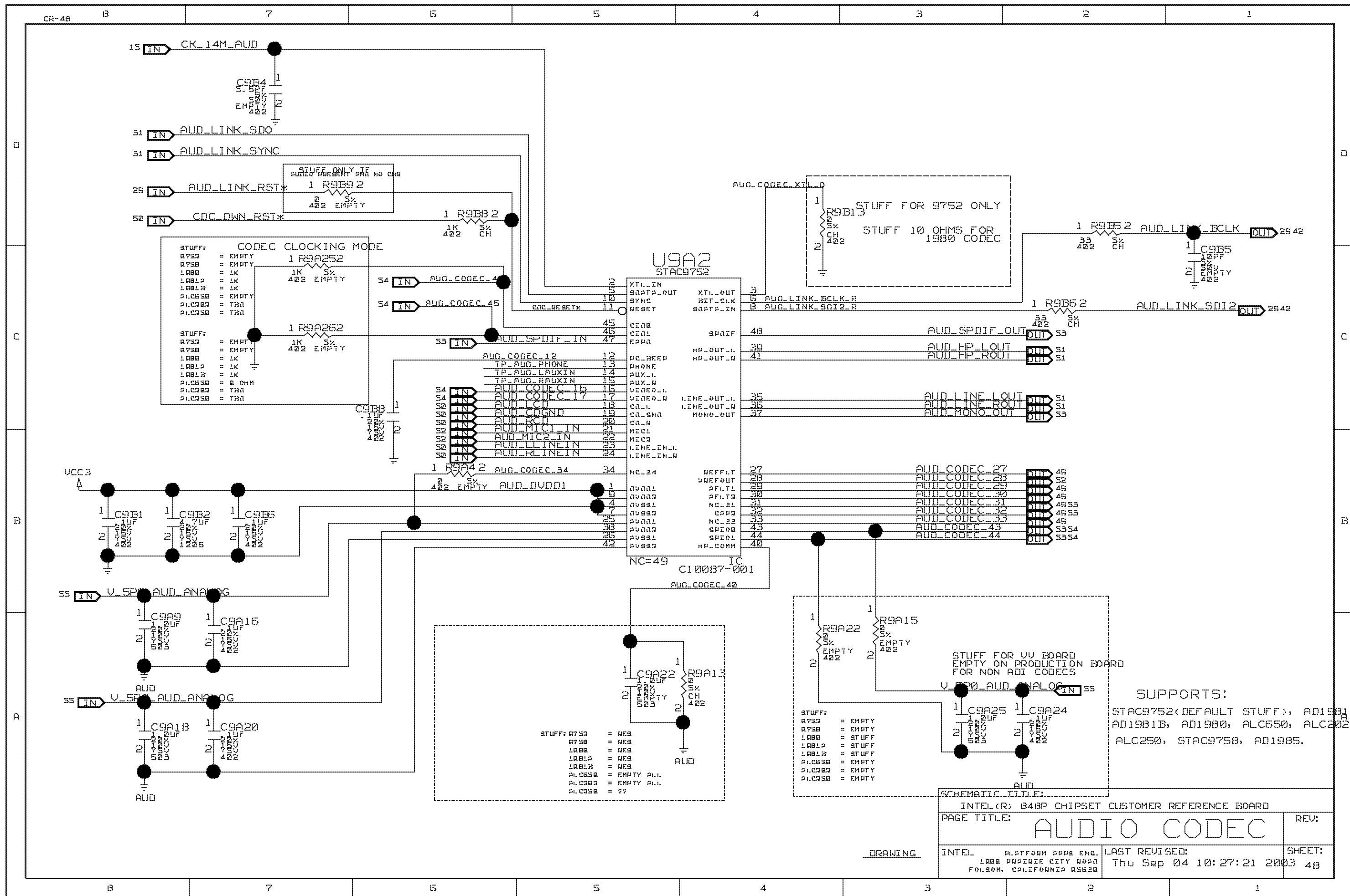
# LAN MCH

## CSA INTERFACE REFERENCE CSA INTERFACE REFERENCE



DRAWING

SCHEMATIC TITLE: INTEL(R) 848P CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: <b>CSA INTERFACE REFERENCE</b>	REV:
INTEL PLATFORM APPS ENG. 1800 BRANIFF CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:27:01 2003
SHEET:	



**CODEC CLOCKING MODE**

STUFF: R752 = EMPTY, R758 = EMPTY, L888 = 1K, L881A = 1K, L881B = 1K, P1C658 = EMPTY, P1C287 = TRN, P1C258 = TRN

1 R9A252  
1K 422 5K EMPTY

STUFF: R752 = EMPT, R758 = EMPTY, L888 = 1K, L881A = 1K, L881B = 1K, P1C658 = 0 OHM, P1C287 = TRN, P1C258 = TRN

1 R9A262  
1K 422 5K EMPTY

STUFF: R752 = RES, R758 = RES, L888 = STUFF, L881A = RES, L881B = STUFF, P1C658 = EMPTY P.L., P1C287 = EMPTY P.L., P1C258 = ??

STUFF: R752 = EMPTY, R758 = EMPTY, L888 = STUFF, L881A = STUFF, L881B = STUFF, P1C658 = EMPTY, P1C287 = EMPTY, P1C258 = EMPTY

**SUPPORTS:**  
 STAC9752 (DEFAULT STUFF), AD1981A, AD1981B, AD1980, ALC650, ALC202, ALC250, STAC9758, AD1985.

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD

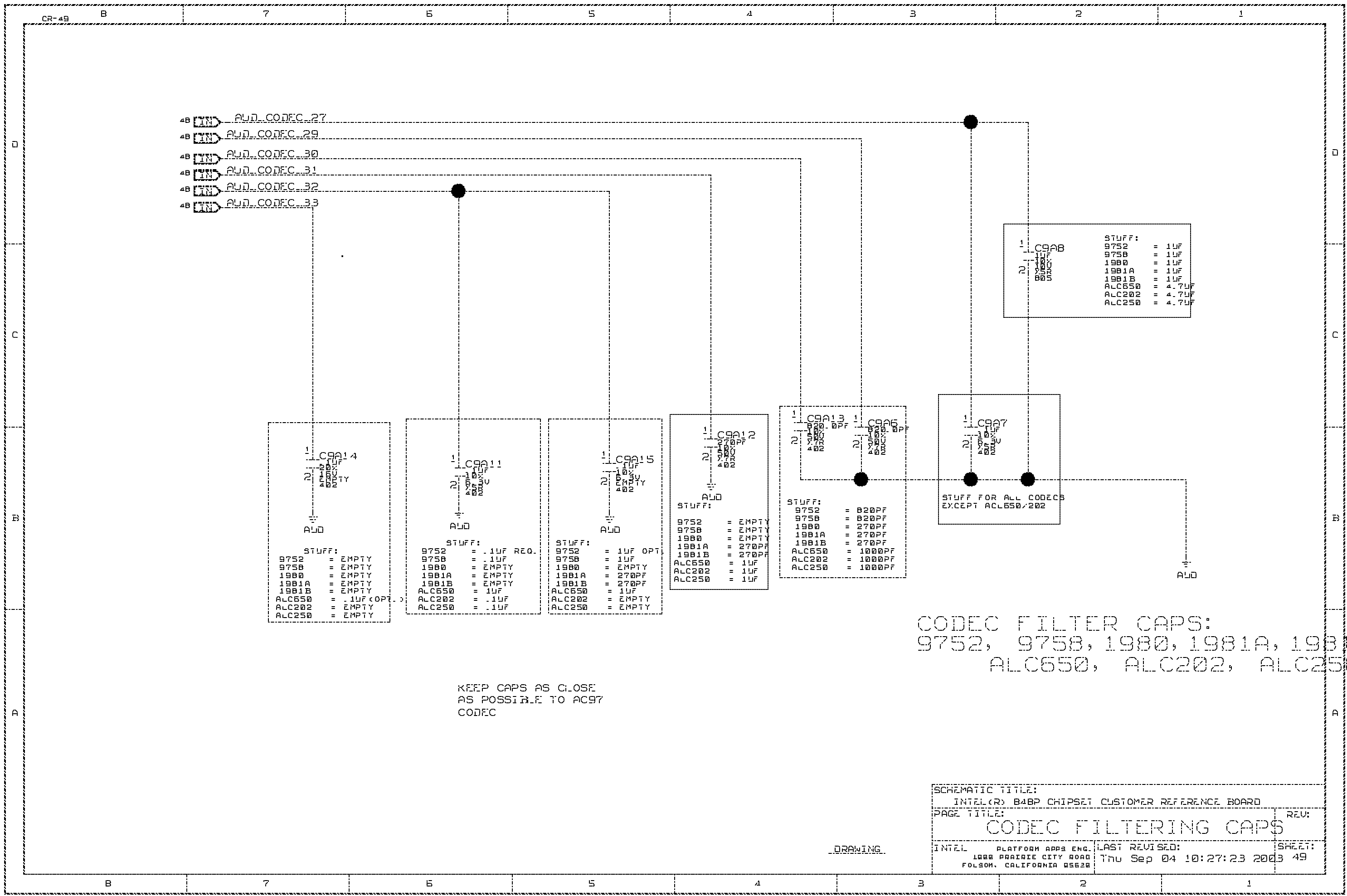
PAGE TITLE: **AUDIO CODEC**

INTEL PLATFORM APPS ENG. 1800 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630

LAST REVISED: Thu Sep 04 10:27:21 2003

REV: SHEET: 4/3

DRAWING



4B IN AUD\_CODEC\_27  
 4B IN AUD\_CODEC\_29  
 4B IN AUD\_CODEC\_30  
 4B IN AUD\_CODEC\_31  
 4B IN AUD\_CODEC\_32  
 4B IN AUD\_CODEC\_33

1 C9A8  
 1 100PF  
 1 100PF  
 2 100PF  
 2 100PF  
 2 100PF  
 2 100PF

STUFF:  
 9752 = 1UF  
 9758 = 1UF  
 1980 = 1UF  
 1981A = 1UF  
 1981B = 1UF  
 ALC650 = 4.7UF  
 ALC202 = 4.7UF  
 ALC250 = 4.7UF

1 C9A14  
 1 100PF  
 2 100PF  
 2 100PF

AUD

STUFF:  
 9752 = EMPTY  
 9758 = EMPTY  
 1980 = EMPTY  
 1981A = EMPTY  
 1981B = EMPTY  
 ALC650 = .1UF (OPT.)  
 ALC202 = EMPTY  
 ALC250 = EMPTY

1 C9A11  
 1 100PF  
 2 100PF  
 2 100PF

AUD

STUFF:  
 9752 = .1UF REQ.  
 9758 = .1UF  
 1980 = EMPTY  
 1981A = EMPTY  
 1981B = EMPTY  
 ALC650 = 1UF  
 ALC202 = .1UF  
 ALC250 = .1UF

1 C9A15  
 1 100PF  
 2 100PF  
 2 100PF

AUD

STUFF:  
 9752 = 1UF OPT.  
 9758 = 1UF  
 1980 = EMPTY  
 1981A = 270PF  
 1981B = 270PF  
 ALC650 = 1UF  
 ALC202 = EMPTY  
 ALC250 = EMPTY

1 C9A12  
 1 100PF  
 2 100PF  
 2 100PF

AUD

STUFF:  
 9752 = EMPTY  
 9758 = EMPTY  
 1980 = EMPTY  
 1981A = 270PF  
 1981B = 270PF  
 ALC650 = 1UF  
 ALC202 = 1UF  
 ALC250 = 1UF

1 C9A13  
 1 100PF  
 2 100PF  
 2 100PF

1 C9A6  
 1 100PF  
 2 100PF  
 2 100PF

STUFF:  
 9752 = 820PF  
 9758 = 820PF  
 1980 = 270PF  
 1981A = 270PF  
 1981B = 270PF  
 ALC650 = 1000PF  
 ALC202 = 1000PF  
 ALC250 = 1000PF

1 C9A7  
 1 100PF  
 2 100PF  
 2 100PF

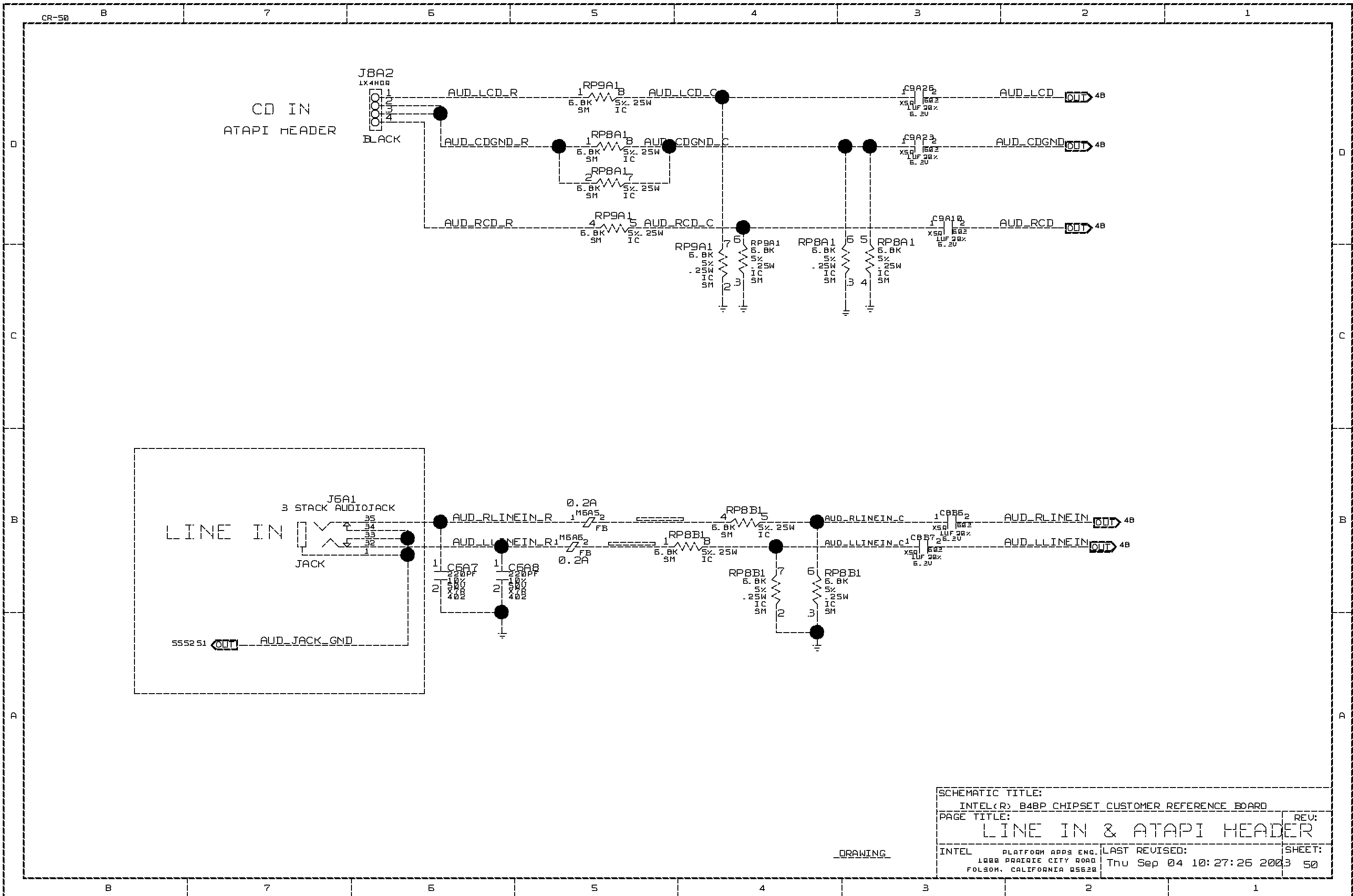
STUFF FOR ALL CODECS  
 EXCEPT ALC650/202

CODEC FILTER CAPS:  
 9752, 9758, 1980, 1981A, 1981B,  
 ALC650, ALC202, ALC250

KEEP CAPS AS CLOSE  
 AS POSSIBLE TO AC97  
 CODEC

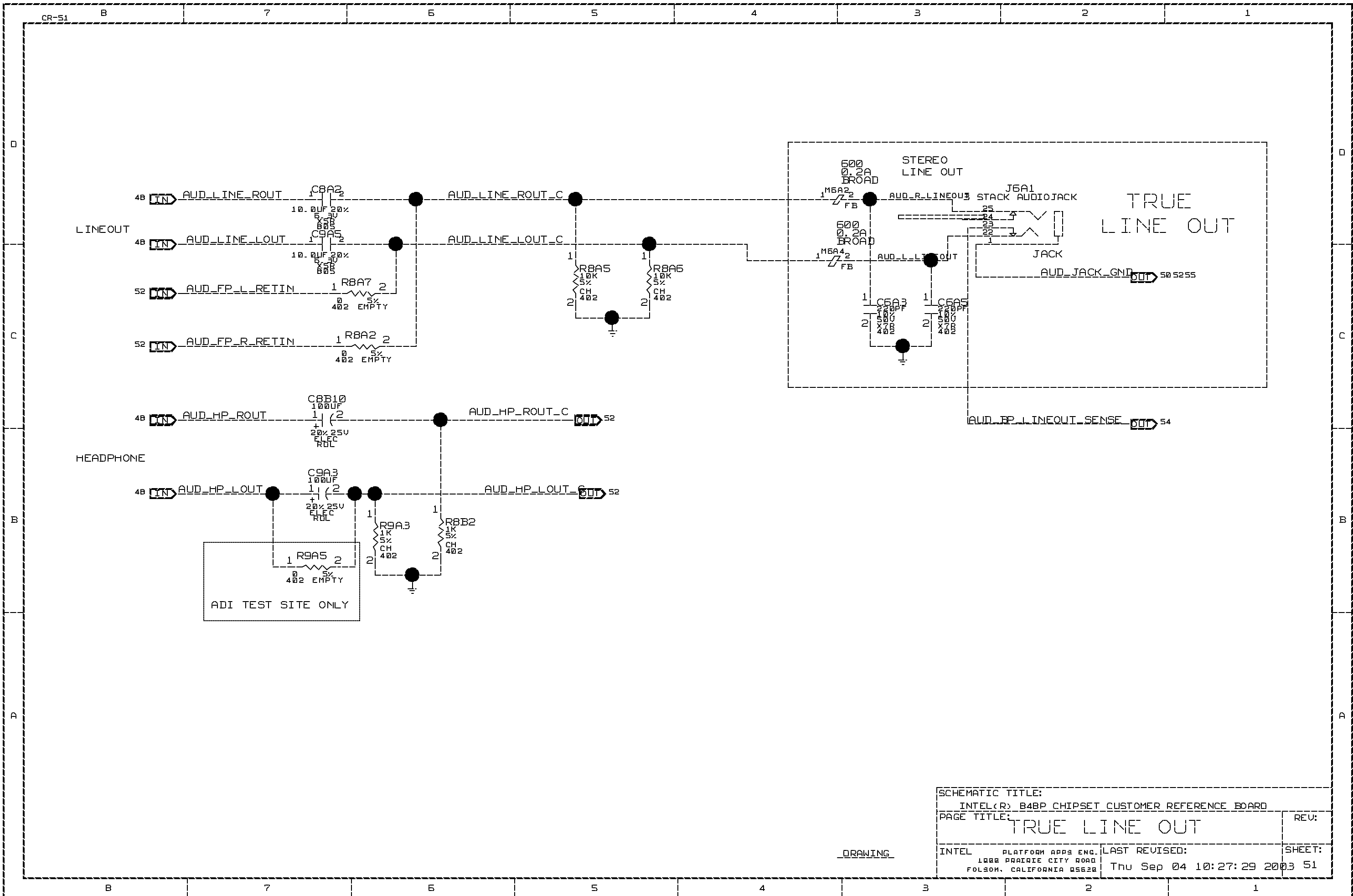
DRAWING

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: CODEC FILTERING CAPS		SHEET:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:27:23 2003 49	



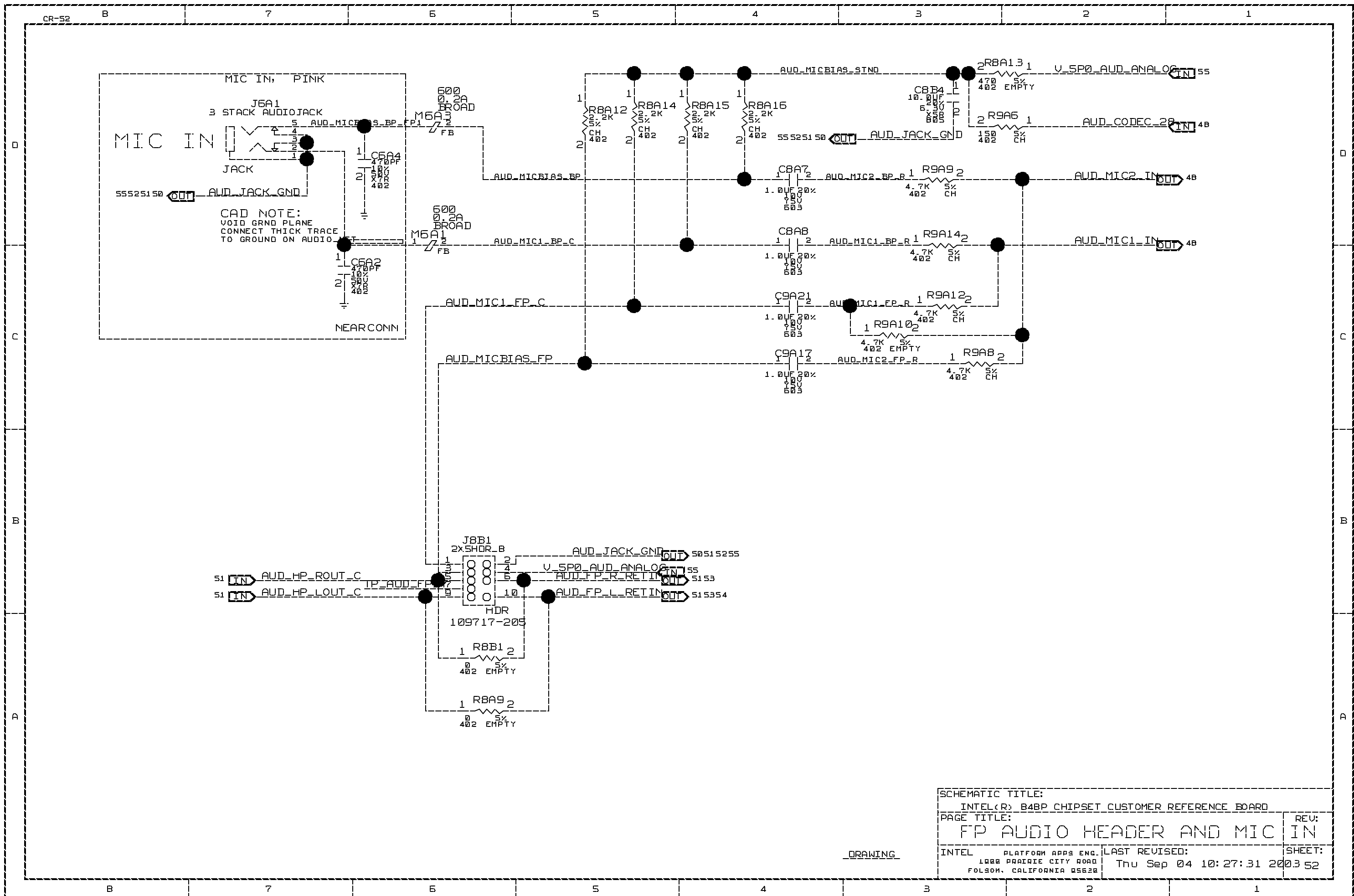
SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		LINE IN & ATAPI HEADER	
INTEL PLATFORM APPS ENG.		LAST REVISED:	
1000 PRAIRIE CITY ROAD		Thu Sep 04 10:27:26 2003	
FOLSOM, CALIFORNIA 95620		SHEET: 50	

DRAWING



SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		TRUE LINE OUT	
INTEL PLATFORM APPS ENG.		LAST REVISED:	
1000 PRAIRIE CITY ROAD		Thu Sep 04 10:27:29 2003 51	
FOLSOM, CALIFORNIA 95620		SHEET:	

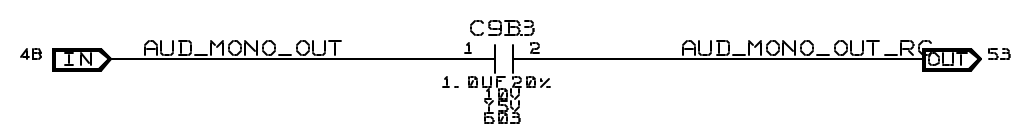
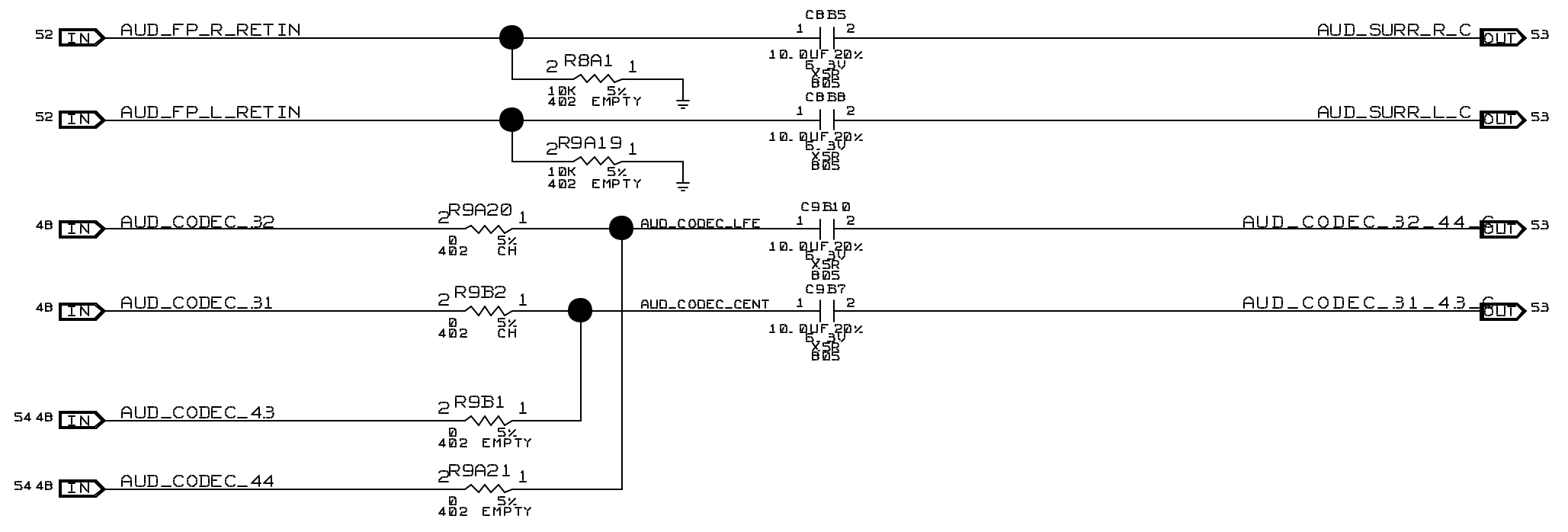
DRAWING



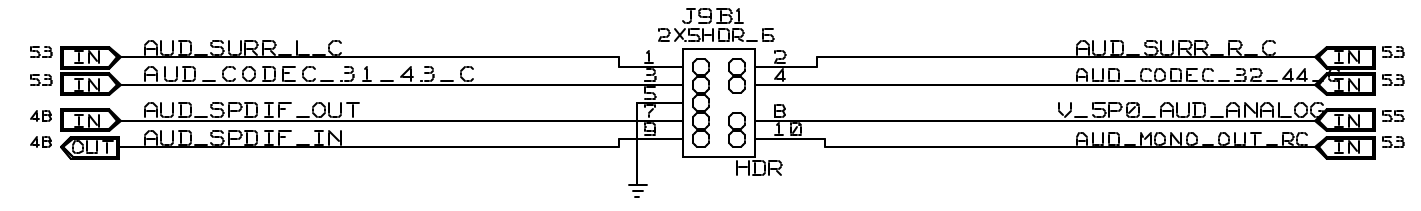
SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		FP AUDIO HEADER AND MIC IN	
INTEL PLATFORM APPS ENG.		LAST REVISED:	REV:
1000 PRAIRIE CITY ROAD		Thu Sep 04 10:27:31 2003	52
FOLSOM, CALIFORNIA 95620		SHEET:	

DRAWING





### 6 CHANNEL AUDIO HEADER

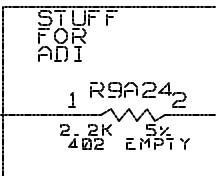


SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		AUDIO OUTPUTS/6 CHANNEL HEADER	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620		LAST REVISED: Thu Sep 04 10:27:33 2003	SHEET: 53

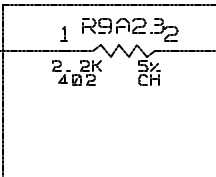
DRAWING

# LINE OUT JACK SENSING

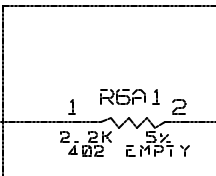
51 IN AUD\_BP\_LINEOUT\_SENSE



AUD\_CODEC\_17 OUT 4B



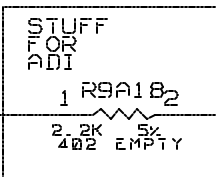
AUD\_CODEC\_43 OUT 4B53



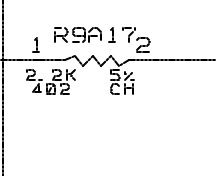
AUD\_CODEC\_45 OUT 4B

# HEADPHONE JACK SENSING

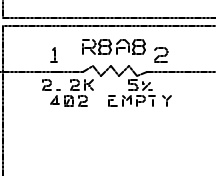
52 IN AUD\_FP\_L\_RETIN



AUD\_CODEC\_16 OUT 4B



AUD\_CODEC\_44 OUT 4B53



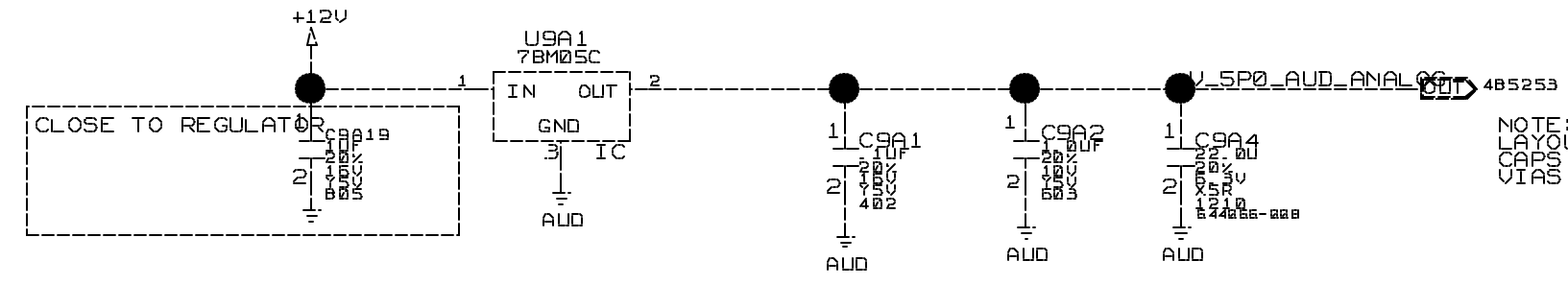
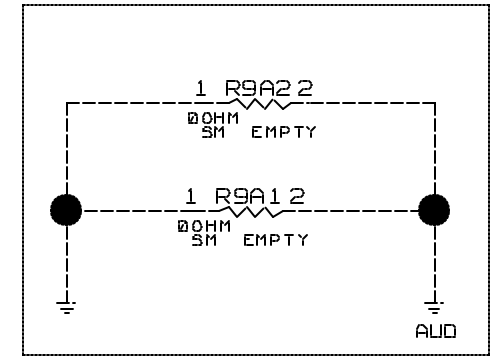
AUD\_CODEC\_46 OUT 4B

DRAWING

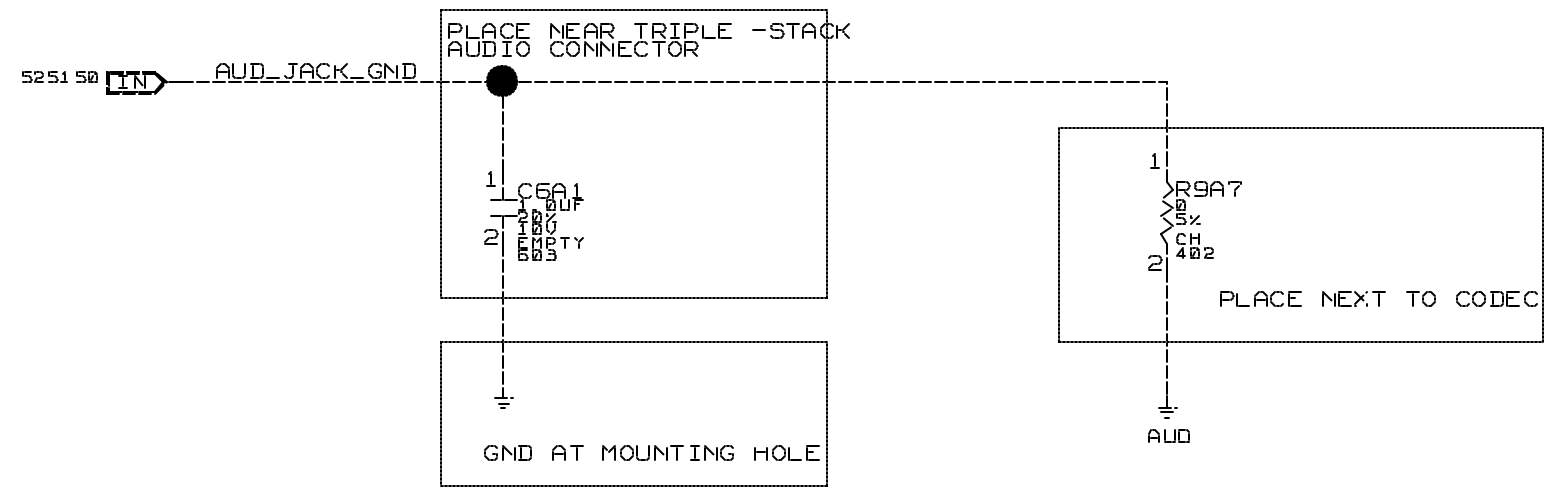
SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		AUDIO JACK SENSING	REV:
INTEL	PLATFORM APPS ENG.	LAST REVISED:	SHEET:
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FOLSOM, CALIFORNIA 95620			

PLACE IN TOP LEFT CORNER OF BOARD

REGULATOR THERMAL TAB SHOULD BE SOLDERED TO A COPPER PAD THAT IS LARGE ENOUGH TO ALLOW 5 TO 10 GROUND VIAS AROUND THE COMPONENT FOR COOLING



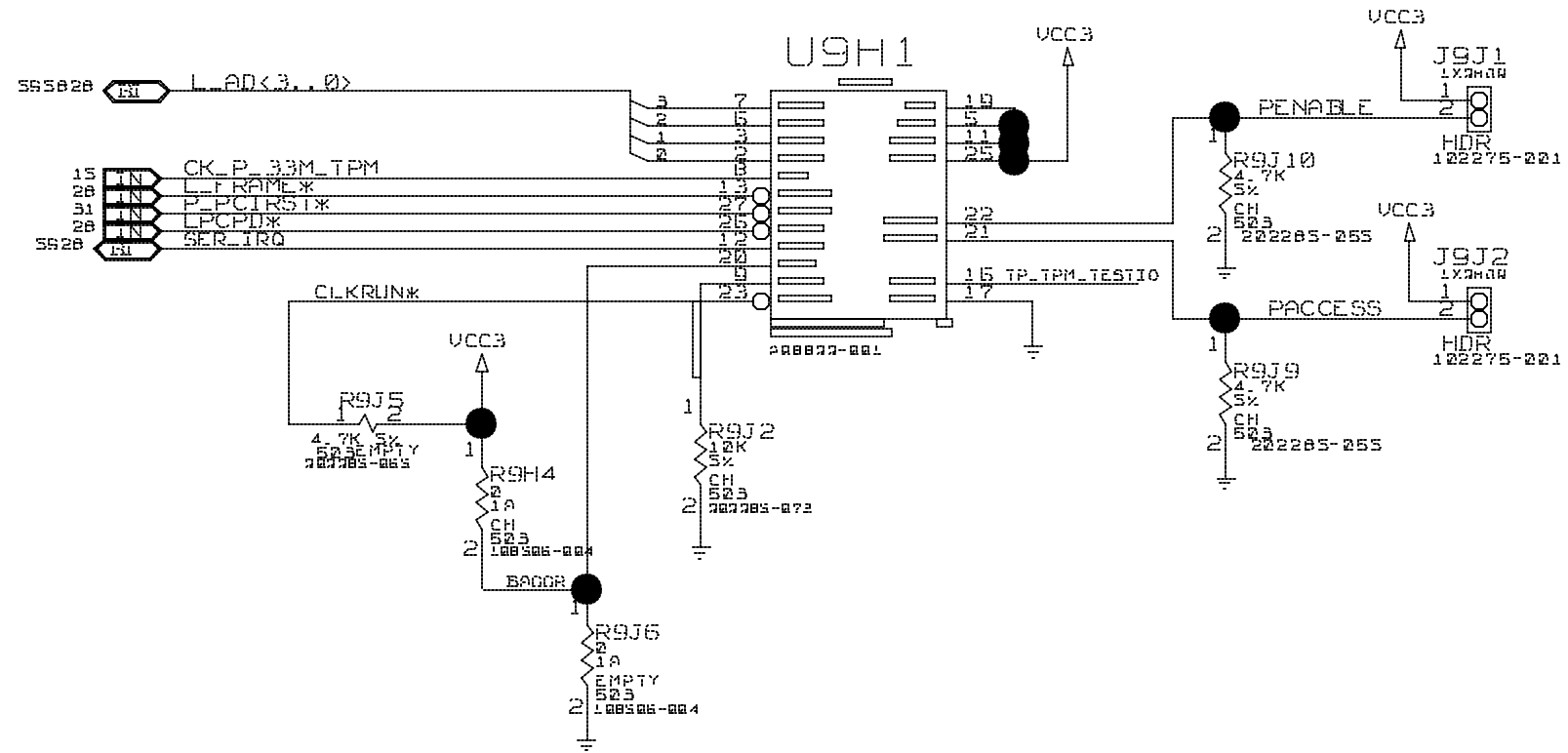
NOTE: LAYOUT SHOULD GO FROM PIN 2 TO CAPS AND THEN THROUGH SEVERAL VIAS TO V\_5P0\_AUD\_ANALOG



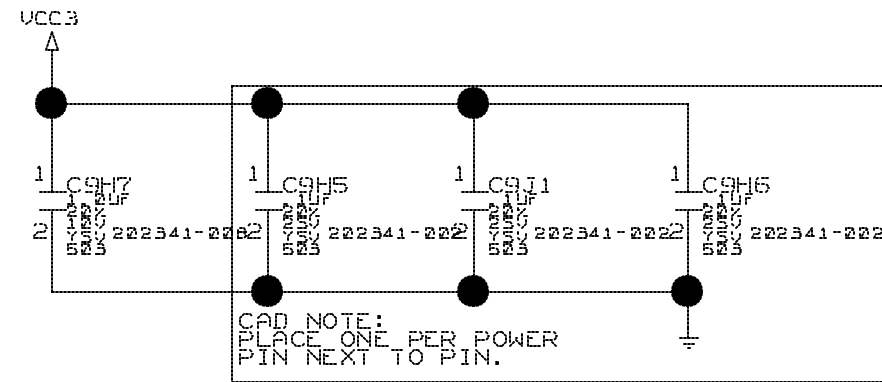
SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		AUDIO VREG	
INTEL PLATFORM APPS ENG.		LAST REVISED:	
1000 PRAIRIE CITY ROAD		Thu Sep 04 10:27:37 2003	
FOLSOM, CALIFORNIA 95620		SHEET: 55	

DRAWING

# SECURITY: TPM (TRUSTED PLATFORM MODULE)



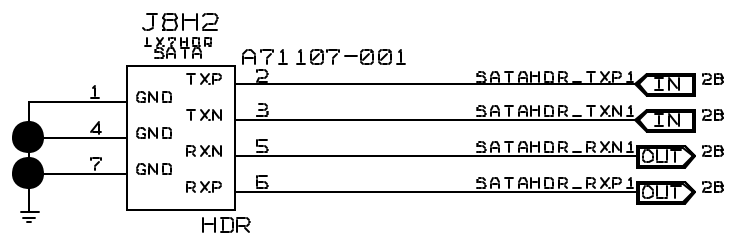
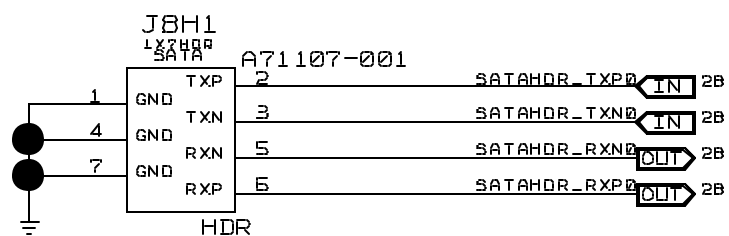
CAD NOTE:  
 CK\_P\_33M\_TPM SHOULD  
 HAVE 20MIL SPACING  
 P\_PCIRST\* SHOULD  
 HAVE 20 MIL SPACING  
 LAD<3..0> HAS 5 MIL  
 SPACING BETWEEN OTHER LAD  
 SIGNALS, BUT 10 MILS TO ALL  
 OTHER SIGNALS.



CAD NOTE:  
 PLACE ONE PER POWER  
 PIN NEXT TO PIN.

SCHEMATIC TITLE: INTEL(R) 848P CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: TPM (TRUSTED PLATFORM MODULE)		SHEET:
INTEL PLATFORM APPS ENG. 1888 BRANIFF CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:27:39 2003	55

DRAWING



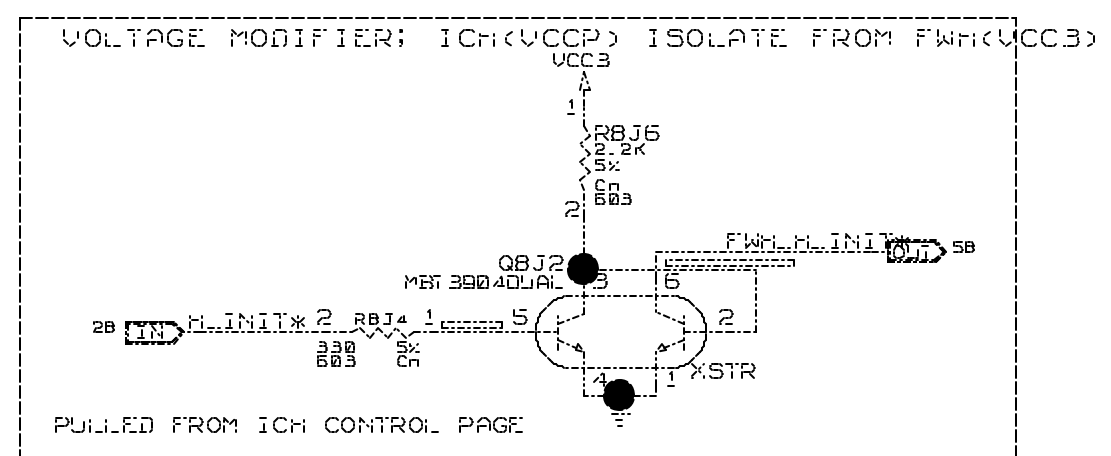
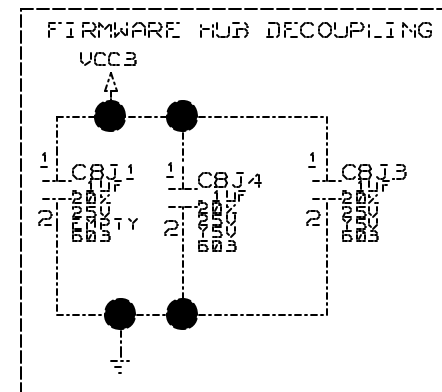
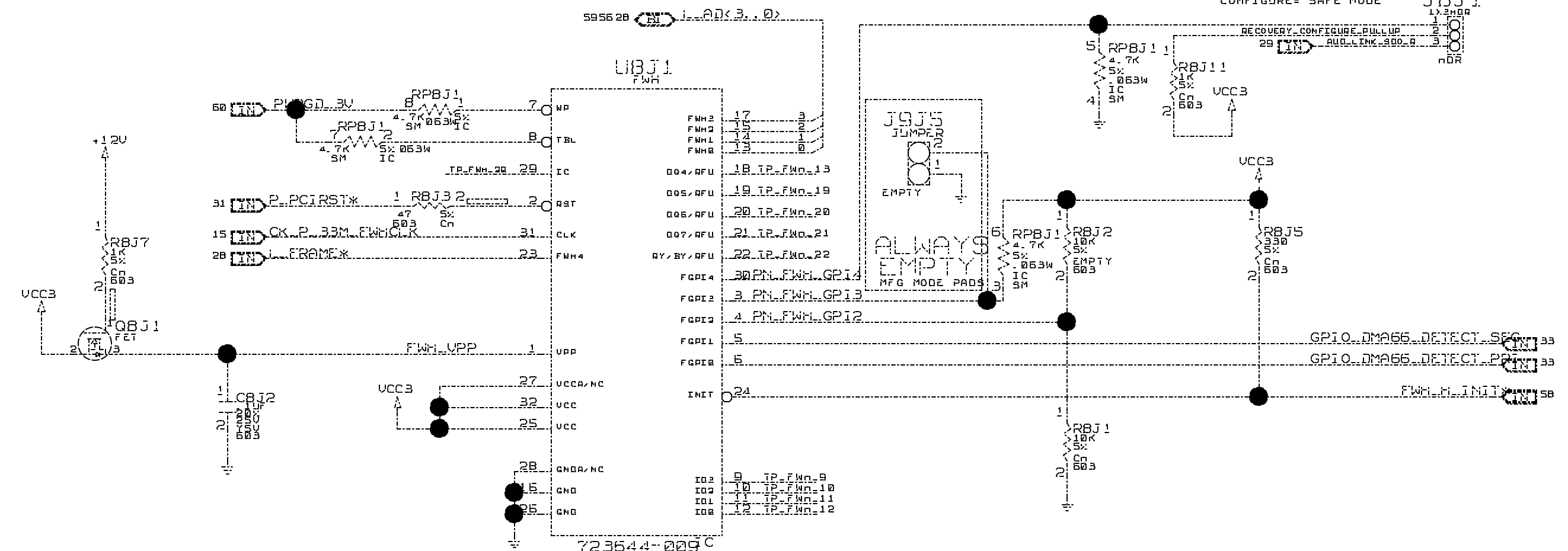
DRAWING

SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		SATA CONNECTORS	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620		LAST REVISED: Thu Sep 04 10:27:41 2003	SHEET: 03 57

RECOVER/CONFIGURE HEADERS	
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

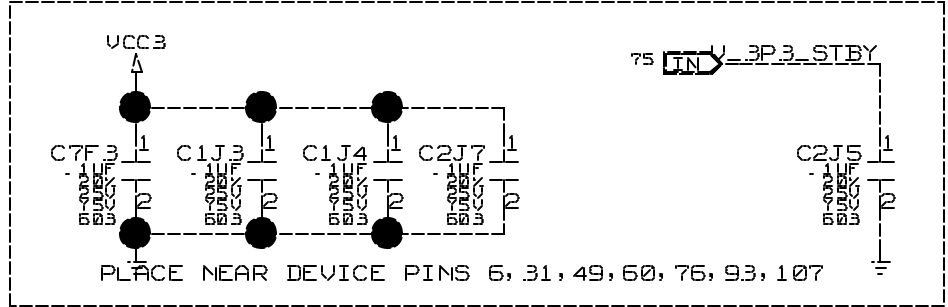
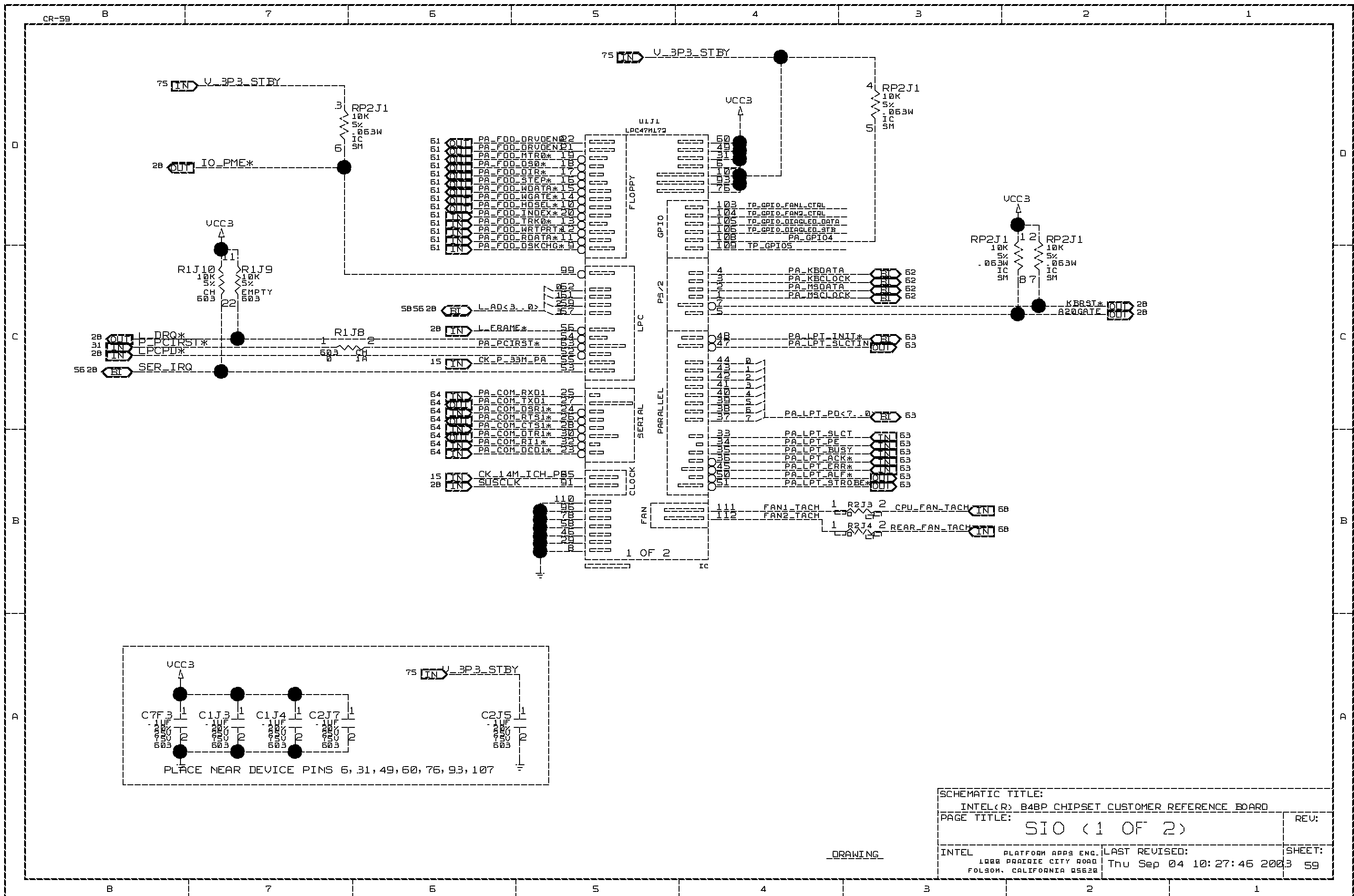
CONFIGURE= SAFE MODE

JBJ1



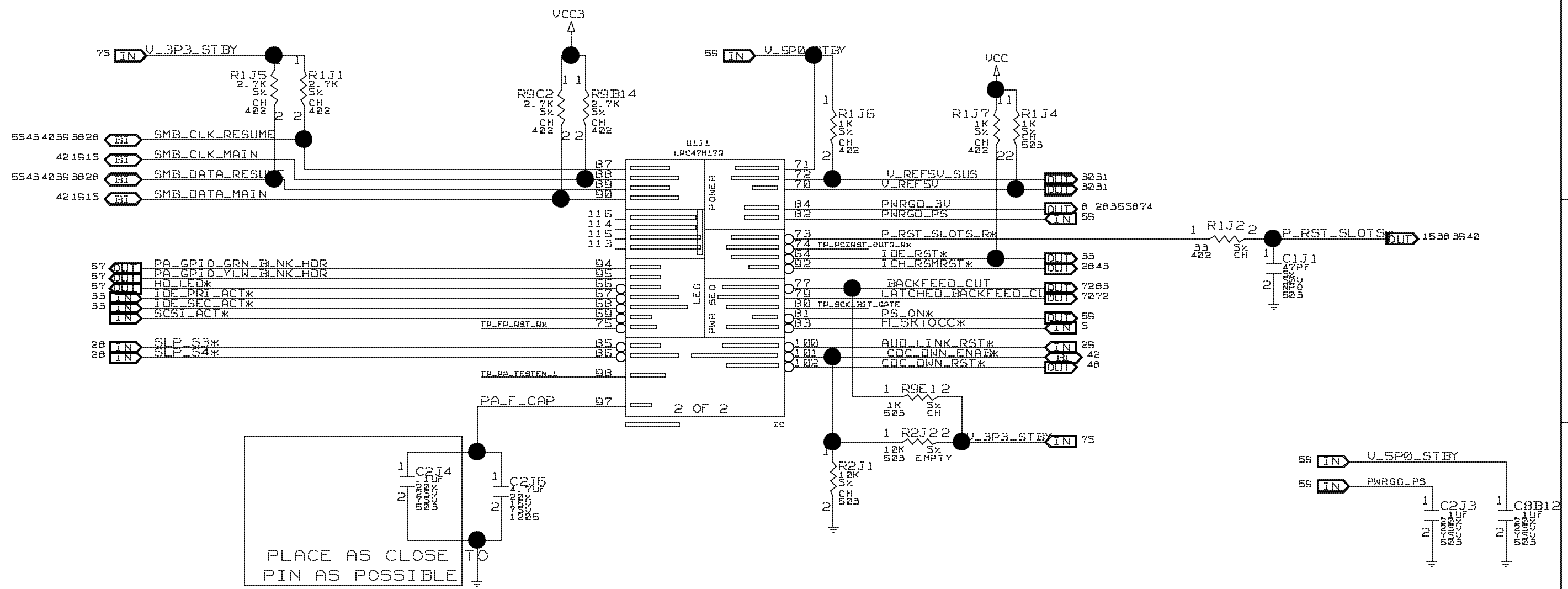
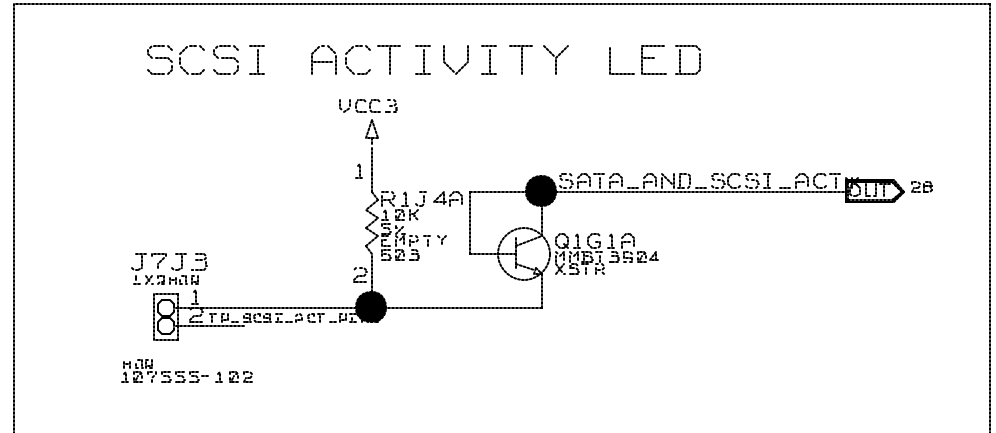
SCHEMATIC TITLE:	
INTEL(R) BABP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:	REV:
FIRMWARE HUB	
INTEL PLATFORM APPS ENG.	LAST REVISED:
1000 PRAIRIE CITY ROAD	Thu Sep 04 10:27:44 2003
FOLSOM, CALIFORNIA 95620	SHEET: 58

DRAWING



SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		SIO (1 OF 2)	
INTEL		PLATFORM APPS ENG.	LAST REVISED:
1000 PRAIRIE CITY ROAD		Thu Sep 04 10:27:46 2003	
FOLSOM, CALIFORNIA 95630		SHEET: 59	

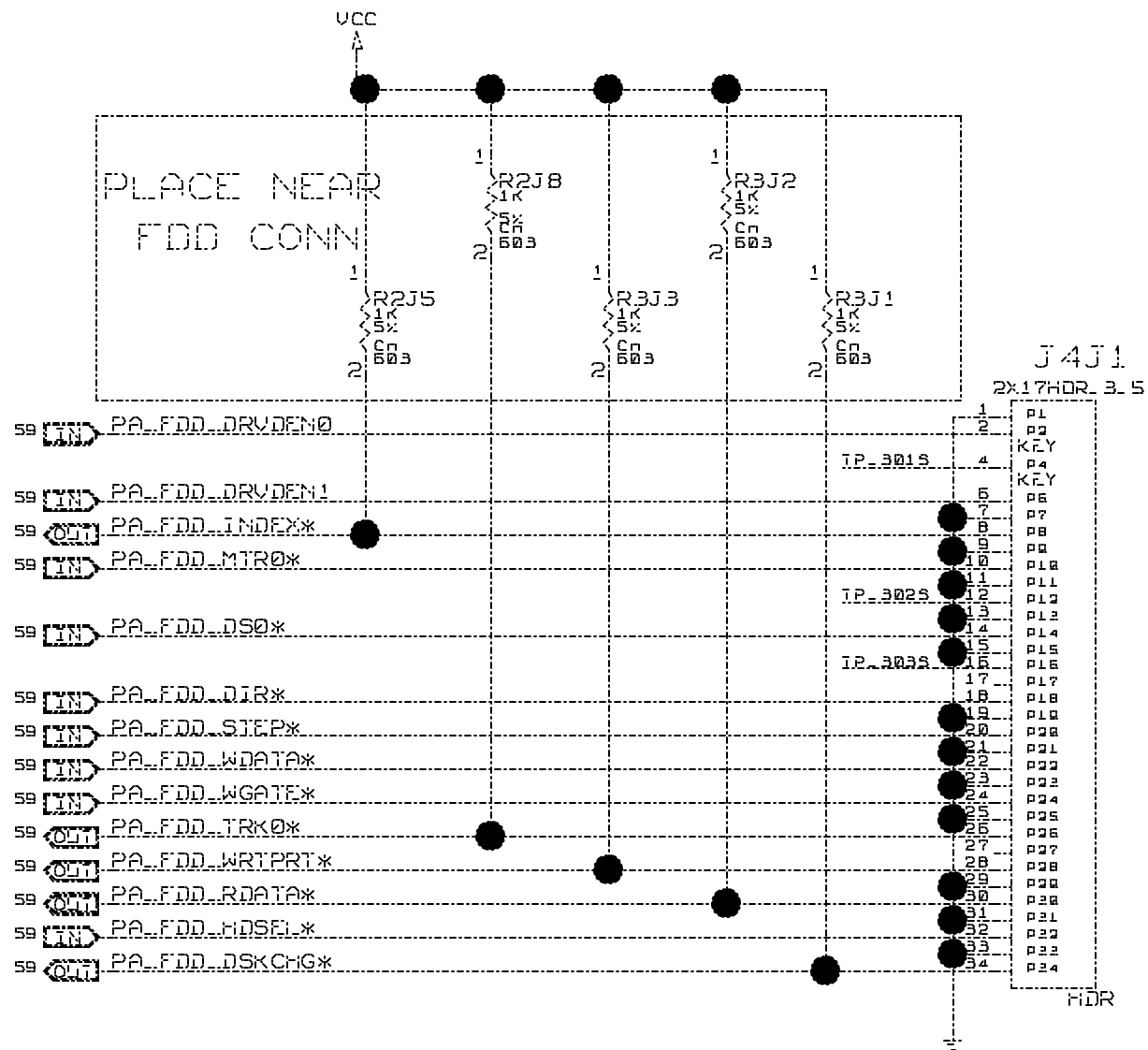
DRAWING



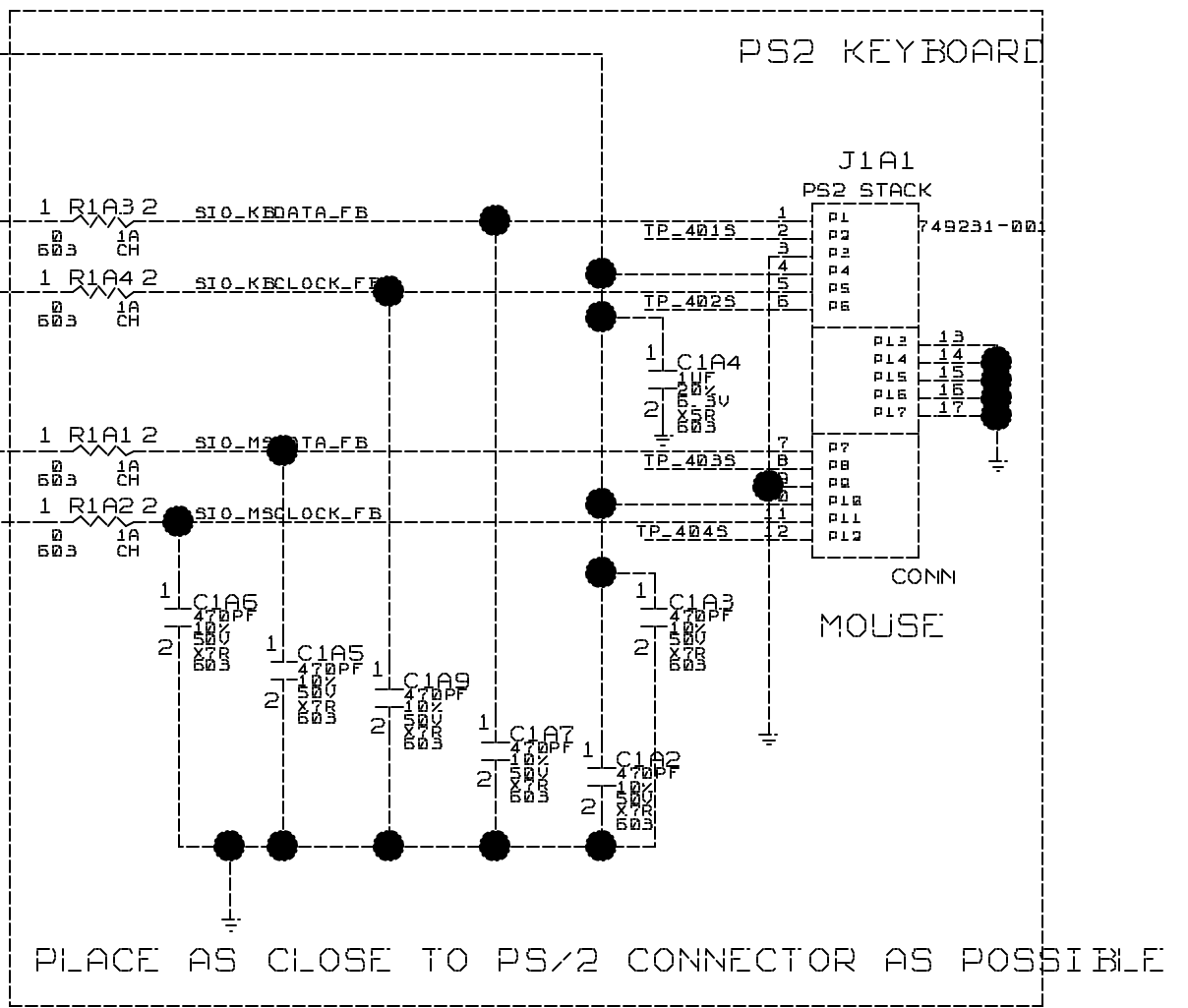
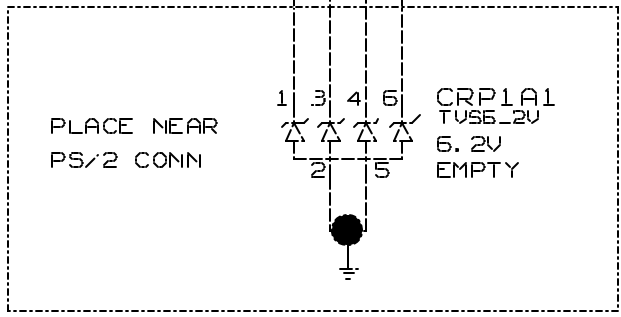
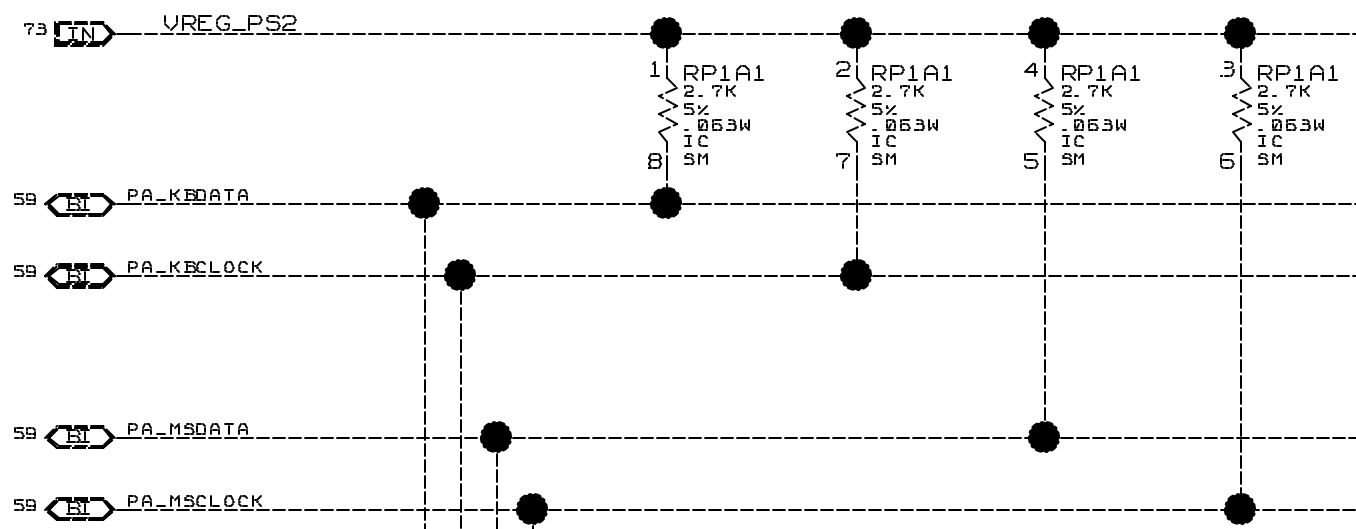
SCHEMATIC TITLE:		INTEL(R) 848P CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		SIO (2 OF 2)	
INTEL PLATFORM APPS ENG. 1800 BRANIFF CITY ROAD FOLSOM, CALIFORNIA 95620		LAST REVISED: Thu Sep 04 10:27:48 2003	REV: SHEET: 60

DRAWING



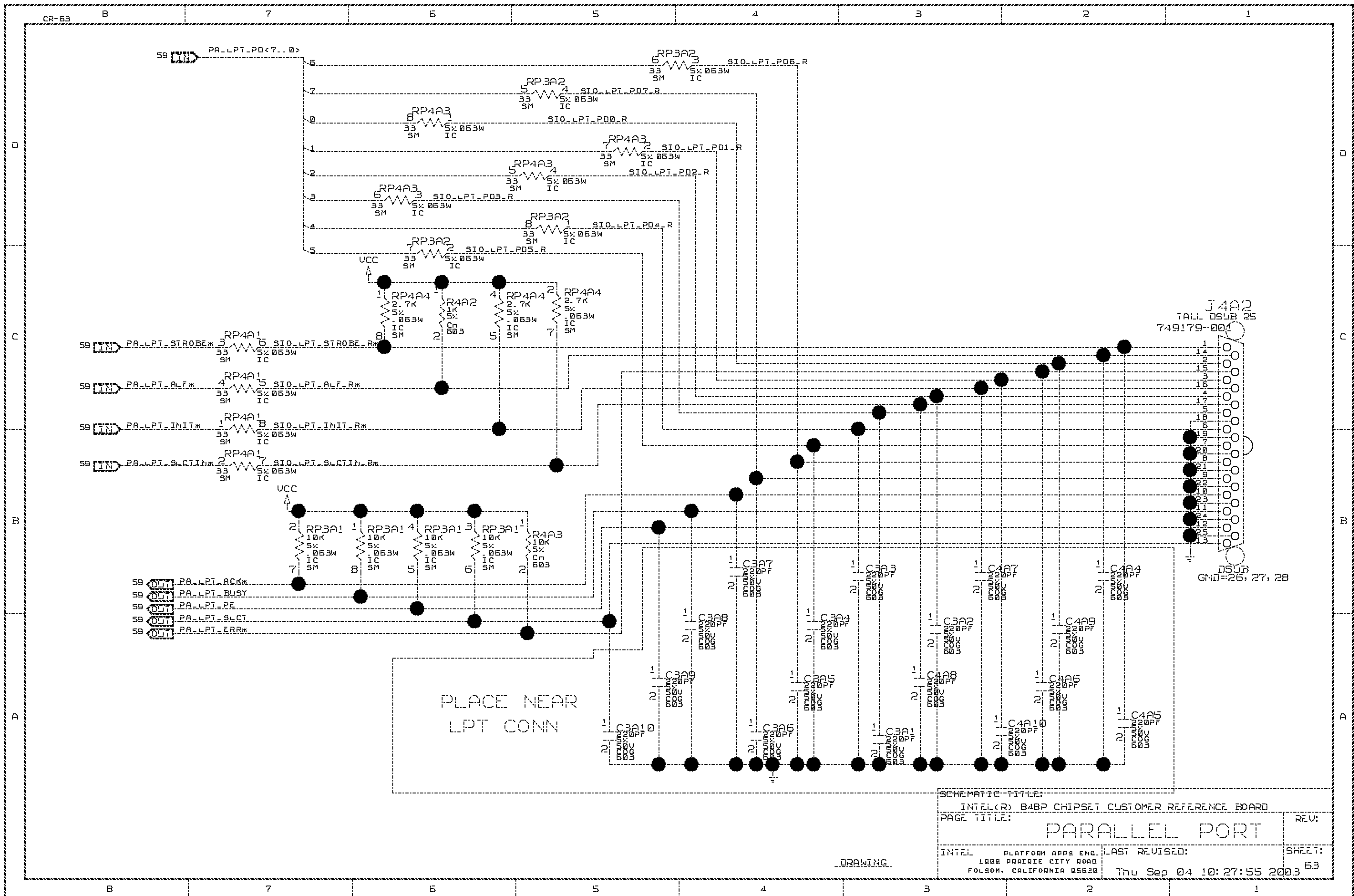


SCHEMATIC TITLE:		INTEL(R) BABP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		FLOPPY CONNECTOR	
DRAWING		INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:27:50 2003 61
		REV:	SHEET:

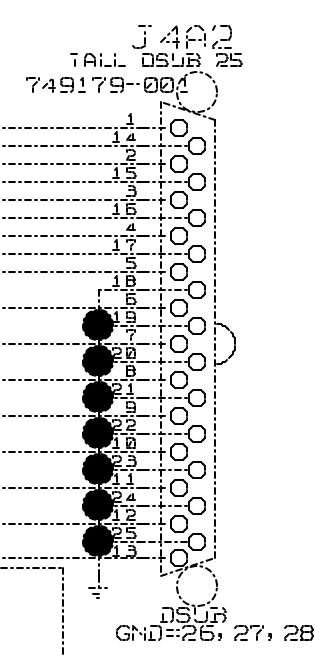
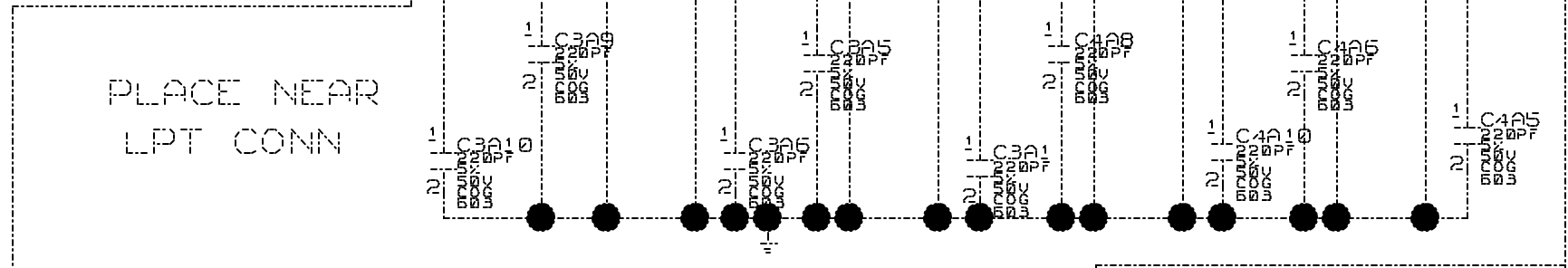
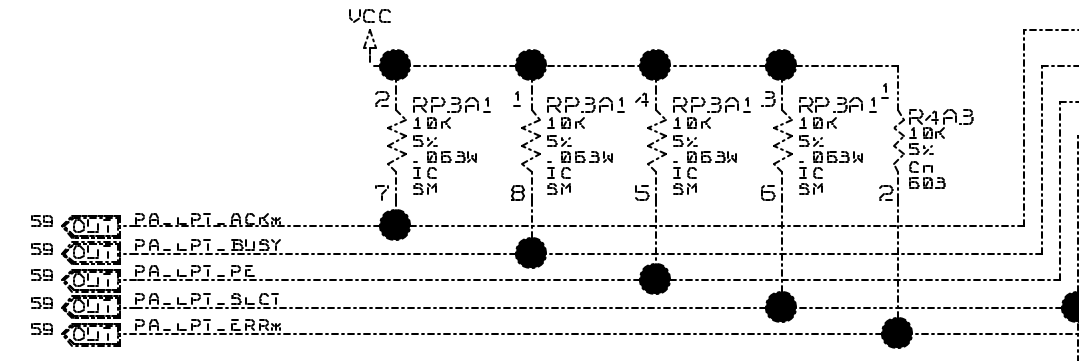
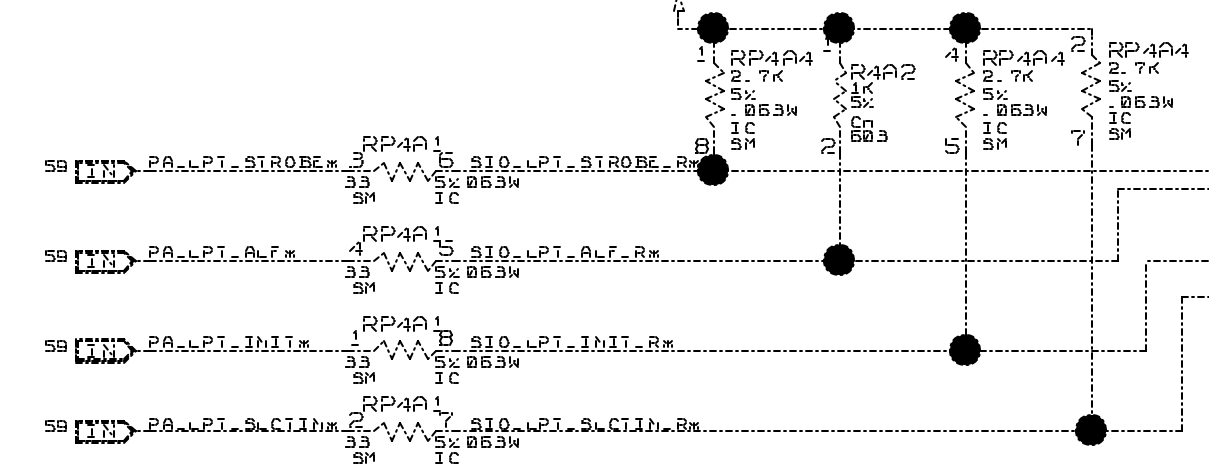
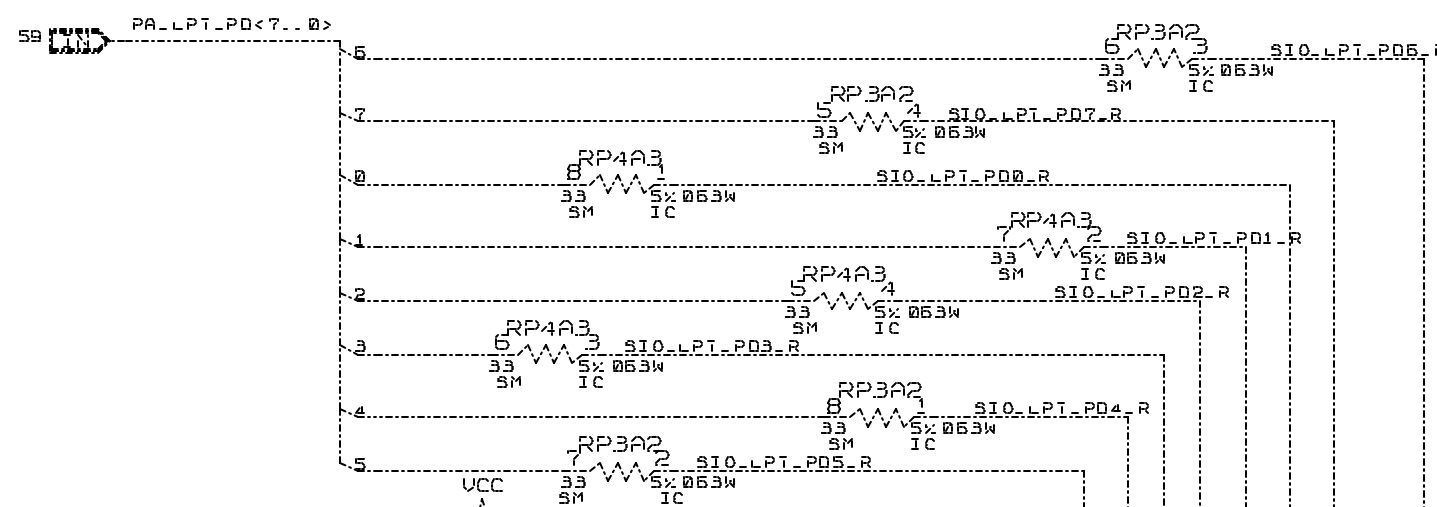


DRAWING

SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		ATX DOUBLE--STACKED	
INTEL PLATFORM APPS ENG.		LAST REVISED:	
1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620		Thu Sep 04 10:27:52 2003	
SHEET:		032	



CR-63 B 7 5 5 4 3 2 1

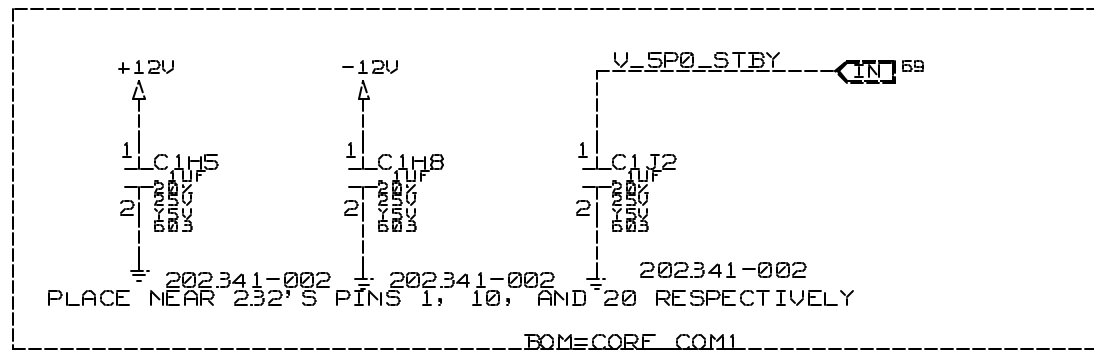
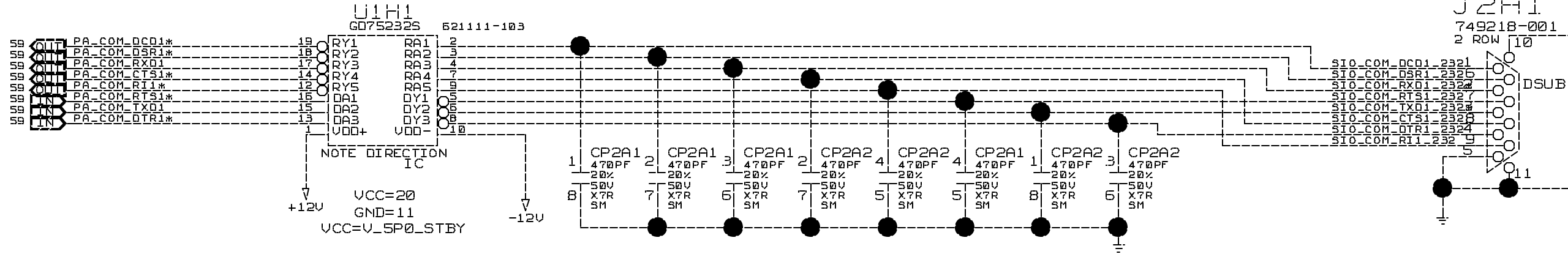


SCHEMATIC TITLE:		INTEL(R) BABP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		PARALLEL PORT	
DRAWING:		REV:	
INTEL PLATFORM APPS ENG. 1088 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620		LAST REVISED: Thu Sep 04 10:27:55 2003	
SHEET:		53	

B 7 5 5 4 3 2 1

DO NOT USE NATIONAL  
OR GOLDSTAR PARTS OF THIS  
BASE P/N

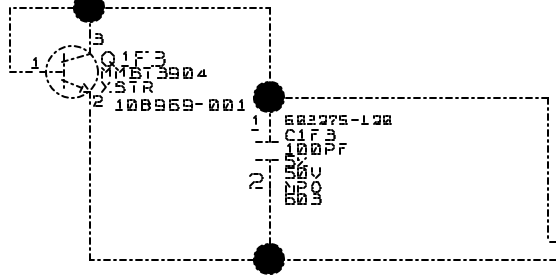
SERIAL PORT A  
J2A1  
749218-001  
2 ROW 10



SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: SERIAL PORT		SHEET:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: Thu Sep 04 10:27:59 2003 64

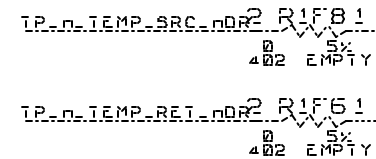
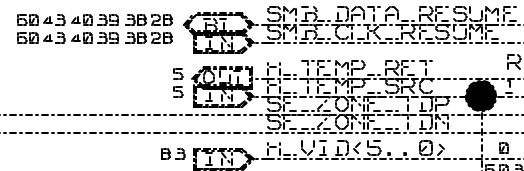
DRAWING

CAD NOTE:  
SOUTHEAST THERMAL ZONE SENSOR  
PLACE BELOW DIMMS

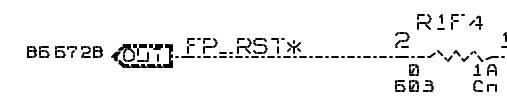


ALL STUFFED IF HECETA5  
ALL EMPTY IF HECETA4

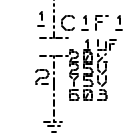
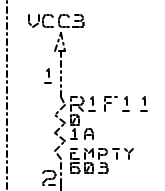
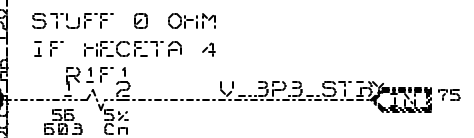
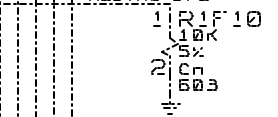
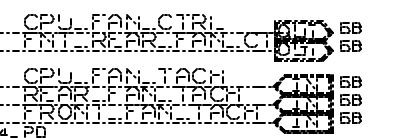
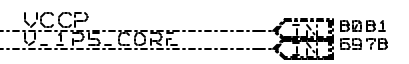
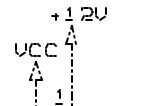
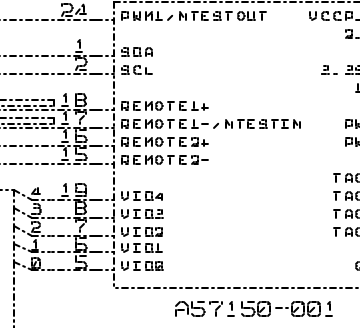
CAD NOTE:  
10MIL TRACE ON SE\_ZONE\_TDN AND TDP



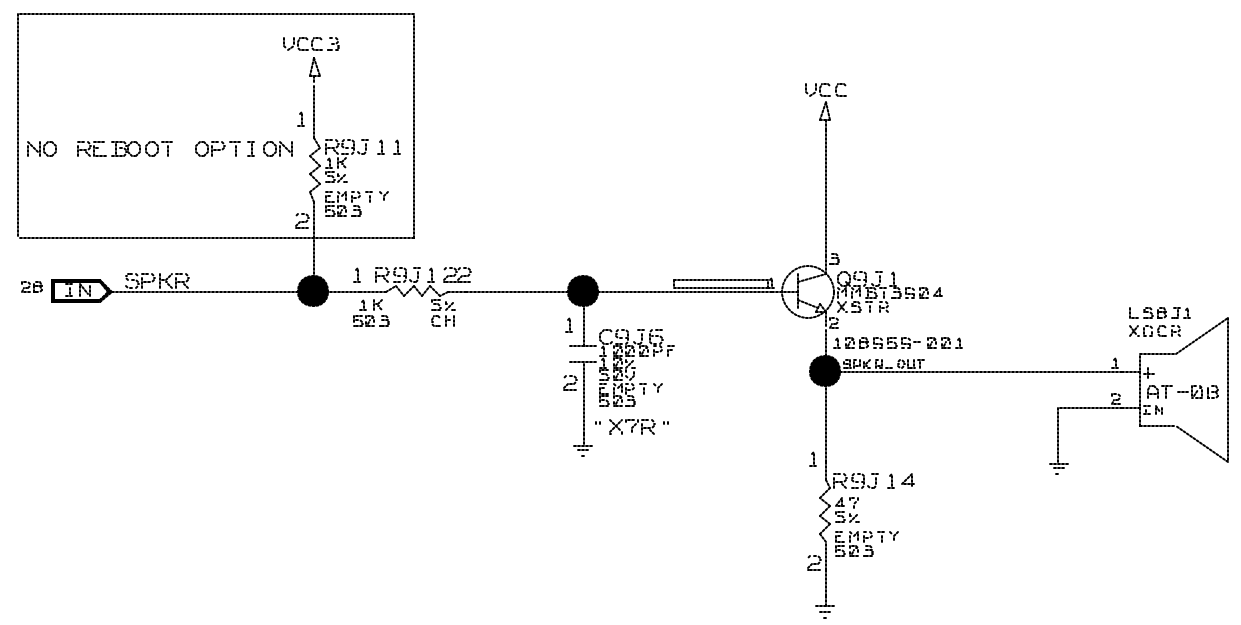
ALL STUFFED IF HECETA4  
ALL EMPTY IF HECETA5



PRELIMINARY  
U1F2  
HECETA5

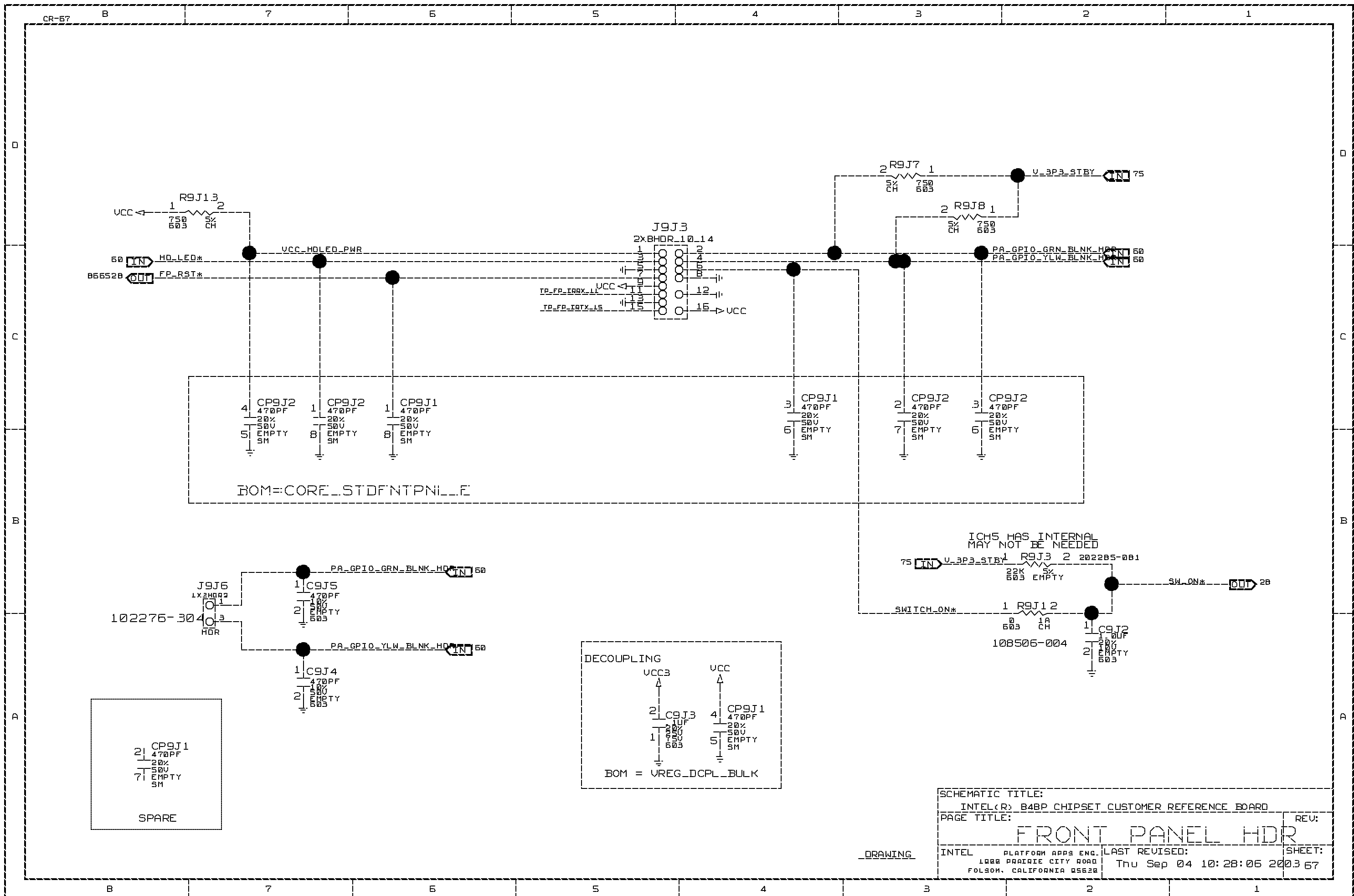


SCHEMATIC TITLE:		INTEL(R) BABP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		HECETA	
DRAWING:		LAST REVISED:	SHEET:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620		Thu Sep 04 10:28:01 2003	65



SCHEMATIC TITLE:		INTEL(R) 848P CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		SPEAKER	
INTEL PLATFORM APPS ENG. 1888 BRANNE CITY ROAD FOLSOM, CALIFORNIA 95620		LAST REVISED: Thu Sep 04 10:28:03 2003	REV: SHEET:

DRAWING



BOM=CORE\_STDFNTPNILL

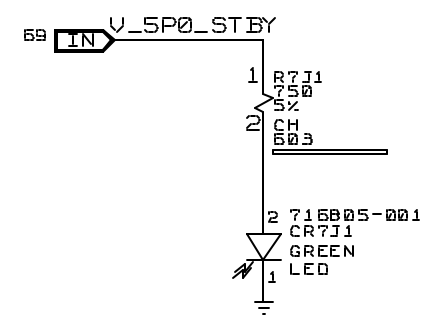
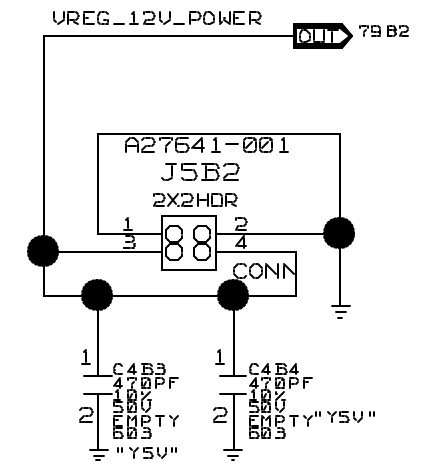
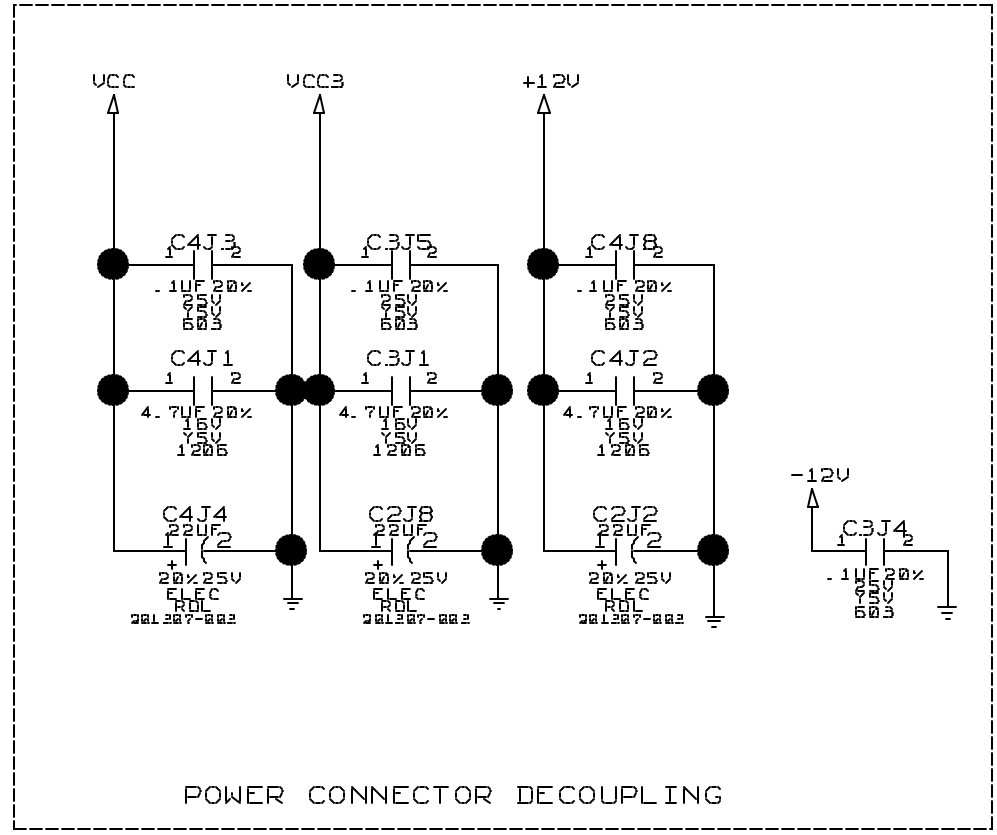
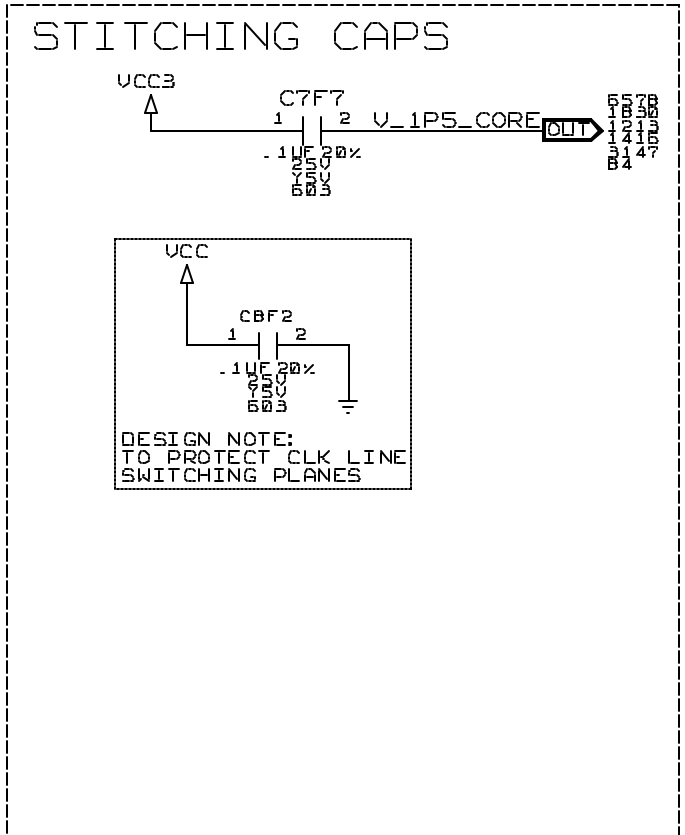
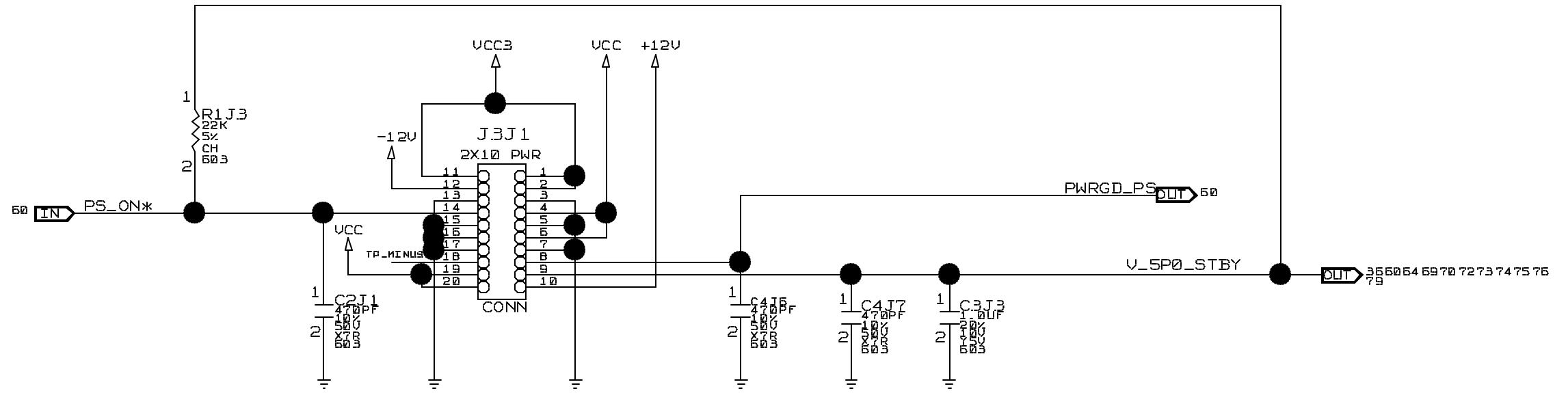
DECOUPLING  
 UCC3  
 UCC  
 C9J3  
 CP9J1  
 BOM = VREG\_DCPL\_BULK

CP9J1  
 470PF  
 20%  
 50V  
 EMPTY  
 SM  
 SPARE

SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		FRONT PANEL HDR	
DRAWING		LAST REVISED:	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620		Thu Sep 04 10:28:06 2003	03 67







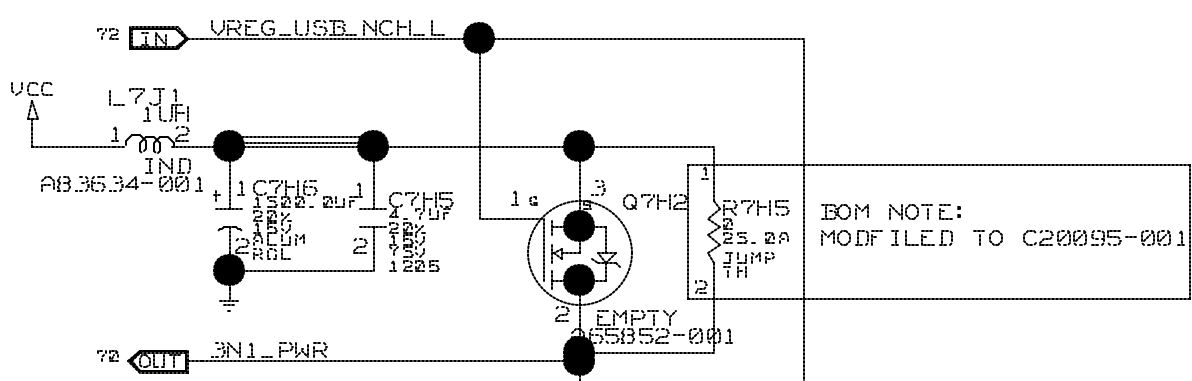
SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: STANDARD POWER CONNECTOR		SHEET:
DRAWING	INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:28:11 2009

CAD NOTE:  
 MAKE TRACE WIDTH 12 MILS  
 ON SC2614\_2  
 CONNECTED DOWNSTREAM OF VTT BULK

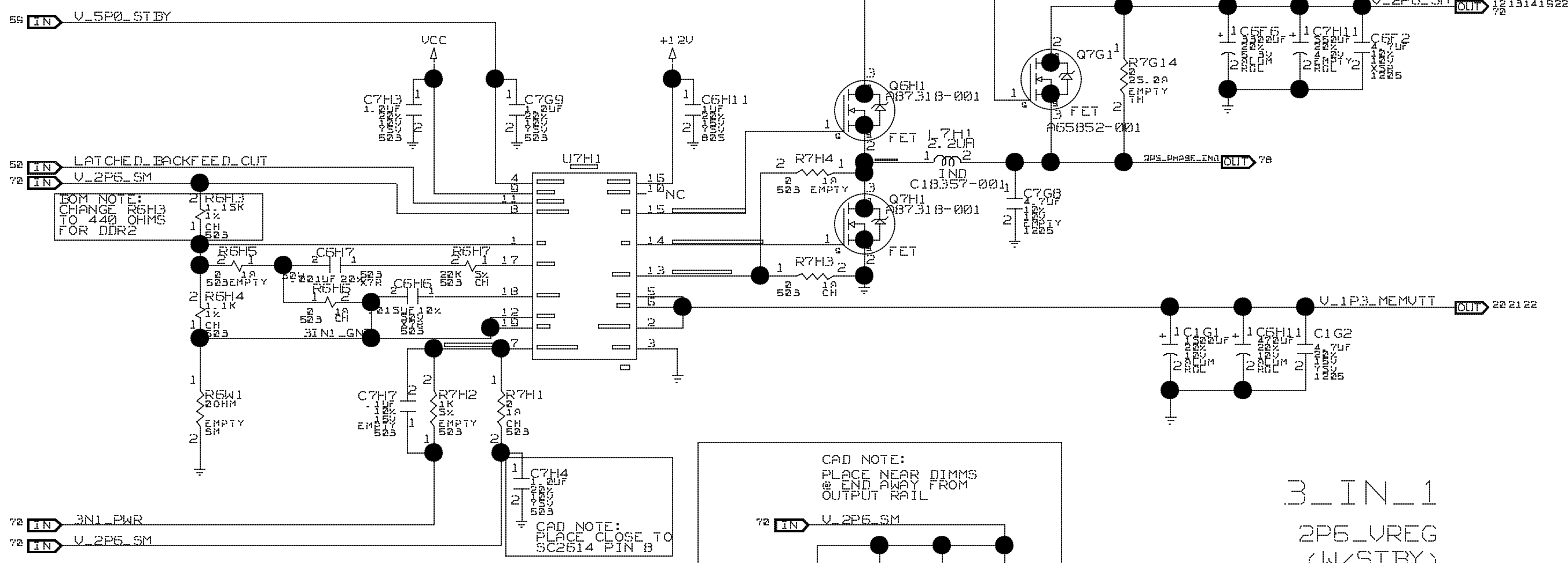
CAD NOTE:  
 MAKE TRACE WIDTH A 50 MIL SHAPE  
 ON SC2614\_5 & SC2614\_6

CAD NOTE:  
 MAKE TRACE WIDTH 12 MILS ON  
 SC2614\_1

CAD NOTE:  
 MAKE TRACE WIDTH 18 MILS ON  
 SC2614\_7

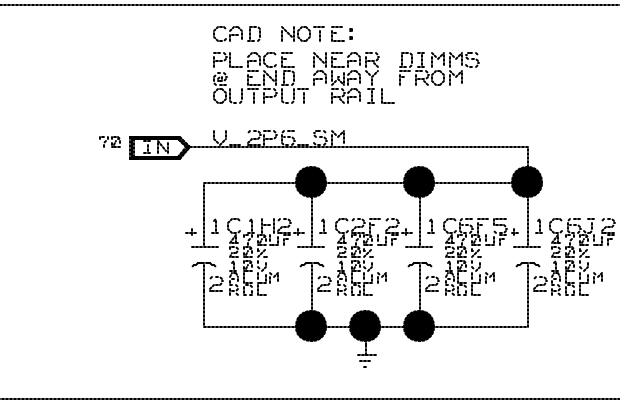


BOM NOTE:  
 MODIFIED TO C20095-001



BOM NOTE:  
 CHANGE R6H3  
 TO 440 OHMS  
 FOR DDR2

CAD NOTE:  
 PLACE CLOSE TO  
 SC2614 PIN B



3\_IN\_1  
 2P5\_VREG  
 (W/STBY)  
 1P3V\_VREG

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: 2P5_VREG AND 1P3V_VREG		REV:
INTEL PLATFORM APPS ENG. 1800 BRANDEE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:28:15 2003	SHEET: 03 70

DRAWING

# PB MOUNTING HOLES

J1G1  
 MTG\_HOLE  
 [NC9] 9  
 EMPTY  
 GND=1, 2, 3, 4, 5, 6, 7, 8

J9G1  
 MTG\_HOLE  
 [NC9] 9  
 EMPTY  
 GND=1, 2, 3, 4, 5, 6, 7, 8

J7G1  
 MTG\_HOLE  
 [NC9] 9  
 EMPTY  
 GND=1, 2, 3, 4, 5, 6, 7, 8

J7J1  
 MTG\_HOLE  
 [NC9] 9  
 EMPTY  
 GND=1, 2, 3, 4, 5, 6, 7, 8

J1B1  
 MTG\_HOLE  
 [NC9] 9  
 EMPTY  
 GND=1, 2, 3, 4, 5, 6, 7, 8

J7A1  
 MTG\_HOLE  
 [NC9] 9  
 EMPTY  
 GND=1, 2, 3, 4, 5, 6, 7, 8

J1J1  
 MTG\_HOLE  
 [NC9] 9  
 EMPTY  
 GND=1, 2, 3, 4, 5, 6, 7, 8

J8A1  
 MTG\_HOLE  
 [NC9] 9  
 EMPTY  
 GND=1, 2, 3, 4, 5, 6, 7, 8

DRAWING

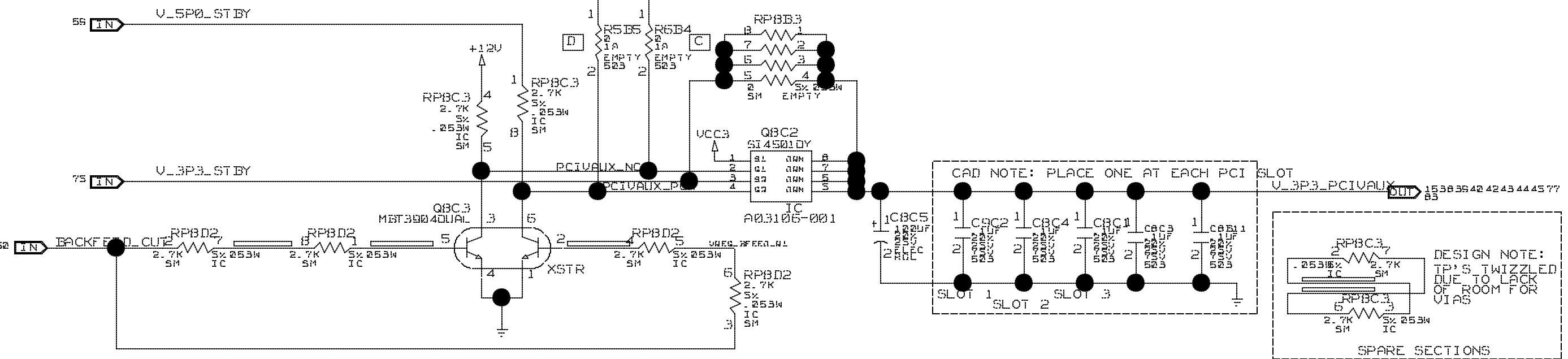
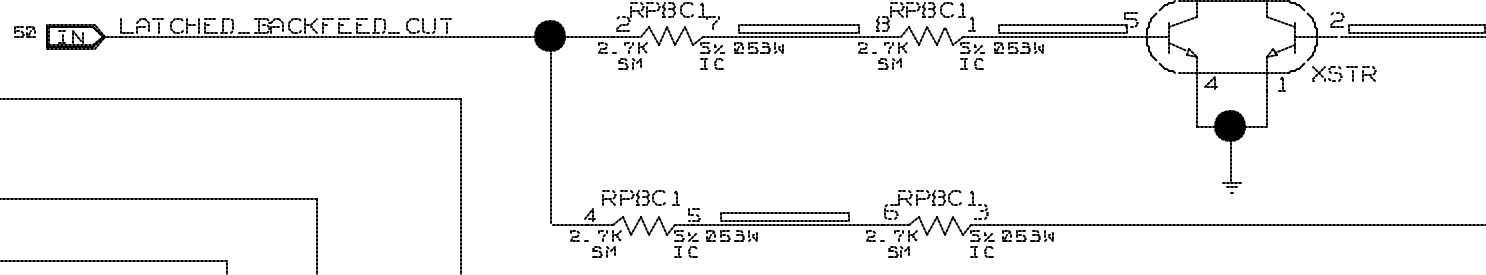
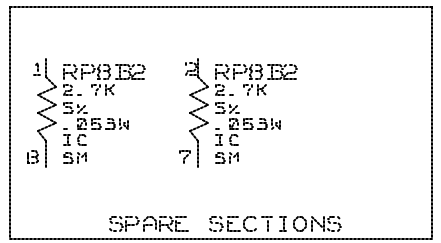
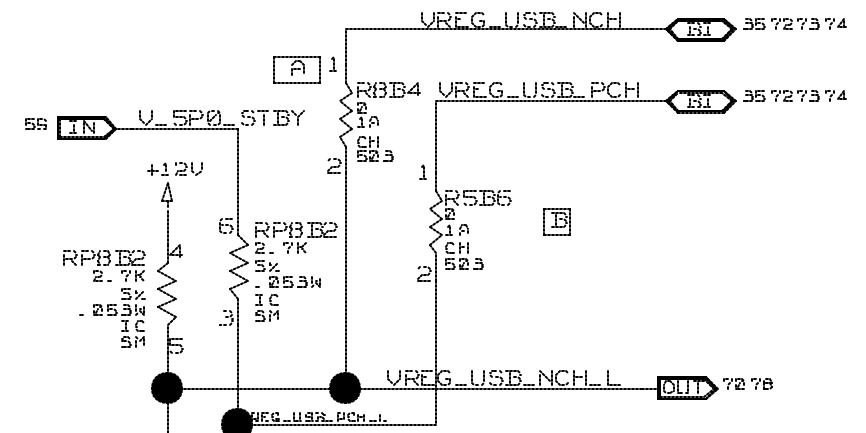
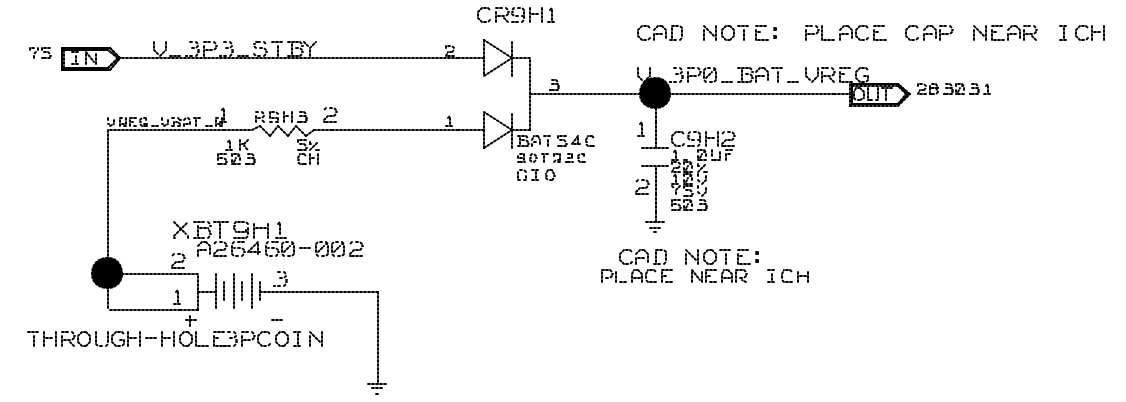
SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: PB MOUNTING HOLES		SHEET: 71
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:28:17 2003	

# BATTERY

BOM=UREG  
ROOM = UREG UNLESS SPECIFIED

### NOTES:

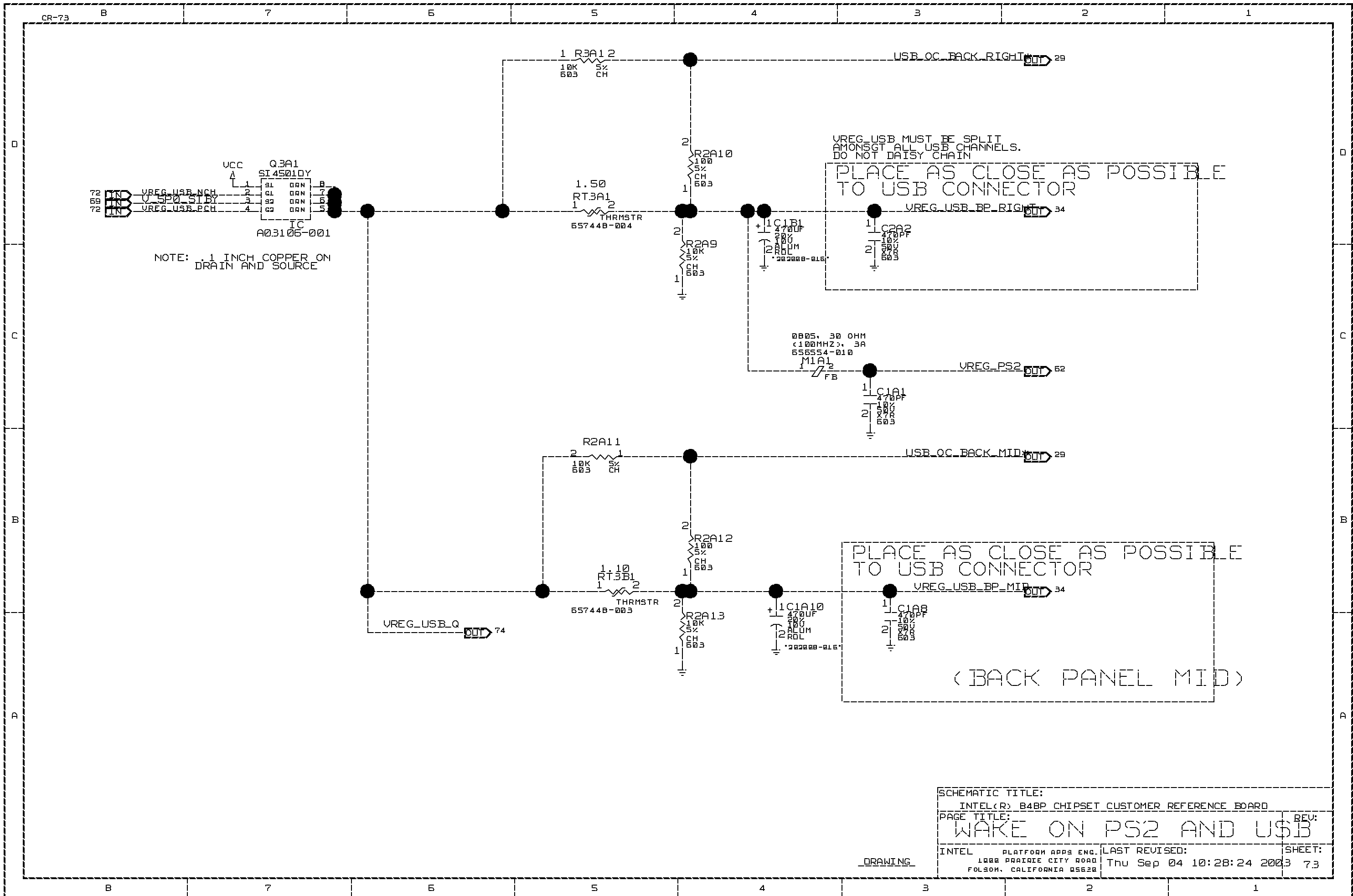
USB/PS2WAKE	A & B	C & D
S3 ONLY	STUFF	EMPTY
S3, S4, S5	EMPTY	STUFF

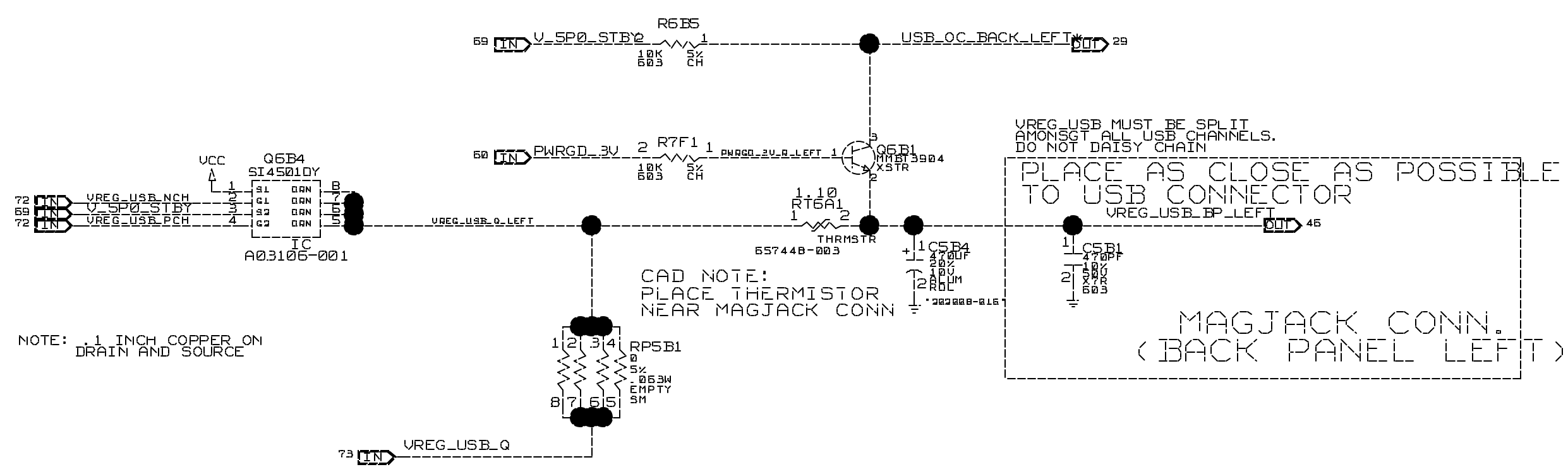


# PCI VAUX

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: WAKE ON PS2 & USB (BACK PANEL RIGHT)		SHEET:
INTEL PLATFORM APPS ENG. 1800 BRANDEE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:28:21 2003	72

DRAWING





NOTE: .1 INCH COPPER ON DRAIN AND SOURCE

CAD NOTE:  
PLACE THERMISTOR  
NEAR MAGJACK CONN

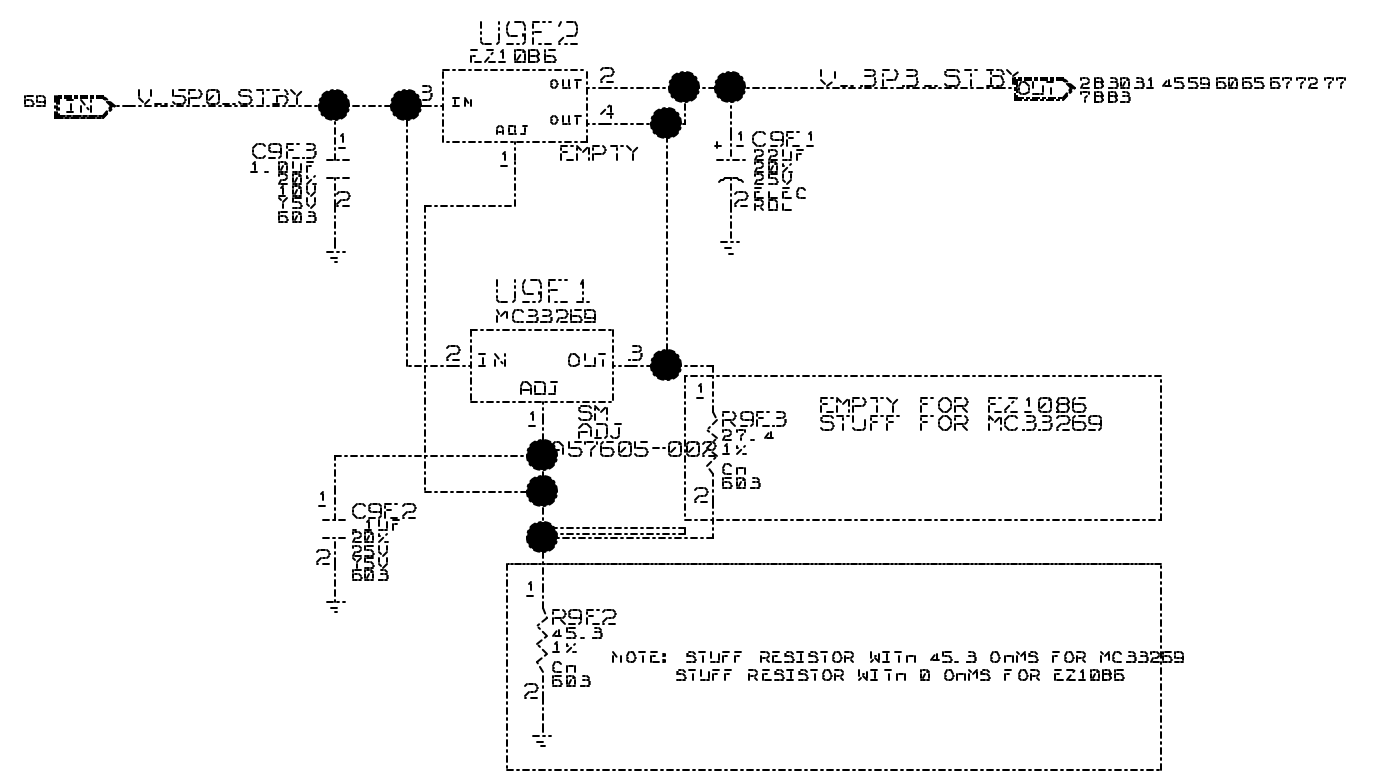
VREG\_USB MUST BE SPLIT  
AMONGST ALL USB CHANNELS.  
DO NOT DAISY CHAIN

PLACE AS CLOSE AS POSSIBLE  
TO USB CONNECTOR

MAGJACK CONN.  
(BACK PANEL LEFT)

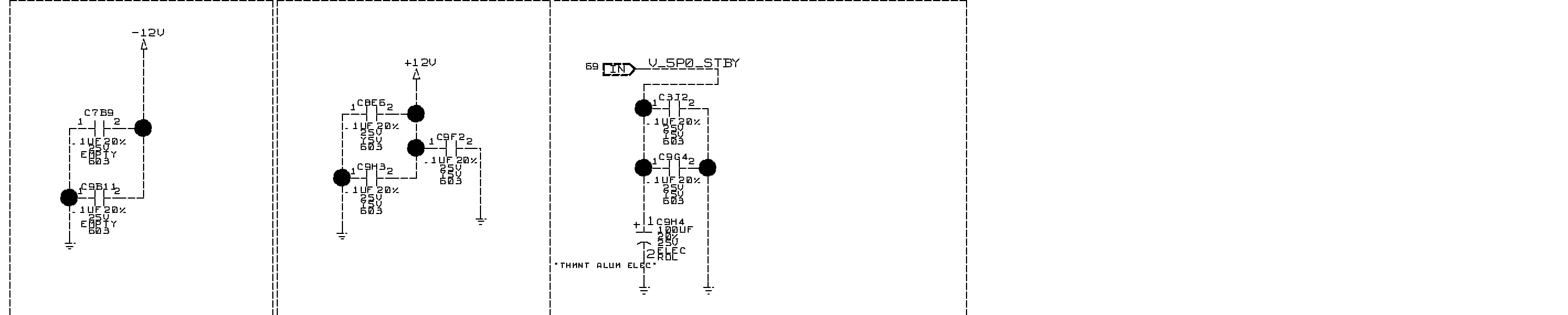
SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		WAKE ON USB AND MAGNETICS JACK	
INTEL PLATFORM APPS ENG.		LAST REVISED:	REV:
1000 PRAIRIE CITY ROAD		Thu Sep 04 10:28:25 2003	03 74
FOLSOM, CALIFORNIA 95620		SHEET:	

DRAWING



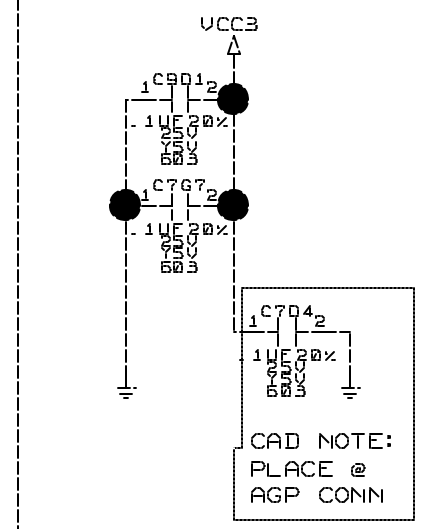
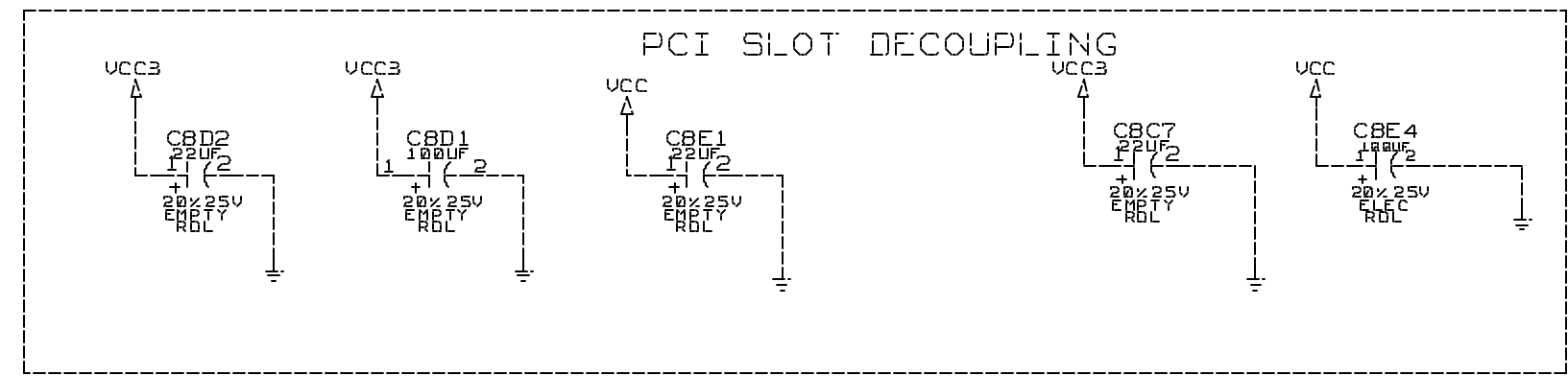
SCHEMATIC TITLE:	
INTEL(R) BABP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:	REV:
3.3V STANDBY	
INTEL PLATFORM APPS ENG.	LAST REVISED:
1000 PRAIRIE CITY ROAD	Thu Sep 04 10:28:28 2003 75
FOLSOM, CALIFORNIA 95620	SHEET:

..DRAWING.

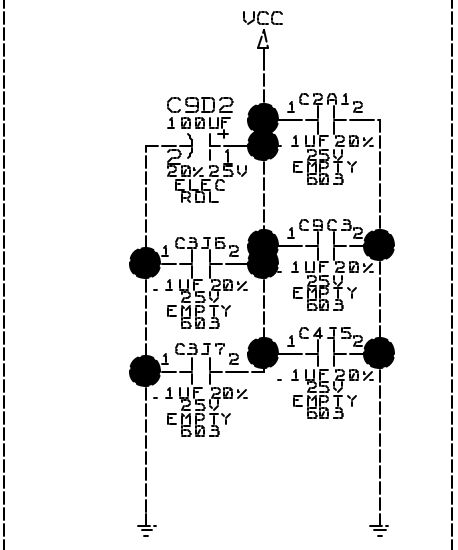


CAD NOTE:  
ONE FOR EACH PCI SLOT

CAD NOTE:  
ONE FOR EACH PCI SLOT  
ONE FOR AGP CONN



CAD NOTE:  
ONE FOR EACH PCI SLOT  
ONE FOR AGP CONN



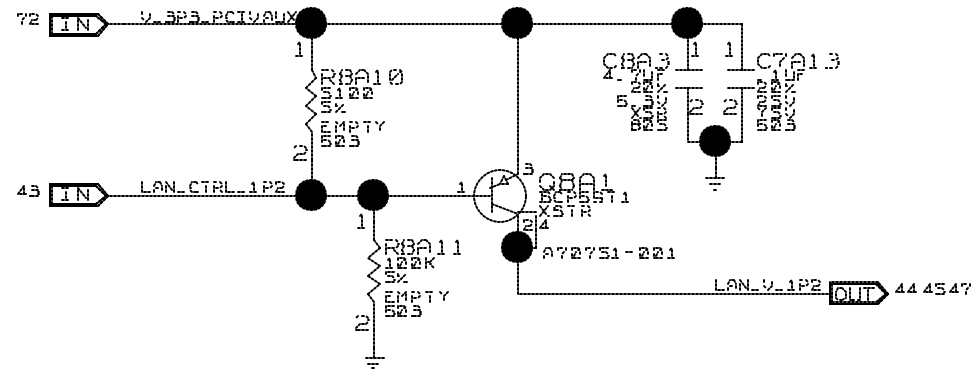
CAD NOTE:  
ONE FOR EACH PCI SLOT

SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: VREG BULK DECOUPLING		SHEET:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:28:29 2003	76

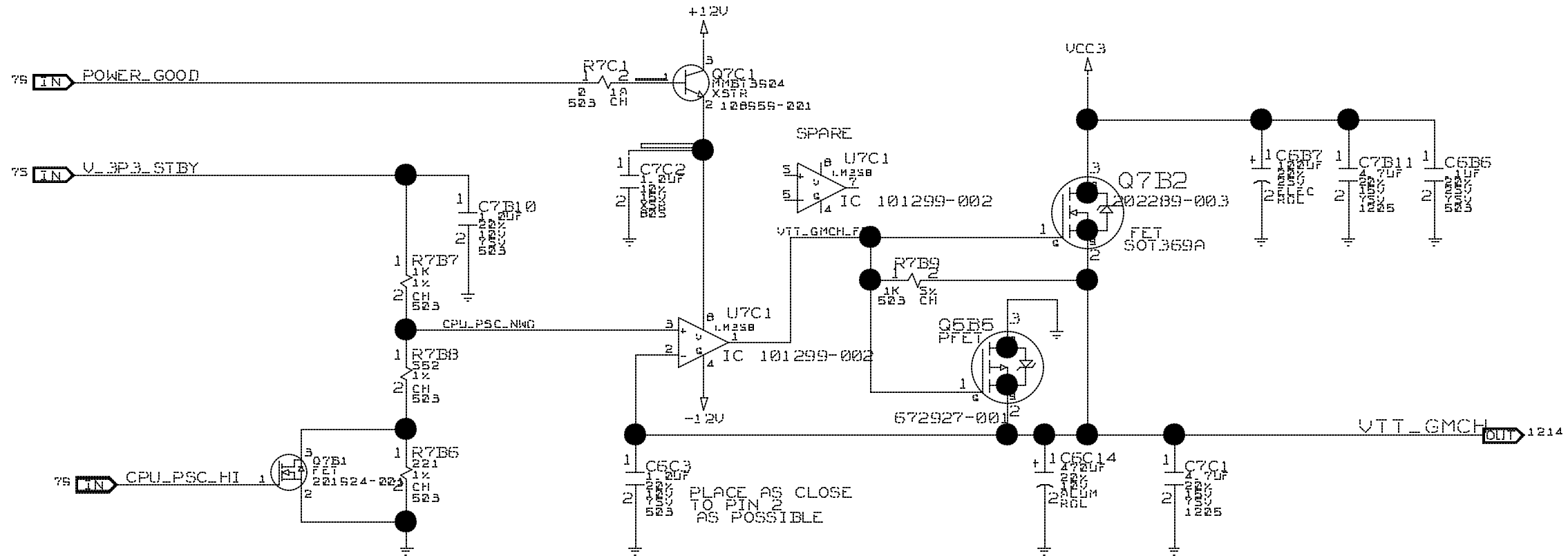
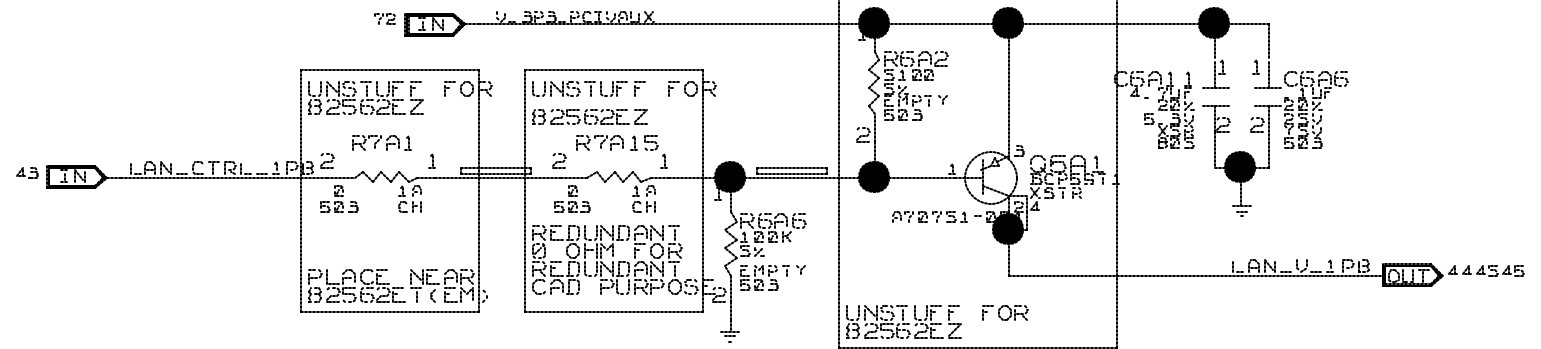
DRAWING



### 1.2V LAN REGULATION

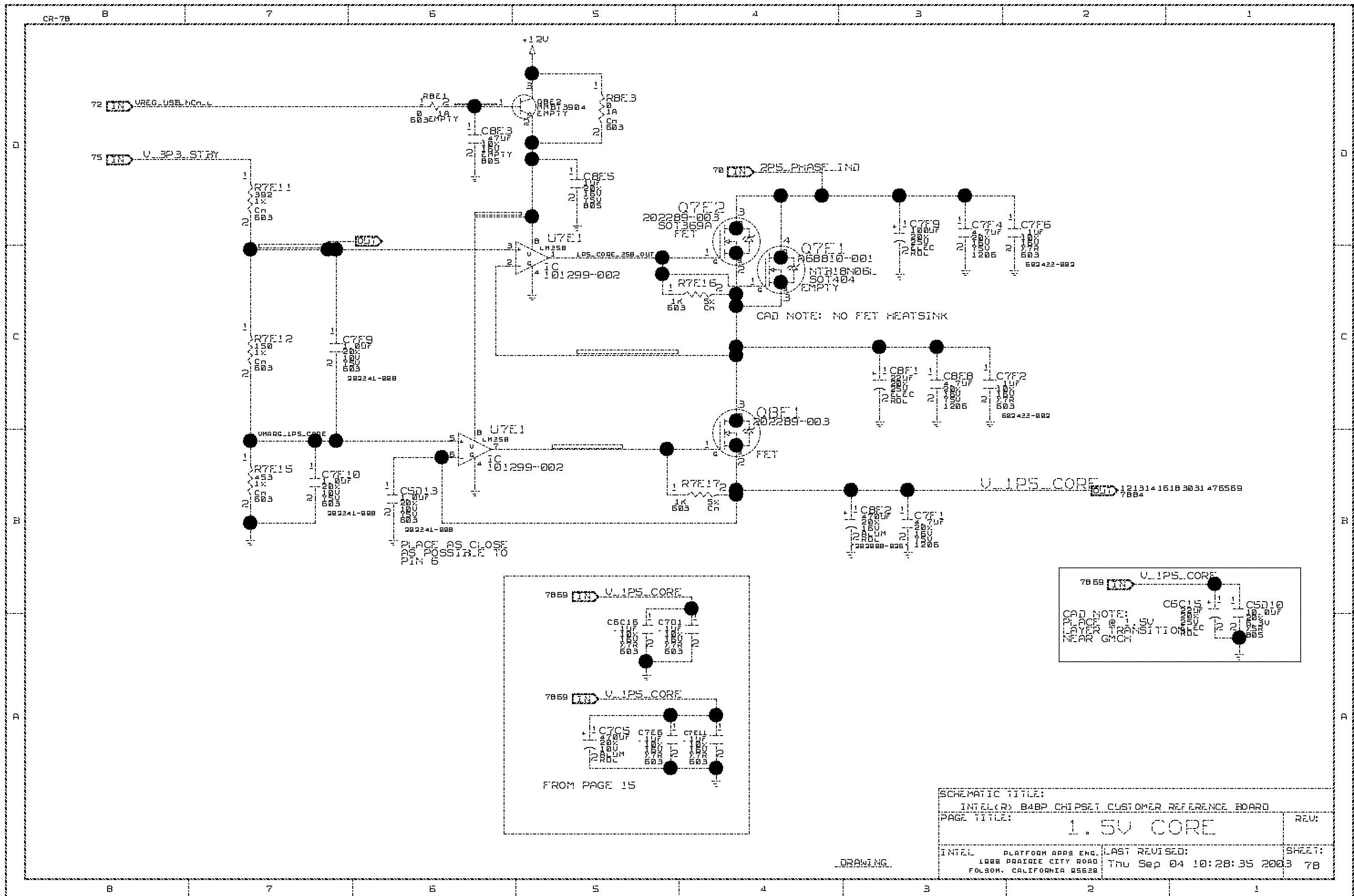


### 1.1V LAN REGULATION



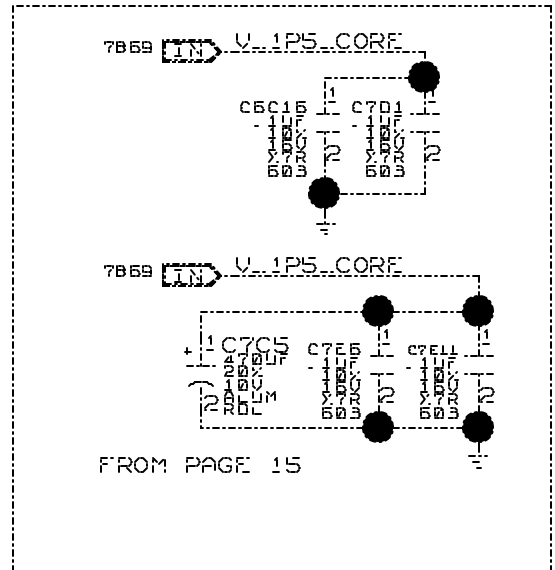
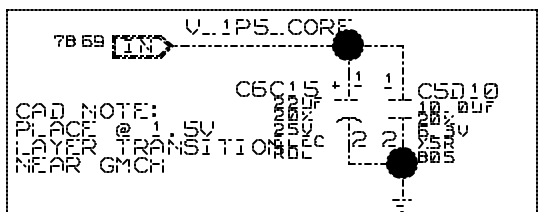
SCHEMATIC TITLE:	
INTEL(R) B48P CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:	REV:
LAN VREG/PROCESSOR SELECT	
INTEL PLATFORM APPS ENG. 1888 BRANDEE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:28:33 2003 77
SHEET:	

DRAWING



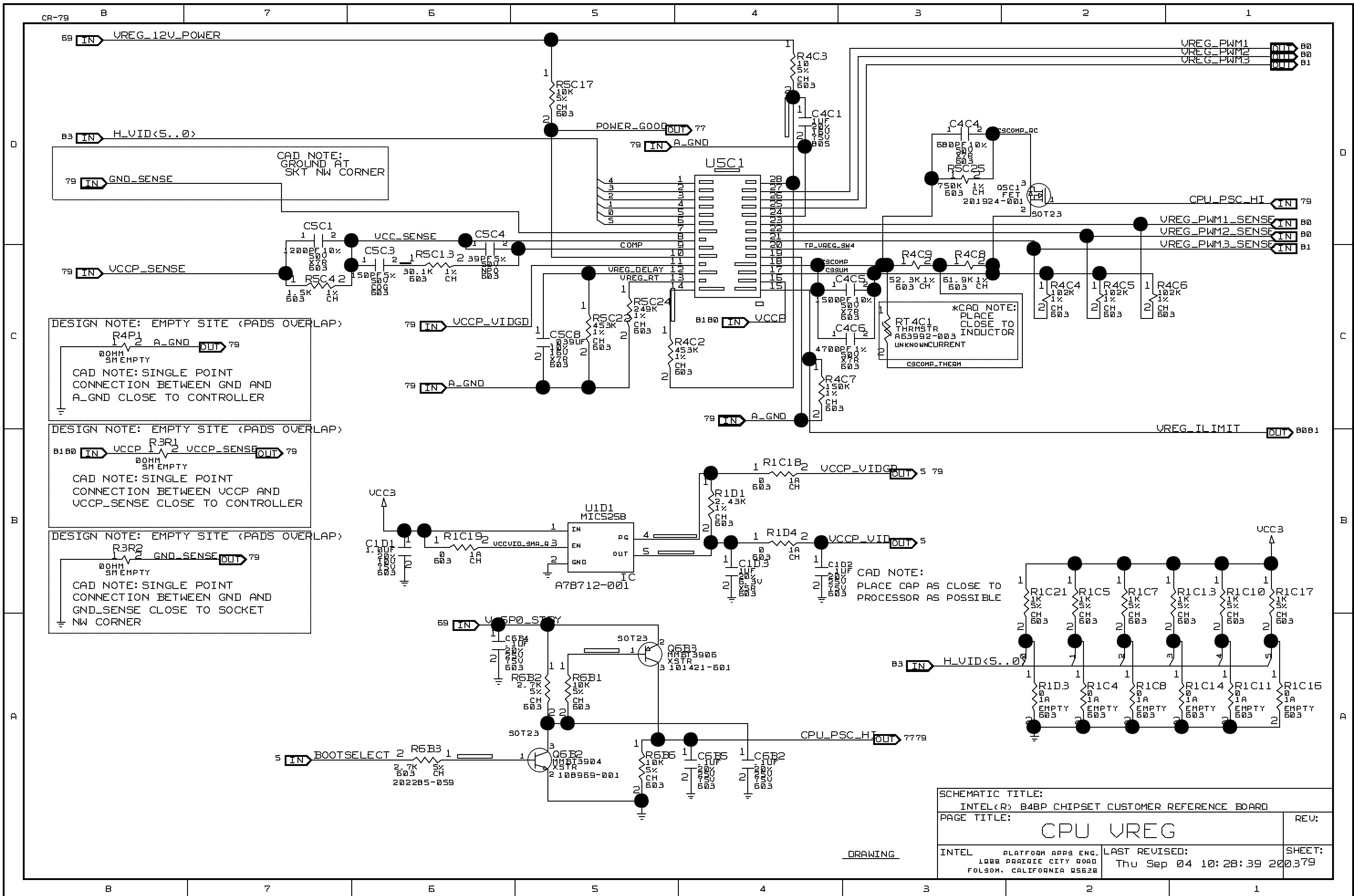
CAD NOTE: NO FET HEATSINK

PLACE AS CLOSE AS POSSIBLE TO PIN 6



FROM PAGE 15

SCHEMATIC TITLE:		INTEL(R) BABP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		1.5V CORE	
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620		LAST REVISED: Thu Sep 04 10:28:35 2003	
DRAWING		SHEET: 78	



CAD NOTE:  
GROUND AT  
SKT NW CORNER

DESIGN NOTE: EMPTY SITE (PADS OVERLAP)  
R4P1  
00HM  
SM EMPTY  
CAD NOTE: SINGLE POINT  
CONNECTION BETWEEN GND AND  
A\_GND CLOSE TO CONTROLLER

DESIGN NOTE: EMPTY SITE (PADS OVERLAP)  
R3R1  
00HM  
SM EMPTY  
CAD NOTE: SINGLE POINT  
CONNECTION BETWEEN UCCP AND  
UCCP\_SENSE CLOSE TO CONTROLLER

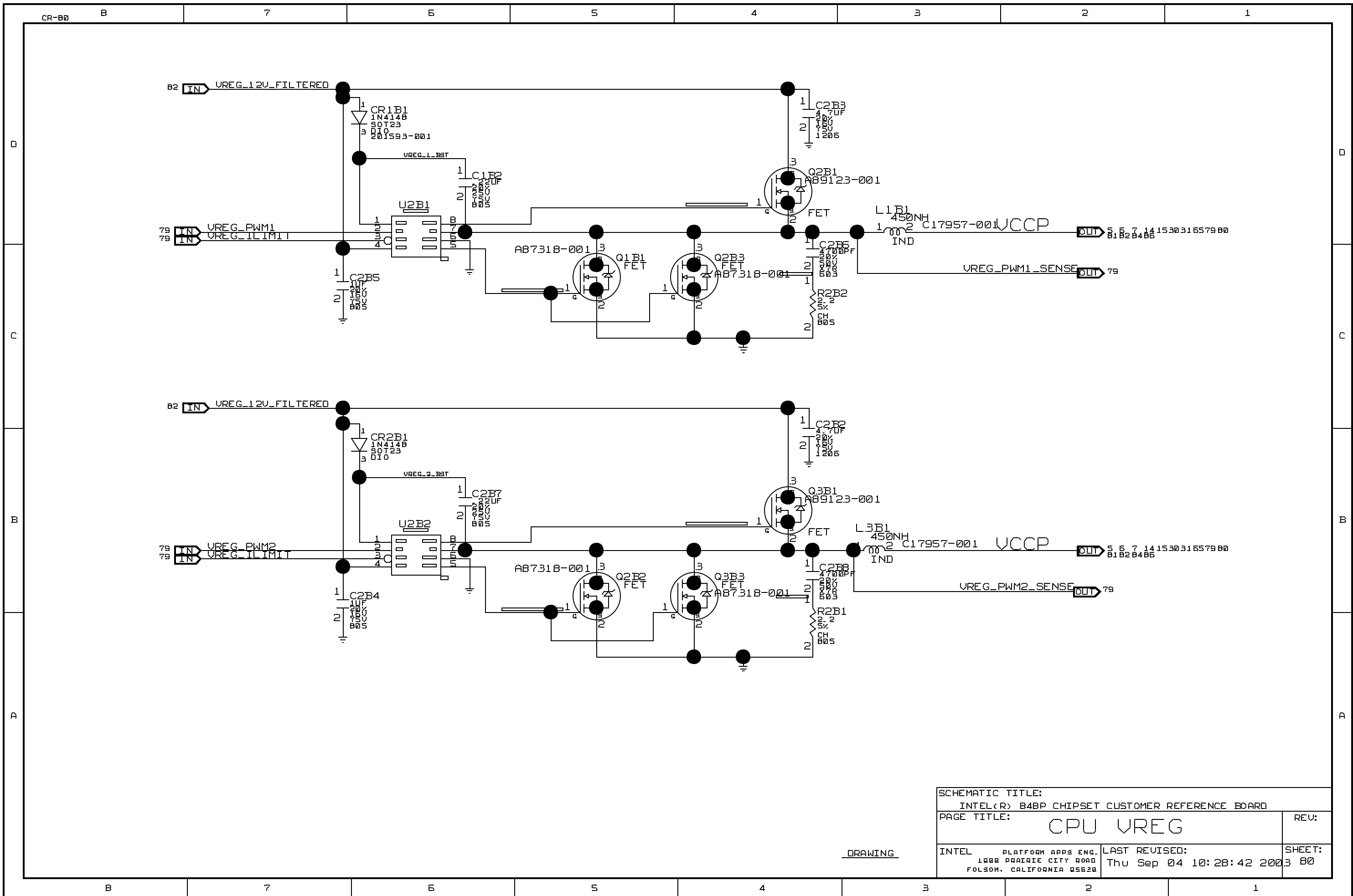
DESIGN NOTE: EMPTY SITE (PADS OVERLAP)  
R3R2  
00HM  
SM EMPTY  
CAD NOTE: SINGLE POINT  
CONNECTION BETWEEN GND AND  
GND\_SENSE CLOSE TO SOCKET  
NW CORNER

CAD NOTE:  
PLACE CAP AS CLOSE TO  
PROCESSOR AS POSSIBLE

\*CAD NOTE:  
PLACE  
CLOSE TO  
INDUCTOR  
UNKNOWN CURRENT

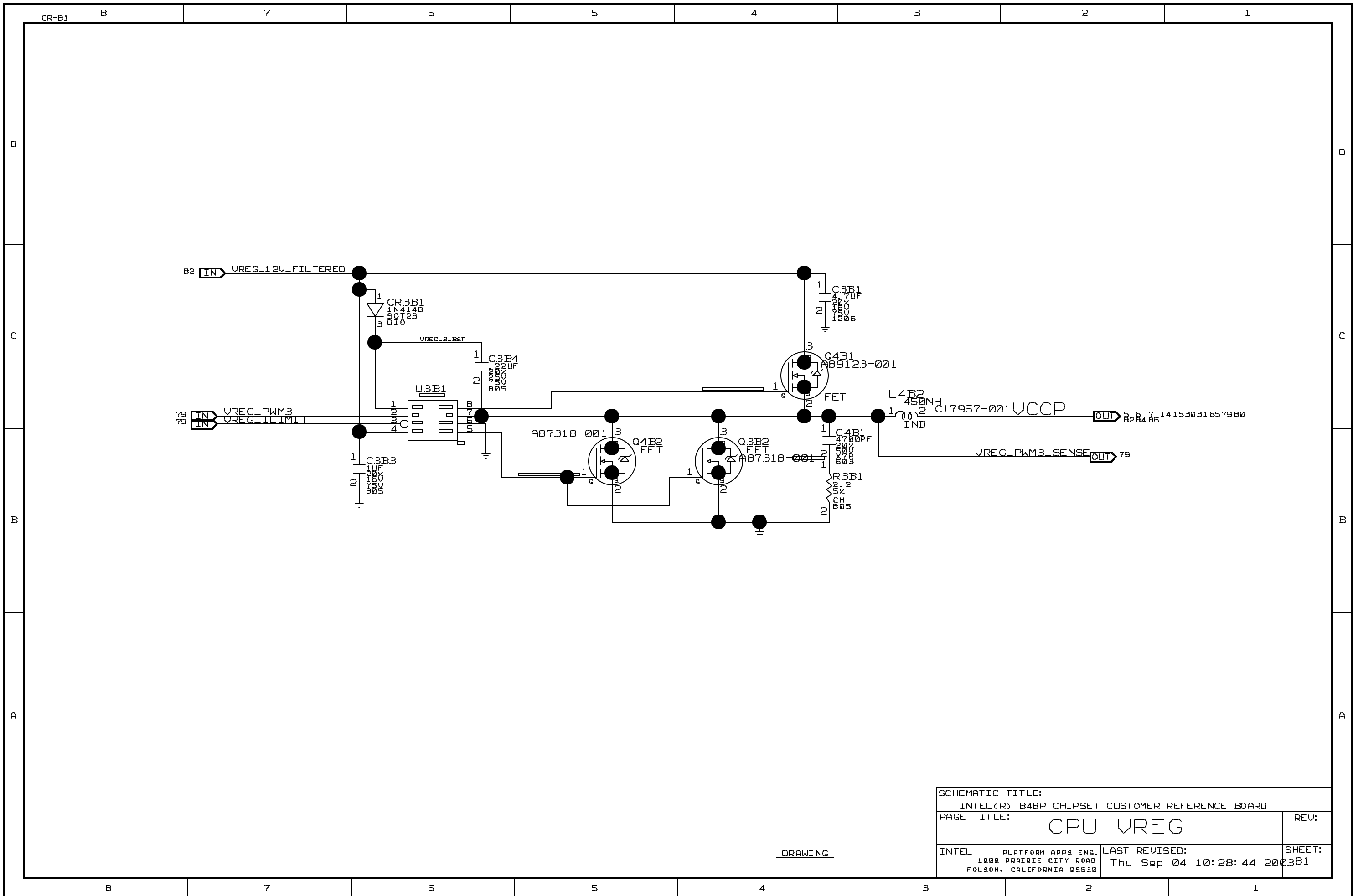
SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		REV:
PAGE TITLE: CPU VREG		SHEET: 0379
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:28:39 2003	

DRAWING



SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: <b>CPU VREG</b>	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:28:42 2003 80
SHEET: 3 80	

DRAWING

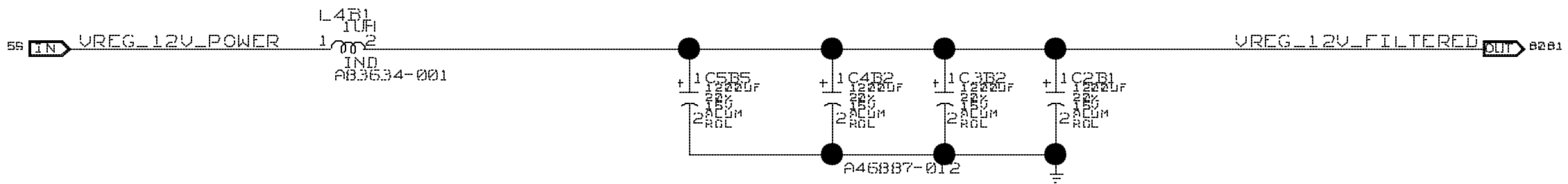
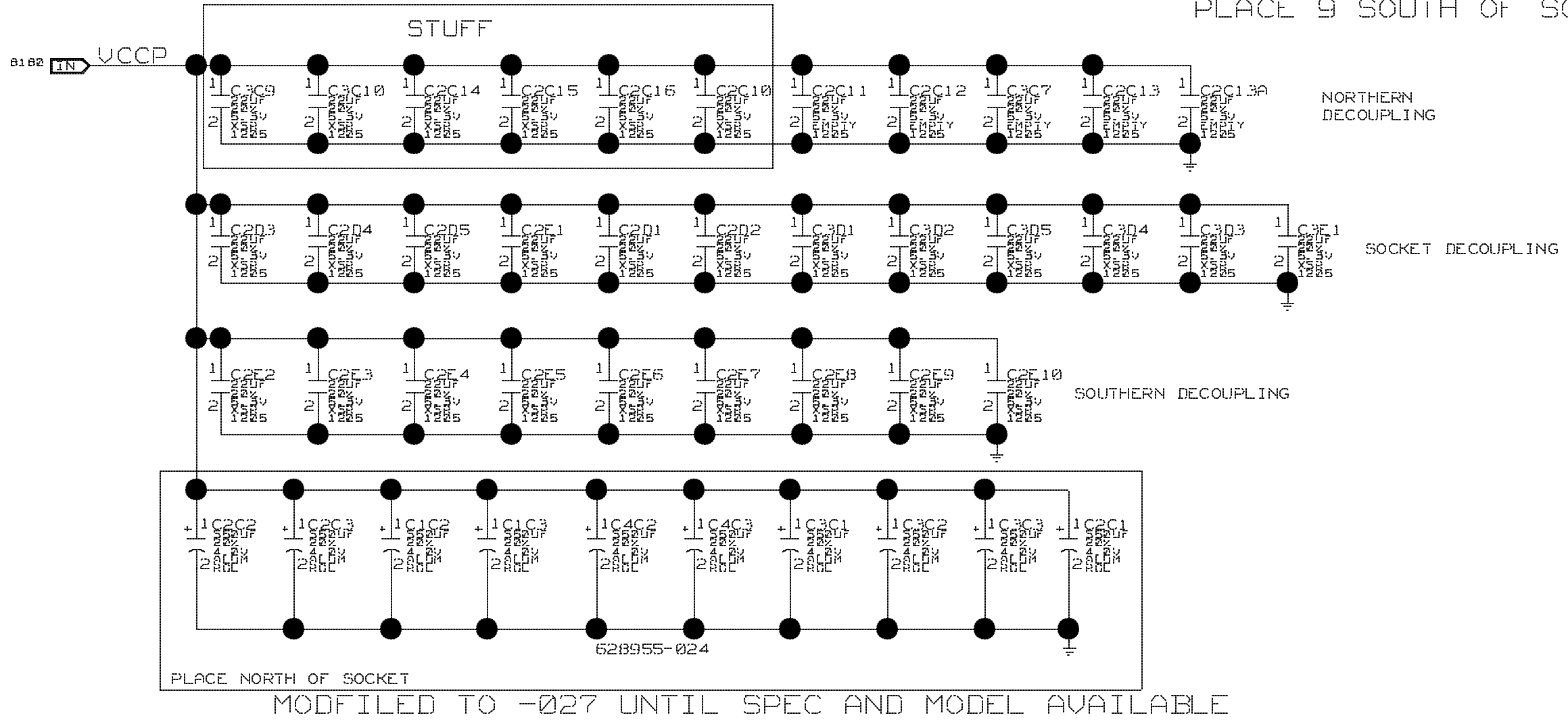


SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		CPU VREG	
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: Thu Sep 04 10:28:44 2003	REV: SHEET: 0381

DRAWING

CAD NOTE: PLACE AS MANY 1206 CAPACITORS AS POSSIBLE WITHIN CPU CAVITY

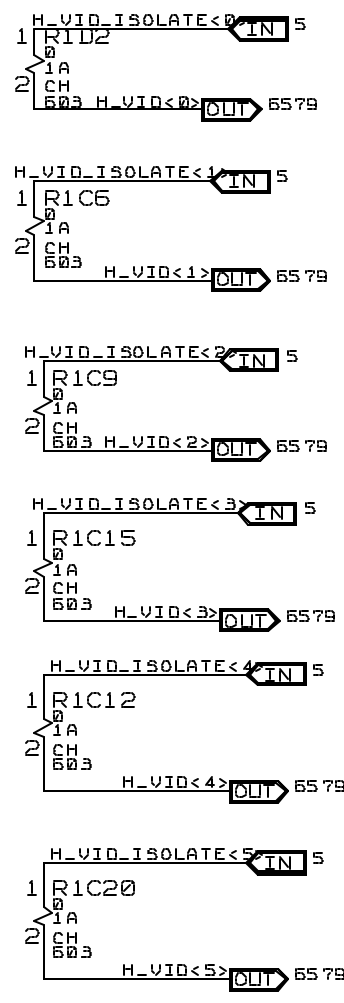
PLACEMENT NOTE FOR 1206:  
 PLACE 11 NORTH OF SOCKET (STUFF 5)  
 PLACE 12 INSIDE CPU SOCKET (STUFF ALL)  
 PLACE 9 SOUTH OF SOCKET (UNSTUFF ALL)



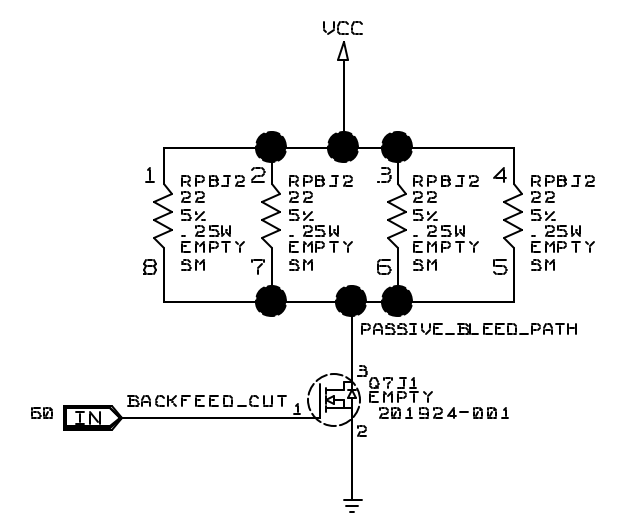
SCHEMATIC TITLE: INTEL(R) B48P CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: <b>CPU DECOUPLING</b>	REV:
INTEL PLATFORM APPS ENG. 1800 BARRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu Sep 04 10:28:45 2003
SHEET:	

DRAWING

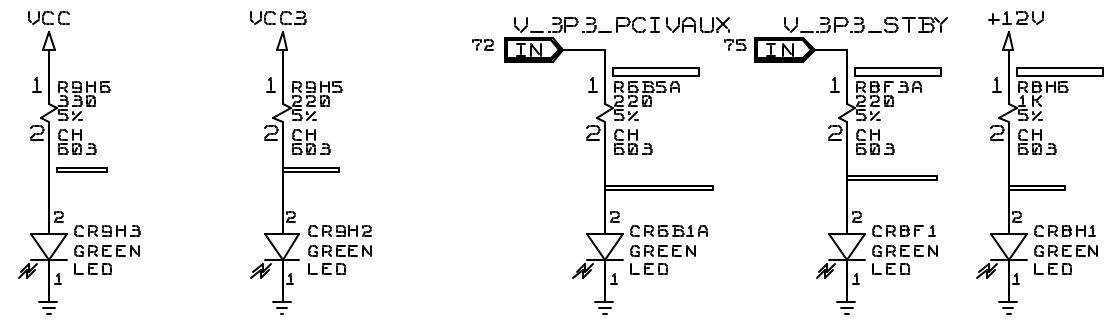
VID JUMPER RESISTORS



PASSIVE BLEED CIRCUIT



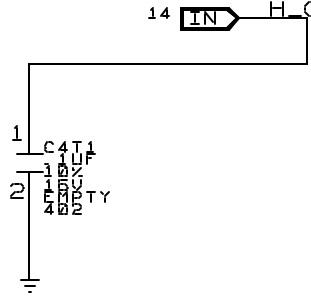
POWER RAIL STATUS LED'S



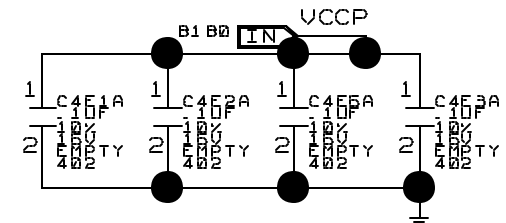
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SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PASSIVE BLEED CKT/STATUS LEDS/FRNT PANEL SWITCHES/VID JMPRS		REV: MPRS
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:28:47 2003	SHEET: 033

MCH BACK DECOUPLING

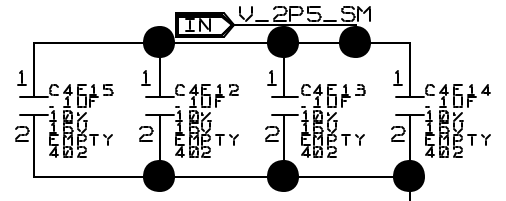


402



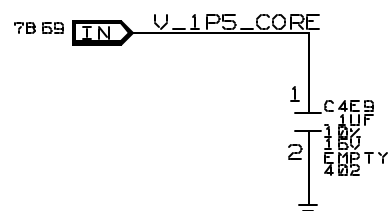
MCH CUB DECOUPLING

402



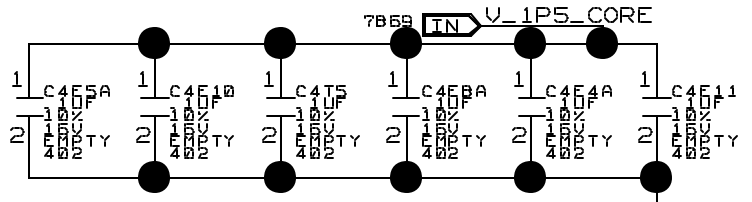
MCH CUB DECOUPLING

402



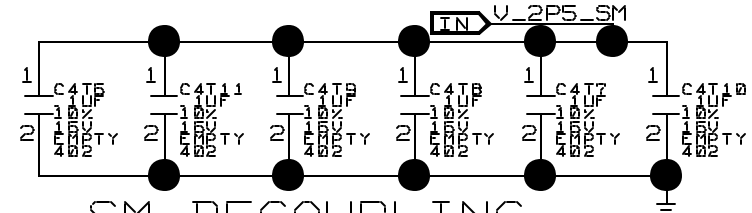
MCH CUB DECOUPLING

402



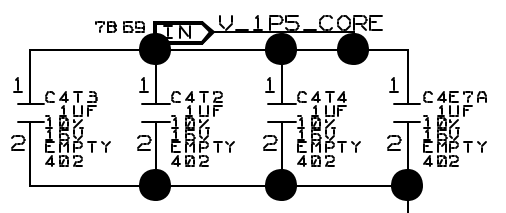
MCH CUB DECOUPLING

402



SM DECOUPLING

402

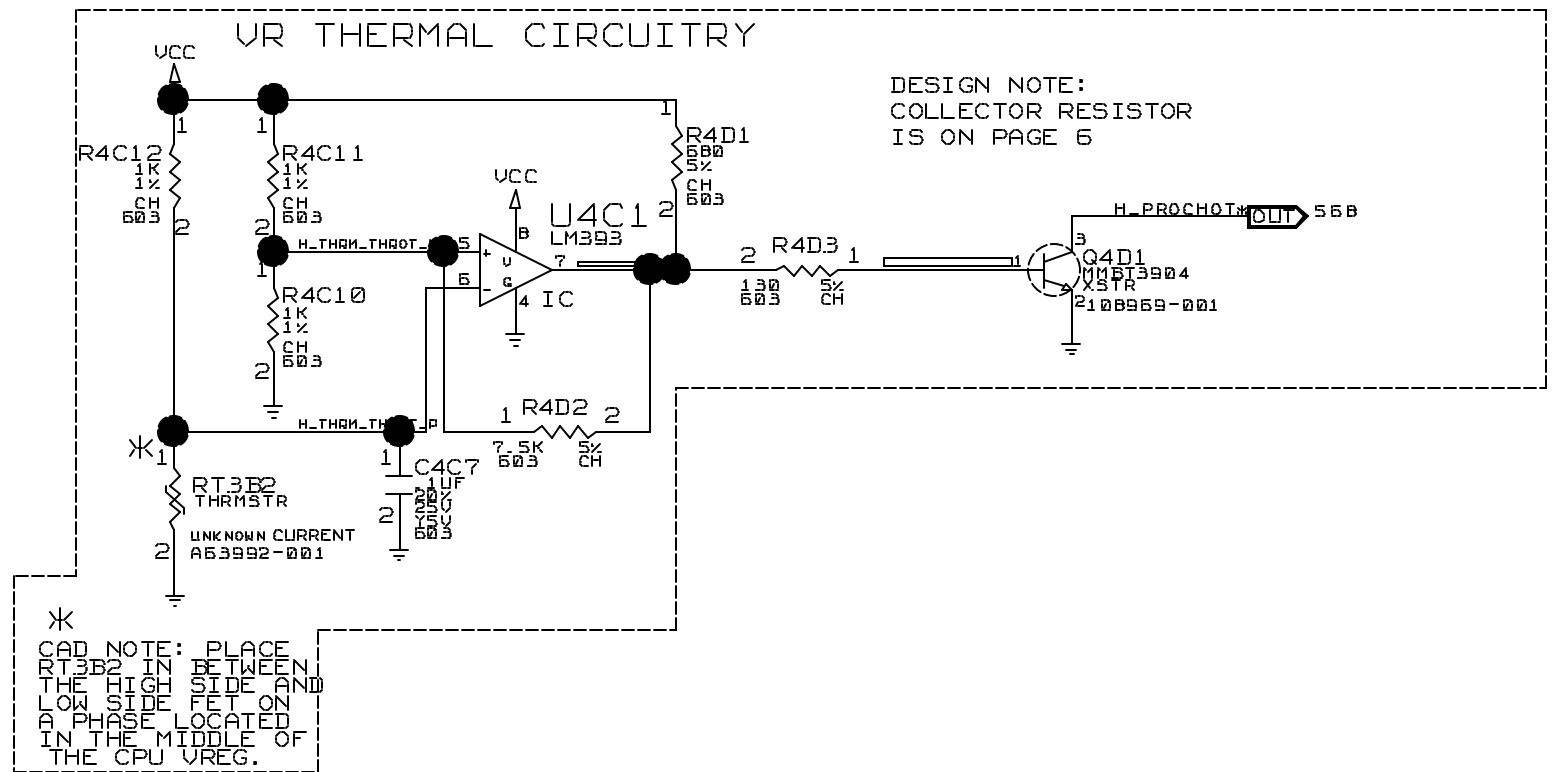


MCH DECOUPLING

SCHEMATIC TITLE:		INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE:		BACKSIDE CAPS	REV:
INTEL	PLATFORM APPS ENG.	LAST REVISED:	SHEET:
1000 PRAIRIE CITY ROAD		Thu Sep 04 10:28:48 2003	0384
FOLSOM, CALIFORNIA 95620			

DRAWING

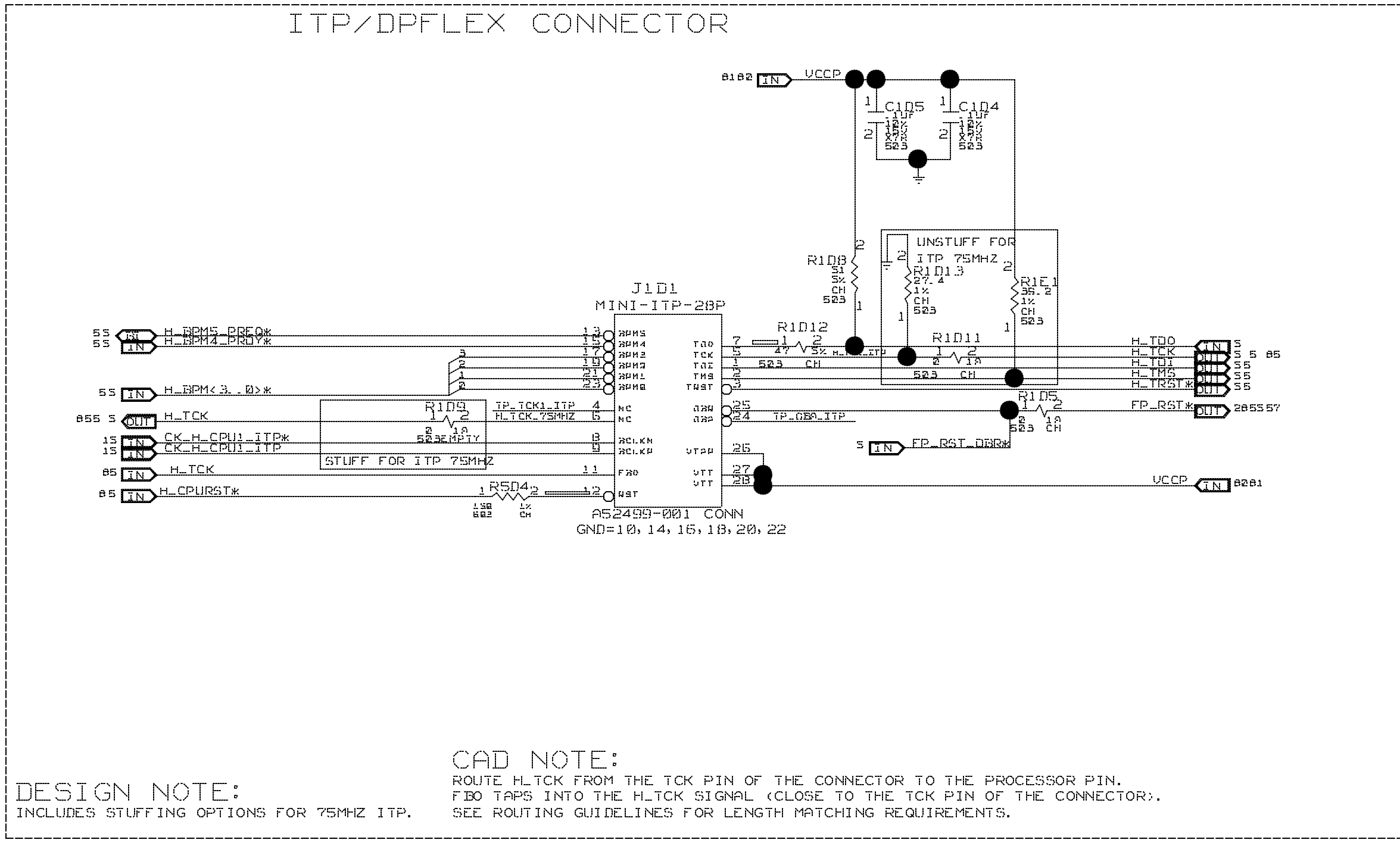




SCHEMATIC TITLE: INTEL(R) B4BP CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: VR THERMAL CIRCUITRY	REV:
INTEL PLATFORM APPS ENG. 1000 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:28:50 2003
	SHEET: 0385

DRAWING

### ITP/DPFLEX CONNECTOR



**DESIGN NOTE:**  
INCLUDES STUFFING OPTIONS FOR 75MHZ ITP.

**CAD NOTE:**  
ROUTE HLTCK FROM THE TCK PIN OF THE CONNECTOR TO THE PROCESSOR PIN.  
FBO TAPS INTO THE HLTCK SIGNAL (CLOSE TO THE TCK PIN OF THE CONNECTOR).  
SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS.

SCHEMATIC TITLE: INTEL(R) 848P CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: <b>ITP</b>	REV:
INTEL PLATFORM APPS ENG. 1800 BRANIFF CITY ROAD FOLSOM, CALIFORNIA 95620	LAST REVISED: Thu Sep 04 10:28:53 2003
SHEET: 0386	

DRAWING