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13	PROCESSOR TERMINATION, STRAPPING, ITP
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INTEL (R) PENTIUM (R) 4 & INTEL (R) 82850 CHIPSET UNIPROCESSOR CUSTOMER REFERENCE SCHEMATICS -REVISION 3.0

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NO VIP/VBP

POWER SYMBOLS USED:
 VCC3
 VCC
 +12V
 -12V
 -5V (PAGE 67, POWER-CONN)

- NOTES:
1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT (PBA) ENG. PARTS LIST FOR ITEMS SHOWN AS OPTIONAL IN THIS SCHEMATIC.
 2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
 3. VCC= +5V UNLESS OTHERWISE SPECIFIED.
 4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
 5. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

SCHEMATIC TITLE: INTEL (R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: COVER SHEET		SHEET: 1
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 16:33:18 2000	

DRAWING

CR-2

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

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8

7

6

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CR-3

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6

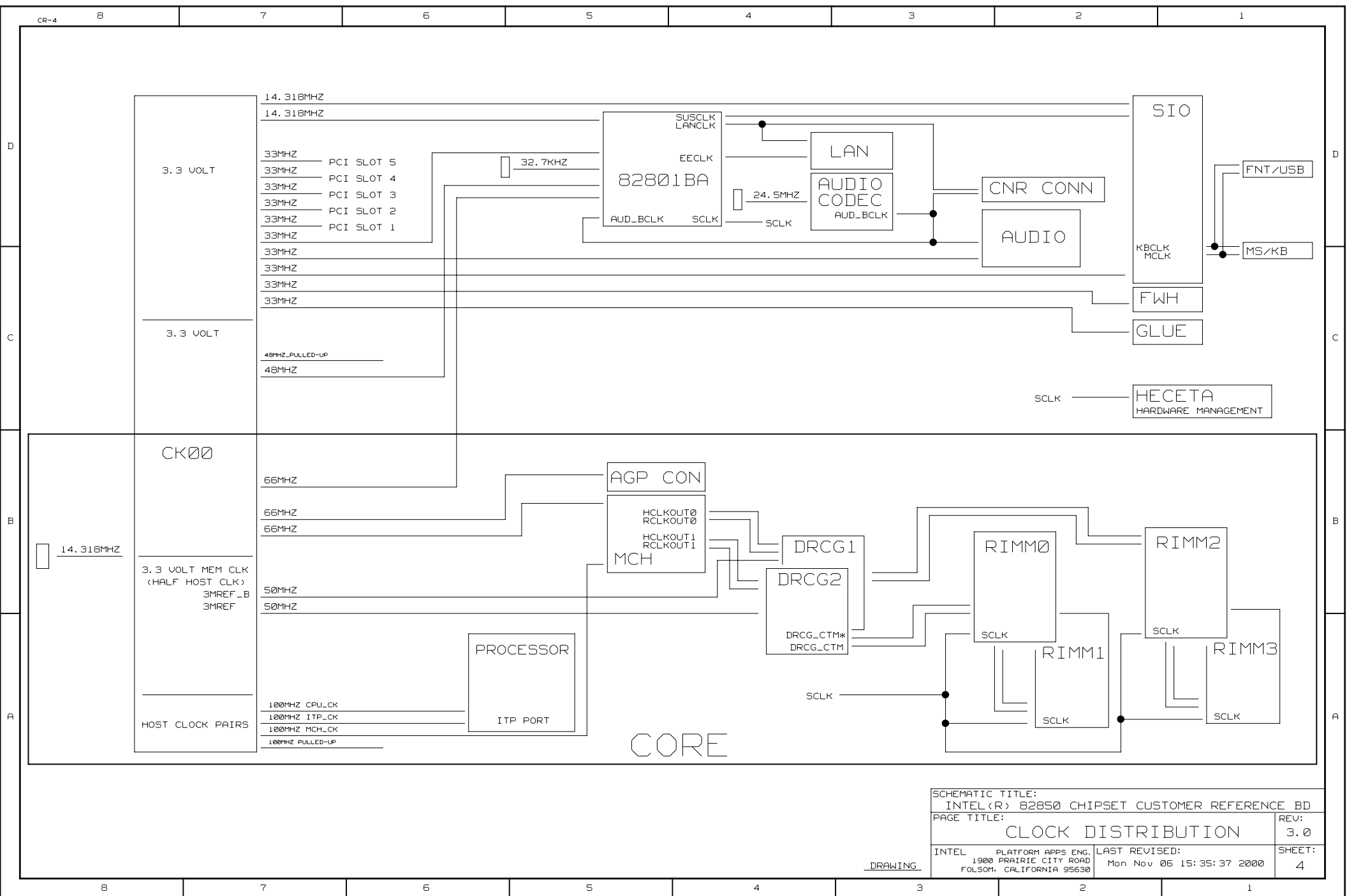
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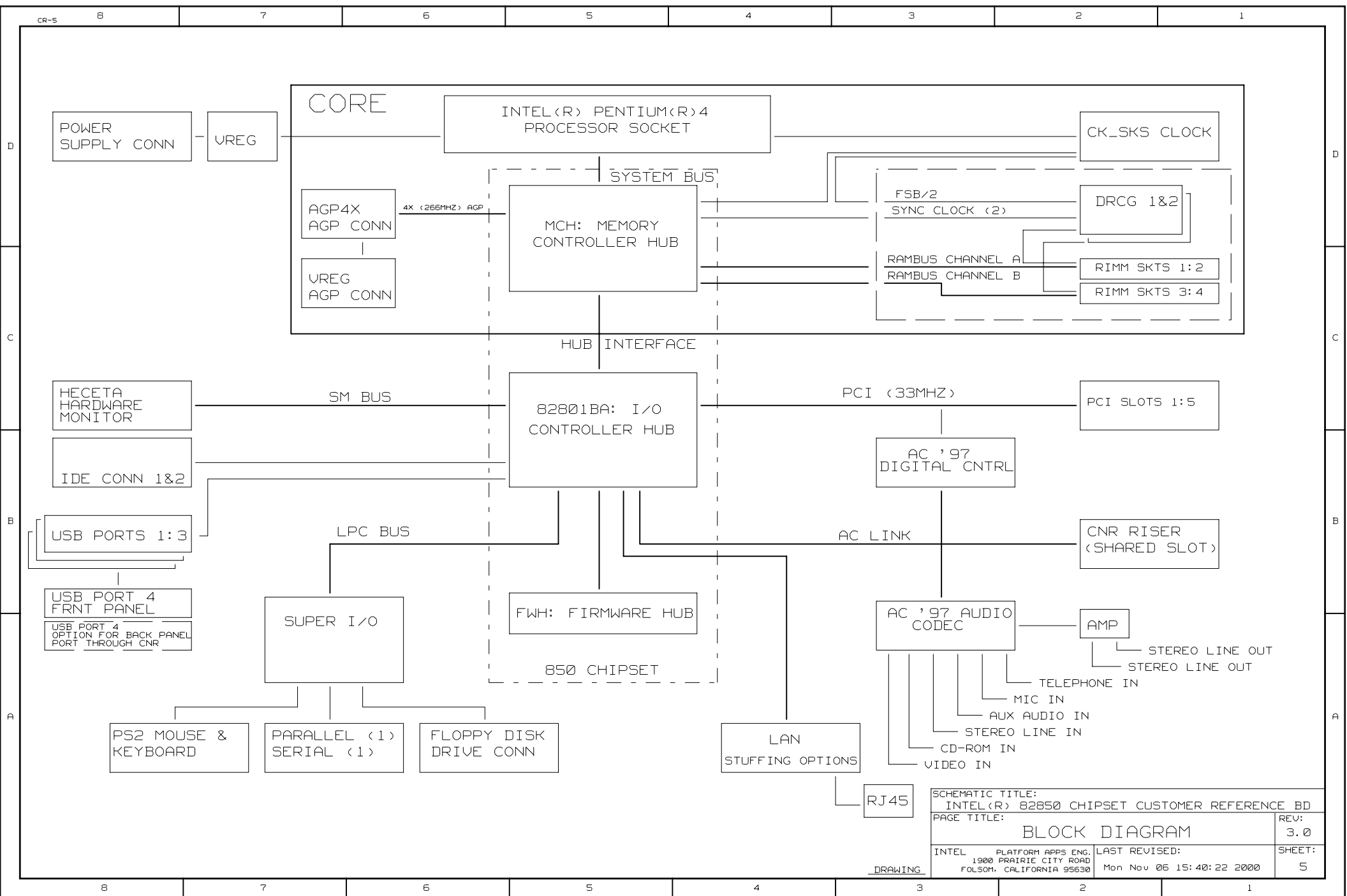
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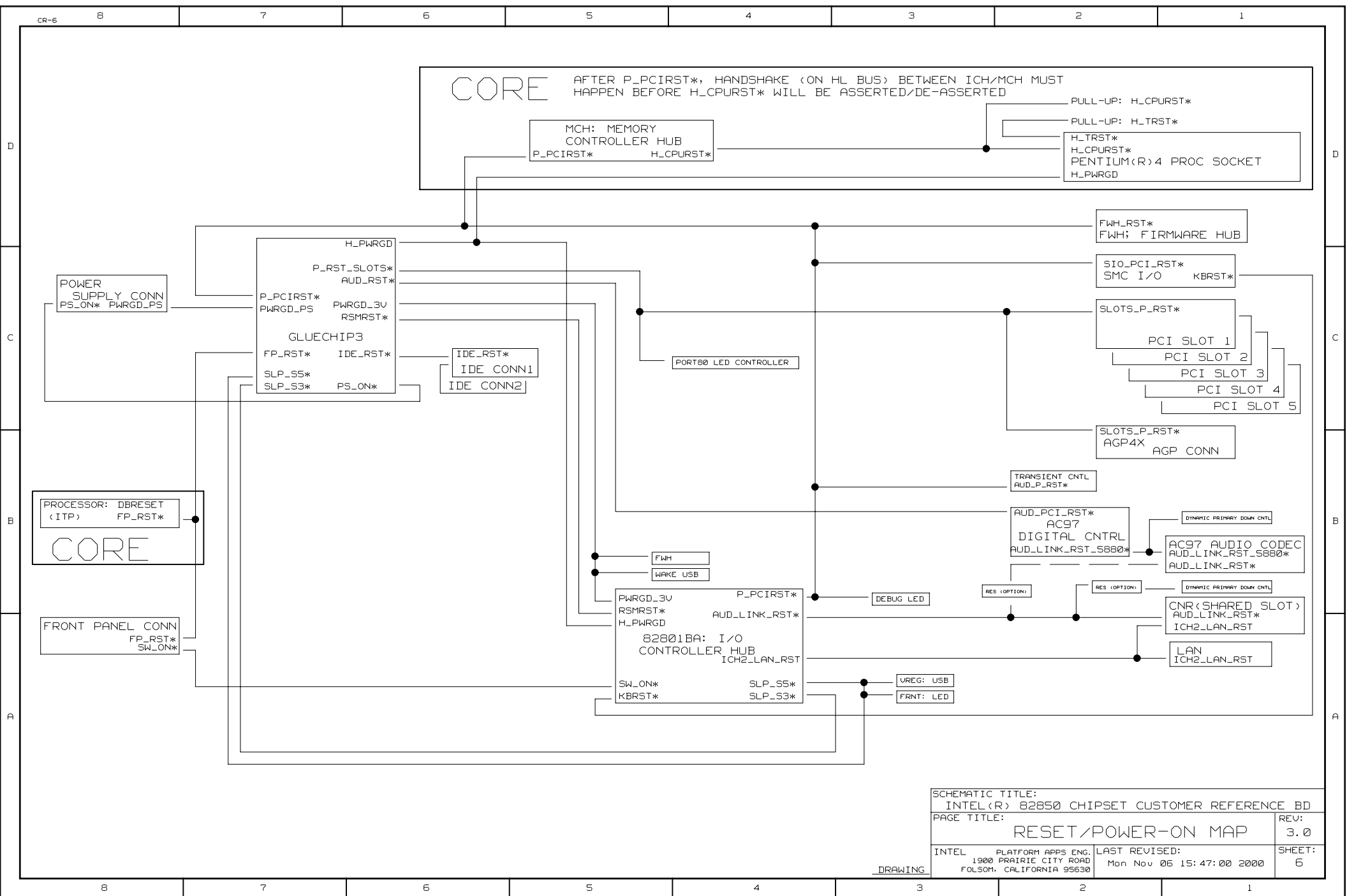


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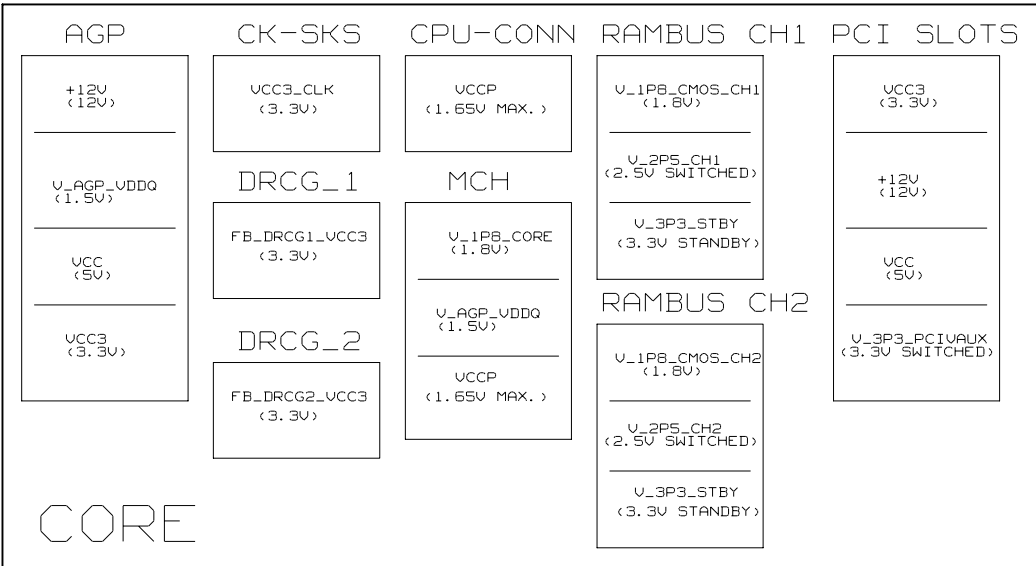
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RESET/POWER-ON MAP

REV: 3.0

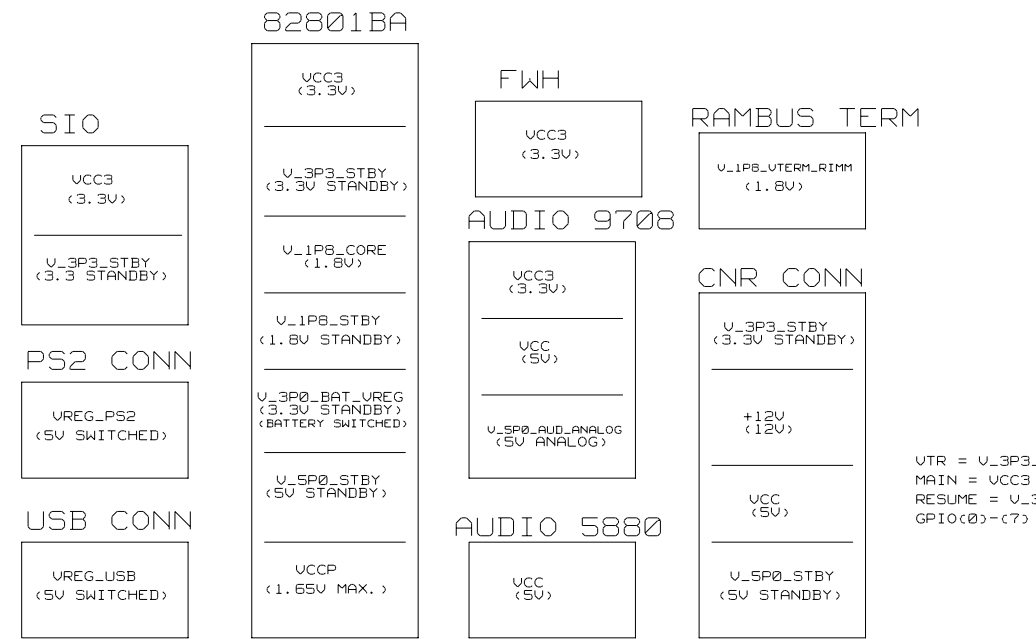
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FOLSOM, CALIFORNIA 95630 SHEET: 6

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DEVICE	NAME	I/O	POWER WELL	USAGE
FWH	FPI4	I	MAIN	NORM# (4.7K P-DOWN)
FWH	FPI3	I	MAIN	MFG_MODE (4.7K P-UP, UCC3)
FWH	FPI2	I	MAIN	PULLED DOWN (10K P-DOWN)
FWH	FPI1	I	MAIN	DMAB6_DETECT_SEC# (15K P-DOWN)
FWH	FPI0	I	MAIN	DMAB6_DETECT_PRI# (15K P-DOWN)
ICH	GPIO[0]	I	MAIN	REQA* (10K P-UP, UCC)
ICH	GPIO[1]	I	MAIN	REQB*\REQ5* (10K P-UP, UCC)
ICH	GPIO[2]-[5]	I	MAIN	PIRQ[E-H] (1K P-UP, UCC3)
ICH	GPIO[6]	I	MAIN	GPIO_ICH2_GPIO6 (10K P-UP, UCC3)
ICH	GPIO[7]	I	MAIN	GPIO_ICH2_GPIO7 (10K P-UP, UCC3)
ICH	GPIO[8]	I	RESUME	GPIO_ICH2_GPIO8 (10K, U_3P3_STBY)
ICH	GPIO[11]	I	RESUME	SMBALERT (22K P-UP, U_3P3_STBY)
ICH	GPIO[12]	I	RESUME	GPIO_SMI_OUT* (10K P-UP, U_3P3_STBY)
ICH	GPIO[13]	I	RESUME	GPIO_PME_SIO_OUT* (22K P-UP, U_3P3_STBY)
ICH	GPIO[16]	O	MAIN	GNTA* (INTERNAL P-UP)
ICH	GPIO[17]	O	MAIN	GNTB*\GNT5* (INTERNAL P-UP)
ICH	GPIO[18]	O	MAIN	TESTPOINT
ICH	GPIO[19]	O	MAIN	TESTPOINT
ICH	GPIO[20]	O	MAIN	GPIO_RMB_SPD_WE* (JUMPER OPT.: 10K P-UP)
ICH	GPIO[21]	O	MAIN	TESTPOINT
ICH	GPIO[22]	OD	MAIN	TESTPOINT
ICH	GPIO[23]	O	MAIN	TESTPOINT
ICH	GPIO[24]	I/O	RESUME	GPIO_LAN_DISABLE (INTERNAL P-UP)
ICH	GPIO[25]	I/O	RESUME	TESTPOINT
ICH	GPIO[27]	I/O	RESUME	GPIO_YELLOW_BLINK
ICH	GPIO[28]	I/O	RESUME	GPIO_GREEN_BLINK
SIO	GP10-GP17	I/O	UCC3	TESTPOINT
SIO	GP20	I/O	UCC3	AUD_EN (10K P-DOWN)
SIO	GP21	I/O	UCC3	NO_POP* (10K P-DOWN)
SIO	GP22	I/O	UCC3	GPIO_RMB_FREQ0 (4.7K P-UP, UCC3)
SIO	GP24	I/O	UCC3	SIO_SYSOPT (OPT. 4.7K P-UP UCC3, P-DOWN)
SIO	GP25	I/O	UCC3	TESTPOINT
SIO	GP26	I/O	UCC3	CDC_DWN_ENAB* (10K P-DWN THRU 1K SERIES)
SIO	GP27	I/O	UCC3	GPIO_SMI_OUT* (10K P-UP, U_3P3_STBY)
SIO	GP30	I/O	UCC3	FAN_TACH2 (10K P-DOWN)
SIO	GP31	I/O	UCC3	FAN_TACH1 (10K P-DOWN)
SIO	GP32	I/O	UCC3	FAN2_PWM
SIO	GP33	I/O	UCC3	FAN1_PWM
SIO	GP34	I/O	UCC3	IRRX2 (10K P-UP, UCC)
SIO	GP35	I/O	UCC3	IRTX2
SIO	GP36	I/O	UCC3	KBRST* (10K P-UP, UCC3)
SIO	GP37	I/O	UCC3	A20GATE (10K P-UP, UCC3)
SIO	GP40	I/O	UCC3	DRVDEN0
SIO	GP41	I/O	UCC3	DRVDEN1
SIO	GP42	I/O	UCC3	GPIO_PME_SIO_OUT* (22K P-UP, U_3P3_STBY)
SIO	GP43	I/O	UCC3	TESTPOINT
SIO	GP50, 51, 52, 54	I/O	UCC3	HDR (4.7K P-UP, UCC3 OR 470 OHM P-DOWN)
SIO	GP53	I/O	UCC3	HDR (4.7K P-UP, UCC3 OR 470 OHM P-DOWN)
SIO	GP55-57	I/O	UCC3	TEST POINT
SIO	GP60	I/O	UCC3	GPIO_RMB_PWRCTRL* (10K/4.7K P-UP OR P-DOWN)
SIO	GP61	I/O	UCC3	GPIO_RMB_FREQ1 (4.7K P-UP, UCC3)



UTR = V_3P3_STBY
 MAIN = UCC3
 RESUME = V_3P3_STBY
 GPIO[0]-[7] ARE 5V TOLERANT (REMAINDER 3.3V TOLERANT)

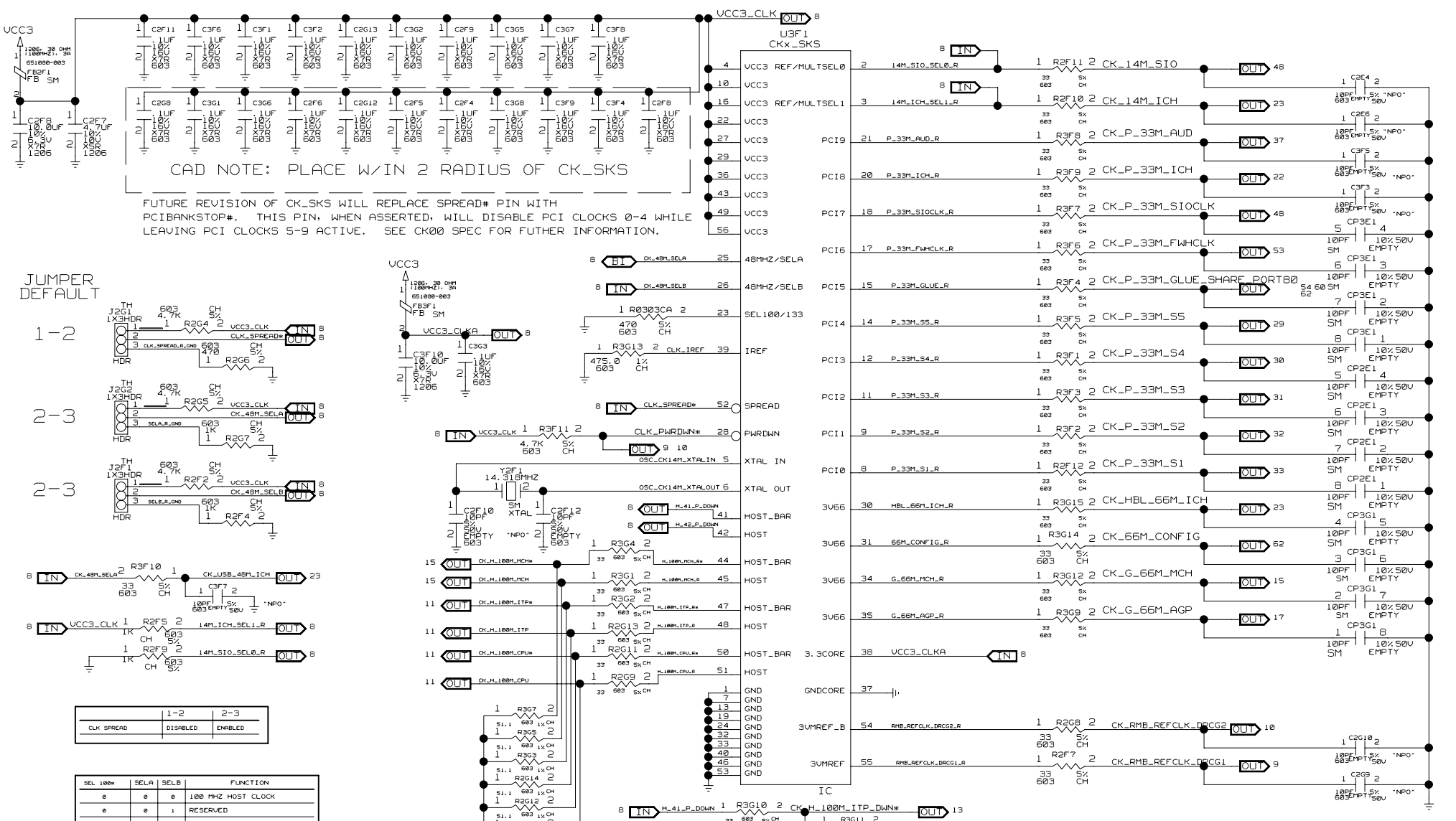
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 INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD

PAGE TITLE:
 PWR DISTRIBUTION & GPIO TABLE

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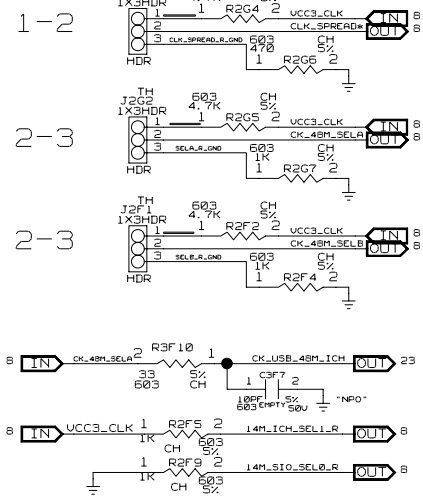
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CAD NOTE: PLACE W/IN 2 RADIUS OF CK_SKS

FUTURE REVISION OF CK_SKS WILL REPLACE SPREAD* PIN WITH PCIBANKSTOP#. THIS PIN, WHEN ASSERTED, WILL DISABLE PCI CLOCKS 0-4 WHILE LEAVING PCI CLOCKS 5-9 ACTIVE. SEE CK00 SPEC FOR FURTHER INFORMATION.

JUMPER DEFAULT



	1-2	2-3
CLK SPREAD	DISABLED	ENABLED

SEL_100*	SELA	SELB	FUNCTION
0	0	0	100 MHZ HOST CLOCK
0	0	1	RESERVED
0	1	0	RESERVED
0	1	1	ALL OUTPUTS TRI-STATE

SCHEMATIC TITLE:
INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD

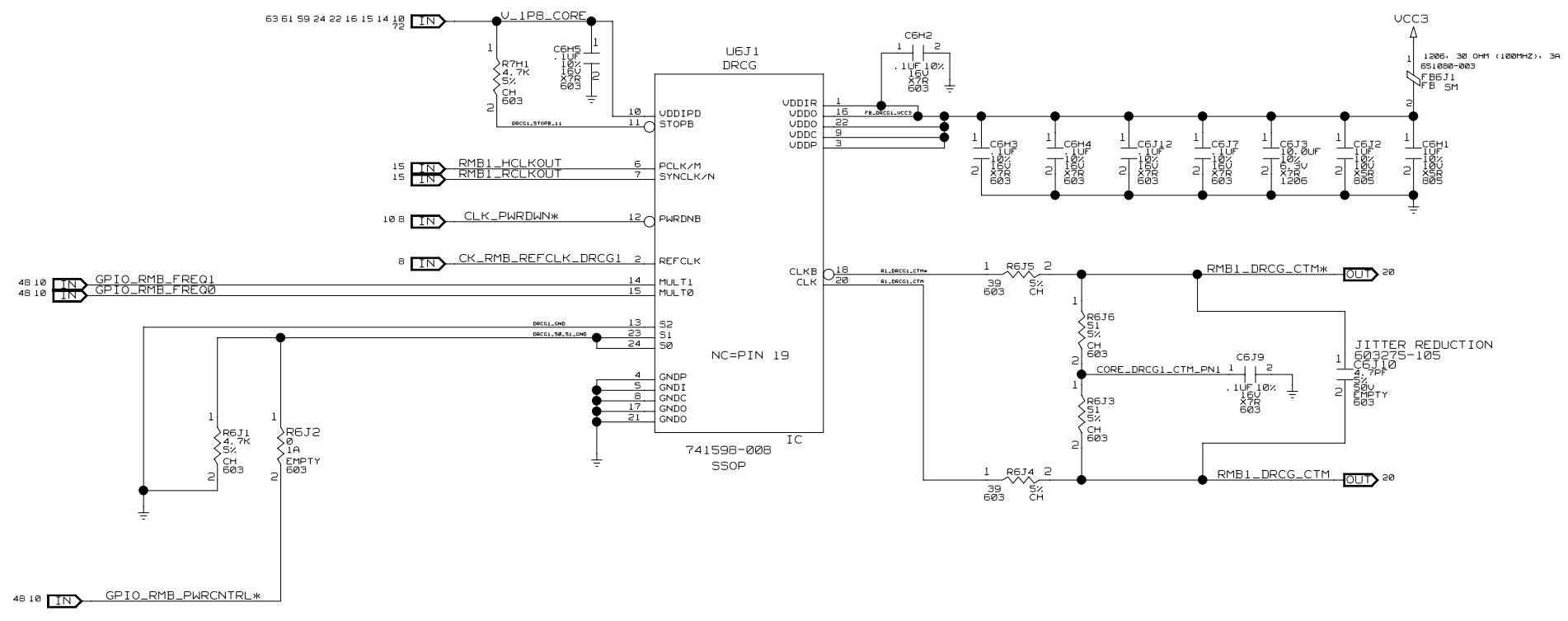
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CK_SKS: CLOCK GENERATOR

REV: 3.0

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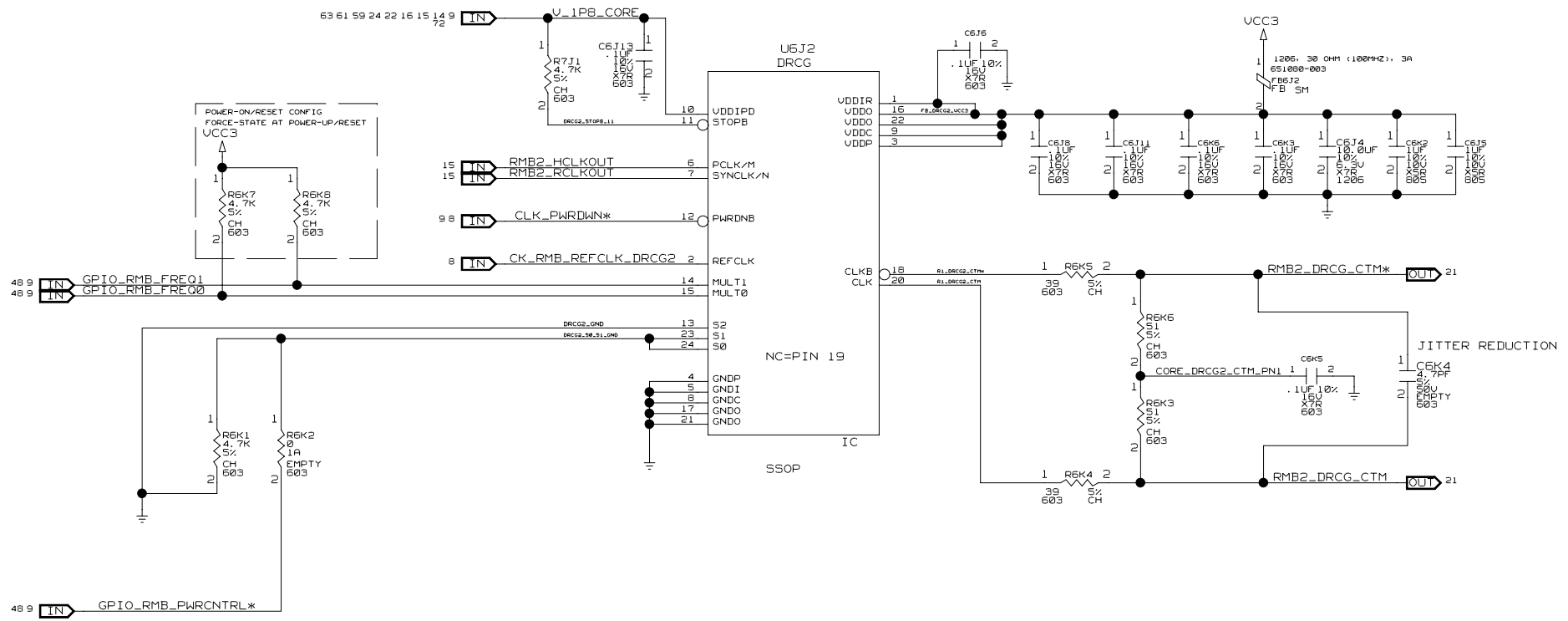
FUNCTION	S0	S1	CLK	CLKB
NORMAL	0	0	NORM	NORM
BYPASS	1	0	ALLCLK	ALLCLKB
TEST	1	1	REFCLK	REFCLKB
OUTPUT TEST (OE)	0	1	H1-Z	H1-Z

MULT0	MULT1	PLLCLK	REFCLK
0	0	4	1
0	1	6	1
1	1	8	1
1	0	0	3

REFCLK & PLL MULTIPLIER SELECT TABLE

SCHEMATIC TITLE:
 INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD
 PAGE TITLE: DRCG-1: CHA
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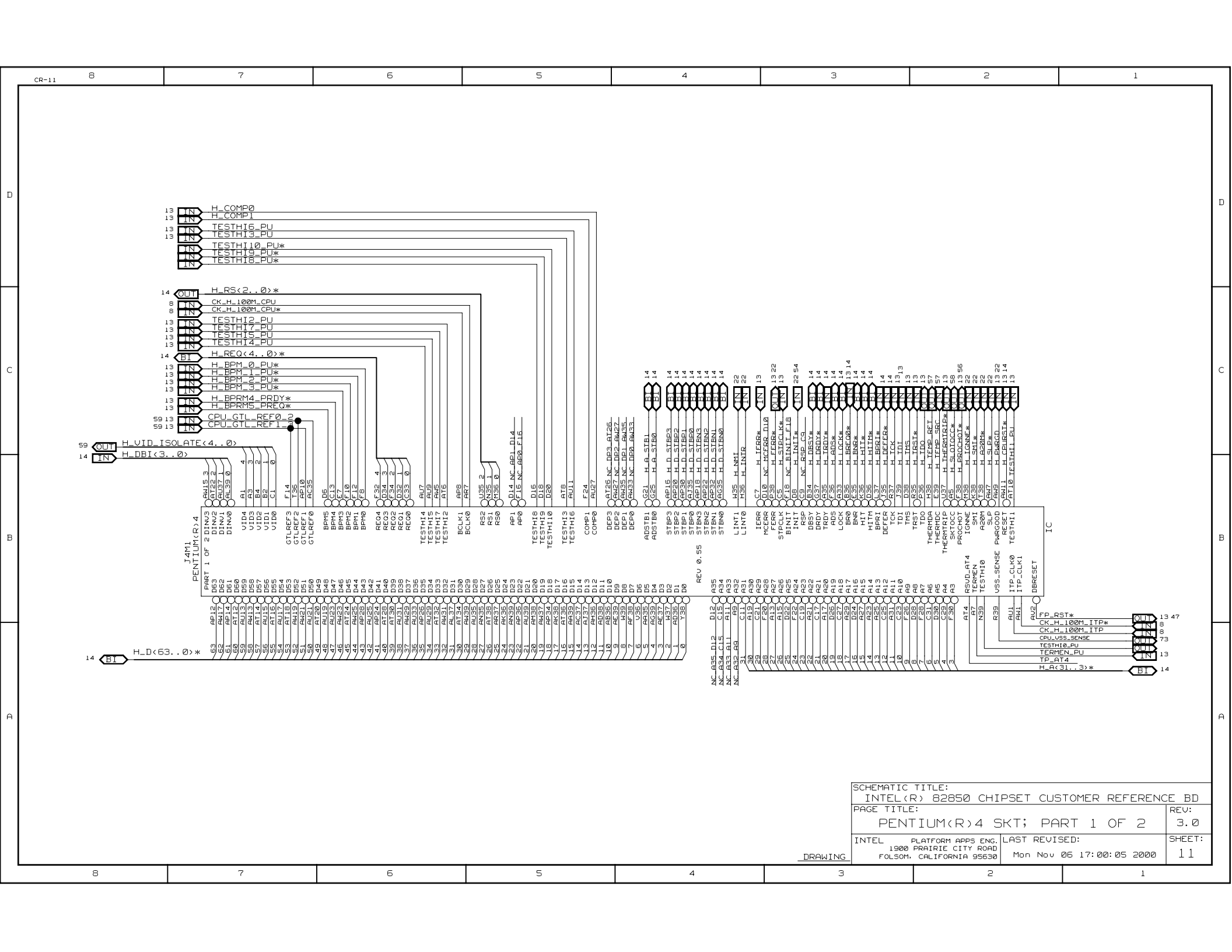


MULT0	MULT1	PLLCLK	REFCLK
0	0	4	1
0	1	6	1
1	1	8	1
1	0	0	3

REFCLK & PLL MULTIPLIER SELECT TABLE

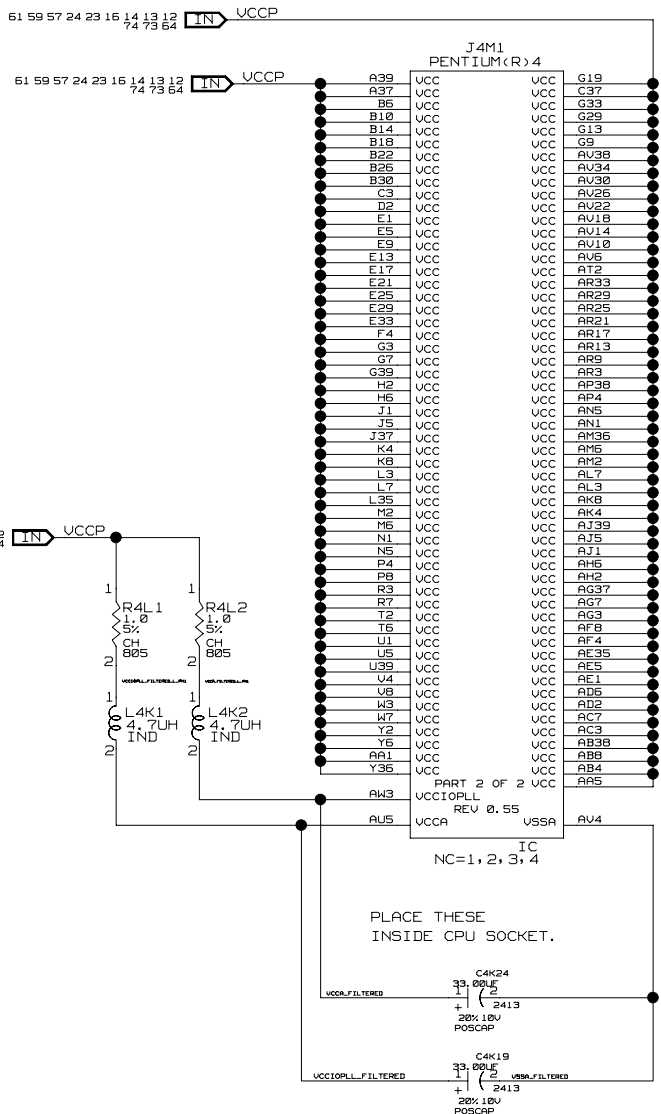
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 FOLSOM, CALIFORNIA 95630

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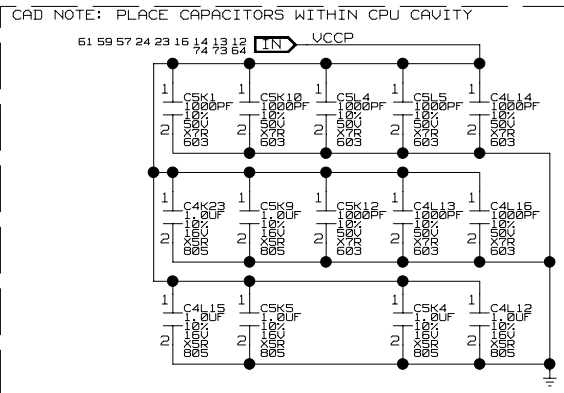
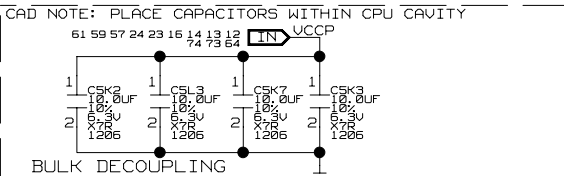
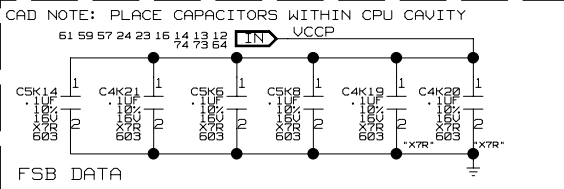
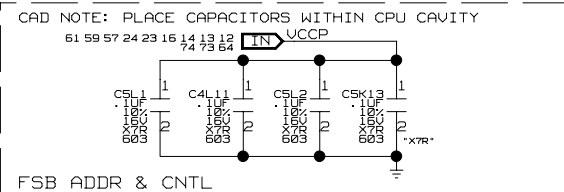


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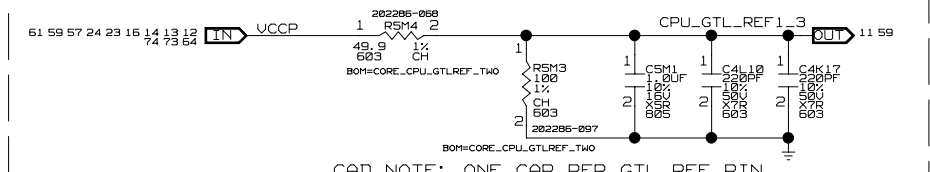
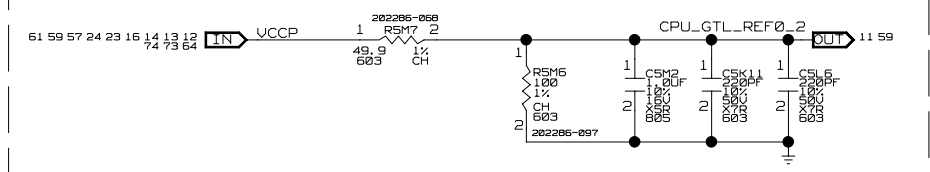
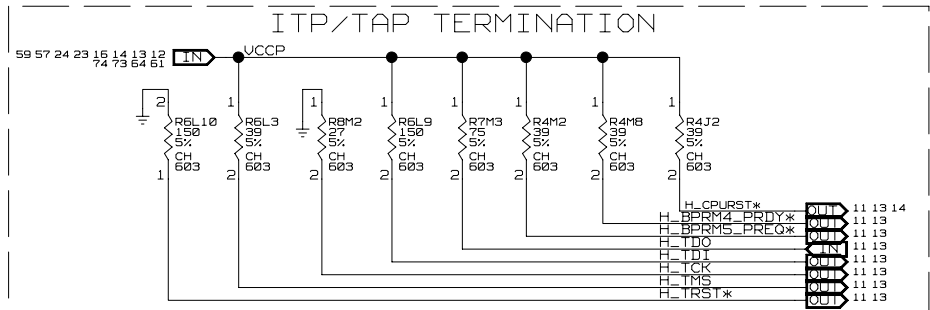
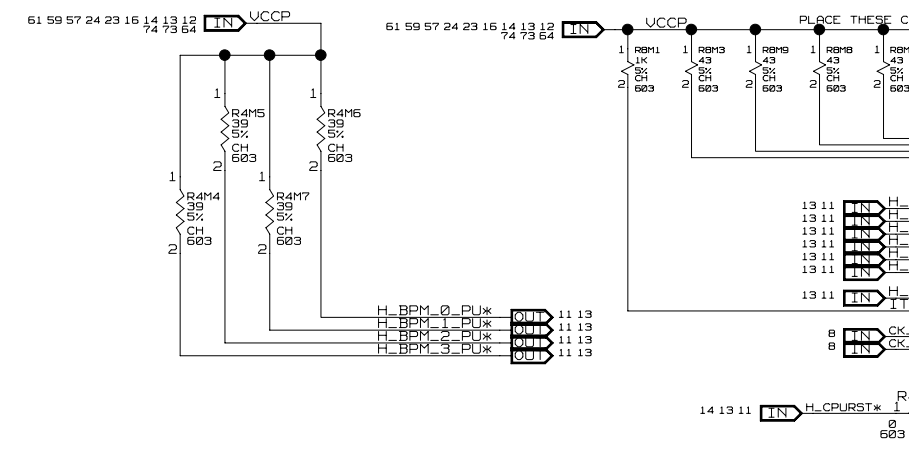
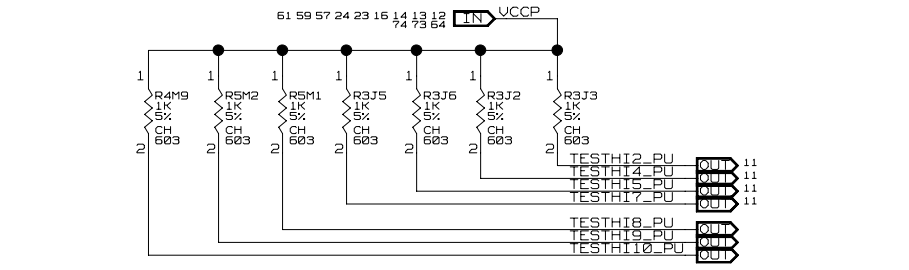
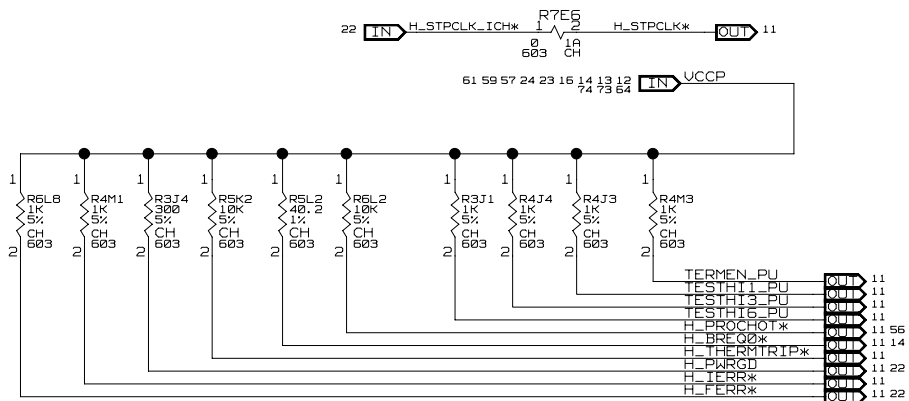


PROCESSOR SOCKET DECOUPLING

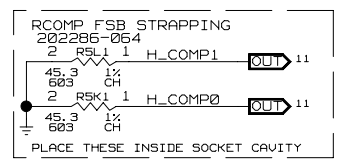


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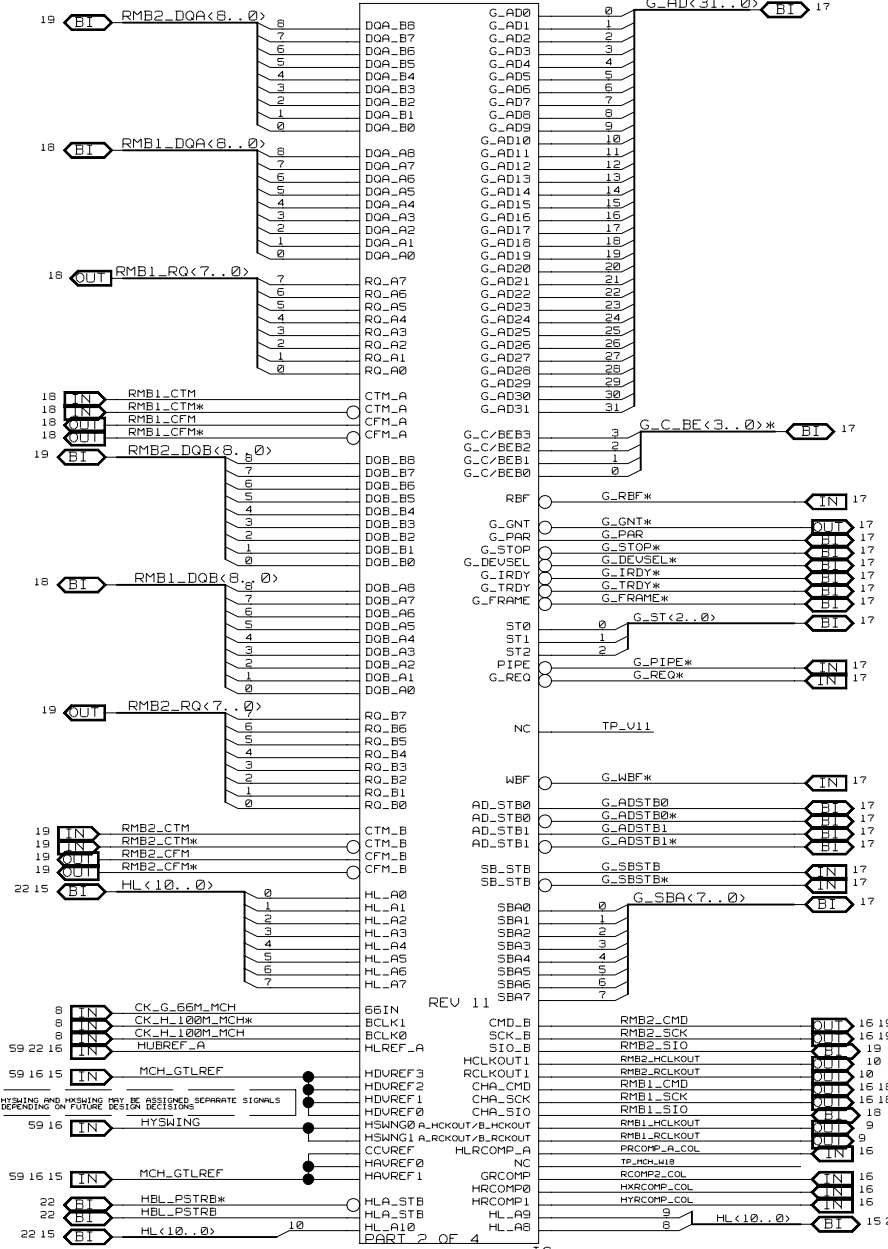
CAD NOTE: ONE CAP PER GTL REF PIN



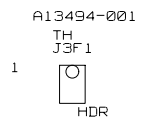
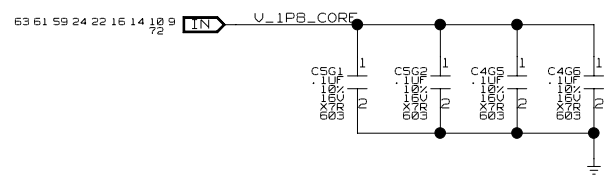
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U5G1
82850

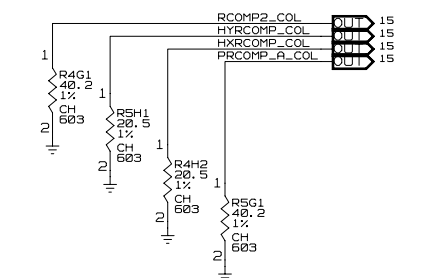
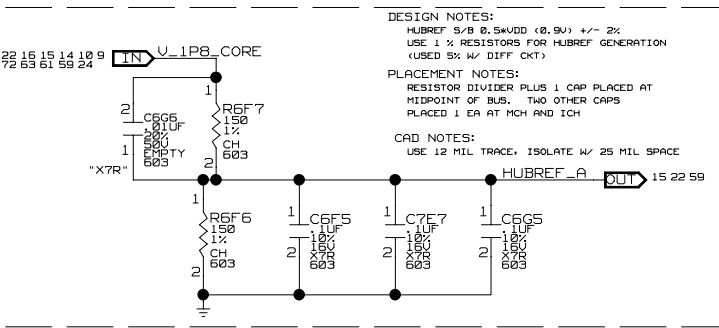
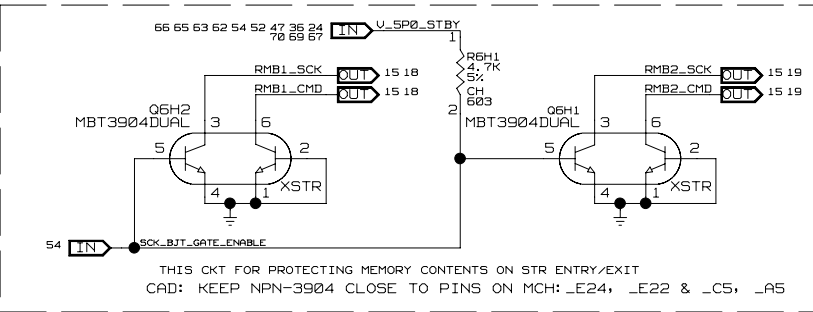
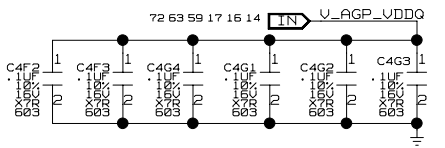
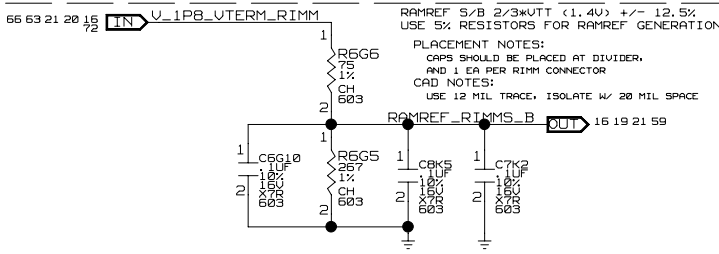
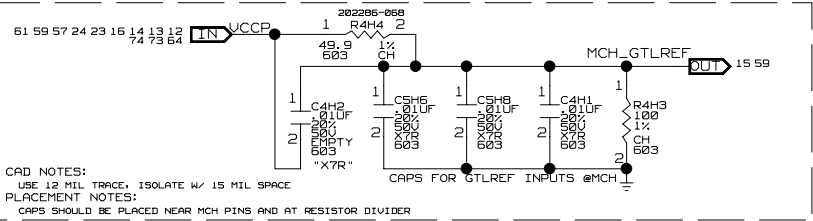
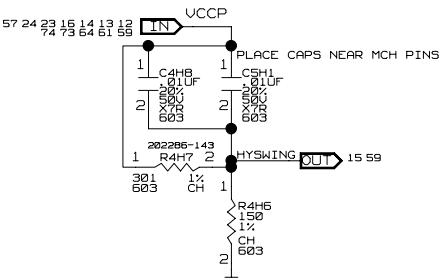
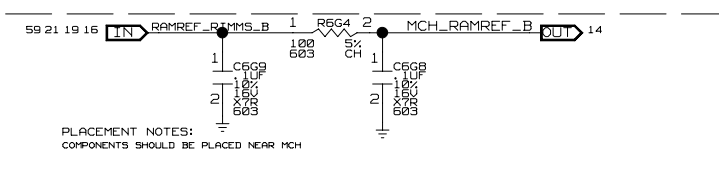
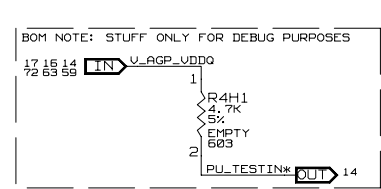
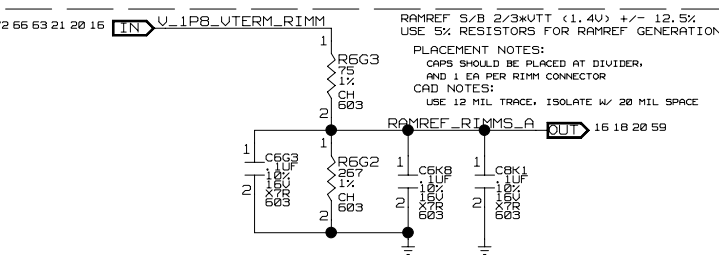
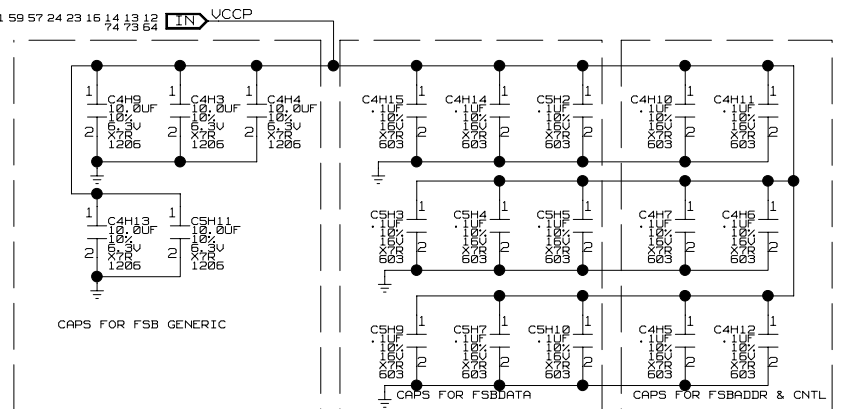
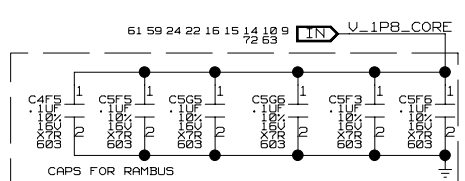
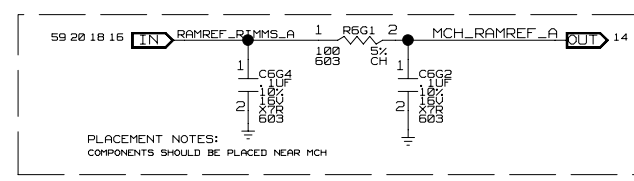


LAYOUT NOTE: ADDITIONAL BACKSIDE DECOUPLING CAPS



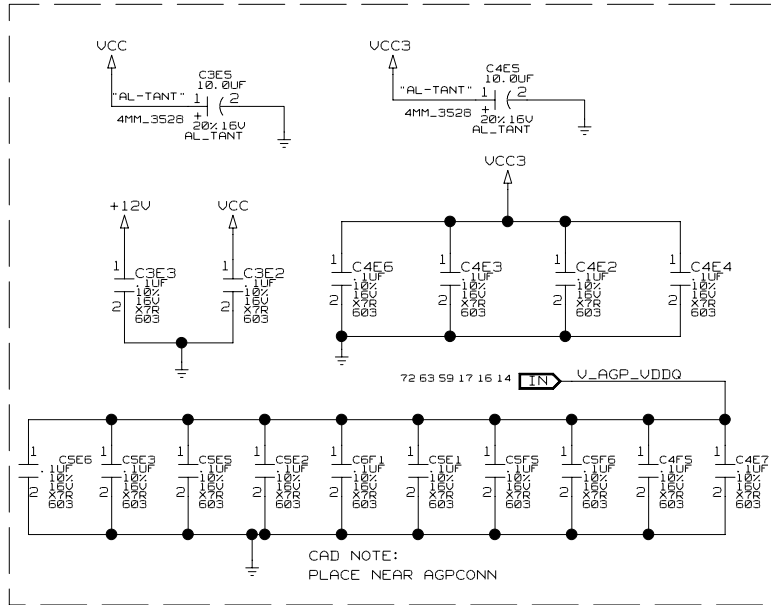
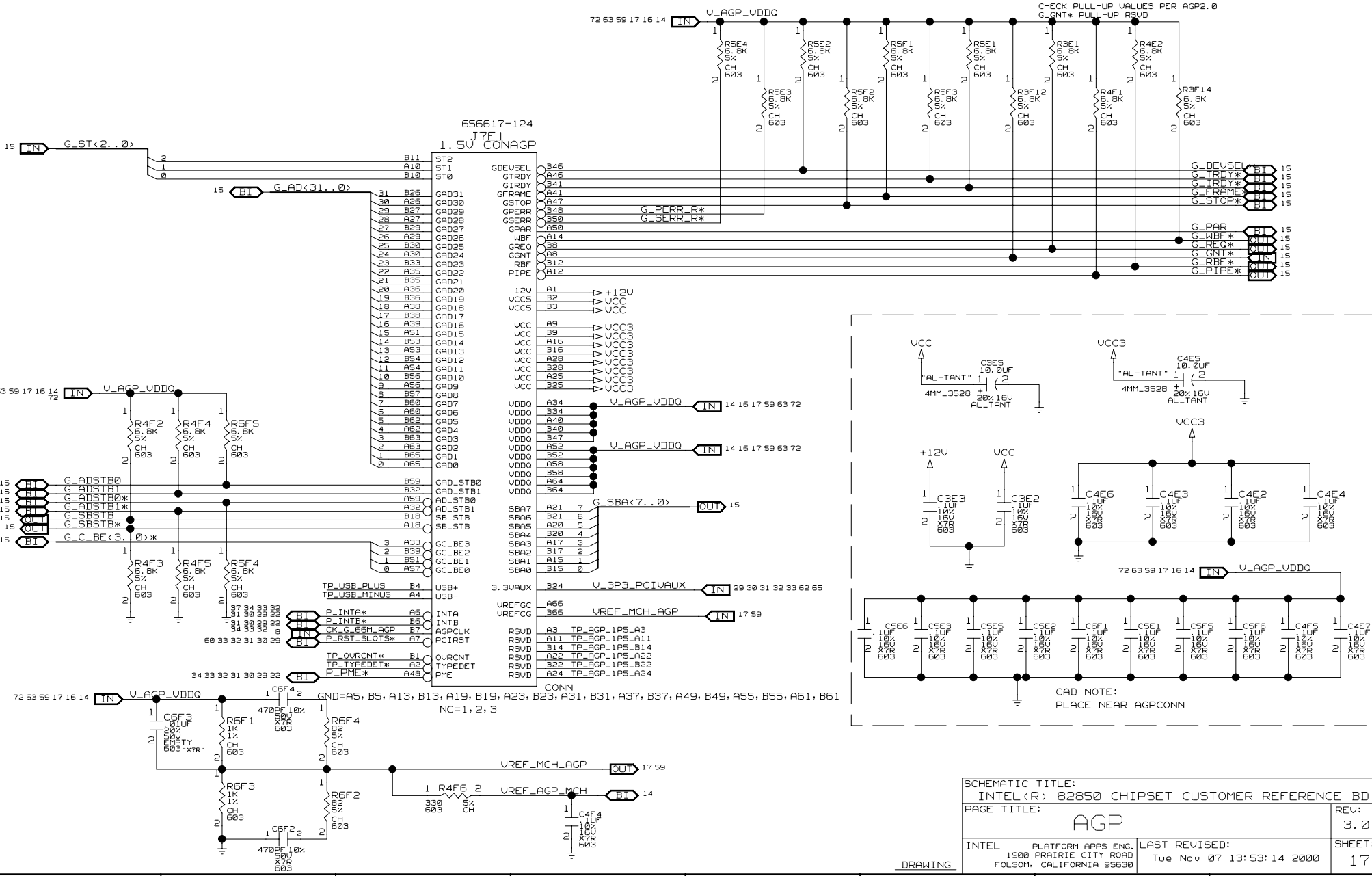
SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: MCH: PARTS 2 OF 4		REV: 3.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 13:40:53 2000	SHEET: 15

DRAWING



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: MCH DECOUPLING/STRAPPINGS		SHEET: 16
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 13:46:00 2000	

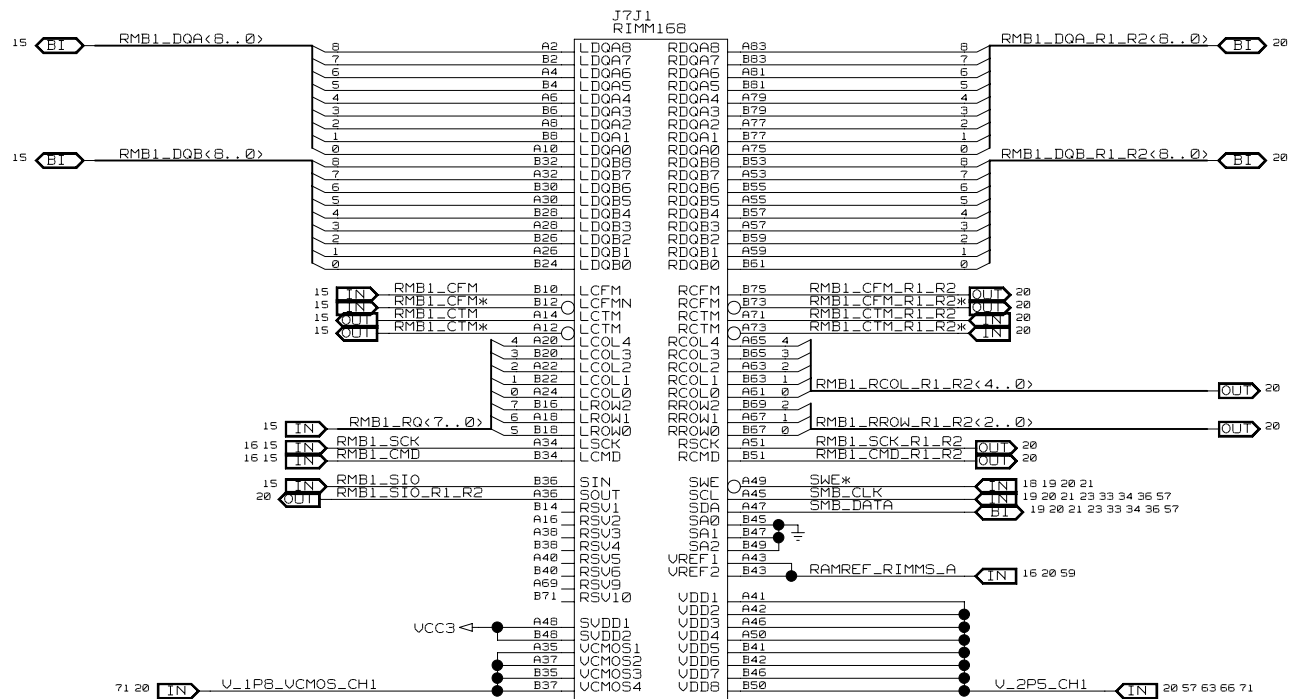
DRAWING



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: AGP		SHEET: 17
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 13:53:14 2000	

RAMBUS #1, RIMM1

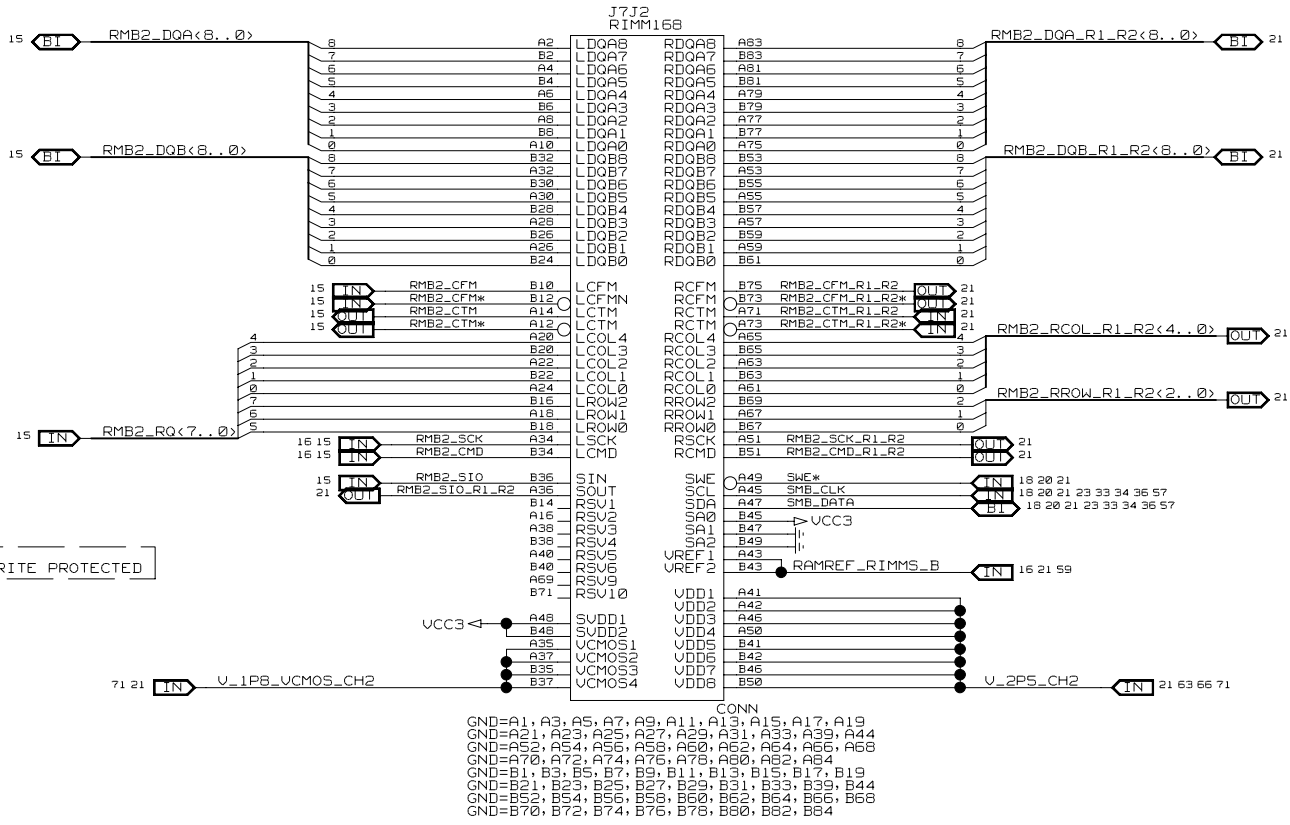
I2C ADDRESS: 000



SCHEMATIC TITLE:	
INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE:	REV:
CHANNEL #1, RIMM #1	3.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 13:54:57 2000
DRAWING	SHEET: 18

RAMBUS #2, RIMM1

I2C ADDR: 001



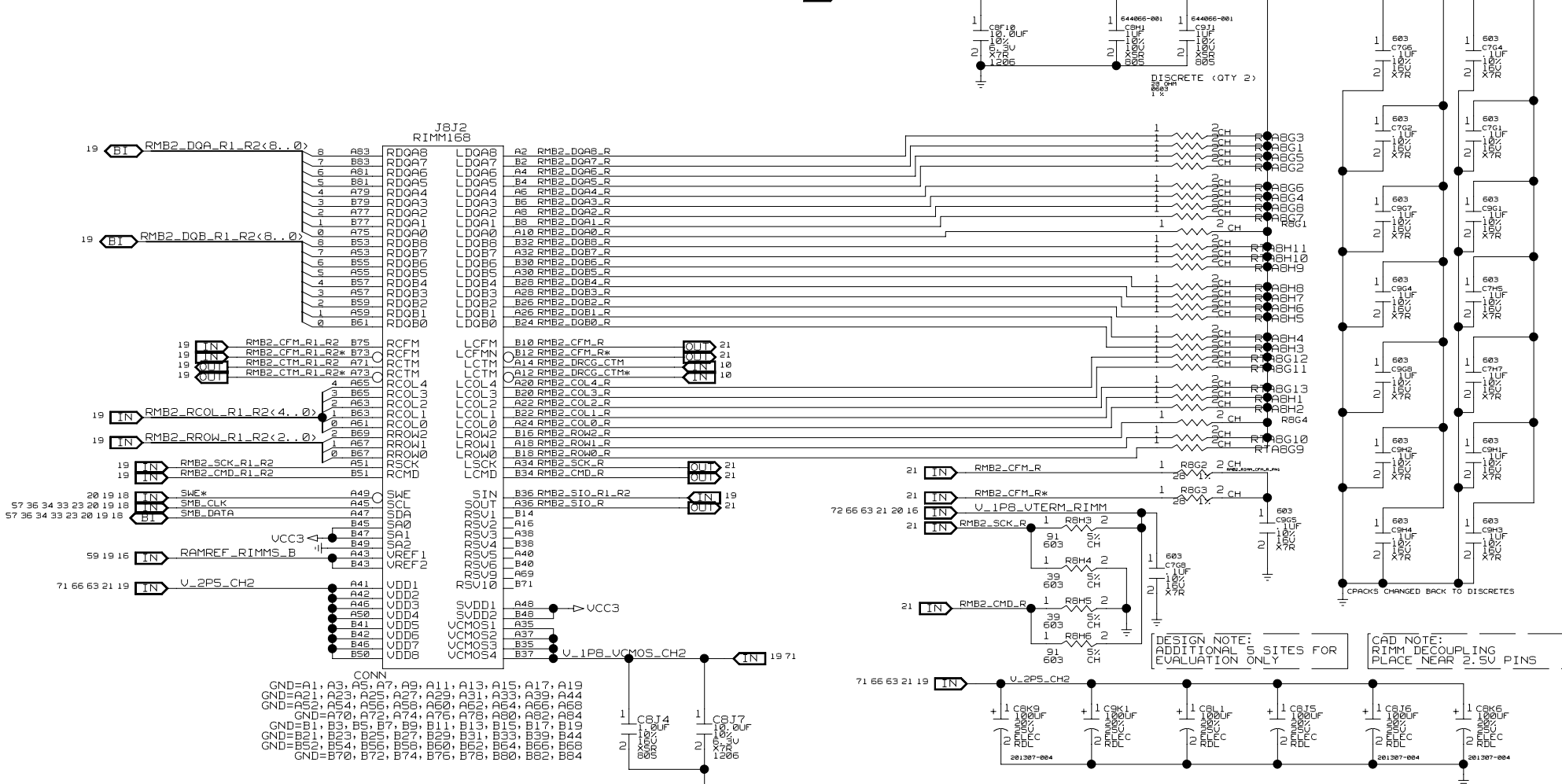
DESIGN NOTE:
SWE: 'HIGH' IS WRITE PROTECTED

SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE: CHANNEL #2, RIMM #1	REV: 3.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 14:26:22 2000
DRAWING	SHEET: 19

RAMBUS #2, RIMM2

I2C ADDR: 011

CAD NOTE:
PLACE ONE CAP PER 2 RESISTORS



DESIGN NOTE:
ADDITIONAL 5 SITES FOR
EVALUATION ONLY

CAD NOTE:
RIMM DECOUPLING
PLACE NEAR 2.5V PINS

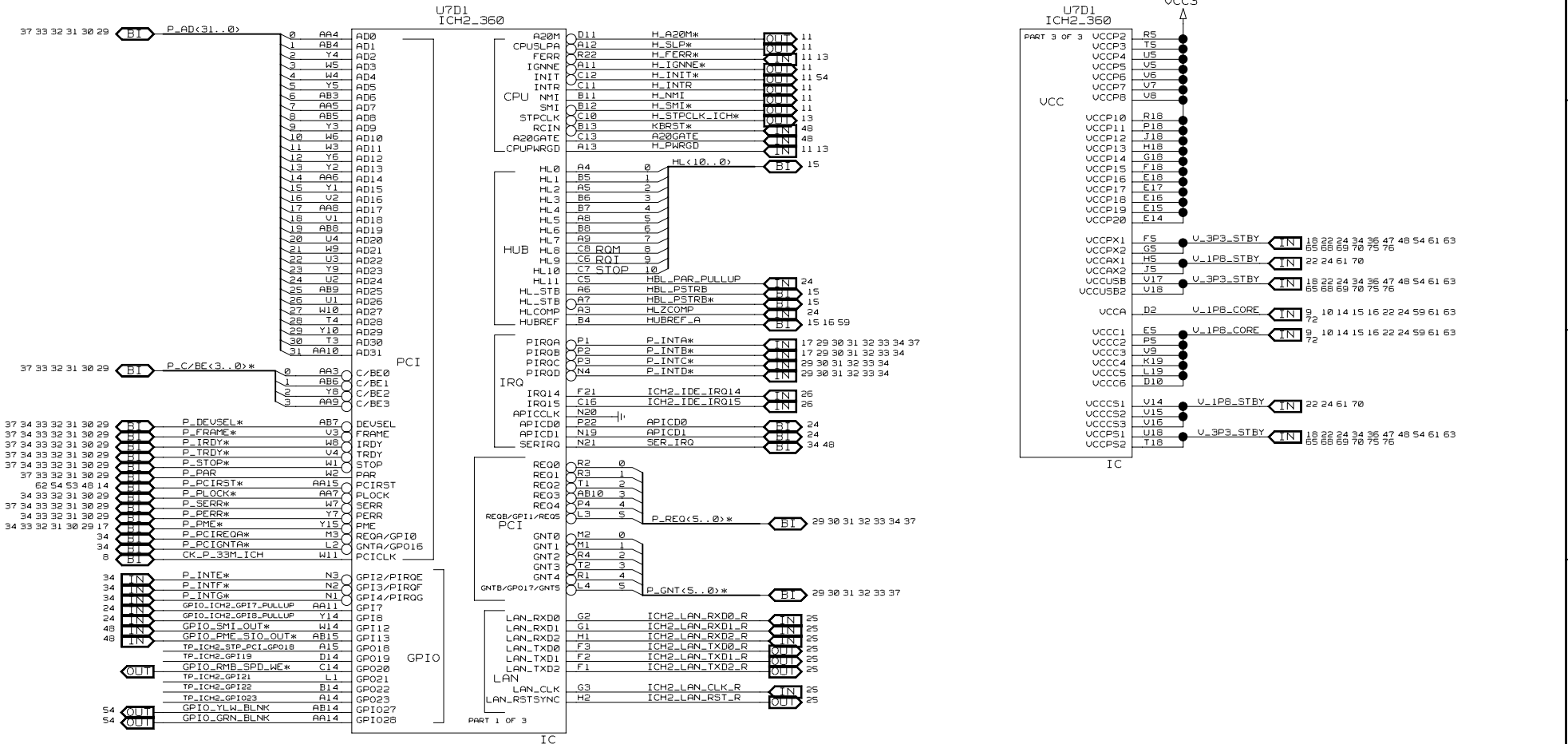
SCHEMATIC TITLE:
INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD

PAGE TITLE:
CHANNEL #2, RIMM #2

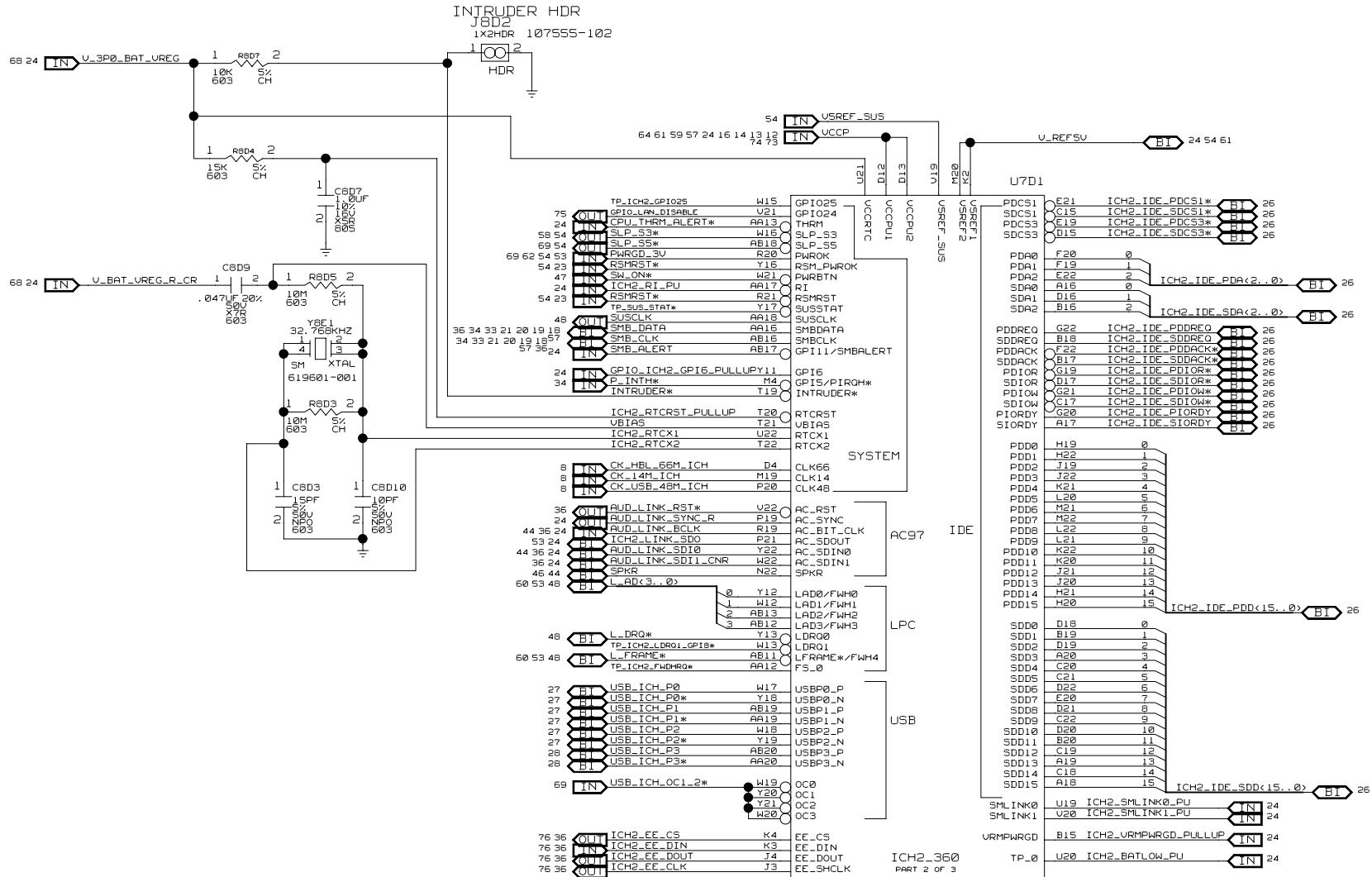
REV:
3.0

INTEL PLATFORM APPS ENG. LAST REVISED: Tue Nov 07 14:31:24 2000 **SHEET:**
FOLSOM, CALIFORNIA 95630 21

DRAWING

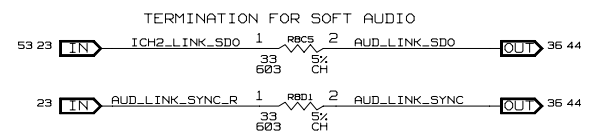
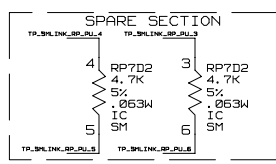
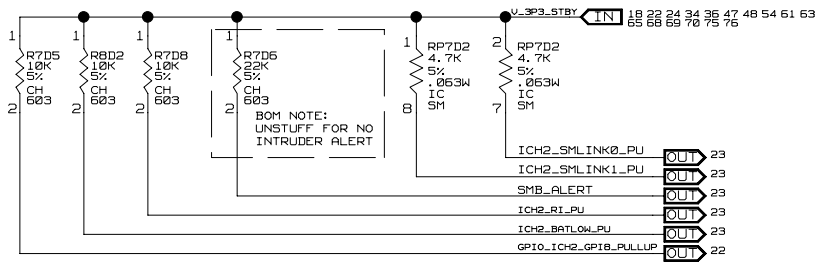
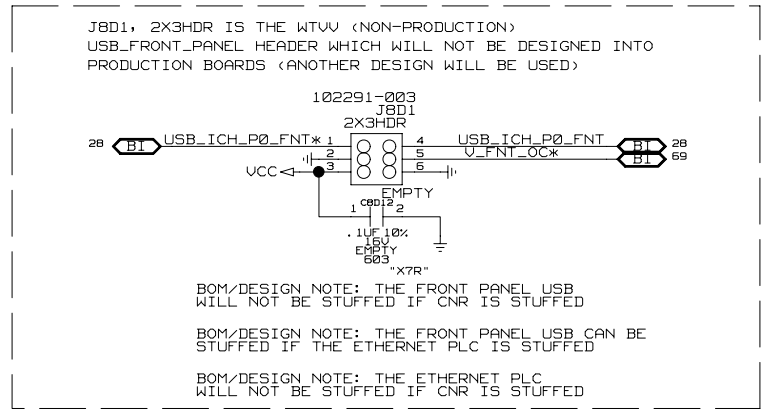
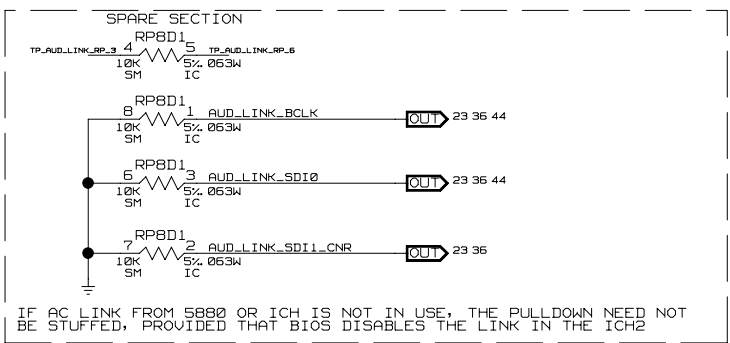
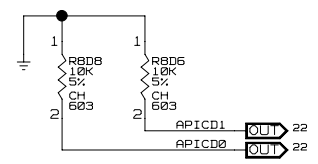
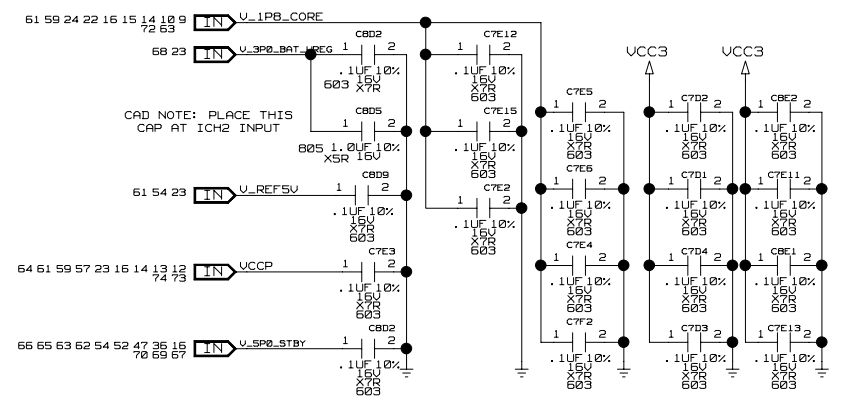
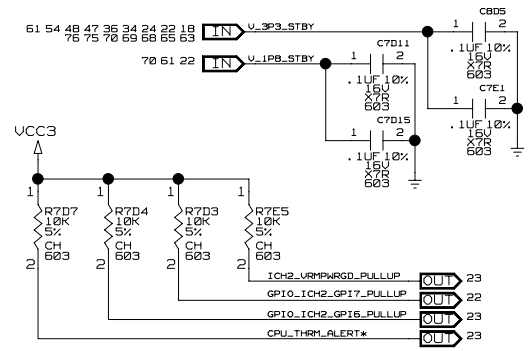
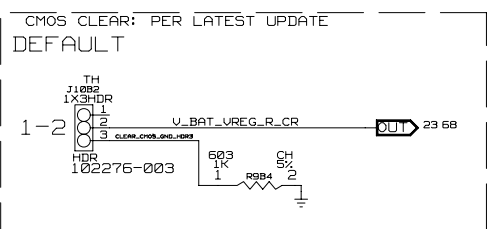


SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE: 82801BA: PCI/GPIO/HUB/IRQ	
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 14:49:58 2000
DRAWING	REV: 3.0 SHEET: 22



GND=B10, B9, C9, D9, D8, D7, D6, D5, C4, E6, E7, E8, E9, J9, . J14, K9, . K14, L9, . L14, M9, . M14, N9, . N14, P9, . P14
 GND=D3, K1, AA1, AA2, AB1, AB2, AA21, AA22, AB21, AB22, A1, A2, A21, A22, B1, B2, B3, B21, B22, C2, C3, A10

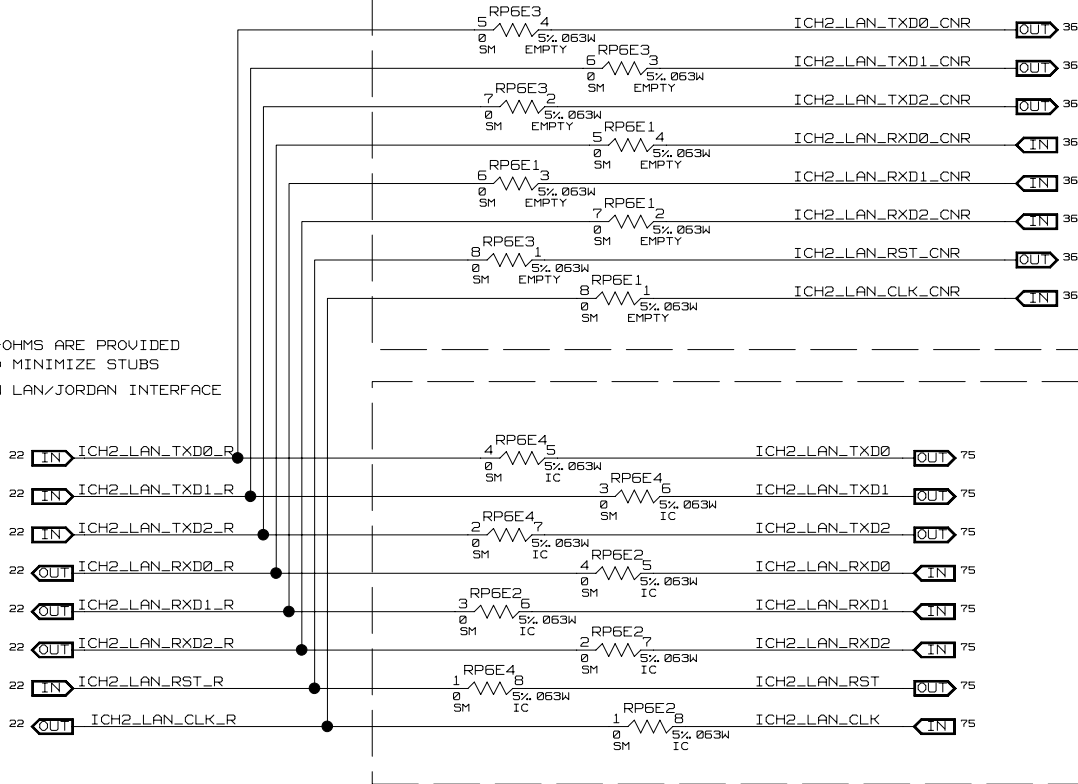
SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE: 82801BA: SYS-MGMT/AC97LPC/USB	REV: 3.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 14:52:05 2000
DRAWING	SHEET: 23



SCHEMATIC TITLE:	
INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE: ICH2 PULLUPS & DECOUPLING	REV: 3.0
LPC/ INTERRUPT/USB/PWR_MGMT/SMBUS	
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD, FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 15:16:29 2000
DRAWING	SHEET: 24

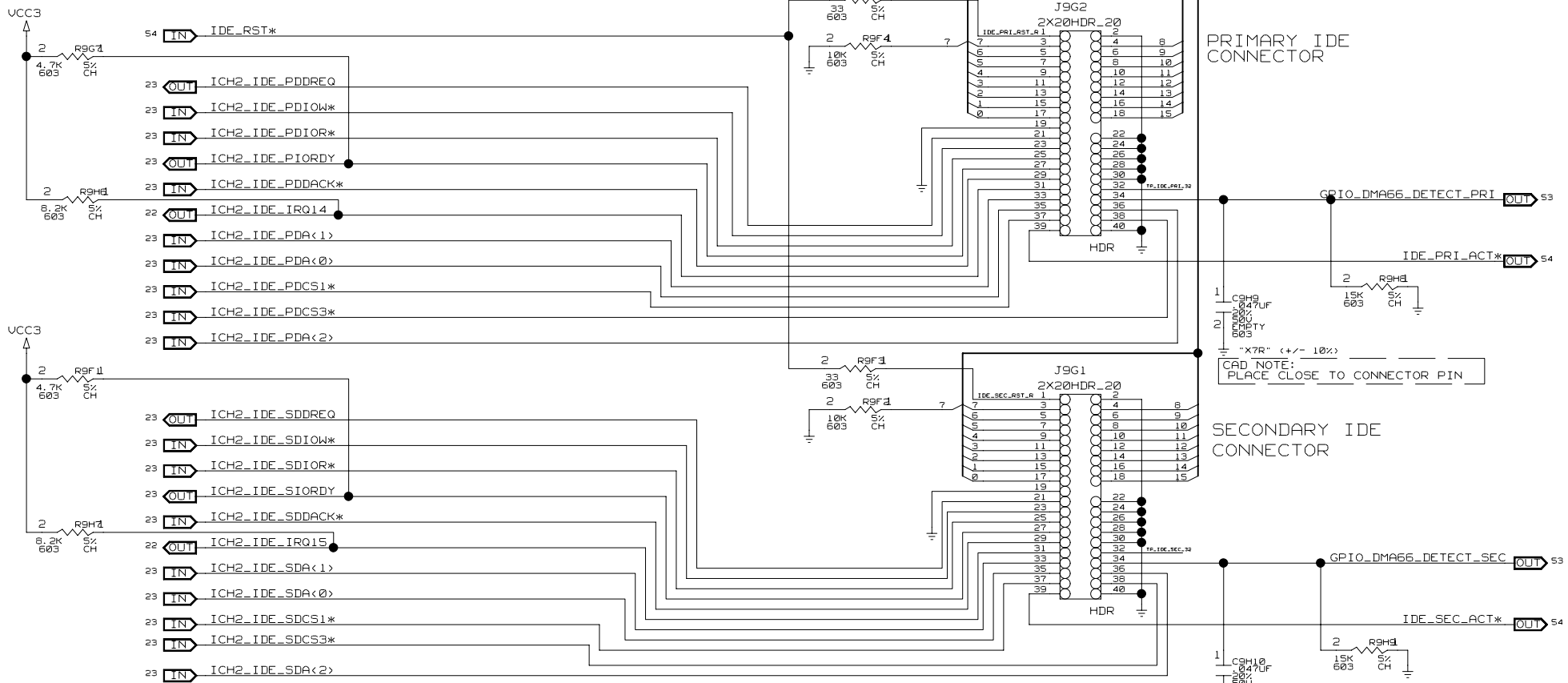
PROPERTIES FOR STUFFING OPTIONS: BOM=AUDIO_CNR
 CNR STUFFING OPTION FOR LAN-UP SOLUTION

0-OHMS ARE PROVIDED
 TO MINIMIZE STUBS
 ON LAN/JORDAN INTERFACE



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE: 82801BA/AC97 & CNR LINK STUFFING OPTION	
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 15:23:38 2000
DRAWING	REV: 3.0 SHEET: 25

DESIGN NOTE:
 SERIES RESISTORS INTEGRATED INTO ICH:
 VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS



PRIMARY IDE CONNECTOR

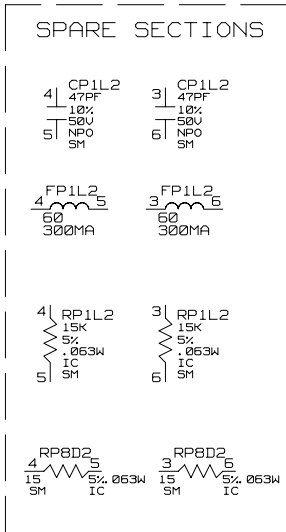
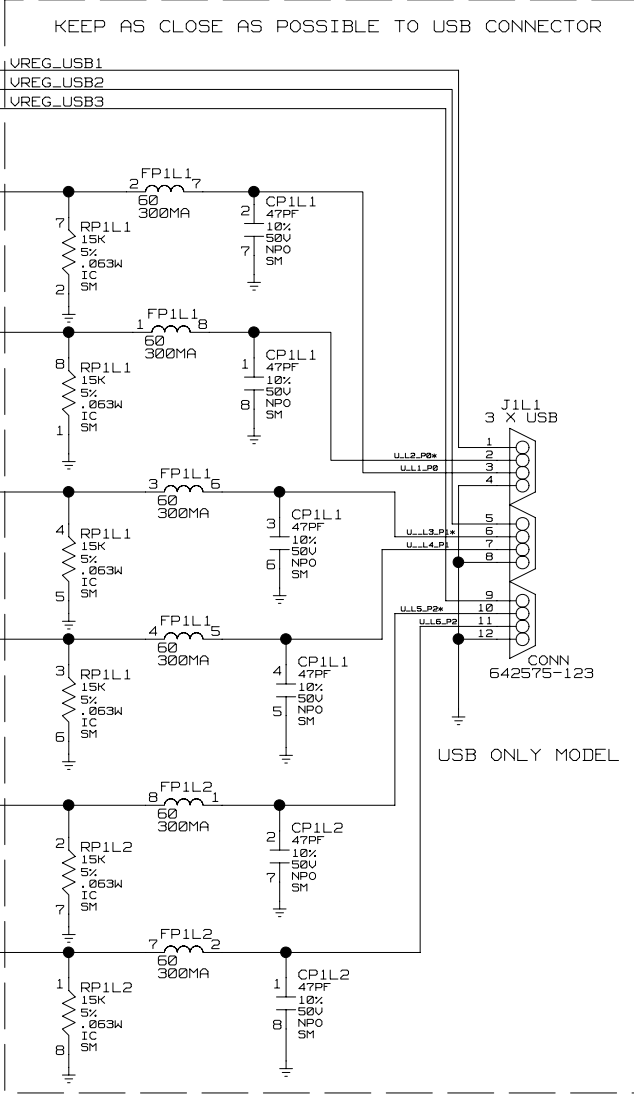
SECONDARY IDE CONNECTOR

CAD NOTE:
 PLACE CLOSE TO CONNECTOR PIN

CAD NOTE:
 PLACE CLOSE TO CONNECTOR PIN

SCHEMATIC TITLE: INTEL (R) 82850 CHIPSET CUSTOMER REFERENCE BD			REV: 3.0
PAGE TITLE: PCI IDE			SHEET: 25
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 16:17:19 2000		

DRAWING



USB ONLY MODEL

CONN 642575-123

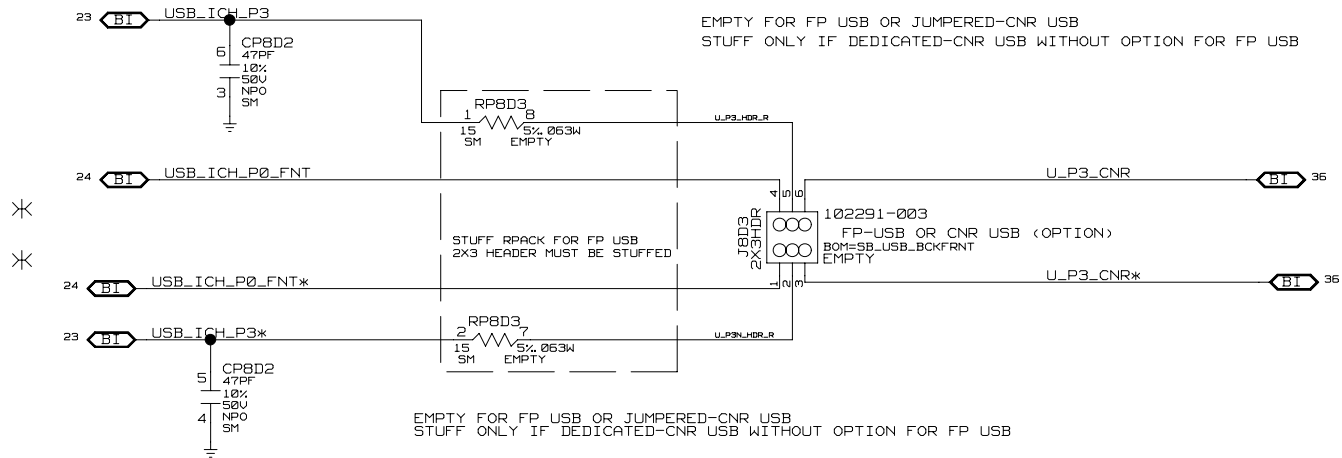
SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: USB TRIPLE HEADER		SHEET: 27
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 15:28:57 2000	

DRAWING

TPS TO INCLUDE/IDENTIFY FRONT PANEL SUPPORT REQUIREMENTS

JUMPER POSITION	FEATURE
1-2, 4-5	* FRONT PANEL USB
5-6, 2-3	CNR USB
	NO OTHER OPTIONS VALID

* DEFAULT STUFFING



SPARES

EMPTY FOR FP USB

RP8D3
4 5
15 5% 063W
SM EMPTY

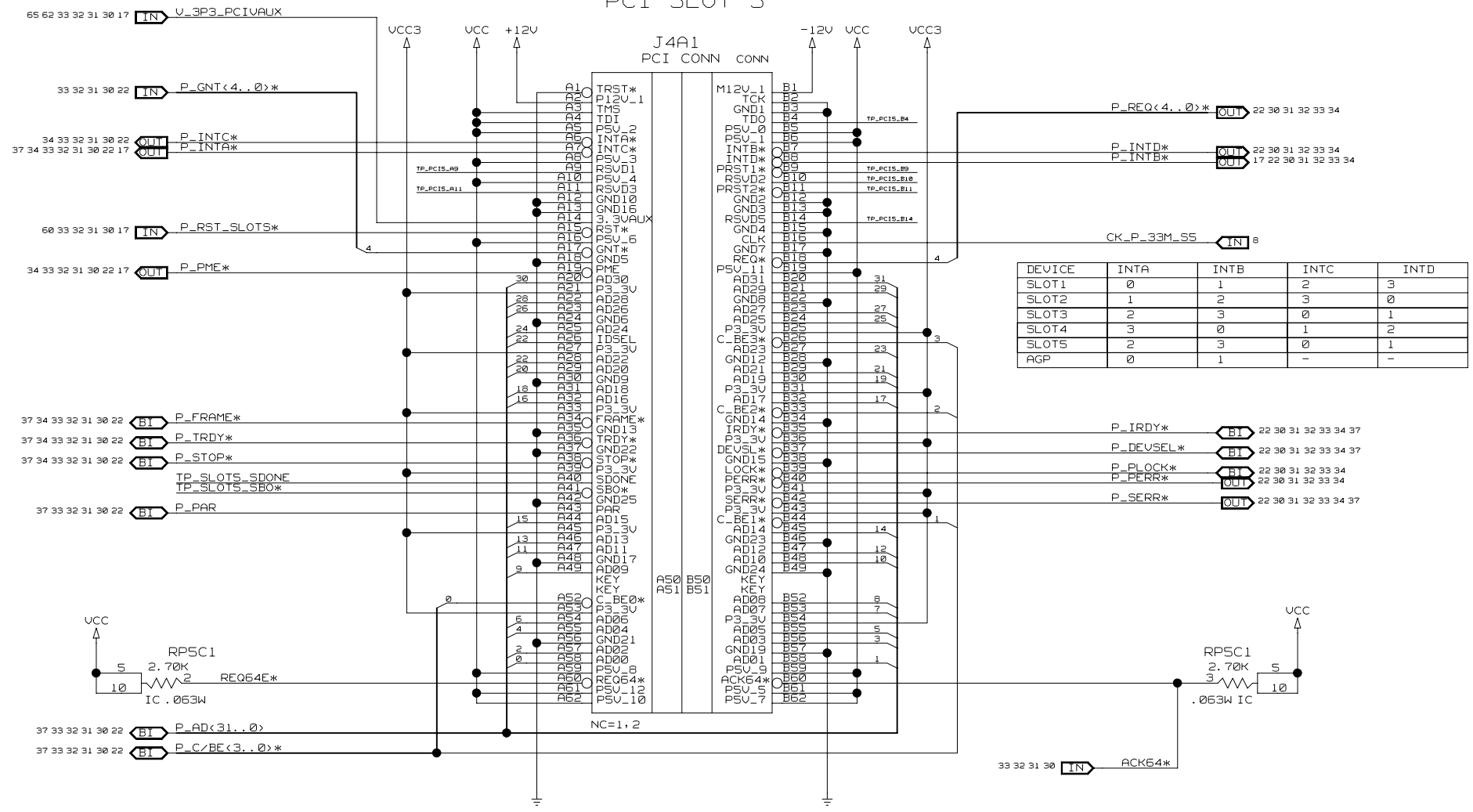
EMPTY FOR FP USB

RP8D3
3 5
15 5% 063W
SM EMPTY

SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: USB/FRONT PANEL HDR		SHEET: 28
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 15:30:17 2000	

DRAWING

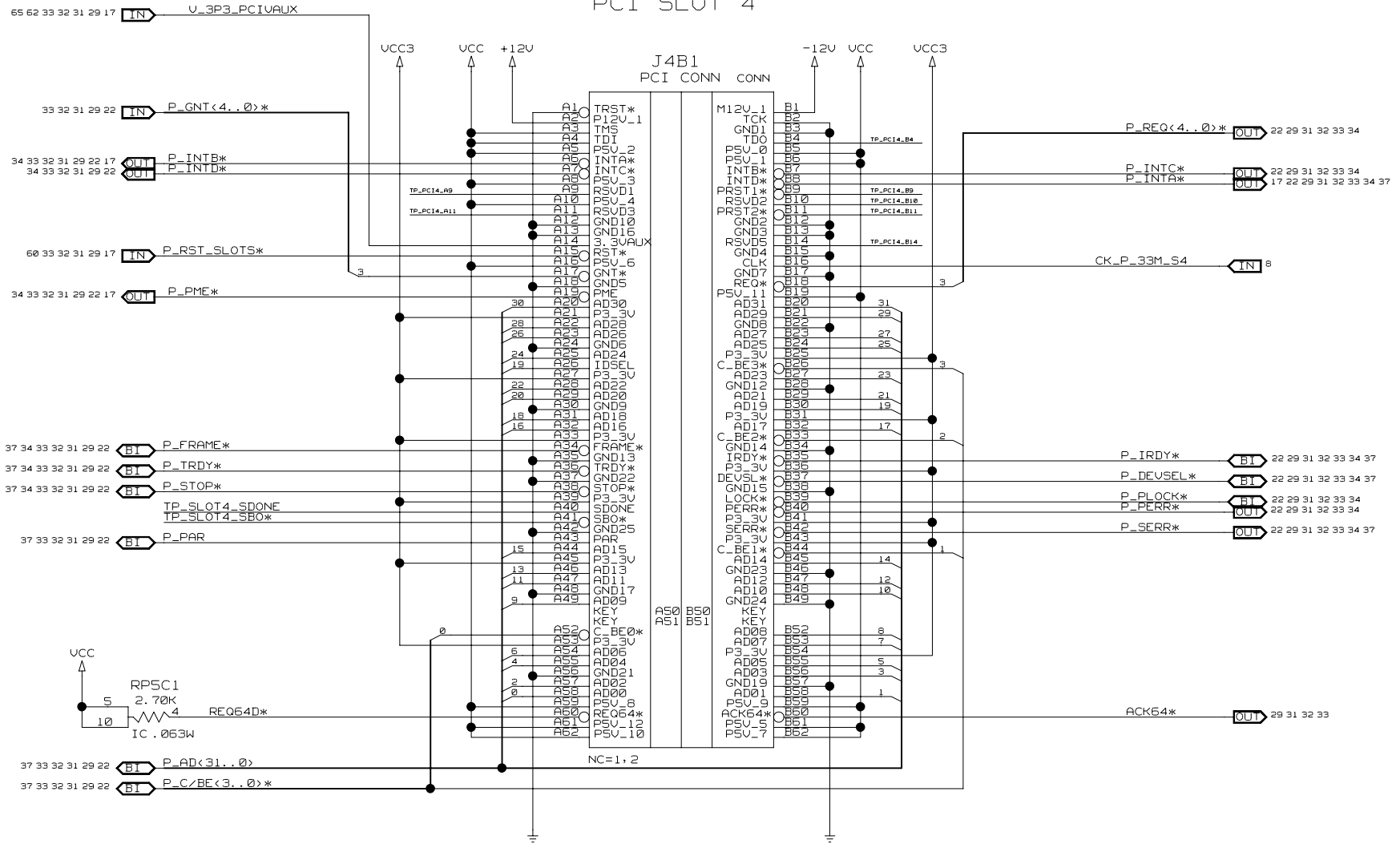
PCI SLOT 5



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: PCI SLOTS		SHEET: 29
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 15:36:43 2000	

DRAWING

PCI SLOT 4

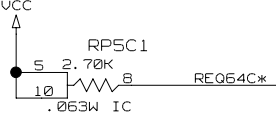
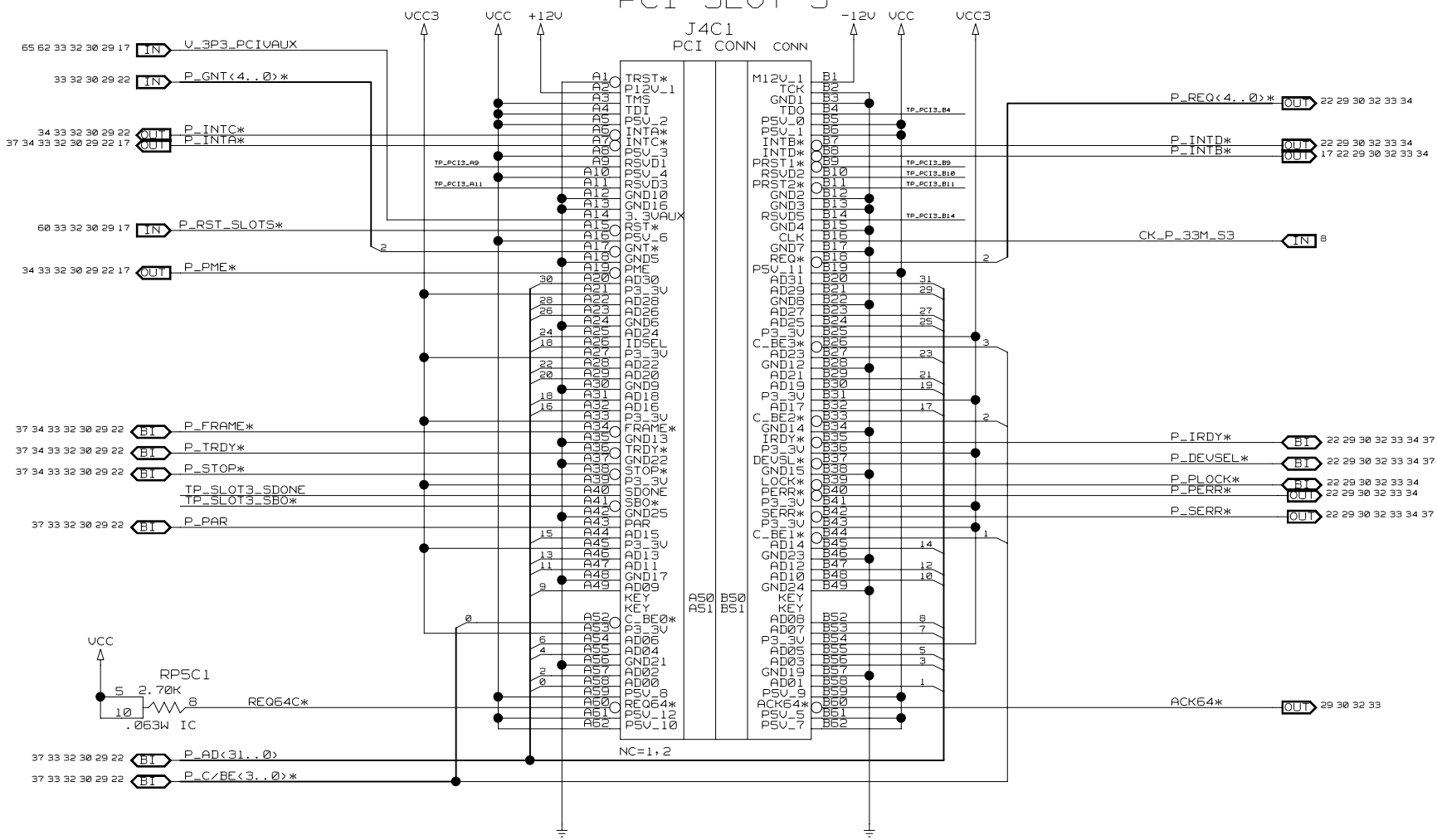


SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: PCI SLOT 4		SHEET: 30
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 15:37:49 2000	

DRAWING

PCI SLOT 3

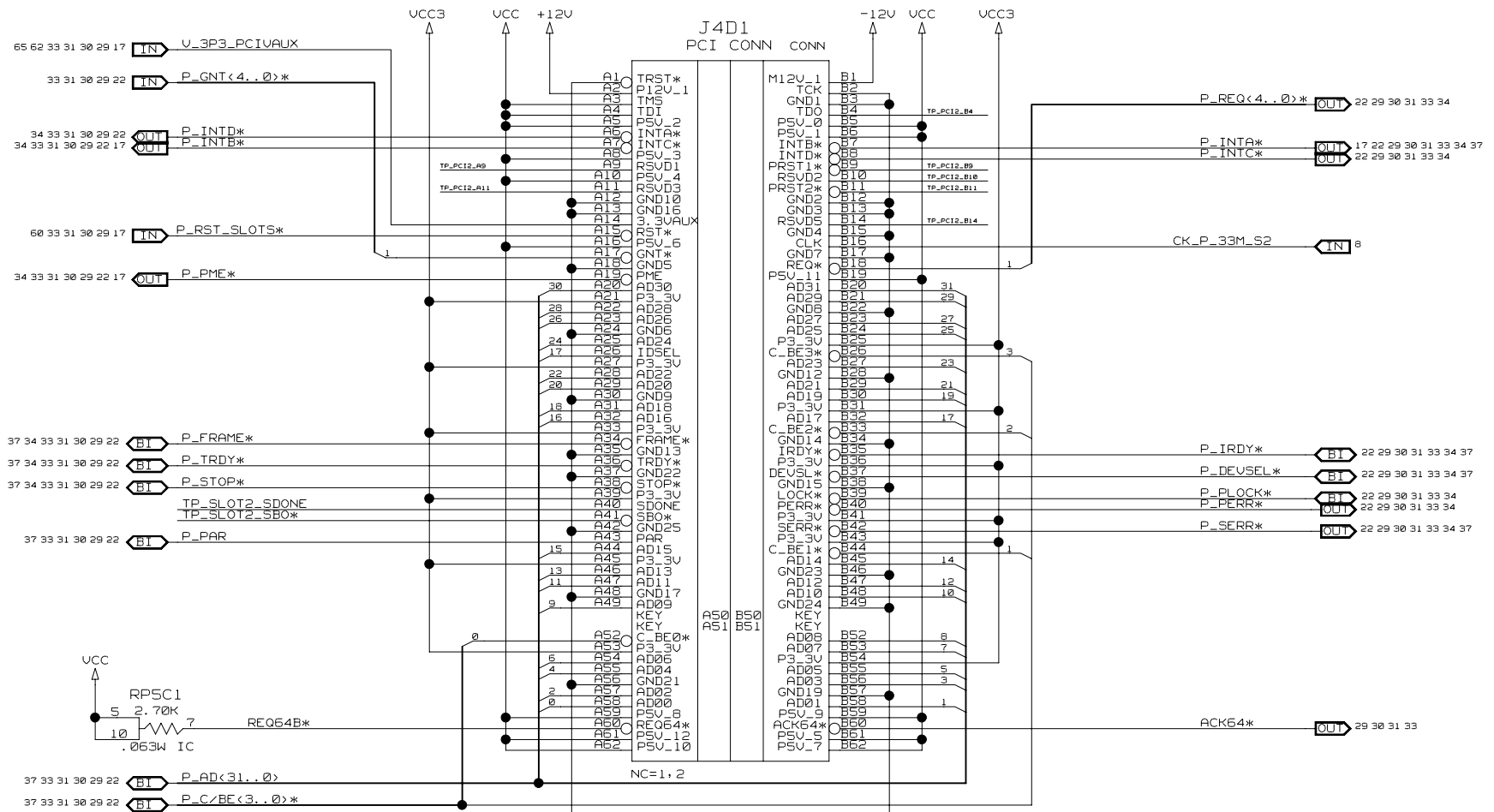
J4C1
PCI CONN CONN



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: PCI SLOT 3		SHEET: 31
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 15:43:16 2000	

DRAWING

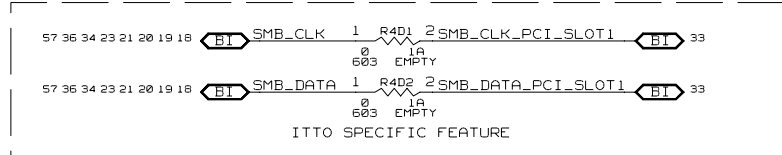
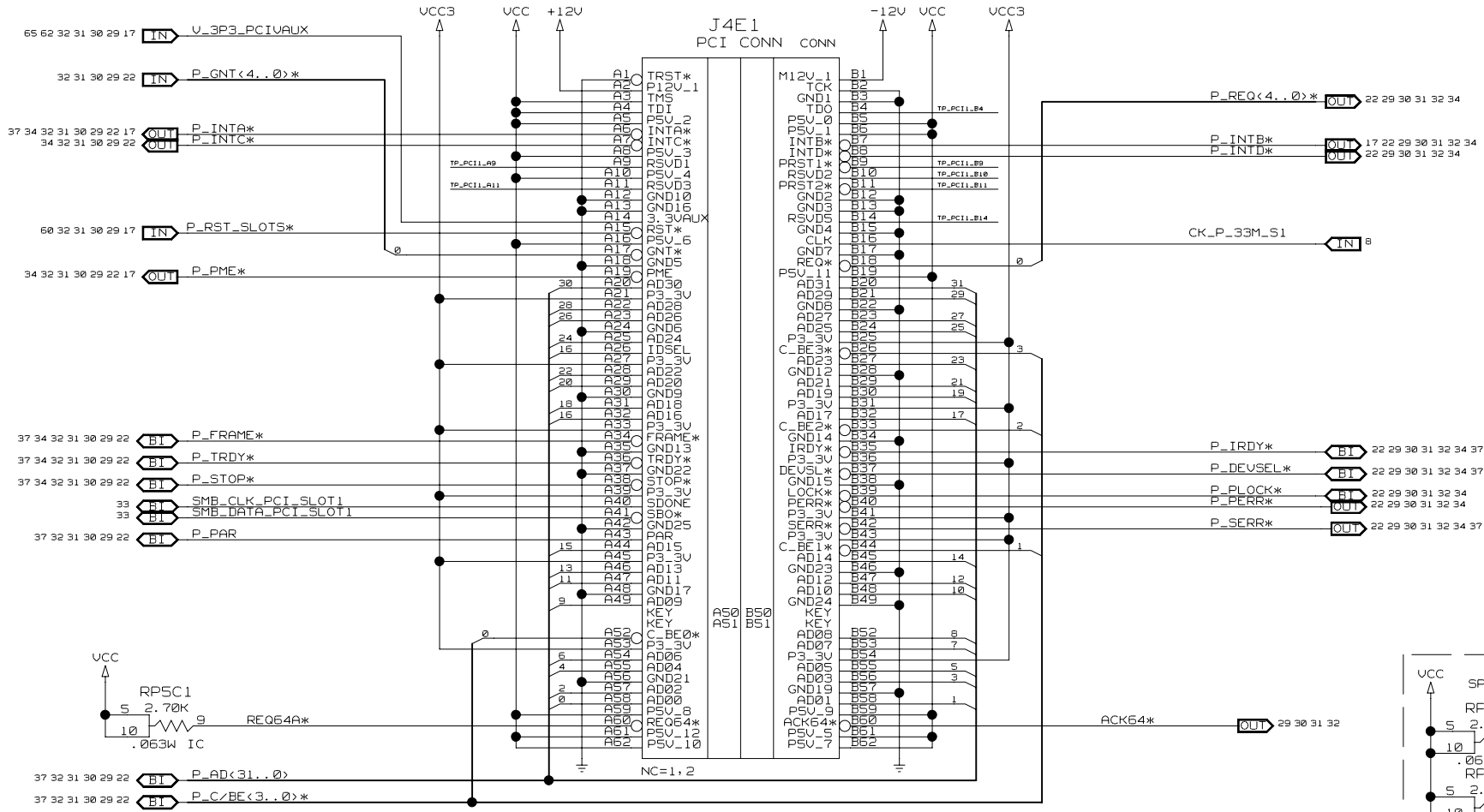
PCI SLOT 2



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: PCI SLOT 2		SHEET: 32
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 15:50:14 2000	

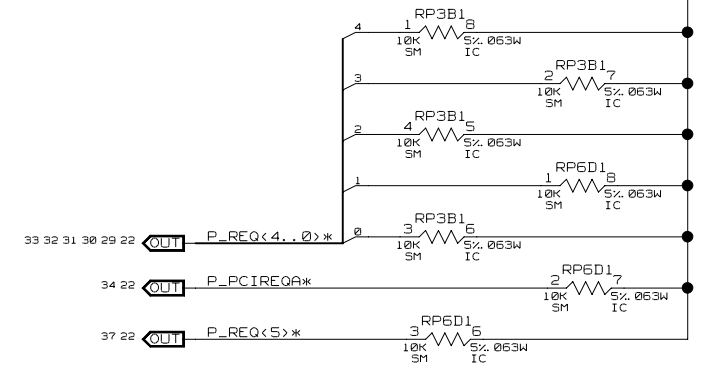
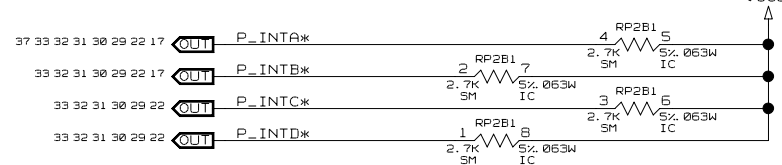
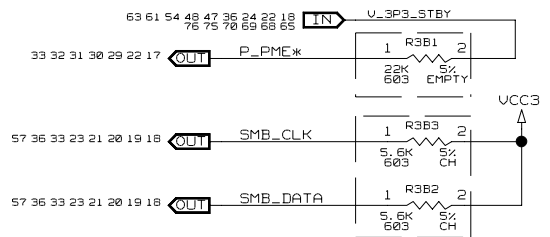
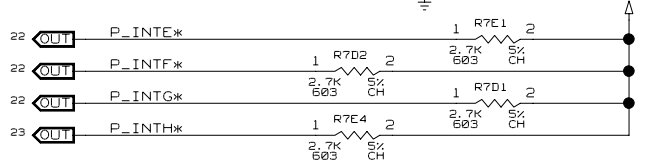
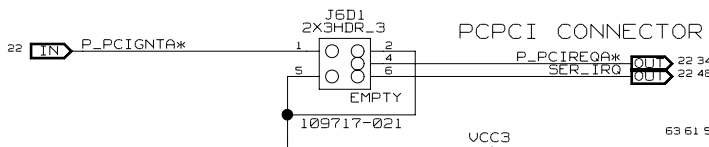
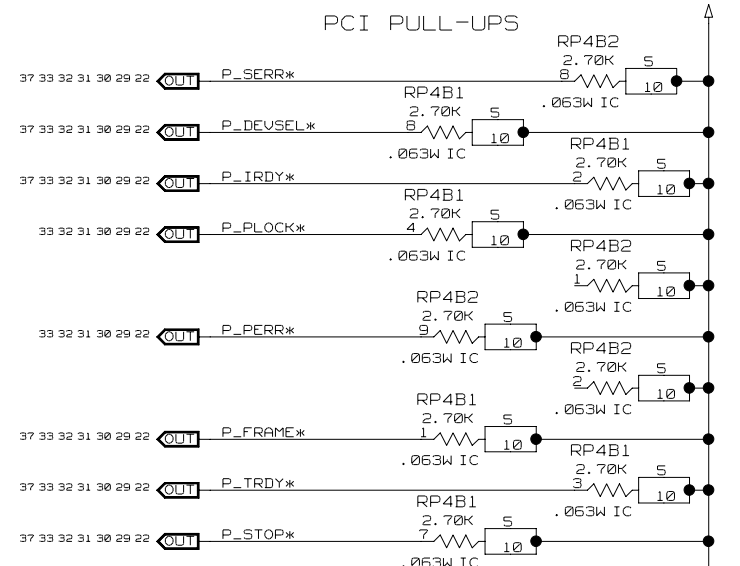
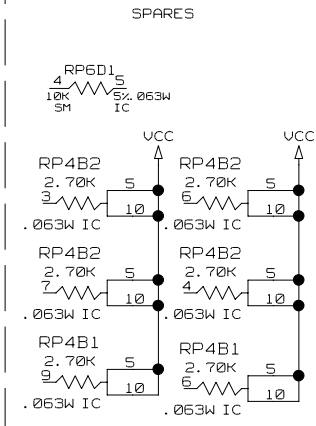
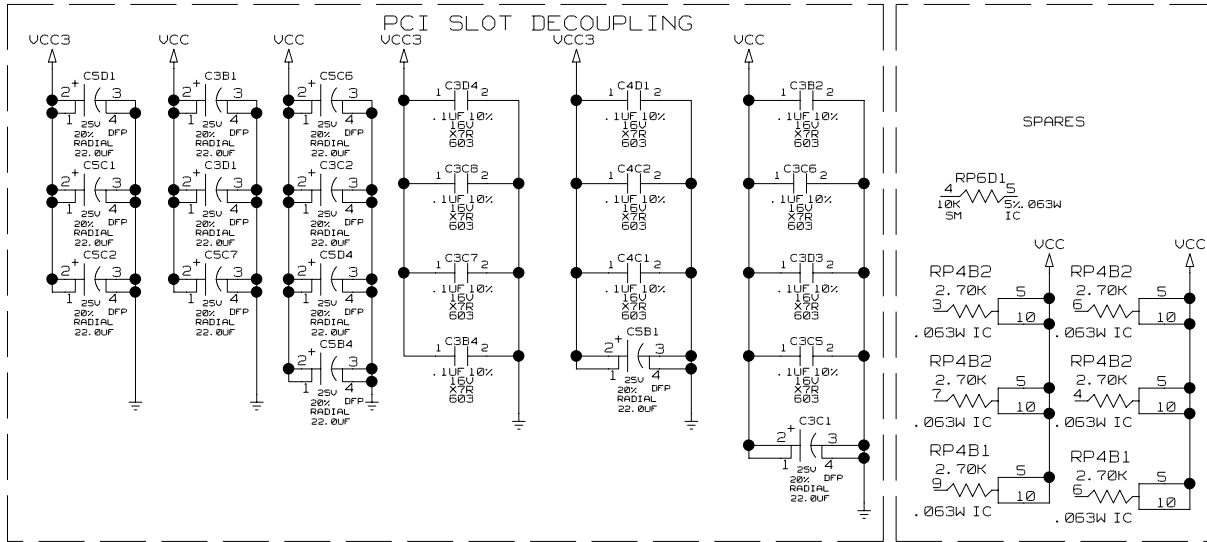
DRAWING

PCI SLOT 1



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: PCI SLOT 1		SHEET: 33
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 15:52:46 2000	

DRAWING



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: ICH PCI TERMINATION		SHEET: 34
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 15:59:04 2000	

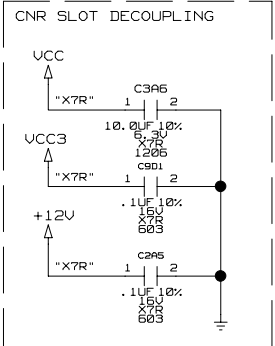
DRAWING

PAGE LEFT INTENTIONALLY BLANK

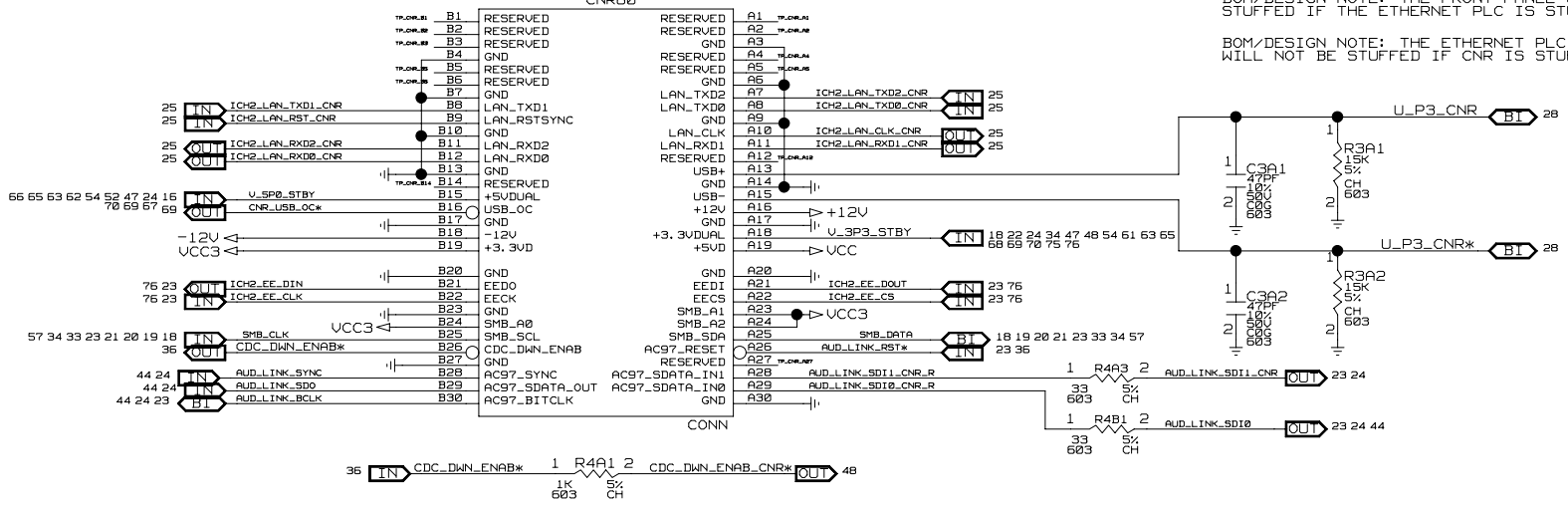
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INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: Tue Nov 07 16:00:39 2000	SHEET: 35

DRAWING

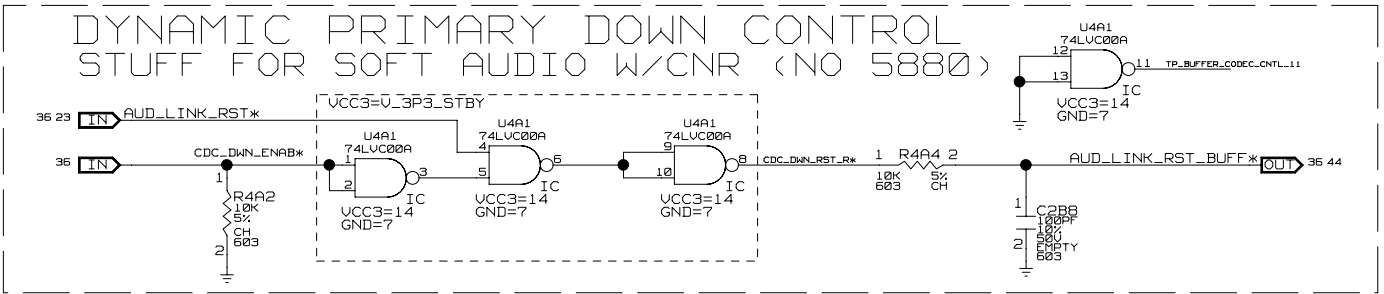
NOTE: CNR SPEC SAYS SMBUS CONTROLLER NOT POWERED BY 3V STBY... COULD BE BACKDRIVE ISSUE



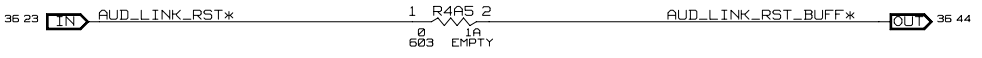
I2C ADDR: 110



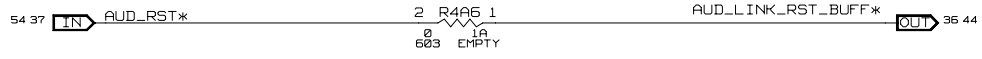
BOM/DESIGN NOTE: THE FRONT PANEL USB WILL NOT BE STUFFED IF CNR IS STUFFED
BOM/DESIGN NOTE: THE FRONT PANEL USB CAN BE STUFFED IF THE ETHERNET PLC IS STUFFED
BOM/DESIGN NOTE: THE ETHERNET PLC WILL NOT BE STUFFED IF CNR IS STUFFED



STUFF FOR SOFT AUDIO <NO CNR, NO 5880>

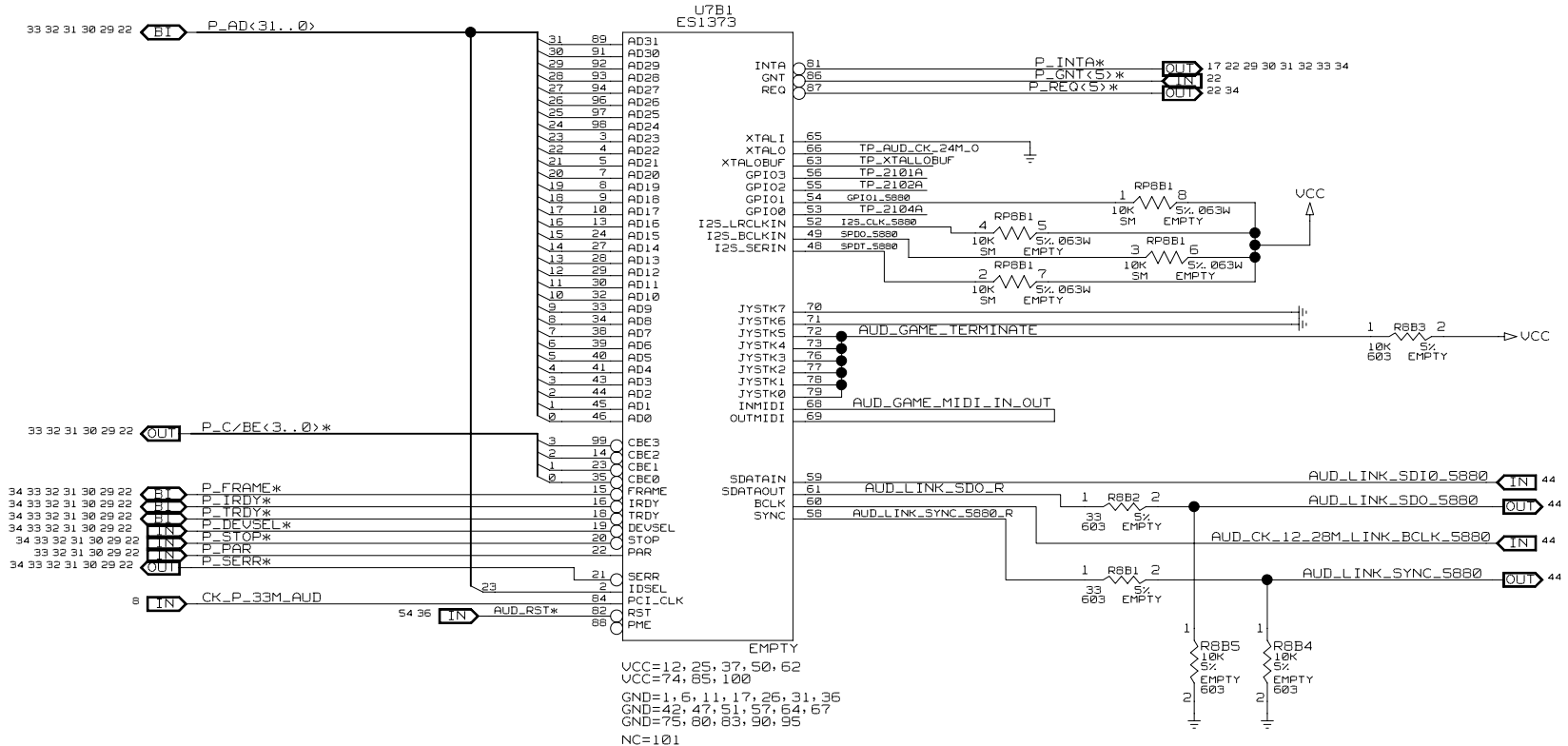


STUFF FOR 5880 <NO SOFT AUDIO>

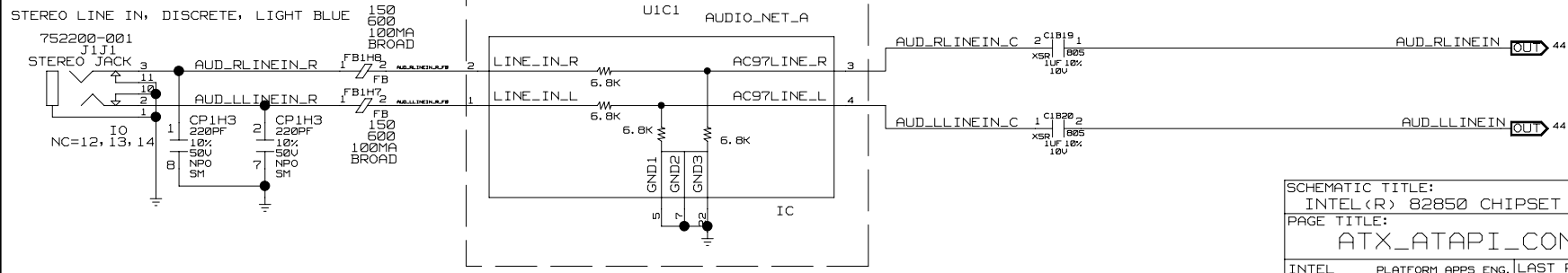
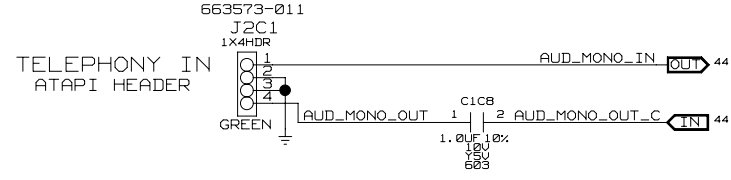
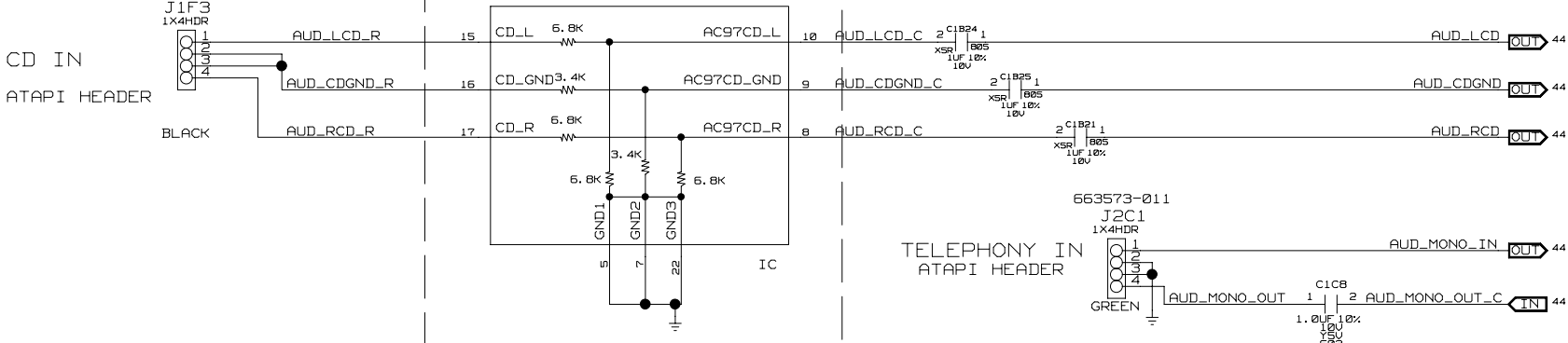
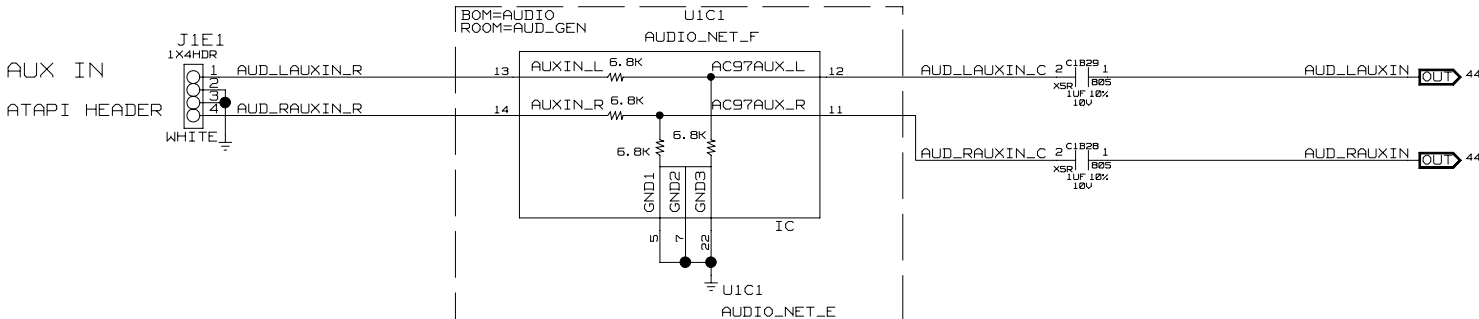
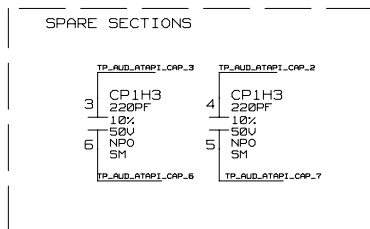
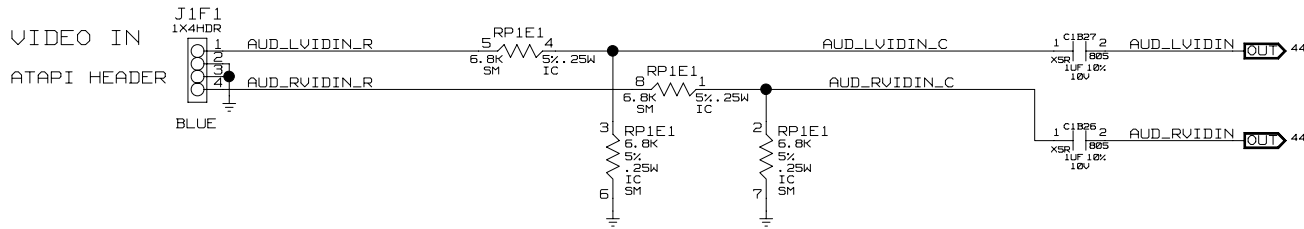


SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: CNR & DYNAMIC PRIMARY DOWN CONTROL		SHEET: 36
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 16:03:07 2000	

DRAWING



SCHEMATIC TITLE:		INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE:		1373_5V_CONTROLLER	
INTEL PLATFORM APPS ENG.		LAST REVISED:	
1900 PRAIRIE CITY ROAD		Tue Nov 07 16:05:46 2000	
FOLSOM, CALIFORNIA 95630		SHEET:	
DRAWING		37	



SCHEMATIC TITLE:
INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD

PAGE TITLE:
ATX_ATAPI_CONNECTORS

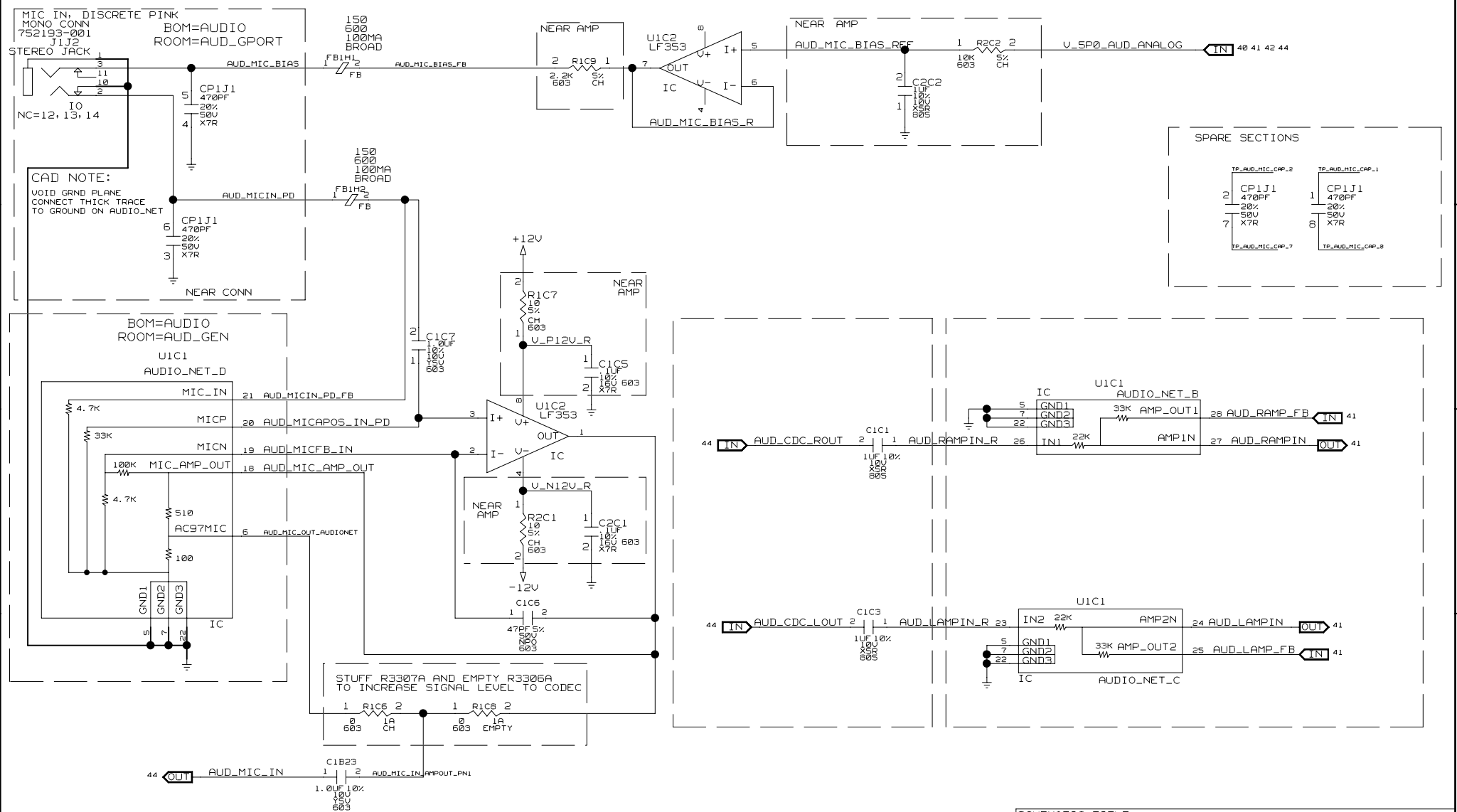
REV: 3.0

INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD, FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Nov 07 16:07:15 2000

SHEET: 38

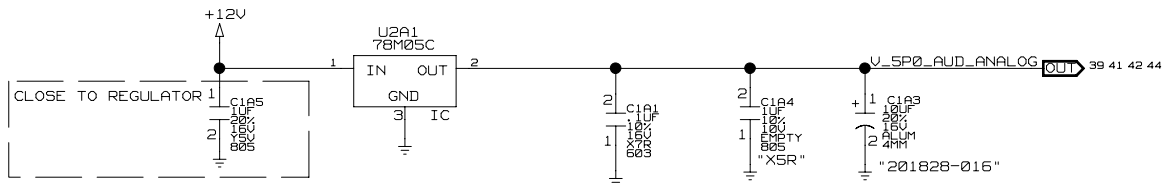
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SCHEMATIC TITLE: INTEL (R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: ATX_MIC_PREAMP&OUTAMP_FB		SHEET: 39
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 16:08:43 2000	

DRAWING

NOTE:
REGULATOR THERMAL TAB SHOULD BE SOLDERED
TO A COPPER PAD THAT IS LARGE ENOUGH
TO ALLOW 5 TO 10 GROUND VIAS AROUND
THE COMPONENT FOR COOLING

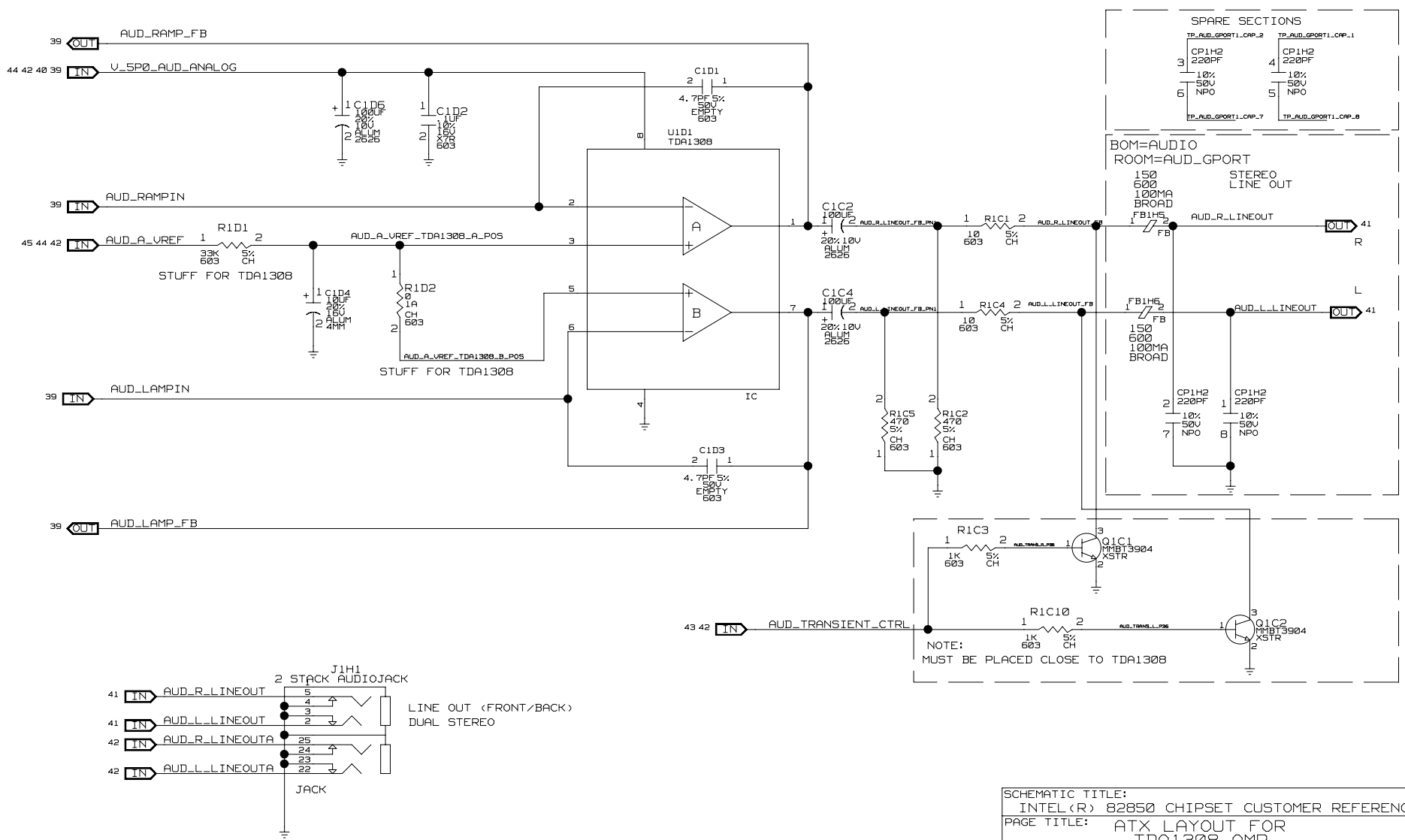


NOTE:
LAYOUT SHOULD GO FROM PIN 2 TO
CAPS AND THEN THROUGH SEVERAL
VIAS TO V_5P0_AUD_ANALOG

SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: AUDIO_VREG		SHEET: 40
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 16:09:58 2000	

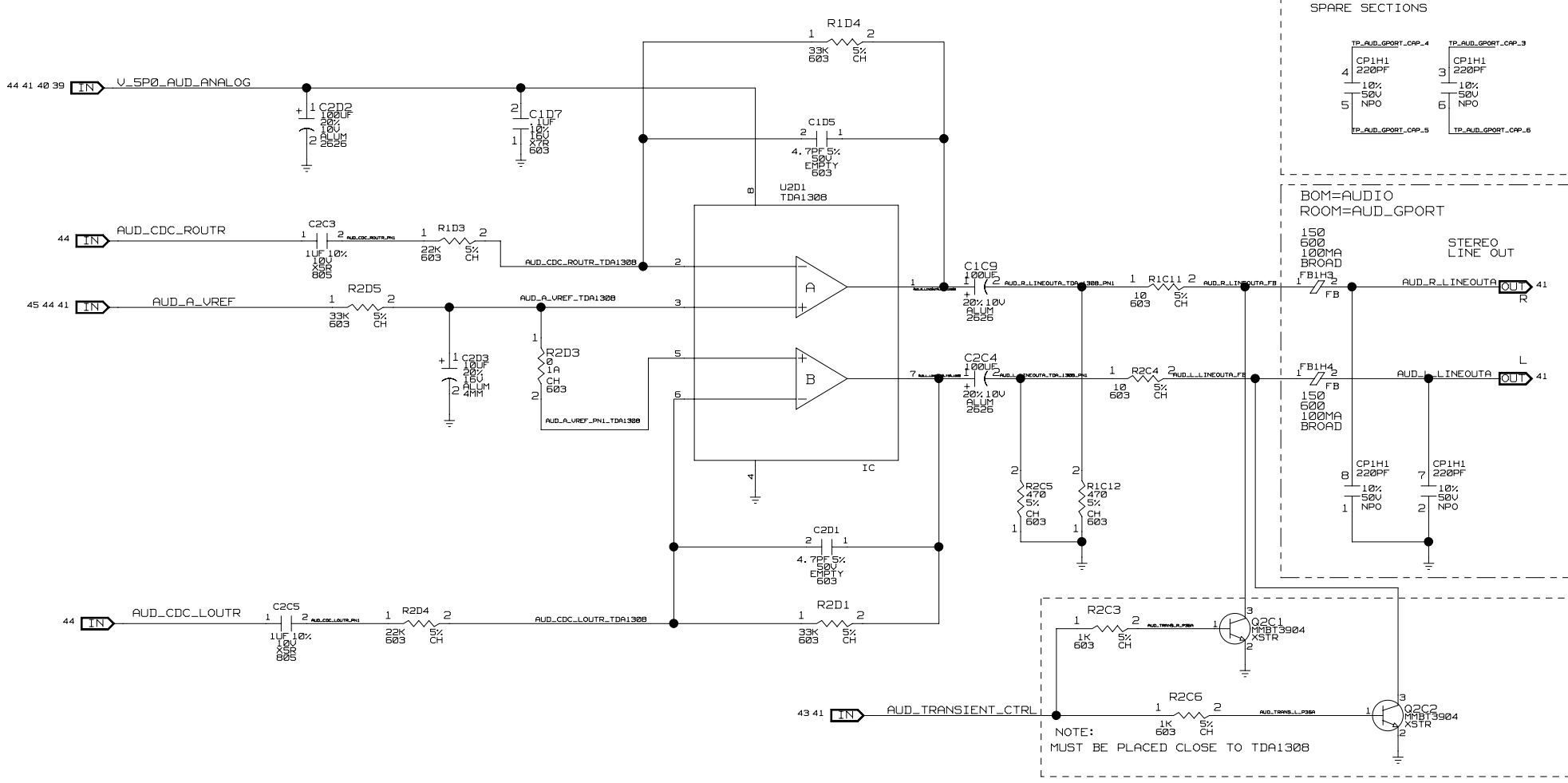
DRAWING

UNABLE TO CHANGE J3990A TO SINGLE STEREO-OUT JACK (752201-001, LIME)
 FOR 2-CHANNEL; AUDIO (CS4297 OR CS4299 CODEC) BECAUSE LAND PATTERNS ARE DIFFERENT



SCHEMATIC TITLE:		INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD
PAGE TITLE:		ATX LAYOUT FOR TDA1308_AMP
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		REV: 3.0
DRAWING		LAST REVISED: Tue Nov 07 16:11:00 2000 SHEET: 41

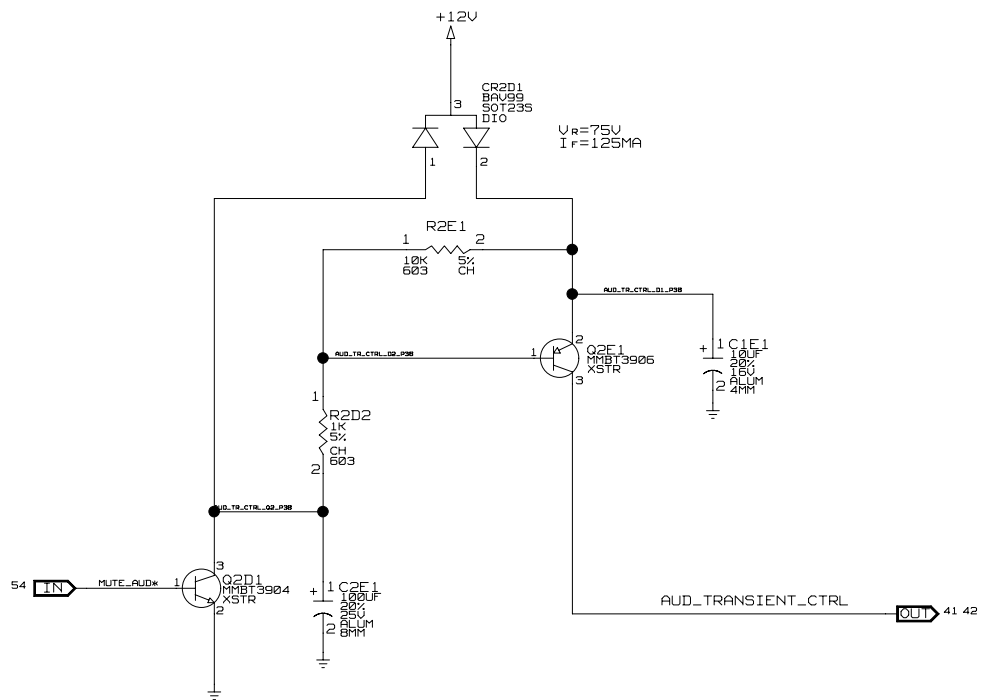
BOM NOTE: FOR 2-CHANNEL OPTION (CS4297 OR CS4299), THIS BECOMES EMPTY



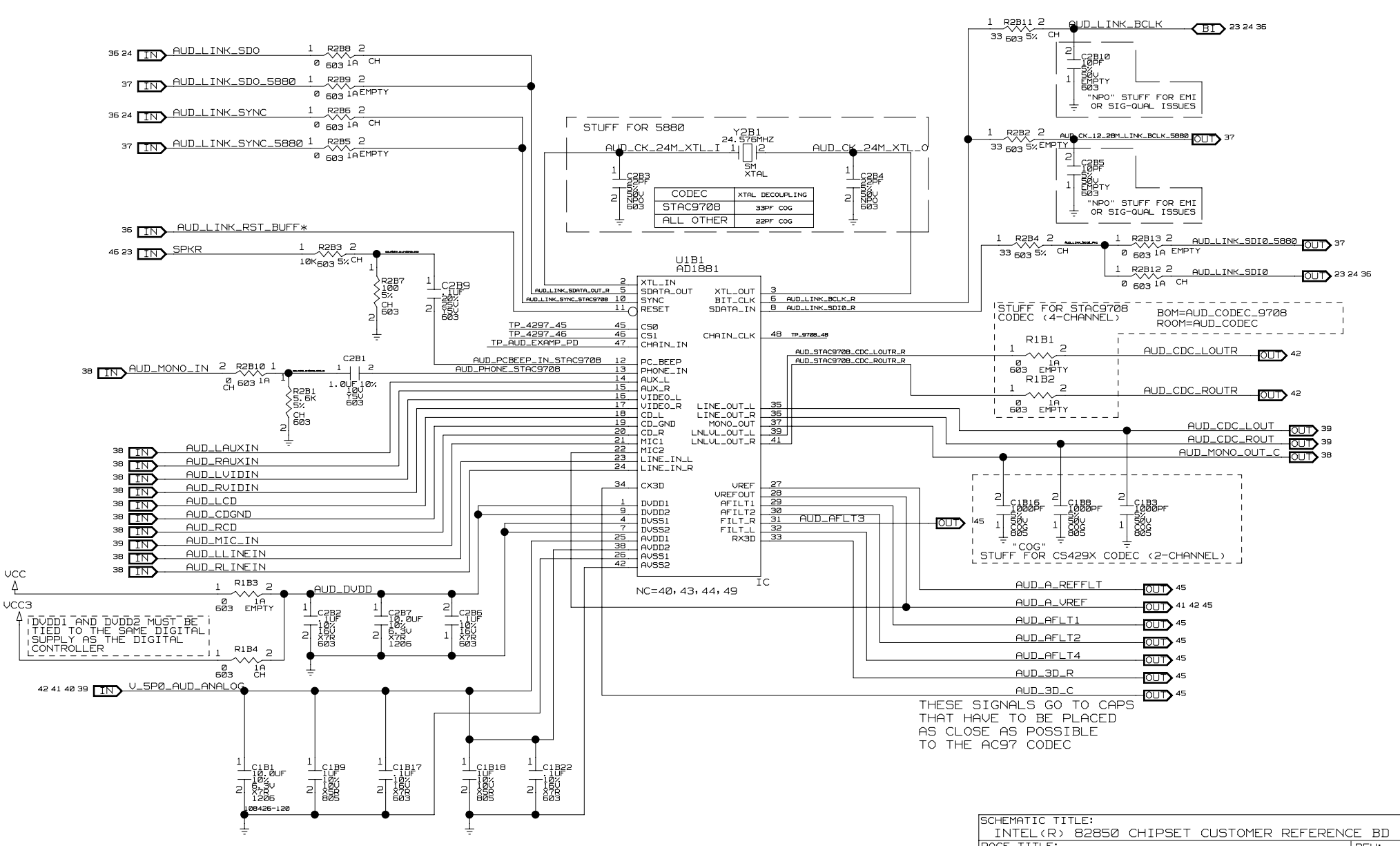
NOTE:
MUST BE PLACED CLOSE TO TDA1308

SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: TDA1308_AMP		SHEET: 42
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 16:13:43 2000	

DRAWING



SCHEMATIC TITLE:		INTEL (R) 82850 CHIPSET CUSTOMER REFERENCE BD
PAGE TITLE:		TRANSIENT CONTROL
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED:	Tue Nov 07 16:14:51 2000
DRAWING	REV:	3.0
	SHEET:	43



SCHEMATIC TITLE:		INTEL (R) 82850 CHIPSET CUSTOMER REFERENCE BD
PAGE TITLE:		ADI1881_CODEC
REV:		3.0
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED:	Tue Nov 07 16:15:56 2000
DRAWING		SHEET: 44

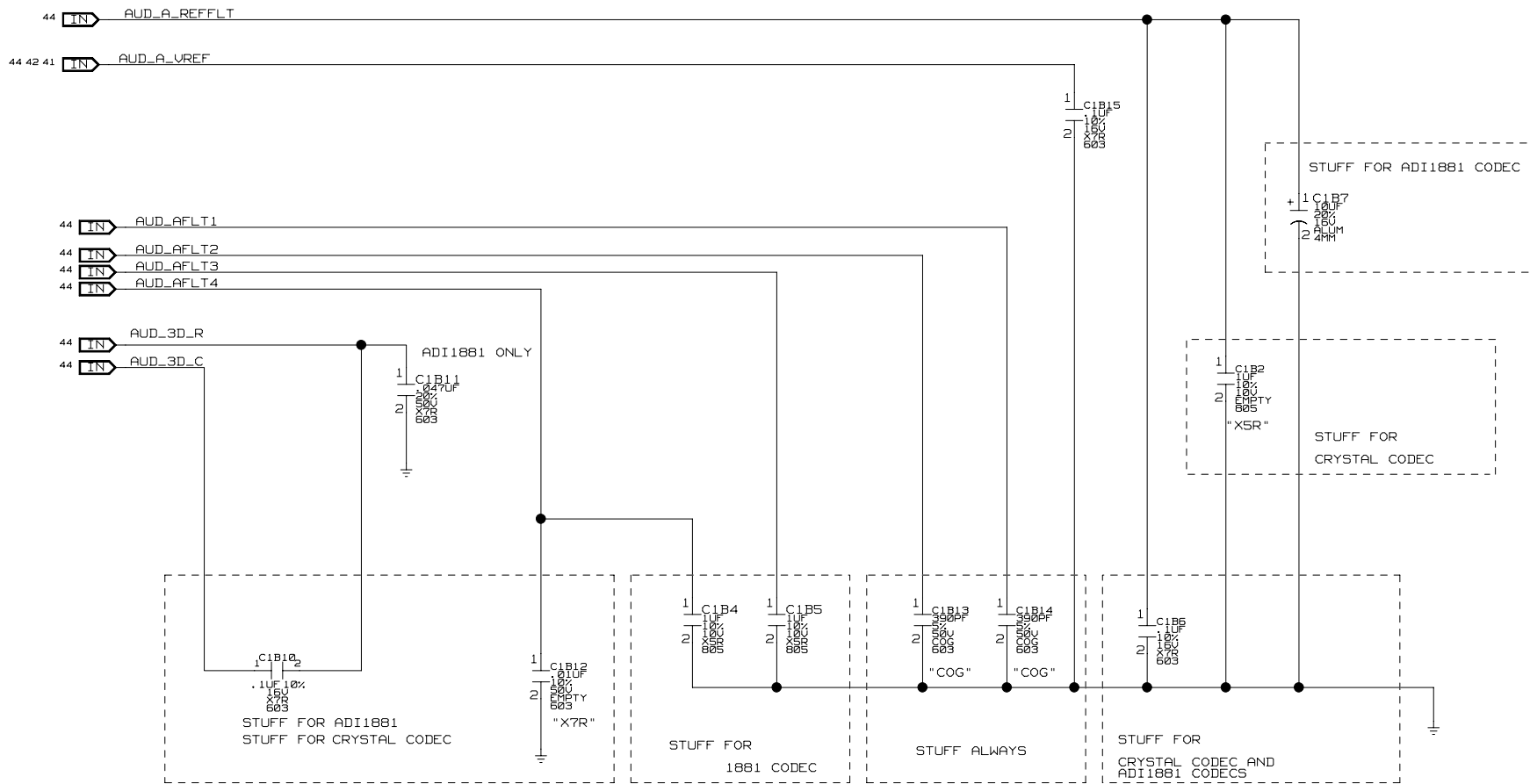
UCC3

UCC3

↑

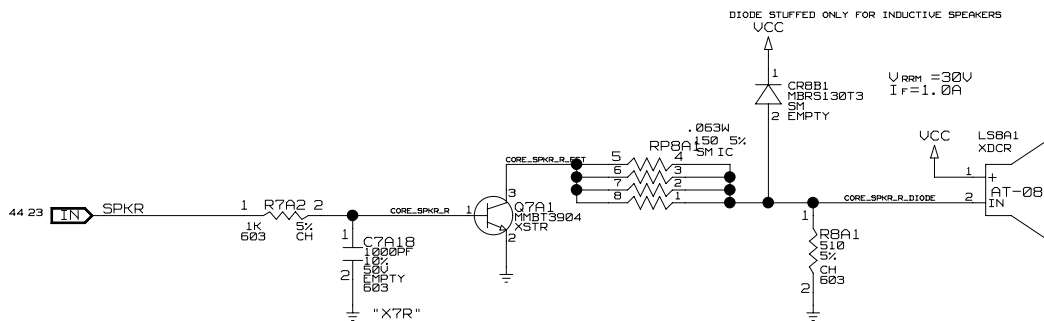
DVDD1 AND DVDD2 MUST BE TIED TO THE SAME DIGITAL SUPPLY AS THE DIGITAL CONTROLLER

KEEP CAPS AS CLOSE AS POSSIBLE TO AC97 CODEC.



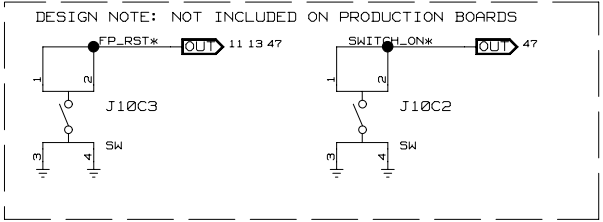
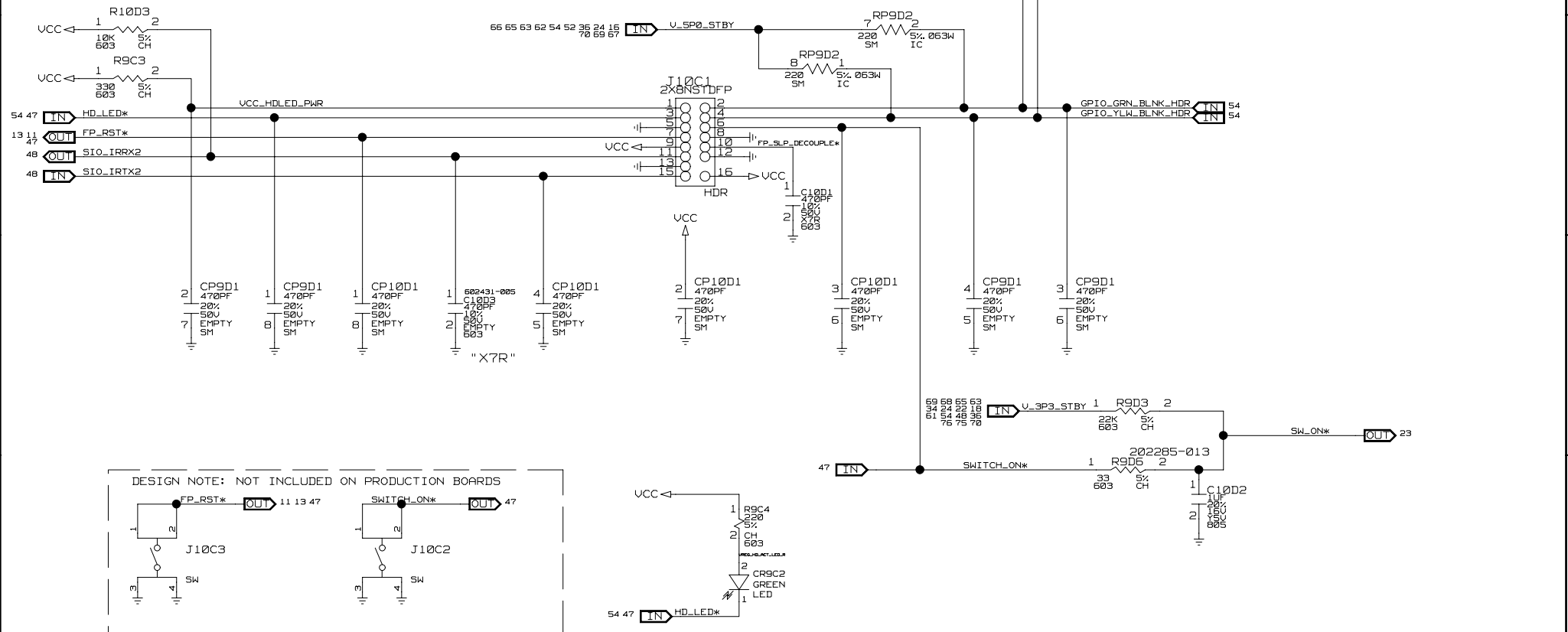
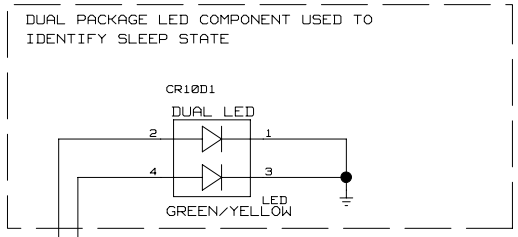
SCHEMATIC TITLE: INTEL (R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: CODEC CAPS		SHEET: 45
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 16:19:11 2000	

DRAWING



SCHEMATIC TITLE:		INTEL (R) 82850 CHIPSET CUSTOMER REFERENCE BD
PAGE TITLE:		SPEAKER
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 16:26:06 2000	REV: 3.0 SHEET: 46

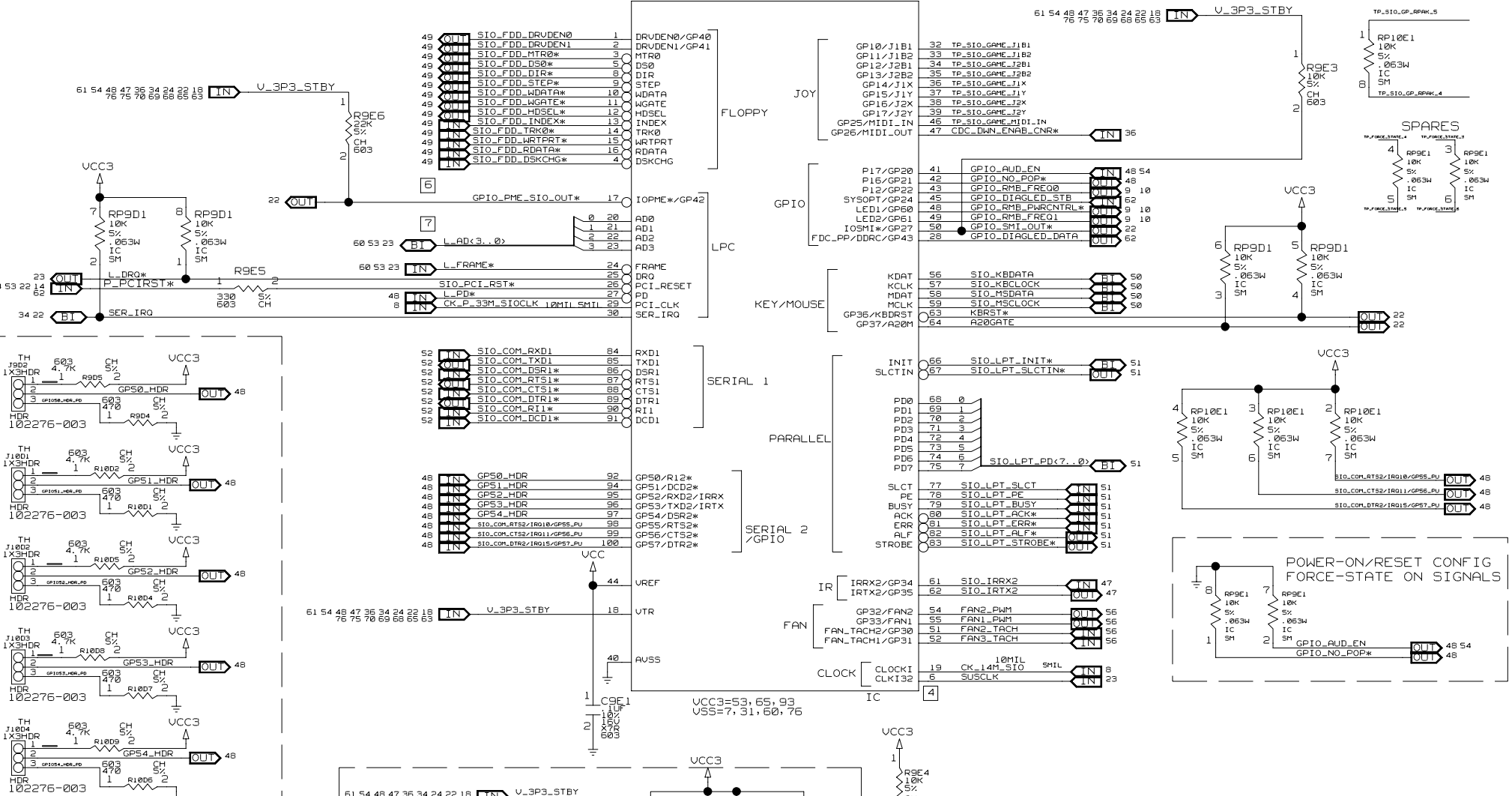
DRAWING



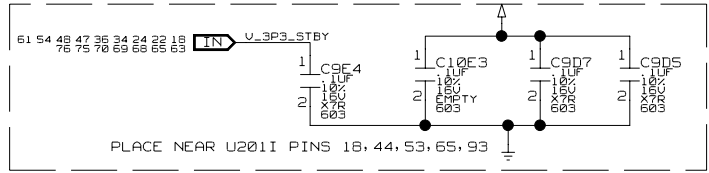
SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: STD FRONT PANEL HDR		SHEET: 47
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 16:27:29 2000	

DRAWING

U9E1
LPC47M102

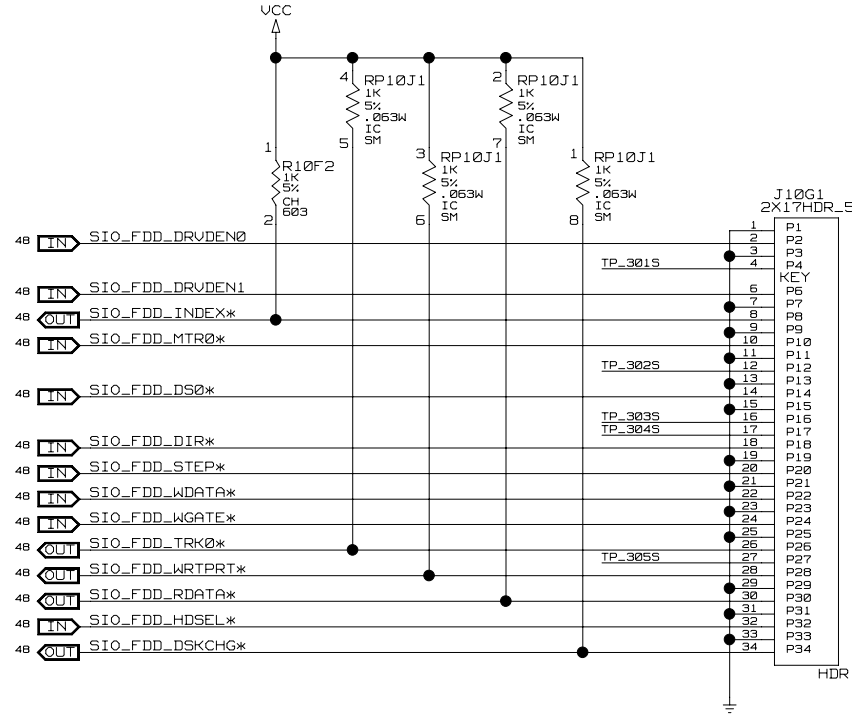


DESIGN NOTE: DEBUG/EVAL ONLY



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: SIO_LPC_47M102		SHEET: 48
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 16:37:45 2000	

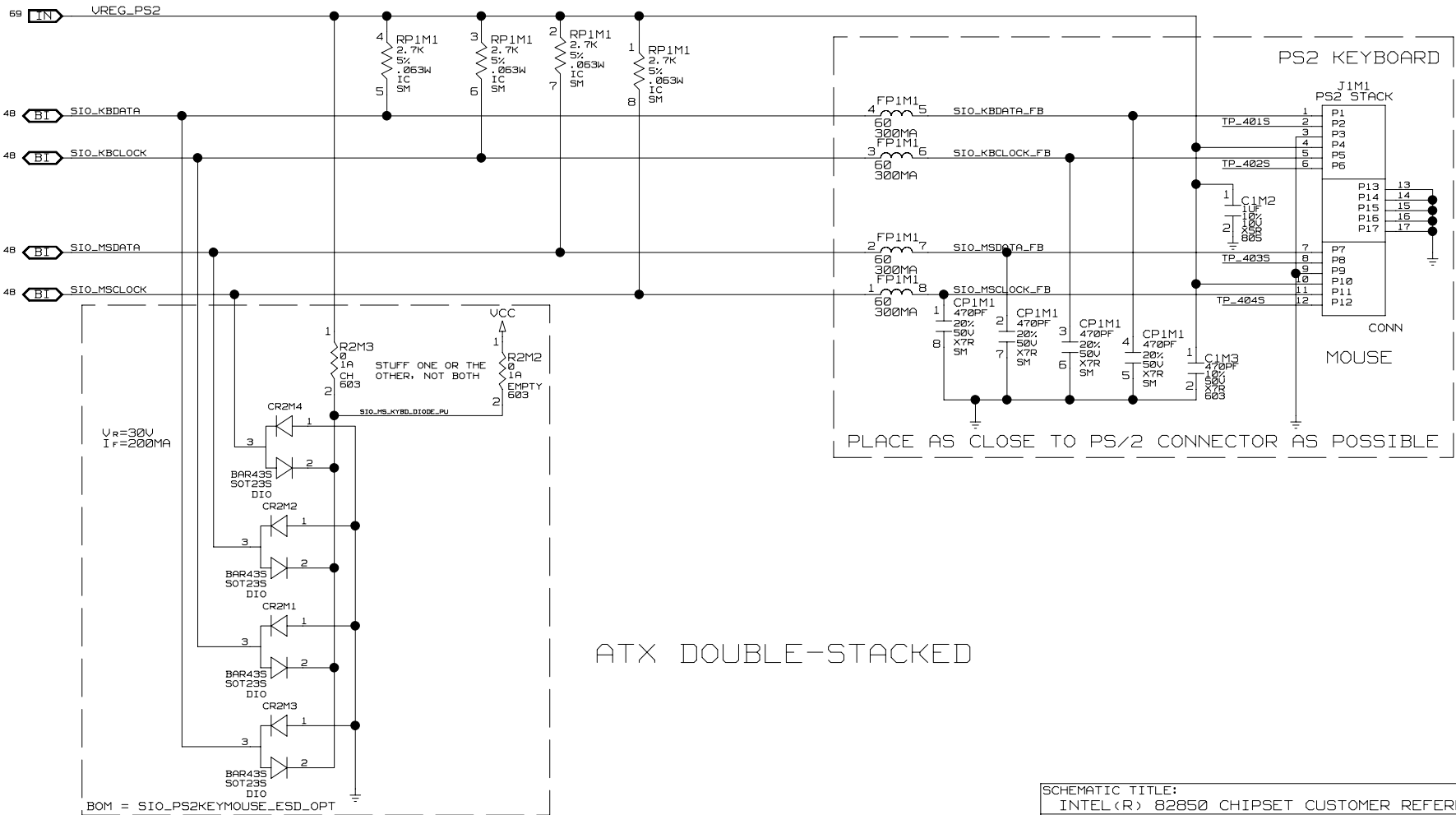
DRAWING



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: ATX_FLOPPY		SHEET: 49
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Nov 07 16:52:58 2000	

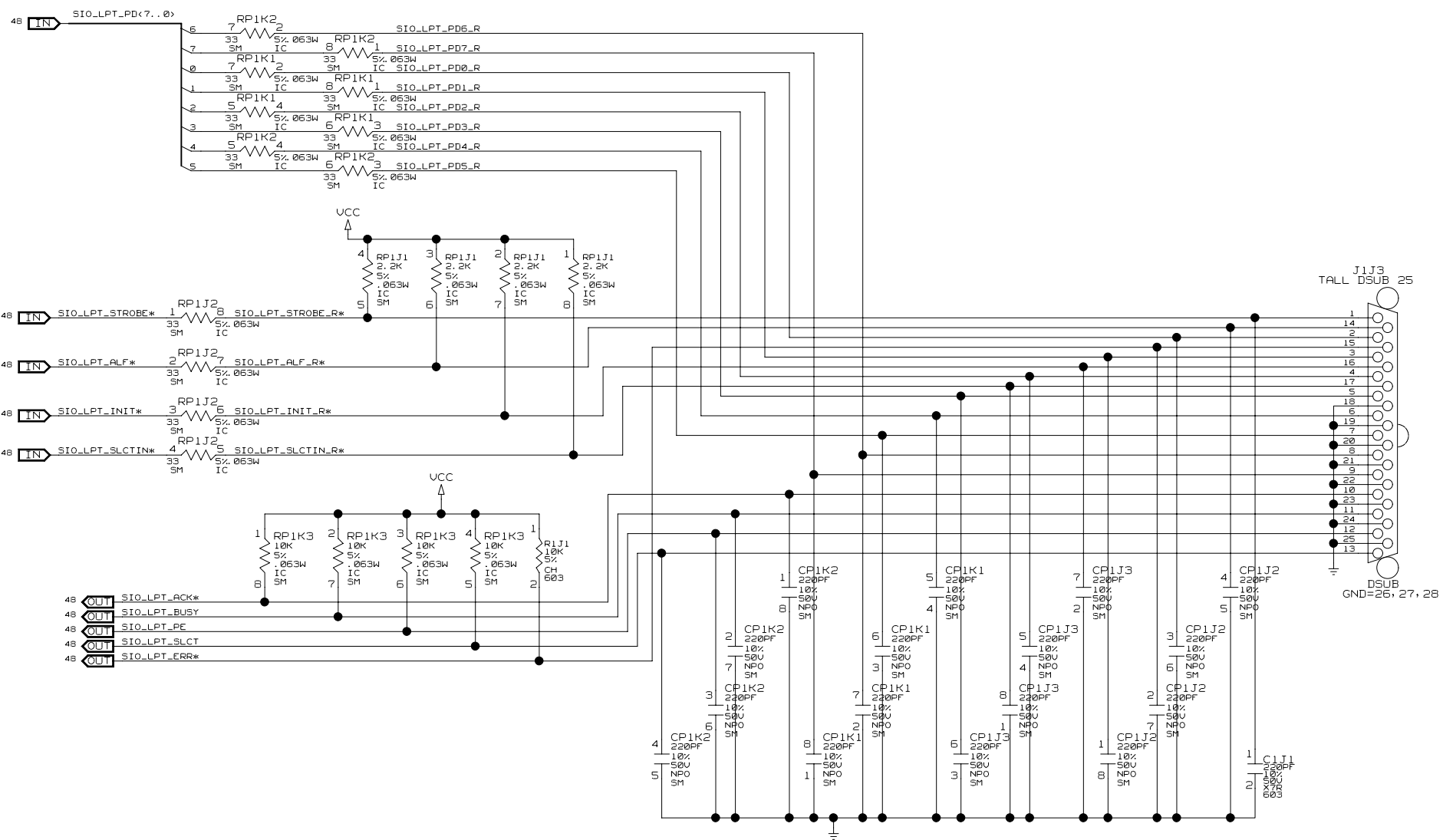
DRAWING

CONNECT TO VREG_PS2
FOR WAKE ON KB/MSE

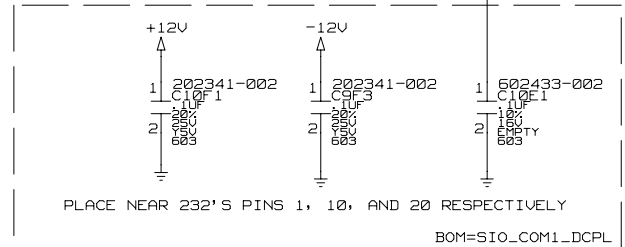
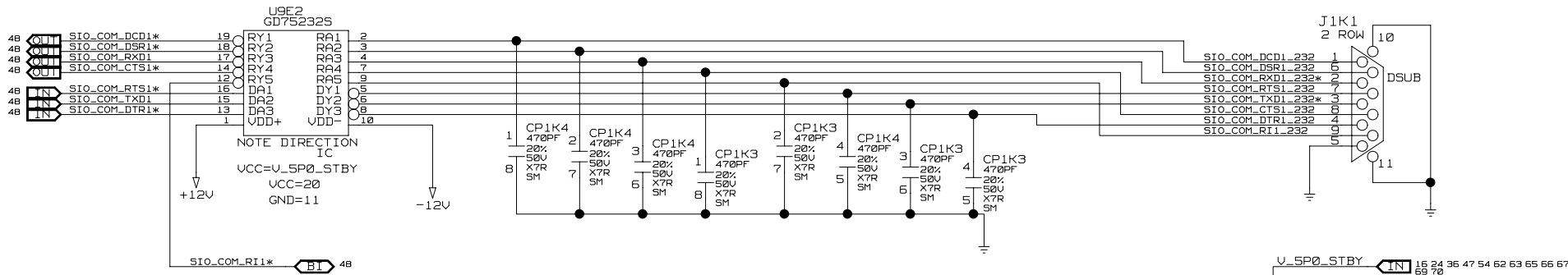


SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: PS2_KEYBOARD/MOUSE		SHEET: 50
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 08:50:43 2000	

DRAWING

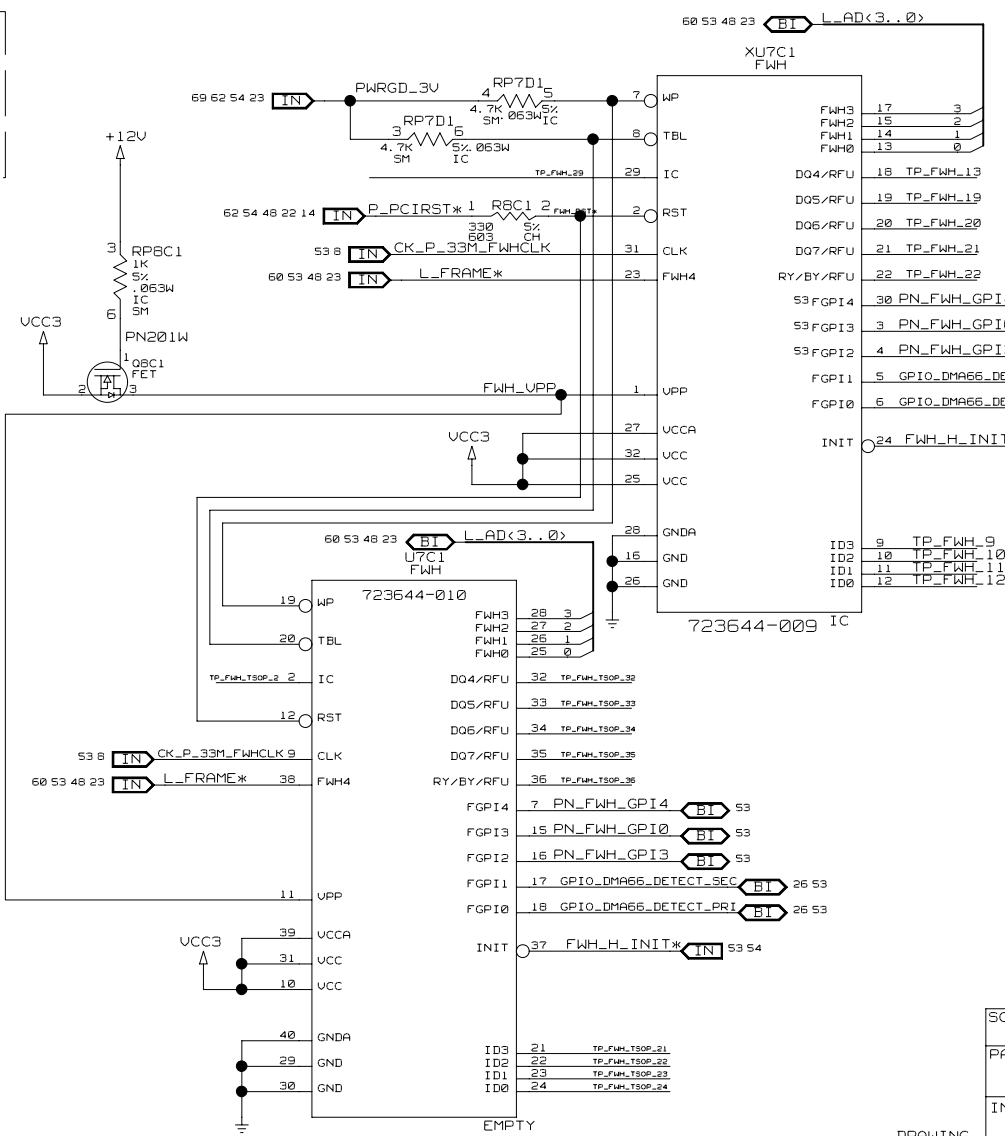
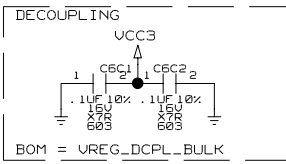
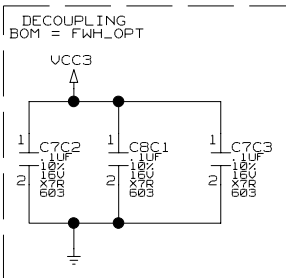
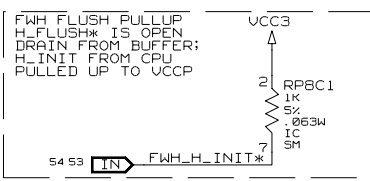


SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE: ATX_PARALLEL_PORT_ALT2	REV: 3.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 08:52:05 2000
DRAWING	SHEET: 51



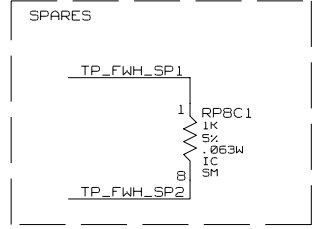
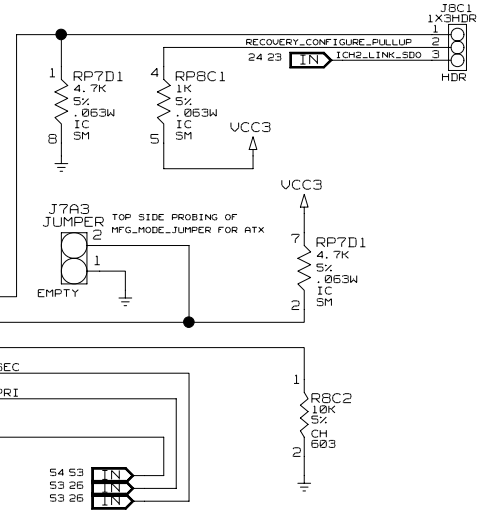
SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: COM1_PORT		SHEET: 52
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 08:54:06 2000	

DRAWING



RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY

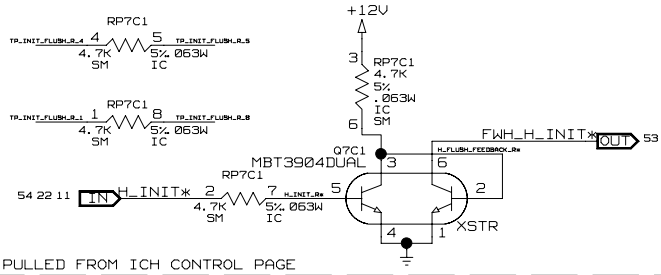
* DEFAULT JUMPER SETTING
CONFIGURE= SAFE MODE



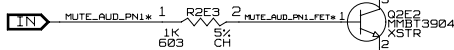
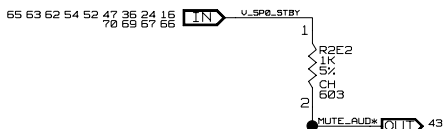
SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: FIRMWARE HUB		SHEET: 53
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 08:56:06 2000	

DRAWING

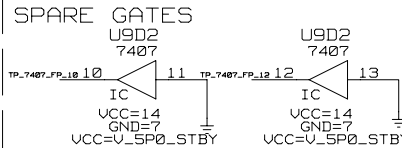
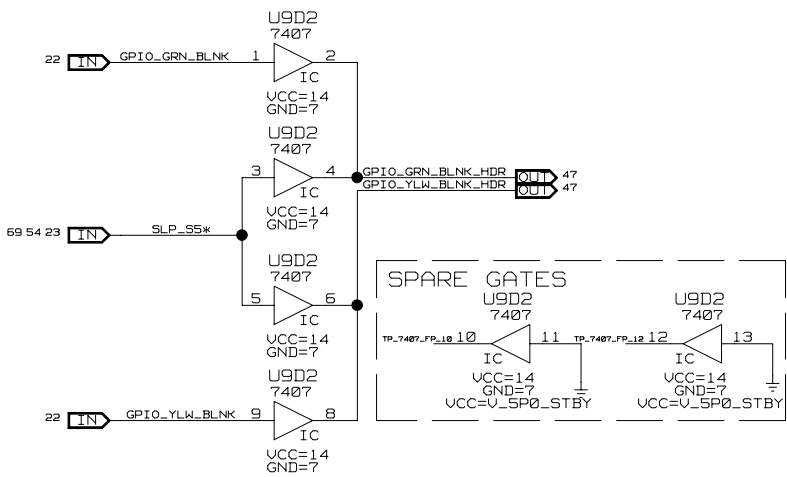
VOLTAGE MODIFIER; ICH(UCCP) ISOLATE FROM FWH(UCC3)



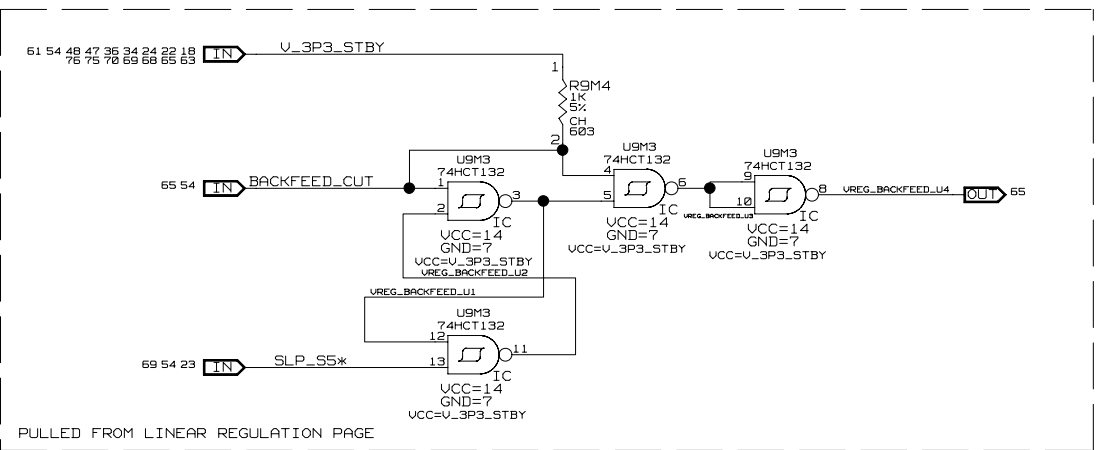
PULLED FROM ICH CONTROL PAGE



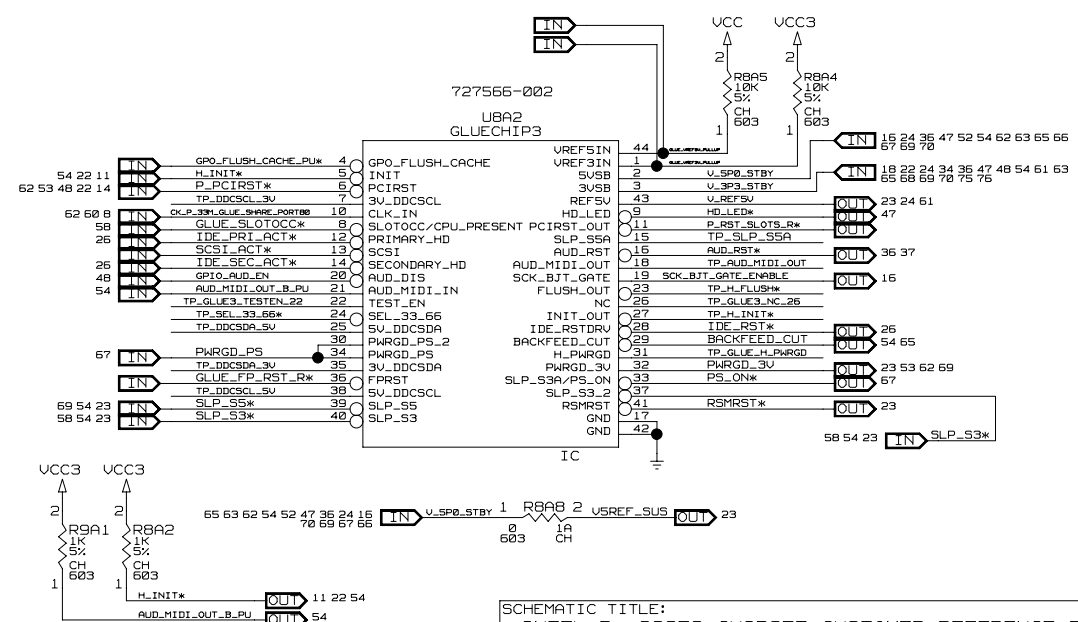
PULLED FROM AUDIO TRANSIENT CONTROL PAGE



PULLED FROM STD-FRONT-PANEL-HDR PAGE



PULLED FROM LINEAR REGULATION PAGE



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: GLUECHIP3		SHEET: 54
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 08:58:05 2000	

DRAWING

CR-55

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

PAGE LEFT INTENTIONALLY BLANK

SCHEMATIC TITLE:		INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE:		BLANK	REV: 3.0
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: Wed Nov 08 08:59:54 2000	SHEET: 55

DRAWING

8

7

6

5

4

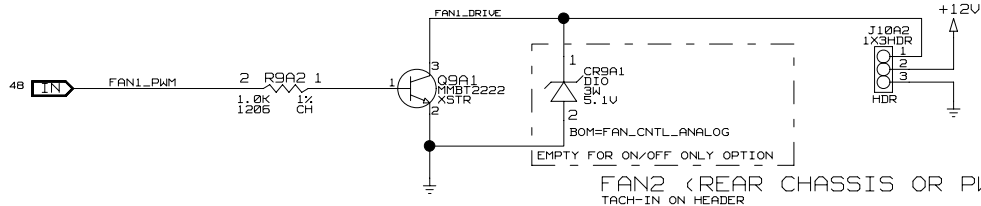
3

2

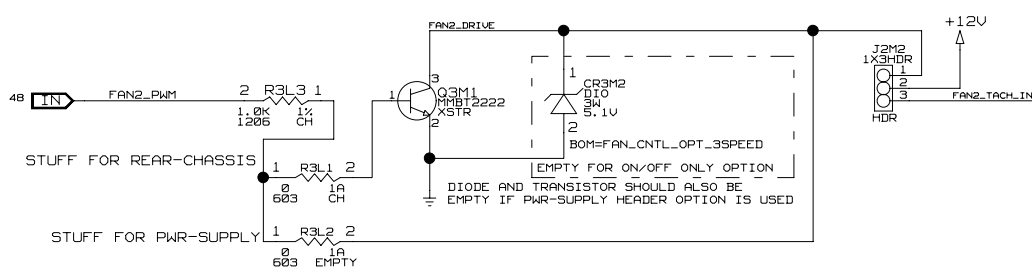
1

FAN SPEED SETTINGS
 FULL ON
 HALF ON (ZENER SET-POINT)
 FULL OFF (SYSTEM POWER-OFF)

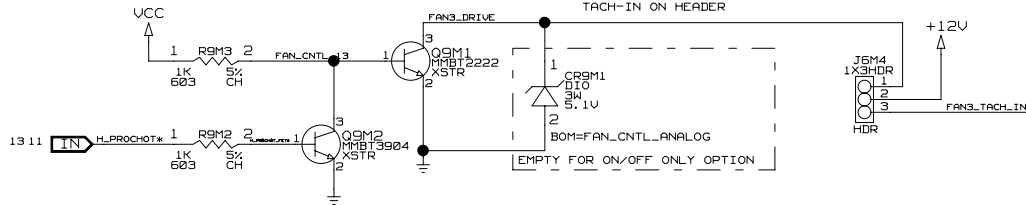
FAN1 (FRONT CHASSIS)
 NO TACH-IN FEATURE ON HEADER



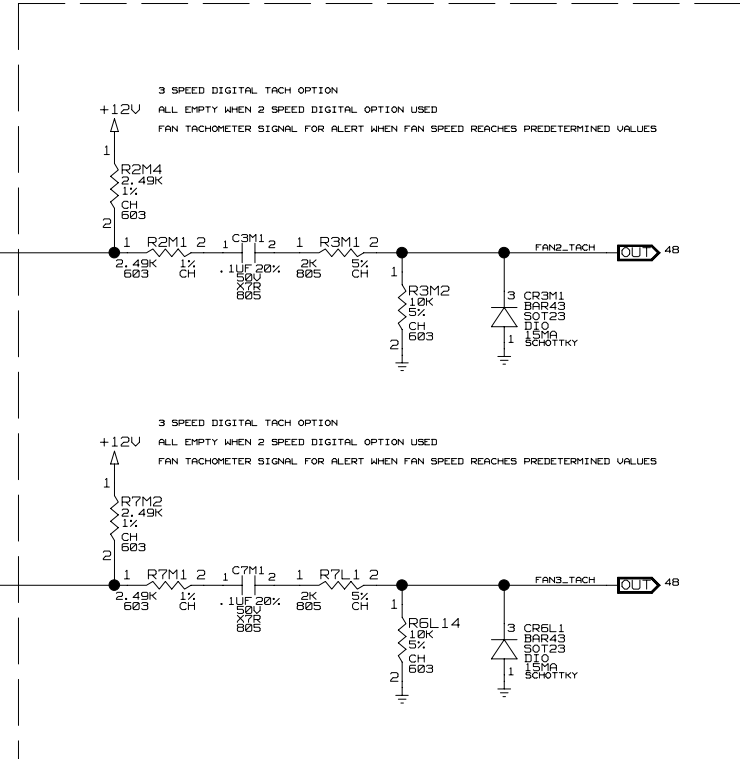
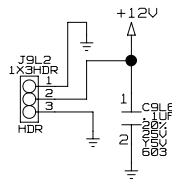
FAN2 (REAR CHASSIS OR PWR SUPPLY)
 TACH-IN ON HEADER



FAN3 (CPU)
 TACH-IN ON HEADER

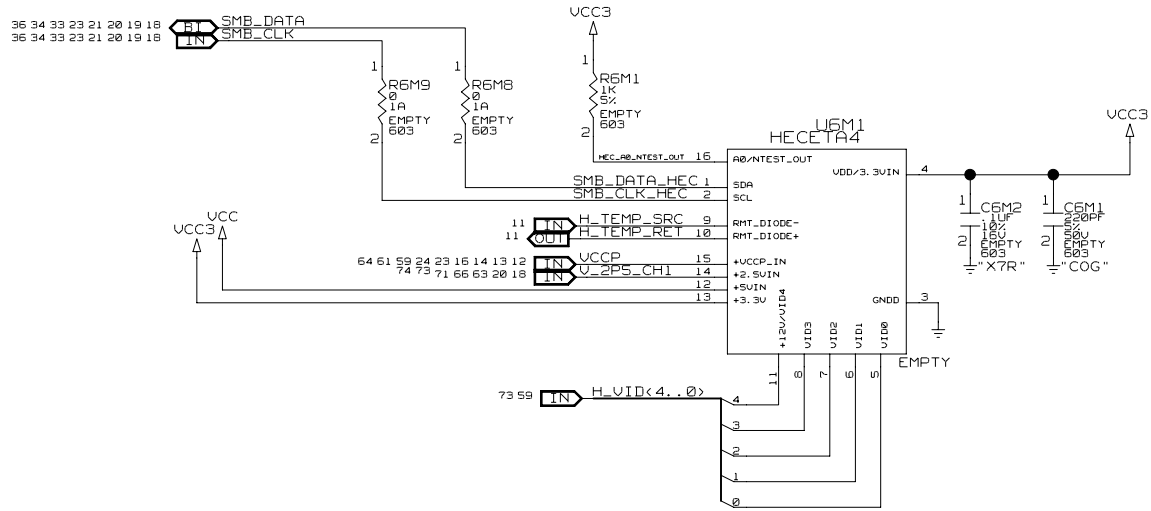


FAN 4 (RIMM COOLER)
 NON-ADJUSTABLE SPEED FAN HEADER



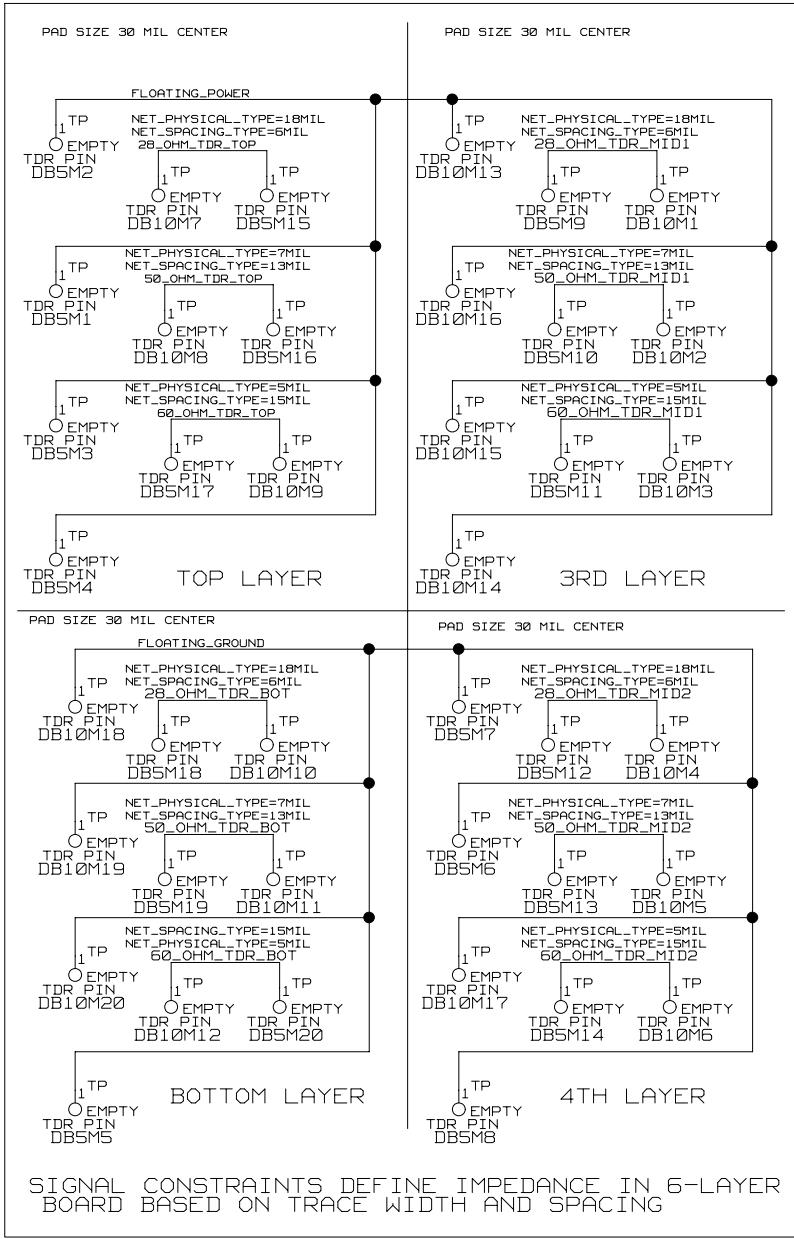
SCHEMATIC TITLE: INTEL (R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: FAN CONTROL		SHEET: 56
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:01:47 2000	

DRAWING

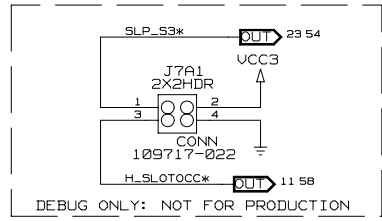
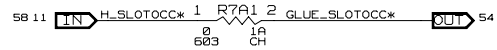
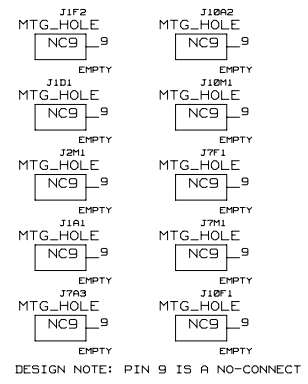


SCHEMATIC TITLE:		INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE:		HARDWARE MANAGEMENT: HECETA	
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:07:10 2000	REV: 3.0	SHEET: 57

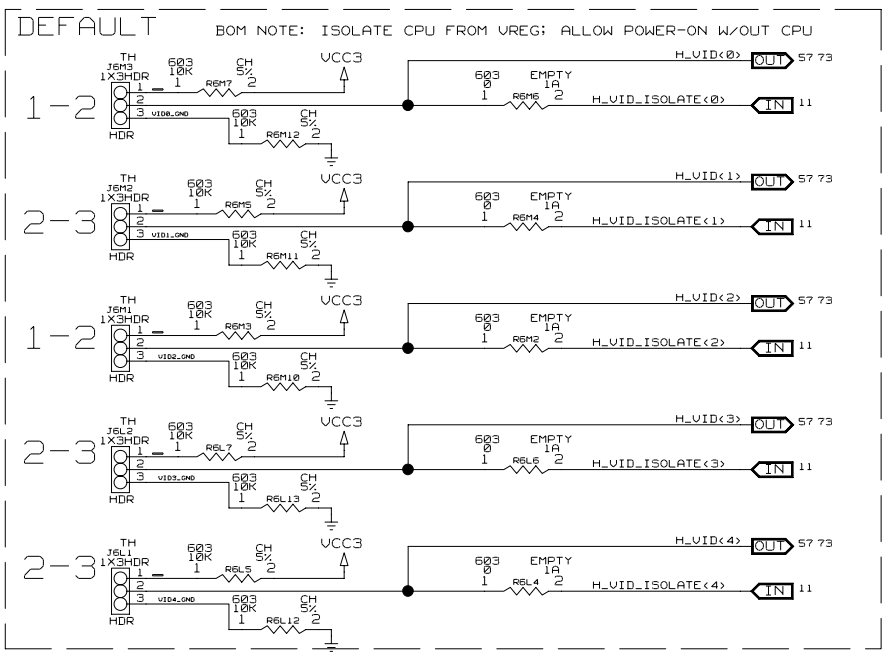
DRAWING



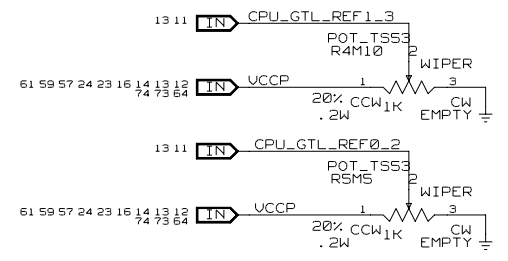
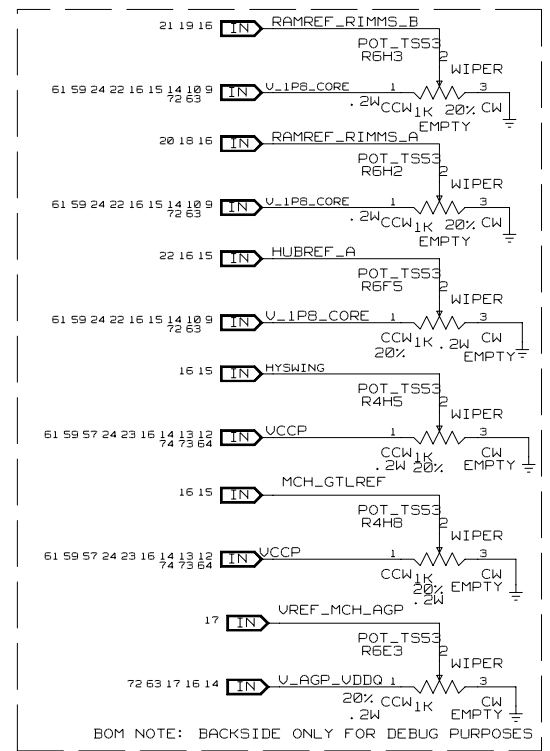
SIGNAL CONSTRAINTS DEFINE IMPEDANCE IN 6-LAYER BOARD BASED ON TRACE WIDTH AND SPACING

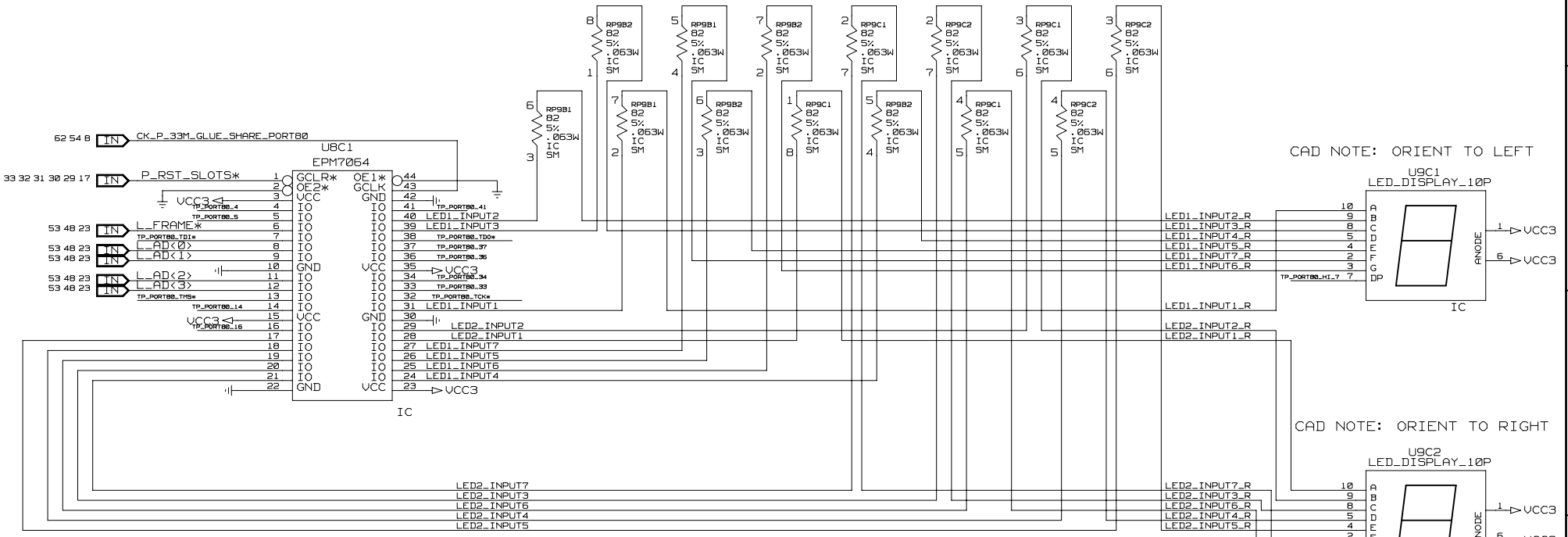
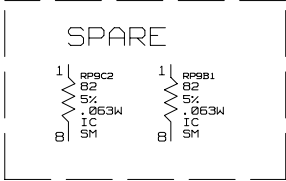


SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: TDR TEST		SHEET: 58
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:08:23 2000	

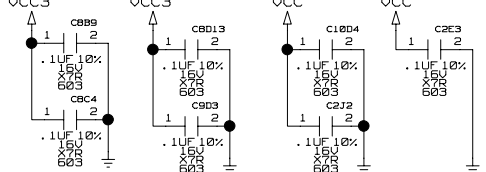


VID4	VID3	VID2	VID1	VID0	VOLTAGE
1	1	1	1	1	OFF
1	1	1	1	0	1.1
1	1	1	0	1	1.125
1	1	1	0	0	1.15
1	1	0	1	1	1.175
1	1	0	1	0	1.2
1	1	0	0	1	1.225
1	1	0	0	0	1.25
1	0	1	1	1	1.275
1	0	1	1	0	1.3
1	0	1	0	1	1.325
1	0	1	0	0	1.35
1	0	0	1	1	1.375
1	0	0	1	0	1.4
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.5
0	1	1	0	1	1.525
0	1	1	0	0	1.55
0	1	0	1	1	1.575
0	1	0	1	0	1.6
0	1	0	0	1	1.625
0	1	0	0	0	1.65
0	0	1	1	1	1.675
0	0	1	1	0	1.7
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.8
0	0	0	0	1	1.825
0	0	0	0	0	1.85





PLACEMENT INSTRUCTIONS: 1 PER 2 RPACKS AND 1 BETWEEN 7SEG LED'S

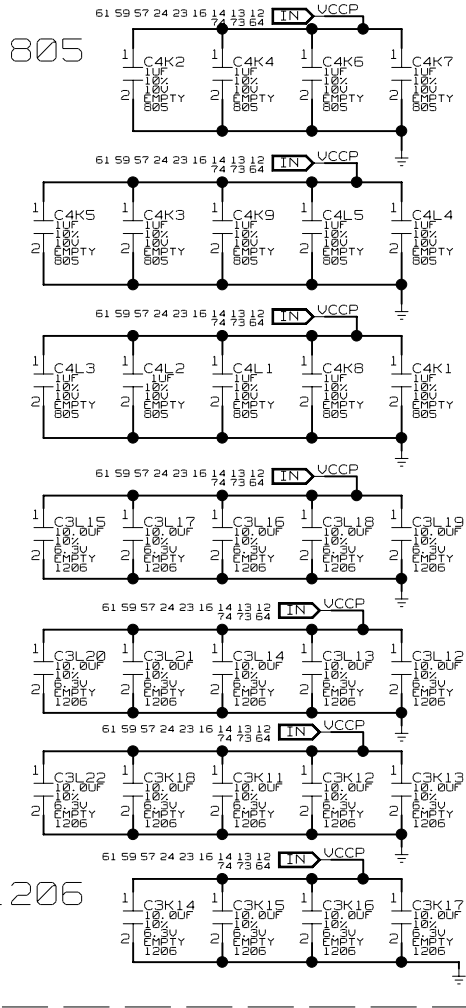


SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: LPC PORT80 DECODER		SHEET: 60
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:10:47 2000	

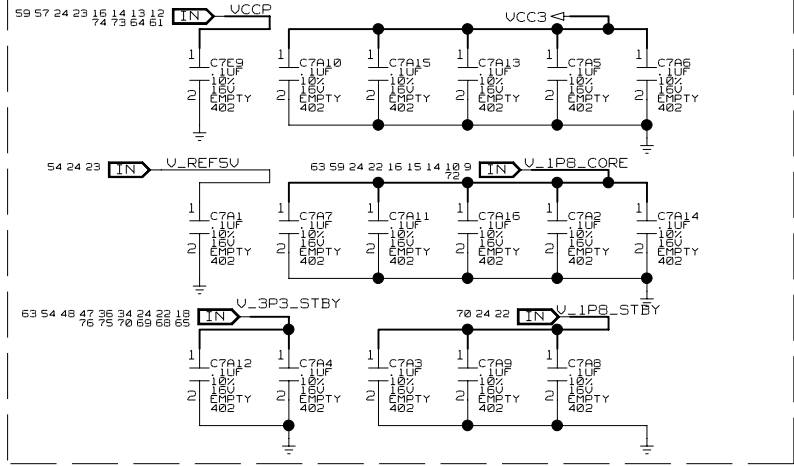
DRAWING

BACK SIDE CPU DECOUPLING; VALIDATION VEHICLE ONLY

805



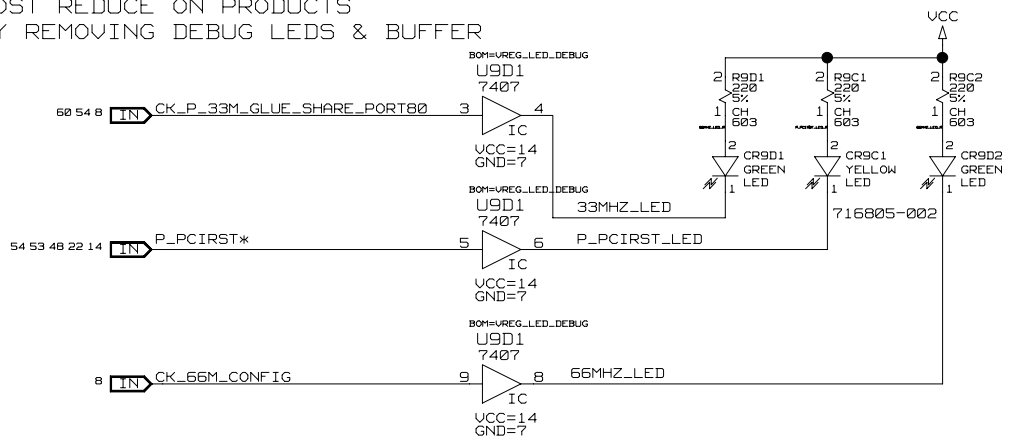
BACK SIDE CHIPSET (ICH) DECOUPLING; VALIDATION VEHICLE ONLY



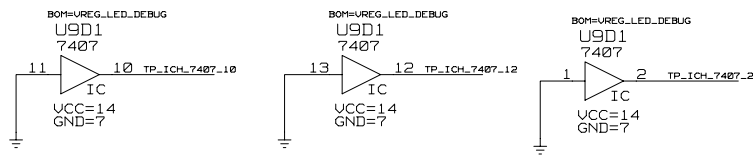
SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: BACKSIDE CAPS		SHEET: 61
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:15:19 2000	

DRAWING

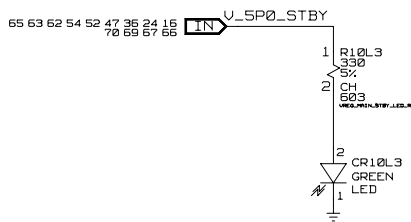
COST REDUCE ON PRODUCTS BY REMOVING DEBUG LEDS & BUFFER



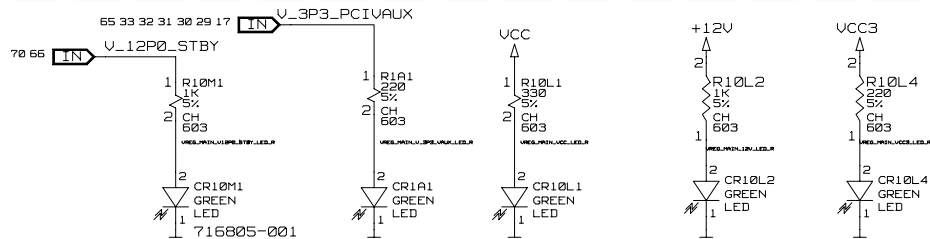
SPARE GATES



COST REDUCE ON PRODUCTS BY REMOVING DEBUG LEDS & BUFFER



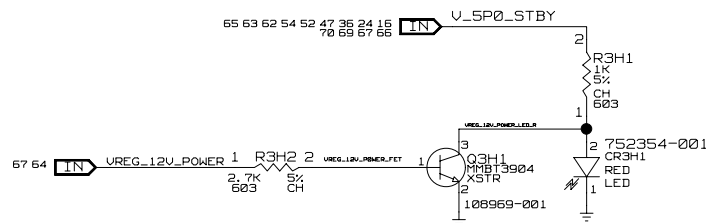
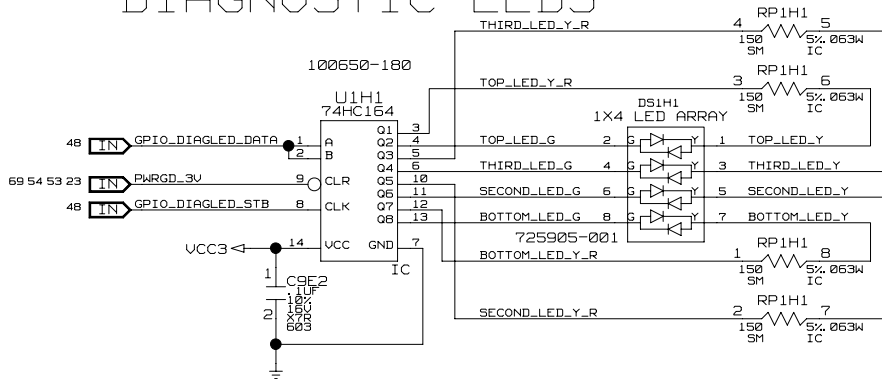
DESIGN NOTE: KEEP ON PRODUCTION BOARDS



DEBUG STUFFING OPTIONS: BOM=VREG_LED_DEBUG

COST REDUCE ON PRODUCTS BY REMOVING DEBUG LEDS

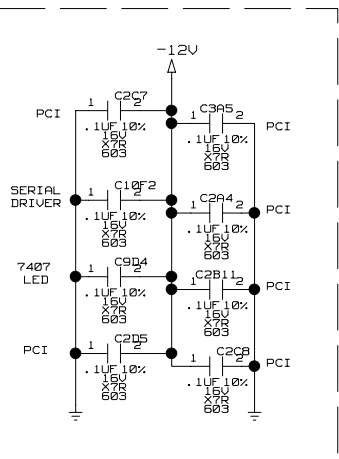
DIAGNOSTIC LEDS



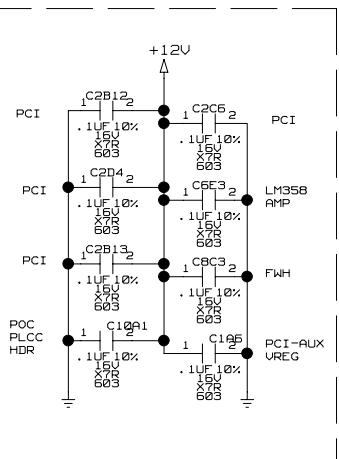
COST REDUCE ON PRODUCTS BY REMOVING DEBUG LEDS

SCHEMATIC TITLE: INTEL (R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: DEBUG_LED_DISPLAY		SHEET: 62
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:16:57 2000	

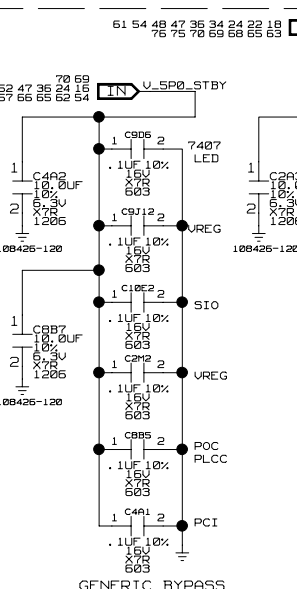
DRAWING



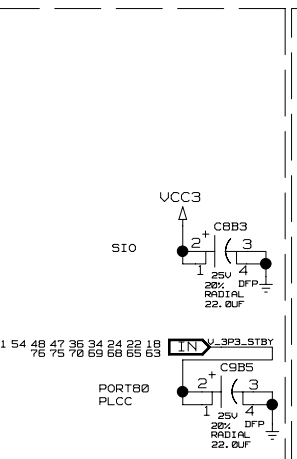
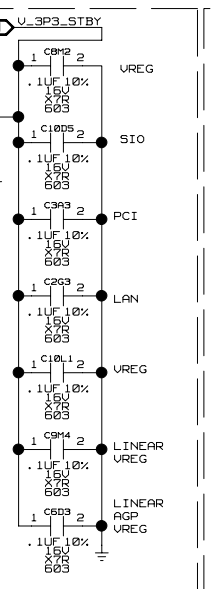
EVERY 3-4 ALONG TRACE
SPECIFIC DEVICE DECOUPLE
SHOULD BE ON DEVICE PG



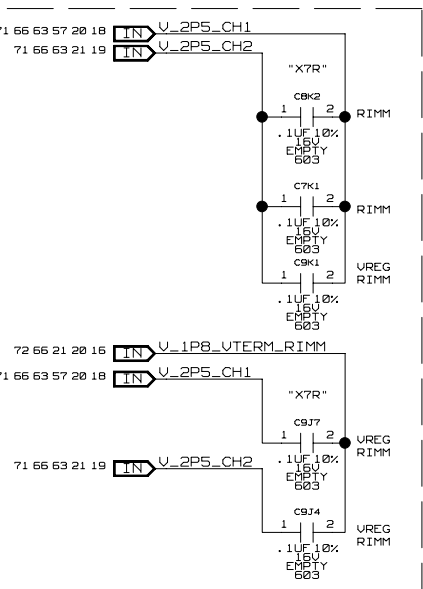
EVERY 3-4 ALONG TRACE
SPECIFIC DEVICE DECOUPLE
SHOULD BE ON DEVICE PG



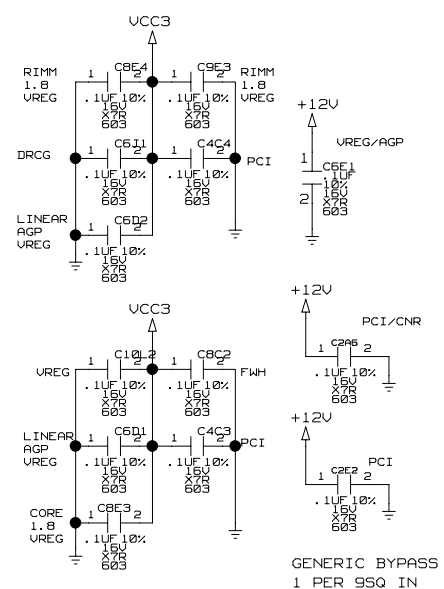
GENERIC BYPASS
1 PER 9SQ IN



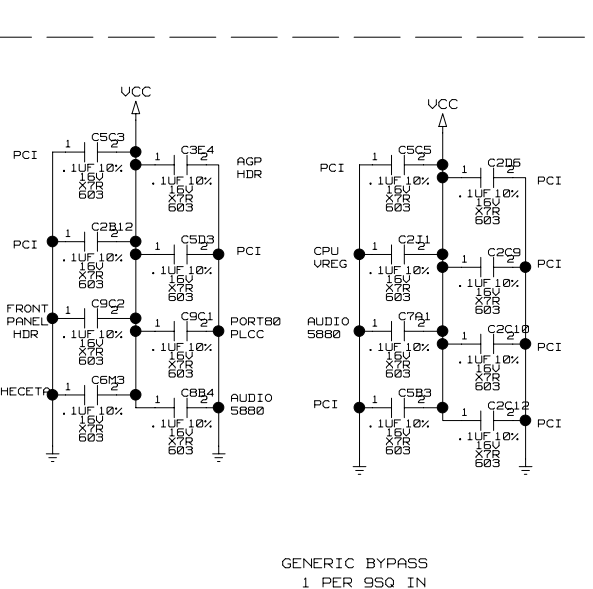
DRAWING



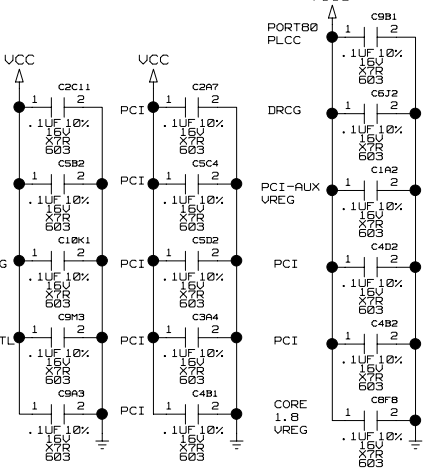
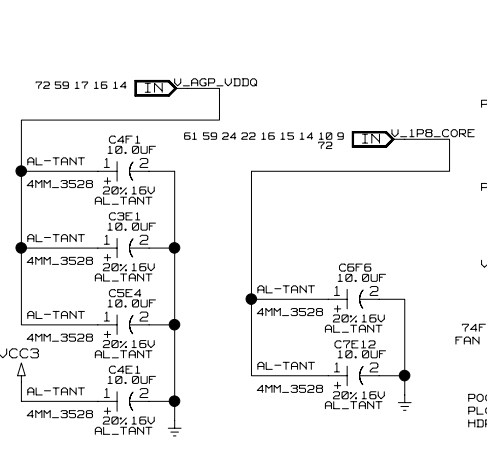
INTERPLANE BYPASS CAPS



GENERIC BYPASS
1 PER 9SQ IN



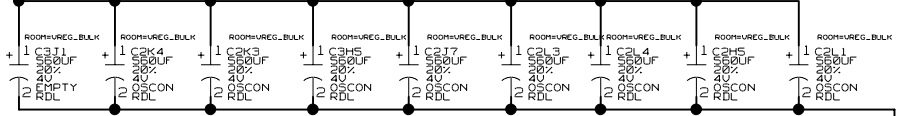
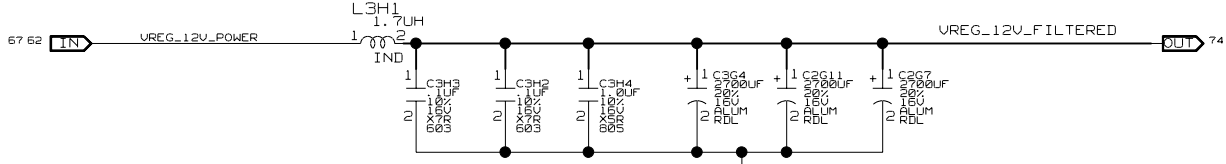
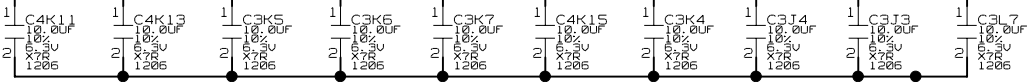
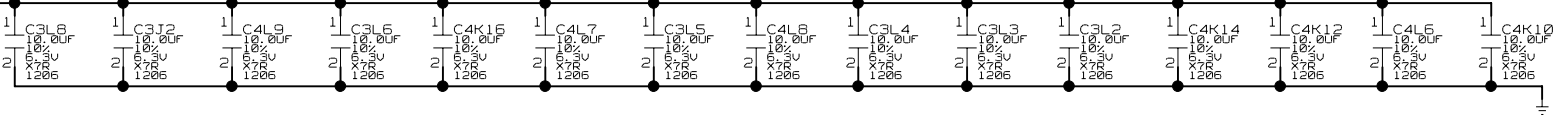
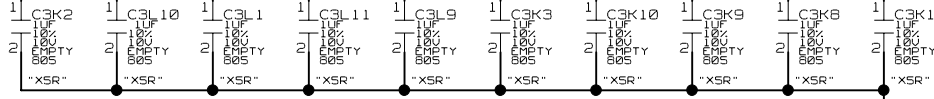
GENERIC BYPASS
1 PER 9SQ IN



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD			
PAGE TITLE: BULK DECOUPLING			REV: 3.0
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD, FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:19:19 2000		SHEET: 63

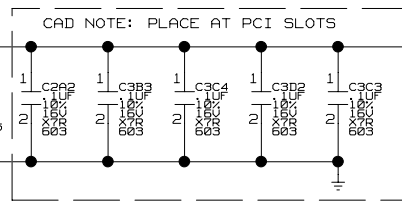
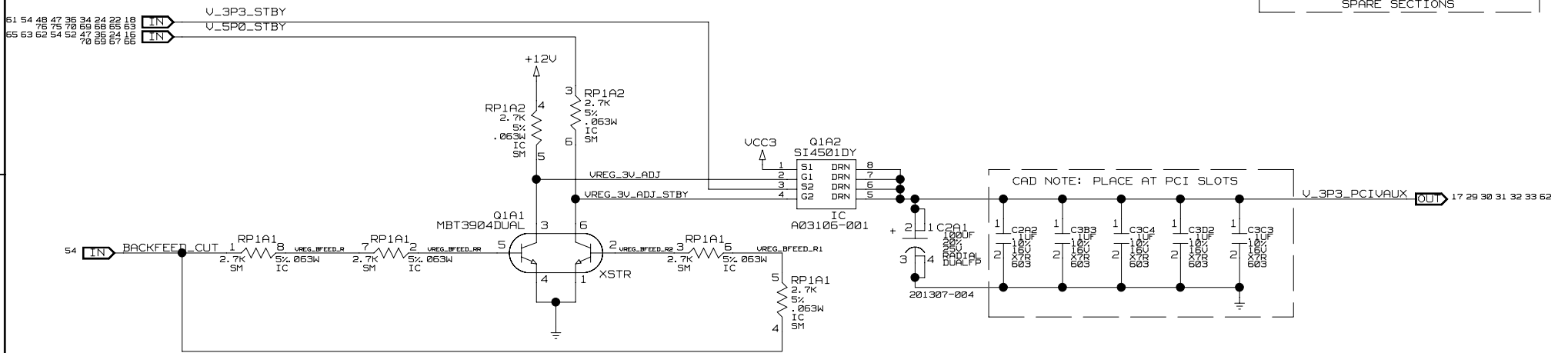
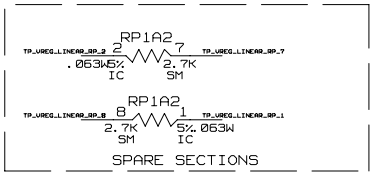
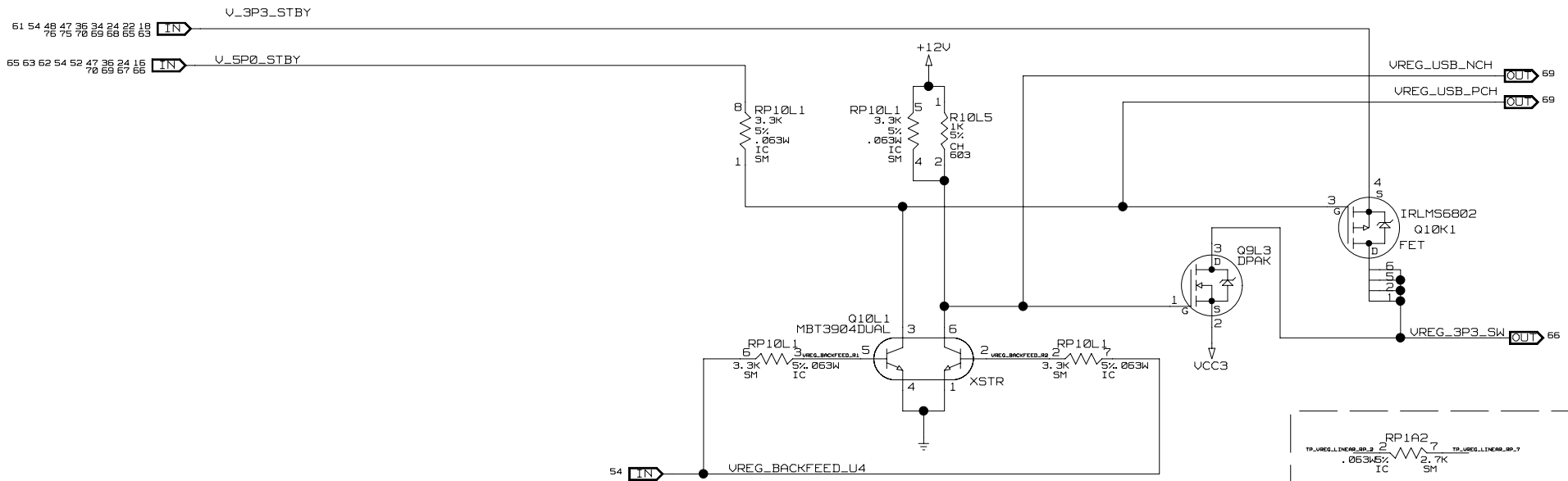
61 59 57 24 23 16 14 13 12
72 73

UCCP

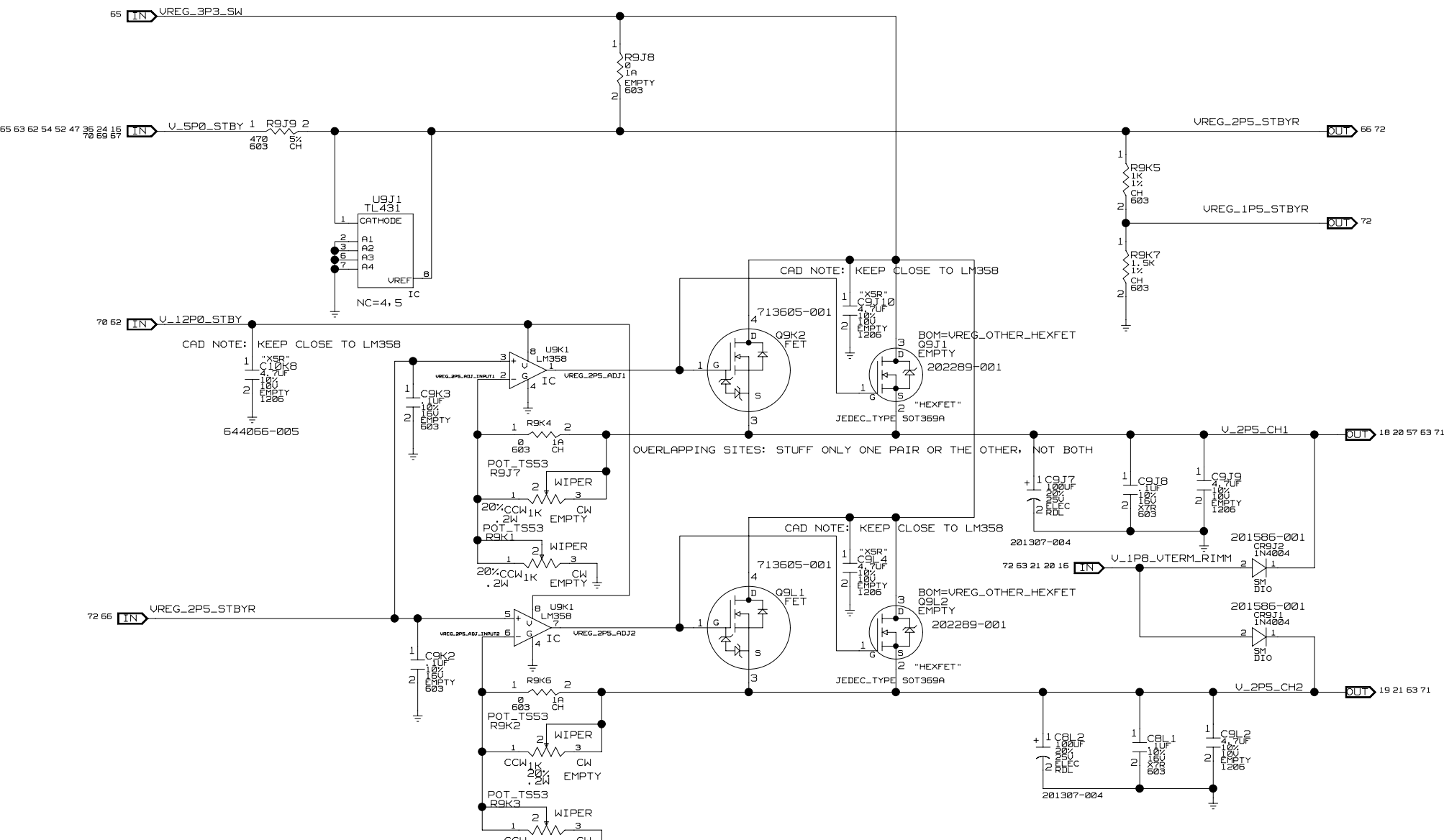


SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		
PAGE TITLE: CAPACITORS		REV: 3.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:20:41 2000	SHEET: 64

DRAWING:

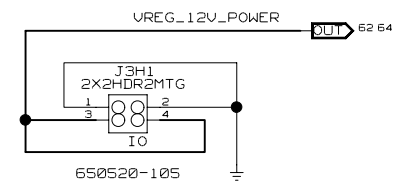
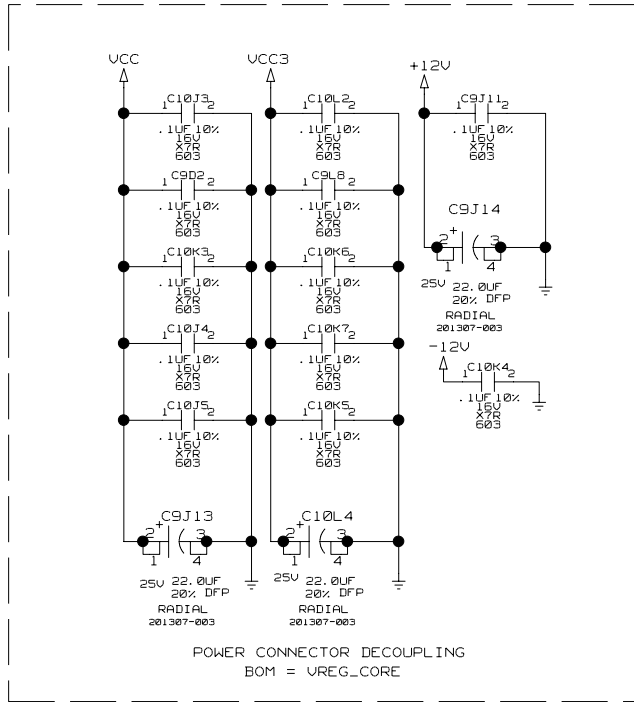
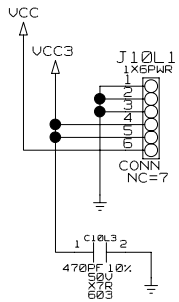
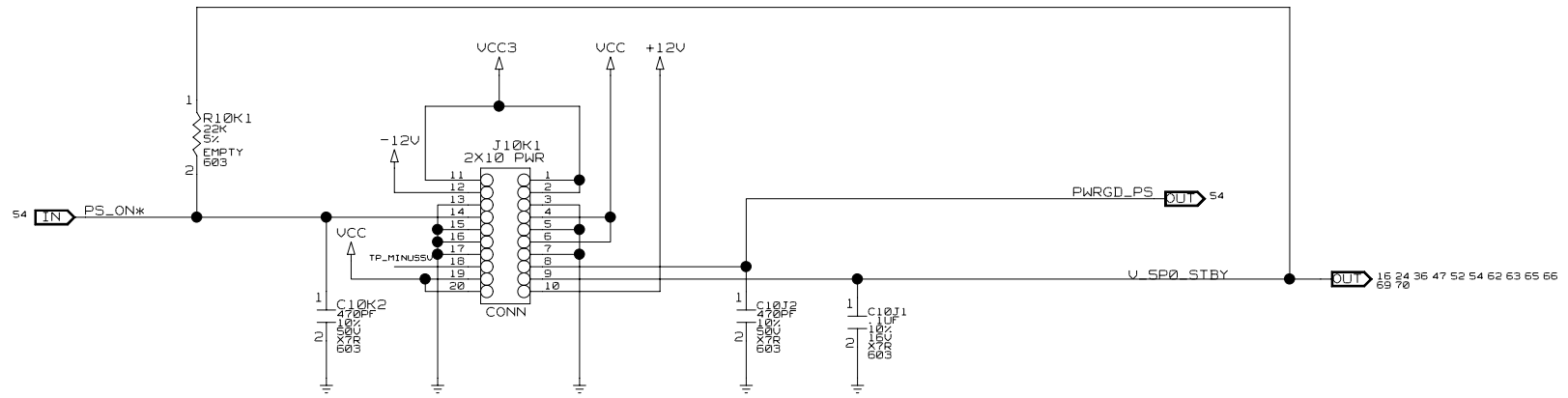


SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: LINEAR REGULATION		SHEET: 65
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:23:16 2000	



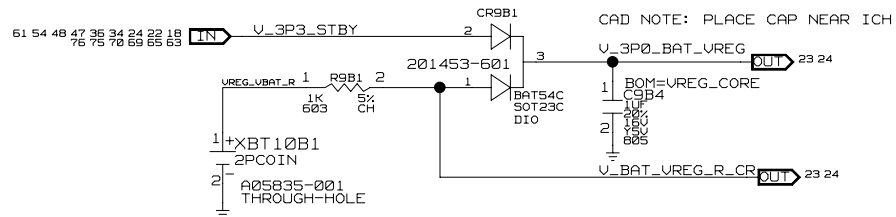
SCHEMATIC TITLE:		INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD
PAGE TITLE:		LINEAR REGULATION
DRAWING:		INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED:		Wed Nov 08 09:24:25 2000
REV:	3.0	
SHEET:	66	

CHANGED FROM DUAL-FOOTPRINT ON MODULE TO SINGLE FOOTPRINT 2X10 POWER CONNECTOR ONLY



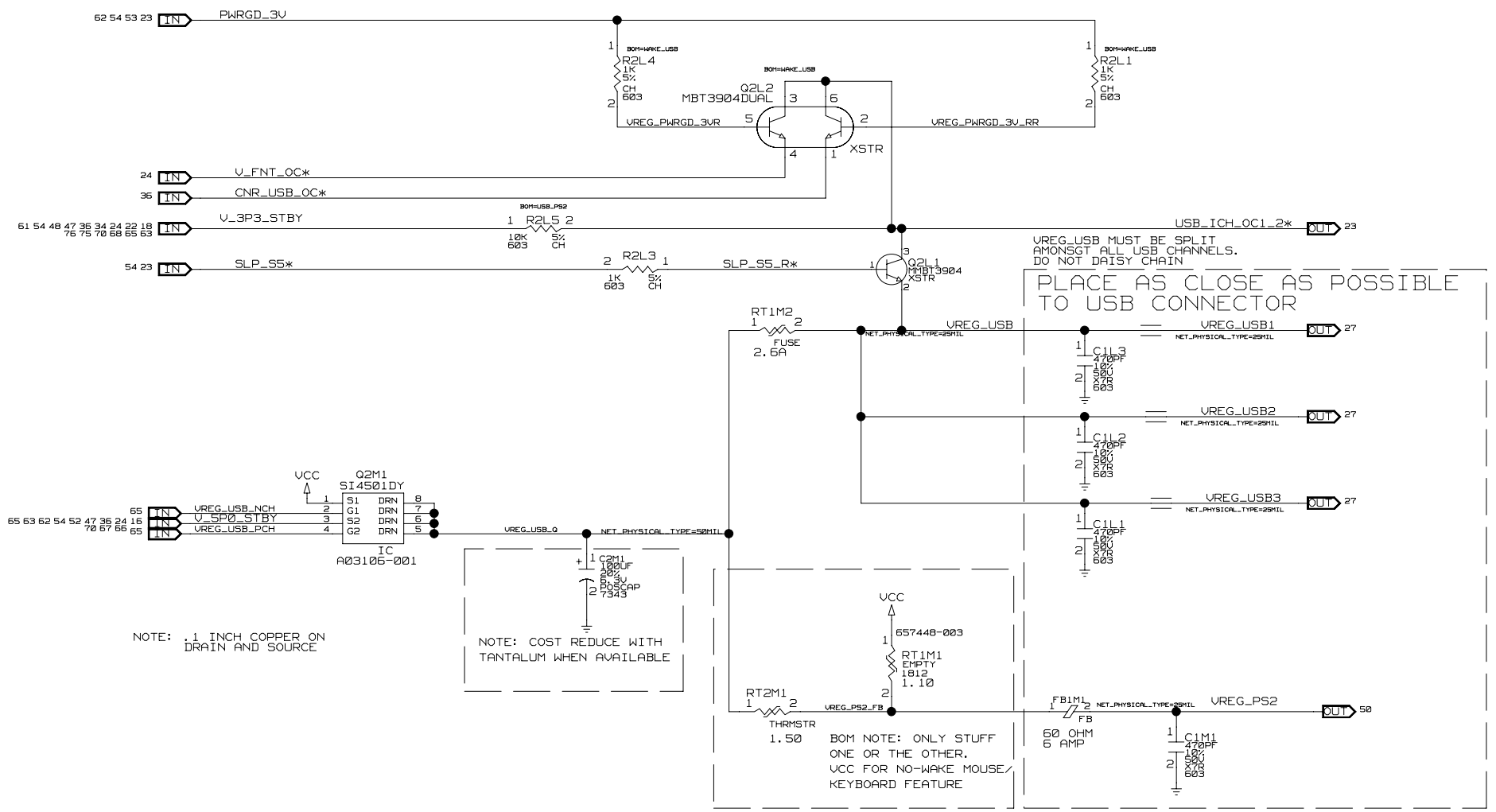
SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: STANDARD POWER CONNECTOR		SHEET: 67
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:38:55 2000	

DRAWING



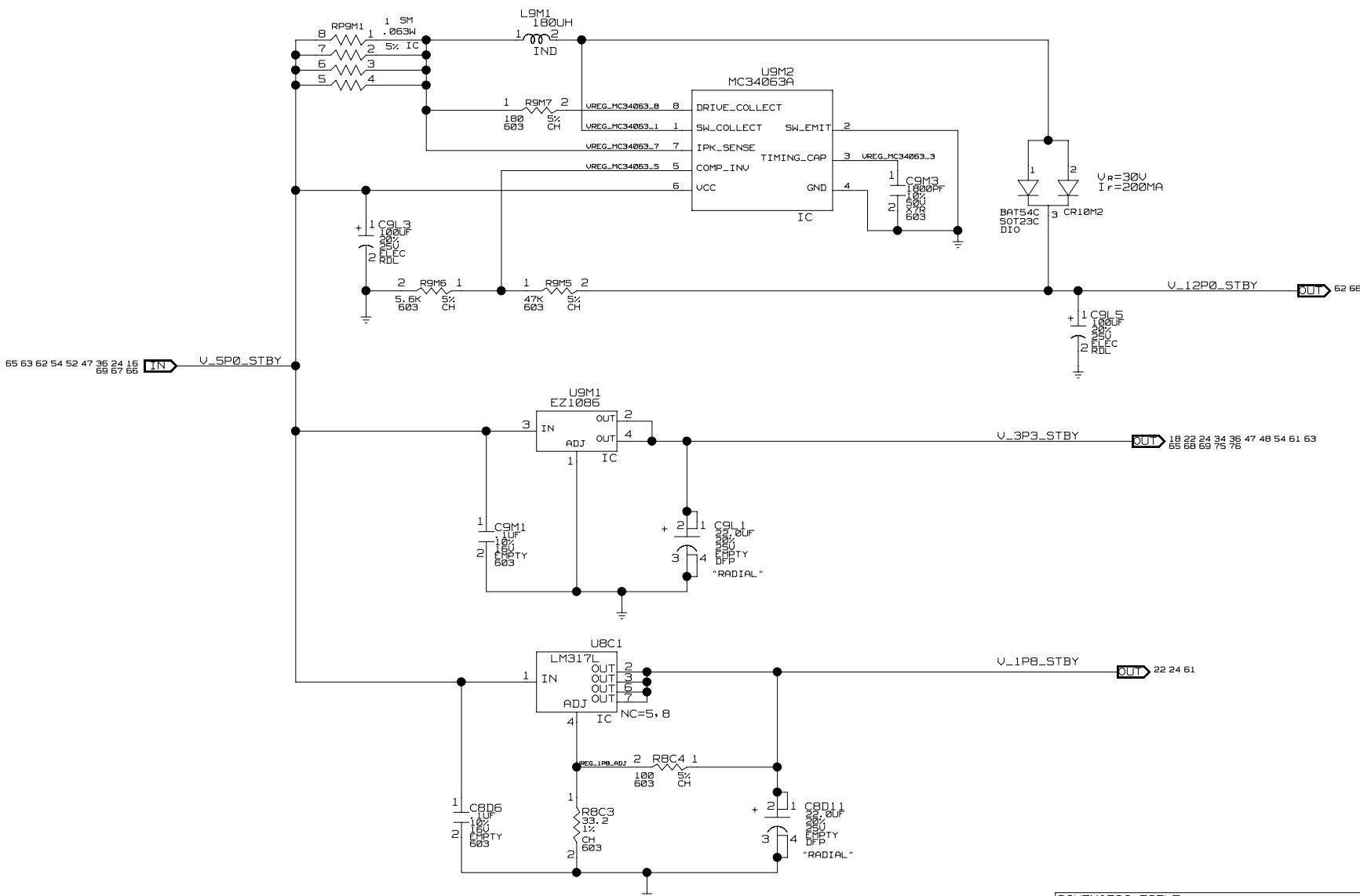
CAD NOTE: DO NOT PLACE BATTERY NEAR MOUNTING HOLES, GROUND OR VIAS

SCHEMATIC TITLE:		INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE:		BATTERY	
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		LAST REVISED: Wed Nov 08 09:44:00 2000	
DRAWING		REV: 3.0 SHEET: 68	

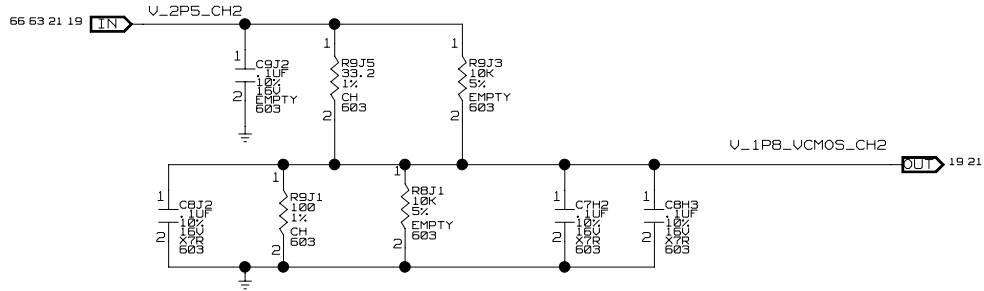
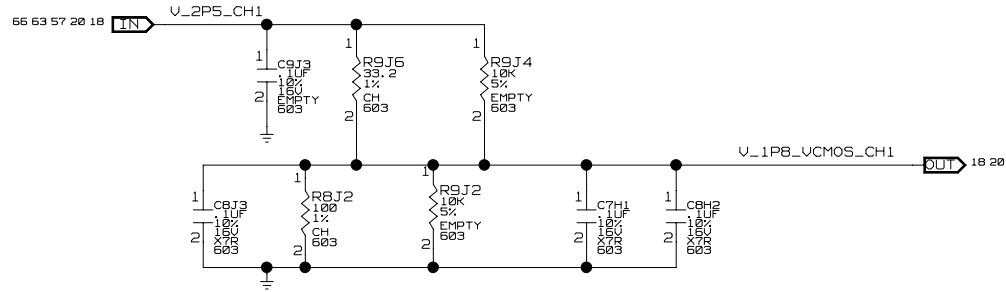


SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: WAKE ON USB & PS2		SHEET: 69
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:49:34 2000	

DRAWING

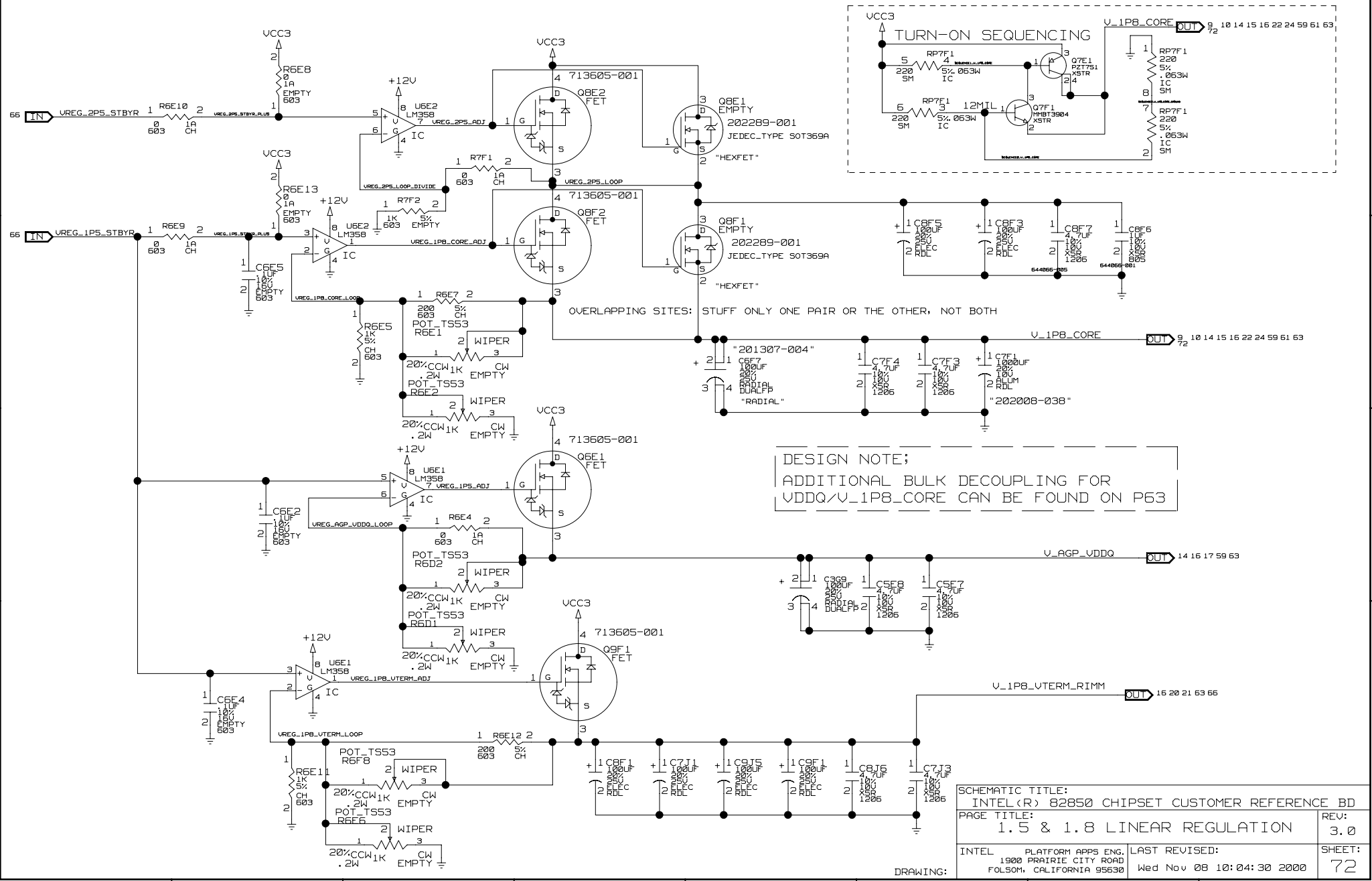


SCHEMATIC TITLE: INTEL<R> 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE: 12V/3.3V/1.8V STANDBY	
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:56:49 2000
DRAWING	REV: 3.0 SHEET: 70



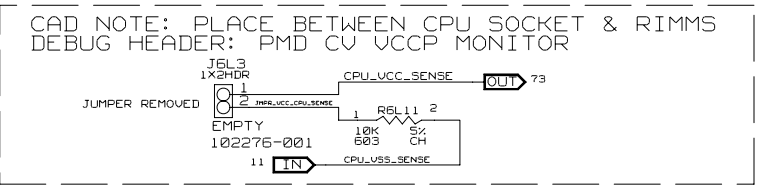
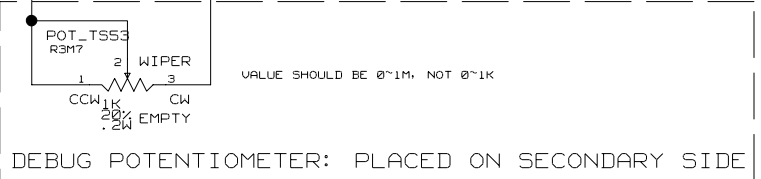
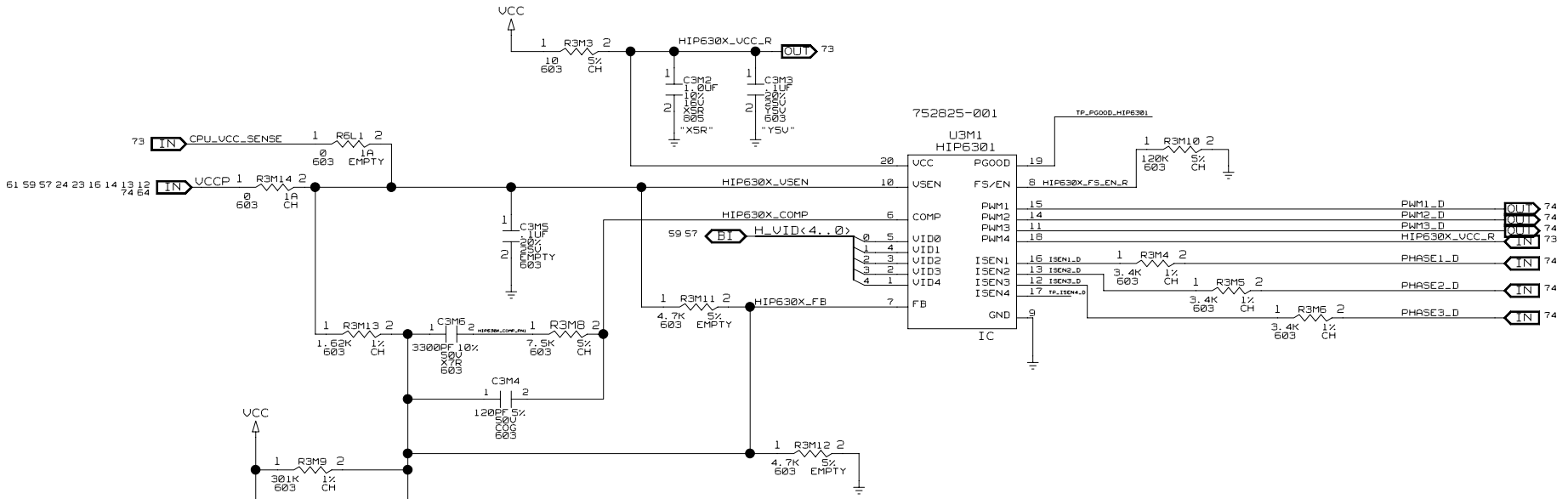
SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: VREG_1PB_VCMOS_RIMM		SHEET: 71
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 09:58:19 2000	

DRAWING

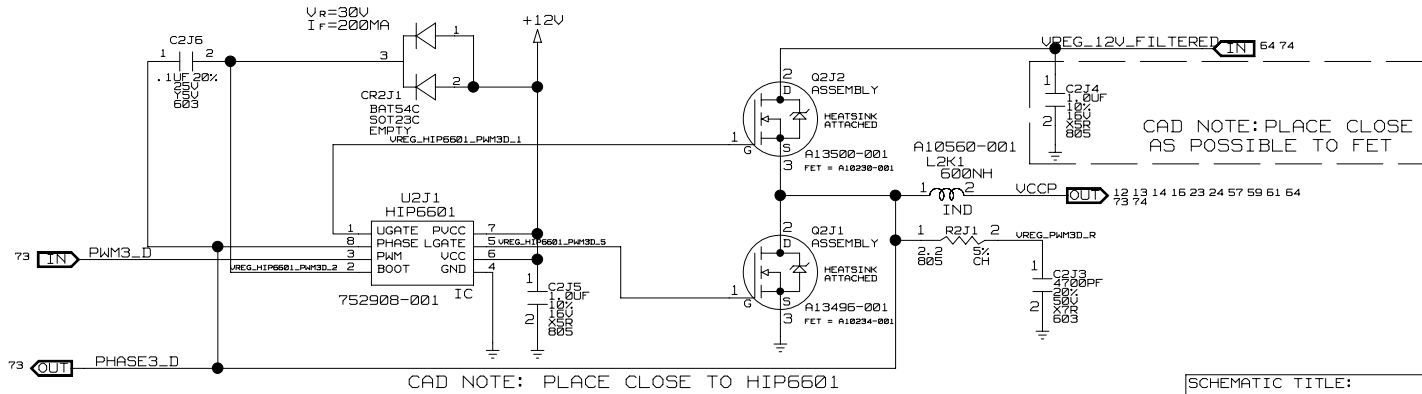
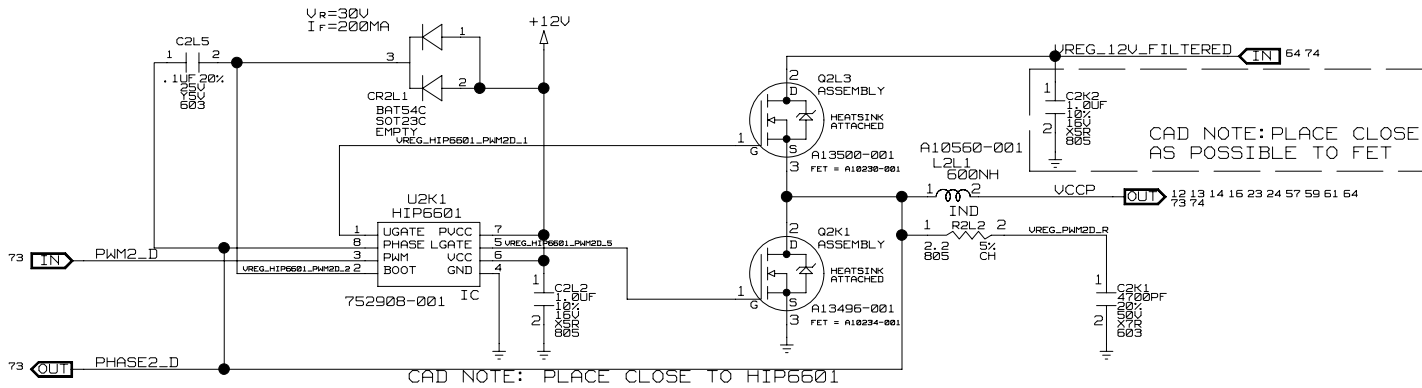
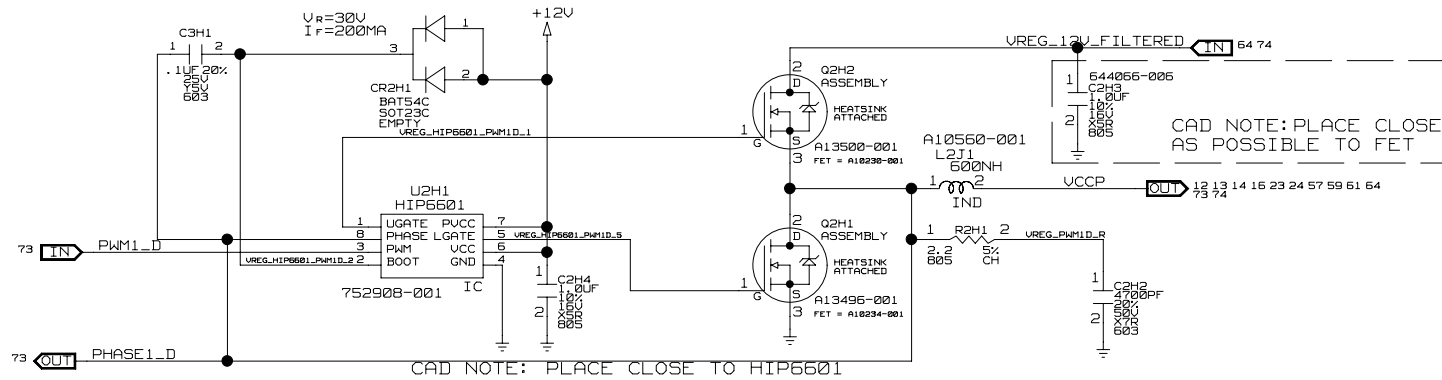


SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: 1.5 & 1.8 LINEAR REGULATION		SHEET: 72
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 10:04:30 2000	

DRAWING:

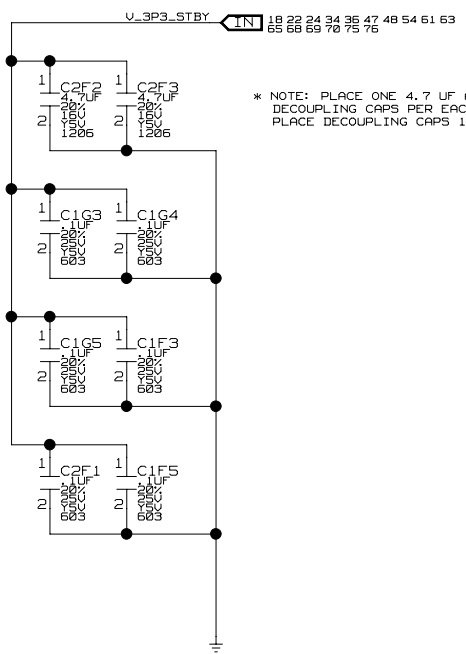


SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD	
PAGE TITLE: PROCESSOR REGULATION	REV: 3.0
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 10:06:14 2000
DRAWING	SHEET: 73

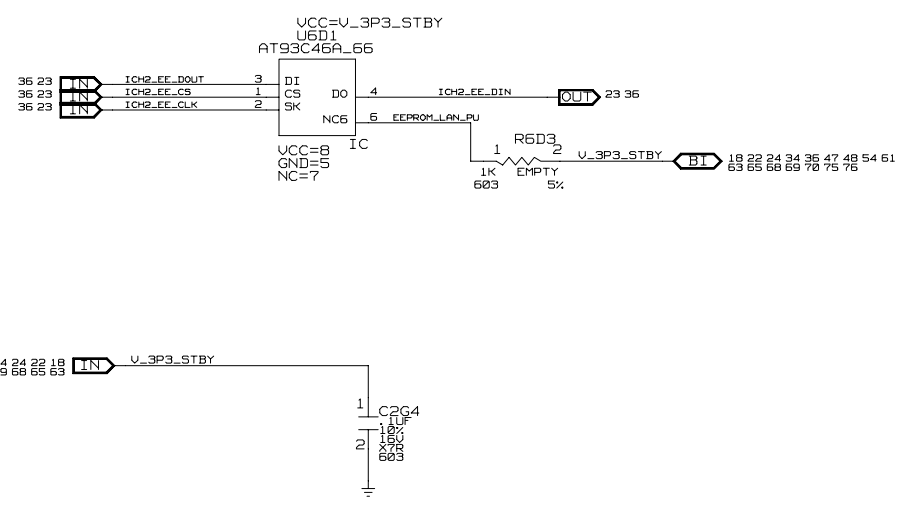


SCHEMATIC TITLE:		INTEL (R) 82850 CHIPSET CUSTOMER REFERENCE BD
PAGE TITLE:		UREG PROCESSOR
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 10:13:29 2000	REV: 3.0 SHEET: 74

DRAWING



* NOTE: PLACE ONE 4.7 UF AND TWO .1 UF DECOUPLING CAPS PER EACH SIDE OF 82559. PLACE DECOUPLING CAPS 130 MILS FROM 82559.



SCHEMATIC TITLE: INTEL(R) 82850 CHIPSET CUSTOMER REFERENCE BD		REV: 3.0
PAGE TITLE: ETHERNET_LAN_CONTROLLER		SHEET: 76
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Nov 08 10:20:43 2000	

DRAWING