

# Intel® 845E Chipset

**Specification Update** 

Intel® 82845 Memory Controller Hub (MCH) for DDR

**April 2003** 

**Notice:** The Intel<sup>®</sup> 82845 MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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# **Revision History**

Rev.	Draft/Changes	Date
-001	Initial Release	May 2002
-002	Corrected the Component Marking Information Table	June 2002
-003	Corrected the Component Marking Information Table	April 2003



### **Preface**

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

#### **Affected Documents/Related Documents**

Document Title	Document Number
Intel® 845E Chipset: Intel® 82845 Memory Controller Hub (MCH) Datasheet	290742-001

### **Nomenclature**

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Errata** are design defects or errors. Errata may cause the behavior of the Intel<sup>®</sup> 845E chipset MCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.



### **Component Identification via Programming Interface**

The Intel<sup>®</sup> 845E chipset MCH may be identified by the following register contents:

Stepping Vendor ID <sup>1</sup>		Device ID <sup>2</sup>	Revision Number <sup>3</sup>
E0	8086h	1A30h	11h

#### NOTES:

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- 1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
- 2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
- 3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

### **Component Marking Information**

The Intel 845E chipset MCH may be identified by the following component markings:

Stepping	Q-Spec	Top Marking	Notes
E0	QD12	RG82845ES	Engineering Sample, Desktop
E0	QD13	RG82845ES	Engineering Sample, Desktop, 533MHz System Bus
E0	SL66N	RG82845E	Production Stepping, Desktop, 533MHz System Bus
E0	QD28	RG82845E	Engineering Sample, Desktop, 533MHz System Bus
E0	SL69S	RG82845E	Production Stepping, Desktop, 533MHz System Bus



### **Summary Table of Changes**

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed Intel 845E chipset MCH steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

#### **Codes Used in Summary Table**

X: Erratum, Specification Change or Clarification that applies to this

stepping.

Doc: Document change or update that will be implemented.

PlanFix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

NoFix There are no plans to fix this erratum.

(No mark) or (Blank Box): This erratum is fixed in listed stepping or specification change does

not apply to listed stepping.

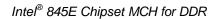
Shaded: This item is either new or modified from the previous version of the document

NO.	E0	SPECIFICATION CHANGES	
		There are no specification changes in this Specification Update revision	

NO.	E0	PLANS	ERRATA
			There are no errata in this Specification Update revision.

NO.	EO	SPECIFICATION CLARIFICATIONS
		There are no specification clarifications in Specification Update revision

NO.	EO	DOCUMENTATION CHANGES
		There are no documentation changes in Specification Update revision







# **Specification Changes**

There are no specification changes in this specification update revision.







### **Errata**

There are no errata in this specification update revision.







# **Specification Clarifications**

There are no specification clarifications in this specification update revision.







# **Documentation Changes**

There are no documentation changes in this specification update revision.