Flexible Small Form Factor Board Design Using the Intel® 855GME and Intel® 852GM Graphics Memory Controller Hubs

White Paper

August 2005

Order Number: 308964-001

Contents

Figures

Tables

Revision History

Date	Revision	Description
August 2005	001	Initial release.

1 Introduction

Small form factors are widely used for market segments such as industrial applications, consumer products, point of sale/information terminals, medical devices, communications, transportation, education terminals, traffic control, and many more.

Intel chipsets are widely used as the building block for small form factor design by third party board vendors. The Intel® 855GME Graphics Memory Controller Hub (GMCH) and Intel® 852GM GMCH are good embedded small form factor solutions with low BOM costs.

Because both GMCHs share similar features and both are physically and electrically compatible, it is clear that a flexible system board design for small form factor should be possible. This document will attempt to outline the minimal BOM, layout, and schematic changes required to achieve this. This implementation will lower inventory expenses, shorten design time, and speed up feature integration.

1.1 Feature Comparison

The table below provides an overview of the features supported by both GMCHs. Designers should use this table to determine which GMCH they require.

Table 1 Feature Comparison

	Intel® 855GME GMCH	Intel® 852GM GMCH
Processor	Intel® Celeron® M or Intel® Pentium® M Processor	Intel® Celeron® M Processor
System Bus	400 MHz	400 MHz
Memory Interface	Single channel DDR SDRAM and has advanced power management logic.	Single channel DDR SDRAM and has advanced power management logic.
	Support 128 Mbit, 256 Mbit, and 512 Mbit memory densities providing maximum capacity of 1 GByte when utilizing x16 devices and up to 2 GBytes with high density 512 Mbit technology.	Support 128 Mbit, 256 Mbit, and 512 Mbit memory densities providing maximum capacity of 1 GByte when utilizing x16 devices.
	Support 72-bit wide modules with ECC.	Without ECC.
	One channel of PC1600/2100/2700 SO-DIMM DDR SDRAM memory.	One channel of PC1600/2100 SO-DIMM DDR SDRAM memory.
	200/266/333-MHz (SSTL_2) DDR DRAM supported	200/266-MHz (SSTL_2) DDR DRAM supported
Display	Four display ports: Analog monitor, dedicated dual channel LVDS LCD panel, and two DVO devices.	Three display ports: analog monitor, dedicated dual channel LVDS LCD panel, and one DVO device.
	A single AGP component is supported by the AGP interface, which is capable of 1x/2x/4x AGP signaling and 2x/4x Fast Write.	ADD interface handles DVO signals.
South Bridge	Supports ICH4	Supports ICH4

1.2 Related Documents

The following table provides a list of collateral that is referenced by this document.

Table 2 Related Documents

Name	Internet Address	File Name
852GM GMCH Documentation	www.intel.com/design/chipsets/mobile/documentation852gm.htm	Design Guide: 25303803.pdf
855GME GMCH Documentation	http://developer.intel.com/design/chipsets/embedded/docs/855gme.htm#guide_c2	Design Guide: 30066904.pdf

1.3 Package Mechanical Comparison

The 855GME and 852GM GMCH both use the same 732-pin micro-FCBGA package with similar ballout. Thus, it is feasible to implement one footprint that can accommodate both GMCHs. This will speed up the redesign process by reducing schematic and layout modification.

Figure 1 Package Dimensions (Top View)

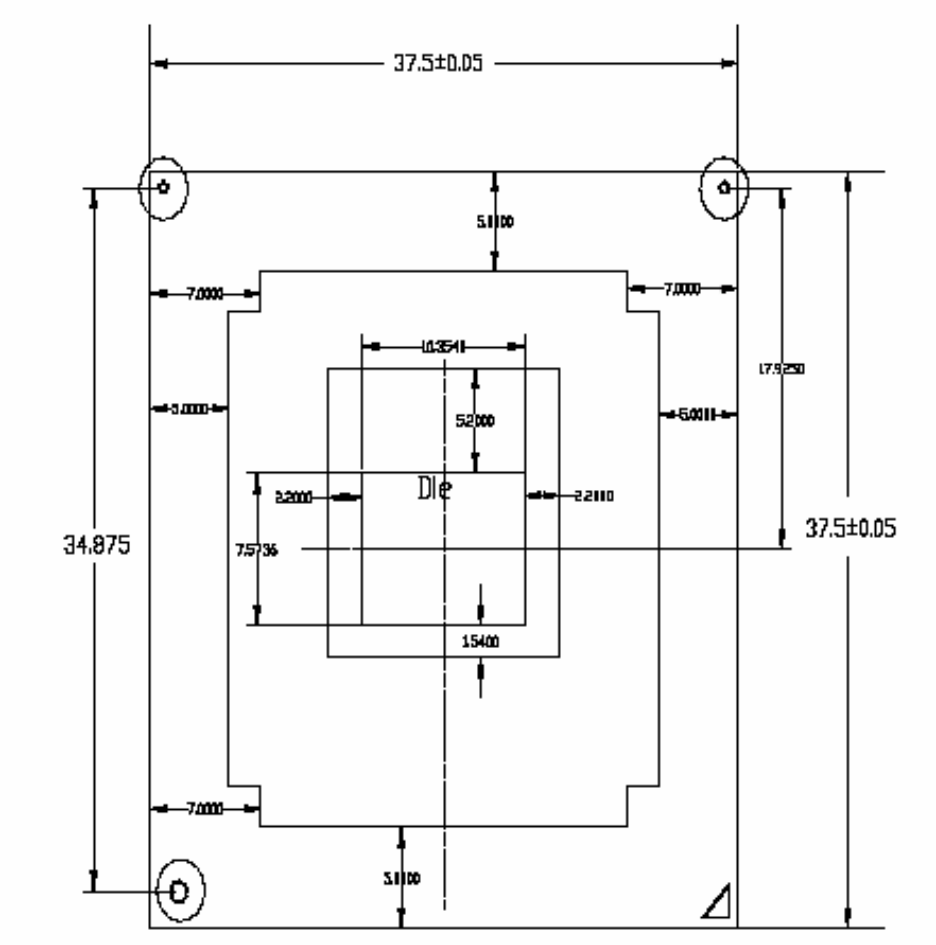


Figure 2 Package Dimensions (Side View)

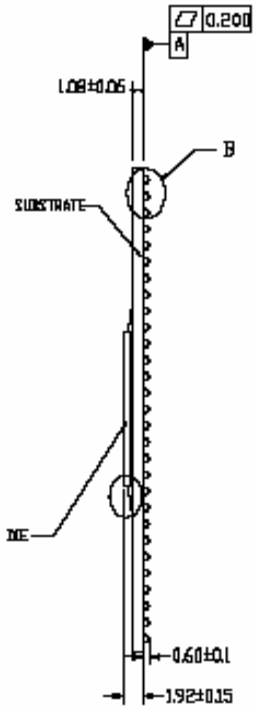
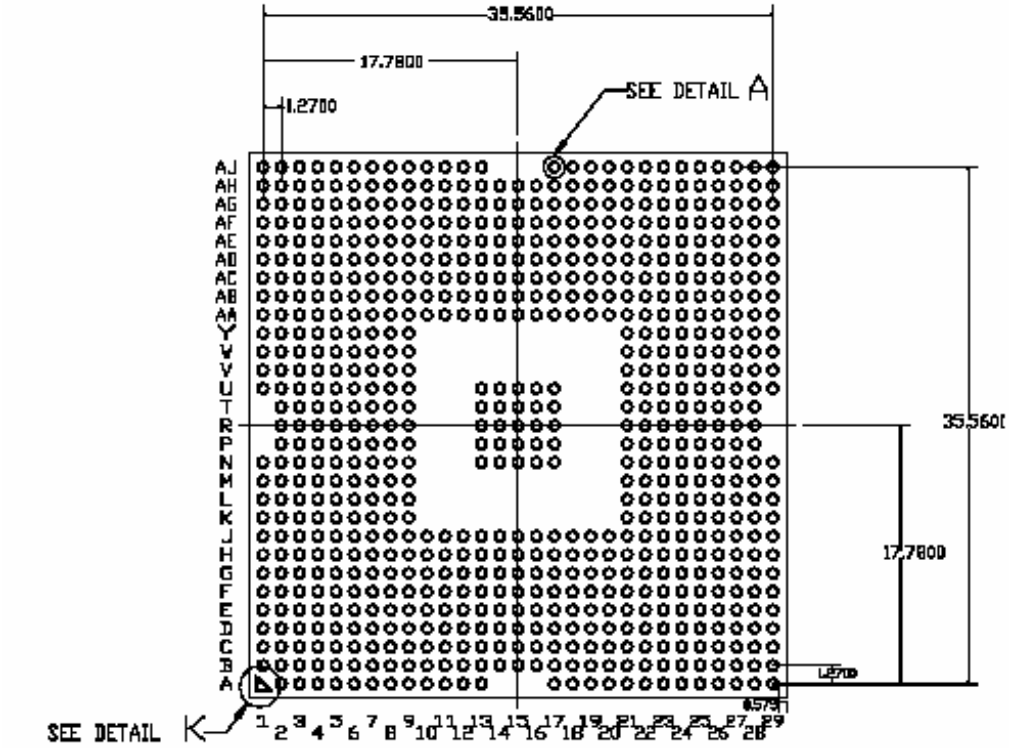


Figure 3 Package Dimensions (Bottom View)



2 Ballout Comparison

The following table lists the ballout differences between the 852GM and 855GME GMCHs.

Table 3 Ballout Comparison

Row	Column	852GM Signal Name	855GME Signal Name
M	5	RSVD	DVOBD[11]
N	5	RSVD	DVOBD[6]
N	3	RSVD	DVOBD[9]
N	2	RSVD	DVOBD[8]
P	5	RSVD	DVOBD[5]
P	4	RSVD	DVOBDCLK#
P	3	RSVD	DVOBDCLK
P	2	RSVD	DVOBD[7]
R	6	RSVD	DVOBD[2]
R	5	RSVD	DVOBD[1]
R	4	RSVD	DVOBD[3]
R	3	RSVD	DVOBD[0]
T	6	RSVD	DVOBHSYNC
T	5	RSVD	DVOBHSNYC
M	1	RSVD	DVOBD[10]

3 Layout and Schematic Comparison

This section discusses the critical schematic and layout guidelines that must be considered to ensure a flexible design.

3.1 Nominal Board Stack-up

Both GMCHs assume a target impedance of 55 Ω ±15%, yielding similar board stack-up requirements. Please refer to the platform design guides for further stack-up details for small form factor or embedded designs.

3.2 Front Side Bus (FSB) Design Guidelines

The 855GME GMCH supports the Intel® Pentium® M and Celeron® M Processors. The 852GM GMCH supports the Celeron M processor. The Celeron M processor can be used in the small form factor design since it is supported by both GMCHs.

It is necessary that the system designer meet the timing and voltage specifications of each component. The FSB signal groups, pin connections, schematic, and layout considerations are the same. Please refer to the platform design guides for further FSB design considerations.

3.3 System Memory Design Guidelines

Both GMCHs have DDR SDRAM system memory interface consisting of SSTL-2 compatible signals. These signals have been divided into several signal groups: data, control, command, CPC, clock, and feedback signals.

3.4 Major Schematic Differences (Signal Pins)

SO-DIMM memory is suggested in the small form factor design. A signal pin comparison for the 852GM and 855GME GMCHs is shown in the table below.

Table 4 Signal Pin Comparison

	Intel® 852GM GMCH	Intel® 855GME GMCH
Clock Signals	SCK [4,3,1,0] SCK# [4,3,1,0]	SCK [5:0], SCK#[5:0]
Data Signals	SDQ [63:0] Data Bus SDQS [7:0] Data Strobe SDM [7:0] Data Mask	SDQ [63:0] Data Bus SDQ [71:64] Check bit for ECC function SDQS [8:0] Data Strobe SDM [8:0] Data Mask

Three differential clock pairs are routed to each DIMM connector in the 855GME GMCH while two differential clock pairs are routed to each DIMM connector in the 852GM GMCH.

The 855GME GMCH has eight additional data check bit signals SDQ [71:64] for ECC function. Due to these extra ECC check bit signals, SDM [8] and SDQS [8] are also added to the 855GME GMCH. Designers are urged to take note of this while routing signals on these two different platforms.

3.5 Layout Considerations

Layout considerations for the memory portion of both platforms are the same. All signal groups are length matched per slot to the DDR clocks for both platforms except clock and feedback signal groups for both chipsets. Swapping of the byte lanes is also allowed for both platforms to facilitate routing SDQ [63:0]. Bit swapping within the SDQ [71:64] byte lane is not allowed.

Table 5 Intel® 855GME GMCH System Memory Length Matching Formula

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock – 2.0 inches	Clock - 0.5 inches
Command to Clock	Clock – 2.0 inches	Clock + 2.0 inches
CPC to Clock	Clock – 2.0 inches	Clock – 1.0 inches
Strobe to Clock	Clock – 2.0 inches	Clock + 0.5 inches
Data to Strobe	Strobe - 25 mils	Strobe + 25 mils

Note: Length matching formula is based on total length of the GMCH die pad to SO-DIMM pin.

Table 6 Intel® 852GM GMCH System Memory Length Matching Formula

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock - 1.0 inches	Clock + 0.5 inches
Command to Clock	Clock - 1.0 inches	Clock + 2.0 inches
CPC to Clock	Clock - 1.0 inches	Clock + 0.5 inches
Strobe to Clock	Clock - 1.0 inches	Clock + 0.5 inches
Data to Strobe	Strobe - 25 mils	Strobe + 25 mils

Note: Length matching formula is based on total length of the GMCH die pad to SO-DIMM pin.

3.6 Integrated Graphic Design Guidelines

The 852GM GMCH contains three display ports: an analog CRT port, a dedicated LVDS port, and a 12-bit Digital Video Out (DVO) port.

The 855GME GMCH contains four display ports: an analog CRT port, a dedicated LVDS port, and two 12-bit DVO ports: DVOB and DVOC.

3.6.1 DVO Port Design Guidelines

The 855GME GMCH supports a flexible, modular design for the DVOB and DVOC ports, connected to the GMCH through a generic connector. The 852GM does not have this feature.

The design and layout considerations are the same for all DVO ports on both platforms, as documented in the *Intel® 855GME GMCH Design Guide*. The DVO interface trace length mismatch requirement is also the same.

Please refer to the platform design guides for details when designing additional DVO ports.

3.6.2 AGP Port Design Guidelines

The 855GME GMCH has an AGP interface and acts as a multiplexer for the ADD interface or external graphic interface. The AGP interface supports 1x/2x/4x AGP signaling and 2x/4x Fast Writes.

The 852GM GMCH does not have an AGP interface, and all DVO signals will be routed to the ADD interface.

Please refer to the platform design guides for detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms) and for design and routing considerations.

3.7 Hub Interface Design Guidelines

The hub interface connects the ICH4 to the GMCHs. Except for the differences in RCOMP resistor values show in the tables below, both platforms have the same design guidelines for hub interface design.

Please refer to the platform design guides for voltage divider circuit designs for HLVREF and HISWING.

Table 7 Intel® 855GME GMCH RCOMP Resistor Values

Component	Trace Impedance	Value	Tied To
Intel® 82801DB ICH4	55 Ω ±15%	48.7 Ω ±1%	Vcc1.5
Intel® 855GME GMCH	55 Ω ±15%	37.4 Ω ±1%	Vcc1.35

Table 8 Intel® 852GM GMCH RCOMP Resistor Values

Component	Trace Impedance	Value	Tied To
Intel® 82801DB ICH4	55 Ω ±15%	48.7 Ω ±1%	Vcc1.5
Intel® 852GM GMCH	55 Ω ±15%	27.4 Ω ±1%	Vcc1.2

4 Platform Power Delivery Comparison

Both GMCHs use IMVP IV for voltage level generation. The power and power sequencing requirements are also the same. On both platforms, the power rails should be stable before PWROK is asserted. Please refer to the platform design guides for platform power delivery guidelines.

5 Platform Clock Routing Comparison

Both GMCHs use the same clock synthesizer/driver component: the CK408 Clock Generator. The system clocks are considered as a subsystem in themselves. Several vendors offer suitable products, as defined in the Intel® CK408 Synthesizer/Driver Specification. Please refer to the platform design guides for platform clock routing guidelines.

6 Conclusion

Designers can use either the 855GME or 852GM GMCH in the small form factor design without major modifications in layout or schematics. The 855GME has several additional features not found on the 852GM. In short, only minor design changes are needed to design a platform to work with either GMCH.