Interfacing Flat-Panel Displays with Intel® Chipsets

Application Note

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Revision History

Date	Revision	Description
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1.0 Abstract

When considering video displays for embedded applications, a liquid crystal display (LCD) flat-panel display (FPD) is an attractive solution. It can be designed and installed into tight spaces and provides a high-resolution image in a low-profile application.

LCD technology basically is a sandwich of layers. In the middle is a layer of liquid-crystal, organic compound. The electrical and optical characteristics of liquid-crystal, organic compounds is the basis for the operation behind the modern flat-panel display.

The optical characteristics of the crystals can twist light 90 degrees. Adding polarizing layers on the top (back side) and bottom (front) enables light to pass from one side of the flat panel to the other, when the crystals are twisted. This technology blocks the light when the crystals are untwisted.

The organic crystal compound is naturally ionized. This ionization allows rotational control when an electric field is applied across the crystal compound to untwist the crystal helix.

Putting criss-crossing, transparent electrodes across the back and front of the flat panel allows X - Y coordination of turning on and off the liquid crystal cells that create pixels on the LCD. This is called “passive” STN (Super Twist Nematic) technology.

Adding a transistor to the location of each cell — at the points where the X and Y electrodes cross —gives more active control of the LCD crystals’ untwisting. This called “active” or TFT (Thin Film Transistor) technology.

Double-layer SuperTwist Nematic (DSTN) displays rely on the capacitance charge driven across the LCD cell to hold the twist off while the rest of the cells are sequentially driven. This causes ghosting when high-speed video is displayed. TFT displays use an active transistor to drive the charge across the LCD cell and are faster at twisting and untwisting the LCD helix. This is better for high speed video.

Adding the transistor to each cell of an LCD display, however, increases the cost of the TFT panels, as compared to DSTN displays.

Intel’s Graphics Memory Control Hub (GMCH) contains all of the necessary graphics-engine components to drive modern, embedded-graphics displays, including cathode-ray tube (CRT) and flat-panel displays. The Digital Video Out (DVO) port is designed for digital transmittal to FPDs using LCDs. But the GMCH doesn't support the features needed for direct interfacing of the DVO port to a DSTN display. Utilizing third-party vendors, DSTN displays can be interfaced effectively to Intel’s GMCH chips, through either the PCI or Accelerated Graphics Port (AGP) bus.

Interfacing the TFT flat panel to the Intel GMCH is as simple as converting the DVO signals to DVI. This is done using a third-party transmitter chip that interfaces with a flat panel interface using a third-party receiver chip. The transmitter/receiver also enables the GMCH to be located farther from the TFT flat panel display.

In conclusion:

- Passive, DSTN LCD technology is a viable solution where cost is an issue and high performance is not an issue.
- Passive, DSTN LCD technology is best implemented using a third-party graphics subsystem that works with the Intel graphics engine.

- Active, TFT LCD technology is a high-end solution that is viable when cost is *not* a consideration.
- Active, TFT FPD technology is best implemented by using a third-party, Transition Minimizer Differential Signal (TMDS) transmitter/receiver pair to interface the Intel graphic engine's DVO port with the flat-panel display.

In the near future, the desktop market will see larger LCD flat panel displays and improved screen resolutions. Manufacturers are starting to add receiver chips inside flat-panel displays to interface directly to the DVI signals coming out of DVO transmitter chips. As these new FPDs are integrated into embedded applications, there will be a growing need to add the necessary hardware to interface to these receiver/flat panel display combined units.

This paper's reference schematics provide details on connecting an Intel GMCH to a DSTN and TFT flat panel.

2.0 Introduction

While technological advances have been fast-paced — for processors, networks, peripherals, and software — there has been little change in video displays, over the past five years. Primarily, the changes have been to improve the display frequencies and resolutions of existing technology.

Most computer monitors still use an analog, Video Graphics Array (VGA) port, an aging technology that represents the minimum standard for PC displays. This situation has, in fact, slowed the adoption of new display technology because of the additional costs of supporting this widespread, analog interface.

Meanwhile, this legacy technology has diminished the advances of digital solutions — the analog interface degrading image quality, when the digital signal must be converted to analog and back to digital, before an image is displayed. With the spread of flat-panel, digital monitors, however, the uses and expectations of digital displays have dramatically increased. Flat-panel displays, such the liquid crystal display (LCD), are being incorporated into everyday embedded electronics appliances — from point-of-sale terminals to DVD players.

As PC technology evolves and the demand for high-performance displays increases, video-display and graphics-controller developers are re-examining the technology that connects computers and displays.

Existing embedded designs utilizing Double-layer SuperTwist Nematic (DSTN) displays can use the Intel architecture in their design without a system redesign. Adding a third-party graphics chip allows existing designs to upgrade to higher-performance Intel processors and chipsets while maintaining existing DSTN-display graphics solutions. There are issues surrounding this option, however, and those are addressed in this paper.

One issue with Intel-DSTN solutions is performance. This issue can be resolved by interfacing a TFT display directly to Intel's DVO graphics port.

This paper examines how to interface Intel architecture to flat-panel technology for embedded markets, beginning with an overview of LCDs and their "passive" and "active" technologies. The Intel graphics engine is examined next, followed by an explanation of how to interface that engine with passive and active LCDs.

Note: If you only wish to read about interfacing the Intel® 810 Chipset with LCDs, see "Intel Implementations for LCDs" on page 25.

3.0 Liquid Crystal Displays

This section examines the basics of liquid crystals and liquid-crystal display (LCD) technology, the two types of LCD technology, and the components of contemporary LCD panels. Also discussed are the basic principals of light and light polarization and how those elements are used in LCDs.

This section's topics include:

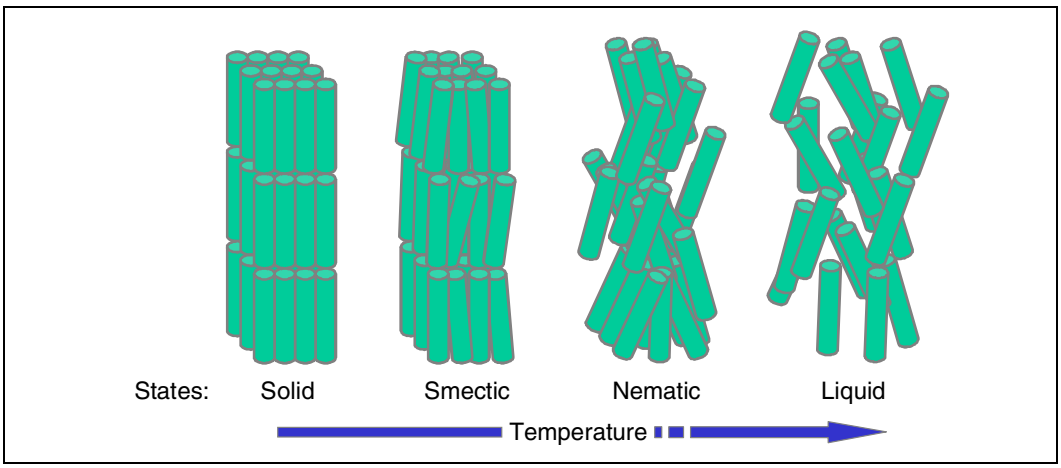
3.1 Liquid Crystals

Much of the functionality of an LCD relies on the behavior of liquid crystals. A sealed container of liquid crystals is one of the component layers of the device. The crystals in the liquid solution are aligned to pass light or unaligned to block the light.

At any given temperature, pressure, and volume, chemical matter has a physical state of solid, liquid, or gas. Liquid crystals are organic compounds whose state is between solid and liquid. The in-between states — going from solid to liquid — are called nematic and smectic. (See Figure 1.)

In the nematic phase, the crystals are loosely aligned in the "natural" structure that reflects the chemical structure of the composite molecules. In the smectic phase, the crystals are more closely aligned with each other.

Figure 1. Liquid Crystal States



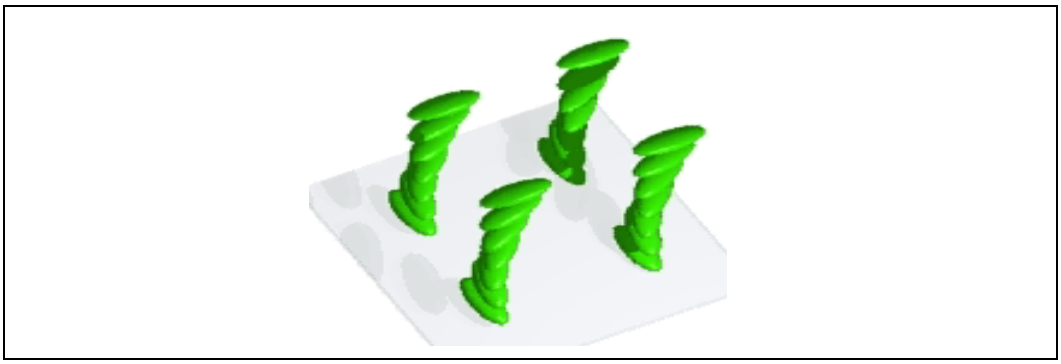
As the temperature decreases, the organic crystal structure becomes more like a solid and turns into a paste. This makes it harder for the crystals to realign, slows the LCD's response time, and degrades the legibility of the displayed image.

As the temperature increases, liquid crystals become more like a liquid, the crystals going out of alignment, with fewer crystals aligned to pass light. This also makes the display difficult to read.

For embedded applications that run in extreme temperatures, both of these conditions are potential problems that should be considered, when selecting a flat-panel for a particular application.

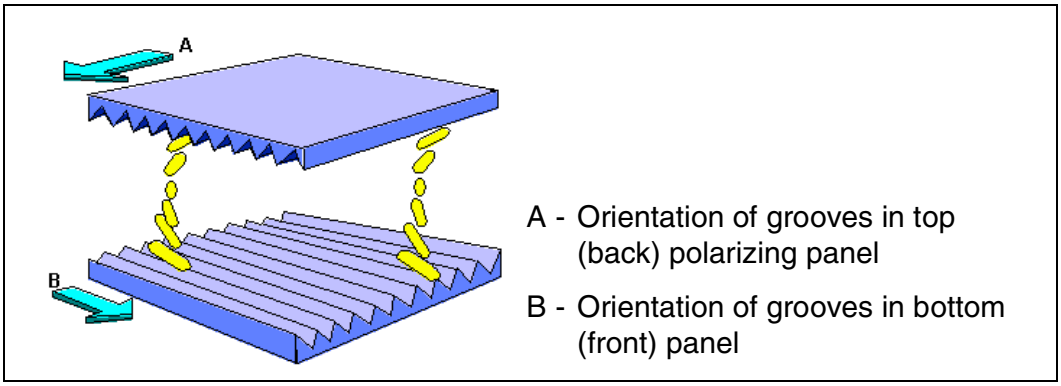
An LCD's design uses the natural alignment of the liquid crystals to arrange the crystals in a twisting shape. (See Figure 2.) This twisted shape pulls the crystals out of alignment, preventing the light from being passed and producing the LCD's "off" condition.

Figure 2. Three-Dimensional Representation of Twisted Crystals in LCDs



This twisting shape is created by putting grooves in the LCD's front and back panels that are 90 degrees out of alignment with each other. (See Figure 3.) As the top and bottom crystals align themselves with the grooves in the panels, the crystals form the twisting shape.

Figure 3. Liquid Crystal Twisting from Back (Top) to Front (Bottom) LCD Panel



Another characteristic of liquid crystals — that is important to LCD functionality — is that the crystals are a naturally ionized compound. Because of that, the crystals can be moved into varying degrees of alignment by putting an electrically charged field across the crystal solution.

Figure 4 shows how an electrical charge is used to align a single liquid crystal. Figure 5 shows how an LCD's electrical field is applied to realign the crystals. The three steps demonstrate how the crystals gradually become aligned, after the charge is applied.

Figure 4. Ionization and Electrical Realignment of Liquid Crystals

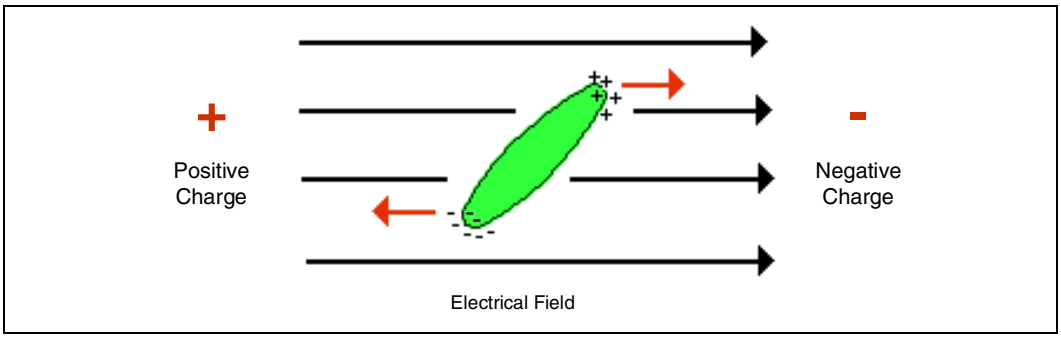
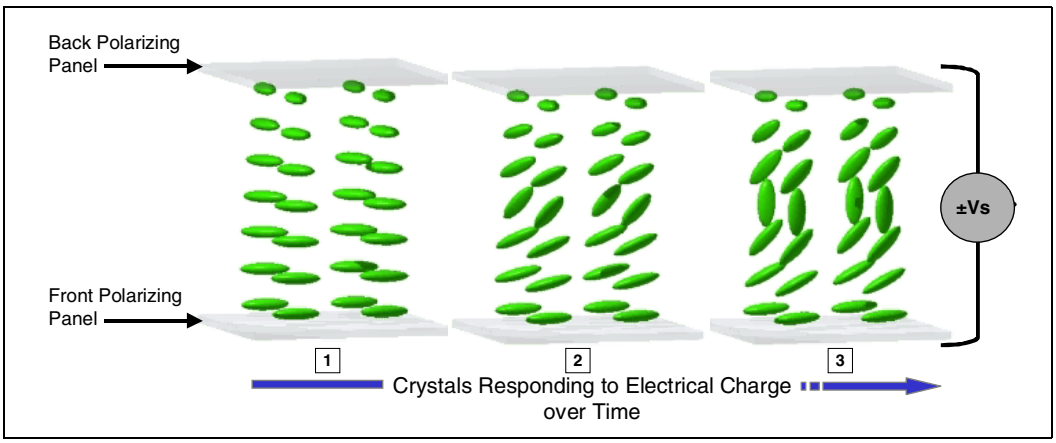


Figure 5. Electrical Field Altering Liquid-Crystal Alignment



When there is no electrical field, the crystals return to their natural, twisting shape. That produces the "on" condition where light is passed by the crystals. When an electrical charge is applied, the crystals are moved out of alignment, so that they can not pass light — producing the "off" condition.

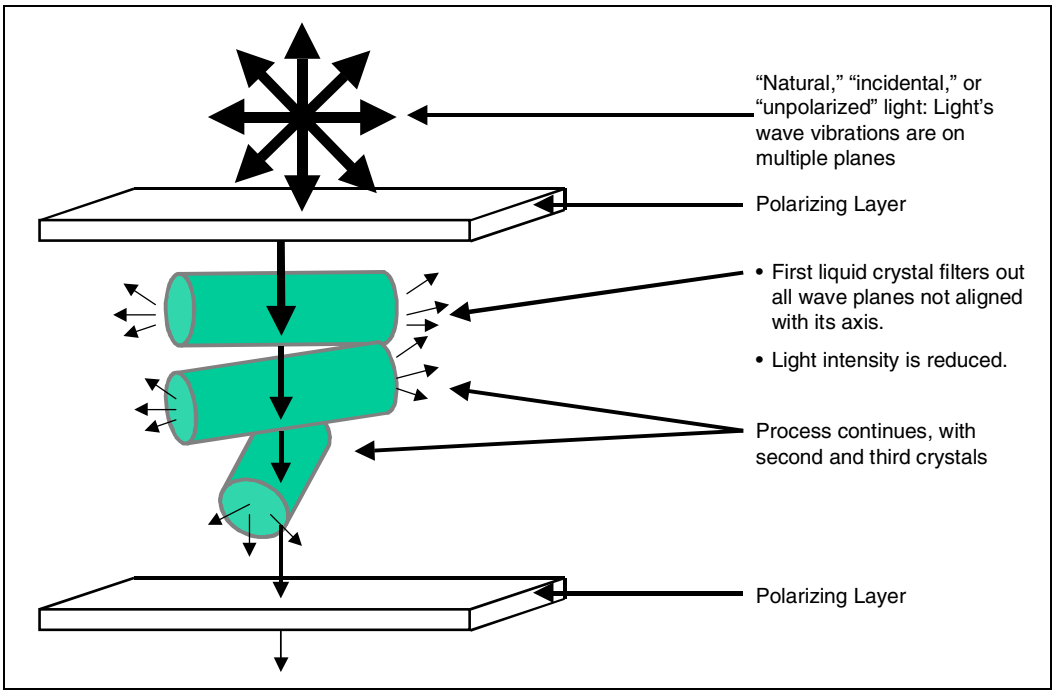
3.2 Light, Polarization, and Liquid Crystals

Light behaves like a particle, a "photon," and a wave, as an electromagnetic wave. LCDs' functionality is based on liquid crystals' interaction with light's wave characteristics.

The wave vibrations of "natural" or "incidental" light are on multiple planes, as shown in Figure 6. When incidental light's multiple-plane waves strike a liquid crystal, most of the waves are reflected or refracted. Light whose wave vibrations are on the same plane as the axis of the crystal, however, are adsorbed and passed by the crystal.

As light passes through the crystal, however, the light's intensity is reduced.

Figure 6. Incidental Light and Liquid Crystals' Polarizing Properties



After the filtered and diminished light has passed through the first crystal, it reaches the second crystal, where the process is repeated. The only light passed by the second crystal is that light whose waves are on the same plane as the second crystal's axis.

3.3 LCD Technology

LCD technology combines the ability of liquid crystals to polarize light with the capability of an electric field to manipulate the crystals to pass or block that light. This section of the paper examines the basic technology of liquid-crystal displays.

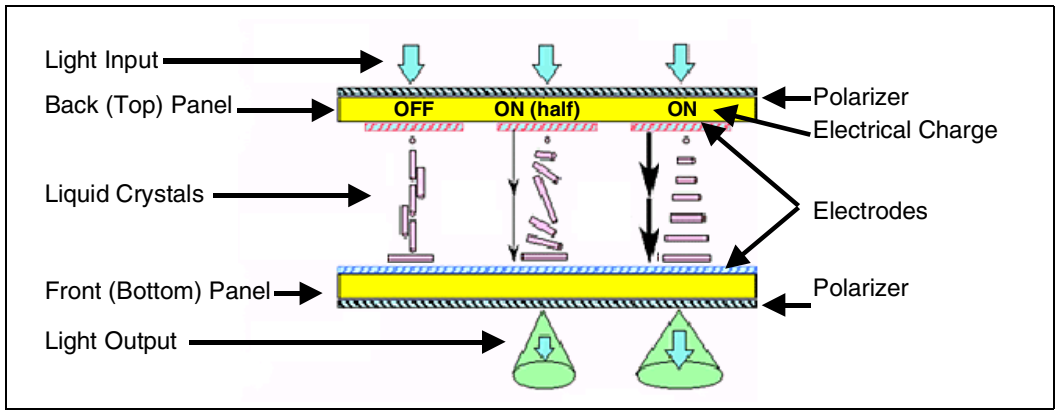
This section's main topics include:

- "Basic Technology" on page 12
- "Basic Components of Contemporary LCDs" on page 15
- "Passive-Technology LCDs" on page 16
- "Active-Technology LCDs" on page 21
- "Comparing Passive and Active Technologies" on page 22

3.3.1 Basic Technology

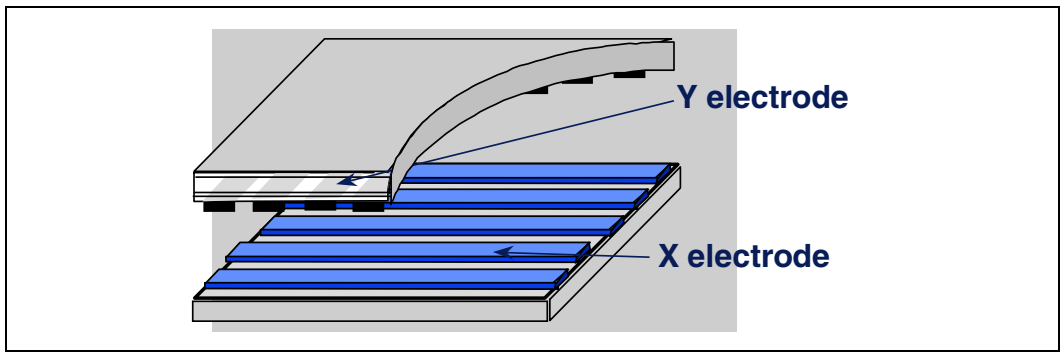
As explained earlier, an LCD passes light when its liquid crystals are aligned. By applying different voltages across the liquid-crystal compound, the LCD can affect the amount of light that is passed. The stronger the electrical charge, the more the crystals are aligned and the less light is passed by the LCD. (See Figure 7.)

Figure 7. Liquid Crystals' Effects on the Polarization and Intensity of Light



To increase the liquid crystals' control over what is displayed by the LCD, polarizing filters are placed at the back and front of the flat-panel device. The panels are put 90 degrees out of alignment with each other so that it is impossible for light to pass, unless the liquid crystals twist the path of the light.

Figure 8. Passive-LCD Matrix Cell Creation



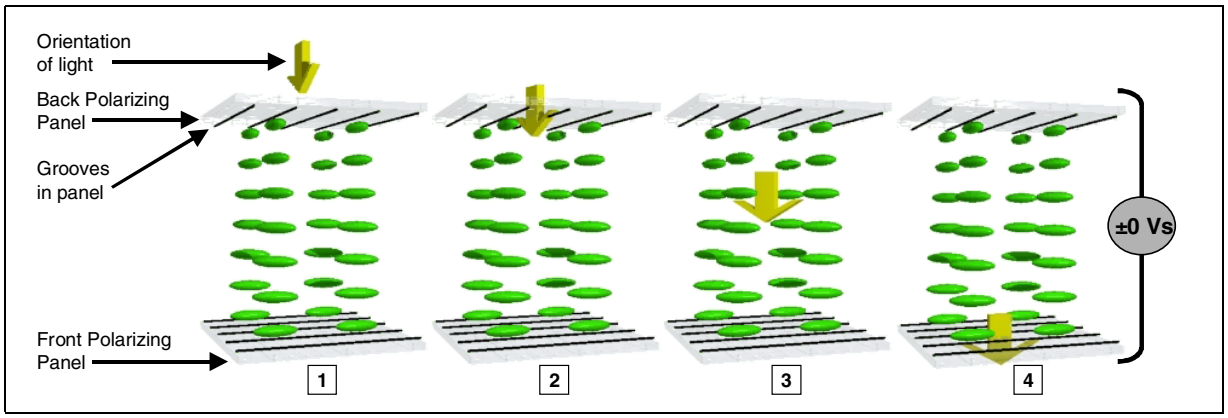
The LCD's electrical field is applied through a grid of horizontal electrodes and vertical electrodes, as shown in Figure 8. Figure 11 shows how the electrodes and other components make up a contemporary LCD panel.

Because the back (top layer) and front (bottom) lens' are 90 degrees out of phase — as shown by the black lines in the Figure 9 — light entering the top layer (in the figure's first frame) becomes polarized (in frame 2) as it enters the first crystalline structure.

Through birefringence, the light gets reflected out and into the crystals directly adjacent to the first crystal and the light is passed down the twisted chain of crystals to the crystal at the front of the LCD (as shown in frame 3 of Figure 9).

When the light comes out of the front crystal (as shown in frame 4 of Figure 9), it has been twisted 90 degrees from the angle it had when it entered the first liquid crystal. Since the front polarizing lens is at 90 degrees, the light passes through. To the observer, the cell is "on" or clear.

Figure 9. Electrical Field Aligning Liquid Crystals



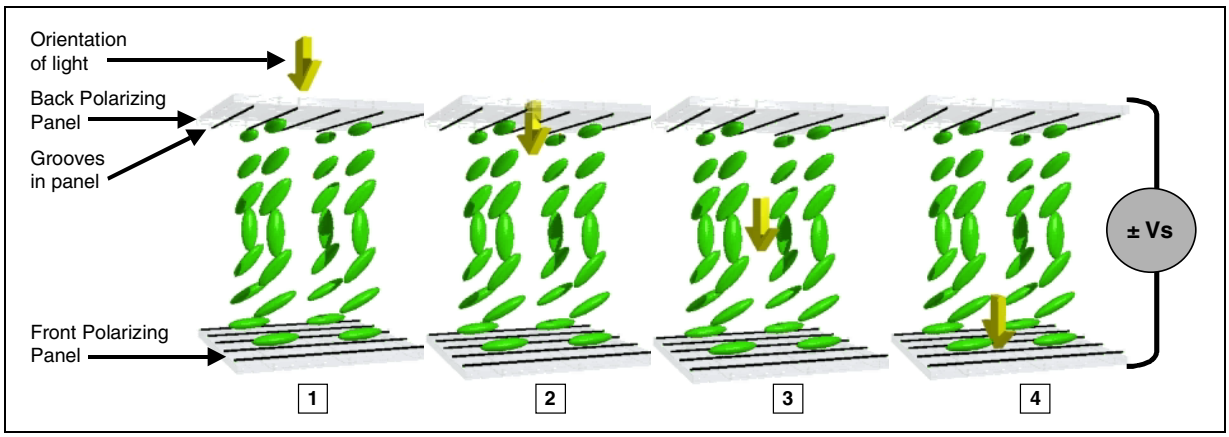
When the light gets to the front (bottom layer) of the twisted structure, it has twisted 90 degrees to align with the polarized panel on the front of the LCD. The light coming out of this panel is seen by the user.

When an electric field is applied across the electrodes in the back (top) and front (bottom) panels, the crystals go out of alignment and light can't pass through. (See Figure 10.) This is because the crystals are untwisted, out of alignment with the other crystals, so light reaching the front (bottom), panel is stopped.

The light coming in, from the back polarizing lens, is at 0 degrees and goes into the first crystal. The next crystal in the structure isn't aligned very well to the first crystal due to the electric charge, and so little light passes from the first crystal to the next. As this process repeats itself, down the crystal chain, it stops at some point. That is because the crystals are not twisted — and, therefore, the crystals are not aligned with each other — so light can not pass from one crystal to another.

The light essentially is not twisted, stays at 0 degrees. If any light does get to the bottom layer, it doesn't get through because the front polarizing lens is at 90 degrees.

Figure 10. Electrical Field Making Liquid Crystals Out of Alignment

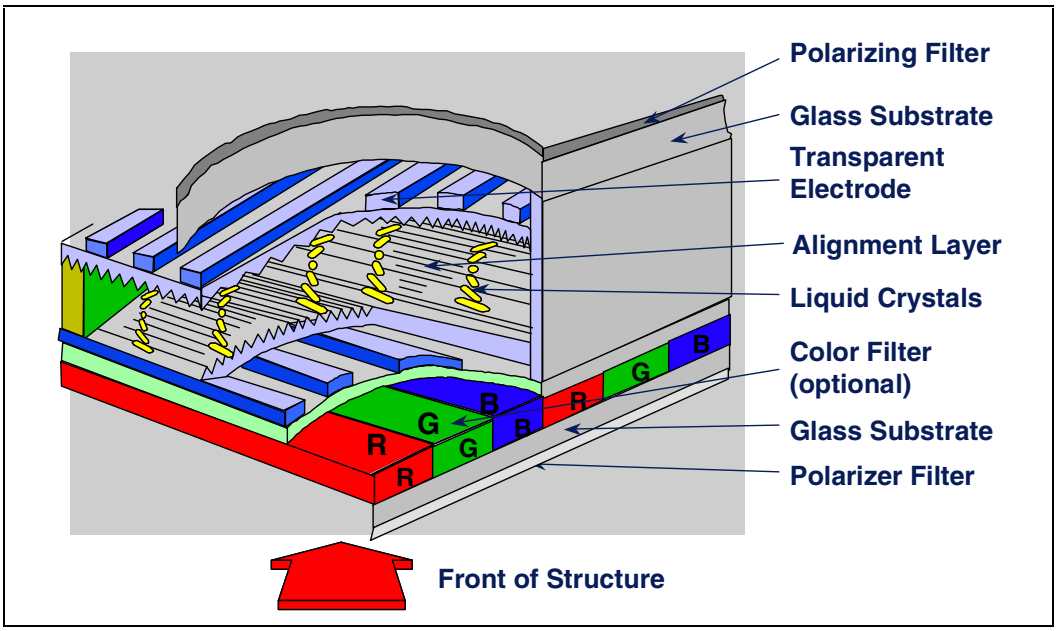


The LCD display needs a strong light source behind it because half of the incidental light is blocked by the back and front polarizing panels. This is what produces the low-contrast image experienced with many passive and active LCD technologies.

Instead of using back-lighting, an LCD can use a mirror to reflect the light that enters the front of the flat panel. Where the LCD's crystals are untwisted, light would not be reflected through the two polarizing layers. This mirror method is a power-saving feature used by some low-cost, low-power LCD displays.

Note: Some LCD designs work the opposite way, the crystals being untwisted in the normal state, blocking light from passing through the liquid-crystal solution. When voltage is applied across the plates of such a design, the crystals twist to align and pass light. It also is important to note that some designs twist the crystals more than 90 degrees. Some designs have a 270-degree twist, which gives a sharper turn on / turn off transition when voltage is applied.

Figure 11. Contemporary LCD Panel: Basic Components Materials



In the construction of LCDs, the size of the electrode mesh varies between color and monochrome FPDs. For *monochrome* LCDs, the intersection of each grid is a single pixel — or a point of illumination — on the front of the monitor. In *color* LCDs, each intersection of electrodes forms a *subpixel* — with red, green, and blue (RGB) subpixels forming each pixel on the LCD. An optional color filter can be used to enhance the RGB properties. Each color subpixel is called a "cell."

3.3.2 Basic Components of Contemporary LCDs

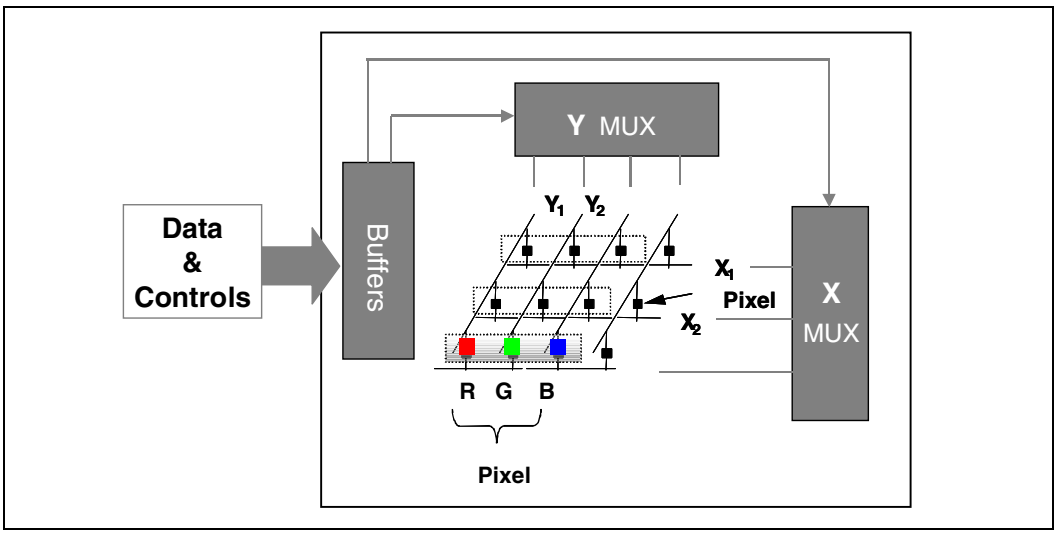
The components of a contemporary LCD panel — as shown in Figure 11 on page 15 — are listed below, from top to bottom (or, from the user's perspective, from back to front):

- Polarizing filter — The filter at the back of the LCD that polarizes the light passing through it to zero degrees. This puts the light out of alignment with the other polarizing layer, not allowing light to pass through unless the crystals can twist the light.
- Glass substrate — The glass that holds the LCD's layers together and gives rigidity to the display.
- Transparent electrode — The back electrode that holds part of the charge that is used to twist the liquid crystals.

- Alignment layer — The grooved layer(s) used to manipulate the liquid crystals. On the standard LCD, there are alignment layers — one at the back and the other at the front of the display. The grooves in the layers are 90 degrees out of align, which causes the crystals to naturally twist.
- Liquid crystal — The crystalline layer that makes the LCD work.
- Color filter (optional) — The filters used to make a pixel for *color* displays. These filters are not required for non-color LCDs.
- Glass substrate — The second glass layer for adding rigidity to the LCD.
- Polarizing filter — The second filter, at the front of the LCD, that polarizes the light passing through it to 90 degrees.

These components are basically the same for the two current types of LCDs: "passive" and "active." Passive technologies resemble the basic functionality just discussed. Active LCDs introduce other technological interventions to more precisely control the crystals and the pixels they illuminate on the LCD's front panel.

Figure 12. Basic Electronics in a Passive-LCD Display



Additional components include the input data, control signals, buffers, row (X MUX) multiplexers, and column (Y MUX) multiplexers.

The data and controls signals are coming from a graphics engine that will be discussed later in "Intel's Graphics Engine" on page 23. These signals are sent to a buffer section, which divide the data into two different sections, the column data and row data. At this point all the data is synchronized to allow the information to be displayed in the LCD panel. The X and Y multiplexers are responsible to select a particular pixel in the display.

3.3.3 Passive-Technology LCDs

There are two types of passive-technology LCDs. The first and most-common type is the Single-Scan Twist Nematic (SSTN). The second type is the Double-layer SuperTwst Nematic (DSTN) display.

3.3.3.1 Twist Nematic Technology

The Twist Nematic (TN) flat-panel display is a passive LCD that uses the grid of horizontal and vertical electrodes, previously described in this paper. (See Figure 8.) At the intersection of each grid is an LCD element that constitutes a single pixel, in a monochrome LCD, or a subpixel, in a color LCD. Each of these pixels or subpixels let light through or block it.

Figure 13. Electrical Characteristics of STN Matrix-Cell Creation

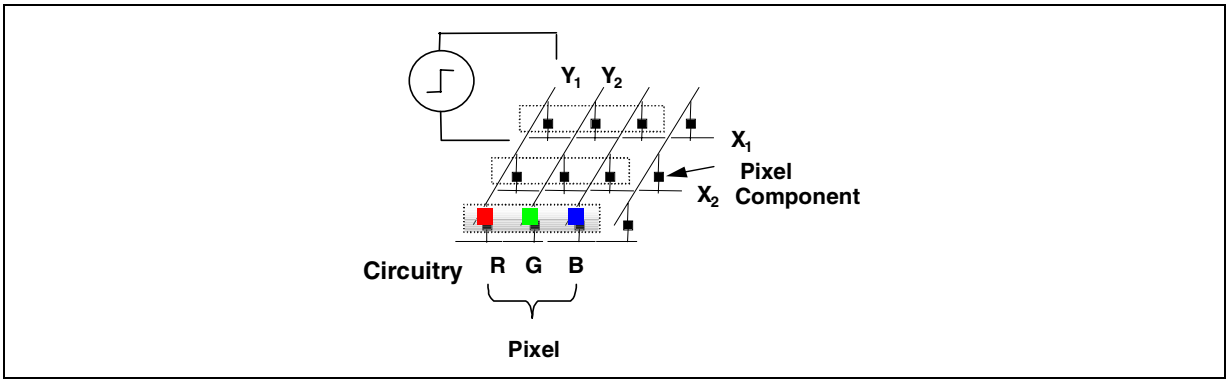
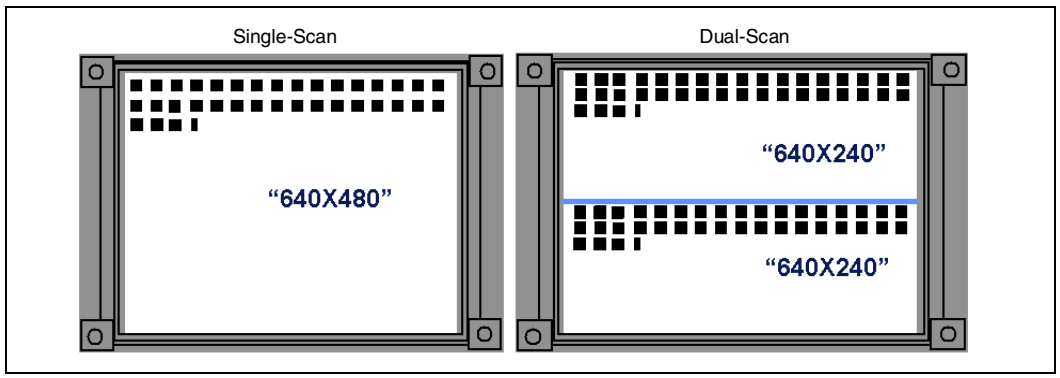


Figure 13 shows the electrical model for the LCD panel matrix. The figure's "Y_1, Y_2" labels represent the *column* electrodes and the "X_1, X_2" labels represent the *row* electrodes. Every intersection of a column and row make a pixel component (subpixel) in a color LCD or a pixel in a monochrome LCD. When voltage is applied to a specific configuration of column and rows, the particular pixel component (Y_1X_1, Y_2X_1, etc.) behaves as a capacitor, passive electrical component.

3.3.3.2 Single-Scan and Dual-Scan Twist Nematic Displays

The Twist Nematic (TN) display matrix requires an organized architecture to facilitate communication between the graphics engine and the display. The market currently has two varieties of TN displays: single-scan and dual-scan.

Figure 14. Comparison of Single-Scan and Dual-Scan Displays



Single-scan (or SSTN) devices display the pixel information from left to right and top to bottom. Pixel 1 is in the top, left corner of the display and the last pixel in the bottom, right corner.

The display's progressive-scan motion sequentially sends all the pixel information in the first row, from left to right. All subsequent rows are sequentially scanned, one at a time, from top to bottom, until the last row is completed. After the display's last pixel receives its information, the process starts over again. This process is called frame creation.

In single-scan technology, a display frame is created with one pixel being written at a given time by multiplexed logic. This method, however, also had a problem in higher-resolution displays. By the time that the last pixel of a frame is being displayed — in the bottom, right corner of the display — the information of the frame's first pixel — in the top, left corner — was starting to drift from their original position or losing the color information.

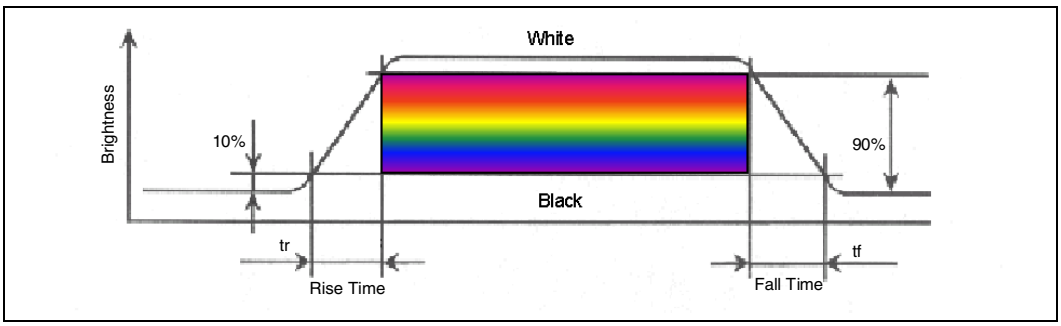
This drifting problem was due to the floating electrical state of the pixels after being written, using a relatively simple electronics. (See Figure 14.) If there is no more voltage change, after a liquid crystal is twisted, the crystal will try to go back to equilibrium, which is its initial position.

This problem with both types of Twist Nematic displays — single- and double-scan — is most noticeable in higher-resolution displays, such as Super Video Graphics Array (SVGA).

Dual-scan (DSTN) displays were developed to reduce the drifting problems with high-resolution displays. The technology does this by dividing the display area into two sub-displays and writing two pixels — one in each of the sub-displays — at a given time. (See Figure 14.)

In early SSTN technology and present DSTN technology, another problem arose. As shown in the Figure 15, the major issue was the display's slow response time. For demanding applications such as high-quality movie videos, Twist Nematic displays were found to be unsuitable.

Figure 15. Optical Time Response of a Selected DSTN Flat-Panel Display



A selected DSTN flat-panel display (Figure 15) has a rise time of 170 ms. High-quality movie videos have display speeds of 30 frames per second which requires a display response time of 33.3 ms — about one-fifth the time of the DSTN's response time.

Note: DSTN flat-panels remain viable, however, for applications where fast response times are not required. In such instances, DSTN displays actually are *preferred* because of the significantly higher costs of active-technology displays.

3.3.3.3 Double-Layer SuperTwist Nematic Technology

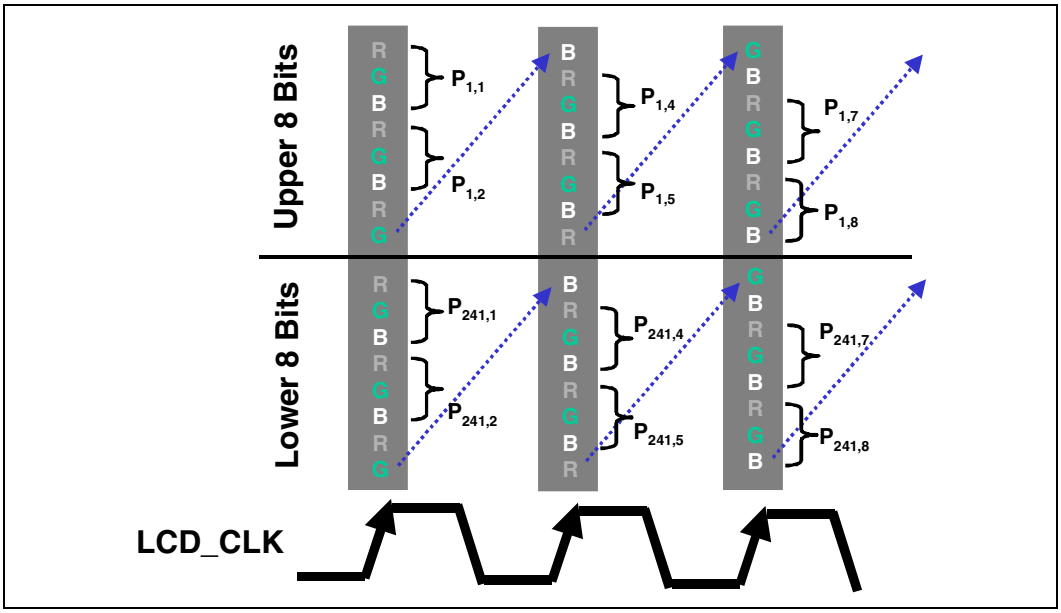
The dual-scan display's problem with the pixels' floating electrical state led to the development of Double-layer SuperTwist Nematic (DSTN) displays. This technology supports higher-resolution formats by dividing the display into segments. That reduces the time required to create the frame, as there are fewer pixels in each segment.

This solution, however, creates a problem for the graphics engine: External memory (RAM) is needed by the graphic engine to act as a virtual display. This approach was used to achieve the same system performance as a standard, cathode-ray tube (CRT) display — without changing the graphics engine.

The need for external memory could have been averted easily by changing the existing architecture of the graphic engine, but that would make existing hardware obsolete. To support legacy systems, a solution was sought outside the graphic engine.

Figure 16 shows the interface between a graphics engine and the passive DSTN LCD. In this case, all the signals are synchronized to a signal called LCD_CLK. Some manufacturer's LCDs, divide this signal into two signals: HSYNC and VSYNC.

Figure 16. DSTN LCD Timing



The upper eight bits of this interface provide the information for the first half of the display. The first clock cycle of LCD_CLK provides complete information for the first two pixels of the display and partial information for the third pixel. In the second clock cycle, the rest of the third pixel's information is provided, along with complete information for pixels 4 and 5, and partial information for pixel 6. In the third clock cycle, the rest of pixel 6's information is provided and complete information for pixels 7 and 8.

In this example, it takes three complete LCD_CLK cycle to transfer eight bits of information in the same row, $P_{1,1}$; $P_{1,2}$; $P_{1,3}$; $P_{1,4}$; $P_{1,5}$; $P_{1,6}$; $P_{1,7}$; $P_{1,8}$; etc. This is called a "progressive sequential scan." The same process is repeated for the lower part of the display, using the lower eight bits of information. The two scans are done simultaneously, $P_{241,1}$; $P_{241,2}$; etc.

This particular display has 480 rows and 640 columns. The common resolution of this display is 640 x 480 pixels, the VGA standard. Once the last pixel information of the display is transferred, the process starts over again with the first pixel. This loop in the process is called the "refresh time" or "frame creation."

Now, the information that the graphics engine provides for each pixel and the refresh time are the perfect combination that Frame Rate Modulation takes advantage.

3.3.3.3.1 Frame Rate Modulation, Dithering, and Video RAM

The solution to the external-RAM problem was solved with the development of Frame Rate Modulation (FRM) circuitry which takes the display data from the RAM and transports it to the monitor. This technology also enhances the gray scale and color painting of Twist Nematic displays.

The color information of a monitor consists of red, green, and blue components (RGB) for each pixel. In DSTN displays, this information comes from the main memory — with one byte each for red, green, and blue — and is saved in external, video RAM. Using video RAM enables the CPU to do other things while the specialized video RAM is optimized for converting the color information into signals that will be understood by the monitor.

This process creates a color palette following the equation $2^{(8 \text{ bits x } 3 \text{ RGB})}$ or 16 million colors. The amount of external memory required to support a VGA resolution display is almost 1 Mbytes. In order to support SVGA resolution, the display requires almost 1.5 Mbytes of RAM. (See Table 1.)

Table 1. Display Modes, Resolutions, and Memory Requirements

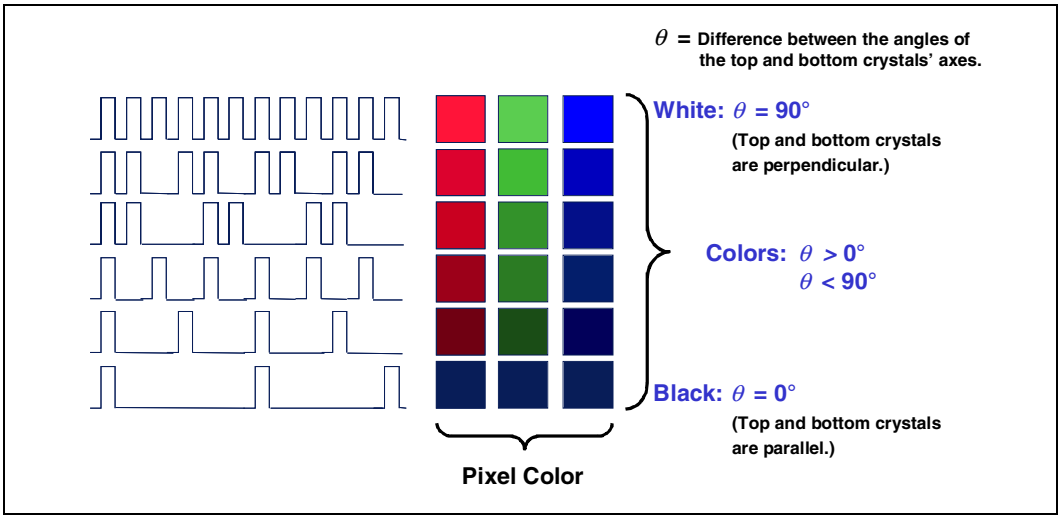
Mode	Resolution	Required Memory	Comments
VGA	640 X 480	922 Kbytes	RGB – 3 bytes
SVGA	800 X 600	1.44 Mbytes	RGB – 3 bytes
XGA	1,024 X 768	2.36 Mbytes	RGB – 3 bytes
SXGA	1,280 X 1,024	3.94 Mbytes	RGB – 3 bytes

Note: While the graphic engine is designed to support this level of screen resolution, not every flat-panel display can.

As discussed earlier, Frame Rate Modulation (FRM) is used to move display information from the "virtual display" of the video RAM to the actual display. FRM receives this input and converts it into a train of pulses that are transported to each display pixel at a rate known as the refresh frequency.

The train of pulses, generated by the FRM, is responsible for each pixel's color. (See Figure 17.)

Figure 17. Frame-Rate Modulation Functionality



To create and maintain a dark red color, a pixel's red component must be excited on every cycle of the refresh frequency. This requires that the shutter be open completely, to allow the light source across the pixel to be observed.

For a lighter shade of red, the graphic engine misses cycles of the refresh frequency, allowing the shutter to be open, but not completely. This same process is used with the green and blue components of each pixel. Together, the red, green, and blue components — and their various shades — produce the complete color palette for each pixel.

The human eye observes the color of white when the red, green, and blue components of the pixel are completely open. The eye sees black when all three components are close. In this second case, no light is passing through the liquid crystals that define the black pixel(s).

Dithering is another method of generating grayscale. This method uses multiple pixels in a specific display region to create a spatial arrangement of completely open or completely close pixels. This reduces the use of FRM circuitry. Instead of pulsing each pixel in the specific region, the vital pixels are pulsed and the rest are completely off, with no pulses needed.

3.3.4 Active-Technology LCDs

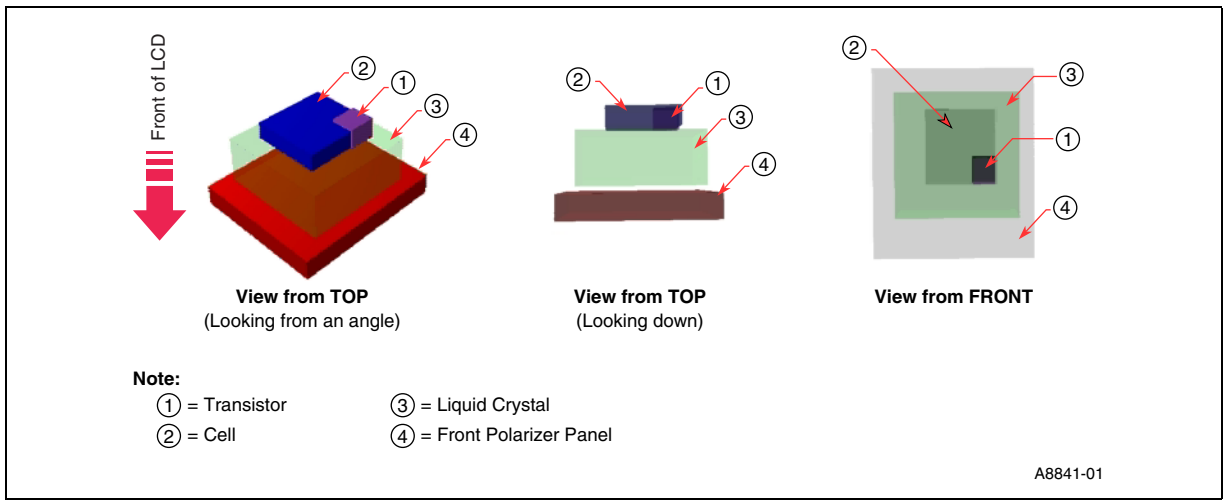
"Active" or "active-matrix" LCDs represent the newer and more powerful type of LCD technology. This section examines the active technology's Thin Film Transistor (TFT) monitor and how it can be interfaced with the Intel® 810 Chipset.

3.3.4.1 Thin Film Transistor Technology

The Thin Film Transistor LCD cell is similar to the previously discussed DSTN LCD cell. The major difference is that a thin, film transistor has been added in one corner to give the system more precise control of the voltage across the electrodes. (See Figure 18.)

The TFT panel is called an active display because of the individual transistors added to each cell.

Figure 18. Thin Film Transistor Technology



Referring to Figure 18, the thin, film transistor controls the voltage across the top and bottom electrodes. This voltage turns the LCD cell on or off.

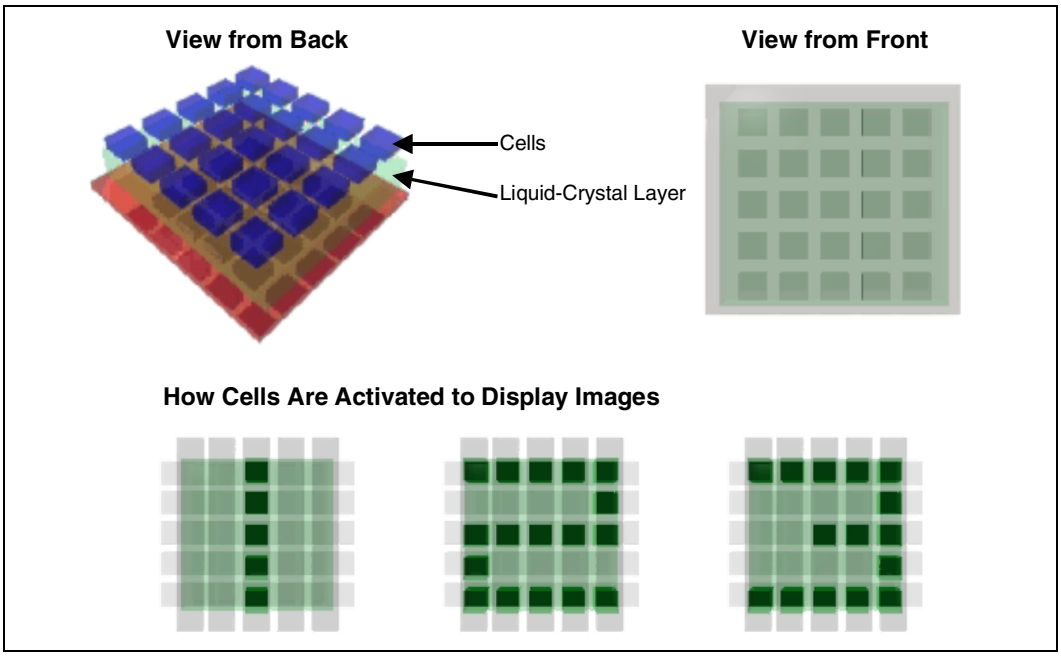
The figure's last frame shows how the cell appears from the front, with the cell turned on and the crystals aligned. Notice the thin, film transistor in the bottom, right corner, blocking a small section of the cell. This is a problem with TFT displays — the thin transistor, though mostly clear, blocking a little of the light coming through the LCD.

Similarly to DSTN LCD monitors, TFT cells are grouped to make an array that can be used to display characters and pixels. The wires needed to control the individual transistors run down the columns and rows of the screen, adding a small dark frame to each subpixel.

Unlike DSTN displays, however, TFT displays isolate each cell, preventing voltage bleeding. The better voltage control also enables the TFT technology to have stronger crystal alignments, producing a higher-contrast display.

The LCD's matrix is the display. The combination of the LCD and the graphics engine — to be discussed later in the paper — is what the human eye captures in any application that needs a display. Figure 19 shows one of the many possible applications. Characters display in this example take a matrix of five columns and five rows to represent the numerals 1, 2, and 3.

Figure 19. Active LCD Matrix Implementation



3.3.5 Comparing Passive and Active Technologies

Having examined both the passive and active LCD technologies earlier in this section, the following discussion examines the advantages and disadvantages of each technology.

3.3.5.1 Passive Technologies: Advantages and Disadvantages

The passive, Twist Nematic (TN) technology has the advantages of being low-cost and easy to manufacture. The primary disadvantage of the technology is its inability to meet the requirements for high-quality video applications, such as DVD. This is due to the technology's slow display response times and other minor problems, such as voltage bleeding between pixels and a low-contrast display.

New TN techniques — such as Double-layer SuperTwist Nematic (DSTN), Frame Rate Modulation (FRM), dithering, and external video RAM — are addressing these problems and creating new alternatives to Intel's existing graphics engine. Most embedded-application engineers know which technology is favored by their embedded flat-panel market — DSTN or the active technology's Thin Film Transistor (TFT), discussed later in this paper.

These advantages make the DSTN technology appropriate for applications where high-speed video is not required. The DSTN FPD's problem with high-end video could be resolved by changing its architecture, but that would make existing products obsolete and violate the philosophy of legacy support.

3.3.5.2 Active Technologies: Advantages and Disadvantages

Active-technology, Thin Film Transistor (TFT) LCDs meet the demands of the high-end video market, but that capability comes with a cost.

TFT displays have the advantage of higher performance than DSTN LCDs — due to the faster switching capabilities of the individual TFT's LCD cells. TFTs also use the graphics engine already inside the Intel® 810 Chipsets — also making the TFT and DVO solution viable for future chipsets that use the DVO port.

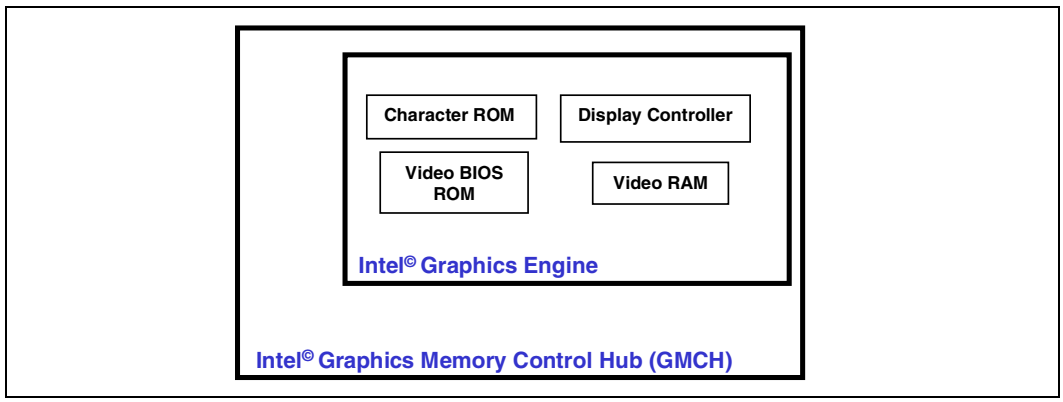
TFT displays, however, are more costly to produce — due to the transistor used for each subpixel.

4.0 Intel's Graphics Engine

To discuss how LCD technology can be interfaced with the Intel® 810 Chipset, we first must understand the Intel chipset and its internal Intel graphics engine.

Intel's graphics engine resembles most of today's PC-display controllers. (See Figure 20.)

Figure 20. PC Video Display's Basic Components



Like most video subsystems, the Intel graphics engine contains:

- **Video RAM** — Data storage whose information determines what is displayed on the screen.
- **Display controller** — The controller that reads the data from the video RAM and transports it to the display. For a DSTN FPD, the controller uses FRM and dithering techniques.

- **Bus connection** — The means by which data in the video RAM communicates with the CPU's memory address space and the video information is converted to assembly instructions.
- **Character ROM** — The ROM that contains data and pixel patterns that are used when the display controller is in the character-display mode.
- **Video BIOS ROM** — The ROM that contains the BIOS drivers and service routines used by applications accessing the display controller and video RAM.

The Intel® 810 Chipset is a high-integration chipset designed for basic graphics/multimedia PC platforms. The chipset consists of Graphics and Memory Controller Hub (GMCH) host bridge and an I/O controller hub (ICH/ICH0) bridge for the I/O subsystems. (See Figure 20.)

The chipset's GMCH integrates a system-memory, DRAM controller that supports a 64-bit (8-byte), 100-MHz DRAM array. The DRAM controller is optimized for maximum efficiency. It provides an interface to a progressive, single-scan monitor with a resolution of up to 1,600 by 1,200 pixels.

The chipset's Digital Video Output (DVO) interface connects to an external device to drive auto-detection for a non-scalar, flat-panel display with a resolution of up to 1,024 by 768 pixels. This output can be connected to a TV-out device or an LCD/flat-panel transmitter.

This shortcoming, for DSTN displays, is why Intel incorporated external RAM in the graphics-engine design, for the RAM to serve as a virtual display. DSTN support was not a requirement, when this powerful 2D and 3D graphic engine was designed.

Through utilization of a "virtual display" in the video RAM, the graphics engine thinks that it is writing to the display. Actually, the graphics engine — which only knows about its interface — is writing to a memory space that maps the display. (For a listing of the memory requirements, see Table 1 on page 20.)

Another display limitation of the Intel® 810 Chipset is its lack of scaleability. Scaling is important for applications that require changing the size of an object, displayed on the flat-panel display, while maintaining the object's shape and other properties. Most graphics software products, particularly vector-based applications, allow you to scale objects.

Scaling helps when the pixel resolution of the LCD is not equal to the resolution that the GMCH is driving. If an LCD has a resolution of 1,600 X 1,240 pixels, but the display is set to 1,024 x 768, hardware scaling would stretch the image to fill the screen at 1,600 x 1,240 pixels.

The Intel GMCH, however, does not support scaling. In the preceding example, an image with a 1,024 x 768 resolution would be displayed in the center of the LCD with a black border around the edges. There would be a 290-pixel border on the left and right (1,600 - 1,024 = 576; 576/2 = 290) and a 236-pixel border on the top and bottom (1,240 - 768 = 472; 472/2 = 236).

Additionally, scaleability is important if the display has to be changed or replaced, related to the end of life of the device or its operation environment. It's possible that the replacement display has higher or lower resolution than the original monitor. Scaling enables the new device to integrate with the pre-existing system, without changing the software application. DVO, as a graphics interface, does not support this feature.

As powerful as they are, Intel's graphics engines do not meet all of customer's present needs. The lack of support for DSTN and scaling are the main reasons why many system design engineers search out other solutions. Third-party solutions are cost-effective and provide DSTN and scaling support.

How does the platform know what type of display is connected? The platform uses the Extended Display Identification Data (EDID) standard explained in the following section.

4.1 Extended Display Identification Data (EDID) Standard

Most video adapters — and Intel's graphics engine — also subscribe to the Extended Display Identification Data (EDID) standard developed by Video Electronics Standards Association (VESA, www.vesa.org). This standard establishes a data format that contains basic information about a monitor and its capabilities, including vendor information, maximum image size, color characteristics, factory preset timings, frequency range limits, and character strings for the monitor's name and serial number.

This monitor information is stored in the display and used to communicate with the system through a Display Data Channel (DDC) that sits between the display and the PC's graphics adapter (Video BIOS ROM). The system uses the EDID data for configuration purposes, so the monitor and system can work together.

The latest version of EDID (1.3) can be used in cathode-ray-tube (CRT) displays, LCD displays, and future display types because EDID offers general descriptions of almost all display parameters.

5.0 Intel Implementations for LCDs

This section of the paper examines how to interface the Intel® 810 Chipset with the two LCD technologies. The topics include:

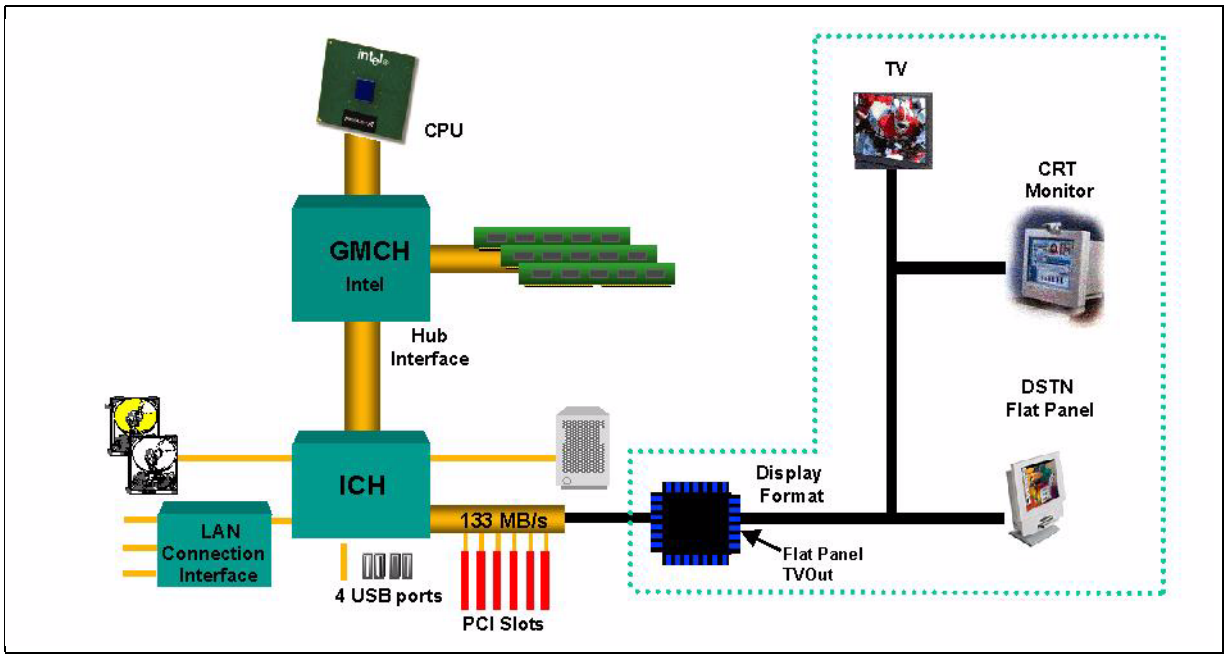
- "Interfacing Passive LCDs and the Intel® 810 Chipset" on page 25
- "Interfacing Active LCDs and the Intel® 810 Chipset" on page 29

5.1 Interfacing Passive LCDs and the Intel® 810 Chipset

Figure 21 shows how the Intel® 810 Chipset can be integrated into a system supporting a passive LCD, using the PCI bus.

The Intel® 810 Chipset has limitations for some video applications. The chipset requires that the application use the progressive, single-scan display mechanism. This creates a issue for DSTN displays because of that monitor's dual-scan technology.

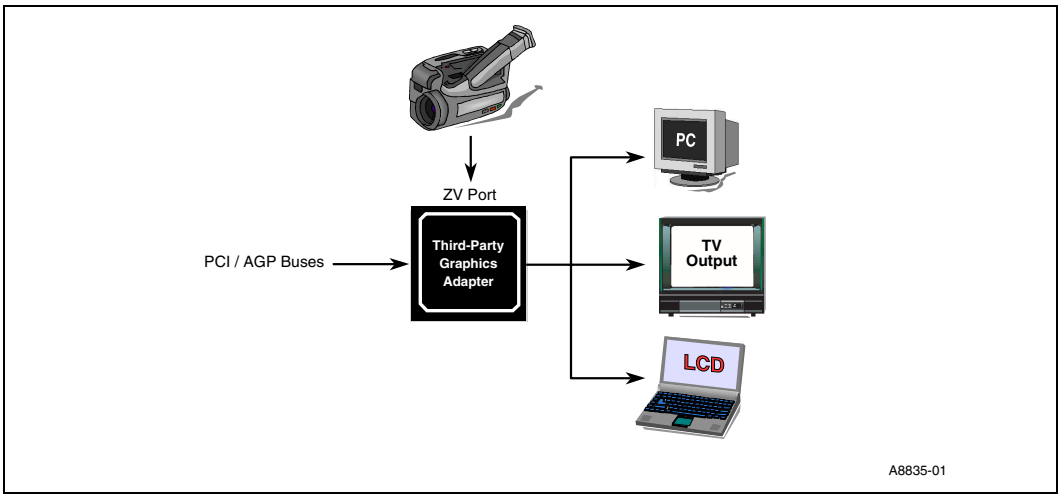
Figure 21. Third-Party Implementation to Support DSTN



5.1.1 Third-Party Solution

Several third-party graphics engines satisfy the high-end display requirements of market applications, such as video games and high-quality, high-speed movie video. (See Figure 22.) The performance of these third-party solutions is compatible with Intel's graphics engine.

Figure 22. Third-Party Graphics Subsystems and High-End Video Capabilities



The advantage of purchasing Intel chipsets is that the graphics engine is included in the chipset design. This frees up board space and eliminates additional cost by not adding external graphics components to the design.

For the smaller display market — that does not demand high-quality, high-speed video — the Intel engine still is a contender, with the addition of some minor components for interfacing with the flat-panel display. A third-party circuit is needed, however, for the engine to interface with the display.

In considering third-party solutions, the Lynx EM+* from Silicon Motion is a cost-effective option. The Lynx EM+ includes 2 Mbytes or 4 Mbytes of video memory within a single footprint. It provides a complete video subsystem that consumes very little power. (The board's block diagram is given in Figure 22.)

The Lynx EM+ also offers enhanced capabilities for dual view and dual applications. The board can simultaneously drive LCD/CRT or LCD/TV display combinations with each display independently supported for full-screen, full-motion video and independent graphics refresh rates, resolutions, and color depths.

A typical use of this capability is a PC-based slide presentation that displays slides to the audience, on a TV/CRT screen, while showing speaker notes to the presenter, on the PC's monitor.

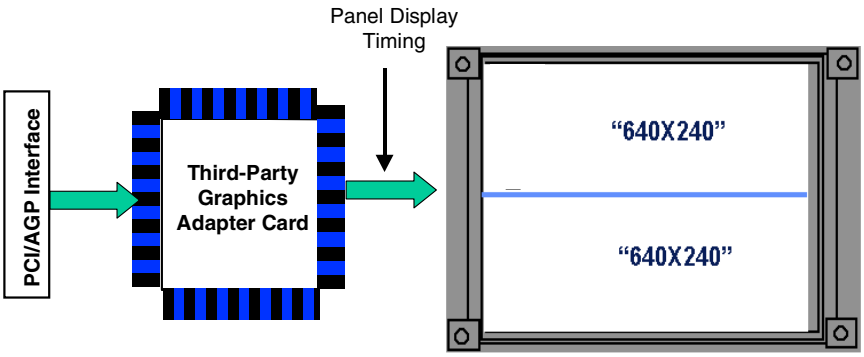
The board's host-interface unit is PCI 2.1 compliant and supports bus-mastering. Other features include a VGA core, an LCD back-end controller, and 135-MHz RAMDAC. Each video window motion uses hardware for scaling, color interpolation, and conversion of the signal from the YUV (YCrCb) color video standard format to the RGB (Red, Green, Blue) format.

When combined with dual-displays support, this third-party solution can output video streams to separate display devices, and bilinearally scale them, to support applications such as full-screen display of local and remote images for video conferencing. The Lynx EM+ also has a robust, two-dimensional drawing engine.

Clearly, the Lynx EM+ is a powerful option, when looking for support of DSTN monitors, Thin Film Transistor displays, and scaling technology. With low-performance LCDs, such as DSTN, powerful 3D graphics engines are optional. Alternately, if DSTN-display and scaling are *not* required, an Intel chipset is the best choice.

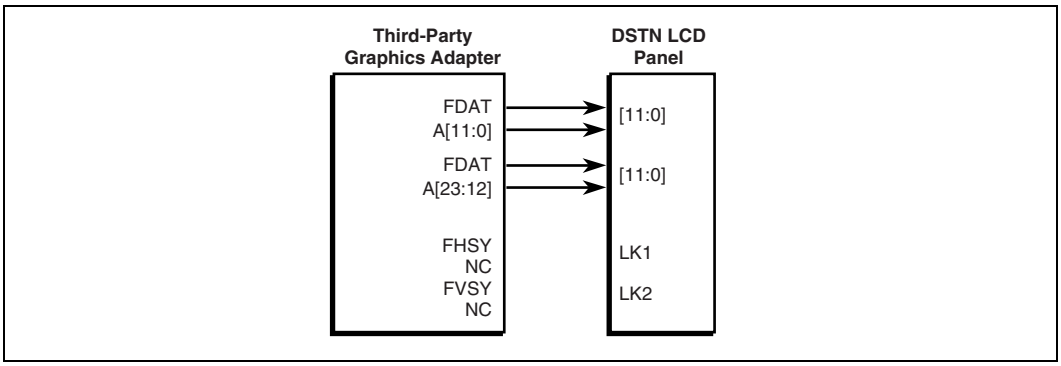
When DSTN support is required and the flat-panel display (FPD) is located close to the system board, the Lynx EM+ is the right choice. That's because the third-party board provides an output port that interfaces directly to the CMOS-interfaced FPD. (See Figure 23 and Figure 24.)

Figure 23. Passive LCD Located Close to the System Board



Note: For an example of panel display timing, see Figure 16.

Figure 24. Passive LCD Located Close to the System Board: Block Diagram



When the FPD is *not* located close to the system board, the Lynx EM+'s same output port can be configured to transport the information to an affordable transmitter/receiver pair. (See Figure 25 and Figure 26.)

Figure 25. Passive LCD with Transmitter/Receiver Pair

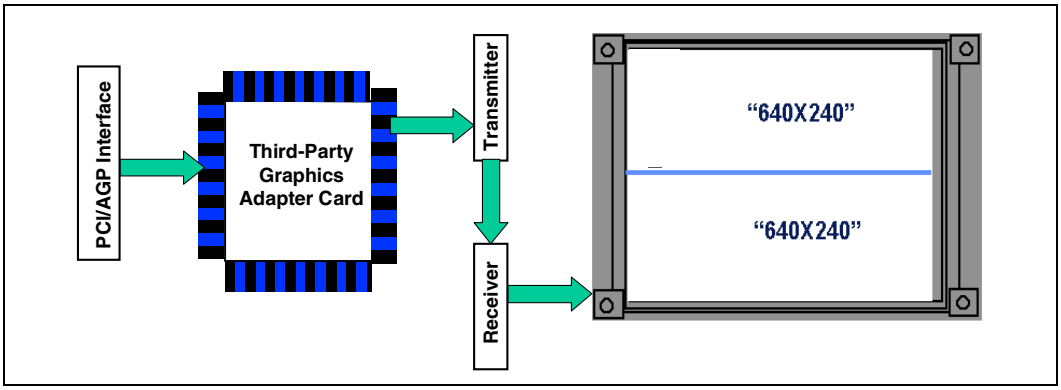
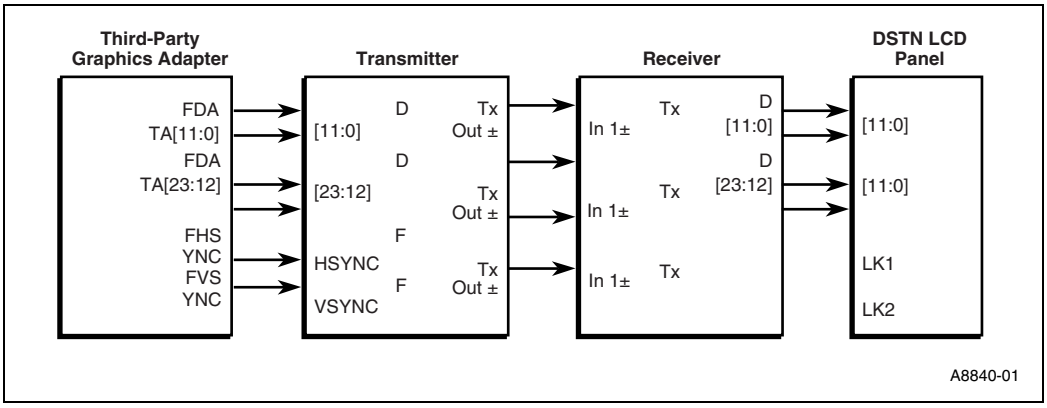


Figure 26. Passive LCD with Transmitter/Receiver Pair: Block Diagram



Lynx EM+ also supports the Low-Voltage Differential-Signaling (LVDS) interface, which some FPDs have. In such instances, only one change would be needed to the block diagram in Figure 26. That change would replace the transmitter/receiver pair with a LVDS transmitter/receiver pair.

Lynx EM+ is a solution to a much bigger market than the one being considered by this paper. Perhaps, developing opportunities to solve every potential customer problem is the existence of Intel's products and third party products as well. The only conditions not satisfied by the Intel® 810 Chipset, for this smaller display market is DSTN and scaling support.

Note: While the subject of this paper is interfacing the Intel® 810 Chipset with LCDs, it should be noted that the Intel® 815 Chipset also can be interfaced with third-party graphics subsystems. The Intel® 815 Chipset has the advantage of being able to interface off the Accelerated Graphics Port (AGP) as well as the PCI bus, as the Intel® 810 Chipset can.

5.2 Interfacing Active LCDs and the Intel® 810 Chipset

In interfacing the Intel® 810 Chipset with active LCDs, there are several issues to consider. Those issues are discussed in the following topics:

- Intel® 810 Chipset DVO to the DVI Transmitter
- From the DVI Transmitter to the DVI Receiver
- From the DVI Receiver to the Flat Panel

Figure 27 gives the block diagram of an embedded Intel system with TFT support. The Intel graphics engine drives the data from the Digital Video Out (DVO) port to the transmitter chip, where the information is communicated to the receiver chip and then the flat-panel display.

The difference between the TFT and DSTN block diagrams is that the DSTN architecture requires a third-party graphics subsystem which is connected from a PCI slot.

Figure 27. Intel® 810 Chipset-to-Thin Film Transistor Block Diagram

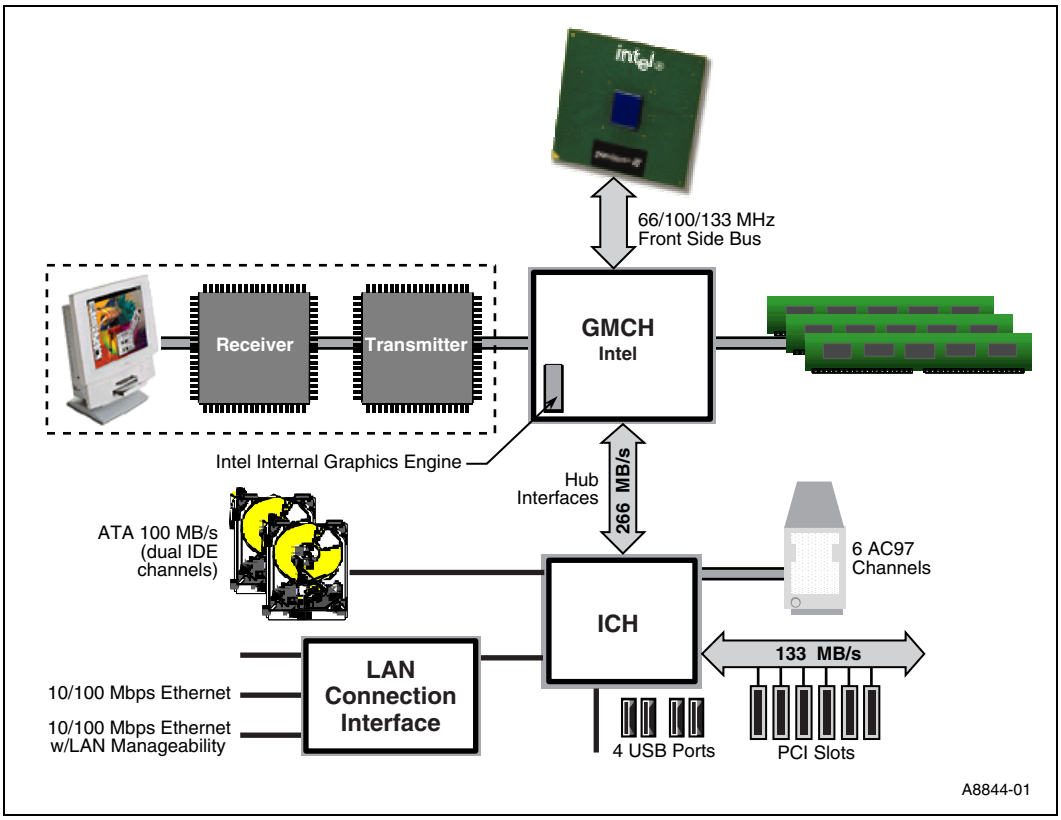
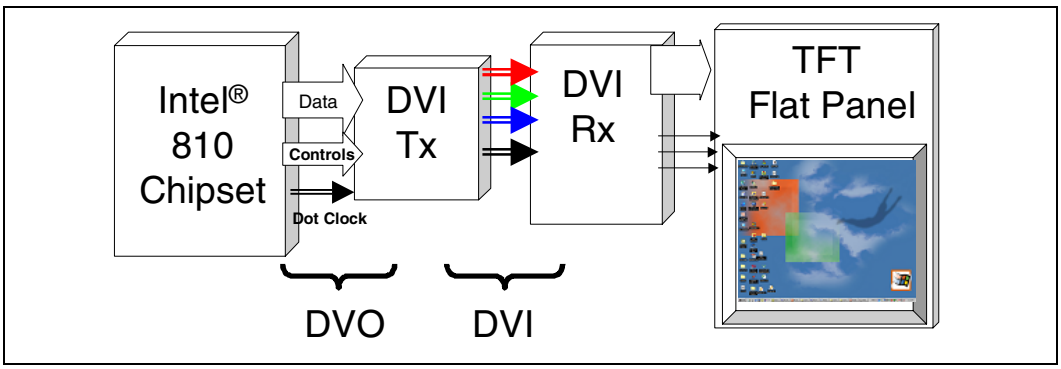


Figure 28 shows the block diagram of the transmission from the DVO port, on the Intel® 810 Chipset, to the TFT flat panel. The Digital Visual Interface (DVI) port interfaces between the transmitter chip and the receiver chip.

Figure 28. DVO Port-to-Intel® 810 Chipset Block Diagram



Until recently, only the transmitter and receiver chips were available for interfacing the Digital Video Out (DVO) port and the TFT panel. Since this document was published, however, other companies have produced combination chips that combine the transmitter and receiver in one unit.

Combination chips eliminate the need for separate components, but they may run into difficulty with display connections.

In a two-chip system such as that in Figure 27, the transmitter chip would be located physically on the system board and the receiver chip would be located on the flat panel display. A long cable could be used as the DVI interface, so that the display could be located a distance away from the system. (The allowable distance, between the chip and the monitor, would be determined by the technical specifications of the transmitter and receiver.)

With a combined chip, however, the display would have to be very close to the system, as with a laptop PC, where the LCD flat panel is mounted to the system board and is located a very short distance away from the platform.

Digital video information is transmitted out of the Intel® 810 Chipset's graphics control hub as DVO data. That data is converted by the transmitter into four differential pair signals sent to the receiver over the DVI bus. The receiver takes the four differential pair signals and converts them into the clocking signals and eight red bits, eight green bits, and eight blue bits.

As shown in Figure 28, the data coming out of the Intel® 810 Chipset and going into the Digital Video Interface (DVI) transmitter is in the Digital Video Out (DVO) format. The data coming out of the DVI transmitter and going into the DVI receiver is in the DVI format.

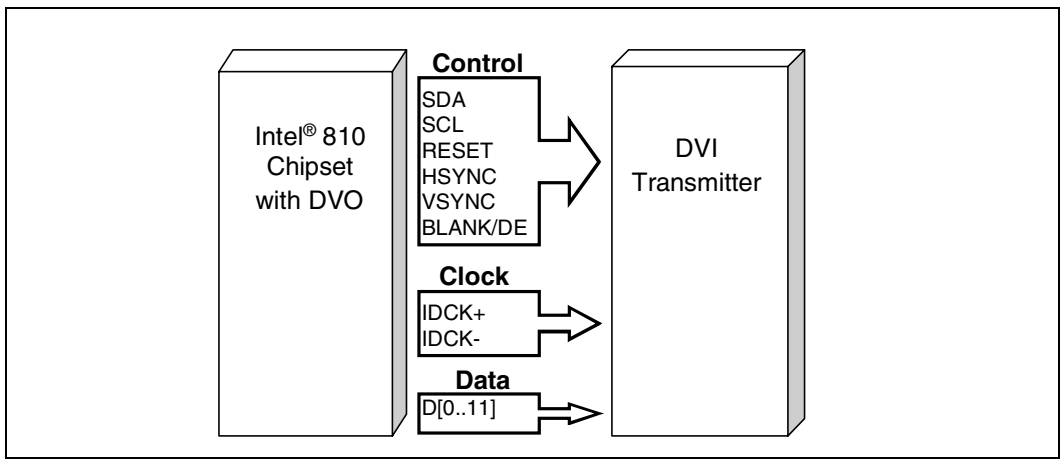
5.2.1 Intel® 810 Chipset DVO to the DVI Transmitter

Digital video information comes out of the Intel® 810 Chipset as Digital Video Out (DVO) information. Figure 29 is a block diagram of the signals passed to the Digital Video Interface (DVI) transmitter from the DVO port of the chipset.

There are 12 data lines, a differential pair clock, and a blank line, that gets translated to the Data Enable (DE) line of the transmitter. There also are vertical synchronization (Vsync) and horizontal synchronization (Hsync) signals that are connected to their corresponding lines on the transmitter.

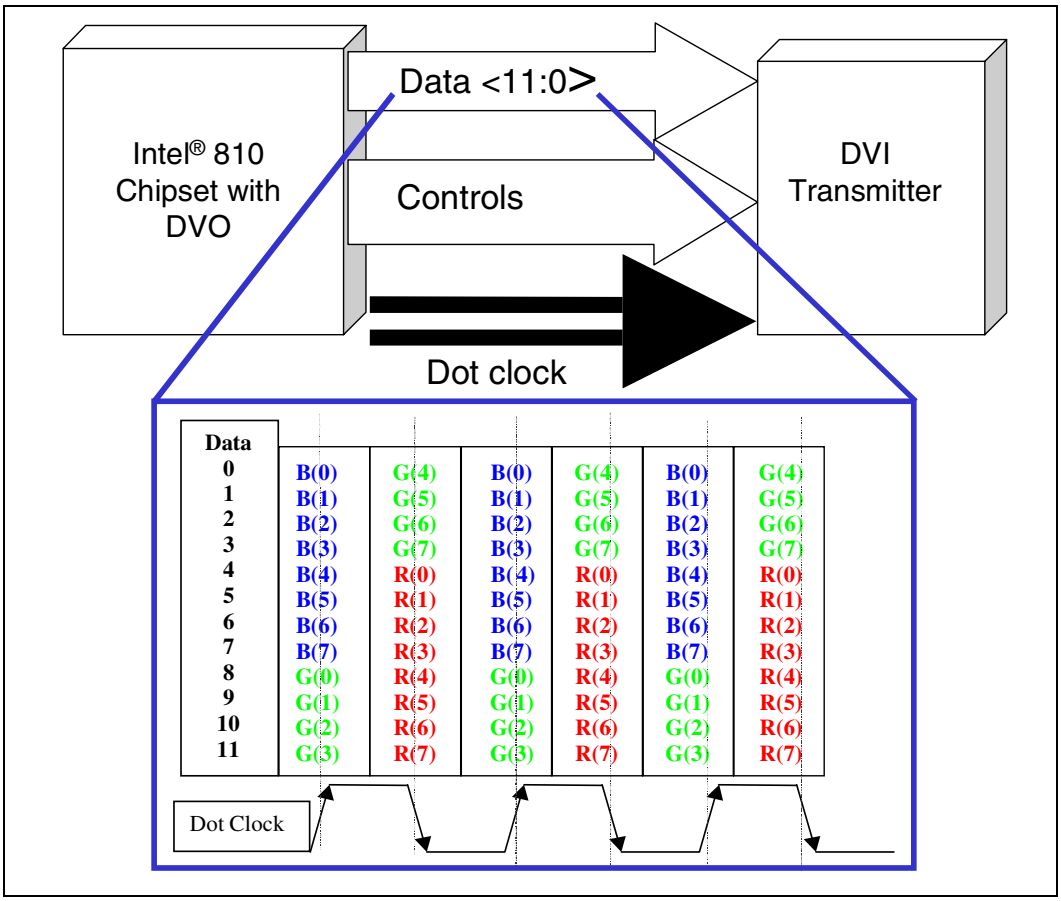
The System Management Bus' System Clock Line (SCL) and System Data Line (SDA) signals are I^2C (EDID) control lines that enable the Intel® 810 Chipset to use low-speed signals to communicate with the DVI transmitter, for setting up configuration registers in the DVI transmitter to work with the Intel chipset.

Figure 29. DVO-Port Transmission Block Diagram



DVO information is transferred to the DVI transmitter by double-pumping the 24 bits of information (3 pixels x 8 bits = 24 bits) over the 12-bit bus on every clock edge. Figure 30 shows how this is done.

Figure 30. Transmission of DVO Data



For the first rising edge of the clock, all eight blue data bits for the first pixel are transmitted on the first eight pins of the DVO bus, DVO[8:0]. The first half of the eight green pixels are transmitted on the last four pins of the DVO bus, DVO[12:9].

During the first falling edge of the clock signal, the second half of the green pixel data is transmitted on the first four pins of the DVO bus, DVO[3:0], and the red color bits for the pixel is transmitted on the last eight pins of the DVO bus, DVO[11:4].

5.2.2 From the DVI Transmitter to the DVI Receiver

The Digital Video Interface (DVI) specification provides a high-speed digital connection for visual data types that is independent of display technology. The specification meets the needs of all segments of the PC industry (such as workstations, desktops, and laptops) and will enable these different segments to unite around one monitor interface specification.

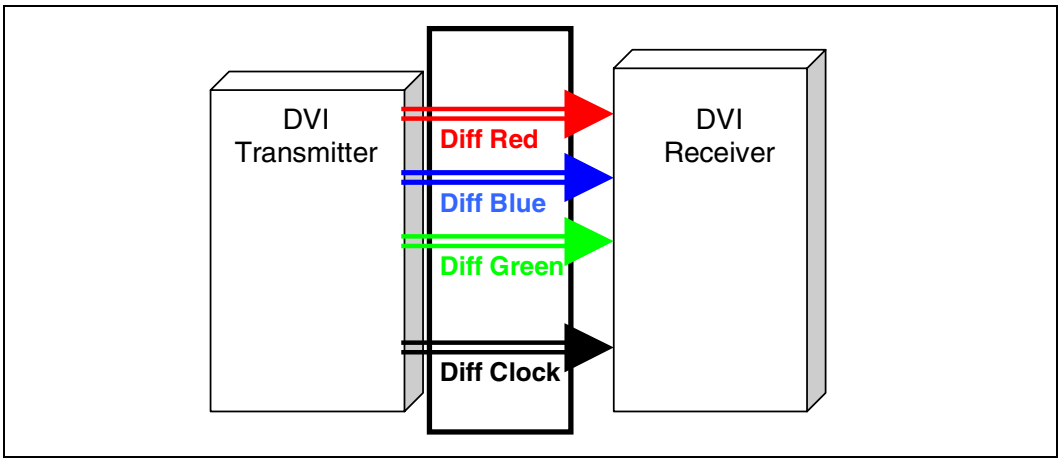
The DVI connection uses the Transition Minimizer Differential Signal (TMDS) standard.

The data transmitted across the DVI connection is a differential pair for the red, green, blue, and clock signals. Figure 31 shows how the data is transmitted. This connection can be made two ways:

- A direct connection from the transmitter to the receiver on the PC board, with the traces routed as differential pairs
- As specified in the DVI specification, using cables with DVI plugs and receptacles

If a direct connection is used — and the transmitter is not far from the receiver — the red, green, blue, and clock traces should be routed as differential pair signals. (Consult your transmitter-chip manufacturer for details of how far a particular chip can drive the data signals.)

Figure 31. DVI Interface Block Diagram



Other important control signals are any Display Data Channel (DDC) control signals and any hot-plug-detect signals. The DDC signals enable communication between the host system and the display, which allows configuration and control information to be exchanged in plug-and-play systems. Support for DDC 2B is implemented on both the Intel® 810 Chipset and Intel® 815 Chipset, using the Extended Display Identification Data (EDID) format.

If the alternative, DVI plug, cable, and receptacle connection method is used, adherence to the DVI interface specification is required. For more information, consult the Desktop Display Working Group Web page at http://www.ddwg.org.

5.2.2.1 Low-Voltage Differential Signaling Design

Low-voltage differential signaling (LVDS) is a signaling method used for high-speed transmission of binary data over copper. It is well-recognized that the benefits of balanced data transmission begin to outweigh the costs over single-ended techniques when signal transition times approach 10 ns.

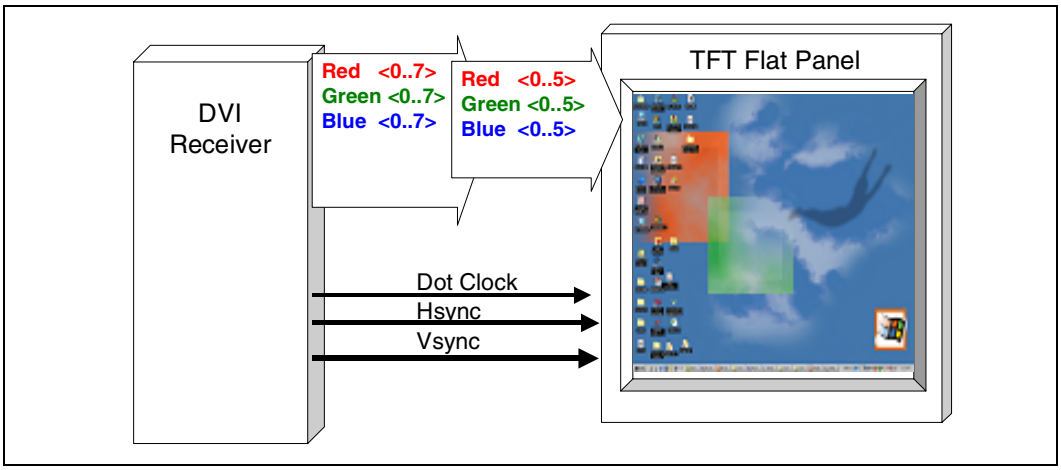
This signalling method represents rates of about 30 Mbps or clock rates of 60 MHz and above (in single-edge clocking systems).

5.2.3 From the DVI Receiver to the Flat Panel

The video data information received by the Digital Video Interface (DVI) receiver is interpreted back into its discrete form: the clock, Hsync, and Vsync signals and eight red, eight green, and eight blue signals. These signals are interfaced to the flat-panel display, as shown in Figure 32.

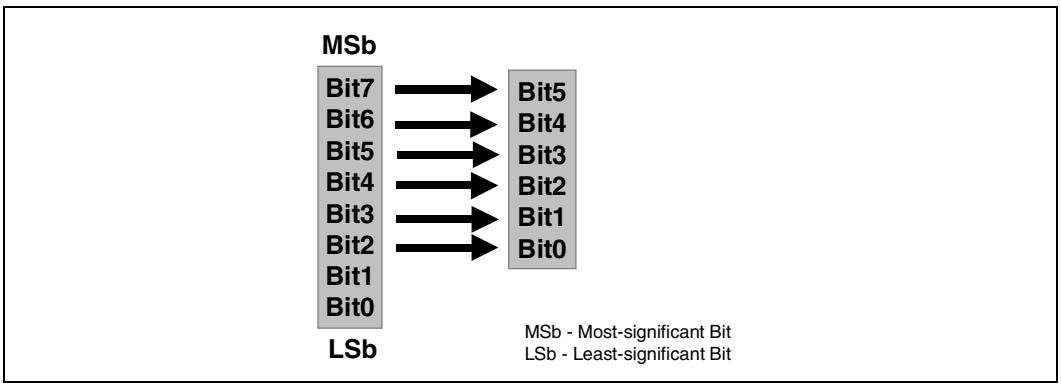
Note: Other details — among them voltage tolerance, drive current, Vih, Vil, Voh, and Vol — should be considered, when connecting the receiver to the display.

Figure 32. DVI-Receiver-to-Thin-Film-Transistor-Display Block Diagram



For a display with only six pins per color — such as the TFT example in Figure 32 — the connection is made by connecting the upper six pins, of each color's eight pins, to the six pins on the flat-panel display. Using the upper six pins reduces the overall color depth of the displayed image, but still enables the display to function. (See Figure 33.)

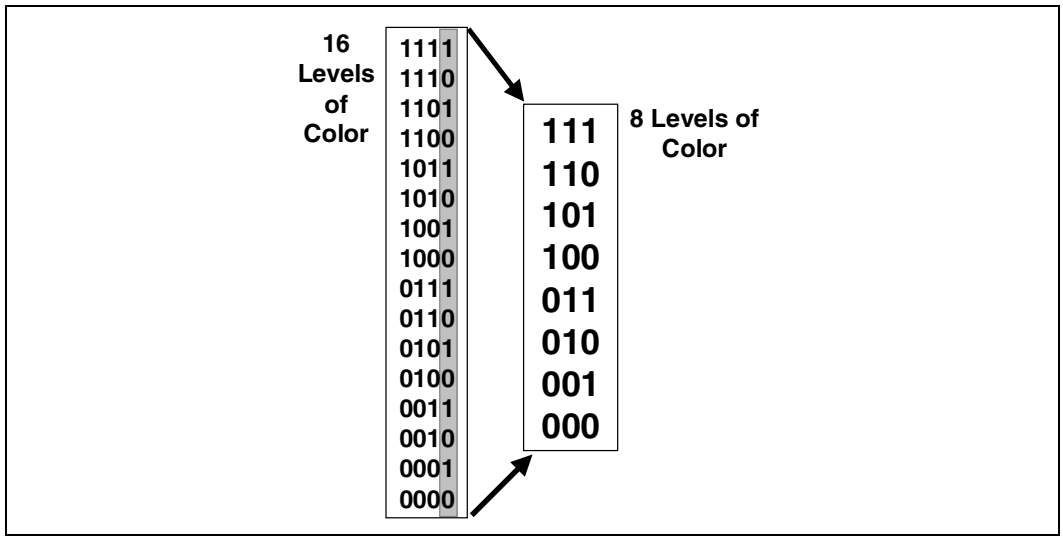
Figure 33. Color-Depth Reduction, From 8-Bit to 6-Bit



The amount of color depth lost is similar to reducing the color count from 24-bit, (eight red, eight green, and eight blue) down to 18-bit, (six red, six green, and six blue). Twenty-four-bit color gives you 16 million color variations, or 256 shades of red, 256 shades of green, and 256 shades of blue. Eighteen-bit color gives you 2.8 million color variations, or 64 shades of red, 64 shades of green, and 64 shades of blue.

As another example of the color resolution reduction, let's say we have 16 levels of color. By removing the least-significant bit — as shown by the columns of 1s and 0s in Figure 34 — we reduce our total bit count from 4 down to 3, thus from 16 levels down to 8.

Figure 34. Color-Depth Reduction, From 16-Bit to 8-Bit



6.0 Conclusions

This section summarizes this paper's findings and examines future issues. The topics include:

6.1 Intel® 810 Chipsets and Passive-Technology LCDs

Intel's graphics engine has two limitations: it does not support scaling nor DSTN technology.

A third-party approach that meets this requirement is the Silicon Motion's LynxEM+* Display Controller. This solution supports DSTN or TFT technologies, occupying one slot in the PCI/AGP bus. When the display is not located close to the system board, a Transition Minimizer Differential Signal (TMDS) or Low-Voltage Differential Signaling (LVDS) transmitter/receiver pair can be used, interfacing with the LynxEM+ controller.

6.2 Intel® 810 Chipsets and Active-Technology LCDs

Among existing third-party solutions, the Silicon Motion LynxEM+* Display Controller can be used to drive the TFT LCD from the PCI bus — for the Intel® 810 Chipset — or from the PCI bus or AGP port — for the Intel® 815 Chipset.

For optimum performance, the Digital Video Out (DVO) port, on the Intel chipset, can be interfaced to the TFT.

Additionally, a TMDS transmitter/receiver pair can be used, when the LCD is not located close to the system board. When the LCD is close to the system board, a SmartASIC SP1015* can be used.

In comparing DSTN and TFT flat-panel displays and their ability to interface with Intel® 810 Chipsets, the biggest difference is cost and performance.

- If cost is *not* an issue and performance is, the best solution is to integrate a TFT FPD with the Intel graphics engine.
- If cost *is* an issue and performance is *not*, the best fit solution would be a DSTN panel configured with a third-party vendor's graphics subsystem.

6.2.1 Discarded Solutions

Another way to interface the Intel® 810 Chipset with passive LCD technologies is to add a translator chip from the TFT to the DSTN. That would allow a system designer the flexibility to still use Intel's internal graphics engine and DVO port. This solution, however, has two problems: performance and cost.

High-speed video — such as the AVI and MPEG formats — would exhibit ghosting effects which would diminish the advantage of having the FPD on the high-speed bus.

On the pricing issue, adding the translator chip would significantly increase costs. Further increasing costs, the addition of the translator chip would require more memory for the frame buffer and more space on the platform.

6.3 Trends

To produce larger TFT displays and increase display resolutions, manufacturers of flat-panel displays are starting to include receiver chips, inside the display panel, as the device's primary interface. Manufacturers also are doing this to accommodate the desktop market.

As these new FPDs are integrated into embedded applications, there will be a growing need to address the issue of interfacing through the DVI.

Reference Schematics

Figure 35 PCI Graphics Using LynxEM+ to Support DSTN Flat Panels.

Figure 36 Intel® 810 Chipset-to-TFT Configuration 1, Using the DVO Port
Interfacing the SmartASIC SP1015 to the DVO port.

Figure 37 Intel® 810 Chipset-to-TFT Configuration 2, Using the DVO Port.
Interfacing the Silicon Image SIL154 to the DVI plug.

Figure 38 DVO Port Interface.
Interfacing the Silicon Image SIL154 to the DVO port on an Intel® 810 Chipset.

Note: These schematic pages are provided as a reference only and may change as the reference design is corrected and updated. Intel does not guarantee any design. Each company is finally responsible for determining the suitability of its own design and is responsible for the quality of its products.

Figure 35. PCI Graphics Using LynxEM+ to Support DSTN Flat Panels

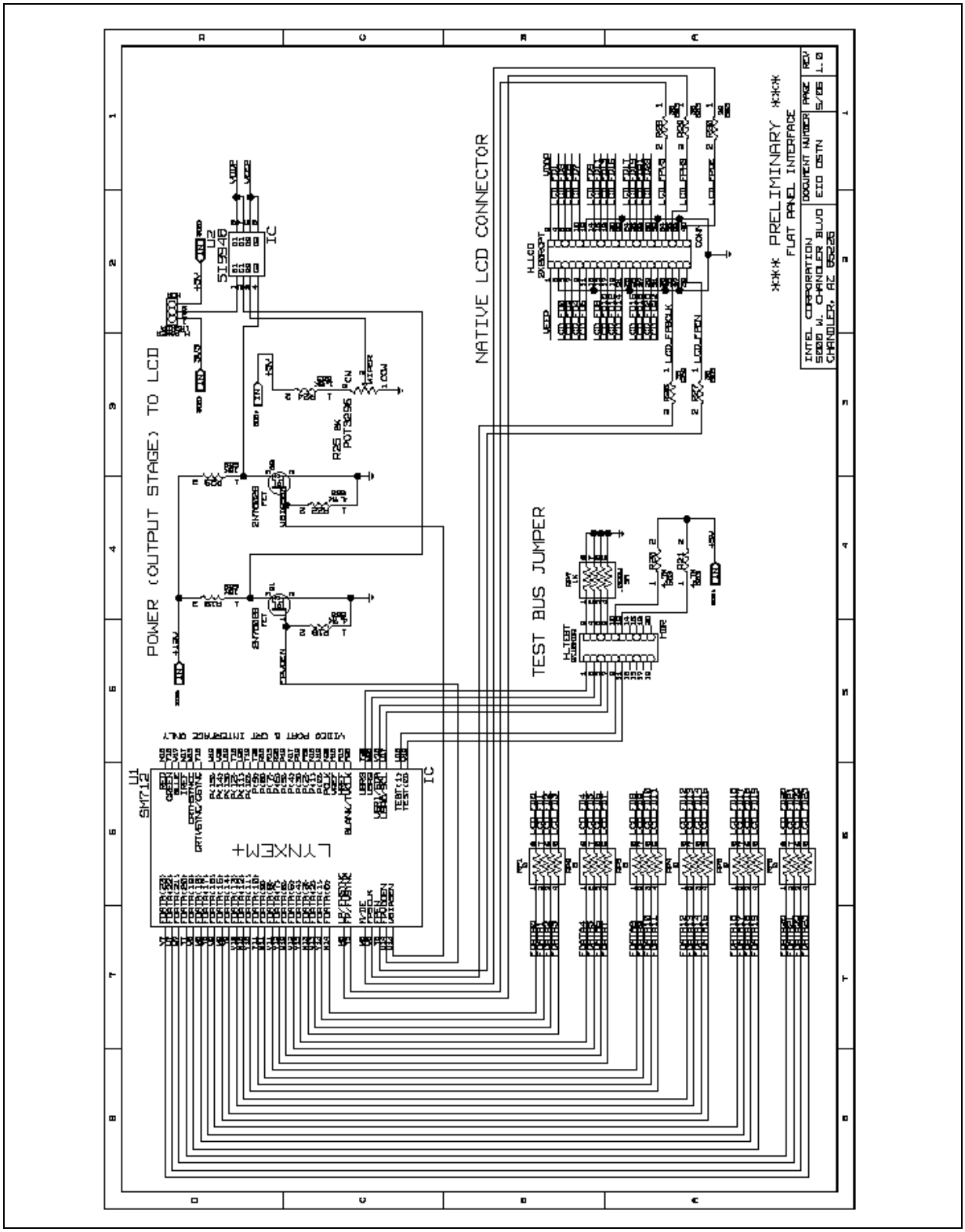


Figure 36. Intel® 810 Chipset-to-TFT Configuration 1, Using the DVO Port

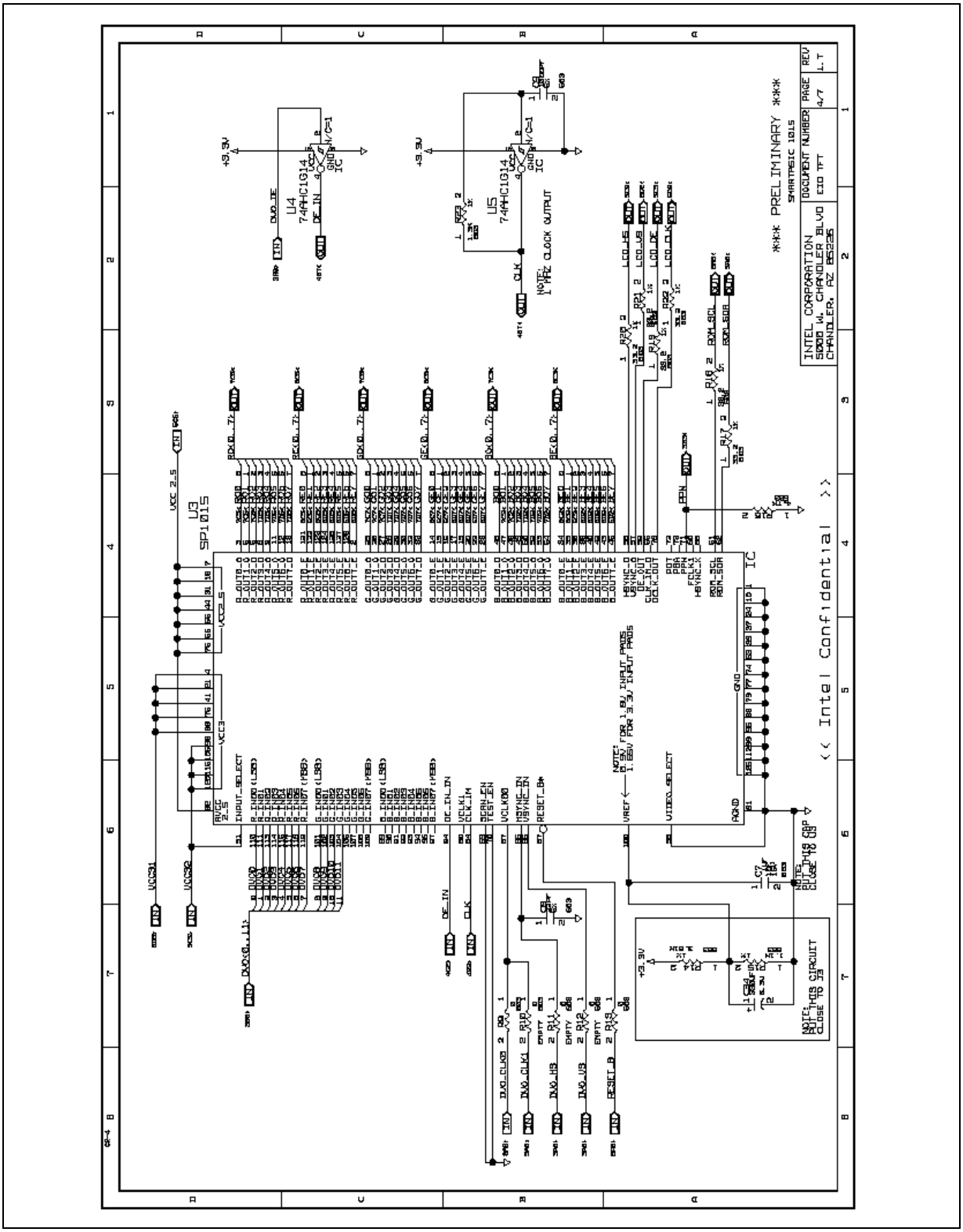


Figure 37. Intel® 810 Chipset-to-TFT Configuration 2, Using the DVO Port

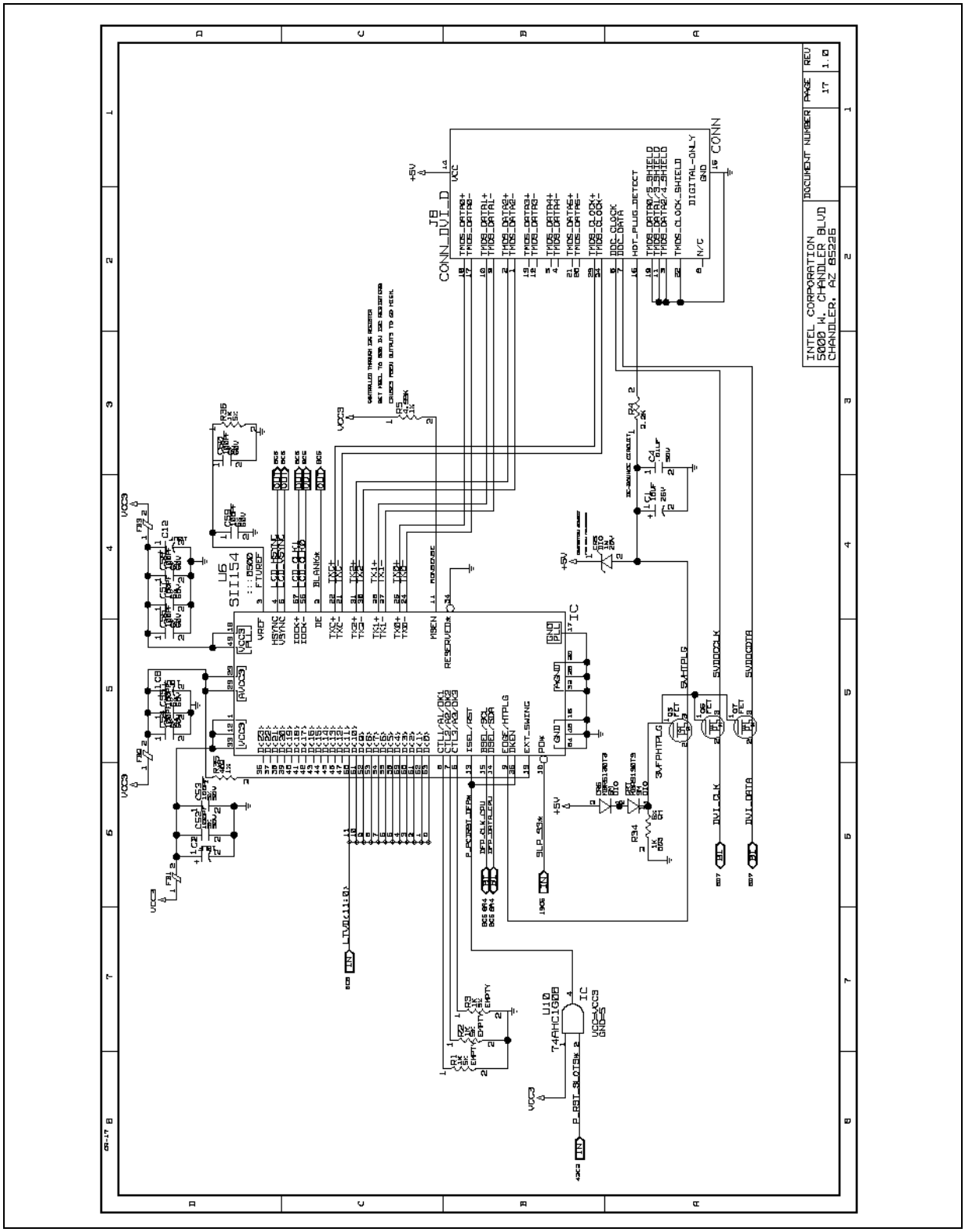
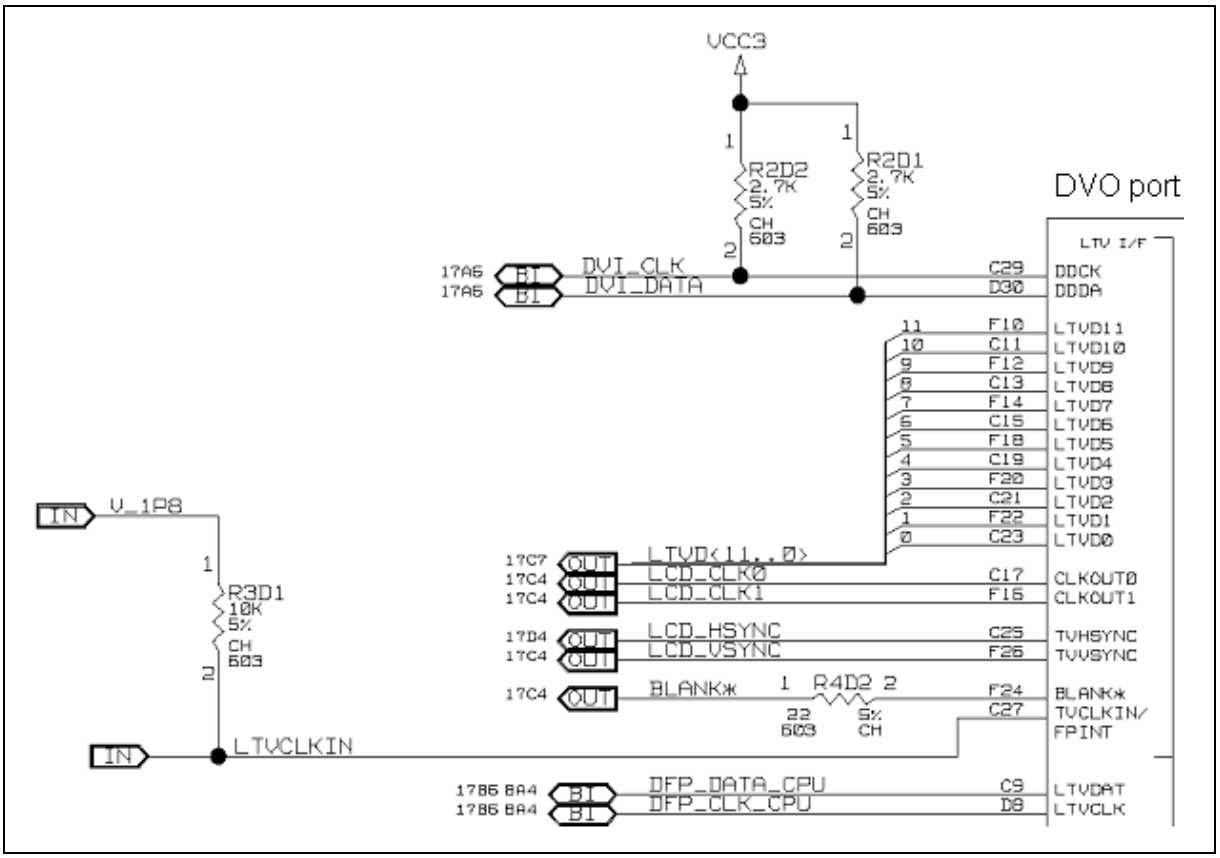


Figure 38. DVO Port Interface



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NOTE:
1. This document is available through an Intel Field Sales Representative.

Glossary

AGP	Accelerated Graphics Port. Refers to the AGP/PCI interface that is utilized by Intel® graphics controllers.
Bifringence	The refraction of light in two slightly different directions to form two rays. A property of isotropic materials such as the liquid crystals in LCDs. (Also called “double refraction.)
CRT	Cathode-Ray Tube. The technology, used in most televisions and computer display screens, to display images. The image is painted by an electron beam that moves back and forth across the back of the screen, lighting up phosphorous dots on the inside of the glass tube.
DDC	Display Data Channel. A channel that sits between the monitor and the PC graphics adapter (with the video BIOS ROM). The channel uses a system’s EDID data for enabling the monitor and PC to work together.
DDWG	Desktop Display Working Group. A group of companies involved with the digital displays that formed to standardize communication protocols for connecting digital displays. The group’s Web site is: http://www.ddwg.org.
DSTN	Double-layer SuperTwist Nematic. A passive-matrix LCD technology that uses two display layers to accommodate higher-resolution displays.
DVI	Digital Visual Interface. A DDWG specification that defines the connector and interface for digital displays.
DVO	Digital Video Out. One of the dedicated ports in all Intel graphics controllers’ digital display channels. Some Intel controllers may have two additional DVO ports, typically multiplexed with the AGP port. This second configuration enables the controller to run in the 24-bit, dual-channel mode.
EDID	Extended Display Identification Data. A VESA data format that contains basic information about a monitor and its capabilities. The data includes vendor information, maximum image size, color characteristics, factory preset timings, frequency range limits, and character strings for the monitor’s name and serial number.
FPD	Flat-Panel Display. Another term for an LCD panel.
Frame Creation	The progressive scan method used by displays that sequentially scan pixels, moving left to right in the top row, and proceeding, one row at a time, from the top row to the bottom. (See “Refresh Rate.”)
FRM	Frame Rate Modulation. The method used to create a color palette or grayscale in passive LCDs.
GMCH	Intel® Graphics and Memory Controller Hub. A term generically referring to one of the Intel graphics and memory controller hub components.
LCD	Liquid Crystal Display. A display device consisting of two sheets of polarizing material with a liquid crystal compound between. Electric current is passed through the liquid to manipulate the liquid’s crystals like a shutter. The current aligns the crystals to block the light, and clear the display, or moves the crystals out of alignment, to pass the light and paint the display.

LVDS	Low-Voltage Differential Signaling. A DDWG standard for high-speed, low-power data transmission.
Nematic	A physical state between the phases of liquid and solid where the compound exists in ambient temperature.
Refresh Rate	The frequency at which a display's pixels receive new input. (See "Frame Creation.")
Smectic	A physical state between the phases of liquid and solid where the compound exists in ambient temperature.
RGB	Red Green Blue. The three primary colors that a graphic engine uses to create a color palette or grayscale.
SSTN	Single-Scan Twist Nematic. Passive technology's initially implementation. This solution, however, had problems with high-resolution displays which led to the development of Double-layer SuperTwist Nematic (DSTN) displays.
SVGA	Super Video Graphics Array. A standard, developed by VESA, that made significant improvements over the screen resolution and the color-pallet size of the previous, VGA standard.
TFT	Thin Film Transistor. A type of LCD, flat-panel display screen, in which each subpixel is controlled by one transistor per cell. For that reason, the device is called an "active" type of display or an "active-matrix LCD." The TFT technology provides the best resolution of all flat-panel designs, but also is the most expensive.
TMDS	Transition Minimized Differential Signaling. The signaling interface, from Silicon Image, that is used in DVI.
TN	Twist Nematic. An early, and still common, type of LCD flat-panel display that consists of a grid of horizontal and vertical wires with a single-pixel, LDC element at each grid intersection. Because the pixel is not further manipulated, this type of display is called a "passive" one. Passive displays were thought to be endangered by the crisper active-matrix displays, but the cost of the active displays — and technological advances such as DSTN — have given the cheaper passive displays renewed life in the market.
VESA	Video Electronics Standards Association. A consortium of video adapter and monitor manufacturers that standardizes video protocols. VESA has developed a family of video standards, among them the Super VGA (SVGA).
VGA	Video Graphics Array. An old, low-end standard for the resolution of PC displays.
YUV	A compressed color video standard format that defines a luminance (Y) signal and two chrominance-differentiated signals (CrCb). Officially, the standard is designated as "YCrCb 4:2:2" or "YCrCb 4:4:4."