Intel® Pentium® M Processor and the Intel® E7501 Chipset Platform

For use with the Intel® Pentium® M Processor and the Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 cache

Design Guide

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Revision History

Date	Revision	Description
January 2007	007	Updated Table 1, “Reference Documents” on page 19.
August 2004	006	Added support for Intel® Pentium® M Low Voltage 738 Processor.
June 2004	005	Added support for the Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 cache Updated recommendation for TEST[1] pin.
July 2003	004	Changes to the command clock and chip select routing in the Memory Interface Guidelines chapter.
June 2003	003	In chapter 13 section 13.1 table 95 (Sheet 4 of 5), recommendation for TEST[3:1] should be No Connect. For testing purposes leave stuffing options to pull-down to Vss.
		In chapter 6 section 6.4.1 table 41, added text to state CMDCLK_B[3:0] and CMDCLK_B[3:0]# signals may be left as No Connect (no termination required).
April 2003	002	In part 2 of 4 of the ICH3 schematics (PDF page 322, schematic page 40), the PSI# signal was moved from GPIO21 (output only) to GPIO6 (input only).
April 2003	001	Initial release of this document.

Introduction 1

This design guide documents Intel's design recommendations for systems based on the Intel® Pentium® M processor or the Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 Cache and Intel® E7501 Chipset. In addition to providing board design recommendations (e.g., layout and routing guidelines), this document addresses system design issues (e.g., power delivery).

Carefully follow the design information, board schematics, debug recommendations, and system checklists provided in this document. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues.

Note that the guidelines recommended in this document are based on experience, simulation work and platform validation completed at Intel while developing the Intel® Pentium® M Processor and Intel® E7501 Chipset-based systems. Recommendations are subject to change.

Board designers may use the associated Intel schematics as a reference. While the schematics cover a specific design implementation, the core schematics remain the same for most Intel® Pentium® M Processor / Intel® E7501 Chipset-based platforms. The schematic set provides a reference schematic for each IIntel® E7501 Chipset component as well as common motherboard options. Additional flexibility is possible through other permutations of these options and components.

Note: Unless otherwise noted, all design considerations for the Intel® Pentium® M Processor may also be used for the Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 Cache. Please refer to the *Intel® Pentium® M Processor Datasheet* and *Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 Cache Datasheet* for detailed processor information.

1.1 Reference Documents

Table 1. Reference Documents (Sheet 1 of 2)

Document	Document Number/Source
Intel® Pentium® M Processor Datasheet	http://www.intel.com/design/chipsets/datashts/252612.htm
Intel® Pentium® M Processor Specification Update	http://www.intel.com/design/intarch/specupdt/252665.htm
Intel® Pentium® M Processor Thermal Design Guide for Embedded Applications	http://www.intel.com/design/intarch/designgd/273885.htm
CK-408 Clock Synthesizer/Driver Specification	Contact your Intel Field Representative
CK-408B Clock Synthesizer/Driver Specification	Contact your Intel Field Representative
ITP700 Debug Port Design Guide	http://www.intel.com/design/Xeon/guides/249679.htm
Intel® Pentium® M Debug Port Design Guide	Contact your Intel Field Representative
Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet	http://developer.intel.com/design/chipsets/e7500/datashts/290733.htm

Table 1. Reference Documents (Sheet 2 of 2)

Document	Document Number/Source
Intel® PCI-64 Hub 2 (P64H2) Thermal and Mechanical Design Guidelines	http://developer.intel.com/design/chipsets/designex/252175.htm
Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet	http://developer.intel.com/design/chipsets/e7500/datashts/290732.htm
PCI Bus Power Management Interface Specification, Revision 1.1	http://www.pcisig.com/specifications/conventional/pci_bus_power_management_interface
PCI Local Bus Specification, Revision 2.2	http://www.pcisig.com/specifications/conventional
PCI Hot Plug Specification, Revision 1.1	http://www.pcisig.com/specifications/conventional/pci_hot_plug
PCI-to-PCI Bridge Architecture Specification, Revision 1.1	http://www.pcisig.com/specifications/conventional/pci_to_pci_bridge_architecture
PCI-X Specification, Revision 1.0a	http://www.pcisig.com/specifications/pcix_20/pci_x
PCI Standard Hot-Plug Controller and Subsystem Specification, Revision 1.0	http://www.pcisig.com/specifications/conventional/pci_hot_plug
System Management Bus Specification (SMBus), Revision 1.1	http://www.smbus.org/specs/
Universal Serial Bus Specification, Revision 1.1	http://www.usb.org/developers/docs/
AP-728 Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions	http://developer.intel.com/design/chipsets/applnots/292276.htm
Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet	http://www.intel.com/design/chipsets/datashts/251927.htm
Intel®E7500/E7501/E7505 Chipset Thermal Design Guide	http://www.intel.com/design/chipsets/e7500/guides/298647.htm
Intel® E7500 and Intel® E7501 Chipsets MCH Thermal Design Guide for Embedded Applications	http://developer.intel.com/design/chipsets/e7501/guides/273819.htm
Distinguishing Between Single-Rank and Double-Rank Registered DDR DIMM Modules Application Note (AP-727)	http://developer.intel.com/design/chipsets/applnots/292275.htm
Intel® Pentium® M Processor on the 90 nm Process with 2-MB L2 Cache Datasheet	http://developer.intel.com/design/mobile/datashts/302189.htm
Intel® Pentium® M Processor on the 90 nm Process with 2-MB L2 Cache Specification Update	http://developer.intel.com/design/mobile/specupdt/302209.htm

Note: Contact your Intel Field Representative for additional reference documentation.

1.2 Terminology

This section defines terminology used throughout the design guide.

Table 2. Conventions and Terminology (Sheet 1 of 4)

Terminology	Description
Aggressor	A network that transmits a coupled signal to another network.
AGTL+	The processor system bus uses a bus technology called Assisted Gunning Transceiver Logic (AGTL+). AGTL+ buffers are open-drain, and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to assist the pull-up resistors during the first clock of a low-to-high voltage transition.
Asynchronous GTL+	Legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output signals (FERR# and IERR#) and non-AGTL+ signals (THERMTRIP# and PROCHOT#) also utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0], and are therefore referred to as Asynchronous GTL+ Signals. All of the Asynchronous GTL+ signals must be asserted for at least two BCLKs in order for the processor to recognize them.
Bus Agent	A component or group of components that, when combined, represent a single load on the system bus.
Core Power	Core power refers to a power rail that is on only during full-power operation. These power rails are on when the active-low PSON signal is asserted to the power supply. The core power rails that are distributed directly from the power supply are: +12 V, +5 V, and +3.3 V.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Crosstalk – Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal. • Forward Crosstalk – Coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal. • Even Mode Crosstalk – Coupling from a signal or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Crosstalk – Coupling from a signal or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Derived Power	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, +2.5 V is derived from a +5 V power rail using a voltage regulator.
Uni-Processor (UP)	Used to specify a system configuration using one processor.
Electromagnetic Compatibility (EMC)	The successful operation of electronic equipment in its intended electromagnetic environment.
Electromagnetic Interference (EMI)	Electromagnetic radiation from an electrical source that exceeds the federally regulated limits.

Table 2. Conventions and Terminology (Sheet 2 of 4)

Terminology	Description
Flight Time	Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{co} of the driver, plus any adjustments to the signal at the receiver needed to ensure the setup time of the receiver. More precisely, flight time is defined as: • The time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications i.e., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when only the driver may drive a test load used to specify the driver's AC timings. • Maximum and Minimum Flight Time – Flight time variations are caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance, and differences in I/O buffer performance as a function of temperature, voltage, and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects. • Maximum flight time is the largest acceptable flight time that a network experiences under all conditions. • Minimum flight time is the smallest acceptable flight time that a network experiences under all conditions.
Full-power	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state, and the S1 (processor stop-grant) state.
GTLREF	Reference voltage for AGTL+ input pins.
Intel® x4 SDDC	Intel® x4 Single Device Data Correction - DDR Memory correction methodology: • Dual channel mode - corrects any number of errors contained in a 4-bit nibble and detects all errors contained entirely within two 4-bit nibbles. • Single Channel mode - corrects single bit errors contained in a 4-bit nibble and detects single bit errors contained entirely within two 4-bit nibbles
X/Y	Format used to signify trace width and space width. X = width and Y = space.
X:Y	Format used to signify trace width and space width **ratio**. X = width and Y = space.
Inter-Symbol Interference (ISI)	The effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line, and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI may impact both timing and signal integrity.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Overshoot	The maximum voltage observed for a signal at the device pad, measured with respect to VCC.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.
Pentium M processor	The Intel® Pentium® M Processor or the Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 Cache. Both processors share a common design guide.
Pin/Ball	The contact point of a component package to the traces on a substrate, such as the motherboard. Signal quality and timings may be measured at the pin.

Table 2. Conventions and Terminology (Sheet 3 of 4)

Terminology	Description
Power-Good	Power-Good, PWRGOOD, or CPUPWRGOOD (an active high signal) indicates that all of the system power supplies and clocks are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.
Power Rails	A power supply has five power rails: +12 V, –12 V, +5 V, +3.3 V, and +5 VSB. In addition to these power rails from the power supply, several other power rails are derived on the motherboard by on-board regulators.
Ringback	The voltage to which a signal changes after reaching its maximum absolute value. Ringback may be caused by reflections, driver oscillations, or other transmission line phenomena.
PSB	The processor system bus is the bus that connects the processor to the MCH.
Setup Window	The time between the beginning of Setup to Clock (TSU_MIN) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
Simultaneous Switching Output (SSO)	Effects which are differences in electrical timing parameters and degradation in signal quality. This is caused by multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal or in the same direction. These are called odd mode and even mode switching, respectively. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (“push-out”) or a decrease in propagation delay (“pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Standby Power Rail	Standby power is supplied by the power supply during times when the system is powered down. The purpose is to maintain functions that always need to be enabled, such as the date and time-of-day within the BIOS. The power supply provides a +5 VSB power rail.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	The minimum voltage extending below VSS observed for a signal at the device pad.
CPU_VCC	CPU_VCC is the core power for the processor. The system bus is terminated to CPU_VCC.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
Voltage Regulator Down (VRD)	A VRD refers to a processor voltage regulator which is placed directly onto the system motherboard.
Voltage Regulator Module (VRM)	A VRM refers to a processor voltage regulator which is designed on an add-in card that interfaces with the system design through a connector on the platform.
MCH	A component of the Intel® E7501 Chipset, the Intel® E7501 Memory Controller Hub contains an integrated processor and DRAM interface.
Intel ICH3-S	A component of the Intel E7501 chipset, the Intel® 82801CA I/O Controller Hub 3-S contains the primary PCI interface, LPC interface, USB, ATA-100, and other legacy functions.

Table 2. Conventions and Terminology (Sheet 4 of 4)

Terminology	Description
Intel P64H2	A component of the Intel E7501 chipset, the Intel® 82870P2 PCI / PCI-X 64-bit Hub 2 Bus Controller.
Hub Interface (HI)	Intel high speed proprietary hub interconnect, known as the Hub Interface (HI), that interfaces the Intel E7501 chipset to the Intel® ICH3-S and Intel® P64H2.
In Target Probe (ITP)	In Target Probe - A debug tool that is needed to debug BIOS, logic, signal integrity, general software, and hardware issues involving CPUs, chipsets, SIOs, PCI devices, and other hardware in a platform.

1.3 System Overview

The Intel® E7501 Chipset is Intel's server/embedded chipset validated for use with the Intel® Pentium® M Processor and the Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 Cache. The chipset architecture provides the performance and feature-set required for uni-processor based servers in the entry-level and mid-range, front-end, and general-purpose server and embedded market segments. A chipset component interconnect, the Hub Interface 2.0 (HI2.0), is designed into the Intel® E7501 Chipset to provide more efficient communication between chipset components for high-speed I/O. Each HI2.0 provides 1.066 Gbytes/s I/O peak bandwidth. The Intel® E7501 MCH has three HI2.0 connections, delivering 3.2 Gbytes/s peak bandwidth for high-speed I/O, which may be used for PCI/PCI-X bridges. The system bus is used to connect the processor with the Intel® E7501 Chipset. The Intel® Pentium® M Processor system bus uses a 400 MHz transfer rate for data transfers, delivering 3.2 Gbytes/s. The Intel® E7501 Chipset architecture supports a 144-bit wide, 200 MHz DDR memory interface also capable of transferring data at 3.2 Gbytes/s.

In addition to these performance features, Intel® E7501 Chipset-based platforms also provide the RASUM (Reliability, Availability, Serviceability, Usability, and Manageability) features required for entry-level and mid-range servers. These features include: Intel® x4 Single Device Data Correction (x4 SDDC) technology ECC for memory, ECC for all high-performance I/O, out-of-band manageability through SMBus target interfaces on all chipset components, memory scrubbing and auto-initialization, processor thermal monitoring, and Hot-Plug PCI. For a complete list of the features on this platform, refer to the component datasheets listed in Table 1.

1.3.1 Intel® Pentium® M Processor

The Intel® Pentium® M Processor is a high performance, lower voltage processor with several micro-architectural enhancements over existing Intel mobile processors. Some key features of the Intel® Pentium® M processor micro-architecture include Dynamic Execution, data pre-fetch logic, 400-MHz source-synchronous Intel® Pentium® M processor system bus, on-die 1-Mbyte second level (L2) cache with Advanced Transfer Cache Architecture, Streaming SIMD Extensions 2 (SSE2), and Enhanced Intel® SpeedStep® technology.

The Intel® Pentium® M Processor system bus uses a source-synchronous transfer of address and data to improve performance and enables addressing at 2X the system bus frequency and data transfers at 4X the system bus frequency of 100 MHz. This allows the 400 MHz system bus support to transfer data at 3.2 Gbytes/s.

The Intel® Pentium® M Processor with 1-Mbyte L2 cache includes the advanced micro-architecture features described in the following sections:

1.3.1.1 Architectural Features

- Supports Intel Architecture with Dynamic Execution
- High performance, low-power core
- On-die, primary 32-kbyte instruction cache and 32-kbyte write-back data cache
- On-die, 1-MByte second level cache with Advanced Transfer Cache Architecture
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2)
- 400-MHz, Source-Synchronous Processor System Bus
- Advanced Power Management features including Enhanced Intel® SpeedStep® Technology

1.3.1.2 Packaging/Power

- 479-ball Micro-FCBGA packages
- 478-pin Micro-FCPGA packages
- VCC-CORE: 1.484 V (highest frequency mode) to 0.956 V (lowest frequency mode)
- VCCA (1.8 V)
- VCCP (1.05 V)

1.3.1.3 Enhanced Intel® SpeedStep® Technology

The Intel® Pentium® M Processor features Enhanced Intel® SpeedStep® Technology. Unlike previous implementations of Intel SpeedStep technology, this technology enables the processor to switch between multiple frequency and voltage points instead of two. This will enable superior performance with optimal power savings. Switching between states is software controlled unlike previous implementations where the GHI# pin is used to toggle between two states. Following are the key features of Enhanced Intel SpeedStep technology:

- Multiple frequency and voltage operating points provide optimal performance at the lowest power.
- Frequency and voltage selection is software controlled by writing to processor MSRs (Model Specific Registers) thus eliminating chipset dependency.
  - If the target frequency is higher than the current frequency, Vcc is ramped up by placing a new value on the VID pins and the PLL then locks to the new frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the new frequency and the Vcc is changed through the VID pin mechanism.
  - Software transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until its completion.
- The processor controls voltage ramp rates internally to ensure glitch free transitions.
- Low transition latency and large number of transitions possible per second.
  - Processor core (including L2 cache) is unavailable for up to 10 µs during the frequency transition.
  - The bus protocol (BNR# mechanism) is used to block snooping.

- No bus master arbiter disable required prior to transition and no processor cache flush necessary.
- Improved Intel Thermal Monitor mode.
  - When the on-die thermal sensor indicates that the die temperature is too high, the processor may automatically perform a transition to a lower frequency/voltage specified in a software programmable MSR.
  - The processor waits for a fixed time period. If the die temperature is down to acceptable levels, an up transition to the previous frequency/voltage point occurs.
  - An interrupt is generated for the up and down Intel Thermal Monitor transitions enabling better system level thermal management.

1.3.2 Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 Cache

All features of the Intel Pentium M processor are supported by the Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 Cache. The processors also utilize the same package and footprint. This section only lists the additional on-die enhancements. For more details, see the *Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 Cache Datasheet*.

New features on the Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 Cache include:

- On-die 2-MB second level cache
- Strained silicon process technology
- Voltage and Power Changes:
  Intel® Pentium® M Processor 745 (90nm, 2MB L2 Cache, 1.8GHz, 400MHz FSB):
  - $V_{CC\text{-}CORE\ (HFM)}$: 1.276V – 1.340V
  - $V_{CC\text{-}CORE\ (LFM)}$: 0.988V
  - V_{CCA}: 1.8V only
  - TDP: 21 W

  Intel® Pentium® M Processor Low Voltage 738 (90 nm, 2 MB L2 Cache, 1.4 GHz, 400 MHz FSB):
  - $V_{CC\text{-}CORE\ (HFM)}$: 1.052 V
  - $V_{CC\text{-}CORE\ (LFM)}$: 0.956 V
  - V_{CCA}: 1.8 V and 1.5 V supported
  - TDP: 10 W

1.3.3 Intel® E7501 Chipset

The Intel® E7501 Chipset consists of three major components:

- The Intel® E7501 Chipset Memory Controller Hub (referred to throughout this document as the MCH).
- The Intel® 82801CA I/O Controller Hub 3 (hereafter referred to as ICH3-S).
- The Intel® 82870P2 PCI/ PCI-X 64-bit Hub 2 (abbreviated to Intel® P64H2).

The chipset components communicate through Hub Interfaces (HIs). The MCH provides four Hub Interface connections: one HI1.5 for the ICH3-S and three HI2.0s for high-speed I/O using Intel P64H2 components. The Hub Interfaces are point-to-point and therefore only support two components (the MCH plus one I/O device). Therefore, the system supports a maximum of three Intel P64H2 devices.

1.3.3.1 Intel® E7501 Memory Controller Hub (MCH)

The MCH is a 1005-ball FC-BGA package. For this platform, the MCH supports the following functionality:

- Platform System Bus:
  - Supports single Intel® Pentium® M Processor at 100 MHz (x4 transfers) - use 400 MHz system bus (2X address, 4X data)
  - Supports PSB peak bandwidth of 3.2 Gbytes/s (400 MHz)
  - Supports Intel Pentium M processor 32-bit system bus addressing model
  - 12 deep in-order queue, two deep defer queue
- Platform Memory Bus:
  - Single or dual channel DDR memory support
  - 144-bit wide, DDR200 memory interface with memory peak bandwidth of 3.2 Gbytes/s
  - Supports x72, ECC, registered DDR200 using 128-Mb, 256-Mb and 512-Mb DRAMs
  - Supports a maximum of 4 Gbytes of memory
  - Error correction:

    Dual Channel supports Single 4-bit Error Correct, Double 4-bit Error Detect (S4EC/ D4ED) using Intel® x4 Single Device Data Correction (x4 SDDC)

    Single Channel supports Single bit Error Correct, Double bit Error Detect (SEC/DED) using Intel® x4 Single Device Data Correction (x4 SDDC)
  - Supports up to 32 simultaneous open pages
- I/O:
  - Provides Hub Interface 1.5 (HI1.5) connection for ICH3-S (Hub Interface_A):

    - 266 Mbytes/s point-to-point connection for ICH3-S with parity protection

    - 8-bit wide, 66 MHz base clock, 4X data transfer

    - Parallel termination mode for longer trace lengths

    - 64-bit inbound addressing, 32-bit outbound addressing
  - Provides three Hub Interface 2.0 (HI2.0) Connections for Intel P64H2 devices (Hub Interfaces B, C and D):

- 1.066 Gbytes/s point-to-point connection per HI2.0 for I/O bridges with ECC protection for up to 3.2 Gbytes/s bandwidth when three devices are used
- 16-bit wide, 66 MHz base clock, 8X data transfer
- Parallel termination mode for longer trace lengths
- 64-bit inbound addressing, 32-bit outbound addressing

- Power Management:
  - Supports C0, C1, C2, S0, S1, and S5 power states **(Does not** support C3, C4, S2, S3 and S4 states)

1.3.3.2 I/O Controller Hub 3 (Intel® 82801CA ICH3-S) Features

The I/O Controller Hub 3 (ICH3-S) provides the legacy I/O subsystem for Intel® E7501 Chipset-based platforms. Additionally, it integrates many advanced I/O functions. The ICH3-S includes the following features:

- Provides Hub Interface 1.5 connection to MCH:
  - 266 Mbytes/s point-to-point connection for ICH3-S with parity protection
  - 8-bit wide, 66 MHz base clock, 4X data transfer
  - Parallel termination mode for longer trace lengths
  - 64-bit inbound addressing, 32-bit outbound addressing
- Two channel ultra ATA/100 bus master IDE controller
- Three Universal Host Controller Interface (UHCI) USB 1.1 compliant host controllers (capabilities for six ports)
- I/O APIC
- *System Management Bus (SMBus) Specification*, Version 2.0 compliant controller
- Low Pin Count (LPC) interface
- *AC'97 Component Specification*, Revision 2.2, compliant interface
- *PCI Local Bus Specification*, Revision 2.2, compliant interface
- Integrated LAN controller

1.3.3.3 PCI/PCI-X 64-bit Hub 2 (Intel® P64H2) Features

The Intel® P64H2 provides PCI/PCI-X, high-performance I/O capabilities including:

- 16-bit Hub Interface 2.0 Connection to MCH:
  - 1.066 Gbytes/s point-to-point connection for I/O bridges with ECC protection
  - 16-bit wide, 66 MHz base clock, 8X data transfer
  - Parallel termination mode for longer trace lengths
  - 64-bit inbound addressing, 32-bit outbound addressing
- Two independent, 64-bit PCI/PCI-X interfaces:
  - *PCI-X Specification*, Revision 1.0, compliant
  - *PCI Local Bus Specification*, Revision 2.2, compliant

— *PCI-PCI Bridge Architecture Specification*, Revision 1.1, compliant

— *PCI Hot-Plug Specification*, Revision 1.1, compliant

— One PCI Hot-Plug Controller (PHPC) per PCI/PCI-X interface

— One IOxAPIC per PCI/PCI-X Interface (16 external, eight internal interrupts)

— SMBus target for access to all internal PCI registers

1.3.4 Peak Bandwidth Summary

Table 3 describes the clock maximum speed, sample rate, and peak bandwidth for each of the interfaces in the Intel® E7501 Chipset-based platform.

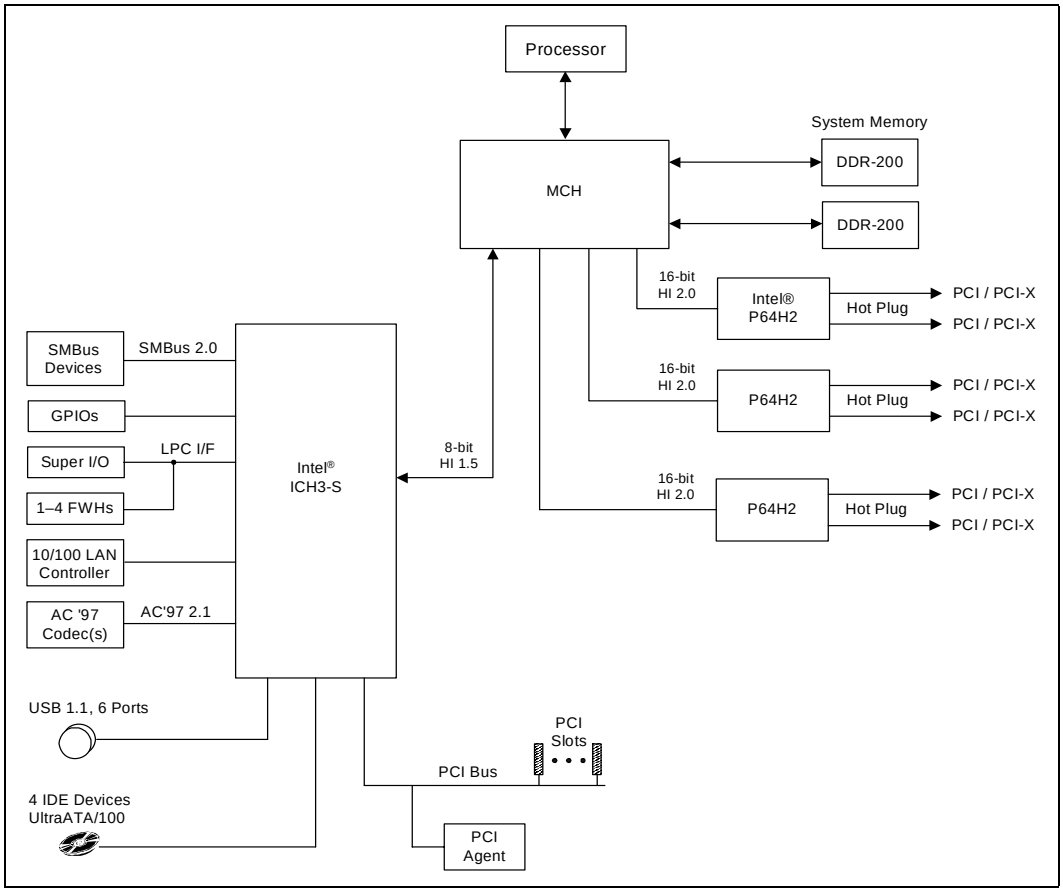
Table 3. Intel® Pentium® M Processor or Intel® E7501 Chipset Platform Peak Bandwidth Summary

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth (Mbytes/s)
System Bus (Data)	100	4	8	3200
DDR Interface • Dual Channel • Single Channel	100	2	16	3200 (Dual Channel) 2200 (Single Channel)
Hub Interface A	66	4	1	266
Hub Interface B, C, D	66	8	2	1066
PCI-X	133	1	8	1066

1.3.5 System Configurations

Figure 1 illustrates an example Intel® E7501 Chipset-based system configuration for server or embedded platforms using the Intel® Pentium® M Processor.

Figure 1. Intel® Pentium® M Processor and Intel® E7501Chipset-Based System Configuration Example



Component Quadrant Layout 2

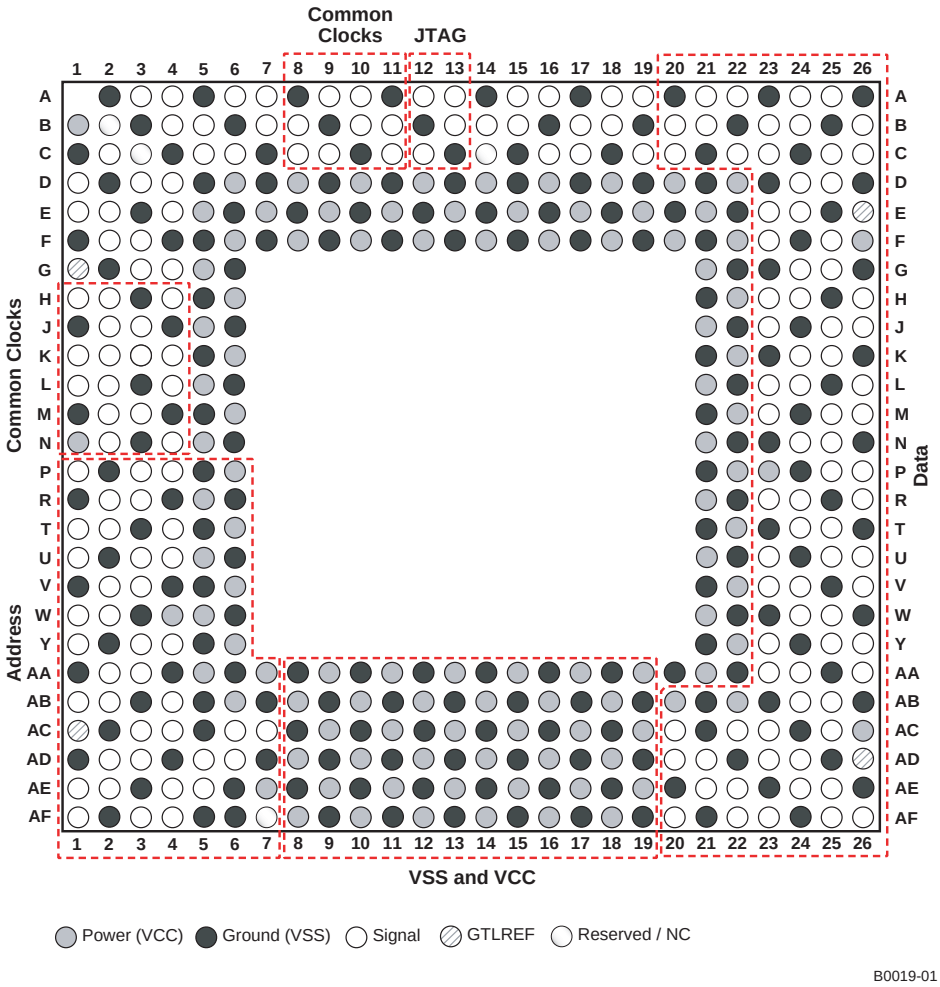
The following figures show only general quadrant information, not exact component pin count. Designers should use only the exact pin assignment to conduct routing analyses. Reference the following documents for exact pin assignment information.

- *Intel® Pentium® M Processor Datasheet*
- *Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 cache Datasheet*
- *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet*
- *Intel® PCI-64 Hub 2 (P64H2) Datasheet*
- *Intel® E7501 Memory Controller Hub (MCH) Datasheet*

2.1 Intel® Pentium® M Processor Quadrant Layout

Figure 2 shows the top view of the Intel® Pentium® M Processor quadrant layout.

Figure 2. Intel® Pentium® M Processor Quadrant Layout (Top View)

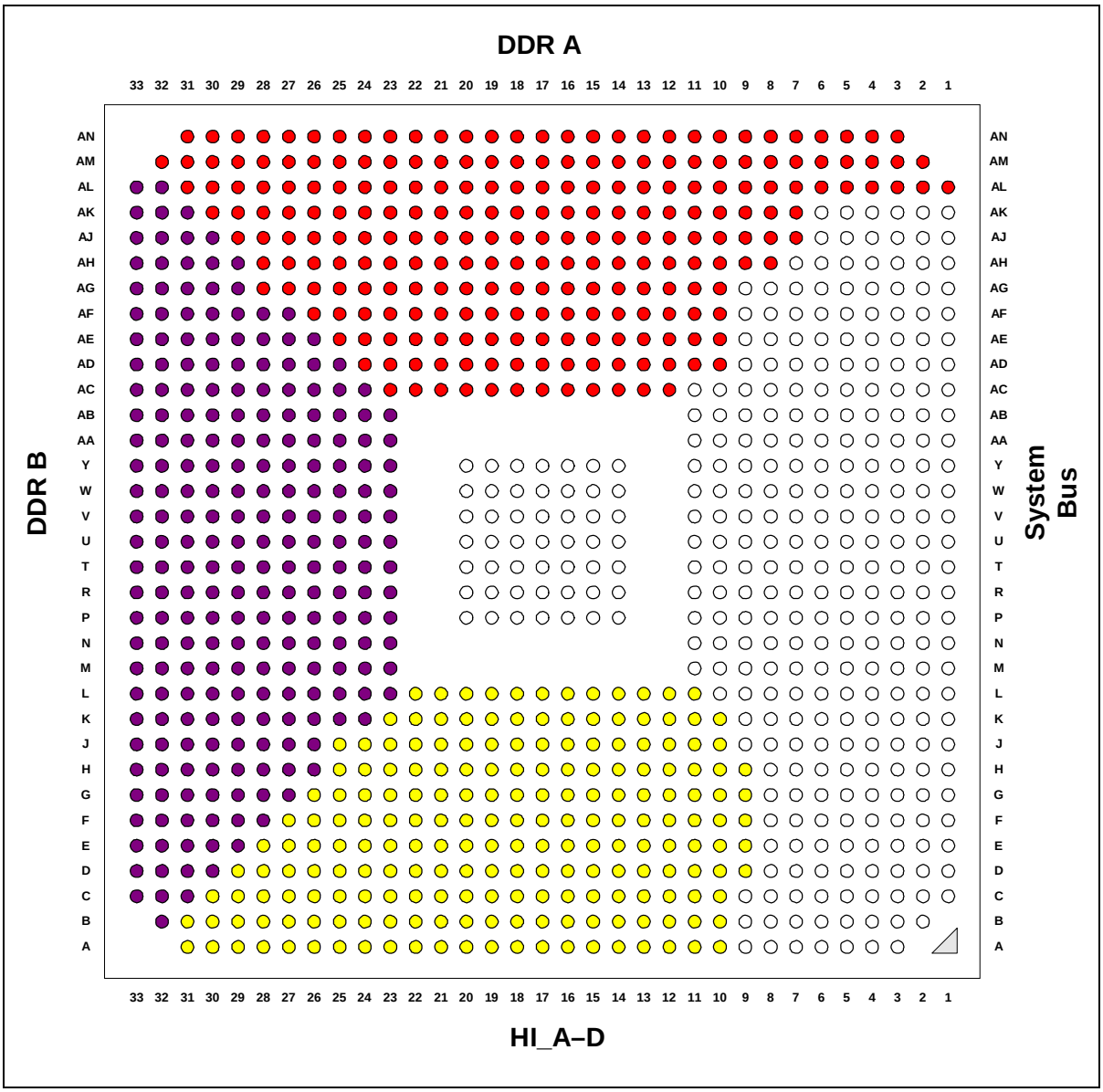


NOTE: Pin B2 is depopulated on the Micro-FCPGA package.

2.2 Intel® E7501 Chipset MCH Quadrant Layout

Figure 3 shows the top view of the Intel® E7501 Chipset MCH quadrant layout.

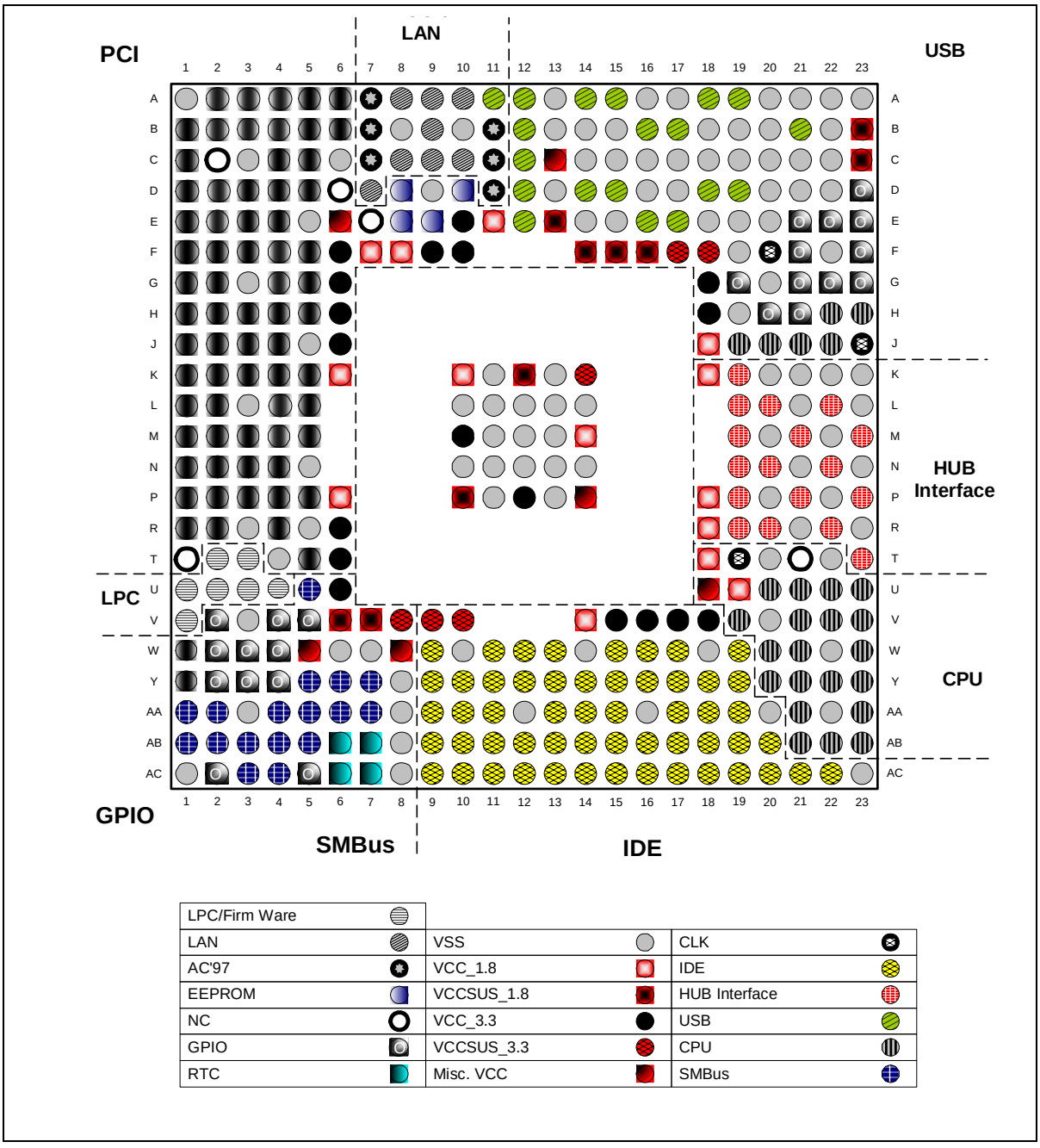
Figure 3. Intel® E7501 Chipset MCH Quadrant Layout (Top View)



2.3 Intel® ICH3-S Quadrant Layout

Figure 4 shows the top view of the Intel® ICH3-S quadrant layout.

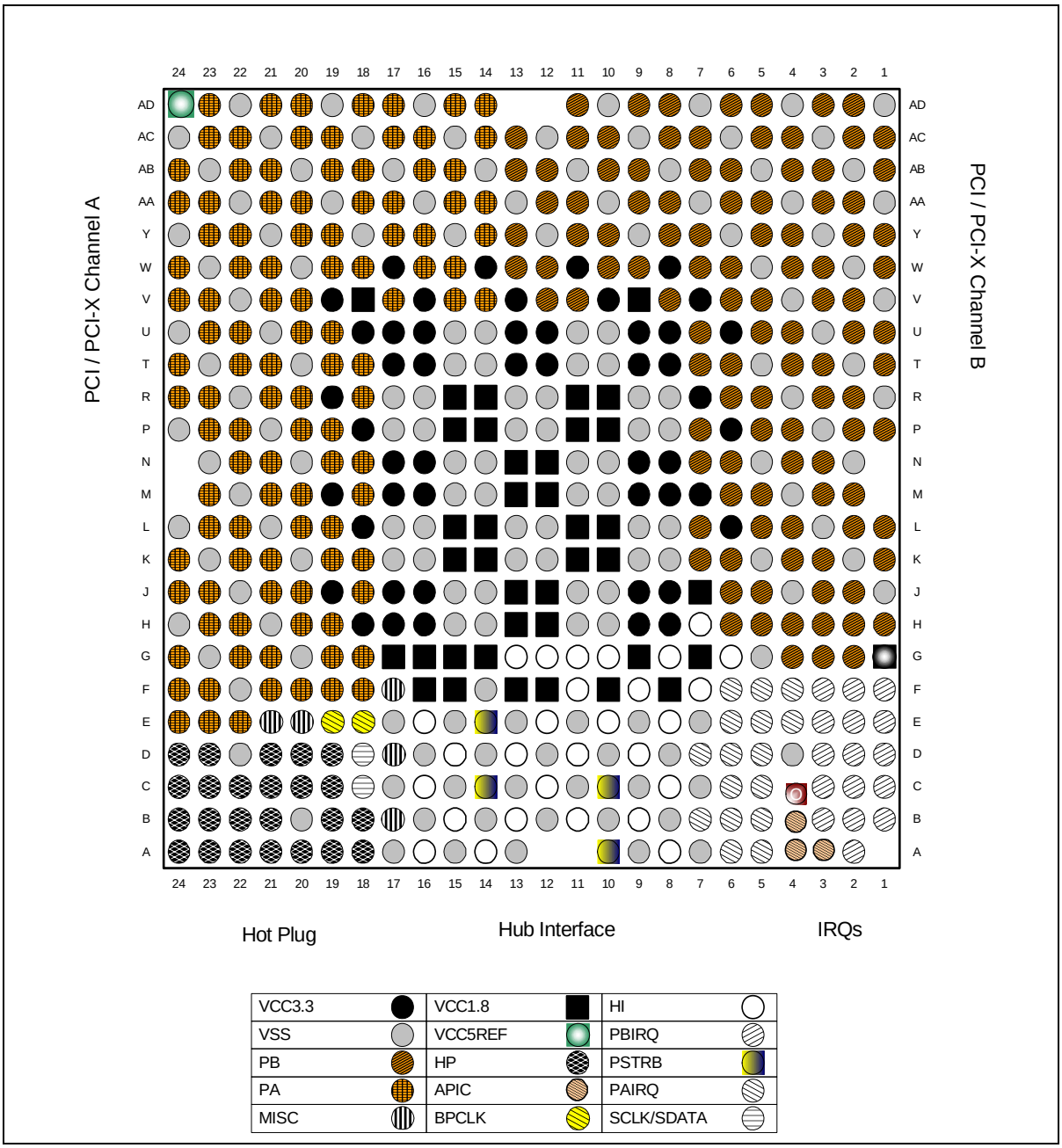
Figure 4. Intel® ICH3-S Quadrant Layout (Top View)



2.4 Intel® P64H2 Quadrant Layout

Figure 5 shows the top view of the Intel® P64H2 quadrant layout.

Figure 5. Intel® P64H2 Quadrant Layout (Top View)



Baseboard Requirements 3

This chapter summarizes the stack-up used for all platform simulations and the placement of components on the motherboard.

3.1 Platform Stack-Up

Figure 6 shows the recommended 10 layer platform stack-up. All layers are 1 oz copper. The processor requires 2 oz of copper to deliver power and 2 oz of copper to deliver ground.

Route signal layers as microstrip on layers 1 and 10. Route signal layers as asymmetric stripline on layers 3, 5, 6 and 8. The signal layers must reference ground on layers 2, 4, 7 or 9 only. Route signals on layers 5 and 6 orthogonally with respect to routes on signal layers to reduce crosstalk between the layers.

Intel strongly recommends that system designers use the stack-up shown in Figure 6 and recommendations in Table 4 when designing their boards. Intel realizes numerous ways exist to achieve these targeted impedance tolerances; contact your board vendor for these specifics. Intel encourages platform designers to perform comprehensive simulation analysis to ensure all timing specifications are met. This is particularly important when a design deviates from the design guidelines provided.

Figure 6. Ten Layer Stack-up, 50 Ω Board with 5-Mil Traces

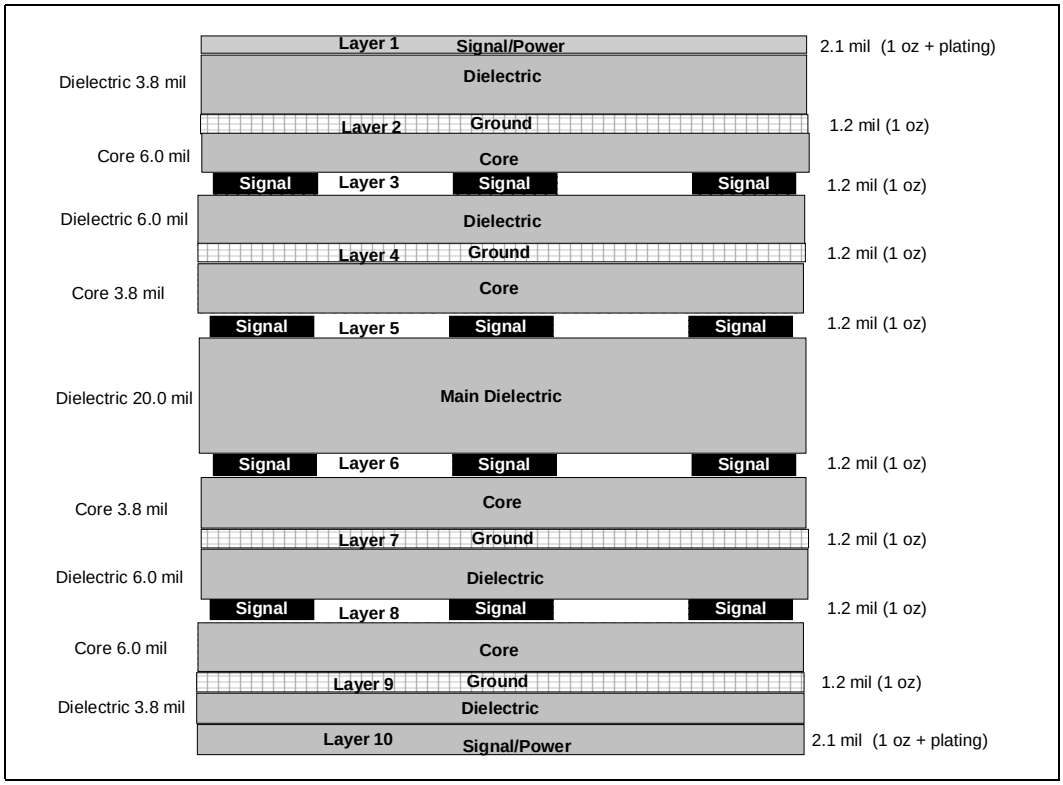


Table 4. Board Requirements

Board Factor	Recommendation
Material	• Standard FR4 Tg 170 Epoxy.
Impedance Requirements	• 50 Ω impedance ± 10% Layers 1, 3, 5, 6, 8 and 10 (except lower left corner SCSI interface). • SCSI interface 83 Ω single-ended, 122 Ω differential pair ± 10% (layer 1 reference layer 3 and layer 10 reference layer 8 using the reference stack-up).
Etch	• 5-mils trace width and space minimum inner/outer. **SCSI interface**: 6-mils separation within a pair, 20-mils space between adjacent pairs.
Finished Via Size	• Minimum via size is 0.014 mil, finished in a 0.025-mil land with 0.035-mil antipad. • Approximately 15,000 plated through holes total.
Finish	• Solder Mask On Bare Copper (SMOBC)
Soldermask Type	• SM-840 minimum web 0.004 mils.
Fabrication	• Edge Routed.
Component Technology	• Through hole / SMT. • QFP, BGA, front side. • Discrete 0603, 0805 back side.

3.2 Processor Thermal Solution Placement and Recommended Keep-Outs

For thermal solution mechanical keep-outs in embedded form factors please refer to the *Intel® Pentium® M Processor for Embedded Applications Thermal Design Guide*.

Platform Clock Routing Guidelines 4

4.1 Platform Clock

To minimize jitter, improve routing, and reduce cost, Intel® E7501 chipset-based systems should use a single chip clock solution, the CK408 or CK408B. The difference between the CK408 and the CK408B is the CK408B provides one additional 100 MHz differential outputs pair. The clock chip provides three (CK408) or four (CK408B) 100 MHz differential output pairs for the processor and MCH, including the ITP connector, and six 66 MHz speed clocks that drive all I/O buses. Figure 7 illustrates the clock architecture. Table 5 presents the CK408 clock groups. Table 6 presents the platform system clock reference. For more information on CK408 or CK408B compliance, contact your Intel representative.

Table 5. CK408 Clock Groups

Clock Group Name	Frequency (MHz)	Receiver
Host_CLK	100	Processor, Debug Port and MCH
CLK66	66	MCH, Intel® ICH3-S, and Intel® P64H2
CLK33_ICH3-S	33	Intel ICH3-S
CLK14	14.318	Intel ICH3-S and SIO
CLK33	33	PCI Connector, SIO, BMC, and FWH
USBCLK	48	Intel ICH3-S

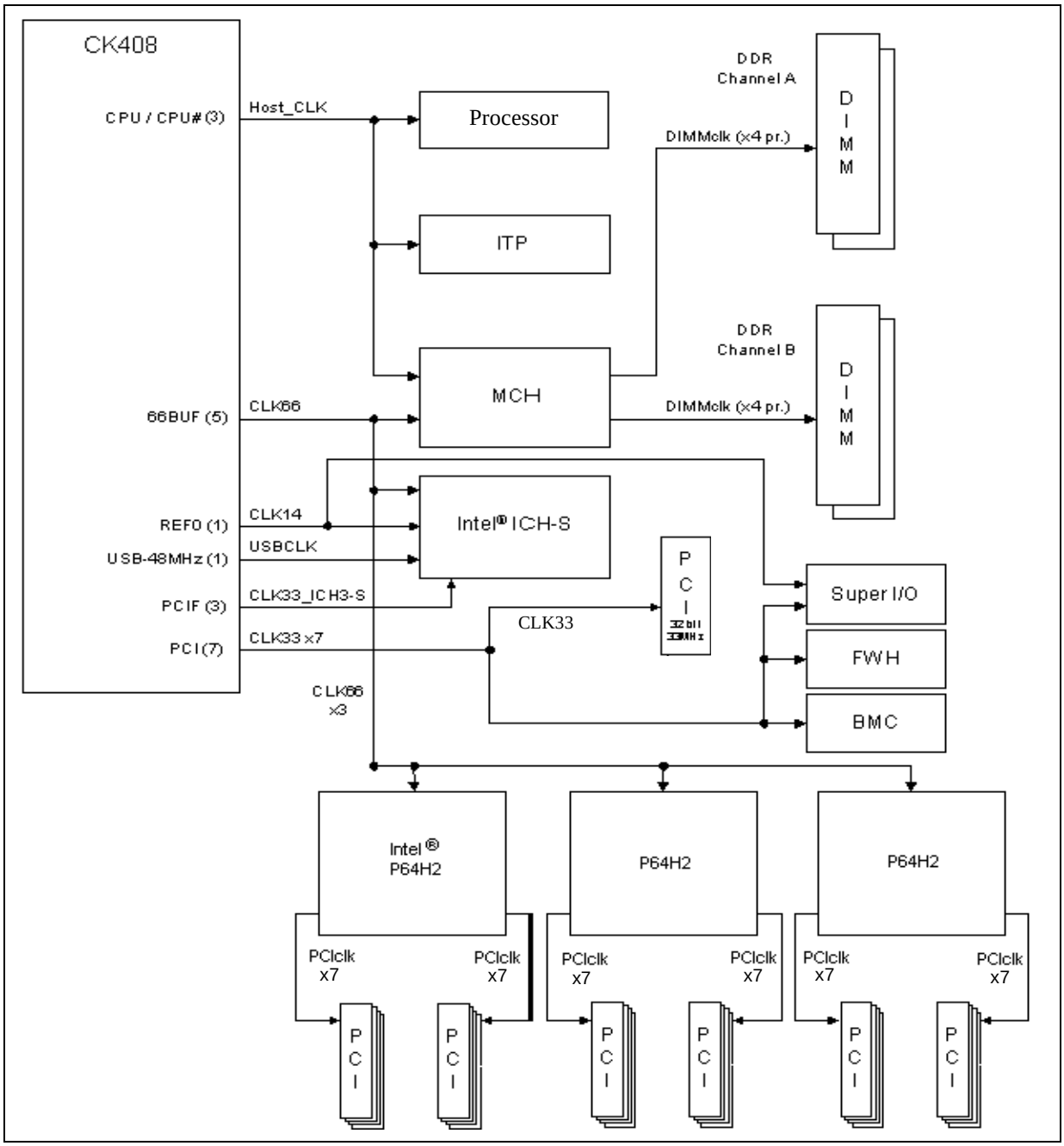
Table 6. Platform System Clock Reference (Sheet 1 of 2)

Clock Group	CK-408 Pin	Component	Component Pin Name
Host_CLK	CPUCLKT<3>	Debug Port	CPUCLKT<3>
	CPUCLKC<3>	Debug Port	CPUCLKC<3>
	CPUCLKT<0>	Processor	CPUCLKT<0>
	CPUCLKC<0>	Processor	CPUCLKC<3>
	CPUCLKT<2>	MCH	CPUCLKT<2>
	CPUCLKC<2>	MCH	FSB_HCLKINN
CLK66	66BUF	MCH	66IN
		Intel® ICH3-S	CLK66
		Intel® P64H2	CLK66
CLK33_ICH3-S	PCIF	Intel ICH3-S	PCICLK
CLK14	REF0	Intel ICH3-S	CLK14
		SIO	CLOCKI
		PCI Video Down	REFCLK
		LPC	LPC_CLK

Table 6. Platform System Clock Reference (Sheet 2 of 2)

Clock Group	CK-408 Pin	Component	Component Pin Name
CLK33	PCI	32-bit PCI Connector	CLK
		PCI Video Down	CLK
		LPC Clock	CLK
		FWH	CLK
		SIO	PCI_CLK
USBCLK	USB-48MHZ	Intel ICH3-S	CLK48

Figure 7. System Clocking Diagram Example



4.2 HOST_CLK Clock Group

The clock synthesizer provides four sets of 100 MHz differential clock outputs. For this platform three sets of 100 MHz differential clock outputs are used. The 100 MHz differential clocks are driven to the Processor, the MCH, and the processor's debug port as shown in Figure 7.

The clock driver differential bus output structure is a Current Mode Current Steering output that develops a clock signal by alternately steering a programmable constant current to the external termination resistors 'Rt'. The resulting amplitude is determined by multiplying IOUT by the value of Rt. The current IOUT is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal may be adjusted for different values of 'R' to match impedances or to accommodate future load requirements. Unused clocks pull-up to V3_3 with a 10 kΩ resistor.

4.2.1 HOST_CLK Clock Topology

The recommended termination for the differential bus clock is a 'Shunt Source Termination'. See Figure 8 for an illustration of this termination scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors 'Rs' provide isolation from the clock driver's output parasitics that would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be selected to match the characteristic impedance of the motherboard, and Rs should be 33 Ω ± 5%. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

- Mult0 pin (pin #43) is pulled-up through a 10 KΩ to VCC setting the multiplication factor 6.
- IREF pin (pin # 42) is connected to ground through a 475 Ω ± 1% resistor – making the IREF 2.32 mA.

Figure 8. Shunt Source Termination

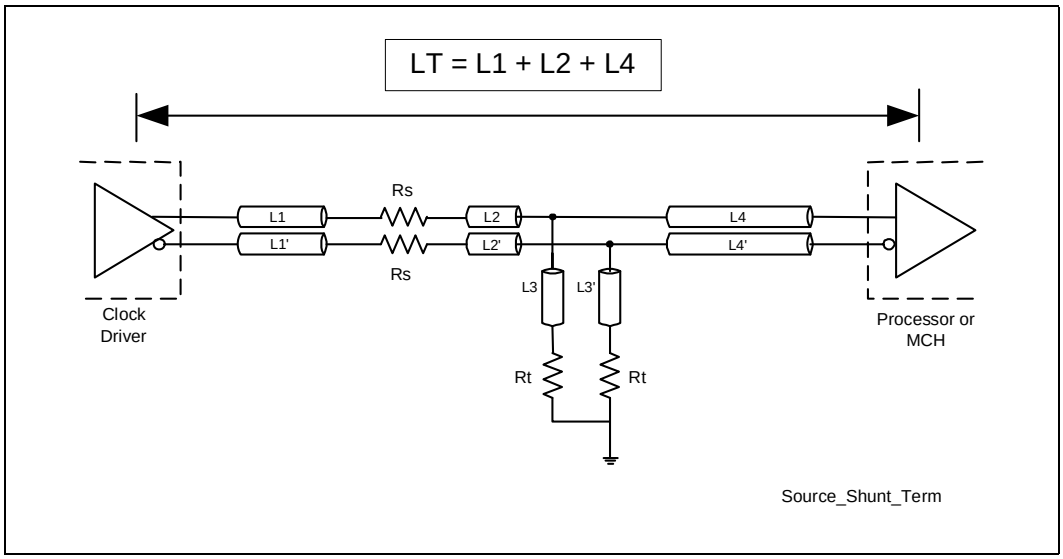


Table 7. HOST_CLK[1:0]# Routing Guidelines (Sheet 1 of 2)

Layout Guideline	Value	Reference	Notes
HOST_CLK Skew between Agents	300 ps total budget: 150 ps for clock driver 150 ps for interconnect	Figure 8 and Figure 9	1,2,3,4
Reference Plane	Ground Referenced (contiguous over the entire length)		
Trace Width	5 mils	Figure 10	7
Differential Pair Spacing	5 mils	Figure 10	5,6
Spacing to Other Traces	25 mils	Figure 10	
Serpentine Spacing	Maintain a minimum S/h ratio of > 26:5.	Figure 10	14
Motherboard Impedance – Differential	100 Ω typical		8
Motherboard Impedance – Single Ended	50 Ω ± 10%		9
Processor, ITP, and MCH Routing Length – L1, L1': Clock Driver to Rs	0 – 0.5“	Figure 8	11
Processor, ITP, and MCH Routing Length – L2, L2': Rs to Rs-Rt Node	0 – 0.2“	Figure 8	11
Processor, ITP, and MCH Routing Length – L3, L3': Rs-Rt Node to Rt	0 – 0.2“	Figure 8	11
Processor, ITP, and MCH Routing Length – L4, L4': Rs-Rt Node to Load	0 – 20“	Figure 8	12
Processor to MCH Length Matching (LT)	-400 mils ± 50 mils (mFCPGA)	Figure 8	10
Processor to ITP Length Matching (LT)	See the *ITP700 Port Design Guide*.	Figure 8	13
HOST_CLKn – HOST_CLKn# (differential pair) Length Matching	± 25 mils		

Table 7. HOST_CLK[1:0]# Routing Guidelines (Sheet 2 of 2)

Layout Guideline	Value	Reference	Notes
Rs Series Termination Value	33 Ω ± 5%	Figure 8	
Rt Shunt Termination Value	49.9 Ω ± 1% (for 50 Ω board impedance)	Figure 8	

NOTES:
1. The skew budget includes clock driver output pair to output pair jitter (differential jitter) and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes clock pairs are routed on a single layer and routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two-bus agents. Measured at the crossing point.
5. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing because this degrades the noise rejection of the network.
7. Set line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack up.
8. The differential impedance of each clock pair is approximately 2*Z single-ended*(1-2*Kb) where Kb is the backwards cross-talk coefficient. For the recommended trace spacing, Kb is very small, and the effective differential impedance is approximately equal to two times the single-ended impedance of each half of the pair.
9. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. When the HOST_CLK traces vary within the tolerances specified, both traces of a differential pair must vary equally.
10. Values are based on the 478-pin Micro-FCPGA socket dimensions/tolerances/parasitics. In general terms, a 4 mm ± 5% socket with a lumped parasitic model. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the system board trace length for the chipset shall be longer than that for the processor (e.g., if Clock Driver-to-MCH = 4.0”, then Clock Driver-to-Process = 3.6” ± 50 mils).
11. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ringback.
12. **Do not change routed layers**. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in Er and the impedance variations due to physical tolerances of circuit board material.
13. When an ITP is implemented, ITP HOST_CLK lengths need to be length matched to the processor HOST_CLK lengths as specified in the *ITP700 Debug Port Design Guide.*
14. Parameter ‘S’ is the distance between the two segments of the serpentined trace. Parameter ‘H’ is the distance between the signal and the referenced plane. The ratio is specified as S/H.

Figure 9. Clock Skew As Measured from Agent to Agent

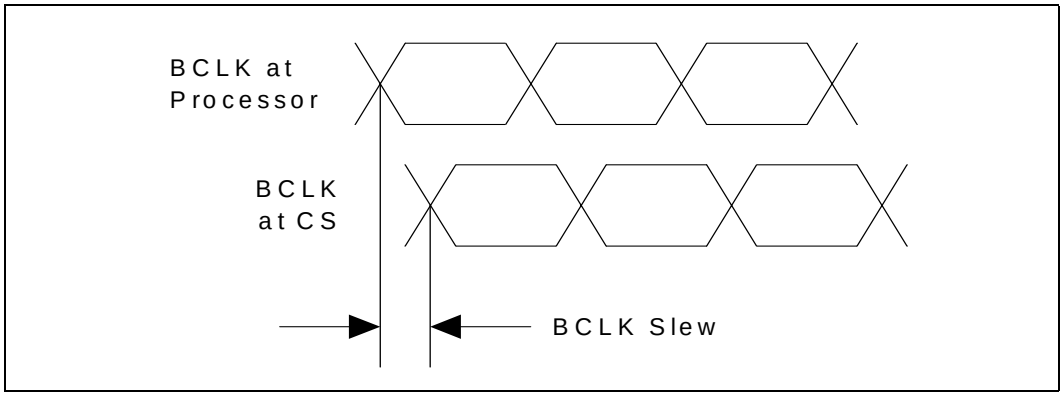
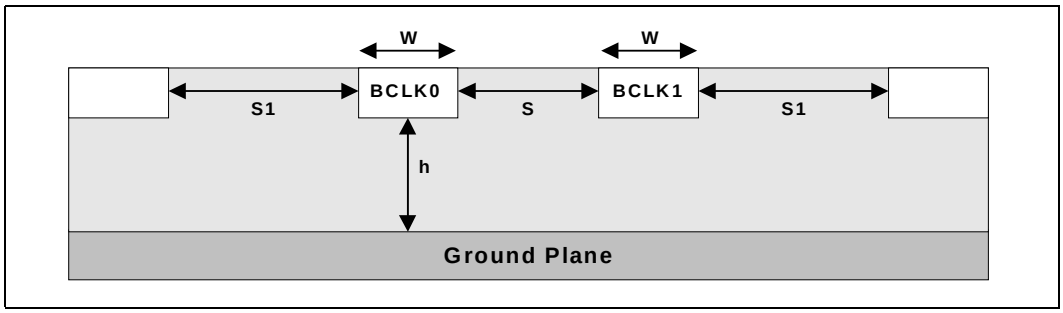


Figure 10. Trace Spacing for HOST_CLK Clocks



4.2.1.1 BCLK Length Matching Requirements (mFCPGA)

To compensate for the extra delay introduced by the processor socket dimensions/tolerances/ parasitics as well as the package parasitics, the Clock Driver-to-MCH (L1 + L2 + L4) motherboard routing will be longer than Clock Driver-to-Processor (L1 + L2 + L4) motherboard routing. **Clock Driver-to-MCH routing should be 400 mils ± 50 mils longer than Clock Driver-to-Processor routing** (i.e., the following relationship should be adhered to):

Clock Driver-to-Processor (L1 + L2 + L4) = Clock Driver-to-MCH (L1 + L2 + L4) – 400 mils ± 50 mils

In order to minimize the clock skew between the processor and the MCH, the L1/L1' segments of the two PSB agents should be exactly trace length matched if possible. The routing should be done such that the shortest L1/L1' segment of the processor is matched within ± 10 mils of the longest L1/L1' segment of the MCH (i.e., the following relationship should be adhered to):

Processor shortest(L1/L1') = MCH longest(L1/L1') ± 10 mils.

Additionally, the routing of each half of the host clock pair for the Intel® Pentium® M processor and MCH should be trace length matched within ± 10 mils of its complement's routing (i.e., the following relationships should be adhered to):

Processor (L1 + L2 + L4) = Processor (L1' + L2' + L4') ± 10 mils

and

MCH (L1 + L2 + L4) = MCH (L1' + L2' + L4') ± 10 mils

4.2.2 HOST_CLK General Routing Guidelines

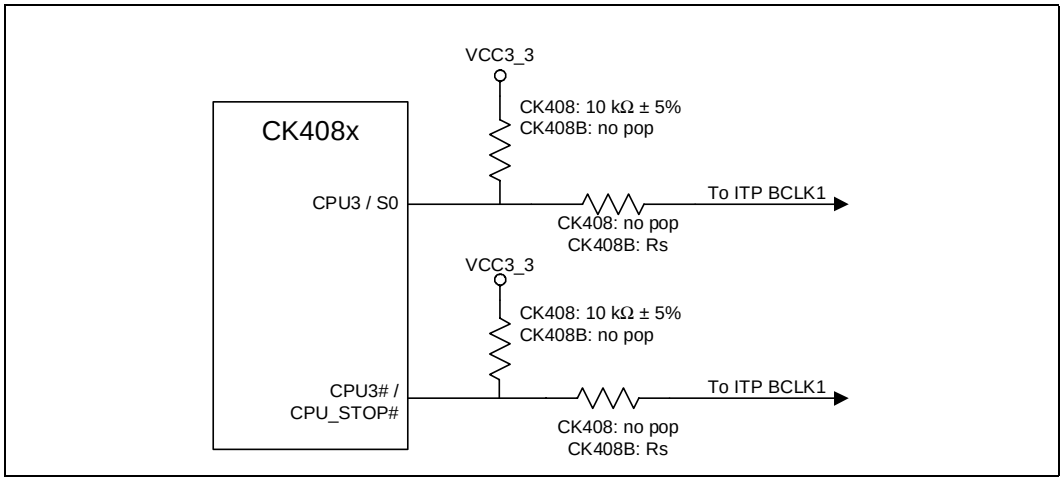
- When routing the differential clocks, do not split up the two halves of a differential clock pair between layers. Route to all agents on the same physical routing layer referenced to ground.
- Do not change routed layers. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in Er and the impedance variations due to physical tolerances of circuit board material.
- Do not place vias between adjacent complementary clock traces, and avoid differential vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias may be placed within length L1, between clock driver and Rs, when needed to shorten length L1.

4.2.3 CK408 vs. CK408B Requirement

The CK408 and CK408B are pin compatible. The only difference between the two chips is the CK408B replaces two signals on the CK408 with a fourth HOST_CLK pair. The fourth HOST_CLK pair is connected to the debug port also known as the In Target Probe (ITP). The ITP is preferred by board designers for preliminary testing and validation. While the CK408B's fourth HOST_CLK pair pins are connected to the ITP, the CK408 pins require the following stuffing options:

- Add one 10 kΩ ± 5% pull-up resistor close to the clock driver before the 33 Ω ± 5% (Rs) (see Figure 11) series resistor on each ITP signal trace (CPU3, CPU3#). This would give the option to use the CK408 instead of the CK408B.
- When using a CK408, the 10 kΩ ± 5% pull-up resistors are the only necessary parts.
- Each unused clock output needs one 10 kΩ ± 5% pull-up resistor close to the clock driver.

Figure 11. Stuffing Options for CK408 and CK408B



4.3 CLK66 Clock Group

In the CLK66 clock group, the driver is the clock synthesizer 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the MCH, Intel ICH3-S, and Intel® P64H2.

Figure 12. Topology for CLK66

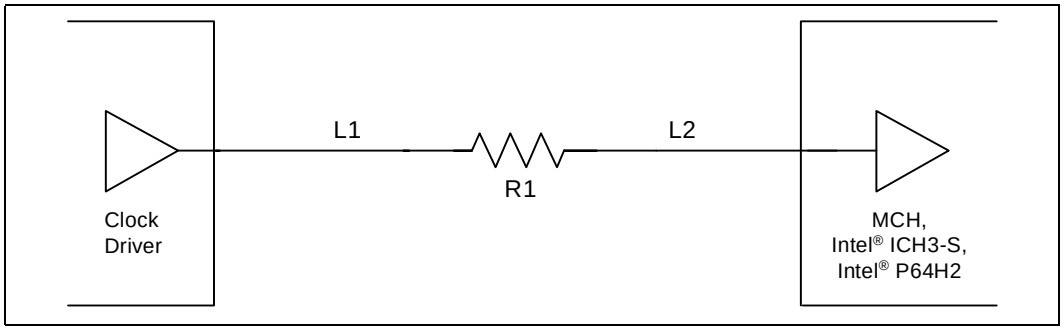


Table 8. CLK66 Routing Guidelines

Parameters	Routing Guidelines
Clock Group	CLK66
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width[3]	5 mils
Trace Spacing[3]	25 mils
Trace Length – L1	0.00 – 0.50”
Trace Length – L2	3.00 – 9.00”
Resistor	R1 = 43 Ω ± 5%
Skew Requirements	All the clocks in the CLK66 group must have < 100-mils skew between each other.
Clock Driver to MCH	X = (3.0 – 9.5”)[1], where X = L1 + L2
Clock Driver to Intel® ICH3-S	X = (3.0 – 9.5”)[1], where X = L1 + L2
Clock Driver to Intel® P64H2	X – 0.34”[2], where X = L1 + L2

NOTES:
1. For better understanding of the concept, refer to Section 4.3.1, “CLK66 Skew Requirements”, Figure 13 and Figure 14.
2. Assuming no connector.
3. All trace width and spacing recommendations are derived from a target impedance and crosstalk sensitivity. This is based upon the stackup defined in Section 3.1. Any deviation from this stackup must be simulated.

4.3.1 CLK66 Skew Requirements

Traces going to the Intel® P64H2 could have up to two connectors. Designers should keep in mind that all total lengths are referenced to the MCH length ('X') and assume no connector. Z is referenced as the card trace length. Each connector is equivalent to 0.60 inch of trace. Adding a single connector on the Intel P64H2 trace would reduce the motherboard trace length by the card length as shown in the following equation and Figure 14:

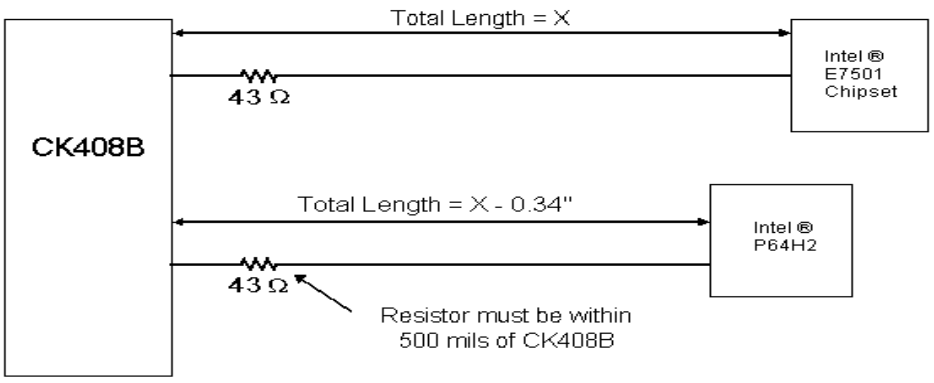
"Z" to X – 0.34" – 0.60" – Z = X – 0.94" – Z

In addition, some OEMs might consider having their adapter card on a PCI extender card (riser), in which case the riser card trace length designator 'Y' should also be accounted for as yet another factor. In this case the last equation would be stated as follows (also see Figure 15):

X – 0.34" – 0.60"– Z – 0.60"– Y = X – 1.54"–Y – Z

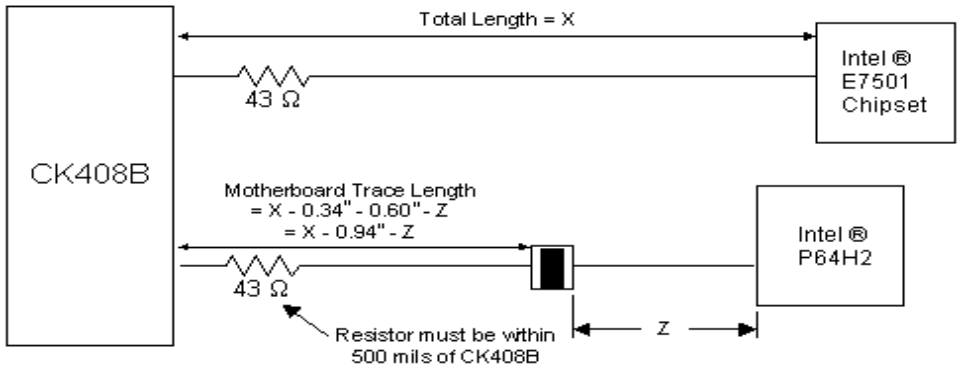
Note that when a riser is used, the motherboard clock trace must be designed for the specific riser card trace length and connector.

Figure 13. Clock Skew Requirements



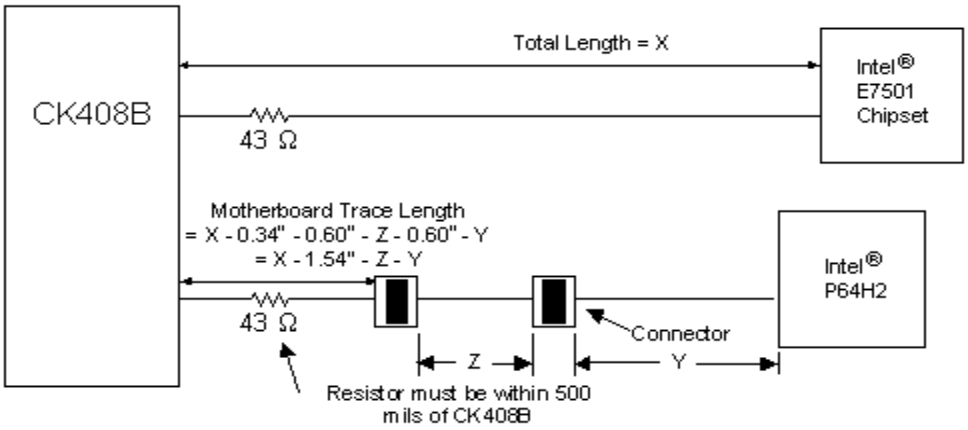
NOTES:
1. All lengths must be matched within 100-mils of target length.
2. 66 MHz clock lines routed with 25-mils isolation from any other signal.
3. Length from CK408 to MCH must be between 3 inches and 9.5 inches.

Figure 14. Example of Adding a Single Connector



NOTES:
1. All lengths must be matched within 100-mils of target length.
2. 66 MHz clock lines routed with 25-mils isolation from any other signal.
3. Length from CK408 to MCH must be between 3 inches and 9.5 inches.
4. Each connector is equivalent to ~ 0.60 inches of trace.
5. Z is the card trace length.

Figure 15. Example of Adding Two Connectors and/or a Riser



NOTES:
1. All lengths must be matched within 100-mils of target length.
2. 66 MHz clock lines routed with 25-mils isolation from any other signal.
3. Length from CK408 to MCH must be between 3 inches and 9.5 inches.
4. Each connector is equivalent to ~ 0.60 inches of trace.
5. Z is the card trace length.
6. Each riser is equivalent to ~0.60 inches + Y where Y is the riser card trace length.
7. The riser must be built with the CLK66 trace length matched to the motherboard routed length.

4.4 CLK33_ICH3-S Clock Group

For the CLK33_ICH3-S clock group, the driver is the clock synthesizer PCIF 33 MHz clock output buffer, and the receiver is the PCICLK 33 MHz clock input buffer at the ICH3-S. Care must be taken to length match this 33 MHz clock with the ICH3-S 66 MHz clock.

Figure 16. Topology for CLK33_ICH3-S

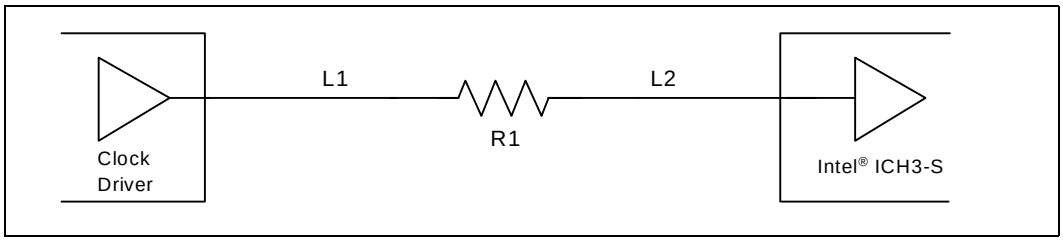


Table 9. CLK33_ICH3-S Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK33_ICH3-S
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width†	5 mils
Trace Spacing†	25 mils
Trace Length – L1	0.00 – 0.50“
Trace Length – L2	3.00 – 9.00“
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	Must be matched to ± 100 mils of CLK66.

† All trace width and spacing recommendations are derived from a target impedance and crosstalk sensitivity. This is based upon the stackup defined in Section 3.1. Any deviation from this stackup must be simulated.

4.5 CLK33 Clock Group

For the CLK33 clock group, the driver is the clock synthesizer 33 MHz clock output buffer, and the receiver is the 33 MHz clock input buffer at the PCI devices on the PCI cards.

Figure 17. Topology for CLK33 to PCI Device Down

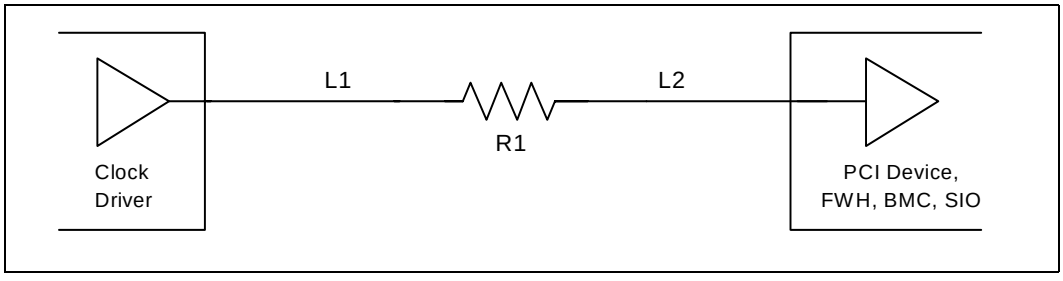


Table 10. CLK33 Routing Guidelines for PCI Device Down

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width†	5 mils
Trace Spacing†	25 mils
Trace Length – L1	0.00 – 0.50“
Trace Length – L2	3.00 – 9.00“
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	PCI device – PCI device skew max allowed by *PCI Local Bus Specification,* Rev 2.2, is 2 ns. Therefore, length match with other CLK33 signals within ± 1 ns.

† All trace width and spacing recommendations are derived from a target impedance and crosstalk sensitivity. This is based on the stackup defined in Section 3.1. Any deviation from this stackup must be simulated.

Figure 18. Topology for CLK33 to PCI Slot

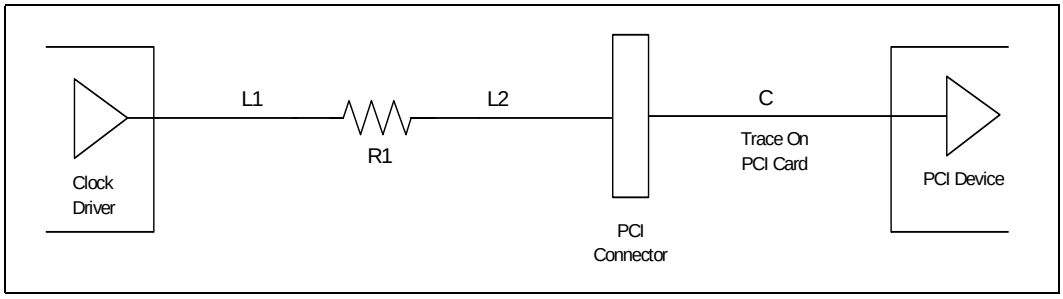


Table 11. CLK33 Routing Guidelines for PCI Slot

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	5 mils
Trace Spacing	10 mils
Trace Length – L1	0.00 – 0.50“
Trace Length – L2	3.00 – 9.00“
Trace Length – C	Routed 2.50 inches per *PCI Local Bus Specification*, Rev 2.2
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	PCI device skew max allowed by *PCI Local Bus Specification,* Rev 2.2, is 2 ns. Therefore, length match with other CLK33 signals within ± 1 ns.

4.6 CLK14 Clock Group

The driver in the CLK14 clock group is the clock synthesizer 14.318 MHz clock output buffer (pin REF0), and the receiver is the 14.318 MHz clock input buffer at the ICH3-S, SIO and LPC.

Figure 19. Topology for CLK14

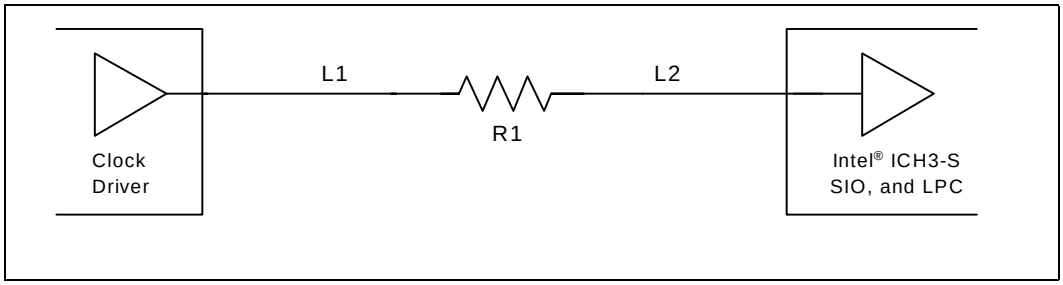


Table 12. CLK14 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK14
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width†	5 mils
Trace Spacing†	10 mils
Trace Length – L1	0.00 – 0.50 inches
Trace Length – L2	3.00 – 9.00 inches
Resistor	R1 = 22 Ω ± 5%
Skew Requirements	None

† All trace width and spacing recommendations are derived from a target impedance and crosstalk sensitivity. This is based upon the stackup defined in Section 3.1. Any deviation from this stackup must be simulated.

4.7 USBCLK Clock Group

For the USBCLK clock group, the driver is the clock synthesizer USB clock output buffer (pin USB-48 MHz), and the receiver is the USB clock input buffer at the ICH3-S (pin CLK48).

Note: This clock is asynchronous to any other clock on the board.

Figure 20. Topology for USB_CLK

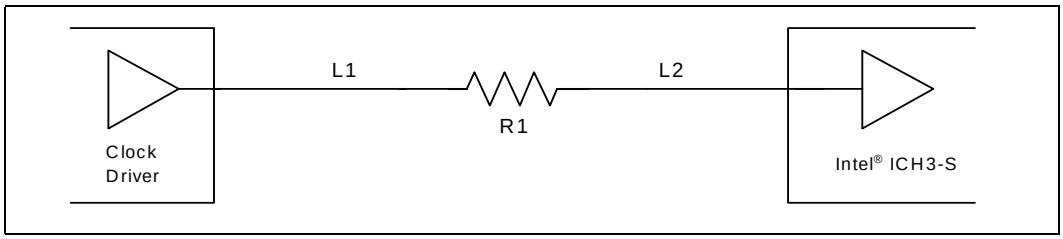


Table 13. USBCLK Routing Guidelines

Parameter	Routing Guideline
Clock Group	USBCLK
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width†	5 mils
Trace Spacing†	25 mils
Trace Length – L1	0.00 – 0.50 inches
Trace Length – L2	3.00 – 12.00 inches
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	None – USBCLK is asynchronous to any other clock on the board

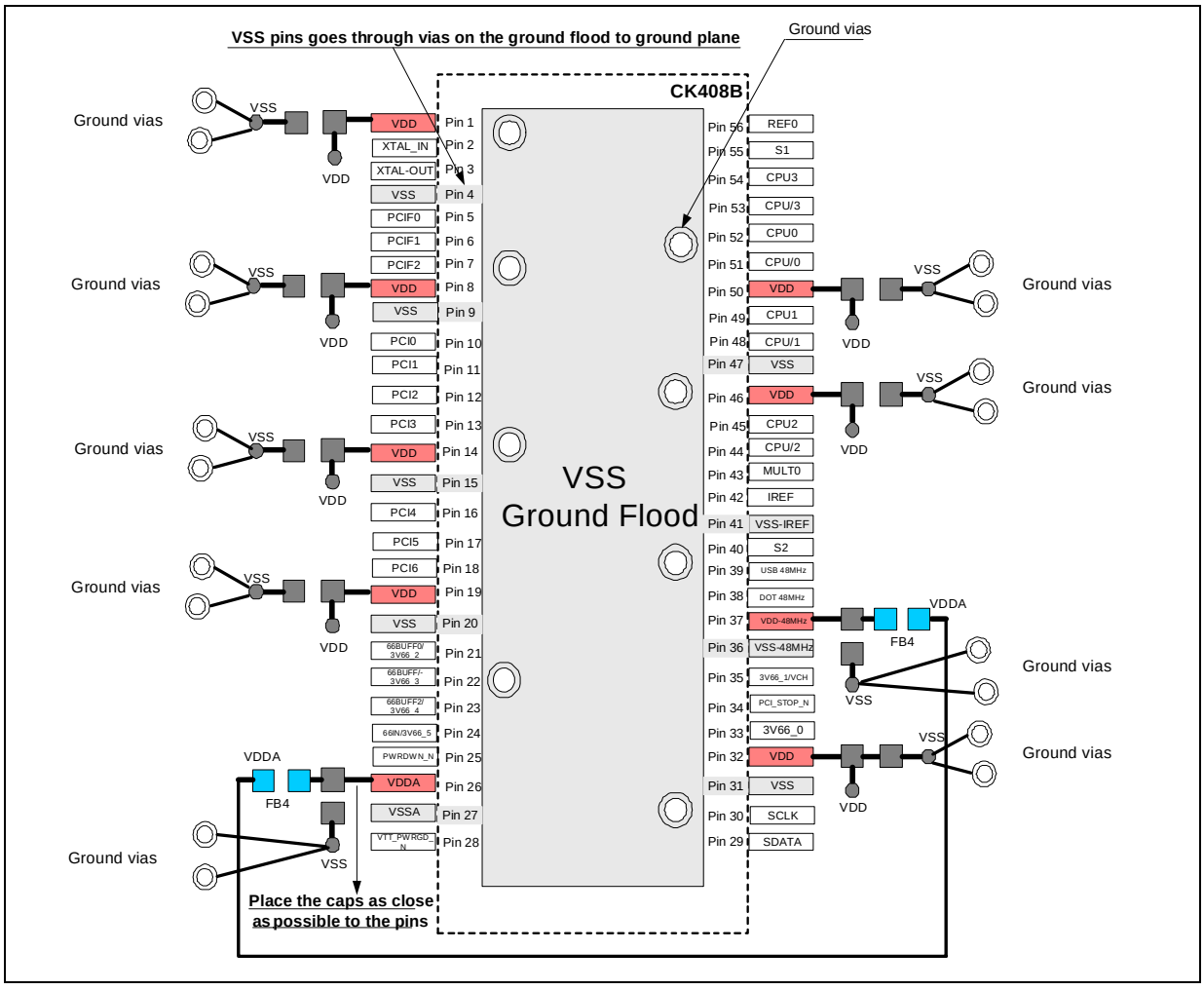
† All trace width and spacing recommendations are derived from a target impedance and crosstalk sensitivity. This is based upon the stackup defined in Section 3.1. Any deviation from this stackup must be simulated.

4.8 Clock Driver Decoupling

The decoupling requirements for a CK408 compliant clock synthesizer are as follows:

- One, 22 µF polarized (decoupling) capacitor placed close to the VDD generation circuitry.
- Eleven, 0.1 µF high-frequency decoupling capacitors placed close to the VDD pins on the clock driver.
- Three, 0.1 µF high-frequency decoupling capacitors placed close to the VDDA pins on the clock driver.
- One, 10 µF polarized (decoupling) capacitor placed close to the VDDA pins on the clock driver.
- One, 0.1 µF high-frequency decoupling capacitor placed close to the VDDA generation circuitry.
- All decoupling capacitors should be placed close to the clock driver pins. Refer to Figure 21.

Figure 21. Decoupling Capacitors Placement and Connectivity



4.9 Clock Driver Power Delivery

Designers must take special care to provide a quiet VDDA supply to the Ref VDD, VDDA and the 48 MHz VDD. These VDDA signals are especially sensitive to switching noise induced by the other VDDs on the clock chip. They are also sensitive to switching noise generated elsewhere in the system such as the processor voltage regulator. It is recommended that a ground flood be placed directly under the clock chip to provide a low inductance connection for the VSS pins. In addition, ground vias should be distributed evenly throughout the ground flood.

Note: For all power connections to planes, decoupling capacitors, and vias, the maximum trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance.

System Bus Routing Guidelines 5

5.1 Intel® Pentium® M Processor System Bus Design Recommendations

For proper operation of the Intel® Pentium® M processor and the Intel® E7501 chipset, it is necessary that the system designer meet the timing and voltage specification of each component. These following recommendations are Intel's recommended guidelines based on extensive simulation and experimentation that make assumptions, which may be different than a customer's system design. The most accurate way to understand the signal integrity and timing of the Intel Pentium M processor system bus in your platform is by performing a comprehensive simulation analysis. It is possible that adjustments to trace impedance, line length, termination impedance, board stack-up, and other parameters may be made to improve system performance.

The following sections discuss the design recommendations for the processor's data, address, and strobe signals.

5.1.1 System Bus Signals

Table 14 lists the system bus signals and their corresponding types. For more signal information refer to the *Intel® Pentium® M Processor Datasheet , Intel® Pentium® M Processor on the 90 nm process with 2-MB L2 cache Datasheet, and the Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet*.

Table 14. System Bus Signal Groups

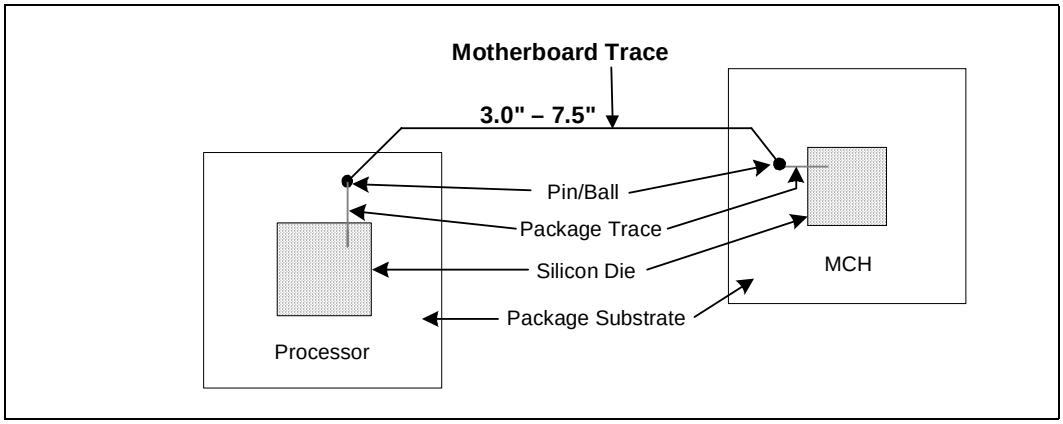
Signal Group	Type	Signals
AGTL+ Common Clock Input	Synchronous to BCLK	BPRI#, DEFER#, RESET#, PREQ#, RS[2:0]#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK	ADS#, BNR#,BPM[3:0]#, BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#
AGTL+ Source Synchronous I/O: 4X Group	Synchronous to assoc. strobe	D[63:0]#, DINV[3:0]#
AGTL+ Source Synchronous I/O: 2X Group	Synchronous to assoc. strobe	A[31:3]#, REQ[4:0]#
AGTL+ Strobes	Synchronous to BCLK [1:0]	ADSTB[1:0]#, DSTBN[3:0]#, DSTBP[3:0]#
Asynchronous GTL+ Input	Asynchronous	A20M#, IGNNE#, INIT#, LINT1/NMI, LINT0/ INTR, SMI#, STPCLK#, SLP#
Asynchronous GTL+ Output	Asynchronous	DBR#, FERR#, IERR#, PROCHOT#, PSI#, THERMTRIP#
System Bus Clock	Clock	BCLK[1:0]
TAP Input	Synchronous to TCK	ITP_CLK[1:0], TCK, TDI, TMS, TRST#
TAP Output	Synchronous to TCK	TDO
Power/Other	Power/Other	GTLREF, COMP[3:0], PWRGOOD, RSVD, TEST[3:1], THERMDA, THERMDC, VCC, VCCA[3:1], VCCP, VCCQ[1:0], VID[5:0], VSS, VCCSENSE, VSSSENSE

5.1.2 Processor System Bus Termination

Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the motherboard for most Intel® Pentium® M processor system bus signals. A simple point-to-point interconnect topology is used in these cases. Figure 22 shows the recommended processor topology used for system bus routing.

In this document the pad is defined as the attach point of the silicon die to the package substrate. The pin/ball is defined as the attach point of the pad to the motherboard. It is also important to remember that package trace length must be factored into total signal length.

Figure 22. Processor System Bus Topology



Refer to Table 15 for a summary of the processor system bus routing recommendations. Use this as a quick reference only. The following sections provide more detailed information for each parameter. Intel strongly recommends simulation of all signals to ensure the design meets setup and hold times.

Table 15. System Bus Routing Summary (Sheet 1 of 2)

Parameter	Platform Routing Guidelines
Trace Width/Spacing	• 5/15 mils or 1:3 ratio with an impedance of 50 Ω ± 10%. • Serpentine ratio of 5:1. See Section 12.3.
Source Synchronous Signal Group	• MCH-to-Processor: 3.0 inches – 7.5 inches pad-to-pad. • Balance trace lengths ± 25 mils with respect to the associated strobes (see Table 18 and Table 20). See Section 12.7 for a detailed description of processor bus tuning. • Route all signals within the same strobe group on the same layer for the entire length of the bus. • Never change layers on source synchronous signals. • Never route over a plane split.
DSTBN[3:0]# / DSTBP[3:0]# and ADSTB[1:0]#	• Follow the same routing rules as the Source Synchronous Signal Group. • Maintain a 25-mil spacing around each strobe signal. • Do not route differentially.

Table 15. System Bus Routing Summary (Sheet 2 of 2)

Parameter	Platform Routing Guidelines
Common Clock Signal	• Follow the same routing rules as the source synchronous Signal Group; however, no length compensation is necessary. • If a layer change must occur, use vias connecting the two reference planes to provide a low impedance path for the return current. Vias should be as close as possible to the signal via.
Routing Requirements	Stripline, ground referenced only.
Motherboard Impedance	50 Ω ± 10%

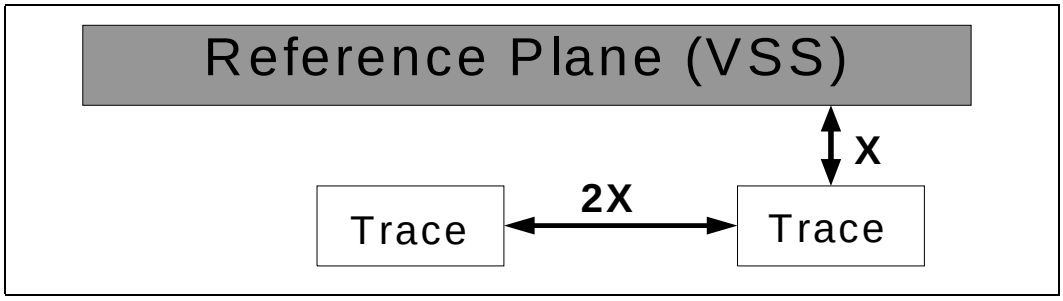
5.1.3 Recommended Stack-up Routing and Spacing Assumptions

The following section describes in more detail the terminology and definitions used for different routing and stack-up assumptions that apply to the recommended motherboard stack-up shown in Figure 6.

5.1.4 Trace Space to Trace - Reference Plane Separation Ratio

Figure 23 illustrates the recommended relationship between the edge-to-edge trace spacing (2X) versus the trace to reference plane separation. An edge-to-edge trace spacing (2X) to trace-reference plane separation (X) ratio of 2:1 ensures a low crosstalk coefficient. All of the effects of crosstalk are difficult to simulate. The timing and layout guidelines for the Intel® Pentium® M processor have been created with the assumption of a 2:1 trace spacing to trace-reference plane ratio. A smaller ratio would have an unpredictable impact due to crosstalk.

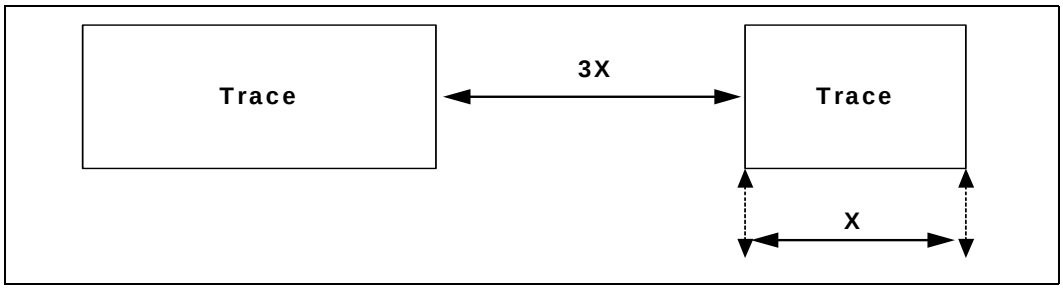
Figure 23. Trace Spacing vs. Trace-Reference Plane Example



5.1.4.1 Trace Space to Trace Width Ratio

Figure 24 illustrates the recommended relationship between the edge-to-edge trace spacing versus trace width ratio for the best signal quality results. In general, a 3:1 trace space to trace width ratio is preferred and highly recommended. In case of routing difficulties on the motherboard, using a 2:1 ratio would be acceptable only when additional simulations conclude that it is possible, which may include some changes to the stack-up or routing assumptions.

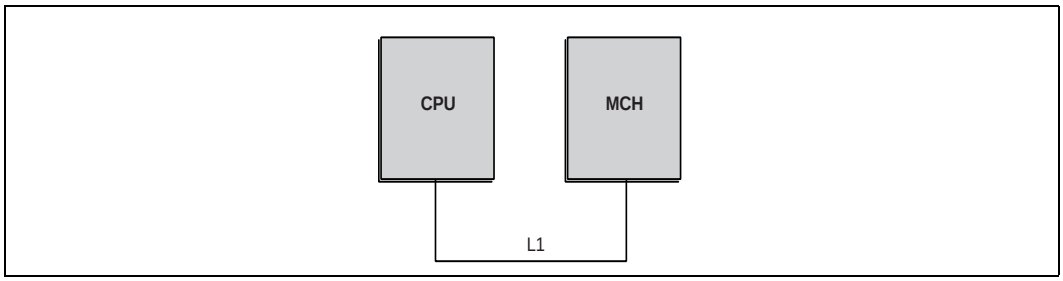
Figure 24. Trace Spacing vs. Trace Width Example



5.1.4.2 Processor RESET# Signal

The RESET# signal is a common clock signal driven by the MCH CPURESET# pin. In a production system where no ITP700FLEX debug port is implemented, a simple point-to-point connection between the CPURESET# pin of the MCH and Intel® Pentium® M processor's RESET# pin is recommended. On-die termination of the AGTL+ buffers on both the processor and the MCH provide proper signal quality for this connection. This is the same case as for the other common clock signals listed in Section 5.1.6, "Common Clock Signals". Follow the same routing guidelines given for common clock signals listed in Section 5.1.6.

Figure 25. Processor RESET# Signal Routing Topology With NO ITP700FLEX Connector



For a system that implements an ITP700FLEX debug port a more elaborate topology is required in order to ensure proper signal quality at both the processor signal pad and the ITP700FLEX input receiver. In this case the topology illustrated in Figure 26 and listed in Table 16 should be implemented.

The CPURESET# signal from the MCH should fork out (do not route one trace from MCH pin and then T-split) towards the processor's RESET# pin as well as towards the R_{tt} and R_S resistive termination network placed next to the ITP700FLEX debug port connector. R_{tt} pulls-up to the VCCP voltage and is placed at the end of the L2 line. R_S should be placed right next to R_{tt} to minimize the routing between them in the vicinity of the ITP700FLEX connector to limit the L3 length. ITP700FLEX operation requires the matching of L2 + L3 - L1 length to the length of the BPM[4:0]# signals length within ± 50 ps.

Currently 1% tolerance resistors are recommended for R_S and R_{tt}. The use of 5% tolerant resistors for these resistors and whether it could provide adequate signal quality performance is under investigation.

Figure 26. Processor RESET# Signal Routing Topology With ITP700FLEX Connector

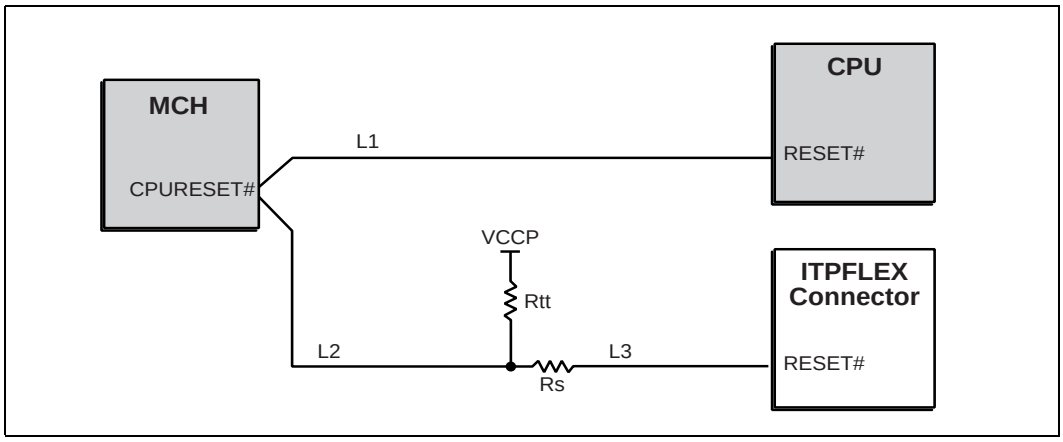


Table 16. Processor RESET# Signal Routing Guidelines with ITP700FLEX Connector

L1	L2+L3	L3	R_S	R_{tt}
3.0” – 7.5”	12.0” max	0.5” max	22.6 Ω ± 1%	54.9 Ω ± 1%

5.1.5 Source Synchronous Signals

All source synchronous signals use an AGTL+ bus driver technology with on-die GTL termination resistors connected in a point-to-point topology between the Intel® Pentium® M processor and the Intel® E7501 MCH. No external termination is needed on these signals. Table 17 list the source synchronous system bus address signals that operate at a double-pumped rate of 200 MHz and the data signals, which operate at a quad-pumped rate of 400 MHz.

Table 17. 2X and 4X Signal Groups

2X Group	4X Group
A[35:3]# REQ[4:0]#	HD[63:0]# DBI[3:0]#

High speed operation of the source synchronous signals requires careful attention to their routing considerations. The following guidelines should be strictly followed, to ensure robust high frequency operation of these signals.

5.1.5.1 Source Synchronous General Routing Guidelines

Source synchronous data and address signals and their associated strobes are partitioned into groups of signals. Flight time skew minimization within the same group of source synchronous signals is a key parameter that allows their high frequency (400 MHz) operation. All the source synchronous signals that belong to **the same group** should be routed on **the same internal layer** for the entire length of the bus. It is OK to split different groups of source synchronous signals between different motherboard layers as long as all the signals that belong to that group are kept on the same layer. Grouping of Intel Pentium M processor system bus source synchronous signals is summarized in and Table 20. This practice results in a significant reduction of the flight time skew

since the dielectric thickness, line width, and velocity of the signals may be uniform across a single layer of the stack-up. A relationship of dielectric thickness, line width, and velocity between layers is not ensured.

The source synchronous signals should be routed as a strip-line on an internal layer with complete reference to ground planes both above and below the signal layer. Routing with references to split planes or power planes other than ground is not allowed. For the recommended stack-up example, see Figure 6.

Skew minimization requires pad-to-pad trace length matching of the Intel Pentium M processor system bus source synchronous signals that belong to the same group including the strobe signals of that group.

5.1.5.2 Source Synchronous – Data

Robust operation of the 400 MHz, source synchronous data signals require tight skew control. For this reason, these signals are split into matched groups as outlined in Table 18. All the signals within the same group must be kept on the same layer of motherboard routing and should be routed to the same pad-to-pad length within ±100 mils of the associated strobes. The two complementary strobe signals associated with each group should be length-matched to each other within ± 25 mils and tuned within ± 25 mils to the average length of the data signals of their associated group. Group-to-group should be length-matched to each other within ±100 mils. This may optimize setup/hold time margin.

Table 18. Intel® Pentium® M Processor System Bus Data Source Synchronous Signal Trace Length Match Mapping

CPU Signal Name	Signal Matching	Strobes Associated with the Group	Strobe Matching
D[15:0]#, DINV0#	± 100 mils	DSTBP0#, DSTBN0#	± 25 mils
D[31:16]#, DINV1#		DSTBP1#, DSTBN1#	
D[47:32]#, DINV2#		DSTBP2#, DSTBN2#	
D[63:48]#, DINV3#		DSTBP3#, DSTBN3#	

1. Strobes of the same group should be trace length-matched to each other within ±25 mils and to the average length of their associated Data signal group.
2. Group-to-group should be length-matched to each other within ±100 mils.

Table 19 lists the source synchronous data signal general routing requirements. Due to the 400 MHz, high frequency operation of the data signals, they must maintain a 1:3 spacing and should be limited to a pad-to-pad trace length minimum of 3.0 inches and maximum of 7.5 inches. The data strobes must also maintain a 1:3 spacing. In this case, the Intel® Pentium® M processor's DSTBN[3:0]# and DSTBP[3:0]# strobe signals must be routed to the Intel® E7501 MCH's HDSTBN[3:0]# and HDSTBP[3:0]# strobe signals with 1:3 spacing from all signals.

Table 19. Intel® Pentium® M Processor System Bus Source Synchronous Data Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Normal Impedance (Ω)	Width and spacing (mils)
CPU	MCH		Min (inches)	Max (inches)		
DINV[3:0]#	DBI[3:0]#	Strip-line	3.0	7.5	50 ± 10%	5 and 15
D[63:0]#	HD[63:0]#					
DSTBN[3:0]#	HDSTBN[3:0]#					
DSTBP[3:0]#	HDSTBP[3:0]#					

5.1.5.3 Source Synchronous – Address

Source synchronous address signals operate at 200 MHz. Thus, their routing requirements are very similar to the data signals. Refer to Section 5.1.5.1, "Source Synchronous General Routing Guidelines" and Section 5.1.5.2, "Source Synchronous – Data" for further details. Table 20 details the partition of the address signals into matched length groups. Due to the lower operating frequency of the address signals, pad-to-pad length matching is relaxed to ± 200 mils. Each group is associated with only one strobe signal. To maximize setup/hold time margin, the address strobes should be trace length-matched to the average trace length of the address signals of their associated group. In addition, each address signal should be trace length-matched within ± 200 mils of its associated strobe signal.

Table 20. Intel® Pentium® M Processor System Bus Address Source Synchronous Signal Trace Length Mismatch Mapping

CPU Signal Name	Signal Matching	Strobe Associated with the Group	Strobe to Associated Address Signal Matching	Notes
REQ[4:0]#, A[16:3]#	± 200 mils	ADSTB0#	± 200 mils	†
A[31:17]#	± 200 mils	ADSTB1#	± 200 mils	†

† ADSTB[1:0]# should be should be trace length-matched to the average length of their associated address signals group.

Table 21 lists the source synchronous address signals general routing requirements. Due to the 200 MHz, high frequency operation of the address signals, they must maintain a 1:3 spacing and trace lengths should be limited to a pad-to-pad trace length minimum of 3.0 inch and a maximum of 7.5 inches. The routing guidelines listed in Table 21 shows the 1:3 spacing for the address signals given a 50 Ω ± 10% characteristic trace impedance. For the address strobes, 1:3 spacing is also required irrespective of the tolerance of the trace impedance.

Table 21. Intel® Pentium® M Processor System Bus Source Synchronous Address Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Normal Impedance (Ω)	Width and spacing (mils)
CPU	MCH		Min (inches)	Max (inches)		
A[31:3]#	HA[31:3]#	Strip-line	3.0	7.5	50 ± 10%	5 and 15
REQ[4:0]#	HREQ[4:0]#					
ADSTB#[1:0]	HADSTB[1:0]#					

5.1.6 Common Clock Signals

All common clock signals use an AGTL+ bus driver technology with on die integrated GTL termination resistors connected in a point-to-point, Zo = 50 Ω, controlled impedance topology between the Intel® Pentium® M processor and the Intel® E7501 MCH. No external termination is needed on these signals. These signals operate at the Intel Pentium M processor system bus frequency of 100 MHz.

Common clock signals should be routed on an internal or external layer while referencing solid ground planes. Based on Intel simulation results, routing on internal or external layers allows for a minimum pad-to-pad motherboard length of 3.0 inches and a maximum of 7.5 inches. Trace length matching for the common clock signals is not required. Intel recommends routing these signals on the same internal or external layer for the entire length of the bus. When routing constraints require routing of these signals with a transition to a different layer, a minimum of one ground stitching via for every two signals should be placed within 100 mils of the signal transition vias.

Routing of the common clock signals should use a minimum of 1:2 trace spacing. This implies a 4 mils trace width with a minimum of 8 mils spacing (i.e., 12 mils minimum pitch) for routing on internal layers. For external layers, route using a 5 mils trace width and a 10 mils minimum spacing (i.e., 15 mils pitch). Break-out routing under the Intel® E7501 MCH or Intel Pentium M processor package outline and nearby vicinity may not allow the implementation of 1:2 trace spacing requirements. Although every attempt should be made to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the MCH and the Intel Pentium M processor package outlines and up to <500 mils outside the outer ball array.

Table 22 summarizes the list of common clock and key routing requirements. RESET# (CPURESET# of MCH) is also a common clock signal but requires a special treatment for the case where an ITP700FLEX debug port is used. See Section 5.1.4.2, “Processor RESET# Signal” on page 60.

Table 22. Intel® Pentium® M Processor System Bus Common Clock Signal Internal Layer Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Normal Impedance (Ω)	Width and spacing (mils)
CPU	MCH		Min (inches)	Max (inches)		
ADS#	ADS#	Strip-line	3.0	7.5	50 ± 10%	4 and 8
BNR#	BNR#					
BPRI#	BPRI#					
BR0#	BREQ0#					
DBSY#	DBSY#					
DEFER#	DEFER#					
DRDY#	DRDY#					
HIT#	HIT#					
HITM#	HITM#					
LOCK#	HLOCK#					
RS[2:0]#	RS[2:0]#					
TRDY#	HTRDY#					
RESET#†	CPURST#					

† For topologies where an ITP700FLEX debug port is implemented, see Section 5.1.4.2, "Processor RESET# Signal" for RESET# (CPURESET#) implementation details.

5.1.7 Asynchronous Signals

5.1.7.1 Topologies

The following sections describe the topologies and layout recommendations for the Asynchronous Open Drain and CMOS signals (see Table 14) found on the platform. All Open Drain signals listed in the following sections below must be pulled-up to V_{CCP} (1.05 V). When any of these Open Drain signals are pulled-up to a voltage higher than V_{CCP}, the reliability and power consumption of the processor may be affected. Therefore, it is very important to follow the recommended termination voltage for these signals.

5.1.7.1.1 Topology 1A: Open Drain (OD) Signals Driven by the Intel® Pentium® M Processor – IERR#

The Topology 1A OD signal IERR# should adhere to the following routing and layout recommendations. Table 23 lists the recommended routing requirements for the IERR# signal of the Intel® Pentium® M processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 50 Ω ± 10% characteristic trace impedance. Series resistor R1 (see Figure 27) is a dampening resistor for reducing overshoot/undershoot reflections on the transmission line. The pull-up voltage for termination resistor R_{tt} is V_{CCP} (1.05 V). Due to the dependencies on system design implementation, IERR# may be implemented in a number of ways to meet design goals. IERR# may be routed as a test point or to any optional system receiver.

Figure 27. Routing Illustration for Topology 1A

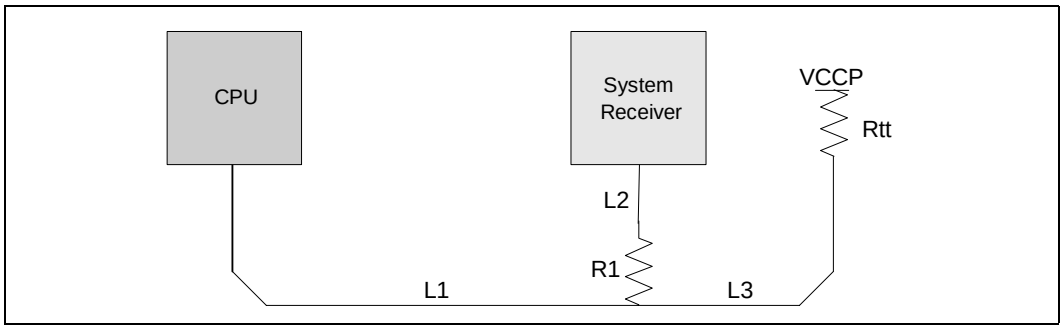


Table 23. Layout Recommendations for Topology 1A

L1	L2	L3	R1	R_{tt}	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	56 Ω ± 5%	56 Ω ± 5%	Micro-strip and Strip-line

5.1.7.1.2 Topology 1B: Open Drain (OD) Signals Driven by the Intel® Pentium® M Processor – FERR# and THERMTRIP#

The Topology 1B OD signals FERR# and THERMTRIP# should adhere to the following routing and layout recommendations. Table 24 lists the recommended routing requirements for the FERR# and THERMTRIP# signals of the Intel Pentium M processor. The routing guidelines allow signals to be routed as either micro-strip or strip-line using 50 Ω ± 10% characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/undershoot reflections on the transmission line. The pull-up voltage for termination resistor R_{tt} is V_{CCP} (1.05 V).

It is recommended that the FERR# signal of the Intel Pentium M processor be routed to the FERR# signal of the Intel ICH3-S. THERMTRIP# may be implemented in a number of ways to meet design goals.

When either FERR# or THERMTRIP# is routed to an optional system receiver and the interface voltage of the optional system receiver does not support a 1.05 V voltage swing, then a voltage translation circuit must be used. When the recommended voltage translation circuit described in Section 5.1.7.2, “Voltage Translation Logic” is used, the driver isolation resistor shown in Figure 32, R_s, may replace the series dampening resistor R1 in Topology 1B. Thus, it is important to note that R1 may no longer be required in such a topology.

Figure 28. Routing Illustration for Topology 1B

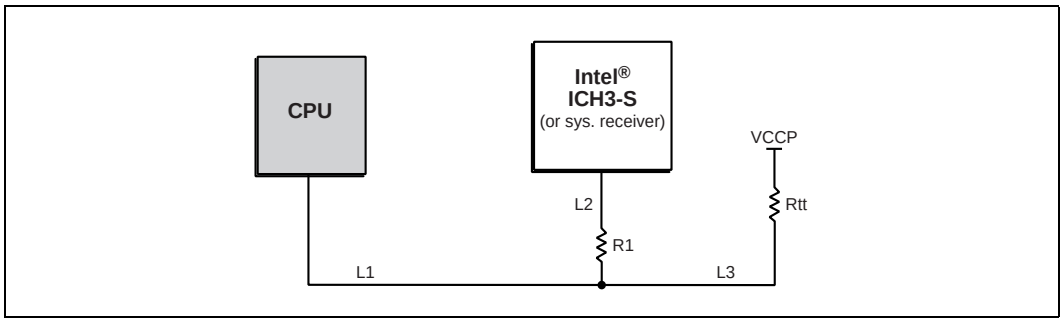


Table 24. Layout Recommendations for Topology 1B

L1	L2	L3	R1	R_{tt}	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	56 Ω ± 5%	56 Ω ± 5%	Micro-strip and Strip-line

5.1.7.1.3 Topology 1C: Open Drain (OD) Signals Driven by the Intel® Pentium® M Processor – PROCHOT#

The Topology 1C OD signal PROCHOT#, should adhere to the following routing and layout recommendations. Table 25 lists the recommended routing requirements for the PROCHOT# signal of the Intel Pentium M processor. The routing guidelines allows the signal to be routed as either a micro-strip or strip-line using 50 Ω ± 10% characteristic trace impedance. Figure 29 shows the recommended implementation for providing voltage translation between the Intel Pentium M processor’s PROCHOT# signal and the ICH3-S or any other system receiver that utilizes a 3.3 V interface voltage (shown as V_IO_RCVR).

Series resistor R_s is a component of the voltage translation logic and serves as a driver isolation resistor. R_s is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of R_s with respect to Q1. The placement of R_s a distance L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 32. R_s should be placed at the beginning of the T-split from the PROCHOT# signal. The pull-up voltage for termination resistor R_{tt} is V_{CCP} (1.05 V).

It is recommended that PROCHOT# be routed to voltage translation logic shown in Figure 29. The receiver at the output of the voltage translation circuit may be the ICH3-S or any optional system receiver that may function properly with the PROCHOT# signal given the nature and usage model of this pin. Intel recommends that the ICH3-S be used as the receiver, thus the translated PROCHOT# signal should be routed to the THRM# signal of the ICH3-S. PROCHOT# is capable of toggling hundreds of times per second to signal a hot temperature condition.

Figure 29. Routing Illustration for Topology 1C

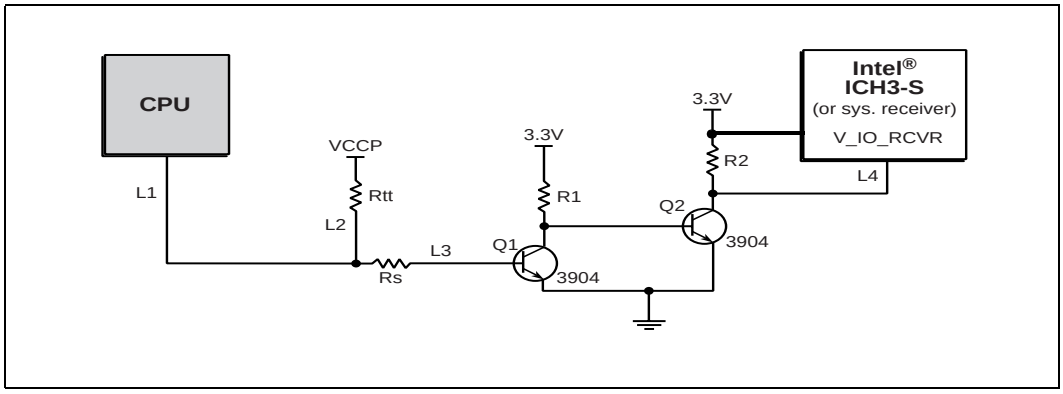


Table 25. Layout Recommendations for Topology 1C

L1	L2	L3	L4	R_S	R1	R2	R_{tt}	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	0.5” – 12.0”	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	56 Ω ± 5%	Micro-strip and Strip-line

5.1.7.1.4 Topology 2A: Open Drain (OD) Signals Driven by ICH3-S – PWRGOOD

The Topology 2A OD signal PWRGOOD should adhere to the following routing and layout recommendations. Table 26 lists the recommended routing requirements for the PWRGOOD signal of the Intel® Pentium® M processor. The routing guidelines allows the signal to be routed as either micro-strip or strip-line using 50 Ω ± 10% characteristic trace impedance. The pull-up voltage for termination resistor R_{tt} is V_{CCP} (1.05 V). Note that the Intel ICH3-S CPUPWRGD signal should be routed point-to-point to the Intel Pentium M processor's PWRGOOD signal. The routing from the Intel Pentium M processor's PWRGOOD pin should fork out to both the termination resistor, R_{tt}, and the ICH3-S. Segments L1 and L2 from Figure 30 should not T-split from a trace from the Intel Pentium M processor pin.

Figure 30. Routing Illustration for Topology 2A

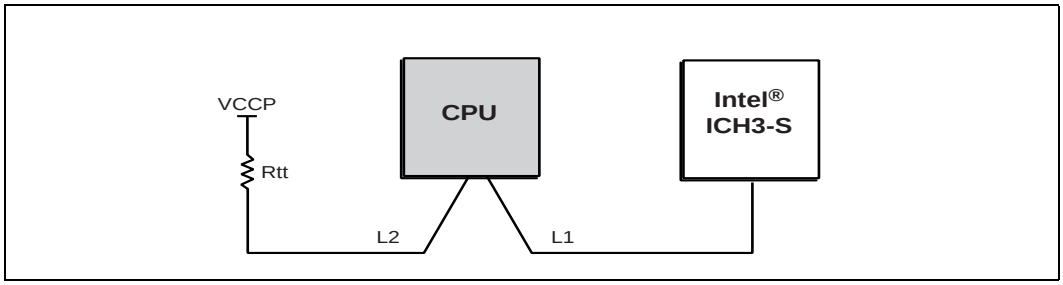


Table 26. Layout Recommendations for Topology 2A

L1	L2	R_{tt}	Transmission Line Type
0.5" – 12.0"	0" – 3.0"	300 Ω ± 5%	Micro-strip and Strip-line

5.1.7.1.5 Topology 2B: CMOS Signals Driven by ICH3-S – LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK#

The Topology 2B CMOS LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK# signals require a 200 Ω ± 5% resistor pull-up to VCCP. should implement a point-to-point connection between the ICH3-S and the Intel® Pentium® M processor with a 200 Ω ± 5% resistor pull-up to VCCP. Additionally the STPCLK# signal requires a 0 Ω resistor placed close to the processor. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 50 Ω ± 10% characteristic trace impedance. No additional motherboard components are necessary for this topology.

Table 27. Layout Recommendations for Topology 2B

L1	Transmission Line Type
0.5" – 12.0"	Micro-strip and Strip-line

5.1.7.1.6 Topology 3: CMOS Signals Driven by ICH3-S to CPU and FWH – INIT#

The signal INIT# should adhere to the following routing and layout recommendations. Table 28 lists the recommended routing requirements for the INIT# signal of the ICH3-S. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 50 Ω ± 10% characteristic trace impedance. Figure 31 shows the recommended implementation for providing voltage translation between the ICH3-S INIT# voltage signaling level and any firmware hub (FWH) that utilizes a 3.3 V interface voltage (shown as a supply V_IO_FWH). See Section 5.1.7.2 for more details on the voltage translator circuit. For convenience, the entire topology and required transistors and resistors for the voltage translator are shown in Figure 31.

Series resistor R_S is a component of the voltage translator logic circuit and serves as a driver isolation resistor. R_S is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance of L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 32. The routing recommendations of transmission line L3 in Figure 31 is listed in Table 28 and Rs should be placed at the beginning of the T-split of the trace from the ICH3-S INIT# pin.

Figure 31. Routing Illustration for Topology 3

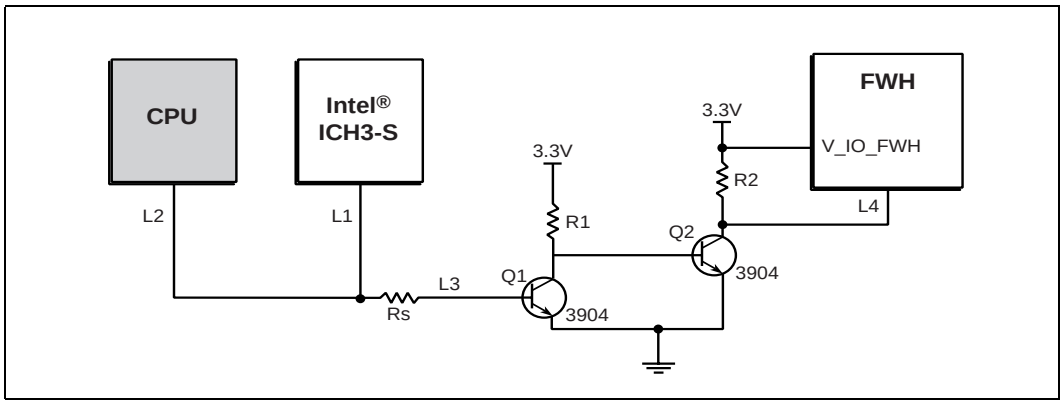


Table 28. Layout Recommendations for Topology 3

L1+L2	L3	L4	R_S	R1	R2	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	0.5” – 6.0”	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	Micro-strip and Strip-line

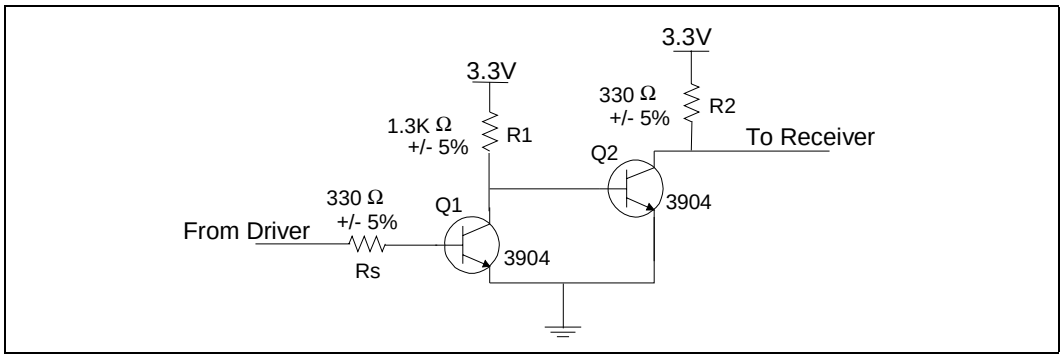
5.1.7.2 Voltage Translation Logic

A voltage translation circuit or component is required on any signals where the voltage signaling level between two components connected by a transmission line may cause unpredictable signal quality. The recommended voltage translation circuit for the platform is shown in Figure 32. For the INIT# signal (see Section 5.1.7.1.6, “Topology 3: CMOS Signals Driven by ICH3-S to CPU and FWH – INIT#”), a specialized version of this voltage translator circuit is used where the driver isolation resistor, R_S, is placed at the beginning of a transmission line that connects to the first bipolar junction transistor, Q1. Though the circuit shown in Figure 32 was developed to work with signals that require translation from a 1.05 V to a 3.3 V voltage level, the same topology and component values, in general, may be adapted for use with other signals as well as providing the interface voltage of the receiver which is also 3.3 V. Any component value changes or component placement requirements for other signals must be simulated in order to ensure good signal quality and acceptable performance from the circuit.

In addition to providing voltage translation between driver and receiver devices, the recommended circuit also provides filtering for noise and electrical glitches. A larger first-stage collector resistor, R1, may be used on the collector of Q1, however, it may result in a slower response time to the output falling edge. In the case of the INIT# signal, resistors with values as close as possible to those listed in Figure 32 should be used without exception.

With the low 1.05 V signaling level of the Intel® Pentium® M processor system bus, the voltage translation circuit provides ample isolation of any transients or signal reflections at the input of transistor Q1 from reaching the output of transistor Q2. Based on simulation results, the voltage translation circuit may effectively isolate transients as large as 200 mV and that last as long as 60 ns.

Figure 32. Voltage Translation Circuit



5.1.8 AGTL+ I/O Buffer Compensation

The Intel Pentium M processor has four compensation pins, COMP[3:0]. Refer to the *Intel® Pentium® Pentium M Processor Datasheet* for additional details on resistive compensation. The Intel® E7501 MCH has two compensation pins, HXRCOMP and HYRCOMP that require compensation resistors to adjust the AGTL+ I/O buffer characteristics to specific board and operating environment characteristics. Also, the MCH requires two special reference voltage generation circuits to pins HXSWNG and HYSWNG for the same purpose described above.

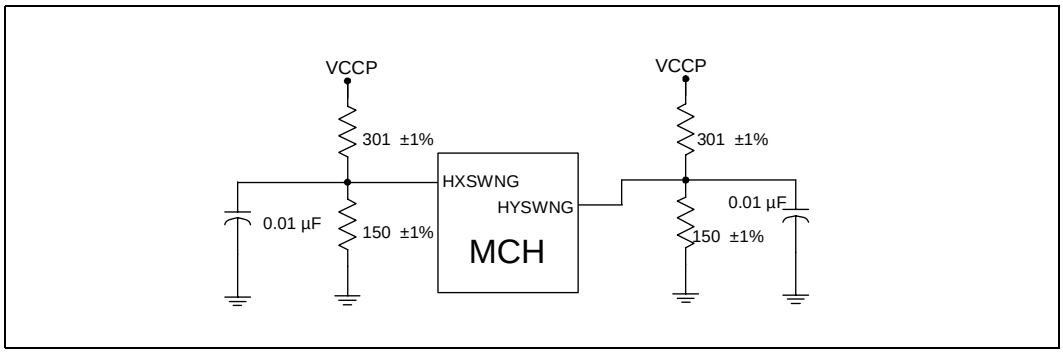
5.1.8.1 Intel® Pentium® M Processor AGTL+ I/O Buffer Compensation

For the Intel® Pentium® M processor, the COMP[2] and COMP[0] pins must each be pulled-down to ground with 27.4 Ω ± 1% resistors and should be connected to the Intel Pentium M processor with a trace impedance of 27.4 Ω. The resistor must be less than 0.5 inches from the processor pins. The COMP[3] and COMP[1] pins must each be pulled-down to ground with 54.9 Ω ± 1% resistors and should be connected to the Intel Pentium M processor with a trace impedance of 54.9 Ω trace. The resistor must be less than 0.5 inches from the processor pins. COMP[3:0] traces should be at least 25 mils (> 50 mils preferred) away from any other toggling signal.

5.1.8.2 Intel® E7501 Chipset AGTL+ I/O Buffer Compensation

For the Intel® E7501 MCH, terminate the HXRCOMP and HYRCOMP with their own 24.9 Ω ± 1% resistor pull-down to ground. Terminate the MCH HXSWNG and HYSWNG using a resistor divider circuit (see Figure 33).

Figure 33. Resistor Divider Circuit For The MCH's HXSWNG And HYSWNG



5.1.9 Intel® Pentium® M Processor System Bus Strapping

The Intel® Pentium® M processor has pins that require termination for proper component operation.

1. For the Intel Pentium M processor, a stuffing option should be provided for the TEST[3:1] pins to allow a 1 kΩ ± 5% pull-down to ground for testing purposes. **For proper processor operation with the E7501 chipset, only the TEST[1] pin resistor should be stuffed, while the TEST [3:2] resistors should remain unstuffed.** Resistors for the stuffing option on these pins should be placed within 2.0 inches of the Intel Pentium M processor.
2. The Intel Pentium M processor's ITP signals, TDI, TMS, TRST and TCK should assume default logic values even when the ITP debug port is not used. The TDO signal may be left open or no connect in this case. Table 29 summarizes the default strapping resistors for these signals. These resistors should be connected to the Intel Pentium M processor within 2.0 inches from their respective pins. It is important to note that Table 29 is applicable only when the onboard ITP nor ITP interposer will not be used. (See chapter 10 for more information on ITP implementation).

Table 29. ITP Signal Default Strapping When ITP Debug Port Not Used

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150Ω ± 5%	VCCP	Within 2.0" of the CPU
TMS	39Ω ± 5%	VCCP	Within 2.0" of the CPU
TRST#	680Ω ± 5%	GND	Within 2.0" of the CPU
TCK	27Ω ± 5%	GND	Within 2.0" of the CPU
TDO	Open	NC	N/A

5.1.10 Intel® Pentium® M Processor $V_{CCSENSE}$/$V_{SSSENSE}$ Design Recommendations

The $V_{CCSENSE}$ and $V_{SSSENSE}$ signals of the Intel® Pentium® M processor provide isolated, low impedance connections to the processor's core power (V_{CC}) and ground (V_{SS}). These pins may be used to sense or measure power (V_{CC}) or ground (V_{SS}) near the silicon with little noise. To make them available for measurement purposes, it is recommended that $V_{CCSENSE}$ and $V_{SSSENSE}$ both be routed with a Zo = 50 Ω ± 10% trace of equal length. Use 3:1 spacing between the routing for the two signals and all other signals should be a minimum of 25 mils (preferably 50 mils) from $V_{CCSENSE}$ and $V_{SSSENSE}$ routing. Terminate each line with an optional (default is No Stuff) 54.9 Ω ± 1% resistor. Also, a ground via spaced 100 mils away from each of the test point vias for $V_{CCSENSE}$ and $V_{SSSENSE}$ should be added. A third ground via should also be placed in between them to allow for a differential probe ground.

Memory Interface Routing Guidelines 6

This chapter documents the configurations Intel simulated to support the memory routing guidelines detailed in the following sections. The customer should simulate any deviations from these recommendations.

In this platform the Intel® E7501 MCH memory interface supports DDR200 and may operate in a dual or single DDR channel configuration. These configurations are defined as follows:

- Dual channel configuration: The MCH consist of two DDR memory channels, channels A and B, that operate in 'lock-step'. Each channel consists of 64 data and eight ECC bits. Logically, this is one, 144-bit wide memory bus; however, each channel is separate electrically.
- Single channel configuration: The MCH consists of one DDR memory channel, channel A. The channel consists of 64 data and eight ECC bits.

Note: Channel B will not operate in single channel mode.

To differentiate between dual and single channel requirements this chapter is divided into two sections:

- Section 6.3, "Dual Channel DDR Overview" describes the requirements for a dual channel configuration.
- Section 6.4, "Single Channel DDR Overview" describes the requirements for a single channel configuration.

Each section covers it's associated routing guidelines for the memory interface. Note that these guidelines apply to channel A and channel B for dual channel operation or channel A for single channel operation.

Each DDR interface has six signal types: Command Clocks, Source Clocked Signals, Source Synchronous Signals, Chip Selects, Clock Enable, and DC Biasing. Refer to the *Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet* for details on the signals.

Table 30. DDR Channel Signal Groups (Sheet 1 of 2)

Group	Signal
Source Synchronous Signals	DQS_x[17:0] DQ_x[63:0] CB_x[7:0]
Command Clocks	CMDCLK_x[3:0] CMDCLK_x[3:0]#
Source Clocked Signals	MA_X[12] RAS_x# CAS_x# WE_x# BA_x[1:0]

Table 30. DDR Channel Signal Groups (Sheet 2 of 2)

Group	Signal
Source Synchronous Signals	DQS_x[17:0] DQ_x[63:0] CB_x[7:0]
Command Clocks	CMDCLK_x[3:0] CMDCLK_x[3:0]#
Chip Selects	CS_x#[7:0]
Clock Enable	CKE_x
DC Biasing	See Table 38

6.1 DDR Channel Impedance Requirements

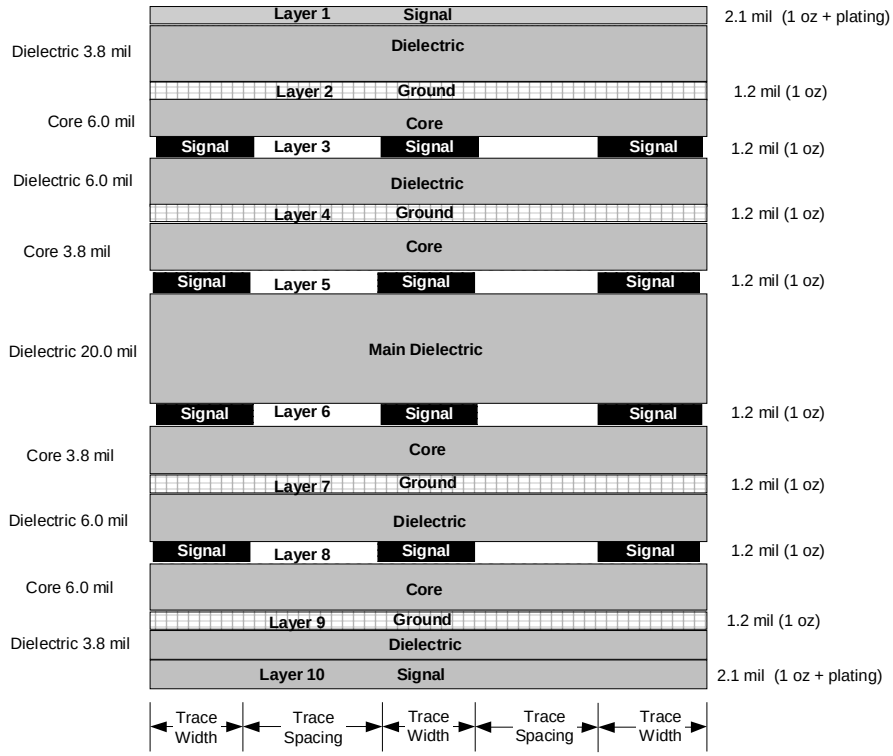
Some DDR channel signal groups require different widths depending on the trace impedance needed for that signal. The following sections in this chapter will detail the recommended impedance for each DDR channel signal group. Table 31 indicates the impedances for the trace widths. Figure 34 shows the trace width and spacing for all DDR signals.

Table 31. Trace Width to Impedance Requirements

Trace Width	Nominal Trace Impedance (Z_0)
4 mils	55 Ω ± 10%
5 mils†	50 Ω ± 10%
6 mils	45 Ω ± 10%
7.5 mils	40 Ω ± 10%

† Spacing is 7.5 mils with a differential impedance of 100 Ω ± 10%.

Figure 34. Trace Width and Spacing for All DDR Signals Except CMDCLK_x[3:0]/ CMDCLK_x[3:0]#

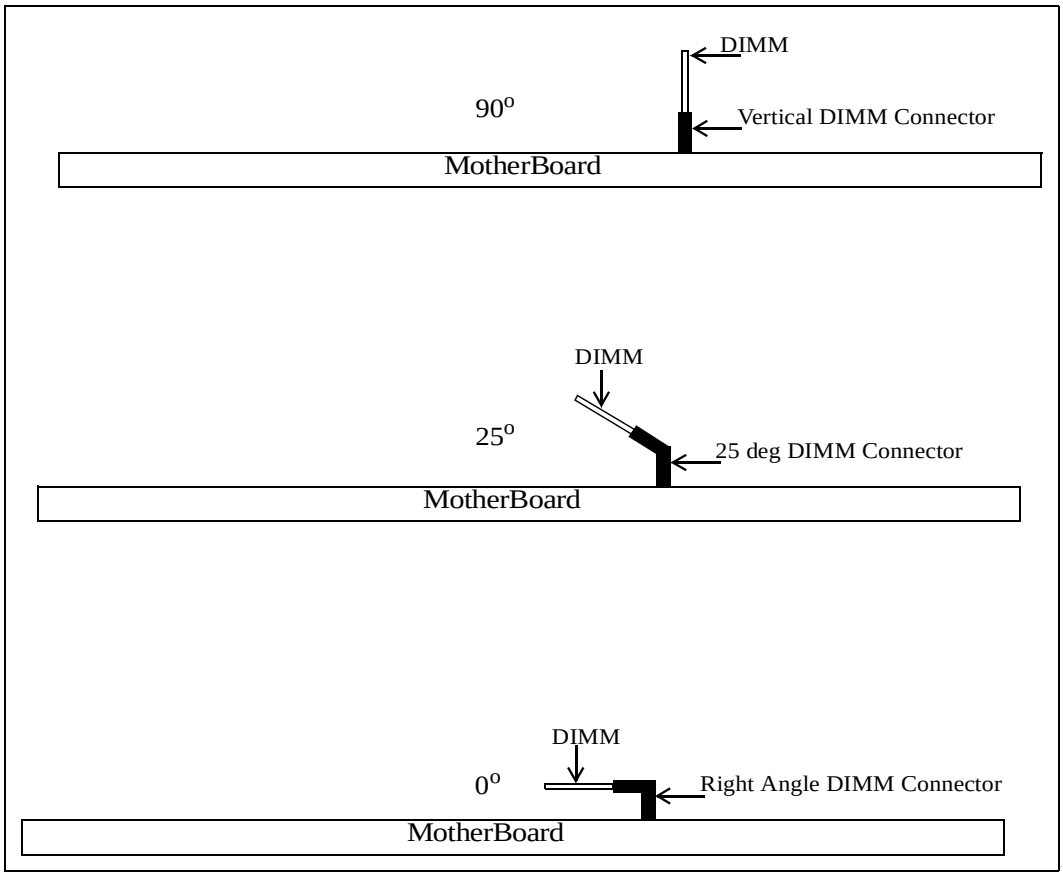


NOTE:
1. Traces on layers 5 and 6 must be routed orthogonally to each other to minimize the effects of crosstalk.
2. Trace width and spacing varies depending on the memory signal group. This chapter will detail the requirements for all the memory signal groups.

6.2 DIMM Types

To allow flexibility in platform design this design guide supports three different DIMM connector types: vertical, 25-degree and right-angle (see Figure 35). Routing guidelines are provided for each DIMM connector type in the following sections.

Figure 35. DIMM Connector Styles Supported



6.3 Dual Channel DDR Overview

In a dual channel DDR configuration, channel A and B are active and operate in lock-step which logically appears to be one 144-bit wide memory bus; however, each channel is separate electrically.

Figure 36 and Figure 37 show both channels being routed to a single bank of DIMMs. The letters ‘A’ and ‘B’ in the figures refer to the DIMM channel. The number following ‘A’ or ‘B’ refers to the DIMM logical group. The DIMMs are physically interleaved. Intel recommends using this interleaving, starting with Channel B closest to the MCH, for optimal routing.

The platform requires DDR DIMMs to be populated in-order, starting with the DIMMs furthest from the MCH in a ‘fill-farthest’ approach (see Figure 37). In addition, single rank DIMMs should be populated furthest when a combination of single ranked and double ranked DIMMs are used. This recommendation is based on the signal integrity requirements of the DDR interface. Intel’s recommendation is to check for correct DIMM placement during BIOS initialization. Additionally, it is strongly recommended that all designs follow the DIMM ordering, SMBus Addressing, Command Clock routing and Chip Select routing documented in Figure 36 and Figure 37. This addressing must be maintained to be compliant with the reference BIOS code supplied by Intel.

Figure 36. 1-DIMM per Channel Implementation

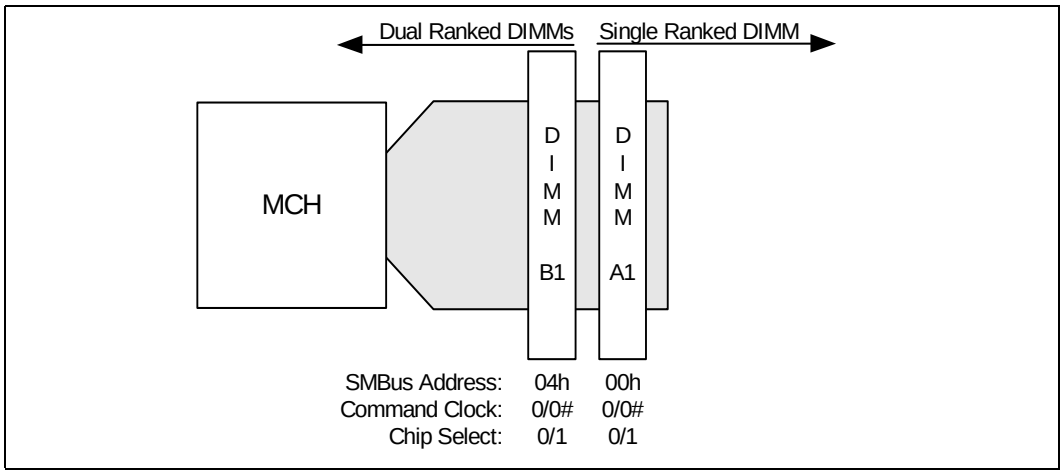
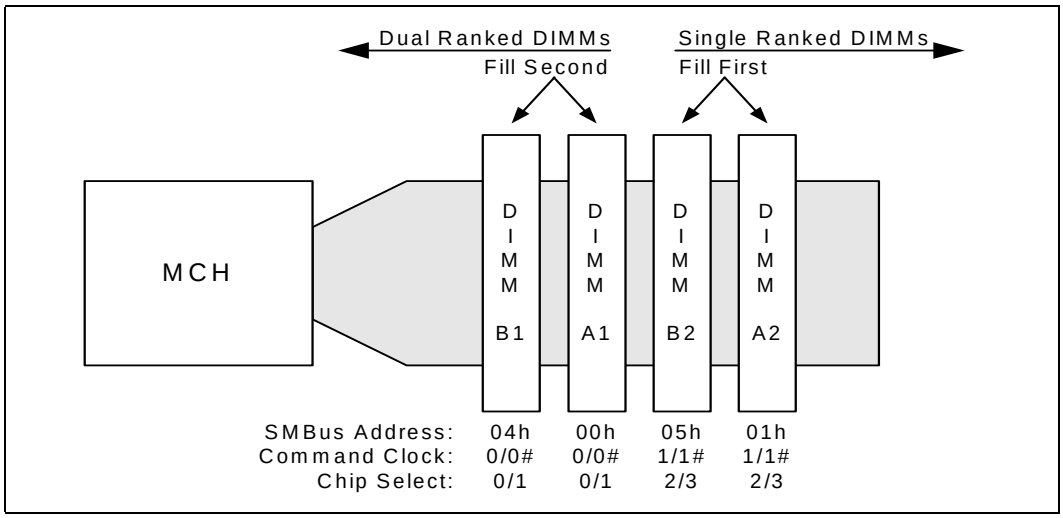


Figure 37. 2-DIMMs per Channel Implementation



Certain combinations of DIMM types in 3-DIMM and 4-DIMM per channel systems have been found to violate the JEDEC write ring back measurement specification. One-DIMM and 2-DIMM per channel systems do not violate the JEDEC write ring back specification. When combining double-rank DIMMs (x4 or x8) with single-rank DIMMs (x4 or x8), if the first populated slot (closest to the MCH) contains a single-ranked DIMM, the write ringback at that DIMM violates the JEDEC DRAM specification (see Figure 39). To reduce write ring back, populate single-ranked DIMMs furthest from the MCH when a combination of single-ranked and double-ranked DIMMs is used (see Figure 38).

To determine if a registered DDR DIMM is a single-bank DIMM or a double-bank DIMM, contact your local Intel representative for more information.

Figure 38. Example of Proper Single and Dual Rank Mixing

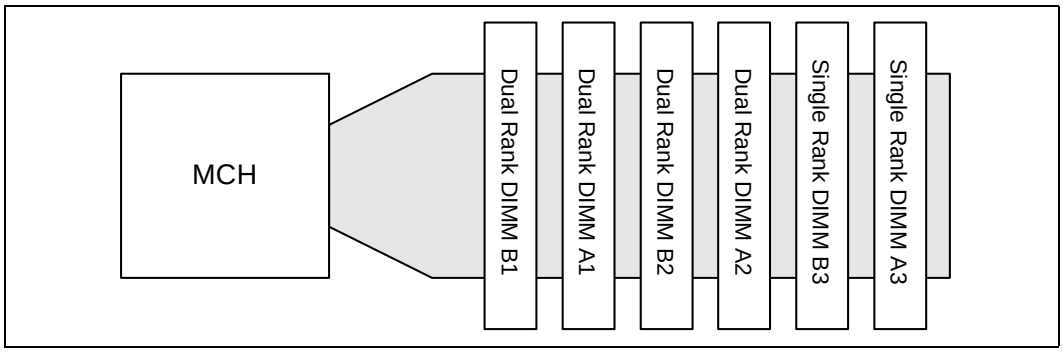
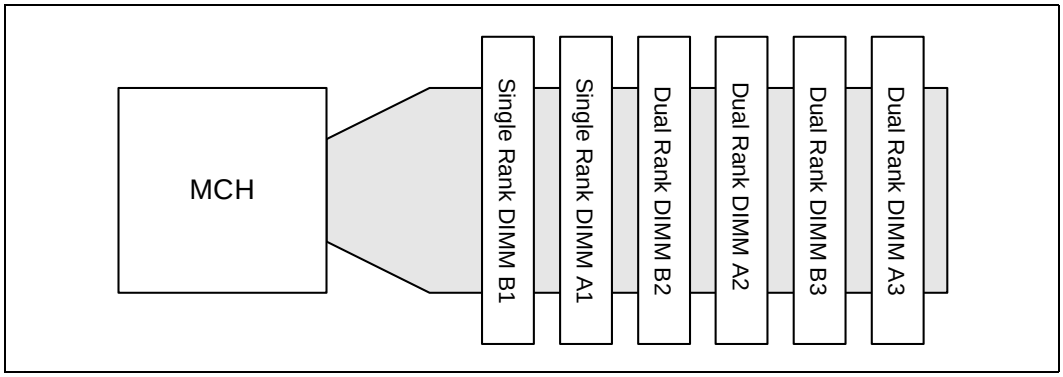


Figure 39. Example of Incorrect Single and Dual Rank Mixing



6.3.1 Dual Channel Source Synchronous Signal Group Routing

The MCH source synchronous signals are divided into groups consisting of data bits (DQ) and check bits (CB). An associated strobe (DQS) exists for each DQ and CB group, as shown in Table 32. The MCH supports both x4 and x8 devices, and the number of signals in each data group depends on the type of devices that are populated. For example, when x4 devices are populated, the 72-bit channel is divided into 18 data groups (16 groups consisting of four data bits each, and two groups consisting of four check bits each). One DQS is associated with each of these groups (18 total). Likewise, when x8 devices are populated, the 72-bit channel is divided into a total of nine data groups. In this case, only nine of the 18 strobes are used.

Table 32. DQ/CB to DQS Mapping (Sheet 1 of 2)

Data Group	Associated Strobe†
DQ_x[7:0]	DQS0, DQS9
DQ_x[15:8]	DQS1, DQS10
DQ_x[23:16]	DQS2, DQS11
DQ_x[31:24]	DQS3, DQS12
DQ_x[39:32]	DQS4, DQS13
DQ_x[47:40]	DQS5, DQS14

† In x4 configurations, the high DQS is associated with the high nibble and the low DQS is associated with the low nibble. In x8 configurations, only the low DQS is used.

Table 32. DQ/CB to DQS Mapping (Sheet 2 of 2)

Data Group	Associated Strobe†
DQ_x[55:48]	DQS6, DQS15
DQ_x[63:56]	DQS7, DQS16
CB_x[7:0]	DQS8, DQS17

† In x4 configurations, the high DQS is associated with the high nibble and the low DQS is associated with the low nibble. In x8 configurations, only the low DQS is used.

Table 33 states the routing requirements for the DQ, DQS and CB signals. All signals in a data group must be length matched to the associated DQSs, as described in Section 12.6, "Length Tuning". Length matching past the last DIMM connector is not critical. Route all data signals and their associated strobes on the same layer. Try to maintain routing the signals on the same layer. When a layer transition must occur, minimize the discontinuity in the ground reference plane. The source synchronous signals require series termination resistors (Rs) placed close to the first DIMM connector, and parallel termination resistors (Rtt) placed after the last DIMM connector. These solutions do not require DQS to CMDCLK pair length matching.

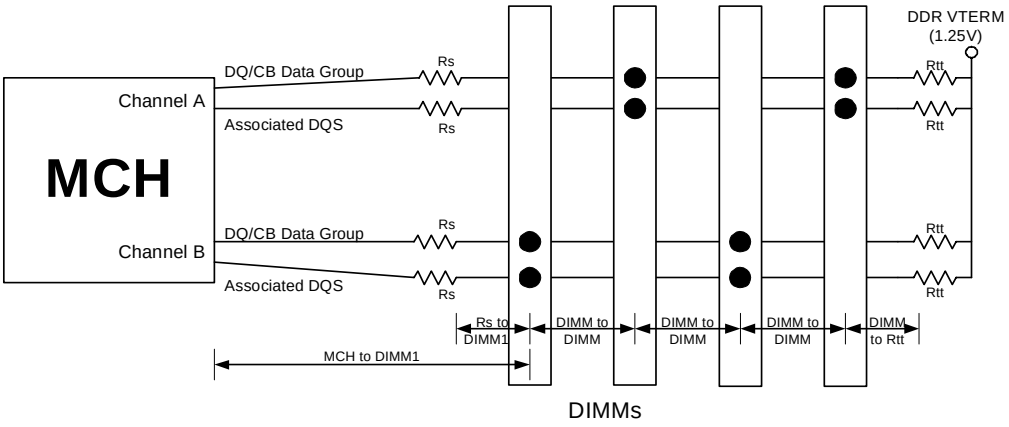
When resistor packs are used for the termination resistors, it is suggested that source synchronous group signals not be mixed with Source Clocked, Chip Select, or Clock Enable signals within the same resistor pack for validation purposes.

Table 33. Dual Channel Source Synchronous Signal Group Routing Guidelines

Parameter	1-DIMM Solution 0°[6], 25°[6], 90°	2-DIMM Solution 25°[6]	2-DIMM Solution 90°	3-DIMM Solution 90°	4-DIMM Solution 90°	Reference
Signal Group[3]	DQ[63:0], CB[7:0], DQS[17:0]					
Topology	Daisy Chain					Figure 40
Reference Plane	Ground					Figure 34
MCH to Rs Trace Impedance (Z_0)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	45 Ω ± 10%	Table 31
Rs to Rtt Trace Impedance (Z_0)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	55 Ω ± 10%	Table 31
MCH to Rs Trace Width	5 mils	5 mils	5 mils	5 mils	6 mils	Figure 34
Rs to Rtt Trace Width	5 mils	5 mils	5 mils	5 mils	4 mils	Figure 34
Nominal Trace Spacing	15 mils ± 1 mil	15 mils ± 1 mil	15 mils ± 1 mil	15 mils ± 1 mil	15 mils ± 1 mil	Figure 34
MCH to DIMM1 Trace Length[4]	1.8" to 5.5"	1.8" to 4.5"	1.8" to 6.0"	3.5" to 6.3"	6.1" to 6.3"	Figure 40
Rs to DIMM1 Trace Length	0.1" to 0.8"	0.1" to 0.8"	0.1" to 0.8"	0.1" to 0.8"	0.1" to 0.8"	Figure 40
DIMM to DIMM Trace Length	Not Supported	1.8" to 2.2" ± 50 mil[7]	1.0" to 1.2" ± 50 mil[5]	1.0" to 1.2" ± 50 mil[5]	1.0" to 1.12" ± 50 mil[5]	Figure 40
DIMM to Rtt Trace Length	< 0.8"	< 0.8"	< 0.8"	< 0.8"	0.3" to 1.3"	Figure 40
Series Resistor (Rs)	10 Ω ± 2%	10 Ω ± 2%	10 Ω ± 2%	10 Ω ± 2%	Not Applicable[1]	Figure 40
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	34.8 Ω ± 1%	Figure 40
MCH Breakout Guidelines[8]	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	
Length Tuning Requirements	DQ to DQS: ± 25 mil[2]	DQ to DQS: ± 25 mil[2]	DQ to DQS: ± 25 mil[2]	DQ to DQS: ± 25 mil[2]	DQ to DQS: ± 25 mil[2]	Figure 41, Section 12.6

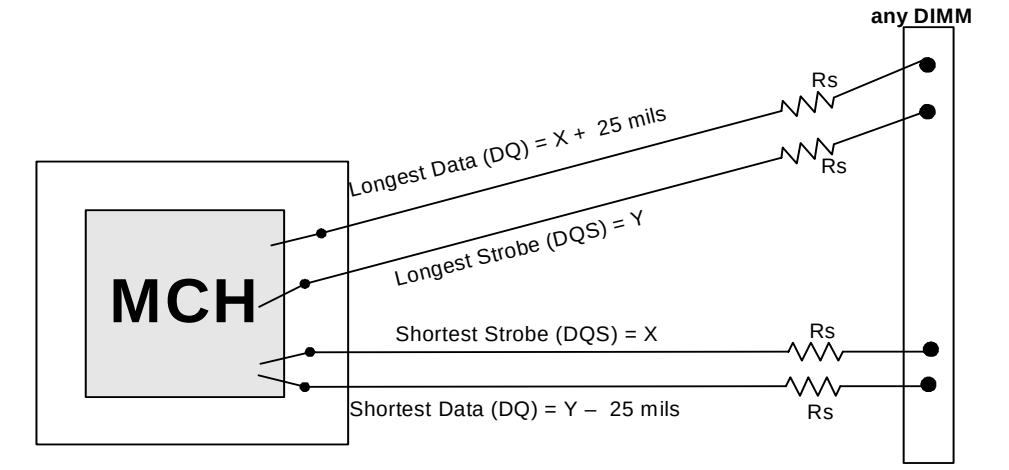
NOTES:
1. No Rs is required. Instead, change the impedance at the first DIMM pin.
2. The DQS pair in the group must also be tuned to each other with this parameter. The DQ and DQS lines in the same group must be length tuned to all DIMMs. Tune all lengths to the Intel® E7501 MCH package trace lengths.
3. Route all data signals and their associated strobes on the same layer from MCH to Rtt.
4. The MCH to DIMM1 trace length is defined as Intel E7501 MCH die pad (PCB trace velocity equivalent, see Section 12.6, "Length Tuning") to DIMM1 pin.
5. Within the same group, this length range should not vary by more than 50 mils. However, the length may be anywhere from 1.0" to 1.2".
6. Ensure angled DIMM connector pin length differences are accounted for when tuning lengths.
7. Within the same group, this length range should not vary by more than 50 mils. However, the length may be anywhere from 1.8" to 2.2".
8. Breakout distance is measured from outer ball array.

Figure 40. Dual Channel Source Synchronous Topology DIMM Solution



NOTE: Indicated lengths measure from the MCH component die pad (PCB trace velocity equivalent, see Section 12.6, "Length Tuning") to the DIMM connector pin (including the series resistor).

Figure 41. Trace Length Matching Requirements for Source Synchronous Routing



NOTES:
1. The DIMM displayed represents **any** DIMM. The two strobes must be within the same tolerance.
2. **All DIMMs must be length matched to the MCH within the specified tolerance.** The recommended method to do this is to length match the DIMM to DIMM signals, then length match the MCH to the first DIMM within the specified tolerance.
3. There are eight Data lines (DQ) per group. For simplicity, only the longest and the shortest are represented here.
4. Indicated lengths measure from the MCH die pad to the DIMM connector pin (including the series resistor). Section 12.6, "Length Tuning" describes how to calculate the correct tuned lengths.
5. Rs only applies to the first DIMM in each channel.

6.3.2 Dual Channel Command Clock Routing

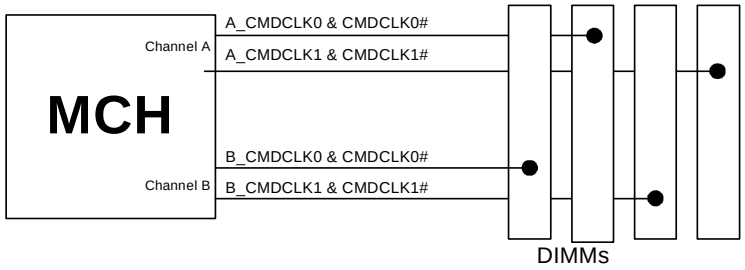
Only one differential clock pair is routed to each DIMM connector because the MCH only supports registered DDR DIMMs. All CMDCLK/CMDCLK# termination is on the DIMM modules. Route each clock and its compliment adjacent to each other. The two complimentary signals (e.g., CMDCLK_x0 and CMDCLK_x0#) must be length matched to each other within ± 2 mils (see Figure 42) and must be routed on the same layer. When a layer transition must occur, minimize the discontinuity in the ground reference plane.

Table 34. Dual Channel Command Clock Pair Routing Guidelines

Parameter	1-DIMM Solution[1] 0°, 25°, 90°	2-DIMM Solution 25°[1]	2-DIMM Solution 90°	3-DIMM Solution 90°	4-DIMM Solution 90°	Reference
Signal Group	CMDCLK CMDCLK#					
Topology	Point-to-point					Figure 42
Reference Plane	Ground					Figure 43
Differential Trace Impedance (Zo)	100 Ω ± 10%	100 Ω ± 10%	100 Ω ± 10%	100 Ω ± 10%	100 Ω ± 10%	Figure 43
Nominal Trace Width	5 mils	5 mils	5 mils	5 mils	5 mils	Figure 43
Differential Trace Spacing	7.5 mils	7.5 mils	7.5 mils	7.5 mils	7.5 mils	Figure 43
Group Trace Spacing	20 mils	20 mils	20 mils	20 mils	20 mils	Figure 43
MCH to DIMM1 Trace Length	3.0” to 4.0"	3.0” to 4.0"	3.0” to 4.0"	4.0" ± 250 mils	7.50" ± 100 mils	Figure 42
MCH to DIMM2 Trace Length	Not Supported	4.0” to 6.0”	4.0” to 6.0”	6.0" ± 250 mils	8.00" ± 100 mils	Figure 42
MCH to DIMM3 Trace Length	Not Supported	Not Supported	Not Supported	8.0” ± 250 mils	8.75" ± 100 mils	Figure 42
MCH to DIMM4 Trace Length	Not Supported	Not Supported	Not Supported	Not Supported	10.75" ± 100 mils	Figure 42
MCH Breakout Guidelines[2]	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	
Length Tuning Requirements	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	Figure 42

NOTES:
1. Ensure angled DIMM connector pin length differences are accounted for when tuning lengths.
2. Breakout distance is measured from outer ball array.

Figure 42. Dual Channel 2-DIMM Command Clock Topology



NOTES:
1. CMDCLK/CMDCLK# must be matched to within ± 2 mils using package trace length compensation.
2. Unused CMDCLK_x/CMDCLK_x# pairs are no connects.
3. Indicated lengths measured from the MCH component die pad to the DIMM connector pin.

6.3.3 Dual Channel Source Clocked Signal Group Routing

The MCH drives the command clock signals and the source-clocked signals together. That is, the MCH drives the command clock in the center of the valid window, and the source-clocked signals propagate with the command clock signal. Therefore, the critical timing is the difference between the command clock flight time and the source clocked signal flight time. The absolute flight time is not as critical.

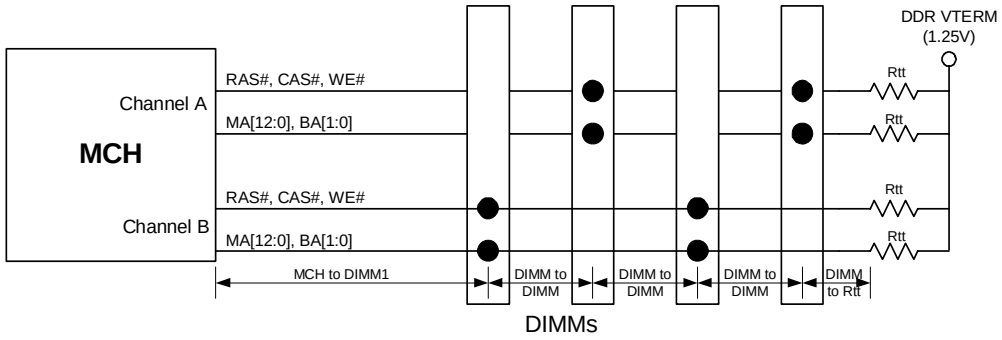
When resistor packs are used for the termination resistors, it is suggested that source synchronous signals not be mixed with Source Clocked, Chip Select, or Clock Enable signals within the same resistor pack for validation purposes.

Table 35. Dual Channel Source Clocked Signal Group Routing Guidelines

Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	3-DIMM Solution 90°	4-DIMM Solution 90°	Reference
Signal Group[1]	RAS#, CAS#, WE#, MA[12:0], BA[1:0]					
Topology	Daisy Chain					Figure 43
Reference Plane	Ground					Figure 34
Trace Impedance (Z_0)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	Table 31
Nominal Trace Width	5 mils	5 mils	5 mils	5 mils	5 mils	Figure 34
Nominal Trace Spacing	15 mils	15 mils	15 mils	15 mils	15 mils	Figure 34
MCH to DIMM1 Trace Length	1.8” to 5.5”	1.8” to 5.5”	1.8” to 5.5”	2.0” to 6.0”	2.0” to 6.0”	Figure 43
DIMM to DIMM Trace Length	Not Applicable	1.8” to 2.2”	1.0” to 1.2”	1.0” to 1.2”	1.0” to 1.2”	Figure 43
DIMM to Rtt Trace Length	< 0.8”	< 0.8”	< 0.8”	< 0.8”	0.3” to 1.3”	Figure 43
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	34.8 Ω ± 1%	Figure 43
MCH Breakout Guidelines[2]	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	

NOTES:
1. No length tuning required.
2. Breakout distance is measured from outer ball array.

Figure 43. Dual Channel Source Clocked Signal Topology



NOTE: Indicated lengths measure from the MCH component die pad to the DIMM connector pin.

6.3.4 Dual Channel Chip Select Routing

The MCH provides eight chip select signals. Two chip selects must be routed to each DIMM (one for each side).

Table 36. Dual Channel Chip Select Routing Guidelines (Sheet 1 of 2)

Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	3-DIMM Solution 90°	4-DIMM Solution 90°	Reference
Signal Group	CS[7:0]#[1]					
Topology	Point to Point					Figure 44
Reference Plane	Ground					Figure 34
Trace Impedance (Z_0)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	Table 31
Nominal Trace Width	5 mils	5 mils	5 mils	5 mils	5 mils	Figure 34
Nominal Trace Spacing	15 mils	15 mils	15 mils	15 mils	15 mils	Figure 34
MCH to DIMM1 Trace Length	3.0” to 4.0”	3.0” to 4.0”	3.0” to 4.0”	4.0" ± 875 mils	7.50" ± 875 mils	Figure 44
MCH to DIMM2 Trace Length	Not Applicable	4.0” to 6.0”	4.0” to 6.0”	6.0" ± 875 mils	8.00" ± 875 mils	Figure 44
MCH to DIMM3 Trace Length	Not Applicable	Not Applicable	Not Applicable	8.0" ± 875 mils	8.75" ± 875 mils	Figure 44
MCH to DIMM4 Trace Length	Not Applicable	Not Applicable	Not Applicable	Not Applicable	10.75" ± 875 mils	Figure 44

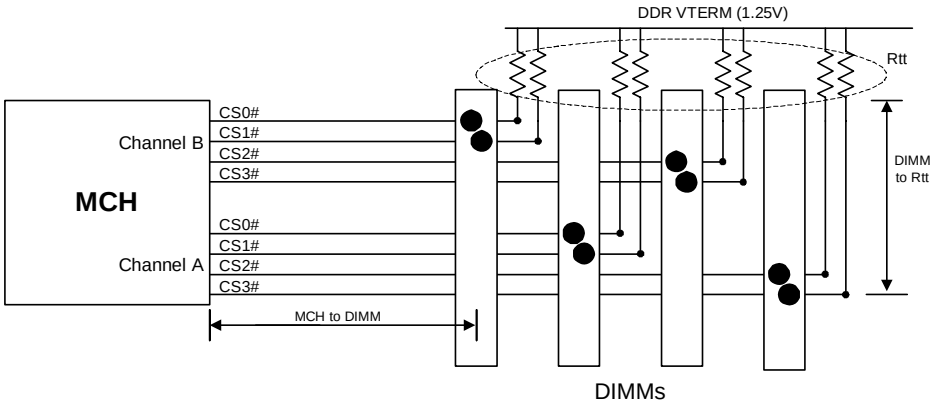
NOTES:
1. Chip selects for each DIMM must be length matched to the corresponding clock within ± 875 mils and require parallel termination resistors (Rtt) to DDR VTERM.
2. Breakout distance is measured from outer ball array.

Table 36. Dual Channel Chip Select Routing Guidelines (Sheet 2 of 2)

Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	3-DIMM Solution 90°	4-DIMM Solution 90°	Reference
Signal Group	CS[7:0]#[1]					
Trace Length - DIMM to Rtt	0.3" to 1.5"	0.3" to 1.5"	0.3" to 1.5"	0.3" to 1.5"	0.1" to 1.5"	Figure 44
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	34.8 Ω ± 1%	Figure 44
MCH Breakout Guidelines[2]	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	

NOTES:
1. Chip selects for each DIMM must be length matched to the corresponding clock within ± 875 mils and require parallel termination resistors (Rtt) to DDR VTERM.
2. Breakout distance is measured from outer ball array.

Figure 44. Dual Channel Chip Select Topology



NOTES:
1. Unused CS_*x*# signals are no connects.
2. Indicated lengths measured from the MCH component die pad to the DIMM connector pin.

6.3.5 Dual Channel Clock Enable Routing

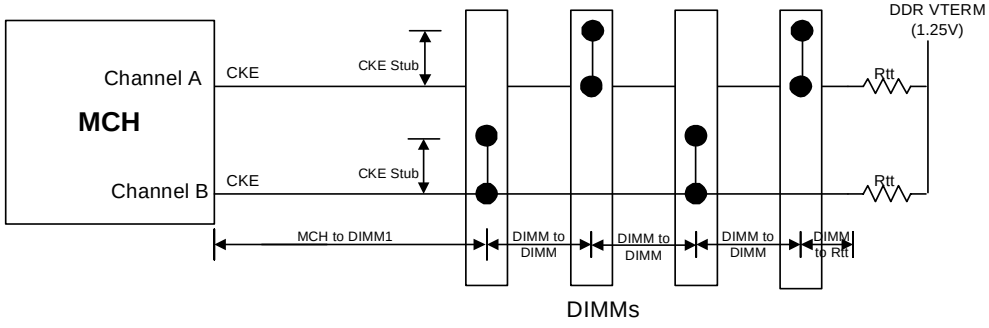
The MCH provides a single clock enable (CKE) signal. This signal is used during initialization to indicate that valid power and clocks are being applied to the DIMMs. Because the CKE signal has higher loading, it requires a lower impedance. The recommended impedance for the CKE signal is 40 Ω. This may be achieved using a 7.5-mils wide trace on the recommended stack-up (refer to Table 31). It is acceptable to route the CKE signal 5-mils wide and 5-mils spacing when breaking out of the MCH. However, the trace must be widened to 7.5-mils before widening the spacing to 15-mils. The CKE signal requires a parallel termination resistor (Rtt) to DDR VTERM placed as close to the last DIMM connector as possible.

Table 37. Dual Channel Clock Enable Routing Guidelines

Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	3-DIMM Solution 90°	4-DIMM Solution 90°	Reference
Signal Group	CKE					
Topology	Daisy Chain with Stubs					Figure 45
Reference Plane	Ground					Figure 34
Trace Impedance (Z_0)	40 Ω ± 10%	40 Ω ± 10%	40 Ω ± 10%	40 Ω ± 10%	40 Ω ± 10%	Table 31
Nominal Trace Width	7.5 mils	7.5 mils	7.5 mils	7.5 mils	7.5 mils	Figure 34
Nominal Trace Spacing	15 mils	15 mils	15 mils	15 mils	15 mils	Figure 34
MCH to DIMM1 Trace Length	1.8” to 6.0”	1.8” to 6.0”	1.8” to 6.0”	1.8” to 6.0”	1.8” to 6.0”	Figure 45
DIMM to DIMM Trace Length	Not Applicable	1.8” to 2.2”	1.0” to 1.2”	0.8” to 1.2”	0.8” to 1.2”	Figure 45
CKE_x Stub Trace Length	< 300 mils	< 300 mils	< 300 mils	< 300 mils	< 300 mils	Figure 45
DIMM to Rtt Trace Length	< 0.8”	< 0.8”	< 0.8”	< 0.8”	< 0.8”	Figure 45
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	34.8 Ω ± 1%	Figure 45
MCH Breakout Guidelines†	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	
Length Tuning Requirements	CKE to CMDCLK/ CMDCLK#: ± 1 inches	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	Figure 45

† Breakout distance is measured from outer ball array.

Figure 45. Dual Channel CKE Topology



NOTE: Indicated lengths measure from the MCH component die pad to the DIMM connector pin.

6.3.6 Dual Channel DC Biasing Signals

The DC Biasing signals are DDR signals which are not channel configuration specific. The following sections describe the DC Biasing signals.

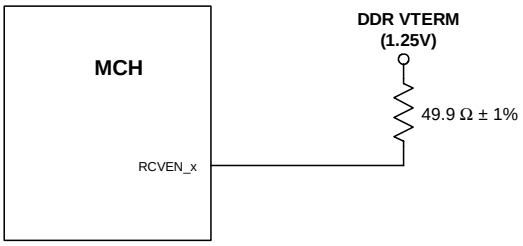
6.3.6.1 Dual Channel Receive Enable Signal (RCVEN#)

The Intel® E7501 MCH requires a pull-up resistor (Rtt) to DDR VTERM on RCVEN. Table 38 lists the guidelines. Figure 46 summarizes these options.

Table 38. Receive Enable Routing Guidelines

Parameter	Intel® E7501 MCH
Signal Group	Receive Enable
Topology	Pull-up
Trace Impedance (Zo)	50 Ω ± 10%
Nominal Trace Width	5 mils
Nominal Trace Spacing	15 mils
Trace Length - MCH RCVENIN to Rtt	No Requirement
Termination Resistor (Rtt)	49.9 Ω ± 1%
Total Length	No Requirement

Figure 46. Dual Channel Receive Enable Signal Routing Guidelines



NOTE: 'x' indicates channel A or B.

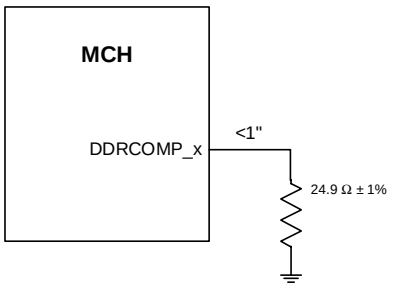
6.3.6.2 Dual Channel DDRCOMP

The MCH uses DDRCOMP_x to calibrate the DDR channel buffers. This is periodically done by sampling the DDRCOMP pin on the MCH. The Intel® E7501 MCH calibrates using a 24.9 Ω ± 1% pull-down to ground. This may be implemented by routing a 15 mils wide trace to a resistive network as depicted in Figure 47. Place a decoupling capacitor between the pull-down and any other terminations.

Table 39. DDRCOMP Routing Guidelines

Parameter	Intel® E7501 MCH
Topology	pull-down
Nominal Trace Width	15 mils
Nominal Trace Spacing	20 mils
Trace Length - MCH to Rtt	< 1.0"
Termination Resistor (Rtt)	24.9 Ω ± 1%
Termination Voltage	Ground

Figure 47. Dual Channel DDRCOMP Resistive Compensation



NOTE: 'x' indicates channel A or B.

6.3.6.2.1 DDRCOMP Tuning

It may be necessary to tune the DDR memory bus for optimum signal integrity based on your platform characteristics. If the signal quality of the memory bus needs to be tuned, then it is recommended that the DDRCOMP_x resistor value be adjusted to achieve optimum signal quality. The 24.9 ohms resistor is used as a starting point and may or may not need to be adjusted depending on your board characteristics.

6.3.6.3 Dual Channel DDRVREF and ODTCOMP

The DDR system memory reference voltage (VREF) is used by the DRAM devices and the MCH to determine the logic level being driven on the data, command, and control signals. VREF of the receiving device must track changes in VTERM to maximize DDR interface margin. However, VTERM and VREF **cannot** be the same power plane due to the sensitivity of the DRAM VREF buffers to the termination plane noise. When a voltage regulator is used, it must reference VTERM (see Figure 48). When a local resistor divider is used, VREF and VTERM must have a common source voltage between them (i.e., both VREF and V_{TT} are derived from the same voltage plane). Use equal value 1% resistors to derive DDR VREF (see Figure 49). Decouple VREF locally at the divider and DIMMs/MCH using one 0.1 µF capacitor per VREF pin.

Figure 48. DDR VREF Voltage Regulator

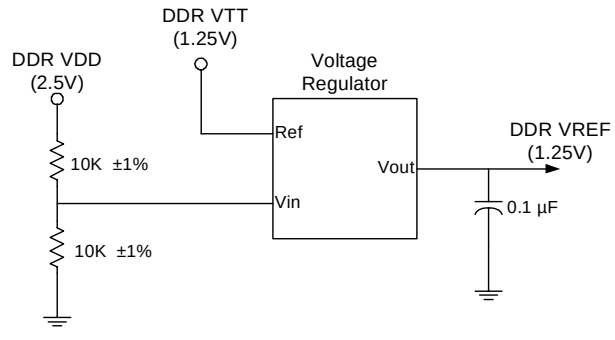
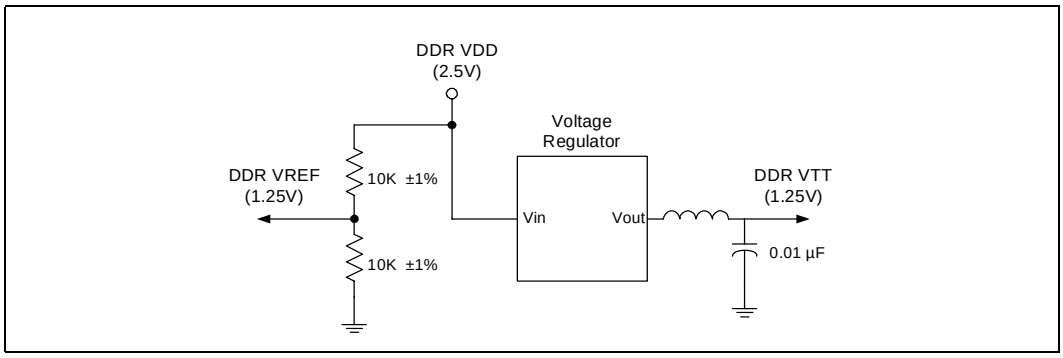


Figure 49. DDR VREF Voltage Divider

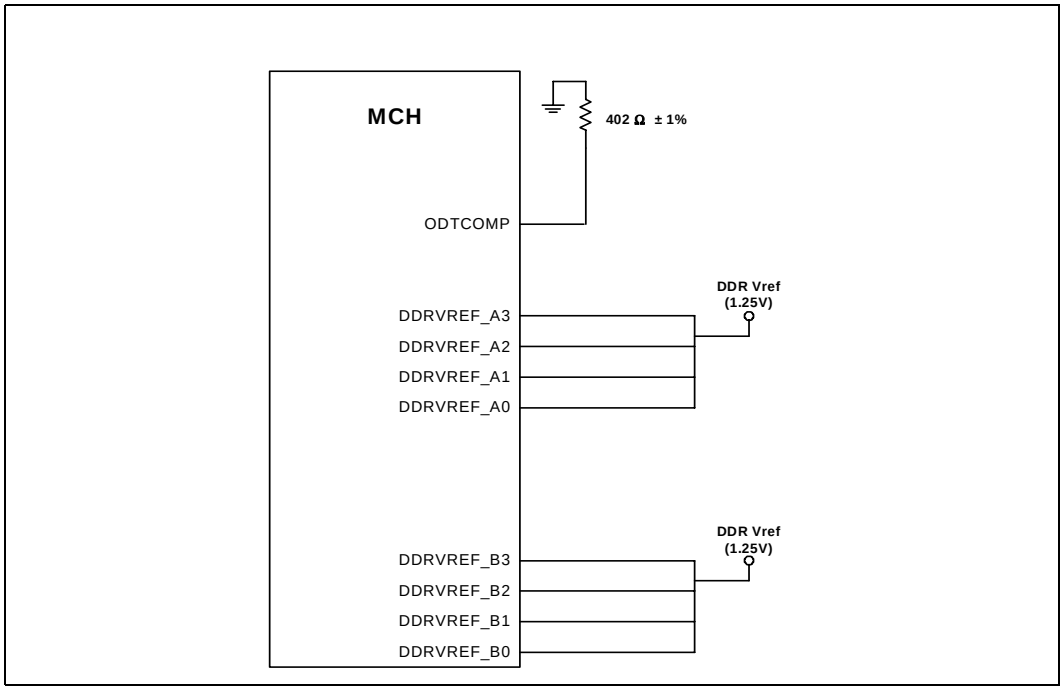


Note: Use equal resistor values for the DDR VREF supply.

The Intel® E7501 MCH includes active read-cycle termination for all source synchronous signals (DQ and DQS signals). This On-Die-Termination Compensation (ODTCOMP) serves to control signal swing at the MCH receiver during read-cycles. It does not function during write-cycles.The ODTCOMP circuit has the effect of a weak pull-up of 200 Ω ± 15% to VTT. The value of termination is not adjustable. The ODTCOMP reduces ringbacks and overshoots, and in some cases may help reduce the need for series termination.

The Intel E7501 MCH has four DDRVREFs per channel (eight total). Route DDRVREF and ODTCOMP traces 5 mils wide. The ODTCOMP signal needs a 402 Ω pull-down resistor. (See Figure 50.).

Figure 50. Dual Channel Routing DDRVREF and ODTCOMP



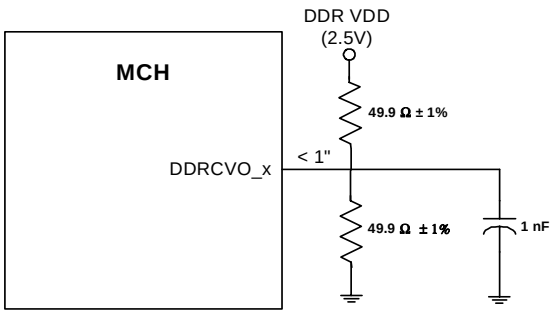
6.3.6.4 Dual Channel DDRCVO

The MCH uses a compensation signal to adjust buffer characteristics and output voltage swing over temperature, process, and voltage skew. Calibration is done periodically by sampling the DDRCVO_x pins on the MCH. Place the voltage divider network (see Figure 51) within one inch of the MCH.

Table 40. DDRCVO Routing Guidelines

Parameter	Intel® E7501 MCH
Topology	Resistor Divider
Nominal Trace Width	15 mils
Nominal Trace Spacing	20 mils
Trace Length - MCH to Divider	< 1.0”

Figure 51. Dual Channel DDRCVO Routing Guidelines

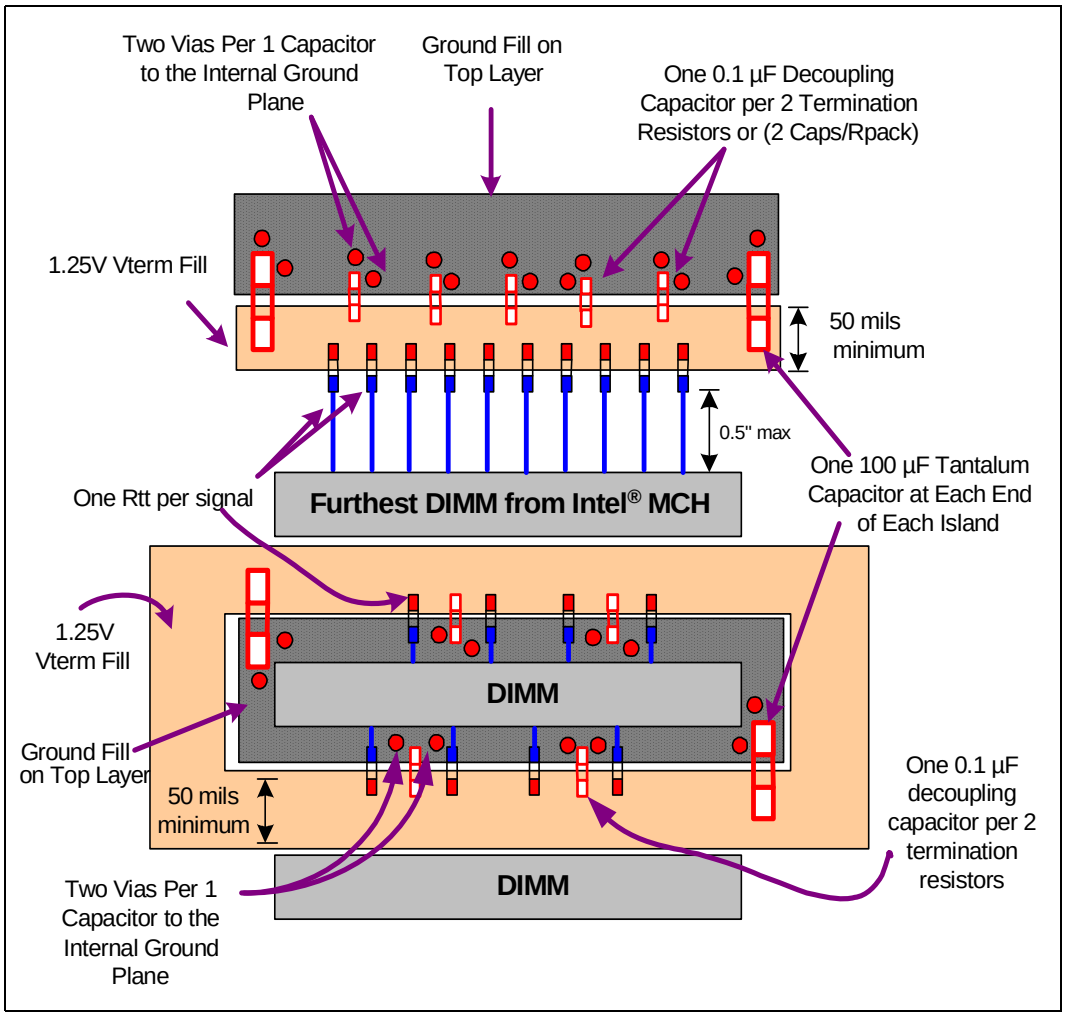


NOTE: ‘x’ indicates channel A or B.

6.3.7 Dual Channel DDR Signal Termination and Decoupling

Place a 1.25 V termination plane on the top layer, just beyond (within 0.5 inch) the DIMM connector furthest from the MCH on each channel, as shown in Figure 52. The VTERM island must be at least 50-mils wide. Use this termination plane to terminate all DIMM signals, using one Rtt resistor per signal. Termination may be done with individual resistors or Rpack. Decouple the VTERM plane using one 0.1 µF decoupling capacitor per two termination resistors. Each decoupling capacitor must have at least two vias between the top layer ground fill and the internal ground plane. In addition place one 100 µF Tantalum capacitor on each end of the termination island for bulk decoupling. Refer to Figure 52.

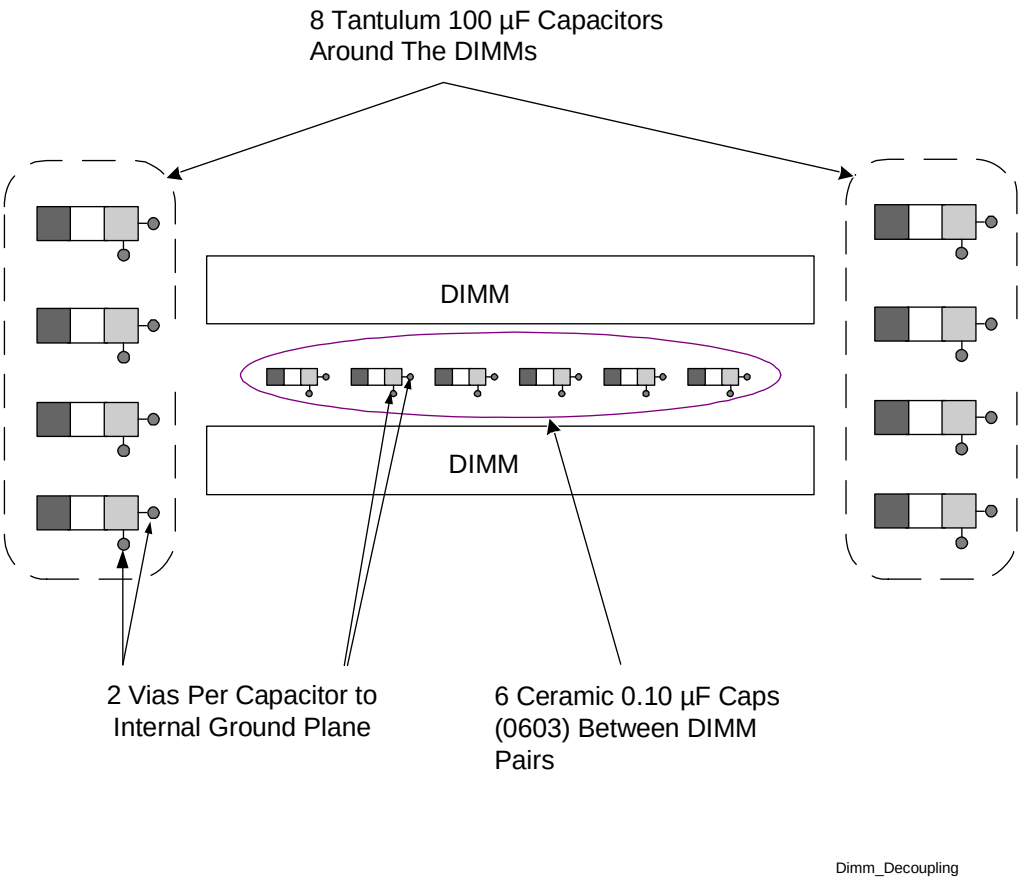
Figure 52. DDR VTerm Plane



6.3.8 2.5 Volt Decoupling Requirements

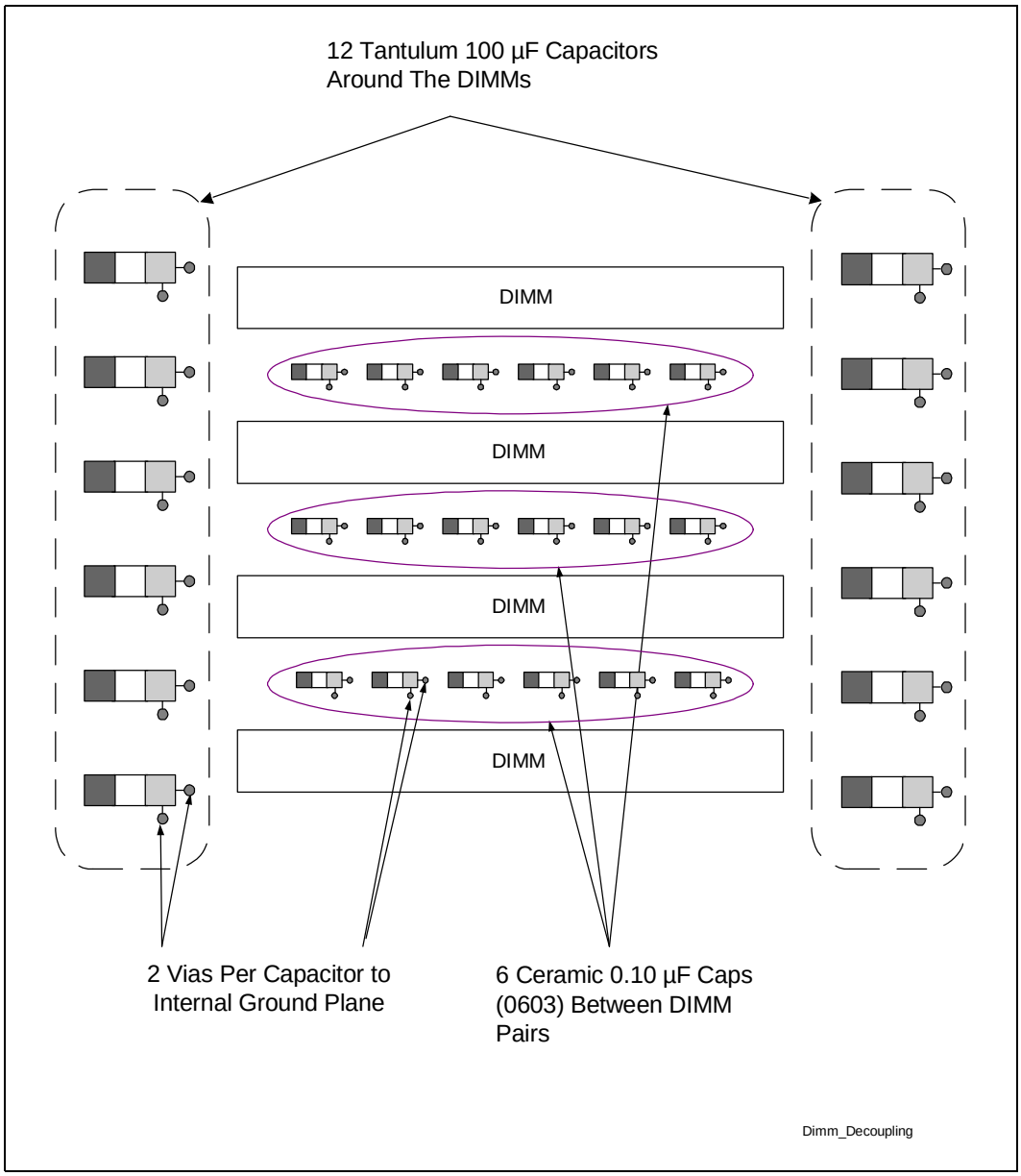
Decouple the DIMM connectors as shown in Figure 53 or Figure 54. Place six ceramic 0.1 µF (0603) capacitors between each pair of DIMM connectors. Place two Tantalum 100 µF capacitors around each DIMM connector and two additional Tantalum 100 µF capacitors per channel, keeping them within 0.5 inch of the DIMM connectors. Figure 53 depicts a 1-DIMM per channel decoupling scheme and Figure 54 depicts a 2-DIMM per channel decoupling scheme. When more DIMMs per channel may be used, continue the decoupling scheme for each additional DIMM connector.

Figure 53. 1-DIMM Per Channel Decoupling



NOTE: For each additional DIMM added per channel, add two additional 100 µF Tantalum capacitors around the DIMM, and add six additional 0.01 µF ceramic capacitors between each DIMM pair.

Figure 54. 2-DIMMs Per Channel Decoupling



6.4 Single Channel DDR Overview

In a single channel DDR configuration, channel A is the only channel that is active. Figure 55 and Figure 56 show channel A being routed to a single bank of DIMMs. The letter 'A' in the DIMM figure refers to the DIMM channel. The number following 'A' refers to the DIMM logical group.

The platform requires DDR DIMMs to be populated in-order, starting with the DIMM furthest from the MCH in a 'fill-farthest' approach (see Figure 55 and Figure 56). In addition, single rank DIMMs should be populated furthest when a combination of single ranked and double ranked DIMMs are used. This recommendation is based on the signal integrity requirements of the DDR interface. Intel recommends checking for correct DIMM placement during BIOS initialization. Additionally, it is strongly recommended that all designs follow the DIMM ordering, SMBus Addressing, Command Clock routing and Chip Select routing documented in Figure 55 and Figure 56. This addressing must be maintained to be compliant with the reference BIOS code supplied by Intel.

Single Channel routing guidelines listed in the following sections are described for one or two DIMMs. When single channel three or four DIMMs guidelines are needed, follow the dual channel guidelines for three or four DIMMs listed in Section 6.3, "Dual Channel DDR Overview".

Figure 55. Single Channel 2-DIMM Implementation

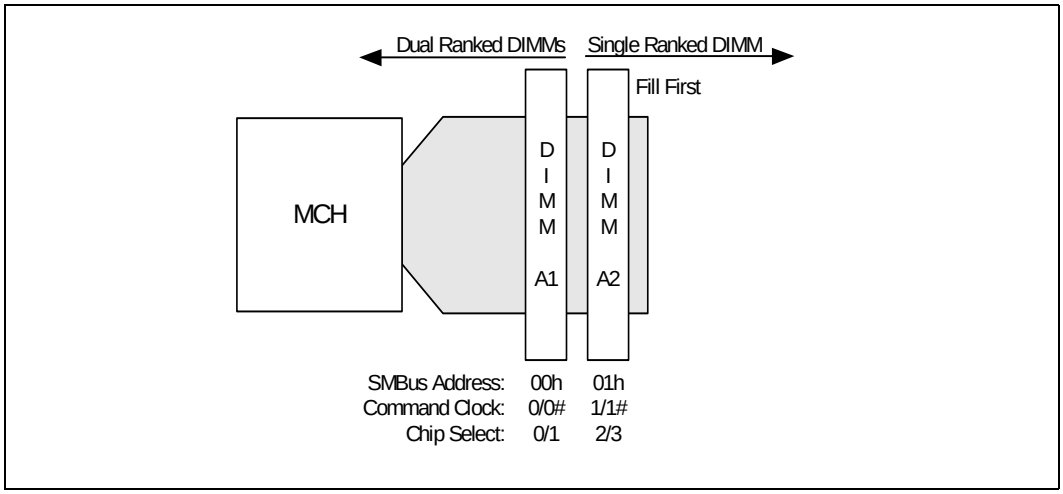
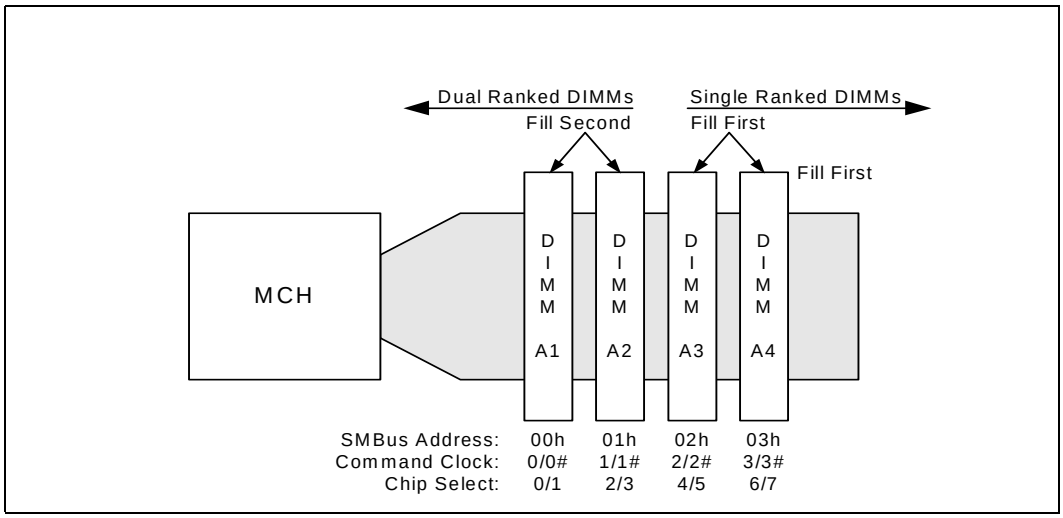


Figure 56. Single Channel 4-DIMM Implementation



Certain combinations of DIMM types in 3-DIMM and 4-DIMM per channel systems have been found to violate the JEDEC write ring back measurement specification. 1-DIMM and 2-DIMM per channel systems do not violate the JEDEC write ring back specification. When combining double-rank DIMMs (x4 or x8) with single-rank DIMMs (x4 or x8), if the first populated slot (closest to the MCH) contains a single-ranked DIMM, the write ringback at that DIMM violates the JEDEC DRAM specification (see Figure 58). To reduce write ring back, populate single-ranked DIMMs furthest from the MCH when a combination of single-ranked and double-ranked DIMMs is used (see Figure 57).

To determine if a registered DDR DIMM is a single-bank DIMM or a double-bank DIMM, refer to *Distinguishing Between Single-Rank and Double-Rank Registered DDR DIMM Modules Application Note (AP-727)* or contact your Intel representative for more information.

Figure 57. Example of Proper Single Channel Rank Mixing

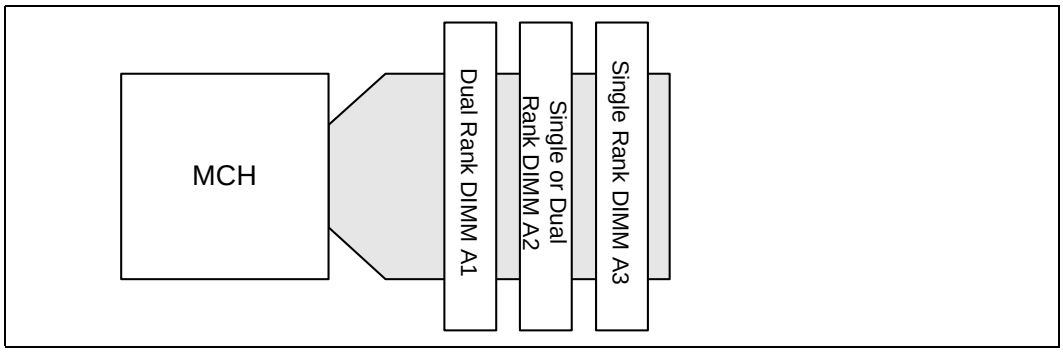
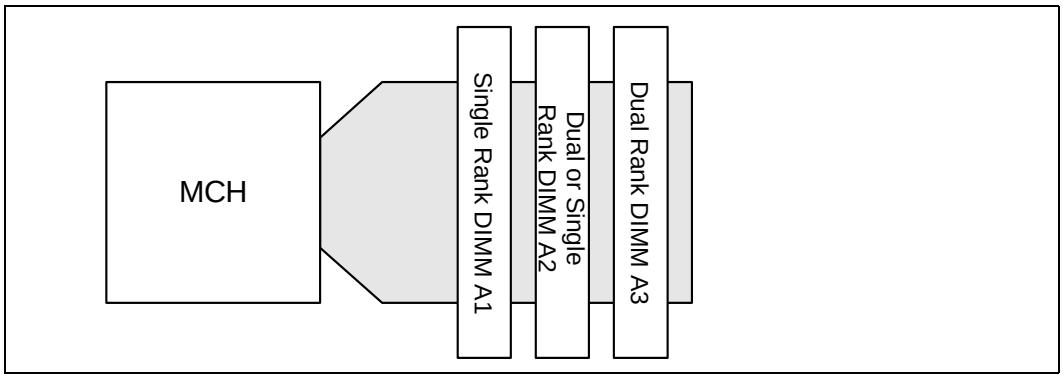


Figure 58. Example of Incorrect Single Channel Rank Mixing



6.4.1 Unused Channel Termination

Channel B is not used in a single channel configuration. Therefore, Channel B's associated signals should terminated as described in Table 41.

Table 41. Channel B Signal Terminations

Signal Name	Single Channel PCB Recommended Connection
Bidirectional Signal Group	
CB_B[7:0]	47 Ω +- 1% pullup to DDR Vterm (1.25 V). See Section 6.4.2.
DQ_B[63:0]	47 Ω +- 1% pullup to DDR Vterm (1.25 V). See Section 6.4.2.
DQS_B[17:0]	47 Ω +- 1% pullup to DDR Vterm (1.25 V). See Section 6.4.2.
RCVENOUT_B#	47 Ω pullup to DDR Vterm (1.25 V). See Section 6.4.7.1.
Output Signal Group	
CMDCLK_B[3:0] CMDCLK_B[3:0]#	No connect or connect each associated CMDCLK_Bx to CMDCLK_Bx# through a 120 Ω resistor.
MA_B[12:0] BA_B[1:0] RAS_B# CAS_B# WE_B# CS_B[7:0]# CKE_B[1:0]	No connect.
Input Signal Group	
DDRCOMP_B	24.9 Ω +-1% pull-down to Ground. See Section 6.4.7.2.
DRCVO_B	Connect to resistor divider network. See Section 6.4.7.4.
DDRVREF_B[3:0]	Connect to DDR VREF (1.25 V). See Section 6.4.7.3.

6.4.2 Single Channel Source Synchronous Signal Group Routing

The MCH source synchronous signals are divided into groups consisting of data bits (DQ) and check bits (CB). An associated strobe (DQS) exists for each DQ and CB group, as shown in Table 42. The MCH supports both x4 and x8 devices, and the number of signals in each data group depends on the type of devices that are populated. For example, when x4 devices are populated, the 72-bit channel is divided into 18 data groups (16 groups consisting of four data bits each, and two groups consisting of four check bits each). One DQS is associated with each of these groups (18 total). Likewise, when x8 devices are populated, the 72-bit channel is divided into a total of nine data groups. In this case, only nine of the 18 strobes are used.

Table 42. Single Channel DQ/CB to DQS Mapping

Data Group	Associated Strobe†
DQ_x[7:0]	DQS0, DQS9
DQ_x[15:8]	DQS1, DQS10
DQ_x[23:16]	DQS2, DQS11
DQ_x[31:24]	DQS3, DQS12
DQ_x[39:32]	DQS4, DQS13
DQ_x[47:40]	DQS5, DQS14
DQ_x[55:48]	DQS6, DQS15
DQ_x[63:56]	DQS7, DQS16
CB_x[7:0]	DQS8, DQS17

† In x4 configurations, the high DQS is associated with the high nibble and the low DQS is associated with the low nibble. In x8 configurations, only the low DQS is used.

Table 43 states the routing requirements for the DQ, DQS and CB signals. All signals in a data group must be length matched to the associated DQSs, as described in Section 12.6, “Length Tuning”. Length matching past the last DIMM connector is not critical. Route all data signals and their associated strobes on the same layer. Try to maintain routing the signals on the same layer. When a layer transition must occur, minimize the discontinuity in the ground reference plane. The source synchronous signals require series termination resistors (Rs) placed close to the first DIMM connector, and parallel termination resistors (Rtt) placed after the last DIMM connector. These solutions do not require DQS to CMDCLK pair length matching.

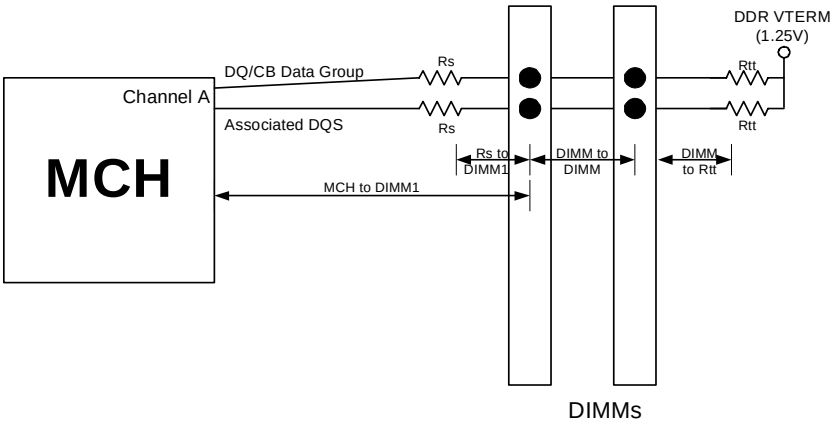
When resistor packs are used for the termination resistors, it is suggested that source synchronous group signals not be mixed with Source Clocked, Chip Select, or Clock Enable signals within the same resistor pack for validation purposes.

Table 43. Single Channel Source Synchronous Signal Group Routing Guidelines

Parameter	1-DIMM Solution 0°[6], 25°[6], 90°	2-DIMM Solution 25°[6]	2-DIMM Solution 90°	Reference
Signal Group[3]	DQ[63:0], CB[7:0], DQS[17:0]			
Topology	Daisy Chain			Figure 59
Reference Plane	Ground			Figure 59
MCH to Rs Trace Impedance (Z_0)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	Table 42
Rs to Rtt Trace Impedance (Z_0)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	Table 42
MCH to Rs Trace Width	5 mils	5 mils	5 mils	Figure 59
Rs to Rtt Trace Width	5 mils	5 mils	5 mils	Figure 59
Nominal Trace Spacing	15 mils ± 1 mil	15 mils ± 1 mil	15 mils ± 1 mil	Figure 59
MCH to DIMM1 Trace Length[4]	1.8” to 5.5"	1-8” to 4.5"	1-8” to 6.0"	Figure 59
Rs to DIMM1 Trace Length	0.1" to 0.8"	0.1" to 0.8"	0.1" to 0.8"	Figure 59
DIMM to DIMM Trace Length	Not Supported	1.8” to 2.2” ± 50 mils[7]	1.0” to 1.2”± 50 mils[5]	Figure 59
DIMM to Rtt Trace Length	< 0.8”	< 0.8”	< 0.8”	Figure 59
Series Resistor (Rs)	10 Ω ± 2%	10 Ω ± 2%	10 Ω ± 2%	Figure 59
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	Figure 59
MCH Breakout Guidelines[8]	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	
Length Tuning Requirements	DQ to DQS: ± 25 mil[2]	DQ to DQS: ± 25 mil[2]	DQ to DQS: ± 25 mil[2]	Figure 60, Section 12.6

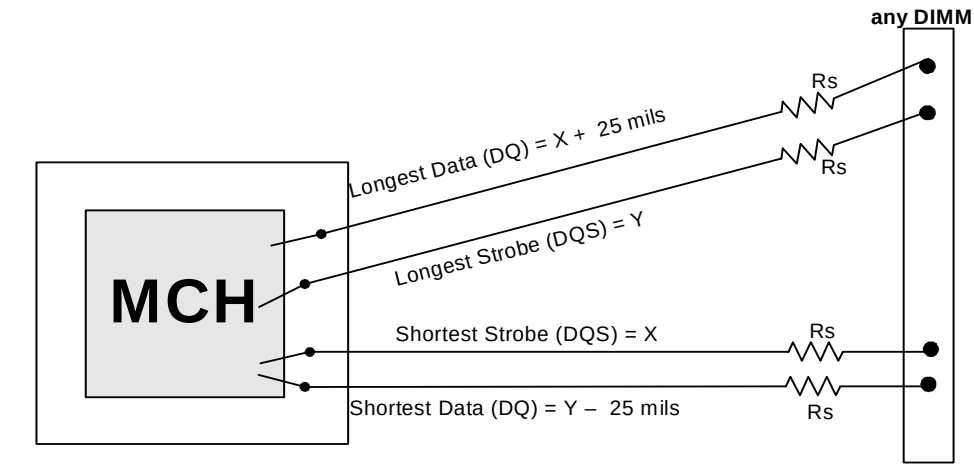
NOTES:
1. No Rs is required. Instead, change the impedance at the first DIMM pin.
2. The DQS pair in the group must also be tuned to each other with this parameter. The DQ and DQS lines in the same group must be length tuned to all DIMMs. Tune all lengths to the Intel® E7501 MCH package trace lengths.
3. Route all data signals and their associated strobes on the same layer from MCH to Rtt.
4. The MCH to DIMM1 trace length is defined as Intel E7501 MCH die pad (PCB trace velocity equivalent, see Section 12.6, “Length Tuning”) to DIMM1 pin.
5. Within the same group, this length range should not vary by more than 50 mils. However, the length may be anywhere from 1.0” to 1.2”.
6. Ensure angled DIMM connector pin length differences are accounted for when tuning lengths.
7. Within the same group, this length range should not vary by more than 50 mils. However, the length may be anywhere from 1.8” to 2.2”.
8. Breakout distance is measured from outer ball array.

Figure 59. Single Channel Source Synchronous Topology DIMM Solution



NOTE: Indicated lengths measure from the MCH component die pad (PCB trace velocity equivalent, see Section 12.6, "Length Tuning") to the DIMM connector pin (including the series resistor).

Figure 60. Trace Length Matching Requirements for Single Channel Source Synchronous Routing



NOTES:
1. The DIMM displayed represents **any** DIMM. The two strobes must be within the same tolerance.
2. **All DIMMs must be length matched to the MCH within the specified tolerance.** The recommended method to do this is to length match the DIMM to DIMM signals, then length match the MCH to the first DIMM within the specified tolerance.
3. There are eight Data lines (DQ) per group. For simplicity, only the longest and the shortest are represented here.
4. Indicated lengths measure from the MCH die pad to the DIMM connector pin (including the series resistor). Section 12.6, "Length Tuning" describes how to calculate the correct tuned lengths.
5. Rs only applies to the first DIMM in each channel.

6.4.3 Single Channel Command Clock Routing

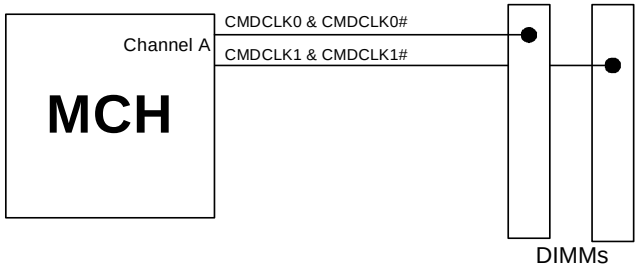
Only one differential clock pair is routed to each DIMM connector because the MCH only supports registered DDR DIMMs. All CMDCLK/CMDCLK# termination is on the DIMM modules. Route each clock and its compliment adjacent to each other. The two complimentary signals (e.g., CMDCLK_x0 and CMDCLK_x0#) must be length matched to each other within ± 2 mils and must be routed on the same layer. When a layer transition must occur, minimize the discontinuity in the ground reference plane.

Table 44. Single Channel Command Clock Pair Routing Guidelines

Parameter	1-DIMM Solution[1] 0°, 25°, 90°	2-DIMM Solution 25°[1]	2-DIMM Solution 90°	Reference
Signal Group	CMDCLK, CMDCLK#			
Topology	Point to point			Figure 61
Reference Plane	Ground			Figure 63
Differential Trace Impedance (Z_0)	100 Ω ± 10%	100 Ω ± 10%	100 Ω ± 10%	Figure 63
Nominal Trace Width	5 mils	5 mils	5 mils	Figure 63
Differential Trace Spacing	7.5 mils	7.5 mils	7.5 mils	Figure 63
Group Trace Spacing	20 mils	20 mils	20 mils	Figure 63
MCH to DIMM1 Trace Length	3.0” to 4.0”	3.0” to 4.0”	3.0” to 4.0”	Figure 61
MCH to DIMM2 Trace Length	Not Supported	4.0” to 6.0"	4.0” to 6.0"	Figure 61
MCH Breakout Guidelines[2]	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	
Length Tuning Requirements	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	Figure 61

NOTE:
1. Ensure angled DIMM connector pin length differences are accounted for when tuning lengths.
2. Breakout distance is measured from outer ball array.

Figure 61. Single Channel 2-DIMM Command Clock Topology



NOTES:
1. CMDCLK/CMDCLK# must be matched to within ± 2 mils using package trace length compensation.
2. Unused CMDCLK_x/CMDCLK_x# pairs are no connects.
3. Indicated lengths measured from the MCH component die pad to the DIMM connector pin.

6.4.4 Single Channel Source Clocked Signal Group Routing

The MCH drives the command clock signals and the source-clocked signals together. That is, the MCH drives the command clock in the center of the valid window, and the source-clocked signals propagate with the command clock signal. Therefore, the critical timing is the difference between the command clock flight time and the source clocked signal flight time. The absolute flight time is not as critical.

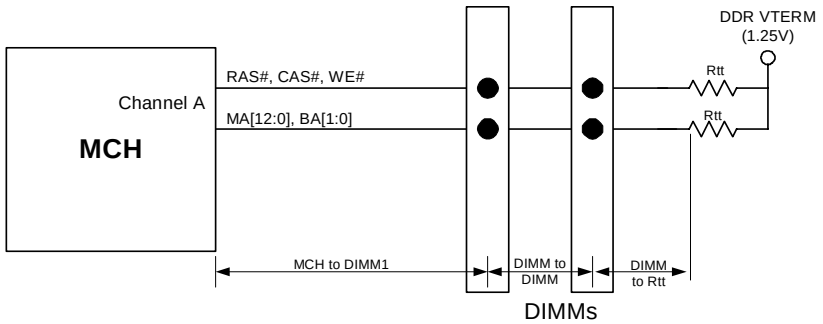
When resistor packs are used for the termination resistors, it is suggested that source synchronous signals not be mixed with Source Clocked, Chip Select, or Clock Enable signals within the same resistor pack for validation purposes.

Table 45. Single Channel Source Clocked Signal Group Routing Guidelines

Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	Reference
Signal Group	RAS#, CAS#, WE#, MA[12:0], BA[1:0]			
Topology	Daisy Chain			Figure 62
Reference Plane	Ground			Figure 59
Trace Impedance (Z_0)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	Table 42
Nominal Trace Width	5 mils	5 mils	5 mils	Figure 59
Nominal Trace Spacing	15 mils	15 mils	15 mils	Figure 34
MCH to DIMM1 Trace Length	1.8” to 5.5”	1.8” to 5.5”	1.8” to 5.5”	Figure 62
DIMM to DIMM Trace Length	Not Applicable	1.8” to 2.2”	1.0” to 1.2”	Figure 62
DIMM to Rtt Trace Length	< 0.8”	< 0.8”	< 0.8”	Figure 62
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	Figure 62
MCH Breakout Guidelines[2]	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	

NOTES:
1. No length tuning required.
2. Breakout distance is measured from outer ball array.

Figure 62. Single Channel Source Clocked Signal Topology



NOTE: Indicated lengths measure from the MCH component die pad to the DIMM connector pin.

6.4.5 Single Channel Chip Select Routing

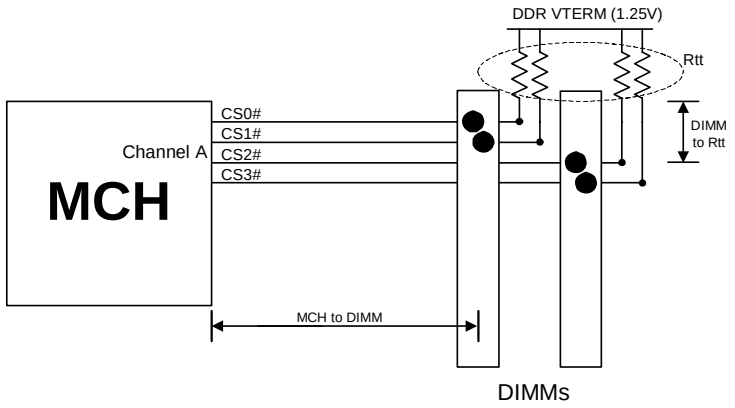
The MCH provides eight chip select signals. Two chip selects must be routed to each DIMM (one for each side).

Table 46. Single Channel Chip Select Routing Guidelines

Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	Reference
Signal Group	CS[7:0]#			
Topology	Point to Point			Figure 63
Reference Plane	Ground			Figure 59
Trace Impedance (Z_0)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	Table 42
Nominal Trace Width	5 mils	5 mils	5 mils	Figure 59
Nominal Trace Spacing	15 mils	15 mils	15 mils	Figure 59
MCH to DIMM1 Trace Length	3.0" to 4.0”	3.0" to 4.0”	3.0" to 4.0”	Figure 63
MCH to DIMM2 Trace Length	Not Applicable	4.0 to 6.0"	4.0 to 6.0"	Figure 63
Trace Length - DIMM to Rtt	0.3" to 1.5”	0.3" to 1.5”	0.3" to 1.5”	Figure 63
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	Figure 63
MCH Breakout Guidelines[2]	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	

NOTES:
1. Chip selects for each DIMM must be length matched to the corresponding clock within ± 875 mils and require parallel termination resistors (Rtt) to DDR VTERM.
2. Breakout distance is measured from outer ball array.

Figure 63. Single Channel Chip Select Topology



NOTES:
1. Unused CS_*x*# signals are no connects.
2. Indicated lengths measured from the MCH component die pad to the DIMM connector pin.

6.4.6 Single Channel Clock Enable Routing

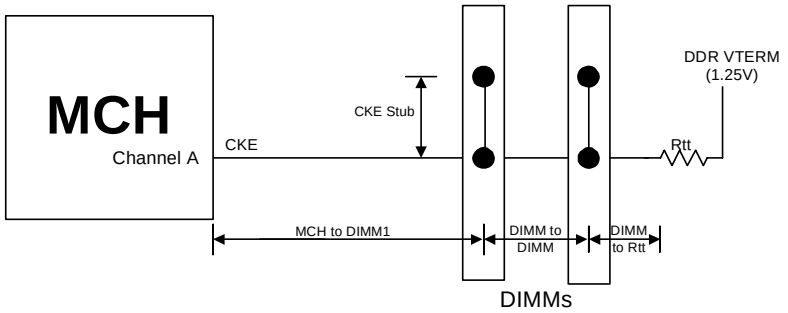
The MCH provides a single clock enable (CKE) signal. This signal is used during initialization to indicate that valid power and clocks are being applied to the DIMMs. Because the CKE signal has higher loading, it requires a lower impedance. The recommended impedance for the CKE signal is 40 Ω. This may be achieved using a 7.5-mils wide trace on the recommended stack-up (refer to Table 31). It is acceptable to route the CKE signal 5-mils wide with 5-mils spacing when breaking out of the MCH. However, the trace must be widened to 7.5 mils before widening the spacing to 15-mils. The CKE signal requires a parallel termination resistor (Rtt) to DDR VTERM placed as close to the last DIMM connector as possible.

Table 47. Single Channel Clock Enable Routing Guidelines

Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	Reference
Signal Group	CKE			
Topology	Daisy Chain with Stubs			Figure 64
Reference Plane	Ground			Figure 59
Trace Impedance (Z_0)	40 Ω ± 10%	40 Ω ± 10%	40 Ω ± 10%	Table 42
Nominal Trace Width	7.5 mils	7.5 mils	7.5 mils	Figure 59
Nominal Trace Spacing	15 mils	15 mils	15 mils	Figure 59
MCH to DIMM1 Trace Length	1.8” to 6.0”	1.8” to 6.0”	1.8” to 6.0”	Figure 64
DIMM to DIMM Trace Length	Not Applicable	1.8” to 2.2”	1.0” to 1.2”	Figure 64
CKE_x Stub Trace Length	< 300 mils	< 300 mils	< 300 mils	Figure 64
DIMM to Rtt Trace Length	< 0.8”	< 0.8”	< 0.8”	Figure 64
MCH Breakout Guidelines†	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	5/5 (1:1), < 500 mils	
Length Tuning Requirements	CKE to CMDCLK/ CMDCLK#: ± 1 inches	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	Figure 64

† Breakout distance is measured from outer ball array.

Figure 64. Single Channel CKE Topology



NOTE: Indicated lengths measure from the MCH component die pad to the DIMM connector pin.

6.4.7 Single Channel DC Biasing Signals

The DC Biasing signals are DDR signals which are not channel configuration specific. The following sections describe the DC Biasing signals.

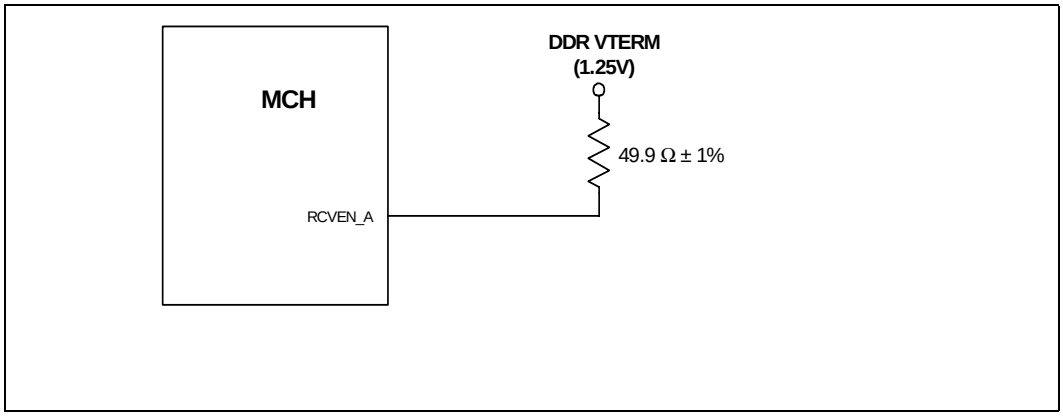
6.4.7.1 Single Channel Receive Enable Signal (RCVEN#)

The Intel® E7501 MCH requires a pull-up resistor (Rtt) to DDR VTERM on RCVEN. Table 48 lists the guidelines. Figure 65 summarizes these options.

Table 48. Single Channel Receive Enable Routing Guidelines

Parameter	Intel® E7501 MCH
Signal Group	Receive Enable
Topology	Pull-up
Trace Impedance (Z_0)	50 Ω ± 10%
Nominal Trace Width	5 mils
Nominal Trace Spacing	15 mils
Trace Length - MCH RCVENIN to Rtt	No Requirement
Termination Resistor (Rtt)	49.9 Ω ± 1%
Total Length	No Requirement

Figure 65. Single Channel Receive Enable Signal Routing Guidelines



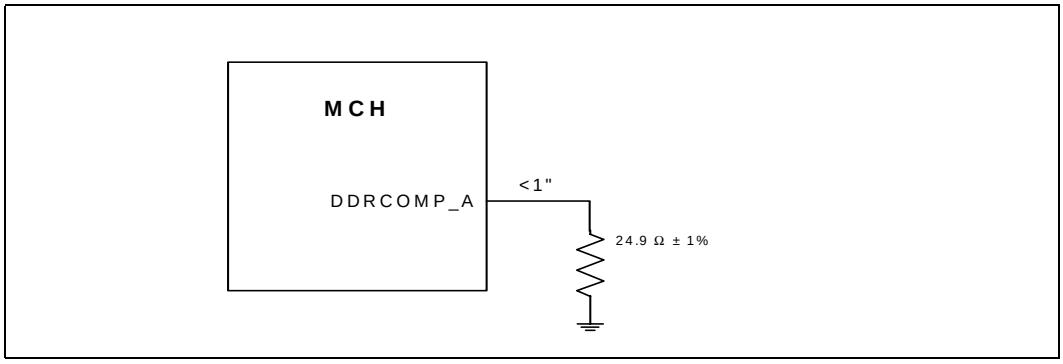
6.4.7.2 Single Channel DDRCOMP

The MCH uses DDRCOMP_A to calibrate the DDR channel buffers. This is periodically done by sampling the DDRCOMP pin on the MCH. The Intel® E7501 MCH calibrates using a 24.9 Ω ± 1% pull-down to ground. This may be implemented by routing a 15 mils wide trace to a resistive network as depicted in Figure 66. Place a decoupling capacitor between the pull-down and any other terminations.

Table 49. DDRCOMP Routing Guidelines

Parameter	Intel® E7501 MCH
Topology	pull-down
Nominal Trace Width	15 mils
Nominal Trace Spacing	20 mils
Trace Length - MCH to Rtt	< 1.0”
Termination Resistor (Rtt)	24.9 Ω ± 1%
Termination Voltage	Ground

Figure 66. Single Channel DDRCOMP Resistive Compensation



6.4.7.2.1 DDRCOMP Tuning

It may be necessary to tune the DDR memory bus for optimum signal integrity based on your platform characteristics. If the signal quality of the memory bus needs to be tuned, then it is recommended that the DDRCOMP_A resistor value be adjusted to achieve optimum signal quality. The 24.9 Ω resistor is used as a starting point and may or may not need to be adjusted depending on your board characteristics.

6.4.7.3 Single Channel DDRVREF and ODTCOMP

The DDR system memory reference voltage (VREF) is used by the DRAM devices and the MCH to determine the logic level being driven on the data, command, and control signals. VREF of the receiving device must track changes in VTERM to maximize DDR interface margin. However, VTERM and VREF *cannot* be the same power plane due to the sensitivity of the DRAM VREF buffers to the termination plane noise. When a voltage regulator is used, it must reference VTERM (see Figure 67). When a local resistor divider is used, VREF and VTERM must have a common source voltage between them (i.e., both VREF and V_{TT} are derived from the same voltage plane). Use equal value 1% resistors to derive DDR VREF (see Figure 68). Decouple VREF locally at the divider and DIMMs/MCH using one 0.1 µF capacitor per VREF pin.

Figure 67. DDR VREF Voltage Regulator

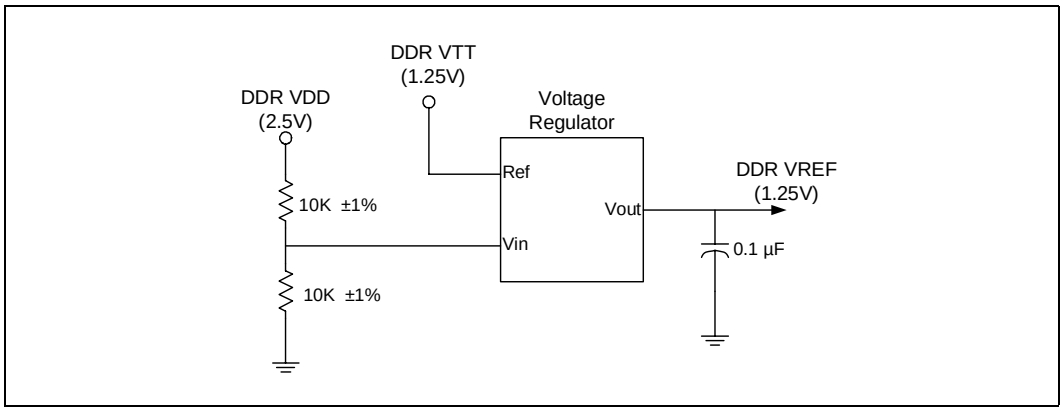
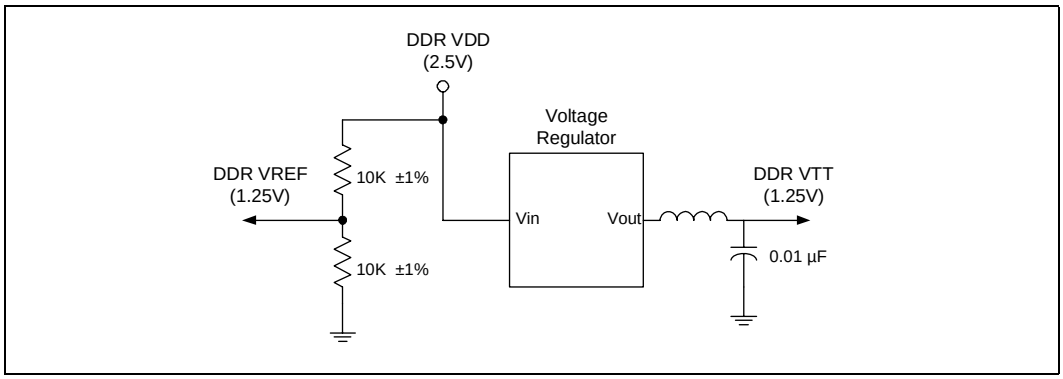


Figure 68. DDR VREF Voltage Divider

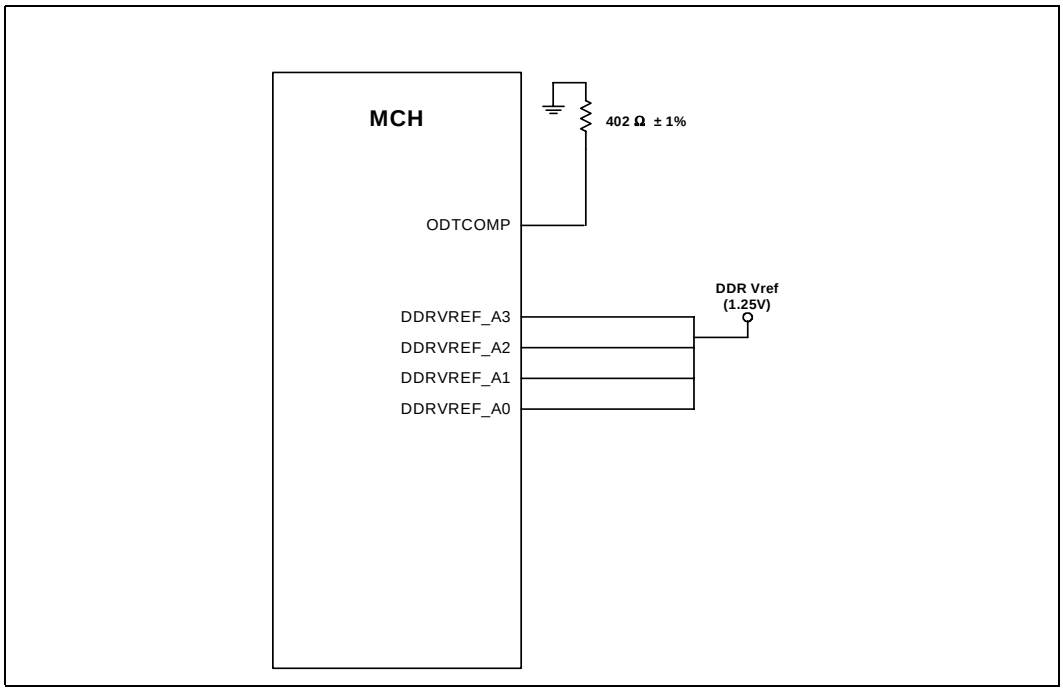


Note: Use equal resistor values for the DDR VREF supply.

The Intel® E7501 MCH includes active Read-cycle termination for all Source Synchronous signals (DQ and DQS signals). This On-Die-Termination Compensation (ODT) serves to control signal swing at the MCH receiver during Read-cycles. It does not function during Write-cycles. The ODTCOMP circuit has the effect of a weak pull-up of 200 Ω ± 15% to VTT. The value of termination is not adjustable. The ODTCOMP reduces ringbacks and overshoots, and in some cases may help reduce the need for series termination.

The MCH only has four VREFs per channel (eight total). Route DDRVREF and ODTCOMP traces 5-mils wide. The ODTCOMP pin is grounded through a 402 Ω pull-down resistor (see Figure 69).

Figure 69. Routing Single Channel DDRVREF and ODTCOMP



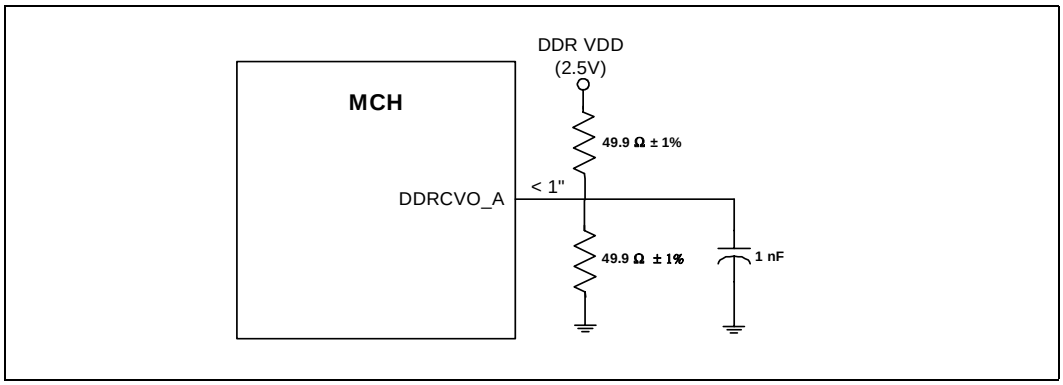
6.4.7.4 Single Channel DDRCVO

The MCH uses a compensation signal to adjust buffer characteristics and output voltage swing over temperature, process, and voltage skew. Calibration is done periodically by sampling the DDRCVO_A pins on the MCH. Place the voltage divider network (see Figure 70) within one inch of the MCH.

Table 50. DDRCVO Routing Guidelines

Parameter	Intel® E7501 MCH
Topology	Resistor Divider
Nominal Trace Width	15 mils
Nominal Trace Spacing	20 mils
Trace Length - MCH to Divider	< 1.0”

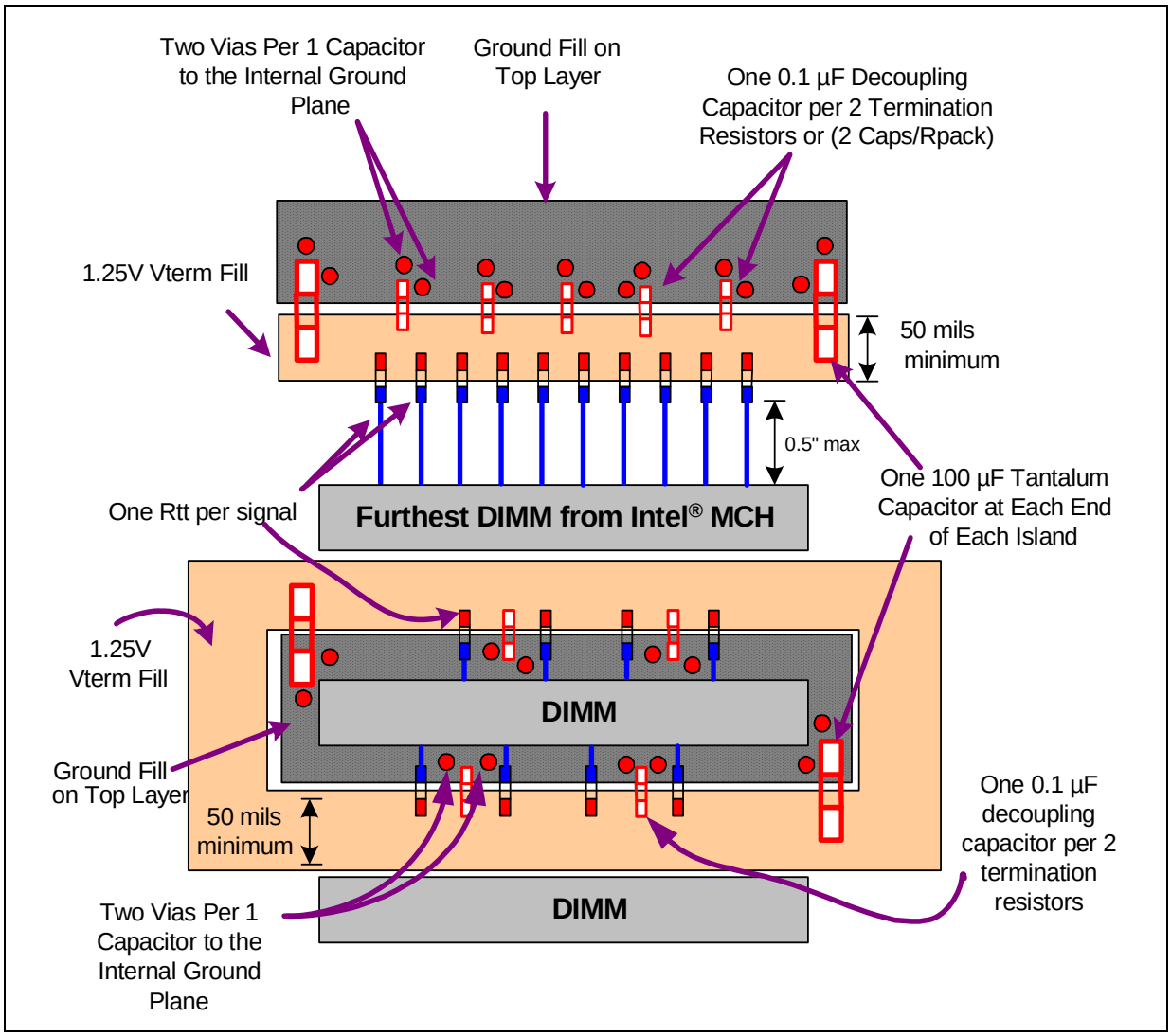
Figure 70. Single Channel DDRCVO Single Channel Routing Guidelines



6.4.8 Single Channel DDR Signal Termination and Decoupling

Place a 1.25 V termination plane on the top layer, just beyond (within 0.5 inch) the DIMM connector furthest from the MCH on each channel, as shown in Figure 71. The VTERM island must be at least 50-mils wide. Use this termination plane to terminate all DIMM signals, using one Rtt resistor per signal. Termination may be done with individual resistors or Rpack. Decouple the VTERM plane using one 0.1 µF decoupling capacitor per two termination resistors. Each decoupling capacitor must have at least two vias between the top layer ground fill and the internal ground plane. In addition, place one 100 µF Tantalum capacitor on each end of the termination island for bulk decoupling. Refer to Figure 71.

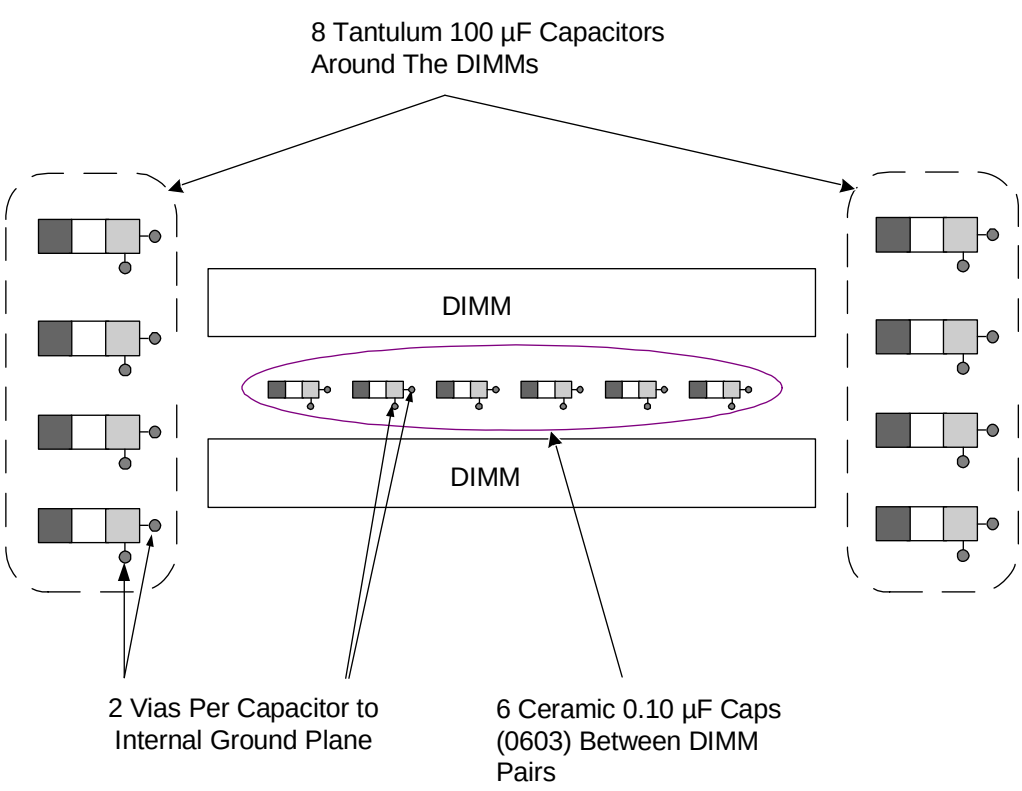
Figure 71. DDR VTerm Plane



6.4.9 2.5 V Decoupling Requirements

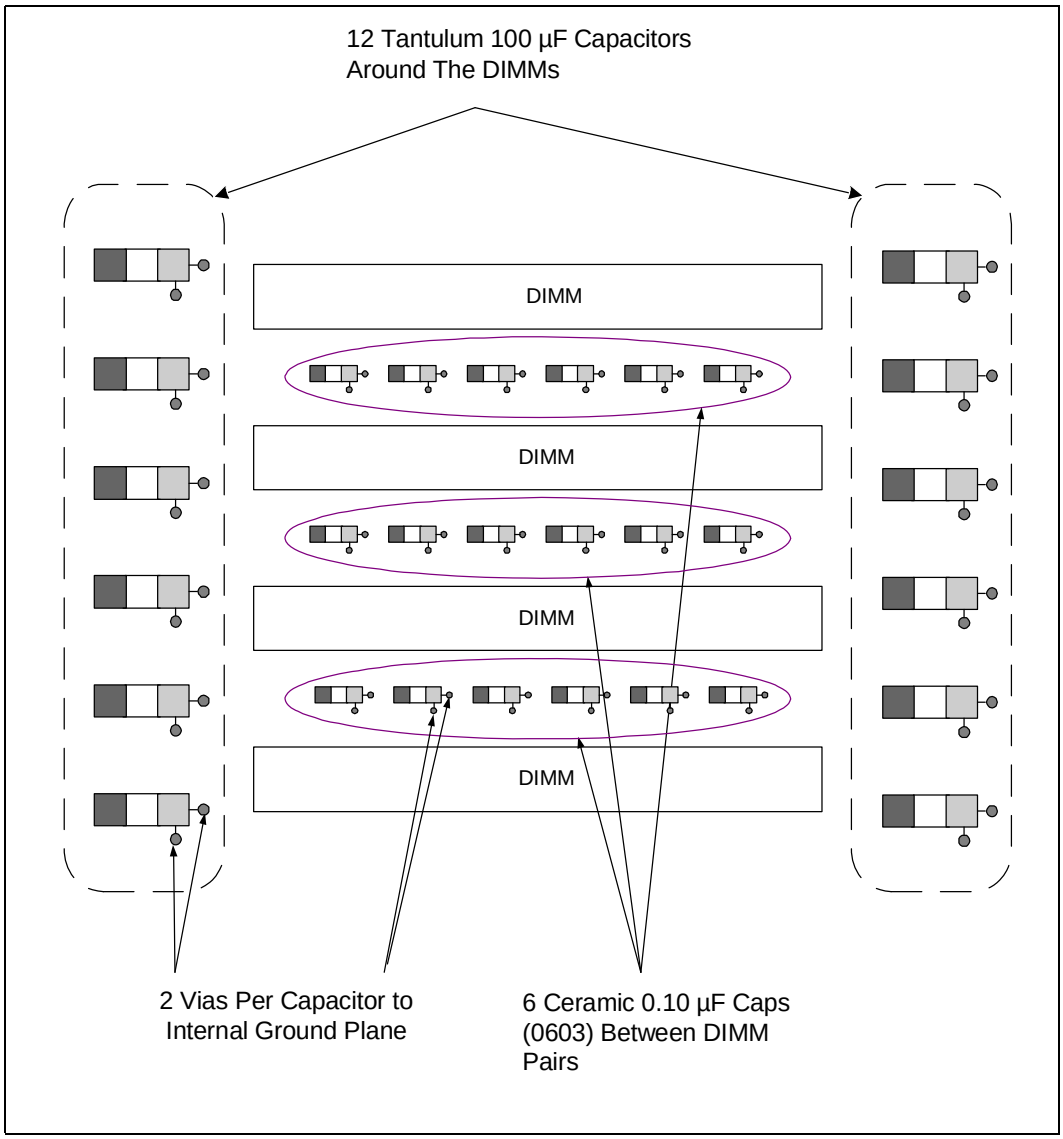
Decouple the DIMM connectors as shown in Figure 72 or Figure 73. Place six ceramic 0.1 µF (0603) capacitors between each pair of DIMM connectors. Place two Tantalum 100 µF capacitors around each DIMM connector and two additional Tantalum 100 µF capacitors per channel, keeping them within 0.5 inch of the DIMM connectors. Figure 72 depicts a single Channel 2-DIMM decoupling scheme and Figure 73 depicts a single channel 4-DIMM decoupling scheme.

Figure 72. Single Channel 2-DIMM Decoupling



NOTE: For each additional DIMM added per channel, add two additional 100 µF Tantalum capacitors around the DIMM, and add six additional 0.01 µF ceramic capacitors between each DIMM pair.

Figure 73. Single Channel 4-DIMM Decoupling



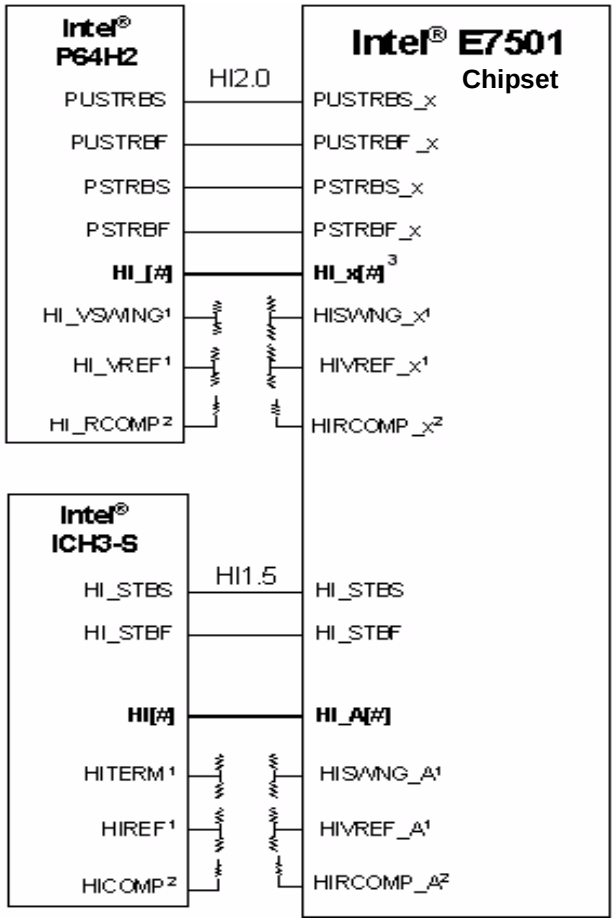
Hub Interface 7

7.1 Signal Naming Convention

Figure 74 has the Hub Interface 2.0 and Hub Interface 1.5 signal naming convention for each component. This figure is intended to give a quick naming cross reference to designers. The specific guidelines and implementation on these signals are given in the following sections.

Note: Throughout the document, the 'x' part of the MCH signal has been dropped for simplicity.

Figure 74. Signal Naming Convention on Both Sides of the Hub Interfaces



NOTES:
1. These signals have individual resistor dividers. For specific values, refer to Figure 78 and Figure 81.
2. These signals have individual pull-up resistors. For specific values, refer to Figure 79 and Figure 82.
3. Signal names for HI2.0 on the MCH: x = Hub Interface B, C, or D.

7.2 Hub Interface 2.0 Implementation

The MCH and Intel® P64H2 ballout assignments are optimized to simplify the Hub Interface routing between these devices. To allow for greater flexibility in design, a connector may be placed on the interface to access a Hub Interface 2.0 (HI2.0) agent that resides on an adapter card. The typical card implementation uses an extension to the 3.3 V PCI-64 connector that provides an additional 70 pins for HI2.0. Power, JTAG and SMBus signals are taken from the PCI portion of the connector. The remaining PCI signals are unused. This approach provides the flexibility to allow either a PCI/PCI-X card or a HI2.0 card to be populated in the slot.

For the 16-bit Hub Interface, HI[7:0] and HI[20] are associated with PSTRBF and PSTRBS, and HI[15:8] and HI[21] are associated with PUSTRBF and PUSTRBS. HI[18:16] are common clock signals; they are sampled using CLK66. The three Hub Interfaces on the MCH are functionally and electrically identical. Therefore, these guidelines apply to all three Hub Interfaces.

Table 51. Hub Interface 2.0 Signal/Strobe Association

Data Group	Associated Strobes
HI[7:0] HI[20]	PSTRBF PSTRBS
HI[15:8] HI[21]	PUSTRBF PUSTRBS

7.2.1 Hub Interface 2.0 High-Speed Routing Guidelines

This section documents the routing guidelines for the Hub Interface 2.0. The Hub Interface 2.0 signal groups are listed in Table 52. The general routing guidelines for the Hub Interface 2.0 signals are given in Table 53.

Table 52. Hub Interface 2.0 Signal Groups

Group	Signal	
	Intel® E7501 MCH	Intel® P64H2
Common Clock Signals	HI[18:16]_x	HI[18:16]
Source Synchronous Signals	HI[21:20]_x, HI[15:0]_x, PSTRBF, PSTRBS, PUSTRBF, PUSTRBS	HI[21:20],HI[15:0], PSTRBF, PSTRBS, PUSTRBF, PUSTRBS
Miscellaneous Signals	HIRCOMP_x, HISWNG_x, HIVREF_x	HI_RCOMP, HI_VSWING, HI_VREF

NOTE: x = B, C, or D

Table 53. Hub Interface 2.0 Routing Parameters

System Type	Trace Length Min-Max (For HI2.0 Device Down)	Trace Length Min-Max (For HI2.0 Card Solution)	Trace Z_0	Trace Width/Spacing	Breakout Width/Spacing
400 MHz	3” – 20”	3” – 14”	50 Ω ± 10%	5/15 mils (1:3)	5/5 mils (1:1) (max dist = 0.5”)

The Hub Interface signals must be routed directly from the MCH to Intel® P64H2 with all signals referenced to ground. Maintain a consistent ground reference plane at all times. In addition, route all signals within a data group (consisting of nine bits of data and a pair of strobes) on the same layer and reference them to the same ground plane. Keep layer transitions to a minimum. When a layer change is required, use only two vias per net and keep all signals within a data group on the same layer.

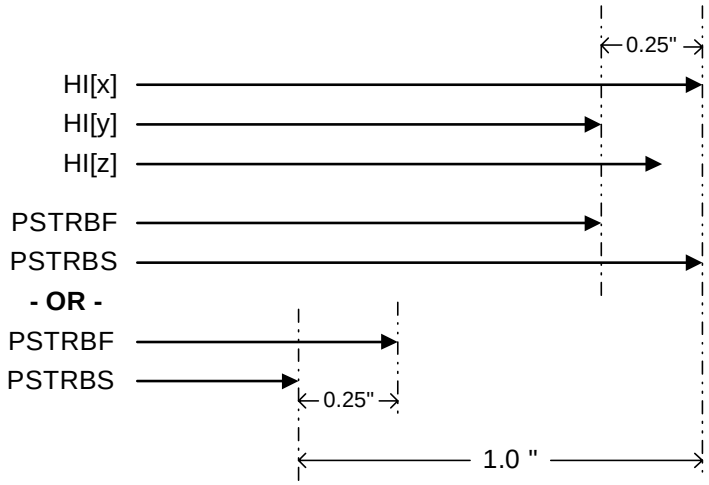
Route the Hub Interface 2.0 data signal traces 5 mils wide using the recommended stack-up. There must be 15-mils spacing between data signal traces 5/15 (1:3). Each strobe signal must have a minimum of 35 mils of spacing from any adjacent signals to minimize effects that cause signal degradation. To break out of the MCH and Intel P64H2 package, the Hub Interface data signals may be routed 5/5 (1:1). The signals must separate to 5/15 (or strobes to 5/35) within 0.5 inch of the outer ball array.

Hub Interface 2.0 requires package length compensation, which is similar to the system bus package length compensation. For Intel® E7501 chipset component package lengths, refer to the component datasheets.

For Hub Interface 2.0 devices on the motherboard, trace length matching of ± 0.25 inch (including package length compensation) is required among all signals within a data group. When the hub device is on an adapter, length matching of ± 0.125 inch (including package length compensation) is required among all signals within a data group. The Hub Interface strobe trace lengths must be 0 to 1.0 inch shorter than the longest Hub Interface data trace.

Figure 75 depicts the length matching rules for a hub device on the motherboard. All of the Hub Interface data signals must be length matched within 0.25 inch. The figure shows HI[x] and HI[y] with the maximum allowed difference in length, while HI[z] is somewhere in the middle. The strobes in each strobe pair (PSTRBF and PSTRBS; PUSTRBF and PUSTRBS) are also matched within 0.25 inch (see Figure 75). However, the absolute length of the strobe pair is adjusted according to the **longest Hub Interface data line**. The upper pair shows the case where one of the strobes is the same **exact** length as the longest Hub Interface data line (which is the longest possible length one of the strobes may be). In this case, the other strobe **must** be equal to or shorter than it, but by no more than 0.25 inch. The lower strobe pair shows the case where one of the strobes is **exactly** 1.0 inch shorter (see Figure 75) than the longest Hub Interface data line (which is the shortest possible length one of the strobes may be). In this case, the other strobe **must** be equal to or longer than it, but by no more than 0.25 inch.

Figure 75. Hub Interface 2.0 Length Matching



NOTES:
1. All signal lines with arrows depict the total length of the signal including the mother board trace length, MCH package trace length, and Intel® P64H2 package trace length.
2. PUSTRBF and PUSTRBS length matching is the same as for PSTRBF and PSTRBS.
3. This figure is only an example for an implementation with the device on the motherboard. For an implementation with the Hub Interface device on a riser card, simply replace both instances of 0.25 inch with 0.125 inch.
4. In the example above, HI[x], HI[y], and HI[z] represent Hub Interface data signals. The other six data signals in the group must also be matched within 0.25 inch. The associated strobe pair must be within 1.0 inch of the longest data signal.

The Hub Interface 2.0 has a minimum trace length requirement of three inches, and a maximum trace length requirement of 20 inches for a device on the motherboard implementation for all Hub Interface signals (using an internal routing layer on the recommended stack-up). However, for a device on an adapter card plugged in a Hub Interface 2.0 connector, the maximum motherboard trace length is 14 inches. This allows three inches for card routing and three inches for connector skew. For a riser card topology, the maximum trace length would reduce by three inches to (11-Y) inches, where Y is the riser card trace length. The riser must be built to not exceed the maximum trace length with the motherboard routed length.

Figure 76. Hub Interface 2.0 Routing Guidelines for Device Down Solutions

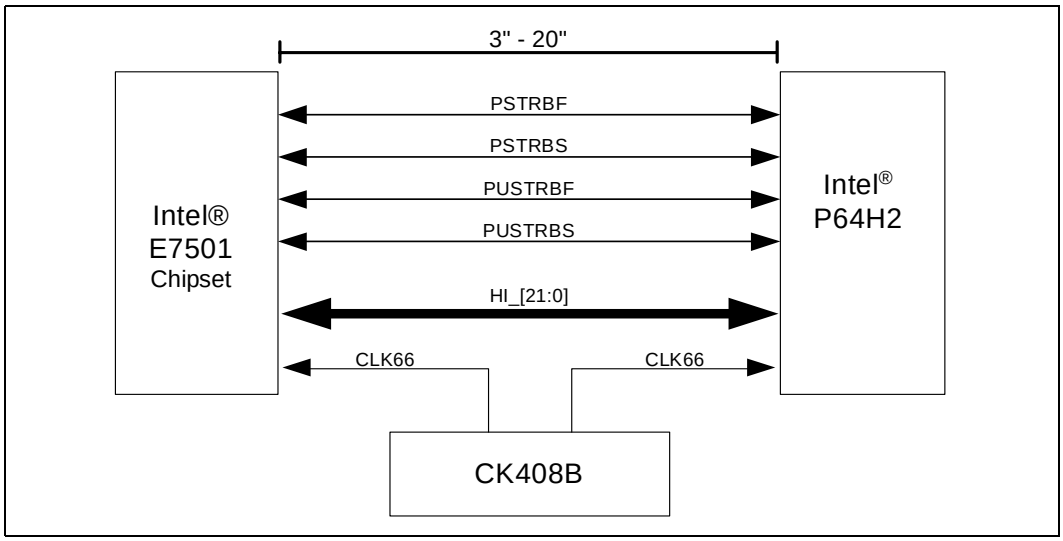
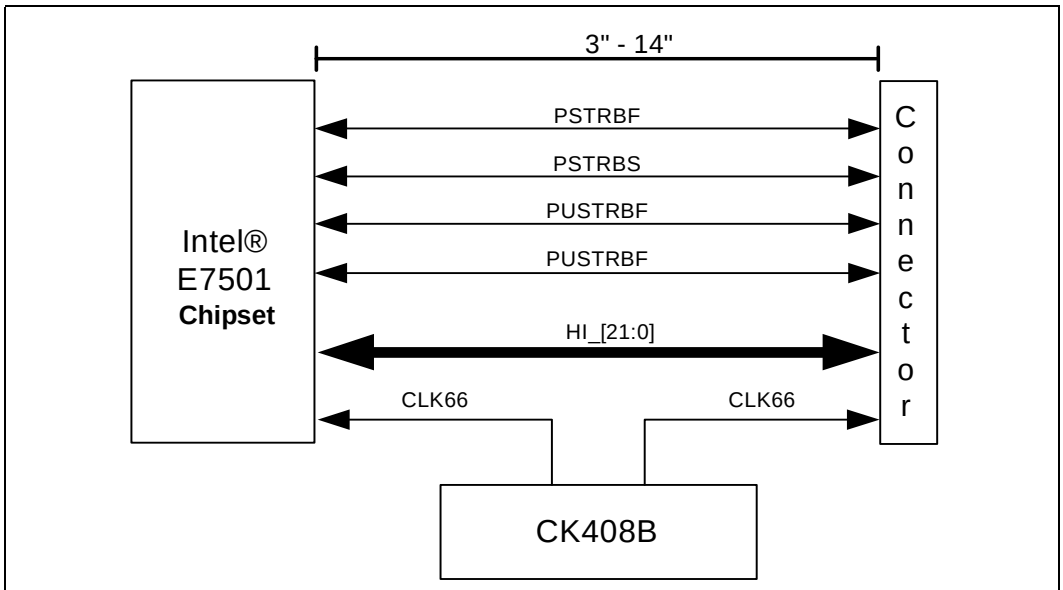


Figure 77. Hub Interface 2.0 Routing Guidelines for Hub Interface Connector Solutions



NOTE: The 14 inch maximum length allows for a single connector and three inch adaptor card trace length. The PCI connector is an equivalent three inch electrical length. The maximum motherboard trace length must be shortened when an additional trace is allocated for the trace of a riser card, making sure to also subtract the additional equivalent trace of a second connector.

7.2.2 Hub Interface 2.0 Generation/Distribution of Reference Voltages

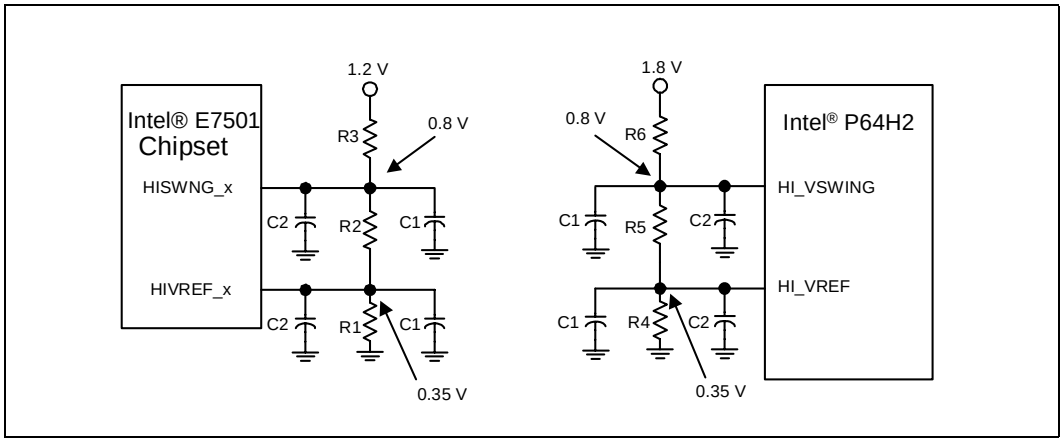
The nominal Hub Interface 2.0 reference voltage is 0.350 V ± 5%. Each Hub Interface 2.0 on the MCH has a dedicated HIVREF pin to sample this reference voltage. Similarly, the Intel® P64H2 has a dedicated reference voltage pin. In addition to the reference voltage, a reference swing

voltage must be supplied to control buffer voltage swing characteristics. The nominal Hub Interface 2.0 reference swing voltage should be 0.8 V ± 5% for the MCH and Intel® P64H2. Each Hub Interface 2.0 on the MCH has a dedicated HISWNG pin to sample this reference swing voltage. The Intel P64H2 has a dedicated reference swing voltage pin as well. Both of these reference voltages may be generated locally with a single voltage divider circuit. Figure 78 shows an example voltage divider circuit.

Table 54. Hub Interface 2.0 Reference Circuit Specifications

Reference Voltage Specification (V)	Reference Swing Voltage Specification (V)	1.2 V Voltage DIvider Circuit Recommended Resistor Values (Ω)	1.8 V Voltage DIvider Circuit Recommended Resistor Values (Ω)
0.350 ± 5%	For Intel® P64H2 = 0.8 ± 5% For MCH = 0.8 ± 5%	R1 = 392 ± 1% R2 = 499 ± 1% R3 = 453 ± 1%	R4 = 261 ± 1% R5 = 332 ± 1% R6 = 750 ± 1%

Figure 78. Hub Interface 2.0 with Locally Generated Voltage Divider Circuit



The resistor values R1, R2, R3, R4, R5, and R6 must be rated at ± 1% tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A 0.1 µF capacitor (C1 in the above circuits) should be placed close to each resistor divider, and a 0.01 µF bypass capacitor (C2 in the above circuits) should be placed near each reference voltage pin. when the length of the trace from the voltage divider to the pin is greater than one inch, place more than one 0.01 µF capacitor near the reference voltage pin. The trace length from the voltage divider circuit to the corresponding pin must be no longer than 3.5 inches.

Both the voltage reference and voltage swing reference signals should be routed 20 mils to 25 mils from all other signals.

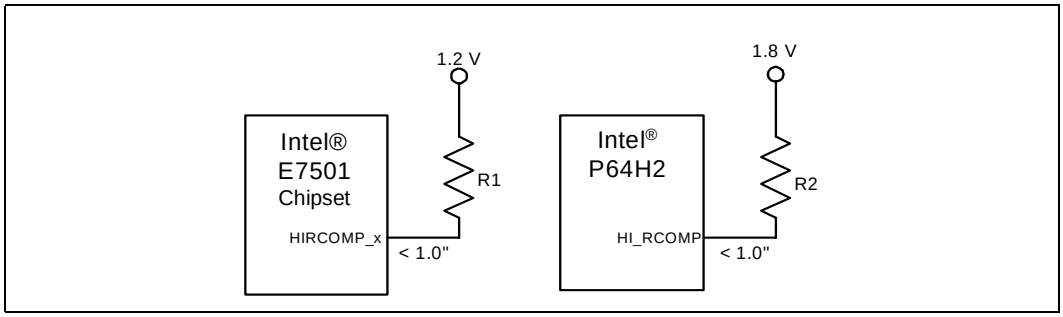
7.2.3 Hub Interface 2.0 Resistive Compensation

The Hub Interface uses a resistive compensation signal (HIRCOMP_x) to compensate buffer characteristics across temperature, voltage, and process. The HIRCOMP_x resistor values are given in Table 55. Figure 79 shows the RCOMP_x circuits. The length of the trace from the component to the pull-up must be less than 1.0 inch and have a trace impedance of 50 Ω ± 10%.

Table 55. Hub Interface 2.0 RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
Intel® MCH	50 Ω ± 10%	R1 = 24.9 Ω ± 1%	VCC1.2
Intel® P64H2	50 Ω ± 10%	R2 = 61.9 Ω ± 1%	VCC1.8

Figure 79. Hub Interface 2.0 RCOMP Circuits



7.2.4 Hub Interface 2.0 Decoupling Guidelines

To improve I/O power delivery, use two, 0.1 µF capacitors per component (i.e., MCH, Intel® P64H2). These capacitors should be placed within 150-mils of each package, adjacent to the rows that contain the Hub Interface. When the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1_8 / VCC1_2 side of the capacitors to the VCC1_8 / VCC1_2 power pins. Similarly, when layout allows, metal fingers running on the VCC1_8 / VCC1_2 side of the board should connect the ground side of the capacitors to the VSS power pins.

7.2.5 Unused Hub Interface 2.0 Interfaces

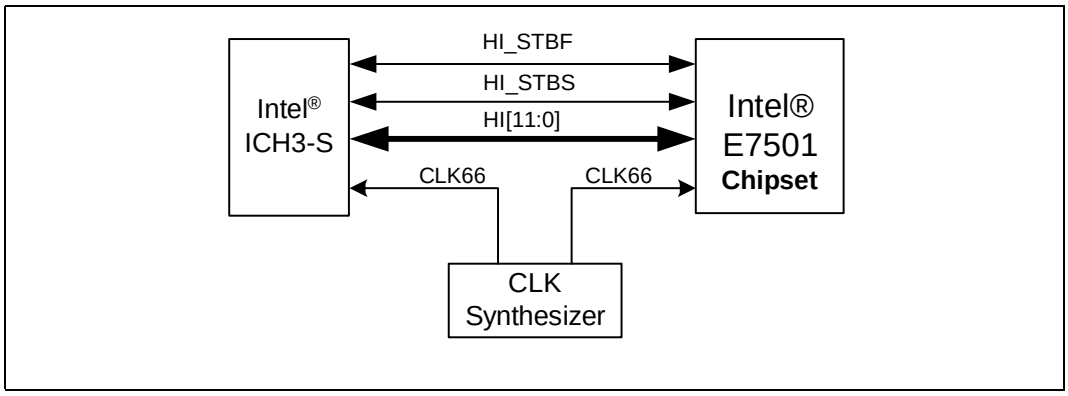
Terminate unused Hub Interface 2.0 interfaces as described below:

- All Hub Interface data and strobe, HIRCOMP_x, and HISWNG_x signals may be left as no connects.
- HIVREF must be tied to ground.

7.3 Hub Interface 1.5 Implementation

The Hub Interface 1.5 signals HI[7:0] are associated with HI_STBS and HI_STBF. For those familiar with Hub Interface 1.0, HI_STBF and HI_STBS are called HI_STB# and HI_STB, respectively.

Figure 80. 8-Bit Hub Interface 1.5 Routing



This section documents the routing guidelines for the Hub Interface 1.5 that is responsible for connecting the MCH to the ICH3-S. Hub Interface 1.5 supports parallel termination mode only; therefore, the DPRSLPVR pin on the ICH3-S must be left as No Connect (NC); this signal has an internal pull-down.

7.3.1 Hub Interface 1.5 High-Speed Routing Guidelines

The Hub Interface signals must be routed directly from the MCH to ICH3-S with all signals referenced to ground. Maintain a consistent ground reference plane at all times. In addition, route all signals within a data group (consisting of nine bits of data and a pair of strobes) on the same layer and reference them to the same ground plane. Keep layer transitions to a minimum. When a layer change is required, use only two vias per net and keep all signals within a data group on the same layer.

The Hub Interface 1.5 signal groups are listed in Table 56. The general routing guidelines for the Hub Interface 1.5 signals are given in Table 57.

Table 56. Hub Interface 1.5 Signal Groups

Group	Signals	
	Intel® E7501	Intel® ICH3-S
Common Clock Signals	HI_A[11:8]	HI[11:8]
Source Synchronous Signals	HI_A[7:0], HI_STBF, HI_STBS	HI[7:0], HI_STBF, HI_STBS
Miscellaneous Signals	HIRCOMP_A, HISWNG_A, HIVREF_A	HICOMP, HITERM, HIREF

Table 57. Hub Interface 1.5 Routing Parameters

System Type	Trace Length Min/Max	Trace Z_0	Trace Width/Spacing	Breakout Width/Spacing
266 MHz	3" – 20"	50 Ω ± 10%	5/15 mils (1:3)	5/5 mils (1:1) (max dist = 0.5")

Route the Hub Interface 1.5 data signal traces 5 mils wide using the recommended stack-up. There must be 15 mils spacing between data signal traces 5/15 (1:3). Each strobe signal must have a minimum of 35 mils of spacing from any adjacent signals to minimize effects that cause signal degradation. To break out of the MCH and ICH3-S package, the Hub Interface data signals may be routed 5/5 (1:1). The signals must separate to 5/15 (or strobes to 5/35) within 0.5 inch of the outer ball array.

For Hub Interface 1.5 devices on the motherboard, each strobe signal trace must be length matched within ± 1 mil, and each data signal trace must be matched with respect to the strobes within ± 0.1 inch. See Figure 75 for an example.

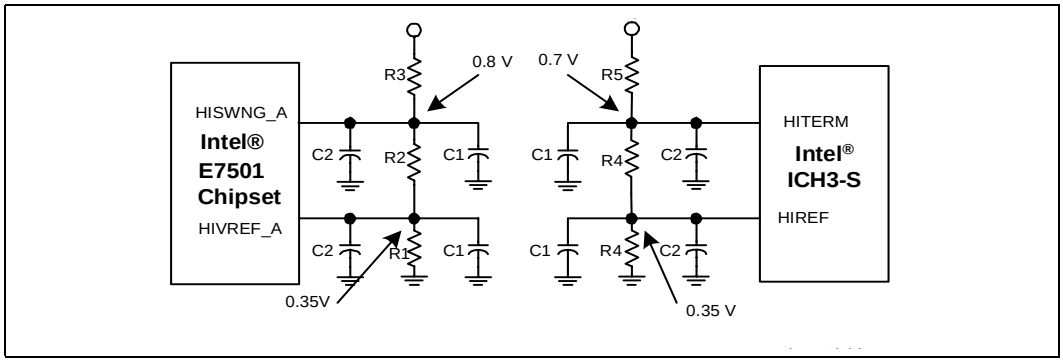
7.3.2 Hub Interface 1.5 Generation/Distribution of Reference Voltages

The nominal Hub Interface 1.5 reference voltage is 0.35 V ± 5%. The 8-bit Hub Interface on the MCH has a dedicated HIVREF pin to sample this reference voltage. In addition to the reference voltage, a reference swing voltage must be supplied to control buffer voltage swing characteristics. The nominal Hub Interface 1.5 reference voltage swing must be 0.8 V ± 5% for the MCH and 0.7 V ± 5% for the Intel® ICH3-S. This voltage is sampled by the MCH using HISWNG, and is sampled by the Intel ICH3-S using HITERM (see Table 58). Both HISWNG and HITERM may be generated locally with a single voltage divider circuit as shown in Figure 81.

Table 58. Hub Interface 1.5 Reference Circuit Specifications

Reference Voltage Specification (V)	Reference Swing Voltage Specification (V)	1.2 V Voltage Divider Circuit Recommended Resistor Values (Ω)	1.8 V Voltage Divider Circuit Recommended Resistor Values (Ω)
0.35 ± 5%	For ICH3-S = 0.7 ± 5% For MCH = 0.8 ± 5%	R1 = 392 ± 1% R2 = 499 ± 1% R3 = 453 ± 1%	R4 = 261 ± 1% R5 = 825 ± 1%

Figure 81. Hub Interface 1.5 Locally Generated Reference Divider Circuits



The values of R1, R2, R3, R4 and R5 must be rated at ± 1% tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A 0.1 µF capacitor (C1 in Figure 81) should be placed within 0.5 inch of each resistor divider, and a 0.01 µF bypass capacitor (C2 in Figure 81) should be placed within 0.25 inch of reference voltage pins. When the length of the trace from the voltage divider to the pin is greater than one inch, place more than one 0.01 µF capacitor near the reference voltage pin. The trace length from the voltage divider circuit to the HIREF and HUBREF pins must be no longer than 3.5 inches.

Both the voltage reference and voltage swing reference signals should be routed at least 20 mils to 25 mils from all other signals.

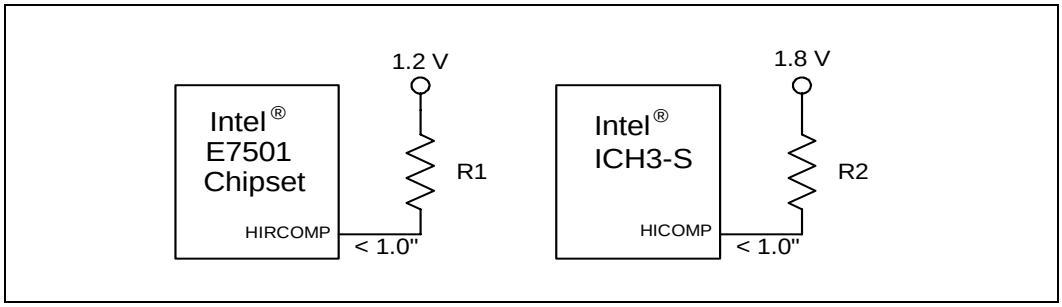
7.3.3 Hub Interface 1.5 Resistive Compensation

The Hub Interface uses a resistive compensation signal (RCOMP) to compensate buffer characteristics for temperature, voltage, and process. The HIRCOMP resistor values are given in Table 59. Figure 80 shows the RCOMP_x circuits. The length of the trace from the component to the pull-up must be less than 1.0 inch and have a trace impedance of 50 Ω ± 10%.

Table 59. Hub Interface 1.5 RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
MCH	50 Ω ± 10%	R1 = 24.9 Ω ± 1%	VCC1_2
Intel® ICH3-S	50 Ω ± 10%	R2 = 78.7 Ω ± 1%	VCC1_8

Figure 82. Hub Interface 1.5 RCOMP Circuits



7.3.4 Hub Interface 1.5 Decoupling Guidelines

To improve I/O power delivery, use two 0.1 µF capacitors per each component (i.e., the ICH3-S and MCH). These capacitors should be placed within 150 mils of each package, adjacent to the rows that contain the Hub Interface. When the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1_8 / VCC1_2 side of the capacitors to the VCC1_8 / VCC1_2 power pins. Similarly, when layout allows, metal fingers running on the VCC1_8 / VCC1_2 side of the board should connect the ground side of the capacitors to the VSS power pins.

Intel® 82870P2 (Intel P64H2) 8

The Intel® 82870P2 (Intel P64H2) is a peripheral chip that performs PCI/PCI-X bridging functions between the Hub Interface 2.0 and the PCI bus. The Intel P64H2 is an integral part of the Intel® E7501 chipset, bridging the MCH and the PCI/PCI-X bus. On the primary bus, the Intel P64H2 uses a 16-bit data bus to interface with the Hub Interface 2.0, and on the secondary bus, it supports two, 64-bit PCI/PCI-X bus segments. Either of the secondary PCI/PCI-X bus interfaces may be configured to operate in PCI or PCI-X mode. Each PCI/PCI-X interface contains an I/OxAPIC with 24 interrupts and a Hot-Plug controller that supports each PCI/PCI-X bus segment.

8.1 PCI/PCI-X Design Guidelines

The Intel P64H2 contains two PCI/PCI-X Interfaces. The PCI Interface has a 33-/66-MHz bus speed, and the PCI-X interface has a 66-/100-/133-MHz bus speed (see Table 60).

Table 60. PCI/PCI-X Frequencies

PCI		
Frequency	**Maximum Slots**	**Voltage**
33 MHz	6	3.3 V, 5 V
66 MHz	2	3.3 V
PCI-X		
Frequency	**Maximum Slots**	**Voltage**
66 MHz	4	3.3 V
100 MHz	2	3.3 V
133 MHz	1	3.3 V

NOTE: Frequencies specified are not the only ones supported, rather the maximum allowed in the configuration.

Intel simulated the PCI/PCI-X bus topologies shown in Section 8.1.2 and Section 8.1.3. If a platform implements a PCI/PCI-X topology not found in the following sections, it is the responsibility of the system designer to ensure the system meets the specified timings. The recommended lengths specified are not intended to replace thorough system simulations and validation.

8.1.1 General PCI-X Routing Guidelines

Most PCI-X signals are timing critical. The timing critical signals have length restrictions for propagation, setup, and hold requirements. Table 61 itemizes all timing critical and some of the non-critical signals. All of the topologies in the following sections itemize the lengths for the timing critical signals in configurations which Intel simulated.

Table 61. Simulated Timing Critical Signals

PxAD[63:0], PxC/BE[7:0]#, PxDEVSEL#, PxFRAME#, PxIRDY#, PxTRDY#, PxSTOP#, PxPERR#, PxSERR#, PxREQ[5:0]#, PxPLOCK#, PxPAR64, PxGNT[5:0]#, PCIXCAP, PxM66EN, Px_133EN, PxREQ64#, PxACK64#, PxIRQ[15:0]

The configurations enumerated in the following sections were simulated using the stack-up provided for 50 Ω ± 10% board impedance. Route the signals stripline with 5-mil wide traces with 10-mil wide spacing 5/10 (1:2).

PCI control signals always require pull-up resistors on the motherboard to ensure they contain stable values when no agent is actively driving the bus. This includes FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, INTA#, INTB#, INTC#, INTD#. In addition the 64-bit extension signals REQ64#, ACK64#, AD[63:32], C/BE[7:4]#, and PAR64 require pull-ups.

In the special case of a 64-bit bus that only contains 64-bit devices down, the pull-ups for AD[63:32], C/BE[7:4]# and PAR64 may not be needed. When the down device drives AD[63:32], C/BE[7:4]# and PAR64 during a 32-bit transaction then pull-ups are not necessary. When the down leaves device AD[63:32], C/BE[7:4]# and PAR64 floating during a 32-bit transaction then pull-ups may be required. Refer to the datasheet or specification for the 64-bit device down to determine when pull-ups are necessary.

The PCI/PCI-X bus has a maximum rating. PCI buses may be down shifted to a lower rating depending on the devices plugged into the bus. PCI/PCI-X buses may not be upshifted. Table 62 lists the ordering of PCI/PCI-X mode and frequencies. This means that when PCI-X 133 MHz is specified, the configuration may run at any mode or frequency below it (see Table 62). Topologies specified at PCI-X 100 MHz configurations may run at any speed below it, but not PCI-X 133 MHz. PCI 66 MHz configurations may be run at PCI 66 MHz, PCI-X 66 MHz, or below. PCI-X 66 MHz configurations *may not* run at PCI 66 MHz.

Table 62. PCI/PCI-X Mode and Frequency Ordering

Bus Mode and Frequency Ordering
PCI-X 133 MHz
PCI-X 100 MHz
PCI 66 MHz
PCI-X 66 MHz
PCI 33 MHz

Note: All topologies documented are stated at the highest rated bus mode and frequency for the motherboard topology.

8.1.2 PCI/PCI-X Routing Requirements (No Hot-Plug Switch)

The Intel® P64H2 supports a large number of PCI/PCI-X configurations. The basic topology of the bus is shown in Figure 83. Multiple slots are connected in a daisy chain topology with the device(s) down on the motherboard at the end of the daisy chain. Table 63 documents the lengths for the configurations Intel simulated. These topologies may also be used for Hot-Plug Parallel mode configurations where a Hot-Plug switch is not used.

Figure 83. Typical PCI/PCI-X Bus Topology

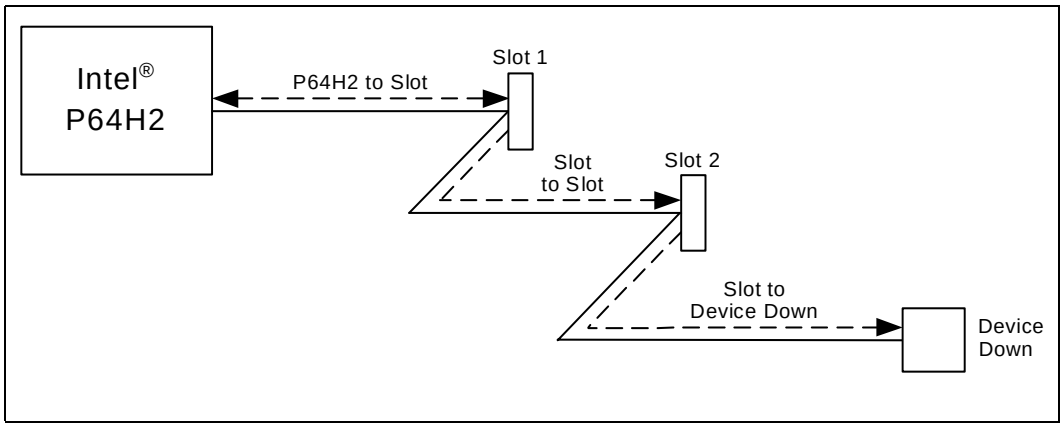


Table 63. Intel® P64H2 PCI/PCI-X Length Requirements

Configuration	Intel® P64H2 to Slot	Slot to Slot[1]	Slot to Device Down
33 MHz, 5 slots / 1 device down	2.0” – 7.0”	1.0”	3.0” – 6.0”
66 MHz, 4 slots / 0 devices down	6.0” – 8.0”	1.5”	N/A
100 MHz, 2 slots / 0 devices down	5.0” – 8.0”	1.0” – 1.75”	N/A
100 MHz, 2 slots / 1 device down	3.0” – 3.5”	0.75”	2.5” – 3.0”
100 MHz, 1 slot / 2 devices down	2.0” – 4.0”	(device to device) 5.0”	2.0”
133 MHz, 1 slot / 0 devices down	1.0” – 8.25”[2]	N/A	N/A
133 MHz, 0 slots / 1 devices down	1.25” – 10.0” Intel® P64H2 to device	N/A	N/A

NOTES:
1. During simulation, slot to slot lengths were held constant for some configurations. Therefore, no range may be given for these length requirements.
2. The 8.25 inches maximum only applies to the signals in the original 32-bit space. The 64-bit extension has a maximum length of 7.0 inches

8.1.3 PCI/PCI-X Hot-Plug Switch Routing Requirements

The Intel® P64H2 supports a large number of PCI/PCI-X Hot-Plug serial mode configurations. These configurations require the usage of a Hot-Plug switch. The Hot-Plug topology of the bus is shown in Figure 84. Hot-Plug switches are connected in a daisy chain topology with the device(s) down on the motherboard at the end of the daisy chain. Table 64 documents the lengths for the configurations that Intel simulated.

Figure 84. Typical Hot-Plug Topology

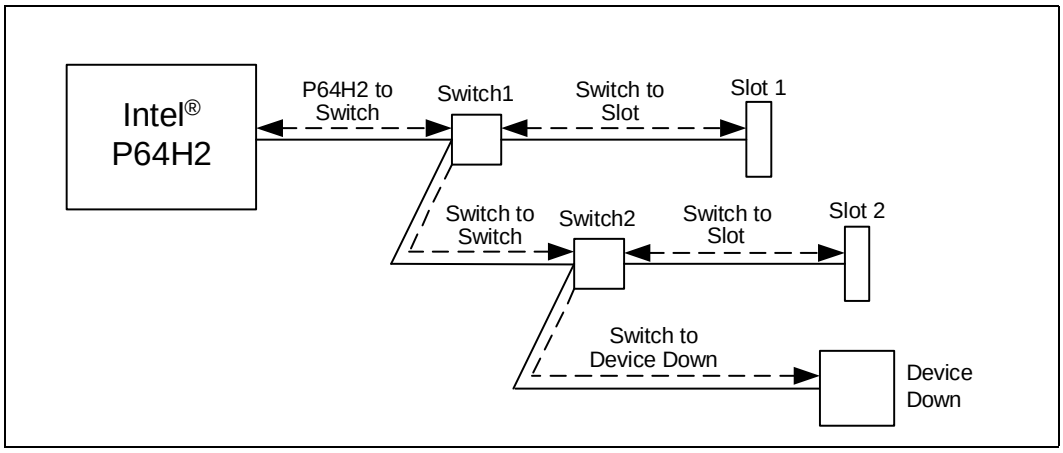


Table 64. Intel® P64H2 Hot-Plug Length Requirements

Configuration	Intel® P64H2 to Switch	Switch to Slot	Switch to Switch	Switch to Device Down
66 MHz, 4 Slots / 0 Device	2.0” – 6.0”	0.5” – 3.0”	0.5”	N/A
100 MHz, 2 Slots / 1 Device	2.5” – 3.5”	0.5” – 0.75”	0.75”	1.5” – 2.5”
100 MHz, 2 Slots / 0 Device	3.5” – 4.5”	1.0” – 1.75”	1.0” – 1.75”	N/A
100 MHz, 1 Slot / 1 Device	4.0” – 5.0”	1.75” – 2.25”	N/A	3.5” – 4.5”
133 MHz, 1 Slot / 0 Devices	1.5” – 3.5”	0.5” – 3.0”	N/A	N/A

NOTE: During simulation, slot to slot lengths were held constant for some configurations. Therefore, no range may be given for these length requirements.

8.1.4 Riser Card Topologies

The following guidelines are for systems that use a PCI-X riser card. A PCI-X riser card is card intended to extend the PCI-X signals. The riser card will contain a PCI-X card edge break-out and PCI-X connector slots. The riser’s PCI-X card edge break-out is plugged into the motherboard’s PCI-X slot and the riser’s PCI-X connector slots are used to plug in PCI-X adapter cards. These guidelines assume a PCI/PCI-X riser card with a 0.7 – 1.0 inch long trace length between slots. These simulations require the clocks for each device and riser card slot to be tuned within 500 ps, or 2.85 inches, of each other. For the riser slot to also support a standard PCI/PCI-X adapter card, the tuning must also include the adapter card length.

The following topologies denote an upper and lower portion to the length requirements. The PCI specification requires the original 32-bit signals to have a card length of 0.75 to 1.5 inches. The 64-bit extension specifies the additional signals in the extension to have a length of 1.75 inches to 2.75 inches. Upper indicates the signals on the extension while Lower indicates signals lying in the original 32-bit space.

In some of the riser card topologies, series resistors are required. These series resistors must be placed on all signals listed in Table 61.

Figure 85 shows a PCI-X channel with a single connector used for a riser. When a one slot riser is used, the channel may be run up to PCI-X 133 MHz. When a three slot riser is used, the channel may be run up to PCI 66 MHz.

Figure 85. PCI-X Riser Card Topology

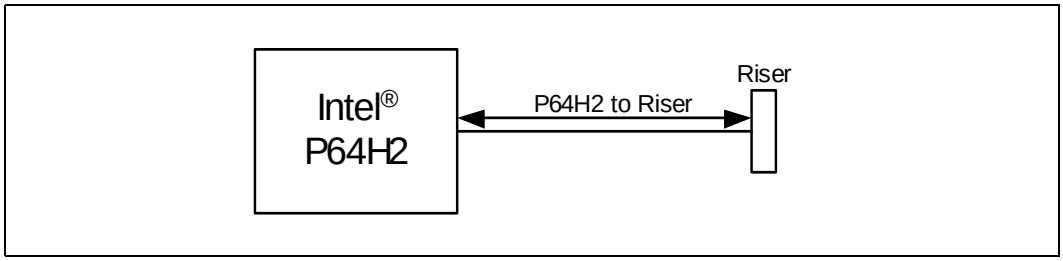


Table 65. PCI-X Riser Card Length Requirements

Configuration	Intel® P64H2 to Riser	
	Lower	Upper
PCI-X 133 MHz, 1 slot riser	1.0” – 7.25”	1.0” – 6.5”
PCI-X 66 MHz, 3 slot riser	1.0” – 8.25”	1.0” – 3.8”

Figure 86 shows a PCI-X channel with a device down before a riser card connector. If a one slot riser is used, the channel may be run up to PCI-X 100 MHz. If a three slot riser is used, the channel may be run up to PCI-X 66 MHz.

Figure 86. Device Down Before PCI-X Riser Card Topology

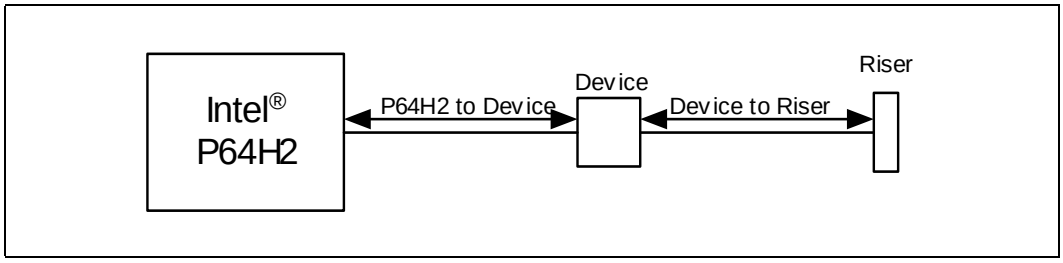


Table 66. Device Down Before PCI-X Riser Card Length Requirements

Configuration	Intel® P64H2 to Device		Device to Riser	
	Lower	Upper	Lower	Upper
PCI-X 100 MHz, 1 slot riser	0.0” – 6.0”	0.0” – 5.0”	0.0” – 6.0”	0.0” – 5.0
PCI-X 66 MHz, 3 slot riser	1.0” – 6.0”	1.0” – 4.0”	1.0” – 4.0”	1.0” – 4.0”

Figure 87 shows a riser card topology with a device down after the riser card connector. The one slot riser requires a 10 Ω series resistor on the riser between the riser fingers and the connector. The three slot riser configuration cannot be run at PCI 66 MHz. It requires a 15 Ω series resistor on the baseboard between the Intel® P64H2 and the Riser connector closer to the riser. A second 15 Ω resistor is also need on the riser itself between the riser card fingers and the first connector.

Figure 87. Device Down After PCI-X Riser Card Topology

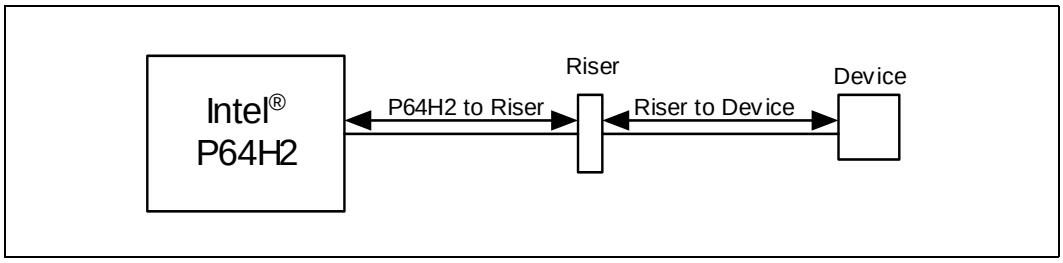


Table 67. Device Down After PCI-X Riser Card Length Requirements

Configuration	Intel® P64H2 to Riser		Riser to Device	
	Lower	Upper	Lower	Upper
PCI-X 100 MHz, 1 slot riser	0.0” – 8.0”	0.0” – 8.0”	0.0” – 8.0”	0.0” – 8.0”
PCI-X 66 MHz, 3 slot riser	1.0” – 6.0”	1.0”– 4.0”	1.0” – 4.0”	1.0” – 2.25”

Figure 88 shows a device down before a PCI-X riser card. Place a 22 Ω series resistor on the stub to riser leg, close to the riser itself. This topology may only be run at PCI 66 MHz or below.

Figure 88. Device Down with Stub Before PCI-X Riser Card Topology

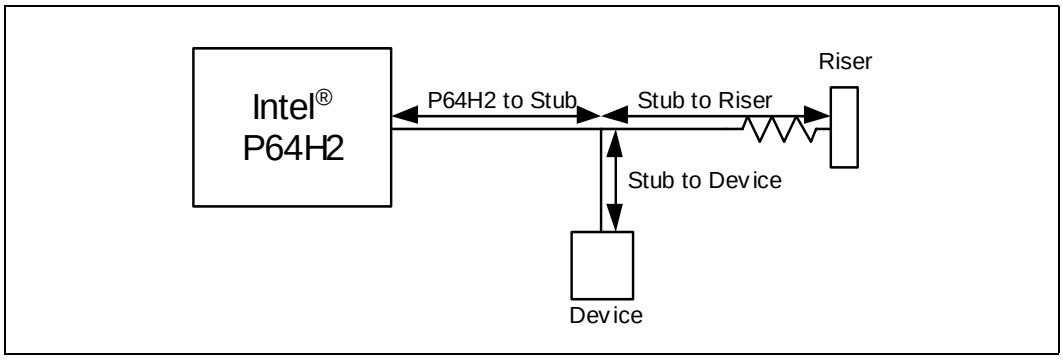


Table 68. Device Down with Stub Before PCI-X Riser Card Length Requirements

Configuration	Intel® P64H2 to Stub		Stub to Riser		Stub to Device	
	Lower	Upper	Lower	Upper	Lower	Upper
PCI-X 66 MHz, 3 slot riser	3.3” – 5.6”	3.3” – 4.6”	0.2” – 2.3”	0.2” – 1.3”	1.9” – 6.5“	1.9” – 5.5”

8.1.5 PCI-X Two Devices Down-Routing Requirements

The following guideline is for a system that uses two devices down on a single PCI-X channel. A good example of usage for this configuration is an I/O Processor or RAID device and a SCSI controller. This channel may be run at PCI-X 100 MHz.

Figure 89. Two Devices Down Card Topology

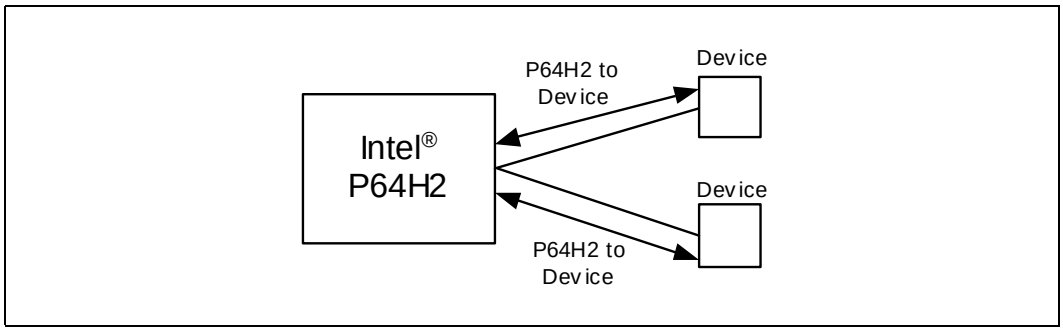


Table 69. Two Devices Down Length Requirements

Configuration	Intel® P64H2 to Device	
	Lower	Upper
100 MHz PCI-X	3.5” – 7.0”	3.5” – 7.0”

8.1.6 Clock Configuration

All PCI clocks must be disabled in the BIOS for any unused/unpopulated PCI/PCI-X slots. The PxPCLKO[5:0] pins may each be disabled by writing to the Disable PCLKOUT 5 – 0 bits (DPCLK, bits 15:10, configuration register offset 40h in each bridge). These clocks function the same in serial and dual-slot parallel modes. In serial mode, the PxPCLKO[5:0] signals are all driven low when the clock to the slot is disabled by the Hot-Plug controller, regardless of the DPCLK bits. Once the Hot-Plug controller connects the clock to the slot, these clocks are enabled again—which clocks are enabled does depend on DPCLK at this point. It is expected that PxPCLK0 may be connected to the PCI slot in single-slot parallel mode.

Figure 90. Hot-Plug Clock Topology

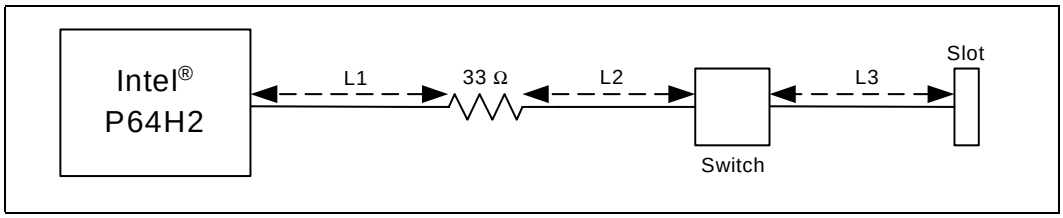


Table 70. Hot-Plug Clock Routing Length Parameters

Clock Speed	L1 (inches)	L2 (inches)	L3 (inches)
66 MHz	0.25 – 1.0	(L_{fbi} – L3) – 2.523	0.75 – 1.25
100 MHz	3.5 – 4.5	0.25 – 0.5 = L3	0.25 – 0.5 = L2
133 MHz	1.5 – 2.5	0.5 – 1.0 = L3	0.5 – 1.0 = L2

Figure 91. No Hot-Plug Clock Topology

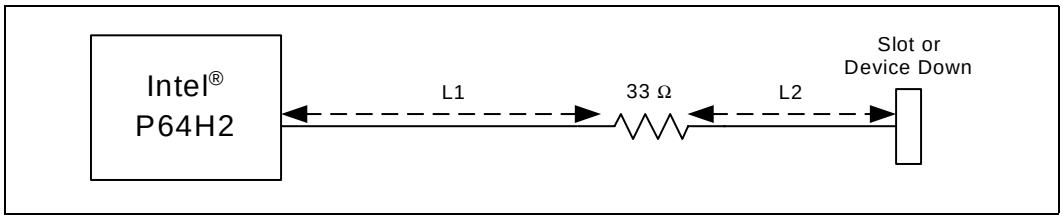


Table 71. No Hot-Plug Clock Routing Length Parameters

Clock Speed	L1 (inches)	L2 (inches) Slot	L2 (inches) Device Down
33 MHz Slot	3.5 – 5.5	0.5 – 5.0	2.9 – 7.9
66 MHz	3.5 – 4.5	0.5 – 1.0	3.0 – 3.5
100 MHz	≤ 1.0	L_{fbi} – 2.5[1]	L_{fbi}[1]
133 MHz	≤ 1.0	L_{fbi} – 2.5[1]	L_{fb}[1]

1. The clock signal and feedback loops are closely related. L2 and L_{fbi} may be any length, but need to be tuned to each other ± 25 mils. Refer to Figure 91 for L2, and Figure 92 for L_{fbi}.

8.1.7 Loop Clock Configuration

You must tie PxPCLKO6 to PxPCLKI because this clock always runs and is needed by the internal PCI PLLs to properly align output signals with the external clocks by removing clock insertion delay. The PxPCLKO6 signal does not have to be routed through a bus switch before returning to PxPCLKI.

Figure 92. Loop Clock Topology

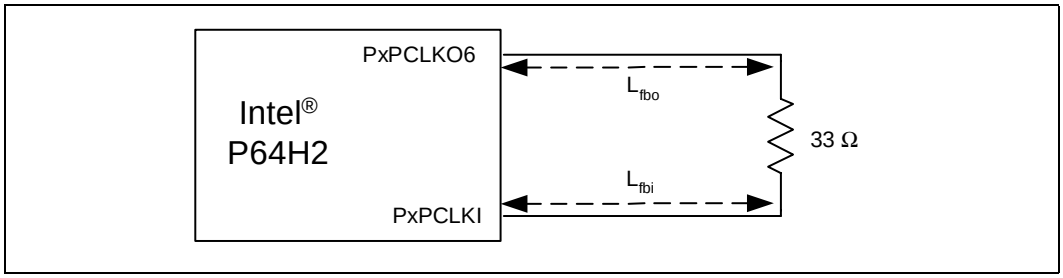


Table 72. Loop Clock Configuration Routing Length Parameters

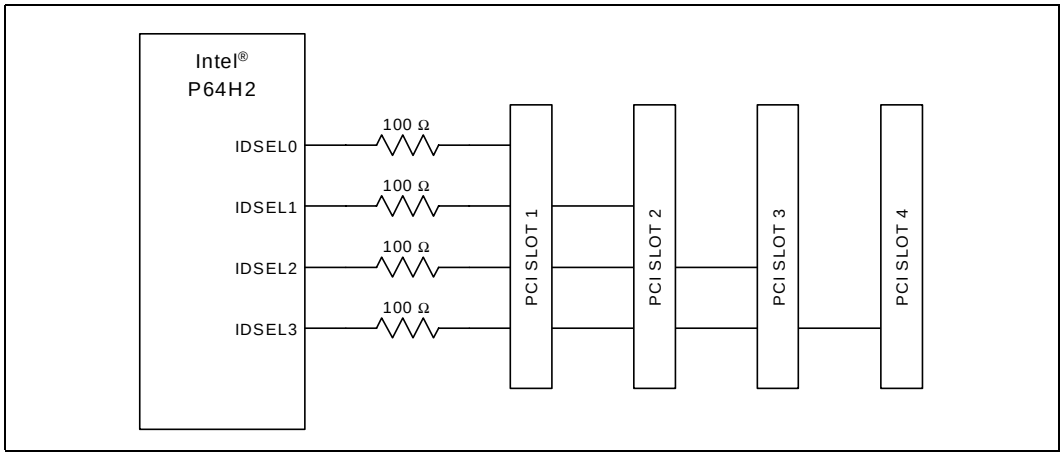
Clock Speed / Configuration	L_{fbo} (inches)	L_{fbi} (inches)
33 MHz / No HP	3.5 – 5.5	2.9 – 7.9
66 MHz / No HP	4.5 – 5.5	3.9 – 4.9
66 MHz / With HP	0.25 – 1.0	7.0 – 12.0
100 MHz / No HP	≤ 1.0	L2 + 2.5†
100 MHz / With HP	4.5 – 5.5	3.9 – 4.9
133 MHz / No HP	0.25 – 1.0	L2 + 2.5†
133 MHz / With HP	3.5 – 4.0	5.5 – 5.7

† L_{fbi} must be the same length (± 25 mils) as any device clock length on the same bus. If a device is down on the motherboard, L_{fbi} = L2. If a devices is on an expansion card, L_{fbi} = L2 + 2.5 inches. Refer to Figure 91 for L2 and Figure 92 for L_{fbi}.

8.1.8 IDSEL Implementation

Designers should use a 100 Ω series coupling resistor on the IDSEL signal when implementing PCI-X. Though the *PCI-X Addendum PCI Local Bus Specification*, Revision 1.0, calls for a 2 kΩ resistor, the current specification, *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a, allows for other resistor values. See Figure 93 for an example of how to implement the coupling resistor. IDSEL mapping per Intel® P64H2 pin is arbitrary. However, AD16 is reserved.

Figure 93. IDSEL Sample Implementation Circuit



8.1.9 SMBus Address

The SMBus interface does not have configuration registers. The SMBus address is set by the states of pins PAGNT[5:4] and PBGNT[5:4] when PWROK is asserted as described in Table 73. Refer to the *Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet* for a more detailed description of Intel® P64H2 strap latching.

Table 73. SMBus Address Configuration

Bit	Value
7	1
6	1
5	PAGNT[5]
4	0
3	PAGNT[4]
2	PBGNT[5]
1	PBGNT[4]

NOTE: There is no bit 0 because it is the read/write direction indicator.

8.2 Hot-Plug Implementation

The Intel® P64H2 contains two integrated Hot-Plug controllers (one per PCI/PCI-X interface) that operate independently. These integrated controllers may be individually disabled or configured to operate in one of the three defined modes of operation: single-slot parallel mode, dual-slot parallel mode, and serial mode. This section describes each of these three modes of operation, as well as switch and button implementation and the Hot-Plug Standard Usage Model.

8.2.1 Standard Usage Model

To define a programming model for the Hot-Plug controllers (HPC), it is necessary to make some assumptions about the interface between a user and a Hot-Plug system that must be incorporated into the hardware solution. The programming model includes two LED indicators, one optional push button, and a sensor on the manually-operated retention latch (MRL) for each supported slot. See Section 8.2.2, “Hot-Plug Switch Implementation” for MRL and attention button implementation. Section 8.2.3, “LED Indicator Outputs” describes the LED indicators. For more information on the Hot-Plug Standard Usage Model, see the *PCI Standard Hot-Plug Controller and Subsystem Specification*, Revision 1.0.

Caution: Users must always notify the operating system through a software user interface or Attention Button (when present) before opening an MRL. This allows the operating system to isolate the slot from the PCI bus and unload the device driver gracefully. The unexpected opening of an MRL leads to unpredictable results, including data corruption, abnormal termination of the operating system, or damage to card or platform hardware.

8.2.1.1 Hot-Removals

1. User selects a slot holding an enabled add-in card and requests that slot be disabled.
   a. User interacts with a software user interface to request that slot be disabled.
   b. User confirms request. System software validates request and initiates slot power down sequence. Power Indicator LED blinks.

   – OR –

   a. User presses momentary Attention Button at that slot.
   b. Software interprets change on HxPRSNT# pin as a push button event. (Software ignores second interrupt on HxPRSNT# caused by button release.) Power Indicator LED blinks.
   c. User is permitted to cancel request within five seconds by pressing Attention Button again.
   d. System software validates request and initiates slot power down sequence.
2. System software waits for card activity on the PCI bus to end.
3. Hot-Plug controller asserts RST#, bus signals and clock lines are disconnected from the slot, and power is removed.
4. Power Indicator LED is turned off. User may open MRL, disconnect cables, and remove card.

8.2.1.2 Hot-Insertions

1. User selects an empty, disabled slot and opens MRL.
2. User inserts add-in card, closes MRL, and attaches cables to card.
3. User requests that slot be enabled.
   a. User requests that slot be enabled through a software user interface.
   b. Power Indicator LED next to slot blinks while system software validates request.

   – OR –

   a. User presses momentary Attention Button at that slot.
   b. Software interprets change on HxPRSNT# pin as a push button event. (Software ignores second interrupt on HxPRSNT# caused by button release.)
   c. User is permitted to cancel request within five seconds by pressing Attention Button again.
   d. Power Indicator LED next to slot blinks while system software validates request.
4. Hot-Plug controller asserts RST# to the slot; main supply voltages are present at the slot.
5. Clock and bus signals are connected to the slot; RST# is deasserted.
6. Power Indicator LED is turned on. The slot is ready for operation.

8.2.2 Hot-Plug Switch Implementation

The mechanical design for the chassis should include a manually-operated retention latch (MRL) that holds an add-in card in the slot. Each MRL should have an associated switch, optical device, or other type of sensor to indicate whether a slot is open or closed. (Note that the terms opened and closed do not necessarily indicate the electrical state of the switches used, but should be thought of as a mechanical door that enables or disables cards to be installed or removed.) A slot may be auto-powered down should someone attempt to remove a card without first notifying the operating system. The mechanical design should be such that it is impossible for an expansion card to be removed without the switch indicating that the slot is open. The mechanical design should also prevent inadvertent switch openings.

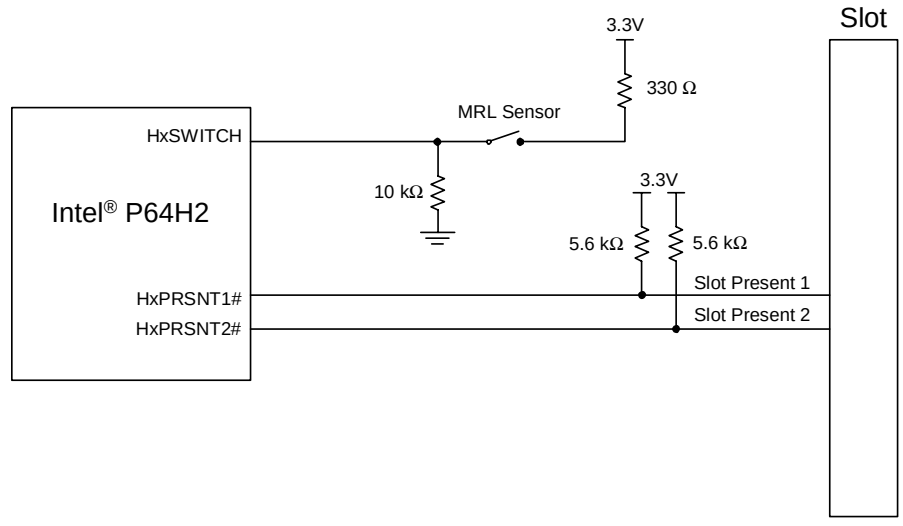
An 'attention button' is a momentary-contact push-button. This button serves to invoke the Hot-Plug service so that an adapter may be added or removed without the use of a software interface. Support for the attention button is optional.

8.2.2.1 Manually-Operated Retention Latch Sensor

The HxSWITCH signal is monitored by the Hot-Plug controller to determine whether or not a slot should be powered. The MRL sensor, or slot switch, should be connected to the HxSWITCH pin such that it drives this pin low to indicate that the slot is closed and may be powered on. When the signal is driven high, it indicates that the slot should immediately be powered off. The MRL Sensor in represented schematically as a switch in Figure 94.

The Slot Present pins on each Hot-Plug slot are connected directly to the HxPRSNT2# and HxPRSNT1# pins on the Intel® P64H2.

Figure 94. Manually-Operated Retention Latch Sensor

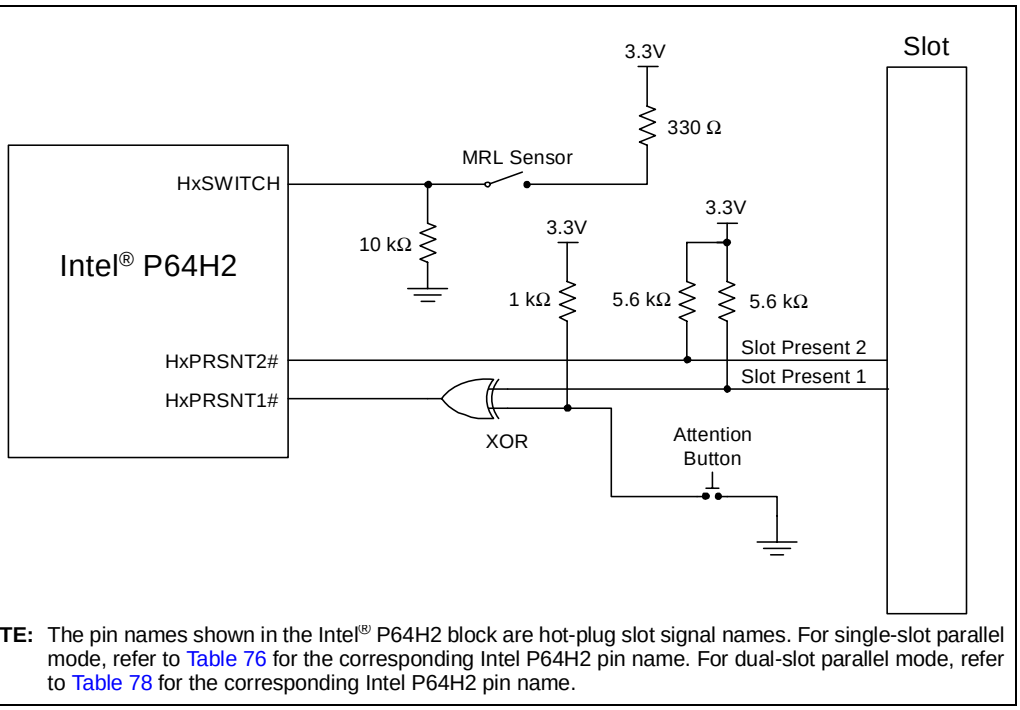


NOTE: The pin names shown in the Intel® P64H2 block are Hot-Plug slot signal names. For single-slot parallel mode, refer to Table 76 for the corresponding Intel P64H2 pin name. For dual-slot parallel mode, refer to Table 78 for the corresponding Intel P64H2 pin name.

8.2.2.2 Optional Attention Button

The Attention Button state is observed on the slot-specific HxPRSNT1# pin. An exclusive-OR (XOR) gate is inserted between the Slot Present signal and the Hot-Plug controller as shown in Figure 95. A momentary contact button is connected to the other input of the XOR gate. When the button is in the released state, the Slot Present signal is unaffected. When the button is actively being pressed/asserted, the Slot Present signal is inverted, signaling the Hot-Plug controller to commence slot power up/down sequence.

Figure 95. Attention Button Implementation



NOTE: The pin names shown in the Intel® P64H2 block are hot-plug slot signal names. For single-slot parallel mode, refer to Table 76 for the corresponding Intel P64H2 pin name. For dual-slot parallel mode, refer to Table 78 for the corresponding Intel P64H2 pin name.

8.2.3 LED Indicator Outputs

The PCI Hot-Plug Standard Usage Model assumes that the platform provides two indicators per slot. Indicators must be placed in close proximity to their associated slot so that the association between the indicators and the Hot-Plug slot is clear.

The LED output signals for all modes of the Intel® P64H2 Hot-Plug controller operation are active high. In all cases, the green LED is the power indicator, and the amber LED is the attention indicator.

8.2.4 Hot Plug Interrupt Routing Requirements

The recommended method to support hot plug is to route the SCI interrupt output signal on the Intel P64H2 (pin PAIRQ7) to an available GPIO pin on the ICH3. A System Controlled Interrupt (SCI) is a system interrupt used by hardware to notify the operating system of ACPI events. SCI is an active-low, shareable, level-triggered interrupt.

8.2.5 Hot-Plug Interrupt Routing Requirements

The recommended method to support Hot-Plug is to route the SCI interrupt output signal on the Intel® P64H2 (pin PAIRQ7) to an available GPIO pin on the ICH3. A System Controlled Interrupt (SCI) is a system interrupt used by hardware to notify the operating system of ACPI events. SCI is an active-low, shareable, level-triggered interrupt.

8.2.6 Disabling/Enabling an Intel® P64H2 Hot-Plug Controller

8.2.6.1 Hot-Plug Strapping Options

The HPx_SLOT[2:0] strapping pins are used to enable and disable the Hot-Plug controller. Table 74 lists the strapping options associated with these pins, and the modes of operation they enable.

Table 74. Hot-Plug Mode

HPx_SLOT [2:0]	Hot-Plug Mode	Notes
000	Hot-Plug Disabled	
001	1-Slot (Parallel Mode)	1
010	2-Slot (Parallel Mode)	2
011	3-Slot (Serial Mode)	3
100	4-Slot (Serial Mode)	3
101	5-Slot (Serial Mode)	3
110	6-Slot (Serial Mode)	3
111	Reserved	

NOTES:
1. Refer to Section 8.2.7 for single-slot parallel mode operation.
2. Refer to Section 8.2.8 for dual-slot parallel mode operation.
3. Refer to Section 8.2.9 for serial mode operation.

8.2.6.2 Hot-Plug Registers' Visibility

The Hot-Plug controller function is completely hidden when the controller is disabled by the slot strapping pins HPx_SLOT[2:0], and the registers are not available or accessible.

8.2.7 Single-Slot Parallel Mode

Single-slot parallel mode allows for only one card to be connected to the PCI/PCI-X Bus. This mode should be used only to implement a one-slot Hot-Plug solution because of the behavior of the PCI bus when in this mode. No serialization/deserialization logic is required for this mode of operation.

8.2.7.1 Required Additional Logic

Single-slot parallel mode requires a power switch to be used to turn the slot power on and off. Single-slot parallel mode does not require the use of a bus and clock switch. In this mode, all PCI signals are driven to ground whenever a PCI card is to be disconnected.

When the platform supports PME# or SMBus connections to the slot, isolation logic is required to disconnect these signals prior to inserting or removing a card. See the *PCI Hot-Plug Specification*, Revision 1.1, for implementation details. The HxSWITCH signal may be used to control the isolation switches.

8.2.7.2 PCI Clock

In single-slot parallel mode, it is expected that PxPCLK 0 is used.

8.2.7.3 Debounced Hot-Plug Switch Input

The switch inputs (PxIRQ15 in this case—see Table 76) to the Hot-Plug controller do not require any debouncing logic in this mode. This logic is contained within the Intel® P64H2. The POWERON value for this input is determined by BIOS. However, it is recommended that BIOS define a logic 0 to represent that the slot may be powered on.

8.2.7.4 Comparator Circuit for PCIXCAP1/PCIXCAP2 Pins

A comparator circuit is required for properly decoding the PCI/PCI-X capability of the slot. Refer to the *PCI Local Bus Specification*, Revision 2.2, for this circuit. For more information on the reference circuit, refer to Section 8.2.8.9. The board designers may also use Table 75 as a reference for non-Hot-Plug designs only.

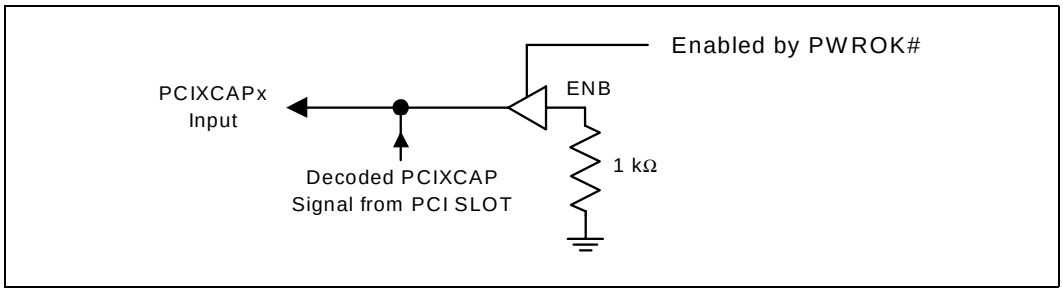
Table 75. Frequency Matrix for Non-Hot Plug Designs

Frequency	M66EN	PCIXCAP1	PCIXCAP2	133EN
PCI 33	0	X	X	X
PCI 66	1	0	0	X
PCI-X 66	X	1	0	X
PCI-X 100	X	1	1	0
PCI-X 133	X	1	1	1

8.2.7.5 Tri-State Buffer or 2:1 Multiplexer for HPx_SLOT[2:0]

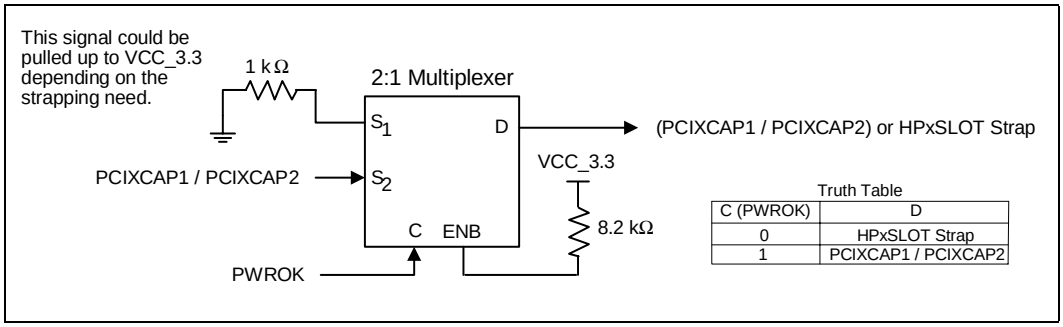
The HPx_SLOT[2:0] pins are pull-ups/pull-downs for determining the slot count and mode of operation for the Intel® P64H2 Hot-Plug controller. The strapping value on these pins is latched on the rising edge of PWROK. In single-slot parallel mode, these pins also function as the PCIXCAP1A, PCIXCAP2A, and PCIXCAP1B inputs to the controller. Logic must exist to preserve the slot count value when the system is in reset (PWROK signal is low). Figure 96 shows an example of the tri-state buffer circuit.

Figure 96. Tri-State Buffer Circuit Example



It is also possible to accomplish this strapping requirement using a 2:1 multiplexer. The PWROK signal may be used to enable the tri-state buffer. The decision is left up to the individual designer on which method to use. See Figure 97 for an example of the optional multiplexer circuit.

Figure 97. MUX Circuit Example



8.2.7.6 Hot-Plug Multiplexed Signals in Single-Slot Parallel Mode

The Hot-Plug signals that connect to the controller are shown in Table 76. In Table 76 the 'Signal' column refers to the name of the slot pin when in single-slot mode. The 'Bus A' and 'Bus B' columns represent the corresponding Intel® P64H2 pins.

Table 76. Single-Slot Parallel Mode Hot-Plug Signal Table

Signal	Type	Multiplexed With				Note
		Bus A	Ball #	Bus B	Ball #	
HxSWITCHA	I	**PAIRQ15**	F4	**PBIRQ15**	F1	
HxFAULTA#	I	**PAIRQ14**	E4	**PBIRQ14**	E1	
HxPRSNT2A#	I	**PAIRQ13**	F5	**PBIRQ13**	D1	

NOTES:
1. HPx_SLOT [N] are pull-ups/pull-downs. When in dual-slot parallel mode, the external logic that decodes the three-state value of PCIXCAP from the card must actively drive these signals to either logic 1 or logic 0 to overcome the value of the pull-up/pull-down, and must be tri-stated during reset and while the card is not connected to avoid damaging the slot count value.
2. The Intel® P64H2 must drive this signal to its corresponding state shown in Table 77 in case the system is set up for single-slot parallel mode so that LEDs are in the appropriate state (off), and the Q-switches remain disconnected. Note that the placement of the signals should be such that the value driven by the Intel P64H2 in dual-slot parallel mode is the same value it would have driven when in serial mode.
3. In both parallel modes, the BUSEN# and CLKEN# signals become active low instead of active high as they are during serial mode.

Table 76. Single-Slot Parallel Mode Hot-Plug Signal Table

Signal	Type	Multiplexed With				Note
		Bus A	Ball #	Bus B	Ball #	
HxPRSNT1A#	I	**PAIRQ12**	E5	**PBIRQ12**	C1	
HxM66ENA	I/O	**PAIRQ11**	D5	**PBIRQ11**	B1	
HxPCIXCAP1A	I	**HPASLOT2**	D20	**HPBSLOT2**	D23	1
HxPCIXCAP2A	I	**HPASLOT1**	C20	**HPBSLOT1**	C23	1
HxRESETA#	O	**PAGNT5**	E22	**PBGNT5**	G4	2
HxGNLEDA	O	**HPA_SOC**	A19	**HPB_SOC**	A24	2
HxAMLEDA	O	**HPA_SOL**	D19	**HPB_SOL**	C22	2
HxBUSENA#	O	**HPA_SORR#**	A18	**HPB_SORR#**	A22	2, 3
HxCLKENA#	O	**HPA_SIL#**	D24	**HPB_SIL#**	D24	2, 3
HxPWRENA	O	**HPA_SOD**	B19	**HPB_SOD**	C24	2

NOTES:
1. HPx_SLOT [N] are pull-ups/pull-downs. When in dual-slot parallel mode, the external logic that decodes the three-state value of PCIXCAP from the card must actively drive these signals to either logic 1 or logic 0 to overcome the value of the pull-up/pull-down, and must be tri-stated during reset and while the card is not connected to avoid damaging the slot count value.
2. The Intel® P64H2 must drive this signal to its corresponding state shown in Table 77 in case the system is set up for single-slot parallel mode so that LEDs are in the appropriate state (off), and the Q-switches remain disconnected. Note that the placement of the signals should be such that the value driven by the Intel P64H2 in dual-slot parallel mode is the same value it would have driven when in serial mode.
3. In both parallel modes, the BUSEN# and CLKEN# signals become active low instead of active high as they are during serial mode.

Table 77. Hot-Plug Controller Output Signal Reset Values

Signals	Reset Value
Px_GNT[5:3]	011
HPx_SOC	0
HPx_SIC	0
HPx_SOL	0
HPx_SOLR	0
HPx_SOD	0
HPx_SORR#	1
HPx_SOR#	0
HPx_SIL#	1

8.2.7.7 SMBus Address Considerations

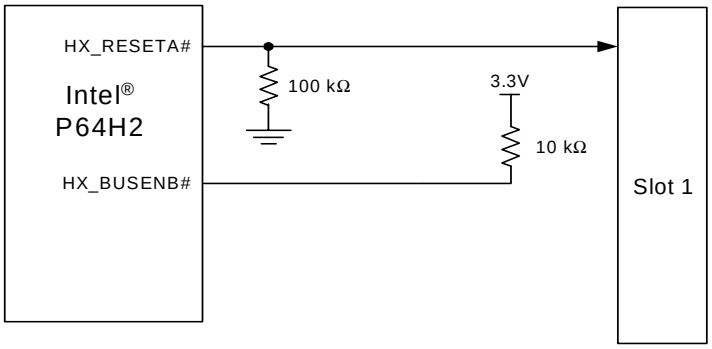
In single-slot parallel mode, the SMBus address strap pins listed in Table 73 are multiplexed with Hot-Plug control signal HxRESETA#. Therefore, it is recommended that the following technique be used for determining an SMBus address. Pull the PAGNT5 (RESETA#) signal to ground through a 100 kΩ ± 5% resistor. This may keep the reset signal active until the Intel® P64H2 is

ready for it to become deasserted. Pull the PAGNT4 (HxBUSENB#) signal to 3.3 V through a 10 kΩ ± 5% resistor. The Intel® P64H2 may be able to drive this signal to ground when the signal must be asserted.

8.2.7.8 Single-Slot Parallel SMBus Circuit

Figure 98 shows the single-slot parallel SMBus circuit.

Figure 98. Single-Slot Parallel SMBus Circuit



NOTE: The pin names shown in the Intel® P64H2 block are hot-plug slot signal names. For single-slot parallel mode, refer to Table 76 for the corresponding Intel P64H2 pin name.

8.2.7.9 Pull-Ups/Pull-Downs in Single-Slot Parallel Mode

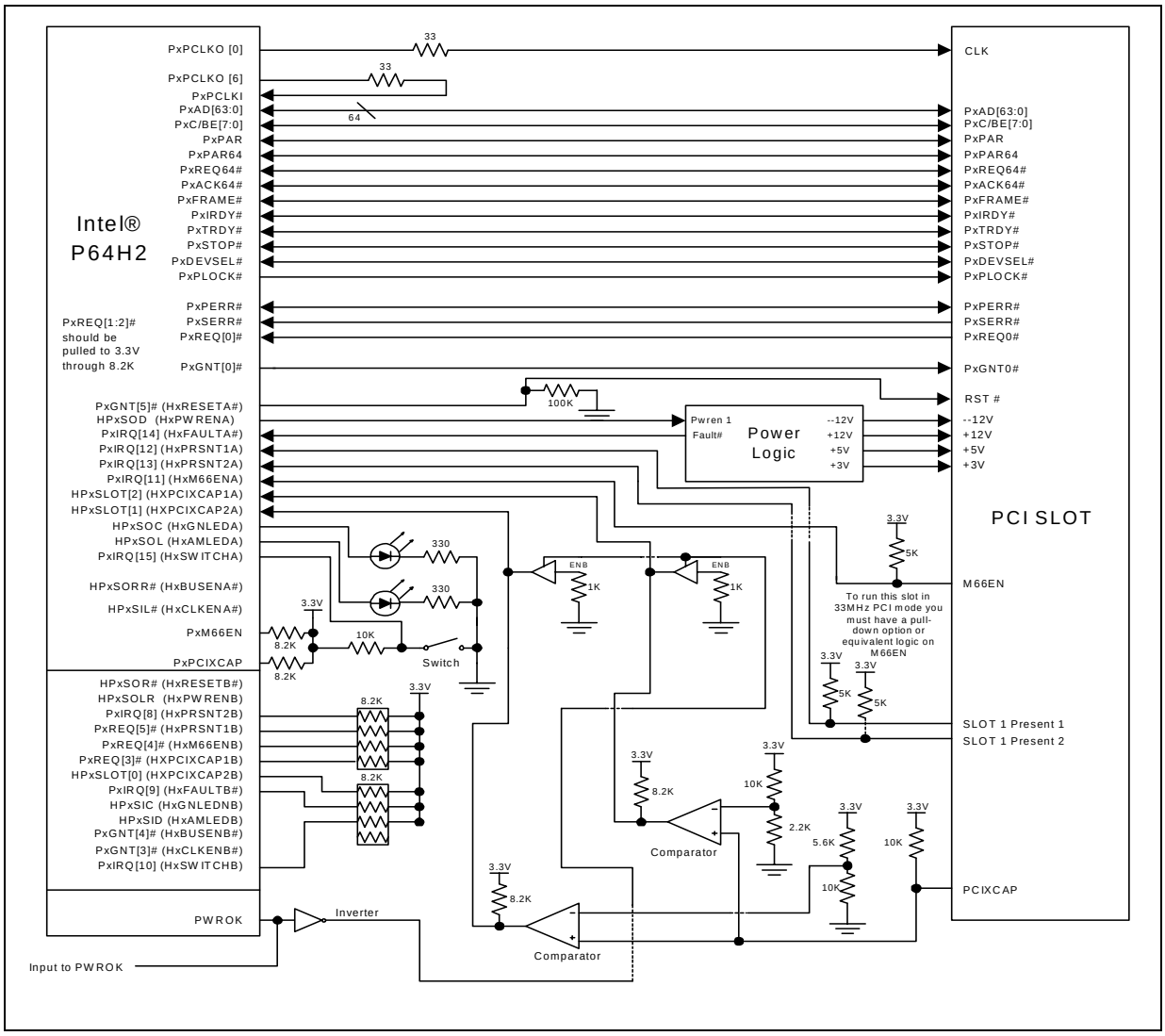
All PCI signals should follow the *PCI Local Bus Specification*, Revision 2.2, pull-up requirements whether they are multiplexed or not. All unused input signals should be pulled to 3.3 V through an 8.2 kΩ ± 5% resistor to keep them from floating.

Table 76 defines which multiplexed signals are to be used with single-slot parallel mode. Note that whether in single or dual-slot parallel mode, all signals from Table 76 are actually multiplexed even though only the signals listed in Table 77 are used. As a result, all unused input signals listed in Table 76 must be pulled to 3.3 V through an 8.2 kΩ ± 5% resistor to keep them from toggling.

8.2.7.10 Reference Schematic for Single-Slot Parallel Mode

Note that the schematic in Figure 99 is based on definition and simulation of the Intel® P64H2. The schematic has not been fully validated.

Figure 99. Reference Schematic for Single-Slot Parallel Mode



8.2.8 Dual-Slot Parallel Mode

Dual-slot parallel mode is used when it is desirable to have two slots that are Hot-Pluggable. No serialization/deserialization logic is required for this mode of operation.

8.2.8.1 Required Additional Logic

Dual-slot parallel mode requires a power switch to be used to turn the slot power on and off. Dual- slot parallel mode also requires the use of a bus and clock switch. Unlike single-slot parallel mode, the PCI signals are not driven to ground whenever a PCI card is to be disconnected. In addition, dual-slot parallel mode requires auto bus and clock disable logic to immediately disable the PCI bus and clock when the power fault signal (from the power switch) goes active.

When the platform supports PME# or SMBus connections to the slots, isolation logic is required to disconnect these signals before inserting or removing a card. See *PCI Hot-Plug Specification*, Revision 1.1, for implementation details.

8.2.8.2 Debounced Hot-Plug Switch Input

The switch inputs (PAIRQ[15] and PAIRQ[10] in this case—see Table 78) to the Hot-Plug controller do not require debouncing logic in this mode. This logic is contained within the Intel® P64H2.

8.2.8.3 Comparator Circuit for PCIXCAP1/PCIXCAP2 Pins

A comparator circuit is required for properly decoding the PCI/PCI-X capability of the slot. Refer to the *PCI Local Bus Specification*, Revision 2.2, for this circuit. An example of this circuit is also contained in the reference schematics. For a frequency reference matrix, see Table 75.

8.2.8.4 Tri-State Buffer or 2:1 Multiplexer for HPx_SLOT[2:0]

As with single-slot parallel mode, the HPx_SLOT[2:0] pins are pull-ups/pull downs for determining the slot count and mode of operation for the Intel P64H2 Hot-Plug controller in dual-slot parallel mode. The strapping value on these pins is latched on the rising edge of PWROK. In dual- slot parallel mode these pins also function as the PCIXCAP1A, PCIXCAP2A, and PCIXCAP1B inputs to the controller. Logic must exist to preserve the slot count value when the system is in reset (PWROK signal is low). Connecting a tri-state buffer or a 2:1 multiplexer to these pins to pull the line high or low accordingly may do this. The PWROK signal may be used to enable the tri-state buffer to drive the line high or low or select the multiplexer signal. See Figure 96 for example of a tri-state buffer circuit, and Figure 97 for a 2:1 multiplexer circuit example.

8.2.8.5 HPx_SID Output Signal

In dual-slot parallel mode, this signal is connected to the Amber LED slot status indicator. During a reset operation, this signal goes high which could flicker the LED on and confuse the user. To avoid having this LED turn on during a reset operation (PWROK logic zero), it is possible to use a buffer to electrically isolate this LED from the HPx_SID signal. The PWROK input signal to the Intel P64H2 should be used to enable this buffer. See the dual-slot parallel mode reference schematic in Section 8.2.8.9 for an example of this circuit.

8.2.8.6 Pull-Ups/Pull-Downs in Dual-Slot Parallel Mode

All PCI signals should follow the *PCI Local Bus Specification*, Revision 2.2, pull-up requirements whether they are multiplexed or not. Any unused input signals should be pulled to 3.3 V through an 8.2 kΩ ± 5% resistor to keep them from floating.

8.2.8.7 Hot-Plug Multiplexed Signals in Dual-Slot Parallel Mode

The Hot-Plug signals that connect to the controller are listed in Table 78. In Table 78 the ‘Signal’ column refers to the name of the slot pin when in dual-slot mode. The ‘Bus A’ and ‘Bus B’ columns represent the corresponding Intel P64H2 pins.

Table 78. Dual-Slot Parallel Mode Hot-Plug Signals Table

Signal	Type	Multiplexed Intel® P64H2 Pin				Note
		Bus A	Ball #	Bus B	Ball #	
HxSWITCHA	I	**PAIRQ15]**	F4	**PBIRQ15**	F1	
HxFAULTA#	I	**PAIRQ14]**	E4	**PBIRQ14**	E1	
HxPRSNT2A#	I	**PA_IRQ13]**	F5	**PBIRQ13**	D1	
HxPRSNT1A#	I	**PAIRQ12]**	E5	**PBIRQ12**	C1	
HxM66ENA	I/O	**PAIRQ11]**	D5	**PBIRQ11**	B1	
HxPCIXCAP1A	I	**HPA_SLOT2]**	D20	**HPB_SLOT2**	D22	1
HxPCIXCAP2A	I	**HPA_SLOT1]**	C20	**HPB_SLOT1**	C23	1
HxRESETA#	O	**PAGNT5]**	E22	**PBGNT5**	G4	3
HxGNLEDA	O	**HPA_SOC**	A19	**HPB_SOC**	A24	3
HxAMLEDA	O	**HPA_SOL**	D19	**HPB_SOL**	C22	3
HxBUSENA#	O	**HPA_SORR#**	A18	**HPB_SORR#**	A22	3, 4
HxCLKENA#	O	**HPA_SIL#**	C21	**HPB_SIL#**	D24	3, 4
HxPWRENA	O	**HPA_SOD**	B19	**HPB_SOD**	C24	3
HxSWITCHB	I	**PAIRQ10**	C5	**PBIRQ10**	F2	
HxFAULTB#	I	**PAIRQ9**	B5	**PBIRQ9**	E2	
HxPRSNT2B#	I	**PAIRQ8**	A5	**PBIRQ8**	D2	
HxPRSNT1B#	I	**PAREQ5**	F24	**PBREQ5**	G3	
HxM66ENB	I/O	**PAREQ4**	F21	**PBREQ4**	H4	
HxPCIXCAP1B	I	**PAREQ3**	F19	**PBREQ3**	H2	
HxPCIXCAP2B	I	**HPA_SLOT0**	A20	**HPB_SLOT0**	B2	1
HxRESETB#	O	**HPA_SOR#**	B18	**HPB_SOR#**	A21	3
HxGNLEDB	O	**HPA_SIC**	A23	**HPB_SIC**	A23	3
HxAMLEDB	O	**HPA_SID**	B24	**HPB_SID**	B24	2
HxBUSENB#	O	**PAGNT4**	F23	**PBGNT4**	H5	3, 4
HxCLKENB#	O	**PAGNT3**	F20	**PBGNT3**	H3	3, 4
HxPWRENB	O	**HPA_SOLR**	C19	**HPB_SOLR**	B22	3

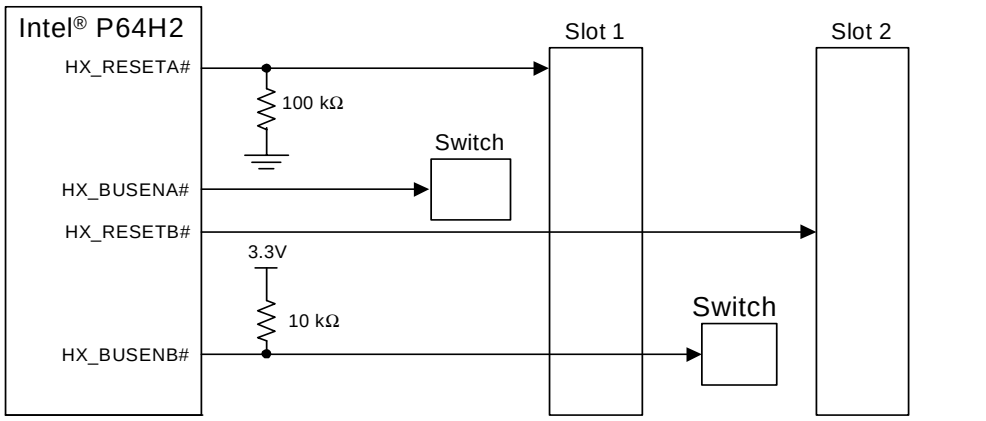
NOTES:
1. HPx_SLOT [N] are pull-ups/pull-downs. When in dual-slot parallel mode, the external logic that decodes the three-state value of PCIXCAP from the card must actively drive these signals to either logic 1 or logic 0 to overcome the value of the pull-up/pull-down, and must be tri-stated during reset and while the card is not connected to avoid damaging the slot count value.
2. HPx_SID must be pulled down on the system board when configuring the Intel® P64H2 for dual-slot parallel mode so that the LED for slot B on busses A and B remain off during reset.
3. The Intel P64H2 must drive this signal to the corresponding state shown in Table 77 in case the system is set up for dual-slot parallel mode so that LEDs are in the appropriate state (off), and the Q-switches remain disconnected. Note that the placement of the signals should be such that the value driven by the Intel P64H2 in dual slot parallel mode is the same value it would have driven when in serial mode.
4. In both parallel modes, the BUSEN# and CLKEN# signals become active low instead of active high, as they are during serial mode.

8.2.8.8 SMBus Address Considerations

In dual-slot parallel mode, the SMBus address strap pins in Table 73 are multiplexed as Hot-Plug control signals HxRESETA# and HxBUSENB#. Therefore, it is recommended that the following technique be used for determining an SMBus address. Pull the PAGNT5 (RESETA#) signals to ground through a 100 kΩ ± 5% resistor. This keeps the reset signal active until the Intel® P64H2 is ready for it to become deasserted. Pull the PAGNT4 (BUSENB#) signals to 3.3 V through a 10 kΩ ± 5% resistor. The Intel P64H2 may be able to drive this signal to ground when the signal must be asserted.

Keep in mind that this limits the range of addresses you may achieve. Using this technique, the address is fixed when operating in dual-slot parallel mode on both controllers. Figure 100 shows a dual-slot parallel SMBus circuit.

Figure 100. Dual-Slot Parallel SMBus Circuit

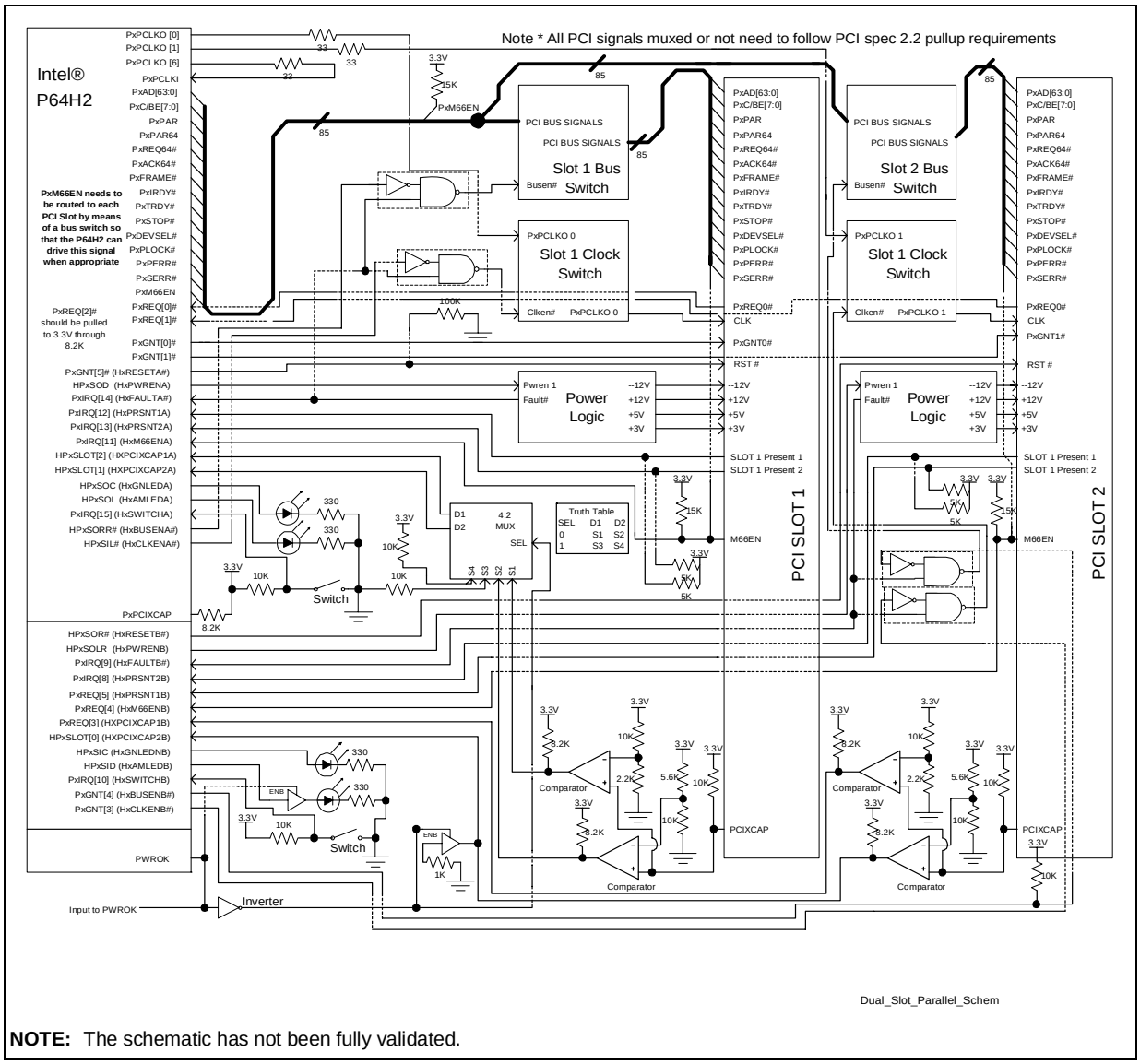


NOTE: The pin names shown in the Intel® P64H2 block are slot pin names. For dual-slot parallel mode, refer to Table 78 for the corresponding Intel P64H2 pin name.

8.2.8.9 Reference Schematic for Dual-Slot Parallel Mode

Note that the schematic in Figure 101 is based on definition and simulation of the Intel P64H2.

Figure 101. Reference Schematic for Dual-Slot Parallel Mode



NOTE: The schematic has not been fully validated.

8.2.9 Three or More Slot Serial Mode

Serial mode allows for three to six slots to be Hot-Pluggable. This mode may also be used to enable slots that are Hot-Pluggable, and others that are not on the same PCI/PCI-X bus.

8.2.9.1 Hot-Plug and Non-Hot-Plug Combinations

To accomplish Hot-Plug and non-Hot-Plug combinations, put the non-Hot-Pluggable devices on their own Hot-Plug serialization logic (for M66EN and PCIXCAP), and scan them in for software to view. Do not electrically isolate those devices—allow software to see their capabilities to choose bus frequency properly.

8.2.9.2 Required Additional Logic

Serial mode requires a power switch to be used to turn the slot power on and off on all Hot-Pluggable slots. Serial mode also requires the use of a bus and clock switch. In addition, serial mode requires auto bus and clock disable logic to immediately disable the PCI bus and clock when the power fault signal (from the power switch) goes active.

When the platform supports PME# or SMBus connections to the slots, isolation logic is required to disconnect these signals before inserting or removing a card. See the *PCI Hot-Plug Specification,* Revision 1.1, for implementation details.

8.2.9.3 Debounced Hot-Plug Switch Input

The switch inputs to the serialization/deserialization logic may require debouncing logic. This depends on the logic used for serialization, and is left up to the individual designer.

8.2.9.4 Comparator Circuit for PCIXCAP1/PCIXCAP2 Pins

A comparator circuit is required for properly decoding the PCI/PCI-X capability of the slot. Refer to the *PCI Local Bus Specification,* Revision 2.2, for this circuit. An example of this circuit is also contained in the reference schematics.

8.2.9.5 HPx_SLOT[2:0]

The HPx_SLOT[2:0] pins are pull-ups/pull-downs that are used to determine the slot count and mode of operation for the Intel® P64H2 Hot-Plug controller. These pins should be strapped to the proper slot count value. See Table 74.

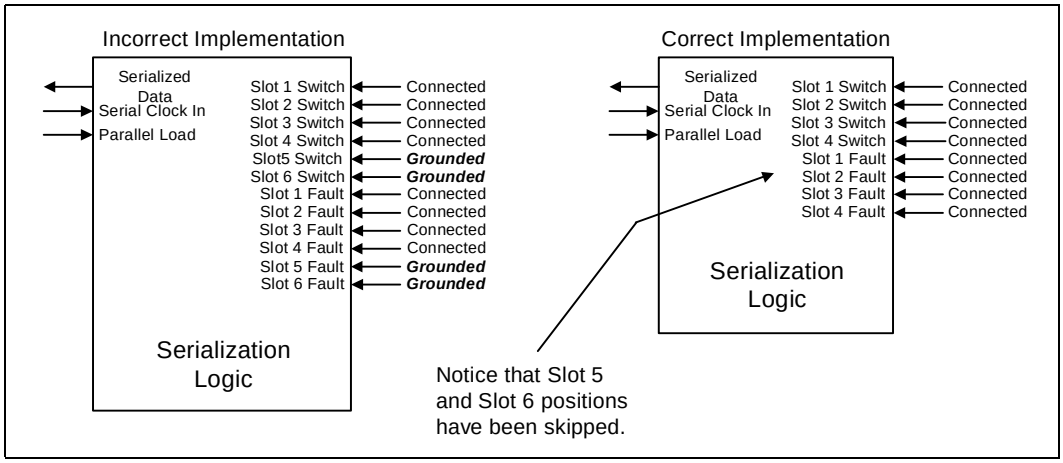
8.2.9.6 Stutter Logic for Implementing Fewer Than Six Slots

The serialized input/output data stream effectively stutters around the unused bit positions corresponding with the number of Hot-Plug slots determined by HPx_SLOT[2:0]. This reduces the amount of logic required to implement fewer than six slots. When HPx_SLOT[2:0] is strapped to enable four Hot-Pluggable slots, bit positions 4 and 5 would be skipped. Refer to Figure 102 for an example of this. Note that this concept also applies to the output data stream as well.

Table 79. Shift Register Input Data

Bit	Byte 0	Byte 1	Byte 2	Byte 3
0	Slot 1 switch (0 = closed)	Slot 1 fault# (0 = fault)	Slot 1 present bit 2	Slot 1 present bit 1
1	Slot 2 switch	Slot 2 fault#	Slot 2 present bit 2	Slot 2 present bit 1
2	Slot 3 switch	Slot 3 fault#	Slot 3 present bit 2	Slot 3 present bit 1
3	Slot 4 switch	Slot 4 fault#	Slot 4 present bit 2	Slot 4 present bit 1
4	Slot 5 switch	Slot 5 fault#	Slot 5 present bit 2	Slot 5 present bit 1
5	Slot 6 switch	Slot 6 fault#	Slot 6 present bit 2	Slot 6 present bit 1
6	Stutter (not used)	Stutter (not used)	Stutter (not used)	Stutter (not used)
7	Stutter (not used)	Stutter (not used)	Stutter (not used)	Stutter (not used)
Bit	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**
0	Slot 1 M66EN	Slot 1 PCIXCAP1	Slot 1 PCIXCAP2	User Defined
1	Slot 2 M66EN	Slot 2 PCIXCAP1	Slot 2 PCIXCAP2	User Defined
2	Slot 3 M66EN	Slot 3 PCIXCAP1	Slot 3 PCIXCAP2	User Defined
3	Slot 4 M66EN	Slot 4 PCIXCAP1	Slot 4 PCIXCAP2	User Defined
4	Slot 5 M66EN	Slot 5 PCIXCAP1	Slot 5 PCIXCAP2	User Defined
5	Slot 6 M66EN	Slot 6 PCIXCAP1	Slot 6 PCIXCAP2	User Defined
6	Stutter (not used)	Stutter (not used)	Stutter (not used)	Stutter (not used)
7	Stutter (not used)	Stutter (not used)	Stutter (not used)	Stutter (not used)

Figure 102. Four-Slot Stutter Logic Implementation Example



8.2.9.7 Pull-Ups/Pull-Downs in Three or More Slot Serial Mode

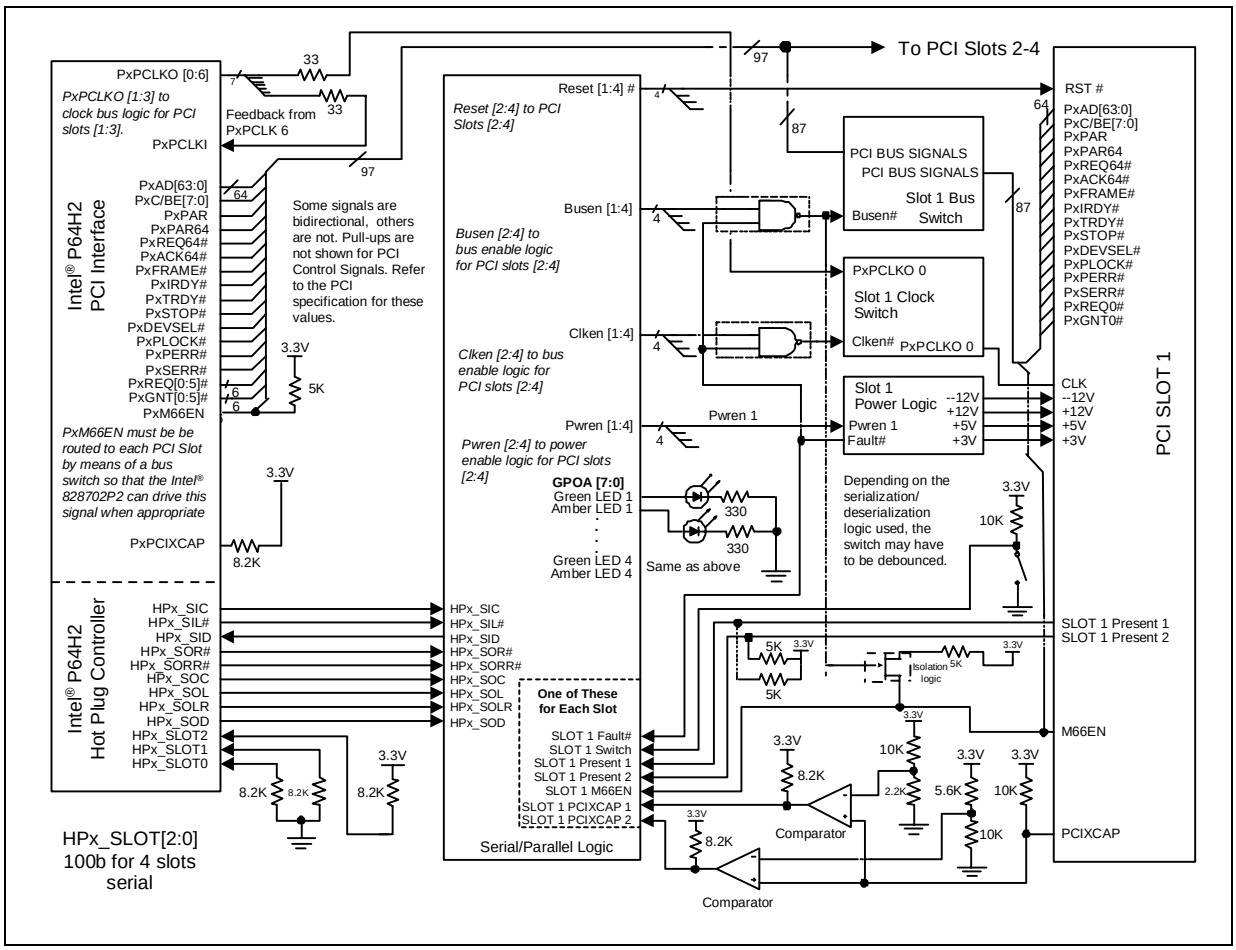
All PCI signals should follow the *PCI Local Bus Specification*, Revision 2.2, pull-up requirements whether they are multiplexed or not. Any unused input signals should be pulled to 3.3 V through an 8.2 kΩ ± 5% resistor to keep them from floating.

8.2.9.8 Reference Schematic for Serial Mode

The schematic in Figure 103 is based on definition and simulation of the Intel® P64H2.

Note: This schematic has not been fully validated.

Figure 103. Reference Schematic for Serial Mode



8.2.10 Intel® P64H2 PCI Interface PCIXCAP and M66EN Pins

8.2.10.1 PCIXCAP Pin Requirements

During all modes of the Intel P64H2 Hot-Plug controller operation, the Intel P64H2 PCI/PCI-X interface pin PxPCIXCAP is not used. This pin should be tied to VCC3_3 through an 8.2 kΩ resistor to avoid having this line float.

The slot-specific HxPCIXCAP1 and HxPCIXCAP2 pins should be connected to their associated slot. See Section 8.2.7, Section 8.2.8, and Section 8.2.9 for more information on properly decoding PCI/PCI-X capability.

8.2.10.2 M66EN Pin Requirements

When operating in single-slot parallel mode, the Intel® P64H2 never drives PxM66EN. This pin should be tied to either VCC3_3 or ground through an 8.2 kΩ ± 5% resistor to avoid having this line float. M66EN on the slot must be connected to the associated HxM66EN pin with a pull-up/ pull-down on the motherboard. When the slot is to be a 33 MHz slot, then M66EN must be pulled to ground on the motherboard. This may make the slot a 33 MHz PCI slot always. When the M66EN pin is pulled high, then the slot cannot be run at 33 MHz PCI. This means that after a card is powered up at 33 MHz (Hot-Plug default), software must reset the bus to at least 66 MHz PCI mode (or a PCI-X mode) before any software attempts accesses to the PCI card. Otherwise, the card could experience operational problems if it requires M66EN for setting up PLLs, etc.

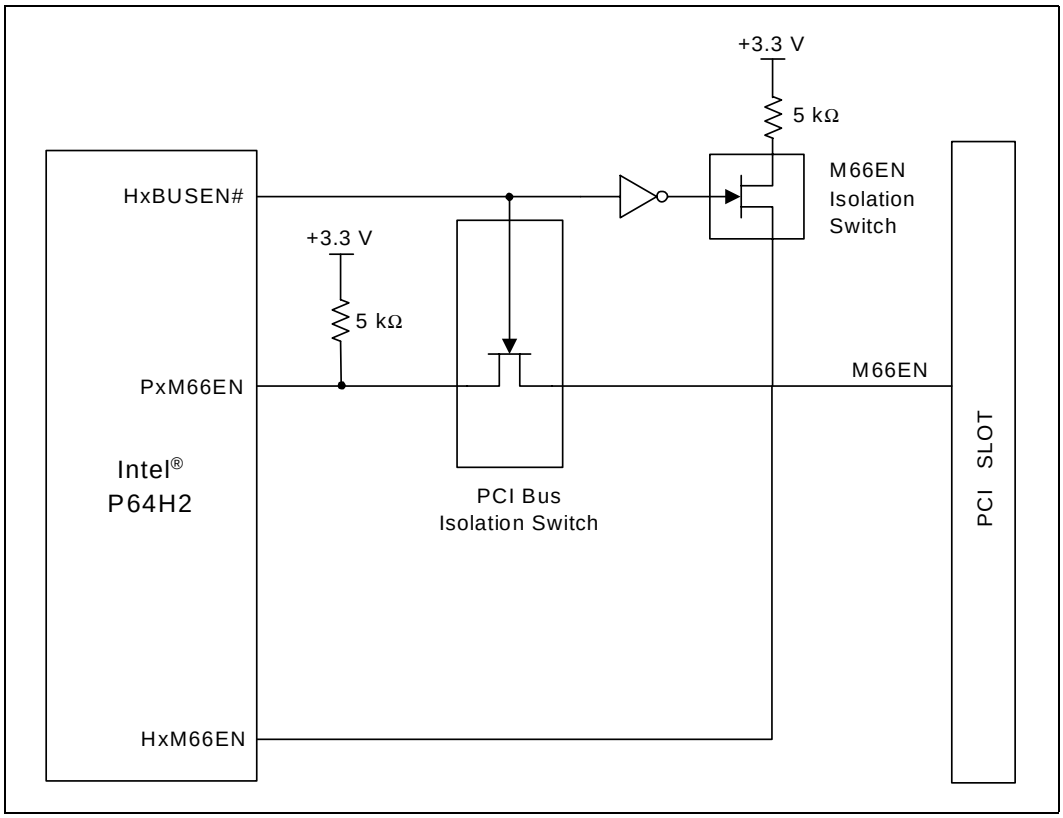
In dual slot parallel and serial modes, the PxM66EN pin (on the Intel P64H2 PCI/PCI-X interface) is a switched PCI bus signal that must be tied to all the slots through isolation logic. All cards must be able to see the value of PxM66EN being driven by the Intel P64H2 when coming out of reset. The HxM66EN pins (on the Intel P64H2 Hot-Plug Interface) should be connected to their associated slots.

The PxM66EN and HxM66EN pins each require 5 kΩ ± 5% pull-up resistors as specified in *PCI Local Bus Specification,* Revision 2.2. When the slot is connected to the bus, the Intel P64H2 may be sinking through both resistors, which is a violation of the specification. The following sections describe two possible M66EN design solutions.

8.2.10.2.1 M66EN Isolation Switch Solution

One possible solution to the issue described in the previous paragraphs is to place a single 5 kΩ ± 5% pull-up on the Intel P64H2 side of the isolation logic and a 5 kΩ ± 5% pull-up on the slot side after the isolation logic, but with its own isolation switch, which uses an inverted version of the bus enable control signal. This way, when the isolation logic has the bus disconnected, the slot side may be pulled up with a 5 kΩ ± 5% resistor. When the isolation logic has the bus connected, the slot side resistor may be isolated, and the M66EN line may be pulled up by the 5 kΩ ± 5% pull-up on the Intel P64H2 side of the isolation logic. Using this method, the Intel P64H2 would only be sinking through a single 5 kΩ resistor at any time and would always be meeting the *PCI Local Bus Specification,* Revision 2.2, on the M66EN pull-up (*PCI Local Bus Specification,* Revision 2.2, Section 7.7.7). See Figure 104.

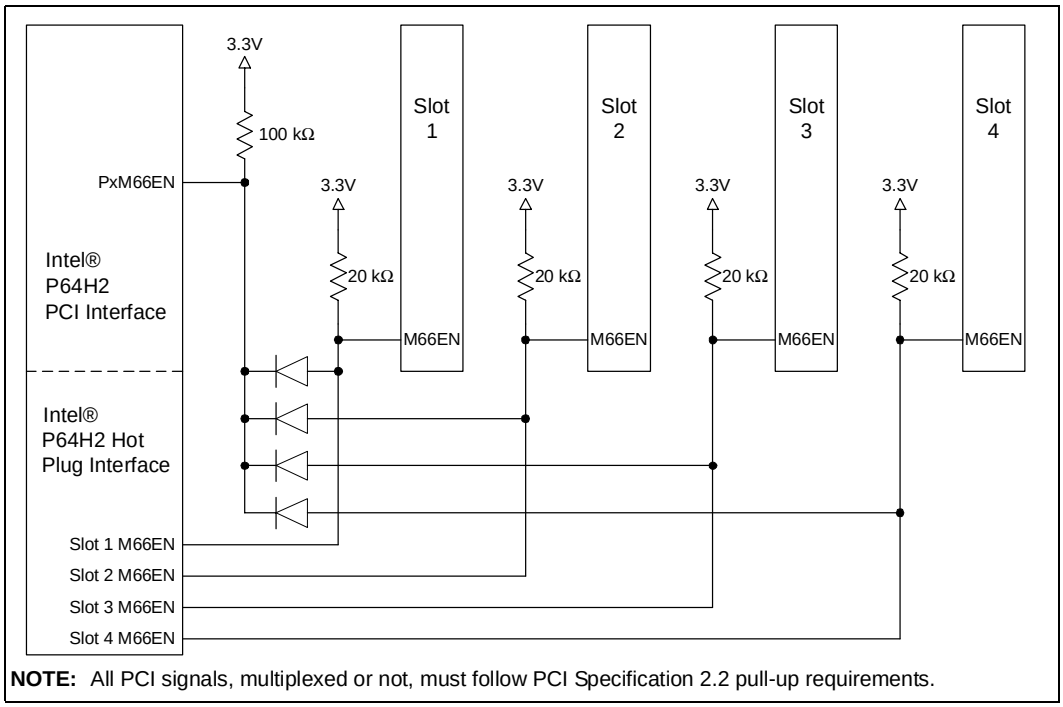
Figure 104. M66EN Isolation Switch Solution



8.2.10.2.2 M66EN Diode Solution

Another possible to the issue described in the previous paragraphs solution is to use diodes to isolate the individual slots from one another while still allowing the Intel® P64H2 to drive the M66EN signals to ground. The Intel P64H2 PCI interface PxM66EN signal should be pulled to 3.3 V through a 100kΩ ± 5% resistor. This signal would then be connected to the individual slots through a reverse biased diode (one diode per slot). The PCI slots should also be pulled up individually to 3.3 V through a resistor of value such that the equivalent of all the resistances on the M66EN bus is approximately 5 kΩ (the PCI recommended value). This circuit allows the Intel P64H2 to pull the slots' M66EN to ground during initial power-up. During normal operation, each of the slots' M66EN signals may be isolated from one another allowing for polling of the Hot-Plug HxM66EN input for slot capability. Figure 105 shows the diode solution implemented in serial mode, where 'Slot x M66EN' is a serialized input to the Hot-Plug controller.

Figure 105. M66EN Diode Solution



NOTE: All PCI signals, multiplexed or not, must follow PCI Specification 2.2 pull-up requirements.

I/O Controller Hub 3 (Intel® ICH3-S) 9

9.1 IDE Interface

This section contains guidelines for connecting and routing the Intel® ICH3-S IDE interface. The ICH3-S has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH3-S has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors may be required, OEMs should verify motherboard signal integrity through simulation. Additional external zero ohm resistors may be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface may be routed with 5-mil traces on 7-mil spaces, and must be less than eight inches long (from ICH3-S to IDE connector). Additionally, maximum length difference between the longest and shortest trace lengths of a channel is 0.5 inch.

9.1.1 Cabling

- **Length of cable:** Each IDE cable must be equal to or less than 18 inches.
- **Capacitance:** The capacitance of each IDE cable must be less than 35 pF.
- **Placement:** A maximum of six inches is allowed between drive connectors on the cable. When a single drive is placed on the cable, it should be placed at the end of the cable. When a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (no more than six inches away from the end of the cable).
- **Grounding:** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- **ICH3-S Placement:** The ICH3-S must be placed equal to or less than eight inches from the ATA connector(s).

9.1.2 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH3-S IDE controller supports PIO, Multi-word (8237 style) DMA and Ultra DMA modes zero through five. The ICH3-S must determine the type of cable that is present to configure itself for the fastest possible transfer mode the hardware may support.

An 80-conductor IDE cable is required for Ultra DMA modes greater than two (Ultra ATA/33). This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, and so on. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the *Small Form Factor Specification SFF-8049*. This specification may be obtained from the Small Form Factor Committee.

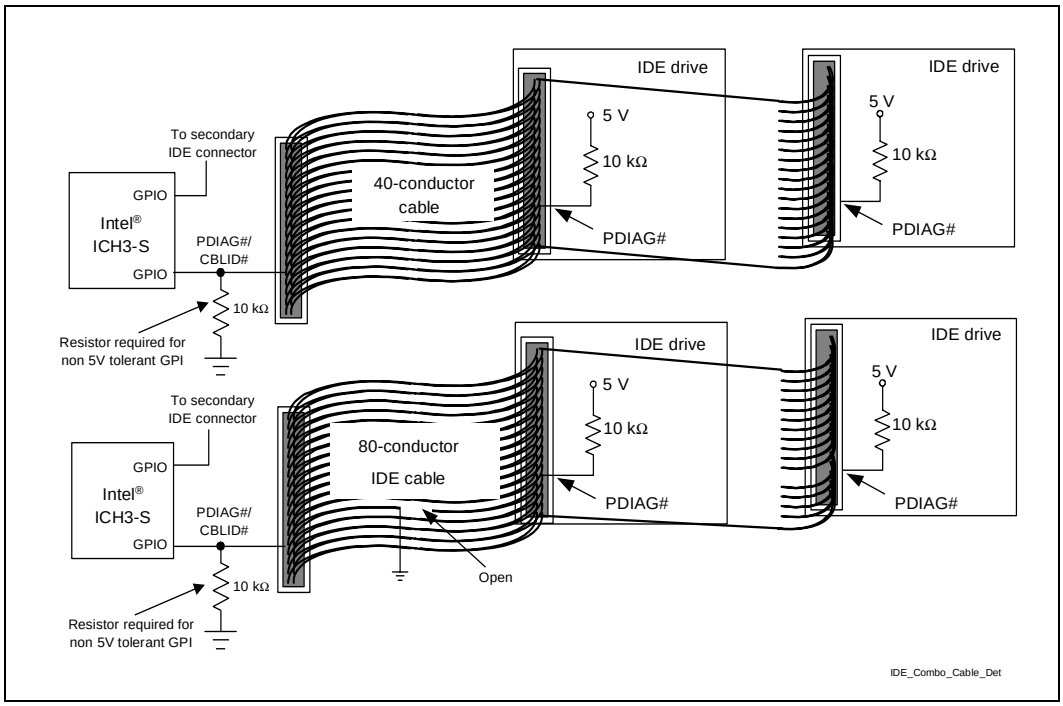
To determine when Ultra DMA modes greater than two (Ultra ATA/33) may be enabled, the ICH3-S requires the system software to attempt to determine the cable type used in the system. When the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. When a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be performed using a combination Host-Side/Device-Side detection mechanism.

9.1.2.1 Combination Host-Side/Device-Side Cable Detection

Host-side detection (described in the *ATA/ATAPI-4 Standard*, Section 5.2.11) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 106. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. Not all of the GPI and GPIO pins on the ICH3-S are 5 V tolerant. A 10 kΩ ± 5% pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating when a device is not present. The pull-down resistor also allows for the use of a non-5 V tolerant GPIO.

Figure 106. Combination Host-Side/Device-Side IDE Cable Detection



This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. When the signal is high, then a 40-conductor cable is present in the system and Ultra DMA modes greater than Mode 2 (Ultra ATA/33) must not be enabled.

When PDIAG#/CBLID# is detected low, an 80-conductor cable may be in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-4 standard. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher

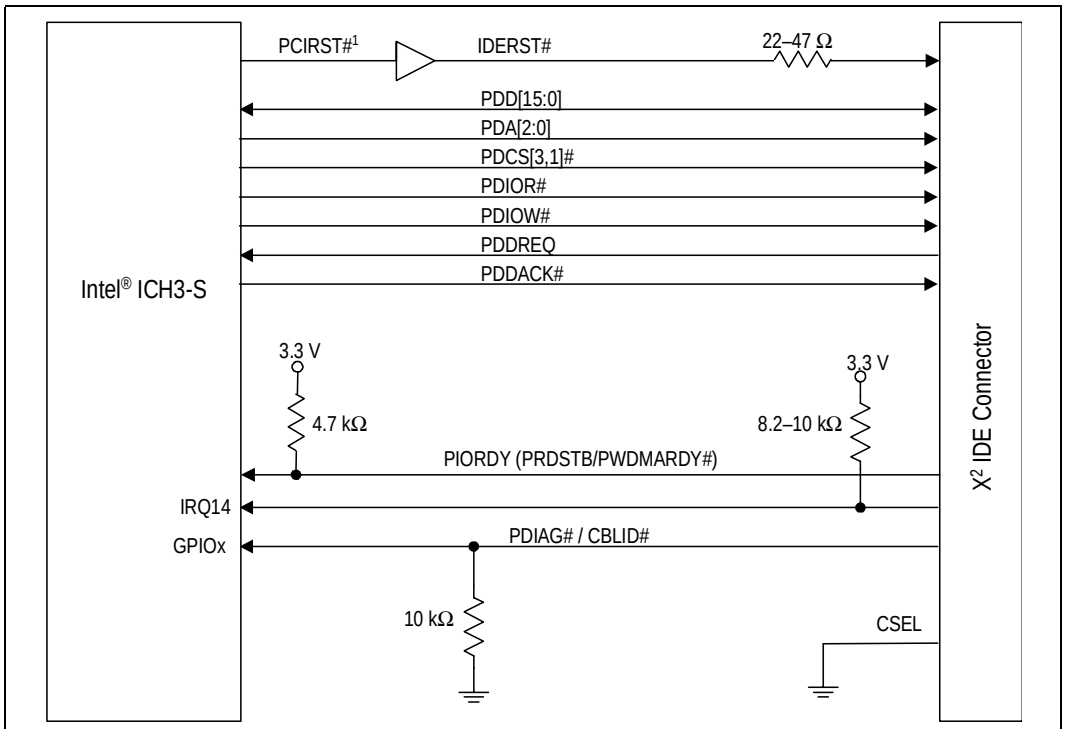
than 2. When ID Word 93, bit 13 is 1, an 80-conductor cable is present. When this bit is 0, a legacy slave (Device 1) is preventing proper cable detection and BIOS should configure the system as though a 40-conductor cable is present and notify the user of the problem.

9.1.3 IDE Connector Requirements

The requirements for the primary and secondary IDE connector are shown in Figure 107.

- A 22 Ω to 47 Ω series resistor is required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3.3.
- A 4.7 kΩ ± 5% pull-up resistor to VCC3.3 is required on PIORDY.
- Series resistors may be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10 kΩ ± 5% resistor to ground on the PDIAG#/CBLID# signal is required on the primary connector. This change is to prevent the GPIOx pin from floating when a device is not present on the IDE interface.

Figure 107. Connection Requirements for IDE Connector

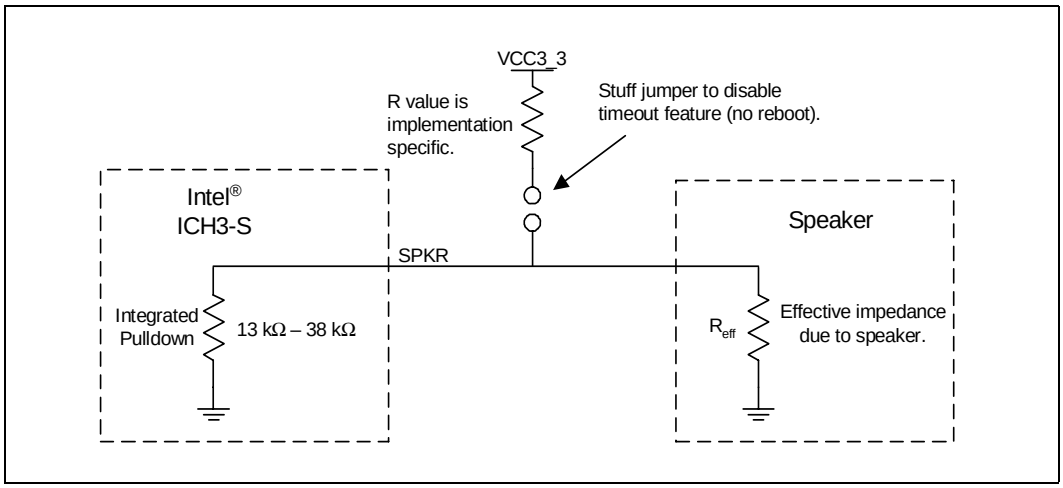


NOTE:
1. Because of ringing, PCIRST# must be buffered.
2. 'X' indicates Primary or Secondary

9.2 SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the 'TCO Timer Reboot function' based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH3-S sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable TCO timer reboot, a jumper may be populated to pull the signal line high (see Figure 108). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (REFF), and the ICH3-S's integrated pull-down resistor may be read as logic high.

Figure 108. Example Speaker Circuit

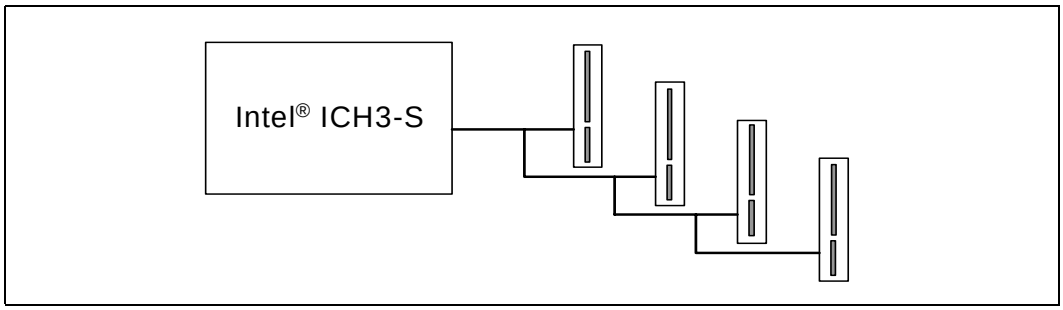


9.3 PCI

The ICH3-S provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification*, Revision 2.2. The implementation is optimized for high-performance data streaming when the ICH3-S is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification*, Revision 2.2.

The ICH3-S supports six PCI Bus masters (excluding the ICH3-S), by providing six REQ# / GNT# pairs. In addition, the ICH3-S supports two PC/PCI REQ# / GNT# pairs, one of which is multiplexed with a PCI REQ# / GNT# pair. Figure 109 shows the PCI bus layout example.

Figure 109. PCI Bus Layout Example



9.4 USB

The ICH3-S contains three UHCI host controllers. Each UHCI controller includes a root hub with two separate USB ports, for a total of six USB ports. This section provides guidelines for routing USB.

9.4.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines help minimize signal quality and EMI problems. USB validation efforts have focused on a ground referenced design.

1. Place the ICH3-S and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
2. USB signals should be ground referenced (on layers 3 and 8).
3. Route USB signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. When it becomes necessary to turn 90 degrees, use two 45-degree turns or an arc instead of a single 90 degree turn. This reduces reflections on the signal by minimizing impedance discontinuities.
5. Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
6. Stubs on USB signals should be avoided because stubs have an effect on signal quality. When stubs are necessary, none should be greater than 200 mils.
7. Route all traces over continuous ground planes with no interruptions. Avoid crossing over anti-etch when possible; this increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces.
8. Keep USB signals clear of the core logic set. High current transients are produced during internal state transitions, and may be very difficult to filter out.
9. Keep traces at least 50 mils away from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires, and helps prevent free radiation of the signal from the edge of the PCB.

9.4.2 USB Routing Parameters

Use the following separation guidelines.

- Recommended trace width and separation is 5-mils trace width with 6-mils spacing (90 Ω differential impedance).
- Maintain parallelism between USB differential signals, with the trace spacing needed to achieve 90 Ω differential impedance.
- Use at a minimum of 20 mils spacing between USB signal pair and other traces on the PCB. This helps to prevent crosstalk. When possible, keep clock and PCI traces at least 50 mils from the USB differential pairs.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk.
- Trace length match USB signal pair traces. The maximum trace length mismatch between USB signal pair should be no greater than 150 mils.

9.4.3 EMI Considerations

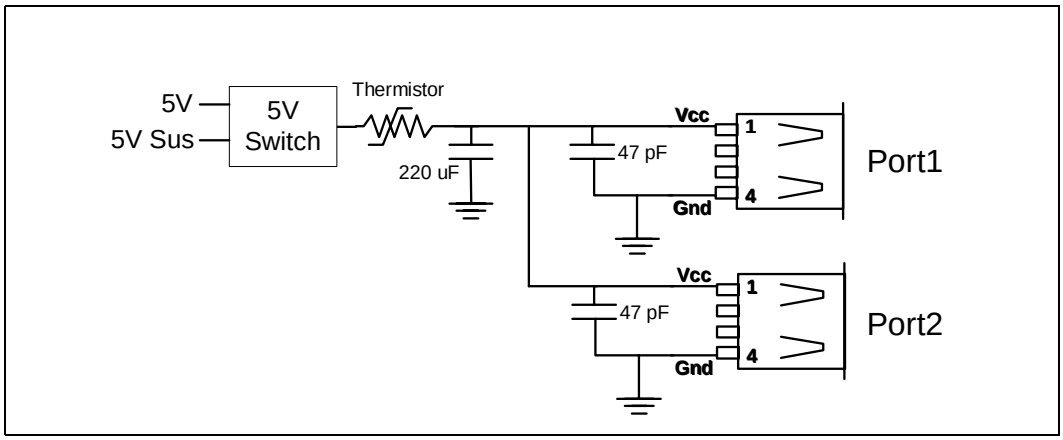
An optional 47 pF capacitor may be placed as close to the USB connector as possible on the USB data lines. This capacitor may be used for improved signal quality (rise/fall time), and to help minimize EMI radiation.

Note: Any EMI or ESD solution should be placed as close to the port as possible. For example, when using a front-panel daughter card, the EMI/ESD solution should be placed on the daughter card.

9.4.4 USB Power Line Layout Topologies

The following is a suggested topology for power distribution of VBUS to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop), and dynamic detach flyback protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach flyback voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port, and the power-carrying traces should be as wide as possible, preferably a plane. Figure 110 shows the suggested USB downstream power connection.

Figure 110. Suggested USB Downstream Power Connection



9.5 Intel® ICH3-S SMBus/SMLink Interface

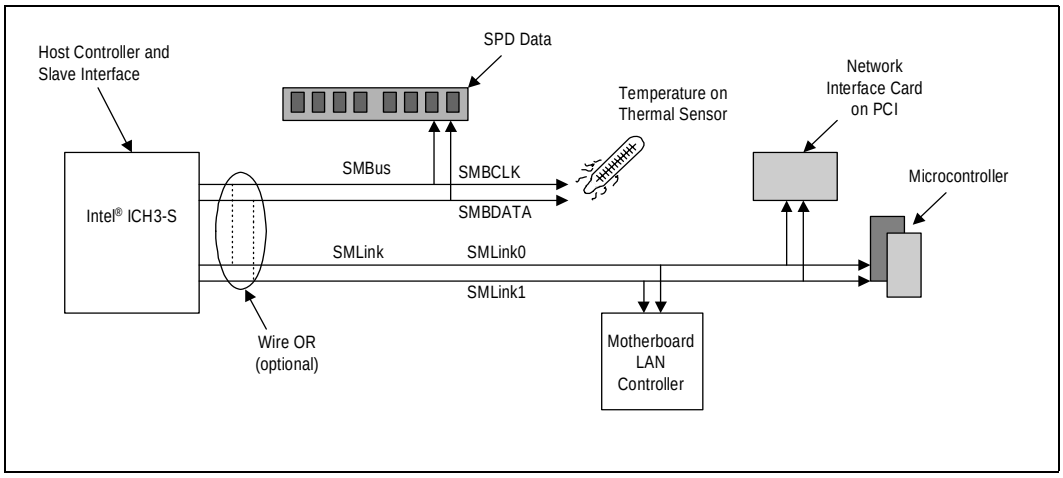
The SMBus interface on the ICH3-S uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus host controller. The SMBus host controller resides inside the ICH3-S. When the SMBus is used only for the SPD EEPROMs (one on each DIMM), both signals should be pulled up with a 4.7 kΩ ± 5% resistor to VCC3.3.

The ICH3-S incorporates an SMLink interface supporting Alert on LAN*, Alert on LAN2*, and a slave functionality. This interface uses two signals, SMLINK[1:0]. SMLINK0 corresponds to an SMBus clock signal, and SMLINK1 corresponds to an SMBus data signal. These signals are part of the SMBus Slave Interface.

For Alert on LAN* functionality, the ICH3-S transmits heartbeat and event messages over the interface. When using the 82562EM Platform LAN Connect Component, the ICH3-S's integrated LAN controller may claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert on LAN2-enabled LAN controller (i.e., Intel® 82550) may connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH3-S SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface may reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface may read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus host controller and the SMBus Slave Interface obey the SMBus 1.1 protocol, so the two interfaces may be externally wire-OR'd together to allow an external management ASIC (e.g., Intel 82550) to access targets on the SMBus as well as the ICH3-S Slave interface. Additionally, the ICH3-S supports slave functionality, including the host Notify protocol, on the SMLink pins. This is done by connecting SMLink0 to SMBCLK and SMLink1 to SMBDATA. Figure 111 shows the Intel ICH3-S SMBus/SMLink interface.

Figure 111. Intel® ICH3-S SMBus / SMLink Interface



Note: Intel does not support external access of the ICH3-S's Integrated LAN controller via the SMLink interface. In addition, Intel does not support access of the ICH3-S's SMBus Slave Interface by the ICH3-S's SMBus host controller. Refer to the *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

9.5.1 SMBus Design Considerations

There is not a single SMBus design solution that may work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing the SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Regardless of the architecture used, there are some general design considerations.

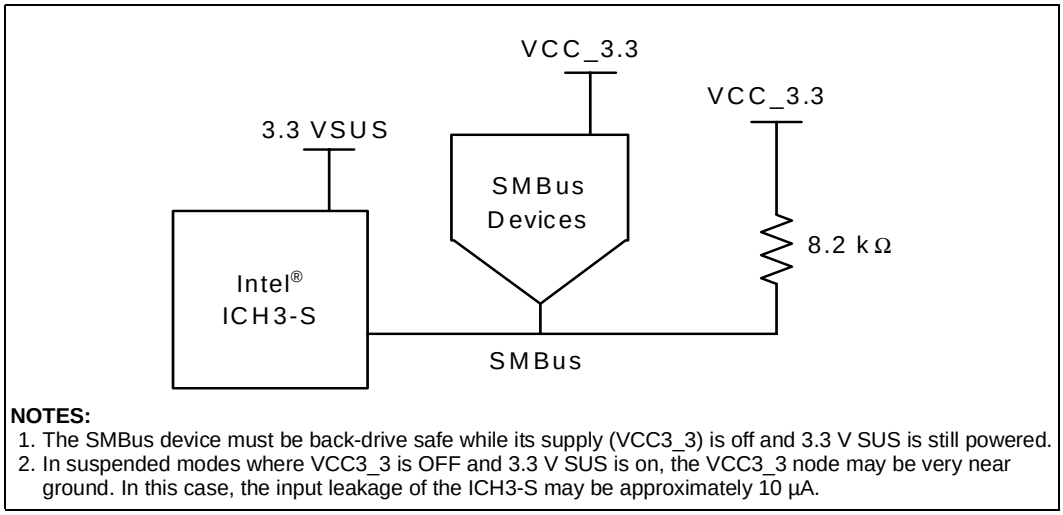
- Device class (High/Low power). Most designs use primarily High Power Devices.
- Amount of VCC_SUSPEND current available (i.e., minimizing load of VCC_SUSPEND).
- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that may sink the least amount of current is the limiting agent on how small the resistor may be. The pull-up resistor may not be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and time specification.
- The maximum bus capacitance that a physical segment may reach is 400 pF.
- The ICH3-S does not run SMBus cycles while in S5.
- SMBus devices that may operate in S5 must be powered by the VCC_SUSPEND supply.
- When the SMBus is connected to PCI, it must be connected to all PCI slots.
- It is recommended that I^2C devices be powered by the 1.8 V supply. During an SMBus transaction in which the device is sending information to the ICH3-S, the device may not release the SMBus when the ICH3-S receives an asynchronous reset. The BIOS uses 1.8 V to reset the devices. SMBus 2.0-compliant devices have a timeout capability which makes them insusceptible to this I^2C issue, allowing flexibility in choosing a voltage supply.

9.5.2 Unified VCC_CORE Architecture

Designing an SMBus using the ICH3-S is based on the power supply source for the SMBus microcontrollers. For the platform, all devices are powered by VCC3_3; therefore, the preferred design choice is the unified VCC3_3 architecture.

In the unified VCC_CORE architecture, all SMBus devices are powered by the VCC3_3 supply. This architecture shown in Figure 112 allows none of the devices to operate in S5, minimizing the load on 3.3 V SUSPEND.

Figure 112. Unified VCC3_3 Architecture

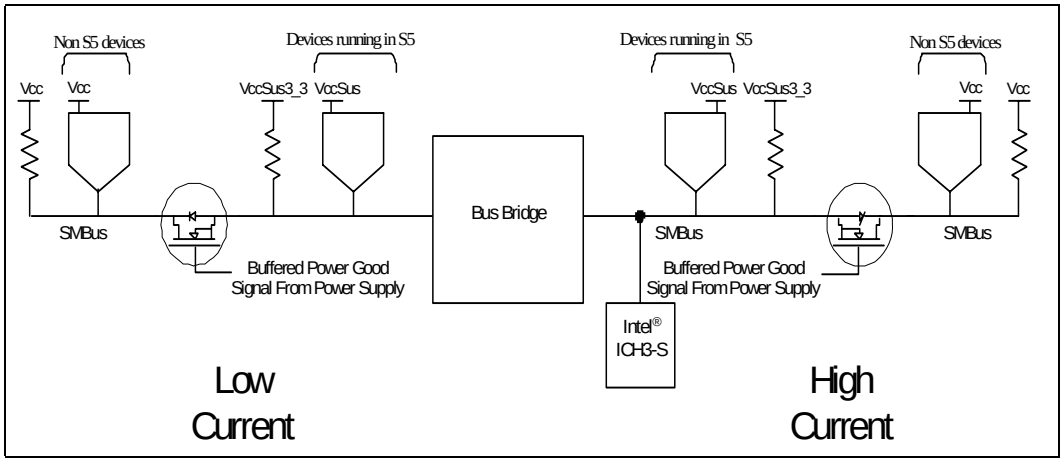


NOTES:
1. The SMBus device must be back-drive safe while its supply (VCC3_3) is off and 3.3 V SUS is still powered.
2. In suspended modes where VCC3_3 is OFF and 3.3 V SUS is on, the VCC3_3 node may be very near ground. In this case, the input leakage of the ICH3-S may be approximately 10 µA.

9.5.3 High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices while also allowing SMBus devices to communicate while in S5. VCC_SUSPEND leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of a Field-Effect Transistor (FET) to isolate the devices powered by the core and suspend supplies (see Figure 113).

Figure 113. High Power/Low Power Mixed VCC_SUSPEND/ VCC_CORE Architecture



Added Considerations for Mixed Architecture:

- The bus switch must be powered by VCC_SUSPEND.
- Devices that are powered by the VCC_SUSPEND well must not drive into other devices that are powered off. This is accomplished with the bus switch.
- The bus bridge may be a device like the Phillips PCA9515.

9.5.4 Calculating The Physical Segment Pull-Up Resistor

Table 80 and Table 81 present references for calculating the value of the pull-up resistor that may be used for a physical bus segment. When any physical bus segment exceeds 400 pF, then a bus bridge device such as the Phillips* PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 80. Bus Capacitance Reference Chart

Device	No. of Devices/ Trace Length	Capacitance Includes	Cap (pF)
Intel® ICH3-S	1	Pin Capacitance	12
CK408	1	Pin Capacitance	10
DIMMS	2	Pin Capacitance (10 pF) + 1 inch of trace capacitance (2 pF/inch) per DIMM and 2 pF connector capacitance per DIMM	28
	3		42
PCI Slots	2	Each PCI add-in card is allowed up to 40 pF + 3 pF per each connector	86
	3		129
	4		172
	5		215
	6		258
SMBus Trace Length in inches	≥ 24”	2 pF per inch of trace length	48
	≥ 36”		72
	≥ 48”		96

Table 81. Bus Capacitance/Pull-Up Resistor Relationship

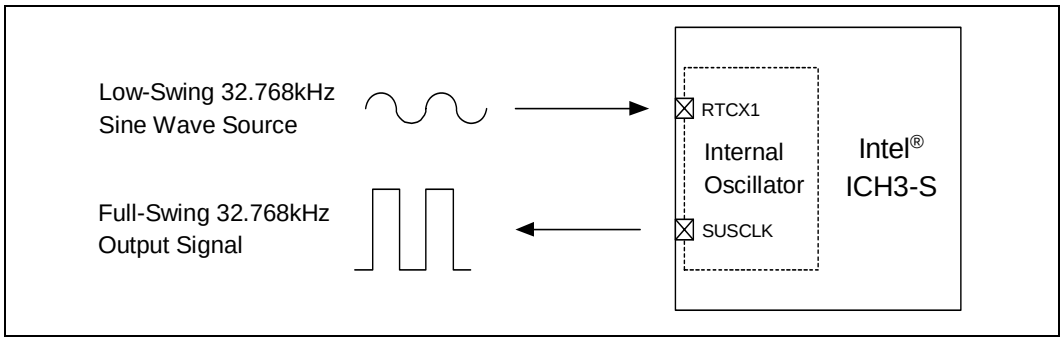
Physical Bus Segment Capacitance	Pull-Up Range (For Vcc = 3.3 V
0 to 100 pF	8.2 kΩ to 1.2 kΩ
100 to 200 pF	4.7 kΩ to 1.2 kΩ
200 to 300 pF	3.3 kΩ to 1.2 kΩ
300 to 400 pF	2.2 kΩ to 1.2 kΩ

9.6 Real Time Clock (RTC)

The ICH3-S contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time, and storing system data in its RAM when the system is powered down.

The ICH3-S uses a crystal circuit that generates a low-swing 32 kHz input sine wave. The RTCX1 input is amplified and driven back to the crystal circuit through the RTCX2 signal. Internal to the ICH3-S, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use illustrated in Figure 114. This ICH-S output pin is called SUSCLK.

Figure 114. RTCX1 and SUSCLK Relationship

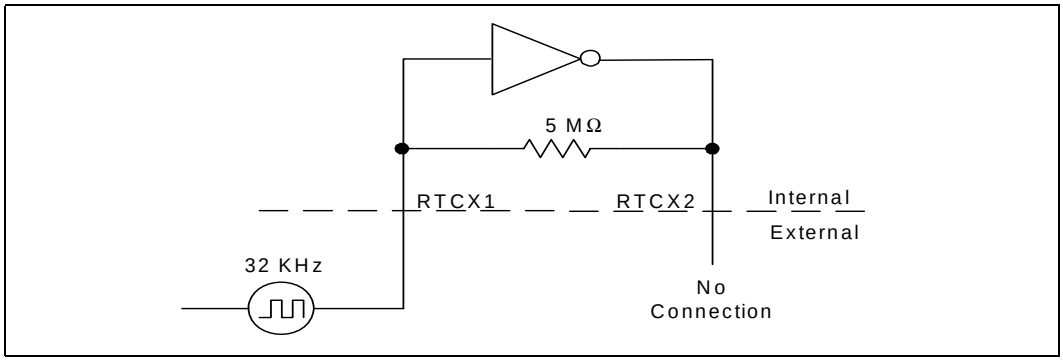


For further information on the RTC, consult Intel application note *AP-728 Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*, available at: http://developer.intel.com/design/chipsets/applnots/292276.htm.

This section presents the recommended hookup for the RTC circuit for the ICH3-S.

Even if the ICH3-S internal RTC is not used, it is still necessary to supply clock inputs to RTCX1 and RTCX2 pins of the ICH3-S because other signals are gated with that clock in suspend modes. However, in this case the frequency (32.768 kHz) of the clock inputs is not critical. A lower-cost crystal may be used, or a single clock input may be driven into the RTCX1 pin with the RTCX2 pin left as no connect, as shown in Figure 115. This is not a validated configuration with ICH3-S.

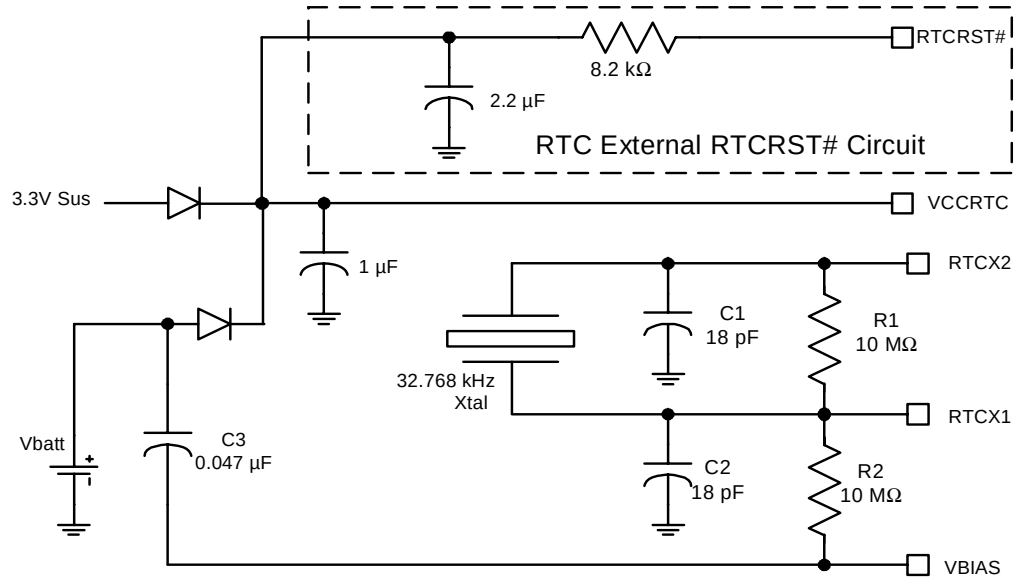
Figure 115. RTC Connection When Not Using Internal RTC



9.6.1 RTC External Circuit

The ICH3-S RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 116 shows the external circuitry that comprises the oscillator of the ICH3-S RTC.

Figure 116. Example of RTC External Circuitry



NOTES:
1. The exact capacitor values must be based on the crystal maker recommendation. (Typical values for C1 and C2 are 18 pF for a crystal load of 12 pF.)
2. VCCRTC: Power for RTC Well
3. RTCX2: Feedback for the external crystal
4. RTCX1: Input to the internal oscillator
5. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.

9.6.2 RTC External RTCRST# Circuit

The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10 ms – 20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1 and remains set until software clears it. Because of this, when the system boots, the BIOS knows that the RTC battery has been removed. Figure 116 shows an example of RTCRST# circuitry that is used in conjunction with the external diode circuit.

9.6.3 External Capacitors

To maintain the RTC accuracy, the external capacitor C3 must be 0.047 µF, and capacitor values C1 and C2 should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (when used), and package. The following equation may be used to choose the external capacitance values:

Cload = [(C1 + Cin1 + Ctrace1)*(C2 + Cin2 + Ctrace2)]/[(C1 + Cin1 + Ctrace1 + C2 + Cin2 + Ctrace2)] + Cparasitic

Where:

Cload = Crystal's load capacitance. This value may be obtained from crystal's specification.

Cin1, Cin2 = input capacitances at RTCX1, RTCX2 balls of the ICH3-S. These values may be obtained in the *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet.*

Ctrace1, Ctrace2 = Trace length capacitances measured from crystal terminals to the RTCX1 and RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces, and the length of the traces. Typical value is approximately:

Ctrace = trace length * 2 pF / inch (dependent upon board characteristics)

Cparasitic = Crystal's parasitic capacitance. This capacitance is created by the existence of two electrode plates, and the dielectric constant of the crystal blank inside the crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C1 and C2 may be selected such that C1 = C2. Using the equation of Cload above, the value of C1 and C2 may be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C2 may be chosen such that C2 > C1. Then C1 may be trimmed to obtain 32.768 kHz.

In certain conditions, both C1 and C2 values may be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C1 and C2 values are smaller then the theoretical values, the RTC oscillation frequency may be higher.

The following example illustrates the use of the practical values C1 and C2 in the case that theoretical values cannot ensure the accuracy of the RTC in a low temperature condition.

9.6.3.1 Example with Load Capacitance

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH3-S, the calculated values of C1 = C2 are 10 pF at room temperature (25° C) to yield a 32.768 kHz oscillation.

At 0° C, the frequency stability of the crystal gives -23 ppm (assumed that the circuit has zero ppm at 25° C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

When the values of C1 and C2 are chosen to be 6.8 pF instead of 10 pF, this causes the RTC to oscillate at a higher frequency at room temperature (+23 ppm). However, this configuration of C1 and C2 makes the circuit oscillate closer to 32.768 kHz at 0° C. The 6.8 pF value of C1 and C2 is the practical value.

Note: The temperature dependency of crystal frequency is a parabolic relationship (ppm / degree squared). The effect of the changing crystal's frequency when operating at 0° C (25° C below room temperature) is the same when operating at 50° C (25° C above room temperature).

9.6.4 RTC Layout Considerations

Since the RTC circuit is very sensitive and requires high accurate oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. ICH3-S requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn pin). Route the RTC circuit short to simplify the trace length measurement and increase accuracy when calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR-4 board material, a 5 mils trace has approximately 2 pF per inch.
- Reduce trace signal coupling by avoiding routing of adjacent PCI signals close to RTCX1, RTCX2, and VBIAS.

9.6.5 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH3-S is not powered by the system.

Example batteries are: Duracell 2032, 2025, or 2016 (or equivalent), which may give many years of operation.

Batteries are rated by storage capacity. The battery life may be calculated by dividing the capacity by the average current required. For example, when the battery storage capacity is 170 mAh (assumed usable), and the average current required is 3 µA, the battery life may be at least:

170,000 µAh / 3 µA = 56,666 h = 6.4 years

The voltage of the battery may affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. The battery voltage of the RTC must be greater than 2 V at all times to ensure the accuracy of the RTC clock.

Connect the battery to the ICH3-S via an isolation diode circuit. The diode circuit allows the ICH3-S RTC-well to be powered by the battery when the system power is not available, and by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 116 is an example of a diode circuit. As noted, a standby power supply should be used in a server system to provide continuous power to the RTC when available to significantly increase the RTC battery life

9.6.6 VBIAS DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC Network of R2 and C3 (see Figure 116); therefore, it is a self-adjusted voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200 mV DC. The RC network of R2 and C3 filters out most of the AC signals that exist on this pin. However, the noise on this pin should be kept to a minimum to ensure the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX1 and RTCX2 signals (using Op-Amp). See application note *AP-728, Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*, for further details on measuring techniques.

Note: VBIAS is also very sensitive to environmental conditions.

9.6.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle may be between 30% and 70%.

When the SUSCLK duty cycle is beyond the 30%–70% range, there is a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK may be probed directly using a normal probe (50 Ω input impedance probe), and it is an appropriate signal to check the RTC frequency to determine the accuracy of the ICH3-S RTC clock.

9.6.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in the G3 state. RTCRST#, when configured as shown in Figure 116, meets this requirement. RSMRST# should have a weak external pull-down to ground, and INTRUDER# should have a weak external pull-up to VCCRTC. This may prevent these nodes from floating in G3, and correspondingly may prevent ICCRTC leakage that may cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

9.7 Internal LAN Layout Guidelines

The ICH3-S provides various options for integrated LAN capability. The platform supports several components depending on the target market. The guidelines use the term 82562ET to refer to both the Intel® 82562ET, and the Intel® 82562EM. The Intel® 82562EM is specified in those cases where a difference exists. Table 82 presents the internal LAN layout guidelines.

Table 82. Internal LAN Layout Guidelines

Platform LAN Connect Component	Connection	Features
Intel® 82562EM	Advanced 10/100 Ethernet	Alert on LAN* & Ethernet 10/100 Connection
Intel® 82562ET	10/100 Ethernet	Ethernet 10/100 Connection

Design guidelines are provided for each required interface and connection. Refer to Figure 117 and Table 83 for the corresponding section of the design guide.

Figure 117. Platform LAN Connect

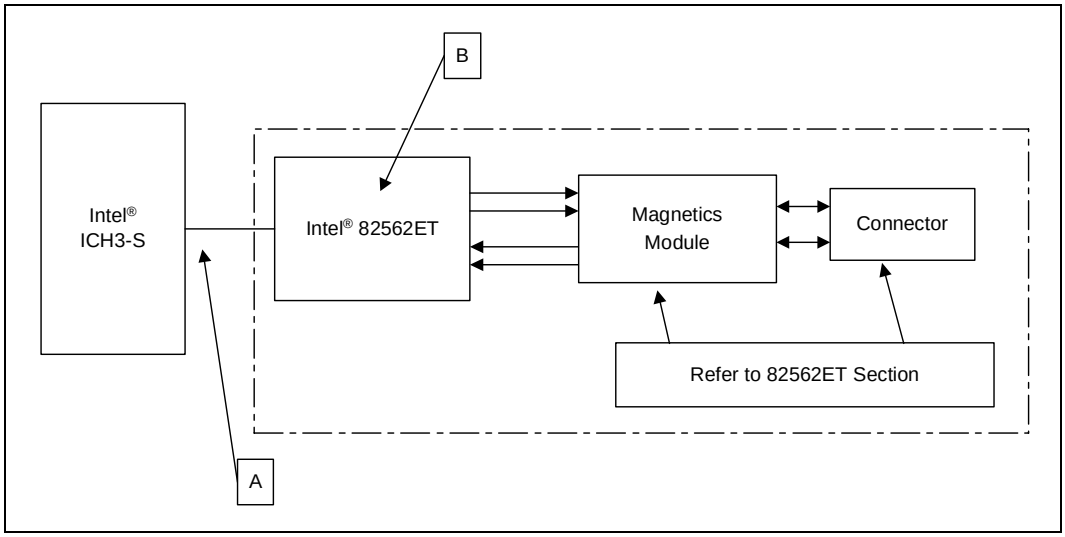


Table 83. LAN Design Guide Section Reference

Layout Section	Figure 117 Reference	Design Guide Section
Intel® ICH3-S – LAN Connect Interface	A	Section 9.7.1, “LCI (LAN Connect Interface) Guidelines”
General Routing Guidelines	B	Section 9.7.2, “General LAN Routing Guidelines and Considerations”
Intel® 82562ET / Intel® 82562EM	B	Section 9.7.3, “Intel® 82562ET/Intel® 82562EM Guidelines”

9.7.1 LCI (LAN Connect Interface) Guidelines

This section contains guidelines on how to implement a Platform LAN Connect (PLC) device on a system motherboard using LCI. It should not be treated as a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH3-S to LAN component interface. The following signal lines are used on this interface:

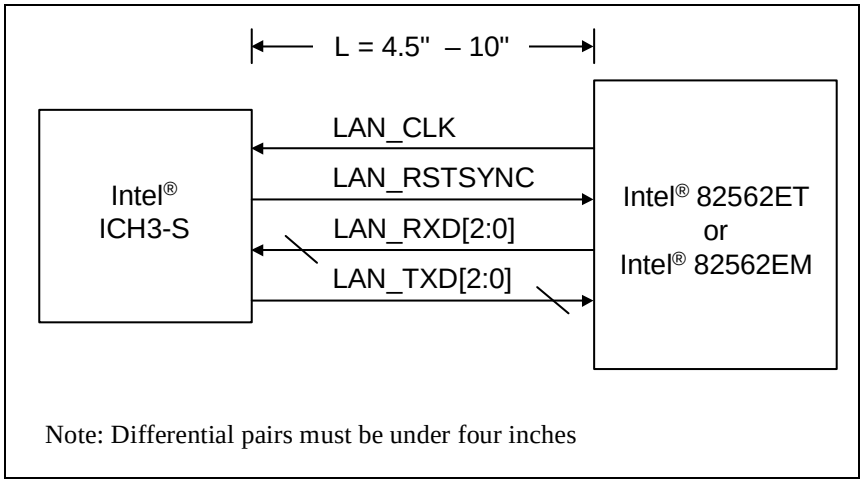
- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports Intel® 82562ET/Intel® 82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD0, and LAN_TXD0 are shared by all components.

9.7.1.1 Bus Topology

The LAN Connect Interface must be configured in direct point-to-point connection between the ICH3-S and the LAN component topology (see Figure 118).

Figure 118. Point-to-Point Interconnect Guideline



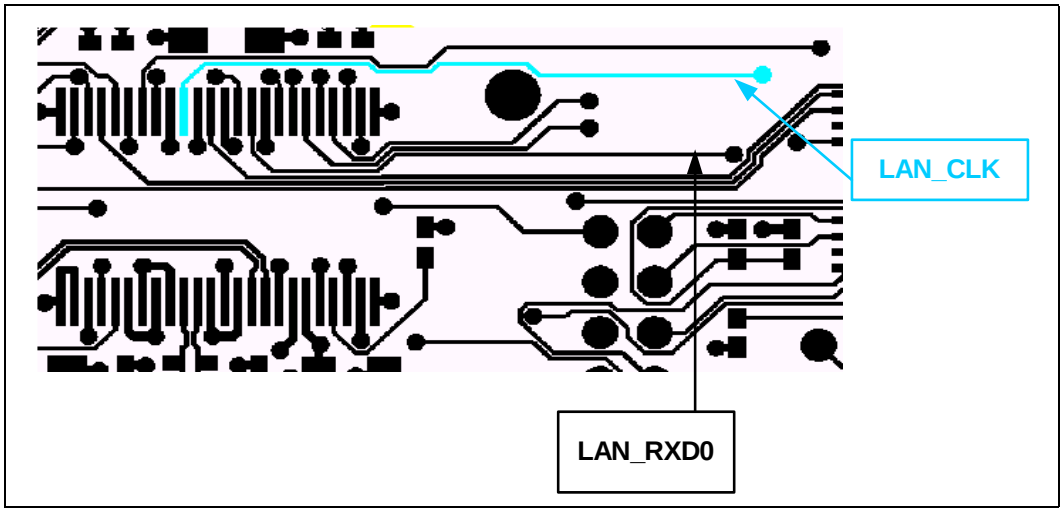
9.7.1.2 LCI Routing Parameters

Route the LCI signals carefully on the motherboard to meet the timing and signal quality requirements of this interface specification. The board designer should simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. Table 84 presents the LCI routing parameter summary. Figure 119 shows the LAN_CLK routing example.

Table 84. LCI Routing Parameter Summary

Parameter	Requirements
Trace Impedance (Z_0)	60 Ω ± 15% due to signal integrity requirements.
Trace Spacing	Minimum of 100 mils from non-LCI signals.
Termination	33 Ω series resistor may be installed at the driver side of the interface.
Length Tuning	On the motherboard, the length of each data trace should be either equal in length to the LAN_CLK trace, or up to 0.5 inch shorter than the LAN_CLK trace. LAN_CLK should always be the longest motherboard trace in each group.

Figure 119. LAN_CLK Routing Example



9.7.2 General LAN Routing Guidelines and Considerations

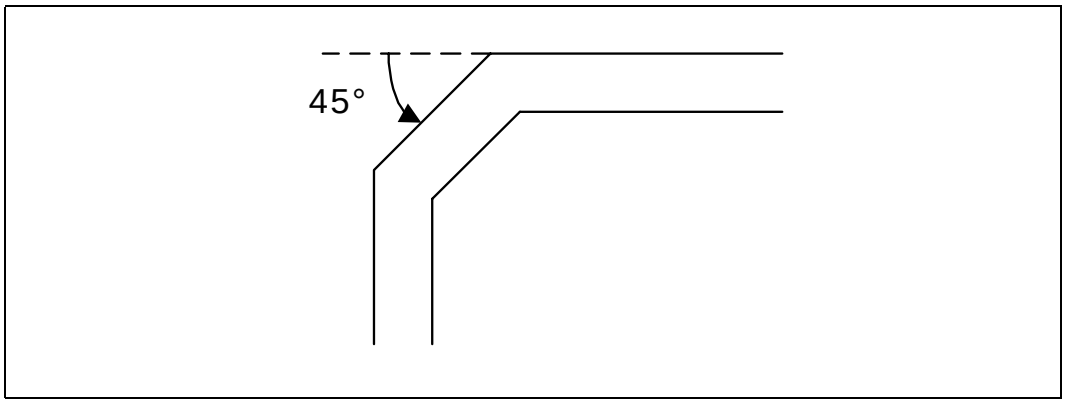
9.7.2.1 General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance:

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under four inches. (Many customer designs with differential traces longer than five inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER [Bit Error Rate].)
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces parallel to the differential traces, or closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to 7 mils.

- For high-speed signals, the number of corners and vias should be kept to a minimum. When a 90 degree bend is required, it is recommended to use two 45-degree bends instead. Refer to Figure 120.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This may prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 120. Routing a 90-Degree Bend



9.7.2.2 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length, and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another when the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which may lower the differential impedance by up to 10 Ω.

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also, for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than 1 inch to the connector/magnetic edge of the board.

9.7.2.3 Signal Isolation

Follow these rules for signal isolation:

- Separate and group signals by function on separate layers when possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Over the length of the trace run, each differential pair should be at least 0.3 inch away from any parallel signal traces.

- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which may increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

9.7.2.4 Power and Ground Connections

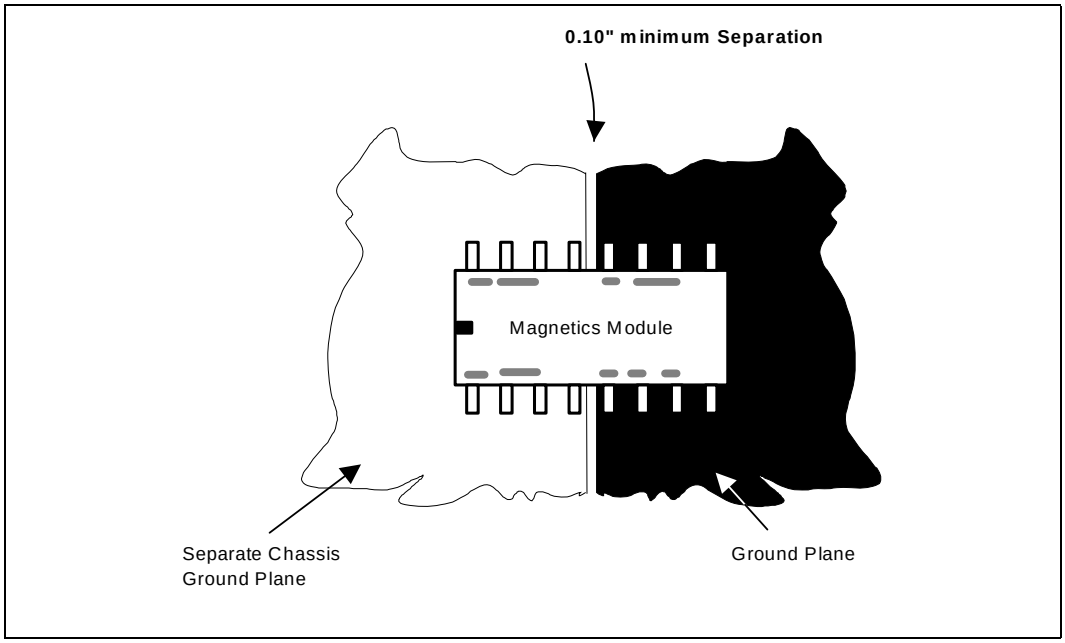
Follow these rules for power and ground connections:

- All VCC balls should be connected to the same power supply.
- All VSS balls should be connected to the same ground plane.
- Four to six decoupling capacitors, including two 4.7 µF capacitors, are recommended.
- Place decoupling as close as possible to power balls.

9.7.2.5 General Power and Ground Plane Consideration

To properly implement the common mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum. Figure 121 shows the ground plane separation.

Figure 121. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return. These may significantly reduce EMI radiation.

The following are guidelines that help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions (don't route over a plane split). When vacant areas exist on a ground or power plane, avoid routing signals over the vacant area. Routing over a vacant area may increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This may minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high-frequency harmonics, which may radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

9.7.2.6 Board Design

The following recommendations are based on a ground referenced design.

- Top Layer Routing

  Sensitive analog signals are routed completely on the top layer without the use of vias. This allows tight control of signal integrity, and removes any impedance inconsistencies due to layer changes.

- Ground Plane

  A layout split (100 mils) of the ground plane under the magnetics module between the primary and secondary side of the module is recommended. It is also recommended to minimize the digital noise injected into the 82562 common ground plane. Suggestions include optimizing decoupling on neighboring noisy digital components, isolating the 82562 digital ground using a ground cutout, etc.

- Power Plane

  Physically separate digital and analog power planes must be provided to prevent digital switching noise from being coupled into the analog power supply plane’s VDD_A. Analog power may be a metal fill ‘island’, separated and RC filtered from digital power.

- Signal Layer Routing

  The digital high-speed signals, which include all of the LAN interconnect interface signals, must be routed on an internal signal layer away from the analog signals.

9.7.2.7 Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs:

- Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and may distort the transmit or receive waveforms.

- Lack of symmetry between the two traces within a differential pair. (For each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry may create common-mode noise and distort the waveforms.
- Excessive distance between the PLC and the magnetics or between the magnetics and the RJ45/11 connector. Beyond a total distance of about four inches, it may become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) may attenuate the analog signals. In addition, any impedance mismatch in the traces may be aggravated when they are long. The magnetics should be as close to the connector as possible (≤ 1 inch).
- Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel may cause degraded long cable BER. Crosstalk getting onto the transmit channel may cause excessive emissions (failing FCC), and may cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inch from the differential traces.
- Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces may put more crosstalk onto the closest receive trace and may greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inch or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ45/11, and the PLC.
- Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
- Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or application note.
- Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. When these are not terminated properly, there may be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The application notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
- Incorrect differential trace impedances. It is important to have ~100 Ω differential impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they've designed for 100 Ω. (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling may lower the effective differential impedance by 5 Ω–20 Ω. A 10 Ω–15 Ω drop in impedance is common.) Short traces may have fewer problems when the differential impedance is a little off.
- Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations may slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This may also cause return loss to fail at higher frequencies and may degrade the transmit BER performance. Caution

should be exercised when a capacitor is put in either of these locations. When a capacitor is used, it should almost certainly be less than 22 pF (6 pF to 12 pF values have been used on past designs with reasonably good success). These capacitors are not necessary, unless there is some overshoot in 100 Mbps mode.

Note: It is important to keep the two traces within a differential pair close to each other. Keeping them close helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces.

Note: 'Close' should be considered to be less than 0.03 inch between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

9.7.3 Intel® 82562ET/Intel® 82562EM Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 9.7.2, "General LAN Routing Guidelines and Considerations". Additional guidelines for implementing an 82562ET or 82562EM platform LAN connect component are provided in the following sections.

9.7.3.1 Intel® 82562ET/Intel® 82562EM Component Placement Guidelines

Component placement may affect signal quality, emissions, and temperature of a board design. This section provides guidelines for component placement.

Careful component placement may:

- Decrease potential problems directly related to electromagnetic interference (EMI), which may cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation affects the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.7.3.2 Crystals and Oscillators

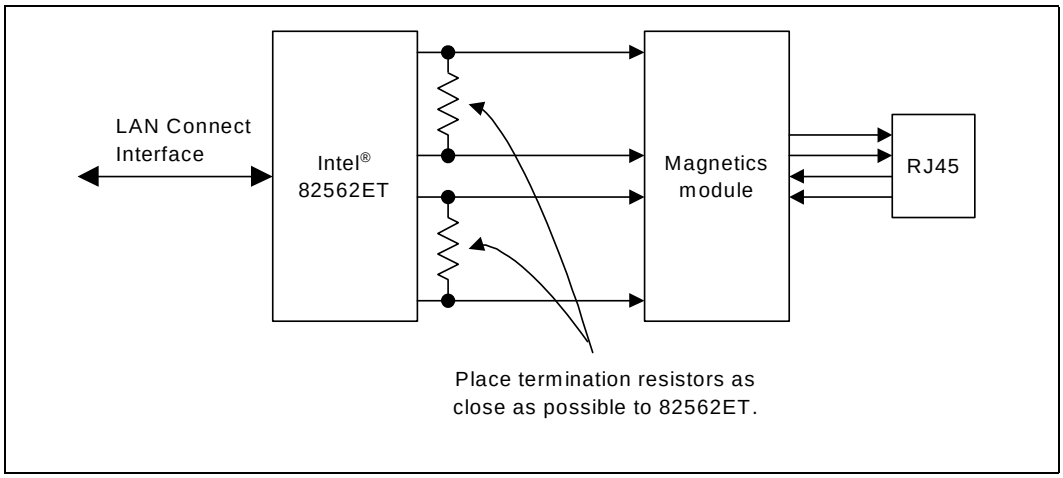
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (when they should exist) should be grounded to prevent possibility of radiation from the crystal case, and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562ET or 82562EM, keeping the trace length as short as possible. Do not route any noisy signals in this area.

9.7.3.3 Intel® 82562ET/Intel® 82562EM Termination Resistors

The 100 Ω ± 1% resistor used to terminate the differential transmit pairs (TDP/TDN), and the 121 Ω ± 1% resistor used to terminate the differential receive pairs (RDP/RDN) should be placed as close to the Platform LAN connect component (82562ET or 82562EM) as possible. This is due to the fact that these resistors are terminating the entire impedance that is seen at the termination source (i.e., Intel 82562ET), including the wire impedance reflected through the transformer. Figure 122 shows the Intel 82562ET/EM termination.

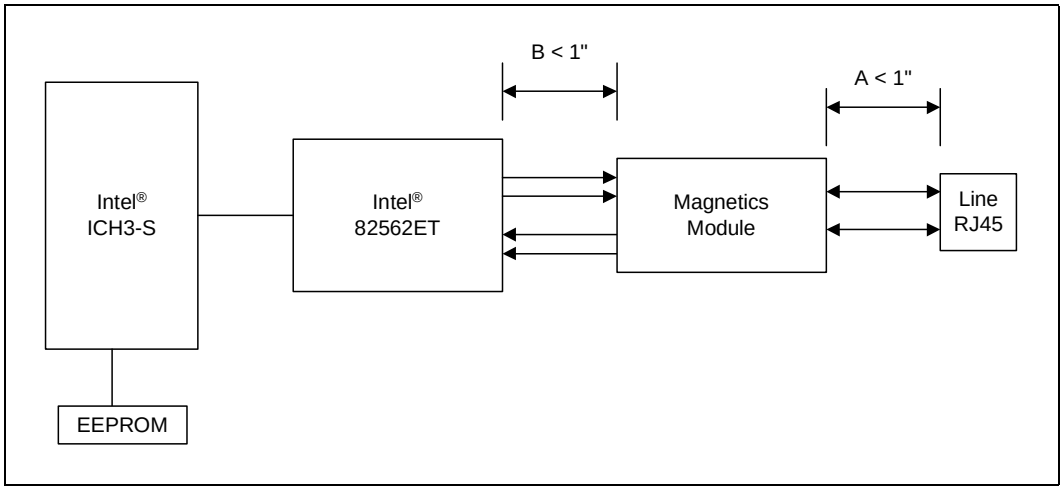
Figure 122. Intel® 82562ET/Intel® 82562EM Termination



9.7.4 Critical Dimensions

There are two dimensions to consider during layout. Distance 'A' from the line RJ45 connector to the magnetics module, and distance 'B' from the 82562ET or 82562EM to the magnetics module. The combined total distances A and B must not exceed two inches (see Figure 123).

Figure 123. Critical Dimensions for Component Placement



9.7.4.1 Distance from Magnetics Module to RJ45 (Distance A)

The distance A in Figure 123 should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than 1 inch of separation. The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance may be approximately 50 Ω; however, the differential impedance may also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation, and with exactly the same lengths and physical dimensions (for example, width).

Warning: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This may degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. When the 82562ET must be placed further than a couple of inches from the RJ45 connector, distance B may be sacrificed. Keeping the total distance between the 82562ET and RJ45 as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often results in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. When the actual impedance is consistently low, a target of 105 Ω –110 Ω should compensate for second order effects.

9.7.4.2 Distance from Intel® 82562ET to Magnetics Module (Distance B)

Distance B should also be designed to be less than 1 inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals may reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and equal length within each differential pair.

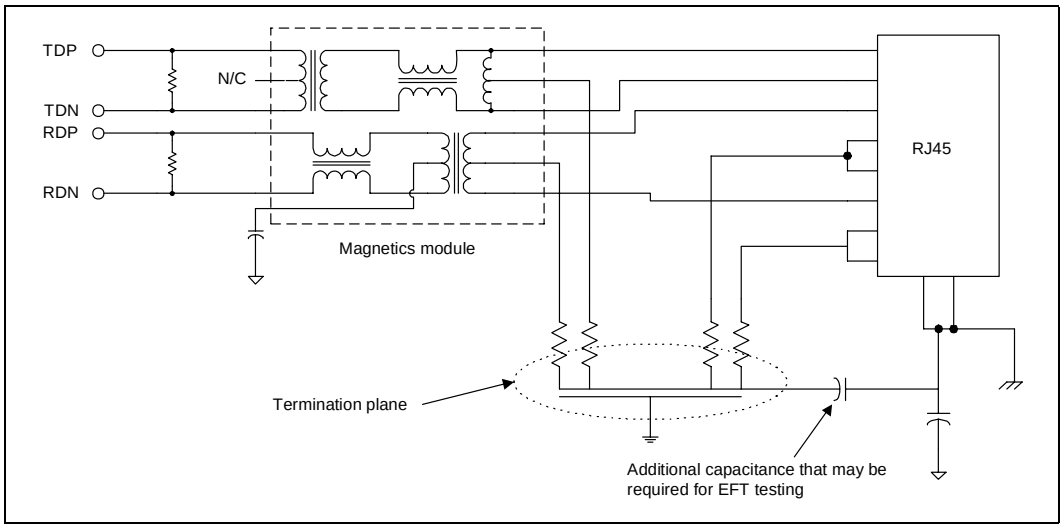
9.7.5 Terminating Unused Connections

In Ethernet designs, it is common practice to terminate unused connections on the RJ45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the Bob Smith Termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane, and couples capacitively to the ground plane, creating the required 1500 pF of capacitance. The signals may be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

9.7.5.1 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required when the termplane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. When a discrete capacitor is used to meet the EFT requirements, it should be rated for at least 1000 Vac. Figure 124 shows the termination plane.

Figure 124. Termination Plane



Debug Port and Logic Analyzer Interface 10

10.1 ITP Support

10.1.1 Overview

One key tool that is needed to debug BIOS, logic, signal integrity, general software, and general hardware issues involving CPUs, chipsets, SIOs, PCI devices, and other hardware in a platform design is the In Target Probe (ITP). The ITP is widely used by various validation, test, and debug groups from third party BIOS vendors, OEMs, and other developers.

10.1.2 Implementation

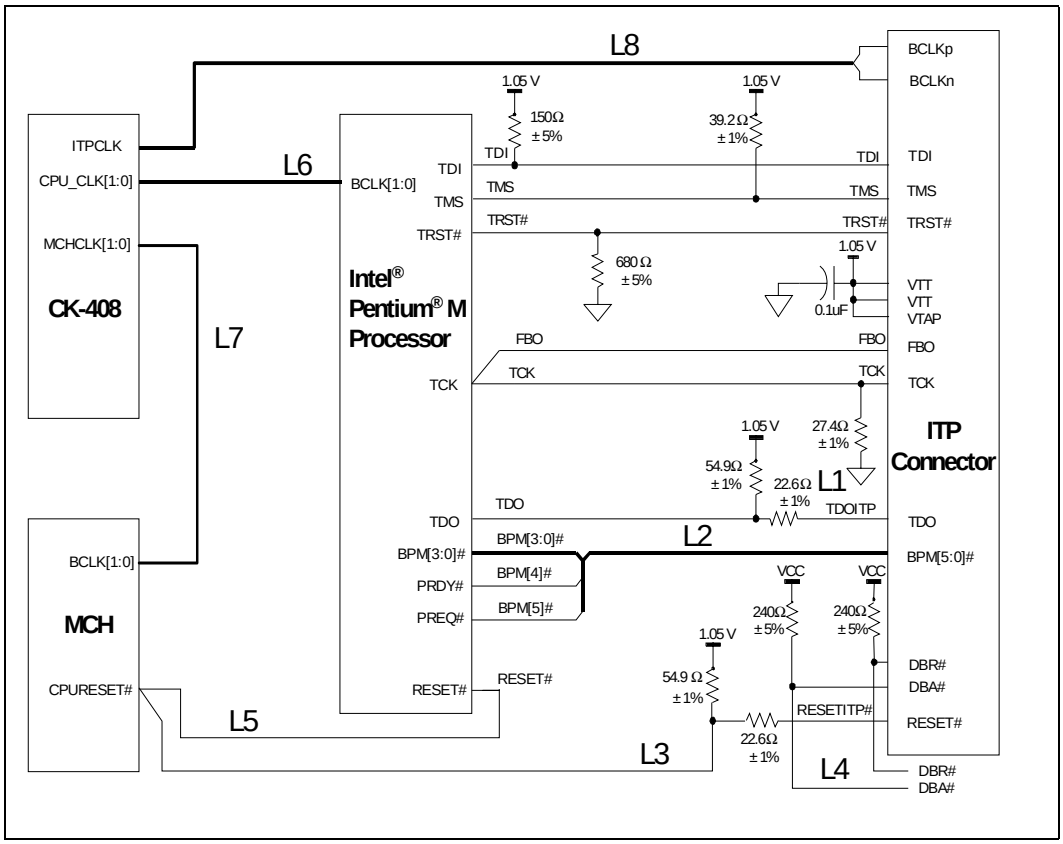
To minimize the ITP connector footprint, the ITP700FLEX is an alternate option. Note that the termination resistors do not need to be stuffed (thus zero additional BOM cost). However, standard signal connection guidelines for the CPU's TAP logic signals for the non-ITP case still need to be followed. In other words, only the traces and component footprints need to be added to the design, with all previous 'non-ITP' guidelines followed otherwise. This way, when ITP support is needed, the termination resistor and connector may be populated as needed for debug support. Note also that when the ITP700FLEX footprint cannot be followed due to mechanical, routing, or footprint reasons, it is acceptable to have a simple via grouping in lieu of the connector to allow for 'blue-wiring' of the ITP.

10.2 Recommended Onboard ITP700FLEX Implementation

10.2.1 ITP Signal Routing Guidelines

Figure 125 illustrates recommended connections between the onboard ITP700FLEX debug port, Intel® Pentium® M processor, Intel® E7501 MCH, and CK-408 clock chip in the cases where the debug port is used.

Figure 125. ITP700FLEX Debug Port Signals



10.2.1.1 TDI, TMS and TRST# Routing Requirements

Route the TDI signal between the ITP700FLEX connector and the Intel Pentium M processor. A 150 Ω ± 5% pull-up to VCCP (1.05 V) should be placed within ± 300 ps of the processor's TDI pin.

Route the TMS signal between the ITP700FLEX connector and the Intel Pentium M processor. A 39.2 Ω ± 1% pull-up to VCCP should be placed within ± 200 ps of the ITP700FLEX connector pin.

Route the TRST# signal between the ITP700FLEX connector and the Intel Pentium M processor. A 510 Ω to 680 Ω ± 5% pull-down to ground should be placed on TRST#. Placement of the pull down resistor is not critical. Avoid having any trace stub from the TRST# signal line to the termination resistor.

10.2.1.2 TCK and TDO Routing Requirements

Route the TCK signal from the ITP700FLEX connector's TCK pin to the Intel Pentium M processor's TCK pin and then fork back from the Intel Pentium M processor TCK pin and route back to the ITP700FLEX connector's FBO pin. A 27.4 Ω ± 1% pull-down to ground should be placed within ± 200 ps of the ITP700FLEX connector pin.

Route the TDO signal from the Intel Pentium M processor to a 54.9 Ω ± 1% pull-up resistor to VCCP that should be placed close to the ITP700FLEX connector's TDO pin. Then insert a 22.6 Ω ± 1% series resistor to connect the 54.9 Ω pull-up and TDOITP net (see Figure 125). Limit the L1 segment length of the TDOITP net to be less than 1.0 inch.

10.2.1.3 BPMx# Routing Requirements

The Intel Pentium M processor drives the BPM[4:0]# signals to the ITP700FLEX at a 100-MHz clock rate. Route the BPM[4:0]# as a Zo=50 Ω point-to-point transmission line connection between the processor and the ITP700FLEX connector. Connect the ITP700FLEX connector's BPM[3:0]# pins to the Intel Pentium M processor's BPM[3:0]# pins. Connect the ITP700FLEX's BPM[4]# signal to the Intel Pentium M processor's PRDY# pin. The ITP700FLEX's integrated far-end terminations as well as the processor's AGTL+ integrated on-die termination ensure proper signal quality for the BPM[4:0]# signals. Due to the length of the ITP700FLEX cable, the length L2 of the BPM[4:0]# signals on the motherboard should be limited to be shorter than 6.0 inches. The BPM[4:0]# signals' length L2 should be length matched to each other within ± 50 ps. The BPM[4:0]# signal trace lengths are matched inside the Intel Pentium M processor package, thus motherboard routing does **not** need to compensate for any processor package trace length mismatch. The BPM[4:0]# signal lengths also need to be matched within ± 50 ps to the L3+L4-L5 net lengths of the RESET# signal.

$$L3 + L4 - L5 = L2 \text{ (within } \pm 50 \text{ ps)}$$

See Figure 125 for topology. See below for more details on routing guidelines for the RESET# signal.

Due to the Intel Pentium M processor's AGTL+ on-die termination for BPM[3:0]# and PRDY#, there is no issue or concern when the BPM[4:0]# pins of the ITP700FLEX connector are left floating when the ITP is not being used and the ITP700FLEX cable is unplugged.

Route the ITP700FLEX connector's BPM[5]# signal as a Zo = 50 Ω point-to-point connection to the Intel Pentium M processor's PREQ# pin. Integrated on the ITP700FLEX BPM[5]# driver signal is a resistive pull-up that ensures proper signal quality at the processor's PREQ# input pin. The IIntel Pentium M processor has an integrated, weak, on-die pull-up to V_{CCP} for the PREQ# signal to ensure a proper logic level when the ITP700FLEX port connector is not plugged in. There is no need for any external termination on the motherboard for the BPM[5]# = PREQ# signal. The maximum length of BPM[5]#/PREQ# should not exceed 6.0 inches.

10.2.1.4 RESET# Routing Guidelines

As explained in Section 5.1.4.2, "Processor RESET# Signal" the RESET# signal forks (see Figure 26 and Figure 125) out from the Intel® E7501 MCH's CPURESET# pin and is routed to the Intel® Pentium® M processor (because of this fork, the L5 segment is subtracted from the total length) and ITP700FLEX debug port. One branch from the fork connects to the Intel Pentium M processor's RESET# pin and the second branch connects to a 54.9 Ω ± 1% termination pull-up resistor to V_{CCP} placed close to the ITP700FLEX debug port. A series 22.6 Ω ± 1% resistor is used to continue the path to the ITP700FLEX RESET# pin with the RESETITP# net in Figure 125.

The length of the RESETITP# net (labeled as net L4) should be limited to be less than 0.5 inches. To ensure correct operational timings, the length of the RESET# nets L3, L4, and L5 with respect to the BPM[4:0]# net length L2 should adhere the following length matching requirement within ± 50 ps.

L3 + L4 – L5 = L2 (within ± 50 ps)

There is no need for pull-up termination on the Intel Pentium M processor side of the RESET# net due to presence of AGTL+ on-die termination on the processor and the Intel E7501 MCH.

10.2.1.5 BCLK Routing Requirements

The ITP700FLEX debug port's BCLKp/BCLKn inputs are driven with a 100-MHz differential clock from the CK-408 clock chip and require 33 Ω series resistors. The CK-408 also feeds another two pairs of 100-MHz differential clocks to the Intel Pentium M processor's BCLK[1:0] and Intel® E7501 chipset's BCLK[1:0] input pins. Common clock signal timing requirements of the Intel® E7501 MCH and the Intel Pentium M processor requires matching of processor and MCH BCLK[1:0] nets L6 and L7, respectively. To ensure correct operation of the ITP700FLEX, the BCLKp/BCLKn net L8 should be tuned to be within ± 50 ps to the sum of length L6 of the BCLK[1:0] lines and the additional length L2 of the BPM#[4:0] signals.

L6 + L2 = L8 (within ± 50 ps)

10.2.1.6 ITPFLEX Routing Requirement Summary

The timing requirements for the BPM[5:0]#, RESET#, and BCLKp/BCLKn signals of the ITP700FLEX debug port requires careful attention to their routing. Standard high frequency bus routing practices should be observed.

1. Keep a minimum of 2:1 spacing in between these signals and to other signals.
2. Reference these signals to ground planes and avoid routing across power plane splits.
3. The number of routing layer transitions should be minimized. When layout constraints require a routing layer transition, any such transition should be accompanied with ground stitching vias placed within 100 mils of the signal via with at least one ground via for every two signals making a layer transition.

The ITP700FLEX VTT and VTAP pins should be shorted together and connected to the VCCP (1.05 V) plane with a 0.1 µF decoupling capacitor placed within 0.1 inch of the VTT pins.

Table 85 summarizes termination resistors values, placement, and voltages the ITP signals need to connect to for proper operation for onboard ITP700FLEX debug port.

Table 85. Recommended ITP700FLEX Signal Terminations

Signal	Termination Value	Termination Voltage	Termination/Decap Location	Notes
TDI	150 Ω ± 5%	VCCP (1.05 V)	Within ± 300 ps of the Intel® Pentium® M processor CPU TDI pin.	5
TMS	39.2 Ω ± 1%	VCCP (1.05 V)	Within ± 200 ps of the ITP700FLEX connector TMS pin.	5
TRST#	510 – 680 Ω ± 5%	GND	Anywhere between the Intel Pentium M processor CPU and ITP700FLEX connector.	5
TCK	27.4 Ω ± 1%	GND	Within ± 200 ps of the ITP700FLEX connector TCK pin.	5
TDO	54.9 Ω ± 1% pull-up and 22.6 Ω ± 1% series resistor	VCCP (1.05 V)	Within one inch of the ITP700FLEX connector TDO pin.	1, 5
BCLK(p/n)				2
FBO	Connect to TCK pin of the Intel Pentium M processor CPU.	N/A	N/A	1
RESET#	54.9 Ω ± 1% pull-up and 22.6 Ω ± 1% series resistor	VCCP (1.05 V)	Within 0.5” of the ITP700FLEX connector RESET# pin.	1
BPM[5:0]#	Not Required			3
DBA#	150-240 Ω ± 5%	VCC of target system recovery circuit.	Within 1 ns of the ITP700FLEX connector DBA# pin.	4
DBR#	150-240 Ω ± 5%	VCC of target system recovery circuit	Within 1 ns of the ITP700FLEX connector DBR# pin.	
VTAP	Short to VCCP plane.	VCCP (1.05 V)		
VTT	Short to VCCP plane.	VCCP (1.05 V)	Add 0.1 µF decap within 0.1 inch of VTT pins of ITP700FLEX connector.	

NOTES:
1. See Figure 125.
2. Refer to Section 10.2.1, “ITP Signal Routing Guidelines”.
3. All of the needed terminations to ensure proper signal quality are integrated inside the Intel Pentium M processor AGTL+ buffers or inside the ITP700FLEX debug port. No need for any external components for the BPM[5:0]# signals.
4. Only required when DBA# is used with any target system circuitry. This signal may be left unconnected when unused.
5. In cases where a system is designed to utilize the ITP700FLEX debug port for debug purposes but the ITP700FLEX connector may or may not be populated at all times although the signal routing and termination or decoupling components are implemented, the component placement guidelines should adhere to the ones listed in Table 85. However, for signals where the termination component placement guidelines for non-ITP700FLEX supported systems (see Table 29) are more restrictive or conservative than the component placement guidelines for the ITP700FLEX supported case, then the more conservative/restrictive guidelines should be followed.

10.3 Intel® Pentium® M Processor Logic Analyzer Support

10.3.1 Overview

A second key tool that is necessary to debug BIOS, logic, signal integrity, general software, and general hardware issues involving CPUs, chipsets, SIOs, PCI devices, and other hardware in platform design is the Intel Pentium M processor system bus logic analyzer probe. This tool is widely used by various validation, test, and debug groups from third party BIOS vendors, OEMs, and other developers).

There are two primary requirements for providing LAI support:

1. Providing a motherboard with a compatible CPU socket. The Intel Pentium M processor system bus logic analyzer probe is an interposer that plugs into the CPU socket, and the CPU then plugs into the LAI. The use of non-standard sockets may also prohibit the logic analyzer probe from working as the locking mechanism may become inaccessible. It is important to check the logic analyzer probe design guidelines to ensure a particular socket may work. Note that the logic analyzer probe was designed to accommodate the most common Intel Pentium M processor sockets on the market.
2. Observing Intel Pentium M processor system bus logic analyzer probe keepout requirements. There are several options to achieving this. Removing the motherboard from the case is typically the first step to meeting keepout requirements. When keepouts still cannot be met, Intel strongly recommends building a separate debug motherboard that has the same bill of material (BOM) and netlist, but with Intel Pentium M processor system bus logic analyzer probe keepout requirements met (this also provides the opportunity to add other test-points).

10.3.2 Implementation

Agilent Technologies* can provide details on the Intel Pentium M processor system bus logic analyzer probe mechanicals (i.e., design guide with keepout info).

10.4 Logic Analyzer Interface (LAI)

Contact LAI vendors to obtain specific information about their LAIs. The following information is general in nature.

Due to the complexity of an Intel Pentium M processor-based system, the LAI is critical in providing the ability to probe and capture Intel Pentium M processor system bus signals. There are two sets of considerations to keep in mind when designing an Intel Pentium M processor-based system that may make use of an LAI:

- Mechanical
- Electrical

10.4.1 Mechanical Considerations

The LAI is installed between the processor socket and the Intel Pentium M processor. The LAI pins plug into the socket, while the Intel Pentium M processor plugs into a socket on the LAI. Cabling this part of the LAI egresses the system to allow an electrical connection between the Intel Pentium M processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keep-out volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may include space normally occupied by the Intel Pentium M processor heat sink. When this is the case, the logic analyzer vendor may provide a cooling solution as part of the LAI.

10.4.2 Electrical Considerations

The LAI may also affect the electrical performance of the Intel Pentium M processor system bus. Therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool may work in the system. Contact the logic analyzer vendor for electrical specifications as load models for the LAI solution they provide.

Platform Power Delivery Guidelines 11

This chapter provides an example for board power delivery of an Intel® Pentium® M Processor and Intel® E7501 chipset-based platform. There are many methods to implement a power delivery system, and this is only one example.

A voltage regulator (VR) is used to regulate power to the core and Intel Pentium M processor system bus rails of the Intel Pentium M processor and the Intel® E7501 chipset PSB. A separate voltage regulator is required for the Intel® E7501 chipset core. The Intel Pentium M processor is offered in Micro-FCPGA packages for socketable boards and Micro-FCBGA packages for surface mount boards.

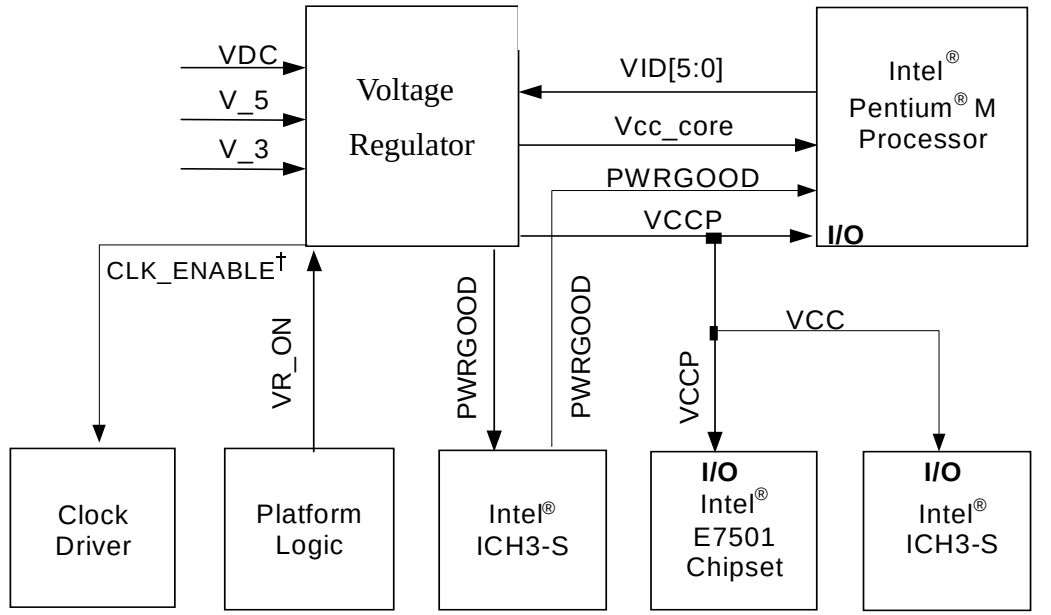
The Intel Pentium M processor supports Enhanced Intel® SpeedStep® technology, which enables real-time dynamic switching of the voltage and frequency between multiple performance modes. This occurs by switching the bus ratios, core operating voltage, and core processor speeds without resetting the system. With Enhanced Intel SpeedStep technology, there will be more than two modes of operation. The processor will be able to operate in more than two voltage levels. Although this specification addresses the highest processor core frequency and the lowest processor core frequency, there will be other modes where the voltage command may be different than that of these two modes.

Terminology used to reference the names of the voltage rails are defined below.

- V_{CC_CORE} is the core rail of the processor.
- V_{CCP} is the PSB rail of the processor and MCH, and is also used for CPU signals of the ICH3-S chipset and the CPU ITP700FLEX debug port when used.

11.1 Processor Voltage Regulator Power Delivery Architectural Block Diagram

Figure 126. Processor Voltage Regulator Block Diagram



NOTES:

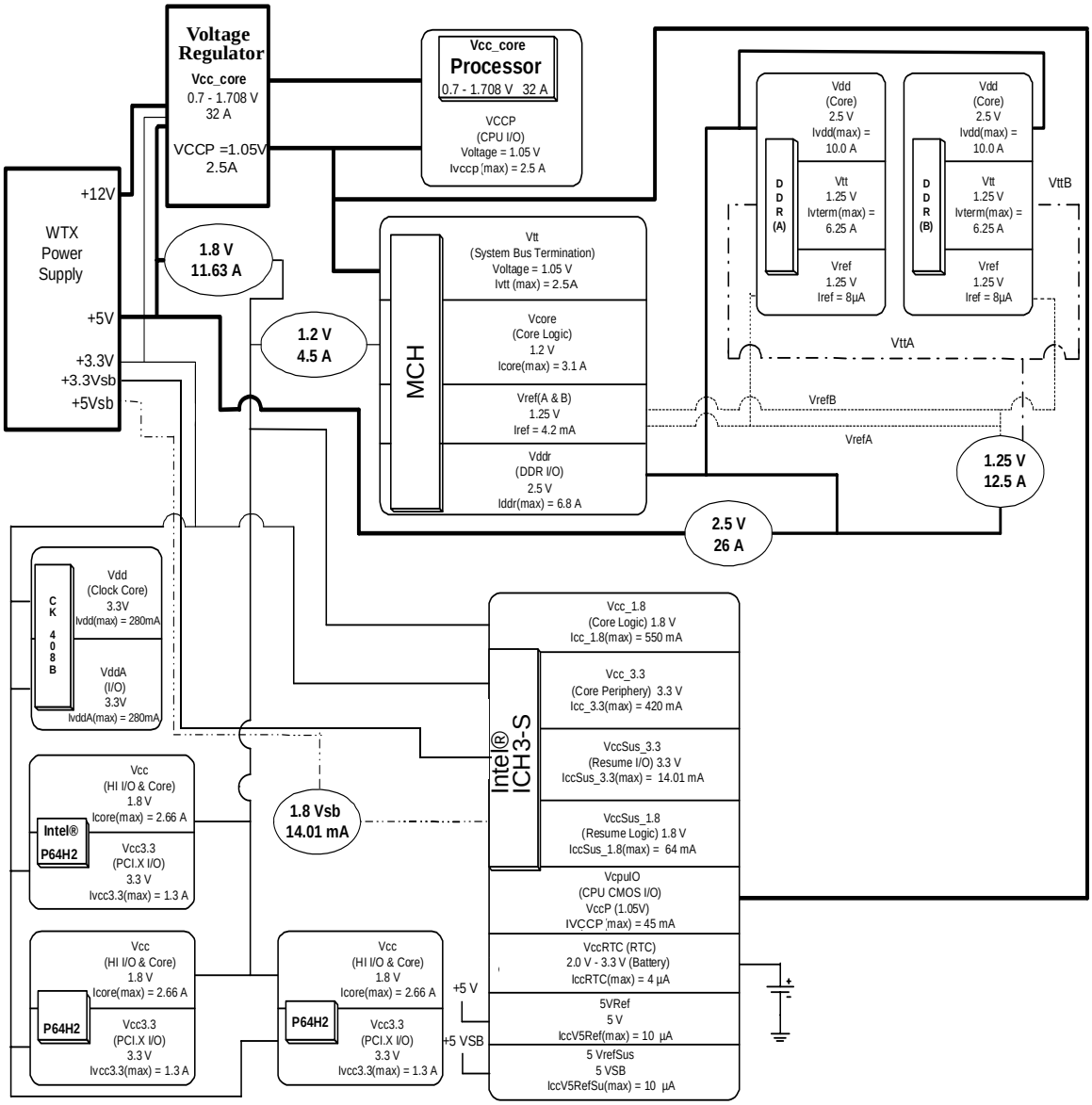
† Desired, but not required feature of a voltage regulator compliant controller. When not implemented by the voltage regulator, both the CLK_ENABLE# and the $t_{CPU-PWRGD}$ timer must be implemented by platform control logic.

The voltage regulator receives three input power rails, VDC, V_5, and V_3. VDC is the main power input to the system. VDC ranges between 5.5 – 21 V. V_5 is the output rail of the main 5.0 V voltage regulator (VR). This rail is typically used to provide drive power to the MOSFET gate driver. V_3 is the output rail of the 3.3 volt VR. This is typically used to provide power to the VR Controller and miscellaneous logic and pull-ups.

11.2 Customer Reference Board Power Delivery

Figure 127 shows the power delivery architecture for the Intel® Pentium® M processor and Intel® E7501 chipset customer reference board.

Figure 127. Power Delivery Example



NOTE: The examples given in this Design Guide are only examples. Many power distribution methods achieve similar results. It is critical, when deviating from these examples in any way, to consider the effects of the change.

11.2.1 Processor Core Voltage (V_{CC_CORE})

The Intel® Pentium® M processor uses six voltage identification pins, VID[5:0], to support automatic selection of power supply voltages. The VID pins for the Intel Pentium M processor are CMOS outputs driven by the processor VID circuitry. For more details about VR design to support the Intel Pentium M processor power supply requirements.

11.2.2 System Bus Voltage (VCCP 1.05 V)

Most Intel Pentium M processor system bus signals use Assisted Gunning Transceiver Logic (AGTL+) signalling technology. This signalling technology provides improved noise margins and reduced ringing through low-voltage swings and controlled edge rates. The termination voltage level for the Intel Pentium M processor AGTL+ signals is VCCP = 1.05 V (nominal).

The AGTL+ inputs require a reference voltage (GTLREF), which is used by the receivers to determine when a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board. Termination resistors are provided on the processor silicon and are terminated to its I/O voltage (VCCP).

The AGTL+ bus depends on incident wave switching. Therefore, timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the system bus, including trace lengths, is highly recommended when designing a system.

Note: VCCP on the Intel Pentium M processor corresponds to CPU_VCC on the Intel® E7501 MCH.

11.2.3 2.5 V

The 2.5 V power plane is used to provide power to the DDR DRAM core, the MCH DDR I/O ring, and reference voltage to the 1.25 V switching regulator. The 2.5 V power plane is created using a switching regulator, which should be able to support up to 26 A of current. This switching regulator receives its input directly from the 5 V power rail of the power supply. The DDR DRAM core requires at most 20.0 A of current. This value is a worst-case current, and is based on DRAM vendor specific specification for maximum current. Power levels may vary. In some cases, current requirements may be less than half of this maximum value, but a maximum current level of 20.0 A should be used to allow interoperability among DRAM devices. The current dedicated for VDD in the MCH is 6.8 A. This regulator is required in all designs.

11.2.4 1.25 V

A voltage regulator derived off 2.5 V produces two 1.25 V rails. One is for the MCH reference voltage (VREF); the other is for DDR termination voltage (V_{TERM}). The switching regulator divides the 2.5 V power rail by 2 to drive 1.25 V reference voltage. This provides some common-mode noise rejection between the DDR termination and I/O voltages. The entire power plane requires about 12 A of maximum current, and may be achieved by using either one or two regulators (one for both channels or one for each channel).

11.2.5 1.8 V

The 1.8 V power plane is created using a switching regulator sourcing from the 5 V power rail on the power supply. The 1.8 V plane powers the ICH3-S core logic, the 1.2 V regulator, and the Hub Interface I/O rings of the Intel® P64H2s. This voltage rail requires approximately 11.63 A maximum current. The Hub Interface on each Intel P64H2 device consumes about 2.66 A. The Hub Interface on the ICH3-S device consumes about 550 mA of current. This regulator is required in all designs.

11.2.6 1.2 V

The 1.2 V power plane powers the MCH core logic requiring 4.5 A. A switching regulator using the 5 V power rail is the regulator's input to power the 1.2V plane.

11.2.7 5 VSB

The 5 VSB power plane comes directly off the 5 VSB power rail and provides 1.8 VSB power through a linear regulator. The resume I/O segment of the ICH3-S requires 64 mA of current, while the 5 VSB-to-1.8 VSB regulator requires 14.01 mA.

11.2.8 3.3 VSB

The 3.3 VSB power plane comes directly off the 3.3 VSB power rail. The power plane is used solely for the resume I/O features of the Intel ICH3-S. This segment is given only about 64 mA. This regulator is required in all designs.

11.2.9 1.8 VSB

As stated before, the 1.8 VSB provides power to the resume logic within the Intel ICH3-S. This logic uses about 14 mA. This regulator is required in all designs.

11.2.10 Power Summary

Table 86 summarizes the platform power. For current up-to-date values, refer to each component's datasheet.

Table 86. Power Summary (Sheet 1 of 2)

Power Rail	Source	Destination	Max Current
0.7 - 1.708 V	Voltage regulator	CPU Core	32 A
1.05	Voltage regulator	CPU PSB, MCH PSB, Intel® ICH3-S	2.5 A
2.5 V	5 V power supply	MCH DDR	27 A
1.25 V	5 V to 2.5 V switching regulator	MCH DDR	12.5 A
1.8 V	5 V power supply	Intel® P64H2, Intel ICH3-S	13.86 A
1.2 V	1.8 V switching regulator	MCH	3.1 A

Table 86. Power Summary (Sheet 2 of 2)

Power Rail	Source	Destination	Max Current
5 VSB	Power Supply	3.3 VSB, 1.8 VSB	78 mA
3.3 VSB	Power supply	Intel ICH3-S	64 mA
1.8 VSB	5 VSB power supply	Intel ICH3-S	14 mA

11.3 Processor Power Delivery Design Guidelines

11.3.1 Processor PLL Power Delivery

VCCA[3:0] is a power source required by the PLL clock generators on the processor silicon. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system; it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). Traditionally this supply is low-pass filtered to prevent any performance degradation. The Intel® Pentium® M processor has an internal PLL super filter for the 1.8 V supply to the VCCA[3:0] pins that dispenses with the need for any external low-pass filtering. However, one 0603 form factor 10 nF and one 1206 form factor 10 µF decoupling capacitor should be placed as close as possible to each of the four VCCA pins (i.e., a pair of capacitors consisting of one 10-nF and one 10-µF should be used for each VCCA pin).

11.3.2 Voltage Identification for Intel® Pentium® M Processor

There are six voltage identification pins on the Intel Pentium M processor. These signals may be used to support automatic selection of V_{CC_CORE} voltages. They are needed to cleanly support voltage specification variations on current and future processors. VID[5:0] is defined in Table 87 below.

The VID[5:0] signals are 1.05 V CMOS level outputs. Intel recommends that 1:2 spacing and routing with a trace impedance of 50 Ω ± 10% be used. No external termination is required for VID[5:0]. To ensure signal quality, a point-to-point routing between the Intel Pentium M processor and the VRM should be used.

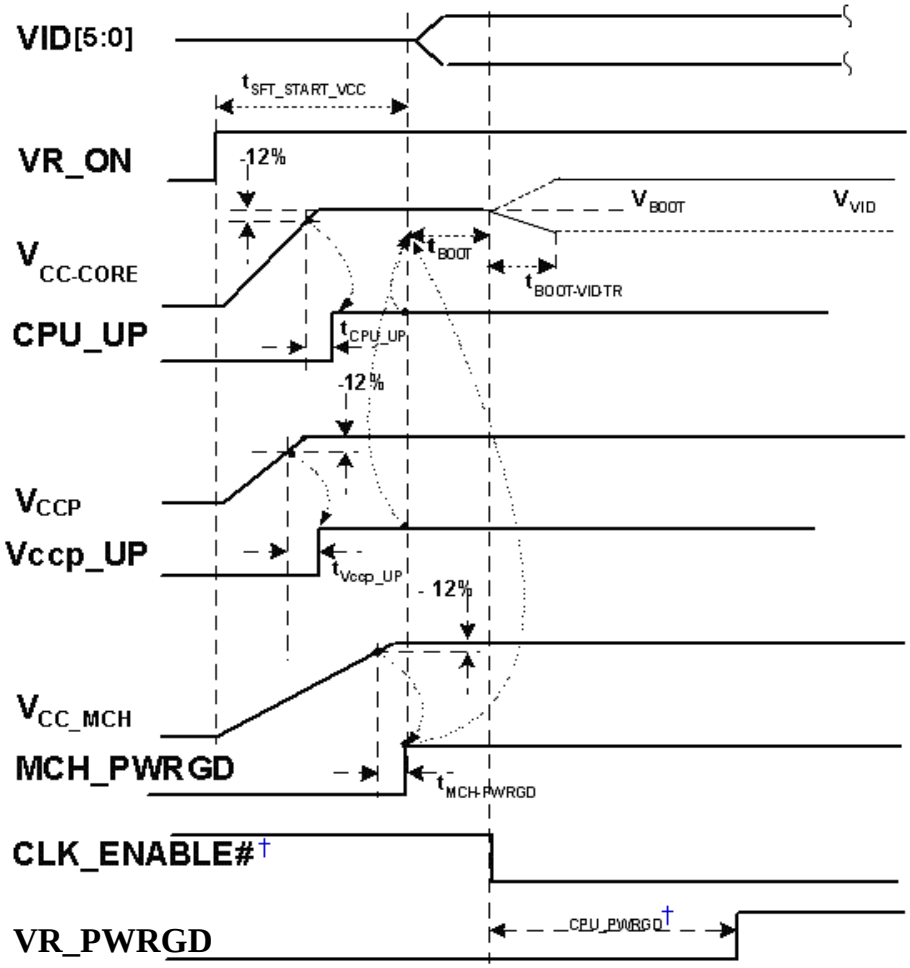
Table 87. VID vs. V_{CC_CORE} Voltage

VID						V_{CC_CORE}	VID						V_{CC_CORE}
5	4	3	2	1		V	5	4	3	2	1		V
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

11.3.3 V_{CC_CORE} Power Sequencing

There is only one enable pin, VR_ON, used to enable the outputs of the voltage regulator. When VR_ON is low, all output voltage rails (V_{CC_CORE} and V_{CCP}) are driven to a 0 V state. When VR_ON is high, V_{CCP} and V_{CC_CORE} are ramp up at the same time.

Figure 128. Power On Sequencing Timing Diagram



† Desired, but not required feature of a processor voltage regulator compliant controller. When not implemented by the voltage regulator controller, both the CLK_ENABLE# and the $t_{CPU\text{-}PWRGD}$ timer must be implemented by platform control logic.

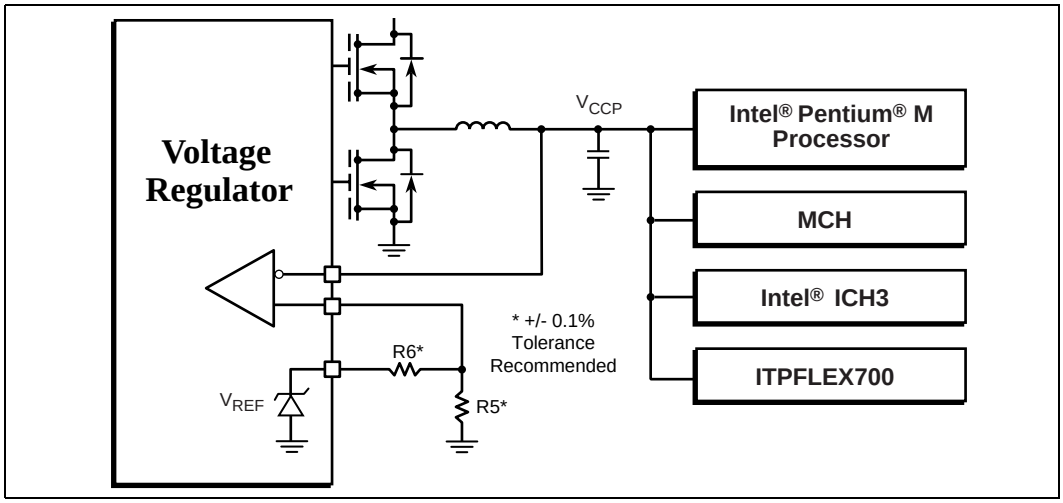
Figure 128 depicts a number of signals that may or may not be platform visible or used in an Intel® Pentium® M processor/Intel® E7501 chipset design. For more details on the relationships and timing requirements between VR_ON, output supply stabilization, and all power good signals.

11.3.4 V_{CCP} Output Requirements

The V_{CCP} output voltage rail provides power to the Intel Pentium M processor system bus rail for the Intel Pentium M processor, the Intel® E7501 MCH, the Intel ICH3-S, and ITP700FLEX debug port when it is used. For the ICH3-S, this rail is known as V_{CPU_IO}. The processor voltage

regulator may be programmed through an external resistor network. See Figure 129. VREF is used to set the highest output voltage in conjunction with the selection of R5 and R6 in the resistor network. Ensure R5 and R6 are precision resistors with +/- 0.1% tolerance.

Figure 129. V_{CCP} Block Diagram



11.3.5 Thermal Power Dissipation

Power dissipation has traditionally been a thermal/mechanical challenge for embedded system designers. The amount of current required from the processor power delivery circuit and the heat generated by processors has increased as processor frequencies go up and the silicon process geometry shrinks. The package of any integrated device may only dissipate so much heat into the surrounding environment. The temperature of a device, such as a processor power delivery circuit-switching transistor, is a balance of heat being generated by the device and its ability to shed heat either through radiation into the surrounding air or by conduction into the circuit board. Increased power may effectively raise the temperature of the processor power delivery circuits. Switching transistor die temperatures may exceed the recommended operating value when the heat cannot be removed from the package effectively.

As the current demands for higher frequency and performance processors increases, the amount of power dissipated (i.e., heat generated) in the processor power delivery circuit is starting to become of concern for Applied Computing system, thermal and electrical design engineers. The high input voltage, low duty factor inherent in power supply designs leads to increasing power dissipation losses in the output stage of the traditional buck regulator topology used in the industry today.

These losses may be attributed to three main areas of the processor power delivery circuit. The switching MOSFET dissipates a significant amount of power during switching of the top control MOSFET, power dissipation resulting from drain to source resistance (R_{DS-ON}) DC losses across the bottom synchronous MOSFET, and the power dissipation generated through the magnetic core and windings of the main power inductor.

There has been significant improvement in the switching MOSFET technology to lower gate charge of the control MOSFET allowing them to switch faster thus reducing switching losses. Improvements in lowering the $R_{DS(ON)}$ parametric of the synchronous MOSFET have resulted in reduced DC losses. The Direct Current Resistance (DCR) of the power inductor has been reduced, as well, to lower the amount of power dissipation in the circuit's magnetic.

These technology improvements by themselves are not sufficient to effectively remove the heat generated during the high current demand and tighter voltage regulation required by today's processors. There are several mechanisms for effectively removing heat from the package of these integrated devices. Some of the most common methods are listed below.

- Attaching a heat spreader or heat pipe to the package with a low thermal co-efficient bonding material.
- Adding and/or increasing the copper fill area attached to high current carrying leads.
- Adding or redirecting air flow to flow across the device.
- Utilize multiple devices in parallel, as allowed, to reduce package power dissipation.
- Utilizing newer/enhanced technology and devices to lower heat generation but with equal or better performance.

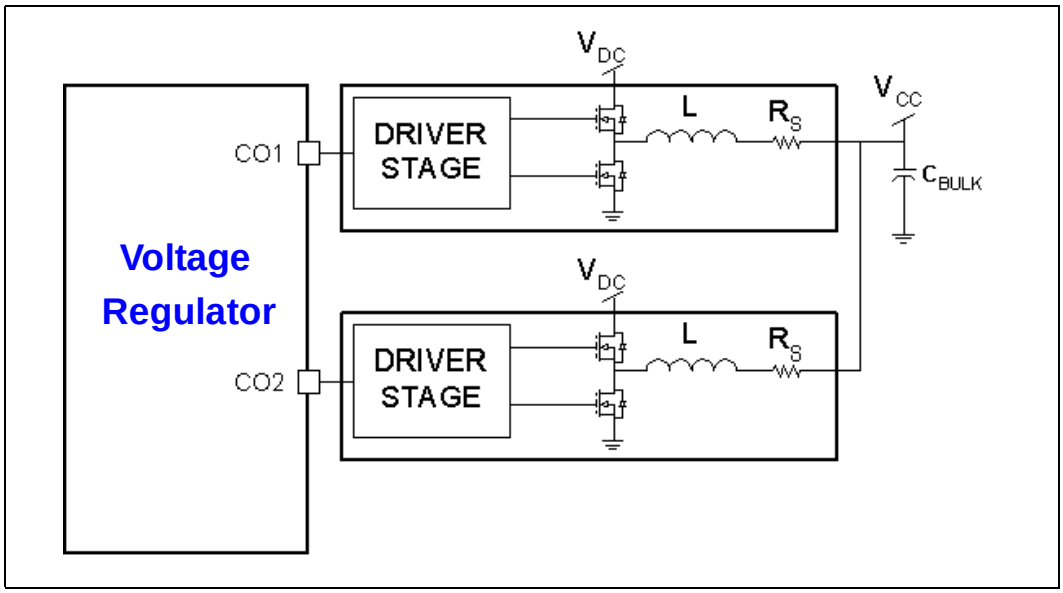
For the system designer, these options are not always available or economically feasible. The most effective method of thermal spreading and heat removal, from these devices, is to generate airflow across the package and add copper fill area to the current carrying leads of the package.

The processor power delivery topology may also be modified to improve the thermal spreading characteristic of the circuit and dramatically reduce the power dissipation requirements of the switching MOSFET and inductor. This topology referred to as multi-phase, provides an output stage of the processor regulator consisting of several smaller buck inductor phases that are summed together at the processor. Each phase may be designed to handle and source a much smaller current. This may reduce the size, quantity, and rating of the components needed in the design. This may also decrease the cost and PCB area needed for the total solution.

11.3.6 Voltage Regulator Topology

In a single-phase topology, the duty cycle of the Control (top) MOSFET is roughly the ratio of the output voltage and the input voltage. Due to the small ratio between V_{CC_CORE} and V_{DC}, the duty cycle of the Control MOSFET is very small. The main power loss in the Control MOSFET is therefore due to the transition or switching loss as it switches on and off. To minimize the transition loss in the Control MOSFET, its transition time must be minimized. This is usually accomplished with the use of a small-size MOSFET. Or similarly, the duty cycle of the Synchronous MOSFET is very large; hence, to minimize the DC loss of the Synchronous MOSFET, its R_{DS-ON} must be small. This is usually accomplished with the use of a large-size MOSFET or several small-size MOSFETs connected in parallel, but this solution usually leads to shoot-through current as it is quite difficult to minimize the effect of the Gate-Glitch phenomenon in the Synchronous MOSFET due to C_{GD} charge coupling effect. Therefore, it is necessary to go to multi-phase topology. In a multi-phase topology, the output load current is sourced from multiple sources or output stages. The term multi-phase implies that the phases or stages are out of phase with respect to each other. For example, in a dual-phase topology, the stages are exactly 180° output of phase.

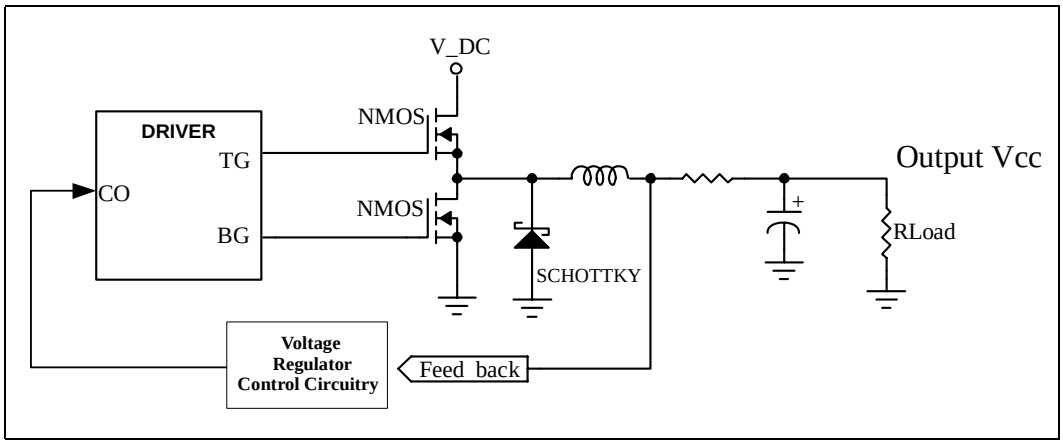
Figure 130. Voltage Regulator Multi-Phase Topology Example



11.3.7 Voltage Regulator Design Recommendations

When laying out the processor power delivery circuit using a traditional Buck Voltage Regulator on a printed circuit board, the following example should be followed (Figure 131).

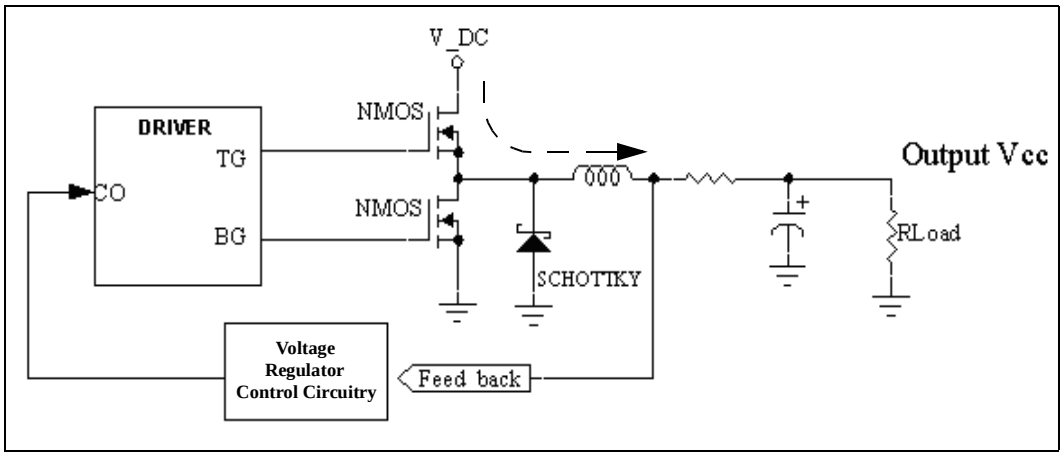
Figure 131. Buck Voltage Regulator Example



11.3.7.1 High Current Path, Top MOSFET Turned ON

The dashed/arrow line in Figure 132 indicates the high current path when the top MOSFET is ON. Current flows from the V_DC power source, through the top MOSFET (there may be more than one of these), through the inductor and sense resistor and finally through the processor, R_{Load}, to ground. The components and current paths shown must be able to not only carry the high current through the processor, but the power source and ground must also be adequate.

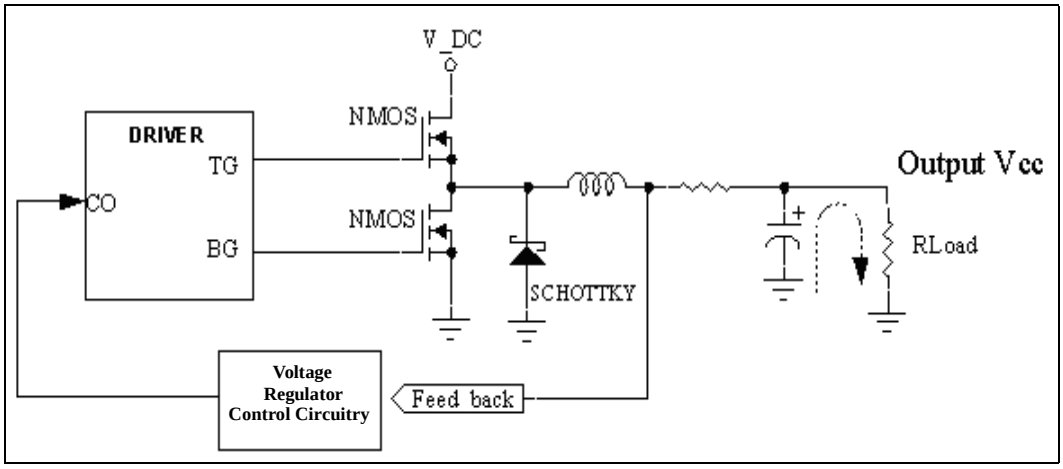
Figure 132. High Current Path With Top MOSFET Turned ON



11.3.7.2 High Current Paths During Abrupt Load Current Changes

During abrupt changes in the load current, the bulk and decoupling capacitors must supply current for the brief period before the regulator circuit may respond. The dashed/arrow line in Figure 133 illustrates this current path. Stray inductance and resistance become a major concern and when they are not minimized, they may compromise the effectiveness of the capacitors. Bulk capacitors for Vcc should be located at the highest current density points. These high-density points are located along the shortest route between the processor core and the sense resistor. Using short, fat traces or planes may minimize both stray inductance and resistance.

Figure 133. High Current Path During Abrupt Load Current Changes

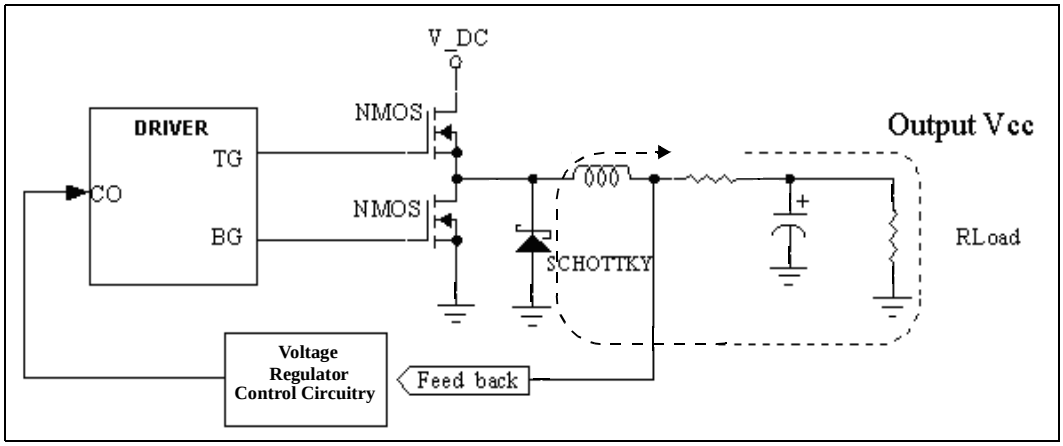


11.3.7.3 High Current Paths During Switching Dead Time

When the top MOSFET turns OFF and before the bottom MOSFET (again there may be more than one of these) is turned ON, the pattern of current flow changes. The inductor is no longer being supplied current through the top MOSFET starts to collapse its magnetic field. The inductor literally becomes a generator, at this point. The dashed line in Figure 134 shows the current path during the time that both top and bottom MOSFETs are OFF, also known as Dead Time. During

Dead Time there is a high current flow through the inductor, processor, ground, and the Schottky diode. The diode and its traces must be laid out in such as to minimize both stray inductance and resistance with short, fat traces or planes.

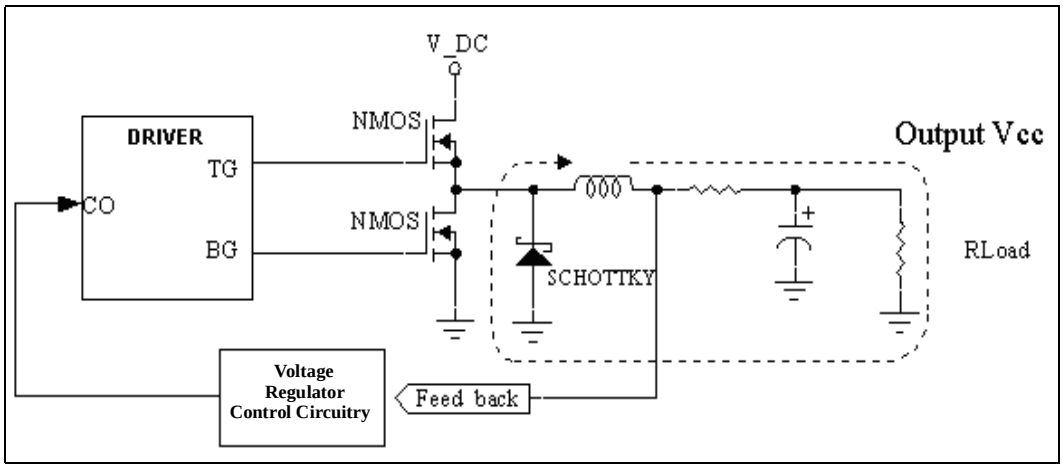
Figure 134. High Current Path With Top and Bottom MOSFETs Turned Off (Dead Time)



11.3.7.4 High Current Path With Bottom MOSFET(s) Turned ON

A few nanoseconds after the top MOSFET is turned OFF, the bottom MOSFET(s) is turned ON. The high current path now switches from the Schottky diode to the bottom MOSFET(s), the current path shown by the dashed/arrow line in Figure 135. Minimize stray inductance and resistance with short, fat traces or planes.

Figure 135. High Current Path With Bottom MOSFET(s) Turned ON



11.3.7.5 General Layout Recommendations

All or the components in the high current paths dissipate some power (i.e., they get warm when current runs through them). To minimize temperature rise and facilitate thermal spreading, large copper fill areas connecting the high current components is imperative. For example, the MOSFET manufacturers recommend that each MOSFET be mounted on one square inch of two-ounce copper. While this may not be possible in all environments, this recommendation serves to illustrate the importance of thermal considerations in the switching regulator layout.

- Bulk capacitors for V_{CC} need three vias per pad when vias are not shared. Clusters of bulk and bypass capacitors may be clustered along the high current paths between the sense resistor and the processor. Clusters may have copper fill areas between capacitors. This provides additional opportunities for vias – don't stop at three.
- Some controllers sense the load on Vcc by monitoring the voltage drop across the sense resistor with a Kelvin connection. The two feedback traces do not handle a high current, but must be of equal lengths to get an accurate load measurement. Connect the feedback signal traces as close as possible to both ends of the sense resistor. While the feedback traces do not handle high current, they are high impedance and susceptible to interference from electrical and magnet noise. Avoid routing these traces near the power inductor and avoid routing through vias.
- The sense resistor is to be placed as close to the inductor as possible, followed by the first two bulk capacitors.
- The lead frame in the power MOSFETs is used to dissipate heat. To do this each of the power MOSFETs requires one square inch of copper.
- Avoid ground loops as they pick up noise. Use star or single point grounding. The source of the lower (Synchronous bottom MOSFET) is an ideal point where the input and output ground planes may be connected.
- Keep the inductor-switching node small by placing the output inductor, switching top MOSFET and synchronous bottom MOSFETs close together on the same copper fill.
- The MOSFET enable/gate traces to the driver must be as short (less than one inch), straight, and wide as possible (20 to 25 mils). Ideally, the driver has to be placed right next to the MOSFETs. Circuits using multiple top or bottom MOSFETs need to have the gate traces serpentined so the all the traces going to the top MOSFETs Gates and most especially the bottom MOSFETs gates are the same length.
- Use the bulk capacitors for the voltage regulator and use multiple layer traces with heavy copper to keep the parasitic resistance low. Use a minimum of three vias per connection on each bulk capacitor.
- Place the top MOSFET drains as close to the VDC-input capacitors as possible.
- The sense resistor has to be wide enough to carry the full load current. A minimum of 1 via per Amp to the Vcc plane should be used. Use more when space permits.
- Use solid 2-oz. copper fill under drain and source connections of the top and bottom MOSFETs.
- The voltage regulator is usually left to the last moment. Often the allocated area is too small, a narrow strip and the location poor. These factors combine so that the design flow, described above usually cannot be followed.
- General Rule: Copper fill is good. Fill the PCB with metal. There should be no large areas of the board without metal. Increase the width of the grounds, V_{CC} and other power rails to fill any blank spots. Large metal fill areas allow the voltage regulator to improve its heat radiation thus run cooler. Large copper fill areas have other benefits too, including reducing series resistance and inductance, capturing and dissipating RF energy by allowing eddy currents to flow.

11.3.8 Processor Decoupling Recommendations

Intel recommends proper design and layout of the system board bulk and high frequency decoupling capacitor solution to meet the transient tolerance at the processor package balls. To meet the transient response of the processor, it is necessary to properly place bulk and high frequency capacitors close to the processor power and ground pins.

11.3.8.1 Transient Response

The inductance of the motherboard power planes slows the ability of the voltage regulator to respond quickly to a current transient. Decoupling a power plane may be broken into several independent parts. The closer to the load the capacitor is placed, the more series inductance is bypassed. By bypassing the inductance of leads, power planes, etc., less capacitance is required. However, areas closer to the load have less room for capacitor placement and therefore, tradeoffs must be made.

The processor causes very large switching transients. These sharp surges of current occur at the transition between low power states and the normal operating states. The system designer must provide adequate high frequency decoupling to manage the highest frequency components of the current transients. Larger bulk storage capacitors supply current during longer lasting changes in current demand.

All of this power bypassing is required due to the relatively slow speed at which a DC-to-DC converter may respond. A typical voltage converter has a reaction time on the order of 1 to 100 µs while the processor's current steps may be at shorter than 1 ns. High Frequency decoupling is typically done with ceramic capacitors with a very low Equivalent Series Resistance (ESR). Because of their low ESR, these capacitors may act very quickly to supply current at the beginning of a transient event. However, because the ceramic capacitors are small, (i.e., they may only store a small amount of charge, thus Bulk capacitors are needed too). Bulk capacitors are typically polarized with high capacitance values and unfortunately higher Equivalent Series Inductance (ESL) and ESR. The higher ESL and ESR of the Bulk capacitor limit how quickly it may respond to a transient event. The Bulk and high frequency capacitors working together may supply the charge needed to stay in regulator before the regulator may react during a transient.

11.3.8.2 High/Mid Frequency and Bulk Decoupling

System motherboards should include high and mid frequency and bulk decoupling capacitors as close to the socket power and ground pins as possible. Decoupling should be arranged such that the lowest ESL devices (0612 reverse geometry) are closest to the processor power pins followed by the 1206 devices (when used), and finally, bulk electrolytics (organic covered tantalum or aluminum covered capacitors). System motherboards should also include bulk decoupling capacitors as close to the processor socket power and ground pins as possible. Table 88 lists three recommended decoupling solutions for V_{CC_CORE}, while Table 89 list the recommended decoupling solutions for the V_{CCP} supply rails.

11.3.8.3 Processor Core Voltage Plane and Decoupling

Due to the high current (up to 32 A) requirements of the processor core voltage, the V_{CC_CORE} is fed from the VRM by means of multiple power planes that provide both low resistance and low inductance paths between the voltage regulator, decoupling capacitors, and processor V_{CC_CORE} pins. To meet the V_{CC_CORE} transient tolerance specifications for the worst-case the maximum ESR of the decoupling solution should be equal to or less than 3 mΩ.

Table 88 lists the decoupling solution recommended by Intel for the Intel® Pentium® M processor's VCC_CORE voltage rail. The decoupling solutions is optimized to meet the voltage regulator dynamic tolerance specifications for a load line of 3 mΩ.

Table 88. V_{CC_CORE} Decoupling Guidelines

Description	Cap (µF)	ESR (mΩ)	ESL (nH)
Low Frequency Decoupling (Polymer Covered Tantalum – POSCAP, Neocap, KO Cap)	12 x 150 µF	42 mΩ (typ) / 12	2.5 nH / 12
Mid Frequency Decoupling (0612 MLCC, >= X5R)	15 x 2.2 µF	5 mΩ (typ) / 15	0.2 nH / 15

11.3.8.4 Processor Side Bus Voltage Plane Decoupling

The 400 MHz high frequency operation of the Intel Pentium M processor side bus requires careful attention to the design of the power delivery for the processor's V_{CCP} (1.05 V). Table 89 summarizes the processor's V_{CCP} (1.05 V) voltage rail decoupling requirements.

- Two 150-µF POSCAPs with an ESR of 42 mΩ may be used for bulk decoupling. One capacitor should be placed next to the Intel Pentium M processor socket and one capacitor in close proximity to the Intel® E7501 MCH package. It is recommended to place each POSCAP on the secondary side of the motherboard to minimize inductance.
- Ten 0.1-µF X7R capacitors in a 0603 form factor should be placed on the secondary side of the motherboard under the Intel Pentium M processor socket cavity next to the V_{CCP} pins of the Intel Pentium M processor. Four capacitors should be spread out near the data and address signal sides and two capacitors on the signal side of the Intel Pentium M processor socket's pin-map.
- For MCH PSB decoupling, see Section 11.4.2.

The Intel Pentium M processor's and Intel E7501 MCH's V_{CCP} pins should be shorted with a wide V_{CCP} plane, preferably on the secondary side such that it may extend across the whole 'shadow' of the Intel Pentium M processor signals routed between the Intel Pentium M processor and Intel E7501 MCH. The 1.05 V voltage regulator feed point into the V_{CCP} plane should be roughly in between the Intel Pentium M processor and Intel E7501 MCH.

Table 89. V_{CCP} Decoupling Guidelines

Description	Cap (µF)	ESR (mΩ)	ESL (nH)	Notes
Low Frequency Bulk Decoupling (Polymer Covered Tantalum – POSCAP, Neocap, KO Cap)	2 x 150 µF	42 mΩ (typ) / 2	2.5 nH / 2	†
High Frequency Decoupling (0603 MLCC, >= X7R) Place next to the Intel Pentium M processor CPU.	10 x 0.1 µF	16 mΩ (typ) / 10	0.6 nH / 10	

† Place one capacitor close to the Intel Pentium M processor and one capacitor close to the Intel® E7501 MCH.

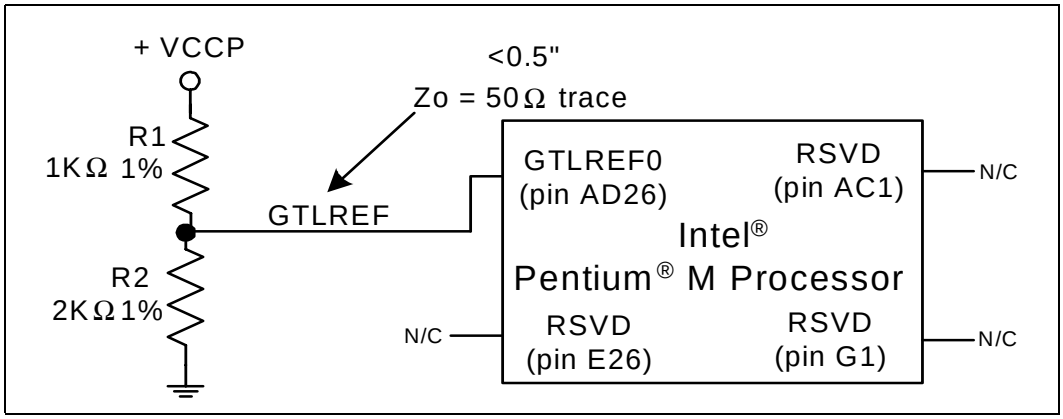
11.3.8.5 GTLREF Layout and Routing Recommendations

There is one AGTL+ reference voltage pin on the Intel Pentium M processor, GTLREF, which is used to set the reference voltage level for the AGTL+ signals (GTLREF). The reference voltage must be supplied to the GTLREF signal, pin AD26 of the Intel Pentium M processor pin-map. The voltage level that needs to be supplied to GTLREF must be equal to 2/3 * V_{CCP} ± 2%. The Intel® E7501 MCH also requires a reference voltage (MCH_GTLREF) to be supplied to its

HDVREF[3:0], HAVREF[1:0], HCCVREF pins. The GTLREF voltage divider for both the Intel® Pentium® M processor and MCH cannot be shared. Thus, both the processor and MCH must have their own locally generated GTLREF networks. Figure 136 shows the recommended topology for generating GTLREF for the Intel Pentium M processor using a R1 = 1 k ± 1% and R2 = 2 k ± 1% resistive divider.

Since the input buffer trip point is set by the 2/3* V_{CCP} on GTLREF and to allow tracking of V_{CCP} voltage fluctuations, **no** decoupling should be placed on the GTLREF pin. The node between R1 and R2 (GTLREF) should be connected to the GTLREF pin of the Intel Pentium M processor with a Zo = 50 trace shorter than 0.5 inches. Space any other switching signals away from GTLREF with a minimum separation of 25 mils. Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the Intel Pentium M processor system bus signals).

Figure 136. Intel® Pentium® M Processor GTLREF0 Voltage Divider Network



11.4 MCH Power Delivery Guidelines

The following guidelines are recommended for an optimal MCH power delivery. The main focus of these guidelines is to minimize chipset power noise and signal integrity problems. The guidelines are not intended to replace thorough system validation of products.

11.4.1 DDR_VTT (1.25 V) Decoupling

To reduce noise on the DDR termination voltage (1.25 V) around the MCH, four 0.1 µF capacitors per-channel are recommended. Evenly distribute placement of decoupling capacitors along the VTT plane around the MCH within one inch of the outer row of balls. Ceramic 0603 body type capacitors are recommended.

11.4.2 CPU_VCC (1.05 V Power Plane)

The Intel® E7501 chipset's CPU_VCC pins and the Processor's V_{CCP} pins are connected to the 1.05 V power plane. This voltage powers the GTL Processor System Bus.

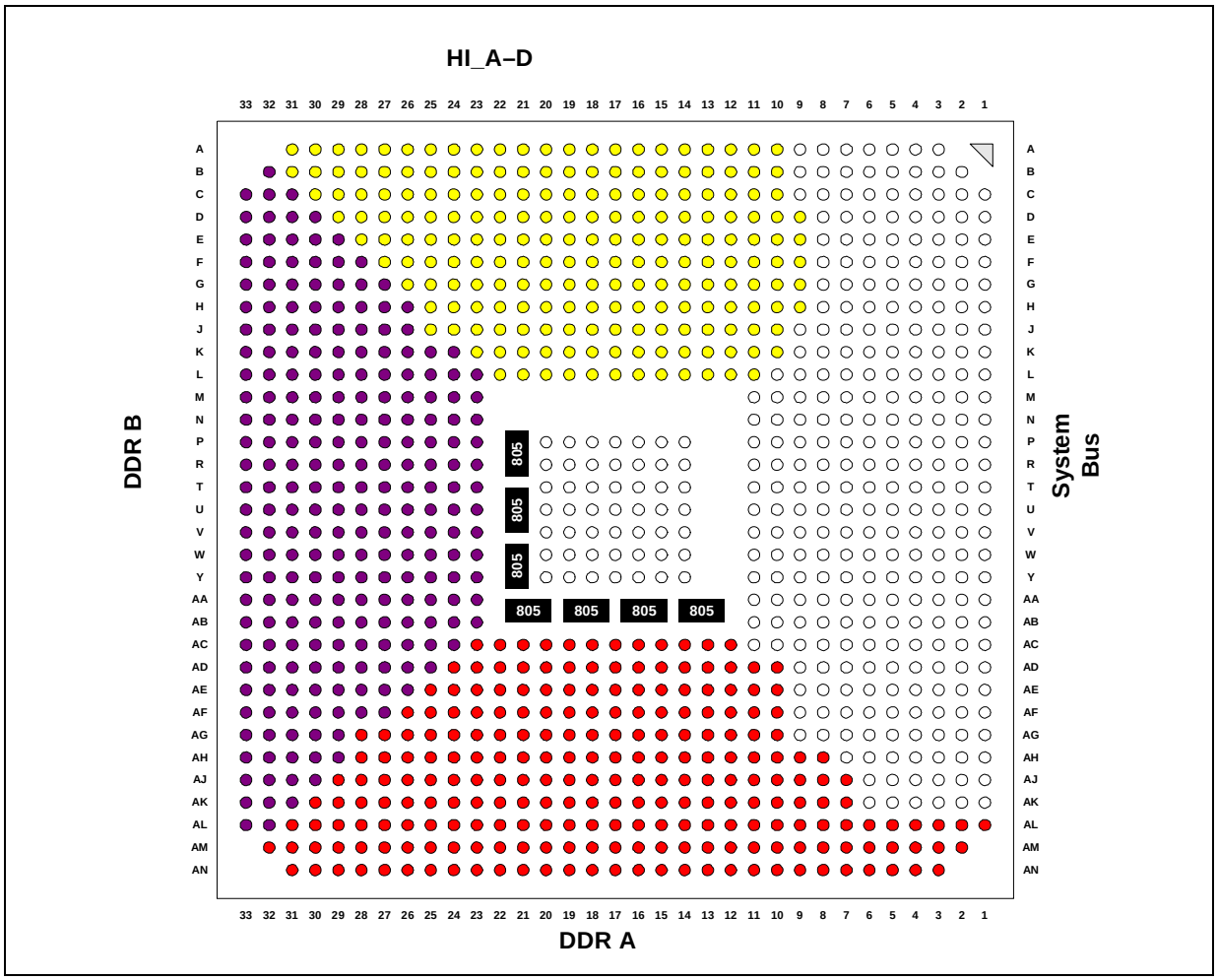
- Five, 0.1 µF capacitors are recommended (with 900 pH to 1.1 nH inductance) to be placed under the MCH for System Bus 1.05 V power plane decoupling.

- thirteen 0.1 µF capacitors are recommended (with 900 pH to 1.1 nH inductance) and should be evenly spaced for the System Bus. At least seven of the capacitors must be within 0.5 inch of the outer row of balls to the MCH.

11.4.3 DDR (2.5 V Power Plane)

Seven 0.1µF capacitors are recommended (with 900 pH to 1.1 nH inductance) to be placed under the MCH for DDR 2.5 V power plane decoupling (see Figure 137). The designer should evenly distribute placement of decoupling capacitors among the DDR interface signal field. It is recommended that the designer use ceramic capacitor 0402 or 0603 package type. In addition to the minimum decoupling capacitors under the MCH, for dual channel, the designer should place a maximum of twenty-one evenly spaced capacitors for both DDR channels, and at least ten must be within 0.5 inch of the outer row of balls to the MCH. For single channel, the designer should place a maximum of eleven evenly spaced capacitors for channel 'A', and at least five must be within 0.5 inch of the outer row of balls to the MCH.

Figure 137. MCH Decoupling (Backside View)



11.4.4 Hub Interface (1.2 V Power Plane)

Seven, 0.1 µF capacitors should be used to improve I/O power delivery to the MCH. These capacitors should be placed within 150 mils of the MCH package, adjacent to the rows that contain the Hub Interface. When the layout allows, wide metal fingers running on the ground side of the board may connect the VCC1_2 side of the capacitors to the VCC1_2 power pins. Similarly, when layout allows, metal fingers running on the VCC1_2 side of the board should connect the ground side of the capacitors to the VSS power pins.

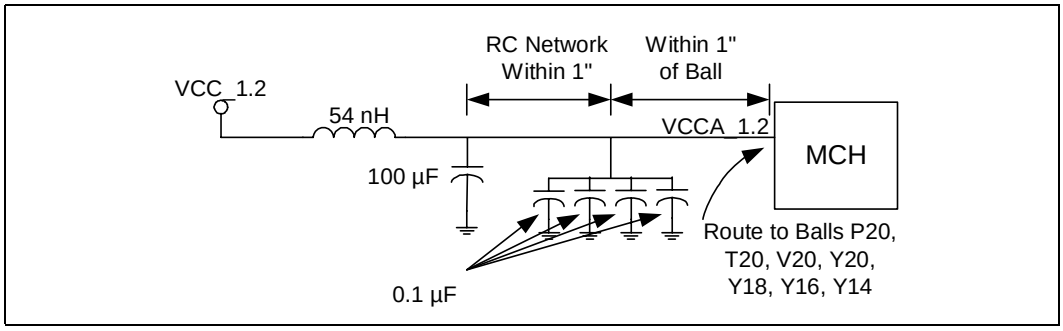
11.4.5 Intel® E7501 Chipset Filter Specifications (1.2 V Power Plane)

VCCA1_2 and VCCAHI1_2 are created by using a low pass filter on VCC1_2. VCCACPU is created by using a low pass filter on CPU_VCC. The MCH has internal analog PLL clock generators, that require quiet power supplies for minimum jitter. Jitter is detrimental to a system; it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency).

When designing the VCCA1_2 filter (Figure 138), follow these guidelines:

- One 54 nH Inductor close to the edge of the package (within 1 inch of the die).
- One 100 µF or 150 µF LF capacitor close to the edge of the package.
- Minimum of two (four preferred) Low ESL HF capacitors, 0.22 µF or 0.1 µF, on the backside of the motherboard under the die.
- Route the VCCA1_2 trace 1 inch, 35 mils wide with 15 mils spacing on three signal layers of the motherboard; connect to VCCA1_2 island on signal layers directly under the MCH core.

Figure 138. Filter Topology for VCCA1_2 (DDR Interface)



When designing the VCCA1_2 and VCCACPU filters (Figure 139 and Figure 140), follow these guidelines:

- One 100 nH Inductor close to the edge of the package (within one inch of the die).
- One 100 µF or 150 µF LF capacitor close to the edge of the package.
- Minimum of one Low ESL HF capacitor, 0.1 µF on the motherboard backside, under the die.

Figure 139. Filter Topology for VCCAHI1_2 (Hub Interface)

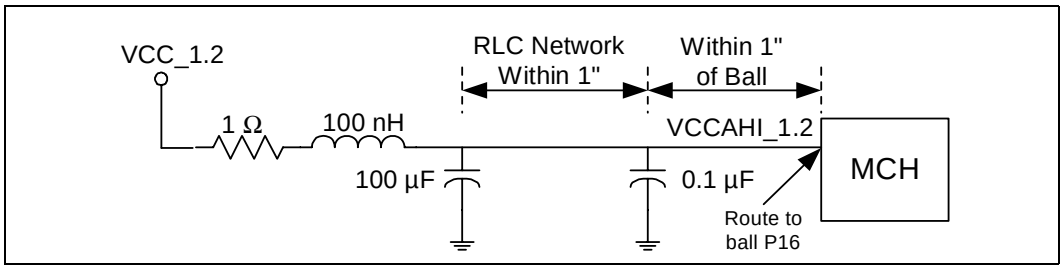
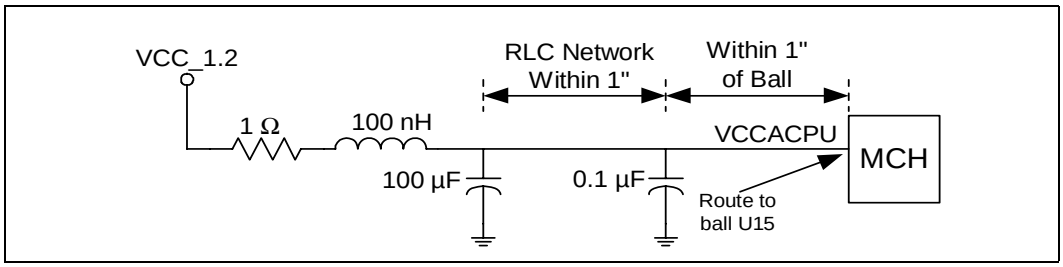


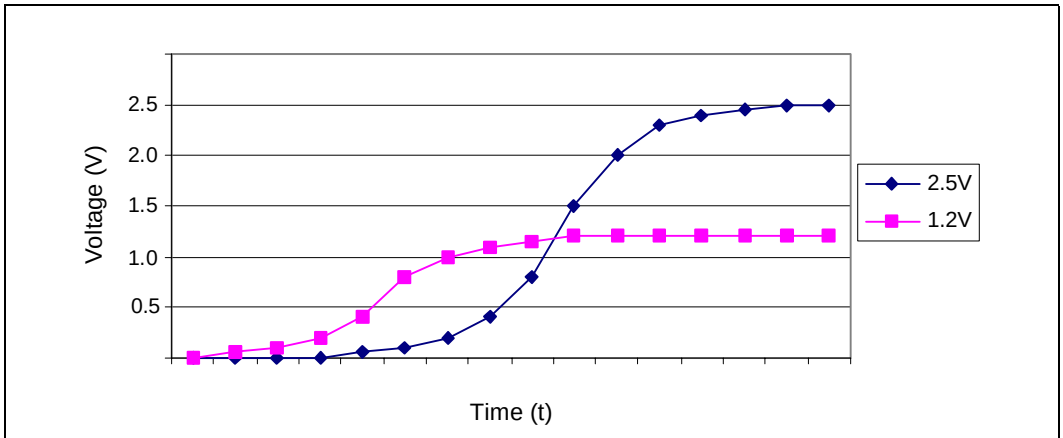
Figure 140. Filter Topology for VCCACPU1_2 (E7501 System Bus)



11.4.6 MCH Power Sequencing Requirement

The MCH has only one power sequencing requirement. The MCH requires that 1.2 V rises with or before 2.5 V to avoid electrical overstress of oxide layers and possible component damage. This means that at any point during system power up, the 2.5 V power plane voltage must not be higher than the 1.2 V power plane voltage until the 1.2 V voltage is within 1.2 V regulation. This is depicted in Figure 141. Notice that at no point before 1.2 V is ramped does the 2.5 V plane exceed the 1.2 V plane's value.

Figure 141. Power Sequencing Requirement for MCH

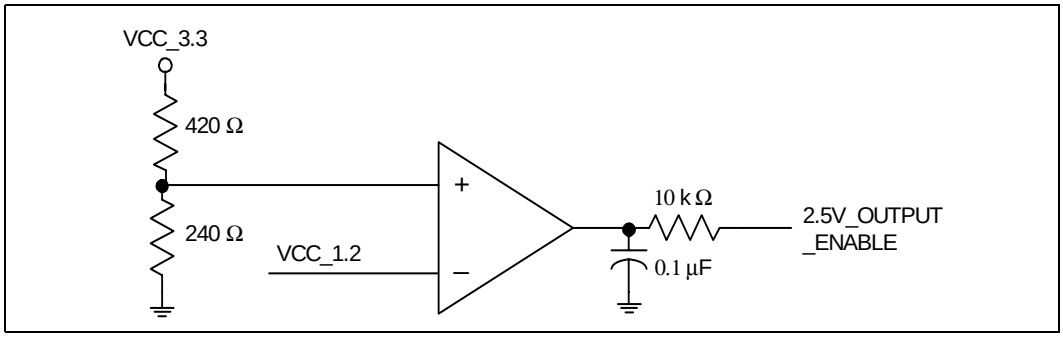


NOTE: This graph does not represent specific values or requirements on data/time frames.

A possible solution to safeguard against 2.5 V coming up before 1.2 V, is to tie the power good signal of the 1.2 V regulator to the output enable pin of the 2.5 V voltage regulator.

When the same voltage regulator is used to derive both 1.2 V and 2.5 V, then other logic must be used. A solution is to use a comparator to 1.2 V, and connect the output of the comparator to the output enable signal of the 2.5 V regulator. Figure 142 shows this implementation.

Figure 142. Sample 2.5 V Output Enable Control Logic



11.5 Intel® ICH3-S Power Delivery Guidelines

11.5.1 1.8 V/3.3 V Power Sequencing

The ICH3-S has two pairs of associated 1.8 V and 3.3 V supplies. These are {VCC1_8, VCC3_3} and {VCCSus1_8, VCCSus3_3}. **The difference between the two associated supplies must never be greater than 2.0 V**. The 1.8 V supply may come up before the 3.3 V supply without violating this rule (though this generally does not occur because the 1.8 V supply is typically derived from the 3.3 V supply with a linear regulator). One serious consequence of violation of this 'Two Volt Rule' is electrical overstress of oxide layers, resulting in component damage.

The majority of the ICH3-S I/O buffers are driven by the 3.3 V supplies but are controlled by logic powered by the 1.8 V supplies. Therefore, another consequence of faulty power sequencing arises when the 3.3 V supply comes up first. In this case, the I/O buffers may be in an undefined state until the 1.8 V logic is powered up. Some signals that are defined as 'Input-only' actually have output buffers that are normally disabled, and the Intel ICH3-S may unexpectedly drive these signals when the 3.3 V supply is active while the 1.8 V supply is not.

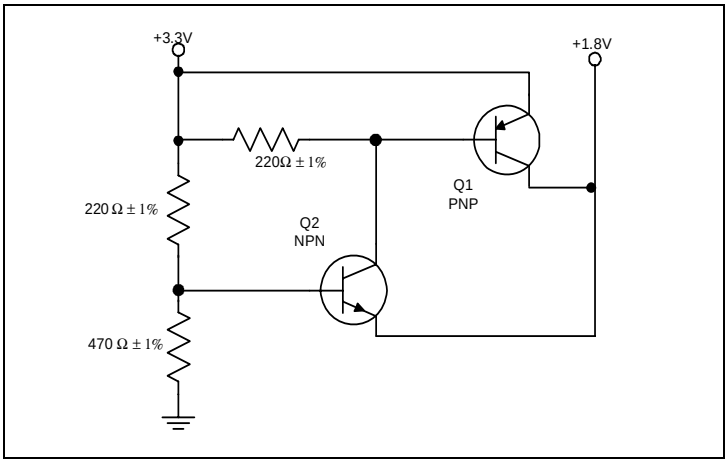
Note: These power sequencing circuits require that a linear regulator derive the ICH3-S 1.8 V power rail. These circuits are all designed with the assumption that 3.3 V is derived by the system power supply and that a 1.8 V linear regulator is used. Such circuitry is not needed if the voltage regulator ensures the Two-Volt Rule.

Figure 143 is an example of power-on sequencing circuit that ensures the Two Volt Rule is obeyed. This circuit uses an NPN (Q2) and a PNP (Q1) transistor to ensure the 1.8 V supply tracks the 3.3 V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.8 V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8 V plane, current may not flow from the 3.3 V supply into 1.8 V plane when the 1.8 V plane reaches 1.8 V.

Note: It is recommended to have a PNP transistor rated accordingly to handle the thermal and current needs to sustain the 1.8 V rail if the 1.8 V supply comes up slow or not at all (i.e., platform held in reset). The current and thermal requirements of the PNP transistor is platform dependant.

It is important to use 1% resistors for precise operating conditions in Figure 143 to ensure the NPN doesn't overheat (junction temperature exceeds 125° C). Overheating could overdrive the 1.8 V rail as high as 2 V.

Figure 143. Example 1.8 V/3.3 V Power Sequencing Circuit



When analyzing systems that may be 'marginally compliant' to the Two Volt Rule, attention must be paid to the behavior of the Intel ICH3-S's RSMRST# and PWROK signals because they control internal isolation logic between the various power planes:

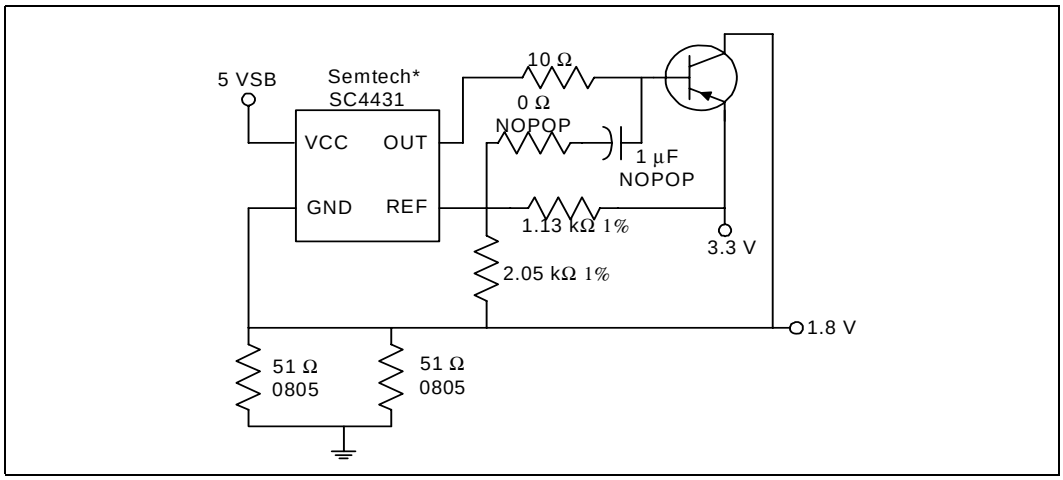
- RSMRST# controls isolation between the RTC well and the resume wells.
- PWROK controls isolation between the resume wells and main wells.

If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

The circuit in Figure 144 may, under high temperature and parameter corner conditions, inject charge onto the 1.8 V rail at steady state. The circuit in Figure 143 does not have this characteristic; it is more susceptible to layout variations and should be fully analyzed and tested to make sure that the implementation meets the 2 V specification. When choosing between the two circuits a designer should understand the trade-offs with respect to their linear regulator design and application.

The Semtech SC4431 monitors the difference between the reference pin (from 3.3 V) and the ground pin (1.8 V). The SC4431 turns on its output when the difference between 1.8 V and 3.3 V is over 1.9 V. Connecting the SC4431 ground pin to 1.8 V requires a series resistor from 1.8 V to ground to complete the current path from the SC4431 VCC (5 VSB) to system ground. The series resistor must be able to dissipate 0.25 W. This may be achieved using a 25 Ω resistor in a 1206 package, or two 51 Ω resistors in 0805 packages. The 1.8 V rail should be able to sink the current from the SC4431 and the 1.13 kΩ / 2.05 kΩ divider.

Figure 144. Another Example 1.8 V/3.3 V Power Sequencing Circuit

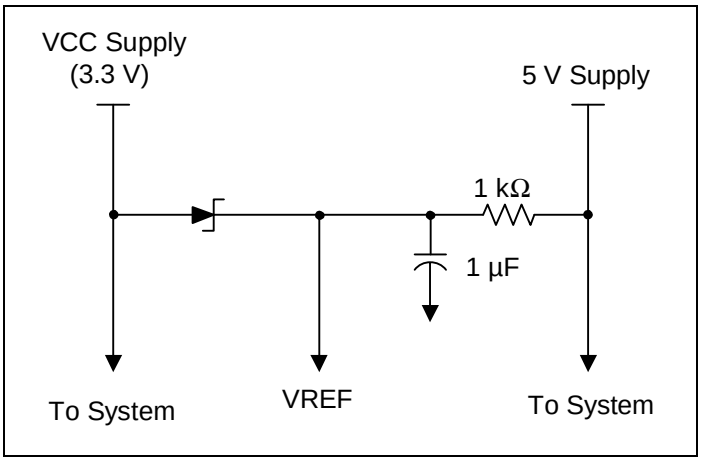


11.5.2 3.3V / V5REF Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the Intel ICH3-S. V5REF must be powered up before VCC3_3, or be no less than 0.7 V less than VCC3_3. Thus, VCC3_3 must never be more than 0.7 V higher than V5REF. Also, V5REF must power down after VCC3_3, or before VCC3_3 within 0.7 V. The rule must be followed in order to ensure the safety of the Intel ICH3-S. When the rule is violated, internal diodes may attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 145 shows a sample implementation of how to satisfy the V5REF/3.3 V sequencing rule.

This rule also applies to the standby rails, but in most platforms, the VCCSUS3_3 rail is derived from the VCCSUS5 rail and therefore, the VCCSUS3_3 rail may always come up after the VCCSUS5 rail. As a result, V5REF_SUS may always be powered up before VCCSUS3_3. In platforms that do not derive the VCCSUS3_3 rail from the VCCSUS5 rail, this rule must be enforced on the platform.

Figure 145. Example 3.3 V/V5REF Sequencing Circuitry



11.5.3 Intel® ICH3-S Power Rails

The Intel ICH3-S refers to its standby rails as suspend. Table 90 lists the nomenclature.

Table 90. Intel® ICH3-S Power Rail Terminology

Platform Terminology	Intel® ICH3-S Terminology
5 V Standby	5 V Suspend
3.3 V Standby	3.3 V Suspend
1.8 V Standby	1.8 V Suspend

11.5.4 Intel® ICH3-S Decoupling Recommendations

The Intel ICH3-S is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the decoupling capacitors specified in Table 91 to ensure that the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible (200 mils nominal). It is recommended that for prototype board designs, the designer include pads for extra power plane decoupling capacitors.

Table 91. Intel® ICH3-S Decoupling Recommendations (Sheet 1 of 2)

Power	Decoupling Requirements	Decoupling Placement
V_CPU_IO	Use **one** 0.1 µF decoupling capacitor.	Locate within 100 mils of the Intel® ICH3-S processor interface balls.
VCCRTC	Use **one** 1.0 µF decoupling capacitor. See Figure 116 for the External Circuitry.	Locate within 100 mils of the VCCRTC interface pin (pin AB6).
VCC_3.3	Requires **six** 0.1 µF decoupling capacitors.	Distribute around the Intel ICH3-S package sides within 100 mils of the package balls: • Top near AUX/PCI • Left across the PCI and LPC • Bottom near IDE • Right near GPIO[43]
VCCSUS_3.3	Requires **two** 0.1 µF decoupling capacitors.	• Place one capacitor on the top side within 200 mils of the USB center. • Place one capacitor on the bottom side near the VCCSUS_3.3 supply.
VCC_1.8	Requires **four** 0.1 µF decoupling capacitors.	• Locate 2 capacitors distributed local to the Hub Interface, within 50 mils of the package Hub Interface balls. • Distribute the remaining capacitors on the left and bottom sides of the package for core delivery.

Table 91. Intel® ICH3-S Decoupling Recommendations (Sheet 2 of 2)

Power	Decoupling Requirements	Decoupling Placement
VCCSUS_1.8	Requires **one** 0.1 µF decoupling capacitor.	Locate within 200 mils of the Intel ICH3-S, Balls B23 and C23.
V5REF_SUS	Requires **one** 0.1 µF decoupling capacitor. V5REF_SUS is the reference voltage for some 5 V tolerant inputs in the Intel ICH3-S (USB data and over current signals). VCCSUS_3.3 must never exceed 0.7 V higher than V5REF_SUS. For most platforms, this power sequencing is not an issue as VCCSUS_3.3 is derived from V5REF_SUS.	
V5_REF	Requires **one** 0.1 µF decoupling capacitor. V5_REF is the reference voltage for most 5 V tolerant inputs in the Intel ICH3-S. Tie to pins V5REF[2:1]. V5REF must power up before or simultaneous to VCC_3.3. It must power down after or simultaneous to VCC_3.3.	

11.6 Intel® P64H2 Power Requirements

11.6.1 Intel® P64H2 Current Requirements

Table 92. Intel® P64H2 Max Sustained Currents

Voltage at PCI/PCI-X Interface	Max Sustained Current
1.8 V at 33 MHz PCI (both segments)	1970 mA
1.8 V at 66 MHz PCI/PCI-X (both segments)	2170 mA
1.8 V at 100 MHz PCI-X (both segments)	2550 mA
1.8 V at 133 MHz PCI-X (both segments)	2660 mA
3.3 V at 33 MHz PCI 6 loads (both segments)	930 mA
3.3 V at 66 MHz PCI 2 loads (both segments)	690 mA
3.3 V at 66 MHz PCI-X 4 loads (both segments)	1300 mA
3.3 V at 100 MHz PCI-X 2 loads (both segments)	1050 mA
3.3 V at 133 MHz PCI-X 1 load (both segments)	770 mA

For more information, refer to the *Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Thermal Design Guide*.

11.6.2 Intel® P64H2 Decoupling Requirements

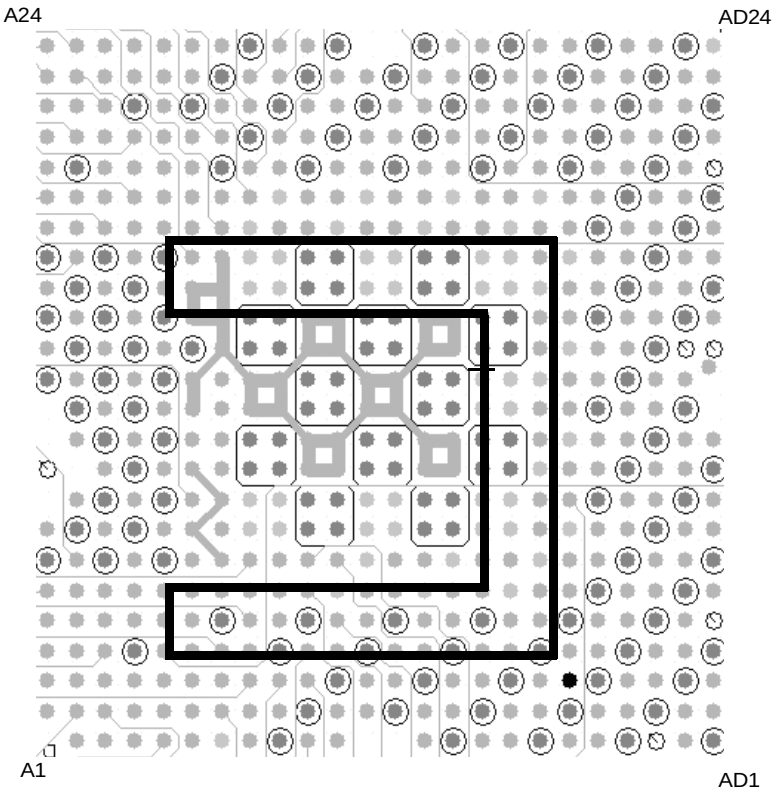
The Intel® P64H2 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in the table below to ensure the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible.

Table 93. Decoupling Capacitor Recommendations

Power Plane/Pins	Number of High-Frequency Decoupling Capacitors	High-Frequency Capacitor Values	Number of Bulk Decoupling Capacitors	Bulk Capacitor Values
1.8 V Core (VCC)	8	0.1 µF	2	4.7 µF (near Intel® P64H2)
1.8 V Hub Interface 2.0 (VCC_1.8)	2	1.0 µF	1	100 µF (near regulator)
3.3 V PCI/PCI-X (VCC_3.3)	20†	0.1 µF	2	4.7 µF (near Intel P64H2)
	6	1.0 µF	1	100 µF (near regulator)

† In the case of the twenty 0.1 µF decoupling capacitors for the Vcc3.3V plane, it is recommended that at least five of these capacitors be placed near the die on the back of the board between ground and the VCC-PCI vias, as shown in Figure 146. This is not a strict requirement, but is recommended to reduce the power resonance frequency at 66 Hz.

Figure 146. Intel® P64H2 3.3 V PCI/PCI-X (VCC_3.3) Capacitor Placement on Backside



NOTE: The outlined area in the figure is the 3.3 V plane. Place at least five 0.1 µF capacitors in this area.

11.6.3 PCIRST# Implementation

PCI-X requires a 100 ms delay from valid power (PWRGD) to reset deassertion (PCIRST#). The system design must ensure this requirement is met.

The Intel® P64H2 reset must be deasserted within 60 ns of the MCH reset deassertion. Intel strongly recommends customers measure this timing relationship on their boards. Failure to meet this guideline may result in a system failing to boot.

11.6.4 Intel® P64H2 Power Sequencing Requirement

The 1.8 V voltage must be valid before the first CLK66 pulse is driven to the Intel P64H2. This may be ensured by gating the CK408 clocks using a power good signal from the 1.8 V regulator. If the first CLK66 pulse is driven before 1.8 V is valid, the Intel P64H2 PLL may fail to correctly lock.

The 1.8 V must drop with or before 3.3 V. This may be achieved by deriving 1.8 V from 3.3 V. When 1.8 V drops after 3.3 V, a noise spike on PCIRST# approaches V_{IH} minimum levels.

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12.1 Return Path

The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, or integrated circuits. The return path is based on electro-magnetic field effects. It is useful to think of the return path as the path of least impedance nearest the signal conductor. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths must be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, and then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance.

The following sets of return path rules apply to all designs:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near system bus signals.
- Do not allow signal layer changes that force the return path to make a reference plane change, even when it is from one ground layer to another ground layer.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not route over via anti-pads or socket anti-pads

When reference plane changes must be made:

- Change from a ground reference to a ground reference and place a via that connects the two planes as close as possible to the signal via. This also applies when making a change from VCC to VCC.
- For symmetric stripline, return path vias for both ground and VCC must be provided.
- Do not switch reference from VCC to ground or vice versa.

12.2 Decoupling Theory

The primary objective of the decoupling guidelines is to minimize the impact of return path discontinuities and to ensure that the I/O has adequate power decoupling. The worst-case return path discontinuity anticipated is for systems that use microstrip structures on the motherboard. When a motherboard uses symmetric stripline with VCC and ground references, then a discontinuity does not exist and additional decoupling is not necessary. When the motherboard routing references only a single reference plane (VCC or ground), then a return path discontinuity exists.

The inductance of the system due to cables and power planes slows the power supply's ability to respond quickly to a current transient. Decoupling a power plane may be broken into several independent parts. The closer to the load the capacitor is placed, the more inductance is bypassed. By bypassing the inductance of leads, power planes etc., less capacitance is required. However, closer to the load there is less room for capacitance. Therefore, trade-offs must be made.

12.2.1 Bulk Decoupling

Larger bulk storage components, such as electrolytic capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition.

Power bypassing is required due to the relatively slow speed at which a DC-to-DC converter may react. Bulk capacitance supplies energy from the time the high-frequency decoupling capacitors are drained, until the power supply may react to the demand. More correctly, the bulk capacitors in the system slow the transient requirement seen by the power source to a rate it is able to supply, while the high-frequency capacitors slow the transient requirement seen by the bulk capacitors to a rate they may supply.

Maintaining voltage tolerance during changes in current requires high-density bulk capacitors with low Effective Series Resistance (ESR), and low Effective Series Inductance (ESL). Use thorough analysis when choosing these components.

12.2.2 High-Frequency Decoupling

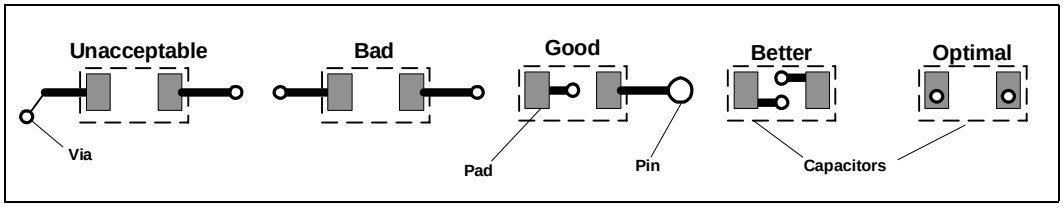
The system boards should include high-frequency capacitors as close to the load power and ground pins as possible. Place as many capacitors as possible in the load cut out area.

In addition, high-frequency decoupling may be required for signal integrity. For systems using microstrip configurations, a return path discontinuity may exist due to the baseboard traces having only one reference plane.

Place high-frequency decoupling as close to the power pins of the load as physically possible. Use both sides of the board when necessary for placing load to achieve the optimum proximity to the power pins. This is vital because the inductance of the board's metal plane layers could cancel the usefulness of these low inductance components.

Shorten the path from the capacitor pads to the pins the capacitor is decoupling. When possible, place the vias connecting to the planes within the pad of the capacitor. When this is not possible, keep the traces as short and wide as is feasible. Possibly one or both ends of the capacitor may be connected directly to the pins of the load without the use of a via. Figure 147 illustrates these concepts.

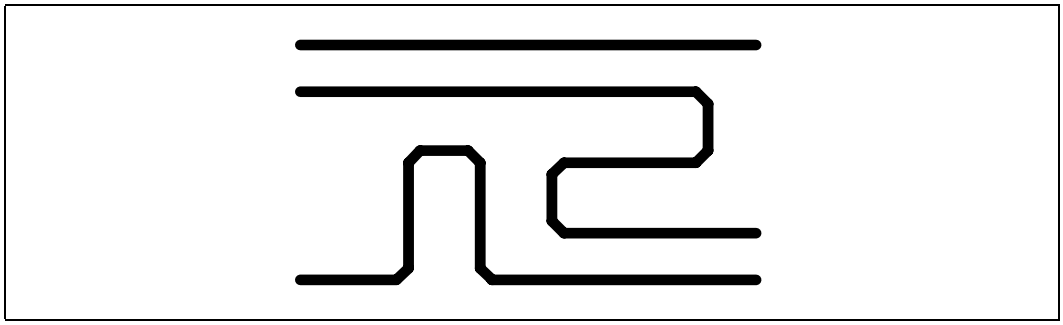
Figure 147. Proper Decoupling Capacitor Placement with Respect to Vias



12.3 Serpentine Routing

A serpentine net is a transmission line that is routed in such a manner that sections of the net double back and couple to other segments of the same net (see Figure 148).

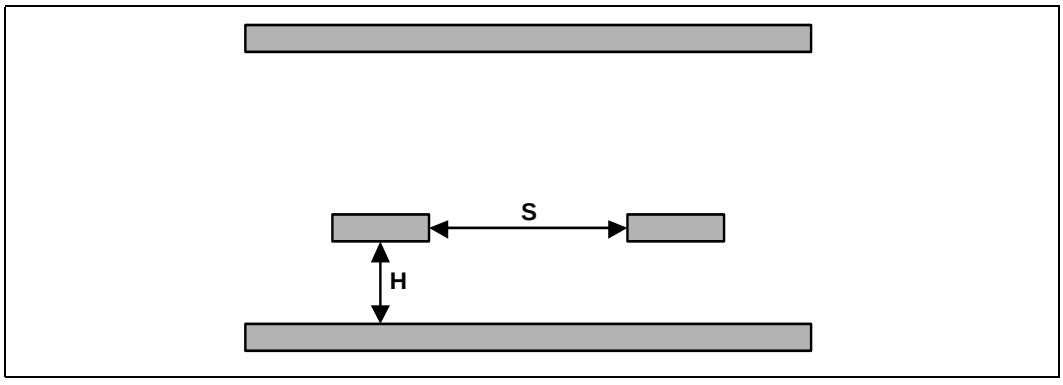
Figure 148. Serpentine Routing



Serpentining a transmission line is sometimes necessary to properly match lengths between nets. It is important to properly control the serpentine to avoid signal integrity and timing problems. The primary impact of a serpentined trace is an observed decrease in the flight time when compared to a straight trace of equal length. This decrease in the flight time is a result of the crosstalk between parallel sections of the serpentined net. As the signal travels down the transmission line, a component of the signal follows the transmission line and behaves as though it were a straight line with no serpentine. However, another portion of the energy propagates perpendicular to the parallel routed portions of the serpentined net via the mutual capacitance and mutual inductance. This creates an extra mode that arrives at the receiver significantly earlier than the other component of the signal. When the coupling between parallel sections is high, significant timing skew may occur when attempting to match trace lengths on a bus. Furthermore, when the coupling is very high, significant signal integrity problems may result.

Serpentine routing requirements are defined using two parameters, as depicted in Figure 149. Parameter ‘S’ is the distance between the two segments of the serpentined trace. Parameter ‘H’ is the distance between the signal and the referenced plane. The ratio is specified as S/H.

Figure 149. Serpentine Spacing-Spacing to Reference Plane Height Ratio



12.4 EMI Design Considerations

As microprocessor amperage and speeds increase, the ability to contain the corresponding electromagnetic radiation becomes more difficult. Frequencies generated by these processors may be in the low gigahertz (GHz) range, which may impact both the system design and the electromagnetic interference (EMI) test methodology.

This section is intended to provide electrical and mechanical design engineers with information that may aid in developing a platform that may meet government EMI regulations. Heatsink grounding, processor shielding, differential and spread spectrum clocking, and the test methodology impact to FCC Class B requirements are specifically discussed.

Designers should be aware that implementing all the recommendations in this guideline may not ensure compliance to EMI regulations. Rather, these guidelines may help to reduce the emissions from processors and motherboards and make chassis design easier.

12.4.1 Brief EMI Theory

Electromagnetic energy transfer may be viewed in four ways: radiated emissions, radiated susceptibility, conducted emissions, and conducted susceptibility. For system designers, reduction of radiated and conducted emissions is the way to achieve EMC compliance. Susceptibility is typically not a major concern in the server environment, although it may be more important in an industrial environment.

The main component of EMI is a radiated electromagnetic wave, which consists of both electric (E-fields), and magnetic (H-fields) waves traveling together and oriented perpendicular to one another. Although E- and H-fields are intimately tied together, they are generated by different sources. E-fields are created by voltage potentials, while H-fields are created by current flow. In a steady state environment (where voltage or current is unchanging), E- and H-fields are also static and of no concern to EMI. Changing voltages and currents are of concern since they contribute to EMI. When a dynamic E-field is present, then there must be a corresponding dynamic H-field, and vice versa. Motherboards with fast processors generate high-frequency E- and H-fields from currents and voltages present in the component silicon and signal traces.

Two methods exist for minimizing E- and H-field system emissions: prevention and containment. Prevention is achieved by implementing design techniques that minimize the ability of the motherboard to generate EMI fields. Containment is used in a chassis environment to contain radiated energy within the chassis. Careful consideration of board layout, trace routing, and grounding may significantly reduce a motherboard’s radiated emissions and make the chassis design easier.

12.4.2 EMI Regulations and Certifications

Original Equipment Manufacturers (OEMs) ensure EMC compliance by meeting EMI regulatory requirements. System designers must ensure that their computer systems do not exceed the emission limit standards set by applicable regulatory agencies. Regulatory requirements referenced in this document include:

- United States Federal Communication Commission (FCC) Part 15 Class B.
- International Electrotechnical Commission's International Special Committee on Radio Interference (CISPR) Publication 22 Class B limits.

The FCC rules require any OEM that sells an ‘off-the-shelf’ motherboard in the United States to pass an open chassis test. Open chassis testing is defined as removing the chassis cover (or top and two sides), and testing for EMI compliance (although permitted emission levels are allowed to be higher). Removing the cover greatly reduces the shielding provided by the chassis and increases the amount of EMI radiation. The purpose of this regulation is to ensure that system boards have reasonable emission levels since they are one of the main contributors to EMI.

12.5 EMI Design Considerations

The following sections describe design techniques that may be applied to minimize EMI emissions. Some techniques have been incorporated into Intel-enabled designs (differential clock drivers, selective clock gating, etc.), and some must be implemented by motherboard designers (trace routing, clocking schemes, etc.).

12.5.1 Spread Spectrum Clocking (SSC)

Spread Spectrum Clocking (SSC) is defined as continuously ramping (or modulating) the processor clock frequency over a predefined range (see Figure 150). SSC reduces radiated emissions by spreading the radiated energy over a wider frequency band (see Figure 151). Thus, instead of maintaining a constant system frequency, SSC modulates the clock frequency along a predetermined path (or modulating profile). Figure 150 shows an example of a predetermined modulation frequency. The modulation frequency is usually selected to be larger than 30 KHz (above the audio band), and small enough not to upset system timings (less than 0.8% of the clock frequency). SSC has been demonstrated to effectively reduce peak radiation levels, making EMC compliance easier to achieve.

To conserve the minimum period requirement for bus timing, the SSC clock is modulated between fnom and (1-δ)*fnom, where fnom is the nominal frequency for a constant frequency clock. The ‘δ’ specifies the total amount of spreading as a relative percentage of fnom. The modulation percentage is always a function of 1-δ and not 1+δ, as increasing the clock frequency above the rated speed of the processor may cause unpredictable operation.

Figure 150. Spread Spectrum Modulation Profile

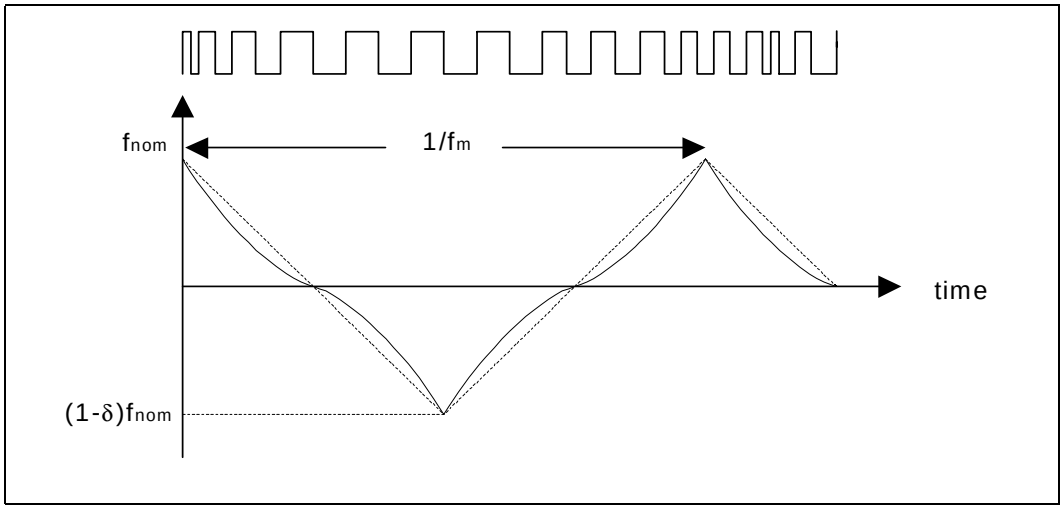
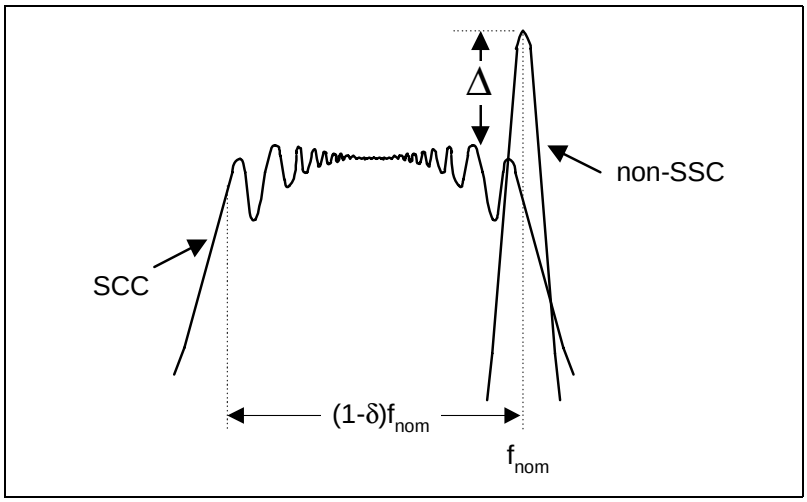


Figure 151. Impact of Spread Spectrum Clocking on Radiated Emissions

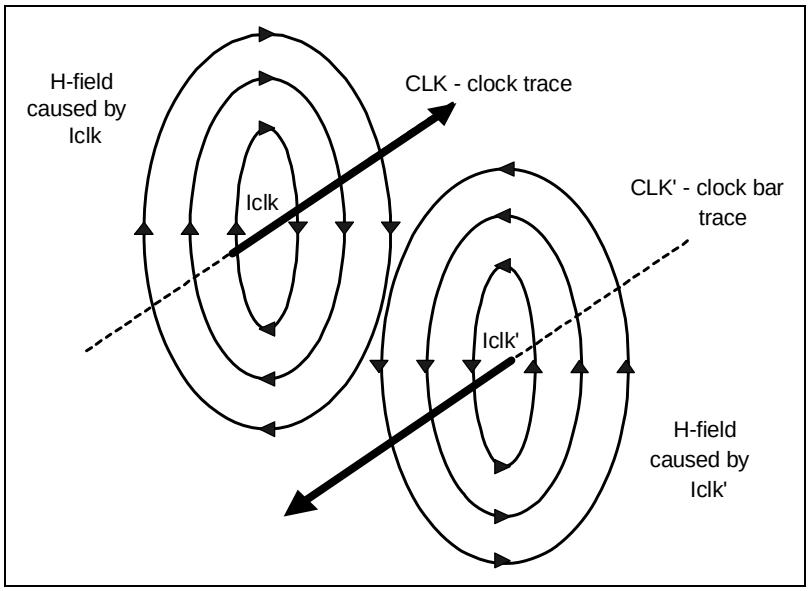


12.5.2 Differential Clocking

Differential clocking requires that the clock generator supply both clock and clock-bar traces. Clock-bar has equal and opposite current as the primary clock, and is also 180 degrees out of phase. To maximize the benefit of differential clocking, both clock lines must be routed parallel to each other for their entire length. Devices connected to the clock must also be designed to accept both the clock and clock-bar signals.

EMI reduction due to differential clocking is caused by H-field cancellation. Since H-field orientation is generated by and is dependent upon current flow, two equal currents flowing in opposite directions and 180 degrees out of phase may have their H-fields cancelled (see Figure 152). Lower H-fields may result in reduced EMI radiation.

Figure 152. Cancellation of H-fields Through Inverse Currents



Differential clocking may also reduce the amount of noise coupled to other traces, which improves signal quality and reduces EMI. I/O signals are particularly important because they often leave the system chassis (serial and parallel ports, keyboards, mouse, etc.), and radiate noise that has been induced onto them. A single-ended clock's return path is usually a reference plane, which is shared by other signals/traces. When noise is created on a single-ended clock, the noise may appear on the reference plane and may be coupled to I/O traces. A differential clock's return path is the clock-bar signal/trace, which is more isolated than the reference plane and minimizes potential I/O trace coupling.

For best results, the trace lengths and routing of the clock lines must be closely matched, and spacing between the two traces should be kept as small as possible. This minimizes loop area and maximizes H-field cancellation. In addition, the real and parasitic terminations of each signal of a differential pair should be the same. Also, the skew between the signal level transitions on the two lines must be small compared to the rise time of the level transitions.

Placing ground traces on the outside of the differential pair may further reduce emissions. Intermediate vias to ground may be needed to reduce the opportunity for re-radiation from the ground traces themselves. Distance between vias should be less than ¼ of a wavelength of the fifth harmonic of the processor core frequency.

12.5.3 PCI Bus Clock Control

Experimental data has indicated a reduction in EMI may be possible by disabling the clocks to unused (and unterminated) PCI slots. CK408, the clock chip that has been specified and designed for this platform, supports individual control of the various PCI clocks. Designers have the option to enable or disable individual PCI clocks depending upon their specific system configuration requirements. Refer to the *CK408 Clock Synthesizer Design Guidelines* for details on how to configure the PCI clocks.

12.5.4 EMI Test Capabilities

FCC regulations in the United States specify the maximum test frequency for products with clocks in excess of 1 GHz is five times the highest clock frequency or 40 GHz, which ever is lower. OEMs are advised to inquire into the capabilities of their preferred EMC test lab to ensure they are able to scan up to the required frequency range.

Processor performance and frequency double approximately every two years. With this in mind, it is advisable to be prepared for the frequencies that may need to be scanned in the next few years.

Since the FCC rules ultimately require testing to 40 GHz, commercial test equipment has been developed that is capable of making measurements to that frequency. Although it may be some time before processors require testing at this frequency, it may be less expensive to upgrade to 40 GHz now, rather than making several intermediate steps.

It is also possible to upgrade various parts at different times. The spectrum analyzer may be upgraded to 40 GHz today with only the necessary antennas to support the initial processor frequencies. As processor speed increases, the necessary antennas and cables may be purchased that support testing to the higher levels.

12.6 Length Tuning

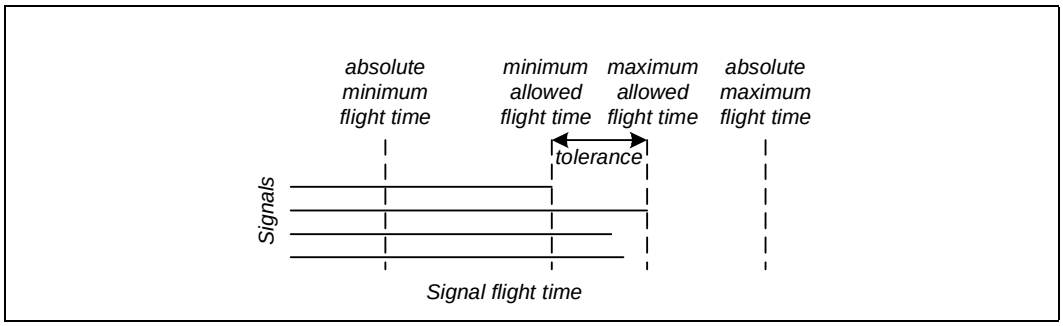
Note: This section does not apply to the Intel® Pentium® M processor system bus.

High speed source synchronous interfaces have very small setup and hold windows. As a result, the signals as a group are very sensitive to skew. A common way to reduce skew is to tune all of the lengths such that the setup and hold windows have the same positional relationship. Length tuning is the matching of two or more signals' total flight time, within a tolerance, to center the setup and hold windows.

Length tuning has several key parameters: signal to be tuned, absolute minimum flight time, absolute maximum flight time, and tolerance. The absolute minimum and maximum flight times define the flexible solution space which lengths may fall within. For a signal to be properly tuned, it must fall within that solution space *and* be within the length tuning tolerance. Figure 153 shows the relationship of these parameters.

A tolerance is a value specifying how far off from exact is allowed. Typically, tolerance is specified in a specific direction, such as –1 ps or ± 2 ps. In the first instance, the total tolerance window or solution space is 1 ps, the second the solution space is 4 ps.

Figure 153. Length Tuning Parameters



The minimum and maximum allowed flight times are at the end points of the tolerance window. The tolerance window may fall anywhere within the range between absolute minimum flight time and maximum flight time. The remainder of this section may simply refer to 'minimum allowed flight time' as 'minimum flight time' and may refer to 'maximum allowed flight time' as 'maximum flight time'.

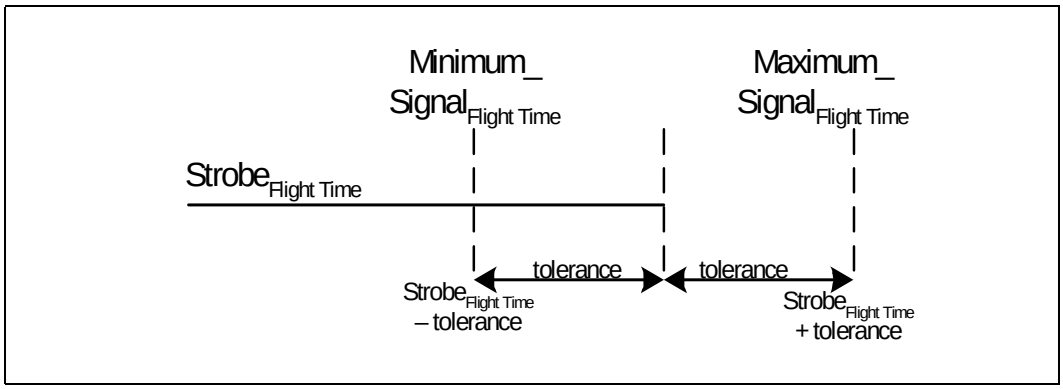
12.6.1 Signal to Strobe Flight Time Relationships

High speed interfaces are commonly latched off of a strobe or a clock. Length tuning ensures that the required setup and hold times of the data signal to the strobe signal or clock signal are not violated due to motherboard routing effects. As a result, each data signal is length tuned with respect to the strobe signal or clock signal. This means that the data signals are all within tolerance of the strobe signal:

$$Minimum\_Signal_{Flight\ Time} = Strobe_{Flight\ Time} - Tolerance$$

$$Maximum\_Signal_{Flight\ Time} = Strobe_{flight\ Time} + Tolerance$$

Figure 154. Signal Length Solution Space with One Strobe

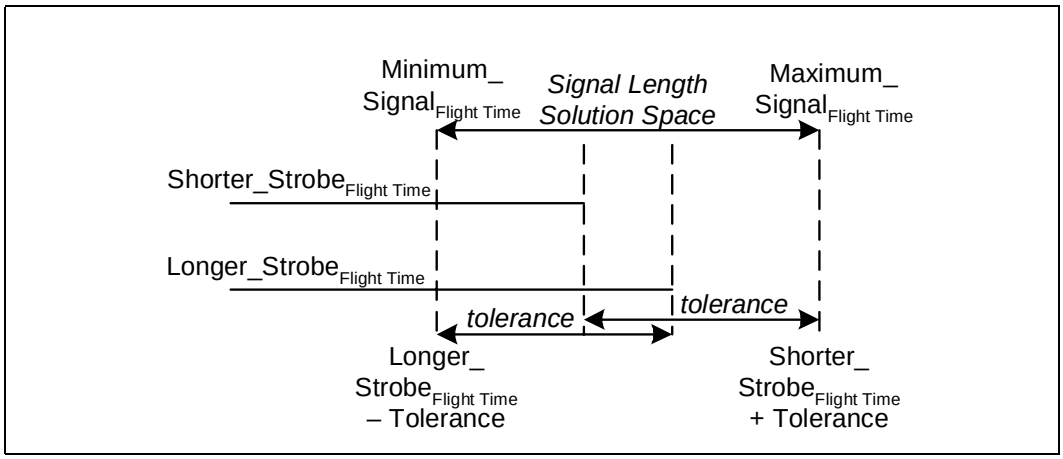


Some groups of high speed signals need to be length tuned to *two* strobes or clocks. In this situation, all signals must be length matched to *both* strobes or clocks and the strobes or clocks must be length matched to each other as well.

$$Minimum\_Signal_{Flight\ Time} = Longer\_Strobe_{Flight\ Time} - Tolerance$$

$$Maximum\_Signal_{Flight\ Time} = Shorter\_Strobe_{Flight\ Time} + Tolerance$$

Figure 155. Signal Length Solution Space with Two Strobes

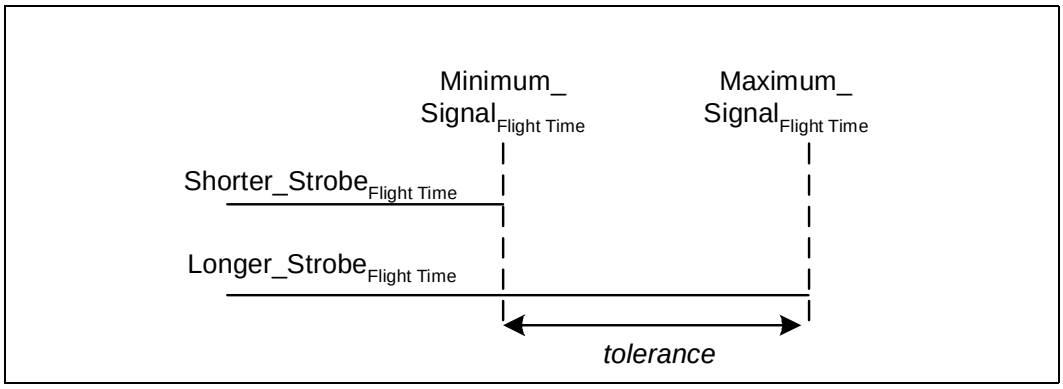


When the strobes are the furthest apart (i.e., as far apart as allowed for signals of the same group), then their difference is the total allowed tolerance. This means that all signals must fall between them, or have a solution space which is "*tolerance*" wide.

$$Longer\_Strobe_{Flight\ Time} = Shorter\_Strobe_{Flight\ Time} + Tolerance$$

$$Shorter\_Strobe_{Flight\ Time} = Longer\_Strobe_{Flight\ Time} - Tolerance$$

Figure 156. Signal Length Solution Space with Maximum Tolerance Strobes



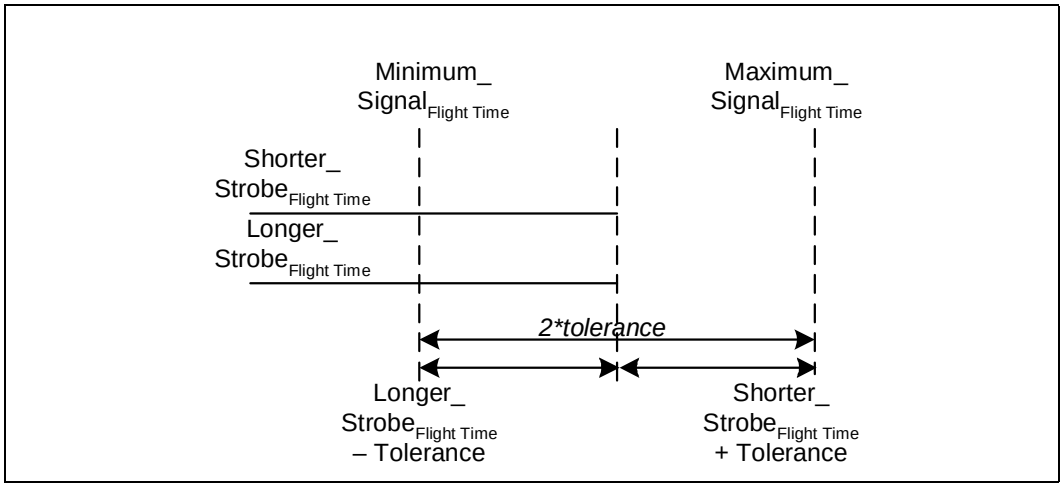
When the strobes have exactly the same flight time, then the signals have a solution space which is *2*tolerance* wide.

$$Strobe_{Flight\ Time} = Longer\_Strobe_{Flight\ Time} = Shorter\_Strobe_{Flight\ Time}$$

$$Minimum\_Signal_{Flight\ Time} = Strobe_{Flight\ Time} - Tolerance$$

$$Maximum\_Signal_{Flight\ Time} = Strobe_{Flight\ Time} + Tolerance$$

Figure 157. Signal Length Solution Space with Matched Strobes



12.6.2 Flight Time Segment Analysis

Length matching often requires package compensation. Every time a signal changes innerconnect or layer, there is an affect on flight time. The most effective way to calculate flight time is to break up each signal into segments of constant flight time, analyze those segments, and then add the segment together.

Flight time is directly proportional to trace length by a constant trace velocity.

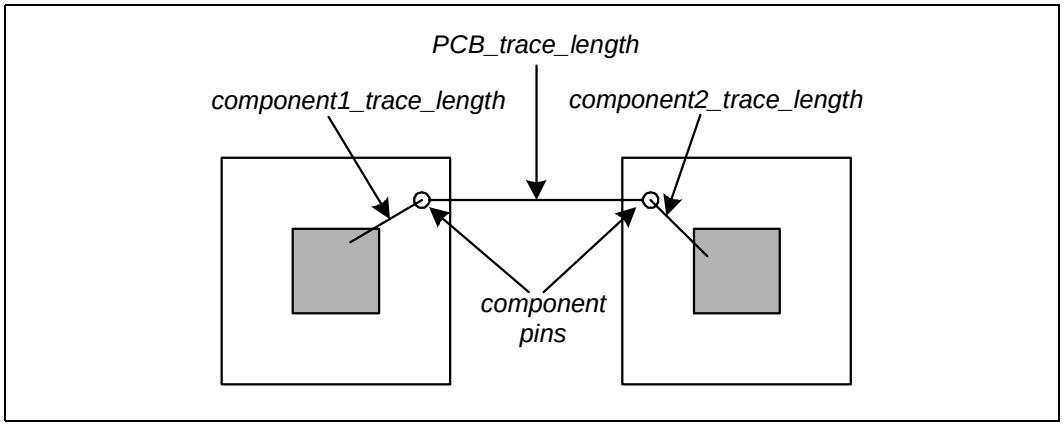
Equation 1. Flight Time

$$flight\_time = \frac{trace\_length}{trace\_velocity}$$

To determine the total flight time, each segment with a constant trace velocity must be identified. These segments are commonly defined at component interconnects. For example, a signal which connects two different components through a PCB would be calculated as follows:

$$Total\_Signal_{Flight\ Time} = Signal_{Componet1\ Flight\ Time} + Signal_{PCB\ Flight\ Time} + Signal_{Component2\ Flight\ Time}$$

Figure 158. Total Signal Length with Two Components



Using the segment lengths and velocities yields:

Equation 2. Total Flight Time

$$total\_flight\_time = \frac{component1\_length}{component1\_velocity} + \frac{PCB\_length}{PCB\_velocitiy} + \frac{component2\_length}{component2\_velocity}$$

12.6.3 Length Tuning Equation Derivation

When routing a motherboard, only one piece of the equation is a variable: *PCB trace length*. For example, when signals are tuned with respect to the strobe, the final equation used by a motherboard designer is derived as follows. First, two equations are defined:

$$\text{Total\_Strobe}_{\text{Flight Time}} = \text{Strobe}_{\text{Component1 Flight Time}} + \text{Strobe}_{\text{PCB Flight Time}} + \text{Strobe}_{\text{Component2 Flight Time}}$$

$$\text{Total\_Signal}_{\text{Flight Time}} = \text{Signal}_{\text{Component1 Flight Time}} + \text{Signal}_{\text{PCB Flight Time}} + \text{Signal}_{\text{Component2 Flight Time}}$$

Combining these equations yields:

$$\text{Total\_Strobe}_{\text{Flight Time}} = \text{Total\_Signal}_{\text{Flight Time}} \pm \text{Tolerance}$$

$$\text{Strobe}_{\text{Component1 Flight Time}} + \text{Strobe}_{\text{PCB Flight Time}} + \text{Strobe}_{\text{Component2 Flight Time}} = \text{Signal}_{\text{Component1 Flight Time}} + \text{Signal}_{\text{PCB Flight Time}} + \text{Signal}_{\text{Component2 Flight Time}} \pm \text{Tolerance}$$

Solving for $\text{Signal}_{\text{PCB Flight Time}}$ yields:

$$\text{Signal}_{\text{PCB Flight Time}} = \text{Strobe}_{\text{Component1 Flight Time}} + \text{Strobe}_{\text{PCB Flight Time}} + \text{Strobe}_{\text{Component2 Flight Time}} - \text{Signal}_{\text{Component1 Flight Time}} - \text{Signal}_{\text{Component2 Flight Time}} \pm \text{Tolerance}$$

Now substituting in velocities and trace lengths, we conclude with Equation 3.

Equation 3. Tuning for One Signal with Respect to One Strobe

$$\begin{aligned}\text{Signal}_{\text{PCB Trace Length}} = {} & ((\text{Strobe}_{\text{Component1 Trace Length}} / \text{Strobe}_{\text{Component1 Trace Velocity}}) \\ & + (\text{Strobe}_{\text{PCB Trace Length}} / \text{Strobe}_{\text{PCB Trace Velocity}}) \\ & + (\text{Strobe}_{\text{Component2 Trace Length}} / \text{Strobe}_{\text{Component2 Trace Velocity}}) \\ & - (\text{Signal}_{\text{Component1 Trace Length}} / \text{Signal}_{\text{Component1 Trace Velocity}}) \\ & - (\text{Signal}_{\text{Component2 Trace Length}} / \text{Signal}_{\text{Component2 Trace Velocity}})) \\ & * \text{Signal}_{\text{PCB Trace Velocity}} \pm \text{Tolerance}\end{aligned}$$

Example 1. DDR Example

The DDR Source Synchronous bus requires groups of eight signals and two strobes to be length tuned within 25 mils. Given that the PCB trace length for DDRA_DQS2 is 3.85 inches, what is the solution space for DDRA_DQS11 and DDRA_DQ20?

To determine the PCB solution space for the signal DDRA_DQ20, you need the PCB length of the strobe DDRA_DQS11. So, we may find the length for DDRA_DQS11 first. Using Equation 3 as a basis:

$$\begin{aligned} DDRA\_DQS11_{PCB\_length} = {} & ((DDRA\_DQS2_{MCH\_length} / DDRA\_DQS2_{MCH\_velocity}) \\ & + (DDRA\_DQS2_{PCB\_length} / DDRA\_DQS2_{PCB\_velocity}) \\ & - (DDRA\_DQS11_{MCH\_length} / DDRA\_DQS11_{MCH\_velocity})) \\ & * DDRA\_DQS11_{PCB\_velocity} \pm Tolerance \end{aligned}$$

The MCH package velocities and trace lengths are located in the *Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet*, "Chipset Interface Trace Length Compensation" Chapter. The datasheet states that the trace delay due to signal velocity is the inverse of velocity. The MCH package trace delay due to signal velocity is 150 ps/in, so the velocity is $(150\ ps/in)^{-1}$. The PCB delay due to signal velocity is 175 ps/in, so the velocity is $(175\ ps/in)^{-1}$. The MCH package trace length for DDRA_DQS2 is 356.06 mils, DDRA_DQS11 is 567.48 mils, and DDRA_DQ20 is 690.51 mils.

$$\begin{aligned} DDRA\_DQS11_{PCB\_length} = {} & ((0.35606\ in * 150\ ps/in) \\ & + (3.850\ in * 175\ ps/in) \\ & - (0.56748\ in * 150\ ps/in)) \\ & / 175\ ps/in \pm 0.025\ in \\ = {} & 3.669\ in \pm 0.025\ in \end{aligned}$$

By setting the PCB length of DDRA_DQS11 as close to 3.669 inches as possible, we may have a wider solution space for all eight of the signals which need to be length tuned to DDRA_DQS2 and DDRA_DQS11. Next, let's find the PCB length for DDRA_DQ20. Using Equation 3 as a basis:

$$\begin{aligned} DDRA\_DQ20_{PCB\_length} = {} & ((DDRA\_DQS2_{MCH\_length} * DDRA\_DQS2_{MCH\_velocity}) \\ & + (DDRA\_DQS2_{PCB\_length} * DDRA\_DQS2_{PCB\_velocity}) \\ & - (DDRA\_DQS20_{MCH\_length} * DDRA\_DQS20_{MCH\_velocity})) \\ & * DDRA\_DQ20_{PCB\_velocity} \pm Tolerance \end{aligned}$$

Then, using the values from above and simplifying the velocity yields:

$$\begin{aligned} DDRA\_DQS11_{PCB\_length} = {} & ((0.35606\ in * 150\ ps/in) \\ & + (3.850\ in * 175\ ps/in) \\ & - (0.69051\ in * 150\ ps/in)) \\ & / 175\ ps/in \pm 0.025\ in \\ = {} & 3.563\ in \pm 0.025\ in \end{aligned}$$

12.6.4 Bus Length Tuning Methodology

Many buses, such as memory and processor system bus, require length tuning a group of signals. A common way to do this is by routing the bus first to determine what the approximate length range is. Then, you may pick an arbitrary signal. Sometimes this signal may be the most difficult to route or adjust to tune. Using the PCB trace length for this signal, you may determine the solution space for the remainder of the signals and strobes in the group.

Intel commonly provides a length tuning calculator spreadsheet. This calculator uses a "seed value." This is the PCB length of an arbitrary signal, typically the signal with the shortest PCB length. Then, the calculator uses all the routing parameters specified in the Platform Design Guide (minimum and maximum lengths, tolerances, signal groups, etc.) to determine the solution space for the bus in question.

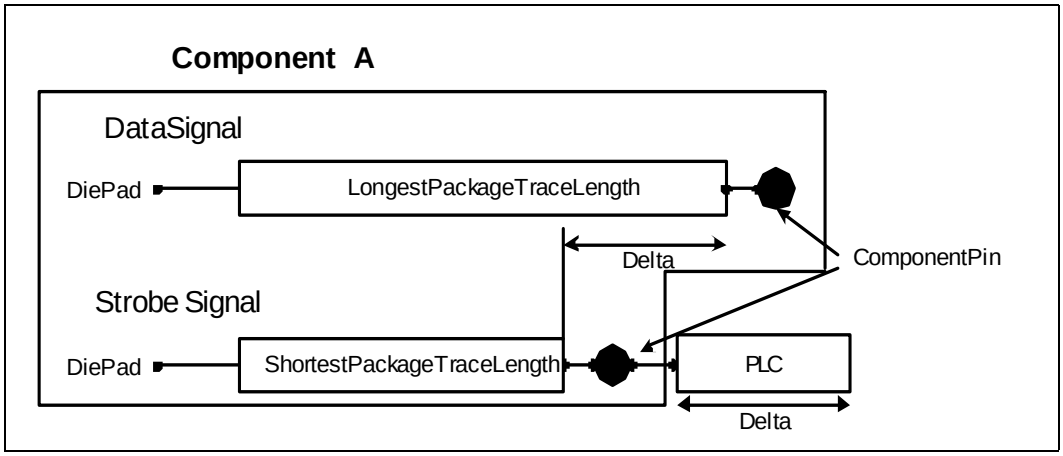
12.7 Processor Bus Tuning

Routing the processor system bus requires length matching within source synchronous groups. As a result, propagation-based length matching is used to account for the strobe-to-signal skew effects. Propagation-based length matching is described in the next section, followed by a routing example.

12.7.1 Compensating for Package Trace Length Differences

The first factor in length matching involves compensating for package trace length differences for signals within the same strobe group. The "package trace length" is defined as the trace segment between the die pad and component package pin. The package lengths on the processor and MCH introduce skew between different signals as illustrated in the example given in Figure 159. Note that "Component A" represents a processor or MCH. The example uses a strobe and data signal, which happen to have the shortest and longest package trace lengths respectively. Each of the signals will have varying amounts of package skew. The amount of skew for a particular signal is based on the difference between that signal's package trace length and the longest signal's package trace length in the same signal group. E.g., signals with shorter package length will have more package trace length compensation than signals with package lengths closer to the longest package trace.

Figure 159. Package Trace Length Differences



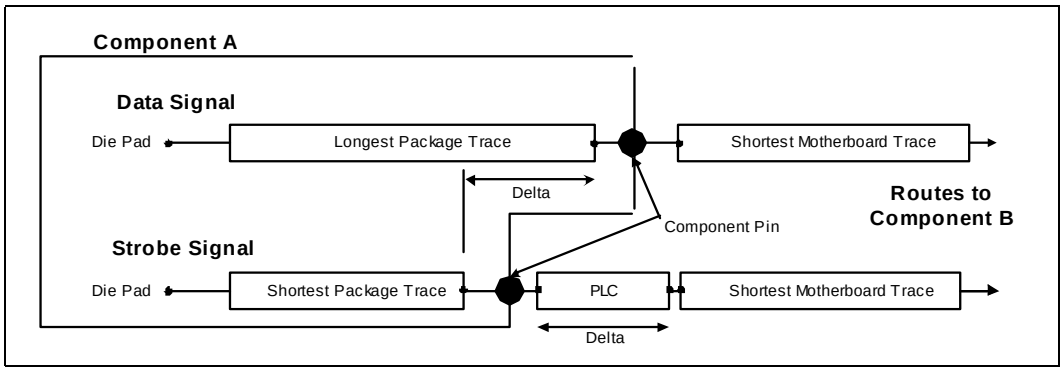
To compensate for package-induced skew, all source synchronous motherboard trace lengths are adjusted by the exact amount of Package Length Compensation (PLC). Equation 4 defines PLC for a particular signal. Signal X is any signal in the group that does not have the longest package length. This includes the strobe signals.

Equation 4. Package Length Compensation (PLC) Definition

$$SignalX_{PLC} = Maximum\_Signal\_in\_Group_{Package\ Length} - SignalX_{Package\ Length}$$

The signals with a package length less than the longest package trace in that group will require additional motherboard trace length equal to $SignalX_{PLC}$. Equation 4 yields a zero PLC for the signal with the longest package length. So the signal with the longest package length would require no amount of additional motherboard trace length. Figure 160 illustrates PLC using a data signal as the longest package trace and strobe signal as “Signal X”.

Figure 160. Example of PLC Compensation on the Motherboard

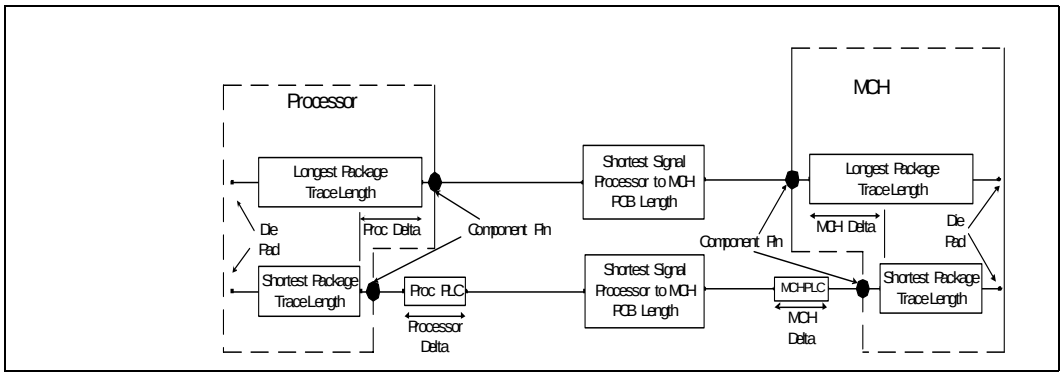


12.7.2 Length Matching Equation

This section explains the length matching compensation scheme, associated equations, and an explanation for determining the motherboard trace lengths. Processor Length Matching is only dependant upon a signals PLC. To determine an actual PCB length, the designer may use one signal as a reference signal to calculate the PCB length of the remaining signals in a group. For simple illustrative purposes, the formulas and examples used are based upon the shortest PCB trace length. However, the formulas could be based off any signal in the group. For simple illustrative purposes, the example also assumes the shortest and longest signals on the processor package are the shortest and longest for the MCH package as well. This is not necessarily the case.

Figure 161 contains the final length matching example that account for PLC in the motherboard trace lengths. The signal whose motherboard trace length between. All source synchronous signals with less than the longest processor and MCH package length require varying amounts of PLC motherboard length segments added to $Shortest\ Signal_{Processor\ to\ MCH\ PCB\ Length}$ respectively.

Figure 161. Illustration of PLC Length Matching



The length matching equation is based on the PLC concepts explained in the previous section. The total pad-to-pad length is represented by Equation 5 for the driver/receiver path and may be derived by adding the total lengths as illustrated in Figure 161.

Equation 5. Processor/MCH Length Matching

$$\text{SignalX}_{\text{Processor Die Pad-to-MCH Die Pad}} = \text{SignalX}_{\text{Processor Package Length}} + \text{SignalX}_{\text{Processor PLC}} + \text{SignalX}_{\text{MCH PLC}} + \text{SignalX}_{\text{MCH Package Length}}$$

The PLC length parameter is calculated using Equation 4. Extracting specific parameters from Equation 5, the total motherboard length for Signal X in the Processor/MCH path is defined in Equation 6.

Equation 6. Processor to MCH PCB Length Definition

$$\text{SignalX}_{\text{Processor to MCH PCB Length}} = \text{SignalX}_{\text{MCH PLC}} + \text{Shortest Signal}_{\text{Processor to MCH PCB Length}}$$

$\text{SignalX}_{\text{Processor to MCH PCB Length}}$ should be chosen to allow all signals in the same signal group to meet the specific system bus routing guidelines documented in Section 5, "System Bus Routing Guidelines" of this document. The PLC adjust the motherboard trace lengths to account for the processor and MCH package effects.

Using this relationship, if $\text{SignalX}_{\text{Processor to MCH PCB Length}}$ are known, then $\text{SignalY}_{\text{Processor to MCH PCB Length}}$ may be determined using Equation 7 respectively.

Equation 7. SignalY Processor /MCH Motherboard Lengths

$$\text{SignalY}_{\text{Processor to MCH PCB Length}} = \text{SignalX}_{\text{Processor to MCH PCB Length}} - \text{SignalX}_{\text{Processor PLC}} + \text{SignalY}_{\text{MCH PLC}}$$

The equation operates by first starting with the known total motherboard length for Signal X and then subtracting Signal X's PLC compensations. The PLC compensation for Signal Y are then added.

12.7.3 System Bus Length Matching Example

Note: Example component values are used in this example and should not be relied upon for actual design of the system bus.

The system bus source synchronous signal group requires groups of signals and associated strobes to be length matched within ± 25 mils between components.

Sample: Given that routing has started with DSTBN0# routed between Processor and MCH with a pad-to-pad route of exactly 4.0 inches, what is the DSTBP0# Processor/MCH motherboard length?

See Section 12.8 for processor package trace lengths. The MCH package trace lengths may be obtained from the Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet. Alternatively the processor and MCH package trace lengths may be found in the Intel® Pentium M Processor System Bus Length Matching Spreadsheet. Contact your Intel representative for information about the Length Matching Spreadsheet tool. For this example, we will use the following processor and MCH values:

- Maximum processor package length is this group is 0.722 inch
- DSTBN0# processor package length is 0.722 inch
- DSTBP0# processor package length is 0.722 inch
- Maximum MCH package length is this group is 1.060 inches
- DSTBN0# MCH package length is 0.842 inch
- DSTBP0# MCH package length is 0.738 inch

Sample Solution: By definition, the DSTBN0# signal 4-inch route already includes the PLC motherboard trace components. The MCH PLC values are determined for DSTBN0# and DSTBP0# using Equation 4.

$$DSTBN0\#_{MCH\ PLC} = Maximum\ in\ Group_{MCH\ Package\ Length} - DSTBN0\#_{MCH\ Package\ Length}$$

$$= 1.060\ inch - 0.842\ inch = 0.218\ inch$$

$$DSTBP0\#_{MCH\ PLC} = Maximum\ in\ Group_{MCH\ Package\ Length} - DSTBP0\#_{MCH\ Package\ Length}$$

$$= 1.060\ inches - 0.738\ inch = 0.322\ inch$$

The DSTBP0# Processor/MCH motherboard lengths are calculated using Equation 7.

$$DSTBP0\#_{Processor\ to\ MCH\ PCB\ Length} = DSTBN0\#_{Processor\ to\ MCH\ PCB\ Length} - DSTBN0\#_{MCH\ PLC} + DSTBP0\#_{MCH\ PLC}$$

$$= 4.000 - 0.218 + 0.322 = 4.104\ inches$$

Since the system bus data signals must be length matched within ± 25 mils between components, the DSTBP0# Processor/MCH motherboard length is 4.104 ± 0.025 inch.

The above example demonstrates the importance of the first routed motherboard traces since these will establish the routing lengths for the remaining signals in the same signal group. Therefore, the $DSTBP0\#_{Processor\ to\ MCH\ PCB\ Length}$ value should be chosen carefully based on routing studies to avoid multiple iterations of length matching computations for each signal.

12.8 Intel® Pentium® M Processor Signal Package Lengths

Table 94 lists the preliminary package trace lengths of the Intel® Pentium® M processor for the source synchronous data and address signals. All the signals within the same group are routed to the same length ± 0.1-mil accuracy. The Intel Pentium M processor package traces are routed as micro-strip lines with a nominal characteristic impedance of 50 Ω ± 10%.

Table 94. Intel® Pentium® M Processor Signal Package Lengths (Sheet 1 of 2)

Signal Group	CPU Signal Name	Intel® Pentium® M Package Trace Length (mils)
Data Group 1	D[15:0]#	722
	DINV[0]#	722
	DSTBP[0]#	722
	DSTBN[0]#	722
Data Group 2	D[31:16]#	564
	DINV[1]#	564
	DSTBP[1]#	564
	DSTBN[1]#	564
Data Group 3	D[47:32]#	661
	DINV[2]#	661
	DSTBP[2]#	661
	DSTBN[2]#	661
Data Group 4	D[63:48]#	758
	DINV[3]#	758
	DSTBP[3]#	758
	DSTBN[3]#	758
Address Group 1	REQ[4:0]#	616
	A[16:3]#	616
	ADSTB[0]#	616
Address Group 2	A[31:17]#	773
	ADSTB[1]#	773

Table 94. Intel® Pentium® M Processor Signal Package Lengths (Sheet 2 of 2)

Signal Group	CPU Signal Name	Intel® Pentium® M Package Trace Length (mils)
Common Clock Signals	ADS#	454
	BNR#	506
	BPRI#	424
	BRO#	336
	DBSY#	445
	DEFER#	349
	DRDY#	529
	HIT#	420
	HITM#	368
	LOCK#	499
	RS[0]#	576
	RS[1]#	524
	RS[2]#	451
	TRDY#	389
	RESET#	455
Differential Host Clocks		
Host Clocks	BCLK0	447
	BCLK1	447

12.9 Common Layout Pitfalls

This section describes common high-speed issues found when laying out a PCB. Examples are provided to aid the board developer in avoiding these issues. The signals described in this section pertain to high-speed signals such as those found on the system bus, memory bus, etc.

12.9.1 Group Like Signals Under BGAs

To minimize impedance for ground and power pins, like-signals should be tied together whenever possible. Figure 162 shows the proper method for grouping like-signals for the processor and Figure 163 shows the MCH grouping. The same methodology should be applied to the Intel® P64H2 and Intel® ICH3-S.

Figure 162. CPU Like-Signals Grouped

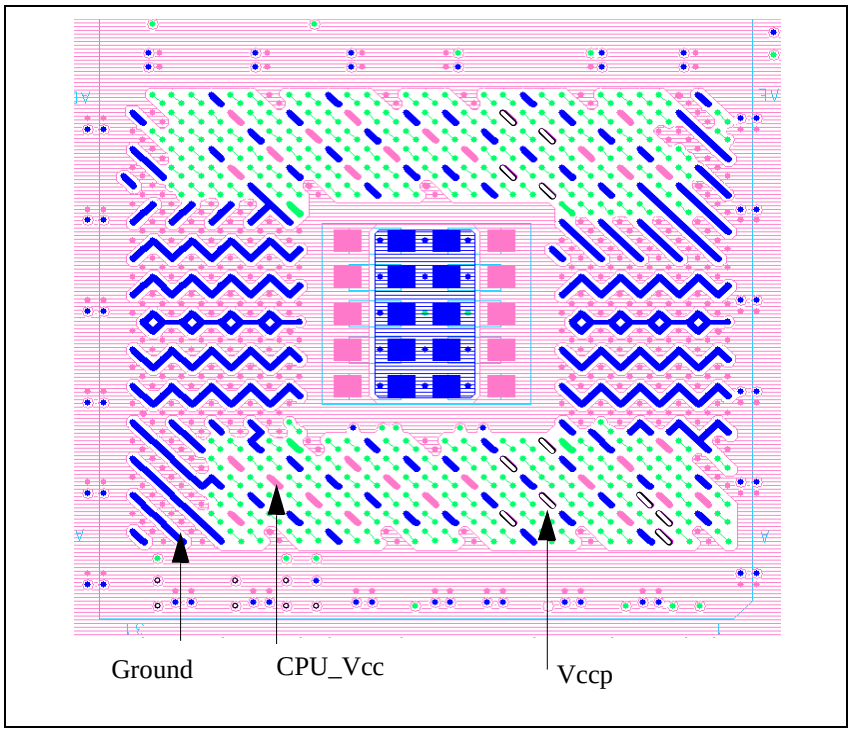
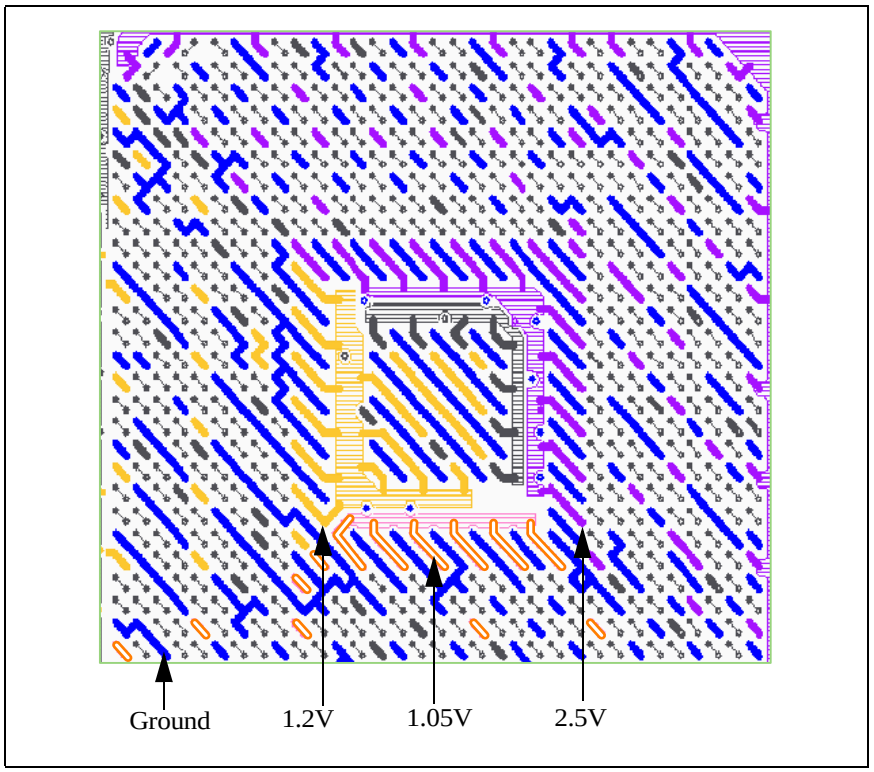


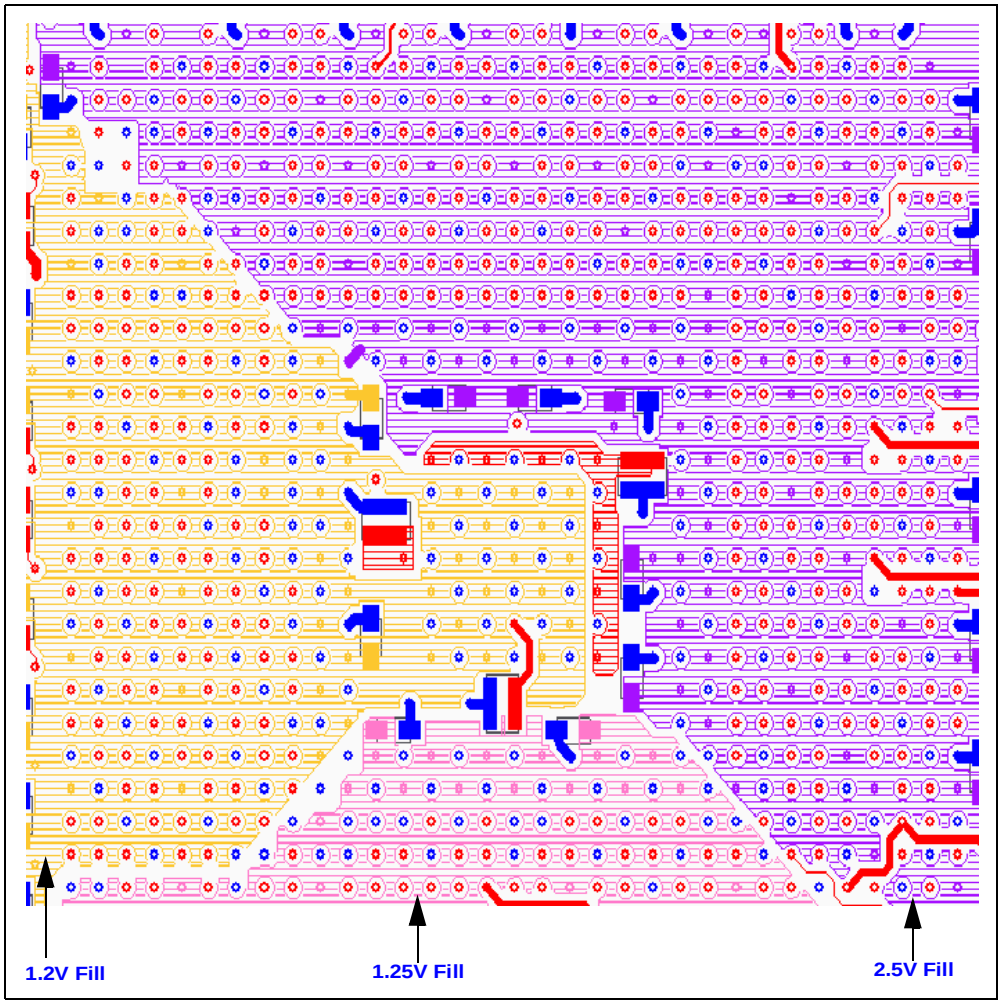
Figure 163. MCH Like-Signals Grouped



12.9.2 Fill Areas Under BGAs

To minimize impedance for ground and power pins, ensure power and ground fills are placed directly under the BGAs. Figure 164 shows the proper method for fills under the MCH. The same methodology should be applied to the processor, Intel® P64H2 and Intel® ICH3-S.

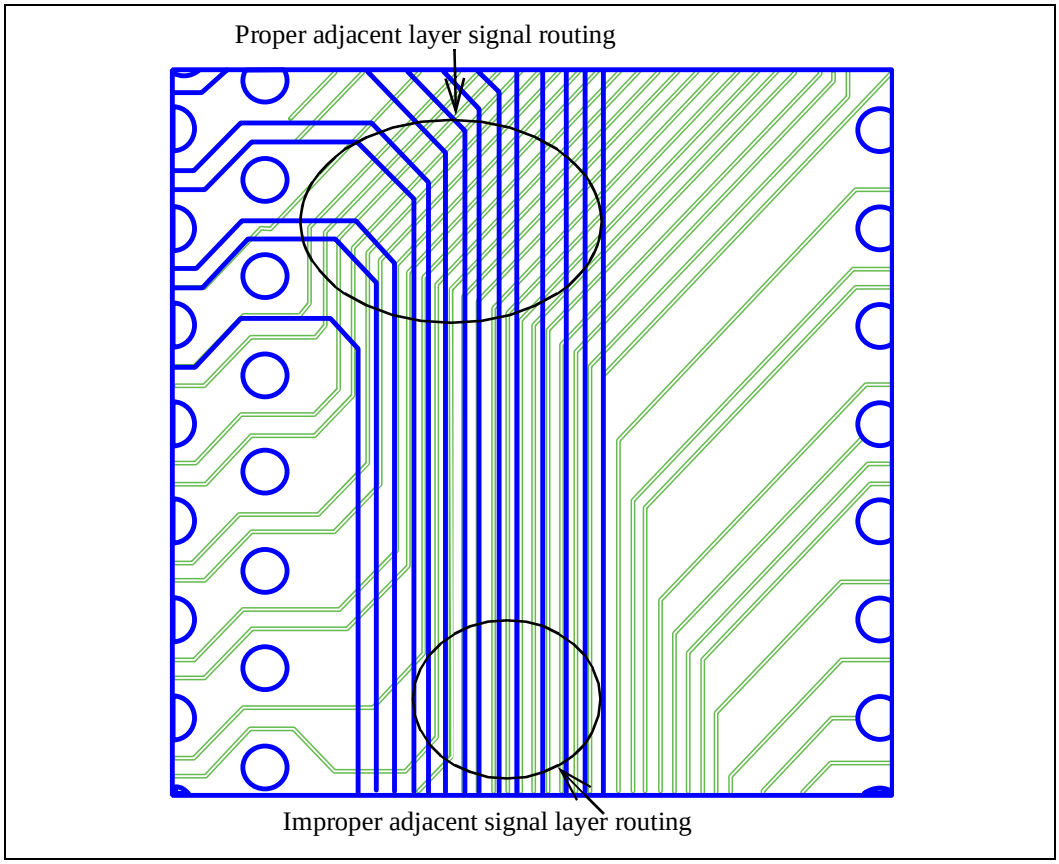
Figure 164. MCH Fill



12.9.3 Signal Parallelism

To minimize high-speed signal induced noise (cross-talk) limit or do not route signals on adjacent layers parallel to each. Figure 165 shows the proper and improper methods for routing signals on adjacent layers.

Figure 165. Signal Parallelism



12.9.4 Via Sharing

To minimize impedance, traces should not share vias. Figure 166 shows the improper method of via sharing. Figure 167 shows how to correct via sharing.

Figure 166. Improper Via Sharing

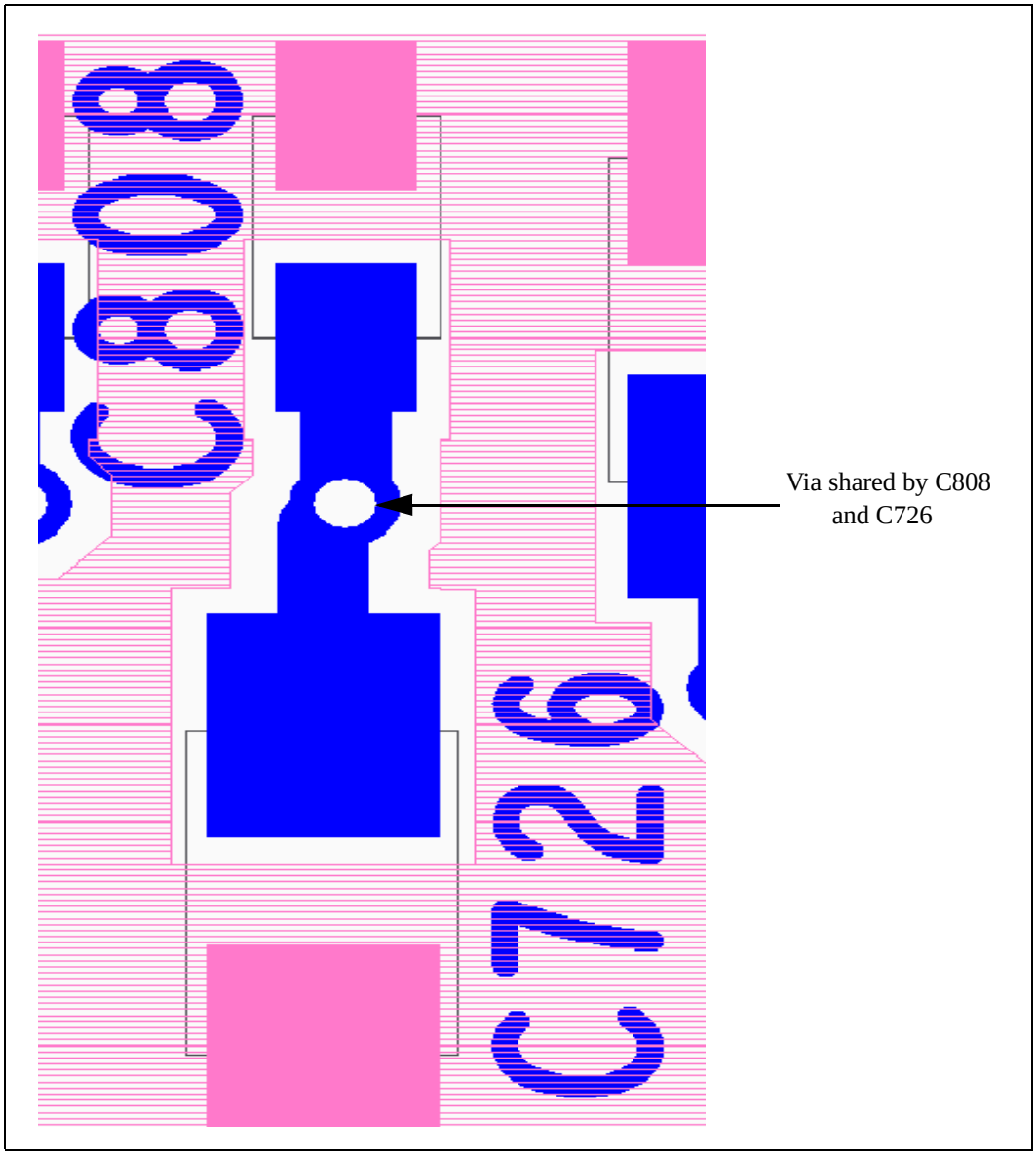
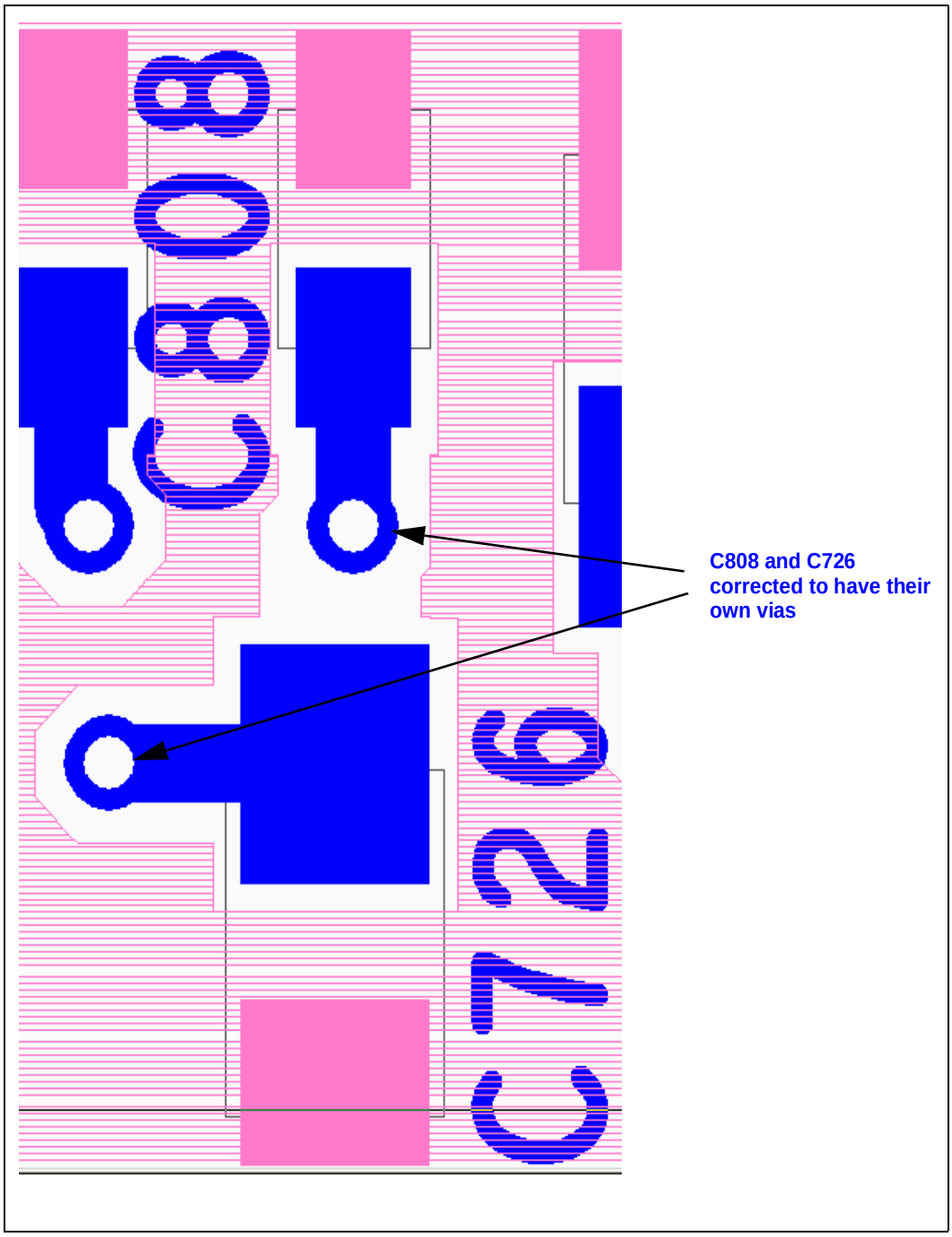


Figure 167. Correct Via Sharing



12.9.5 Necking Down

To maintain the current carrying capacity of a thicker power/ground trace do not neck the trace down. When a trace is necked down, the entire trace essentially takes on the current carrying capacity of the narrowest width thus decreasing the current capacity effect of the thicker traces. Figure 168 shows the improper method of necking down. To correct this issue the same trace may be routed on several different layers and connected by an adequate amount of vias. A second option is shown in Figure 169. This method doubles the narrow trace to correct the neck down.

Figure 168. Improper Necking Down

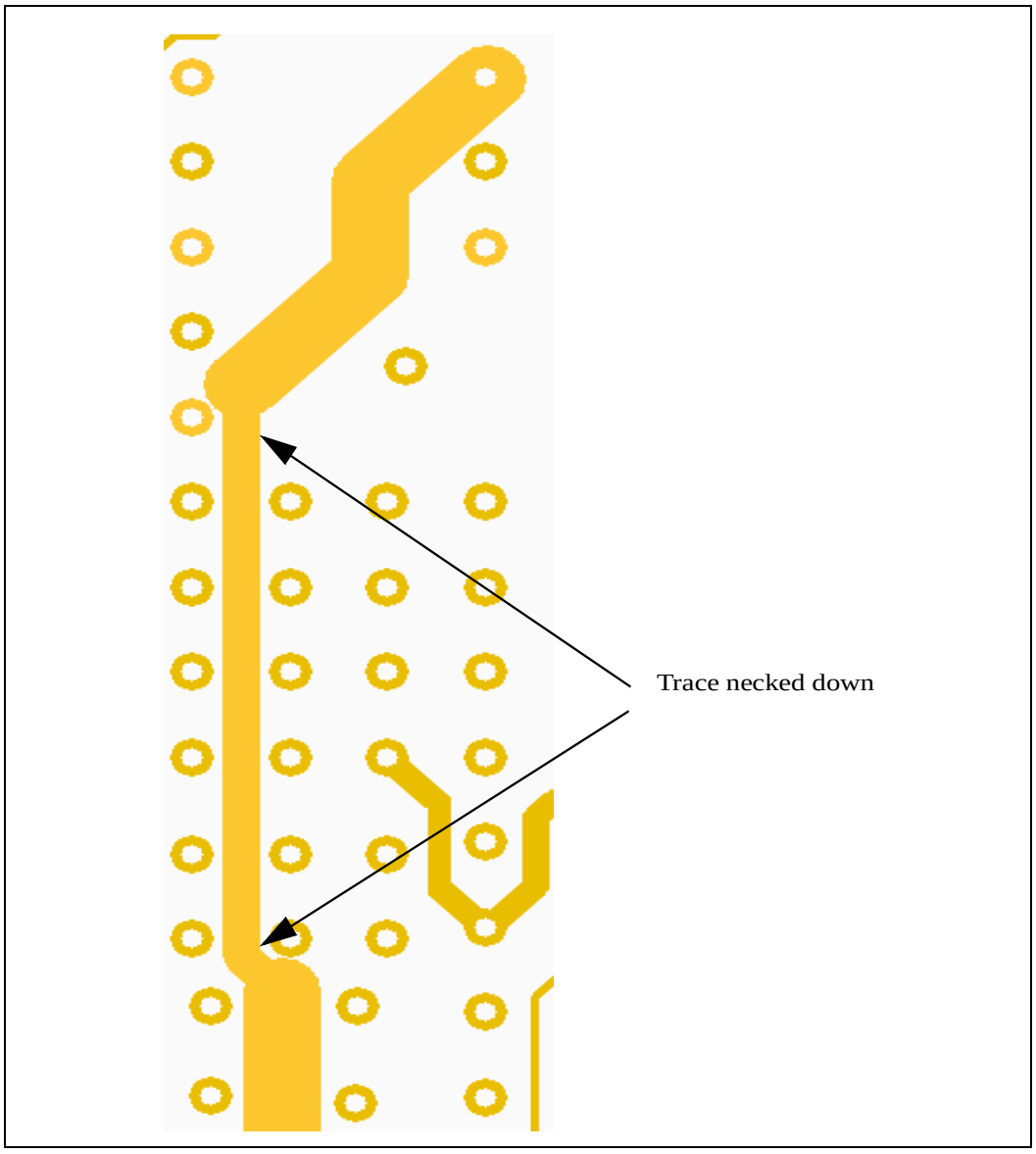
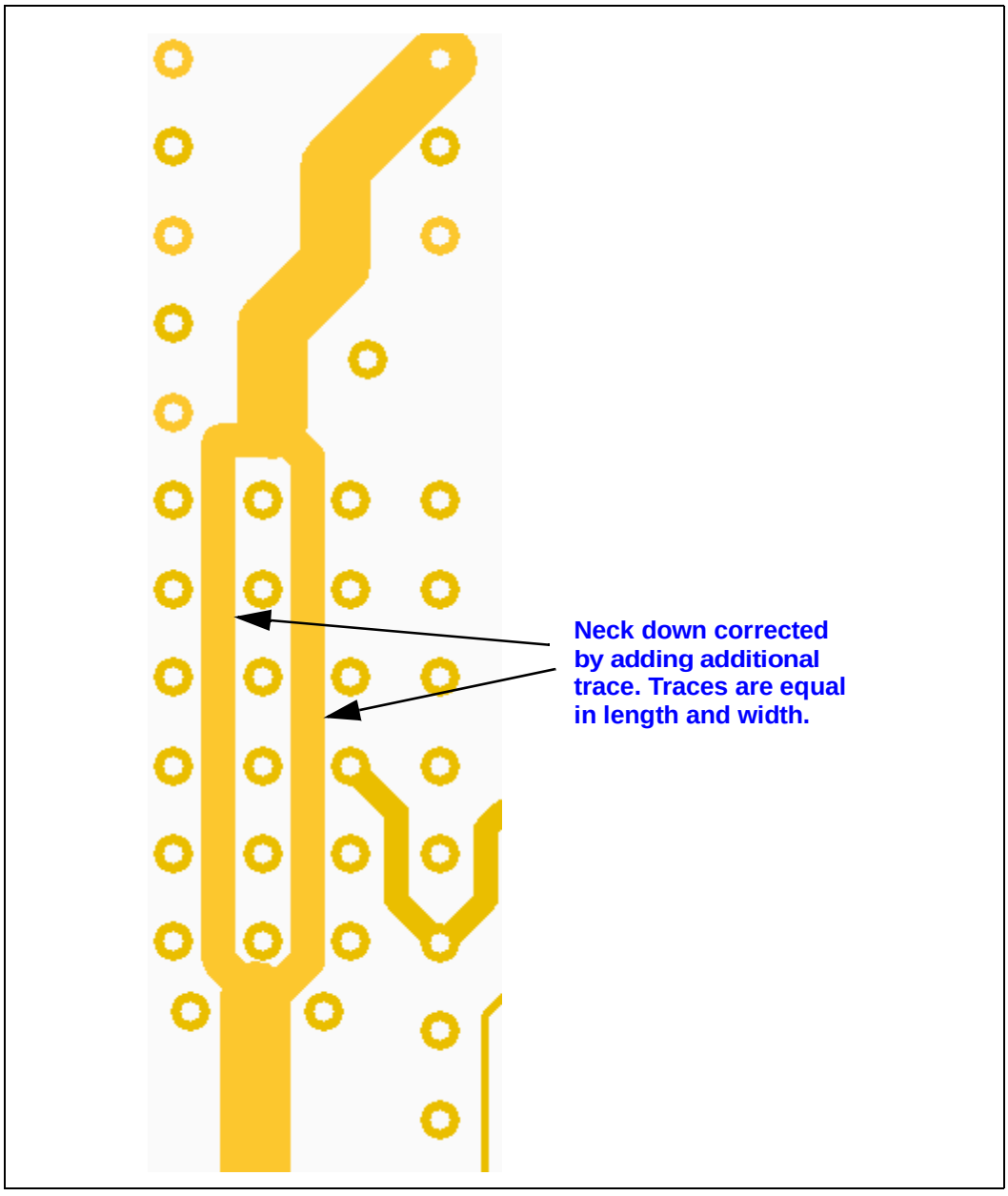


Figure 169. Correct Necking Down



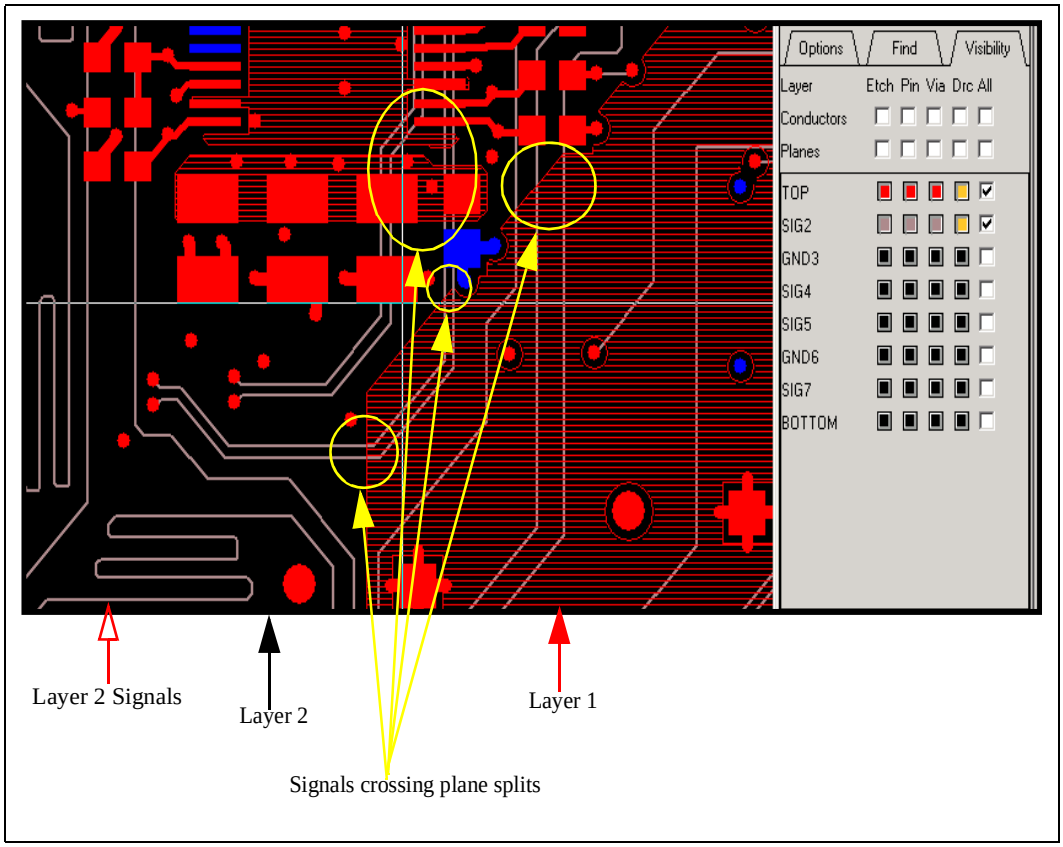
12.9.6 Signals Crossing Plane Splits

Signals that cross an adjacent layers plane boundary is undesirable for two reasons:

- The return current that runs in the reference plane wants to share its current with the adjacent layers reference plane it just crossed over. The return current now has to find a return path on the adjacent layer which will cause signal delay.
- The impedance of the trace will changes each time it crosses a plane.

Figure 170 shows the improper method of signals crossing adjacent layers plane boundaries. Signal routing is done on layer 2 while layer 1 (striped area) contains power and ground. Signals should be routed in a way to avoid this issue such as routing on a different layer or repositioning the signals to avoid the adjacent layers plane boundary.

Figure 170. Signal Crossing Plane Splits



Schematic Checklist 13

13.1 Processor Schematic Checklist

Table 95. Processor Schematic Checklist (Sheet 1 of 5)

Checklist Items	Recommendations	Comments
Intel® Pentium® M Processor System Bus (PSB) Interface Signals		
A[31:3]#[1] ADSTB[1:0]#[2] D[63:0]#[3] DINV[3:0]#[9] DSTBN[3:0]#[4] DSTBP[3:0]#[5] REQ[4:0]#[6]	Connect to processor and the MCH.	Refer to Section 5.1.5.
ADS# BPM[3:0]# BR0# DBSY# DRDY# LOCK# BPRI# DEFER# RS[2:0]# TRDY#[8]	Connect to processor and the MCH.	Refer to Section 5.1.6.
IERR#	• When IERR# is not used: – Terminate with 56 Ω ± 5% resistor to VCCP. • When IERR# is used: – Connect to receiver with a 56 Ω ± 5% series resistor and terminate with 56 Ω ± 5% resistor to VCCP.	Refer to Section 5.1.7.1.1.
BNR# HIT# HITM#	Connect to processor and the MCH.	Refer to Section 5.1.6.
RESET#[7]	• No ITP debug port present: – Connect to processor and the MCH. – On-die termination provides proper signal quality. • ITP debug port present: – Connect to processor and the MCH. – Pull-up to VCCP through a 54.9 Ω ± 1% resistor.	• Refer to Section 5.1.4.2. • For additional information refer to the *ITP700 Debug Port Design Guide* for all schematic, layout and routing recommendations.

Table 95. Processor Schematic Checklist (Sheet 2 of 5)

Checklist Items	Recommendations	Comments
A20M# IGNNE# INIT# LINT0/INTR LINT1/NMI CPU_SLP# SMI#	Connect to the processor and the Intel® ICH3-S. Include 200 Ω ± 5% pull-up to VCCP. See schematics for further details on stuffing option.	Refer to Section 5.1.7.1.5.
PWRGOOD	Recommend 300 Ω ± 5% pull-up to VCCP. Connect to the processor and the Intel ICH3-S.	Refer to Section 5.1.7.1.4.
STPCLK#	Connect to the Intel ICH3-S through a 0 Ω series resistor. Include 200 Ω ± 5% pull-up to VCCP.	
PSI#	Connect to an Intel ICH-3 GPIO pin or customer specific circuitry.	See Schematic for circuitry used to connect to the Intel ICH-3 GPIO pin.
DPSLP#	Pull-up to VCCP with a 200 Ω ± 5% resistor.	The pull-up is required because DPSLP# is not supported.
FERR#/PBE#	Connect to the Intel ICH3-S through voltage translation logic and Terminate with 56 Ω ± 5% pull-up to VCCP.	Refer to Section 5.1.7.1.2.
PROCHOT#	• When supported, connect to the Intel ICH3-S GPIO or customer specific circuitry and terminate with a 56 Ω ± 5% pull-up to VCCP. • When not supported terminate with a 56 Ω ± 5% pull-up to VCCP.	Refer to Section 5.1.7.1.3.
Processor In Target Probe (ITP) Signals		
BPM[3:0]#	• **When ITP700FLEX Is Not Used**: – Leave signals as No Connect (N/C) • **When ITP700FLEX Is Used**: – Point to point connection to CPU pin. **ITP700FLEX** to **CPU** BPM[3:0]# BPM[3:0]# BPM4# PRDY# BPM5# PREQ#	Refer to Section 10.2.
PRDY#	Connect to BPM4# on ITP connector	See previous BPM[3:0] definitions.
PREQ#	Connect to BPM5# on ITP connector	See previous BPM[3:0] definitions.
TCK	• Pull down to GND with a 27 Ω resistor when an ITP700FLEX is not used. • Connect to ITP connector and pull-down to GND with a 27.4 ± 1%Ω resistor when an ITP700FLEX is used.	• **When ITP700FLEX Is Not Used**: – Parallel termination resistor required when neither the onboard ITP nor ITP interposer are planned to be used. • **When ITP700FLEX Is Used**: – ITP's FBO pin should be connected to the processor's TCK pin. • Refer to Section 10.2.

Table 95. Processor Schematic Checklist (Sheet 3 of 5)

Checklist Items	Recommendations	Comments
TDI	• Pull up to VCCP with a 150 Ω resistor when an ITP700FLEX is not used. • Connect to ITP connector and pull-up to VCCP with a 150 Ω ± 1% resistor when an ITP700FLEX is used.	• **When ITP700FLEX Is Not Used**: – Parallel termination resistor required when neither the onboard ITP nor ITP interposer are planned to be used. • Refer to Section 10.2.
TDO	• No Connect when ITP700FLEX is not used. • Connect to ITP connector and pull-up to VCCP with a 54.9 Ω ± 1% resistor when an ITP700FLEX is used.	• **When ITP700FLEX Is Not Used**: – Leave the signal as NC (No Connect). • **When ITP700FLEX Is Used**: – Signal needs to be pulled-up to VCCP. • Refer to Section 10.2.
TRST#	• Pull-down to GND with 680 Ω ± 5% resistor when ITP700FLEX is not used. • Connect to ITP connector and Pull-down to GND with 510 Ω - 680 Ω ± 5%resistor when ITP700FLEX is used.	• **When ITP Is Not Used:** – Parallel termination resistor required when neither the onboard ITP nor ITP interposer are planned to be used. • **When ITP700FLEX Is Used**: – Parallel termination resistor may be placed anywhere between CPU and ITP700FLEX. • Refer to Section 10.2.
TMS	• Pull-up to VCCP with a 39 Ω ± 5% resistor when an ITP700FLEX is not used. • Connect to ITP connector and Pull-up to VCCP with a 39.2 Ω ± 1% when an ITP700FLEX is used.	• **When ITP700FLEX Is Not Used**: – Parallel termination resistor required when neither the onboard ITP nor ITP interposer are planned to be used. • Refer to Section 10.2.
ITP_CLK	• **When ITP700FLEX Is Not Used**: – No connection is required. • **When ITP700FLEX Is Used**: – Connect ITP_CLK[1:0] to CK408 CPUCLK pins through a 33 Ω ± 1% series resistor when an ITP interposer may be used.	Refer to Section 10.2.
DBR#	• No Connect when an ITP interposer may not be used. • Connect to ITP connector and Pull-up to VCCP with a 150 Ω ± 1% resistor.	• **When ITP700FLEX Is NOT Used**: – Signal should be routed from CPU socket to system reset logic. • **When ITP700FLEX Is Used**: – Pull up to VCCP. • Refer to Section 10.2.

Table 95. Processor Schematic Checklist (Sheet 4 of 5)

Checklist Items	Recommendations	Comments
Other Signals		
BCLK[1:0]	Connect to a 49.9 Ω 1% pull-down and to a series resistor (20 – 33 Ω). Connect other side of series resistor to CK408.	• System Bus Clock • Refer to Section 4.2. **NOTE:** BCLK[1:0] are processor pin names that are connected to clocks in the Host_CLK clock group on CK408.
COMP[3:0]	Terminate to GND separately using: • 27.4 Ω ± 1% for COMP0 and COMP2 pins. • 54.9 Ω ± 1% for COMP1 and COMP3 pins.	Refer to Section 5.1.8.
GTLREF[0]	GLTREF0 voltage divider should yield 2/3 of V_{CCP}. • Top divider resistor 1 K Ω ± 1% • Bottom divider resistor 2 K Ω ± 1%	Refer to Section 11.3.8.5.
GTLREF[3:1]	GTLREF[3:1] must be left as No Connects (NC).	Refer to Section 11.3.8.5.
THERMDA	Connect to temperature monitoring circuitry if used.	.
THERMDC	Connect to temperature monitoring circuitry if used.	
THERMTRIP#	• Connect to therm trip logic. • THERMTRIP# must disable the motherboard's power supply.	See schematics for circuitry used to connect THERMTRIP# pin to THERMTRIP logic.
TEST[3:2]	• No Connect. • For testing purposes each pin should have a stuffing option to be pulled down to V_{SS} through its own 1.2K Ω ± 5% resistor.	
TEST[1]	• Pull down to Vss through a 1.2K Ω ± 5% resistor.	
Reserved	Reserved signals must remain as No Connect (NC).	
Processor Power Signals		
VCC	Decoupling options exist depending on what type of capacitors are used	• For the list of different options refer to Section 11.3.8.3. • The Intel® Pentium® M processor contains 72 VCC pins.
VCCA[3:0]	Tie to 1.8 Volts. Decouple with four .01 µF ± 10% capacitors and four 10 µF ± 10% capacitors.	Refer to Section 11.3.1.
VCCP	Decouple with twelve 0.1 µF ± 10% capacitors and two 150 µF ± 10% capacitors	• Place all caps near the Processor. • The Intel Pentium M processor contains 25 VCC pins.
VCCSENSE	No Connect	For testing purposes, pull-down to GND through a 54.9 Ω ± 1% resistor only. Otherwise, leave as no connect.
Processor GND Signals		
VSS	Connect to GND	The Intel Pentium M processor contains 192 Vss pins.

Table 95. Processor Schematic Checklist (Sheet 5 of 5)

Checklist Items	Recommendations	Comments
VSSSENSE	No Connect	For testing purposes, pull-down to GND through a 54.9 Ω ± 1% resistor.
Processor Signals Not Supported By the Intel® E7501 Chipset		
DPWR#	• No Connect. • For testing purposes, a stuffing option should be provided to pull-up to VCCP through a 1 KΩ resistor	

NOTES:
1. A[31:3]# pins on the processor correspond to HA[31:3]# pins on the MCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the MCH.
3. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the MCH.
4. DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the MCH.
5. DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the MCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the MCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the MCH.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the MCH.
9. The DINV[3:0]# pins on the processor corresponds to the DBI[3:0]# pins on the MCH.

13.2 MCH Schematic Checklist

Table 96. MCH Schematic Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Comments
Host Interface Signals		
ADS# BNR# BPRI# BREQ0#[1] CPURST#[2] DBI[3:0]#[12] DBSY# DEFER# DRDY# HA[35:3]#[3] HD[63:0]#[4] HADSTB[1:0]#[5] HDSTBN[3:0]#[6] HDSTBP[3:0]#[7] HIT# HITM# HLOCK#[13] HREQ[4:0]#[8] HTRDY#[9] RS[2:0]# XERR#[10]	See processor section of this checklist.	
Signals Not Supported by the Intel® Pentium® M Processor		
AP[1:0] BINIT# DP[3:0]# RSP# HA[35:32]#	• Pull-up to V_{CCP} through a 1 K Ω ± 5% resistor. • See schematics for further details on stuffing options.	
DDR Interfaces A and B / Connector Signals		
DQ_x[63:0] CB_x[7:0] DQS_x[17:0]	Dependent upon configuration.	Refer to Section 6.4.2.
MA_x[12:0] BA_x[1:0] RAS_x# CAS_x# WE_x#	Terminate these signals to DDR VTERM (1.25 V).	Refer to Section 6.4.4.
CS_x[7:0]#	Terminate these signals to DDR VTERM (1.25 V).	Refer to Section 6.4.5.
CMDCLK_x[3:0] CMDCLK_x[3:0]#	Connect directly to the corresponding DIMM.	Signal Integrity. Refer to Section 6.4.3.
CKE_x	Terminate to DDR VTERM (1.25 V).	Refer to Section 6.4.6.
RCVEN_x#	Pull-up to DDRVTERM through a 49.9 Ω ± 1%. Refer to Figure 46.	Refer to Section 6.3.6.1.
DDRCOMP_x	Pull-down to GND through a 24.9 Ω ± 1% resistor.	Refer to Section 6.3.6.2.
DDRCVO_x	Connect as shown in Figure 51.	Refer to Section 6.3.6.4.

Table 96. MCH Schematic Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Comments
ODTCOMP	Pull-down to GND through a 402 Ω ± 1% resistor.	Refer to Section 6.3.6.3.
Hub Interface A Signals		
HI[11:0] HI_STBF[11] HI_STBS[11]	• Connect to the Intel® ICH3-S. • Must not have pull-up, pull-down, or series resistors.	Refer to Section 7.3.1.
HIRCOMP_A	• Tie the MCH RCOMP pin to a 24.9 Ω ± 1% pull-up to $V_{CC\_1.2}$ • (For Trace Impedance = 50 Ω ± 10%).	• Used to calibrate the I/O Buffers. • Resistive compensation is used by the Intel ICH3-S and MCH to adjust the buffer characteristics to specific board characteristic. • Refer to Section 7.3.3.
Hub Interface B, C, and D Signals		
HI[18:0]_x HI[21:20]_x PSTRBF_x PSTRBS_x PUSTRBF_x PUSTRBS_x	• Connect to Intel® P64H2. • Must **not** have pull-up, pull-down, or series resistors.	Refer to Section 7.2
HIRCOMP_B HIRCOMP_C HIRCOMP_D	• Tie the MCH RCOMP pins to a 24.9 Ω ± 1% pull-up to VCC_1.2 (For trace impedance = 50 Ω ± 10%). • Tie the Intel P64H2's RCOMP pin to 61.9 Ω ± 1%, pull-up to 1.8 V.	• Used to calibrate the I/O Buffers. • Resistive compensation is used by the Intel P64H2 and MCH to adjust the buffer characteristics to specific board characteristics. • Refer to Section 7.2.3.
Unused 16 bit interfaces	• All data, strobe, HISWNG_x, and HIRCOMP_x signals may be left as no connect. • HIVREF_[D:B] must be connected to ground.	• The MCH has integration detection logic that detects unpopulated 16-bit interfaces without external pull-ups and pull-downs. • Refer to Section 7.2.5.
Clocks and Reset Signals		
HCLKINP HLCKINN	Connect to CK408 through a 33 Ω ± 1% series resistor with a 49.9 Ω ± 1% pull-down resistor to ground.	Refer to Section 4.2.1.
CLK66	Connect to CK408 66BUF pin using a 43 Ω ± 5% series resistor.	Refer to Section 4.3
RSTIN#	Connect to PCIRST# output of the Intel ICH3-S.	
Miscellaneous Signals		
XORMODE#	4.7 kΩ ± 5% pull-up to VCC_3.3.	Required for normal operation.
Reserved (Pin B30)	4.7 kΩ ± 5% pull-up to VCC_3.3.	Required for normal operation.
Reserved (Pin D29)	1 kΩ ± 5% pull-down to GND.	Required for normal operation.

Table 96. MCH Schematic Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Comments
HXRCOMP HYRCOMP	Tie each COMP pin to a 24.9 Ω ±1% pull-down resistor to GND.	• This signal is used to calibrate the Host AGTL+ I/O buffer characteristics to specific board characteristics. • Refer to Section 5.1.8.2.
HXSWNG HYSWNG	Each signal has its own resistor divider circuit. See Figure 33 for circuitry information.	Refer to Section 5.1.8.2.
Unused Hub Interface Signals		
	• All data, strobe, HISWNG_x, and HIRCOMP_x signals may be left as no connect. • HIVREF_[D:A] must be connected to GND.	• The MCH has integration detection logic that may detect unpopulated 16-bit interfaces without external pull-ups and pull-downs. • Refer to Section 7.2.5.
Voltage References – Power Planes		
HDVREF[3:0] HAVREF[1:0] HCCVREF	• Use one dedicated voltage divider for all these signals. • Decouple the voltage divider with a 1 µF capacitor and use a 220 pF at the MCH pins.	• To provide constant and clean power delivery to the data, address and common clock signals of the host AGTL+ interface. • Refer to Section 11.3.8.5.
DDR_VREF_x[3:0]	Direct connect to DDR_Vref (1.25 V).	Refer to Section 6.3.6.3.
HXSWING HYSWING	• 150 Ω ±1% pull-down to GND. • 301 Ω ± 1% pull-up to CPU_VCC • C1 = C2 = 0.01 µF	The HXSWING and HYSWING inputs of MCH are used to provide reference voltage for the compensation logic. Refer to Section 5.1.8.
HISWNG_[D:A], HIVREF_[D:A]	Voltage divider circuit required. Refer to Figure 78 and Figure 81 for circuit information.	• The MCH 16-bit Hub Interfaces use a compensation voltage to control the buffer voltage characteristics. When multiple 16-bit Hub Interfaces are used, an HISWNG divider circuit may be shared among the interfaces as long as the trace length from the divider circuit is less than 3.5". • Refer to Section 7.2.2 and Section 7.3.2.
Voltage Sequencing Requirement		
1.2 V and 2.5 V	1.2 V must rise with or before 2.5 V.	Refer to Section 11.4.6.
Decoupling Requirements		
1.25 V (VTT_DDR)	Two 0.1 µF and two 0.01 µF caps.	Refer to Section 11.4.1.
CPU_VCC	Eighteen 0.1 µF caps	Refer to Section 11.4.2.
2.5 V (DDR)	Dual channel -twenty-eight 0.1 µF caps. Single channel - eighteen 0.1 µF caps.	Refer to Section 11.4.3.

Table 96. MCH Schematic Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Comments
1.2 V (Hub Interface)	Seven 0.1 µF caps.	Refer to Section 11.4.4.
VCCA1_2 VCCAHI1_2 VCCACPU_1.2	RLC filters.	Refer to Section 11.4.5.

NOTES:
1. The BREQ0# pin on the MCH corresponds to the BR0# pin on the processor.
2. The CPURST# pin on the MCH corresponds to the RESET# pin on the processor.
3. HA[35:3]# pins on the MCH correspond to A[31:3]# pins on the processor.
4. HD[63:0]# pins on the MCH correspond to D[63:0]# pins on the processor.
5. HADSTB[1:0]# pins on the MCH correspond to ADSTB[1:0]# pins on the processor.
6. HADSTBN[3:0]# pins on the MCH correspond to DSTBN[3:0]# pins on the processor.
7. HADSTBP[3:0]# pins on the MCH correspond to DSTBP[3:0]# pins on the processor.
8. HREQ[4:0]# pins on the MCH correspond to REQ[4:0]# pins on the processor.
9. The HTRDY# pin on the MCH corresponds to the TRDY# pin on the processor.
10. The MCH XERR# pin may be connected to the processor IERR# pin.
11. In HI1.0 mode, HI_STBF and HI_STBS used to be referred as HI_STB# and HI_STB respectively.
12. The DBI[3:0]# pins on the MCH correspond to DINV[3:0]# pins on the processor.
13. The HLOCK# pin on the MCH corresponds to the LOCk# pin on the processor.

13.3 Intel® ICH3-S Schematic Checklist

Note: No inputs to the Intel® ICH3-S may be left floating.

Table 97. Intel® ICH3-S Schematic Checklist (Sheet 1 of 8)

Checklist Items	Recommendations	Comments
Processor Signals		
A20M# CPUSLP# (SLP#) FERR# IGNNE# INIT# LINT1[1] LINT0[1] SMI# STPCLK#	Refer to the signal recommendations under the Processor Schematic Checklist.	
RCIN# A20GATE	Pull-up is required when driven by an open drain signal (the value of the resistor is determined by the driver).	Typically driven by Open Drain external Micro-controller.
CPUPWRGD	Recommend 300 Ω ± 5% pull-up to CPU_VCC. Connect to the processor and the Intel ICH3-S.	Asserted by the Intel® ICH3-S when all processor voltage supplies are stable.
FWH Interface Signals		
FWH[3:0]/ LAD[3:0] LDRQ[1:0]	No extra pull-ups required. Connect straight to FWH/LPC and, when supported, a BMC (Bus Management Controller).	The Intel ICH3-S integrates 24 kΩ pull-up resistors on these signal lines.
GPIO Signals		
GPIO[7:0]	• Unused core well inputs must be pulled up to VCC_3.3. • GPIO[1:0] may be used as REQ[B:A]#. • GPIO[1] may be used as REQ[5]#. • GPIO[5:2] may be used as PIRQ[H:E]#. • These signals are 5 V tolerant.	• These pins are in the Main Power Well. Pull-ups must use the VCC_3.3 plane. • Ensure all unconnected signals are **outputs only.**
GPIO[8] & [13:11]	• Unused resume well inputs must be pulled up to VCCSUS3.3. • These are the only GPIs that may be used as ACPI compliant wake events. • These signals are not 5 V tolerant. • GPIO[11] may be used as SMBALERT#.	• These pins are in the resume power well. Pull-ups go to VCCSUS3.3 plane. • These are the only GPI signals in the resume well with associated status bits in the GPE1_STS register.
GPIO[23:16]	• GPIO[22] is open drain. • GPIO[17:16] may be used as GNT[B:A]#. • GPIO[17] may be used as PCI GNT[5]#.	• Fixed as output only. May be left NC. • In main power well.
GPIO[28,27,25,24]	• I/O pins. Default as an output. May be left NC. • From resume power well (VCC_SUS3.3).	GPIO[26] is not implemented in the ICH3-S.

Table 97. Intel® ICH3-S Schematic Checklist (Sheet 2 of 8)

Checklist Items	Recommendations	Comments
GPIO[43:32]	From main power well (VCC_3.3).	• I/O pins. • Defaults as an output when enabled as GPIOs. • GPIO[31:29] is not implemented.
Hub Interface Signals		
HI[11:0] HI_STBS HI_STBF	No pull-up resistor required.	Refer to Section 7.3.1.
HICOMP	78.7 Ω ± 1% pull-up resistor to VCC_1.8.	Refer to Section 7.3.3.
HIREF HITERM	Divider circuit required. See Figure 82 for circuit information.	Refer to Section 7.3.2.
IDE Signals		
PDD[15:0] SDD[15:0]	No extra series termination resistors or other pull-ups/pull-downs are required.	• Refer to the ATA/ATAPI-6 specification. These signals have integrated series resistors. • Refer to Section 9.1.3. • Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω, but may range from 31 Ω to 43 Ω.
PDIOW# PDIOR# PDDACK# PDA[2:0] PDCS1# PDCS3# SDIOW# SDIOR# SDDACK# SDA[2:0] SDCS1# SDCS3#	No extra series termination resistors. Pads for series resistors may be implemented should the system designer have signal integrity concerns.	• These signals have integrated series resistors. • Refer to Section 9.1.3. • Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω, but may range from 31 Ω to 43 Ω.
PDREQ SDREQ	• No extra series termination resistors. • No pull-down resistors required.	• These signals have integrated series resistors in the ICH3-S. • These signals have integrated pull-down resistors in the ICH3-S. • Refer to Section 9.1.3.
PIORDY SIORDY	• No extra series termination resistors. • 4.7 kΩ ± 5% pull-up to 3.3 V	• These signals have integrated series resistors in the Intel ICH3-S. • Refer to Section 9.1.3.
IRQ14 IRQ15	• 8.2 kΩ – 10 kΩ pull-up resistors to 3.3 V • No extra series termination resistors.	• Open drain outputs from drive. • Refer to Section 9.1.3.
IDERST#	The PCIRST# signal should be buffered to form the IDERST# signal. A 22 – 47 Ω series resistor is recommended on this signal.	Refer to Section 9.1.3.

Table 97. Intel® ICH3-S Schematic Checklist (Sheet 3 of 8)

Checklist Items	Recommendations	Comments
Cable Detect	Connect IDE pin PDIAG#/CBLID# to an ICH3-S GPI pin. Connect a 10 kΩ resistor to ground on the signal line.	• The 10 kΩ resistor to GND prevents GPI from floating when no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. • Refer to Section 9.1.2.1. **NOTE:** All ATA66/ATA100 drives may have the capability to detect cables.
Interrupt Interface Signals		
APICCLK	Use 10 kΩ ± 5%pull-down resistor to GND.	
APICD[1:0]	Use 10 kΩ ± 5% pull-down resistor to GND.	
PIRQ[D:A]#	• These signals require a pull-up resistor. • 2.7 kΩ ± 5% pull-up to 5 V or an 8.2 kΩ ± 5% pull-up to 3.3 V.	Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: • PIRQ[A]# is connected to IRQ16. • PIRQ[B]# is connected to IRQ17. • PIRQ[C]# is connected to IRQ18. • PIRQ[D]# is connected to IRQ19. This frees the ISA interrupts.
PIRQ[H:E]#/ GPIO[5:2]	• These signals require a pull-up resistor. • 2.7 kΩ ± 5% pull-up to VCC_5 or an 8.2 kΩ ± 5% pull-up to 3.3 V.	These signals are connected to the internal I/O APIC in the following fashion: • PIRQ[E]# is connected to IRQ20. • PIRQ[F]# is connected to IRQ21. • PIRQ[G]# is connected to IRQ22. • PIRQ[H]# is connected to IRQ23. This frees the ISA interrupts.
SERIRQ	8.2 kΩ ± 5% pull-up to 3.3 V.	Open drain signal.

Table 97. Intel® ICH3-S Schematic Checklist (Sheet 4 of 8)

Checklist Items	Recommendations	Comments
LAN Interface Signals		
LAN_CLK	Connect to LAN_CLK on Platform LAN Connect Device.	• LAN connect interface signals may be left as NC if not used because the input buffers are internally terminated. • Refer to Section 9.7.
LAN_RXD[2:0]	Connect to LAN_RXD on Platform LAN Connect Device.	
LAN_TXD[2:0], LAN_RSTSYNC	Connect to LAN_TXD on Platform LAN Connect Device.	
Miscellaneous Signals		
SPKR	Has integrated pull-down.	• The integrated pull-down is enabled only at boot/ reset for strapping functions. At all other times, the pull-down is disabled. • Refer to Section 9.2.
TP[0]	8.2 kΩ – 10 kΩ pull-up to VCCSUS3.3.	
AC_SDOUT	No extra pull-down needed.	This pin has a weak internal pull-down.
EE_DOUT	• Connect to EE_DIN of EEPROM. (Input from EEPROM perspective and output from ICH3-S perspective.) • If unused, leave No Connect.	ICH3-S contains an integrated pull-up resistor for this signal.
EE_DIN	• Connect to EE_DOUT of EEPROM. (Ouput from EEPROM perspective and input from ICH3-S perspective.) • If unused, leave No Connect.	ICH3-S contains an integrated pull-up resistor for this signal.
PCI Interface Signals		
PERR# SERR# PLOCK# STOP# DEVSEL# TRDY# IRDY# FRAME# REQ#[4:0] GPIO[0]/REQ[A]# GPIO[1]/REQ[B]#/ REQ[5]#	8.2 kΩ ± 5% pull-up to 3.3 V, or a 2.7 kΩ ± 5% pull-up to 5 V.	
PCIRST#	Depending on the load this signal may have to be buffered.	Improves Signal Integrity.
GNT[4:0]#	No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented, they must be pulled up to 3.3 V.	These signals are actively driven by the Intel ICH3-S.
PME#	No extra pull-up resistor.	This signal has integrated pull-up of 18 kΩ to 42 kΩ.

Table 97. Intel® ICH3-S Schematic Checklist (Sheet 5 of 8)

Checklist Items	Recommendations	Comments
GNT[A]# GPIO[16] GNT[B]# GNT[5]# GPIO[17]	No extra pull-up needed.	• These signals have integrated pull-ups of 24 kΩ. • GNT[A] has an added strap function of 'top block swap'. The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A jumper to a pull-down resistor may be added to manually enable the function.
Power Signals		
V_CPU_IO	• Connect to CPU_VCC. • Use one 0.1 µF decoupling capacitor.	Refer to Section 11.5.4.
VCCRTC	• No clear CMOS jumper on VCCRTC. Use a jumper on RTCRST# or a GPI, or use a safe mode strapping for Clear CMOS. • Requires one 0.1 µF decoupling capacitor.	Refer to Section 11.5.4.
VCC3_3	Use six 0.1 µF decoupling capacitors.	Refer to Section 11.5.4.
VCCSUS3_3	Use two 0.1 µF decoupling capacitors.	Refer to Section 11.5.4.
VCC1_8	Use four 0.1 µF decoupling capacitors.	Refer to Section 11.5.4.
VCCSUS1_8	Use one 0.1 µF decoupling capacitor.	Refer to Section 11.5.4.
V5REF_SUS	• If USB is implemented in the platform, V5REF_Sus must be connected to VSUS5. • Use one 0.1 µF decoupling capacitor.	Refer to Section 11.5.4.
V5REF	Requires one 1.0 µF decoupling capacitor.	Refer to Section 11.5.4.
Power Sequencing Requirements		
V5REF_Sus and VCCSus3_3	V5REF_Sus must power up before or simultaneous to VCCSus3_3. It must power down after or simultaneous to VCCSus3_3. (For most platforms this sequencing is not an issues because VCCSus3_3 is derived from V5SUS.)	Refer to Figure 141 for an example circuit schematic that may be used to ensure the proper V5REF sequencing.
V5REF and VCC3_3	V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3.	Refer to Section 11.5.2.
VCC3_3 and VCC1_8	The difference between VCC3_3 and VCC1_8 must never be greater than 2.0 V.	Refer to Section 11.5.1.
VCCSus3_3 and VCCSus1_8	The difference between VCCSus3_3 and VCCSus1_8 must never be greater than 2.0 V.	Refer to Section 11.5.1.

Table 97. Intel® ICH3-S Schematic Checklist (Sheet 6 of 8)

Checklist Items	Recommendations	Comments
Power Management Signals		
THRM#	• Connect to temperature Sensor. • If not used: 8.2 kΩ ± 5% pull-up to 3.3 V.	Input to the Intel ICH3-S cannot float. THRM# polarity bit defaults THRM# to active low.
SLP_S3# SLP_S5#	No pull-up/down resistors needed. Signals driven by ICH3-S.	Signals driven by the Intel ICH3-S.
PWROK	• This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both 3.3 V and 1.8 V have reached their nominal voltages. • Use external weak pull-down.	Refer to Section 9.6.8.
PWRBTN#	Connect to a momentary switch tied to ground. No extra pull-up resistors.	This signal has an integrated pull-up of 18 kΩ – 42 kΩ.
RI#	8.2 kΩ ± 5% pull-up to VCCSUS3_3.	If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set, and the system will interpret that as a wake event.
RSMRST#	• May be tied to LAN_RST#. • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCCSUS3_3 and VCCSUS1.8 have reached their nominal voltages. • 10 kΩ ± 5% pull-down to ground.	Refer to Section 9.6.8.
SUS_STAT#	Disconnect from the Intel ICH3-S and leave not connected. Use 8.2 kΩ pull-up resistor to VCC_3.3 for remaining devices on LPC bus.	

Table 97. Intel® ICH3-S Schematic Checklist (Sheet 7 of 8)

Checklist Items	Recommendations	Comments
RTC Signals		
VBIAS	Use one 0.047 µF capacitor.	• For noise immunity on VBIAS signal. • Refer to Figure 116.
RTCRST		Refer to Section 9.6.8.
RTCX1 RTCX2	• Connect a 32.768 kHz Crystal Oscillator across these pins with a 10 MΩ resistor. Decouple each signal using a 18 pF capacitor. • RTCX1 may optionally be driven by an external oscillator instead of a crystal. These signals are 1.8 V only, and must not be driven by a 3.3 V source.	• The external circuitry shown in Figure 116 is required to maintain the accuracy of the RTC. • Refer to Section 9.6.1. • The circuitry is required because the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on the power supply of more than 100 mV may temporarily shut off the oscillator for hundreds of milliseconds. • Refer to Section 9.6.3 for decoupling requirements.
System Management Signals		
SMBDATA SMBCLK SMLINK[1:0]	• Connect SMBCLK to SMLink0 and SMBDATA to SMLink1. • Require external pull-up resistors, dependant upon bus capacitance and termination power plane.	• Refer to Section 9.5. • Value of pull-up resistors determined by line load, from Section 9.5.4.
SMBALERT#/ GPIO[11]	See GPIO section when SMBALERT# is not implemented.	
INTRUDER#	10 kΩ ± 5% pull-up to VCCRTC (VBAT) if not needed.	Refer to Section 9.6.8.

Table 97. Intel® ICH3-S Schematic Checklist (Sheet 8 of 8)

Checklist Items	Recommendations	Comments
USB Signals		
USBRBIAS	18.2 Ω ± 1% pull-down to ground.	
USBP[5:0]P USBP[5:0]N	No external resistors are required.	Integrated 15 kΩ pull-down, effective output driver impedance of 45 Ω provided.
OC[5:0]#	If not used: 10 kΩ ± 5% pull-up to VCCSUS3_3.	Inputs must not float.

NOTES:
1. LINT1 and LINT0 map to INTR and NMI in the ICH3-S.

13.4 Intel® 82870P2 (Intel P64H2) Schematic Checklist

Table 98. Intel® P64H2 Schematic Checklist (Sheet 1 of 5)

Checklist Items	Recommendations	Comments
Hub Interface Signals		
HI[21, 20, 18:0] PUSTRBF PUSTRBS PSTRBF PSTRBS	Connect to the MCH.	Refer to Section 7.2.1
HI_[19]	HI[19] must be left as no connect.	
HI_RCOMP	• 61.9 Ω ± 1% pull-up to 1.8 V. • The trace length between the Intel® P64H2 pin and the resistor lead should be less than one inch.	Refer to Section 7.2.3
HI_VREF HI_VSWING	• Intel P64H2 Hub reference swing voltage = 0.800 V ± 5%. • Intel P64H2 Hub reference voltage = 0.350 V ± 5%. • R4 = 261 Ω ± 1%, R5 = 332 Ω ± 1%, R6 = 750 Ω ± 1%. • Decouple the Intel P64H2 pin with a 0.01 µF. • Decouple the network nodes with a 0.1 µF	Refer to Section 7.2.2
PCI/PCI-X Bus Interface Signals		
PxAD[63:32] PxC/BE#[7:4] PxDEVSEL# PxFRAME# PxIRDY# PxTRDY# PxSTOP# PxPERR# PxSERR# PxREQ[5:0]# PxPLOCK# PxPAR64 PxACK64# PxREQ64#	• 8.2 kΩ ± 5% pull-up to 3.3 V. • Pull-ups on PxAD[63:32], PxC/BE#[7:4], PxPAR64 not needed if bus only contains 64-bit devices	See *PCI Specification*, Rev 2.2.
PAGNT3#	8.2 kΩ ± 5% pull-down to ground.	
PBGNT3#	8.2 kΩ ± 5% pull-down to ground.	
GNT[A]#/ GPIO[16] GNT[B]/ GNT[5]#/ GPIO[17]	No extra pull-up needed.	These signals have integrated pull-ups of 24 kΩ.
IDSEL	The series resistor to the device IDSEL should be 100 Ω. NOTE: The Intel P64H2 does not have an IDSEL pin. Instead, the designer may chose a pin from PxAD[31:17].	This has changed from the PCI-X 1.0 Specification. There is a specification change that allows for values other than the original 2 kΩ value.
3.3Vaux	Leave this as unconnected on the PCI slots.	The Intel P64H2 does not support PCI bus power management.

Table 98. Intel® P64H2 Schematic Checklist (Sheet 2 of 5)

Checklist Items	Recommendations	Comments
PxPCIXCAP	• If implementing hot plug, PxPCIXCAP should be pulled up to 3.3 V through an 8.2 kΩ resistor. • If not implementing hot plug, this signal requires 8.2 kΩ resistor pull-up or pull-down depending on the configuration.	If not implementing hot plug, see *PCI-X Specification* recommendations for PxPCIXCAP connection.
Px_133EN	• For 133 MHz (max) PCI-X capable bus: 8.2 kΩ ± 5% pull-up to 3.3 V. • For 100 MHz (max) PCI-X capable bus: 8.2 kΩ ± 5% pull-down to ground.	Only active if Px_PCIXCAP pins are high.
Interrupt Interface Signals		
PAIRQ[15:0] PBIRQ[15:0]	8.2 kΩ ± 5% pull-up to 3.3 V	
APICCLK APICD[1:0]	8.2 kΩ ± 5% pull-up to 3.3 V.	
Hot Plug Interface Enabled		
PxPCIXCAP	8.2 kΩ ± 5% pulled up to 3.3 V.	These PCI signals are connected to separate pins on the Intel® P64H2. See Section 8.2.7.3, and Section 8.2.8.4 for the corresponding Hot-Plug mode implementation. Unused inputs should not float.
M66EN	8.2 kΩ ± 5% pulled up to 3.3 V.	Unused inputs should not float.
HxSWITCH	Connect to MRL Sensor. Open MRL should pull HxSWITCH to 3.3 V. Closed MRL should pull HxSWITCH to GND.	Refer to Section 8.2.2.
HxPRSNT1# HxPRSNT2#	• 5.6 kΩ ± 5% pull-up to 3.3 V. • If implementing Attention Button, PRSNT1# is the XOR of the momentary push-button and Slot Present signal.	Refer to Section 8.2.2.
Hot Plug – Single Slot Parallel Mode Specific Signals		
HPx_SLOT[2:0]†	• SLOT[0]: 8.2 kΩ pull-up to 3.3 V. • SLOT[1]: 8.2 kΩ pull-down to GND. • SLOT[2]: 8.2 kΩ pull-down to GND.	• This is a strapping pin for enabling Single Slot Parallel Mode which is latched during reset. SLOT[1] also functions as the HxPCIXCAP2A input when not in reset. SLOT2 also functions as the HxPCIXCAP1A input when not in reset. • Refer to Section 8.2.6.1.
PxIRQ[14:8]†	8.2 kΩ ± 5% pull-up to 3.3 V.	These signals are mapped to hot plug functions in single slot hot plug mode.

Table 98. Intel® P64H2 Schematic Checklist (Sheet 3 of 5)

Checklist Items	Recommendations	Comments
PxIRQ[15]†	8.2Ω – 10 kΩ pull-up to 3.3 V.	A logic one on this pin indicates to the controller that the PCI slot should be immediately powered off. This signal is also connected to a SPST switch to GND which, when pressed, indicates by logic zero that the slot may be powered on.
Hot Plug – Dual Slot Parallel Mode Specific Signals		
HPx_SLOT[2:0]†	• SLOT[0]: 8.2 kΩ pull-down to GND. • SLOT[1]: 8.2 kΩ pull-up to VCC_3.3. • SLOT[2]: 8.2 kΩ pull-down to GND.	• This is a strapping pin for enabling Single Slot Parallel Mode which is latched during reset. SLOT[1] also functions as the HxPCIXCAP2A input when not in reset. SLOT2 also functions as the HxPCIXCAP1A input when not in reset. • Refer to Table 78.
PxIRQ[15]† PxIRQ[10]†	8.2 Ω – 10 kΩ pull-up to 3.3 V.	A logic one on this pin indicates to the controller that the PCI slot should be immediately powered off. This signal is also connected to a SPST switch to GND which when pressed indicates by logic zero that the slot may be powered on.
PxIRQ[9:8]† PxIRQ[14:11]†	8.2 kΩ ± 5% pull-up to 3.3 V.	These signals are mapped to hot plug functions in dual slot hot plug mode.
PPxSID†	8.2 kΩ ± 5% pull-down to ground.	This insures that the LED for slot B on busses A and B remain off during reset.
Hot Plug – Serial Mode Specific Signals		
HPx_SLOT[2:0]†	Pulled to VCC_3.3 or GND through a 8.2 kΩ ± 5% resistor depending on the number of PCI hot plug slots to be enabled.	The strapping pin list options for enabling Serial Mode is located in Table 78.
Hot Plug – Disabled Signals		
HPxSLOT[2:0]	8.2 kΩ ± 5% pull-down to ground.	• HPxSLOT[2:0] signals should be strapped to zero to disable hot plug mode. • See Table 76.
HPx_SID	8.2 kΩ ± 5% pull-up to 3.3 V or pull-down to ground.	Unused inputs should not float.
HPx_SIC HPx_SIL# HPx_SOR# HPx_SORR# HPx_SOC HPx_SOL HPx_SOLR HPx_SOD	If disabling hot plug mode, these signals may be left as no connect.	

Table 98. Intel® P64H2 Schematic Checklist (Sheet 4 of 5)

Checklist Items	Recommendations	Comments
PxPCIXCAP	This signal requires 8.2 kΩ resistor pull-up or pull-down depending on the configuration.	See *PCI-X Specification* recommendations for PxPCIXCAP connection.
SMBus Interface Signals		
SDTA SCLK	8.2 kΩ ± 5% pull-up to 3.3 V.	Value of pull-up resistors determined by line load, from Section 9.5.4.
Power Signals		
VCC (1.8 V)	• Connect to 1.8 V power supply. • Decoupling: – 8 X 0.1 µF capacitors near the Intel® P64H2. – 2 X 4.0 µF capacitors near regulator.	Refer to Section 11.6.2.
VCC1.8	• Connect to 1.8 V Power Supply. • Decoupling: – 2 X 1.0 µF capacitors near the Intel P64H2. – 1 X 100.0 µF capacitors near regulator.	Refer to Section 11.6.2.
VCC3.3	Connect to 3.3 V Power Supply. Decoupling: • 20 0.1 µF capacitors near the Intel P64H2. • 6 X 1.0 µF capacitors near the Intel P64H2. • 2 X 4.7 µF capacitors near regulator. • 1 X 100.0 µF capacitors near regulator.	Refer to Section 11.6.2.
VCC5REF	Connect to 5 V Power Supply.	5 V
Power Sequencing Requirements		
1.8 V and CLK66	1.8 V must be valid before first CLK66 pulse.	Refer to Section 11.6.4.
1.8 V and 3.3 V	1.8 V must drop before 3.3 V.	Refer to Section 11.6.4.
PWRGD to PCIRST#	• PCIRST# must lag PWRGD by 100 ms. • PCIRST# must deassert with 60 ns of MCH reset.	Refer to Section 11.6.4.
Miscellaneous Signals		
BPCLK100 BPCLK133	These may be left as no connects.	
CLK200 CLK200#	When not used, pull-up to VCC3.3 with a 8.2 kΩ ± 5% resistor.	
BPCLK100 BPCLK133	These may be left as no connects.	
CLK200 CLK200#	8.2 kΩ ± 5% pull-up to 3.3 V.	
TP0	8.2 kΩ ± 5% pull-up to VCC3.3.	
RSTIN#	Connect to the PCIRST# output of the Intel ICH3-S.	Reset In. When asserted, this signal asynchronously resets the Intel P64H2 logic and asserts PCIRST# active output from each PCI interface.

Table 98. Intel® P64H2 Schematic Checklist (Sheet 5 of 5)

Checklist Items	Recommendations	Comments
TEST#	8.2 kΩ ± 5% pull-up to VCC3.3.	
RASERR#	8.2 kΩ ± 5% pull-up to VCC3.3.	

† x = A or B

13.5 CK408 Schematic Checklist

For additional information, refer to the *CK408 Clock Synthesizer/Driver Specification* and your component's datasheet.

Table 99. CK408 Schematic Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Reason/Impact
V3_CLK, V3_CLKA	Isolate from the 3.3 V power plane and use extra decoupling.	Refer to Section 4.7.
66BUFF[2:0]	Connect to the Intel® P64H2 using a series 43 Ω ± 5% resistor.	Refer to Section 4.3.
66IN	No Connect.	
3V66_0	Connect to the Intel® ICH3-S using a series 43 Ω ± 5% resistor.	Refer to Section 4.3.
3V66_1_VCH	Connect to MCH using a series 43 Ω ± 5% resistor.	Refer to Section 4.3.
CPU[3:0] CPU[3:0]#	• Connect to the processor, MCH, or ITP using a series 33 Ω ± 5% resistor, and terminate to GND through a 49.9 Ω ± 1% resistor. • Unused Clock outputs: 10K Ω ± 5% pull-up to VCC3.3.	Refer to Section 4.2.
DOT_48MHz	No Connect.	
IREF	475 Ω ± 1% pull-down to ground.	
MULT0	10 kΩ ± 5% pull-up to V3_CLK.	
PCI[4:0]	Connect to a series 33 Ω ± 5% resistor for PCI33_CLK33, VIDEO_CLK33, FWH_CLK33, SIO_CLK33, and LPC_CLK33.	Refer to Section 4.5.
PCI[6:5]	No Connect.	
PCIF[0]	Connect to a series 33 Ω ± 5% resistor for ICH3_CLK33.	Refer to Section 4.4.
PCIF[2:1]	No Connect.	
PCI_STOP#	10 kΩ ± 5% pull-up to V3_CLK.	
PWRDWN#	Connect to SLP_S3_N.	
REF0	Connect to a series 22 Ω ± 5% resistor for CLK 14 output to LPC, VIDEO, SIO and ICH3-S.	Refer to Section 4.6.
FS[0]	10 kΩ ± 5% pull-down to ground.	See schematic for reference circuit.
FS[1]	10 kΩ ± 5% pull-down to ground.	
SCLK, SDTA	Connect to the 3 V SMBus partition.	
USB_48MHz	Connect to the Intel ICH3-S using a 33 Ω ± 5% series resistor to ICH3_CLK48.	Refer to Section 4.7.
VDD, VDD_48MHz, VDDA	Terminate to V3_CLK_A.	Refer to Section 4.9.

Table 99. CK408 Schematic Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Reason/Impact
VSS, VSS_48MHz, VSS_IREF	Terminate to GND.	Refer to Section 4.9.
VTT_PWRGD#	1 kΩ ± 5% pull-down to ground.	
XTAL_IN XTAL_OUT	• Connect XTAL_IN to pin 1 of the crystal oscillator and to a 10 pF capacitor to ground. • Connect XTAL_out to pin 2 of the crystal oscillator and to a 10 pF capacitor to ground.	

Layout Checklist 14

All trace width and spacing recommendations are derived from a target impedance and crosstalk sensitivity. This is based upon the stackup defined in Section 3.1. Any deviation from this stackup must be simulated.

14.1 Processor Checklist

Table 100. Processor Layout Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Comments
Intel® Pentium® M General Layout Recommendations		
General Guidelines	• Maintain the same ground reference when transitioning layers—add stitching vias when reference plane changes. • Group like signals together under the processor such as ground, 1.2 V, 2.5 V, etc. • Ensure power and ground fills are placed directly under the processor. • Minimize signal parallelism • Do not share vias. • Maintain trace width. Do not neck-down • Ensure signals do not cross adjacent layer plane splits. • Connect termination resistors directly to termination plane (flood is on outer layer). • Ensure package compensation is factored into the trace lengths.	• Refer to Section 12.9.1. • Refer to Section 12.9.2. • Refer to Section 12.9.3. • Refer to Section 12.9.4. • Refer to Section 12.9.5. • Refer to Section 12.9.6. • Refer to Section 12.7.1.
Intel® Pentium® M Processor Side Bus (PSB) Interface Signals		
A[31:3]#[1] ADSTB[1:0]#[2] DSTBN[3:0]#[3] DSTBP[3:0]#[4] DINV[3:0]#[9] D[63:0]#[5] REQ[4:0]#[6]	• Trace impedance = 50 Ω ± 10%. • Route all signals within the same strobe group on the same layer (do not change layer), and balance within group ± 25 mils with respect to the strobe. • The distance from processor pad to MCH pad is between three inches and 7.5 inches. • Do not route signals on adjacent layers parallel to each other for more than 0.5 inch.	• Balance signal lengths within each strobe group. Refer to Section 5.1. • AGTL+ Source Synchronous I/O. • Refer to Section 12.9.3.

Table 100. Processor Layout Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Comments
ADS# BINIT# BNR# BPM[3:0]# BR0# DBSY# DRDY# HIT# HITM# LOCK# MCERR# BPRI# DEFER# RESET#[7] RS[2:0]# TRDY#[8]	• Trace impedance = 50 Ω ± 10%. • Route traces using 5/15 mils (1:3) spacing. • Route signals on same layer. If this is not possible, a minimum of one ground stitching via for every two signals should be place within 100 mils of the signals transition vias. • Route traces with at least 50% of the trace width directly over a reference plane. • The distance from processor pad to MCH pad is between three inches and 7.5 inches.	• AGTL+ Common Clock Signals. • Refer to Section 5.1. • Ensure package compensation is factored into the trace lengths. Refer to Section 12.7.1.
ICH3-S Interface Signals		
A20M# IGNNE# INIT# LINT0/INTR LINT1/NMI SMI# SLP#	• Connect to the processor and the Intel® ICH3-S. • Trace impedance = 50 Ω ± 10%. • Route traces using 5/10 mils (1:2) spacing. • Try to keep signals on the same layer for the whole bus, but not at expense of AGTL+ Source Synchronous I/O. • Maximum agent to agent length is 12 inches. Place pull-up resistor within three inches of Processor.	• Asynchronous GTL+ Input Signals. • Refer to Section 5.1.7.
PSI# STPCLK#	• Connect to the processor and the Intel ICH3-S. • Trace impedance = 50 Ω ± 10%. • Route traces using 5/10 mils (1:2) spacing. • Try to keep signals on the same layer for the whole bus, but not at expense of AGTL+ SS I/O. • Maximum agent to agent length is nine inches. Place pull-up resistor within three inches of Processor. • Series dampening resistor placed within two inches of the Intel ICH3-S pin.	See Section 5.1.7.1.5.
FERR#/PBE# IERR# PROCHOT# THERMTRIP#	• Connect to the processor and the Intel ICH3-S. • Trace impedance = 50 Ω ± 10%. • Route traces using 5/15 mils (1:3) spacing. • Try to keep signals on the same layer for the whole bus, but not at expense of AGTL+ SS I/O. • Maximum agent to agent length is ten inches. Place pull-up resistor within three inches of the processor and the Intel ICH3-S.	• Async GLT+ Output. • Refer to Section 5.1.7.1.2.
IERR#	• If IERR# is used: • Series resistor should be placed near the system receiver and between the receive and termination resistor.	See Section 5.1.7.1.1.

Table 100. Processor Layout Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Comments
Processor In Target Probe (ITP) Signals		
BPM[3:0]# PRDY# PREQ#	**When ITP700FLEX Is Used**: Point to point connection to CPU pin through a Zo = 50 Ω trace.	**When ITP700FLEX Is Used**: Point to point connection to CPU pin. **ITP700FLEX** to **CPU** BPM[3:0]# BPM[3:0]# BPM4# PRDY# BPM5# PREQ#
TCK	**When ITP700FLEX Is Used**: Parallel termination resistor placed within ± 200 ps of ITP700FLEX connector.	
TDI	**When ITP700FLEX Is Used**: Parallel termination resistor placed within ± 300 ps of CPU pin.	
TDO	**When ITP700FLEX Is Used**: Series dampening resistor is placed within one inch of ITP700FLEX connector.	
TRST#	• **When ITP Is Not Used:** – Parallel termination resistor placed within two inches of the CPU pin. This is required when neither the onboard ITP nor ITP interposer are planned to be used. • **When ITP700FLEX Is Used**: – Parallel termination resistor may be placed anywhere between CPU and ITP700FLEX. Avoid any trace stub from signal line to parallel termination resistor.	
TMS	• **When ITP700FLEX Is Not Used**: – Parallel termination resistor placed within two inches of the CPU pin. This is required when neither the onboard ITP nor ITP interposer are planned to be used. • **When ITP700FLEX Is Used**: – Parallel termination resistor placed within ± 200 ps of CPU pin.	
Other Signals		
BCLK, BCLK#	Compliments should be length matched to the processor and MCH. The MCH's BCLK, BCLK# signals should be offset accordingly. See Table 7.	• System Bus Clock • Refer to Section 4.2.

Table 100. Processor Layout Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Comments
Processor Power and GND Signals		
VCCA[3:0]	• To satisfy damping requirements, total series resistance in the filter (from CPU_VCC to the top plate of the capacitor) must be at least 0.35 Ω. It includes the minimum DCR of the inductor, and any resistance (routing or discrete components) between CPU_VCC and capacitor top plate. • The total maximum resistance cannot be greater than 1.1 Ω as measured from VCC (more specifically, the baseboard via that connects the PLL filter to the VCC plane) to the processor VCCA interposer pin. Also, maximum trace resistance from the filter capacitor to processor socket pin should be less than 0.02 Ω.	• An isolated power for internal PLL. • Refer to Section 11.3.1.
VCCSENSE VSSSENSE	• Route traces using 5/15 mils (1:3) spacing. • Place via next to the processor socket's pin for measurement of CPU_VCC/VSS.	

NOTES:
1. A[31:3]# pins on the processor correspond to HA[31:3]# pins on the MCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the MCH.
3. DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the MCH.
4. DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the MCH.
5. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the MCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the MCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the MCH.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the MCH.
9. DINV[4:0]# pins on the processor correspond to DBI[4:0]# pins on the MCH.

14.2 Intel® E7501 MCH Layout Checklist

Table 101. Intel® E7501 Chipset MCH Layout Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Comments
Intel® E7501 Chipset MCH General Layout Recommendations		
General Guidelines	• 5 on 15 mils (1:3) spacing is maintained for Data/Strobe/CMD signals; 5 on 7.5 mils (1:1.5) spacing is maintained for CMDCLK_x/CMDCLK_x# signals. • When using the recommended stack-up, outer layer routing of DDR signals should be kept to a minimum (except for reference voltages). Via up close to passive devices, and immediately via back down following the device. • Try to maintain same ground reference when transitioning layers—add stitching via when reference plane changes. • Connect termination resistors directly to termination plane (flood is on outer layer). • Space traces out as much as possible through the DIMMs. • Group like signals together under the MCH such as ground, 1.2 V, 2.5 V, etc. • Ensure power and ground fills are placed directly under the processor. • Minimize signal parallelism • Do not share vias. • Maintain trace width. Do not neck-down. • Ensure signals do not cross adjacent layer plane splits. • Connect termination resistors directly to termination plane (flood is on outer layer). • Ensure package compensation is factored into the trace lengths.	• Refer to Section 12.9.1. • Refer to Section 12.9.2. • Refer to Section 12.9.3. • Refer to Section 12.9.4. • Refer to Section 12.9.5. • Refer to Section 12.9.6.

Table 101. Intel® E7501 Chipset MCH Layout Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Comments
Host Interface Signals		
ADS# BNR# BPRI# BREQ0#[1] CPURST#[2] DBSY# DEFER# HA[31:3]#[3] HD[63:0]#[4] HADSTB[1:0]#[5] HDSTBN[3:0]#[6] HDSTBP[3:0]#[7] HIT# HITM# HLOCK#[12] HREQ[4:0]#[8] HTRDY#[9] DRDY# RS[2:0]# XERR#[10] DBI[3:0]#[11]	See processor section of this checklist.	
DDR Interfaces A and B Connector Signals		
DQ_x[63:0] CB_x[7:0] DQS_x[17:0]	• Route entirely on the same layer from MCH to DIMM to termination (no layer transitions). Place the series resistor < 800 mils from the first DIMM connector. • All signals in a data group must be length matched to the associated DQS within ± 25 mils. • Place termination resistor within 800 mils from the last DIMM connector for 1- to 3-DIMM designs, 4-DIMM design is 0.3 inch to 1.3 inches.	• For dual channel, refer to Section 6.3.1. • For single channel, refer to Section 6.4.2.
RAS_x# CAS_x# WE_x# MA_x[12:0] BA_x[1:0]	• Place termination resistor within 800 mills from last DIMM connector for 1- to 3-DIMM designs, 4-DIMM design is 0.3 inch to 1.3 inches. • No more than two vias/layer transitions, not including breakout and passive devices.	• For dual channel, refer to Section 6.3.3. • For single channel, refer to Section 6.4.4.
CS_x[7:0]#	Place termination resistor within 1.5 inches from the connector.	• For dual channel, refer to Section 6.3.4. • For single channel, refer to Section 6.4.5.
CMDCLK_x[3:0] CMDCLK_x[3:0]#	Clock signals within a differential pair must be matched to each other within ± 2 mils. These signals must be routed 5 on 7.5, and must be at least 20 mils away from any other signal. Use exact lengths as defined in Table 34 or Table 44.	• For dual channel, refer to Section 6.3.2. • For single channel, refer to Section 6.4.3.

Table 101. Intel® E7501 Chipset MCH Layout Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Comments
CKE_x	• Route 40 Ω using a 7.5 mils wide trace. • The CKE signal must be length matched to the clock signal at each DIMM within two inches. • Place termination resistor within 800 mils from last DIMM connector. When routing creates stubs, keep the stub length less than 300 mils.	• For dual channel, refer to Section 6.3.5. • For single channel, refer to Section 6.4.6.
RCVEN_x#	Route 50 Ω using a 5-mil wide trace with 15-mil wide spacing. Use topology in Table 38 or Table 48.	• For dual channel, refer to Section 6.3.6.1. • For single channel, refer to Section 6.4.7.1.
DDRCOMP_x	Route 15 mils wide trace with 20 mils wide spacing. Place pull-up resistor within one inch of the MCH.	• For dual channel, refer to Section 6.3.6.2. • For single channel, refer to Section 6.4.7.2.
DDRCVO_x	Route 15 mils wide trace with 20 mils wide spacing. Place resistive network within one inch of the MCH.	• For dual channel, refer to Section 6.3.6.4. • For single channel, refer to Section 6.4.7.4.
DDRVREF_x[3:0]	Place a 0.1 µF capacitor next to each MCH pin.	• For dual channel, refer to Section 6.3.6.3. • For single channel, refer to Section 6.4.7.3.
Decoupling	• Spread termination decoupling capacitors evenly around the termination plane. • Spread 2.5 V decoupling capacitors evenly around the DIMMs.	• For dual channel, refer to Section 6.3.7. • For single channel, refer to Section 6.4.8.
Hub Interface		
General Guidelines	• Hub interface data spacing of 5 /15 (1:3) is maintained for data, and 5/35 (1:7) for strobes. • Space signals out as much as possible on breakout from the BGA. • Hub interface data group signals are routed on the same layer, transitioning together when a layer change is required. • Maximum length of 20 inches (stripline routing). • Length match Hub Interface 2.0 strobes within one inch from data. Length match according to Figure 75. • Hub Interface 1.5: Length match data ± 100 mils and strobes ± 1mil.	Refer to Section 7.2.1 and Section 7.3.1 of this document.

Table 101. Intel® E7501 Chipset MCH Layout Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Comments
Clocks and Reset Signals		
HCLKINP HLCKINN	HCLKs should be length matched to the processor's BCLK. See Table 7 for routing guidelines.	Refer to Section 4.2.
CLK66	Place series resistor close to CK408.	Refer to Section 4.3.
RSTIN#	Connect to PCIRST# output of the Intel® ICH3-S.	
Miscellaneous Signals		
HIRCOMP_x HIVREF_[D:A] HISWNG_[D:A]	• RCOMP, VSWING, VREF resistor networks are less than one inch away from the MCH. • VSWING, VREF trace width is greater than 15 mils. • HIRCOMP_x must have a 50 Ω impedance.	Refer to Section 7.2.2, Section 7.2.3, Section 7.3.2, and Section 7.3.3.
HXRCOMP HYRCOMP	Ensure trace impedance = 50 ohms.	This signal is used to calibrate the Host AGTL+ I/O buffers characteristics to specific board characteristic.
XORMODE#	No layout requirements.	This signal is used to put the MCH outputs in XOR-mode for board level testing.
Voltage References – Power Planes		
HDVREF[3:0] HAVREF[1:0] HCCVREF	Use one dedicated voltage divider for all these signals. Decouple the voltage divider with a 1 µF capacitor.	• To provide constant and clean power delivery to the data, address, and common clock signals of the host AGTL+ interface. • Refer to Section 11.3.8.5.
HXSWNG HYSWNG	No layout requirements.	The HXSWNG and HYSWNG inputs of MCH are used to provide reference voltage for the compensation logic.
VCCA	High-frequency decoupling for VCCA planes is located as close as possible to the associated MCH pin.	

NOTES:
1. The BREQ0# pin on the MCH corresponds to the BR0# pin on the processor.
2. The CPURST# pin on the MCH corresponds to the RESET# pin on the processor.
3. HA[35:3]# pins on the MCH correspond to A[31:3]# pins on the processor.
4. HD[63:0]# pins on the MCH correspond to D[63:0]# pins on the processor.
5. HADSTB[1:0]# pins on the MCH correspond to ADSTB[1:0]# pins on the processor.
6. HADSTBN[3:0]# pins on the MCH correspond to DSTBN[3:0]# pins on the processor.
7. HADSTBP[3:0]# pins on the MCH correspond to DSTBP[3:0]# pins on the processor.
8. HREQ[4:0]# pins on the MCH correspond to REQ[4:0]# pins on the processor.
9. The HTRDY# pin on the MCH corresponds to the TRDY# pin on the processor.
10. The MCH XERR# pin may be connected to the processor IERR# pin.
11. The DBI[3:0]# pins on the MCH correspond to DINV[3:0]# pins on the processor.
12. The HLOCK# pin on the MCH correspond to LOCK# pin on the processor.

14.3 Intel® ICH3-S Layout Checklist

Table 102. Intel® ICH3-S Layout Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Comments
Processor Signals		
A20M# CPUSLP# FERR# IGNNE# INIT# LINT[1:0] SMI# STPCLK#	See processor section of this checklist.	
FWH Interface		
Decoupling	• 0.1 µF capacitors should be placed between the VCC supply balls and the VSS ground balls. The capacitors should be within 390 mils from the VCC supply balls. • 4.7 µF capacitors should be placed between the VCC supply balls and the VSS ground balls, and no less than 390 mils from the VCC supply balls.	
Hub Interface - See MCH section		
IDE Checklist		
General Guidelines	• Traces are routed 5 mils wide with 7 mils spacing. • Max trace length is eight inches long. • The maximum length difference between the longest and shortest trace length is 0.5 inches.	• Refer to ATA ATAPI-4 specification. • Refer to Section 9.1.3.
LAN Interface		
General Guidelines	Traces: 5 mils wide, 10 mils spacing.	Refer to Section 9.7.
	LAN Max Trace Length ICH3-S to CNR: L = Three inches to nine inches (0.5 inch to three inches on card).	To meet timing requirements.
	Stubs due to R-pak CNR/LOM stuffing option should not be present.	To minimize inductance.
	Maximum Trace Lengths: • Intel® ICH3-S to Intel® 82562EH: L = 4.5 inches to 10 inches. • Intel® 82562ET: L = 3.5 inches to ten inches • Intel® 82562EM: L = 3.5 inches to ten inches	To meet timing requirements.
	Maximum mismatch between the length of a clock trace and the length of any data trace is 0.5 inch (clock must be the longest trace).	To meet timing and signal quality requirements.

Table 102. Intel® ICH3-S Layout Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Comments
General Guidelines	Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN phy.	To meet timing and signal quality requirements.
	Keep the total length of each differential pair under four inches.	Issues found with traces longer than four inches. See Section 9.7.2.1. • IEEE phy conformance failures • Excessive EMI and or degraded receive BER.
	Do not route the transmit differential traces closer than 100 mils to the receive differential traces.	To minimize crosstalk.
	Distance between differential traces and any other signal line must be at least 100 mils. (300 mils is recommended.)	To minimize crosstalk.
	Route 5 mils on 7 mils for differential pairs (out of LAN phy).	To meet timing and signal quality requirements.
	Differential trace impedance should be controlled to be ~100 Ω.	To meet timing and signal quality requirements.
	For high-speed signals, the number of corners and vias should be kept to a minimum. When a 90-degree bend is required, use two 45-degree bends.	To meet timing and signal quality requirements.
	Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
	Do not route traces and vias under crystals or oscillators.	This prevents coupling to or from the clock.
	Trace width to height ratio above the ground plane should be between 1:1 and 3:1.	To control trace EMI radiation.
	Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.
	Vias to decoupling capacitors should be sufficiently large in diameter.	To decrease series inductance.
	Isolate I/O signals from high speed signals.	To minimize crosstalk.
	Avoid routing high-speed LAN or Phone line traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar device.	To minimize crosstalk.
	Place the Intel® 82562EM / Intel® 82562ET component more than 1.5 inches away from any board edge.	This minimizes the potential for EMI radiation problems.
	Place at least one bulk capacitor (4.7 µF or greater OK) on each side of the Intel 82562EM / Intel 82562ET component.	Research and development has shown that this is a robust design recommendation.
	Place decoupling capacitors (0.1 µF) as close to the Intel 82562EM / Intel 82562ET component as possible.	

Table 102. Intel® ICH3-S Layout Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Comments
Power Decoupling		
V_CPU_IO[2:0]	Use one 0.1 µF decoupling capacitor. Locate within 100 mils of the Intel ICH3-S processor interface balls.	Used to pull-up all processor I/F signals.
VCC_3.3	Requires six 0.1 µF decoupling capacitors. Distribute around the Intel ICH3-S package sides within 100 mils from the package balls: • Top near AUX/PCI • Left across the PCI and LPC • Bottom near IDE	
VCCSUS_3.3	Requires two 0.1 µF decoupling capacitors. Place one capacitor on the top side within 200 mils of the USB center. Place other on bottom side near the VCCSus3_3 supply.	
VCC_1.8	Requires four 0.1 µF decoupling capacitors. Locate two capacitors distributed local to the Hub Interface; within 50 mils of the package Hub Interface balls. Distribute remaining capacitors on the left and bottom sides of the package for core delivery.	
VCCSUS_1.8	Requires one 0.1 µF decoupling capacitor. Locate within 200 mils of balls B23 and C23 of the ICH3-S.	
V5_REF_SUS	Requires one 0.1 µF decoupling capacitor. V5_REF_Sus affects only 5 V tolerance for USB OC[5:0]# balls, and may be connected to VCCSus3_3 when 5 V tolerance on these signal is not required.	
V5_REF	Requires one 0.1 µF decoupling capacitor. V5REF is the reference voltage for 5 V tolerant inputs in the ICH3-S. Tie to balls V5REF[2:1]. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3.	
General Guidelines	• Group like signals together under the ICH such as ground, 1.8 V, 3.3 V, etc. • Ensure power and ground fills are placed directly under the ICH.	• Refer to Section 12.9.1. • Refer to Section 12.9.2.
RTC		
General Guidelines	• RTC pin to crystal termination trace length should be less than one inch. • Minimize capacitance between RTCX1 and RTCX2. • Put ground plane underneath crystal components. • Do not route switching signals under the external components (unless on other side of board).	

Table 102. Intel® ICH3-S Layout Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Comments
USB		
General Guidelines	• Route all traces over continuous planes (ground) with no interruptions. Avoid crossing over anti-etch when possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.) • Keep traces at least 50 mils away from the edge of the reference ground plane. This helps prevent the coupling of the signal onto adjacent wires, and helps prevent free radiation of the signal from the edge of the PCB. • Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. • Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 20 mils, though it is recommended to keep clocks and PCI traces at least 50 mils from the USB differential pairs when possible. • Use 20 mils minimum spacing between USB signal pairs and other signal traces. This helps to prevent crosstalk. • USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pair (such as USBP2P and USBP2N) should be no greater than 150 mils. • No termination resistors needed for USB. The Intel ICH3-S has internal 15 kΩ resistors. • 47 pF parallel capacitors may be placed as close to the USB connector as possible.	

14.4 Intel® P64H2 Layout Checklist

Table 103. Intel® P64H2 Layout Checklist

Checklist Items	Recommendations	Reason/Impact
Hub Interface	See MCH Hub Interface section of this checklist.	
PCI-X Interface	See Section 8.1 for complete list of topologies and lengths.	
General Guidelines	• Group like signals together under the Intel® P64H2 such as ground, 1.8 V, 3.3 V, etc. • Ensure power and ground fills are placed directly under the Intel P64H2.	• Refer to Section 12.9.1. • Refer to Section 12.9.2.

Schematics A

The following schematics for the Intel® Pentium® M processor/Intel® E7501 chipset compatible platform Customer Reference Board (CRB) are included in this section.

- System Block Diagram
- Processor Socket
- MCH Pullups
- Thermal Monitors
- Processor Decoupling
- ITP, Processor Pullups
- MCH System Bus
- MCH Hub Interface
- MCH DDR Interface
- MCH Power/Ground
- DDR A Series Resistors
- DDR A DIMMs
- DDR A Termination
- DDR B Series Resistors
- DDR B DIMMs
- DDR B Termination
- P64H2 #1
- P64H2 #2
- P64H2 #1 PCI Pullups
- P64H2 #2 PCI Pullups
- PCI-X Slot 1A
- PCI-X Slot 1B
- PCI-X Slots 2A, 2B, 2C
- PCI-X Slot 2D and VXB Connector
- ICH
- USB and IDE Connectors
- 32-Bit PCI Slot (Debug)
- PCI Video
- 2.5 V and VTT_DDR Power Regulation
- 1.8 V Power Regulation

- Power Connector and Power OK Circuit
- CPUVCC Regulator
- CK-408B
- FWH, LPC Connector (Debug)
- SIO, Legacy I/O
- 1.2 V Regulation
- LAN Controller and Connector
- SCSI Controller, Connectors, and Termination
- Mounting Holes
- VCCP Regulation
- SMBUS Mux Logic
- Front Panel and BMC Connectors
- Spare Gates
- Port 80

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE

INTEL(R) PENTIUM(R) M PROCESSOR / INTEL(R) E7501 CHIPSET PLATFORM REFERENCE SCHEMATICS

REV A2.1

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NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

BOM RELEASE DATE		PB NUMBER	
SIGNATURE	DATE	intel CORPORATION 5000 W CHANDLER BLVD CHANDLER, AZ 85226	
DRN BY			
CHK BY		TITLE	
ENGR APVD			
APVD			PAGE 1/82 / REV A2.1
APVD			

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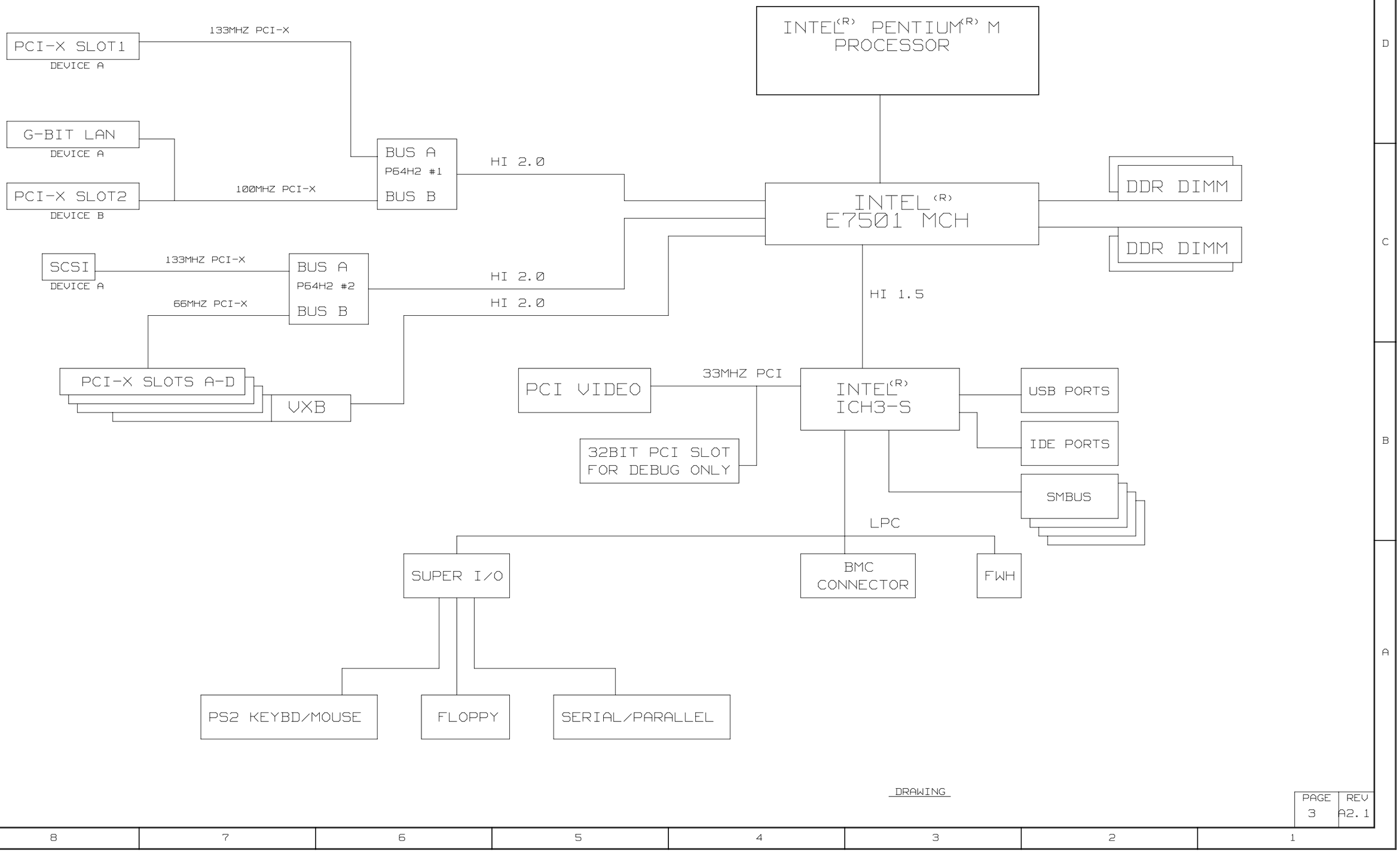
SYSTEM BLOCK DIAGRAM



DRAWING

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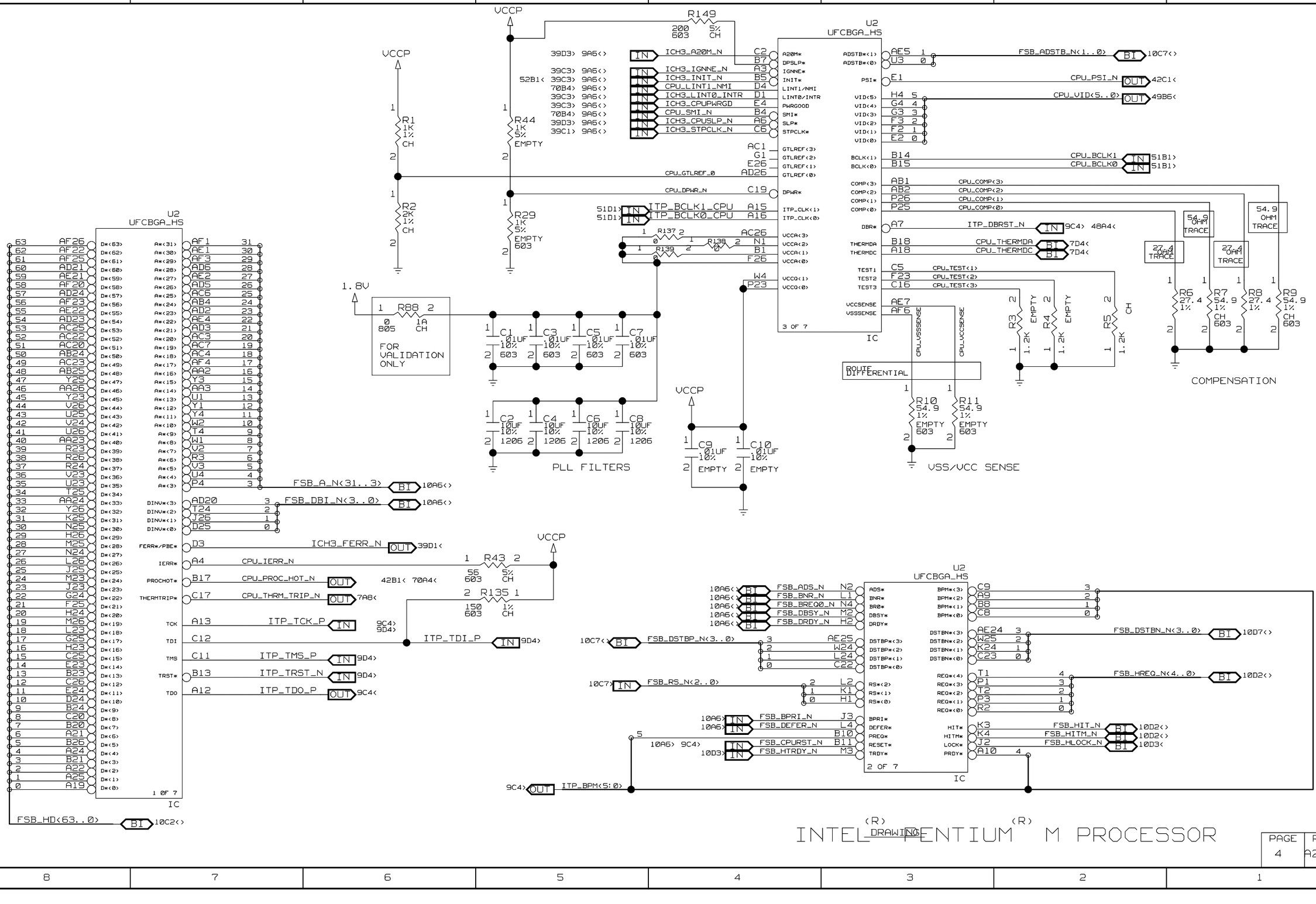

(R) (R)
INTEL PENTIUM M PROCESSOR

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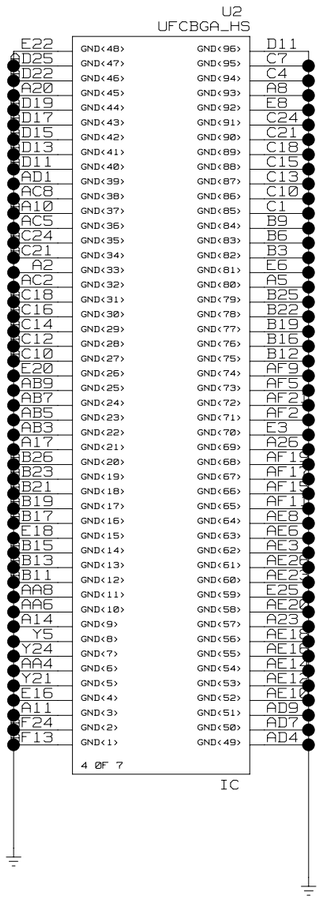
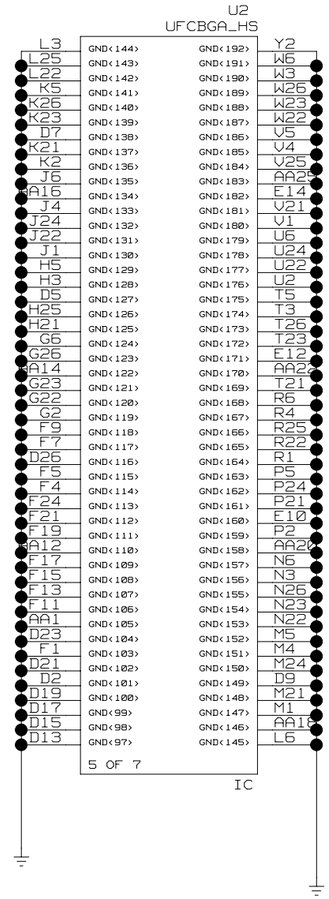
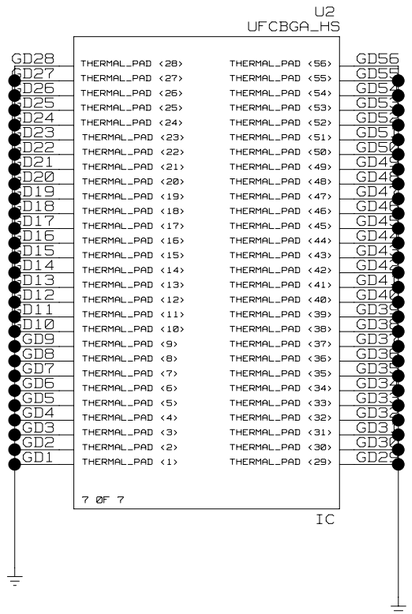
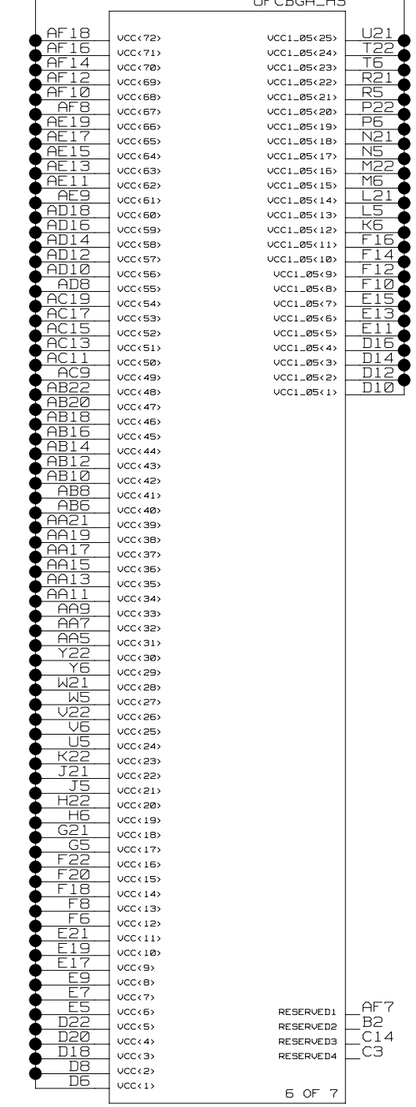






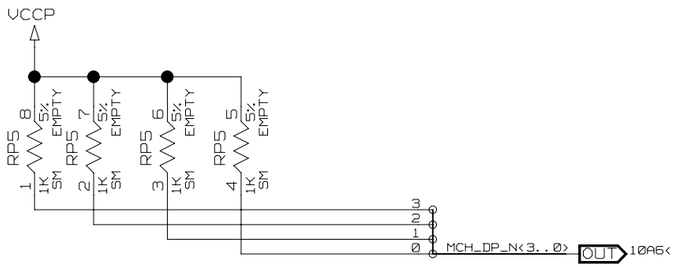
CPUVCC

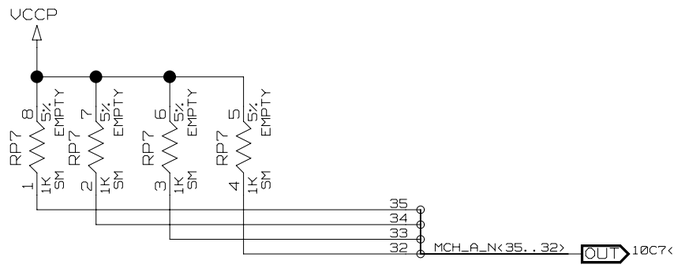
VCCP

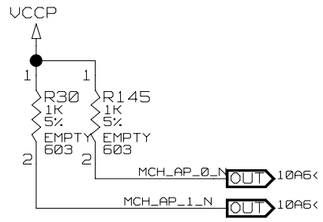


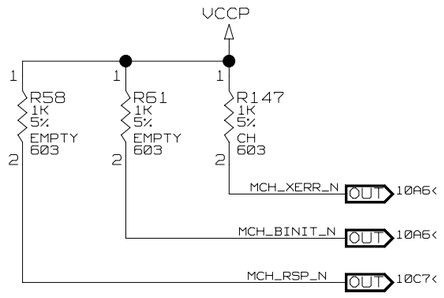
DRAWING

PAGE	REV
5	A2.1









MCH PULL-UP RESISTORS

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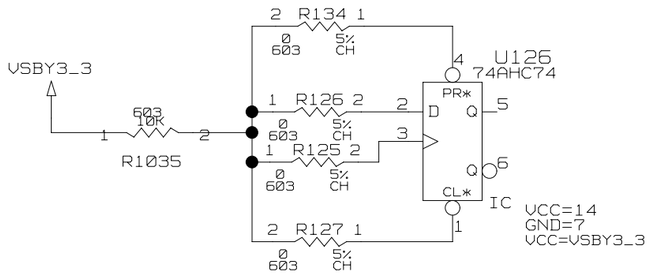

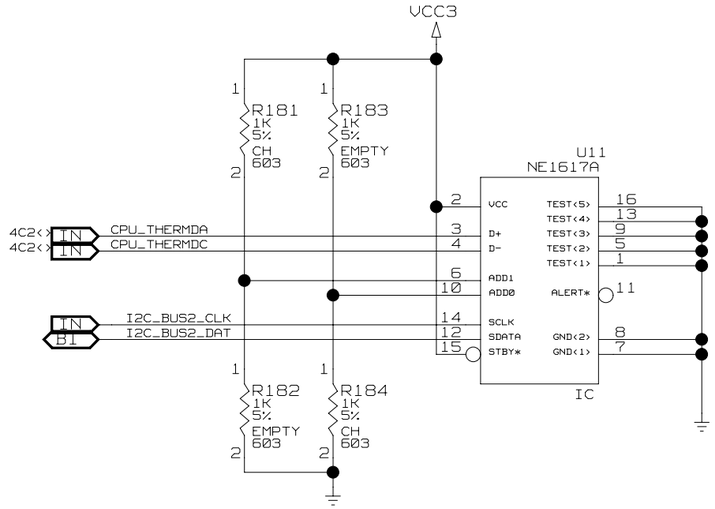

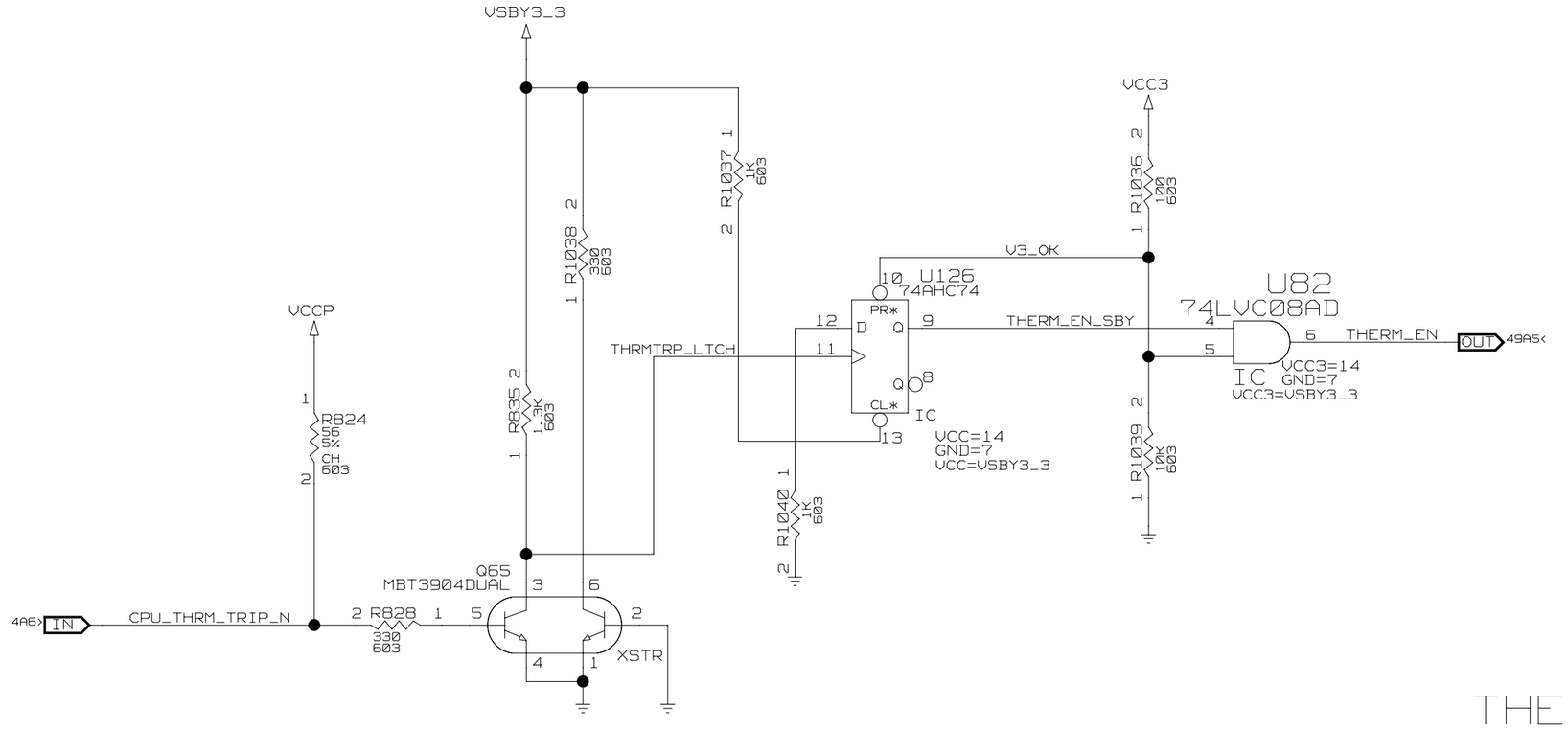

THERMTRIP LATCH LOGIC

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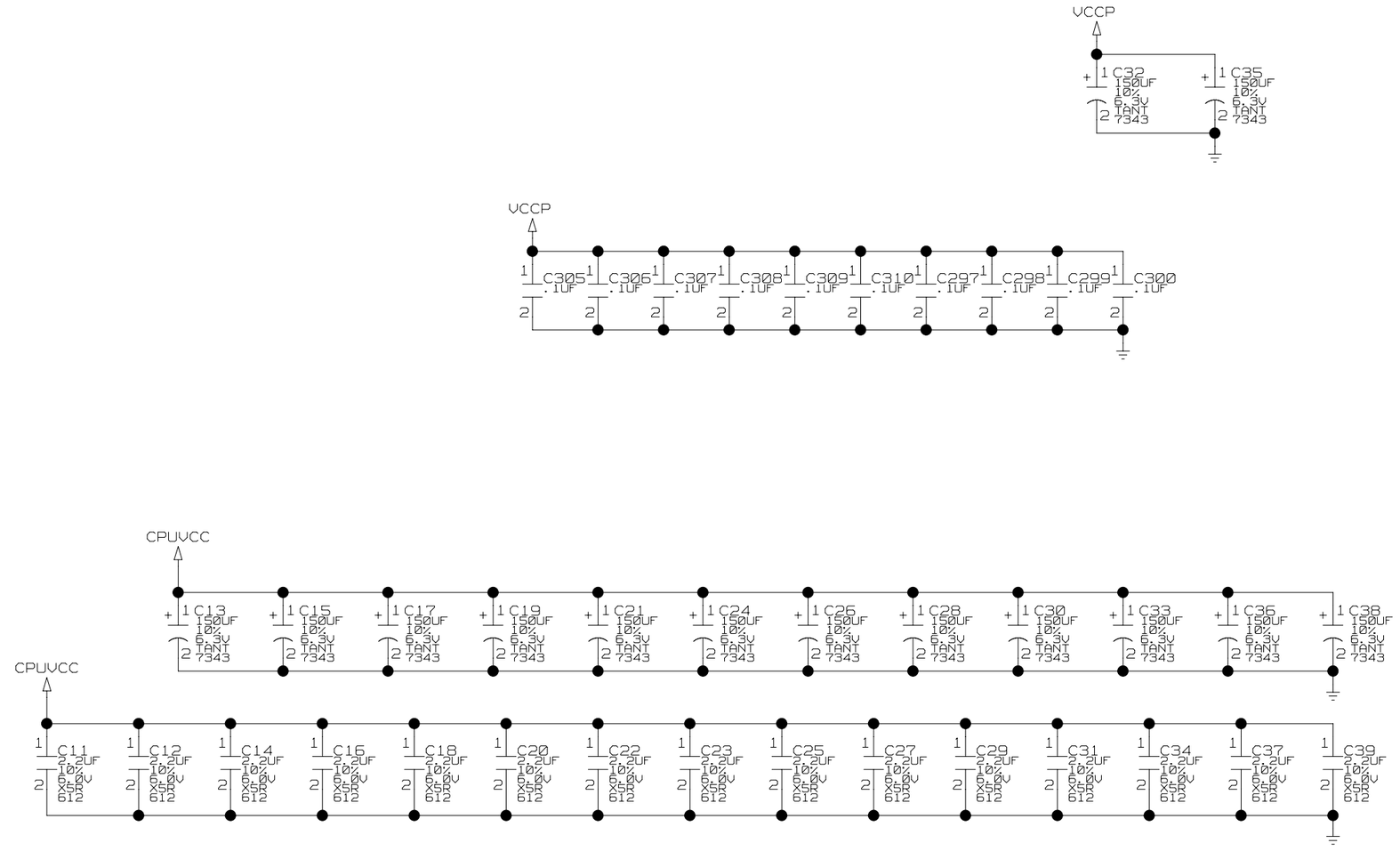

PROCESSOR DECOUPLING

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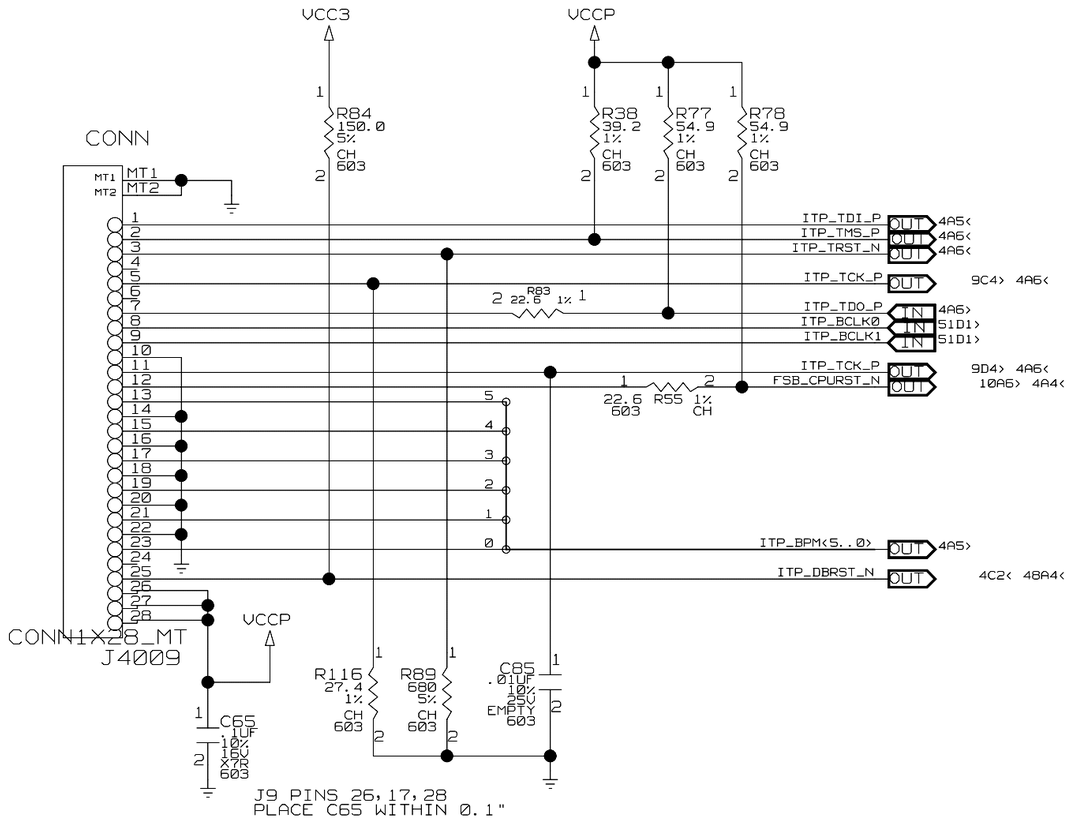

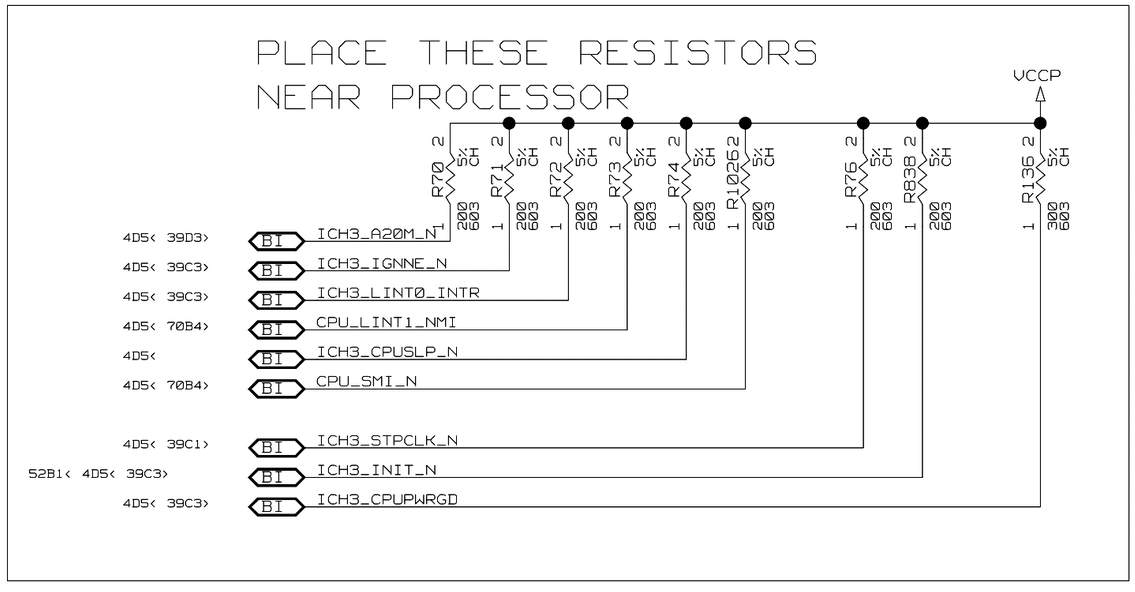

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PAGE	REV
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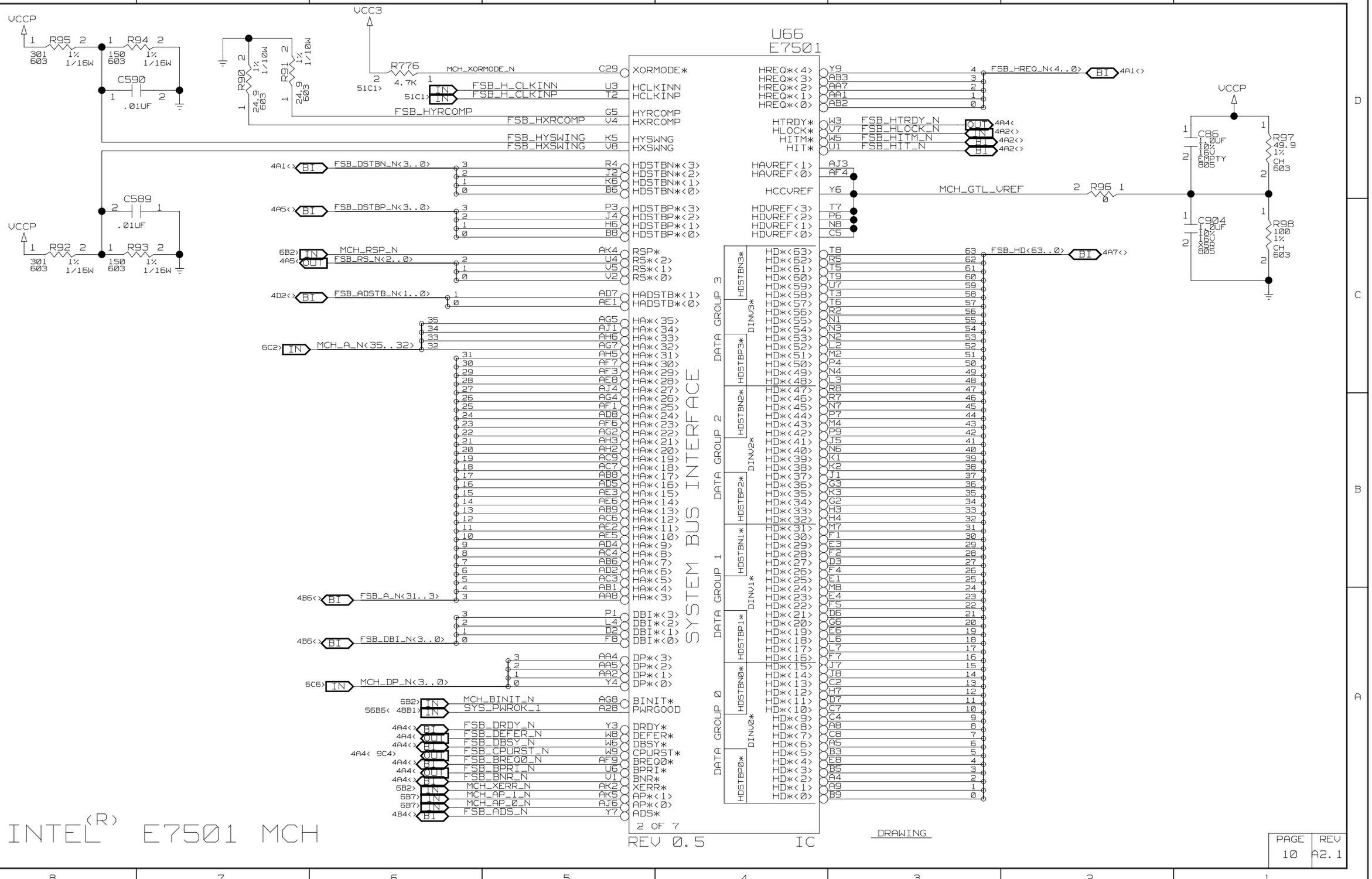
VCCP
R95 301 1% 1/16W
R94 150 1% 1/16W
C590 .01UF
VCC3
R776 4.7K
MCH_XORMODE_N
FSB_H_CLKINN
FSB_H_CLKINP
R90 24.9 1% 1/10W
R91 24.9 1% 1/10W
FSB_HYRCOMP
FSB_HXRCOMP
FSB_HYSWING
FSB_HXSWING
C589 .01UF
R92 301 1% 1/16W
R93 150 1% 1/16W
U66
E7501
XORMODE*
HCLKINN
HCLKINP
HYRCOMP
HXRCOMP
HYSWING
HXSWING
FSB_DSTBN_N<3..0>
HDSTBN*<3>
HDSTBN*<2>
HDSTBN*<1>
HDSTBN*<0>
FSB_DSTBP_N<3..0>
HDSTBP*<3>
HDSTBP*<2>
HDSTBP*<1>
HDSTBP*<0>
MCH_RSP_N
FSB_RS_N<2..0>
RSP*
RS*<2>
RS*<1>
RS*<0>
FSB_ADSTB_N<1..0>
HADSTB*<1>
HADSTB*<0>
MCH_A_N<35..32>
HA*<35>
HA*<34>
HA*<33>
HA*<32>
HA*<31>
HA*<30>
HA*<29>
HA*<28>
HA*<27>
HA*<26>
HA*<25>
HA*<24>
HA*<23>
HA*<22>
HA*<21>
HA*<20>
HA*<19>
HA*<18>
HA*<17>
HA*<16>
HA*<15>
HA*<14>
HA*<13>
HA*<12>
HA*<11>
HA*<10>
HA*<9>
HA*<8>
HA*<7>
HA*<6>
HA*<5>
HA*<4>
HA*<3>
FSB_A_N<31..3>
FSB_DBI_N<3..0>
DBI*<3>
DBI*<2>
DBI*<1>
DBI*<0>
MCH_DP_N<3..0>
DP*<3>
DP*<2>
DP*<1>
DP*<0>
MCH_BINIT_N
SYS_PWROK_1
BINIT*
PWRGOOD
FSB_DRDY_N
FSB_DEFER_N
FSB_DBSY_N
FSB_CPURST_N
FSB_BREQ0_N
FSB_BPRI_N
FSB_BNR_N
MCH_XERR_N
MCH_AP_1_N
MCH_AP_0_N
FSB_ADS_N
DRDY*
DEFER*
DBSY*
CPURST*
BREQ0*
BPRI*
BNR*
XERR*
AP*<1>
AP*<0>
ADS*
2 OF 7
SYSTEM BUS INTERFACE
REV 0.5
IC
HREQ*<4>
HREQ*<3>
HREQ*<2>
HREQ*<1>
HREQ*<0>
FSB_HREQ_N<4..0>
HTRDY*
HLOCK*
HITM*
HIT*
FSB_HTRDY_N
FSB_HLOCK_N
FSB_HITM_N
FSB_HIT_N
HAVREF<1>
HAVREF<0>
HCCVREF
HDVREF<3>
HDVREF<2>
HDVREF<1>
HDVREF<0>
MCH_GTL_VREF
R96 0
C86 1.0UF
R97 49.9 1% CH 603
C904 1.0UF
R98 100 1% CH 603
FSB_HD<63..0>
DATA GROUP 3
DATA GROUP 2
DATA GROUP 1
DATA GROUP 0
HDSTBN3*
HDSTBP3*
HDSTBN2*
HDSTBP2*
HDSTBN1*
HDSTBP1*
HDSTBN0*
HDSTBP0*
DINV3*
DINV2*
DINV1*
DINV0*
HD*<63>
HD*<62>
HD*<61>
HD*<60>
HD*<59>
HD*<58>
HD*<57>
HD*<56>
HD*<55>
HD*<54>
HD*<53>
HD*<52>
HD*<51>
HD*<50>
HD*<49>
HD*<48>
HD*<47>
HD*<46>
HD*<45>
HD*<44>
HD*<43>
HD*<42>
HD*<41>
HD*<40>
HD*<39>
HD*<38>
HD*<37>
HD*<36>
HD*<35>
HD*<34>
HD*<33>
HD*<32>
HD*<31>
HD*<30>
HD*<29>
HD*<28>
HD*<27>
HD*<26>
HD*<25>
HD*<24>
HD*<23>
HD*<22>
HD*<21>
HD*<20>
HD*<19>
HD*<18>
HD*<17>
HD*<16>
HD*<15>
HD*<14>
HD*<13>
HD*<12>
HD*<11>
HD*<10>
HD*<9>
HD*<8>
HD*<7>
HD*<6>
HD*<5>
HD*<4>
HD*<3>
HD*<2>
HD*<1>
HD*<0>
INTEL(R) E7501 MCH
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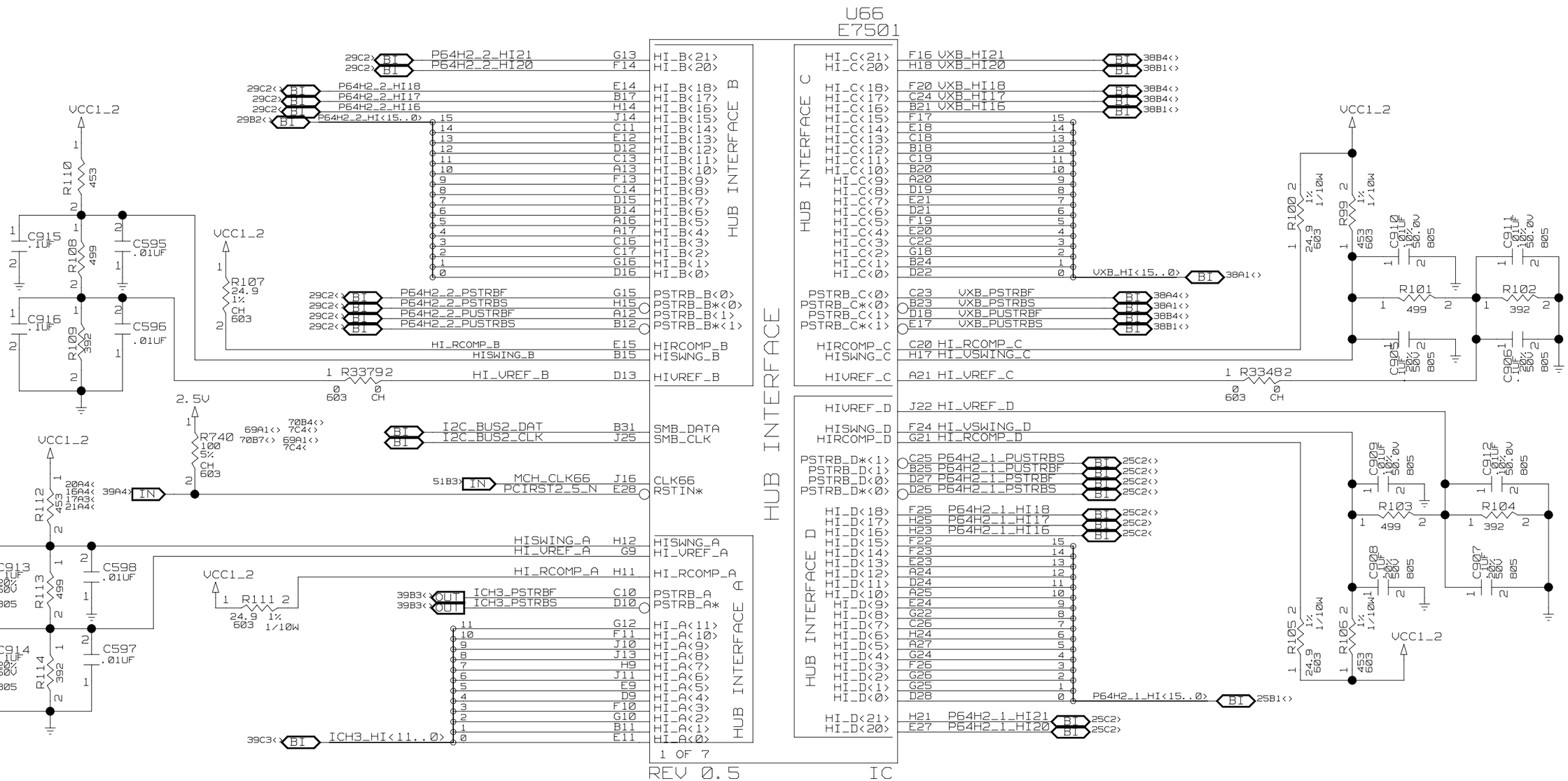
U66
E7501
HUB INTERFACE B
HUB INTERFACE A
HUB INTERFACE C
HUB INTERFACE D
HUB INTERFACE
HI_B<21> G13 P64H2_2_HI21
HI_B<20> F14 P64H2_2_HI20
HI_B<18> E14 P64H2_2_HI18
HI_B<17> B17 P64H2_2_HI17
HI_B<16> H14 P64H2_2_HI16
HI_B<15> J14 P64H2_2_HI<15..0>
HI_B<14> C11
HI_B<13> E12
HI_B<12> D12
HI_B<11> C13
HI_B<10> A13
HI_B<9> F13
HI_B<8> C14
HI_B<7> D15
HI_B<6> B14
HI_B<5> A16
HI_B<4> A17
HI_B<3> C16
HI_B<2> C17
HI_B<1> G16
HI_B<0> D16
PSTRB_B<0> G15 P64H2_2_PSTRBF
PSTRB_B*<0> H15 P64H2_2_PSTRBS
PSTRB_B<1> A12 P64H2_2_PUSTRBF
PSTRB_B*<1> B12 P64H2_2_PUSTRBS
HIRCOMP_B E15 HI_RCOMP_B
HISWING_B B15
HIVREF_B D13 HI_VREF_B
SMB_DATA B31 I2C_BUS2_DAT
SMB_CLK J25 I2C_BUS2_CLK
CLK66 J16 MCH_CLK66
RSTIN* E28 PCIRST2_S_N
HISWNG_A H12
HI_VREF_A G9
HI_RCOMP_A H11
PSTRB_A C10 ICH3_PSTRBF
PSTRB_A* D10 ICH3_PSTRBS
HI_A<11> G12
HI_A<10> F11
HI_A<9> J10
HI_A<8> J13
HI_A<7> H9
HI_A<6> J11
HI_A<5> E9
HI_A<4> D9
HI_A<3> F10
HI_A<2> G10
HI_A<1> B11
HI_A<0> E11
ICH3_HI<11..0>
1 OF 7
REV 0.5
IC
HI_C<21> F16 VXB_HI21
HI_C<20> H18 VXB_HI20
HI_C<18> F20 VXB_HI18
HI_C<17> C24 VXB_HI17
HI_C<16> B21 VXB_HI16
HI_C<15> F17
HI_C<14> E18
HI_C<13> C18
HI_C<12> B18
HI_C<11> C19
HI_C<10> B20
HI_C<9> A20
HI_C<8> D19
HI_C<7> E21
HI_C<6> D21
HI_C<5> F19
HI_C<4> E20
HI_C<3> C22
HI_C<2> G18
HI_C<1> B24
HI_C<0> D22
VXB_HI<15..0>
PSTRB_C<0> C23 VXB_PSTRBF
PSTRB_C*<0> B23 VXB_PSTRBS
PSTRB_C<1> D18 VXB_PUSTRBF
PSTRB_C*<1> E17 VXB_PUSTRBS
HIRCOMP_C C20 HI_RCOMP_C
HISWNG_C H17 HI_VSWING_C
HIVREF_C A21 HI_VREF_C
HIVREF_D J22 HI_VREF_D
HISWNG_D F24 HI_VSWING_D
HIRCOMP_D G21 HI_RCOMP_D
PSTRB_D*<1> C25 P64H2_1_PUSTRBS
PSTRB_D<1> B25 P64H2_1_PUSTRBF
PSTRB_D<0> D27 P64H2_1_PSTRBF
PSTRB_D*<0> D26 P64H2_1_PSTRBS
HI_D<18> F25 P64H2_1_HI18
HI_D<17> H25 P64H2_1_HI17
HI_D<16> H23 P64H2_1_HI16
HI_D<15> F22
HI_D<14> F23
HI_D<13> E23
HI_D<12> A24
HI_D<11> D24
HI_D<10> A25
HI_D<9> E24
HI_D<8> G22
HI_D<7> C26
HI_D<6> H24
HI_D<5> A27
HI_D<4> G24
HI_D<3> F26
HI_D<2> G26
HI_D<1> G25
HI_D<0> D28
P64H2_1_HI<15..0>
HI_D<21> H21 P64H2_1_HI21
HI_D<20> E27 P64H2_1_HI20
VCC1_2
2.5V
R110 453
R108 499
R109 392
R107 24.9 1% CH 603
R740 100 5% CH 603
R112 453
R113 499
R114 392
R111 2 24.9 1% 1/10W 603
R33792 0 603 CH
R33482 0 603 CH
R100 2 24.9 1% 1/10W 603
R99 2 453 1% 1/10W 603
R105 2 24.9 1% 1/10W 603
R106 2 453 1% 1/10W 603
R101 499
R102 392
R103 499
R104 392
C915 .1UF
C595 .01UF
C916 .1UF
C596 .01UF
C913 .1UF 20% 50V 805
C598 .01UF
C914 .1UF 20% 50V 805
C597 .01UF
C910 .01UF 10% 50.0V 805
C911 .01UF 10% 50.0V 805
C905 .1UF 10% 50V 805
C909 .01UF 10% 50.0V 805
C912 .01UF 10% 50.0V 805
C908 .1UF 10% 50V 805
C907 .1UF 10% 50V 805
IN
OUT
BI
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E7501 MCH

U66
E7501

MCH DDR

15C8<	B1	DDRA_DQ63	AM4	DQ_A<63>
15C8<	B1	DDRA_DQ62	AL5	DQ_A<62> HIGH NIBBLE
15B8<	B1	DDRA_DQ61	AE11	DQ_A<61> DATA GROUP 8
15B8<	B1	DDRA_DQ60	AH10	DQ_A<60>
15C8<	B1	DDRA_DQS16	AH9	DQS_A<16>
15C8<	B1	DDRA_DQS7	AL6	DQS_A<7>
15C8<	B1	DDRA_DQ59	AM2	DQ_A<59>
15C8<	B1	DDRA_DQ58	AM3	DQ_A<58> LOW NIBBLE
15C8<	B1	DDRA_DQ57	AJ9	DQ_A<57> DATA GROUP 8
15C8<	B1	DDRA_DQ56	AG10	DQ_A<56>
15B8<	B1	DDRA_DQ55	AM6	DQ_A<55>
15B8<	B1	DDRA_DQ54	AM9	DQ_A<54> HIGH NIBBLE
15A8<	B1	DDRA_DQ53	AF12	DQ_A<53> DATA GROUP 7
15B8<	B1	DDRA_DQ52	AG12	DQ_A<52>
15B8<	B1	DDRA_DQS15	AM7	DQS_A<15>
15B8<	B1	DDRA_DQS6	AL8	DQS_A<6>
15B8<	B1	DDRA_DQ51	AN5	DQ_A<51>
15B8<	B1	DDRA_DQ50	AG11	DQ_A<50> LOW NIBBLE
15B8<	B1	DDRA_DQ49	AH11	DQ_A<49> DATA GROUP 7
15B8<	B1	DDRA_DQ48	AE12	DQ_A<48>
15A8<	B1	DDRA_DQ47	AM10	DQ_A<47>
15A8<	B1	DDRA_DQ46	AJ12	DQ_A<46> HIGH NIBBLE
15A8<	B1	DDRA_DQ45	AF13	DQ_A<45> DATA GROUP 6
15C8<	B1	DDRA_DQ44	AE15	DQ_A<44>
15A8<	B1	DDRA_DQS14	AK12	DQS_A<14>
15A8<	B1	DDRA_DQS5	AM12	DQS_A<5>
15A8<	B1	DDRA_DQ43	AL11	DQ_A<43>
15A8<	B1	DDRA_DQ42	AN12	DQ_A<42> LOW NIBBLE
15A8<	B1	DDRA_DQ41	AH13	DQ_A<41> DATA GROUP 6
15C8<	B1	DDRA_DQ40	AE14	DQ_A<40>
15C8<	B1	DDRA_DQ39	AG14	DQ_A<39>
15A8<	B1	DDRA_DQ38	AH14	DQ_A<38> HIGH NIBBLE
15D5<	B1	DDRA_DQ37	AN13	DQ_A<37> DATA GROUP 5
15D5<	B1	DDRA_DQ36	AK14	DQ_A<36>
15A8<	B1	DDRA_DQS13	AJ13	DQS_A<13>
15A8<	B1	DDRA_DQS4	AL13	DQS_A<4>
15C8<	B1	DDRA_DQ35	AF15	DQ_A<35>
15A8<	B1	DDRA_DQ34	AJ15	DQ_A<34> LOW NIBBLE
15D5<	B1	DDRA_DQ33	AM13	DQ_A<33> DATA GROUP 5
15D5<	B1	DDRA_DQ32	AL14	DQ_A<32>
15D8<	B1	DDRA_DQ31	AJ19	DQ_A<31>
15C5<	B1	DDRA_DQ30	AN21	DQ_A<30> HIGH NIBBLE
15C5<	B1	DDRA_DQ29	AJ21	DQ_A<29> DATA GROUP 4
15C5<	B1	DDRA_DQ28	AH20	DQ_A<28>
15C5<	B1	DDRA_DQS12	AK20	DQS_A<12>
15C5<	B1	DDRA_DQS3	AE18	DQS_A<3>
15D8<	B1	DDRA_DQ27	AL20	DQ_A<27>
15C5<	B1	DDRA_DQ26	AM21	DQ_A<26> LOW NIBBLE
15C5<	B1	DDRA_DQ25	AH19	DQ_A<25> DATA GROUP 4
15C5<	B1	DDRA_DQ24	AF19	DQ_A<24>
15B5<	B1	DDRA_DQ23	AJ18	DQ_A<23>
15B5<	B1	DDRA_DQ22	AL17	DQ_A<22> HIGH NIBBLE
15C5<	B1	DDRA_DQ21	AM19	DQ_A<21> DATA GROUP 3
15B5<	B1	DDRA_DQ20	AN20	DQ_A<20>
15B5<	B1	DDRA_DQS11	AK18	DQS_A<11>
15C5<	B1	DDRA_DQS2	AG18	DQS_A<2>
15B5<	B1	DDRA_DQ19	AF18	DQ_A<19>
15B5<	B1	DDRA_DQ18	AN17	DQ_A<18> LOW NIBBLE
15C5<	B1	DDRA_DQ17	AL19	DQ_A<17> DATA GROUP 3
15B5<	B1	DDRA_DQ16	AK19	DQ_A<16>
15A5<	B1	DDRA_DQ15	AJ22	DQ_A<15>
15A5<	B1	DDRA_DQ14	AL22	DQ_A<14> HIGH NIBBLE
15A5<	B1	DDRA_DQ13	AK24	DQ_A<13> DATA GROUP 2
15B5<	B1	DDRA_DQ12	AM25	DQ_A<12>
15A5<	B1	DDRA_DQS10	AK23	DQS_A<10>
15A5<	B1	DDRA_DQS1	AL23	DQS_A<1>
15B5<	B1	DDRA_DQ11	AE20	DQ_A<11>
15B5<	B1	DDRA_DQ10	AG21	DQ_A<10> LOW NIBBLE
15A5<	B1	DDRA_DQ9	AM24	DQ_A<9> DATA GROUP 2
15B5<	B1	DDRA_DQ8	AN25	DQ_A<8>
15A5<	B1	DDRA_DQ7	AL25	DQ_A<7>
15A5<	B1	DDRA_DQ6	AL26	DQ_A<6> HIGH NIBBLE
15D3<	B1	DDRA_DQ5	AM28	DQ_A<5> DATA GROUP 1
15D3<	B1	DDRA_DQ4	AN29	DQ_A<4>
15A5<	B1	DDRA_DQS9	AF21	DQS_A<9>
15A5<	B1	DDRA_DQS0	AM27	DQS_A<0>
15A5<	B1	DDRA_DQ3	AH22	DQ_A<3>
15A5<	B1	DDRA_DQ2	AE21	DQ_A<2> LOW NIBBLE
15A5<	B1	DDRA_DQ1	AN28	DQ_A<1> DATA GROUP 1
15D3<	B1	DDRA_DQ0	AF22	DQ_A<0>
15D5<	B1	DDRA_CB7	AG15	CB_A<7>
15D5<	B1	DDRA_CB6	AM15	CB_A<6> HIGH NIBBLE
15D8<	B1	DDRA_CB5	AG17	CB_A<5> CHECK BITS
15D8<	B1	DDRA_CB4	AE17	CB_A<4>
15D8<	B1	DDRA_DQS17	AF16	DQS_A<17>
15D8<	B1	DDRA_DQS8	AJ16	DQS_A<8>
15D5<	B1	DDRA_CB3	AK15	CB_A<3> LOW NIBBLE
15D5<	B1	DDRA_CB2	AL16	CB_A<2>
15D8<	B1	DDRA_CB1	AH16	CB_A<1> CHECK BITS
15D8<	B1	DDRA_CB0	AE16	CB_A<0>

ADDRESS BUS

WE_A*	AE23	DDRA_WE_N_R	OUT	18C6<> 16A5< 17A5<
CAS_A*	AE22	DDRA_CAS_N_R	OUT	18C6<> 16A5< 17A5<
RAS_A*	AN24	DDRA_RAS_N_R	OUT	22B8<> 16A5< 17A5<
MA_A<12>	AM31	DDRA_MA12_R	OUT	18A6<> 16A5< 17A5<
MA_A<11>	AK30	DDRA_MA11_R	OUT	18A6<> 16A5< 17A5<
MA_A<10>	AJ24	DDRA_MA10_R	OUT	18C8<> 16A5< 17A5<
MA_A<9>	AM30	DDRA_MA9_R	OUT	18A6<> 16A5< 17A5<
MA_A<8>	AK29	DDRA_MA8_R	OUT	18B6<> 16A5< 17A5<
MA_A<7>	AL29	DDRA_MA7_R	OUT	18A8<> 16A5< 17A5<
MA_A<6>	AL28	DDRA_MA6_R	OUT	18D6<> 16A5< 17A5<
MA_A<5>	AH28	DDRA_MA5_R	OUT	18A6<> 16A5< 17A4<
MA_A<4>	AG27	DDRA_MA4_R	OUT	18B6<> 16A5< 17A4<
MA_A<3>	AJ27	DDRA_MA3_R	OUT	18B6<> 16A5< 17A5<
MA_A<2>	AH26	DDRA_MA2_R	OUT	18A8<> 16A5< 17A5<
MA_A<1>	AK26	DDRA_MA1_R	OUT	18A8<> 16A5< 17A4<
MA_A<0>	AF24	DDRA_MA0_R	OUT	18D8<> 16A4< 17A4<

BA_A<1>	AH23	DDRA_BA1_R	OUT	18D8<> 16A4< 17A4<
BA_A<0>	AL31	DDRA_BA0_R	OUT	22B8<> 16A4< 17A4<

CHIP SELECT

CS_A*<7>	AL2			
CS_A*<6>	AL3			
CS_A*<5>	AK7			
CS_A*<4>	AN8			
CS_A*<3>	AH8	DDRA_CS3_N_R	OUT	18B8<> 17A5<
CS_A*<2>	AL10	DDRA_CS2_N_R	OUT	22C6<> 16A5<
CS_A*<1>	AK11	DDRA_CS1_N_R	OUT	22B8<> 16A5<
CS_A*<0>	AE13	DDRA_CS0_N_R	OUT	16A5<

N/C1	AM22	DDRA_RCV_EN_IN		
RCVENOUT_A*	AG20	DDRA_RCV_EN_OUT		
DDRCOMP_A	AH17			DDRA_DRCOMP
DDRCVOH_A	AK17			
N/C3	AN16			DDRCVOL_A
CKE_A	AE19			DDRA_CKE OUT 18A6<> 16A4< 17A4<
RESERVED5	AM18			

COMMAND CLOCK

CMDCLK_A3	AE25			
CMDCLK_A3*	AE24			
CMDCLK_A2	AG26			
CMDCLK_A2*	AF25			
CMDCLK_A1	AJ25	DDRA_CMDCLK1	OUT	17A4<
CMDCLK_A1*	AH25	DDRA_CMDCLK1_N	OUT	17A4<
CMDCLK_A0	AG24	DDRA_CMDCLK0	OUT	16A4<
CMDCLK_A0*	AG23	DDRA_CMDCLK0_N	OUT	16A4<

REF VOLTAGE

DDRVREF_A<5>	AJ28			
DDRVREF_A<3>	AK21			
DDRVREF_A<2>	AM16			
DDRVREF_A<1>	AL9			
DDRVREF_A<0>	AJ7			
RESERVED7	D29			
RESERVED4	B30			
RESERVED1	AK27			

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REV 0.5 IC

R161 2 EMPTY
R203 2 EMPTY
R117 2 0 603 0
R118 2 0 EMPTY 0
R202 402 1% CH 603
R775 4.7K 5% CH 603
R948 1K 1% CH 603
R47 EMPTY 0
R841 603 CH 1% 49.9
R115 7 1% EMPTY 603
R212 1 24.9 1% 603 CH 2

VTT_DDR
VCC3
2.5V
DDRCVO_A
VREF_DDR_MCH
IN
47C4> 47C7> 13A3<

R923 0
R924 0
R925 0
C1143 .1UF
C1144 .1UF
C1145 .1UF

C1669 603 .1UF
C1668 603 .1UF
C1667 603 .1UF
C1666 603 .1UF

R521 49.9 1% CH 603
R524 6.98K 1% EMPTY 603
C777 .01UF
C778 .01UF 50V EMPTY 603
R3157 49.9 1% CH 603

R523 6.98K 1% EMPTY 603
R522 13K 1% EMPTY 603
C779 .01UF 50V EMPTY 603
C780 .01UF EMPTY

DRAWING

PAGE	REV
12	A2.1

E7501 MCH

U66 E7501 — MCH DDR B

19D8<	B1	DDRB_DQ63	AB26	DQ_B<63>		
19D8<	B1	DDRB_DQ62	AC27	DQ_B<62>	HIGH NIBBLE	
19D3<	B1	DDRB_DQ61	AJ31	DQ_B<61>	DATA GROUP 8	
19C8<	B1	DDRB_DQ60	AL32	DQ_B<60>		
19D3<	B1	DDRB_DQS16	AF28	DQS_B<16>		
19D3<	B1	DDRB_DQS7	AE27	DQS_B<7>		
19D8<	B1	DDRB_DQ59	AA25	DQ_B<59>		
19D8<	B1	DDRB_DQ58	AB25	DQ_B<58>	LOW NIBBLE	
19D3<	B1	DDRB_DQ57	AG29	DQ_B<57>	DATA GROUP 8	
19C8<	B1	DDRB_DQ56	AJ30	DQ_B<56>		
19C8<	B1	DDRB_DQ55	AH33	DQ_B<55>		
19C8<	B1	DDRB_DQ54	AG30	DQ_B<54>	HIGH NIBBLE	
19C8<	B1	DDRB_DQ53	AA26	DQ_B<53>	DATA GROUP 7	
19C8<	B1	DDRB_DQ52	AC28	DQ_B<52>		
19C8<	B1	DDRB_DQS15	AD27	DQS_B<15>		
19D8<	B1	DDRB_DQ56	AE28	DQS_B<6>		
19C8<	B1	DDRB_DQ51	AH31	DQ_B<51>		
19D8<	B1	DDRB_DQ50	AH32	DQ_B<50>	LOW NIBBLE	
19C8<	B1	DDRB_DQ49	AB27	DQ_B<49>	DATA GROUP 7	
19C8<	B1	DDRB_DQ48	Y25	DQ_B<48>		
19B8<	B1	DDRB_DQ47	V25	DQ_B<47>		
19B8<	B1	DDRB_DQ46	AB29	DQ_B<46>	HIGH NIBBLE	
19B8<	B1	DDRB_DQ45	AB32	DQ_B<45>	DATA GROUP 6	
19A8<	B1	DDRB_DQ44	Y28	DQ_B<44>		
19B8<	B1	DDRB_DQS14	AB30	DQS_B<14>		
19B8<	B1	DDRB_DQS5	AC31	DQS_B<5>		
19B8<	B1	DDRB_DQ43	AD31	DQ_B<43>		
19B8<	B1	DDRB_DQ42	V26	DQ_B<42>	LOW NIBBLE	
19B8<	B1	DDRB_DQ41	AB33	DQ_B<41>	DATA GROUP 6	
19A8<	B1	DDRB_DQ40	AA29	DQ_B<40>		
19A8<	B1	DDRB_DQ39	W26	DQ_B<39>		
19A8<	B1	DDRB_DQ38	AG33	DQ_B<38>	HIGH NIBBLE	
19B8<	B1	DDRB_DQ37	AD32	DQ_B<37>	DATA GROUP 5	
19B8<	B1	DDRB_DQ36	AA28	DQ_B<36>		
19A8<	B1	DDRB_DQS13	AC30	DQS_B<13>		
19A8<	B1	DDRB_DQS4	AE32	DQS_B<4>		
19A8<	B1	DDRB_DQ35	W25	DQ_B<35>		
19A8<	B1	DDRB_DQ34	AF31	DQ_B<34>	LOW NIBBLE	
19C8<	B1	DDRB_DQ33	AE33	DQ_B<33>	DATA GROUP 5	
19B8<	B1	DDRB_DQ32	W27	DQ_B<32>		
19A8<	B1	DDRB_DQ31	T25	DQ_B<31>		
19D5<	B1	DDRB_DQ30	R28	DQ_B<30>	HIGH NIBBLE	
19D5<	B1	DDRB_DQ29	P31	DQ_B<29>	DATA GROUP 4	
19D5<	B1	DDRB_DQ28	N32	DQ_B<28>		
19D5<	B1	DDRB_DQS12	R31	DQS_B<12>		
19D5<	B1	DDRB_DQS3	R29	DQS_B<3>		
19A8<	B1	DDRB_DQ27	T32	DQ_B<27>		
19D5<	B1	DDRB_DQ26	R26	DQ_B<26>	LOW NIBBLE	
19D5<	B1	DDRB_DQ25	P33	DQ_B<25>	DATA GROUP 4	
19D5<	B1	DDRB_DQ24	P30	DQ_B<24>		
19D5<	B1	DDRB_DQ23	V31	DQ_B<23>		
19C5<	B1	DDRB_DQ22	V33	DQ_B<22>	HIGH NIBBLE	
19C5<	B1	DDRB_DQ21	T27	DQ_B<21>	DATA GROUP 3	
19C5<	B1	DDRB_DQ20	R32	DQ_B<20>		
19C5<	B1	DDRB_DQS11	U31	DQS_B<11>		
19C5<	B1	DDRB_DQS2	U33	DQS_B<2>		
19D5<	B1	DDRB_DQ19	T26	DQ_B<19>		
19C5<	B1	DDRB_DQ18	U30	DQ_B<18>	LOW NIBBLE	
19C5<	B1	DDRB_DQ17	T30	DQ_B<17>	DATA GROUP 3	
19C5<	B1	DDRB_DQ16	T29	DQ_B<16>		
19B5<	B1	DDRB_DQ15	P28	DQ_B<15>		
19B5<	B1	DDRB_DQ14	P26	DQ_B<14>	HIGH NIBBLE	
19B5<	B1	DDRB_DQ13	L31	DQ_B<13>	DATA GROUP 2	
19B5<	B1	DDRB_DQ12	J31	DQ_B<12>		
19B5<	B1	DDRB_DQS10	N29	DQS_B<10>		
19B5<	B1	DDRB_DQS1	M31	DQS_B<1>		
19C5<	B1	DDRB_DQ11	P25	DQ_B<11>		
19C5<	B1	DDRB_DQ10	P27	DQ_B<10>	LOW NIBBLE	
19B5<	B1	DDRB_DQ9	K32	DQ_B<9>	DATA GROUP 2	
19B5<	B1	DDRB_DQ8	J33	DQ_B<8>		
19A5<	B1	DDRB_DQ7	N26	DQ_B<7>		
19A5<	B1	DDRB_DQ6	M29	DQ_B<6>	HIGH NIBBLE	
19A5<	B1	DDRB_DQ5	G32	DQ_B<5>	DATA GROUP 1	
19A5<	B1	DDRB_DQ4	N27	DQ_B<4>		
19A5<	B1	DDRB_DQS9	H31	DQS_B<9>		
19A5<	B1	DDRB_DQS0	L30	DQS_B<0>		
19A5<	B1	DDRB_DQ3	N25	DQ_B<3>		
19A5<	B1	DDRB_DQ2	J32	DQ_B<2>	LOW NIBBLE	
19A5<	B1	DDRB_DQ1	K30	DQ_B<1>	DATA GROUP 1	
19A5<	B1	DDRB_DQ0	F33	DQ_B<0>		
19C5<	B1	DDRB_CB7	AA32	CB_B<7>		
19B5<	B1	DDRB_CB6	AA31	CB_B<6>	HIGH NIBBLE	
19A8<	B1	DDRB_CB5	U27	CB_B<5>	CHECK BITS	
19A8<	B1	DDRB_CB4	U28	CB_B<4>		
19D8<	B1	DDRB_DQS17	Y30	DQS_B<17>		
19D8<	B1	DDRB_DQS8	W29	DQS_B<8>		
19C5<	B1	DDRB_CB3	AA33	CB_B<3>		
19B5<	B1	DDRB_CB2	Y31	CB_B<2>	LOW NIBBLE	
19D8<	B1	DDRB_CB1	U25	CB_B<1>	CHECK BITS	
19D8<	B1	DDRB_CB0	V28	CB_B<0>		

ADDRESS BUS

WE_B*	D32	DDRB_WE_N_R	OUT	22D8<> 20A5< 21A5<
CAS_B*	H28	DDRB_CAS_N_R	OUT	22D8<> 20A5< 21A5<
RAS_B*	V32	DDRB_RAS_N_R	OUT	18D4<> 20A5< 21A5<
MA_B<12>	C32	DDRB_MA12_R	OUT	22A8<> 20A5< 21A5<
MA_B<11>	C31	DDRB_MA11_R	OUT	22B8<> 20A5< 21A5<
MA_B<10>	L25	DDRB_MA10_R	OUT	22D8<> 20A5< 21A5<
MA_B<9>	F29	DDRB_MA9_R	OUT	22B8<> 20A5< 21A5<
MA_B<8>	E31	DDRB_MA8_R	OUT	22A8<> 20A5< 21A5<
MA_B<7>	E33	DDRB_MA7_R	OUT	22B6<> 20A5< 21A5<
MA_B<6>	F31	DDRB_MA6_R	OUT	22A6<> 20A5< 21A5<
MA_B<5>	G29	DDRB_MA5_R	OUT	22A8<> 20A5< 21A5<
MA_B<4>	F32	DDRB_MA4_R	OUT	22B6<> 20A5< 21A5<
MA_B<3>	G30	DDRB_MA3_R	OUT	22A6<> 20A5< 21A5<
MA_B<2>	H30	DDRB_MA2_R	OUT	22D6<> 20A5< 21A5<
MA_B<1>	K29	DDRB_MA1_R	OUT	22D8<> 20A5< 21A5<
MA_B<0>	M26	DDRB_MA0_R	OUT	18C8<> 20A5< 21A5<

BA_B<1>	H27	DDRB_BA1_R	OUT	22B6<> 20A4< 21A5<
BA_B<0>	K26	DDRB_BA0_R	OUT	18D4<> 20A4< 21A4<

CHIP SELECT

CS_B*<7>	Y27			
CS_B*<6>	AD28			
CS_B*<5>	AE26			
CS_B*<4>	AE31			
CS_B*<3>	AF27	DDRB_CS3_N_R	OUT	18B8<> 21A5<
CS_B*<2>	AF30	DDRB_CS2_N_R	OUT	18B8<> 21A5<
CS_B*<1>	AK32	DDRB_CS1_N_R	OUT	22C6<> 20A5<
CS_B*<0>	AH29	DDRB_CS0_N_R	OUT	22C6<> 20A5<

N/C2	N30	DDRB_RCV_EN_IN		1 R198 2 EMPTY
RCVENOUT_B*	R25	DDRB_RCV_EN_OUT		
DDRCOMP_B	W30			DDRB_DRCOMP
DDRCVOH_B	W32			DDRCVO_B
N/C4	V29			1 R45 2 EMPTY DDRBCVOL_B
CKE_B	M32			1 R124 2 0 603 0 DDRB_CKE OUT 22D6<> 20A4< 21A4<
RESERVED6	K33			

COMMAND CLOCK

CMDCLK_B3	K27			
CMDCLK_B3*	L27			
CMDCLK_B2	J26			
CMDCLK_B2*	K25			
CMDCLK_B1	L28	DDRB_CMDCLK1	OUT	21A4<
CMDCLK_B1*	M28	DDRB_CMDCLK1_N	OUT	21A4<
CMDCLK_B0	J29	DDRB_CMDCLK0	OUT	20A4<
CMDCLK_B0*	J28	DDRB_CMDCLK0_N	OUT	20A4<

REF VOLTAGE

DDRVREF_B<3>	N33		
DDRVREF_B<2>	U26		
DDRVREF_B<1>	AG32		
DDRVREF_B<0>	AC25		
RESERVED3	E30		
RESERVED2	M25		

R50 0 EMPTY 603; R51 0 EMPTY 603

VREF_DDR_MCH — IN — 12A3< 47C4> 47C7>

R928 0; R927 0; R926 0

C1146 .1UF; C1147 .1UF; C1148 .1UF

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VTT_DDR

R120 7 1% EMPTY 603

2 R215 1 24.9 603 1% CH

VTT_DDR

2 603 CH 1% 49.9 R843 1

2.5V

R528 49.9 1% CH 603

VTT_DDR

R527 6.98K 1% EMPTY 603

C783 .01UF

C784 .01UF 5% 50V EMPTY 603

R3125 49.9 1% CH 603

VTT_DDR

R526 6.98K 1% EMPTY 603

R525 13K 1% EMPTY 603

C782 .01UF 5% 50V EMPTY 603

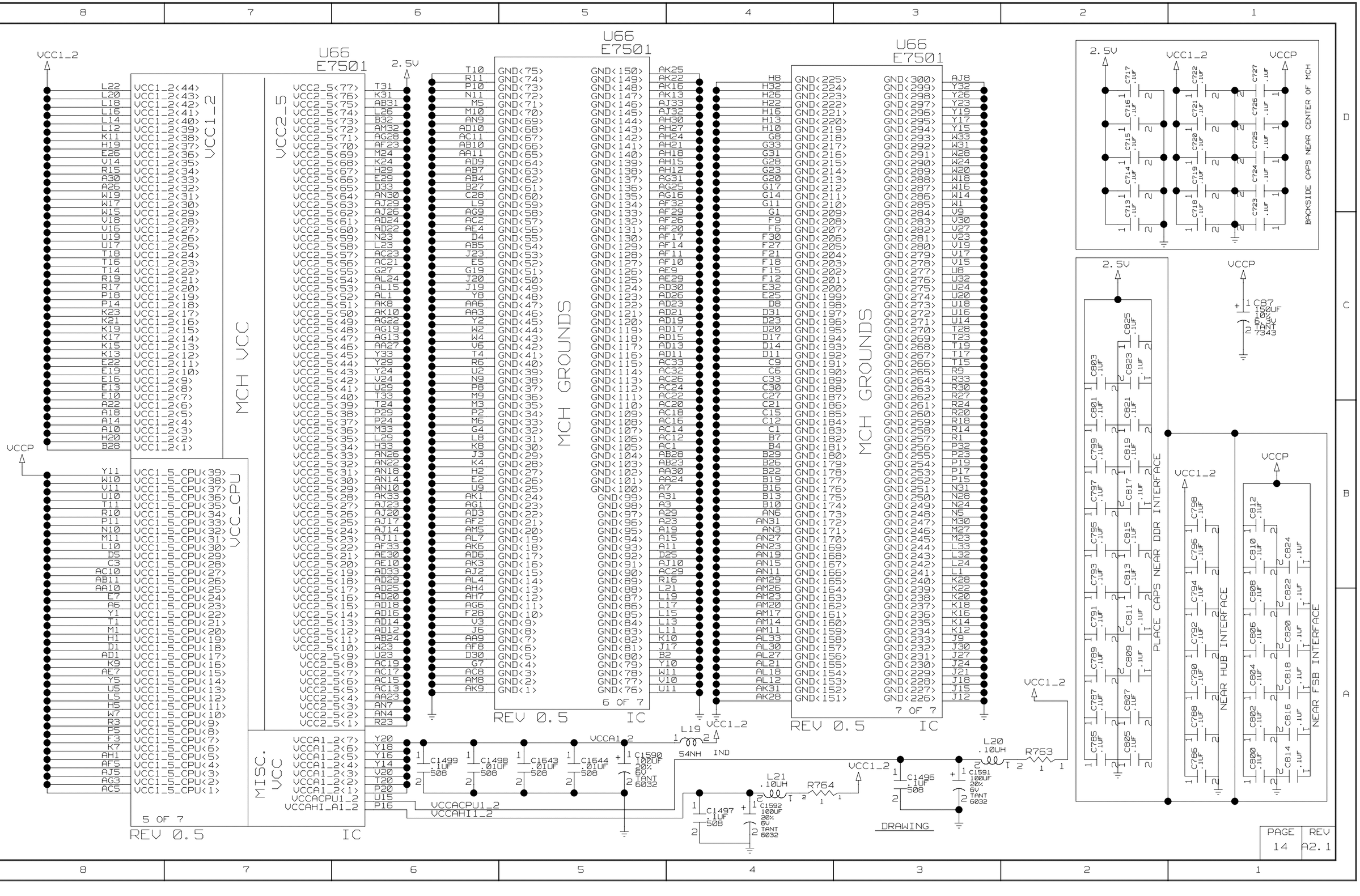
C781 .01UF 5% 50V EMPTY 603

DRAWING

REV 0.5

IC

PAGE	REV
13	A2.1


U66
E7501
MCH VCC
VCC1_2
VCC1_5_CPU
VCC_CPU
5 OF 7
REV 0.5
IC
U66
E7501
VCC2_5
MCH GROUNDS
6 OF 7
REV 0.5
IC
U66
E7501
MCH GROUNDS
7 OF 7
REV 0.5
IC
MISC. VCC
IC
2.5V
VCC1_2
VCCP
VCCA1_2
VCCACPU1_2
VCCAHI1_2
L19
54NH IND
L20
.10UH
L21
.10UH
R763
R764
DRAWING
BACKSIDE CAPS NEAR CENTER OF MCH
PLACE CAPS NEAR DDR INTERFACE
NEAR HUB INTERFACE
NEAR FSB INTERFACE
PAGE 14
REV A2.1

DDR CHANNEL A SERIES RESISTORS

RP13
12B8< B1 DDRA_DQ27 1 8 DDRA_DQ27_R B1
12B8< B1 DDRA_DQ31 2 7 DDRA_DQ31_R B1
12A8< B1 DDRA_CB4 3 6 DDRA_CB4_R B1
12A8< B1 DDRA_CB5 4 5 DDRA_CB5_R B1
10 5% .063W
16D4<> 17D4<> 18A8<>
16D5<> 17D4<> 18B6<>
16D3<> 17D2<> 18A8<>
16D3<> 17D2<> 18B6<>

RP14
12A8< B1 DDRA_CB0 1 8 DDRA_CB0_R B1
12A8< B1 DDRA_CB1 2 7 DDRA_CB1_R B1
12A8< B1 DDRA_DQS8 3 6 DDRA_DQS8_R B1
12A8< B1 DDRA_DQS17 4 5 DDRA_DQS17_R B1
10 5% .063W
16D2<> 17D2<> 18D8<>
16D2<> 17D2<> 18D8<>
16D2<> 17D2<> 18D8<>
16D3<> 17D2<> 18D8<>

RP15
12C8< B1 DDRA_DQ39 1 8 DDRA_DQ39_R B1
12C8< B1 DDRA_DQ44 2 7 DDRA_DQ44_R B1
12C8< B1 DDRA_DQ35 3 6 DDRA_DQ35_R B1
12C8< B1 DDRA_DQ40 4 5 DDRA_DQ40_R B1
10 5% .063W
16D5<> 17D5<> 18A8<>
16D6<> 17D5<> 18B8<>
16D5<> 17D5<> 18A8<>
16D5<> 17D5<> 18B8<>

RP16
12D8< B1 DDRA_DQ63 1 8 DDRA_DQ63_R B1
12D8< B1 DDRA_DQ58 2 7 DDRA_DQ58_R B1
12D8< B1 DDRA_DQ57 3 6 DDRA_DQ57_R B1
12D8< B1 DDRA_DQ59 4 5 DDRA_DQ59_R B1
10 5% .063W
16D7<> 17D6<> 18B8<>
16D6<> 17D6<> 18B8<>
16D6<> 17D6<> 18B8<>
16D6<> 17D6<> 18B8<>

RP17
12D8< B1 DDRA_DQ56 1 8 DDRA_DQ56_R B1
12D8< B1 DDRA_DQS16 2 7 DDRA_DQS16_R B1
12D8< B1 DDRA_DQ62 3 6 DDRA_DQ62_R B1
12D8< B1 DDRA_DQ57 4 5 DDRA_DQ57_R B1
10 5% .063W
16D6<> 17D6<> 18B6<>
16D7<> 17D6<> 18C6<>
16D7<> 17D6<> 18C6<>
16D6<> 17D6<> 18B6<>

RP18
12D8< B1 DDRA_DQS15 1 8 DDRA_DQS15_R B1
12D8< B1 DDRA_DQS6 2 7 DDRA_DQS6_R B1
12D8< B1 DDRA_DQ54 3 6 DDRA_DQ54_R B1
12D8< B1 DDRA_DQS5 4 5 DDRA_DQS5_R B1
10 5% .063W
16D6<> 17D6<> 18B8<>
16D6<> 17D6<> 18B8<>
16D6<> 17D6<> 18C8<>
16D6<> 17D6<> 18C8<>

RP19
12C8< B1 DDRA_DQ50 1 8 DDRA_DQ50_R B1
12D8< B1 DDRA_DQ60 2 7 DDRA_DQ60_R B1
12D8< B1 DDRA_DQ51 3 6 DDRA_DQ51_R B1
12D8< B1 DDRA_DQ61 4 5 DDRA_DQ61_R B1
10 5% .063W
16D6<> 17D6<> 18C8<>
16D7<> 17D6<> 18C8<>
16D6<> 17D6<> 18C8<>
16D7<> 17D6<> 18C8<>

RP20
12C8< B1 DDRA_DQ48 1 8 DDRA_DQ48_R B1
12D8< B1 DDRA_DQ52 2 7 DDRA_DQ52_R B1
12C8< B1 DDRA_DQ49 3 6 DDRA_DQ49_R B1
12D8< B1 DDRA_DQ53 4 5 DDRA_DQ53_R B1
10 5% .063W
16D6<> 17D6<> 18B8<>
16D6<> 17D6<> 18B8<>
16D6<> 17D6<> 18B8<>
16D6<> 17D6<> 18B8<>

RP21
12C8< B1 DDRA_DQ45 1 8 DDRA_DQ45_R B1
12C8< B1 DDRA_DQ41 2 7 DDRA_DQ41_R B1
12D8< B1 DDRA_DQS14 3 6 DDRA_DQS14_R B1
12C8< B1 DDRA_DQS5 4 5 DDRA_DQS5_R B1
10 5% .063W
16D6<> 17D5<> 18A8<>
16D5<> 17D5<> 18C6<>
16D6<> 17D5<> 18A8<>
16D5<> 17D5<> 18C6<>

RP22
12C8< B1 DDRA_DQ42 1 8 DDRA_DQ42_R B1
12C8< B1 DDRA_DQ46 2 7 DDRA_DQ46_R B1
12C8< B1 DDRA_DQ47 3 6 DDRA_DQ47_R B1
12C8< B1 DDRA_DQ43 4 5 DDRA_DQ43_R B1
10 5% .063W
16D5<> 17D5<> 18D6<>
16D6<> 17D5<> 18D6<>
16D6<> 17D5<> 18D6<>
16D5<> 17D5<> 18D6<>

RP23
12C8< B1 DDRA_DQS4 1 8 DDRA_DQS4_R B1
12C8< B1 DDRA_DQ34 2 7 DDRA_DQ34_R B1
12C8< B1 DDRA_DQ38 3 6 DDRA_DQ38_R B1
12C8< B1 DDRA_DQS13 4 5 DDRA_DQS13_R B1
10 5% .063W
16D5<> 17D5<> 18B6<>
16D5<> 17D5<> 18B6<>
16D5<> 17D5<> 18B6<>
16D5<> 17D5<> 18B6<>

RP24
12C8< B1 DDRA_DQ36 1 8 DDRA_DQ36_R B1
12C8< B1 DDRA_DQ32 2 7 DDRA_DQ32_R B1
12C8< B1 DDRA_DQ37 3 6 DDRA_DQ37_R B1
12C8< B1 DDRA_DQ33 4 5 DDRA_DQ33_R B1
10 5% .063W
16D5<> 17D5<> 18A8<>
16D5<> 17D5<> 18A8<>
16D5<> 17D5<> 18A8<>
16D5<> 17D5<> 18A8<>

RP25
12A8< B1 DDRA_CB2 1 8 DDRA_CB2_R B1
12A8< B1 DDRA_CB6 2 7 DDRA_CB6_R B1
12A8< B1 DDRA_CB3 3 6 DDRA_CB3_R B1
12A8< B1 DDRA_CB7 4 5 DDRA_CB7_R B1
10 5% .063W
16D2<> 17D2<> 18D8<
16D3<> 17D2<> 18C8<>
16D2<> 17D2<> 18D8<>
16D3<> 17D2<> 18C8<>

RP26
12B8< B1 DDRA_DQ24 1 8 DDRA_DQ24_R B1
12B8< B1 DDRA_DQ28 2 7 DDRA_DQ28_R B1
12B8< B1 DDRA_DQ29 3 6 DDRA_DQ29_R B1
12B8< B1 DDRA_DQ25 4 5 DDRA_DQ25_R B1
10 5% .063W
16D4<> 17D4<> 18D6<>
16D5<> 17D4<> 18D6<>
16D5<> 17D4<> 18D8<>
16D4<> 17D4<> 18D6<>

RP27
12B8< B1 DDRA_DQS3 1 8 DDRA_DQS3_R B1
12B8< B1 DDRA_DQS12 2 7 DDRA_DQS12_R B1
12B8< B1 DDRA_DQ30 3 6 DDRA_DQ30_R B1
12B8< B1 DDRA_DQ26 4 5 DDRA_DQ26_R B1
10 5% .063W
16D4<> 17D4<> 18B6<>
16D5<> 17D4<> 18D8<>
16D5<> 17D4<> 18D8<>
16D4<> 17D4<> 18B6<>

RP28
12B8< B1 DDRA_DQ17 1 8 DDRA_DQ17_R B1
12B8< B1 DDRA_DQ21 2 7 DDRA_DQ21_R B1
12B8< B1 DDRA_DQS2 3 6 DDRA_DQS2_R B1
12B8< B1 DDRA_DQS11 4 5 DDRA_DQS11_R B1
10 5% .063W
16D4<> 17D4<> 18A6<>
16D4<> 17D4<> 18A6<>
16D4<> 17D4<> 18A6<>
16D4<> 17D4<> 18A8<>

RP29
12B8< B1 DDRA_DQ18 1 8 DDRA_DQ18_R B1
12B8< B1 DDRA_DQ22 2 7 DDRA_DQ22_R B1
12B8< B1 DDRA_DQ23 3 6 DDRA_DQ23_R B1
12B8< B1 DDRA_DQ19 4 5 DDRA_DQ19_R B1
10 5% .063W
16D4<> 17D4<> 18A8<>
16D4<> 17D4<> 18A8<>
16D4<> 17D4<> 18B6<>
16D4<> 17D4<> 18A6<>

RP30
12A8< B1 DDRA_DQ10 1 8 DDRA_DQ10_R B1
12A8< B1 DDRA_DQ11 2 7 DDRA_DQ11_R B1
12B8< B1 DDRA_DQ20 3 6 DDRA_DQ20_R B1
12B8< B1 DDRA_DQ16 4 5 DDRA_DQ16_R B1
10 5% .063W
16D3<> 17D3<> 18A6<>
16D3<> 17D3<> 18A6<>
16D4<> 17D4<> 18A6<>
16D4<> 17D4<> 18A6<>

RP31
12A8< B1 DDRA_DQ8 1 8 DDRA_DQ8_R B1
12B8< B1 DDRA_DQ12 2 7 DDRA_DQ12_R B1
12A8< B1 DDRA_DQ9 3 6 DDRA_DQ9_R B1
12A8< B1 DDRA_DQS1 4 5 DDRA_DQS1_R B1
10 5% .063W
16D3<> 17D3<> 18C6<>
16D4<> 17D3<> 18C6<>
16D3<> 17D3<> 18D6<>
16D3<> 17D3<> 18D6<>

RP32
12B8< B1 DDRA_DQ13 1 8 DDRA_DQ13_R B1
12A8< B1 DDRA_DQS10 2 7 DDRA_DQS10_R B1
12B8< B1 DDRA_DQ14 3 6 DDRA_DQ14_R B1
12B8< B1 DDRA_DQ15 4 5 DDRA_DQ15_R B1
10 5% .063W
16D4<> 17D3<> 18D6<>
16D4<> 17D3<> 18C6<>
16D4<> 17D3<> 18A6<>
16D4<> 17D3<> 18A6<>

RP33
12A8< B1 DDRA_DQ1 1 8 DDRA_DQ1_R B1
12A8< B1 DDRA_DQS9 2 7 DDRA_DQS9_R B1
12A8< B1 DDRA_DQS0 3 6 DDRA_DQS0_R B1
12A8< B1 DDRA_DQ6 4 5 DDRA_DQ6_R B1
10 5% .063W
16D3<> 17D3<> 22A8<>
16D3<> 17D3<> 18C6<>
16D3<> 17D3<> 18C6<>
16D3<> 17D3<> 18C6<>

RP34
12A8< B1 DDRA_DQ2 1 8 DDRA_DQ2_R B1
12A8< B1 DDRA_DQ7 2 7 DDRA_DQ7_R B1
12A8< B1 DDRA_DQ3 3 6 DDRA_DQ3_R B1
4 5
10 5% .063W
16D3<> 17D3<> 18C6<>
16D3<> 17D3<> 18C6<>
16D3<> 17D3<> 18C6<>

DRAWING

PLACE NEAR DIMM A-1

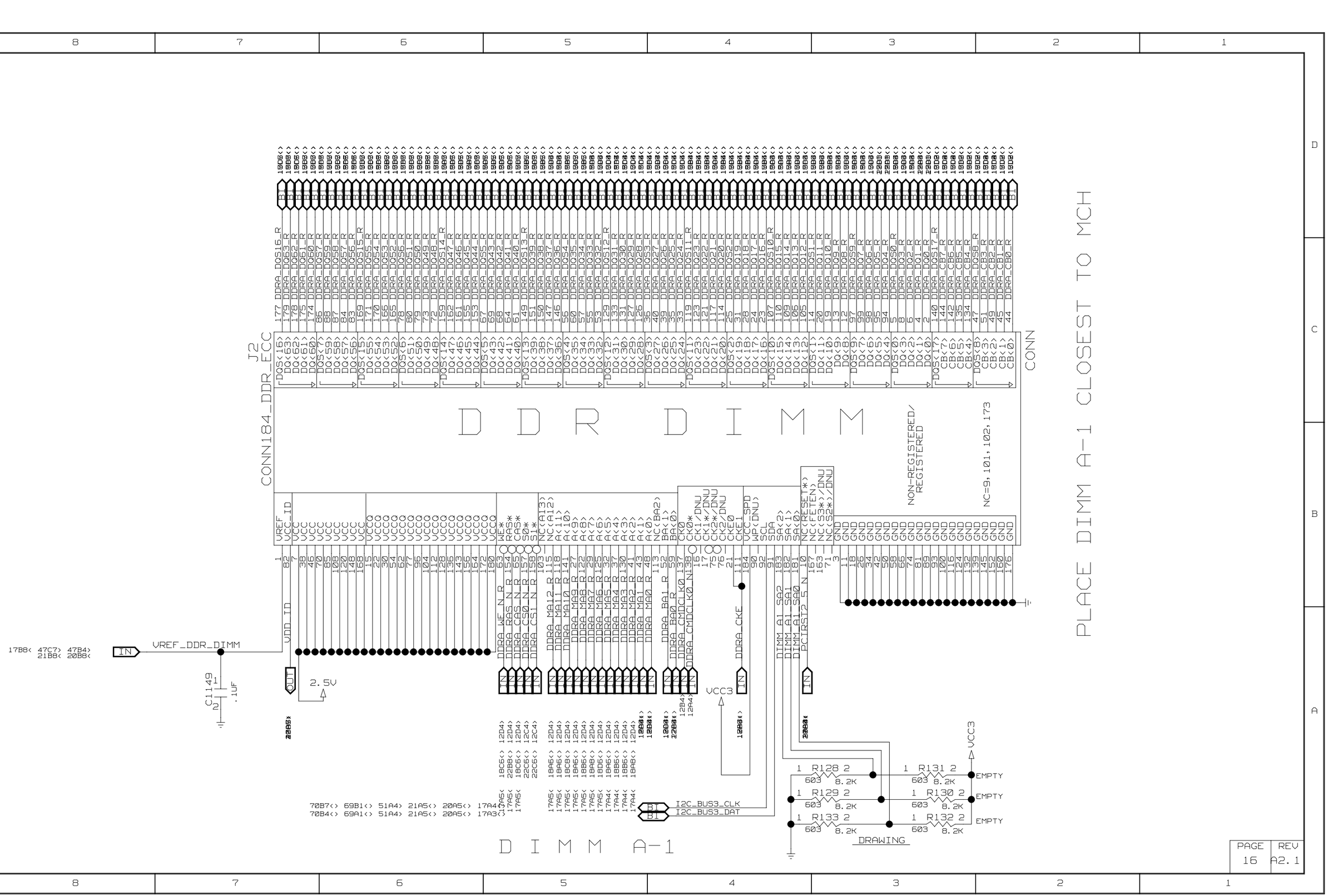
RP35
12A8< B1 DDRA_DQ0 1 8 DDRA_DQ0_R B1
12A8< B1 DDRA_DQ4 3 6 DDRA_DQ4_R B1
12A8< B1 DDRA_DQ5 4 5 DDRA_DQ5_R B1
10 5% .063W
22A8<>
16D3<> 17D3<>
16D3<> 17D3<>
16D3<> 17D3<>
22A8<>

2.5V
C843 1 2 1UF 10%
C842 1 2 1UF 10%
C841 1 2 1UF 10%
C840 1 2 1UF 10%
C839 1 2 1UF 10%
C838 1 2 1UF 10% 16V 603
0.1UF BACKSIDE OR FRONTSIDE CAPS
6 CAPS BETWEEN EACH PAIR OF DIMMS

2.5V
C765 1 2 100UF 20% 6.3V TANT 6032
C764 1 2 100UF 20% 6.3V TANT 6032
C763 1 2 100UF 20% 6.3V TANT 6032
C762 1 2 100UF 20% 6.3V TANT 6032
C761 1 2 100UF 20% 6.3V TANT 6032
C760 1 2 100UF 20% 6.3V TANT 6032
PLACE 100UF CAPS SURROUNDING CHANNEL A DIMMS

CAD NOTE:
ALL CAPS SHOULD HAVE DIRECT CONNECTION
TO 2.5V PLANE AND 2 VIAS TO GND.

PAGE	REV
15	A2.1


DDR DIMM A-1
PLACE DIMM A-1 CLOSEST TO MCH
J2
CONN184_DDR_ECC
CONN
VREF_DDR_DIMM
VDD_ID
2.5V
C1149
.1UF
DDRA_WE_N_R
DDRA_RAS_N_R
DDRA_CAS_N_R
DDRA_CS0_N_R
DDRA_CS1
DDRA_MA12_R
DDRA_MA11_R
DDRA_MA10_R
DDRA_MA9_R
DDRA_MA8_R
DDRA_MA7_R
DDRA_MA6_R
DDRA_MA5_R
DDRA_MA4_R
DDRA_MA3_R
DDRA_MA2_R
DDRA_MA1_R
DDRA_MA0_R
DDRA_BA1_R
DDRA_BA0_R
DDRA_CMDCLK0_N
DDRA_CMDCLK0
DDRA_CKE
VCC3
DIMM_A1_SA2
DIMM_A1_SA1
DIMM_A1_SA0
PCIRST2_5_N
NON-REGISTERED/
REGISTERED
NC=9,101,102,173
I2C_BUS3_CLK
I2C_BUS3_DAT
R128 2 603 8.2K
R131 2 603 8.2K
R129 2 603 8.2K
R130 2 603 8.2K
R133 2 603 8.2K
R132 2 603 8.2K
EMPTY
DRAWING
DIMM A-1
PAGE 16
REV A2.1

DDR DIMM

DIMM A-2

J5
CONN184_DDR_ECC

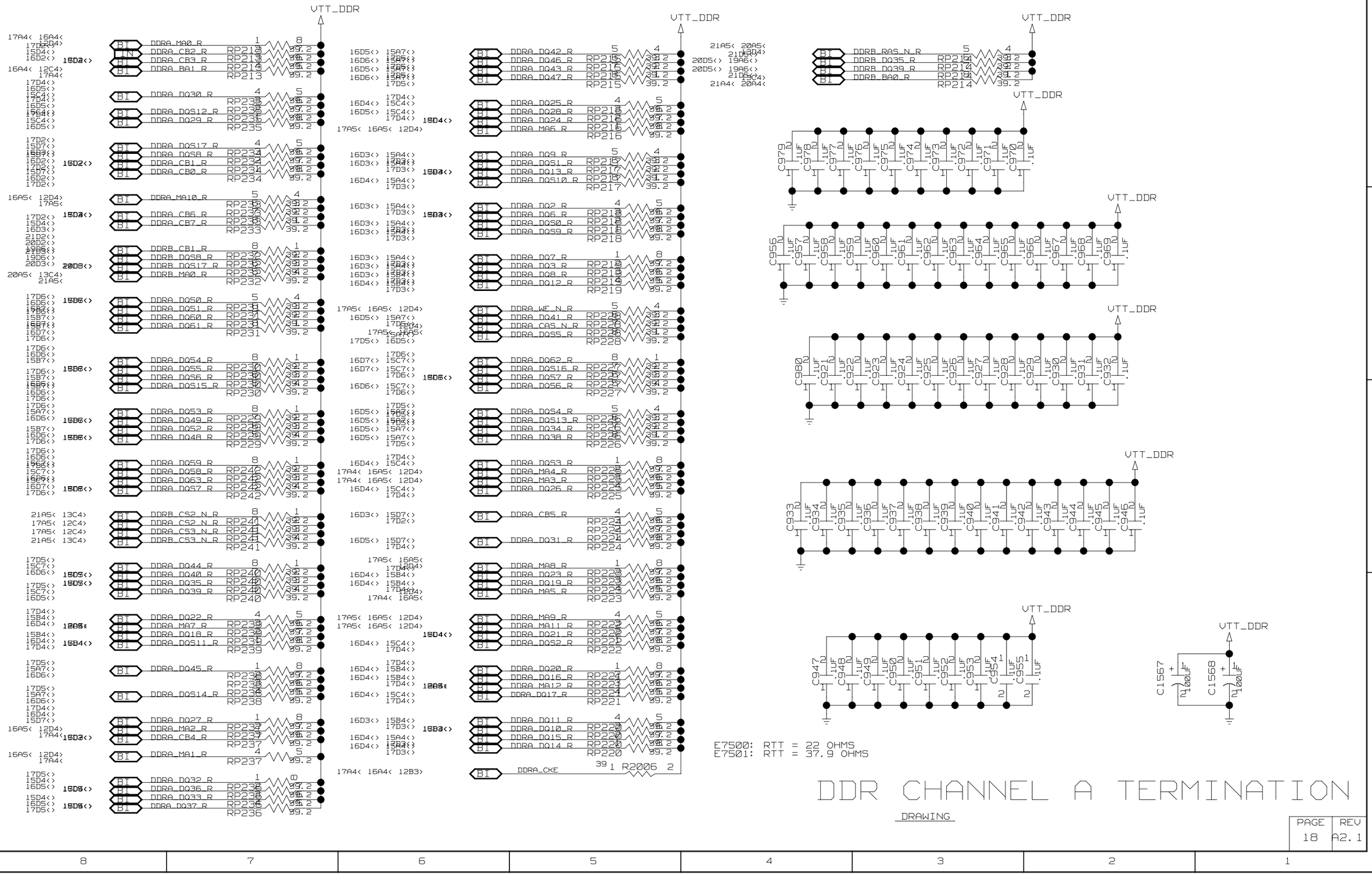
CONN

NON-REGISTERED/
REGISTERED

NC=9,101,102,173

DRAWING

PAGE	REV
17	A2.1



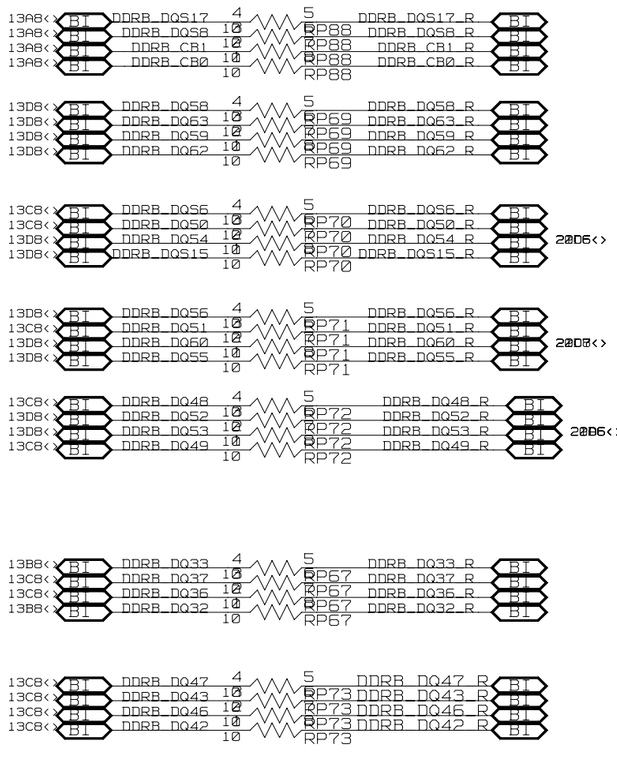
E7500: RTT = 22 OHMS
E7501: RTT = 37.9 OHMS

DDR CHANNEL A TERMINATION

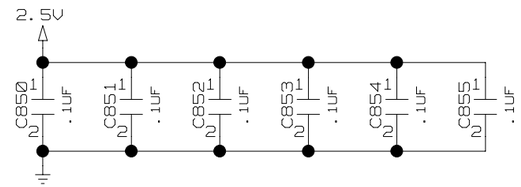
DRAWING

PAGE	REV
18	A2.1

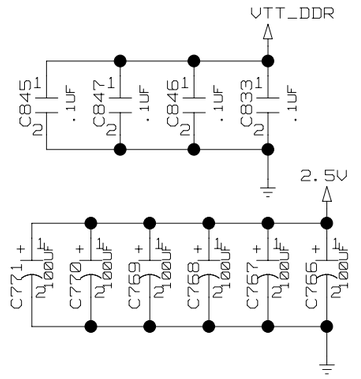
D D R CHANNEL B SERIES RESISTORS



PLACE NEAR D I M M B-1



0.1 UF BACKSIDE OR FRONTSIDE CAPS
6 CAPS BETWEEN EACH PAIR OF DIMMS



PLACE 100UF CAPS SURROUNDING CHAN B DIMMS
CAD NOTE: ALL CAPS SHOULD HAVE
DIRECT ATTACHMENT TO 2.5V PLANE,
AND 2 VIAS TO GND

DRAWING

PAGE	REV
19	A2.1

DDR DIMM B-1

CONN184_DDR_ECC

J1

CONN

NON-REGISTERED/
REGISTERED

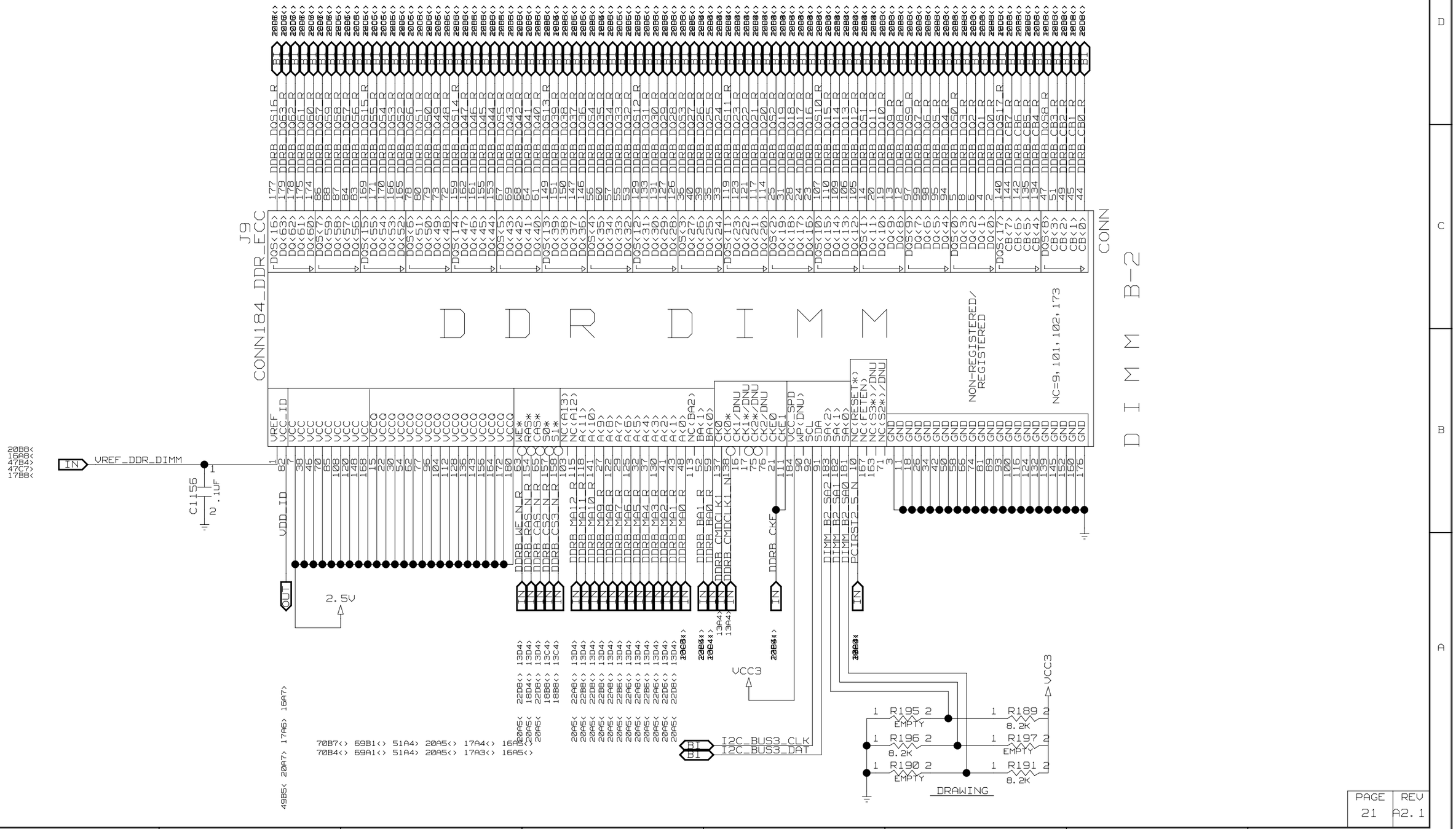
NC=9,101,102,173

DDR DIMM B-1

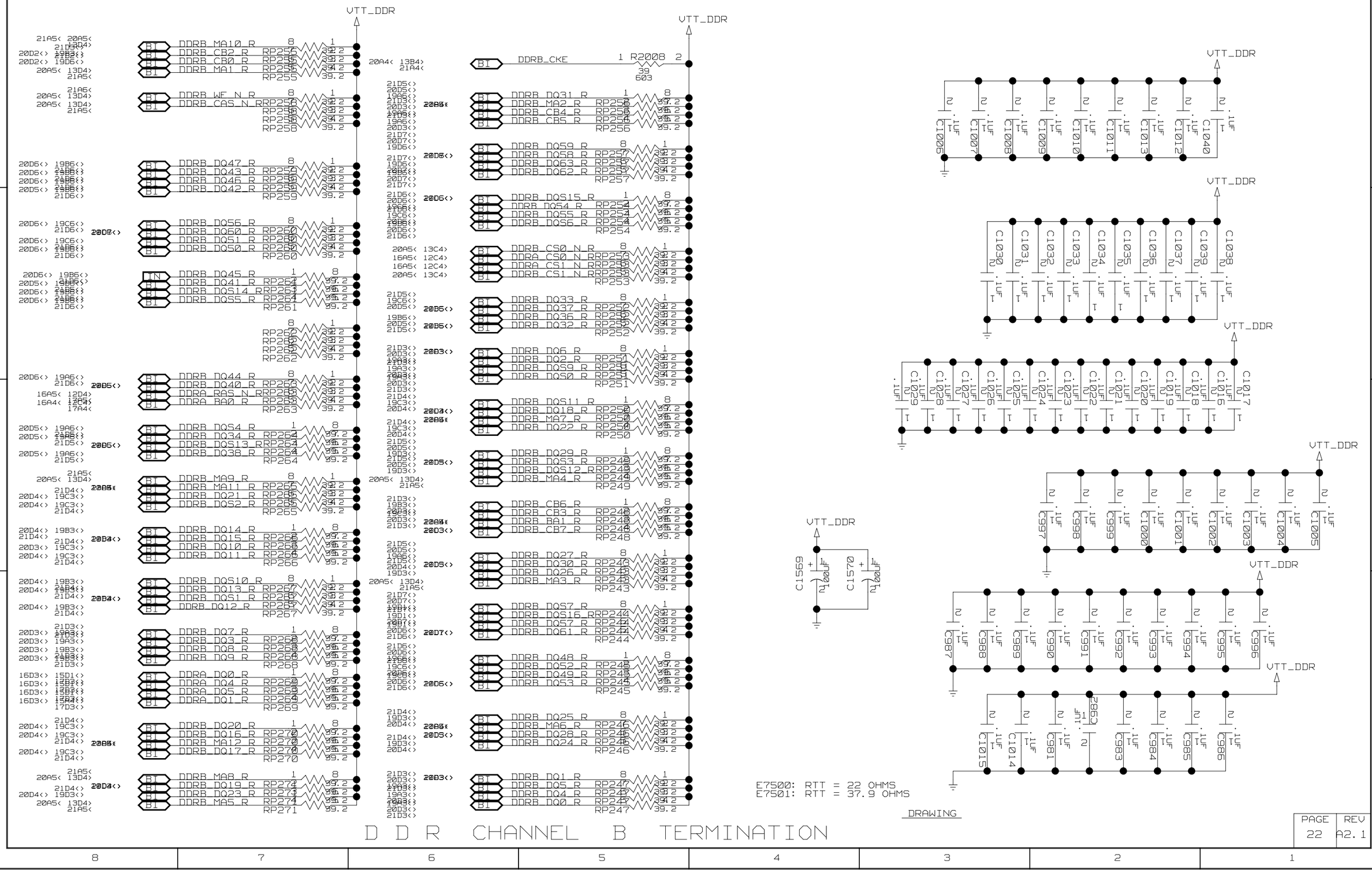
PLACE DIMM B - 1 CLOSEST TO MCH

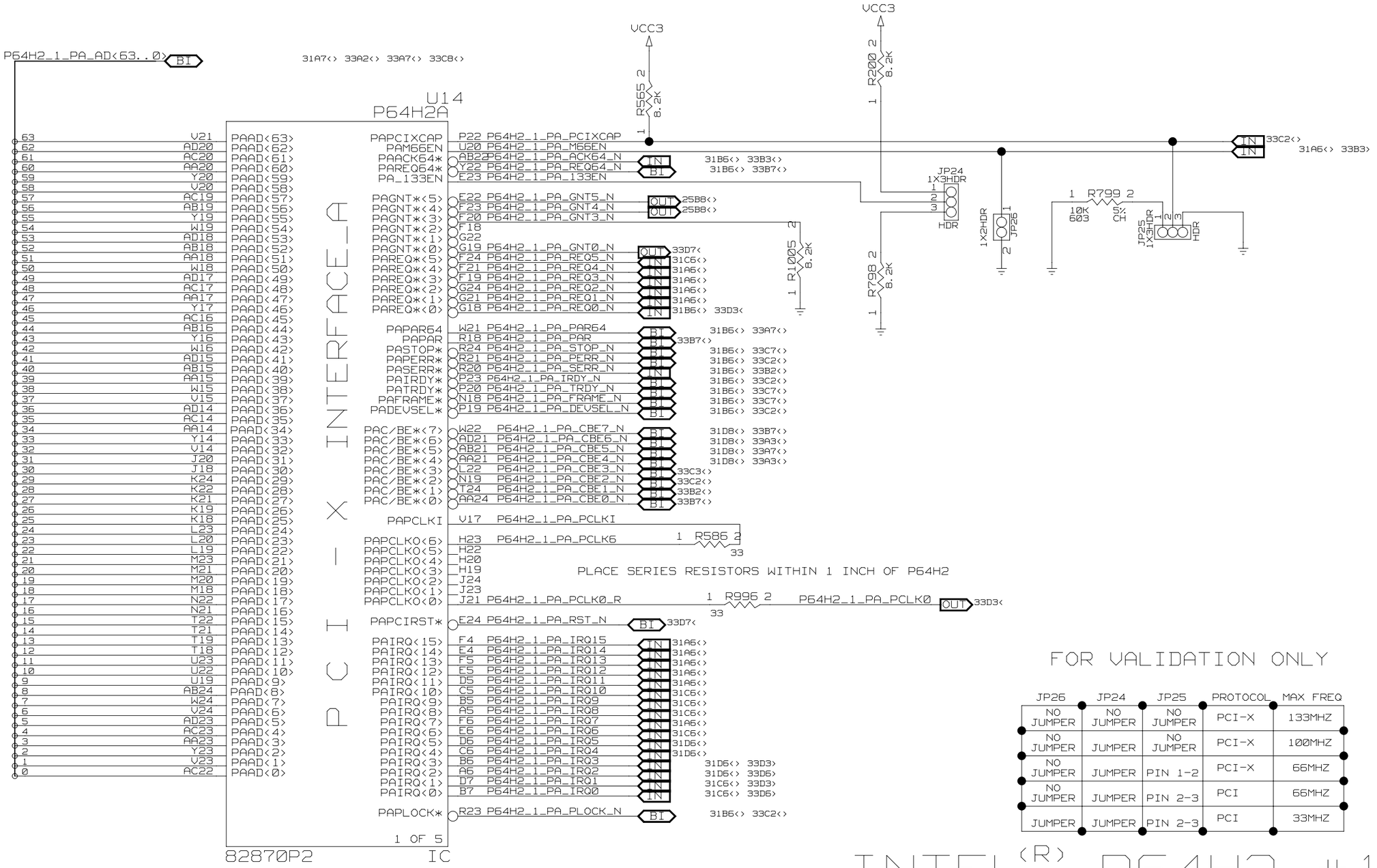
DRAWING

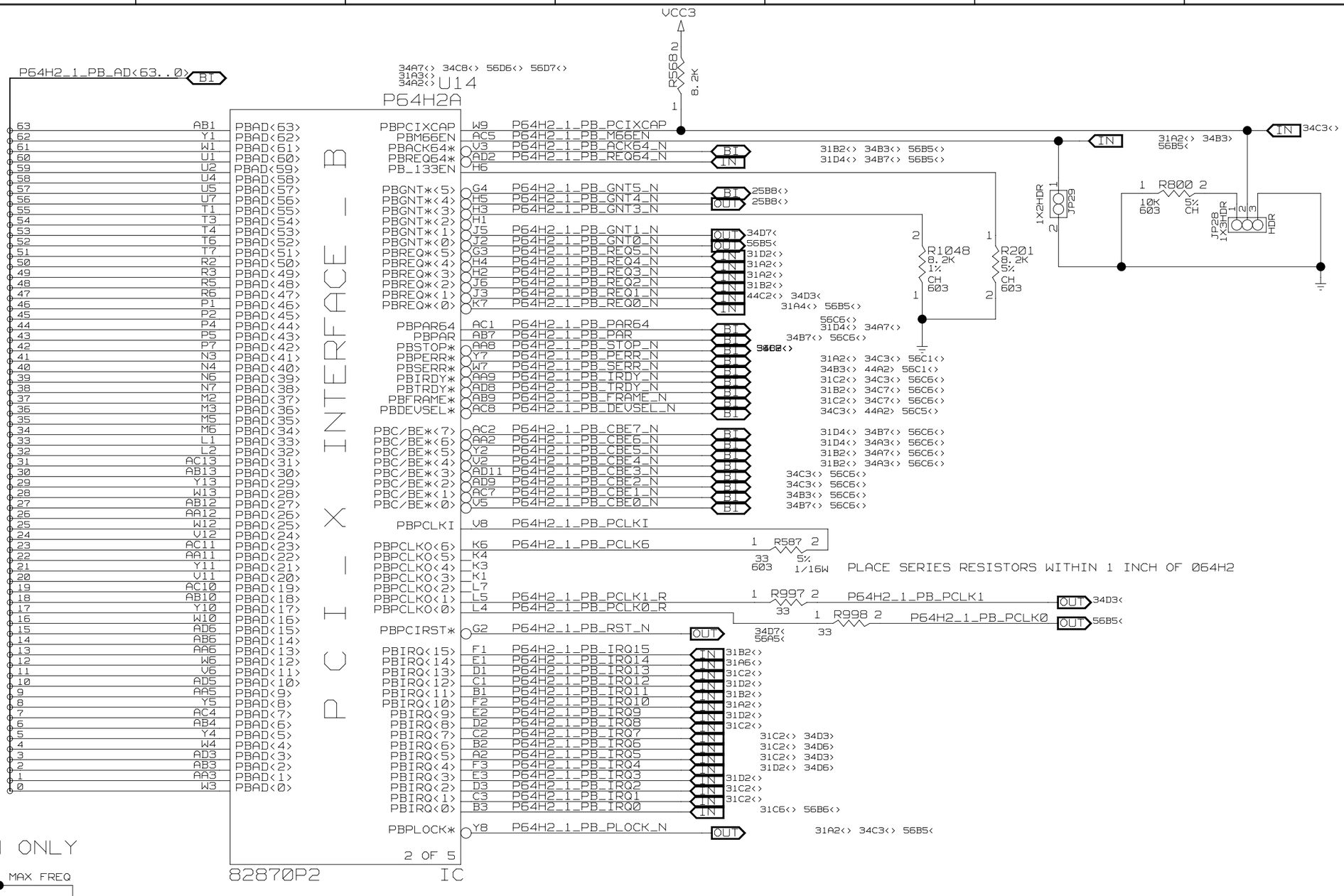
PAGE	REV
20	A2.1

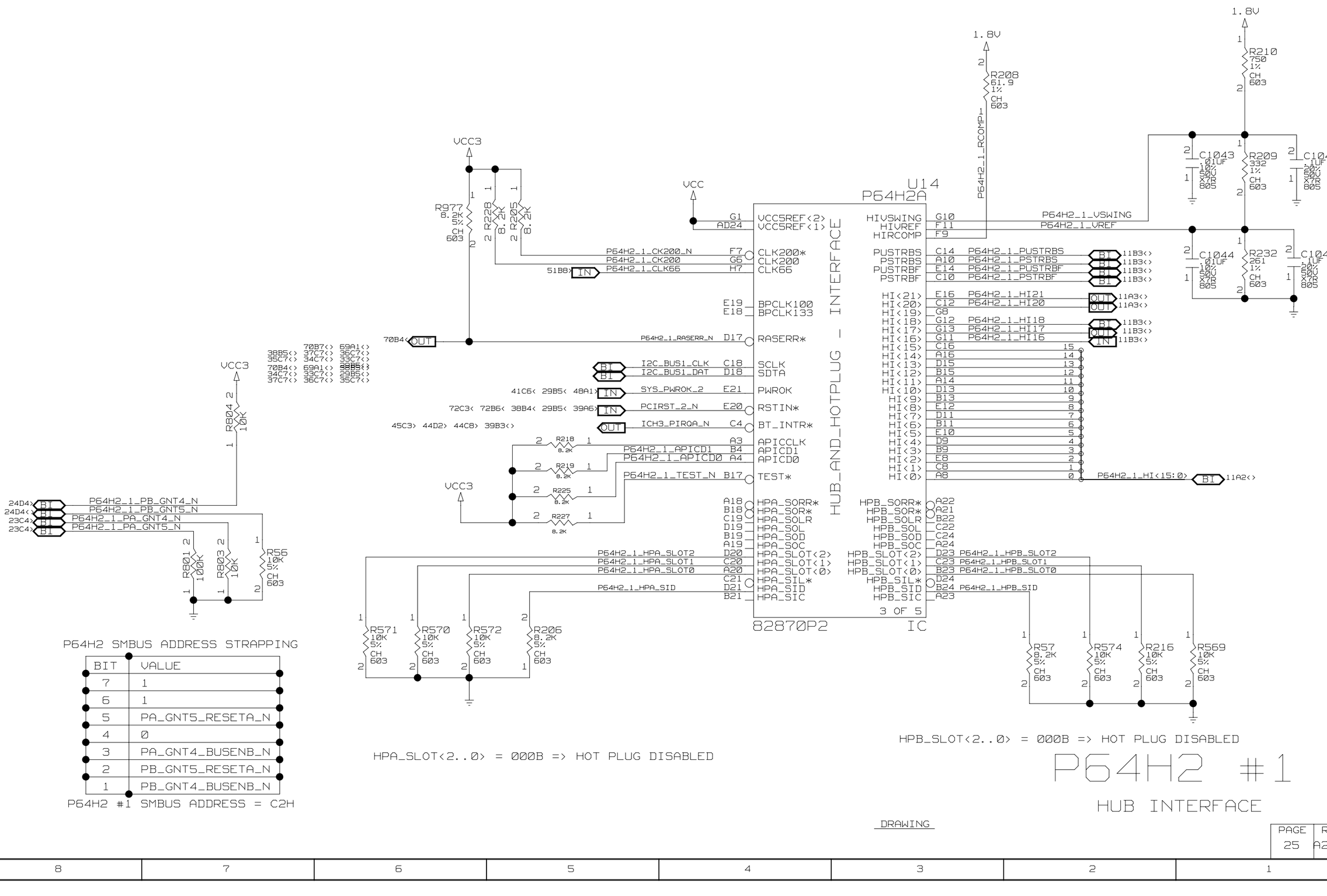


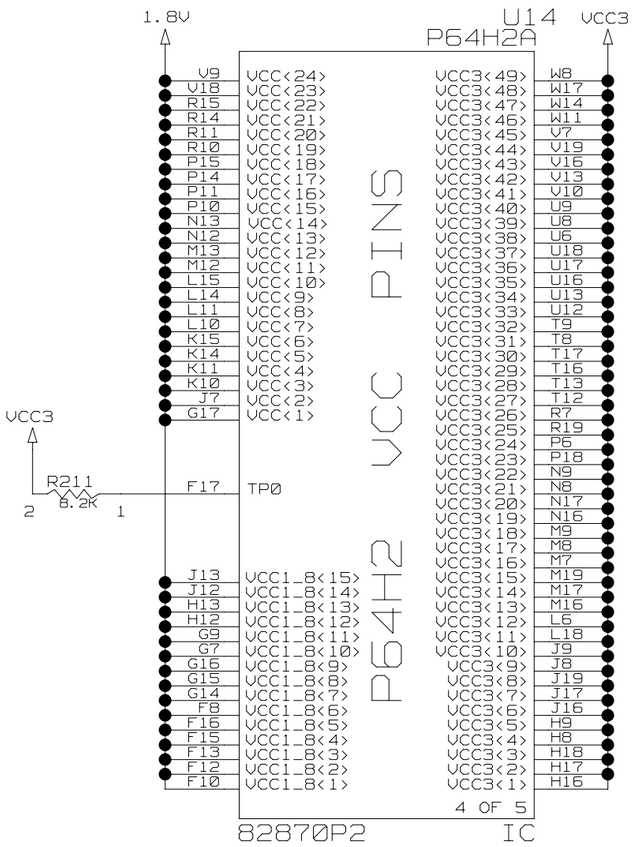
PAGE	REV
21	A2.1

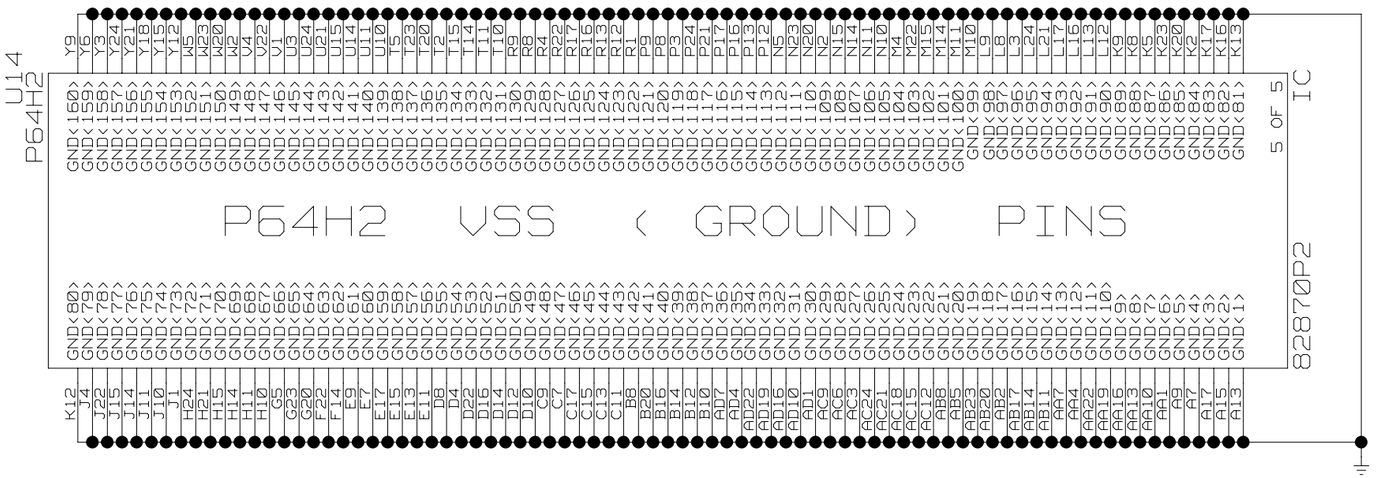

VTT_DDR
DDRB_MA10_R RP255
DDRB_CB2_R RP255
DDRB_CB0_R RP255
DDRB_MA1_R RP255
DDRB_WE_N_R RP256
DDRB_CAS_N_R RP256
DDRB_DQ47_R RP259
DDRB_DQ43_R RP259
DDRB_DQ46_R RP259
DDRB_DQ42_R RP259
DDRB_DQ56_R RP260
DDRB_DQ60_R RP260
DDRB_DQ51_R RP260
DDRB_DQ50_R RP260
DDRB_DQ45_R RP261
DDRB_DQ41_R RP261
DDRB_DQS14_R RP261
DDRB_DQS5_R RP261
RP262
DDRB_DQ44_R RP263
DDRB_DQ40_R RP263
DDRA_RAS_N_R RP263
DDRA_BA0_R RP263
DDRB_DQS4_R RP264
DDRB_DQ34_R RP264
DDRB_DQS13_R RP264
DDRB_DQ38_R RP264
DDRB_MA9_R RP265
DDRB_MA11_R RP265
DDRB_DQ21_R RP265
DDRB_DQS2_R RP265
DDRB_DQ14_R RP266
DDRB_DQ15_R RP266
DDRB_DQ10_R RP266
DDRB_DQ11_R RP266
DDRB_DQS10_R RP267
DDRB_DQ13_R RP267
DDRB_DQS1_R RP267
DDRB_DQ12_R RP267
DDRB_DQ7_R RP268
DDRB_DQ3_R RP268
DDRB_DQ8_R RP268
DDRB_DQ9_R RP268
DDRA_DQ0_R RP269
DDRA_DQ4_R RP269
DDRA_DQ5_R RP269
DDRA_DQ1_R RP269
DDRB_DQ20_R RP270
DDRB_DQ16_R RP270
DDRB_MA12_R RP270
DDRB_DQ17_R RP270
DDRB_MA8_R RP271
DDRB_DQ19_R RP271
DDRB_DQ23_R RP271
DDRB_MA5_R RP271
VTT_DDR
DDRB_CKE R2008 603
DDRB_DQ31_R RP256
DDRB_MA2_R RP256
DDRB_CB4_R RP256
DDRB_CB5_R RP256
DDRB_DQS9_R RP257
DDRB_DQ58_R RP257
DDRB_DQ63_R RP257
DDRB_DQ62_R RP257
DDRB_DQS15_R RP254
DDRB_DQ54_R RP254
DDRB_DQ55_R RP254
DDRB_DQS6_R RP254
DDRB_CS0_N_R RP253
DDRA_CS0_N_R RP253
DDRA_CS1_N_R RP253
DDRB_CS1_N_R RP253
DDRB_DQ33_R RP252
DDRB_DQ37_R RP252
DDRB_DQ36_R RP252
DDRB_DQ32_R RP252
DDRB_DQ6_R RP251
DDRB_DQ2_R RP251
DDRB_DQS9_R RP251
DDRB_DQS0_R RP251
DDRB_DQS11_R RP250
DDRB_DQ18_R RP250
DDRB_MA7_R RP250
DDRB_DQ22_R RP250
DDRB_DQ29_R RP249
DDRB_DQS3_R RP249
DDRB_DQS12_R RP249
DDRB_MA4_R RP249
DDRB_CB6_R RP248
DDRB_CB3_R RP248
DDRB_BA1_R RP248
DDRB_CB7_R RP248
DDRB_DQ27_R RP243
DDRB_DQ30_R RP243
DDRB_DQ26_R RP243
DDRB_MA3_R RP243
DDRB_DQS7_R RP244
DDRB_DQS16_R RP244
DDRB_DQS7_R RP244
DDRB_DQ61_R RP244
DDRB_DQ48_R RP245
DDRB_DQ52_R RP245
DDRB_DQ49_R RP245
DDRB_DQ53_R RP245
DDRB_DQ25_R RP246
DDRB_MA6_R RP246
DDRB_DQ28_R RP246
DDRB_DQ24_R RP246
DDRB_DQ1_R RP247
DDRB_DQ5_R RP247
DDRB_DQ4_R RP247
DDRB_DQ0_R RP247
C1005 C1007 C1008 C1009 C1010 C1011 C1013 C1012 C1040
C1030 C1031 C1032 C1033 C1034 C1035 C1036 C1037 C1039 C1038
C1029 C1028 C1027 C1026 C1025 C1024 C1023 C1022 C1021 C1020 C1019 C1018 C1016 C1017
C997 C998 C999 C1000 C1001 C1002 C1003 C1004 C1005
C987 C988 C989 C990 C991 C992 C993 C994 C995 C996
C1015 C1014 C981 C983 C984 C985 C986
C1559 C1570 100UF
C2862 1UF
E7500: RTT = 22 OHMS
E7501: RTT = 37.9 OHMS
DRAWING
D D R CHANNEL B TERMINATION
PAGE 22
REV A2.1

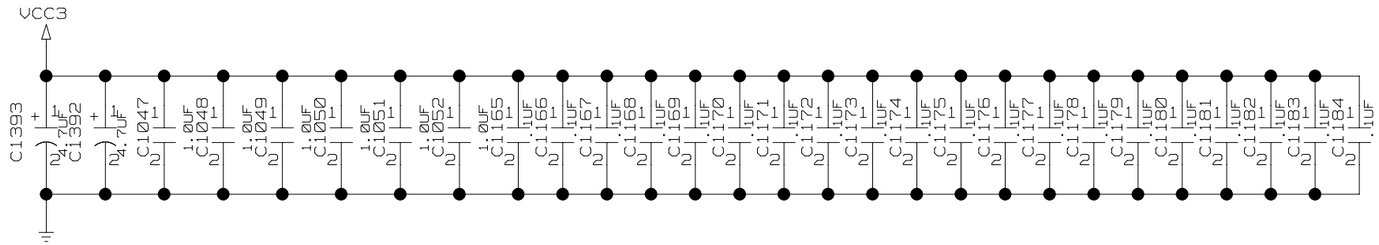

P64H2_1_PA_AD<63..0>
BI
31A7<> 33A2<> 33A7<> 33C8<>
U14
P64H2A
INTERFACE_A
PCI-X
82870P2
IC
1 OF 5
VCC3
R565 2 8.2K
R200 2 8.2K
R798 2 8.2K
R1005 2 8.2K
R799 2
10K
JP24 1X3HDR
JP26 1X2HDR
JP25 1X3HDR
HDR
PAPCIXCAP P22 P64H2_1_PA_PCIXCAP
PAM66EN U20 P64H2_1_PA_M66EN
PAACK64* AB22 P64H2_1_PA_ACK64_N
PAREQ64* Y22 P64H2_1_PA_REQ64_N
PA_133EN E23 P64H2_1_PA_133EN
PAGNT*<5> F22 P64H2_1_PA_GNT5_N
PAGNT*<4> F23 P64H2_1_PA_GNT4_N
PAGNT*<3> F20 P64H2_1_PA_GNT3_N
PAGNT*<2> F18
PAGNT*<1> G22
PAGNT*<0> G19 P64H2_1_PA_GNT0_N
PAREQ*<5> F24 P64H2_1_PA_REQ5_N
PAREQ*<4> F21 P64H2_1_PA_REQ4_N
PAREQ*<3> F19 P64H2_1_PA_REQ3_N
PAREQ*<2> G24 P64H2_1_PA_REQ2_N
PAREQ*<1> G21 P64H2_1_PA_REQ1_N
PAREQ*<0> G18 P64H2_1_PA_REQ0_N
PAPAR64 W21 P64H2_1_PA_PAR64
PAPAR R18 P64H2_1_PA_PAR
PASTOP* R24 P64H2_1_PA_STOP_N
PAPERR* R21 P64H2_1_PA_PERR_N
PASERR* R20 P64H2_1_PA_SERR_N
PAIRDY* P23 P64H2_1_PA_IRDY_N
PATRDY* P20 P64H2_1_PA_TRDY_N
PAFRAME* N18 P64H2_1_PA_FRAME_N
PADEVSEL* P19 P64H2_1_PA_DEVSEL_N
PAC/BE*<7> W22 P64H2_1_PA_CBE7_N
PAC/BE*<6> AD21 P64H2_1_PA_CBE6_N
PAC/BE*<5> AB21 P64H2_1_PA_CBE5_N
PAC/BE*<4> AA21 P64H2_1_PA_CBE4_N
PAC/BE*<3> L22 P64H2_1_PA_CBE3_N
PAC/BE*<2> N19 P64H2_1_PA_CBE2_N
PAC/BE*<1> T24 P64H2_1_PA_CBE1_N
PAC/BE*<0> AA24 P64H2_1_PA_CBE0_N
PAPCLKI V17 P64H2_1_PA_PCLKI
PAPCLKO<6> H23 P64H2_1_PA_PCLK6
PAPCLKO<5> H22
PAPCLKO<4> H20
PAPCLKO<3> H19
PAPCLKO<2> J24
PAPCLKO<1> J23
PAPCLKO<0> J21 P64H2_1_PA_PCLK0_R
PAPCIRST* E24 P64H2_1_PA_RST_N
PAIRQ<15> F4 P64H2_1_PA_IRQ15
PAIRQ<14> E4 P64H2_1_PA_IRQ14
PAIRQ<13> F5 P64H2_1_PA_IRQ13
PAIRQ<12> E5 P64H2_1_PA_IRQ12
PAIRQ<11> D5 P64H2_1_PA_IRQ11
PAIRQ<10> C5 P64H2_1_PA_IRQ10
PAIRQ<9> B5 P64H2_1_PA_IRQ9
PAIRQ<8> A5 P64H2_1_PA_IRQ8
PAIRQ<7> F6 P64H2_1_PA_IRQ7
PAIRQ<6> E6 P64H2_1_PA_IRQ6
PAIRQ<5> D6 P64H2_1_PA_IRQ5
PAIRQ<4> C6 P64H2_1_PA_IRQ4
PAIRQ<3> B6 P64H2_1_PA_IRQ3
PAIRQ<2> A6 P64H2_1_PA_IRQ2
PAIRQ<1> D7 P64H2_1_PA_IRQ1
PAIRQ<0> B7 P64H2_1_PA_IRQ0
PAPLOCK* R23 P64H2_1_PA_PLOCK_N
R586 2 33
R996 2 33
P64H2_1_PA_PCLK0
PLACE SERIES RESISTORS WITHIN 1 INCH OF P64H2
33C2<>
31A6<> 33B3>
31B6<> 33B3<>
31B6<> 33B7<>
25B8<>
33D7<
31C6<>
31A6<>
31B6<> 33D3<
31B6<> 33A7<>
33B7<>
31B6<> 33C7<>
31B6<> 33C2<>
31B6<> 33B2<>
31B6<> 33C7<>
31B6<> 33C7<>
31B6<> 33C2<>
31D8<> 33B7<>
31D8<> 33A3<>
31D8<> 33A7<>
31D8<> 33A3<>
33C3<>
33C2<>
33B2<>
33B7<>
33D3<
31D6<> 33D3>
31D6<> 33D6>
31C6<> 33D3>
31C6<> 33D6>
31B6<> 33C2<>
FOR VALIDATION ONLY
JP26 JP24 JP25 PROTOCOL MAX FREQ
NO JUMPER NO JUMPER NO JUMPER PCI-X 133MHZ
NO JUMPER JUMPER NO JUMPER PCI-X 100MHZ
NO JUMPER JUMPER PIN 1-2 PCI-X 66MHZ
NO JUMPER JUMPER PIN 2-3 PCI 66MHZ
JUMPER JUMPER PIN 2-3 PCI 33MHZ
INTEL(R) P64H2 #1
133MHZ SLOT1
DRAWING
PAGE 23
REV A2.1


P64H2_1_PB_AD<63..0>
U14
P64H2A
X INTERFACE - B
PCI
82870P2 IC
2 OF 5
VCC3
R568 2
8.2K
R587 2
33
5%
1/16W
PLACE SERIES RESISTORS WITHIN 1 INCH OF 064H2
R997 2
R998 2
R1048
8.2K
1%
CH
603
R201
8.2K
5%
R800 2
10K
JP29
1X2HDR
JP28
1X3HDR
HDR
FOR VALIDATION ONLY
JP29 JP28 PROTOCOL MAX FREQ
NO JUMPER | NO JUMPER | PCI-X | 100MHZ
NO JUMPER | PIN 1-2 | PCI-X | 66MHZ
NO JUMPER | PIN 2-3 | PCI | 66MHZ
JUMPER | PIN 2-3 | PCI | 33MHZ
DRAWING
P64H2 #1
100MHZ PCI-X SLOT
AND LAN CONTROLLER
PAGE 24
REV A2.1


U14
P64H2A
HUB_AND_HOTPLUG - INTERFACE
82870P2
IC
3 OF 5
VCC3
VCC
1.8V
VCC5REF<2>
VCC5REF<1>
P64H2_1_CK200_N
P64H2_1_CK200
P64H2_1_CLK66
CLK200*
CLK200
CLK66
BPCLK100
BPCLK133
RASERR*
SCLK
SDTA
PWROK
RSTIN*
BT_INTR*
APICCLK
APICD1
APICD0
TEST*
HPA_SORR*
HPA_SOR*
HPA_SOLR
HPA_SOL
HPA_SOD
HPA_SOC
HPA_SLOT<2>
HPA_SLOT<1>
HPA_SLOT<0>
HPA_SIL*
HPA_SID
HPA_SIC
HIVSWING
HIVREF
HIRCOMP
P64H2_1_RCOMP
P64H2_1_VSWING
P64H2_1_VREF
PUSTRBS
PSTRBS
PUSTRBF
PSTRBF
HI<21>
HI<20>
HI<18>
HI<17>
HI<16>
HI<15:0>
HPB_SORR*
HPB_SOR*
HPB_SOLR
HPB_SOL
HPB_SOD
HPB_SOC
HPB_SLOT<2>
HPB_SLOT<1>
HPB_SLOT<0>
HPB_SIL*
HPB_SID
HPB_SIC
P64H2_1_HPA_SLOT2
P64H2_1_HPA_SLOT1
P64H2_1_HPA_SLOT0
P64H2_1_HPA_SID
P64H2_1_HPB_SLOT2
P64H2_1_HPB_SLOT1
P64H2_1_HPB_SLOT0
P64H2_1_HPB_SID
R977 8.2K 5%
R228 8.2K
R205 8.2K
R208 61.9 1%
R210 750 1%
R209 332 1%
R232 261 1%
C1043 .01UF 10% 50V X7R 805
C1041 .1UF 20% 50V X7R 805
C1044 .01UF 10% 50V X7R 805
C1042 .1UF 20% 50V X7R 805
R804 10K
R801 100K
R803 10K
R56 10K 5%
R218 8.2K
R219 8.2K
R225 8.2K
R227 8.2K
R571 10K 5%
R570 10K 5%
R572 10K 5%
R206 8.2K 5%
R57 8.2K 5%
R574 10K 5%
R216 10K 5%
R569 10K 5%
CH 603
P64H2 SMBUS ADDRESS STRAPPING
BIT
VALUE
7 1
6 1
5 PA_GNT5_RESETA_N
4 0
3 PA_GNT4_BUSENB_N
2 PB_GNT5_RESETA_N
1 PB_GNT4_BUSENB_N
P64H2 #1 SMBUS ADDRESS = C2H
HPA_SLOT<2..0> = 000B => HOT PLUG DISABLED
HPB_SLOT<2..0> = 000B => HOT PLUG DISABLED
P64H2 #1
HUB INTERFACE
DRAWING
PAGE 25
REV A2.1





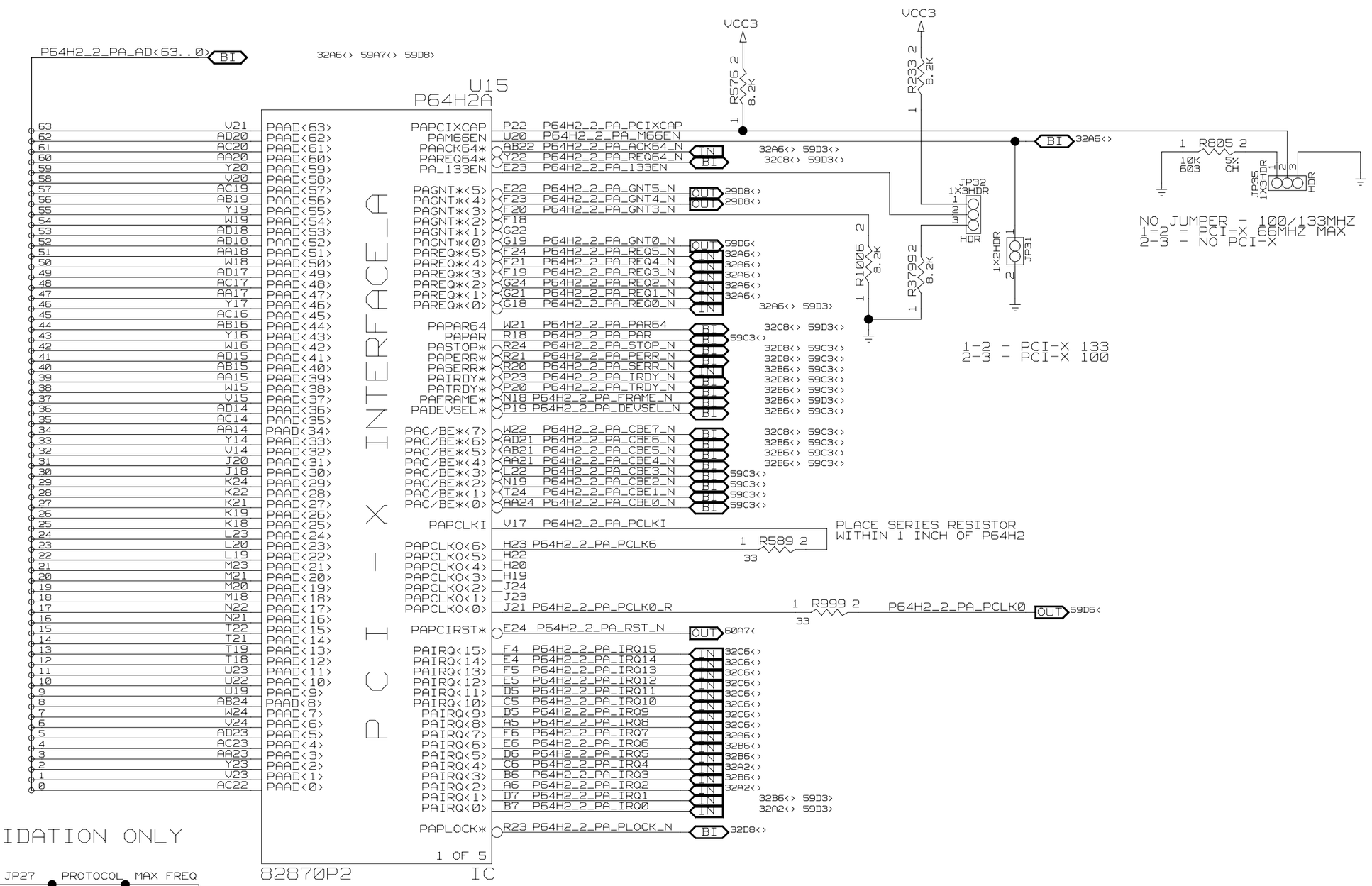


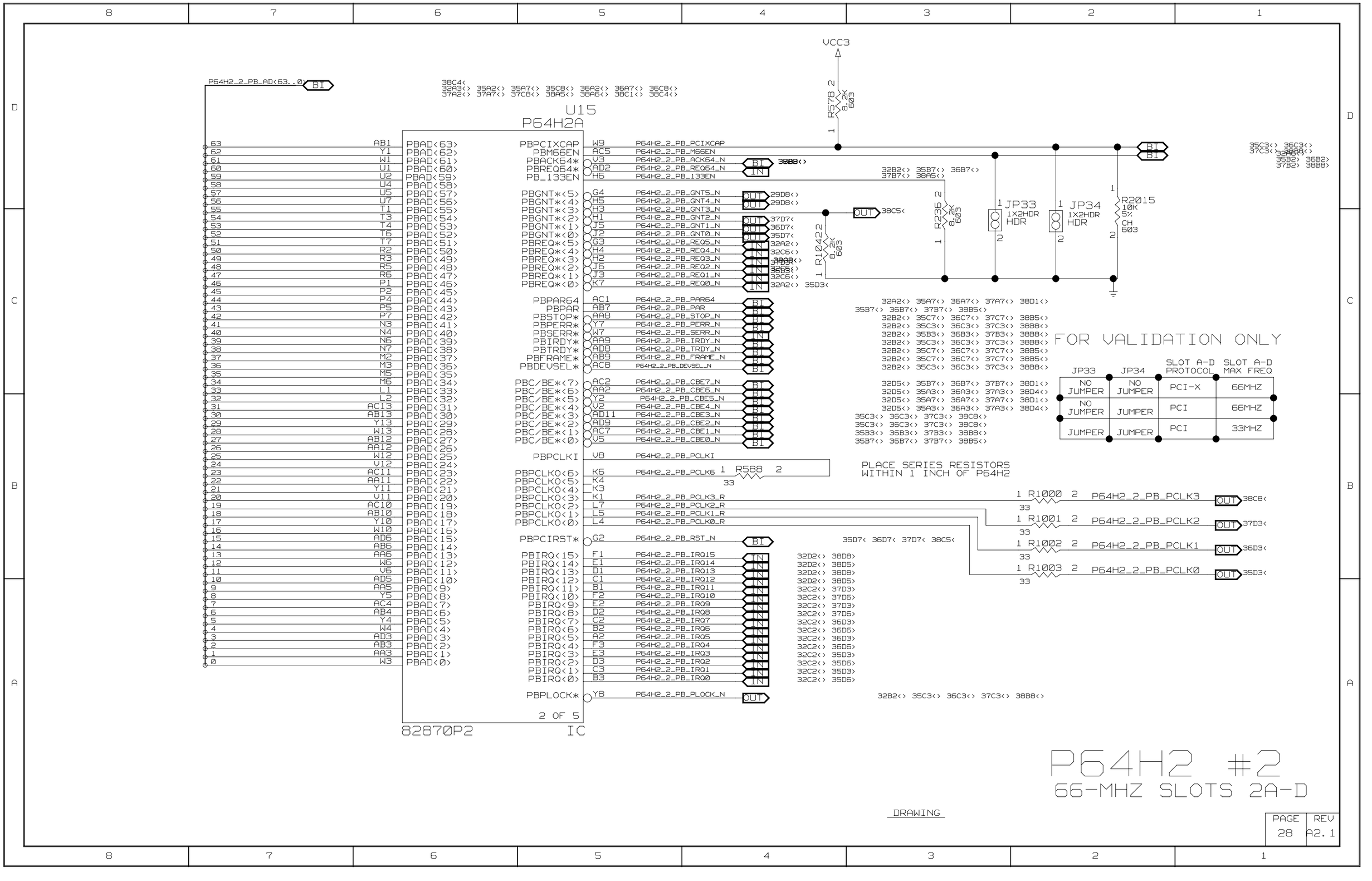
P64H2 #1

POWER AND DECOUPLING

DRAWING

PAGE	REV
26	A2.1


P64H2_2_PA_AD<63..0>
32A6<> 59A7<> 59D8>
U15
P64H2A
PCI-X INTERFACE_A
82870P2 IC
1 OF 5
VCC3
R576 2 8.2K
R233 2 8.2K
R1005 2 8.2K
R37992 8.2K
JP32 1X3HDR
JP31 1X2HDR
R805 2 10K 5% 603
JP35 1X3HDR
NO JUMPER - 100/133MHZ
1-2 - PCI-X 66MHZ MAX
2-3 - NO PCI-X
1-2 - PCI-X 133
2-3 - PCI-X 100
PLACE SERIES RESISTOR WITHIN 1 INCH OF P64H2
R589 2 33
R999 2 33
P64H2_2_PA_PCLK0
FOR VALIDATION ONLY
JP31 JP32 JP27 PROTOCOL MAX FREQ
NO JUMPER NO JUMPER NO JUMPER PCI-X 133MHZ
NO JUMPER JUMPER NO JUMPER PCI-X 100MHZ
NO JUMPER JUMPER PIN 1-2 PCI-X 66MHZ
NO JUMPER JUMPER PIN 2-3 PCI 66MHZ
JUMPER JUMPER PIN 2-3 PCI 33MHZ
P64H2 #2
SCSI CONTROLLER
DRAWING
PAGE 27
REV A2.1


P64H2_2_PB_AD<63..0>
U15
P64H2A
82870P2
IC
2 OF 5
VCC3
R578 2 8.2K 603
R1042 2 8.2K 603
R235 2 8.2K 603
JP33 1X2HDR HDR
JP34 1X2HDR HDR
R2015 10K 5% CH 603
FOR VALIDATION ONLY
JP33 JP34 SLOT A-D PROTOCOL SLOT A-D MAX FREQ
NO JUMPER NO JUMPER PCI-X 66MHZ
NO JUMPER JUMPER PCI 66MHZ
JUMPER JUMPER PCI 33MHZ
PLACE SERIES RESISTORS WITHIN 1 INCH OF P64H2
R588 33
R1000 33 P64H2_2_PB_PCLK3
R1001 33 P64H2_2_PB_PCLK2
R1002 33 P64H2_2_PB_PCLK1
R1003 33 P64H2_2_PB_PCLK0
P64H2 #2
66-MHZ SLOTS 2A-D
DRAWING
PAGE 28
REV A2.1

28C4> BI P64H2_2_PB_GNT4_N
28D4> BI P64H2_2_PB_GNT5_N
27D4> BI P64H2_2_PA_GNT4_N
27D4> BI P64H2_2_PA_GNT5_N

R807 10K
R809 10K
R808 10K
R805 10K

P64H2 SMBUS ADDRESS STRAPPING

BIT	VALUE
7	1
6	1
5	PA_GNT5_N
4	0
3	PA_GNT4_N
2	PB_GNT5_N
1	PB_GNT4_N

P64H2 #2 SMBUS ADDRESS = C0H

VCC3

R978 8.2K 1% 1/16W 603
R265 8.2K
R241 8.2K

VCC

U15
P64H2A

	G1	VCC5REF<2>	
	AD24	VCC5REF<1>	
P64H2_2_CK200_N	F7	CLK200*	
P64H2_2_CK200	G5	CLK200	
51B8> IN P64H2_2_CLK66	H7	CLK66	
	E19	BPCLK100	
	E18	BPCLK133	
70B7< OUT P64H2_2_RASERR_N	D17	RASERR*	
38B5< 37C7< 36C7< 35C7< 34C7< 33C7< 25C5< 70B7< 69A1< I2C_BUS1_CLK BI	C18	SCLK	
37C7< 36C7< 35C7< 34C7< 33C7< 25C5< 70B4< 69A1< 38B5< 41C6< 25B5< 48A1< I2C_BUS1_DAT BI	D18	SDTA	
SYS_PWROK_2 IN	E21	PWROK	
72C3< 72B6< 38B4< 25B5< 39A6> PCIRST_2_N IN	E20	RSTIN*	
44D2> 44C4> 39B3<> ICH3_PIRQB_N OUT	C4	BT_INTR*	
P64H2_2_APICCLK	A3	APICCLK	
P64H2_2_APICD1	B4	APICD1	
P64H2_2_APICD0	A4	APICD0	
P64H2_2_TEST_N	B17	TEST*	
	A18	HPA_SORR*	
	B18	HPA_SOR*	
	C19	HPA_SOLR	
	D19	HPA_SOL	
	B19	HPA_SOD	
	A19	HPA_SOC	
P64H2_2_HPA_SLOT2	D20	HPA_SLOT<2>	
P64H2_2_HPA_SLOT1	C20	HPA_SLOT<1>	
P64H2_2_HPA_SLOT0	A20	HPA_SLOT<0>	
	C21	HPA_SIL*	
P64H2_2_HPA_SID	D21	HPA_SID	
	B21	HPA_SIC	
		3 OF 5	

82870P2 IC

R240 10K
R254 8.2K
R253 8.2K
R252 8.2K

R812 10K
R1051 10K
R1050 10K
R1043 8.2K

HPA_SLOT<2..0> = 000B => HOT PLUG DISABLED

1.8V

R258 61.9 1% CH 603

	G10	P64H2_2_VSWING	
	F11	P64H2_2_VREF	
	F9	P64H2_2_RCOMP	
PUSTRBS	C14	P64H2_2_PUSTRBS	BI 11C7<>
PSTRBS	A10	P64H2_2_PSTRBS	BI 11C7<>
PUSTRBF	E14	P64H2_2_PUSTRBF	BI 11C7<>
PSTRBF	C10	P64H2_2_PSTRBF	BI 11C7<>
HI<21>	E16	P64H2_2_HI21	OUT 11D7<>
HI<20>	C12	P64H2_2_HI20	OUT 11D7<>
HI<19>	G8		
HI<18>	G12	P64H2_2_HI18	BI 11D7<>
HI<17>	G13	P64H2_2_HI17	OUT 11D7<>
HI<16>	G11	P64H2_2_HI16	IN 11D7<>
HI<15>	C16		15
HI<14>	A16		14
HI<13>	D15		13
HI<12>	B15		12
HI<11>	A14		11
HI<10>	D13		10
HI<9>	B13		9
HI<8>	E12		8
HI<7>	D11		7
HI<6>	B11		6
HI<5>	F10		5
HI<4>	D9		4
HI<3>	B9		3
HI<2>	E8		2
HI<1>	C8		1
HI<0>	A8		0 P64H2_2_HI<15:0> BI 11D7<>

HPB_SORR*	A22		
HPB_SOR*	A21		
HPB_SOLR	B22		
HPB_SOL	C22		
HPB_SOD	C24		
HPB_SOC	A24		
HPB_SLOT<2>	D23	P64H2_2_HPB_SLOT2	
HPB_SLOT<1>	C23	P64H2_2_HPB_SLOT1	
HPB_SLOT<0>	B23	P64H2_2_HPB_SLOT0	
HPB_SIL*	D24		
HPB_SID	B24	P64H2_2_HPB_SID	
HPB_SIC	A23		

R146 8.2K 5% CH 603

RS81 10K
RS82 10K
RS80 10K

HPB_SLOT<2..0> = 000B => HOT PLUG DISABLED

1.8V

R260 750 1% CH 603

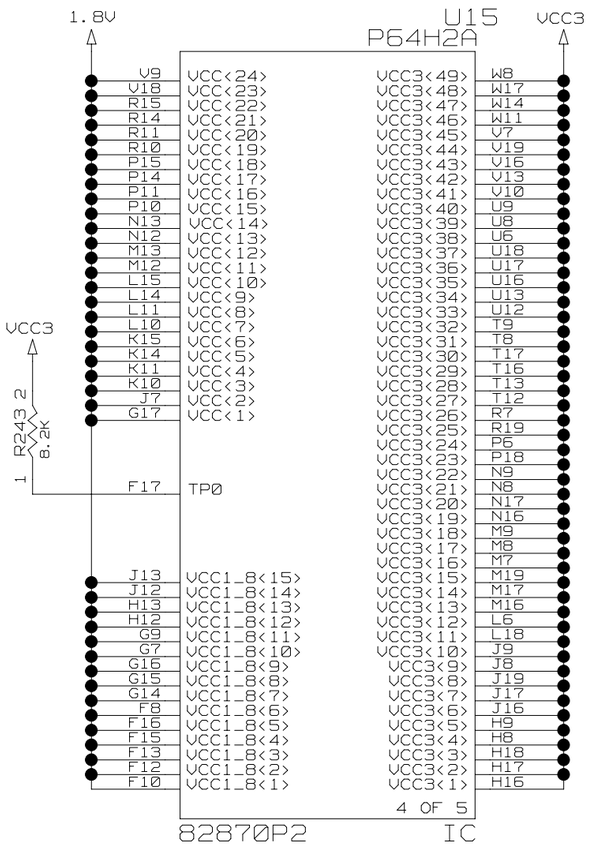
C1055 .01UF 10% 50V X7R 805
R259 332 1% CH 603
C1053 .01UF 10% 50V X7R 805

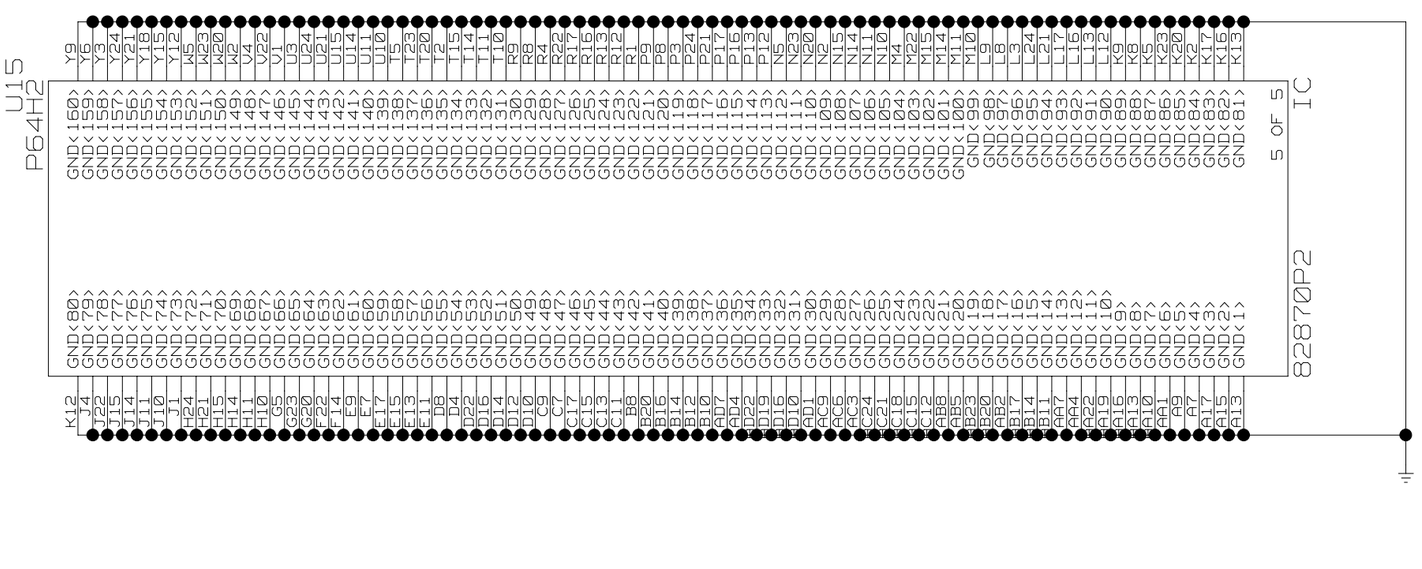
C1056 .01UF 10% 50V X7R 805
R257 261 1% CH 603
C1054 .01UF 10% 50V X7R 805

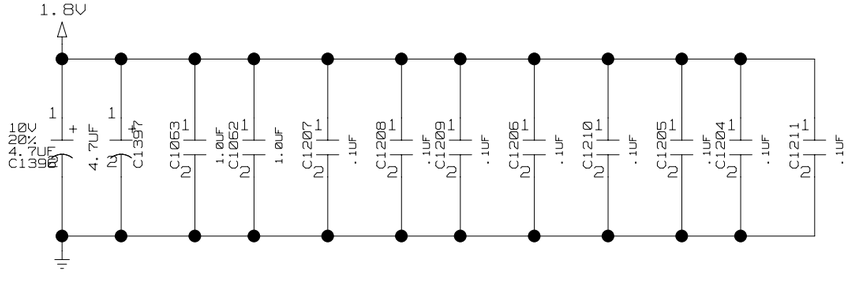
P64H2 #2
HUB INTERFACE

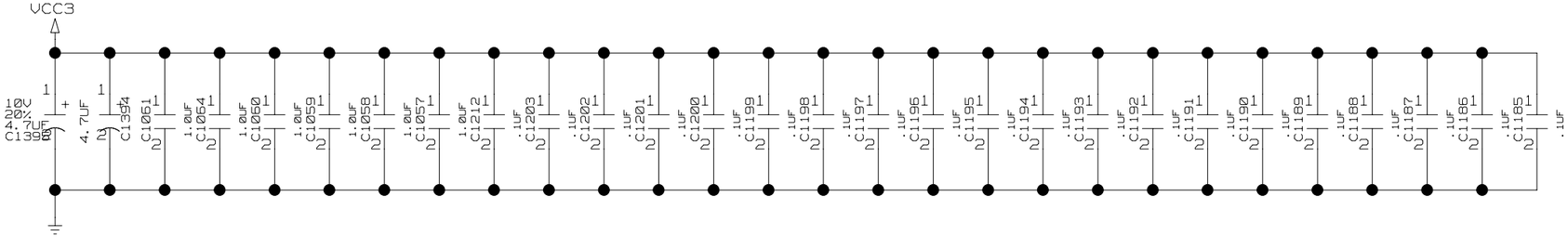
DRAWING

PAGE	REV
29	A2.1







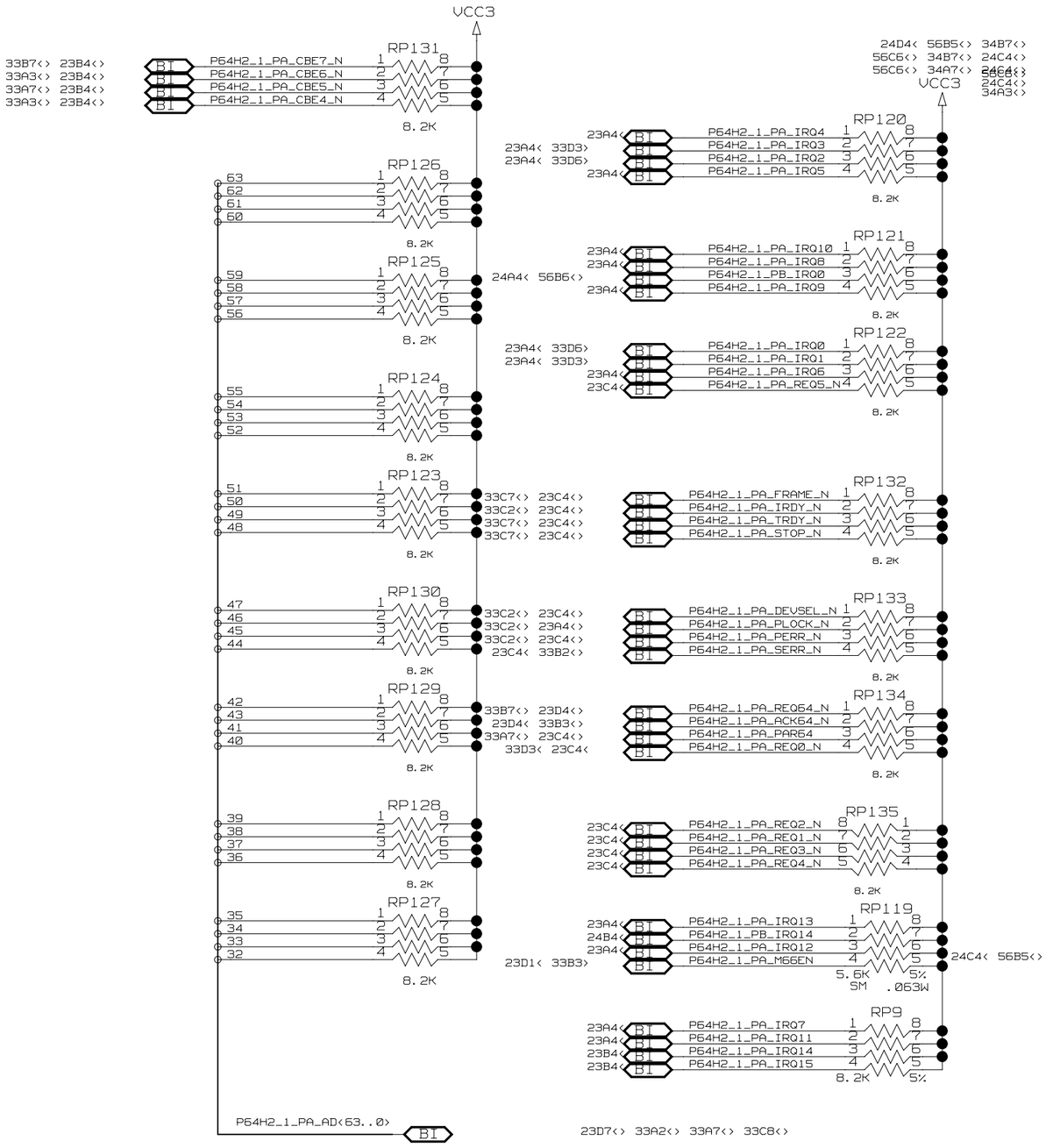


P64H2 #2
POWER AND DECOUPLING

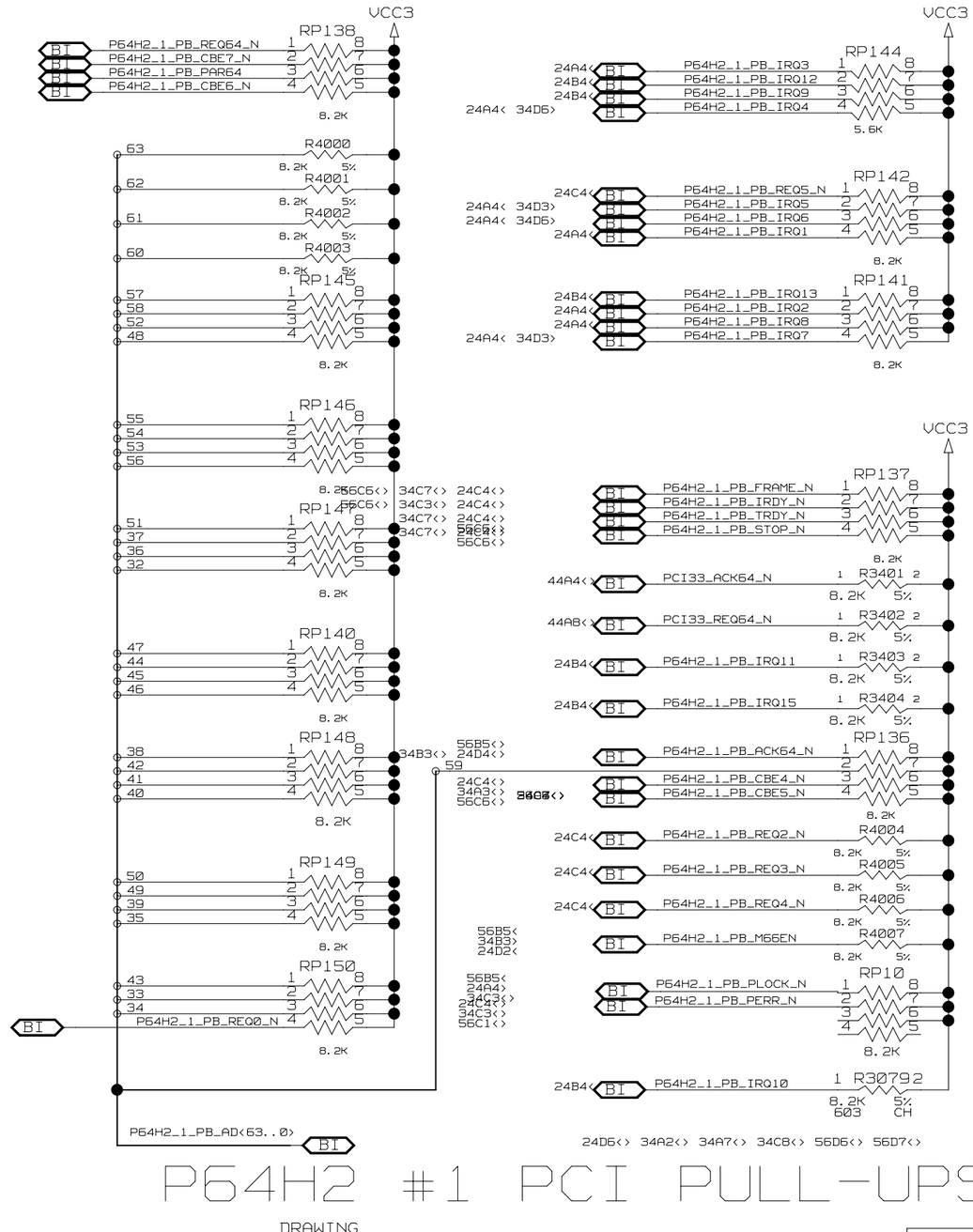
DRAWING

PAGE	REV
30	A2.1

P64H2 #1 PCI BUS A PULL-UPS



P64H2 #1 PCI BUS B PULL-UPS



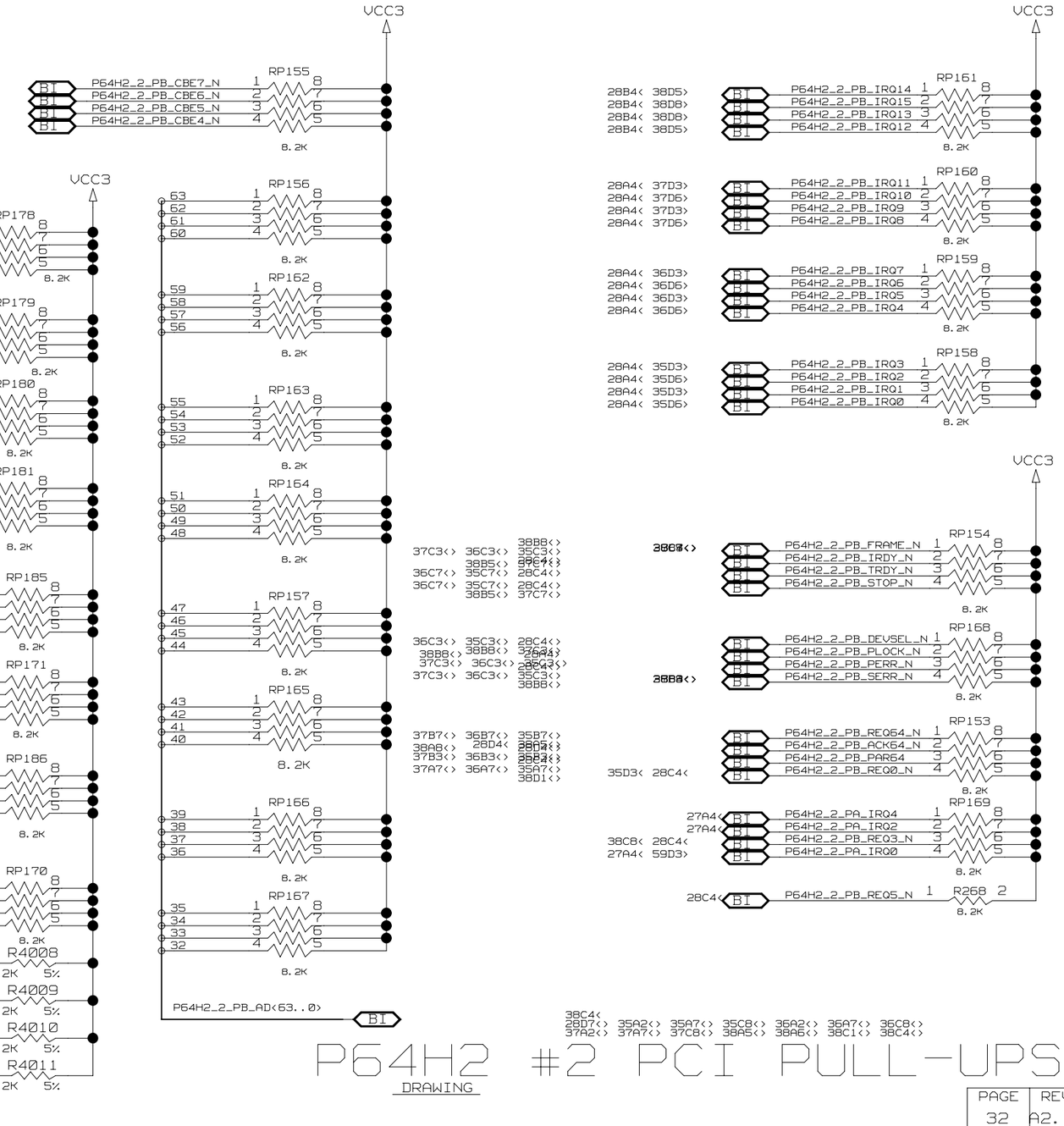
P64H2 #1 PCI PULL-UPS

DRAWING

PAGE	REV
31	A2.1

P64H2 #2 PCI BUS A PULL-UPS

P64H2 #2 PCI BUS B PULL-UPS



P64H2 #2 PCI PULL-UPS

DRAWING

PAGE	REV
32	A2.1

PCI_X_3V

J20

CONN

VCC3 +12VPC -12VPC VSBY3_3 VCC

PCI_SLOTS_TRST_N SLOT_1A_TMS SLOT_1A_TDI P64H2_1_PA_IRQ0 P64H2_1_PA_IRQ2 SLOT_1A_3VAUX P64H2_1_PA_RST_N P64H2_1_PA_GNT0_N ICH3_PME_N SLOT_1A_PME_N P64H2_1_PA_AD<17> SLOT_1A_IDSEL P64H2_1_PA_FRAME_N P64H2_1_PA_TRDY_N P64H2_1_PA_STOP_N I2C_BUS1_CLK I2C_BUS1_DAT P64H2_1_PA_PAR P64H2_1_PA_CBE0_N P64H2_1_PA_REQ64_N P64H2_1_PA_CBE7_N P64H2_1_PA_CBE5_N P64H2_1_PA_PAR64 P64H2_1_PA_AD<63..0>

PCI_SLOTS_TCK P64H2_1_PA_IRQ1 P64H2_1_PA_IRQ3 P64H2_1_PA_PCLK0 P64H2_1_PA_REQ0_N P64H2_1_PA_CBE3_N P64H2_1_PA_CBE2_N P64H2_1_PA_IRDY_N P64H2_1_PA_DEVSEL_N P64H2_1_PA_PCIXCAP P64H2_1_PA_PLOCK_N P64H2_1_PA_PERR_N P64H2_1_PA_SERR_N P64H2_1_PA_CBE1_N P64H2_1_PA_M66EN P64H2_1_PA_ACK64_N P64H2_1_PA_CBE6_N P64H2_1_PA_CBE4_N

R275 5.6K R966 5.6K R965 5.6K R272 0 CH 603 R271 0 CH 603 R273 100 R270 5.6K

C1217 .1UF C1218 .1UF C1399 22UF 1210

C1215 .1UF C1214 .1UF C1213 .1UF C1216 .1UF C1398 22UF 1210

C1220 .1UF C1401 22.0UF C1219 .1UF C1400 22.0UF

PCIX SLOT 1 (133MHZ)
P64H2 #1, PCI BUS A
IDSEL = AD17
REQ#/GNT# = 0
IRQ#<0..3>
PCLK 0

DRAWING

PAGE	REV
33	A2.1

PCI_X_3V

J21

CONN

VCC3 +12VPC -12VPC VSBY3_3 VCC

PCI_SLOTS_TRST_N
SLOT_1B_TMS
SLOT_1B_TDI
P64H2_1_PB_IRQ4
P64H2_1_PB_IRQ6
SLOT_1B_3VAUX
P64H2_1_PB_RST_N
P64H2_1_PB_GNT1_N
ICH3_PME_N
SLOT_1B_PME_N
P64H2_1_PB_AD<18>
SLOT_1B_IDSEL
P64H2_1_PB_FRAME_N
P64H2_1_PB_TRDY_N
P64H2_1_PB_STOP_N
I2C_BUS1_CLK
I2C_BUS1_DAT
P64H2_1_PB_PAR
P64H2_1_PB_CBE0_N
P64H2_1_PB_REQ64_N
P64H2_1_PB_CBE7_N
P64H2_1_PB_CBE5_N
P64H2_1_PB_PAR64
P64H2_1_PB_AD<63..0>

PCI_SLOTS_TCK
P64H2_1_PB_IRQ5
P64H2_1_PB_IRQ7
P64H2_1_PB_PCLK1
P64H2_1_PB_REQ1_N
P64H2_1_PB_CBE3_N
P64H2_1_PB_CBE2_N
P64H2_1_PB_IRDY_N
P64H2_1_PB_DEVSEL_N
P64H2_1_PB_PCIXCAP
P64H2_1_PB_PLOCK_N
P64H2_1_PB_PERR_N
P64H2_1_PB_SERR_N
P64H2_1_PB_CBE1_N
P64H2_1_PB_M66EN
P64H2_1_PB_ACK64_N
P64H2_1_PB_CBE6_N
P64H2_1_PB_CBE4_N
P64H2_1_PB_AD<63..0>

PCIX SLOT 2 (100MHZ)
P64H2 #1, PCI BUS B
IDSEL = AD18
REQ#/GNT# = 1
IRQ#<4..7>
PCLK1

DRAWING

PAGE	REV
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PCI_X_3V

J23

CONN

VCC3 +12VPC -12VPC VSBY3_3 VCC

PCI_SLOTS_TRST_N
SLOT_2A_TMS
SLOT_2A_TDI
P64H2_2_PB_IRQ0
P64H2_2_PB_IRQ2
SLOT_2A_3VAUX
P64H2_2_PB_RST_N
P64H2_2_PB_GNT0_N
ICH3_PME_N
SLOT_2A_PME_N
P64H2_2_PB_AD<17>
SLOT_2A_IDSEL
P64H2_2_PB_FRAME_N
P64H2_2_PB_TRDY_N
P64H2_2_PB_STOP_N
I2C_BUS1_CLK
I2C_BUS1_DAT
P64H2_2_PB_PAR
P64H2_2_PB_CBE0_N
P64H2_2_PB_REQ64_N
P64H2_2_PB_CBE7_N
P64H2_2_PB_CBE5_N
P64H2_2_PB_PAR64
P64H2_2_PB_AD<63..0>

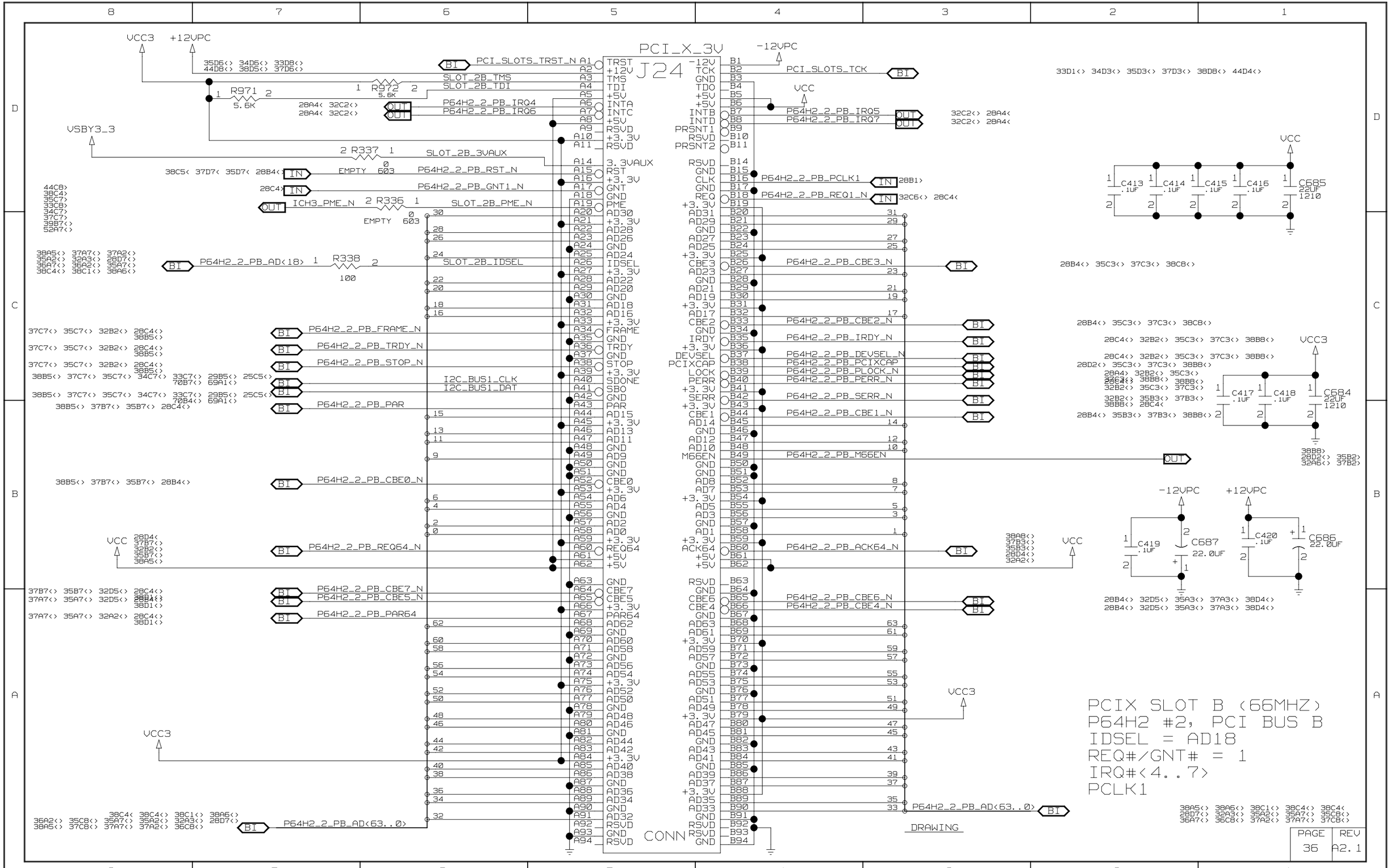
PCI_SLOTS_TCK
P64H2_2_PB_IRQ1
P64H2_2_PB_IRQ3
P64H2_2_PB_PCLK0
P64H2_2_PB_REQ0_N
P64H2_2_PB_CBE3_N
P64H2_2_PB_CBE2_N
P64H2_2_PB_IRDY_N
P64H2_2_PB_DEVSEL_N
P64H2_2_PB_PCIXCAP
P64H2_2_PB_PLOCK_N
P64H2_2_PB_PERR_N
P64H2_2_PB_SERR_N
P64H2_2_PB_CBE1_N
P64H2_2_PB_M66EN
P64H2_2_PB_ACK64_N
P64H2_2_PB_CBE6_N
P64H2_2_PB_CBE4_N

C408 C407 C406 C405 C683 22UF 1210
C410 C409 C680 22UF 1210
C412 C682 22.0UF
C411 C681 22.0UF

PCIX SLOT A (66MHZ)
P64H2 #2, PCI BUS B
IDSEL = AD17
REQ#/GNT# = 0
IRQ#<0..3>
PCLK0

DRAWING

PAGE	REV
35	A2.1


PCI_X_3V
J24
CONN
PCI_SLOTS_TRST_N
SLOT_2B_TMS
SLOT_2B_TDI
P64H2_2_PB_IRQ4
P64H2_2_PB_IRQ6
SLOT_2B_3VAUX
P64H2_2_PB_RST_N
P64H2_2_PB_GNT1_N
ICH3_PME_N
SLOT_2B_PME_N
P64H2_2_PB_AD<18>
SLOT_2B_IDSEL
P64H2_2_PB_FRAME_N
P64H2_2_PB_TRDY_N
P64H2_2_PB_STOP_N
I2C_BUS1_CLK
I2C_BUS1_DAT
P64H2_2_PB_PAR
P64H2_2_PB_CBE0_N
P64H2_2_PB_REQ64_N
P64H2_2_PB_CBE7_N
P64H2_2_PB_CBE5_N
P64H2_2_PB_PAR64
P64H2_2_PB_AD<63..0>
PCI_SLOTS_TCK
P64H2_2_PB_IRQ5
P64H2_2_PB_IRQ7
P64H2_2_PB_PCLK1
P64H2_2_PB_REQ1_N
P64H2_2_PB_CBE3_N
P64H2_2_PB_CBE2_N
P64H2_2_PB_IRDY_N
P64H2_2_PB_DEVSEL_N
P64H2_2_PB_PCIXCAP
P64H2_2_PB_PLOCK_N
P64H2_2_PB_PERR_N
P64H2_2_PB_SERR_N
P64H2_2_PB_CBE1_N
P64H2_2_PB_M66EN
P64H2_2_PB_ACK64_N
P64H2_2_PB_CBE6_N
P64H2_2_PB_CBE4_N
P64H2_2_PB_AD<63..0>
VCC
VCC3
VSBY3_3
+12VPC
-12VPC
R971
R972
R337
R336
R338
EMPTY
C413
C414
C415
C416
C685
C417
C418
C684
C419
C687
C420
C686
PCIX SLOT B (66MHZ)
P64H2 #2, PCI BUS B
IDSEL = AD18
REQ#/GNT# = 1
IRQ#<4..7>
PCLK1
DRAWING
PAGE
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REV
A2.1

PCIX SLOT C (66MHZ)
P64H2 #2, PCI BUS B
IDSEL = AD19
REQ#/GNT# = 2
IRQ#<8..11>
PCLK2

DRAWING

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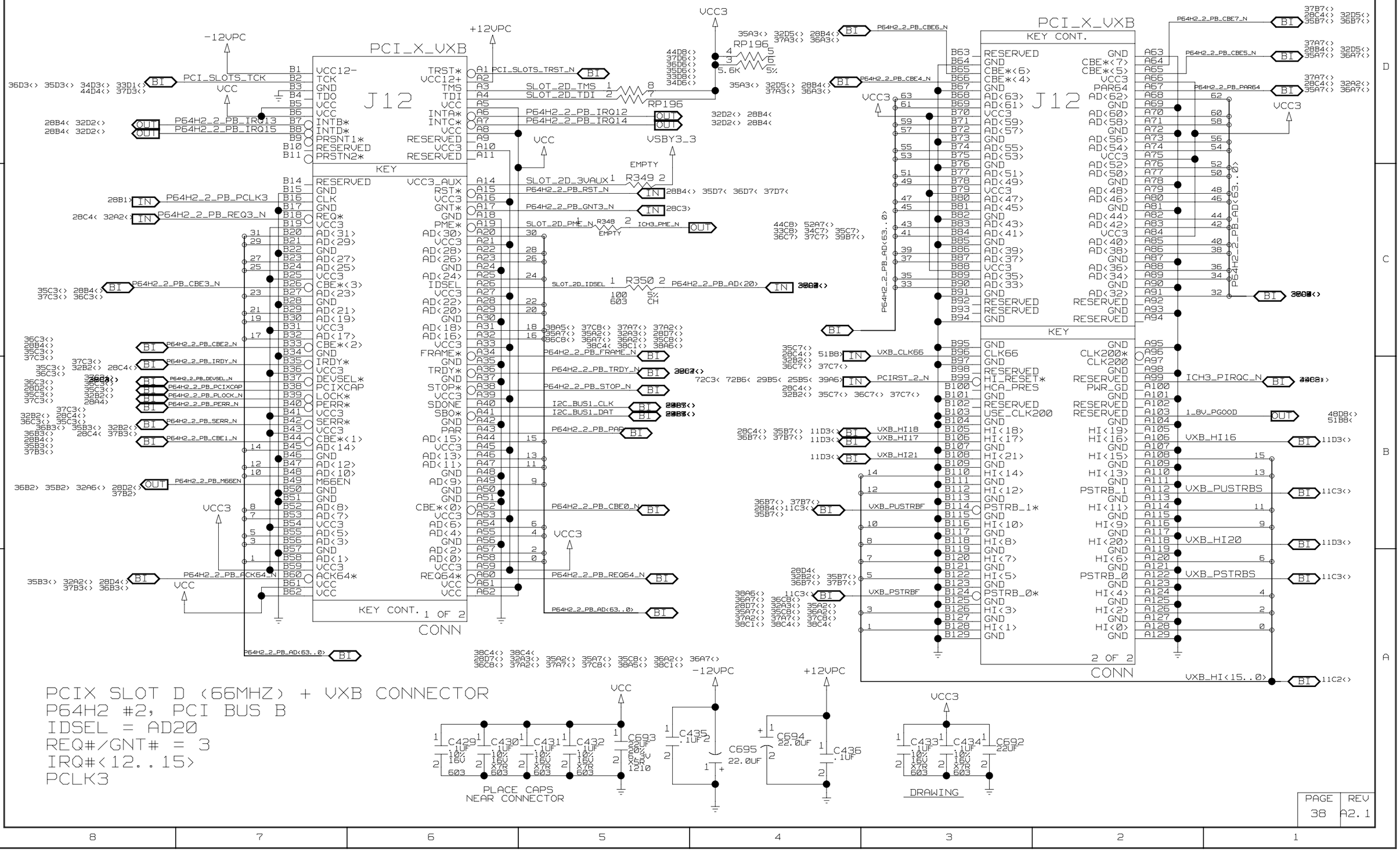
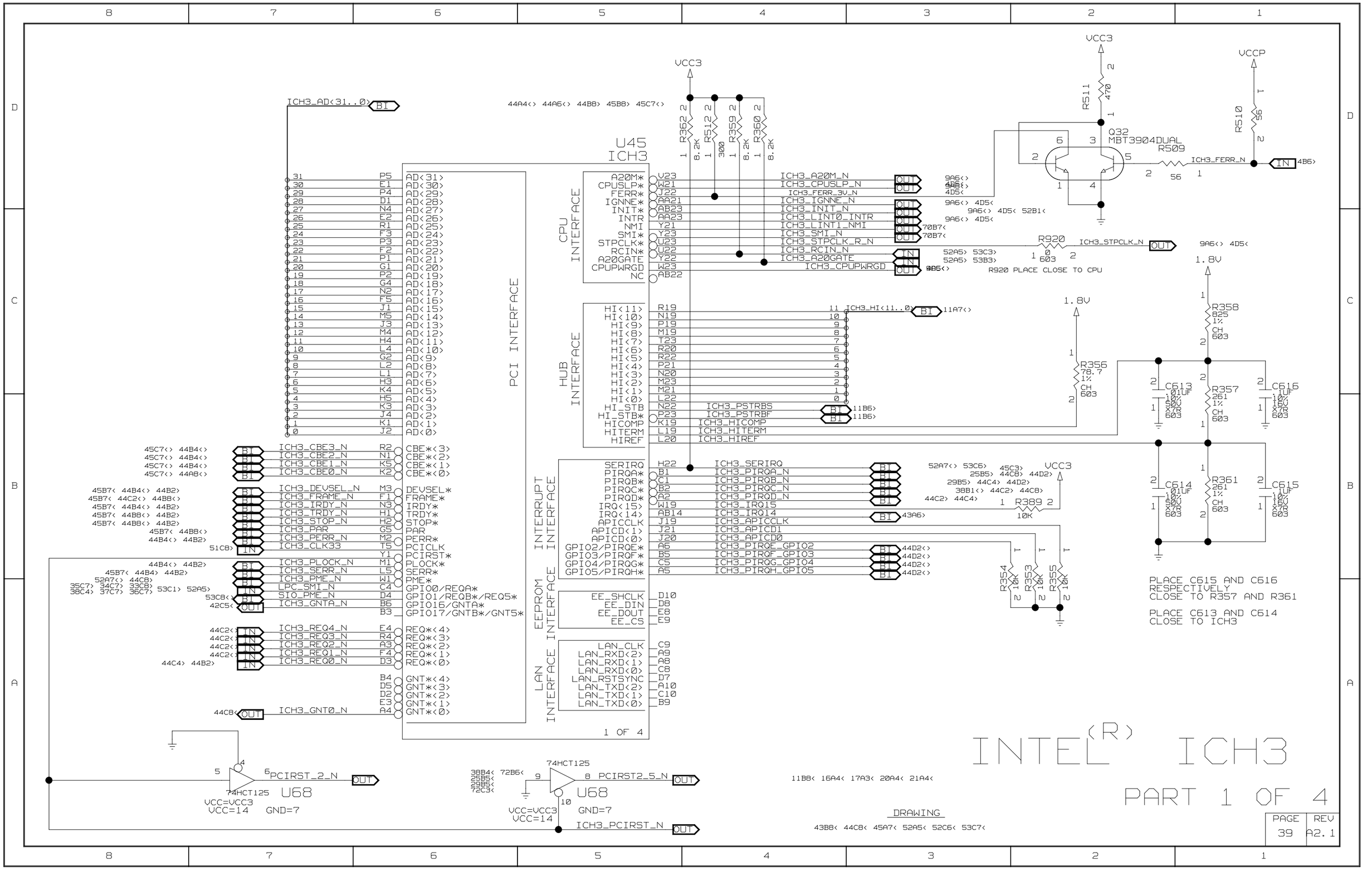

PCI_X_VXB
J12
KEY
KEY CONT. 1 OF 2
CONN
PCI_X_VXB
KEY CONT.
J12
KEY
2 OF 2
CONN
-12VPC
+12VPC
VCC
VCC3
VSBY3_3
PCI_SLOTS_TCK
PCI_SLOTS_TRST_N
SLOT_2D_TMS
SLOT_2D_TDI
SLOT_2D_3VAUX
SLOT_2D_PME_N
SLOT_2D_IDSEL
I2C_BUS1_CLK
I2C_BUS1_DAT
P64H2_2_PB_IRQ12
P64H2_2_PB_IRQ13
P64H2_2_PB_IRQ14
P64H2_2_PB_IRQ15
P64H2_2_PB_RST_N
P64H2_2_PB_GNT3_N
P64H2_2_PB_REQ3_N
P64H2_2_PB_PCLK3
P64H2_2_PB_AD<20>
P64H2_2_PB_FRAME_N
P64H2_2_PB_IRDY_N
P64H2_2_PB_TRDY_N
P64H2_2_PB_DEVSEL_N
P64H2_2_PB_STOP_N
P64H2_2_PB_PCIXCAP
P64H2_2_PB_PLOCK_N
P64H2_2_PB_PERR_N
P64H2_2_PB_SERR_N
P64H2_2_PB_CBE1_N
P64H2_2_PB_PAR
P64H2_2_PB_CBE0_N
P64H2_2_PB_REQ64_N
P64H2_2_PB_ACK64_N
P64H2_2_PB_M66EN
P64H2_2_PB_AD<63..0>
P64H2_2_PB_CBE3_N
P64H2_2_PB_CBE2_N
P64H2_2_PB_CBE7_N
P64H2_2_PB_CBE6_N
P64H2_2_PB_CBE5_N
P64H2_2_PB_CBE4_N
P64H2_2_PB_PAR64
VXB_CLK66
PCIRST_2_N
ICH3_PIRQC_N
1_8V_PGOOD
VXB_HI16
VXB_PUSTRBS
VXB_HI20
VXB_PSTRBS
VXB_HI<15..0>
VXB_HI18
VXB_HI17
VXB_HI21
VXB_PUSTRBF
VXB_PSTRBF
RP196
RP196
R349
R348
R350
PCIX SLOT D (66MHZ) + VXB CONNECTOR
P64H2 #2, PCI BUS B
IDSEL = AD20
REQ#/GNT# = 3
IRQ#<12..15>
PCLK3
PLACE CAPS
NEAR CONNECTOR
DRAWING
PAGE 38
REV A2.1


U45
ICH3
PCI INTERFACE
CPU INTERFACE
HUB INTERFACE
INTERRUPT INTERFACE
EEPROM INTERFACE
LAN INTERFACE
ICH3_AD<31..0>
ICH3_CBE3_N
ICH3_CBE2_N
ICH3_CBE1_N
ICH3_CBE0_N
ICH3_DEVSEL_N
ICH3_FRAME_N
ICH3_IRDY_N
ICH3_TRDY_N
ICH3_STOP_N
ICH3_PAR
ICH3_PERR_N
ICH3_CLK33
ICH3_PLOCK_N
ICH3_SERR_N
ICH3_PME_N
LPC_SMI_N
SIO_PME_N
ICH3_GNTA_N
ICH3_REQ4_N
ICH3_REQ3_N
ICH3_REQ2_N
ICH3_REQ1_N
ICH3_REQ0_N
ICH3_GNT0_N
ICH3_A20M_N
ICH3_CPUSLP_N
ICH3_FERR_3V_N
ICH3_IGNNE_N
ICH3_INIT_N
ICH3_LINT0_INTR
ICH3_LINT1_NMI
ICH3_SMI_N
ICH3_STPCLK_R_N
ICH3_RCIN_N
ICH3_A20GATE
ICH3_CPUPWRGD
ICH3_HI<11..0>
ICH3_PSTRBS
ICH3_PSTRBF
ICH3_HICOMP
ICH3_HITERM
ICH3_HIREF
ICH3_SERIRQ
ICH3_PIRQA_N
ICH3_PIRQB_N
ICH3_PIRQC_N
ICH3_PIRQD_N
ICH3_IRQ15
ICH3_IRQ14
ICH3_APICCLK
ICH3_APICCD1
ICH3_APICCD0
ICH3_PIRQE_GPIO2
ICH3_PIRQF_GPIO3
ICH3_PIRQG_GPIO4
ICH3_PIRQH_GPIO5
EE_SHCLK
EE_DIN
EE_DOUT
EE_CS
LAN_CLK
LAN_RXD<2>
LAN_RXD<1>
LAN_RXD<0>
LAN_RSTSYNC
LAN_TXD<2>
LAN_TXD<1>
LAN_TXD<0>
ICH3_FERR_N
ICH3_STPCLK_N
ICH3_IRQ14
ICH3_PCIRST_N
PCIRST_2_N
PCIRST2_5_N
R362 8.2K
R512 300
R359 8.2K
R360 8.2K
R511 470
R510 56
R509 56
Q32 MBT3904DUAL
R920 0 603
R920 PLACE CLOSE TO CPU
R358 825 1% CH 603
R356 78.7 1% CH 603
R357 261 1% CH 603
R361 261 1% CH 603
R389 10K
R354 10K
R353 10K
R355 10K
C613 .01UF 10% 50V X7R 603
C614 .01UF 10% 50V X7R 603
C615 .1UF 10% 16V X7R 603
C616 .1UF 10% 16V X7R 603
PLACE C615 AND C616 RESPECTIVELY CLOSE TO R357 AND R361
PLACE C613 AND C614 CLOSE TO ICH3
74HCT125 U68
VCC=VCC3 VCC=14 GND=7
1 OF 4
INTEL(R) ICH3
PART 1 OF 4
DRAWING
PAGE 39
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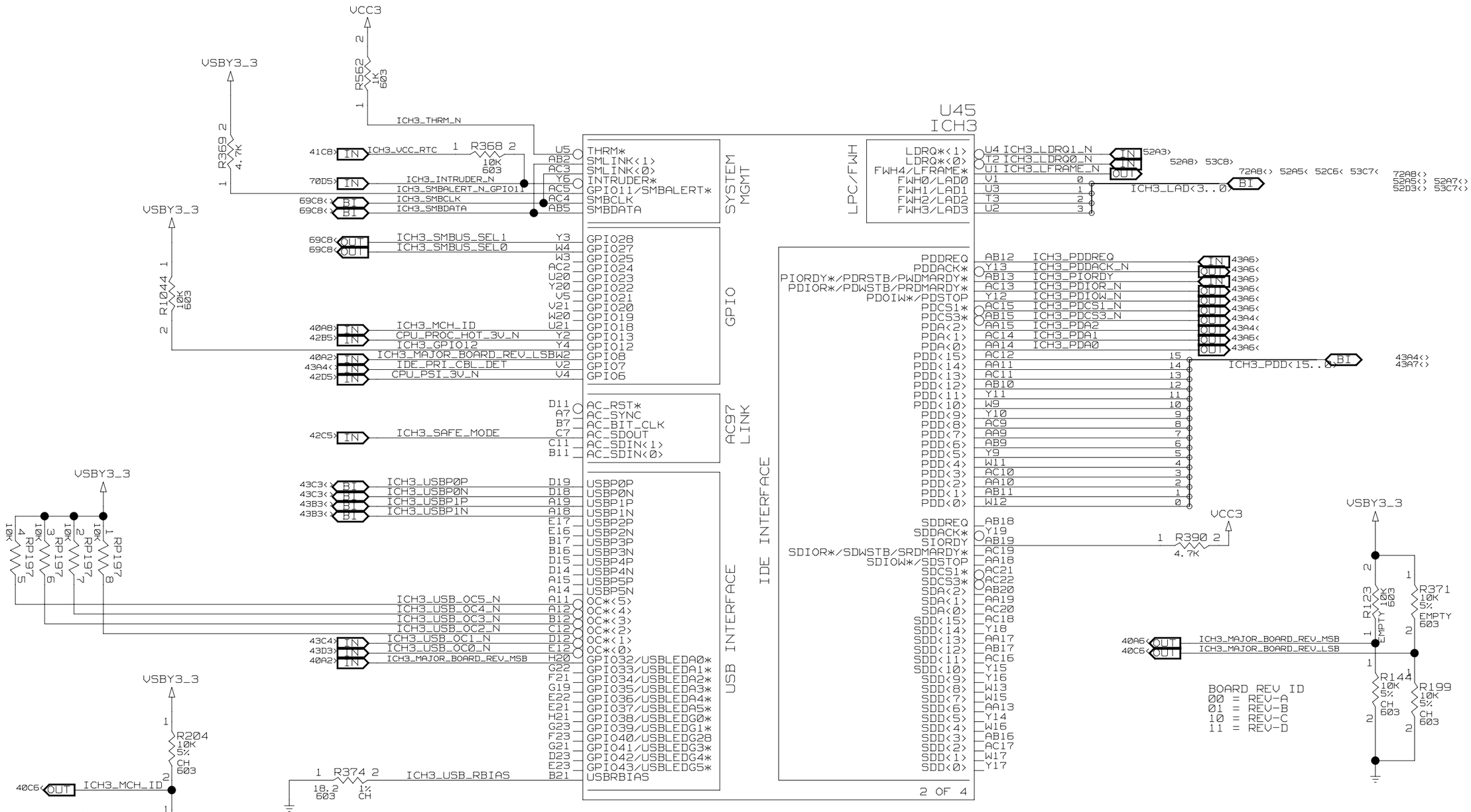
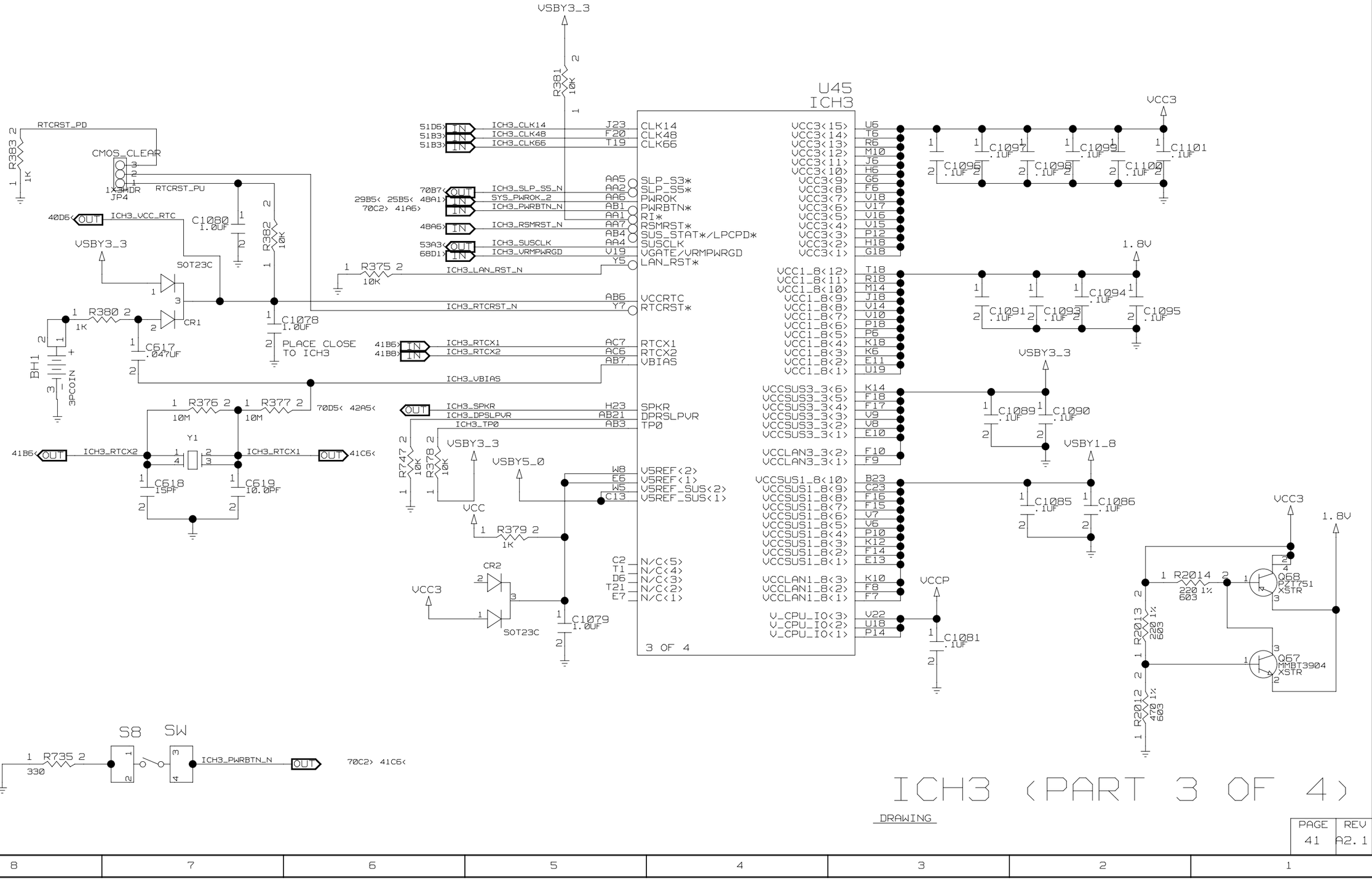


ICH3 (PART 2 OF 4)

DRAWING

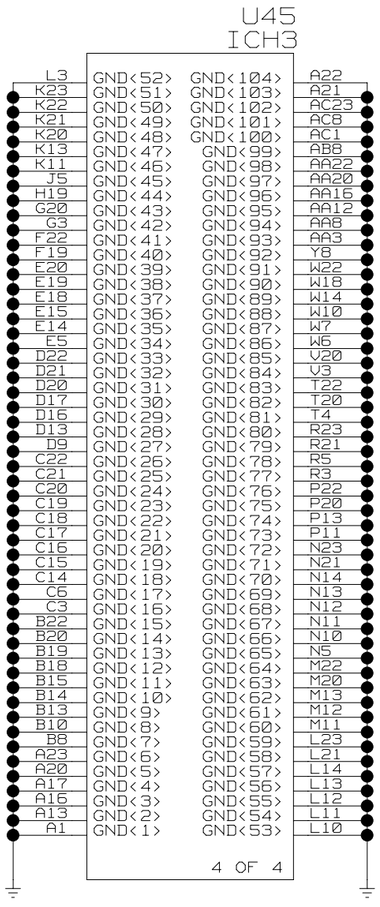
PAGE	REV
40	A2.1

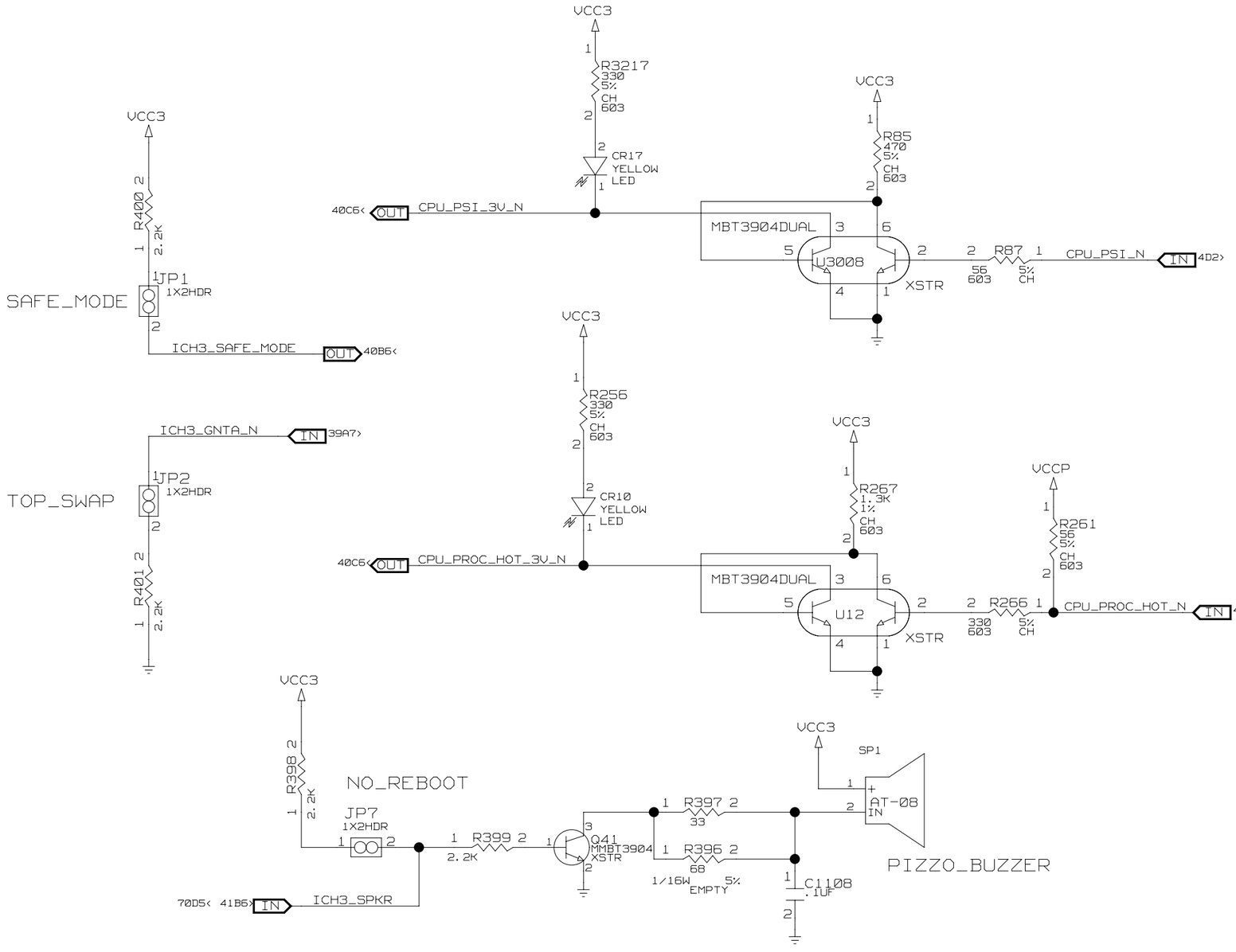


ICH3 (PART 3 OF 4)

DRAWING

PAGE	REV
41	A2.1





STRAP OPTIONS AND SPEAKER CIRCUITRY

ICH3 (PART 4 OF 4)

DRAWING

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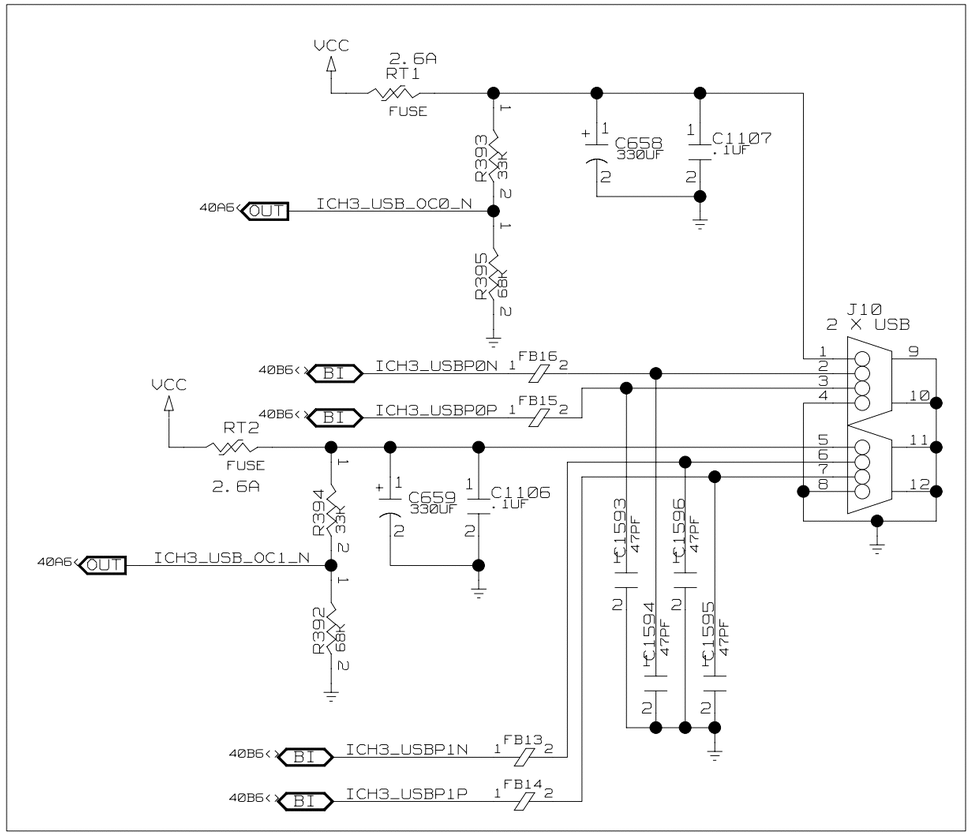
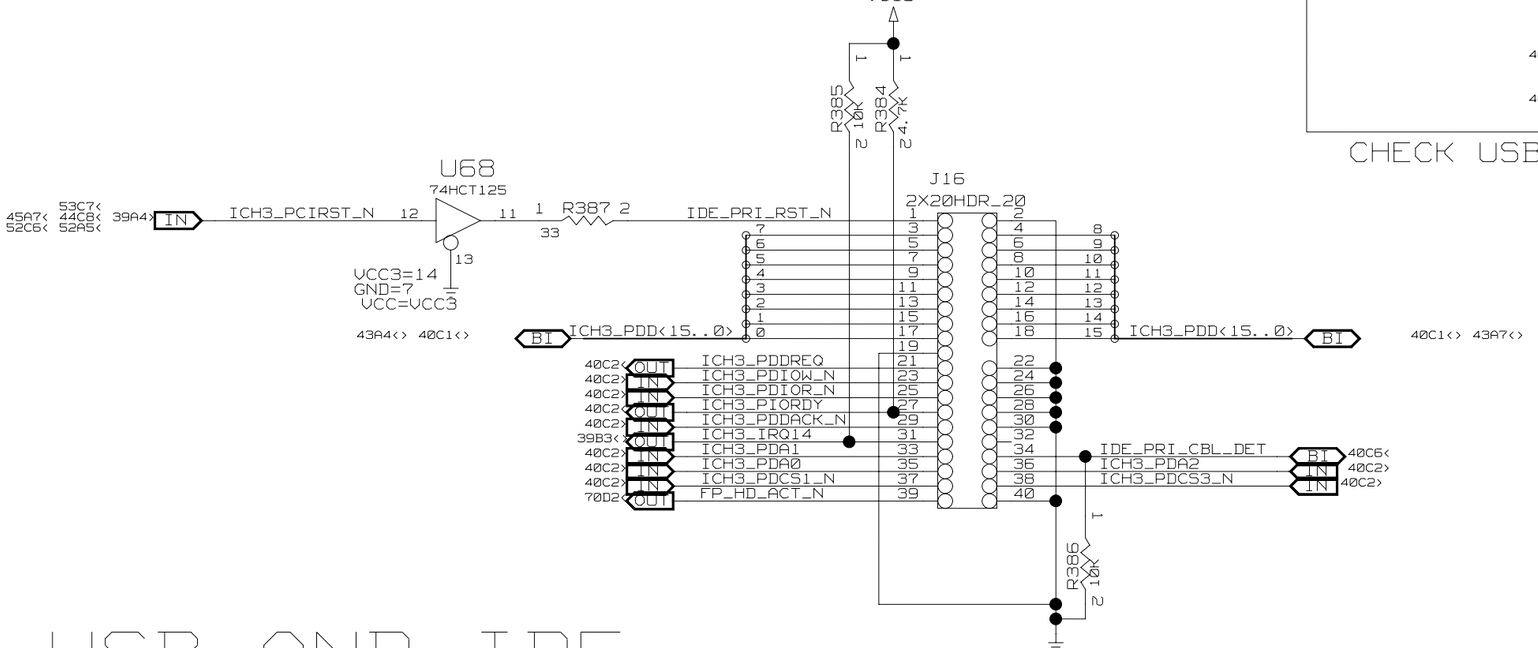


CHECK USB DESIGN GUIDELINES



USB AND IDE

DRAWING

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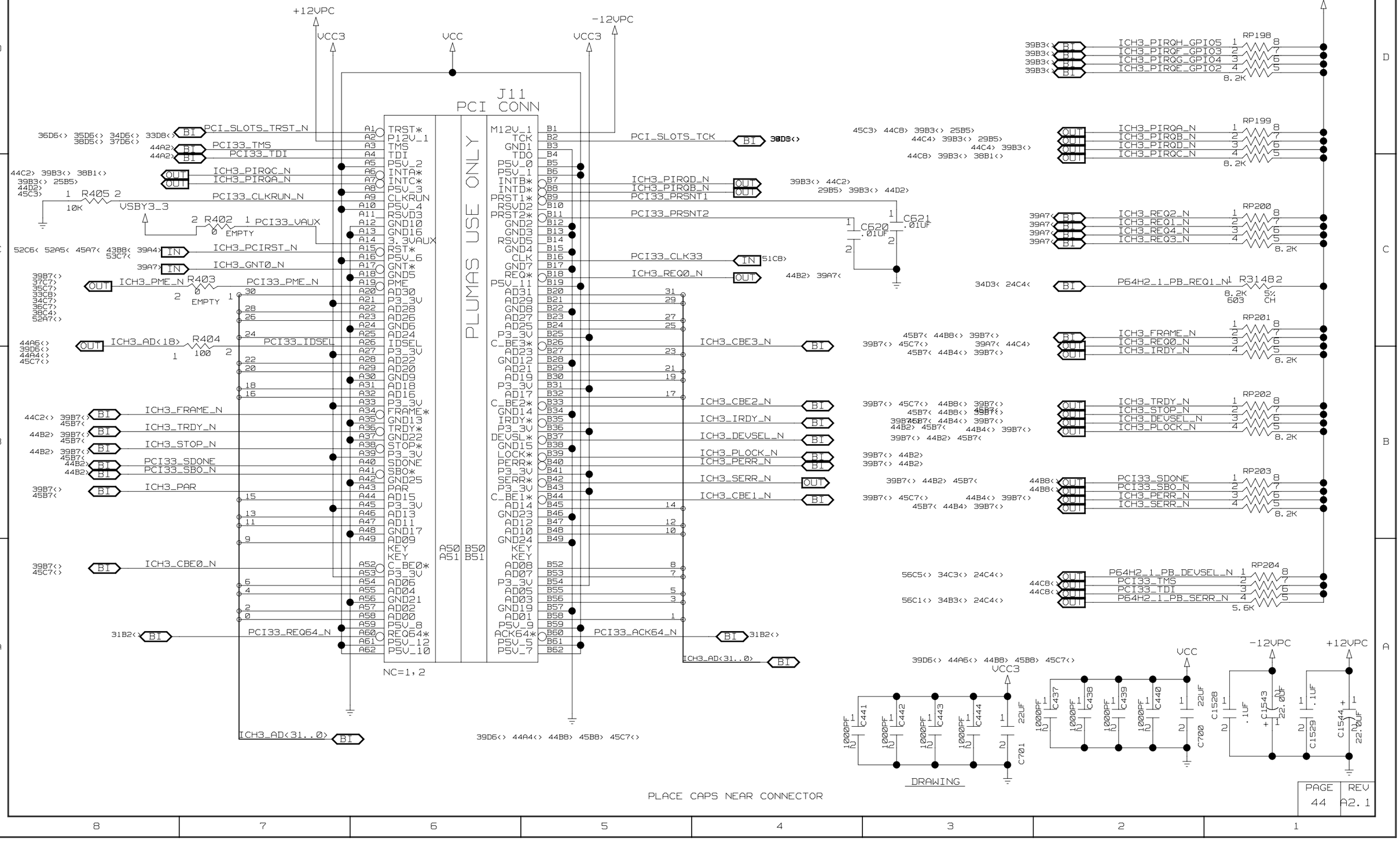
PCI-33 (ICH3) CONNECTOR, TERMINATION, AND DECOUPLING



PLACE CAPS NEAR CONNECTOR

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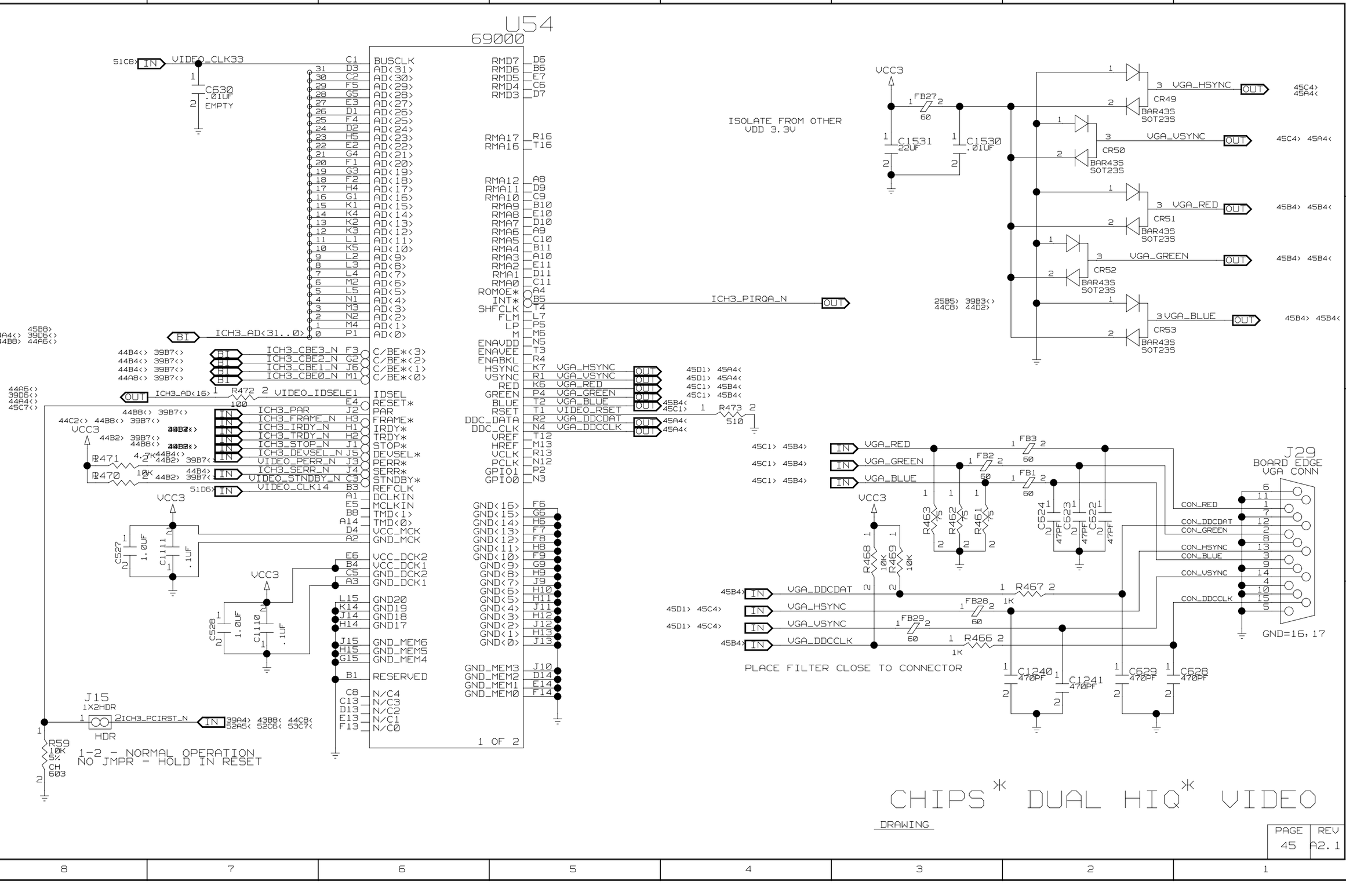
U54
69000
51C8> IN VIDEO_CLK33
C630 .01UF EMPTY
51D6> IN VIDEO_CLK14
AD<31> AD<30> AD<29> AD<28> AD<27> AD<26> AD<25> AD<24> AD<23> AD<22> AD<21> AD<20> AD<19> AD<18> AD<17> AD<16> AD<15> AD<14> AD<13> AD<12> AD<11> AD<10> AD<9> AD<8> AD<7> AD<6> AD<5> AD<4> AD<3> AD<2> AD<1> AD<0>
BI ICH3_AD<31..0>
ICH3_CBE3_N ICH3_CBE2_N ICH3_CBE1_N ICH3_CBE0_N
C/BE*<3> C/BE*<2> C/BE*<1> C/BE*<0>
OUT ICH3_AD<16> R472 100 VIDEO_IDSEL
IDSEL RESET* PAR FRAME* IRDY* TRDY* STOP* DEVSEL* PERR* SERR* STNDBY* REFCLK DCLKIN MCLKIN TMD<1> TMD<0> VCC_MCK GND_MCK VCC_DCK2 VCC_DCK1 GND_DCK2 GND_DCK1 GND20 GND19 GND18 GND17 GND_MEM6 GND_MEM5 GND_MEM4 RESERVED N/C4 N/C3 N/C2 N/C1 N/C0
ICH3_PAR ICH3_FRAME_N ICH3_IRDY_N ICH3_TRDY_N ICH3_STOP_N ICH3_DEVSEL_N VIDEO_PERR_N ICH3_SERR_N VIDEO_STNDBY_N
R471 4.7K R470 10K
VCC3
C527 1.0UF C1111 .1UF
C528 1.0UF C1110 .1UF
J15 1X2HDR HDR
ICH3_PCIRST_N
R59 10K 5% CH 603
1-2 - NORMAL OPERATION
NO JMPR - HOLD IN RESET
RMD7 RMD6 RMD5 RMD4 RMD3
RMA17 RMA16
RMA12 RMA11 RMA10 RMA9 RMA8 RMA7 RMA6 RMA5 RMA4 RMA3 RMA2 RMA1 RMA0
ROMOE* INT* SHFCLK FLM LP M ENAVDD ENAVEE ENABKL
ICH3_PIRQA_N
HSYNC VSYNC RED GREEN BLUE RSET DDC_DATA DDC_CLK VREF HREF VCLK PCLK GPIO1 GPIO0
VGA_HSYNC VGA_VSYNC VGA_RED VGA_GREEN VGA_BLUE VIDEO_RSET VGA_DDCDAT VGA_DDCCLK
R473 510
GND<16> GND<15> GND<14> GND<13> GND<12> GND<11> GND<10> GND<9> GND<8> GND<7> GND<6> GND<5> GND<4> GND<3> GND<2> GND<1> GND<0>
GND_MEM3 GND_MEM2 GND_MEM1 GND_MEM0
1 OF 2
ISOLATE FROM OTHER VDD 3.3V
VCC3
FB27 60
C1531 22UF C1530 .01UF
VGA_HSYNC VGA_VSYNC VGA_RED VGA_GREEN VGA_BLUE
CR49 CR50 CR51 CR52 CR53
BAR43S SOT23S
J29 BOARD EDGE VGA CONN
CON_RED CON_DDCDAT CON_GREEN CON_HSYNC CON_BLUE CON_VSYNC CON_DDCCLK
GND=16,17
R458 10K R459 10K
R463 75 R462 75 R461 75
C624 47PF C623 47PF C622 47PF
FB3 FB2 FB1 60
R467 1K R466 1K
FB28 FB29
C1240 470PF C1241 470PF C629 470PF C628 470PF
PLACE FILTER CLOSE TO CONNECTOR
CHIPS* DUAL HIQ* VIDEO
DRAWING
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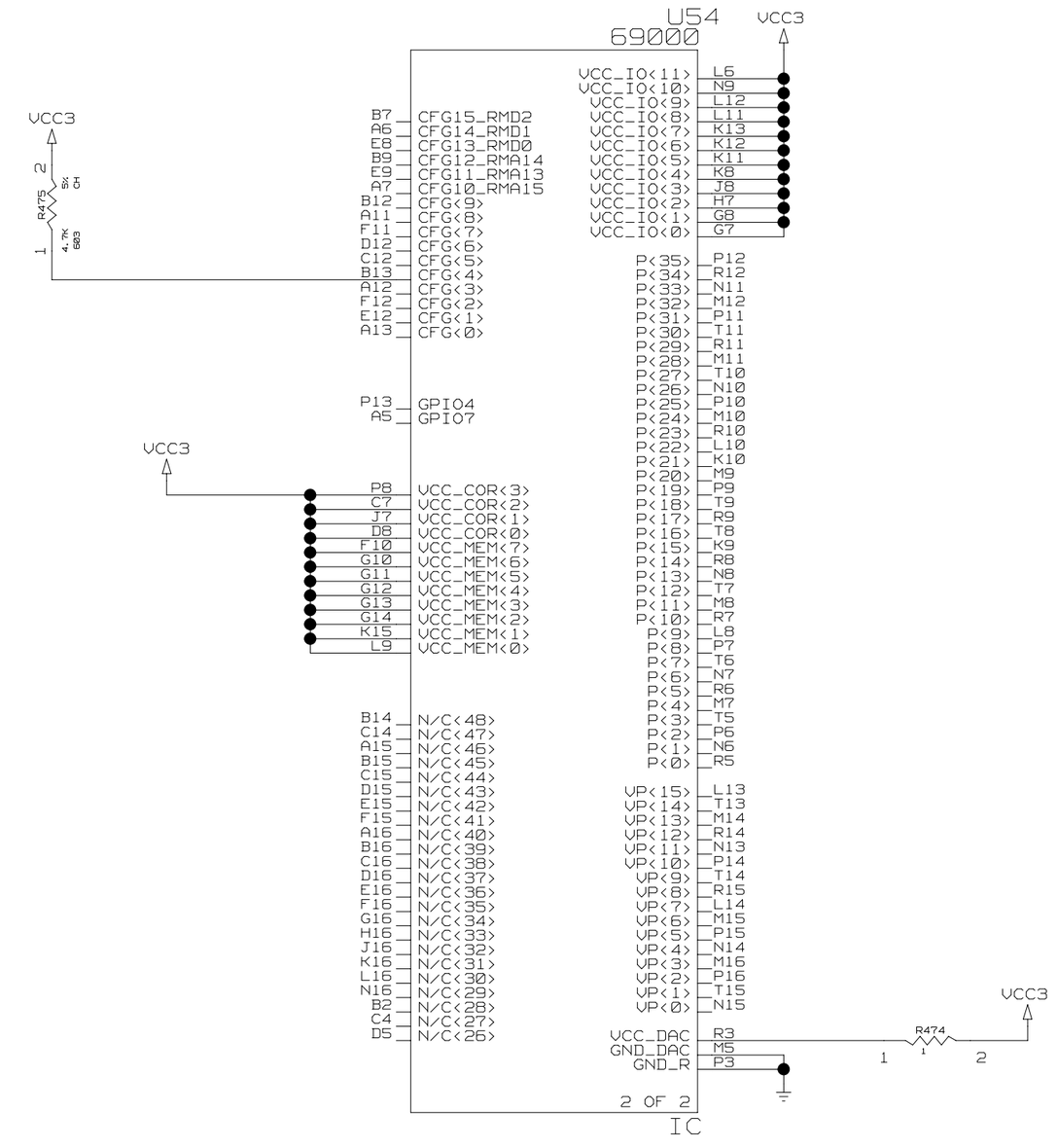

DRAWING

VIDEO

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VTT_DDR SUPPLY

+2.5V SUPPLY

U104 FAN5066

U103 LM2904

U1 LTC1929

Q44 N-MOSFET IC

Q43 N-MOSFET IC

Q1 N-MOSFET IC

Q2 N-MOSFET IC

Q3 N-MOSFET IC

Q4 N-MOSFET IC

Q5 N-MOSFET IC

Q6 N-MOSFET IC

Q7 N-MOSFET IC

Q8 N-MOSFET IC

VCC

VCC3

VQP

2.5V

HIDRV

LODRV

VTT_DDR_L

VTT_DDR

RC5051_ENABLE

VTT_DDR_PGOOD

2_5V_PGOOD

VREF_DDR_MCH

VREF_DDR_DIMM

V2_5_L1

V2_5_L2

V2_5SENSE1_P

V2_5SENSE1_M

V2_5SENSE2_P

V2_5SENSE2_M

1929_VOS_P

1929_VOS_M

PLACE CAPS CLSOE TO HIGH-SIDE FETS

ROUTE AS DIFF PAIR

ORIGINATING NEAR DIMMS

PLACE BETWEEN VR PINS 2,3

PLACE BETWEEN VR PINS 13, 14

PLACE C1124 BETWEEN VR PINS 20, 21

SMALL SIGNAL GROUND

NOTE
FOR E7501 A0 STEPPING, R423=16.2K
FOR E7501 A1 STEPPING, R423=17.4K

DRAWING

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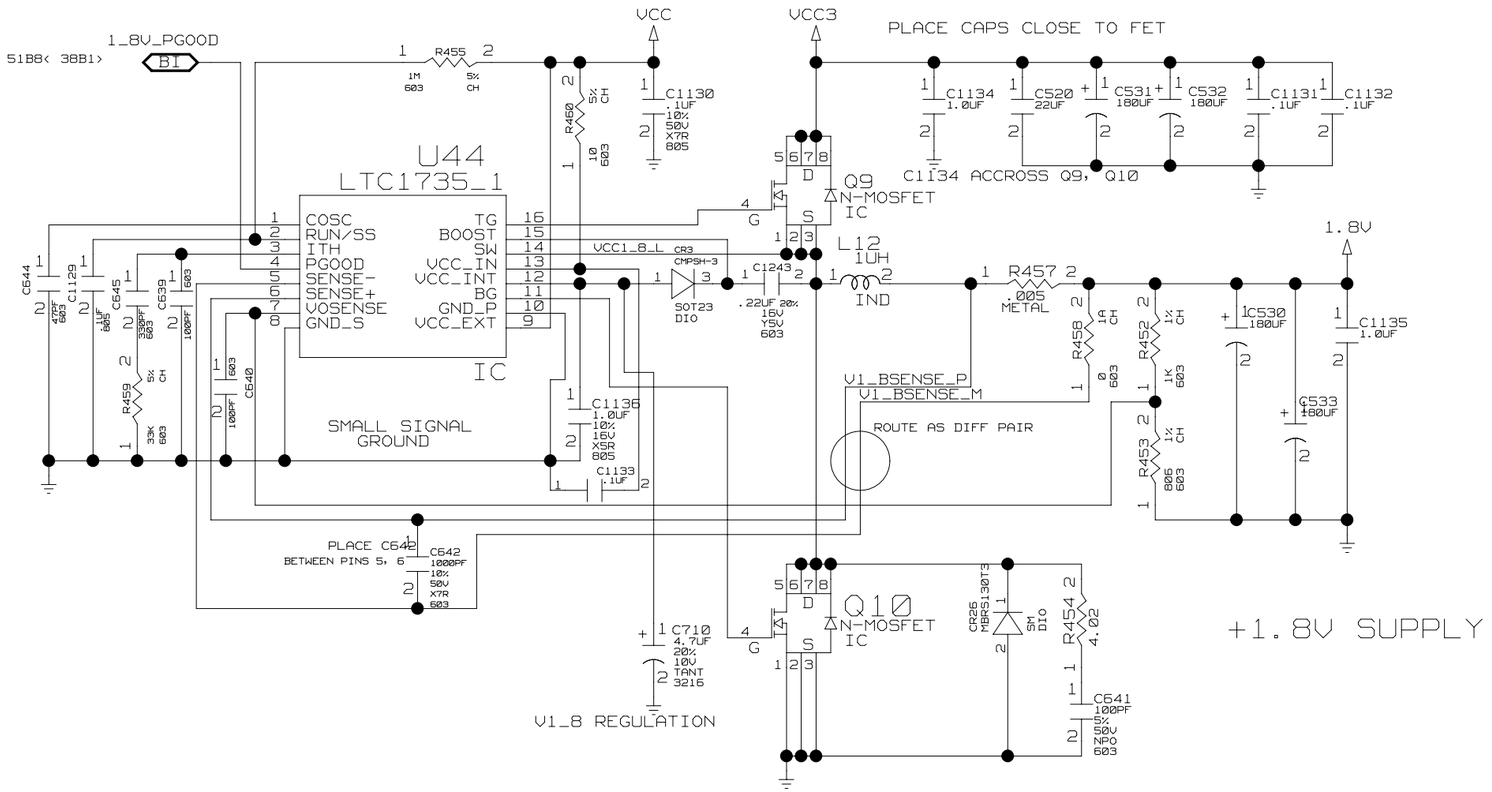
1_8V_PGOOD
51B8< 38B1>
BI
R455 1M 603 5% CH
VCC
VCC3
PLACE CAPS CLOSE TO FET
C1130 .1UF 10% 50V X7R 805
R460 5% CH 10 603
C1134 1.0UF
C520 22UF
C531 180UF
C532 180UF
C1131 .1UF
C1132 .1UF
C1134 ACCROSS Q9, Q10
U44
LTC1735_1
COSC
RUN/SS
ITH
PGOOD
SENSE-
SENSE+
VOSENSE
GND_S
TG
BOOST
SW
VCC_IN
VCC_INT
BG
GND_P
VCC_EXT
IC
Q9
N-MOSFET
IC
VCC1_8_L
CR3 CMPSH-3 SOT23 DIO
C1243 .22UF 20% 16V Y5V 603
L12 1UH IND
R457 .005 METAL
1.8V
R458 1A CH 0 603
R452 1% CH 1K 603
R453 1% CH 1K 603 805
C1530 180UF
C533 180UF
C1135 1.0UF
V1_BSENSE_P
V1_BSENSE_M
ROUTE AS DIFF PAIR
C544 470PF 603
C1129 1UF 805
C545 330PF 603
C639 100PF 603
R459 5% CH 33K 603
C640 100PF 603
SMALL SIGNAL GROUND
C1136 1.0UF 10% 16V X5R 805
C1133 .1UF
PLACE C642 BETWEEN PINS 5, 6
C642 1000PF 10% 50V X7R 603
C710 4.7UF 20% 10V TANT 3216
V1_8 REGULATION
Q10
N-MOSFET
IC
CR26 MBRS130T3 SM DIO
R454 4.02
C641 100PF 5% 50V NPO 603
+1.8V SUPPLY
VSBY5_0
VSBY1_8
LT1761_1_8
LT1761
IN
SHDN*
GND
OUT
BYP
U18
IC
C882 1.0UF 10% 16V X5R 805
C638 .01UF 20% 50V X7R 603
C709 10UF 20% 16V TANT 3528
VSBY1_8 REGULATION
VSBY1_8
VSBY5_0
VSBY3_3
VSBY3_3
U59
LTC1326
VCC3
VCC
VCCA
PBR*
GND
RST
RST*
SRST*
IC
R529 1% CH 6.04K 603
R530 5% CH 10K 603
R546 10K 603
R1016 5% CH 20K 603
ICH3_RSMRST_N
OUT 41C6<
STANDBY SUPPLY MONITOR
70C2> BI PWROK_RST_N
S9 SW
R648 1A CH 0 603
RESET_BTN
C1137 1.0UF 10% 16V X5R 805
VCC3
CR9 GREEN LED
R1047 1K 5% CH 603
R531 10K 5% CH 603
R224 5% CH 330 603
SOT23C BAV70LT1
CR72
49A4< 70B7> IN PS_PWRGD_SYS
PWROK_0
U72 74LVC14 IC VCC3=14 GND=7
47B6> IN 2_5V_PGOOD R771 0 603 0 CH
47D5> IN VTT_DDR_PGOOD R768 0 603 0 CH
R770 0 603 0 CH
4C2< 9C4> IN ITP_DBRST_N R976 0 603 0 CH
68B6> IN VCCP_PGOOD R143 0 603 1A CH
SYS_PWROK_1
SYS_PWROK_2
OUT
10A6< 55B6<
41C6< 25B5< 29B5<
PWROK GENERATION
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POWER CONNECTORS

VRD ENABLE LOGIC

J100 CONN24_WTX_MAIN
J101 CONN22_WTX
J102 CONN8_WTX_DIG
U16 QS3384
U17 QS3384
U113 74ACT04
U82 74LVC08AD
U57 74LVC00A
Q48 MMBT3904 XSTR
Q60 MBT3904DUAL XSTR
J4 2X3HDR HDR
J6 2X3HDR HDR
J28 1X2HDR HDR
RP1 100
RP2 100

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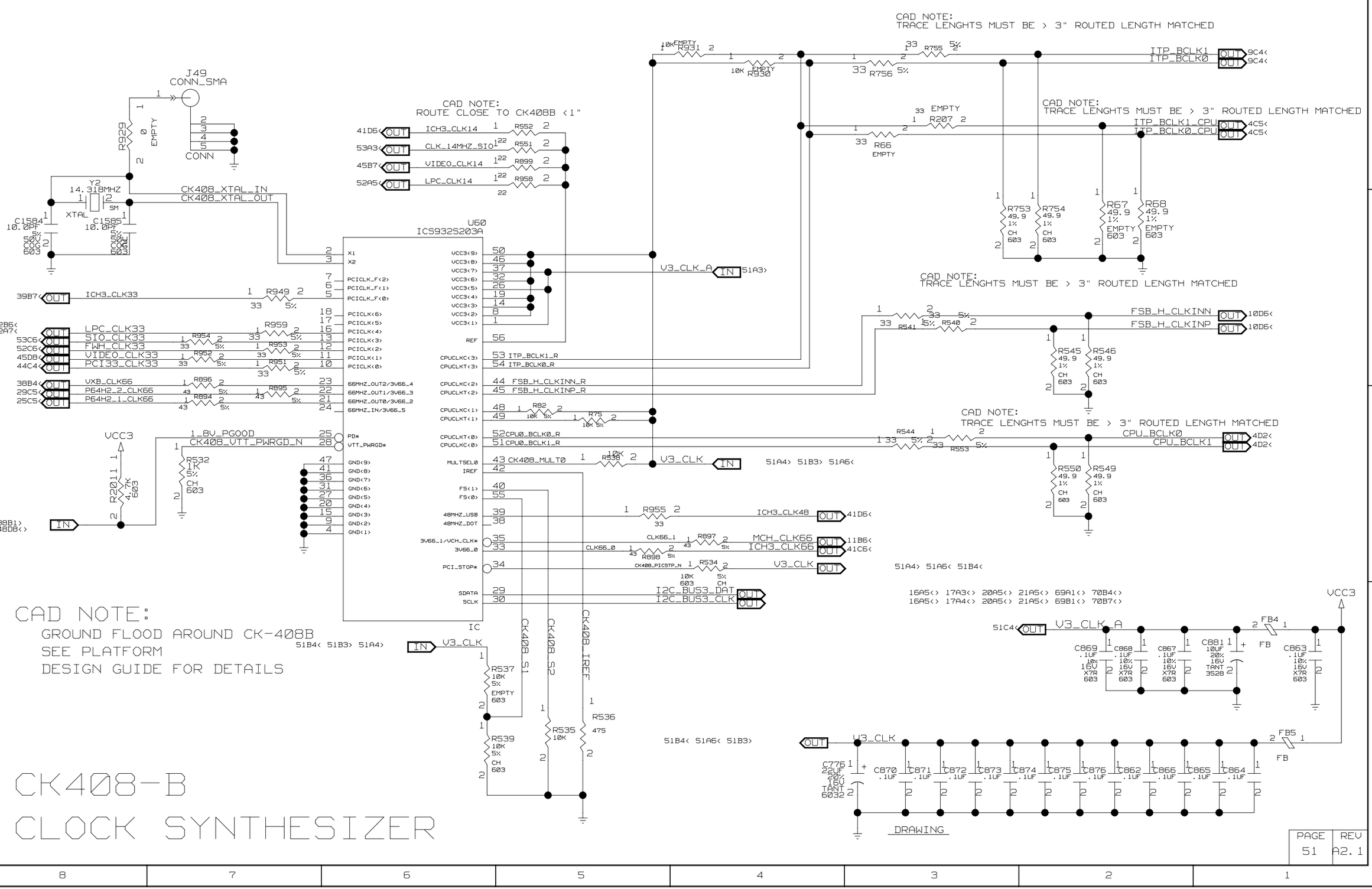

CAD NOTE:
GROUND FLOOD AROUND CK-408B
SEE PLATFORM
DESIGN GUIDE FOR DETAILS

FWH CIRCUITRY

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WP JUMPER SETTING

1 - 2	BIOS WRITE PROTECT
3 - 4	LOCK ENABLE
NO JUMPER	WRITE ENABLE

N/C TSOP ONLY
1, 3, 4, 5, 6, 8, 13, 14

DECOUPLING

U69
FWH_8M
IC

J27
1X4HDR
HDR

J50
2X30RCPT
CONN
NC=61, 62

Q33
MBT3904DUAL
XSTR

SIO CIRCUITRY

U56
LPC47B27

DEPOPULATE IF USING LPC CONNECTOR FOR DEBUG

R1053 8.2K 1% CH 603

R932 8.2K

DEFAULT I/O ADDRESS IS 2E

R499 4.7K 603 5% CH

R933 8.2K 1%

R497 1K 603 5% CH

R963 0

R757 GP30 4.7K 5%

R758 GP31 4.7K 603 5% CH

C712 2.2UF 20% 6V TANT 3216

C885 .1UF 10% 16V X7R 603

C886 .1UF 10% 16V X7R 603

C887 .1UF 10% 16V X7R 603

C888 .1UF 10% 16V X7R 603

C889 .01UF 20% 50V X7R 603

C883 .1UF 10% 16V X7R 603

C884 .1UF 10% 16V X7R 603

VCC3=53,65,93
VSS=7,31,60,76

IC

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LEGACY I/O

MOUSE & KEYBOARD

VCC
RT5 THRMSTR 1.10
V5_KB_RT
FB18 FB
V5_KB
C1450 .01UF 10% 50V X7R 603
C1449 1000PF 10% 50V X7R 603
RP283 2.7K 5% .063W
KBDATA
KBCLK
MSDATA
MSCLK
FB17
CON_KBDATA
CON_KBCLK
CON_MSDATA
CON_MSCLK
C1448 C1451 C1452 C1453 470PF 5% 50V COG 603

J40
PS2 STACK
P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15 P16 P17
CONN

PARALLEL PORT

CR45 MMBD914LT1 SOT23 DIO
LPT_V5_0
RP211 RP208 RP212 RP206 2.7K 5% .063W IC SM
R560 2.7K 5% CH 603

LPT_STROBE_N
LPT_ALF_N
LPT_PD0
LPT_PD1
LPT_INIT_N
LPT_PD2
LPT_SLCTIN_N
LPT_PD3
LPT_ERROR_N
LPT_PD4
LPT_PD5
LPT_PD6
LPT_PD7
LPT_ACK_N
LPT_BUSY
LPT_PE
LPT_SLCT
RP209 RP210 RP207 33 5%
LPT_STROBE_N_R
LPT_ALF_N_R
LPT_PD0_R
LPT_PD1_R
LPT_INIT_N_R
LPT_PD2_R
LPT_SELECTIN_R
LPT_PD3_R
LPT_PD4_R
LPT_PD5_R
LPT_PD6_R
LTP_PD7_R
C1246 C1245 C1260 C1244 C1257 C1247 C1258 C1259 C1253 C1251 C1254 C1250 C1255 C1249 C1256 C1248 C1252 180PF

J31
TALL DSUB 25
I47
27

SERIAL PORT

J35
2 ROW
DSUB

+12VPC
U61
GD75232S
VDD+ RA1 RA2 RA3 RA4 RA5 DY1 DY2 DY3 VDD-
RY1 RY2 RY3 RY4 RY5 DA1 DA2 DA3 VDD-
SER_DCD SER_DSR SER_RXD SER_CTS SER_RI SER_RTS SER_TXD SER_DTR
COM_DCD1_N COM_DSR1_N COM_RXD1 COM_CTS1_N COM_RI1_N COM_RTS1_N COM_TXD1 COM_DTR1_N
IC
VCC=20
GND=11
-12VPC
C1265 C1267 C1263 C1261 C1266 C1268 C1264 C1262 220PF

FLOPPY CONNECTOR

J34
2X17HDR_5
HDR
DRVEN0 DRVEN1 INDEX_N MTR0_N DS0_N DIR_N STEP_N WDATA_N WGATE_N TRK0_N WRTPRT_N RDATA_N HDSEL_N DSKCHG_N
RP205 1K 5%
R559 1K 603 5% CH

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V1.2 REGULATION

NOTE: ROUTE AS DIFFERENTIAL PAIR

1_2_PGOOD — OUT 47BB

VCC

C1548 .1UF 20% 50V X7R 805

R813 1M 5% CH 603

R817 10

U115 LTC1735_1 IC

1	COSC	TG	16
2	RUN/SS	BOOST	15
3	ITH	SW	14
4	PGOOD	VCC_IN	13
5	SENSE-	VCC_INT	12
6	SENSE+	BG	11
7	VOSENSE	GND_P	10
8	GND_S	VCC_EXT	9

C1561 47PF 5% 50V NPO 603

C1549 .1UF 20% 50V X7R 805

C1563 330PF 10% 50V X7R 603

R816 33K 5% CH 603

C1559 100PF 5% 50V NPO 603

C1562 100PF 5% 50V NPO 603

SMALL SIGNAL GROUND

C1547 1.0UF

C1566 4.7UF 20% 10V TANT 3216

C1552 .1UF

PLACE C1550 BETWEEN PINS 5, 6

C1560 100PF 10% 50V X7R 603

PLACE C1547 CLOSE TO PINS 10, 12

CR78 CMPSH-3 SOT23 DIO

C1564 .22UF 20% 16V X5R 603

Q49 N-MOSFET IC

PLACE CAPS CLOSE TO FET

C1546 22UF 20% 6.3V X5R 1210

C1555 180UF 20% 4V ALUM 7343

C1556 180UF 20% 4V ALUM 7343

C1553 .1UF 20% 50V X7R 805

C1550 1UF 20% 50V X7R 805

C1551 1.0UF 10% 16V X5R 805

L22 1UH IND

R8142 .01 2010 1% CH

R815 0

R818 402 1% CH 603

R819 806 1% CH 603

C1558 180UF 20% 4V ALUM 7343

C1557 180UF 20% 4V ALUM 7343

C1554 1.0UF 10% 16V X5R 805

VCC1_2

V1_2SENSE_P

V1_2SENSE_N

VCC1_2_L

R797 4.7 EMPTY

C1565 100PF 5% 50V NPO 603

Q50 N-MOSFET IC

CR79 MBRS130T3 DIO

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INTEL(R) 82544EI GIGABIT LAN CONTROLLER

LAN CONTROLLER
P64H2 #1, PCI BUS B
IDSEL = AD17
REQ#/GNT# = 0
IRQ#0

24D6<> 31A3<> 34A2<> 34A7<> 56D7<>

U79
82544EI

PCI ADD/DATA/CTL

P64H2_1_PB_AD<63..0> BI

63 AF21 AD<63>
62 AD21 AD<62>
61 AC21 AD<61>
60 AC22 AD<60>
59 AD23 AD<59>
58 AC24 AD<58>
57 AC25 AD<57>
56 AB23 AD<56>
55 AB24 AD<55>
54 AB26 AD<54>
53 AA23 AD<53>
52 AA25 AD<52>
51 AA26 AD<51>
50 Y23 AD<50>
49 Y24 AD<49>
48 Y26 AD<48>
47 W23 AD<47>
46 W25 AD<46>
45 W26 AD<45>
44 V24 AD<44>
43 V26 AD<43>
42 U23 AD<42>
41 U25 AD<41>
40 U26 AD<40>
39 T23 AD<39>
38 T24 AD<38>
37 T26 AD<37>
36 R23 AD<36>
35 R25 AD<35>
34 R26 AD<34>
33 P23 AD<33>
32 P24 AD<32>
31 AB4 AD<31>
30 AB1 AD<30>
29 AC3 AD<29>
28 AB3 AD<28>
27 AC2 AD<27>
26 AE4 AD<26>
25 AC1 AD<25>
24 AF4 AD<24>
23 AD5 AD<23>
22 AF6 AD<22>
21 AC6 AD<21>
20 AE6 AD<20>
19 AF7 AD<19>
18 AD7 AD<18>
17 AC7 AD<17>
16 AF8 AD<16>
15 AC12 AD<15>
14 AE12 AD<14>
13 AF13 AD<13>
12 AC13 AD<12>
11 AD13 AD<11>
10 AF14 AD<10>
9 AE14 AD<9>
8 AC14 AD<8>
7 AD15 AD<7>
6 AC15 AD<6>
5 AF16 AD<5>
4 AE16 AD<4>
3 AC16 AD<3>
2 AF17 AD<2>
1 AD17 AD<1>
0 AF18 AD<0>

CBE#<7> AC19 P64H2_1_PB_CBE7_N BI 24C4<> 31D4<>
CBE#<6> AF20 P64H2_1_PB_CBE6_N BI 34B4<> 34B7<>
CBE#<5> AE20 P64H2_1_PB_CBE5_N BI 24C4<> 31B2<>
CBE#<4> AC20 P64H2_1_PB_CBE4_N BI 34B4<> 34A7<>
CBE#<3> AF5 P64H2_1_PB_CBE3_N BI 24B4<> 34C3<>
CBE#<2> AE8 P64H2_1_PB_CBE2_N BI 24B4<> 34C3<>
CBE#<1> AF12 P64H2_1_PB_CBE1_N BI 24B4<> 34B3<>
CBE#<0> AF15 P64H2_1_PB_CBE0_N BI 24B4<> 34B7<>

PAR AC11 P64H2_1_PB_PAR BI 24C4<> 34B7<>
PAR64 AD19 P64H2_1_PB_PAR64 BI 34B4<>
FRAME# AC8 P64H2_1_PB_FRAME_N BI 24C4<> 31C2<>
IRDY# AF9 P64H2_1_PB_IRDY_N BI 34C4<> 34C7<>
TRDY# AD9 P64H2_1_PB_TRDY_N BI 24C4<> 31B2<>
STOP# AE10 P64H2_1_PB_STOP_N BI 24C4<> 31B2<>
IDSEL AC5 LAN_IDSEL 34C7<>
DEVSEL# AF10 P64H2_1_PB_DEVSEL_N BI 24C4<> 34C3<>
VIO<2> AF24 44A2>
VIO<1> AF3

REQ64# AF19 P64H2_1_PB_REQ64_N BI 31D4<> 34B7<>
ACK64# AC18 P64H2_1_PB_ACK64_N BI 24B4<> 31B2<>
REQ# AA1 P64H2_1_PB_REQ0_N BI 31A4<> 24C4<> 34B3<>
GNT# AA4 P64H2_1_PB_GNT0_N IN 24C4>
LOCK# AC10 P64H2_1_PB_PLOCK_N IN

CLK Y3 P64H2_1_PB_PCLK0 IN 24B2>
M66EN AE18 P64H2_1_PB_M66EN IN
RST# Y1

LAN_PWR_GOOD B21 SYS_PWR0K_1 IN 48B1> 10A6<
PME# AA2 PME_N
APM_WAKEUP P25
AUX_PWR Y4 AUX_PWR
PWR_STATE1 V1
PWR_STATE0 V4

INTA# W2 P64H2_1_PB_IRQ0 BI 31C6<> 24A4<

1 OF 4
IC

P64H2_1_PB_LAN_RST_N

R900 2 1K 5% CH 603 1
R934 2 10K 5% 1/16W 603 1
VCC3

JP14
1X2HDR
1 2 P64H2_1_PB_RST_N IN 24B4> 34D7<
HDR

R226 10K 5% CH 603 1 2

1-2 - NORMAL OPERATION
NO JMPR - HOLD IN RESET

P64H2_1_PB_AD<17> BI

R759 2 100 5% CH 603 1
R653 2 10K 5% CH 603 1

VCC3

U101
AT93C46A_66

8 VCC
3 DI
1 CS
2 SK
5 GND
NC=6,7
DO 4

C1599 .01UF 5% 50V X7R 603 1 2

R936 2 1K 1% 1/16W 603 1

IC

EE_DI D25
EE_DO D24
EE_CS D23
EE_SK E24

U79
82544EI

EE_D1
EE_D0
EE_CS
EE_SK

EEPROM/FLASH INTJTAG

F26 FL_ADD<18>
D26 FL_ADD<17>
H26 FL_ADD<16>
E26 FL_ADD<15>
F25 FL_ADD<14>
G25 FL_ADD<13>
F24 FL_ADD<12>
G23 FL_ADD<11>
L26 FL_ADD<10>
G26 FL_ADD<9>
J26 FL_ADD<8>
H24 FL_ADD<7>
J23 FL_ADD<6>
H25 FL_ADD<5>
J24 FL_ADD<4>
K25 FL_ADD<3>
K24 FL_ADD<2>
K26 FL_ADD<1>
M25 FL_ADD<0>
L23 FL_CS*
H23 FL_OE*
F23 FL_WE*

L25 FL_DATA<7>
M26 FL_DATA<6>
N24 FL_DATA<5>
M24 FL_DATA<4>
P26 FL_DATA<3>
N23 FL_DATA<2>
N26 FL_DATA<1>
M23 FL_DATA<0>

R939 2 680 1

A14 LOX
C23 XOFF
A23 XON
C22 ABV_HI
D21 BLW_LO

MISC.

K1 SDP7
K2 SDP6
K3 SDP4
K4 SDP3
J3 SDP2
J1 SDP1
G2 SDP0

R935 1 330 2
CR81 YELLOW LED

56B2< BI 82544EI_TEST A13 TEST
L3 GMII_TEST1
L2 GMII_TEST0
B8 COL_TEST
C8 CRS_TEST

SERR# AD11 P64H2_1_PB_SERR_N BI
PERR# AF11 P64H2_1_PB_PERR_N BI

44A2>
34B3<>
34C4<>
24C4<>
31A2<>

ZN_COMP W1 ZN_COMP
ZP_COMP W4 ZP_COMP

R660 2 24.9 1% 1

TBI_MODE A21 TBI_MODE
TX_DATA<9> A7
TX_DATA<8> D8
TX_DATA<7> D7
TX_DATA<6> A6
TX_DATA<5> B6
TX_DATA<4> D6
TX_DATA<3> A5
TX_DATA<2> C5
TX_DATA<1> D5
TX_DATA<0> A4
GTX_CLK C7 82544EI_TEST
EWRAP D13

TBI INT

RX_DATA<9> D12
RX_DATA<8> C12
RX_DATA<7> B11
RX_DATA<6> C11
RX_DATA<5> A10
RX_DATA<4> D10
RX_DATA<3> A9
RX_DATA<2> B9
RX_DATA<1> D9
RX_DATA<0> A8
RBC0 B13
RBC1 A12

R664 2 24.9 1% 1
R938 2 1% 1
RP27 5% 2
1 8
2 7
3 6
4 5
680 5% SM .063W

56A4< BI

Y3 25.000MHZ
SM
1XTAL
C1271 22PF 5% 50V NP0 603 2
C1270 22PF 5% 50V NP0 603 2

LINK_UP* P3 LINK_UP_N OUT 58C3<
RX_ACTIVITY* P1
TX_ACTIVITY* R4 LINK_ACT_N OUT 58C3<
LINK10* R3
LINK100* R2 LINK100_N OUT 58B3<
LINK1000* R1 LINK1000_N OUT 58B3<

LED

XTAL1 B4 XTAL1
XTAL2 C4 XTAL2
REF E3
R658 2 2.49K 1% 1

MDI_0- C1 MDIO_N BI 58B8<>
MDI_0+ C2 MDIO BI 58B8<>
MDI_1- D1 MDI1_N BI 58B8<>
MDI_1+ D2 MDI1 BI 58B8<>
MDI_2- E1 MDI2_N BI 58B8<>
MDI_2+ E2 MDI2 BI 58B8<>
MDI_3- F1 MDI3_N BI 58B8<>
MDI_3+ F2 MDI3 BI 58B8<>

PHY

TCK T3 JTAG_TCK
TDI U4
TDO U2
TMS U1 JTAG_TMS
TRST* T1

R937 2 1K 1
R659 1K 1
R652 2 1K 1

JTAG

2 OF 4
IC

VCC3

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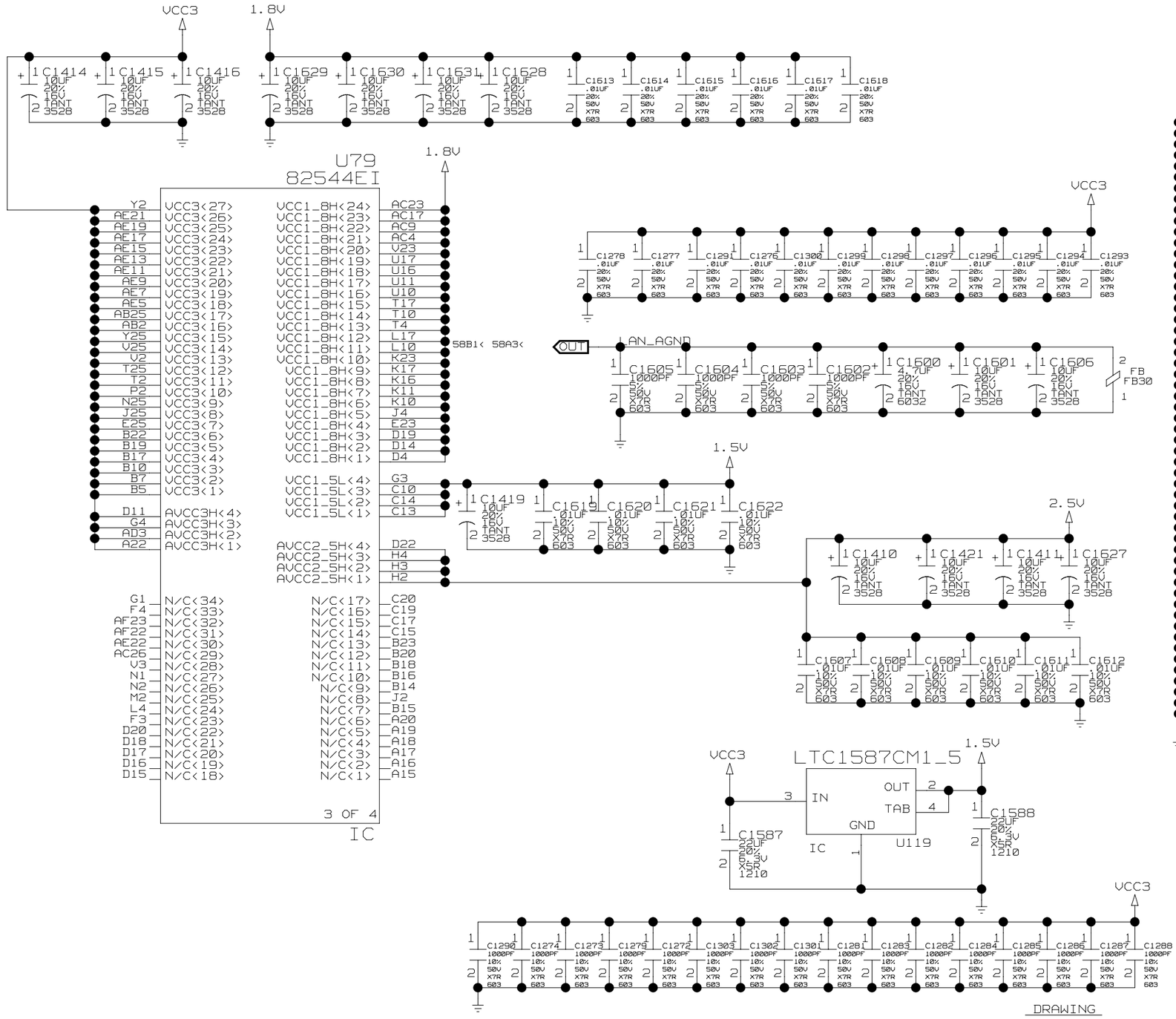
GIGABIT LAN CONTROLLER



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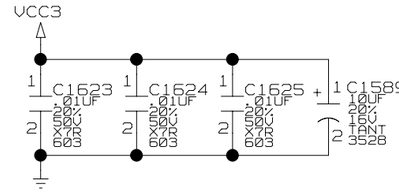

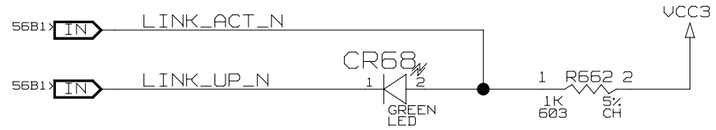

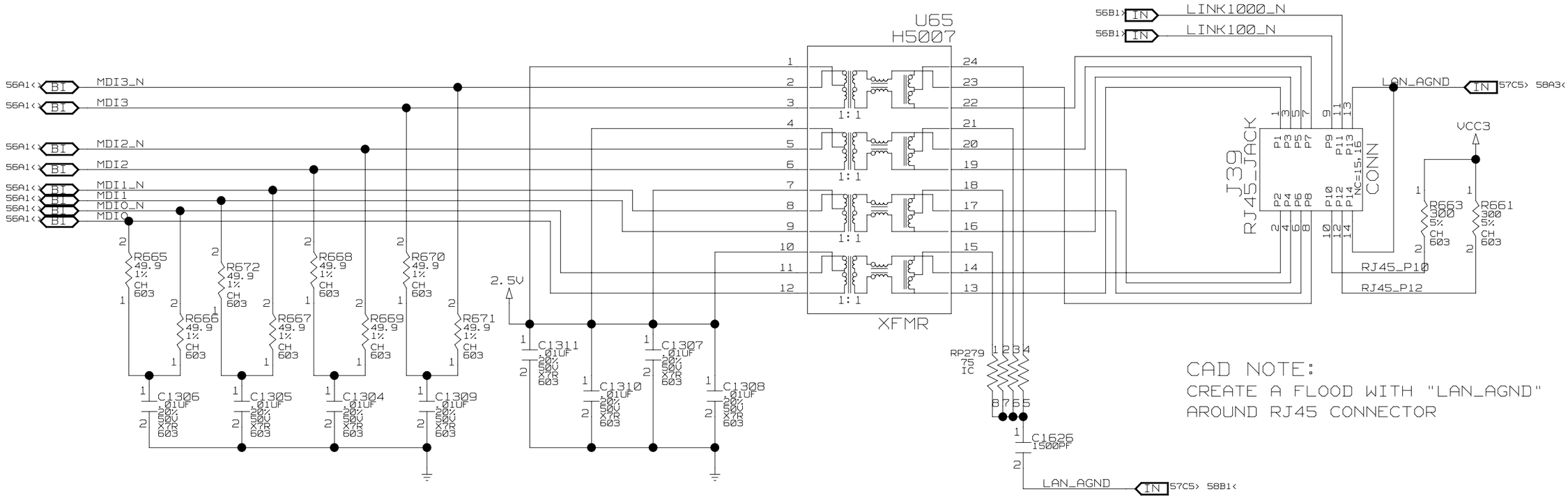

LAN MAGNETICS AND CONNECTOR

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SCSI CONTROLLER

U78
AIC_7902A

R673 1 2 0
32A6<> 27D6<> 59A7<>
OUT P64H2_2_PA_AD<17>
R679 1 2 100
27B2> IN P64H2_2_PA_PCLK0 T1 PCLK
R3 TRST*
27C4> IN P64H2_2_PA_GNT0_N AE1 GNT*
SCSI_IDESL AE4 IDSEL
R676 1 2 0
R674 1 2 0
R675 1 2 0
T4 TCK
U4 TMS
P4 TDI

AD<63:0>
63 AC17 AD<63>
62 AD17 AD<62>
61 AE17 AD<61>
60 AF17 AD<60>
59 AC18 AD<59>
58 AD18 AD<58>
57 AE18 AD<57>
56 AC19 AD<56>
55 AD19 AD<55>
54 AE19 AD<54>
53 AC20 AD<53>
52 AD20 AD<52>
51 AE20 AD<51>
50 AF20 AD<50>
49 AC21 AD<49>
48 AD21 AD<48>
47 AE21 AD<47>
46 AC22 AD<46>
45 AD22 AD<45>
44 AE22 AD<44>
43 AD23 AD<43>
42 AE23 AD<42>
41 AF23 AD<41>
40 AD24 AD<40>
39 AF24 AD<39>
38 AE24 AD<38>
37 AF26 AD<37>
36 AF25 AD<36>
35 AE26 AD<35>
34 AE25 AD<34>
33 AD26 AD<33>
32 AD25 AD<32>
31 AC2 AD<31>
30 AD2 AD<30>
29 AE2 AD<29>
28 AC3 AD<28>
27 AD3 AD<27>
26 AE3 AD<26>
25 AF3 AD<25>
24 AC4 AD<24>
23 AF4 AD<23>
22 AC5 AD<22>
21 AD5 AD<21>
20 AE5 AD<20>
19 AF5 AD<19>
18 AC6 AD<18>
17 AD6 AD<17>
16 AE6 AD<16>
15 AC10 AD<15>
14 AD10 AD<14>
13 AE10 AD<13>
12 AC11 AD<12>
11 AD11 AD<11>
10 AE11 AD<10>
9 AF11 AD<9>
8 AC12 AD<8>
7 AE12 AD<7>
6 AC13 AD<6>
5 AD13 AD<5>
4 AE13 AD<4>
3 AF13 AD<3>
2 AC14 AD<2>
1 AD14 AD<1>
0 AE14 AD<0>

59D8> 32A6<> 27D6<> BI P64H2_2_PA_AD<63:0>

P2 RSVD1
R2 RSVD2
V4 RSVD3
U3 TEST10

SAME AS AIC7902

1 OF 6

IC

INTA* AB3 P64H2_2_PA_IRQ0 OUT 32A2<> 27A4<
INTB* AB2 P64H2_2_PA_IRQ1 OUT 32B6<> 27A4<
PREQ* AF1 P64H2_2_PA_REQ0_N OUT 32A6<> 27C4<
TDO R4
ACK64* AC15 P64H2_2_PA_ACK64_N BI 32A6<> 27D4<
REQ64* AD15 P64H2_2_PA_REQ64_N BI 27D4<> 32C8<>
PAR64 AF16 P64H2_2_PA_PAR64 BI 27C4<> 32C8<>
FRAME* AD7 P64H2_2_PA_FRAME_N BI 27C4<> 32B6<>
IRDY* AE7 P64H2_2_PA_IRDY_N BI 27C4<> 32D8<>
PAR AD9 P64H2_2_PA_PAR BI 27C4<>
DEVSEL* AD8 P64H2_2_PA_DEVSEL_N BI 27C4<> 32B6<>
TRDY* AC8 P64H2_2_PA_TRDY_N BI 27C4<> 32B6<>
STOP* AE8 P64H2_2_PA_STOP_N BI 27C4<> 32D8<>
PERR* AF8 P64H2_2_PA_PERR_N BI 27C4<> 32D8<>
SERR* AC9 P64H2_2_PA_SERR_N BI 32B6<> 27C4<

CBE*<7> AE15 P64H2_2_PA_CBE7_N BI 27C4<> 32C8<>
CBE*<6> AC16 P64H2_2_PA_CBE6_N BI 27C4<> 32B6<>
CBE*<5> AD16 P64H2_2_PA_CBE5_N BI 27C4<> 32B6<>
CBE*<4> AE16 P64H2_2_PA_CBE4_N BI 27B4<> 32B6<>
CBE*<3> AD4 P64H2_2_PA_CBE3_N BI 27B4<>
CBE*<2> AC7 P64H2_2_PA_CBE2_N BI 27B4<>
CBE*<1> AE9 P64H2_2_PA_CBE1_N BI 27B4<>
CBE*<0> AD12 P64H2_2_PA_CBE0_N BI 27B4<>

ROMOE* P24
SEECS AC26 SCSI_SEECS
MWE* T23
ROMCS* N23
BRDWE AB24
BRDOE* AB23

1K R677 EMPTY 1 2

MA<18> N24
MA<17> N25
MA<16> T24
MA<15> T25
MA<14> R25
MA<13> R24
MA<12> T26
MA<11> P25
MA<10> P23
MA<9> P26
MA<8> R23
MA<7> U23
MA<6> U24
MA<5> U25
MA<4> U26
MA<3> V23
MA<2> V24
MA<1> V25
MA<0> W23

MD<7> AA23
MD<6> Y26
MD<5> Y25
MD<4> Y24
MD<3> Y23
MD<2> W26
MD<1> W25
MD<0> W24

SEECK AC25 SCSI_SEECK
SEEDO AC24 SCSI_SEEDO
SEEDI AC23 SCSI_SEEDI

RSVD4 W4
TEST2 Y4 AIC7902_TEST2 BI 62A8<>
RSVD8 AA24
RSVD7 AA25
RSVD6 AB26
RSVD5 AB25

3.3 VOLT PART ONLY

VCC3

U64
AT93C66
4 CS
3 SK
2 DI
1 DO
8 VCC
5 GND
6 ORG
NC=7
IC

R678 1 2 2.7K 603 5% CH
C1312 .01UF 2 1

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SCSI CONTROLLER

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AIC_7902A

SCSI

2 OF 6
IC

3 OF 6
IC

1-2 = NORMAL OPERATION
NO JMPR = HOLD IN RESET

DRAWING

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SCSI CONTROLLER

U78
AIC_7902A

IN SCSI_CORE_VCC

C1426 10UF 20% 16V TANT 3528
C1317 .01UF

AF21	VCC1_8<20>	GND<72>	AB22
AF18	VCC1_8<19>	GND<71>	AB21
AF15	VCC1_8<18>	GND<70>	AB18
AF12	VCC1_8<17>	GND<69>	AB17
AF9	VCC1_8<16>	GND<68>	AB14
AF6	VCC1_8<15>	GND<67>	AB13
AA26	VCC1_8<14>	GND<66>	AB10
AA1	VCC1_8<13>	GND<65>	AB9
W1	VCC1_8<12>	GND<64>	AB6
V26	VCC1_8<11>	GND<63>	AB5
R26	VCC1_8<10>	GND<62>	AA22
R1	VCC1_8<9>	GND<61>	AA5
M1	VCC1_8<8>	GND<60>	V22
L26	VCC1_8<7>	GND<59>	V5
L1	VCC1_8<6>	GND<58>	U22
K25	VCC1_8<5>	GND<57>	U5
D14	VCC1_8<4>	GND<56>	T16
C17	VCC1_8<3>	GND<55>	T15
A14	VCC1_8<2>	GND<54>	T14
A7	VCC1_8<1>	GND<53>	T13
		GND<52>	T12
		GND<51>	T11
		GND<50>	R16
		GND<49>	R15
		GND<48>	R14
		GND<47>	R13
		GND<46>	R12
		GND<45>	R11
		GND<44>	P22
		GND<43>	P16
		GND<42>	P15
		GND<41>	P14
		GND<40>	P13
		GND<39>	P12
		GND<38>	P11
		GND<37>	P5
		GND<36>	N22
		GND<35>	N16
		GND<34>	N15
		GND<33>	N14
		GND<32>	N13
		GND<31>	N12
		GND<30>	N11
		GND<29>	N5
		GND<28>	M16
		GND<27>	M15
		GND<26>	M14
		GND<25>	M13
		GND<24>	M12
		GND<23>	M11
		GND<22>	L16
		GND<21>	L15
		GND<20>	L14
		GND<19>	L13
		GND<18>	L12
		GND<17>	L11
		GND<16>	K22
		GND<15>	K5
		GND<14>	J22
		GND<13>	J5
		GND<12>	F22
		GND<11>	F5
		GND<10>	E22
		GND<9>	E21
		GND<8>	E18
		GND<7>	E17
		GND<6>	E14
		GND<5>	E13
		GND<4>	E10
		GND<3>	E9
		GND<2>	E6
		GND<1>	E5

POWERS/GROUNDS

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IC

63B6 IN SCSI_VCC

C898 10UF 20% 16V X5R 1210
C1324 .1UF
C1321 .01UF 5% 50V X7R 603
C1323 .1UF
C1314 .01UF
C1424 10UF 20% 16V TANT 3528

C897 10UF 20% 16V X5R 1210
C1319 .1UF
C1322 .01UF 5% 50V X7R 603
C1320 .1UF
C1315 .01UF
C1423 10UF 20% 16V TANT 3528

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AIC_7902A

H22	SVCCA25<5>	M5	SVCCB25<5>
G22	SVCCA25<4>	L5	SVCCB25<4>
E20	SVCCA25<3>	H5	SVCCB25<3>
E19	SVCCA25<2>	G5	SVCCB25<2>
E16	SVCCA25<1>	E8	SVCCB25<1>
E15	SVCCA25<0>	E7	SVCCB25<0>

G26	SVCC1_8<3>	K1	SVCC33<5>
D4	SVCC1_8<2>	H26	SVCC33<4>
C23	SVCC1_8<1>	D23	SVCC33<3>
C3	SVCC1_8<0>	A16	SVCC33<2>
		A4	SVCC33<1>
		A1	SVCC33<0>

AF22	VCC3<16>
AF19	VCC3<15>
AF14	VCC3<14>
AF10	VCC3<13>
AF7	VCC3<12>
AF2	VCC3<11>
Y22	VCC3<10>
W22	VCC3<9>
T22	VCC3<8>
T5	VCC3<7>
R22	VCC3<6>
R5	VCC3<5>
M22	VCC3<4>
L22	VCC3<3>
E12	VCC3<2>
E11	VCC3<1>

POWERS/GROUNDS

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IC

C1316 .01UF
C1422 10UF 20% 16V TANT 3528
VCC3
C1425 10UF 20% 16V TANT 3528
C1313 .01UF
VCC3
C1427 10UF 20% 16V TANT 3528
C1318 .01UF

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SCSI CONTROLLER

U78
AIC_7902A

SCSI POWER/GND AND TEST

W2 PXAGND1
Y2 PXAGND2
V1 PCAGND1
V2 PCAGND2
AA3 PZGND
AB1 PAGUARDG
C14 AGND<5>
C13 AGND<4>
C12 AGND<3>
B14 AGND<2>
A13 AGND<1>
C11 AGND<0>
C10 STAGARDG
D10 SRAGARDG

63C4< 62C3> 62B3> OUT SCSI_AGND

PXVCC18 P1
PXAVCC18 Y1
PXAVCC331 U1
PXAVCC332 U2
PCAVCC331 T2
PCAVCC332 T3
PZV33 AA2
PAGUARDV AC1
VCC3

AVCC18<3> D7
AVCC18<2> C7
AVCC18<1> B7
AVCC18<0> A8

AVCC33<4> A10
AVCC33<3> A9
AVCC33<2> B8
AVCC33<1> A12
AVCC33<0> A11

STAGARDV C8
SRAGARDV D8

TERMPWRA H23 AIC7902_TERMPWRA
TERMPWRB D12 AIC7902_TERMPWRB

VIO<9> AB20
VIO<8> AB19
VIO<7> AB16
VIO<6> AB15
VIO<5> AB12
VIO<4> AB11
VIO<3> AB8
VIO<2> AB7
VIO<1> Y5
VIO<0> W5

62A8< BI AIC7902_TEST9 Y3 TEST9
W3 TEST8
V3 TEST7
D13 TEST6
D11 TEST5
G23 TEST4

TEST3 H24 AIC7902_TEST3 BI 62A8<>
TEST1 AA4 AIC7902_TEST1 BI 62A8<>
TEST0 AB4 AIC7902_TEST0 BI 62A8<>

5 OF 6
IC

SCSI_CORE_VCC IN 63B2> 61D8<

C1335 .01UF 5% 50V X7R 603
C1428 10UF 20% 16V TANT 3528

SCSI_CORE_VCCA_PX
FB6 FB
C1333 .01UF 5% 50V X7R 603
C1429 10UF 20% 16V TANT 3528
62C8> 62B3> 62C3> 63C4< OUT SCSI_AGND

SCSI_V3_3A_PX
FB9 FB
C1334 .01UF 5% 50V X7R 603
C1330 .01UF 5% 50V X7R 603
C1329 .01UF 5% 50V X7R 603
C1430 10UF 20% 16V TANT 3528
63C4< 62C8> 62B3> 62C3> OUT SCSI_AGND

SCSI_CORE_VCCA
FB10 FB
C1331 .01UF 5% 50V X7R 603
C1328 .01UF 5% 50V X7R 603
C1431 10UF 20% 16V TANT 3528
62C8> 62C3> 62B3> 63C4< OUT SCSI_AGND

SCSI_V3_3A_0
FB8 FB
C1332 .01UF 5% 50V X7R 603
C1327 .01UF 5% 50V X7R 603
C1432 10UF 20% 16V TANT 3528
62C8> 62B3> 62C3> 63C4< OUT SCSI_AGND

SCSI_V3_3A_1
FB7 FB
C1325 .01UF 5% 50V X7R 603
C1326 .01UF 5% 50V X7R 603
62C8> 62B3> 62C3> 63C4< OUT SCSI_AGND

VCC3

C1340 1000PF 10% 50V X7R 603
C1339 1000PF 10% 50V X7R 603

R688 1K 5% 1/16W LVTRMPWR_A IN 64C5> 65D5<
R689 1K LVTRMPWR_B IN 54C2> 56D5<

R1007 10K 603
R1008 10K 603
R1009 10K 603
R1010 10K 603
U71 1.24V DIO NC=1,2
U70 1.24V DIO NC=1,2

62B4< BI AIC7902_TEST3 R1011 4.7K 603 EMPTY

RP280 4.7K EMPTY
62B7< BI AIC7902_TEST9
59A3< BI AIC7902_TEST2
62B4< BI AIC7902_TEST1
62B4< BI AIC7902_TEST0

NOPOP RP280 AND R1011 FOR
AIC7902 A-2 AND LATER STEPPINGS

C1336 .01UF 5% 50V X7R 603
C1337 .01UF 5% 50V X7R 603
C1338 .01UF 5% 50V X7R 603
C1341 .1UF

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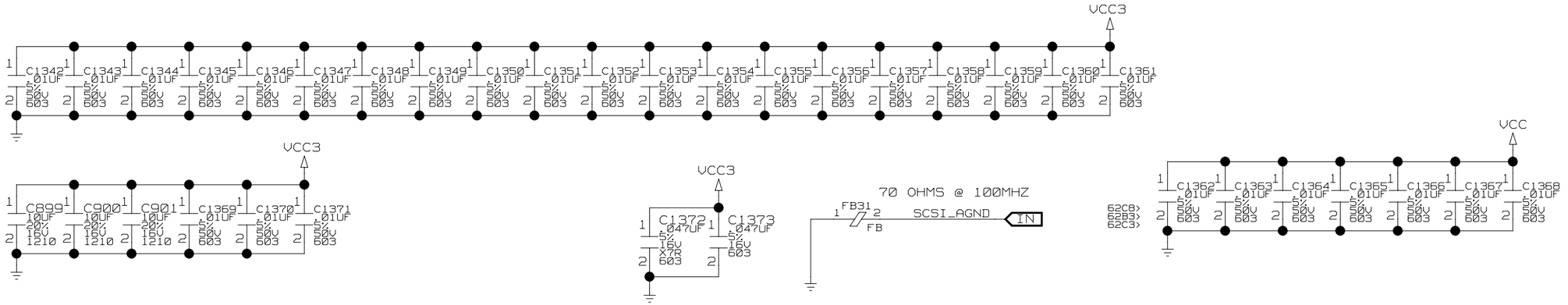
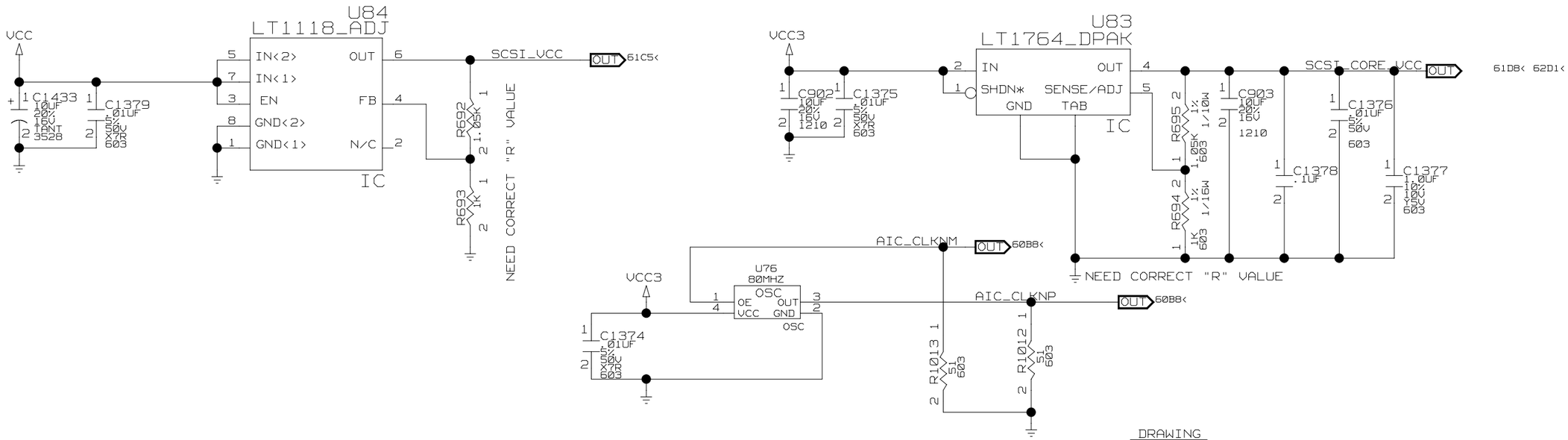
AIC - 7902 SCSI DECOUPLING RECOMMENDATION FOR POWER SUPPLIES



ISOLATE DIGITAL & ANALOG GROUND

VOLTAGE REGULATORS AND SCSI CLOCK



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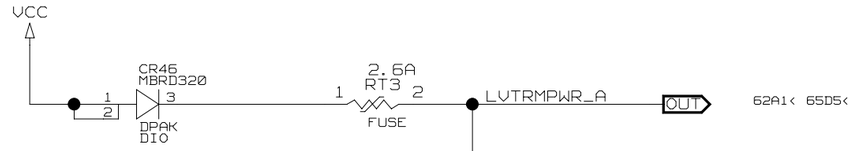
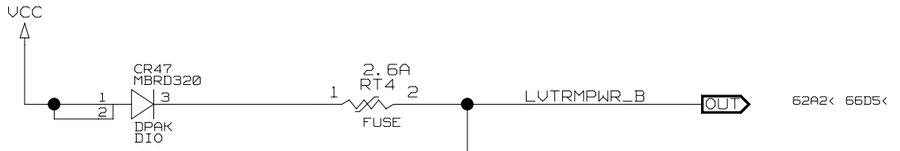
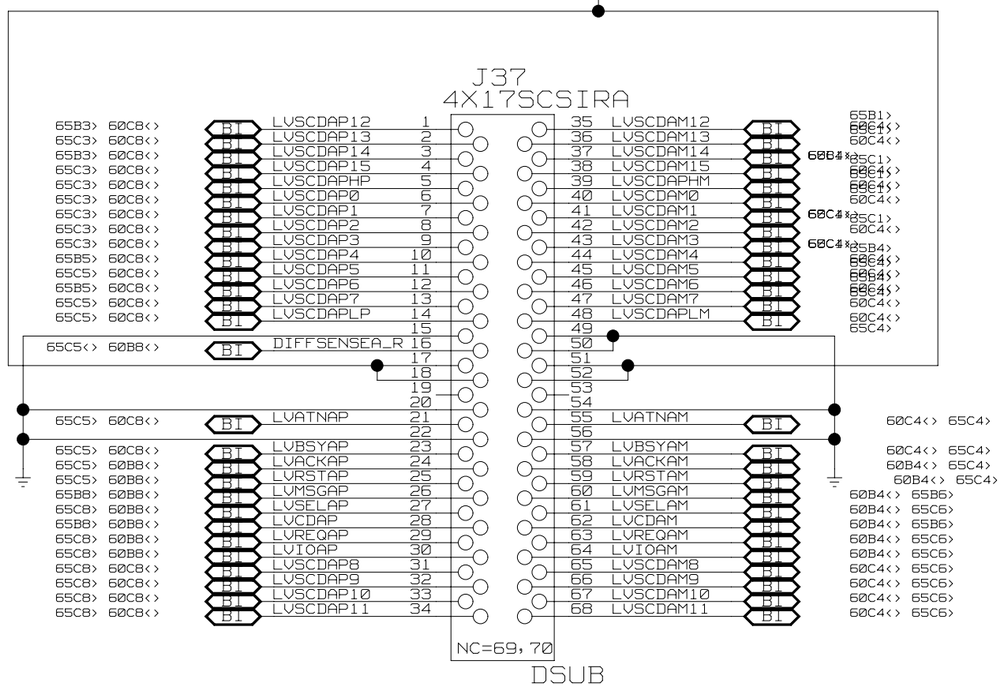
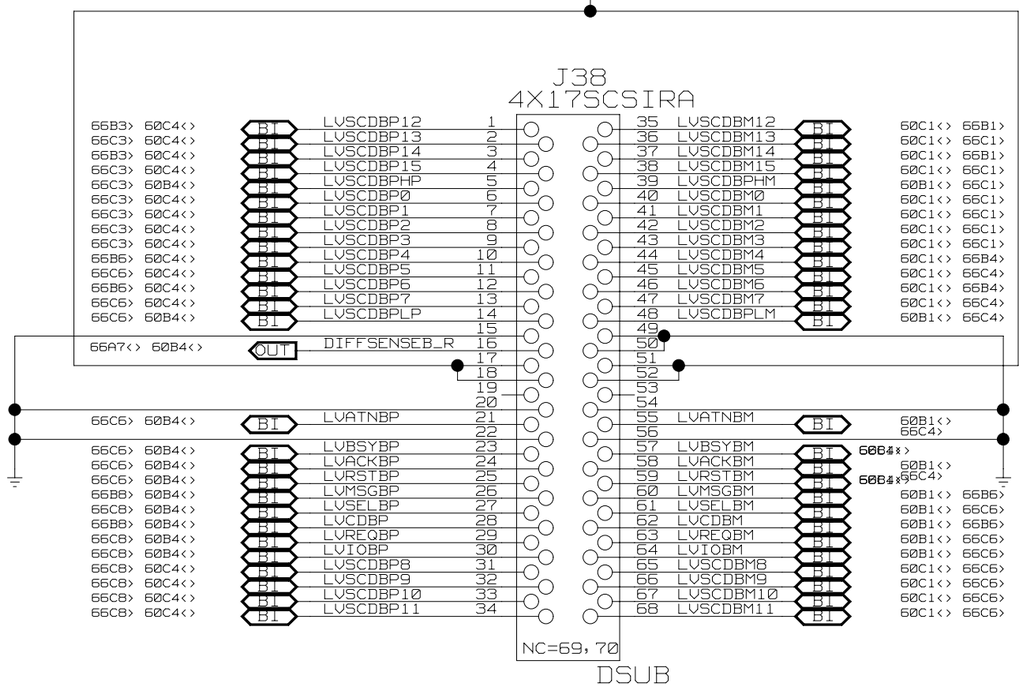
SCSI CONNECTORS A AND B









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TERMINATION SCSI CHANNEL A

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40 MIL

LVTRMPWR_A IN 64C5> 62A1<

C1380 .1UF

C1434 10UF 20% 16V TANT 3528

DIFFSENSEA_R BI 60B8<> 64B7<>

R697 4.7K 603 5% 1/16W

R702 20K

CHA_TERMEN 60B5> IN

R700 1K

U93 DS2119M

DIFFSENSE, TPWR1, TPWR2, DIFF_CAP, HS_GND, HS_GND, GND, ISO, MSTR/SLV, VREF, IC

RP<9> LVSELAP 25 — RN<9> 26 LVSELAM

RP<8> LVREQAP 23 — RN<8> 24 LVREQAM

RP<7> LVSCDAP8 20 — RN<7> 21 LVSCDAM8

RP<6> LVSCDAP10 18 — RN<6> 19 LVSCDAM10

RP<5> LVSCDAP11 11 — RN<5> 12 LVSCDAM11

RP<4> LVSCDAP9 9 — RN<4> 10 LVSCDAM9

RP<3> LVIOAP 7 — RN<3> 8 LVIOAM

RP<2> LVCDAP 4 — RN<2> 5 LVCDAM

RP<1> LVMSGAP 2 — RN<1> 3 LVMSGAM

20 MIL

C1435 4.7UF 20% 10V 3216

C1381 .1UF

20 MIL

U94 DS2119M

DIFFSENSE, TPWR1, TPWR2, DIFF_CAP, HS_GND, HS_GND, GND, ISO, MSTR/SLV, VREF, IC

RP<9> LVSCDAP5 25 — RN<9> 26 LVSCDAM5

RP<8> LVSCDAP7 23 — RN<8> 24 LVSCDAM7

RP<7> LVATNAP 20 — RN<7> 21 LVATNAM

RP<6> LVBSYAP 18 — RN<6> 19 LVBSYAM

RP<5> LVRSTAP 11 — RN<5> 12 LVRSTAM

RP<4> LVACKAP 9 — RN<4> 10 LVACKAM

RP<3> LVSCDAPLP 7 — RN<3> 8 LVSCDAPLM

RP<2> LVSCDAP6 4 — RN<2> 5 LVSCDAM6

RP<1> LVSCDAP4 2 — RN<1> 3 LVSCDAM4

C1384 .1UF

20 MIL

C1436 4.7UF 20% 10V 3216

C1382 .1UF

20 MIL

U95 DS2119M

DIFFSENSE, TPWR1, TPWR2, DIFF_CAP, HS_GND, HS_GND, GND, ISO, MSTR/SLV, VREF, IC

RP<9> LVSCDAP13 25 — RN<9> 26 LVSCDAM13

RP<8> LVSCDAP15 23 — RN<8> 24 LVSCDAM15

RP<7> LVSCDAP0 20 — RN<7> 21 LVSCDAM0

RP<6> LVSCDAP2 18 — RN<6> 19 LVSCDAM2

RP<5> LVSCDAP3 11 — RN<5> 12 LVSCDAM3

RP<4> LVSCDAP1 9 — RN<4> 10 LVSCDAM1

RP<3> LVSCDAPHP 7 — RN<3> 8 LVSCDAPHM

RP<2> LVSCDAP14 4 — RN<2> 5 LVSCDAM14

RP<1> LVSCDAP12 2 — RN<1> 3 LVSCDAM12

20 MIL

C1437 4.7UF 20% 10V 3216

C1383 .1UF

20 MIL

TERMINATION SCSI CHANNEL B

DRAWING

PAGE	REV
66	A2.1

40 MIL

LVTRMPWR_B IN 64C2> 62A2<

C1388 .1UF

C1441 10UF 20% 16V TANT 3528

R704 4.7K 5% 1/16W 603

U96
DS2119M

DIFFSENSE TPWR1 TPWR2 DIFF_CAP HS_GND HS_GND GND ISO MSTR/SLV VREF IC

RP<9> RP<8> RP<7> RP<6> RP<5> RP<4> RP<3> RP<2> RP<1>

RN<9> RN<8> RN<7> RN<6> RN<5> RN<4> RN<3> RN<2> RN<1>

LVSELBP LVREQBP LVSCDBP8 LVSCDBP10 LVSCDBP11 LVSCDBP9 LVIOBP LVCDBP LVMSGBP

LVSELBM LVREQBM LVSCDBM8 LVSCDBM10 LVSCDBM11 LVSCDBM9 LVIOBM LVCDBM LVMSGBM

C1440 4.7UF 20% 10V 3216

C1387 .1UF

20 MIL

U97
DS2119M

DIFFSENSE TPWR1 TPWR2 DIFF_CAP HS_GND HS_GND GND ISO MSTR/SLV VREF IC

RP<9> RP<8> RP<7> RP<6> RP<5> RP<4> RP<3> RP<2> RP<1>

RN<9> RN<8> RN<7> RN<6> RN<5> RN<4> RN<3> RN<2> RN<1>

LVSCDBP5 LVSCDBP7 LVATNBP LVBSYBP LVRSTBP LVACKBP LVSCDBPLP LVSCDBP6 LVSCDBP4

LVSCDBM5 LVSCDBM7 LVATNBM LVBSYBM LVRSTBM LVACKBM LVSCDBPLM LVSCDBM6 LVSCDBM4

20K R708

C1389 .1UF

C1439 4.7UF 20% 10V 3216

C1386 .1UF

20 MIL

U98
DS2119M

DIFFSENSE TPWR1 TPWR2 DIFF_CAP HS_GND HS_GND GND ISO MSTR/SLV VREF IC

RP<9> RP<8> RP<7> RP<6> RP<5> RP<4> RP<3> RP<2> RP<1>

RN<9> RN<8> RN<7> RN<6> RN<5> RN<4> RN<3> RN<2> RN<1>

LVSCDBP13 LVSCDBP15 LVSCDBP0 LVSCDBP2 LVSCDBP3 LVSCDBP1 LVSCDBPHP LVSCDBP14 LVSCDBP12

LVSCDBM13 LVSCDBM15 LVSCDBM0 LVSCDBM2 LVSCDBM3 LVSCDBM1 LVSCDBPHM LVSCDBM14 LVSCDBM12

C1438 4.7UF 20% 10V 3216

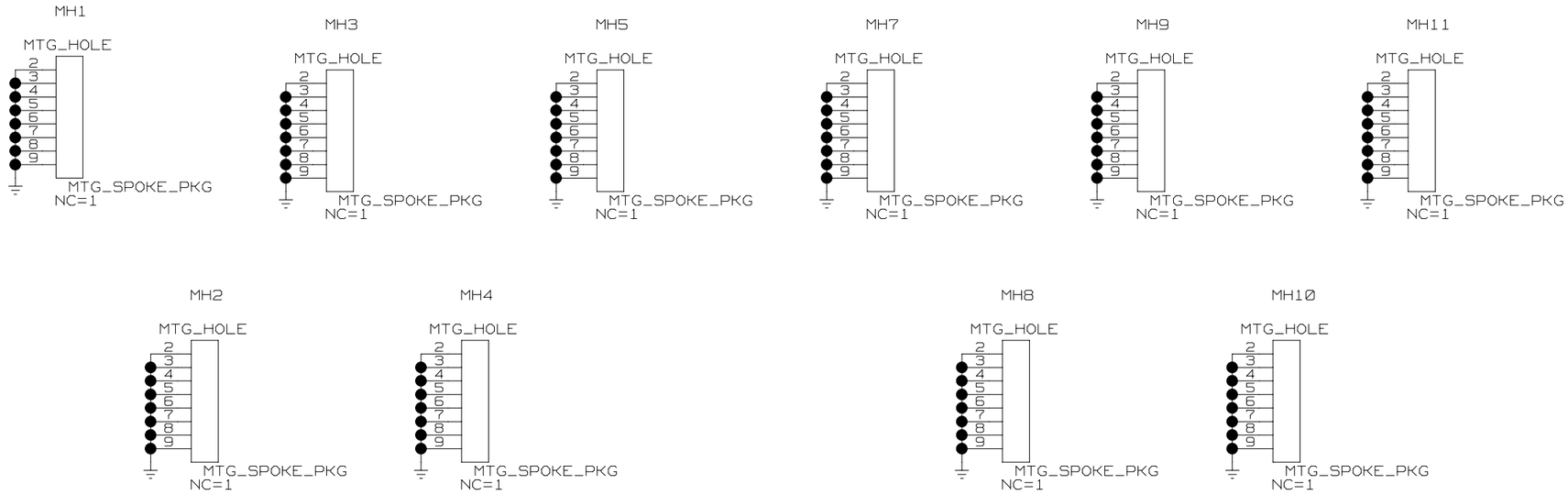
C1385 .1UF

20 MIL

64B4> 60B4<> BI DIFFSENSEB_R

60B1> IN CHB_TERMEN

R709 1K



MOUNTING HOLES

DRAWING

PAGE	REV
67	A2.1

+12V INPUT CAPS

+12V
C51 .01UF 5% 50V X7R 603
+12V
C74 10UF 20% 15V Y5V 1210
C75 10UF 20% 15V Y5V 1210

VCC
C59 .01UF 5% 50V X7R 603
C78 1.0UF 10% 10V X5R 805

VCC3
R54 680 5% CH 603
50B3> IN VID_PGOOD
R141 2 0 603 1A CH
ICH3_VRMPWRGD OUT 41C6<

VCC
+12V
R121 1M 5% CH 603
R119 10 5% CH 603
C72 1UF 20% 6.3V X5R 603
C73 1000PF 10% 50V X7R 603

U4
SC1470 IC
VCC 10
VIN 2
VCCA 4
FB 5
ILIM 11
EN/PSV 1
LX 12
VOUT 3
PGOOD 6
DH 13
DL 9
BST 14
AGND 7
GND 8
VCCP_PGOOD OUT 48A4<

VCC
R140 2 0 603 1A EMPTY
C88 .01UF 5% 50V X7R 603
R31 2 8.25K 603 1% CH

VCC
CR12 30V SM DIO 5A SCHOTTKY
R122 2 0 603 1A CH
C60 .1UF 10% 16V X7R 603

SI4966-DY IC
MOSFET_DUAL_8P
U5
D2<2> 6
D2<1> 5
S2 3
D1<2> 8
D1<1> 7
S1 1
G2 4
G1 2
+12V

L1 3.3UH IND
R86 2 .002 1% SM METAL
VCCP

CR13 30V SM DIO 5A SCHOTTKY
R69 4.02 5% EMPTY 1206
C94 100PF 5% 50V NPO 603
1_05_FBK

C90 100PF 5% 50V NPO 603
R37 11.0K .1% CH 603
R36 10K .1% CH 603
NOTE: 0.1% TOLERANCE

C91 1UF 20% 6.3V X5R 603
MUST USE 12-MILLI OHM POS/SP CAP
C80 330UF 10% 4V TANT 7343
CR14 40V SM DIO 1A SCHOTTKY

1_05_AGND
TIE AGND AND GND TOGETHER AT THE OUTPUT CAPS
R150 2 0 805 1A CH

1.05V VCCP REGULATION

DRAWING

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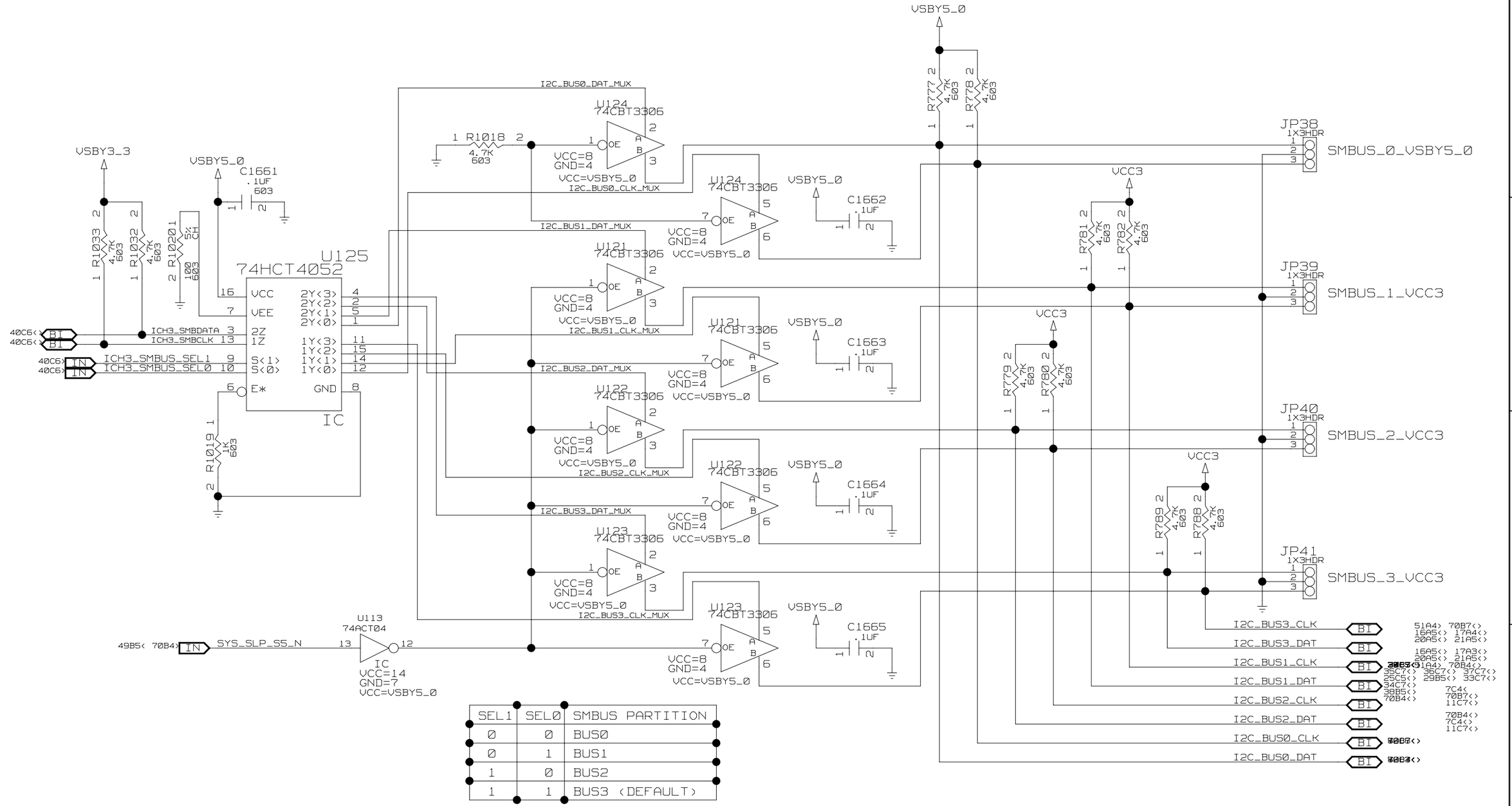

SEL1	SEL0	SMBUS PARTITION
0	0	BUS0
0	1	BUS1
1	0	BUS2
1	1	BUS3 (DEFAULT)

SMBUS MUX

DRAWING

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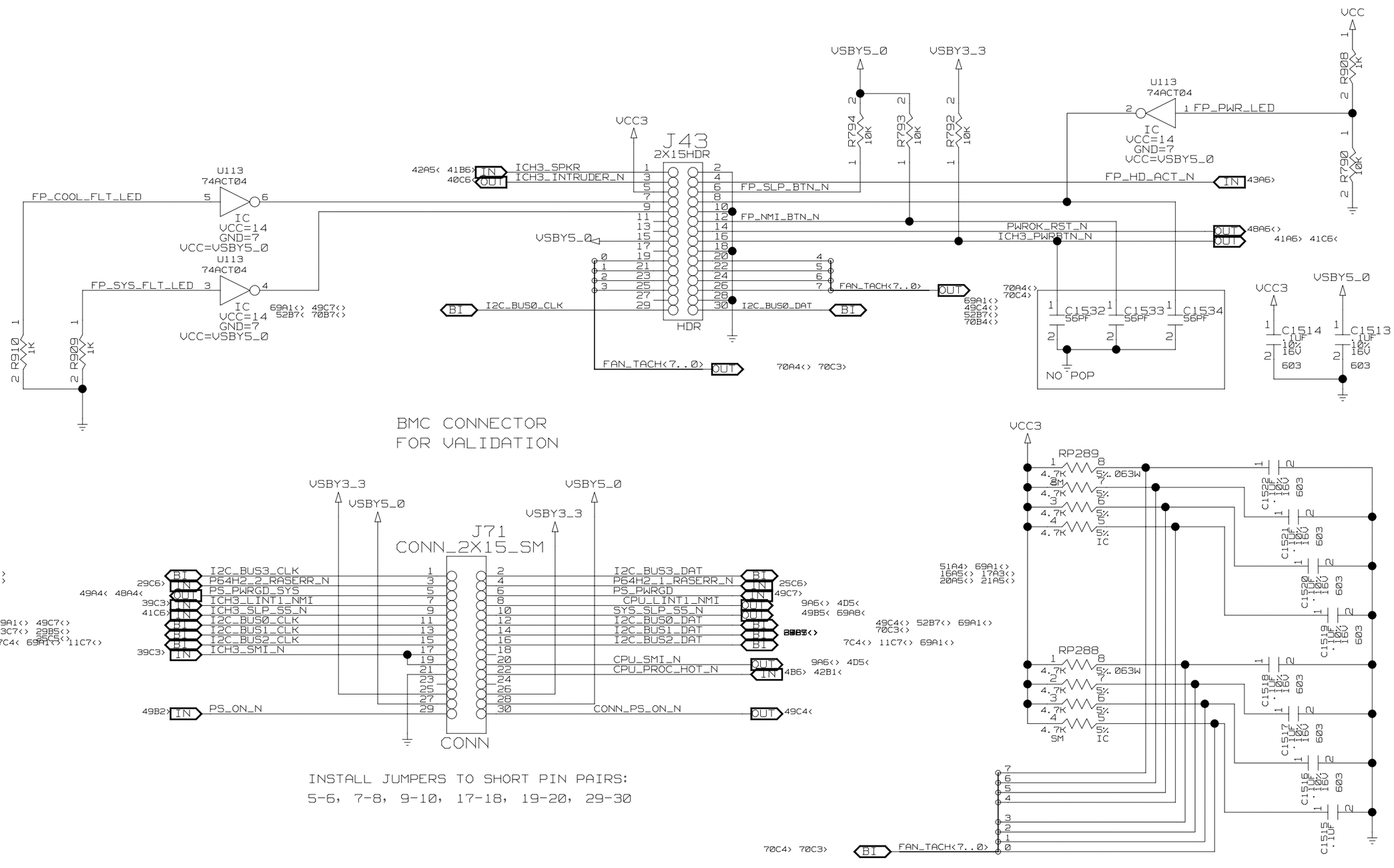
VCC
R908 1K
R790 10K
U113 74ACT04
FP_PWR_LED
IC VCC=14 GND=7 VCC=VSBY5_0
VSBY5_0
VSBY3_3
R794 10K
R793 10K
R792 10K
VCC3
J43
2X15HDR
ICH3_SPKR
ICH3_INTRUDER_N
FP_SLP_BTN_N
FP_NMI_BTN_N
PWROK_RST_N
ICH3_PWRBTN_N
FP_HD_ACT_N
FAN_TACH<7..0>
I2C_BUS0_CLK
I2C_BUS0_DAT
HDR
FP_COOL_FLT_LED
FP_SYS_FLT_LED
R910 1K
R909 1K
C1532 56PF
C1533 56PF
C1534 56PF
NO POP
C1514 .1UF 10% 16V 603
C1513 .1UF 10% 16V 603
BMC CONNECTOR
FOR VALIDATION
J71
CONN_2X15_SM
I2C_BUS3_CLK
P64H2_2_RASERR_N
PS_PWRGD_SYS
ICH3_LINT1_NMI
ICH3_SLP_S5_N
I2C_BUS0_CLK
I2C_BUS1_CLK
I2C_BUS2_CLK
ICH3_SMI_N
PS_ON_N
I2C_BUS3_DAT
P64H2_1_RASERR_N
PS_PWRGD
CPU_LINT1_NMI
SYS_SLP_S5_N
I2C_BUS0_DAT
I2C_BUS1_DAT
I2C_BUS2_DAT
CPU_SMI_N
CPU_PROC_HOT_N
CONN_PS_ON_N
CONN
INSTALL JUMPERS TO SHORT PIN PAIRS:
5-6, 7-8, 9-10, 17-18, 19-20, 29-30
RP289 4.7K 5% .063W SM
RP288 4.7K 5% .063W SM
C1522 .1UF 10% 16V 603
C1521 .1UF 10% 16V 603
C1520 .1UF 10% 16V 603
C1519 .1UF 10% 16V 603
C1518 .1UF 10% 16V 603
C1517 .1UF 10% 16V 603
C1516 .1UF 10% 16V 603
C1515 .1UF 10% 16V 603
FAN_TACH<7..0>
FRONT PANEL CONNECTOR
DRAWING
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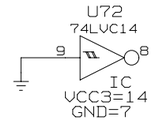
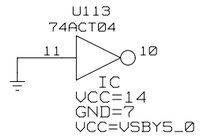
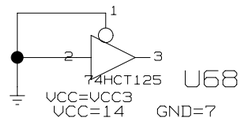
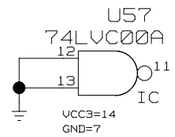
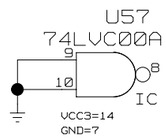
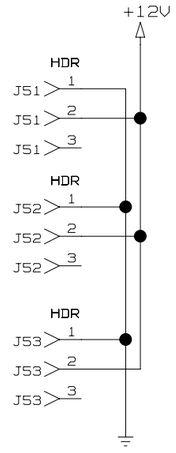








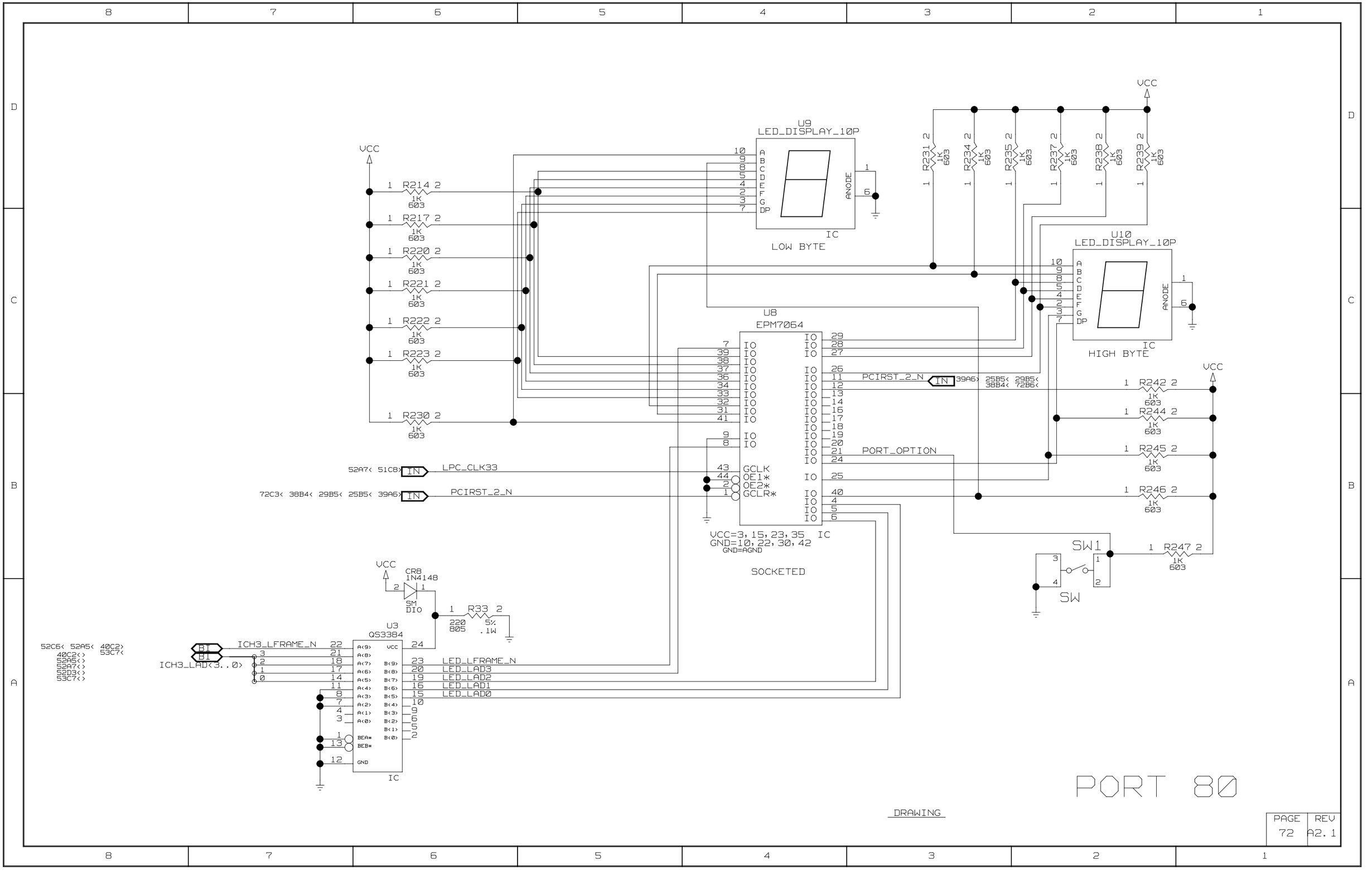




SPARE GATES

DRAWING

PAGE	REV
71	A2.1


U9
LED_DISPLAY_10P
ANODE
IC
LOW BYTE
U10
LED_DISPLAY_10P
ANODE
IC
HIGH BYTE
VCC
R214 2
R217 2
R220 2
R221 2
R222 2
R223 2
R230 2
R231 2
R234 2
R235 2
R237 2
R238 2
R239 2
1K
603
U8
EPM7064
PCIRST_2_N
IN
PORT_OPTION
LPC_CLK33
GCLK
OE1*
OE2*
GCLR*
VCC=3, 15, 23, 35 IC
GND=10, 22, 30, 42
GND=AGND
SOCKETED
R242 2
R244 2
R245 2
R246 2
R247 2
SW1
SW
CR8
1N4148
SM
DIO
R33 2
220
805
5%
.1W
U3
QS3384
ICH3_LFRAME_N
ICH3_LAD<3..0>
LED_LFRAME_N
LED_LAD3
LED_LAD2
LED_LAD1
LED_LAD0
VCC
GND
BEA*
BEB*
IC
PORT 80
DRAWING
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REV
A2.1

*** Signal Cross-Reference ***
--- for the entire design --

1_2_PGOOD	55D5> 47B8<
1_05_AGND	68A4<
1_05_FBK	68A4<
1_8V_PGOOD	38B1> 48D8<> 51B8<
2_5V_PGOOD	47B6> 48A4<
1929_VOS_M	47A3<
1929_VOS_P	47A3<
82544EI_TEST	56A4<> 56B2<>
AIC7902_TERMPWRA	62C5<
AIC7902_TERMPWRB	62C5<
AIC7902_TEST0	62A8<> 62B5<>
AIC7902_TEST1	62A8<> 62B5<>
AIC7902_TEST2	59A3<> 62A8<>
AIC7902_TEST3	62A8<> 62B5<>
AIC7902_TEST9	62A8<> 62B7<>
AIC_CLKNM	63A4> 60B8<
AIC_CLKNM_R	60B7<
AIC_CLKNP	63A3> 60B8<
AIC_CLKNP_R	60B7<
AUX_PWR	56B7<
CHA_TERMEN	60B5> 65A5<
CHB_TERMEN	60B1> 66A5<
CK408_IREF	51A5<>
CK408_MULT0	51B5<
CK408_PICSTP_N	51B5<
CK408_S1	51A5<
CK408_S2	51A5<
CK408_VTT_PWRGD_N	51B7<
CK408_XTAL_IN	51C7<
CK408_XTAL_OUT	51C7<>
CLK66_0	51B5<>
CLK66_1	51B5<>
CLK_14MHZ_SIO	51D6> 53A3<
COM_CTS1_N	54C1> 53B6<
COM_DCD1_N	54C1> 53B6<
COM_DSR1_N	54C1> 53B6<
COM_DTR1_N	53B6> 54C1<
COM_RI1_N	54C1> 53B6<
COM_RTS1_N	53B6> 54C1<
COM_RXD1	54C1> 53B6<
COM_TXD1	53B6> 54C1<
CONN_PS_ON_N	70A4> 49C4<
CON_BLUE	45B1<
CON_DDCCLK	45A1<
CON_DDCDAT	45B1<
CON_GREEN	45B1<
CON_HSYNC	45B1<
CON_KBCLK	54C6<
CON_KBDATA	54D6<
CON_MSCLK	54C6<
CON_MSDATA	54C6<
CON_RED	45B1<
CON_VSYNC	45B1<
CPU0_BCLK0_R	51B5<>
CPU0_BCLK1_R	51B5<>
CPU_BCLK0	51B1> 4D2<
CPU_BCLK1	51B1> 4D2<
CPU_COMP<3..0>	4C3<> 4D3<>
CPU_DPWR_N	4D4<
CPU_GTLREF_0	4D4<
CPU_IERR_N	4B7<>
CPU_LINT1_NMI	9A6<> 70B4> 4D4<
CPU_OK	49A3<
CPU_OK_N	49A4<>
CPU_OK_N_R	49A3<
CPU_PROC_HOT_3V_N	42B5> 40C6<
CPU_PROC_HOT_N	4B6> 42B1< 70A4<
CPU_PSI_3V_N	42D5> 40C6<
CPU_PSI_N	4D2> 42C1<
CPU_SMI_N	9A6<> 70B4> 4D4<
CPU_TEST<3..1>	4C3<
CPU_THERMDA	4C2<> 7D4<
CPU_THERMDC	4C2<> 7D4<
CPU_THRM_TRIP_N	4A6> 7A8<
CPU_VCCSENSE	4C3<>
CPU_VID<5..0>	4D2> 49B6<
CPU_VSSSENSE	4C3<>
DDRA_BA0_R	12C4> 22B8<> 16A4< 17A4<
DDRA_BA1_R	12C4> 18D8<> 16A4< 17A4<
DDRA_CAS_N_R	12D4> 18C6<> 16A5< 17A5<
DDRA_CB0	12A8<> 15D8<>
DDRA_CB0_R	15D7<> 16D2<> 17D2<> 18D8<>
DDRA_CB1	12A8<> 15D8<>
DDRA_CB1_R	15D7<> 16D2<> 17D2<> 18D8<>
DDRA_CB2	12A8<> 15D5<>
DDRA_CB2_R	15D4<> 16D2<> 17D2<> 18D8<
DDRA_CB3	12A8<> 15D5<>
DDRA_CB3_R	15D4<> 16D2<> 17D2<> 18D8<>
DDRA_CB4	12A8<> 15D8<>
DDRA_CB4_R	15D7<> 16D3<> 17D2<> 18A8<>
DDRA_CB5	12A8<> 15D8<>
DDRA_CB5_R	15D7<> 16D3<> 17D2<> 18B6<>
DDRA_CB6	12A8<> 15D5<>
DDRA_CB6_R	15D4<> 16D3<> 17D2<> 18C8<>
DDRA_CB7	12A8<> 15D5<>
DDRA_CB7_R	15D4<> 16D3<> 17D2<> 18C8<>
DDRA_CKE	12B4> 18A6<> 16A4< 17A4<
DDRA_CMDCLK0	12B4> 16A4<
DDRA_CMDCLK0_N	12A4> 16A4<
DDRA_CMDCLK1	12B4> 17A4<
DDRA_CMDCLK1_N	12A4> 17A4<
DDRA_CS0_N_R	12C4> 22C6<> 16A5<
DDRA_CS1_N_R	12C4> 22C6<> 16A5<
DDRA_CS2_N_R	12C4> 18B8<> 17A5<
DDRA_CS3_N_R	12C4> 18B8<> 17A5<
DDRA_DQ0	12A8<> 15D3<>
DDRA_DQ0_R	15D2<> 16D3<> 17D2<> 22A8<>
DDRA_DQ1	12A8<> 15A5<>
DDRA_DQ1_R	15A4<> 16D3<> 17D3<> 22A8<>
DDRA_DQ2	12A8<> 15A5<>
DDRA_DQ2_R	15A4<> 16D3<> 17D3<> 18C6<>
DDRA_DQ3	12A8<> 15A5<>
DDRA_DQ3_R	15A4<> 16D3<> 17D3<> 18C6<>
DDRA_DQ4	12A8<> 15D3<>
DDRA_DQ4_R	15D2<> 16D3<> 17D3<> 22A8<>
DDRA_DQ5	12A8<> 15D3<>
DDRA_DQ5_R	15D2<> 16D3<> 17D3<> 22A8<>
DDRA_DQ6	12A8<> 15A5<>
DDRA_DQ6_R	15A4<> 16D3<> 17D3<> 18C6<>
DDRA_DQ7	12A8<> 15A5<>
DDRA_DQ7_R	15A4<> 16D3<> 17D3<> 18C6<>
DDRA_DQ8	12A8<> 15B5<>
DDRA_DQ8_R	15B4<> 16D3<> 17D3<> 18C6<>
DDRA_DQ9	12A8<> 15A5<>
DDRA_DQ9_R	15A4<> 16D3<> 17D3<> 18D6<>
DDRA_DQ10	12A8<> 15B5<>
DDRA_DQ10_R	15B4<> 16D3<> 17D3<> 18A6<>
DDRA_DQ11	12A8<> 15B5<>
DDRA_DQ11_R	15B4<> 16D3<> 17D3<> 18A6<>
DDRA_DQ12	12B8<> 15B5<>
DDRA_DQ12_R	15B4<> 16D4<> 17D3<> 18C6<>
DDRA_DQ13	12B8<> 15A5<>
DDRA_DQ13_R	15A4<> 16D4<> 17D3<> 18D6<>
DDRA_DQ14	12B8<> 15A5<>
DDRA_DQ14_R	15A4<> 16D4<> 17D3<> 18A6<>
DDRA_DQ15	12B8<> 15A5<>
DDRA_DQ15_R	15A4<> 16D4<> 17D3<> 18A6<>
DDRA_DQ16	12B8<> 15B5<>
DDRA_DQ16_R	15B4<> 16D4<> 17D3<> 18A6<>
DDRA_DQ17	12B8<> 15C5<>
DDRA_DQ17_R	15C4<> 16D4<> 17D4<> 18A6<>
DDRA_DQ18	12B8<> 15B5<>
DDRA_DQ18_R	15B4<> 16D4<> 17D4<> 18A8<>
DDRA_DQ19	12B8<> 15B5<>
DDRA_DQ19_R	15B4<> 16D4<> 17D4<> 18A6<>
DDRA_DQ20	12B8<> 15B5<>
DDRA_DQ20_R	15B4<> 16D4<> 17D4<> 18A6<>
DDRA_DQ21	12B8<> 15C5<>
DDRA_DQ21_R	15C4<> 16D4<> 17D4<> 18A6<>
DDRA_DQ22	12B8<> 15B5<>
DDRA_DQ22_R	15B4<> 16D4<> 17D4<> 18A8<>
DDRA_DQ23	12B8<> 15B5<>
DDRA_DQ23_R	15B4<> 16D4<> 17D4<> 18B6<>
DDRA_DQ24	12B8<> 15C5<>
DDRA_DQ24_R	15C4<> 16D4<> 17D4<> 18D6<>
DDRA_DQ25	12B8<> 15C5<>
DDRA_DQ25_R	15C4<> 16D4<> 17D4<> 18D6<>
DDRA_DQ26	12B8<> 15C5<>
DDRA_DQ26_R	15C4<> 16D4<> 17D4<> 18B6<>
DDRA_DQ27	12B8<> 15D8<>
DDRA_DQ27_R	15D7<> 16D4<> 17D4<> 18A8<>
DDRA_DQ28	12B8<> 15C5<>
DDRA_DQ28_R	15C4<> 16D5<> 17D4<> 18D6<>
DDRA_DQ29	12B8<> 15C5<>
DDRA_DQ29_R	15C4<> 16D5<> 17D4<> 18D8<>
DDRA_DQ30	12B8<> 15C5<>
DDRA_DQ30_R	15C4<> 16D5<> 17D4<> 18D8<>
DDRA_DQ31	12C8<> 15D8<>
DDRA_DQ31_R	15D7<> 16D5<> 17D4<> 18B6<>
DDRA_DQ32	12C8<> 15D5<>
DDRA_DQ32_R	15D4<> 16D5<> 17D4<> 18A8<>
DDRA_DQ33	12C8<> 15D5<>
DDRA_DQ33_R	15D4<> 16D5<> 17D5<> 18A8<>
DDRA_DQ34	12C8<> 15A8<>
DDRA_DQ34_R	15A7<> 16D5<> 17D5<> 18B6<>
DDRA_DQ35	12C8<> 15C8<>
DDRA_DQ35_R	15C7<> 16D5<> 17D5<> 18A8<>
DDRA_DQ36	12C8<> 15D5<>
DDRA_DQ36_R	15D4<> 16D5<> 17D5<> 18A8<>
DDRA_DQ37	12C8<> 15D5<>
DDRA_DQ37_R	15D4<> 16D5<> 17D5<> 18A8<>
DDRA_DQ38	12C8<> 15A8<>
DDRA_DQ38_R	15A7<> 16D5<> 17D5<> 18B6<>
DDRA_DQ39	12C8<> 15C8<>
DDRA_DQ39_R	15C7<> 16D5<> 17D5<> 18A8<>
DDRA_DQ40	12C8<> 15C8<>
DDRA_DQ40_R	15C7<> 16D5<> 17D5<> 18B8<>
DDRA_DQ41	12C8<> 15A8<>
DDRA_DQ41_R	15A7<> 16D5<> 17D5<> 18C6<>
DDRA_DQ42	12C8<> 15A8<>
DDRA_DQ42_R	15A7<> 16D5<> 17D5<> 18D6<>
DDRA_DQ43	12C8<> 15A8<>
DDRA_DQ43_R	15A7<> 16D5<> 17D5<> 18D6<>
DDRA_DQ44	12C8<> 15C8<>
DDRA_DQ44_R	15C7<> 16D6<> 17D5<> 18B8<>
DDRA_DQ45	12C8<> 15A8<>
DDRA_DQ45_R	15A7<> 16D6<> 17D5<> 18A8<>
DDRA_DQ46	12C8<> 15A8<>
DDRA_DQ46_R	15A7<> 16D6<> 17D5<> 18D6<>
DDRA_DQ47	12C8<> 15A8<>
DDRA_DQ47_R	15A7<> 16D6<> 17D5<> 18D6<>
DDRA_DQ48	12C8<> 15B8<>
DDRA_DQ48_R	15B7<> 16D6<> 17D5<> 18B8<>
DDRA_DQ49	12C8<> 15B8<>
DDRA_DQ49_R	15B7<> 16D6<> 17D6<> 18B8<>
DDRA_DQ50	12D8<> 15B8<>
DDRA_DQ50_R	15B7<> 16D6<> 17D6<> 18C8<>
DDRA_DQ51	12D8<> 15B8<>
DDRA_DQ51_R	15B7<> 16D6<> 17D6<> 18C8<>
DDRA_DQ52	12D8<> 15B8<>
DDRA_DQ52_R	15B7<> 16D6<> 17D6<> 18B8<>
DDRA_DQ53	12D8<> 15A8<>
DDRA_DQ53_R	15A7<> 16D6<> 17D6<> 18B8<>
DDRA_DQ54	12D8<> 15B8<>
DDRA_DQ54_R	15B7<> 16D6<> 17D6<> 18C8<>
DDRA_DQ55	12D8<> 15B8<>
DDRA_DQ55_R	15B7<> 16D6<> 17D6<> 18C8<>
DDRA_DQ56	12D8<> 15C8<>
DDRA_DQ56_R	15C7<> 16D6<> 17D6<> 18B6<>
DDRA_DQ57	12D8<> 15C8<>
DDRA_DQ57_R	15C7<> 16D6<> 17D6<> 18C6<>
DDRA_DQ58	12D8<> 15C8<>
DDRA_DQ58_R	15C7<> 16D6<> 17D6<> 18B8<>
DDRA_DQ59	12D8<> 15C8<>
DDRA_DQ59_R	15C7<> 16D6<> 17D6<> 18B8<>
DDRA_DQ60	12D8<> 15B8<>
DDRA_DQ60_R	15B7<> 16D7<> 17D6<> 18C8<>
DDRA_DQ61	12D8<> 15B8<>
DDRA_DQ61_R	15B7<> 16D7<> 17D6<> 18C8<>
DDRA_DQ62	12D8<> 15C8<>
DDRA_DQ62_R	15C7<> 16D7<> 17D6<> 18C6<>
DDRA_DQ63	12D8<> 15C8<>
DDRA_DQ63_R	15C7<> 16D7<> 17D6<> 18B8<>
DDRA_DQS0	12A8<> 15A5<>
DDRA_DQS0_R	15A4<> 16D3<> 17D3<> 18C6<>
DDRA_DQS1	12A8<> 15A5<>
DDRA_DQS1_R	15A4<> 16D3<> 17D3<> 18D6<>
DDRA_DQS2	12B8<> 15C5<>
DDRA_DQS2_R	15C4<> 16D4<> 17D4<> 18A6<>
DDRA_DQS3	12B8<> 15C5<>
DDRA_DQS3_R	15C4<> 16D4<> 17D4<> 18B6<>
DDRA_DQS4	12C8<> 15A8<>
DDRA_DQS4_R	15A7<> 16D5<> 17D5<> 18B6<>
DDRA_DQS5	12C8<> 15A8<>
DDRA_DQS5_R	15A7<> 16D5<> 17D5<> 18C6<>
DDRA_DQS6	12D8<> 15B8<>
DDRA_DQS6_R	15B7<> 16D6<> 17D6<> 18C8<>
DDRA_DQS7	12D8<> 15C8<>
DDRA_DQS7_R	15C7<> 16D6<> 17D6<> 18B8<>
DDRA_DQS8	12A8<> 15D8<>
DDRA_DQS8_R	15D7<> 16D2<> 17D2<> 18D8<>
DDRA_DQS9	12A8<> 15A5<>
DDRA_DQS9_R	15A4<> 16D3<> 17D3<> 18C6<>
DDRA_DQS10	12A8<> 15A5<>
DDRA_DQS10_R	15A4<> 16D4<> 17D3<> 18D6<>
DDRA_DQS11	12B8<> 15C5<>
DDRA_DQS11_R	15C4<> 16D4<> 17D4<> 18A8<>
DDRA_DQS12	12B8<> 15C5<>
DDRA_DQS12_R	15C4<> 16D5<> 17D4<> 18D8<>
DDRA_DQS13	12C8<> 15A8<>
DDRA_DQS13_R	15A7<> 16D5<> 17D5<> 18B6<>
DDRA_DQS14	12C8<> 15A8<>
DDRA_DQS14_R	15A7<> 16D6<> 17D5<> 18A8<>
DDRA_DQS15	12D8<> 15B8<>
DDRA_DQS15_R	15B7<> 16D6<> 17D6<> 18B8<>
DDRA_DQS16	12D8<> 15C8<>
DDRA_DQS16_R	15C7<> 16D7<> 17D6<> 18C6<>
DDRA_DQS17	12A8<> 15D8<>
DDRA_DQS17_R	15D7<> 16D3<> 17D2<> 18D8<>
DDRA_DRCOMP	12B3<
DDRA_MA0_R	12D4> 18D8<> 16A4< 17A4<
DDRA_MA1_R	12D4> 18A8<> 16A5< 17A4<
DDRA_MA2_R	12D4> 18A8<> 16A5< 17A4<
DDRA_MA3_R	12D4> 18B6<> 16A5< 17A4<
DDRA_MA4_R	12D4> 18B6<> 16A5< 17A4<
DDRA_MA5_R	12D4> 18A6<> 16A5< 17A4<
DDRA_MA6_R	12D4> 18D6<> 16A5< 17A4<
DDRA_MA7_R	12D4> 18A8<> 16A5< 17A5<
DDRA_MA8_R	12D4> 18B6<> 16A5< 17A5<
DDRA_MA9_R	12D4> 18A6<> 16A5< 17A5<
DDRA_MA10_R	12D4> 18C8<> 16A5< 17A5<
DDRA_MA11_R	12D4> 18A6<> 16A5< 17A5<
DDRA_MA12_R	12D4> 18A6<> 16A5< 17A5<
DDRA_RAS_N_R	12D4> 22B8<> 16A5< 17A5<
DDRA_RCV_EN_IN	12B5<
DDRA_RCV_EN_OUT	12B5<>
DDRA_WE_N_R	12D4> 18C6<> 16A5< 17A5<
DDRBCVOL_B	13B4<
DDRB_BA0_R	13C4> 18D4<> 20A4< 21A4<
DDRB_BA1_R	13C4> 22B6<> 20A4< 21A4<
DDRB_CAS_N_R	13D4> 22D8<> 20A5< 21A5<
DDRB_CB0	13A8<> 19D8<>
DDRB_CB0_R	19D6<> 20D2<> 21D2<> 22D8<>
DDRB_CB1	13A8<> 19D8<>
DDRB_CB1_R	18C8<> 19D6<> 20D2<> 21D2<>
DDRB_CB2	13A8<> 19B5<>
DDRB_CB2_R	19B4<> 20D2<> 21D2<> 22D8<>
DDRB_CB3	13A8<> 19C5<>
DDRB_CB3_R	19C4<> 20D2<> 21D3<> 22B6<>
DDRB_CB4	13A8<> 19A8<>
DDRB_CB4_R	19A6<> 20D3<> 21D3<> 22D6<>
DDRB_CB5	13A8<> 19A8<>
DDRB_CB5_R	19A6<> 20D3<> 21D3<> 22D6<>
DDRB_CB6	13A8<> 19C5<>
DDRB_CB6_R	19C4<> 20D3<> 21D3<> 22B6<>
DDRB_CB7	13A8<> 19C5<>
DDRB_CB7_R	19C4<> 20D3<> 21D3<> 22B6<>
DDRB_CKE	13B4> 22D6<> 20A4< 21A4<
DDRB_CMDCLK0	13A4> 20A4<
DDRB_CMDCLK0_N	13A4> 20A4<
DDRB_CMDCLK1	13A4> 21A4<
DDRB_CMDCLK1_N	13A4> 21A4<
DDRB_CS0_N_R	13C4> 22C6<> 20A5<
DDRB_CS1_N_R	13C4> 22C6<> 20A5<
DDRB_CS2_N_R	13C4> 18B8<> 21A5<
DDRB_CS3_N_R	13C4> 18B8<> 21A5<
DDRB_DQ0	13A8<> 19A5<>
DDRB_DQ0_R	19A4<> 20D3<> 21D3<> 22A6<>
DDRB_DQ1	13A8<> 19A5<>
DDRB_DQ1_R	19A4<> 20D3<> 21D3<> 22A6<>
DDRB_DQ2	13A8<> 19A5<>
DDRB_DQ2_R	19A4<> 20D3<> 21D3<> 22C6<>
DDRB_DQ3	13A8<> 19A5<>
DDRB_DQ3_R	19A4<> 20D3<> 21D3<> 22A8<>
DDRB_DQ4	13A8<> 19A5<>
DDRB_DQ4_R	19A4<> 20D3<> 21D3<> 22A6<>
DDRB_DQ5	13A8<> 19A5<>
DDRB_DQ5_R	19A4<> 20D3<> 21D3<> 22A6<>
DDRB_DQ6	13A8<> 19A5<>
DDRB_DQ6_R	19A4<> 20D3<> 21D3<> 22C6<>
DDRB_DQ7	13A8<> 19A5<>
DDRB_DQ7_R	19A4<> 20D3<> 21D3<> 22A8<>
DDRB_DQ8	13A8<> 19B5<>
DDRB_DQ8_R	19B4<> 20D3<> 21D3<> 22A8<>
DDRB_DQ9	13A8<> 19B5<>
DDRB_DQ9_R	19B4<> 20D3<> 21D3<> 22A8<>
DDRB_DQ10	13A8<> 19C5<>
DDRB_DQ10_R	19C4<> 20D3<> 21D3<> 22B8<>
DDRB_DQ11	13A8<> 19C5<>
DDRB_DQ11_R	19C4<> 20D3<> 21D4<> 22B8<>
DDRB_DQ12	13A8<> 19B5<>
DDRB_DQ12_R	19B4<> 20D4<> 21D4<> 22A8<>
DDRB_DQ13	13A8<> 19B5<>
DDRB_DQ13_R	19B4<> 20D4<> 21D4<> 22A8<>
DDRB_DQ14	13B8<> 19B5<>
DDRB_DQ14_R	19B4<> 20D4<> 21D4<> 22B8<>
DDRB_DQ15	13B8<> 19B5<>
DDRB_DQ15_R	19B4<> 20D4<> 21D4<> 22B8<>
DDRB_DQ16	13B8<> 19C5<>
DDRB_DQ16_R	19C4<> 20D4<> 21D4<> 22A8<>
DDRB_DQ17	13B8<> 19C5<>
DDRB_DQ17_R	19C4<> 20D4<> 21D4<> 22A8<>
DDRB_DQ18	13B8<> 19C5<>
DDRB_DQ18_R	19C4<> 20D4<> 21D4<> 22B6<>
DDRB_DQ19	13B8<> 19D5<>
DDRB_DQ19_R	19D4<> 20D4<> 21D4<> 22A8<>
DDRB_DQ20	13B8<> 19C5<>
DDRB_DQ20_R	19C4<> 20D4<> 21D4<> 22A8<>
DDRB_DQ21	13B8<> 19C5<>
DDRB_DQ21_R	19C4<> 20D4<> 21D4<> 22B6<>
DDRB_DQ22	13B8<> 19D5<>
DDRB_DQ22_R	19D4<> 20D4<> 21D4<> 22B6<>
DDRB_DQ23	13B8<> 19D5<>
DDRB_DQ23_R	19D4<> 20D4<> 21D4<> 22A8<>
DDRB_DQ24	13B8<> 19D5<>
DDRB_DQ24_R	19D4<> 20D4<> 21D4<> 22A6<>
DDRB_DQ25	13B8<> 19D5<>
DDRB_DQ25_R	19D4<> 20D4<> 21D4<> 22A6<>
DDRB_DQ26	13B8<> 19D5<>
DDRB_DQ26_R	19D4<> 20D4<> 21D4<> 22B6<>
DDRB_DQ27	13B8<> 19A8<>
DDRB_DQ27_R	19A6<> 20D4<> 21D5<> 22B6<>
DDRB_DQ28	13B8<> 19D5<>
DDRB_DQ28_R	19D4<> 20D5<> 21D5<> 22A6<>
DDRB_DQ29	13B8<> 19D5<>
DDRB_DQ29_R	19D4<> 20D5<> 21D5<> 22B6<>
DDRB_DQ30	13B8<> 19D5<>
DDRB_DQ30_R	19D4<> 20D5<> 21D5<> 22B6<>
DDRB_DQ31	13B8<> 19A8<>
DDRB_DQ31_R	19A6<> 20D5<> 21D5<> 22D6<>
DDRB_DQ32	13B8<> 19B8<>
DDRB_DQ32_R	19B6<> 20D5<> 21D5<> 22C6<>
DDRB_DQ33	13C8<> 19C8<>
DDRB_DQ33_R	19C6<> 20D5<> 21D5<> 22C6<>
DDRB_DQ34	13C8<> 19A8<>
DDRB_DQ34_R	19A6<> 20D5<> 21D5<> 22B8<>
DDRB_DQ35	13C8<> 19A8<>
DDRB_DQ35_R	18D4<> 19A6<> 20D5<> 21D5<>
DDRB_DQ36	13C8<> 19B8<>
DDRB_DQ36_R	19B6<> 20D5<> 21D5<> 22C6<>
DDRB_DQ37	13C8<> 19C8<>
DDRB_DQ37_R	19C6<> 20D5<> 21D5<> 22C6<>
DDRB_DQ38	13C8<> 19A8<>
DDRB_DQ38_R	19A6<> 20D5<> 21D5<> 22B8<>
DDRB_DQ39	13C8<> 19A8<>
DDRB_DQ39_R	18D4<> 19A6<> 20D5<> 21D5<>
DDRB_DQ40	13C8<> 19A8<>
DDRB_DQ40_R	19A6<> 20D5<> 21D5<> 22B8<>
DDRB_DQ41	13C8<> 19B8<>
DDRB_DQ41_R	19B6<> 20D5<> 21D5<> 22C8<>
DDRB_DQ42	13C8<> 19B8<>
DDRB_DQ42_R	19B6<> 20D5<> 21D5<> 22C8<>
DDRB_DQ43	13C8<> 19B8<>
DDRB_DQ43_R	19B6<> 20D5<> 21D6<> 22D8<>
DDRB_DQ44	13C8<> 19A8<>
DDRB_DQ44_R	19A6<> 20D6<> 21D6<> 22C8<>
DDRB_DQ45	13C8<> 19B8<>
DDRB_DQ45_R	19B6<> 20D6<> 21D6<> 22C8<
DDRB_DQ46	13C8<> 19B8<>
DDRB_DQ46_R	19B6<> 20D6<> 21D6<> 22D8<>
DDRB_DQ47	13C8<> 19B8<>
DDRB_DQ47_R	19B6<> 20D6<> 21D6<> 22D8<>
DDRB_DQ48	13C8<> 19C8<>
DDRB_DQ48_R	19C6<> 20D6<> 21D6<> 22A6<>
DDRB_DQ49	13C8<> 19C8<>
DDRB_DQ49_R	19C6<> 20D6<> 21D6<> 22A6<>
DDRB_DQ50	13C8<> 19D8<>
DDRB_DQ50_R	19D6<> 20D6<> 21D6<> 22C8<>
DDRB_DQ51	13C8<> 19C8<>
DDRB_DQ51_R	19C6<> 20D6<> 21D6<> 22C8<>
DDRB_DQ52	13D8<> 19C8<>
DDRB_DQ52_R	19C6<> 20D6<> 21D6<> 22A6<>

DRAWING

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```
DDRB_DQ53       13D8<> 19C8<>
DDRB_DQ53_R     19C6<> 20D6<> 21D6<> 22A6<>
DDRB_DQ54       13D8<> 19D8<>
DDRB_DQ54_R     19D6<> 20D6<> 21D6<> 22C6<>
DDRB_DQ55       13D8<> 19C8<>
DDRB_DQ55_R     19C6<> 20D6<> 21D6<> 22C6<>
DDRB_DQ56       13D8<> 19C8<>
DDRB_DQ56_R     19C6<> 20D6<> 21D6<> 22C8<>
DDRB_DQ57       13D8<> 19D2<>
DDRB_DQ57_R     19D1<> 20D6<> 21D6<> 22A6<>
DDRB_DQ58       13D8<> 19D8<>
DDRB_DQ58_R     19D6<> 20D6<> 21D6<> 22D6<>
DDRB_DQ59       13D8<> 19D8<>
DDRB_DQ59_R     19D6<> 20D6<> 21D7<> 22D6<>
DDRB_DQ60       13D8<> 19C8<>
DDRB_DQ60_R     19C6<> 20D7<> 21D7<> 22C8<>
DDRB_DQ61       13D8<> 19D2<>
DDRB_DQ61_R     19D1<> 20D7<> 21D7<> 22A6<>
DDRB_DQ62       13D8<> 19D8<>
DDRB_DQ62_R     19D6<> 20D7<> 21D7<> 22D6<>
DDRB_DQ63       13D8<> 19D8<>
DDRB_DQ63_R     19D6<> 20D7<> 21D7<> 22D6<>
DDRB_DQS0       13A8<> 19A5<>
DDRB_DQS0_R     19A4<> 20D3<> 21D3<> 22C6<>
DDRB_DQS1       13A8<> 19B5<>
DDRB_DQS1_R     19B4<> 20D4<> 21D4<> 22A8<>
DDRB_DQS2       13B8<> 19C5<>
DDRB_DQS2_R     19C4<> 20D4<> 21D4<> 22B8<>
DDRB_DQS3       13B8<> 19D5<>
DDRB_DQS3_R     19D4<> 20D5<> 21D5<> 22B6<>
DDRB_DQS4       13C8<> 19A8<>
DDRB_DQS4_R     19A6<> 20D5<> 21D5<> 22B8<>
DDRB_DQS5       13C8<> 19B8<>
DDRB_DQS5_R     19B6<> 20D6<> 21D6<> 22C8<>
DDRB_DQS6       13D8<> 19D8<>
DDRB_DQS6_R     19D6<> 20D6<> 21D6<> 22C6<>
DDRB_DQS7       13D8<> 19D2<>
DDRB_DQS7_R     19D1<> 20D7<> 21D7<> 22A6<>
DDRB_DQS8       13A8<> 19D8<>
DDRB_DQS8_R     18C8<> 19D6<> 20D3<> 21D3<>
DDRB_DQS9       13A8<> 19A5<>
DDRB_DQS9_R     19A4<> 20D3<> 21D3<> 22C6<>
DDRB_DQS10      13A8<> 19B5<>
DDRB_DQS10_R    19B4<> 20D4<> 21D4<> 22A8<>
DDRB_DQS11      13B8<> 19C5<>
DDRB_DQS11_R    19C4<> 20D4<> 21D4<> 22B6<>
DDRB_DQS12      13B8<> 19D5<>
DDRB_DQS12_R    19D4<> 20D5<> 21D5<> 22B6<>
DDRB_DQS13      13C8<> 19A8<>
DDRB_DQS13_R    19A6<> 20D5<> 21D5<> 22B8<>
DDRB_DQS14      13C8<> 19B8<>
DDRB_DQS14_R    19B6<> 20D6<> 21D6<> 22C8<>
DDRB_DQS15      13D8<> 19C8<>
DDRB_DQS15_R    19C6<> 20D6<> 21D6<> 22C6<>
DDRB_DQS16      13D8<> 19D2<>
DDRB_DQS16_R    19D1<> 20D7<> 21D7<> 22A6<>
DDRB_DQS17      13A8<> 19D8<>
DDRB_DQS17_R    18C8<> 19D6<> 20D3<> 21D3<>
DDRB_DRCOMP     13B3<>
DDRB_MA0_R      13D4> 18C8<> 20A5< 21A5<
DDRB_MA1_R      13D4> 22D8<> 20A5< 21A5<
DDRB_MA2_R      13D4> 22D6<> 20A5< 21A5<
DDRB_MA3_R      13D4> 22A6<> 20A5< 21A5<
DDRB_MA4_R      13D4> 22B6<> 20A5< 21A5<
DDRB_MA5_R      13D4> 22A8<> 20A5< 21A5<
DDRB_MA6_R      13D4> 22A6<> 20A5< 21A5<
DDRB_MA7_R      13D4> 22B6<> 20A5< 21A5<
DDRB_MA8_R      13D4> 22A8<> 20A5< 21A5<
DDRB_MA9_R      13D4> 22B8<> 20A5< 21A5<
DDRB_MA10_R     13D4> 22D8<> 20A5< 21A5<
DDRB_MA11_R     13D4> 22B8<> 20A5< 21A5<
DDRB_MA12_R     13D4> 22A8<> 20A5< 21A5<
DDRB_RAS_N_R    13D4> 18D4<> 20A5< 21A5<
DDRB_RCV_EN_IN  13B5<
DDRB_RCV_EN_OUT 13B5<>
DDRB_WE_N_R     13D4> 22D8<> 20A5< 21A5<
DDRCVOL_A       12B4<
DDRCVO_A        12B2<
DDRCVO_B        13B3<
DIFFSENSEA      60B7<
DIFFSENSEA_R    60B8<> 64B7<> 65C5<>
DIFFSENSEB      60B3<
DIFFSENSEB_R    60B4<> 64B3> 66A7<>
DIMM_A1_SA0     16A4<
DIMM_A1_SA1     16A4<
```

```
DIMM_A1_SA2     16A4<
DIMM_A2_SA0     17A3<
DIMM_A2_SA1     17A3<
DIMM_A2_SA2     17A3<
DIMM_B1_SA0     20A4<
DIMM_B1_SA1     20A4<
DIMM_B1_SA2     20A4<
DIMM_B2_SA0     21A4<
DIMM_B2_SA1     21A4<
DIMM_B2_SA2     21A4<
DIR_N           53D6> 54A2<
DRVEN0          53D6> 54B2<
DRVEN1          53D6> 54B2<
DSKCHG_N        54A2> 53C6<
DSO_N           53D6> 54A2<
EE_CS           56C4<>
EE_DI           56C4<>
EE_DO           56C4<>
EE_SK           56C4<>
FAN_TACH<7..0>  70A3<> 70C3> 70C4>
FP_COOL_FLT_LED 70D8<
FP_HD_ACT_N     43A6> 70D2<
FP_NMI_BTN_N    70C4<
FP_PWR_LED      70D2<
FP_SLP_BTN_N    70D4<
FP_SYS_FLT_LED  70C7<
FSB_ADSTB_N<1..0> 4D2<> 10C6<>
FSB_ADS_N       4B4<> 10A6<>
FSB_A_N<31..3>  4B6<> 10A6<>
FSB_BNR_N       4A4<> 10A6<>
FSB_BPRI_N      10A6> 4A4<
FSB_BREQ0_N     4A4<> 10A6<>
FSB_CPURST_N    9C4> 10A6> 4A4<
FSB_DBI_N<3..0> 4B6<> 10A6<>
FSB_DBSY_N      4A4<> 10A6<>
FSB_DEFER_N     10A6> 4A4<
FSB_DRDY_N      4A4<> 10A6<>
FSB_DSTBN_N<3..0> 4A1<> 10D6<>
FSB_DSTBP_N<3..0> 4A5<> 10C6<>
FSB_HD<63..0>   4A8<> 10C2<>
FSB_HITM_N      4A2<> 10D3<>
FSB_HIT_N       4A2<> 10D3<>
FSB_HLOCK_N     4A2<> 10D3<
FSB_HREQ_N<4..0> 4A1<> 10D2<>
FSB_HTRDY_N     10D3> 4A4<
FSB_HXRCOMP     10D5<
FSB_HXSWING     10D5<
FSB_HYRCOMP     10D6<
FSB_HYSWING     10D5<
FSB_H_CLKINN    51C1> 10D6<
FSB_H_CLKINN_R  51C5<>
FSB_H_CLKINP    51C1> 10D6<
FSB_H_CLKINP_R  51B5<>
FSB_RS_N<2..0>  10C6> 4A5<
FWH_CLK33       51C8> 52C6<
FWH_FGP_10      52C4<
FWH_FGP_11      52C4<
FWH_FGP_12      52C4<
FWH_FGP_13      52C4<
FWH_FGP_14      52C4<
FWH_IC          52D5<
FWH_INIT_N      52C4<
FWH_J4BIT_1     52D8<
FWH_J4BIT_4     52D7<
FWH_TBL_N       52D5<
FWH_WP_N        52D5<
GND=AGND        72B4<>
GP30            53A4<>
GP31            53A4<>
HDSEL_N         53C6> 54A2<
HIDRV           47D4<
HISWING_A       11B6<
HISWING_B       11C6<
HI_RCOMP_A      11B6<
HI_RCOMP_B      11C6<>
HI_RCOMP_C      11C4<>
HI_RCOMP_D      11C4<>
HI_VREF_A       11B6<
HI_VREF_B       11C6<
HI_VREF_C       11C4<
HI_VREF_D       11C4<
HI_VSWING_C     11C4<
HI_VSWING_D     11C4<
I2C_BUS0_CLK    49C7<> 69A1<> 70B7<> 70C5<> 52B7<
I2C_BUS0_CLK_MUX 69D5<>
```

```
I2C_BUS0_DAT    49C4<> 52B7<> 69A1<> 70B4<> 70C4<>
I2C_BUS0_DAT_MUX 69D6<>
I2C_BUS1_CLK    25C5<> 29B5<> 33C7<> 34C7<> 35C7<>
                36C7<> 37C7<> 38B5<> 69A1<> 70B7<>
I2C_BUS1_CLK_MUX 69C5<>
I2C_BUS1_DAT    25C5<> 29B5<> 33C7<> 34C7<> 35C7<>
                36C7<> 37C7<> 38B5<> 69A1<> 70B4<>
I2C_BUS1_DAT_MUX 69C6<>
I2C_BUS2_CLK    11C6<> 69A1<> 70B7<> 7C4<
I2C_BUS2_CLK_MUX 69B5<>
I2C_BUS2_DAT    7C4<> 11C6<> 69A1<> 70B4<>
I2C_BUS2_DAT_MUX 69C6<>
I2C_BUS3_CLK    16A4<> 17A3<> 20A4<> 21A4<> 51A4>
                69B1<> 70B7<>
I2C_BUS3_CLK_MUX 69B5<>
I2C_BUS3_DAT    16A4<> 17A3<> 20A4<> 21A4<> 51A4>
                69A1<> 70B4<>
I2C_BUS3_DAT_MUX 69B6<>
ICH3_A20GATE    52A5> 53C3> 39C3<
ICH3_A20M_N     9A6<> 39D3> 4D4<
ICH3_AD<31..0>  39D6<> 44A4<> 44A7<> 44C8> 45B7>
                45C7<>
ICH3_APICCLK    39B4<
ICH3_APICD0     39B4<>
ICH3_APICD1     39B4<>
ICH3_CBE0_N     39B7<> 44A8<> 45C7<>
ICH3_CBE1_N     39B7<> 44B4<> 45C7<>
ICH3_CBE2_N     39B7<> 44B4<> 45C7<>
ICH3_CBE3_N     39B7<> 44C4<> 45C7<>
ICH3_CLK14      51D6> 41D5<
ICH3_CLK33      51C8> 39B7<
ICH3_CLK48      51B4> 41D5<
ICH3_CLK66      51B4> 41D5<
ICH3_CPUPWRGD   9A6<> 39C3> 4D4<
ICH3_CPUSLP_N   9A6<> 39D3> 4D4<
ICH3_DEVSEL_N   39B7<> 44B2> 44B4<> 45B7<
ICH3_DPSLPUR    41B6<>
ICH3_DPSLP_N    9A6<> 39C3> 4D4<
ICH3_FERR_3V_N  39D4<
ICH3_FERR_N     4B6> 39D1<
ICH3_FRAME_N    39B7<> 44B8<> 44C2<> 45B7<
ICH3_GNT0_N     39A7> 44C7<
ICH3_GNTA_N     39A7> 42C5<
ICH3_GPIO12     40C6<
ICH3_HI<11..0>  11A7<> 39C3<>
ICH3_HICOMP     39B4<>
ICH3_HIREF      39B4<
ICH3_HITERM     39B4<
ICH3_IGNNE_N    9A6<> 39D3> 4D4<
ICH3_INIT_N     9A6<> 39C3> 4D4< 52B1<
ICH3_INTRUDER_N 70D5> 40C6<
ICH3_IRDY_N     39B7<> 44B2> 44B4<> 45B7<
ICH3_IRQ14      39B3<> 43A6>
ICH3_IRQ15      39B4<
ICH3_LAD<3..0>  40C2<> 52A5<> 52A7<> 52D3<> 53C7<>
                72A7<>
ICH3_LAN_RST_N  41C6<
ICH3_LDRQ0_N    52A8> 53C8> 40D2<
ICH3_LDRQ1_N    52A3> 40D2<
ICH3_LFRAME_N   40D2> 72A7<> 52A5< 52C6< 53C7<
ICH3_LINT0_INTR 9A6<> 39C3> 4D4<
ICH3_LINT1_NMI  39C3> 70B7<
ICH3_MAJOR_BOARD_REV_LSB 40A2> 40C6<
ICH3_MAJOR_BOARD_REV_MSB 40A2> 40A6<
ICH3_MCH_ID     40A8> 40C6<
ICH3_PAR        39B7<> 44B8<> 45B7<
ICH3_PCIRST_N   39A5> 43B8< 44C7< 45A7< 52A5< 52C6<
                53C7<
ICH3_PDA0       40C2> 43A6<
ICH3_PDA1       40C2> 43A6<
ICH3_PDA2       40C2> 43A4<
ICH3_PDCS1_N    40C2> 43A6<
ICH3_PDCS3_N    40C2> 43A4<
ICH3_PDD<15..0> 40C1<> 43A4<> 43A6<>
ICH3_PDDACK_N   40C2> 43A6<
ICH3_PDDREQ     43A6> 40C2<
ICH3_PDIOR_N    40C2> 43A6<
ICH3_PDIOW_N    40C2> 43A6<
ICH3_PERR_N     39B7<> 44B2> 44B4<>
ICH3_PIORDY     43A6> 40C2<
ICH3_PIRQA_N    25B5> 39B3<> 44C7> 44D2> 45C4>
ICH3_PIRQB_N    29B5> 39B3<> 44C4> 44D2>
ICH3_PIRQC_N    38B1<> 39B3<> 44C2> 44C7>
ICH3_PIRQD_N    39B3<> 44C4> 44D2>
ICH3_PIRQE_GPIO2 39B3<> 44D2<>
```

```
ICH3_PIRQF_GPIO3 39B3<> 44D2<>
ICH3_PIRQG_GPIO4 39B3<> 44D2<>
ICH3_PIRQH_GPIO5 39B3<> 44D2<>
ICH3_PLOCK_N    39B7<> 44B2> 44B4<>
ICH3_PME_N      33D7> 34D7> 35D7> 36D7> 37D7> 38C5>
                39B7<> 44CB> 52A7<>
ICH3_PSTRBF     11B6> 39B4<>
ICH3_PSTRBS     11B6> 39B4<>
ICH3_PWRBTN_N   41A6> 70C2> 41C5<
ICH3_RCIN_N     52A5> 53C3> 39C3<
ICH3_REQ0_N     44C2> 44C4> 39A7<
ICH3_REQ1_N     44C2<> 39A7<
ICH3_REQ2_N     44C2<> 39A7<
ICH3_REQ3_N     44C2<> 39A7<
ICH3_REQ4_N     44C2<> 39A7<
ICH3_RSMRST_N   48A6> 41C5<
ICH3_RTCRST_N   41C6<
ICH3_RTCX1      41B6> 41C6<
ICH3_RTCX2      41B8> 41C6<
ICH3_SAFE_MODE  42C5> 40B6<
ICH3_SERIRQ     39B3<> 52A7<> 53C6>
ICH3_SERR_N     39B7<> 44B2> 44B4> 45B7<
ICH3_SLP_S5_N   41C5> 70B7<
ICH3_SMBALERT_N_GPIO11 40C6<
ICH3_SMBCLK     40C6<> 69C8<>
ICH3_SMBDATA    40C6<> 69C8<>
ICH3_SMBUS_SEL0 40C6> 69C8<
ICH3_SMBUS_SEL1 40C6> 69C8<
ICH3_SMI_N      39C3> 70B7<
ICH3_SPKR       41B6> 42A5< 70D5<
ICH3_STOP_N     39B7<> 44B2> 44B8<> 45B7<
ICH3_STPCLK_N   9A6<> 39C2> 4D4<
ICH3_STPCLK_R_N 39C4<>
ICH3_SUSCLK     41C5> 53A3<
ICH3_THRM_N     40D6<
ICH3_TP0        41B6<
ICH3_TRDY_N     39B7<> 44B2> 44B8<> 45B7<
ICH3_USBP0N     40B6<> 43C3<>
ICH3_USBP0P     40B6<> 43C3<>
ICH3_USBP1N     40B6<> 43B3<>
ICH3_USBP1P     40B6<> 43B3<>
ICH3_USB_OC0_N  43D3> 40A6<
ICH3_USB_OC1_N  43C4> 40A6<
ICH3_USB_OC2_N  40A6<
ICH3_USB_OC3_N  40B6<
ICH3_USB_OC4_N  40B6<
ICH3_USB_OC5_N  40B6<
ICH3_USB_RBIAS  40A6<
ICH3_VBIAS      41B6<
ICH3_VCC_RTC    41C7> 40D6<
ICH3_VRMPWRGD   68D1> 41C5<
IDE_PRI_CBL_DET 43A4<> 40C6<
IDE_PRI_RST_N   43B6<
INDEX_N         54A2> 53C6<
ITP_BCLK0       51D1> 9C4<
ITP_BCLK0_CPU   51D1> 4C4<
ITP_BCLK0_R     51C5<>
ITP_BCLK1       51D1> 9C4<
ITP_BCLK1_CPU   51D1> 4C4<
ITP_BCLK1_R     51C5<>
ITP_BPM<?..?>   4A5> 9C4>
ITP_DBRST_N     9C4> 4C2< 48A4<
ITP_TCK_P       9C4> 9D4> 4A6<
ITP_TDI_P       9D4> 4A5<
ITP_TDO_P       4A6> 9D4<
ITP_TMS_P       9D4> 4A6<
ITP_TRST_N      9D4> 4A6<
JTAG_TCK        56A2<
JTAG_TMS        56A2<
KBCLK           53C3<> 54C8<
KBDATA          53C3<> 54D8<
LAN_AGND        57C5> 58A3< 58B1<
LAN_IDSEL       56C6<
LED_LAD0        72A6<>
LED_LAD1        72A6<>
LED_LAD2        72A6<>
LED_LAD3        72A6<>
LED_LFRAME_N    72A6<>
LINK100_N       56B1> 58B3<
LINK1000_N      56B1> 58B3<
LINK_ACT_N      56B1> 58C3<
LINK_UP_N       56B1> 58C3<
LODRV           47D4<
LPC_CLK14       51D6> 52A5<
LPC_CLK33       51C8> 52A7< 72B6<
```

```
LPC_CLKRUN_N    52A7<
LPC_LDRQ0_N     52A7<
LPC_LDRQ1_N     52A5<
LPC_SMI_N       52A5> 53C2> 39A7<
LPC_SUS_STAT_N  53C8> 52A7<
LPT_ACK_N       54A7> 53B3<
LPT_ALF_N       53B3> 54B7<
LPT_ALF_N_R     54B6<
LPT_BUSY        54A7> 53B3<
LPT_ERROR_N     54A7> 53B3<
LPT_INIT_N      53B3> 54B7<
LPT_INIT_N_R    54B6<
LPT_PD0         53B3<> 54B7<>
LPT_PD0_R       54B6<
LPT_PD1         53B3<> 54B7<>
LPT_PD1_R       54B6<
LPT_PD2         53B3<> 54B7<>
LPT_PD2_R       54B6<
LPT_PD3         53B3<> 54A7<>
LPT_PD3_R       54A6<
LPT_PD4         53B3<> 54A7<>
LPT_PD4_R       54A6<
LPT_PD5         53B3<> 54A7<>
LPT_PD5_R       54A6<
LPT_PD6         53B3<> 54A7<>
LPT_PD6_R       54A6<
LPT_PD7         53B3<> 54A7<>
LPT_PE          54A7> 53B3<
LPT_SELECTIN_N_R 54B6<
LPT_SLCT        54A7> 53B3<
LPT_SLCTIN_N    53B3> 54B7<
LPT_STROBE_N    53B3> 54B7<
LPT_STROBE_N_R  54B6<
LPT_V5_0        54B7<
LTP_PD7_R       54A6<
LVACKAM         60C5<> 64B6<> 65C4>
LVACKAP         60C7<> 64B7<> 65C5>
LVACKBM         60B1<> 64B2<> 66C4>
LVACKBP         60B4<> 64B3<> 66C5>
LVATNAM         60C5<> 64B6<> 65C4>
LVATNAP         60C7<> 64B7<> 65C5>
LVATNBM         60B1<> 64B2<> 66C4>
LVATNBP         60B4<> 64B3<> 66C5>
LVBSYAM         60C5<> 64B6<> 65C4>
LVBSYAP         60C7<> 64B7<> 65C5>
LVBSYBM         60B1<> 64B2<> 66C4>
LVBSYBP         60B4<> 64B3<> 66C5>
LVCDAM          60B5<> 64B6<> 65C6>
LVCDAP          60B7<> 64B7<> 65C8>
LVCDBM          60B1<> 64B2<> 66C6>
LVCDBP          60B4<> 64B3<> 66C8>
LVIOAM          60B5<> 64B6<> 65C6>
LVIOAP          60B7<> 64B7<> 65C8>
LVIOBM          60B1<> 64B2<> 66C6>
LVIOBP          60B4<> 64B3<> 66C8>
LVMSGAM         60B5<> 64B6<> 65B6>
LVMSGAP         60B7<> 64B7<> 65B8>
LVMSGBM         60B1<> 64B2<> 66B6>
LVMSGBP         60B4<> 64B3<> 66B8>
LVREQAM         60B5<> 64B6<> 65C6>
LVREQAP         60B7<> 64B7<> 65C8>
LVREQBM         60B1<> 64B2<> 66C6>
LVREQBP         60B4<> 64B3<> 66C8>
LVRSTAM         60B5<> 64B6<> 65C4>
LVRSTAP         60B7<> 64B7<> 65C5>
LVRSTBM         60B1<> 64B2<> 66C4>
LVRSTBP         60B4<> 64B3<> 66C5>
LVSCDAM0        60C5<> 64C6<> 65C1>
LVSCDAM1        60C5<> 64C6<> 65C1>
LVSCDAM2        60C5<> 64C6<> 65C1>
LVSCDAM3        60C5<> 64B6<> 65C1>
LVSCDAM4        60C5<> 64B6<> 65B4>
LVSCDAM5        60C5<> 64B6<> 65C4>
LVSCDAM6        60C5<> 64B6<> 65C4>
LVSCDAM7        60C5<> 64B6<> 65C4>
LVSCDAM8        60C5<> 64B6<> 65C6>
LVSCDAM9        60C5<> 64A6<> 65C6>
LVSCDAM10       60C5<> 64A6<> 65C6>
LVSCDAM11       60C5<> 64A6<> 65C6>
LVSCDAM12       60C5<> 64C6<> 65B1>
LVSCDAM13       60C5<> 64C6<> 65C1>
LVSCDAM14       60C5<> 64C6<> 65C1>
LVSCDAM15       60C5<> 64C6<> 65C1>
LVSCDAP0        60C7<> 64C7<> 65C3>
LVSCDAP1        60C7<> 64C7<> 65C3>
```

DRAWING

PAGE	REV
74	A2.1

LVSCDAP2 60C7<> 64C7<> 65C3>
LVSCDAP3 60C7<> 64B7<> 65C3>
LVSCDAP4 60C7<> 64B7<> 65B5>
LVSCDAP5 60C7<> 64B7<> 65C5>
LVSCDAP6 60C7<> 64B7<> 65C5>
LVSCDAP7 60C7<> 64B7<> 65C5>
LVSCDAP8 60C7<> 64B7<> 65C8>
LVSCDAP9 60C7<> 64A7<> 65C8>
LVSCDAP10 60C7<> 64A7<> 65C8>
LVSCDAP11 60C7<> 64A7<> 65C8>
LVSCDAP12 60C7<> 64C7<> 65B3>
LVSCDAP13 60C7<> 64C7<> 65C3>
LVSCDAP14 60C7<> 64C7<> 65C3>
LVSCDAP15 60C7<> 64C7<> 65C3>
LVSCDAPHM 60C5<> 64C6<> 65C1>
LVSCDAPHP 60C7<> 64C7<> 65C3>
LVSCDAPLM 60C5<> 64B6<> 65C4>
LVSCDAPLP 60C7<> 64B7<> 65C5>
LVSCDBM0 60C1<> 64C2<> 66C1>
LVSCDBM1 60C1<> 64C2<> 66C1>
LVSCDBM2 60C1<> 64C2<> 66C1>
LVSCDBM3 60C1<> 64B2<> 66C1>
LVSCDBM4 60C1<> 64B2<> 66B4>
LVSCDBM5 60C1<> 64B2<> 66C4>
LVSCDBM6 60C1<> 64B2<> 66C4>
LVSCDBM7 60C1<> 64B2<> 66C4>
LVSCDBM8 60C1<> 64B2<> 66C6>
LVSCDBM9 60C1<> 64A2<> 66C6>
LVSCDBM10 60C1<> 64A2<> 66C6>
LVSCDBM11 60C1<> 64A2<> 66C6>
LVSCDBM12 60C1<> 64C2<> 66B1>
LVSCDBM13 60C1<> 64C2<> 66C1>
LVSCDBM14 60C1<> 64C2<> 66C1>
LVSCDBM15 60C1<> 64C2<> 66C1>
LVSCDBP0 60C4<> 64C3<> 66C3>
LVSCDBP1 60C4<> 64C3<> 66C3>
LVSCDBP2 60C4<> 64C3<> 66C3>
LVSCDBP3 60C4<> 64B3<> 66C3>
LVSCDBP4 60C4<> 64B3<> 66B5>
LVSCDBP5 60C4<> 64B3<> 66C5>
LVSCDBP6 60C4<> 64B3<> 66C5>
LVSCDBP7 60C4<> 64B3<> 66C5>
LVSCDBP8 60C4<> 64B3<> 66C8>
LVSCDBP9 60C4<> 64A3<> 66C8>
LVSCDBP10 60C4<> 64A3<> 66C8>
LVSCDBP11 60C4<> 64A3<> 66C8>
LVSCDBP12 60C4<> 64C3<> 66B3>
LVSCDBP13 60C4<> 64C3<> 66C3>
LVSCDBP14 60C4<> 64C3<> 66C3>
LVSCDBP15 60C4<> 64C3<> 66C3>
LVSCDBPHM 60B1<> 64C2<> 66C1>
LVSCDBPHP 60B4<> 64C3<> 66C3>
LVSCDBPLM 60B1<> 64B2<> 66C4>
LVSCDBPLP 60B4<> 64B3<> 66C5>
LVSELAM 60B5<> 64B6<> 65C6>
LVSELAP 60B7<> 64B7<> 65C8>
LVSELBM 60B1<> 64B2<> 66C6>
LVSELBP 60B4<> 64B3<> 66C8>
LVTRMPWR_A 64D5> 62A1< 65D5<
LVTRMPWR_B 64D2> 62A3< 66D5<
MCH_AP_0_N 6B7> 10A6<
MCH_AP_1_N 6B7> 10A6<
MCH_A_N<35..32> 6C2> 10C6<
MCH_BINIT_N 6B2> 10A6<
MCH_CLK66 51B4> 11B6<
MCH_DP_N<3..0> 6C6> 10A6<
MCH_GTL_VREF 10D3<
MCH_RSP_N 6B2> 10C6<
MCH_XERR_N 6B2> 10A6<
MCH_XORMODE_N 10D6<
MDI1 56A2<> 58B8<>
MDI1_N 56A2<> 58B8<>
MDI2 56A2<> 58B8<>
MDI2_N 56A2<> 58B8<>
MDI3 56A2<> 58B8<>
MDI3_N 56A2<> 58B8<>
MDIO 56A2<> 58B8<>
MDIO_N 56A2<> 58B8<>
MSCLK 53C3<> 54C8<
MSDATA 53C3<> 54C8<
MTRO_N 53D6> 54A2<
P64H2_1_APICD0 25B5<>
P64H2_1_APICD1 25B5<>
P64H2_1_CK200 25C5<
P64H2_1_CK200_N 25C5<

P64H2_1_CLK66 51B8> 25C5<
P64H2_1_HI16 11B3<> 25C2<
P64H2_1_HI17 11B3<> 25C2>
P64H2_1_HI18 11B3<> 25C2<>
P64H2_1_HI20 11A3<> 25C2>
P64H2_1_HI21 11A3<> 25C2>
P64H2_1_HI<?..?> 11A2<> 25B1<>
P64H2_1_HPA_SID 25A5<
P64H2_1_HPA_SLOT0 25B5<
P64H2_1_HPA_SLOT1 25B5<
P64H2_1_HPA_SLOT2 25B5<
P64H2_1_HPB_SID 25A3<
P64H2_1_HPB_SLOT0 25B3<
P64H2_1_HPB_SLOT1 25B3<
P64H2_1_HPB_SLOT2 25B3<
P64H2_1_PA_133EN 23D5<
P64H2_1_PA_ACK64_N 31B6<> 33B3<> 23D4<
P64H2_1_PA_AD<63..0> 23D7<> 31A7<> 33A2<> 33A7<>
33C7<>
P64H2_1_PA_CBE0_N 23B4<> 33B7<>
P64H2_1_PA_CBE1_N 23B4<> 33B2<>
P64H2_1_PA_CBE2_N 23B4<> 33C2<>
P64H2_1_PA_CBE3_N 23B4<> 33C3<>
P64H2_1_PA_CBE4_N 23B4<> 31D8<> 33A3<>
P64H2_1_PA_CBE5_N 23B4<> 31D8<> 33A7<>
P64H2_1_PA_CBE6_N 23B4<> 31D8<> 33A3<>
P64H2_1_PA_CBE7_N 23B4<> 31D8<> 33B7<>
P64H2_1_PA_DEVSEL_N 23C4<> 31B6<> 33C2<>
P64H2_1_PA_FRAME_N 23C4<> 31B6<> 33C7<>
P64H2_1_PA_GNT0_N 23C4> 33D7<
P64H2_1_PA_GNT3_N 23C5<>
P64H2_1_PA_GNT4_N 23C4> 25B8<>
P64H2_1_PA_GNT5_N 23C4> 25B8<>
P64H2_1_PA_IRDY_N 23C4<> 31B6<> 33C2<>
P64H2_1_PA_IRQ0 31C6<> 33D6> 23A4<
P64H2_1_PA_IRQ1 31C6<> 33D3> 23A4<
P64H2_1_PA_IRQ2 31D6<> 33D6> 23A4<
P64H2_1_PA_IRQ3 31D6<> 33D3> 23A4<
P64H2_1_PA_IRQ4 31D6<> 23A4<
P64H2_1_PA_IRQ5 31D6<> 23A4<
P64H2_1_PA_IRQ6 31C6<> 23A4<
P64H2_1_PA_IRQ7 31A6<> 23A4<
P64H2_1_PA_IRQ8 31C6<> 23A4<
P64H2_1_PA_IRQ9 31C6<> 23A4<
P64H2_1_PA_IRQ10 31C6<> 23A4<
P64H2_1_PA_IRQ11 31A6<> 23A4<
P64H2_1_PA_IRQ12 31A6<> 23A4<
P64H2_1_PA_IRQ13 31A6<> 23A4<
P64H2_1_PA_IRQ14 31A6<> 23B4<
P64H2_1_PA_IRQ15 31A6<> 23B4<
P64H2_1_PA_M66EN 31A6<> 33B3> 23D1<
P64H2_1_PA_PAR 23C4<> 33B7<>
P64H2_1_PA_PAR64 23C4<> 31B6<> 33A7<>
P64H2_1_PA_PCIXCAP 33C2<> 23D1<
P64H2_1_PA_PCLK0 23B3> 33D3<
P64H2_1_PA_PCLK0_R 23B5<>
P64H2_1_PA_PCLK6 23B5<>
P64H2_1_PA_PCLKI 23B5<
P64H2_1_PA_PERR_N 23C4<> 31B6<> 33C2<>
P64H2_1_PA_PLOCK_N 23A4<> 31B6<> 33C2<>
P64H2_1_PA_REQ0_N 31B6<> 23C4< 33D3<
P64H2_1_PA_REQ1_N 31A6<> 23C4<
P64H2_1_PA_REQ2_N 31A6<> 23C4<
P64H2_1_PA_REQ3_N 31A6<> 23C4<
P64H2_1_PA_REQ4_N 31A6<> 23C4<
P64H2_1_PA_REQ5_N 31C6<> 23C4<
P64H2_1_PA_REQ64_N 23D4<> 31B6<> 33B7<>
P64H2_1_PA_RST_N 23B4<> 33D7<
P64H2_1_PA_SERR_N 31B6<> 33C2<> 23C4<
P64H2_1_PA_STOP_N 23C4<> 31B6<> 33C7<>
P64H2_1_PA_TRDY_N 23C4<> 31B6<> 33C7<>
P64H2_1_PB_ACK64_N 24D4<> 31B2<> 34B3<> 56B6<>
P64H2_1_PB_AD<63..0> 24D6<> 31A3<> 34A2<> 34A7<>
34C7<> 56D6<> 56D7<>
P64H2_1_PB_CBE0_N 24B4<> 34B7<> 56C6<>
P64H2_1_PB_CBE1_N 24B4<> 34B3<> 56C6<>
P64H2_1_PB_CBE2_N 24B4<> 34C3<> 56C6<>
P64H2_1_PB_CBE3_N 24C4<> 34C3<> 56C6<>
P64H2_1_PB_CBE4_N 24C4<> 31B2<> 34A3<> 56C6<>
P64H2_1_PB_CBE5_N 24C4<> 31B2<> 34A7<> 56C6<>
P64H2_1_PB_CBE6_N 24C4<> 31D4<> 34A3<> 56C6<>
P64H2_1_PB_CBE7_N 24C4<> 31D4<> 34B7<> 56C6<>
P64H2_1_PB_DEVSEL_N 24C4<> 34C3<> 44A2> 56C6<>
P64H2_1_PB_FRAME_N 24C4<> 31C2<> 34C7<> 56C6<>
P64H2_1_PB_GNT0_N 24C4> 56B6<

P64H2_1_PB_GNT1_N 24D4> 34D7<
P64H2_1_PB_GNT3_N 24D5<>
P64H2_1_PB_GNT4_N 24D4> 25B8<>
P64H2_1_PB_GNT5_N 24D4<> 25B8<>
P64H2_1_PB_IRDY_N 24C4<> 31C2<> 34C3<> 56C6<>
P64H2_1_PB_IRQ0 31C6<> 56B6<> 24A4<
P64H2_1_PB_IRQ1 31C2<> 24A4<
P64H2_1_PB_IRQ2 31C2<> 24A4<
P64H2_1_PB_IRQ3 31D2<> 24A4<
P64H2_1_PB_IRQ4 31D2<> 34D6> 24A4<
P64H2_1_PB_IRQ5 31C2<> 34D3> 24A4<
P64H2_1_PB_IRQ6 31C2<> 34D6> 24A4<
P64H2_1_PB_IRQ7 31C2<> 34D3> 24A4<
P64H2_1_PB_IRQ8 31C2<> 24A4<
P64H2_1_PB_IRQ9 31D2<> 24B4<
P64H2_1_PB_IRQ10 31A2<> 24B4<
P64H2_1_PB_IRQ11 31B2<> 24B4<
P64H2_1_PB_IRQ12 31D2<> 24B4<
P64H2_1_PB_IRQ13 31C2<> 24B4<
P64H2_1_PB_IRQ14 31A6<> 24B4<
P64H2_1_PB_IRQ15 31B2<> 24B4<
P64H2_1_PB_LAN_RST_N 56A7<
P64H2_1_PB_M66EN 31A2<> 34B3> 24D2< 56B5<
P64H2_1_PB_PAR 24C4<> 34B7<> 56C6<>
P64H2_1_PB_PAR64 24C4<> 31D4<> 34A7<> 56C6<>
P64H2_1_PB_PCIXCAP 34C3<> 24D1<
P64H2_1_PB_PCLK0 24B2> 56B6<
P64H2_1_PB_PCLK0_R 24B5<>
P64H2_1_PB_PCLK1 24B2> 34D3<
P64H2_1_PB_PCLK1_R 24B5<>
P64H2_1_PB_PCLK6 24B5<>
P64H2_1_PB_PCLKI 24B5<
P64H2_1_PB_PERR_N 24C4<> 31A2<> 34C3<> 56C1<>
P64H2_1_PB_PLOCK_N 24A4> 31A2<> 34C3<> 56B6<
P64H2_1_PB_REQ0_N 31A4<> 56B6<> 24C4<
P64H2_1_PB_REQ1_N 44C2<> 24C4< 34D3<
P64H2_1_PB_REQ2_N 31B2<> 24C4<
P64H2_1_PB_REQ3_N 31A2<> 24C4<
P64H2_1_PB_REQ4_N 31A2<> 24C4<
P64H2_1_PB_REQ5_N 31D2<> 24C4<
P64H2_1_PB_REQ64_N 31D4<> 34B7<> 56B6<> 24D4<
P64H2_1_PB_RST_N 24B4> 34D7< 56A6<
P64H2_1_PB_SERR_N 24C4<> 34C3<> 44A2> 56C1<>
P64H2_1_PB_STOP_N 24C4<> 31B2<> 34C7<> 56C6<>
P64H2_1_PB_TRDY_N 24C4<> 31C2<> 34C7<> 56C6<>
P64H2_1_PSTRBF 11B3<> 25C2<>
P64H2_1_PSTRBS 11B3<> 25C2<>
P64H2_1_PUSTRBF 11B3<> 25C2<>
P64H2_1_PUSTRBS 11B3<> 25C2<>
P64H2_1_RASERR_N 25C6> 70B4<
P64H2_1_RCOMP 25C3<>
P64H2_1_TEST_N 25B5<
P64H2_1_VREF 25C2<
P64H2_1_VSWING 25C2<
P64H2_2_APICCLK 29B5<
P64H2_2_APICD0 29B5<>
P64H2_2_APICD1 29B5<>
P64H2_2_CK200 29C5<
P64H2_2_CK200_N 29C5<
P64H2_2_CLK66 51B8> 29C5<
P64H2_2_HI16 11D7<> 29C2<
P64H2_2_HI17 11D7<> 29C2>
P64H2_2_HI18 11D7<> 29C2<>
P64H2_2_HI20 11D6<> 29C2>
P64H2_2_HI21 11D6<> 29C2>
P64H2_2_HI<?..?> 11D7<> 29B2<>
P64H2_2_HPA_SID 29A5<
P64H2_2_HPA_SLOT0 29A5<
P64H2_2_HPA_SLOT1 29A5<
P64H2_2_HPA_SLOT2 29B5<
P64H2_2_HPB_SID 29A3<
P64H2_2_HPB_SLOT0 29A3<
P64H2_2_HPB_SLOT1 29A3<
P64H2_2_HPB_SLOT2 29B3<
P64H2_2_PA_133EN 27D5<
P64H2_2_PA_ACK64_N 32A6<> 59D3<> 27D4<
P64H2_2_PA_AD<?..?> 27D7<> 32A6<> 59A6<> 59D8>
P64H2_2_PA_CBE0_N 27B4<> 59C3<>
P64H2_2_PA_CBE1_N 27B4<> 59C3<>
P64H2_2_PA_CBE2_N 27B4<> 59C3<>
P64H2_2_PA_CBE3_N 27B4<> 59C3<>
P64H2_2_PA_CBE4_N 27C4<> 32B6<> 59C3<>
P64H2_2_PA_CBE5_N 27C4<> 32B6<> 59C3<>
P64H2_2_PA_CBE6_N 27C4<> 32B6<> 59C3<>
P64H2_2_PA_CBE7_N 27C4<> 32C8<> 59C3<>

P64H2_2_PA_DEVSEL_N 27C4<> 32B6<> 59C3<>
P64H2_2_PA_FRAME_N 27C4<> 32B6<> 59D3<>
P64H2_2_PA_GNT0_N 27C4> 59D6<
P64H2_2_PA_GNT3_N 27D5<>
P64H2_2_PA_GNT4_N 27D4> 29D8<>
P64H2_2_PA_GNT5_N 27D4> 29D8<>
P64H2_2_PA_IRDY_N 27C4<> 32D8<> 59D3<>
P64H2_2_PA_IRQ0 32A2<> 59D3> 27A4<
P64H2_2_PA_IRQ1 32B6<> 59D3> 27A4<
P64H2_2_PA_IRQ2 32A2<> 27A4<
P64H2_2_PA_IRQ3 32B6<> 27A4<
P64H2_2_PA_IRQ4 32A2<> 27A4<
P64H2_2_PA_IRQ5 32B6<> 27A4<
P64H2_2_PA_IRQ6 32B6<> 27A4<
P64H2_2_PA_IRQ7 32A6<> 27A4<
P64H2_2_PA_IRQ8 32C6<> 27A4<
P64H2_2_PA_IRQ9 32C6<> 27A4<
P64H2_2_PA_IRQ10 32C6<> 27B4<
P64H2_2_PA_IRQ11 32C6<> 27B4<
P64H2_2_PA_IRQ12 32C6<> 27B4<
P64H2_2_PA_IRQ13 32C6<> 27B4<
P64H2_2_PA_IRQ14 32C6<> 27B4<
P64H2_2_PA_IRQ15 32C6<> 27B4<
P64H2_2_PA_M66EN 27D3<> 32A6<>
P64H2_2_PA_PAR 27C4<> 59C3<>
P64H2_2_PA_PAR64 27C4<> 32C8<> 59D3<>
P64H2_2_PA_PCIXCAP 27D5<
P64H2_2_PA_PCLK0 27B3> 59D6<
P64H2_2_PA_PCLK0_R 27B5<>
P64H2_2_PA_PCLK6 27B5<>
P64H2_2_PA_PCLKI 27B5<
P64H2_2_PA_PERR_N 27C4<> 32D8<> 59C3<>
P64H2_2_PA_PLOCK_N 27A4<> 32D8<>
P64H2_2_PA_REQ0_N 32A6<> 59D3> 27C4<
P64H2_2_PA_REQ1_N 32A6<> 27C4<
P64H2_2_PA_REQ2_N 32A6<> 27C4<
P64H2_2_PA_REQ3_N 32A6<> 27C4<
P64H2_2_PA_REQ4_N 32A6<> 27C4<
P64H2_2_PA_REQ5_N 32A6<> 27C4<
P64H2_2_PA_REQ64_N 27D4<> 32C8<> 59D3<>
P64H2_2_PA_RST_N 27B4> 60A7<
P64H2_2_PA_SERR_N 32B6<> 59C3<> 27C4<
P64H2_2_PA_STOP_N 27C4<> 32D8<> 59C3<>
P64H2_2_PA_TRDY_N 27C4<> 32B6<> 59C3<>
P64H2_2_PB_133EN 28D5<
P64H2_2_PB_ACK64_N 28D4<> 32A2<> 35B3<> 36B3<>
37B3<> 38A8<>
P64H2_2_PB_AD<63..0> 28D7<> 32A3<> 35A2<> 35A7<>
35C7<> 36A2<> 36A7<> 36C7<> 37A2<>
37A7<> 37C7<> 38A5<> 38A7<> 38C1<>
38C4<> 38C4<
P64H2_2_PB_CBE0_N 28B4<> 35B7<> 36B7<> 37B7<>
38B5<>
P64H2_2_PB_CBE1_N 28B4<> 35B3<> 36B3<> 37B3<>
38B8<>
P64H2_2_PB_CBE2_N 28B4<> 35C3<> 36C3<> 37C3<>
38C8<>
P64H2_2_PB_CBE3_N 28B4<> 35C3<> 36C3<> 37C3<>
38C8<>
P64H2_2_PB_CBE4_N 28B4<> 32D4<> 35A3<> 36A3<>
37A3<> 38D3<>
P64H2_2_PB_CBE5_N 28B4<> 32D4<> 35A7<> 36A7<>
37A7<> 38D1<>
P64H2_2_PB_CBE6_N 28C4<> 32D4<> 35A3<> 36A3<>
37A3<> 38D3<>
P64H2_2_PB_CBE7_N 28C4<> 32D4<> 35B7<> 36B7<>
37B7<> 38D1<>
P64H2_2_PB_DEVSEL_N 28C4<> 32B2<> 35C3<> 36C3<>
37C3<> 38B8<>
P64H2_2_PB_FRAME_N 28C4<> 32B2<> 35C7<> 36C7<>
37C7<> 38C5<>
P64H2_2_PB_GNT0_N 28C4> 35D7<
P64H2_2_PB_GNT1_N 28C4> 36D7<
P64H2_2_PB_GNT2_N 28C4> 37D7<
P64H2_2_PB_GNT3_N 28C3> 38C5<
P64H2_2_PB_GNT4_N 28D4> 29D8<>
P64H2_2_PB_GNT5_N 28D4> 29D8<>
P64H2_2_PB_IRDY_N 28C4<> 32B2<> 35C3<> 36C3<>
37C3<> 38B8<>
P64H2_2_PB_IRQ0 32C2<> 35D6> 28A4<
P64H2_2_PB_IRQ1 32C2<> 35D3> 28A4<
P64H2_2_PB_IRQ2 32C2<> 35D6> 28A4<
P64H2_2_PB_IRQ3 32C2<> 35D3> 28A4<
P64H2_2_PB_IRQ4 32C2<> 35D6> 28A4<
P64H2_2_PB_IRQ5 32C2<> 35D3> 28A4<

P64H2_2_PB_IRQ6 32C2<> 36D6> 28A4<
P64H2_2_PB_IRQ7 32C2<> 36D3> 28A4<
P64H2_2_PB_IRQ8 32C2<> 37D6> 28A4<
P64H2_2_PB_IRQ9 32C2<> 37D3> 28A4<
P64H2_2_PB_IRQ10 32C2<> 37D6> 28A4<
P64H2_2_PB_IRQ11 32C2<> 37D3> 28A4<
P64H2_2_PB_IRQ12 32D2<> 38D5> 28B4<
P64H2_2_PB_IRQ13 32D2<> 38D8> 28B4<
P64H2_2_PB_IRQ14 32D2<> 38D5> 28B4<
P64H2_2_PB_IRQ15 32D2<> 38D8> 28B4<
P64H2_2_PB_M66EN 28D2<> 32A6<> 35B2> 36B2> 37B2>
38B8>
P64H2_2_PB_PAR 28C4<> 35B7<> 36B7<> 37B7<> 38B5<>
P64H2_2_PB_PAR64 28C4<> 32A2<> 35A7<> 36A7<> 37A7<>
38D1<>
P64H2_2_PB_PCIXCAP 28D2<> 35C3<> 36C3<> 37C3<>
38B8<>
P64H2_2_PB_PCLK0 28B1> 35D3<
P64H2_2_PB_PCLK0_R 28B5<>
P64H2_2_PB_PCLK1 28B1> 36D3<
P64H2_2_PB_PCLK1_R 28B5<>
P64H2_2_PB_PCLK2 28B1> 37D3<
P64H2_2_PB_PCLK2_R 28B5<>
P64H2_2_PB_PCLK3 28B1> 38C8<
P64H2_2_PB_PCLK3_R 28B5<>
P64H2_2_PB_PCLK6 28B5<>
P64H2_2_PB_PCLKI 28B5<
P64H2_2_PB_PERR_N 28C4<> 32B2<> 35C3<> 36C3<>
37C3<> 38B8<>
P64H2_2_PB_PLOCK_N 28A4> 32B2<> 35C3<> 36C3<>
37C3<> 38B8<>
P64H2_2_PB_REQ0_N 32A2<> 28C4< 35D3<
P64H2_2_PB_REQ1_N 32C6<> 28C4< 36D3<
P64H2_2_PB_REQ2_N 32C6<> 28C4< 37D3<
P64H2_2_PB_REQ3_N 32A2<> 28C4< 38C8<
P64H2_2_PB_REQ4_N 32C6<> 28C4<
P64H2_2_PB_REQ5_N 32A2<> 28C4<
P64H2_2_PB_REQ64_N 32B2<> 35B7<> 36B7<> 37B7<>
38A5<> 28D4<
P64H2_2_PB_RST_N 28B4<> 35D7< 36D7< 37D7< 38C5<
P64H2_2_PB_SERR_N 32B2<> 35C3<> 36C3<> 37C3<>
38B8<> 28C4<
P64H2_2_PB_STOP_N 28C4<> 32B2<> 35C7<> 36C7<>
37C7<> 38B5<>
P64H2_2_PB_TRDY_N 28C4<> 32B2<> 35C7<> 36C7<>
37C7<> 38B5<>
P64H2_2_PSTRBF 11C6<> 29C2<>
P64H2_2_PSTRBS 11C6<> 29C2<>
P64H2_2_PUSTRBF 11C6<> 29C2<>
P64H2_2_PUSTRBS 11C6<> 29C2<>
P64H2_2_RASERR_N 29C6> 70B7<
P64H2_2_RCOMP 29C3<>
P64H2_2_TEST_N 29B5<
P64H2_2_VREF 29C3<
P64H2_2_VSWING 29C3<
PCI33_ACK64_N 31B2<> 44A4<>
PCI33_CLK33 51C8> 44C4<
PCI33_CLKRUN_N 44C7<
PCI33_IDSEL 44C7<
PCI33_PME_N 44C7<
PCI33_PRSNT1 44C5<
PCI33_PRSNT2 44C5<
PCI33_REQ64_N 31B2<> 44A8<>
PCI33_SBO_N 44B2> 44B8<>
PCI33_SDONE 44B2> 44B8<>
PCI33_TDI 44A2> 44C7<>
PCI33_TMS 44A2> 44D7<>
PCI33_VAUX 44C7<
PCIRST2_5_N 39A5> 11B8< 16A4< 17A3< 20A4< 21A4<

PCIRST_2_N 39A7> 25B5< 29B5< 38B3< 72B6< 72C3<

PCI_SLOTS_TCK 33D2<> 34D3<> 35D3<> 36D3<> 37D3<>
38D7<> 44D4<>
PCI_SLOTS_TRST_N 33D8<> 34D6<> 35D6<> 36D6<> 37D6<>
38D5<> 44D7<>
PME_N 56B7<>
PORT_OPTION 72B3<>
PS_ON_N 49B3> 70A7<
PS_PWRGD 49C7> 70B4<
PS_PWRGD_SYS 70B7> 48A4< 49A3<
PWROK_0 48A3<
PWROK_RST_N 48A5<> 70C2>
RC5051_ENABLE 47D8<
RDATA_N 54A2> 53C6<

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RJ45_P10	58A2<
RJ45_P12	58A2<
RTCRST_PD	41D8<
RTCRST_PU	41C7<
R_ICH3_INIT_N	52B2<
SCSI_AGND	62B3> 62C3> 62C7> 63C4<
SCSI_CORE_VCC	63B2> 61D8< 62D1<
SCSI_CORE_VCCA	62C4<
SCSI_CORE_VCCA_PX	62D4<
SCSI_IDESL	59D6<
SCSI_SEECK	59A4<>
SCSI_SEECS	59C3<>
SCSI_SEEDI	59A4<>
SCSI_SEEDO	59A4<>
SCSI_V3_3A_0	62B4<
SCSI_V3_3A_1	62B4<
SCSI_V3_3A_PX	62C4<
SCSI_VCC	63B6> 61C5<
SER_CTS	54C3<
SER_DCD	54C3<
SER_DSR	54C3<
SER_DTR	54C3<>
SER_RI	54C3<
SER_RTS	54C3<>
SER_RXD	54C3<
SER_TXD	54C3<>
SIOCLKRUN	53C4<>
SIO_CLK33	51C8> 53C6<
SIO_LDRQ0_N	53C6<>
SIO_PME_N	39A7<> 53C8<>
SLOT_1A_3VAUX	33D6<
SLOT_1A_IDSEL	33C6<
SLOT_1A_PME_N	33D7<
SLOT_1A_TDI	33D6<
SLOT_1A_TMS	33D6<
SLOT_1B_3VAUX	34D6<
SLOT_1B_IDSEL	34C6<
SLOT_1B_PME_N	34D6<
SLOT_1B_TDI	34D6<
SLOT_1B_TMS	34D6<
SLOT_2A_3VAUX	35D6<
SLOT_2A_IDSEL	35C6<
SLOT_2A_PME_N	35D6<
SLOT_2A_TDI	35D6<
SLOT_2A_TMS	35D6<
SLOT_2B_3VAUX	36D6<
SLOT_2B_IDSEL	36C6<
SLOT_2B_PME_N	36D6<
SLOT_2B_TDI	36D6<
SLOT_2B_TMS	36D6<
SLOT_2C_3VAUX	37D6<
SLOT_2C_IDSEL	37C6<
SLOT_2C_PME_N	37D6<
SLOT_2C_TDI	37D6<
SLOT_2C_TMS	37D6<
SLOT_2D_3VAUX	38C5<>
SLOT_2D_IDSEL	38C5<>
SLOT_2D_PME_N	38C5<>
SLOT_2D_TDI	38D5<>
SLOT_2D_TMS	38D5<>
SMC_SYS0PT	53C4<>
STEP_N	53D6> 54A2<
SYS_PWROK_1	48B1> 10A6< 56B6<
SYS_PWROK_2	48A1> 25B5< 29B5< 41C5<
SYS_SLP_S5_N	70B4> 49B5< 69A7<
TBI_MODE	56C2<
THERM_EN	7B3> 49A5<
THERM_EN_SBY	7B5<>
THRMTRP_LTCH	7B6<
TRK0_N	54A2> 53C6<
V1_2SENSE_N	55B3<
V1_2SENSE_P	55B3<
V1_8SENSE_M	48C6<
V1_8SENSE_P	48C6<
V2_5SENSE1_M	47A3<
V2_5SENSE1_P	47A3<
V2_5SENSE2_M	47A5<
V2_5SENSE2_P	47A5<
V2_5_L1	47B3<
V2_5_L2	47A4<
V3_CLK	51A4> 51B4> 51A6< 51B4<
V3_CLK_A	51A2> 51C4<
V3_OK	7B5<
V5_KB	54D6<
V5_KB_RT	54D7<

VCC1_2_L	55B3<
VCC1_8_L	48D6<
VCCA1_2	14A5<
VCCACPU1_2	14A6<
VCCAHI1_2	14A6<
VCCP_PGOOD	68B6> 48A4<
VDD_ID	16A7> 17A6> 20A7> 21A7> 49B5<
VGA_BLUE	45B5> 45C1> 45B3<
VGA_DDCCLK	45B5> 45A4<
VGA_DDCDAT	45B5> 45A4<
VGA_GREEN	45B5> 45C1> 45B3<
VGA_HSYNC	45C5> 45D1> 45A4<
VGA_RED	45C1> 45C5> 45B3<
VGA_VSYNC	45C5> 45D1> 45A4<
VIDEO_CLK14	51D6> 45B7<
VIDEO_CLK33	51C8> 45D7<
VIDEO_IDSEL	45B7<
VIDEO_PERR_N	45B7<>
VIDEO_RSET	45B5<
VIDEO_STNDBY_N	45B7<
VID_PGOOD	50B3> 68D2<
VMR_DAC_SS	50B3<> 50C2<>
VQP	47D4<
VRD_ON_N	49A2<>
VRD_ON_N_R	49A2<
VREF_DDR_DIMM	47B4> 47C7> 16A8< 17B7< 20B8< 21B8<
VREF_DDR_MCH	47C4> 47C7> 12A3< 13A3<
VRM_CORE	50A8<> 50B4<>
VRM_ON	49A2> 50B5<
VRM_PBOOT	50C2< 50C7<
VRM_VID<5..0>	49A7> 49D4> 50B5<
VTT_DDR_L	47D3<
VTT_DDR_PGOOD	47D5> 48A4<
VXB_CLK66	51C8> 38C3<
VXB_HI16	11D3<> 38B1<>
VXB_HI17	11D3<> 38B3<>
VXB_HI18	11D3<> 38B3<>
VXB_HI20	11D3<> 38B1<>
VXB_HI21	11D3<> 38B3<>
VXB_HI<15..0>	11C3<> 38A1<>
VXB_PSTRBF	11C3<> 38A4<>
VXB_PSTRBS	11C3<> 38A1<>
VXB_PUSTRBF	11C3<> 38B4<>
VXB_PUSTRBS	11C3<> 38B1<>
WDATA_N	53D6> 54A2<
WGATE_N	53D6> 54A2<
WRTPRT_N	54A2> 53C6<
WTX_SLEEP	49C5<
XTAL1	56A2<
XTAL2	56A2<>
ZN_COMP	56C2<
ZP_COMP	56C2<

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*** Unit Cross-Reference ***
--- for the entire design --

BH1	BATT_HLDR_3P	41B8
C1	CAPN	4C5
C2	CAPN	4B5
C3	CAPN	4C5
C4	CAPN	4B5
C5	CAPN	4C5
C6	CAPN	4B5
C7	CAPN	4C5
C8	CAPN	4B5
C9	CAPN	4B4
C10	CAPN	4B4
C11	CAPN	8B6
C12	CAPN	8B5
C13	CAP-P	8B5
C14	CAPN	8B5
C15	CAP-P	8B5
C16	CAPN	8B5
C17	CAP-P	8B4
C18	CAPN	8B4
C19	CAP-P	8B4
C20	CAPN	8B4
C21	CAP-P	8B4
C22	CAPN	8B4
C23	CAPN	8B3
C24	CAP-P	8B3
C25	CAPN	8B3
C26	CAP-P	8B3
C27	CAPN	8B3
C28	CAP-P	8B2
C29	CAPN	8B2
C30	CAP-P	8B2
C31	CAPN	8B2
C32	CAP-P	8D2
C33	CAP-P	8B2
C34	CAPN	8B2
C35	CAP-P	8D1
C36	CAP-P	8B1
C37	CAPN	8B1
C38	CAP-P	8B1
C39	CAPN	8B1
C40	CAPN	50B8
C41	CAPN	50B8
C42	CAPN	50A7
C43	CAPN	50B7
C44	CAPN	50A7
C45	CAPN	50A6
C46	CAPN	50A8
C47	CAPN	50C6
C48	CAPN	50A8
C49	CAPN	50D5
C50	CAP-P	50D7
C51	CAPN	50A7
C52	CAPN	50A7
C53	CAPN	50B2
C54	CAPN	50C2
C55	CAPN	50A1
C56	CAPN	50C1
C57	CAPN	50C1
C58	CAPN	50D7
C59	CAPN	68D5
C60	CAPN	68C5
C61	CAPN	68D7
C62	CAPN	50C5
C63	CAPN	50D4
C64	CAPN	50A4
C65	CAPN	9B6
C66	CAPN	50A3
C67	CAPN	50A3
C68	CAPN	50A3
C69	CAPN	50A2
C70	CAPN	50A2
C71	CAPN	50A2
C72	CAPN	68B8
C73	CAPN	68B7
C74	CAPN	68D6
C75	CAPN	68D6
C76	CAPN	50D7
C78	CAPN	68D5
C80	CAP-P	68B2
C83	CAPN	50D6
C84	CAPN	50B5
C85	CAPN	9B5
C86	CAPN	10D1
C87	CAP-P	14C1
C88	CAPN	68A7
C90	CAPN	68B3
C91	CAPN	68B2
C93	CAPN	50C2
C94	CAPN	68B4
C297	CAPN	8C2
C298	CAPN	8C2
C299	CAPN	8C2
C300	CAPN	8C2
C305	CAPN	8C4
C306	CAPN	8C4
C307	CAPN	8C3
C308	CAPN	8C3
C309	CAPN	8C3
C310	CAPN	8C3
C405	CAPN	35D1
C406	CAPN	35D1
C407	CAPN	35D2
C408	CAPN	35D2
C409	CAPN	35C1
C410	CAPN	35C1
C411	CAPN	35B1
C412	CAPN	35B2
C413	CAPN	36D2
C414	CAPN	36D2
C415	CAPN	36D1
C416	CAPN	36D1
C417	CAPN	36C1
C418	CAPN	36C1
C419	CAPN	36B2
C420	CAPN	36B1
C421	CAPN	37D2
C422	CAPN	37D2
C423	CAPN	37D1
C424	CAPN	37D1
C425	CAPN	37C1
C426	CAPN	37C1
C427	CAPN	37B2
C428	CAPN	37B1
C429	CAPN	38A6
C430	CAPN	38A6
C431	CAPN	38A5
C432	CAPN	38A5
C433	CAPN	38A3
C434	CAPN	38A3
C435	CAPN	38A5
C436	CAPN	38A4
C437	CAPN	44A2
C438	CAPN	44A2
C439	CAPN	44A2
C440	CAPN	44A2
C441	CAPN	44A3
C442	CAPN	44A3
C443	CAPN	44A3
C444	CAPN	44A3
C445	CAPN	49D2
C446	CAPN	49D2
C447	CAPN	49C2
C448	CAPN	49C3
C449	CAPN	49B1
C450	CAPN	49B1
C451	CAPN	49B1
C452	CAPN	49B1
C453	CAPN	49C2
C454	CAPN	49C2
C499	CAPN	49D1
C500	CAPN	49D1
C501	CAPN	49D1
C502	CAPN	49D2
C503	CAPN	49D2
C504	CAPN	49D2
C505	CAPN	49C2
C506	CAPN	49B2
C507	CAPN	49B2
C508	CAPN	49B1
C509	CAPN	49B1
C510	CAPN	49B1
C520	CAPN	48D5
C521	CAPN	49D2
C522	CAPN	49D2
C523	CAPN	49B2
C524	CAPN	49B2
C527	CAPN	45B8
C528	CAPN	45A7
C530	CAP-P	48D4
C531	CAP-P	48D5
C532	CAP-P	48D4
C533	CAP-P	48C4
C589	CAPN	10C8
C590	CAPN	10D8
C595	CAPN	11C8
C596	CAPN	11C8
C597	CAPN	11B8
C598	CAPN	11B8
C613	CAPN	39C2
C614	CAPN	39B2
C615	CAPN	39B1
C616	CAPN	39C1
C617	CAPN	41C7
C618	CAPN	41B7
C619	CAPN	41B7
C620	CAPN	44C4
C621	CAPN	44C3
C622	CAPN	45B2
C623	CAPN	45B2
C624	CAPN	45B2
C628	CAPN	45A1
C629	CAPN	45A2
C630	CAPN	45D7
C631	CAPN	47A8
C632	CAPN	47A8
C633	CAPN	47B2
C634	CAPN	47A4
C635	CAPN	47B8
C638	CAPN	48C2
C639	CAPN	48D8
C640	CAPN	48C8
C641	CAPN	48B5
C642	CAPN	48C7
C644	CAPN	48D8
C645	CAPN	48D8
C648	CAPN	49D1
C649	CAPN	49D2
C650	CAPN	49C2
C651	CAPN	49B1
C656	CAP-P	47A1
C657	CAP-P	47A1
C658	CAP-P	43D2
C659	CAP-P	43C3
C680	CAPN	35C1
C681	CAP-P	35B1
C682	CAP-P	35B2
C683	CAPN	35D1
C684	CAPN	36C1
C685	CAPN	36D1
C686	CAP-P	36B1
C687	CAP-P	36B2
C688	CAPN	37C1
C689	CAPN	37D1
C690	CAP-P	37B1
C691	CAP-P	37B2
C692	CAPN	38A3
C693	CAPN	38A5
C694	CAP-P	38A4
C695	CAP-P	38A4
C700	CAPN	44A2
C701	CAPN	44A3
C702	CAPN	47B2
C703	CAPN	47B2
C704	CAPN	47B2
C705	CAPN	47B2
C706	CAP-P	47A6
C709	CAP-P	48D1
C710	CAP-P	48C6
C711	CAP-P	52D2
C712	CAP-P	53A8
C713	CAPN	14C2
C714	CAPN	14D2
C715	CAPN	14D2
C716	CAPN	14D2
C717	CAPN	14D2
C718	CAPN	14C1
C719	CAPN	14D1
C720	CAPN	14D1
C721	CAPN	14D1
C722	CAPN	14D1
C723	CAPN	14C1
C724	CAPN	14D1
C725	CAPN	14D1
C726	CAPN	14D1
C727	CAPN	14D1
C760	CAP-P	15B1
C761	CAP-P	15B1
C762	CAP-P	15B1
C763	CAP-P	15B1
C764	CAP-P	15C1
C765	CAP-P	15C1
C766	CAP-P	19A1
C767	CAP-P	19A1
C768	CAP-P	19A1
C769	CAP-P	19A2
C770	CAP-P	19A2
C771	CAP-P	19A2
C776	CAP-P	51A3
C777	CAPN	12B2
C778	CAPN	12B1
C779	CAPN	12A2
C780	CAPN	12A1
C781	CAPN	13A2
C782	CAPN	13A2
C783	CAPN	13B2
C784	CAPN	13B1
C785	CAPN	14A2
C786	CAPN	14A1
C787	CAPN	14A2
C788	CAPN	14A1
C789	CAPN	14A2
C790	CAPN	14A1
C791	CAPN	14A2
C792	CAPN	14A1
C793	CAPN	14B2
C794	CAPN	14A1
C795	CAPN	14B2
C796	CAPN	14B1
C797	CAPN	14B2
C798	CAPN	14B1
C799	CAPN	14B2
C800	CAPN	14A1
C801	CAPN	14B2
C802	CAPN	14A1
C803	CAPN	14C2
C804	CAPN	14A1
C805	CAPN	14A2
C806	CAPN	14A1
C807	CAPN	14A2
C808	CAPN	14A1
C809	CAPN	14A2
C810	CAPN	14B1
C811	CAPN	14A2
C812	CAPN	14B1
C813	CAPN	14B2
C814	CAPN	14A1
C815	CAPN	14B2
C816	CAPN	14A1
C817	CAPN	14B2
C818	CAPN	14A1
C819	CAPN	14B2
C820	CAPN	14A1
C821	CAPN	14B2
C822	CAPN	14A1
C823	CAPN	14C2
C824	CAPN	14B1
C825	CAPN	14C2
C833	CAPN	19B1
C838	CAPN	15B2
C839	CAPN	15B2
C840	CAPN	15B2
C841	CAPN	15B2
C842	CAPN	15C2
C843	CAPN	15C2
C845	CAPN	19B2
C846	CAPN	19B2
C847	CAPN	19B2
C850	CAPN	19C2
C851	CAPN	19C2
C852	CAPN	19C2
C853	CAPN	19C1
C854	CAPN	19C1
C855	CAPN	19C1
C862	CAPN	51A2
C863	CAPN	51A1
C864	CAPN	51A1
C865	CAPN	51A1
C866	CAPN	51A2
C867	CAPN	51A2
C868	CAPN	51A2
C869	CAPN	51A2
C870	CAPN	51A3
C871	CAPN	51A3
C872	CAPN	51A3
C873	CAPN	51A3
C874	CAPN	51A2
C875	CAPN	51A2
C876	CAPN	51A2
C881	CAP-P	51A1
C882	CAPN	48C3
C883	CAPN	53D2
C884	CAPN	53D1
C885	CAPN	53A8
C886	CAPN	53A8
C887	CAPN	53A7
C888	CAPN	53A7
C889	CAPN	53A7
C893	CAPN	52D2
C894	CAPN	52D1
C895	CAPN	52D1
C897	CAPN	61B4
C898	CAPN	61C4
C899	CAPN	63C8
C900	CAPN	63C8
C901	CAPN	63C7
C902	CAPN	63B5
C903	CAPN	63B3
C904	CAPN	10C1
C905	CAPN	11C2
C906	CAPN	11C1
C907	CAPN	11B1
C908	CAPN	11B2
C909	CAPN	11B2
C910	CAPN	11C2
C911	CAPN	11C1
C912	CAPN	11B1
C913	CAPN	11B8
C914	CAPN	11B8
C915	CAPN	11C8
C916	CAPN	11C8
C921	CAPN	18B4
C922	CAPN	18B3
C923	CAPN	18B3
C924	CAPN	18B3
C925	CAPN	18B3
C926	CAPN	18B3
C927	CAPN	18B3
C928	CAPN	18B3
C929	CAPN	18B2
C930	CAPN	18B2
C931	CAPN	18B2
C932	CAPN	18B2
C933	CAPN	18B4
C934	CAPN	18B4
C935	CAPN	18B4
C936	CAPN	18B3
C937	CAPN	18B3
C938	CAPN	18B3
C939	CAPN	18B3
C940	CAPN	18B3
C941	CAPN	18B3
C942	CAPN	18B2
C943	CAPN	18B2
C944	CAPN	18B2
C945	CAPN	18B2
C946	CAPN	18B2
C947	CAPN	18A4
C948	CAPN	18A4
C949	CAPN	18A3
C950	CAPN	18A3
C951	CAPN	18A3
C952	CAPN	18A3
C953	CAPN	18A3
C954	CAPN	18A3
C955	CAPN	18A3
C956	CAPN	18C4
C957	CAPN	18C4
C958	CAPN	18C4
C959	CAPN	18C3
C960	CAPN	18C3
C961	CAPN	18C3
C962	CAPN	18C3

DRAWING

PAGE	REV
77	A2.1

C963	CAPN	18C3
C964	CAPN	18C3
C965	CAPN	18C3
C966	CAPN	18C2
C967	CAPN	18C2
C968	CAPN	18C2
C969	CAPN	18C2
C970	CAPN	18D3
C971	CAPN	18D3
C972	CAPN	18D3
C973	CAPN	18D3
C974	CAPN	18D3
C975	CAPN	18D3
C976	CAPN	18D3
C977	CAPN	18D4
C978	CAPN	18D4
C979	CAPN	18D4
C980	CAPN	18B4
C981	CAPN	22A2
C982	CAPN	22A2
C983	CAPN	22A2
C984	CAPN	22A2
C985	CAPN	22A2
C986	CAPN	22A1
C987	CAPN	22A3
C988	CAPN	22A3
C989	CAPN	22A3
C990	CAPN	22A2
C991	CAPN	22A2
C992	CAPN	22A2
C993	CAPN	22A2
C994	CAPN	22A2
C995	CAPN	22A1
C996	CAPN	22A1
C997	CAPN	22B2
C998	CAPN	22B2
C999	CAPN	22B2
C1000	CAPN	22B2
C1001	CAPN	22B2
C1002	CAPN	22B1
C1003	CAPN	22B1
C1004	CAPN	22B1
C1005	CAPN	22B1
C1006	CAPN	22D3
C1007	CAPN	22D3
C1008	CAPN	22D3
C1009	CAPN	22D2
C1010	CAPN	22D2
C1011	CAPN	22D2
C1012	CAPN	22D2
C1013	CAPN	22D2
C1014	CAPN	22A3
C1015	CAPN	22A3
C1016	CAPN	22C1
C1017	CAPN	22C1
C1018	CAPN	22C2
C1019	CAPN	22C2
C1020	CAPN	22C2
C1021	CAPN	22C2
C1022	CAPN	22C2
C1023	CAPN	22C2
C1024	CAPN	22C2
C1025	CAPN	22C3
C1026	CAPN	22C3
C1027	CAPN	22C3
C1028	CAPN	22C3
C1029	CAPN	22C3
C1030	CAPN	22C3
C1031	CAPN	22C3
C1032	CAPN	22C2
C1033	CAPN	22C2
C1034	CAPN	22C2
C1035	CAPN	22C2
C1036	CAPN	22C2
C1037	CAPN	22C2
C1038	CAPN	22C1
C1039	CAPN	22C1
C1040	CAPN	22D1
C1041	CAPN	25D1
C1042	CAPN	25C1
C1043	CAPN	25D1
C1044	CAPN	25C1
C1045	CAPN	26B4
C1046	CAPN	26B4
C1047	CAPN	26A5

C1048	CAPN	26A5
C1049	CAPN	26A5
C1050	CAPN	26A5
C1051	CAPN	26A4
C1052	CAPN	26A4
C1053	CAPN	29D1
C1054	CAPN	29C1
C1055	CAPN	29D1
C1056	CAPN	29C1
C1057	CAPN	30A5
C1058	CAPN	30A5
C1059	CAPN	30A5
C1060	CAPN	30A5
C1061	CAPN	30A6
C1062	CAPN	30B4
C1063	CAPN	30B4
C1064	CAPN	30A6
C1078	CAPN	41C7
C1079	CAPN	41A5
C1080	CAPN	41C7
C1081	CAPN	41A3
C1085	CAPN	41B2
C1086	CAPN	41B2
C1089	CAPN	41B3
C1090	CAPN	41B2
C1091	CAPN	41C3
C1093	CAPN	41C2
C1094	CAPN	41C2
C1095	CAPN	41C2
C1096	CAPN	41C3
C1097	CAPN	41C3
C1098	CAPN	41C2
C1099	CAPN	41C2
C1100	CAPN	41C2
C1101	CAPN	41C2
C1106	CAPN	43C2
C1107	CAPN	43D2
C1108	CAPN	42A3
C1110	CAPN	45A7
C1111	CAPN	45B7
C1112	CAPN	47B1
C1113	CAPN	47B1
C1114	CAPN	47B1
C1115	CAPN	47B1
C1124	CAPN	47A6
C1125	CAPN	47B8
C1126	CAPN	47B8
C1127	CAPN	47B6
C1128	CAPN	47A6
C1129	CAPN	48D8
C1130	CAPN	48D6
C1131	CAPN	48D4
C1132	CAPN	48D4
C1133	CAPN	48C6
C1134	CAPN	48D5
C1135	CAPN	48C4
C1136	CAPN	48C6
C1137	CAPN	48A5
C1143	CAPN	12A3
C1144	CAPN	12A3
C1145	CAPN	12A3
C1146	CAPN	13A4
C1147	CAPN	13A4
C1148	CAPN	13A4
C1149	CAPN	16A7
C1152	CAPN	17B7
C1153	CAPN	20B7
C1156	CAPN	21B7
C1157	CAPN	26B3
C1158	CAPN	26B3
C1159	CAPN	26B3
C1160	CAPN	26B3
C1161	CAPN	26B3
C1162	CAPN	26B2
C1163	CAPN	26B2
C1164	CAPN	26B2
C1165	CAPN	26A4
C1166	CAPN	26A4
C1167	CAPN	26A4
C1168	CAPN	26A4
C1169	CAPN	26A3
C1170	CAPN	26A3
C1171	CAPN	26A3
C1172	CAPN	26A3
C1173	CAPN	26A3

C1174	CAPN	26A3
C1175	CAPN	26A3
C1176	CAPN	26A2
C1177	CAPN	26A2
C1178	CAPN	26A2
C1179	CAPN	26A2
C1180	CAPN	26A2
C1181	CAPN	26A2
C1182	CAPN	26A1
C1183	CAPN	26A1
C1184	CAPN	26A1
C1185	CAPN	30A1
C1186	CAPN	30A1
C1187	CAPN	30A1
C1188	CAPN	30A1
C1189	CAPN	30A2
C1190	CAPN	30A2
C1191	CAPN	30A2
C1192	CAPN	30A2
C1193	CAPN	30A2
C1194	CAPN	30A3
C1195	CAPN	30A3
C1196	CAPN	30A3
C1197	CAPN	30A3
C1198	CAPN	30A3
C1199	CAPN	30A4
C1200	CAPN	30A4
C1201	CAPN	30A4
C1202	CAPN	30A4
C1203	CAPN	30A4
C1204	CAPN	30B2
C1205	CAPN	30B3
C1206	CAPN	30B3
C1207	CAPN	30B4
C1208	CAPN	30B4
C1209	CAPN	30B3
C1210	CAPN	30B3
C1211	CAPN	30B2
C1212	CAPN	30A5
C1213	CAPN	33B1
C1214	CAPN	33B2
C1215	CAPN	33B2
C1216	CAPN	33B1
C1217	CAPN	33C1
C1218	CAPN	33C1
C1219	CAPN	33A1
C1220	CAPN	33A2
C1221	CAPN	34B2
C1222	CAPN	34B1
C1223	CAPN	34C1
C1224	CAPN	34D1
C1225	CAPN	34D2
C1226	CAPN	34D2
C1227	CAPN	34D1
C1228	CAPN	34C1
C1240	CAPN	45A2
C1241	CAPN	45A2
C1243	CAPN	48D6
C1244	CAPN	54A6
C1245	CAPN	54A6
C1246	CAPN	54A6
C1247	CAPN	54A6
C1248	CAPN	54A4
C1249	CAPN	54A4
C1250	CAPN	54A5
C1251	CAPN	54A5
C1252	CAPN	54A4
C1253	CAPN	54A5
C1254	CAPN	54A5
C1255	CAPN	54A5
C1256	CAPN	54A4
C1257	CAPN	54A6
C1258	CAPN	54A6
C1259	CAPN	54A5
C1260	CAPN	54A6
C1261	CAPN	54C3
C1262	CAPN	54B3
C1263	CAPN	54C3
C1264	CAPN	54B3
C1265	CAPN	54C3
C1266	CAPN	54B4
C1267	CAPN	54C3
C1268	CAPN	54B3
C1269	CAPN	56B5
C1270	CAPN	56B1

C1271	CAPN	56B1
C1272	CAPN	57A5
C1273	CAPN	57A5
C1274	CAPN	57A6
C1276	CAPN	57C5
C1277	CAPN	57C5
C1278	CAPN	57C5
C1279	CAPN	57A5
C1281	CAPN	57A4
C1282	CAPN	57A4
C1283	CAPN	57A4
C1284	CAPN	57A4
C1285	CAPN	57A3
C1286	CAPN	57A3
C1287	CAPN	57A3
C1288	CAPN	57A3
C1290	CAPN	57A6
C1291	CAPN	57C5
C1293	CAPN	57C3
C1294	CAPN	57C3
C1295	CAPN	57C3
C1296	CAPN	57C4
C1297	CAPN	57C4
C1298	CAPN	57C4
C1299	CAPN	57C4
C1300	CAPN	57C4
C1301	CAPN	57A4
C1302	CAPN	57A5
C1303	CAPN	57A5
C1304	CAPN	58A7
C1305	CAPN	58A7
C1306	CAPN	58A8
C1307	CAPN	58A5
C1308	CAPN	58A5
C1309	CAPN	58A6
C1310	CAPN	58A5
C1311	CAPN	58A6
C1312	CAPN	59C1
C1313	CAPN	61A3
C1314	CAPN	61C3
C1315	CAPN	61B3
C1316	CAPN	61B3
C1317	CAPN	61D8
C1318	CAPN	61A2
C1319	CAPN	61B4
C1320	CAPN	61B3
C1321	CAPN	61C3
C1322	CAPN	61B4
C1323	CAPN	61C3
C1324	CAPN	61C4
C1325	CAPN	62B3
C1326	CAPN	62B3
C1327	CAPN	62B3
C1328	CAPN	62C3
C1329	CAPN	62C2
C1330	CAPN	62C3
C1331	CAPN	62C3
C1332	CAPN	62B3
C1333	CAPN	62C3
C1334	CAPN	62C3
C1335	CAPN	62D3
C1336	CAPN	62A5
C1337	CAPN	62A5
C1338	CAPN	62A4
C1339	CAPN	62A4
C1340	CAPN	62A3
C1341	CAPN	62A4
C1342	CAPN	63D8
C1343	CAPN	63D8
C1344	CAPN	63D7
C1345	CAPN	63D7
C1346	CAPN	63D7
C1347	CAPN	63D7
C1348	CAPN	63D6
C1349	CAPN	63D6
C1350	CAPN	63D6
C1351	CAPN	63D6
C1352	CAPN	63D5
C1353	CAPN	63D5
C1354	CAPN	63D5
C1355	CAPN	63D5
C1356	CAPN	63D4
C1357	CAPN	63D4
C1358	CAPN	63D4
C1359	CAPN	63D4

C1360	CAPN	63D3
C1361	CAPN	63D3
C1362	CAPN	63C3
C1363	CAPN	63C3
C1364	CAPN	63C2
C1365	CAPN	63C2
C1366	CAPN	63C2
C1367	CAPN	63C2
C1368	CAPN	63C1
C1369	CAPN	63C7
C1370	CAPN	63C7
C1371	CAPN	63C7
C1372	CAPN	63C5
C1373	CAPN	63C5
C1374	CAPN	63A6
C1375	CAPN	63B5
C1376	CAPN	63B2
C1377	CAPN	63A2
C1378	CAPN	63A3
C1379	CAPN	63B8
C1380	CAPN	65D6
C1381	CAPN	65B7
C1382	CAPN	65B4
C1383	CAPN	65B1
C1384	CAPN	65B5
C1385	CAPN	66B1
C1386	CAPN	66B4
C1387	CAPN	66B7
C1388	CAPN	66D6
C1389	CAPN	66B5
C1390	CAP-P	26B4
C1391	CAP-P	26B4
C1392	CAP-P	26A5
C1393	CAP-P	26A6
C1394	CAP-P	30A6
C1395	CAP-P	30A6
C1396	CAP-P	30B5
C1397	CAP-P	30B4
C1398	CAPN	33B1
C1399	CAPN	33C1
C1400	CAP-P	33A1
C1401	CAP-P	33A1
C1402	CAP-P	34B1
C1403	CAP-P	34B1
C1404	CAPN	34D1
C1405	CAPN	34C1
C1410	CAP-P	57B4
C1411	CAP-P	57B3
C1414	CAP-P	57D8
C1415	CAP-P	57D7
C1416	CAP-P	57D7
C1419	CAP-P	57B6
C1421	CAP-P	57B4
C1422	CAP-P	61B3
C1423	CAP-P	61B2
C1424	CAP-P	61C2
C1425	CAP-P	61A3
C1426	CAP-P	61D8
C1427	CAP-P	61A3
C1428	CAP-P	62D3
C1429	CAP-P	62C2
C1430	CAP-P	62C2
C1431	CAP-P	62C2
C1432	CAP-P	62B1
C1433	CAP-P	63B8
C1434	CAP-P	65D5
C1435	CAP-P	65B7
C1436	CAP-P	65B4
C1437	CAP-P	65B2
C1438	CAP-P	66B2
C1439	CAP-P	66B4
C1440	CAP-P	66B7
C1441	CAP-P	66D5
C1448	CAPN	54C6
C1449	CAPN	54D6
C1450	CAPN	54D6
C1451	CAPN	54C6
C1452	CAPN	54C6
C1453	CAPN	54C6
C1479	CAP-P	47D4
C1481	CAP-P	47D1
C1482	CAP-P	47D1
C1483	CAP-P	47D1
C1484	CAP-P	47D2
C1496	CAPN	14A3

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C1497	CAPN	14A4
C1498	CAPN	14A6
C1499	CAPN	14A6
C1501	CAPN	47D7
C1502	CAPN	47D7
C1503	CAPN	47D5
C1504	CAPN	47D8
C1505	CAPN	47D7
C1506	CAPN	47D3
C1507	CAPN	47D2
C1508	CAPN	47C4
C1513	CAPN	70C1
C1514	CAPN	70C1
C1515	CAPN	70A1
C1516	CAPN	70A1
C1517	CAPN	70A1
C1518	CAPN	70A1
C1519	CAPN	70B1
C1520	CAPN	70B1
C1521	CAPN	70B1
C1522	CAPN	70B1
C1528	CAPN	44A1
C1529	CAPN	44A1
C1530	CAPN	45D3
C1531	CAPN	45D3
C1532	CAPN	70C2
C1533	CAPN	70C2
C1534	CAPN	70C2
C1543	CAP-P	44A1
C1544	CAP-P	44A1
C1546	CAPN	55C3
C1547	CAPN	55B5
C1548	CAPN	55D4
C1549	CAPN	55C8
C1550	CAPN	55C1
C1551	CAPN	55C2
C1552	CAPN	55B4
C1553	CAPN	55C1
C1554	CAPN	55B1
C1555	CAP-P	55D2
C1556	CAP-P	55C2
C1557	CAP-P	55B1
C1558	CAP-P	55B1
C1559	CAPN	55B7
C1560	CAPN	55B5
C1561	CAPN	55C8
C1562	CAPN	55B6
C1563	CAPN	55C7
C1564	CAPN	55C3
C1565	CAPN	55A2
C1566	CAP-P	55B4
C1567	CAP-P	18A2
C1568	CAP-P	18A1
C1569	CAP-P	22A4
C1570	CAP-P	22A4
C1575	CAPN	47A6
C1576	CAPN	47B2
C1577	CAP-P	47D4
C1584	CAPN	51C8
C1585	CAPN	51C8
C1587	CAPN	57A5
C1588	CAPN	57A3
C1589	CAP-P	58D2
C1590	CAP-P	14A5
C1591	CAP-P	14A3
C1592	CAP-P	14A4
C1593	CAPN	43C2
C1594	CAPN	43B2
C1595	CAPN	43B2
C1596	CAPN	43C2
C1597	CAPN	47C7
C1598	CAPN	56B5
C1599	CAPN	56D4
C1600	CAP-P	57C4
C1601	CAP-P	57C3
C1602	CAPN	57C4
C1603	CAPN	57C4
C1604	CAPN	57C5
C1605	CAPN	57C5
C1606	CAP-P	57C3
C1607	CAPN	57B4
C1608	CAPN	57B4
C1609	CAPN	57B4
C1610	CAPN	57B3
C1611	CAPN	57B3

C1612	CAPN	57B3
C1613	CAPN	57D5
C1614	CAPN	57D5
C1615	CAPN	57D5
C1616	CAPN	57D5
C1617	CAPN	57D4
C1618	CAPN	57D4
C1619	CAPN	57B5
C1620	CAPN	57B5
C1621	CAPN	57B5
C1622	CAPN	57B5
C1623	CAPN	58D3
C1624	CAPN	58D3
C1625	CAPN	58D2
C1626	CAPN	58A3
C1627	CAP-P	57B3
C1628	CAP-P	57D6
C1629	CAP-P	57D7
C1630	CAP-P	57D6
C1631	CAP-P	57D6
C1641	CAPN	47C8
C1642	CAPN	47C8
C1643	CAPN	14A5
C1644	CAPN	14A5
C1661	CAPN	69D7
C1662	CAPN	69C4
C1663	CAPN	69C4
C1664	CAPN	69B4
C1665	CAPN	69B4
C1666	CAPN	12C1
C1667	CAPN	12C1
C1668	CAPN	12D1
C1669	CAPN	12D1
C1670	CAPN	49C5
C1671	CAPN	49C7
C4059	CAPN	50A7
C4061	CAPN	50A6
CR1	DIOSOT23C	41C7
CR2	DIOSOT23C	41B5
CR3	DIODE	48D6
CR4	DIODE	47A4
CR5	DIODE	47B6
CR6	DIODE	47A6
CR7	DIODE	47B2
CR8	DIODE	72B6
CR9	LED	48B3
CR10	LED	42C4
CR11	SCHOTTKY	50A2
CR12	SCHOTTKY	68C6
CR13	SCHOTTKY	68B4
CR14	SCHOTTKY	68B1
CR16	SCHOTTKY	50A4
CR17	LED	42D4
CR18	SCHOTTKY	50C2
CR26	DIODE	48C5
CR45	DIODE	54B7
CR46	DIODPAK	64D7
CR47	DIODPAK	64D4
CR49	DIOSOT23S	45D2
CR50	DIOSOT23S	45D2
CR51	DIOSOT23S	45C2
CR52	DIOSOT23S	45C2
CR53	DIOSOT23S	45C2
CR68	LED	58C2
CR72	DIOSOT23C	48A4
CR74	SCHOTTKY	47D2
CR78	DIODE	55C4
CR79	DIODE	55A2
CR80	DIODE	47C7
CR81	LED	56A4
CR3008	SCHOTTKY	50D4
FB1	FERR_BD	45B2
FB2	FERR_BD	45B3
FB3	FERR_BD	45B2
FB4	FERRITE	51A1
FB5	FERRITE	51A1
FB6	FERRITE	62D2
FB7	FERRITE	62B2
FB8	FERRITE	62B2
FB9	FERRITE	62C2
FB10	FERRITE	62C2
FB13	FERR_BD	43B2
FB14	FERR_BD	43B2
FB15	FERR_BD	43C2
FB16	FERR_BD	43C2

FB17	FBPAK4L	54C7 54D7
FB18	FERR_BD	54D6
FB27	FERR_BD	45D3
FB28	FERR_BD	45A3
FB29	FERR_BD	45A3
FB30	FERRITE	57C3
FB31	FERRITE	63C4
J1	CONN184_DDR_ECC	20C7
J2	CONN184_DDR_ECC	16C7
J4	2X3HDR	49A6
J5	CONN184_DDR_ECC	17C7
J6	2X3HDR	49A6
J9	CONN184_DDR_ECC	21C7
J10	CON2XUSB	43C1
J11	CONPCI	44D6
J12	PCI_X_VXB	38D2 38D6
J15	1X2HDR	45A8
J16	2X20HDR20	43B5
J20	PCI_X_3V	33D5
J21	PCI_X_3V	34D5
J23	PCI_X_3V	35D5
J24	PCI_X_3V	36D5
J25	PCI_X_3V	37D5
J27	1X4HDR	52D7
J28	1X2HDR	49A5
J29	CONVGAEDGE	45B1
J31	DSUB25TALL_B	54B4
J34	2X17HDR5	54B3
J35	DSUB9	54D2
J37	4X17SCSIRA	64C6
J38	4X17SCSIRA	64C3
J39	RJ45_JACK	58B2
J40	PS2STACK	54D5
J43	2X15HDR	70D4
J49	CONN_SMA	51D7
J50	2X30RCPT	52B6
J51	1X3HDR	71A5 71B5
J52	1X3HDR	71A5
J53	1X3HDR	71A5
J71	CONN_2X15_SM	70B5
J100	CONN24_WTX_MAIN	49D8
J101	CONN22_WTX	49C5
J102	CONN8_WTX_DIG	49D5
J4009	CONN1X28_MT	9B6
JP1	1X2HDR	42C6
JP2	1X2HDR	42C6
JP4	1X3HDR	41C7
JP7	1X2HDR	42A5
JP14	1X2HDR	56A6
JP19	1X2HDR	60A6
JP24	1X3HDR	23D3
JP25	1X3HDR	23C2
JP26	1X2HDR	23C3
JP28	1X3HDR	24D1
JP29	1X2HDR	24D2
JP31	1X2HDR	27C3
JP32	1X3HDR	27D3
JP33	1X2HDR	28C2
JP34	1X2HDR	28C2
JP35	1X3HDR	27D1
JP38	1X3HDR	69D2
JP39	1X3HDR	69C2
JP40	1X3HDR	69C2
JP41	1X3HDR	69B2
L1	INDUCTOR	68B4
L2	INDUCTOR	50C1
L3	INDUCTOR	50B2
L7	INDUCTOR	47B2
L8	INDUCTOR	47A4
L12	INDUCTOR	48D6
L18	INDUCTOR	47D2
L19	INDUCTOR	14A4
L20	INDUCTOR	14A3
L21	INDUCTOR	14A4
L22	INDUCTOR	55C3
MH1	MTG_HOLE	67D7
MH2	MTG_HOLE	67C7
MH3	MTG_HOLE	67D6
MH4	MTG_HOLE	67C6
MH5	MTG_HOLE	67D5
MH7	MTG_HOLE	67D4
MH8	MTG_HOLE	67C4
MH9	MTG_HOLE	67D3
MH10	MTG_HOLE	67C3
MH11	MTG_HOLE	67D2

POT1	POT_TC03	47C8
POT2	POT_TC03	47C8
Q1	MOSFETN	47B3
Q2	MOSFETN	47B3
Q3	MOSFETN	47A5
Q4	MOSFETN	47A5
Q5	MOSFETN	47B3
Q6	MOSFETN	47B3
Q7	MOSFETN	47A4
Q8	MOSFETN	47A4
Q9	MOSFETN	48D6
Q10	MOSFETN	48C6
Q11	MOSFETN	50C3
Q20	MGSF1N02LT1	52C5
Q21	MOSFETN	50C3
Q22	MOSFETN	50B3
Q23	MOSFETN	50A3
Q24	MOSFETN	50C2
Q25	MOSFETN	50A2
Q26	MOSFETN	50C2
Q27	MOSFETN	50B2
Q32	MBT3904DUAL	39D2
Q33	MBT3904DUAL	52B2
Q41	NPN	42A4
Q43	MOSFETN	47D3
Q44	MOSFETN	47D3
Q48	NPN	49B3
Q49	MOSFETN	55C3
Q50	MOSFETN	55A3
Q60	MBT3904DUAL	49A2
Q65	MBT3904DUAL	7A6
Q67	NPN	41A1
Q68	PZT751	41A1
R1	RESN	4D6
R2	RESN	4C6
R3	RESN	4C2
R4	RESN	4C2
R5	RESN	4C2
R6	RESN	4C1
R7	RESN	4C1
R8	RESN	4C1
R9	RESN	4C1
R10	RESN	4B3
R11	RESN	4B3
R12	RESN	49A4
R13	RESN	50C8
R14	RESN	50C8
R15	RESN	50B8
R16	RESN	50C7
R17	RESN	50C7
R18	RESN	50B7
R19	RESN	50C7
R20	RESN	50B7
R21	RESN	50A7
R22	RESN	50A6
R23	RESN	50A6
R24	RESN	50C6
R25	RESN	50B6
R26	RESN	50D6
R27	RESN	50D5
R28	RESN	50D6
R29	RESN	4C5
R30	RESN	6B8
R31	RESN	68A6
R32	RESN	50A5
R33	RESN	72A6
R34	RESN	50A4
R35	RESN	50D4
R36	RESN	68A3
R37	RESN	68B3
R38	RESN	9D5
R39	RESN	50C8
R40	RESN	50B5
R41	RESN	50B1
R42	RESN	50C1
R43	RESN	4B5
R44	RESN	4D5
R45	RESN	13B5
R46	RESN	49D4
R47	RESN	12A4
R48	RESN	49D3
R49	RESN	49D3
R50	RESN	13A5
R51	RESN	13A5
R52	RESN	50D6

R53	RESN	50B6
R54	RESN	68D2
R55	RESN	9C5
R56	RESN	25B7
R57	RESN	25A2
R58	RESN	6B3
R59	RESN	45A8
R60	RESN	50C2
R61	RESN	6B3
R63	RESN	49A2
R64	RESN	49D3
R65	RESN	50D2
R66	RESN	51D3
R67	RESN	51C2
R68	RESN	51C2
R69	RESN	68B4
R70	RESN	9A6
R71	RESN	9A6
R72	RESN	9A5
R73	RESN	9A5
R74	RESN	9A5
R75	RESN	51B5
R76	RESN	9A4
R77	RESN	9D5
R78	RESN	9D4
R80	RESN	49D3
R81	RESN	49D3
R82	RESN	51B5
R83	RESN	9D5
R84	RESN	9D6
R85	RESN	42D3
R86	RESN	68B3
R87	RESN	42C2
R88	RESN	4C6
R89	RESN	9B5
R90	RESN	10D7
R91	RESN	10D7
R92	RESN	10C8
R93	RESN	10C7
R94	RESN	10D7
R95	RESN	10D8
R96	RESN	10D2
R97	RESN	10D1
R98	RESN	10C1
R99	RESN	11D2
R100	RESN	11D2
R101	RESN	11C1
R102	RESN	11C1
R103	RESN	11B2
R104	RESN	11B1
R105	RESN	11B2
R106	RESN	11B2
R107	RESN	11C7
R108	RESN	11C8
R109	RESN	11C8
R110	RESN	11D8
R111	RESN	11B7
R112	RESN	11B8
R113	RESN	11B8
R114	RESN	11B8
R115	RESN	12D2
R116	RESN	9B6
R117	RESN	12B4
R118	RESN	12A4
R119	RESN	68B8
R120	RESN	13D2
R121	RESN	68C7
R122	RESN	68C6
R123	RESN	40B1
R124	RESN	13B5
R125	RESN	7C6
R126	RESN	7C6
R127	RESN	7C6
R128	RESN	16A3
R129	RESN	16A3
R130	RESN	16A3
R131	RESN	16A3
R132	RESN	16A3
R133	RESN	16A3
R134	RESN	7D6
R135	RESN	4B5
R136	RESN	9A4
R137	RESN	4C4
R138	RESN	4C4
R139	RESN	4C4

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R140	RESN	68B8
R141	RESN	68D2
R142	RESN	49D3
R143	RESN	48A4
R144	RESN	40A1
R145	RESN	6B7
R146	RESN	29A2
R147	RESN	6B2
R148	RESN	49D3
R149	RESN	9A5
R150	RESN	68A2
R152	RESN	17A3
R153	RESN	17A3
R154	RESN	17A2
R155	RESN	17A2
R159	RESN	17A2
R160	RESN	17A3
R161	RESN	12B4
R165	RESN	20A3
R166	RESN	20A3
R167	RESN	20A3
R168	RESN	20A3
R169	RESN	20A3
R170	RESN	20A3
R174	RESN	49A5
R181	RESN	7D3
R182	RESN	7C3
R183	RESN	7D3
R184	RESN	7C3
R189	RESN	21A3
R190	RESN	21A3
R191	RESN	21A3
R195	RESN	21A3
R196	RESN	21A3
R197	RESN	21A3
R198	RESN	13B4
R199	RESN	40A1
R200	RESN	23D3
R201	RESN	24C2
R202	RESN	12A5
R203	RESN	12B4
R204	RESN	40A7
R205	RESN	25C5
R206	RESN	25A5
R207	RESN	51D3
R208	RESN	25D3
R209	RESN	25D1
R210	RESN	25D1
R211	RESN	26B8
R212	RESN	12C2
R213	RESN	40A7
R214	RESN	72D6
R215	RESN	13D2
R216	RESN	25A2
R217	RESN	72C6
R218	RESN	25B5
R219	RESN	25B5
R220	RESN	72C6
R221	RESN	72C6
R222	RESN	72C6
R223	RESN	72C6
R224	RESN	48B2
R225	RESN	25B5
R226	RESN	56A7
R227	RESN	25B5
R228	RESN	25C5
R229	RESN	60A6
R230	RESN	72B6
R231	RESN	72D3
R232	RESN	25C1
R233	RESN	27D3
R234	RESN	72D3
R235	RESN	72D2
R236	RES	28C3
R237	RESN	72D2
R238	RESN	72D2
R239	RESN	72D2
R240	RES	29B7
R241	RESN	29C5
R242	RESN	72C2
R243	RESN	30C8
R244	RESN	72B2
R245	RESN	72B2
R246	RESN	72B2
R247	RESN	72B1

R255	RESN	60B7
R256	RESN	42C4
R257	RESN	29C1
R258	RESN	29D3
R259	RESN	29D1
R260	RESN	29D1
R261	RESN	42B2
R262	RESN	29B7
R263	RESN	29B7
R264	RESN	29B7
R265	RESN	29C6
R266	RESN	42B2
R267	RESN	42C3
R268	RESN	32A1
R270	RES	33D2
R271	RESN	33D7
R272	RESN	33D6
R273	RES	33C7
R275	RES	33D8
R277	RESN	34D6
R278	RESN	34D6
R279	RES	34C7
R329	RESN	35D6
R330	RESN	35D6
R331	RES	35C7
R336	RESN	36D6
R337	RESN	36D6
R338	RES	36C7
R342	RESN	37D6
R343	RESN	37D6
R344	RES	37C7
R348	RESN	38C5
R349	RESN	38C5
R350	RESN	38C5
R353	RESN	39B2
R354	RESN	39B3
R355	RESN	39B2
R356	RESN	39C2
R357	RESN	39C1
R358	RESN	39C1
R359	RESN	39D4
R360	RESN	39D4
R361	RESN	39B1
R362	RESN	39D4
R368	RESN	40D6
R369	RESN	40D7
R371	RESN	40B1
R374	RESN	40A6
R375	RESN	41C6
R376	RESN	41B7
R377	RESN	41B7
R378	RESN	41B6
R379	RESN	41B5
R380	RESN	41C7
R381	RESN	41D5
R382	RESN	41C7
R383	RESN	41C8
R384	RESN	43B5
R385	RESN	43B6
R386	RESN	43A5
R387	RESN	43B6
R389	RESN	39B2
R390	RESN	40B2
R392	RESN	43B3
R393	RESN	43D2
R394	RESN	43C3
R395	RESN	43C2
R396	RESN	42A3
R397	RESN	42A3
R398	RESN	42B5
R399	RESN	42A4
R400	RESN	42D6
R401	RESN	42B6
R402	RESN	44C7
R403	RESN	44C7
R404	RESN	44C7
R405	RESN	44C8
R421	RESN	47B7
R422	RESN	47A8
R423	RESN	47A8
R424	RESN	47A8
R425	RESN	47B2
R426	RESN	47A3
R427	RESN	47B2
R428	RESN	47A4

R429	RESN	47B8
R430	RESN	47A8
R431	RESN	47A8
R433	RESN	47A3
R434	RESN	47B1
R435	RESN	47A1
R436	RESN	47A1
R452	RESN	48C5
R453	RESN	48C5
R454	RESN	48C5
R455	RESN	48D7
R457	RESN	48D5
R458	RESN	48C5
R459	RESN	48C8
R460	RESN	48D7
R461	RESN	45B3
R462	RESN	45B3
R463	RESN	45B3
R466	RESN	45A3
R467	RESN	45B2
R468	RESN	45B3
R469	RESN	45B3
R470	RESN	45B8
R471	RESN	45B8
R472	RESN	45B7
R473	RESN	45B4
R474	RESN	46A4
R475	RESN	46C7
R482	RESN	52C7
R483	RESN	52D8
R484	RESN	52B1
R485	RESN	52C3
R486	RESN	52C3
R487	RESN	52C3
R488	RESN	52C5
R489	RESN	52C6
R490	RESN	52C3
R491	RESN	52C7
R492	RESN	52C2
R493	RESN	52C2
R494	RESN	52C3
R495	RESN	52D6
R496	RESN	52D7
R497	RESN	53C3
R499	RESN	53C3
R500	RESN	49C1
R501	RESN	49C1
R502	RESN	49C1
R503	RESN	49C1
R504	RESN	49D1
R505	RESN	49D1
R506	RESN	49D1
R507	RESN	49D1
R509	RESN	39D2
R510	RESN	39D1
R511	RESN	39D2
R512	RESN	39D4
R520	RESN	49A2
R521	RESN	12C1
R522	RESN	12A2
R523	RESN	12A2
R524	RESN	12B1
R525	RESN	13A2
R526	RESN	13A2
R527	RESN	13C1
R528	RESN	13C2
R529	RESN	48A8
R530	RESN	48A8
R531	RESN	48B3
R532	RESN	51B7
R534	RESN	51B4
R535	RESN	51A5
R536	RESN	51A5
R537	RESN	51A6
R538	RESN	51B5
R539	RESN	51A6
R540	RESN	51C3
R541	RESN	51C3
R544	RESN	51B3
R545	RESN	51C2
R546	RESN	51C2
R549	RESN	51B2
R550	RESN	51B2
R551	RESN	51D5
R552	RESN	51D5

R553	RESN	51B3
R559	RESN	54A2
R560	RESN	54B4
R562	RESN	40D6
R565	RESN	23D4
R568	RESN	24D4
R569	RESN	25A1
R570	RESN	25A6
R571	RESN	25A6
R572	RESN	25A6
R574	RESN	25A2
R576	RESN	27D4
R578	RES	28D4
R580	RES	29A2
R581	RES	29A2
R582	RES	29A2
R586	RESN	23B4
R587	RESN	24B3
R588	RESN	28B4
R589	RESN	27B4
R646	RESN	48A7
R648	RESN	48A6
R652	RESN	56A2
R653	RESN	56D5
R658	RESN	56A1
R659	RESN	56A1
R660	RESN	56C1
R661	RESN	58B1
R662	RESN	58C1
R663	RESN	58B1
R664	RESN	56C1
R665	RESN	58A8
R666	RESN	58A7
R667	RESN	58A7
R668	RESN	58A7
R669	RESN	58A7
R670	RESN	58A6
R671	RESN	58A6
R672	RESN	58A7
R673	RESN	59D8
R674	RESN	59D5
R675	RESN	59D6
R676	RESN	59D6
R677	RESN	59C3
R678	RESN	59C1
R679	RESN	59D7
R680	RESN	60B7
R681	RESN	60B5
R682	RESN	60A5
R683	RESN	60A1
R684	RESN	60A5
R685	RESN	60A1
R688	RESN	62A2
R689	RESN	62A3
R692	RESN	63B6
R693	RESN	63A6
R694	RESN	63A3
R695	RESN	63B3
R697	RESN	65C3
R700	RESN	65A4
R702	RESN	65B6
R704	RESN	66C3
R708	RESN	66B6
R709	RESN	66A4
R735	RESN	41A8
R740	RESN	11C7
R747	RESN	41B6
R748	RESN	47C6
R749	RESN	47C6
R750	RESN	47D5
R751	RESN	47D5
R752	RESN	47D8
R753	RESN	51C3
R754	RESN	51C2
R755	RESN	51D3
R756	RESN	51D3
R757	RESN	53A4
R758	RESN	53A3
R759	RESN	56D5
R760	RESN	60B2
R761	RESN	60B5
R763	RESN	14A2
R764	RESN	14A4
R765	RESN	60B4
R766	RESN	60B7

R768	RESN	48A4
R770	RESN	48A4
R771	RESN	48A4
R772	RESN	49B3
R773	RESN	49B5
R774	RESN	49B4
R775	RESN	12A4
R776	RESN	10D6
R777	RESN	69D4
R778	RESN	69D3
R779	RESN	69C3
R780	RESN	69C3
R781	RESN	69C3
R782	RESN	69C3
R788	RESN	69B2
R789	RESN	69B2
R790	RESN	70D1
R792	RESN	70D3
R793	RESN	70D3
R794	RESN	70D4
R797	RESN	55B2
R798	RESN	23C3
R799	RESN	23C2
R800	RESN	24D2
R801	RESN	25B7
R803	RESN	25B7
R804	RESN	25B7
R805	RESN	27D2
R806	RES	29D6
R807	RES	29D7
R808	RES	29D7
R809	RES	29D7
R812	RES	29A6
R813	RESN	55D5
R814	RESN	55C2
R815	RESN	55B2
R816	RESN	55B7
R817	RESN	55C5
R818	RESN	55B2
R819	RESN	55B2
R824	RESN	7A7
R828	RESN	7A7
R835	RESN	7A6
R838	RESN	9A4
R841	RESN	12C3
R843	RESN	13C3
R894	RESN	51B7
R895	RESN	51B7
R896	RESN	51C7
R897	RESN	51B4
R898	RESN	51B5
R899	RESN	51D5
R900	RESN	56A6
R908	RESN	70D1
R909	RESN	70C7
R910	RESN	70C8
R920	RESN	39C2
R923	RESN	12A3
R924	RESN	12A3
R925	RESN	12A3
R926	RESN	13A3
R927	RESN	13A4
R928	RESN	13A4
R929	RESN	51D8
R930	RESN	51D4
R931	RESN	51D4
R932	RESN	53C7
R933	RESN	53C2
R934	RESN	56A5
R935	RESN	56A4
R936	RESN	56D3
R937	RESN	56A2
R938	RESN	56C1
R939	RESN	56B4
R948	RESN	12A5
R949	RESN	51C7
R951	RESN	51C7
R952	RESN	51C7
R953	RESN	51C7
R954	RESN	51C7
R955	RESN	51B5
R956	RESN	47C5
R957	RESN	47B5
R958	RESN	51D5
R959	RESN	51C7

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```
R960  RESN      52A7
R961  RESN      52A4
R962  RESN      52A7
R963  RESN      53C7
R965  RESN      33D6
R966  RESN      33D7
R967  RESN      34D7
R968  RESN      34D6
R969  RESN      35D7
R970  RESN      35D6
R971  RESN      36D7
R972  RESN      36D6
R973  RESN      37D7
R974  RESN      37D6
R976  RESN      48A4
R977  RESN      25C6
R978  RESN      29C6
R996  RESN      23B4
R997  RESN      24B3
R998  RESN      24B3
R999  RESN      27B4
R1000 RESN      28B2
R1001 RESN      28B2
R1002 RESN      28B2
R1003 RESN      28B2
R1005 RESN      23C4
R1006 RESN      27C3
R1007 RESN      62A4
R1008 RESN      62A2
R1009 RESN      62A4
R1010 RESN      62A2
R1011 RESN      62A7
R1012 RESN      63A4
R1013 RESN      63A4
R1016 RESN      48A7
R1017 RESN      48A1
R1018 RESN      69D6
R1019 RESN      69B7
R1020 RESN      69C8
R1021 RESN      49A3
R1022 RESN      49A2
R1026 RESN      9A5
R1032 RESN      69C8
R1033 RESN      69C8
R1035 RESN      7C7
R1036 RES       7B4
R1037 RESN      7B6
R1038 RESN      7B6
R1039 RESN      7A4
R1040 RESN      7A5
R1042 RES       28C4
R1043 RESN      29A5
R1044 RESN      40C7
R1047 RESN      48B3
R1048 RESN      24C3
R1050 RES       29A6
R1051 RES       29A6
R1053 RESN      53C7
R1502 RESN      39C4
R2000 RESN      49C4
R2001 RESN      49D6
R2002 RESN      49C6
R2003 RESN      49C5
R2005 RESN      49C5
R2006 RESN      18A5
R2008 RESN      22D5
R2011 RESN      51B8
R2012 RESN      41A2
R2013 RESN      41A2
R2014 RESN      41A1
R2015 RESN      28D2
R3033 RESN      50C5
R3079 RESN      31A1
R3125 RESN      13B1
R3148 RESN      44C1
R3157 RESN      12B1
R3217 RESN      42D4
R3348 RESN      11C2
R3379 RESN      11C7
R3401 RESN      31B1
R3402 RESN      31B1
R3403 RESN      31B1
R3404 RESN      31B1
R3799 RESN      27C3
R4000 RESN      31D3
```

```
R4001 RESN      31D3
R4002 RESN      31C3
R4003 RESN      31C3
R4004 RESN      31B1
R4005 RESN      31A1
R4006 RESN      31A1
R4007 RESN      31A1
R4008 RESN      32A5
R4009 RESN      32A5
R4010 RESN      32A5
R4011 RESN      32A5
RP1   RPAK4C-4R 49A6
RP2   RPAK4C-4R 49A6
RP5   RPAK4C-4R 6D7 6D8
RP7   RPAK4C-4R 6D3 6D4
RP9   RPAK4C-4R 31A5
RP10  RPAK4C-4R 31A1
RP13  RPAK4C-4R 15D7
RP14  RPAK4C-4R 15D7
RP15  RPAK4C-4R 15C7 15D7
RP16  RPAK4C-4R 15C7
RP17  RPAK4C-4R 15C7
RP18  RPAK4C-4R 15B7
RP19  RPAK4C-4R 15B7
RP20  RPAK4C-4R 15B7
RP21  RPAK4C-4R 15A7
RP22  RPAK4C-4R 15A7
RP23  RPAK4C-4R 15A7
RP24  RPAK4C-4R 15D5
RP25  RPAK4C-4R 15D5
RP26  RPAK4C-4R 15C5
RP27  RPAK4C-4R 15C5
RP28  RPAK4C-4R 15C5
RP29  RPAK4C-4R 15B5
RP30  RPAK4C-4R 15B5
RP31  RPAK4C-4R 15A5 15B5 15B5
RP32  RPAK4C-4R 15A5
RP33  RPAK4C-4R 15A5
RP34  RPAK4C-4R 15A5
RP35  RPAK4C-4R 15D2
RP66  RPAK4C-4R 19B4 19C4
RP67  RPAK4C-4R 19B7 19C7
RP68  RPAK4C-4R 19D2
RP69  RPAK4C-4R 19D7
RP70  RPAK4C-4R 19C7 19C7 19D7 19D7
RP71  RPAK4C-4R 19C7
RP72  RPAK4C-4R 19C7
RP73  RPAK4C-4R 19B7
RP74  RPAK4C-4R 19B7
RP75  RPAK4C-4R 19A7
RP76  RPAK4C-4R 19A7
RP77  RPAK4C-4R 19A7
RP78  RPAK4C-4R 19D4
RP79  RPAK4C-4R 19D4
RP80  RPAK4C-4R 19C4 19D4
RP81  RPAK4C-4R 19C4
RP82  RPAK4C-4R 19C4
RP83  RPAK4C-4R 19B4
RP84  RPAK4C-4R 19B4
RP85  RPAK4C-4R 19A4
RP86  RPAK4C-4R 19A4
RP87  RPAK4C-4R 19A4
RP88  RPAK4C-4R 19D7
RP119 RPAK4C-4R 31A5
RP120 RPAK4C-4R 31D5
RP121 RPAK4C-4R 31C5
RP122 RPAK4C-4R 31C5
RP123 RPAK4C-4R 31B7 31C7
RP124 RPAK4C-4R 31C7
RP125 RPAK4C-4R 31C7
RP126 RPAK4C-4R 31C7 31C7 31D7 31D7
RP127 RPAK4C-4R 31A7
RP128 RPAK4C-4R 31A7
RP129 RPAK4C-4R 31B7
RP130 RPAK4C-4R 31B7
RP131 RPAK4C-4R 31D7
RP132 RPAK4C-4R 31B5 31C5
RP133 RPAK4C-4R 31B5
RP134 RPAK4C-4R 31B5
RP135 RPAK4C-4R 31A5
RP136 RPAK4C-4R 31B1
RP137 RPAK4C-4R 31C1
RP138 RPAK4C-4R 31D3
RP140 RPAK4C-4R 31B3
RP141 RPAK4C-4R 31C1
```

```
RP142 RPAK4C-4R 31C1 31D1 31D1
RP144 RPAK4C-4R 31D1
RP145 RPAK4C-4R 31C3
RP146 RPAK4C-4R 31C3
RP147 RPAK4C-4R 31B3 31C3
RP148 RPAK4C-4R 31B3
RP149 RPAK4C-4R 31A3
RP150 RPAK4C-4R 31A3
RP153 RPAK4C-4R 32A1 32B1
RP154 RPAK4C-4R 32B1
RP155 RPAK4C-4R 32D4
RP156 RPAK4C-4R 32C4
RP157 RPAK4C-4R 32B4
RP158 RPAK4C-4R 32C1
RP159 RPAK4C-4R 32C1
RP160 RPAK4C-4R 32C1
RP161 RPAK4C-4R 32D1
RP162 RPAK4C-4R 32C4
RP163 RPAK4C-4R 32C4
RP164 RPAK4C-4R 32B4
RP165 RPAK4C-4R 32B4
RP166 RPAK4C-4R 32A4
RP167 RPAK4C-4R 32A4
RP168 RPAK4C-4R 32B1
RP169 RPAK4C-4R 32A1
RP170 RPAK4C-4R 32A5
RP171 RPAK4C-4R 32B5
RP172 RPAK4C-4R 32A7
RP173 RPAK4C-4R 32A7
RP174 RPAK4C-4R 32B7
RP175 RPAK4C-4R 32B7
RP176 RPAK4C-4R 32C7
RP177 RPAK4C-4R 32C7
RP178 RPAK4C-4R 32C5
RP179 RPAK4C-4R 32C5
RP180 RPAK4C-4R 32C5
RP181 RPAK4C-4R 32B5
RP182 RPAK4C-4R 32B7
RP183 RPAK4C-4R 32C7
RP184 RPAK4C-4R 32D7
RP185 RPAK4C-4R 32B5
RP186 RPAK4C-4R 32A5
RP196 RPAK4C-4R 38D4 38D4 38D5 38D5
RP197 RPAK4C-4R 40B7 40B8
RP198 RPAK4C-4R 44D1
RP199 RPAK4C-4R 44C1 44D1
RP200 RPAK4C-4R 44C1
RP201 RPAK4C-4R 44B1 44C1
RP202 RPAK4C-4R 44B1
RP203 RPAK4C-4R 44B1
RP204 RPAK4C-4R 44A1
RP205 RPAK4C-4R 54A2
RP206 RPAK4C-4R 54B4
RP207 RPAK4C-4R 54A7
RP208 RPAK4C-4R 54B5 54B6
RP209 RPAK4C-4R 54B7
RP210 RPAK4C-4R 54B7
RP211 RPAK4C-4R 54B6
RP212 RPAK4C-4R 54B5
RP213 RPAK4C-4R 18D7
RP214 RPAK4C-4R 18D3
RP215 RPAK4C-4R 18D5
RP216 RPAK4C-4R 18D5
RP217 RPAK4C-4R 18C5 18D5
RP218 RPAK4C-4R 18C5
RP219 RPAK4C-4R 18C5
RP220 RPAK4C-4R 18A5
RP221 RPAK4C-4R 18A5
RP222 RPAK4C-4R 18A5
RP223 RPAK4C-4R 18A5 18B5
RP224 RPAK4C-4R 18B5
RP225 RPAK4C-4R 18B5
RP226 RPAK4C-4R 18B5
RP227 RPAK4C-4R 18B5 18C5
RP228 RPAK4C-4R 18C5
RP229 RPAK4C-4R 18B7
RP230 RPAK4C-4R 18B7 18C7
RP231 RPAK4C-4R 18C7
RP232 RPAK4C-4R 18C7
RP233 RPAK4C-4R 18C7
RP234 RPAK4C-4R 18D7
RP235 RPAK4C-4R 18D7
RP236 RPAK4C-4R 18A7
RP237 RPAK4C-4R 18A7
RP238 RPAK4C-4R 18A7
```

```
RP239 RPAK4C-4R 18A7
RP240 RPAK4C-4R 18A7 18B7
RP241 RPAK4C-4R 18B7
RP242 RPAK4C-4R 18B7
RP243 RPAK4C-4R 22A5 22B5
RP244 RPAK4C-4R 22A5
RP245 RPAK4C-4R 22A5
RP246 RPAK4C-4R 22A5
RP247 RPAK4C-4R 22A5
RP248 RPAK4C-4R 22B5
RP249 RPAK4C-4R 22B5
RP250 RPAK4C-4R 22B5
RP251 RPAK4C-4R 22B5 22C5
RP252 RPAK4C-4R 22C5
RP253 RPAK4C-4R 22C5
RP254 RPAK4C-4R 22C5
RP255 RPAK4C-4R 22D7
RP256 RPAK4C-4R 22D5
RP257 RPAK4C-4R 22D5
RP258 RPAK4C-4R 22D7
RP259 RPAK4C-4R 22C7 22D7
RP260 RPAK4C-4R 22C7
RP261 RPAK4C-4R 22C7
RP262 RPAK4C-4R 22C7
RP263 RPAK4C-4R 22B7
RP264 RPAK4C-4R 22B7
RP265 RPAK4C-4R 22B7
RP266 RPAK4C-4R 22B7
RP267 RPAK4C-4R 22A7
RP268 RPAK4C-4R 22A7
RP269 RPAK4C-4R 22A7
RP270 RPAK4C-4R 22A7
RP271 RPAK4C-4R 22A7
RP277 RPAK4C-4R 56C1
RP279 RPAK4C-4R 58A3 58A4
RP280 RPAK4C-4R 62A7
RP282 RPAK4C-4R 60B8
RP283 RPAK4C-4R 54D7 54D8 54D8
RP288 RPAK4C-4R 70A2 70B2
RP289 RPAK4C-4R 70B2
RT1   FUSE_SMT   43D3
RT2   FUSE_SMT   43C3
RT3   FUSE_SMT   64D6
RT4   FUSE_SMT   64D3
RT5   THERMISTOR 54D7
S8    SWSPST_PB_SM 41A7
S9    SWSPST_PB_SM 48A5
SP1   SPKR       42B3
SW1   SWSPST_PB_SM 72B2
U1    LTC1929    47B7
U2    BANIAS_HS 4B3 4C7 4D3 5C4 5D2 5D5 5D7
U3    QS3384     72A6
U4    SC1470     68B6
U5    MOSFETN_8P 68B5
U8    EPM7064    72C4
U9    LED_DISPLAY_10P 72D4
U10   LED_DISPLAY_10P 72C2
U11   NE1617A    7D2
U12   MBT3904DUAL 42B3
U14   P64H2A     23D5 24D5 25D3 26C6 26D6
U15   P64H2A     27D5 28D5 29C3 30D6 30D7
U16   QS3384     49B7
U17   QS3384     49A7
U18   LT1761     48C3
U44   LTC1735_1 48D7
U45   ICH3       39D5 40D3 41D3 42D7
U54   69000      45D5 46D4
U56   LPC47B27   53D5
U57   74LVC00A   49A3 49A4 71B3 71C3
U59   LTC1326    48A7
U60   ICS932S203A 51C6
U61   GD75232S   54D2
U64   AT93C66    59C1
U65   H5007      58B4
U66   E7501      10D4 11D4 12D5 13D5 14D3 14D5 14D6
U68   74HCT125   39A5 39A7 43B7 71C4
U69   FWH_8M     52D4
U70   TLV431A    62A2
U71   TLV431A    62A4
U72   74LVC14    48A2 48B2 71D5
U76   OSC_PWR    63A5
U78   AIC_7902A 59D4 60C2 60D6 61C1 61D6 62D5
U79   82544EI    56C2 56C7 57D2 57D6
U82   74LVC08AD 7B4 49B4
U83   LT1764_DPAK 63B3
```

```
U84   LT1118_ADJ 63B7
U93   DS2119M    65C7
U94   DS2119M    65C4
U95   DS2119M    65C2
U96   DS2119M    66C7
U97   DS2119M    66C4
U98   DS2119M    66C2
U101  AT93C46    56D4
U103  LM2904     47C6
U104  FAN5066    47D6
U113  74ACT04    49B6 69B6 70C7 70D2 70D7 71C5
U115  LTC1735_1 55C5
U119  LT1587CM1_5 57A4
U121  74CBT3306 69C5
U122  74CBT3306 69B5 69C5
U123  74CBT3306 69B5
U124  74CBT3306 69D5
U125  74HCT4052 69C7
U126  74AHC74   7B5 7C6
U3003 SC1476    50C4
U3008 MBT3904DUAL 42C3
Y1    XTAL4P    41B7
Y2    CRYSTAL   51D8
Y3    CRYSTAL   56B1
```

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