Intel® 855GME Chipset and Intel® 82801DB I/O Controller Hub (ICH4) Embedded Platform

For use with the Intel® Pentium® M Processor, Intel® Pentium® M Processor on 90 nm process with 2 MB L2 cache, and the Intel® Celeron® M Processor

Platform Design Guide

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Revision History

Date	Revision	Description
January 2007	007	Updated Table 2., Reference Documents.
September 2006	006	Revised 1.5V / 3.3V power sequencing for ICH4.
October 2005	005	-Updated related document references with current URLs. -Added references to documentation needed for this document. -Clarified feature listings to accurately reflect the latest supported features and products. -Updated section 6.2 references to 18bit LVDS support. -Small consistency changes made throughout the document. -Revised stackup description and diagram in Chapter 3 to conform with a reference platform.
August 2004	004	Added support for Intel® Pentium® M Low Voltage 738 Processor.
June 2004	003	Added support for the Intel Pentium M processor on the 90 nm process with 2 MB L2 cache
February 2004	002	ICH4 updates
October 2003	001	Initial release of this document.

Introduction 1

This design guide provides Intel's design recommendations for systems based on the Intel® Pentium M processor, Intel® Pentium M processor on the 90 nm process with 2 MB L2 cache, and the Intel® Celeron® M Processor. This document contains design recommendations, board schematics, and a system checklist. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues.

The Intel reference schematics may be used as a reference for board designers. Contact your local Intel representative for the latest revision of the customer reference schematics. While the schematics should cover specific designs, the core schematics remain the same for most Intel 855GME chipset platforms.

The Pentium M processor in the 478-pin package with the Intel 855GME chipset delivers a high-performance embedded platform solution. The processor and chipset support a 400 MHz source synchronous Pentium M processor system bus using a split-transaction, deferred-reply protocol. Table 1 presents conventions and terminology used in this document.

Note: Unless otherwise noted, all design considerations for the Intel Pentium M processor may also be used for the Intel Pentium M processor on the 90 nm process with 2 MB L2 cache or the Intel Celeron M Processor. Refer to the *Intel® Pentium® M Processor Datasheet*, *Intel® Pentium® M Processor on the 90 nm Process with 2 MB L2 Cache Datasheet*, and the *Intel® Celeron® M Processor Datasheet* for detailed processor information.

1.1 Terms and Definitions

Table 1. Terms and Definitions (Sheet 1 of 2)

Term	Definition
AC	Audio Codec
ADD	AGP Digital Display
AMC	Audio/Modem Codec
Anti-etch	Any plane-split, void or cutout in a V_{CC} or GND plane is referred to as an anti-etch.
ASF	Alert Standards Format
BER	Bit Error Rate
CMC	Common Mode Choke
CRB	Customer Reference Board
CRT	Cathode Ray Tube
DAC	Digital-to-Analog Converter
DVO	Digital Video Out
EMI	Electro Magnetic Interference
ESD	Electrostatic Discharge
FS	Full Speed – Refers to USB 1.1 Full Speed

Table 1. Terms and Definitions (Sheet 2 of 2)

Term	Definition
FSB	Pentium M/Celeron M Front Side Bus - Processor to GMCH interface
FWH	Firmware Hub – A non-volatile memory device used to store the system BIOS.
GMCH	Graphics Memory Controller Hub
HS	High Speed – Refers to USB 2.0 High Speed
ICH4	Intel® 82801DB I/O Controller Hub 4 (ICH4): Fourth generation I/O controller hub
LCI	LAN Connect Interface
LOM	LAN on Motherboard
LPC	Low Pin Count
LS	Low Speed – Refers to USB 1.0 Low Speed.
LVDS	Low Voltage Digital Signaling
MC	Modem Codec
micro FC-BGA	Micro Flip Chip Ball Grid Array
micro FC-PGA	Micro Flip Chip Pin Grid Array
PCM	Pulse Code Modulation
PLC	Platform LAN Connect
RTC	Real Time Clock
SMBus	System Management Bus – A two-wire interface through which various system components may communicate.
SPD	Serial Presence Detect
STD	Suspend-To-Disk
STR	Suspend-To-Ram
TCO	Total Cost of Ownership
TDM	Time Division Multiplexed
TDR	Time Domain Reflectometry
USB	Universal Serial Bus
VRM	Voltage Regulator Module

1.2 Reference Documents

Table 2 lists reference documents.

Table 2. Reference Documents (Sheet 1 of 2)

Document	Document Number/Source
82562ET 10/100 Mbps Platform LAN Connect (PLC) Product Datasheet	Contact Your Intel Field Representative
AC'97 Specification, Revision 2.3	http://www.intel.com/labs/media/audio/#97spec23
Advanced Configuration and Power Interface Specification (ACPI), Revision 2a	http://www.acpi.info/spec.htm
Application Note AP-728: ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions	http://www.intel.com/design/chipsets/applnots/292276.htm
CK-408 Clock Synthesizer/Driver Specification, Revision 1.0 or later	Contact Your Intel Field Representative
Communication and Networking Riser (CNR) Specification, Revision 1.2	http://developer.intel.com/technology/cnr/index.htm
ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions (Application Note AP-728)	http://developer.intel.com/design/chipsets/applnots/
Intel CK-SSC Spread Spectrum Clock Specification	Contact Your Intel Field Representative
Intel® 82801DB I/O Controller Hub (ICH4) Datasheet	http://www.intel.com/design/chipsets/datashts/290744.htm
Intel® 82801DB I/O Controller Hub (ICH4): Thermal and Mechanical Design Guidelines	http://www.intel.com/design/chipsets/designex/298651.htm
Intel® 855GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet	http://www.intel.com/design/chipsets/datashts/252615.htm
Intel® 855GME Chipset Graphics and Memory Controller Hub (GMCH) Specification Update Addendum (for embedded designs only)	http://developer.intel.com/design/intarch/specupdt/274004.htm
Intel® Celeron® M Processor Datasheet	http://www.intel.com/design/mobile/datashts/300302.htm
Intel® Celeron® M Processor Specification Update	http://developer.intel.com/design/mobile/specupdt/300303.htm
Intel® DDR 200 JEDEC Spec Addendum	http://developer.intel.com
Intel® DDR 200/266/333 JEDEC Specification Addendum	http://www.intel.com/technology/memory/ddr/specs/ddr200-266-333_spec_addend_rev1.pdf
Intel® Pentium® M Processor Datasheet	http://www.intel.com/design/mobile/datashts/252612.htm
Intel® Pentium® M Processor Specification Update	http://developer.intel.com/design/intarch/specupdt/252665.htm
Intel® Pentium® M Processor on the 90 nm Process with 2 MB L2 Cache Datasheet	http://developer.intel.com/design/mobile/datashts/302189.htm
Intel® Pentium® M Processor on the 90 nm Process with 2 MB L2 Cache Specification Update	http://developer.intel.com/design/mobile/specupdt/302209.htm
Intel® Pentium® M Processor on the 90 nm Process with 2 MB L2 Cache for Embedded Applications Thermal Design Guide	http://developer.intel.com/design/intarch/designgd/302231.htm

Table 2. Reference Documents (Sheet 2 of 2)

Document	Document Number/Source
ITP700 Debug Port Design Guide	http://www.intel.com/design/Xeon/guides/249679.htm
JEDEC 184-Pin Unbuffered DDR DIMM Specification	Contact Your Intel Field Representative
JEDEC Double Data Rate (DDR) SDRAM Specification	Contact Your Intel Field Representative
JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification	Contact Your Intel Field Representative
Low Pin Count Interface Specification	http://www.intel.com/design/chipsets/industry/lpc.htm
PCI Bus Power Management Interface Specification	www.pcisig.com
PCI Local Bus Specification	www.pcisig.com
PCI-PCI Bridge Specification	www.pcisig.com
SMBUS Specification, Revision 2.0	http://www.smbus.org/specs/
Ultra Low Voltage Intel® Celeron® M Processor at 600 MHz Addendum to the Intel® Celeron® M Processor Datasheet	http://www.intel.com/design/intarch/datashts/301753.htm
ULV Intel® Celeron® M Processor at 600 MHz for Embedded Applications Thermal Design Guide	http://developer.intel.com/design/intarch/designgd/302288.htm
Universal Serial Bus Revision 2.0 Specification	http://www.usb.org/developers/docs/

System Overview 2

The Intel® 855GME chipset is a Graphics Memory Controller Hub (GMCH) component for embedded platforms. It provides the processor interface, system memory interface (DDR SDRAM), hub interface, CRT, LVDS, and a DVO interface. It is optimized for the Pentium® M processor and the Intel® 82801DB I/O Controller Hub 4 (ICH4).

The accelerated hub architecture interface (the chipset component interconnect) is designed into the chipset to provide an efficient, high-bandwidth communication channel between the GMCH and the ICH4.

An ACPI-compliant Intel 855GME chipset embedded platform may support the Full-On (S0), Power On Suspend (S1-M), Suspend to RAM (S3), Suspend to Disk (S4), and Soft-Off (S5) power management states. Through the use of an appropriate LAN device, the chipset also supports wake-on LAN* for remote administration and troubleshooting. The chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true plug-and-play for the platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC’97 allows the OEM to use software-configurable AC’97 audio and modem coder/decoders (codecs) instead of the traditional ISA devices.

2.1 Terminology

For this document, the following terminology applies.

- *Pentium M processor* refers to either the Intel® Pentium® M processor on the 0.13-micron process or Intel Pentium M processor on the 90 nm process with 2 MB L2 cache.
- *Celeron M processor* refers to the Intel® Celeron® M processor.
- *82855GME* refers to Intel’s mobile Graphics Memory Controller Hub (GMCH) optimized for the Intel Pentium M and Intel Celeron M processors.
- ICH4 refers to the Intel® 82801DB I/O Controller Hub 4.

2.2 System Features

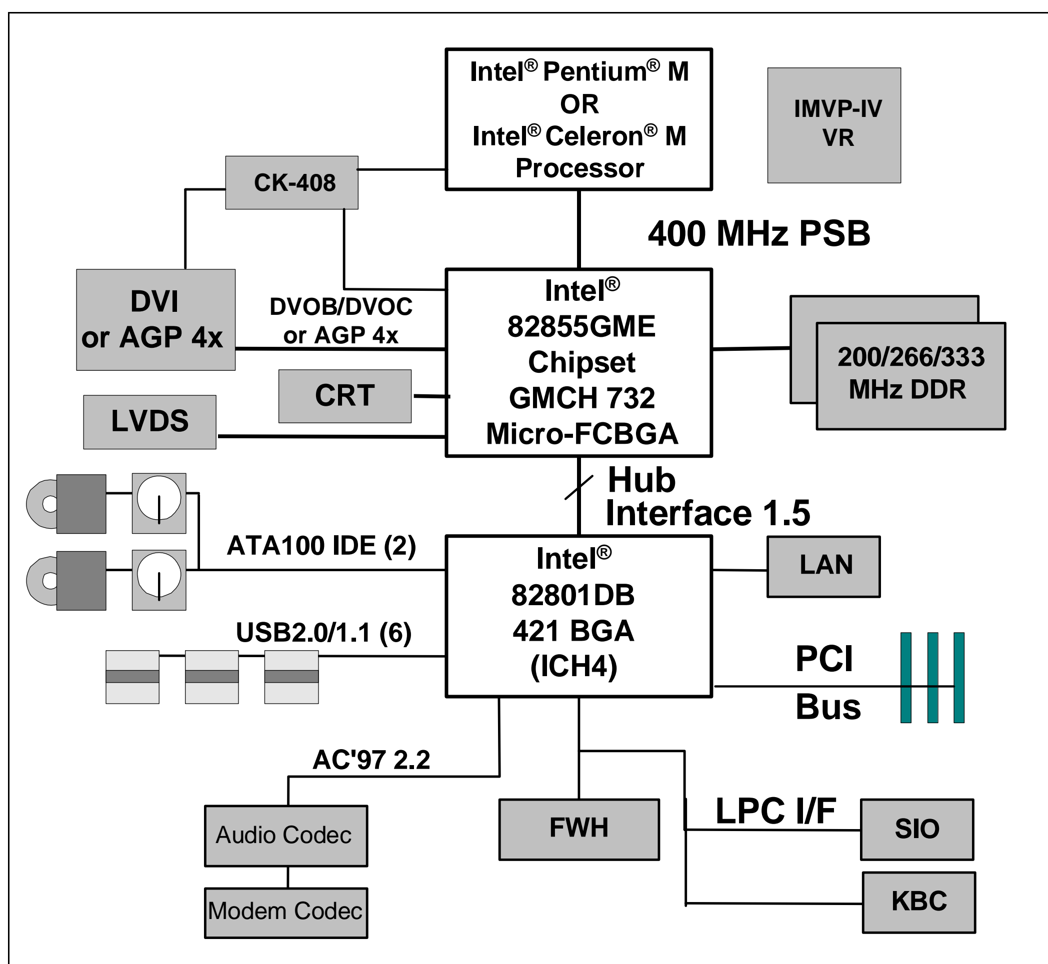
The Pentium M processor is a high performance, low power processor with several microarchitectural enhancements over existing Intel low-power processors. Some key features of the Pentium M processor microarchitecture include dynamic execution, data pre-fetch logic, 400 MHz source-synchronous Front Side Bus (FSB), on-die 1 MB L2 cache with advanced transfer cache architecture, streaming SIMD extensions 2 (SSE2), and Enhanced Intel SpeedStep® technology.

The Pentium M Processor on the 90 nm Process with 2 MB L2 cache provides additional enhancements to the Intel Pentium M processor by doubling the L2 cache size to 2 MB and being fabricated on Intel’s latest 90 nm process technology. Other microarchitectural enhancements on the processor also extend the performance while keeping power dissipation low.

The Intel Celeron M processor is a low power value processor incorporating similar microarchitecture as the Intel Pentium M processor.

The Intel 855GME chipset contains two core components: the GMCH and the ICH4. The GMCH integrates a 400 MHz Pentium M processor front side bus controller, integrated graphics controller hub, integrated LVDS interface, two digital video out ports multiplexed with an AGP 4x controller, a 200/266/333 MHz DDR-SDRAM controller, and a high-speed accelerated hub architecture interface for communication with the ICH4 (Hub Interface 1.5). The ICH4 integrates an Ultra ATA 100/66/33 controller, USB host controller that supports the USB 1.1 and USB 2.0 specification, LPC interface, FWH Flash BIOS interface controller, PCI interface controller, AC'97 digital controller and a hub interface for communication with the GMCH. Figure 1 illustrates the embedded Intel® 855GME chipset system block diagram.

Figure 1. Embedded Intel® 855GME Chipset System Block Diagram



2.3 Component Features

2.3.1 Pentium® M Processor

2.3.1.1 Architectural Features

- On-die primary 32 Kbyte instruction cache and 32 Kbyte write-back data cache
- On-die 1 Mbyte second-level cache
- Supports Streaming SIMD Extensions 2 (SSE2)
- Assisted Gunning Transceiver Logic (AGTL+) bus driver technology
- Enhanced Intel SpeedStep® technology to enable real-time dynamic switching between multiple voltage and frequency points
- Supports host bus Dynamic Bus Inversion (DINV)
- Dynamic power-down of data bus buffers
- BPRI# control to disable address/control buffers

2.3.1.2 Packaging/Power

- 478-pin micro FC-PGA and 479-ball micro FC-BGA packages (removed pin on the micro FC-PGA package is used solely for mechanical distinction between the Pentium M/Celeron M and previous generation processors)
- $V_{CC\text{-}CORE}$: 1.484 V (highest frequency mode) to 0.956 V (lowest frequency mode); V_{CCA} (1.8 V); V_{CCP} (1.05 V)

2.3.2 Intel Pentium M Processor on the 90 nm Process with 2 MB L2 Cache

All features of the Intel Pentium M processor are supported by the Intel Pentium M Processor on the 90 nm process with 2 MB L2 cache. The processors also utilize the same package and footprint. This section only lists the additional on-die enhancements. For more details, see the *Intel Pentium M Processor on the 90 nm Process with 2 MB L2 Cache Datasheet.*

New features on the Intel Pentium M Processor on the 90 nm process with 2 MB L2 cache include:

- On-die 2 MB second level cache
- Strained silicon process technology

Voltage and power changes include:

- Intel Pentium M processor 745 (90 nm, 2 MB L2 Cache, 1.8 GHz, 400 MHz FSB):
  - $V_{CC\text{-}CORE\ (HFM)}$: 1.276V – 1.340
  - $V_{CC\text{-}CORE\ (LFM)}$: 0.988V
  - V_{CCA}: 1.8V only
  - TDP: 21 W

- Intel Pentium M processor Low Voltage 738 (90 nm, 2 MB L2 Cache, 1.4 GHz, 400 MHz FSB):
  - $V_{CC-CORE\ (HFM)}$: 1.052V
  - $V_{CC-CORE\ (LFM)}$: 0.956V
  - V_{CCA}: 1.8V and 1.5V supported
  - TDP: 10 W

2.3.3 Intel® Celeron® M Processor

Most features of the Intel Pentium M processor are supported by the Intel Celeron M Processor. For more details, see the *Intel Celeron M Processor Datasheet*.

Processor Features:

- Pin compatible with the Intel Pentium M Processor.
- 1.3 GHz operation, available in 478-pin micro FCPGA and 479-ball micro FCBGA packages
- On-die 512 Kbytes second-level cache
- Voltage/Power Changes:
  - $V_{CC-CORE}$ for 1.3GHz: 1.356V
  - TDP for 1.3GHz = 24.5 W
- No support for Enhanced Intel SpeedStep® technology, Deeper Sleep operation, or Intel® Thermal Monitor 2.

2.3.4 Intel® Celeron® M Processor on 90nm process

Most features of the Intel Pentium M processor on 90 nm process with 2 MB L2 cache are supported by the Intel Celeron M processor on 90nm process. For more details, see the *Intel® Celeron® M Processor Datasheet on 90 nm process Datasheet.*

- Intel Celeron M Processor 370 (90 nm, 1.5 GHz, 400 MHz FSB):
  - On-die 1-MB L2 Cache
  - TDP = 21 W
  - VCCA: 1.8 V and 1.5 V supported only
- Intel Celeron M Processor Ultra Low Voltage 373 (90 nm, 1.0 GHz, 400 MHz FSB):
  - On-die 512-KB L2 Cache
  - TDP = 5.5 W
  - VCCA: 1.8 V and 1.5 V supported

2.3.5 ULV Intel® Celeron® M Processor at 600 MHz

Most features of the Intel Celeron M processor are supported by the ULV Intel Celeron M at 600 MHz processor. For more details, see the *Ultra Low Voltage Intel® Celeron® M Processor at 600*

MHz Addendum to the Intel® Celeron® M Processor Datasheet.

- Intel Celeron M Processor Ultra Low Voltage at 600 MHz (130 nm, 600 MHz, 400 MHz FSB):
  - On-die 512-KB L2 Cache
  - TDP = 7 W
  - VCC-CORE: 1.004 V
  - VCCA: 1.8 V supported
  - 479-ball micro FCBGA package

2.3.6 Intel® 855GME Chipset Graphics Memory Controller Hub (GMCH)

2.3.6.1 Intel® Pentium® M Processor/Intel Celeron M Processor FSB Support

- Optimized for Intel Pentium M processor/Intel Celeron M processor in 478-pin Micro-FCPGA and 479-ball micro-FCBGA package
- AGTL+ bus driver technology with integrated GTL termination resistors (gated AGTL+ receivers for reduced power)
- Supports 32-bit AGTL+ bus addressing (no support for 36-bit address extension)
- Supports uniprocessor systems
- 400-MHz, source-synchronous FSB
- 2X Address, 4X Data

2.3.6.2 Integrated System Memory DRAM Controller

- Supports up to two double-sided SO-DIMMs or DIMMs (four rows populated), unbuffered
- PC1600/PC2100/PC2700 DDR-SDRAM (with or without ECC)
- Supports 64-Mbit, 128-Mbit, 256-Mbit, and 512-Mbit technologies for x8 and x16 width devices
- Maximum of 1 Gbyte of system memory with 512-Mbit technology devices; maximum of 2 Gbytes of system memory with high-density 512-Mbit technology devices
- Supports 200-MHz, 266-MHz, and 333-MHz DDR devices
- 64-bit data interface (72-bit with ECC) Supports up to 16 simultaneous open pages
- Support for SO-DIMM Serial Presence Detect (SPD) scheme via SMBus interface
- S3 power management support via self refresh mode using CKE

2.3.6.3 Internal Graphics Controller

- Graphics Core Frequency
  - Display/Render frequency up to 250 MHz (with 1.35 V core voltage)
- 3D Graphics Engine
  - 3D Setup and Render Engine
  - Zone Rendering
  - High-quality performance Texture Engine
- Analog Display Support
  - 350-MHz integrated 24-bit RAMDAC
  - Hardware color cursor support
  - Accompanying I2C and DDC channels provided through multiplexed interface
  - Dual independent pipe for dual independent display
  - Simultaneous display: same images and native display timings on each display device
- Digital Video Out Port (DVOB & DVOC) support
  - DVOB & DVOC with 165-MHz dot clock support for each 12-bit interface
  - Compliant with DVI Specification 1.5
- Dedicated LFP (local flat panel) support
  - Single or dual channel LVDS panel support up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz per channel
  - SSC support of 0.5%, 1.0%, and 2.5% center and down spread with external SSC clock
  - Supports data format of 18 bpp
  - LCD panel power sequencing compliant with SPWG timing specification
  - Compliant with ANSI/TIA/EIA 644-1995 spec
  - Integrated PWM interface for LCD backlight inverter control

- — Bi-linear Panel fitting
- Internal Graphics Features (Intel 855GME chipset)
  - — Core Vcc = 1.2 V or 1.35 V (to support higher graphics core frequency and DDR333)
  - — Graphics core frequency
- Display core frequency at 133 MHz, 200 MHz, 250 MHz
- Render core frequency at 100 MHz, 133 MHz, 166 MHz, 200 MHz, 250 MHz
- Intel® Dual-Frequency Graphics Technology
  - — 3D Graphics Engine
- Enhanced Hardware Binning Instruction Set supported
- Bi-Cubic Filtering supported
- Linear Gamma Blending for Video Mixer Rendering (VMR)
- Video Mixer Rendering (VMR) supported
  - — Graphics Power Management
- Dynamic Core Frequency Switching
- Intel® Smart 2D Display Technology
- Memory Self-Refresh During C3
- Intel® Display Power Saving Technology

2.3.6.4 Package/Power

- 732-pin Micro-FCBGA (37.5 mm x 37.5 mm)
- VTTLF, VTTHF (1.05 V)
- VCC, VCCASM, VCCHL, VCCAHPLL, VCCAGPLL, VCCADPLLA, VCCADPLLB (1.2 V or 1.35 V; as needed to support 250 MHz graphics core frequency and DDR333)
- VCCADAC, VCCDVO, VCCDLVDS, VCCALVDS (1.5 V)
- VCCSM, VCCQSM, VCCTXLVDS (2.5 V)
- VCCGPIO (3.3 V)
- Power Management (Intel 855GME chipset)
  - — Optimized Clock Gating for 3D and Display Engines
  - — On-die thermal sensor

2.3.6.5 Multiplexed AGP 4x and Intel® DVO Interface

The 855GME GMCH multiplexes an AGP 4x interface with two Intel DVOs. The DVO ports can each support a single channel DVO device. If both ports are active in single channel mode, they will have identical display timings and data. Alternatively, the DVO ports can combine to support dual channel devices supporting higher resolutions and refresh rates. When an external AGP device is installed in the system, all internal graphics driver (IGD) functionality are disabled.

2.3.6.6 Accelerated Graphics Port (AGP) Interface

- Supports AGP 2.0 data transfers
- Supports a single AGP (1X/2X/4X) device (either via a connector or on the motherboard)
- Only supports 1.5 V VDDQ for AGP electricals
- PCI semantic (FRAME# initiated) accesses to DRAM are snooped
- AGP semantic (PIPE# and SBA) traffic to DRAM is not snooped on the PSB and is therefore not coherent with the CPU caches
- High priority access support
- Delayed transaction support for AGP reads that cannot be serviced immediately
- AGP Busy/Stop Protocol support
- Support for D3 Hot and Cold Device states
- AGP Clamping and Sense Amp control

2.3.6.7 Packaging/Power

- 732-pin micro FC-BGA (37.5 mm x 37.5 mm)
- V_{TTLF}, V_{TTHF} (1.05 V); V_{CC}, V_{CCASM}, V_{CCHL}, $V_{CCAHPLL}$, $V_{CCAGPLL}$, $V_{CCADPLLA}$, $V_{CCADPLLB}$ (1.2 V); V_{CCADAC}, V_{CCDVO}, $V_{CCDLVDS}$, $V_{CCALVDS}$, (1.5 V); V_{CCSM}, V_{CCQSM}, $V_{CCTXLVDS}$ (2.5 V); V_{CCGPIO} (3.3 V)

2.3.7 Intel® 82801DB I/O Controller Hub 4 (ICH4)

- Upstream accelerated hub architecture interface for access to the GMCH
- PCI 2.2 interface (six PCI request/grant pairs)
- Bus master IDE controller (supports Ultra ATA 100/66/33)
- USB 1.1 and USB 2.0 host controllers
- I/O APIC
- SMBus 2.0 Controller
- FWH Interface
- LPC Interface
- AC’97 2.2 Interface
- Alert-On-LAN*
- IRQ Controller

2.3.7.1 Packaging/Power

- 421-pin, BGA package (31 mm x 31 mm)
- V_{CC}1_5 (1.5 V main logic voltage); V_{CCSUS}1_5 (1.5 V resume logic voltage); V_{CCLAN}1_5 (1.5 V LAN logic voltage); V_{CC}3_3 (3.3 V main I/O voltage); V_{CCSUS}3_3 (3.3 V resume I/O voltage); V_{CCLAN}3_3 (3.3 V LAN I/O voltage); $V5_{REF}$ (5 V); $V5_{REF_SUS}$ (5 V); V_{CCRTC}; V_{CCHI} (1.5 V); V_{CCP} (1.05 V)

2.3.8 Firmware Hub (FWH)

- An integrated hardware Random Number Generator (RNG) on Intel specific parts
- Register-based locking
- Hardware-based locking
- Five GPIs

2.3.8.1 Packaging/Power

- 32-pin TSOP/PLCC
- 3.3 V core and 3.3 V/12 V for fast programming

General Design Considerations 3

This section documents motherboard layout and routing guidelines for the Intel® 855GME chipset platforms. It does not discuss the functional aspects of any bus or layout guidelines for an add-in device.

When the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, Intel recommends that critical signals be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e., 55 Ω ± 15%) is the nominal trace impedance for a 5 mil wide external trace and a 4 mil wide internal trace. However, some stack-ups may lead to narrower or wider traces on internal or external layers to meet the 55 Ω impedance target; that is, the impedance of the trace when not subjected to fields created by changing current in neighboring traces.

Note: The trace impedance target assumes that the trace is not subjected to the EM fields created by changing current in neighboring traces. It is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces when calculating flight times. Using wider spaces between the traces can minimize trace-to-trace coupling and reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, follow the routing guidelines documented in this section. Also, all high-speed, impedance controlled signals (e.g., Pentium® M processor/Celeron® M processor FSB signals) must have continuous GND referenced planes and cannot be routed over or under power/GND plane splits.

3.1 Nominal Board Stack-up

The Intel 855GME chipset-based platforms require a board stack-up yielding a target impedance of 55 Ω ± 15%. Figure 2 illustrates an example of an 8-layer board stack-up. The left side of the figure illustrates the starting dimensions of the metal and dielectric material thickness as well as drawn trace width dimensions prior to lamination, conductor plating, and etching. After the motherboard materials are laminated, conductors plated, and etched, somewhat different dimensions result. Dielectric materials become thinner, under/over etching of conductors alters their trace width, and conductor plating makes them thicker.

Note: For the purpose of extracting electrical models from transmission line properties, the final dimensions of signals after lamination, plating, and etching should be used.

The stack-up uses 1.2-mil (1 oz.) copper on power planes to reduce I*R drops and 0.6-mil copper thickness on the outer signal layers: primary side layer (L1), and secondary side layer (L8). Additionally, 1.2-mil copper thickness is used on the internal signal layers: Layer 3 (L3), and Layer 6 (L6). After plating, the external layers become 1.2 to 2 mils thick.

To ensure impedance control of 55 Ω, the primary and secondary side layer microstrip lines should reference solid ground planes on Layer 2 and Layer 7, respectively.

Figure 2. Recommended Board Stack-up Dimensions

Stackup		Dielectric Thickness (mills)	Layer No.	Layer Type	Copper Weight (oz)	Trace Width (mils)	Trace Impedance (ohms)
			1	SIGNAL	1/2+plating	5	55
PREPREG	>	3					
			2	PLANE	1		
CORE	>	5					
			3	SIGNAL	1	4	55
PREPREG	>	5					
			4	PLANE	1		
CORE	>	28					
			5	PLANE	1		
PREPREG	>	5					
			6	SIGNAL	1	4	55
CORE	>	5					
			7	PLANE	1		
PREPREG	>	3					
			8	SIGNAL	1/2+plating	5	55

Internal signal traces on Layer 3 and Layer 6 are unbalanced striplines. To meet the nominal 55 Ω characteristic impedance for these traces, they reference a solid ground plane on Layer 2 and Layer 7. In the remaining sections of the motherboard layout, Layer 4 and Layer 5 are used for power delivery.

The secondary side layer (L8) is also used for power delivery in many cases since it benefits from the thick copper plating of the external layer plating as well as referencing the Layer 7 ground plane. The benefit of such a stack-up is low inductance power delivery.

3.2 Alternate Stack-Ups

Designers may choose to use different stack-ups (number of layers, thickness, trace width, etc.) from the example outlined in Figure 2. However, the following key elements should be observed:

1. Final post lamination, post etching, and post plating dimensions should be used for electrical model extractions.
2. Power plane layers should be 1 oz. thick and the outer signal layers should be ½ oz. thick, while the internal signal layers shall be 1 0z. thick. External layers become 1 – 1.5 oz. (1.2 – 2 mils) thick after plating.
3. All high-speed signals should reference solid ground planes through the length of their routing and should not cross plane splits. To ensure this, both planes surrounding striplines should be GND.
4. Intel recommends that high-speed signal routing be done on internal, stripline layers.
5. For high-speed signals transitioning between layers next to the component, the signal pins should be accounted for by the GND stitching vias that would stitch all the GND plane layers in that area of the motherboard. Due to the arrangement of the processor and the GMCH pin-maps, GND vias placed near all GND lands are also very close to high-speed signals that may be transitioning to an internal layer. Thus, no additional ground stitching vias (besides the GND pin vias) are required in the immediate vicinity of the processor and GMCH package to accompany the signal transitions from the component side into an internal layer.
6. High-speed routing on external layers should be minimized to avoid EMI. Routing on external layers also introduces different delays compared to internal layers. This makes it extremely difficult to do length matching when some routing is done on both internal and external layers.
7. When Intel’s recommended stack-up guidelines are not used, the designer is liable for all aspects of their board design, i.e., understanding impacts of signal integrity (SI) and power distribution.

Pentium® M Processor/Celeron® M Processor FSB Design and Power Delivery Guidelines 4

The following layout guidelines support designs using the Pentium® M processor/Celeron® M processor and the Intel® 855GME chipset Graphics Memory Controller Hub (82855GME). Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the motherboard for most FSB signals. A simple point-to-point interconnect topology is used in these cases.

4.1 Pentium® M Processor/Celeron® M Processor FSB Design Recommendations

For proper operation of the Pentium M processor/Celeron M processor and the GMCH FSB interface, it is necessary that the system designer meet the timing and voltage specification of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation that make assumptions that may differ from an OEM's system design. The most accurate way to understand the signal integrity and timing of the Pentium M processor/Celeron M FSB in your platform is by performing a comprehensive simulation analysis. It is possible that adjustments to trace impedance, line length, termination impedance, board stack-up, and other parameters may be made that improve system performance.

Refer to the latest *Intel® Pentium® M Processor Datasheet* , *Intel® Celeron® M Processor Datasheet,* or *Intel® Pentium® M Processor on 90nm Process with 2 MB L2 Cache Datasheet* for a FSB signal list, signal types, and definitions.

The following sections provide design recommendations for data, address, and strobes. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate. The following topology and layout guidelines are subject to change. The guidelines are derived from empirical testing with GMCH package models.

4.1.1 Recommended Stack-up Routing and Spacing Assumptions

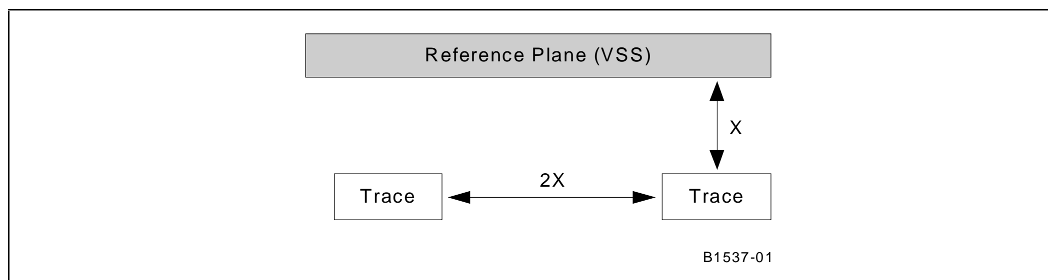
The following section describes in more detail the terminology and definitions used for different routing and stack-up assumptions that apply to Intel's recommended motherboard stack-up described in Section 3.1.

4.1.1.1 Trace to Trace Spacing – Reference Plane Separation Ratio

Figure 3 illustrates Intel's recommended relationship between the edge-to-edge trace spacing (2X) versus the trace-to-reference plane separation (X). An edge-to-edge trace spacing (2X) to trace-reference plane separation (X) ratio of 2:1 ensures a low crosstalk coefficient. The timing and layout guidelines for the processor have been created with the assumption of a 2:1 trace spacing to reference plane ratio. A smaller ratio has an unpredictable impact due to crosstalk.

Figure 3 illustrates the trace spacing versus trace-to-reference plane example.

Figure 3. Trace Spacing versus Trace-to-Reference Plane Example

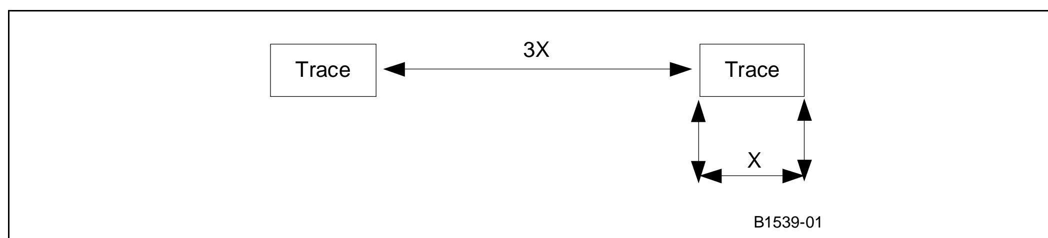


4.1.1.2 Trace Space to Trace Width Ratio

Figure 3 illustrates Intel's recommended relationship between the edge-to-edge trace spacing versus trace width ratio for the best signal quality results. In general, a 3:1 trace space-to-trace width ratio (shown in Figure 4) is preferred. In case of routing difficulties on the motherboard, using a 2:1 ratio would be acceptable **only** if additional simulations conclude that it is possible, which may include some changes to the stack-up or routing assumptions.

Figure 4 illustrates the three-to-one trace spacing-to-trace width example.

Figure 4. Three-to-One Trace Spacing-to-Trace Width Example



4.1.2 Common Clock Signals

All common clock signals use an AGTL+ bus driver technology with on-die integrated GTL termination resistors connected in a point-to-point, Zo = 55 Ω, controlled impedance topology between the processor and the GMCH. No external termination is needed on these signals. These signals operate at the processor FSB frequency of 100 MHz.

Common clock signals should be routed on an internal layer while referencing solid ground planes. Based on current simulation results, routing on internal layers allows for a minimum pin-to-pin motherboard length of one inch and a maximum of 6.5 inches. Trace length matching for the common clock signals is not required. For details on minimum motherboard trace length requirements, refer to Section 4.1.2.1 and Table 3. Intel recommends routing these signals on the

same internal layer for the entire length of the bus. If constraints require routing these signals with a transition to a different layer, a minimum of one ground stitching via for every two signals should be placed within 100 mils of the signal transition vias.

Routing of the common clock signals should use 2:1 trace spacing to trace width. This implies a minimum of 8 mils spacing (i.e., 12 mil minimum pitch) for a 4 mil trace width for routing on internal layers. Practical cases of escape routing under the GMCH or processor package outline and vicinity may not allow the implementation of 2:1 trace spacing requirements. Although every attempt should be made to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the GMCH and the Pentium M processor/Celeron M package outlines and up to 200 – 300 mils outside the package outline.

RESET# (CPURESET# of GMCH) is also a common clock signal but requires a special treatment for the case where an ITP700FLEX debug port is used. Refer to Section 4.1.6 for further details.

Table 3 presents the Pentium M processor/Celeron M processor FSB common clock signal internal layer routing guidelines.

Table 3. Pentium® M Processor/Celeron® M Processor FSB Common Clock Signal Internal Layer Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Spacing Width
CPU	GMCH		Min (mils)	Max (inches)		
ADS#	ADS#	Stripline	997	6.5	55 ± 15%	2:1
BNR#	BNR#	Stripline	1298	6.5	55 ± 15%	2:1
BPRI#	BPRI#	Stripline	1215	6.5	55 ± 15%	2:1
BR0#	BR0#	Stripline	1411	6.5	55 ± 15%	2:1
DBSY#	DBSY#	Stripline	1159	6.5	55 ± 15%	2:1
DEFER#	DEFER#	Stripline	1291	6.5	55 ± 15%	2:1
DPWR#	DPWR#	Stripline	1188	6.5	55 ± 15%	2:1
DRDY#	DRDY#	Stripline	1336	6.5	55 ± 15%	2:1
HIT#	HIT#	Stripline	1303	6.5	55 ± 15%	2:1
HITM#	HITM#	Stripline	1203	6.5	55 ± 15%	2:1
LOCK#	HLOCK#	Stripline	1198	6.5	55 ± 15%	2:1
RS0#	RS0#	Stripline	1315	6.5	55 ± 15%	2:1
RS1#	RS1#	Stripline	1193	6.5	55 ± 15%	2:1
RS2#	RS2#	Stripline	1247	6.5	55 ± 15%	2:1
TRDY#	HTRDY#	Stripline	1312	6.5	55 ± 15%	2:1
RESET#†	CPURESET#	Stripline	1101	6.5	55 ± 15%	2:1

† For topologies where an ITP700FLEX debug port is implemented, refer to Section 4.1.6 for RESET# (CPURESET#) implementation details.

4.1.2.1 Processor Common Clock Signal Package Length Compensation

Trace length matching for the common clock signals is not required. However, package compensation for the common clock signals is required for the minimum board trace. Refer to Table 4 and the example for more details.

Package length compensation should not be confused with length matching. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of compensating for package length variance across a signal group.

All common clock signals are required to meet the minimum pad-to-pad requirement of 2212 mils based on ADS# (as this signal has the longest package lengths). This implies a minimum pin-to-pin motherboard trace length of 997 mils additional motherboard trace will be added to some of the shorter common clock nets on the system board. This trace length is added to meet the longest common clock signal total trace lengths from the die-pad of the processor to the associated die-pad of the chipset.

For example:

ADS# = 997 mils board trace + 454 CPU PKG + 761 GMCH PKG = 2212 pad-to-pad length.

BR0# = X mils board trace + 465 CPU PKG + 336 GMCH PKG = 2212 pad-to-pad length.

Therefore: X = BR0# board trace = 2212 - 365 - 465 = 1411 pin-to-pin length.

Figure 5 illustrates the common clock topology.

Figure 5. Common Clock Topology

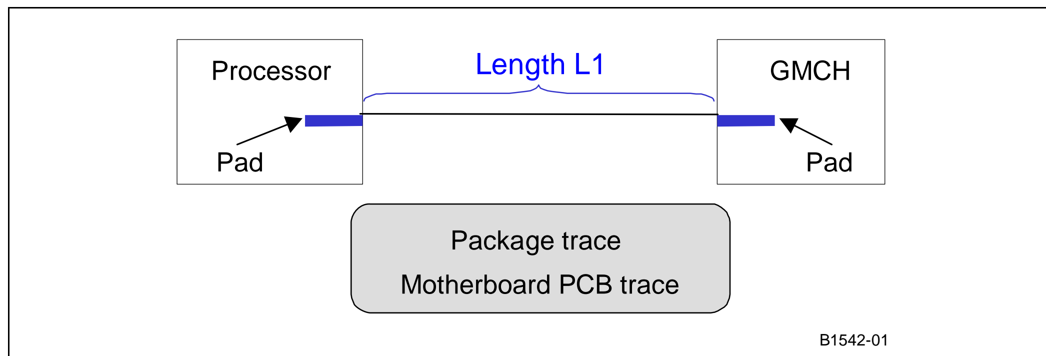


Table 4 presents the processor and GMCH FSB common clock signal length package lengths and minimum board trace lengths.

Table 4. Processor and GMCH FSB Common Clock Signal Package Lengths and Minimum Board Trace Lengths

Signal Names		Package Length		Total Pad-to-Pad Minimum Length Requirements L1 (mils)	Minimum Pin to Pin Routable Board Trace Length (mils)
CPU	GMCH	CPU	GMCH		
ADS#	ADS#	454	761	2212	997
BNR#	BNR#	506	408	2212	1298
BPRI#	BPRI#	424	573	2212	1215
BR0#	BR0#	336	465	2212	1411
DBSY#	DBSY#	445	608	2212	1159
DEFER#	DEFER#	349	572	2212	1291
DPWR#	DPWR#	506	518	2212	1188
DRDY#	DRDY#	529	347	2212	1336
HIT#	HIT#	420	489	2212	1303
HITM#	HITM#	368	641	2212	1203
LOCK#	HLOCK#	499	515	2212	1198
RS0#	RS0#	576	321	2212	1315
RS1#	RS1#	524	495	2212	1193
RS2#	RS2#	451	514	2212	1247
TRDY#	HTRDY#	389	511	2212	1312
RESET#	CPURESET#	455	656	2212	1101

4.1.3 Source Synchronous Signals General Routing Guidelines

All source synchronous signals use an AGTL+ bus driver technology with on-die GTL termination resistors connected in a point-to-point, Zo = 55 Ω controlled impedance topology between the Pentium M processor/Celeron M processor and the GMCH. No external termination is needed on these signals. The source synchronous Pentium M processor/Celeron M processor FSB address signals operate at a double-pumped rate of 200 MHz, while the source synchronous processor FSB data signals operate at a quad-pumped rate of 400 MHz. High-speed operation of the source synchronous signals requires careful attention to their routing considerations. Adhere to the following guidelines to ensure robust high-frequency operation of these signals.

Source synchronous data and address signals and their associated strobes are partitioned into groups of signals. Flight time skew minimization within the same group of source synchronous signals is a key parameter that allows their high-frequency (400 MHz) operation. All the source synchronous signals that belong to **the same group** should be routed on **the same internal layer** for the entire length of the bus. It is permissible to split different groups of source synchronous signals between different motherboard layers as long as all the signals that belong to that group are kept on the same layer. Grouping of the Pentium M processor/Celeron M processor FSB source synchronous signals is summarized in Table 5 and Table 7. This practice results in a significant

reduction of the flight time skew because the dielectric thickness, line width, and velocity of the signals are uniform across a single layer of the stack-up. The relationship of dielectric thickness, line width, and velocity between layers cannot be ensured.

Source synchronous signals should be routed as a stripline on an internal layer with complete reference to ground planes both above and below the signal layer. Routing with references to split planes or power planes other than ground is **not** allowed. For Intel's recommended stack-up example as shown in Figure 2, source synchronous Pentium M processor/Celeron M processor FSB signals are routed on Layer 3 and Layer 6. Layer 2 and Layer 7 are solid grounds across the entire motherboard. However, this is not sufficient because significant coupling exists between signal Layer 3 and power plane Layer 4 as well as signal Layer 6 and power plane Layer 5. To ensure complete ground referencing, Layer 4 and Layer 5 are converted to ground plane floods in the areas where source synchronous processor FSB signals are routed. In addition, all ground plane areas are stitched with ground vias in the vicinity of the Pentium M processor/Celeron M processor and Intel 855GME chipset package outlines with the vias of the ground pins of the Pentium M processor/Celeron M processor and Intel 855GME chipset pin-map.

Note: If the trace impedance can be controlled to within ± 10 percent, the FSB data signals can be routed using 2:1 spacing guidelines. The strobes, however, must still be routed with 3:1 spacing.

Figure 6 illustrates a motherboard layout and a cross-sectional view of Intel's recommended stack-up of the Pentium M processor/Celeron M processor FSB source synchronous DATA and ADDRESS signals referencing ground planes on both Layer 7 and Layer 5.

Note: In the socket cavity of the Pentium M processor/Celeron M processor, Layer 5 and Layer 6 are used for V_{CC} core power delivery. However, outside the socket cavity, Layer 6 signals are routed on top of a solid Layer 7 ground plane. Layer 5 is converted to a ground flood under the shadow of the Pentium M processor/Celeron M processor FSB signals routing between the Pentium M processor/Celeron M processor and GMCH. Stitching of all the GND planes is provided by the ground vias in the pin map of the Pentium M processor/Celeron M processor and GMCH.

Figure 6. Layer 6 Pentium® M Processor/Celeron® M Processor FSB Source Synchronous Signals GND Referencing to Layer 5 and Layer 7 Ground Planes

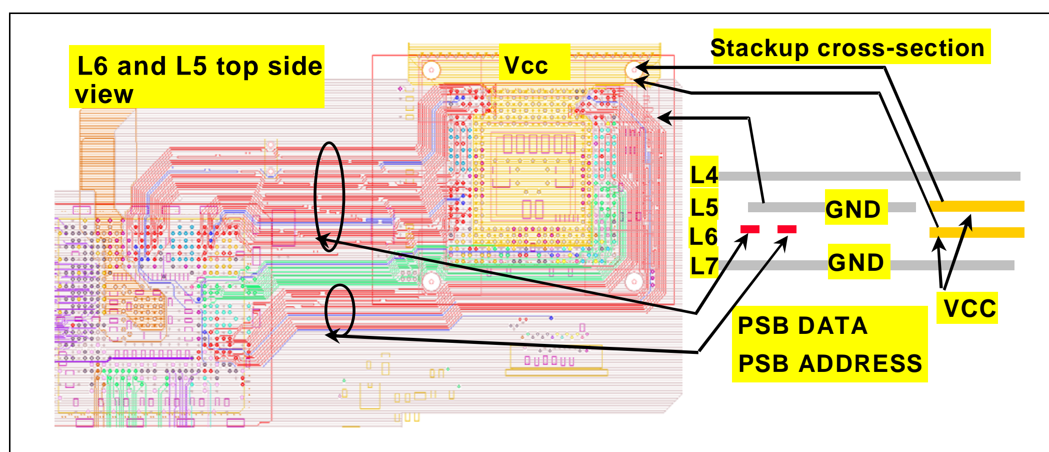


Figure 7 illustrates the Layer 6 Pentium M processor/Celeron M processor FSB source synchronous data signals.

Figure 7. Layer 6 Pentium® M Processor/Celeron® M Processor FSB Source Synchronous Data Signals

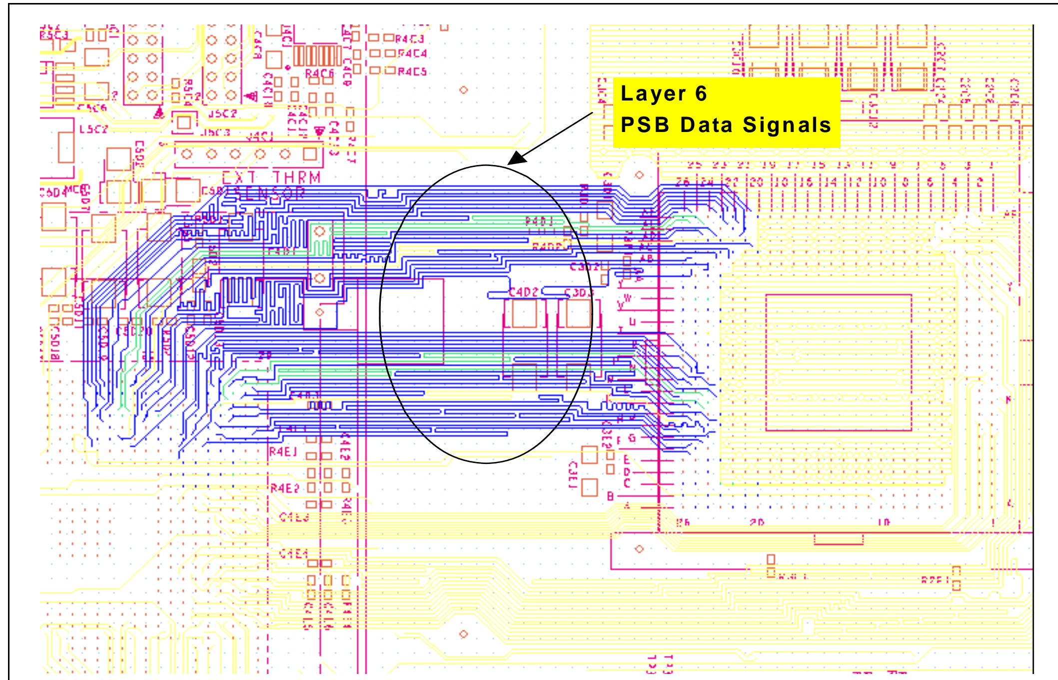
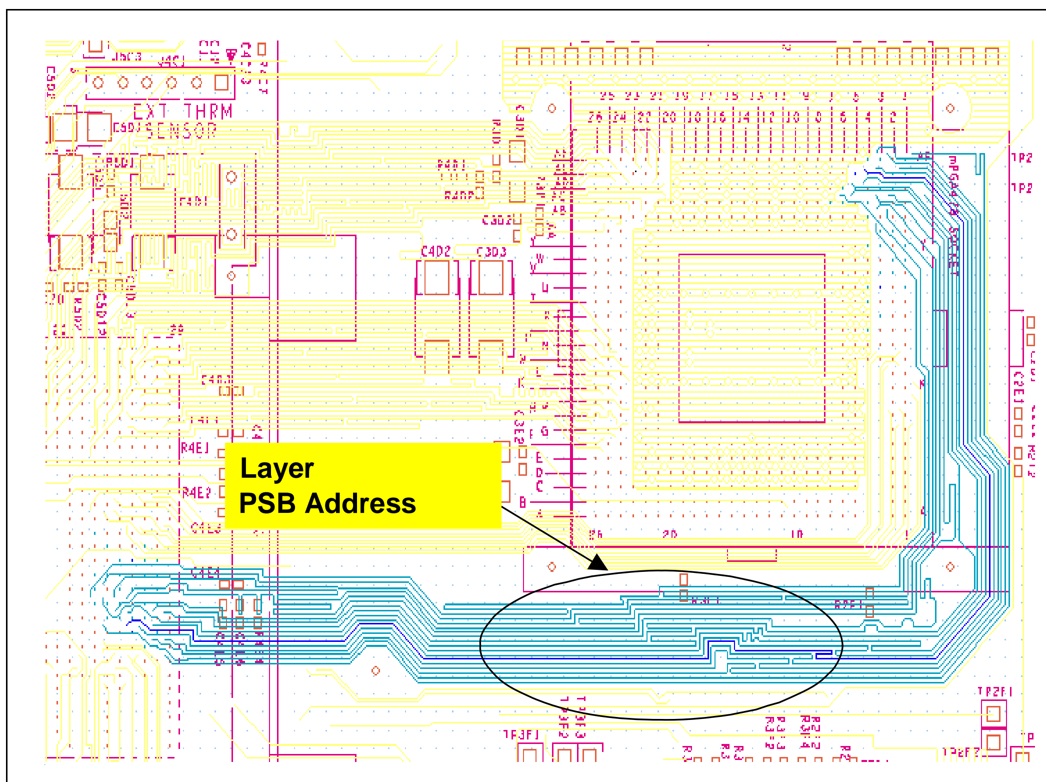


Figure 8 illustrates the Layer 6 Pentium M processor/Celeron M processor FSB source synchronous address signals.

Figure 8. Layer 6 Pentium® M Processor/Celeron® M Processor FSB Source Synchronous Address Signals



In a similar way, Figure 9 illustrates Intel's recommended layout and stack-up example of how another group of Pentium M processor/Celeron M processor FSB source synchronous Data and Address signals may reference ground planes on both Layer 2 and Layer 4.

Note: In the socket cavity of the Pentium M processor/Celeron M processor, Layer 3 is used for V_{CC} core power delivery to reduce the I*R drop. However, outside of the socket cavity Layer 3 signals are routed below a solid Layer 2 ground plane. Layer 4 is converted to a ground flood under the shadow of the Pentium M processor/Celeron M processor FSB signals routing between the Pentium M processor/Celeron M processor and GMCH. Figure 10 and Figure 11 show example routing for Intel customer reference board.

Figure 9 illustrates the Layer 3 Pentium M processor/Celeron M processor FSB source synchronous signals ground referencing to Layer 2 and Layer 4 ground planes.

Figure 9. Layer 3 Pentium® M Processor/Celeron® M Processor FSB Source Synchronous Signals GND Referencing to Layer 2 and Layer 4 Ground Planes

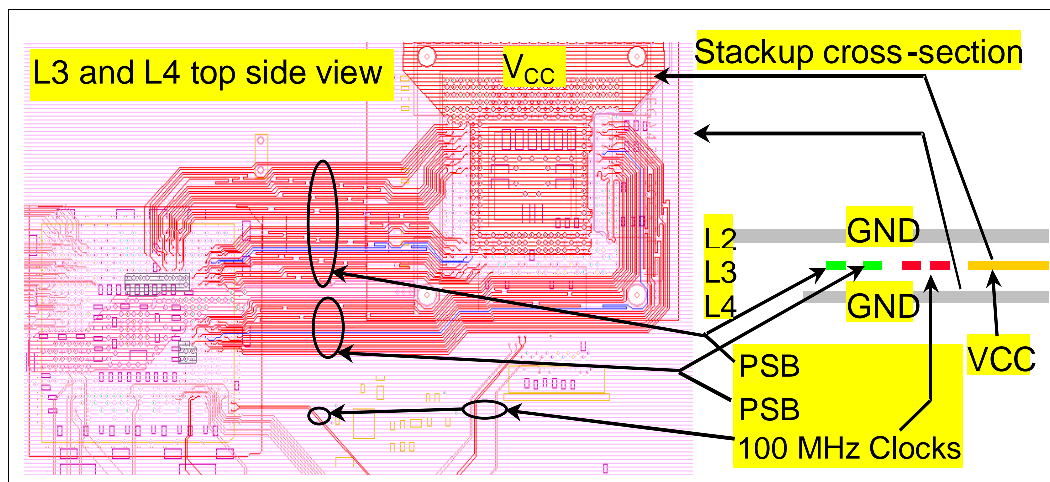


Figure 10 illustrates the Layer 3 Pentium M processor/Celeron M processor FSB source synchronous data signals.

Figure 10. Layer 3 Pentium® M Processor/Celeron® M Processor FSB Source Synchronous Data Signals

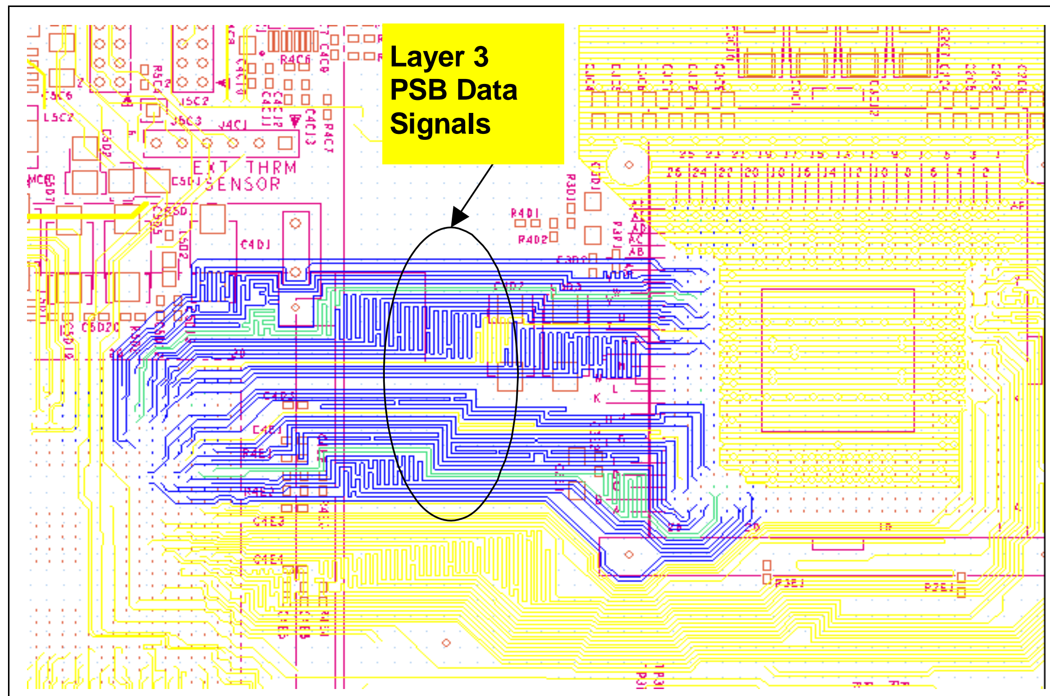
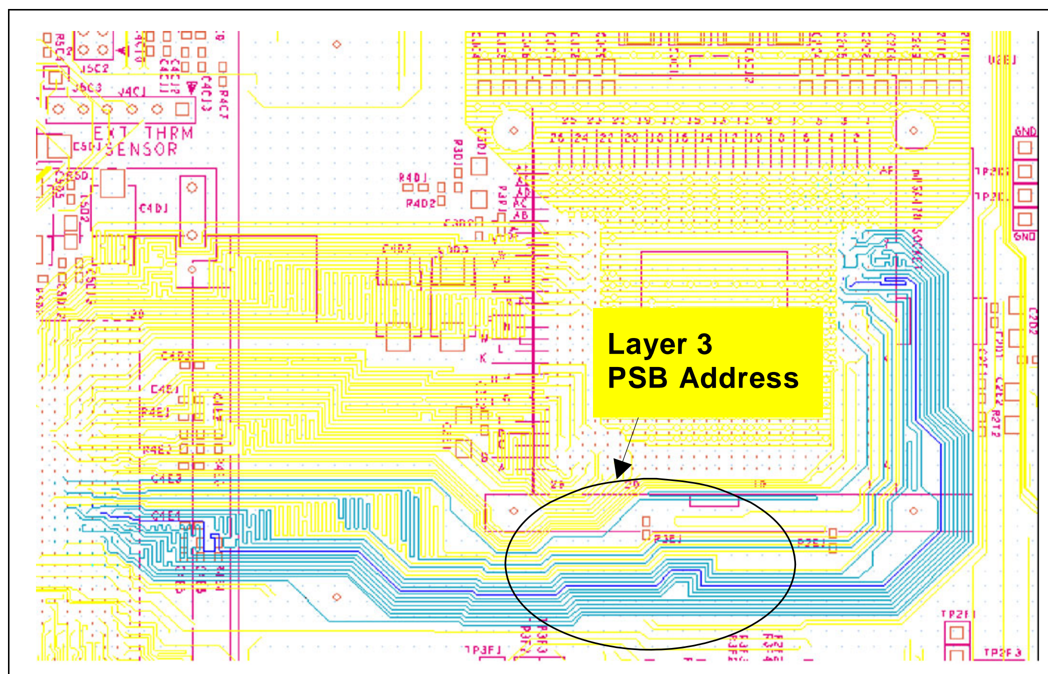


Figure 11 illustrates the Layer 3 Pentium M processor/Celeron M processor FSB source synchronous address signals.

Figure 11. Layer 3 Pentium® M Processor/Celeron® M Processor FSB Source Synchronous Address Signals



4.1.3.1 Source Synchronous Length-Matching Constraints

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, all of which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables are more restrictive length-matching requirements called length-matching constraints. These additional requirements further restrict the minimum-to-maximum length range of each signal group with respect to strobe, within the overall boundaries defined in the guideline tables, as required to guarantee adequate timing margins. The amount of minimum-to-maximum length variance allowed for each group around the strobe reference length varies from signal group to signal group depending on the amount of timing variation that may be tolerated.

4.1.3.2 Package Length Compensation

The Pentium M processor/Celeron M processor package length does not need to be accounted for in the motherboard routing since the Pentium M processor/Celeron M processor has the source synchronous signals and the strobes length matched within the group inside the package routing. However, trace length matching of the GMCH package length **does** need to be accounted for in the motherboard routing because the package does not have the source synchronous signals and the strobes length matched within the group inside the package routing. Refer to Table 9 for the Pentium M processor/Celeron M processor and Intel 855GME chipset package lengths. Skew minimization requires Intel 855GME chipset die-pad to Pentium M processor/Celeron M processor pin (pad-to-pin) trace length matching of the Pentium M processor FSB source synchronous signals belong to the same group including the strobe signals of that group.

Package length compensation should not be confused with length matching. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting package length variance across a signal group. There is some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length-matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

4.1.3.3 Source Synchronous – Data Group

Robust operation of the 400 MHz, source synchronous data signals require tight skew control. For this reason, these signals are split into matched groups as outlined in Table 5. All the signals within the same group should be kept on the same layer of motherboard routing and should be routed to the same pad to pin length within ±100 mils of the associated strobes. Only the Pentium M processor/Celeron M processor has the package trace equalization for signals within each data and address group. The GMCH does not have the package trace equalization for signals within each data and address group. See Table 9 for the package lengths. Refer to Section 4.1.2.1 for trace length and package compensation requirements. The two complementary strobe signals associated with each group should be length matched (pad-to-pin) to each other within ± 25 mils and tuned to the average length of the data signals (pad-to-pin) of their associated group. This will optimize setup/hold time margin. Current simulation results provide routing guidelines using 3:1 spacing for the FSB source synchronous data and strobe signals. This implies a minimum of 12 mil spacing (i.e., 16 mil minimum pitch) for a four mil trace width. Practical cases of escape routing under the GMCH or the processor package outline and vicinity may not even allow the implementation of 2:1 trace spacing requirements. Although every attempt should be made to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the GMCH and the processor package outlines and up to 200 – 300 mils outside the package outline. The benefits of additional spacing include increased signal quality and voltage margining. The trace routing and length-matching requirements are noted in Section 4.1.3.1 to Section 4.1.3.5.

Note: If trace impedance can be controlled to within ± 10 percent, the FSB data signals can then be routed using 2:1 spacing guidelines. The strobes, however, must still be routed with 3:1 spacing.

Table 5 presents the Pentium M processor/Celeron M processor FSB data source synchronous signal trace length mismatch mapping.

Table 5. Pentium® M Processor/Celeron® M processor FSB Data Source Synchronous Signal Trace Length Mismatch Mapping

Data Group	DINV Signal for Associated Data Group	Signal Matching	Data Strobes Associated with the Group	Strobe Matching	Notes
D[15:0]#	DINV0#	± 100 mils	DSTBP0#, DSTBN0#	± 25 mils	1, 2
D[31:16]#	DINV1#	± 100 mils	DSTBP1#, DSTBN1#	± 25 mils	1, 2
D[47:32]#	DINV2#	± 100 mils	DSTBP2#, DSTBN2#	± 25 mils	1, 2
D[63:48]#	DINV3#	± 100 mils	DSTBP3#, DSTBN3#	± 25 mils	1, 2

NOTES:
1. Strobes of the same group should be trace length matched to each other within ± 25 mils and to the average length of their associated data signal group.
2. All length-matching formulas are based on GMCH die-pad to Pentium M processor/Celeron M processor pin total length per byte lane. Package length tables are provided for all signals to facilitate this pad-to-pin matching.

Table 6 lists the source synchronous data signal general routing requirements. Due to the 400 MHz high-frequency operation, the data signals should be limited to a pin-to-pin trace length minimum of 0.50 inch and maximum of 5.5 inches.

Table 6. Pentium® M Processor/Celeron M Processor System Bus Source Synchronous Data Signal Routing Guidelines

Signal Names				Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Spacing Width
Data Group #1	Data Group #2	Data Group #3	Data Group #4		Min (inches)	Max (inches)		
D[15:0]#	D[31:16]#	D[47:32]#	D[63:48]#	Stripline	0.5	5.5	55 ± 15%	3:1
DINV0#	DINV1#	DINV2#	DINV3#	Stripline	0.5	5.5	55 ± 15%	3:1
DSTBN[0]#	DSTBN[1]#	DSTBN[2]#	DSTBN[3]#	Stripline	0.5	5.5	55 ± 15%	3:1
DSTBP[0]#	DSTBP[1]#	DSTBP[2]#	DSTBP[3]#	Stripline	0.5	5.5	55 ± 15%	3:1

4.1.3.4 Source Synchronous – Address Group

Source synchronous address signals operate at 200 MHz. Thus, their routing requirements are very similar to the data signals. Refer to Section 4.1.3 and Section 4.1.3.3 for further details. Table 7 details the partition of the address signals into matched length groups. Due to the lower operating frequency of the address signals, pad-to-pin length matching is relaxed to ± 200 mils. Each group is associated with only one strobe signal. To maximize setup/hold time margin, the address strobes should be trace length matched to the average trace length of the address signals of their associated group. In addition, each address signal should be trace length matched within ± 200 mils of its associated strobe signal.

Table 7. Pentium® M Processor/Celeron M Processor FSB Address Source Synchronous Signal Trace Length Mismatch Mapping

CPU Signal Name	Signal Matching	Strobe Associated with the Group	Strobe to Associated Address Signal Matching	Notes
REQ[4:0]#, A[16:3]#	± 200 mils	ADSTB0#	± 200 mils	1, 2, 3
A[31:17]#	± 200 mils	ADSTB1#	± 200 mils	1, 2, 3

NOTES:

1. ADSTB[1:0]# should be trace length matched to the average length of their associated address signals group.
2. Each address signal should be trace length matched to its associated address strobe within ± 200 mils.
3. All length-matching formulas are based on GMCH die-pad to Pentium M processor/Celeron M processor pin total length per signal group. Package length tables are provided for all signals to facilitate this pad to pin matching.

Table 8 lists the source synchronous address signal general routing requirements. They should be routed to a pin-to-pin length minimum of 0.50 inches and a maximum of 6.5 inches. Due to the 200 MHz high-frequency operation of the address signals, the routing guidelines listed in Table 8 allow for 2:1 spacing for the address signals given a 55 Ω ± 15% characteristic trace impedance except for address strobe signals. But if space permits, 3:1 spacing is strongly advised for these signals.

Table 8. Pentium® M Processor/Celeron® M Processor FSB Source Synchronous Address Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Spacing Width
Address Group #1	Address Group #2		Min (inches)	Max (inches)		
A[16:3]#	A[31:17]#	Stripline	0.5	6.5	55 ± 15%	2:1
REQ[4:0]#		Stripline	0.5	6.5	55 ± 15%	2:1
ADSTB#[0]	ADSTB#[1]	Stripline	0.5	6.5	55 ± 15%	3:1

4.1.3.5 Pentium® M Processor/Celeron® M Processor and Intel® 855GME Chipset GMCH (82855GME) FSB Signal Package Lengths

Table 9 presents package trace lengths of the Pentium M processor/Celeron M processor and the 82855GME for the source synchronous data and address signals. The Pentium M processor/Celeron M processor FSB package signals within the same group are routed to the same package trace length, but the Intel 855GME chipset package signals within the same group are **not routed** to the same package trace length. As a result, package length compensation is required for GMCH. Refer to Section 4.1.4 for length-matching constraints and Section 4.1.3.2 for package length compensation. The Pentium M processor/Celeron M processor package traces are routed as microstrip lines with a nominal characteristic impedance of 55 Ω ± 15%.

Table 9. Pentium® M Processor/Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 1 of 6)

Signal Group	CPU Signal Name	Pentium® M Processor/Celeron® M Processor Package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Data Group 1	D15#	721	HD15#	554
	D14#	721	HD14#	393
	D13#	721	HD13#	494
	D12#	721	HD12#	620
	D11#	721	HD11#	319
	D10#	721	HD10#	504
	D9#	721	HD9#	438
	D8#	721	HD8#	458
	D7#	721	HD7#	329
	D6#	721	HD6#	518
	D5#	721	HD5#	693
	D4#	721	HD4#	600
	D3#	721	HD3#	387
	D2#	721	HD2#	438
	D1#	721	HD1#	620
	D0#	721	HD0#	329
	DINV[0]#	721	DINV[0]#	514
	DSTBP[0]#	721	HDSTBP[0]#	662
	DSTBN[0]#	721	HDSTBN[0]#	763

Table 9. Pentium® M Processor/Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 2 of 6)

Signal Group	CPU Signal Name	Pentium® M Processor/Celeron® M Processor Package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Data Group 2	D31#	564	HD31#	914
	D30#	564	HD30#	464
	D29#	564	HD29#	691
	D28#	564	HD28#	768
	D27#	564	HD27#	453
	D26#	564	HD26#	815
	D25#	564	HD25#	837
	D24#	564	HD24#	493
	D23#	564	HD23#	766
	D22#	564	HD22#	731
	D21#	564	HD21#	522
	D20#	564	HD20#	714
	D19#	564	HD19#	412
	D18#	564	HD18#	834
	D17#	564	HD17#	634
	D16#	564	HD16#	593
	DINV[1]#	564	DINV[1]#	628
	DSTBP[1]#	564	HDSTBP[1]#	736
	DSTBN[1]#	564	HDSTBN[1]#	787

Table 9. Pentium® M Processor/Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 3 of 6)

Signal Group	CPU Signal Name	Pentium® M Processor/Celeron® M Processor Package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Data Group 3	D47#	661	HD47#	654
	D46#	661	HD46#	647
	D45#	661	HD45#	460
	D44#	661	HD44#	563
	D43#	661	HD43#	726
	D42#	661	HD42#	828
	D41#	661	HD41#	608
	D40#	661	HD40#	358
	D39#	661	HD39#	655
	D38#	661	HD38#	619
	D37#	661	HD37#	747
	D36#	661	HD36#	633
	D35#	661	HD35#	675
	D34#	661	HD34#	683
	D33#	661	HD33#	501
	D32#	661	HD32#	664
	DINV[2]#	661	DINV[2]#	784
	DSTBP[2]#	661	HDSTBP[2]#	502
	DSTBN[2]#	661	HDSTBN[2]#	538

Table 9. Pentium® M Processor/Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 4 of 6)

Signal Group	CPU Signal Name	Pentium® M Processor/Celeron® M Processor Package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Data Group 4	D63#	758	HD63#	579
	D62#	758	HD62#	509
	D61#	758	HD61#	431
	D60#	758	HD60#	522
	D59#	758	HD59#	490
	D58#	758	HD58#	347
	D57#	758	HD57#	649
	D56#	758	HD56#	372
	D55#	758	HD55#	541
	D54#	758	HD54#	598
	D53#	758	HD53#	469
	D52#	758	HD52#	575
	D51#	758	HD51#	326
	D50#	758	HD50#	549
	D49#	758	HD49#	511
	D48#	758	HD48#	372
	DINV[3]#	758	DINV[3]#	431
	DSTBP[3]#	758	HDSTBP[3]#	463
	DSTBN[3]#	758	H DSTBN[3]#	505

Table 9. Pentium® M Processor/Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 5 of 6)

Signal Group	CPU Signal Name	Pentium® M Processor/Celeron® M Processor Package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Address Group 1	REQ4#	616	HREQ4#	276
	REQ3#	616	HREQ3#	383
	REQ2#	616	HREQ2#	247
	REQ1#	616	HREQ1#	378
	REQ0#	616	HREQ0#	569
	A16#	616	HA16#	491
	A15#	616	HA15#	375
	A14#	616	HA14#	562
	A13#	616	HA13#	501
	A12#	616	HA12#	522
	A11#	616	HA11#	566
	A10#	616	HA10#	560
	A9#	616	HA9#	327
	A8#	616	HA8#	333
	A7#	616	HA7#	274
	A6#	616	HA6#	523
	A5#	616	HA5#	551
	A4#	616	HA4#	352
	A3#	616	HA3#	468
	ADSTB[0]#	616	HADSTB[0]#	419

Table 9. Pentium® M Processor/Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 6 of 6)

Signal Group	CPU Signal Name	Pentium® M Processor/Celeron® M Processor Package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Address Group 2	A31#	773	HA31#	617
	A30#	773	HA30#	484
	A29#	773	HA29#	558
	A28#	773	HA28#	579
	A27#	773	HA27#	631
	A26#	773	HA26#	556
	A25#	773	HA25#	535
	A24#	773	HA24#	353
	A23#	773	HA23#	382
	A22#	773	HA22#	545
	A21#	773	HA21#	429
	A20#	773	HA20#	414
	A19#	773	HA19#	284
	A18#	773	HA18#	389
	A17#	773	HA17#	457
	ADSTB[1]#	773	HADSTB[1]#	504
Host Clocks	BCLK0	447	BCLK	1138
	BCLK1	447	BCLK#	1145
ITP Signals	BPM[3:0]	593	—	—

4.1.4 Length-Matching Constraints

The routing guidelines presented in the following subsections define Intel’s recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routing lengths for each signal group. These are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, there are more restrictive length-matching requirements called length-matching constraints. These additional requirements further restrict the minimum to maximum length range of each signal group with respect to clock strobe, within the overall boundaries defined in the guideline tables, as required to ensure adequate timing margins.

The amount of minimum to maximum length variance allowed for each group around the clock strobe reference length varies from signal group to signal group depending on the amount of timing variation that may be tolerated. Refer to Table 6 for source synchronous data matching requirements and Table 7 for source synchronous address matching requirements.

4.1.5 Asynchronous Signals

The following sections describe the topologies and layout recommendations for the Asynchronous Open Drain and CMOS signals found on the platform. All Open Drain signals listed in the following sections must be pulled up to V_{CCP} (1.05 V). If any of these Open Drain signals are pulled up to a voltage higher than V_{CCP}, the reliability and power consumption of the processor may be affected. Therefore, it is very important to follow the recommended pull-up voltage for these signals. All signals must meet the AC and DC specifications as documented in the *Intel® Pentium® M Processor Datasheet* , *Intel® Celeron® M Processor Datasheet*, or *Intel® Pentium® M Processor on 90 nm Process with 2 MB L2 Cache Datasheet.*

Table 10 presents the asynchronous AGTL+ nets.

Table 10. Asynchronous AGTL+ Nets

Signal Names	Description	Topology #	CPU I/O Type	Output	Output Buffer Type	Input	Input Power Well
IERR#	Internal error	1A	O	CPU	AGTL+	System Receiver	Vcc_Receiver
FERR#	Floating point error	1B	O	CPU	AGTL+	Intel® 82801DB ICH4	Main I/O (3.3 V)
THRMTRIP#	Thermal sensor	1B	O	CPU	AGTL+	System Receiver	Vcc_Receiver
PROCHOT#	Thermal sensor	1C	O	CPU	AGTL+	System Receiver	Vcc_Receiver
PWRGOOD	System power good	2A	I	ICH4	OD CMOS	CPU	N/A
DPSLP#†	Deep sleep		I			CPU	
LINT0/INTR	Local interrupts	2B	I	ICH4	CMOS	CPU	N/A
LINT1/NMI	Local interrupts	2B	I	ICH4	CMOS	CPU	N/A
SLP#	Sleep	2B	I	ICH4	CMOS	CPU	N/A
STPCLK#	Processor stop clock	2B	I	ICH4	CMOS	CPU	N/A
IGNNE#	Ignore next numeric error	2B	I	ICH4	CMOS	CPU	N/A
SMI#	System management interrupt	2B	I	ICH4	CMOS	CPU	N/A
A20M#	Address 20 mask	2B	I	ICH4	CMOS	CPU	N/A
INIT#	Processor initialize	3	I	ICH4	CMOS	CPU, FWH	N/A, 3.3 V

† Only supported by ICH4 device. When not used, pull-up at CPU with 4.7 KΩ ± 5% resistor at V_{CCP}.

4.1.5.1 Topology 1A: Open Drain (OD) Signals Driven by the Pentium® M Processor – IERR#

The Topology 1A OD signal IERR# should adhere to the following routing and layout recommendations. Table 11 presents the layout recommendations for Topology 1A. The routing guidelines allow the signal to be routed as either microstrip or striplines using 55 Ω ± 15% characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/undershoot reflections on the transmission line. The pull-up voltage for termination resistor Rtt is V_{CCP} (1.05 V). Due to the dependencies on system design implementation, IERR# may be implemented in a number of ways to meet design goals. IERR# may be routed as a test point or to any optional system receiver. Figure 12 illustrates the routing illustration for Topology 1A.

Figure 12. Routing Illustration for Topology 1A

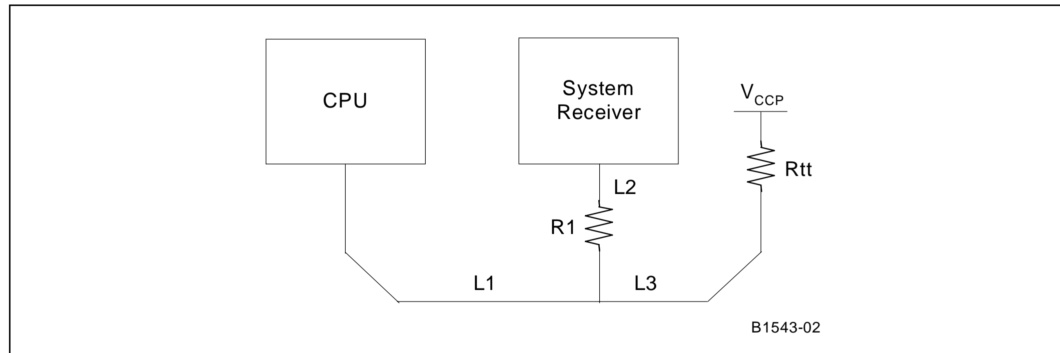


Table 11. Layout Recommendations for Topology 1A

L1	L2	L3	R1	Rtt	Transmission Line Type
0.5 – 12 inches	0 – 3 inches	0 – 3 inches	56 Ω ± 5%	56 Ω ± 5%	Microstrip
0.5 – 12 inches	0 – 3 inches	0 – 3 inches	56 Ω ± 5%	56 Ω ± 5%	Stripline

4.1.5.2 Topology 1B: Open Drain (OD) Signals Driven by the Pentium® M Processor/Celeron® M Processor – FERR# and THERMTRIP#

The Topology 1B OD signals FERR# and THERMTRIP# should adhere to the following routing and layout recommendations. Table 12 presents the layout recommendations for Topology 1B. The routing guidelines allow the signals to be routed as either microstrips or striplines using 55 Ω ± 15% characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/undershoot reflections on the transmission line. The pull-up voltage for termination resistor Rtt is V_{CCP} (1.05 V).

Intel recommends that the FERR# signal of the Pentium M processor/Celeron M processor be routed to the FERR# signal of the ICH4. THERMTRIP# may be implemented in a number of ways to meet design goals. It may be routed to the ICH4 or any optional system receiver. Intel recommends that the THERMTRIP# signal of the Pentium M processor/Celeron M processor be routed to the THERMTRIP# signal of the ICH4. The ICH4's THERMTRIP# signal is a new signal to the I/O controller hub architecture that allows the ICH4 to quickly put the whole system into a S5 state whenever the catastrophic thermal trip point has been reached.

If either FERR# or THERMTRIP# is routed to an optional system receiver rather than the ICH4 and the interface voltage of the optional system receiver does not support a 1.05 V voltage swing, then a voltage translation circuit must be used. If the recommended voltage translation circuit described in Section 4.1.5.7 is used, the driver isolation resistor shown in Figure 18, Rs, should replace the series dampening resistor R1 in Topology 1B. Thus R1 is no longer required in such a topology. Figure 13 illustrates the routing illustration for Topology 1B.

Figure 13. Routing Illustration for Topology 1B

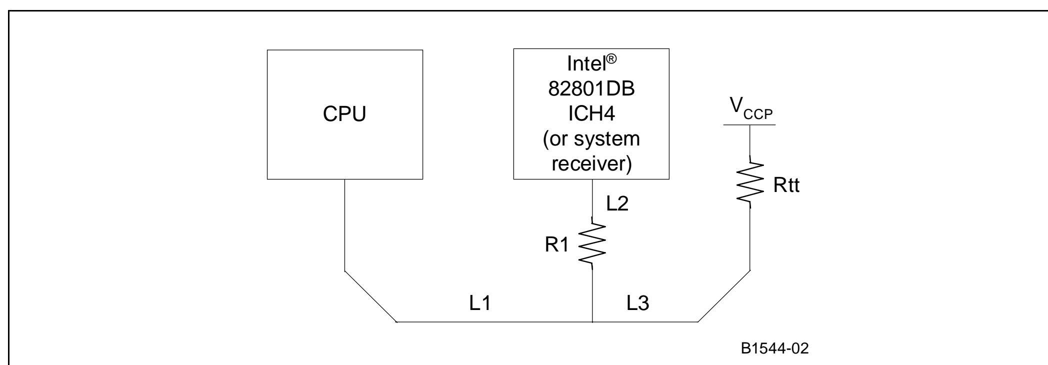


Table 12. Layout Recommendations for Topology 1B

L1	L2	L3	R1	Rtt	Transmission Line Type
0.5 – 12 inches	0 – 3 inches	0 – 3 inches	56 Ω ± 5%	56 Ω ± 5%	Microstrip
0.5 – 12 inches	0 – 3 inches	0 – 3 inches	56 Ω ± 5%	56 Ω ± 5%	Stripline

4.1.5.3 Topology 1C: Open Drain (OD) Signals Driven by the Pentium® M Processor/Celeron® M Processor – PROCHOT#

The Topology 1C OD signal PROCHOT# should adhere to the following routing and layout recommendations. Table 13 presents the layout recommendations for Topology 1C. The routing guidelines allow the signal to be routed as either a microstrip or stripline using 55 Ω ± 15% characteristic trace impedance. Figure 14 illustrates Intel's recommended implementation for providing voltage translation between the Pentium M processor/Celeron M processor PROCHOT# signal and a system receiver that utilizes a 3.3 V interface voltage (shown as V_IO_RCVR). The receiver at the output of the voltage translation circuit may be any system receiver that may function properly with the PROCHOT# signal given the nature and usage model of this pin. PROCHOT# is capable of toggling hundreds of times per second to signal a hot temperature condition.

Series resistor Rs is a component of the voltage translation logic and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 18. Rs should be placed at the beginning of the T-split from the PROCHOT# signal. The pull-up voltage for termination resistor Rtt is V_{CCP} (1.05 V).

Figure 14. Routing Illustration for Topology 1C

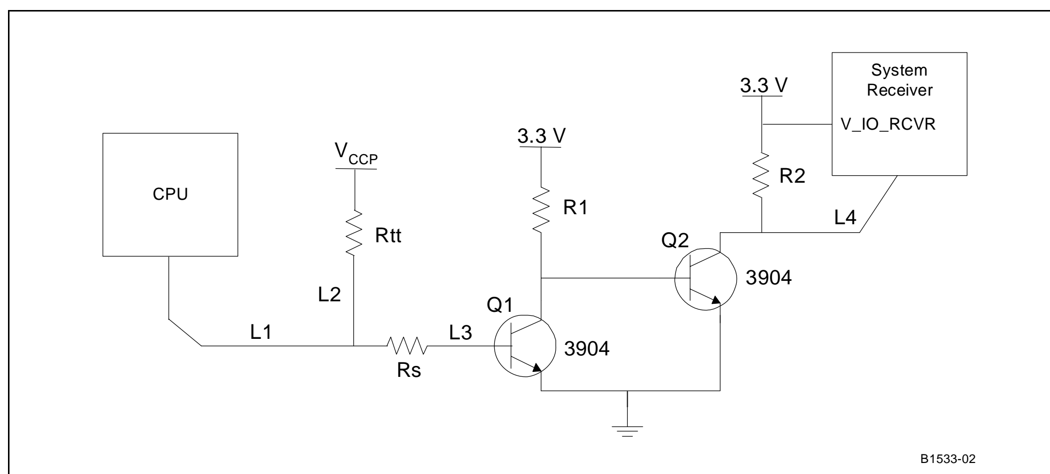


Table 13. Layout Recommendations for Topology 1C

L1	L2	L3	L4	Rs	R1	R2	Rtt	Transmission Line Type
0.5 – 12 inches	0 – 3 inches	0 – 3 inches	0.5 – 12 inches	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	56 Ω ± 5%	Microstrip
0.5 – 12 inches	0 – 3 inches	0 – 3 inches	0.5 – 12 inches	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	56 Ω ± 5%	Stripline

4.1.5.4 Topology 2A: Open Drain (OD) Signals Driven by ICH4 – PWRGOOD

The Topology 2A OD signal PWRGOOD, which is driven by the ICH4 (CMOS signal input to processor) should adhere to the following routing and layout recommendations. Table 14 presents the recommended routing requirements for the PWRGOOD signal of the processor. The routing guidelines allow the signal to be routed as either microstrip or striplines using 55 Ω ± 15% characteristic trace impedance. The pull-up voltage for termination resistor Rtt is V_{CCP} (1.05 V).

The ICH4's CPUPWRGD signal should be routed point-to-point to the processor's PWRGOOD signal. The routing from the processor's PWRGOOD pin should fork out to both the termination resistor, Rtt, and the ICH4. Segments L1 and L2 should not T-split from a trace from the pin. Figure 15 illustrates the routing illustration for Topology 2A.

Figure 15. Routing Illustration for Topology 2A

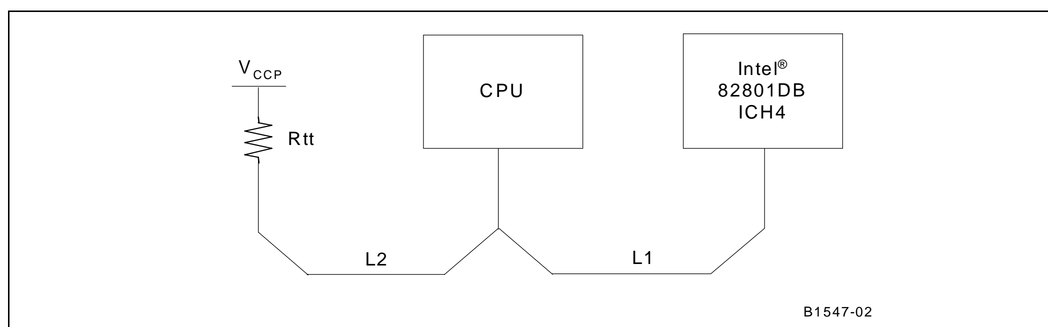


Table 14. Layout Recommendations for Topology 2A

L1	L2	Rtt	Transmission Line Type
0.5 – 12 inches	0 – 3 inches	330 Ω ± 5%	Microstrip
0.5 – 12 inches	0 – 3 inches	330 Ω ± 5%	Stripline

4.1.5.5 Topology 2B: CMOS Signals Driven by ICH4-LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK#

The Topology 2B CMOS LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK# signals should implement a point-to-point connection between the ICH4 and the Pentium M processor/Celeron M processor. Table 15 presents the layout recommendations for Topology 2B. Routing guidelines allow both signals to be routed as either microstrip or striplines using 55 Ω ± 15% characteristic trace impedance. No additional motherboard components are necessary for this topology. Figure 16 illustrates the routing illustration for Topology 2B.

Figure 16. Routing Illustration for Topology 2B

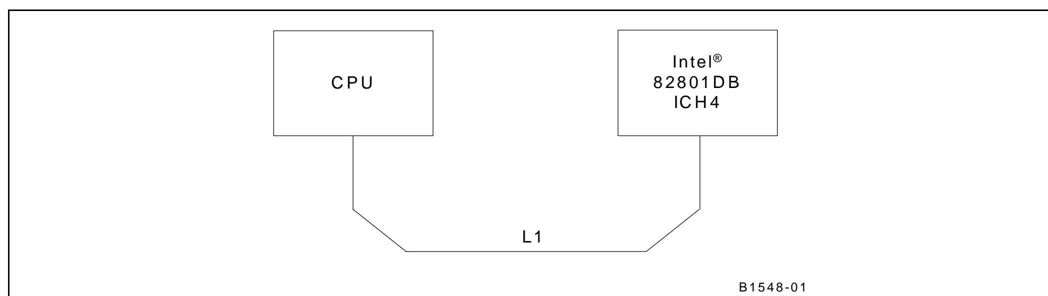


Table 15. Layout Recommendations for Topology 2B

L1	Transmission Line Type
0.5 – 12 inches	Microstrip
0.5 – 12 inches	Stripline

4.1.5.6 Topology 3: CMOS Signals Driven by ICH4 to CPU and FWH – INIT#

The signal INIT# should adhere to the following routing and layout recommendations. Table 16 presents the layout recommendations for Topology 3. The routing guidelines allow both signals to be routed as either microstrip or striplines using 55 Ω ± 15% characteristic trace impedance. Figure 17 illustrates Intel's recommended implementation for providing voltage translation between the ICH4's INIT# voltage signaling level and any firmware hub (FWH) that utilizes a 3.3 V interface voltage (shown as a supply V_IO_FWH). Refer to Section 4.1.5.7 for more details on the voltage translator circuit. For convenience, the entire topology and required transistors and resistors for the voltage translator are shown in Figure 17.

Series resistor Rs is a component of the voltage translator logic circuit and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance of L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 18. The routing recommendations of transmission line L3 in Figure 17 is listed in Table 16 and Rs should be placed at the beginning of the T-split of the trace from the ICH4's INIT# pin.

Figure 17. Routing Illustration for Topology 3

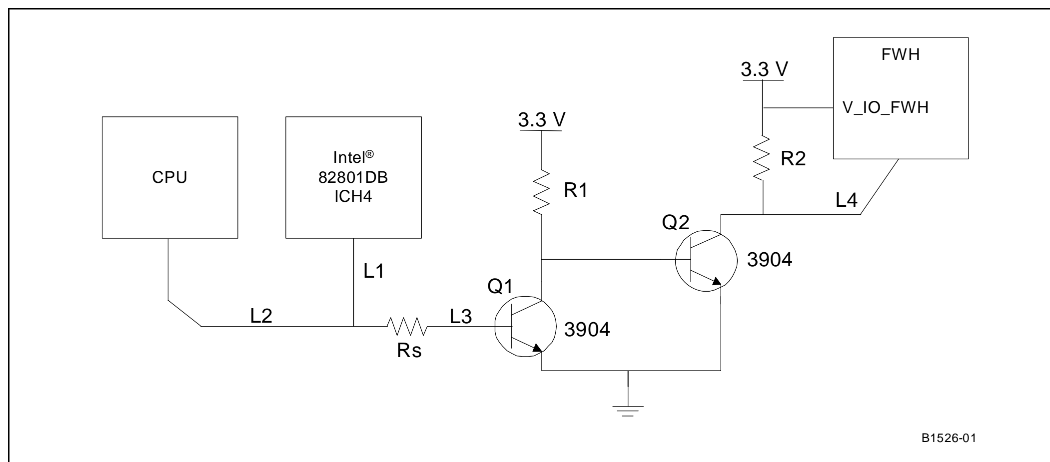


Table 16. Layout Recommendations for Topology 3

L1 + L2	L3	L4	Rs	R1	R2	Transmission Line Type
0.5 – 12 inches	0 – 3 inches	0.5 – 6 inches	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	Microstrip
0.5 – 12 inches	0 – 3 inches	0.5 – 6 inches	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	Stripline

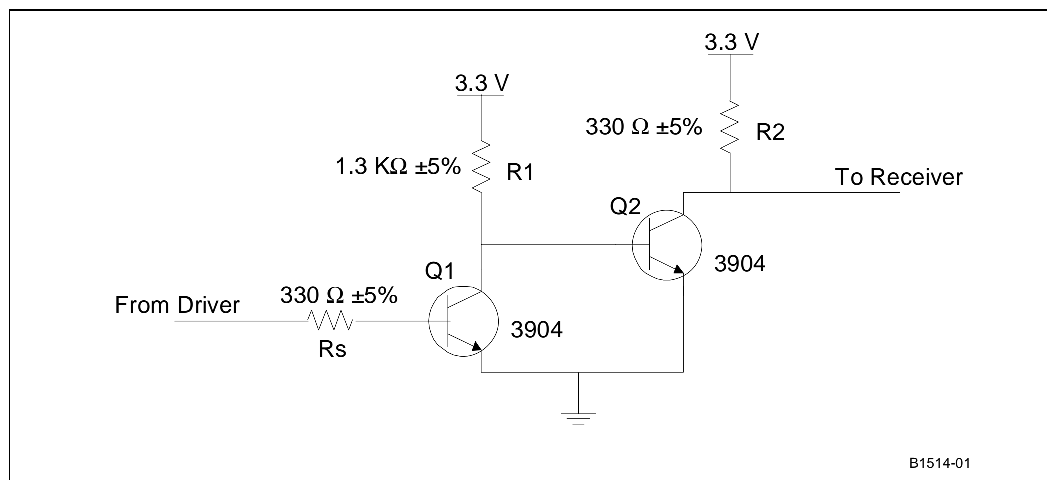
4.1.5.7 Voltage Translation Logic

A voltage translation circuit or component is required on any signals where the voltage signaling level between two components connected by a transmission line may cause unpredictable signal quality. Intel's recommended voltage translation circuit for the platform is shown in Figure 18. For the INIT# signal (Section 4.1.5.6), a specialized version of this voltage translator circuit is used where the driver isolation resistor, Rs, is place at the beginning of a transmission line that connects to the first bipolar junction transistor, Q1. Though the circuit shown in Figure 18 was developed to work with signals that require translation from a 1.05 V to a 3.3 V voltage level, the same topology and component values, in general, may be adapted for use with other signals as well, provided the interface voltage of the receiver is also 3.3 V. Any component value changes or component placement requirements for other signals must be simulated to ensure good signal quality and acceptable performance from the circuit.

In addition to providing voltage translation between driver and receiver devices, Intel's recommended circuit also provides filtering for noise and electrical glitches. A larger first-stage collector resistor, R1, may be used on the collector of Q1. However, it results in a slower response time to the output falling edge. In the case of the INIT# signal, use resistors with values as close as possible to those listed in Figure 18.

With the low 1.05 V signaling level of the Pentium M processor/Celeron M processor system bus, the voltage translation circuit provides ample isolation of any transients or signal reflections at the input of transistor Q1 from reaching the output of transistor Q2. Based on simulation results, the voltage translation circuit may effectively isolate transients as large as 200 mV and that last as long as 60 ns.

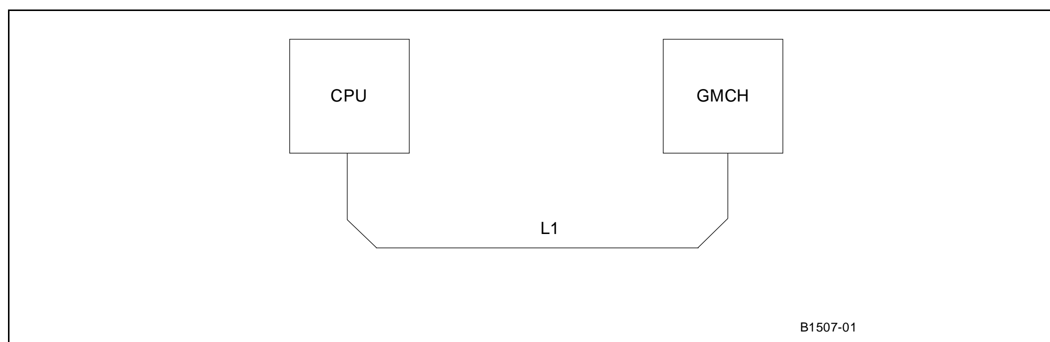
Figure 18. Voltage Translation Circuit



4.1.6 Processor RESET# Signal

The RESET# signal is a common clock signal driven by the GMCH CPURESET# pin. In a production system where no ITP700FLEX debug port is implemented, a simple point-to-point connection between the CPURESET# pin of the GMCH and the Pentium M processor/Celeron M processor RESET# pin is recommended (see Figure 19). On-die termination of the AGTL+ buffers on both the processor and the GMCH provide proper signal quality for this connection. This is the same case as for the other common clock signals listed Section 4.1.2. Length L1 of this interconnect should be limited to minimum of one inch and maximum of 6.5 inches.

Figure 19. Processor RESET# Signal Routing Topology With NO ITP700FLEX Connector



For a system that implements an ITP700FLEX debug port, a more elaborate topology is required to ensure proper signal quality at both the processor signal pad and the ITP700FLEX input receiver. In this case, implement the topology shown in Figure 20. The CPURESET# signal from the GMCH should fork out (do not route one trace from GMCH pin and then T-split) towards the processor's RESET# pin as well as toward the Rtt and Rs resistive termination network placed next to the ITP700FLEX debug port connector. Rtt (220 Ω + 5%) pulls up to the V_{CCP} voltage and is placed at the end of the L2 line that is limited to a six inch maximum length. Place Rs (22.6 Ω ± 1%) next to Rtt to minimize routing between them in the vicinity of the ITP700FLEX connector to limit the L3 length to less than 0.5 inch. ITP700FLEX operation requires matching the L2 + L3 - L1 length to the length of the BPM[4:0]# signals within ± 50 ps. Refer to Section 4.3.1 for more details on ITP700FLEX signal routing. Refer to Table 17 for routing length summary and termination resistor values.

Figure 20 illustrates the processor RESET# signal routing topology with an ITP700FLEX connector.

Figure 20. Processor RESET# Signal Routing Topology With ITP700FLEX Connector

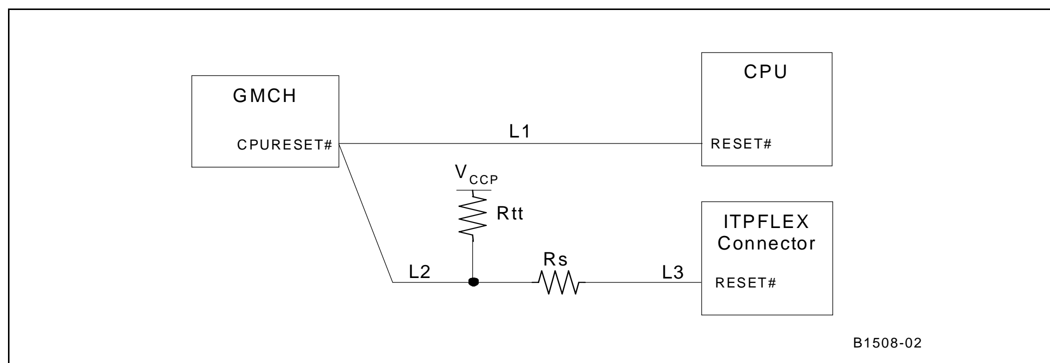


Table 17 presents processor RESET# signal routing guidelines with an ITP700FLEX connector.

Table 17. Processor RESET# Signal Routing Guidelines with an ITP700FLEX Connector

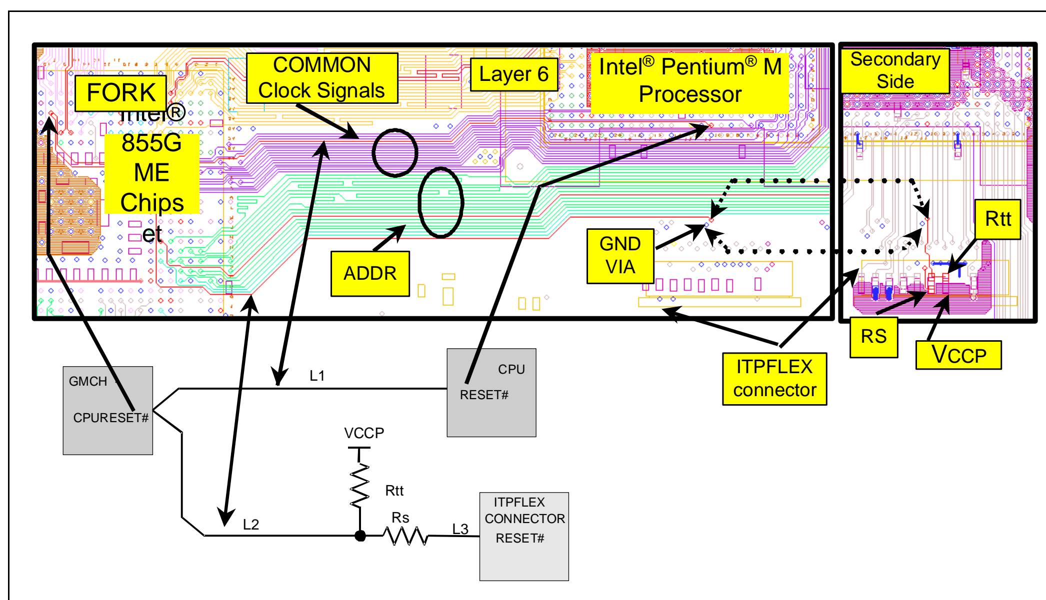
L1	L2 + L3	L3	Rs	Rtt
1 – 6 inches	6 inches max.	0.5 inch max.	Rs = 22.6 Ω ± 1%	Rtt = 220 ± 5%

4.1.6.1 Processor RESET# Routing Example

Figure 21 illustrates a board routing example for the RESET# signal with an ITP700FLEX debug port implemented. Figure 21 illustrates how the CPURST# pin of GMCH forks out into two branches on Layer 6 of the motherboard. One branch is routed directly to the Pentium M processor/Celeron M processor RESET# pin among the rest of the common clock signals. Another branch routes below the address signals and vias down to the secondary side that route to the Rs and Rtt resistors. These resistors are placed in the vicinity of the ITP700FLEX debug port.

Note: The placement of Rs and Rtt next to each other is to minimize the routing between Rs and Rtt as well as the minimal routing between Rs and the ITP700FLEX connector. Also, because a transition between Layer 6 and the secondary side occurs, a GND stitching via is added to ensure continuous ground reference of the secondary side routing of the RESET# signal to ITP700FLEX connector.

Figure 21. Processor RESET# Signal Routing Example with ITP700FLEX Debug Port



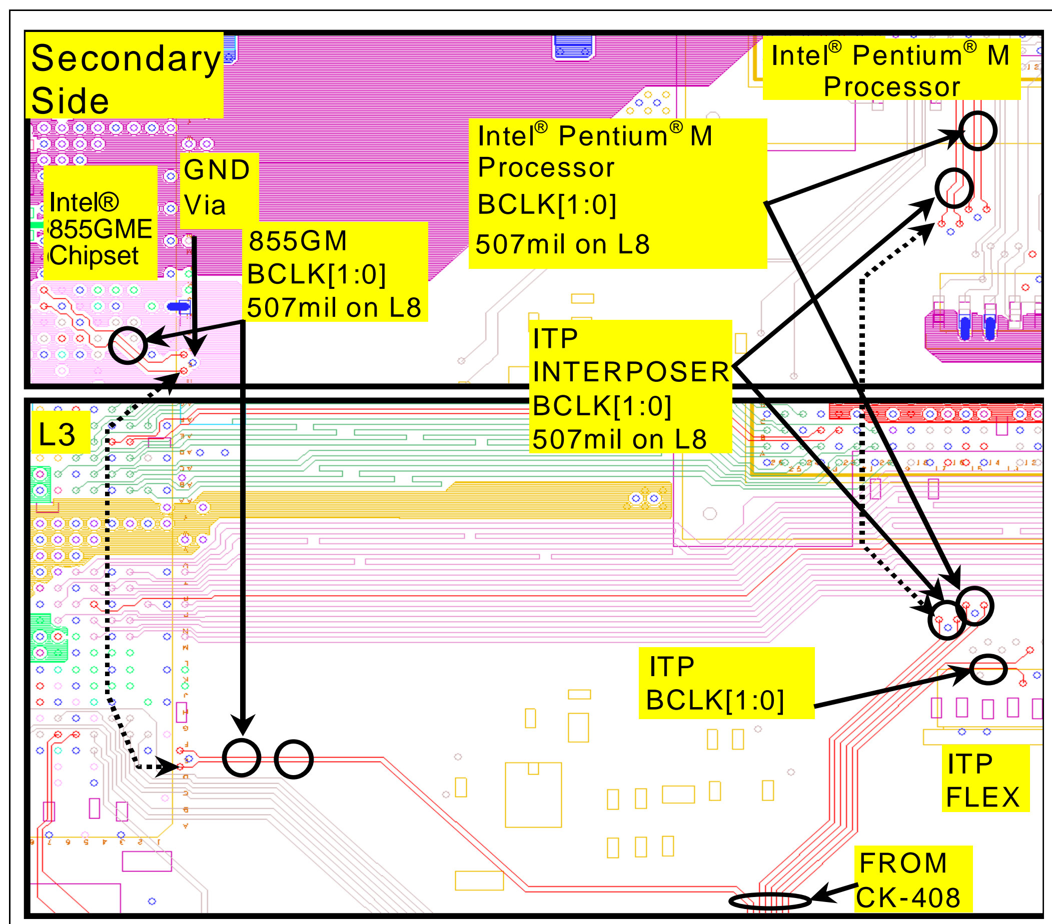
4.1.7 Processor and GMCH and Host Clock Signals

Figure 22 illustrates processor and GMCH host clock signal routing. Both the processor and the GMCH's BCLK[1:0] signals are initially routed from the CK-408 clock generator on Layer 3. In Intel's recommended routing example (Figure 22), secondary side layer routing of BCLK[1:0] is 507 mils long. To meet length-matching requirements between the processor and GMCH's BCLK[1:0] signals, a similar transition from Layer 3 to the secondary side layer is done next to the GMCH package outline. Routing of the GMCH's BCLK[1:0] signals on the secondary side is also trace tuned to 507 mils. BCLK[1:0] layer transition vias are accompanied by GND stitching vias. For similar reasons, routing for the ITP interposer's BCLK[1:0] signals also transition from Layer 3 to the secondary side layer and have 507-mil long traces on this layer. Throughout the routing length on Layer 3, BCLK[1:0] signals should reference a solid GND plane on Layer 2 and Layer 4 as shown in Figure 9.

If a system supports either the on-board ITP700FLEX connector or ITP Interposer only, then differential host clock routing to either the ITP700FLEX connector or CPU socket (but not both) is required.

Figure 22 illustrates the Pentium M processor/Celeron M processor and Intel 82855GME GMCH host clock layout routing example.

Figure 22. Pentium® M Processor/Celeron® M Processor and Intel® 855GME Chipset GMCH (82855GME) Host Clock Layout Routing Example



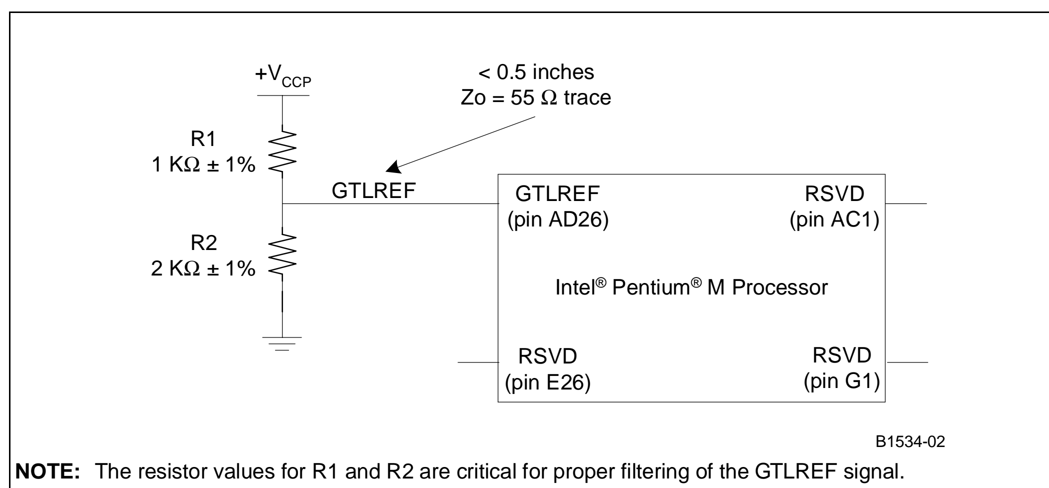
4.1.8 Processor GTLREF Layout and Routing Recommendations

There is one AGTL+ reference voltage pin on the Pentium M processor/Celeron M processor, GTLREF, used to set the reference voltage level for the AGTL+ signals (GTLREF). The reference voltage must be supplied to the GTLREF pin. The voltage level supplied to GTLREF must be equal to 2/3 * V_{CCP} ± 2%. The GMCH also requires a reference voltage (MCH_GTLREF) to be supplied to its HVREF[4:0] pins. The GTLREF voltage divider for both the processor and GMCH cannot be shared. Thus, both the processor and GMCH must have their own locally generated GTLREF networks. Figure 23 illustrates Intel's recommended topology for generating GTLREF for the processor using a R1 = 1 kΩ ± 1% and R2 = 2 kΩ ± 1% resistive divider.

Since the input buffer trip point is set by the 2/3*V_{CCP} on GTLREF and to allow tracking of V_{CCP} voltage fluctuations, **no** decoupling should be placed on the GTLREF pin. The node between R1 and R2 (GTLREF) should be connected to the GTLREF pin of the processor with Zo = 55 Ω trace shorter than 0.5 inch. Space any other switching signals away from GTLREF with a minimum separation of 25 mils. Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals).

RSVD signal pins E26, G1, and AC1 are to be left unconnected on Pentium M processor/Celeron M processor based systems.

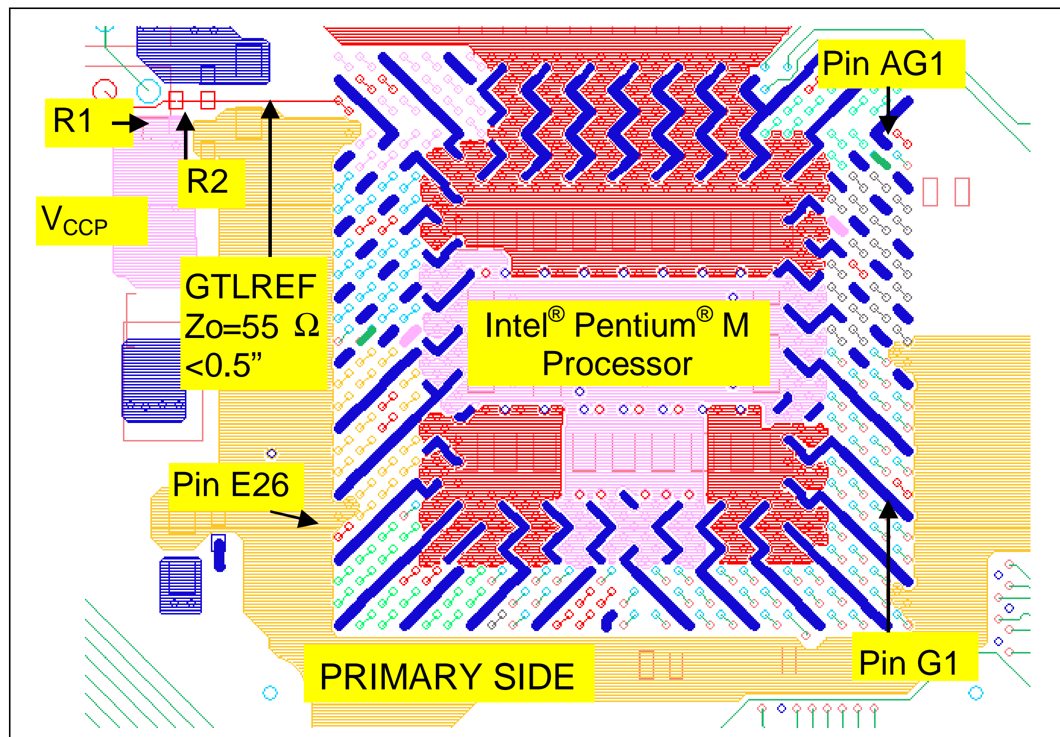
Figure 23. Pentium® M Processor/Celeron® M Processor GTLREF Voltage Divider Network



NOTE: The resistor values for R1 and R2 are critical for proper filtering of the GTLREF signal.

Intel's recommended layout of GTLREF for the Pentium M processor/Celeron M processor is shown in Figure 24. To avoid interaction with Pentium M processor FSB routing and power delivery, GTLREF's R1 and R2 components are placed next to each other on the primary side of the motherboard and connected with a Zo = 55 Ω, 370 mil long trace to the GTLREF pin on the Pentium M processor/Celeron M processor, which meets the 0.5-inch maximum length requirement. The BGA ball lands on the primary side for the RSVD signal pins E26, G1, and AC1 are shown for illustrative purposes and are not routed.

Figure 24. Pentium® M Processor/Celeron® M Processor GTLREF Motherboard Layout



4.1.9 AGTL+ I/O Buffer Compensation

The Pentium M processor/Celeron M processor has four pins, COMP[3:0], and the GMCH has two pins, HRCOMP[1:0], that require compensation resistors to adjust the AGTL+ I/O buffer characteristics to specific board and operating environment characteristics. The GMCH requires two special reference voltage generation circuits to pins HSWNG[1:0] for the same purpose described above. Refer to the *Intel® 855GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet*, *Intel® Pentium® M Processor Datasheet*, *Intel® Celeron® M Processor Datasheet* and *Intel® Pentium® M Processor on 90 nm process with 2 MB L2 Cache Datasheet* for details on resistive compensation.

4.1.9.1 Pentium® M Processor/Celeron® M Processor AGTL+ I/O Buffer Compensation

For the Pentium M processor/Celeron M processor, the COMP[2] and COMP[0] pins (see Figure 25) each must be pulled down to ground with 27.4 Ω ± 1% resistors and should be connected to the Pentium M processor/Celeron M processor with a Zo = 27.4 Ω trace that is less than 0.5 inch from the processor pins. The COMP[3] and COMP[1] pins (see Figure 26) each must be pulled down to ground with 54.9 Ω ± 1% resistors and should be connected to the Pentium M processor/Celeron M processor with a Zo = 55 Ω trace that is less than 0.5 inch from the processor pins. COMP[3:0] traces should be at least 25 mils (> 50 mils preferred) away from any other toggling signal.

Figure 25 illustrates the Pentium M processor/Celeron M processor COMP[2] and COMP[0] resistive compensation.

Figure 25. Pentium® M Processor/Celeron® M Processor COMP[2] and COMP[0] Resistive Compensation

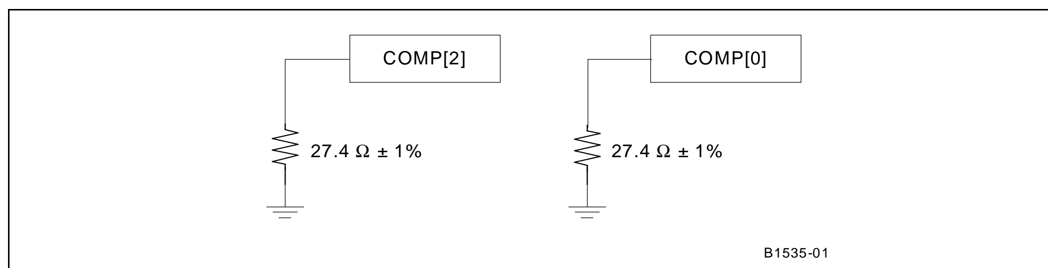
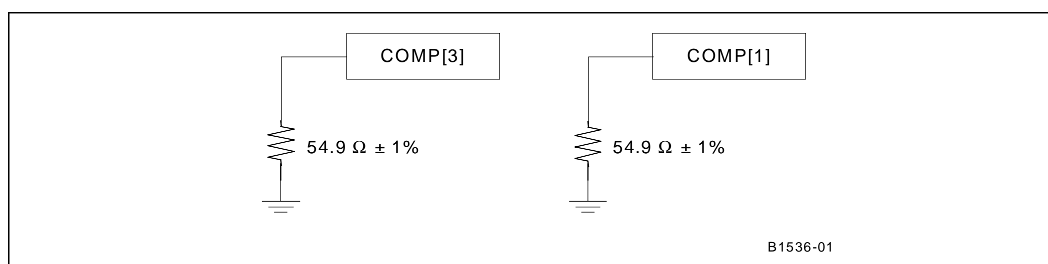


Figure 26 illustrates the Pentium M processor/Celeron M Processor COMP[3] and COMP[1] resistive compensation.

Figure 26. Pentium® M Processor/Celeron® M Processor COMP[3] and COMP[1] Resistive Compensation



Intel's recommended layout of the Pentium M processor/Celeron M processor COMP[3:0] resistors is shown in Figure 27. To avoid interaction with Pentium M processor/Celeron M processor FSB routing on internal layers and V_{CCA} power delivery on the primary side, Layer 1, COMP[1:0] resistors are placed on the secondary side. Ground connections to the COMP[1:0] resistors use a small ground flood on the secondary side layer and connect only with a single GND via to stitch the GND planes. The compact layout as shown in Figure 27 should be used to avoid excessive perforation of the V_{CCP} plane power delivery. Figure 27 illustrates how a 27.4 Ω resistor connects with an ~18 mil wide (Zo = 27.4 Ω) and 160 mil long trace to COMP0. Necking down to 14 mils is allowed for a short length to pass between the dog bones. The 54.9 Ω resistor connects with a regular 5 mil wide (Zo = 55 Ω) and 267 mil long trace to COMP1. Placement of COMP[1:0] on the primary side is possible as well. An alternative placement implementation is shown in Figure 28.

To minimize motherboard space usage and produce a robust connection, the COMP[3:2] resistors are also placed on the secondary side (Figure 27, right side). A 27.4 Ω resistor connects with an 18 mil wide (Zo = 27.4 Ω) and 260 mil long trace to COMP2. Necking down to 14 mils is allowed for a short length to pass in between the dog bones. The COMP2 (Figure 27, left side) dog bone trace connection on the primary side is also widened to 14 mils to meet the Zo = 27.4 Ω characteristic impedance target. The right side of Figure 27 also illustrates how the 54.9 Ω ± 1% resistor connects with a regular 5 mil wide (Zo = 55 Ω) and 100 mil long trace to COMP3. The ground connection of COMP[3:2] is done with a small flood plane on the secondary side that connects to the GND vias of pins AA1 and Y2 of the Pentium M processor/Celeron M processor pin-map. This is done to avoid via interaction with the Pentium M processor/Celeron M processor FSB routing on Layer 3 and Layer 6.

For COMP2 and COMP0, it is extremely important that 18 mil wide dog bone connections on the primary side and 18 mil wide traces on the secondary sides be used to connect the signals to compensation resistors on the secondary side, as shown in Figure 29. The 18 mil wide dog bones and traces are used to achieve the Zo = 27.4 Ω target to ensure proper operation of the Pentium M processor/Celeron M processor FSB. Refer to Figure 25 for more details.

Figure 27 illustrates the Pentium M processor/Celeron M processor COMP[3:0] resistor layout.

Figure 27. Pentium® M Processor/Celeron® M Processor COMP[3:0] Resistor Layout

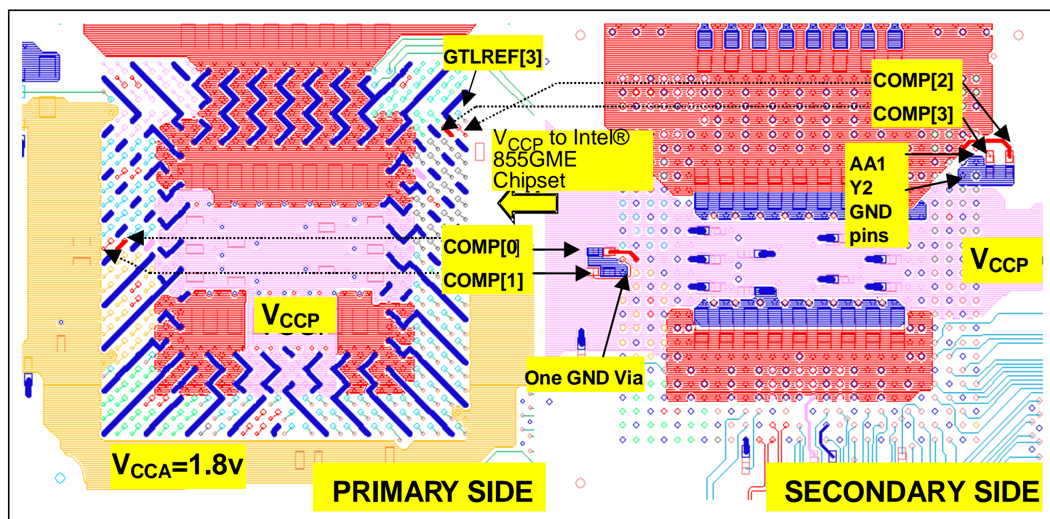


Figure 28 illustrates the Pentium M processor/Celeron M processor COMP[1:0] resistor alternative primary side layout.

Figure 28. Pentium® M Processor/Celeron® M Processor COMP[1:0] Resistor Alternative Primary Side Layout

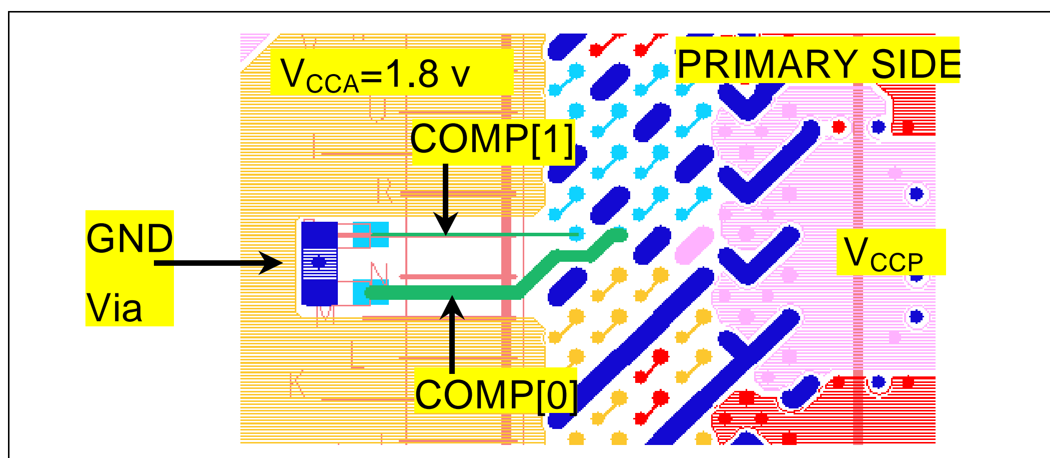
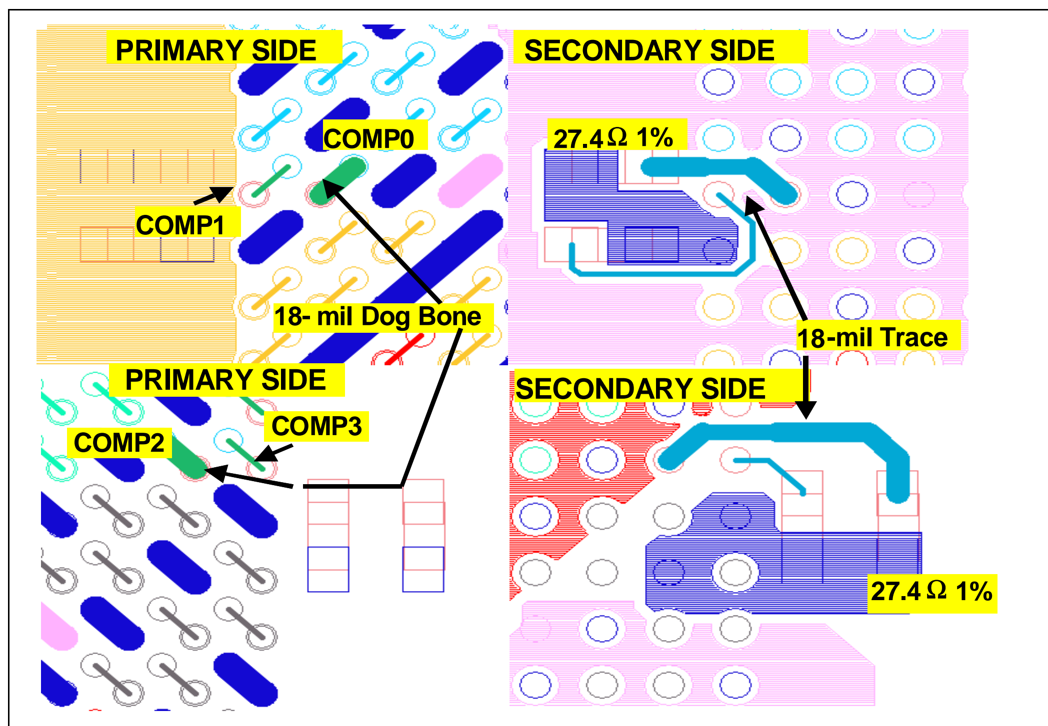


Figure 29 illustrates the COMP2 and COMP0 18-mil wide dog bones and traces.

Figure 29. COMP2 and COMP0 18-mil Wide Dog Bones and Traces



4.1.10 Pentium® M Processor/Celeron® M Processor System Bus Strapping

The Pentium M processor/Celeron M processor and GMCH both have pins that require termination for proper component operation.

1. For the processor, provide a stuffing option for the TEST[3] pin to allow a 1 kΩ ±5% pull-down to ground for testing purposes. For proper processor operation, the resistor should not be stuffed. Resistors for the stuffing option on these pins should be placed within two inches of the processor. For normal operation, these resistors should not be stuffed.
2. The processor's ITP signals, TDI, TMS, TRST and TCK should assume default logic values even if the ITP debug port is not used. The TDO signal may be left open or no connect in this case. These resistors should be connected to the processor within two inches from their respective pins.

Note: Table 18 is applicable only when neither the onboard ITP nor ITP interposer are planned to be used. Refer to Section 4.2.2 on cautions against designs with lack of debug tools support. Intel does not recommend use of the ITP interposer debug port if there is a dependence only on the motherboard termination resistors

The signals below should be isolated from the motherboard via specific termination resistors on the ITP interposer itself per interposer debug port recommendations. For the case where the onboard ITP700FLEX debug port is used, refer to Section 4.3 for default termination recommendations.

Table 18 presents the ITP signal default strapping when an ITP debug port is not used.

Table 18. ITP Signal Default Strapping When ITP Debug Port is Not Used

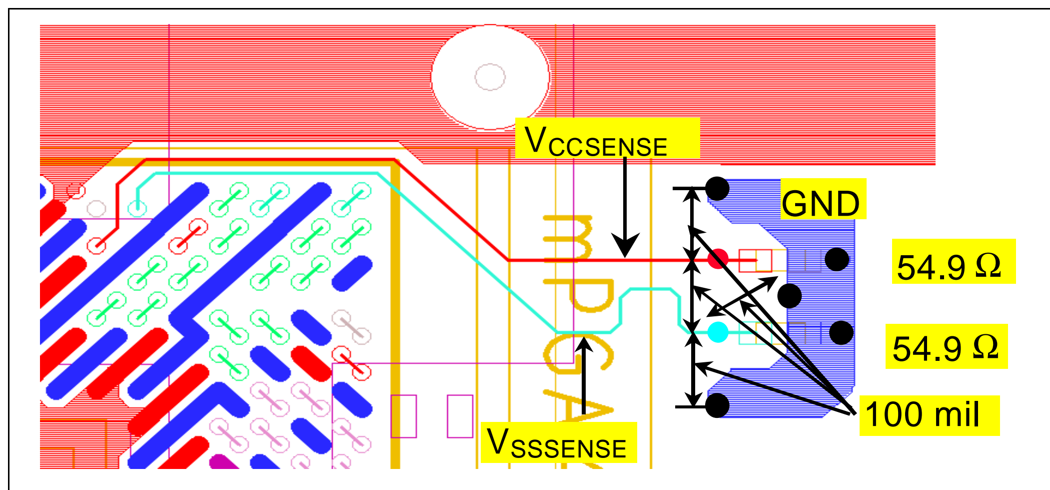
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 Ω ± 5%	V_{CCP}	Within two inches of the CPU
TMS	39 Ω ± 5%	V_{CCP}	Within two inches of the CPU
TRST#	680 Ω ± 5%	GND	Within two inches of the CPU
TCK	27 Ω ± 5%	GND	Within two inches of the CPU
TDO	Open	NC	N/A

4.1.11 Pentium® M Processor/Celeron® M Processor $V_{CCSENSE}$/ $V_{SSSENSE}$ Design Recommendations

The $V_{CCSENSE}$ and $V_{SSSENSE}$ signals of the Pentium M processor/Celeron M processor provide isolated, low-impedance connections to the processor's core power (V_{CC}) and ground (V_{SS}). These pins may be used to sense or measure power (V_{CC}) or ground (V_{SS}) near the silicon with little noise. To make them available for measurement purposes, Intel recommends that $V_{CCSENSE}$ and $V_{SSSENSE}$ both be routed with a Zo = 55 Ω ± 15% trace of equal length. Use 3:1 spacing between the routing for the two signals and all other signals should be a minimum of 25 mils (preferably 50 mils) from $V_{CCSENSE}$ and $V_{SSSENSE}$ routing. Terminate each line with an optional (default is No Stuff) 54.9 Ω ± 1% resistor. Also, add a ground via spaced 100 mils away from each of the test point vias for $V_{CCSENSE}$ and $V_{SSSENSE}$. Place a third ground via between them to allow for a differential probe ground.

Figure 30 illustrates the $V_{CCSENSE}$/$V_{SSSENSE}$ routing example.

Figure 30. $V_{CCSENSE}$/$V_{SSSENSE}$ Routing Example



4.1.12 PLL Voltage Design for Low Voltage Intel® Pentium® M Processors on 90 nm Process with 2 MB L2 Cache

One primary difference between the Intel Pentium M processor (130nm) and the Low Voltage Intel® Pentium® M processor on 90 nm process with 2 MB L2 cache or the Intel® Celeron® M Processor on 90nm process is the analog PLL voltage supplying the processor's on-die clock generators. The VCCA PLL power delivery pins of the Low Voltage Intel® Pentium® M Processors on 90 nm process with 2 MB L2 cache and the Intel® Celeron® M Processor on 90nm process have the option of using either a 1.8 V or 1.5 V power supply. For a platform supporting only Low Voltage Intel® Pentium® M Processors on 90 nm process with 2 MB L2 cache or Intel® Celeron® M Processor on 90nm process, the VCCA[3:0] pin should be powered by the 1.5 V rail, since the 1.5 V rail is already required for the GMCH. This eliminates the need for a 1.8 V rail on the platform. However, if a platform is to also support Intel® Pentium® M processors (130nm) and standard voltage Intel® Pentium® M processors on 90 nm process with 2 MB L2 cache, then the 1.8 V rail must be used for the analog PLL voltage supply.

4.2 Intel System Validation Debug Support

In any design, it is critical to enable industry-standard tools to allow for debugging a wide range of issues that come up in the normal design cycle. In embedded designs, electrical/logic visibility is limited, often making debugging time-consuming. In some cases, progress requires board redesign or extensive rework. The following topics are very important to general system debug capabilities.

4.2.1 ITP Support

4.2.1.1 Background/Justification

One key tool that is needed to debug BIOS, logic, signal integrity, general software, and general hardware issues involving CPUs, chipsets, SIOs, PCI devices, and other hardware in a platform design is the In Target Probe (ITP). The ITP is widely used by various validation, test, and debug groups within Intel (as well as by third-party BIOS vendors, OEMs, and other developers).

Note: It is critical that ITP support is provided. Any Pentium M processor/Celeron M processor with the Intel 855GME chipset system designed without ITP support may prevent assistance from various Intel validation, test, and debug groups in debugging various issues. ITP support can be done with zero additional BOM cost and minimal layout/footprint costs.

The cost for not providing ITP support may range from none, if no blocking issues are found in the system design, to schedule slips of a month or more. The latter scenario represents the time needed to spin a board design and required assembly time to add an ITP port when it is absolutely required and other mechanical and routing issues prevent the use of an ITP interposer, if one exists.

4.2.1.2 Implementation

To minimize the ITP connector footprint, the ITP700FLEX alternative is a better option for mobile designs. However, standard signal connection guidelines for the processor TAP logic signals for the non-ITP case should be followed so that only the traces and component **footprints** need to be

added to the design, with all previous non-ITP guidelines followed otherwise. This way, when ITP support is needed, termination values and connector can be populated as needed for debug support.

Note: If the ITP700FLEX footprint cannot be followed due to mechanical or routing reasons, it may be adequate to have a simple via grouping in lieu of the connector to allow for 'blue-wiring' of the ITP, provided that footprints for the resistors are available on board and that the blue-wiring from the signal vias to the ITP700FLEX connector are as short as possible.

4.2.2 Pentium® M Processor/Celeron® M Processor Logic Analyzer Support (FSB LAI)

4.2.2.1 Background/Justification

The Pentium M processor/Celeron M processor System Bus Logic Analyzer probe (FSB LAI) is widely used by various validation, test, and debug groups within Intel (as well as by third-party BIOS vendors, OEMs, and other developers) and is needed to debug BIOS, logic, signal integrity, general software, and general hardware issues involving CPUs, chipsets, SIOs, PCI devices, and other hardware. Agilent Technologies, Inc.* has developed this tool for the processor.

A Pentium M/Celeron M Processor with Intel 855GME chipset system designed without FSB LAI support may severely limit the ability of various Intel validation, test, and debug groups from debugging various issues in a reasonable amount of time.

Since support may be limited, it is critical that the following FSB LAI support is provided:

1. Provide a motherboard with a CPU socket. The FSB LAI is an interposer that plugs into the CPU socket, and the CPU then plugs into the LAI. The use of non-standard sockets may prohibit the LAI from working as the locking mechanism may become inaccessible. It is important to check the LAI design guidelines to ensure a particular socket will work. The LAI was designed to accommodate the most common processor sockets on the market.
2. Observe FSB LAI keepout requirements. There are several options to achieving this, for example, removing the motherboard from the case (typically the first step to meeting keepout requirements) or relocating components that would otherwise be in the keepout area for debug purposes (e.g., axial lead devices that can be de-soldered and re-soldered to the other side of the board, parts that can be removed and blue-wired further away, etc.). If keepouts still cannot be met, Intel strongly recommends that a separate debug motherboard be built which has the same BOM and Netlist, but has FSB LAI keepout requirements met. This also enables the addition of other test points.

4.2.2.2 Implementation

Contact your local Intel field representative to obtain design information from Agilent Technologies, Inc. on the Pentium M processor/Celeron M processor FSB LAI mechanicals (i.e., design guide with keepout volume information). Refer to Section 4.3.3 for more details.

4.2.3 Intel® Pentium® M Processor/Celeron® M Processor On-Die Logic Analyzer Trigger (ODLAT) Support

The Pentium M processor/Celeron M processor provides support for three address/data recognizers on-die for setting on-die logic analyzer triggers (ODLAT) or breakpoints. Details on the ODLAT are available from American Arium*.

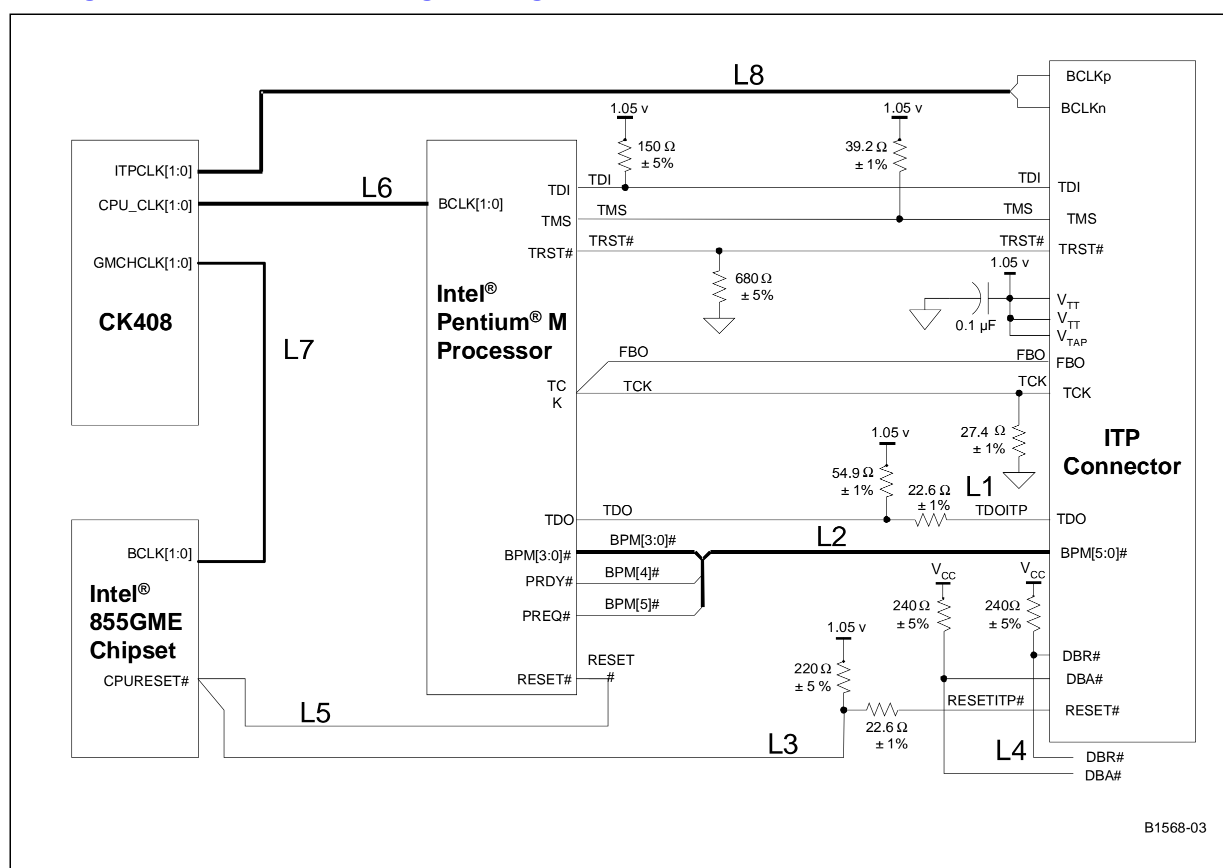
4.3 Onboard Debug Port Routing Guidelines

For systems incorporating the Pentium M processor/Celeron M processor , the debug port should be implemented as either an onboard debug port or via an interposer. Refer to the *ITP700FLEX Debug Port Design Guide*, found at http://developer.intel.com/design/Xeon/guides/249679.htm for the most up-to-date information.

4.3.1 ITP Signal Routing Guidelines

Figure 31 illustrates recommended connections between the onboard ITP700FLEX debug port, Pentium M processor, Intel® 82855GME (GMCH), and CK-408 clock chip in the cases where the debug port is used.

Figure 31. ITP700FLEX Debug Port Signals



1. Route the TDI signal between the ITP700FLEX connector and the Pentium M processor/Celeron M processor. Place a 150-Ω ±5% pull-up to V_{CCP} (1.05 V) within ± 300 ps of the TDI pin.
2. Route the TMS signal between ITP700FLEX connector and the Pentium M processor/Celeron M processor. Place a 39.2-Ω ±1% pull-up to V_{CCP} within ± 200 ps of the ITP700FLEX connector pin.
3. Route the TRST# signal between ITP700FLEX connector and the Pentium M processor/Celeron M processor. Place a 510 Ω to 680 Ω ± 5% pull-down to ground on TRST#. Placement of the pull-down resistor is not critical. Avoid having any trace stub from the TRST# signal line to the termination resistor.
4. Route the TCK signal from the ITP700FLEX connector's TCK pin to the Pentium M processor/Celeron M processor TCK pin and then fork back from the Pentium M processor/Celeron M processor TCK pin and route back to ITP700FLEX connector's FBO pin. A 27.4 Ω ± 1% pull-down to ground should be placed within ± 200 ps of the ITP700FLEX connector pin.
5. Route the TDO signal from the Pentium M processor/Celeron M processor to a 54.9 Ω ± 1% pull-up resistor to V_{CCP} that should be placed close to ITP700FLEX connector's TDO pin. Then insert a 22 6 Ω ± 1% series resistor to connect the 54.9 Ω pull-up and 'TDOITP' net (see Figure 31). Limit the L1 segment length of the TDOITP net to less than one inch.

The Pentium M processor/Celeron M processor drives the BPM[4:0]# signals to the ITP700FLEX at a 100 MHz clock rate. Route the BPM[4:0]# as a Zo=55 Ω point-to-point transmission line connection between the processor and the ITP700FLEX connector. Connect the ITP700FLEX connector's BPM[3:0]# pins to Pentium M processor/Celeron M processor BPM[3:0]# pins. Connect the ITP700FLEX's BPM[4]# signal to the Pentium M processor/Celeron M processor PRDY# pin. The ITP700FLEX's integrated far-end terminations as well as the processor's AGTL+ integrated on-die termination ensure proper signal quality for the BPM[4:0]# signals. Due to the length of the ITP700FLEX cable, the length L2 of the BPM[4:0]# signals on the motherboard should be limited to shorter than six inches. The BPM[4:0]# signals' length L2 should be length matched to each other within ± 50 ps. The BPM[4:0]# signal trace lengths are matched inside the Pentium M processor/Celeron M processor package, thus motherboard routing does **not** need to compensate for any processor package trace length mismatch. The BPM[4:0]# signal lengths also need to be matched within ± 50 ps to the L3+L4-L5 net lengths of the RESET# signal, i.e., L3 + L4 – L5 = L2 (within ± 50 ps).

Refer to Figure 31 for topology. See below for details on routing guidelines for the RESET# signal.

Due to the Pentium M processor/Celeron M processor AGTL+ on-die termination for BPM[3:0]# and PRDY#, there is no issue or concern if the BPM[4:0]# pins of the ITP700FLEX connector are left floating when the ITP is not being used and the ITP700FLEX cable is unplugged.

Route the ITP700FLEX connector's BPM[5]# signal as a Zo = 55 Ω point-to-point connection to the Pentium M processor/Celeron M processor PREQ# pin. Integrated on the ITP700FLEX BPM[5]# driver signal is a resistive pull-up that ensures proper signal quality at the processor's PREQ# input pin. The Pentium M processor/Celeron M processor has an integrated, weak, on-die pull-up to V_{CCP} for the PREQ# signal to ensure a proper logic level when the ITP700FLEX port connector is not plugged in. There is no need for any external termination on the motherboard for the BPM[5]# = PREQ# signal. The maximum length of BPM[5]#/PREQ# should not exceed six inches.

As explained in Section 4.1.6, the RESET# signal forks (see Figure 20) out from the 82855GME's CPURESET# pin and is routed to the Pentium M processor/Celeron M processor and ITP700FLEX debug port. One branch from the fork connects to the Pentium M processor/Celeron

M processor RESET# pin and the second branch connects to a 220 Ω ± 5% termination pull-up resistor to V_{CCP} placed close to the ITP700FLEX debug port. A series 22.6 Ω ± 1% resistor is used to continue the path to the ITP700FLEX RESET# pin with the RESETITP# net in Figure 31. The length of the RESETITP# net (labeled as net L4) should be limited to less than 0.5 inch. To ensure correct operational timings, the length of the RESET# nets L3, L4, and L5 with respect to the BPM[4:0]# net length L2 should adhere to the following length matching requirement within ± 50 ps., i.e., L3 + L4 – L5 = L2 (within ± 50 ps).

There is no need for pull-up termination on the Pentium M processor/Celeron M processor side of the RESET# net due to presence of AGTL+ on-die termination on the processor and the 82855GME.

The ITP700FLEX debug port's BCLKp/BCLKn inputs are driven with a 100 MHz differential clock from the CK-408 clock chip. The CK-408 also feeds two other pairs of 100-MHz differential clocks to the Pentium M processor/Celeron M processor BCLK[1:0] and Intel 855GME chipset BCLK[1:0] input pins. Common clock signal timing requirements of the 82855GME and the Pentium M processor requires matching of processor and GMCH BCLK[1:0] nets L6 and L7, respectively. To ensure correct operation of ITP700FLEX, the BCLKp/BCLKn net L8 should be tuned to within ± 50 ps to the sum of length L6 of the BCLK[1:0] lines and the additional length L2 of the BPM#[4:0] signals, i.e., L6 + L2 = L8 (within ± 50 ps).

The timing requirements for the BPM[5:0]#, RESET#, and BCLKp/BCLKn signals of the ITP700FLEX debug port require careful attention to their routing. Standard high-frequency bus routing practices should be observed.

1. Keep a minimum of 2:1 spacing in between these signals and to other signals.
2. Reference these signals to ground planes and avoid routing across power plane splits.
3. Minimize the number of routing layer transitions. When layout constraints require a routing layer transition, accompany such transitions with ground stitching vias placed within 100 mils of the signal via with at least one ground via for every two signals making a layer transition.

DBR# should be routed to the system reset logic (e.g., the SYSRST# signal of the ICH4) and initiate the equivalent of a front panel reset commonly found in desktop systems. The 150 Ω to 240 Ω pull-up resistor should be placed within 1 ns of the ITP700FLEX connector.

Note: The CPU should **not** be power cycled when DBR# is asserted.

DBA# is an optional system signal that may be used to indicate to the system that the ITP/TAP port is being used. When not implemented, this signal may be left as no connect. When implemented, it should be routed with a 150 Ω to 240 Ω pull-up resistor placed within 1 ns of the ITP700FLEX connector. Refer to the *ITP700 Debug Port Design Guide* for more details on DBA# usage.

The ITP700FLEX VTT and VTAP pins should be shorted together and connected to the V_{CCP} (1.05 V) plane with a 0.1 µF decoupling capacitor placed within 0.1 inch of the VTT pins.

Table 19 summarizes termination resistors values, placement, and voltages the ITP signals connect to for proper operation for onboard ITP700FLEX debug port.

Table 19. Recommended ITP700FLEX Signal Terminations

Signal	Termination Value	Termination Voltage	Termination/Decap Location	Notes
TDI	150 Ω ± 5%	V_{CCP} (1.05 V)	Within ± 300 ps of the Pentium M processor CPU TDI pin	5
TMS	39.2 Ω ± 1%	V_{CCP} (1.05 V)	Within ± 200 ps of the ITP700FLEX connector TMS pin	5
TRST#	510-680 Ω ± 5%	GND	Anywhere between Pentium M processor CPU and ITP700FLEX connector	5
TCK	27.4 Ω ± 1%	GND	Within ± 200 ps of the ITP700 FLEX connector TCK pin	5
TDO	54.9 Ω ± 1% pull-up and 22.6 Ω ± 1% series resistor	V_{CCP} (1.05 V)	Within one inch of the ITP700FLEX connector TDO pin	1, 5
BCLK(p/n)				2
FBO	Connect to TCK pin of Pentium M processor CPU	N/A	N/A	1
RESET#	220 Ω ± 5% pull-up and 22.6 Ω ± 1% series resistor	V_{CCP} (1.05 V)	Within 0.5 inch of the ITP700FLEX connector RESET# pin	1
BPM[5:0]#	Not Required			3
DBA#	150-240 Ω ± 5%	V_{CC} of target system recovery circuit	Within 1 ns of the ITP700FLEX connector DBA# pin	4
DBR#	150-240 Ω ± 5%	V_{CC} of target system recovery circuit	Within 1 ns of the ITP700FLEX connector DBR# pin	
VTAP	Short to V_{CCP} plane	V_{CCP} (1.05 V)		
VTT	Short to V_{CCP} plane	V_{CCP} (1.05 V)	Add 0.1 µF decap within 0.1 inch of VTT pins of ITP700FLEX connector	

NOTES:
1. Refer to Figure 31.
2. Refer to Section 4.3.1 for more information.
3. All the needed terminations to ensure proper signal quality are integrated inside the Pentium M processor AGTL+ buffers or inside the ITP700FLEX debug port. No need for any external components for the BPM[5:0]# signals.
4. Only required if DBA# is used with any target system circuitry. This signal may be left unconnected if unused.
5. In cases where a system is designed to use the ITP700FLEX debug port for debug purposes but the ITP700FLEX connector may or may not be populated at all times although the signal routing and termination or decoupling components are implemented, the component placement guidelines should adhere to the ones listed. However, for signals where the termination component placement guidelines for non-ITP700FLEX supported systems (see Table 18) are more restrictive or conservative than the component placement guidelines for the ITP700FLEX supported case, then the more conservative/restrictive guidelines should be followed.

4.3.1.1 ITP Signal Routing Example

Figure 33 illustrates Intel's recommended layout example for the ITP700FLEX signals. The ITP700FLEX connector is placed on the primary side of the motherboard and results in a smooth, straight-forward routing solution.

Note: The V_{CCP} (1.05 V) power delivery continues from the Pentium M processor/Celeron M processor socket cavity on the secondary side of the motherboard through the pin field as shown on the right side of Figure 33. Three V_{CCP} vias in conjunction with three ground stitching vias allow a transition to the primary side to connect to the VTT and VTAP pins of the ITP700FLEX connector and a transition back to the secondary side of the motherboard. A small V_{CCP} flood is created on the secondary side under the body of the ITP700FLEX connector with a 0.1 µF decoupling capacitor. This provides a convenient connection for the 220 Ω and 54.9 Ω pull-ups for RESET# and TDO signals as well as the 39.2 Ω pull-up for the TMS signal.

Notice the very short trace from the 22.6 Ω series resistors for the RESET# and TDO signals to the ITP700FLEX pins. Refer to Section 4.1.6 for more details on RESET# signal routing.

The 150 Ω TDI pull-up is connected to the V_{CCP} (1.05 V) flood on the secondary side close to the Pentium M processor/Celeron M processor pin.

The ITP700FLEX TCK pin has a 27.4 Ω pull-down to ground very close to the ITP700FLEX connector and routes to the Pentium M processor/Celeron M processor TCK pin and loops back with no stub to the FBO pin of the ITP700FLEX connector.

BCLKp/BCLKn are routed in this example on Layer 3. For more BCLKp/BCLKn routing details, refer to Figure 22 in Section 4.1.7.

All other signals incorporate a straight forward routing methodology between the ITP700FLEX and Pentium M processor pins.

4.3.1.2 ITP_CLK Routing to ITP700FLEX Connector

A layout example for ITP_CLK/ITP_CLK# routing to an ITP700FLEX connector is shown in Figure 32. The CK-408 clock chip is mounted on the primary side of the motherboard and the differential clock pair breaks out on the same side. The differential ITP clock pair routing requires the use of a pair of 33 Ω ± 5% series resistors placed within 0.5 inch of the clock chip output pins followed by a pair of 49.9 Ω ± 1% termination resistors to ground. Serpentining of the ITP_CLK traces is performed to meet the ± 50 ps length matching requirement between ITP_CLK and the sum of length L6 of the BCLK[1:0] lines and the additional length L2 of the BPM#[5:0] signals in Figure 31. The ITP_CLK pair routing then switches back to the primary side layer through a via near the ITP700FLEX connector.

Figure 32 illustrates the ITP_CLK to ITP700FLEX connector layout example.

Figure 32. ITP_CLK to ITP700FLEX Connector Layout Example

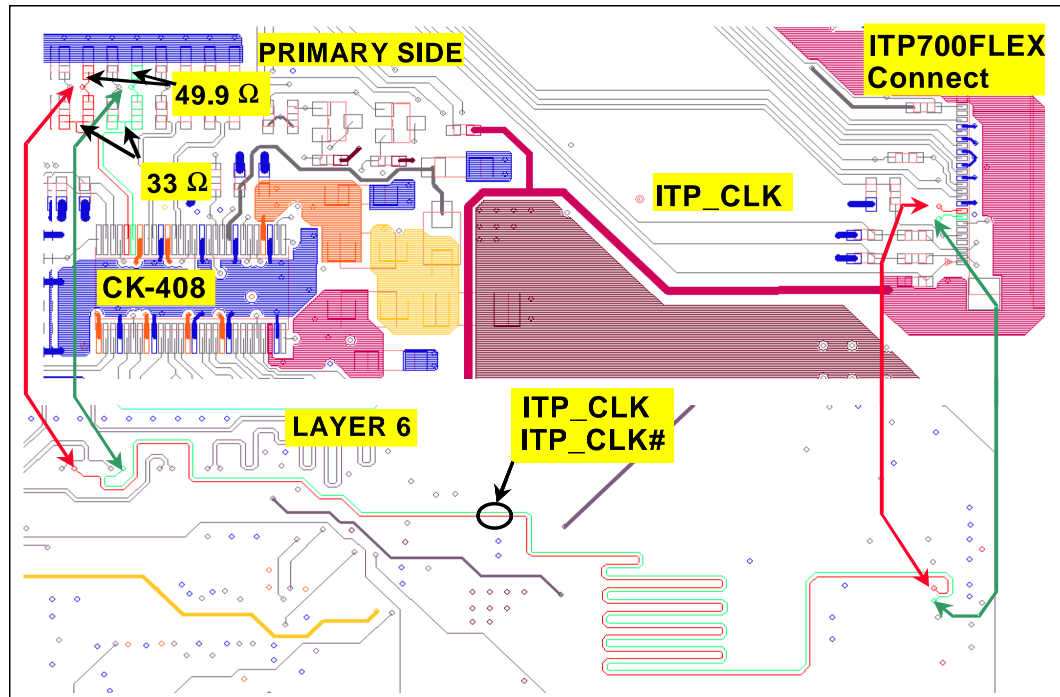
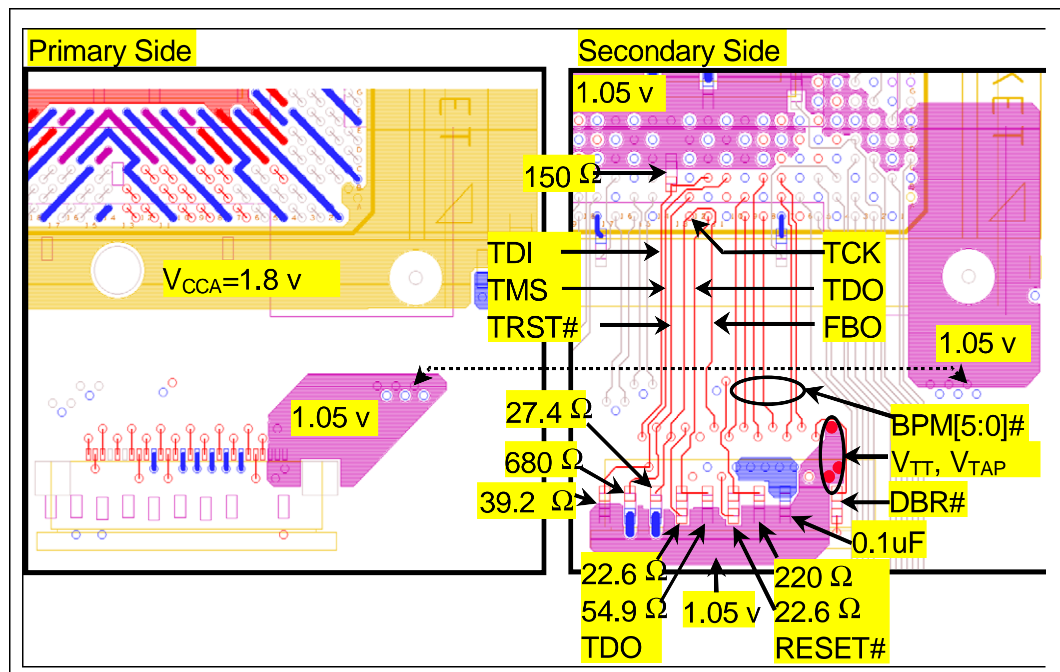


Figure 33 illustrates the ITP700FLEX signals layout example.

Figure 33. ITP700FLEX Signals Layout Example



4.3.1.3 ITP700FLEX Design Guidelines for Production Systems

For production systems that do not populate the onboard ITP700FLEX debug port connector, observe the following guidelines to ensure that all necessary signals are terminated properly.

Table 18 summarizes all signals that require termination when a system does not populate the ITP700FLEX connector but still implements the routing for all the signals. This includes TDI, TMS, TRST#, and TCK. Based on Intel's recommended values in this table, the resistor tolerances for TMS and TCK may be relaxed from ± 1 percent to ± 5 percent to reduce cost. Also, TDO may be left as no connect; thus, the 54.9 Ω ± 1% pull-up and 22.6 Ω ± 1% series resistors may be removed.

For the ITP700FLEX connector's RESET# input signal, remove the 220 Ω ± 5% resistor and the 22.6 Ω ± 1% series resistor.

The series 33 Ω and 49.9 Ω ± 1% parallel termination resistors on the ITP_CLK/ITP_CLK# differential host clock inputs to the ITP700FLEX connector may also be depopulated for production systems. The only requirement is that the BIOS should disable the third differential host clock pair routed from the CK-408 clock chip to the ITP700FLEX connector.

Finally, the 150 Ω to 240 Ω pull-up resistor for the DBR# output signal from the ITP700FLEX connector may or may not be depopulated, depending on how it affects the system reset logic that it is connected to. It is the system designer's responsibility to determine whether termination for DBR# is required for a given system implementation. The same is also true for DBA#, if implemented. This signal is not required and may be left as no connect. However, it is the system designer's responsibility to determine whether termination for DBA# is required.

4.3.2 Recommended ITP Interposer Debug Port Implementation

Intel is working with American Arium* to provide ITP interposer cards for use in debugging Pentium M processor-based systems as an alternative to the onboard ITP700FLEX in cases where the onboard connector cannot be supported. The ITP interposer card is an additional component that integrates a Pentium M processor socket along with ITP700 connector on a single interposer card that is compatible with the 478-pin Pentium M processor socket.

Table 18 summarizes all the signals that require termination for a system designed for use with the ITP interposer. This includes TDI, TMS, TRST#, and TCK. TDO may be left as a no connect.

DBR# should be routed to the system reset logic (e.g., the SYSRST# signal of the ICH4) and initiate the equivalent of a front panel reset commonly found in desktop systems. The 150 Ω to 240 Ω pull-up resistor should be placed within 1 ns of the ITP connector.

Note: The processor should **not** be power cycled when DBR# is asserted.

DBA# is an optional system signal that may be used to indicate to the system that the ITP/TAP port is being used. When not implemented, this signal may be left as no connect. When implemented, it should be routed with a 150 Ω to 240 Ω pull-up resistor placed within 1 ns of the ITP connector.

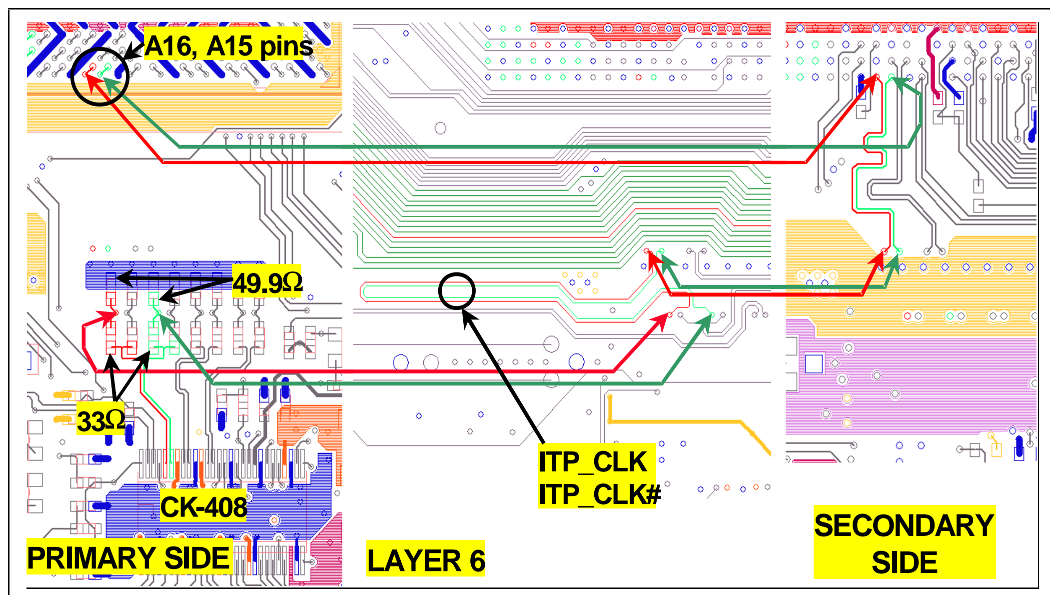
4.3.2.1 ITP_CLK Routing to ITP Interposer

A layout example for ITP_CLK/ITP_CLK# routing to the CPU socket for supporting an ITP interposer is shown in Figure 34. The CK-408 clock chip is mounted on the primary side layer of the motherboard and the differential clock pair also breaks out on the same side. The differential ITP clock pair routing also requires a pair of 33 Ω ± 5% series resistors placed within 0.5 inch of the clock chip output pins and followed by a pair of 49.9 Ω ± 1% termination resistors to ground. The majority of the ITP_CLK differential serpentine routing takes place on internal Layer 6 below the Pentium M processor/Celeron M processor FSB address signal routing.

Completion of ITP+CLK routing on Layer 6 is not possible due to Pentium M processor/Celeron M processor FSB routing on Layer 6. Therefore, the ITP_CLK differential pair then is routed to the secondary side layer to complete routing to the ITP_CLK (pin A16) and ITP_CLK# (pin A15) pins of the Pentium M processor/Celeron M processor while matching the BCLK[1:0] routing on the secondary side for a 507 mil length (see Figure 22 and description in Section 4.1.7). Routing to the CPU socket on the primary side layer is not possible because of the presence of the Vcca 1.8V or 1.5V plane flood along the A-signal side row of the pin-map. ITP_CLK routing to the ITP interposer should achieve the ± 50 ps length matching requirement of the BCLK[1:0] lines.

Figure 34 illustrates the ITP_CLK to CPU ITP interposer layout example.

Figure 34. ITP_CLK to CPU ITP Interposer Layout Example



4.3.2.2 ITP Interposer Design Guidelines for Production Systems

For production systems that do not use the ITP interposer, observe the following guidelines to ensure that all necessary signals are terminated properly.

Table 18 summarizes all the signals that require termination when a system does not use the ITP interposer. This includes TDI, TMS, TRST#, and TCK. TDO may be left as no connect.

The series 33 Ω and 49.9 Ω ± 1% parallel termination resistors on the ITP_CLK/ITP_CLK# differential host clock inputs to the processor socket may be depopulated for production systems. The only requirement is that the BIOS should disable the third differential host clock pair routed from the CK-408 clock chip to the Pentium M processor/Celeron M processor socket.

Finally, the 150 Ω to 240 Ω pull-up resistor for the DBR# output signal from processor socket may or may not be depopulated, depending on how it affects the system reset logic that it is connected to. It is the system designer's responsibility to determine whether termination for DBR# is required for a given system implementation. The same is also true for DBA#, if implemented. This signal is not required and may be left as no connect. However, it is the system designer's responsibility to determine whether termination for DBA# is required.

4.3.3 Logic Analyzer Interface (LAI)

Intel is working with Agilent Technologies, Inc.* to provide logic analyzer interfaces (LAIs) for use in debugging Pentium M processor/Celeron M processor-based systems. The following information is general; contact the LAI vendor for specific information about their LAIs.

Due to the complexity of a Pentium M processor/Celeron M processor-based system, the LAI is critical in providing the ability to probe and capture Pentium M processor/Celeron M processor system bus signals. Observe the following mechanical and electrical considerations when designing a Pentium M processor/Celeron M processor-based system that may use a LAI.

4.3.3.1 Mechanical Considerations

The LAI is installed between the processor socket and the Pentium M processor/Celeron M processor. The LAI pins plug into the socket, while the Pentium M processor in the 478-pin package plugs into a socket on the LAI. Cabling this part of the LAI egresses the system to allow an electrical connection between the Pentium M processor/Celeron M processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must ensure that system keepout volume remains unobstructed.

4.3.3.2 Electrical Considerations

The LAI also affects the electrical performance of the Pentium M processor/Celeron M processor system bus. Therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool works in the system. Contact the logic analyzer vendor for electrical specifications as load models for the LAI solution they provide.

4.4 Intel® Mobile Voltage Positioning IV

Contact your Intel Field Representative for more information on electrical requirements for the DC-to-DC voltage regulator for the Pentium M processor/Celeron M Processor.

System Memory Design Guidelines (DDR-SDRAM) 5

5.1 Introduction

The Intel® 855GME Chipset Double Data Rate (DDR) SDRAM system memory interface consists of SSTL-2 compatible signals. These SSTL-2 compatible signals have been divided into several signal groups: data, control, command, CPC, clock, and feedback signals.

Table 20 presents the signal grouping. Refer to the *Intel® 855GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet* for details on these signals.

Table 20. Intel® 855GME Chipset DDR Signal Groups

Group	Signal Name	Description
Clocks	SCK[5:0]	DDR-SDRAM differential clocks - (three per DIMM)
	SCK[5:0]#	DDR-SDRAM inverted differential clocks - (three per DIMM)
Data	SDQ[63:0]	Data bus
	SDQ[71:64]	Check bits for ECC function
	SDQS[8:0]	Data strobes
	SDM[8:0]	Data mask
Control	SCKE[3:0]	Clock enable - (one per Device Row)
	SCS[3:0]#	Chip select - (one per Device Row)
Command	SMA[12:6,3,0]	Memory address bus
	SBA [1:0]	Bank select
	SRAS#	Row address select
	SCAS#	Column address select
	SWE#	Write enable
CPC	SMA[5,4,2,1]	Command per clock (DIMM0)
	SMAB[5,4,2,1]	Command per clock (DIMM1)
Feedback	RCVENOUT#	Receive enable output (no external connection)
	RCVENIN#	Receive enable input (no external connection)

5.2 Length Matching and Length Formulas

The routing guidelines presented in the following subsections define Intel's recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching formulas are also provided that further restrict the minimum to maximum length range of each signal group with respect to clock, within the overall boundaries, as required to ensure adequate timing margins. These secondary constraints are referred to as length matching constraints and the formulas used are referred to as length matching formulas.

All signal groups, except feedback signals, are length matched to the DDR clocks. The clocks on a given DIMM are matched to within ± 25 mils of the target length. A different clock target length may be used for each DIMM. The difference in clock target lengths between DIMM0 and DIMM1 should not exceed one inch. Table 21 presents a simple summary of the length matching formulas for each signal group.

Table 21. Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock – 1.5 inches	Clock - 0.5 inch
Command to Clock	Clock – 1.5 inches	Clock + 1 inch
CPC to Clock	Clock – 1.5 inches	Clock - 0.5 inch
Strobe to Clock	Clock – 1.5 inches	Clock - 0.5 inch
Data to Strobe	Strobe – 25 mils	Strobe + 25 mils

NOTE: All length matching formulas are based on GMCH die-pad to DIMM pin total length.

Package length tables are provided for all signals to facilitate this pad-to-pin matching. Length formulas should be applied to each DIMM slot separately. The full geometry and routing guidelines along with the exact length matching formulas and associated diagrams are provided in the individual signal group guidelines sections to follow.

A DDR DIMM trace length calculator may be used to ensure layout trace lengths meet these recommendations. Contact the local Intel Field Representative for information on obtaining this tool.

5.3 Package Length Compensation

As mentioned above, all length matching is done for GMCH die-pad to DIMM pin. This is done to compensate for package length variation across each signal group in order. The Intel® 855GME chipset Graphics Memory Controller Hub (82855GME) does not equalize package lengths internally as some previous GMCH components have; the 82855GME requires a length matching or tuning process. The justification for this is based on the belief that length variance in the package based on ball position is naturally tuned out when the pin escape is completed to the edge of the package. Length matching in the package would then tend to create a mismatch at the package edge.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the

process of adjusting package length variation across a signal group. There is some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation where required.

5.4 Topologies and Routing Guidelines

The GMCH Double Data Rate (DDR) SDRAM system memory interface implements the low swing, high-speed, terminated SSTL_2 topology. This section contains information related to the recommended interconnect topologies and routing guidelines for each of the signal groups that comprise the DDR interface. When implemented as defined, these guidelines provide for a robust DDR solution on a GMCH chipset based design.

5.4.1 Clock Signals – SCK[5:0], SCK[5:0]#

The clock signal group includes the differential clock pairs SCK[5:0]/SCK[5:0]#. The GMCH generates and drives these differential clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. The GMCH only supports unbuffered DDR DIMMs. Three differential clock pairs are routed to each DIMM connector. Table 22 presents the clock signal mapping.

Table 22. Clock Signal Mapping

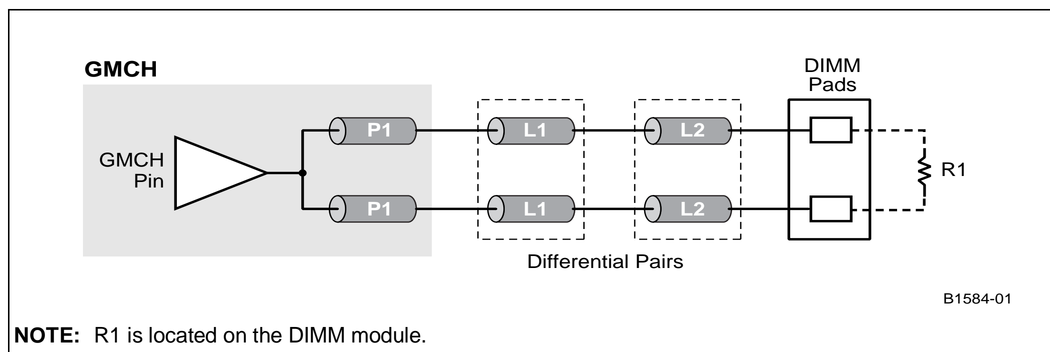
Signal	Relative To
SCK[2:0]/SCK[2:0]#	DIMM0
SCK[5:3]/SCK[5:3]#	DIMM1

5.4.2 Clock Topology Diagram

The 82855GME provides six differential clock output pairs, or three clock pairs per DIMM socket. Refer to the routing guidelines in Section 5.4.3 for detailed length and spacing rules for each segment. The clock signals should be routed as closely-coupled differential pairs over the entire length. Spacing to other DDR signals should not be less than 20 mils. Isolation spacing to non-DDR signals should be 25 mils.

Figure 35 illustrates the DDR clock routing topology (SCK[5:0]/SCK[5:0]#).

Figure 35. DDR Clock Routing Topology (SCK[5:0]/SCK[5:0]#)



NOTE: R1 is located on the DIMM module.

5.4.3 DDR Clock Routing Guidelines

Table 23 presents the DDR clock signal group routing guidelines.

Table 23. DDR Clock Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Definition
Signal Group	SCK[5:0] and SCK[5:0]#
Topology	Differential Pair Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	42 Ω ± 15%
Differential Mode Impedance (Zdiff)	70 Ω ± 15%
Nominal Trace Width (See exceptions for breakout region below.)	Inner Layers: 7 mils Outer Layers: 8 mils (pin escapes only)
Nominal Pair Spacing (edge to edge) (See exceptions for breakout region below)	Inner Layers: 4 mils Outer Layers: 5 mils (pin escapes only)
Minimum Pair-to-Pair Spacing (See exceptions for breakout region below.)	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other DDR Signals (See exceptions for breakout region below.)	20 mils
Minimum Isolation Spacing to Non-DDR Signals	25 mils
Maximum Via Count	2 (per side)
Package Length Range – P1	1000 mils ± 350 mils Refer to clock package length for exact lengths.
Trace Length Limits – L1	Max = 300 mils (breakout segment)
Length Limits – P1 + L1 + L2	Min = 3.5 inches Max = 6.5 inches
Total Length – P1 + L1 + L2	Total length target is determined by placement Total length for DIMM0 group = X0 Total length for DIMM1 group = X1

NOTES:
1. Pad-to-pin length tuning is used on clocks to achieve minimal variance. Package lengths range between approximately 600 mils and 1400 mils. Exact package lengths for each clock signal are provided at the end of this section. Overall target length should be established based on placement and routing flow. The resulting motherboard segment lengths must fall within the ranges specified.
2. The DDR clocks should be routed on internal layers, except for pin escapes. Intel recommends that pin escape vias be located directly adjacent to the ball pads on all clocks. Surface layer routing should be minimized.
3. Exceptions to the trace width and spacing geometries are allowed in the breakout region to fan-out the interconnect pattern. Reduced spacing should be avoided as much as possible.

Table 23. DDR Clock Signal Group Routing Guidelines (Sheet 2 of 2)

Parameter	Definition
SCK to SCK# Length Matching	Match total length to ±10 mils
Clock to Clock Length Matching (Total Length)	Match all DIMM0 clocks to X0 ± 25 mils Match all DIMM1 clocks to X1 ± 25 mils
Breakout Exceptions (Reduced geometries for MCH breakout region)	Inner Layers: 4 mil trace, 4 mil pair space allowed Outer Layers: 5 mil trace, 5 mil pair space allowed Pair-to-pair spacing of 5 mils allowed Spacing to other DDR signals of 5 mils allowed Maximum breakout length is 0.3 inch

NOTES:
1. Pad-to-pin length tuning is used on clocks to achieve minimal variance. Package lengths range between approximately 600 mils and 1400 mils. Exact package lengths for each clock signal are provided at the end of this section. Overall target length should be established based on placement and routing flow. The resulting motherboard segment lengths must fall within the ranges specified.
2. The DDR clocks should be routed on internal layers, except for pin escapes. Intel recommends that pin escape vias be located directly adjacent to the ball pads on all clocks. Surface layer routing should be minimized.
3. Exceptions to the trace width and spacing geometries are allowed in the breakout region to fan-out the interconnect pattern. Reduced spacing should be avoided as much as possible.

5.4.3.1 Clock Length Matching Requirements

The GMCH provides three differential clock pairs for each DIMM. A differential clock pair is made up of a SCK signal and its complement signal SCK#. Refer to Section 5.2 for more details on length matching requirements.

The differential pairs for one DIMM are:

SCK[0]/SCK[0]#
SCK[1]/SCK[1]#
SCK[2]/SCK[2]#

The differential pairs for the second DIMM are:

SCK[3]/SCK[3]#
SCK[4]/SCK[4]#
SCK[5]/SCK[5]#

The two sets of differential clocks must be length tuned on the motherboard such that any pair to pair package length variation is tuned out. The three pairs associated with DIMM0 are tuned to a fixed overall length, including package, and the three pairs associated with DIMM1 are tuned to a fixed overall length.

The two traces associated with each clock pair are length matched within the package, however some additional compensation may be required on the motherboard to achieve the ±10-mil length tolerance within the pair.

Between clock pairs the package length varies substantially. The motherboard length of each clock pair must be length adjusted to tune out package variance. The total length including package should be matched to within ± 25 mils of each other. This may result in a clock length variance of as much as 700 mils on the motherboard.

The first step in determining the routing lengths for clocks and all other clock-relative signal groups is to establish the target length for each DIMM clock group. These target lengths are shown as X0 and X1 in Figure 36.These are the lengths to which all clocks within the corresponding group are matched and the reference length values used to calculate the length ranges for the other signal groups.

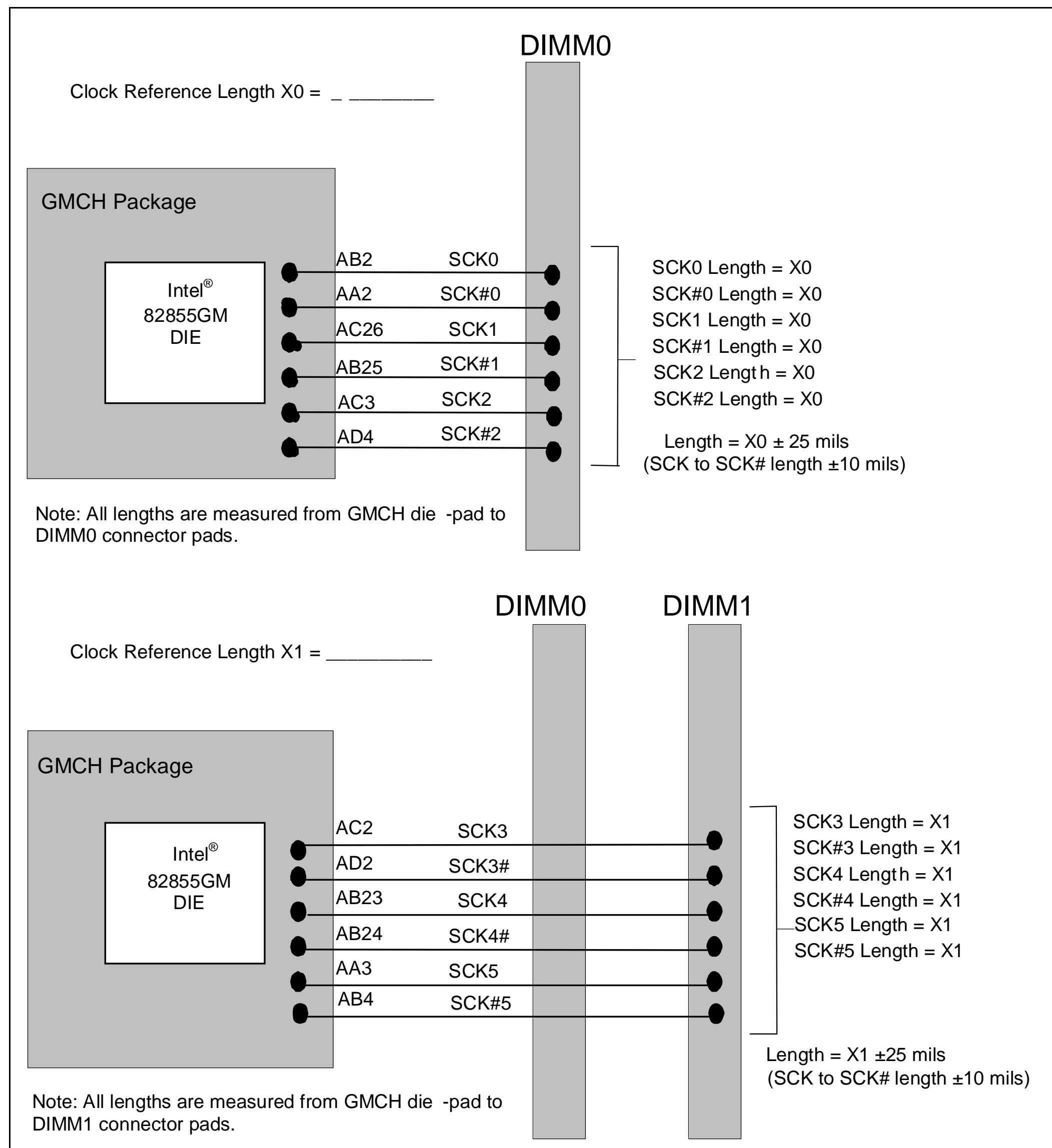
5.4.3.2 Clock Reference Lengths

The clock reference length for each DIMM clock group is calculated by first determining the longest total clock length required to complete the clock routing. A table of clock package lengths is provided in Table 24 to assist with this calculation. After the longest total length is determined for each clock group, this figure becomes a lower bound for the associated clock reference length. At this point it is helpful to have completed a test route of the SDQ/SDQS bus such that final clock reference lengths may be defined with consideration of the impact on SDQ/SDQS bus routability. Some iteration may be required.

Once the reference lengths X0 and X1 are defined then the next step is to tune each clock pair's motherboard trace segment lengths as required such that the overall length of each clock equals the associated clock reference length plus or minus the 25 mil tolerance. Again, the reference length for the two sets of clocks should be offset by the nominal routing length between SO-DIMM connectors.

Figure 36 illustrates the DDR clock trace length matching diagram.

Figure 36. DDR Clock Trace Length Matching Diagram



5.4.3.3 Clock Length Package Table

The package length data in Table 24 should be used to tune the motherboard length of each SCK/SCK# clock pair between the GMCH and the associated DIMM socket. Intel recommends that die-pad to DIMM pin length be tuned to within ± 25 mils to optimize timing margins on the interface.

Table 24. DDR Clock Package Lengths

Signal	Pin Number	Package Length (mils)
SCK[0]	AB2	1177
SCK[0]#	AA2	1169
SCK[1]	AC26	840
SCK[1]#	AB25	838
SCK[2]	AC3	1129
SCK[2]#	AD4	1107
SCK[3]	AC2	1299
SCK[3]#	AD2	1305
SCK[4]	AB23	643
SCK[4]#	AB24	656
SCK[5]	AA3	1128
SCK[5]#	AB4	1146

Package length compensation may be performed on each individual clock output thereby matching total length on SCK/SCK# exactly, or alternatively the average package length may be used for both outputs of a pair and length tuning done with respect to the motherboard portion only. Refer to Section 5.5.3 for more information.

5.4.4 Data Signals – SDQ[71:0], SDM[8:0], SDQS[8:0]

The GMCH data signals are source synchronous signals that include a 72-bit wide data bus, a set of eight data mask bits, and a set of eight data strobe signals. There is an associated data strobe and data mask bit for each of the eight data byte groups, making for a total of eight 10-bit byte lanes. This section summarizes the SDQ/SDM to SDQS routing guidelines and length matching recommendations.

- The data signals include SDQ[71:0], SDM[8:0], and SDQS[8:0].
- The data signals should transition from an external layer to an internal signal layer under the GMCH. Keep to the same internal layer until transitioning back to an external layer at the series resistor.
- After the series resistor, the signal should transition from the external layer to the same internal layer and route to DIMM0.
- At DIMM0, the signal should transition to an external layer and connect to the appropriate pad of the connector.
- After the DIMM0 transition, continue to route the signal on the same internal layer to DIMM1.
- Transition back out to an external layer and connect to the appropriate pad of DIMM1.

- Connection to the termination resistor should be through the same internal layer with a transition back to the external layer near the resistor. External trace lengths should be minimized.

To facilitate routing, swapping of the byte lanes is allowed for SDQ[63:0]. Bit swapping within the byte lane is also allowed for SDQ[63:0] only. The checkbits SDQ[71:64] cannot be byte lane swapped with another SDQ byte lane. Bit swapping within the SDQ[71:64] byte lane is not allowed. It is suggested that the parallel termination be placed on both sides of DIMM1 to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series (Rs) and parallel (Rt) data and strobe termination resistors, but data and strobe signals cannot be placed within the same R pack as the command or control signals. The tables and diagrams below present Intel's recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Intel recommends that the full data bus SDQ[63:0], mask bus SDM[7:0], and strobe signals SDQS[7:0] be routed on the same internal signal layer. It is required that the SDQ byte group and the associated SDM and SDQS signals within a byte lane be routed on the same internal layer.

The total length of SDQ, SDM, and SDQS traces between the GMCH and the DIMMs must be within the range defined in the overall guidelines, and is also constrained by a length range boundary based on SCK/SCK# clock length, and an SDQ/SDM to SDQS length matching requirement within each byte lane.

Note: All length matching must be done inclusive of package length. SDQ, SDM, and SDQS package lengths are provided in Table 27 to facilitate this process.

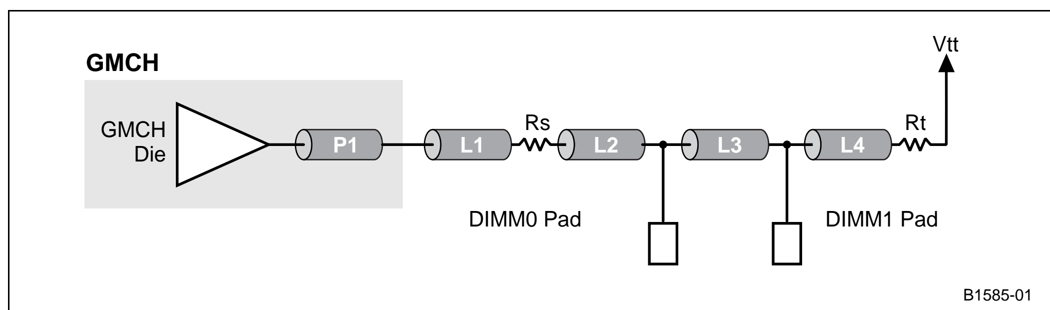
There are two levels of matching implemented on the data bus signals. The first is the length range constraint on the SDQS signals based on clock reference length. The second is SDQ/SDM to SDQS length matching within a byte lane. The length of the SDQS signal for each byte lane must fall within a range determined by the clock reference length, as defined in the SDQS to SCK/SCK# length matching section. The actual length of SDQS for each byte lane may fall anywhere within this range based on placement and routing flow.

After the SDQS length for a byte lane is established, the SDQ, SDM, and SDQS signals within the byte lane must be length matched to each other, inclusive of package length, as described in the SDQ to SDQS length matching section.

5.4.4.1 Data Bus Topology

Figure 37 illustrates the data signal routing topology.

Figure 37. Data Signal Routing Topology



The data signals should be routed using a 2:1 trace spacing to trace width ratio for signals within the DDR group, except for clocks and strobes. Data signals should be routed on inner layers with minimized external trace lengths.

Table 25 presents the data signal group routing guidelines.

Table 25. Data Signal Group Routing Guidelines

Parameter	Definition
Signal Group	SDQ[71:0], SDQS[8:0], SDM[8:0]
Motherboard Topology	Daisy Chain with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	SDQ/SDM: 2:1 (e.g., 8 mil space to 4 mil trace) SDQS: 3 to 1 (e.g., 12 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	700 mils ± 300 mils Refer to Table 27 for package length details.
Trace Length P1+ L1 – GMCH Die-Pad to Series Termination Resistor Pad	Min = 2 inches - L2 Max = 6 inches - L3 - L2
Trace Length L2 – Series Termination Resistor Pad to First DIMM Pad	Max = 0.75 inch
Total Length P1+ L1+L2 – Total Length from GMCH to First DIMM Pad	Min = 2 inches Max = 6 inches - L3
Trace Length L3 – First DIMM Pad to Last DIMM Pad	Min = 0.25 inch Max = 2 inches
Trace Length L4 – Last DIMM Pad to Parallel Termination Resistor Pad	Max = 1 inch
Total Length P1+ L1+L2+L3 – Total Length from GMCH to Second DIMM Pad	Min = 2 inches + L3 Max = 6 inches
Series Termination Resistor (Rs)	10 Ω ± 5%
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	6
Length Matching Requirements	Match SDQS to SCK/SCK# Refer to length matching Section 5.4.4.2 and Figure 38. SDQ/SDM to SDQS, to ± 25 mils, within each byte lane. Refer to length matching Section 5.4.4.3 and Figure 39.

NOTES:
1. Power distribution vias from Rt to Vtt are not included in this count.
2. The overall minimum and maximum length to the DIMM must comply with clock length matching requirements.

5.4.4.2 SDQS to Clock Length Matching Requirements

The first step in length matching is to determine the SDQS length range based on the SCK/SCK# reference length defined previously. The total length of the SDQS strobe signals, including package length, between the GMCH die-pad and the DIMMs must fall within the range defined in the formulas below. Refer to the clock section for the definition of the clock reference length. Refer to Table 25 for the definition of the various trace segments.

Length range formula for DIMM0:

X_0 = SCK[2:0]/SCK[2:0]# total reference length, including package length. Refer to Section 5.4.3.1 for more information.

Y_0 = SDQS[7:0] total length = GMCH package + L1 + L2, as shown in Figure 37, where:

$(X_0 – 1.5 \text{ inches}) \leq Y_0 \leq (X_0 - 0.5 \text{ inch})$

Length range formula for DIMM1:

X_1 = SCK[5:3]/SCK[5:3]# total reference length, including package length. Refer to Section 5.4.3.1 for more information.

Y_1 = SDQS[7:0] total length = GMCH package + L1 + L2 + L3, as shown in Figure 37 where:

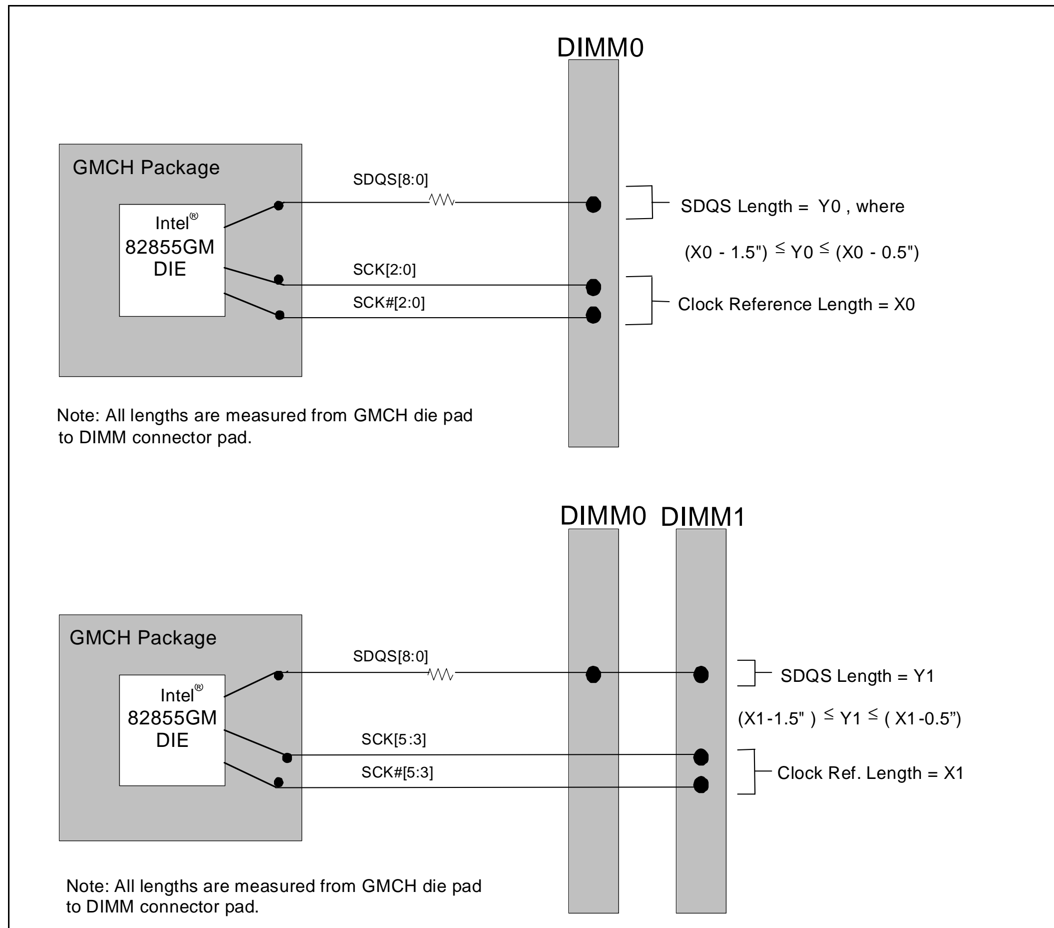
$(X_1 – 1.5 \text{ inches}) \leq Y_1 \leq (X_1 - 0.5 \text{ inch})$

Length matching is only performed from the GMCH to the DIMMs, and does not involve the length of L4, which may vary over its entire range. Intel recommends that routing segment length L3 between DIMM0 to DIMM1 be held fairly constant and equal to the offset between clock reference lengths X0 and X1. This produces the most straightforward length-matching scenario.

Note: A nominal SDQS package length of 700 mils may be used to estimate byte lane lengths prior to performing package length compensation.

Figure 38 illustrates the SDQS to clock trace length matching diagram.

Figure 38. SDQS to Clock Trace Length Matching Diagram



5.4.4.3 Data to Strobe Length Matching Requirements

The data bit signals SDQ[71:0] are grouped by byte lanes and associated with a data mask signal, SDM[8:0], and a data strobe, SDQS[8:0]. The guidelines are as follows:

For DIMM0, this length matching includes the motherboard trace length to the pads of the DIMM0 connector (L1 + L2) plus package length.

For DIMM1, the motherboard trace length to the pads of the DIMM1 connector (L1 + L2 + L3) plus package length.

Length range formula for SDQ and SDM:

X = SDQS total length, including package length, as defined previously

Y = SDQ, SDM total length, including package length, within same byte lane, where

$(X - 25 \text{ mils}) \le Y \le (X + 25 \text{ mils})$

Length matching is not required from the DIMM1 to the parallel termination resistors.

5.4.4.4 SDQ to SDQS Mapping

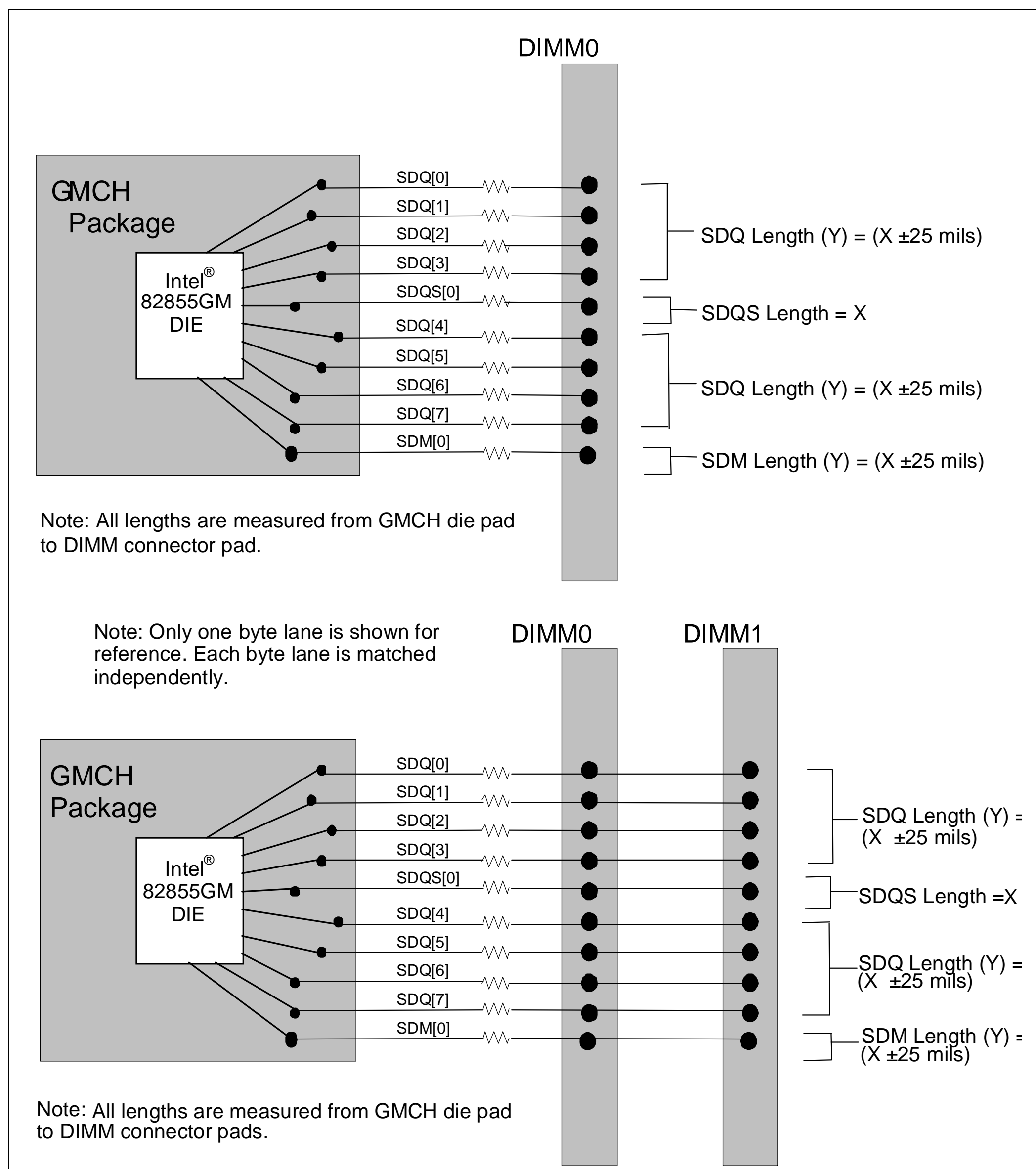
Table 26 defines the mapping between the nine byte lanes, nine mask bits, and the nine SDQS signals, as required to do the required length matching.

Table 26. SDQ/SDM to SDQS Mapping

Signal	Mask	Relative To
SDQ[7:0]	SDM[0]	SDQS[0]
SDQ[15:8]	SDM[1]	SDQS[1]
SDQ[23:16]	SDM[2]	SDQS[2]
SDQ[31:24]	SDM[3]	SDQS[3]
SDQ[39:32]	SDM[4]	SDQS[4]
SDQ[56:40]	SDM[5]	SDQS[5]
SDQ[55:48]	SDM[6]	SDQS[6]
SDQ[63:56]	SDM[7]	SDQS[7]
SDQ[71:64]	SDM[8]	SDQS[8]

Figure 39 illustrates the length matching requirements between the SDQ, SDM, and SDQS signals within a byte lane.

Figure 39. SDQ/SDM to SDQS Trace Length Matching Diagram



5.4.4.5 SDQ/SDQS Signal Package Lengths

The package length data in Table 27 should be used to tune the length of each SDQ, SDM, and SDQS motherboard trace as required to achieve the overall length matching requirements defined in the prior sections.

Table 27. DDR SDQ/SDM/SDQS Package Lengths (Sheet 1 of 2)

Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)
SDQ[0]	AF2	785	SDQ[32]	AH16	766
SDQ[1]	AE3	751	SDQ[33]	AG17	558
SDQ[2]	AF4	690	SDQ[34]	AF19	510
SDQ[3]	AH2	903	SDQ[35]	AE20	579
SDQ[4]	AD3	682	SDQ[36]	AD18	408
SDQ[5]	AE2	739	SDQ[37]	AE18	458
SDQ[6]	AG4	741	SDQ[38]	AH18	658
SDQ[7]	AH3	845	SDQ[39]	AG19	596
SDQ[8]	AD6	607	SDQ[40]	AH20	677
SDQ[9]	AG5	756	SDQ[41]	AG20	730
SDQ[10]	AG7	685	SDQ[42]	AF22	562
SDQ[11]	AE8	558	SDQ[43]	AH22	702
SDQ[12]	AF5	734	SDQ[44]	AF20	563
SDQ[13]	AH4	825	SDQ[45]	AH19	644
SDQ[14]	AF7	644	SDQ[46]	AH21	716
SDQ[15]	AH6	912	SDQ[47]	AG22	783
SDQ[16]	AF8	622	SDQ[48]	AE23	592
SDQ[17]	AG8	624	SDQ[49]	AH23	752
SDQ[18]	AH9	676	SDQ[50]	AE24	666
SDQ[19]	AG10	634	SDQ[51]	AH25	817
SDQ[20]	AH7	710	SDQ[52]	AG23	639
SDQ[21]	AD9	508	SDQ[53]	AF23	667
SDQ[22]	AF10	569	SDQ[54]	AF25	707
SDQ[23]	AE11	469	SDQ[55]	AG25	783
SDQ[24]	AH10	648	SDQ[56]	AH26	834
SDQ[25]	AH11	622	SDQ[57]	AE26	701
SDQ[26]	AG13	572	SDQ[58]	AG28	808
SDQ[27]	AF14	655	SDQ[59]	AF28	756
SDQ[28]	AG11	599	SDQ[60]	AG26	782
SDQ[29]	AD12	460	SDQ[61]	AF26	748
SDQ[30]	AF13	536	SDQ[62]	AE27	673

Table 27. DDR SDQ/SDM/SDQS Package Lengths (Sheet 2 of 2)

Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)
SDQ[31]	AH13	642	SDQ[63]	AD27	608
			SDQ[64]	AG14	566
			SDQ[65]	AE14	477
			SDQ[66]	AE17	571
			SDQ[67]	AG16	530
			SDQ[68]	AH14	701
			SDQ[69]	AE15	421
			SDQ[70]	AF16	491
			SDQ[71]	AF17	530
SDQS[0]	AG2	925	SDM[0]	AE5	838
SDQS[1]	AH5	838	SDM[1]	AE6	693
SDQS[2]	AH8	756	SDM[2]	AE9	538
SDQS[3]	AE12	466	SDM[3]	AH12	606
SDQS[4]	AH17	678	SDM[4]	AD19	492
SDQS[5]	AE21	487	SDM[5]	AD21	470
SDQS[6]	AH24	770	SDM[6]	AD24	557
SDQS[7]	AH27	858	SDM[7]	AH28	917
SDQS[8]	AD15	418	SDM[8]	AH15	685

5.4.5 Control Signals – SCKE[3:0], SCS[3:0]#

The GMCH control signals, SCKE[3:0] and SCS[3:0]#, are clocked into the DDR SDRAM devices using clock signals SCK[5:0]/SCK[5:0]#. The GMCH drives the control and clock signals together, with the clocks crossing in the valid control window. The GMCH provides one chip select (CS) and one clock enable (CKE) signal per DIMM physical device row. Two chip select and two clock enable signals are routed to each DIMM. Refer to Table 28 for the CKE and CS# signal to DIMM mapping.

Table 28. Control Signal to DIMM Mapping

Signal	Relative To	GMCH Pin
SCS#[0]	DIMM0	AD23
SCS#[1]	DIMM0	AD26
SCS#[2]	DIMM1	AC22
SCS#[3]	DIMM1	AC25
SCKE[0]	DIMM0	AC7
SCKE[1]	DIMM0	AB7
SCKE[2]	DIMM1	AC9
SCKE[3]	DIMM1	AC10

The control signal routing should transition from an external layer to an internal signal layer under the GMCH, keep to the same internal layer until transitioning back out to an external layer to connect to the appropriate pad of the DIMM connector and the parallel termination resistor. When the layout requires additional routing before the termination resistor, return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.

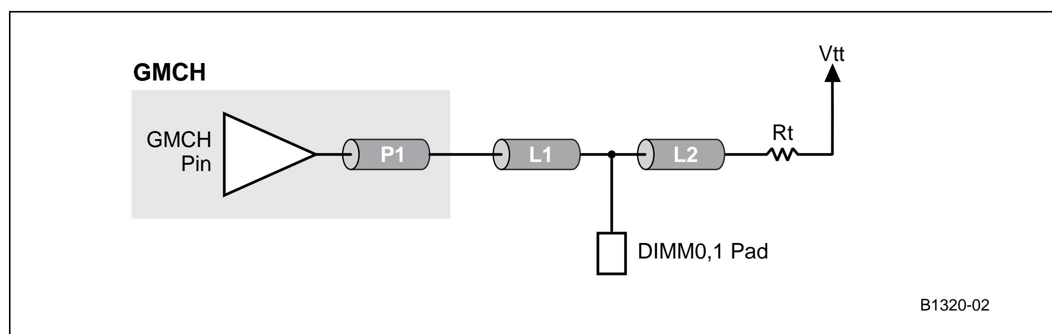
External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of return current continuous. Intel suggests that all control signals be routed on the same internal layer.

Resistor packs are acceptable for the parallel (Rt) control termination resistors, but control signals cannot be placed within the same R pack as the data or command signals. The table and diagrams below present Intel's recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

5.4.5.1 Control Signal Routing Topology

Figure 40 illustrates the control signal routing topology.

Figure 40. Control Signal Routing Topology



The control signals should be routed using 2:1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. Control signals should be routed on inner layers with minimized external trace lengths.

5.4.5.2 Control Signal Routing Guidelines

Table 29 presents the control signal routing guidelines.

Table 29. Control Signal Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SCKE[3:0], SCS[3:0]#
Motherboard Topology	Point-to-Point with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2:1 (e.g., 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils ± 250 mils Refer to Table 30 for package length details.
Trace Length P1 + L1 – GMCH Die-Pad to DIMM Pad	Min = 2 inches Max = 6 inches
Trace Length L2 – DIMM Pad to Parallel Termination Resistor Pad	Max = 2 inches
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	3
Length Matching Requirements	Match CTRL to SCK[5:0]/SCK[5:0]# Refer to length matching in Section 5.4.5.3 and Figure 41.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. It is possible to route using two vias if one via is shared that connects to the DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the DIMM must comply with clock length matching requirements.

5.4.5.3 Control to Clock Length Matching Requirements

The length of the control signals, between the GMCH die-pad and the DIMM must fall within the range defined below, with respect to the associated clock reference length. Refer to Figure 40 for a definition of the various trace segments that make up this path. The length of trace from the DIMM to the termination resistor need not be length matched. The length matching requirements are also shown in Figure 41.

Length range formula for DIMM0:

X_0 = SCK[2:0]/SCK[2:0]# total reference length, including package length. Refer to Section 5.4.3.1 for more information.

Y_0 = SCS[1:0]# and SCKE[1:0] total length = GMCH package length + L1, as shown in Figure 40, where:

$(X_0 – 1.5 \text{ inches}) \leq Y_0 \leq (X_0 - 0.5 \text{ inch})$

Length range formula for DIMM1:

X_1 = SCK[5:3]/SCK[5:3]# total reference length, including package length. Refer to Section 5.4.3.1 for more information.

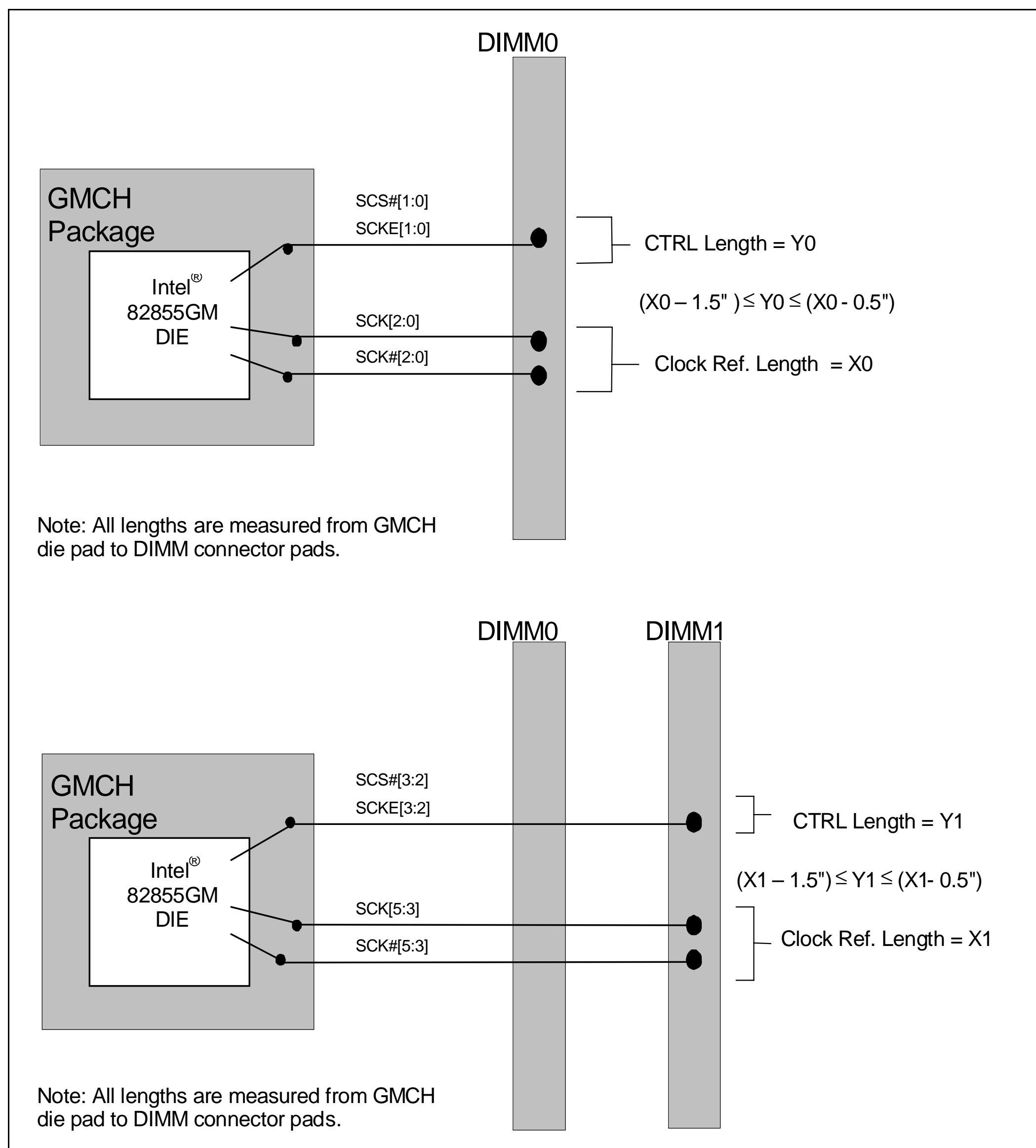
Y_1 = SCS[3:2]# and SCKE[3:2] total length = GMCH package length + L1, as shown in Figure 40, where:

$(X_1 – 1.5 \text{ inches}) \leq Y_1 \leq (X_1 - 0.5 \text{ inch})$

No length matching is required from the DIMM to the termination resistor. A nominal CS/CKE package length of 500 mils may be used to estimate baseline Mbyte lengths.

Figure 41 illustrates the length matching requirements between the control signals and clock.

Figure 41. Control Signal to Clock Trace Length Matching Diagram



5.4.5.4 Control Group Package Length Table

The package length data in the Table 30 should be used to match the overall length of each command signal to its associated clock reference length.

Note: Due to the relatively small variance in package length and adequate timing margins it is acceptable to use a fixed 500 mil nominal package length for all control signals, thereby reducing the complexity of the motherboard length calculations.

Table 30. Control Group Package Lengths

Signal	Pin Number	Package Length (mils)
SCS[0]#	AD23	502
SCS[1]#	AD26	659
SCS[2]#	AC22	544
SCS[3]#	AC25	612
SCKE[0]	AC7	443
SCKE[1]	AB7	389
SCKE[2]	AC9	386
SCKE[3]	AC10	376

5.4.6 Command Signals – SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#

The 82855GME command signals, SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, and SWE#, are clocked into the DDR SDRAMs using the clock signals SCK[5:0]/SCK[5:0]#. The GMCH drives the command and clock signals together, with the clocks crossing in the valid command window. The command signal group is supported by a daisy-chain topology.

5.4.6.1 Command Signal Routing Topology

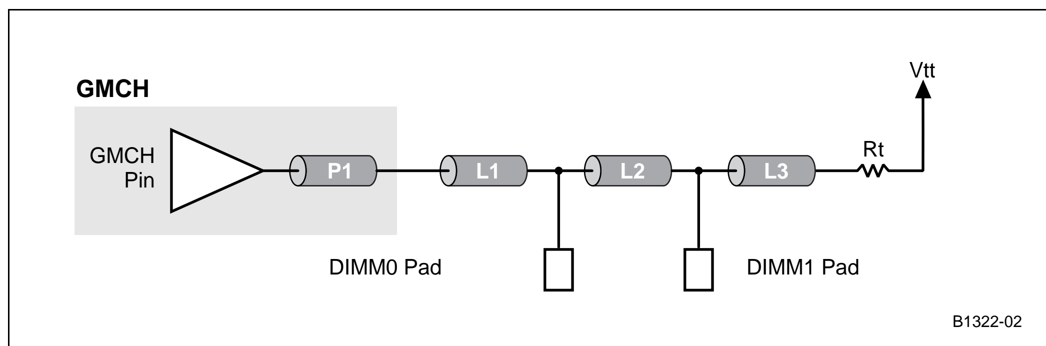
The command signal routing should transition from an external layer to an internal signal layer under the GMCH. Keep the same internal layer until transitioning to an external layer immediately prior to connecting the DIMM0 connector pad. At the via transition for DIMM0, continue the signal route on the same internal layer until transitioning back out to an external layer to connect to the pad of DIMM1. After DIMM1, transition to the same internal layer or stay on the external layer and route the signal to Rt.

Intel suggests that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the parallel command termination resistors but command signals cannot be placed within the same R-packs as data, strobe, or control signals.

Figure 42 illustrates the command routing for topology.

Figure 42. Command Routing for Topology



The command signals should be routed using a 2:1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. Command signals should be routed on inner layers with minimized external traces.

5.4.6.2 Command Topology Routing Guidelines

Table 31 presents Intel's recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to DIMM0 and DIMM1.

Table 31. Command Topology Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines
Signal Group	SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#
Motherboard Topology	Daisy-Chain with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2:1 (e.g., 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils ± 250 mils Refer to Table 32 for package length details.
Trace Length P1+ L1	Min = 2 inches Max = 5.5 inches
Trace Length P1+ L1+L2+L3	Max = 7.5 inches
Trace Length L2 – Total DIMM to DIMM spacing	Max = 2 inches

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the DIMM must comply with clock length matching requirements.
4. It is possible to route using three vias if one via is shared that connects to the DIMM1 pad and parallel termination resistor.

Table 31. Command Topology Routing Guidelines (Sheet 2 of 2)

Parameter	Routing Guidelines
Trace Length L3 – Second DIMM Pad to Parallel Resistor Pad	Max = 1.5 inches
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	6
Length Matching Requirements	CMD to SCK/SCK# Refer to length matching Section 5.4.6.3 and Figure 43 for details.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the DIMM must comply with clock length matching requirements.
4. It is possible to route using three vias if one via is shared that connects to the DIMM1 pad and parallel termination resistor.

5.4.6.3 Command Topology Length Matching Requirements

The routing length of the command signals, between the GMCH die-pad and the DIMM must be within the range defined below, with respect to the associated clock reference length. Refer to Figure 42 for a definition of the various motherboard trace segments. The length of trace from the DIMM to the termination resistor need not be length matched.

Length range formula for DIMM0:

X_0 = SCK[2:0]/SCK[2:0]# total reference length, including package length. Refer to Section 5.4.3.1 for more information.

Y_0 = CMD signal total length = GMCH package + L1, as shown in Figure 42, where:

$(X_0 - 1.5 \text{ inches}) \leq Y_0 \leq (X_0 + 1 \text{ inch})$

Length range formula for DIMM1:

X_1 = SCK[5:3]/SCK[5:3]# total reference length, including package length. Refer to Section 5.4.3.1 for more information.

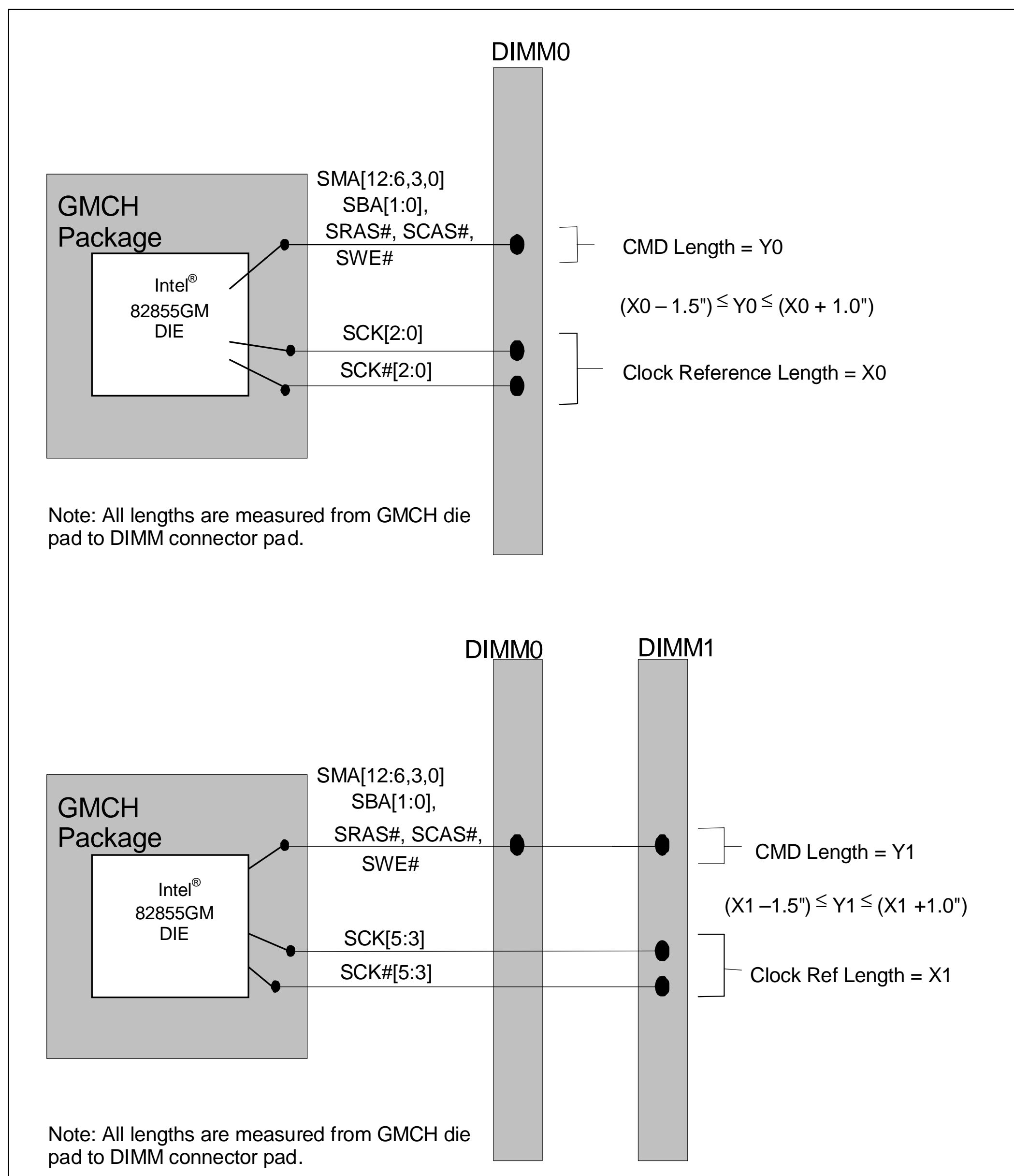
Y_1 = CMD signal total length = GMCH package + L1 + L2 + L3, as shown in Figure 42, where:

$(X_1 - 1.5 \text{ inches}) \leq Y_1 \leq (X_1 + 1 \text{ inch})$

No length matching is required from DIMM1 to the termination resistor. A nominal CMD package length of 500 mils may be used to estimate baseline motherboard lengths. Refer to Section 5.3 for more details on package length compensation.

Figure 43 illustrates the length matching requirements between the command signals and clock.

Figure 43. Topology Command Signal to Clock Trace Length Matching Diagram



5.4.6.4 Command Group Package Length Table

The package length data in Table 32 should be used to match the overall length of each command signal to its associated clock reference length.

Table 32. Command Group Package Lengths

Signal	Pin Number	Pkg Length (mils)
SMA[0]	AC18	420
SMA[3]	AD17	472
SMA[6]	AD8	591
SMA[7]	AD7	596
SMA[8]	AC6	630
SMA[9]	AC5	681
SMA[10]	AC19	377
SMA[11]	AD5	683
SMA[12]	AB5	609
SBA[0]	AD22	592
SBA[1]	AD20	435
SCAS#	AC24	562
SRAS#	AC21	499
SWE#	AD25	751

5.4.7 CPC Signals – SMA[5,4,2,1], SMAB[5,4,2,1]

The 82855GME control signals, SMA[5,4,2,1] and SMAB[5,4,2,1], are common clocked signals. They are clocked into the DDR SDRAM devices using clock signals SCK[5:0]/SCK[5:0]#. The GMCH drives the CPC and clock signals together, with the clocks crossing in the valid control window. The GMCH provides one set of CPC signals per DIMM slot. Refer to Table 33 for the SMA and SMAB signal to DIMM mapping.

Table 33. Control Signal to DIMM Mapping

Signal	Relative To	GMCH Pin
SMA[1]	DIMM0	AD14
SMA[2]	DIMM0	AD13
SMA[4]	DIMM0	AD11
SMA[5]	DIMM0	AC13
SMAB[1]	DIMM1	AD16
SMAB[2]	DIMM1	AC12
SMAB[4]	DIMM1	AF11
SMAB[5]	DIMM1	AD10

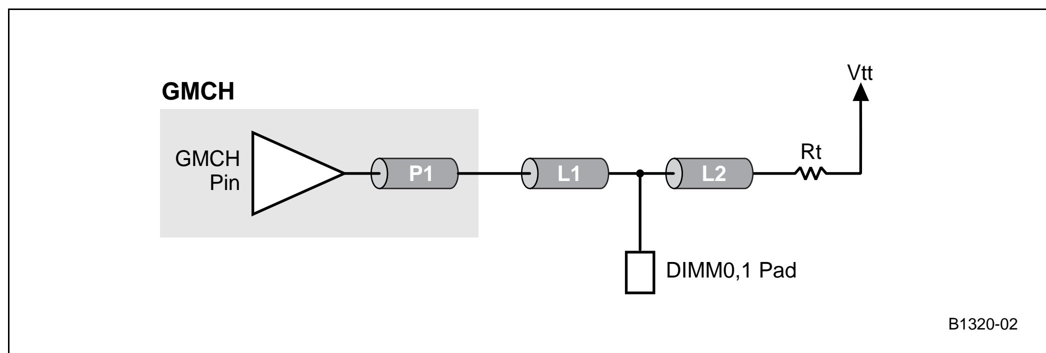
The guidelines below should be followed.

- The CPC signal routing should transition from an external layer to an internal signal layer under the GMCH.
- Keep to the same internal layer until transitioning back out to an external layer to connect to the appropriate pad of the SO-DIMM connector and the parallel termination resistor.
- If the layout requires additional routing before the termination resistor, return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.
- External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths.
- All internal and external signals should be ground reference to keep the path of return current continuous. Intel suggests that all CPC signals be routed on the same internal layer.
- Resistor packs are acceptable for the parallel (Rt) CPC termination resistors. Figure 44 and Figure 34 present the recommended topology and layout routing guidelines for the DDR-SDRAM CPC signals.

5.4.7.1 CPC Signal Routing Topology

Figure 44 illustrates the CPC control signal routing topology.

Figure 44. CPC Control Signal Routing Topology



The CPC signals should be routed using 2:1 trace space to width ratio for signals within the DDR group, except clocks and strobes. CPC signals should be routed on inner layers with minimized external trace lengths.

5.4.7.2 CPC Signal Routing Guidelines

Table 34 presents CPC control signal routing guidelines.

Table 34. CPC Control Signal Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[5,4,2,1], SMAB[5,4,2,1]
Motherboard Topology	Point-to-Point with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2:1 (e.g., 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils ± 250 mils Refer to Table 35 for package length details.
Trace Length P1+ L1	Min = 2 inches Max = 6 inches
Trace Length L2 – DIMM Pad to Parallel Termination Resistor Pad	Max = 2 inches
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	3
Length Matching Requirements	Match CPC to SCK[5:0]/SCK[5:0]# Refer to length matching Section 5.4.7.3 and Figure 45 for details.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. It is possible to route using two vias if one via is shared that connects to the DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the DIMM must comply with clock length matching requirements.

5.4.7.3 CPC to Clock Length Matching Requirements

The total length of the CPC signals, between the GMCH die-pad and the DIMM must fall within the range defined below, with respect to the associated clock reference length. Refer to Figure 44 for a definition of the various trace segments. The length the trace from the DIMM to the termination resistor need not be length matched. The length matching requirements are also shown in Figure 45. A table of CPC signal package length is provided at the end of this section.

Length range formula for DIMM0:

X_0 = SCK[2:0]/SCK[2:0]# total reference length, including package length. Refer to Section 5.4.3.1 for more information.

Y_0 = SMA[5,4,2,1] total length = GMCH Package + L1, as shown in Figure 44, where:

$(X_0 - 1.5 \text{ inches}) \leq Y_0 \leq (X_0 - 0.5 \text{ inch})$

Length range formula for DIMM1:

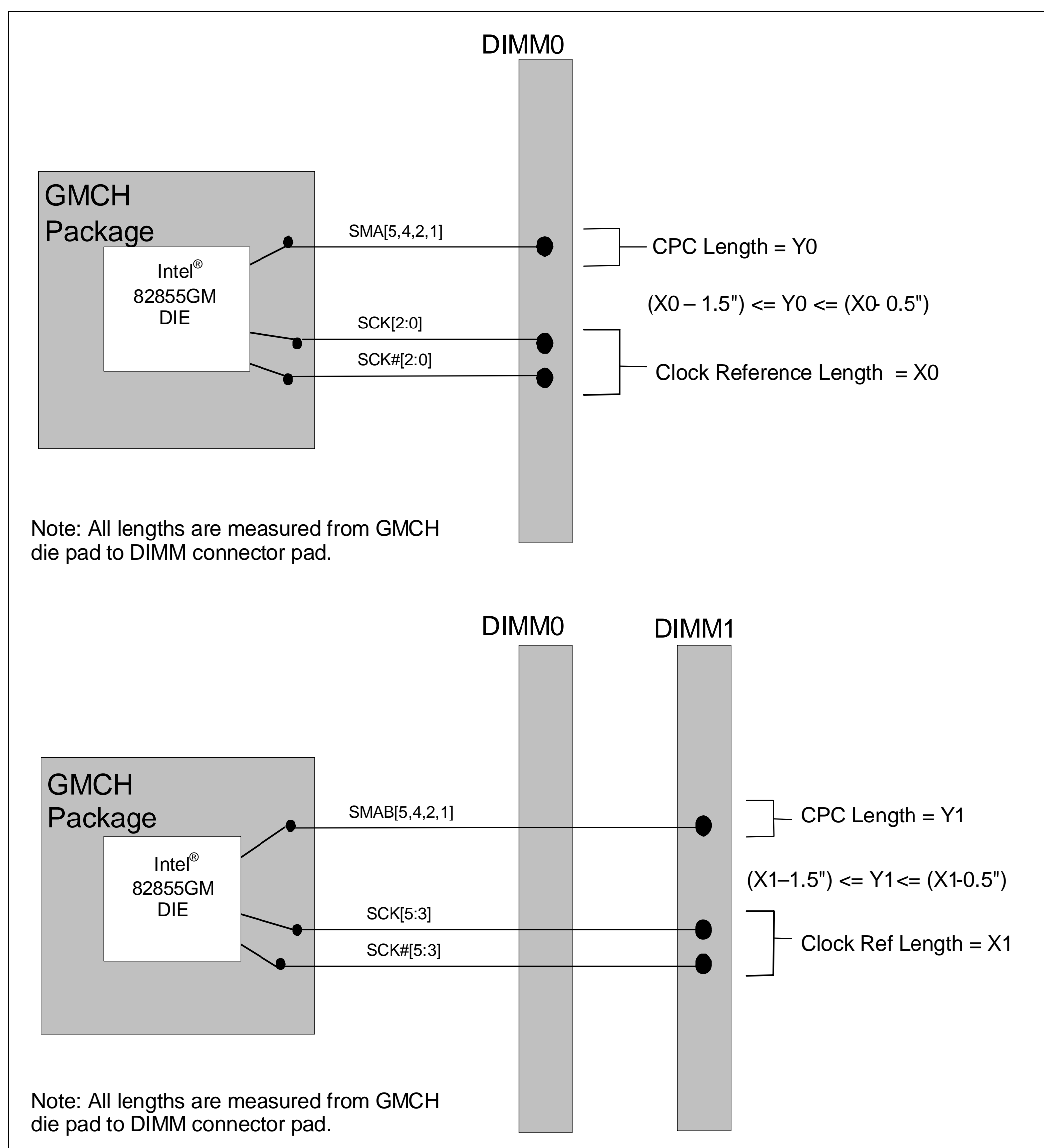
X_1 = SCK[5:3]/SCK[5:3]# total reference length, including package length. Refer to Section 5.4.3.1 for more information.

Y_1 = SMAB[5,4,2,1] total length = GMCH Package + L1, as shown in Figure 44, where:

$(X_1 – 1.5 \text{ inches}) \le Y_1 \le (X_1 - 0.5 \text{ inch})$

No length matching is required from DIMM1 to the termination resistor. Figure 45 illustrates the length matching requirements between the CPC signals and clock. A nominal CPC package length of 500 mils may be used to estimate baseline motherboard lengths.

Figure 45. CPC Signals to Clock Length Matching Diagram



5.4.7.4 CPC Group Package Length Table

The package length data in Table 35 should be used to match the overall length of each CPC signal to its associated clock reference length.

Table 35. CPC Group Package Lengths

Signal	Pin Number	Pkg Length (mils)
SMA[1]	AD14	398
SMA[2]	AD13	443
SMA[4]	AD11	430
SMA[5]	AC13	346
SMAB[1]	AD16	427
SMAB[2]	AC12	395
SMAB[4]	AF11	716
SMAB[5]	AD10	631

5.4.8 Feedback – RCVENOUT#, RCVENIN#

The 82855GME provides a feedback signal called ‘receive enable’ (RCVENIN#), which is used to measure timing for memory read data. The Intel® 855GME chipset has the RCVENOUT# signal shunted directly to RCVENIN# inside the package to reduce timing variation. With this change it is no longer necessary to provide an external connection. However, Intel recommends that both signals be transitioned to the bottom side with vias located adjacent to the package ball to facilitate probing.

5.5 ECC Guidelines

The GMCH may be configured to operate in an ECC data integrity mode that allows multiple bit error detection and single bit error correction. This option to design for and support ECC DDR memory modules is dependent on design objectives. By default ECC functionality is disabled on the platform.

5.5.1 Graphics Limitations Using ECC Memory

Memory with ECC enabled requires additional system memory resources. This will cause the integrated graphics engine to have less memory bandwidth for access to the graphics frame buffer. ECC memory is supported with internal graphics only. For additional information, refer to the Intel® 855GME Chipset *Graphics and Memory Controller Hub (GMCH) Specification Update Addendum (for embedded designs only, document 274004)*.

5.5.2 GMCH ECC Functionality

When non-ECC memory modules are to be the only supported memory type on the platform, the eight DDR check bits signals, associated strobe and data mask bit associated with the ECC device for each DIMM may be left as no connects on the GMCH.

Note: All three differential clocks per DDR DIMM must be routed and driven to each respective DIMM connector, regardless of ECC support.

For the GMCH, this includes SDQ[71:64], SDQS8, and SDM8. The DRAM Data Integrity Mode (DDIM) bit of the DRC register (Device 0; Offset 7C-7Fh; bit 21) provides the option to enable or disable ECC operation mode in the GMCH. By default, this bit is set to '0' and ECC functionality is disabled. In such a case, the SDQ[71:64] and SDQS8 pins of the GMCH may be left as no connects.

On platforms where ECC memory is supported, it is important that all relevant SDQ and SDQS signals to the DIMMs be disabled when the system is populated with only non-ECC or a combination of ECC and non-ECC memory. In such cases, the registers mentioned in the next section must be programmed appropriately.

5.5.3 DRAM Clock Flexibility

The DRAM Clock Control Disable Register (DCLKDIS: I/O Address 2E-2Fh) and the DRAM Controller Power Management Control Register, bit 10, (PWRMG: I/O Address 68-6Bh) provides the capability to enable and disable the CS/CKE and SCK signals to unpopulated DIMMs. The GMCH provides the flexibility to route any differential clock pair to any SCK clock pair on the DIMMs provided that the BIOS enables/disables these clocks appropriately (e.g., the GMCH's SCK0 pair may be routed either to the DIMM's SCK0 pair or any other pair such as SCK1 or SCK2, etc.). By default, the enable/disable bits for the clock pairs are set to '1' and are disabled or tri-stated.

5.6 External Thermal Sensor Based Throttling (ETS#)

The GMCH's ETS# input pin is an active low input that can be used with an external thermal sensor to monitor the temperature of the DDR SO-DIMMs for a possible thermal condition. Assertion of ETS# will result in the limiting of DRAM bandwidth on the DDR memory interface to reduce the temperature in the vicinity of the system memory.

By default, the functionality and input buffer associated with ETS# are disabled. Also, the GMCH can be programmed to send an SERR, SCI, or SMI message to the ICH4 upon the assertion of this signal. External thermal sensors that are suitable for the purpose described above would need to have a small form factor and be able to accurately monitor the ambient temperature in the vicinity of the DDR system memory.

Intel is in the process of enabling this feature on the Intel 855GME chipset GMCH and is actively engaging with thermal sensor vendors to ensure compatibility and suitability of vendors' products with the ETS# pin. This includes electrical design guidelines for the ETS# pin and usage/placement guidelines of the thermal sensors for maximum effectiveness. Current third-party vendor product offerings that may be suitable for the ETS# pin application include ambient temperature thermal

sensors and remote diode thermal sensors. Also, thermal sensors that implement an open-drain output for signaling a thermal event would provide the most flexibility from electrical and layout design perspectives.

5.6.1 ETS# Usage Model

The thermal sensors targeted for this application with the GMCH's ETS# are planned to be capable of measuring the ambient temperature only and should be able to assert ETS# if the preprogrammed thermal limits/conditions are met or exceeded. Because many variables within a mobile system can affect the temperature measured at any given point in a system, the expected usage and effectiveness of ETS# is also very focused. Because of factors such as thermal sensor placement, airflow within a mobile chassis, adjacent components, thermal sensor sensitivity, and thermal sensor response time, ETS# can effectively be used for controlling skin temperatures. However, due to the location of the thermal sensor, ETS# should not be used for measuring or controlling the Tj or Tcase parameters of DDR-SDRAM devices since it cannot respond quickly enough to dynamic changes in DRAM power.

5.6.2 ETS# Design Guidelines

ETS#, as implemented in the GMCH, is an active low signal and does **not** have an integrated pull-up to maintain a logic 1. As a result of this, an external 8.2 kΩ. to 10 kΩ. pull-up resistor should be provided near the ETS# pin, connected to 3.3 V. Ideally, the thermal sensor should implement an open drain type output buffer to drive ETS#. A system is expected to have one thermal sensor per SO-DIMM connector on the motherboard.

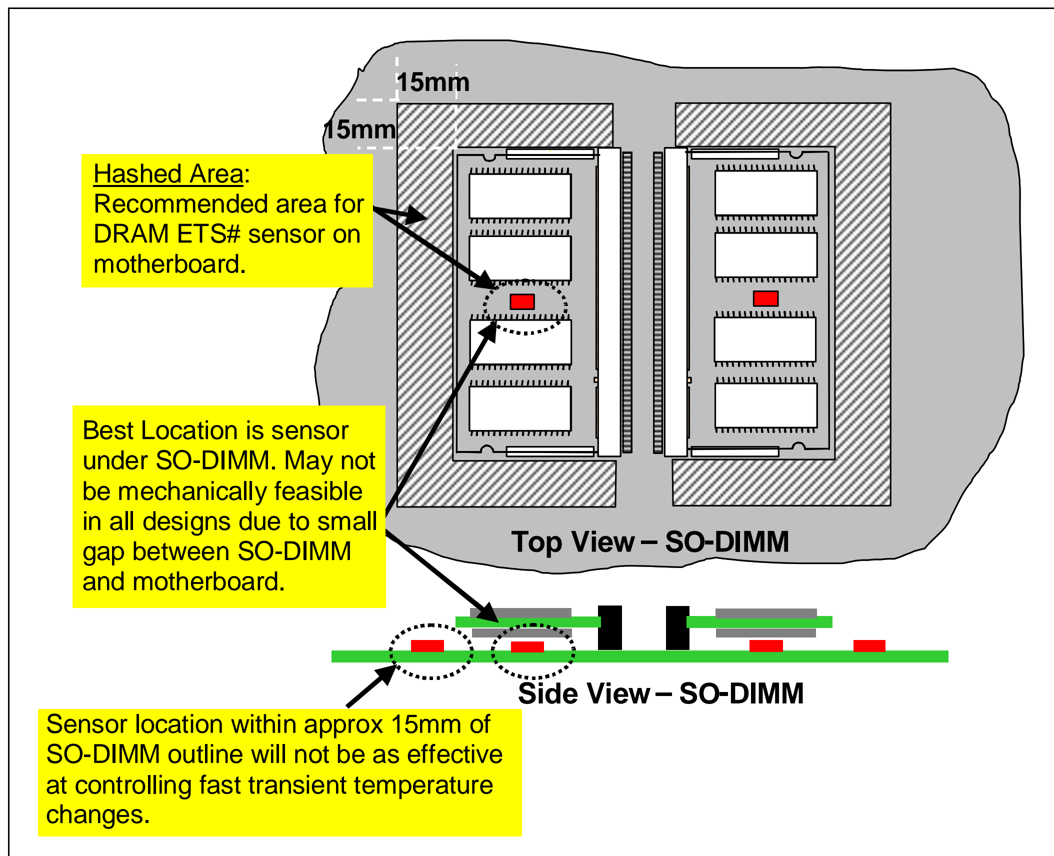
5.6.3 Thermal Sensor Routing and Placement Guidelines

Routing guidelines and other special motherboard design considerations will vary with the vendor and type of thermal sensor chosen for this ETS# application. As a result, vendor specific design guidelines should also be followed closely to ensure proper operation of this feature. As a general rule, system designers should follow good design practices in ensuring good signal integrity on this signal as well as achieving adequate isolation from adjacent signals. Also, any thermal design considerations (e.g. proper ground flood placement underneath the external thermal sensor, proper isolation of the differential signal routing for thermal diode applications, etc.) for the external thermal sensor itself should also be met.

The factors that can affect the accuracy of thermal sensors' ambient temperature measurements make sensor placement a critical and challenging task. Ideally, one thermal sensor should be placed near each SO-DIMM in a system. The thermal sensor should be located in an area where the effects of airflow and conduction from adjacent components are minimized. This allows for the best correlation of thermal sensor temperature to chassis or notebook surface temperature. See Figure 46 for details.

Assuming airflow is negligible within a system, the optimal placement of the thermal sensor is on the surface of the motherboard directly beneath the shadow of an SO-DIMM module centered longitudinally and laterally in relation to the outline of the SO-DIMM. The thermal sensor should have a form factor small enough to allow it to fit beneath double-sided memory modules (i.e., modules with memory devices on both sides of a module). If placement within the outline of an SO-DIMM is not possible, then the next best option is to locate it within approximately 15 mm (0.6 inches) of the outline/SO-DIMM shadow. Again, this assumes negligible effects from airflow.

Figure 46. DDR Memory Thermal Sensor Placement



Integrated Graphics Display Port 6

The GMCH contains four display ports: an analog CRT port, a dedicated LVDS port, and two 12-bit Digital Video Out (DVO) ports. Section 6.1 discusses the CRT and RAMDAC routing requirements. Section 6.2 discusses the dedicated LVDS port. Section 6.3 discusses the DVOB and DVOC design guideline. Section 6.4 provides recommendations for a flexible modular design guideline for DVOB and DVOC muxed interfaces. Section 6.5 provides recommendations for the GPIO signal group.

6.1 Analog RGB/CRT Guidelines

6.1.1 RAMDAC/Display Interface

The GMCH integrated graphics/chipset design interfaces to an analog display using a RAMDAC. The RAMDAC is a subsection of the graphics controller display engine and consists of three identical 8-bit digital-to-analog converter (DAC) channels, one for the display's red, green, and blue electron guns.

Each RGB output is doubly terminated with a 75 Ω resistor: One 75 Ω resistor is connected from the DAC output to the board ground, and the other termination resistor exists within the display. The equivalent DC resistance at the output of each DAC is 37.5 Ω. The current output from each DAC flows into this equivalent resistive load to produce a video voltage, without the need for external buffering. There is also an LC pi-filter on each channel that is used to reduce high-frequency noise and to reduce EMI. To maximize performance, the filter impedance, cable impedance, and load impedance should be matched.

Since the DAC runs at speeds up to 350 MHz, special attention should be paid to signal integrity and EMI, RGB routing, component placement, component selection, and cable and load impedance (monitor). They all play a large role in the analog display's quality and robustness. This holds true for all resolutions, but especially for those at 1600 x 1200 resolutions or higher.

6.1.2 Reference Resistor (REFSET)

A reference resistor, REFSET, is used to set the reference current for the DAC. This resistor is an external resistor with a one percent tolerance that is placed on the circuit board. A reference resistor may be selected from a range between 124 Ω to 137 Ω (one percent). Based on board design, DAC RGB outputs may be measured when the display is completely white. When the RGB voltage value is between 665 mV and 770 mV, the video level is within VESA specification and the resistor value that was chosen is optimal for board design.

Use this formula to calculate the value of REFSET.

$$REFSET = \frac{V_{reference}}{I_{reference}} = \frac{V_{bg}/4}{32 \cdot 73.2\mu A}$$

Intel recommends using a 137 Ω, one percent resistor for REFSET. See Figure 48 for Intel's recommended REFSET resistor placement.

A reference voltage is generated on the GMCH from a bandgap voltage reference circuit. The bandgap reference voltage level is approximately 1.2 V and this voltage is divided by four to generate the reference voltage. The VESA video standard defines the LSB current for each DAC channel. The RAMDAC reference current is designed on-die to be equal to 32LSB.

6.1.3 RAMDAC Board Design Guidelines

Take care when routing the analog RAMDAC signals. This is especially true to successfully support high display resolution where pixel frequency may be as high as 350 MHz. Intel recommends that each analog R, G, B signal be routed single-endedly. The analog RGB signals should be routed with an impedance of 37.5 Ω. Intel recommends that these routes be routed on an inner routing layer and that it be shielded with VSS planes, if possible. Spacing between DAC channels and to other signals should be maximized; Intel recommends 20-mil spacing. The RGB signals require pi filters that should be placed near the VGA connector. It consists of two 3.3 pF caps with a 75 Ω ferrite bead at 100 MHz between them. The RGB signals should have a 75 Ω, one percent terminating pull-down resistor. The complement signals (R#, G#, and B#) should be grounded to the ground plane.

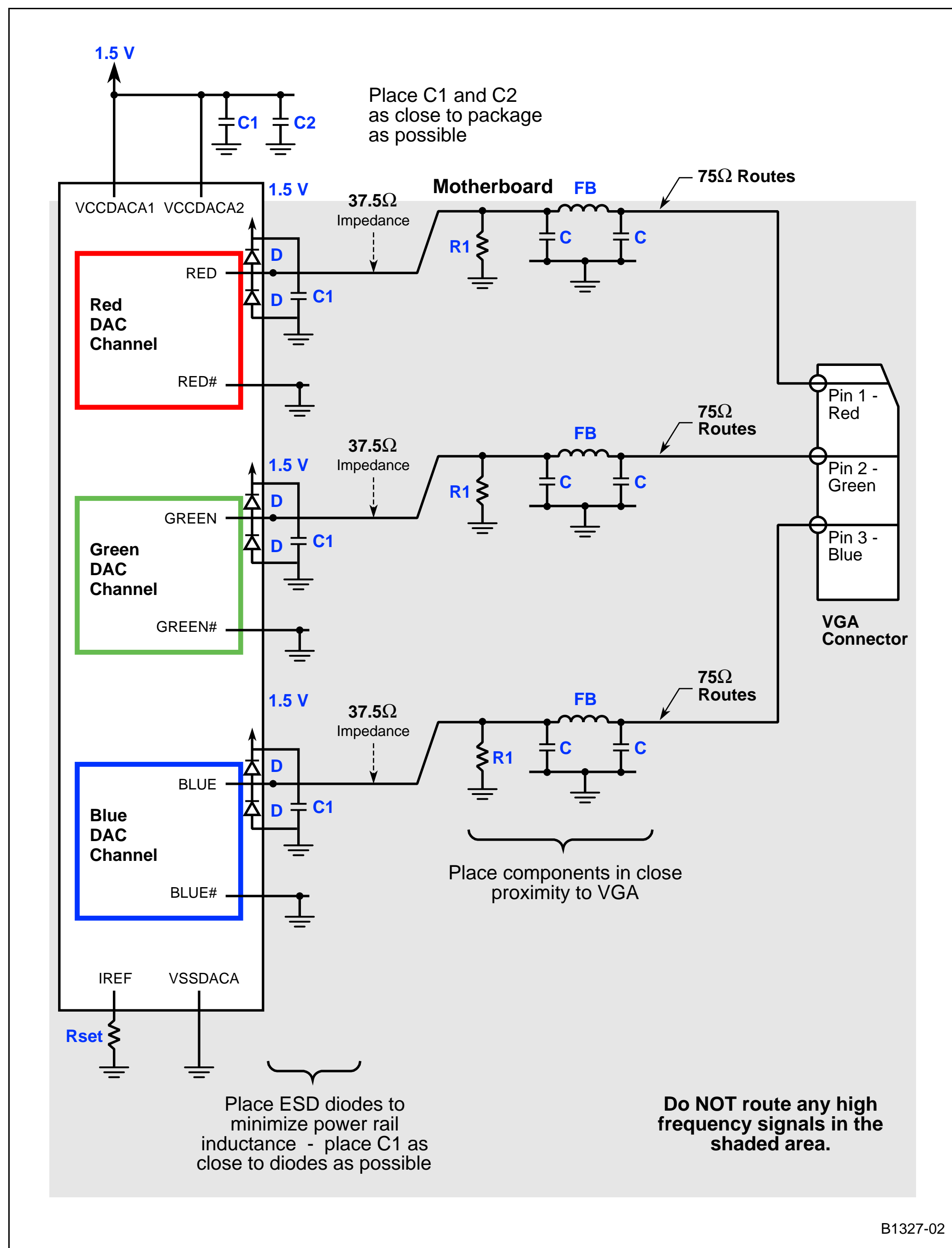
Intel recommends that the pi filter and terminating resistors be placed as close as possible to the VGA connector. After the 75 Ω termination resistor, the RGB signals routing to the pi-filters and the VGA connector *should ideally be routed with 75* Ω *impedance (~ 5 mil traces)*, *or as close to* 75 Ω *impedance as possible.*

The RGB signals also require protection diodes between 1.5 V and ground. These diodes should have low C ratings (~5 pF max) and small leakage current (~ 10 mA at 120° C) and should be properly decoupled with a 0.1 µF cap. These diodes and decoupling should be placed to minimize power rail inductance. The choice between diodes (or diode packs) should comprehend the recommended electrical characteristics in addition to cost.

6.1.4 DAC Routing Guidelines

Figure 47 presents the GMCH DAC routing guidelines.

Figure 47. GMCH DAC Routing Guidelines



The DAC channel (red, green, blue) outputs are routed as single-ended shielded current output routes that are terminated prior to connecting to the video PI-filter and VGA connector. Table 36 presents Intel's recommended GMCH DAC components.

Table 36. Recommended GMCH DAC Components

Recommended DAC Board Components				
Component	**Value**	**Tolerance**	**Power**	**Type**
R1	75 Ω	1 %	1/16 W	SMT, Metal Film
REFSET	137 Ω	1 %	1/16 W	SMT, Metal Film
C1	0.1 µF	20 %	-----	SMT, Ceramic
C2	0.01 µF	20 %	-----	SMT, Ceramic
C	3.3 pF	10 %	-----	SMT, Ceramic
D	PAC DN006	-------	350 mW	California Micro Devices – ESD diodes for VGA SOIC package Or equivalent diode array
FB	75 Ω @ 100 MHz	--------	-------	MuRata* BLM11B750S

Figure 48 illustrates the REFSET placement.

Figure 48. REFSET Resistor Placement

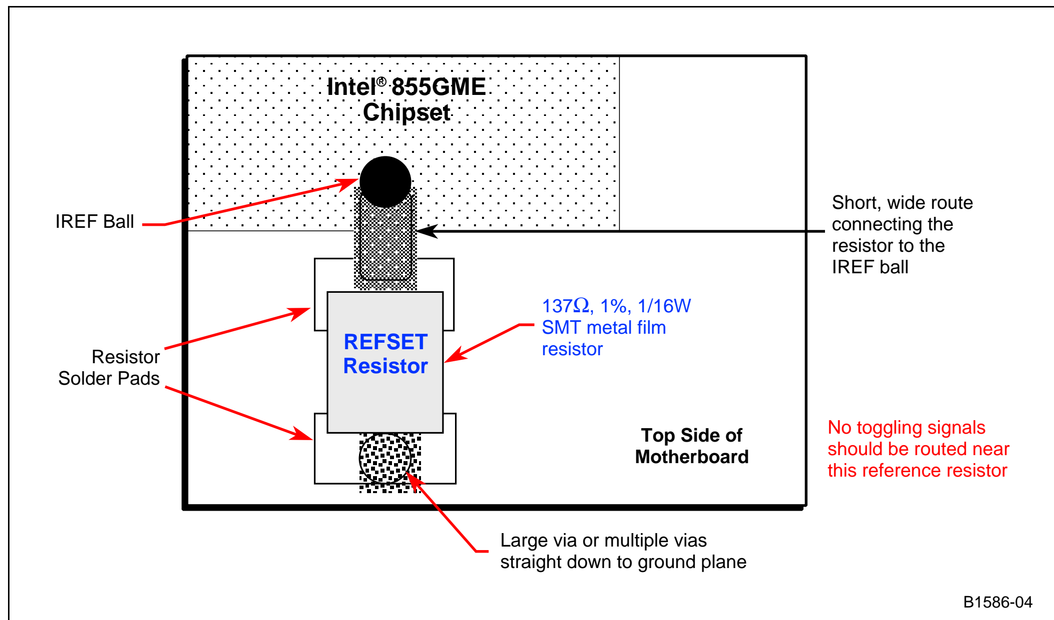
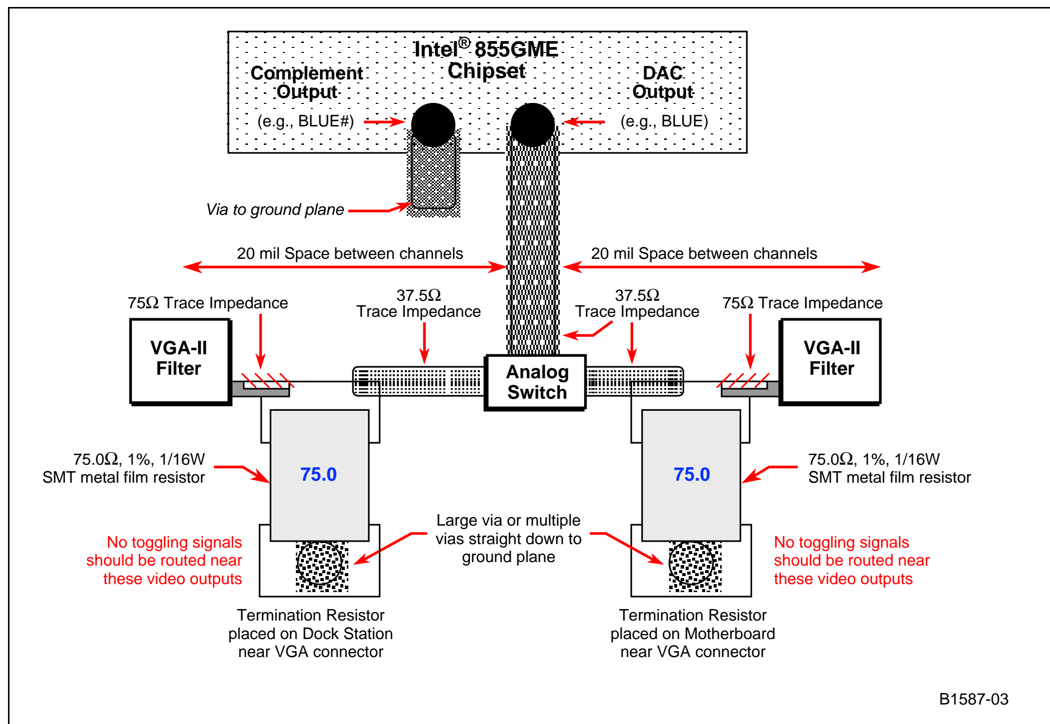


Figure 49 illustrates Intel's recommended routing of the termination resistors.

Figure 49. DAC R, G, B Routing and Resistor Layout Example



6.1.5 DAC Power Requirements

The DAC requires a 1.5 V supply through its two V_{CCADAC} balls. The two may share a set of capacitors, 0.1 µF and 0.01 µF, but this connection should have low inductance. Separate analog power or ground planes are not required for the DAC.

However, because the DAC is an analog circuit, it is particularly sensitive to AC noise seen on its power rail. Designs should provide as clean and quiet a supply as possible to the V_{CCA_DAC}. Additional filtering and/or separate voltage rail may be needed to do so. On the Intel CRB, there is a place holder for a LC filter in case there is noise present in the V_{CCA} power rail.

- Video DAC Power Supply DC Specification: 1.50 V ± 5%
- Video DAC Power Supply AC Specification:
  - ± 0.3% from 0.10 Hz to 10 MHz
  - ± 0.95% from 10 MHz to maximum pixel clock frequency
- Absolute minimum voltage at the V_{CCA} package ball = 1.40 V

6.1.6 HSYNC and VSYNC Design Considerations

HSYNC and VSYNC signals are connected to the analog display attached to the VGA connector. These are 3.3 V outputs from the GMCH. A 39 Ω series resistor is required before routing to the VGA connector. Also, capacitors (28 pF to 33 pF) before and after the series resistor may be needed to meet the VESA rise/fall time specification.

Unidirectional buffers (high impedance buffers) are required on both HYSNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.

6.1.7 DDC and I²C Design Considerations

DDCADATA and DDCACLK are 3.3 volt IO buffers connecting the GMCH to the monitor. If higher signaling voltage (5.5 V) is required by the monitor, level shifting devices may be used. Pull-up resistors of 2.2 kΩ (or of the appropriate value derived from simulation) are required on each of these signals.

6.2 LVDS Transmitter Interface

The Intel® LVDS (Low Voltage Differential Signaling) transmitter serializer converts up to 18 bits of parallel digital RGB data, (6 bits per RGB), along with up to 4 bits for control (SHFCLK, HSYNC, VSYNC, DE) into two 4-channel serial bit streams for output by the LVDS transmitter.

The transmitter is fully differential and utilizes a current mode drive with a high impedance output. The drive current develops a differential swing in the range of 250 mV to 450 mV across a 100 Ω termination load.

The parallel digital data is serially converted to a 7-bit serial bit stream that is transmitted over the 8-channel LVDS interface at 7x the input clock. The differential output clock channel transmits the output clock at the input clock frequency. While the differential output channels transmit the data at the 7x clock rate (1 bit time is 7x the input clock). The 7x serializer synchronizes and regenerates an input clock from 35 MHz to 112 MHz. Typical operation is at 65 MHz (15.4 ns), therefore, at a 7x clock rate, 1bit time would be 2.2 ns. With data cycle times as small as 2.2 ns, propagation delay mismatch is critical, such that intra-channel skew (skew between the inverting and non-inverting output) must be minimized.

The following differential signal groups comprise the LVDS interface. The topology rules for each group are defined in subsequent sections.

Table 37. Signal Group and Signal Pair Names

Channel	Signal Group	Signal Pair Names
Channel A	Clocks	ICLKAM, ICLKAP
	Data Bus	IYAM[3:0], IYAP[3:0]
Channel B	Clocks	ICLKBM, ICLKBP
	Data Bus	IYBM[3:0], IYBP[3:0]

6.2.1 LVDS Length Matching Constraints

The routing guidelines presented in the following subsections define Intel's recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group. These recommendations are provided to achieve optimal SI and timing. In addition to the absolute length limits provided, more restrictive length matching requirements are also provided. The additional requirements further restrict the minimum to maximum length range of each signal group with respect to clock strobe, as required to ensure adequate timing margins.

6.2.1.1 LVDS Package Length Compensation

As mentioned in Section 6.2.1, all length matching is done from GMCH die-pad to LVDS connector pin. The reason for this is to compensate for the package length variation across each signal group to minimize timing variance. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the GMCH requires a length matching process. Refer to Table 39 for the Intel® 855GME chipset LVDS package lengths information.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting package length variance across a signal group. Of course, there is some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

6.2.2 LVDS Routing Guidelines

Each LVDS channel is required to be length matched to within ± 20 mils of the LVDS clock strobe signals. The two complementary signals in each clock strobe pair, as well as in each data pair, are also required to be length matched to within ± 20 mils of each other. See Table 38 for a summary of LVDS signal group routing guidelines.

Table 38. LVDS Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Definition
Signal Group	LVDS
Topology	Differential Pair Point to Point
Reference Plane	Ground Referenced
Differential Mode Impedance (Zdiff)	100 Ω ± 15%
Nominal Trace Width	4 mils
Nominal Pair Spacing (edge to edge)	7 mils
Minimum Pair to Pair Spacing (See exceptions for breakout region below.)	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other LVDS Signals (See exceptions for breakout region below.)	20 mils
Minimum Isolation Spacing to non-LVDS Signals	20 mils

Table 38. LVDS Signal Group Routing Guidelines (Sheet 2 of 2)

Parameter	Definition
Maximum Via Count	2 (per line)
Package Length Range	550 mils ± 150mils (Refer to Table 39 for exact lengths.)
Total Length	Maximum 10 inches
Data to Clock Length Matching	Match all segments to ± 20 mils. (Refer to Section 6.2.1 for more information.)
Clock to Clock# Length Matching (Total Length)	Match clocks to X0 ± 20 mils.
Data to Data# Length Matching (Total Length)	Match data to ± 20 mils.
Breakout Exceptions (Reduced geometries for GMCH breakout region)	Breakout section should be as short as possible. Try to maintain trace width as 4 mils, spacing 7 mils, while the spacing between pairs may be 10-20 mils.

The traces associated with the LVDS Transmitter timing domain signals are differential traces terminated across 100 Ω ± 15 Ω and should be routed as:

- Stripline only.
- Isolate all other signals from the LVDS signals to prevent coupling from other sources onto the LVDS lines.
- Use controlled impedance traces that match the differential impedance of your transmission medium (i.e., cable) and termination resistor.
- Run the differential pair trace lines as close together as possible as soon as they leave the IC, not greater than 10 mils. This helps eliminate reflections and ensure noise is coupled as common mode. Plus, noise induced on the differential lines is much more likely to appear as common mode, which is rejected by the receiver.
- The LVDS transmitter timing domain signals have a maximum trace length of 10 inches. This maximum applies to all of the LVDS transmitter signals.
- Traces must be ground referenced and must not switch layers between the GMCH and connector.

When choosing cables, it is important to remember:

- Use controlled impedance media. The differential impedance of cable LVDS uses should be 100 Ω. Cables should not introduce major impedance discontinuities that cause signal reflection.
- Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable, multi-conductor) for noise reduction and signal quality.
- Cable length must be less than 16 inches.

Table 39 presents the LVDS package lengths.

Table 39. LVDS Package Lengths

Signal Group	GMCH Signal Name	Package Trace Length (mils)	Signal Group	GMCH Signal Name	Package Trace Length (mils)
CHANNEL A	ICLKAP	503.7	CHANNEL B	ICLKAP	502.0
	ICLKAM	498.8		ICLKAM	499.1
	IYAP0	399.6		IYBP0	359.8
	IYAM0	385.4		IYBM0	353.7
	IYAP1	487.5		IYBP1	524.7
	IYAM1	466.2		IYBM1	516.6
	IYAP2	572.6		IYBP2	623.3
	IYAM2	566.2		IYBM2	604.2
	IYAP3	643.2		IYBP3	441.8
	IYAM3	637.8		IYBM3	441.7

6.3 Digital Video Out Port

The GMCH DVO port interface supports a wide variety of third-party DVO compliant devices (e.g., TV encoder, TMDS transmitter or integrated TV encoder, and TMDS transmitter). The GMCH has two dedicated DVO ports, DVOB and DVOC. Intel's DVO port is a 1.5 V interface that may support transactions up to 165 MHz. Some of the DVO port command signals may require a voltage translation circuit depending on the third-party device. Refer to Table 40 for the DVO interface signals.

6.3.1 DVO Interface Signal Groups

Table 40 presents the DVO interface signal groups.

Table 40. DVO Interface Signal Groups

Signal Group	GMCH Signal Name	Signal Type	Signal Group	GMCH Signal Name	Signal Type
DVOB	DVOBFLDSTL	Input	DVOC	DVOCFLDSTL	Input
	DVOBHSYNC	Output		DVOCHSYNC	Output
	DVOBVSYNC	Output		DVOCVSYNC	Output
	DVOBBLANK#	Output		DVOCBLANK#	Output
	DVOBD[11:0]	Output		DVOCD[11:0]	Output
	DVOBCLK (DVOBCLK[0])	Output Strobe		DVOCCLK (DVOCCLK[0])	Output Strobe
	DVOBCLK# (DVOBCLK[1])	Output Strobe		DVOCCLK# (DVOCCLK[1])	Output Strobe
Common Signals for Both DVO Ports	DVOBCCLKINT	Input	Voltage Reference, RCOMP	DVORCOMP	
	DVOBCINTR#	Input		GVREF	
	ADDID[7:0]	Input			
	DVODETECT	Input			

6.3.1.1 DVO/I^{2}C to AGP Pin Mapping

The DVODETECT signal is muxed with the GPAR signal on the AGP bus. This signal will act as a strap to indicate if the interface is in AGP or DVO mode. The GMCH has an internal 8.2-k, pull-down on this signal that will naturally pull it low. If an AGP graphics device is present, the signal will be pulled high at the AGP graphics device and the AGP/DVO mux select bit in the SHIC register will be set to AGP mode.

The SBA[7:0] signals act as straps for an ADDID. These pins are used to communicate to the Video BIOS when an external device is interfaced to the DVO port. If an on-board DVO device is implemented, ADDID[7] should be strapped low. When an AGP graphics device is present, DVODETECT=1 (AGP mode).

Table 41. AGP/DVO Pin Muxing

DVO MODE	AGP MODE	DVO MODE	AGP MODE	DVO MODE	AGP MODE
DVOBD[0]	GAD[3]	DVOCD[0]	GAD[19]	MI2CCLK	GIRDY#
DVOBD[1]	GAD[2]	DVOCD[1]	GAD[20]	MI2CDATA	GDEVSEL#
DVOBD[2]	GAD[5]	DVOCD[2]	GAD[21]	MDVICLK	GTRDY#
DVOBD[3]	GAD[4]	DVOCD[3]	GAD[22]	MDVIDATA	GFRAME#
DVOBD[4]	GAD[7]	DVOCD[4]	GAD[23]	MDDCCDATA	GAD[15]
DVOBD[5]	GAD[6]	DVOCD[5]	GCBE#[3]	MDDCCLK	GSTOP#
DVOBD[6]	GAD[8]	DVOCD[6]	GAD[25]	DVOBCINT#	GAD[30]
DVOBD[7]	GCBE#[0]	DVOCD[7]	GAD[24]	DVOBCCLKINT	GAD[13]
DVOBD[8]	GAD[10]	DVOCD[8]	GAD[27]	ADDID[7]	GSBA[7]
DVOBD[9]	GAD[9]	DVOCD[9]	GAD[26]	ADDID[6]	GSBA[6]
DVOBD[10]	GAD[12]	DVOCD[10]	GAD[29]	ADDID[5]	GSBA[5]
DVOBD[11]	GAD[11]	DVOCD[11]	GAD[28]	ADDID[4]	GSBA[4]
DVOBCLK	GADSTB[0]	DVOCCLK	GADSTB[1]	ADDID[3]	GSBA[3]
DVOBCLK#	GADSTB#[0]	DVOCCLK#	GADSTB#[1]	ADDID[2]	GSBA[2]
DVOBHSYNC	GAD[0]	DVOCHSYNC	GAD[17]	ADDID[1]	GSBA[1]
DVOBVSYNC	GAD[1]	DVOCVSYNC	GAD[16]	ADDID[0]	GSBA[0]
DVOBBLANK#	GCBE#[1]	DVOCBLANK#	GAD[18]	DVODETECT	GPAR
DVOBFLDSTL	GAD[14]	DVOCFLDSTL	GAD[31]	DPMS	GPIPE#

6.3.2 DVOB and DVOC Port Interface Routing Guidelines

For Intel 855GM chipset platforms, guidelines apply for both interfaces.

6.3.2.1 Length Mismatch Requirements

The routing guidelines presented in the following subsections define Intel's recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching requirements are also provided which further restrict the minimum to maximum length range of each signal group with respect to clock strobe, as required to ensure adequate timing margins. Refer to Table 42 for DVO interface trace length matching requirements.

Table 42. DVO Interface Trace Length Mismatch Requirements

Data Group	Signal Matching to Strobe Clock	DVO Clock Strobes Associated With the Group	Clock Strobe Matching	Notes
DVOBD [11:0]	±100 mils	DVOBCLK[1:0]	± 10 mils	1, 2
DVOCD [11:0]	±100 mils	DVOCCLK[1:0]	± 10 mils	1, 2

NOTES:
1. Data signals of the same group should be trace length matched to the clock within ± 100 mil including package lengths.
2. **All length matching formulas are based on GMCH die-pad to DVO device pin total length.** Package length tables are provided for all signals to facilitate this pad-to-pin matching.

6.3.2.2 Package Length Compensation

As mentioned in Section 6.3.2.1, all length matching is done from GMCH die-pad to DVO connector pin. The reason for this is to compensate for the package length variation across each signal group to minimize timing variance. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the GMCH requires a length matching process. Refer to Table 44 for the DVO interface package lengths information.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting out package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

6.3.2.3 DVOB and DVOC Routing Guidelines

Table 43 provides the DVOB and DVOC routing guideline summary.

Table 43. DVOB and DVOC Routing Guideline Summary (Sheet 1 of 2)

Parameter	Definition
Signal Group	DVOBD [11:0], DVCBD [11:0]
Motherboard Topology	Point to point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils
Minimum Spacing to Trace Width Ratio	2:1 (e.g., 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DVO Signals	20 mils
Minimum Spacing to Other DVO Signals	12 mils (See exceptions for breakout region below.)
Minimum Spacing of DVOBCLK [1:0] or DVOCCLK[1:0] to any other signals	12 mils
Package Length Range	Refer to Table 44 for package lengths.

Table 43. DVOB and DVOC Routing Guideline Summary (Sheet 2 of 2)

Parameter	Definition
Total Length	Minimum = 1.5 inches Maximum = 6 inches
Data to Clock Strobe Length Matching Requirements	± 100 mils
CLK0 to CLK1 Length Matching Requirements	± 10 mils

The DVO interface does not require any external termination. They are routed point-to-point as follows:

- All signals should be routed as striplines (inner layers).
- All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines may be met. The trace length and trace spacing requirements ***must*** not be violated by any signal.
- Route the DVOBCLK[1:0] or DVOCCLK[1:0] signal pairs 4 mils wide and 8 mils apart with a max trace length of six inches. This signal pair should be a minimum of 12 mils from any adjacent signals.
- To break out of the 82855GME, the DVOB and/or DVOC data signals may be routed with a trace width of 4 mils and a trace spacing of 7 mils. The signals should be separated to a trace width of 4 mils and a trace spacing of 8 mils within 0.3 inch of the GMCH component.

Table 44. DVO Interface Package Lengths (Sheet 1 of 2)

Signal	Pin Number	Package Length (mils)	Signal	Pin Number	Package Length (mils)
DVOBCLK	P3	475	DVOCCLK	J3	601
DVOBCLK#	P4	439	DVOCCLK#	J2	675
DVOBD[0]	R3	489	DVOCD[0]	K5	489
DVOBD[1]	R5	439	DVOCD[1]	K1	692
DVOBD[2]	R6	343	DVOCD[2]	K3	622
DVOBD[3]	R4	415	DVOCD[3]	K2	685
DVOBD[4]	P6	409	DVOCD[4]	J6	536
DVOBD[5]	P5	387	DVOCD[5]	J5	518
DVOBD[6]	N5	466	DVOCD[6]	H2	720
DVOBD[7]	P2	533	DVOCD[7]	H1	771
DVOBD[8]	N2	568	DVOCD[8]	H3	649
DVOBD[9]	N3	504	DVOCD[9]	H4	625
DVOBD[10]	M1	611	DVOCD[10]	H6	521
DVOBD[11]	M5	510	DVOCD[11]	G3	762
DVOBFLDSTL	M2	566	DVOCFLDSTL	H5	566
DVOBHSYNC	T6	339	DVOCHSYNC	K6	491
DVOBVSYNC	T5	362	DVOCVSYNC	L5	440

Table 44. DVO Interface Package Lengths (Sheet 2 of 2)

Signal	Pin Number	Package Length (mils)	Signal	Pin Number	Package Length (mils)
DVOBBLANK#	L2	583	DVOCBLANK#	L3	541
DVOBCCLKINT	M3	520			
DVOBCINTR#	G2	712			

6.3.3 DVOB and DVOC Assumptions, Definitions, and Specifications

The source synchronous solution space consists of all designs in which the flight time mismatch between a strobe and its associated data is less than the total allowable skew:

$T_{skew} = T_{\mathbf{flight}data} - T_{\mathbf{flight}strobe}$

Where $T_{\mathbf{flight}data}$ and $T_{\mathbf{flight}strobe}$ are the driver-pad-to-receiver-pin flight times of the data and the strobe respectively.

The DVO physical interface is a point-to-point topology using 1.5 V signaling. The DVO uses a 165 MHz clock.

The flight time skew simulations reproduce all parameters that could cause a skew between two signals, including motherboard and add-in card line lengths, effective capacitance in the buffer models, crosstalk on each of the different interconnect combinations, data pattern dependencies, and Inter-Symbol Interference (ISI) induced skews.

6.3.4 DVOB and DVOC Simulation Method

Figure 50 illustrates a DVOB and DVOC simulations model. The DVO component is a third-party chip.

Figure 50. DVOB and DVOC Simulations Model

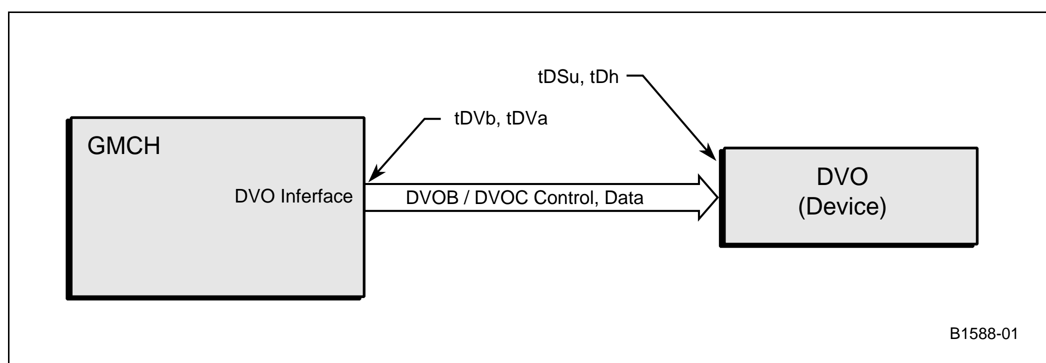
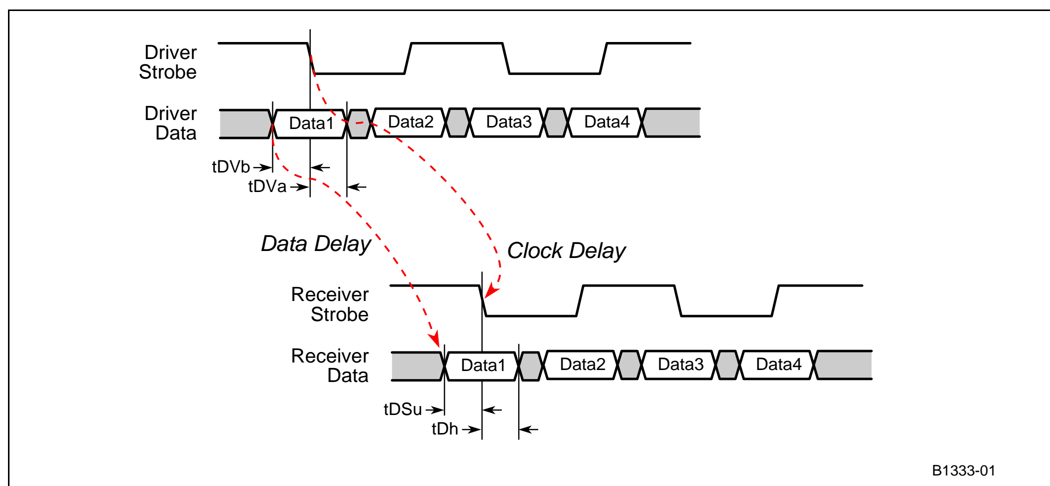


Figure 51 illustrates the driver-receiver waveforms relationship specification.

Figure 51. Driver-Receiver Waveforms Relationship Specification



The setup margin and the hold margin for a particular design depends on the values of the data valid times and the data setup and hold times on both the driver and the receiver sides. However, available margins are not absolute values. Any skew due to routing and loading differences, any coupling differences in the parallel traces, and any effects of Simultaneous Switching Output (such as ISI, ground bounce, etc.) should be accounted for in the timing budget as they reduce the total available margin for the design.

Table 45 presents the allowable interconnect skew calculations.

Table 45. Allowable Interconnect Skew Calculation

Component	Skew Element	Symbol	Setup	Hold	Units
Driver	Data Valid before Strobe	tDVb	570		ps
	Data Valid after Strobe	tDVa		770	ps
Interconnect	Allowable Skew		Vendor specific	Vendor specific	ps
Receiver	Data Setup to Strobe	tDSu	Vendor specific		ps
	Data Hold from Strobe	tDh		Vendor specific	ps

All numbers in this table are from the 82855GME specification documents that are applicable for this interface. For third-party receiver devices, refer to appropriate third-party vendor specifications.

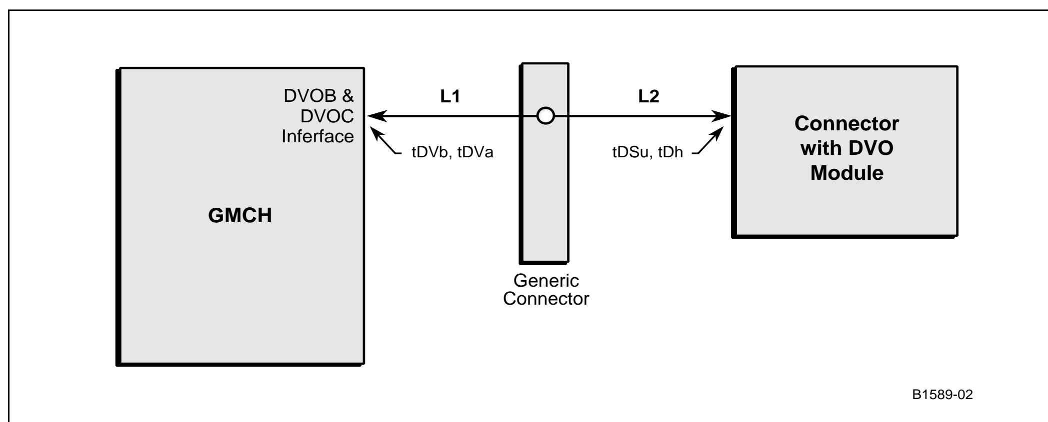
6.4 DVOB and DVOC Port Flexible (Modular) Design

The GMCH supports flexible design interfaces described in this section.

6.4.1 DVOB and DVOC Module Design

The 82855GME supports a DVO module design connected to the GMCH through a generic connector. Simulation method is the same as in Section 6.3.4. Lengths L1 and L2 are determined by simulation as L1 = four inches and L2 = two inches. Refer to Figure 53 for the generic connector parasitic model.

Figure 52. DVO Enabled Simulation Model



All signals should be routed as striplines (inner layers). All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to ± 100 mils with respect to the strobe clocks as possible to provide optimal timing margin. Each strobe pair must be separated from other signals by at least 12 mils.

Table 46 presents the DVO enabled routing guideline summary.

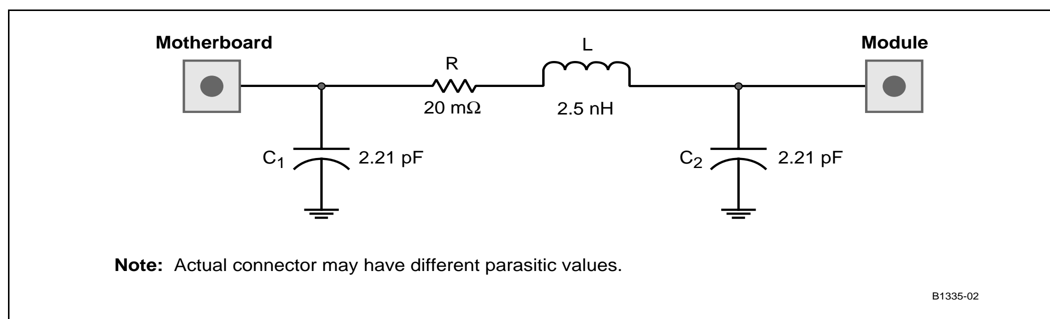
Table 46. DVO Enabled Routing Guideline Summary

Signal	Maximum Length	Trace Width	Trace Spacing	Length Mismatch	Notes
DVO Timing Domain	L1=4 in L2=2 in	4 mils	8 mils	± 100 mils	

6.4.1.1 Generic Connector Model

Figure 53 illustrates the generic connector model used in simulation for flexible DVO implementation. This is only for reference. The actual connector may have different parasitic values. Designs using this approach need to be simulated first.

Figure 53. Generic Module Connector Parasitic Model



6.5 DVO GMBUS and DDC Interface Considerations

The GMCH DVOB and/or DVOC port controls the video front-end devices via the GMBUS (I^2C) interface. DDCADATA and DDCACLK should be connected to the CRT connector. The GMBUS should be connected to the DVO device, as required by the specifications for those devices. The protocol and bus may be used to configure registers in the TV encoder, TMDS transmitter, or any other external DVI device. The GMCH also has an option to utilize the DDCPCLK and DDCPDATA to collect EDID (Extended Display Identification) from a digital display panel.

Pull-ups (or pull-ups with the appropriate value derived from simulating the signal) typically ranging from 2.2 kΩ to 10 kΩ are required on each of these signals.

The GMCH signal groups in Table 47 list the six possible GMBUS pairs.

Table 47. GMBUS Pair Mapping and Options

Pair #	Signal Name	Buffer Type	Description	Notes
0	DDCADATA	3.3 V	DDC for Analog monitor (CRT) connection	This cannot be shared with other DDC or I2C pairs due to legacy monitor issues.
	DDCACLK			
1	LCLKCTRLA	3.3 V	For control of SSC clock generator devices down on motherboard	If SSC is not supported, then may be used for DVOB or DVOC GMBUS.
	LCLKCTRLB			
2	DDCPDATA	3.3 V	DDC for Digital Display connection via the integrated LVDS display port for support for EDID panel*	If EDID panels are not supported, may optionally use as GMBUS for DVOB or DVOC.
	DDCPCLK			
3	MDVIDATA	1.5 V	GMBUS control of DVI devices (TMDS or TV encoder)	May optionally use as GMBUS for DVOB or DVOC.
	MDVICLK			
4	MI2CDATA	1.5 V	GMBUS control of DVI devices (TMDS or TV encoder)	May optionally use as GMBUS for DVOB or DVOC.
	MI2CCLK			
5	MDDCDATA	1.5 V	DDC for Digital Display connection via TMDS device	May optionally use as GMBUS for DVOB or DVOC.
	MDDCCLK			

NOTE: MDDC pair is not available for use with the Extreme Graphics Driver.
NOTE: All GMBUS pairs may be optionally programmed to support any interface and is programmed through the BMP utility.

If any of GMBUS pairs are not used, 2.2 k-100 kΩ pull-up (or pull-ups with the appropriate value derived from simulating the signal) resistors are required, except for CRT DDCADATA/DDCCLK and LCLKCTRLA/LCLKCTRLB GMBUS pair. LCLKCTRLA/LCLKCTRLB are used as bootup straps. Refer to the *Intel® 855GM Chipset GMCH Datasheet* for details on strapping options. This will prevent the GMCH from confusing noise on these lines for false cycles.

6.5.1 Leaving the GMCH DVOB or DVOC Port Unconnected

When the motherboard does not implement any of the possible video devices with the DVO port, follow the guidelines recommended on the motherboard. DVO Output signals may be left unconnected if they are not used.

Pull-down resistors are required for the following signals if not used:

- DVOBFLDSTL
- DVOCFLDSTL
- DVOBCCLKINT

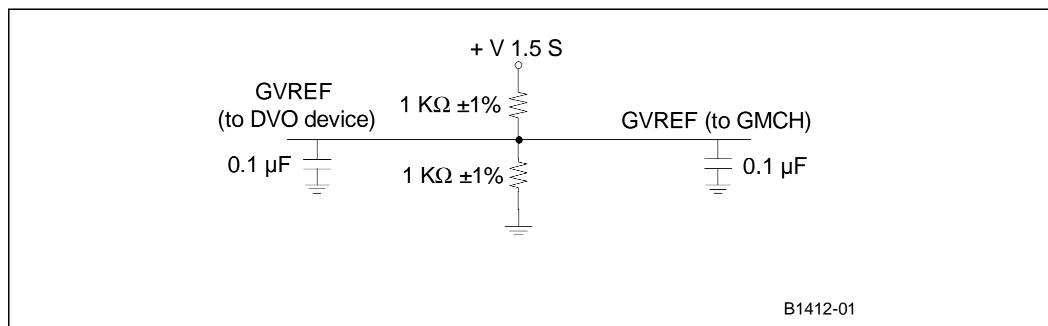
Pull-up resistors are required for the following signals if not used:

- DVOBCINTR#

6.6 Miscellaneous Input Signals and Voltage Reference

- ADDID[7]: Pull-down to ground with a 1 KΩ resistor when using the DVOB or DVOC port. This is a vBIOS strapping option to load the TPV AIM module for DVOB and DVOC port. Pull-down not required if DVOB or DVOC is not enabled.
- ADDID[6:0]: Leave unconnected (NC).
- DVODETECT: Leave unconnected (NC) when using the DVOB or DOVC port.
- DVORCOMP is used to calibrate the DVOB buffers. It should be connected to ground via a 40.2 Ω 1% resistor using a routing guideline of 10 mil trace and 20 mil spacing.
- DPMS: connects to 1.5 V version of the Intel® 82801DB I/O Controller Hub (ICH4) SUSCLK or a clock that runs during S1.
- GVREF: Reference voltage for the DVOB and DVOC input buffers. Figure 54 illustrates the GVREF reference voltage information.

Figure 54. GVREF Reference Voltage



AGP Port Design Guidelines 7

For detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms), refer to the latest AGP Interface Specification, Revision 2.0, which can be found at http://www.agpforum.org.

7.1 AGP Interface

The 855GME AGP buffers operate in only one mode: 1.5-V drive, not 3.3-V safe. This mode is compliant with the AGP 2.0 Specification.

AGP 4X, 2X and 1X must operate at 1.5 V. The AGP interface supports up to 4X AGP signaling. AGP semantic cycles to DRAM are not snooped on the host bus.

The GMCH supports PIPE# or SBA [7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA [7:0] mechanism must be selected during system initialization.

The AGP interface is clocked from a 66-MHz clock. The AGP interface is asynchronous to the host bus, system memory, and internal graphics device. When AGP interface has been enabled, the internal graphics will be disabled using GMCH strapping option. The AGP interface is synchronous to the hub interface with a clock ratio of 1:1 (66 MHz: 66 MHz).

The GMCH multiplexes the AGP signal interface with two DVO ports. These DVO ports are capable of supporting a variety of digital display devices such as TMDS transmitters and TV-Out encoders. It is possible to use the DVO ports in dual-channel mode to support higher resolutions and refresh rates (single channel mode is limited to a 165-MHz pixel clock rate).

7.1.1 AGP 2.0

The AGP Interface Specification, Revision 2.0, enhances the functionality of the original AGP Interface Specification, Revision 1.0, by allowing 4X data transfers (i.e., four data samples per clock), and 1.5-volt operation. The 4X operation of the AGP interface provides for "quad-pumping" of the AGP AD (address/data) and SBA (side-band addressing) buses. That is, data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is ¼ of a 15-ns (66-MHz) clock or 3.75 ns. It is important to understand that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, data is sampled twice during a 66-MHz clock cycle.

Therefore, the data cycle time is 7.5 ns. To allow for these high-speed data transfers, the 2X mode of AGP operation uses source-synchronous data strobing. During 4X operation, the AGP interface uses differential source-synchronous strobing.

With data cycle times as small as 3.75 ns and setup/hold times of one ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be long. If the mismatch between a data line and the associated strobe is too great, or if there is noise on the interface, incorrect data will be sampled. The low-voltage operation on AGP (1.5 V) requires even more noise immunity.

7.1.2 AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: 1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals. Each group has different routing requirements.

In addition, within the 2X/4X timing domain signals, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements, as well as trace width and spacing requirements. Because of the multiplexed AGP/DVO interface, there are trace length matching requirements within each set of 2X/4X signals, as well as between sets of 2X/4X signals. The signal groups are listed in following table.

Table 48. AGP 2.0 Signal Groups

1x Signals	2x Signals	4x Signals
CLK (3.3 V) GRBF# GWBF# GST_[2:0] GPIPE# GREQ# GGNT# GPAR GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL# GAD_[31:0] GC/BE_[3:0]# GADSTB_[1:0]	2X signals include all 1X signals and: GADSTB_[1:0] GSBSTB GAD_[31:0] signals and associated GC/BE_[3:0]# signals are running at 2X mode.	4X signals include all 1X signals and: GADSTB_[1:0] GADSTB_[1:0]# GSBSTB GSBSTB# GAD_[31:0] signals and associated GC/BE_[3:0]# signals are running at 4X mode.

Table 49. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobes in 2X	Associated Strobes in 4X
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

The routing guidelines for each group of signals (1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals) will be addressed separately.

7.2 AGP Routing Guidelines

7.2.1 1x Timing Domain Routing Guidelines

7.2.1.1 Trace Length Requirements for AGP 1X

This section contains information on the 1X timing domain routing guidelines. The AGP 1X timing domain signals (see Table 50) have a maximum trace length of 10 inches. The target impedance is 55 Ω± 15%. This maximum applies to ALL of the signals listed as 1X timing domain signals in Table 46. In addition to the maximum trace length requirement, these signals must meet the trace spacing and trace length mismatch requirements in Section 7.2.1.2 and Section 7.2.1.3.

Table 50. Layout Routing Guidelines for AGP 1X Signals

1X signals	Max. Length (inches)	Width (mils)	Space (mils)
CLK_AGP_SLT	10	4	4
AGP_PIPE#	10	4	4
AGP_RBF#	10	4	4
AGP_WBF#	10	4	4
AGP_ST[2:0]	10	4	4
AGP_FRAME#	10	4	4
AGP_IRDY#	10	4	4
AGP_TRDY#	10	4	4
AGP_STOP#	10	4	4
AGP_DEVSEL#	10	4	4
AGP_REQ#	10	4	4
AGP_GNT#	10	4	4
AGP_PAR	10	4	4

7.2.1.2 Trace Spacing Requirements

AGP 1X timing domain signals (see Table 50) can be routed with 4-mil minimum trace separation.

7.2.1.3 Trace Length Mismatch

There are no trace length mismatch requirements for 1X timing domain signals. These signals must meet minimum and maximum trace length requirements.

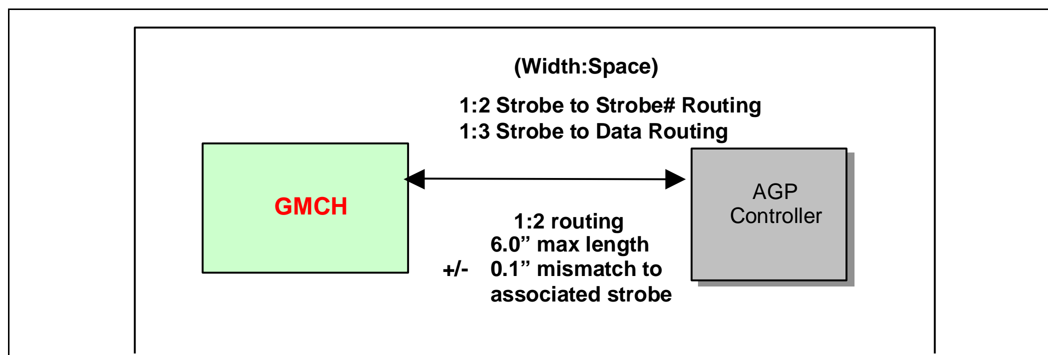
7.2.2 2x/4x Timing Domain Routing Guidelines

7.2.2.1 Trace Length Requirements for AGP 2X/4X

These trace length guidelines apply to ALL of the signals listed as 2x/4x timing domain signals in Table 51. In addition to these maximum trace length requirements, these signals must meet the trace spacing and trace length mismatch requirements in Section 7.2.1.2 and Section 7.2.1.3.

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. These routing rules are divided by trace spacing. In 1:2 spacing, the distance between the traces is two times the width of traces.

Figure 55. AGP Layout Guidelines



For 2X/4X lines in AGP interface, the max length is 6.0 inches (pin to pin) and 1:2 trace spacing is required. 2X signals must be matched to their associated strobe within 0.1 inch. 4X signals must be matched to both of their associated strobes within 0.1 inch. Reduce line length mismatch to ensure added margin.

7.2.2.2 Trace Spacing Requirements

AGP 2X/4X timing domain signals must be routed as documented in Table 48. They should be routed using 4-mil traces. Additionally, the signals can be routed with 5-mil spacing when breaking out of the GMCH. The routing must widen to the requirement in Table 50 within 0.3 inches of the GMCH package.

Since the strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source synchronous AGP interface, special care should be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g. AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 4-mil traces with 8 mils of space (1:2) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 15 mils (1:3). The strobe pair must be length matched to less than ± 0.1 inches (that is, a strobe and its compliment must be the same length within ± 0.1 inches).

Table 51. Layout Guidelines for AGP 2x/4x Signals

Signal	Maximum Length (inches)	Trace Space (mils) (4 mil traces)	Length Mismatch (inches)	Relative To	Notes
2X/4X Timing Domain Set#1	6	8	± 0.1	AGP_ADSTB0 and AGP_ADSTB0#	AGP_ADSTB0, AGP_ADSTB0# must be the same length (±10 mils)
2X/4X Timing Domain Set#2	6	8	± 0.1	AGP_ADSTB1 and AGP_ADSTB1#	AGP_ADSTB1, AGP_ADSTB1# must be the same length (±10 mils)
2X/4X Timing Domain Set#3	6	8	± 0.1	AGP_SBSTB and AGP_SBSTB #	AGP_SBSTB, AGP_SBSTB# must be the same length (±10 mils)

7.2.2.3 Trace Length Mismatch Requirements

Table 52. AGP 2.0 Data Lengths Relative to Strobe Length

Max Trace Length	Trace Spacing	Strobe Length	Min Trace Length	Max Trace Length
< 6 in	1:2	X	X - 0.1 in	X + 0.1 in

The trace length minimum and maximum (relative to strobe length) should be applied to each set of 2X/4X timing domain signals independently. If AD_STB0 is 5 inches and ADSTB0# is 5.01 inches, then AD[15:0] and C/BE[1:0] must be between 4.91 inches and 5.1 inches. However, AD_STB1 and ADSTB1# can be 3.5 inches and 3.51 inches (and therefore AD[31:16] and C/BE#[3:2] must be between 3.41 inches and 3.6 inches). In addition, all 2X/4X timing domain signals must meet the maximum trace length requirements.

- All signals should be routed as strip lines (inner layers).
- All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements must not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to 0 inches as possible to provide optimal timing margin.

The strobe pair must be length matched to less than ± 0.01 inches (that is, a strobe and its compliment must be the same length within ± 0.01 inches).

Table 53 shows the AGP 2.0 routing summary.

Table 53. AGP 2.0 Routing Guideline Summary

Signal	Maximum Length	Trace Spacing (4 mil traces)	Length Mismatch	Relative To	Notes
1X Timing Domain	10 in	4 mils	No Requirement	N/A	None
2X/4X Timing Domain Set#1	6 in	8 mils	± 0.1 in	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	6 in	8 mils	± 0.1 in	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	6 in	8 mils	± 0.1 in	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length

7.2.3 AGP Clock Skew

The maximum total AGP clock skew between the GMCH and the graphics component is 1 ns for all data transfer modes. This 1 ns includes skew and jitter, which originates on the motherboard, add-in module (if used), and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but also at all points on the clock edge that falls in the switching range. The 1 ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew (the motherboard designer shall determine how the 0.9 ns is allocated between the board and the synthesizer).

7.2.4 AGP Signal Noise Decoupling Guidelines

The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the Intel chipset GMCH. The following guidelines are not intended to replace thorough system validation on Intel chipset-based products.

- A minimum of six 0.01-µF capacitors are required and must be as close as possible to the GMCH. These should be placed within 70 mils of the outer row of balls on the GMCH for VDDQ decoupling. Ideally, this should be as close as possible.
- The designer should evenly distribute placement of decoupling capacitors in the AGP interface signal field.
- Intel recommends that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.
- To add the decoupling capacitors within 70 mils of the GMCH and/or close to the vias, trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1.0 inch max.).

In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. One extra 0.01 uF capacitor per 10 vias is required. The capacitor should be placed as close as possible to the center of the via field.

7.2.5 AGP Interface Package Lengths

Table 54. AGP Interface Package Lengths (Sheet 1 of 2)

Signal	Pin Number	Package Length (mils)
GAD0	T6	339
GAD1	T5	362
GAD2	R5	440
GAD3	R3	489
GAD4	R4	415
GAD5	R6	343
GAD6	P5	387
GAD7	P6	409
GAD8	N5	466
GAD9	N3	504
GAD10	N2	568
GAD11	M5	510
GAD12	M1	611
GAD13	M3	520
GAD14	M2	566
GAD15	T7	296
GAD16	L5	440
GAD17	K6	491

Signal	Pin Number	Package Length (mils)
GADSTB_0	P3	475
GADSTBB_0	P4	439
GADSTB_1	J3	601
GADSTBB_1	J2	675
GSBA_0	E5	686
GSBA_1	F5	617
GSBA_2	E3	738
GSBA_3	E2	865
GSBA_4	G5	668
GSBA_5	F4	688
GSBA_6	G6	518
GSBA_7	F6	613
GSBSTB	F2	799
GSBSTBB	F3	761
GPIPEB	D5	644
GCBEB_0	P2	553
GCBEB_1	L2	583
GCBEB_2	L4	515

Table 54. AGP Interface Package Lengths (Sheet 2 of 2)

Signal	Pin Number	Package Length (mils)
GAD18	L3	541
GAD19	K5	489
GAD20	K1	692
GAD21	K3	622
GAD22	K2	685
GAD23	J6	536
GAD24	H1	772
GAD25	H2	720
GAD26	H4	625
GAD27	H3	649
GAD28	G3	762
GAD29	H6	521
GAD30	G2	712
GAD31	H5	566

Signal	Pin Number	Package Length (mils)
GCBEB_3	J5	518
GST_0	C4	750
GST_1	C3	797
GST_2	C2	856
GRBFB	D3	962
GWBFB	D2	947
GFRAMEB	M6	486
GIRDYB	K7	751
GTRDYB	N7	350
GSTOPB	P7	423
GDEVSELB	N6	399
GREQB	B3	762
GGNTB	B2	849
GPAR	L7	623

7.2.6 AGP Routing Ground Reference

Intel strongly recommends that at least the following critical signals be referenced to ground from the GMCH to an AGP controller connector using a minimum number of vias on each net:

- AD_STB0
- AD_STB0#
- AD_STB1
- AD_STB1#
- SB_STB
- SB_STB#
- G_TRDY#
- G_IRDY#
- G_GNT#
- ST[2:0]

7.2.7 Pull-Ups

The AGP 2.0 Specification requires AGP control signals to have pull-up resistors to VDDQ to ensure they contain stable values when no agent is actively driving the bus. Also, the AD_STB[1:0]# and ST_STB# strobes require pull-down resistors to GND. The Intel 855GME chipset GMCH has integrated many of these pull-up/pull-down resistors on the AGP interface and a few other signals not required by the AGP 2.0 Specification. Pull-ups are allowed on any signal except AD_STB[1:0]# and SB_STB#.

The Intel chipset GMCH has no support for the PERR# and SERR# pins of an AGP graphics controller that supports PERR# and SERR#. Pull-ups to a 1.5-V source are required down on the motherboard in such cases.

Table 55. AGP Pull-Up/Pull-Down Requirements and Straps

Signal	AGP 2.0 Signal Pull-Up/ Pull-Down Requirements	GMCH Integrated Pull-Up/ Pull-Down	Notes
DEVSEL#		Pull-Up	
FRAME#		Pull-Up	
GNT#		Pull-Up	
INTA#	Pull-Up		3, 5
INTB#	Pull-Up		3, 5
IRDY#		Pull-Up	
PERR#	Pull-Up		2
PIPE#		Pull-Up	
RBF#		Pull-Up	
REQ#		Pull-Up	1
SERR#	Pull-Up		2
ST[2:0]		Pull-Down	4
STOP#	Pull-Up	Pull-Up	
TRDY#		Pull-Up	
WBF#		Pull-Up	
AD_STB[1:0]		Pull-Up	
AD_STB[1:0]#		Pull-Down	
SB_STB		Pull-Up	
SB_STB#		Pull-Down	
SBA[7:0]		Pull-Up	1

NOTES:
1. The Intel chipset GMCH has integrated pull-ups to ensure that these signals do not float when there is no add-in card in the connector.
2. The Intel chipset GMCH does not implement the PERR# and SERR# signals. Pull-ups on the motherboard are required for AGP graphics controllers that implement these signals.
3. The Intel chipset GMCH does not implement interrupt signals. AGP graphics controller's INTA# and INTB# signals must but routed to the system PCI interrupt request handler where the pull-up requirement should be met as well. For 855GME/ICH4 chipset-based systems, they can be routed to the ICH4's PIRQ signals that are open drain and require pull-ups on the motherboard.
4. ST[1:0] provide the strapping options for 100-MHz PSB operation and DDR memory, respectively.
5. INTA# and INTB# should be pulled to 3.3 V, not VDDQ.
6. The pull-up/pull-down resistor value requirements are shown in Table 52.

Table 56. AGP 2.0 Pull-up Resistor Values

Rmin	Rmax
4 kΩ	16 kΩ

The recommended AGP pull-up/pull-down resistor value is 8.2 kΩ.

7.2.8 AGP VDDQ and VCC

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller and VDDQ is the interface voltage.

7.2.9 VREF Generation for AGP 2.0 (2X and 4X)

7.2.9.1 1.5 V AGP Interface (2X/4X)

The voltage divider networks consist of AC and DC elements. The reference voltage that should be supplied to the Vref pins of the GMCH and the graphics controller is ½ * VDDQ. Two 1 kΩ ± 1% resistors can be used to divide VDDQ down to the necessary voltage level.

The Vref divider network should be placed as close to the AGP interface as is practical to get the benefit of the common mode power supply effects. However, the trace spacing around the Vref signals must be a minimum of 25 mils to reduce crosstalk and maintain signal integrity.

7.2.10 AGP Compensation

The 855GME chipset GMCH AGP interface supports resistive buffer compensation. For PCBs with characteristic impedance of 55 Ω, tie the GRCOMP pin to a 40.2 Ω ± 1% pull-down resistor (to ground) via a 10-mil wide, very short (≈ 0.5 inches) trace.

AGP Link:

http://www.intel.com/technology/agp/info.htm

AGP StressTool Link:

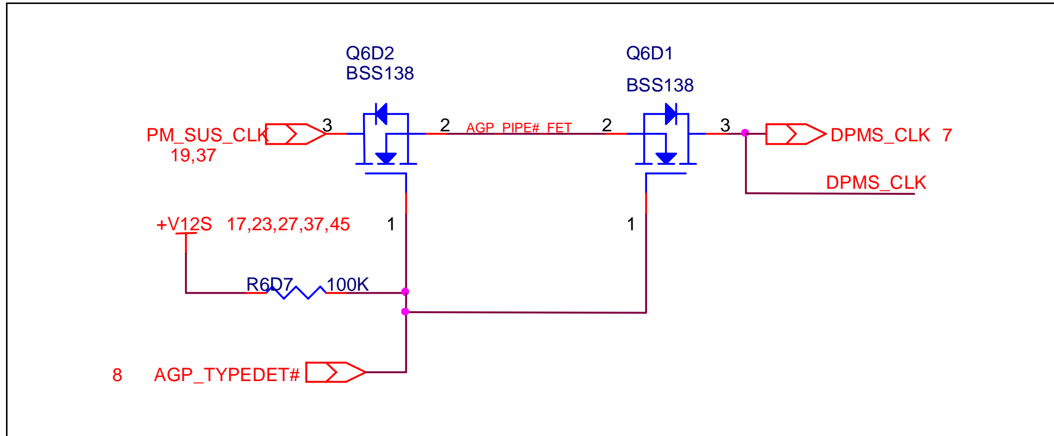
http://www.intel.com/technology/agp/downloads/agp_stress.htm

7.2.11 PM_SUS_CLK/AGP_PIPE# Design Consideration

The following design consideration provides the option to support both AGP and DVO devices with one ADD Connector. Refer to Figure 56 and customer reference schematics for more detail.

The GMCH expects either the PM_SUS_CLK signal from the ADD connector when there is a no AGP device or the AGP_PIPE# signal when there is an AGP device. The AGP_TYPEDET# signal is driven high when no AGP card is detected, allowing DPMS_CLK to be driven by PM_SUS_CLK. In the case where an AGP card is detected, AGP_TYPE# signal goes high which allows DMPS_CLK to be driven by AGP_PIPE#.

Figure 56. DPMS Circuit

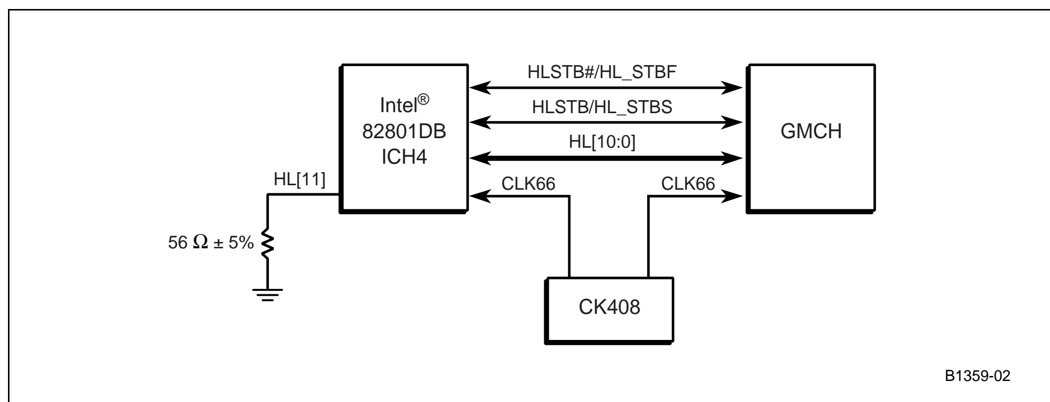


Hub Interface 8

The GMCH and Intel® 82801DB I/O Controller Hub 4 (ICH4) pin-map assignments have been optimized to simplify the Hub Interface routing between these devices. Intel recommends that the Hub Interface signals be routed directly from the GMCH to the ICH4 with all signals referenced to ground. Layer transitions should be minimized. When a layer change is required, use only two vias per net and keep all data signals and associated strobe signals on the same layer.

The Hub Interface signals are broken into two groups: data signals (HL) and strobe signals (HLSTB). For the 11-bit Hub Interface, HL[10:0] are associated with the data signals while HLSTB and HLSTB# are associated with the strobe signals. Figure 57 illustrates the Hub Interface routing example.

Figure 57. Hub Interface Routing Example



8.1 Hub Interface Compensation

This section documents the routing guidelines for the 11-bit Hub Interface using enhanced (parallel) termination. This Hub Interface connects the ICH4 to the Intel® 855GME chipset Graphics Memory Controller Hub (82855GME). The ICH4 should strap its HLRCOMP pin to V_{CCHI} = 1.5 V, as summarized in Table 57. The GMCH should strap its HLRCOMP pin to V_{CCHL} =1.35 V, as summarized in Table 57. The trace impedance must equal 55 Ω ± 15%.

Table 57. Hub Interface RCOMP Resistor Values

Component	Trace Impedance	HLRCOMP Resistor Value	HLRCOMP Resistor Tied to
Intel® 82801DB ICH4	55 Ω ± 15%	48.7 Ω ± 1%	V_{CC}1_5
GMCH	55 Ω ± 15%	37.4 Ω ± 1%	V_{CC}1_35

8.2 Hub Interface Data HL[10:0] and Strobe Signals

The Hub Interface HL[10:0] data signals should be routed on the same layer as Hub Interface Strobe signals.

8.2.1 HL[10:0] and Strobe Signals Internal Layer Routing

Traces should be routed four mils wide with eight mils trace spacing (4 on 8) and 20 mils spacing from other signals. To break out of the GMCH and ICH4 packages, the HL[10:0] signals may be routed four on seven. The signal must be separated to four on eight within 300 mils from the package. The minimum HL[10:0] on board signal trace length is 1.5 inches, while the maximum is six inches. The HL[10:0] signals must be matched within ± 100 mils of the HLSTB differential pair. There is no explicit matching requirement between the individual HL[10:0] signals. The hub interface strobe signals HLSTB and HLSTB# should be routed as a differential pair, four mils wide with eight mils trace spacing (4 on 8). The maximum length for strobe signals is six inches. Each strobe signal must be the same length and each HL[10:0] signal must be matched to within ± 100 mils of the strobe signals. All length matching should be done from GMCH die to the ICH4 die. Refer to package lengths in Table 59 and Table 60.

Table 58. Hub Interface Signals Internal Layer Routing Summary

Signal	Min. length (inches)	Max. length (inches)	Width (mils)	Space (mils)	Mismatch length (mils)	Relative To	Space with other signals (mils)	Notes
HL[10:0]	1.5	6	4	8	± 100	Differential HLSTB pair	20	
HLSTB and HLSTB#	1.5	6	4	8	± 100	Data lines	20	HLSTB and HLSTB# must be the same length (±10 mils)

Table 59. Hub Interface Package Lengths for Intel 82801DB I/O Controller Hub 4 (ICH4) (Sheet 1 of 2)

Signal	Pin Number	Package Length (mils) A-Stepping	Package Length (mils) B-Stepping
HUB_PD0	L19	551	584
HUB_PD1	L20	562	596
HUB_PD2	M19	552	588
HUB_PD3	M21	567	602
HUB_PD4	P19	599	645
HUB_PD5	R19	627	669
HUB_PD6	T20	623	674
HUB_PD7	R20	593	622
HUB_PD8	P23	668	702
HUB_PD9	L22	559	593
HUB_PD10	N22	682	729

Table 59. Hub Interface Package Lengths for Intel 82801DB I/O Controller Hub 4 (ICH4) (Sheet 2 of 2)

Signal	Pin Number	Package Length (mils) A-Stepping	Package Length (mils) B-Stepping
HUB_PD11	K21	560	593
HUB_CLK	T21	605	643
HUB_PSTRB	P21	541	604
HUB_PSTRB#	N20	565	612

Table 60. Hub Interface Package Lengths for the Intel® 855GME Chipset

Signal	Pin Number	Package Length (mils)
HL[0]	U7	281
HL[1]	U4	408
HL[2]	U3	476
HL[3]	V3	484
HL[4]	W2	551
HL[5]	W6	355
HL[6]	V6	328
HL[7]	W7	343
HL[8]	T3	499
HL[9]	V5	399
HL[10]	V4	457
GCLKIN	Y3	539
HLSTB	W3	504
HLSTB#	V2	548

8.2.2 Terminating HL[11]

The HL[11] signal exists on the ICH4 but not the GMCH and is not used on the platform. HL[11] must be pulled down to ground via a 56 Ω resistor.

8.3 Hub VREF/VSWING Generation/Distribution

The Hub Interface reference voltage (V_{REF}) is used on both the GMCH (HLVREF) and the ICH4 (HIREF). The Hub interface also has a reference voltage (VSWING) for the GMCH (PSWING) and the ICH4 (VSWING), to control voltage swing and impedance strength of the Hub Interface buffers. The V_{REF} voltage requirements must be set appropriately for proper operation. Section 8.3.1 to Section 8.3.4 provides details on the different options for V_{REF} and V_{SWING} voltage divider circuitry requirements. Table 61 presents the V_{REF} and V_{SWING} voltage specifications.

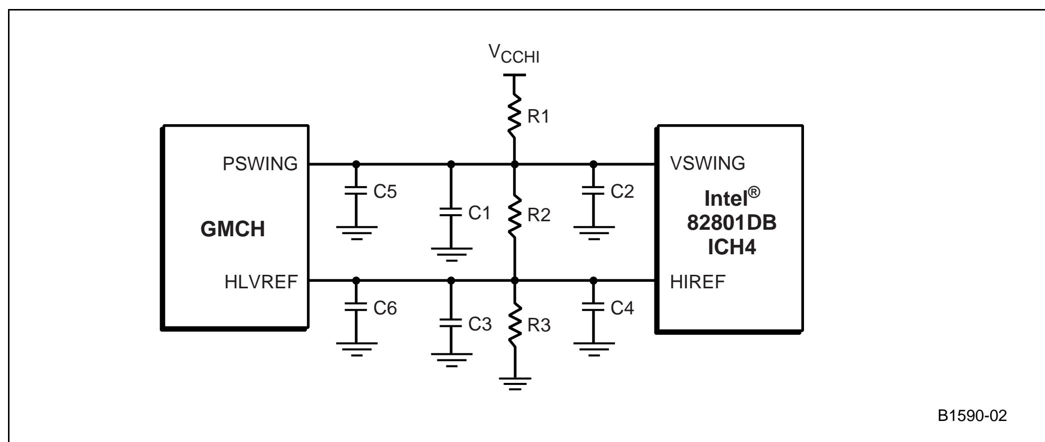
Table 61. Hub Interface V_{REF}/V_{SWING} Generation Circuit Specifications

V_{REF}	V_{SWING}	Notes
HIREF (ICH4) HLVREF (GMCH)	VSWING (ICH4) PSWING (GMCH)	
350 mV ± 8%	800 mV ± 8%	Refer to Section 8.3.1, Section 8.3.2 and Section 8.3.4 for recommendations for the V_{REF}/V_{SWING} voltage generation circuitry. Refer to Table 62, Table 64 for Intel's recommended resistor values.

8.3.1 Single Generation Reference Voltage Divider Circuit

The GMCH and ICH4 may share the same single voltage divider circuit. This option provides one voltage divider circuit to generate both V_{REF} and V_{SWING} reference voltage. The reference voltage for both V_{REF} and V_{SWING} must meet the voltage specification in Table 61. When the voltage specifications are not met, an individual locally generated voltage divider circuit is required. The maximum trace length from the GMCH to ICH4 is four inches or less. The voltage divider circuit should be placed midway between the GMCH and ICH4. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). When the trace length exceeds four inches, the locally generated voltage reference divider should be used. Refer to Section 8.3.2 for more details. Figure 58 illustrates the single V_{REF}/V_{SWING} voltage generation circuit for Hub Interface.

Figure 58. Single V_{REF}/V_{SWING} Voltage Generation Circuit for Hub Interface



The resistor values, R1, R2, and R3 must be rated at one percent tolerance. Refer to Table 62 for Intel's recommended resistor values. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. Two 0.1 µF capacitors (C1 and C3) should be placed close to the divider. In addition, the 0.01-µF bypass capacitor (C2, C4, C5, and C6) should be placed within 0.25 inch of HLVREF/HI_{REF} pin (for C4 and C6) and HI_VSWING/PSWING pin (for C2 and C5).

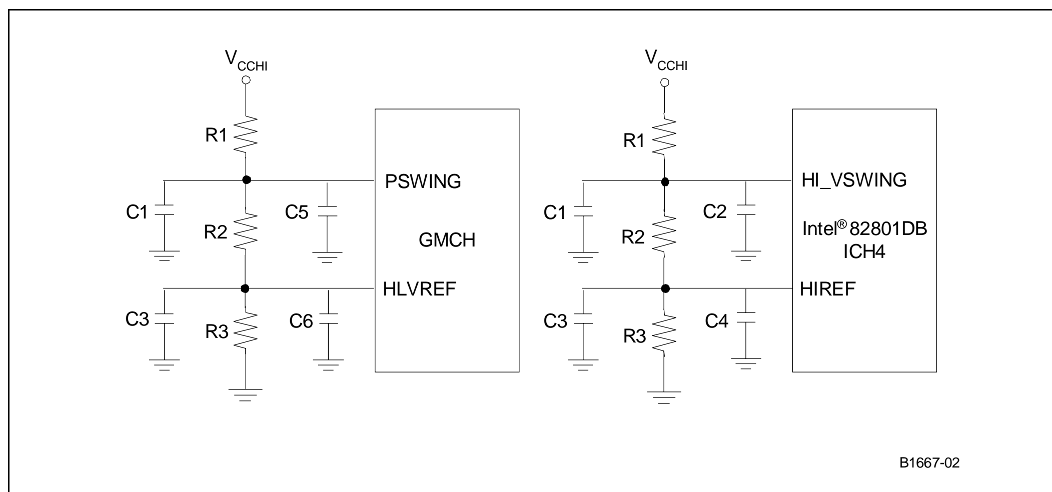
Table 62. Recommended Resistor Values for Single V_{REF}/V_{SWING} Divider Circuit

	Recommended Resistor Values			V_{CCHI}
Option 1	R1 = 80.6 Ω ± 1%	R2 = 51.1 Ω ±1%	R3 = 40.2 Ω ±1%	1.5 V
Option 2	R1 = 255 Ω ± 1%	R2 = 162 Ω ±1%	R3 = 127 Ω ±1%	1.5 V
Option 3	R1 = 226 Ω ± 1%	R2 = 147 Ω ±1%	R3 = 113 Ω ±1%	1.5 V
	C1 and C3 = 0.1 µF (near divider) C2, C4, C5, C6 = 0.01 µF (near component)			

8.3.2 Locally Generated Reference Voltage Divider Circuit

This section describes the option to generate the voltage references separately for GMCH and ICH4, to be used if the routing distance between GMCH and ICH4 is greater than four inches. One voltage divider circuit is used to generate both HIVREF and HI_VSWING voltage references for ICH4. Another voltage divider circuit is used for GMCH. The reference voltage for both HIVREF and HI_VSWING must meet the voltage specification in Table 61. The resistor values R1, R2, and R3 must be rated at one percent tolerance (see Table 62). Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). If the voltage specifications are not met, an individually generated voltage divider circuit for HIVREF and HI_VSWING is required. Figure 59 illustrates the ICH4 and GMCH locally generated reference voltage divider circuit.

Figure 59. Intel® 82801DB ICH4 and GMCH Locally Generated Reference Voltage Divider Circuit



8.3.3 Single GMCH and Intel® 82801DB I/O Controller Hub (ICH4) Voltage Generation/Separate Divider Circuit for V_{SWING}/V_{REF}

This section describes the option to use one voltage divider circuit for V_{REF}, shared by both ICH4 and GMCH, while using another voltage divider circuit for V_{SWING}. This allows for tuning the two reference voltages independently. The reference voltage for both HIVREF and HI_VSWING must meet the voltage specification in Table 61. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV).

Figure 60 illustrates the shared GMCH and ICH4 reference voltage with separate voltage divider circuit for V_{SWING} and V_{REG}.

Figure 60. Shared GMCH and Intel® 82801DB I/O Controller Hub 4 (ICH4) Reference Voltage with Separate Voltage Divider Circuit for V_{SWING} and V_{REG}

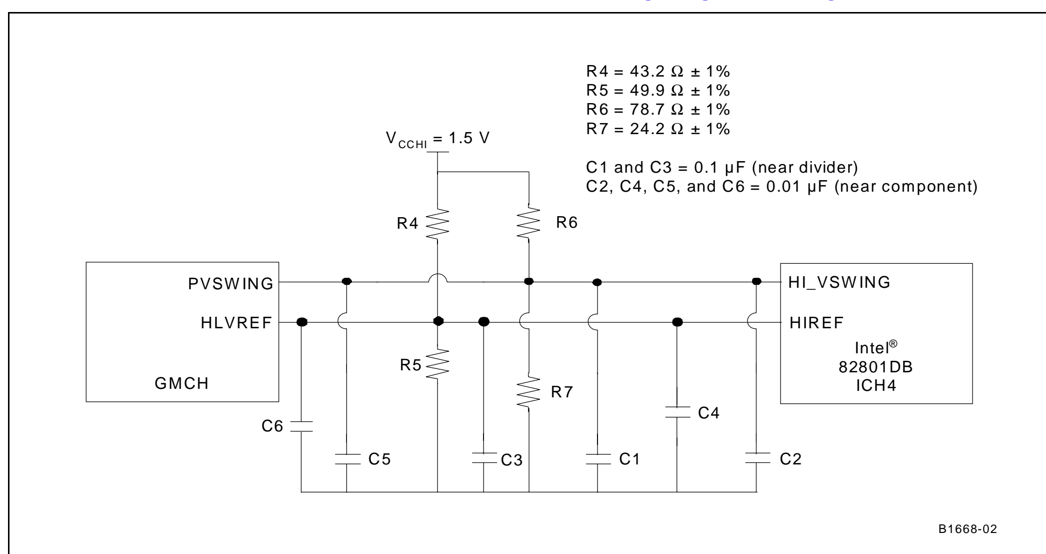


Table 63 presents Intel's recommended resistor values for separate HIVREF and HI_VSWING divider circuits.

Table 63. Recommended Resistor Values for Separate HIVREF and HI_VSWING Divider Circuits

Signal	Recommended Resistor Values	V_{CCHI}	Capacitor Value
HIVREF (350 mV)	R4 = 43.2 Ω ± 1% R5 = 49.9 Ω ± 1%	V_{CCHI} = 1.5 V	C3 = 0.1 µF (near divider) C2, C5 = 0.01 µF (near component)
HI_VSWING (800 mV)	R6 = 78.7 Ω ± 1% R7 = 24.2 Ω ± 1%	V_{CCHI} = 1.5 V	C1 = 0.1 µF (near divider) C4, C6 = 0.01 µF (near component)

8.3.4 Separate GMCH and Intel® 82801DB I/O Controller Hub (ICH4) Voltage Generation/Separate Divider Circuits for V_{REF} and V_{SWING}

This option allows for tuning the voltage references HIVREF and HI_VSWING individually, for both ICH4 and GMCH. The reference voltage for both HIVREF and HI_VSWING must meet the voltage specification in Table 61. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV).

Figure 61 illustrates the Individual HIVREF and HI_VSWING voltage reference divider circuits for the ICH4 and GMCH.

Figure 61. Individual HIVREF and HI_VSWING Voltage Reference Divider Circuits for the Intel® 82801DB I/O Controller Hub 4 (ICH4) and GMCH

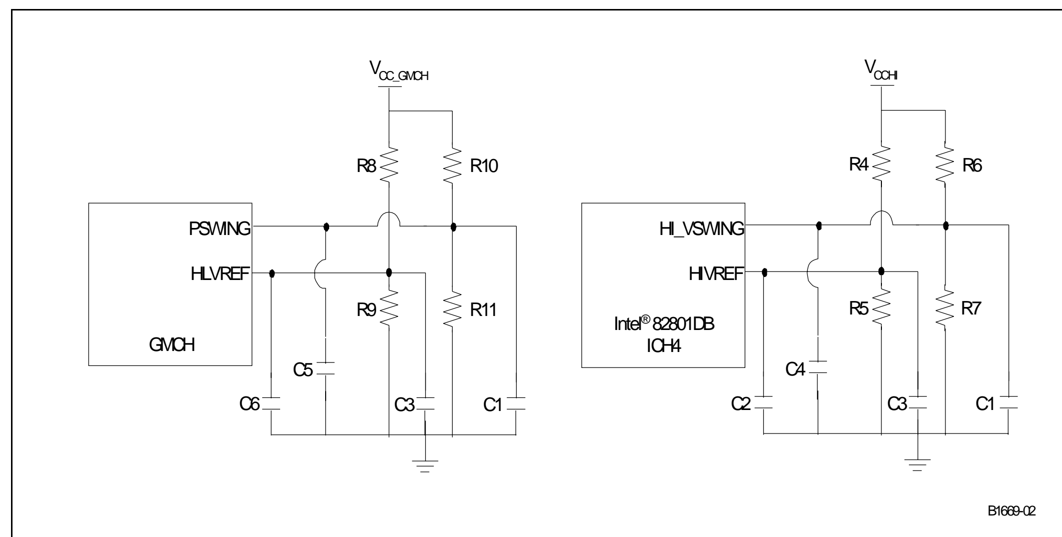


Table 64 presents Intel's recommended resistor values for HIVREF and HI_VSWING divider circuits for the ICH4 and GMCH.

Table 64. Recommended Resistor Values for HIVREF and HI_VSWING Divider Circuits for Intel® 82801DB I/O Controller Hub 4 (ICH4) and GMCH

Chipset Component	Signal	Recommended Resistor Values	V_{CCHI}	Capacitor value
Intel® 82801DB ICH4	HIVREF (350 mV)	R4 = 487 Ω ±1% R5 = 150 Ω ±1%	V_{CCHI} = 1.5 V	C3 = 0.1 µF (near divider) C2 = 0.01 µF (near component)
	HI_VSWING (800 mV)	R6 = 130 Ω ±1% R7 = 150 Ω ±1%	V_{CCHI} = 1.5 V	C1 = 0.1 µF (near divider) C4 = 0.01 µF (near component)
GMCH	HLVREF (350 mV)	R8 = 243 Ω ±1% R9 = 100 Ω ±1%	V_{CCGMCH} = 1.2 V	C3 = 0.1 µF (near divider) C6 = 0.01 µF (near component)
	PSWING (800 mV)	R10 = 49.9 Ω ±1% R11 = 100 Ω ±1%	V_{CCGMCH} = 1.2 V	C1 = 0.1 µF (near divider) C5 = 0.01 µF (near component)

8.4 Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1 µF capacitors per each component (i.e., the ICH4 and GMCH). These capacitors should be placed within 50 mils from each package, adjacent to the rows that contain the Hub Interface. When the layout allows, wide metal fingers running on the V_{SS} side of the board should connect the V_{CCHI} side of the capacitors to the V_{CCHI} power pins. Similarly, if layout allows, metal fingers running on the V_{CCHI} side of the board should connect the ground side of the capacitors to the VSS power pins.

I/O Subsystem 9

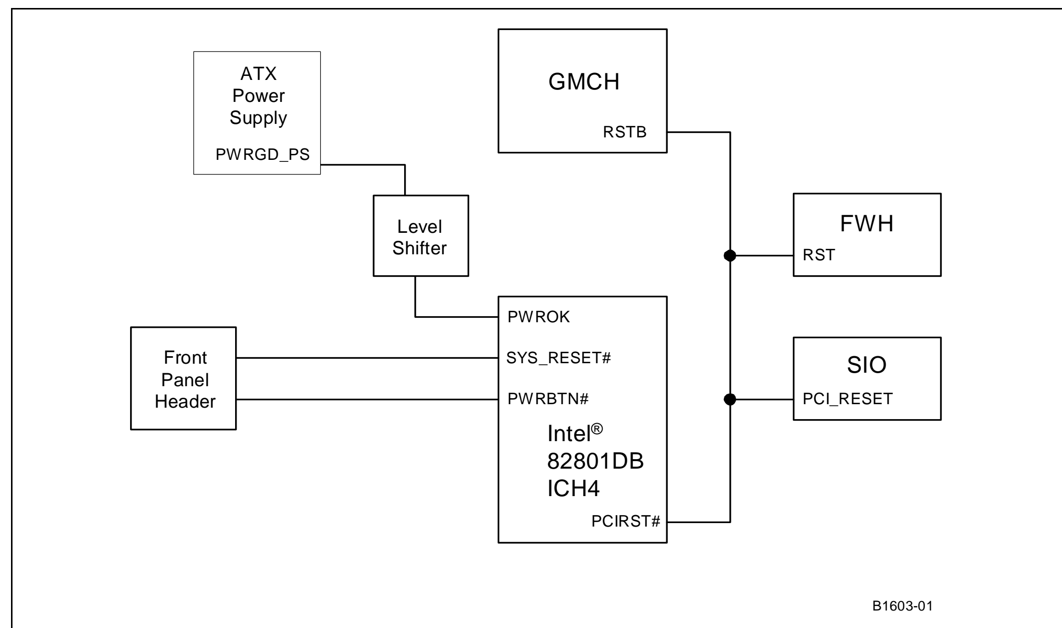
9.1 SYS_RESET# Usage Model

The System Reset signal (SYS_RESET#) on the Intel® 82801DB I/O Controller Hub 4 (ICH4) may be connected directly to the reset button on the system's front panel, provided that the front panel header pulls this signal up to 3.3 V standby through a weak pull-up resistor. The ICH4 has internal logic to debounce this signal for 16 ms, allowing the SMBus to go idle before resetting the system. This helps prevent slave devices on the SMBus from hanging because they are reset in the middle of a cycle. When a Pentium® M processor ITP700FLEX debug port is implemented on the system, Intel recommends that the DBR# signal of the ITP interface be connected to SYS_RESET# as well.

9.2 PWRBTN# Usage Model

The Power Button signal (PWRBTN#) on the ICH4 may be connected directly to the power button on the system's front panel. This signal is internally pulled-up to 3.3 V standby through a weak pull-up resistor (24 kΩ nominal). The ICH4 has internal logic to debounce this signal for 16 ms. Figure 62 illustrates the SYS_RESET# and PWRTBN# connection.

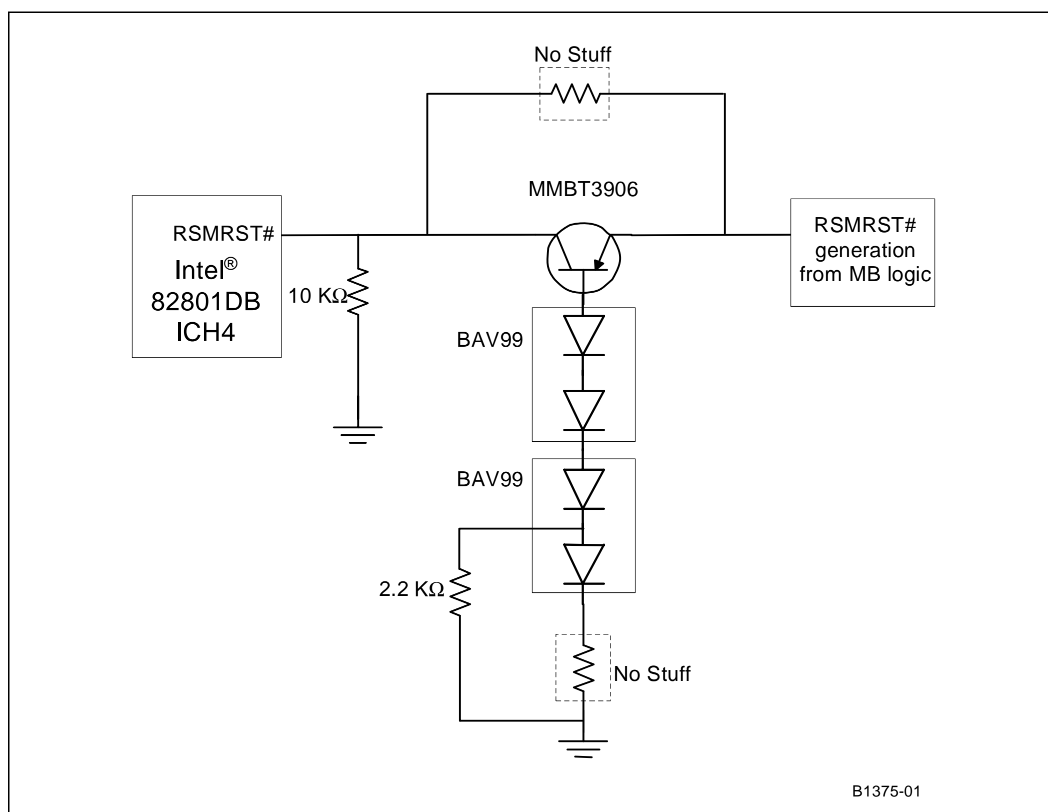
Figure 62. SYS_RESET# and PWRBTN# Connection



9.2.1 Power Well Isolation Control Strap Requirements

The circuit shown in Figure 63 may be implemented to control well isolation between the V_{CCSUS}3_3 and RTC power wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail. Failure to implement this circuit or a circuit that functions similar to this may result in excessive droop on the V_{CCRTC} node during Sx-to-G3 power state transitions (removal of AC power and battery power). Droop on this node may potentially cause the CMOS to be cleared or corrupted, the RTC to lose time after several AC/battery power cycles, or the intruder bit might assert erroneously. Figure 63 illustrates the RTC power well isolation control.

Figure 63. RTC Power Well Isolation Control



9.3 IDE Interface

This section contains guidelines for connecting and routing the ICH4 IDE interface. The ICH4 has two independent IDE channels. The ICH4 has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors may be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0 Ω resistors may be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface may be routed with 5 mil traces on 7 mil spaces, and must be less than eight inches long (from ICH4 to IDE connector). Additionally, the maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inch.

9.3.1 Cabling

- Length of cable: Each IDE cable must be equal to or less than 18 inches.
- Capacitance: Less than 35 pF
- Placement: A maximum of six inches between drive connectors on the cable. When a single drive is placed on the cable it should be placed at the end of the cable. When a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (six inches away from the end of the cable).
- Grounding: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- ICH4 Placement: The ICH4 must be placed equal to or less than eight inches from the ATA connector(s).

9.3.1.1 Cable Detection for Ultra ATA 66 and Ultra ATA100

The ICH4 IDE controller supports PIO, Multi-word (8237 style) DMA, Ultra DMA modes 0 through 5, and Native Mode IDE.

Note: There are no motherboard hardware requirements for supporting Native Mode IDE. Native Mode IDE is supported through the operating system and system drivers. The ICH4 must determine the type of cable that is present to configure itself for the fastest possible transfer mode that the hardware may support.

An 80-conductor IDE cable is required for Ultra DMA modes greater than two (Ultra ATA/33). This cable uses the same 40 pin connector as the old 40 pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, and so on. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40 pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification may be obtained from the Small Form Factor Committee.

To determine if Ultra DMA modes greater than two (Ultra ATA/33) may be enabled, the ICH4 requires the system software to attempt to determine the cable type used in the system. When the system software detects an 80 conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. When a 40 conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

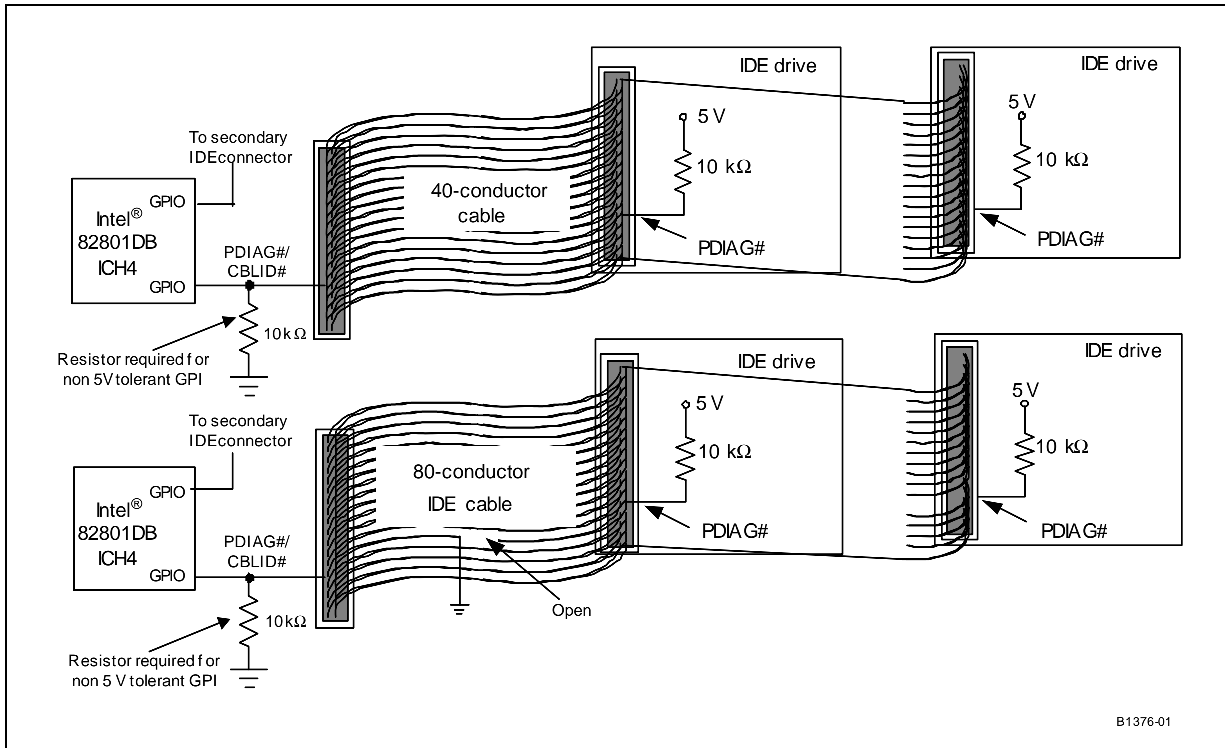
Intel recommends that cable detection be done using a combination host-side/device-side detection mechanism.

Note: Host-Side detection cannot be implemented on an NLX form factor system because this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the device-side detection mechanism only.

9.3.1.2 Combination Host-Side/Device-Side Cable Detection

Host-side detection (described in the *ATA/ATAPI-6 Standard*) requires the use of two GPI pins (one for each IDE channel). Figure 64 illustrates the proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. A 10 kΩ pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present, and allows for use of a non-5 V tolerant GPIO.

Figure 64. Combination Host-Side/Device-Side IDE Cable Detection



This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. When the signal is high, there is 40 conductor cable in the system and Ultra DMA modes greater than two must not be enabled.

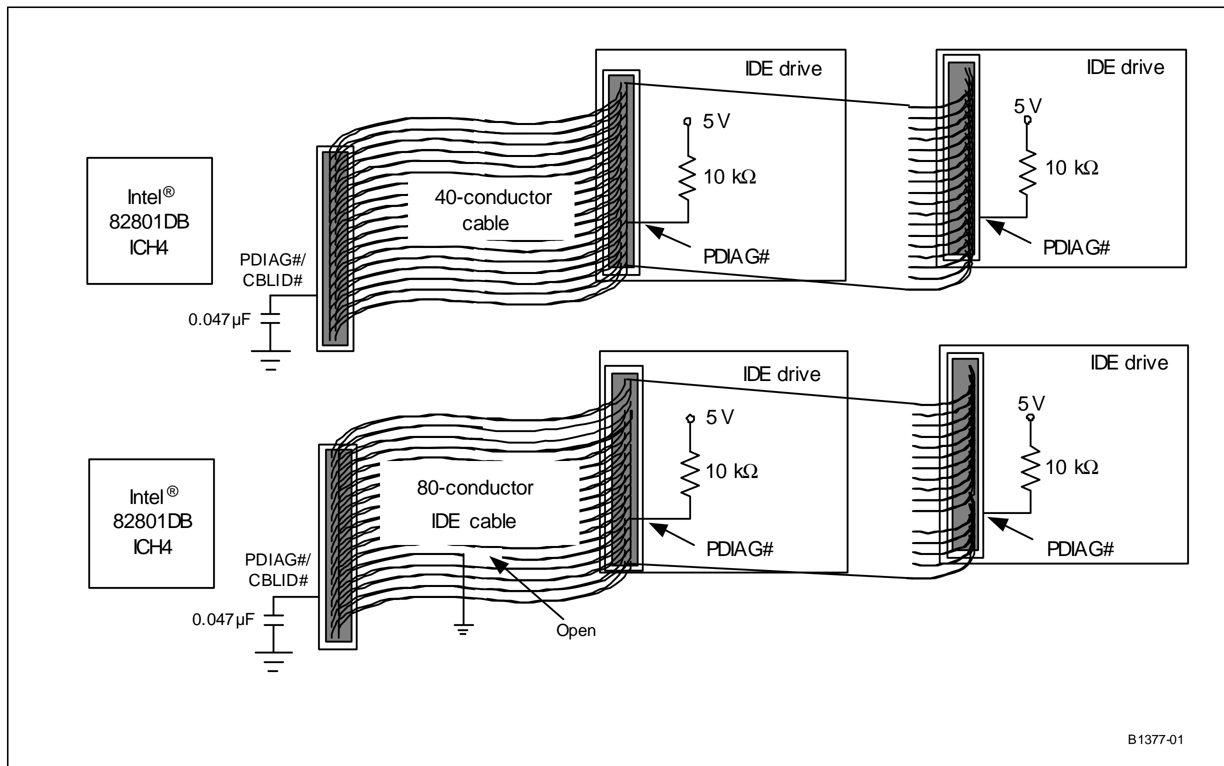
When PDIAG#/CBLID# is detected low, there may be an 80 conductor cable in the system, or there may be a 40 conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-6 Standard. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than two. When ID Word 93, bit 13, is a ‘1’, an 80 conductor cable is present. When this bit is ‘0’, a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40 conductor cable is present and should notify the user of the problem.

9.3.1.3 Device-Side Cable Detection

For platforms that must implement device-side detection only (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in Figure 65. This capacitor should not be populated when implementing Intel's recommended combination host-side/device-side cable detection mechanism described above.

Note: Some drives may not support device-side cable detection.

Figure 65. Device Side IDE Cable Detection



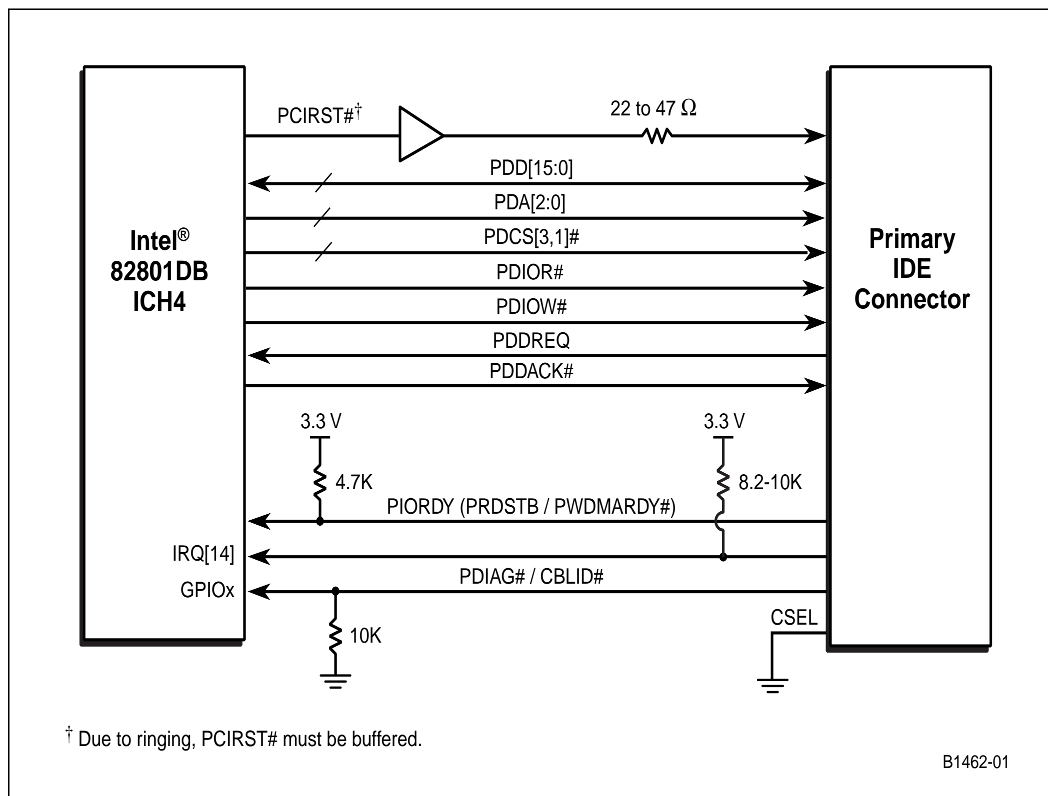
This mechanism creates a resistor-capacitor (RC) time constant. Drives supporting Ultra DMA modes greater than two (Ultra DMA/33) drives PDIAG#/CBLID# low, then releases it (pulled up through a 10 K resistor). The drive samples the signal after releasing it. In an 80 conductor cable, PDIAG#/CBLID# is not connected through to the host; therefore the capacitor has no effect.

In a 40 conductor cable, the signal is connected to the host. Therefore the signal rises more slowly as the capacitor charges. The drive may detect the difference in rise times, and reports the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the *ATA/ATAPI-6 Standard*.

9.3.2 Primary IDE Connector Requirements

Figure 66 illustrates connections requirements for the Primary IDE connector.

Figure 66. Connection Requirements for the Primary IDE Connector



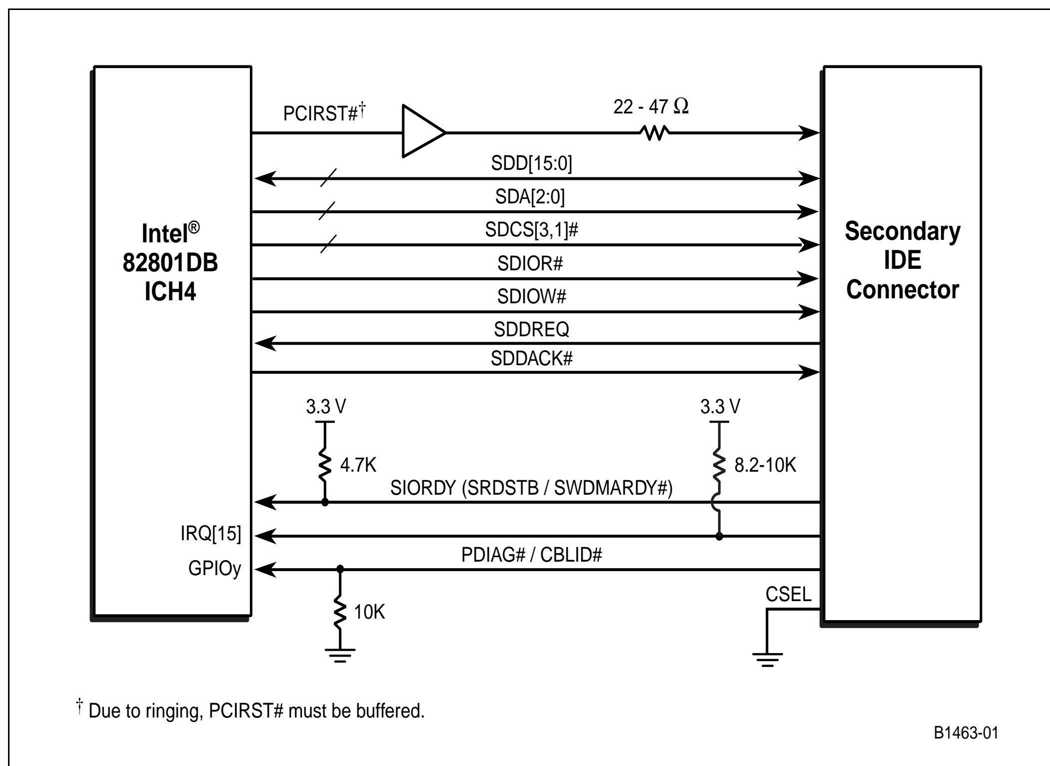
Follow these requirements for the Primary IDE connector.

- 22 Ω - 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 KΩ - 10 KΩ pull-up resistor is required on IRQ14 to V_{CC}3_3.
- A 4.7 KΩ, pull-up resistor to V_{CC}3_3 is required on PIORDY and SIORDY.
- Series resistors may be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10 KΩ resistor to ground on the PDIAG#/CBLID# signal is required on the primary connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

9.3.3 Secondary IDE Connector Requirements

Figure 67 illustrates connection requirements for the Secondary IDE connector.

Figure 67. Connection Requirements for Secondary IDE Connector



Follow these requirements for the Secondary IDE connector.

- 22 Ω - 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 KΩ - 10 KΩ pull-up resistor is required on IRQ15 to V_{CC}3_3.
- A 4.7 KΩ, pull-up resistor to V_{CC}3_3 is required on PIORDY and SIORDY.
- Series resistors may be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10 KΩ resistor to ground on the PDIAG#/CBLID# signal is required on the secondary connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

9.4 PCI

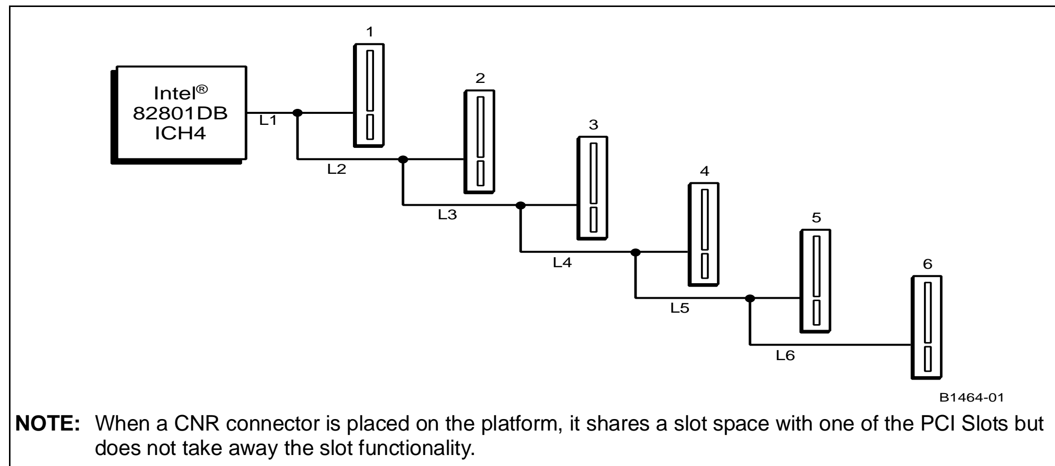
The ICH4 provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification,* Revision 2.2. The implementation is optimized for high performance data streaming when the ICH4 is acting as either the target or the initiator in the PCI bus.

The ICH4 supports six PCI Bus masters (excluding the ICH4), by providing six REQ#/GNT# pairs. In addition, the ICH4 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

9.4.1 PCI Routing Summary

The following represents a summary of the routing guidelines for the PCI slots. Simulations assume that PCI cards follow the PCI Revision 2.2 specification trace length guidelines. Figure 68 illustrates the PCI bus layout example.

Figure 68. PCI Bus Layout Example



NOTE: When a CNR connector is placed on the platform, it shares a slot space with one of the PCI Slots but does not take away the slot functionality.

Figure 69 illustrates the PCI bus layout with IDSEL.

Figure 69. PCI Bus Layout with IDSEL

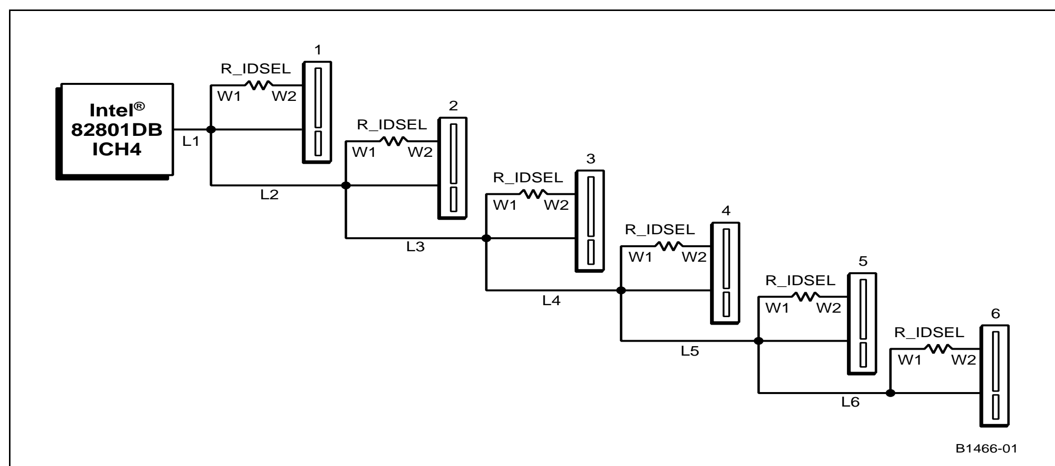


Table 65 presents the PCI data signals routing summary.

Table 65. PCI Data Signals Routing Summary

PCI Routing Req.	Trace Impedance	Topology	Maximum Trace Length (Inches)					
			L1	L2	L3	L4	L5	L6
5 on 7	47 Ω to 69 Ω 60 Ω target	Two Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1.5	N/A	N/A	N/A	N/A
		Two Slots with one down device W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1	3	N/A	N/A	N/A
		Three Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1.5	1.5	N/A	N/A	N/A
		Three Slots with one down device W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1	1	3	N/A	N/A
		Four Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1	1	1	N/A	N/A
		Four Slots with one down device W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 10	1	1	1	3	N/A
	51 Ω to 69 Ω 60 Ω target	Five Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 8	1	1	1	1	N/A
		Six Slots W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω	5 to 7	1	1	1	1	1

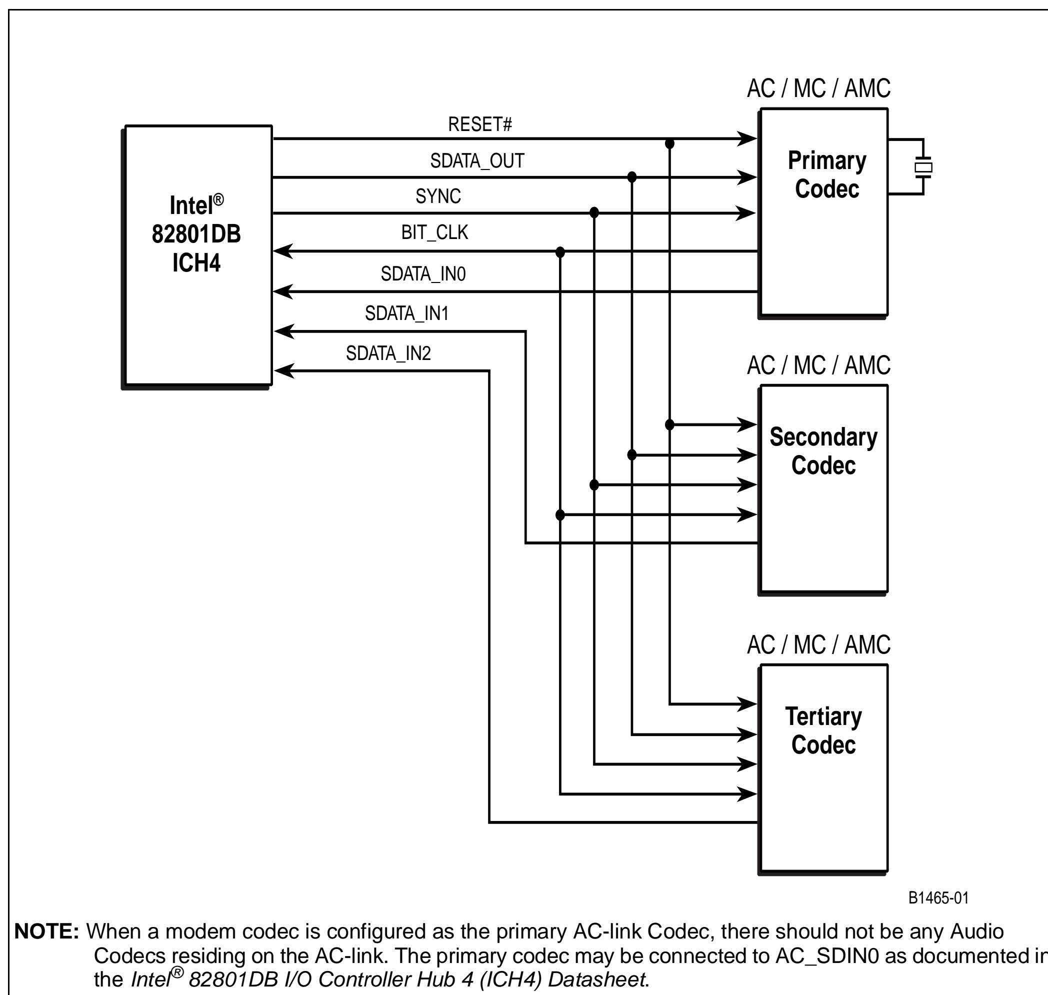
9.5 AC’97

The ICH4 implements an AC’97 2.1, 2.2, and 2.3 compliant digital controller. Contact your codec IHV (Independent Hardware Vendor) for information on 2.2 compliant products. The AC’97 2.2 specification is on the Intel website at: http://developer.intel.com/ial/scalableplatforms/audio

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH4 AC-link allows a maximum of three codecs to be connected.

Figure 70 illustrates a three-codec topology of the AC-link for the ICH4.

Figure 70. Intel® 82801DB I/O Controller Hub 4 (ICH4) AC'97 – Codec Connection



NOTE: When a modem codec is configured as the primary AC-link Codec, there should not be any Audio Codecs residing on the AC-link. The primary codec may be connected to AC_SDIN0 as documented in the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*.

Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH4) and to any other codec present. That clock is used as the time base for latching and driving data. **Clocking AC_BIT_CLK directly off the CK-408 clock chip's 14.31818 MHz output is not supported.**

The ICH4 supports wake-on-ring from S1-S5 via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH4 has weak pull-down/pull-ups that are always enabled. This keeps the link from floating when the AC-link is off or there are no codecs present.

When the shut-off bit is not set, it implies that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOUT are driven by the codec and the ICH4 respectively. However, AC_SDIN0, AC_SDIN1, and AC_SDIN2 may not be driven. When the link is enabled, the assumption may be made that there is at least one codec.

Figure 71 illustrates the ICH4 AC'97 - AC_BIT_CLK topology.

Figure 71. Intel® 82801DB I/O Controller Hub 4 (ICH4) AC'97 – AC_BIT_CLK Topology

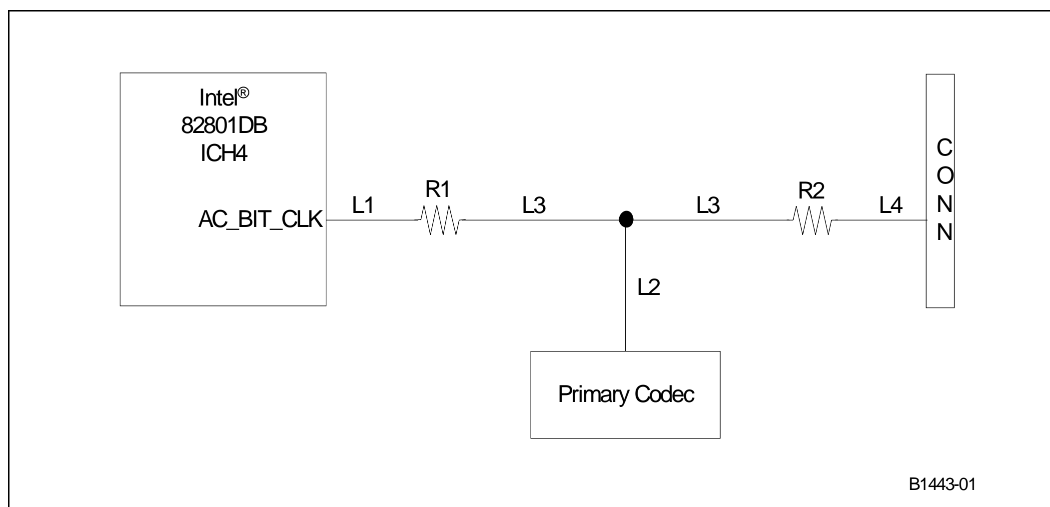


Table 66 presents the AC'97 AC_BIT_CLK routing summary.

Table 66. AC'97 AC_BIT_CLK Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_BIT_CLK Signal Length Matching
5 on 5	L1 = (1 to 8) – L3 L2 = 0.1 to 6 L3 = 0.1 to 0.4 L4 = (1 to 6) – L3	R1 = 33 Ω - 47 Ω R2 = Option 0 Ω resistor for debugging purposes	N/A

NOTES:
1. Simulations were performed using Analog Device's* Codec (AD1885) and the Cirrus Logic's* Codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data indicates that a 47 Ω resistor for R1 is best for the Sigmatel* 9750 codec.

Figure 72 illustrates the ICH4 AC'97 – AC_SDOUT/ AC_SYNC topology.

Figure 72. Intel® 82801DB I/O Controller Hub 4 (ICH4) AC'97 – AC_SDOUT/AC_SYNC Topology

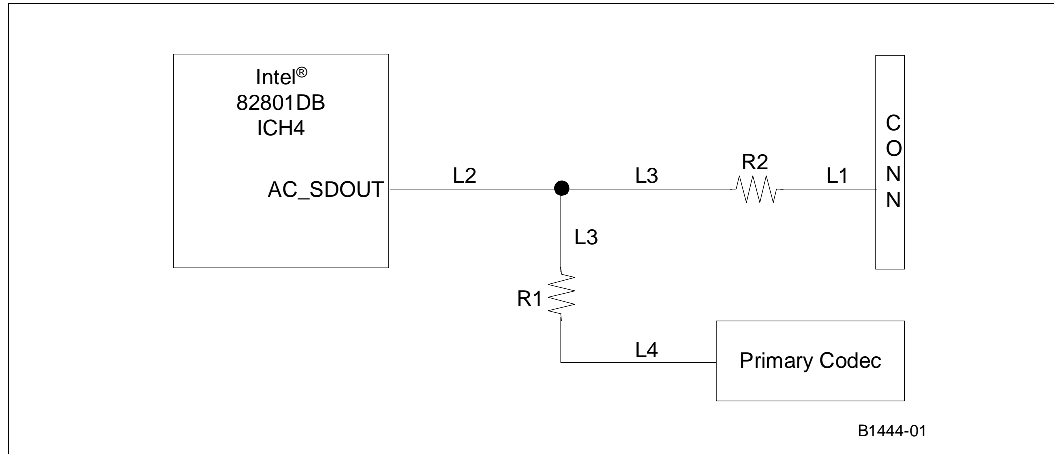


Table 67 presents the AC'97 AC_SDOUT/AC_SYNC routing summary.

Table 67. AC'97 AC_SDOUT/AC_SYNC Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_SDOUT/AC_SYNC Signal Length Matching
5 on 5	L1 = (1 to 6) – L3 L2 = 1 to 8 L3 = 0.1 to 0.4 L4 = (0.1 to 6) – L3	R1 = 33 Ω - 47 Ω R2 = R1 if the connector card that is going to be used with the platform does not have a series termination on the card. Otherwise R2 = 0 Ω.	N/A

NOTES:
1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel* 9750 codec.

Figure 73 illustrates the ICH4 AC’97 – AC_SDIN topology.

Figure 73. Intel® 82801DB I/O Controller Hub 4 (ICH4) AC’97 – AC_SDIN Topology

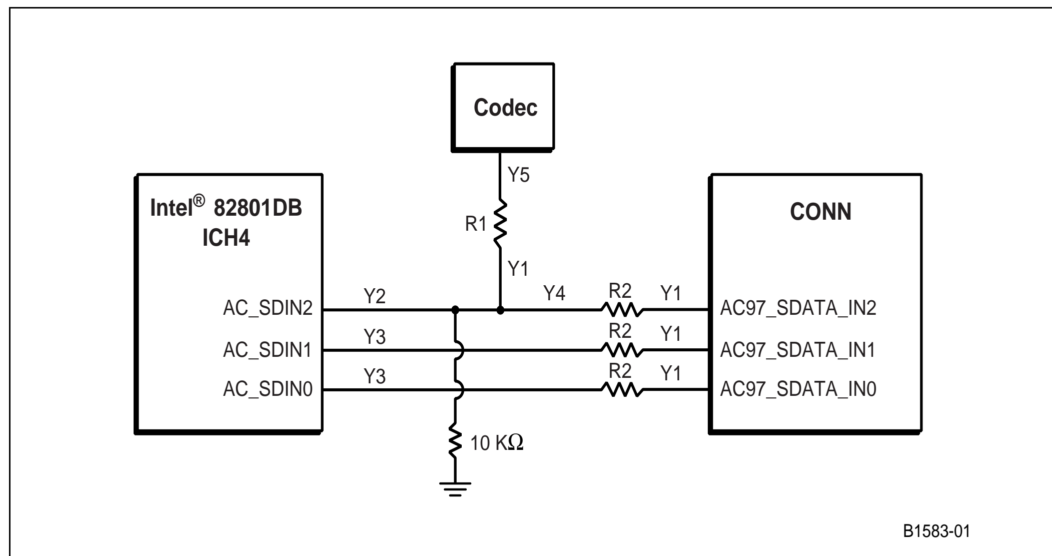


Table 68 presents the AC’97 AC_SDIN routing summary.

Table 68. AC’97 AC_SDIN Routing Summary

AC’97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_SDIN Signal Length Matching
5 on 5	Y1 = 0.1 to 0.4 Y2 = (1 to 8) – Y1 Y3 = (1 to 14) – Y1 Y4 = (1 to 6) – Y1 Y5 = (0.1 to 6) – Y1	R1 = 33 Ω - 47 Ω R2 = R1 if the connector card that is going to be used with the platform does not have a series termination on the card. Otherwise R2 = 0 Ω	N/A

NOTES:
1. Simulations were performed using Analog Device’s Codec (AD1885) and the Cirrus Logic’s Codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel 9750 codec.

9.5.1 AC'97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors may be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper and electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper and electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

9.5.2 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH4 platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH4 platform.

- Active components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH4 supports wake-on-ring from S1-S5 states via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. When no codec is attached to the link, internal pull-downs prevent the inputs from floating, so external resistors are not required.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

9.5.2.1 Valid Codec Configurations

Table 69 presents supported codec configurations.

Table 69. Supported Codec Configurations

Option	Primary Codec	Secondary Codec	Tertiary Codec	Notes
1	Audio	Audio	Audio	1
2	Audio	Audio	Modem	1
3	Audio	Audio	Audio/Modem	1
4	Audio	Modem	Audio	1
5	Audio	Audio/Modem	Audio	1
6	Audio/Modem	Audio	Audio	1

NOTES:
1. For power management reasons, codec power management registers are in audio space. As a result, if there is an audio codec in the system it must be primary.
2. There cannot be two modems in a system because there is only one set of modem DMA channels.
3. The ICH4 supports a modem codec on any of the AC-SDIN lines. However the modem codec ID must be either 00 or 01.

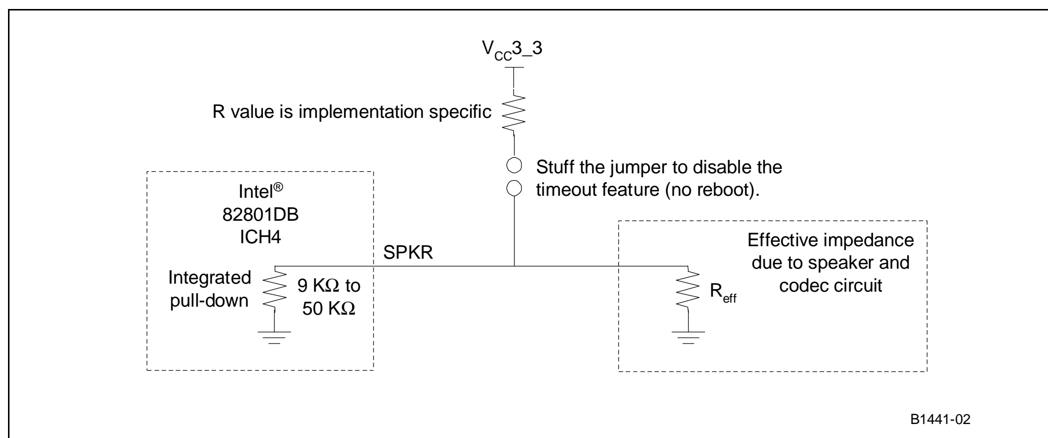
9.5.3 SPKR Pin Configuration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the TCO Timer Reboot function based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH4 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Its default state is a logical zero or set to reboot. To disable the feature, a jumper may be populated to pull the signal line high (see Figure 74).

The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{eff}), and the ICH4's integrated pull-down resistor are read as logic high (0.5 * $V_{CC}3_3$ to $V_{CC}3_3$ + 0.5 V).

Figure 74 illustrates an example of the speaker circuit.

Figure 74. Example Speaker Circuit



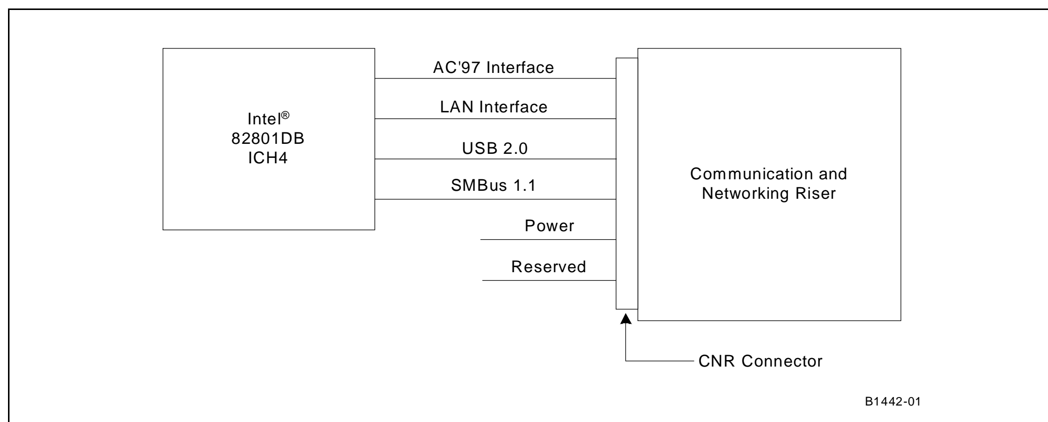
9.6 CNR

Refer to the related documents, *Communication and Network Riser Specification,* Revision 1.2, available at: http://developer.intel.com/technology/cnr/cnrspec_12.htm.

The Communication and Networking Riser (CNR) specification defines a hardware scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. This interface supports multi-channel audio, V.90 analog modem, phone-line based networking, 10/100 Ethernet-based networking, SMBus Interface Power Management Rev 1.1, and USB 2.0. The CNR specification defines the interface, which should be configured prior to shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot, therefore the system designer may not sacrifice a PCI slot if he decides not to include a CNR in a particular build.

Figure 75 illustrates the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. The Platform LAN Connection (PLC) may be either an Intel® 82562ET, or an Intel® 82562EM device. Refer to the CNR specification for additional information.

Figure 75. CNR Interface



9.6.1 AC’97 Audio Codec Detect Circuit and Configuration Options

Table 70 presents signal descriptions of general circuits to implement a number of different codec configurations.

Refer to the *Communication and Network Riser Specification,* Revision 1.2, for Intel’s recommended codec configurations.

Table 70. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC’97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC'97 Interface (held in reset), because the CNR codec(s) is going to be the primary device(s) on the AC'97 Interface.
AC_RST#	Reset signal from the AC'97 Digital Controller (ICH4).
AC_SDINn	AC'97 serial data from an AC'97-compliant codec to an AC'97-compliant controller (i.e., the ICH4).

9.6.2 CNR 1.2 AC’97 Disable and Demotion Rules for the Motherboard

The following are the CNR1.1/1.2 AC’97 Disable and Demotion Rules for the motherboard:

1. All AC’97 Rev. 2.2.non-chaining codecs on the motherboard must always disable themselves when the CDC_DN_ENAB# signal is in a high state.
2. A motherboard AC’97 Codec must never change its address or SDATA_IN line used, regardless of the state of the CDC_DN_ENAB# signal.
3. On a motherboard containing an AC’97 controller supporting three AC’97 Codecs, the AC’97 Revision 2.2, or AC’97 Revision 2.3 codec on the motherboard, must be connected to the SDATA_IN2 signal of the CNR connector.
4. A motherboard should not contain more than a single AC’97 codec.

These rules allow for forward and backward compatibility between CNR Version 1.1/1.2 cards.

For more information on chaining, consult the *Communication and Network Riser Specification,* Revision 1.2.

Figure 76 illustrates motherboard AC’97 CNR implementation with a single codec down onboard.

Figure 76. Motherboard AC’97 CNR Implementation with a Single Codec Down Onboard

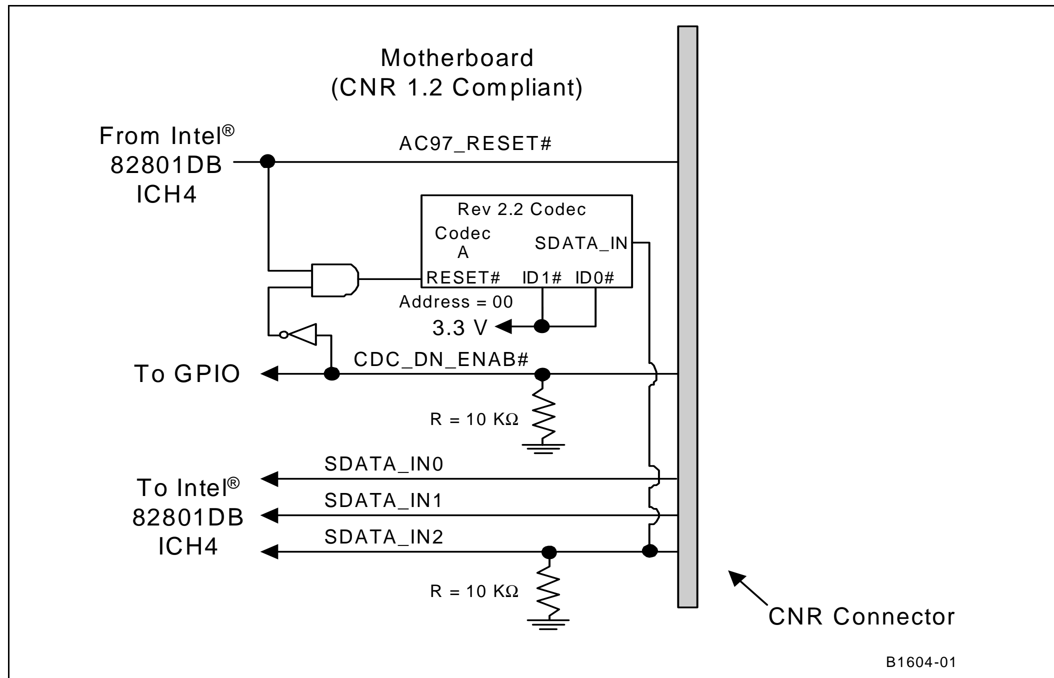
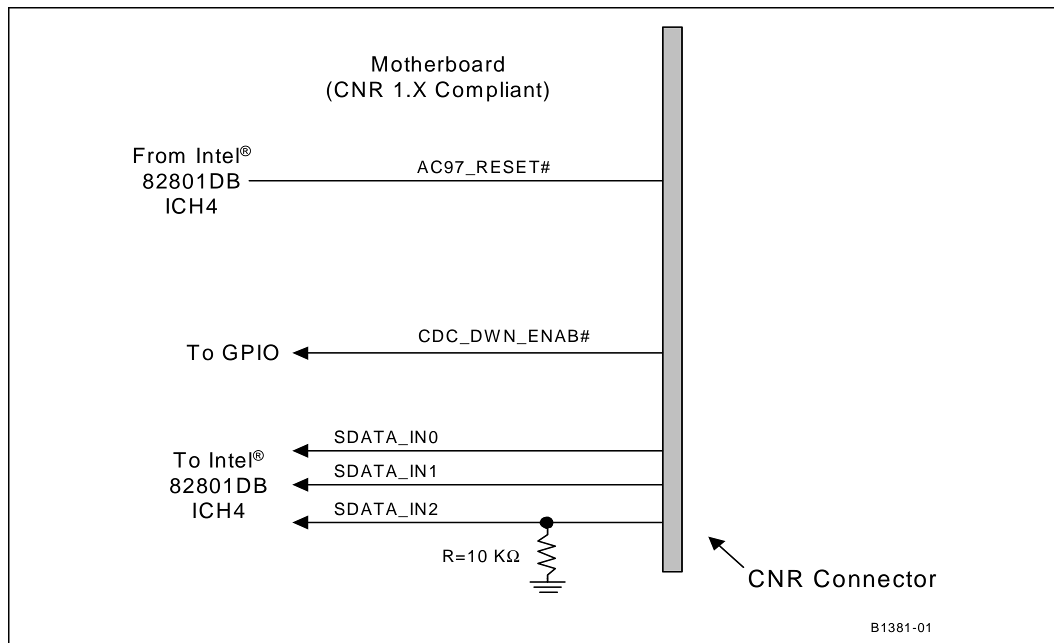


Figure 77 illustrates motherboard AC’97 CNR implementation with no codec down onboard.

Figure 77. Motherboard AC’97 CNR Implementation with No Codec Down Onboard



9.6.3 CNR Routing Summary

Table 71 presents a summary of the various interface routing requirements of the CNR Riser.

Table 71. CNR Routing Summary

CNR Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
USB (4 on 4.5) Data pair must be at least 20 mils from nearest neighbor	10 inches	No more than 150 mils trace mismatch.	Ground
AC '97 (5 on 5)	AC_BIT_CLK (Refer to Table 66.) AC_SDOUT (Refer to Table 67.) AC_SDIN (Refer to Table 68.)	N/A	Ground
LAN (5 on 10)	9.5 inches (Refer to Table 81.)	Equal to or up to 500 mils shorter than the LAN_CLK trace.	Ground

9.7 USB 2.0 Guidelines and Recommendations

9.7.1 Layout Guidelines

9.7.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines help minimize signal quality and EMI problems. The USB 2.0 validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second plane is power, the third plane is ground and the fourth is a signal layer. This results in the placement of most of the routing on the fourth plane (closest to the ground plane), allowing a higher component density on the first plane.

1. Place the ICH4 and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
2. USB 2.0 signals should be ***ground referenced***.
3. Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
5. Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
6. Stubs on high-speed USB signals should be avoided, as stubs cause signal reflections and affect signal quality. When a stub is unavoidable in the design, the sum of all stubs for a particular signal line should not exceed 200 mils.

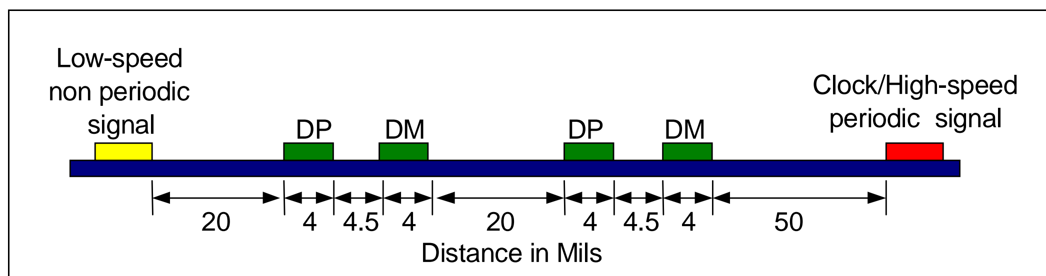
7. Route all traces over continuous planes (V_{CC} or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 9.7.2 for more information.
8. Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
9. Keep USB 2.0 USB signals clear of the core logic set. High current transients are produced during internal state transitions and may be very difficult to filter out.
10. Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (V_{CC} or GND, depending on the plane the trace is over). For the suggested stack-up the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

9.7.1.2 USB 2.0 Trace Separation

Use the following separation guidelines. Figure 78 illustrates Intel's recommended USB trace spacing.

1. Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. Deviations normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the least possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stack-up being used. 4 mil traces with 4.5 mil spacing results in approximately 90 Ω differential trace impedance.
3. Minimize the length of high-speed clock and periodic signal traces that run parallel to high-speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
4. Based on simulation data, use 20 mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

Figure 78. Recommended USB Trace Spacing



9.7.1.3 USBRBIAS Connection

The USBRBIAS pin and the USBRBIAS# pin may be shorted and routed 5 on 5 to one end of a 22.6 Ω ± 1% resistor to ground. Place the resistor within 500 mils of the ICH4 and avoid routing next to clock pins. Figure 79 illustrates a USBRBIAS connection.

Figure 79. USBRBIAS Connection

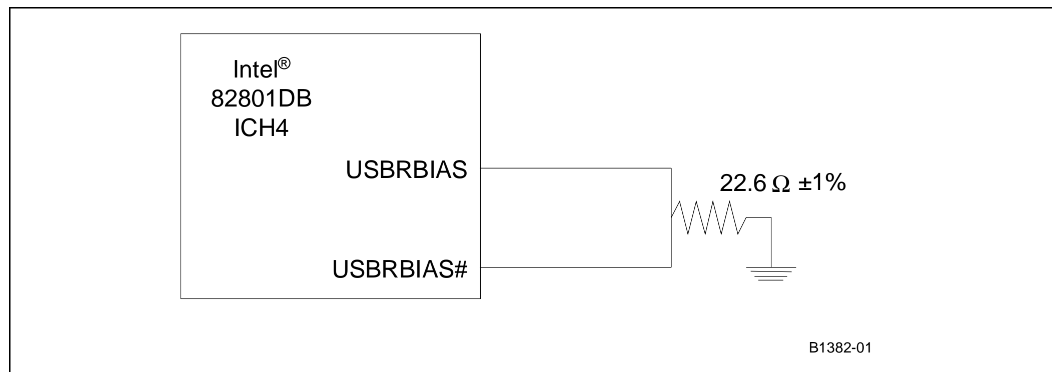


Table 72 presents the USBRBIAS/USBRBIAS# routing summary.

Table 72. USBRBIAS/USBRBIAS# Routing Summary

USBRBIAS/ USBRBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
5 on 5	500 mils	N/A	N/A

9.7.1.4 USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. Refer to Section 9.7.4 for details.

9.7.1.5 USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Maximum trace length mismatch between USB 2.0 signal pair should be no greater than 150 mils.

9.7.1.6 USB 2.0 Trace Length Guidelines

Table 73 presents the USB 2.0 trace length preliminary guidelines, with common-mode choke.

Table 73. USB 2.0 Trace Length Preliminary Guidelines with Common-Mode Choke)

Topology	USB 2.0 Routing Requirements/ Trace Impedance	Signal Referencing	Signal Matching	Cable Length	Motherboard Trace Length	Card Trace Length	Maximum Total Length
Back Panel	4 on 4.5/90 Ω differential	Ground	The max mismatch between data pairs should not be greater than 150 mils	N/A	17 inches	N/A	17 inches
CNR	4 on 4.5/90 Ω differential	Ground		N/A	8 inches	6 inches	14 inches
Front Panel	4 on 4.5/90 Ω differential	Ground		9	6	2	17
				10.5	5	2	17.5
				12	4	2	18
				13.5	3	2	18.5
				15	2	2	19

NOTES:
1. These lengths are based on simulation results and may be updated in the future.
2. All lengths are based on using a common-mode choke. Refer to Section 9.7.4 for details on common-mode choke.
3. Numbers in this table are based on the following assumptions:
   a) CNR configuration: maximum six inches trace on add-on card.
4. An approximate 1:1 trade-off may be assumed from motherboard trace length vs. daughtercard trace length (e.g., trade one inch of daughtercard for one inch of motherboard trace lengths).
5. Numbers in the table are based on the following simulation assumptions:
   a) Trace length on front panel connector card assumed a maximum of two inches.
   b) USB twisted pair shielded cable as specified in USB 2.0 specification was used.

9.7.2 Plane Splits, Voids, and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cutouts.

9.7.2.1 V_{CC} Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the V_{CC} plane.

1. Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them. USB signaling is not purely differential in all speeds (i.e., the Full-speed Single Ended Zero is common mode).
2. Avoid routing of USB 2.0 signals 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

   When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

   When crossing a plane split is completely unavoidable, proper placement of stitching caps may minimize the adverse effects on EMI and signal quality performance caused by crossing

the split. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge or bypass power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates V_{CC}5 and V_{CC}3_3 planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to V_{CC}5 and the other side should tie to V_{CC}3_3. Stitching caps provide a high-frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

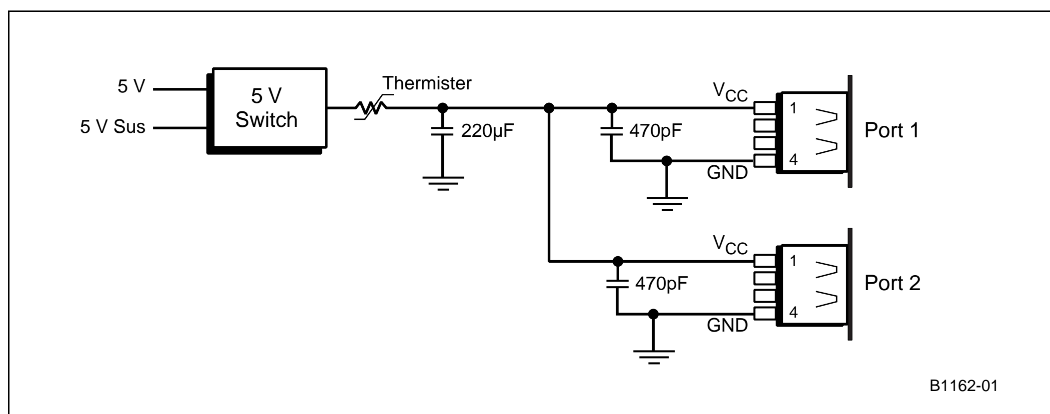
9.7.2.2 GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

9.7.3 USB Power Line Layout Topology

This section presents a suggested topology for power distribution of Vbus to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach fly-back protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach fly-back voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port and the power carrying traces should be as wide as possible, preferably, a plane. A good rule-of-thumb is to make the power-carrying traces wide enough that the system fuse blows on an over-current event. When the system fuse is rated at 1 A, the power carrying traces should be wide enough to carry at least 1.5 A. Figure 80 illustrates a good downstream power connection.

Figure 80. Good Downstream Power Connection



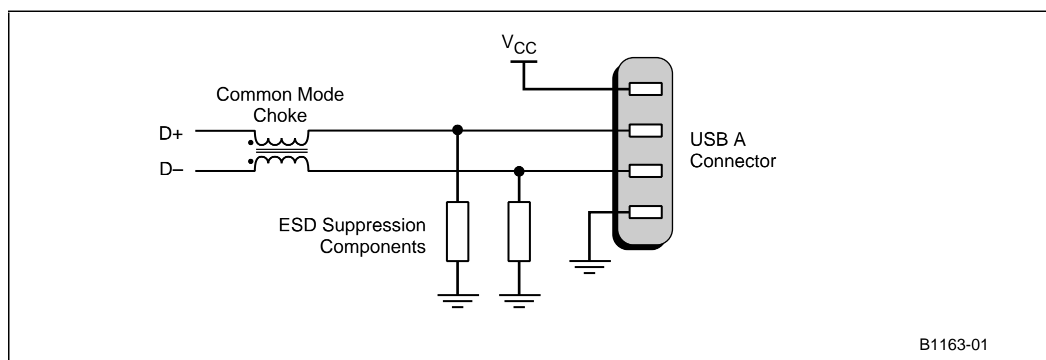
9.7.4 EMI Considerations

The following guidelines apply to the selection and placement of common-mode chokes and ESD protection devices.

9.7.4.1 Common Mode Chokes

Testing has shown that common-mode chokes may provide required noise attenuation. A design should include a common-mode choke footprint to provide a stuffing option **in the event** the choke is needed to pass EMI testing. Figure 81 illustrates the schematic of a typical common-mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins. In systems that route USB to a front panel header, the choke should be placed on the front panel card.

Figure 81. Common-Mode Choke Schematic



Common-mode chokes distort full-speed and high-speed signal quality. As the common-mode impedance increases, the distortion increases, so you need to test the effects of the common-mode choke on full speed and high-speed signal quality. Common-mode chokes with a target impedance of 80 Ω to 90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common-mode choke that meets the designer’s needs is a two-step process.

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
2. After you have a part that gives passing EMI results the second step is to test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed and high-speed USB operation.

9.7.5 ESD

Classic USB (1.0/1.1) provided ESD suppression using in-line ferrites and capacitors that formed a low pass filter. This technique does not work for USB 2.0 due to the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 81. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common-mode choke solution, Intel recommends including footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

9.7.6 Front Panel Solutions

9.7.6.1 Internal USB Cables

The front panel internal cable solution chosen must meet all the requirements of Chapter 6 of the USB 2.0 specification for high-/full-speed cabling for each port with the exceptions described in Cable Option 2.

9.7.6.1.1 Internal Cable Option 1

Use standard high-speed/full-speed compatible USB cables. These must meet all cabling requirements called out in Chapter 6 of the USB 2.0 specification. Intel's recommended motherboard mating connector pin-out is covered in detail later in this document.

9.7.6.1.2 Internal Cable Option 2

Use custom cables that meet all of the requirements of Chapter 6 of the USB 2.0 specification with the following additions/exceptions.

- They may share a common jacket, shield and drain wire.

Two ports with signal pairs that share a common jacket may combine Vbus and ground wires into a single wire provided the following conditions are met:

- The bypass capacitance required by Section 7.2.4.1 of the USB 2.0 specification is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughtercard). Refer to the front panel daughtercard referenced later for details.
- Selecting proper wire size: A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the USB 2.0 specification that has = ½ the resistance of either of the two wires being combined. The data is provided for reference in Table 74.

Table 74. Conductor Resistance

American Wire Gauge (AWG)	Ω/100 Meters Maximum
28	23.20
26	14.60
24	9.09
22	5.74
20	3.58

NOTE: This table is the same as Table 6-6 of the Universal Serial Bus 2.0 Specification.

Example 1. Two 24-gauge (AWG) power or ground wires may be replaced with one 20-gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the USB 2.0 specification at the USB connectors as well as at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure the system passes droop requirements. Cables that provide individual power and ground conductors for each port may usually meet droop requirements by providing adequate capacitance near the motherboard mating connector because droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case, all transients are seen/dampened by the capacitance at the motherboard mating connector before they may cause problems with the adjacent port sharing the same cable. Refer to Section 7.2.2 and 7.2.4.1 of the USB 2.0 specification for more details.

Note: Cables that contain more than two signal pairs are not recommended by Intel due to unpredictable impedance characteristics.

9.7.6.2 Motherboard/PCB Mating Connector

Proper selection of a motherboard mating connector for front panel USB support is important to ensure that signal quality is not adversely affected because of poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the USB 2.0 specification.

9.7.6.2.1 Pin-Out

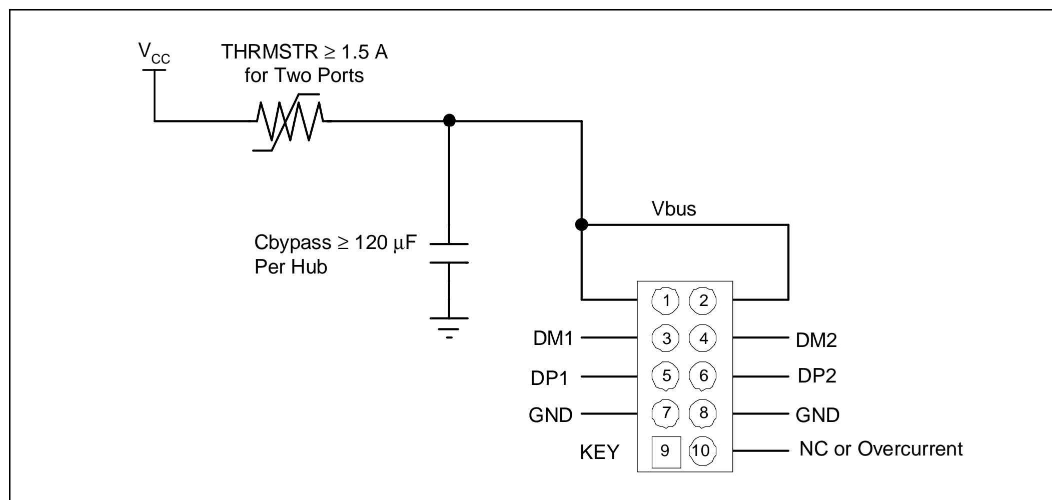
Intel recommends a 10 pin, 0.1-inch pitch stake pin assembly with the pin-out listed in Table 75 and shown in Figure 82.

Table 75. Front Panel Header Pin-Out

Pin	Description
1	V_{CC}
2	V_{CC}
3	dm1
4	dm2
5	dp1
6	dp2
7	Gnd
8	Gnd
9	key
10	No connect or over-current sense

Figure 82 illustrates the front panel header schematic.

Figure 82. Front Panel Header Schematic



Intel recommends that the fuse element (thermistor) for the front panel header be included on the motherboard to protect the motherboard from damage.

- This protects the motherboard from damage in the case where an un-fused front panel cable solution is used.
- It also provides protection from damage if an un-keyed cable is inadvertently plugged onto the front panel USB connector.
- It provides protection to the motherboard in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between Vbus and ground.

9.7.6.2.2 Routing Considerations

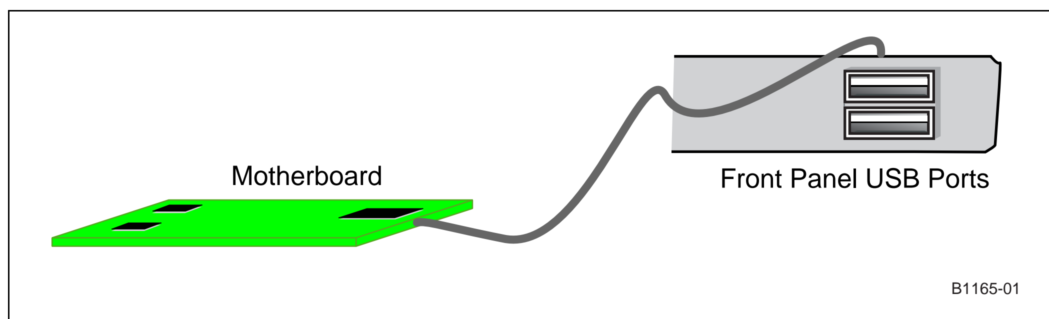
Traces or surface shapes from V_{CC} to the thermistor, to Cbypass and to the connector power and ground pins should be at least 50 mils wide to ensure adequate current carrying capability.

There should be double vias on power and ground nets, and the trace lengths should be kept as short as possible.

9.7.6.3 Front Panel Connector Card

The best way to provide front or side panel support for USB is to use a daughtercard and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they are the most effective. Figure 83 illustrates the major components associated with a typical front/side panel USB solution that uses a front panel connector card.

Figure 83. Motherboard Front Panel USB Support



Note: The terms 'connector card' and 'daughtercard' are used interchangeably.

When designing the motherboard with front/side panel support, the system integrator should know which type of cable assembly should be used. When the system integrator plans to use a connector card, ensure that there are not duplicate EMI/ESD/thermistor components placed on the motherboard because this usually causes drop/droop and signal quality degradation or failure.

9.7.6.3.1 Front Panel daughtercard Design Guidelines

Place the Vbus bypass capacitance, common-mode choke, and ESD suppression components on the daughtercard as close as possible to the connector pins.

Follow the same layout, routing and impedance control guidelines as specified for motherboards.

Minimize the trace length on the front panel connector card. Intel recommends using a trace length less than two inches.

Use the same mating connector pin-out as outlined for the motherboard in Section 9.7.6.2.1. Use the same routing guidelines as described in Section 9.7.1.

Trace length guidelines are presented in Table 73.

9.8 I/O Advanced Programmable Interrupt Controller (IOAPIC)

The ICH4 is designed to be backwards compatible with a number of the legacy interrupt handling mechanisms as well as to be compliant with the latest I/O (x) APIC architecture. In addition to implementing two 8259 interrupt controllers (PIC), the ICH4 also incorporates an Advanced Programmable Interrupt Controller (APIC) that is implemented through the 3-wire serial APIC bus that connects all I/O and local APICs. An advancement in the interrupt delivery and control architecture of the ICH4 is represented by support for the I/O (x) APIC specification where PCI devices deliver interrupts as write cycles that are written directly to a register that represents the desired interrupt. These are ultimately delivered via the serial APIC bus or FSB. Furthermore, on Pentium® M processor/Celeron M processor based systems, the ICH4 has the option to let the integrated I/O APIC behave as an I/O (x) APIC. This allows the ICH4 to deliver interrupts in a parallel manner rather than a serial manner. This is accomplished by I/O APIC writes to a region of memory that is snooped by the processor and thereby knows what interrupt goes active.

On Pentium M/Celeron M processor-based platforms, the serial I/O APIC bus interface of the ICH4 should be disabled. I/O (x) APIC is supported on the platform and the servicing of interrupts is accomplished via a FSB interrupt delivery mechanism.

The serial I/O APIC bus interface of the ICH4 should be disabled as follows.

- Tie APICCLK directly to ground.
- Tie APICD0, APICD1 to ground through a 10 kΩ resistor. (Separate pull-downs are required if using XOR chain testing)

The Pentium M processor/Celeron M processor does not have pins dedicated for a serial I/O APIC bus interface and thus, no hardware change is necessary. However, enabling I/O APIC support in the BIOS and operating system on Pentium M processor/Celeron M processor based systems rather than the legacy 8259 interrupt controller may provide performance benefits and efficiencies that the I/O (x) APIC have over older PIC architecture.

9.8.1 PIRQ Routing Example

Table 76 presents how the ICH4 uses the PCI IRQ when the I/OAPIC is active.

Table 76. I/OAPIC Interrupt Inputs 16 Through 23 Usage

Number	I/OAPIC INTIN PIN	Function in ICH4 using the PCI IRQ in I/OAPIC
1	I/OAPIC INTIN PIN 16 (PIRQA)	USB UHCI Controller #1
2	I/OAPIC INTIN PIN 17 (PIRQB)	AC'97 Audio and Modem; option for SMBus
3	I/OAPIC INTIN PIN 18 (PIRQC)	USB UHCI Controller #3; Native IDE
4	I/OAPIC INTIN PIN 19 (PIRQD)	USB UHCI Controller #2
5	I/OAPIC INTIN PIN 20 (PIRQE)	Internal LAN; option for SCI, TCO, MMT #0,1,2
6	I/OAPIC INTIN PIN 21 (PIRQF)	Option for SCI, TCO, MMT #0,1,2
7	I/OAPIC INTIN PIN 22 (PIRQG)	Option for SCI, TCO, MMT #0,1,2
8	I/OAPIC INTIN PIN 23 (PIRQH)	USB EHCI Controller, Option for SCI, TCO, MMT #0,1,2

Due to different system configurations, IRQ line routing to the PCI slots (swizzling) should be made to minimize the sharing of interrupts between both internal ICH4 functions and PCI functions. Figure 84 illustrates an example of IRQ line routing to the PCI slots

Note: It is not necessarily an optimal routing scheme; an optimal scheme depends on individual system PCI IRQ usage.

Figure 84. Example PIRQ Routing

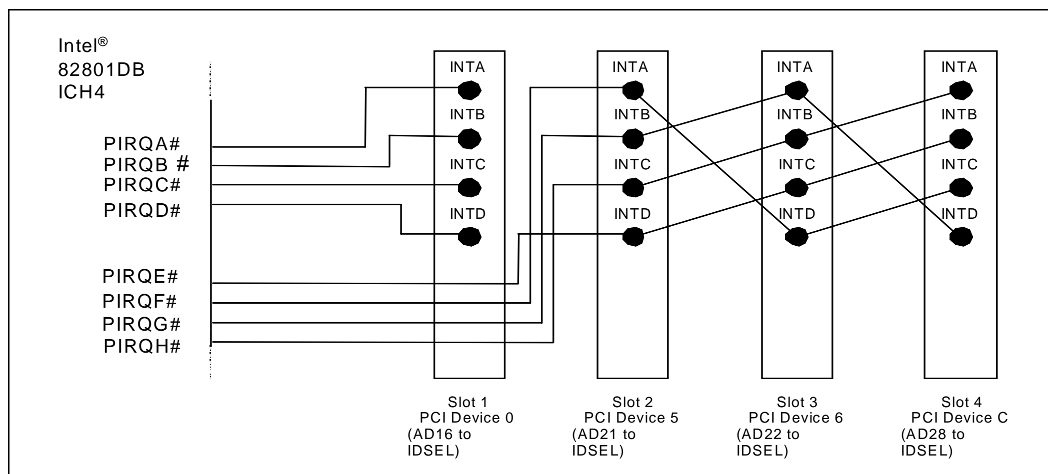


Figure 84 is an example. It is up to the board designer to route these signals in a way that proves the most efficient for their particular system. A PCI slot may be routed to share interrupts with any of the ICH4's internal device/functions (but at a higher latency cost).

9.9 SMBus 2.0/SMLink Interface

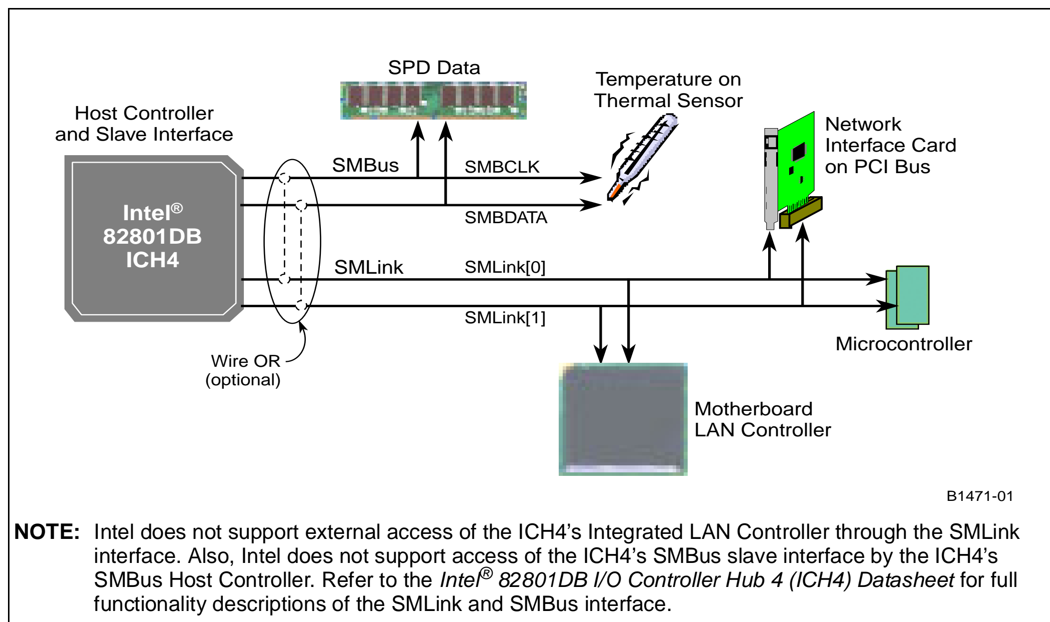
The SMBus interface on the ICH4 uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus host controller. The SMBus host controller resides inside the ICH4.

The ICH4 incorporates an SMLink interface supporting Alert-on-LAN*, Alert-on-LAN2*, and a slave functionality. It uses two signals, SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB slave interface.

For Alert-on-LAN* functionality, the ICH4 transmits heartbeat and event messages over the interface. When using the Intel® 82562EM Platform LAN Connect component, the ICH4's integrated LAN controller claims the SMLink heartbeat and event messages and sends them out over the network. An external, Alert-on-LAN2*-enabled LAN Controller (i.e., Intel 82562EM 10/100 Mbps Platform LAN Connect) connects to the SMLink signals to receive heartbeat and event messages, as well as access the ICH4 SMBus slave interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface may reset or wake a system, generate SMI# or interrupts, and send a message. The slave-read interface may read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus host controller and the SMBus slave interface obey the SMBus 1.0 protocol, so the two interfaces may be externally wire-OR'ed together to allow an external management ASIC (such as Intel 82562EM 10/100 Mbps Platform LAN Connect) to access targets on the SMBus as well as the ICH4 slave interface. Additionally, the ICH4 supports slave functionality, including the host notify protocol, on the SMLink pins. To be fully compliant with the SMBus 2.0 specification (which requires the host notify cycle), the SMLink and SMBus signals **must** be tied together externally. This is done by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA. Figure 85 illustrates SMBUS 2.0/SMLink protocol.

Figure 85. SMBUS 2.0/SMLink Protocol



NOTE: Intel does not support external access of the ICH4's Integrated LAN Controller through the SMLink interface. Also, Intel does not support access of the ICH4's SMBus slave interface by the ICH4's SMBus Host Controller. Refer to the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

9.9.1 SMBus Architecture and Design Considerations

9.9.1.1 SMBus Design Considerations

There is not a single SMBus design solution that works for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging because they add so much capacitance to the bus. This extra capacitance has a large effect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

1. Device class (high/low power). Most designs use primarily high power devices.
2. Are there devices that must run in S3?
3. Amount of $V_{CC_SUSPEND}$ current available, i.e., minimizing load of $V_{CC_SUSPEND}$.

9.9.1.2 General Design Issues/Notes

Regardless of the architecture used, there are some general considerations.

1. The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that may sink the least amount of current is the limiting agent on how small the resistor may be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and fall time specification.
2. The maximum bus capacitance that a physical segment may reach is 400 pF.
3. The ICH4 does not run SMBus cycles while in S3.
4. SMBus devices that may operate in S3 must be powered by the $V_{CC-SUSPEND}$ supply.
5. When SMBus is to be connected to PCI, it must be connected to all PCI slots.

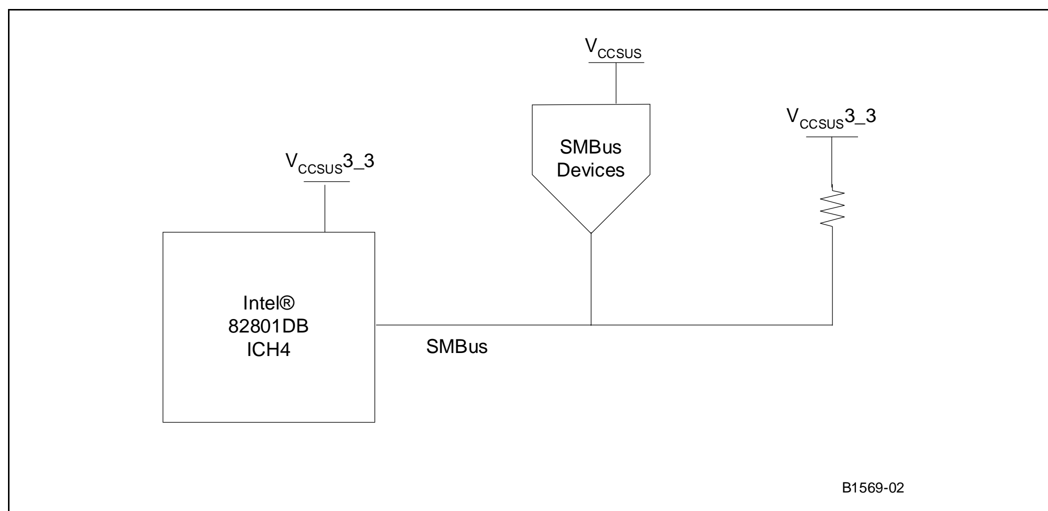
9.9.1.3 Power Supply Considerations

9.9.1.3.1 Unified $V_{CC_SUSPEND}$ Architecture

In this design all SMBus devices are powered by the $V_{CC_SUSPEND}$ supply. Consideration must be made to provide enough $V_{CC_SUSPEND}$ current while in S3.

Figure 86 illustrates the unified $V_{CC_SUSPEND}$ architecture.

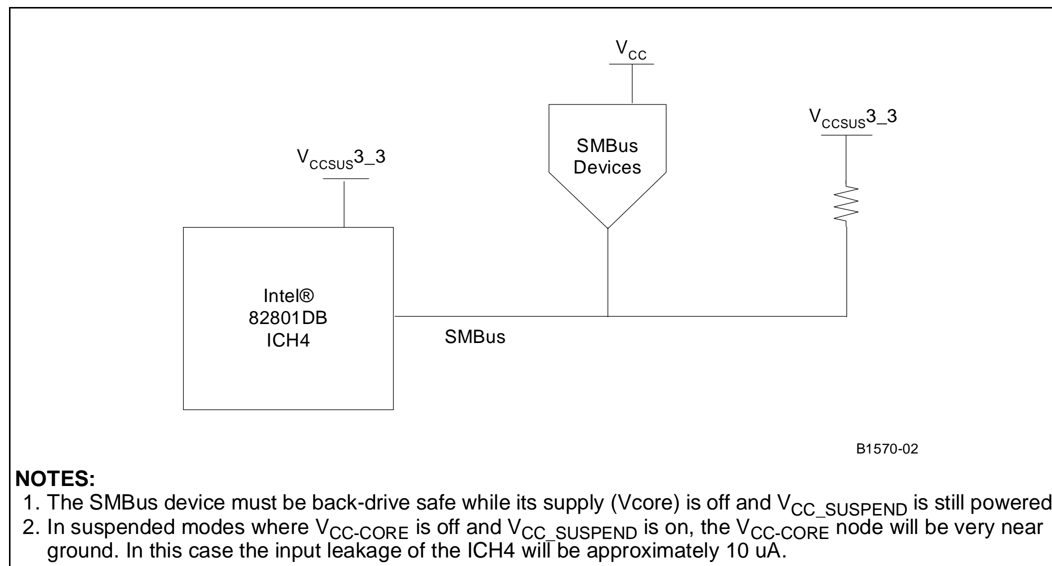
Figure 86. Unified $V_{CC_SUSPEND}$ Architecture



9.9.1.3.2 Unified $V_{CC\text{-}CORE}$ Architecture

In this design, all SMBUS devices are powered by the $V_{CC\text{-}CORE}$ supply. This architecture allows none of the devices to operate in S3, but minimizes the load on $V_{CC_SUSPEND}$. Figure 87 illustrates the unified $V_{CC\text{-}CORE}$ architecture.

Figure 87. Unified $V_{CC\text{-}CORE}$ Architecture

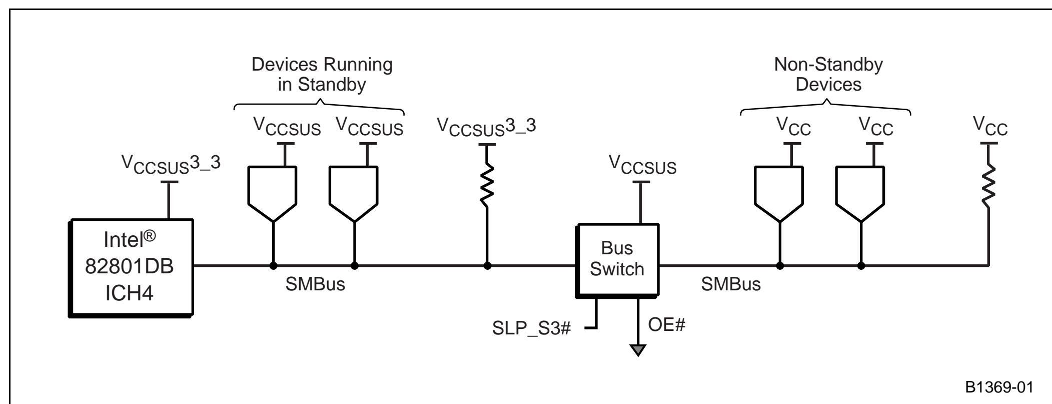


NOTES:
1. The SMBus device must be back-drive safe while its supply (Vcore) is off and $V_{CC_SUSPEND}$ is still powered.
2. In suspended modes where $V_{CC\text{-}CORE}$ is off and $V_{CC_SUSPEND}$ is on, the $V_{CC\text{-}CORE}$ node will be very near ground. In this case the input leakage of the ICH4 will be approximately 10 uA.

9.9.1.3.3 Mixed Power Supply Architecture

This design allows for SMBus devices to communicate while in S3, yet minimizes $V_{CC_SUSPEND}$ leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a bus switch to isolate the devices powered by the core and suspend supplies. Figure 88 illustrates the mixed $V_{CC_SUSPEND}$/$V_{CC\text{-}CORE}$ architecture.

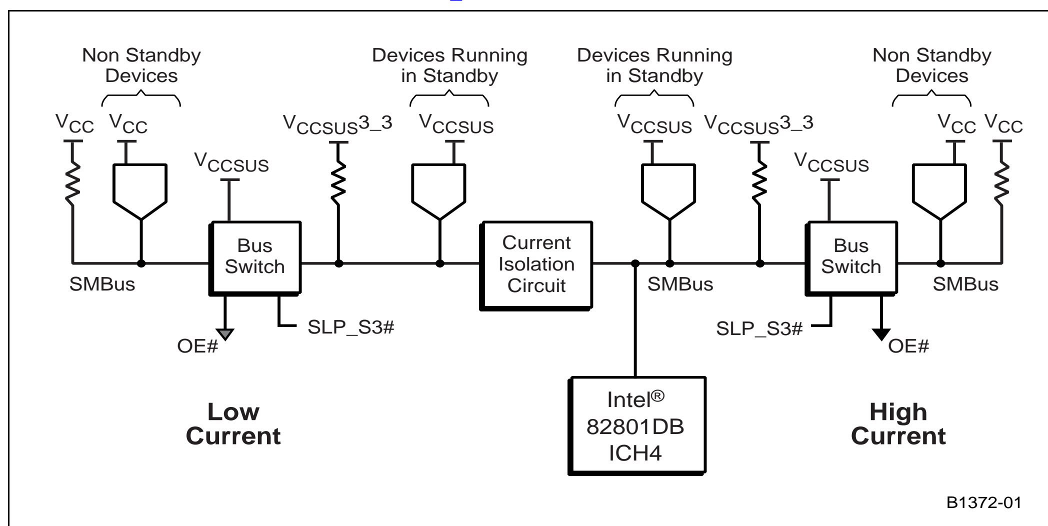
Figure 88. Mixed $V_{CC_SUSPEND}$/$V_{CC\text{-}CORE}$ Architecture



9.9.1.4 Device Class Considerations

In addition to the power supply considerations described above, system designers should take into consideration the SMBus device class (high power/low power) used on the bus. When the design supports both high- power and low-power devices on the bus, current isolation of high-power segment and low-power segment of the bus is needed as shown in Figure 89.

Figure 89. High Power/Low Power Mixed $V_{CC_SUSPEND}/V_{CC\text{-}CORE}$ Architecture



9.10 FWH

The following sections provide general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes may be incorporated in the BIOS. Refer to the *FWH BIOS Specification* or equivalent.

9.10.1 FWH Decoupling

A 0.1 µF capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pins to decouple high-frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pins to decouple low-frequency noise. The capacitors should be placed no further than 390 mils from the V_{CC} supply pins.

9.10.2 In-Circuit FWH Programming

All cycles destined for the FWH appear on PCI. The ICH4 hub interface to PCI bridge puts all CPU boot cycles out on PCI (before sending them out on the FWH interface). When the ICH4 is set for subtractive decode, these boot cycles may be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. To boot from a PCI card, it is necessary to keep the ICH4 in subtractive decode mode. When a PCI boot card is inserted and the ICH4 is programmed for positive decode, there are two devices positively decoding the same cycle.

9.10.3 FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the ICH4 INIT# signal needs to be at a value slightly higher than the VIH min FWH INIT# pin specification. The inactive state of this signal is typically governed by the formula V_CPU_IO(min) - noise margin. Therefore if the V_CPU_IO(min) of the processor is 1.60 V, the noise margin is 200 mV and the VIH min spec of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because 1.6 V - 0.2 V = 1.40 V, which is greater than the 1.35 V minimum of the FWH. When the VIH min of the FWH was 1.45 V, there would be an incompatibility and logic translation would need to be used. The examples above do not take into account any noise that may be encountered on the INIT# signal. Care must be taken to ensure that the VIH min specification is met with ample noise margin. In applications where it is necessary to use translation logic, refer to Section 4.1.5.7.

The solution assumes that level translation is necessary. Figure 17 in Section 4.1.5.6 implements a solution for the ICH4 FWH signal INIT#. Trace lengths and resistor values may be found in Section 4.1.5.6. The Voltage Translator circuitry is shown in Section 4.1.5.7. Intel recommends that any system that implements a FWH should have its INIT# input connected to the ICH4.

9.10.4 FWH INIT# Assertion/Deassertion Timings

Due to the large routing solution space and necessity of a voltage translator in the design of a FWH on Pentium M processor and ICH4 based platforms, the following timing requirements must be met to ensure proper system operation.

For INIT# assertion timings, a conservative analysis of the worst case signal propagation times shows that no timing concerns exist because the ICH4 asserts INIT# for 16 PCI clocks (485 ns) before deasserting. This provides adequate time for INIT# to propagate to both the Pentium M processor and FWH.

For the INIT# deassertion event, the critical timing is the minimum period of time before the Pentium M processor is ready to begin fetching code from the FWH after the INIT#-based reset begins. This minimum period is conservatively set at one CPU clock (10 ns). This also represents the maximum allowed propagation time for the INIT# signal from the ICH4 to the FWH.

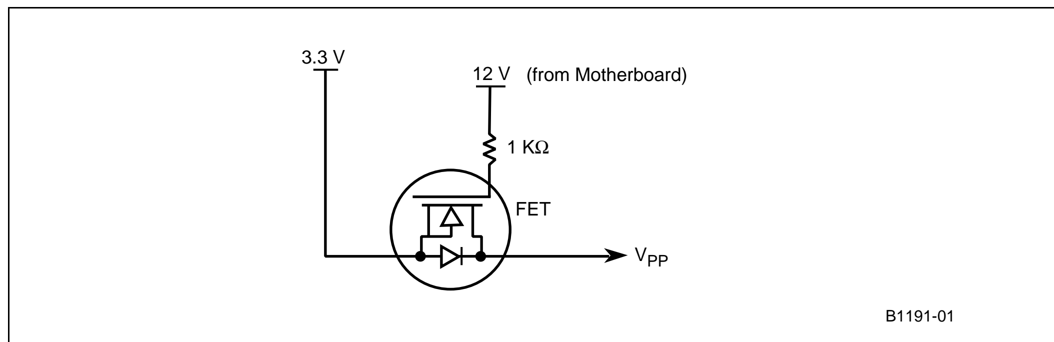
Systems that use alternative devices (i.e., not a FWH) to store the firmware may or may not require the use of INIT#. When INIT# is not used, an analysis should be done to ensure there is no negative impact to system operation. When INIT# is implemented on such a device, voltage translation may be necessary, and the assertion/deassertion timings noted above still apply.

9.10.5 FWH V_{PP} Design Guidelines

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports V_{PP} of 3.3 V or 12 V. When V_{PP} is 12 V, the flash cells program about 50 percent faster than at 3.3 V. However, the FWH supports only 12 V on V_{PP} for 80 hours (3.3 V on Vpp does not affect the life of the device). The 12 V on V_{PP} would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The V_{PP} pin MUST be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. To decrease programming time, it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit allows testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation. Figure 90 illustrates the FWH V_{PP} isolation circuitry.

Figure 90. FWH V_{PP} Isolation Circuitry

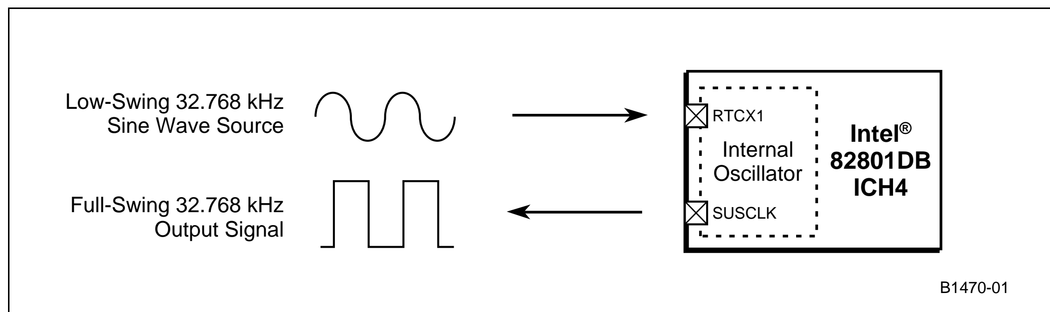


9.11 RTC

The ICH4 contains a real-time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH4 uses a crystal circuit to generate a low-swing, 32 KHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH4, the RTCX1 signal is amplified to drive internal logic as well as generate a free-running, full swing clock output for system use. This output ball of the ICH4 is called SUSCLK as shown in Figure 91.

Figure 91. RTCX1 and SUSCLK Relationship in the Intel® 82801DB I/O Controller Hub 4 (ICH4)

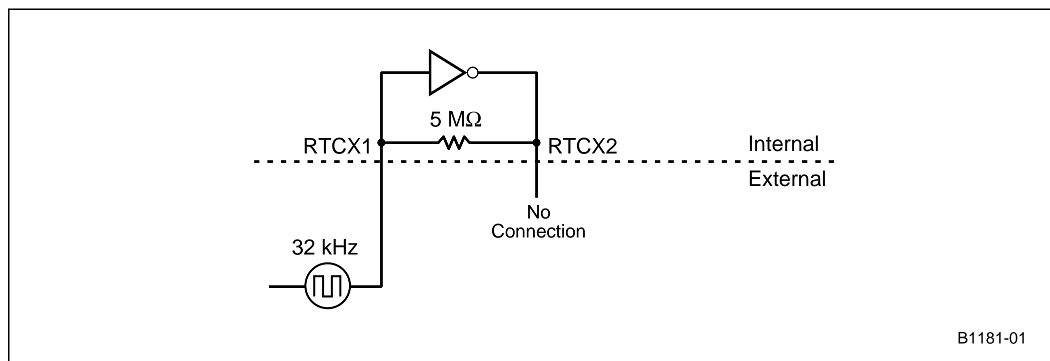


For further information on the RTC, consult *ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions (Application Note AP-728)*. This application note is valid for the ICH4.

Even if the ICH4 internal RTC is not used, it is still necessary to supply a clock input to RTCX1 of the ICH4 because other signals are gated off that clock in suspend modes. However, in this case the frequency accuracy (32.768 KHz) of the clock inputs is not critical; an inexpensive crystal may be used or a single clock input may be driven into RTCX1with RTCX2 left as no connect. Figure 92 illustrates the external circuitry for the ICH4 where the internal RTC is not used.

Note: This is not a validated feature on the ICH4. The peak-to-peak swing on RTCX1 cannot exceed 1.0 V.

Figure 92. External Circuitry for the Intel® 82801DB I/O Communications Hub 4 (ICH4) Where the Internal RTC is Not Used



9.11.1 RTC Crystal

The ICH4 RTC module requires an external oscillating source of 32.768 KHz connected on the RTCX1 and RTCX2 balls. Figure 93 illustrates the external circuitry that comprises the oscillator of the ICH4 RTC.

Figure 93. External Circuitry for the Intel® 82801DB I/O Controller Hub 4 (ICH4) RTC

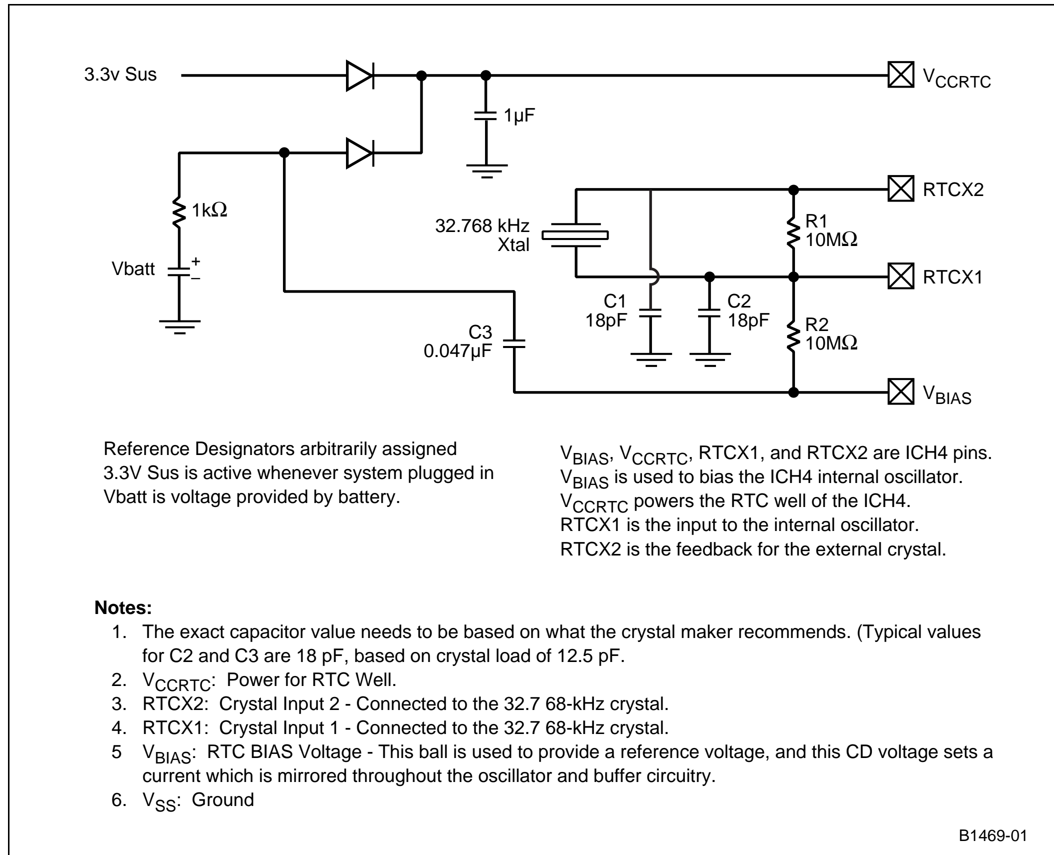


Table 77 presents the RTC routing summary.

Table 77. RTC Routing Summary

RTC Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R1, R2, C1, and C2 Tolerances	Signal Referencing
5 mil trace width (results in ~2 pF per inch)	1 inch	NA	R1 = R2 = 10 MΩ ±5% C1 = C2 = (NPO class) Refer to Section 9.11.2 for calculating a specific capacitance value for C1 and C2.	Ground

9.11.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C_3 needs to be 0.047 µF and capacitor values C_1 and C_2 should be chosen to provide the manufacturer's specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. Equation 1 may be used to choose the external capacitance values.

Equation 1. External Capacitance Values

$$C_{load} = [(C_1 + C_{in1} + C_{trace1}) * (C_2 + C_{in2} + C_{trace2})]/C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2} + C_{parasitic}$$

where:

- C_{load} = Crystal's load capacitance. This value may be obtained from Crystal's specification.
- C_{in1} and C_{in2} = Input capacitances at RTCX1, RTCX2 balls of the ICH4. These values may be obtained in the ICH4's datasheet.
- C_{trace1} and C_{trace2} = Trace length capacitances measured from crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. A typical value, based on a 5-mil wide trace and a ½ ounce copper pour, is approximately equal to:
  C_{trace} = trace length * 2 pF/inch
- $C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the existence of two electrode plates and the dielectric constant of the crystal blank inside the crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C_1 and C_2 may be chosen such that $C_1 = C_2$. Using the equation of C_{load} above, the value of C_1 and C_2 may be calculated to give the best accuracy (closest to 32.768 KHz) of the RTC circuit at room temperature. However, C_2 may be chosen such that $C_2 > C_1$. Then C_1 may be trimmed to obtain the 32.768 KHz.

In certain conditions, both C_1 and C_2 values may be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 KHz. When C_1 and C_2 values are smaller then the theoretical values, the RTC oscillation frequency are higher.

Example 2 (below) demonstrates the use of the practical values C_1 and C_2 in the case that theoretical values cannot ensure the accuracy of the RTC in low temperature condition.

Example 2. Use of Practical Values for C_1 and C_2

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH4, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25° C) to yield a 32.768 KHz oscillation.

At 0° C the frequency stability of crystal gives – 23 ppm (assumed that the circuit has 0 ppm at 25° C). This makes the RTC circuit oscillate at 32.767246 KHz instead of 32.768 KHz.

When the values of C_1 and C_2 are chosen to be 6.8 pF instead of 10 pF, the RTC oscillates at a higher frequency at room temperature (+23 ppm), but this configuration of C_1 and C_2 makes the circuit oscillate closer to 32.768 KHz at 0° C. The 6.8 pF value of C1 and C2 is the **practical value**.

Note: The temperature dependency of crystal frequency is a parabolic relationship (ppm/degree square). The effect of changing the crystal's frequency when operating at 0° C (25° C below room temperature) is the same when operating at 50° C (25° C above room temperature).

9.11.3 RTC Layout Considerations

Since the RTC circuit is very sensitive and requires high accuracy oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

1. Reduce trace capacitance by minimizing the RTC trace length. The ICH4 requires a trace length less than one inch on each branch (from crystal's terminal to RTCXn ball). Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR-4, a 5 mil trace has approximately 2 pF per inch.
2. Trace signal coupling must be limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2, and V_{BIAS}.
3. Intel recommends a ground guard plane.
4. The oscillator V_{CC} should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

9.11.4 RTC External Battery Connections

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH4 is not powered by the system.

Example batteries are Duracell* 2032, 2025, or 2016 (or equivalent), which may give many years of operation. Batteries are rated by storage capacity. The battery life may be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 5 µA, the battery life may be at least:

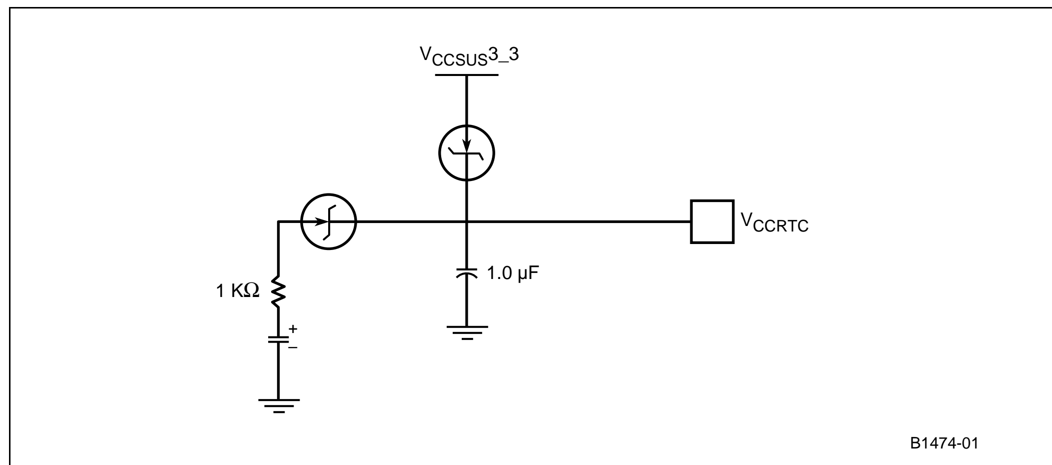
170,000 µAh/5 µA = 34,000 h = 3.9 years

The voltage of the battery may affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy may be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH4 through a Schottky diode circuit for isolation. The Schottky diode circuit allows the ICH4 RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available.

Figure 94 illustrates an example of a diode circuit that is used.

Figure 94. Diode Circuit to Connect RTC External Battery

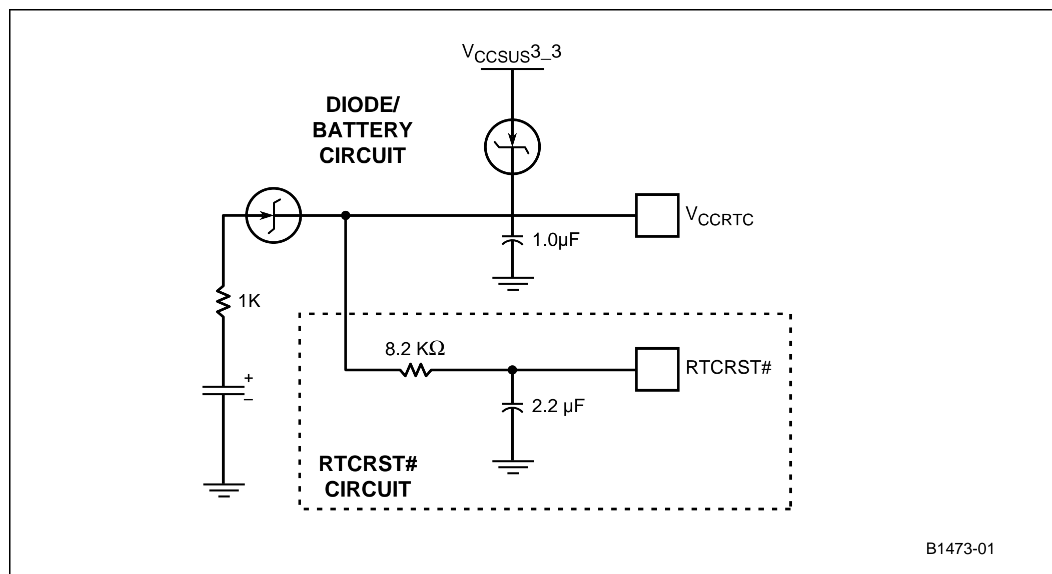


A standby power supply should be used in a mobile system to provide continuous power to the RTC when available, which significantly increases the RTC battery life and thereby the RTC accuracy.

9.11.5 RTC External RTCRST# Circuit

Figure 95 illustrates the RTCRST# external circuit for the ICH4 RTC.

Figure 95. RTCRST# External Circuit for the Intel® 82801DB I/O Controller Hub 4 (ICH4) RTC



The ICH4 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (V_{BATT}) were selected to create an RC time delay, such that RTCRST# may go high some time after the battery voltage is valid. The RC time delay should be in the range of

18 ms - 25 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 94) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 95 is an example of this circuitry that is used in conjunction with the external diode circuit.

9.11.6 V_{BIAS} DC Voltage and Noise Measurements

V_{BIAS} is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC network of R2 and C3 (see Figure 93). Therefore, it is a self-adjusting voltage. Board designers should not manually bias the voltage level on V_{BIAS}. Checking V_{BIAS} level is used for testing purposes only to determine the right bias condition of the RTC circuit.

V_{BIAS} should be at least 200 mV DC. The RC network of R2 and C3 filters out most of AC signal noise that exists on this ball. However, the noise on this ball should be minimized to ensure the stability of the RTC oscillation.

Probing V_{BIAS} requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). Refer to Application Note AP-728 for further details on measuring techniques.

Note: V_{BIAS} is also very sensitive to environmental conditions.

9.11.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle may be between 30-70 percent. When the SUSCLK duty cycle is beyond the 30-70 percent range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK may be probed directly using normal probe (50 Ω input impedance probe) and it is an appropriated signal to check the RTC frequency to determine the accuracy of the ICH4's RTC. Refer to Application Note AP-728 for further details.

9.11.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to V_{CCRTC} or pulled-down to ground while in the G3 state. RTCRST# when configured as shown in Figure 95 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to V_{CCRTC}. This may prevent these nodes from floating in G3, and correspondingly prevents I_{CCRTC} leakage that may cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

9.12 Internal LAN Layout Guidelines

The ICH4 provides several options for LAN capability. The platform supports several components depending upon the target market. Available LAN components include the Intel® 82562ET, and Intel® 82562EM Platform LAN Connect components. Table 78 presents the LAN component connections and features.

Table 78. LAN Component Connections/Features

LAN Component	Interface to ICH4	Connection	Features
Intel® 82562EM (48-Pin SSOP)	LCI	Advanced 10/100 Ethernet	Ethernet 10/100 connection, Alert on LAN* (AoL)
Intel® 82562ET (48-Pin SSOP)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

Design guidelines are provided for each required interface and connection. Figure 96 illustrates the ICH4/Platform LAN Connect section.

Figure 96. Intel® 82801DB I/O Controller Hub 4 (ICH4)/Platform LAN Connect Section

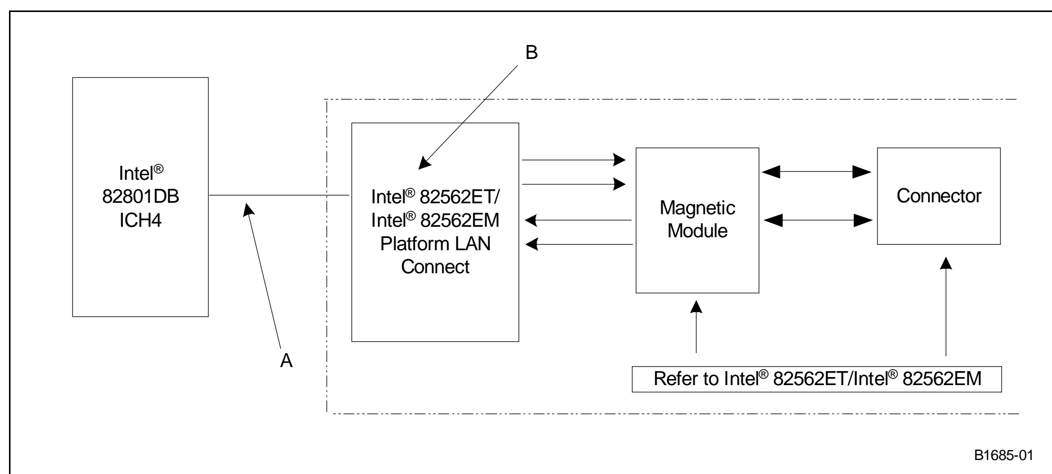


Table 79 presents the LAN design guide section reference.

Table 79. LAN Design Guide Section Reference

Layout Section	Reference	Design Guide Section
ICH4 – LAN Connect Interface (LCI)	A	Refer to Section 9.12.1 for more information.
Intel® 82562ET/Intel® 82562EM Platform LAN Connect	B	Refer to Section 9.12.2 for more information.

9.12.1 ICH4 – LAN Connect Interface Guidelines

This section contains guidelines on how to implement a Platform LAN Connect device on a system motherboard. It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH4 to LAN Connect Interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports Intel® 82562ET and Intel® 82562EM Platform LAN Connect components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by all components. The AC characteristics for this interface are found in the *Intel® I/O Controller Hub (ICH4) Datasheet*.

9.12.1.1 Bus Topologies

The Platform LAN Connect Interface may be configured in several topologies:

- Direct point-to-point connection between the ICH4 and the LAN component
- LOM/CNR Implementation
- LOM (LAN On Motherboard) Point-To-Point Interconnect

The following are guidelines for a single solution motherboard. Either Intel 82562EM, Intel 82562ET or CNR are uniquely installed. Figure 97 illustrates the single source interconnect.

Figure 97. Single Solution Interconnect

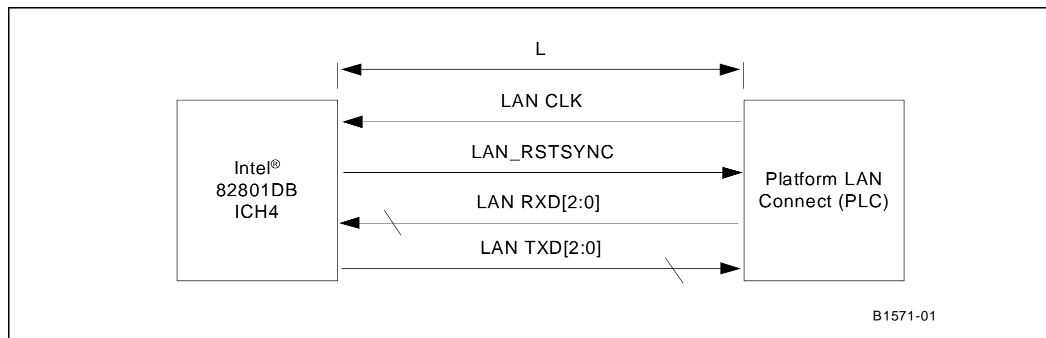


Table 80 presents the LAN LOM routing summary.

Table 80. LAN LOM Routing Summary

LAN Routing Requirements	Maximum Trace Length		Signal Referencing	LAN Signal Length Matching
5 on 10	Intel® 82562ET/EM Platform LAN Connect component	4.5 – 12 inches	Ground	Data signals must be equal to or no more than 0.5 inch (500 mils) shorter than the LAN clock trace.
	Intel® 82562ET/EM Platform LAN Connect component on CNR	2 – 9.5 inches		

9.12.1.1.1 LOM (LAN on Motherboard) and CNR Interconnect

The following guidelines apply to an all-inclusive configuration of PLC design. This layout combines LAN on motherboard and CNR solutions. The resistor pack ensures that either a CNR option or LAN on motherboard option may be implemented at one time. Figure 98 illustrates the LOM/LCNR interconnect. Table 81 presents the LAN LOM/CNR dual routing summary.

Figure 98. LOM/CNR Interconnect

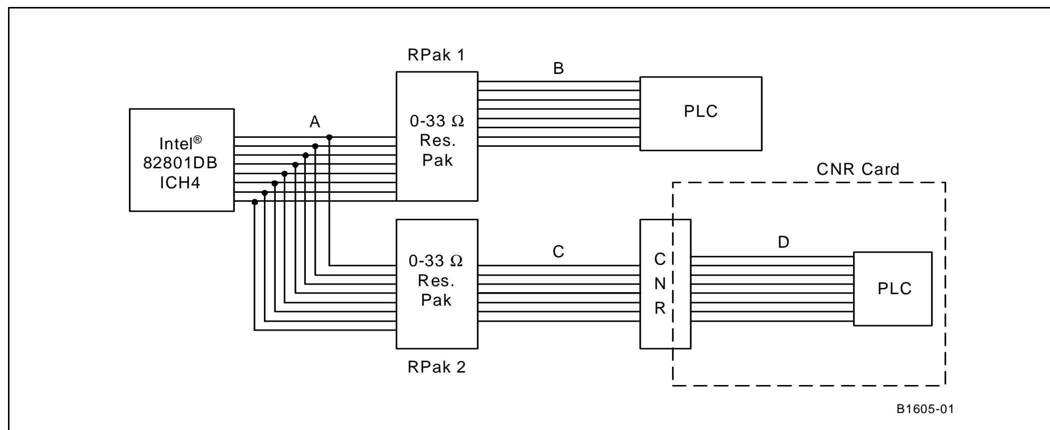


Table 81. LAN LOM/CNR Dual Routing Summary

LAN Routing Requirements	LAN Component	Maximum Trace Length				Signal Reference	LAN Signal Length Matching
		A	B	C	D		
5 on 10	**Intel® 82562ET/EM Platform LAN Connect**	0.5 to 7.5 inches	4 inches to (11.5 inches – A)	NA	NA	Ground	Data signals must be equal to or no more than 0.5 inch (500 mils) shorter than the LAN clock trace.
	Intel® 82562ET/EM Platform LAN Connect on CNR†	0.5 to 7.5 inches	NA	1.5 inches to (9 inches – A)	0.5 to 3 inches		

† Total trace length should not exceed 9.5 inches.

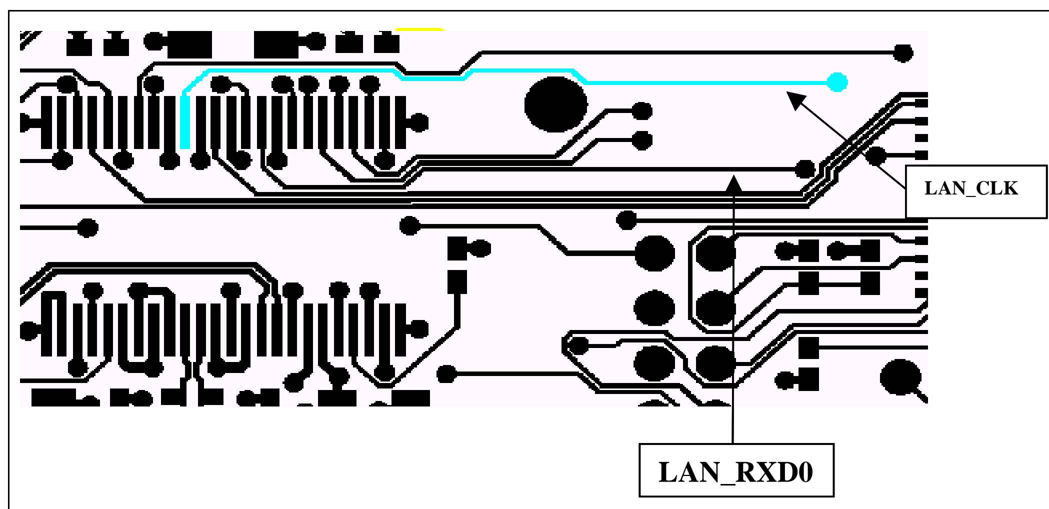
The following are additional guidelines for this configuration:

- Stubs due to the resistor pack should not be present on the surface.
- The resistor pack value may be 0 Ω to 33 Ω.

9.12.1.2 Signal Routing and Layout

Platform LAN connect interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines. Intel recommends that the board designer simulate the board routing to verify that specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard, the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inch shorter than the LAN_CLK trace. LAN_CLK should always be the longest motherboard trace in each group. Figure 99 illustrates the LAN_CLK routing example.

Figure 99. LAN_CLK Routing Example



9.12.1.3 Crosstalk Consideration

Noise due to crosstalk must be minimized. Crosstalk is the key cause of timing skews and is the largest part of the t_{RMATCH} skew parameter. The sum of the trace length mismatch between LAN_CLK and the LAN data signals is t_{RMATCH}. To meet this requirement on the board, the length of each data trace must be either equal to or up to 0.5 inch shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize crosstalk noise from non-PLC signals.

9.12.1.4 Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard. Intel recommends using an impedance of 55 Ω ± 15%. Otherwise, signal integrity requirements may be violated.

9.12.1.5 Line Termination

Line termination mechanisms are not specified for the LAN Connect Interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 0 Ω to 33 Ω series resistor may be installed at the driver side of the interface should the developer have concerns about over/undershoot.

Note: The receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

9.12.1.6 Disabling the ICH4 Integrated LAN

The LAN Connect Interface on the ICH4 may be left as a no-connect if it is not used.

9.12.2 Intel® 82562ET/Intel® 82562EM Platform LAN Connect Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 9.12.1. Additional guidelines for implementing an Intel® 82562ET or Intel® 82562EM Platform LAN Connect component are provided below.

9.12.2.1 Guidelines for Intel 82562ET/Intel 82562EM Platform LAN Connect Component Placement

Component placement may affect signal quality, emissions, and temperature of a board design. This section provides guidelines for component placement.

Careful component placement may:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation affects the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. It is imperative that all designs be optimized to fit in a very small space.

9.12.2.2 Crystals and Oscillators

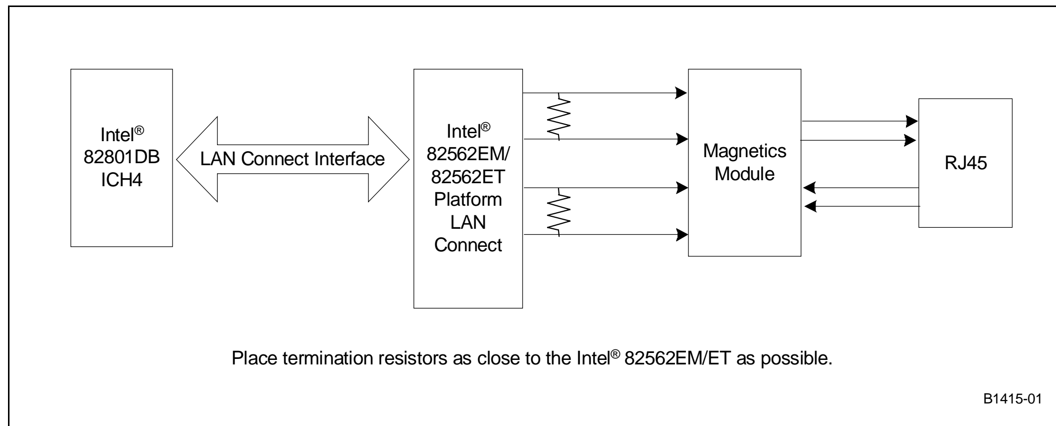
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they exist) should be grounded to prevent the possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discrete components as close as possible to the Intel 82562ET/ Intel EM Platform LAN Connect component, keeping the trace length as short as possible and do not route any noisy signals in this area.

9.12.2.3 Intel 82562ET/Intel 82562EM Platform LAN Connect Termination Resistors

The 100 Ω ±1% resistor used to terminate the differential transmit pairs (TDP/TDN) and the 121 Ω ±1% receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN connect component (Intel 82562ET or Intel 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e., Intel 82562ET), including the wire impedance reflected through the transformer. Figure 100 illustrates the Intel® 82562ET/Intel® 82562EM platform LAN connect termination.

Figure 100. Intel® 82562ET/Intel® 82562EM Platform LAN Connect Termination



9.12.2.4 Critical Dimensions

There are two dimensions to consider during layout: distance 'A' from the line RJ-45 connector to the magnetics module and distance 'B' from the Intel® 82562ET or Intel® 82562EM to the magnetics module. The combined total distances A and B must not exceed four inches (preferably, less than two inches). Figure 101 illustrates the critical dimensions for component placement.

Figure 101. Critical Dimensions for Component Placement

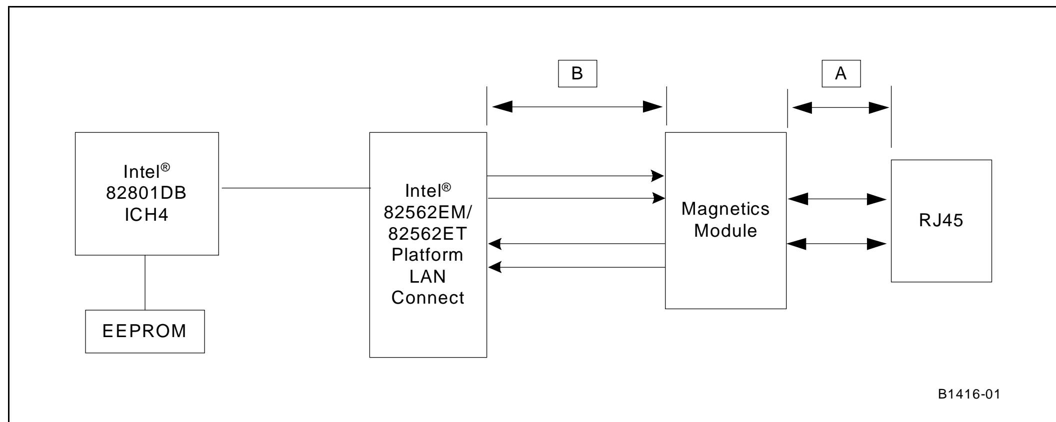


Table 82 presents the critical dimensions for component placement.

Table 82. Critical Dimension Guidelines for Component Placement (for Figure 101)

Distance	Priority	Guideline
A	1	<1 inch
B	2	<1 inch

9.12.2.4.1 Distance from Magnetics Module to RJ-45 (Distance A)

The distance A in Figure 101 above should be given the highest priority in board layout. The distance between the magnetics module and the RJ-45 connector should be kept to less than one inch of separation. Observe the following trace characteristics:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance is approximately 55 Ω; however, the differential impedance may also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This may degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. When the Intel® 82562ET must be placed further than a couple of inches from the RJ-45 connector, distance B may be sacrificed. Keeping the total distance between the Intel 82562ET and RJ-45 as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. When the actual impedance is consistently low, a target of 105 Ω to 110 Ω should compensate for second order effects.

9.12.2.4.2 Distance from Intel 82562ET to Magnetics Module (Distance B)

Distance B should be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces intended for use with high-speed signals should observe proper termination practices. Proper termination of signals may reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetrical and equal length within each differential pair.

9.12.2.5 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous ground plane with no interruptions. the signal conductors should not cross any vacant areas on a ground or power plane. This increases inductance and associated radiated noise levels.
- Separate noisy logic grounds from analog signal grounds to reduce coupling. Noisy logic grounds may sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc.

- Connect all ground vias to every ground plane; and similarly, every power via to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds to minimize the loop area between a signal path and its return path.
- Rise and fall times should be as slow as possible because signals with fast rise and fall times contain many high-frequency harmonics that may radiate significantly.
- The most sensitive signal returns closest to the chassis ground should be connected together. This results in a smaller loop area and reduces the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk may be studied using electronics modeling software.

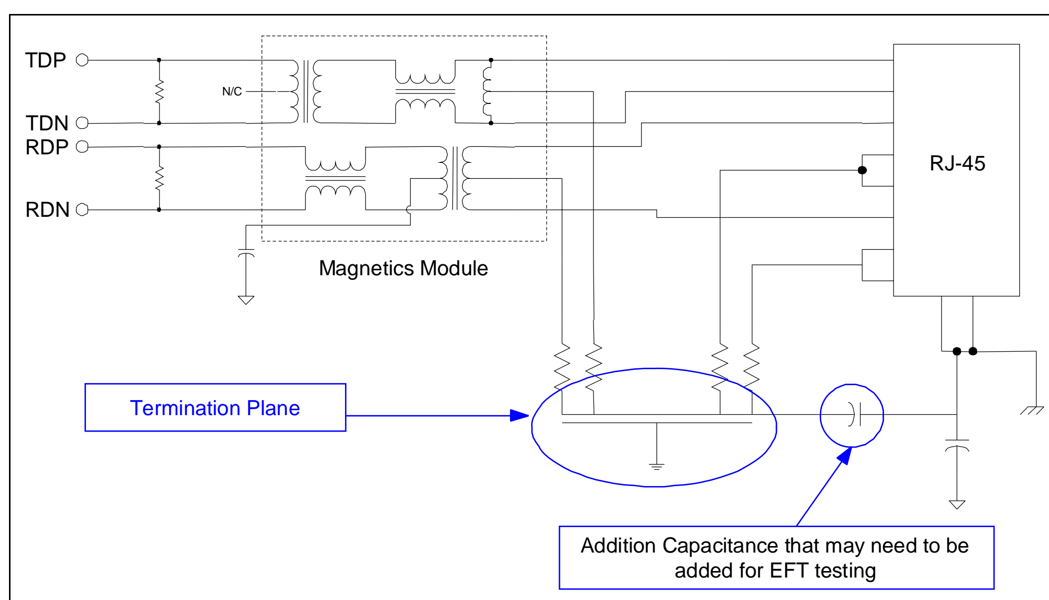
9.12.2.5.1 Terminating Unused Connections

In Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals may be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

9.12.2.5.2 Termination Plane Capacitance

Intel recommends that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ-45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. When a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 VAC. Figure 102 illustrates the termination plane.

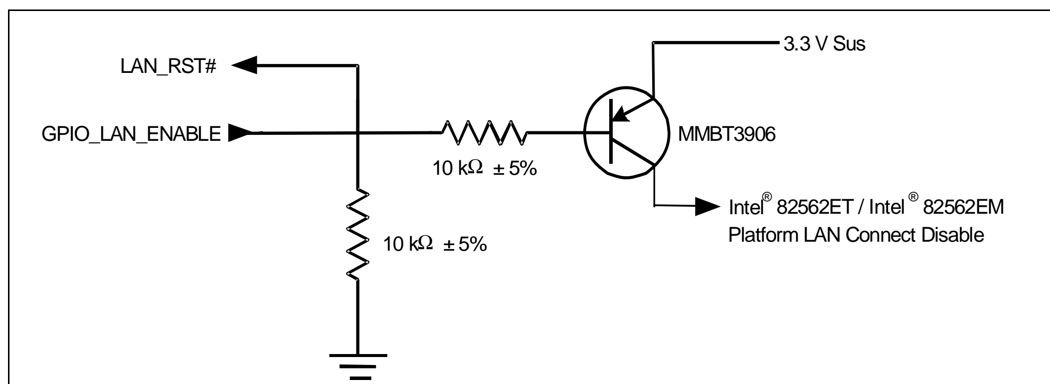
Figure 102. Termination Plane



9.12.3 Intel® 82562ET/ Intel® 82562EM Platform LAN Connect Disable Guidelines

To disable the Intel® 82562ET/ Intel® 82562EM Platform LAN Connect, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28, to be LAN_Enable (enabled high), LAN defaults to enabled on initial power-up and after an AC power loss. This circuit shown below allows this behavior. The BIOS controlling the GPIO may disable the LAN microcontroller. Figure 103 illustrates the Intel 82562ET/EM platform LAN connect disable circuitry.

Figure 103. Intel® 82562ET/EM Platform LAN Connect Disable Circuitry



Four pins are used to put the Intel® 82562ET/ Intel® 82562EM Platform LAN Connect controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 83 describes the operational/disable features for this design.

Configure the four control signals presented in Table 83 as follows: Test_En should be pulled down through a 100 Ω resistor. The remaining three control signals should each be connected through 100 Ω series resistors to the common node ‘Intel 82562ET/EM _Disable’ of the disable circuit.

Table 83. Intel® 82562ET/EM Platform LAN Connect Control Signals

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled with Clock (low power)
1	1	1	1	Disabled without Clock (lowest power)

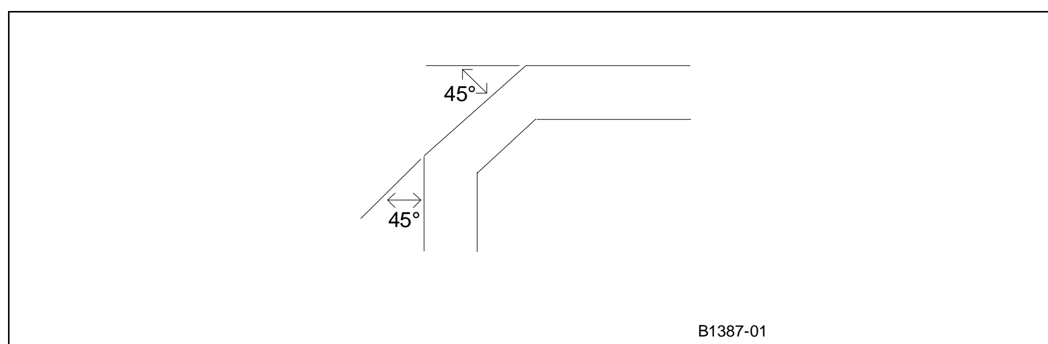
9.12.4 General Intel® 82562ET/ Intel® 82562EM Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Keep signal traces as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance:

Note: Some suggestions are specific to a 4.3 mil stack-up.

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under four inches. Many customer designs with differential traces longer than five inches have had one or more of the following issues: IEEE phy conformance failures, excessive electromagnetic interference (EMI), and/or degraded receive bit error rate (BER).
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (Intel recommends 300 mils).
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, minimize the number of corners and vias. When a 90° bend is required, Intel recommends using two 45° bends instead (see Figure 104).
- Route traces away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This prevents coupling to or from the clock. As a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 104. Trace Routing



9.12.4.1 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace width to trace height above the ground plane. To minimize trace inductance, high-speed signals and signal layers close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance,

the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which may lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils edge to edge.

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. For similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/ edge of the board.

9.12.4.2 Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.

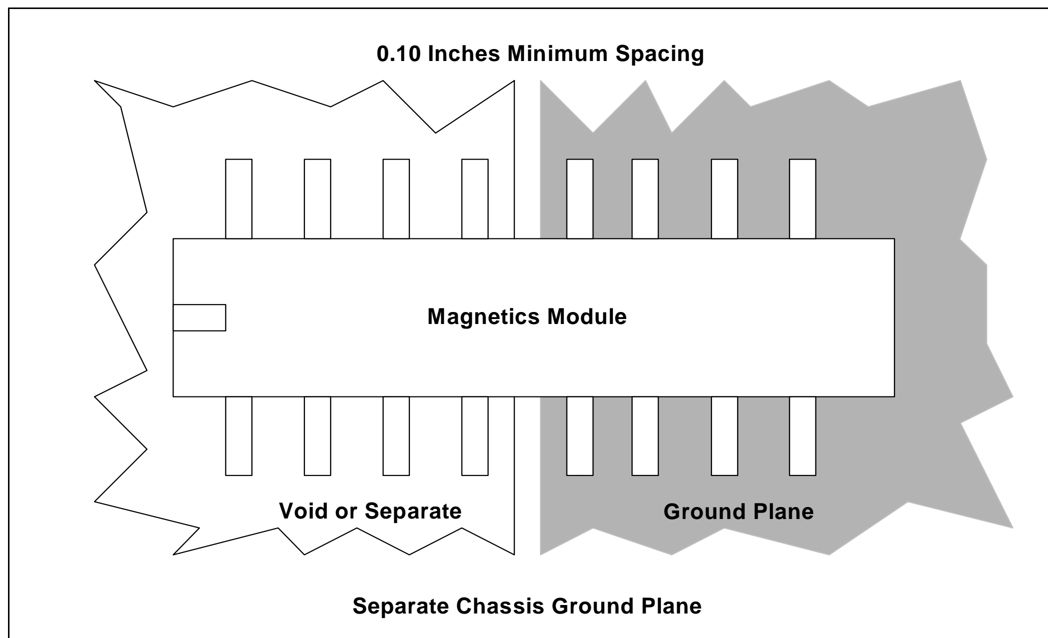
Note: Over the length of the trace run, each differential pair should be at least 0.3 inch away from any parallel signal traces.

- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which may increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

9.12.4.3 Magnetics Module General Power and Ground Plane Considerations

To properly implement the common-mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum. Figure 105 illustrates the ground plane separation.

Figure 105. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small. Power inputs bypassed to signal return significantly reduce EMI radiation.

Some rules to follow that help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions; do not route over a split plane. Avoid routing signals over any vacant areas on a ground or power plane. This increases inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- Connect all ground vias to every ground plane; and connect every power via to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high-frequency harmonics, which may radiate EMI.
- Split the ground plane beneath the filter/transformer module. The RJ-45 connector side of the transformer module should have chassis ground beneath it. Splitting ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer. There should not be a power plane under the magnetics module.

9.12.4.4 Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN On Motherboard designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. For each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC. Asymmetry may create common-mode noise and distort the waveforms.
3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45 connector. Beyond a total distance of about four inches, it may become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) attenuate the analog signals. In addition, any impedance mismatch in the traces is aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (= one inch).
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel causes degraded long cable BER. Crosstalk getting onto the transmit channel may cause excessive emissions (failing FCC) and may cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inch from the differential traces.
5. Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces puts more crosstalk onto the closest receive trace and may greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inch or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45, and the PLC.
6. Use of an inferior magnetics module. The magnetics modules that Intel uses have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
7. Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or Application Note.
8. Not using (or incorrectly using) the termination circuits for the unused pins at RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or term plane. When these are not terminated properly, there may be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The Application Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. Incorrect differential trace impedances. It is important to have ~100 Ω differential impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is common to observe customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they have designed for 100 Ω. (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling may lower the effective differential impedance by 5 Ω- 20 Ω. A 10 Ω to 15 Ω drop in impedance is common. Short traces have fewer problems if the differential impedance is a little off.

10. Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the Intel® 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations may slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This also causes return loss to fail at higher frequencies and degrades the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. When a cap is used, it should be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) These caps are not necessary, unless there is some overshoot in 100 Mbps mode.

It is important to keep the two traces within a differential pair close to each other. Close is considered to be less than 0.030 inch between the two traces within a differential pair. Intel recommends 0.007 inch trace-to-trace spacing. Keeping traces close helps make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces and better receive BER for the receive traces.

9.13 General Purpose Inputs/Outputs (GPIO)

The ICH4 has 12 general purpose inputs, eight general purpose outputs, and 16 general purpose inputs/outputs. Table 84 presents the GPIO configurations.

Table 84. GPIO Configurations (Sheet 1 of 2)

GPIO #	Power Well	Input, Output, I/O	Tolerance	Note
0	Core	Input	5 V	2
1	Core	Input	5 V	2
2	Core	Input	5 V	2
3	Core	Input	5 V	2
4	Core	Input	5 V	2
5	Core	Input	5 V	2
6	Core	Input	5 V	
7	Core	Input	5 V	
8	Resume	Input	3.3 V	
11	Resume	Input	3.3 V	2
12	Resume	Input	3.3 V	
13	Resume	Input	3.3 V	
16	Core	Output	3.3 V	2
17	Core	Output	3.3 V	2
18	Core	Output	3.3 V	
19	Core	Output	3.3 V	
20	Core	Output	3.3 V	
21	Core	Output	3.3 V	
22	Core	Output (Open Drain)	3.3 V	

NOTES:
1. Defaults as an output.
2. May be used as a GPIO if the native function is not needed. ICH4 defaults these signals to native functionality.

Table 84. GPIO Configurations (Sheet 2 of 2)

GPIO #	Power Well	Input, Output, I/O	Tolerance	Note
23	Core	Output	3.3 V	
24	Resume	Input-Output	3.3 V	1
25	Resume	Input-Output	3.3 V	1
27	Resume	Input-Output	3.3 V	1
28	Resume	Input-Output	3.3 V	1
32	Core	Input-Output	3.3 V	1
33	Core	Input-Output	3.3 V	1
34	Core	Input-Output	3.3 V	1
35	Core	Input-Output	3.3 V	1
36	Core	Input-Output	3.3 V	1
37	Core	Input-Output	3.3 V	1
38	Core	Input-Output	3.3 V	1
39	Core	Input-Output	3.3 V	1
40	Core	Input-Output	3.3 V	1
41	Core	Input-Output	3.3 V	1
42	Core	Input-Output	3.3 V	1
43	Core	Input-Output	3.3 V	1

NOTES:
1. Defaults as an output.
2. May be used as a GPIO if the native function is not needed. ICH4 defaults these signals to native functionality.

Miscellaneous Logic 10

The Intel® 82801DB I/O Controller Hub 4 (ICH4) requires additional external circuitry to function properly. Some of these functionalities include meeting timing specifications, buffering signals, and switching between power wells. This logic may be implemented through the use of the Glue Chip or discrete logic.

10.1 Glue Chip 4

To reduce the component count and BOM (Bill of Materials) cost of the ICH4 platform, Intel has developed and ASIC component that integrates miscellaneous platform logic into a single chip. The ICH4 Glue Chip is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost may be reduced.

Features include:

- Dual, strapping, selectable feature sets
- Audio-disable circuit
- Mute audio circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK (PWRGD_3V) signal generation
- Power sequencing/ BACKFEED_CUT
- Power supply turn on circuitry
- RSMRST# generation
- Voltage translation from DDC to VGA monitor
- HSYNC/VSYNC voltage translation to VGA monitor
- Tri-state buffers for test
- Extra GP logic gates
- Power LED drivers
- Flash FLUSH#/INIT# circuit

More information regarding this component is available from the vendors presented in Table 85 on the next page.

Table 85. Glue Chip 4 Vendor Information

Vendor	Contact Information	Vendor Part Number
Philips Semiconductor	http://www.semiconductors.philips.com	PCA9504A
Fujitsu Microelectronics	http://www.fujitsumicro.com	MB87B302ABPD-G-ER

10.2 Discrete Logic

As an alternative solution, discrete circuitry may be implemented into a design instead of using the Glue Chip.

Platform Clock Routing Guidelines 11

11.1 System Clock Groups

The system clocks are considered as a subsystem in themselves. At the center of this subsystem is the clock synthesizer/driver component. Several vendors offer suitable products, as defined in the *Intel CK408 Synthesizer/Driver Specification*. This device provides the set of clocks required to implement a platform-level motherboard solution. Table 86 presents a breakdown of the various individual clocks.

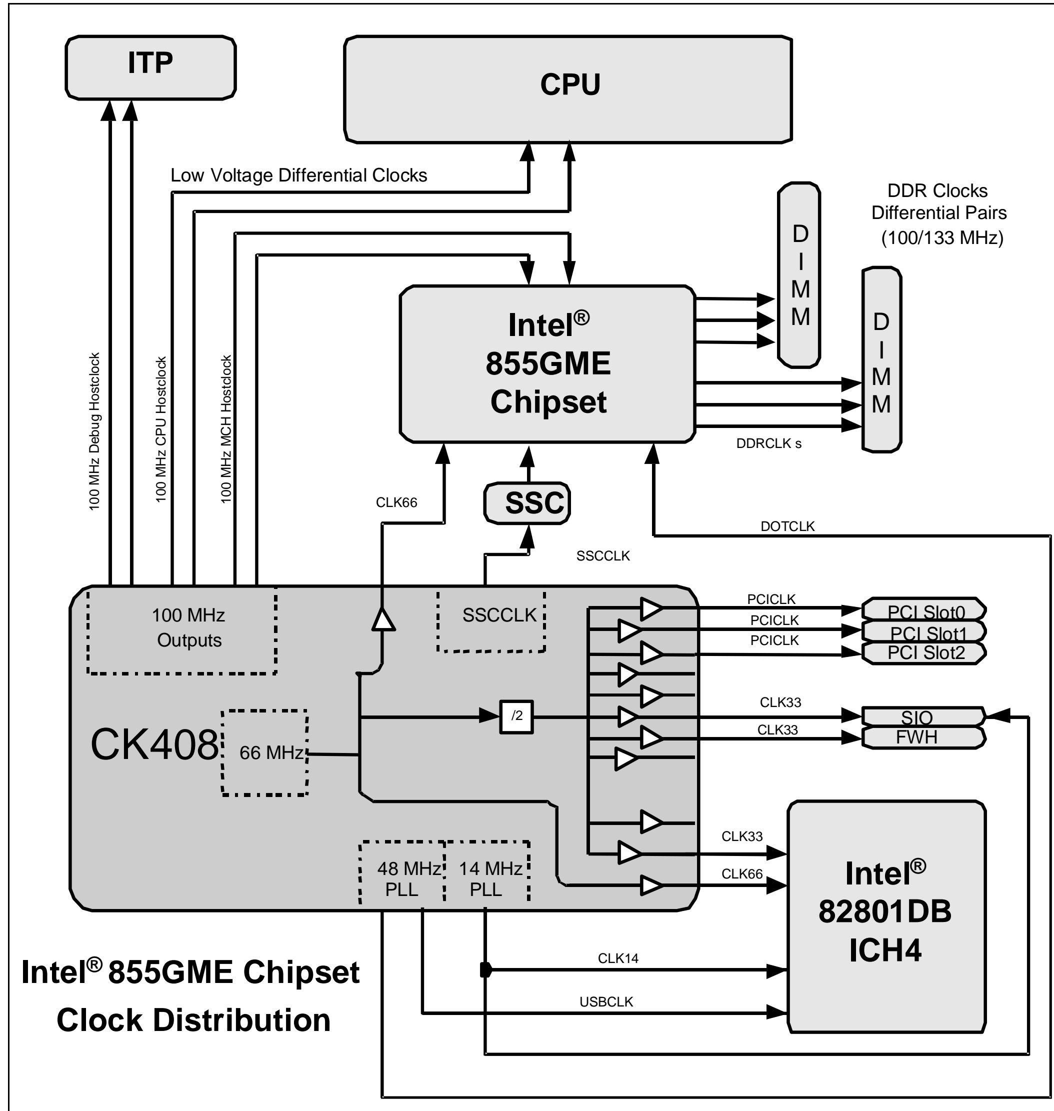
Note: When used in Intel® 855GME chipset platforms, the CK408 is configured in the unbuffered mode and a host clock swing of 710 mV.

Table 86. Individual Clock Breakdown

Clock Group	Frequency	Driver/Pin	Receiver/s	Comments
HOST_CLK	100 MHz	CK408 CPU[2:0]	CPU GMCH Debug Port	Length matched Differential signaling
CLK66	66 MHz	CK408 3V66[5:0]	GMCH Intel® 82801DB I/O Controller Hub 4 (ICH4)	Length matched
CLK33	33 MHz	CK408 PCIF[2:0] PCI[6:0]	ICH4 SIO FWH	Length matched to CLK66 Synchronous but not edge aligned with CLK66 Phase delay of 1.5 ns to 3.5 ns
PCICLK (Expansion)	33 MHz	CK408 PCI[6:0] PCIF[2:0]	PCI Conn #1 PCI Conn #2 PCI Conn #3	Length matched to CLK33 CLK33 length minus 2.5 inches
CLK14	14 MHz	CK408 REF0	ICH4 SIO	Independent clock
DOTCLK	48 MHz	CK408 48 MHz	GMCH	Independent clock
SSCCLK	48/66 MHz	CK408 VCH	GMCH	Independent clock
USBCLK	48 MHz	CK408 48 MHz	ICH4	Independent clock

Figure 106 illustrates the system clock subsystem including the clock generator, major platform components, and all the related clock interconnects.

Figure 106. Clock Distribution Diagram



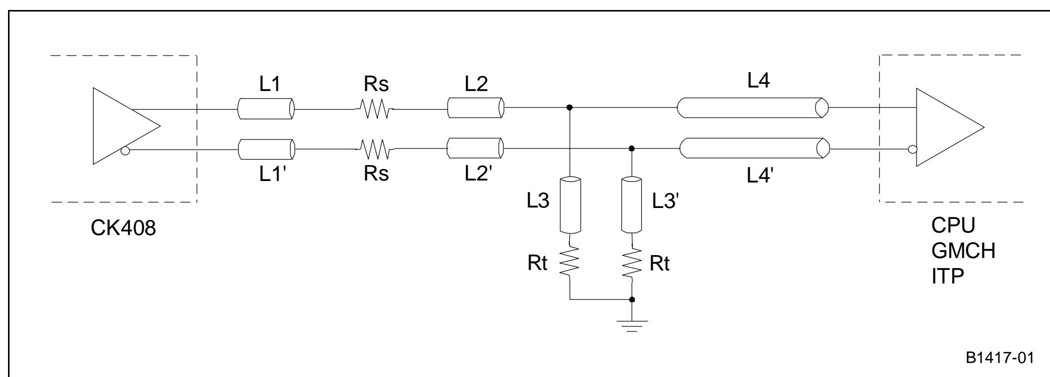
11.2 Clock Group Topologies and Routing Constraints

The topology diagrams and routing constraint tables provided on the following pages define Intel's recommended topology and routing rules for each of the platform level clocks. These topologies and rules have been simulated and verified to produce the required waveform integrity and timing characteristics for reliable platform operation.

11.2.1 Host Clock Group

The clock synthesizer provides three pairs of 100 MHz differential clock outputs using a 0.7 V voltage swing. The 100 MHz differential clocks are driven to the Pentium® M processor, the GMCH, and the processor debug port with the topology shown in Figure 107. The host clocks are routed point-to-point as closely coupled differential pairs on the motherboard, with dedicated buffers for each of the three loads. These clocks utilize a source shunt termination scheme as shown below.

Figure 107. Source Shunt Termination Topology



The clock driver differential bus output structure is a 'Current Mode Current Steering' output which develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt. The resulting amplitude is determined by multiplying I_{OUT} by the value of Rt. The current I_{OUT} is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of Rt to match impedances or to accommodate future load requirements.

Intel's recommended termination for the differential bus clock is a 'Source Shunt termination.' Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

Intel's recommended value for Rt is a 49.9 Ω ± 1% resistor. The tight tolerance is required to minimize crossing voltage variance. The recommended value for Rs is 33 Ω ± 5%. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

The MULT0 pin (CK408 pin #43) should be pulled up through a 10 kΩ to V_{CC} – setting the multiplication factor to six.

The IREF pin (CK408 pin #42) should be tied to ground through a 475 Ω ± 1% resistor – making the IREF 2.32 mA. Table 87 presents the host clock group routing constraints.

Table 87. Host Clock Group Routing Constraints

Parameter	Definition
Class Name	HOST_CLK
Class Type	Individual Differential Pairs
Topology	Differential Source Shunt Terminated
Reference Plane	Ground Referenced (contiguous over length)
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Differential Mode Impedance (Zdiff)	100 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Inner Layer Pair Spacing (edge to edge) (except as allowed below)	7.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Nominal Outer Layer Pair Spacing (edge to edge) (except as allowed below)	5.0 mils
Minimum Spacing to Other Signals	25 mils
Serpentine Spacing	25 mils
Maximum Via Count	5 (per side)
Series Termination Resistor Value	33 Ω ± 5%
Shunt Termination Resistor Value	49.9 Ω ± 1%
Trace Length Limits – L1 & L1’	Up to 500 mils
Trace Length Limits – L2 & L2’	Up to 200 mils
Trace Length Limits – L3 & L3’	Up to 500 mils
Trace Length Limits – L4 & L4’	2 to 8 inches
Total Length Range– L1 + L2 + L4	2 to 8.5 inches
Length Matching Required	Yes (Pin to Pad)
HCLK to HCLK# Length Matching	± 10 mils (per segment) ± 10 mils (overall)
CPU Clock to GMCH Clock Length Matching	Match HCLKs (pin to pad) ± 20 mils Match L1 segment to ± 10 mils across all pairs. Refer to Section 11.2.1.2 for more information.
Breakout Region Exceptions	No breakout exceptions allowed.

NOTES:
1. Differential pairs should be routed as a closely coupled side-by-side pair on a single layer over their entire length.
2. To minimize skew, Intel recommends that all clocks be routed on a single layer. If clock pairs are to be routed on multiple layers, the routed length on each layer should be equalized across all clock pairs.
3. To minimize skew, Intel recommends that all clock pairs be length matched from CK408 pin to CPU and GMCH die-pad, and length compensated on the motherboard for differences in package length and for socket/interposer effective length. A table of package lengths and equivalent socket length is provided.
4. The motherboard length of the ITP connector clock pair should be matched to the motherboard length of the CPU clock pair plus the length of the BPM#[4:0] signals, within ± 50 ps.

11.2.1.1 Host Clock Group General Routing Guidelines

When routing the 100 MHz differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.

If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.

Do not place vias between adjacent complementary clock traces. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

11.2.1.2 Clock-to-Clock Length Matching and Compensation

The HCLK pairs to the CPU and GMCH should be matched as close as possible in total length from CK408 pin to the die-pad of the receiving device. In addition, the L1/L1’ segments of all three clock pairs should be length matched to within ±10 mils. Pair-to-pair overall length matching requires knowledge of the package lengths of various CPUs, and the GMCH, as well as the effective length of the CPU socket/interposer if used.

Once routing lengths are defined for the CPU and GMCH, match the motherboard length of the ITP clock pair to the motherboard length of the CPU clock pair.

Table 88 presents the clock package length.

Table 88. Clock Package Length

Parameter	Length
Pentium® M Processor Package Length	485 mils
Intel® 855GME chipset GMCH Package Length	1142 mils
CPU Socket Equivalent Length	157 mils

11.2.1.3 EMI Constraints

Clocks are a significant contributor to EMI and should be treated with care. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to the VSS reference plane only.

11.2.2 CLK66 Clock Group

The 66 MHz clocks are series terminated and routed point-to-point on the motherboard, with dedicated buffers for each of the loads. These clocks are all length tuned to match each other and the CLK33 clocks. Figure 108 illustrates the CLK66 clock group topology.

Figure 108. CLK66 Clock Group Topology

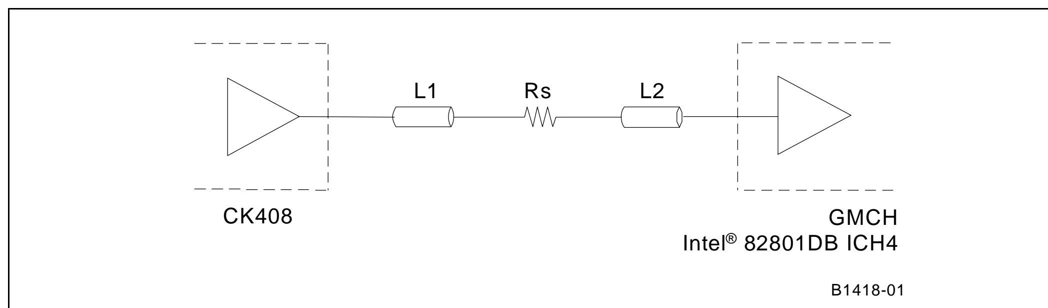


Table 89 presents the CLK66 clock group routing constraints.

Table 89. CLK66 Clock Group Routing Constraints

Parameter	Definition
Class Name	CLK66
Class Type	Individual Nets
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ± 5%
Trace Length Limits – L1	Up to 500 mils (breakout segment)
Trace Length Limits – L2	4 to 8.5 inches
Total Length Range – L1 + L2	4 to 9 inches
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	± 100 mils CLK66 to CLK66
Breakout Region Exceptions. (Reduced spacing for GMCH and ICH breakout region)	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

NOTE: The overall length of CLK66 is considered the reference length for CLK33 and PCICLK. The length of this clock should be set within the range and then used as the basis for defining the length of all other length matched clocks.

11.2.3 CLK33 Clock Group

The 33 MHz clocks are series terminated and routed point-to point on the motherboard with dedicated buffers for each of the loads. These clocks are length tuned to match the CLK66 clocks, however, they are out of phase due to an internal phase delay in the CK408. Figure 109 illustrates the CLK33 group topology. Table 90 presents the CLK33 clock group routing constraints.

Figure 109. CLK33 Group Topology

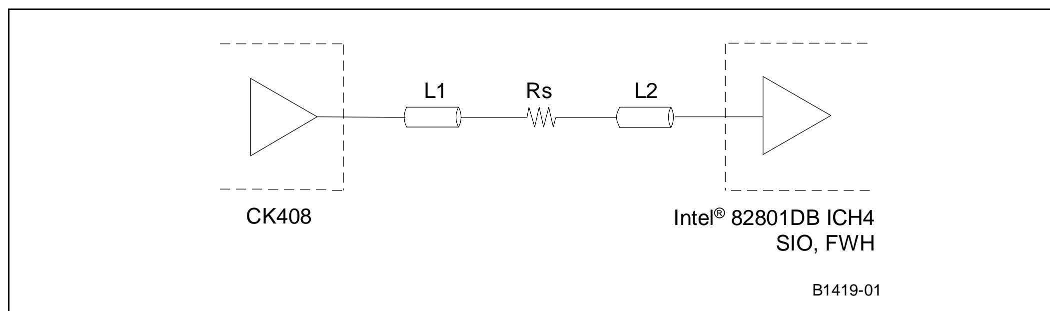


Table 90. CLK33 Clock Group Routing Constraints

Parameter	Definition
Class Name	CLK33
Class Type	Individual Nets
Topology	Series Terminated Point-to-Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ± 5%
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	4 to 8.5 inches
Total Length Range – L1 + L2	CLK66 Length
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Matching	± 100 mils CLK33 to CLK33 to CLK66
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

11.2.4 PCI Clock Group

The PCI clocks are series terminated and routed point-to-point as on the motherboard between the CK408 and the PCI connectors with dedicated buffers for of the three slots. These clocks are synchronous to the CLK33 clocks and are length tuned to compensate for the segment on the PCI daughtercard. Figure 110 illustrates the PCI clock group topology. Table 91 presents the PCICLK clock group routing constraints.

Figure 110. PCI Clock Group Topology

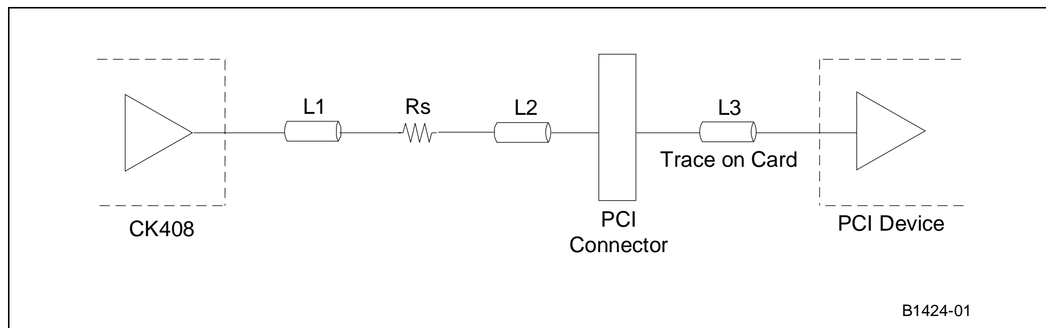


Table 91. PCICLK Clock Group Routing Constraints

Parameter	Definition
Class Name	PCICLK
Class Type	Individual Nets
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ± 5%
Trace Length Limits – L1	Up to 500 mils (breakout segment)
Trace Length Limits – L2	1.5 to 8 inches
Trace Length Limits – L3	2.5 inches (as per PCI specification)
Total Length Range – L1 + L2	CLK33 – 2.5 inches (for nominal matching)
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	± 2 inches PCICLK to (CLK33 – 2.5 inches)
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

11.2.5 CLK14 Clock Group

The 14 MHz clocks are series terminated and routed point-to-point on the motherboard. A single clock output is shared between the two loads. These clocks are length tuned to each other but are not synchronous with any other clocks. Figure 111 illustrates the CLK14 clock group topology. Table 92 presents the CLK14 clock group routing constraints.

Figure 111. CLK14 Clock Group Topology

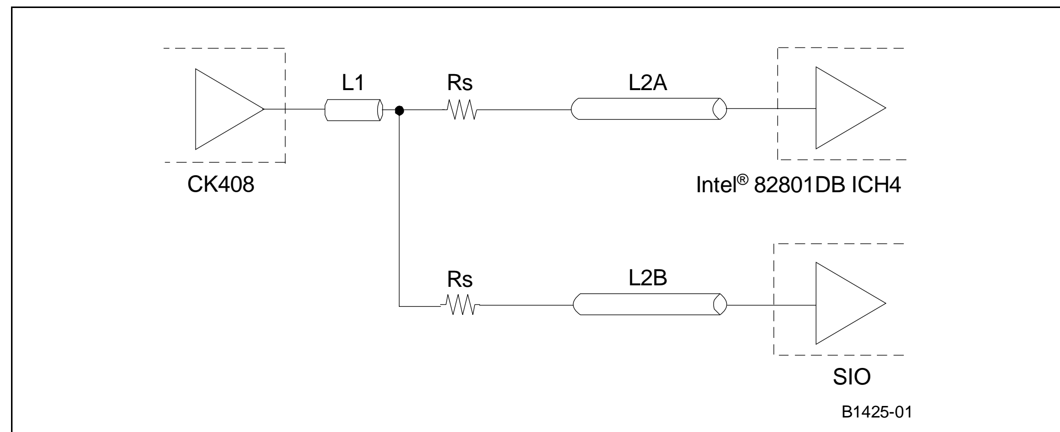


Table 92. CLK14 Clock Group Routing Constraints

Parameter	Definition
Class Name	CLK14
Class Type	Individual Nets
Topology	Dual Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4 (per driver/receiver path)
Series Termination Resistor Value	33 Ω ± 5%
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2A, L2B	2 to 8.5 inches
Total Length Range – L1 + L2A & L1 + L2B	2 to 9 inches
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	± 500 mils CLK14A to CLK14B
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

11.2.6 DOTCLK Clock Group

The 48 MHz DOTCLK is series terminated and routed point-to-point on the motherboard. This clock operates independently and is not length-tuned to any other clock. Figure 112 illustrates the DOTCLK clock topology. Table 93 presents the DOTCLK clock routing constraints.

Figure 112. DOTCLK Clock Topology

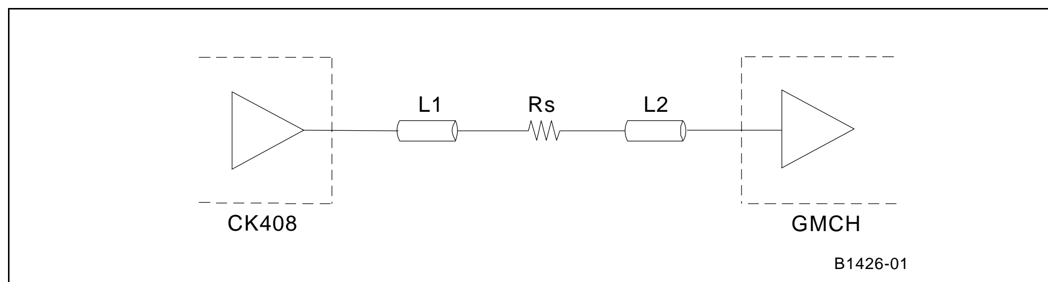


Table 93. DOTCLK Clock Routing Constraints

Parameter	Definition
Class Name	DOTCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	25 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ± 5%
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	2 to 8 inches
Total Length Range – L1 + L2	2 to 8.5 inches
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

NOTE: The DOTCLK is used internally by the GMCH to generate the pixel clock and must exhibit very low jitter. Care should be taken to avoid routing through noisy areas and spacing rules should be observed. Guard traces may be employed if necessary with ground stake vias on no less than 0.5 inch intervals.

11.2.7 SSCCLK Clock Group

The 48/66 MHz SSCCLK operates independently and is not length tuned to any other clock. This clock employs a spread-spectrum device in its path to reduce EMI. The overall clock path is divided into two segments as shown in Figure 113, with each segment series terminated and routed point-to-point. Table 94 presents the SSCCLK clock routing constraints.

Figure 113. SSCCLK Clock Topology

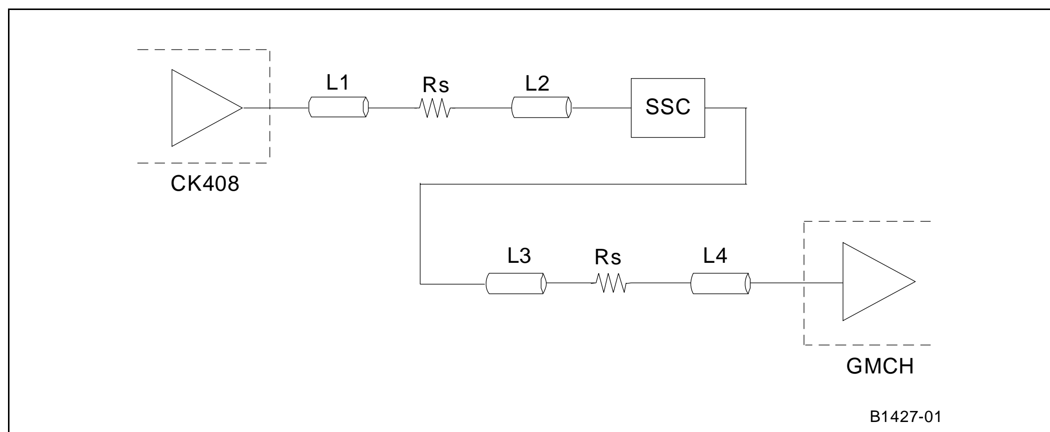


Table 94. SSCCLK Clock Routing Constraints

Parameter	Definition
Class Name	SSCCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Maximum Via Count	4 (per driver/receiver path)
Series Termination Resistor Value	33 Ω ± 5%
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	1 to 4 inches
Trace Length Limits – L3	Up to 500 mils
Trace Length Limits – L4	1 to 7 inches
Total Length Range – L1 + L2 + L3 + L4	3 to 8.5 inches
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

11.2.8 USBCLK Clock Group

The 48 MHz USBCLK is series terminated and routed point-to-point on the motherboard. This clock operates independently and is not length tuned to any other clock. Figure 114 illustrates the USBCLK clock topology. Table 95 presents the USBCLK clock routing constraints.

Figure 114. USBCLK Clock Topology

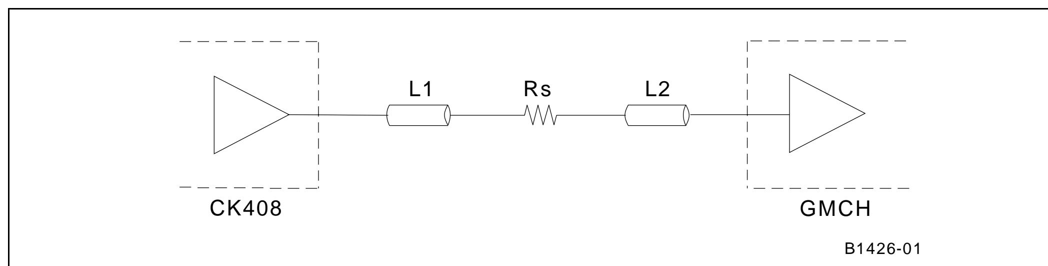


Table 95. USBCLK Clock Routing Constraints

Parameter	Definition
Class Name	USBCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ± 5%
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	3 to 12 inches
Total Length Range – L1 + L2	3 to 12.5 inches
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3 inch

11.3 CK-408 Clock Updates for Pentium® M Processor Platforms

To maximize the power savings on Intel® 855GME chipset-based systems, additional control registers have been added to the CK-408 clock generator to allow option to tri-state the CPU[2:0] host clocks during CPU_STOP# or PWRDWN assertion. The option to have CPU[2:0] driven (default) or tri-stated can be programmed through the serial I^2C bus interface to the CK-408 clock driver. If the tri-state feature on the CPU[2:0] signals is chosen, Intel recommends that the STP_CPU# signal from the ICH4 drive the CK-408's CPU_STOP# signal. Intel also recommends that the ICH4's DPSLP# signal be connected to the DPSLP# pin of the processor and GMCH. Functionally, the ICH4's STP_CPU# and DPSLP# signals are equivalent. However, STP_CPU# is powered by the main I/O well (3.3 V) and is sent to the CK-408 whereas DPSLP# is driven to the processor interface voltage (1.05 V).

11.4 CK-408 PWRDWN# Signal Connections

For systems that do not support S1M but do support the S3 state, the PWRDWN# input of the CK-408 clock chip should be connected to the SLP_S3# output of the ICH4. Intel **does not** recommend that PWRDWN# be pulled-up to the CK-408's 3.3 V power supply if the S3 state is the second highest, power consuming state supported by the platform (i.e., S1M and S2 not supported). The advantage of using SLP_S3# rather than the 3.3 V supply to qualify PWRDWN# is that it reduces the likelihood of the CK-408 clocks driving into unpowered components and potentially damaging the clock input buffers. SLP_S3# can help reduce power consumption because it is asserted before the 3.3 V supply is shut off, thus minimizing the amount of time that the clocks are left toggling.

Platform Power Delivery Guidelines 12

12.1 Definitions

S0/S1 Full-power/stop-grant state:

During full-power operation, all components on the motherboard remain powered.

Note: Full-power operation includes both the full-on operating state and the S1 (processor stop-grant) state.

Suspend operation:

During suspend operation; power is removed from some components on the motherboard. The customer reference board supports three suspend states: Suspend-to-RAM (S3), Suspend-to-Disk (S4), and Soft-off (S5).

- **S3/Suspend-To-RAM (STR)**:
  In the S3 state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered.
- **S4/Suspend-To-Disk**
  In the S4 state, the system state is stored in non-volatile secondary storage (e.g., a hard disk) and all unnecessary system logic is turned off. Only logic required to wake the system remain powered. Standby power rails may or may not be powered depending on system design and the presence of AC or battery power.
- **S5/Soft-off**
  The S5 state corresponds to the G2 state. Restart is only possible with the power button.

Power rails:

An ATX power supply has 6 power rails: +5 V, -5 V, +12 V, -12 V, +3.3 V, 5 Vsb. In addition to these power rails, several other power rails are created with voltage regulators.

Core power rail:

Power rail that is only on during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX 12 V power supply are +5 V, -5 V, +12 V, -12 V, +3.3 V.

Standby power rail:

A power rail that is on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is: 5 Vsb (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.

Derived power rail:

A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3 Vsb is usually derived (on the motherboard) from 5 Vsb using a voltage regulator.

Dual power rail:

A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during suspend operation and derived from a core supply during full-power operation.

Note: The voltage on a dual power rail may be misleading.

12.2 Power Delivery Map

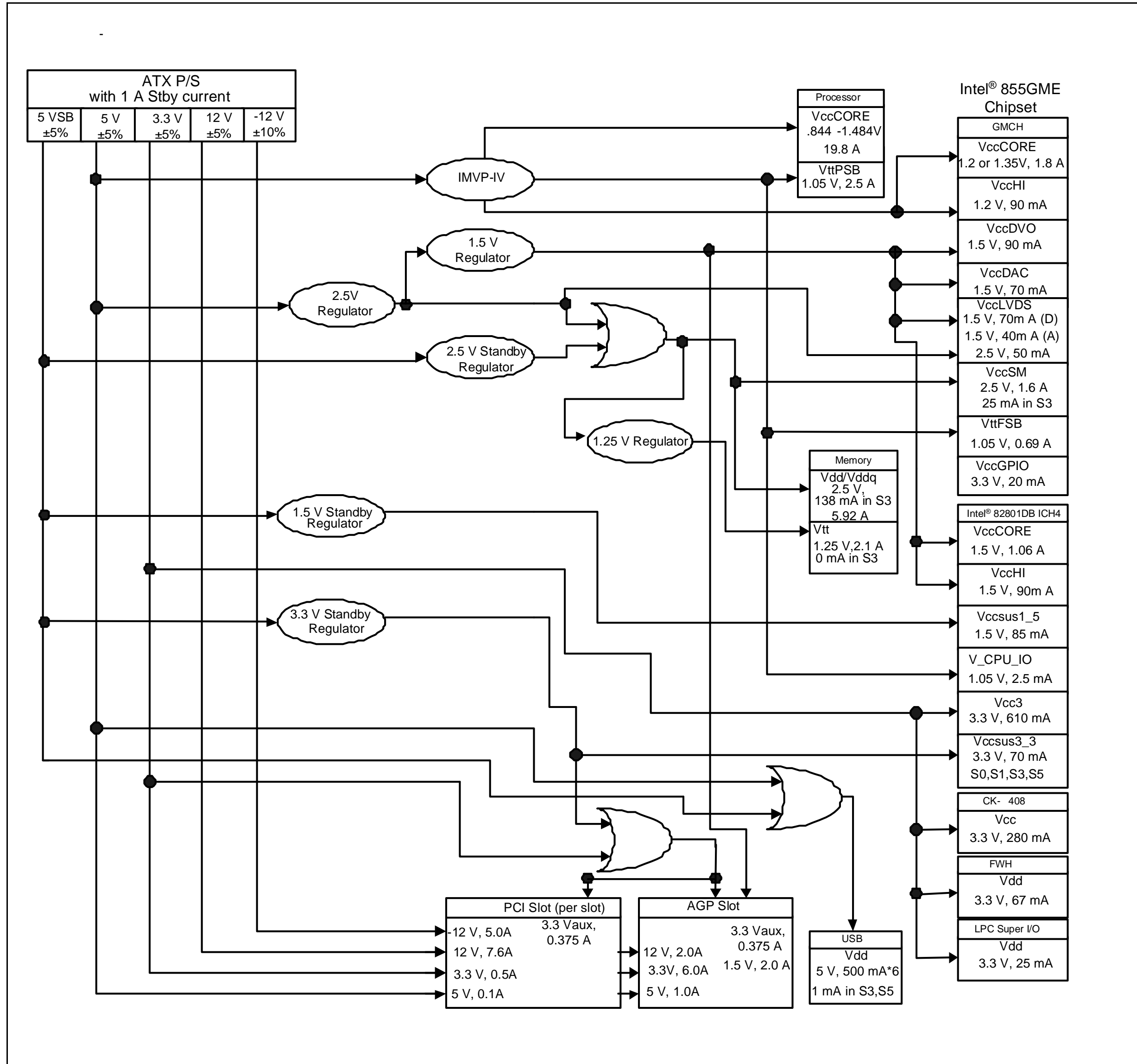
During STR, only the necessary devices are powered. These devices include: main memory, the Intel® 82801DB I/O Controller Hub 4 (ICH4) resume well, PCI wake devices (via 3.3 Vaux), AC’97, and USB. To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device’s power requirements, both in suspend and in full-power. The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create dual power rails.

The solutions in this design guide are only examples. Many power distribution methods achieve the similar results. When deviating from these examples, it is critical to consider the effect of a change.

12.2.1 Platform Power Delivery Architectural Block Diagram

Figure 115 illustrates the platform power delivery architectural block diagram.

Figure 115. Platform Power Delivery Block Diagram



12.3 Intel® 855GME Chipset Platform Power-Up Sequence

The following sections describe the power-on timing sequence for Intel® 855GME Chipset Graphics Memory Controller Hub (82855GME) based platforms.

12.3.1 Processor Power Sequence Requirement

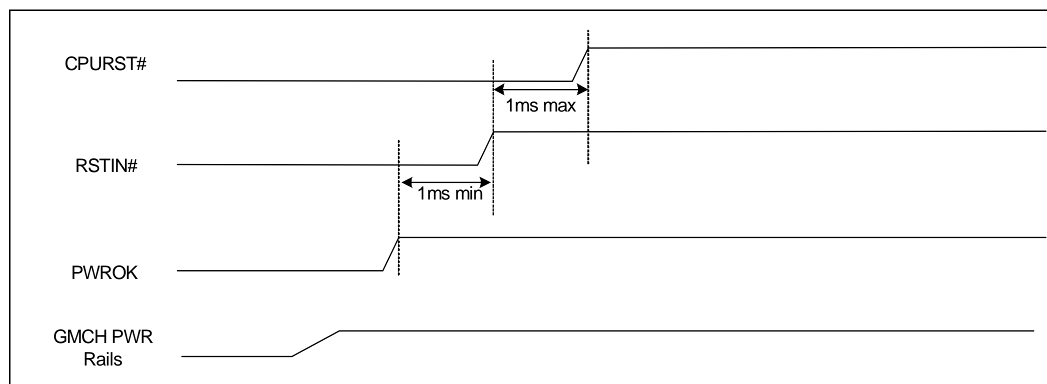
Contact your Intel Field Representative for details on the Pentium® M processor with the Intel® IMVP-IV voltage regulator.

12.3.2 GMCH Power Sequencing Requirements

All GMCH power rails should be stable before PWROK is asserted. The power rails may be brought up in any order desired. **However, good design practice would have all GMCH power rails come up as close in time as practical, with the core voltage (1.35 V) coming up first.** RSTIN#, which brings GMCH out of reset, should be deasserted only after PWROK has been active for one ms. After GMCH is out of reset, it deasserts CPURST# within one ms.

Figure 116 illustrates the GMCH power-up sequence.

Figure 116. GMCH Power-up Sequence



12.3.3 Intel® 82801DB I/O Controller Hub 4 (ICH4) Power Sequencing Requirements

Figure 117 and Figure 118 show the power-up reset and sequence for ICH4. The VRMPWRGD input should be connected to the processor voltage regulator PWRGD output. When both PWROK and VRMPWRGD are asserted, it indicates that core power and system power are stable and PCIRST# is de-asserted a minimum of 1 ms later. It is the responsibility of the system designer to ensure that the power and timing requirements for the processor and GMCH are met. Refer to the *Intel® 82801DB I/O Controller Hub (ICH4) Datasheet* for more information.

Figure 117 illustrates the ICH4 power-up reset sequence.

Figure 117. Intel® 82801DB I/O Controller Hub 4 (ICH4) Power-up Reset

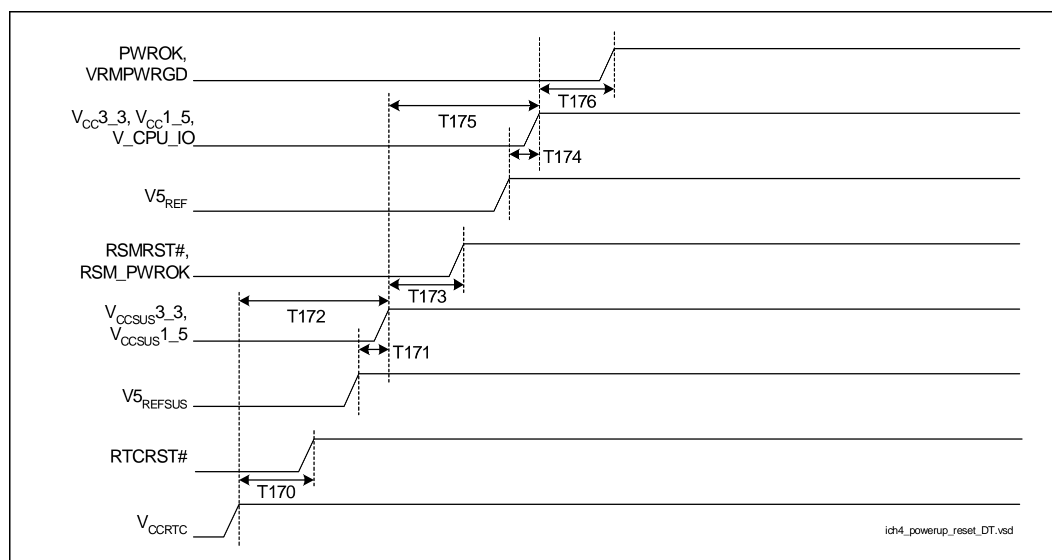


Figure 118 illustrates the ICH4 power-up sequence.

Figure 118. Intel® 82801DB I/O Controller Hub 4 (ICH4) Power-Up Sequence

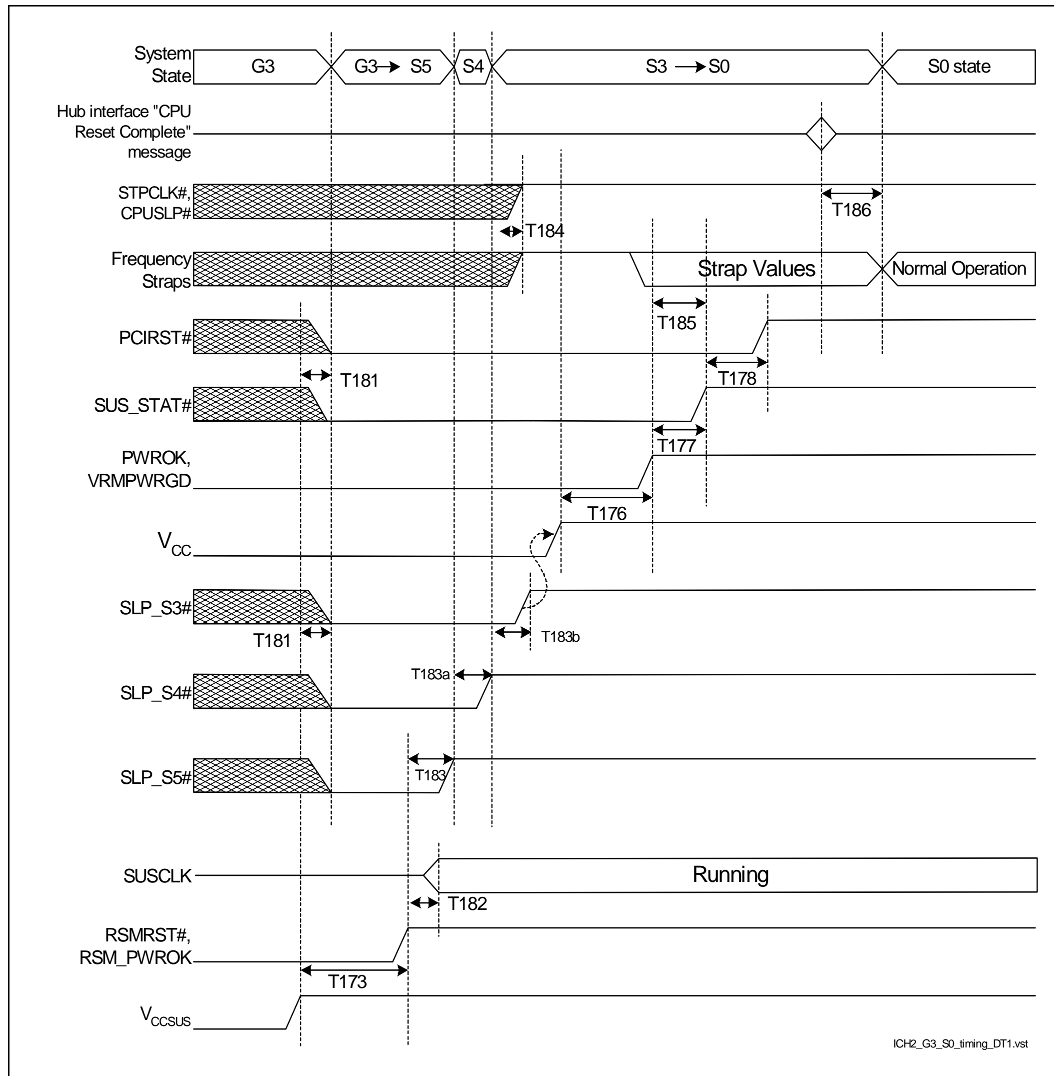


Table 96 presents the timing sequence parameters as they relate to Figure 118.

Table 96. Timing Sequence Parameters for Figure 118

Sym	Description	Min	Max	Units	Notes	Figure
T170	V_{CCRTC} active to RTCRST# inactive	5		ms	1	115
T171	$V5_{REFSUS}$ active to $V_{CCSUS}3_3$, $V_{CCSUS}1_5$ active	0		ms		115
T172	V_{CCRTC} supply active to V_{CCSUS} supplies active	0		ms	2	115
T173	V_{CCSUS} supplies active to LAN_RST# active, RSMRST# inactive	10	-	ms		115,116
T174	$V5_{REF}$ active to $V_{CC}3_3$, $V_{CC}1_5$, V_{CCHI} active	0		ms	1	115
T175	V_{CCSUS} supplies active to Vcc supplies active	0		ms	2	115
T176	V_{CC} supplies active to PWROK, VRMPWRGD active	10	-	ms		115, 116
T177	PWROK and VRMPWRGD active and SYS_RESET# inactive to SUS_STAT# inactive	32	38	RTCCLK		116
T178	SUS_STAT# inactive to PCIRST# inactive	1	3	RTCCLK		116
T181	V_{CCSUS} active to SLP_S5#, SUS_STAT# and PCIRST# active		50	ns		116
T182/T183	RSMRST# inactive to SUSCLK running, SLP_S5# inactive		110	ms	3	116
T183a	SLP_S5# inactive to SLP_S4# inactive	1	2	RTCCLK		116
T183b	SLP_S4# inactive to SLP_S3# inactive	1	2	RTCCLK		116
T184	V_{CC} active to STPCLK#, CPUSLP# inactive, and CPU Frequency Strap signals high		50	ns		116
T185	PWROK and VRMPWRGD active and SYS_RESET# inactive to SUS_STAT# inactive and CPU Frequency Straps latched to strap values	32	38	RTCCLK	4	116
T186	CPU Reset Complete to Frequency Straps signals unlatched from strap values	7	9	CLK66	5	116

NOTES:
1. The $V5_{REF}$ supply must power up before or simultaneously with its associated 3.3 V supply, and must power down simultaneously with or after the 3.3 V supply.
2. The V_{CCSUS} supplies must never be active while the V_{CCRTC} supply is inactive.
3. When there is no RTC battery in the system, so V_{CCRTC} and the V_{CCSUS} supplies come up together, the delay from RTCRST# and the RSMRST# inactive to SUSCLK toggling may be as much as 1000 ms.
4. These transitions are clocked off the internal RTC. One RTC is approximately 32 µs.
5. This transition is clocked off the 66 MHz CLK66. One CLK66 is approximately 15 ns.

12.3.3.1 3.3 V/1.5 V Power Sequencing

The ICH4 has power sequencing requirements for the 3.3 V and 1.5 V rails in respect to each other. This requirement is as follows: The 1.5 V rail must power up before or simultaneously with the 3.3 V rail. The 3.3 V and 1.5 V rails must power down simultaneously.

The majority of the ICH4 I/O buffers are driven by the 3.3 V supplies but are controlled by logic powered by the 1.5 V supplies. Therefore, another consequence of faulty power sequencing arises when the 3.3 V supply comes up first. In this case, the I/O buffers may be in an undefined state until the 1.5 V logic is powered up. Some signals that are defined as 'Input-only' actually have output buffers that are normally disabled, and the Intel ICH4 may unexpectedly drive these signals when the 3.3 V supply is active while the 1.5 V supply is not.

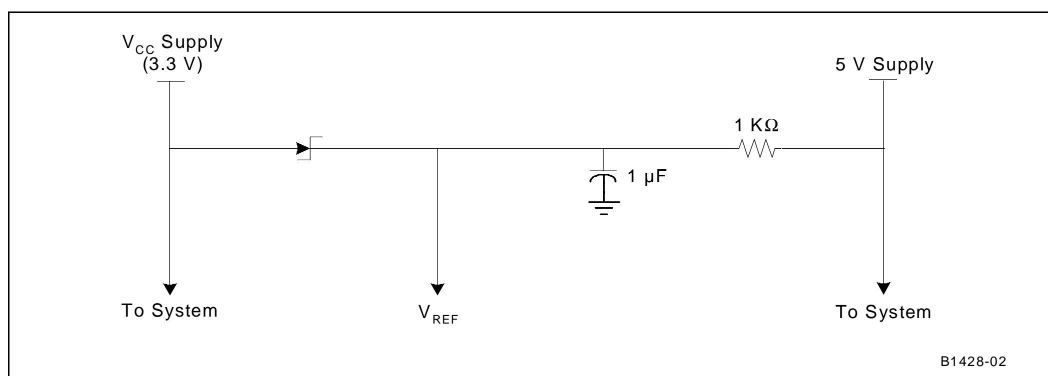
12.3.3.2 $V5_{REF}$/ $V5_{REFSUS}$ Sequencing

$V5_{REF}$ is the reference voltage for 5 V tolerance on inputs to the ICH4. $V5_{REF}$ must be powered up before $V_{CC}3_3$, or after $V_{CC}3_3$ within 0.7 V. Also, $V5_{REF}$ must power down after $V_{CC}3_3$, or before $V_{CC}3_3$ within 0.7 V. These rules must be followed to ensure proper functionality of the ICH4. When the rule is violated, internal diodes attempt to draw power sufficient to damage the diodes from the $V_{CC}3_3$ rail. Figure 119 illustrates a sample implementation of how to satisfy the $V5_{REF}$/ 3.3 V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the $V_{CCSUS}3_3$ rail is derived from the $V_{CCSUS}5$ and therefore, the $V_{CCSUS}3_3$ rail always comes up after the $V_{CCSUS}5$ rail. As a result, $V5_{REF_SUS}$ is always powered up before $V_{CCSUS}3_3$. In platforms that do not derive the $V_{CCSUS}3_3$ rail from the $V_{CCSUS}5$ rail, this rule must be comprehended in the platform design.

Additionally, the ICH4 requires the $V5_{REF_SUS}$ rail to be hooked to a 5 V sustained source.

Figure 119. Example $V5_{REF}$/$V5_{REFSUS}$ Sequencing Circuitry



12.3.3.3 $V_{5REFSUS}$ Design Guidelines

To meet reliability and testing requirements for the USB interface, observe the following design recommendations for the V5REFSUS pins of the ICH4. Changes to the USB specification regarding continuous short conditions must be addressed. The USB 1.1 specification requires host controllers to withstand a continuous short between the USB 5-V connector supply and a USB signal at the connector. However, the duration is unspecified. The USB 2.0 specification requires this duration to be at least 24 hours. This in turn requires that the V5REFSUS pin be at 5 V as long as the attached USB devices are powered. The recommendation is to provide a +V5ALWAYS (active S0-S5)

supply to the V5REFSUS pin if available as shown in Figure 120. However, if support for wake on USB from S3 and support for self-powered USB devices are not required, then use the option shown in Figure 121. V5REFSUS can be supplied by a combination of +V5S (active in S0 only) and +V3ALWAYS (active S0-S5).

Figure 120. V5REFSUS With +V5ALWAYS Connection Option

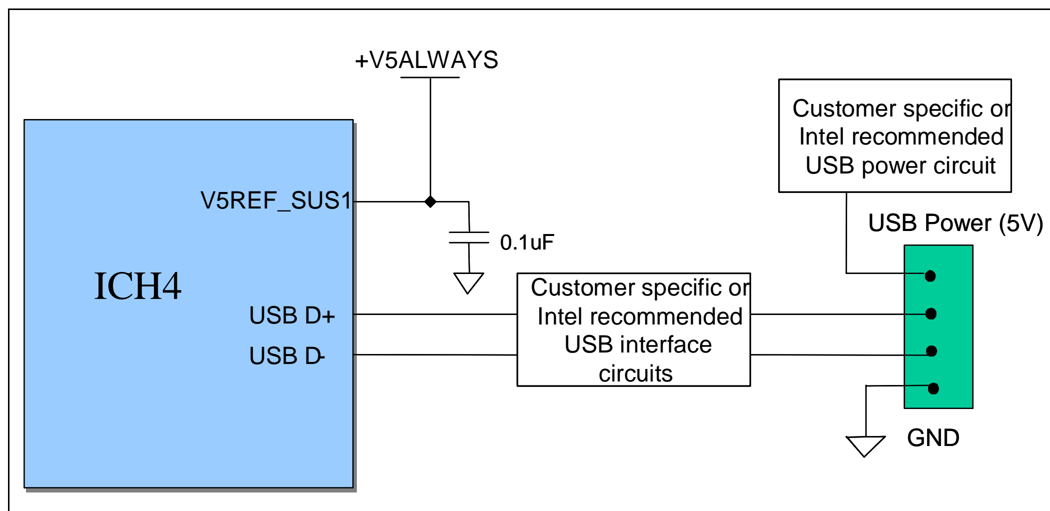
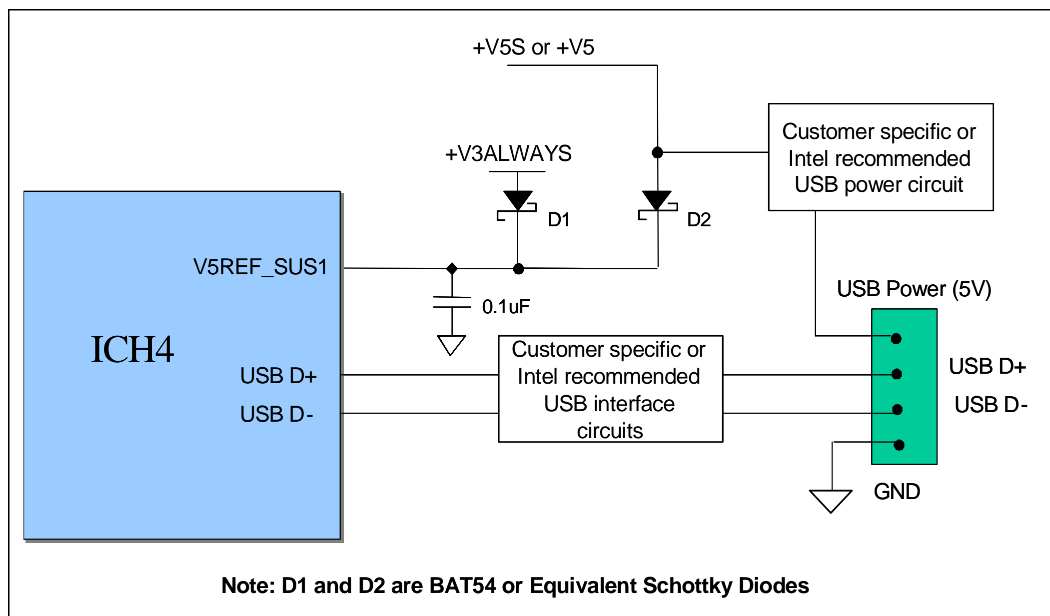


Figure 121. V5REFSUS With +V3ALWAYS and +V5S or +V5 Connection Option



12.3.3.4 Power Supply PS_ON Consideration

When a pulse on SLP_S3# or SLP_5# is short enough (~ 10 – 100 ms) such that PS_ON is driven active during the exponential decay of the power rails, a few power supply designs may not be designed to handle this short pulse condition. In this case, the power supply does not respond to this event and never powers back up. These power supplies would need to be unplugged and

re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they may properly respond to PS_ON. This level varies with affected power supply.

The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue may affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

The platform designer must ensure that the power supply used with the platform is not affected by this issue.

12.3.4 DDR Memory Power Sequencing Requirements

No DDR-SDRAM power sequencing requirements are specified during power up or power down if the following criteria are met:

- V_{DD} and V_{DDQ} to memory devices are driven from a single power converter output.
- V_{TT} is limited to 1.44 V (reflecting VDDQ(max)/2 + 50 mV V_{REF} variation + 40 mV V_{TT} variation)
- V_{REF} tracks $V_{DDQ}/2$
- A minimum resistance of 42 Ω (22 Ω series resistor + 22 Ω parallel resistor ± 5% tolerance) limits the input current from the VTT supply into any pin.

If the above criteria cannot be met by the system design, Table 97 must be adhered to during power up. Refer to *Intel® DDR 200 JEDEC Spec Addendum* for more details.

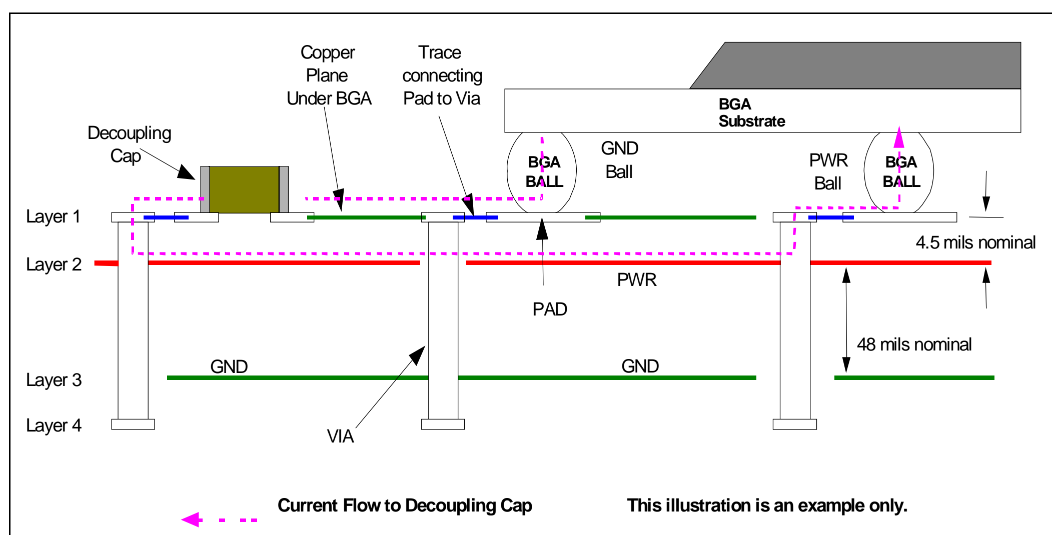
Table 97. DDR Power-Up Initialization Sequence

Voltage Description	Sequencing	Voltage Relationship to Avoid Latch-up
V_{DDQ}	After or with V_{DD}	$< V_{DD} + 0.3$ V
V_{TT}	After or with V_{DDQ}	$< V_{DDQ} + 0.3$ V
V_{REF}	After or with V_{DDQ}	$< V_{DDQ} + 0.3$ V

12.4 Intel® 855GME Chipset Platform Power Delivery Guidelines

Each component is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. Intel recommends that the developer use the amount of decoupling capacitors specified in this document to ensure the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible. Rotate caps that set over power planes so that the loop inductance is minimized (see Figure 122). The basic theory for minimizing loop inductance is to consider which voltage is on Layer 2 (power or ground) and spin the decoupling cap with the opposite voltage toward the BGA (Ball Grid Array). This greatly minimizes the total loop inductance. Intel recommends that for prototype board designs, the designer should include pads for extra power plane decoupling caps.

Figure 122. Example for Minimizing Loop Inductance



12.4.1 Processor Decoupling/Power Delivery Guidelines

Refer to the *Intel® Pentium® M Processor Datasheet, Intel® Pentium® M Processor on the 90 nm process with 2 MB L2 Cache Datasheet, and Intel® Celeron® M Processor Datasheet* for details.

12.4.2 Intel® 855GME Chipset and Decoupling Guidelines

Decoupling in Table 98 is based on the voltage regulator solution used on the customer reference board design.

Table 98. GMCH Decoupling Recommendations

Pin Name	Configuration	F	Qty	TYPE	Notes
V_{CC}	Connect to V_{CC}1_2S for 855GM/855GME	0.1 µF 10 µF 150 µF	4 1 2	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	1 X 0.1 µF within 200 mils 3 X 0.1 µF on bottom side
V_{TTLF}	Connect to V_{CCP}	0.1 µF 10 µF 150 µF	2 1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	2 X 0.1 µF on bottom side
V_{TTHF}	Connect to caps directly	0.1 µF	5	XR7, 0603, 16 V, 10%	
V_{CCHL}	Connect to V_{CC}1_2S for 855GM/855GME	0.1 µF 10 µF	2 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20%	1 X 0.1 µF within 200 mils 1 X 0.1 µF on bottom side
V_{CCSM}	Connect to V_{CCSUS}2_5	0.1 µF 150 µF	11 2	XR7, 0603, 16 V, 10% TANT, D, 10 V, 20%	Refer to Section 12.4.2.1 for more information.
V_{CCDVO}	Connect to V_{CC}1_5S	0.1 µF 10 µF 150 µF	2 1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	1 X 0.1 µF within 200 mils 1 X 0.1 µF on bottom side
$V_{CCDLVDS}$	Connect to V_{CC}1_5S	0.1 µF 22 µF 47 µF	1 1 1	XR7, 0603, 16 V, 10% TANT, B, 10 V, 20% TANT, D, 10 V, 20%	1 X 0.1 µF within 200 mils
$V_{CCTXLVDS}$	Connect to V_{CCSUS}2_5	0.1 µF 22 µF 47 µF	3 1 1	XR7, 0603, 16 V, 10% TANT, B, 10 V, 20% TANT, D, 10 V, 20%	1 X 0.1 µF within 200 mils 2 X 0.1 µF on bottom side
V_{CCGPIO}	Connect to V_{CC}3_3S	0.1 µF 10 µF	1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20%	
SMVREF		0.1 µF	1	XR7, 0603, 16 V, 10%	1 X 0.1 µF on bottom side

12.4.2.1 GMCH V_{CCSM} Decoupling

For the V_{CCSM} pins of the GMCH, a minimum of eleven, 0603 form factor, 0.1 µF, high-frequency capacitors is required and must be placed within 150 mils of the GMCH package. The capacitors should be evenly distributed along the GMCH DDR system memory interface and must be placed perpendicular to the GMCH with the power (2.5 V) side of the capacitors facing the GMCH.

- Every GMCH ground and V_{CCSM} power ball in the system memory interface should have its own via.
- Each capacitor should also have its own 2.5 V via within 25 mils of the capacitor pad for connecting to a 2.5 V copper flood. The traces from the capacitors should also be wide and connect to the outer row of balls on the GMCH.

- The ground end of each capacitor must connect to the ground flood and to the ground plane through a via. Each via should be as close to the associated capacitor pad as possible, within 25 mils and with as thick a trace as possible.
- The system memory interface also requires low frequency decoupling. Place two 150 µF electrolytic capacitors between the GMCH and the first DIMM connector.

12.4.2.2 DDR SDRAM VDD Decoupling

Discontinuities in the DDR signal return paths occur when the signals transition between the motherboard and the DIMMs. To account for this ground to 2.5 V discontinuity, a minimum of nine 0603 form factor 0.1 µF high-frequency bypass capacitors is required between the DIMMs to help minimize any anticipated return path discontinuities that should be created. The capacitors should be distributed as evenly as possible between the two DIMMs.

- Wide ground trace from each capacitor should be connect to a via that transitions to the ground plane. Each ground via should be placed as close to the ground pad as possible.
- Wide 2.5 V trace from each capacitor should connect to a via that transitions to the 2.5 V copper flood. Each via should be placed as close to the capacitor pad as possible. Each capacitor pad should also connect to the closest 2.5 V DIMM pin on either the first or second DIMM connector with a wide trace.
- The DDR DIMMs also require bulk decoupling in addition to what is required by the GMCH. Place a minimum of four 100-150 µF capacitors near the DIMM connectors.

12.4.2.3 DDR V_{TT} Decoupling Placement and Layout Guidelines

The V_{TT} termination rail must be decoupled using high-speed bypass capacitors, one 0603 form factor, 0.1 µF capacitor and one 0603 form factor, 0.01 µF capacitor per two DDR signals. They must be placed no more than 100 mils from the termination resistors.

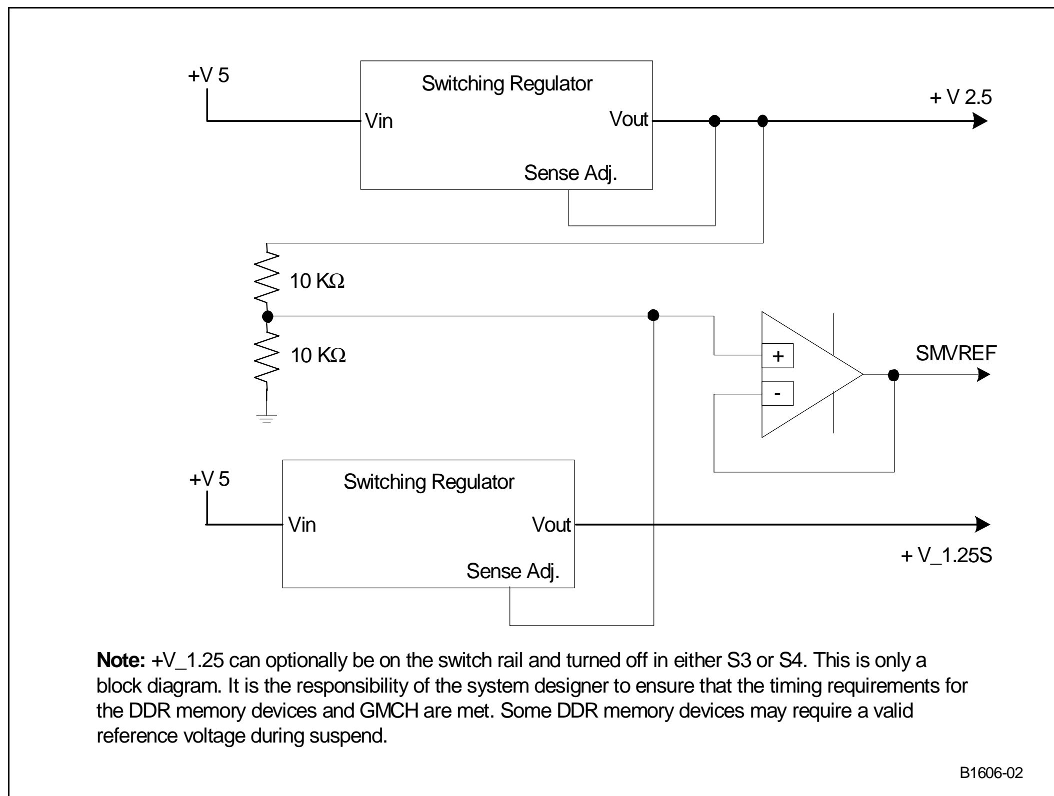
- A V_{TT} copper flood must be used. The decoupling capacitors must be spread out across the termination rail so that all the parallel termination resistors are near high-frequency capacitors.
- Each capacitor ground via should be as close to the capacitor pad as possible, within 25 mils with as thick a trace as possible.
- Place one 4.7 µF ceramic capacitor on each end of the V_{TT} termination rail, and place on 4.7 µF ceramic capacitor near the center of the termination rail. The power end of these capacitors must connect directly to the V_{TT} termination rail and the ground end is connected to ground.
- For low frequency bulk decoupling at the V_{TT} termination rail, evenly place four 470 µF capacitors.

12.4.3 DDR Memory Power Delivery Design Guidelines

The main focus of these GMCH guidelines is to minimize signal integrity problems and improve the power delivery to the GMCH system memory interface and the DDR memory DIMMs. This section discusses the DDR memory system voltage and current requirements as determined at publishing of this document. This document is not the original source for these specifications. Figure 123 illustrates the implementation of 2.5 V, 1.25 V and SMVREF on the CRB only as an example. It is the responsibility of the system designer to ensure that the power requirements for the DDR and GMCH are met. Refer to the following documents for the latest details on voltage and current requirements found in this design guide.

- *JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification*
- *JEDEC 184-Pin Unbuffered DDR DIMM Specification*

Figure 123. DDR Power Delivery Block Diagram



12.4.3.1 2.5 V Power Delivery Guidelines

The 2.5 V power for the GMCH system memory interface and the DDR DIMMs is delivered around the DDR command, control, and clock signals. Special attention must be paid to the 2.5 V copper flooding to ensure proper GMCH and DIMM power delivery. This 2.5 V flood must extend from the GMCH 2.5 V power vias all the way to the 2.5 V DDR voltage regulator and its bulk capacitors. The 2.5 V DDR voltage regulator must connect to the 2.5 V flood with a minimum of six vias. The DIMM connector 2.5 V pins as well as the GMCH 2.5 V power vias must connect to the 2.5 V copper flood.

In the areas where the copper flooding necks down around the GMCH make sure to keep these neck down lengths as short as possible. The 2.5 V copper flooding under the DIMM connectors must encompass all the DIMM 2.5 V pins and must be solid except for the small areas where the clocks are routed within the DIMM pin field to their specified DIMM pins.

Note: A minimum of 12 mil isolation spacing should be maintained between the copper flooding and any signals on the same layer.

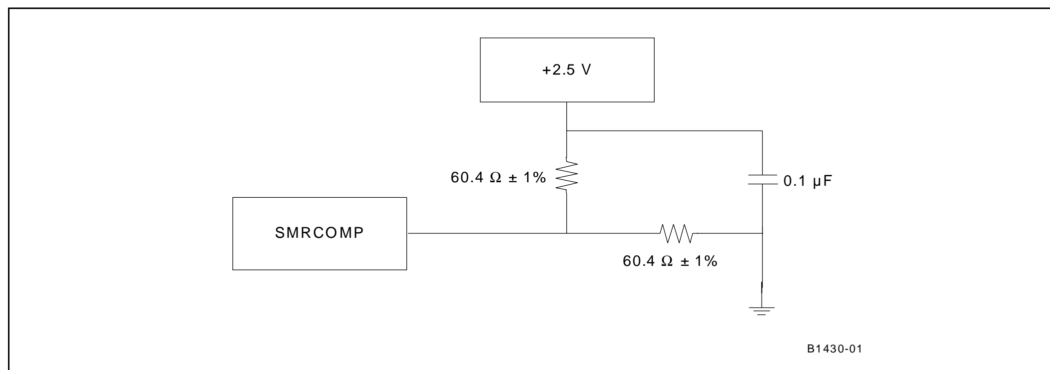
12.4.3.2 GMCH and DDR SMVREF Design Recommendations

There is one SMVREF pin on the GMCH that is used to set the reference voltage level for the DDR system memory signals (SMVREF). The voltage level that needs to be supplied to this pin must be equal to $V_{CCSM}/2$. As shown in Figure 123, Intel recommends an OpAmp buffer to generate SMVREF from the 2.5 V supply. This should be used as the V_{REF} signals to both the DDR memory devices and the SMVREF signal to the GMCH. A resistor divider is not a recommended solution since SMVREF has a tight tolerance of ± 2%.

12.4.3.3 DDR SMRCOMP Resistive Compensation

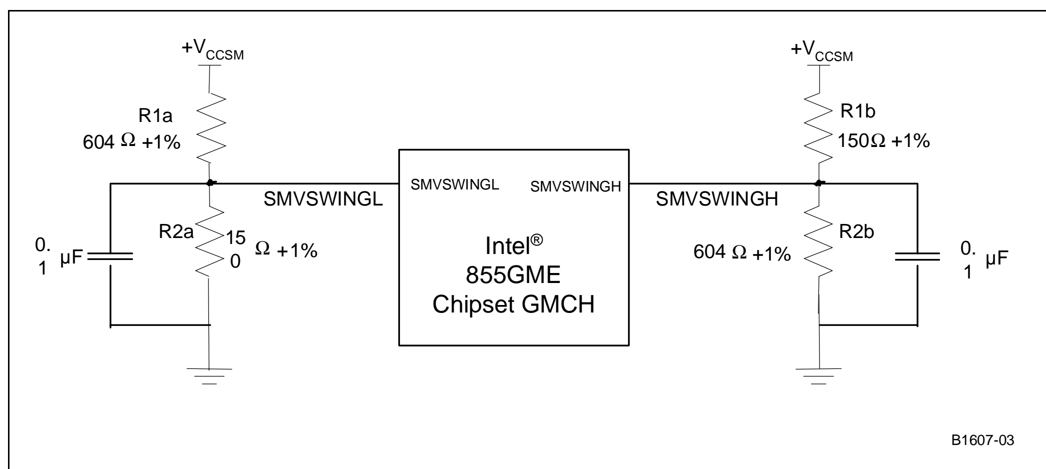
The GMCH requires a system memory compensation resistor, SMRCOMP, to adjust buffer characteristics to specific board and operation environment characteristics. Refer to the *Intel® 855GM/855GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet* and Figure 124 for details on resistive compensation. The SMRCOMP signal should be routed with as wide a trace as possible. It should be a minimum of 12 mils wide and be isolated from other signals with a minimum of 10 mils spacing. A 0.1 µF capacitor should be placed near the 2.5 V supply of the voltage divider and **not** on the SMRCOMP pin.

Figure 124. GMCH SMRCOMP Resistive Compensation



The GMCH's system memory resistive compensation mechanism also requires the generation of reference voltages to the SMVSWINGL and SMVSWINGH pins. The schematic for SMVSWINGL and SMVSWINGH voltage generation is shown in Figure 125. Two resistive dividers with R1b = R2a = 150 Ω ± 1% and R1a = R2b = 604 Ω ± 1% generate the SMVSWINGL and SMVSWINGH voltages. SMVSWINGL and SMVSWINGH components should be placed within 0.5 inch of their respective pins and connected with a 15 mil wide trace. To avoid coupling with any other signals, maintain a minimum of 25 mils of separation to other signals.

Figure 125. GMCH System Memory Reference Voltage Generation Circuit



12.4.3.4 DDR V_{TT} Termination

Intel's recommended topology for DDR-SDRAM Data, Control, and Command signal groups requires that all these signals be terminated to a 1.25 V source, V_{TT}, at the end of the memory channel opposite the GMCH. Intel recommends that V_{TT} be generated from the same source as used for V_{CCSM}, and not be used for GMCH and DDR SMVREF. This is because SMVREF has a much tighter tolerance and V_{TT} may vary more easily depending on signal states. A solid 1.25 V termination island should be used for this purpose and be placed on the surface signal layer, just beyond the last DIMM connector and must be at least 50 mils wide.

The data and command signals should be terminated using one resistor per signal. Resistor packs and ± 5% tolerant resistors are acceptable for this application. Only signals from the same DDR signal group may share a resistor pack. Refer to Section 5 for system memory guidelines.

12.4.3.5 DDR SMRCOMP, SMVREF and V_{TT} 1.25 V Supply Disable in S3/Suspend

Regardless of how these 1.25 V supplies for GMCH are generated, they may be disabled during the S3 suspend state to further save power on the platform. This is possible because the GMCH does not require a valid reference voltage nor does it require the enabling of resistive compensation during suspend. **However, some DDR memory devices may require a valid reference voltage during suspend**. It is the responsibility of the system designer to ensure that requirements of the DDR memory devices are met.

Note: The 2.5 V V_{CCSM} power pins of the GMCH and the V_{DD} power pins of the DDR memory devices do need to be on in S3 state.

12.4.4 Other GMCH Reference Voltage and Analog Power Delivery

12.4.4.1 GMCH GTLVREF

For GMCH, the GTLREF generation circuit has been broken down into three separate voltage references: host data reference voltage (HDVREF[2:0]), host address reference voltage (HAVREF) and host common clock reference voltage (HCCVREF). Maximum length from pin to voltage divider for each reference voltage should be less than 0.5 inch. Intel recommends 10 mil wide traces. GMCH V_{REF} may be maintained as individual voltage dividers as shown in Figure 126, Figure 127, and Figure 128.

Figure 126 illustrates the GMCH HDVREF[2:0] reference voltage generation circuit.

Figure 126. GMCH HDVREF[2:0] Reference Voltage Generation Circuit

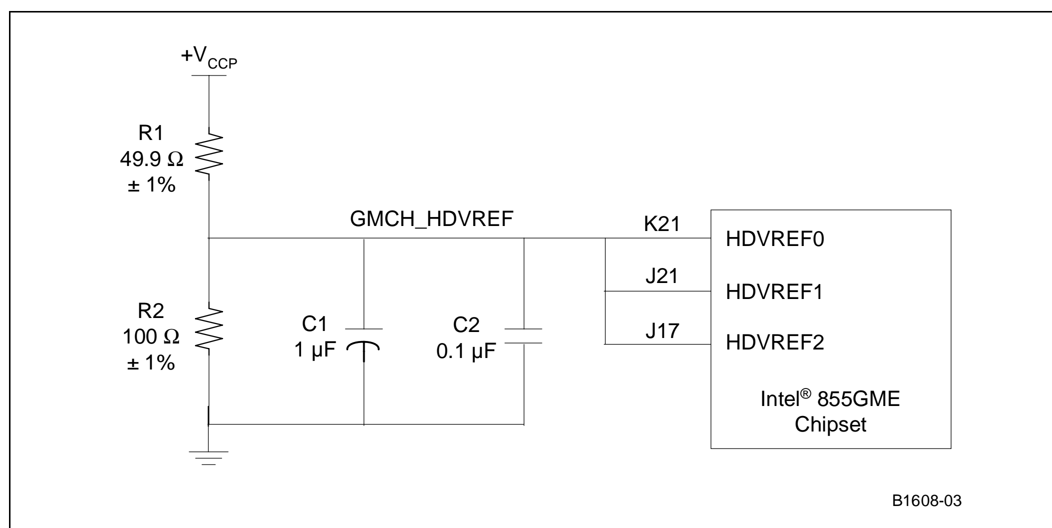


Figure 127 illustrates the GMCH HAVREF reference voltage generation circuit.

Figure 127. GMCH HAVREF Reference Voltage Generation Circuit

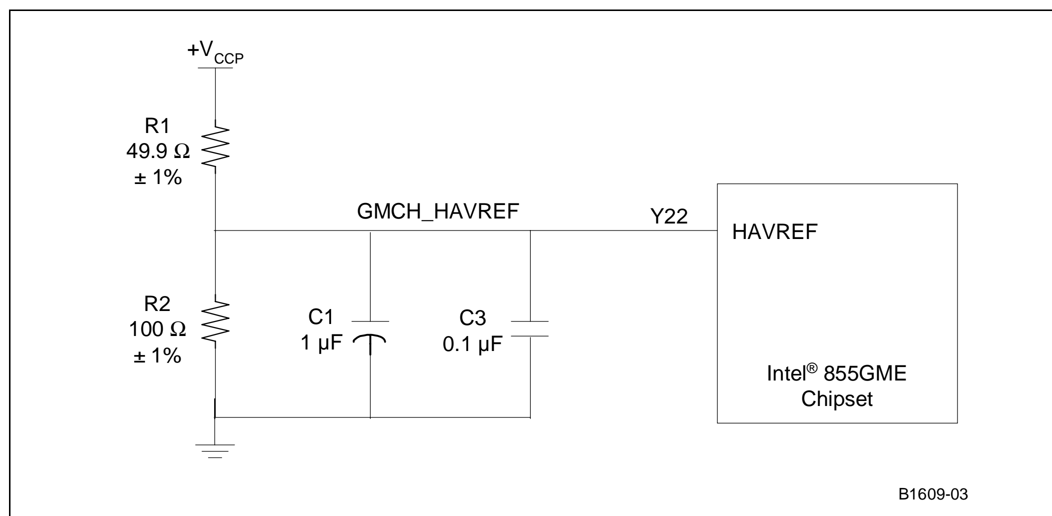
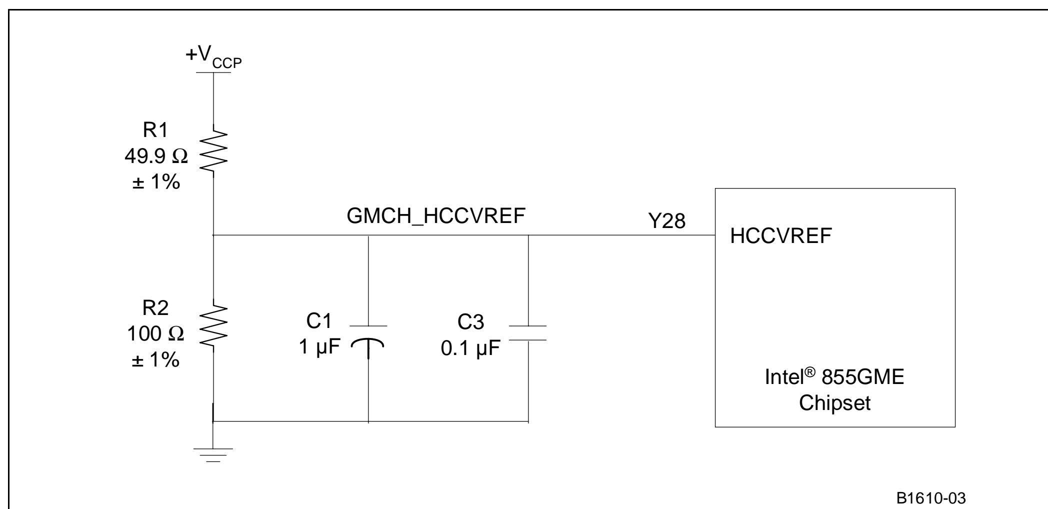


Figure 128 illustrates the GMCH HCCVREF reference voltage generation circuit.

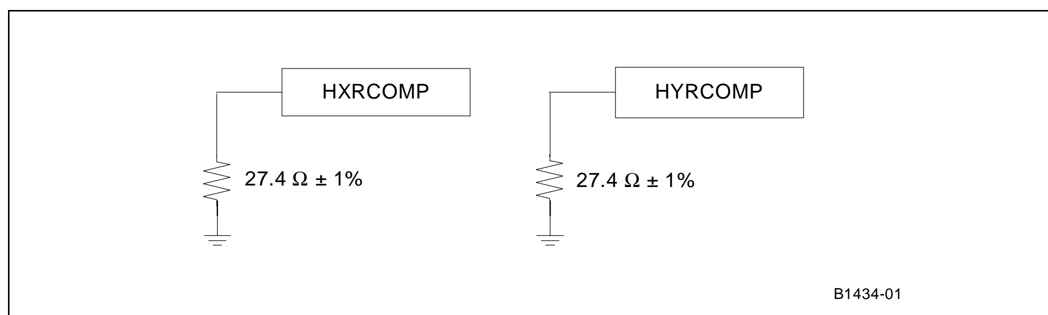
Figure 128. GMCH HCCVREF Reference Voltage Generation Circuit



12.4.4.2 GMCH AGTL+ I/O Buffer Compensation

The HXRCOMP and HYRCOMP pins of the GMCH should each be pulled-down to ground with a 27.4 Ω ± 1% resistor (see Figure 129). The maximum trace length from pin to resistor should be less than 0.5 inch and should be 18 mil wide to achieve the Zo = 27.4 Ω target. Also, the routing for HRCOMP should be at least 25 mils away from any switching signal.

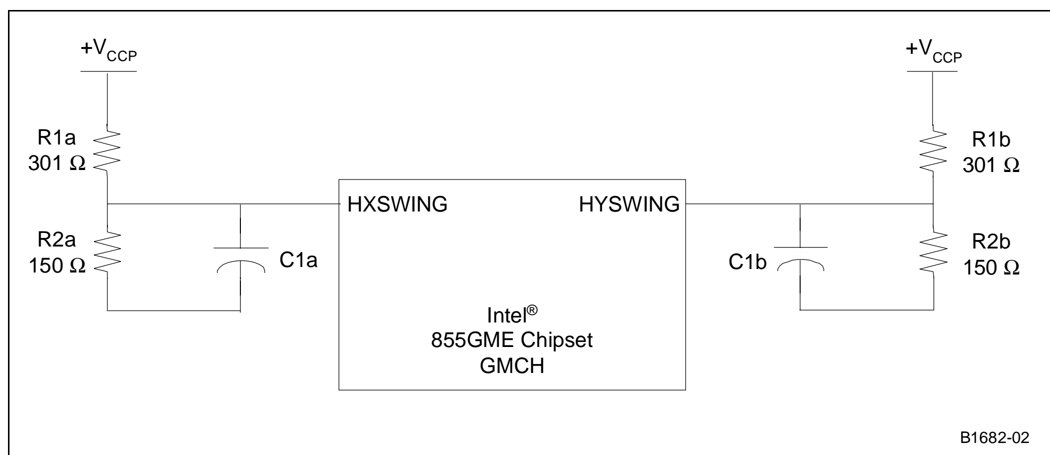
Figure 129. GMCH HXRCOMP and HYRCOMP Resistive Compensation



12.4.4.3 GMCH AGTL+ Reference Voltage

The GMCH's AGTL+ I/O buffer resistive compensation mechanism also requires the generation of reference voltages to the HXSWING and HYSWING pins with a value of 1/3*V_{CCP}. Implementations for HXSWING and HYSWING voltage generation are shown in Figure 130. Two resistive dividers with R1a = R1b = 301 Ω ± 1% and R2a = R2b = 150 Ω ± 1% generate the HXSWING and HYSWING voltages. C1a = C1b = 0.1 µF act as decoupling capacitors and connect HXSWING and HYSWING to V_{CC_CORE}. HSWING components should be placed within 0.5 inch of their respective pins and connected with a 15 mil wide trace. To avoid coupling with any other signals, maintain a minimum of 25 mils of separation to other signals.

Figure 130. GMCH HXSWING and HYSWING Reference Voltage Generation Circuit



12.4.4.4 GMCH Analog Power

Table 99 presents the eight analog circuits that require filtered supplies on the GMCH. They are: V_{CCASM}, V_{CCQSM}, $V_{CCAHPLL}$, $V_{CCADPLLA}$, $V_{CCADPLLB}$, V_{CCADAC}, $V_{CCAGPLL}$, and $V_{CCALVDS}$.

V_{CCADAC}, $V_{CCAGPLL}$, and $V_{CCALVDS}$ do not require an RLC filter but do require decoupling capacitors. Figure 131 illustrates an example analog supply filter.

Figure 131. Example Analog Supply Filter

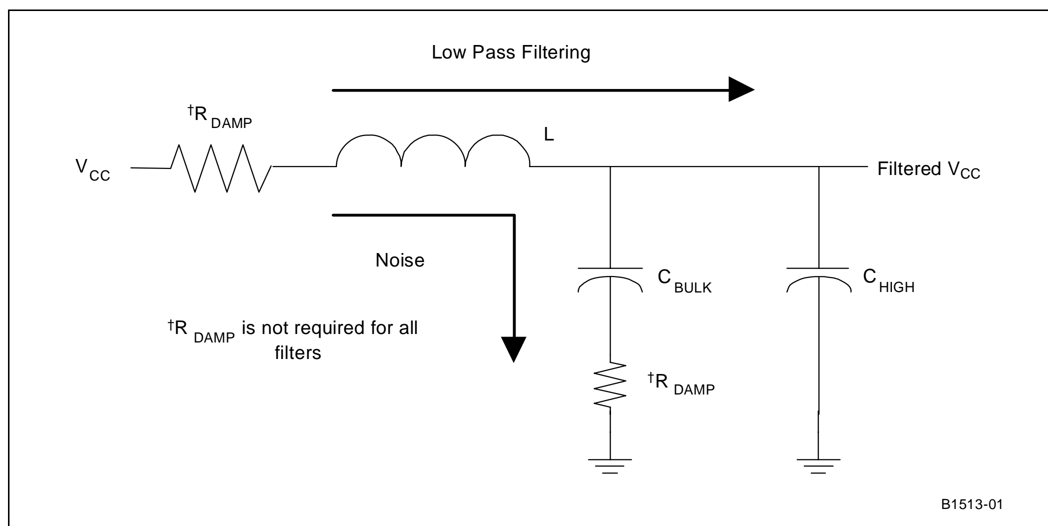


Table 99 presents the analog supply filter requirements.

Table 99. Analog Supply Filter Requirements

Required Intel® 855GME Chipset Filters	Config	Rdamp	Rdamp location	L	Cbulk	Chigh
V_{CCASM}	V1.2S V1.35S (855GME)	None	N/A	1210 1.0 µH DCRmax 0.169 Ωs	100 µF	0603 0.1 µF X5R
V_{CCQSM}	V2.5S	1 Ω	In series with Cbulk	0805 0.68 µH DCRmax 0.80 Ωs	1206 4.7 µF X5R	0603 0.1 µF X5R
$V_{CCAHPLL}$	V_1.2S V_1.35S	None	N/A	None		0603 0.1 µF X5R
$V_{CCADPLLA}$	V_1.2S V_1.35S	1 Ω	In series with inductor	0805 0.10 µH	220 µF	0603 0.1 µF X5R
$V_{CCADPLLB}$	V_1.2S V_1.35S	1 Ω	In series with inductor	0805 0.10 µH	220 µF	0603 0.1 µF X5R
V_{CCADAC}	V1.5S	None	N/A	None	None	0603 0.1 µF X5R 0603 0.01 µF X5R
$V_{CCAGPLL}$	V_1.2S V_1.35S	None	N/A	None	None	0603 0.1 µF X5R
$V_{CCALVDS}$	V1.5S	None	N/A	None	None	0603 0.1 µF X5R 0603 0.01 µF X5R

12.4.5 Intel® 82801DB I/O Controller Hub 4 (ICH4) Decoupling/ Power Delivery Guidelines

12.4.5.1 ICH4 Decoupling

The ICH4 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of decoupling capacitance is added in parallel to the voltage input pins. Intel recommends that the developer use the amount of high-frequency decoupling capacitors specified in table below to ensure that component maintains stable supply voltages. Low-frequency decoupling is dependent on layout and system power supply design. Table 100 presents the Intel® 82801DB I/O Controller Hub 4 (ICH4) decoupling requirements.

Table 100. Intel® 82801DB I/O Controller Hub 4 (ICH4) Decoupling Requirements

Pin Name	Configuration	F	Qty
V_{CC}3_3	Connect to V_{CC}3_3S	0.1 µF	6
V_{CCSUS}3_3	Connect to V_{CC}3_3A	0.1 µF	2
V_{CCLAN}3_3	Connect to V_{CC}3_3	0.1 µF	2
V_CPU_IO	Connect to V_{CCP} (Intel® IMVP-IV)	0.1 µF 1 µF	1 1
V_{CC}1_5	Connect to V_{CC}1_5S	0.1 µF	2
V_{CCSUS}1_5	Connect to V_{CC}1_5A	0.1 µF	2
V_{CCLAN}1_5	Connect to V_{CC}1_5	0.1 µF	2
$V5_{REF}$	Connect to V_{CC}5_REF	0.1 µF	1
$V5_{REF_SUS}$	Connect to V_{CC}5A	0.1 µF	1
V_{CCRTC}	Connect to V_{CC_RTC}	0.1 µF	1
V_{CCHI}	Connect to V_{CC}1_5S	0.1 µF	2
V_{CCPLL}	Connect to V_{CC}1_5S	0.1 µF	1
		0.01 µF	1

NOTE: Capacitors should be placed less than 100 mils from the package.

12.4.6 Hub Interface Decoupling

Refer to Section 8.4 for details.

12.4.7 FWH Decoupling

Place a 0.1 µF capacitor between the V_{CC} supply pins and the V_{SS} ground pins to decouple high-frequency noise, which may affect the programmability of the device. Additionally, place a 4.7 µF capacitor between the V_{CC} supply pins and the V_{SS} ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the VCC supply pins.

12.4.8 General LAN Decoupling

The following are general LAN decoupling recommendations:

- All V_{CC} pins should be connected to the same power supply.
- All V_{SS} pins should be connected to the same ground plane.
- Intel recommends four to six decoupling capacitors, including two 4.7 µF capacitors.
- Place decoupling as close as possible to power pins.

Reserved, NC, and Test Signals 13

The Intel® Pentium® M processor, Intel® Pentium® M processor on the 90 nm process with 2 MB L2 cache, and Intel® 855GM chipset GMCH may have signals listed as "RSVD", "NC", or other names of which the functionality is Intel reserved. The following section contains recommendations on how to handle these Intel reserved signals on the processor or GMCH.

13.1 Intel® Pentium® M Processor/Intel® Celeron® M Processor RSVD Signals

The Intel Pentium M/Celeron® M processors have a total of three TEST, and eight RSVD signals that are Intel reserved in the pin-map. All other RSVD signals are to be left unconnected but should have access to open routing channels for possible future use. The location of the Intel reserved signals in the processor pin-map is listed in Table 101.

Table 101. Processor RSVD and TEST Signal Pin-Map Locations

Signal Name	Ball Name
RSVD (LAI usage)	AF7
RSVD (key)	A1
RSVD	B2
RSVD	C3
RSVD	C14
RSVD (PSI#)	E1
RSVD (former GTLREF1)	E26
RSVD (former GTLREF2)	G1
RSVD (former GTLREF3)	AC1
TEST1	C5
TEST2	F23
TEST3	C16

13.2 Intel® Pentium® M Processor on 90 nm Process with 2 MB L2 Cache RSVD Signals

The Intel Pentium M processor on the 90 nm process with 2 MB L2 cache is pin compatible with the Intel Pentium M/Intel Celeron M processor. Pins C14 and C16 are defined as BSEL1 and BSEL0 respectively for Dothan processor for future platform functionality. They should be left as NC on 855GME chipset based systems.

13.3 Intel 855GME Chipset GMCH RSVD Signals

The Intel 855GME chipset GMCH has a total of 13 RSVD and 12 NC signals that are Intel reserved in the pin-map. The recommendation is to provide test points for all RSVD signals for possible future use. All NC signals should be left as no connects. The location of the Intel reserved signals in the GMCH pin-map is listed in Table 102.

Table 102. Intel 855GME Chipset GMCH RSVD and NC Signal Pin-Map Locations

Signal Name	Ball Name
AJ29	NC
AH29	NC
B29	NC
A29	NC
AJ28	NC
A28	NC
AA9	NC
AJ4	NC
AJ2	NC
A2	NC
AH1	NC
B1	NC
D7	RSVD
F12	RSVD
D12	RSVD
B12	RSVD
AA5	RSVD
L4	RSVD
F3	RSVD
D3	RSVD
B3	RSVD
F2	RSVD
D2	RSVD
C2	RSVD
B2	RSVD

Schematic Checklist Summary 14

The following checklist provides design recommendations and guidance for Pentium® M processor/Celeron® M processor systems with the Intel® 855GME chipset.

The schematic checklist is a tool used to ensure that design recommendations detailed in this Platform Design Guide have been followed prior to schematic reviews. The items contained in this checklist attempt to address important connections and critical supporting circuitry; however, **it is not a complete list**. For complete design recommendations, refer to the main content of this document (referred to as the Platform Design Guide) and the appended Customer Reference Board (CRB) schematics. The information in this guide is subject to change.

Note: Unless otherwise specified the default tolerance on resistors is ± 5%.

14.1 Pentium® M Processor/Celeron® M Processor Checklist

14.1.1 Connection Recommendations

Table 103 presents the connection recommendations.

Table 103. Connection Recommendations (Sheet 1 of 3)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	√
A20M#				Point-to-point connection to the Intel® 82801DB I/O Controller Hub 4 (ICH4), (A20M# signal).	
BR0#				Point-to-point connection to GMCH (BREQ0# signal).	
COMP0, COMP2	27.4 Ω ± 1% pull-down to GND			Resistor placed within 0.5 inch of processor pin. Trace should be 27.4 Ω ± 15%.	
COMP1, COMP3	54.9 Ω ± 1% pull-down to GND			Resistor placed within 0.5 inch of processor pin. Trace should be 55 Ω ± 15%.	
DPSLP#	4.7 KΩ pull-up to V_{CCP} at CPU 1 KΩ pull-up to V_{CCP} at GMCH			Used only with the ICH4-M. The ICH4 does not provide this signal.	
FERR#	56 Ω pull-up to V_{CCP}	56 Ω from pull-up to ICH4 pin		Point-to-point connection to ICH4 (FERR# signal), with pull-up resistor and series resistor placed by the ICH4.	

Table 103. Connection Recommendations (Sheet 2 of 3)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	√
GTLREF	1 KΩ ± 1% pull-up to V_{CCP} 2 KΩ ± 1% pull-down to GND			Voltage divider should be placed within 0.5 inch of processor pin.	
IERR#	56 Ω pull-up to V_{CCP}			IERR# is a 1.05 V signal. Voltage translation logic and/or series resistor may be required if used.	
INIT#			R1 = 1.3 KΩ R2 = 330 Ω Rs = 330 Ω	Point-to-point connection to the ICH4 (INIT# signal). Voltage translation circuit is required if connecting to FWH. Signal is T-split from the ICH4 to FWH. Refer to Figure 132.	
IGNNE#				Point-to-point connection to the ICH4 (IGNNE# signal).	
LINT0				Point-to-point connection to the ICH4 (INTR signal).	
LINT1				Point-to-point connection to the ICH4 (NMI signal).	
PROCHOT#	56 Ω pull up to V_{CCP}		R1 = 1.3 KΩ R2 = 330 Ω Rs = 330 Ω	PROCHOT# is a V_{CCP} signal. Voltage translation logic may be required if used. **When Voltage Translation is Required:** Driver isolation resistor (Rs) should be placed at the beginning of the T-split to the system receiver. Refer to Figure 133.	
PSI#				May be left as not connected (NC) if not used for Intel® IMVP.	
PWRGOOD	330 Ω pull-up to V_{CCP}			Point-to-point connection to the ICH4, with resistor placed by the processor.	
RESET#	220 Ω ± 5% pull-up to V_{CCP} WHEN USING ITP700FLEX	22.6 Ω ± 1% from pull-up to ITP700FLEX		**When ITP700FLEX is Not Used:** Point-to-point connection to GMCH (CPURST# signal). **When ITP700FLEX is Used:** RESET# connects from processor to GMCH (CPURST# signal) and then forks out to ITP700FLEX, with pull-up and series damping resistor placed next to ITP.	
SLP#				Point-to-point connection to the ICH4 (CPUSLP# signal).	
SMI#				Point-to-point connection to the ICH4 (SMI# signal).	
STPCLK#				Point-to-point connection to the ICH4 (STPCLK# signal).	

Table 103. Connection Recommendations (Sheet 3 of 3)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	√
TEST[3:1]	1 KΩ pull-down to GND (default: no stuff)			For each signal, stuffing option for pull-down should be provided for testing purposes. For normal operation, leave the resistors unpopulated.	
THERMTRIP#	56 Ω pull-up to V_{CCP}	56 Ω from pull-up to the ICH4 pin		Point-to-point connection to an ICH4 (THERMTRIP# signal), with pull-up and series resistors placed by ICH4. THERMTRIP# is a V_{CCP} signal. When connecting to device other than an ICH4, voltage translation logic may be required.	
V_{CC}[72:1]	Connect to CPU_CORE			From Intel® IMVP-IV specification power supply.	
V_{CCA}[3:0]	Connect to V_{1P8}			The Low Voltage Intel Pentium M Processor on the 90 nm process with 2 MB L2 cache will support a V_{CCA} of 1.8 V or 1.5 V.	
V_{CC}1_05 [25:1]	Connect to V_{CCP}				
$V_{CCSENSE}$, $V_{SSSENSE}$	54.9 Ω ± 1% pull-down to GND (Default: no stuff)			For each signal, stuffing option for pull-down should be provided for testing purposes. Also, a test point for differential probe ground should be placed between the two resistors. For normal operation, leave the resistors unpopulated.	
GND[192:1]	Connect to GND				

Figure 132 illustrates the routing illustration for INIT# for the Pentium M processor/Celeron M processor.

Figure 132. Routing Illustration for INIT# for the Pentium® M Processor/Celeron® M Processor

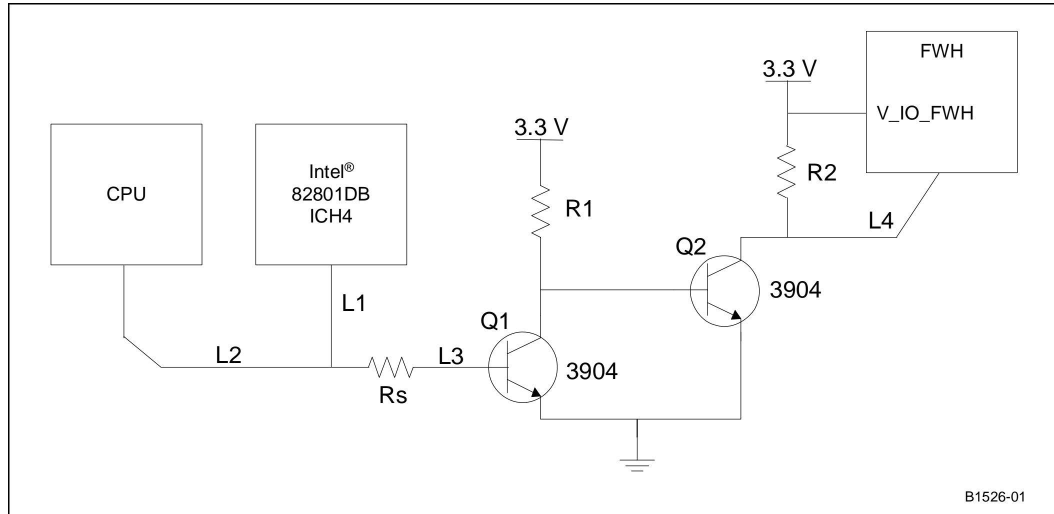
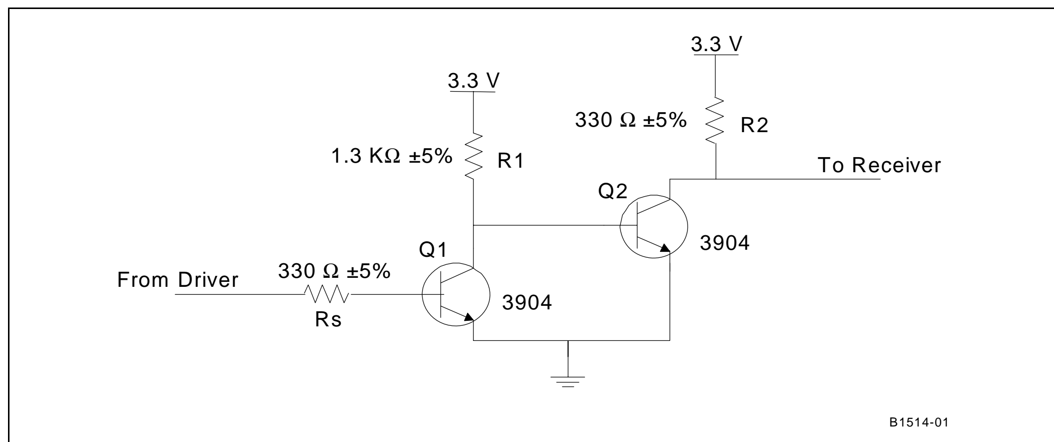


Figure 133 illustrates the voltage translation circuit for PROCHOT# for the Pentium M processor/ Celeron M Processor.

Figure 133. Voltage Translation Circuit for PROCHOT# for the Pentium® M Processor/ Celeron® M Processor



14.1.2 In Target Probe (ITP)

Table 104 presents the In Target Probe (ITP) information.

Table 104. In Target Probe (ITP)

Pin Name	System Pull-up/Pull-down	Series Termination Resistor (Ω)	Notes	√
BPM[5:0]#			Connect to processor directly.	
DBR#	150-240 Ω pull-up to V_{CC3}		When using ITP on interposer card, DBR# should also be connected to DBR# pin at the processor. The 150-240 Ω pull-up resistor should be placed within 1 ns of the ITP700FLEX connector. The CPU should **not** be power cycled when DBR# is asserted.	
RESET#	220 Ω ± 5 % pull-up to V_{CCP} WHEN USING ITP700FLEX	22.6 Ω ± 1% from pull-up to ITP700FLEX	Refer to the RESET# notes in Table 103.	
FBO			Connect to TCK pin of processor. Refer to Section 4.3.1 for layout details.	
TCK	27.4 Ω ± 1% pull-down to GND		Connect to processor, with resistor placed by ITP. Refer to Section 4.3.1 for layout details.	
TDI	150 Ω pull-up to V_{CCP}		Connect to processor with resistor placed by the processor. Refer to Section 4.3.1 for layout details.	
TDO	54.9 Ω ± 1% pull-up to V_{CCP}	22.6 Ω ± 1% from pull-up to ITP700FLEX	Connect to processor with resistors placed by ITP. When ITP not used, this signal may be left as NC.	
TMS	39.2 Ω ± 1% pull-up to V_{CCP}		Connect to processor with resistor placed by ITP.	
TRST#	680 Ω pull-down to GND		Connect to processor with resistor located anywhere between processor and ITP.	
VTAP, VTT[1:0]	Connect to V_{CCP}		One 0.1 µF decoupling cap near ITP is required. Refer to Section 4.3.1 for layout details.	

14.1.3 Decoupling Recommendations

14.1.3.1 V_{CCP} (I/O)

Table 105 presents the V_{CCP} (I/O) decoupling recommendations.

Table 105. V_{CCP} (I/O) Decoupling Recommendations

Description	C, µF	ESR, mΩ	ESL, nH	Notes	√
Low Frequency Decoupling (Polymer Covered Tantalum - POSCAP, Neocap, KO Cap)	2 x 150 µF	42 mΩ (typ)/2	2.5 nH/2	Refer to the *Intel® Pentium® M Processor Datasheet, Intel® Pentium® M Processor on the 90 nm process with 2 MB L2 cache Datasheet, and Intel® Celeron® M Processor Datasheet* for more information.	
High Frequency Decoupling (0603 MLCC, >= X7R)	10 x 0.1 µF	16 mΩ (typ)/10	0.6 nH/10		

14.1.3.2 V_{CCA} (PLL)

Table 106 presents the V_{CCA} (PLL) decoupling recommendations.

Table 106. V_{CCA} (PLL) Decoupling Recommendations

Description	C, µF	Notes	√
Mid Frequency Decoupling (Polymer Covered Tantalum - POSCAP, Neocap, KO Cap)	4 x 10 µF	Place one 10 µF and one 0.01 µF for each V_{CCA} pin.	
High Frequency Decoupling (0603 MLCC, >= X7R). Place next to the Pentium M processor.	4 x 0.01 µF	Place one 10 µF and one 0.01 µF for each V_{CCA} pin.	

14.1.3.3 V_{CC} (CORE)

Table 107 presents the V_{CC} (CORE) decoupling recommendations.

Table 107. V_{CC} (CORE) Decoupling Recommendations (Sheet 1 of 2)

Option	Description	C, µF	ESR, mΩ	ESL, nH	√
#1	Low-Frequency Decoupling (Polymer Covered Tantalum – POSCAP, Neocap, KO Cap)	12 x 150 µF	36 mΩ (typ)/12	2.5 nH/12	

NOTES:
1. Decoupling guidelines are recommendations based on Intel reference board design. The Intel Customer Reference Board uses option #4. This is the preferred recommendation for decoupling.
2. When deciding on overall decoupling solution, customers may need to take layout and PCB board design into consideration.
3. Option #4 is to be used with small footprint (100 mm^2 or less) 0.36 µH ± 20% inductors.

Table 107. V_{CC} (CORE) Decoupling Recommendations (Sheet 2 of 2)

Option	Description	C, µF	ESR, mΩ	ESL, nH	√
	Mid-Frequency Decoupling (0612 MLCC, X5R or better)	15 x 2.2 µF	5 mΩ (typ)/15	0.2 nH/15	
#2	Low-Frequency Decoupling (1206 MLCC, X5R or better)	40x10 µF	5 mΩ (typ)/40	1.2 nH/40	
	Mid-Frequency Decoupling (0612 MLCC, X5R or better)	15 x 2.2 µF	5 mΩ (typ)/15	0.2 nH/15	
#3	Low Frequency Decoupling (Polymer Covered Aluminum – SP Cap, A0 Cap)	5 x 330 µF	15 mΩ (max)/5	3.5 nH/5	
	Low Frequency Decoupling (1206 MLCC, >= X5R)	25 x 10 µF	5 mΩ (typ)/25	1.2 nH/25	
	Mid Frequency Decoupling (0612 MLCC, >= X5R)	15 x 2.2 µF	5 mΩ (typ)/15	0.2 nH/15	
#4 (Note 1)	Low-Frequency Decoupling (Polymer Covered Aluminum – SP CAP, AO Cap)	4 x 220 µF	12 mΩ (max)/4	3.5 nH/4	
	Mid-Frequency Decoupling (0805 MLCC>= X5R)	35 x 10 µF	5 mΩ (typ)/35	0.6 nH/35	

NOTES:
1. Decoupling guidelines are recommendations based on Intel reference board design. The Intel Customer Reference Board uses option #4. This is the preferred recommendation for decoupling.
2. When deciding on overall decoupling solution, customers may need to take layout and PCB board design into consideration.
3. Option #4 is to be used with small footprint (100 mm^2 or less) 0.36 µH ± 20% inductors.

14.2 CK-408 Clock Checklist

14.2.1 Connection Recommendations

Table 108 presents the CK-408 connection recommendations.

Table 108. CK-408 Connection Recommendations (Sheet 1 of 2)

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	√
3V66_[0] 3V66_[1]*		33 Ω ± 5%	When the signal is used, one 33 Ω series resistor is required. When the signal is NOT used, it should be left as NC or connected to a test point. *Two possible topologies for 3V66_1: • Use directly for GMCH's DREFSSCLK. • Use as input to an SSC device with SSC output to GMCH's DREFSSCLK.	
3V66_[4:2]		33 Ω ± 5%	The Intel CRB routes 3V66[2] (pin 21) to GCLKIN on GMCH. The other two signals route to ICH4 (CLK66) and AGP connector (AGPCLK).	

Table 108. CK-408 Connection Recommendations (Sheet 2 of 2)

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	√
CPU[0], CPU[0]# CPU[1], CPU[1]# CPU[2], CPU[2]#	49.9 Ω ± 1% pull- down to GND	33 Ω ± 5%	Use one pair for the processor and another pair for GMCH. When onboard ITP is implemented, the third pair of clock signals is used for the ITP connector. Otherwise, it may be routed to the dedicated ITP clock pins on the processor socket. Refer to Chapter 11 for routing requirements.	
DOT_48MHZ		33 Ω ± 5%	Connect to GMCH's DREFCLK.	
I_{REF}	475 Ω ± 1% pull-down to GND		Adjusts IREF to 2.32 mA.	
MULT[0]	10 KΩ pull-up to V_{CC}3_CLK (V_{CC}3-CLK on CRB implements additional filtering for CK-408 power.)		Sets multiplication factor to six.	
PCI[6:0]		33 Ω ± 5%	Connect to various PCI devices and other 33 MHZ clock inputs for devices such as FWH and SIO (LPC). Use one clock for the ICH4. Unused clock pins should be left as NC or connected to a test point.	
PCIF[2:0]		33 Ω ± 5%		
PWRDWN#	Terminate to V_{CC}3_CLK through 1 K Ω resistor.		The Intel CRB does not support S1M state.	
REF0		33 Ω ± 5%	This is the 14.318 MHz clock reference signal for the ICH4, SIO and LPC. Each receiver requires one 33 Ω series resistor.	
SEL[2:1]	Intel CRB uses 1 KΩ pull-downs to GND.		Configured for un-buffered mode, 100 MHZ host clock, 0.710 mV swing.	
SEL[0]	Intel CRB uses 1 KΩ pull-up to V_{CC}3_CLK.			
USB_48MHZ		33 Ω ± 5%	Connect to the ICH4's 48 MHz clock input.	
XTAL_IN, XTAL_OUT	Terminate each pin to GND through a 10 pF ± 5% capacitor.		Connect to a 14.318 MHz crystal, placed within 500 mils of CK-408.	
V_{DD}[7:0], V_{DDA}, V_{DD_48MHZ}	Connect to V_{CC}3.		Refer to clock vendor datasheet for decoupling info.	
V_{SS}[5:0], V_{SSA}, V_{SS_48MHZ}	Connect to GND.			
V_{SSIREF}	Connect to GND.			

14.3 Intel® 855GME Chipset GMCH (82855GME) Checklist

14.3.1 System Memory

14.3.1.1 GMCH System Memory Interface Checklist

Table 109 presents the GMCH system memory interface checklist.

Table 109. GMCH System Memory Interface Checklist (Sheet 1 of 2)

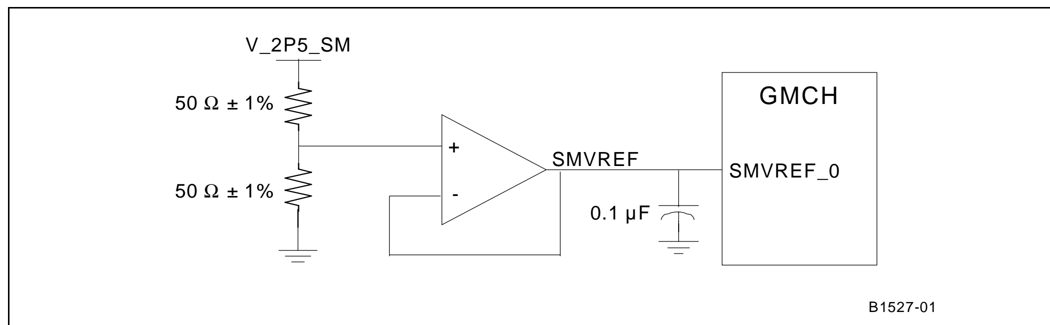
Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	√
SRCVENIN#			This signal should be routed to a via next to ball and left as a NC.	
SRCVENOUT#			This signal should be routed to via next to ball and left as a NC.	
SBA[1:0]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0 and DIMM 1.	
SCAS#	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0 and DIMM 1.	
SRAS#	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0 and DIMM 1.	
SWE#	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0 and DIMM 1.	
SCKE[1:0]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0	
SCKE[3:2]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 1	
SCS#[1:0]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0	
SCS#[3:2]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 1	
SDQ[63:0]	56 Ω pull-up to V_1P25_MEMVTT	10 Ω	Connect to DIMM 0 and DIMM 1.	
SDM[7:0]	56 Ω pull-up to V_1P25_MEMVTT	10 Ω	Connect to DIMM 0 and DIMM 1.	
SDQS[7:0]	56 Ω pull-up to V_1P25_MEMVTT	10 Ω	Connect to DIMM 0 and DIMM 1.	
SDQ[71:64]	56 Ω pull-up to V_1P25_MEMVTT	10 Ω	When ECC support is not implemented, SDQ[71:64], SDM8, and SDQS8 should be left as NC. For ECC support, these signals connect to DIMMs.	
SDM8	56 Ω pull-up to V_1P25_MEMVTT	10 Ω	When ECC support is not implemented, SDQ[71:64], SDM8, and SDQS8 should be left as NC. For ECC support, these signals connect to DIMMs.	

Table 109. GMCH System Memory Interface Checklist (Sheet 2 of 2)

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	√
SDQS8	56 Ω pull-up to V_1P25_MEMVTT	10 Ω	When ECC support is not implemented, SDQ[71:64], SDM8, and SDQS8 should be left as NC. For ECC support, these signals connect to DIMMs.	
SMA[12:6,3,0]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0 and DIMM 1.	
SMA[5,4,2,1]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0.	
SMAB[5,4,2,1]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 1.	
SCK0, SCK0# SCK1, SCK1# SCK2, SCK2#			These clock signals route differentially directly to DIMM 0. Alternatively, refer to Section 5.5.2 for information regarding GMCH clock routing flexibility.	
SCK3, SCK3# SCK4, SCK4# SCK5, SCK5#			These clock signals route differentially directly to DIMM 1. Alternatively, refer to Section 5.5.2 for information regarding GMCH clock routing flexibility.	
SMVREF_0	Resistor divider to V_2P5_SM consists of two identical resistors (50 Ω – 150 Ω 1%)		Signal voltage level = V_2P5_SM/ 2. Optionally, the Intel CRB may support a buffer to provide the necessary current and reference voltage to SMVREF. Refer to Figure 134. Place a 0.1 µF cap by GMCH, DIMM 0, and DIMM 1 pins. Refer to Section 12.4.3.2 for more information.	
SMVSWINGL	604 Ω 1% pull-up to V_2P5_SM 150 Ω 1% pull-down to GND		Signal voltage level = 1/5 * V_2P5_SM. Need 0.1 µF cap at the GMCH pin.	
SMVSWINGH	150 Ω 1% pull-up to V_2P5_SM 604 Ω 1% pull-down to GND		Signal voltage level = 4/5 * V_2P5_SM. Need 0.1 µF cap at the GMCH pin.	
SMRCOMP	60.4 Ω 1% pull-up to V_2P5_SM 60.4 Ω 1% pull-down to GND		Signal voltage level = 1/2 * V_2P5_SM. Need 0.1 µF cap to GND near the voltage divider.	

Figure 134 illustrates the reference voltage level for SMVREF.

Figure 134. Reference Voltage Level for SMVREF



14.3.1.2 DDR DIMM Interface Checklist

Table 110 presents the DDR DIMM interface checklist.

Table 110. DDR DIMM Interface Checklist

Pin Name	Configuration	Notes	√
A13/NC (pin 103)		Signal may be left as NC (Not Connected).	
CS[3:2]# (pin163, 71)		Signal may be left as NC.	
BA2 (pin 113)		Signal may be left as NC.	
V_{REF} (pin 1)	Connected to Intel® 82855GME SMVREF signal	Signal voltage level = V_2P5_SM/ 2. Place a 0.1µF cap by GMCH, DIMM 0, and DIMM 1 pins.	
V_{DD}[9:1]	Connect to V_2P5_SM	Power must be provided during S3.	
V_{DDSPD}	Connect to V_2P5_CORE		
SA[2:1]	Connect to GND	These lines are used for strapping the SPD address for each DIMM.	
SA0	DIMM 0: connect to GND DIMM 1: connect to V_2P5_SM	These lines are used for strapping the SPD address for each DIMM.	
V_{SS}[22:1]	Connect to GND		
RESET#(DU) (pin 10)		Signal may be left as NC.	
SDA/SCL	Connect to the ICH4 SMBUS and SMLINK through isolation circuitry.	Refer to Section 9.9 for more information.	
WP (pin 90)		Signal may be left as NC.	
NC (FETEN) (pin 167)		Signal may be left as NC.	
V_{DDQ}[16:1]	Connect to V_2P5_SM		
V_{DDID} (pin 82)		Signal may be left as NC.	
NC[4:1] (pins 9,101,102,173)		Signal may be left as NC.	

14.3.1.3 DIMM Decoupling Recommendation Checklist

Table 111 presents the DIMM decoupling recommendation checklist.

Table 111. DIMM Decoupling Recommendation Checklist

Pin Name	F	Qty	Notes	√
V_1P25_MEMVTT	0.1 µF 4.7 µF† 470 µF	(55†) 3 4	Place one 0.1 µF cap close to every two pull-up resistors terminated to V_1P25_MEMVTT (VTT for DDR signal termination). Place two 4.7 µF caps at either end of the VTT island and one near the center. Four 470 µF capacitors may be placed as bulk decoupling. Refer to Section 12.4.2.2 for more information.	
V_2P5_SM	0.1 µF 100-150 µF (220 µF†) (100 µF†)	9 (15†) 4 (3†) (1†)	Intel recommends a minimum of nine high frequency caps to be placed between the DIMMS. A minimum of four low frequency caps are required.	

† Used on Intel CRB.

14.3.2 Front Side Bus (FSB) Checklist

Table 112 presents the FSB Checklist.

Table 112. FSB Checklist (Sheet 1 of 2)

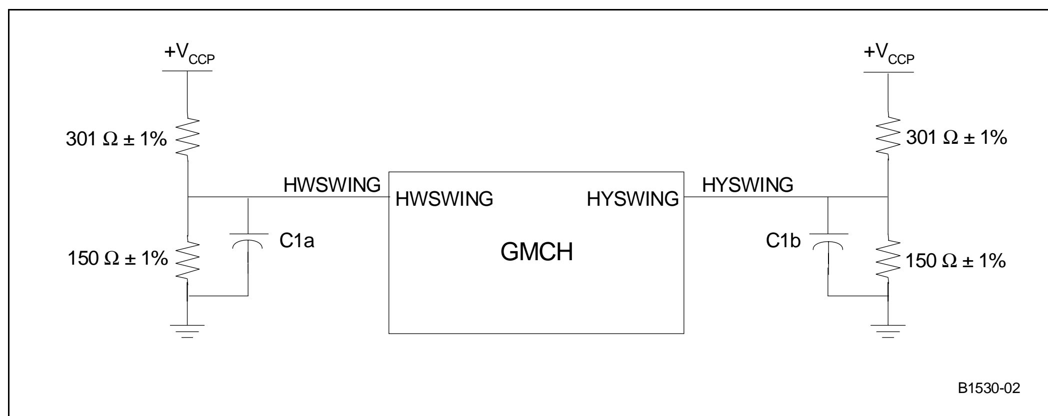
Pin Name	System Pull-up/Pull-down	Notes	√
ADS#		Connect directly to processor (ADS# signal).	
HTRDY#		Connect directly to processor (TRDY# signal).	
DRDY#		Connect directly to processor (DRDY# signal).	
DEFER#		Connect directly to processor (DEFER# signal).	
HITM#		Connect directly to processor (HITM# signal).	
HIT#		Connect directly to processor (HIT# signal).	
HLOCK#		Connect directly to processor (LOCK# signal).	
BREQ0#		Connect directly to processor (BR0# signal).	
BNR#		Connect directly to processor (BNR# signal).	
BPRI#		Connect directly to processor (BPRI# signal).	
DBSY#		Connect directly to processor (DBSY# signal).	
RS[2:0]#		Connect directly to processor (RS[2:0]# signals).	
HA[31:3]#		Connect directly to processor (A[31:3]# signals).	
HREQ[4:0]#		Connect directly to processor (REQ[4:0]# signals).	
HADSTB[1:0]#		Connect directly to processor (HADSTB[1:0]# signals).	
BCLK, BCLK#	Refer to the CK408 Checklist for CPU[0], CPU[0]#, CPU[1], CPU[1]#, CPU[2], and CPU[2]#.	Connect to CK408.	

Table 112. FSB Checklist (Sheet 2 of 2)

Pin Name	System Pull-up/Pull-down	Notes	√
HDSTBN[3:0]#		Connect directly to processor (DSTBN[3:0]# signals).	
HDSTBP[3:0]#		Connect directly to processor (DSTBP[3:0]# signals).	
DINV[3:0]#		Connect directly to processor (DINV[3:0]# signals).	
CPURST#	54.9 Ω 1% pull-up to V_{CCP}. 22.6, 1% series to ITP (pin 12). Refer to the Pentium M Processor Checklist for RESET#.	Connect to processor (RESET# signal) and ITP (if implemented).	
HD[63:0]#		Connect directly to processor (D[63:0]# signals).	
DPWR#		Connect directly to processor (DPWR# signal).	
DPSLP#	1 KΩ pull-up to V_{CCP} at GMCH. 4.7 KΩ pull-up to V_{CCP} at CPU.	Used only with the ICH4-M. The ICH4 does not provide this signal.	
HXSWING	301 Ω 1% pull-up to V_{CCP} 150 Ω 1% pull-down to GND	Signal voltage level = 1/3 of V_{CCP}. C1a = 0.1 µF. C1b=0.1 µF. Trace should be 10 mil wide with 20 mil spacing. Refer to Figure 135.	
HYSWING	301 Ω 1% pull-up to V_{CCP} 150 Ω 1% pull-down to GND	Signal voltage level = 1/3 of V_{CCP}. C1a=0.1 µF. C1b=0.1 µF. Trace should be 10-mil wide with 20 mil spacing. Refer to Figure 135.	
HXRCOMP	27.4 Ω 1% pull down to GND	One pull-down resistor where trace should be 10 mil wide with 20 mil spacing.	
HYRCOMP	27.4 Ω 1% pull down to GND	One pull-down resistor where trace should be 10 mil wide with 20 mil spacing.	
HDVREF[2:0]	49.9 Ω 1% pull-up to V_{CCP} 100 Ω 1% pull-down to GND	Signal voltage level = 2/3 of V_{CCP}. Need one 0.1 µF cap and one 1 µF cap near voltage divider.	
HAVREF	49.9 Ω 1% pull-up to V_{CCP} 100 Ω 1% pull-down to GND	Signal voltage level = 2/3 of V_{CCP}. Need one 0.1 µF cap.	
HCCVREF	49.9 Ω 1% pull-up to V_{CCP} 100 Ω 1% pull-down to GND	Signal voltage level = 2/3 of V_{CCP}. Need one 0.1 µF cap and one 1 µF cap for voltage divider.	

Figure 135 illustrates the Intel 855GME Chipset HXSWING and HYSWING reference voltage generation circuit.

Figure 135. Intel® 855GME Chipset HXSWING and HYSWING Reference Voltage Generation Circuit



14.3.3 Hub Interface Checklist

Table 113 presents the hub interface checklist.

Table 113. Hub Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
HI[10:0]		Connect to the ICH4 (HI[10:0] signals). Refer to Section 8.2.1 for more information.	
HLSTB (S)		Connect to the ICH4 (HL_STBS signal).	
HLSTB# (F)		Connect to the ICH4 (HL_STBF signal).	
HLVREF	Refer to Section 8.3.	Signal voltage level = 0.35 V ± 8%.	
PSWING	Refer to Section 8.3.	Signal voltage level = 2/3 of V1P35_GMCH or 0.8 V ± 8%.	
HLRCOMP	37.4 Ω 1% pull-up to V1P35_GMCH	Refer to Section 8.1 for more information.	

14.3.4 Graphics Interfaces Checklist

14.3.4.1 Low Voltage Digital Signalling (LVDS) Checklist

Table 114 presents the LVDS checklist.

Table 114. LVDS Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
LIBG	1.5 KΩ 1% pull-down to GND	†	
IYAP[3:0]/ IYAM[3:0] IYBP[3:0]/ IYBM[3:0]		The Intel CRB routes these data pairs directly to a 30-pin dual channel LVDS connector.†	
ICLKAP/ ICLKAM ICLKBP/ ICLKBM		†	
DDCPCLK, DDCPDATA	2.2 k to 10 k pull-up to 3.3 V	LVDS Panel DDC Clock/Data pair to collect digital display EDID information.†	
PANELVDDEN	100 k pull-down	Used for LVDS Panel Power control.†	
PANELBKLTEN	100 k pull-down	Used for LVDS Panel backlight enable.†	
PANELBKLTCTL	100 k pull-down	Used for LVDS Panel backlight brightness control.†	
† Can be left as NC if not used			

14.3.4.2 Digital Video Out (DVO) Checklist

Table 115 presents the DVO checklist.

Table 115. DVO Checklist (Sheet 1 of 2)

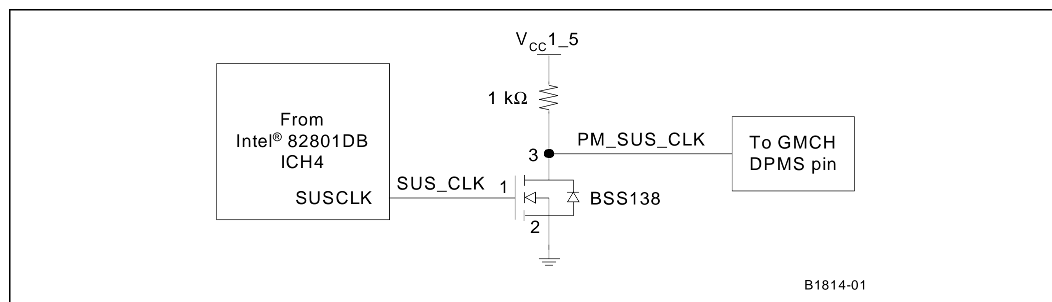
Pin Name	System Pull-up/Pull-down	Notes	√
DVORCOMP	40.2 Ω 1% pull-down to GND	Trace should be 10-mil wide with 20-mil spacing.	
GVREF	1 KΩ 1% pull-up to V_1P5_CORE 1 KΩ 1% pull-down to GND	Signal voltage level = 1/2 of V_1P5_CORE. Need 0.1 μF cap at GMCH pin.	
DVOCD[11:0]		When unused, these signals may be left as NC. DVO Routing is to ADD connector on Intel CRB. For AGP these signals are: GAD[29:19] and GCBE#. See Chapter 3.6.3 of the 855GME datasheet for exact assignment.	
DVOCCLK, DVOCCLK#		When unused, these signals may be left as NC. For AGP these signals are: GAD_STB1, GAD_STB1#.	
DVOCHSYNC		When unused, these signals may be left as NC. For AGP this signal is: GAD[17].	

Table 115. DVO Checklist (Sheet 2 of 2)

Pin Name	System Pull-up/Pull-down	Notes	√
DVOCVSYNC		When unused, these signals may be left as NC. For AGP this signal is: GAD[16].	
DVOCBLANK#		When unused, these signals may be left as NC. For AGP this signal is: GAD[18].	
DVOCFLDSTL	100 KΩ pull-down to GND	Pull-down resistor required only if signal is unused (10 K-100 K). It is up to DVO device to drive this signal. For AGP this signal is: GAD[31].	
DVOBCINTR#	100 KΩ pull-up to V_1P5_CORE	Pull-up resistor required only if signal is unused (10 K-100 K). It is up to the DVO device to drive this signal. For AGP this signal is: GAD[30].	
DVOBCCLKINT	100 KΩ pull-down to GND	Pull-down resistor required only if signal is unused (10 K-100 K). It is up to the DVO device to drive this signal. For AGP this signal is: GAD[13].	
DVOBD[11:0]		When this port is unused, it may be left as NC. For AGP these signals are: GAD[12:2]. Refer to Chapter 3.6.3 of the 855GME datasheet for exact assignment.	
DVOBCLK, DVOBCLK#		When this port is unused, it may be left as NC. For AGP these signals are: AD_STB0, AD_STB0#.	
DVOBHSYNC		When this port is unused, it may be left as NC. For AGP this signal is: GAD[0].	
DVOBVSYNC		When this port is unused, it may be left as NC. For AGP this signal is: GAD[1].	
DVOBBLANK#		When this port is unused, it may be left as NC. For AGP this signal is: GCBE#1.	
DVOBFLDSTL (pin M2)	100 KΩ pull-down to GND	Pull-down resistor required only if this signal is unused (10K-100K). For AGP this signal is: GAD[14].	
MI2CCLK, MI2CDATA	2.2 KΩ pull-up to V_1P5_CORE	Pull-up resistor required on each signal even if they are unused (2.2 K-100 K). This signal is 1.5 V tolerant. It may require voltage translation circuit. For AGP these signals are: GIRDY#, GDEVSEL#.	
MDVICLK, MDVIDATA	2.2 KΩ pull-up to V_1P5_CORE	Pull-up resistor required on each signal even if they are unused (2.2 K-100 K). This signal is 1.5 V tolerant. It may require voltage translation circuit. For AGP these signals are: GTRDY#, GFRAME#.	
MDDCCLK, MDDCDATA	2.2 KΩ pull-up to V_1P5_CORE	Pull-up resistor required on each signal even if they are unused (2.2 K-100 K). This signal is 1.5 V tolerant. It may require voltage translation circuit. For AGP these signals are: GSTOP#, GAD[15].	
ADDID[6:0]		Leave as NC. For AGP these signals are: GSBA[6:0].	
ADDID7	1 KΩ pull-down to GND if DVO device is onboard	When DVO interface is not used, this signal may be left as NC. Otherwise, pull-down is needed. For AGP this signal is: GSBA[7].	
GCLKIN	33 Ω series at CK408	Connect to CK408, 66 MHz clock.	
DVODETECT	1 KΩ pull-up to V_1P5_CORE if DVO interface is unused	When DVO interface is used, leave as NC. This signal has internal pull-down. For AGP this signal is: GPAR.	
DPMS		Connect to 1.5 V version of the ICH4's SUSCLK or a clock that runs during S1. For AGP this signal is: GPIPE.	

Figure 136 illustrates the DPMS clock implementation.

Figure 136. DPMS Clock Implementation



14.3.4.3 Digital-to-Audio Converter (DAC) Checklist

Table 116 presents the DAC checklist.

Table 116. DAC Checklist (Sheet 1 of 2)

Pin Name	System Pull-up/Pull-down	In Series	Notes	√
REFSET	124-137 Ω 1% pull-down to GND		137 Ω used on Intel CRB.	
RED #	Connect to GND.		Need to connect to RED's return path.	
BLUE #	Connect to GND.		Need to connect to BLUE's return path.	
GREEN#	Connect to GND.		Need to connect to GREEN's return path.	
RED	On GMCH side of ferrite bead: 75 Ω 1% pull-down to GND, 3.3 pF cap to GND, ESD diode protection for V_1P5_CORE On VGA side of ferrite bead: 3.3 pF cap to GND	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
BLUE	On GMCH side of ferrite bead: 75 Ω 1% pull-down to GND, 3.3 pF cap to GND, ESD diode protection for V_1P5_CORE. On VGA side of ferrite bead: 3.3 pF cap to GND	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	

† Value used on Intel CRB.

Table 116. DAC Checklist (Sheet 2 of 2)

Pin Name	System Pull-up/Pull-down	In Series	Notes	√
GREEN	On GMCH side of ferrite bead: 75 Ω 1% pull-down to GND, 3.3 pF cap to GND, ESD diode protection for V_1P5_CORE On VGA side of ferrite bead: 3.3 pF cap to GND	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
HSYNC	33 pF cap to GND at connector (470 pF†)	39 Ω	Unidirectional buffer is required. Refer to Section 6.1.6 for more information.	
VSYNC	33 pF cap to GND at connector (470 pF†)	39 Ω	Unidirectional buffer is required. Refer to Section 6.1.6 for more information.	

† Value used on Intel CRB.

14.3.5 Miscellaneous Signal Checklist

Table 117 presents the miscellaneous signal checklist.

Table 117. Miscellaneous Signal Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
RSTIN#		Reset: (I) Connect to the ICH4 PCI_RST# (if ~4 loads). May need to be buffered.	
PWROK		Power OK: (I) 3 V signal. Indicates GMCH power is stable.	
AGPBUSY#	8.2k pull-up to $V_{CC}3$	AGP Busy: (O)	
DDCACLK, DDCADATA	2.2k pull-up to $V_{CC}5$ after translation logic	CRT DDC Clock/Data Needs to be translated from 3 V to 5 V.	
EXTTS_0	10 KΩ 1% pull-up to $V_{CC}3$		
DPWR# (pin AA22)		Connect directly to the processor.	
LCLKCTLB		Used for SSC chip data control on Intel CRB. Leave this signal as NC if not used.	
LCLKCTLA		Used for SSC chip data control on Intel CRB. Leave as NC if not used.	
DREFCLK	33 Ω series at CK408.	DAC Display Clock Input Connect to CK408 48 MHz DOT CLK (pin 38).	
DREFSSCLK	33 Ω series at CK408.	LVDS SSC Clock Input. 48 MHz or 66 MHz, SSC or non-SSC. Connect to CK408 3V66_1/VCH CLK (pin 35). Optional to connect to SSC chip for enhanced spread.	
GST2 (C2) GST1 (C3) GST0 (C4)	Leave as NC or 1 KΩ pull-up to V_1P5_CORE	These pins have internal pull-down and can be left as No Connects, since the BIOS will program the memory and graphics frequencies accordingly.	

14.3.6 GMCH Decoupling Recommendations Checklist

Table 118 presents the GMCH decoupling recommendations checklist.

Table 118. GMCH Decoupling Recommendations Checklist (Sheet 1 of 2)

Pin Name	Configuration	F	Qty	Notes	√
V_{CC}[18:1]	Connect to V1P35_GMCH.	0.1 µF 150 µF 10 µF	4 2 1	Bulk decoupling is based on VR solutions used on CRB design.	
V_{TTLF}[21:1]	Connect to V_{CCP}	0.1 µF 270 µF 10 µF	3 1 1	Bulk decoupling is based on VR solutions used on CRB design.	

NOTE: Decoupling guidelines are recommendations based on our reference board design. Customers may need to take layout and PCB board design into consideration when deciding on overall decoupling solution.

Table 118. GMCH Decoupling Recommendations Checklist (Sheet 2 of 2)

Pin Name	Configuration	F	Qty	Notes	√
V_{TTHF}[5:1]		0.1 µF	5	Connect pins directly to caps to GND.	
V_{CCHL}[8:1]	Connect to V1P35_GMCH.	0.1 µF 10 µF	2 1	Bulk decoupling is based on VR solutions used on CRB design.	
V_{CC_SM}[37:1]	Connect to V_2P5_SM.	0.1 µF 150 µF	11 2	Bulk decoupling is based on VR solutions used on CRB design.	
V_{CC_QSM}[2:1]	Connect to V_2P5_SM with filter network.	0.1 µF 4.7 µF+1Ω	1 1 each	0.68 µH from power supply to GMCH pins. On GMCH side of inductor: one 0.1 µF to GND, 4.7 µF + 1 Ω to GND.	
V_{CCASM}[2:1]	Connect to V1P35_GMCH with filter network.	0.1 µF 100 µF	1 1	1 µH from power supply to GMCH pins, with caps on GMCH side of inductor.	
V_{CC_DVO}[16:1]	Connect to V_1P5_CORE.	0.1 µF 10 µF 150 µF	2 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
V_{CC_ADAC}[2:1]	Connect to V_1P5_CORE.	0.01 µF 0.1 µF 220 µF (no stuff)	1 1 1	Route VSSADAC to other side of the caps, then to ground. Consider a 0 Ω 0805 resistor between the caps and V_1P5_CORE. This and the 220 µF cap footprint are there in case there is noise issue with the VGA supply.	
V_{CC_ALVDS}	Connect to V_1P5_CORE	0.1 µF 0.01 µF	1 1	Route VSSALVDS to other side of the caps, then to ground.	
V_{CC_DLVDS}[4:1]	Connect to V_1P5_CORE	0.1 µF 22 µF 47 µF	1 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
V_{CC_TXLVDS}[4:1]	Connect to V_2P5_CORE	0.1 µF 22 µf 47 µF	3 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
V_{CC_GPIO}[2:1]	Connect to V_{CC}3	0.1 µF 10 µF	1 1	Bulk decoupling is based on VR solutions used on CRB design.	
V_{CC_AHPLL}	Connect to V1P35_GMCH	0.1 µF	1		
V_{CC_GPLL}	Connect to V1P35_GMCH	0.1 µF	1		
V_{CC_ADPLLA}	Connect to V1P35_GMCH with filter network	0.1 µF 220 µF	1 1	0.1 µH (1 Ω series on CRB) from power supply to GMCH pins, with caps on GMCH side of inductor.	
V_{CC_ADPLLB}	Connect to V1P35_GMCH with filter network	0.1 µF 220 µF	1 1	0.1 µH (1 Ω series on CRB) from power supply to GMCH pins, with caps on GMCH side of inductor.	

NOTE: Decoupling guidelines are recommendations based on our reference board design. Customers may need to take layout and PCB board design into consideration when deciding on overall decoupling solution.

14.4 Intel® 82801DB I/O Controller Hub 4 (ICH4) Checklist

Note: Inputs to the ICH4 must not be left floating. Many GPIO signals are fixed inputs that must be pulled up to different sources.

14.4.1 PCI Interface and Interrupts

Table 119 presents the PCI interface and interrupts checklist.

Table 119. PCI Interface and Interrupts Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
DEVSEL#	2.7 KΩ pull-up to V_{CC}	For signals requiring pull-up resistors, the recommendation is to use an 8.2 KΩ resistor to $V_{CC}3_3$ or a 2.7 KΩ resistor to $V_{CC}5$. Refer to the PCI 2.2 Component Specification for further information on pull-up recommendations.	
FRAME#	2.7 KΩ pull-up to V_{CC}		
REQ[4:0]# REQ5#/REQB#/GPIO1	2.7 KΩ pull-up to V_{CC}	Each signal requires a pull-up resistor.	
PCIREQA#/GPIO0	2.7 KΩ pull-up to V_{CC}		
PCIGNTA#/GPIO16		GNTA is also used as a strap for “top block swap”. It is sampled on the rising edge of PWROK. By default, this signal is HIGH (strap function DISABLED). It may be enabled by a pull-down to GND through a 1 KΩ resistor.	
IRDY#	2.7 KΩ pull-up to V_{CC}		
LOCK#	2.7 KΩ pull-up to V_{CC}		
PERR#	2.7 KΩ pull-up to V_{CC}		
SERR#	2.7 KΩ pull-up to V_{CC}		
STOP#	2.7 KΩ pull-up to V_{CC}		
TRDY#	2.7 KΩ pull-up to V_{CC}		
PME#		The ICH4 has an internal pull-up to $V_{CCSUS}3_3$.	
PCIRST#		47 Ω series at FWH	
APICCLK	0 Ω to GND	May also be connected directly to ground.	
APICD[1:0]	10 KΩ pull-down to GND	When XOR chain testing is **NOT** used: Pull down the signals through a shared 10 KΩ resistor. When XOR chain testing is used: Each signal requires a separate 10 KΩ pull-down resistor.	
IRQ[15:14]	8.2 KΩ pull-up to $V_{CC}3$	Each signal requires a pull-up resistor.	
PIRQ[A:D]# PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5	8.2 KΩ pull-up to $V_{CC}3$	External pull up is required for P_INT[A:D]#. External pull up is required when muxed signal (P_INT[H:E]#/ GPIO[5:2]) is implemented as PIRQ.	
SER IRQ	10 KΩ pull-up to $V_{CC}3$		

14.4.2 General Purpose I/O (GPIO) Recommendations Checklist

Note: Ensure ALL unconnected signals are OUTPUTS ONLY. Main power well GPIOs are 5 V tolerant, except for GPIO[43:32]. Resume power well GPIOs are not 5 V tolerant.

Table 120 presents the GPIO recommendations checklist.

Table 120. GPIO Recommendations Checklist (Sheet 1 of 2)

Recommendations	√
GPIO[7] & [5:0]: • These pins are in the Main Power Well. Pull-ups must use the V_{CC}3_3 plane. • Unused core well inputs must be pulled up to V_{CC}3_3. • GPIO[1:0] may be used as REQ[B:A]#. • GPIO[1] may be used as PCI REQ[5]#. • GPIO[5:2] may be used as PIRQ[H:E]#. • These signals are 5 V tolerant. • These pins are inputs.	
GPIO[8] & [13:11]: • These pins are in the Resume Power Well. Pull-ups go to V_{CCSUS}3_3 plane. • Unused resume well inputs must be pulled up to V_{CCSUS}3_3. • These are the only GPIOs that may be used as ACPI compliant wake events. • These signals are not 5 V tolerant. • GPIO[8] may be used as SMC_EXTSMI# • GPIO[11] may be used as SMBALERT#. • GPIO[13] may be used as SMC_WAKE_SCI# • These pins are inputs.	
GPIO[23:16]: • Fixed as output only. May be left NC. • In Main Power Well (V_{CC}3_3). • GPIO[17:16] may be used as GNT[B:A]#. • GPIO[17] may be used as PCI GNT[5]#. • STP_PCI#/GPIO[18] - used in mobile as STP_PCI# only. • SLP_S1#/GPIO[19] - used in mobile as SLP_S1# only. • STP_CPU#/GPIO[20] - used in mobile as STP_CPU# only. • C3_STAT#/GPIO[21] - used in mobile as C3_STAT# only. • CPUPERF#/GPIO[22] - open drain signal. Used in mobile as CPUPERF# only. • SSMUXSEL/GPIO[23] - used in mobile as SSMUXSEL only.	
GPIO[28,27,25,24]: • I/O pins. Default as outputs. May be left as NC. • These pins are in the Resume Power Well. • CLKRUN#/GPIO[24] (Note: Use V_{CC}3_3 if signal is required to be pulled-up.) • GPIO[28, 27, 25] from resume power well (V_{CCSUS}3_3). (Note: Use V_{CC}3_3 if this signal is required to be pulled-up.) • These signals are NOT 5 V tolerant. • GPIO[25] may be used as AUDIO_PWRDN.	

Table 120. GPIO Recommendations Checklist (Sheet 2 of 2)

Recommendations	√
GPIO[43:32]: • I/O pins. From main power well (V_{CC}3_3). • Default as outputs when enabled as GPIOs. • These signals are **NOT** 5 V tolerant. • GPIO[32] may be used as AGP_SUSPEND#. • GPIO[33] may be used as KSC_VPPEN#. • GPIO[34] may be used as SER_EN. • GPIO[35] may be used as FWH_WP#. • GPIO[36] may be used as FWH_TBL#. • GPIO[40] may be used as IDE_PATADET. • GPIO[41] may be used as IDE_SATADET.	

14.4.3 SMBus System Management Interface Checklist

Table 121 presents the SMBus system management interface checklist.

Table 121. SMBus System Management Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
INTRUDER#	100 KΩ pull-up to V_{CCRTC} (V_{BAT})	RTC well input requires pull-up (10 K-100 K) to reduce leakage from coin cell battery in G3.	
SMBALERT#/ GPIO[11]	10 KΩ pull-up to V_3P3_STBY		
SMBCLK, SMBDATA, SMLINK[1:0]	Pull-up to V_3P3_STBY (CRB incorporates an isolation circuit that ties pull-ups to V_{CC}3.)	Require external pull-up resistors. Pull up value is determined by bus characteristics. The SMBus and SMLink signals must be connected together externally for SMBus 2.0 compliance: SMBCLK connected to SMLink[0] and SMBDATA connected to SMLink[1].	

14.4.4 AC'97 Interface Checklist

Table 122 presents the AC'97 interface checklist.

Table 122. AC'97 Interface Checklist

Pin Name	System Pull-up/Pull-down	Series Termination Resistor	Notes	√
ACBITCLK	None	33-47 Ω	The internal pull-down resistor is controlled by the AC'97 Global Control Register, ACLINK Shut Off bit: 1 = Enabled 0 = Disabled When no AC'97 devices are connected to the link, BIOS must set the ACLINK Shut Off bit for the internal keeper resistors to be ENABLED. At that point, pull-ups/pull-downs are NOT needed on ANY of the link signals.	
ACSDATAIN[2:0]	Requires 10 kΩ pull-down to GND if a CNR card is used on the platform	33-47 Ω	A series termination resistor is required for the PRIMARY CODEC. A series termination resistor is required for the SECONDARY and TERTIARY CODEC if the resistor is not found on CODEC. This pin has a weak internal 20 kΩ nominal pull-down. For platforms routing AC_SDIN2 to CNR, the additional 10 kΩ pull-down is required to set the proper DC level for CNR card switching circuitry.	
ACSDATAOUT	None	33-47 Ω	A series termination resistor is required for the PRIMARY CODEC. One series termination resistor is required for the SECONDARY/ TERTIARY CODEC connector card if the resistor is not found on the connector card.	
ACSYNC	None	33-47 Ω	A series termination resistor is required for the PRIMARY CODEC. One series termination resistor is required for the SECONDARY/ TERTIARY CODEC connector card if the resistor is not found on the connector card.	

14.4.5 Intel® ICH4 Power Management Interface Checklist

Table 123 presents the ICH4 power management interface checklist.

Table 123. Intel® ICH4 Power Management Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
SLP_S3# SLP_S4# SLP_S5#	No pull-up/pull-down resistors needed.	Signals driven by the ICH4.	
PWRBTN#		Has integrated pull-up of 18 KΩ – 42 KΩ. Internally de-bounced by the ICH4.	
PWROK	Weak pull-down to GND.	This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both V_{CC}3_3 and V_{CC}1_5 have reached their nominal voltages.	
RI#	8.2 KΩ pull-up to V_{CCSUS}3_3	When this signal is enabled as a wake event, it needs to be powered during a power loss event. When this signal goes low (active), when power returns the RI_STS bit should be set and the system should interpret that as a wake event.	
RSMRST#	Weak pull-down to GND.	RSMRST# is a RTC well input and requires pull-down to reduce leakage from coin cell battery in G3. Input must not float in G3. CRB uses 10 KΩ pull-down. This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both V_{CC}3_3 and V_{CC}1_5 have reached their nominal voltages. May be tied to LANRST#.	
THRM#	4.7 KΩ Pull-up to V_{CC}3_3 if TEMP SENSOR not used	External pull-up not required if connecting to temperature sensor. This input to the ICH4 cannot float. THRM# polarity bit defaults to active low, so pull up.	
SYSRST#	22 KΩ pull-up to V_{CCSUS}3_3 if not actively driven.	This signal to the ICH4 should not float. It needs to be at valid level all the time.	

14.4.6 FWH/LPC Interface Checklist

Table 124 presents the FWH/LPC interface checklist.

Table 124. FWH/LPC Interface

Pin Name	System Pull-up/Pull-down	Notes	√
LAD[3:0]/FWH[3:0] LFRAME#/FWH[4] LDRQ[1:0]#		The ICH4 integrates 20 KΩ nominal pull-up resistors on these signals. No extra pull-ups required. Connect straight to FWH/LPC.	

14.4.7 USB Interface Checklist

Table 125 presents the USB interface checklist.

Table 125. USB Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
OC[5:0]#	10 KΩ pull-up to $V_{CCSUS}3_3$ if not driven	No pull-up is required if signals are driven. Signals must NOT float if they are not being used.	
USBRBIAS, USBRBIAS#	22.6 Ω ± 1% pull-down to GND	Connect signals together and pull down through a common resistor, placed within 500 mils of the ICH4. Avoid routing next to clock pin.	

14.4.8 Hub Interface Checklist

Table 126 presents the Hub Interface checklist.

Table 126. Hub Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
HICOMP	48.7 Ω 1% pull-up to V_1P5_CORE	Place resistor within 0.5 inch of the ICH4 pad using a thick trace. Refer to Section 8.1 for more information.	
HIREF, HISWING	HIREF signal voltage level = 0.35 V ± 8%. HISWING signal voltage level = 0.80 V ± 8%.	Refer to Section 8.4 for several recommended options that may be used to generate these references.	
HI[11]	56 Ω pull-down to GND	HI[11] is not available on the GMCH.	

14.4.9 RTC Circuitry Checklist

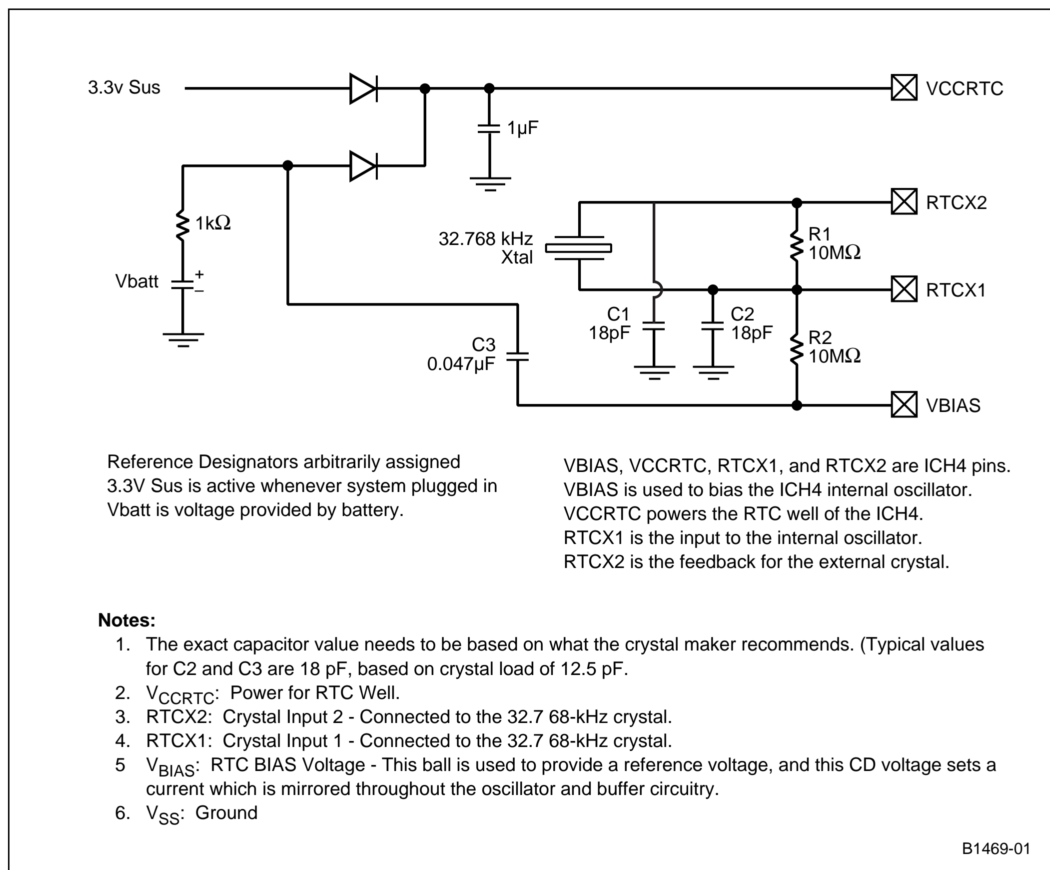
Table 127 presents the RTC circuitry checklist.

Table 127. RTC Circuitry Checklist

Pin Name	System Pull-up/Pull-down	In Series	Notes	√
RTCRST#	22 KΩ pull-up to V_{CCRTC} (V_{BAT}) and 1 µF cap to GND		RTCRST# requires 18-25 ms delay. Use a 1 µF cap to ground. Pull up with 22 KΩ resistor. Any resistor or capacitor combination that yields a suitable time constant is acceptable.	
RTCX1 RTCX2			Connect a 32.768 KHz crystal oscillator across these pins with a 10 MΩ resistor and a decoupling cap at each signal. Values for C1 and C2 are dependent on crystal. Refer to the RTC example in Figure 137.	
V_{BIAS}		1 KΩ 0.047 µF	Connect to CLK_RTCX1 through a 10 MΩ resistor. Connect to V_{BATT} through a 1 KΩ in series with a 0.047 µF capacitor.	

Figure 137 illustrates the external circuitry for the RTC.

Figure 137. External Circuitry for the RTC



14.4.10 LAN Interface Checklist

Table 128 presents the LAN interface checklist.

Table 128. LAN Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
LANCLK		Connect to LAN_CLK on the platform LAN Connect Device (CRB places a 33 Ω series resistor near LAN Connect Device). When LAN interface is not used, leave the signal unconnected (NC). Refer to Section 9.12.1 for routing requirement.	
LANRST#	10 KΩ pull-down to GND, if the ICH4 LAN is not used	Timing Requirement: Signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both $V_{CCSUS}3_3$ and $V_{CCSUS}1_5$ have reached their nominal voltages. May be tied to RSMRST#. **NOTE:** When the ICH4 LAN controller is NOT used, pull LANRST# down through a 10 KΩ resistor.	
LANRXD[2:0] LANTXD[2:0]		Connect to LAN_RXD and LAN_TXD on the platform LAN Connect Device. When LAN interface is not used, leave the signal unconnected (NC).	
LANRSTSYNC		Connect to LAN_RSTSYNC on Platform LAN Connect Device. When LAN interface is not used, leave the signal unconnected (NC).	

14.4.11 Primary IDE Interface Checklist

Table 129 presents the Primary IDE interface checklist.

Table 129. Primary IDE Interface Checklist

Pin Name	System Pull-up/Pull-down	Series Damping	Notes	√
PDD[15:0]			These signals have integrated series resistors.	
PDA[2:0], PDCS1#, PDCS3#, PDDACK#, PDIOW#, PDIOR#			These signals have integrated series resistors. Pads for series resistors may be implemented should the system designer have signal integrity concerns.	
PDDREQ			These signals have integrated series resistors and pull-down resistors in the ICH4.	
PIORDY	4.7 KΩ pull-up to $V_{CC}3$		This signal has integrated series resistor in the ICH4.	

14.4.12 IDE Interface (Secondary IDE Connector) Checklist

Table 130 presents the IDE interface (Secondary IDE connector) checklist.

Table 130. IDE Interface (Secondary IDE Connector) Checklist

Pin Name	System Pull-up/Pull-down	Series Damping	Notes	√
SDD[15:0]			These signals have integrated series resistors.	
SDA[2:0], SDCS1#, SDCS3#, SDDACK#, SDIOW#, SDIOR#			These signals have integrated series resistors. Pads for series resistors may be implemented should the system designer have signal integrity concerns.	
SDDREQ			These signals have integrated series resistors and pull-down resistors in the ICH4.	
SIORDY	4.7 KΩ pull-up to $V_{CC}3$		This signal has integrated series resistor in the ICH4.	

14.4.13 Miscellaneous Signals Checklist

Table 131 presents the miscellaneous signals checklist.

Table 131. Miscellaneous Signals Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
SPKR		SPKR is a strapping option for the TCO Timer Reboot function and is sampled on the rising edge of PWROK. An integrated weak pull-down is enabled only at boot/reset. Status of strap is readable through the NO_REBOOT bit (D31:F0, Offset D4h, bit 1): 1 = Disabled 0 = Enabled (normal operation) To disable, a jumper may be populated to pull SPKR high. Value of pull-up must be such that the voltage divider output caused by the pull-up, effective impedance of speaker and codec circuit, and internal pull-down should be read as logic high (0.5 * $V_{CC}3_3$ to $V_{CC}3_3$ + 0.5).	
TP0	Requires external pull-up resistor to $V_{CCSUS}3_3$.	CRB uses a 10 KΩ pull-up to V_3P3_STBY.	

14.4.14 Intel® ICH4 Decoupling Recommendations Checklist

Table 132 presents the ICH4 decoupling recommendations checklist.

Table 132. Intel® ICH4 Decoupling Recommendations Checklist

Pin Name	Configuration	Value	Q	Notes	√
V_{CC}1_5 V_{CCHI}[3:0]	Connect to V_1P5_CORE.	0.1 µF 0.1 µF	2 2	Low frequency decoupling is dependent on layout and power supply design.	
V_{CC}3_3	Connect to V_{CC}3	0.1 µF	6	Low frequency decoupling is dependent on layout and power supply design.	
V_{CCSUS}1_5	Connect to V_1P5_STBY	0.1 µF	2	Low frequency decoupling is dependent on layout and power supply design.	
V_{CCSUS}3_3	Connect to V_3P3_STBY.	0.1 µF	2	Low frequency decoupling is dependent on layout and power supply design.	
V5$_{REF}$[2:1]	Connect to V_{CC} through 1 KΩ	0.1 µF	1	Caps from V5$_{REF}$ to ground. Also connect diode from V5$_{REF}$ to V_{CC}3. CRB also generates via Glue Chip 4.	
V5$_{REF_SUS}$	Connect to V_5P0_STBY through 1 KΩ	0.1 µF	1	Caps from V5$_{REF_SUS}$ to ground. Also connect diode from V5$_{REF_SUS}$ to V_3P3_STBY. CRB generates via Glue Chip.	
VCC_CPU_IO	Connect to V_{CCP}.	0.1 µF 1 µF	1 1		
V_{CCPLL}	Connect to V_1P5_CORE.	0.1 µF 0.01 µF	1 1		
V_{CCRTC}	Connect to V_3P0_BAT_VREG.	0.1 µF	1		

NOTE: All decoupling guidelines are recommendations based on our reference board design. Customers need to take their layout and PCB board design into consideration when deciding on their overall decoupling solution. Capacitors should be placed less than 100 mils from the package.

14.5 USB Power Checklist

14.5.1 Downstream Power Connection Checklist

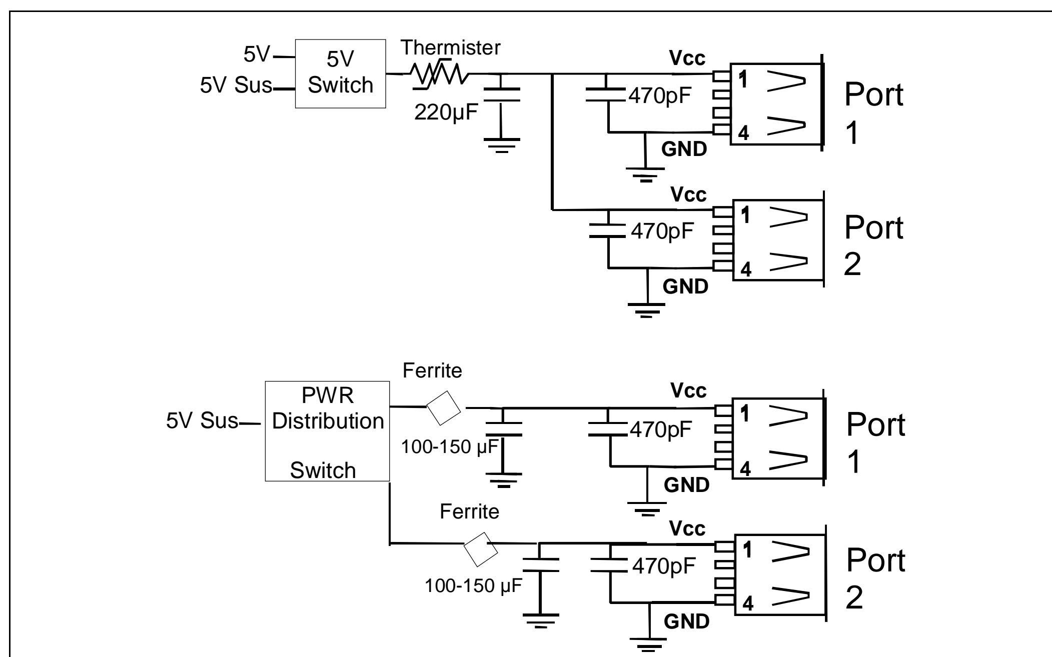
Table 133 presents the downstream power connection checklist.

Table 133. Downstream Power Connection Checklist

USB Power	Notes	√
USB_VCC[E:A]	Intel recommends one 220 µF and two 470 pF capacitors for every two power lines. Either a thermister or a power distribution switch (with short circuit and thermal protection) is required. Refer to the good downstream power connection example in Figure 138.	

Figure 138 illustrates the good downstream power connection example.

Figure 138. Good Downstream Power Connection - Example



14.6 LAN Checklist

14.6.1 Connection Recommendations Checklist (for Intel® 82562ET/82562EM Platform LAN Connect

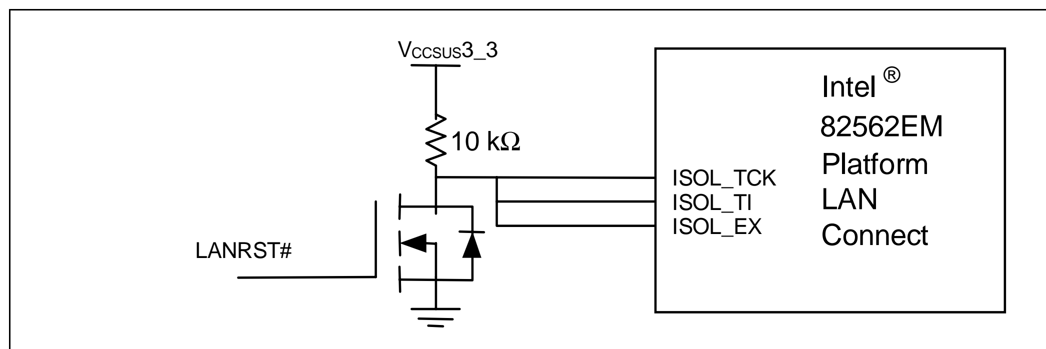
Table 134 presents the connections recommendations checklist for Intel® 82562ET/82562EM platform LAN connect.

Table 134. Connection Recommendations Checklist for Intel® 82562ET/82562EM Platform LAN Connect

Pin Name	System Pull-up/Pull-down	Term Resistor	Notes	√
ISOL_EX, ISOL_TCK, ISOL_TI	10 KΩ pull-up to $V_{CCSUS}3_3$		When LAN is enabled, all three signals needs to be pulled up through a common 10 KΩ pull-up resistor. Refer to Figure 139.	
RBIAS10	562 Ω ± 1%pull-down to GND			
RBIAS100	619 Ω ± 1%pull-down to GND			
RDP, RDN		124 Ω ± 1%	Connect 124 Ω resistor between RDP and RDN.	
TDP, TDN		100 Ω ± 1%	Connect 100 Ω resistor between TDP and TDN.	
TESTEN	100 Ω pull-down to GND			
X1, X2			Connect a 25 MHz crystal across these two pins. 33 pF on each pin to ground.	
LANRST#			On CRB, the power monitoring logic waits for PM_PWROK to go high before deasserting this signal to enable the LAN device. Also refer to LANRST# in Section 14.4.10. Refer to Figure 139.	

Figure 139 illustrates the LAN_RST# design recommendation.

Figure 139. LAN_RST# Design Recommendation



14.6.2 Decoupling Recommendations Checklist

Table 135 presents the decoupling recommendations checklist.

Table 135. Decoupling Recommendations Checklist

Signal Name	Configuration	F	Qty	Notes	√
V_{CC}[2:1], V_{CCP}[2:1], V_{CCA}[2:1], V_{CCT}[4:1]	Connect to V_3P3_STBY	0.1 µF 4.7 µF	8 2		
V_{CCR}[2:1]	Connect to V_3P3_STBY through filter.	0.1 µF 4.7 µF 1000 pF	1 1 1	4.7 µH from power supply to V_{CCR} pins. Caps on V_{CCR} side of the inductor.	

Layout Checklist 15

This checklist selectively highlights some of the design considerations that should be reviewed prior to manufacturing Pentium® M processor/Celeron® M processor systems that implement the Intel® 855GME chipset. Items contained within the checklist attempt to address important connections to these devices and any critical supporting circuitry. **This is not a complete list, and it does not ensure that a design will function properly.** Refer to details in this document and the appended Customer Reference Board schematics for complete design recommendations. The recommendations and considerations in this guide are subject to change.

The following recommendations are a summary of the information presented in this design guide. They are based on the example 8-layer stackup detailed in Chapter 3. Deviation from the example stackup will require thorough signal integrity and timing simulations.

15.1 Processor Checklist

Table 136 presents the processor layout checklist.

Table 136. Processor Layout Checklist (Sheet 1 of 5)

Checklist Items	Recommendations	Comments
Pentium® M Processor FSB Interface Signals		
A[31:3]#[1] ADSTB[1:0]#[2] DSTBN[3:0]#[3] DSTBP[3:0]#[4] DINV[3:0]# D[63:0]#[5] REQ[4:0]#[6]	• Trace impedance = 55 Ω ± 15%. • Use stripline routing, referencing ground planes above and below the signal layer. • Route data strobes and data signals 4/12 with board trace length between 0.5 and 5.5 inches total trace length including package compensation. • Use GMCH die-pad to processor pin length for all length matching operations. • Length match data strobes of the same group to within ± 25 mils of each other and to the average length of their associated data signal group. • Route all data signals as groups, on the same layer, and balance within group ± 100 mils with respect to the associated strobes. • Route address strobes 4/12 and address signals 4/8 with board trace length between 0.5 and 6.5 inches total trace length including package compensation. • Trace length match address strobes to ± 200 mils of average length of their associated address signals group.	• AGTL+ Source Synchronous Signals. • Refer to Section 4.1.3 for more information.
ADS# BNR# BR0# DBSY# DRDY# HIT# HITM# LOCK# DPWR# BPRI# DEFER# RS[2:0]# TRDY#[8]	• Trace impedance = 55 Ω ± 15%. • Use stripline routing, referencing solid ground planes. • Route traces using 4/8 mils spacing with board trace length between 0.997 and 6.5 inches. • Trace length matching is not required for common clock signals. • Package length compensation is necessary in determining minimum board trace length.	• AGTL+ Common Clock Signals. • Refer to Section 4.1.2 for more information.
RESET#[7]	• **When ITP700 Is Not Used:** • Trace impedance = 55 Ω ± 15%. • Use stripline routing, referencing solid ground planes. • Route traces using 4/8 mils spacing with board trace length between one and 6.5 inches. • Trace length matching is not required for common clock signals. • Package length compensation is necessary in determining minimum board trace length.	• Refer to ITP Section of this layout checklist for treatment of RESET# signal when implementing ITP700FLEX debug port. • AGTL+ Common Clock Signal. • Refer to Section 4.1.6 for more information.

Table 136. Processor Layout Checklist (Sheet 2 of 5)

Checklist Items	Recommendations	Comments
Intel® 82801DB I/O Controller Hub (ICH4) Interface Signals		
IERR#	• May be routed as a test point or to any optional system receiver. • May be routed as stripline or microstrip with trace impedance = 55 Ω ± 15%. • Place series resistor R1 within three inches of system receiver. • Place pull-up resistor Rtt within three inches of series resistor R1. • Pull-up voltage for termination resistor Rtt is V_{CCP} (1.05).	• Asynchronous AGTL+ Output Signal. • Refer to Topology 1A in Section 4.1.5.1 for resistor values and trace length recommendations.
PROCHOT#	• May be routed as stripline or microstrip with trace impedance = 55 Ω ± 15%. • Use Intel's recommended voltage translation logic for an appropriate system receiver. • Pull-up voltage for termination resistor Rtt is V_{CCP} (1.05) • Place series resistor Rs at the beginning of trace T-split and within three inches from Q1.	• Asynchronous AGTL+ Output Signal. • Refer to Topology 1C in Section 4.1.5.3 for resistor values and trace length recommendations.
FERR# THERMTRIP#	• Connect FERR# to the processor and the Intel® 82801DB I/O Controller Hub 4 (ICH4). • Recommend connecting processor signal THERMTRIP# to the ICH4, but may be connected to any optional system receiver, with consideration for any voltage level translation if necessary. • May be routed as stripline or microstrip with trace impedance = 55 Ω ± 15%. • Place series resistor R1 within three inches of system receiver. • Place pull-up resistor Rtt within three inches of series resistor R1. • Pull-up voltage for termination resistor Rtt is V_{CCP} (1.05).	• Asynchronous AGTL+ Output Signals. • Refer to Topology 1B in Section 4.1.5.2 for resistor values and trace length recommendations. • Refer to Section 4.1.5.7 for voltage translation recommendations.
IPWRGOOD	• May be routed as stripline or microstrip with trace impedance = 55 Ω ± 15% • Route point-to-point between the ICH4 signal CPUPWRGD and CPU signal PWRGOOD, trace length range between 0.5 and 12 inches. • Place a termination resistor Rtt within three inches of CPU pin. T-split routing should not be used. • Pull-up voltage for termination resistor Rtt is V_{CCP} (1.05)	• Asynchronous Open Drain CMOS Input Signal. • Refer to Topology 2A in Section 4.1.5.4 for resistor values and detailed routing recommendations.
IGNNE# LINT0/INTR LINT1/NMI SMI# SLP# A20M# STPCLK#	• May be routed as stripline or microstrip with trace impedance = 55 Ω ± 15%. • Implement a point-to-point connection between the ICH4 and CPU, trace length range between 0.5 and 12 inches. • No additional components are necessary for this topology.	• Asynchronous CMOS Input Signals. • Refer to Topology 2B in Section 4.1.5.5.

Table 136. Processor Layout Checklist (Sheet 3 of 5)

Checklist Items	Recommendations	Comments
INIT#	• May be routed as stripline or microstrip with trace impedance = 55 Ω ± 15%. • Route signal point-to-point between the ICH4 and CPU, trace length range between 0.5 and 12 inches. • Voltage level translation is required from the ICH4 INIT# pin to FWH. • Place series resistor Rs at the beginning of trace T-split and within three inches from Q1.	• Asynchronous CMOS Input Signal. • Refer to Topology 3 in Section 4.1.5.6 for resistor values and trace length recommendations. • Refer also to Section 4.1.5.7 for more details on voltage translation recommendations. • The Intel customer reference board makes use of an optional alternative circuit for FWH voltage translation. Refer to schematic appendix.
Processor In Target Probe (ITP) Signals for ITP700FLEX Debug Port		
BPM[3:0]# PRDY# PREQ#	• Route as a point-to-point transmission line connections from CPU pins to the ITP700FLEX connector via Zo = 55 Ω ± 15% traces. Limit trace length to shorter than six inches. **ITP700** to **CPU** BPM[3:0]# BPM[3:0]# BPM4# PRDY# BPM5# PREQ# • Length match to each other within ± 50 ps. • These signals also must be length matched to the net lengths of the RESET# signal within ± 50 ps, as detailed in Section 4.3.1.	• Refer to Section 4.3 for important design considerations when implementing ITP700FLEX. • Refer to Section 4.1.10 for default strapping and placement when ITP debug port is not implemented.
RESET#[7]	• **When ITP700 Is Used**: • Fork out this signal from GMCH (**do not T-split**) and route to CPU and to Rtt/Rs termination network placed near ITP700FLEX debug connector. • Complete routing by connecting Rs to the ITP700FLEX connector, limiting trace length to less than 0.5 inch (L3). • Rtt is pulled-up to V_{CCP} and should be placed right next to Rs. • Trace length from GMCH to the Rtt/Rs network near the debug connector should be limited to less than six inches (L2). • The forked trace from the GMCH to the CPU should be limited to a length range of 1.0 to 6 inches (L1). • ITP700FLEX debug operation requires matching L2 + L3 - L1 length to within ± 50 ps of the length of the BPM[4:0] signals detailed above.	Refer to Section 4.1.6 and Section 4.3.1 for details on ITP700FLEX/RESET# routing recommendations and resistive network resistor values.
DBR#	• **When ITP700 Is Used**: • Route to system reset logic with a pull-up resistor to target system V_{CC}. • Place pull-up resistor within one ns of the ITP700FLEX debug connector.	

Table 136. Processor Layout Checklist (Sheet 4 of 5)

Checklist Items	Recommendations	Comments
TCK	• **When ITP700 Is Used**: • Fork out this signal from the CPU (**do not T-split**) and route to the TCK pin and the FBO pin of ITP700FLEX debug connector. • Parallel termination resistor to ground is placed within ±200 ps of ITP700 connector.	Refer to Section 4.3.1 for details on routing CPU TAP logic signals for ITP700 debug operation.
TDI	• **When ITP700 Is Used**: • Route between CPU and debug connector pin. • Parallel termination resistor to V_{CCP} is placed within ±300 ps of CPU pin.	
TDO	• **When ITP700 Is Used**: • Route from CPU pin to a pull-up resistor to V_{CCP} placed near the debug connector TDO pin. • Place a series resistor connecting the pull-up resistor to the ITP700FLEX debug connector, limiting trace length from the series resistor to the debug connector to less than one inch.	
TRST#	• **When ITP700 Is Used**: • Route between CPU and debug connector pin. • Parallel termination resistor to ground should be placed anywhere between CPU and ITP700. Avoid any trace stub from signal line to parallel termination resistor.	
TMS	• **When ITP700 Is Used**: • Route between CPU and debug connector pin. • Parallel termination resistor to V_{CCP} should be placed within ±200 ps of the ITP700FLEX debug connector pin.	
Other Signals		
BCLK, BCLK#	• CPU BCLK, BCLK# from CK-408 should be routed as differential pairs and length matched to the GMCH BCLK, BCLK# signals. • **When ITP700 Is Used**: • ITP BCLK, BCLK# should be routed with similar recommendations, but should be length matched to within ±50 ps of the system bus clock pairs and the additional length of the BPM[4:0]# signals, to ensure correct operation of ITP700FLEX.	• Refer to host clock group routing guidelines detailed in Section 11.2.1. • Refer to Chapter 10 for detailed breakdown of all system clock routing recommendations.
COMP[0,2]	• Terminate each signal to ground with 27.4Ω ±1% resistors. • Connect each to CPU with a Zo = 27.4Ω trace that is less than 0.5 inch from the pin. • Spacing from other switching signal traces should be a minimum of 25 mils.	Refer to Section 4.1.9.1 for detailed layout recommendations.

Table 136. Processor Layout Checklist (Sheet 5 of 5)

Checklist Items	Recommendations	Comments
COMP[1,3]	• Terminate each signal to ground with 54.9 Ω ±1% resistors. • Connect each to CPU with a Zo = 55Ω trace that is less than 0.5 inch from the pin. • Spacing from other switching signal traces should be a minimum of 25 mils.	Refer to Section 4.1.9.1 for detailed layout recommendations.
Processor Power and GND Measurement/Sense Signals		
$V_{CCSENSE}$ $V_{SSSENSE}$	• Route traces of equal length using 3:1spacing, Zo = 55 Ω ± 15%. • Place via next to the processor socket's pin for measurement of CPU_VCC/V_{SS}. • Place a ground via 100 mils from each test point via.	Refer to Section 4.1.11 for more information.
Processor Decoupling, VREF, and Filtering		
GTLREF	• Connect CPU GTLREF pin to a 1 K Ω ± 1% and 2 K Ω ± 1% resistive divider to V_{CCP}. • No decoupling on this signal. • Connect voltage divider node to CPU GTLREF pin with a Zo = 55 Ω trace that is shorter than 0.5 inch. • Minimum separation from other switching signals should be 25 mils.	Refer to Section 4.1.8 for more information.
V_{CC} (CORE) Decoupling	Intel recommends bulk decoupling: • (4) 220 µF SP caps - ESR 12 mΩ (max) and ESL 3.5 µH, placed near CPU north power corridor (pin map row AF). Intel recommends mid-frequency decoupling: • (35) 10 µF 0805 caps - ESR 5 mΩ (typ) and ESL 0.6 nH placed in and near package outline.	Refer to the *Intel® Pentium® M Processor Datasheet, Intel® Pentium® M Processor on the 90 nm Process with 2 MB L2 Cache Datasheet,* and *Intel® Celeron® M Processor Datasheet* for more information.
V_{CCP} Decoupling	Intel recommends bulk decoupling: • (2) 150 µF POSCAP - ESR 42 mΩ (typ) and ESL 2.5 nH, placed one each near the CPU and the GMCH packages. • (10) 0.1 µF X7R 0603 caps - ESR 16 mΩ (typ) and ESL 0.6 nH, placed on the secondary side within the CPU package outline.	Refer to the *Intel® Pentium® M Processor Datasheet, Intel® Pentium® M Processor on the 90 nm process with 2 MB L2 Cache Datasheet,* and *Intel® Celeron® M Processor Datasheet* for more information.

NOTES:
1. A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
3. DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
4. DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
5. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH. Refer to the ITP portion of this checklist, Section 4.1.6 and Section 4.3.1 for treatment of RESET# when using ITP700FLEX debug port.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

15.2 Intel® 855GME Chipset GMCH (82855GME) Layout Checklist

Table 137 presents the Intel® 855GME chipset GMCH layout checklist.

Table 137. Intel® 855GME Chipset GMCH Layout Checklist (Sheet 1 of 5)

Checklist Items	Recommendations	Comments
Host Interface Signals		
ADS# BNR# BPRI# BREQ0#[1] CPURST#[2] DBSY# DEFER# HA[31:3]#[3] HD[63:0]#[4] HADSTB[1:0]#[5] HDSTBN[3:0]#[6] HDSTBP[3:0]#[7] HIT# HITM# HLOCK#[10] HREQ[4:0]#[8] HTRDY#[9] DRDY# RS[2:0]# DINV[3:0]#	Refer to the Processor section of this checklist.	
DDR System Memory Interface		
SCK[5:0] SCK[5:0]#	• Route as closely-coupled differential pairs, three clock pairs to each DIMM. • Spacing to other DDR signals should not be less than 20 mils. Isolation from non-DDR signals should be 25 mils. • Route on internal layers, except for pin escapes. • Nominal internal trace width 7 mils and nominal internal spacing four mils. • Routed trace length limits are 3.5 to 6.5 inches. • Length match clock pairs to ±10 mils. • Match all DIMM0 clocks to ± 25 mils. • Match all DIMM1 clocks to ± 25 mils. • Use GMCH package lengths for pad-to-pin length tuning.	Refer to the detailed routing guidelines in Section 5.4.3.
SDQ[71:0] SDM[8:0] SDQS[8:0]	• Route SDQ/SDM with trace impedance 55 Ω ± 15% using 2:1 spacing. • Route SDQS strobes similarly with 3:1 spacing. • Isolation from non-DDR signals should be 20 mils. • Overall min/max length to the DIMM must comply with clock length matching requirements.	Refer to the detailed routing guidelines in Section 5.4.4.

Table 137. Intel® 855GME Chipset GMCH Layout Checklist (Sheet 2 of 5)

Checklist Items	Recommendations	Comments
SCKE[3:0] SCS[3:0]#	• Route with trace impedance 55 Ω ± 15% using 2:1 spacing. • Isolation from non-DDR signals should be 20 mils. • GMCH pad to DIMM trace length limits are two to six inches. • Place parallel termination resistor within two inches of DIMM pad. • Overall min/max length to the DIMM must comply with clock length matching requirements.	Refer to the detailed routing guidelines in Section 5.4.5.
SRAS# SCAS# SWE# SMA[12:6,3,0] SBA[1:0]	• Route with trace impedance 55 Ω ± 15% using 2:1 spacing. • Isolation from non-DDR signals should be 20 mils. • GMCH pad to first DIMM trace length limits are 2 to 5.5 inches. • Total DIMM to DIMM spacing should be less than two inches. • Place parallel termination resistor within 1.5 inches of the second DIMM pad. • Overall min/max length to the DIMM must comply with clock length matching requirements.	Refer to the detailed routing guidelines in Section 5.4.6.
SMA[5,4,2,1] SMAB[5,4,2,1]	• Route with trace impedance 55 Ω ± 15% using 2:1 spacing. • Isolation from non-DDR signals should be 20 mils. • GMCH pad to DIMM trace length limits are two to six inches. • Place parallel termination resistor within two inches of the DIMM pad. • Overall min/max length to the DIMM must comply with clock length matching requirements.	Refer to the detailed routing guidelines in Section 5.4.7.
RCVENIN# RCVENOUT#	• Internally shunted on Intel® 855GME chipset - no external connection necessary. • Recommendation is that both signals be transitioned to the secondary side with vias next to the package balls to facilitate probing.	Refer to the detailed routing guidelines in Section 5.4.8.

Table 137. Intel® 855GME Chipset GMCH Layout Checklist (Sheet 3 of 5)

Checklist Items	Recommendations	Comments
DDR System Memory Decoupling		
GMCH V_{CCSM} Decoupling	• Requires a minimum of (11) 0603, 0.1 µF caps placed within 150 mils of the GMCH package. • Distribute evenly along the DDR memory interface, placed perpendicular to the GMCH with the power side of the caps facing the GMCH. • Each GMCH ground and V_{CCSM} power ball should have its own via. • Each via should be as close to the associated cap pad as possible, within 25 mils and with as thick a trace as possible.	Refer to Section 12.4.2.1 for more information.
DDR Bypass Caps	• Place nine evenly spaced 0.1 µF 0603 caps between the DIMMs. • A wide trace from each cap should connect to a via that transitions to the ground plane layer. • A wide trace should connect the 2.5 V side of each cap to a via that transitions to the 2.5 V plane, each via placed as close to the cap pad as possible. • Each cap should also connect to the closest 2.5 V DIMM pin on either DIMM connector with a wide trace.	• Helps minimize return path discontinuities. • Refer to Section 12.4.2.2 for more information.
DDR VTT Decoupling	• Decouple V_{TT} termination rail using one 0603 0.1 µF capacitor per two DDR signals. • Spread out placement across the V_{TT} termination rail, connecting directly to the rail, so that each parallel termination resistor is within 100 mils of one of these high-frequency capacitors. • Each ground via should be as close to the associated cap pad as possible, within 25 mils and with as thick a trace as possible. • Also, place one 4.7 µF ceramic capacitor on each end of the termination island, and place one 4.7 µF ceramic capacitor near the center of the termination island. • Low frequency bulk decoupling requirements at the V_{TT} termination rail should be met with (4) 470 µF caps placed evenly across the VTT rail, including one cap at each end.	Refer to Section 12.4.2.3 for more information.

Table 137. Intel® 855GME Chipset GMCH Layout Checklist (Sheet 4 of 5)

Checklist Items	Recommendations	Comments
Hub Interface		
General Guidelines	• Route hub interface data and strobes with trace impedance 55 Ω ± 15% using 2:1 spacing and V_{SS} reference. • Route hub interface strobe and its complement as a differential pair, length matched within ± 10 mils. • Maximum length for both data and strobe signals is six inches. • Minimum length for both data and strobe signals is 1.5 inches. • Hub interface data and strobe signals are routed on the same layer, transitioning together when a layer change is required. • Keep layer changes to a minimum, using only two vias per net.	• Refer to Section 8.2.1 for detailed routing recommendations. • The platform design guide example references routing guidelines for the 11-bit Hub Interface using enhanced (parallel) termination.
Clocks and Reset Signals		
BCLK BCLK#	• The differential host clock pair should be length matched to ± 10 mils and to the processor BCLK/BCLK# pair within ± 20 mils overall (match L1 segments to ± 10 mils across all pairs). • Route as stripline traces 4/7 mils spacing (except as allowed for pin escapes). • Total length range is 2 to 8.5 inches.	• Refer to host clock group routing guidelines detailed in Section 11.2.1. • Refer to Chapter 10 for detailed breakdown of all system clock routing recommendations.
GCLKIN (CLK66)	• Place series resistor close to CK408, within 500 mils. • Total trace length range is four to nine inches. • Minimum spacing 20 mils. • Overall length of CLK66 is considered the reference length for all other clocks, except USBCLK and CLK14. • The length of CLK66 traces should be matched within ± 100 mils and then used as the basis for defining the length of all other length matched clocks.	Refer to CLK66 clock group routing guidelines detailed in Section 11.2.2.
RSTIN#	Connect to PCIRST# output of the Intel® 82801DB ICH4.	
GMCH Decoupling, VREF, and Filtering		
HLRCOMP HLVREF PSWING	• GMCH HLRCOMP signal should be strapped to 1.2 V via 27.4 Ω ± 1% HLRCOMP resistor with trace impedance 55 Ω ± 15%. • HLVREF and PSWING voltage requirements must be set appropriately for proper hub interface operation. The case is similar for HIREF and HIVSWING signals on ICH4.	Refer to Section 8.3 for HI specific voltage requirements and several options for voltage divider circuits.

Table 137. Intel® 855GME Chipset GMCH Layout Checklist (Sheet 5 of 5)

Checklist Items	Recommendations	Comments
HXRCOMP HYRCOMP	• Each signal should be pulled to ground with a 27.4 Ω ± 1% resistor. • Max trace length to the resistor should be less than 0.5 inch and should be 18 mils wide to achieve the characteristic impedance target of 27.4 Ω. • Maintain 25 mil separation from any switching signals.	• This signal is used to calibrate the Host AGTL+ I/O buffers characteristics to specific board characteristics. • Refer to Section 12.4.2.2 for more information.
HDVREF[2:0] HAVREF HCCVREF	• Max length from pin to voltage divider for each reference voltage should be less than 0.5 inch. • Intel recommends 10 mil traces.	• To provide constant and clean power delivery to the data, address, and common clock signals of the host AGTL+ interface. • Refer to Section 12.4.4.1 for recommended individual voltage divider circuits.
HXSWING HYSWING	• Voltage divider components for each input should be placed within 0.5 inch of their respective pins. • Use a 15 mil wide trace maintaining a minimum of 25 mils separation to other signals.	• The HXSWING and HYSWING inputs of GMCH are used to provide reference voltage for the compensation logic. • Refer to Section 12.4.4.3 for more information.
Analog Power Filtering	There are eight analog circuits that require filtered supplies on the Intel® 855GME chipset.	Refer to Section 12.4.4.4 for detailed filter requirements.

NOTES:
1. The BREQ0# pin on the GMCH corresponds to the BR0# pin on the processor.
2. The CPURST# pin on the GMCH corresponds to the RESET# pin on the processor.
3. HA[35:3]# pins on the GMCH correspond to A[31:3]# pins on the processor.
4. HD[63:0]# pins on the GMCH correspond to D[63:0]# pins on the processor.
5. HADSTB[1:0]# pins on the GMCH correspond to ADSTB[1:0]# pins on the processor.
6. HADSTBN[3:0]# pins on the GMCH correspond to DSTBN[3:0]# pins on the processor.
7. HADSTBP[3:0]# pins on the GMCH correspond to DSTBP[3:0]# pins on the processor.
8. HREQ[4:0]# pins on the GMCH correspond to REQ[4:0]# pins on the processor.
9. The HTRDY# pin on the GMCH corresponds to the TRDY# pin on the processor.
10. The HLOCK# pin on the GMCH correspond to LOCK# pin on the processor.

15.3 Intel® 82801DB I/O Control Hub 4 (ICH4) Layout Checklist

Table 138 presents the Intel® 82801DB I/O Controller Hub 4 (ICH4) layout checklist.

Table 138. Intel® 82801DB I/O Controller Hub 4 (ICH4) Layout Checklist (Sheet 1 of 5)

Checklist Items	Recommendations	Comments
Processor Signals		
A20M# CPUSLP# FERR# IGNNE# INIT# LINT[1:0] SMI# STPCLK#	Refer to the Processor section of this checklist.	
FWH Interface		
Decoupling	• 0.1 µF capacitors should be placed between the V_{CC} supply balls and the VSS ground balls, and no less than 390 mils from the V_{CC} supply balls. • 4.7 µF capacitors should be placed between the V_{CC} supply balls and the VSS ground balls, and no less than 390 mils from the V_{CC} supply balls.	
Hub Interface - Refer to General Guidelines in the GMCH section of this checklist.		
IDE Checklist		
General Guidelines	• Traces are routed 5 mils wide with 7 mils spacing. • Max trace length is eight inches long. • The maximum length difference between the longest and shortest trace length is 0.5 inch.	• Refer to Section 9.3 for primary/ secondary IDE details. • Refer to ATA ATAPI-4 specification.
LAN Interface		
General Guidelines	Maintain board trace impedance 55 Ω ± 15% per example 8-layer stack-up to avoid violation of signal integrity requirements.	Refer to Section 3.1 for more information.
	Traces: 5 mils wide, 10 mils spacing.	Refer to Section 9.12.1.1.

Table 138. Intel® 82801DB I/O Controller Hub 4 (ICH4) Layout Checklist (Sheet 2 of 5)

Checklist Items	Recommendations	Comments
General Guidelines	• Point-to-Point Single Solution - trace length range, Intel® 82801DB I/O Controller Hub 4 (ICH4) to Intel® 82562ET/ Intel® 82562EM Platform LAN Connect component should be 4.5 to 12 inches. Range for CNR is 2 to 9.5 inches. • LOM and CNR Solution - trace length range ICH4 to RPAK should be L1 = 0.5 to 7.5 inches. • Range for RPAK to PLC is L2 = 4 to (11.5 - L1) inches. • Range for RPAK to CNR is L2 = 1.5 to (9.0 - L1) inches. • CNR card trace length range is 0.5 to 3 inches. • Total trace length is not to exceed 9.5 inches.	• To meet timing requirements. • Refer to Section 9.12.1.1.1 for more information.
	Stubs due to RPAK CNR/LOM stuffing option should not be present on the surface.	To minimize inductance.
	All routing should reference V_{SS}.	
	Maximum mismatch between the length of LAN_CLK and the length of any data trace is 0.5 inch (clock must be the longest trace).	To meet timing and signal quality requirements.
	Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN phy.	To meet timing and signal quality requirements.
	Keep the total length of each differential pair under four inches.	Issues found with traces longer than four inches. • IEEE phy conformance failures • Excessive EMI and or degraded receive BER.
	Do not route the transmit differential traces closer than 100 mils to the receive differential traces.	To minimize crosstalk.
	Distance between differential traces and any other signal line must be at least 100 mils. (Intel recommends 300 mils.)	To minimize crosstalk.
	Differential trace impedance should be controlled to be ~100 Ω.	To meet timing and signal quality requirements.
	For high-speed signals, the number of corners and vias should be minimized. When a 90-degree bend is required, use two 45-degree bends.	To meet timing and signal quality requirements.
	Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
	Do not route traces and vias under crystals or oscillators.	This prevents coupling to or from the clock.

Table 138. Intel® 82801DB I/O Controller Hub 4 (ICH4) Layout Checklist (Sheet 3 of 5)

Checklist Items	Recommendations	Comments
General Guidelines	Trace width to height ratio above the ground plane should be between 1:1 and 3:1.	To control trace EMI radiation.
	Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.
	Vias to decoupling capacitors should be sufficiently large in diameter.	To decrease series inductance.
	Isolate I/O signals from high speed signals.	To minimize crosstalk.
	Avoid routing high-speed LAN or Phone line traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar device.	To minimize crosstalk.
	Place the Intel® 82562ET/ Intel® 82562EM Platform LAN Connect component more than 1.5 inches away from any board edge.	This minimizes the potential for EMI radiation problems.
	Place at least one bulk capacitor (4.7 µF or greater OK) on each side of the Intel® 82562ET/ Intel® 82562EM Platform LAN Connect component.	Research and development has shown that this is a robust design recommendation.
	Place decoupling capacitors (0.1 µF) as close to the Intel 82562ET/ Intel 82562EM Platform LAN Connect component as possible.	
ICH4 Power Decoupling		
V_CPU_IO[2:0]	Use one 0.1 µF and one 1 µF decoupling capacitor. Locate within 100 mils of the ICH4 package near ball AA23.	Refer to Section 12.4.5.1 for more information.
$V_{CC}3_3$	Requires six 0.1 µF decoupling capacitors. Place caps within 100 mils of the ICH4 package near balls A4, A1, H1, T1, AC10, and AC18.	
$V_{CCSUS}3_3$	Requires two 0.1 µF decoupling capacitors. Place within 100 mils of the ICH4 package near balls A22 and AC5.	
$V_{CC}1_5$	Requires two 0.1 µF decoupling capacitors. Place within 100 mils of the ICH4 package near balls K23 and C23.	
$V_{CCSUS}1_5$	Requires two 0.1 µF decoupling capacitors. Place within 100 mils of the ICH4 package near balls A16 and AC1.	
$V5_{REF_SUS}$	Requires one 0.1 µF decoupling capacitor. $V5_{REF_SUS}$ affects only 5 V tolerance for USB OC[5:0]# balls, and may be connected to $V_{CCSUS}3_3$ when 5 V tolerance on these signal is not required.	

Table 138. Intel® 82801DB I/O Controller Hub 4 (ICH4) Layout Checklist (Sheet 4 of 5)

Checklist Items	Recommendations	Comments
$V5_{REF}$	Requires one 0.1 µF decoupling capacitor placed near ball E7. $V5_{REF}$ is the reference voltage for 5 V tolerant inputs in the ICH4. Tie to balls $V5_{REF}$[2:1]. $V5_{REF}$ must power up before or simultaneous to $V_{CC}3_3$. It must power down after or simultaneous to $V_{CC}3_3$.	
V_{CCRTC}	Requires one 0.1 µF decoupling capacitor placed near ball AB5.	
V_{CCHI}	Requires two 0.1 µF decoupling capacitors placed near balls T23 and N23.	
V_{CCPLL}	Requires one 0.1 µF and one 0.01 µF decoupling capacitor placed near ball C22.	
RTC		
General Guidelines	• RTC ball to crystal termination trace length should be less than one inch. • Use five mil trace width (results in approximately 2 pF per inch). • Minimize capacitance between RTCX1 and RTCX2. • Put ground plane underneath crystal components. • Do not route switching signals under the external components (unless on other side of board).	Refer to Section 9.11.1 for more information.
USB		
General Guidelines	• Route all traces over continuous planes (ground) with no interruptions. Avoid crossing over anti-etch when possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.) • Keep traces at least 50 mils away from the edge of the reference ground plane. This helps prevent the coupling of the signal onto adjacent wires, and helps prevent free radiation of the signal from the edge of the PCB.	• Refer to Section 9.7.1 for detailed USB guidelines. • Refer to Section 9.7.1.4 for termination recommendations.

Table 138. Intel® 82801DB I/O Controller Hub 4 (ICH4) Layout Checklist (Sheet 5 of 5)

Checklist Items	Recommendations	Comments
General Guidelines	• Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. (Recommended: Use of impedance calculator to determine the trace width and spacing required for the specific board stack-up being used. Using 4 mil traces with 4.5 mil spacing results in approximately 90 Ω differential trace impedance. • Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 50 mils. • Use 20 mils minimum spacing between USB signal pairs and other signal traces. This helps to prevent crosstalk. • USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pairs should be no greater than 150 mils. • No termination resistors needed for USB.	• Refer to Section 9.7.1 for detailed USB guidelines. • Refer to Section 9.7.1.4 for termination recommendations.

Schematics A

The following schematics of the Intel® 855GME chipset are included in this section.

- Cover Page
- TABLES: Block Diagram
- TABLES: Reset Map
- TABLES: Clock Distribution
- TABLES: GPIO/IDSEL Mapping
- TABLES: Voltage Distribution
- CORE: CK_408 (Main Clock Generation)
- CORE: CPU Connector, 1 of 2
- CORE: CPU Connector, 2 of 2
- CORE: CPU Pull-Ups, PLL Circuitry, TJPRO Connector
- CORE: GMCH
- CORE: GMCH Circuitry
- CORE: GMCH PLL, Straps, LVDS Clock Generation
- CORE: DDR Series Termination
- CORE: DIMM Connectors
- CORE: DDR Parallel Termination (Strobes, CNTRL)
- CORE: DDR Vterm Caps
- CORE: AGP Digital Display Connector
- CORE: VGA Connector
- ICH: Intel® 82801DB I/O Controller Hub
- ICH: ICH Pull-up/Pull-downs
- CORE: LVDS
- ICH: IDE Primary and Secondary
- ICH: USB Back Panel Connectors
- ICH: USB Front Panel VREG and OC#
- ICH: PCI Slots 3 - 1
- ICH: PCI Pull-ups
- SMBUS Isolation
- LAN: Intel® 82562EM Platform LAN Connect
- AUDIO: Codec (AD1885 or CS4201)
- AUDIO: Codec Filtering Caps

- AUDIO: Aux-In, CD-In, Line-In: ATAPI Headers
- AUDIO: Mic-In
- AUDIO: Line-Out
- AUDIO: Front Panel Audio Header
- AUDIO: Transient Control
- AUDIO: Analog VREG
- SIO: LPC47M102
- SIO: Floppy
- SIO: Keyboard and Mouse Ports (PS/2)
- SIO: Parallel Port
- SIO: COM1
- FWH: MFG Mode and Recovery Jumpers
- GLUE4
- PC Speaker
- Front Panel Header
- Mounting Holes
- FAN: Fan Headers (3)
- VREG: 2.5 V Memory, Standby Memory
- VREG: 1.25 V Memory VVT
- VREG: ATX Power Connector 2X10
- VREG: Battery, PCI VAUX, USB_NCH and USB_PCH
- VREG: USB Back Panel, PS/2
- VREG: 1.5 V Stand-by and 3.3 V Stand-by
- VREG: Bulk Decoupling
- VREG: 2.5 V STR Decoupling
- VREG: Core 1.5 V
- VREG: Intel® IMVP-IV VReg
- VREG: CPU Decoupling, CPU VREG Decoupling
- DEBUG: ITP Port and Pull-ups
- Revision History

PAGE #	COMPONENT/FUNCTION
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3	TABLES: RESET MAP
4	TABLES: CLOCK DISTRIBUTION
5	TABLES: GPIO/IDSEL MAPPING
6	TABLES: VOLTAGE DISTRIBUTION
7	CORE: CK_408 (MAIN CLOCK GENERATOR)
8	CORE: CPU CONNECTOR 1 OF 2
9	CORE: CPU CONNECTOR 2 OF 2
10	CORE: CPU PULL-UPS,PLL CIRCUITRY,TJPRO CONN
11-13	CORE: 855GME GMCH
14	CORE: 855GME CIRCUITRY
15	CORE: 855GME PLL, STRAPS, LVDS CLOCK GEN
16	CORE: DDR SERIES TERMINATION
17	CORE: DIMM CONNECTORS
18-19	CORE: DDR PARALLEL TERM (STROBES, CNTL)
20	CORE: DDR VTERM CAPS
21	CORE: AGP DIGITAL DISPLAY CONNECTOR
22	CORE: VGA CONNECTOR
23-24	ICH: 82801DB I/O CONTROLLER HUB
25	ICH: ICH PULL-UP/PULL-DOWNS
26	CORE: LVDS
27	ICH: IDE PRIMARY & SECONDARY
28	ICH: USB BACK PANEL CONNECTORS
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30-32	ICH: PCI SLOTS 3 - 1, SLOT1 SHARED WITH EVMC
33	ICH: PCI PULL-UPS
34	SMBUS ISOLATION
35	LAN: 82562EM
36	AUDIO: CODEC (AD1981A)
37	AUDIO: CODEC FILTERING CAPS
38	AUDIO: AUX-IN, CD-IN, LINE-IN: ATAPI HEADERS
39	AUDIO: MIC-IN
40	AUDIO: LINE-OUT
41	AUDIO: FRONT PANEL AUDIO HEADER
42	AUDIO: TRANSIENT CONTROL
43	AUDIO: ANALOG VREG
44	SIO: LPC47M102
45	SIO: FLOPPY
46	SIO: KEYBOARD & MOUSE PORTS (PS/2)
47	SIO: PARALLEL PORT
48	SIO: COM1 (DFM29)

PAGE #	COMPONENT/FUNCTION
49	FWH: MFG MODE AND RECOVERY JUMPERS
50	GLUE4
51	PC SPEAKER
52	FRONT PANEL HEADER
53	LABELS / MOUNTING HOLES
54	FAN: FAN HEADERS (3)
55	VREG: 2.5V MEMORY, STANDBY-MEMORY
56	VREG: 1.25V MEMORY VTT
57	VREG: ATX POWER CONNECTOR 2X10
58	VREG: BATTERY, PCI VAUX, USB_NCH & USB_PCH
59	VREG: USB BACK PANEL, PS/2
60	VREG: 1.5V STBY & 3.3V STBY
61	VREG: BULK DECOUPLING
62	VREG: 2.5V STR DECOUPLING
63	VREG: CORE 1.5V
64	VREG: CPU MAIN REGULATOR (CPU_CORE)
65	VREG: CPU DECOUPLING, CPU VREG DECOUPLING
66	VREG: 855GM CORE REGULATOR, VCCP REGULATOR
67	DEBUG: TITLE PAGE
68	DEBUG: ITP PORT AND PULL-UPS
69	MOON ISA RESISTORS
70	CPU STATUS LEDS
71	DEBUG: DIAGNOSTIC LEDS ,JUMPERS (H_VID)
72	DEBUG: PORT80 DECODER
73	DEBUG: HUBLINK PROBE, POC CIRCUIT, LED STATUS
74	DEBUG: DIAGNOSTIC JUMPERS (SMI, STPCLK), SMA CONNECTOR
75	REVISION HISTORY

INTEL(R) PENTIUM(R) M PROCESSOR
INTEL(R) 82855GME GMCH
INTEL(R) 82801DB I/O CONTROLLER HUB 4

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NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

REVISIONS

REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE

855GME

CRB SCHEMATICS
2-DDR SDRAM, 8 LAYER, ATX

FAB B
REV 1.4

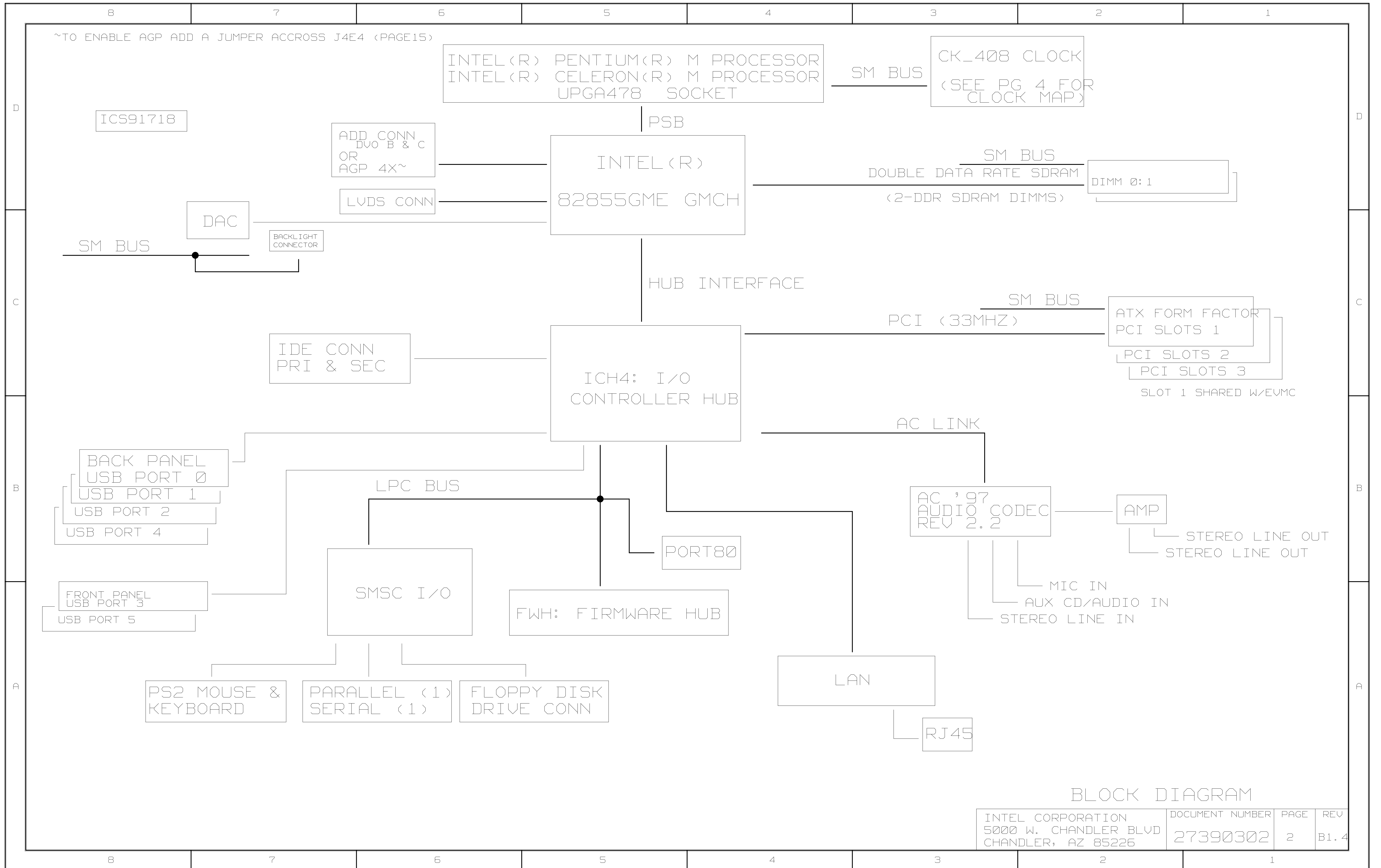
PBA: C24895-202

POWER SYMBOLS USED:
VCC3
VCC
VCCP
+12V
-12V

NOTES:

1. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
2. VCC = +5 VOLTS UNLESS OTHERWISE SPECIFIED.
3. VCC3 = +3.3 VOLTS UNLESS OTHERWISE SPECIFIED.
4. VCCP = +1.05 VOLTS UNLESS OTHERWISE SPECIFIED.
5. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	27390302	1/75	B1.4


~TO ENABLE AGP ADD A JUMPER ACCROSS J4E4 (PAGE15)
INTEL(R) PENTIUM(R) M PROCESSOR
INTEL(R) CELERON(R) M PROCESSOR
UPGA478 SOCKET
SM BUS
CK_408 CLOCK
(SEE PG 4 FOR CLOCK MAP)
ICS91718
PSB
ADD CONN
DVO B & C
OR
AGP 4X~
LVDS CONN
INTEL(R)
82855GME GMCH
SM BUS
DOUBLE DATA RATE SDRAM
DIMM 0:1
(2-DDR SDRAM DIMMS)
DAC
BACKLIGHT CONNECTOR
SM BUS
HUB INTERFACE
SM BUS
PCI (33MHZ)
ATX FORM FACTOR
PCI SLOTS 1
PCI SLOTS 2
PCI SLOTS 3
SLOT 1 SHARED W/EVMC
IDE CONN
PRI & SEC
ICH4: I/O
CONTROLLER HUB
AC LINK
BACK PANEL
USB PORT 0
USB PORT 1
USB PORT 2
USB PORT 4
LPC BUS
AC '97
AUDIO CODEC
REV 2.2
AMP
STEREO LINE OUT
STEREO LINE OUT
PORT80
FRONT PANEL
USB PORT 3
USB PORT 5
SMSC I/O
FWH: FIRMWARE HUB
MIC IN
AUX CD/AUDIO IN
STEREO LINE IN
LAN
PS2 MOUSE &
KEYBOARD
PARALLEL (1)
SERIAL (1)
FLOPPY DISK
DRIVE CONN
RJ45
BLOCK DIAGRAM
INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226
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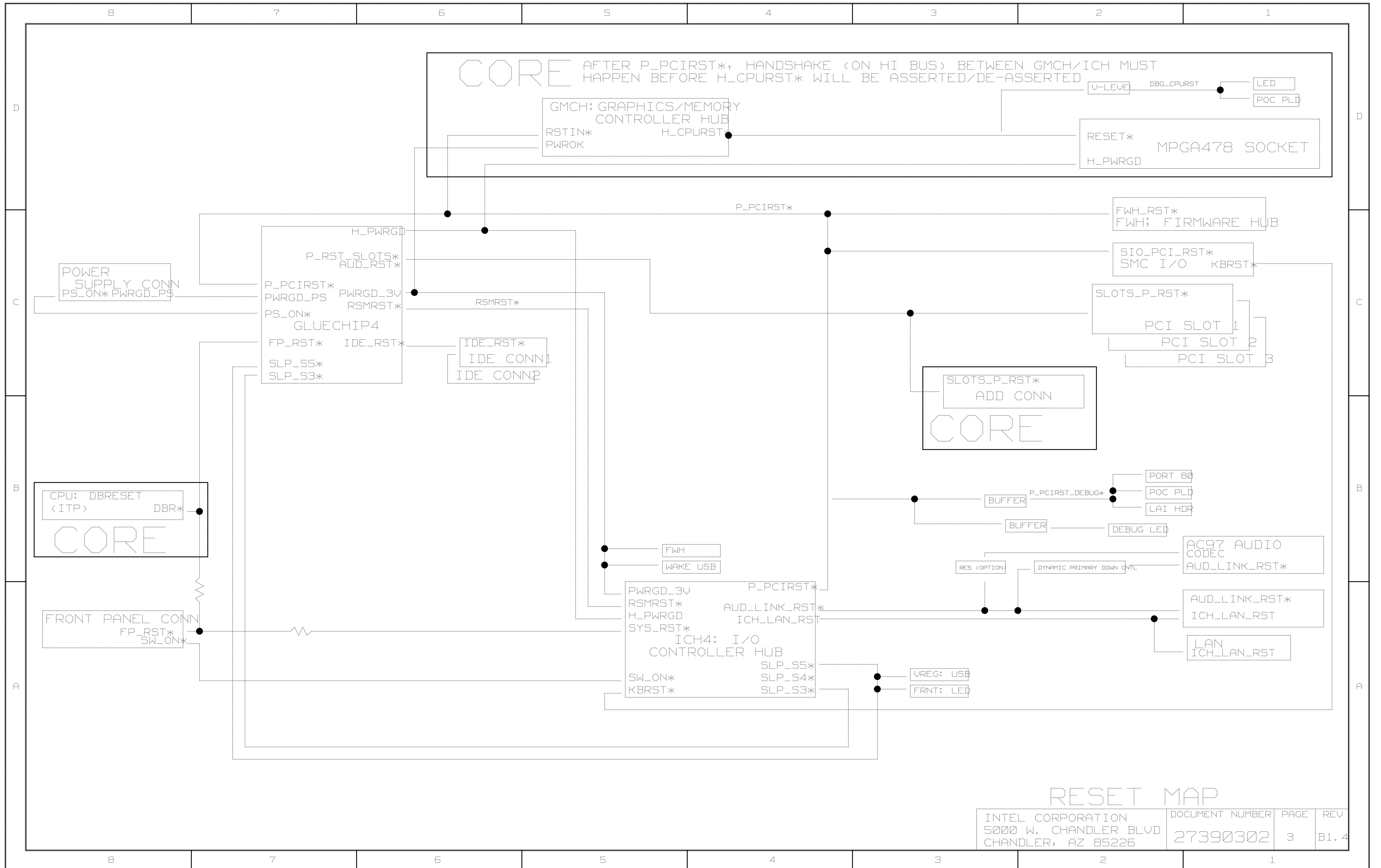

CORE
AFTER P_PCIRST*, HANDSHAKE (ON HI BUS) BETWEEN GMCH/ICH MUST
HAPPEN BEFORE H_CPURST* WILL BE ASSERTED/DE-ASSERTED
V-LEVEL
DBG_CPURST
LED
POC PLD
GMCH: GRAPHICS/MEMORY
CONTROLLER HUB
RSTIN*
PWROK
H_CPURST*
RESET*
MPGA478 SOCKET
H_PWRGD
P_PCIRST*
FWH_RST*
FWH; FIRMWARE HUB
SIO_PCI_RST*
SMC I/O
KBRST*
H_PWRGD
P_RST_SLOTS*
AUD_RST*
POWER
SUPPLY CONN
PS_ON*
PWRGD_PS
P_PCIRST*
PWRGD_PS
PS_ON*
PWRGD_3V
RSMRST*
GLUECHIP4
RSMRST*
SLOTS_P_RST*
PCI SLOT 1
PCI SLOT 2
PCI SLOT 3
FP_RST*
IDE_RST*
IDE_RST*
IDE CONN1
IDE CONN2
SLP_S5*
SLP_S3*
SLOTS_P_RST*
ADD CONN
CORE
CPU: DBRESET
(ITP)
DBR*
CORE
PORT 80
BUFFER
P_PCIRST_DEBUG*
POC PLD
LAI HDR
BUFFER
DEBUG LED
FWH
WAKE USB
AC97 AUDIO
CODEC
AUD_LINK_RST*
RES (OPTION)
DYNAMIC PRIMARY DOWN CNTL
PWRGD_3V
RSMRST*
H_PWRGD
SYS_RST*
P_PCIRST*
AUD_LINK_RST*
ICH_LAN_RST
AUD_LINK_RST*
ICH_LAN_RST
FRONT PANEL CONN
FP_RST*
SW_ON*
ICH4: I/O
CONTROLLER HUB
LAN
ICH_LAN_RST
SLP_S5*
SLP_S4*
SLP_S3*
SW_ON*
KBRST*
VREG: USB
FRNT: LED
RESET MAP
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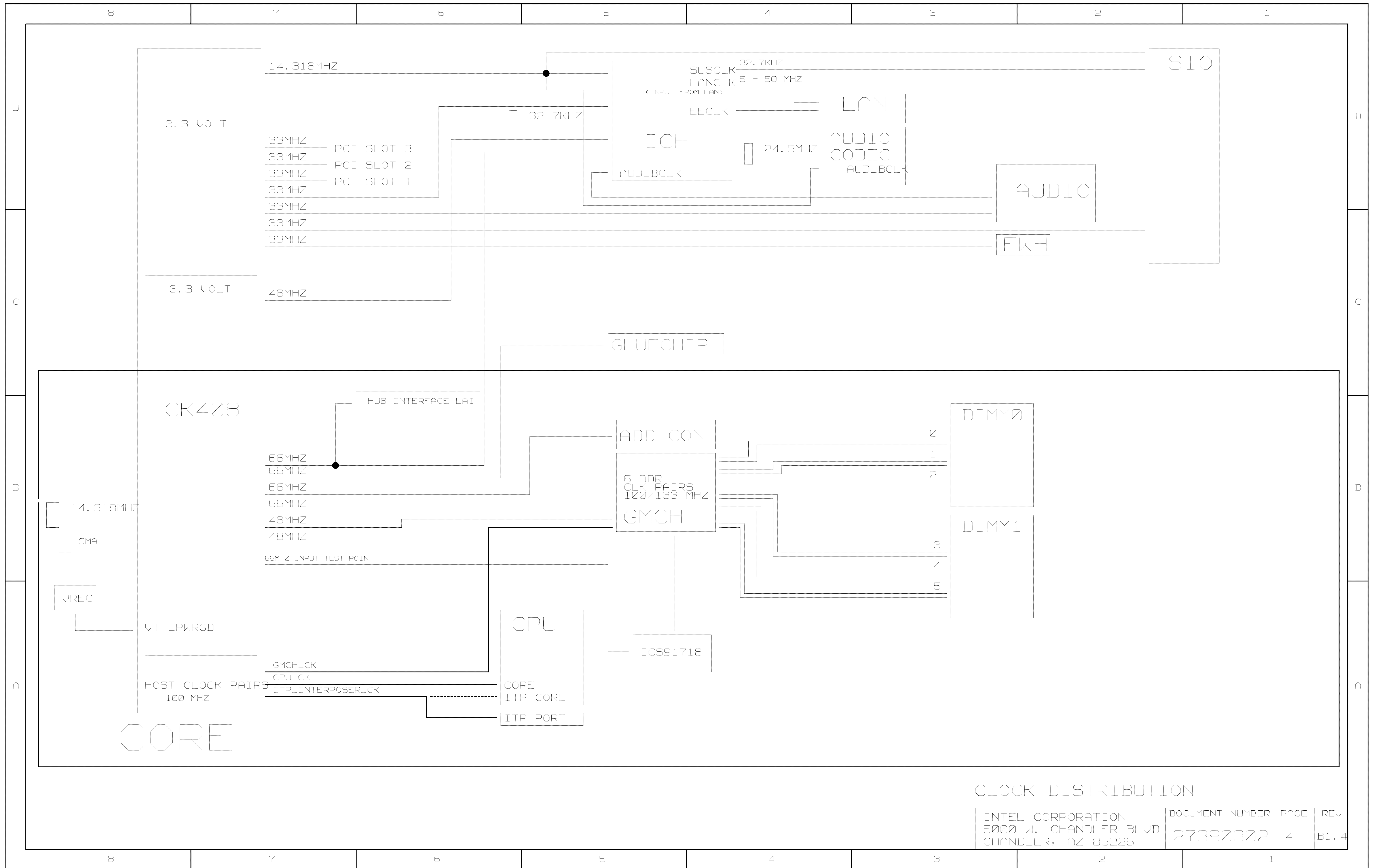

14.318MHZ
SUSCLK
LANCLK
(INPUT FROM LAN)
32.7KHZ
5 - 50 MHZ
SIO
LAN
EECLK
32.7KHZ
3.3 VOLT
ICH
AUDIO
CODEC
24.5MHZ
AUD_BCLK
33MHZ
PCI SLOT 3
33MHZ
PCI SLOT 2
33MHZ
PCI SLOT 1
33MHZ
AUD_BCLK
AUDIO
33MHZ
33MHZ
33MHZ
FWH
3.3 VOLT
48MHZ
GLUECHIP
CK408
HUB INTERFACE LAI
ADD CON
DIMM0
66MHZ
66MHZ
66MHZ
66MHZ
48MHZ
48MHZ
6 DDR
CLK PAIRS
100/133 MHZ
GMCH
DIMM1
14.318MHZ
SMA
66MHZ INPUT TEST POINT
VREG
VTT_PWRGD
CPU
ICS91718
GMCH_CK
CPU_CK
ITP_INTERPOSER_CK
HOST CLOCK PAIRS
100 MHZ
CORE
ITP CORE
ITP PORT
CORE
CLOCK DISTRIBUTION
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ICH4

PIN NAME	PWR WELL	USAGE	DURING RESET	S3/S4/S5	INTERNAL PULL-UP	NOTES
GPI(0)	CORE	P_REQA#	---	---		
GPI(1)	CORE	P_REQ5#	---	---		
GPI(2)	CORE	P_IRQE#	---	---		
GPI(3)	CORE	P_IRQF#	---	---		
GPI(4)	CORE	P_IRQG#	---	---		
GPI(5)	CORE	P_IRQH#	---	---		
GPI(6)	CORE	UNUSED	---	---		
GPI(7)	CORE	UNUSED	---	---		
GPI(8)	RESUME	UNUSED	---	---		
GPI(11)	RESUME	SMB_ALERT#	---	---		
GPI(12)	RESUME	LPC_SIO_SMI#	---	---		
GPI(13)	RESUME	LPC_SIO_PME#	---	---		
GPO(16)	CORE	P_GNTA#	HIGH	OFF	24K	
GPO(17)	CORE	P_GNT5#	HIGH	OFF	24K	
GPO(18)	CORE	UNUSED	HIGH	OFF		
GPO(19)	CORE	LVDS_BKLTSEL0	HIGH	OFF		
GPO(20)	CORE	LVDS_BKLTSEL1	HIGH	OFF		
GPO(21)	CORE	ISA_GO_NOGO	HIGH	OFF		
GPO(22)	CORE	UNUSED	HIGH-Z	OFF		
GPO(23)	CORE	UNUSED	LOW	OFF		
GPIO(24)	RESUME	UNUSED	LOW	DEFINED		
GPIO(25)	RESUME	GPO_GRN_BLNK	HIGH	DEFINED		
GPIO(27)	RESUME	GPO_YEL_BLNK	HIGH	DEFINED		
GPIO(28)	RESUME	GPO_LAN_DISABLE	HIGH	DEFINED		
GPIO(32)	CORE	UNUSED	HIGH	OFF		
GPIO(33)	CORE	GPO_AUD_EN*	HIGH	OFF		
GPIO(34)	CORE	UNUSED	HIGH	OFF		
GPIO(35)	CORE	UNUSED	HIGH	OFF		
GPIO(36)	CORE	UNUSED	HIGH	OFF		
GPIO(37)	CORE	(BOARD1)	HIGH	OFF		
GPIO(38)	CORE	(BOARD2)	HIGH	OFF		
GPIO(39)	CORE	(BOARD3)	HIGH	OFF		
GPIO(40)	CORE	(BOARD4)	HIGH	OFF		
GPIO(41)	CORE	UNUSED	HIGH	OFF		
GPIO(42)	CORE	UNUSED	HIGH	OFF		
GPIO(43)	CORE	UNUSED	HIGH	OFF		
RI*	RESUME					
THERM*	CORE					

FWH

PIN NAME	PWR WELL	USAGE	DURING RESET	S3/S4/S5	INTERNAL PULL-UP	NOTES
GPI4		CONFIG JUMPER	INPUT	DEFINED		CONFIG JUMPER
GPI3		MANUF MODE	INPUT	DEFINED		MANUF MODE
GPI2		HI/LOW BIOS CONFIG	INPUT	DEFINED		SPARE HI/LOW BIOS CONFIG STRAP
GPI1		GPIO_DMA66_DETECT_SEC	INPUT	DEFINED		ATA66 CABLE DETECT - SECONDARY
GPI0		GPIO_DMA66_DETECT_PRI	INPUT	DEFINED		ATA66 CABLE DETECT - PRIMARY

SIO

PIN NAME	PWR WELL	USAGE	DURING RESET	S3/S4/S5	INTERNAL PULL-UP	NOTES
GPIO20		RESISTOR STRAP OPTION	INPUT	DEFINED		DESIGN FEATURE WITH RESISTOR STRAPPING
GPIO21		RESISTOR STRAP OPTION	INPUT	DEFINED		DESIGN FEATURE WITH RESISTOR STRAPPING
GP027/IOSMI*		IO_SMI*	INPUT	DEFINED		SENDS IO SMI REQUEST TO ICH2

MULTI-PLEXED GPIO PINS ON SIO USED FOR SPECIFIC FUNCTIONS (NOT AS GPIO) ARE NOT IDENTIFIED HERE
UN-USED GPIO PINS ON SIO ARE NOT IDENTIFIED HERE

IRQ ROUTING TABLE

	AGP	SLOT1	SLOT2	SLOT3	AC97/ SMBUS	USB 2.0 #0	USB 2.0 #1	USB 2.0 #2	USB 2.0 #3	LAN
INT A	A			D			A			
INT B	B			C	A					
INT C				A					A	
INT D				B				A		
INT E		D	C							A
INT F		A	B							
INT G		B	A							
INT H		C	D			A				
REG /GNT		0	1	2						
IDSEL		16	17	18						24

GPIO, IRQ, IDSEL MAPS

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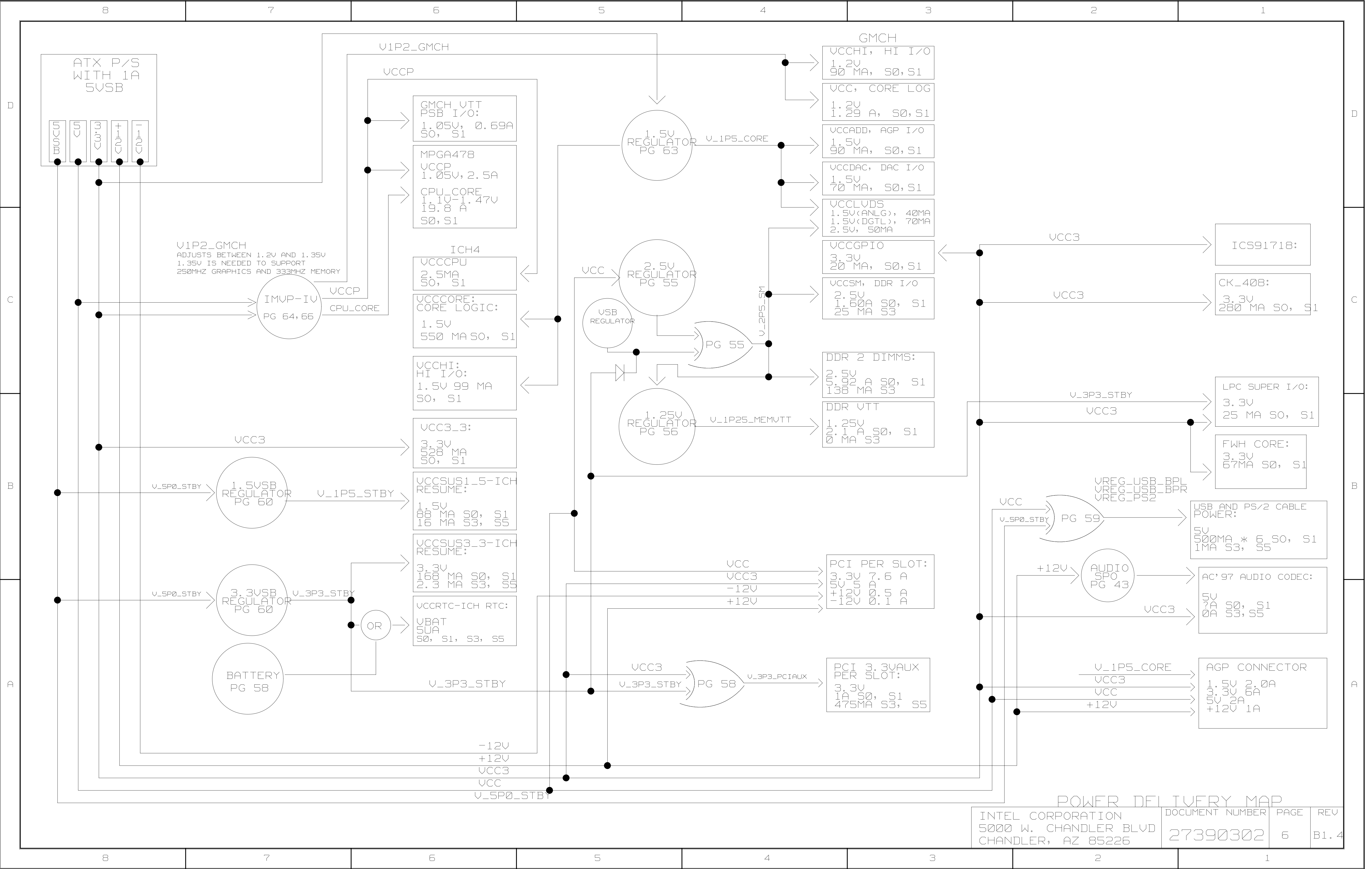

ATX P/S WITH 1A 5VSB
5VSB
5V
3.3V
+12V
-12V
V1P2_GMCH
VCCP
GMCH VTT PSB I/O: 1.05V, 0.69A S0, S1
MPGA478 VCCP 1.05V,2.5A CPU_CORE 1.1V-1.47V 19.8 A S0,S1
V1P2_GMCH
ADJUSTS BETWEEN 1.2V AND 1.35V
1.35V IS NEEDED TO SUPPORT
250MHZ GRAPHICS AND 333MHZ MEMORY
IMVP-IV PG 64,66
VCCP
CPU_CORE
ICH4
VCCCPU 2.5MA S0, S1
VCCCORE: CORE LOGIC: 1.5V 550 MA S0, S1
VCCHI: HI I/O: 1.5V 99 MA S0, S1
VCC3
VCC3_3: 3.3V 528 MA S0, S1
V_5P0_STBY
1.5VSB REGULATOR PG 60
V_1P5_STBY
VCCSUS1_5-ICH RESUME: 1.5V 88 MA S0, S1 16 MA S3, S5
V_5P0_STBY
3.3VSB REGULATOR PG 60
V_3P3_STBY
VCCSUS3_3-ICH RESUME: 3.3V 168 MA S0, S1 2.3 MA S3, S5
OR
VCCRTC-ICH RTC: VBAT 5UA S0, S1, S3, S5
BATTERY PG 58
V_3P3_STBY
1.5V REGULATOR PG 63
V_1P5_CORE
VCC
2.5V REGULATOR PG 55
VSB REGULATOR
PG 55
V_2P5_SM
1.25V REGULATOR PG 56
V_1P25_MEMVTT
GMCH
VCCHI, HI I/O 1.2V 90 MA, S0,S1
VCC, CORE LOG 1.2V 1.29 A, S0,S1
VCCADD, AGP I/O 1.5V 90 MA, S0,S1
VCCDAC, DAC I/O 1.5V 70 MA, S0,S1
VCCLVDS 1.5V(ANLG), 40MA 1.5V(DGTL), 70MA 2.5V, 50MA
VCCGPIO 3.3V 20 MA, S0,S1
VCCSM, DDR I/O 2.5V 1.60A S0, S1 25 MA S3
DDR 2 DIMMS: 2.5V 5.92 A S0, S1 138 MA S3
DDR VTT 1.25V 2.1 A S0, S1 0 MA S3
VCC
VCC3
-12V
+12V
PCI PER SLOT: 3.3V 7.6 A 5V 5 A +12V 0.5 A -12V 0.1 A
VCC3
V_3P3_STBY
PG 58
V_3P3_PCIAUX
PCI 3.3VAUX PER SLOT: 3.3V 1A S0, S1 475MA S3, S5
VCC3
ICS91718:
VCC3
CK_408: 3.3V 280 MA S0, S1
V_3P3_STBY
VCC3
LPC SUPER I/O: 3.3V 25 MA S0, S1
FWH CORE: 3.3V 67MA S0, S1
VREG_USB_BPL
VREG_USB_BPR
VREG_PS2
VCC
V_5P0_STBY
PG 59
USB AND PS/2 CABLE POWER: 5V 500MA * 6 S0, S1 1MA S3, S5
+12V
AUDIO SPO PG 43
AC'97 AUDIO CODEC: 5V ?A S0, S1 0A S3, S5
VCC3
V_1P5_CORE
VCC3
VCC
+12V
AGP CONNECTOR 1.5V 2.0A 3.3V 6A 5V 2A +12V 1A
-12V
+12V
VCC3
VCC
V_5P0_STBY
POWER DELIVERY MAP
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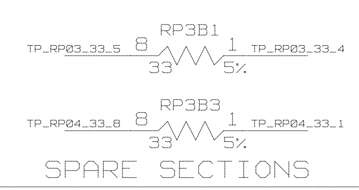
TURN-ON CK-408 WHEN GMCH/CPU/VCCP VOLTAGES ARE STABLE

DEFAULT = JUMP FOR 100MHZ SUPPORT

CAD NOTE:
TIE VSSA (U3F1-27)
DIRECTLY TO C13G4-2

SMB ADDRESS
11010010
D2 WRITE
D3 READ

SEL_2	SEL_1	SEL_0	FUNCTION
0	0	0	66 MHZ HOST CLOCK
0	0	1	100 MHZ HOST CLOCK
0	1	0	RESERVED
0	1	1	RESERVED
1	X	X	SEE CK-408 CLOCK SPEC
MID	0	0	ALL OUTPUTS HI-Z
MID	0	1	TEST MODE
MID	1	0	SEE CK-408 CLOCK SPEC
MID	1	1	SEE CK-408 CLOCK SPEC
			MID = 1.0V TO 1.8V



CK-408

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U8D1
PENTIUM_M_LAI

H_D<63..48>*
H_D<47..32>*
H_D<31..16>*
H_D<15..0>*
H_A<31..17>*
H_A<16..3>*
H_DBI<3>*
H_DBI<2>*
H_DBI<1>*
H_DBI<0>*
H_FERR*
H_IERR*
H_PROCHOT*
H_THERMTRIP*
H_TCK
H_TDI
H_TMS
H_TRST*
H_TDO

1 OF 6
PRELIMINARY IC

U8D1
PENTIUM_M_LAI

H_ADS*
H_BNR*
H_BR<0>*
H_DBSY*
H_DRDY*
H_STBP<3>*
H_STBP<2>*
H_STBP<1>*
H_STBP<0>*
H_RS<2..0>*
H_BPRI*
H_DEFER*
H_BPM5_PREQ*
H_CPURST*
H_TRDY*
H_BPM3_ITP*
H_BPM2_ITP*
H_BPM1_ITP*
H_BPM0_ITP*
H_STBN<3>*
H_STBN<2>*
H_STBN<1>*
H_STBN<0>*
H_REQ<4..0>*
H_HIT*
H_HITM*
H_LOCK*
H_BPM4_PRDY*

2 OF 6
PRELIMINARY IC

U8D1
PENTIUM_M_LAI

H_A20M*
H_DPSLP*
H_IGNNE*
H_INIT*
H_NMI
H_INTR
H_PWRGD
H_SMI*
H_SLP*
H_STPCLK*
CPU_GTLREF
H_DPWR*
CK_H_100M_ITP_CPU*
CK_H_100M_ITP_CPU
CPU_PLL3
CPU_PLL2
CPU_PLL1
CPU_VCCA
H_ADSTB1*
H_ADSTB0*
H_VID_ISOLATE<5..0>
CK_H_100M_CPU*
CK_H_100M_CPU
COMP3
COMP2
COMP1
COMP0
H_DBR*
H_TEMP_RET
H_TEMP_SRC
TEST1
TEST2
TEST3

C7D5 .01UF 10% 50V X7R 603
C7D4 10.0UF 20% 6.3V X5R 1206
VCCP

3 OF 6
PRELIMINARY IC

R3R1 1K 1% EMPTY 603
R3P3 1K 1% EMPTY 603
R2R2 1K 1% EMPTY 603

ROUTE DIFFERENTIALLY

R9C10 54.9 1% EMPTY 603
R9C8 54.9 1% EMPTY 603

VCCP
R2P7 4.7K 5% CH 603
H_DPSLP*

CPU 1 OF 2

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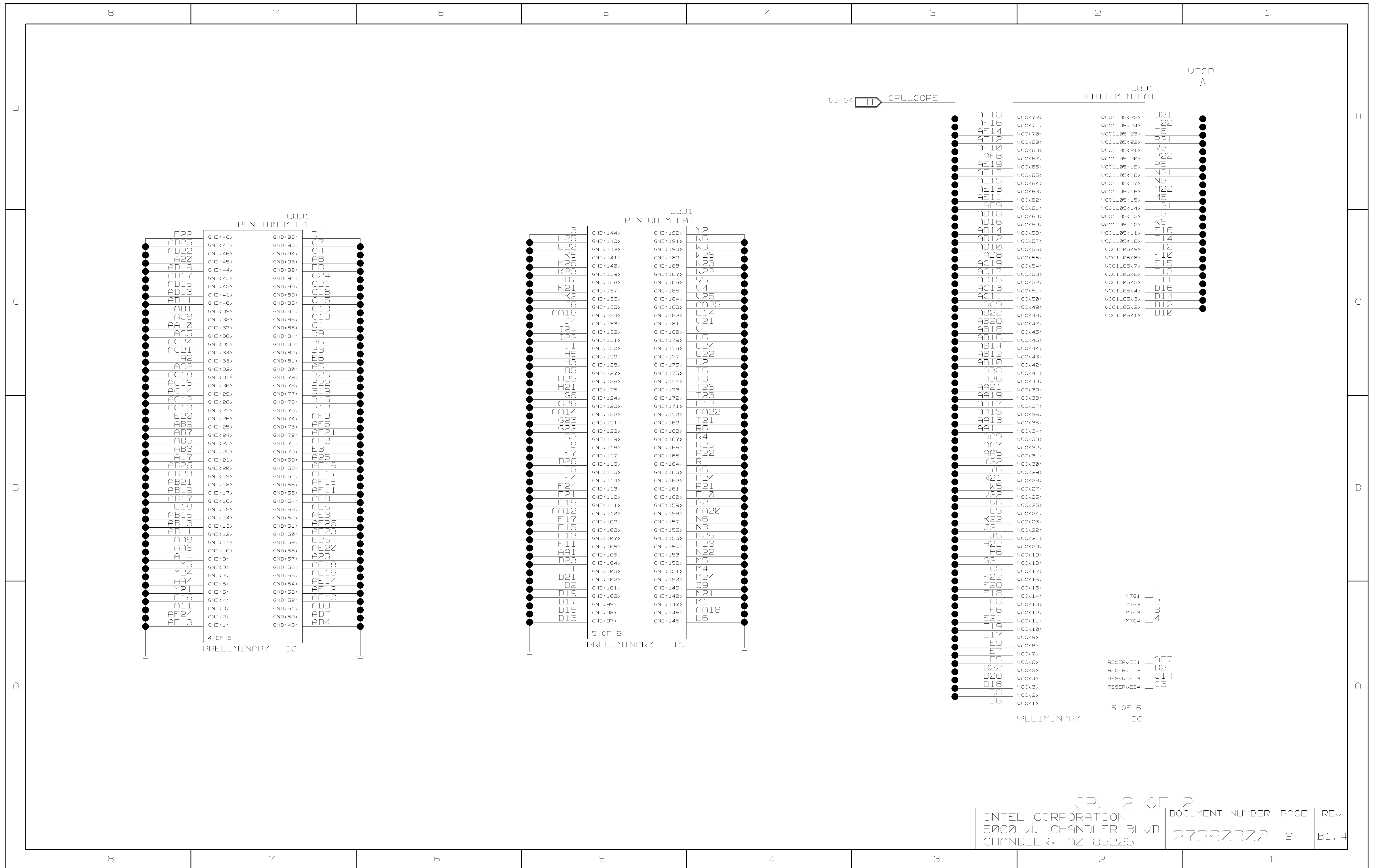

8
7
6
5
4
3
2
1
D
C
B
A
U8D1
PENTIUM_M_LAI
4 OF 6
PRELIMINARY IC
U8D1
PENIUM_M_LAI
5 OF 6
PRELIMINARY IC
65 64
IN
CPU_CORE
VCCP
U8D1
PENTIUM_M_LAI
6 OF 6
PRELIMINARY IC
MTG1
MTG2
MTG3
MTG4
RESERVED1
RESERVED2
RESERVED3
RESERVED4
AF7
B2
C14
C3
CPU 2 OF 2
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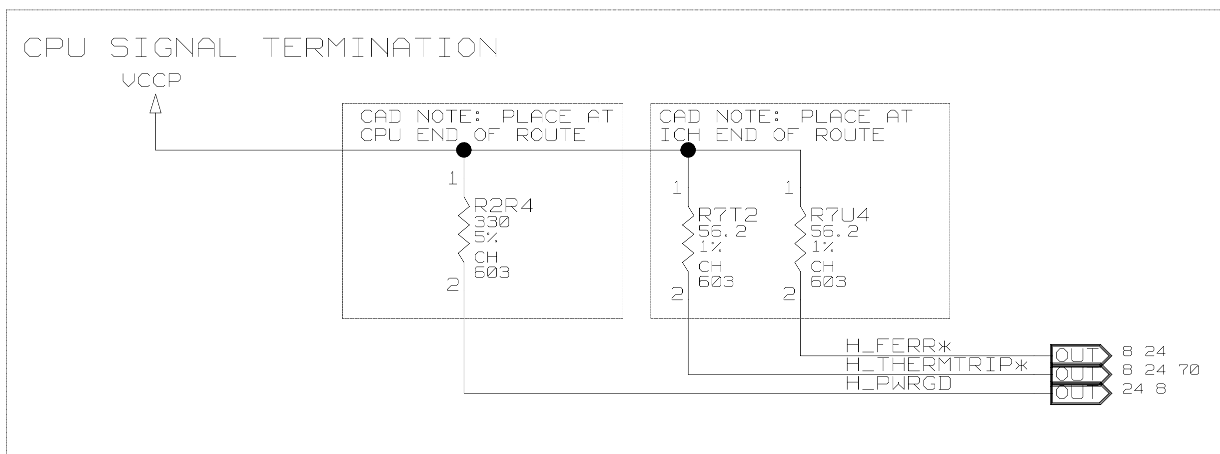

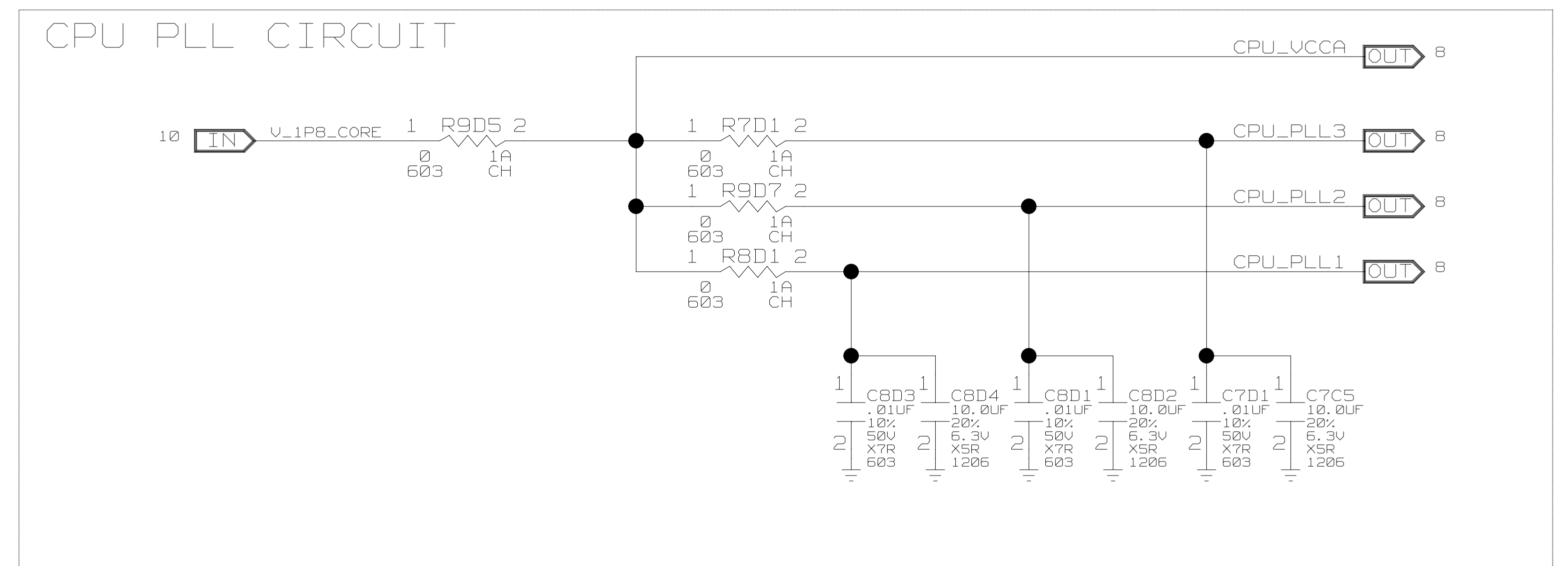

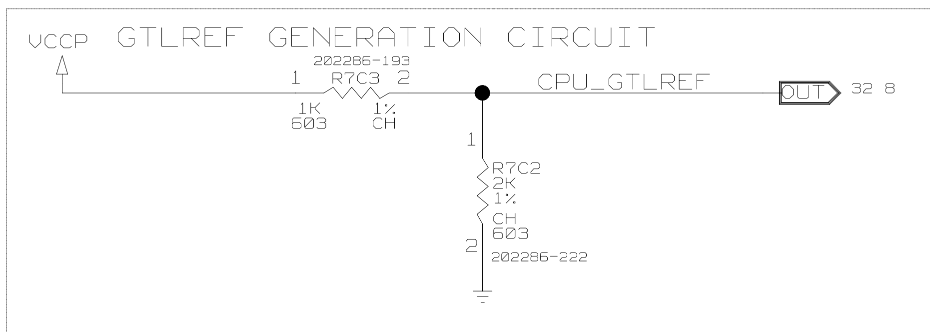

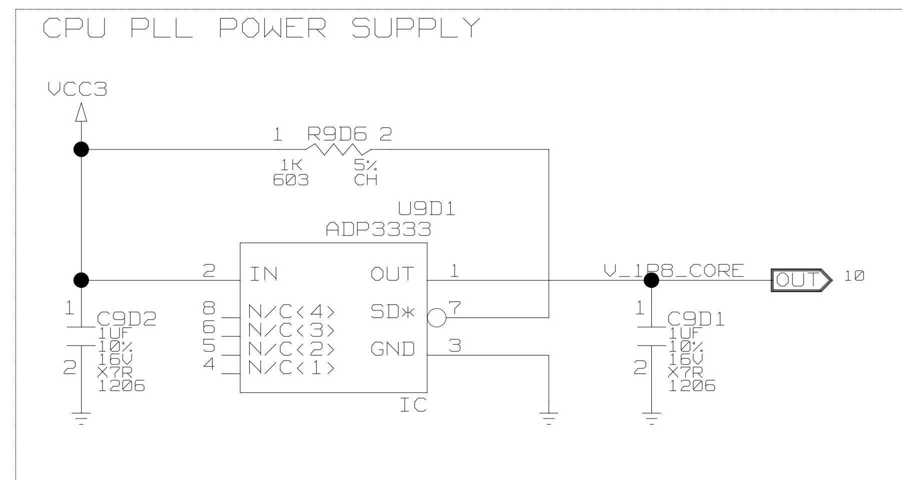

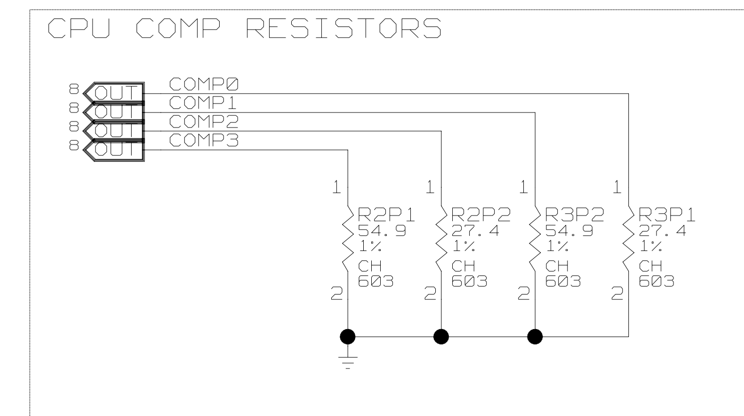

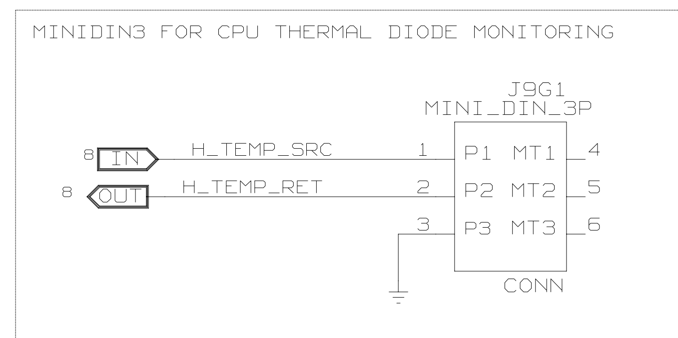

CPU CIRCUITS

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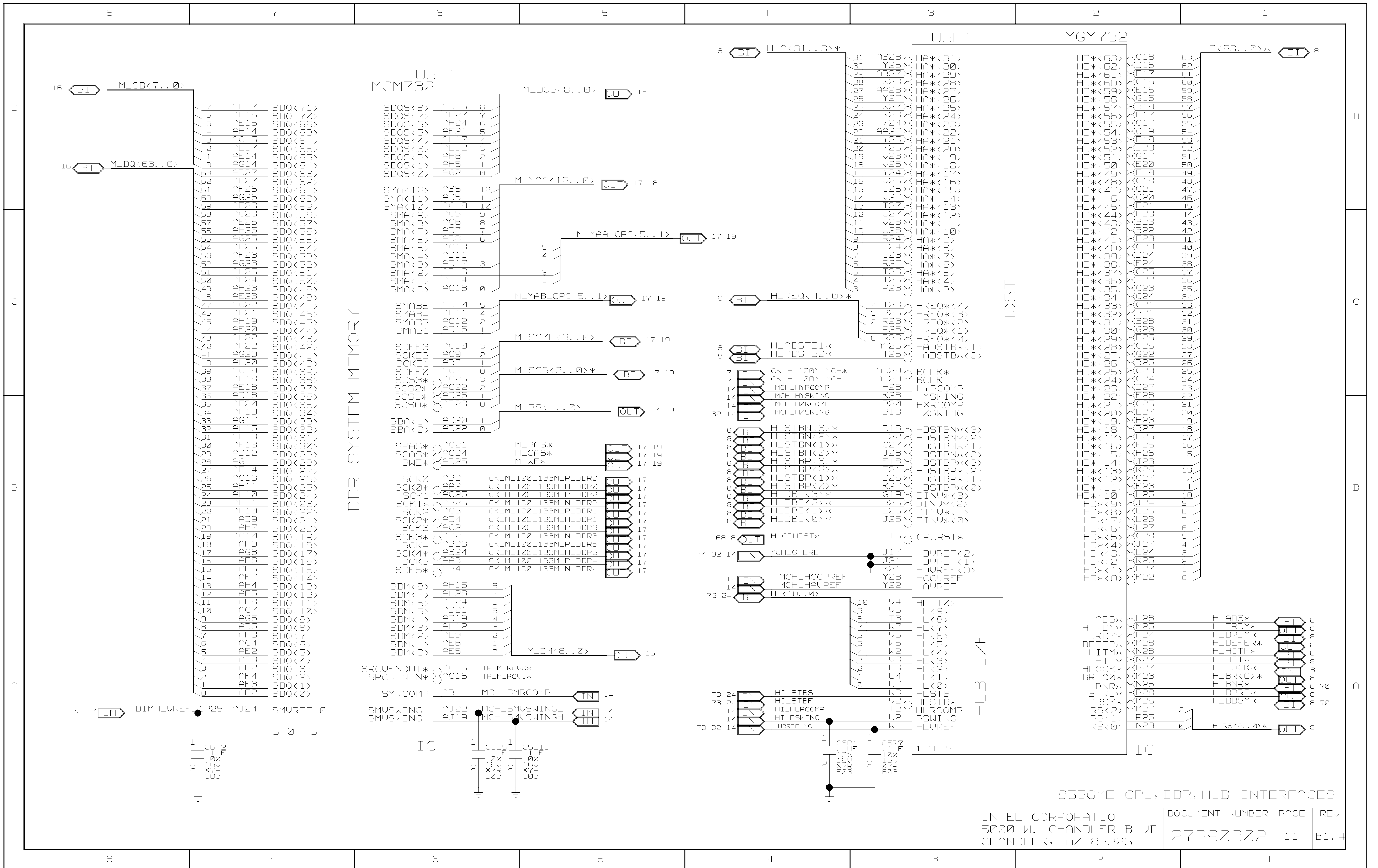
U5E1
MGM732
DDR SYSTEM MEMORY
5 OF 5
IC
M_CB<7..0>
M_DQ<63..0>
M_DQS<8..0>
M_MAA<12..0>
M_MAA_CPC<5..1>
M_MAB_CPC<5..1>
M_SCKE<3..0>
M_SCS<3..0>*
M_BS<1..0>
M_RAS*
M_CAS*
M_WE*
CK_M_100_133M_P_DDR0
CK_M_100_133M_N_DDR0
CK_M_100_133M_P_DDR2
CK_M_100_133M_N_DDR2
CK_M_100_133M_P_DDR1
CK_M_100_133M_N_DDR1
CK_M_100_133M_P_DDR3
CK_M_100_133M_N_DDR3
CK_M_100_133M_P_DDR5
CK_M_100_133M_N_DDR5
CK_M_100_133M_P_DDR4
CK_M_100_133M_N_DDR4
M_DM<8..0>
TP_M_RCVO*
TP_M_RCVI*
MCH_SMRCOMP
DIMM_VREF
MCH_SMVSWINGL
MCH_SMVSWINGH
C6F2
C6E5
C5E11
.1UF
10%
16V
X7R
603
U5E1
MGM732
HOST
HUB I/F
1 OF 5
IC
H_A<31..3>*
H_D<63..0>*
H_REQ<4..0>*
H_ADSTB1*
H_ADSTB0*
CK_H_100M_MCH*
CK_H_100M_MCH
MCH_HYRCOMP
MCH_HYSWING
MCH_HXRCOMP
MCH_HXSWING
H_STBN<3>*
H_STBN<2>*
H_STBN<1>*
H_STBN<0>*
H_STBP<3>*
H_STBP<2>*
H_STBP<1>*
H_STBP<0>*
H_DBI<3>*
H_DBI<2>*
H_DBI<1>*
H_DBI<0>*
H_CPURST*
MCH_GTLREF
MCH_HCCVREF
MCH_HAVREF
HI<10..0>
HI_STBS
HI_STBF
HI_HLRCOMP
HI_PSWING
HUBREF_MCH
C6R1
C5R7
H_ADS*
H_TRDY*
H_DRDY*
H_DEFER*
H_HITM*
H_HIT*
H_LOCK*
H_BR<0>*
H_BNR*
H_BPRI*
H_DBSY*
H_RS<2..0>*
855GME-CPU, DDR, HUB INTERFACES
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U5E1
MGM732

DAC
BLUE C9 VGA_BLUE OUT 12 22
BLUE* D9
GREEN C8 VGA_GREEN OUT 12 22
GREEN* D8
RED A7 VGA_RED OUT 12 22
RED* A8
HSYNC H10 VGA_HSYNC OUT 22
VSYNC J9 VGA_VSYNC OUT 22
REFSET E8 VGA_REFSET IN 14
DDCACLK B6 GLUE4_DDCSCL_3V BI 50
DDCADATA G9 GLUE4_DDCSDA_3V BI 50

LVDS
IYAM<3> C13, IYAM<2> C15, IYAM<1> E15, IYAM<0> G14 — LVDS_YAM<3..0> OUT 26
IYAP<3> B13, IYAP<2> C14, IYAP<1> E14, IYAP<0> F14 — LVDS_YAP<3..0> OUT 26
IYBM<3> G11, IYBM<2> C12, IYBM<1> E12, IYBM<0> H12 — LVDS_YBM<3..0> OUT 26
IYBP<3> G10, IYBP<2> C11, IYBP<1> E11, IYBP<0> G12 — LVDS_YBP<3..0> OUT 26
ICLKAM D14 LVDS_CLKAM OUT 26
ICLKAP E13 LVDS_CLKAP OUT 26
ICLKBM E10 LVDS_CLKBM OUT 26
ICLKBP F10 LVDS_CLKBP OUT 26
DDCPCLK B4 LVDS_DDCPCLK BI 26
DDCPDATA C5 LVDS_DDCPDATA BI 26
PANELBKLTCTL G8 LVDS_BKLTCTL OUT 26
PANELBKLTEN F8 LVDS_BKLTEN OUT 26
PANELVDDEN A5 LVDS_VDDEN OUT 26
LIBG A10 LVDS_LVBG
R5D2 1.5K 1% CH 603

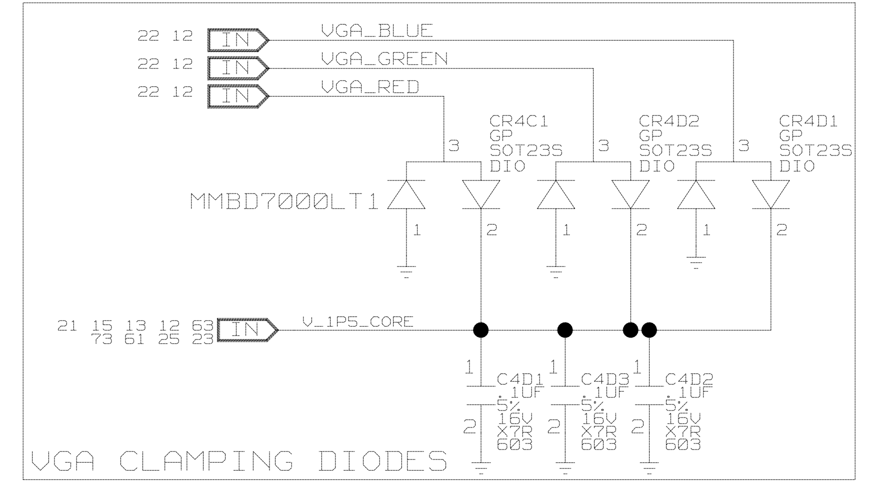
CLKS
DREFCLK B7 CK_48M_DOTCLK IN 7
DREFSSCLK B17 DREFSSCLK IN 15
LCLKCTLA H9 LCLKCTLA BI 15 26
LCLKCTLB C6 LCLKCTLB BI 15 26

MISC
DPWR* AA22 H_DPWR* OUT 8
DPSLP* Y23 MCH_DPSLP*
RSTIN* AD28 P_PCIRST* IN 25 15 44 49 50 71 72
VCCP R4R2 1K 5% CH 603
PWROK J11
EXTTS_0 D6
R5P8 0 603 1A EMPTY PWRGD_3V IN 50 24 29 49 59 66
R5P9 0 603 1A CH CPU_VR_PWRGD IN 64 7
MCH_EXTTS IN 15

NC
N/C1 A2, N/C2 A28, N/C3 A29, N/C4 AA9, N/C5 AH1, N/C6 AH29, N/C7 AJ2, N/C8 AJ28, N/C9 AJ29, N/C10 AJ4, N/C11 B1, N/C12 B29

DVO
21 BI DVOBD<11..0>: DVOBD<11> M5, DVOBD<10> M1, DVOBD<9> N3, DVOBD<8> N2, DVOBD<7> P2, DVOBD<6> N5, DVOBD<5> P5, DVOBD<4> P6, DVOBD<3> R4, DVOBD<2> R6, DVOBD<1> R5, DVOBD<0> R3
23 21 15 13 12 63 73 61 25 IN V_1P5_CORE — R5D6 100K 1% CH 603
21 BI DVOBCLK P3
21 BI DVOBCLK* P4
21 BI DVOBHSYNC T6
21 BI DVOBVSYNC T5
21 BI DVOBBLANK* L2
21 BI DVOBFLDSTL M2
21 BI DVOBCINTRB G2 DVOBCINTR*
21 BI DVOBCCLKINT M3
21 BI DVOCD<11..0>: DVOCD<11> G3, DVOCD<10> H6, DVOCD<9> H4, DVOCD<8> H3, DVOCD<7> H1, DVOCD<6> H2, DVOCD<5> J5, DVOCD<4> J6, DVOCD<3> K2, DVOCD<2> K3, DVOCD<1> K1, DVOCD<0> K5
R3E6 100K 1% CH 603
R3E7 100K 1% CH 603
21 BI DVOCCLK J3
21 BI DVOCCLK* J2
21 BI DVOCHSYNC K6
21 BI DVOCVSYNC L5
21 BI DVOCBLANK* L3
21 BI DVOCFLDSTL H5
R3D4 100K 1% CH 603
21 BI MI2CCLK K7
21 BI MI2CDATA N6
21 BI MDVICLK N7
21 BI MDVIDATA M6
21 BI MDDCCLK P7
21 BI MDDCDATA T7
21 BI ADDID<7..0>: ADDID<7> F6, ADDID<6> G6, ADDID<5> F4, ADDID<4> G5, ADDID<3> E2, ADDID<2> E3, ADDID<1> F5, ADDID<0> E5
21 15 BI DVODETECT L7
21 12 BI DPMS_CLK D5 DPMS
32 21 BI DVO_VREF F1 GVREF
AGP_BUSY* F7 AGPBUSY*
C5D18 .1UF 10% 16V X7R 603
14 BI MCH_DVORCOMP D1 DVORCOMP
7 BI CK_66M_GMCH Y3 GCLKIN
RSVD1 AA5, RSVD2 B12
21 BI ADD_RSVD_A8 B2 RSVD3
21 BI ADD_RSVD_B8 B3 RSVD4
21 15 BI AGP_ST2 C2 RSVD5
RSVD6 D12
21 BI ADD_RSVD_A14 D2 RSVD7
21 BI ADD_RSVD_B12 D3 RSVD8
RSVD9 D7
RSVD10 F12
21 BI ADD_RSVD_B18 F2 RSVD11
21 BI ADD_RSVD_A18 F3 RSVD12
21 BI ADD_RSVD_B39 L4 RSVD13
21 15 BI AGP_ST1 C3 GST<1>
21 15 BI AGP_ST0 C4 GST<0>
VCC3 R5D4 8.2K 5% CH 603 AGP_BUSY*

2 OF 5
IC



73 61 25 23 21 15 13 12 63 IN V_1P5_CORE R2G142 1K 603 5% CH
DPMS_CLK_R R7N1 0 603 1A CH DPMS_CLK OUT 12 21
Q2G1 FET BSS138LT3
44 24 IN SUSCLK

855GME-VIDEO, CLKS, CTRL, POWER, GND

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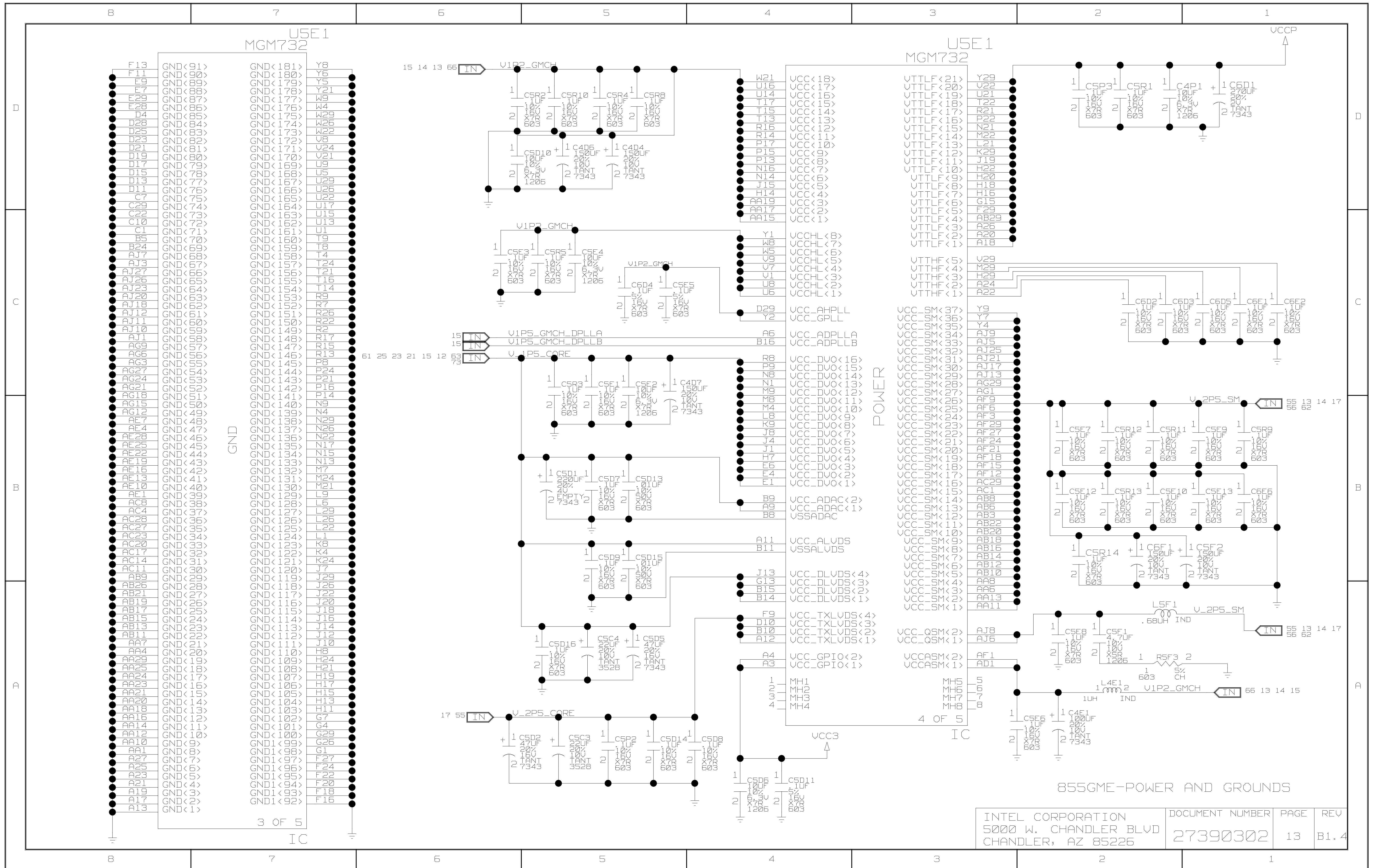
U5E1
MGM732
GND
3 OF 5
IC
U5E1
MGM732
POWER
4 OF 5
IC
V1P2_GMCH
V1P5_GMCH_DPLLA
V1P5_GMCH_DPLLB
V_1P5_CORE
V_2P5_CORE
V_2P5_SM
VCCP
VCC3
855GME-POWER AND GROUNDS
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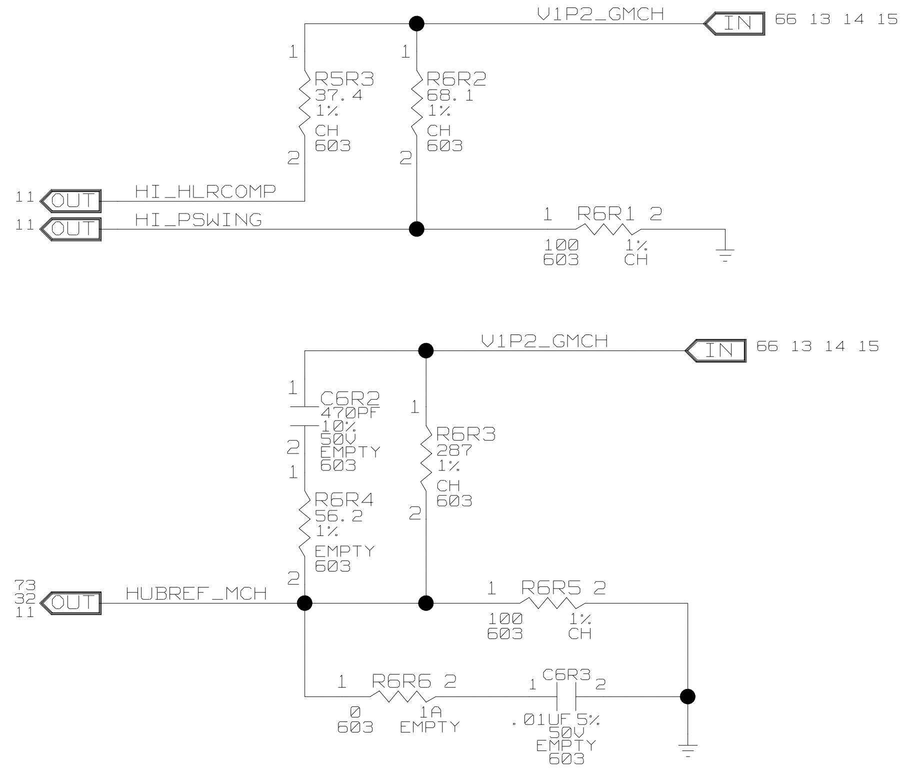
HUBLINK

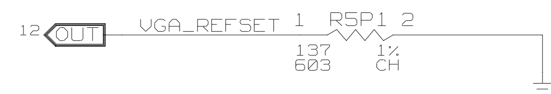


GMCH CORE VOLTAGE TABLE

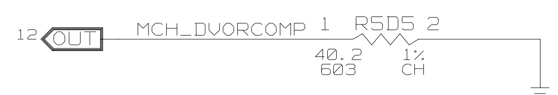
RESISTOR	1.2V	1.35V
R6R3	243, 1%	287, 1%
R5R3	27.4, 1%	37.4, 1%
R6R2	49.9, 1%	68.1, 1%

NOTE: SEE PG66 FOR RELATED STUFFING OPTIONS

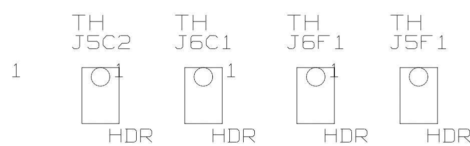
DAC



DVO

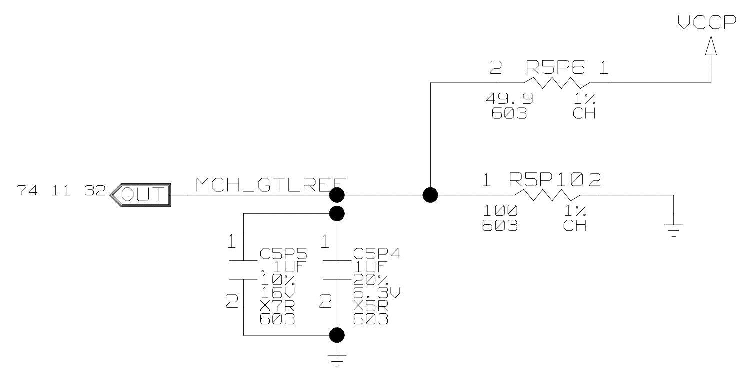


HEATSINK RETENTION CLIPS: QTY(4)

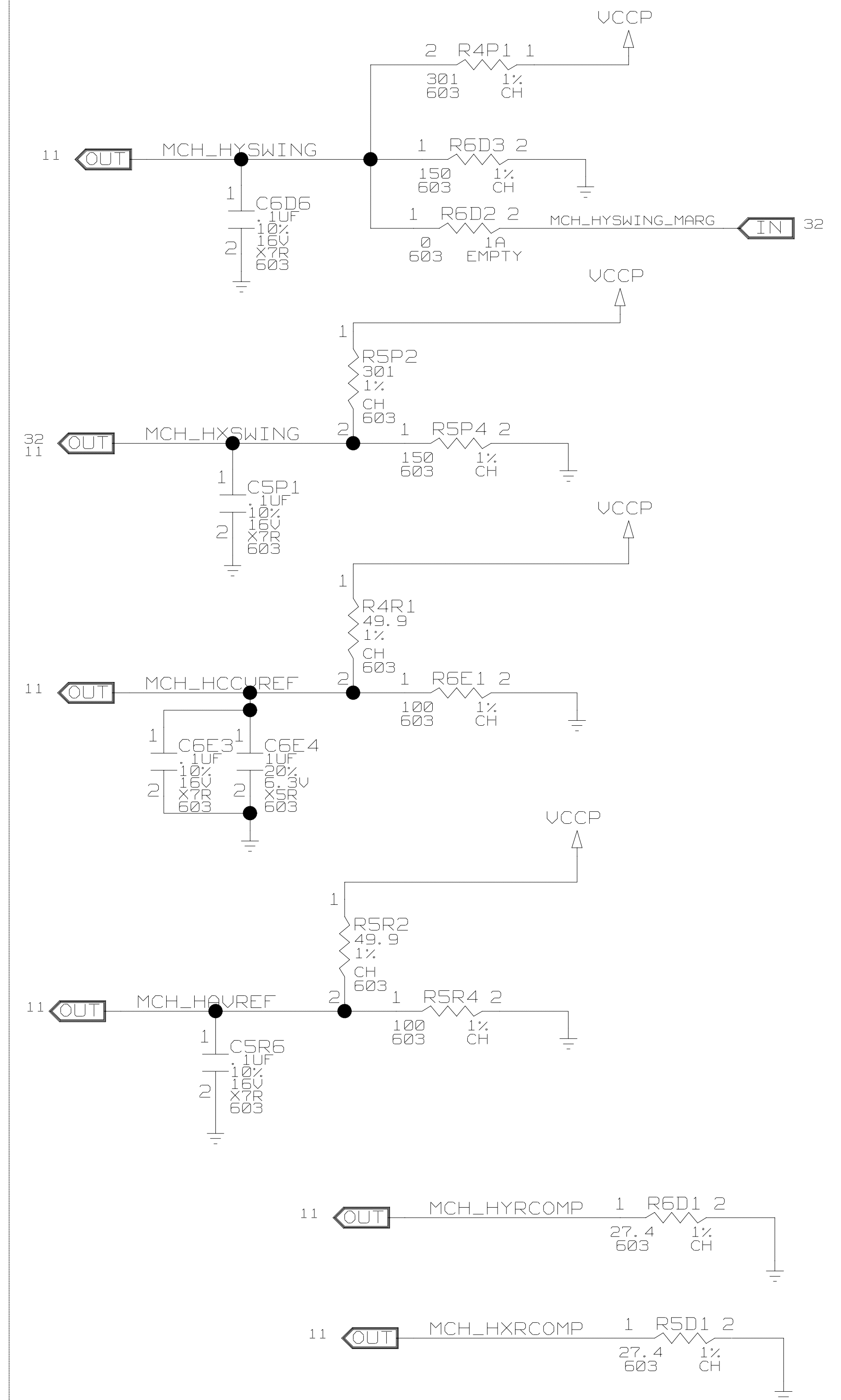


MEMORY

GTL

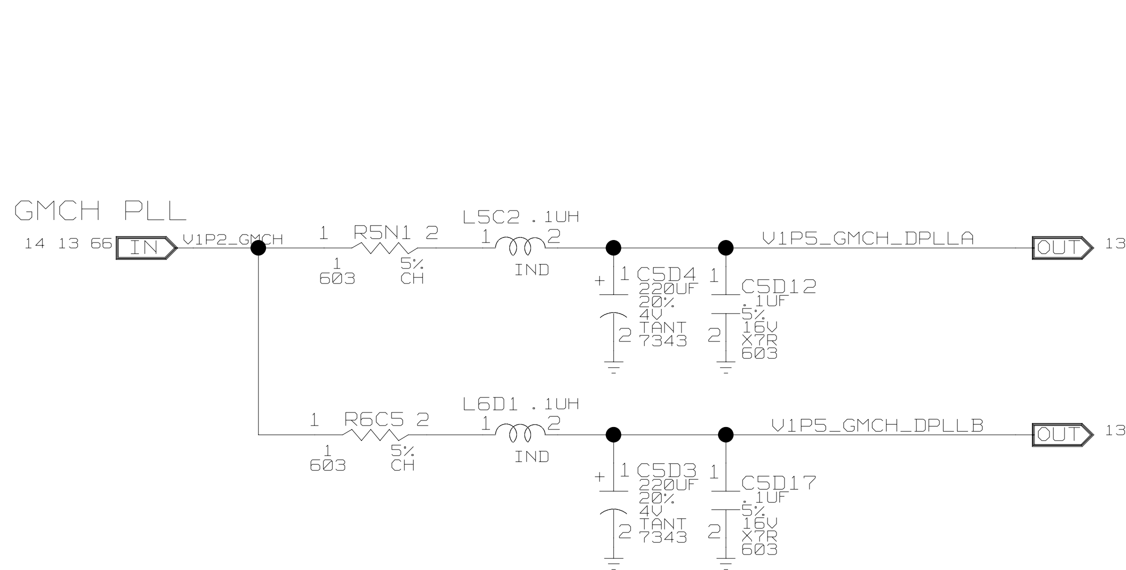


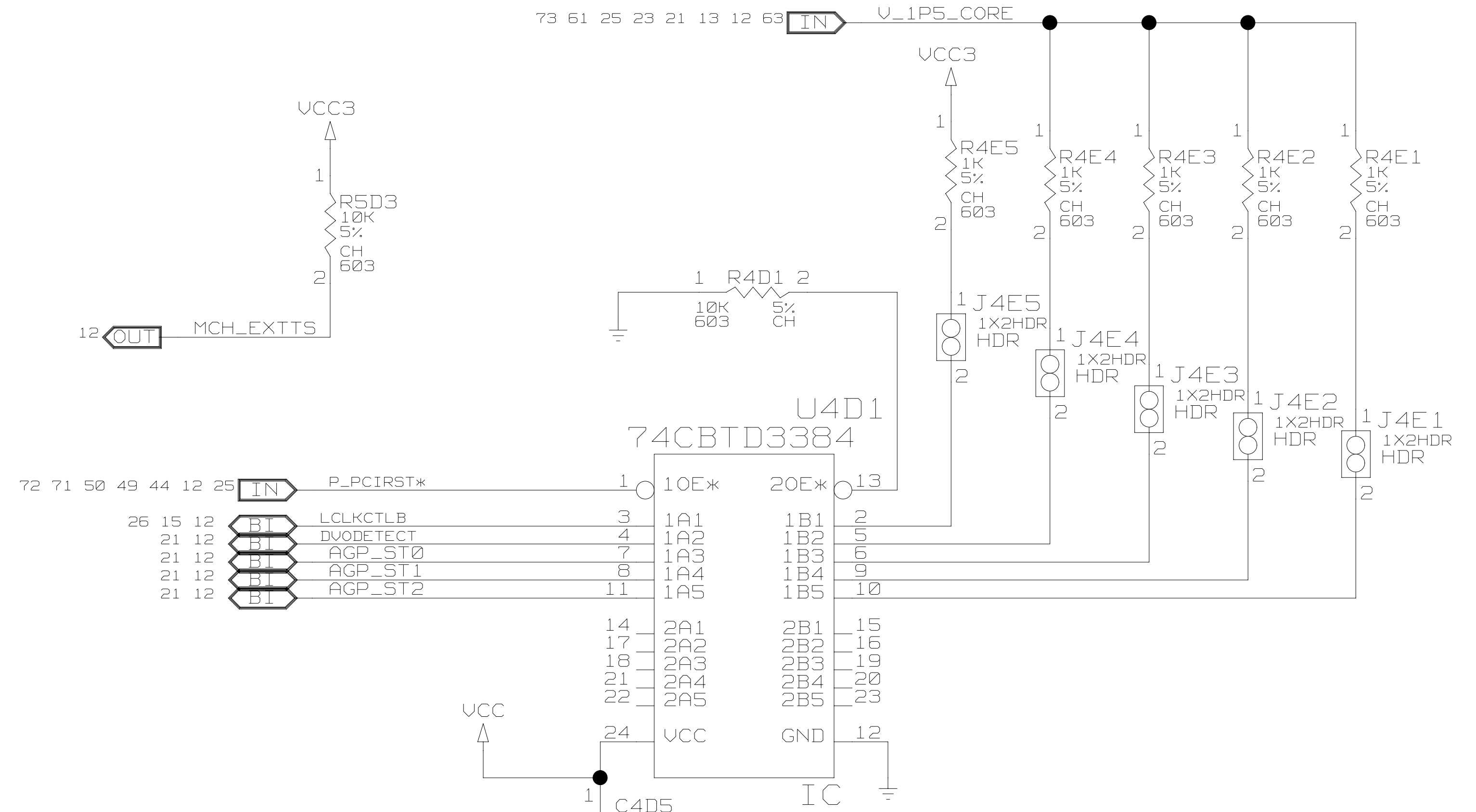
MCH COMPENSATION & REFERENCE VOLTAGE



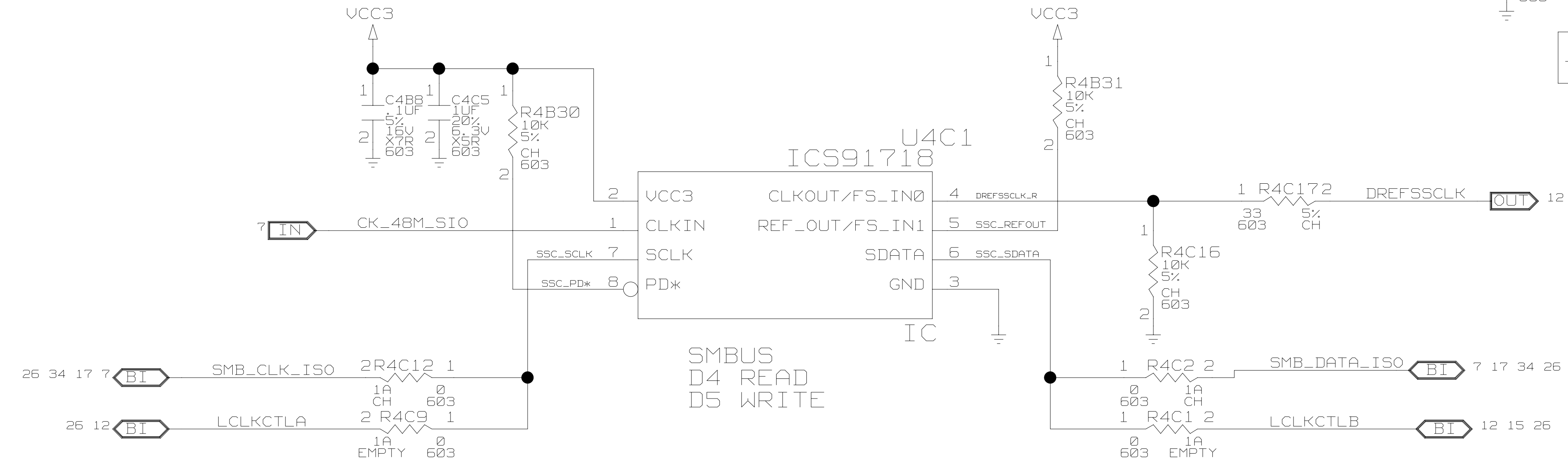
855GME-CIRCUITRY

GMCH STRAPPING OPTIONS





SPREAD SPECTRUM CLOCK GENERATOR FOR LVDS DISPLAY PLL



GMCH STRAPPING OPTIONS

	FUNCTION	BOAD DEFAULT	OPTIONAL OVERIDE
J4E4	DVO/AGP STRAP	NO SHUNT FOR DVO	SHUNT FOR AGP

GMCH FREQUENCY STRAPPING

J4E1	J4E2	J4E3	FSB FREQ	MEM FREQ	GFX FREQ
0	0	0	400	266	200
0	0	1	400	200	200
0	1	0	400	200	133
1*	1*	1*	400	333	250

* DEFAULT STRAPPING
0 = NO SHUNT 1 = SHUNT

GMCH PLL AND STRAPPING & LVDS CLOCK

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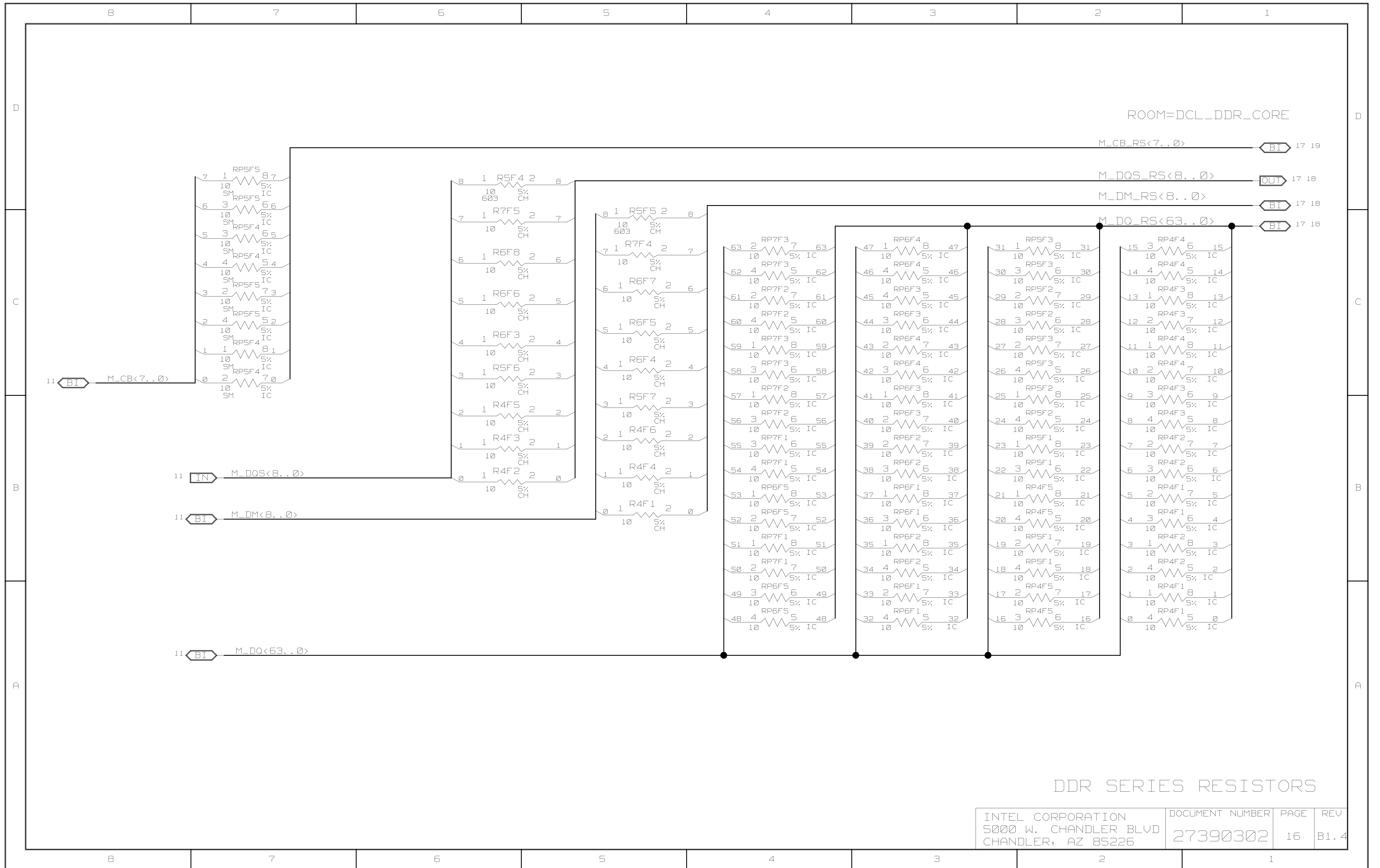

ROOM=DCL_DDR_CORE
M_CB_RS<7..0>
M_DQS_RS<8..0>
M_DM_RS<8..0>
M_DQ_RS<63..0>
M_CB<7..0>
M_DQS<8..0>
M_DM<8..0>
M_DQ<63..0>
DDR SERIES RESISTORS
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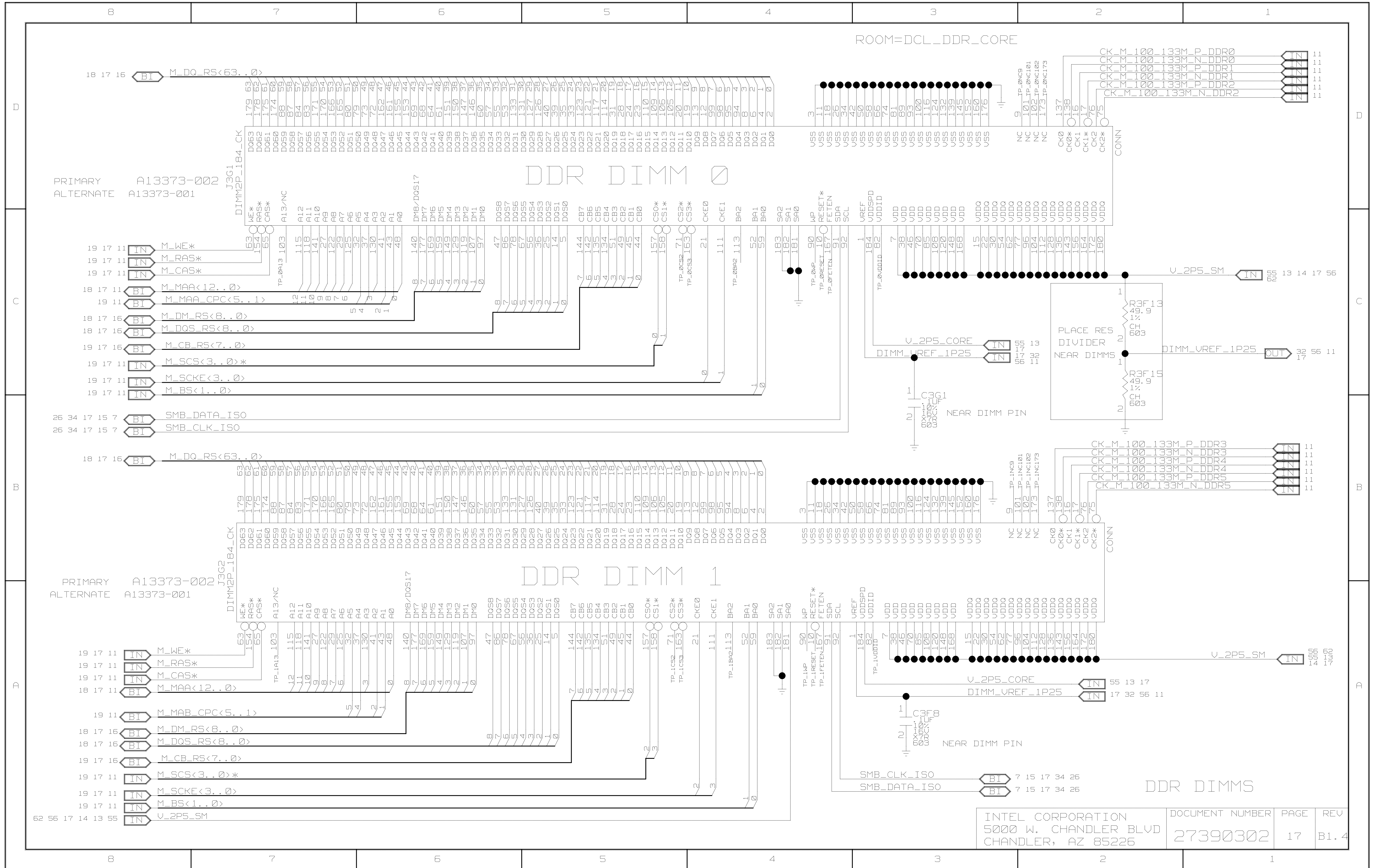
ROOM=DCL_DDR_CORE
DDR DIMM 0
PRIMARY A13373-002
ALTERNATE A13373-001
J3G1
DIMM2P_184_CK
M_DQ_RS<63..0>
M_WE*
M_RAS*
M_CAS*
M_MAA<12..0>
M_MAA_CPC<5..1>
M_DM_RS<8..0>
M_DQS_RS<8..0>
M_CB_RS<7..0>
M_SCS<3..0>*
M_SCKE<3..0>
M_BS<1..0>
SMB_DATA_ISO
SMB_CLK_ISO
CK_M_100_133M_P_DDR0
CK_M_100_133M_N_DDR0
CK_M_100_133M_P_DDR1
CK_M_100_133M_N_DDR1
CK_M_100_133M_P_DDR2
CK_M_100_133M_N_DDR2
V_2P5_SM
V_2P5_CORE
DIMM_VREF_1P25
PLACE RES DIVIDER NEAR DIMMS
R3F13 49.9 1% CH 603
R3F15 49.9 1% CH 603
C3G1 1UF 10% 16V X7R 603
NEAR DIMM PIN
DDR DIMM 1
PRIMARY A13373-002
ALTERNATE A13373-001
J3G2
DIMM2P_184_CK
M_MAB_CPC<5..1>
CK_M_100_133M_P_DDR3
CK_M_100_133M_N_DDR3
CK_M_100_133M_P_DDR4
CK_M_100_133M_N_DDR4
CK_M_100_133M_P_DDR5
CK_M_100_133M_N_DDR5
C3F8 1UF 10% 16V X7R 603
NEAR DIMM PIN
DDR DIMMS
INTEL CORPORATION
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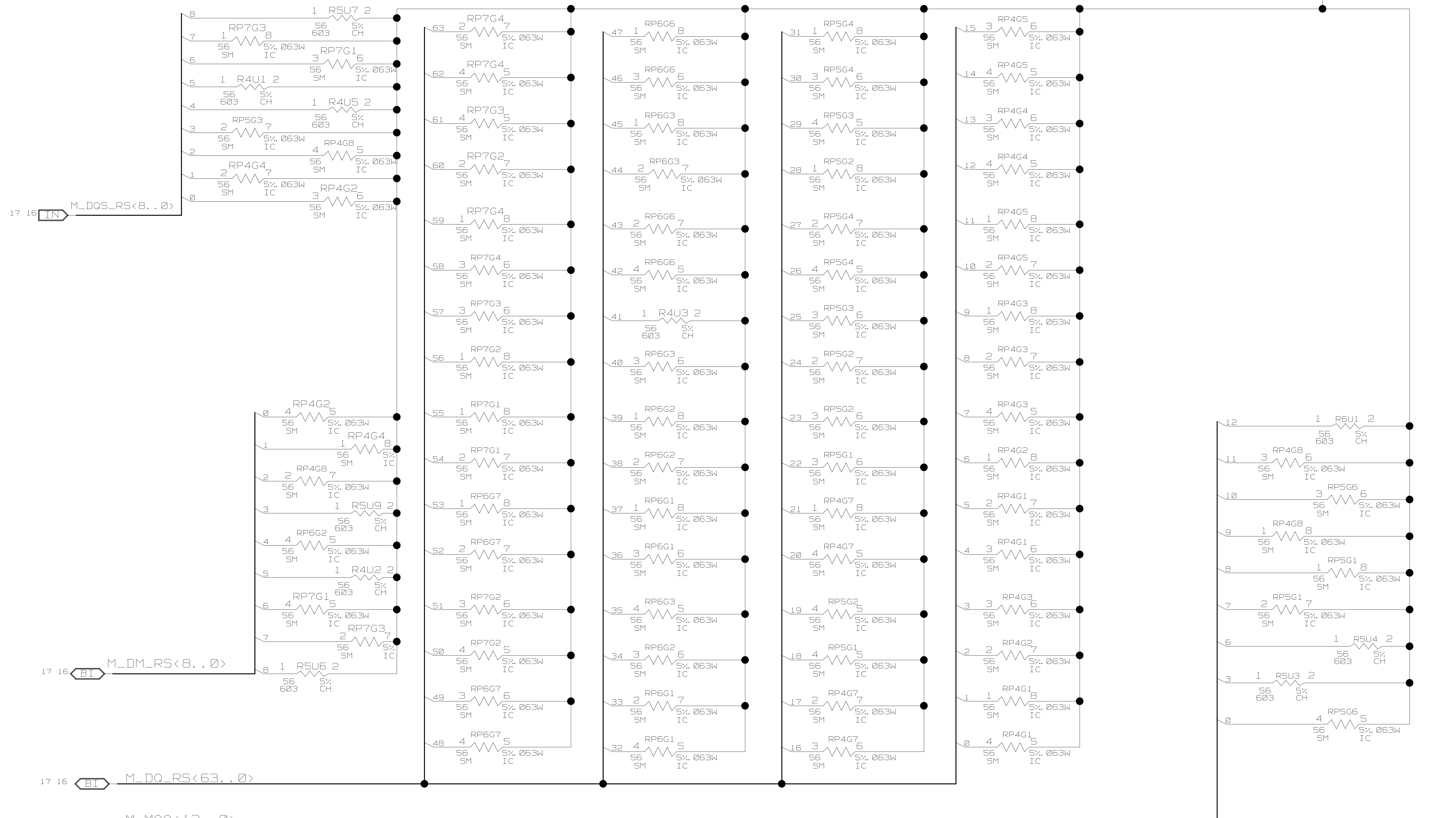

DDR TERMINATION RESISTORS

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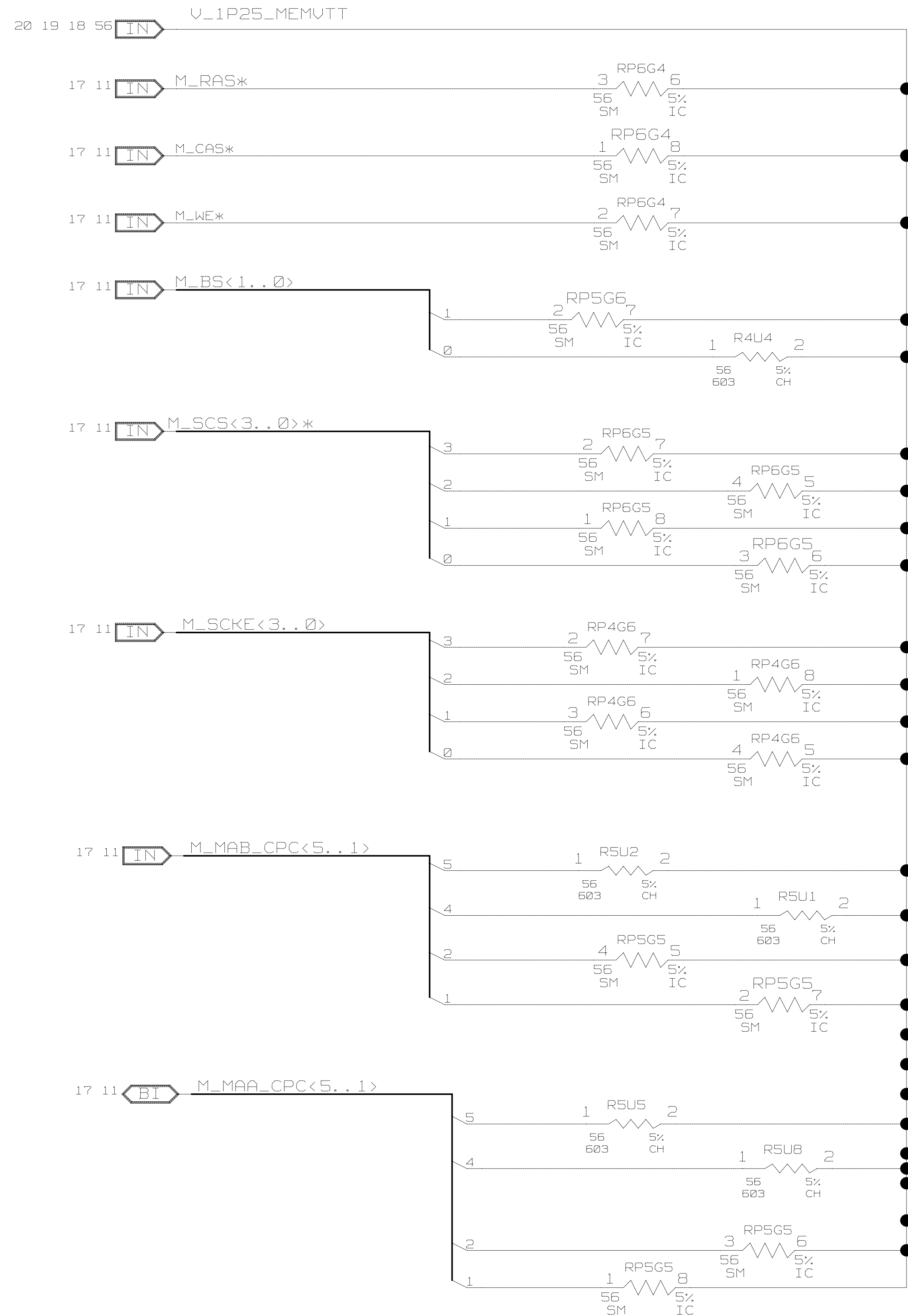
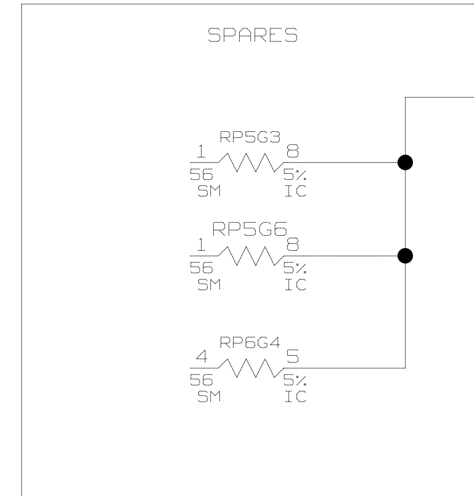
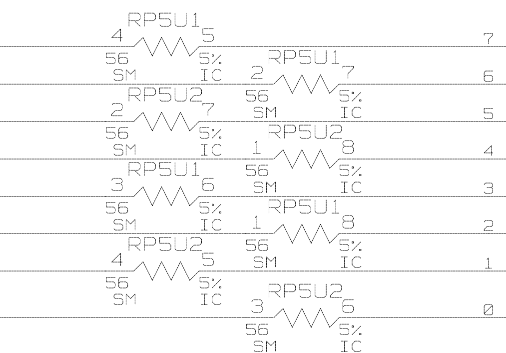
NOTE:

CS SIGNALS MUST HAVE IT'S OWN RES/RPACK
CKE SIGNALS MUST HAVE IT'S OWN RES/RPACK
CPC SIGNALS MUST HAVE IT'S OWN RES/RPACK

ROOM=DCL_DDR_CORE







DDR TERMINATION RESISTORS

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
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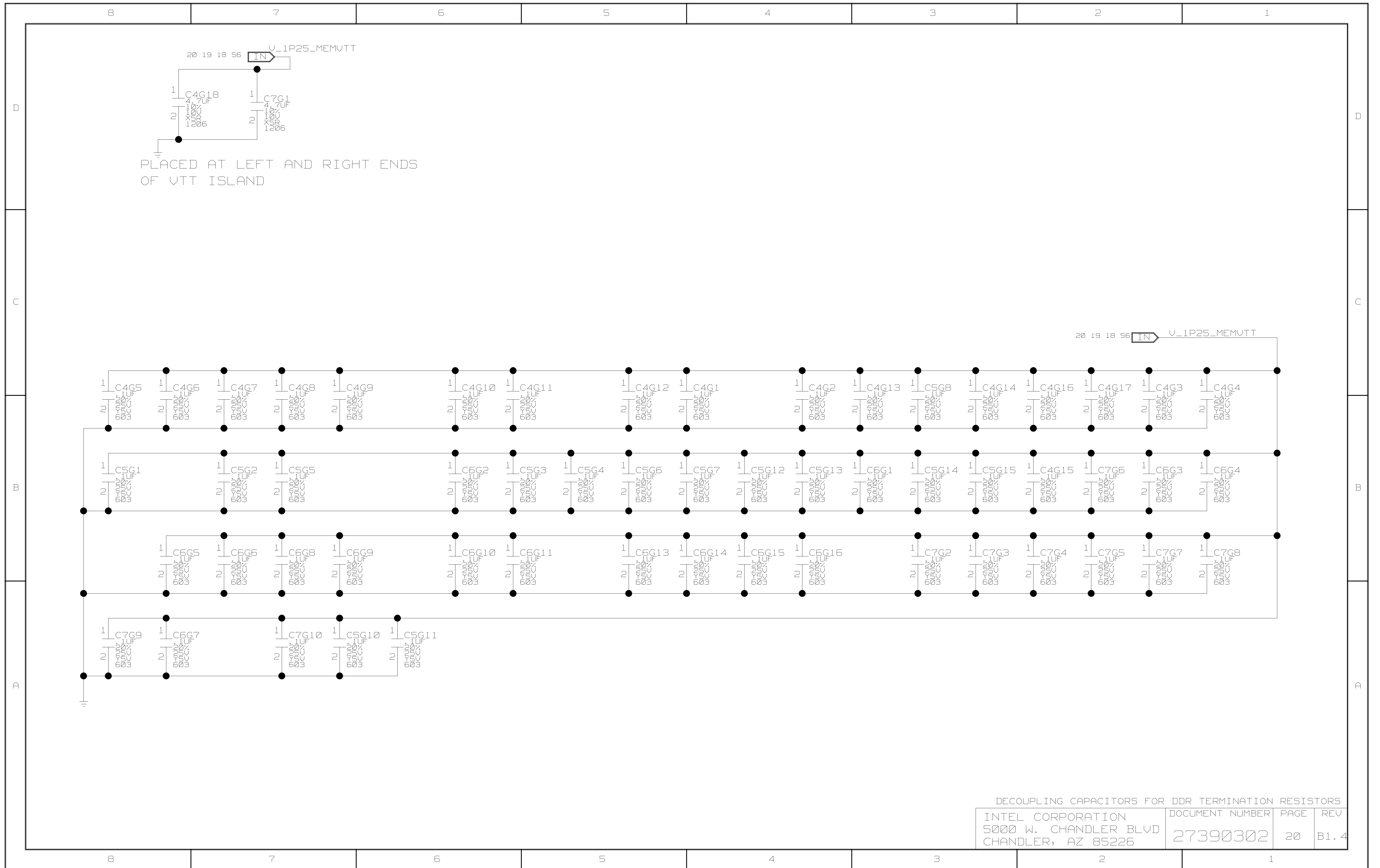

20 19 18 56
IN
V_1P25_MEMVTT
C4G18
4.7UF
10%
10V
X5R
1206
C7G1
4.7UF
10%
10V
X5R
1206
PLACED AT LEFT AND RIGHT ENDS
OF VTT ISLAND
C4G5
C4G6
C4G7
C4G8
C4G9
C4G10
C4G11
C4G12
C4G1
C4G2
C4G13
C5G8
C4G14
C4G16
C4G17
C4G3
C4G4
C5G1
C5G2
C5G5
C6G2
C5G3
C5G4
C5G6
C5G7
C5G12
C5G13
C6G1
C5G14
C5G15
C4G15
C7G6
C6G3
C6G4
C6G5
C6G6
C6G8
C6G9
C6G10
C6G11
C6G13
C6G14
C6G15
C6G16
C7G2
C7G3
C7G4
C7G5
C7G7
C7G8
C7G9
C6G7
C7G10
C5G10
C5G11
.1UF
20%
25V
Y5V
603
DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS
INTEL CORPORATION
5000 W. CHANDLER BLVD
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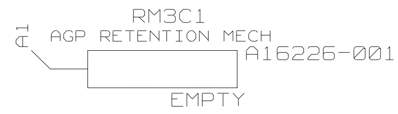
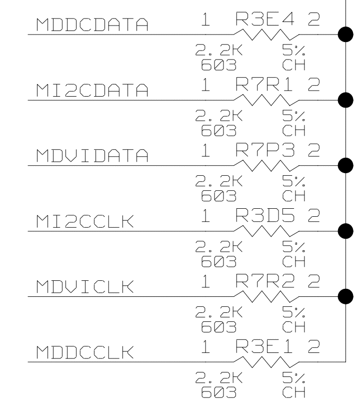
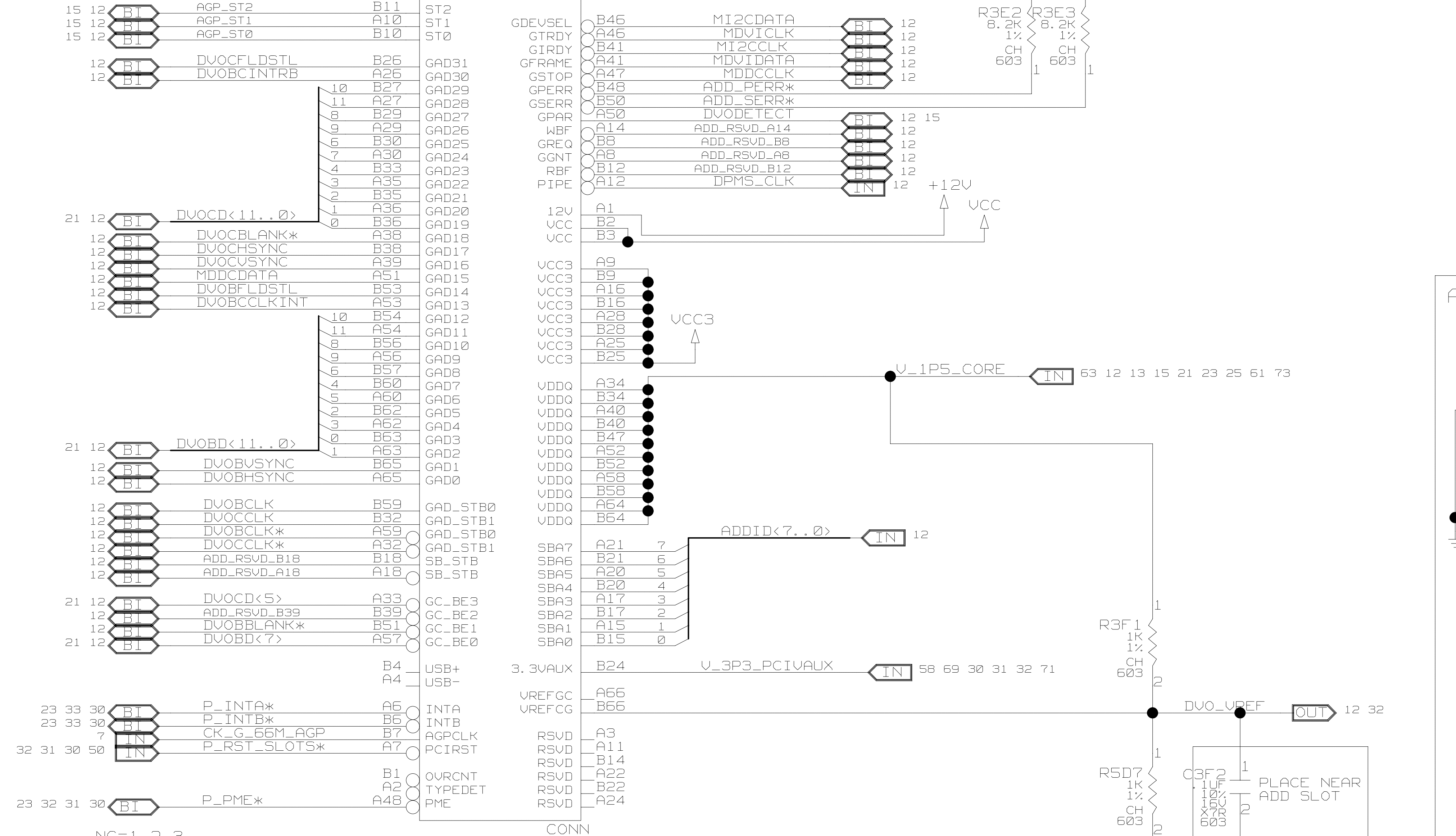
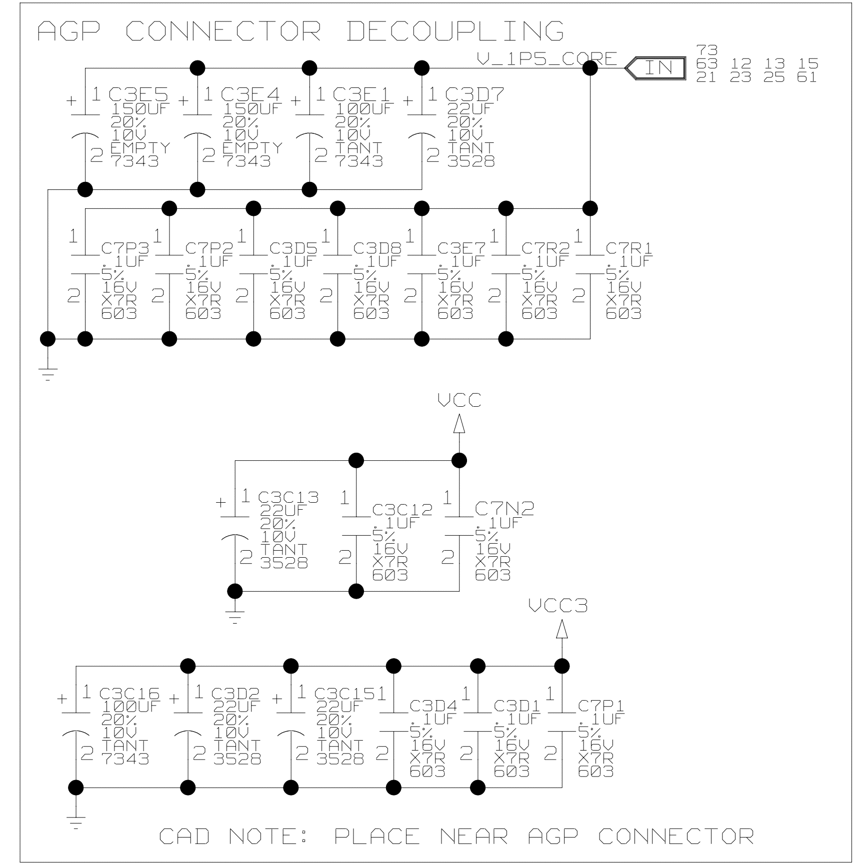
ROOM=DCL_CORE_AGP







NC=1,2,3
GND=A5,B5,A13,B13,A19,B19,A23,B23,A31,B31,A37,B37,A49,B49,A55,B55,A61,B61



AGP DIGITAL DISPLAY

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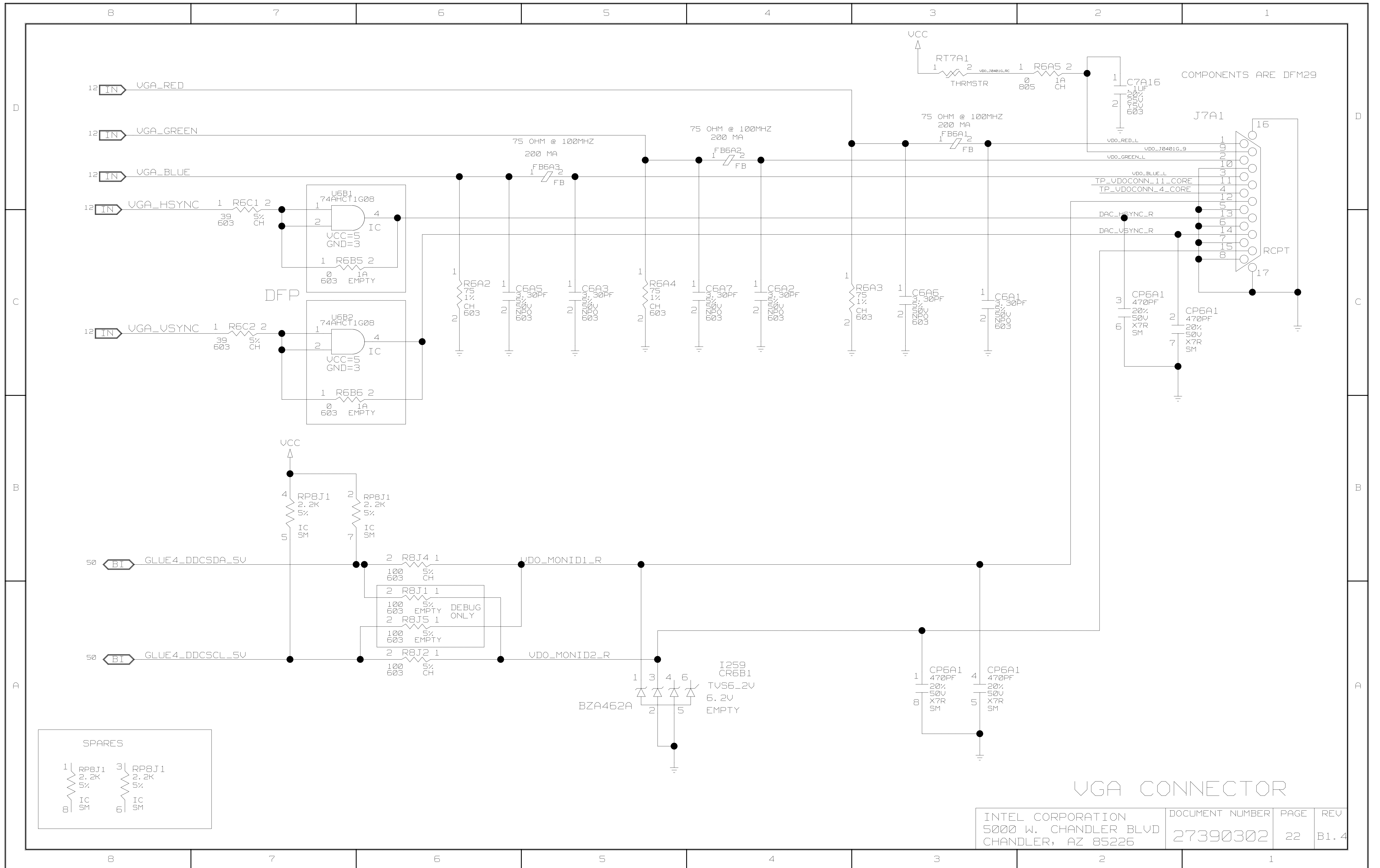

VGA_RED
VGA_GREEN
VGA_BLUE
VGA_HSYNC
VGA_VSYNC
GLUE4_DDCSDA_5V
GLUE4_DDCSCL_5V
VDO_MONID1_R
VDO_MONID2_R
DAC_HSYNC_R
DAC_VSYNC_R
TP_VDOCONN_11_CORE
TP_VDOCONN_4_CORE
75 OHM @ 100MHZ
200 MA
COMPONENTS ARE DFM29
J7A1
RCPT
THRMSTR
DFP
DEBUG ONLY
SPARES
VCC
U6B1
U6B2
74AHCT1G08
VCC=5
GND=3
BZA462A
CR6B1
TVS6_2V
6.2V
EMPTY
VGA CONNECTOR
INTEL CORPORATION
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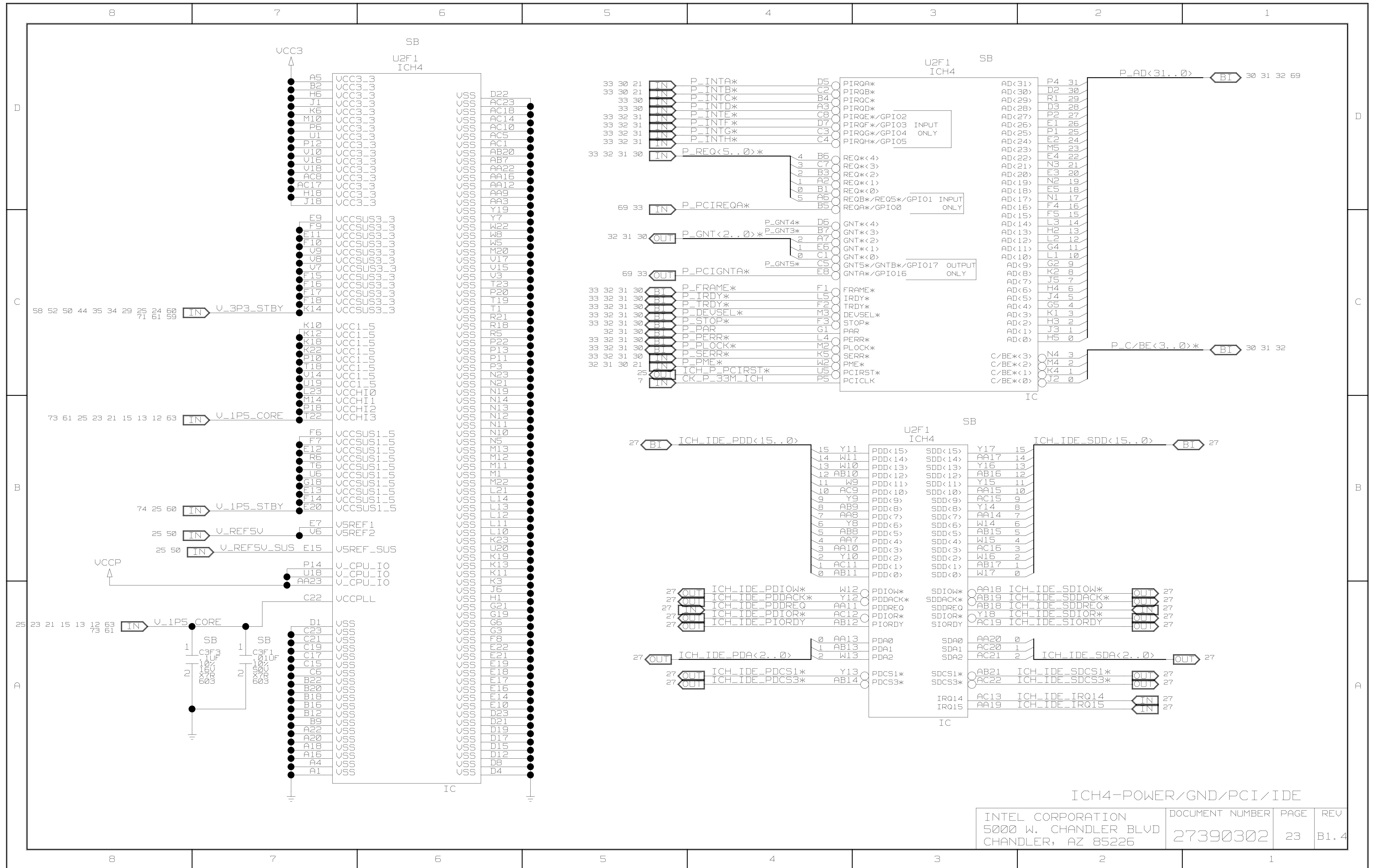
SB
U2F1
ICH4
VCC3
V_3P3_STBY
V_1P5_CORE
V_1P5_STBY
V_REF5V
V_REF5V_SUS
VCCP
C3F3
.1UF
10%
16V
X7R
603
C3F1
.01UF
10%
50V
X7R
603
P_AD<31..0>
P_C/BE<3..0>*
P_REQ<5..0>*
P_PCIREQA*
P_GNT<2..0>*
P_PCIGNTA*
P_FRAME*
P_IRDY*
P_TRDY*
P_DEVSEL*
P_STOP*
P_PAR
P_PERR*
P_PLOCK*
P_SERR*
P_PME*
ICH_P_PCIRST*
CK_P_33M_ICH
ICH_IDE_PDD<15..0>
ICH_IDE_SDD<15..0>
ICH_IDE_PDIOW*
ICH_IDE_PDDACK*
ICH_IDE_PDDREQ
ICH_IDE_PDIOR*
ICH_IDE_PIORDY
ICH_IDE_SDIOW*
ICH_IDE_SDDACK*
ICH_IDE_SDDREQ
ICH_IDE_SDIOR*
ICH_IDE_SIORDY
ICH_IDE_PDA<2..0>
ICH_IDE_SDA<2..0>
ICH_IDE_PDCS1*
ICH_IDE_PDCS3*
ICH_IDE_SDCS1*
ICH_IDE_SDCS3*
ICH_IDE_IRQ14
ICH_IDE_IRQ15
ICH4-POWER/GND/PCI/IDE
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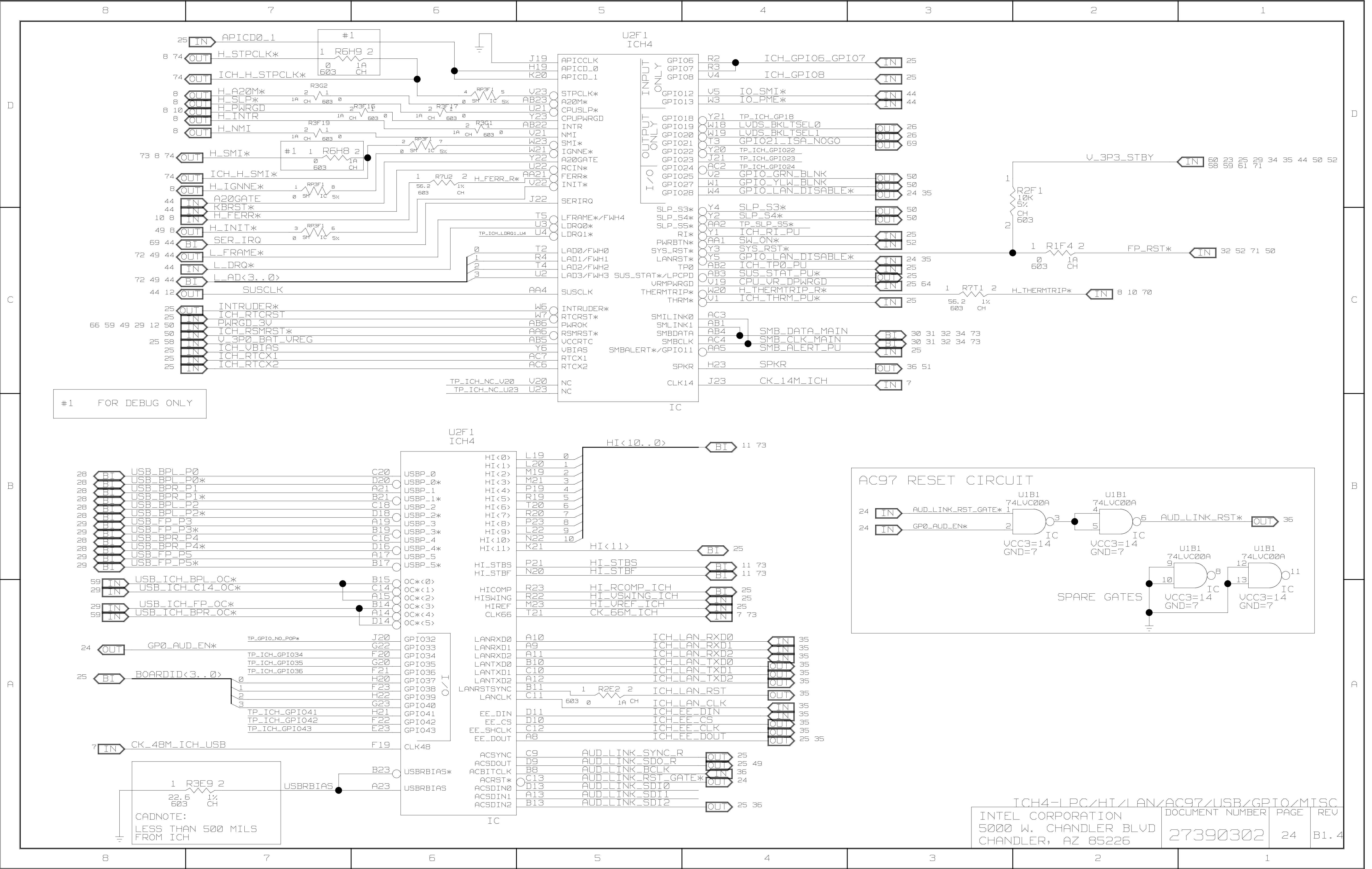

U2F1
ICH4
APICD0_1
H_STPCLK*
ICH_H_STPCLK*
H_A20M*
H_SLP*
H_PWRGD
H_INTR
H_NMI
H_SMI*
ICH_H_SMI*
H_IGNNE*
A20GATE
KBRST*
H_FERR*
H_INIT*
SER_IRQ
L_FRAME*
L_DRQ*
L_AD<3..0>
SUSCLK
INTRUDER*
ICH_RTCRST
PWRGD_3V
ICH_RSMRST*
V_3P0_BAT_VREG
ICH_VBIAS
ICH_RTCX1
ICH_RTCX2
TP_ICH_NC_V20
TP_ICH_NC_U23
#1 FOR DEBUG ONLY
APICCLK
APICD_0
APICD_1
STPCLK*
A20M*
CPUSLP*
CPUPWRGD
INTR
NMI
SMI*
IGNNE*
A20GATE
RCIN*
FERR*
INIT*
SERIRQ
LFRAME*/FWH4
LDRQ0*
LDRQ1*
LAD0/FWH0
LAD1/FWH1
LAD2/FWH2
LAD3/FWH3
SUSCLK
INTRUDER*
RTCRST*
PWROK
RSMRST*
VCCRTC
VBIAS
RTCX1
RTCX2
NC
INPUT ONLY
OUTPUT ONLY
I/O
GPIO6
GPIO7
GPIO8
GPIO12
GPIO13
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO25
GPIO27
GPIO28
SLP_S3*
SLP_S4*
SLP_S5*
RI*
PWRBTN*
SYS_RST*
LANRST*
TP0
SUS_STAT*/LPCPD
VRMPWRGD
THERMTRIP*
THRM*
SMLINK0
SMLINK1
SMBDATA
SMBCLK
SMBALERT*/GPIO11
SPKR
CLK14
ICH_GPIO6_GPIO7
ICH_GPIO8
IO_SMI*
IO_PME*
TP_ICH_GP18
LVDS_BKLTSEL0
LVDS_BKLTSEL1
GPIO21_ISA_NOGO
TP_ICH_GPIO22
TP_ICH_GPIO23
TP_ICH_GPIO24
GPIO_GRN_BLNK
GPIO_YLW_BLNK
GPIO_LAN_DISABLE*
SLP_S3*
SLP_S4*
TP_SLP_S5*
ICH_RI_PU
SW_ON*
SYS_RST*
GPIO_LAN_DISABLE*
ICH_TP0_PU
SUS_STAT_PU*
CPU_VR_DPWRGD
H_THERMTRIP_R*
ICH_THRM_PU*
SMB_DATA_MAIN
SMB_CLK_MAIN
SMB_ALERT_PU
SPKR
CK_14M_ICH
V_3P3_STBY
R2F1
10K
5%
CH
603
R1F4
FP_RST*
R7T1
56.2
H_THERMTRIP*
HI<10..0>
HI<11>
HI_STBS
HI_STBF
HI_RCOMP_ICH
HI_VSWING_ICH
HI_VREF_ICH
CK_66M_ICH
USB_BPL_P0
USB_BPL_P0*
USB_BPR_P1
USB_BPR_P1*
USB_BPL_P2
USB_BPL_P2*
USB_FP_P3
USB_FP_P3*
USB_BPR_P4
USB_BPR_P4*
USB_FP_P5
USB_FP_P5*
USB_ICH_BPL_OC*
USB_ICH_C14_OC*
USB_ICH_FP_OC*
USB_ICH_BPR_OC*
GP0_AUD_EN*
TP_GPIO_NO_POP*
TP_ICH_GPIO34
TP_ICH_GPIO35
TP_ICH_GPIO36
BOARDID<3..0>
TP_ICH_GPIO41
TP_ICH_GPIO42
TP_ICH_GPIO43
CK_48M_ICH_USB
USBRBIAS
R3E9
22.6
CADNOTE:
LESS THAN 500 MILS FROM ICH
USBP_0
USBP_0*
USBP_1
USBP_1*
USBP_2
USBP_2*
USBP_3
USBP_3*
USBP_4
USBP_4*
USBP_5
USBP_5*
OC*<0>
OC*<1>
OC*<2>
OC*<3>
OC*<4>
OC*<5>
GPIO32
GPIO33
GPIO34
GPIO35
GPIO36
GPIO37
GPIO38
GPIO39
GPIO40
GPIO41
GPIO42
GPIO43
CLK48
USBRBIAS*
USBRBIAS
HI_STBS
HI_STBF
HICOMP
HISWING
HIREF
CLK66
LANRXD0
LANRXD1
LANRXD2
LANTXD0
LANTXD1
LANTXD2
LANRSTSYNC
LANCLK
EE_DIN
EE_CS
EE_SHCLK
EE_DOUT
ACSYNC
ACSDOUT
ACBITCLK
ACRST*
ACSDIN0
ACSDIN1
ACSDIN2
ICH_LAN_RXD0
ICH_LAN_RXD1
ICH_LAN_RXD2
ICH_LAN_TXD0
ICH_LAN_TXD1
ICH_LAN_TXD2
R2E2
ICH_LAN_RST
ICH_LAN_CLK
ICH_EE_DIN
ICH_EE_CS
ICH_EE_CLK
ICH_EE_DOUT
AUD_LINK_SYNC_R
AUD_LINK_SDO_R
AUD_LINK_BCLK
AUD_LINK_RST_GATE*
AUD_LINK_SDI0
AUD_LINK_SDI1
AUD_LINK_SDI2
AC97 RESET CIRCUIT
U1B1
74LVC00A
AUD_LINK_RST_GATE*
GP0_AUD_EN*
AUD_LINK_RST*
VCC3=14
GND=7
SPARE GATES
ICH4-LPC/HI/LAN/AC97/USB/GPIO/MISC
INTEL CORPORATION
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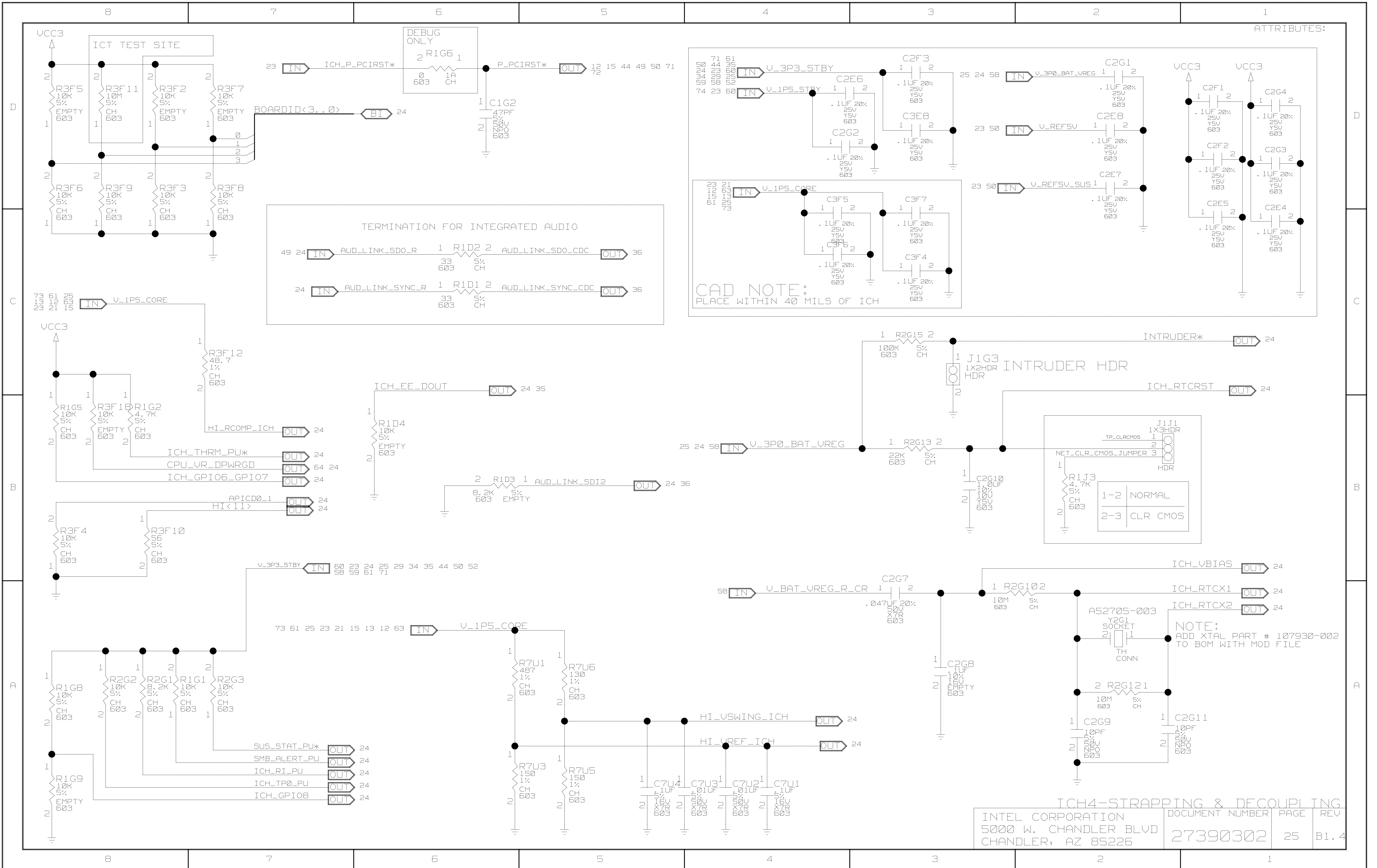
ICT TEST SITE
DEBUG ONLY
TERMINATION FOR INTEGRATED AUDIO
CAD NOTE:
PLACE WITHIN 40 MILS OF ICH
INTRUDER HDR
1-2 NORMAL
2-3 CLR CMOS
NOTE:
ADD XTAL PART # 107930-002
TO BOM WITH MOD FILE
ICH4-STRAPPING & DECOUPLING
INTEL CORPORATION
5000 W. CHANDLER BLVD
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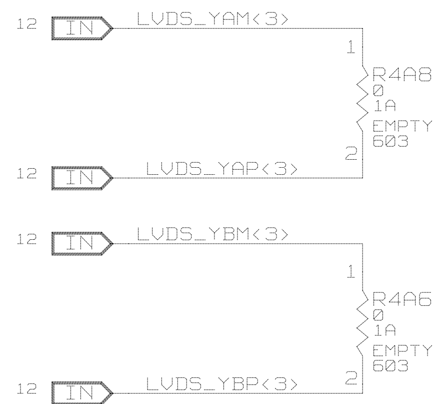
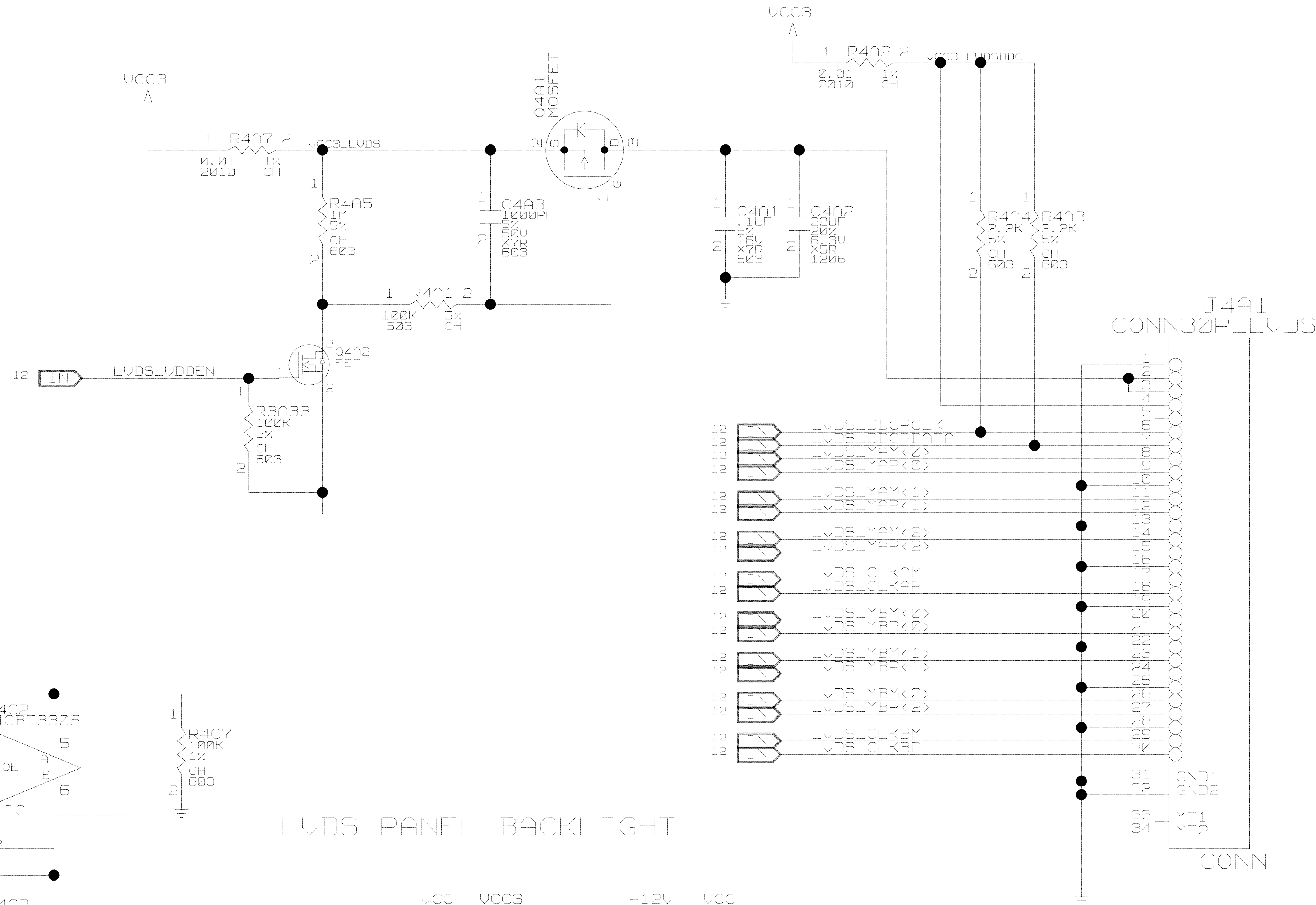
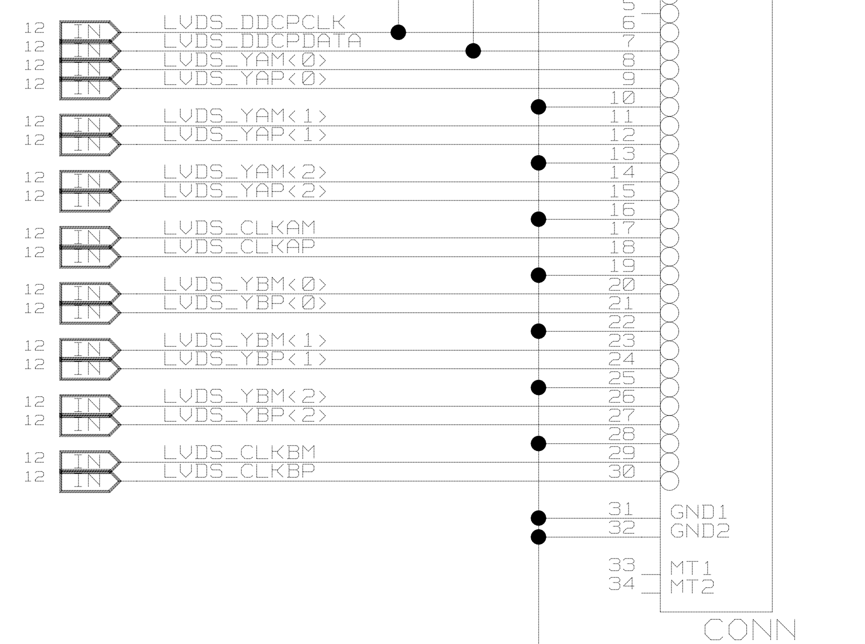
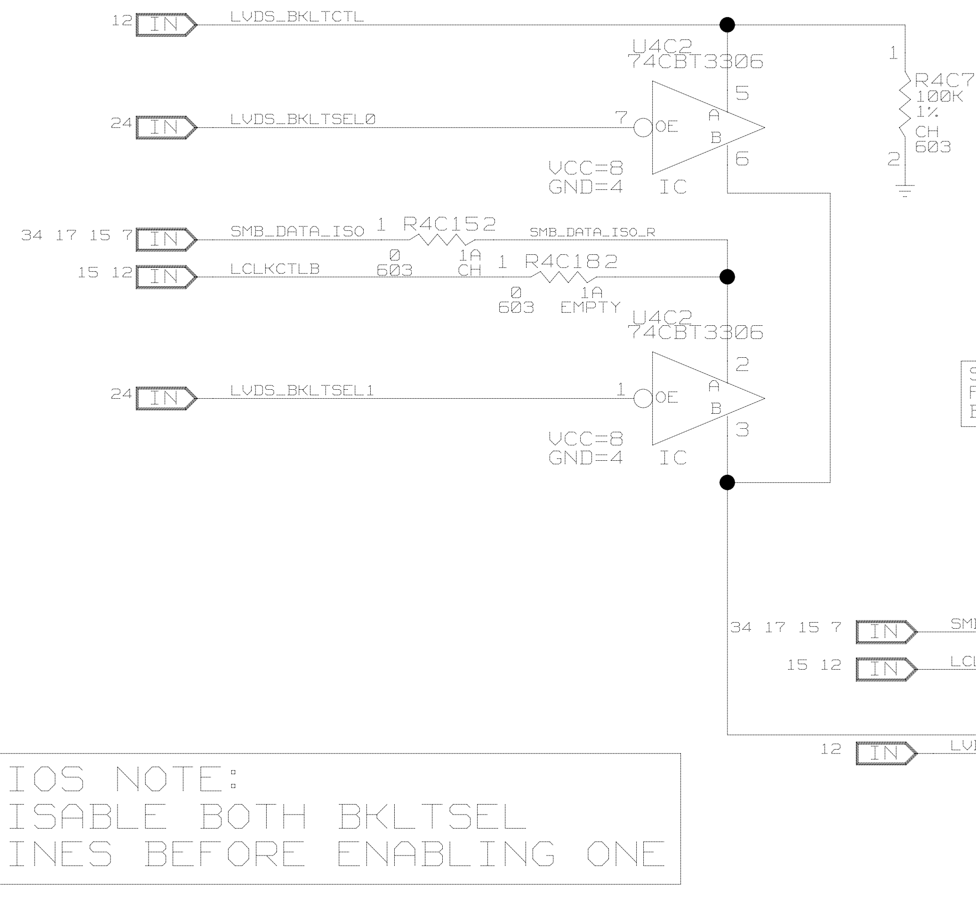
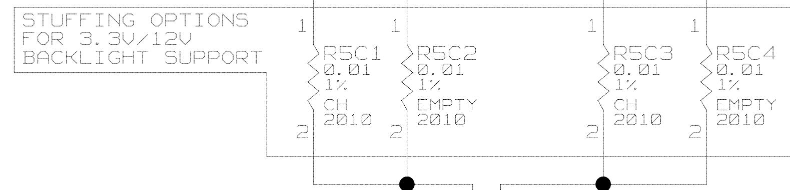


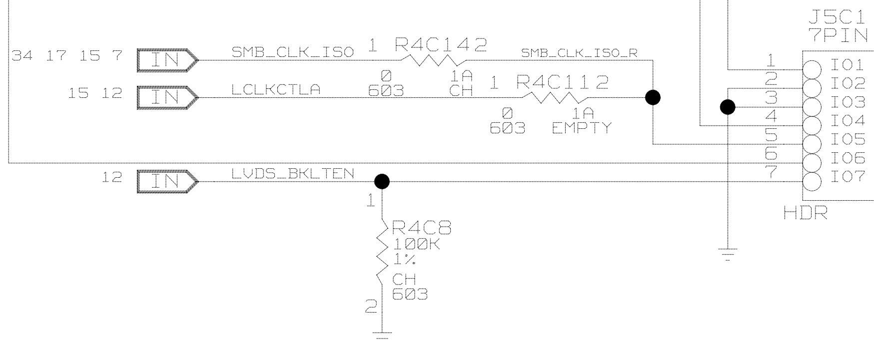




LVDS PANEL BACKLIGHT







BIOS NOTE:
DISABLE BOTH BKLTSEL
LINES BEFORE ENABLING ONE

LVDS CONNECTOR

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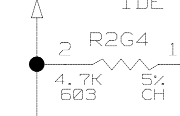
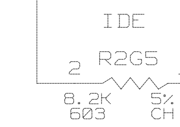
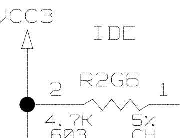
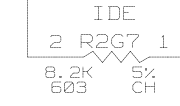
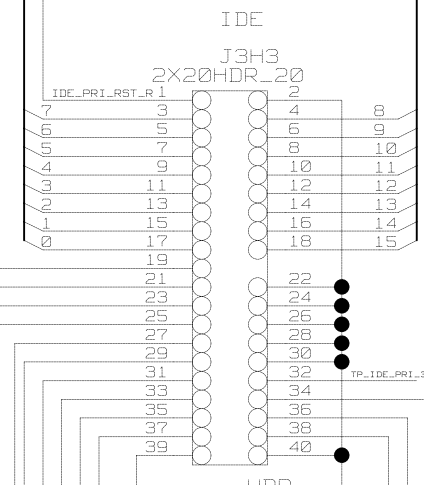
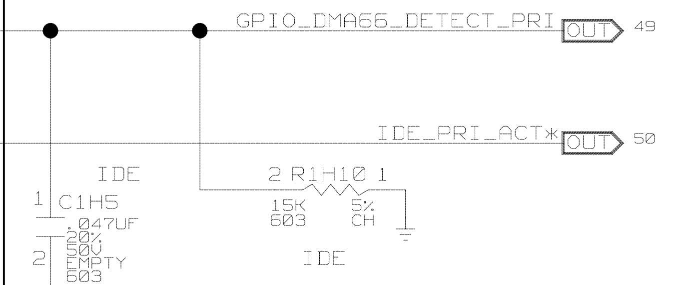
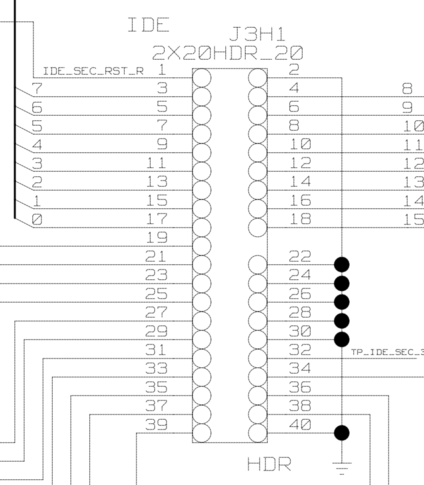
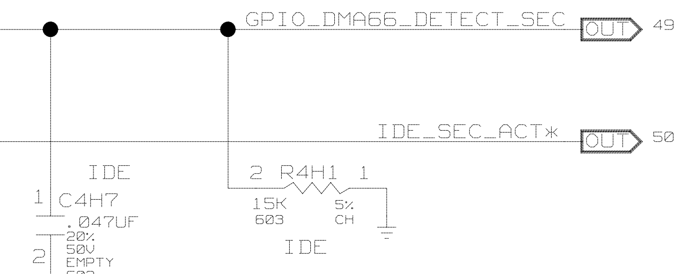
IDE CONNECTORS

DESIGN NOTE:
SERIES RESISTORS INTEGRATED INTO ICH:
VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS







DESIGN NOTE:
DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR*, XIORDY*) WITHIN +/-250MIL
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/-10MIL

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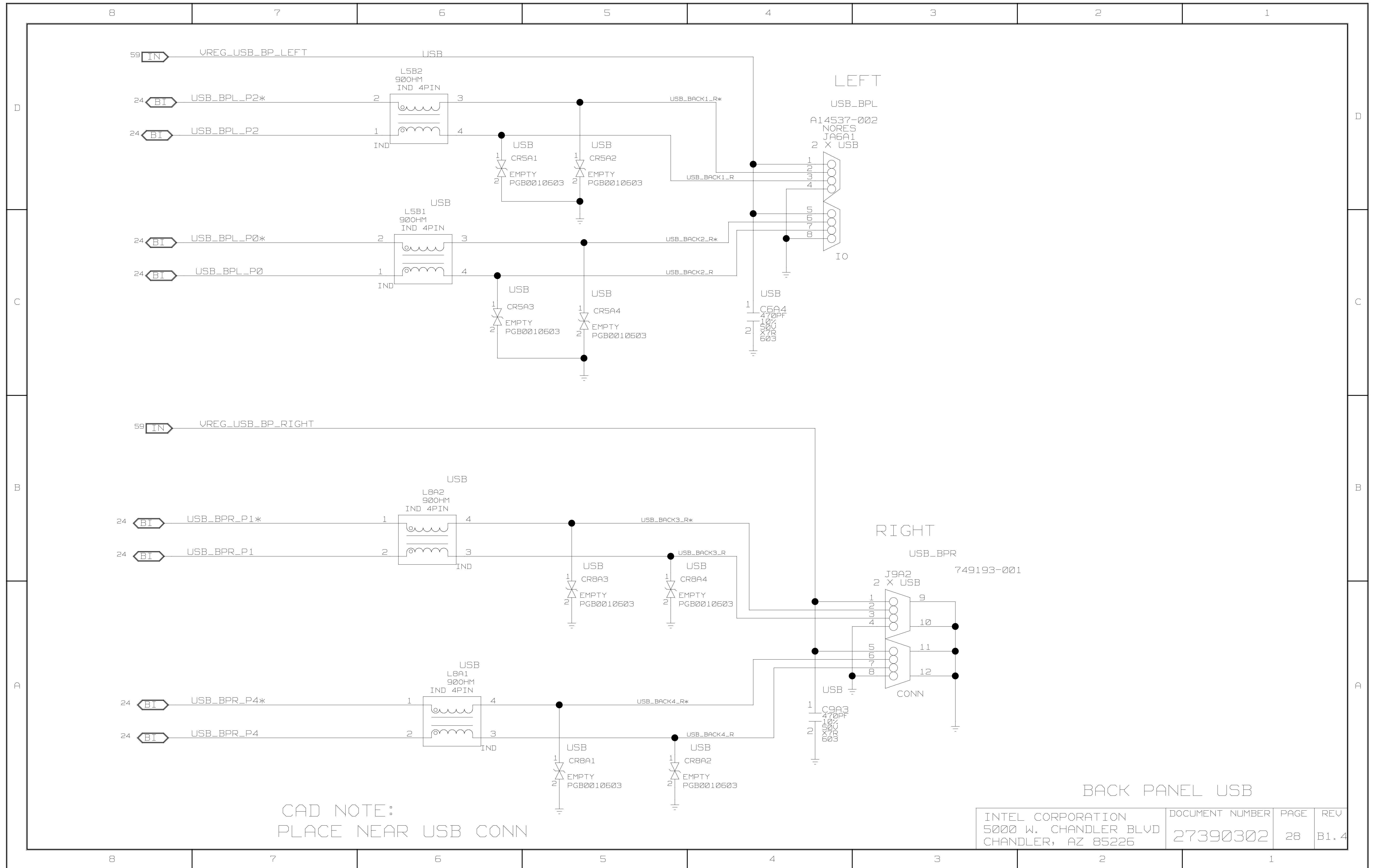

VREG_USB_BP_LEFT
USB_BPL_P2*
USB_BPL_P2
USB_BPL_P0*
USB_BPL_P0
L5B2
900HM
IND 4PIN
L5B1
CR5A1
CR5A2
CR5A3
CR5A4
EMPTY
PGB0010603
USB_BACK1_R*
USB_BACK1_R
USB_BACK2_R*
USB_BACK2_R
LEFT
USB_BPL
A14537-002
NORES
JA6A1
2 X USB
IO
C6A4
470PF
10%
50V
X7R
603
VREG_USB_BP_RIGHT
USB_BPR_P1*
USB_BPR_P1
USB_BPR_P4*
USB_BPR_P4
L8A2
L8A1
CR8A1
CR8A2
CR8A3
CR8A4
USB_BACK3_R*
USB_BACK3_R
USB_BACK4_R*
USB_BACK4_R
RIGHT
USB_BPR
749193-001
J9A2
CONN
C9A3
CAD NOTE:
PLACE NEAR USB CONN
BACK PANEL USB
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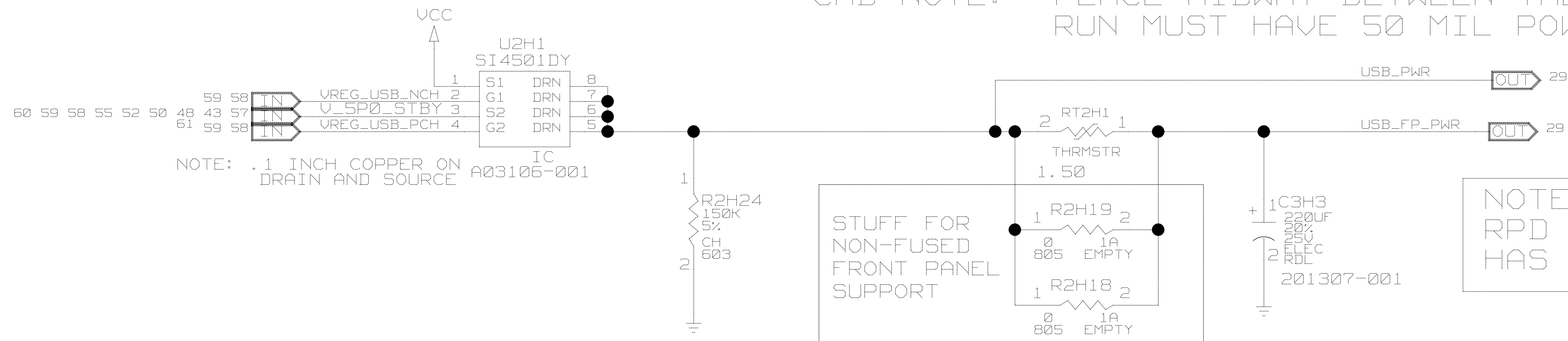
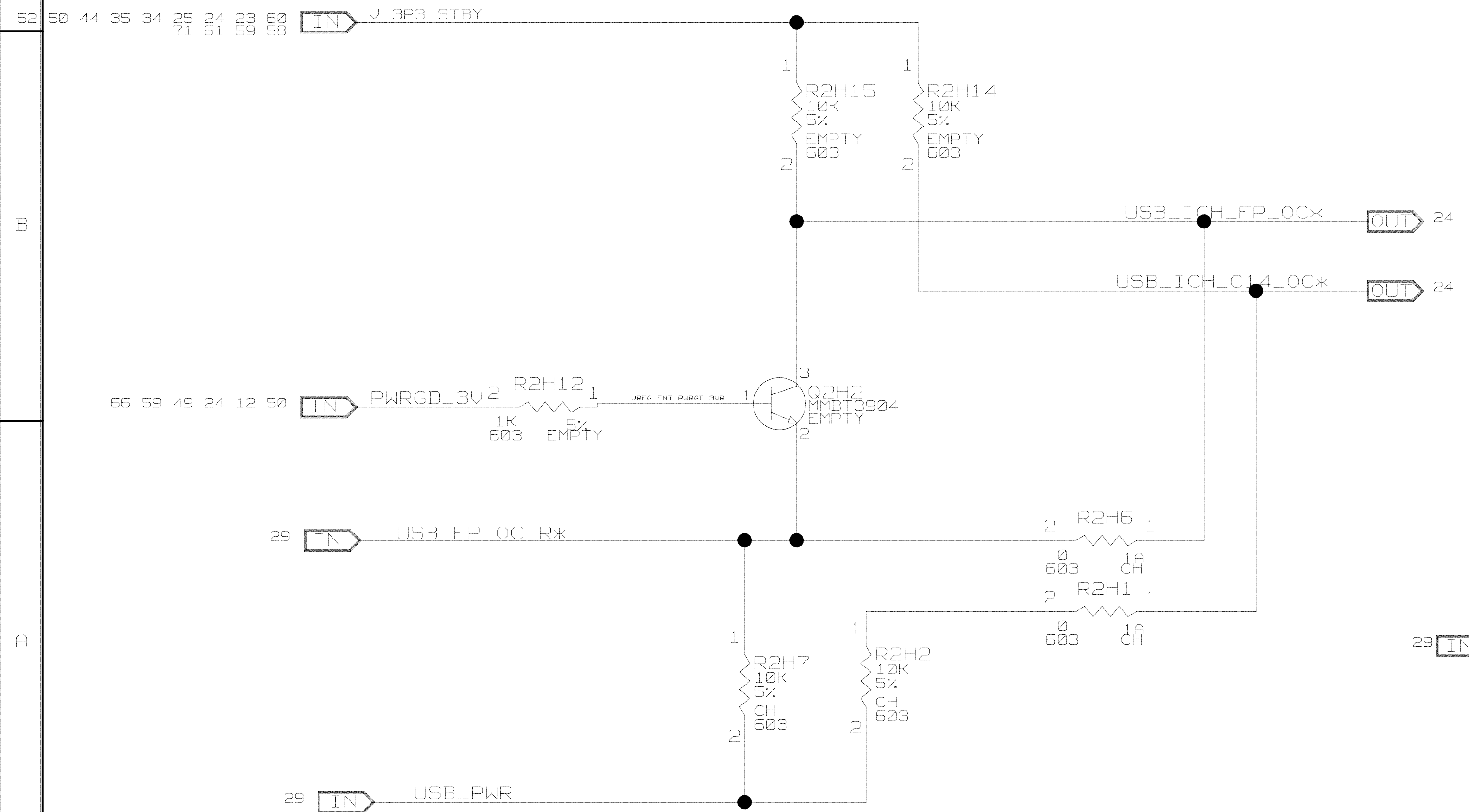
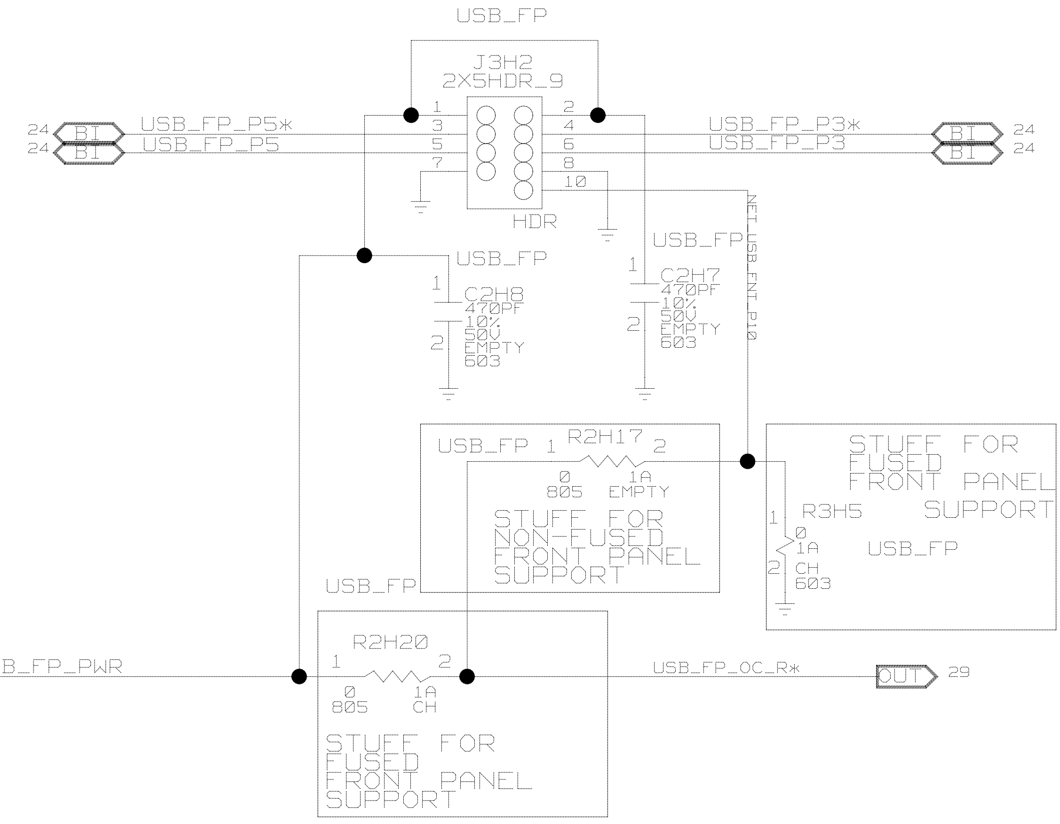
CAD NOTE;
TRACE ROUTING IS 7.5 MIL, 7.5 MIL SPACING



CAD NOTE:
LEAVE ROOM FOR 2 CHOKES,
1 THERMISTER AND 1 TH CAP.





USB FNT PANEL/POWER

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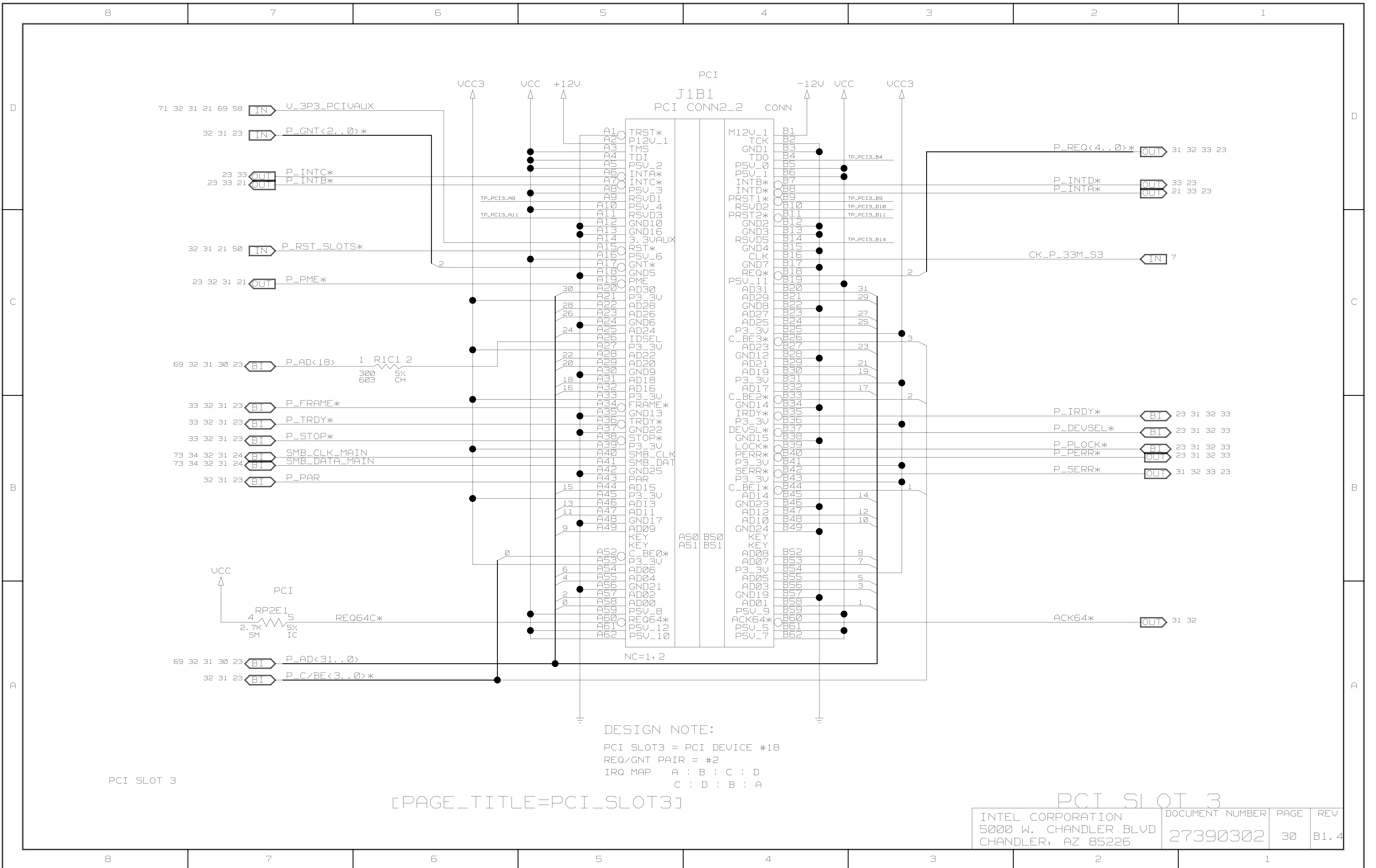

PCI
J1B1
PCI CONN2_2 CONN
VCC3
VCC
+12V
-12V
V_3P3_PCIVAUX
P_GNT<2..0>*
P_INTC*
P_INTB*
P_RST_SLOTS*
P_PME*
P_AD<18>
R1C1
300
603
5%
CH
P_FRAME*
P_TRDY*
P_STOP*
SMB_CLK_MAIN
SMB_DATA_MAIN
P_PAR
P_REQ<4..0>*
P_INTD*
P_INTA*
CK_P_33M_S3
P_IRDY*
P_DEVSEL*
P_PLOCK*
P_PERR*
P_SERR*
ACK64*
REQ64C*
RP2E1
2.7K
SM
IC
P_AD<31..0>
P_C/BE<3..0>*
NC=1,2
DESIGN NOTE:
PCI SLOT3 = PCI DEVICE #18
REQ/GNT PAIR = #2
IRQ MAP A : B : C : D
C : D : B : A
PCI SLOT 3
[PAGE_TITLE=PCI_SLOT3]
PCI SLOT 3
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5000 W. CHANDLER BLVD
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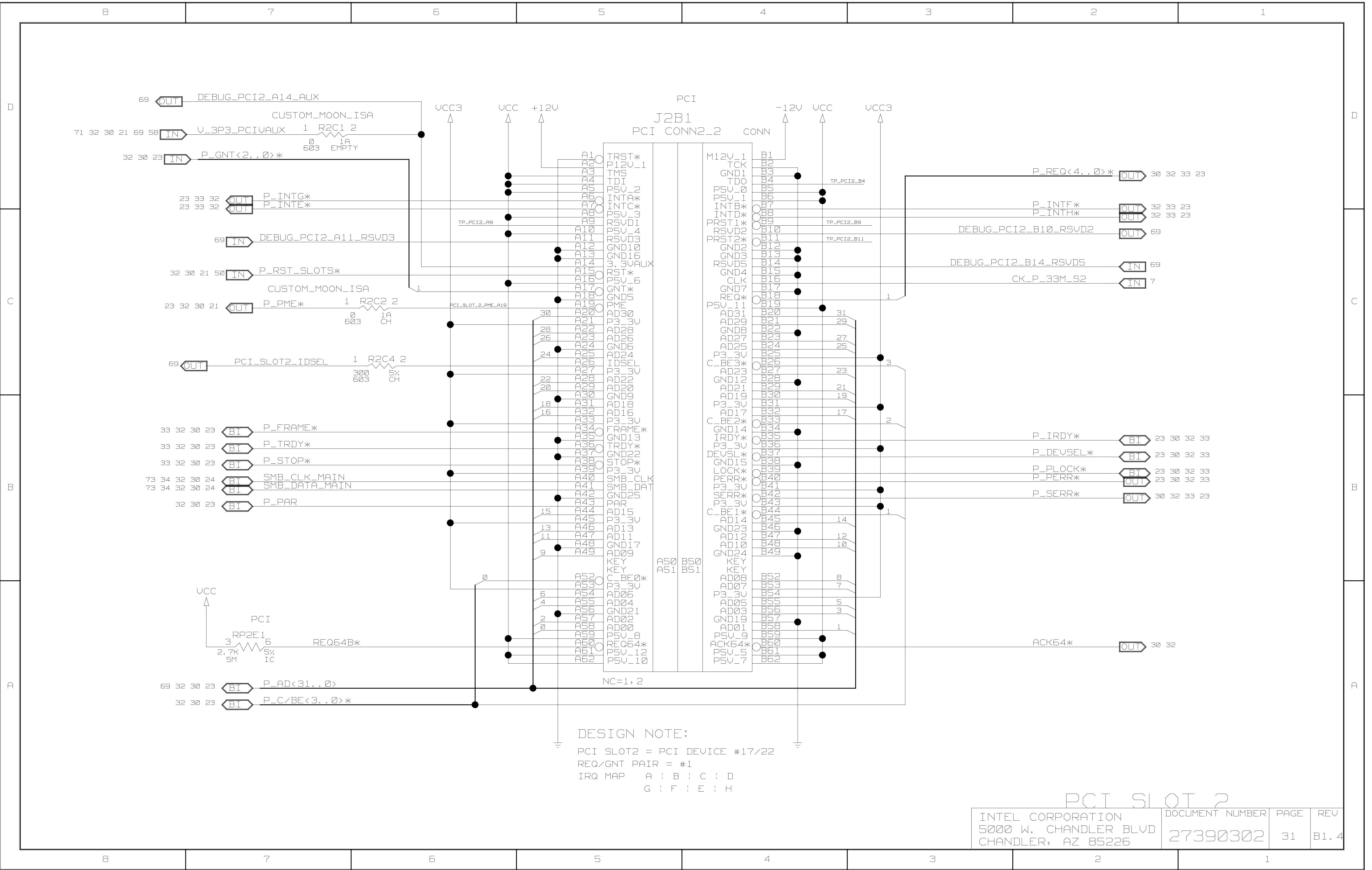

PCI
J2B1
PCI CONN2_2
CONN
VCC3
VCC
+12V
-12V
DEBUG_PCI2_A14_AUX
CUSTOM_MOON_ISA
V_3P3_PCIVAUX
R2C1
0
603
1A
EMPTY
P_GNT<2..0>*
P_INTG*
P_INTE*
DEBUG_PCI2_A11_RSVD3
P_RST_SLOTS*
P_PME*
R2C2
1A
CH
PCI_SLOT2_IDSEL
R2C4
300
603
5%
P_FRAME*
P_TRDY*
P_STOP*
SMB_CLK_MAIN
SMB_DATA_MAIN
P_PAR
RP2E1
2.7K
SM
5%
IC
REQ64B*
P_AD<31..0>
P_C/BE<3..0>*
TP_PCI2_A9
PCI_SLOT_2_PME_A19
TP_PCI2_B4
TP_PCI2_B9
TP_PCI2_B11
P_REQ<4..0>*
P_INTF*
P_INTH*
DEBUG_PCI2_B10_RSVD2
DEBUG_PCI2_B14_RSVD5
CK_P_33M_S2
P_IRDY*
P_DEVSEL*
P_PLOCK*
P_PERR*
P_SERR*
ACK64*
TRST*
P12V_1
TMS
TDI
P5V_2
INTA*
INTC*
P5V_3
RSVD1
P5V_4
RSVD3
GND10
GND16
3.3VAUX
RST*
P5V_6
GNT*
GND5
PME
AD30
P3_3V
AD28
AD26
GND6
AD24
IDSEL
AD22
AD20
GND9
AD18
AD16
FRAME*
GND13
TRDY*
GND22
STOP*
SMB_CLK
SMB_DAT
GND25
PAR
AD15
AD13
AD11
GND17
AD09
KEY
C_BE0*
AD06
AD04
GND21
AD02
AD00
P5V_8
REQ64*
P5V_12
P5V_10
M12V_1
TCK
GND1
TDO
P5V_0
P5V_1
INTB*
INTD*
PRST1*
RSVD2
PRST2*
GND2
GND3
RSVD5
GND4
CLK
GND7
REQ*
P5V_11
AD31
AD29
GND8
AD27
AD25
C_BE3*
AD23
GND12
AD21
AD19
AD17
C_BE2*
GND14
IRDY*
DEVSL*
GND15
LOCK*
PERR*
SERR*
C_BE1*
AD14
GND23
AD12
AD10
GND24
AD08
AD07
AD05
AD03
GND19
AD01
P5V_9
ACK64*
P5V_5
P5V_7
NC=1,2
DESIGN NOTE:
PCI SLOT2 = PCI DEVICE #17/22
REQ/GNT PAIR = #1
IRQ MAP A : B : C : D
G : F : E : H
PCI SLOT 2
INTEL CORPORATION
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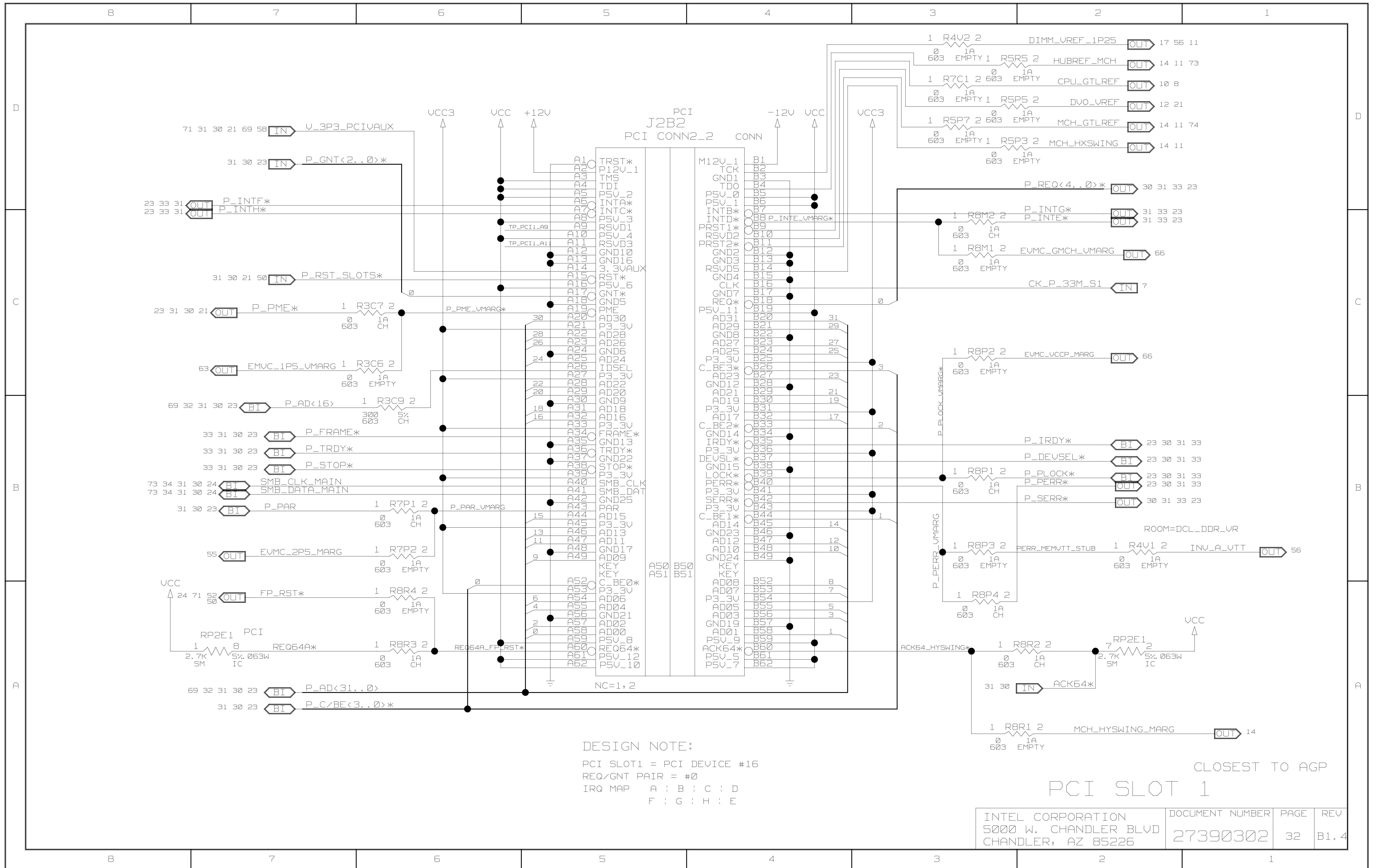
PCI
J2B2
PCI CONN2_2
CONN
VCC3
VCC
+12V
-12V
V_3P3_PCIVAUX
P_GNT<2..0>*
P_INTF*
P_INTH*
P_RST_SLOTS*
P_PME*
EMVC_1P5_VMARG
P_AD<16>
P_FRAME*
P_TRDY*
P_STOP*
SMB_CLK_MAIN
SMB_DATA_MAIN
P_PAR
EVMC_2P5_MARG
FP_RST*
REQ64A*
P_AD<31..0>
P_C/BE<3..0>*
DIMM_VREF_1P25
HUBREF_MCH
CPU_GTLREF
DVO_VREF
MCH_GTLREF
MCH_HXSWING
P_REQ<4..0>*
P_INTG*
P_INTE*
EVMC_GMCH_VMARG
CK_P_33M_S1
EVMC_VCCP_MARG
P_IRDY*
P_DEVSEL*
P_PLOCK*
P_PERR*
P_SERR*
ROOM=DCL_DDR_VR
INV_A_VTT
ACK64*
MCH_HYSWING_MARG
DESIGN NOTE:
PCI SLOT1 = PCI DEVICE #16
REQ/GNT PAIR = #0
IRQ MAP A : B : C : D
F : G : H : E
CLOSEST TO AGP
PCI SLOT 1
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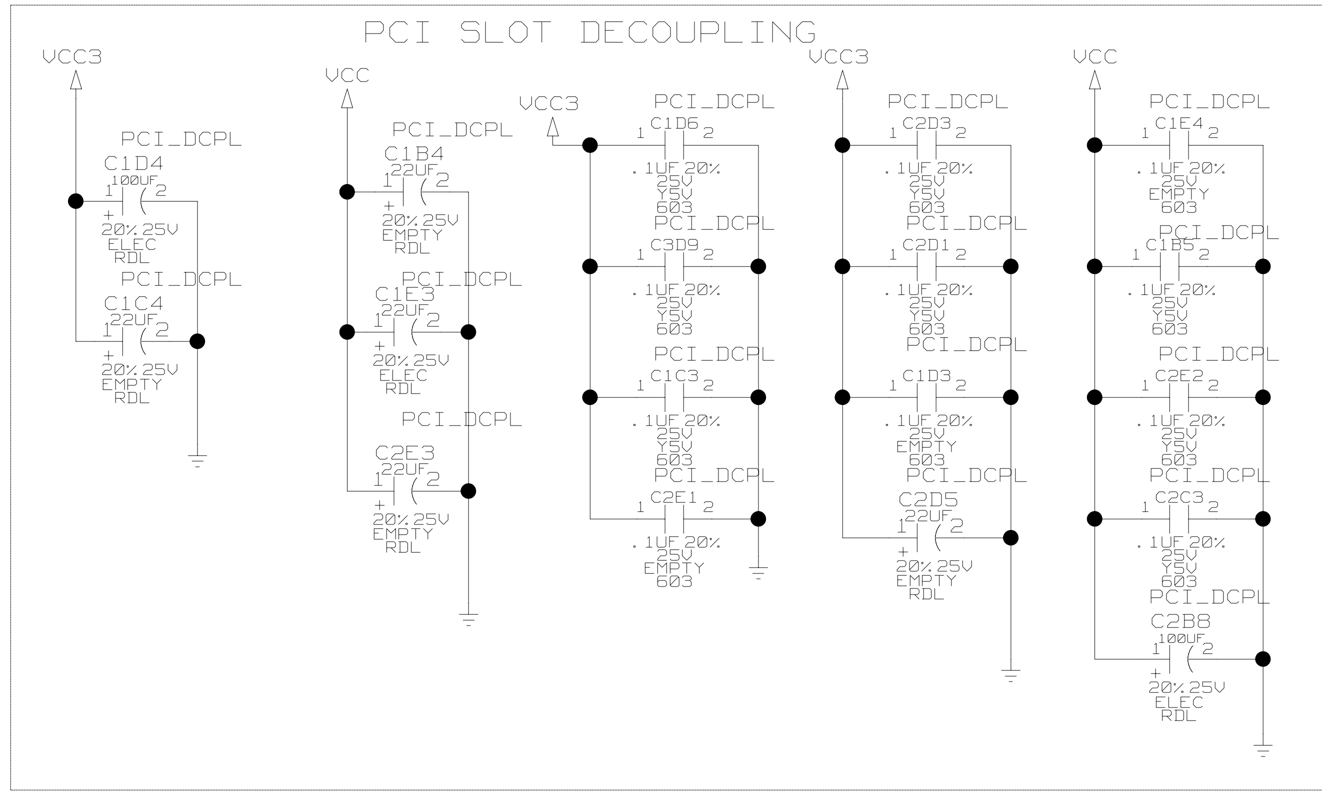

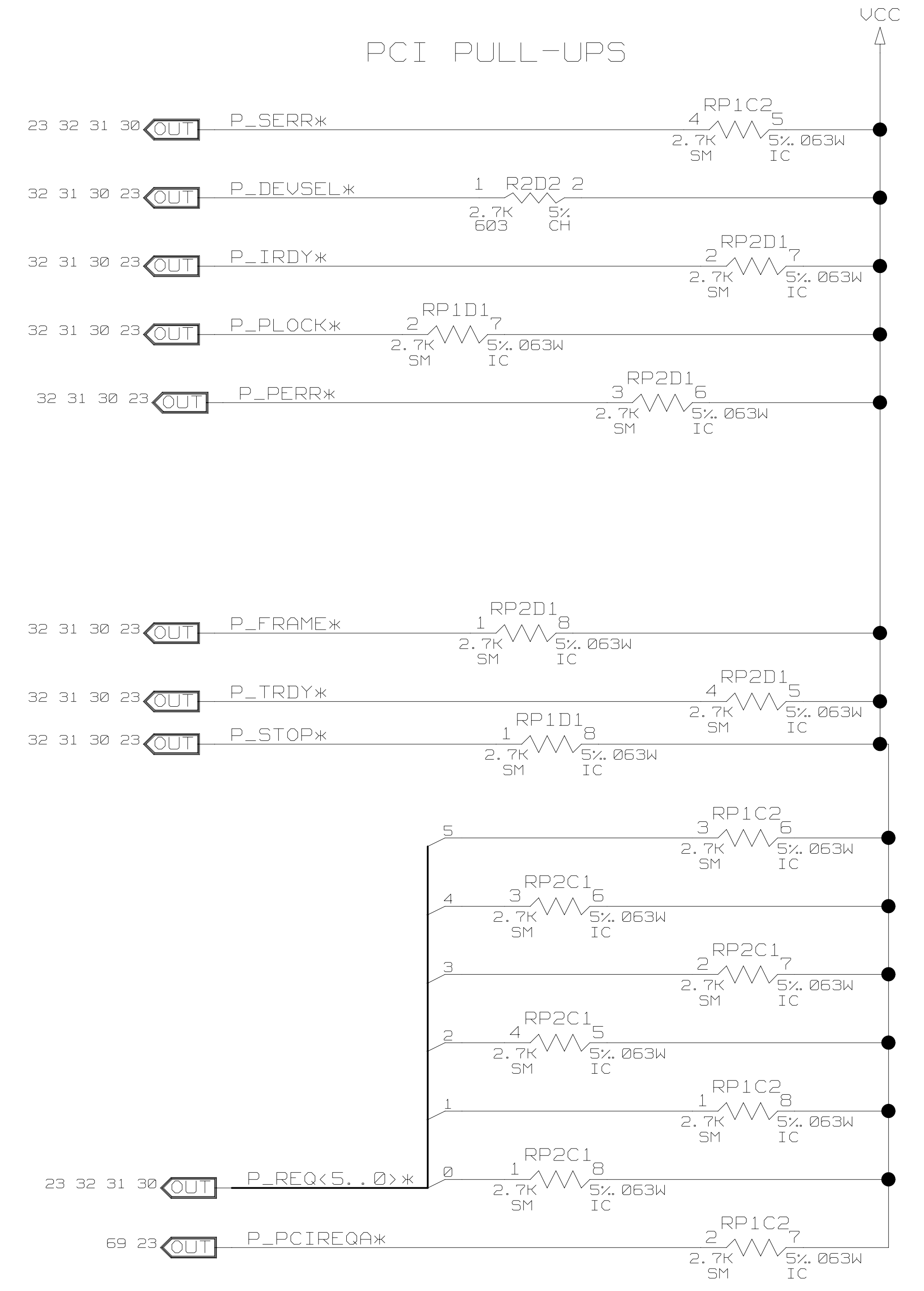

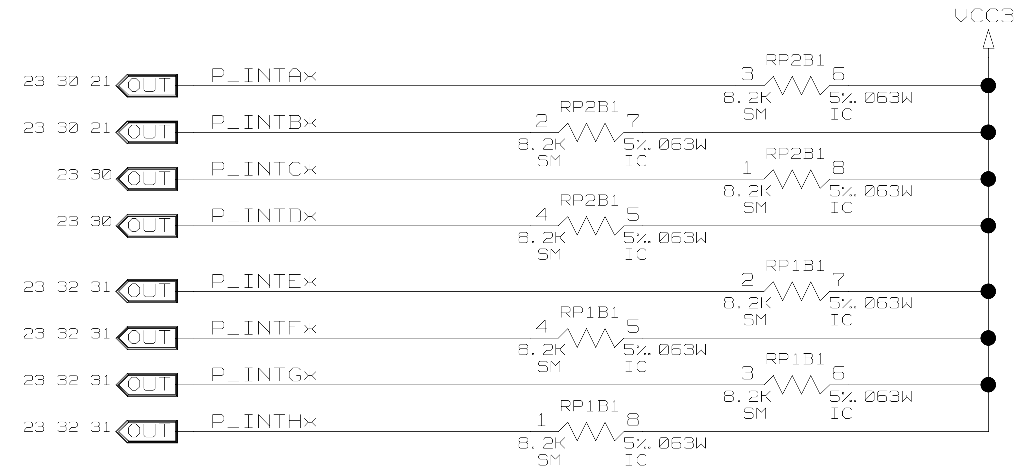

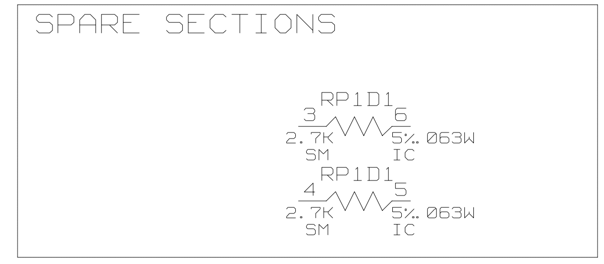

PCI TERMINATION AND DECOUPLING

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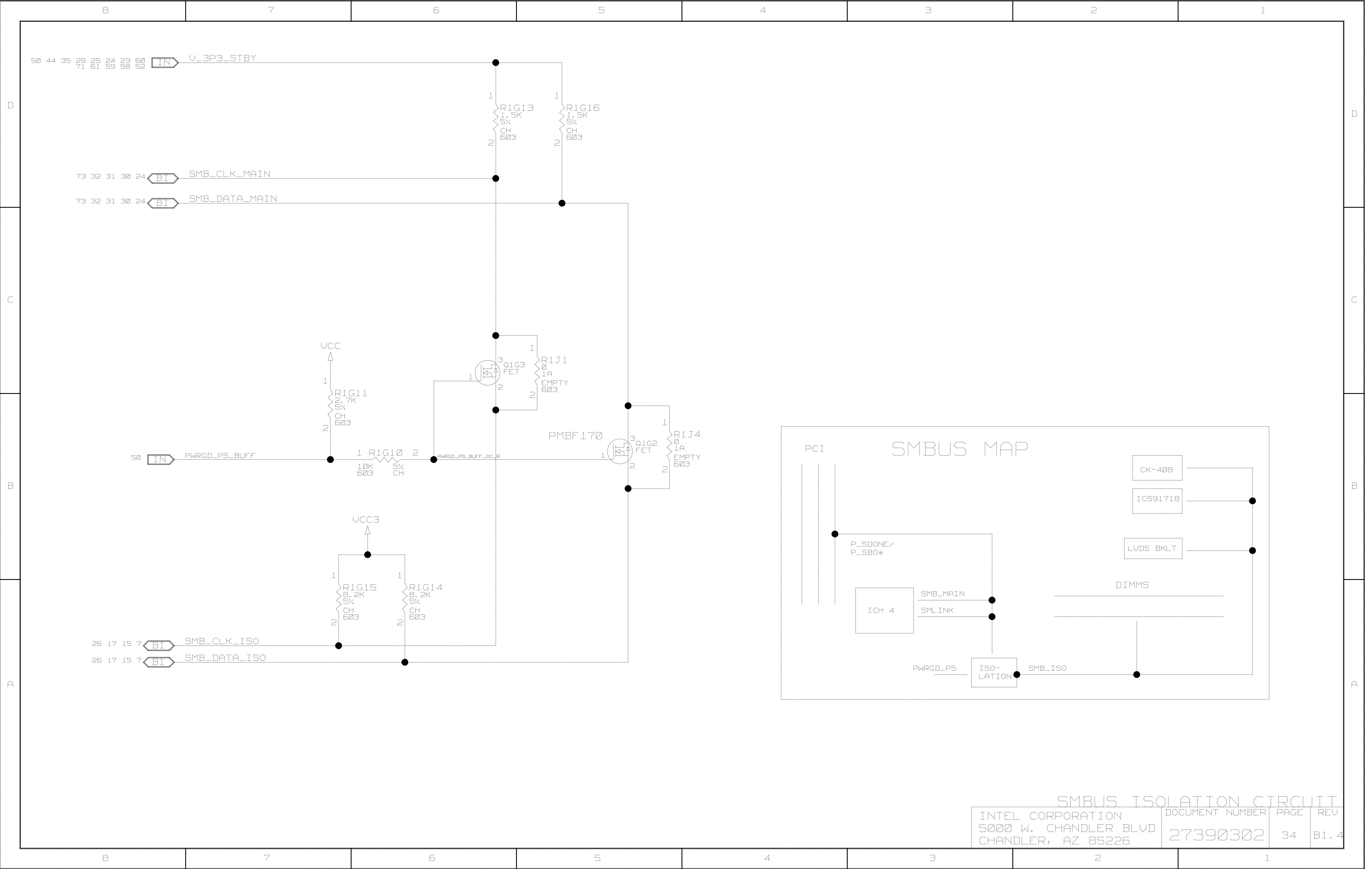
V_3P3_STBY
SMB_CLK_MAIN
SMB_DATA_MAIN
PWRGD_PS_BUFF
SMB_CLK_ISO
SMB_DATA_ISO
R1G13
R1G16
R1G11
R1G10
R1G15
R1G14
R1J1
R1J4
Q1G3
Q1G2
PMBF170
VCC
VCC3
SMBUS MAP
PCI
CK-408
ICS91718
LVDS BKLT
DIMMS
ICH 4
SMB_MAIN
SMLINK
P_SDONE/
P_SBO*
PWRGD_PS
ISO-
LATION
SMB_ISO
SMBUS ISOLATION CIRCUIT
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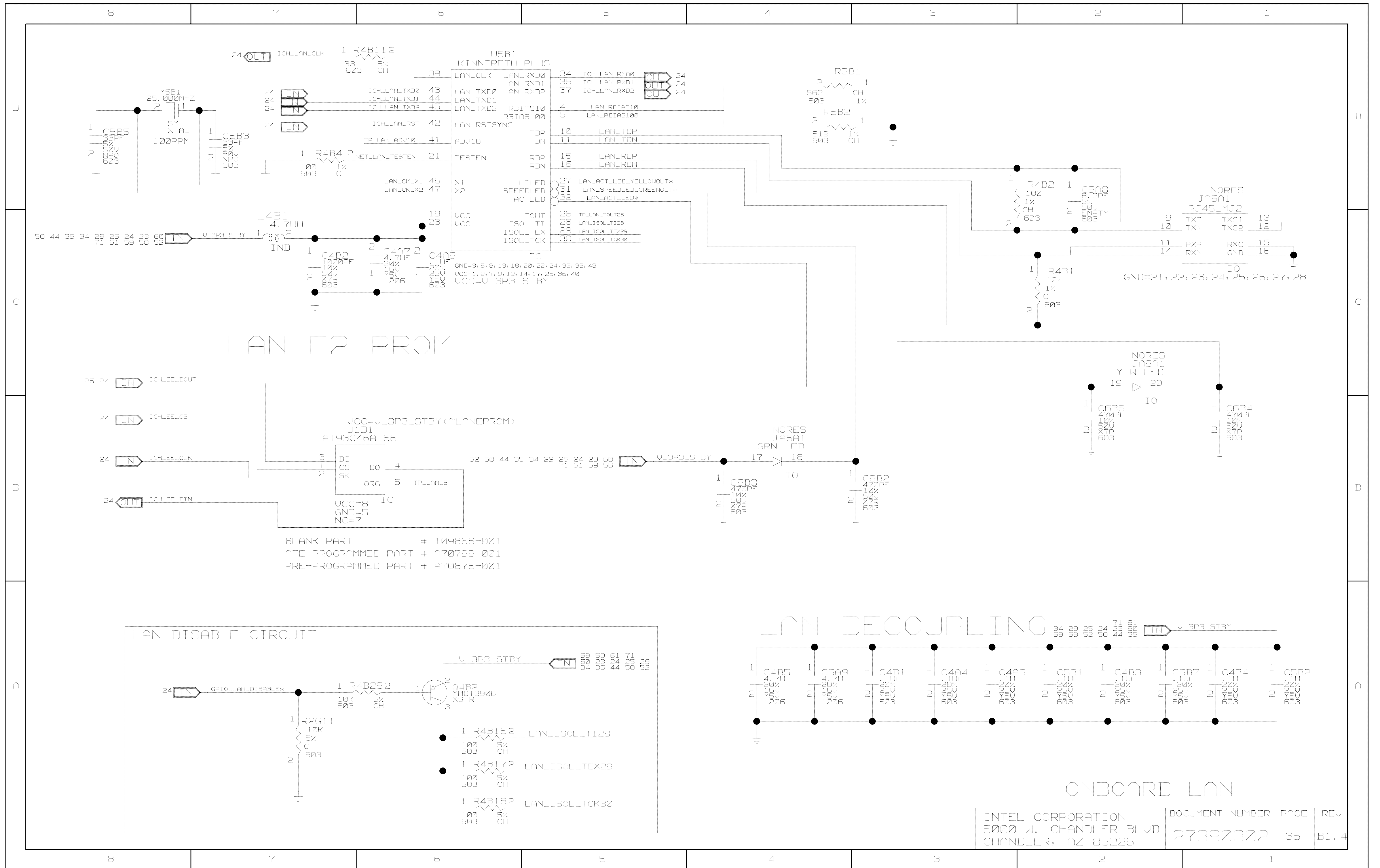

U5B1
KINNERETH_PLUS
LAN E2 PROM
VCC=V_3P3_STBY(~LANEPROM)
U1D1
AT93C46A_66
BLANK PART # 109868-001
ATE PROGRAMMED PART # A70799-001
PRE-PROGRAMMED PART # A70876-001
LAN DISABLE CIRCUIT
LAN DECOUPLING
NORES
JA6A1
RJ45_MJ2
GND=21,22,23,24,25,26,27,28
YLW_LED
GRN_LED
ONBOARD LAN
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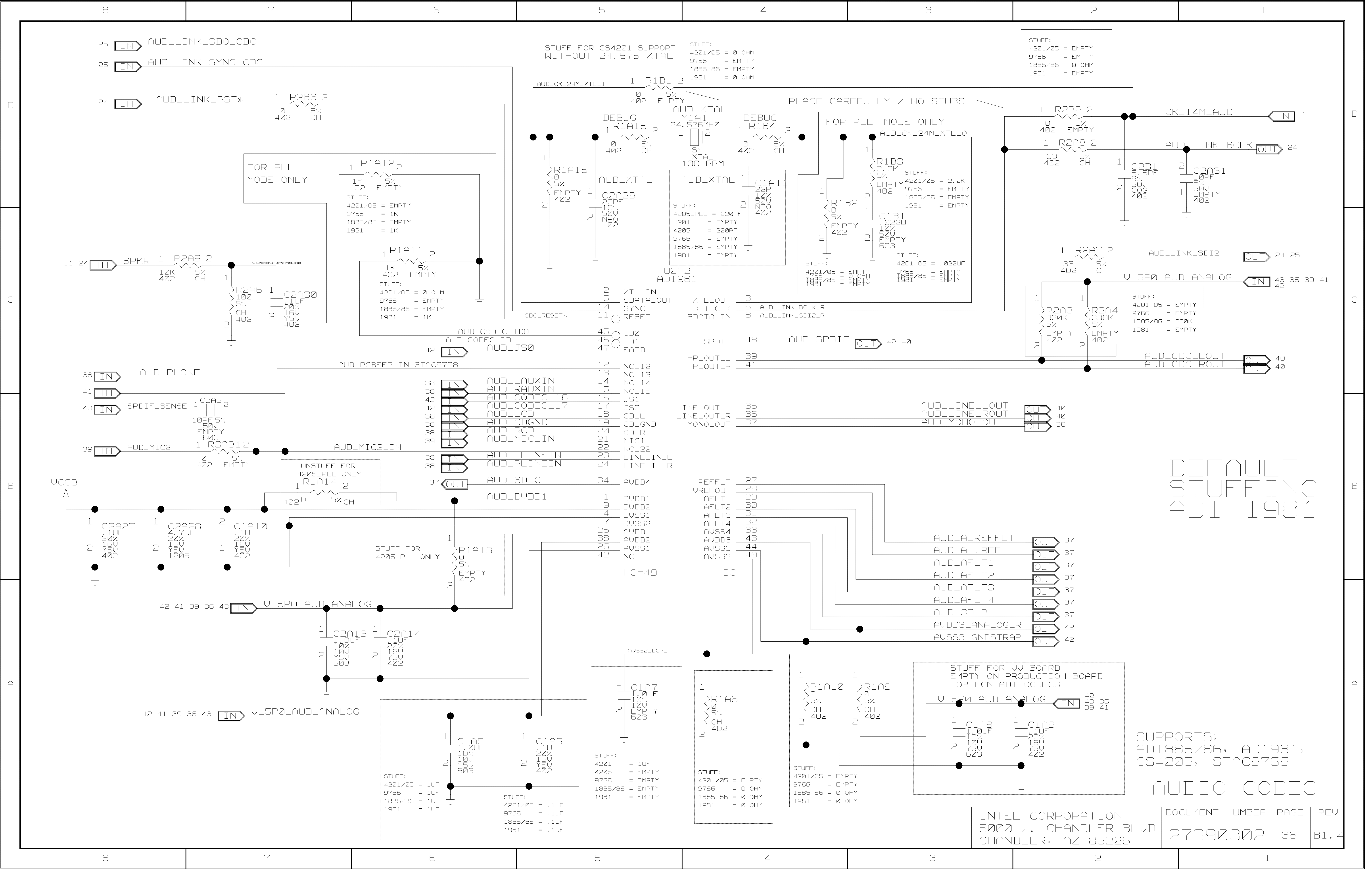

STUFF FOR CS4201 SUPPORT WITHOUT 24.576 XTAL
PLACE CAREFULLY / NO STUBS
FOR PLL MODE ONLY
U2A2
AD1981
UNSTUFF FOR 4205_PLL ONLY
STUFF FOR 4205_PLL ONLY
STUFF FOR VV BOARD EMPTY ON PRODUCTION BOARD FOR NON ADI CODECS
DEFAULT STUFFING ADI 1981
SUPPORTS: AD1885/86, AD1981, CS4205, STAC9766
AUDIO CODEC
INTEL CORPORATION
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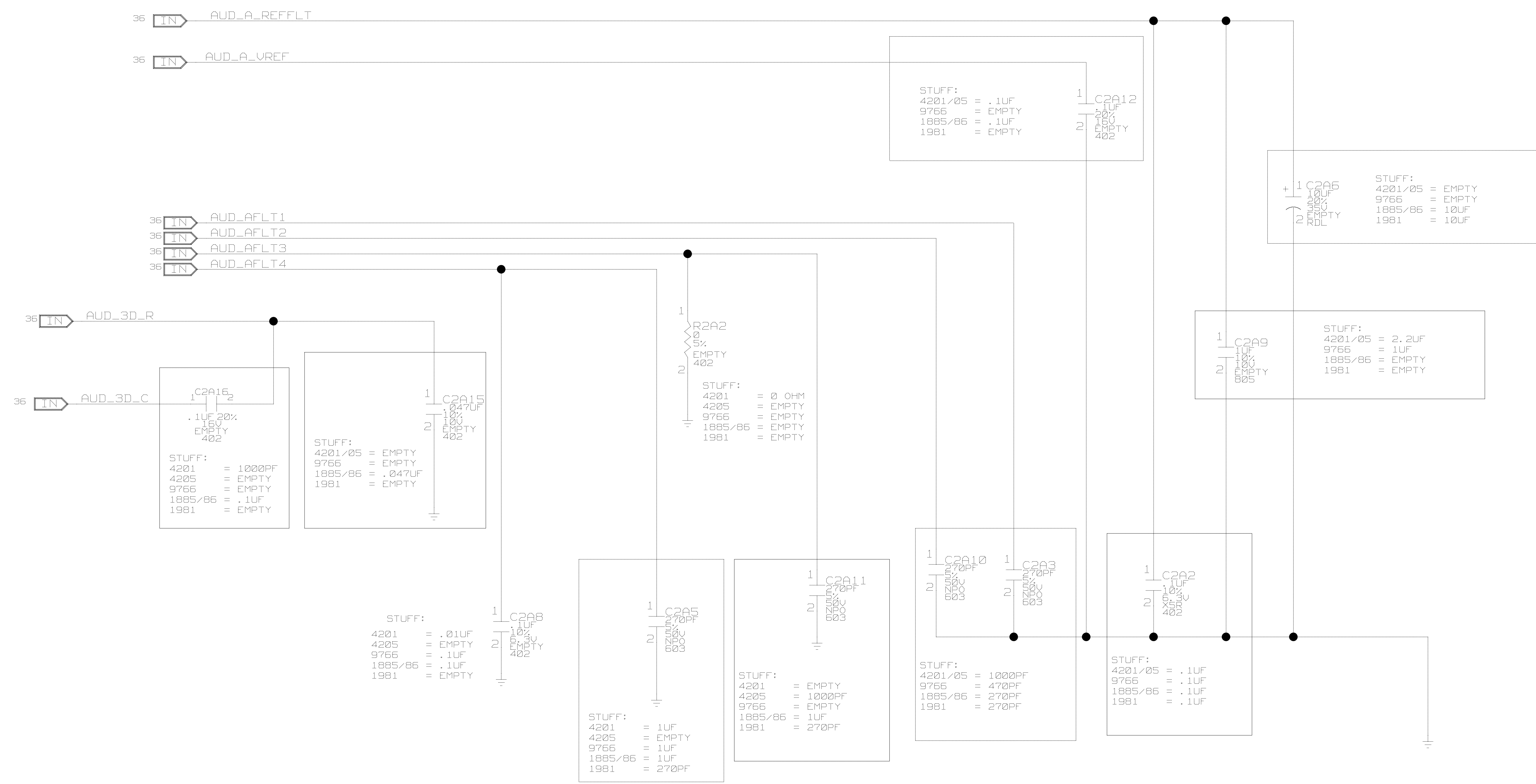

CODEC FILTER CAPS:
1981, 1885/86, 4205, 9766

DEFAULT STUFFING ADI 1981

AUDIO SUBMODULE 2

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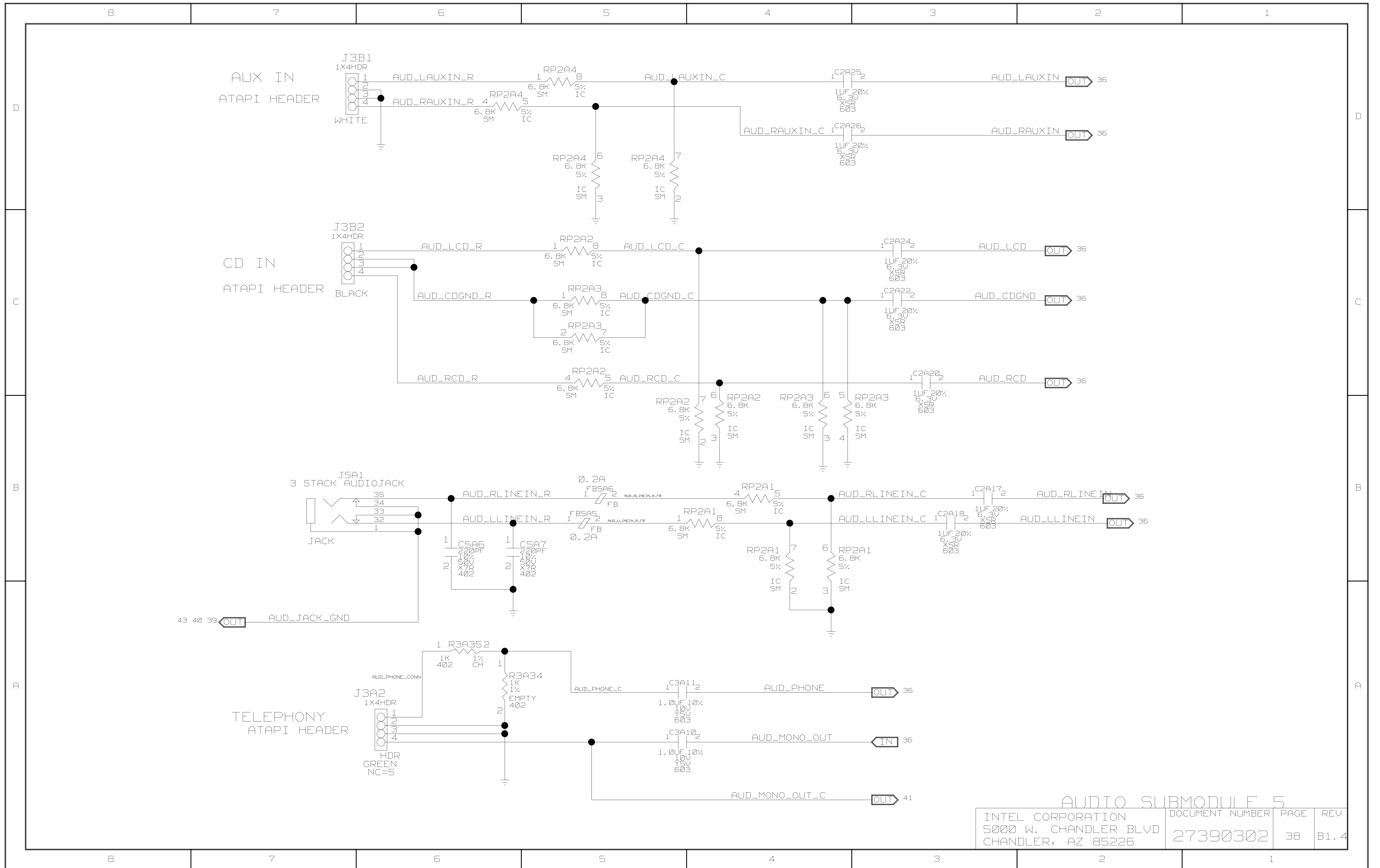

AUX IN
ATAPI HEADER
J3B1
1X4HDR
WHITE
AUD_LAUXIN_R
AUD_RAUXIN_R
RP2A4
AUD_LAUXIN_C
AUD_RAUXIN_C
C2A25
C2A26
1UF 20%
6.3V
X5R
603
AUD_LAUXIN
AUD_RAUXIN
OUT
36
CD IN
ATAPI HEADER
J3B2
1X4HDR
BLACK
AUD_LCD_R
AUD_LCD_C
AUD_CDGND_R
AUD_CDGND_C
AUD_RCD_R
AUD_RCD_C
RP2A2
RP2A3
C2A24
C2A22
C2A20
AUD_LCD
AUD_CDGND
AUD_RCD
6.8K
5%
SM
IC
J5A1
3 STACK AUDIOJACK
JACK
AUD_RLINEIN_R
AUD_LLINEIN_R
0.2A
FB5A6
FB5A5
FB
RP2A1
AUD_RLINEIN_C
AUD_LLINEIN_C
C2A17
C2A18
AUD_RLINEIN
AUD_LLINEIN
C5A6
C5A7
220PF
10%
50V
X7R
402
AUD_JACK_GND
43 40 39
R3A352
1K
1%
CH
R3A34
EMPTY
AUD_PHONE_CONN
AUD_PHONE_C
C3A11
C3A10
1.0UF 10%
10V
Y5V
603
AUD_PHONE
AUD_MONO_OUT
IN
AUD_MONO_OUT_C
41
J3A2
1X4HDR
TELEPHONY
ATAPI HEADER
HDR
GREEN
NC=5
AUDIO SUBMODULE 5
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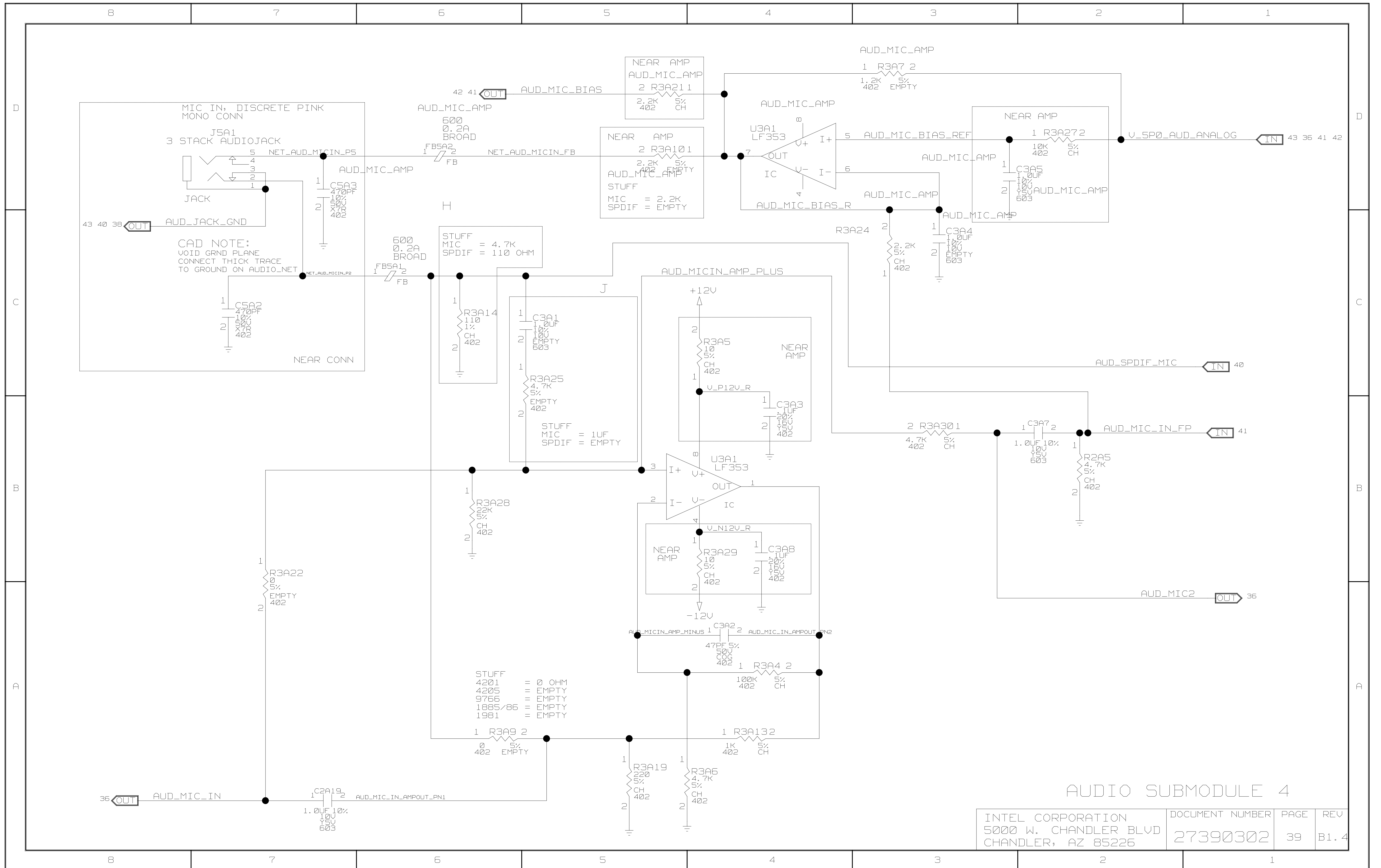

AUD_MIC_AMP
1 R3A7 2
1.2K 5% 402 EMPTY
NEAR AMP
AUD_MIC_AMP
2 R3A21 1
2.2K 5% 402 CH
42 41 OUT AUD_MIC_BIAS
MIC IN, DISCRETE PINK
MONO CONN
J5A1
3 STACK AUDIOJACK
JACK
NET_AUD_MICIN_P5
AUD_MIC_AMP
600
0.2A
BROAD
FB5A2
FB
NET_AUD_MICIN_FB
NEAR AMP
2 R3A10 1
2.2K 5% 402 EMPTY
AUD_MIC_AMP
STUFF
MIC = 2.2K
SPDIF = EMPTY
U3A1
LF353
OUT
IC
AUD_MIC_BIAS_REF
AUD_MIC_BIAS_R
NEAR AMP
1 R3A27 2
10K 5% 402 CH
V_5P0_AUD_ANALOG
IN 43 36 41 42
C3A5
1.0UF 10% 10V Y5V 603
C3A4
1.0UF 10% 10V EMPTY 603
R3A24
2.2K 5% CH 402
C5A3
470PF 10% 50V X7R 402
43 40 38 OUT AUD_JACK_GND
CAD NOTE:
VOID GRND PLANE
CONNECT THICK TRACE
TO GROUND ON AUDIO_NET
NET_AUD_MICIN_P2
C5A2
470PF 10% 50V X7R 402
NEAR CONN
H
STUFF
MIC = 4.7K
SPDIF = 110 OHM
600
0.2A
BROAD
FB5A1
FB
R3A14
110 1% CH 402
J
C3A1
1.0UF 10% 10V EMPTY 603
R3A25
4.7K 5% EMPTY 402
STUFF
MIC = 1UF
SPDIF = EMPTY
AUD_MICIN_AMP_PLUS
+12V
R3A5
10 5% CH 402
NEAR AMP
V_P12V_R
C3A3
1UF 20% 16V Y5V 402
AUD_SPDIF_MIC
IN 40
2 R3A30 1
4.7K 5% 402 CH
C3A7
1.0UF 10% 10V Y5V 603
AUD_MIC_IN_FP
IN 41
R2A5
4.7K 5% CH 402
U3A1
LF353
OUT
IC
R3A28
22K 5% CH 402
V_N12V_R
NEAR AMP
R3A29
10 5% CH 402
C3A8
1UF 20% 16V Y5V 402
-12V
AUD_MIC2
OUT 36
R3A22
0 5% EMPTY 402
AUD_MICIN_AMP_MINUS
C3A2
47PF 5% 50V COG 402
AUD_MIC_IN_AMPOUT_PN2
1 R3A4 2
100K 5% 402 CH
STUFF
4201 = 0 OHM
4205 = EMPTY
9766 = EMPTY
1885/86 = EMPTY
1981 = EMPTY
1 R3A9 2
0 5% 402 EMPTY
1 R3A13 2
1K 5% 402 CH
R3A19
220 5% CH 402
R3A6
4.7K 5% CH 402
36 OUT AUD_MIC_IN
C2A19
1.0UF 10% 10V Y5V 603
AUD_MIC_IN_AMPOUT_PN1
AUDIO SUBMODULE 4
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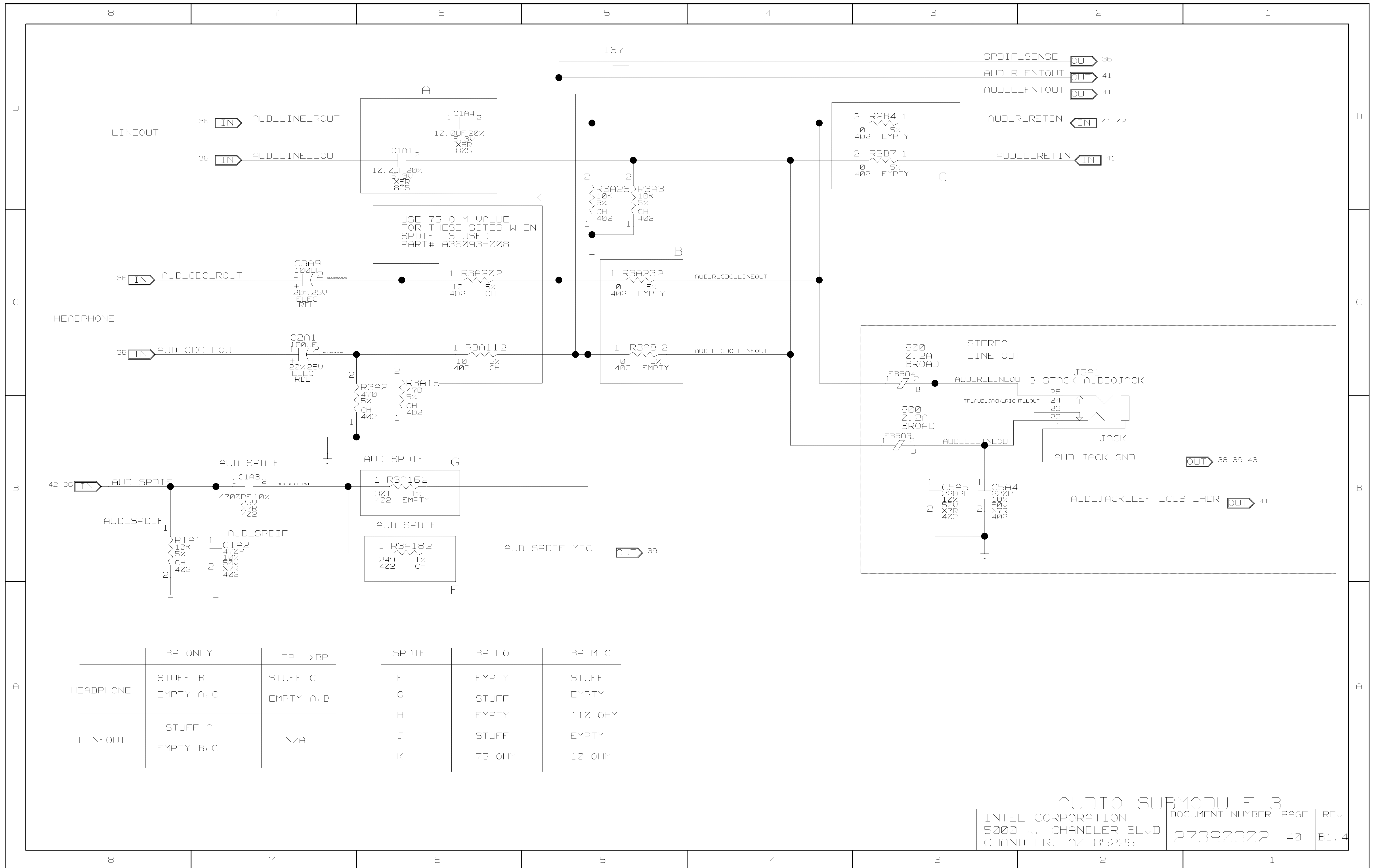

	BP ONLY	FP-->BP
HEADPHONE	STUFF B EMPTY A, C	STUFF C EMPTY A, B
LINEOUT	STUFF A EMPTY B, C	N/A

SPDIF	BP LO	BP MIC
F	EMPTY	STUFF
G	STUFF	EMPTY
H	EMPTY	110 OHM
J	STUFF	EMPTY
K	75 OHM	10 OHM

AUDIO SUBMODULE 3

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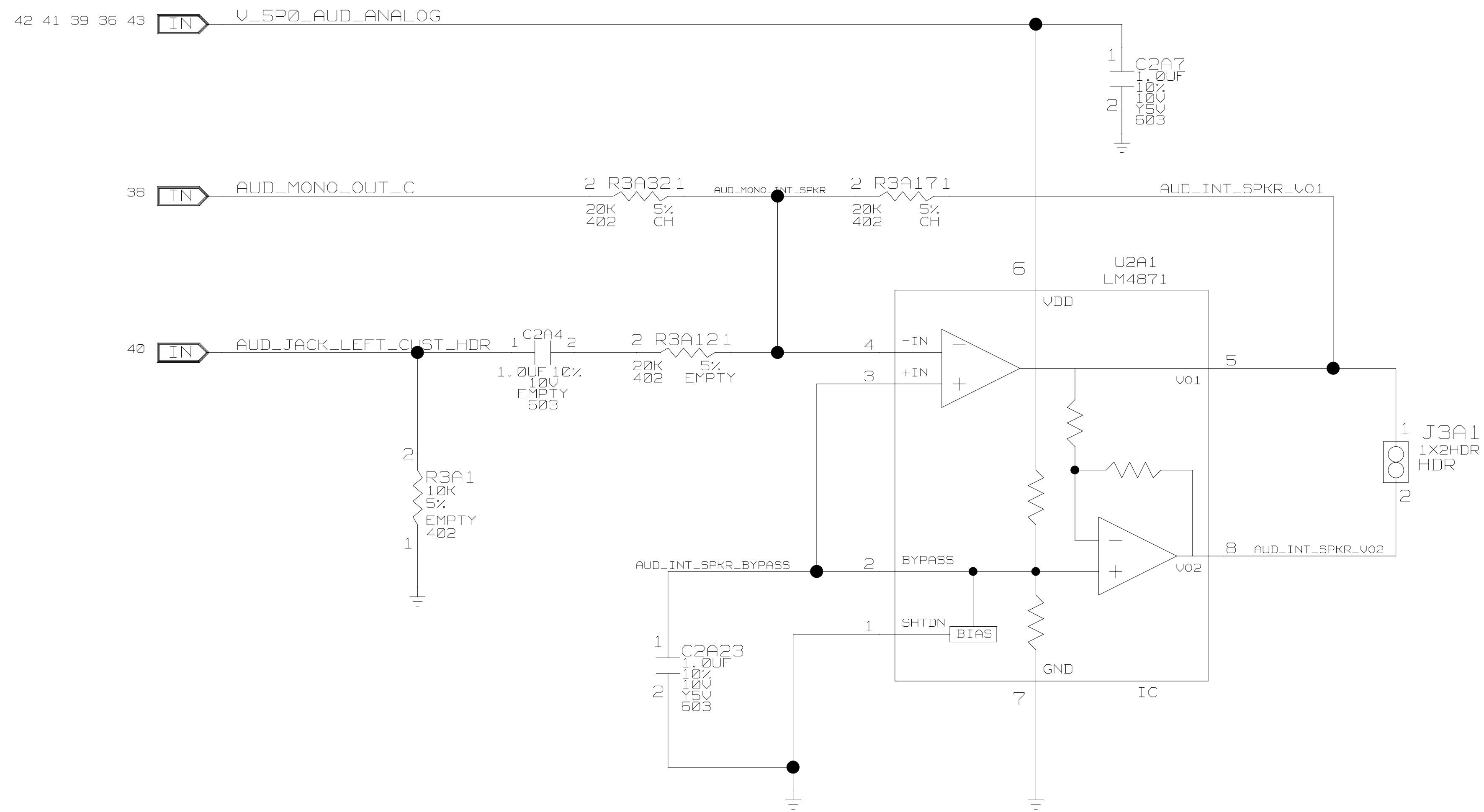
NOTE:
FP DONGLE MUST HAVE
MIC JACK RING SHUNT SPRING
TERMINAL CONNECTED
TO GND FOR PROPER
MIC SENSING OPERATION

PLACE NEAR AUDIO CIRCUIT

INTERNAL SPEAKER CIRCUIT



AUDIO FRONT PANEL

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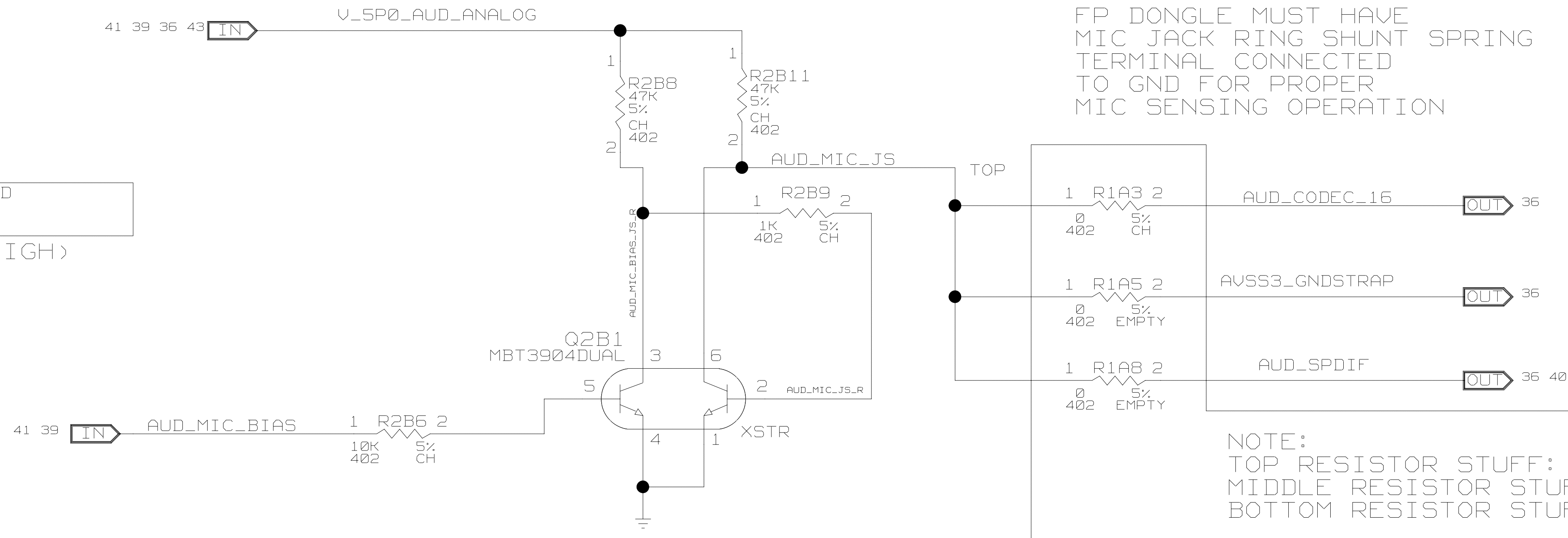
GPIO LOCATIONS:

NOT CONNECTED

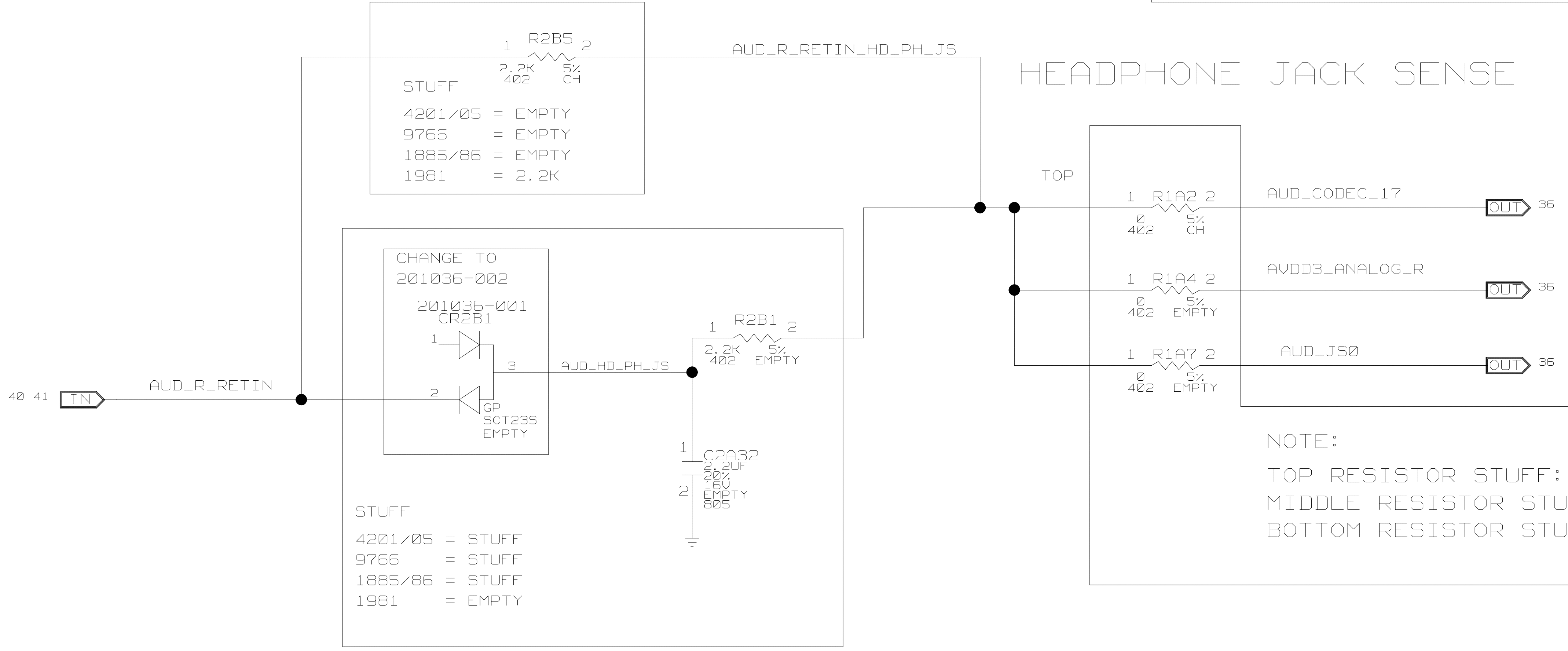
4205: 43, 44, 41, 40, 39
1981: 16, 17 (ACTIVE HIGH)
9766: 43, 44
4291: NONE
1885/86: 47, 48

MIC JACK SENSE

NOTE:
FP DONGLE MUST HAVE
MIC JACK RING SHUNT SPRING
TERMINAL CONNECTED
TO GND FOR PROPER
MIC SENSING OPERATION



HEADPHONE JACK SENSE



DEFAULT
STUFFING
ADI 1981

MIC/HEADPHONE

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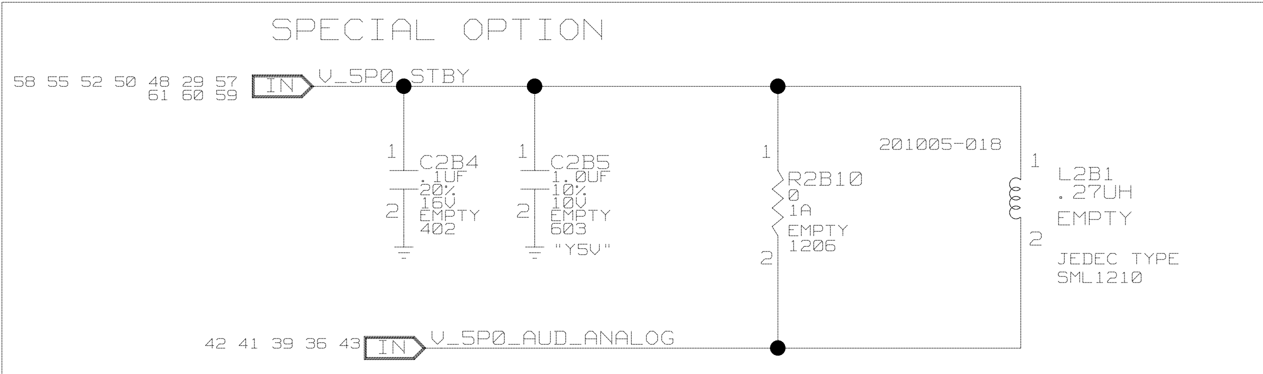
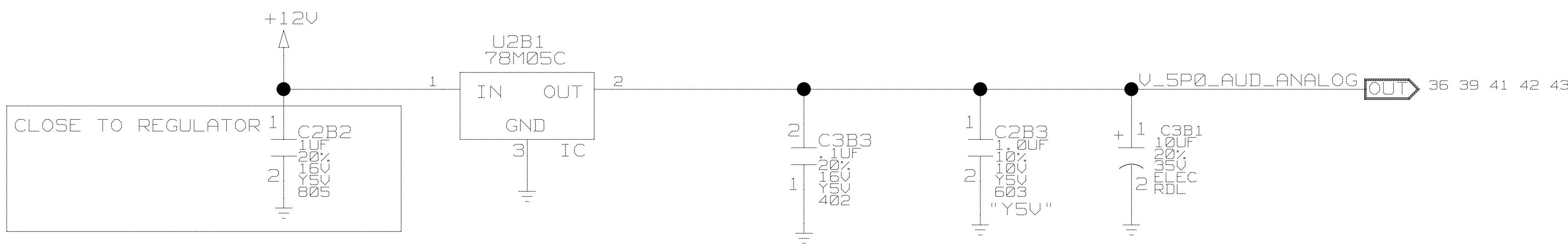
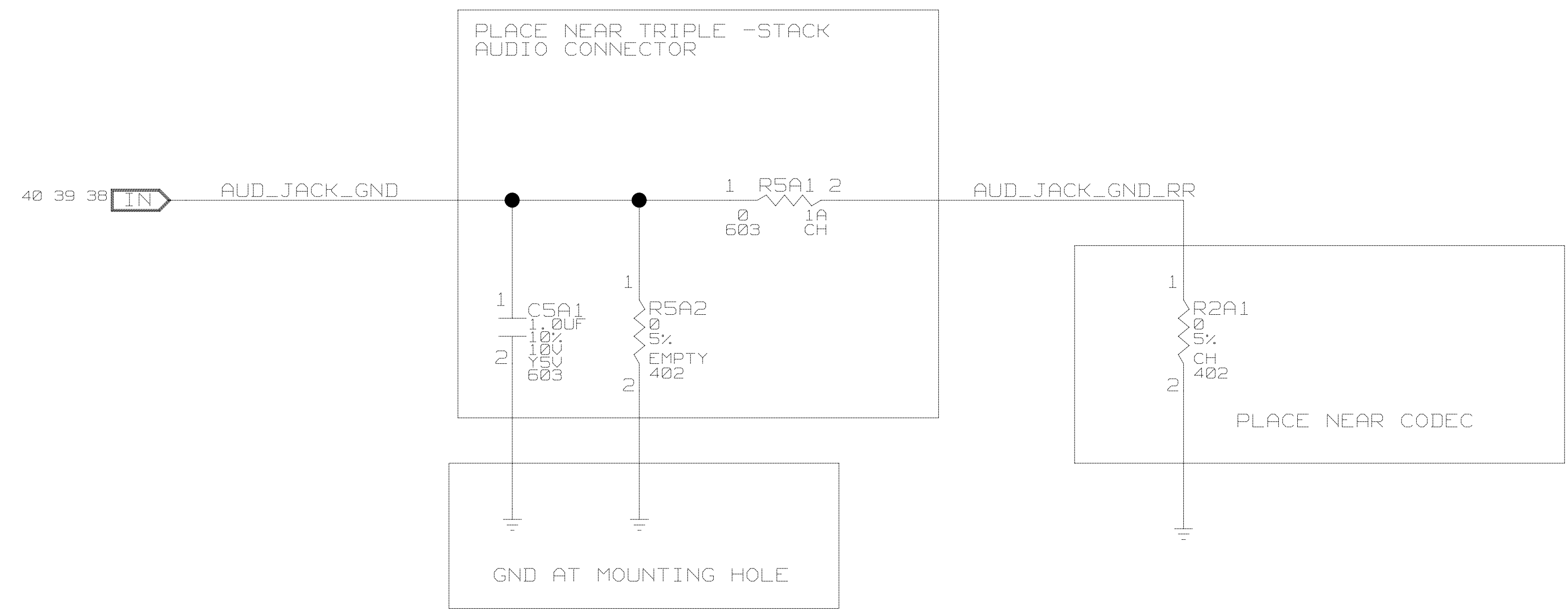


REGULATOR THERMAL TAB SHOULD BE SOLDERED
TO A COPPER PAD THAT IS LARGE ENOUGH
TO ALLOW 5 TO 10 GROUND VIAS AROUND
THE COMPONENT FOR COOLING



NOTE:
LAYOUT SHOULD GO FROM PIN 2 TO
CAPS AND THEN THROUGH SEVERAL
VIAS TO V_5P0_AUD_ANALOG



AUDIO VREG

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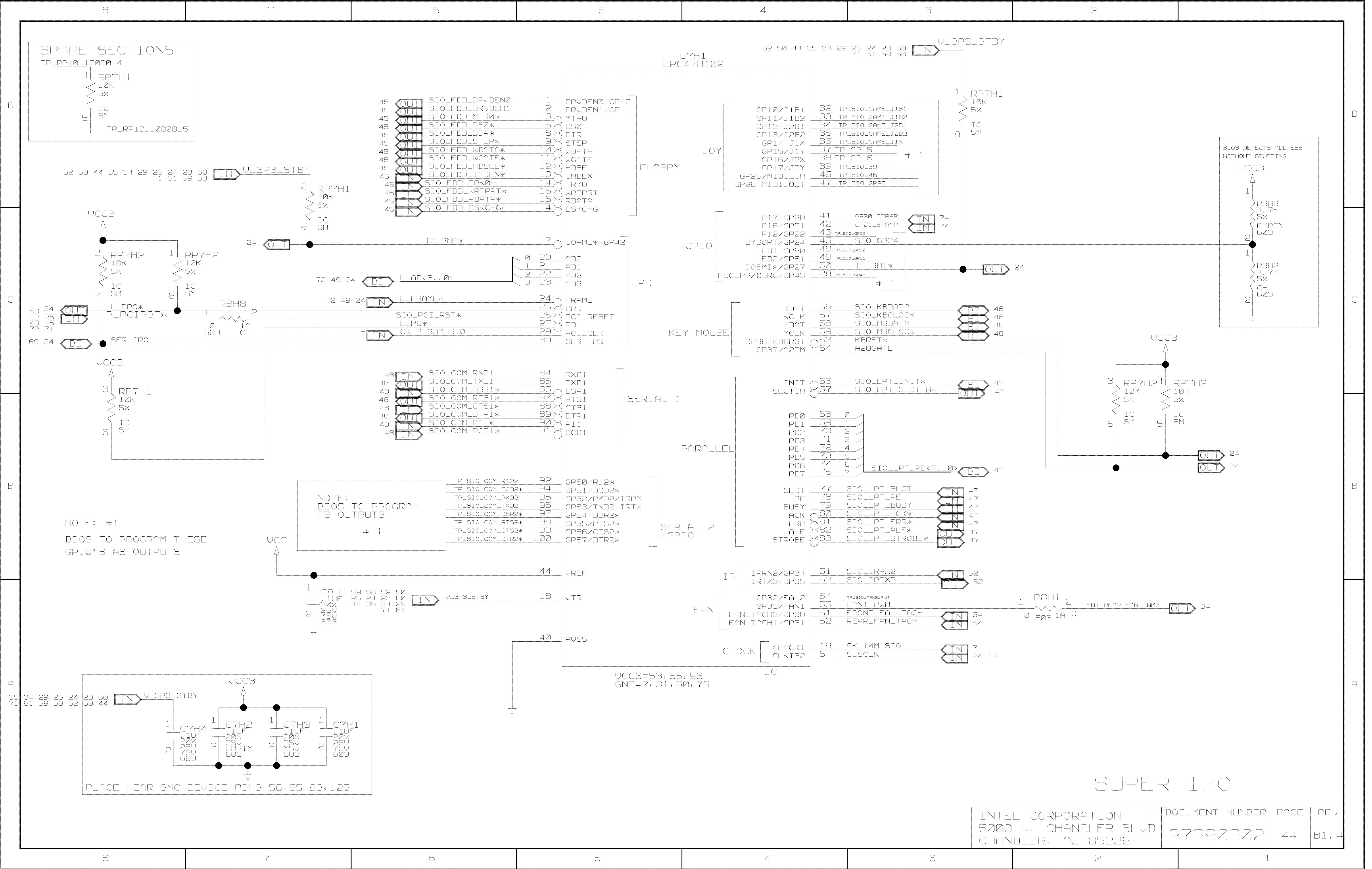
SPARE SECTIONS
U7H1
LPC47M102
FLOPPY
LPC
SERIAL 1
SERIAL 2 /GPIO
JOY
GPIO
KEY/MOUSE
PARALLEL
IR
FAN
CLOCK
BIOS DETECTS ADDRESS WITHOUT STUFFING
NOTE: BIOS TO PROGRAM AS OUTPUTS # 1
NOTE: #1
BIOS TO PROGRAM THESE GPIO'S AS OUTPUTS
VCC3=53,65,93
GND=7,31,60,76
PLACE NEAR SMC DEVICE PINS 56,65,93,125
SUPER I/O
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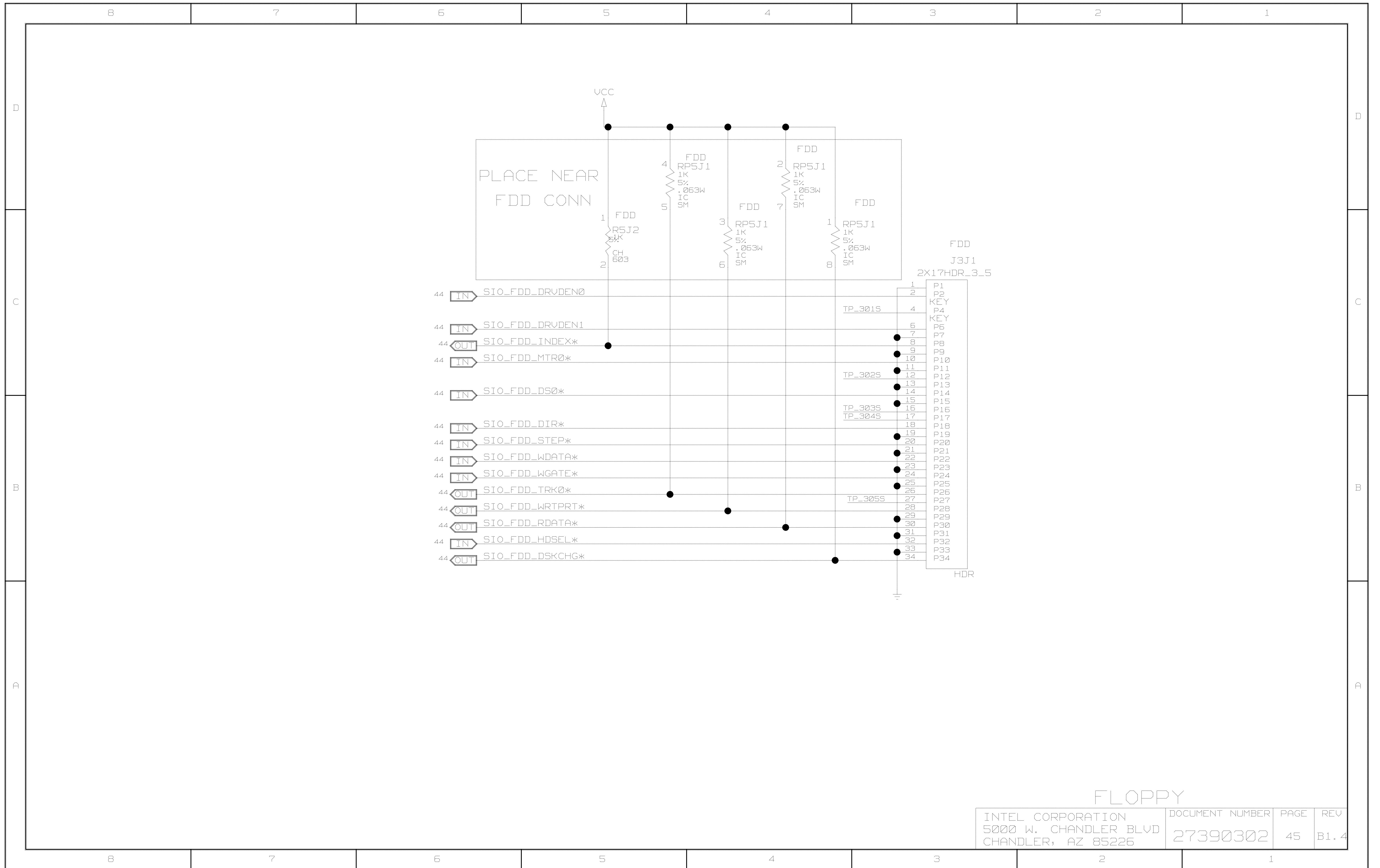
VCC
PLACE NEAR
FDD CONN
FDD
R5J2
1K
5%
CH
603
RP5J1
1K
5%
.063W
IC
SM
FDD
J3J1
2X17HDR_3_5
HDR
SIO_FDD_DRVDEN0
SIO_FDD_DRVDEN1
SIO_FDD_INDEX*
SIO_FDD_MTR0*
SIO_FDD_DS0*
SIO_FDD_DIR*
SIO_FDD_STEP*
SIO_FDD_WDATA*
SIO_FDD_WGATE*
SIO_FDD_TRK0*
SIO_FDD_WRTPRT*
SIO_FDD_RDATA*
SIO_FDD_HDSEL*
SIO_FDD_DSKCHG*
IN
OUT
TP_301S
TP_302S
TP_303S
TP_304S
TP_305S
KEY
FLOPPY
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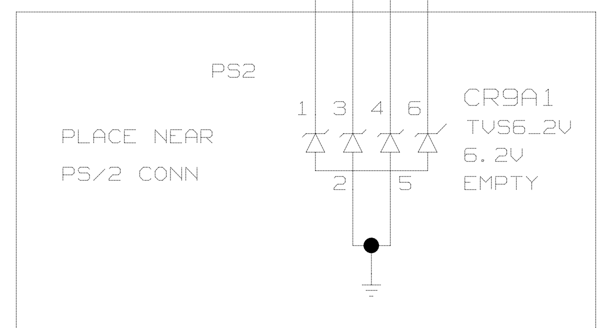
COMPONENTS ARE DFM29

PS2 KEYBOARD

MOUSE



PLACE AS CLOSE TO PS/2 CONNECTOR AS POSSIBLE

ATX DOUBLE-STACKED

PS/2 STACK

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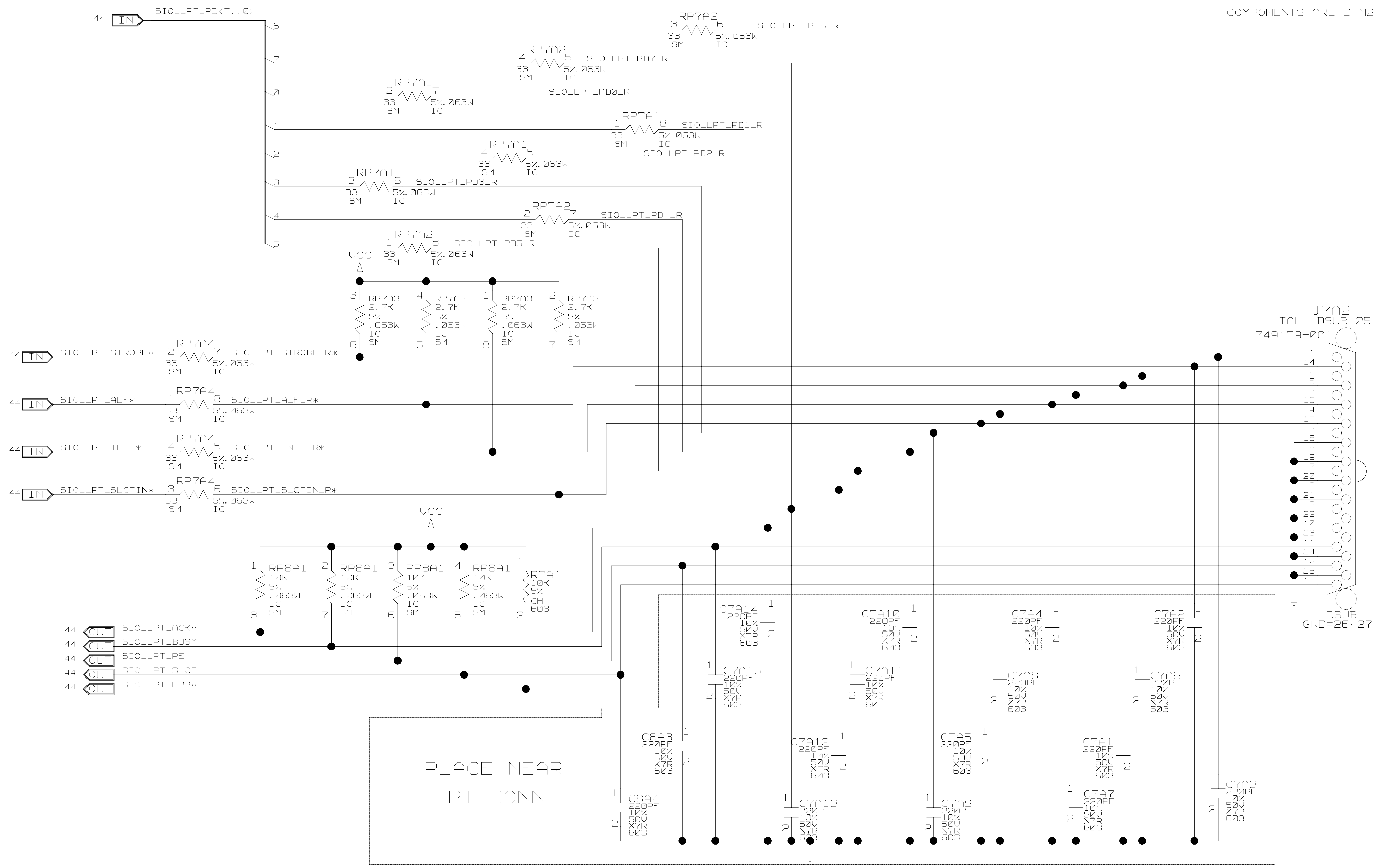

PARALLEL PORT

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5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

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COMPONENTS ARE DFM29

SERIAL PORT A

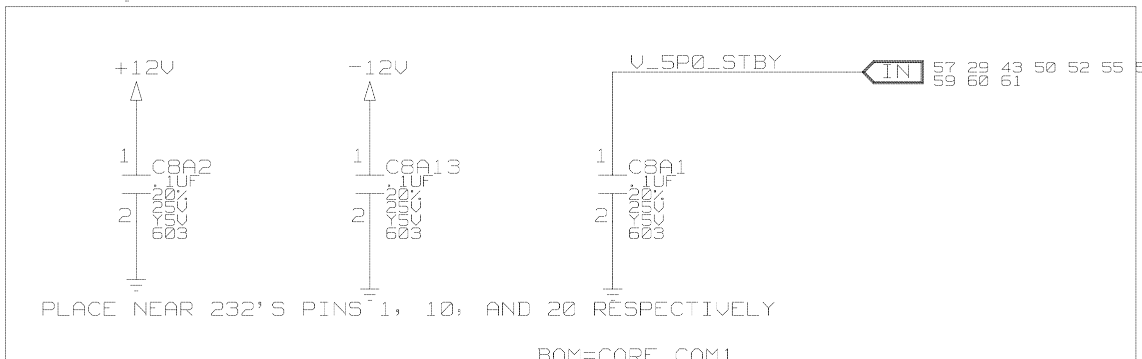
DO NOT USE NATIONAL
OR GOLDSTAR PARTS OF THIS
BASE P/N

U8A1
GD75232S

J8A1
2 ROW

NOTE DIRECTION
IC

VCC=20
GND=11
VCC=V_5P0_STBY



SERIAL PORT

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RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY

* DEFAULT JUMPER SETTING

CONFIGURE= SAFE MODE

J1G4
1X3HDR
RECOVERY_CONFIGURE_PULLUP
25 24 IN AUD_LINK_SDO_R
HDR

U1H1
FWH

72 44 24 BI L_AD<3..0>

66 59 29 24 12 50 IN PWRGD_3V
RP1H1 8 4.7K SM 1 5% IC — 7 WP
RP1H1 6 4.7K SM 3 5% IC — 8 TBL
TP_FWH_29 — 29 IC
72 71 50 44 15 12 25 IN P_PCIRST* — R2H11 2 47 603 1 5% CH — FWH_PCIRST* — 2 RST
7 IN CK_P_33M_FWH — 31 CLK
72 44 24 IN L_FRAME* — 23 FWH4

+12V
R1H2 1K 5% CH 603
VCC3
Q1H1 FET
FWH_VPP — 1 VPP
C1G10 .1UF 20% 25V Y5V 603

VCC3
27 VCCA/NC
32 VCC
25 VCC
28 GNDA/NC
16 GND
26 GND

FWH3 17 3
FWH2 15 2
FWH1 14 1
FWH0 13 0
DQ4/RFU 18 TP_FWH_13
DQ5/RFU 19 TP_FWH_19
DQ6/RFU 20 TP_FWH_20
DQ7/RFU 21 TP_FWH_21
RY/BY/RFU 22 TP_FWH_22
FGPI4 30 PN_FWH_GPI4
FGPI3 3 PN_FWH_GPI3
FGPI2 4 PN_FWH_GPI2
FGPI1 5 GPIO_DMA66_DETECT_SEC IN 27
FGPI0 6 GPIO_DMA66_DETECT_PRI IN 27
INIT 24 FWH_H_INIT* IN 49
ID3 9 TP_FWH_9
ID2 10 TP_FWH_10
ID1 11 TP_FWH_11
ID0 12 TP_FWH_12

723644-009 IC

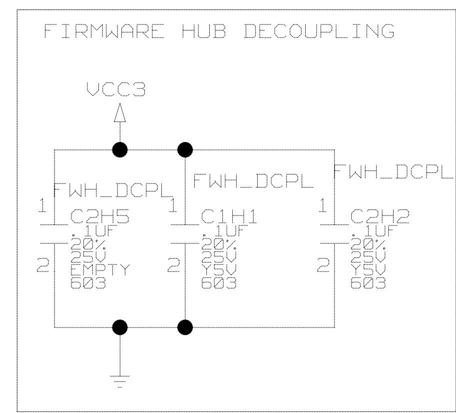
J2J2
JUMPER
EMPTY
ALWAYS EMPTY

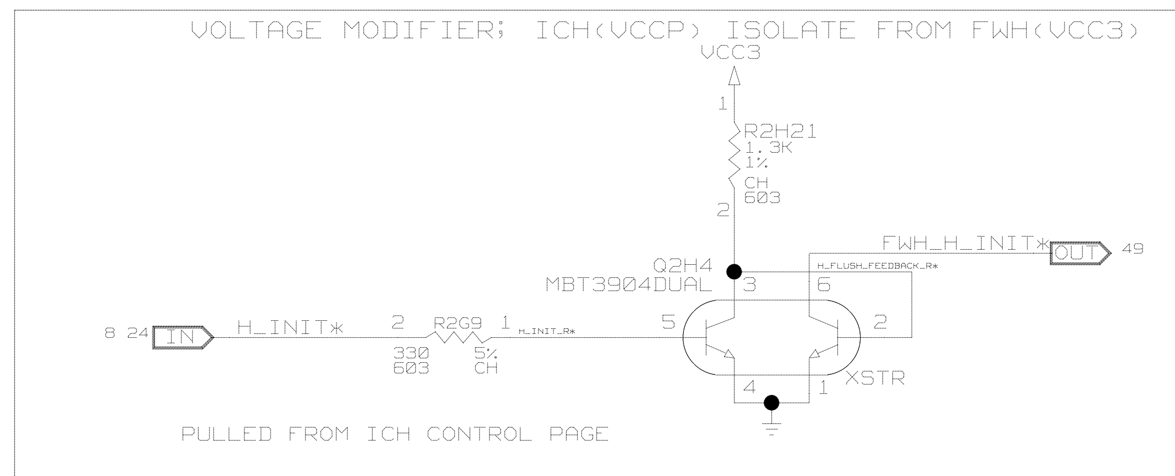
RP1H1 4.7K 5% IC SM
R1G12 1K 5% CH 603
VCC3
RP1H1 4.7K 5% IC SM
R2H22 330 5% CH 603
R1H5 10K 5% EMPTY 603
R1H7 10K 5% CH 603

NOTE:
PULLDOWNS ON GPI0 AND GPI1
ARE ON IDE PAGE

FWH SOCKET - INTEL P/N: 201138-032, AMP P/N: 822475-1

PLCC EXTRACTION TOOL
AMP: 821980-1 OR
AMP: 822476-1





FIRMWARE HUB

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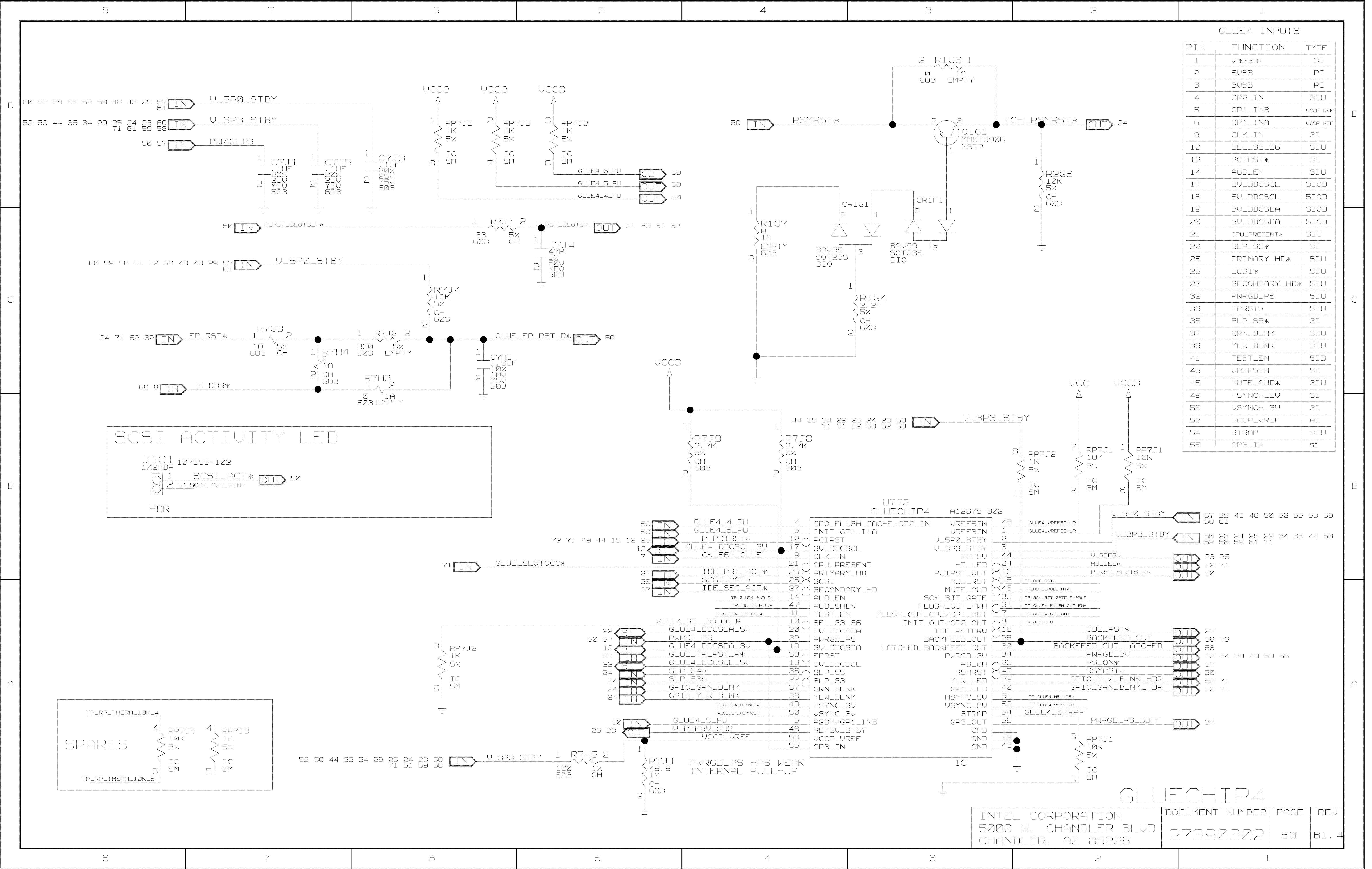
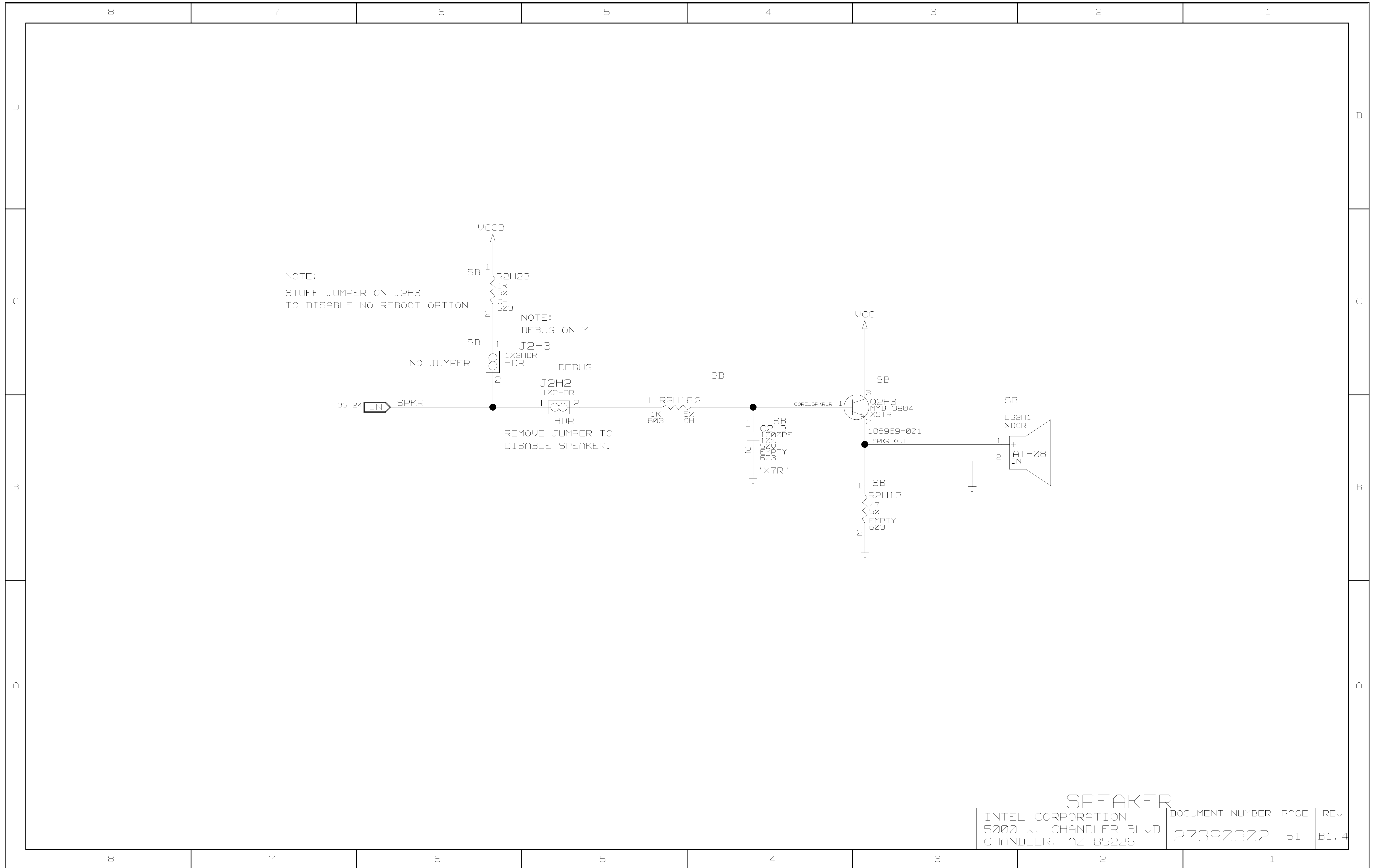


GLUE4 INPUTS

PIN	FUNCTION	TYPE
1	VREF3IN	3I
2	5VSB	PI
3	3VSB	PI
4	GP2_IN	3IU
5	GP1_INB	VCCP REF
6	GP1_INA	VCCP REF
9	CLK_IN	3I
10	SEL_33_66	3IU
12	PCIRST*	3I
14	AUD_EN	3IU
17	3V_DDCSCL	3IOD
18	5V_DDCSCL	5IOD
19	3V_DDCSDA	3IOD
20	5V_DDCSDA	5IOD
21	CPU_PRESENT*	3IU
22	SLP_S3*	3I
25	PRIMARY_HD*	5IU
26	SCSI*	5IU
27	SECONDARY_HD*	5IU
32	PWRGD_PS	5IU
33	FPRST*	5IU
36	SLP_S5*	3I
37	GRN_BLNK	3IU
38	YLW_BLNK	3IU
41	TEST_EN	5ID
45	VREF5IN	5I
46	MUTE_AUD*	3IU
49	HSYNCH_3V	3I
50	VSYNCH_3V	3I
53	VCCP_VREF	AI
54	STRAP	3IU
55	GP3_IN	5I



VCC3
SB
R2H23
1K
5%
CH
603
NOTE:
STUFF JUMPER ON J2H3
TO DISABLE NO_REBOOT OPTION
NOTE:
DEBUG ONLY
J2H3
1X2HDR
HDR
NO JUMPER
DEBUG
J2H2
1X2HDR
HDR
36 24
IN
SPKR
R2H162
1K
603
5%
CH
REMOVE JUMPER TO
DISABLE SPEAKER.
C2H3
1000PF
10%
50V
EMPTY
603
"X7R"
VCC
CORE_SPKR_R
Q2H3
MMBT3904
XSTR
108969-001
SPKR_OUT
R2H13
47
5%
EMPTY
603
LS2H1
XDCR
AT-08
IN
SPEAKER
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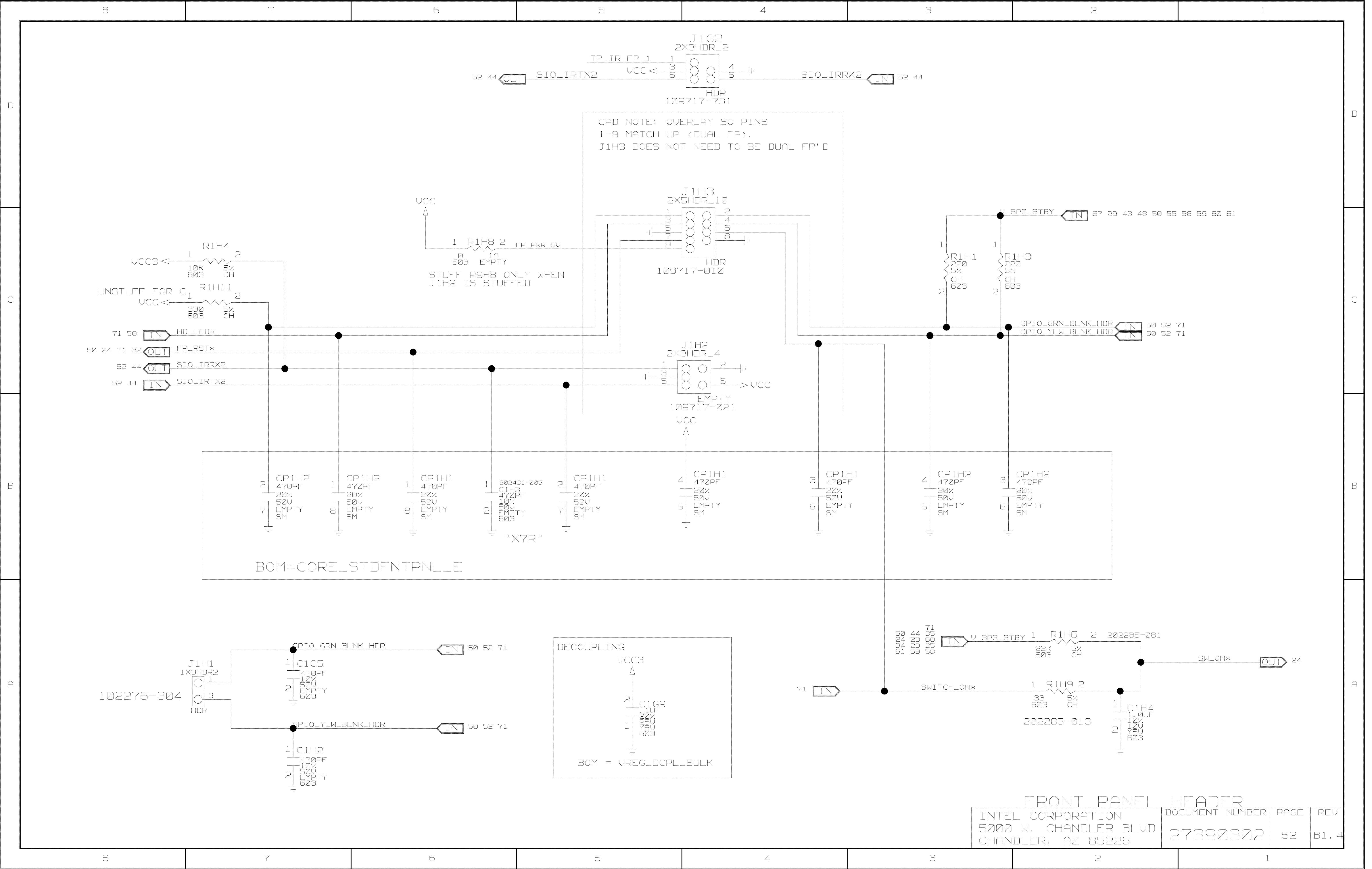
J1G2
2X3HDR_2
TP_IR_FP_1
VCC
SIO_IRTX2
SIO_IRRX2
HDR
109717-731
CAD NOTE: OVERLAY SO PINS
1-9 MATCH UP (DUAL FP).
J1H3 DOES NOT NEED TO BE DUAL FP'D
J1H3
2X5HDR_10
HDR
109717-010
VCC
R1H8
FP_PWR_5V
STUFF R9H8 ONLY WHEN
J1H2 IS STUFFED
R1H4
VCC3
UNSTUFF FOR C
R1H11
VCC
HD_LED*
FP_RST*
SIO_IRRX2
SIO_IRTX2
V_5P0_STBY
R1H1
R1H3
GPIO_GRN_BLNK_HDR
GPIO_YLW_BLNK_HDR
J1H2
2X3HDR_4
EMPTY
109717-021
BOM=CORE_STDFNTPNL_E
"X7R"
J1H1
1X3HDR2
102276-304
HDR
C1G5
C1H2
DECOUPLING
VCC3
C1G9
BOM = VREG_DCPL_BULK
V_3P3_STBY
R1H6
202285-081
SW_ON*
SWITCH_ON*
R1H9
202285-013
C1H4
FRONT PANEL HEADER
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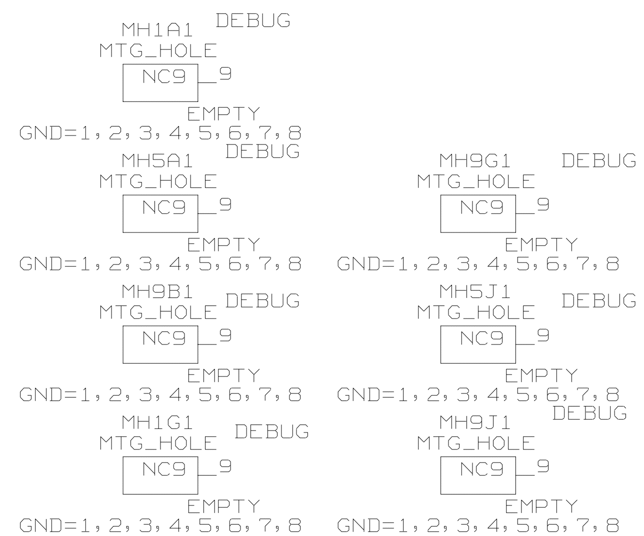

CONNECTOR LOCATION

	X	Y
PS/2	8525	6210
USB/LAN	7965	5927
COM	6940	6115
PAR	5362	5843
VGA	5136	6190
DIAGLED	4636	6045
USB	4151	6026
AUD	3291	6218

LABELS

DEBUG
LB8H1
SILK
1
INTELtm

'INTEL' LOGO SILKSCREEN

2.0 X 0.250
MAKE EMPTY ON BOM

LB9J1
LABEL
1

A19177-001
1375X250_TARGET

MOUNTING HOLES & LABELS

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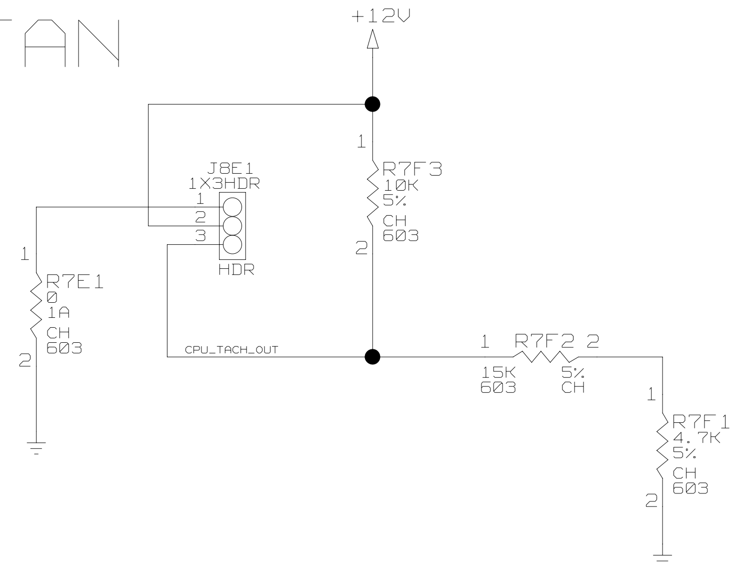
CPU ALWAYS-ON FAN

(PLACE BELOW/RIGHT CPU SOCKET)



REAR CHASSIS FAN

(PLACE ABOVE/RIGHT CPU SOCKET)

44 IN FNT_REAR_FAN_PWM3

VCC

R8G1 1K 5% EMPTY 603

R7G1 5% EMPTY 220 603

VCC

Q8G1 MMBT3904 EMPTY

VCC3

R7H1 1K 5% EMPTY 603

R7G2 0 1A EMPTY 603

R9C1 5% EMPTY 10 603

REAR_FAN_PWM_R

Q9B2 MMBT2222 EMPTY 101416-601

REAR_DRIVER

R9B5 0 1A CH 603

J9B1 1X3HDR HDR

REAR_TACH_OUT

+12V

R9B6 10K 5% CH 603

R9B7 15K 603 5% CH

REAR_FAN_TACH OUT 44

R9B8 4.7K 5% CH 603

VCC3

R2H4 1K 5% EMPTY 603

R2H3 5% EMPTY 10 603

FRONT_FAN_PWM

Q2H1 MMBT2222 EMPTY 101416-601

FRONT_PWM_DRIVER

R2H9 0 1A CH 603

+12V

J2H1 1X3HDR HDR

FRONT_TACH_OUT

+12V

R2H10 10K 5% EMPTY 603

R2H8 15K 603 5% EMPTY

FRONT_FAN_TACH OUT 44

R2H5 4.7K 5% EMPTY 603

(PLACE LOWER LEFT CORNER OF PLATFORM)

CPU & CHASSIS FANS

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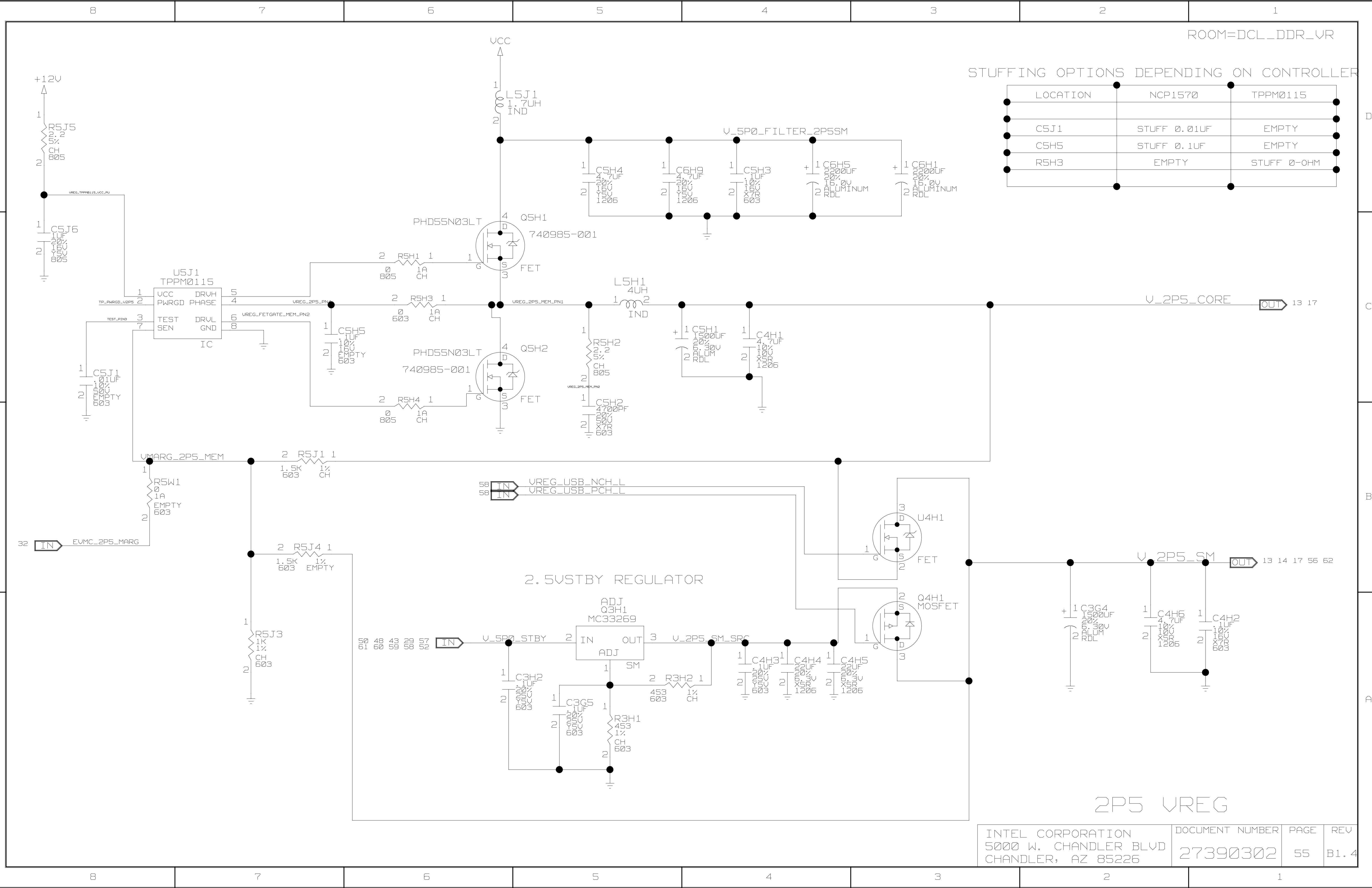

ROOM=DCL_DDR_VR
STUFFING OPTIONS DEPENDING ON CONTROLLER
LOCATION | NCP1570 | TPPM0115
C5J1 | STUFF 0.01UF | EMPTY
C5H5 | STUFF 0.1UF | EMPTY
R5H3 | EMPTY | STUFF 0-OHM
VCC
+12V
V_5P0_FILTER_2P5SM
PHD55N03LT Q5H1 740985-001 FET
PHD55N03LT Q5H2 740985-001 FET
U5J1 TPPM0115
L5H1 4UH IND
V_2P5_CORE
OUT 13 17
VMARG_2P5_MEM
VREG_USB_NCH_L
VREG_USB_PCH_L
EVMC_2P5_MARG
U4H1 FET
Q4H1 MOSFET
V_2P5_SM
OUT 13 14 17 56 62
2.5VSTBY REGULATOR
ADJ Q3H1 MC33269
V_5P0_STBY
V_2P5_SM_SRC
2P5 VREG
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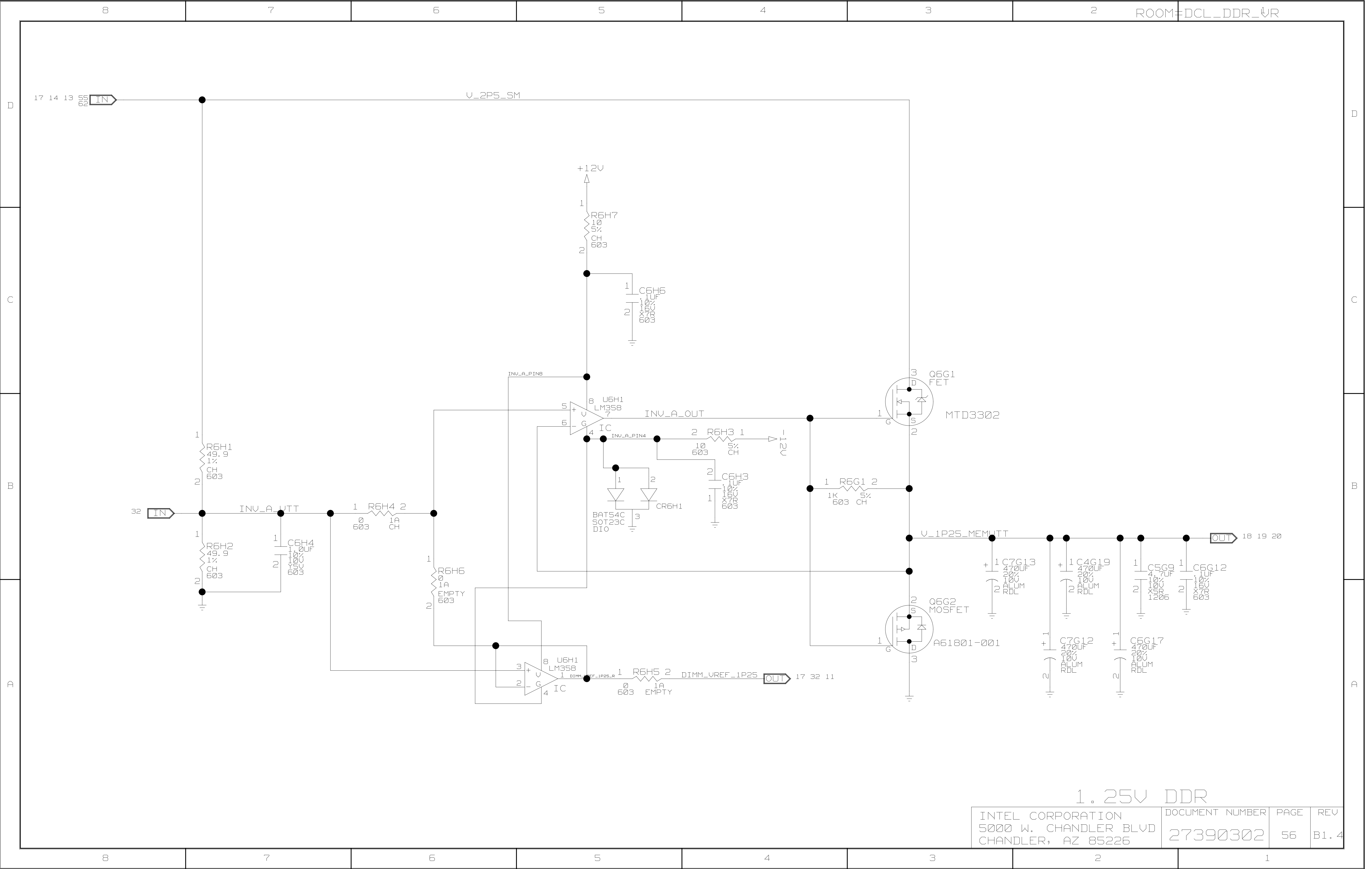

ROOM=DCL_DDR_VR
V_2P5_SM
IN
+12V
R6H7
10
5%
CH
603
C6H6
.1UF
10%
16V
X7R
603
INV_A_PIN8
U6H1
LM358
IC
INV_A_OUT
INV_A_PIN4
R6H3
10
603
5%
CH
-12V
C6H3
.1UF
10%
16V
X7R
603
BAT54C
SOT23C
DIO
CR6H1
Q6G1
FET
MTD3302
R6G1
1K
603
5%
CH
R6H1
49.9
1%
CH
603
INV_A_VTT
R6H4
0
603
1A
CH
R6H2
49.9
1%
CH
603
C6H4
1.0UF
10%
10V
Y5V
603
R6H6
0
1A
EMPTY
603
V_1P25_MEMVTT
OUT
18 19 20
C7G13
470UF
20%
10V
ALUM
RDL
C4G19
470UF
20%
10V
ALUM
RDL
C5G9
4.7UF
10%
10V
X5R
1206
C6G12
.1UF
10%
16V
X7R
603
Q6G2
MOSFET
A61801-001
C7G12
470UF
20%
10V
ALUM
RDL
C6G17
470UF
20%
10V
ALUM
RDL
R6H5
0
603
1A
EMPTY
DIMM_VREF_1P25
OUT
17 32 11
1.25V DDR
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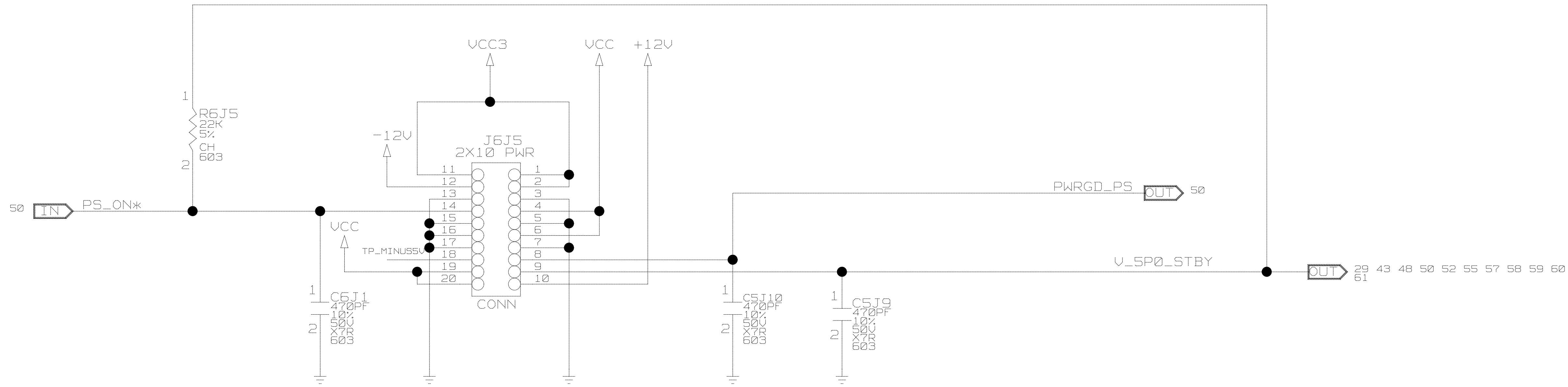

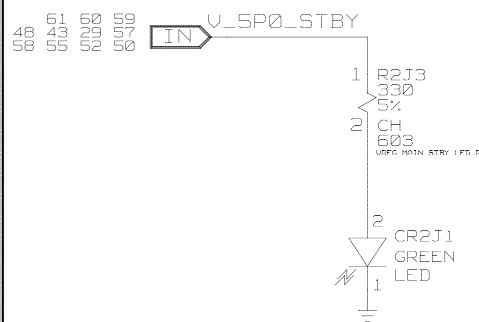

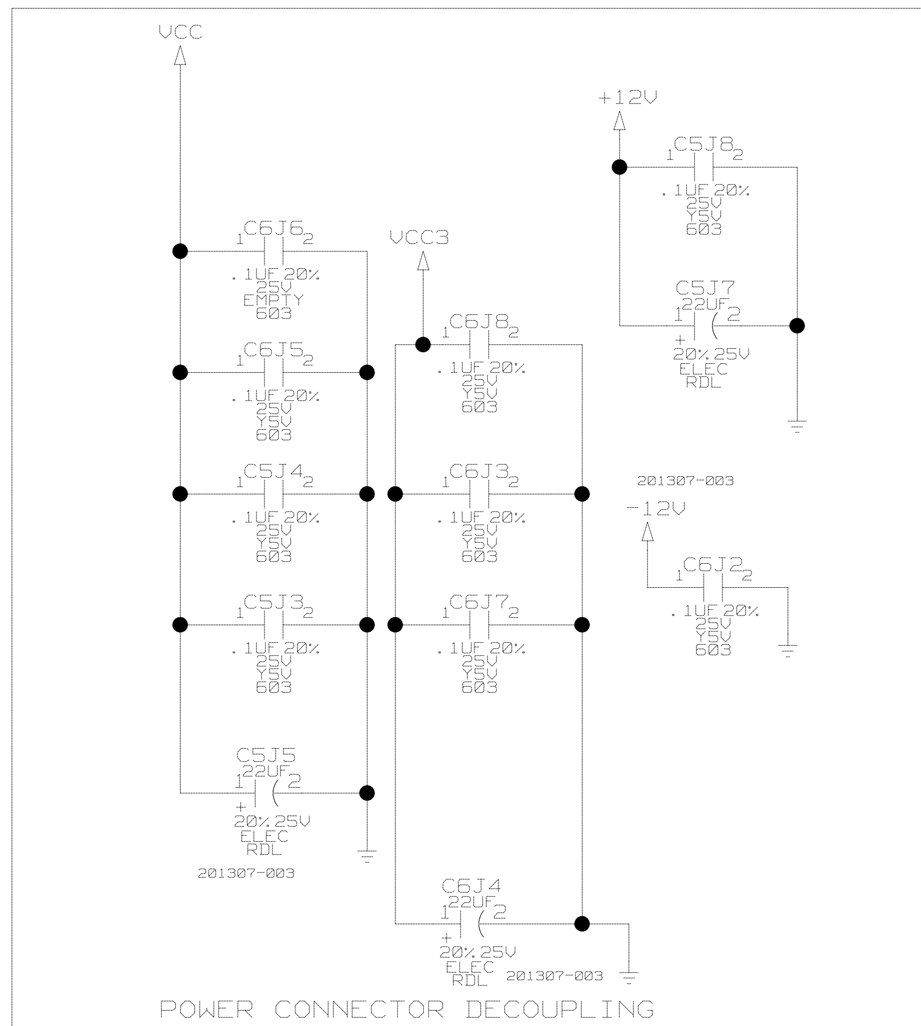

ATX POWER CONNECTOR

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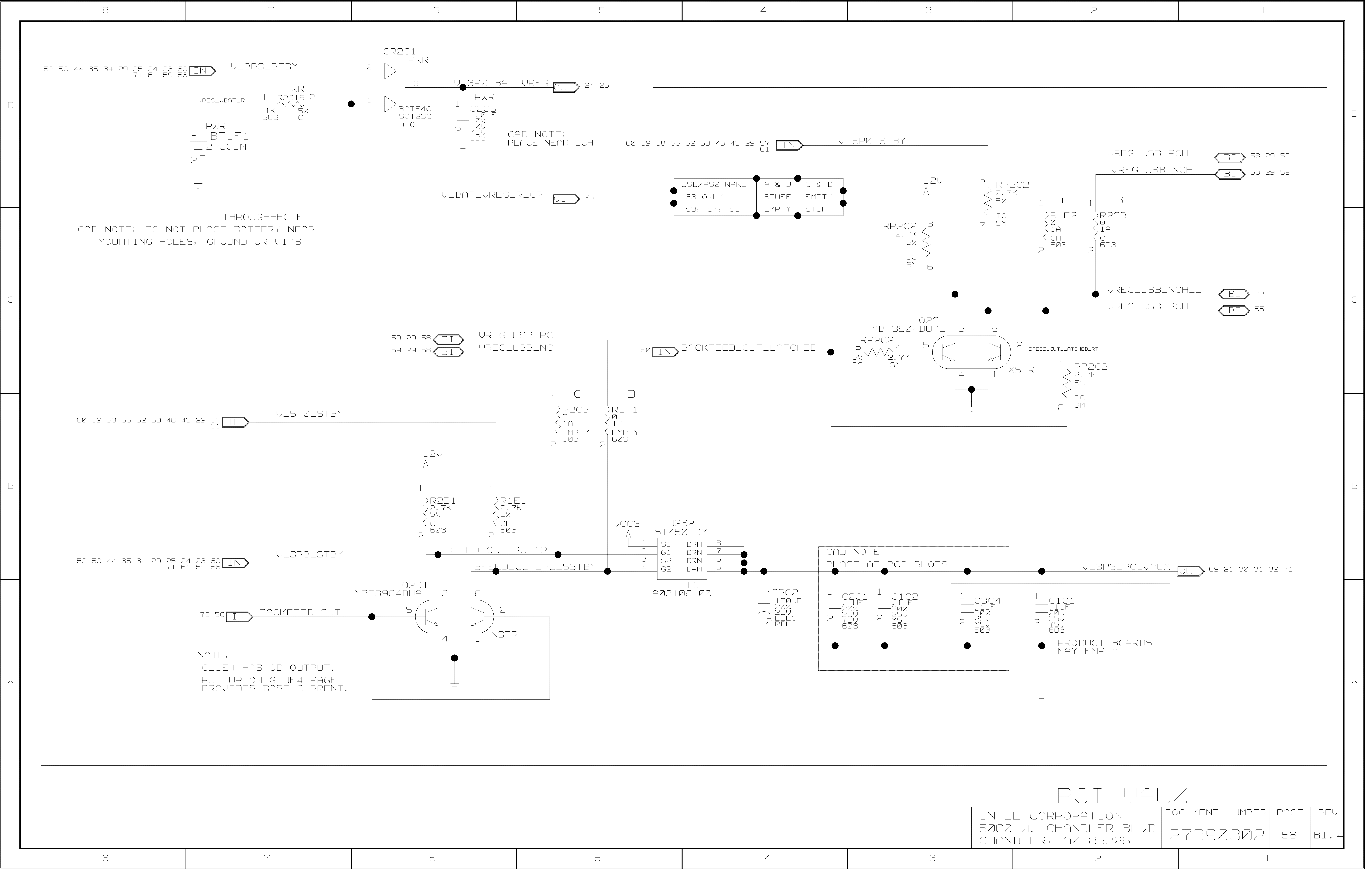
V_3P3_STBY
CR2G1
PWR
BAT54C
SOT23C
DIO
V_3P0_BAT_VREG
PWR
R2G16
1K
603
5%
CH
VREG_VBAT_R
C2G6
1.0UF
10%
10V
Y5V
603
CAD NOTE:
PLACE NEAR ICH
PWR
BT1F1
2PCOIN
V_BAT_VREG_R_CR
THROUGH-HOLE
CAD NOTE: DO NOT PLACE BATTERY NEAR
MOUNTING HOLES, GROUND OR VIAS
V_5P0_STBY
USB/PS2 WAKE
A & B
C & D
S3 ONLY
STUFF
EMPTY
S3, S4, S5
EMPTY
STUFF
VREG_USB_PCH
VREG_USB_NCH
+12V
RP2C2
2.7K
5%
IC
SM
R1F2
R2C3
VREG_USB_NCH_L
VREG_USB_PCH_L
Q2C1
MBT3904DUAL
BACKFEED_CUT_LATCHED
BFEED_CUT_LATCHED_RTN
XSTR
R2C5
R1F1
EMPTY
R2D1
R1E1
VCC3
U2B2
SI4501DY
S1
G1
S2
G2
DRN
BFEED_CUT_PU_12V
BFEED_CUT_PU_5STBY
IC
A03106-001
Q2D1
MBT3904DUAL
BACKFEED_CUT
NOTE:
GLUE4 HAS OD OUTPUT.
PULLUP ON GLUE4 PAGE
PROVIDES BASE CURRENT.
C2C2
100UF
20%
25V
ELEC
RDL
CAD NOTE:
PLACE AT PCI SLOTS
C2C1
C1C2
C3C4
C1C1
.1UF
20%
25V
Y5V
603
PRODUCT BOARDS
MAY EMPTY
V_3P3_PCIVAUX
PCI VAUX
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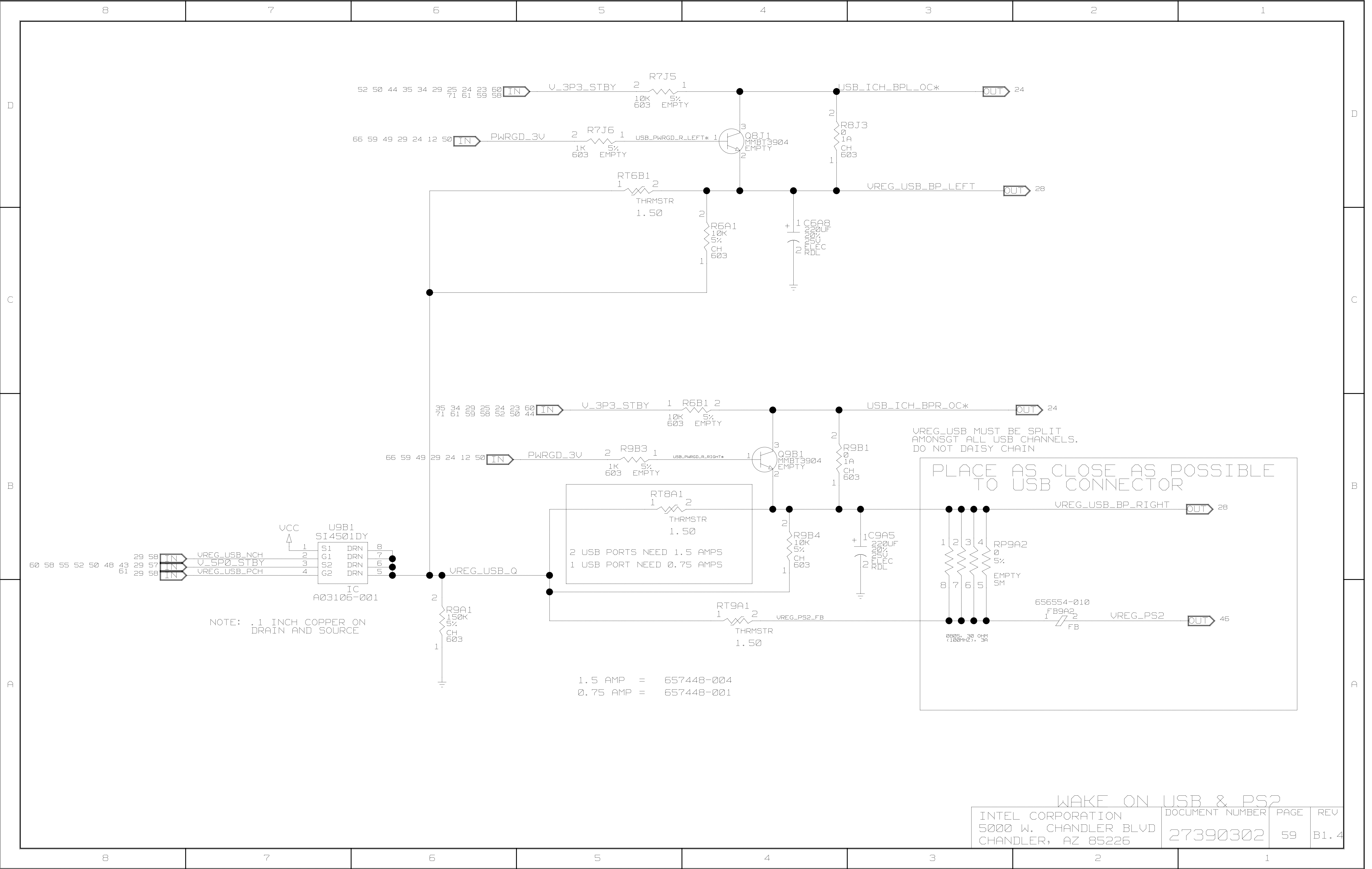

V_3P3_STBY
R7J5
10K 603 5% EMPTY
USB_ICH_BPL_OC*
PWRGD_3V
R7J6
1K 603 5% EMPTY
USB_PWRGD_R_LEFT*
Q8J1 MMBT3904 EMPTY
R8J3 0 1A CH 603
RT6B1 THRMSTR 1.50
R6A1 10K 5% CH 603
C6A8 220UF 20% 25V ELEC RDL
VREG_USB_BP_LEFT
V_3P3_STBY
R6B1
10K 603 5% EMPTY
USB_ICH_BPR_OC*
PWRGD_3V
R9B3
1K 603 5% EMPTY
USB_PWRGD_R_RIGHT*
Q9B1 MMBT3904 EMPTY
R9B1 0 1A CH 603
VREG_USB MUST BE SPLIT
AMONSGT ALL USB CHANNELS.
DO NOT DAISY CHAIN
PLACE AS CLOSE AS POSSIBLE
TO USB CONNECTOR
RT8A1 THRMSTR 1.50
2 USB PORTS NEED 1.5 AMPS
1 USB PORT NEED 0.75 AMPS
R9B4 10K 5% CH 603
C9A5 220UF 20% 25V ELEC RDL
VREG_USB_BP_RIGHT
RP9A2 0 5% EMPTY SM
VCC
U9B1 SI4501DY
VREG_USB_NCH
V_5P0_STBY
VREG_USB_PCH
S1 G1 S2 G2 DRN DRN DRN DRN
IC A03106-001
VREG_USB_Q
R9A1 150K 5% CH 603
RT9A1 THRMSTR 1.50
VREG_PS2_FB
656554-010
FB9A2 FB
0805, 30 OHM (100MHZ), 3A
VREG_PS2
NOTE: .1 INCH COPPER ON
DRAIN AND SOURCE
1.5 AMP = 657448-004
0.75 AMP = 657448-001
WAKE ON USB & PS2
INTEL CORPORATION
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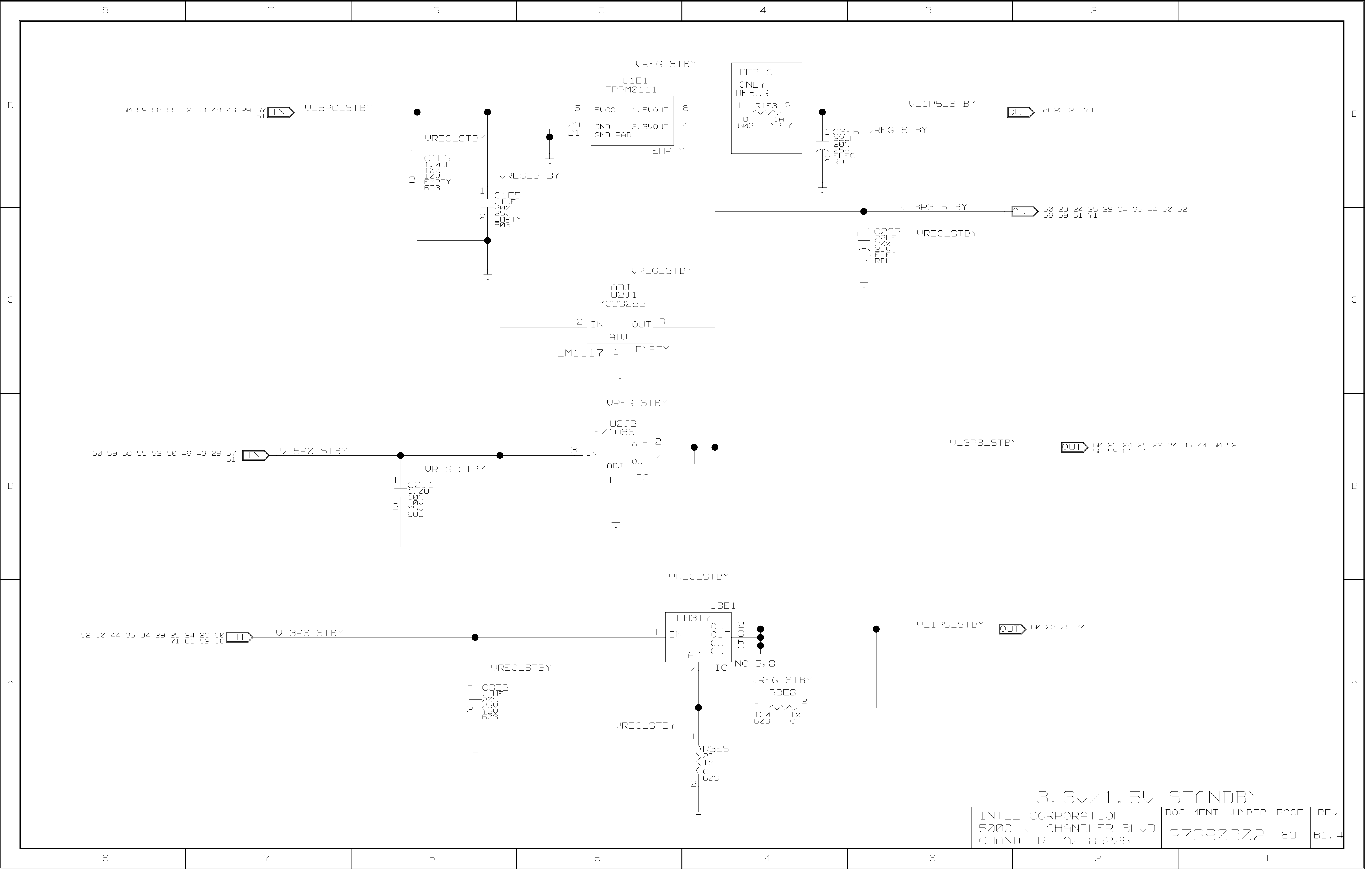

VREG_STBY
U1E1
TPPM0111
V_5P0_STBY
60 59 58 55 52 50 48 43 29 57 61
IN
5VCC
1.5VOUT
GND
3.3VOUT
GND_PAD
EMPTY
C1E6
1.0UF
10%
10V
EMPTY
603
C1E5
.1UF
20%
25V
EMPTY
603
DEBUG
ONLY
DEBUG
R1F3
0
603
1A
EMPTY
V_1P5_STBY
OUT
60 23 25 74
C3E6
22UF
20%
25V
ELEC
RDL
V_3P3_STBY
60 23 24 25 29 34 35 44 50 52
58 59 61 71
C2G5
22UF
20%
25V
ELEC
RDL
ADJ
U2J1
MC33269
IN
OUT
ADJ
LM1117
EMPTY
U2J2
EZ1086
IN
OUT
OUT
ADJ
IC
C2J1
1.0UF
10%
10V
Y5V
603
U3E1
LM317L
52 50 44 35 34 29 25 24 23 60
71 61 59 58
V_3P3_STBY
OUT
ADJ
NC=5,8
C3E2
.1UF
20%
25V
Y5V
603
R3E8
100
603
1%
CH
R3E5
20
1%
CH
603
3.3V/1.5V STANDBY
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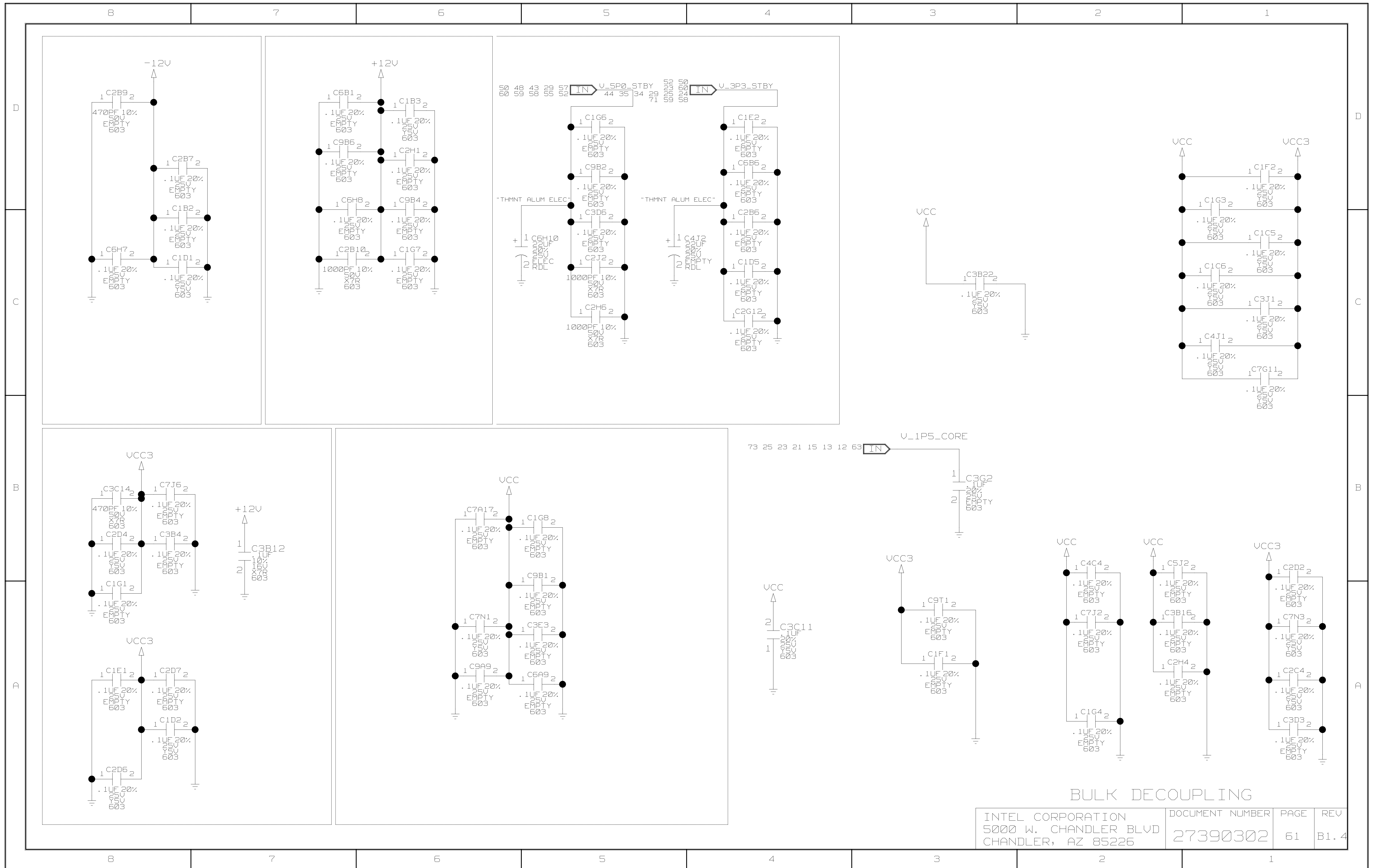
BULK DECOUPLING
INTEL CORPORATION
5000 W. CHANDLER BLVD
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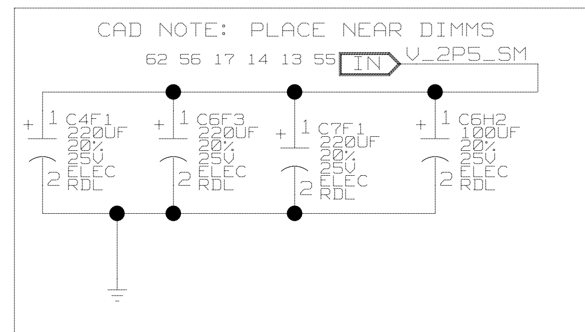
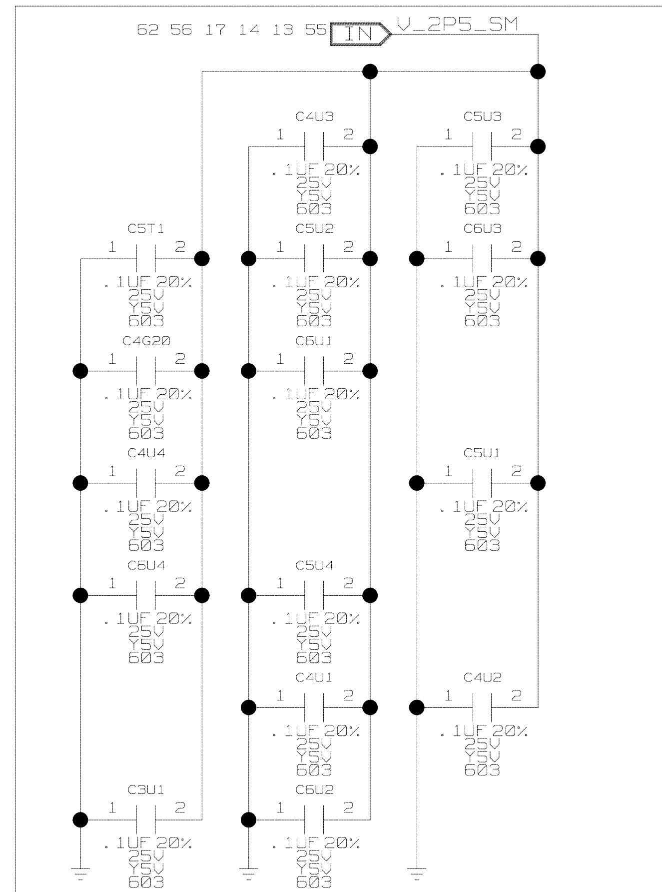
REV
B1.4
V_5P0_STBY
V_3P3_STBY
V_1P5_CORE
"THMNT ALUM ELEC"
-12V
+12V
VCC
VCC3





DDR 2P5 SM DECOUPLING

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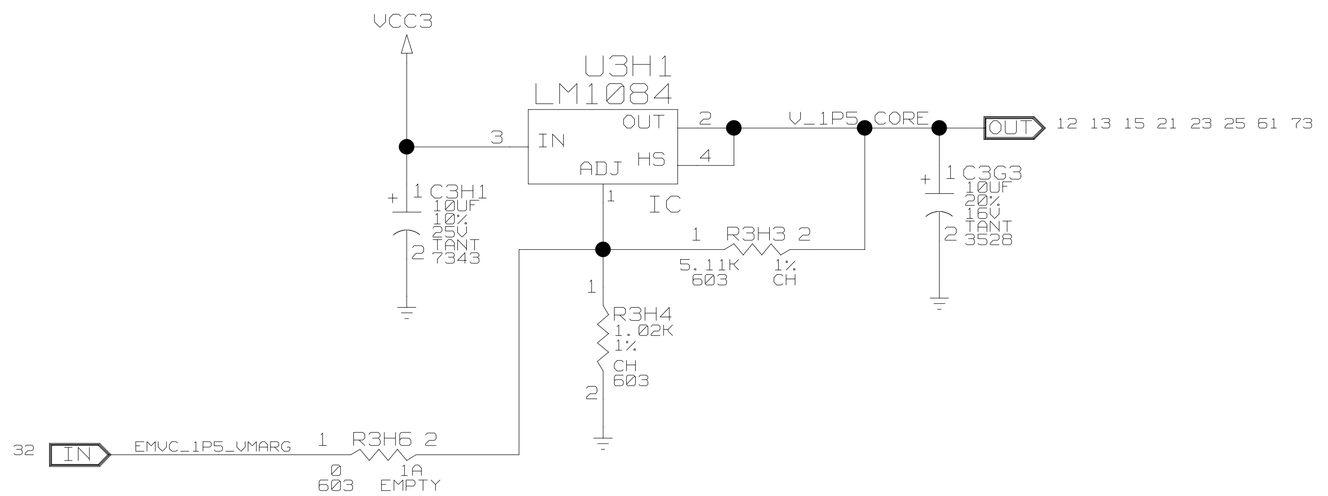

1.5V REGULATOR

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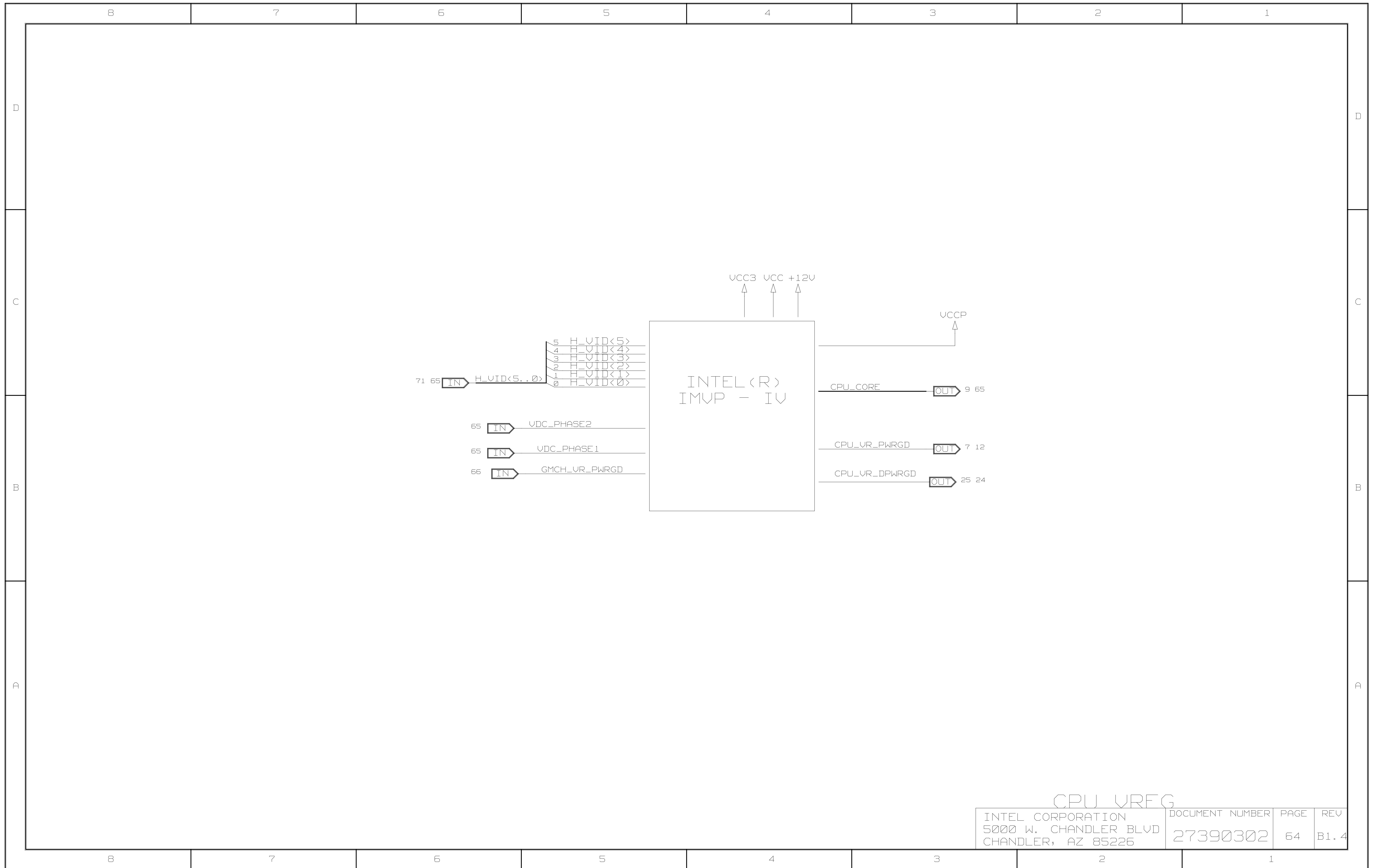

VCC3
VCC
+12V
VCCP
INTEL(R)
IMVP - IV
71 65 IN H_VID<5..0>
5 H_VID<5>
4 H_VID<4>
3 H_VID<3>
2 H_VID<2>
1 H_VID<1>
0 H_VID<0>
65 IN VDC_PHASE2
65 IN VDC_PHASE1
66 IN GMCH_VR_PWRGD
CPU_CORE OUT 9 65
CPU_VR_PWRGD OUT 7 12
CPU_VR_DPWRGD OUT 25 24
CPU VREG
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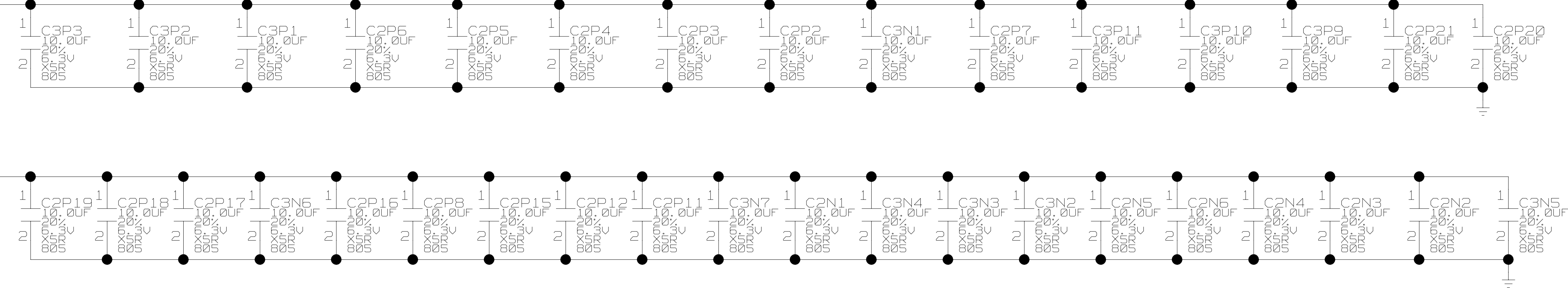
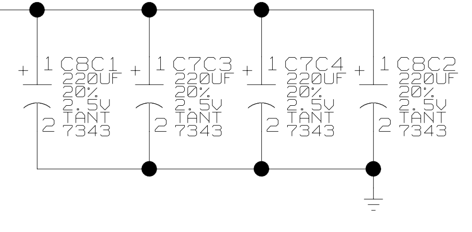
ROOM = DCL_CORE_CPU_VREG

9 64 IN CPU_CORE

MID FREQUENCY CPU DECOUPLING

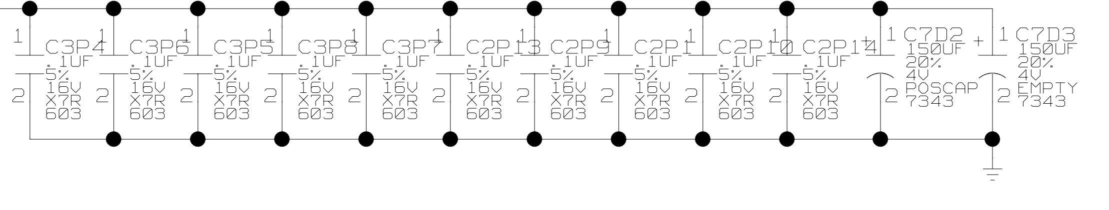


BULK CPU DECOUPLING

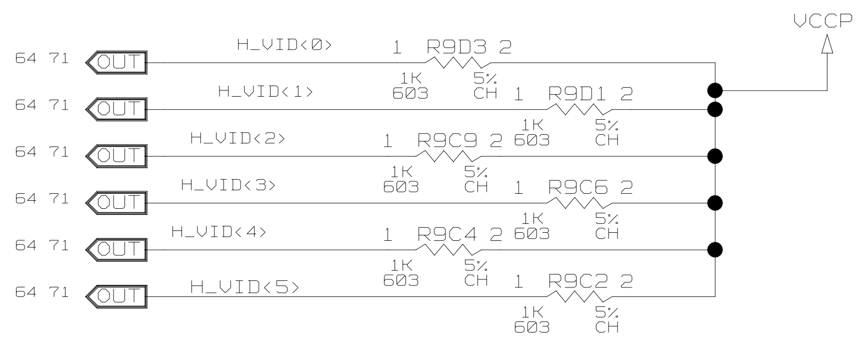


VCCP

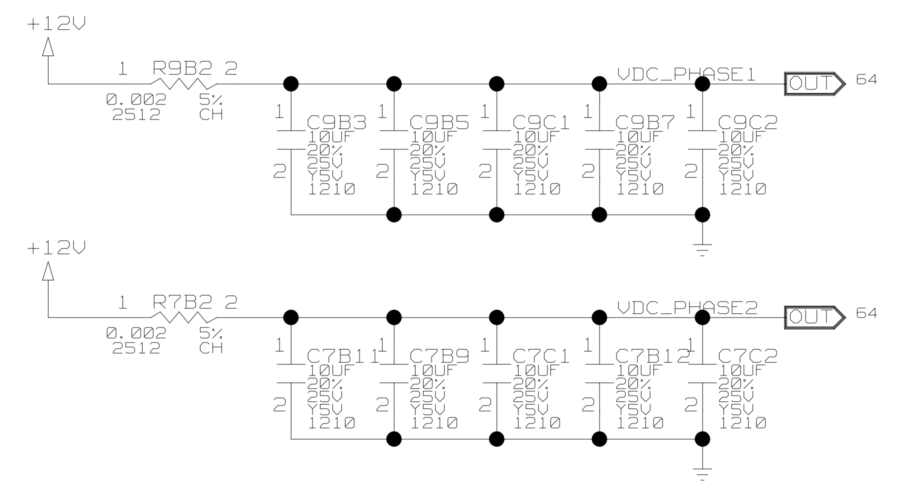
VCCP CPU DECOUPLING



PLACE ON BOTTOM OF CPU UNDER BANIAS SOCKET CAVITY



CPU VR FET DRAIN VOLTAGE



CPU DECOUPLING

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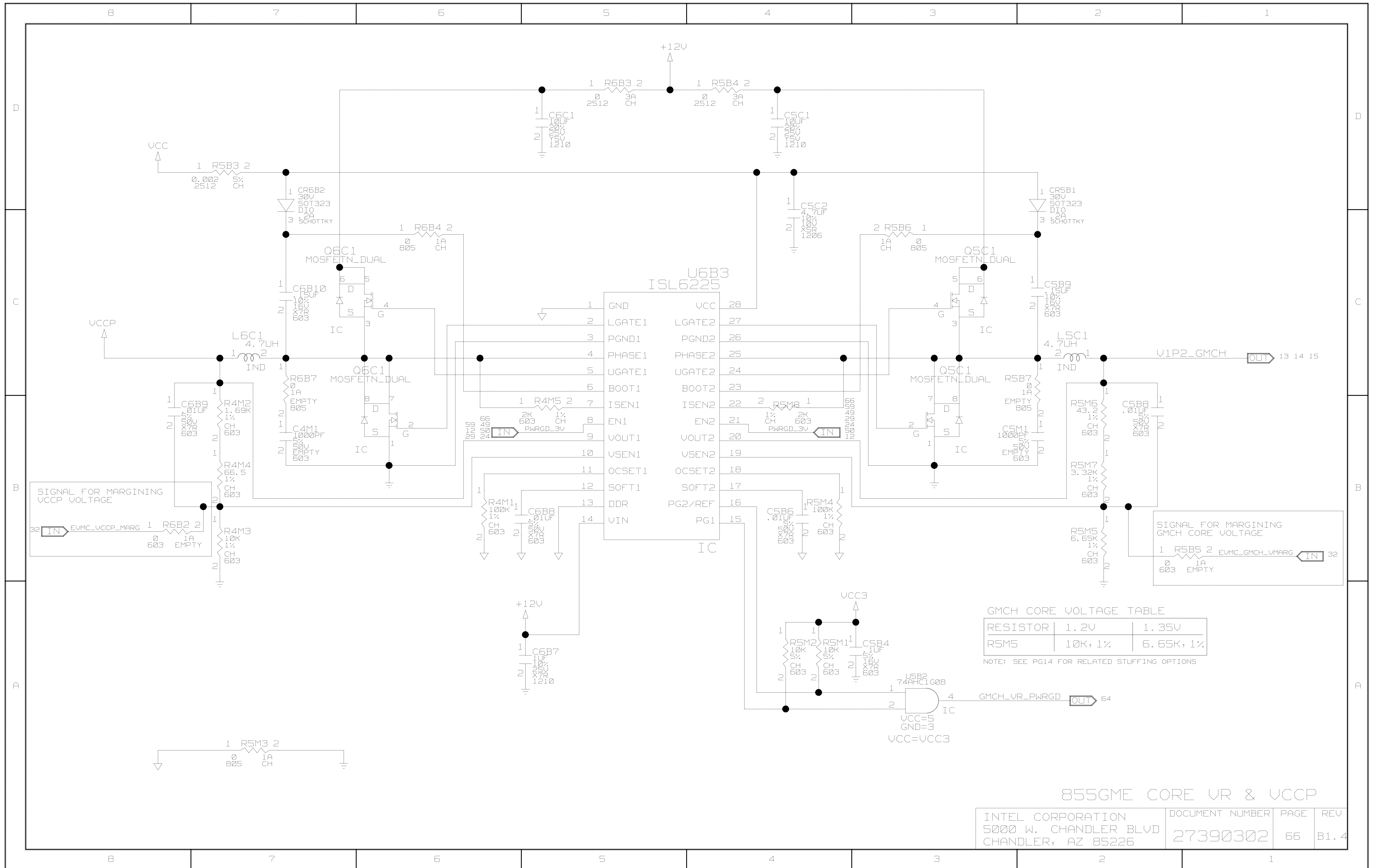
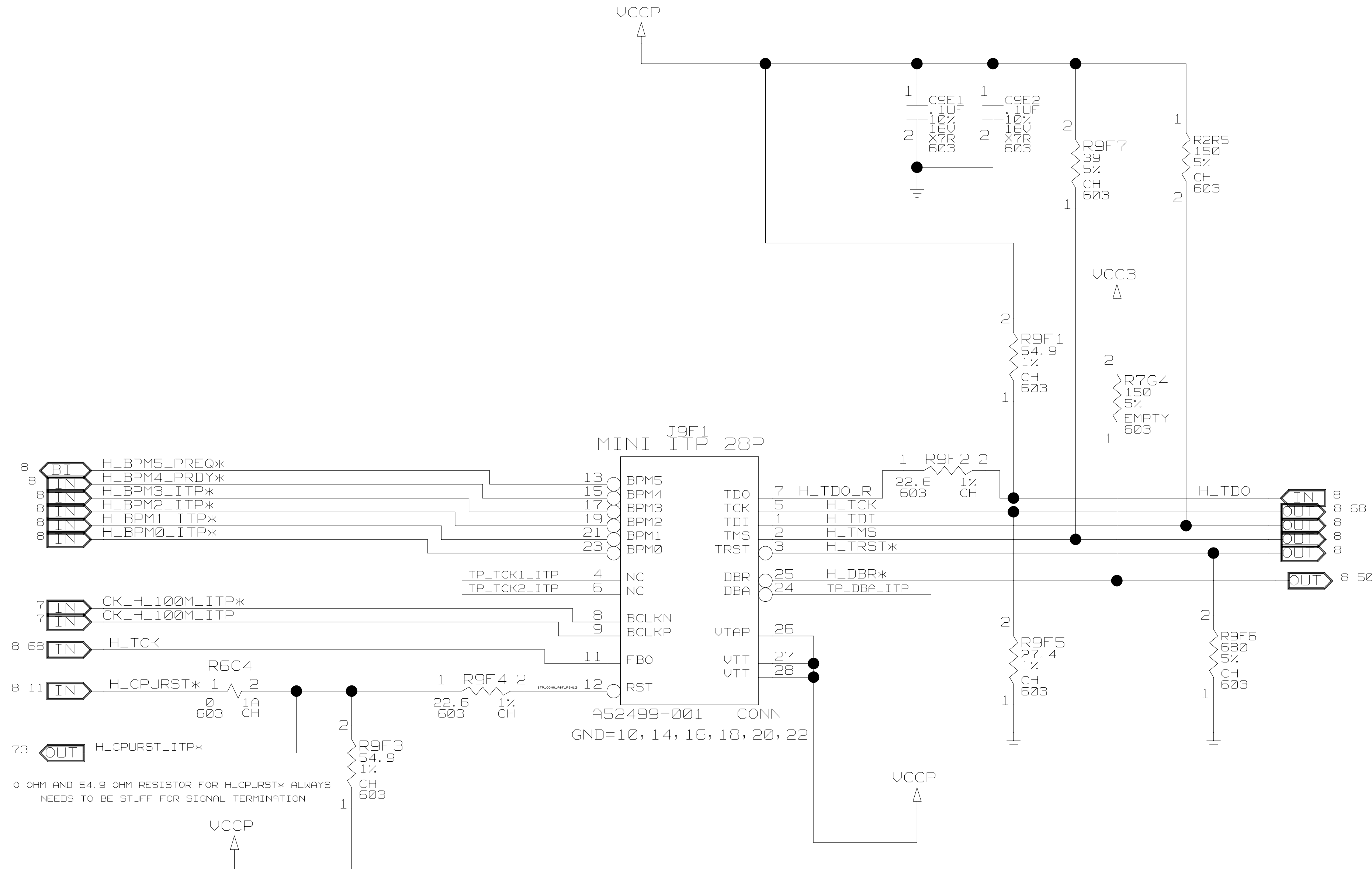


RESISTOR	1.2V	1.35V
R5M5	10K, 1%	6.65K, 1%

DEBUG PAGES



ITP 700FLEX CONNECTOR

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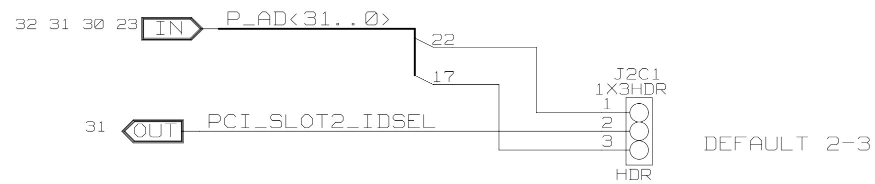
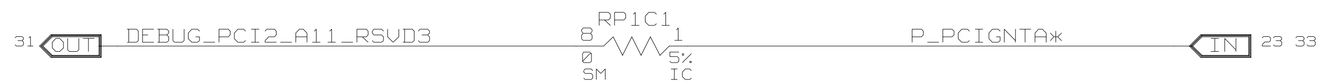
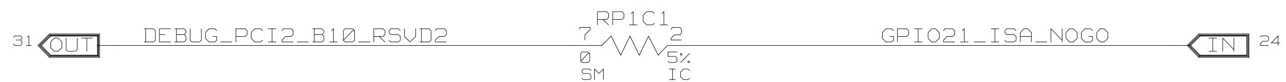
J2B3/J2C1	PCI SLOT 2 MODE
1-2	MOON ISA
2-3	PCI (DEFAULT)







DEBUG HOOKS MOON ISA

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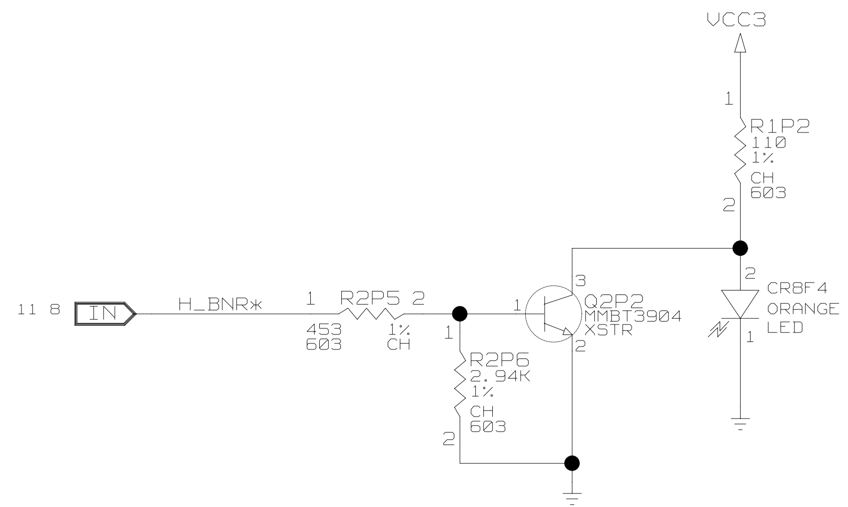

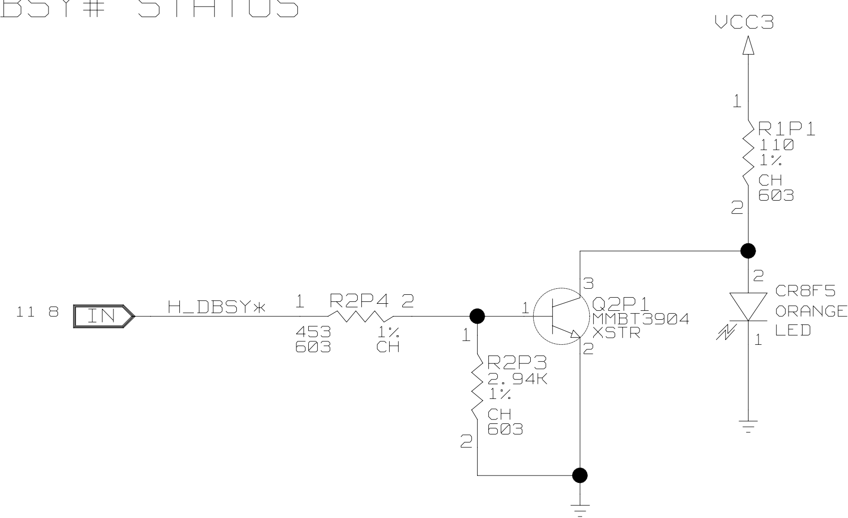

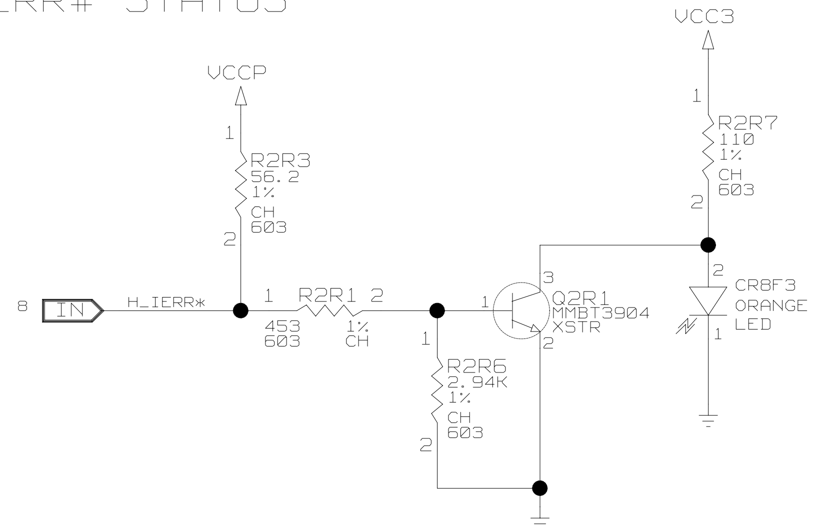

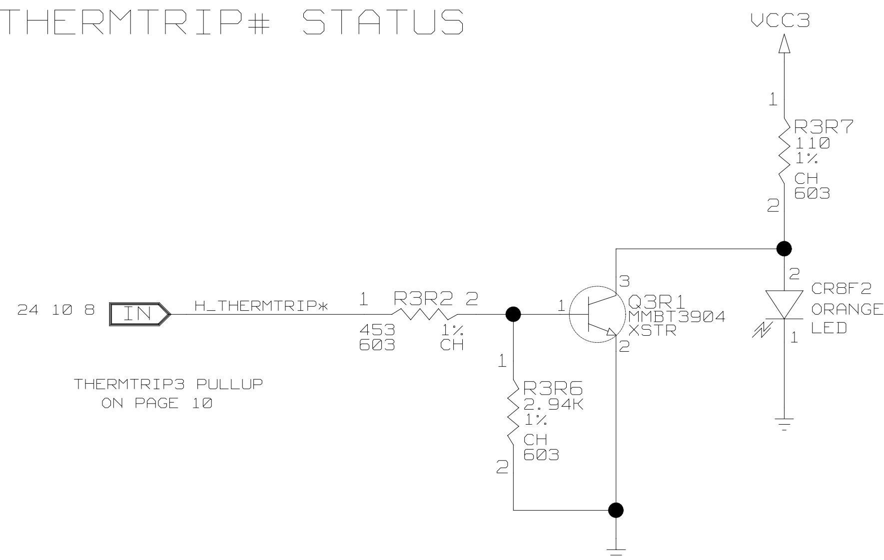

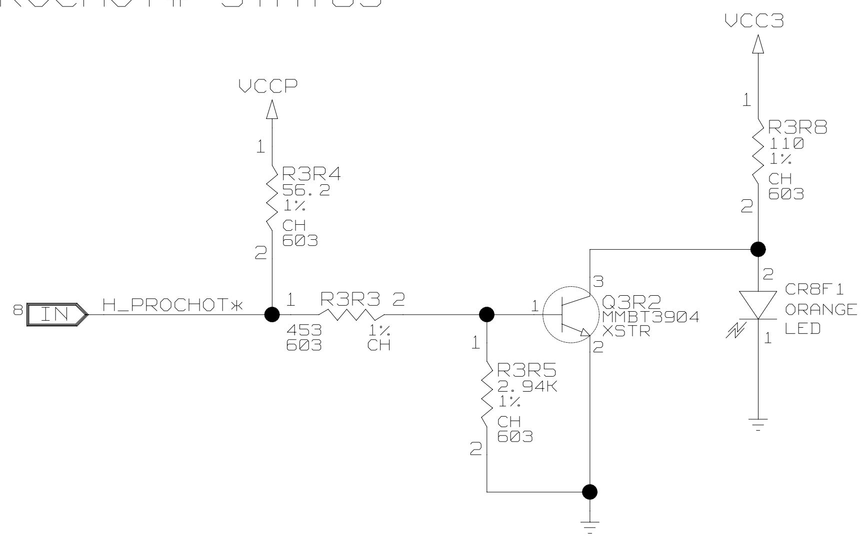

CPU STATUS LEDS

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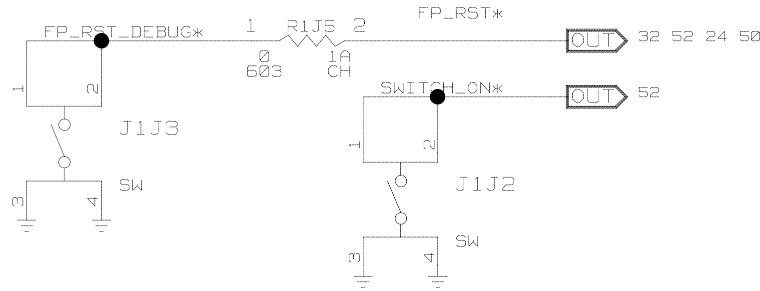
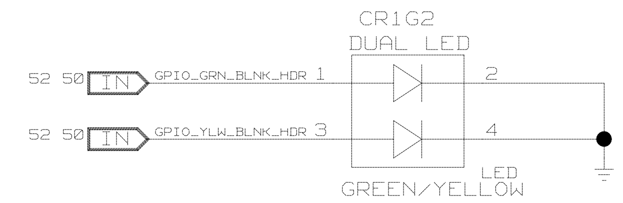
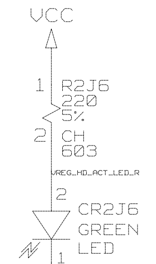
DEBUG/EV FEATURE: FRONT PANEL SWITCHES



VCC
R7J3
330
5%
CH
603
CR7J1
ORANGE
LED
U7J1
74AHCT1G08
50 49 12 25 44 15 72
IN
P_PCIRST*
P_PCIRST_LED*
IC
VCC=5
GND=3

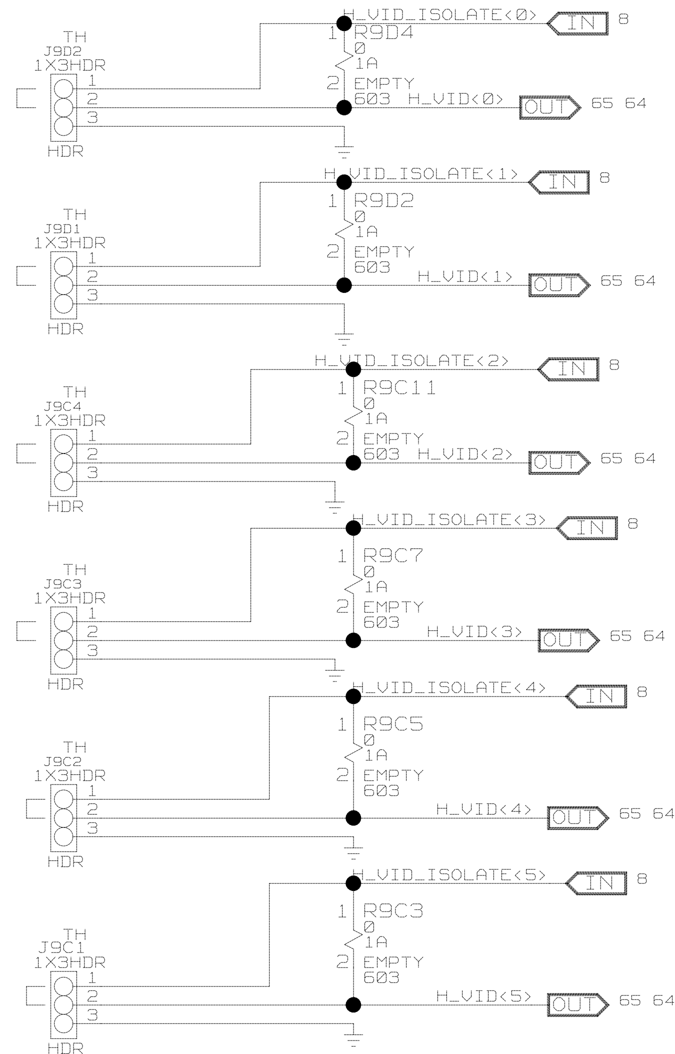
PRODUCT FEATURE: STATUS LED'S





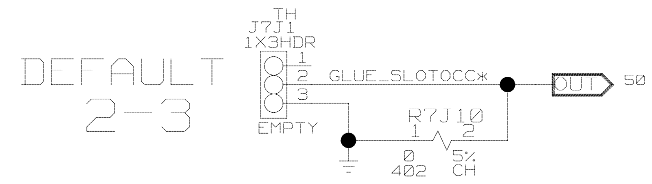
52 50 IN HD_LED*

DEBUG/EV FEATURE: VID JUMPERS

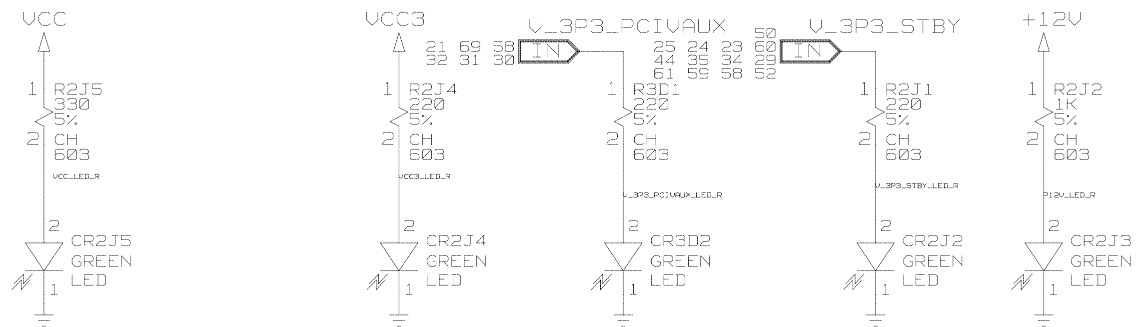


VID 5	4	3	2	1	0	VCORE	VID 5	4	3	2	1	0	VCORE
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

DEBUG/EV FEATURE: POWER-ON FORCING HEADER



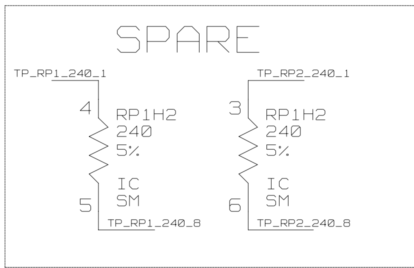
DEBUG/EV FEATURE: POWER RAIL STATUS LED'S



DEBUG STUFFING OPTIONS: BOM=VREG_LED_DEBUG

DEBUG LED DISPLAY

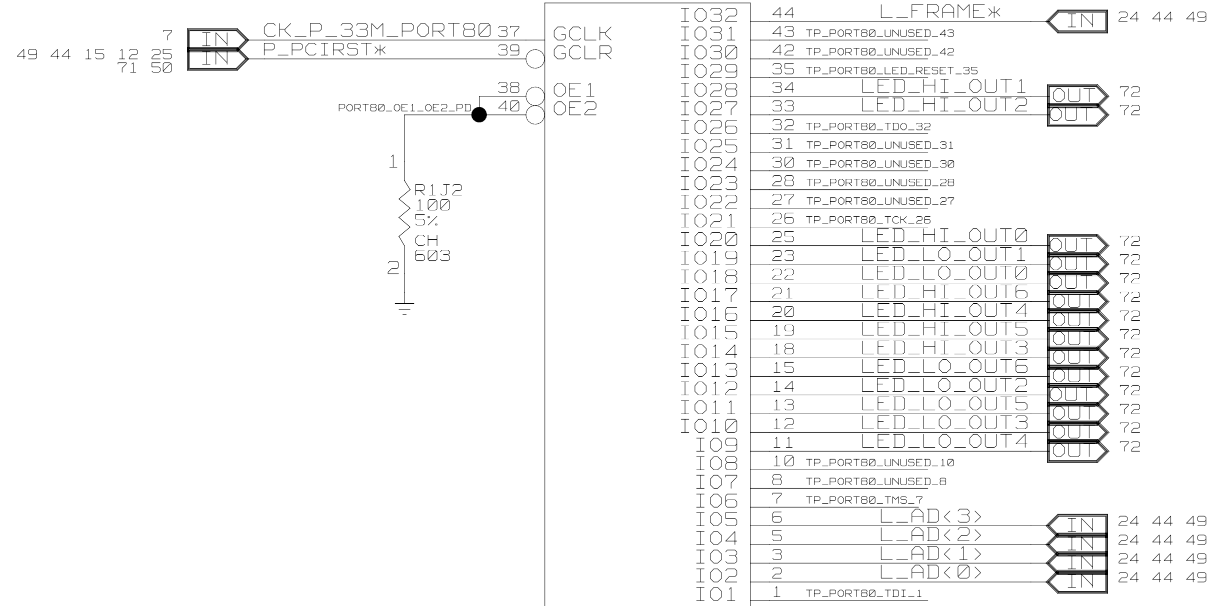
INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	27390302	71	B1.4

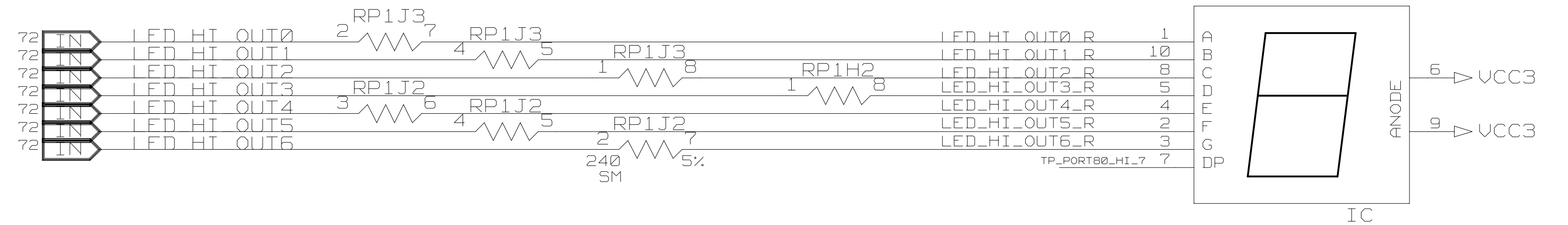


BLANK PART NUMBER: 3.3V COMPATIBLE (IPN XXXXXX-XXX)
PROGRAM FILE FROM D.E.SUBMITTED TO VENDOR
PROGRAM PART NUMBER & PLD-FA: A38794-001

EPM7032AETC44-10
44 PIN TQFP

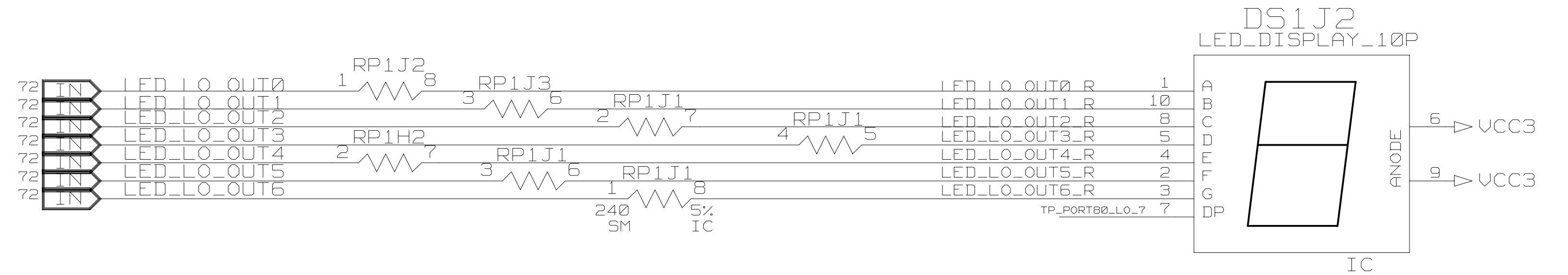
CAD NOTE: ORIENT TO LEFT



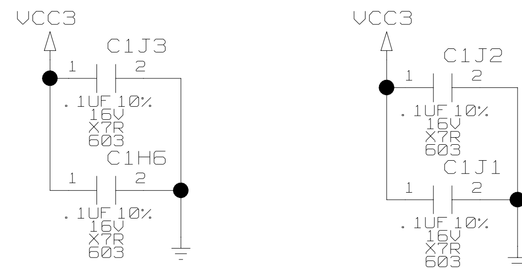


ALL RPACKS 240 OHMS

CAD NOTE: ORIENT TO RIGHT



CAD NOTE: PLACE 1 EACH ON PINS 6 & 9 OF EACH DISPLAY



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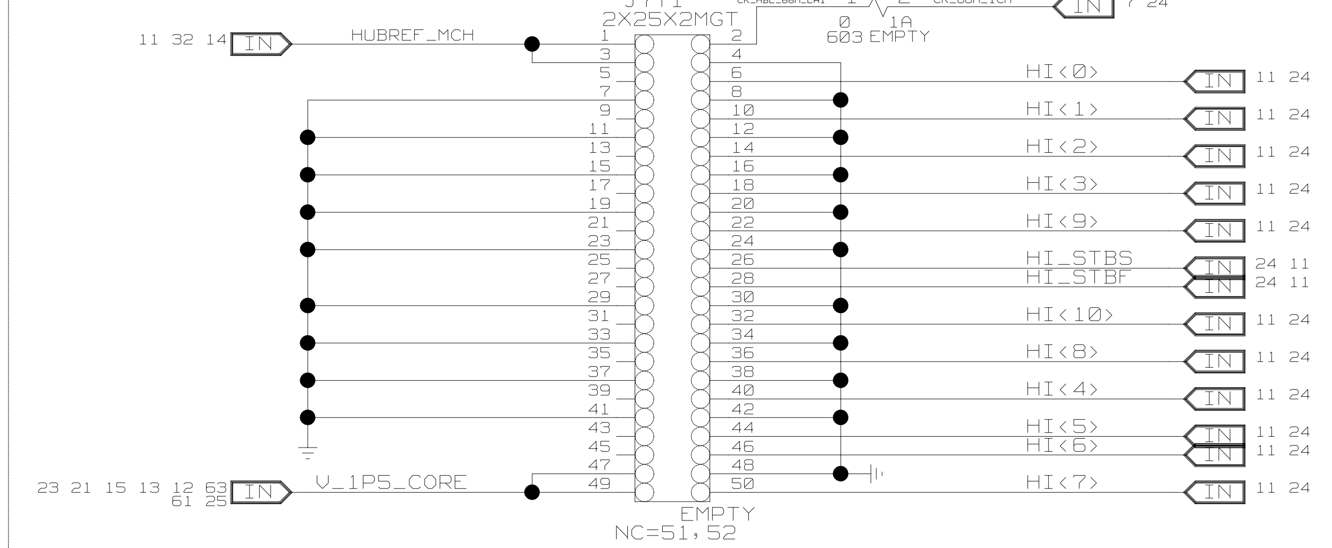
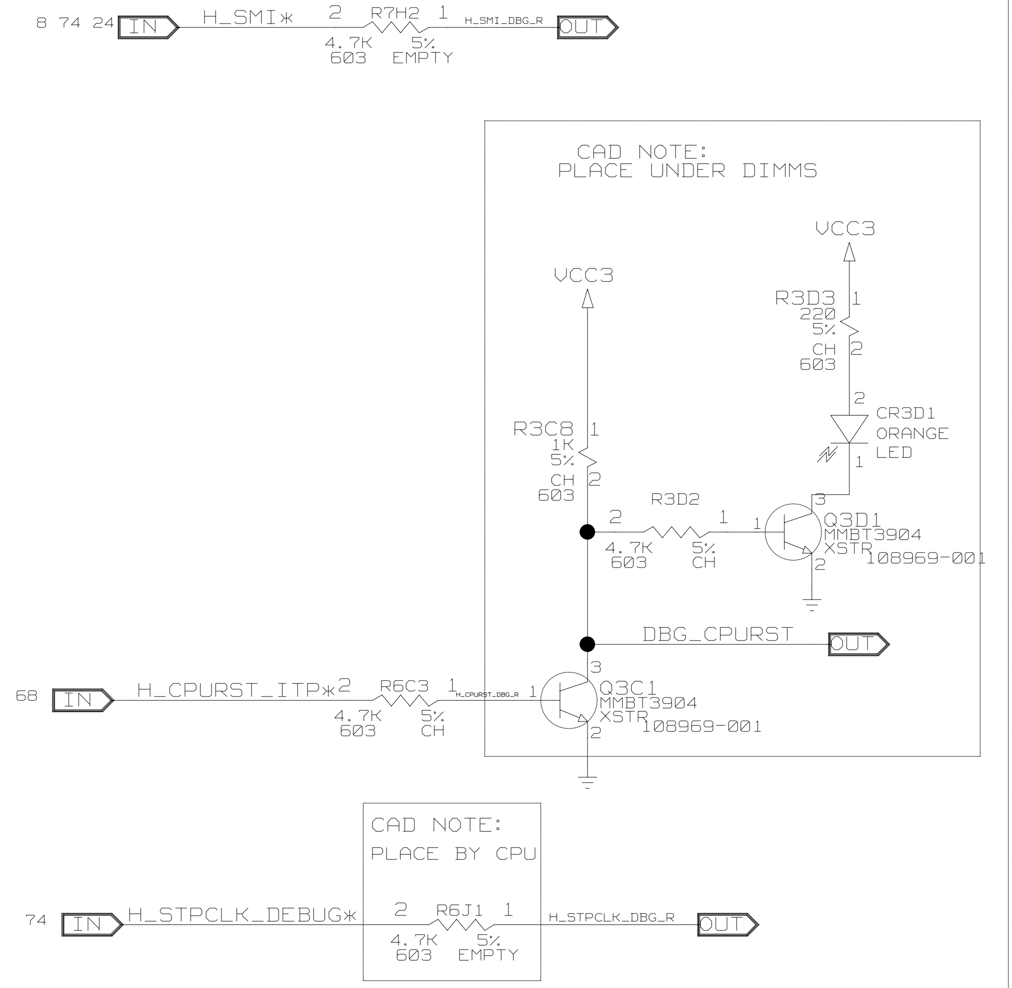
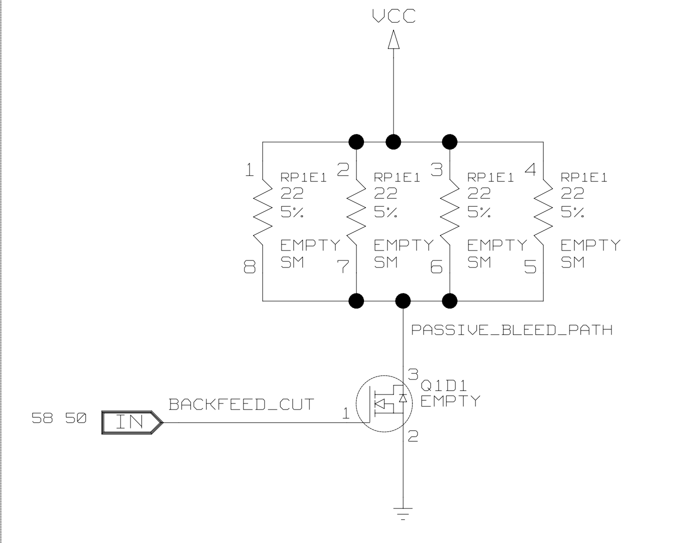
INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	27390302	72	B1.4

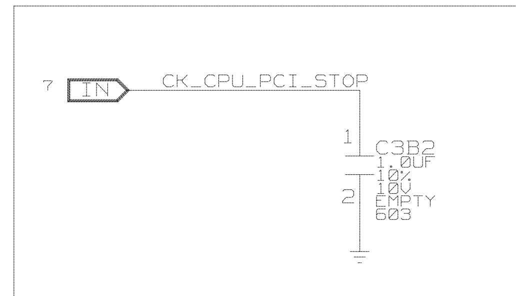


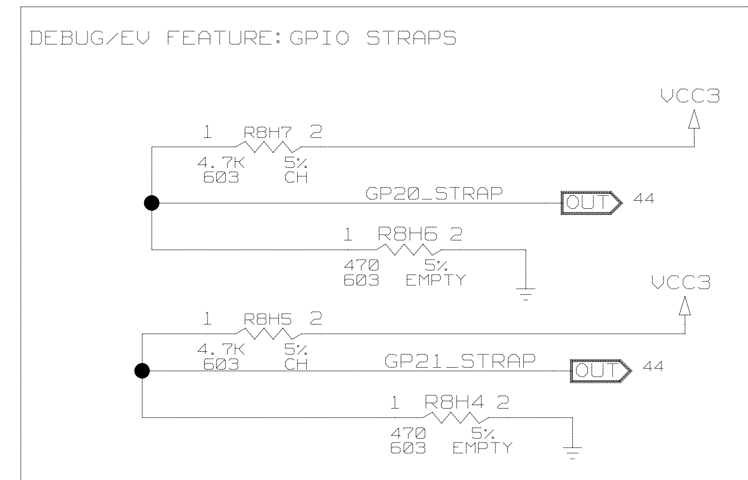


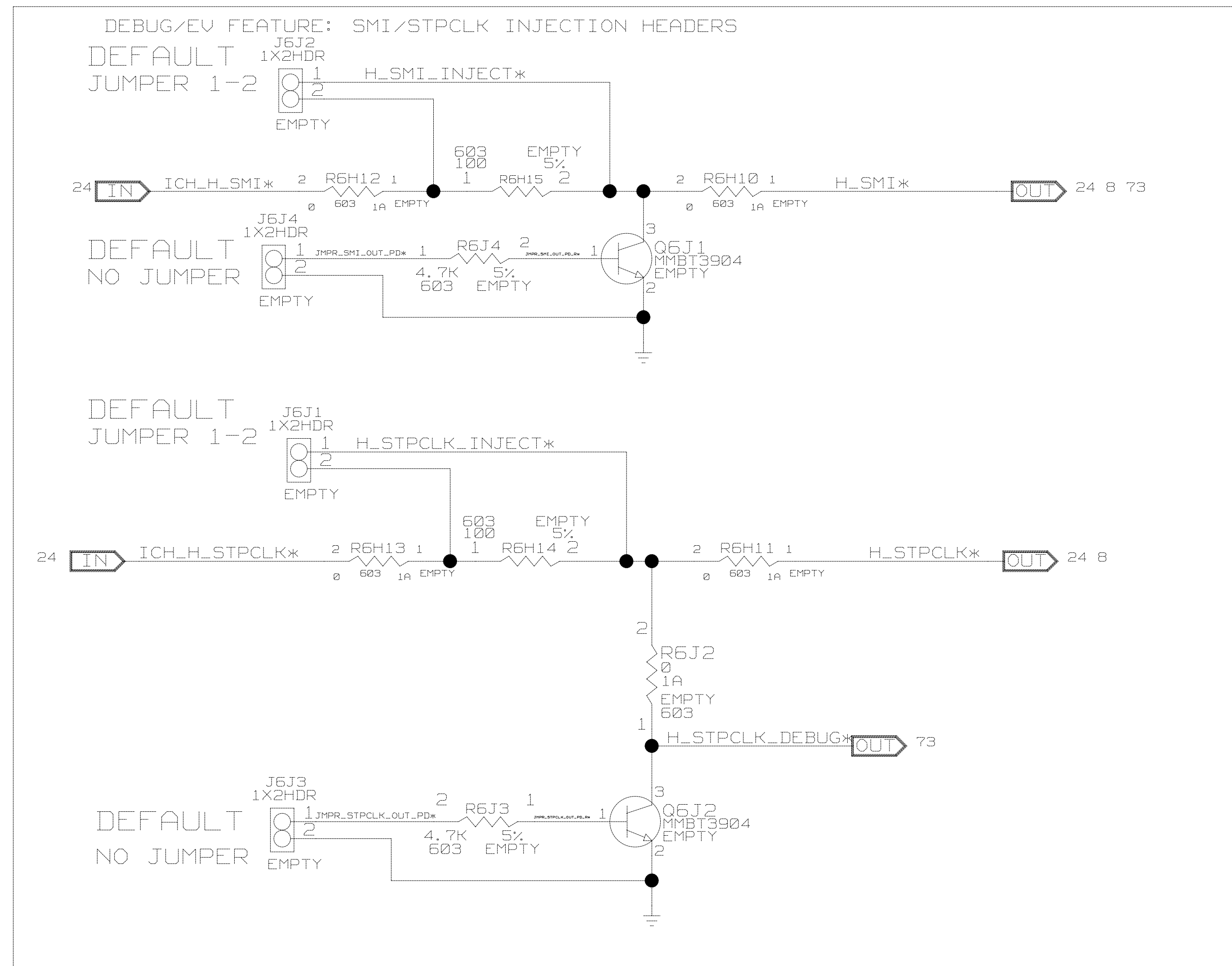


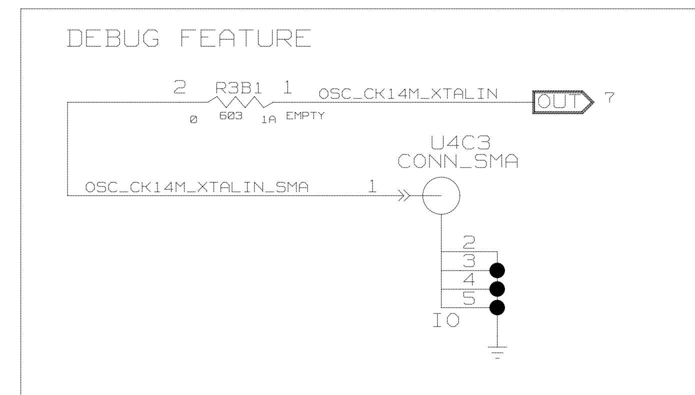
HUBLINK PROBE, TDR COUPONS, LEDS

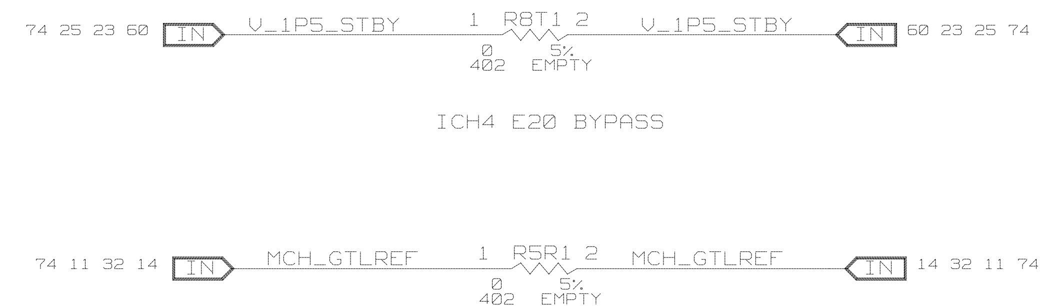
INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	27390302	73	B1.4











DEBUG HEADERS

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	27390302	74	B1.4

REVISION HISTORY

FAB B - REV 1.3

REMOVED UNSUPPORTED SPEED

FAB B - REV 1.4

CHANGED ALL REFERENCES FROM 855GM TO 855GME
PAGE 2 UPDATED BLOCK DIAGRAM TO SHOW AGP 4X ON ADD CONNECTOR
PAGE 2 ADDED INTEL CELERON M PROCESSOR TO CPU BLOCK
PAGE 6 ADDED NOTE TO SHOW V1P2_GMCH NET IS ACTUALLY 1.35 AND 1.2, DEPENDING ON SPEED NEEDED
PAGE 8 REMOVED NS NOTE
PAGE 10 POPULATED PLL CAPS
PAGE 15 UPDATED STRAPPING TABLE

REVISION HISTORY

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	27390302	75	B1.4