Intel® 855GME Chipset and Intel® 6300ESB ICH Embedded Platform

For use with the Intel® Pentium® M Processor, Intel® Pentium® M Processor on 90 nm process with 2 MB L2 cache, and the Intel® Celeron® M Processor

Design Guide

October 2005

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Revision History

Date	Revision	Description
January 2007	006	Updated Table 2., "Reference Documents".
October 2005	005	-Added additional acronyms to the terminology table. -Clarified feature listings to accurately reflect latest supported features and products. -Added descriptions of processors currently supported by the 855GME. -Updated related documents references with current URLs. -Added additional references to reflect document changes/additions. -Revised stackup description in Chapter 3 to make sense. -Fixed control signal to DIMM mapping. -Added clarification on HSYNC/VSYNC isolation requirements. -Added chapter for AGP design guidelines. -Updated Section 6.2 references to 18bit LVDS support. -Cleaned up formatting of Table 50 (LVDS Package Lengths). -Replaced Section 6.3.1 subsections with Table 51 for readability. -Added DVO to AGP pin mapping section (Section 6.3.1.1). -Small consistency changes made throughout the document. -Corrected references to PWRGOOD: Changed table 10 (section 4.1.5) to say AND gate, edited section 4.1.5.4 to remove 6300ESB and replace with AND gate Figure will be updated as well, changed reference to 6300ESB in schematics checklist and layout checklist to AND gate. -Deleted duplicate copy of Intel® 6300ESB power delivery figure in section 4.8. -Added Standby power distribution section for Intel® 6300ESB. -Deleted section 4.8.8 (Intel® 6300ESB power estimates) and added note. -Change decoupling table for Intel® 6300ESB to match DG insert rev 1.6. -Deleted section 4.9 Thermal Design power and added note. -Deleted superfluous transient response background information. -Cleaned up Hub Interface chapter 8 deleted conflicting info etc. -Updated all Intel® 6300ESB information in chapter 9 to match the DG insert rev 1.6: Layout and routing, FWH, GPIO and Power managment. -Updated table 104 with 855GME spec update change (package lengths) from November 2004 revision. -Updated Chapter 12 with all Intel® 6300ESB recommendations to match DG insert rev 1.6. -Updated chapter 13 with all Intel® 6300ESB layout recommendations to match DG insert rev 1.6.
November 2004	004	Updated sections 8 and 11 with new Intel® 6300ESB information.
August 2004	003	Added support for Intel® Pentium® M Low Voltage 738 Processor.
June 2004	002	Updated with support for the Intel® Pentium® M Processor on 90 nm process with 2 MB L2 cache
January 2004	001	Initial public release of this document.

Introduction 1

This design guide provides Intel's design recommendations for systems based on the Intel® Pentium M® Processor, Intel® Pentium® M Processor on 90 nm process with 2 MB L2 cache, or Intel® Celeron M Processor using the Intel® 855GME Chipset and Intel® 6300 ESB I/O Controller Hub. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues.

The Intel reference schematics located at the end of this document may be used as a reference for board designers. While the schematics shall cover specific designs, the core schematics remain the same for most Intel® 855GME/6300ESB I/O Controller Hub chipset platforms.

The Pentium M/Celeron M processor in the 478-pin or 479-BGA package with the Intel 855GME/6300ESB I/O controller hub chipset delivers a high-performance embedded platform solution. The processor and chipset support a 400 MHz source synchronous Pentium M/Celeron M processor system bus using a split-transaction, deferred-reply protocol. Table 1 presents conventions and terminology used in this document.

Note: Unless otherwise noted, all design considerations for the Intel Pentium M Processor may also be used for the Intel Pentium M Processor on 90 nm process with 2 MB L2 cache, or the Intel Celeron M Processor. Refer to the *Intel® Pentium® M Processor Datasheet*, *Intel®* Pentium® M Processor on 90 nm process with 2 MB L2 cache *Datasheet*, and the *Intel® Celeron® M Processor Datasheet* for detailed processor information.

Table 1. Conventions and Terminology (Sheet 1 of 2)

Convention/ Terminology	Definition
AC	Audio Codec
AMC	Audio/Modem Codec
Anti-Etch	Any plane-split, void or cutout in a VCC or GND plane is referred to as an anti-etch
ASF	Alert Standards Format
BER	Bit Error Rate
CMC	Common Mode Choke
CRB	Customer Reference Board
CRT	Cathode Ray Tube
DAC	Digital-to-Analog Converter
DDR	Double Data Rate
DVO	Digital Video Out
EMI	Electro Magnetic Interference
ESD	Electrostatic Discharge
FS	Full Speed – Refers to USB 1.1 Full Speed
FSB	Front Side Bus
FWH	Firmware Hub – A non-volatile memory device used to store the system BIOS
GMCH	Graphics Memory Controller Hub

Table 1. Conventions and Terminology (Sheet 2 of 2)

Convention/ Terminology	Definition
HI	Hub Interface
HS	High Speed – Refers to USB 2.0 High Speed
IDE	Integrated Device Electronics
IMVP	Intel Mobile Voltage Positioning
LCI	LAN Connect Interface
LOM	LAN on Motherboard
LPC	Low Pin Count
LS	Low Speed – Refers to USB 1.0 Low Speed.
LVDS	Low Voltage Differential Signaling - often used to specify a type of digital display output
MC	Modem Codec
PCI	Peripheral Component Interconnect
PCM	Pulse Code Modulation
PLC	Platform LAN Connect
RTC	Real Time Clock
SATA	Serial Advanced Technology Attachment
SDRAM	Synchronous Dynamic Random Access Memory
SMBus	System Management Bus – A two-wire interface through which various system components may communicate.
SPD	Serial Presence Detect
STD	Suspend-To-Disk
STR	Suspend-To-Ram
TCO	Total Cost of Ownership
TDM	Time Division Multiplexed
TDR	Time Domain Reflectometry
UBGA	Micro Ball Grid Array
USB	Universal Serial Bus
VRM	Voltage Regulator Module

1.1 Reference Documents

Table 2 contains a list of reference documents.

Table 2. Reference Documents

Document	Location
Intel® Pentium® M Processor Datasheet	http://www.intel.com/design/mobile/datashts/252612.htm
Intel® Pentium® M Processor Specification Update	http://developer.intel.com/design/intarch/specupdt/252665.htm
Intel® Pentium® M Processor on 90 nm process with 2 MB L2 cache Datasheet	http://developer.intel.com/design/mobile/datashts/302189.htm
Intel® Pentium® M Processor on 90 nm process with 2 MB L2 cache Specification Update	http://developer.intel.com/design/mobile/specupdt/302209.htm
Intel® Pentium® M Processor on 90 nm Process with 2-MB L2 cache for Embedded Applications Thermal Design Guide	http://developer.intel.com/design/intarch/designgd/302231.htm
Intel® Pentium® M Processor and Intel® Celeron® M Processor for Embedded Applications Thermal Design Guide	http://developer.intel.com/design/intarch/designgd/273885.htm
Intel® Celeron® M Processor Datasheet	http://www.intel.com/design/mobile/datashts/300302.htm
Intel® Celeron® M Processor Specification Update	http://developer.intel.com/design/mobile/specupdt/300303.htm
Intel® Celeron® M Processor on 90 nm Process for Embedded Applications Thermal Design Guide	http://developer.intel.com/design/intarch/designgd/305994.htm
Ultra Low Voltage Intel® Celeron® M Processor at 600 MHz Addendum to the Intel® Celeron® M Processor Datasheet	http://www.intel.com/design/intarch/datashts/301753.htm
ULV Intel® Celeron® M Processor at 600 MHz for Embedded Applications Thermal Design Guide	http://developer.intel.com/design/intarch/designgd/302288.htm
Intel® 855GM/855GME Chipset (GMCH) Datasheet	http://www.intel.com/design/chipsets/datashts/252615.htm
Intel® 855GM Chipset Graphics and Memory Controller Hub (GMCH) Specification Update	http://developer.intel.com/design/chipsets/specupdt/253572.htm
Intel® 855GME Chipset Graphics and Memory Controller Hub (GMCH) Specification Update Addendum for Embedded Applications	http://developer.intel.com/design/intarch/specupdt/274004.htm
Intel® 855GME and Intel® 852GM Chipset Memory Controller Hub (MCH) Thermal Design Guide for Embedded Applications	http://developer.intel.com/design/intarch/designgd/273838.htm
Intel® 6300ESB I/O Controller Hub Datasheet	http://developer.intel.com/design/intarch/datashts/300641.htm
Intel® 6300ESB I/O Controller Hub Thermal and Mechanical Design Guide	http://developer.intel.com/design/intarch/designgd/300682.htm
Application Note AP-728: ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions	http://www.intel.com/design/chipsets/applnots/292276.htm
ITP700 Debug Port Design Guide	http://www.intel.com/design/Xeon/guides/249679.htm
JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification	Contact Your Intel Field Representative
Intel® DDR 200/266/333 JEDEC Specification Addendum	http://www.intel.com/technology/memory/ddr/specs/ddr200-266-333_spec_addend_rev1.pdf

System Overview 2

The Intel® 855GME chipset contains a Graphics Memory Controller Hub (GMCH) component for embedded platforms. The GMCH provides the processor interface, system memory interface (DDR SDRAM), hub interface, CRT, LVDS, and a DVO interface. It is optimized for the Intel® Pentium® M processor and the Intel® 6300ESB ICH.

The accelerated hub architecture interface (the chipset component interconnect) is designed into the chipset to provide an efficient, high bandwidth, communication channel between the GMCH and the 6300ESB ICH.

An ACPI-compliant Intel 855GME chipset embedded platform may support the Full-On (S0), Power On Suspend (S1-M), Suspend to RAM (S3), Suspend to Disk (S4), and Soft-Off (S5) power management states. Through the use of an appropriate LAN device, the chipset also supports wake-on LAN for remote administration and troubleshooting. The chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true plug-and-play for the platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC'97* allows the OEM to use software-configurable AC'97 audio and modem coder/decoders (codecs) instead of the traditional ISA devices.

2.1 Terminology

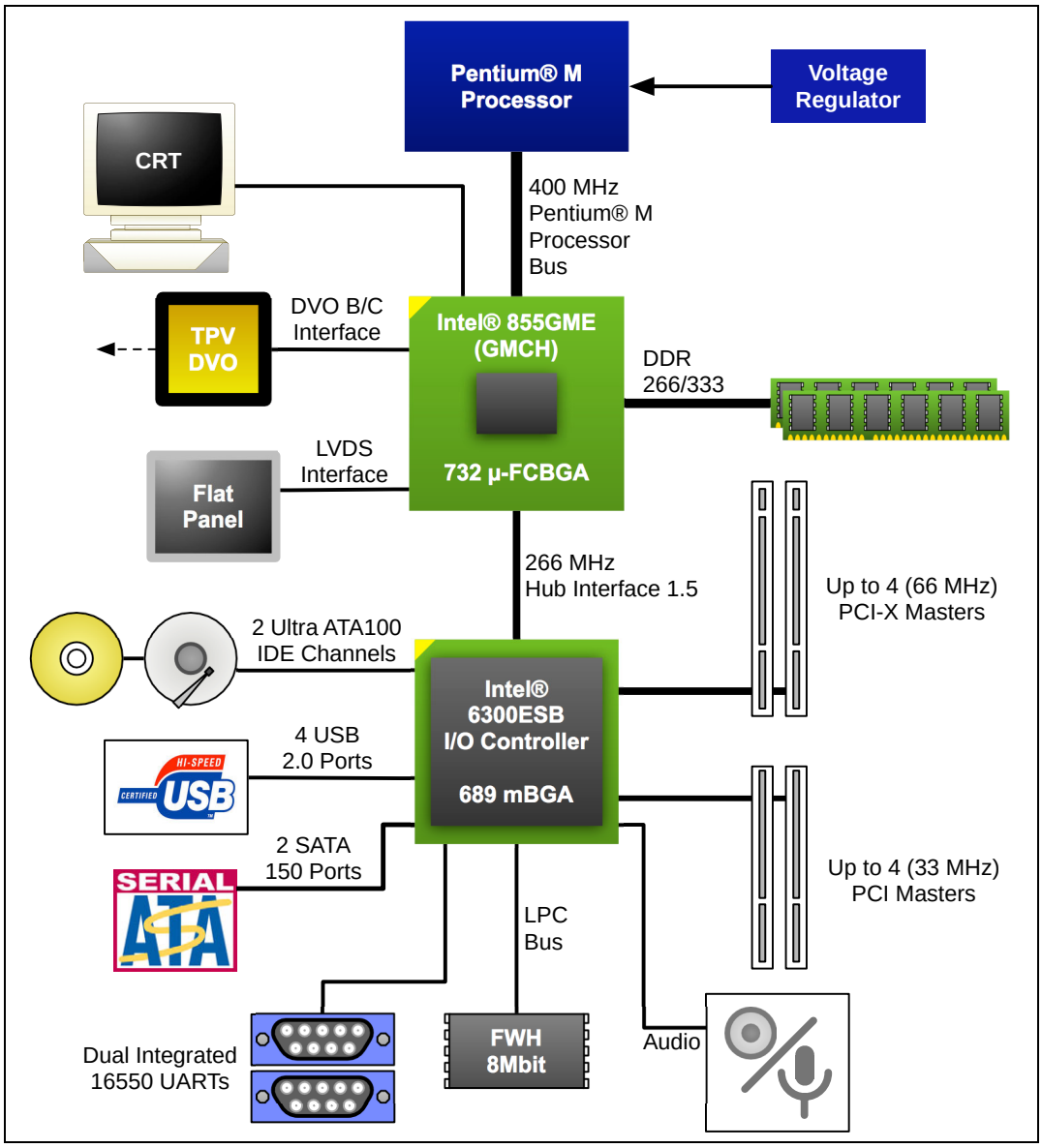
For this document, the following terminology applies.

82855GME	Intel's mobile Graphics Memory Controller Hub.
6300ESB	Intel's ICH southbridge device for embedded and enterprise applications.
Intel® Pentium M Processor	The Intel Pentium M processor or the Intel® Pentium® M processor on 90nm process with 2MB L2 cache

2.2 System Features

The 855GME chipset contains two core components: the GMCH and the 6300ESB ICH. The GMCH integrates a 400 MHz Intel® Pentium® M processor/Celeron® M processor system bus controller, integrated graphics controller interface, integrated LVDS interface, two digital video out ports, a 266/333 MHz DDR-SDRAM controller, and a high-speed accelerated hub architecture interface for communication with the 6300ESB. The 6300ESB integrates an Ultra ATA 100/66/33 controller, USB host controller that supports the USB 1.1 and USB 2.0 specification, LPC interface, FWH Flash BIOS interface controller, PCI interface controller, PCI-X interface controller, two port Serial ATA controller, AC'97 digital controller, two 16550 UART serial ports, and a hub interface for communication with the GMCH. Figure 1 depicts the embedded Intel 855GME chipset system block diagram.

Figure 1. Embedded Intel® 855GME Chipset System Block Diagram



2.3 Component Features

2.3.1 Intel® Pentium® M Processor

2.3.1.1 Architectural Features

- On-die primary 32 Kbyte instruction cache and 32 Kbyte write-back data cache
- On-die 1 Mbyte second level cache
- Supports Streaming SIMD Extensions 2 (SSE2)
- Assisted Gunning Transceiver Logic (AGTL+) bus driver technology
- Enhanced Intel SpeedStep® technology to enable real-time dynamic switching between multiple voltage and frequency points
- Supports host bus Dynamic Bus Inversion (DINV)
- Dynamic power down of data bus buffers
- BPRI# control to disable address/control buffers

2.3.1.2 Packaging/Power

- 478-pin, Micro-FCPGA and 479-ball Micro-FCBGA packages
- VCC-CORE for Intel® Pentium® M Processor at 1.6GHz: 1.484 V (highest frequency mode) to 0.956 V (lowest frequency mode); VCCA (1.8 V); VCCP (1.05 V)
- VCC-CORE for Low Voltage Intel® Pentium® M Processor at 1.1 GHz: 1.180 V (highest frequency mode) to 0.956 V (lowest frequency mode); VCCA (1.8 V); VCCP (1.05 V)
- TDP: 24.5 W for the Intel® Pentium® M Processor at 1.6 GHz
- TDP: 12 W for the Low Voltage Intel® Pentium® M Processor at 1.1 GHz

2.3.2 Intel® Pentium® M Processor on 90 nm Process with 2 MB L2 Cache

All features of the Intel Pentium M processor are supported by the Intel Pentium M Processor on the 90 nm process with 2 MB L2 cache. The processors also utilize the same package and footprint. This section only lists the additional on-die enhancements. For more details, see the *Intel Pentium M Processor on 90nm Process with 2 MB L2 Cache Datasheet*.

New features on the Intel Pentium M Processor on the 90nm process with 2MB L2 cache include:

- On-die 2-MB L2 cache
- Strained silicon process technology

Voltage and Power Changes:

- Intel® Pentium® M Processor 745 (90 nm, 2 MB L2 Cache, 1.8 GHz, 400 MHz FSB):
  - $V_{CC\text{-}CORE\ (HFM)}$: 1.276 V – 1.340 V
  - $V_{CC\text{-}CORE\ (LFM)}$: 0.988 V
  - V_{CCA}: 1.8 V only
  - TDP: 21 W

- Intel® Pentium® M Processor Low Voltage 738 (90 nm, 2 MB L2 Cache, 1.4 GHz, 400 MHz FSB):
  - $V_{CC\text{-}CORE\ (HFM)}$: 1.052 V
  - $V_{CC\text{-}CORE\ (LFM)}$: 0.956 V
  - V_{CCA}: 1.8 V and 1.5 V supported
  - TDP: 10 W

2.3.3 Intel® Celeron® M Processor

Most features of the Intel Pentium M processor are supported by the Intel Celeron M Processor. For more details, see the *Intel® Celeron® M Processor Datasheet.*

Processor Features

- Pin-compatible with the Intel® Pentium® M processor.
- 1.3 GHz operation, available in 478-pin micro FCPGA and 479-ball micro FCBGA packages
- On-die 512-KB second level cache
- Voltage/Power Changes
  - VCC-CORE for 1.3 GHz: 1.356V
  - TDP for 1.3 GHz = 24.5 W
- No support for Enhanced Intel SpeedStep® Technology, Deeper Sleep operation, or Intel® Thermal Monitor 2.

2.3.4 Intel® Celeron® M Processor on 90 nm process

Most features of the Intel Pentium M processor on 90 nm process with 2 MB L2 cache are supported by the Intel Celeron M processor on 90nm process. For more details, see the *Intel® Celeron® M Processor Datasheet on 90 nm process Datasheet.*

- Intel® Celeron® M Processor 370 (90 nm, 1.5 GHz, 400 MHz FSB):
  - On-die 1-MB L2 Cache
  - TDP = 21 W
  - V_{CCA}: 1.8 V and 1.5 V supported only
- Intel® Celeron® M Processor Ultra Low Voltage 373 (90 nm, 1.0 GHz, 400 MHz FSB):
  - On-die 512-KB L2 Cache
  - TDP = 5.5 W
  - V_{CCA}: 1.8 V and 1.5 V supported

2.3.5 ULV Intel® Celeron® M Processor at 600 MHz

Most features of the Intel Celeron M processor are supported by the ULV Intel Celeron M at 600 MHz processor. For more details, see the *Ultra Low Voltage Intel® Celeron® M Processor at 600 MHz Addendum to the Intel® Celeron® M Processor Datasheet.*

- Intel® Celeron® M Processor Ultra Low Voltage at 600 MHz (130 nm, 600 MHz, 400 MHz FSB):
  - On-die 512-KB L2 Cache
  - TDP = 7 W
  - VCC-CORE: 1.004 V
  - V_{CCA}: 1.8 V supported
  - 479-ball micro FCBGA package

2.3.6 Intel® 855GME Chipset Graphics Memory Controller Hub (82855GME)

2.3.6.1 Intel® Pentium® M Processor/Intel® Celeron® M Processor Support

- Optimized for the Pentium M processor/Celeron M processor in 478-pin micro-FCPGA and 479-ball micro-FCBGA package
- AGTL+ bus driver technology with integrated GTL termination resistors (gated AGTL+ receivers for reduced power)
- Supports 32-bit AGTL+ bus addressing (no support for 36-bit address extension).
- Supports Uni-processor (UP) systems.
- 400 MT/s Pentium M processor FSB support (100 MHz)
- 2X Address, 4X Data
- 12 deep in-order queue

2.3.6.2 Integrated System Memory DRAM Controller

- Supports up to two double-sided DIMMs (four rows populated) with unbuffered PC2100/ PC2700 DDR-SDRAM (with or without ECC)
- Supports 64 Mbit, 128 Mbit, 256 Mbit and 512 Mbit technologies for x8 and x16 width devices
- Maximum of 2 Gbytes system memory by using 512 Mbit technology devices (double sided)
- Supports 266 MHz, and 333 MHz DDR devices
- 64-bit data interface (72-bit with ECC)
- 2100/2700 system memory interface
- Supports up to 16 simultaneous open pages

2.3.6.3 Internal Graphics Controller

- Graphics Core Frequency
  - Display/Render frequency up to 250 MHz (with 1.35 V core voltage)
- 3D Graphics Engine
  - 3D Setup and Render Engine

  - — Zone Rendering
  - — High quality performance Texture Engine
- Analog Display Support
  - — 350-MHz integrated 24-bit RAMDAC
  - — Hardware color cursor support
  - — Accompanying I2C and DDC channels provided through multiplexed interface
  - — Dual independent pipe for dual independent display
  - — Simultaneous display: same images and native display timings on each display device
- Digital Video Out Port (DVOB & DVOC) support
  - — DVOB & DVOC with 165-MHz dot clock support for each 12-bit interface
  - — Compliant with DVI Specification 1.5
- Dedicated LFP (local flat panel) support
  - — Single or dual channel LVDS panel support up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz per channel
  - — SSC support of 0.5%, 1.0%, and 2.5% center and down spread with external SSC clock
  - — Supports data format of 18 bpp
  - — LCD panel power sequencing compliant with SPWG timing specification
  - — Compliant with ANSI/TIA/EIA –644-1995 spec
  - — Integrated PWM interface for LCD backlight inverter control
  - — Bi-linear Panel fitting
- Internal Graphics Features (855GME)
  - — Core Vcc = 1.2 V or 1.35 V (to support higher graphics core frequency and DDR333)
  - — Graphics core frequency
- Display core frequency at 133 MHz, 200 MHz, 250 MHz
- Render core frequency at 100 MHz, 133 MHz, 166 MHz, 200 MHz, 250 MHz
- Intel® Dual-Frequency Graphics Technology
  - — 3D Graphics Engine
- Enhanced Hardware Binning Instruction Set supported
- Bi-Cubic Filtering supported
- Linear Gamma Blending for Video Mixer Rendering (VMR)
- Video Mixer Rendering (VMR) supported
  - — Graphics Power Management
- • Dynamic Core Frequency Switching
- Intel® Smart 2D Display Technology
- Memory Self-Refresh During C3
- Intel® Display Power Saving Technology

2.3.6.4 Packaging/Power

- 732-pin Micro-FCBGA (37.5 mm x 37.5 mm)
- VTTLF, VTTHF (1.05 V)
- VCC, VCCASM, VCCHL, VCCAHPLL, VCCAGPLL, VCCADPLLA, VCCADPLLB (1.2 V or 1.35 V; as needed to support 250MHz graphics core frequency and DDR333)
- VCCADAC, VCCDVO, VCCDLVDS, VCCALVDS, (1.5 V)
- VCCSM, VCCQSM, VCCTXLVDS (2.5 V)
- VCCGPIO (3.3 V)
- Power Management (855GME)
  - — Optimized Clock Gating for 3D and Display Engines
  - — On-die thermal sensor

2.3.7 Intel® 6300ESB System Features

The Intel® 6300ESB I/O Controller Hub system consists of:

- The I/O Controller Hub (Intel® 6300ESB I/O Controller Hub) which provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many I/O functions.

The Intel® 6300ESB I/O Controller Hub integrates:

- Upstream Hub Interface for access to the MCH
- Two port Serial ATA controller
- Two channel Ultra ATA/100 Bus Master IDE controller
- One EHCI USB 2.0 host controller and two UHCI USB 1.1 host controllers (expanded capabilities for four ports)
- I/O APIC
- SMBus 2.0 controller
- FWH interface
- LPC interface
- AC’97 2.2 interface
- PCI-X 1.0 interface at 66MHz
- PCI 2.2 interface
- Two Serial I/O ports
- Two-Stage Watchdog timer

2.3.8 Firmware Hub (FWH)

- An integrated hardware Random Number Generator (RNG) on Intel parts
- Register-based locking

- Hardware-based locking
- Five GPIs

2.3.8.1 Packaging/Power

- 32-pin TSOP/PLCC
- 3.3-V core and 3.3 V/12 V for fast programming

General Design Considerations 3

This section documents motherboard layout and routing guidelines for the Intel® 855GME/ 6300ESB chipset platforms. It does not discuss the functional aspects of any bus or the layout guidelines for an add-in device.

When the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, Intel recommends that critical signals be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines shall be simulated.

The trace impedance typically noted (i.e., 55 Ω ± 15 percent) is the nominal trace impedance for a 5 mil wide external trace and a 4 mil wide internal trace. However, some stack-ups may lead to narrower or wider traces on internal or external layers in order to meet the 55 Ω impedance target. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. Note the trace impedance target assumes that the trace is not subjected to the EM fields created by changing current in neighboring traces. It is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces when calculating flight times. Using wider spaces between the traces may minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section shall be followed. Also, all high-speed, impedance-controlled signals (e.g., Intel® Pentium® M processor FSB signals) shall have continuous GND referenced planes and cannot be routed over or under power/GND plane splits.

3.1 Nominal Board Stack-Up

The Intel 855GME/6300ESB chipset-based platforms require a board stack-up yielding a target impedance of 55 Ω ± 15n percent. An example of an 8-layer board stack-up is shown in Figure 2. The left side of the figure illustrates the starting dimensions of the metal and dielectric material thickness as well as drawn trace width dimensions prior to lamination, conductor plating, and etching. After the motherboard materials are laminated, conductors plated, and etched, somewhat different dimensions result. Dielectric materials become thinner, under/over etching of conductors alters their trace width, and conductor plating makes them thicker.

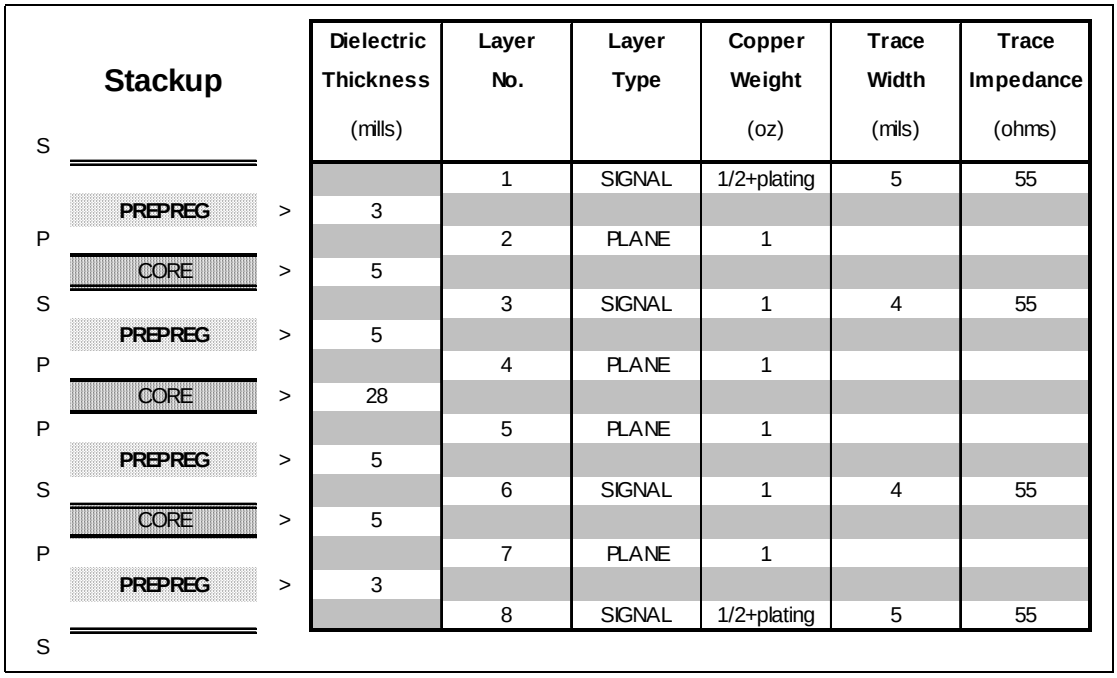
Note: For the purpose of extracting electrical models from transmission line properties, the final dimensions of signals after lamination, plating, and etching should be used.

The stack-up uses 1.2-mil (1 oz.) copper on power planes to reduce I*R drops and 0.6-mil copper thickness on the outer signal layers: primary side layer (L1), and secondary side layer (L8). Additionally, 1.2-mil copper thickness is used on the internal signal layers: Layer 3 (L3), and Layer 6 (L6). After plating, the external layers become 1.2 to 2 mils thick.

To meet the nominal 55 Ω characteristic impedance primary and secondary side layer micro-strip lines are drawn at 5 mil trace width but end up with a 4 mil final trace width after etching. For the same reason, the 5 mil thick prepreg between the primary side layer and Layer 2 starts at 5 mils but becomes 4.5 mils after lamination. This situation and result also applies to Layer 7 and the secondary side layer.

To ensure impedance control of 55 Ω, the primary and secondary side layer micro-strip lines shall reference solid ground planes on Layer 2 and Layer 7, respectively.

Figure 2. Recommended Board Stack-up Dimensions



Dielectric Thickness (mils)	Layer No.	Layer Type	Copper Weight (oz)	Trace Width (mils)	Trace Impedance (ohms)
	1	SIGNAL	1/2+plating	5	55
3					
	2	PLANE	1		
5					
	3	SIGNAL	1	4	55
5					
	4	PLANE	1		
28					
	5	PLANE	1		
5					
	6	SIGNAL	1	4	55
5					
	7	PLANE	1		
3					
	8	SIGNAL	1/2+plating	5	55

Internal signal traces on Layer 3 and Layer 6 are unbalanced strip-lines. To meet the nominal 55 Ω characteristic impedance for these traces, they reference a solid ground plane on Layer 2 and Layer 7. Because the coupling to Layer 4 and Layer 5 is still significant, (especially true when thinner stack-ups use balanced strip-lines on internal layers) these layers are converted to ground floods in the areas of the motherboard where the speed-critical interfaces such as the Intel Pentium M/Celeron M Processor FSB or DDR system memory are routed. In the remaining sections of the motherboard layout the Layer 4 and Layer 5 layers are used for power delivery.

For 55 Ω characteristic impedance Layer 3 (Layer 6), strip-lines have a 4 mil final trace width and are separated by a core dielectric thickness of 4.8 mils after lamination from the Layer 2 (Layer 7) ground plane and 4.8 mil thickness prepreg after lamination to separate it from Layer 4 (Layer 5). The starting thickness of these core and prepreg dielectric layers before lamination is 5 mils and 5 mils, respectively.

The secondary side layer (L8) is also used for power delivery in many cases since it benefits from the thick copper plating of the external layer plating as well as referencing the close (3 mil prepreg thickness) Layer 7 ground plane. The benefit of such a stack-up is low inductance power delivery.

3.2 Alternate Stack-Ups

Designers may choose to use different stack-ups (number of layers, thickness, trace width, etc.) from the one example outlined in Figure 2. However, the following key elements shall be observed:

1. Final post lamination, post etching, and post plating dimensions shall be used for electrical model extractions.
2. Power plane layers shall be 1 oz. thick and the outer signal layers shall be ½ oz. thick, while the internal signal layers shall be 1 oz. thick. External layers become 1 – 1.5 oz. (1.2 – 2 mils) thick after plating.
3. All high-speed signals shall reference solid ground planes through the length of their routing and shall not cross plane splits. To ensure this, both planes surrounding strip-lines shall be GND.
4. Intel recommends that high-speed signal routing be done on internal, strip-line layers.
5. For high-speed signals transitioning between layers next to the component, the signal pins shall be accounted for by the GND stitching vias that would stitch all the GND plane layers in that area of the motherboard. Due to the arrangement of the Intel Pentium M/Celeron M Processor and Intel 855GME chipset Graphics Memory Controller Hub (82855GME) pin-maps, GND vias placed near all GND lands are also very close to high-speed signals that may be transitioning to an internal layer. Thus, no additional ground stitching vias (besides the GND pin vias) are required in the immediate vicinity of the Intel Pentium M/Celeron M Processor and 82855GME packages to accompany the signal transitions from the component side into an internal layer.
6. High-speed routing on external layers shall be minimized in order to avoid EMI. Routing on external layers also introduces different delays compared to internal layers. This makes it extremely difficult to do length matching when some routing is done on both internal and external layers.
7. When Intel's recommended stackup guidelines are not used, the designer is liable for all aspects of their board design (i.e., understanding impacts of SI and power distribution).

Intel® Pentium® M/Celeron® M Processor FSB Design and Power Delivery Guidelines 4

The following layout guidelines support designs using the Intel® Pentium® M/Celeron® M Processor and the Intel® 855GME chipset Graphics Memory Controller Hub (82855GME). Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the motherboard for most Intel Pentium M/Celeron M Processor FSB signals. A simple point-to-point interconnect topology is used in these cases.

4.1 Intel® Pentium® M/Celeron® M Processor FSB Design Recommendations

For proper operation of the Intel Pentium M/Celeron M Processor and the Intel 855GME chipset, it is necessary that the system designer meet the timing and voltage specification of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation that make assumptions, which may be different from an OEM's system design. The most accurate way to understand the signal integrity and timing of the Intel Pentium M/Celeron M Processor FSB in your platform is by performing a comprehensive simulation analysis. It is possible that adjustments to trace impedance, line length, termination impedance, board stack-up, and other parameters may be made that improve system performance.

Refer to the latest *Intel® Pentium® M Processor Datasheet*, *Intel® Pentium® M Processor on the 90nm Process with 2MB L2 Cache Datasheet, or Intel® Celeron® M Processor Datasheet* for a FSB signal list, signal types, and definitions. Below are the design recommendations for the data, address, and strobes. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate. The following topology and layout guidelines are preliminary and subject to change. The guidelines are derived from empirical testing with GMCH package models.

4.1.1 Recommended Stack-Up Routing and Spacing Assumptions

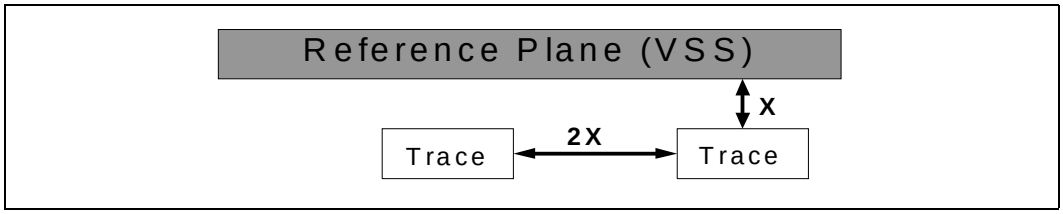
The following section describes in more detail, the terminology and definitions used for different routing and stack-up assumptions that apply to the recommended motherboard stack-up shown in Section 3.1.

4.1.1.1 Trace Space to Trace – Reference Plane Separation Ratio

Figure 3 illustrates the recommended relationship between the edge-to-edge trace spacing (2X) versus the trace to reference plane separation (X). An edge-to-edge trace spacing (2X) to trace – reference plane separation (X) ratio of 2:1 ensures a low crosstalk coefficient. All the

effects of crosstalk are difficult to simulate. The timing and layout guidelines for the Intel Pentium M/Celeron M Processor have been created with the assumption of a 2:1 trace spacing to reference plane ratio. A smaller ratio has an unpredictable impact due to crosstalk.

Figure 3. Trace Spacing versus Trace to Reference Plane Example



4.1.1.2 Trace Space to Trace Width Ratio

Figure 3 illustrates the recommended relationship between the edge-to-edge trace spacing versus trace width ratio for the best signal quality results. In general, a 3:1 trace space-to-trace width ratio (shown in Figure 5) is preferred and highly recommended. In case of routing difficulties on the motherboard, using a 2:1 ratio (shown in Figure 4) would be acceptable **only** if additional simulations conclude that it is possible, which may include some changes to the stack-up or routing assumptions.

Figure 4. Two-to-One Trace Spacing-to-Trace Width Example

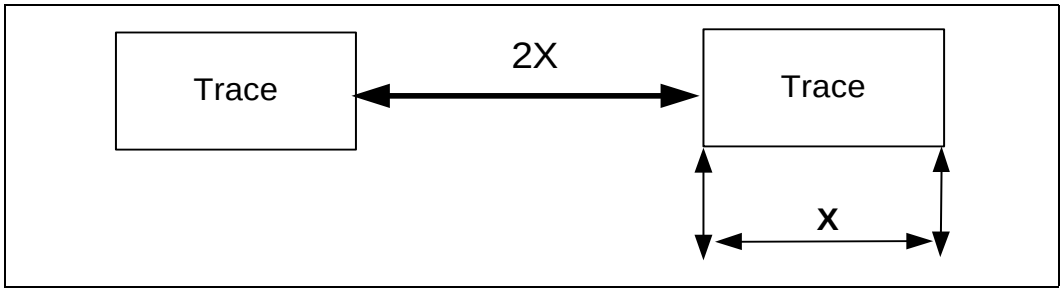
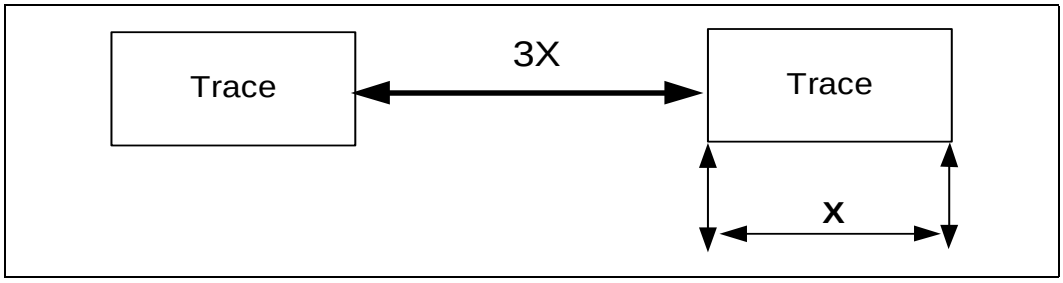


Figure 5. Three-to-One Trace Spacing-to-Trace Width Example



4.1.1.3 Recommended Stack-up Calculated Coupling Model

The importance of maintaining an adequate trace space to trace width ratio is to achieve the best signal quality possible given routing constraints. The simulations performed that resulted in the recommended 3:1 trace spacing to trace width ratio are to keep the coupling between adjacent traces below a maximum value. For the recommended stack-up, the constants shown in Figure 2 are assumed to be constant for a **typical** stack-up. This means the mutual to self-coupling

relationship given below does not take into account the normal tolerances that are allowed for in the recommended board stack-up's parameters. For the recommended stack-up shown in Figure 2, the calculated capacitive coupling maximum value is represented by the following relationship:

$$(C_{MUTUAL}/C_{SELF}) \times 100 = 8.15\%$$

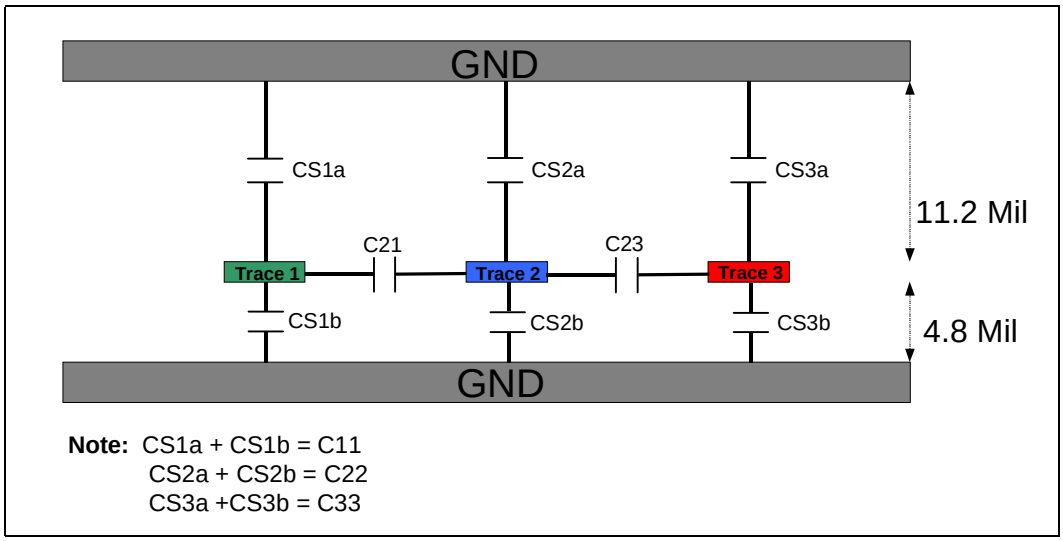
As shown in Figure 6, the coupling values are calculated based on a three-line model, represented by Trace 1, Trace 2, and Trace 3. Based on the capacitive coupling model shown, the aforementioned parameters are:

$$C_{MUTUAL} = C21 + C23$$

$$C_{SELF} = C22 \text{ (Trace 2, i.e., CS2a + CS2b)}$$

When a stack-up that is employed does not adhere to the recommended stack-up, a new extraction must be made for the stack-up using a 2D field solver program. According to the 2D field solver results, new coupling calculations must be performed to ensure that the coupling results are less than the aforementioned capacitive coupling maximum value of 8.15 percent. When the coupling results are greater than the maximum value, additional system-level simulations must be performed to avoid any signal quality issues due to crosstalk effects.

Figure 6. Recommended Stack-up Capacitive Coupling Model



4.1.1.4 Signal Propagation Time-to-Distance Relationship and Assumptions

Due to the high-frequency nature of some interfaces and signals, length matching may or may not exist as part of the routing requirements for a given interface. In general, the tolerances that specific signals in a bus must be routed to are stated as a length measured in mils or inches and are specific to the recommended motherboard stack-up (refer to Section 3.1). However, some length matching tolerances for signals listed in this design guide may be stated as a measurement of time. In such cases, the correlation of the period of time to an actual length value depends on board stack-up.

Based on the recommended stack-up, the signal propagation time to distance relationship, for the purpose of this design guide, is as follows:

- Strip-line (internal layer) routing: 180 ps for 1.0 inch

For example, a length-matching requirement of ± 50 ps for routing on a strip-line (internal) layer would correlate to a trace length whose tolerance are ± 278 mils of an associated trace. The signal propagation time-to-distance relationship listed above is based on a single transmission line model incorporating a **typical** stack-up. Thus, no other signals or traces are accounted for in such a model and there is an assumption of zero coupling with other traces. Also, the recommended stack-up's parameter tolerances are not taken into account in the typical stack-up assumptions. Finally, in cases that need to account for worst-case stack-up parameters and for even- or odd mode coupling, new extractions from the stack-up model must be done to provide an accurate signal propagation time-to-distance relationship.

4.1.2 Common Clock Signals

All common clock signals use an AGTL+ bus driver technology with on-die integrated GTL termination resistors connected in a point-to-point, Zo = 55 Ω, controlled impedance topology between the Intel Pentium M/Celeron M Processor and the GMCH. No external termination is needed on these signals. These signals operate at the Intel Pentium M/Celeron M Processor FSB frequency of 100 MHz.

Common clock signals shall be routed on an internal layer while referencing solid ground planes. Based on current simulation results, routing on internal layers allows for a minimum pin-to-pin motherboard length of 1.0 inch and a maximum of 6.5 inches. Trace length matching for the common clock signals is not required. For details on minimum motherboard trace length requirements, refer to Section 4.1.2.1 and Table 3 for more details. Intel recommends routing these signals on the same internal layer for the entire length of the bus. When routing constraints require routing of these signals with a transition to a different layer, a minimum of one ground stitching via for every two signals shall be placed within 100 mils of the signal transition vias.

Routing of the common clock signals shall use 2:1 trace spacing to trace width. This implies a minimum of 8 mils spacing (i.e., 12 mil minimum pitch) for a 4 mil trace width for routing on internal layers. Practical cases of escape routing under the 82855GME or Intel Pentium M/Celeron M Processor package outline and vicinity may not allow the implementation of 2:1 trace spacing requirements. Although every attempt shall be made to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the GMCH and the Intel Pentium M/Celeron M Processor package outlines and up to 200–300 mils outside the package outline.

Table 3 summarizes the list of common clock and key routing requirements. RESET# (CPURESET# of GMCH) is also a common clock signal but requires a special treatment for the case where an ITP700FLEX debug port is used. Refer to Section 4.1.6 for further details.

Table 3. Intel® Pentium® M/Celeron® M Processor System Bus Common Clock Signal Internal Layer Routing Guidelines (Sheet 1 of 2)

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width and Spacing (mils)
CPU	GMCH		Min (mils)	Max (inches)		
ADS#	ADS#	Strip-line	997	6.5	55 ± 15%	4 and 8
BNR#	BNR#	Strip-line	1298	6.5	55 ± 15%	4 and 8
BPRI#	BPRI#	Strip-line	1215	6.5	55 ± 15%	4 and 8
BR0#	BR0#	Strip-line	1411	6.5	55 ± 15%	4 and 8

† For topologies where an ITP700FLEX debug port is implemented, refer to Section 4.1.6 for RESET# (CPURESET#) implementation details.

Table 3. Intel® Pentium® M/Celeron® M Processor System Bus Common Clock Signal Internal Layer Routing Guidelines (Sheet 2 of 2)

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width and Spacing (mils)
CPU	GMCH		Min (mils)	Max (inches)		
DBSY#	DBSY#	Strip-line	1159	6.5	55 ± 15%	4 and 8
DEFER#	DEFER#	Strip-line	1291	6.5	55 ± 15%	4 and 8
DPWR#	DPWR#	Strip-line	1188	6.5	55 ± 15%	4 and 8
DRDY#	DRDY#	Strip-line	1336	6.5	55 ± 15%	4 and 8
HIT#	HIT#	Strip-line	1303	6.5	55 ± 15%	4 and 8
HITM#	HITM#	Strip-line	1203	6.5	55 ± 15%	4 and 8
LOCK#	HLOCK#	Strip-line	1198	6.5	55 ± 15%	4 and 8
RS0#	RS0#	Strip-line	1315	6.5	55 ± 15%	4 and 8
RS1#	RS1#	Strip-line	1193	6.5	55 ± 15%	4 and 8
RS2#	RS2#	Strip-line	1247	6.5	55 ± 15%	4 and 8
TRDY#	HTRDY#	Strip-line	1312	6.5	55 ± 15%	4 and 8
RESET#†	CPURESET#	Strip-line	1101	6.5	55 ± 15%	4 and 8

† For topologies where an ITP700FLEX debug port is implemented, refer to Section 4.1.6 for RESET# (CPURESET#) implementation details.

4.1.2.1 Intel® Pentium® M/Celeron® M Processor Common Clock Signal Package Length Compensation

Trace length matching for the common clock signals is not required. However, package compensation for the common clock signals is required for the minimum board trace. Refer to Table 4 and the example for more details. Package length compensation shall not be confused with length matching. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting out package length variance across a signal group.

All common clock signals are required to meet the minimum pad-to-pad requirement of 2.212 inches, based on ADS# (as this signal has the longest package lengths) implies a minimum pin-to-pin motherboard trace length of 1.0 inches or more depending on package lengths. As a result, additional motherboard trace is added to some of the shorter common clock nets on the system board in order to meet the longest common clock signal total trace lengths from the die-pad of the processor to the associated die-pad of the chipset.

For example:

ADS# = 997 mils board trace + 454 Intel Pentium M/Celeron M Processor PKG + 761 GMCH PKG = 2212 pad-to-pad length.

BR0# = X mils board trace + 465 Intel Pentium M/Celeron M Processor PKG + 336 GMCH PKG = 2212 pad-to-pad length.

Therefore: BR0# board trace = 2212 pad-to-pad length - 465 Intel Pentium M/Celeron M Processor PKG - 336 GMCH PKG = 1411 pin-to-pin length.

Figure 7 depicts the common clock topology.

Figure 7. Common Clock Topology

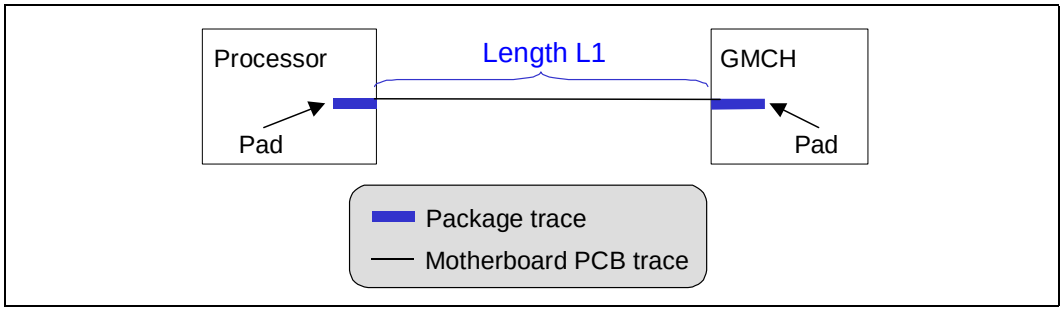


Table 4. Intel® Pentium® M/Celeron® M Processor and Intel® GMCH FSB Common Clock Signal Package Lengths and Minimum Board Trace Lengths

Signal Names		Package Length		Total Pad-to-Pad Min. Length Requirements L1	Minimum Routable Board Trace Length
CPU	GMCH	CPU	GMCH		
ADS#	ADS#	454	761	2212	997
BNR#	BNR#	506	408	2212	1298
BPRI#	BPRI#	424	573	2212	1215
BR0#	BR0#	336	465	2212	1411
DBSY#	DBSY#	445	608	2212	1159
DEFER#	DEFER#	349	572	2212	1291
DPWR#	DPWR#	506	518	2212	1188
DRDY#	DRDY#	529	347	2212	1336
HIT#	HIT#	420	489	2212	1303
HITM#	HITM#	368	641	2212	1203
LOCK#	HLOCK#	499	515	2212	1198
RS0#	RS0#	576	321	2212	1315
RS1#	RS1#	524	495	2212	1193
RS2#	RS2#	451	514	2212	1247
TRDY#	HTRDY#	389	511	2212	1312
RESET#	CPURESET#	455	656	2212	1101

4.1.3 Source Synchronous Signals General Routing Guidelines

All source synchronous signals use an AGTL+ bus driver technology with on-die GTL termination resistors connected in a point-to-point, Zo = 55 Ω controlled impedance topology between the Intel Pentium M/Celeron M Processor and the GMCH. No external termination is needed on these signals. Source synchronous Intel Pentium M/Celeron M Processor FSB address signals operate at a double-pumped rate of 200 MHz while the source synchronous processor FSB data signals operate at a quad-pumped rate of 400 MHz. High speed operation of the source synchronous signals requires careful attention to their routing considerations. The following guidelines shall be strictly adhered to, to ensure robust high-frequency operation of these signals.

Source synchronous data and address signals and their associated strobes are partitioned into groups of signals. Flight time skew minimization within the same group of source synchronous signals is a key parameter that allows their high-frequency (400 MHz) operation. All the source synchronous signals that belong to **the same group** shall be routed on **the same internal layer** for the entire length of the bus. It is permissible to split different groups of source synchronous signals between different motherboard layers as long as all the signals that belong to that group are kept on the same layer. Grouping of the Intel Pentium M/Celeron M Processor FSB source synchronous signals is summarized in Table 5 and Table 7. This practice results in a significant reduction of the flight time skew because the dielectric thickness, line width, and velocity of the signals are uniform across a single layer of the stack-up. The relationship of dielectric thickness, line width, and velocity between layers cannot be ensured.

The source synchronous signals shall be routed as a strip-line on an internal layer with complete reference to ground planes both above and below the signal layer. Routing with references to split planes or power planes other than ground is **not** allowed. For the recommended stack-up example as shown in Figure 2, source synchronous Intel Pentium M/Celeron M Processor FSB signals are routed on Layer 3 and Layer 6. Layer 2 and Layer 7 are solid grounds across the entire motherboard. However, this is not sufficient because significant coupling exists between signal layer, Layer 3 and power plane Layer 4 as well as signal layer, Layer 6 and power plane Layer 5. To ensure complete ground referencing, Layer 4 and Layer 5 are converted to ground plane floods in the areas where the source synchronous processor FSB signals are routed. In addition, all the ground plane areas are stitched with ground vias in the vicinity of the Intel Pentium M/Celeron M Processor and Intel 855GME chipset package outlines with the vias of the ground pins of the Intel Pentium M/Celeron M Processor and Intel 855GME chipset pin-map.

Figure 8 illustrates a motherboard layout and a cross-sectional view of the recommended stack-up of the Intel Pentium M/Celeron M Processor FSB source synchronous DATA and ADDRESS signals referencing ground planes on both Layer 7 and Layer 5. In the socket cavity of the Intel Pentium M/Celeron M Processor, Layer 5 and Layer 6 are used for VCC core power delivery. However, outside the socket cavity Layer 6 signals are routed on top of a solid Layer 7 ground plane and also Layer 5 is converted to a ground flood under the shadow of the Intel Pentium M/Celeron M Processor FSB signals routing between the Intel Pentium M/Celeron M Processor and GMCH. Stitching of all the GND planes is provided by the ground vias in the pin-map of the Intel Pentium M/Celeron M Processor and GMCH.

Figure 8. Layer 6 Intel® Pentium® M/Celeron® M Processor FSB Source Synchronous Signals GND Referencing to Layer 5 and Layer 7 Ground Planes

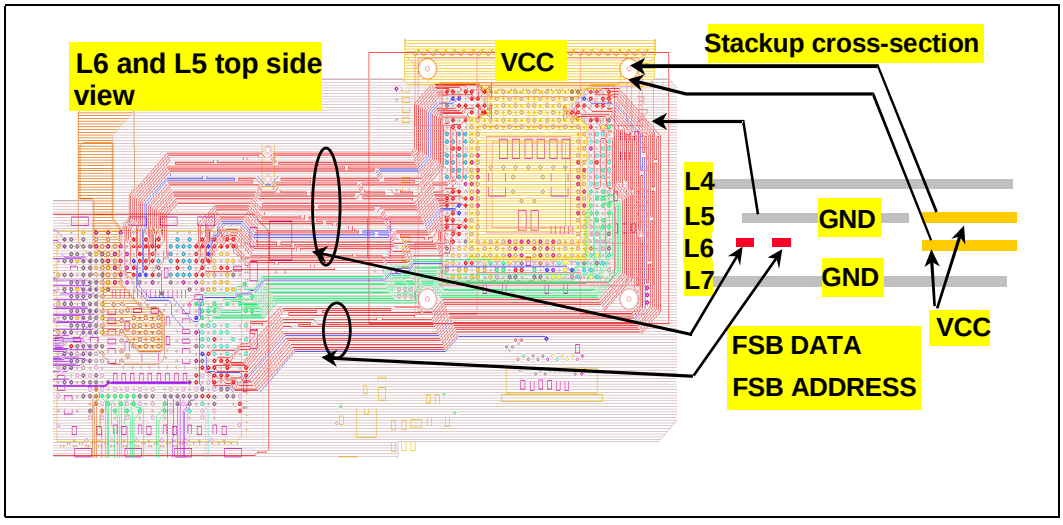


Figure 9. Layer 6 Intel® Pentium® M/Celeron® M Processor FSB Source Synchronous Data Signals

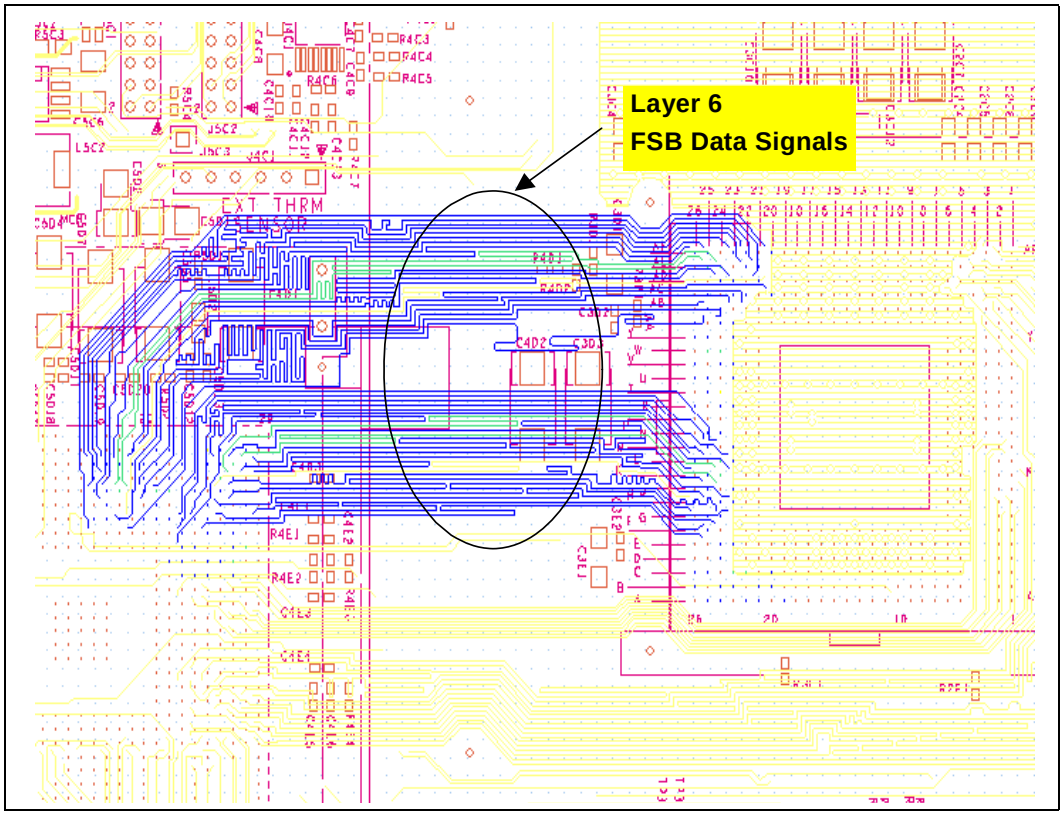
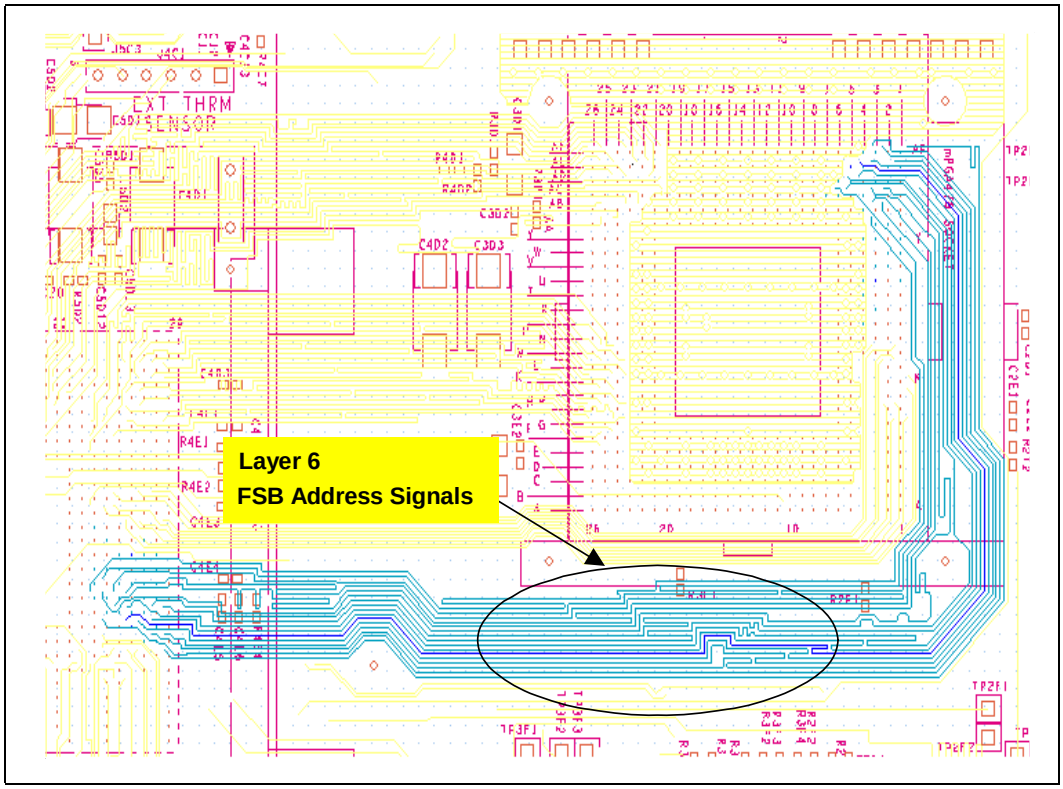


Figure 10. Layer 6 Intel® Pentium® M/Celeron® M Processor System Bus Source Synchronous Address Signals



In a similar way, Figure 11 illustrates a recommended layout and stack-up example of how another group of Intel Pentium M/Celeron M Processor FSB source synchronous DATA and ADDRESS signals may reference ground planes on both Layer 2 and Layer 4. In the socket cavity of the Intel Pentium M/Celeron M Processor, Layer 3 is used for VCC core power delivery to reduce the I*R drop. However, outside of the socket cavity, Layer 3 signals are routed below a solid Layer 2 ground plane. Layer 4 is converted to a ground flood under the shadow of the Intel Pentium M/Celeron M Processor FSB signals routing between the Pentium M/Celeron M processor and GMCH. Figure 12 and Figure 13 depict example routing for Intel customer reference board.

Figure 11. Layer 3 Intel® Pentium® M/Celeron® M Processor FSB Source Synchronous Signals GND Referencing to Layer 2 and Layer 4 Ground Planes

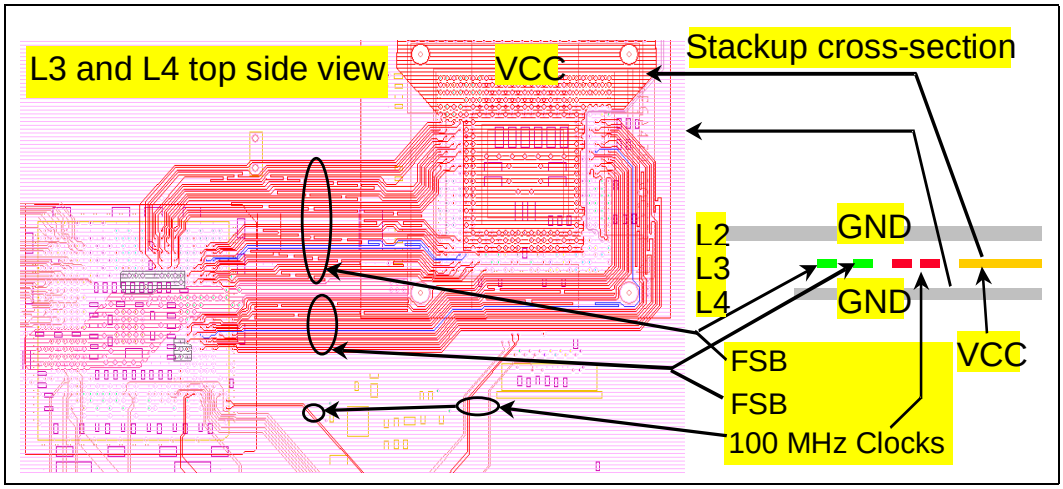


Figure 12. Layer 3 Intel® Pentium® M/Celeron® M Processor FSB Source Synchronous Data Signals

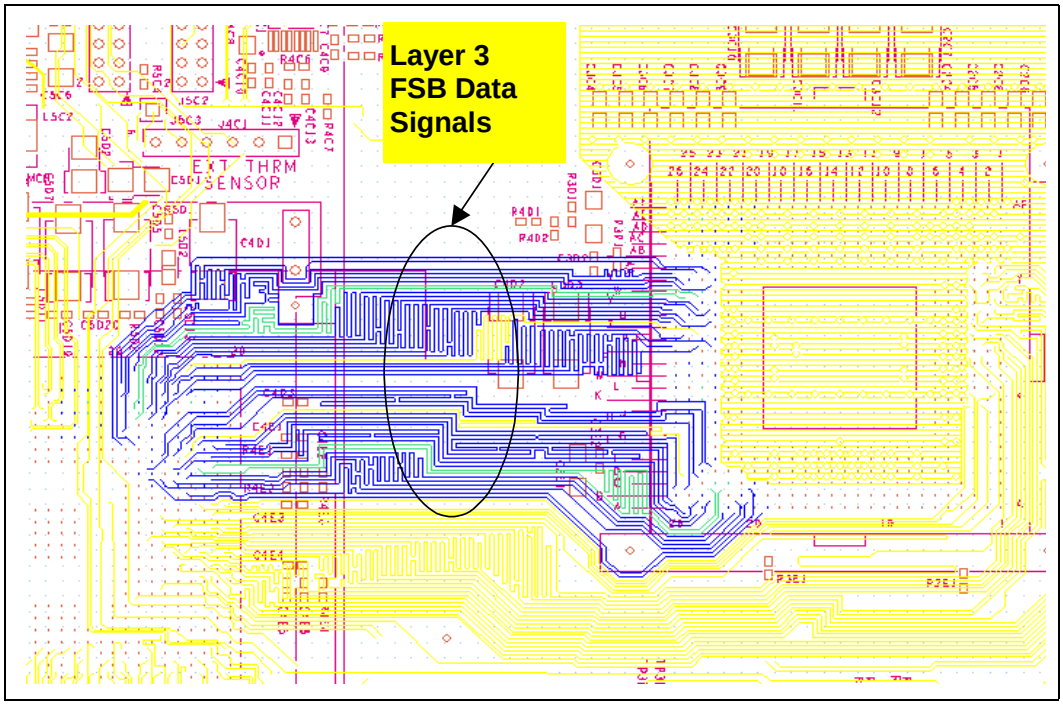
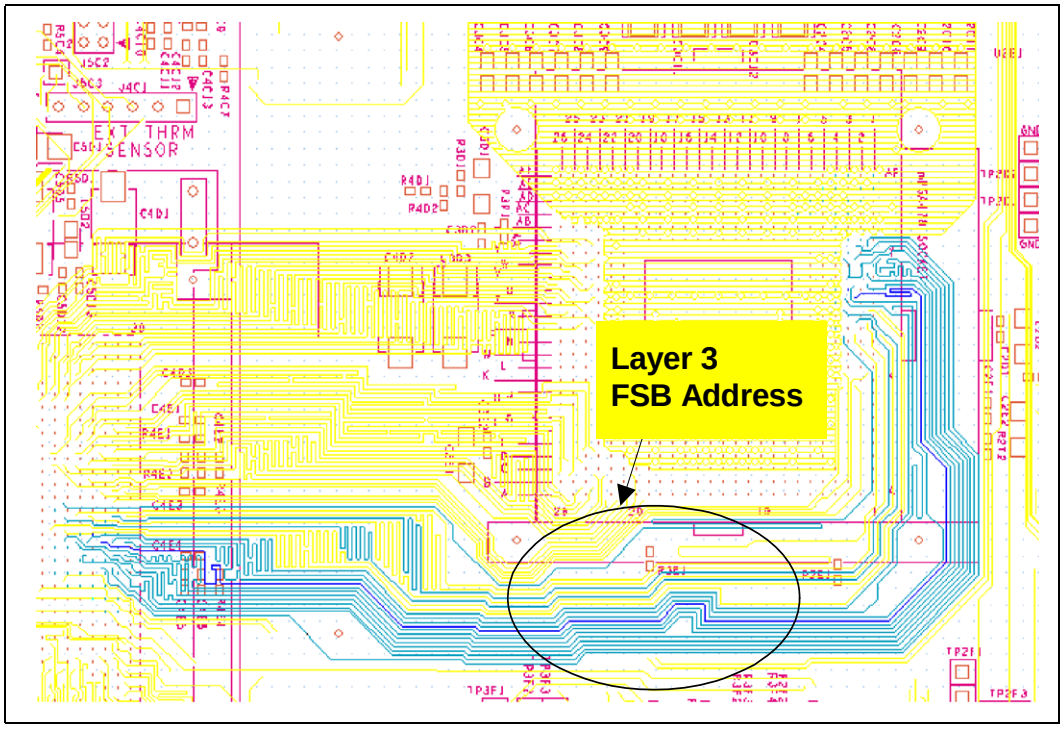


Figure 13. Layer 3 Intel® Pentium® M/Celeron® M Processor FSB Source Synchronous Address Signals



Skew minimization requires pin-to-pad trace length matching of the Intel Pentium M/Celeron M Processor FSB source synchronous signals that belong to the same group including the strobe signals of that group. Refer to Section 4.1.2.1 for trace length matching and package compensations requirements.

Current simulation results provide routing guidelines using 3:1 spacing for the Intel Pentium M/Celeron M Processor FSB source synchronous data and strobe signals. This implies a minimum of 12 mil spacing (i.e., 16 mil minimum pitch) for a 4 mil trace width. Practical cases of escape routing under the GMCH or Intel Pentium M/Celeron M Processor package outline and vicinity may not even allow the implementation of 2:1 trace spacing requirements. Although every attempt shall be made to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the GMCH and the Intel Pentium M/Celeron M Processor package outlines and up to 200 – 300 mils outside the package outline. The benefits of additional spacing include increased signal quality and voltage margining. The trace routing and length matching requirements are as follows in Section 4.1.3.1 to Section 4.1.3.3.

4.1.3.1 Source Synchronous – Data Group

Robust operation of the 400 MHz, source synchronous data signals require tight skew control. For this reason, these signals are split into matched groups as outlined in Table 5. All the signals within the same group shall be kept on the same layer of motherboard routing and shall be routed to the same pad-to-pin length within ±100 mils of the associated strobes. Only the Intel Pentium M/Celeron M Processor has the package trace equalization for signals within each data and address group. The GMCH does not have package trace equalization for signals within each data and address group. All signals shall be routed on the system board to meet the pad-to-pin matching requirement of ± 100 mils. Refer to Table 9 for the Intel 855GME chipset package lengths.

Refer to Section 4.1.2.1 for trace length and package compensation requirements. The two complementary strobe signals associated with each group shall be length matched (pad-to-pin) to each other within ± 25 mils and tuned to the average length of the data signals (pad-to-pin) of their associated group. This optimizes setup/hold time margin.

Table 5. Intel® Pentium® M/Celeron® M Processor FSB Data Source Synchronous Signal Trace Length Mismatch Mapping

Data Group	DINV Signal for Associated Data Group	Signal Matching	Data Strobes Associated with the Group	Strobe Matching	Notes
D[15:0]#	DINV0#	± 100 mils	DSTBP0#, DSTBN0#	± 25 mils	1, 2
D[31:16]#	DINV1#	± 100 mils	DSTBP1#, DSTBN1#	± 25 mils	1, 2
D[47:32]#	DINV2#	± 100 mils	DSTBP2#, DSTBN2#	± 25 mils	1, 2
D[63:48]#	DINV3#	± 100 mils	DSTBP3#, DSTBN3#	± 25 mils	1, 2

NOTES:
1. Strobes of the same group shall be trace length matched to each other within ± 25 mils and to the average length of their associated data signal group.
2. All length matching formulas are based on GMCH die-pad to Intel Pentium M/Celeron M Processor pin total length per byte lane. Package length tables are provided for all signals to facilitate this pad-to-pin matching.

Table 6 lists the source synchronous data signal general routing requirements. Due to the 400 MHz, high-frequency operation the data signals shall be limited to a pin-to-pin trace length minimum of 0.50 inches and maximum of 5.5 inches.

Table 6. Intel® Pentium® M/Celeron® M Processor System Bus Source Synchronous Data Signal Routing Guidelines

Signal Names				Trans-mission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width and spacing (mils)
Data Group #1	Data Group #2	Data Group #3	Data Group #4		Min (inches)	Max (inches)		
D[15:0]#	D[31:16]#	D[47:32]#	D[63:48]#	Strip-line	0.5	5.5	55 ± 15%	4 and 12
DINV0#	DINV1#	DINV2#	DINV3#	Strip-line	0.5	5.5	55 ± 15%	4 and 12
DSTBN[0]#	DSTBN[1]#	DSTBN[2]#	DSTBN[3]#	Strip-line	0.5	5.5	55 ± 15%	4 and 12
DSTBP[0]#	DSTBP[1]#	DSTBP[2]#	DSTBP[3]#	Strip-line	0.5	5.5	55 ± 15%	4 and 12

4.1.3.2 Source Synchronous – Address Group

Source synchronous address signals operate at 200 MHz. Thus, their routing requirements are very similar to the data signals. Refer to Section 4.1.3 and Section 4.1.3.1 for further details. Table 7 details the partition of the address signals into matched length groups. Due to the lower operating frequency of the address signals, pad-to-pin length matching is relaxed to ± 200 mils. Each group is associated with only one strobe signal. To maximize setup/hold time margin, the address strobes shall be trace length matched to the average trace length of the address signals of their associated group. In addition, each address signal shall be trace length matched within ± 200 mils of its associated strobe signal.

Table 7. Intel® Pentium® M/Celeron® M Processor FSB Address Source Synchronous Signal Trace Length Mismatch Mapping

CPU Signal Name	Signal Matching	Strobe Associated with the Group	Strobe to Associated Address Signal Matching	Notes
REQ[4:0]#, A[16:3]#	± 200 mils	ADSTB0#	± 200 mils	1, 2, 3
A[31:17]#	± 200 mils	ADSTB1#	± 200 mils	1, 2, 3

NOTES:
1. ADSTB[1:0]# shall be trace length matched to the average length of the associated address signals group.
2. Each address signal shall be trace length matched to its associated address strobe within ± 200 mils.
3. All length matching formulas are based on GMCH die-pad to Pentium M/Celeron M processor pin total length per signal group. Package length tables are provided for all signals to facilitate this pad to pin matching.

Table 8 lists the source synchronous address signals general routing requirements. They should be routed to a pin-to-pin length minimum of 0.50 inches and a maximum of 6.5 inches. Due to the 200 MHz, high-frequency operation of the address signals, the routing guidelines listed in Table 8 allow for 2:1 spacing for the address signals given a 55 Ω ± 15% characteristic trace impedance except for address strobe signals. But if space permits, 3:1 spacing is strongly advised for these signals.

Table 8. Intel® Pentium® M/Celeron® M Processor FSB Source Synchronous Address Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width and Spacing (mils)
Address Group #1	Address Group #2		Min (inches)	Max (inches)		
A[16:3]#	A[31:17]#	Strip-line	0.50	6.5	55 ± 15%	4 and 8
REQ[4:0]#		Strip-line	0.50	6.5	55 ± 15%	4 and 8
ADSTB#[0]	ADSTB#[1]	Strip-line	0.50	6.5	55 ± 15%	4 and 12

4.1.3.3 Intel® Pentium® M/Celeron® M Processor and Intel® 855GME Chipset GMCH (82855GME) FSB Signal Package Lengths

Table 9 lists the preliminary package trace lengths of the Pentium M/Celeron M processor and the 82855GME for the source synchronous data and address signals. The Pentium M/Celeron M processor FSB package signals within the same group are **routed** to the same package trace length, but the Intel 855GME chipset package signals within the same group are **not routed** to the same package trace length. As a result of this package length compensation is required for GMCH. Refer to Section 4.1.4 for length matching constraints and to Section 4.1.4.1 package length compensation for further details. The Pentium M/Celeron M processor package traces are routed as micro-strip lines with a nominal characteristic impedance of 55 Ω ± 15 percent.

Table 9. Intel® Pentium® M/Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 1 of 6)

Signal Group	CPU Signal Name	Intel® Pentium® M/Celeron® M Processor Package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Data Group 1	D15#	721	HD15#	554
	D14#	721	HD14#	393
	D13#	721	HD13#	494
	D12#	721	HD12#	620
	D11#	721	HD11#	319
	D10#	721	HD10#	504
	D9#	721	HD9#	438
	D8#	721	HD8#	458
	D7#	721	HD7#	329
	D6#	721	HD6#	518
	D5#	721	HD5#	693
	D4#	721	HD4#	600
	D3#	721	HD3#	387
	D2#	721	HD2#	438
	D1#	721	HD1#	620
	D0#	721	HD0#	329
	DINV[0]#	721	DINV[0]#	514
	DSTBP[0]#	721	HDSTBP[0]#	662
	DSTBN[0]#	721	HDSTBN[0]#	763

Table 9. Intel® Pentium® M/Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 2 of 6)

Signal Group	CPU Signal Name	Intel® Pentium® M/Celeron® M Processor Package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Data Group 2	D31#	564	HD31#	914
	D30#	564	HD30#	464
	D29#	564	HD29#	691
	D28#	564	HD28#	768
	D27#	564	HD27#	453
	D26#	564	HD26#	815
	D25#	564	HD25#	837
	D24#	564	HD24#	493
	D23#	564	HD23#	766
	D22#	564	HD22#	731
	D21#	564	HD21#	522
	D20#	564	HD20#	714
	D19#	564	HD19#	412
	D18#	564	HD18#	834
	D17#	564	HD17#	634
	D16#	564	HD16#	593
	DINV[1]#	564	DINV[1]#	628
	DSTBP[1]#	564	HDSTBP[1]#	736
	DSTBN[1]#	564	HDSTBN[1]#	787

Table 9. Intel® Pentium® M/Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 3 of 6)

Signal Group	CPU Signal Name	Intel® Pentium® M/Celeron® M Processor Package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Data Group 3	D47#	661	HD47#	654
	D46#	661	HD46#	647
	D45#	661	HD45#	460
	D44#	661	HD44#	563
	D43#	661	HD43#	726
	D42#	661	HD42#	828
	D41#	661	HD41#	608
	D40#	661	HD40#	358
	D39#	661	HD39#	655
	D38#	661	HD38#	619
	D37#	661	HD37#	747
	D36#	661	HD36#	633
	D35#	661	HD35#	675
	D34#	661	HD34#	683
	D33#	661	HD33#	501
	D32#	661	HD32#	664
	DINV[2]#	661	DINV[2]#	784
	DSTBP[2]#	661	HDSTBP[2]#	502
	DSTBN[2]#	661	HDSTBN[2]#	538

Table 9. Intel® Pentium® M/Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 4 of 6)

Signal Group	CPU Signal Name	Intel® Pentium® M/Celeron® M Processor Package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Data Group 4	D63#	758	HD63#	579
	D62#	758	HD62#	509
	D61#	758	HD61#	431
	D60#	758	HD60#	522
	D59#	758	HD59#	490
	D58#	758	HD58#	347
	D57#	758	HD57#	649
	D56#	758	HD56#	372
	D55#	758	HD55#	541
	D54#	758	HD54#	598
	D53#	758	HD53#	469
	D52#	758	HD52#	575
	D51#	758	HD51#	326
	D50#	758	HD50#	549
	D49#	758	HD49#	511
	D48#	758	HD48#	372
	DINV[3]#	758	DINV[3]#	431
	DSTBP[3]#	758	HDSTBP[3]#	463
	DSTBN[3]#	758	H DSTBN[3]#	505

Table 9. Intel® Pentium® M/Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 5 of 6)

Signal Group	CPU Signal Name	Intel® Pentium® M/Celeron® M Processor Package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Address Group 1	REQ4#	616	HREQ4#	276
	REQ3#	616	HREQ3#	383
	REQ2#	616	HREQ2#	247
	REQ1#	616	HREQ1#	378
	REQ0#	616	HREQ0#	569
	A16#	616	HA16#	491
	A15#	616	HA15#	375
	A14#	616	HA14#	562
	A13#	616	HA13#	501
	A12#	616	HA12#	522
	A11#	616	HA11#	566
	A10#	616	HA10#	560
	A9#	616	HA9#	327
	A8#	616	HA8#	333
	A7#	616	HA7#	274
	A6#	616	HA6#	523
	A5#	616	HA5#	551
	A4#	616	HA4#	352
	A3#	616	HA3#	468
	ADSTB[0]#	616	HADSTB[0]#	419

Table 9. Intel® Pentium® M/Celeron® M Processor and GMCH Source Synchronous FSB Signal Package Lengths (Sheet 6 of 6)

Signal Group	CPU Signal Name	Intel® Pentium® M/Celeron® M Processor Package Trace Length (mils)	GMCH Signal Name	GMCH Package Trace Length (mils)
Address Group 2	A31#	773	HA31#	617
	A30#	773	HA30#	484
	A29#	773	HA29#	558
	A28#	773	HA28#	579
	A27#	773	HA27#	631
	A26#	773	HA26#	556
	A25#	773	HA25#	535
	A24#	773	HA24#	353
	A23#	773	HA23#	382
	A22#	773	HA22#	545
	A21#	773	HA21#	429
	A20#	773	HA20#	414
	A19#	773	HA19#	284
	A18#	773	HA18#	389
	A17#	773	HA17#	457
	ADSTB[1]#	773	HADSTB[1]#	504
Host Clocks	BCLK0	447	BCLK	1138
	BCLK1	447	BCLK#	1145
ITP Signals	BPM[3:0]	593	—	—

4.1.4 Length Matching Constraints

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routing lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, there are more restrictive length matching requirements called length-matching constraints. These additional requirements further restrict the minimum to maximum length range of each signal group with respect to clock strobe, within the overall boundaries defined in the guideline tables, as required to ensure adequate timing margins.

The amount of minimum to maximum length variance allowed for each group around the clock strobe reference length varies from signal group to signal group depending on the amount of timing variation that may be tolerated. Refer to Table 6 for source synchronous data matching requirements and Table 7 for source synchronous address matching requirements.

4.1.4.1 Package Length Compensation

The Intel Pentium M/Celeron M Processor package length does not need to be accounted for in the motherboard routing since the Intel Pentium M/Celeron M Processor has the source synchronous signals and the strobes length matched within the group inside the package routing. However trace length matching of the GMCH package length *does* need to be accounted for in the motherboard routing because the package does not have the source synchronous signals and the strobes length matched within the group inside the package routing. Refer to Table 9 for the Intel Pentium M/Celeron M Processor and Intel 855GME chipset package lengths. Skew minimization requires Intel 855GME chipset die-pad to Intel Pentium M/Celeron M Processor pin (pad-to-pin) trace length matching of the Intel Pentium M/Celeron M Processor FSB source synchronous signals that belong to the same group including the strobe signals of that group.

As mentioned briefly above, all length matching is done GMCH die-pad to Intel Pentium M/Celeron M Processor pin. The reason for this is to compensate for the package length variation across each signal group to minimize timing variance. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the GMCH requires a length matching process.

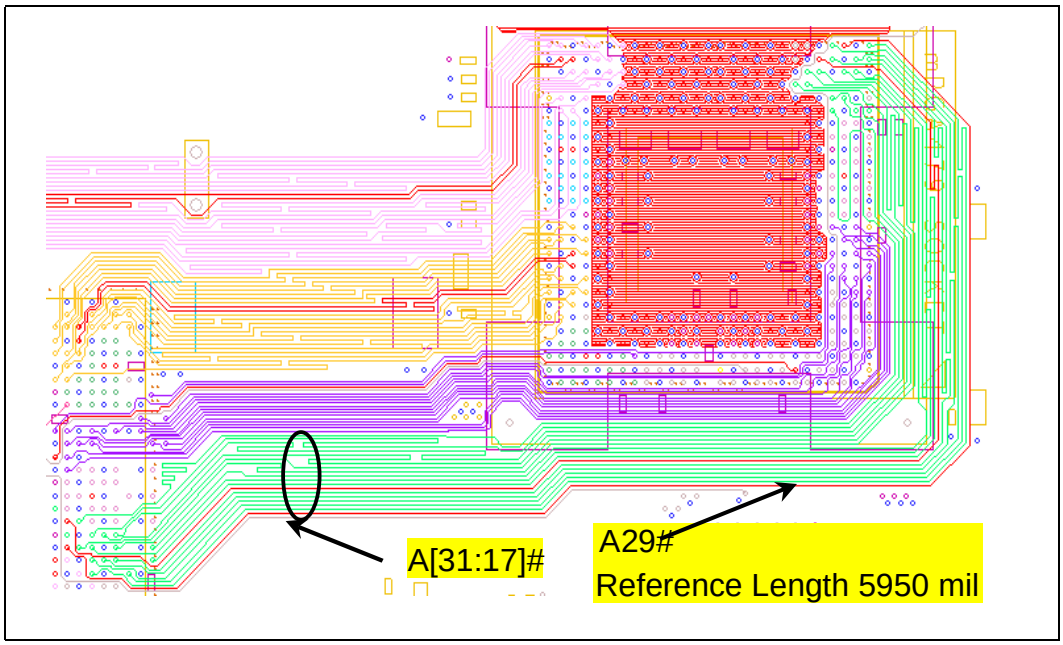
Package length compensation shall not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting package length variance across a signal group. There is some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

4.1.4.2 Trace Length Equalization Procedures

Figure 15 illustrates the trace length matching procedure described below. It is convenient to perform the trace length matching with the aid of a simple Microsoft Excel* spreadsheet or other spreadsheet software. The layout editor used in this example is Allegro*.

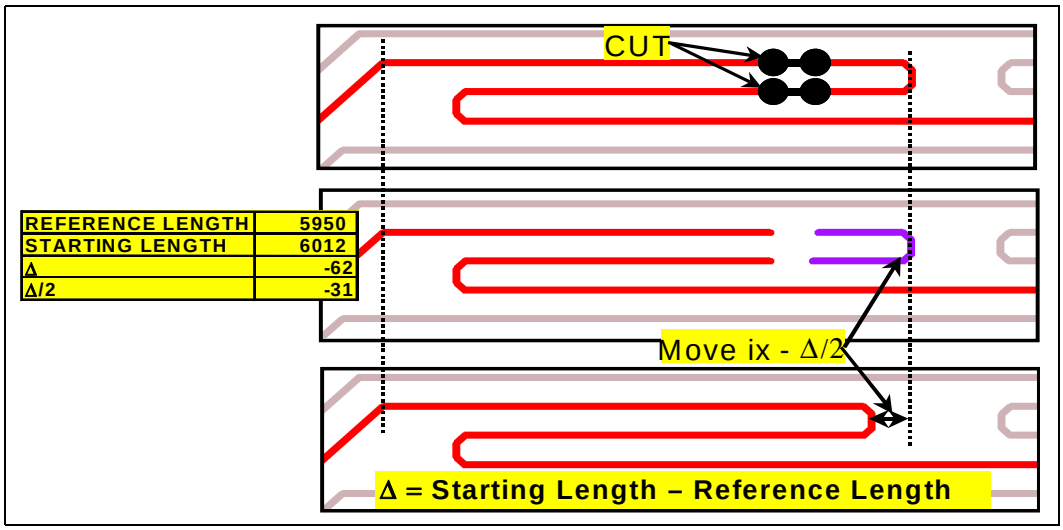
1. Cell B3 in Excel is preset to calculate the Δ, which is the difference between the starting length and reference length. This cell calculates the function B1 - B2.
2. Cell B4 calculates half of the Δ. This cell calculates the function B3/2.
3. Pre-route all the traces to approximately the same length using serpentines. The serpentines must use the same 3:1 spacing as the rest of the routing. It is useful to make the traces 16 to 32 mils longer than needed in this stage. It is also important that there shall be **no** 90° angles in the serpentines.
4. In the group of traces to be equalized, select the trace that cannot be made any shorter. Taking A[31:17]# as an example, in Figure 14 the longest trace that defines the reference length turns out to be A29#. Notice that there are no serpentines on this signal. Use the Allegro* I (info) command to report the reference length of the longest trace in the group. Record the reference length in cell B1 of Excel*.

Figure 14. Reference Trace Length Selection



5. Use the Allegro* I (info) command to report the current length of the trace to be equalized. Record the length in cell B2 of the Excel* spreadsheet.
6. Use the Allegro* "Cut" command to cut the trace in two locations of the serpentine as shown in Figure 15. This operation generates a floating section of the serpentine.
7. Use the Allegro* "Move ix" (i.e., if vertical routing) command to move the floating section by the Δ/2 distance listed in cell B4.
8. Reconnect the floating segment if needed.
9. Repeat steps 5 through 8 for the reminder of the traces in the group.

Figure 15. Trace Length Equalization Procedures with Allegro*



4.1.5 Asynchronous Signals

The following sections describe the topologies and layout recommendations for the asynchronous open drain and CMOS signals found on the platform. All open drain signals listed in the following sections must be pulled-up to VCCP (1.05 V). When any of these open drain signals are pulled-up to a voltage higher than VCCP, the reliability and power consumption of the processor may be affected. Therefore, it is very important to follow the recommended pull-up voltage for these signals. All signals must meet the AC and DC specifications as documented in the *Intel Pentium® M Processor Datasheet, Intel Pentium® M Processor on the 90nm Process with 2MB L2 Cache Datasheet*, or the *Intel Celeron® M Processor Datasheet*.

Table 10. Asynchronous AGTL+ Nets

Signal Names	Description	Topology #	CPU I/O Type	Output	Output Buffer Type	Input	Input Power Well
IERR#	Internal error	1A	O	CPU	AGTL+	System Receiver	Vcc_Receiver
FERR#	Floating point error	1B	O	CPU	AGTL+	6300ESB	Main I/O (3.3 V)
THRMTRIP#	Thermal sensor	1B	O	CPU	AGTL+	System Receiver	Vcc_Receiver
PROCHOT#	Thermal sensor	1C	O	CPU	AGTL+	System Receiver	Vcc_Receiver
PWRGOOD	System power good	2A	I	AND Gate	OD CMOS	CPU	N/A
DPSLP#††	Deep sleep		I			CPU	
LINT0/INTR	Local interrupts	2B	I	6300ESB	CMOS	CPU	N/A
LINT1/NMI	Local interrupts	2B	I	6300ESB	CMOS	CPU	N/A
SLP#	Sleep	2B	I	6300ESB	CMOS	CPU	N/A
STPCLK#	Processor stop clock	2B	I	6300ESB	CMOS	CPU	N/A
IGNNE#	Ignore next numeric error	2B	I	6300ESB	CMOS	CPU	N/A
SMI#	System management interrupt	2B	I	6300ESB	CMOS	CPU	N/A
A20M#	Address 20 mask	2B	I	6300ESB	CMOS	CPU	N/A
INIT#	Processor initialize	3	I	6300ESB	CMOS	CPU, FWH	N/A, 3.3 V

†† Only supported by ICH4-M device. When not used, pull-up at CPU with 4.7 KΩ ± 5% resistor at VCCP.

4.1.5.1 Topology 1A: Open Drain (OD) Signals Driven by the Intel Pentium M/Celeron M Processor – IERR#

The Topology 1A OD signal IERR# shall adhere to the following routing and layout recommendations. Table 11 lists the recommended routing requirements for the IERR# signal of the Intel Pentium M/Celeron M processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/undershoot reflections on the transmission line. The pull-up voltage for termination resistor Rtt is VCCP (1.05 V). Due to the dependencies on system design implementation, IERR# may be implemented in a number of ways to meet design goals. IERR# may be routed as a test point or to any optional system receiver. Figure 16 depicts the routing illustration for Topology 1A.

Figure 16. Routing Illustration for Topology 1A

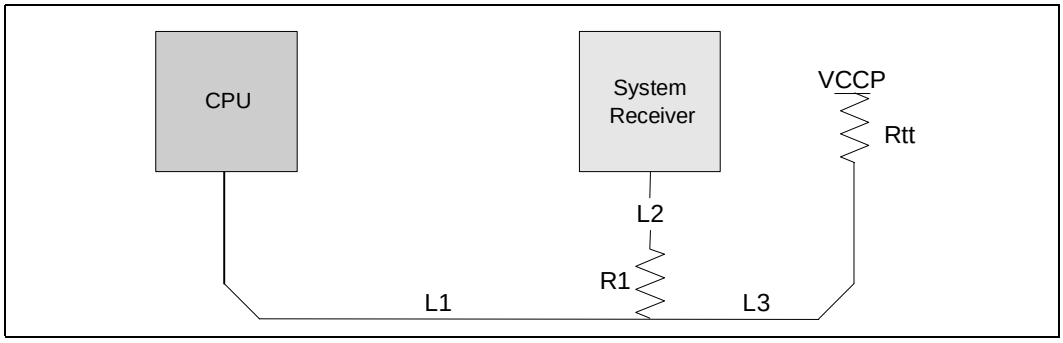


Table 11. Layout Recommendations for Topology 1A

L1	L2	L3	R1	Rtt	Transmission Line Type
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	56 Ω ± 5%	56 Ω ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	56 Ω ± 5%	56 Ω ± 5%	Strip-line

4.1.5.2 Topology 1B: Open Drain (OD) Signals Driven by the Intel Pentium M/Celeron M Processor – FERR# and THERMTRIP#

The Topology 1B OD signals FERR# and THERMTRIP# shall adhere to the following routing and layout recommendations. Table 12 lists the recommended routing requirements for the FERR# and THERMTRIP# signals of the Intel Pentium M/Celeron M processor. The routing guidelines allow the signals to be routed as either micro-strips or strip-lines using 55 Ω ± 15 percent characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/undershoot reflections on the transmission line. The pull-up voltage for termination resistor Rtt is VCCP (1.05 V).

Intel recommends that the FERR# signal of the Intel Pentium M/Celeron M processor be routed to the FERR# signal of the Intel® 6300ESB. THERMTRIP# may be implemented in a number of ways to meet design goals. It may be routed to the 6300ESB or any optional system receiver. It is recommended that the THERMTRIP# signal of the Intel Pentium M/Celeron M processor be routed to the THERMTRIP# signal of the 6300ESB. The 6300ESB's THERMTRIP# signal is a new signal to the I/O controller hub architecture that allows the 6300ESB to quickly put the whole system into a S5 state whenever the catastrophic thermal trip point has been reached.

When either FERR# or THERMTRIP# is routed to an optional system receiver rather than the 6300ESB and the interface voltage of the optional system receiver does not support a 1.05 V voltage swing, a voltage translation circuit must be used. When the recommended voltage translation circuit described in Section 4.1.5.7 is used, the driver isolation resistor shown in Figure 22, Rs, shall replace the series dampening resistor R1 in Topology 1B. Thus, R1 is no longer required in such a topology. Figure 17 depicts the routing illustration for Topology 1B.

Figure 17. Routing Illustration for Topology 1B

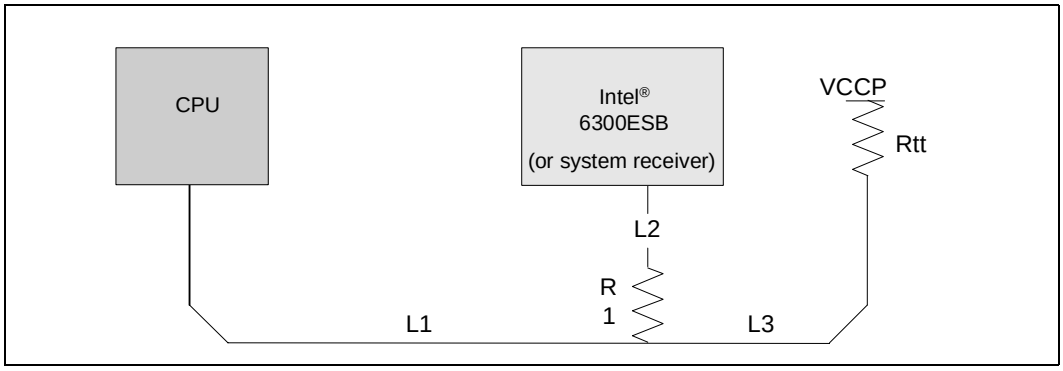


Table 12. Layout Recommendations for Topology 1B

L1	L2	L3	R1	Rtt	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	56 Ω ± 5%	56 Ω ± 5%	Micro-strip
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	56 Ω ± 5%	56 Ω ± 5%	Strip-line

4.1.5.3 Topology 1C: Open Drain (OD) Signals Driven by the Intel Pentium M/Celeron M Processor – PROCHOT#

The Topology 1C OD signal PROCHOT#, shall adhere to the following routing and layout recommendations. Table 13 lists the recommended routing requirements for the PROCHOT# signal of the Intel Pentium M/Celeron M processor. The routing guidelines allow the signal to be routed as either a micro-strip or strip-line using 55 Ω ± 15 percent characteristic trace impedance. Figure 18 depicts the recommended implementation for providing voltage translation between the Intel Pentium M/Celeron M processor’s PROCHOT# signal and a system receiver that utilizes a 3.3 V interface voltage (shown as V_IO_RCVR).

Series resistor Rs is a component of the voltage translation logic and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 22. Rs shall be placed at the beginning of the T-split from the PROCHOT# signal. The pull-up voltage for termination resistor Rtt is VCCP (1.05 V).

Intel recommends that PROCHOT# be routed using the voltage translation logic shown in Figure 18. The receiver at the output of the voltage translation circuit may be any system receiver that may function properly with the PROCHOT# signal given the nature and usage model of this pin. PROCHOT# is capable of toggling hundreds of times per second to signal a hot temperature condition.

Figure 18. Routing Illustration for Topology 1C

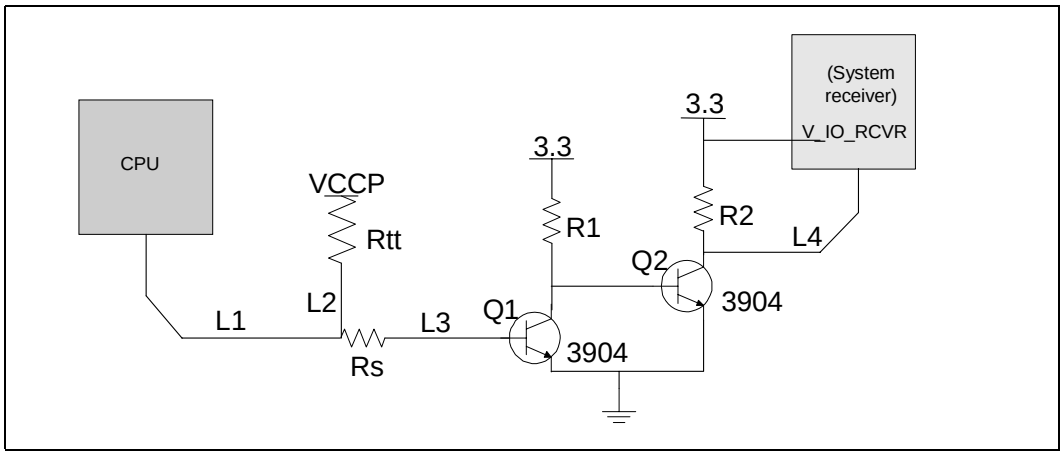


Table 13. Layout Recommendations for Topology 1C

L1	L2	L3	L4	Rs	R1	R2-	Rtt	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	0.5” – 12.0”	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	56 Ω ± 5%	Micro-strip
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	0.5” – 12.0”	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	56 Ω ± 5%	Strip-line

4.1.5.4 Topology 2A: Open Drain (OD) Signals Driven by AND Gate– PWRGOOD

The Topology 2A OD signal PWRGOOD, which is driven by an AND gate (Intel Pentium M/Celeron M processor CMOS signal input), shall adhere to the following routing and layout recommendations. Table 14 lists the recommended routing requirements for the PWRGOOD signal of the Intel Pentium M/Celeron M processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 55 Ω ± 15 percent characteristic trace impedance. The pull-up voltage for termination resistor Rtt is VCCP (1.05 V). Figure 19 depicts the routing illustration for Topology 2A.

Note: The output from the AND Gate (AND of power supply PWRGD_3V and CPU VR__PWRGD) shall be routed point-to-point to the Intel Pentium M/Celeron M processor’s PWRGOOD signal. The routing from the Intel Pentium M/Celeron M processor’s PWRGOOD pin shall fork out to the termination resistor, Rtt, and the AND gate. Segments L1 and L2 from Table 14 shall not T-split from a trace from the Intel Pentium M/Celeron M processor pin.

Figure 19. Routing Illustration for Topology 2A

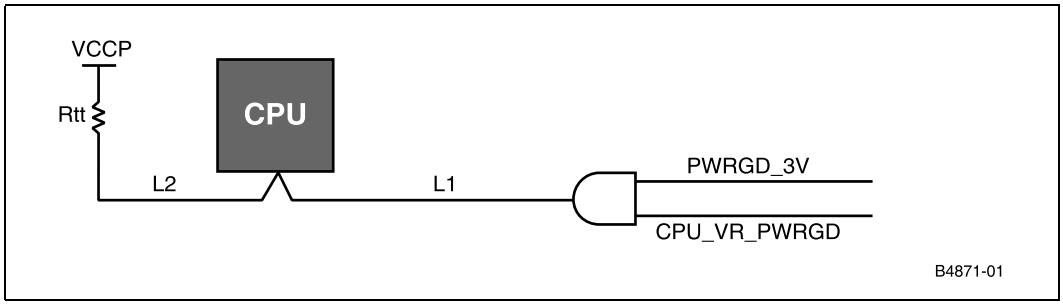


Table 14. Layout Recommendations for Topology 2A

L1	L2	Rtt	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	330 Ω ± 5%	Micro-strip
0.5” – 12.0”	0” – 3.0”	330 Ω ± 5%	Strip-line

4.1.5.5 Topology 2B: CMOS Signals Driven by 6300ESB-LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK#

The Topology 2B CMOS LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK# signals shall implement a point-to-point connection between the 6300ESB and the Intel Pentium M/Celeron M processor. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 55 Ω ± 15 percent characteristic trace impedance. No additional motherboard components are necessary for this topology. Figure 20 depicts the routing illustration and Table 15 presents the layout recommendations for Topology 2B.

Figure 20. Routing Illustration for Topology 2B

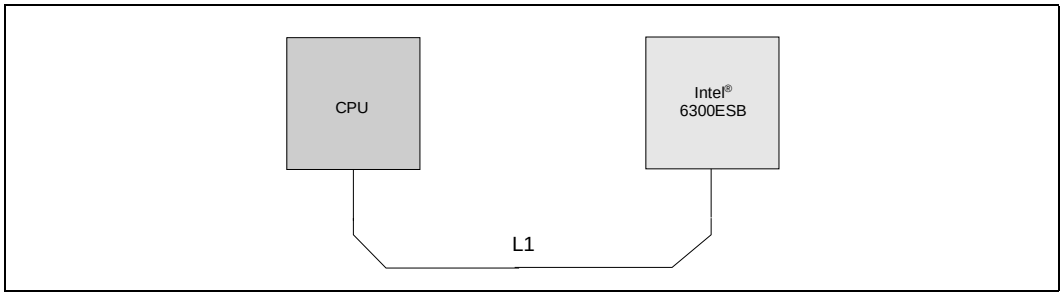


Table 15. Layout Recommendations for Topology 2B

L1	Transmission Line Type
0.5” – 12.0”	Micro-strip
0.5” – 12.0”	Strip-line

4.1.5.6 Topology 3: CMOS Signals Driven by 6300ESB to CPU and FWH – INIT#

The signal INIT# shall adhere to the following routing and layout recommendations. Table 16 lists the recommended routing requirements for the INIT# signal of the 6300ESB. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 55 Ω ± 15 percent characteristic trace impedance. Figure 21 depicts the recommended implementation for providing voltage translation between the 6300ESB’s INIT# voltage signaling level and any firmware hub (FWH) that utilizes a 3.3 V interface voltage (shown as a supply V_IO_FWH). Refer to Section 4.1.5.7 for more details on the voltage translator circuit. For convenience, the entire topology and required transistors and resistors for the voltage translator are shown in Figure 21.

Series resistor Rs is a component of the voltage translator logic circuit and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance of L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 22. The routing recommendations of transmission line L3 in Figure 21 are listed in Table 16. Rs must be placed at the beginning of the T-split of the trace from 6300ESB’s INIT# pin.

Figure 21. Routing Illustration for Topology 3

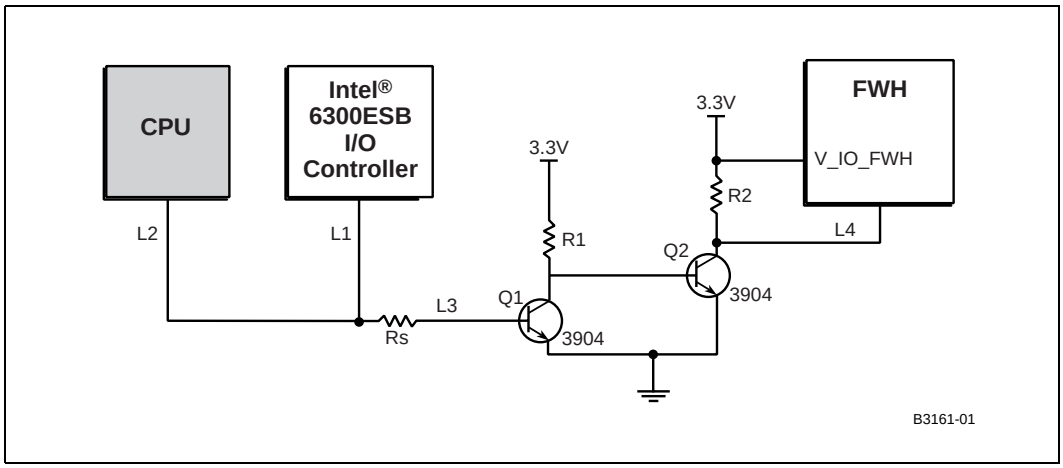


Table 16. Layout Recommendations for Topology 3

L1 + L2	L3	L4	Rs	R1	R2	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	0.5” – 6.0”	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	Micro-strip
0.5” – 12.0”	0” – 3.0”	0.5” – 6.0”	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	Strip-line

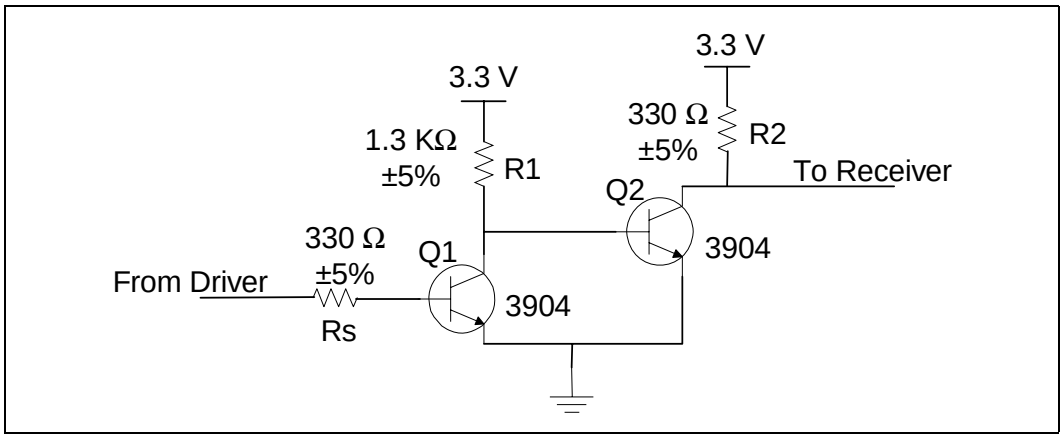
4.1.5.7 Voltage Translation Logic

A voltage translation circuit or component is required on any signals where the voltage signaling level between two components connected by a transmission line may cause unpredictable signal quality. The recommended voltage translation circuit for the platform is shown in Figure 22. For the INIT# signal (Section 4.1.5.6), a specialized version of this voltage translator circuit is used where the driver isolation resistor, Rs, is place at the beginning of a transmission line that connects to the first bipolar junction transistor, Q1. Though the circuit shown in Figure 22 was developed to work with signals that require translation from a 1.05 V to a 3.3 V voltage level, the same topology and component values, in general, may be adapted for use with other signals as well, provided the interface voltage of the receiver is also 3.3 V. Any component value changes or component placement requirements for other signals must be simulated in order to ensure good signal quality and acceptable performance from the circuit.

In addition to providing voltage translation between driver and receiver devices, the recommended circuit also provides filtering for noise and electrical glitches. A larger first-stage collector resistor, R1, may be used on the collector of Q1, however, it results in a slower response time to the output falling edge. In the case of the INIT# signal, resistors with values as close as possible to those listed in Figure 22 shall be used without exception.

With the low 1.05 V signaling level of the Intel Pentium M/Celeron M processor system bus, the voltage translation circuit provides ample isolation of any transients or signal reflections at the input of transistor Q1 from reaching the output of transistor Q2. Based on simulation results, the voltage translation circuit may effectively isolate transients as large as 200 mV and that last as long as 60 ns.

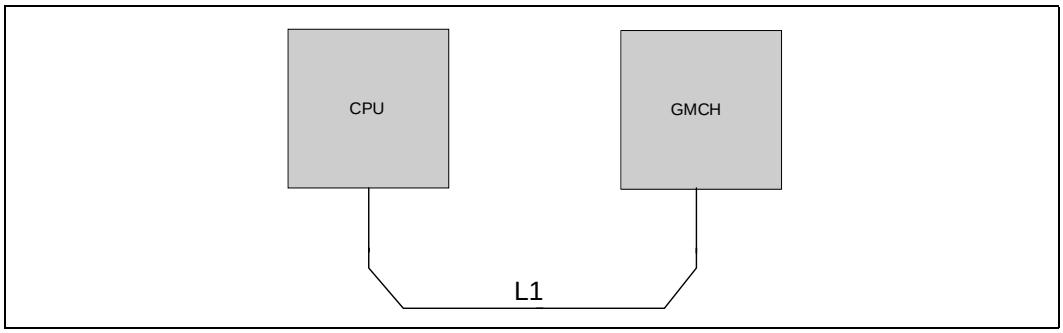
Figure 22. Voltage Translation Circuit



4.1.6 Pentium® M/Celeron® M Processor RESET# Signal

The RESET# signal is a common clock signal driven by the GMCH CPURESET# pin. In a production system where no ITP700FLEX debug port is implemented, a simple point-to-point connection between the CPURESET# pin of the GMCH and the Intel Pentium M/Celeron M processor's RESET# pin is recommended (see Figure 23). On-die termination of the AGTL+ buffers on both the processor and the GMCH provide proper signal quality for this connection. This is the same case as for the other common clock signals listed Section 4.1.2. Length L1 of this interconnect shall be limited to minimum of 1 inch and maximum of 6.5 inches.

Figure 23. Processor RESET# Signal Routing Topology With NO ITP700FLEX Connector



For a system that implements an ITP700FLEX debug port a more elaborate topology is required to ensure proper signal quality at both the processor signal pad and the ITP700FLEX input receiver. In this case the topology illustrated in Figure 24 shall be implemented. The CPURESET# signal from the GMCH shall fork out (do not route one trace from GMCH pin and then T-split) towards the processor's RESET# pin as well as toward the Rtt and Rs resistive termination network placed next to the ITP700FLEX debug port connector. Rtt (220 Ω + 5 percent) pulls-up to the VCCP voltage and is placed at the end of the L2 line that is limited to a 6-inch maximum length.

Rs (22.6 Ω ± 1 percent) must be placed right next to Rtt to minimize routing between them in the vicinity of the ITP700FLEX connector to limit the L3 length to less than 0.5 inches. ITP700FLEX operation requires the matching of L2 + L3 - L1 length to the length of the BPM[4:0]# signals length within ± 50 ps. See Section 4.3 for more details on ITP700FLEX signal routing and Section 4.1.1.4 for more details on signal propagation time to distance correlation. See Table 17 for routing length summary and termination resistor values.

Figure 24. Processor RESET# Signal Routing Topology With ITP700FLEX Connector

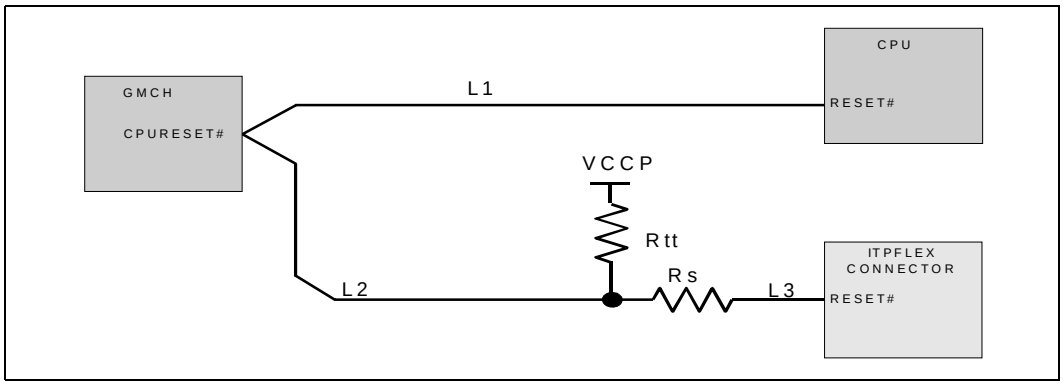


Table 17. Processor RESET# Signal Routing Guidelines with ITP700FLEX Connector

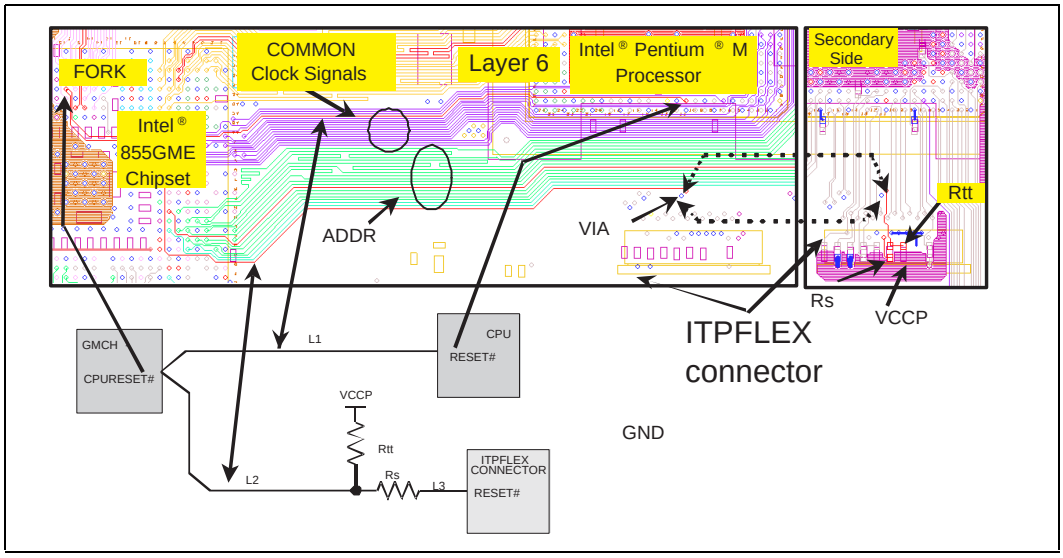
L1	L2 + L3	L3	Rs	Rtt
1.0” – 6.0”	6.0” max	0.5” max	Rs = 22.6 Ω ± 1%	Rtt = 220 ± 5%

4.1.6.1 Processor RESET# Routing Example

Figure 25 illustrates a board routing example for the RESET# signal with an ITP700FLEX debug port implemented. Figure 25 illustrates how the CPURST# pin of GMCH forks out into two branches on Layer 6 of the motherboard. One branch is routed directly to the Intel Pentium M/Celeron M processor RESET# pin among the rest of the common clock signals. Another branch routes below the address signals and vias down to the secondary side that route to the Rs and Rtt resistors. These resistors are placed in the vicinity of the ITP700FLEX debug port.

Note: The placement of Rs and Rtt next to each other is to minimize the routing between Rs and Rtt as well as the minimal routing between Rs and the ITP700FLEX connector. Also, because a transition between Layer 6 and the secondary side occurs, a GND stitching via is added to ensure continuous ground reference of the secondary side routing of the RESET# signal to ITP700FLEX connector.

Figure 25. Processor RESET# Signal Routing Example with ITP700FLEX Debug Port

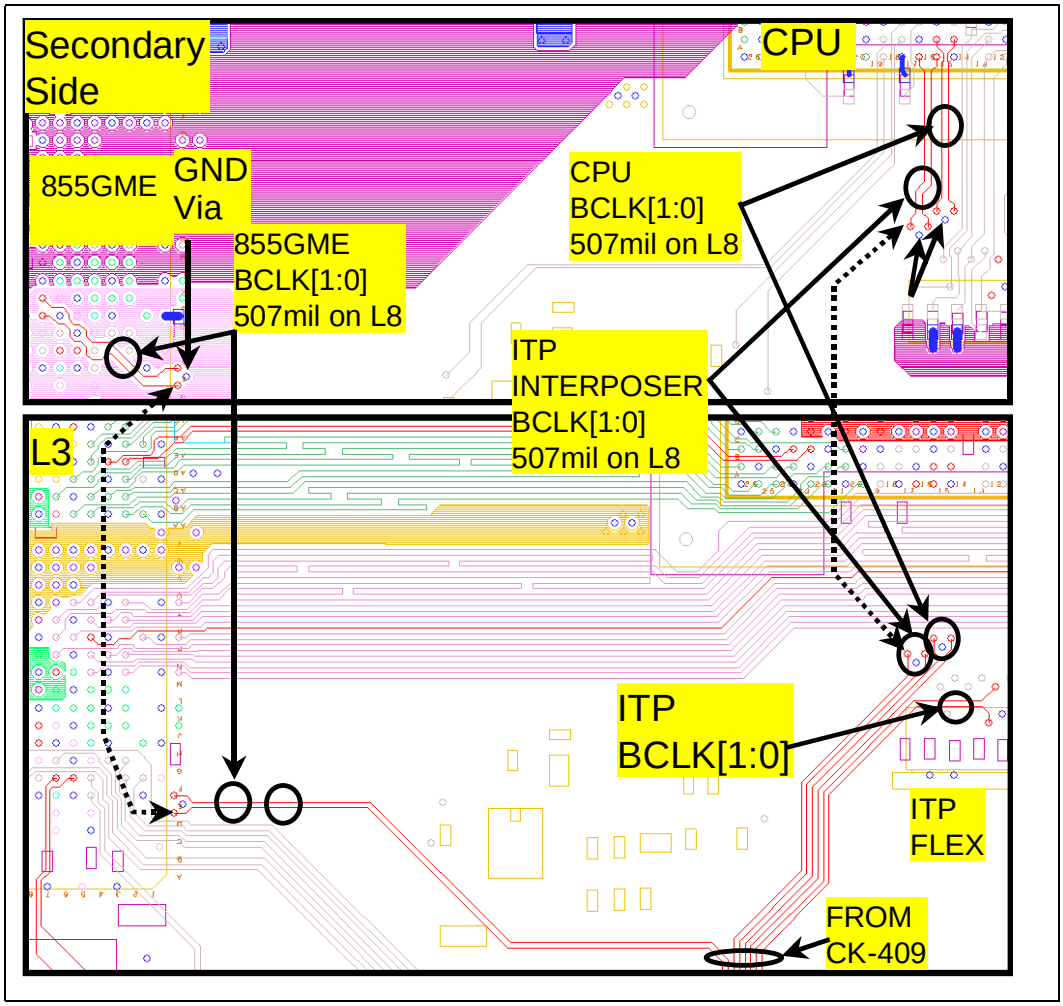


4.1.7 Pentium® M/Celeron® M Processor and Intel 855GME Chipset GMCH (82855GME) Host Clock Signals

Figure 26 illustrates Intel Pentium M/Celeron M processor and 82855GME host clock signal routing. Both the Intel Pentium M/Celeron M processor and the GMCH's BCLK[1:0] signals are initially routed from the CK409 clock generator on Layer 3. In the recommended routing example (Figure 26) secondary side layer routing of BCLK[1:0] is 507 mils long. To meet length-matching requirements between the Intel Pentium M/Celeron M processor and GMCH's BCLK[1:0] signals, a similar transition from Layer 3 to the secondary side layer is done next to the Intel 855GME chipset package outline. Routing of the GMCH's BCLK[1:0] signals on the secondary side is also trace tuned to 507 mils. BCLK[1:0] layer transition vias are accompanied by GND stitching vias. For similar reasons, routing for the ITP interposer's BCLK[1:0] signals also transition from Layer 3 to the secondary side layer and have 507-mil long traces on this layer. Throughout the routing length on Layer 3, BCLK[1:0] signals shall reference a solid GND plane on Layer 2 and Layer 4 as shown in Figure 11.

When a system supports either the onboard ITP700FLEX connector or ITP Interposer only, differential host clock routing to either the ITP700FLEX connector or CPU socket (but not both) is required.

Figure 26. Intel® Pentium® M/Celeron® M Processor and Intel® 855GME Chipset GMCH (82855GME) Host Clock Layout Routing Example



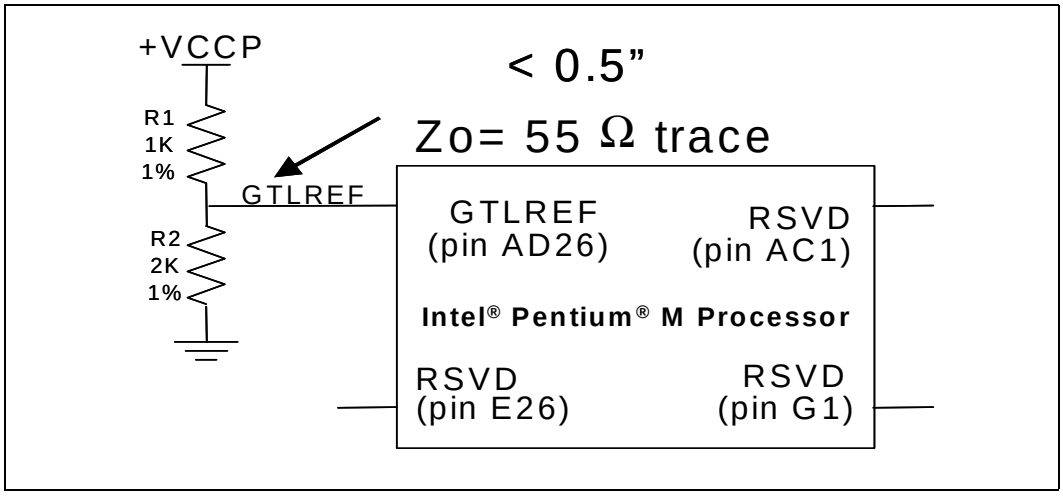
4.1.8 Pentium® M/Celeron® M Processor GTLREF Layout and Routing Recommendations

There is one AGTL+ reference voltage pin on the Intel Pentium M/Celeron M processor, GTLREF, which is used to set the reference voltage level for the AGTL+ signals (GTLREF). The reference voltage must be supplied to the GTLREF pin. The voltage level that needs to be supplied to GTLREF must be equal to 2/3 * VCCP ± 2%. The GMCH also requires a reference voltage (MCH_GTLREF) to be supplied to its HVREF[4:0] pins. The GTLREF voltage divider for both the Intel Pentium M/Celeron M processor and GMCH cannot be shared. Thus, both the processor and GMCH must have their own locally generated GTLREF networks. Figure 27 depicts the recommended topology for generating GTLREF for the Intel Pentium M/Celeron M processor using a R1 = 1 kΩ ± 1% and R2 = 2 kΩ ± 1% resistive divider.

Because the input buffer trip point is set by the 2/3*VCCP on GTLREF to allow tracking of VCCP voltage fluctuations, **no** decoupling shall be placed on the GTLREF pin. The node between R1 and R2 (GTLREF) shall be connected to the GTLREF pin of the Intel Pentium M/Celeron M processor with Zo = 55 Ω trace shorter than 0.5 inches. Space any other switching signals away from GTLREF with a minimum separation of 25 mils. Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the Intel Pentium M/Celeron M processor system bus signals).

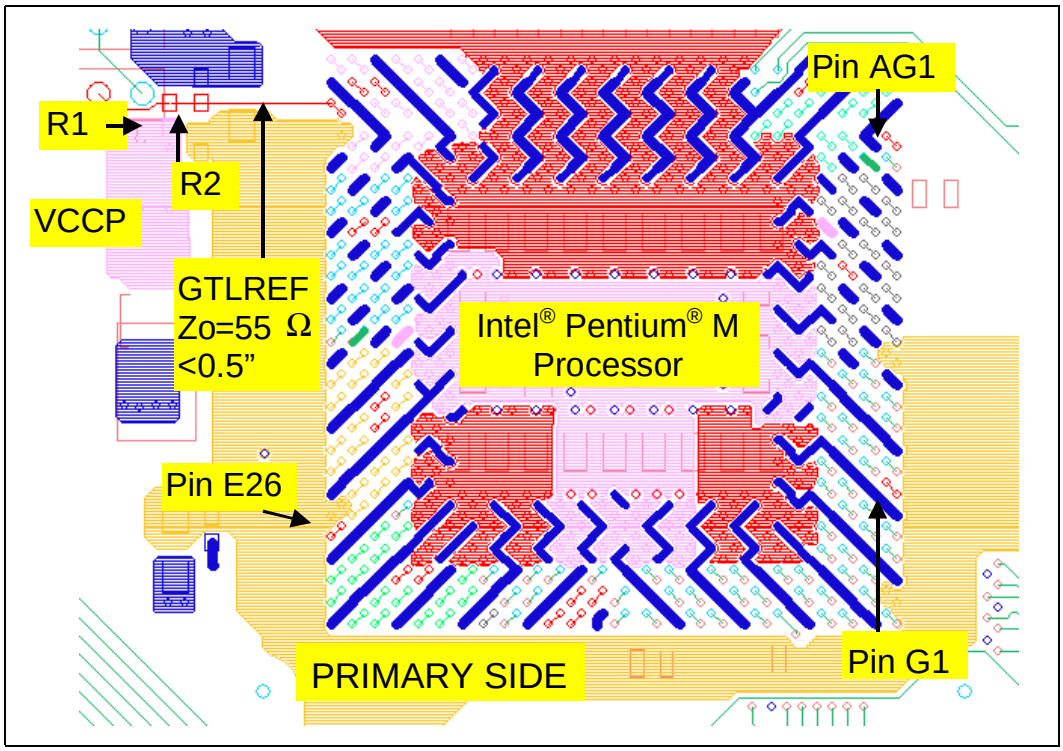
Previous revisions of design guides and the Intel Pentium M/Celeron M processor pin-map contained references to three additional pins devoted to the delivery of the GTLREF reference voltage to the package. These three pins have been renamed into RSVD pins and are required to be left as no connects on the platform. RSVD signal pins E26, G1, and AC1 are to be left unconnected on Intel Pentium M/Celeron M processor-based systems.

Figure 27. Intel® Pentium® M/Celeron® M Processor GTLREF Voltage Divider Network



A recommended layout of GTLREF for the Intel Pentium M/Celeron M processor is shown in Figure 28. To avoid interaction with Intel Pentium M/Celeron M processor FSB routing and power delivery, GTLREF's R1 and R2 components are placed next to each other on the primary side of the motherboard and connected with a Zo = 55 Ω, 370 mil long trace to the GTLREF pin on the Intel Pentium M/Celeron M processor, which meets the 0.5-inch maximum length requirement. The BGA ball lands on the primary side for the RSVD signal pins E26, G1, and AC1 are shown for illustrative purposes and are not routed.

Figure 28. Intel® Pentium® M/Celeron® M Processor GTLREF Motherboard Layout



4.1.9 AGTL+ I/O Buffer Compensation

The Intel Pentium M/Celeron M processor has four pins, COMP[3:0], and the GMCH has two pins, HRCOMP[1:0], that require compensation resistors to adjust the AGTL+ I/O buffer characteristics to specific board and operating environment characteristics. The GMCH requires two special reference voltage generation circuits to pins HSWNG[1:0] for the same purpose described above. Refer to the *Intel Pentium® M Processor Datasheet*, *Intel Celeron® M Datasheet*, *Intel Pentium® M Processor on 90nm Process with 2MB L2 Cache Datasheet* and *Intel® 855GM/855GME Chipset (GMCH) Datasheet* for details on resistive compensation.

4.1.9.1 Pentium® M/Celeron® M Processor AGTL+ I/O Buffer Compensation

For the Intel Pentium M/Celeron M processor, the COMP[2] and COMP[0] pins (see Figure 29) each must be pulled-down to ground with 27.4 Ω ± 1% resistors and shall be connected to the Intel Pentium M/Celeron M processor with a Zo = 27.4 Ω trace that is less than 0.5 inches from the processor pins. The COMP[3] and COMP[1] pins (see Figure 30) each must be pulled-down to ground with 54.9 Ω ± 1% resistors and shall be connected to the Intel Pentium M/Celeron M processor with a Zo = 55 Ω trace that is less than 0.5 inches from the processor pins. COMP[3:0] traces shall be at least 25 mils (> 50 mils preferred) away from any other toggling signal.

Figure 29. Intel® Pentium® M/Celeron® M Processor COMP[2] and COMP[0] Resistive Compensation

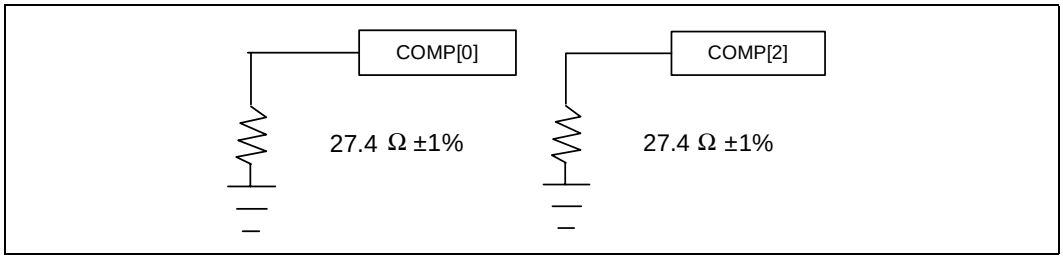
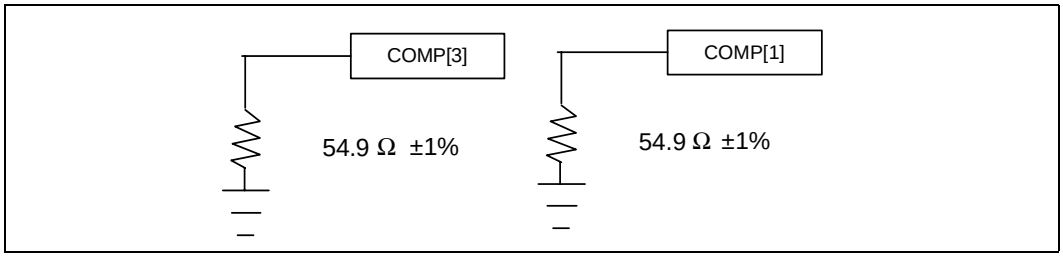


Figure 30. Intel® Pentium® M/Celeron® M ProcessorCOMP[3] and COMP[1] Resistive Compensation



The recommended layout of the Intel Pentium M/Celeron M processor COMP[3:0] resistors is illustrated in Figure 31. To avoid interaction with Intel Pentium M/Celeron M processor FSB routing on internal layers and VCCA power delivery on the primary side, Layer 1, COMP[1:0] resistors are placed on the secondary side. Ground connections to the COMP[1:0] resistors use a small ground flood on the secondary side layer and connect only with a single GND via to stitch the GND planes. The compact layout as shown in Figure 31 shall be used to avoid excessive perforation of the V_{CCP} plane power delivery. Figure 31 illustrates how a 27.4 Ω resistor connects with an ~18 mil wide (Zo = 27.4 Ω) and 160 mil long trace to COMP0. Necking down to 14 mils is allowed for a short length to pass in between the dog bones. The 54.9 Ω resistor connects with a regular 5 mil wide (Zo = 55 Ω) and 267 mil long trace to COMP1. Placement of COMP[1:0] on the primary side is possible as well. An alternative placement implementation is shown in Figure 32.

To minimize motherboard space usage and produce a robust connection, the COMP[3:2] resistors are also placed on the secondary side (Figure 31, right side). A 27.4 Ω resistor connects with an 18 mil wide (Zo = 27.4 Ω) and 260 mil long trace to COMP2. Necking down to 14 mils is allowed for a short length to pass in between the dog bones. Notice that the COMP2 (Figure 31, left side) dog bone trace connection on the primary side is also widened to 14 mils to meet the Zo = 27.4 Ω characteristic impedance target. The right side of Figure 31 also illustrates how the 54.9 Ω ± 1% resistor connects with a regular 5 mil wide (Zo = 55 Ω) and 100 mil long trace to COMP3. The ground connection of COMP[3:2] is done with a small flood plane on the secondary side that connects to the GND vias of pins AA1 and Y2 of the Intel Pentium M/Celeron M processor pin-map. This is done to avoid via interaction with the Intel Pentium M/Celeron M processor FSB routing on Layer 3 and Layer 6.

For COMP2 and COMP0, it is extremely important that 18 mil wide dog bone connections on the primary side and 18-mil wide traces on the secondary sides be used to connect the signals to compensation resistors on the secondary side, as shown in Figure 33. The 18-mil wide dog bones and traces are used to achieve the Zo = 27.4 Ω target to ensure proper operation of the Intel Pentium M/Celeron M processor FSB. Refer to Figure 29 for more details.

Figure 31. Intel® Pentium® M/Celeron® M Processor COMP[3:0] Resistor Layout

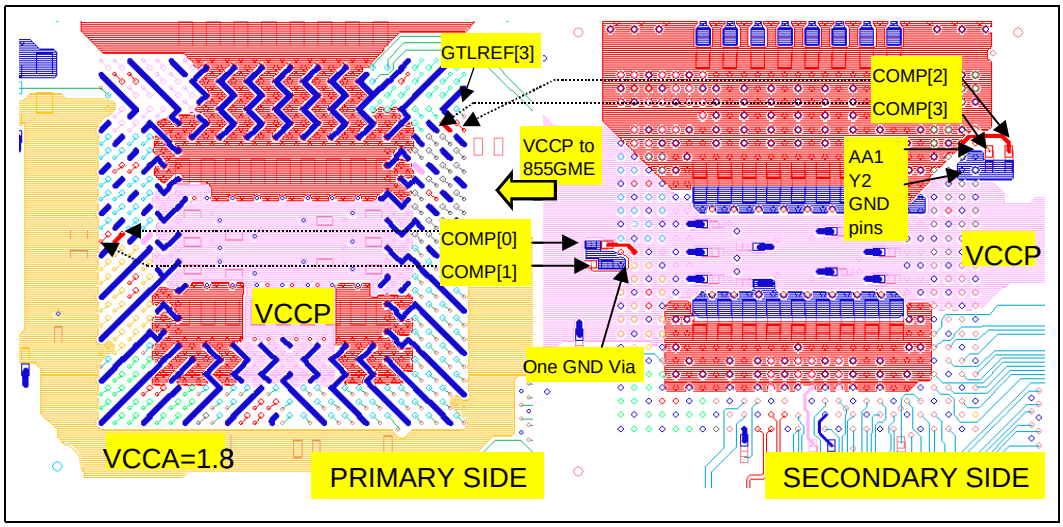


Figure 32. Intel® Pentium® M/Celeron® M Processor COMP[1:0] Resistor Alternative Primary Side Layout

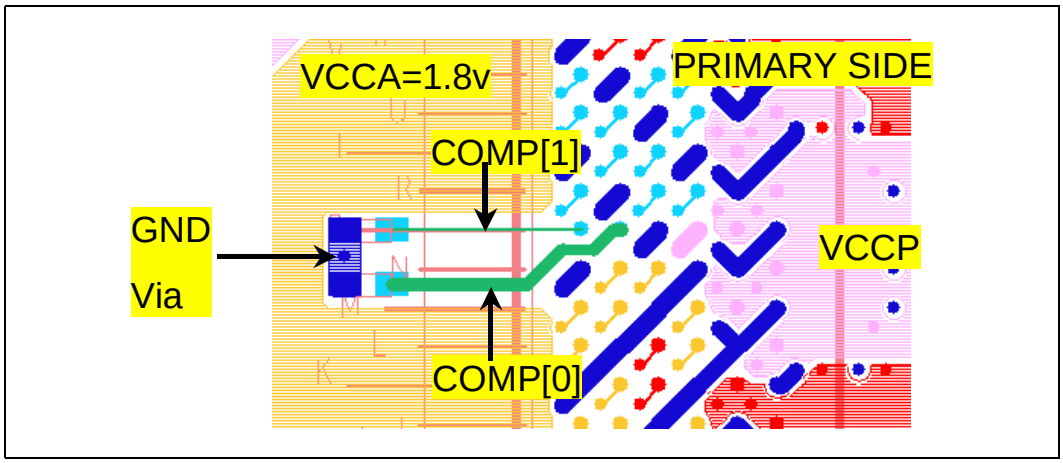
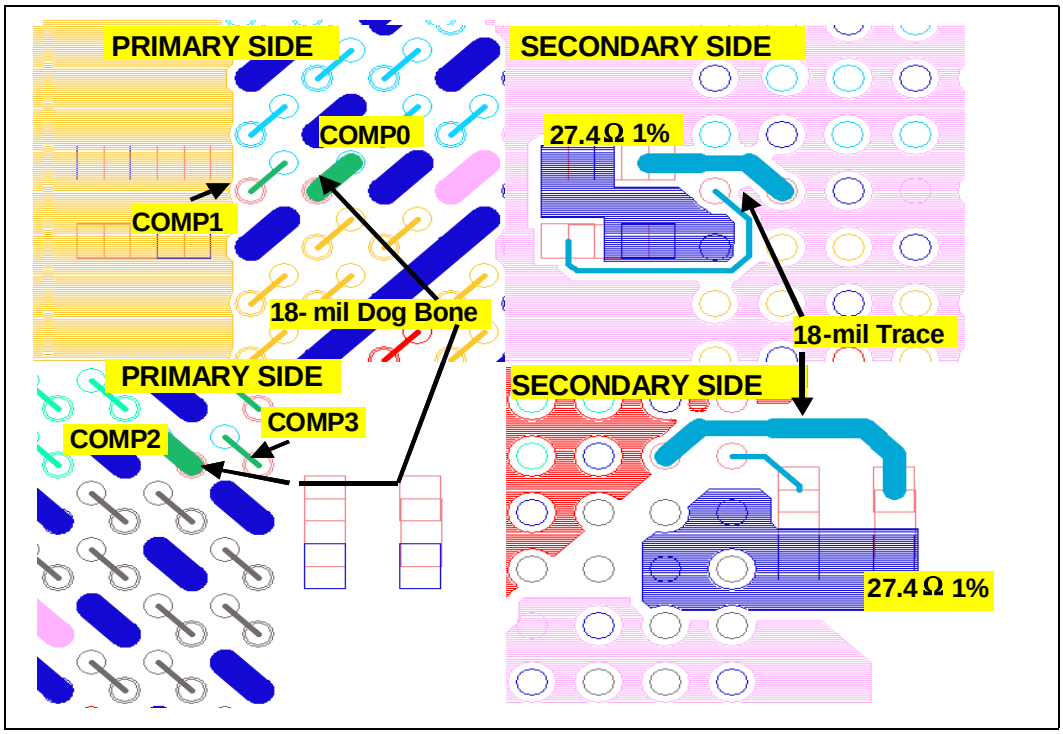


Figure 33. COMP2 and COMP0 18-mil Wide Dog Bones and Traces



4.1.10 Pentium® M/Celeron® M Processor System Bus Strapping

The Intel Pentium M/Celeron M processor and GMCH both have pins that require termination for proper component operation.

For the Intel Pentium M/Celeron M processor, a stuffing option shall be provided for the TEST[3] pin to allow a 1 kΩ ±5 percent pull-down to ground for testing purposes. For proper processor operation, the resistor shall not be stuffed. Resistors for the stuffing option on these pins shall be placed within 2.0 inches of the Intel Pentium M/Celeron M processor. Figure 2 illustrates the recommended layout for the stuffing options. For normal operation, these resistors shall not be stuffed.

The Intel Pentium M/Celeron M processor's ITP signals, TDI, TMS, TRST and TCK shall assume default logic values even if the ITP debug port is not used. The TDO signal may be left open or no connect in this case. Table 18 summarizes the default strapping resistors for these signals. These resistors shall be connected to the Intel Pentium M/Celeron M processor within 2.0 inches from their respective pins.

Note: Table 18 is applicable only when neither the onboard ITP nor ITP interposer are planned to be used. Refer to Section 4.2.2 on cautions against designs with lack of debug tools support. Intel does not recommend use of the ITP interposer debug port if there is a dependence only on the motherboard termination resistors.

The signals below shall be isolated from the motherboard via specific termination resistors on the ITP interposer itself according to interposer debug port recommendations. For the case where the onboard ITP700FLEX debug port is used, refer to Section 4.3 for default termination recommendations.

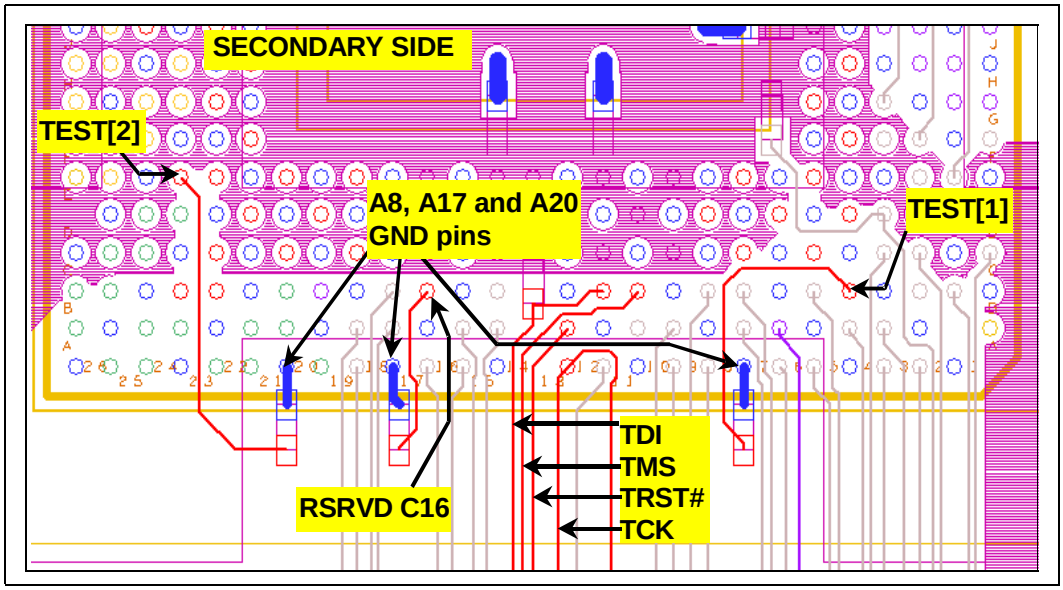
Table 18. ITP Signal Default Strapping When ITP Debug Port Not Used

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 Ω ± 5%	VCCP	Within 2.0" of the CPU
TMS	39 Ω ± 5%	VCCP	Within 2.0" of the CPU
TRST#	680 Ω ± 5%	GND	Within 2.0" of the CPU
TCK	27 Ω ± 5%	GND	Within 2.0" of the CPU
TDO	Open	NC	N/A

Figure 34 illustrates the recommended layout for the Intel Pentium M/Celeron M processor's strapping resistors. To avoid interaction with Intel Pentium M/Celeron M processor FSB routing, the TEST[2:1] and RSVD (pin C16) signal resistors are placed on the secondary side of the motherboard. To avoid GND via interaction with the Intel Pentium M/Celeron M processor FSB routing, the resistors share GND via connections with the A8, A17, and A20 ground pins of the Intel Pentium M/Celeron M processor.

The 150 Ω, pull-up resistor to V_{CCP} (1.05 V) for TDI is shown in Figure 34 on the secondary side of the board. The placement of the strapping resistors for TDI, TMS, TRST#, and TCK is not critical.

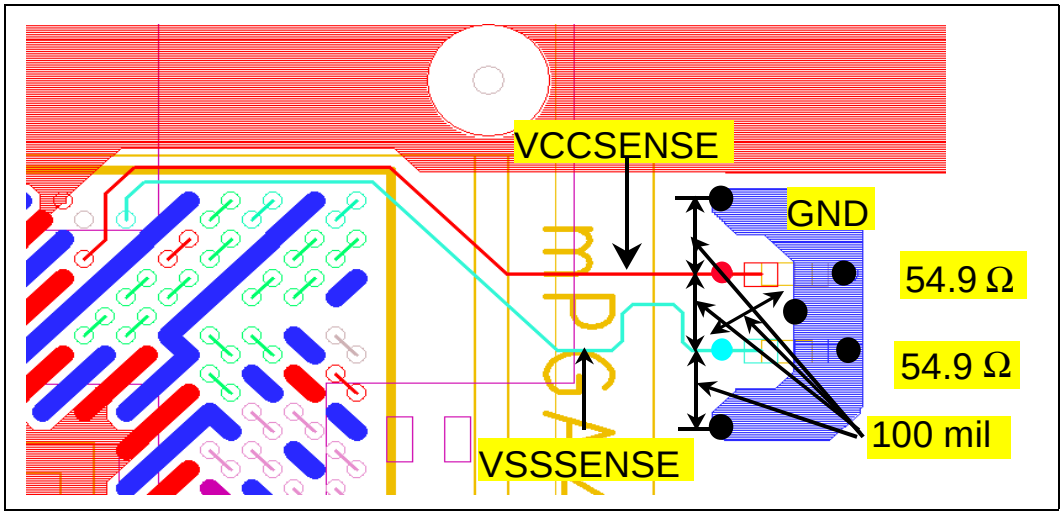
Figure 34. Intel® Pentium® M/Celeron® M Processor Strapping Resistor Layout



4.1.11 Pentium® M/Celeron® M Processor $V_{CCSENSE}/V_{SSSENSE}$ Design Recommendations

The VCCSENSE and VSSSENSE signals of the Intel Pentium M/Celeron M processor provide isolated, low impedance connections to the processor's core power (VCC) and ground (VSS). These pins may be used to sense or measure power (VCC) or ground (VSS) near the silicon with little noise. To make them available for measurement purposes, it is recommended that VCCSENSE and VSSSENSE both be routed with a Zo = 55 Ω ± 15 percent trace of equal length. Use 3:1 spacing between the routing for the two signals and all other signals shall be a minimum of 25 mils (preferably 50 mils) from VCCSENSE and VSSSENSE routing. Terminate each line with an optional (default is No Stuff) 54.9 Ω ± 1 percent resistor. Also, a ground via spaced 100 mils away from each of the test point vias for VCCSENSE and VSSSENSE shall be added. A third ground via shall also be placed in between them to allow for a differential probe ground. Refer to Figure 35 for the recommended layout example.

Figure 35. $V_{CCSENSE}/V_{SSSENSE}$ Routing Example



4.1.12 PLL Voltage Design for Low Voltage Intel® Pentium® M Processors on 90 nm process with 2 MB L2 Cache

One primary difference between the Intel Pentium M processor (130nm) and the Low Voltage Intel® Pentium® M Processor on 90 nm process with 2 MB L2 cache or the Intel® Celeron® M Processor on 90nm process is the analog PLL voltage supplying the processor's on-die clock generators. The VCCA PLL power delivery pins of the Low Voltage Intel Pentium M Processors on 90 nm process with 2 MB L2 cache and the Intel® Celeron® M Processor on 90nm process have the option of using either a 1.8 V or 1.5 V power supply. For a platform supporting only Low Voltage Intel Pentium M Processors on 90 nm process with 2 MB L2 cache or Intel® Celeron® M Processor on 90nm process, the VCCA[3:0] pin should be powered by the 1.5 V rail, since the 1.5 V rail is already required for GMCH. This eliminates the need for a 1.8 V rail on the platform. However, if a platform is to also support Intel Pentium M processors (130nm) and standard voltage Intel® Pentium® M Processors on 90 nm process with 2 MB L2 cache, then the 1.8 V rail must be used for the analog PLL voltage supply.

4.2 Intel System Validation Debug Support

In any design, it is critical to enable industry-standard tools to allow for debugging a wide range of issues that come up in the normal design cycle. In embedded designs, electrical/logic visibility is very limited, often making progress on debugging such issues very time consuming. In some cases progress it not possible without board re-design or extensive rework. Two topics in particular are very important to general system debug capabilities.

4.2.1 ITP Support

4.2.1.1 Background/Justification

One key tool that is needed to debug BIOS, logic, signal integrity, general software, and general hardware issues involving CPUs, chipsets, SIOs, PCI devices, and other hardware in a platform design is the In Target Probe (ITP). The ITP is widely used by various validation, test, and debug groups within Intel (as well as by third party BIOS vendors, OEMs, and other developers).

Note: It is extremely important that any Intel Pentium M/Celeron M processor/Intel 855GME chipset-based systems designed without ITP support may prevent assistance from various Intel validation, test, and debug groups in debugging various issues. For this reason, it is critical that ITP support is provided. This may be done with zero additional BOM cost and minimal layout/footprint costs.

The cost for not providing this support may be anywhere from none, if there are no blocking issues found in the system design, to schedule slips of a month or more. The latter scenario represents the time needed to spin a board design and required assembly time to add an ITP port when absolutely required and other mechanical and routing issues prevent the use of an ITP interposer, if one exists.

4.2.1.2 Implementation

To minimize the ITP connector footprint, the ITP700Flex alternative is a better option for embedded designs. The termination values do not need to be stuffed, thus zero additional BOM cost. However, standard signal connection guidelines for the CPU's TAP logic signals for the non-ITP case still need to be followed. In other words, only the traces and component footprints need to be added to the design, with all previous non-ITP guidelines followed otherwise. This way, when ITP support is needed, the termination values and connector may be populated as needed for debug support.

Note: When the ITP700Flex footprint cannot be followed due to mechanical, routing, or footprint reasons, it is acceptable to have a simple via grouping in lieu of the connector to allow for 'blue-wiring' of the ITP.

4.2.2 Pentium® M/Celeron® M Processor Logic Analyzer Support (FSB LAI)

4.2.2.1 Background/Justification

The second key tool (other than the ITP) that is needed to debug BIOS, logic, signal integrity, general software, and general hardware issues involving CPUs, chipsets, SIOs, PCI devices, and other hardware in platform design is the Intel Pentium M/Celeron M processor FSB Logic Analyzer probe. This critical tool is widely used by various validation, test, and debug groups within Intel as well as by third party BIOS vendors, OEMs, and other developers. For the Intel Pentium M/Celeron M processor, Agilent* Corporation has developed this tool and provides the only visibility to this critical system bus.

Note: **It is extremely important that any Intel Pentium M/Celeron M processor/Intel 855GME chipset-based systems designed without Intel Pentium M/Celeron M processor FSB LAI support may severely limit the ability of various Intel validation, test, and debug groups from debugging various issues in a reasonable amount of time. For this reason, it is very critical that Pentium® M/Celeron® M Processor FSB LAI support is provided.**

There are two primary pieces to providing this support:

1. Providing a motherboard with a CPU socket. The Intel Pentium M/Celeron M processor FSB LAI is an interposer that plugs into the CPU socket, and the CPU then plugs into the logic analyzer. The use of non-standard sockets may also prohibit the logic analyzer from working as the locking mechanism may become inaccessible. It is important to check the logic analyzer design guidelines to ensure a particular socket will work. The logic analyzer was designed to accommodate the most common (and at the time, the only known) Intel Pentium M/Celeron M processor sockets on the market.
2. Observing Intel Pentium M/Celeron M processor FSB LAI keepout requirements. There are several options to achieve this. For example, removing the motherboard from the case (typically the first step to meeting keepout requirements) or relocating any components that would otherwise be in the keepout area for debug purposes (i.e., axial lead devices that can be de-soldered and re-soldered to the other side of the board, parts that can be removed and blue-wired further away, etc.). When keepouts still cannot be met, Intel strongly recommends that a separate debug motherboard be built that has the same bill of materials (BOM) and Netlist, but with Intel Pentium M/Celeron M processor FSB LAI keepout requirements met (this also gives the opportunity to add other test-points).

4.2.2.2 Implementation

Details from Agilent Corporation on the Intel Pentium M/Celeron M processor FSB LAI mechanicals (i.e., design guide with keepout volume information) are available for ordering. Contact your local Intel field representative to obtain the latest design information. Refer to Section 4.3.3 for more details.

4.2.3 Intel® Pentium® M/Celeron® M Processor On-Die Logic Analyzer Trigger (ODLAT) Support

The Intel Pentium M/Celeron M processor provides support for three address/data recognizers on-die for setting on-die logic analyzer triggers (ODLAT) or breakpoints. Details from American Arium* on the ODLAT are currently available for ordering.

4.3 Onboard Debug Port Routing Guidelines

In Intel Pentium M/Celeron M processor-based systems, the debug port should be implemented as either an onboard debug port or via an interposer. Refer to the *ITP700FLEX Debug Port Design Guide*, which may be found on http://developer.intel.com/design/Xeon/guides for the design of your platform.

Note: When any differences exist between the general information of the *ITP700 Debug Port Design Guide* reference document and this design guide, the implementation recommended in this design guide takes precedence and should be followed. Specifically, the implementation for the TDO, RESET#, and BPM[5:0]# signals on the Intel Pentium M/Celeron M processor does differ from the default ITP debug port recommendations. The changes described below should be adhered to closely.

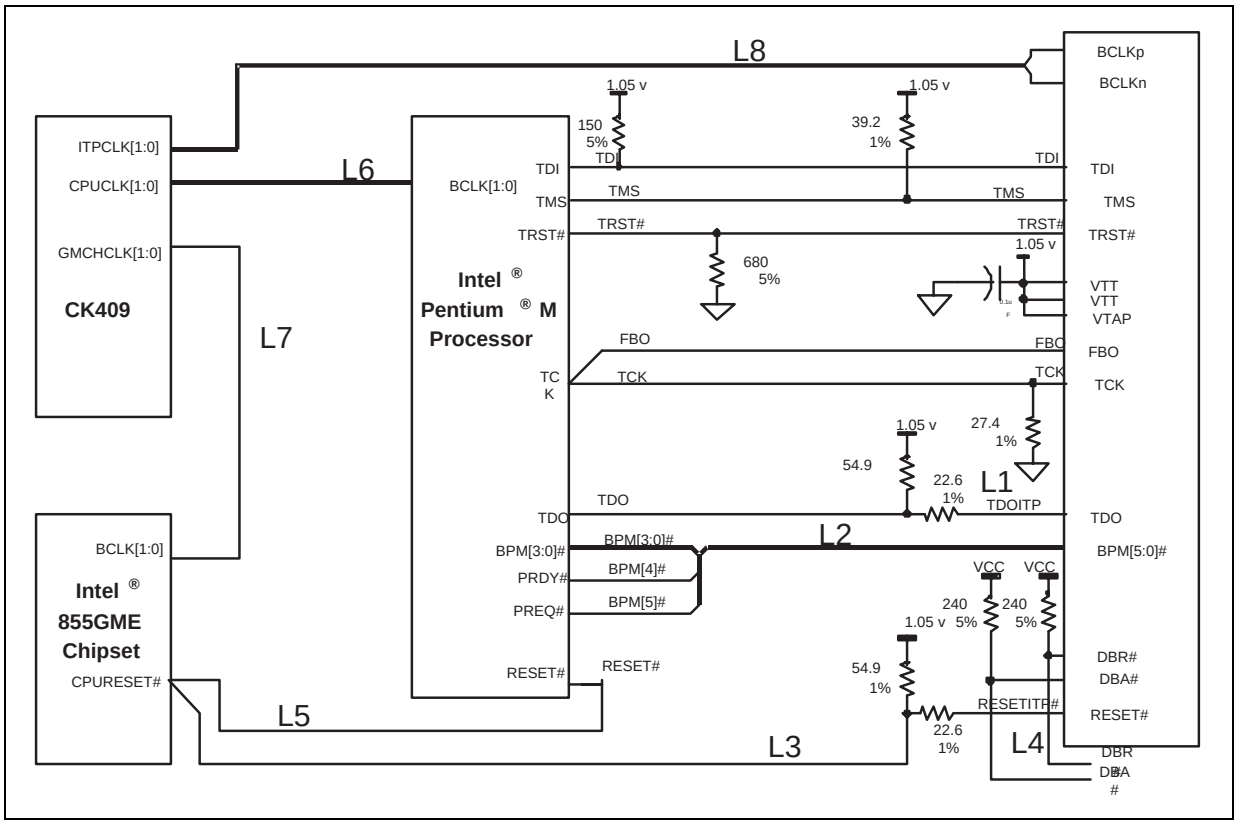
4.3.1 Recommended Onboard ITP700FLEX Implementation

4.3.1.1 ITP Signal Routing Guidelines

Figure 36 illustrates recommended connections between the onboard ITP700FLEX debug port, Intel Pentium M/Celeron M processor, 82855GME, and CK409 clock chip in the cases where the debug port is used.

For the purpose of this discussion on ITP700FLEX signal routing, refer to Section 4.1.1.4 for more details on the signal propagation time to distance relationships for the length matching requirements that are listed as periods of time below. It is understood that the time to distance relationships mentioned in Section 4.1.1.4 apply only to the specific assumptions made and it is the responsibility of the system designer to determine what is the appropriate length that correlates to the listed time periods as length matching requirements.

Figure 36. ITP700FLEX Debug Port Signals



1. Route the TDI signal between the ITP700FLEX connector and the Intel Pentium M/Celeron M processor. A 150-Ω ±5 percent pull-up to VCCP (1.05 V) should be placed within ± 300 ps of the TDI pin.
2. Route the TMS signal between ITP700FLEX connector and the Intel Pentium M/Celeron M processor. A 39.2-Ω ±1 percent pull-up to VCCP should be placed within ± 200 ps of the ITP700FLEX connector pin.
3. Route the TRST# signal between ITP700FLEX connector and the Intel Pentium M/Celeron M processor. A 510 Ω to 680 Ω ± 5 percent pull-down to ground should be placed on TRST#. Placement of the pull-down resistor is not critical. Avoid having any trace stub from the TRST# signal line to the termination resistor.
4. Route the TCK signal from the ITP700FLEX connector's TCK pin to the Intel Pentium M/Celeron M processor's TCK pin and then fork back from the Pentium M processor TCK pin and route back to ITP700FLEX connector's FBO pin. A 27.4 Ω ± 1 percent pull-down to ground should be placed within ± 200 ps of the ITP700FLEX connector pin.
5. Route the TDO signal from the Intel Pentium M/Celeron M processor to a 54.9 Ω ± 1 percent pull-up resistor to VCCP that should be placed close to ITP700FLEX connector's TDO pin. Then insert a 22.6 Ω ± 1 percent series resistor to connect the 54.9 Ω pull-up and 'TDOITP' net (see Figure 36). Limit the L1 segment length of the TDOITP net to less than 1.0 inch.

The Intel Pentium M/Celeron M processor drives the BPM[4:0]# signals to the ITP700FLEX at a 100 MHz clock rate. Route the BPM[4:0]# as a Zo=55 Ω point-to-point transmission line connection between the processor and the ITP700FLEX connector. Connect the ITP700FLEX

connector's BPM[3:0]# pins to Intel Pentium M/Celeron M processor's BPM[3:0]# pins. Connect the ITP700FLEX's BPM[4]# signal to the Intel Pentium M/Celeron M processor's PRDY# pin. The ITP700FLEX's integrated far-end terminations as well as the processor's AGTL+ integrated on-die termination ensure proper signal quality for the BPM[4:0]# signals. Due to the length of the ITP700FLEX cable, the length L2 of the BPM[4:0]# signals on the motherboard should be limited to shorter than 6.0 inches. The BPM[4:0]# signals' length L2 should be length matched to each other within ± 50 ps. The BPM[4:0]# signal trace lengths are matched inside the Intel Pentium M/Celeron M processor package, thus motherboard routing does **not** need to compensate for any processor package trace length mismatch. The BPM[4:0]# signal lengths also need to be matched within ± 50 ps to the L3+L4-L5 net lengths of the RESET# signal, i.e., L3 + L4 – L5 = L2 (within ± 50 ps).

Refer to Figure 36 for topology. See below for more details on routing guidelines for the RESET# signal.

Due to the Intel Pentium M/Celeron M processor's AGTL+ on-die termination for BPM[3:0]# and PRDY#, there is no issue or concern if the BPM[4:0]# pins of the ITP700FLEX connector are left floating when the ITP is not being used and the ITP700FLEX cable is unplugged.

Route the ITP700FLEX connector's BPM[5]# signal as a Zo = 55 Ω point-to-point connection to the Intel Pentium M/Celeron M processor's PREQ# pin. Integrated on the ITP700FLEX BPM[5]# driver signal is a resistive pull-up that ensures proper signal quality at the processor's PREQ# input pin. The Intel Pentium M/Celeron M processor has an integrated, weak, on-die pull-up to VCCP for the PREQ# signal to ensure a proper logic level when the ITP700FLEX port connector is not plugged in. There is no need for any external termination on the motherboard for the BPM[5]# = PREQ# signal. The maximum length of BPM[5]#/PREQ# should not exceed 6.0 inches.

As explained in Section 4.1.6, the RESET# signal forks (see Figure 14) out from the 82855GME's CPURESET# pin and is routed to the Intel Pentium M/Celeron M processor and ITP700FLEX debug port. One branch from the fork connects to the Intel Pentium M/Celeron M processor's RESET# pin and the second branch connects to a 220 Ω ± 5 percent termination pull-up resistor to VCCP placed close to the ITP700FLEX debug port. A series 22.6 Ω ± 1 percent resistor is used to continue the path to the ITP700FLEX RESET# pin with the RESETITP# net in Figure 36. The length of the RESETITP# net (labeled as net L4) should be limited to less than 0.5 inches. To ensure correct operational timings, the length of the RESET# nets L3, L4, and L5 with respect to the BPM[4:0]# net length L2 should adhere to the following length matching requirement within ± 50 ps., i.e., L3 + L4 – L5 = L2 (within ± 50 ps).

There is no need for pull-up termination on the Intel Pentium M/Celeron M processor side of the RESET# net due to presence of AGTL+ on-die termination on the processor and the 82855GME.

The ITP700FLEX debug port's BCLKp/BCLKn inputs are driven with a 100 MHz differential clock from the CK409 clock chip. The CK409 also feeds two other pairs of 100-MHz differential clocks to the Intel Pentium M/Celeron M processor BCLK[1:0] and Intel 855GME chipset BCLK[1:0] input pins. Common clock signal timing requirements of the 82855GME and the Intel Pentium M/Celeron M processor requires matching of processor and GMCH BCLK[1:0] nets L6 and L7, respectively. To ensure correct operation of ITP700FLEX, the BCLKp/BCLKn net L8 should be tuned to within ± 50 ps to the sum of length L6 of the BCLK[1:0] lines and the additional length L2 of the BPM#[4:0] signals, i.e., L6 + L2 = L8 (within ± 50 ps).

The timing requirements for the BPM[5:0]#, RESET#, and BCLKp/BCLKn signals of the ITP700FLEX debug port require careful attention to their routing. Standard high-frequency bus routing practices should be observed.

1. Keep a minimum of 2:1 spacing in between these signals and to other signals.

2. Reference these signals to ground planes and avoid routing across power plane splits.
3. The number of routing layer transitions should be minimized. When layout constraints require a routing layer transition, any such transition shall be accompanied with ground stitching vias placed within 100 mils of the signal via with at least one ground via for every two signals making a layer transition.

DBR# should be routed to the system reset logic (e.g., the SYSRST# signal of the 6300ESB) and initiate the equivalent of a front panel reset commonly found in desktop systems. The 150 Ω to 240 Ω pull-up resistor should be placed within 1 ns of the ITP700FLEX connector.

Note: The CPU should **not** be power cycled when DBR# is asserted.

DBA# is an optional system signal that may be used to indicate to the system that the ITP/TAP port is being used. When not implemented, this signal may be left as no connect. When implemented, it shall be routed with a 150 Ω to 240 Ω pull-up resistor placed within 1 ns of the ITP700FLEX connector. Refer to the *ITP700 Debug Port Design Guide* for more details on DBA# usage.

The ITP700FLEX VTT and VTAP pins should be shorted together and connected to the VCCP (1.05 V) plane with a 0.1 µF decoupling capacitor placed within 0.1 inch of the VTT pins. Table 19 summarizes termination resistors values, placement, and voltages the ITP signals need to connect to for proper operation for onboard ITP700FLEX debug port.

Table 19. Recommended ITP700FLEX Signal Terminations (Sheet 1 of 2)

Signal	Termination Value	Termination Voltage	Termination/Decap Location	Notes
TDI	150 Ω ± 5%	VCCP (1.05 V)	Within ± 300 ps of the Intel Pentium M/Celeron M processor CPU TDI pin	5
TMS	39.2 Ω ± 1%	VCCP (1.05 V)	Within ± 200 ps of the ITP700FLEX connector TMS pin	5
TRST#	510-680 Ω ± 5%	GND	Anywhere between Intel Pentium M/Celeron M processor CPU and ITP700FLEX connector	5
TCK	27.4 Ω ± 1%	GND	Within ± 200 ps of the ITP700 FLEX connector TCK pin	5
TDO	54.9 Ω ± 1% pull-up and 22.6 Ω ± 1% series resistor	VCCP (1.05 V)	Within 1” of the ITP700FLEX connector TDO pin	1, 5
BCLK(p/n)				2
FBO	Connect to TCK pin of Intel Pentium M/Celeron M processor CPU	N/A	N/A	1
RESET#	220 Ω ± 5% pull-up and 22.6 Ω ± 1% series resistor	VCCP (1.05 V)	Within 0.5” of the ITP700FLEX connector RESET# pin	1
BPM[5:0]#	Not Required			3
DBA#	150-240 Ω ± 5%	VCC of target system recovery circuit	Within 1 ns of the ITP700FLEX connector DBA# pin	4
DBR#	150-240 Ω ± 5%	VCC of target system recovery circuit	Within 1 ns of the ITP700FLEX connector DBR# pin	

Table 19. Recommended ITP700FLEX Signal Terminations (Sheet 2 of 2)

Signal	Termination Value	Termination Voltage	Termination/Decap Location	Notes
VTAP	Short to VCCP plane	VCCP (1.05 V)		
VTT	Short to VCCP plane	VCCP (1.05 V)	Add 0.1 µF decap within 0.1 inch of VTT pins of ITP700FLEX connector	

NOTES:
1. Refer to Figure 36.
2. Refer to Section 4.3.1.1 for more information.
3. All the needed terminations to ensure proper signal quality are integrated inside the Intel Pentium M/Celeron M processor AGTL+ buffers or inside the ITP700FLEX debug port. No need for any external components for the BPM[5:0]# signals.
4. Only required if DBA# is used with any target system circuitry. This signal may be left unconnected if unused.
5. In cases where a system is designed to use the ITP700FLEX debug port for debug purposes but the ITP700FLEX connector may or may not be populated at all times although the signal routing and termination or decoupling components are implemented, the component placement guidelines should adhere to the ones listed. However, for signals where the termination component placement guidelines for non-ITP700FLEX supported systems (see Table 7) are more restrictive or conservative than the component placement guidelines for the ITP700FLEX supported case, then the more conservative/restrictive guidelines should be followed.

4.3.1.2 ITP Signal Routing Example

Figure 38 illustrates a recommended layout example for the ITP700FLEX signals. The ITP700FLEX connector is placed on the primary side of the motherboard and results in a smooth, straight-forward routing solution.

Note: The V_{CCP} (1.05 V) power delivery continues from the Intel Pentium M/Celeron M processor socket cavity on the secondary side of the motherboard through the pin field as shown on the right side of Figure 38. Three V_{CCP} vias in conjunction with three ground stitching vias allow a transition to the primary side to connect to the VTT and VTAP pins of the ITP700FLEX connector and a transition back to the secondary side of the motherboard. A small V_{CCP} flood is created on the secondary side under the body of the ITP700FLEX connector with a 0.1 µF decoupling capacitor. This provides a convenient connection for the 220 Ω and 54.9 Ω pull-ups for RESET# and TDO signals as well as the 39.2 Ω pull-up for the TMS signal.

Notice the very short trace from the 22.6 Ω series resistors for the RESET# and TDO signals to the ITP700FLEX pins. Refer to Section 4.1.6 for more details on RESET# signal routing.

The 150 Ω TDI pull-up is connected to the V_{CCP} (1.05 V) flood on the secondary side close to Intel Pentium M/Celeron M processor pin.

The ITP700FLEX TCK pin has a 27.4 Ω pull-down to ground very close to the ITP700FLEX connector and routes to the Intel Pentium M/Celeron M processor's TCK pin and loops back with no stub to the FBO pin of the ITP700FLEX connector.

BCLKp/BCLKn are routed in this example on Layer 3. For more BCLKp/BCLKn routing details, refer to Figure 4.1.6 in Section 4.1.7.

All other signals incorporate a straight forward routing methodology between the ITP700FLEX and Intel Pentium M/Celeron M processor pins.

4.3.1.3 ITP_CLK Routing to ITP700FLEX Connector

A layout example for ITP_CLK/ITP_CLK# routing to an ITP700FLEX connector is shown in Figure 37. The CK409 clock chip is mounted on the primary side of the motherboard and the differential clock pair breaks out on the same side. The differential ITP clock pair routing requires the use of a pair of 33 Ω ± 5 percent series resistors placed within 0.5 inches of the clock chip output pins followed by a pair of 49.9 Ω ± 1 percent termination resistors to ground. Serpentining of the ITP_CLK traces is performed to meet the ± 50 ps length matching requirement between ITP_CLK and the sum of length L6 of the BCLK[1:0] lines and the additional length L2 of the BPM#[5:0] signals in Figure 36. The ITP_CLK pair routing then switches back to the primary side layer through a via near the ITP700FLEX connector. Figure 38 depicts the ITP700FLEX signals layout example.

Figure 37. ITP_CLK to ITP700FLEX Connector Layout Example

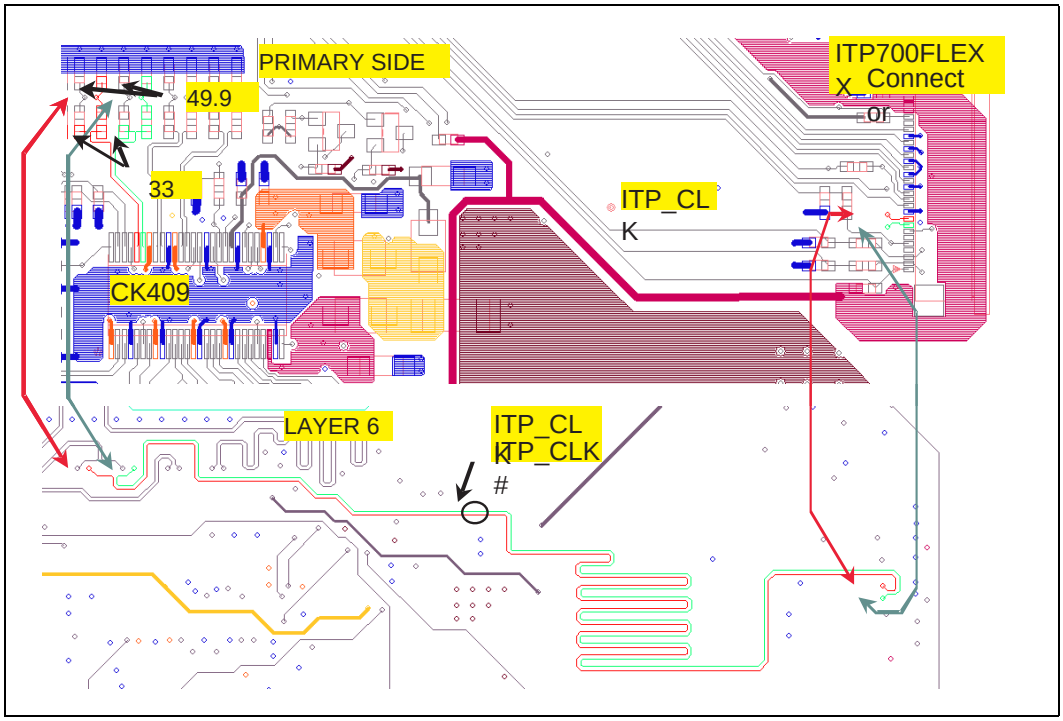
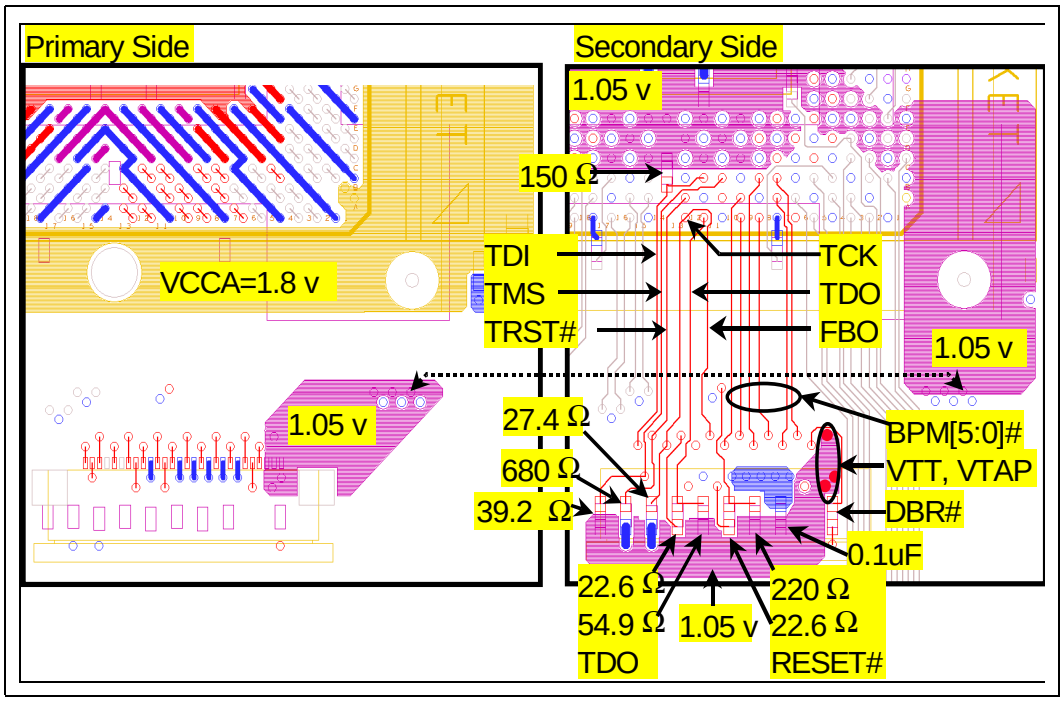


Figure 38. ITP700FLEX Signals Layout Example



4.3.1.4 ITP700FLEX Design Guidelines for Production Systems

For production systems that do not populate the onboard ITP700FLEX debug port connector, the following guidelines should be followed to ensure that all necessary signals are terminated properly.

Table 7 summarizes all the signals that require termination when a system does not populate the ITP700FLEX connector but still implements the routing for all the signals. This includes TDI, TMS, TRST#, and TCK. Based on the recommended values in this table, the resistor tolerances for TMS and TCK may be relaxed from ± 1 percent to ± 5 percent to reduce cost. Also, TDO may be left as a no-connect, thus the 54.9 Ω ± 1 percent pull-up and 22.6 Ω ± 1 percent series resistors may be removed.

For the ITP700FLEX connector's RESET# input signal, the 220 Ω ± 5 percent resistor should be removed as well as the 22.6 Ω ± 1 percent series resistor.

The series 33 Ω and 49.9 Ω ± 1 percent parallel termination resistors on the ITP_CLK/ITP_CLK# differential host clock inputs to the ITP700FLEX connector may also be depopulated for production systems. The only requirement is that the BIOS should disable the third differential host clock pair routed from the CK409 clock chip to the ITP700FLEX connector.

Finally, the 150 Ω to 240 Ω pull-up resistor for the DBR# output signal from the ITP700FLEX connector may or may not be depopulated depending on how it affects the system reset logic to which it is connected. Thus, it is the responsibility of the system designer to determine whether termination for DBR# is required or not for a given system implementation. The same is also true for DBA#, if implemented. This signal is not required and may be left as no connect. However, it is the responsibility of the system designer to determine whether termination for DBA# is required

4.3.2 Recommended ITP Interposer Debug Port Implementation

Intel is working with American Arium* to provide ITP interposer cards for use in debugging Intel Pentium M/Celeron M processor-based systems as an alternative to the onboard ITP700FLEX in cases where the onboard connector cannot be supported. The ITP interposer card is an additional component that integrates a Intel Pentium M/Celeron M processor socket along with ITP700 connector on a single interposer card that is compatible with the 478-pin Intel Pentium M/Celeron M processor socket.

Table 7 summarizes all the signals that require termination for a system designed for use with the ITP interposer. This includes TDI, TMS, TRST#, and TCK. TDO may be left as a no connect.

DBR# should be routed to the system reset logic (e.g., the SYSRST# signal of the 6300ESB) and initiate the equivalent of a front panel reset commonly found in desktop systems. The 150 Ω to 240 Ω pull-up resistor should be placed within 1 ns of the ITP connector.

Note: The processor should **not** be power cycled when DBR# is asserted.

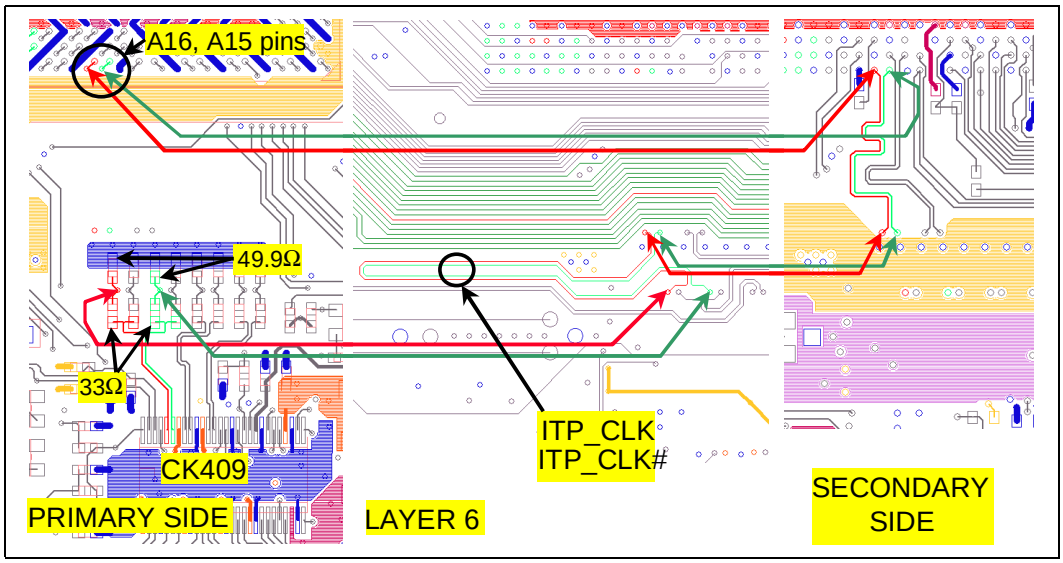
DBA# is an optional system signal that may be used to indicate to the system that the ITP/TAP port is being used. When not implemented, this signal may be left as no connect. When implemented, it shall be routed with a 150 Ω to 240 Ω pull-up resistor placed within 1 ns of the ITP connector.

4.3.2.1 ITP_CLK Routing to ITP Interposer

A layout example for ITP_CLK/ITP_CLK# routing to the CPU socket for supporting an ITP interposer is shown in Figure 39. The CK409 clock chip is mounted on the primary side layer of the motherboard and the differential clock pair also breaks out on the same side. The differential ITP clock pair routing also requires a pair of 33 Ω ± 5 percent series resistors placed within 0.5 inches of the clock chip output pins and followed by a pair of 49.9 Ω ± 1 percent termination resistors to ground. The majority of the ITP_CLK differential serpentine routing takes place on internal Layer 6 below the Intel Pentium M/Celeron M processor FSB address signal routing.

Completion of ITP+CLK routing on Layer 6 is not possible due to Intel Pentium M/Celeron M processor FSB routing on Layer 6. Therefore the ITP_CLK differential pair then is routed to the secondary side layer to complete routing to the ITP_CLK (pin A16) and ITP_CLK# (pin A15) pins of the Intel Pentium M/Celeron M processor while matching the BCLK[1:0] routing on the secondary side for a 507 mil length (see Figure 16 and description in Section 4.1.7). Routing to the CPU socket on the primary side layer is not possible because of the presence of the VCCA 1.8 V or 1.5 V plane flood along the A-signal side row of the pin-map. ITP_CLK routing to the ITP interposer should achieve the ± 50 ps length matching requirement of the BCLK[1:0] lines.

Figure 39. ITP_CLK to CPU ITP Interposer Layout Example



4.3.2.2 ITP Interposer Design Guidelines for Production Systems

For production systems that do not use the ITP interposer, observe the following guidelines to ensure that all necessary signals are terminated properly.

Table 7 summarizes all the signals that require termination when a system does not use the ITP interposer. This includes TDI, TMS, TRST#, and TCK. TDO may be left as a no connect.

The series 33 Ω and 49.9 Ω ± 1 percent parallel termination resistors on the ITP_CLK/ITP_CLK# differential host clock inputs to the processor socket may also be depopulated for production systems. The only requirement is that the BIOS should disable the third differential host clock pair routed from the CK409 clock chip to the Intel Pentium M/Celeron M processor socket.

Finally, the 150 Ω to 240 Ω pull-up resistor for the DBR# output signal from processor socket may or may not be depopulated depending on how it affects the system reset logic that it is connected to. Thus, it is the responsibility of the system designer to determine whether termination for DBR# is required or not for a given system implementation. The same is also true for DBA# if implemented. This signal is not required and may be left as no connect. However, it is the responsibility of the system designer to determine whether termination for DBA# is required.

4.3.3 Logic Analyzer Interface (LAI)

Intel is working with Agilent Corporation to provide logic analyzer interfaces (LAIs) for use in debugging Intel Pentium M/Celeron M processor-based systems. LAI vendors should be contacted to get specific information about their logic analyzer interfaces. The following information is general; specific information must be obtained from the logic analyzer vendor.

Due to the complexity of a Intel Pentium M/Celeron M processor-based system, the LAI is critical in providing the ability to probe and capture Intel Pentium M/Celeron M processor system bus signals. There are two sets of considerations to keep in mind when designing a Intel Pentium M/Celeron M processor-based system that may make use of a LAI: mechanical and electrical.

4.3.3.1 Mechanical Considerations

The LAI is installed between the processor socket and the Intel Pentium M/Celeron M processor. The LAI pins plug into the socket, while the Intel Pentium M/Celeron M processor in the 478-pin package plugs into a socket on the LAI. Cabling this part of the LAI egresses the system to allow an electrical connection between the Intel Pentium M/Celeron M processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system.

Note: It is possible that the keepout volume reserved for the LAI may include space normally occupied by the Intel Pentium M/Celeron M processor heat sink. When this is the case, the logic analyzer vendor shall provide a cooling solution as part of the LAI.

4.3.3.2 Electrical Considerations

The LAI also affects the electrical performance of the Intel Pentium M/Celeron M processor system bus. Therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool works in the system. Contact the logic analyzer vendor for electrical specifications as load models for the LAI solution they provide.

4.3.4 Processor Phase Lock Loop (PLL) Design Guidelines

4.3.4.1 Processor PLL Power Delivery

V_{CCA}[3:0] is a power source required by the PLL clock generators on the processor silicon. Because these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system because it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). Traditionally this supply is low-pass filtered to prevent any performance degradation. The Intel Pentium M/Celeron M processor has an internal PLL super filter for the 1.8 V supply to the VCCA [3:0] pins that dispenses with the need for any external low-pass filtering. However, one 0603 form factor 10 nF and one 1206 form factor 10 µF decoupling capacitor should be placed as close as possible to each of the four VCCA pins (i.e., a pair of capacitors consisting of one 10 nF and one 10 µF should be used for each VCCA pin). VCCA power delivery should meet the 1.8 V ± 5 percent tolerance at the VCCA pins. As a result, to meet the current demand of the Intel Pentium M/Celeron M processor and the future Intel Pentium M/Celeron M processor family, it is strongly recommended that the VCCA feed resistance from the 1.8 V power supply up to the VCCA shorting scheme described below be less than 0.1 Ω. It is recommended that the main VCCA feed be connected to the Intel Pentium M/Celeron M processor VCCA1 pin. Refer to Section 4.3.4.3 for Intel Pentium M/Celeron M processor PLL decoupling requirements.

Figure 40 illustrates the recommended layout example of the VCCA[3:0] pins feed and decoupling. The 1.8 V flood on Layer 3 from the Intel 855GME chipset is a via routed up to the primary side layer with a cluster of five 1.8 V vias and two GND stitching vias as shown on the left and middle side of Figure 40. On the primary layer side, a wide flood in a U-shape shorts the four VCCA[3:0] pins of the processor. To minimize resistance and inductance of the U-shaped VCCA flood shorting the VCCA[3:0] pins, the flood should be at least 100 mils wide and be spaced at least 25 mils from any switching signals. When possible, a flood wider than the 100 mil minimum shall be implemented and shall reference a ground plane only. Do not reference any switching signals or split planes. The recommended wide flood on the primary side benefits from low

inductance connections to the VCCA[3:0] pins due to the close proximity of the Layer 2 solid ground plane 4 mils below the primary side 1.8 V flood. (Refer to the stack-up description in Figure 140.)

VCCA0 capacitors are also placed on the primary side. No via is needed on the VCCA0 side of the capacitors that connect to the VCCA0 pin. A small ground flood on the primary side shorts the ground side of the 1206 form factor 10 µF VCCA0 decoupling capacitors via two ground stitching vias to minimize interaction with Intel Pentium M/Celeron M processor FSB routing. The 0603 form factor 10 nF VCCA0 decoupling capacitor connects to internal ground planes through a single ground stitching via.

VCCA1 decoupling capacitors are placed on the primary side on the bottom right corner of the Intel Pentium M/Celeron M processor socket. No via is required to connect the VCCA1 side of the decoupling capacitors to the VCCA1 pin. A small ground plane connects the groundside of the 1206 form factor 10 µF VCCA1 capacitors with a pair of vias to an internal ground plane. The 10 µF decoupling capacitor connects to internal ground planes through a single ground stitching via.

The decoupling capacitors for VCCA2 are placed on the primary side on the right of the Intel Pentium M/Celeron M processor socket. A small ground flood on the primary side is shared by the GND-side of the two required decoupling capacitors for VCCA2. Both the 10 nF and the 10 µF capacitor are placed in a vertical orientation on the primary side to avoid interaction with Intel Pentium M/Celeron M processor FSB routing and do not require vias on the VCCA2 side to connect to the VCCA2 pin.

Figure 41 depicts the Intel Pentium M/Celeron M processor 1.8 V Intel customer reference board routing example.

Figure 40. Intel® Pentium® M/Celeron® M Processor 1.8-V VCCA[3:0] Recommended Power Delivery and Decoupling

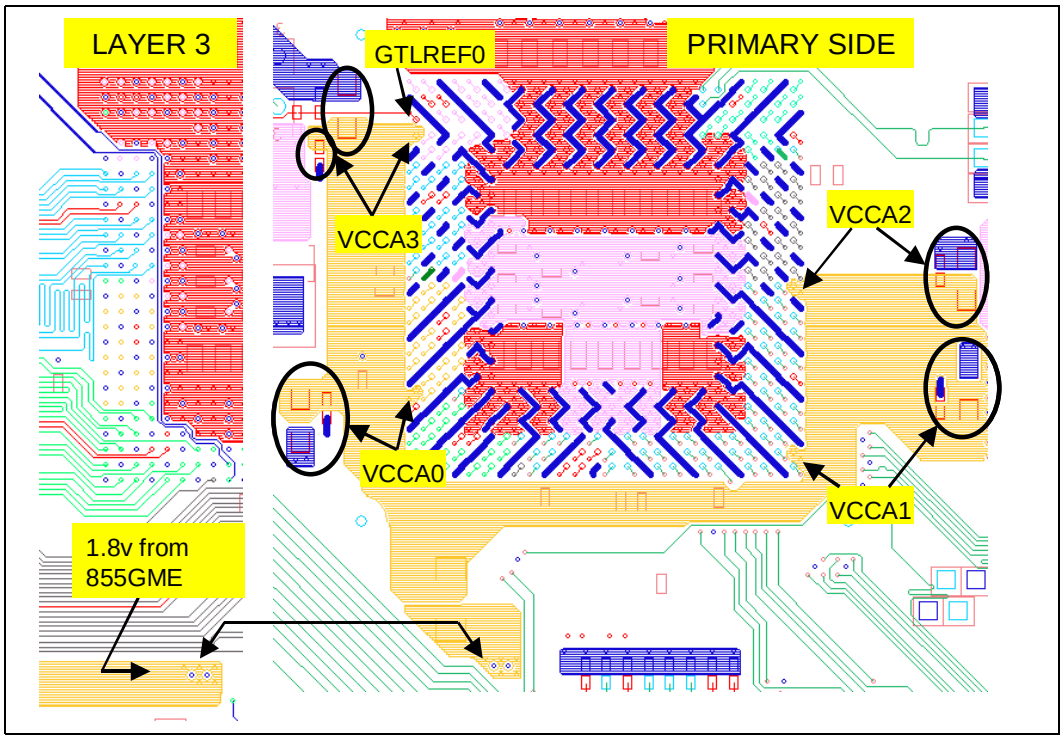
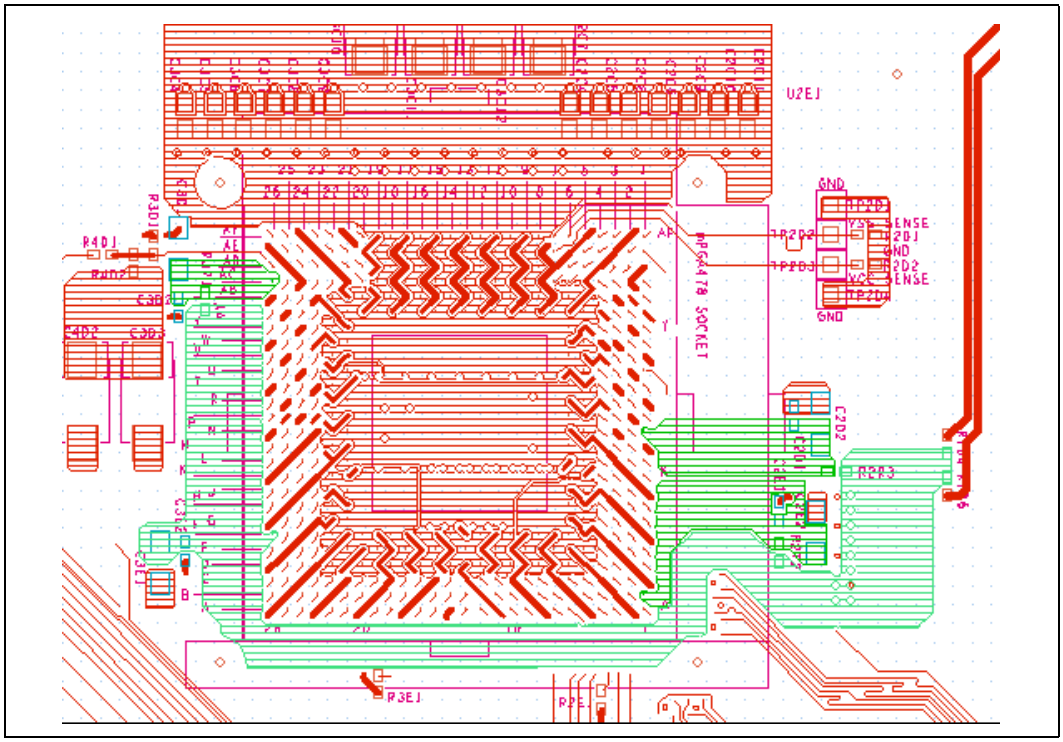


Figure 41. Intel® Pentium® M/Celeron® M Processor 1.8 V Intel® Customer Reference Board Routing Example



4.3.4.2 Processor PLL Voltage Supply Power Sequencing

Refer to Section 4.8 for more details on platform power sequencing requirements for the 1.8 V supply to the Intel Pentium M/Celeron M processor PLLs.

4.3.4.3 Processor PLL Decoupling Requirements

Table 20 presents the $V_{CCA[3:0]}$ decoupling guidelines.

Table 20. $V_{CCA[3:0]}$ Decoupling Guidelines

Description	Cap (µF)	Notes
Mid-Frequency Decoupling	4 x 10 µF	(Polymer Covered Tantalum – POSCAP, Neocap, KO Cap)
High-Frequency Decoupling	4 x 10 nF	(0603 MLCC, >= X7R) Place next to the Intel Pentium M/Celeron M processor CPU.

NOTES:
1. VCCA[3:0] should be tied to Vcc1_8S.
2. One 10 µF and one 10 nF capacitor pair should be used for each VCCA pin.

4.3.5 Intel® Pentium® M/Celeron® M Processor Power Status Indicator (PSI#) Signal

PSI# is located at pin E1 of the Intel Pentium M/Celeron M processor pin-map and may be used to:

- Improve the light load efficiency of the voltage regulator, resulting in platform power savings
- Simplify voltage regulator designs because it removes the need for integrated 100 µs timers that are required to mask the PWRGOOD signal during Intel SpeedStep® Technology transitions

4.3.6 Thermal Power Dissipation

The amount of current required from the processor power delivery circuit and the heat generated by processors has increased as processor frequencies go up and the silicon process geometry shrinks. The package of any integrated device may only dissipate so much heat into the surrounding environment. The temperature of a device, such as a processor power delivery circuit-switching transistor, is a balance of heat being generated by the device and its ability to shed heat either through radiation into the surrounding air or by conduction into the circuit board. Increased power effectively raises the temperature of the processor power delivery circuits. Switching transistor die temperatures may exceed the recommended operating value if the heat cannot be removed from the package effectively.

As the demands for higher frequency and performance processors increase, the amount of power dissipated, i.e., heat generated, in the processor power delivery circuit is a concern for system, thermal and electrical design engineers. The high input voltage, low duty factor inherent in power supply designs leads to increasing power dissipation losses in the output stage of the traditional buck regulator topology used in the industry today.

These power dissipation losses may be attributed to the following three main areas of the processor power delivery circuit:

- During switching of the top control MOSFET
- Resulting from drain to source resistance ($R_{DS\_(ON)}$) DC losses across the bottom synchronous MOSFET
- Generated through the magnetic core and windings of the main power inductor

There has been significant improvement in the switching MOSFET technology to lower gate charge of the control MOSFET allowing them to switch faster, thus reducing switching losses. For example, improvements in lowering the $R_{DS(ON)}$ parametric of the synchronous MOSFET have resulted in reduced DC losses and the Direct Current Resistance (DCR) of the power inductor has been reduced to lower the amount of power dissipation in the circuit's magnetic.

However, these technology improvements by themselves are not sufficient to effectively remove the heat generated during the high current demand and tighter voltage regulation required by today's mobile processors. There are several mechanisms for effectively removing heat from the package of these integrated devices. Some of the most common methods are listed below.

- Attaching a heat spreader or heat pipe to the package with a low thermal coefficient bonding material.
- Adding and/or increasing the copper fill area attached to high current carrying leads.
- Adding or redirecting air flow to stream across the device.

- Using multiple devices in parallel, as allowed, to reduce package power dissipation.
- Using newer/enhanced technology and devices to lower heat generation but with equal or better performance.

For the designer, these options are not always available or economically feasible. The most effective method of thermal spreading and heat removal from these devices is to generate airflow across the package and add copper fill area to the current carrying leads of the package.

The processor power delivery topology also may be modified to improve the thermal spreading characteristic of the circuit and dramatically reduce the power dissipation requirements of the switching MOSFET and inductor. This multi-phase topology provides an output stage of the processor regulator, which consists of several smaller buck inductor phases that are summed together at the processor. Each phase may be designed to handle and source a much smaller current, which may reduce the size, quantity, and rating of the design components and may decrease the cost and PCB area needed for the total solution. The implementation options for this topology are discussed in the next section.

4.4 Intel® Pentium® M/Celeron® M Processor Decoupling Recommendations

Intel recommends proper design and layout of the system board bulk and high-frequency decoupling capacitor solution to meet the transient tolerance at the processor package balls. To meet the transient response of the processor, it is necessary to properly place bulk and high-frequency capacitors close to the processor power and ground pins.

4.4.1 Transient Response

The inductance of the motherboard power planes slows the voltage regulator's ability to respond quickly to a current transient. Decoupling a power plane may be partitioned into several independent parts. The closer the capacitor is placed to the load, the more stray inductance is bypassed. Less capacitance is required when bypassing the inductance of leads, power planes, etc. However, areas closer to the load have less room for capacitor placement, and trade-offs must be made.

The processor causes very large switching transients. These sharp surges of current occur at the transition between low power states and the normal operating states. The system designer must provide adequate high-frequency decoupling to manage the highest frequency components of the current transients. Larger bulk storage capacitors supply current during longer-lasting changes in current demand.

All of this power bypassing is required because the DC-to-DC converter is relatively slow to respond. A typical voltage converter has a reaction time on the order of 1 to 100 µs while the processor's current steps may be shorter than 1 ns. High-frequency decoupling is typically done with ceramic capacitors with a very low ESR. Because of their low ESR, these capacitors may act very quickly to supply current at the beginning of a transient event. However, because the ceramic capacitors are small and may only store a small amount of charge, bulk capacitors are needed too. Bulk capacitors are typically polarized with high capacitance values and unfortunately higher ESLs and ESRs. The higher ESL and ESR of the bulk capacitor limit how quickly it may respond to a transient event. The bulk and high-frequency capacitors working together may supply the charge needed to stay in regulator before the regulator may react during a transient.

4.4.2 High-Frequency/Mid-Frequency and Bulk Decoupling Capacitors

System motherboards shall include high and mid-frequency and bulk decoupling capacitors as close to the socket power and ground pins as possible. Decoupling shall be arranged such that the lowest ESL devices (0612 reverse geometry type, if used for some of the recommended options below) are closest to the processor power pins followed by the 1206 devices (if used), and finally bulk electrolytics (organic covered tantalum or aluminum covered capacitors). System motherboards shall include bulk-decoupling capacitors as close to the processor socket power and ground pins as possible. The layout example shown in Section 4.4.3 shall be followed closely. Table 21 lists four recommended decoupling solutions for $V_{CC-CORE}$, while Table 22 lists the Intel Pentium M/Celeron M processor Vccp decoupling recommendations. Table 24 lists the recommended GMCH decoupling solutions for the V_{CCP} and V_{CCGMCH} supply rails, respectively.

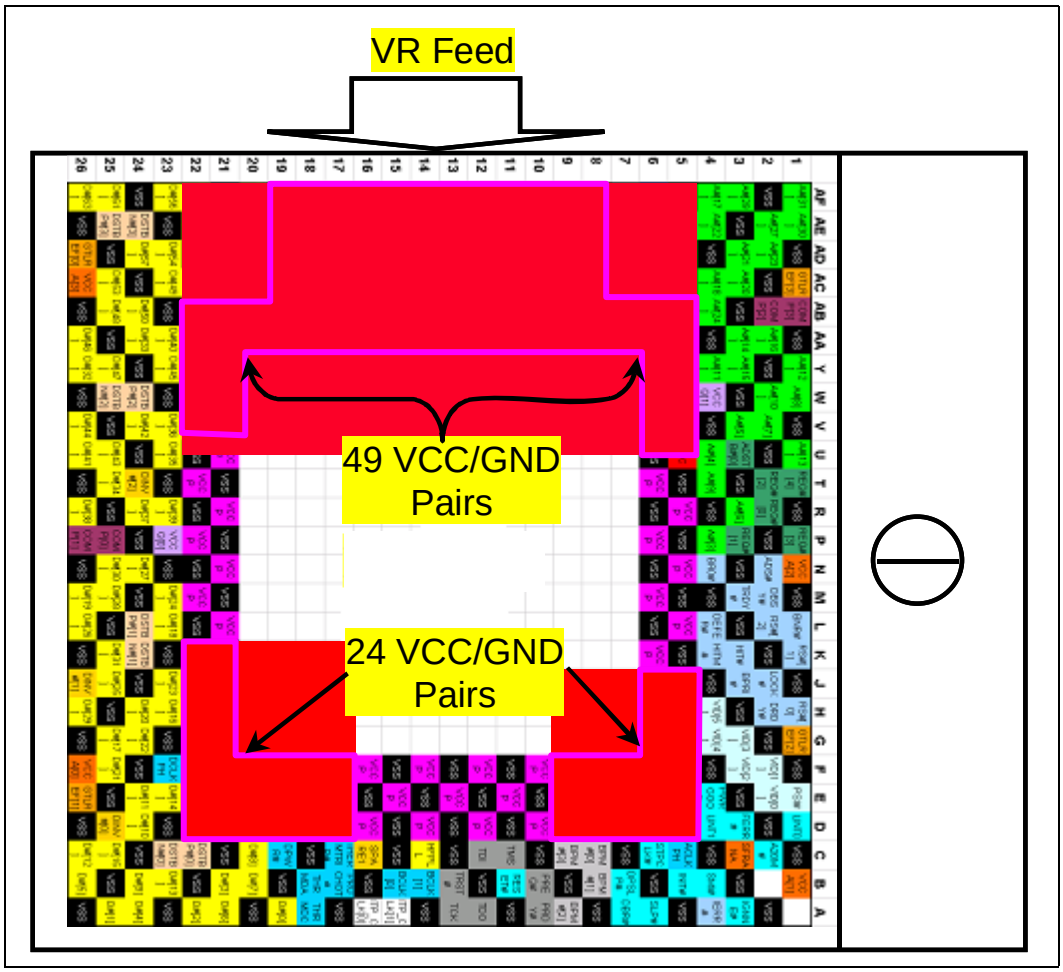
4.4.3 Processor Core Voltage Plane and Decoupling

Due to the high current requirements of the processor core voltage, the $V_{CC-CORE}$ is fed from the VRM by multiple power planes that provide both low resistance and low inductance paths between the voltage regulator, decoupling capacitors, and processor $V_{CC-CORE}$ pins. To meet the $V_{CC-CORE}$ transient tolerance specifications for the worst-case stimulus, the maximum Equivalent Series Resistance (ESR) of the decoupling solution shall be equal to or less than 3 mΩ.

Figure 2 (in Section 3.1) depicts an example of a motherboard power plane stack-up that allows for both robust, high-frequency signal routing and robust $V_{CC-CORE}$ power delivery.

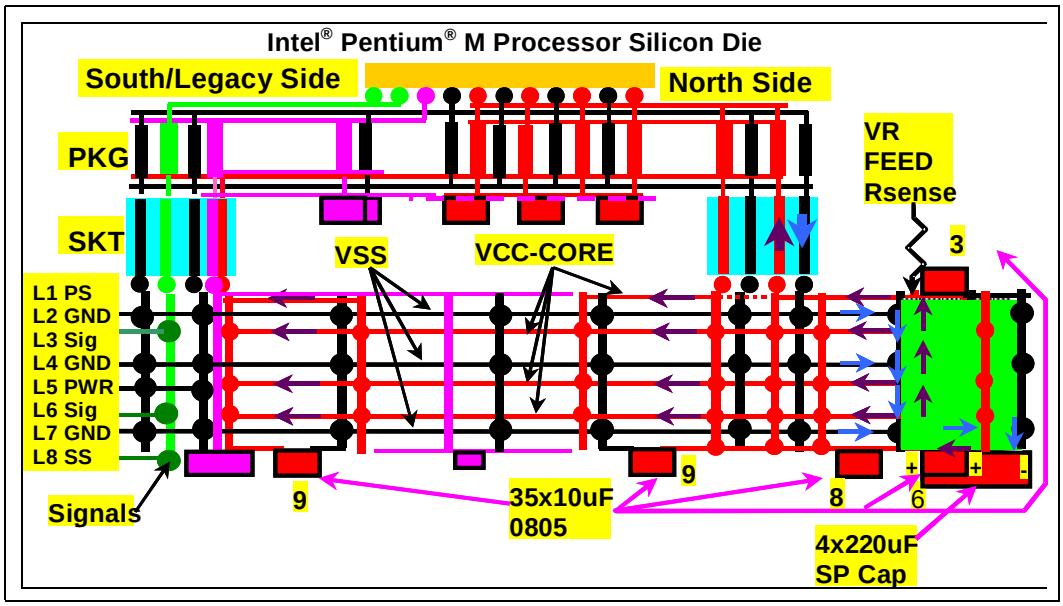
The Intel Pentium M/Celeron M processor pin-map is shown in Figure 42 for reference. Note the highlighted $V_{CC-CORE}$ power delivery corridor pins concentrated on the north side of the pin-map that contains 49 $V_{CC-CORE}$/GND pin pairs while the south side of the socket contains only 24 $V_{CC-CORE}$/GND pin pairs. Because access to the 24 south side pin pairs is blocked by the legacy signals, the only option available for providing robust core power delivery to the Intel Pentium M/Celeron M processor is by placing the VRM and most of the decoupling capacitors to the north of the core power delivery corridor (found on the north side of the 49 $V_{CC-CORE}$/GND pin pairs). It is not advised to feed the VR from any other side other than this $V_{CC-CORE}$ corridor on the north side of the Intel Pentium M/Celeron M processor socket. Due to the high current demand, all the $V_{CC-CORE}$ and ground vias of the Intel Pentium M/Celeron M processor pin-map shall have vias that are connected to both internal and external power planes. Sharing of vias between several $V_{CC-CORE}$ pins or ground pins is not allowed.

Figure 42. Intel® Pentium® M/Celeron® M Processor Socket Core Power Delivery Corridor



A conceptual diagram of this $V_{CC-CORE}$ power delivery scheme is shown in Figure 43.

Figure 43. Intel® Pentium® M/Celeron® M Processor Core Power Delivery and Decoupling Concept Example (Option #4)



In this example, (option 4) bulk-decoupling 220 µF SP capacitors from $V_{CC-CORE}$ decoupling option 4 are placed on the north side of the secondary side layer in the Intel Pentium M/Celeron M processor $V_{CC-CORE}$ power delivery corridor. Notice the VRM feed point (sense resistor connection) is on the positive terminal side of the 220 µF SP capacitors. Both $V_{CC-CORE}$ and ground vias are used on both sides of the SP capacitors' positive terminal side to reduce the inductance of the capacitor connection as illustrated by the current flow loop area in Figure 43. When the VR feed is on the negative side of the SP capacitors, both $V_{CC-CORE}$ and GND stitching vias are needed on both the positive and negative terminals of the capacitor to reduce the effective inductance of the capacitor.

Layers 1 (primary side layer), 3, 5, 6, and (secondary side layer) 8 are used for $V_{CC-CORE}$ current feeding while referencing Layers 2, 4, and 7 (ground planes) with a small dielectric separation (see Figure 2). These layers are solid ground planes in the areas under the Intel Pentium M/Celeron M processor package outline and where the decoupling capacitors are placed. This results in a reduction in effective loop inductance. For the recommended layout examples shown in Table 21 and Figure 44, a low inductance value of ~41 pH is achieved.

Bulk decoupling capacitors respond too slowly to handle the fast current transients of the processor. For this reason, 0805 mid-frequency decoupling capacitors are added on the primary and secondary side. Some are placed under the package outline of the processor while the rest are placed in the periphery of the processor along the AF signal row of the pin-map where a majority of the $V_{CC-CORE}$ power pins are found. Four-mil power plane separation between the secondary side power plane flood and Layer 7 ground while using the 0805 capacitors significantly reduces the inductance of these capacitors. Results from a 3D field solver simulation suggest that an ESL of 600 pH per capacitor may be used to help achieve the specific layout style described in previous sections. The ESL of the 0805 capacitors is a very critical parameter; the layout style shown in the recommendation in a latter section shall be closely followed. To stress the importance of 0805 capacitors that result in an ESL of 600 pH, it may be compared to ~1.2 nH ESL for 1206 form factor capacitors.

Note: The 0805 capacitors have $V_{CC-CORE}$ and ground vias on both negative and positive terminals similar to the 220 µF SP capacitors to achieve a low inductance connection.

The motivation for concentrating the majority of the 0805 mid/high-frequency decoupling capacitors and all of the SP-type bulk decoupling capacitors on the secondary side layer is to take advantage of the $V_{CC-CORE}$ corridor that establishes a robust connection from the VRM feed to the decoupling capacitors. On the primary side, the dog bone via connections for the $V_{CC-CORE}$ pins and ground pins effectively separate the $V_{CC-CORE}$ plane flood into multiple relatively narrow strips separated by alternating Vss dog bones. These narrow floods that feed the inner $V_{CC-CORE}$ pins of the processor are non-ideal and for this reason, robust connections to capacitors are performed on the secondary side. Only three of the mid-frequency decoupling capacitors need to be placed on the primary side.

Table 21 lists four possible decoupling solutions recommended by Intel for the Intel Pentium M/Celeron M processor's VCC_CORE voltage rail. All the decoupling solutions are optimized to meet the Intel® IMVP-IV dynamic tolerance specifications for a load line of 3 mΩ. When a correct motherboard layout is used, all four options may result in comparable electrical performance. However, when comparing all four options, option 4 is the recommended $V_{CC-CORE}$ decoupling solution for Intel Pentium M/Celeron M processor-based systems. Option 4 offers the benefits of robust electrical performance, comparable efficiency, minimal cost, minimal motherboard surface area requirements, and lowest acoustic noise. Option 4 is a polymer-covered aluminum and ceramic-decoupling capacitor based solution that implements four polymer-covered aluminum (SP type) capacitors that have a low ESR of 12 mΩ each. It also uses 35 x 10 µF 0805 MLCC mid-frequency decoupling capacitors. Substitution of the 0805 capacitors with 1206 or other capacitors with higher inductance is not allowed. The other three $V_{CC-CORE}$ decoupling options are listed below:

In option 1, bulk decoupling is done with 12 x 150 µF polymer-covered *tantalum* capacitors (POSCAP type) and mid-frequency decoupling requires the use of 15 x 2.2 µF 0612 MLCC capacitors characterized by ~0.2 nH inductance (if correct layout is used).

Note: In this case, 1206 form factor capacitors cannot be substituted because their 1.2 nH inductance value is too high (6x higher than for 0612 capacitors). Though it may result in good electrical performance when implemented with a correct layout, option 1 occupies more area than the alternative options.

Option 2 uses purely ceramic decoupling capacitors, employing 40 x 10 µF 1206 MLCC capacitors as bulk decoupling and 15 x 2.2 µF 0612 MLCC capacitors. The layout for option 2 may be more difficult to implement when compared to option 4 due to the large 1206 form factor capacitors and the challenge in making a robust connection using 0612 capacitors. To achieve a surge-free transient response, option 2 needs to use 0.2 µH inductors that consequently lead to high ripple current and lower efficiency than the other solutions.

Option 3 uses five polymer-covered *aluminum* (SP type) capacitors that have a very low ESR of 15 mΩ so that only five such capacitors are required. It also uses 25 x 10 µF 1206 and 15 x 2.2 µF 0612 mid-frequency decoupling capacitors. Substitution of 0612 form factor capacitors with other form factor capacitors with higher ESL ratings is not allowed. Option 3 is similar to option 4 but it requires more motherboard area and has higher cost associated with it.

Table 21. Intel® Pentium® M/Celeron® M Processor $V_{CC-CORE}$ Decoupling Guidelines

Option	Description	Cap	ESR	ESL
1	Low-Frequency Decoupling (Polymer-Covered Tantalum – POSCAP, Neocap, KO Cap)	12 x 150 µF	36 mΩ (typ)/12	2.5 nH/12
	Mid-Frequency Decoupling (0612 MLCC, >= X5R)	15 x 2.2 µF	5 mΩ (typ)/15	0.2 nH/15
2	Low-Frequency Decoupling (1206 MLCC, >= X5R)	40 x 10 µF	5 mΩ (typ)/40	1.2 nH/40
	Mid-Frequency Decoupling (0612 MLCC, >= X5R)	15 x 2.2 µF	5 mΩ (typ)/15	0.2 nH/15
3	Low-Frequency Decoupling (Polymer-Covered Aluminum – SP Cap, A0 Cap)	5 x 330 µF	15 mΩ (max)/5	3.5 nH/5
	Low-Frequency Decoupling (1206 MLCC, >= X5R)	25 x 10 µF	5 mΩ (typ)/25	1.2 nH/25
	Mid-Frequency Decoupling (0612 MLCC, >= X5R)	15 x 2.2 µF	5 mΩ (typ)/15	0.2 nH/15
4	Low-Frequency Decoupling (Polymer-Covered Aluminum – SP CAP, AO Cap)	4 x 220 µF	12 mΩ (max)/4	3.5 nH/4
	Mid-Frequency Decoupling (0805 MLCC>= X5R)	35 x 10 µF	5 mΩ (typ)/35	0.6 nH/35

† Option 4 is to be used with small footprint (100 mm^2 or less) 0.36 µH ± 20% inductors.

Compared to options 1-3, option 4 represents cost- and space-optimized decoupling solutions that provide a competitive level of VRM performance and efficiency. Option 4 is the recommended $V_{CC-CORE}$ decoupling solution for Intel Pentium M/Celeron M processor-based systems and offers the best balance of performance, cost, and motherboard surface area requirements.

An example layout implementation of the recommended option 4 is illustrated in Figure 44, Figure 45, Figure 46, and Figure 47. Figure 44 and Figure 45 show how the four, low-frequency SP decoupling capacitors are placed on the secondary side and connected to the AF signal row of the Intel Pentium M/Celeron M processor pins with a solid $V_{CC-CORE}$ flood area along with eight of the mid-frequency 0805 ceramic mecoupling capacitors that are in between. To minimize the inductance of the SP capacitor connection for the layout style shown, the sense resistors' VRM feed is on the positive terminal side of the SP capacitors. In this case each of the SP capacitors is connected to two pairs of $V_{CC-CORE}$/GND vias on the positive terminal. Refer to Figure 45 for more details. When the VRM sense resistors connect from the negative side of the SP capacitors, two pairs of $V_{CC-CORE}$/GND vias are needed on both positive and negative terminals of the SP capacitors.

Thirty-two 10 µF, 0805 capacitors are placed on the secondary side (Layer 8) while the remaining three are placed on the primary side (Layer 1). Six of the 10-µF capacitors are placed outside the socket outline with a 90-mil (or closer) pitch (as shown in Figure 45) and are divided evenly on either side for the four 220 µF bulk capacitors (three to the left and three to the right of the SP capacitors). Each of these six 0805 capacitors have a pair of $V_{CC-CORE}$ and GND stitching vias next to both positive and negative terminals of the capacitors. The stitching vias connect to the internal ground and $V_{CC-CORE}$ planes, respectively.

The eight 10 µF, 0805 capacitors (see Figure 45) that are located between the SP capacitors and the Intel Pentium M/Celeron M processor $V_{CC-CORE}$ 'north corridor' pins also have a pair of $V_{CC-CORE}$ and GND stitching vias on both sides of their terminals. The negative terminals share $V_{CC-CORE}$ and GND stitching via connections with the six 0805 ceramic and SP capacitors mentioned previously. The positive terminal $V_{CC-CORE}$ and GND stitching connections are shared with the 'north corridor' and ground pins of the AF signal row of the Intel Pentium M/Celeron M processor socket.

To allow good current flow from the SP capacitors to the north side of the $V_{CC-CORE}$ corridor pins, it is recommended that these eight 10 µF 0805 capacitors be spaced 100 mils apart from each other even if the motherboard design rules allow tighter spacing. The 100 mil horizontal spacing allows some $V_{CC-CORE}$ flood between the capacitor ground pads (see Figure 45) as well as additional connections to internal Layers 3, 5, and 6 as illustrated in Figure 46. An additional nine 10 µF, 0805 capacitors are placed along the Y signal row of the Intel Pentium M/Celeron M processor pins on the secondary side below the $V_{CC-CORE}$ 'north corridor' pins under the shadow of the socket cavity. These nine capacitors are spaced 90 mils apart. Each of these nine 0805 capacitors have a pair of $V_{CC-CORE}$ and GND stitching vias next to both their positive and negative terminals. The stitching vias connect to the internal ground and $V_{CC-CORE}$ planes respectively. The positive terminal $V_{CC-CORE}$ and GND stitching vias are shared with the AA signal row of the Intel Pentium M/Celeron M processor's $V_{CC-CORE}$ and ground pins.

A wide $V_{CC-CORE}$ power delivery corridor flood on the secondary side of the motherboard connects the 0805 ceramic and SP capacitors that are placed to the north of the Intel Pentium M/Celeron M processor socket and the nine capacitors that are placed under the shadow of the socket cavity on the secondary side. The flood is as wide as the whole AF signal row and shall connect to all the $V_{CC-CORE}$ pins in signal rows Y, W, V, and U as illustrated in Figure 45.

The remaining nine (out of 32) 10 µF, 0805 (see Figure 44) capacitors on the secondary side are used to decouple the remainder of the 24 $V_{CC-CORE}$/GND pin pairs on the south side of the Intel Pentium M/Celeron M processor socket. These capacitors are placed along signal row G of the Intel Pentium M/Celeron M processor pins with a 90 mil (or smaller) pitch. Each of the nine capacitors has a pair of $V_{CC-CORE}$ and GND stitching vias on both sides of their terminals. Five out of nine capacitors share positive terminals with $V_{CC-CORE}$ and GND stitching via connections with signal row F's $V_{CC-CORE}$ and GND pins. The remaining four capacitors are placed next to the V_{CCP} pins of signal row F and have their own $V_{CC-CORE}$ vias but do share GND stitching vias.

As shown on the secondary side of Figure 44, a wide $V_{CC-CORE}$ flood connects the positive terminal of these nine capacitors to all 24 $V_{CC-CORE}$ pins of the Intel Pentium M/Celeron M processor pin-map on the south side including the $V_{CC-CORE}$ pins of signal rows K, J, H, and G. The reason for interruption of the $V_{CC-CORE}$ flood on the secondary side between the north and south sides is to allow the V_{CCP} corridor connection between the DATA and ADDR sides of the Intel Pentium M/Celeron M processor socket.

The primary side view in Figure 44 depicts two wide $V_{CC-CORE}$ floods that connect from the $V_{CC-CORE}$ stitching vias of the nine capacitors next to their negative terminal to the $V_{CC-CORE}$ pins of the two clusters of the 24 $V_{CC-CORE}$ pins in rows K, J, H, G, F, E, and D of the Intel Pentium M/Celeron M processor pin-map.

Note: The specific arrangement of the vias for the $V_{CC-CORE}$ dog bones to allow connection of all $V_{CC-CORE}$ BGA balls in this cluster of 24 pins to the $V_{CC-CORE}$ flood shapes on the primary.

As shown in Figure 44, the $V_{CC-CORE}$ floods are isolated between the north and south sides of the $V_{CC-CORE}$ pins of the Intel Pentium M/Celeron M processor socket on both the primary and secondary sides. The reason for the discontinuity of the $V_{CC-CORE}$ floods on the primary and secondary sides is to facilitate V_{CCP} power delivery. Consequently, this allows the V_{CCP} corridor

connections between the DATA and ADDR sides of the Intel Pentium M/Celeron M processor socket on the secondary side and the V_{CCP} flood for all DATA, ADDR, and legacy side V_{CCP} pins on the primary side (see Figure 44).

In reality, the north and south sides of the $V_{CC-CORE}$ floods are bridged by means of $V_{CC-CORE}$ planes in Layers 3, 5, and 6 as illustrated in Figure 46. Layers 3, 5, and 6 connect the $V_{CC-CORE}$ stitching vias next to the negative terminals of the nine capacitors on the north side with the $V_{CC-CORE}$ stitching vias next to the negative terminals of the nine capacitors on the south side. Layers 3, 5, and 6 $V_{CC-CORE}$ corridors use the fact that there are no Intel Pentium M/Celeron M processor FSB signals routed under the shadow of the Intel Pentium M/Celeron M processor socket cavity. All the $V_{CC-CORE}$ pins of the Intel Pentium M/Celeron M processor pin-map shall connect to the internal $V_{CC-CORE}$ planes of Layers 3, 5, and 6.

Special attention shall be given to not route any of the Intel Pentium M/Celeron M processor FSB or any other signal in a way that would block $V_{CC-CORE}$ connections to all the $V_{CC-CORE}$ power pins of the Intel Pentium M/Celeron M processor socket in Layers 3, 5, and 6. Figure 46 also depicts how the $V_{CC-CORE}$ planes on Layers 3, 5, and 6 make an uninterrupted connection all the way from the SP capacitors and sense resistors in the north side of the $V_{CC-CORE}$ corridor up to the south side of the 24 $V_{CC-CORE}$ pins of the Intel Pentium M/Celeron M processor socket. This continuous connection is imperative on all three internal layers because neither the primary nor the secondary side $V_{CC-CORE}$ floods make one continuous, robust connection from ‘north to south.’

The remaining three 10 µF, 0805 capacitors are placed on the primary side immediately above the shadow of the three 0805 capacitors on the secondary side and are placed at the same pitch (90 mils) as shown in Figure 44 and Figure 45. Two are on the side closest to the signal column 24 and 25 of the Intel Pentium M/Celeron M processor pins while one is on the side closest to signal column 2. The area between these three capacitors may be efficiently used for VRM sense resistor connections as illustrated in the primary side zoom view in Figure 45.

Special care shall be taken to provide a robust connection on the $V_{CC-CORE}$ floods on the primary side from the sense resistors to the $V_{CC-CORE}$ corridor pins on the north side of the Intel Pentium M/Celeron M processor socket. This robust connection is needed due to the presence of the GND dog bones on the primary side. The specific arrangement of $V_{CC-CORE}$ and GND vias as shown in Figure 45 shall be closely followed to provide a robust connection to the $V_{CC-CORE}$ floods for **ALL** $V_{CC-CORE}$ BGA balls and vias on the primary side in the AF, AE, AD, AC, AB, AA, Y, W, V, and U signal rows of the Intel Pentium M/Celeron M processor socket connecting all the way up to $V_{CC-CORE}$ stitching vias next to negative terminals of the nine 0805 capacitors placed under the socket cavity shadow.

Figure 47 depicts a magnified view of the recommended layout for the SP capacitor connections to minimize their inductance on the secondary side (Layer 8) of the motherboard. The $V_{CC-CORE}$ pin side of the capacitor has two $V_{CC-CORE}$ vias placed 82 mils above the $V_{CC-CORE}$ pad of the SP capacitor within the shadow of the SP capacitor. These two $V_{CC-CORE}$ vias are paired with two GND vias with a 50-mil offset to reduce the inductance of the connection between the capacitor and the plane. An additional pair of GND vias are placed 82 mils below the ground pad of the SP capacitor (also under the shadow of the SP capacitor body) to allow efficient stitching of ground planes on Layers 1, 2, 4, 7, and 8 in this area. Outside the shadow of the SP capacitors, the $V_{CC-CORE}$/GND via pairs of the SP capacitors are shared with the $V_{CC-CORE}$/GND via pairs of the 0805 capacitors. The placement of additional vias is not advised because this results in excessive perforation of the internal power planes due to the antipad voids. The pitch between the SP caps is 220 mils (or closer).

The layout concepts described in Figure 44 through Figure 47 result in an estimated $V_{CC-CORE}$ effective resistance of 0.58 mΩ and an effective inductance of ~4 pH. Despite the use of multiple power planes, this is still significant compared to the 3 mΩ load line target resistance and

compared to the 17.1 pH (600 pH/35) inductance of the thirty-five 0805 decoupling capacitors. When alternative layout solutions are used, they shall be implemented with a level of robustness greater than or equal to that in the previous example. In terms of robustness, this refers to creating a low resistance and inductance connection between the bulk and mid-frequency capacitors and the processor pins.

For options 1 to 3 in Table 21, the layout concepts described above and depicted in Figure 42 through Figure 47 are also similar in many respects. The main difference between the layout implementations of option 4 compared to options 1 to 3 is the use of 0612 reverse geometry capacitors. To be effective, these 0612 capacitors need to occupy the space within the Intel Pentium M/Celeron M processor socket cavity shadow on the secondary side for both the north and south sides of the pin-map as well as outside the socket shadow along the 'north power corridor' pins. Intel recommends the adoption of option 4 for the $V_{CC-CORE}$ decoupling. When option 1, 2, or 3 is used, the arrangement of the $V_{CC-CORE}$/GND vias in the Intel Pentium M/Celeron M processor pin field is recommended to be refined based on recommendations and layout example described above.

Figure 44. $V_{CC-CORE}$ Power Delivery and Decoupling Example – Option 4 (Primary and Secondary Side Layers)

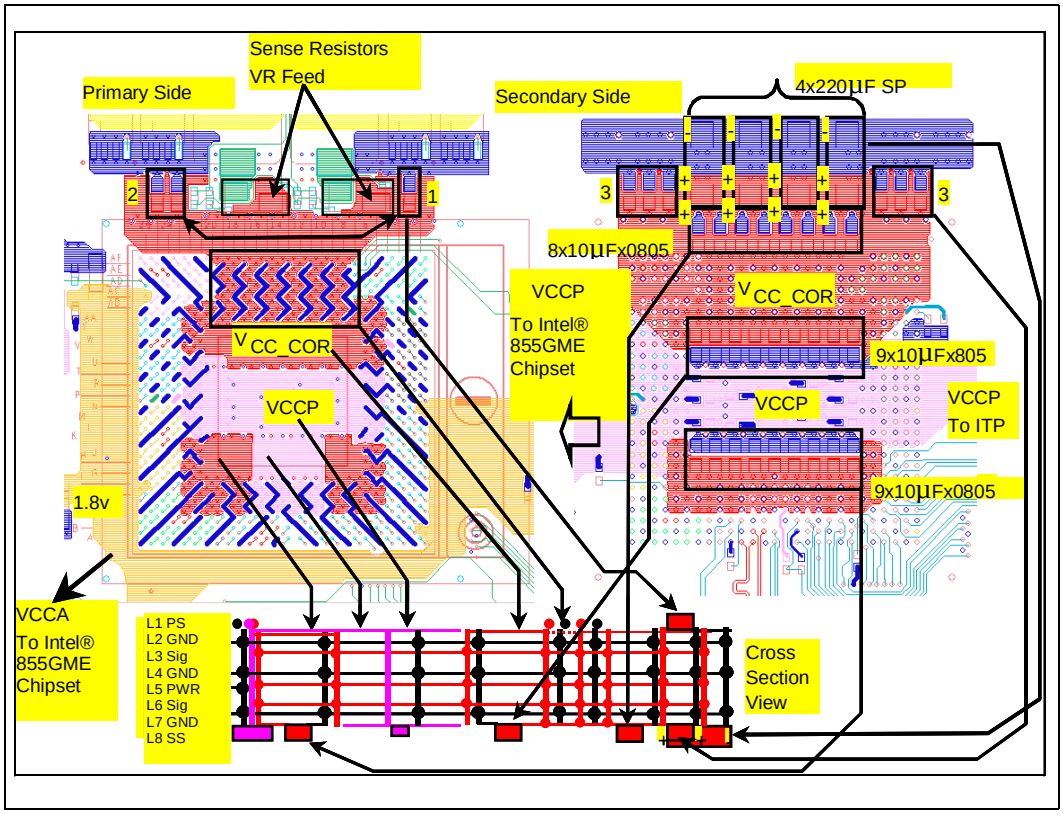


Figure 45. Intel® Pentium® M/Celeron® M Processor Core Power Delivery 'North Corridor' Zoom-in View

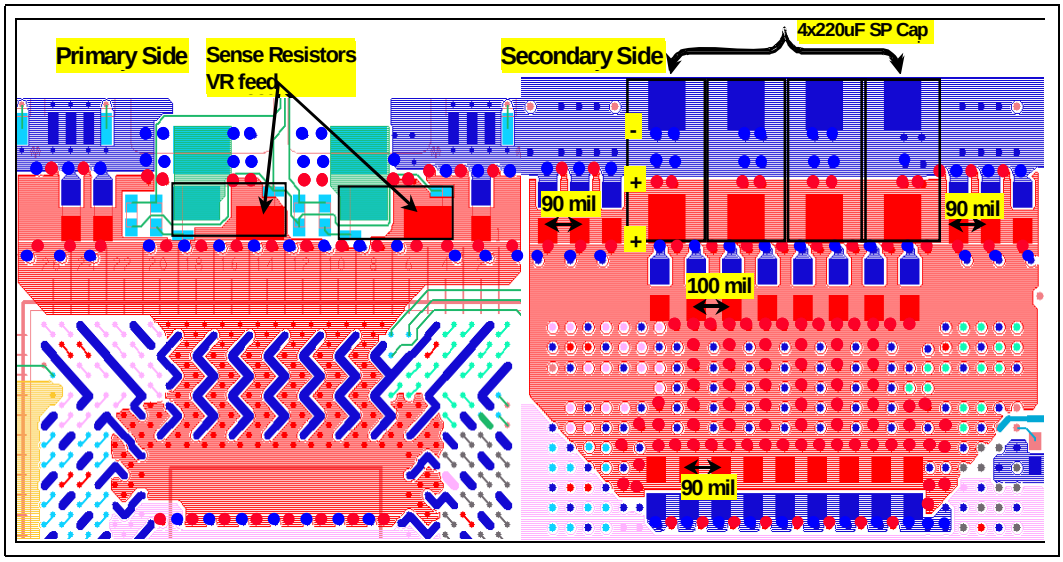


Figure 46. $V_{CC-CORE}$ Power Delivery and Decoupling Example – Option 4 (Layers 3, 5, and 6)

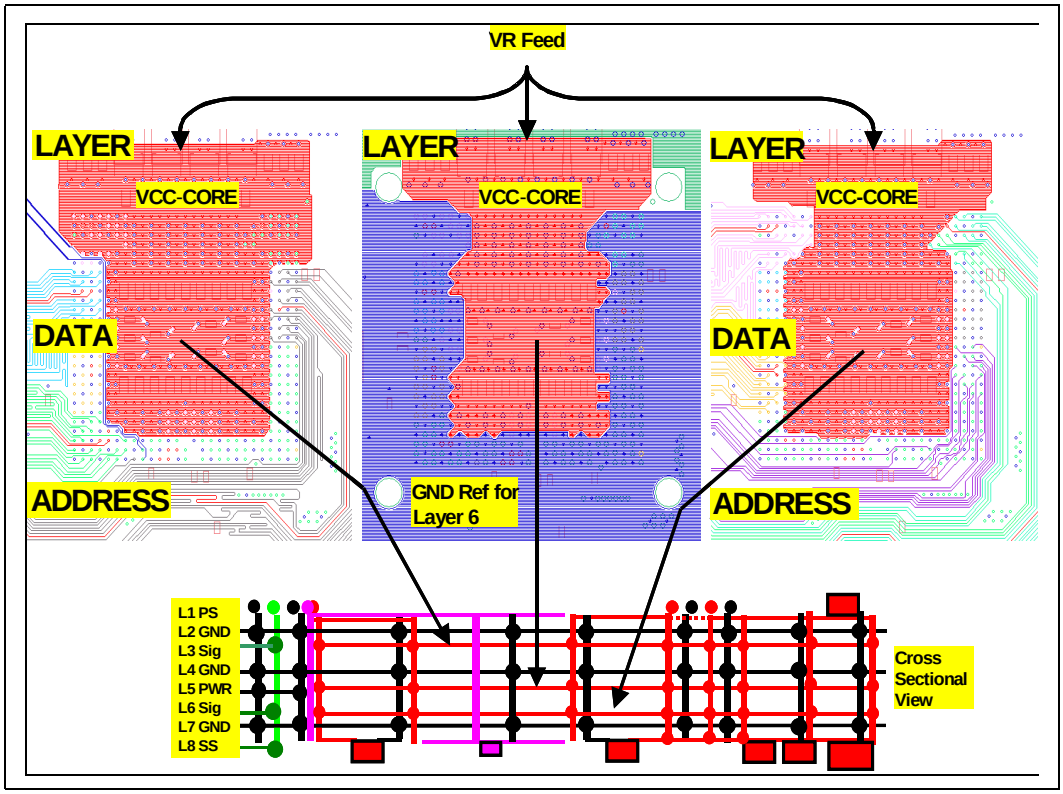
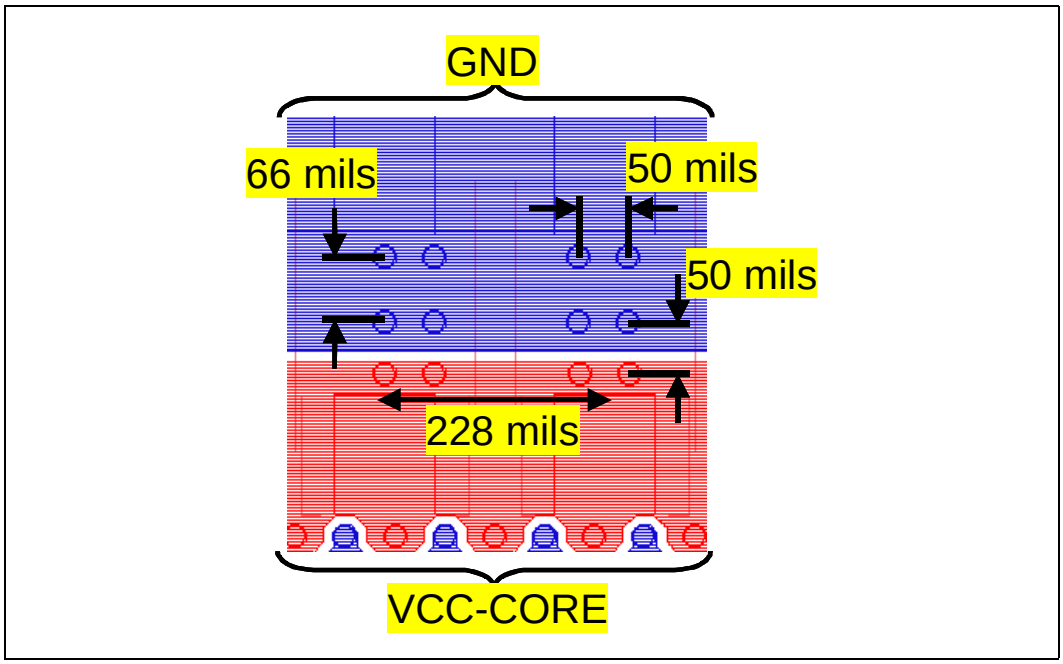


Figure 47. Recommended SP Cap Via Connection Layout (Secondary Side Layer)



4.4.4 Processor and GMCH VCCP Voltage Plane and Decoupling

The 400 MHz high-frequency operation of the Intel Pentium M/Celeron M processor and 82855GME's Intel Pentium M/Celeron M processor FSB requires careful attention to the design of the power delivery for VCCP (1.05 V) to the Intel Pentium M/Celeron M processor and GMCH. Refer to Table 22 that presents and summarizes the VCCP voltage rail decoupling requirements. Two 150 µF POSCAPs with an ESR of 42 mΩ shall be used for bulk decoupling. The recommendation is to place each POSCAP on the secondary side of the motherboard to minimize inductance.

- One capacitor shall be placed next to the Intel Pentium M/Celeron M processor socket.
- One capacitor shall be placed in close proximity to the GMCH package.
- Ten 0.1 µF X7R capacitors in a 0603 form factor shall be placed on the secondary side of the motherboard under the Intel Pentium M/Celeron M processor socket cavity next to the VCCP pins of the Intel Pentium M/Celeron M processor.
- Four capacitors shall be spread out near the data and address signal sides.
- Two capacitors shall be placed on the legacy signal side of the Intel Pentium M/Celeron M processor socket's pin-map.
- The Intel Pentium M/Celeron M processor and GMCH VCCP pins shall be shorted with a wide, VCCP plane, preferably on the secondary side such that it extends across the whole shadow of the Intel Pentium M/Celeron M processor FSB signals routed between the Intel Pentium M/Celeron M processor and 82855GME. The 1.05 volt VR feed point into the VCCP plane shall be roughly between the Intel Pentium M/Celeron M processor and 82855GME.

Table 22. Intel® Pentium® M/Celeron® M Processor V_{CCP} Decoupling Guidelines

Description	Cap	ESR	ESL	Notes
Low-Frequency Decoupling (Polymer-Covered Tantalum – POSCAP, Neocap, KO Cap)	2 x 150 µF	42 mΩ (typ)/2	2.5 nH/2	
High-Frequency Decoupling (0603 MLCC, >= X7R) Place next to the CPU	10 x 0.1 µF	16 mΩ (typ)/10	0.6 nH/10	

4.4.5 GMCH Core Voltage Plane and Decoupling

The VCC-GMCH (1.35 V) plane feeds the internal core logic of the 82855GME. VCC-GMCH does not employ on-package decoupling. To ensure accurate VCC-GMCH voltage on the GMCH die, follow the decoupling guidelines listed in Table 24 on page 108. The component form factors, layout style, and decoupling capacitor values must be used with no deviation.

4.5 Power and Sleep State Definitions

Suspend-To-RAM (STR): In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered.

Full-power operation: During full-power operation, all components on the motherboard remain powered. Full-power operation includes both the full-on operating state and the S1 (PROCESSOR stop-grant state) state.

Suspend operation: During suspend operation; power is removed from some components on the motherboard. The customer reference board supports three suspend states: Suspend-to-RAM (S3), Suspend-to- Disk (S4), and Soft-off (S5).

Power rails: An ATX power supply has 6 power rails: +5 V, -5 V, +12 V, -12 V, +3.3 V, 5 Vsb. In addition to these power rails, several other power rails are created with voltage regulators.

Core power rail: Power rail that is only on during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX 12 V power supply are +5 V, -5 V, +12 V, -12 V, +3.3 V.

Standby power rail: A power rail that is on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is: 5 Vsb (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.

Derived power rail: A derived power rail is any power rail generated from another power rail using an onboard voltage regulator. For example, 3.3 Vsb is usually derived (on the motherboard) from 5 Vsb using a voltage regulator.

Dual power rail: A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during suspend operation and derived from a core supply during full-power operation.

Note: The voltage on a dual power rail may be misleading.

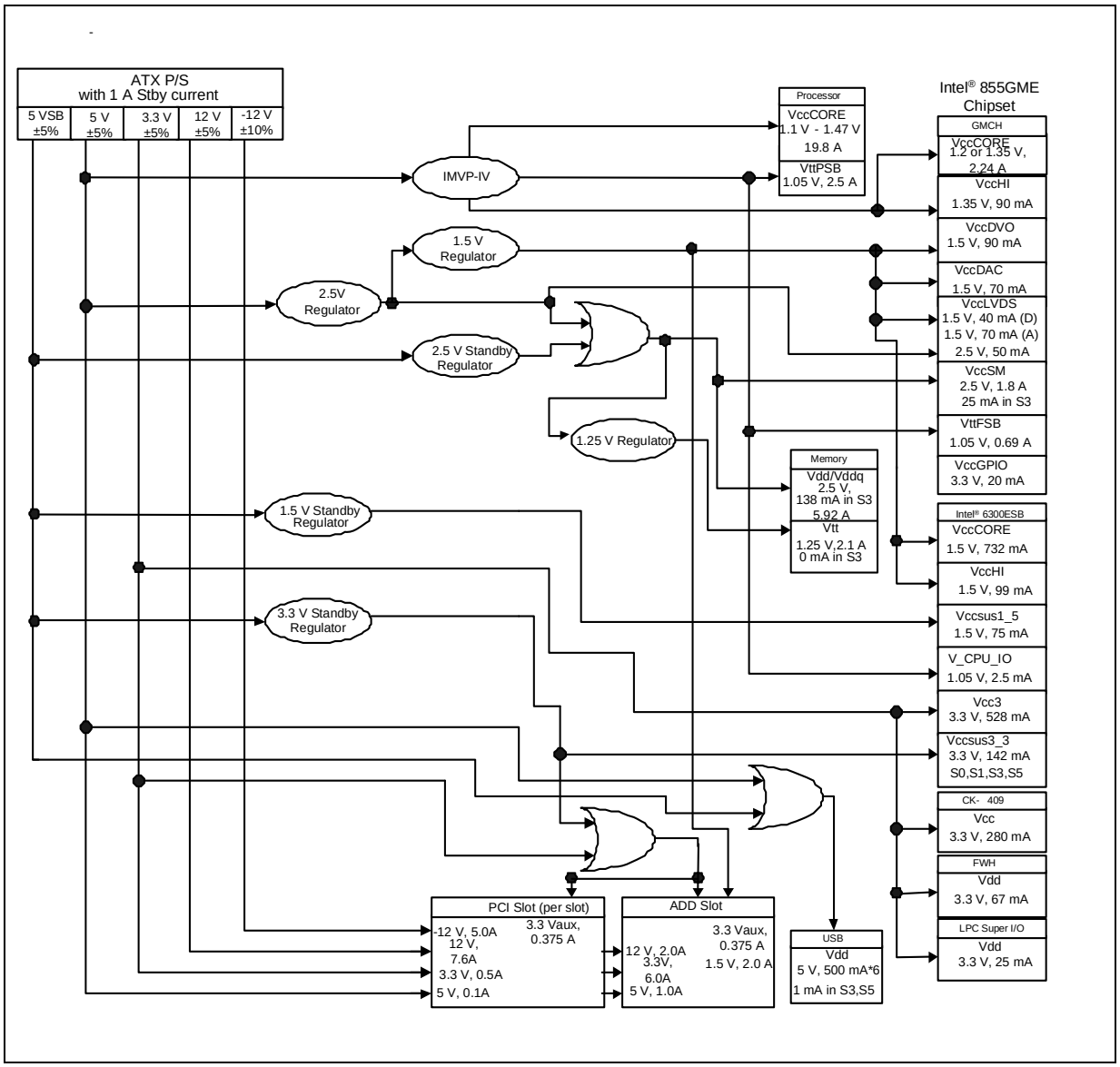
4.6 Power Delivery Map

Figure 48 depicts power delivery map for an example Intel 855GME chipset/6300ESB platform.

During STR, only the necessary devices are powered. These devices include: main memory, the 6300ESB resume well, PCI wake devices (via 3.3 Vaux), AC'97, and USB. To ensure that enough power is available during STR, a thorough power budget shall be completed. Power requirements shall include each device's power requirements, both in suspend and in full-power. The power requirements shall be compared with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create dual power rails.

The solutions in this Design Guide are only examples. Many power distribution methods achieve similar results. When deviating from these examples, it is critical to consider the effect of a change.

Figure 48. Platform Power Delivery Map



Note: Contact your Intel sales field representative for more information on the electrical requirements for DC-to-DC voltage regulator (IMVP-IV) for the Pentium® M Processor/Intel Celeron® M processor. Consult the appropriate component EDS or datasheet for complete specifications.

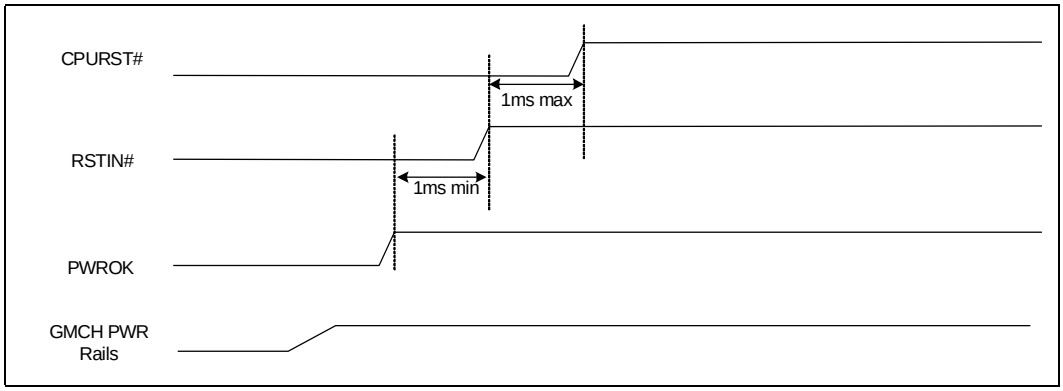
4.7 Intel 855GME Chipset Platform Power-Up Sequence

The following sections describe the power-on timing sequence for Intel 855GME chipset Graphics Memory Controller Hub (82855GME) based platforms.

4.7.1 GMCH Power Sequencing Requirements

All GMCH power rails shall be stable before PWROK is asserted. The power rails may be brought up in any order desired. **However, good design practice would have all GMCH power rails come up as close in time as practical, with the core voltage (1.35 V) coming up first.** RSTIN#, which brings GMCH out of reset, shall be deasserted only after PWROK has been active for 1 ms. After GMCH is out of reset, it deasserts CPURST# within 1 ms.

Figure 49. GMCH Power-up Sequence



4.7.2 6300ESB Power Sequencing Requirements

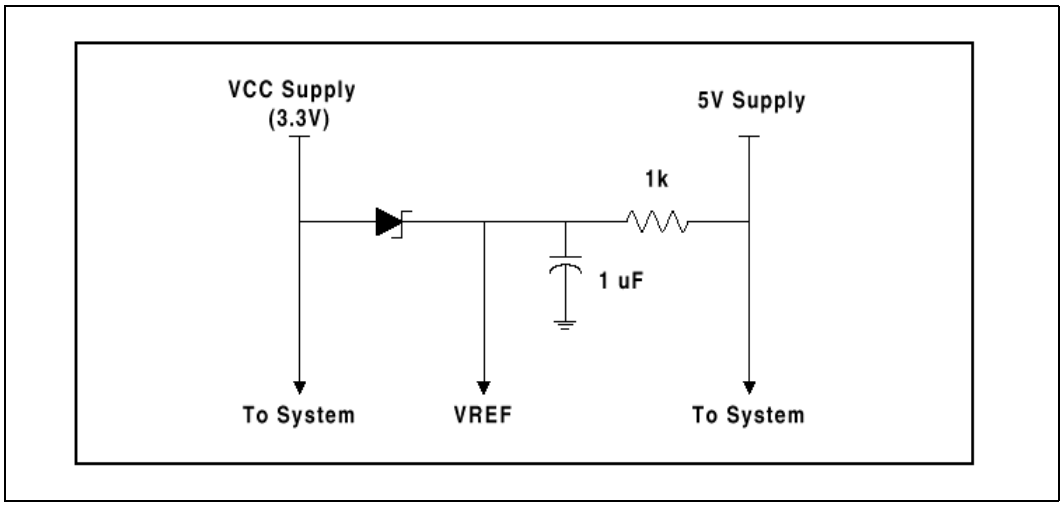
4.7.2.1 V_{5REF}/3.3V Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the 6300ESB. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V. It must also power down after or simultaneous to Vcc3_3. These rules must be followed to ensure the safety of the 6300ESB. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 50 shows a sample implementation of how to satisfy the V5REF/3.3 V sequencing rule.

This rule also applies to V5REF_Sus and VccSus3_3. However, in most platforms, the VccSus3_3 rail is derived from the 5 VSB through a voltage regulator and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus (which is derived directly from

VccSus5) will always be powered up before VccSus3_3 and thus circuitry to satisfy the sequence requirement is not needed. However, in platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be observed in the platform design as described above. See Figure 50.

Figure 50. Example V_{5REF}/3.3 V Sequencing Circuitry



4.7.2.2 3.3V/1.5V Power Sequencing

The Intel® 6300ESB has power sequencing requirements for the 3.3 V and 1. 5V rails in respect to each other. This requirement is as follows: The 3.3 V and 1.5 V rails must power up or down simultaneously. When I/O pads are powered by the 3.3 V rail before the core is powered by the 1.5 V rail, a current spike anomaly will be observed.

4.7.3 PCI-X Power Sequencing

The 1.5 V voltage must be valid before the first CLK66 pulse is driven into the 6300ESB ICH. This can be guaranteed by gating the CK409 clocks using a power good signal from the 1.5V regulator. When the first CLK66 pulse is driven before 1.5V is valid, the PCI-X PLL may fail to correctly lock.

4.7.4 DDR Memory Power Sequencing Requirements

No DDR-SDRAM power sequencing requirements are specified during power up or power down if the following criteria are met:

- VDD and VDDQ to memory devices are driven from a single power converter output.
- VTT is limited to 1.44 V (reflecting VDDQ(max)/2 + 50 mV VREF variation + 40 mV VTT variation).
- VREF tracks VDDQ/2.
- A minimum resistance of 42 Ω (22 Ω series resistor + 22 Ω parallel resistor ± 5 percent tolerance) limits the input current from the VTT supply into any pin.

When the above criteria cannot be met by the system design, Table 23 must be adhered to during power up. Refer to *Intel® DDR 200 JEDEC Spec Addendum* for more details.

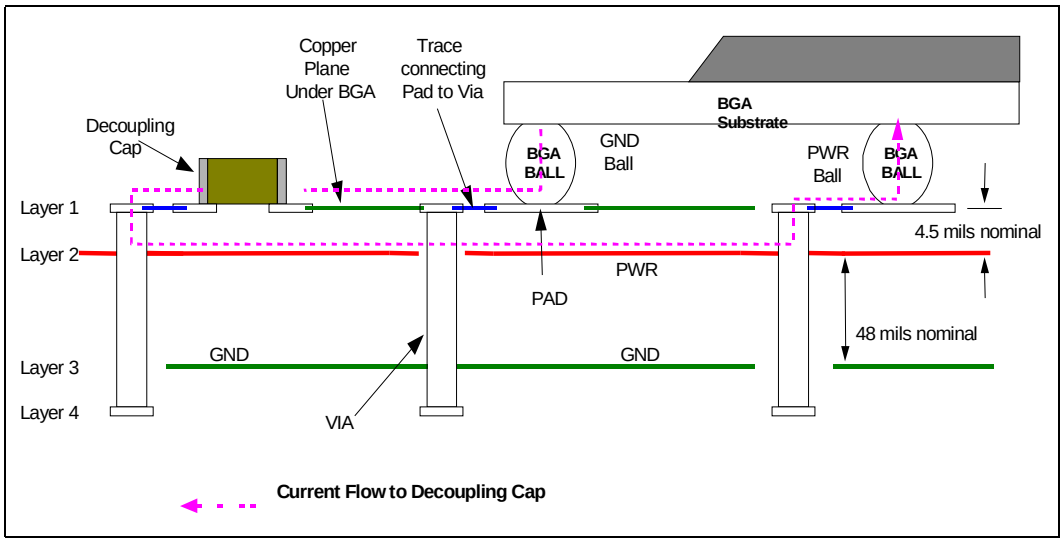
Table 23. DDR Power-Up Initialization Sequence

Voltage Description	Sequencing	Voltage Relationship to Avoid Latch-up
VDDQ	After or with VDD	< VDD + 0.3 V
VTT	After or with VDDQ	< VDDQ + 0.3 V
VREF	After or with VDDQ	< VDDQ + 0.3 V

4.8 Intel 855GME Chipset Platform Power Delivery Guidelines

Each component is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. Intel recommends that the developer use the amount of decoupling capacitors specified in this document to ensure the component maintains stable supply voltages. The capacitors shall be placed as close to the package as possible. Rotate caps that sit over power planes so that the loop inductance is minimized (see Figure 51). The basic theory for minimizing loop inductance is to consider which voltage is on Layer 2 (power or ground) and spin the decoupling cap with the opposite voltage toward the ball grid array (BGA). This greatly minimizes the total loop inductance. Intel recommends that for prototype board designs, the designer shall include pads for extra power plane decoupling caps.

Figure 51. Example for Minimizing Loop Inductance



4.8.1 Intel 855GME Chipset and Decoupling Guidelines

Decoupling in Table 24 is based on the voltage regulator solution used on the customer reference board design.

Table 24. GMCH Decoupling Recommendations

Pin Name	Configuration	F	Qty	TYPE	Notes
VCC	Connect to VCC1_35S	0.1 µF 10 µF 150 µF	4 1 2	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	1 X 0.1 µF within 200 mils 3 X 0.1 µF on bottom side
VTTLF	Connect to VCCP	0.1 µF 10 µF 150 µF	2 1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	2 X 0.1 µF on bottom side
VTTHF	Connect to caps directly	0.1 µF	5	XR7, 0603, 16 V, 10%	
VCCHL	Connect to VCC1_35S	0.1 µF 10 µF	2 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20%	1 X 0.1 µF within 200 mils 1 X 0.1 µF on bottom side
VCCSM	Connect to VCCSus2_5	0.1 µF 150 µF	11 2	XR7, 0603, 16 V, 10% TANT, D, 10 V, 20%	Refer to Section 4.8.1.1 for more information.
VCCDVO	Connect to VCC1_5S	0.1 µF 10 µF 150 µF	2 1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	1 X 0.1 µF within 200 mils 1 X 0.1 µF on bottom side
VCCDLVDS	Connect to VCC1_5S	0.1 µF 22 µF 47 µF	1 1 1	XR7, 0603, 16 V, 10% TANT, B, 10 V, 20% TANT, D, 10 V, 20%	1 X 0.1 µF within 200 mils
VCCTXLVDS	Connect to VCCSus2_5	0.1 µF 22 µF 47 µF	3 1 1	XR7, 0603, 16 V, 10% TANT, B, 10 V, 20% TANT, D, 10 V, 20%	1 X 0.1 µF within 200 mils 2 X 0.1 µF on bottom side
VCCGPIO	Connect to Vcc3_3S	0.1 µF 10 µF	1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20%	
SMVREF		0.1 µF	1	XR7, 0603, 16 V, 10%	1 X 0.1 µF on bottom side

4.8.1.1 GMCH VCCSM Decoupling

For the VCCSM pins of the GMCH, a minimum of eleven 0603 form factor, 0.1 µF, high-frequency capacitors is required and must be placed within 150 mils of the GMCH package. The capacitors shall be evenly distributed along the GMCH DDR system memory interface and placed perpendicular to the GMCH with the power (2.5 V) side of the capacitors facing the GMCH.

- Every GMCH ground and VCCSM power ball in the system memory interface shall have its own via.
- Each capacitor shall also have its own 2.5 V via within 25 mils of the capacitor pad for connecting to a 2.5 V copper flood. The traces from the capacitors shall also be wide and connect to the outer row of balls on the GMCH.
- The ground end of each capacitor must connect to the ground flood and to the ground plane through a via. Each via shall be as close to the associated capacitor pad as possible, within 25 mils and with as thick a trace as possible.
- The system memory interface also requires low frequency decoupling. Place two 150 µF electrolytic capacitors between the GMCH and the first DIMM connector.

4.8.1.2 DDR SDRAM VDD Decoupling

Discontinuities in the DDR signal return paths occur when the signals transition between the motherboard and the DIMMs. To account for this ground to 2.5 V discontinuity, a minimum of nine 0603 form factor 0.1 µF high-frequency bypass capacitors is required between the DIMMs to help minimize any anticipated return path discontinuities that shall be created. The capacitors shall be distributed as evenly as possible between the two DIMMs.

- Wide ground trace from each capacitor shall be connect to a via that transitions to the ground plane. Each ground via shall be placed as close to the ground pad as possible.
- Wide 2.5 V trace from each capacitor shall connect to a via that transitions to the 2.5 V copper flood. Each via shall be placed as close to the capacitor pad as possible. Each capacitor pad shall also connect to the closest 2.5 V DIMM pin on either the first or second DIMM connector with a wide trace.
- The DDR DIMMs also require bulk decoupling in addition to what is required by the GMCH. Place a minimum of four 100-150 µF capacitors near the DIMM connectors.

4.8.1.3 DDR VTT Decoupling Placement and Layout Guidelines

The VTT termination rail must be decoupled using high-speed bypass capacitors, one 0603 form factor, 0.1 µF capacitor per two DDR signals. They must be placed no more than 100 mils from the termination resistors.

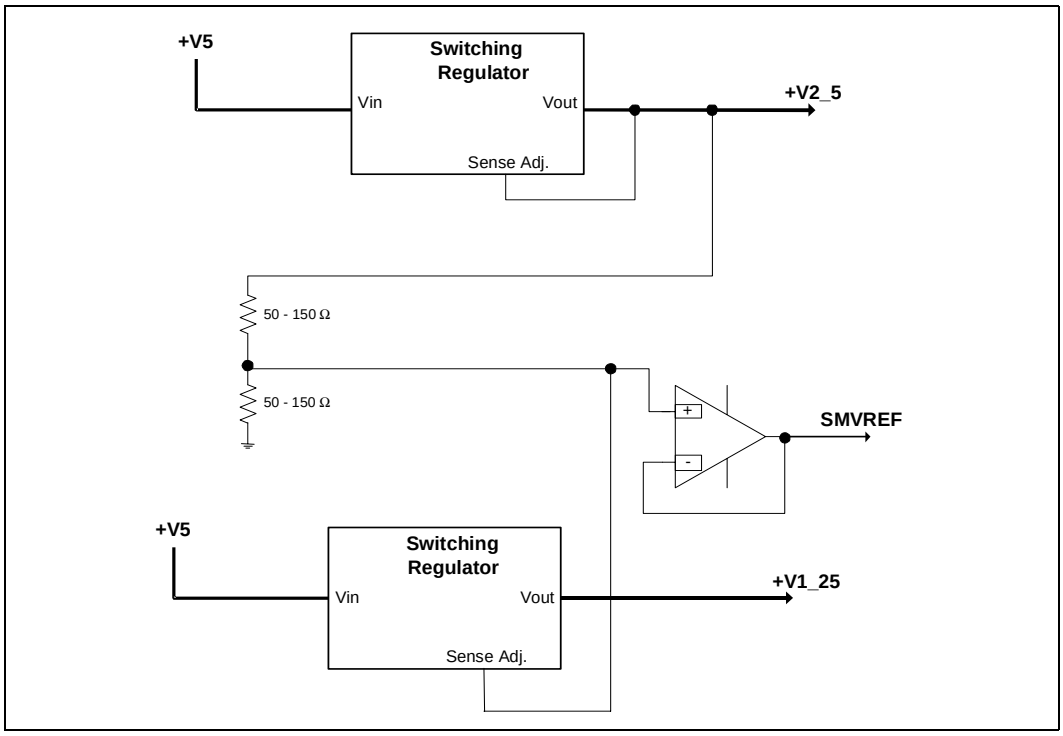
- A VTT copper flood must be used. The decoupling capacitors must be spread out across the termination rail so that all the parallel termination resistors are near high-frequency capacitors.
- Each capacitor ground via shall be as close to the capacitor pad as possible, within 25 mils with as thick a trace as possible.
- Place one 4.7 µF ceramic capacitor on each end of the VTT termination rail, and place one 4.7 µF ceramic capacitor near the center of the termination rail. The power end of these capacitors must connect directly to the VTT termination rail and the ground end is connected to ground.
- For low-frequency bulk decoupling at the VTT termination rail, evenly place four 470 µF capacitors.

4.8.2 DDR Memory Power Delivery Design Guidelines

The focus of these GMCH guidelines is to minimize signal integrity problems and improve power delivery to the GMCH system memory interface and the DDR memory DIMMs. This section discusses the DDR memory system voltage and current requirements as determined at publishing of this document. This document is not the original source for these specifications. Figure 52 depicts the implementation of 2.5 V, 1.25 V and SMVREF on the CRB only as an example. It is the responsibility of the system designer to ensure that the power requirements for the DDR and GMCH are met. Refer to the following documents for the latest details on voltage and current requirements found in this design guide.

- *JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification*
- *JEDEC 184-Pin Unbuffered DDR DIMM Specification*
- *Intel 855GM/855GME Chipset (GMCH) Datasheet*

Figure 52. DDR Power Delivery Block Diagram



Note: +V_1.25 may optionally be on the switch rail and turned off in either S3 or S4. This is only a block diagram. It is the responsibility of the system designer to ensure that the timing requirements for the DDR memory devices and GMCH are met.

4.8.2.1 2.5 V Power Delivery Guidelines

The 2.5 V power for the GMCH system memory interface and the DDR DIMMs is delivered around the DDR command, control, and clock signals. Special attention must be paid to the 2.5 V copper flooding to ensure proper GMCH and DIMM power delivery. This 2.5 V flood must extend from the GMCH 2.5 V power vias all the way to the 2.5 V DDR voltage regulator and its bulk capacitors. The 2.5 V DDR voltage regulator must connect to the 2.5 V flood with a minimum of six vias. The DIMM connector 2.5 V pins as well as the GMCH 2.5 V power vias must connect to the 2.5 V copper flood.

In the areas where the copper flooding necks down around the GMCH make sure to keep these neck down lengths as short as possible. The 2.5 V copper flooding under the DIMM connectors must encompass all the DIMM 2.5 V pins and must be solid except for the small areas where the clocks are routed within the DIMM pin field to their specified DIMM pins.

Note: A minimum of 12 mil isolation spacing shall be maintained between the copper flooding and any signals on the same layer.

Table 25 depicts the voltage and current specifications for each the GMCH and memory reference and termination voltages. For convenience, tolerances are given in both percentage and volts, although validation shall be done using the specifications exactly as they are written. When the

spec states a tolerance in terms of volts (e.g., VREF says ± 0.025 V), that specific voltage tolerance shall be used, not a percentage of the measured value. Likewise, percentages shall be used where stated.

As shown in the tables, only the 2.5 V supply has an absolute specification. The 1.25 V supply for both VREF and VTT need to track the 2.5 V supply closely.

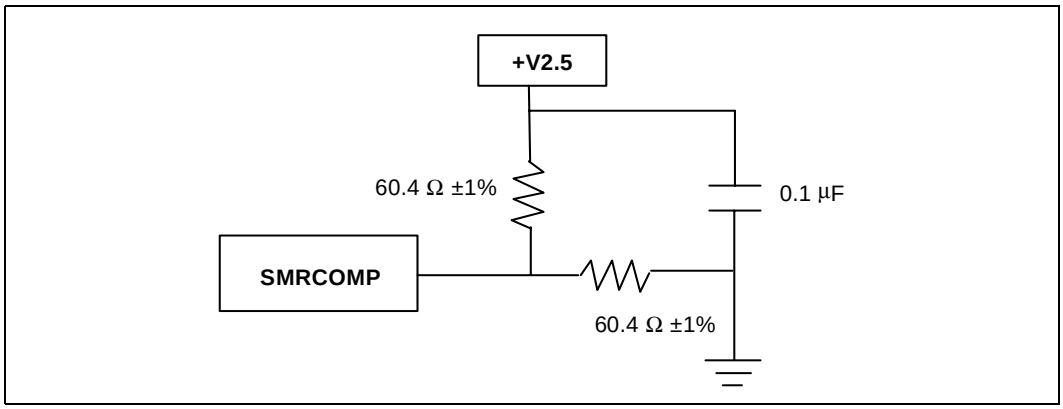
4.8.2.2 GMCH and DDR SMVREF Design Recommendations

There is one SMVREF pin on the GMCH that is used to set the reference voltage level for the DDR system memory signals (SMVREF). The voltage level that needs to be supplied to this pin must be equal to VCCSM/2. As shown in Figure 52 an OpAmp buffer is recommended to generate SMVREF from the 2.5 V supply. This shall be used as the VREF signals to both the DDR memory devices and the SMVREF signal to the GMCH. Note that SMVREF must be provided in S3.

4.8.2.3 DDR SMRCOMP Resistive Compensation

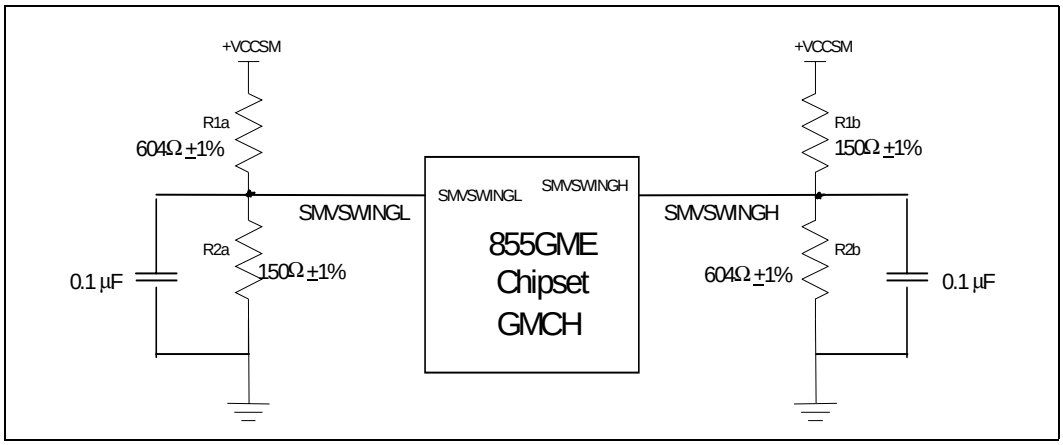
The GMCH requires a system memory compensation resistor, SMRCOMP, to adjust buffer characteristics to specific board and operation environment characteristics. Refer to the *Intel® 855GM/855GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet* and Figure 53 for details on resistive compensation. The SMRCOMP signal shall be routed with as wide a trace as possible. It shall be a minimum of 12 mils wide and be isolated from other signals with a minimum of 10 mils spacing.

Figure 53. GMCH SMRCOMP Resistive Compensation



The GMCH's system memory resistive compensation mechanism also requires the generation of reference voltages to the SMVSWINGL and SMVSWINGH pins. The schematic for SMVSWINGL and SMVSWINGH voltage generation is illustrated in Figure 54. Two resistive dividers with R1b = R2a = 150 Ω ± 1% and R1a = R2b = 604 Ω ± 1% generate the SMVSWINGL and SMVSWINGH voltages. SMVSWINGL and SMVSWINGH components shall be placed within 0.5 inches of their respective pins and connected with a 15 mil wide trace. To avoid coupling with any other signals, maintain a minimum of 25 mils of separation to other signals.

Figure 54. GMCH System Memory Reference Voltage Generation Circuit



4.8.2.4 DDR VTT Termination

The recommended topology for DDR-SDRAM Data, Control, and Command signal groups requires that all these signals be terminated to a 1.25 V source, VTT, at the end of the memory channel opposite the GMCH. It is recommended that this VTT be generated from the same source as used for VCCSM, and not be used for GMCH and DDR SMVREF. This is because SMVREF has a much tighter tolerance and VTT may vary more easily depending on signal states. A solid 1.25 V termination island shall be used for this purpose and be placed on the surface signal layer, just beyond the last DIMM connector and must be at least 50 mils wide.

The data and command signals shall be terminated using one resistor per signal. Resistor packs and ± 5 percent tolerant resistors are acceptable for this application. Only signals from the same DDR signal group may share a resistor pack. Refer to Section 5 for system memory guidelines.

4.8.2.5 DDR SMRCOMP and VTT 1.25 V Supply Disable in S3/Suspend

Regardless of how these 1.25 V supplies for GMCH are generated, they may be disabled during the S3 suspend state to further save power on the platform. This is possible because the GMCH does not require the enabling of resistive compensation during suspend. **However, some DDR memory devices may require a valid reference voltage during suspend**. It is the responsibility of the system designer to ensure that requirements of the DDR memory devices are met.

Note: The 2.5 V VCCSM power pins of the GMCH and the VDD power pins of the DDR memory devices do need to be on in S3 state.

4.8.3 Other GMCH Reference Voltage and Analog Power Delivery

4.8.3.1 GMCH GTLVREF

For GMCH, the GTLREF generation circuit has been broken down into three separate voltage references: host data reference voltage (HDVREF[2:0]), host address reference voltage (HAVREF) and host common clock reference voltage (HCCVREF). Maximum length from pin to voltage divider for each reference voltage shall be less than 0.5 inches. Ten-mil wide traces are recommended. GMCH VREF may be maintained as individual voltage dividers as shown in Figure 55, Figure 56, and Figure 57.

Figure 55. GMCH HDVREF[2:0] Reference Voltage Generation Circuit

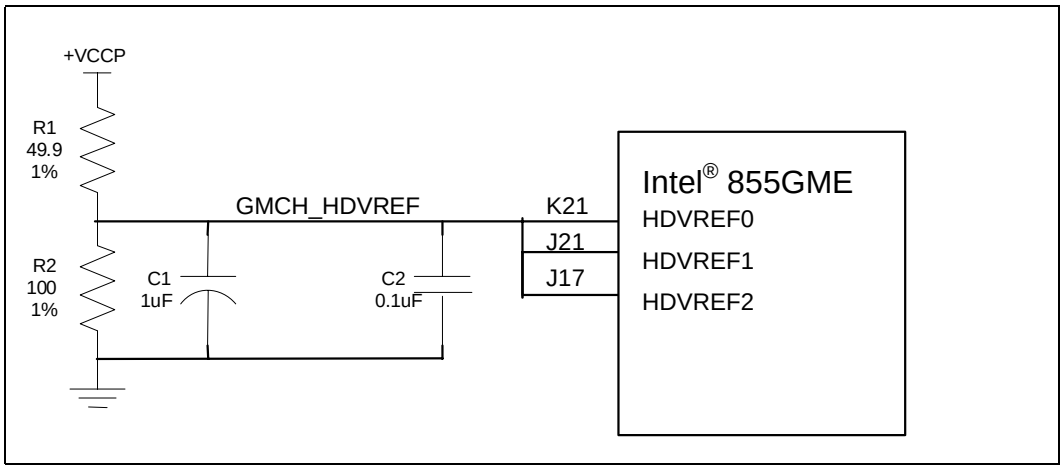


Figure 56. GMCH HAVREF Reference Voltage Generation Circuit

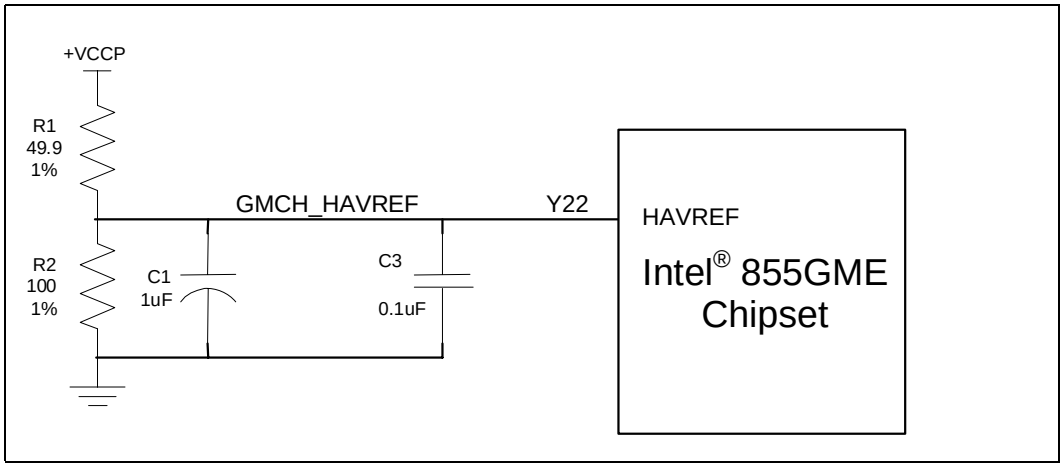
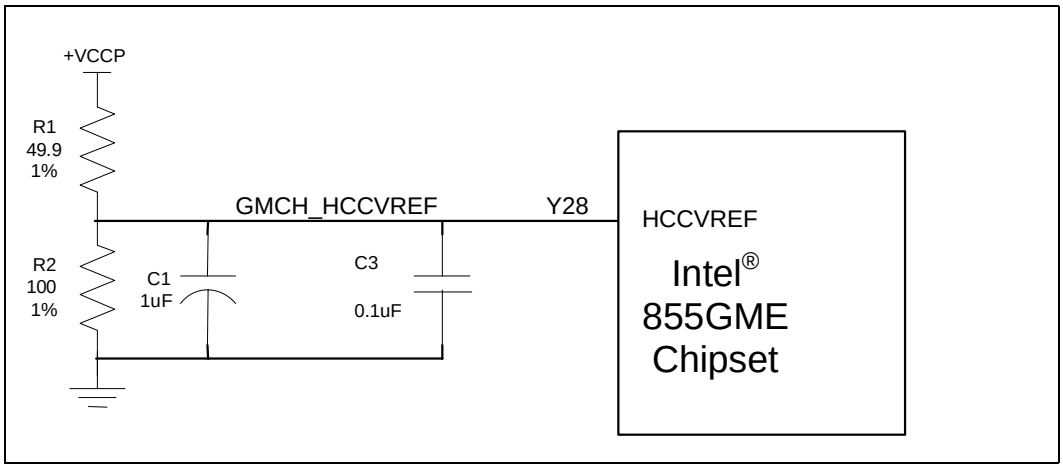


Figure 57. GMCH HCCVREF Reference Voltage Generation Circuit



Sample layout for GMCH VREF generation is shown in Figure 58 and Figure 59.

Figure 58. Primary Side of the Motherboard Layout

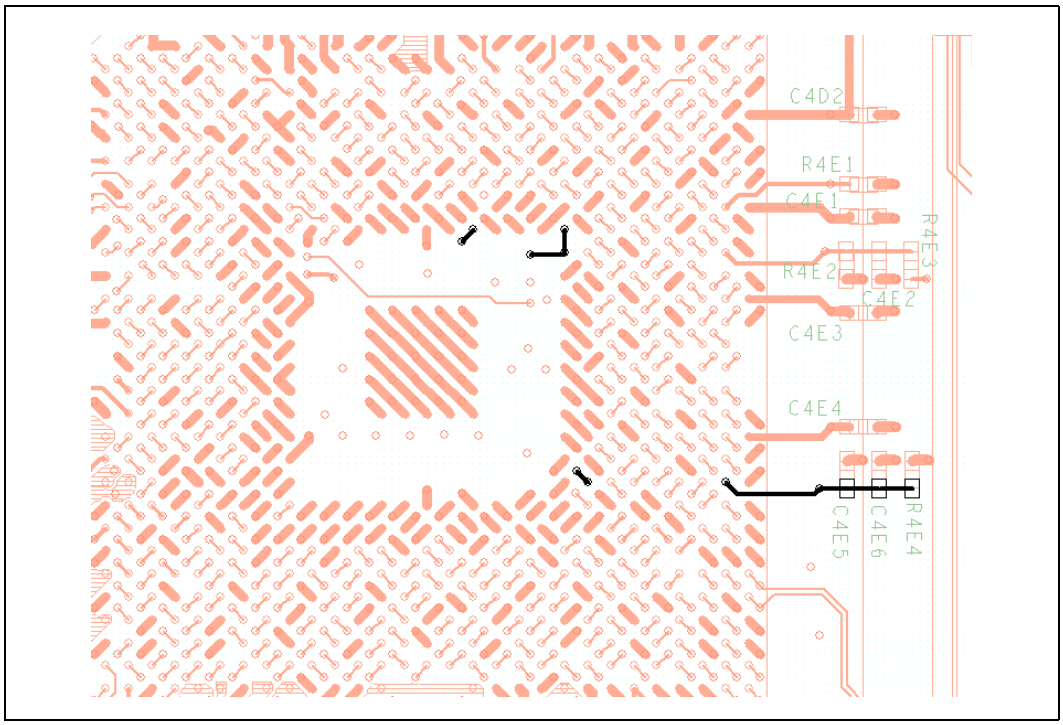
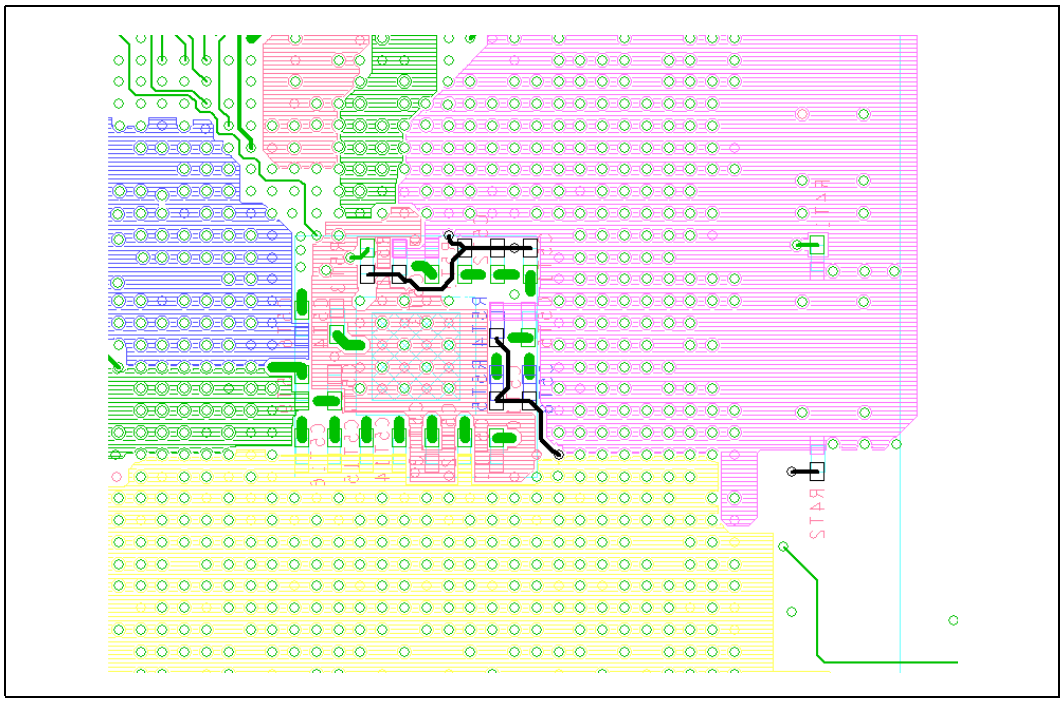


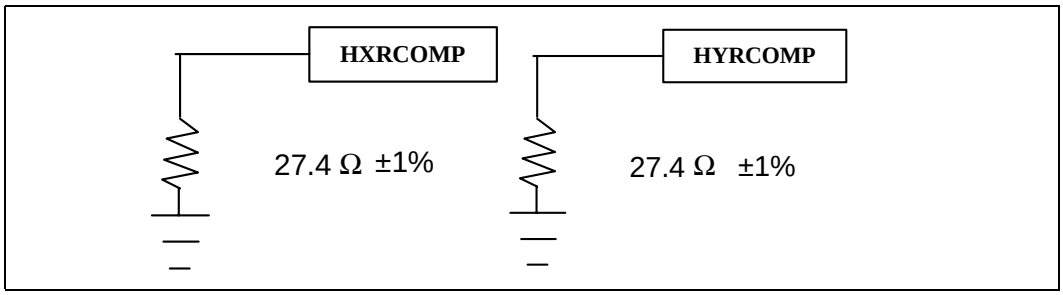
Figure 59. Secondary Side of the Motherboard Layout



4.8.3.2 GMCH AGTL+ I/O Buffer Compensation

The HXRCOMP and HYRCOMP pins of the GMCH shall each be pulled-down to ground with a 27.4 Ω ± 1 percent resistor (see Figure 60). The maximum trace length from pin to resistor shall be less than 0.5 inches and shall be 18 mil wide to achieve the Zo = 27.4 Ω target. Also, the routing for HRCOMP shall be at least 25 mils away from any switching signal.

Figure 60. GMCH HXRCOMP and HYRCOMP Resistive Compensation

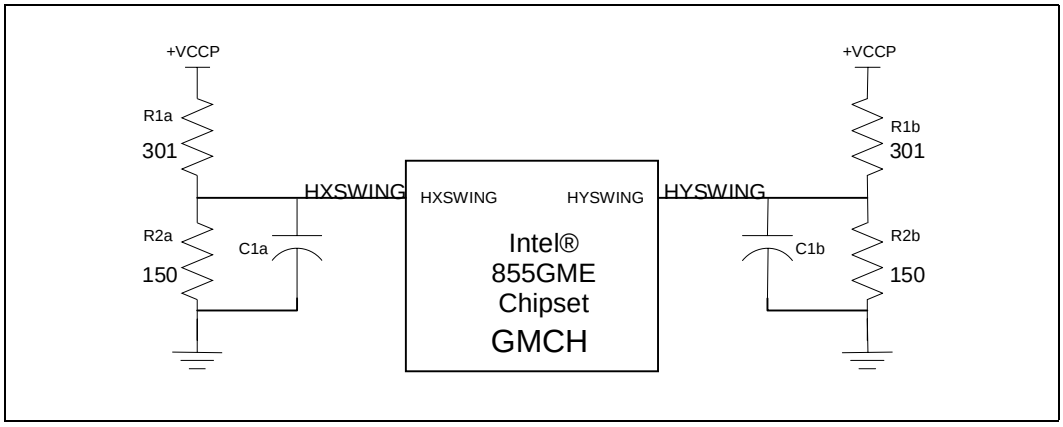


4.8.3.3 GMCH AGTL+ Reference Voltage

The GMCH's AGTL+ I/O buffer resistive compensation mechanism also requires the generation of reference voltages to the HXSWING and HYSWING pins with a value of 1/3*VCCP. Implementations for HXSWING and HYSWING voltage generation are illustrated in Figure 61. Two resistive dividers with R1a = R1b = 301 Ω ± 1 percent and R2a = R2b = 150 Ω ± 1 percent generate the HXSWING and HYSWING voltages. C1a = C1b = 0.1 µF act as decoupling capacitors and connect HXSWING and HYSWING to VCC_CORE. HSWING components shall

be placed within 0.5 inches of their respective pins and connected with a 15 mil wide trace. To avoid coupling with any other signals, maintain a minimum of 25 mils of separation to other signals.

Figure 61. GMCH HXSWING and HYSWING Reference Voltage Generation Circuit



4.8.3.4 GMCH Analog Power

Table 25 summarizes the eight analog circuits that require filtered supplies on the GMCH. They are: VCCASM, VCCQSM, VCCAHPLL, VCCADPLLA, VCCADPLLB, VCCADAC, VCCAGPLL, and VCCALVDS. VCCADAC, VCCAGPLL, and VCCALVDS do not require an RLC filter but do require decoupling capacitors. Figure 62 depicts an example analog supply filter.

Figure 62. Example Analog Supply Filter

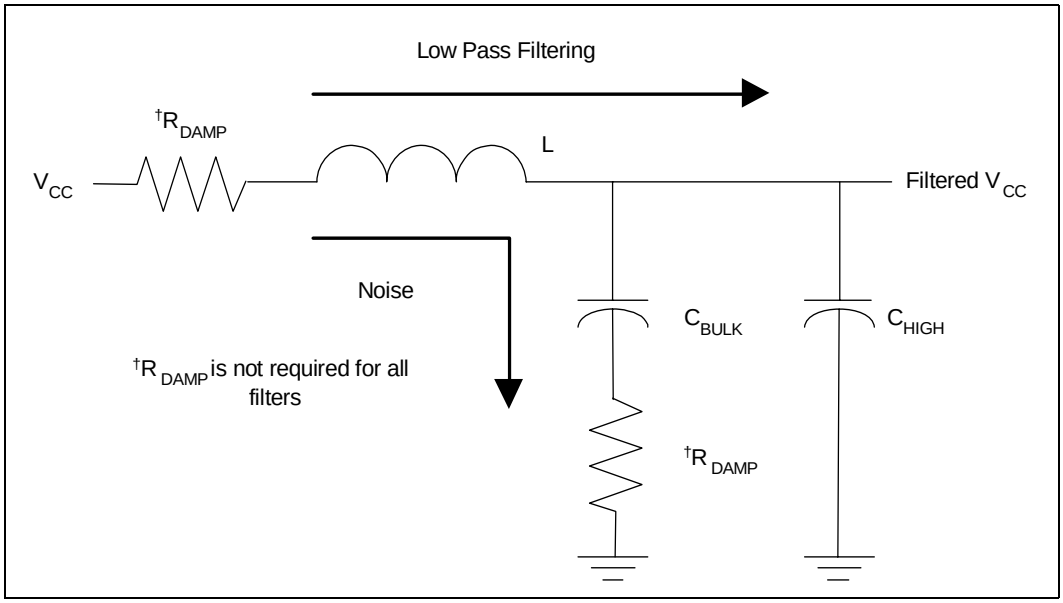


Table 25. Analog Supply Filter Requirements

Required Intel® 855GME Chipset Filters	Rdamp	Rdamp location	L	Cbulk	Chigh
VCCASM	None	N/A	1210 1.0 µH DCRmax 0.169 Ωs	100 µF	0603 0.1 µF X5R
VCCQSM	1 Ω	In series with Cbulk	0805 0.68 µH DCRmax 0.80 Ωs	1206 4.7 µF X5R	0603 0.1 µF X5R
VCCAHPLL	None	N/A	None		0603 0.1 µF X5R
VCCADPLLA	1 Ω	In series with inductor	0805 0.10 µH	220 µF	0603 0.1 µF X5R
VCCADPLLB	1 Ω	In series with inductor	0805 0.10 µH	220 µF	0603 0.1 µF X5R
VCCADAC	None	N/A	None	None	0603 0.1 µF X5R 0603 0.01 µF X5R
VCCAGPLL	None	N/A	None	None	0603 0.1 µF X5R
VCCALVDS	None	N/A	None	None	0603 0.1 µF X5R 0603 0.01 µF X5R

4.8.4 Intel® 6300ESB Power Delivery

Figure 63. Intel® 6300ESB Power Delivery Example

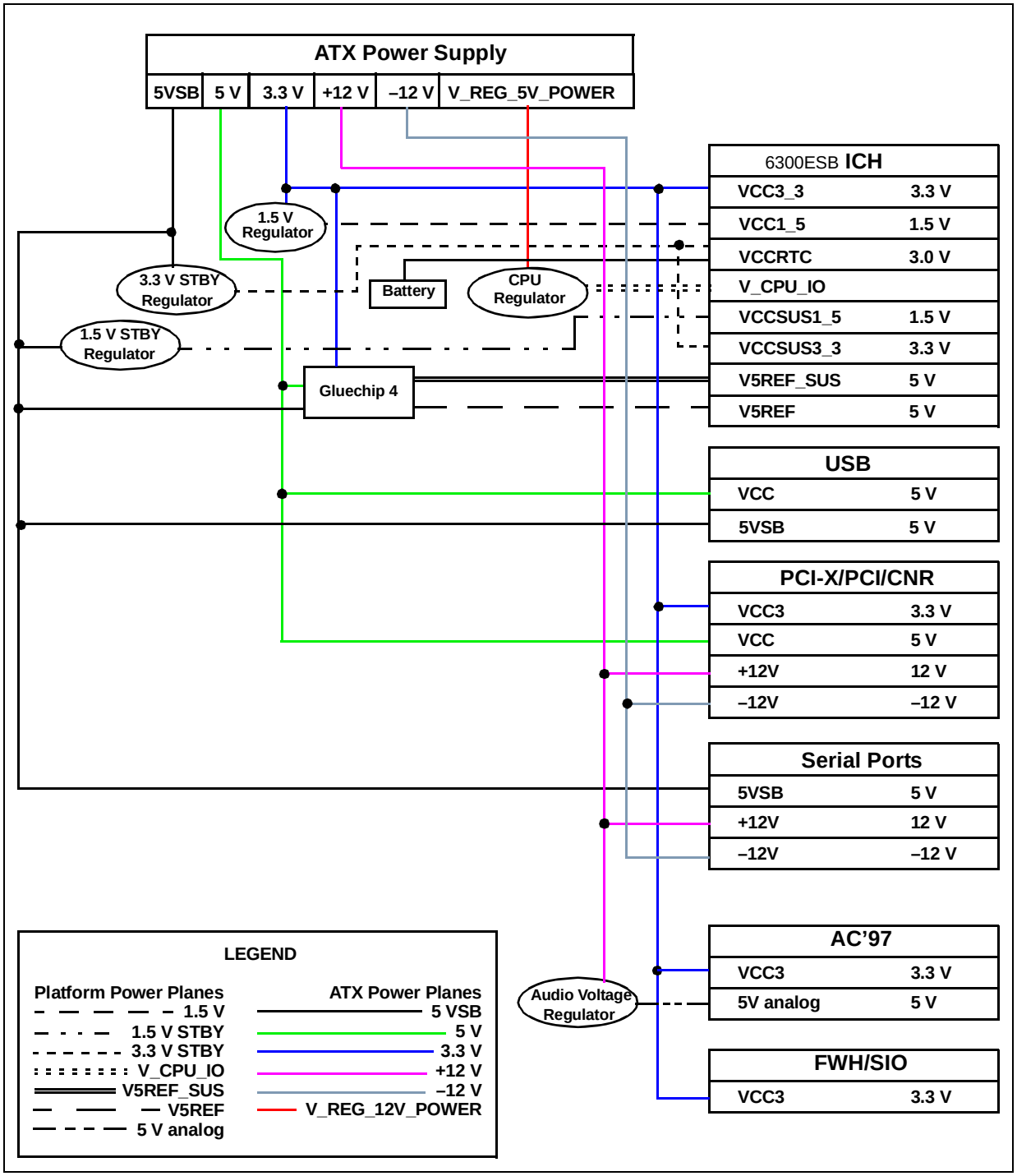


Figure 63 shows the suggested power delivery architecture for the 6300ESB chipset. This power delivery architecture supports the 'Instantly Available PC Design Guidelines' through the *suspend-to-RAM (STR)* state. During STR, only the necessary devices are powered. These devices include: main memory, the 6300ESB resume well, PCI-X and PCI wake devices (via 3.3 Vaux) and USB (USB may only be powered when sufficient standby power is available). In order to ensure that enough power is available during STR, a thorough power budget must be completed.

The power requirements must include each device's power requirements, both in *suspend* and in *full-power*. The power requirements must be compared against the power budget supplied by the power supply. Due to the requirements of main memory and PCI 3.3Vaux (and possibly other devices in the system), it is necessary to create a *dual* power rail.

The models given in this Design Guide are only examples. There are many power distribution methods that achieve the similar results. It is critical, when deviating from these examples in any way, to consider the effect of the change.

In addition to the power planes provided by the ATX power supply, a 6300ESB chipset-based system (using *Suspend-to-RAM*) requires seven power planes to be generated on the board.

1. 5 V: The 1.5 V plane powers the 6300ESB Hub Interface 1.5 I/O buffers, as well as other components. For 6300ESB preliminary power requirements on this rail, see Table 26. For decoupling considerations, see Section 4.8.9, "Intel® 6300ESB Decoupling Recommendations" on page 120.

Note: This regulator is required in ALL designs.

3.3 VSB: The 3.3 VSB plane powers the I/O buffers in the resume well of the 6300ESB and the PCI 3.3 Vaux suspend power pins. The 3.3 Vaux requirement states that during suspend, the system must deliver 375 mA to each wake-enabled card and 20 mA to each non wake-enabled card. During full-power operation, the system must be able to supply 375 mA to EACH card. Therefore, the total current requirement is:

Full-power Operation: 375 mA * number of PCI-X and PCI slots

Suspend Operation: 375+20 * (number of PCI-X and PCI slots – 1)

In addition to the PCI 3.3 Vaux, the 6300ESB suspend well power requirements must be considered as shown in Figure 63

Note: This regulator is required in ALL designs.

1.5VSB: A 1.5 V Standby regulator should be used to power the resume well of the 6300ESB.

4.8.5 Power Supply PS_ON Consideration

When a pulse on SLP_S3# or SLP_S5# is short enough (~ 10-100 ms) so that PS_ON is driven active during the exponential decay of the power rails, a few power supply designs may not be designed to handle this short pulse condition. In this case, the power supply does not respond to this event and does not power back up. These power supplies need to have their power cords disconnected, then reconnected to restore power to the system. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they may properly respond to PS_ON. This level varies with affected power supply.

The ATX spec does not specify a minimum pulse width on PS_ON de-assertion; power supplies must be able to handle any pulse width. This issue may affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

The platform designer must ensure that the power supply used with the platform is not affected by this issue.

4.8.6 Intel® 6300ESB Analog Power Delivery

Ensure the 5 V analog plane used by AC ‘97 Audio is provided through a proper audio voltage regulator (Figure 63).

4.8.7 Intel® 6300ESB Standby Power Distribution

To avoid radiated or conducted noise being coupling into the 6300ESB through the resume wells, the standby power rails (V5REF_Sus & VccSus3_3) should be implemented using planes rather than traces. The planes will have the capability to absorb the noise where a trace would serve as antennae

4.8.8 Intel® 6300ESB Power Consumption

Refer to the Intel® 6300ESB *I/O Controller Hub Datasheet* for power consumption information.

4.8.9 Intel® 6300ESB Decoupling Recommendations

The 6300ESB is capable of generating large current swings when switching between logic high and logic low. This condition may cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in Table 26 to ensure the component maintains stable supply voltages. Place the capacitors as close to the package as possible (100 mils nominal). Rotate caps that sit over power planes so that the loop inductance is minimized. The basic theory for minimizing loop inductance is to consider which voltage is on layer two (power or ground) and spin the decoupling cap with the opposite voltage towards the BGA (Ball Grid Array). This greatly minimizes the total loop inductance. It is recommended that for prototype board designs the designer include pads for extra power plane decoupling caps.

4.8.10 6300ESB Power Signal Decoupling

Table 26. Power Signal Decoupling

Pin	Capacitor	Quantity	Decoupling Placement
V_CPU_IO	0.1 µF	1	Close to the 6300ESB
V_{CC}RTC	0.1 µF	2	One close to the 6300ESB and one close to the battery
V_{CC}3.3	0.1 µF 0.01µF	12 4	Close to the 6300ESB
V_{CC}Sus3.3	0.1 µF 0.01 µF 1.0 µF	4 1 1	
V_{CC}1_5	0.1 µF 0.01 µF	6 2	
V_{CC}Sus1_5	0.1 µF	4	
V5REF_Sus	0.1 µF	1	
V5REF	0.1 µF	1	
V_{CC}PLL	0.1 µF	3	
V_{CC}HI	0.1 µF	2	
VCCREF (3.3 V)	1.0 µF	1	
VCCA	0.1 µF	1	

4.8.11 Hub Interface Decoupling

Refer to Section 8.1.6 for details.

4.8.12 FWH Decoupling

A 0.1 µF capacitor shall be placed between the VCC supply pins and the VSS ground pins to decouple high-frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the V_{CC} supply pins. Note that the value of the low-frequency bulk decoupling capacitor is dependent on board layout and system power supply design.

4.9 Thermal Design Power

Refer to the *Intel*® 855GME *Chipset Memory Controller Hub (MCH) Thermal Design Guide for Embedded Applications* and the I*ntel*® 6300ESB *I/O Controller Hub Thermal and Mechanical Design Guide* for information on thermal design.

System Memory Design Guidelines (DDR-SDRAM) 5

5.1 Introduction

The Intel® 855GME Chipset Double Data Rate (DDR) SDRAM system memory interface consists of SSTL-2 compatible signals. These SSTL-2 compatible signals have been divided into several signal groups: data, control, command, CPC, clock, and feedback signals. Table 27 summarizes the different signal grouping. Refer to the *Intel® 855GM/855GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet* for details on the signals listed.

Table 27. Intel® 855GME Chipset DDR Signal Groups

Group	Signal Name	Description
Clocks	SCK[5:0]	DDR-SDRAM differential clocks - (three per DIMM)
	SCK[5:0]#	DDR-SDRAM inverted differential clocks - (three per DIMM)
Data	SDQ[63:0]	Data bus
	SDQ[71:64]	Check bits for ECC function
	SDQS[8:0]	Data strobes
	SDM[8:0]	Data mask
Control	SCKE[3:0]	Clock enable - (one per Device Row)
	SCS[3:0]#	Chip select - (one per Device Row)
Command	SMA[12:6,3,0]	Memory address bus
	SBA [1:0]	Bank select
	SRAS#	Row address select
	SCAS#	Column address select
	SWE#	Write enable
CPC	SMA[5,4,2,1]	Command per clock (DIMM0)
	SMAB[5,4,2,1]	Command per clock (DIMM1)
Feedback	RCVENOUT#	Receive enable output (no external connection)
	RCVENIN#	Receive enable input (no external connection)

5.2 Length Matching and Length Formulas

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching formulas are also provided that further restrict the minimum to maximum length range of each signal group with respect to clock, within the overall boundaries, as required to ensure adequate timing margins. These secondary constraints are referred to as length matching constraints and the formulas used are referred to as length matching formulas.

All signal groups, except feedback signals, are length matched to the DDR clocks. The clocks on a given DIMM are matched to within ± 25 mils of the target length. A different clock target length may be used for each DIMM. The difference in clock target lengths between DIMM0 and DIMM1 shall not exceed 1 inch. A simple summary of the length matching formulas for each signal group is provided in Table 28.

Table 28. Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock –1.5”	Clock - 0.5”
Command to Clock	Clock – 1.5”	Clock + 1.0”
CPC to Clock	Clock – 1.5”	Clock - 0.5”
Strobe to Clock	Clock – 1.5”	Clock - 0.5”
Data to Strobe	Strobe – 25 mils	Strobe + 25 mils

NOTE: All length matching formulas are based on GMCH die-pad to DIMM pin total length.

Package length tables are provided for all signals to facilitate this pad-to-pin matching. Length formulas shall be applied to each DIMM slot separately. The full geometry and routing guidelines along with the exact length matching formulas and associated diagrams are provided in the individual signal group guidelines sections to follow.

An available DDR DIMM trace length calculator may be used to ensure layout trace lengths meet these recommendations. Contact the local Intel Field Representative for information on obtaining this tool.

5.3 Package Length Compensation

As mentioned above, all length matching is done for GMCH die-pad to DIMM pin. The reason for this is to compensate for the package length variation across each signal group in order. The Intel 855GME chipset Graphics Memory Controller Hub (82855GME) does not equalize package lengths internally as some previous GMCH components have; the 82855GME requires length matching or tuning process. The justification for this is based on the belief that length variance in the package based on ball position is naturally tuned out when the pin escape is completed to the edge of the package. Length matching in the package would then tend to create a mismatch at the package edge.

Package length compensation shall not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the

process of adjusting package length variation across a signal group. Of course, there is some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation where required.

5.4 Topologies and Routing Guidelines

The Intel 855GME chipset's Double Data Rate (DDR) SDRAM system memory interface implements the low swing, high-speed, terminated SSTL_2 topology. This section contains information related to the recommended interconnect topologies and routing guidelines for each of the signal groups that comprise the DDR interface. When implemented as defined, these guidelines provide a robust DDR solution on an Intel 855GME chipset-based design. The first group to be presented are the clocks, because most of the signal groups have length formulas that are based on clock length.

5.4.1 Clock Signals – SCK[5:0], SCK[5:0]#

The clock signal group includes the differential clock pairs SCK[5:0]/SCK[5:0]#. The GMCH generates and drives these differential clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. The GMCH only supports unbuffered DDR DIMMs, three differential clock pairs are routed to each DIMM connector. Table 29 summarizes the clock signal mapping.

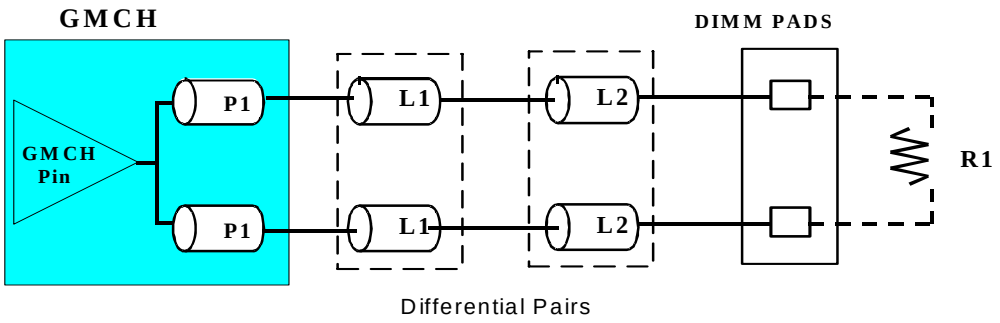
Table 29. Clock Signal Mapping

Signal	Relative To
SCK[2:0]/SCK[2:0]#	DIMM0
SCK[5:3]/SCK[5:3]#	DIMM1

5.4.2 Clock Topology Diagram

The 82855GME provides six differential clock output pairs, or three clock pairs per DIMM socket. The motherboard clock routing topology is shown in Figure 64. Refer to the routing guidelines in Section 5.4.3 for detailed length and spacing rules for each segment. The clock signals shall be routed as closely-coupled differential pairs over the entire length. Spacing to other DDR signals shall not be less than 20 mils. Isolation spacing to non-DDR signals shall be 25 mils.

Figure 64. DDR Clock Routing Topology (SCK[5:0]/SCK[5:0]#)



NOTE: R1 is located on the DIMM module.

5.4.3 DDR Clock Routing Guidelines

Table 30 presents the DDR clock signal group routing guidelines.

Table 30. DDR Clock Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Definition
Signal Group	SCK[5:0] and SCK[5:0]#
Topology	Differential Pair Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	42 Ω ± 15%
Differential Mode Impedance (Zdiff)	70 Ω ± 15%
Nominal Trace Width (See exceptions for breakout region below.)	Inner Layers: 7 mils Outer Layers: 8 mils (pin escapes only)
Nominal Pair Spacing (edge to edge) (See exceptions for breakout region below)	Inner Layers: 4 mils Outer Layers: 5 mils (pin escapes only)
Minimum Pair-to-Pair Spacing (See exceptions for breakout region below.)	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other DDR Signals (See exceptions for breakout region below.)	20 mils
Minimum Isolation Spacing to Non-DDR Signals	25 mils
Maximum Via Count	2 (per side)

NOTES:
1. Pad-to-pin length tuning is used on clocks to achieve minimal variance. Package lengths range between approximately 600 mils and 1400 mils. Exact package lengths for each clock signal are provided at the end of this section. Overall target length shall be established based on placement and routing flow. The resulting motherboard segment lengths must fall within the ranges specified.
2. The DDR clocks shall be routed on internal layers, except for pin escapes. It is recommended that pin escape vias be located directly adjacent to the ball pads on all clocks. Surface layer routing shall be minimized.
3. Exceptions to the trace width and spacing geometries are allowed in the breakout region to fan-out the interconnect pattern. Reduced spacing shall be avoided as much as possible.

Table 30. DDR Clock Signal Group Routing Guidelines (Sheet 2 of 2)

Parameter	Definition
Package Length Range – P1	1000 mils ± 350 mils Refer to clock package length for exact lengths.
Trace Length Limits – L1	Max = 300 mils (breakout segment)
Length Limits – P1 + L1 + L2	Min = 3.5” Max = 6.5”
Total Length – P1 + L1 + L2	Total length target is determined by placement Total length for DIMM0 group = X0 Total length for DIMM1 group = X1
SCK to SCK# Length Matching	Match total length to ±10 mils
Clock to Clock Length Matching (Total Length)	Match all DIMM0 clocks to X0 ± 25 mils Match all DIMM1 clocks to X1 ± 25 mils
Breakout Exceptions (Reduced geometries for MCH breakout region)	Inner Layers: 4 mil trace, 4 mil pair space allowed Outer Layers: 5 mil trace, 5 mil pair space allowed Pair-to-pair spacing of 5 mils allowed Spacing to other DDR signals of 5 mils allowed Maximum breakout length is 0.3”

NOTES:
1. Pad-to-pin length tuning is used on clocks to achieve minimal variance. Package lengths range between approximately 600 mils and 1400 mils. Exact package lengths for each clock signal are provided at the end of this section. Overall target length shall be established based on placement and routing flow. The resulting motherboard segment lengths must fall within the ranges specified.
2. The DDR clocks shall be routed on internal layers, except for pin escapes. It is recommended that pin escape vias be located directly adjacent to the ball pads on all clocks. Surface layer routing shall be minimized.
3. Exceptions to the trace width and spacing geometries are allowed in the breakout region to fan-out the interconnect pattern. Reduced spacing shall be avoided as much as possible.

5.4.3.1 Clock Length Matching Requirements

The 82855GME provides three differential clock pairs for each DIMM. A differential clock pair is made up of a SCK signal and its complement signal SCK#. Refer to Section 5.2 for more details on length matching requirements.

The differential pairs for one DIMM are:

SCK[0]/SCK[0]#
SCK[1]/SCK[1]#
SCK[2]/SCK[2]#

The differential pairs for the second DIMM are:

SCK[3]/SCK[3]#
SCK[4]/SCK[4]#
SCK[5]/SCK[5]#

The two sets of differential clocks must be length tuned on the motherboard such that any pair to pair package length variation is tuned out. The three pairs associated with DIMM0 are tuned to a fixed overall length, including package, and the three pairs associated with DIMM1 are tuned to a fixed overall length.

The two traces associated with each clock pair are length matched within the package, however some additional compensation may be required on the motherboard in order to achieve the ±10-mil length tolerance within the pair.

Between clock pairs the package length varies substantially. The motherboard length of each clock pair must be length adjusted to tune out package variance. The total length including package shall be matched to within ± 25 mils of each other. This may result in a clock length variance of as much as 700 mils on the motherboard.

The clock lengths to DIMM1 may be up to 1.0 inch longer than the clock lengths to DIMM0.

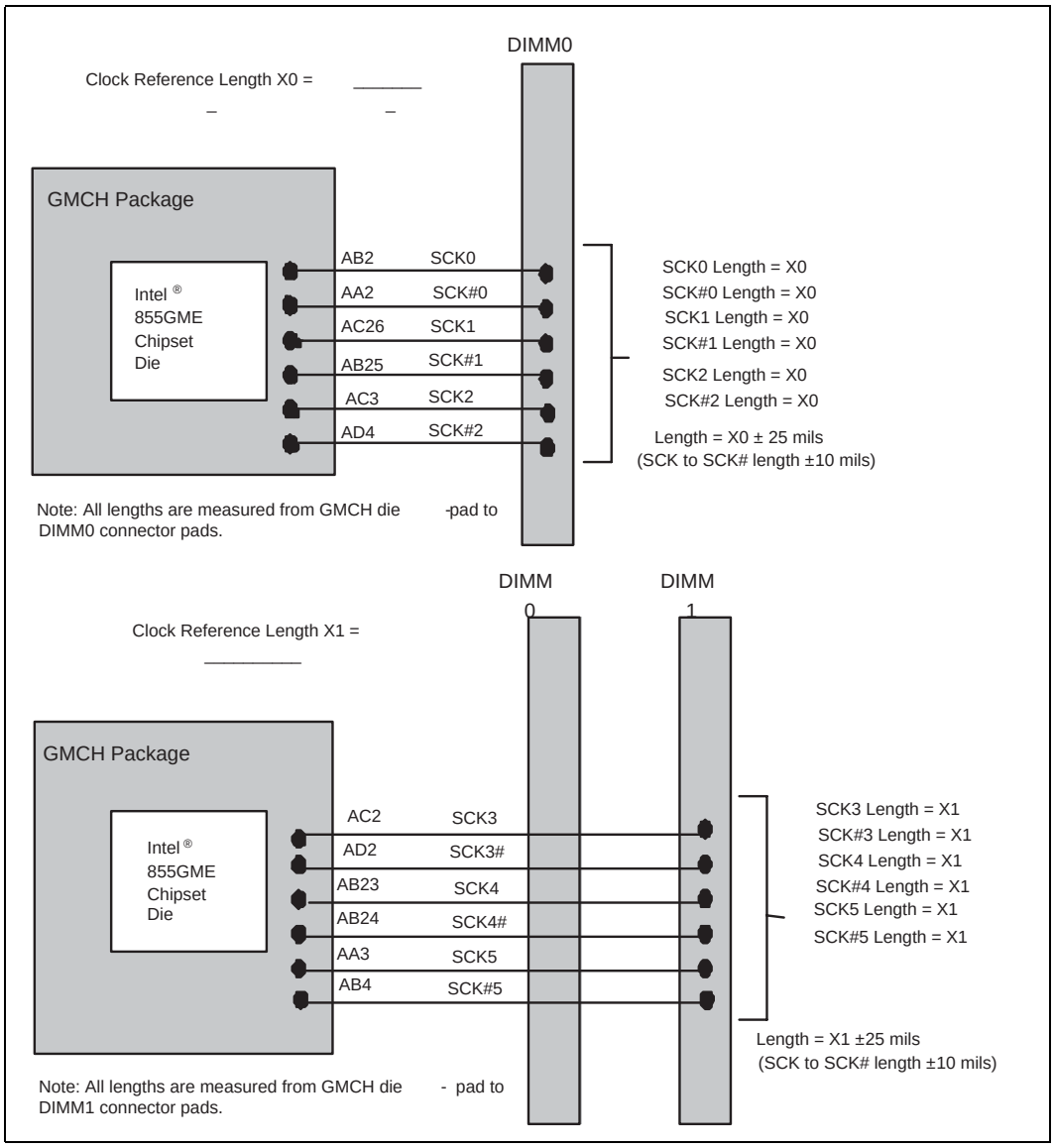
The first step in determining the routing lengths for clocks and all other clock-relative signal groups is to establish the target length for each DIMM clock group. These target lengths are shown as X0 and X1 in Figure 65.These are the lengths to which all clocks within the corresponding group are matched and the reference length values used to calculate the length ranges for the other signal groups.

5.4.3.2 Clock Reference Lengths

The clock reference length for each DIMM clock group is calculated by first determining the longest total clock length required to complete the clock routing. A table of clock package lengths is provided in Table 31 to assist with this calculation. After the longest total length is determined for each clock group, this figure becomes a lower bound for the associated clock reference length. At this point it is helpful to have completed a test route of the SDQ/SDQS bus such that final clock reference lengths may be defined with consideration of the impact on SDQ/SDQS bus routability. Some iteration may be required.

After the reference lengths X0 and X1 are defined then it remains to tune each clock pair's motherboard trace segment lengths as required such that the overall length of each clock equals the associated clock reference length plus or minus the 25 mil tolerance. Again, the reference length for the two sets of clocks shall be offset by the nominal routing length between DIMM connectors.

Figure 65. DDR Clock Trace Length Matching Diagram



5.4.3.3 Clock Length Package Table

Use the package length data in Table 31 to tune the motherboard length of each SCK/SCK# clock pair between the GMCH and the associated DIMM socket. Intel recommends that die-pad to DIMM pin length be tuned to within ± 25 mils in order to optimize timing margins on the interface.

Table 31. DDR Clock Package Lengths

Signal	Pin Number	Package Length (mils)
SCK[0]	AB2	1177
SCK[0]#	AA2	1169
SCK[1]	AC26	840
SCK[1]#	AB25	838
SCK[2]	AC3	1129
SCK[2]#	AD4	1107
SCK[3]	AC2	1299
SCK[3]#	AD2	1305
SCK[4]	AB23	643
SCK[4]#	AB24	656
SCK[5]	AA3	1128
SCK[5]#	AB4	1146

Package length compensation may be performed on each individual clock output thereby matching total length on SCK/SCK# exactly, or alternatively the average package length may be used for both outputs of a pair and length tuning done with respect to the motherboard portion only. See Section 5.5.2 for more information on DRAM clock flexibility.

5.4.4 Data Signals – SDQ[71:0], SDM[8:0], SDQS[8:0]

The GMCH data signals are source synchronous signals that include a 72-bit wide data bus, a set of eight data mask bits, and a set of eight data strobe signals. There is an associated data strobe and data mask bit for each of the eight data byte groups, making for a total of eight 10-bit byte lanes. This section summarizes the SDQ/SDM to SDQS routing guidelines and length matching recommendations.

- The data signals include SDQ[71:0], SDM[8:0], and SDQS[8:0].
- The data signals shall transition from an external layer to an internal signal layer under the GMCH. Keep to the same internal layer until transitioning back to an external layer at the series resistor.
- After the series resistor, the signal shall transition from the external layer to the same internal layer and route to DIMM0.
- At DIMM0, the signal shall transition to an external layer and connect to the appropriate pad of the connector.
- After the DIMM0 transition, continue to route the signal on the same internal layer to DIMM1.
- Transition back out to an external layer and connect to the appropriate pad of DIMM1.
- Connection to the termination resistor shall be through the same internal layer with a transition back to the external layer near the resistor. External trace lengths shall be minimized.

To facilitate routing, swapping of the byte lanes is allowed for SDQ[63:0]. Bit swapping within the byte lane is also allowed for SDQ[63:0] only. The checkbits SDQ[71:64] cannot be byte lane swapped with another SDQ byte lane. Bit swapping within the SDQ[71:64] byte lane is not allowed. It is suggested that the parallel termination be placed on both sides of DIMM1 to simplify routing and minimize trace lengths. All internal and external signals shall be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series (Rs) and parallel (Rt) data and strobe termination resistors, but data and strobe signals cannot be placed within the same R pack as the command or control signals. The tables and diagrams below depict the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Intel recommends that the full data bus SDQ[63:0], mask bus SDM[7:0], and strobe signals SDQS[7:0] be routed on the same internal signal layer. It is required that the SDQ byte group and the associated SDM and SDQS signals within a byte lane be routed on the same internal layer.

The total length of SDQ, SDM, and SDQS traces between the GMCH and the DIMMs must be within the range defined in the overall guidelines, and is also constrained by a length range boundary based on SCK/SCK# clock length, and an SDQ/SDM to SDQS length matching requirement within each byte lane.

Note: All length matching must be done inclusive of package length. SDQ, SDM, and SDQS package lengths are provided in Table 34 to facilitate this process.

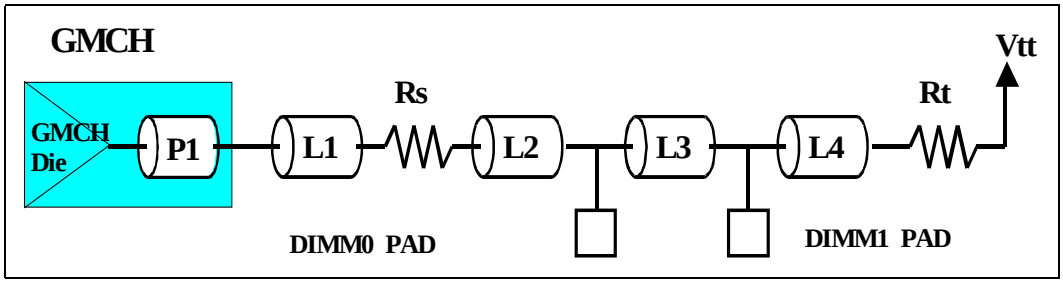
There are two levels of matching implemented on the data bus signals. The first is the length range constraint on the SDQS signals based on clock reference length. The second is SDQ/SDM to SDQS length matching within a byte lane. The length of the SDQS signal for each byte lane must fall within a range determined by the clock reference length, as defined in the SDQS to SCK/SCK# length matching section. The actual length of SDQS for each byte lane may fall anywhere within this range based on placement and routing flow.

After the SDQS length for a byte lane is established, the SDQ, SDM, and SDQS signals within the byte lane must be length matched to each other, inclusive of package length, as described in the SDQ to SDQS length matching section.

5.4.4.1 Data Bus Topology

Figure 66 depicts the data signal routing topology.

Figure 66. Data Signal Routing Topology



The data signals shall be routed using a 2:1 trace spacing to trace width ratio for signals within the DDR group, except for clocks and strobes. Data signals shall be routed on inner layers with minimized external trace lengths.

Table 32 presents the data signal group routing guidelines.

Table 32. Data Signal Group Routing Guidelines

Parameter	Definition
Signal Group	SDQ[71:0], SDQS[8:0], SDM[8:0]
Motherboard Topology	Daisy Chain with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	SDQ/SDM: 2:1 (e.g., 8 mil space to 4 mil trace) SDQS: 3 to 1 (e.g., 12 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	700 mils ± 300 mils Refer to package length for details.
Trace Length P1+ L1 – GMCH Die-Pad to Series Termination Resistor Pad	Min = 2”-L2 Max = 6”-L3-L2
Trace Length L2 – Series Termination Resistor Pad to First DIMM Pad	Max = 0.75”
Total Length P1+ L1+L2 – Total Length from GMCH to First DIMM Pad	Min = 2.0” Max = 6”-L3
Trace Length L3 – First DIMM Pad to Last DIMM Pad	Min = 0.25” Max = 2.0”
Trace Length L4 – Last DIMM Pad to Parallel Termination Resistor Pad	Max = 1.0”
Total Length P1+ L1+L2+L3 – Total Length from GMCH to Second DIMM Pad	Min = 2”+L3 Max = 6.0”
Series Termination Resistor (Rs)	10 Ω ± 5%
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	6
Length Matching Requirements	Match SDQS to SCK/SCK# Refer to length matching Section 5.4.4.2 and Figure 67. SDQ/SDM to SDQS, to ± 25 mils, within each byte lane. Refer to length matching Section 5.4.4.3 and Figure 68.

NOTES:
1. Power distribution vias from Rt to Vtt are not included in this count.
2. The overall minimum and maximum length to the DIMM must comply with clock length matching requirements.

5.4.4.2 SDQS to Clock Length Matching Requirements

The first step in length matching is to determine the SDQS length range based on the SCK/SCK# reference length defined previously. The total length of the SDQS strobe signals, including package length, between the GMCH die-pad and the DIMMs must fall within the range defined in the formulas below. Refer to the clock section for the definition of the clock reference length. Refer to Table 32 for the definition of the various trace segments.

Length range formula for DIMM0:

X_0 = SCK[2:0]/SCK[2:0]# total reference length, including package length. Refer to Section 5.4.1 for more information.

Y_0 = SDQS[7:0] total length = GMCH package + L1 + L2, as shown in Figure 66, where:

$(X_0 – 1.5”) \leq Y_0 \leq (X_0 - 0.5”)$

Length range formula for DIMM1:

X_1 = SCK[5:3]/SCK[5:3]# total reference length, including package length. Refer to Section 5.4.1 for more information.

Y_1 = SDQS[7:0] total length = GMCH package + L1 + L2 + L3, as shown in Figure 66 where:

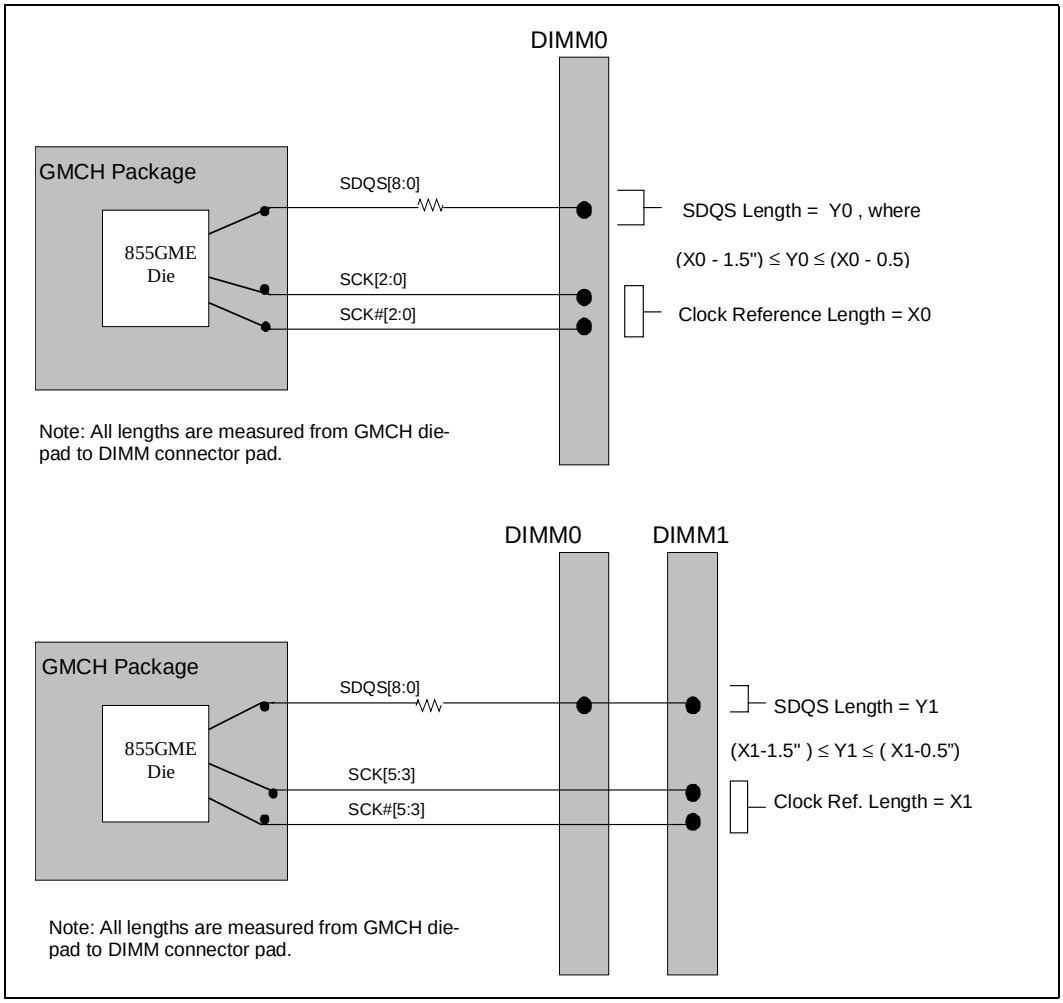
$(X_1 – 1.5”) \leq Y_1 \leq (X_1 - 0.5”)$

Length matching is only performed from the GMCH to the DIMMs, and does not involve the length of L4, which may vary over its entire range. Intel recommends that routing segment length L3 between DIMM0 to DIMM1 be held fairly constant and equal to the offset between clock reference lengths X0 and X1. This produces the most straightforward length-matching scenario.

Note: A nominal SDQS package length of 700 mils may be used to estimate byte lane lengths prior to performing package length compensation.

Figure 67 depicts the SDQS to clock trace length matching diagram.

Figure 67. SDQS to Clock Trace Length Matching Diagram



5.4.4.3 Data to Strobe Length Matching Requirements

The data bit signals SDQ[71:0] are grouped by byte lanes and associated with a data mask signal, SDM[8:0], and a data strobe, SDQS[8:0]. The data and mask signals must be length matched to their associated strobe within ± 25 mils, including package.

For DIMM0 this length matching includes the motherboard trace length to the pads of the DIMM0 connector (L1 + L2) plus package length.

For DIMM1, the motherboard trace length to the pads of the DIMM1connector (L1 + L2 + L3) plus package length.

Length range formula for SDQ and SDM:

X = SDQS total length, including package length, as defined previously

Y = SDQ, SDM total length, including package length, within same byte lane, where

(X – 25 mils) ≤ Y ≤ (X + 25 mils)

Length matching is not required from the DIMM1 to the parallel termination resistors. Figure 68 presents the length matching requirements between the SDQ, SDM, and SDQS signals within a byte lane. Byte lane mapping is defined in Table 33.

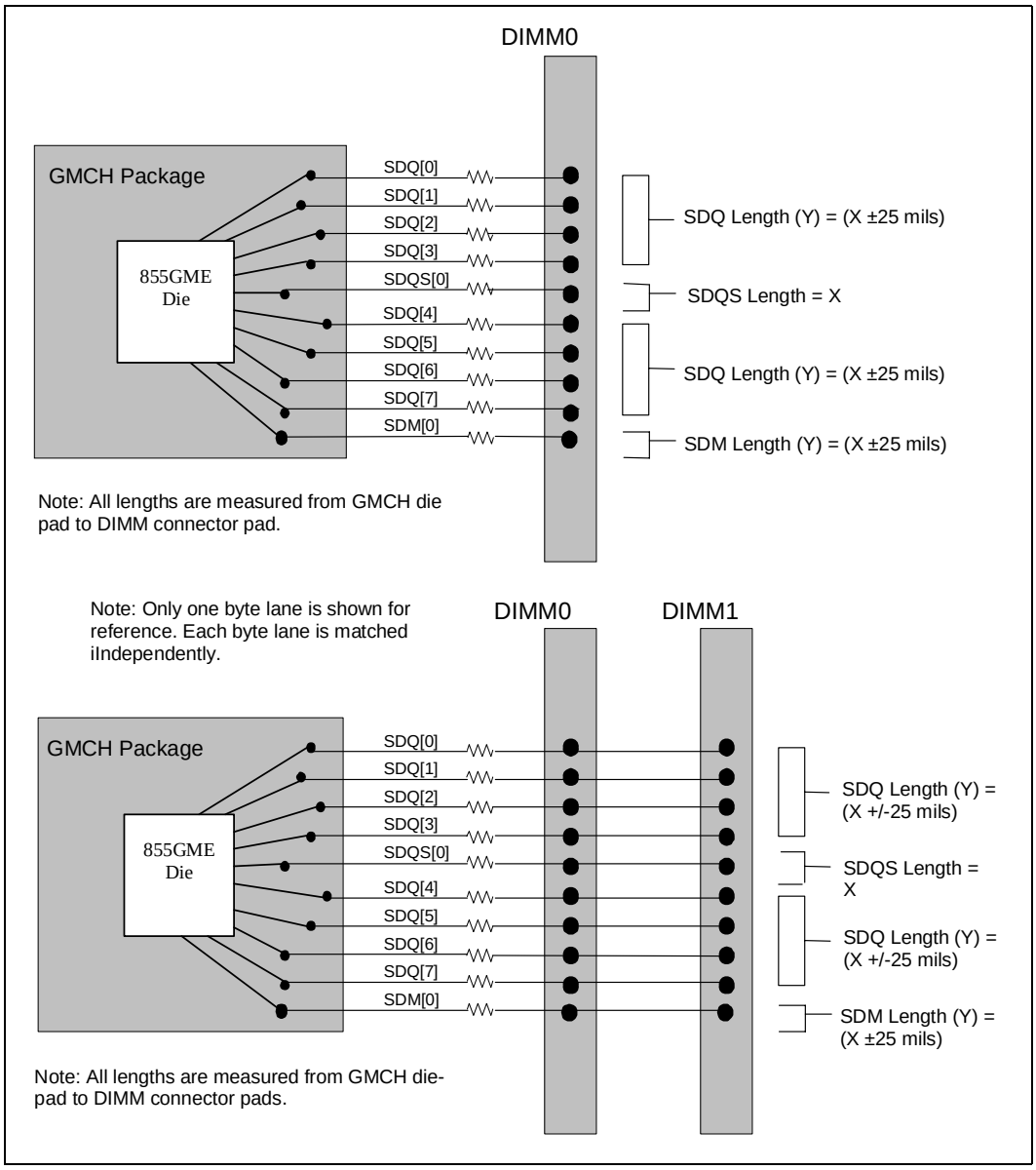
5.4.4.4 SDQ to SDQS Mapping

Table 33 defines the mapping between the nine byte lanes, nine mask bits, and the nine SDQS signals, as required to do the required length matching.

Table 33. SDQ/SDM to SDQS Mapping

Signal	Mask	Relative To
SDQ[7:0]	SDM[0]	SDQS[0]
SDQ[15:8]	SDM[1]	SDQS[1]
SDQ[23:16]	SDM[2]	SDQS[2]
SDQ[31:24]	SDM[3]	SDQS[3]
SDQ[39:32]	SDM[4]	SDQS[4]
SDQ[47:40]	SDM[5]	SDQS[5]
SDQ[55:48]	SDM[6]	SDQS[6]
SDQ[63:56]	SDM[7]	SDQS[7]
SDQ[71:64]	SDM[8]	SDQS[8]

Figure 68. SDQ/SDM to SDQS Trace Length Matching Diagram



5.4.4.5 SDQ/SDQS Signal Package Lengths

The package length data in Table 34 shall be used to tune the length of each SDQ, SDM, and SDQS motherboard trace as required to achieve the overall length matching requirements defined in the prior sections.

Table 34. DDR SDQ/SDM/SDQS Package Lengths (Sheet 1 of 2)

Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)
SDQ[0]	AF2	785	SDQ[32]	AH16	766
SDQ[1]	AE3	751	SDQ[33]	AG17	558
SDQ[2]	AF4	690	SDQ[34]	AF19	510
SDQ[3]	AH2	903	SDQ[35]	AE20	579
SDQ[4]	AD3	682	SDQ[36]	AD18	408
SDQ[5]	AE2	739	SDQ[37]	AE18	458
SDQ[6]	AG4	741	SDQ[38]	AH18	658
SDQ[7]	AH3	845	SDQ[39]	AG19	596
SDQ[8]	AD6	607	SDQ[40]	AH20	677
SDQ[9]	AG5	756	SDQ[41]	AG20	730
SDQ[10]	AG7	685	SDQ[42]	AF22	562
SDQ[11]	AE8	558	SDQ[43]	AH22	702
SDQ[12]	AF5	734	SDQ[44]	AF20	563
SDQ[13]	AH4	825	SDQ[45]	AH19	644
SDQ[14]	AF7	644	SDQ[46]	AH21	716
SDQ[15]	AH6	912	SDQ[47]	AG22	783
SDQ[16]	AF8	622	SDQ[48]	AE23	592
SDQ[17]	AG8	624	SDQ[49]	AH23	752
SDQ[18]	AH9	676	SDQ[50]	AE24	666
SDQ[19]	AG10	634	SDQ[51]	AH25	817
SDQ[20]	AH7	710	SDQ[52]	AG23	639
SDQ[21]	AD9	508	SDQ[53]	AF23	667
SDQ[22]	AF10	569	SDQ[54]	AF25	707
SDQ[23]	AE11	469	SDQ[55]	AG25	783
SDQ[24]	AH10	648	SDQ[56]	AH26	834
SDQ[25]	AH11	622	SDQ[57]	AE26	701
SDQ[26]	AG13	572	SDQ[58]	AG28	808
SDQ[27]	AF14	655	SDQ[59]	AF28	756
SDQ[28]	AG11	599	SDQ[60]	AG26	782
SDQ[29]	AD12	460	SDQ[61]	AF26	748
SDQ[30]	AF13	536	SDQ[62]	AE27	673
SDQ[31]	AH13	642	SDQ[63]	AD27	608
			SDQ[64]	AG14	566
			SDQ[65]	AE14	477
			SDQ[66]	AE17	571

Table 34. DDR SDQ/SDM/SDQS Package Lengths (Sheet 2 of 2)

Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)
			SDQ[67]	AG16	530
			SDQ[68]	AH14	701
			SDQ[69]	AE15	421
			SDQ[70]	AF16	491
			SDQ[71]	AF17	530
SDQS[0]	AG2	925	SDM[0]	AE5	838
SDQS[1]	AH5	838	SDM[1]	AE6	693
SDQS[2]	AH8	756	SDM[2]	AE9	538
SDQS[3]	AE12	466	SDM[3]	AH12	606
SDQS[4]	AH17	678	SDM[4]	AD19	492
SDQS[5]	AE21	487	SDM[5]	AD21	470
SDQS[6]	AH24	770	SDM[6]	AD24	557
SDQS[7]	AH27	858	SDM[7]	AH28	917
SDQS[8]	AD15	418	SDM[8]	AH15	685

5.4.5 Control Signals – SCKE[3:0], SCS[3:0]#

The 82855GME control signals, SCKE[3:0] and SCS[3:0]#, are clocked into the DDR SDRAM devices using clock signals SCK[5:0]/SCK[5:0]#. The GMCH drives the control and clock signals together, with the clocks crossing in the valid control window. The GMCH provides one chip select (CS) and one clock enable (CKE) signal per DIMM physical device row. Two chip select and two clock enable signals are routed to each DIMM. Refer to Table 35 for the CKE and CS# signal to DIMM mapping.

Table 35. Control Signal to DIMM Mapping

Signal	Relative To	DIMM Pin
SCS[0]#	DIMM0	AD23
SCS[1]#	DIMM0	AD26
SCS[2]#	DIMM1	AC22
SCS[3]#	DIMM1	AC25
SCKE[0]	DIMM0	AC7
SCKE[1]	DIMM0	AB7
SCKE[2]	DIMM1	AC9
SCKE[3]	DIMM1	AC10

The control signal routing shall transition from an external layer to an internal signal layer under the GMCH, keep to the same internal layer until transitioning back out to an external layer to connect to the appropriate pad of the DIMM connector and the parallel termination resistor. When the layout requires additional routing before the termination resistor, return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.

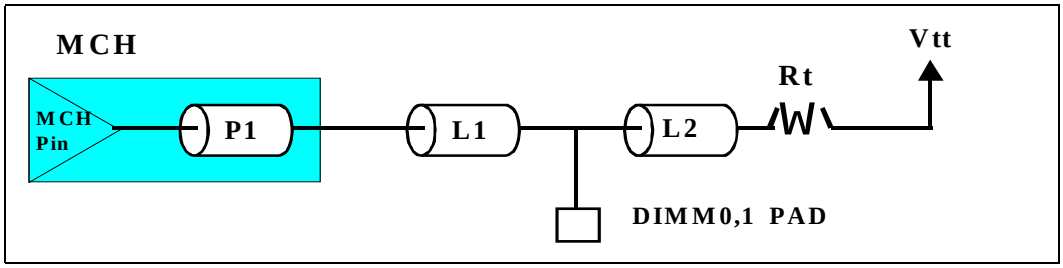
External trace lengths shall be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals shall be ground reference to keep the path of return current continuous. Intel suggests that all control signals be routed on the same internal layer.

Resistor packs are acceptable for the parallel (Rt) control termination resistors, but control signals cannot be placed within the same R pack as the data or command signals. The table and diagrams below depict the recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

5.4.5.1 Control Signal Routing Topology

Figure 69 depicts the control signal routing topology.

Figure 69. Control Signal Routing Topology



The control signals shall be routed using 2:1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. Control signals shall be routed on inner layers with minimized external trace lengths.

5.4.5.2 Control Signal Routing Guidelines

Table 36 defines the control signal routing guidelines.

Table 36. Control Signal Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SCKE[3:0], SCS[3:0]#
Motherboard Topology	Point-to-Point with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2:1 (e.g., 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils ± 250 mils Refer to package length for exact lengths.
Trace Length P1 + L1 – GMCH Die-Pad to DIMM Pad	Min = 2.0 inches Max = 6.0 inches
Trace Length L2 – DIMM Pad to Parallel Termination Resistor Pad	Max = 2.0 inches
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	3
Length Matching Requirements	Match CTRL to SCK[5:0]/SCK[5:0]# Refer to length matching in Section 5.4.5.3 and Figure 70.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. It is possible to route using two vias if one via is shared that connects to the DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the DIMM must comply with clock length matching requirements.

5.4.5.3 Control to Clock Length Matching Requirements

The length of the control signals, between the GMCH die-pad and the DIMM must fall within the range defined below, with respect to the associated clock reference length. Refer to Figure 69 for a definition of the various trace segments that make up this path. The length of trace from the DIMM to the termination resistor need not be length matched. The length matching requirements are also shown in Figure 70. Length range formula for DIMM0:

X_0 = SCK[2:0]/SCK[2:0]# total reference length, including package length. Refer to Section 5.4.3.1 for more information.

Y_0 = SCS[1:0]# and SCKE[1:0] total length = GMCH package length + L1, as shown in Figure 69, where:

$(X_0 – 1.5”) \leq Y_0 \leq (X_0 - 0.5”)$

Length range formula for DIMM1:

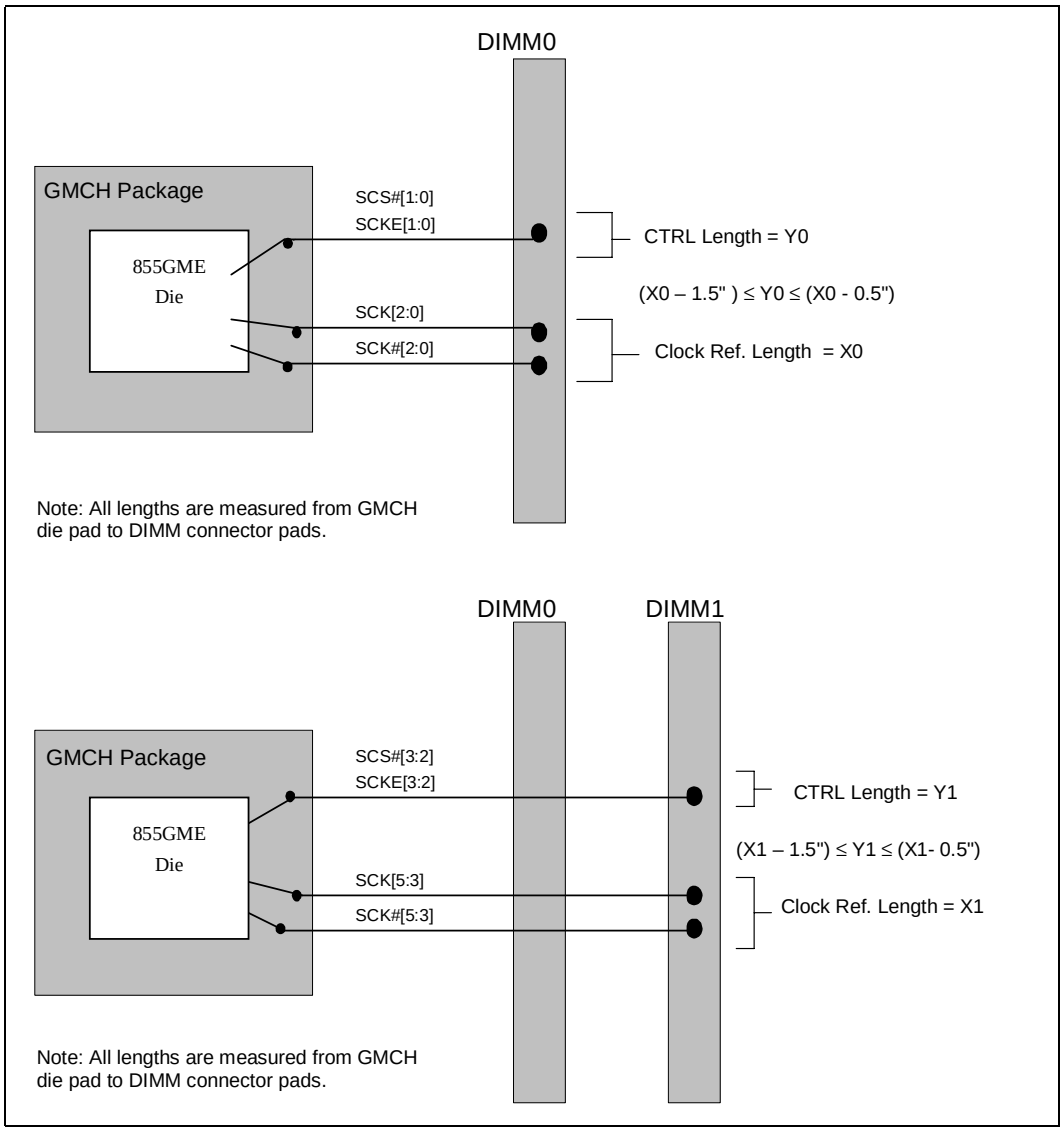
X_1 = SCK[5:3]/SCK[5:3]# total reference length, including package length. Refer to Section 5.4.3.1 for more information.

Y_1 = SCS[3:2]# and SCKE[3:2] total length = GMCH package length + L1, as shown in Figure 69, where:

$(X_1 – 1.5”) \leq Y_1 \leq (X_1 - 0.5”)$

No length matching is required from the DIMM to the termination resistor. Figure 70 depicts the length matching requirements between the control signals and clock. A nominal CS/CKE package length of 500 mils may be used to estimate baseline Mbyte lengths.

Figure 70. Control Signal to Clock Trace Length Matching Diagram



5.4.5.4 Control Group Package Length Table

The package length data in the Table 37 shall be used to match the overall length of each command signal to its associated clock reference length.

Note: Due to the relatively small variance in package length and adequate timing margins it is acceptable to use a fixed 500 mil nominal package length for all control signals, thereby reducing the complexity of the motherboard length calculations.

Table 37. Control Group Package Lengths

Signal	Pin Number	Package Length (mils)
SCS[0]#	AD23	502
SCS[1]#	AD26	659
SCS[2]#	AC22	544
SCS[3]#	AC25	612
SCKE[0]	AC7	443
SCKE[1]	AB7	389
SCKE[2]	AC9	386
SCKE[3]	AC10	376

5.4.6 Command Signals – SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#

The 82855GME command signals, SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, and SWE#, are clocked into the DDR SDRAMs using the clock signals SCK[5:0]/SCK[5:0]#. The GMCH drives the command and clock signals together, with the clocks crossing in the valid command window. The command signal group is supported by a daisy-chain topology.

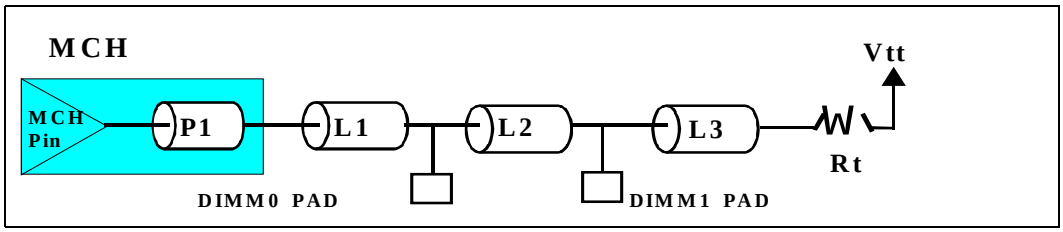
5.4.6.1 Command Signal Routing Topology

The command signal routing shall transition from an external layer to an internal signal layer under the GMCH. Keep the same internal layer until transitioning to an external layer immediately prior to connecting the DIMM0 connector pad. At the via transition for DIMM0, continue the signal route on the same internal layer until transitioning back out to an external layer to connect to the pad of DIMM1. After DIMM1, transition to the same internal layer or stay on the external layer and route the signal to Rt.

Intel suggests that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals shall be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the parallel command termination resistors but command signals cannot be placed within the same R-packs as data, strobe, or control signals. Figure 71 and Table 38 present the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to DIMM0 and DIMM1.

Figure 71. Command Routing for Topology



The command signals shall be routed using a 2:1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. Command signals shall be routed on inner layers with minimized external traces.

5.4.6.2 Command Topology Routing Guidelines

Table 38 presents the command topology routing guidelines.

Table 38. Command Topology Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines
Signal Group	SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#
Motherboard Topology	Daisy-Chain with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2:1 (e.g., 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils ± 250 mils Refer to Table 39 for exact package lengths.
Trace Length P1+ L1	Min = 2.0 inches Max = 5.5 inches
Trace Length P1+ L1+L2+L3	Max = 7.5 inches
Trace Length L2 – Total DIMM to DIMM spacing	Max = 2.0 inches
Trace Length L3 – Second DIMM Pad to Parallel Resistor Pad	Max = 1.5 inches

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the DIMM must comply with clock length matching requirements.
4. It is possible to route using three vias if one via is shared that connects to the DIMM1 pad and parallel termination resistor.

Table 38. Command Topology Routing Guidelines (Sheet 2 of 2)

Parameter	Routing Guidelines
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	6
Length Matching Requirements	CMD to SCK/SCK# Refer to length matching Section 5.4.6.3 and Figure 72 for details.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the DIMM must comply with clock length matching requirements.
4. It is possible to route using three vias if one via is shared that connects to the DIMM1 pad and parallel termination resistor.

5.4.6.3 Command Topology Length Matching Requirements

The routing length of the command signals, between the GMCH die-pad and the DIMM must be within the range defined below, with respect to the associated clock reference length. Refer to Figure 71 for a definition of the various motherboard trace segments. The length of trace from the DIMM to the termination resistor need not be length matched.

Length range formula for DIMM0:

X_0 = SCK[2:0]/SCK[2:0]# total reference length, including package length. Refer to Section 5.4.3.1 for more information.

Y_0 = CMD signal total length = GMCH package + L1, as shown in Figure 71, where:

$(X_0 – 1.5”) \leq Y_0 \leq (X_0 + 1.0”)$

Length range formula for DIMM1:

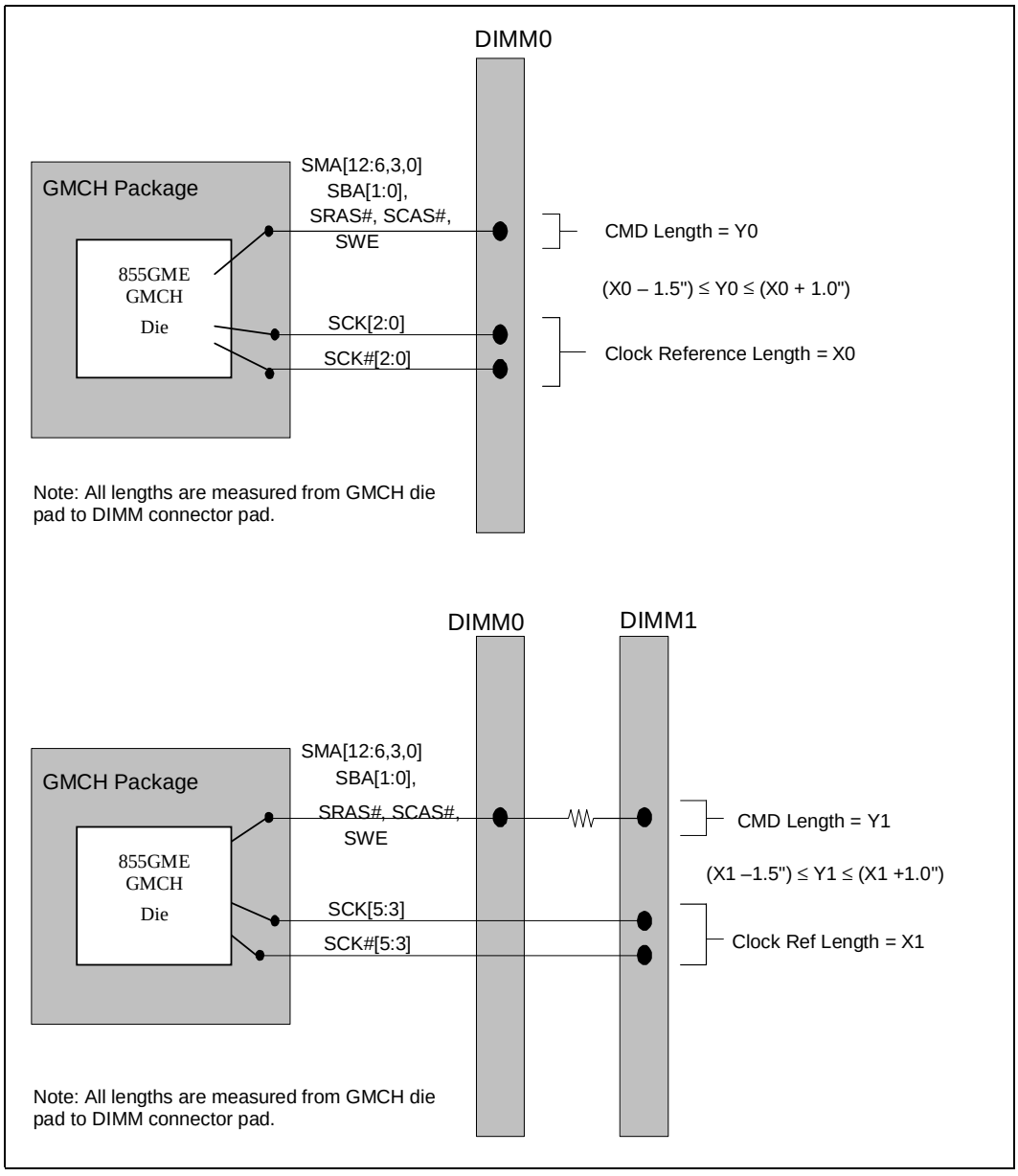
X_1 = SCK[5:3]/SCK[5:3]# total reference length, including package length. Refer to Section 5.4.3.1 for more information.

Y_1 = CMD signal total length = GMCH package + L1 + L2 + L3, as shown in Figure 71, where:

$(X_1 – 1.5”) \leq Y_1 \leq (X_1 + 1.0”)$

No length matching is required from DIMM1 to the termination resistor. Figure 72 depicts the length matching requirements between the command signals and clock. A nominal CMD package length of 500 mils may be used to estimate baseline Mbyte lengths. Refer to Section 5.3 for more details on package length compensation.

Figure 72. Topology Command Signal to Clock Trace Length Matching Diagram



5.4.6.4 Command Group Package Length Table

The package length data in Table 39 shall be used to match the overall length of each command signal to its associated clock reference length.

Table 39. Command Group Package Lengths

Signal	Pin Number	Pkg Length (mils)
SMA[0]	AC18	420
SMA[3]	AD17	472
SMA[6]	AD8	591
SMA[7]	AD7	596
SMA[8]	AC6	630
SMA[9]	AC5	681
SMA[10]	AC19	377
SMA[11]	AD5	683
SMA[12]	AB5	609
SBA[0]	AD22	592
SBA[1]	AD20	435
SCAS#	AC24	562
SRAS#	AC21	499
SWE#	AD25	751

5.4.7 CPC Signals – SMA[5,4,2,1], SMAB[5,4,2,1]

The 82855GME control signals, SMA[5,4,2,1] and SMAB[5,4,2,1], are common clocked signals. They are “clocked” into the DDR SDRAM devices using clock signals SCK[5:0]/SCK[5:0]#. The GMCH drives the CPC and clock signals together, with the clocks crossing in the valid control window. The GMCH provides one set of CPC signals per DIMM slot. Refer to Table 40 for the SMA and SMAB signal to DIMM mapping.

Table 40. Control Signal to DIMM Mapping

Signal	Relative To	DIMM Pin
SMA[1]	DIMM0	AD14
SMA[2]	DIMM0	AD13
SMA[4]	DIMM0	AD11
SMA[5]	DIMM0	AC13
SMAB[1]	DIMM1	AD16
SMAB[2]	DIMM1	AC12
SMAB[4]	DIMM1	AF11
SMAB[5]	DIMM1	AD10

The CPC signal routing shall transition from an external layer to an internal signal layer under the GMCH. Keep the same internal layer until transitioning out to an external layer to connect to the appropriate pad of the DIMM connector and the parallel termination resistor. When the layout requires additional routing before the termination resistor, return to the same internal layer and transition to an external layer immediately prior to parallel termination resistor.

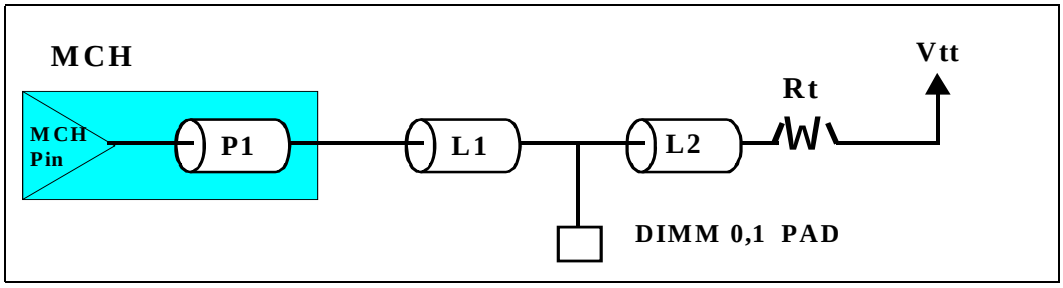
External trace lengths shall be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals shall be ground reference to keep the path of return current continuous. Intel suggests that all control signals be routed on the same internal layer.

Resistor packs are acceptable for the parallel (Rt) control termination resistors, but control signals cannot be placed within the same R pack as the data or command signals. The table and diagrams below depict the recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

5.4.7.1 CPC Signal Routing Topology

Figure 73 depicts the CPC control signal routing topology.

Figure 73. CPC Control Signal Routing Topology



The CPC signals shall be routed using 2:1 trace space to width ratio for signals within the DDR group, except clocks and strobes. CPC signals shall be routed on inner layers with minimized external trace lengths.

5.4.7.2 CPC Signal Routing Guidelines

Table 41 presents CPC control signal routing guidelines.

Table 41. CPC Control Signal Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[5,4,2,1], SMAB[5,4,2,1]
Motherboard Topology	Point-to-Point with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2:1 (e.g., 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils ± 250 mils Refer to package length Table 42 for exact lengths.
Trace Length P1+ L1	Min = 2.0 inches Max = 6.0 inches
Trace Length L2 – DIMM Pad to Parallel Termination Resistor Pad	Max = 2.0 inches
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	3
Length Matching Requirements	Match CPC to SCK[5:0]/SCK[5:0]# Refer to length matching Section 5.4.7.3 and Figure 74 for details.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. It is possible to route using two vias if one via is shared that connects to the DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the DIMM must comply with clock length matching requirements.

5.4.7.3 CPC to Clock Length Matching Requirements

The total length of the CPC signals, between the GMCH die-pad and the DIMM must fall within the range defined below, with respect to the associated clock reference length. Refer to Figure 73 for a definition of the various trace segments. The length the trace from the DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 74. A table of CPC signal package length is provided at the end of this section.

Length range formula for DIMM0:

X_0 = SCK[2:0]/SCK[2:0]# total reference length, including package length. Refer to Section 5.4.1 for more information.

Y_0 = SMA[5,4,2,1] total length = GMCH Package length + L1, as shown in Figure 73, where:

$(X_0 – 1.5”) \leq Y_0 \leq (X_0 - 0.5”)$

Length range formula for DIMM1:

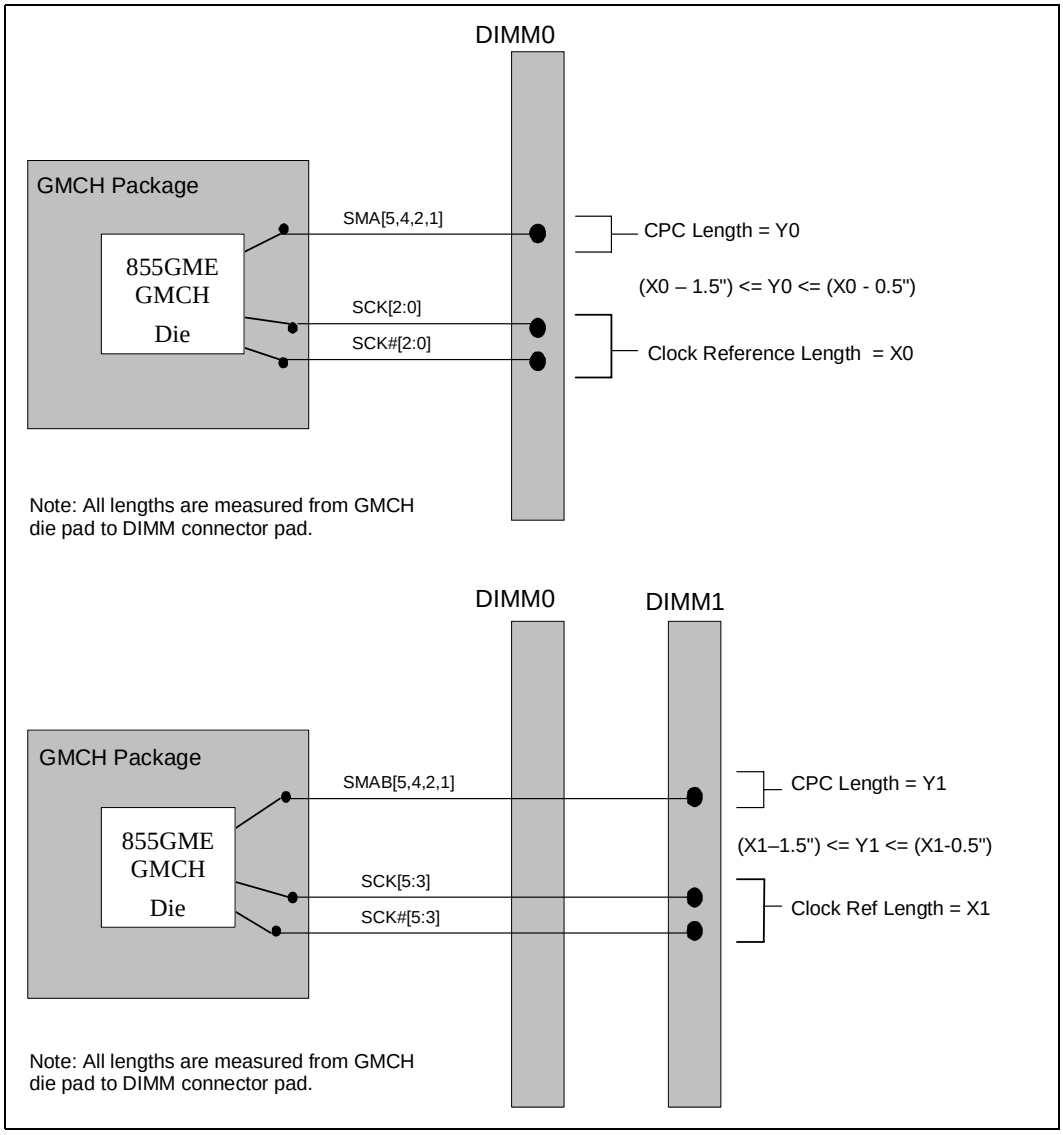
X_1 = SCK[5:3]/SCK[5:3]# total reference length, including package length. Refer to Section 5.4.1 for more information.

Y_1 = SMAB[5,4,2,1] total length = GMCH Package length + L1, as shown in Figure 73, where:

$(X_1 – 1.5”) \leq Y_1 \leq (X_1 - 0.5”)$

No length matching is required from DIMM1 to the termination resistor. Figure 74 depicts the length matching requirements between the CPC signals and clock. A nominal CPC package length of 500 mils may be used to estimate baseline Mbyte lengths.

Figure 74. CPC Signals to Clock Length Matching Diagram



5.4.7.4 CPC Group Package Length Table

The package length data in Table 42 shall be used to match the overall length of each CPC signal to its associated clock reference length.

Table 42. CPC Group Package Lengths

Signal	Pin Number	Pkg Length (mils)
SMA[1]	AD14	398
SMA[2]	AD13	443
SMA[4]	AD11	430
SMA[5]	AC13	346
SMAB[1]	AD16	427
SMAB[2]	AC12	395
SMAB[4]	AF11	716
SMAB[5]	AD10	631

5.4.8 Feedback – RCVENOUT#, RCVENIN#

The 82855GME provides a feedback signal called ‘receive enable’ (RCVENIN#), which is used to measure timing for memory read data. The Intel 855GME chipset has the RCVENOUT# signal shunted directly to RCVENIN# inside the package to reduce timing variation. With this change it is no longer necessary to provide an external connection. However, it is recommended that both signals be transitioned to the bottom side with vias located adjacent to the package ball in order to facilitate probing.

5.5 ECC Guidelines

The GMCH may be configured to operate in an ECC data integrity mode that allows multiple bit error detection and single bit error correction. This option to design for and support ECC DDR memory modules is dependent on design objectives. By default ECC functionality is disabled on the platform.

For more information on ECC functionality, see the *Intel® 855GME Chipset Graphics and Memory Controller Hub (GMCH) Specification Update Addendum for Embedded Applications*.

5.5.1 GMCH ECC Functionality

When non-ECC memory modules are to be the only supported memory type on the platform, the eight DDR check bits signals, associated strobe and data mask bit associated with the ECC device for each DIMM may be left as no connects on the GMCH.

Note: All three differential clocks per DDR DIMM must be routed and driven to each respective DIMM connector, regardless of ECC support.

The DRAM Data Integrity Mode (DDIM) bit of the DRC register (Device 0; Offset 7C-7Fh; bit 21) provides the option to enable or disable ECC operation mode in the GMCH. By default, this bit is set to '0' and ECC functionality is disabled. In such a case, the SDQ[71:64] and SDQS8 pins of the GMCH may be left as no connects.

On platforms where ECC memory is supported, it is important that all relevant SDQ and SDQS signals to the DIMMs be disabled when the system is populated with only non-ECC or a combination of ECC and non-ECC memory. In such cases, the registers mentioned in the next section must be programmed appropriately.

5.5.2 DRAM Clock Flexibility

The DRAM Clock Control Disable Register (DCLKDIS: I/O Address 2E-2Fh) and the DRAM Controller Power Management Control Register, bit 10, (PWRMG: I/O Address 68-6Bh) provides the capability to enable and disable the CS/CKE and SCK signals to unpopulated DIMMs. The GMCH provides the flexibility to route any differential clock pair to any SCK clock pair on the DIMMs provided that the BIOS enables/disables these clocks appropriately (e.g., the GMCH's SCK0 pair may be routed either to the DIMM's SCK0 pair or any other pair such as SCK1 or SCK2, etc.).

Integrated Graphics Display Port 6

The GMCH contains four display ports: an analog CRT port, a dedicated LVDS port, and two 12-bit Digital Video Out (DVO) ports. Section 6.1 discusses the CRT and RAMDAC routing requirements. Section 6.2 discusses the dedicated LVDS port. Section 6.3 discusses the DVOB and DVOC design guideline. Section 6.4 provides recommendations for a flexible modular design guideline for DVOB and DVOC muxed interfaces. Section 6.5 provides recommendations for the GPIO signal group.

6.1 Analog RGB/CRT Guidelines

6.1.1 RAMDAC/Display Interface

The GMCH integrated graphics/chipset design interfaces to an analog display using a RAMDAC. The RAMDAC is a subsection of the graphics controller display engine and consists of three identical 8-bit digital-to-analog converter (DAC) channels, one for the display's red, green, and blue electron guns.

Each RGB output is doubly terminated with a 75 Ω resistance: One 75 Ω resistance is connected from the DAC output to the board ground, and the other termination resistance exists within the display. The equivalent DC resistance at the output of each DAC is 37.5 Ω. The current output from each DAC flows into this equivalent resistive load to produce a video voltage, without the need for external buffering. There is also an LC pi-filter on each channel that is used to reduce high-frequency noise and to reduce EMI. In order to maximize the performance, the filter impedance, cable impedance, and load impedance shall be matched.

Since the DAC runs at speeds up to 350 MHz, special attention shall be paid to signal integrity and EMI. RGB routing, component placement, component selection, cable and load impedance (monitor). They all play a large role in the analog display's quality and robustness. This holds true for all resolutions, but especially for those at 1600 x 1200 resolutions or higher.

6.1.2 Reference Resistor (RSET)

A reference resistor, Rset, is used to set the reference current for the DAC. This resistor is an external resistor with a 1% tolerance that is placed on the circuit board. A reference resistor may be selected from a range between 124 Ω to 137 Ω (1 percent). Based on board design, DAC RGB outputs may be measured when the display is completely white. When the RGB voltage value is between 665 mV and 770 mV, the video level is within VESA specification and the resistor value that was chosen is optimal for board design. Refer to Figure 76 for the recommended Rset placement.

A reference voltage is generated on the GMCH from a bandgap voltage reference circuit. The bandgap reference voltage level is approximately 1.2 V and this voltage is divided by four to generate the reference voltage. The VESA video standard defines the LSB current for each DAC channel. The RAMDAC reference current is designed on-die to be equal to 32 LSB.

6.1.3 RAMDAC Board Design Guidelines

For the DAC to successfully run at speeds up to 350 MHz, care shall be taken when routing the analog RAMDAC signals. Intel recommends that each analog R, G, and B signal be routed single-endedly. The analog RGB signals shall be routed with an impedance of 37.5 Ω. Intel recommends that these routes be routed on an inner routing layer and that it be shielded with VSS planes, if possible. Spacing between DAC channels and to other signals shall be maximized; 20-mil spacing is recommended. The RGB signals require pi filters that shall be placed near the VGA connector. It consists of two 3.3 pF caps with a 75 Ω at 100 MHz FB between them. The RGB signals shall have a 75 Ω, 1 percent terminating pull-down resistor. The complement signals (R#, G#, and B#) shall be grounded to the ground plane.

Intel recommends that the pi filter and terminating resistors be placed as close as possible to the VGA connector. After the 75 Ω termination resistor, the RGB signals shall continue on to their pi filters and the VGA connector, but shall now ideally be routed with a 75 Ω impedance (~ 5 mil traces).

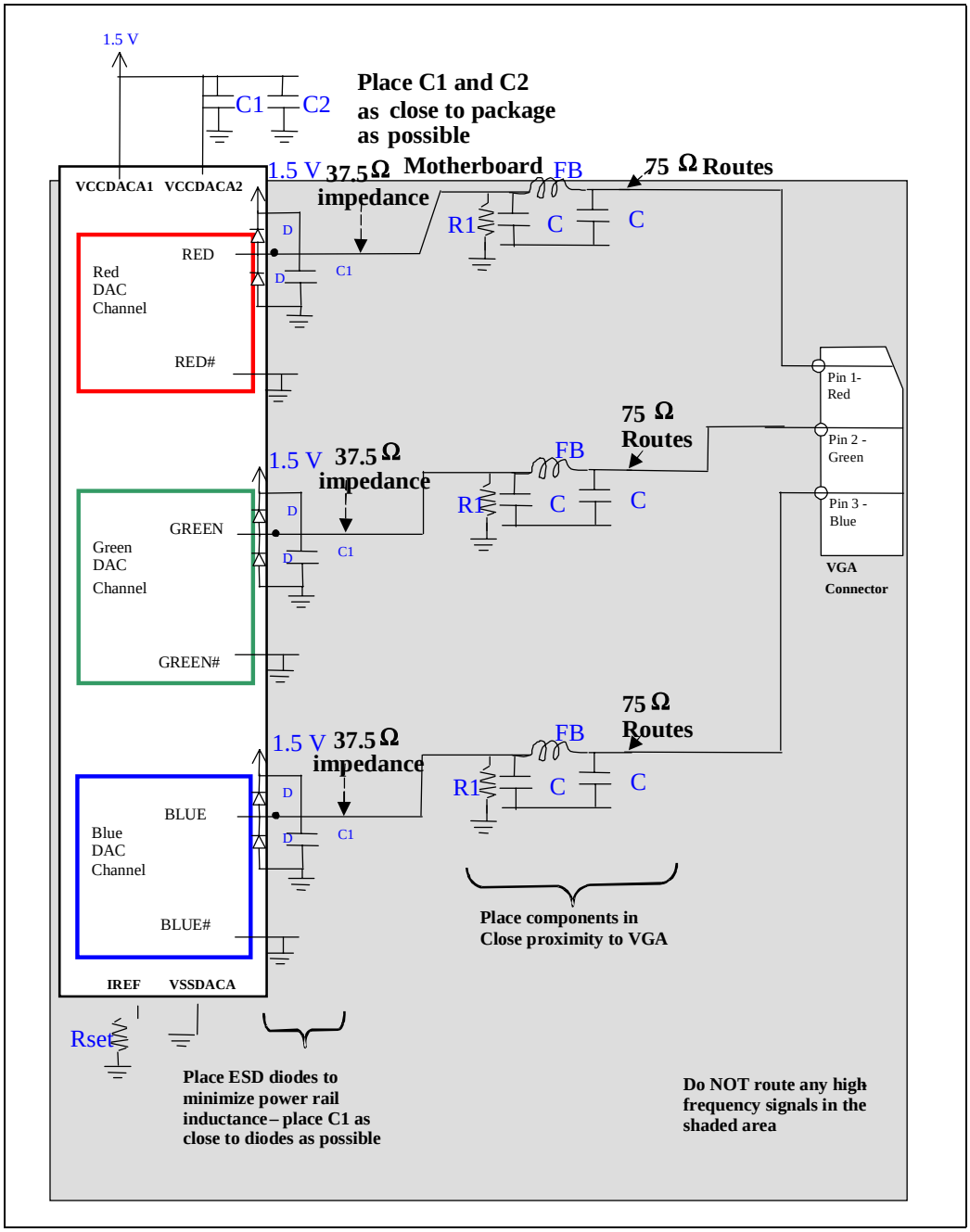
The RGB signals also require protection diodes between 1.5 V and ground. These diodes shall have low C ratings (~5 pF max) and small leakage current (~ 10 µA at 120° C) and shall be properly decoupled with a 0.1 µF cap. These diodes and decoupling shall be placed to minimize power rail inductance. The choice between diodes (or diode packs) shall comprehend the recommended electrical characteristics in addition to cost.

The RGB signals shall be length matched as closely as possible, from the Intel® 855GME chipset Graphics Memory Controller Hub (82855GME) to the VGA connector and shall not exceed 200 mils of mismatch.

6.1.4 DAC Routing Guidelines

Figure 75 presents the GMCH DAC routing guidelines.

Figure 75. GMCH DAC Routing Guidelines



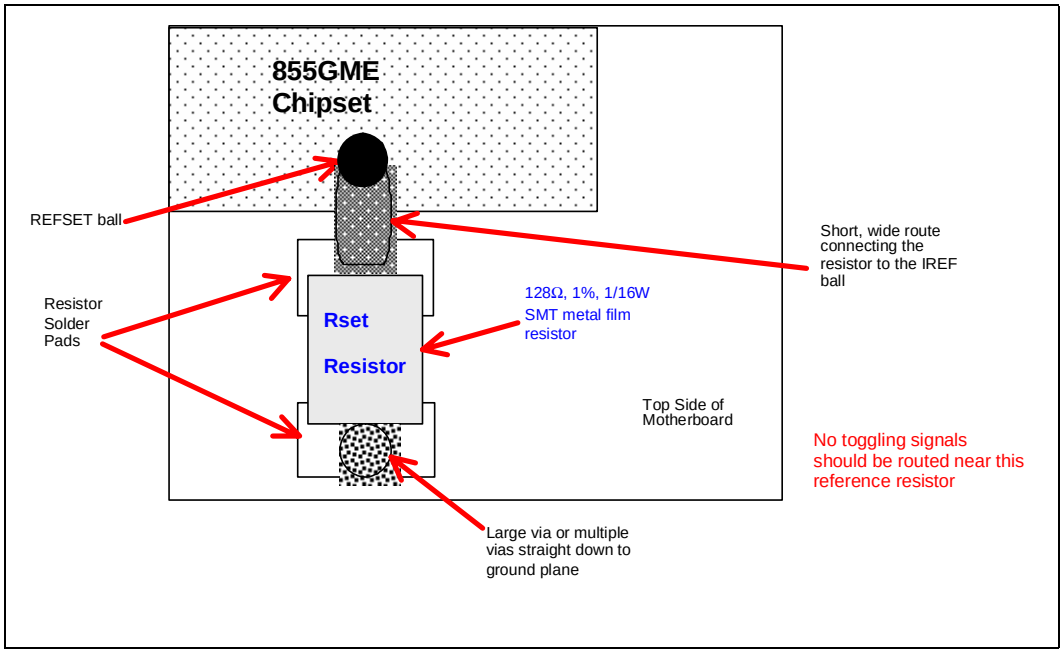
The DAC channel (red, green, blue) outputs are routed as single-ended shielded current output routes that are terminated prior to connecting to the video PI-filter and VGA connector. Table 43 presents the recommended GMCH DAC components.

Table 43. Recommended GMCH DAC Components

Recommended DAC Board Components				
Component	**Value**	**Tolerance**	**Power**	**Type**
R1	75.0 Ω	1 %	1/16 W	SMT, Metal Film
Rset	128.0 Ω	1 %	1/16 W	SMT, Metal Film
C1	0.1 µF	20 %	-----	SMT, Ceramic
C2	0.01 µF	20 %	-----	SMT, Ceramic
C	3.3 pF	10 %	-----	SMT, Ceramic
D	PAC DN006	-------	350 mW	California Micro Devices – ESD diodes for VGA SOIC package Or equivalent diode array
FB	75 Ω @ 100 MHz	--------	-------	MuRata* BLM11B750S

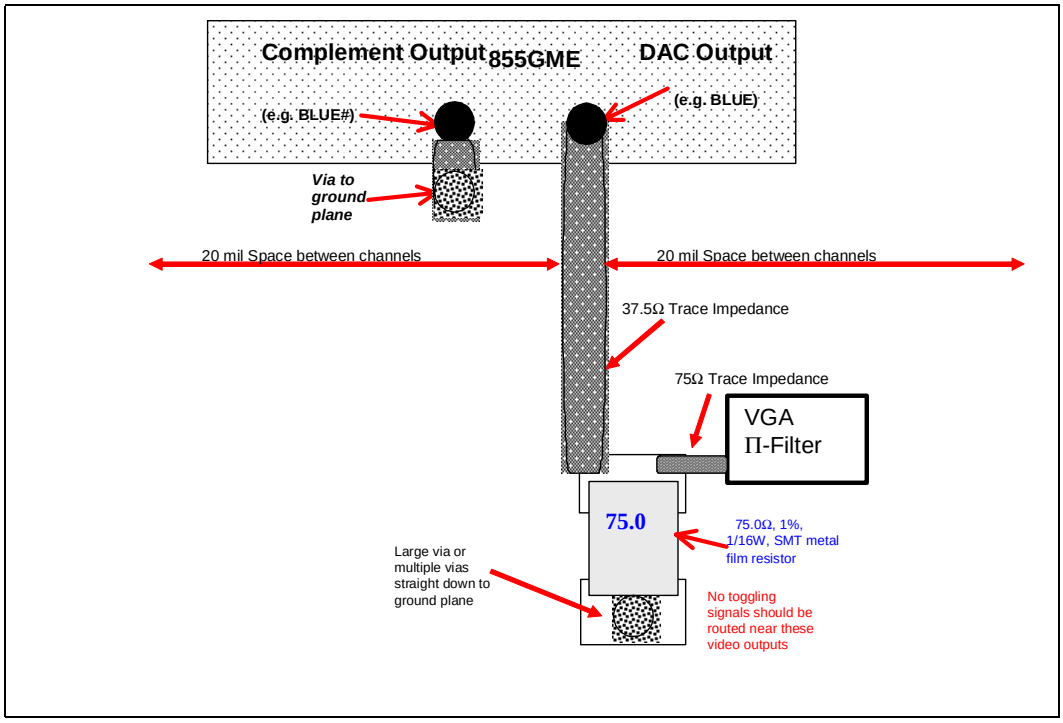
Figure 76 depicts the recommended Rset placement.

Figure 76. Rset Placement



The recommended routing of the termination resistors is shown in Figure 77.

Figure 77. DAC R, G, B Routing and Resistor Layout Example



6.1.5 DAC Power Requirements

The DAC requires a 1.5 V supply through its two VCCADAC balls. The two may share a set of capacitors, 0.1 µF and 0.01 µF, but this connection shall have low inductance. Separate analog power or ground planes are not required for the DAC.

However, because the DAC is an analog circuit, it is particularly sensitive to AC noise seen on its power rail. Designs shall provide as clean and quiet a supply as possible to the VCCA_DAC. Additional filtering and/or separate voltage rail may be needed to do so.

- Video DAC Power Supply DC Specification: 1.50 V ± 5 percent
- Video DAC Power Supply AC Specification:
  - ± 0.3 percent from 0.10 Hz to 10 MHz
  - ± 0.95 percent from 10 MHz to maximum pixel clock frequency
- Absolute minimum voltage at the VCCA package ball = 1.40 V

Refer to the latest *Intel® 855GM/855GME Chipset (GMCH) Datasheet* for latest AC/DC specification.

6.1.6 HSYNC and VSYNC Design Considerations

HSYNC and VSYNC signals are connected to the analog display attached to the VGA connector. These are 3.3 V outputs from the GMCH. A 39 Ω series resistor is required before routing to the VGA connector. Also, capacitors (28 pF to 33 pF) before and after the series resistor may be needed to meet the VESA rise/fall time specification.

Unidirectional buffers (high impedance buffers) are required on both HYSNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.

6.1.7 DDC and I2C Design Considerations

DDCADATA and DDCACLK are 3.3 volt IO buffers connecting the GMCH to the monitor. To avoid potential electrical overstress on these signals, bidirectional level-shifting devices are required. These signals require 2.2 kΩ pull-ups (or pull-ups with the appropriate value derived from simulation) on each of these signals. Refer to Section 6.5 for further pull-up recommendations for the DDC (GPIO) signal group.

6.2 LVDS Transmitter Interface

The Intel® LVDS (Low Voltage Differential Signaling) transmitter serializer converts up to 18 bits of parallel digital RGB data, (6 bits per RGB), along with up to 4 bits for control (SHFCLK, HSYNC, VSYNC, DE) into two 4 channel serial bit streams for output by the LVDS transmitter.

The transmitter is fully differential and utilizes a current mode drive with a high impedance output. The drive current develops a differential swing in the range of 250 mV to 450 mV across a 100 Ω termination load.

The parallel digital data is serially converted to a 7-bit serial bit stream that is transmitted over the 8-channel LVDS interface at 7x the input clock. The differential output clock channel transmits the output clock at the input clock frequency. While the differential output channels transmit the data at the 7x clock rate (1 bit time is 7x the input clock). The 7x serializer synchronizes and regenerates an input clock from 35 MHz to 112 MHz. Typical operation is at 65 MHz (15.4 ns), therefore, at a 7x clock rate, 1bit time would be 2.2 ns. With data cycle times as small as 2.2 ns, propagation delay mismatch is critical, such that intra-channel skew (skew between the inverting and non-inverting output) must be kept minimal.

The following differential signal groups comprise the LVDS interface. The topology rules for each group are defined in subsequent sections.

Table 44. Signal Group and Signal Pair Names

Channel	Signal Group	Signal Pair Names
Channel A	Clocks	ICLKAM, ICLKAP
	Data Bus	IYAM[3:0], IYAP[3:0]
Channel B	Clocks	ICLKBM, ICLKBP
	Data Bus	IYBM[3:0], IYBP[3:0]

6.2.1 Length Matching Constraints

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group. These recommendations are provided to achieve optimal SI and timing. In addition to the absolute length limits provided, more restrictive length matching requirements are also provided. The additional requirements further restrict the minimum to maximum length range of each signal group with respect to clock strobe, within the overall boundaries defined in the guideline tables, as required to ensure adequate timing margins. These secondary constraints are referred to as length matching constraints. The amount of minimum to maximum length variance allowed for each group around the clock strobe reference length varies from signal group to signal group depending on the amount of timing variation that may be tolerated. Refer to Table 45 for LVDS length matching requirements.

Each LVDS channel is length matched to the LVDS strobe signals. The strobes on a given channel are matched to within ± 25 mils of the target length.

Table 45. LVDS Signal Trace Length Matching Requirements

Signal Group	Data pair	Signal Matching	Clock Strobes associated with the Channel	Strobe Matching
CHANNEL A	IYAM0, IYAP0	± 20 mils	ICLKAM, ICLKAP	± 20 mils
	IYAM1, IYAP1	± 20 mils		
	IYAM2, IYAP2	± 20 mils		
	IYAM3, IYAP3	± 20 mils		
CHANNEL B	IYBM0, IYBP0	± 20 mils	ICLKAM, ICLKAP	± 20 mils
	IYBM1, IYBP1	± 20 mils		
	IYBM2, IYBP2	± 20 mils		
	IYBM3, IYBP3	± 20 mils		

NOTE: All length matching formulas are based on GMCH die-pad to LVDS connector pin total length. Package length tables are provided for all signals in order to facilitate this pad-to-pin matching.

6.2.1.1 Package Length Compensation

As mentioned in Section 6.2.1, all length matching is done from GMCH die-pad to LVDS connector pin. The reason for this is to compensate for the package length variation across each signal group in order to minimize timing variance. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the GMCH requires a length matching process. Refer to Table 47 for the Intel 855GME chipset LVDS package lengths information.

Package length compensation shall not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting package length variance across a signal group. Of course, there is some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

6.2.2 LVDS Routing Guidelines

Table 46. LVDS Signal Group Routing Guidelines

Parameter	Definition
Signal Group	LVDS
Topology	Differential Pair Point to Point
Reference Plane	Ground Referenced
Differential Mode Impedance (Zdiff)	100 Ω ± 15%
Nominal Trace Width	4 mils
Nominal Pair Spacing (edge to edge)	7 mils
Minimum Pair to Pair Spacing (See exceptions for breakout region below.)	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other LVDS Signals (See exceptions for breakout region below.)	20 mils
Minimum Isolation Spacing to non-LVDS Signals	20 mils
Maximum Via Count	2 (per line)
Package Length Range – P1	550 mils ± 150mils (Refer to Table 47 for exact lengths.)
Total Length –	Max 10”
Clock Length Matching	Match all segments to ± 20 mils (Refer to Section 6.2.1 for more information.)
Clock to Clock Length Matching (Total Length)	Match clocks to X0 ± 20 mils
Breakout Exceptions (Reduced geometries for GMCH breakout region)	Breakout section shall be as shorter as possible. Try to maintain trace width as 4 mils, spacing 7 mils, while the spacing between pairs may be 10-20 mils.

The traces associated with the LVDS Transmitter timing domain signals are differential traces terminated across 100 Ω ± 15 Ω and shall be routed as:

- Strip-line only.
- Isolate all other signals from the LVDS signals to prevent coupling from other sources onto the LVDS lines.
- Use controlled impedance traces that match the differential impedance of your transmission medium (i.e., cable) and termination resistor (**Note**: the transmission medium’s Zdiff shall be maintained to 100 Ω ± 15 percent).
- Run the differential pair trace lines as close together as possible as soon as they leave the IC, not greater than 10 mils. This helps eliminate reflections and ensure noise is coupled as common mode. Plus, noise induced on the differential lines is much more likely to appear as common mode, which is rejected by the receiver.
- The LVDS transmitter timing domain signals have a maximum trace length of 10.0 inches. This maximum applies to all of the LVDS transmitter signals.
- Traces must be ground referenced and must not switch layers between the GMCH and connector.

When choosing cables, it is important to remember:

- Use controlled impedance media. The differential impedance of cable LVDS uses shall be 100 Ω. Cables shall not introduce major impedance discontinuities that cause signal reflection.
- Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable, multi-conductor) for noise reduction and signal quality.
- Cable length must be less than 16 inches.

Table 47. LVDS Package Lengths

Signal Group	GMCH Signal Name	Package Trace Length (mils)	Signal Group	GMCH Signal Name	Package Trace Length (mils)
CHANNEL A	ICLKAP	503.7	CHANNEL B	ICLKAP	502.0
	ICLKAM	498.8		ICLKAM	499.1
	IYAP0	399.6		IYBP0	359.8
	IYAM0	385.4		IYBM0	353.7
	IYAP1	487.5		IYBP1	524.7
	IYAM1	466.2		IYBM1	516.6
	IYAP2	572.6		IYBP2	623.3
	IYAM2	566.2		IYBM2	604.2
	IYAP3	643.2		IYBP3	441.8
	IYAM3	637.8		IYBM3	441.7

6.3 Digital Video Out Port

The GMCH DVO port interface supports a wide variety of third party DVO-compliant devices (e.g., TV encoder, TMDS transmitter or integrated TV encoder and TMDS transmitter). The 82855GME has two dedicated Digital Video Out Ports (DVOB and DVOC). Intel's DVO port is a 1.5 V only interface that may support transactions up to 165 MHz. Some of the DVO port command signals may require voltage translation circuit depending on the third party device.

6.3.1 DVO Interface Signal Groups

Table 48 shows the DVO interface signal groups.

Table 48. DVO Interface Signal Groups

Signal Group	GMCH Signal Name	Signal Type	Signal Group	GMCH Signal Name	Signal Type
DVOB	DVOBFLDSTL	Input	DVOC	DVOCFLDSTL	Input
	DVOBHSYNC	Output		DVOCHSYNC	Output
	DVOBVSYNC	Output		DVOCVSYNC	Output
	DVOBBLANK#	Output		DVOCBLANK#	Output
	DVOBD[11:0]	Output		DVOCD[11:0]	Output
	DVOBCLK (DVOBCLK[0])	Output Strobe		DVOCCLK (DVOCCLK[0])	Output Strobe
	DVOBCLK# (DVOBCLK[1])	Output Strobe		DVOCCLK# (DVOCCLK[1])	Output Strobe
Common Signals for Both DVO Ports	DVOBCCLKINT	Input	Voltage Reference, RCOMP	DVORCOMP	
	DVOBCINTR#	Input			
	ADDID[7:0]	Input		GVREF	
	DVODETECT	Input			

6.3.1.1 DVO/I²C to AGP Pin Mapping

The DVODETECT signal is muxed with the GPAR signal on the AGP bus. This signal will act as a strap to indicate if the interface is in AGP or DVO mode. The GMCH has an internal 8.2-k, pull-down on this signal that will naturally pull it low. If an AGP graphics device is present, the signal will be pulled high at the AGP graphics device and the AGP/DVO mux select bit in the SHIC register will be set to AGP mode.

The SBA[7:0] signals act as straps for an ADDID. These pins are used to communicate to the Video BIOS when an external device is interfaced to the DVO port. If an on-board DVO device is implemented, ADDID[7] should be strapped low. When an AGP graphics device is present, DVODETECT=1 (AGP mode).

Table 49. AGP/DVO Pin Muxing

DVO MODE	AGP MODE	DVO MODE	AGP MODE	DVO MODE	AGP MODE
DVOBD[0]	GAD[3]	DVOCD[0]	GAD[19]	MI2CCLK	GIRDY#
DVOBD[1]	GAD[2]	DVOCD[1]	GAD[20]	MI2CDATA	GDEVSEL#
DVOBD[2]	GAD[5]	DVOCD[2]	GAD[21]	MDVICLK	GTRDY#
DVOBD[3]	GAD[4]	DVOCD[3]	GAD[22]	MDVIDATA	GFRAME#
DVOBD[4]	GAD[7]	DVOCD[4]	GAD[23]	MDDCCDATA	GAD[15]
DVOBD[5]	GAD[6]	DVOCD[5]	GCBE#[3]	MDDCCLK	GSTOP#
DVOBD[6]	GAD[8]	DVOCD[6]	GAD[25]	DVOBCINT#	GAD[30]
DVOBD[7]	GCBE#[0]	DVOCD[7]	GAD[24]	DVOBCCLKINT	GAD[13]
DVOBD[8]	GAD[10]	DVOCD[8]	GAD[27]	ADDID[7]	GSBA[7]
DVOBD[9]	GAD[9]	DVOCD[9]	GAD[26]	ADDID[6]	GSBA[6]
DVOBD[10]	GAD[12]	DVOCD[10]	GAD[29]	ADDID[5]	GSBA[5]
DVOBD[11]	GAD[11]	DVOCD[11]	GAD[28]	ADDID[4]	GSBA[4]
DVOBCLK	GADSTB[0]	DVOCCLK	GADSTB[1]	ADDID[3]	GSBA[3]
DVOBCLK#	GADSTB#[0]	DVOCCLK#	GADSTB#[1]	ADDID[2]	GSBA[2]
DVOBHSYNC	GAD[0]	DVOCHSYNC	GAD[17]	ADDID[1]	GSBA[1]
DVOBVSYNC	GAD[1]	DVOCVSYNC	GAD[16]	ADDID[0]	GSBA[0]
DVOBBLANK#	GCBE#[1]	DVOCBLANK#	GAD[18]	DVODETECT	GPAR
DVOBFLDSTL	GAD[14]	DVOCFLDSTL	GAD[31]	DPMS	GPIPE#

6.3.2 DVOB and DVOC Port Interface Routing Guidelines

For Intel 855GME chipset platforms, guidelines apply for both interfaces.

6.3.2.1 Length Mismatch Requirements

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching requirements are also provided that further restrict the minimum to maximum length range of each signal group with respect to clock strobe, within the overall boundaries defined in the guideline tables, as required to ensure adequate timing margins. These secondary constraints are referred to as length matching constraints. The amount of minimum to maximum length variance allowed for each group around the clock strobe reference length varies from signal group to signal group depending on the amount of timing variation, which may be tolerated. Refer to Table 50 for DVO length matching requirements.

Table 50. DVO Interface Trace Length Mismatch Requirements

Data Group	Signal Matching to Strobe Clock	DVO Clock Strobes Associated With the Group	Clock Strobe Matching	Notes
DVOBD [11:0]	±100 mils	DVOBCLK[1:0]	± 10 mils	1, 2
DVOCD [11:0]	±100 mils	DVOCCLK[1:0]	± 10 mils	1, 2

NOTES:
1. Data signals of the same group shall be trace length matched to the clock within ± 100 mil including package lengths.
2. **All length matching formulas are based on GMCH die-pad to DVO device pin total length.** Package length tables are provided for all signals to facilitate this pad-to-pin matching.

6.3.2.2 Package Length Compensation

As mentioned in Section 6.3.2.1, all length matching is done from GMCH die-pad to DVO connector pin. The reason for this is to compensate for the package length variation across each signal group in order to minimize timing variance. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the GMCH requires a length matching process. Refer to Table 52 for the DVOB package lengths information and refer to Table 53 for DVOC package lengths information.

Package length compensation shall not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting out package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

6.3.2.3 DVOB and DVOC Routing Guidelines

Table 51 provides the DVOB and DVOC routing guideline summary.

Table 51. DVOB and DVOC Routing Guideline Summary

Parameter	Definition
Signal Group	DVOBD [11:0], DVCBD [11:0]
Motherboard Topology	Point to point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils
Minimum Spacing to Trace Width Ratio	2:1 (e.g., 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DVO Signals	20 mils
Minimum Spacing to Other DVO Signals	12 mils (See exceptions for breakout region below.)
Minimum Spacing of DVOBCLK [1:0] or DVOCCLK[1:0] to any other signals	12 mils
Package Length Range – P1	Refer to Table 52 and Table 53 for package lengths.
Total Length –	Max 6”
Data to Clock Strobe Length Matching Requirements	+ 100 mils (Refer to Table 50 for length matching requirements.)
CLK0 to CLK1 Length Matching Requirements	+ 10 mils (Refer to Table 50 for length matching requirements.)

The routing guideline recommendations in this section apply for both interfaces. Refer to Table 52 for GMCH DVOB package lengths and Table 53 for GMCH DVOC package lengths.

- All signals shall be routed as striplines (inner layers).
- All signals in a signal group shall be routed on the same layer. Routing studies have shown that these guidelines may be met. The trace length and trace spacing requirements ***must*** not be violated by any signal.
- Route the DVOBCLK[1:0] or DVOCCLK[1:0] signal pairs 4 mils wide and 8 mils apart with a max trace length of 6 inches. This signal pair shall be a minimum of 12 mils from any adjacent signals.
- To break out of the 82855GME, the DVOB and/or DVOC data signals may be routed with a trace width of 4 mils and a trace spacing of 7 mils. The signals shall be separated to a trace width of 4 mils and a trace spacing of 8 mils within 0.3 inches of the GMCH component.

Table 52. DVOB Interface Package Lengths (Sheet 1 of 2)

Signal	Pin Number	Package Length (mils)
DVOBBLANK#	L2	583
DVOBCCLKINT	M3	520
DVOBCINTR#	G2	712
DVOBCLK	P3	475
DVOBCLK#	P4	439
DVOBD[0]	R3	489

Table 52. DVOB Interface Package Lengths (Sheet 2 of 2)

Signal	Pin Number	Package Length (mils)
DVOBD[1]	R5	439
DVOBD[2]	R6	343
DVOBD[3]	R4	415
DVOBD[4]	P6	409
DVOBD[5]	P5	387
DVOBD[6]	N5	466
DVOBD[7]	P2	553
DVOBD[8]	N2	568
DVOBD[9]	N3	504
DVOBD[10]	M1	611
DVOBD[11]	M5	510
DVOBFLDSTL	M2	566
DVOBHSYNC	T6	339

Table 53. DVOC Interface Package Lengths

Signal	Pin Number	Package Length (mils)
DVOCBLANK#	L3	541
DVOCCLK	J3	601
DVOCCLK#	J2	675
DVOCD[0]	K5	489
DVOCD[1]	K1	692
DVOCD[2]	K3	622
DVOCD[3]	K2	685
DVOCD[4]	J6	536
DVOCD[5]	J5	518
DVOCD[6]	H2	720
DVOCD[7]	H1	771
DVOCD[8]	H3	649
DVOCD[9]	H4	625
DVOCD[10]	H6	521
DVOCD[11]	G3	762
DVOCFLDSTL	H5	566
DVOCHSYNC	K6	491
DVOCVSYNC	L5	440

6.3.2.4 DVOB and DVOC Port Termination

The DVO interface does not require external termination.

6.3.3 DVOB and DVOC Assumptions, Definitions, and Specifications

The source synchronous solution space consists of all designs in which the flight time mismatch between a strobe and its associated data is less than the total allowable skew:

$T_{skew} = T_{flightdata} - T_{flightstrobe}$

Where $T_{flightdata}$ and $T_{flightstrobe}$ are the driver-pad-to-receiver-pin flight times of the data and the strobe respectively.

The DVO physical interface is a point-to-point topology using 1.5 V signaling. The DVO uses a 165 MHz clock.

The flight time skew simulations reproduce all parameters that could cause a skew between two signals, including motherboard and add-in card line lengths, effective capacitance in the buffer models, crosstalk on each of the different interconnect combinations, data pattern dependencies, and ISI induced skews.

6.3.4 DVOB and DVOC Simulation Method

A model for simulation purposes is shown in Figure 78. The DVO component is a third party-chip.

Figure 78. DVOB and DVOC Simulations Model

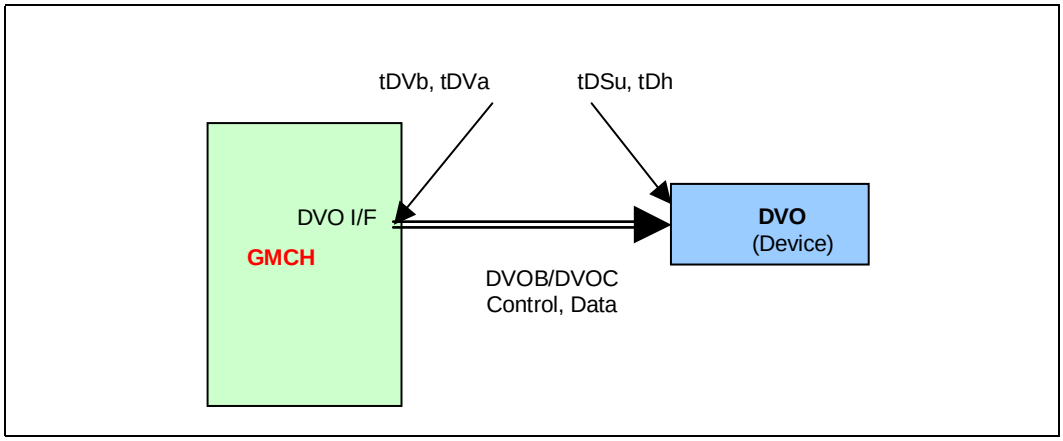
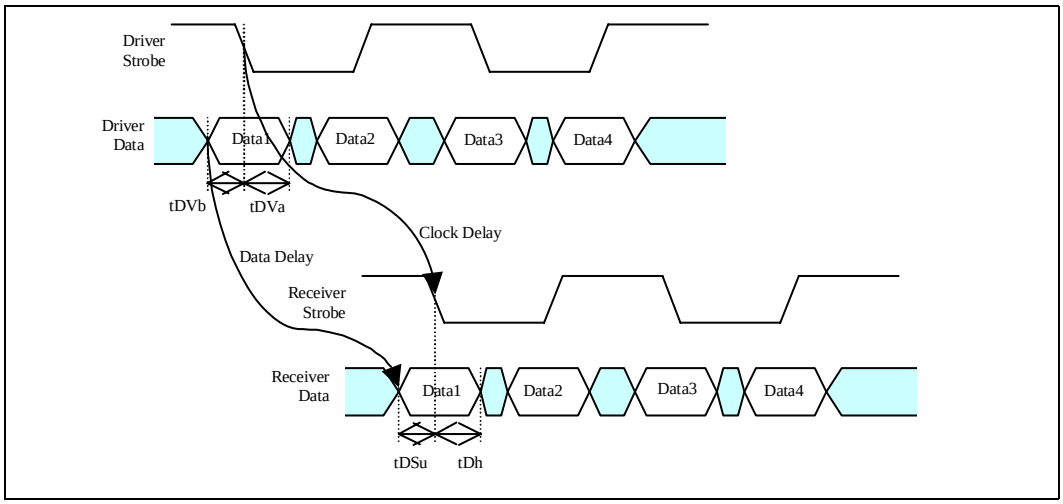


Figure 79. Driver-Receiver Waveforms Relationship Specification



The setup margin and the hold margin for a particular design depends on the values of the data valid times and the data setup and hold times on both the driver and the receiver sides. However, available margins are not absolute values. Any skew due to routing and loading differences, any coupling differences in the parallel traces, and any effects of SSO (ISI, ground bounce, etc.) shall be accounted for in the timing budget as they reduce the total available margin for the design.

Table 54. Allowable Interconnect Skew Calculation

Component	Skew Element	Symbol	Setup	Hold	Units
Driver	Data Valid before Strobe	tDVb	570		ps
	Data Valid after Strobe	tDVa		770	ps
Interconnect	Allowable Skew		Vendor Specific	Vendor Specific	ps
Receiver	Data Setup to Strobe	tDSu	Vendor Specific		ps
	Data Hold from Strobe	tDh		Vendor Specific	ps

All numbers in this table are from the 82855GME specification documents that are applicable for this interface. For third party receiver devices, refer to appropriate third party vendor specifications.

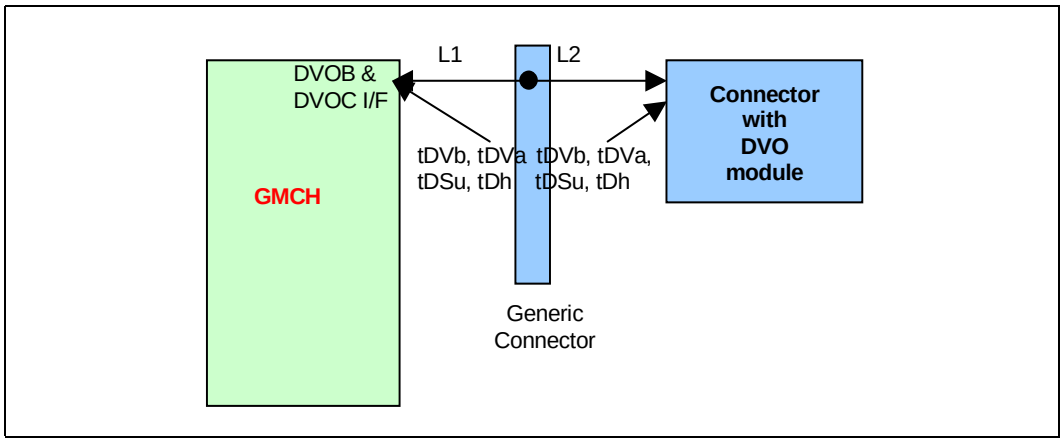
6.4 DVOB and DVOC Port Flexible (Modular) Design

The GMCH supports flexible design interfaces described in this section.

6.4.1 DVOB and DVOC Module Design

The 82855GME supports a DVO module design connected to the GMCH through a generic connector. Simulation method is the same as in Section 6.3.4. Lengths L1 and L2 are determined by simulation as L1 = 4 inches and L2 = 2 inches. Refer to Figure 81 for the generic connector parasitic model.

Figure 80. DVO Enabled Simulation Model



All signals shall be routed as striplines (inner layers).All signals in a signal group shall be routed on the same layer. Routing studies have shown that these guidelines may be met. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group shall be as close to ± 100 mils with respect to the strobe clocks as possible to provide optimal timing margin. Table 55 depicts DVO enabled routing guideline summary.

Table 55. DVO Enabled Routing Guideline Summary

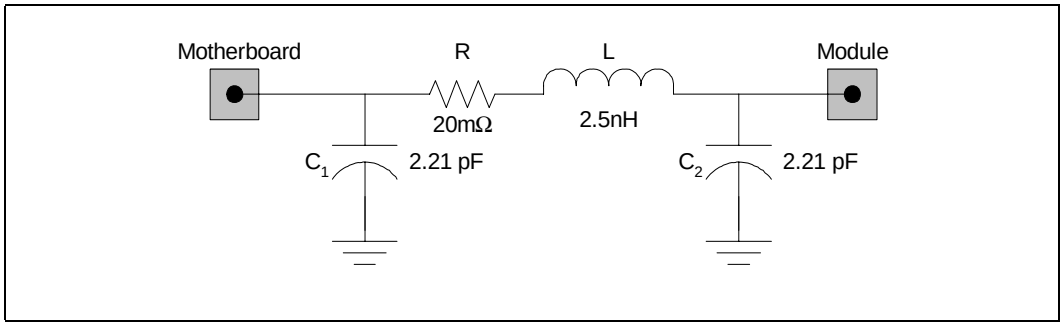
Signal	Maximum Length	Trace Width	Trace Spacing	Length Mismatch	Notes
DVO Timing Domain	L1=4 in L2=2 in	4 mils	8 mils	± 100 mils	

For DVO module case, the simulation model is the same as Figure 80 and the routing guideline is the same as in Table 55; each strobe pair must be separated from other signals by at least 12 mils. For multiplexed design, more conservative length mismatch (± 0.1 inches) is adopted.

6.4.1.1 Generic Connector Model

Figure 81 depicts the generic connector model used in simulation for flexible DVO implementation. This is only for reference. The actual connector may have different parasitic values. Designs using this approach need to be simulated first.

Figure 81. Generic Module Connector Parasitic Model



6.5 DVO GMBUS and DDC Interface Considerations

The GMCH DVOB and/or DVOC port controls the video front-end devices via the GMBUS (I^2C) interface. DDCADATA and DDCACLK shall be connected to the CRT connector. The GMBUS shall be connected to the DVO device, as required by the specifications for those devices. The protocol and bus may be used to configure registers in the TV encoder, TMDS transmitter, or any other external DVI device. The GMCH also has an option to utilize the DDCPCLK and DDCPDATA to collect EDID (Extended Display Identification) from a digital display panel.

Pull-ups (or pull-ups with the appropriate value derived from simulating the signal) typically ranging from 2.2 kΩ to 10 kΩ are required on each of these signals.

The following GMCH signal groups list the five possible GMBUS pairs.

Table 56. GMBUS Pair Mapping and Options

Pair #	Signal Name	Buffer Type	Description	Notes
0	DDCADATA	3.3 V	DDC for Analog monitor (CRT) connection	This cannot be shared with other DDC or I2C pairs due to legacy monitor issues.
	DDCACLK			
1	LCLKCTRLA	3.3 V	For control of SSC clock generator devices down on motherboard	If SSC is not supported, then may be used for DVOB or DVOC GMBUS.
	LCLKCTRLB			
2	DDCPDATA	3.3 V	DDC for Digital Display connection via the integrated LVDS display port for support for EDID panel*	If EDID panels are not supported, may optionally use as GMBUS for DVOB or DVOC.
	DDCPCLK			
3	MDVIDATA	1.5 V	GMBUS control of DVI devices (TMDS or TV encoder)	May optionally use as GMBUS for DVOB or DVOC.
	MDVICLK			
4	MI2CDATA	1.5 V	GMBUS control of DVI devices (TMDS or TV encoder)	May optionally use as GMBUS for DVOB or DVOC.
	MI2CCLK			
5	MDDCDATA	1.5 V	DDC for Digital Display connection via TMDS device	May optionally use as GMBUS for DVOB or DVOC.
	MDDCCLK			

NOTE: MDDC pair is not available for use with the Extreme Graphics Driver.
NOTE: All GMBUS pairs may be optionally programmed to support any interface and is programmed through the BMP utility.

When any of the GMBUS pairs (except DDCADATA/DDCACLK for CRT) are not used, 2.2 k-100 kΩ pull-up (or pull-ups with the appropriate value derived from simulating the signal) resistors are required except for LCLKCTRLA/LCLKCTRLB GMBUS pair. This prevents the GMCH DVOB interface from confusing noise on these lines for false cycles.

6.5.1 Leaving the GMCH DVOB or DVOC Port Unconnected

When the motherboard does not implement any of the possible video devices with the DVO port, follow the guidelines recommended on the motherboard. DVO Output signals may be left unconnected if they are not used.

Pull-down resistors are required for the following signals if not used:

- DVOBFLDSTL
- DVOCFLDSTL
- DVOBCCLKINT

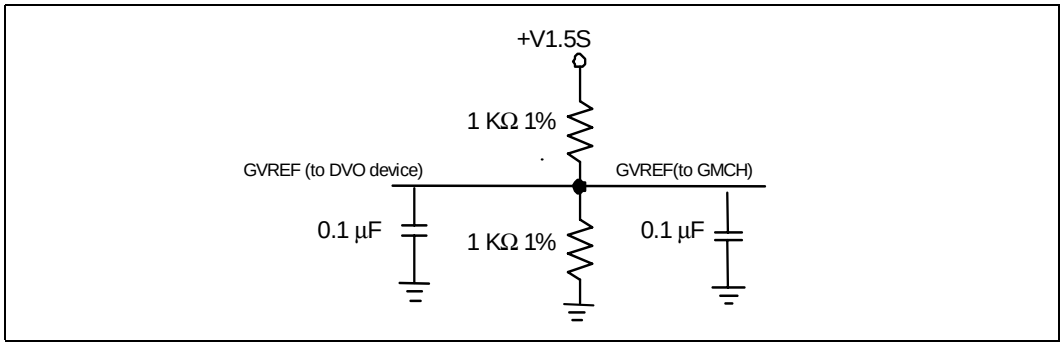
Pull-up resistors are required for the following signals if not used:

- DVOBCINTR#

6.6 Miscellaneous Input Signals and Voltage Reference

- ADDID[7]: Pull-down to ground with a 1 KΩ resistor when using the DVOB or DVOC port. This is a vBIOS strapping option to load the TPV AIM module for DVOB and DVOC port. Pull-down not required if DVOB or DVOC is not enabled.
- ADDID[6:0]: Leave unconnected (NC).
- DVODETECT: Leave unconnected (NC) when using the DVOB or DOVC port.
- DVORCOMP is used to calibrate the DVOB buffers. It shall be connected to ground via a 40.2 Ω 1 percent resistor using a routing guideline of 10 mil trace and 20 mil spacing.
- DPMS: Connects to 1.5 V version of the Intel® 6300ESB SUSCLK or a clock that runs during S1.
- GVREF: Reference voltage for the DVOB and DVOC input buffers. Refer to Figure 82 for proper signal conditioning.

Figure 82. GVREF Reference Voltage



AGP Port Design Guidelines 7

For detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms), refer to the latest AGP Interface Specification, Revision 2.0, which can be found at http://www.agpforum.org.

7.1 AGP Interface

The 855GME AGP buffers operate in only one mode: 1.5-V drive, not 3.3-V safe. This mode is compliant with the AGP 2.0 Specification.

AGP 4X, 2X and 1X must operate at 1.5 V. The AGP interface supports up to 4X AGP signaling. AGP semantic cycles to DRAM are not snooped on the host bus.

The GMCH supports PIPE# or SBA [7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA [7:0] mechanism must be selected during system initialization.

The AGP interface is clocked from a 66-MHz clock. The AGP interface is asynchronous to the host bus, system memory, and internal graphics device. When AGP interface has been enabled, the internal graphics will be disabled using GMCH strapping option. The AGP interface is synchronous to the hub interface with a clock ratio of 1:1 (66 MHz: 66 MHz).

The GMCH multiplexes the AGP signal interface with two DVO ports. These DVO ports are capable of supporting a variety of digital display devices such as TMDS transmitters and TV-Out encoders. It is possible to use the DVO ports in dual-channel mode to support higher resolutions and refresh rates (single channel mode is limited to a 165-MHz pixel clock rate).

7.1.1 AGP 2.0

The AGP Interface Specification, Revision 2.0, enhances the functionality of the original AGP Interface Specification, Revision 1.0, by allowing 4X data transfers (i.e., four data samples per clock), and 1.5-volt operation. The 4X operation of the AGP interface provides for "quad-pumping" of the AGP AD (address/data) and SBA (side-band addressing) buses. That is, data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is ¼ of a 15-ns (66-MHz) clock or 3.75 ns. It is important to understand that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, data is sampled twice during a 66-MHz clock cycle.

Therefore, the data cycle time is 7.5 ns. To allow for these high-speed data transfers, the 2X mode of AGP operation uses source-synchronous data strobing. During 4X operation, the AGP interface uses differential source-synchronous strobing.

With data cycle times as small as 3.75 ns and setup/hold times of one ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be long. If the mismatch between a data line and the associated strobe is too great, or if there is noise on the interface, incorrect data will be sampled. The low-voltage operation on AGP (1.5 V) requires even more noise immunity.

7.1.2 AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: 1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals. Each group has different routing requirements.

In addition, within the 2X/4X timing domain signals, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements, as well as trace width and spacing requirements. Because of the multiplexed AGP/DVO interface, there are trace length matching requirements within each set of 2X/4X signals, as well as between sets of 2X/4X signals. The signal groups are listed in following table.

Table 57. AGP 2.0 Signal Groups

1x Signals	2x Signals	4x Signals
CLK (3.3 V) GRBF# GWBF# GST_[2:0] GPIPE# GREQ# GGNT# GPAR GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL# GAD_[31:0] GC/BE_[3:0]# GADSTB_[1:0]	2X signals include all 1X signals and: GADSTB_[1:0] GSBSTB GAD_[31:0] signals and associated GC/BE_[3:0]# signals are running at 2X mode.	4X signals include all 1X signals and: GADSTB_[1:0] GADSTB_[1:0]# GSBSTB GSBSTB# GAD_[31:0] signals and associated GC/BE_[3:0]# signals are running at 4X mode.

Table 58. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobes in 2X	Associated Strobes in 4X
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

The routing guidelines for each group of signals (1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals) will be addressed separately.

7.2 AGP Routing Guidelines

7.2.1 1x Timing Domain Routing Guidelines

7.2.1.1 Trace Length Requirements for AGP 1X

This section contains information on the 1X timing domain routing guidelines. The AGP 1X timing domain signals (see Table 59) have a maximum trace length of 10 inches. The target impedance is 55 Ω± 15%. This maximum applies to ALL of the signals listed as 1X timing domain signals in Table 46. In addition to the maximum trace length requirement, these signals must meet the trace spacing and trace length mismatch requirements in Section 7.2.1.2 and Section 7.2.1.3.

Table 59. Layout Routing Guidelines for AGP 1X Signals

1X signals	Max. Length (inches)	Width (mils)	Space (mils)
CLK_AGP_SLT	10	4	4
AGP_PIPE#	10	4	4
AGP_RBF#	10	4	4
AGP_WBF#	10	4	4
AGP_ST[2:0]	10	4	4
AGP_FRAME#	10	4	4
AGP_IRDY#	10	4	4
AGP_TRDY#	10	4	4
AGP_STOP#	10	4	4
AGP_DEVSEL#	10	4	4
AGP_REQ#	10	4	4
AGP_GNT#	10	4	4
AGP_PAR	10	4	4

7.2.1.2 Trace Spacing Requirements

AGP 1X timing domain signals (see Table 59) can be routed with 4-mil minimum trace separation.

7.2.1.3 Trace Length Mismatch

There are no trace length mismatch requirements for 1X timing domain signals. These signals must meet minimum and maximum trace length requirements.

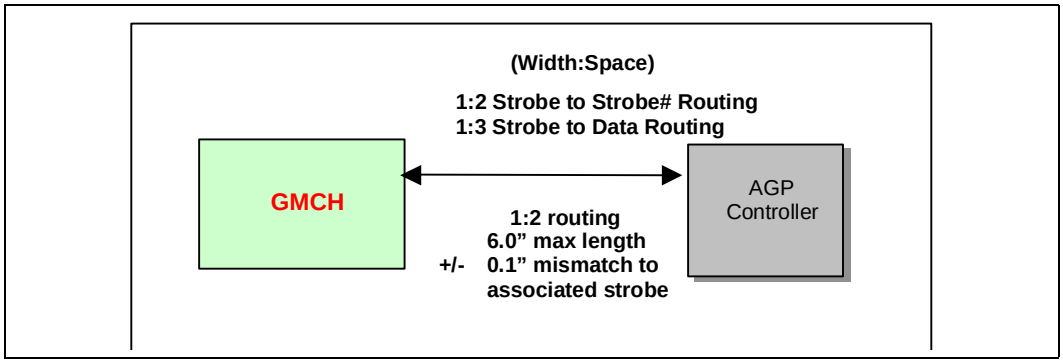
7.2.2 2x/4x Timing Domain Routing Guidelines

7.2.2.1 Trace Length Requirements for AGP 2X/4X

These trace length guidelines apply to ALL of the signals listed as 2x/4x timing domain signals in Table 60. In addition to these maximum trace length requirements, these signals must meet the trace spacing and trace length mismatch requirements in Section 7.2.1.2 and Section 7.2.1.3.

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. These routing rules are divided by trace spacing. In 1:2 spacing, the distance between the traces is two times the width of traces.

Figure 83. AGP Layout Guidelines



For 2X/4X lines in AGP interface, the max length is 6.0 inches (pin to pin) and 1:2 trace spacing is required. 2X signals must be matched to their associated strobe within 0.1 inch. 4X signals must be matched to both of their associated strobes within 0.1 inch. Reduce line length mismatch to ensure added margin.

7.2.2.2 Trace Spacing Requirements

AGP 2X/4X timing domain signals must be routed as documented in Table 57. They should be routed using 4-mil traces. Additionally, the signals can be routed with 5-mil spacing when breaking out of the GMCH. The routing must widen to the requirement in Table 59 within 0.3 inches of the GMCH package.

Since the strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source synchronous AGP interface, special care should be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 4-mil traces with 8 mils of space (1:2) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 15 mils (1:3). The strobe pair must be length matched to less than ± 0.1 inches (that is, a strobe and its compliment must be the same length within ± 0.1 inches).

Table 60. Layout Guidelines for AGP 2x/4x Signals

Signal	Maximum Length (inches)	Trace Space (mils) (4 mil traces)	Length Mismatch (inches)	Relative To	Notes
2X/4X Timing Domain Set#1	6	8	± 0.1	AGP_ADSTB0 and AGP_ADSTB0#	AGP_ADSTB0, AGP_ADSTB0# must be the same length (±10 mils)
2X/4X Timing Domain Set#2	6	8	± 0.1	AGP_ADSTB1 and AGP_ADSTB1#	AGP_ADSTB1, AGP_ADSTB1# must be the same length (±10 mils)
2X/4X Timing Domain Set#3	6	8	± 0.1	AGP_SBSTB and AGP_SBSTB #	AGP_SBSTB, AGP_SBSTB# must be the same length (±10 mils)

7.2.2.3 Trace Length Mismatch Requirements

Table 61. AGP 2.0 Data Lengths Relative to Strobe Length

Max Trace Length	Trace Spacing	Strobe Length	Min Trace Length	Max Trace Length
< 6 in	1:2	X	X - 0.1 in	X + 0.1 in

The trace length minimum and maximum (relative to strobe length) should be applied to each set of 2X/4X timing domain signals independently. If AD_STB0 is 5 inches and ADSTB0# is 5.01 inches, then AD[15:0] and C/BE[1:0] must be between 4.91 inches and 5.1 inches. However, AD_STB1 and ADSTB1# can be 3.5 inches and 3.51 inches (and therefore AD[31:16] and C/BE#[3:2] must be between 3.41 inches and 3.6 inches). In addition, all 2X/4X timing domain signals must meet the maximum trace length requirements.

- All signals should be routed as strip lines (inner layers).
- All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements must not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to 0 inches as possible to provide optimal timing margin.

The strobe pair must be length matched to less than ± 0.01 inches (that is, a strobe and its compliment must be the same length within ± 0.01 inches).

Table 62 shows the AGP 2.0 routing summary.

Table 62. AGP 2.0 Routing Guideline Summary

Signal	Maximum Length	Trace Spacing (4 mil traces)	Length Mismatch	Relative To	Notes
1X Timing Domain	10 in	4 mils	No Requirement	N/A	None
2X/4X Timing Domain Set#1	6 in	8 mils	± 0.1 in	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	6 in	8 mils	± 0.1 in	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	6 in	8 mils	± 0.1 in	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length

7.2.3 AGP Clock Skew

The maximum total AGP clock skew between the GMCH and the graphics component is 1 ns for all data transfer modes. This 1 ns includes skew and jitter, which originates on the motherboard, add-in module (if used), and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but also at all points on the clock edge that falls in the switching range. The 1 ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew (the motherboard designer shall determine how the 0.9 ns is allocated between the board and the synthesizer).

7.2.4 AGP Signal Noise Decoupling Guidelines

The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the Intel chipset GMCH. The following guidelines are not intended to replace thorough system validation on Intel chipset-based products.

- A minimum of six 0.01-µF capacitors are required and must be as close as possible to the GMCH. These should be placed within 70 mils of the outer row of balls on the GMCH for VDDQ decoupling. Ideally, this should be as close as possible.
- The designer should evenly distribute placement of decoupling capacitors in the AGP interface signal field.
- Intel recommends that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.
- To add the decoupling capacitors within 70 mils of the GMCH and/or close to the vias, trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1.0 inch max.).

In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. One extra 0.01 uF capacitor per 10 vias is required. The capacitor should be placed as close as possible to the center of the via field.

7.2.5 AGP Interface Package Lengths

Table 63. AGP Interface Package Lengths (Sheet 1 of 2)

Signal	Pin Number	Package Length (mils)
GAD0	T6	339
GAD1	T5	362
GAD2	R5	440
GAD3	R3	489
GAD4	R4	415
GAD5	R6	343
GAD6	P5	387
GAD7	P6	409
GAD8	N5	466
GAD9	N3	504
GAD10	N2	568
GAD11	M5	510
GAD12	M1	611
GAD13	M3	520
GAD14	M2	566
GAD15	T7	296
GAD16	L5	440
GAD17	K6	491

Signal	Pin Number	Package Length (mils)
GADSTB_0	P3	475
GADSTBB_0	P4	439
GADSTB_1	J3	601
GADSTBB_1	J2	675
GSBA_0	E5	686
GSBA_1	F5	617
GSBA_2	E3	738
GSBA_3	E2	865
GSBA_4	G5	668
GSBA_5	F4	688
GSBA_6	G6	518
GSBA_7	F6	613
GSBSTB	F2	799
GSBSTBB	F3	761
GPIPEB	D5	644
GCBEB_0	P2	553
GCBEB_1	L2	583
GCBEB_2	L4	515

Table 63. AGP Interface Package Lengths (Sheet 2 of 2)

Signal	Pin Number	Package Length (mils)
GAD18	L3	541
GAD19	K5	489
GAD20	K1	692
GAD21	K3	622
GAD22	K2	685
GAD23	J6	536
GAD24	H1	772
GAD25	H2	720
GAD26	H4	625
GAD27	H3	649
GAD28	G3	762
GAD29	H6	521
GAD30	G2	712
GAD31	H5	566

Signal	Pin Number	Package Length (mils)
GCBEB_3	J5	518
GST_0	C4	750
GST_1	C3	797
GST_2	C2	856
GRBFB	D3	962
GWBFB	D2	947
GFRAMEB	M6	486
GIRDYB	K7	751
GTRDYB	N7	350
GSTOPB	P7	423
GDEVSELB	N6	399
GREQB	B3	762
GGNTB	B2	849
GPAR	L7	623

7.2.6 AGP Routing Ground Reference

Intel strongly recommends that at least the following critical signals be referenced to ground from the GMCH to an AGP controller connector using a minimum number of vias on each net:

- AD_STB0
- AD_STB0#
- AD_STB1
- AD_STB1#
- SB_STB
- SB_STB#
- G_TRDY#
- G_IRDY#
- G_GNT#
- ST[2:0]

7.2.7 Pull-Ups

The AGP 2.0 Specification requires AGP control signals to have pull-up resistors to VDDQ to ensure they contain stable values when no agent is actively driving the bus. Also, the AD_STB[1:0]# and ST_STB# strobes require pull-down resistors to GND. The Intel 855GME chipset GMCH has integrated many of these pull-up/pull-down resistors on the AGP interface and a few other signals not required by the AGP 2.0 Specification. Pull-ups are allowed on any signal except AD_STB[1:0]# and SB_STB#.

The Intel chipset GMCH has no support for the PERR# and SERR# pins of an AGP graphics controller that supports PERR# and SERR#. Pull-ups to a 1.5-V source are required down on the motherboard in such cases.

Table 64. AGP Pull-Up/Pull-Down Requirements and Straps

Signal	AGP 2.0 Signal Pull-Up/ Pull-Down Requirements	GMCH Integrated Pull-Up/ Pull-Down	Notes
DEVSEL#		Pull-Up	
FRAME#		Pull-Up	
GNT#		Pull-Up	
INTA#	Pull-Up		3, 5
INTB#	Pull-Up		3, 5
IRDY#		Pull-Up	
PERR#	Pull-Up		2
PIPE#		Pull-Up	
RBF#		Pull-Up	
REQ#		Pull-Up	1
SERR#	Pull-Up		2
ST[2:0]		Pull-Down	4
STOP#	Pull-Up	Pull-Up	
TRDY#		Pull-Up	
WBF#		Pull-Up	
AD_STB[1:0]		Pull-Up	
AD_STB[1:0]#		Pull-Down	
SB_STB		Pull-Up	
SB_STB#		Pull-Down	
SBA[7:0]		Pull-Up	1

NOTES:
1. The Intel chipset GMCH has integrated pull-ups to ensure that these signals do not float when there is no add-in card in the connector.
2. The Intel chipset GMCH does not implement the PERR# and SERR# signals. Pull-ups on the motherboard are required for AGP graphics controllers that implement these signals.
3. The Intel chipset GMCH does not implement interrupt signals. AGP graphics controller's INTA# and INTB# signals must but routed to the system PCI interrupt request handler where the pull-up requirement should be met as well. For 855GME/ICH4 chipset-based systems, they can be routed to the ICH4's PIRQ signals that are open drain and require pull-ups on the motherboard.
4. ST[1:0] provide the strapping options for 100-MHz PSB operation and DDR memory, respectively.
5. INTA# and INTB# should be pulled to 3.3 V, not VDDQ.
6. The pull-up/pull-down resistor value requirements are shown in Table 65.

Table 65. AGP 2.0 Pull-up Resistor Values

Rmin	Rmax
4 kΩ	16 kΩ

The recommended AGP pull-up/pull-down resistor value is 8.2 kΩ.

7.2.8 AGP VDDQ and VCC

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller and VDDQ is the interface voltage.

7.2.9 VREF Generation for AGP 2.0 (2X and 4X)

7.2.9.1 1.5 V AGP Interface (2X/4X)

The voltage divider networks consist of AC and DC elements. The reference voltage that should be supplied to the Vref pins of the GMCH and the graphics controller is ½ * VDDQ. Two 1 kΩ ± 1% resistors can be used to divide VDDQ down to the necessary voltage level.

The Vref divider network should be placed as close to the AGP interface as is practical to get the benefit of the common mode power supply effects. However, the trace spacing around the Vref signals must be a minimum of 25 mils to reduce crosstalk and maintain signal integrity.

7.2.10 AGP Compensation

The 855GME chipset GMCH AGP interface supports resistive buffer compensation. For PCBs with characteristic impedance of 55 Ω, tie the GRCOMP pin to a 40.2 Ω ± 1% pull-down resistor (to ground) via a 10-mil wide, very short (≈ 0.5 inches) trace.

AGP Link:

http://www.intel.com/technology/agp/info.htm

AGP StressTool Link:

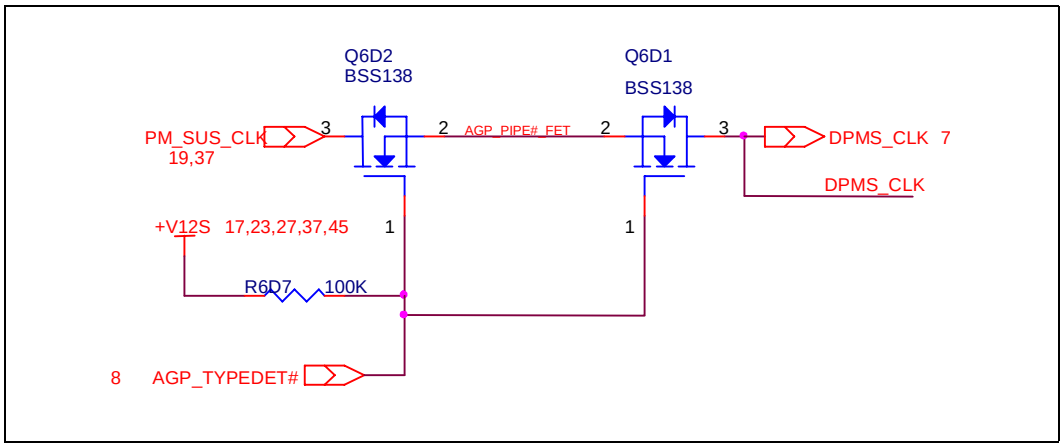
http://www.intel.com/technology/agp/downloads/agp_stress.htm

7.2.11 PM_SUS_CLK/AGP_PIPE# Design Consideration

The following design consideration provides the option to support both AGP and DVO devices with one ADD Connector. Refer to Figure 84 and customer reference schematics for more detail.

The GMCH expects either the PM_SUS_CLK signal from the ADD connector when there is a no AGP device or the AGP_PIPE# signal when there is an AGP device. The AGP_TYPEDET# signal is driven high when no AGP card is detected, allowing DPMS_CLK to be driven by PM_SUS_CLK. In the case where an AGP card is detected, AGP_TYPE# signal goes high which allows DMPS_CLK to be driven by AGP_PIPE#.

Figure 84. DPMS Circuit



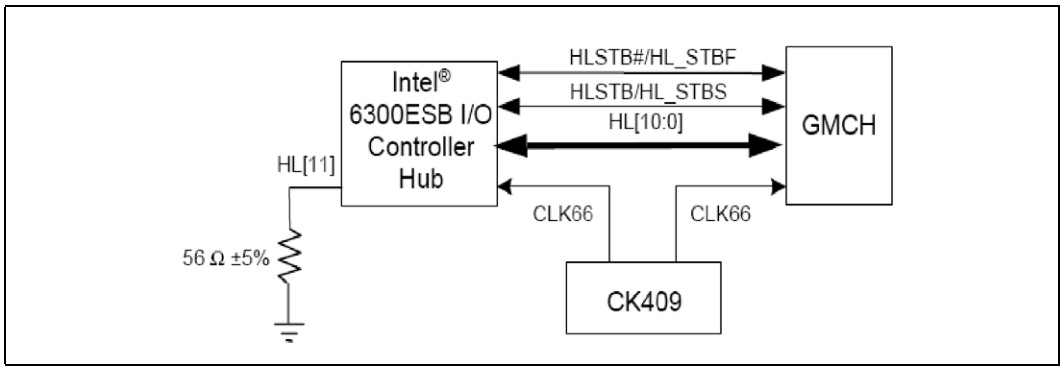
Hub Interface 8

The GMCH and 6300ESB ballout assignments have been optimized to simplify the Hub Interface routing between these devices. It is recommended that the Hub Interface signals be routed directly from the GMCH to the 6300ESB with all signals referenced to V_{SS}. Layer transition should be keep to a minimum. When a layer change is required, use only two vias per net and keep all data signals and associated strobe signal on the same layer.

The Hub Interface signals are broken into two groups: data signals (HI) and strobe signals (HI_STB). For the 8-bit Hub Interface, HI[11:0] are associated with HI_STB/HI_STBS and HI_STB#/HI_STBF.

Note: These routing guidelines are created using the stack-up described in Figure 2, "Recommended Board Stack-up Dimensions" on page 34.

Figure 85. 8-Bit Hub Interface Routing Example



8.1 8-Bit Hub Interface Routing Guidelines.

8.1.1 8-Bit Hub Interface Data Signals

The 8-bit Hub Interface data signal traces (HI[11:0]) should be routed through stripline or microstrip routing with 5 mil width and 15 mil spacing. (See Table 66.) These signals may be routed 5 mil width and 5 mil spacing for navigation around components, mounting holes or in order to break out of the GMCH and the 6300ESB package. The signals must be separated no longer than 300 mils from the package.

Table 66. Hub Interface 1.5 Data Signals Routing Summary

Digital Signal Requirement	Maximum Trace Length	Referencing	Data Signal Length Matching
5 mil width, 15 mil spacing	8 inches	Ground	Each strobe signal must be the same length, and each data signal must be matched within ± 0.25 inches of the strobe signals.

8.1.2 8-Bit Hub Interface Signal Referencing

The 8-bit Hub Interface data signal traces (HI[11:0]) and the two Hub Interface strobe signals (HI_STB/HI_STBS and HI_STB#/HI_STBF) must all be referenced to ground to insure proper noise immunity.

8.1.3 8-Bit Hub Interface Strobe Signals

The Hub Interface strobe signals should be routed 5 mil width, 15 mil spacing. (See Table 67.) This strobe pair should have a minimum of 20 mils spacing from any adjacent signals.

Table 67. Hub Interface 1.5 Strobe Signals Routing Summary

Strobe Signal Requirements	Maximum Trace Length	Referencing	Strobe Signal Length Matching
5 mil width, 20 mil spacing (from other signals), 15 mil spacing (intra-pair)	8 inches	Ground	Each strobe signal must be the same length, and each data signal must be matched within ± 0.25 inches of the strobe signal.

8.1.4 8-bit Hub Interface HIREF and HI_VSWING Generation/ Distribution

HIREF is the Hub Interface reference voltage. The 6300ESB uses HI_VSWING to control voltage swing and impedance strength of the Hub Interface buffers. The HIREF and HI_VSWING voltage requirement and associated resistor recommendations for the voltage divider circuit are listed in Table 68. Four options are given for the divider circuit, choose the one that best supports your platform.

Table 68. 8-Bit Hub Interface HIREF/HI_VSWING Generation Circuit Specifications

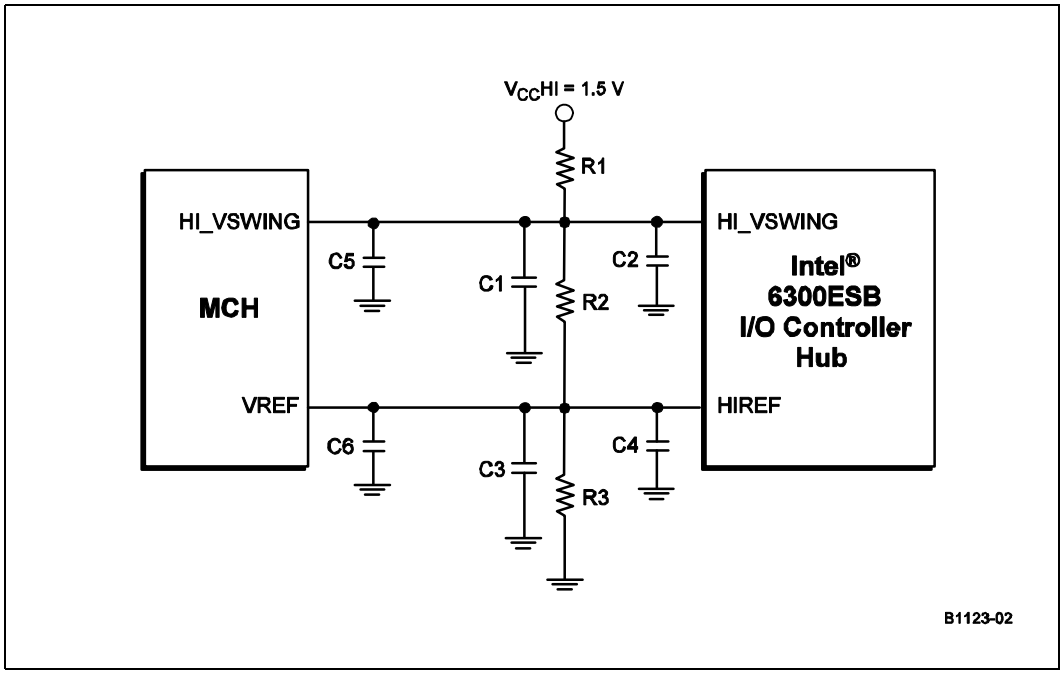
HIREF Voltage Specification (V)	HI_VSWING Voltage Specification (V)	Recommended Values for the HIREF/ HI_VSWING Divider Circuit (Ω)
350 mV ± 2%	800 mV ± 2%	Option A (Figure 86& Figure 87) R1 = 226 Ω ± 1%, R2 = 147 Ω ± 1%, R3 = 113 Ω ± 1% Option B (Figure 86& Figure 87) R1 = 80.6 Ω ± 1%, R2 = 51.1 Ω ± 1%, R3 = 40.2 Ω ± 1% Option C (Figure 86& Figure 87) R1 = 255 Ω ± 1%, R2 = 162 Ω ± 1%, R3 = 127 Ω ± 1% Option D (Figure 88& Figure 89) R4 = 78.7 Ω ± 1%, R5 = 24.2 Ω ± 1%, R6 = 43.2 Ω ± 1%, R7 = 49.9 Ω ± 1%

NOTES: Capacitance Values For All Options
7. C1 and C3 = 0.1 µF (near divider)
8. C2, C4, C5, C6 = 0.01 µF (near GMCHGMCH and 6300ESB)
9. The resistor values R1, R2, R3, R4, R5, R6, and R7 must be rated at 1% tolerance.

Note: HIREF and HI_VSWING is derived from 1.5 V which is the nominal core voltage for the 6300ESB. Voltage supply tolerance for driver voltage must be within a ± 5% range of nominal.

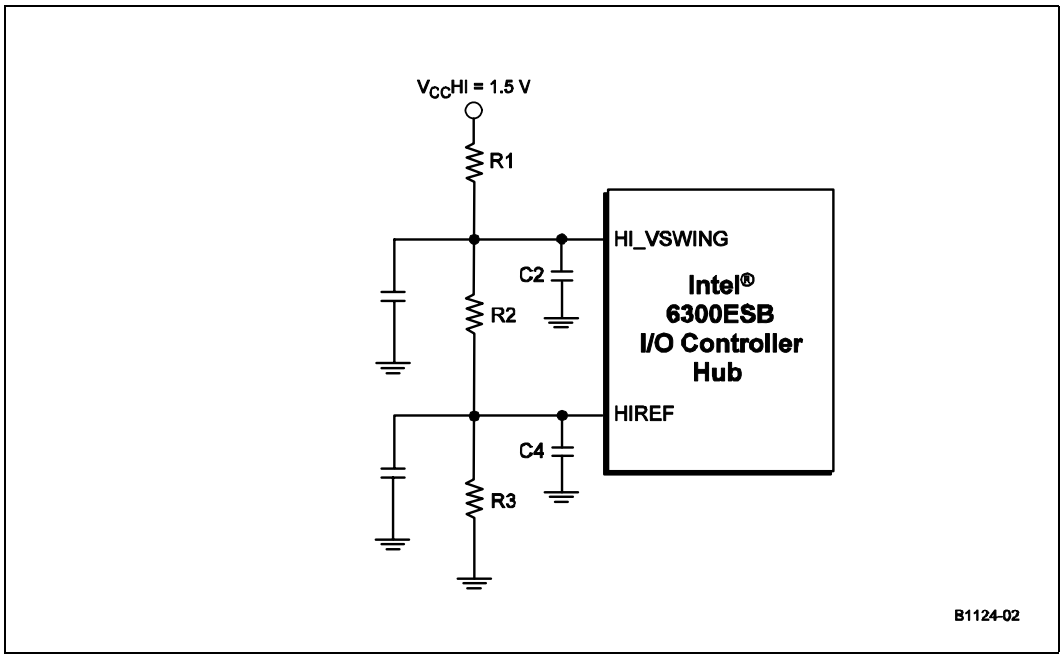
The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. The maximum distance from divider to device is four inches (less is better). Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). When the single HIREF/HI_VSWING divider circuit is located more than four inches away, then the locally generated reference divider should be used. Below are four examples of the HIREF/HI_VSWING divider circuit.

Figure 86. 8-Bit Hub Interface Single HIREF/HI_VSWING Generation Circuit Option A



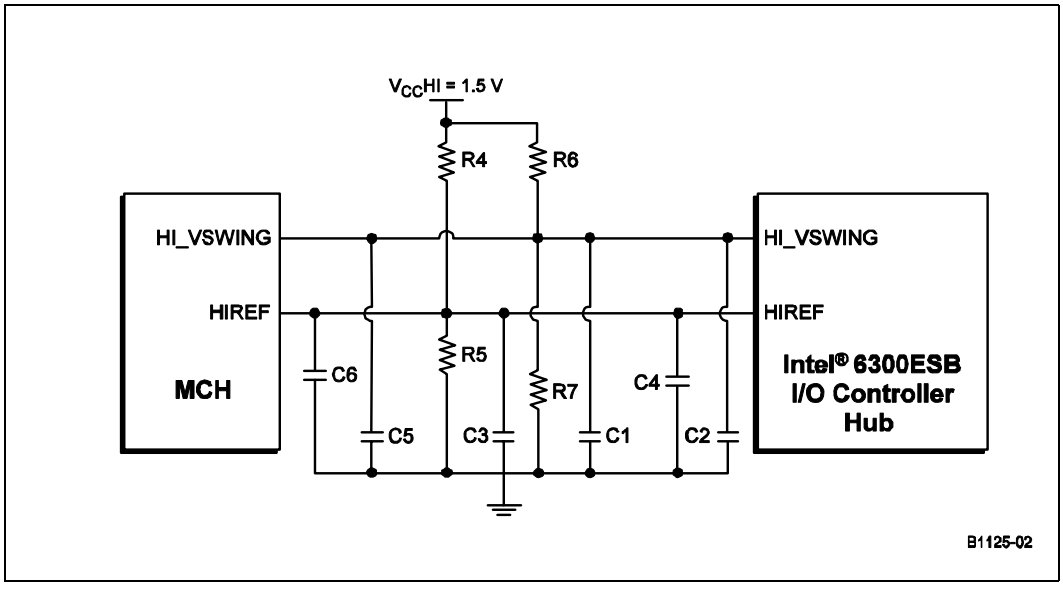
1. Two 0.1 µF capacitors (C1 and C3) should be placed close to the divider.
2. Each 0.01 µF bypass capacitor (C2, C4, C5, and C6) should be placed within 0.25 inches of HIREF/VREF pin (for C4 and C6) and HI_VSWING pin (for C2 and C5).

Figure 87. 8-Bit Hub Interface Local HIREF/HI_VSWING Generation Circuit Option B



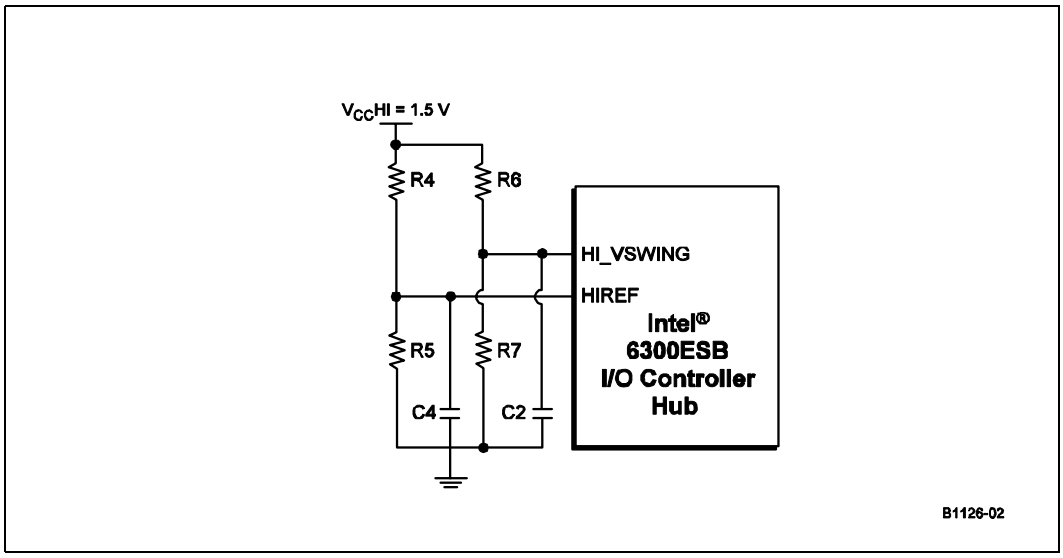
1. Each 0.01 µF bypass capacitor should be placed within 0.25 inches of HIREF/VREF pin (C4) and HI_VSWING pin (C2).

Figure 88. 8-Bit Hub Interface Single HIREF/HI_VSWING Generation Circuit Option C



1. Two 0.1 µF capacitors (C1 and C3) should be placed close to the divider.
2. Each 0.01 µF bypass capacitor (C2, C4, C5, and C6) should be placed within 0.25 inches of HIREF/VREF pin (for C4 and C6) and HI_VSWING pin (for C2 and C5)

Figure 89. 8-Bit Hub Interface Local HIREF/HI_VSWING Generation Circuit Option D



1. Each 0.01 µF bypass capacitor should be placed within 0.25 inches of HIREF/VREF pin (C4) and HI_VSWING pin (C2).

8.1.4.1 GMCH Single Generated Voltage Reference Divider Circuit

This option allows the GMCH to use one voltage divider circuit to generate both HLVREF and HLPSWING voltage references. The reference voltage for both HLVREF and HLPSWING must meet the voltage specification in Table 68. The resistor values R1, R2, and R3 must be rated at 1 percent tolerance (see Table 69). Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). When the voltage specifications are not met, individually generated voltage divider circuits for HLVREF and PSWING are required. Refer to Section 8.1.4.2 for more details. Figure 90 depicts the GMCH locally generated reference voltage divider circuit.

Figure 90. GMCH Locally Generated Reference Voltage Divider Circuit

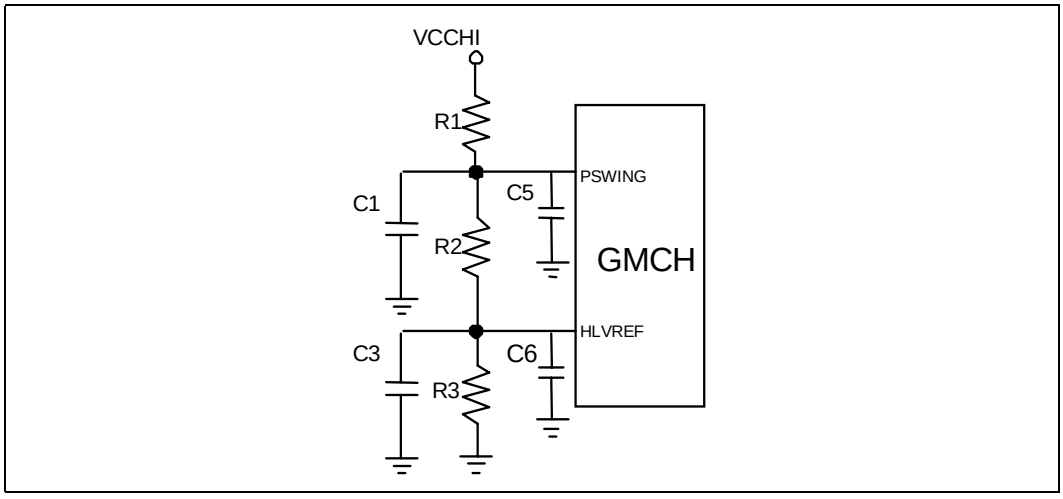


Table 69. Recommended Resistor Values for Single VREF/VSWING Divider Circuit

	Recommended Resistor Values			VCCHI
Option 1	R1 = 80.6 Ω ± 1%	R2 = 51.1 Ω ±1%	R3 = 40.2 Ω ±1%	1.5 V
Option 2	R1 = 255 Ω ± 1%	R2 = 162 Ω ±1%	R3 = 127 Ω ±1%	1.5 V
Option 3	R1 = 226 Ω ± 1%	R2 = 147 Ω ±1%	R3 = 113 Ω ±1%	1.5 V
	C1 and C3 = 0.1 µF (near divider) C5, C6 = 0.01 µF (near component)			

8.1.4.2 Separate GMCH Voltage Divider Circuits for HLVREF and PSWING

This option allows for tuning the voltage references HLVREF and PSWING individually. The reference voltage for both HLVREF and PSWING must meet the voltage specification in Table 70. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). Figure 91 depicts the individual HLVREF and PSWING voltage reference divider circuits for GMCH. Table 70 presents the recommended resistor values for HLVREF and PSWING divider circuits for GMCH.

Figure 91. Individual HLVREF and PSWING Voltage Reference Divider Circuits for GMCH

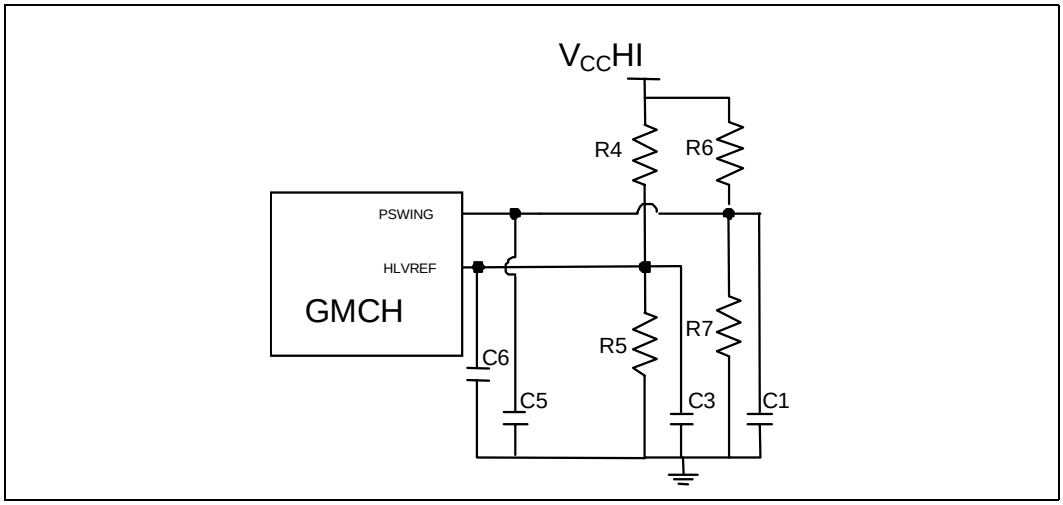


Table 70. Recommended Resistor Values for HLVREF and PSWING Divider Circuits for GMCH

Signal Name	Recommended Resistor Values	VCCHI	Capacitor
HLVREF (350 mV)	R4 = 287 Ω ±1% R5 = 100 Ω ±1%	VCCHI=1.35 V	C3 = 0.1 µF (near divider); C6 = 0.01 µF (near component)
PSWING (800 mV)	R6 = 68.1 Ω ±1% R7 = 100 Ω ±1%	VCCHI=1.35 V	C1 = 0.1 µF (near divider) C5 = 0.01 µF (near component)

8.1.5 Hub Interface Compensation

This section documents the routing guidelines for the 8-bit Hub Interface using enhanced (parallel) termination (the method of termination is dependant upon the Northbridge). This Hub Interface connects the Intel® 855GME chipset Graphics Memory Controller Hub (82855GME) to the 6300ESB. As shown in Table 71, the 6300ESB shall strap its HLRCOMP pin to $V_{CC}HI$ = 1.5 V and the GMCH shall strap its HLRCOMP pin to $V_{CC}HL$ =1.35 V. The trace impedance must equal 55 Ω ± 15 percent.

Table 71. Hub Interface RCOMP Resistor Values

Component	Trace Impedance	HLRCOMP Resistor Value	HLRCOMP Resistor Tied to
6300ESB	55 Ω ± 15%	48.1 Ω ± 1%	Vcc1_5
GMCH	55 Ω ± 15%	37.4 Ω ± 1%	Vcc1_35

8.1.6 8-Bit Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1 µF capacitors per each component (i.e., the 6300ESB and GMCH). These capacitors should be placed within 50 mils from each package, adjacent to the rows that contain the Hub Interface. When the layout allows, wide metal fingers running on the V_{SS} side of the board should connect the $V_{CC}HI$=1.5 V side of the capacitors to the $V_{CC}HI$=1.5 V power pins. Similarly, when the layout allows, metal fingers running on the $V_{CC}HI$=1.5 V side of the board should connect the ground side of the capacitors to the V_{SS} power pins.

8.1.7 Terminating HI_11 If Not Used

The HL[11] signal exists on the 6300ESB but not the GMCH and is not used on the platform. HL[11] must be pulled down to ground via a 56 Ω resistor.

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9.1 Serial ATA Interface

9.1.1 Layout Guidelines

Note: These routing guidelines are created using the stack-ups described in Section 3.1, "Nominal Board Stack-Up" on page 33.

9.1.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design.

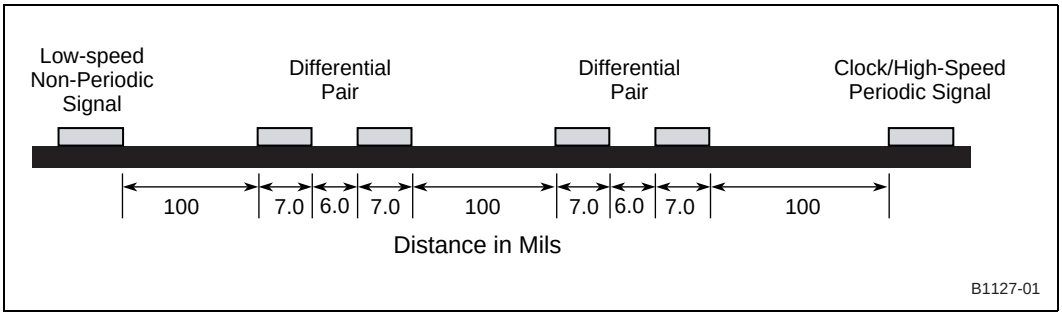
4. Serial ATA signals must be have *consistent plane* r*eferencing* maintained for the entire path between driver and receiver. Signals routed on microstrip may be referenced to either power or ground but not both. Stripline signals should be surrounded by power planes (Vcc or GND) and shall be maintained consistent along the entire transmission path.
5. Route all traces using microstrip over continuous planes (Vcc or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane may cause signal reflections and should be avoided.
6. No layer changes or vias other than the package ball shall be allowed.
7. Do not route SATA traces around or under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
8. No 90 degree bends or stubs.
9. The allowable breakout region is 500 mils from the package.
10. Do not route SATA traces through connectors or any other obstruction that would require a deviation in the intra-pair spacing and thus, differential impedance. The exception is the breakout region from the pin whose length should be minimized to reduce reflections.

9.1.1.2 Serial ATA Trace Separation

Use the following separation guidelines. Figure 92 provides an illustration of the recommended trace spacing.

1. Maintain parallelism and consistent trace spacing between SATA differential signals with the trace spacing needed to achieve 79.3 Ω ± 10% differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Ensure that the amount and length of the deviations are kept to the minimum possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used; keeping in mind that the target is a 79.3 Ω ± 10% differential impedance. For the board stackup parameters referred to in Section 3.1, "Nominal Board Stack-Up" on page 33, 7.0 mil traces with 6.0 mil spacing results in approximately 79.3 Ω ± 10% differential trace impedance.
3. Based on simulation data, use 100 mil minimum spacing between 6300ESB Serial ATA signal pairs and other signal traces for optimal signal quality. This helps to reduce crosstalk.

Figure 92. Serial ATA Trace Spacing Recommendation



9.1.1.3 Serial ATA Trace Length Pair Matching

Serial ATA signal pair traces should be trace length matched. The difference of two line traces in a differential pair should be restricted to below 10 mils.

9.1.1.4 Serial ATA Trace Length Guidelines

The length of the differential pairs (i.e., Tx pair and Rx pair) should be designed to within the recommend values. The recommended length of the trace is from two to eight inches. When the trace length of the differential pair is longer than recommended, the high-frequency differential signal suffers significant signal attenuation and an increase in inter-symbol interference.

Table 72. SATA Routing Summary

Differential Trace Impedance	SATA Routing Requirements	Trace Length	SATA Signal Length Matching
79.3 Ω ± 15%	7 mil width, 6 mil spacing (Based on stackup described in Section 3.1.)	2-8 inches	Length mismatch between signals in a data pair should be no more 10 mils.

9.1.1.5 SATA BIAS Connections

It is recommended that the SATARBIASP and the SATARBIASN pins be shorted at the package and the routed to one end of a 24.9 Ω ± 1% resistor to ground. Place the resistor within 500 mils of the 6300ESB and avoid routing next to clock pins.

Figure 93. SATA BIAS Connections

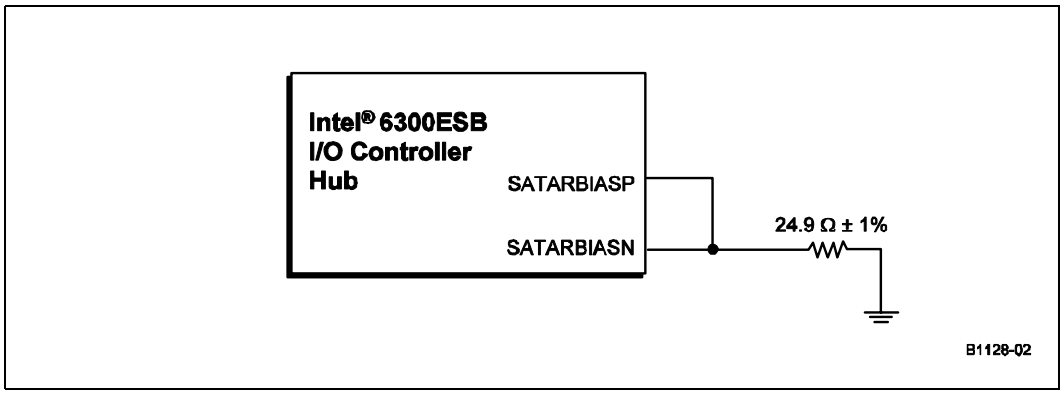


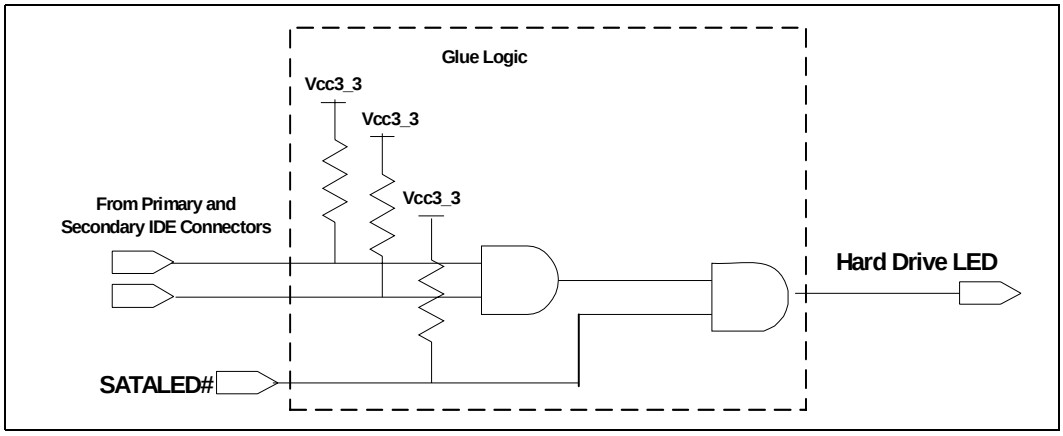
Table 73. SATA BIAS Routing Summary

Trace Impedance	SATARBIASP/SATARBIASN Routing Requirements	Maximum Trace Length
55 Ω ± 10%	5 mil width, 5 mil spacing	500 mils

9.1.1.6 SATALED# Implementation

The 6300ESB provides a signal (SATALED#) to indicate SATA device activity. In order for this signal to work in conjunction with Parallel ATA hard drives, Intel recommends implementing the glue logic shown in Figure 94.

Figure 94. SATALED# Circuitry Example



This signal is open-drain and requires an weak external pull-up to Vcc3.3. When low, SATALED# indicates SATA device activity and should activate the hard drive LED. When tri-stated, the signal will not activate the LED.

Note: Ensure that all connectors and cables comply with the *SATA Gold Specification, Revision 1.0,* dated August 29, 2001 or later.

9.2 IDE Interface

Note: These routing guidelines are created using the stack-up described in Section 3.1, "Nominal Board Stack-Up" on page 33.

This section contains guidelines for connecting and routing the 6300ESB IDE interface. The 6300ESB has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The 6300ESB has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0 Ω resistors may be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date. When used, place these resistors close to the connector.

Table 74. IDE Signal Groups

Signal Group	Primary	Secondary
Data	PDD[15:0]	SDD[15:0]
Strobes	PDIOR# (write) PDIORDY (read)	SDIOR# (write) SDIORDY (read)

The IDE interface must be routed with 5 mil width traces, 7 mil spacing (dependent upon stackup parameters), and must be less than eight inches long (from 6300ESB to IDE connector). See Table 75 below for routing summary.

Note: A max of two layer transitions are allowed. All transitions must be routed within 1.5 inches from the 6300ESB pin. After the 1.5 inch layer transition boundary, all strobe and data signals must be routed on the same layer. No layer transitions are allowed at the IDE connector.

Table 75. IDE Routing Summary

Trace Impedance	IDE Routing Requirements	Maximum Trace Length	IDE Signal Length Matching
55 Ω ± 10%	5 mil width, 7 mil spacing (based on stackup assumptions in Section 3.1)	8 inches	The two strobe signals must be matched within 100 mils of each other. The data lines must be within ± 500 mils of the average length of the two strobe signals.

9.2.1 Cabling

Length of cable: Each IDE cable must be equal to 18 inches.

Capacitance: Less than 35 pF.

Placement: A maximum of six inches between drive connectors on the cable. When a single drive is placed on the cable, it should be placed at the end of the cable. When a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (six inches away from the end of the cable).

Grounding: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

9.3 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The 6300ESB IDE Controller supports PIO, Multi-word (8237 style) DMA, and Ultra DMA modes 0 through 5, and Native Mode IDE. Please note that there are no motherboard hardware requirements for supporting Native Mode IDE. Native Mode IDE is supported through the operating system and system drivers. The 6300ESB needs to determine the type of cable that is present, in order to configure itself for the fastest possible transfer mode that the hardware may support.

An 80-conductor IDE cable is required for Ultra DMA modes greater than two (Ultra ATA/33). This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the *Small Form Factor Specification SFF-8049*. This specification may be obtained from the Small Form Factor Committee.

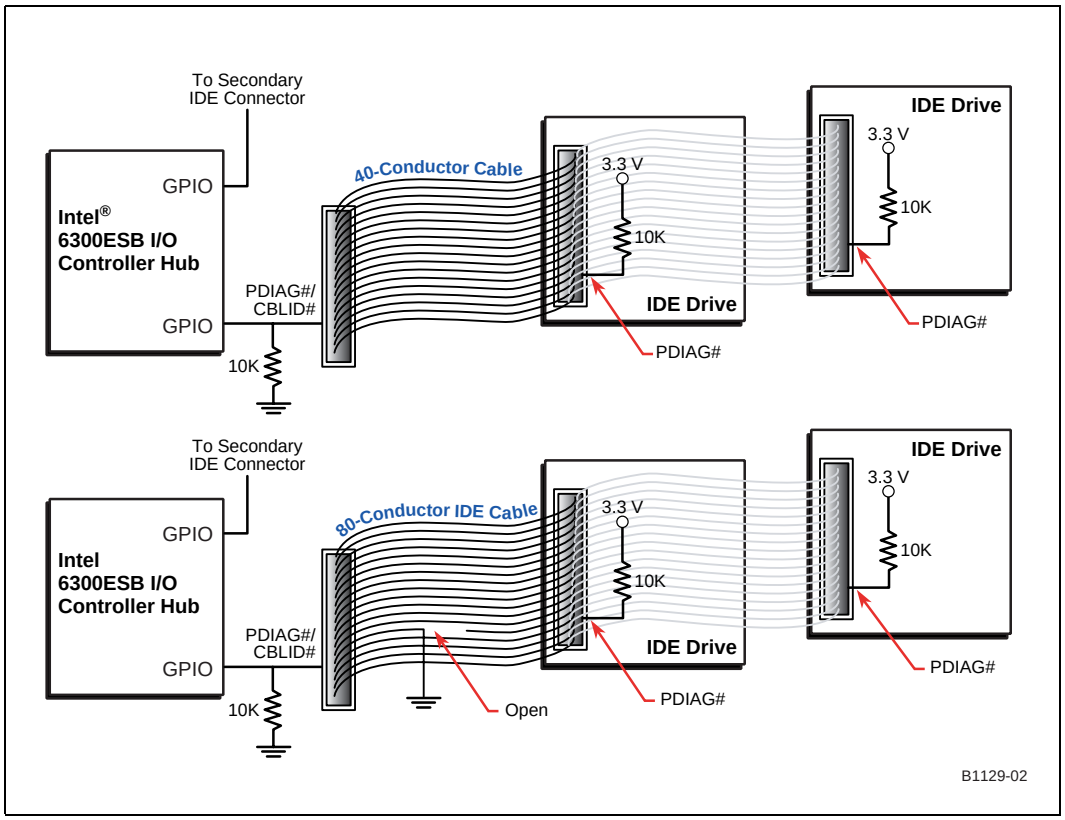
To determine when Ultra DMA modes greater than two (Ultra ATA/33) may be enabled, the 6300ESB requires the system software to attempt to determine the cable type used in the system. When the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. When a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be performed using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system, since this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side Detection mechanism only.

9.3.1 Combination Host-Side/Device-Side Cable Detection

Host-side detection (described in the *ATA/ATAPI-6 Standard*) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 95. All IDE devices have a 10 KΩ pull-up resistor to 5 V on this signal. A 10 KΩ pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present and allows for use of a non-5 V tolerant GPIO.

Figure 95. Combination Host-Side/Device-Side IDE Cable Detection



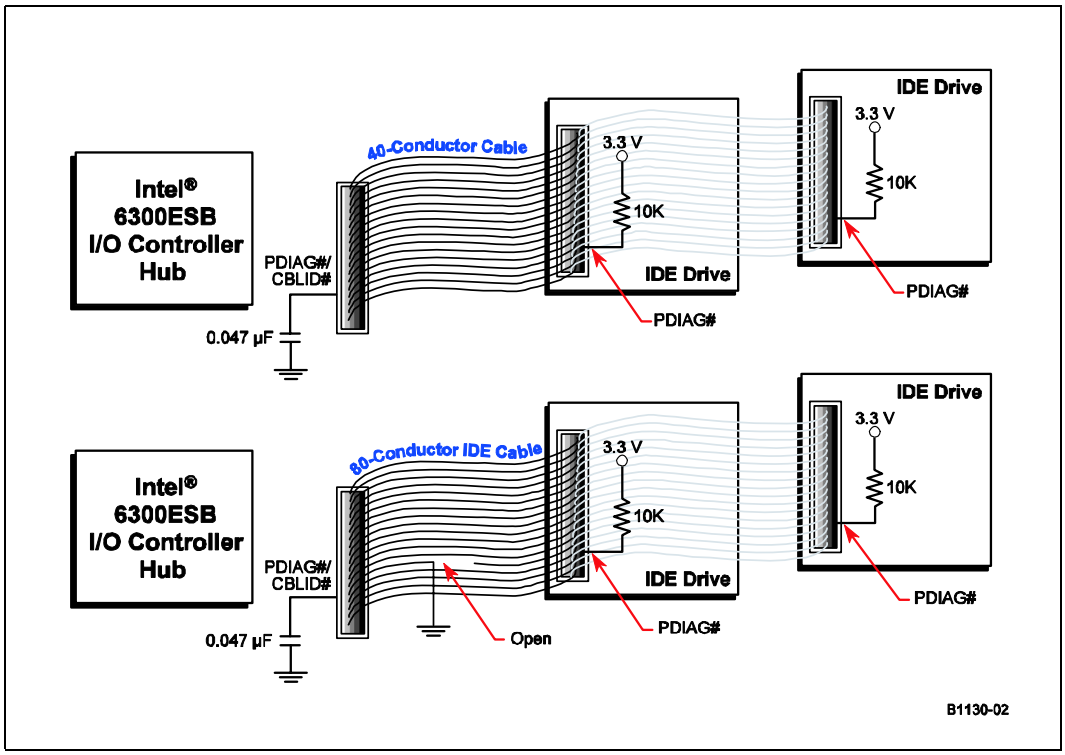
This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. When the signal is high, there is 40-conductor cable in the system and Ultra DMA modes greater than two (Ultra ATA/33) must not be enabled.

When PDIAG#/CBLID# is detected low, there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the *ATA/ATAPI-6 standard*. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than two. When ID Word 93, bit 13 is a one, an 80-conductor cable is present. When this bit is zero, a legacy slave (Device 1) is preventing proper cable detection and BIOS should configure the system as though a 40-conductor cable is present, and notify the user of the problem.

9.3.2 Device-Side Cable Detection

For platforms that must implement Device-Side detection only (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in Figure 96. This capacitor should not be populated when implementing the recommended combination Host-Side/Device-Side cable detection mechanism described above. Please note some drives may not support device-side cable detection.

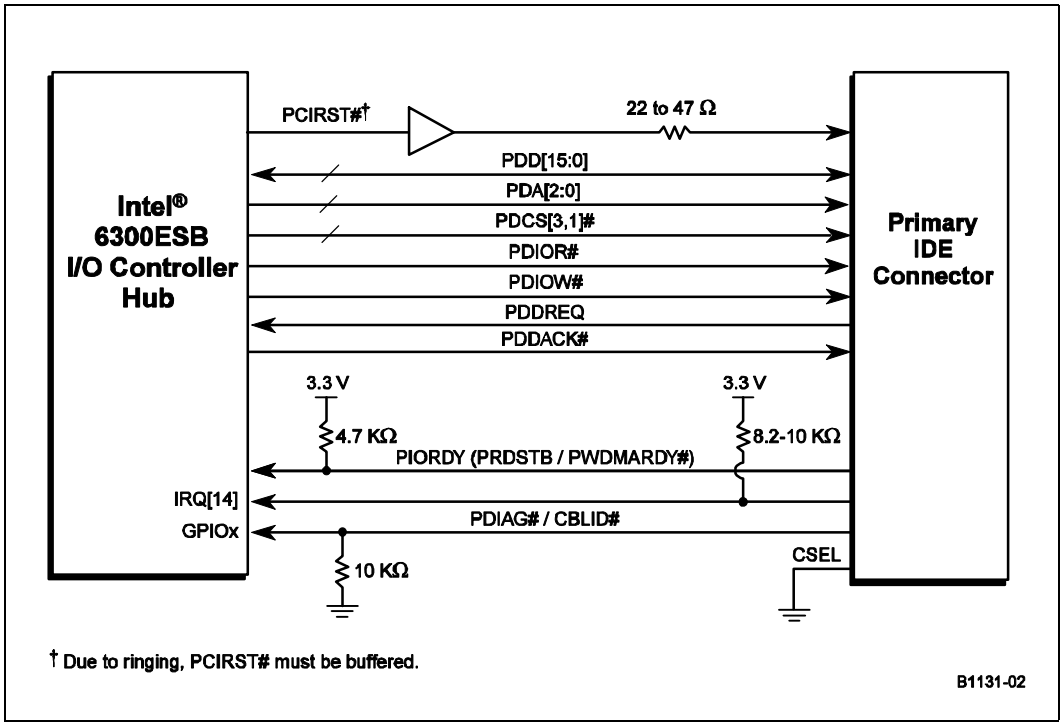
Figure 96. Device Side IDE Cable Detection



This mechanism creates a resistor-capacitor (RC) time constant. Hard drives supporting Ultra DMA modes greater than two (Ultra DMA/33) drive PDIAG#/CBLID# low and then release it (pulled up through a 10 KΩ resistor). The drive samples the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host and therefore the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host. Therefore, the signal rises slower as the capacitor charges. The drive may detect the difference in rise times and it reports the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the *ATA/ATAPI-6 Standard*.

9.3.3 Primary IDE Connector Requirements

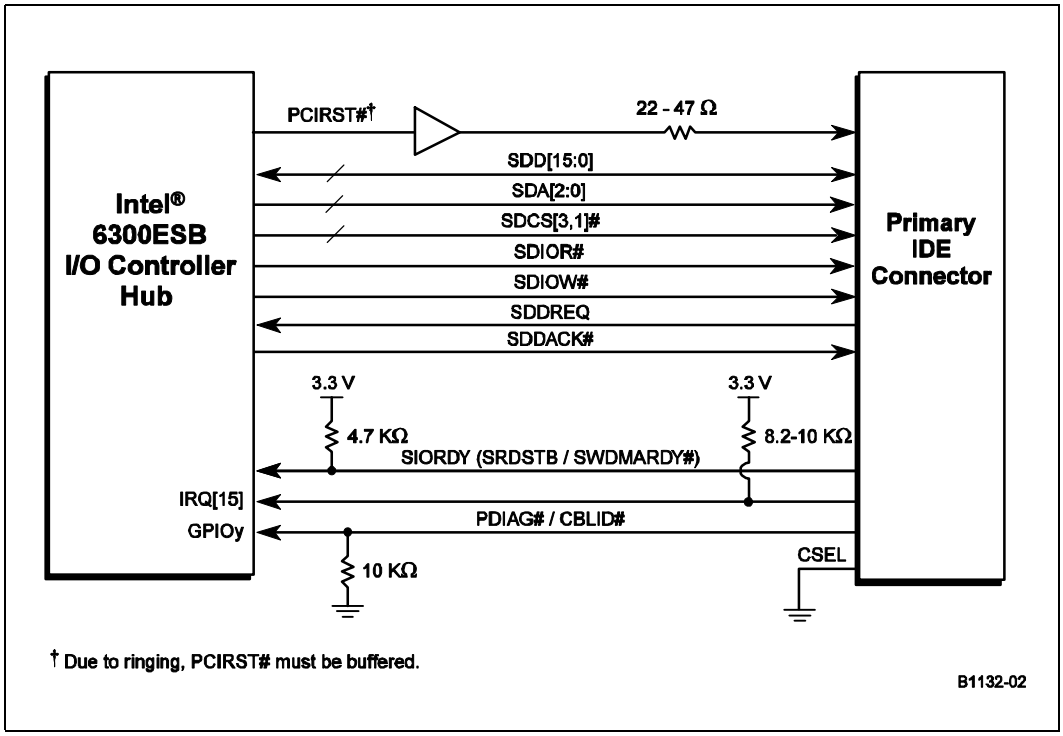
Figure 97. Connection Requirements for Primary IDE Connector



- 22 Ω - 47 Ω series resistors are required on PCIRST#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2K Ω to 10K Ω pull-up resistor is required on IRQ14 to $V_{CC}3.3$.
- A 4.7K Ω pull-up resistor to $V_{CC}3.3$ is required on PIORDY.
- Series resistors are not required but may be placed on the control and data line to improve signal quality. Place the resistors as close to the connector as possible. Resistor values are from 33-47 Ω.
- The 10K Ω resistor to ground on the PDIAG#/CBLID# signal is required on the Primary Connector. This change is to prevent the GPI pin from floating when a device is not present on the IDE interface.
- Place all resistors as close to the IDE connector as possible.

9.3.4 Secondary IDE Connector Requirements

Figure 98. Connection Requirements for Secondary IDE Connector



- 22 Ω - 47 Ω series resistors are required on PCIRST#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 KΩ to 10 KΩ pull-up resistor is required on IRQ15 to $V_{CC}3.3$.
- A 4.7 KΩ pull-up resistor to $V_{CC}3.3$ is required on SIORDY.
- Series resistors are not required but may be placed on the control and data line to improve signal quality. Place the resistors as close to the connector as possible. Resistor values are from 33 Ω - 47 Ω.
- The 10 KΩ resistor to ground on the PDIAG#/CBLID# signal is required on the Secondary Connector. This change is to prevent the GPI pin from floating when a device is not present on the IDE interface.
- Place all resistors as close to the IDE connector as possible.

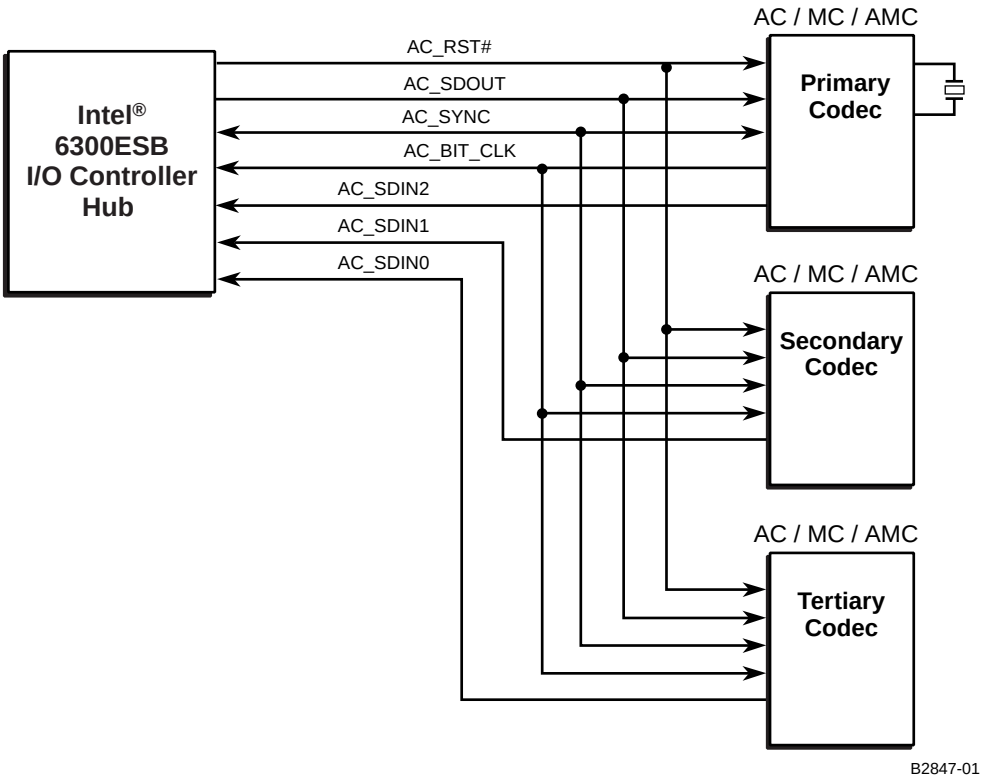
9.4 AC'97.

The 6300ESB implements an AC'97 2.2 compliant digital controller. Please contact your codec IHV (Independent Hardware Vendor) for information on 2.2 compliant products. The *AC'97 2.2 Specification* is on the Intel web site:

http://www.intel.com/design/chipsets/audio/

The AC-link is a unidirectional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the 6300ESB AC-link allows a maximum of three codecs to be connected. Figure 99 shows a three-codec topology of the AC-link for the 6300ESB.

Figure 99. 6300ESB AC'97 - Codec Connection



NOTES:
1. When a modem codec is configured as the primary AC-link codec, there cannot be any audio codecs residing on the AC-link.
2. The primary codec must be connected to AC_SDIN2 when also routing to CNR. If CNR does not exist on the platform, the primary codec may be connected to AC_8DIN0 as documented in the Intel® 6300ESB I/O Controller Hub Datasheet

Note: The following routing guidelines are created using the stack-up described in Section 3.1, "Nominal Board Stack-Up" on page 33.

Using the assumed six layer stack-up, the AC'97 interface may be routed using 5 mil traces with 10 mil spacing between the traces. Maximum length between the 6300ESB and the CODEC/CNR is 14 inches. This assumes that a CNR riser card implements its audio solution with a maximum trace length of six inches for the AC-link. The CNR and mother board target trace impedance should be Z_0 = 55 Ω ± 10% dependant on platform stackup described in Section 3.1, "Nominal Board Stack-Up" on page 33.

Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (6300ESB) and to any other codec present. That clock is used as the time base for latching and driving data.

The 6300ESB supports wake on ring from S1-S5 through the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The 6300ESB has pull-downs/pull-ups that are always enabled. This will keep the link from floating when the AC-link is off, or there are no codecs present.

When the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOUT will be driven by the codec and the 6300ESB, respectively. However, AC_SDIN0, AC_SDIN1 and AC_SDIN2 may not be driven. When the link is enabled, the assumption may be made that there is at least one codec.

Note: A 15 pF cap to Gnd should replace an unpopulated motherboard codec for the CLK and SDATA_IN lines to reduce reflection and improve signal quality.

Figure 100. 6300ESB AC'97 – AC_BIT_CLK Topology

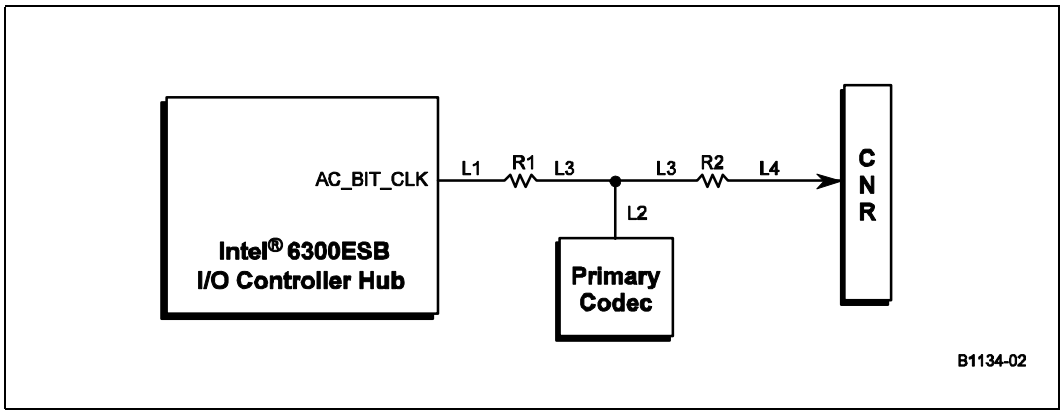


Table 76. AC'97 AC_BIT_CLK Routing Summary

Trace Impedance	AC'97 Routing Requirements	Trace Lengths	Series Termination Resistance	AC_BIT_CLK Signal Length Matching
55 Ω ± 10%	5 mil width, 10 mil spacing (based on stackup assumptions in Section 3.1)	L1 = 3 to 8 inches L2 = 0.1 to 0.5inches L3 = 0.1 to 0.5 inches L4 = 3 to 6 inches	R1 = 34.2 Ω - 37.8 Ω R2 = R1 (Optional 0 Ω resistor for debug purposes only).	N/A

Figure 101. 6300ESB AC'97 – AC_SDOUT/AC_SYNC Topology

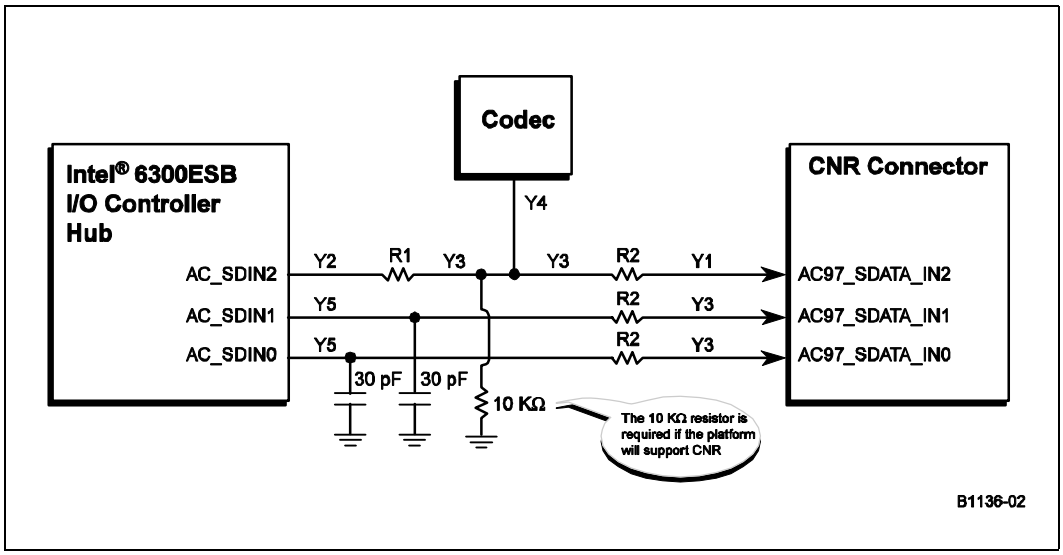


Table 77. AC'97 AC_SDOUT/AC_SYNC Routing Summary

Trace Impedance	AC'97 Routing Requirements	Trace Lengths	Series Termination Resistance	AC_SDOUT/AC_SYNC Signal Length Matching
55 Ω ± 10%	5 mil width, 10 mil spacing (based on stackup assumptions in Section 3.1)	L1 =3 to 6 inches L2 = 3 to 6 inches L3 = 0.1 to 0.5 inches L4 = 3 to 6 inches	R1 = 34 Ω - 38 Ω R2 = R1	N/A

Figure 102. 6300ESB AC'97 – AC_SDIN Topology

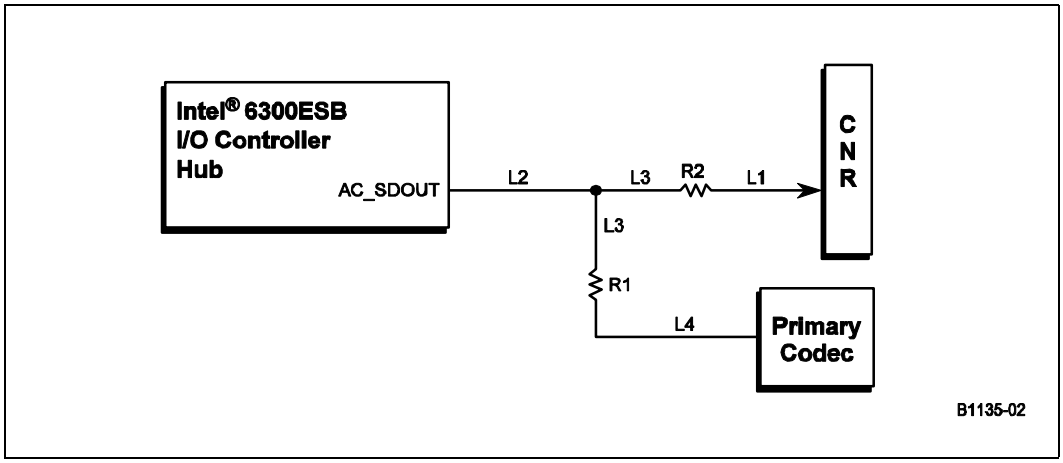


Table 78. AC'97 AC_SDIN Routing Summary

Trace Impedance	AC'97 Routing Requirements	Trace Lengths	Series Termination Resistance	AC_SDIN Signal Length Matching
55 Ω ± 10%%	5 mil width, 10 mil spacing (based on stackup assumptions in Section 3.1)	Y1 = 3 to 6 inches Y2 = 3 to 8 inches Y3 = 0.1 to 0.5 inches Y4 = 0.1 to 0.5 inches Y5 = 3 to12 inches	R1 = 34 Ω - 38 Ω R2 =R1	N/A

Note: AC_BIT_CLK, SDATA_OUT, SDATA_IN, SYNC all need to be routed on the same layer and NO layer changes are allowed.

9.4.1 AC'97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes must be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.

- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors may be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane
- Locate the crystal or oscillator close to the codec.

9.4.2 Motherboard Implementation

The following design considerations are provided for the implementation of an 6300ESB using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the 6300ESB.

- Active Components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The 6300ESB supports wake-on-ring from S1-S5 states through the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. In this case, the modem codec may be powered by either its own or an external clock source. When no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

9.4.2.1 Valid Codec Configurations

Table 79 describes the valid codec configurations.

Table 79. Supported Codec Configurations

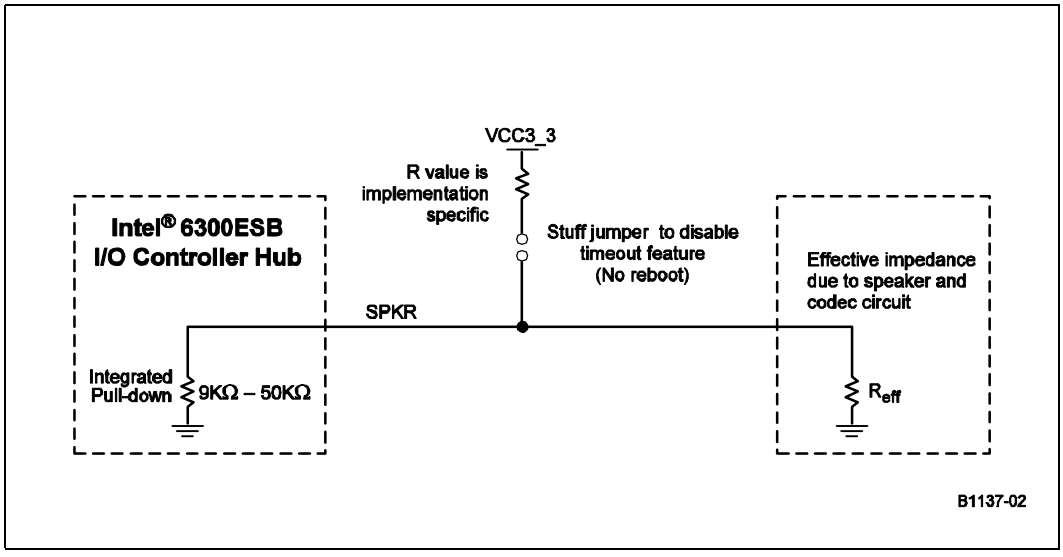
Option	Primary Codec	Secondary Codec	Tertiary Codec
1	Audio	Audio	Audio
2	Audio	Audio	Modem
3	Audio	Audio	Audio/Modem
4	Audio	Modem	Audio
5	Audio	Audio/Modem	Audio
6	Audio/Modem	Audio	Audio
7	Modem	-	-

NOTE: For power management reasons, codec power management registers are in audio space. As a result, when there is an audio codec in the system it must be Primary. In addition, there cannot be two modems in a system since there is only one set of modem DMA channels.

9.4.3 SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the TCO Timer Reboot function based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the 6300ESB sends an SMI# to the processor upon a TCO timer time out. The status of this strap is readable through the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper may be populated to pull the signal line high (see Figure 103). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{eff}), and the 6300ESB's integrated pull-down resistor will be read as logic high ($0.5\ V_{CC}3.3$ to $V_{CC}3.3 + 0.5$ V).

Figure 103. Example Speaker Circuit



9.4.4 AC_SDOUT Pin Consideration

AC_SDOUT is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the Safe Mode function based on the state of the AC_SDOUT pin on the rising edge of PWROK. When enabled, the 6300ESB will force the appropriate bits to engage Safe Mode. The status of this strap is readable through the SAFE_MODE bit (bit 2, D31: F0, Offset D4h). The AC_SDOUT signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot.

To disable the feature, a jumper may be populated to pull the signal line high. The value of the pull-up must be such that the voltage divider output caused by the pull-up and the 6300ESB's integrated pull-down resistor will be read as logic high (0.5 V_{CC}3.3 to V_{CC}3.3 + 0.5 V).

9.4.5 SIU0_DTR# Pin Consideration

SIU0_DTR# is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the Top Swap function based on the state of the SIU0_DTR# pin on the rising edge of PWROK. When disabled, the 6300ESB will not invert A16 for cycles targeting FWH BIOS space. The status of this strap is readable through the TOP_SWAP bit (bit 5, D31: F0, Offset D5h). The SIU0_DTR# signal has a weak integrated pull-up resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot.

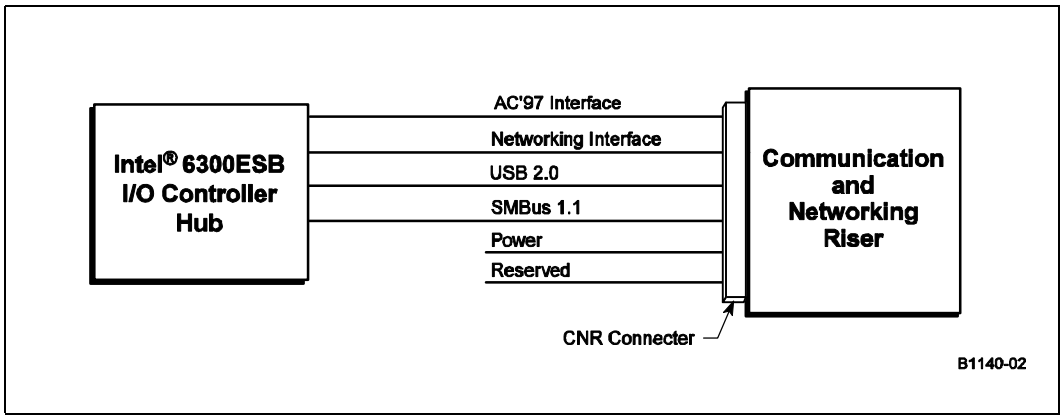
To disable the feature, a jumper may be populated to pull the signal line low. The value of the pull-down must be such that the voltage divider output caused by the pull-down and the 6300ESB's integrated pull-up resistor will be read as logic low.

9.5 Communication Network Riser

The *Communication and Networking Riser (CNR) Specification* defines a hardware scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. This interface supports AC'97 multi-channel audio, V.90 analog modem, phone-line based networking, SMBus Interface Power Management Rev 1.1, and USB 2.0. The CNR Specification defines the interface, which should be configured prior to shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot, therefore, the system designer will not sacrifice a PCI slot if they decide not to include a CNR in a particular build. For more information, refer to the *Communication and Network Riser Specification, Revision 1.2*, available at http://developer.intel.com/technology/cnr/download.htm

Figure 104 shows the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. Refer to the *CNR Specification* for additional information.

Figure 104. CNR Interface



9.5.1 AC'97 Audio Codec Detect Circuit and Configuration Options

Table 80 provides general circuits to implement a number of different codec configurations. Please refer to the *Communication Network Riser Specification, Revision 1.2*, for Intel's recommended codec configurations

Table 80. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC'97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC'97 Interface.
AC97_RESET#	Reset signal from the AC'97 Digital Controller (6300ESB).
SDATA_IN*n*	AC'97 serial data from an AC'97-compliant codec to an AC'97-compliant controller (i.e., the 6300ESB).

9.5.1.1 CNR 1.2 AC'97 Disable and Demotion Rules for the Motherboard

The following are the CNR 1.1/1.2 AC'97 Disable and Demotion Rules for the motherboard.

- All AC'97 *Rev 2.2* codecs on the motherboard **must** always disable themselves when the CDC_DN_ENAB# signal is in a high state.
- A motherboard AC'97 codec **must** never change its address or SDATA_IN line used, regardless of the state of the CDC_DN_ENAB# signal.
- On a motherboard containing an AC'97 Controller supporting three AC'97 Codecs, the AC'97 Revision 2.2 codec on the motherboard **must** be connected to the SDATA_IN2 signal of the CNR connector.

The above rules allow for forward and backward compatibility between CNR Version 1.1/1.2 cards. For more information on chaining consult the *Communication Network Riser Specification, Revision 1.2*.

Figure 105. Motherboard AC'97 CNR Implementation with a Single Codec Down On Board

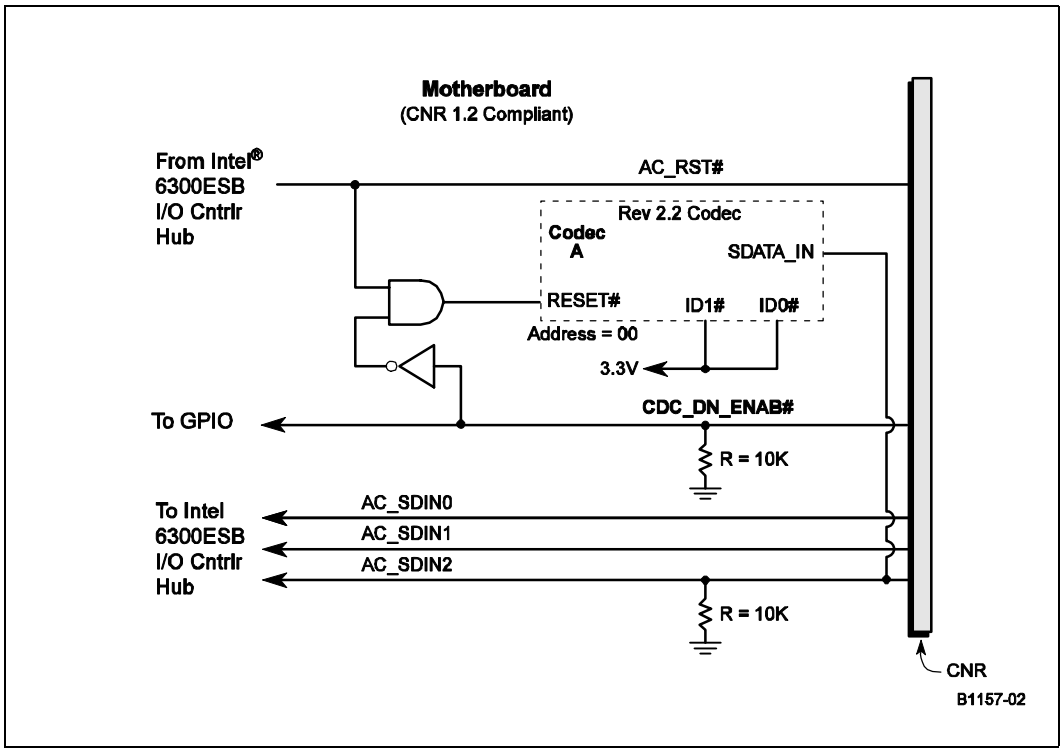
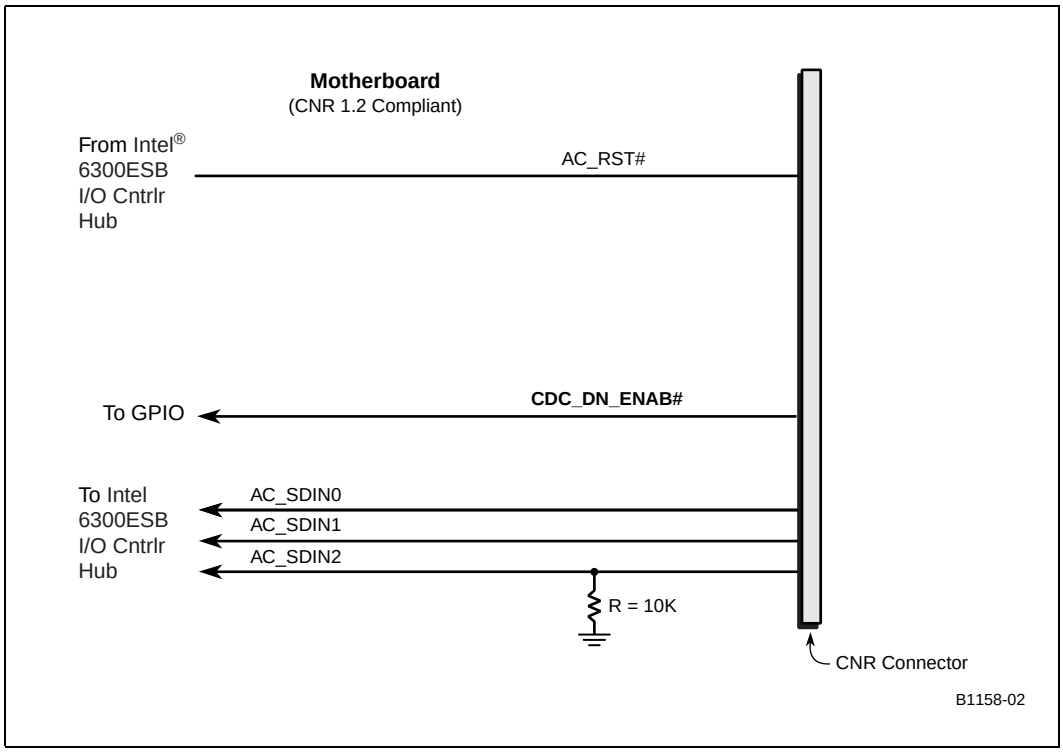


Figure 106. Motherboard AC'97 CNR Implementation without Codec Down On Board



9.5.2 CNR Routing Summary

Table 81 represents a summary of the various interfaces routing requirements to the CNR Riser.

Table 81. CNR Routing Summary

Trace Impedance	CNR Routing Requirements	Maximum Trace Length to CNR connector	Signal Length Matching	Signal Referencing
90 Ω Differential	USB (7.5 on 7.5) (See Section 9.6.1.6 for more details)	10 inches	No more than 150 mils trace mismatch.	Ground
55 Ω ± 10%	AC'97 (5 on 10)	AC_BIT_CLK (See Table 76) AC_SDOUT (See Table 77) AC_SDIN (See Table 78)	N/A	Ground

9.6 USB 2.0

9.6.1 Layout Guidelines

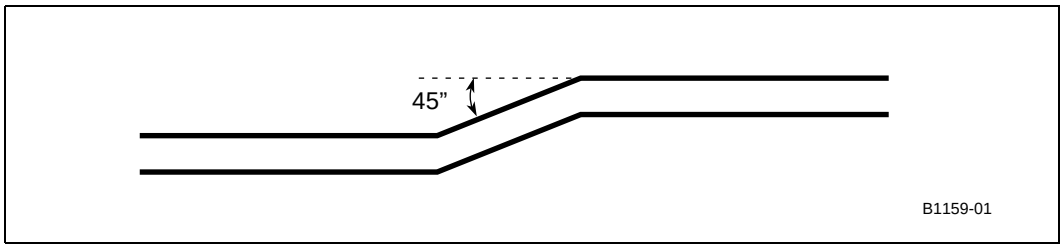
Note: These routing guidelines are created using the stack-ups described in Section 3.1, "Nominal Board Stack-Up" on page 33.

9.6.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems.

1. Place the 6300ESB and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
2. USB 2.0 signals should be ***ground referenced*** (on recommended stackup this would be bottom signal layer).
3. Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities. (See Figure 107.)
5. Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
6. Stubs on High-speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. When a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils.
7. Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch when possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 9.6.2, "Plane Splits, Voids and Cut-Outs (Anti-Etch)" on page 213.
8. Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
9. Keep the USB 2.0 signals clear of the core logic set. High current transients are produced during internal state transitions and may be very difficult to filter out.
10. Follow the 20 x h thumb rule by keeping traces at least 20 x (height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stackup the height above the plane is 4.5 mils. This calculates to a 90 mils spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

Figure 107. Trace Routing

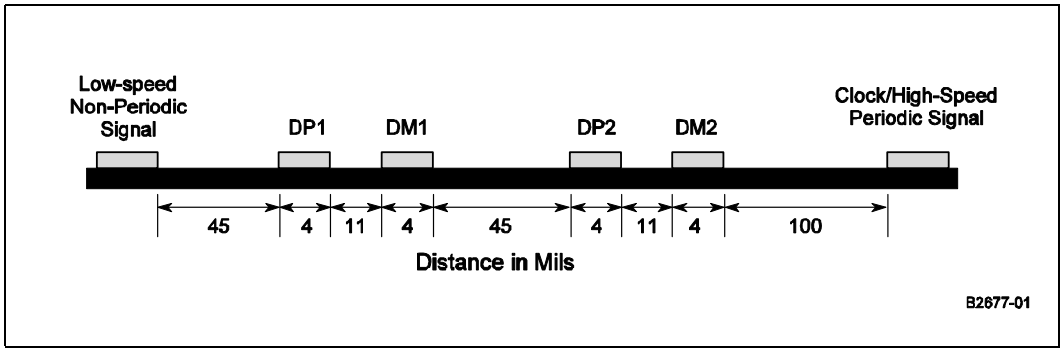


9.6.1.2 USB 2.0 Trace Separation

Use the following separation guidelines. Figure 108 provides illustration of the recommended trace spacing.

1. Maintain parallelism between USB differential signals with the trace spacing needed to achieve the target differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used; keeping in mind the target differential impedance.
3. Minimize the length of high-speed clock and periodic signal traces that run parallel to High-speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 100 mils.
4. Based on simulation data, use 45 mils minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

Figure 108. Recommended General USB Trace Spacing (55 Ω ± 10%)



9.6.1.3 USB BIAS Connections

The USBRBIAS pin and the USBRBIAS# pin may be shorted and routed 5 mils width, 5 mils spacing, to one end of a 22.6 Ω ± 1% resistor to ground. Place the resistor within 500 mils of the 6300ESB and avoid routing next to clock pins. (See Figure 109 and Table 82 for more information.)

Figure 109. USB BIAS Connections

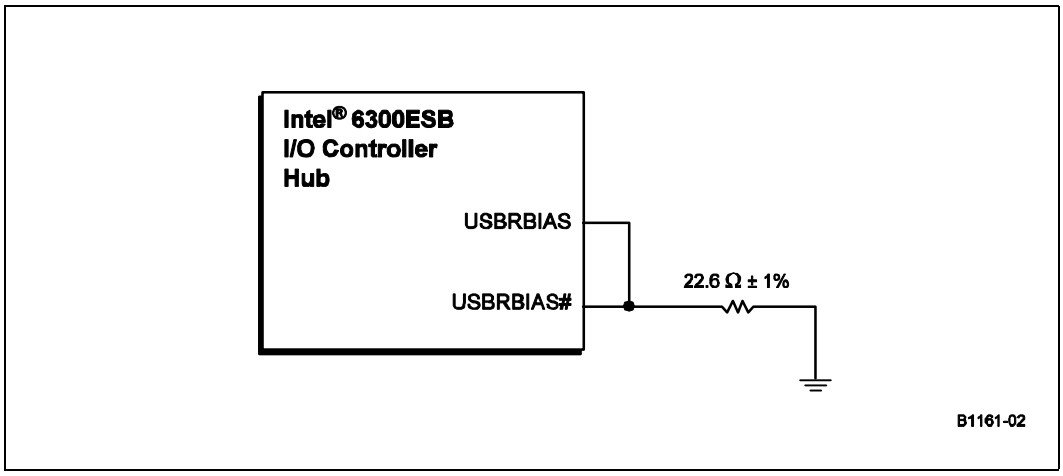


Table 82. USB BIAS Routing Summary

Trace Impedance	USBRBIAS/USBRBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
55 Ω ± 10%	5 mils width, 5 mils spacing	500 mils	N.A.	N.A.

9.6.1.4 USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See Section 9.6.4, “EMI Considerations” on page 214 for details.

9.6.1.5 USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pair should not be greater that 60 mils.

9.6.1.6 USB 2.0 Trace Length Guidelines

Table 83 and Table 84 provide trace length guidelines.

9.6.1.6.1 Platforms With A Nominal Impedance Of 55 Ω ± 10% (Microstrip)

Table 83. USB 2.0 Back Panel Trace Length Guidelines (Common-mode Choke, 55 Ω ± 10%)

Differential Impedance	Pair Spacing	Signal Referencing	Signal Matching	Maximum Motherboard Trace Length
100 ± 10%	45 mils	Ground	The max mismatch between data pairs should not be greater than 60 mils	7.4 inches
	80 mils			10.1 inches

NOTE: Two options are given for motherboard trace length, choose the parameters that best suit your system.

Table 84. USB 2.0 CNR Trace Length Guidelines (Common-mode Choke, 55 Ω ± 10%)

Differential Impedance	Pair Spacing	Maximum Motherboard Trace Length	Maximum CNR Card Length	Signal Matching
100 ± 10%	45 mils	1.0 inches	5.6 inches	The max mismatch between data pairs should not be greater than 60 mils
		2 inches	4 inches	
		5 inches	2 inches	
	80 mils	1.9 inches	6 inches	
		3.5 inches	4 inches	
		6.2 inches	2 inches	

NOTE: Many options are given for motherboard trace length and CNR card trace length, choose the parameters that best suit your system.

Table 85. USB 2.0 Front Panel Trace Length Guidelines (Common-mode Choke, 55 Ω ± 10%)

Differential Impedance	Pair Spacing	Maximum Cable Length	Maximum Motherboard Trace Length	Maximum Front Panel Length	Signal Matching
100 ± 10%	45 mils	9.1 inches	4.9 inches	1.5 inches	The max mismatch between data pairs should not be greater than 60 mils
		6.5 inches	5.47 inches	2.5 inches	

NOTE: Two options are given for motherboard trace length, Cable Length and Front panel Length, choose the parameters that best suit your system.

9.6.2 Plane Splits, Voids and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cut-outs.

9.6.2.1 V_{CC} Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the V_{CC} plane.

Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces which might be coupling to them. USB signaling is not purely differential in all speeds (i.e., the Full-speed Single Ended Zero is common mode).

Note: Avoid routing of USB 2.0 signals 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits when a choice has to be made between one or the other.

When crossing a plane split is completely unavoidable, proper placement of stitching caps may minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge voltage plane splits close to where High-speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates $V_{CC}5$ and $V_{CC}3.3$ planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to $V_{CC}5$ and the other side should tie to $V_{CC}3.3$. Stitching caps provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

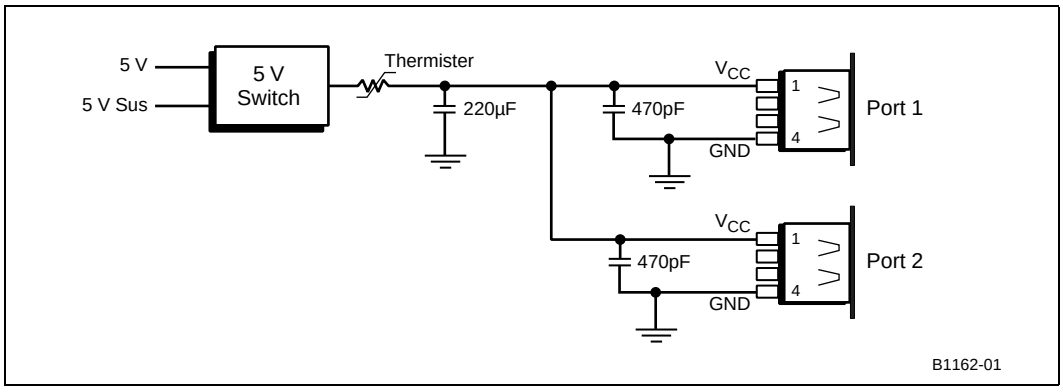
9.6.2.2 GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

9.6.3 USB Power Line Layout Topology

The following is a suggested topology for power distribution of V_{BUS} to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach fly back protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach fly back voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane. Make the power-carrying traces wide enough that the system fuse will blow on an over current event. When the system fuse is rated at 1 amps, the power-carrying traces should be wide enough to carry at least 1.5 amps.

Figure 110. Good Downstream Power Connection



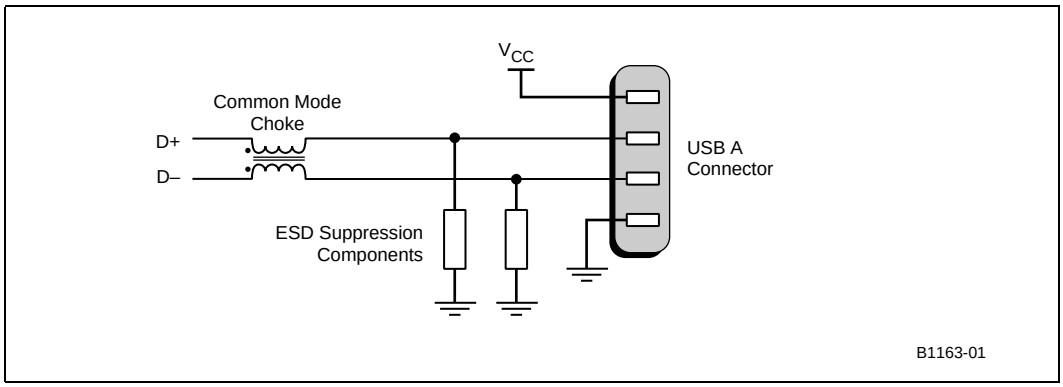
9.6.4 EMI Considerations

The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices.

9.6.4.1 Common-Mode Chokes

Testing has shown that common-mode chokes may provide required noise attenuation. A design should include a common-mode choke footprint to provide a stuffing option ***in the event*** the choke is needed to pass EMI testing. Figure 111 shows the schematic of a typical common-mode choke and ESD suppression components. Place the choke as close as possible to the USB connector signal pins. In systems that route USB to a front panel header, place the choke on the front panel card. (See Section 9.6.6.3, "Front Panel Connector Card" on page 218 for more information.)

Figure 111. A Common-Mode Choke



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion will increase, so you should test the effects of the common mode choke on full speed and high-speed signal quality. Common-mode chokes with a target impedance of 80 Ω to 100 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common-mode choke that meets the designer's needs is a two-step process.

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
2. Once you have a part that gives passing EMI results the second step is to test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing includes checking the signal quality for low-speed, full-speed and high-speed USB operation.

9.6.5 ESD

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. ESD protection is needed for USB lines. Refer to the Intel® ICH Family USB ESD Considerations Application Note for ESD protection implementation guidelines. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 111. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, it is recommended to include footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

9.6.6 Front Panel Solutions

9.6.6.1 Internal USB Cables

The front panel internal cable solution must meet all the requirements of Chapter 6 of the *Universal Serial Bus Specification, Revision 2.0*, for High-/Full-speed cabling for each port with the exceptions described in Cable Option 2. For more information refer to the Intel FPIO design guideline available at http://www.formfactors.org/developer/specs/fpio_design_guideline.pdf

9.6.6.1.1 Internal Cable Option 1

Use standard High-speed/Full-speed compatible USB cables. These must meet all cabling requirements called out in Chapter 6 of the *Universal Serial Bus Specification, Revision 2.0*. Recommended motherboard mating connector pin-out is covered in detail in Section 9.6.6.2.

9.6.6.1.2 Internal Cable Option 2

Use custom cables that meet all of the requirements of Chapter 6 of the *Universal Serial Bus Specification, Revision 2.0*, with the following additions/exceptions.

1. They may share a common jacket, shield and drain wire.
2. Two ports with signal pairs that share a common jacket may combine V_{BUS} and ground wires into a single wire provided the following conditions are met:
   a. The bypass capacitance required by Section 7.2.4.1 of the *Universal Serial Bus Specification, Revision 2.0*, is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughter card). Refer to the front panel daughter card referenced later for details.
   b. Selecting proper wire size: A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the *Universal Serial Bus Specification, Revision 2.0*, that has ½ the resistance of either of the two wires being combined. The data is provided for reference in Table 86.

Table 86. Conductor Resistance (Table 6-6 from USB 2.0 Specification)

American Wire Gauge (AWG)	Ohm (Ω) / 100 meters maximum
28	23.20
26	14.60
24	9.09
22	5.74
20	3.58

Example: Two 24 gauge (AWG) power or ground wires may be replaced with one 20-gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the *Universal Serial Bus Specification, Revision 2.0*, at the USB connectors as well as at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure the system passes droop requirements. Cables that provide individual power and ground conductors for each port may usually meet droop requirements by providing adequate capacitance near the motherboard mating connector, since droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case, all transients will be seen/dampened by the capacitance at the motherboard mating connector before they may cause problems with the adjacent port sharing the same cable. See sections 7.2.2 and 7.2.4.1 of the *Universal Serial Bus Specification, Revision 2.0*, for more details.

Note: Cables that contain more than two signal pairs are not recommended due to unpredictable impedance characteristics.

9.6.6.2 Motherboard/PCB Mating Connector

Proper selection of a motherboard mating connector for front panel USB support is important to ensure signal quality is not adversely affected due to a poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the *Universal Serial Bus Specification, Revision 2.0*.

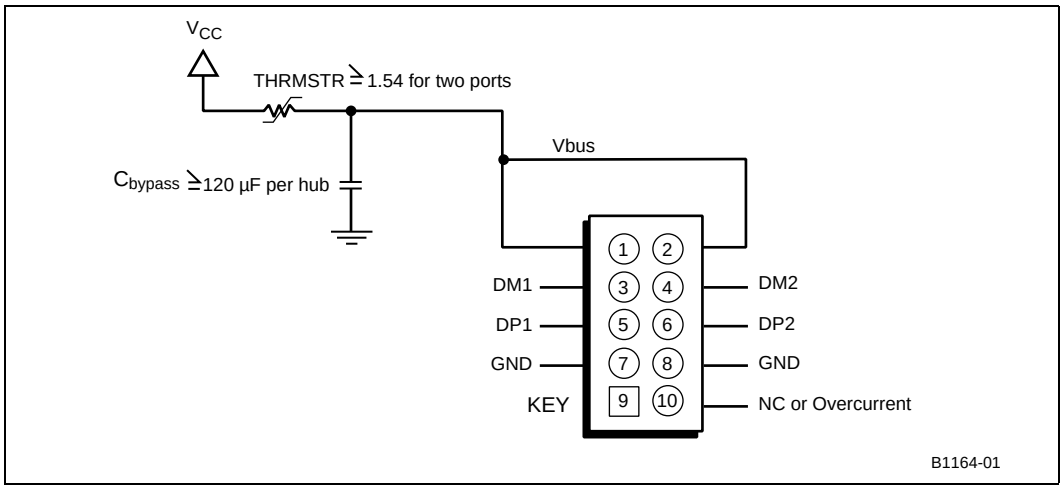
9.6.6.2.1 Pin-Out

A ten pin, 0.1-inch pitch stake pin assembly is recommended with the pin-out listed in Table 9.6.6.3 and schematic shown in Figure 112.

Table 87. Front Panel Header Pin-Out

Pin	Description
1	Vcc
2	Vcc
3	dm1
4	dm2
5	dp1
6	dp2
7	GND
8	GND
9	key
10	no connect or over-current sense

Figure 112. Front Panel Header Schematic



Note: It is **highly** recommended that the fuse element (thermistor) for the front panel header be included on the motherboard to protect the motherboard from damage in the following instances:

1. If an un-fused front panel cable solution is used.
2. If an un-keyed cable is inadvertently plugged onto the front panel USB connector.
3. If the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between V_{BUS} and ground.

9.6.6.2.2 Routing Considerations

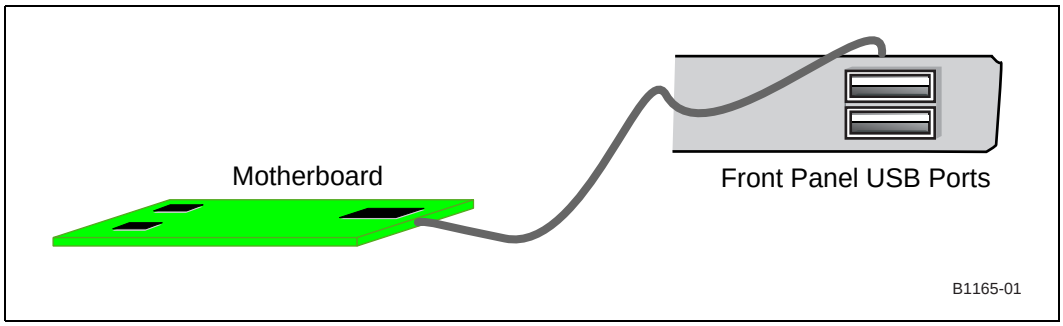
Traces or surface shapes from V_{CC} to the thermistor, to C_{BYPASS} and to the connector power and ground pins should be at least 50 mils wide to ensure adequate current carrying capability. There should be double vias on power and ground nets, and the trace lengths should be kept as short as possible.

9.6.6.3 Front Panel Connector Card

The best way to provide front or side panel support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. Figure 113 shows the major components associated with a typical front/side panel USB solution that uses a front panel connector card. For more information refer to the Intel FPIO design guideline available at:

http://www.formfactors.org/developer/specs/fpio_design_guideline.pdf.

Figure 113. Motherboard Front Panel USB Support



Note: When designing front panel I/O in a system where a connector card will be used ensure that there aren't duplicate EMI/ESD/thermistor components. Duplicate components will result in drop/droop and signal quality degradation or failure.

9.6.6.3.1 Front Panel Daughter Card Design Guidelines

1. Place the V_{BUS} bypass capacitance, CMC, and ESD suppression components on the daughter card as close as possible to the connector pins.
2. Follow the same layout, routing and impedance control guidelines as specified for motherboards.
3. Minimize the trace length on the front panel connector card. Trace length less than two inches is recommended.
4. Use the same mating connector pin-out as outlined for the motherboard in Section 9.6.6.3, "Front Panel Connector Card" on page 218.
5. Use the same routing guidelines as described in Section 9.6.1, "Layout Guidelines" on page 210.
6. Trace length guidelines are given in Table 84 and Table 85.

9.7 Low Pin Count (LPC) Interface.

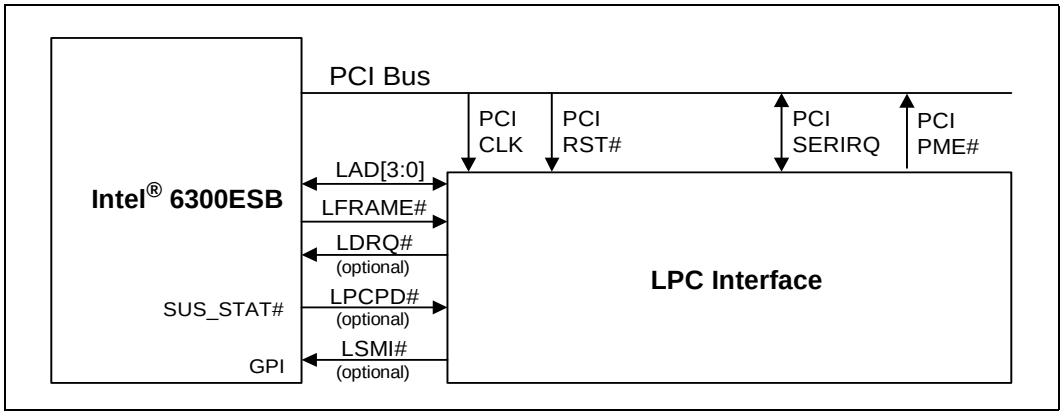
The 6300ESB implements a Low Pin Count (LPC) Interface compliant with the *Low Pin Count Interface Specification Revision 1.0*. The following section provides design guidelines for proper interfacing with the LPC bus. These guidelines will help to minimize signal integrity issues and maintain conformance to LPC specifications.

The LPC Interface to the 6300ESB is shown in Figure 114. Note that the 6300ESB implements all of the signals that are shown as optional, but peripherals are not required to do so. For the 6300ESB:

- LSMI# may be connected to any of the 6300ESB's GPIO signals, as they may be configured as inputs to generate an SMI#.
- The Super I/O's PME# may be connected to the PCI PME# signal, however this may cause software problems. A better choice is to connect it to one of the 6300ESB's GPIO signals, as they may configured to generate an SCI.
- The 6300ESB's SUS_STAT# signal is connected directly to the LPCPD# signal.

All the other signals have the same name on the 6300ESB and on the LPC Interface.

Figure 114. LPC Interface Diagram



9.7.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design.

1. LPC signals should be *ground referenced.*
2. Route all traces using microstrip or stripline over continuous planes (Vcc or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane may cause signal reflections and should be avoided.
3. Route LPC signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. No 90 degree bends or stubs.

9.7.2 LPC Trace Length Matching

LPC clock traces should be trace length matched. Max trace length mismatch between clocks coming from the clock driver should be no greater that 250 mils.

9.7.3 LPC Interface Routing Guidelines

Figure 115. LPC Interface Topology

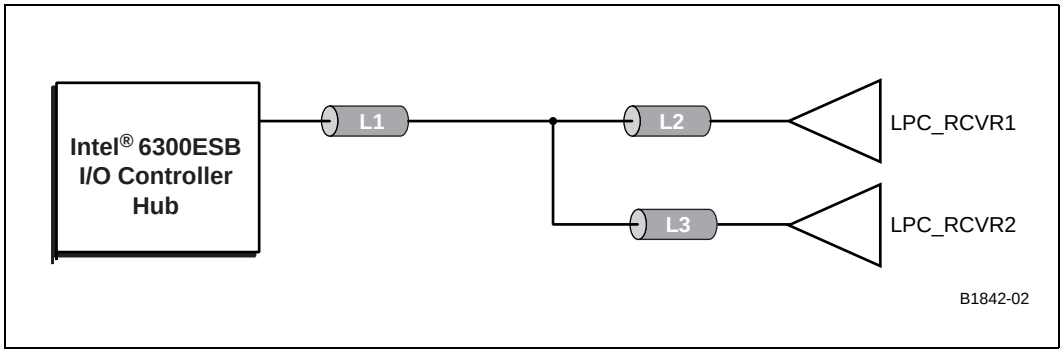


Table 88. LPC Interface Routing Summary

Trace Impedance	LPC Routing Requirements	Trace Lengths	LPC Clock Length Matching
55 Ω ± 10%	5 mil width, 12 mil spacing (based on stackup assumptions in Section 3.1)	L1 = 2 to 8 inches L2 = 0 to 6 inches L3 =0 to 6 inches	No more than 0.25 inches (250 mils) difference between clock signals.

9.8 SMBus 2.0/SMLink Interface

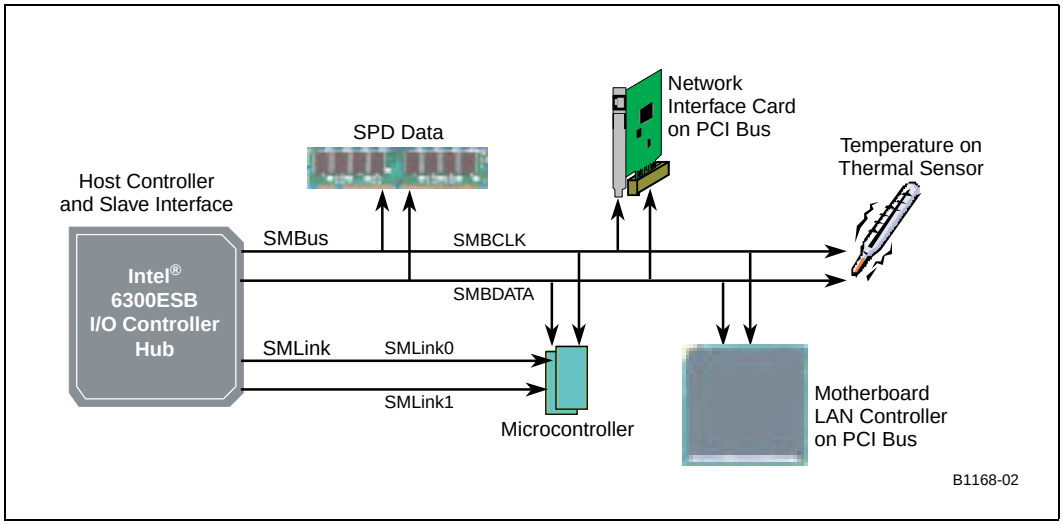
The SMBus interface on the 6300ESB uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus (see Figure 116). These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the 6300ESB.

The 6300ESB incorporates a SMLink interface supporting Alert on LAN*, Alert on LAN2* and a slave functionality. It uses two signals SMLINK [1:0]. SMLINK[0] corresponds to an SMBus clock signal and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert on LAN* functionality, the 6300ESB transmits heartbeat and event messages over the interface. When using the Intel® 82562EM/82562EX Platform LAN Connect Component, it will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert on LAN2*-enabled LAN Controller (e.g., Intel 82562EM/82562EX 10/100 Mbps Platform LAN Connect) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the 6300ESB SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface may reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface may read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces may be externally wire-ORed together to allow an external management ASIC (such as Intel 82562EM/82562EX 10/100 Mbps Platform LAN Connect) to access targets on the SMBus as well as the 6300ESB Slave interface. Additionally, the 6300ESB supports slave functionality, including the Host Notify protocol, on the SMLink pins.

Figure 116. SMBUS 2.0/SMLink Interface



Note: Intel does not support access of the 6300ESB SMBus Slave Interface by the 6300ESB SMBus Host Controller. Refer to the *Intel®* 6300ESB I/O Controller Hub *Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

9.8.1 SMBus Architecture & Design Considerations

9.8.1.1 SMBus Design Considerations.

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

- Device class (High/Low power). Most designs use primarily High Power Devices.
- Mixed Power Architecture. If there are devices that must run in S3, special considerations must be made (see Section 9.8.1.3).
- Amount of $V_{CC\_SUSPEND}$ current available (i.e., minimizing load of $V_{CC\_SUSPEND}$).

9.8.1.2 General Design Issues / Notes

Regardless of the architecture used, there are some general considerations.

- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally, the SMBus device that may sink the least

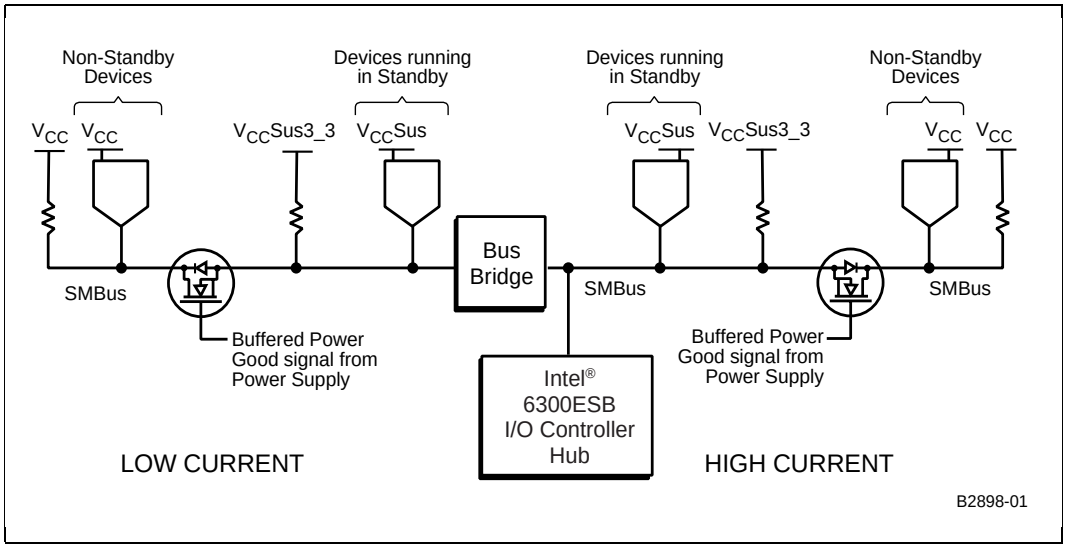
amount of current is the limiting agent on how small the resistor may be. The pull-up resistor may not be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and time specification.

- The maximum bus capacitance that a physical segment may reach is 400 pF.
- The 6300ESB does not run SMBus cycles while in S3.
- SMBus devices that may operate in STR must be powered by the $V_{CC\_SUSPEND}$ supply.
- When the SMBus is connected to the PCI Bus, it must be connected to all PCI slots in the system.

9.8.1.3 High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices while also allowing SMBus devices to communicate while in S3. $V_{CC\_SUSPEND}$ leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of a FET to isolate the devices powered by the core and suspend supplies. See Figure 117.

Figure 117. High Power/Low Power Mixed $V_{CC\_SUSPEND}$/V_{CC_CORE} Architecture



NOTES:
1. Added considerations for mixed architecture.
2. The bus switch must be powered by $V_{CC_}$SUSPEND.
3. Devices powered by the $V_{CC_}$SUSPEND well must not drive into other devices that are powered off. This is accomplished with the bus switch.
4. The bus bridge can be a device like the Philips* PCA9515.

9.8.1.4 Calculating the Physical Segment Pull-Up Resistor

The following tables are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. When any physical bus segment exceeds 400 pF, then a bus bridge device such as the Philips Semiconductor* PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 89. Bus Capacitance Reference Chart

Device	# of Devices/ Trace Length	Capacitance Includes	Cap (pF)
6300ESB	1	Pin Capacitance	12
CK409	1	Pin Capacitance	10
DIMMS/RIMMS	2	Pin Capacitance (10 pF) + 1 inch worth of trace capacitance (2 pF/inch) per DIMM/RIMM and 2 pF connector capacitance per DIMM/RIMM.	28
	3		42
PCI	2	Each PCI add-in card is allowed up to 40 pF + 3 pF per each connector.	86
	3		129
	4		172
	5		215
SMBus Trace Length in inches	= 24	2 pF per inch of trace length	48
	= 36		72
	= 48		96
CNR	1	Pin Capacitance (10 pF) + 6 inch worth of trace capacitance (2 pF/inch) and 2 pF connector capacitance.	24

Table 90. Bus Capacitance/Pull-Up Resistor Relationship

Physical Bus Segment Capacitance	Pull-Up Range (For Vcc = 3.3V
0 to 100 pF	8.2K Ω to 1.2 KΩ
100 to 200 pF	4.7K Ω to 1.2 KΩ
200 to 300 pF	3.3K Ω to 1.2 KΩ
300 to 400 pF	2.2K Ω to 1.2 KΩ

9.9 PCI

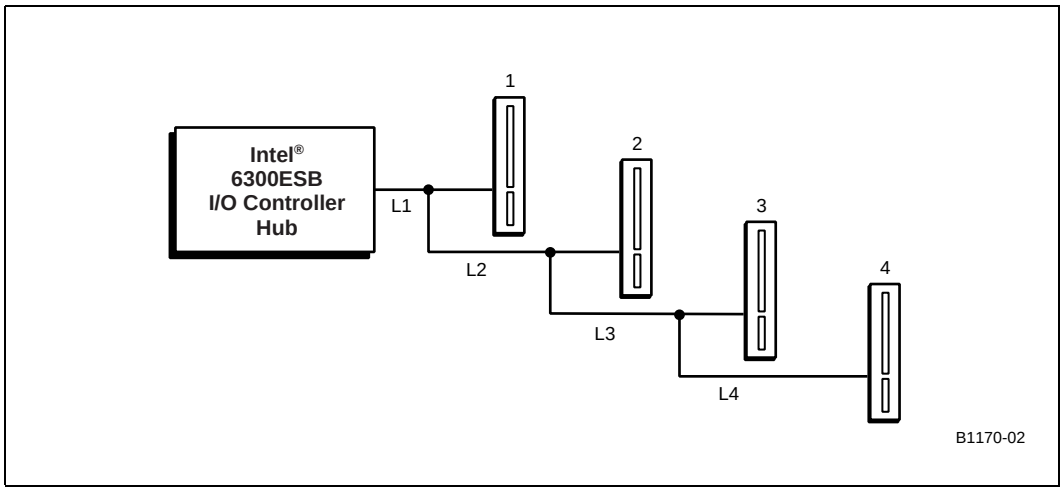
The 6300ESB provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the 6300ESB is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, please refer to the *PCI Local Bus Specification, Revision 2.2*.

9.9.1 PCI Routing Summary

The following represents a summary of the routing guidelines for the PCI devices. The 6300ESB supports four PCI devices. Simulations assume that PCI cards follow the *PCI Local Bus Specification, Revision 2.2*, trace length guidelines.

Note: These routing guidelines are created using the stack-up described in Section 3.1, “Nominal Board Stack-Up” on page 33.

Figure 118. PCI Bus Layout Example



Note: When a CNR connector is placed on the platform, it will share a slot space with one of the PCI slots. However, it will not take away from the slot functionality unless the CNR slot is occupied by a CNR card.

Figure 119. PCI Bus Layout Example with IDSEL

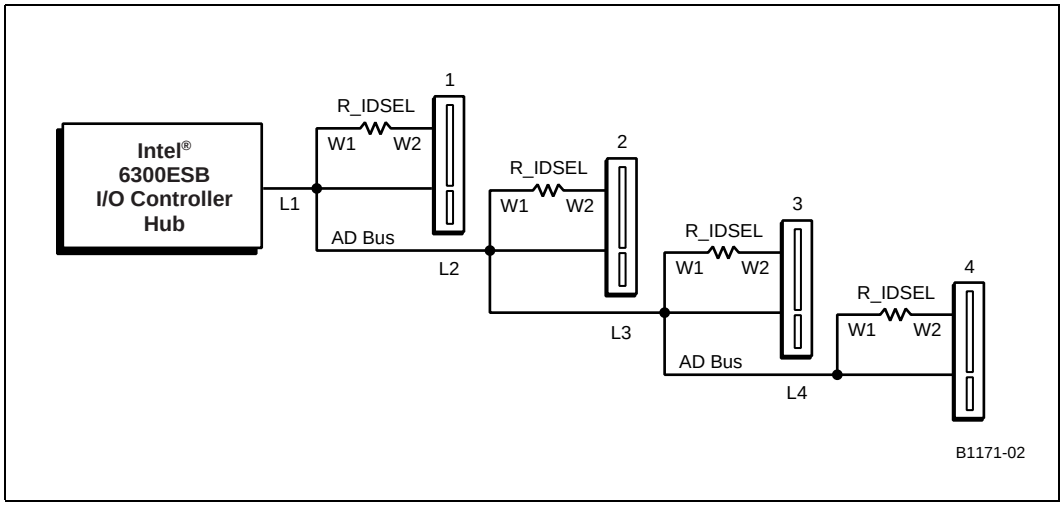


Table 91. PCI Data Signals Routing Summary

Trace Impedance	PCI Routing Requirements	Topology	Maximum Trace Length L1 L2 L3 L4			
55 Ω ± 10%	5 mils width, 7 mils spacing (based on stackup assumptions in Section 3.1)	2 Slots W1 = W2 = 0.5 inches, R_IDSEL = 300 to 900 Ω	10 inches	1.0 inch		
		3 Slots W1 = W2 = 0.5 inches, R_IDSEL = 300 to 900 Ω	10 inches	1.0 inch	1.0 inch	
		4 Slots W1 = W2 = 0.5 inches, R_IDSEL = 300 to 900 Ω	10 inches	1.0 inch	1.0 inch	1.0 inch

Figure 120. PCI 33MHz Clock Layout Example

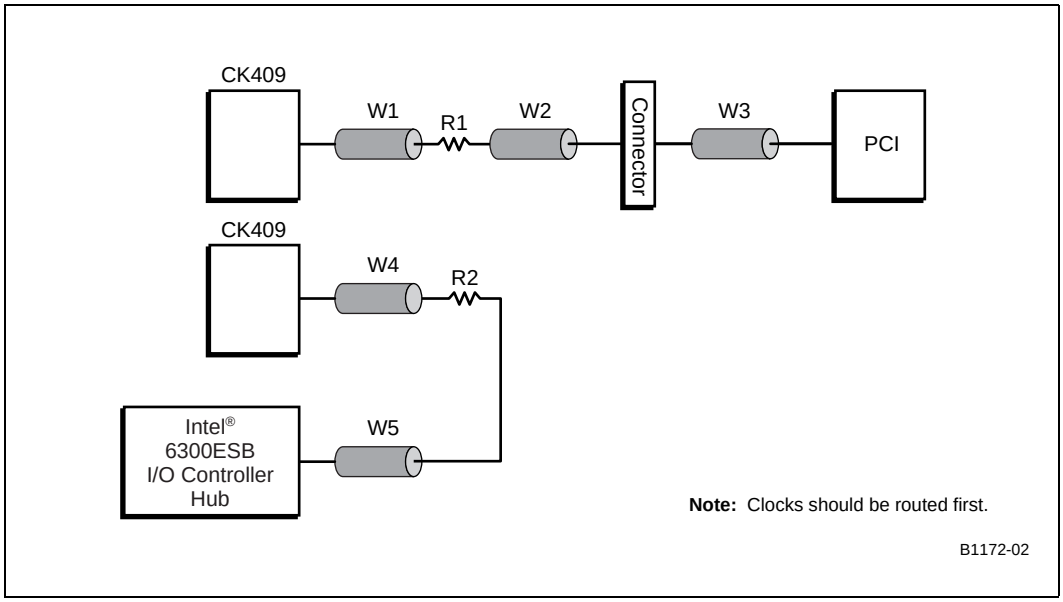


Table 92. PCI 33 MHz Clock Signals Routing Summary

Trace Impedance	PCI Routing Requirements	Topology	Maximum Trace Length	Resistor Values
55 Ω ± 10%	5 mils width, 50mils spacing (based on stackup assumptions in Section 3.1)	2 -4 Devices	W1 = 0.5 inches W2 = W5 – 4.5” W3 = 2.5 inches (Shown as a reference only) W4 = 0.5 inches W5 = May be as long as needed as long as W2 is scaled accordingly	R1 = 33 Ω R2 = 33 Ω

9.9.2 PIRQ Routing Example

Table 93 shows how the 6300ESB uses the PCI IRQ when the IOAPIC is active.

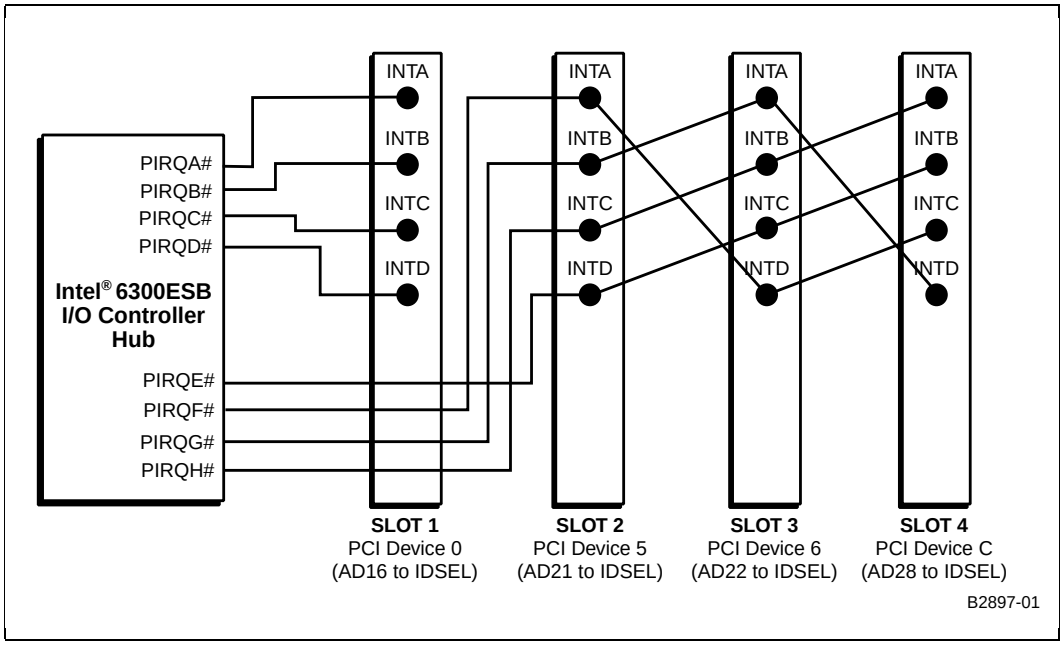
Table 93. IOAPIC Interrupt Inputs 16 through 23 Usage

No	IOAPIC INTIN PIN	Function in 6300ESB using the PCI IRQ in IOAPIC
1	IOAPIC INTIN PIN 16 (PIRQA)	USB UHCI Controller #1
2	IOAPIC INTIN PIN 17 (PIRQB)	AC'97 Audio and Modem; option for SMBus
3	IOAPIC INTIN PIN 18 (PIRQC)	USB UHCI Controller #3; Native mode SATA/IDE
4	IOAPIC INTIN PIN 19 (PIRQD)	USB UHCI Controller #2
5	IOAPIC INTIN PIN 20 (PIRQE)	Option for SCI, TCO, MMT #0,1,2
6	IOAPIC INTIN PIN 21 (PIRQF)	Option for SCI, TCO, MMT #0,1,2
7	IOAPIC INTIN PIN 22 (PIRQG)	Option for SCI, TCO, MMT #0,1,2
8	IOAPIC INTIN PIN 23 (PIRQH)	USB EHCI Controller, Option for SCI, TCO, MMT #0,1,2

Due to different system configurations, IRQ line routing to the PCI slots (swizzling) should be made to minimize the sharing of interrupts between both internal 6300ESB functions and PCI functions. The figure below shows an example of IRQ line routing to the PCI slots

It is not necessarily an optimal routing scheme; an optimal scheme depends on individual system PCI IRQ usage.

Figure 121. Example PIRQ Routing



NOTE: This figure is an example; it is up to the board designer to route these signals in the most efficient manner for their particular system. A PCI slot can be routed to share interrupts with any of the Intel 6300ESB I/O Controller Hub's internal devices/functions, but at a higher latency cost.

9.10 PCI-X Design Guidelines

This section contains guidelines for connecting and routing the 6300ESB PCI-X interface. The 6300ESB supports up to four PCI-X devices. This section provides guidelines for PCI-X connector and motherboard design, including component and resistor placement. When considering PCI-X device configurations refer to Table 94 which shows all the slot/device-down options possible with the 6300ESB PCI-X Interface.

Table 94. PCI-X Slot/Device Configurations

PCI-X 1.0 Segment Configurations	# of Slots	# of Devices Down
6 loads, 3 pairs REQ/GNT	3	0
5 loads, 3 pairs REQ/GNT	2	1
6 loads, 4 pairs REQ/GNT	2	2
5 loads, 4 pairs REQ/GNT	1	3
4 loads, 4 pairs REQ/GNT	0	4

Note: Bounded by six electrical loads and four REQ/GNT pairs (1 slot = 2 electrical loads)

Note: These routing guidelines are created using the stack-up described in Section 3.1, "Nominal Board Stack-Up" on page 33.

The PCI-X interface may be routed with 5 mils traces on 12 mils spaces (dependent upon stackup parameters), and must be less than eight inches long (from 6300ESB to PCI-X connector). Trace spacing of 5 mils is only acceptable when necessary to route through pin fields. For more information, refer to the *PCI-X Specification, Rev 1.0*.

Table 95. PCI-X Routing Summary

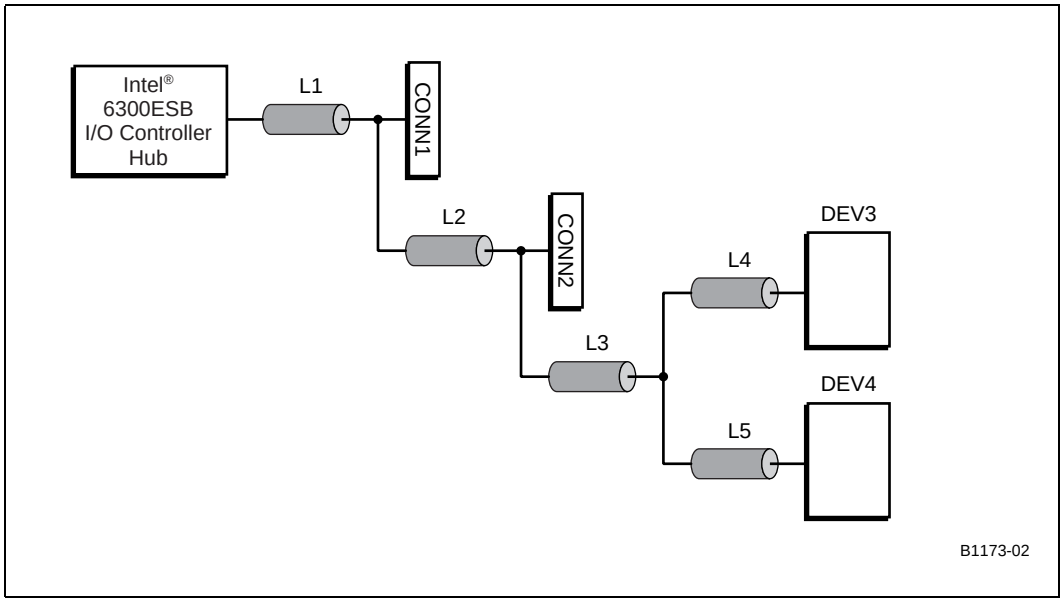
Trace Impedance	PCI-X Routing Requirements	Maximum Trace Length (To first connector)	Maximum Trace Length Between Connectors	Clock Signal Spacing	PCI-X Signal Length Matching
55 Ω ± 10%	5 mils width, 12 mils spacing (based on stackup assumptions in Section 3.1)	8 inches	1.5 inches	50 mils	Clocks coming from the clock driver must be length matched.

Table 96. PCI-X Frequencies

Frequency	Max Slots	Voltage
66 MHz	3	3.3 V

9.10.1 66 MHz Topologies and Trace Length

Figure 122. 66 MHz PCI-X, Two Slots, Two Down Devices Configuration

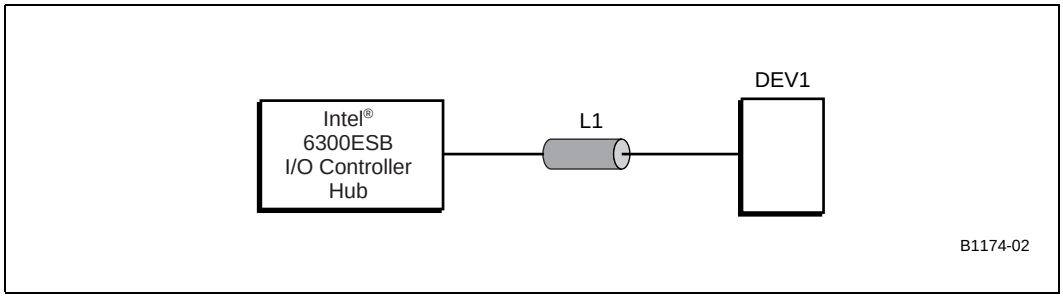


Note: For this configuration the recommended pull-up value for the PXPCICAP signal is 8.2 KΩ

Table 97. 66 MHz PCI-X, Two Slots, Two Down Devices Routing Length Parameters

Segment	Length [inches]	Total Routing Length
L1	2 – 8.0	33 inches (Including cards 0.75 - 2.75 inches)
L2	1.5 Maximum	
L3	6 Maximum	
L4, L5	8 Maximum	

Figure 123. 66 MHz PCI-X, One Down Device Configuration

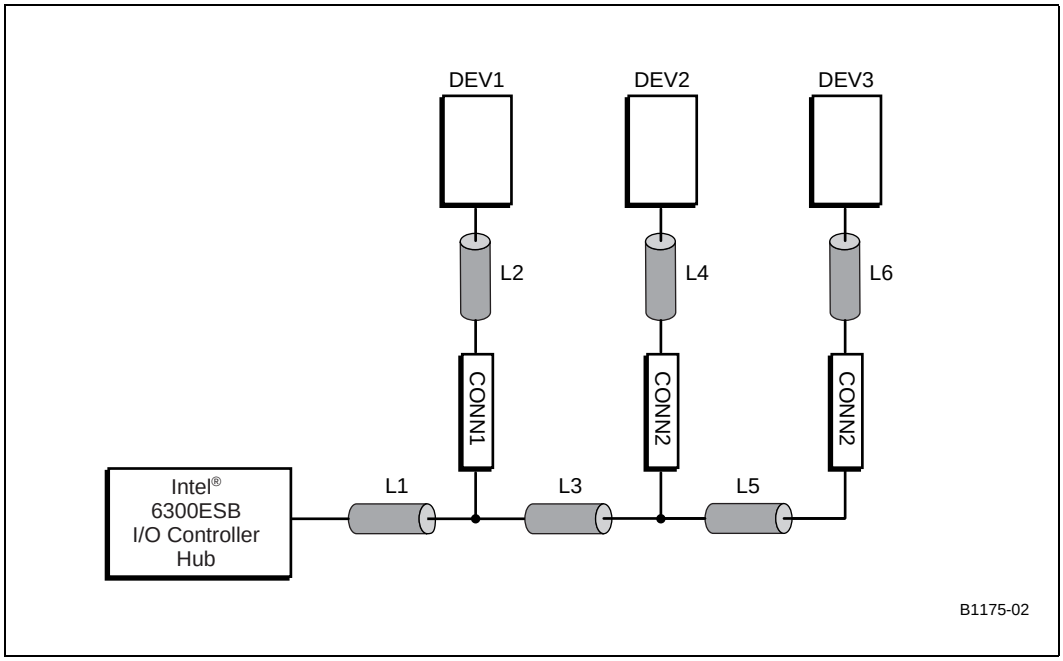


Note: For this configuration the recommended pull-up value for the PXPCICAP signal is 8.2 KΩ

Table 98. 66 MHz PCI-X, One Down Device Routing Length Parameters

Segment	Length [inches]
L1	2 – 8.0

Figure 124. 66 MHz PCI-X, Three Slot Configuration

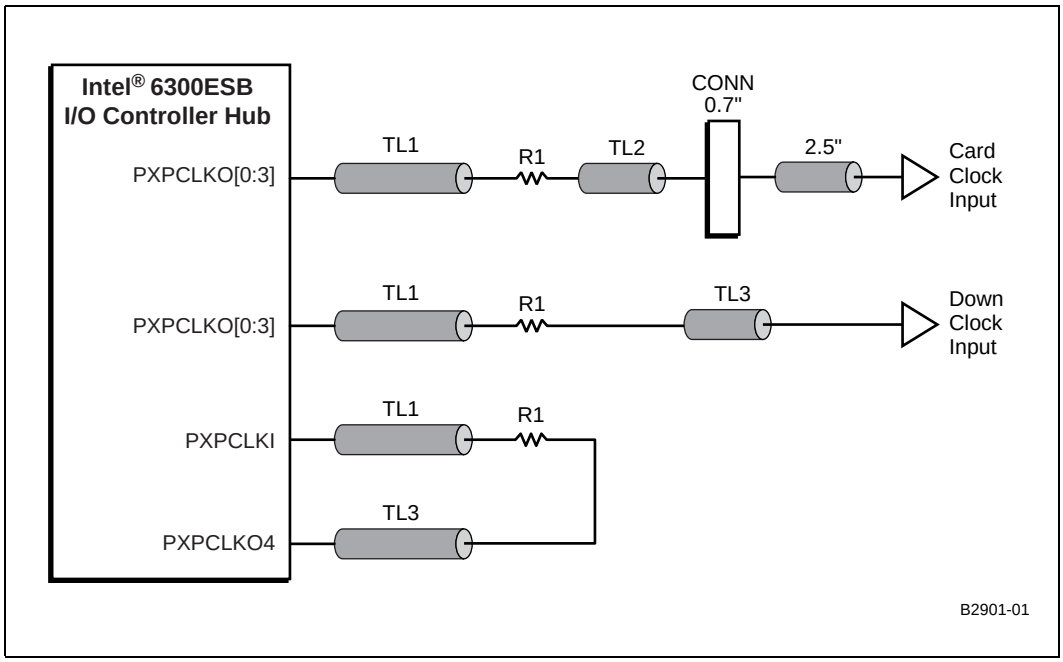


Note: For this configuration the recommended pull-up value for the PXPCICAP signal is 4.7 KΩ

Table 99. 66 MHz PCI-X, Three Slot Configuration Routing Length Parameters

Segment	Length [inches]
L1	2 – 8.0
L3, L5	1.5 Maximum
L2, L4, L6	0.75 – 2.75

Figure 125. 66 MHz Clock Signal Configuration



9.10.1.1 PCI-X Clock Length Matching Guidelines

The total path length of each clock signal must be matched to all of the other clock lines to ensure that all of the clock edges arrive at the clock inputs of the devices at the same time. Figure 125 above diagrams the general clock layout and the following formulas give the clock matching requirements.

Note: Maximum path length of any clock should be kept below 30 inches.

These guidelines account for the fact that there is some delay though the PCI-X mated connector, and through the 2.5 inches of specified trace length for the daughter cards. The PXPCLKI signal is a clock that is fed back to the 6300ESB chip as a timing reference and must be matched to the other clocks.

- The length of the sum of (TL1 + TL2) must be matched to within ± 0.1 inch between all clocks passing to PCI-X connectors.
- For down devices and the PXPCLKI feedback clock: TL1 + TL3 = TL1 + TL2 (for slots) + 3.2 inches ± 0.1 inch (the extra 3.2 inches account for the extra delay through the connector and traces of daughter cards).

9.10.2 IDSEL Series Resistor

The value for the series resistor on the IDSEL signal should be 100 Ω. No device is permitted to connect IDSEL to PXAD[16] (device number 0), since this device number is reserved for the source bridge. For systems that have add-in board connectors and connect IDSEL to the PXAD bus, the first two add-in board connectors are recommended to be connected according to Table 100 to minimize the length of the IDSEL trace.

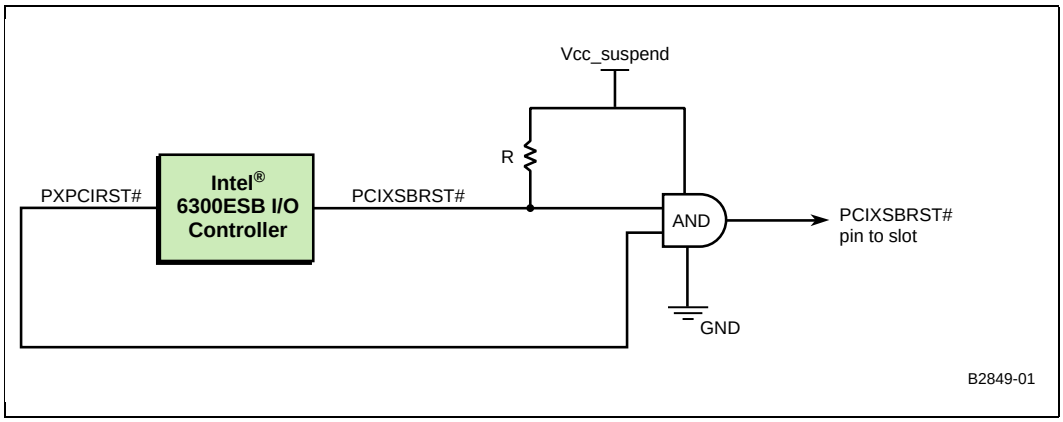
Table 100. IDSEL to PXAD Bit Assignment

Slot #	PXAD Bit	Device Number
1	17	1
2	18	2

9.10.3 PCI-X Secondary Bus Reset

The Secondary Bus Reset (SBR) function on the 6300ESB enables the user to change the mode and frequency of the PCI-X Bus without resetting the entire system. If this function is not needed in the system design refer to Section 9.10.3.1. When utilizing the SBR function an external circuit is required. Refer to Figure 126 for proper implementation:

Figure 126. Usage Model for SBR Functionality



NOTE: Recommended pull-up resistor value (R) is 100 KΩ –200 KΩ

9.10.3.1 Secondary Bus Reset Not Utilized

When the SBR function on the 6300ESB is not utilized the following should be considered:

- The SBR pin PCIXSBRST# (Ball AA7) may be left as a No Connect
- The PCI-X slots should be tied to the system reset logic (PXPCIRST#)

9.10.4 PME# Signal Sharing

In many cases the system designer will choose to share the PME# signal between the PCI-X bus and the PCI bus. While this option has been tested, certain considerations must be made when using this configuration.

9.10.4.1 Issues with Sharing PME#

Many operating systems recommend that the PME# signal is not shared when designing an optimal system. Refer to your specific operating system for issues that may occur when routing a shared PME# signal.

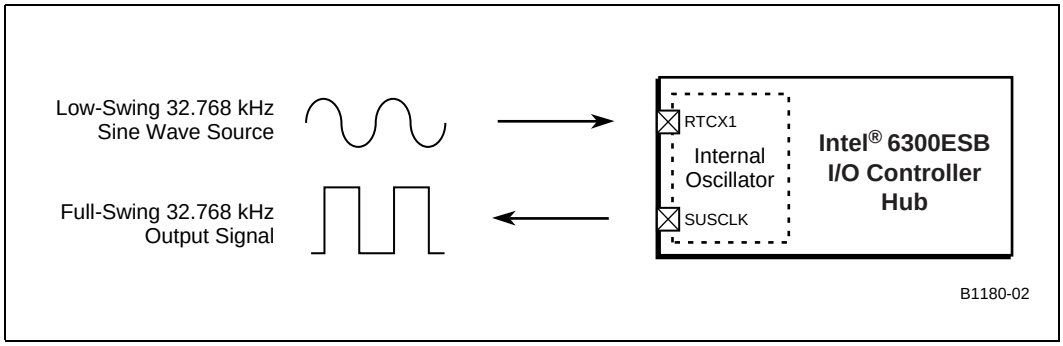
For more information on General Purpose Event (GPE) Register recommendations for Microsoft Windows* operating systems refer to the document *GPE Routing for Microsoft Windows*, which can be found at http://www.microsoft.com/whdc/hwdev/tech/onnow/GPE_routing.mspx

9.11 RTC

The 6300ESB contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The 6300ESB uses a crystal circuit to generate a low-swing 32 KHz input sine wave. This input is amplified and driven back to the crystal circuit through the RTCX2 signal. Internal to the 6300ESB, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use. This output ball of the 6300ESB is called SUSCLK. This is illustrated in Figure 127.

Figure 127. RTCX1 and SUSCLK Relationship in 6300ESB

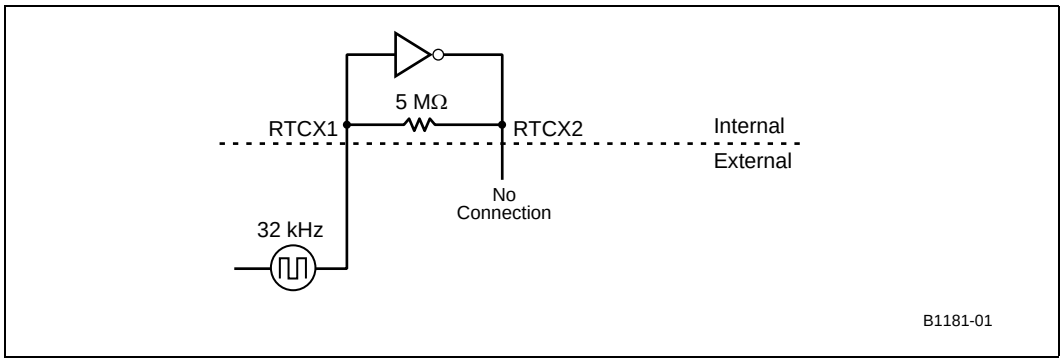


For further information on the RTC, consult Application Note AP-728 *ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*. This application note is valid for the 6300ESB.

Even when the 6300ESB internal RTC is not used, it is still necessary to supply a clock input to RTCX1 of the platform because other signals are gated off that clock in suspend modes. However, in this case, the frequency accuracy (32.768 KHz) of the clock inputs is not critical; a crystal may be used or a single clock input may be driven into RTCX1with RTCX2 left as no connect, as shown in Figure 128.

Note: This is not a validated feature on 6300ESB. Please note that the peak-to-peak swing on RTCX1 may not exceed 2.0 V.

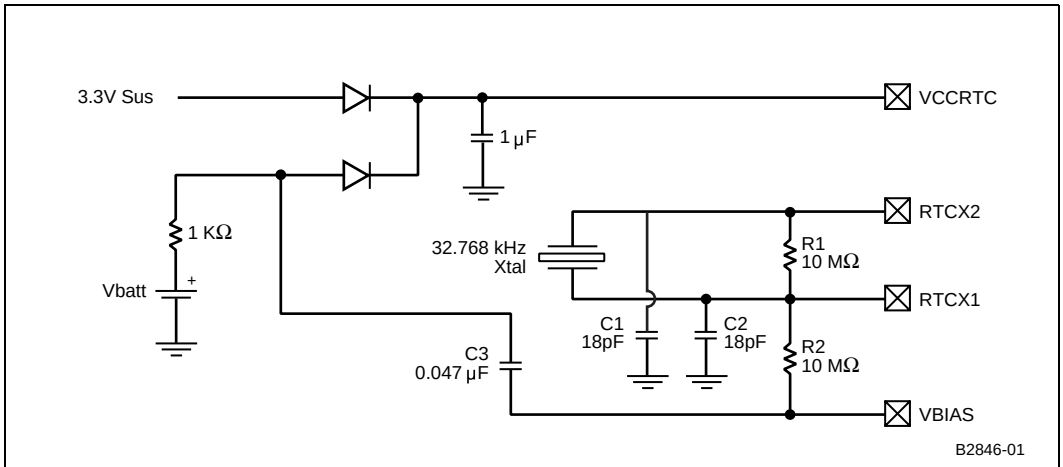
Figure 128. External Circuitry in the 6300ESB Without Use of Internal RTC



9.11.1 RTC Crystal

The 6300ESB RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 129 shows the external circuitry that comprises the oscillator of the 6300ESB RTC.

Figure 129. External Circuitry for the 6300ESB RTC



NOTES:
1. The exact capacitor values for C1 and C2 must be based on the crystal maker recommendations. Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.
2. Reference designators are arbitrarily assigned.
3. 3.3 V Sus is active whenever the system is plugged in.
4. Vbatt is voltage provided by the battery.
5. VccRTC, RTCX1, and RTCX2 are 6300ESB pins.
6. VccRTC powers the 6300ESB RTC well.
7. RTCX1 is the input to the internal oscillator.
8. RTCX2 is the feedback for the external crystal.
9. VBIAS is used to provide a reference voltage, and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.
10. Diodes must be Schottky

Table 101. RTC Routing Summary

Trace Impedance	RTC Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R1, R2, C1, and C2 tolerances	Signal Referencing
55 Ω ± 10%	5 mil trace width (results in ~2pF per inch)	1 inch	NA	R1 = 10M Ω ± 5% C1 = C2 = (NPO class) See Section 9.11.2 for calculating a specific capacitance value for C1 and C2.	Ground

9.11.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C_3 needs to be 0.047 µF and capacitor values C_1 and C_2 should be chosen to provide the manufacturer's specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation may be used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})*(C_2 + C_{in2} + C_{trace2})]/[(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

C_{load} = Crystal's load capacitance. This value may be obtained from Crystal's specification.

C_{in1}, C_{in2} = input capacitances at RTCX1, RTCX2 balls of the 6300ESB. These values may be obtained in the ICHn's data sheet.

C_{trace1}, C_{trace2} = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. A typical value, based on a 5 mil wide trace and a ½ ounce copper pour, is approximately equal to:

C_{trace} = trace length * 2 pF/inch

$C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the exist of two electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C_1, C_2 may be chosen such that $C_1 = C_2$. Using the equation of C_{load} above, the value of C_1, C_2 may be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C_2 may be chosen so that $C_2 > C_1$. Then C_1 may be trimmed to obtain the 32.768 kHz.

In certain conditions, both C_1, C_2 values may be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C_1, C_2 value are smaller then the theoretical values, the RTC oscillation frequency is higher.

The following example illustrates the use of the practical values C_1, C_2 in the case that theoretical values may not ensure the accuracy of the RTC in low temperature condition:

Example:

According to a required 12 pF load capacitance of a typical crystal that is used with the ICHn, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25° C) to yield an 32.768 kHz oscillation.

At 0° C the frequency stability of crystal gives –23 ppm (assumed that the circuit has 0 ppm at 25° C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

When the values of C_1, C_2 are chosen to be 6.8 pF instead of 10 pF, the RTC oscillates at higher frequency at room temperature (+23 ppm), but this configuration of C_1 / C_2 makes the circuit oscillate closer to 32.768 kHz at 0° C. The 6.8 pF value of C1 and 2 is the **practical value**.

Note: The temperature dependency of a crystal frequency is a parabolic relationship (ppm/degree square). The effect of changing crystal's frequency when operating at 0°C (25° below room temperature) is the same when operating at 50° C (25° C above room temperature).

9.11.3 RTC Layout Considerations

Since the RTC circuit is very sensitive and requires a highly accurate oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. The 6300ESB requires a trace length less than one inch on each branch (from crystal's terminal to RTCXn ball). Routing of the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of board's material. On FR406, a 5 mil trace has approximately 2 pF per inch.
- Trace signal coupling must be importantly reduced, by avoiding routing of adjacent PCI signals close to RTCX1, RTCX2, and VBIAS.
- Ground guard plane is highly recommended.
- The oscillator V_{CC} should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

9.11.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the 6300ESB is not powered by the system.

Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent). Batteries are rated by storage capacity. The battery life, measured in years, may be calculated by dividing the capacity by the average current required. For example, when the battery storage capacity is 220 mAh (approximate) and the average current required is 8.5 µA, the battery life will be at least:

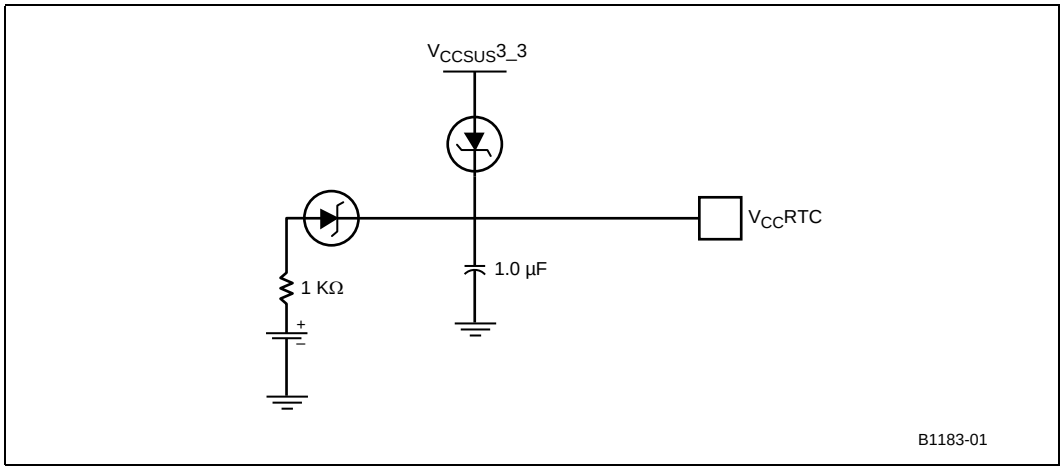
$$\sim 220{,}000\ \mu Ah / 8.5\ \mu A \cong 26{,}000h \cong 3\ years$$

Note: Refer to the 6300ESB *I/O Controller Hub Datasheet* for actual DC Current Characteristics.

The voltage of the battery may affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy may be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the 6300ESB through an isolation Schottky diode circuit. The Schottky diode circuit allows the 6300ESB RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 130 is an example of a diode circuit that is used.

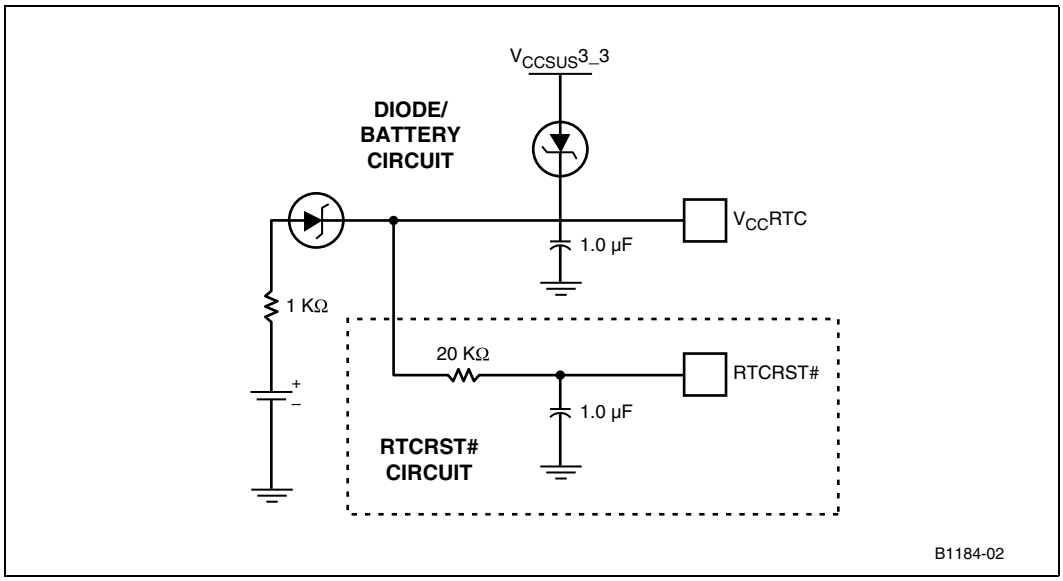
Figure 130. Diode Circuit to Connect RTC External Battery



A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which increases the RTC battery life and thereby the RTC accuracy.

9.11.5 RTC External RTCRST# Circuit

Figure 131. RTCRST# External Circuit for the 6300ESB RTC



The 6300ESB RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18-25 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

The RTCRST# signal may also be used to detect a low battery voltage. RTCRST# will be asserted during a power up from G3 state if the battery voltage is below 2 V. This sets the RTC_PWR_STS bit as described above. When desired, BIOS may request that the user replace the battery.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 130) to allow the RTC well to be powered by the battery when the system power is not available. Figure 131 is an example of this circuitry that is used in conjunction with the external diode circuit.

9.11.6 V_{BIAS} DC Voltage and Noise Measurements

V_{BIAS} is a DC voltage level necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC Network of R2 and C3 (see Figure 129); therefore, it is a self-adjusted voltage. Board designers should not manually bias the voltage level on V_{BIAS}. Checking V_{BIAS} level is used for testing purposes only to determine the right bias condition of the RTC circuit.

V_{BIAS} should be at least 200 mV DC. The RC network of R2 and C3 will filter out most of AC signal that exist on this ball, however, the noise on this ball should be kept minimal in order to ensure the stability of the RTC oscillation.

Probing V_{BIAS} requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). See Application Note AP-728 for further details on measuring techniques.

Note: V_{BIAS} is also very sensitive to environmental conditions.

9.11.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), the SUSCLK duty cycle may be between 30-70%. When the SUSCLK duty cycle is beyond 30-70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK may be probed directly using normal probe (50 Ω input impedance probe). It is an appropriated signal you may use to check the RTC frequency to determine the accuracy of the 6300ESB's RTC Clock (see Application Note AP-728 for further details).

9.11.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to V_{CC}RTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in Figure 131 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to V_{CC}RTC. This prevents these nodes from floating in G3, and correspondingly prevents I_{CC}RTC leakage that may cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

9.12 Serial I/O

The 6300ESB supports two Serial I/O ports. For proper functionality of the Serial I/O ports ensure the clock input (UART_CLK) has the correct value.

System designers have two options for the input clock:

- 48 MHz -*Recommended*
- 14.745 MHz

Warning: If using the 14.745 MHz option, ensure it is **14.745** MHz. Any deviation from this value, such as using a common system clock (14.318 MHz), will cause improper functioning of the Serial I/O.

Note: A 48 MHz clock input is the recommended value to ease system design. A CK409 has an 48 MHz clock available so no other clock source for the Serial I/O would be necessary.

9.12.1 Serial I/O Interface Not Utilized

When the Serial I/O is not utilized in the system, all associated pins may be left as No Connect.

Note: SIU_DTR# is a strap pin. To utilize the strap feature (TOP Swap) a pull-down to ground is necessary. Refer to the 6300ESB *Datasheet* for more details.

9.13 FWH

9.13.1 FWH Vendors

The following vendors manufacture firmware hubs that conform to the *Intel® FWH Specification*. Contact the vendor directly for information on packaging and density.

SST http://www.sst.com/
STM http://www.st.coml
ATMEL http://www.atmel.com

9.13.2 FWH Decoupling

A 0.1 µF capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the V_{CC} supply pins.

9.13.3 In-circuit FWH Programming

All cycles destined for the FWH appear on PCI. The 6300ESB Hub Interface to PCI Bridge places all CPU boot cycles out on PCI (before sending them out on the FWH interface). When the 6300ESB is set for subtractive decode, these boot cycles may be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. In order to boot from a PCI card, it is necessary to keep the 6300ESB in subtractive decode mode. When a PCI boot card is inserted and the 6300ESB is programmed for positive decode, there are two devices positively decoding the same cycle.

9.13.4 FWH INIT# Voltage Compatibility

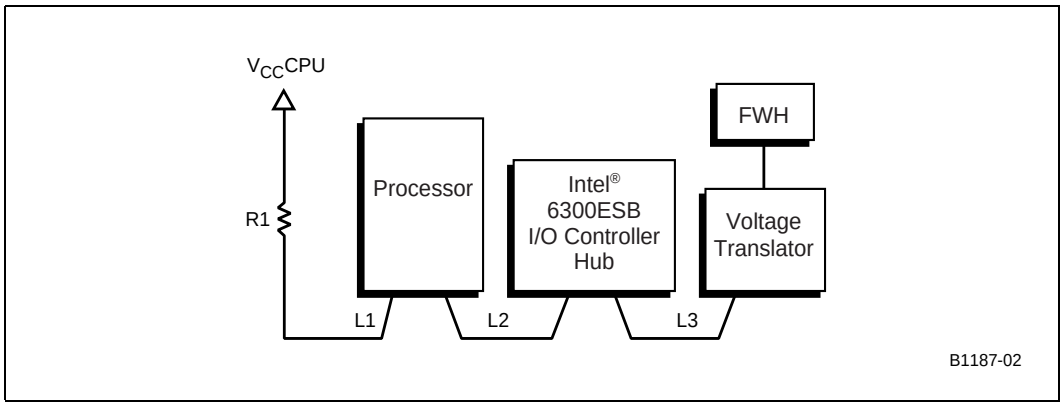
The FWH INIT# signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the 6300ESB INIT# signal needs to be at a value slightly higher than the V_{IH} min FWH INIT# pin specification. The 6300ESB inactive state of this signal is typically governed by the formula:

$$V\_CPU\_IO\ min - noise\ margin \geq V_{IH}min$$

Therefore, if the V_CPU_IO min of the processor is 1.6 V, the noise margin is 200 mV and the V_{IH} min spec of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because 1.6 V - 0.2 V = 1.40 V which is greater than the 1.35 V minimum of the FWH. If the V_{IH} min of the FWH was 1.45 V, then there would be an incompatibility and level translation would need to be used. These examples do not take into account actual noise that may be encountered on INIT#. Care must be taken to ensure that the V_{IH} min. specification is met with ample noise margin.

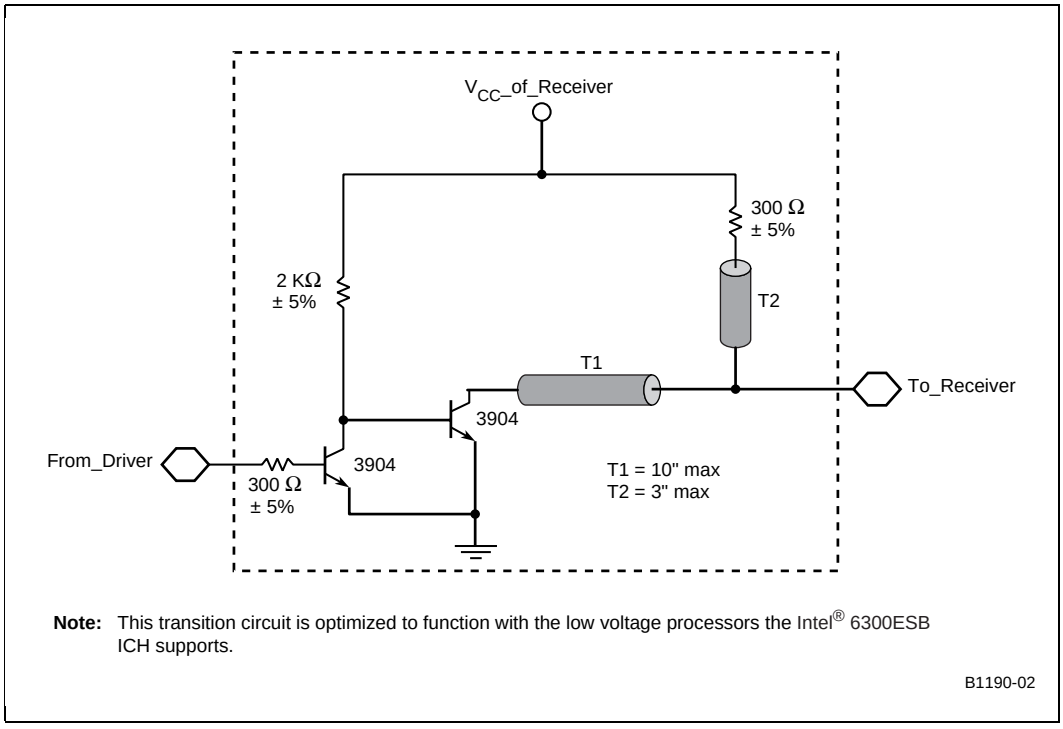
The following solutions assume that level translation is necessary. The figure below implements the INIT# signal UP (Figure 132) topology solution for the 6300ESB, FWH and the CPU. The level translator circuitry is shown in Figure 133.

Figure 132. FWH/CPU UP Signal Topology Solution



NOTE: The recommended value for R1 depends on the Processor used in the system. See the Processor design guidelines for more info.

Figure 133. FWH Level Translation Circuitry



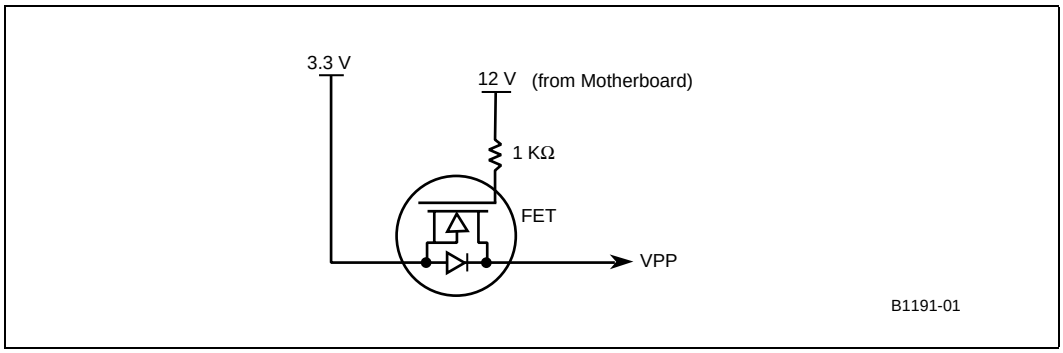
Note: This transition circuit is optimized to function with the low voltage processors the Intel® 6300ESB ICH supports.

9.13.5 FWH V_{PP} Design Guidelines

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports V_{PP} of 3.3 V or 12 V. When V_{PP} is 12 V, the flash cells programs about 50% faster than at 3.3 V. However, the FWH only supports 12 V V_{PP} for 80 hours (3.3 V on Vpp does not affect the life of the device). The 12 V V_{PP} would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The V_{PP} pin MUST be tied to 3.3 V on the motherboard. (See Figure 134.)

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 134. FWH VPP Isolation Circuitry



9.14 GPIO Summary

The 6300ESB platform has 12 general purpose inputs, 9 general purpose outputs, and 16 general purpose inputs/outputs.

Table 102. GPIO Summary (Sheet 1 of 2)

GPIO Number	Power Well	Input-Output	Tolerance	If Not Used
0	Core	Input	3.3 V	Recommend an 8.2 KΩ pull-up resistor to $V_{CC}3.3$
1	Core	Input	3.3 V	
2	Core	Input	5 V	Recommend an 8.2 KΩ pull-up resistor to $V_{CC}3.3$ or a 2.7 KΩ pull-up resistor to $V_{CC}5$
3	Core	Input	5 V	
4	Core	Input	5 V	
5	Core	Input	5 V	
6	Core	Input	3.3 V	Recommend an 8.2 KΩ pull-up resistor to $V_{CC}3.3$
7	Core	Input	3.3 V	
8	Resume	Input	3.3 V	Recommend an 8.2 KΩ pull-up resistor to $V_{CCSus}3.3$
11	Resume	Input	3.3 V	
12	Resume	Input	3.3 V	
13	Resume	Input	3.3 V	

Table 102. GPIO Summary (Sheet 2 of 2)

GPIO Number	Power Well	Input-Output	Tolerance	If Not Used
16	Core	Output	3.3 V	May leave as no connect
17	Core	Output	3.3 V	
18	Core	Output	5 V	
19	Core	Output	5 V	
20	Core	Output	5 V	
21	Core	Output	5 V	
23	Core	Output	5 V	
24	Resume	Input-Output†	3.3 V	
25	Resume	Input-Output†	3.3 V	
27	Resume	Input-Output†	3.3 V	
28	Resume	Input-Output†	3.3 V	
32	Core	Input-Output†	3.3 V	
33	Core	Input-Output†	3.3 V	
34	Core	Input-Output†	3.3 V	
35	Core	Input-Output†	3.3 V	
36	Core	Input-Output†	3.3 V	
37	Core	Input-Output†	3.3 V	May leave as no connect
38	Core	Input-Output†	3.3 V	
39	Core	Input-Output†	3.3 V	
40	Core	Input-Output†	3.3 V	
41	Core	Input-Output†	3.3 V	
42	Core	Input-Output†	3.3 V	
43	Core	Input-Output†	3.3 V	
56	RTC	Output	3.3 V	
57	RTC	Output	3.3 V	

† Defaults as an Output to the 6300ESB.

9.15 Power Management

9.15.1 SYS_RESET# Usage Model

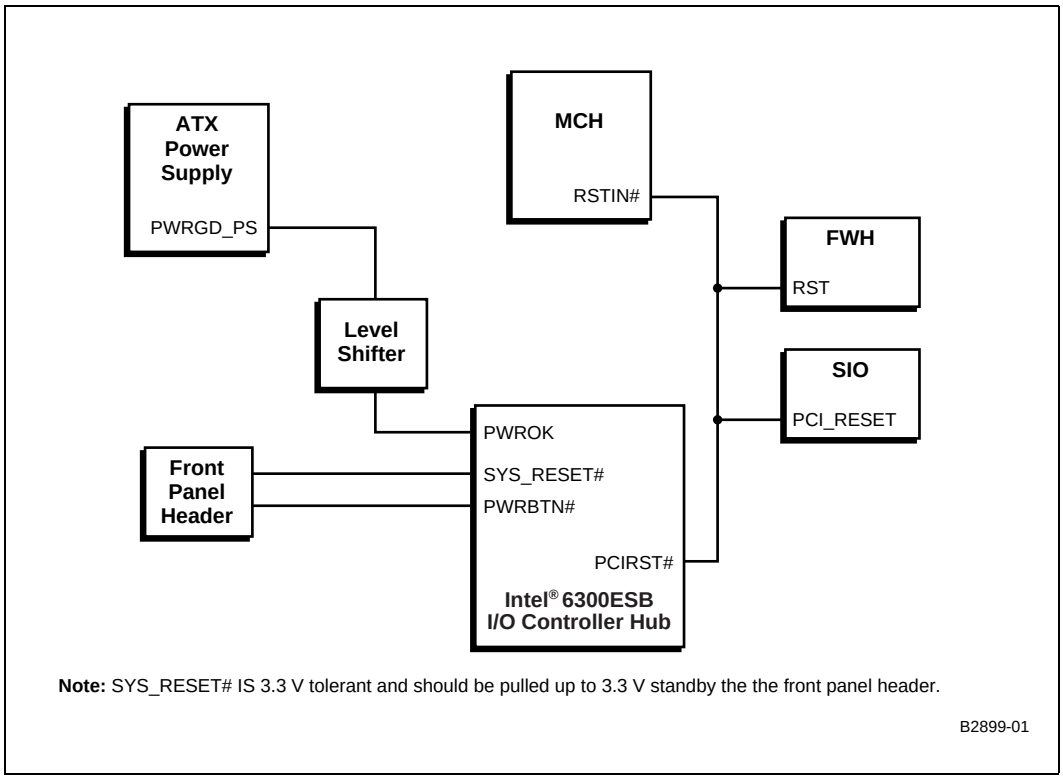
The System Reset ball (SYS_RESET#) on the 6300ESB may be connected directly to the reset button on the system front panel, provided that the front panel header pulls this signal up to 3.3 V standby through a weak pull-up resistor. The 6300ESB will debounce signals on this pin (16 ms) and allow the SMBus to go idle before resetting the system. This helps to prevent a slave device on the SMBus from hanging by resetting in the middle of a cycle.

Note: The PWORK signal should not be used to implement front panel reset.

9.15.2 PWRBTN# Usage Model

The Power Button ball (PWRBTN#) on the 6300ESB may be connected directly to the power button on the system front panel. This signal is internally pulled-up in the 6300ESB to 3.3 V standby through a pull-up resistor (24 KΩ nominal). The 6300ESB has 16 ms of internal debounce logic on this pin.

Figure 135. SYS_RESET# and PWRBTN# Connection

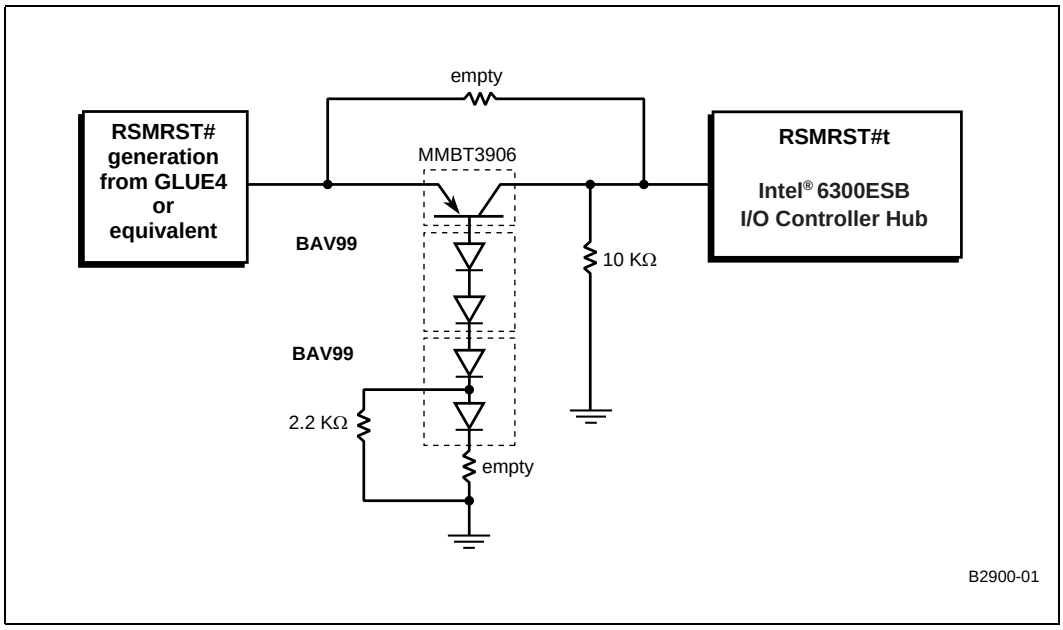


9.15.3 Power-Well Isolation Control Strap Requirements

Note: The RSMRST# signal of the 6300ESB must transition from 20% signal level to 80% signal level and vice-versa within 50uS.

The circuit shown in Figure 136 may be implemented to control well isolation between the VccSUS3.3 and RTC power-wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail. Failure to implement this circuit or a circuit that functions similar to this may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power). Droop on this node may potentially cause the CMOS to be cleared or corrupted, the RTC to lose time after several AC power cycles, or the intruder bit might assert erroneously.

Figure 136. RTC Power Well Isolation Control



Miscellaneous Logic 10

The 6300ESB requires additional external circuitry to function properly. Some of these functionalities include meeting timing specifications, buffering signals, and switching between power wells. This logic may be implemented through the use of the Glue Chip* or discrete logic.

10.1 Glue Chip 4*

To reduce the component count and BOM (Bill of Materials) cost of the 6300ESB platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The 6300ESB Glue Chip is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost may be reduced.

Features include:

- Dual, strapping, selectable feature sets
- Audio-disable circuit
- Mute audio circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK (PWRGD_3V) signal generation
- Power sequencing/BACKFEED_CUT
- Power supply turn on circuitry
- RSMRST# generation
- Voltage translation from DDC to VGA monitor
- HSYNC/VSYNC voltage translation to VGA monitor
- Tri-state buffers for test
- Extra GP logic gates
- Power LED drivers
- Flash FLUSH#/INIT# circuit

More information regarding this component is available from the vendors presented in Table 103.

Table 103. Glue Chip 4 Vendor Information

Vendor	Contact Information	Vendor Part Number
Philips Semiconductor*	http://www.semiconductors.philips.com	PCA9504A
Fujitsu Microelectronics*	http://www.fujitsumicro.com	MB87B302ABPD-G-ER

10.2 Discrete Logic

As an alternative solution, discrete circuitry may be implemented into a design instead of using the Glue Chip.

Platform Clock Routing Guidelines 11

11.1 System Clock Groups

The system clocks are considered as a subsystem in themselves. At the center of this subsystem is the clock synthesizer/driver component. Several vendors offer suitable products, as defined in the *Intel CK409 Synthesizer/Driver Specification*. This device provides the set of clocks required to implement a platform-level motherboard solution. Table 104 presents a breakdown of the various individual clocks.

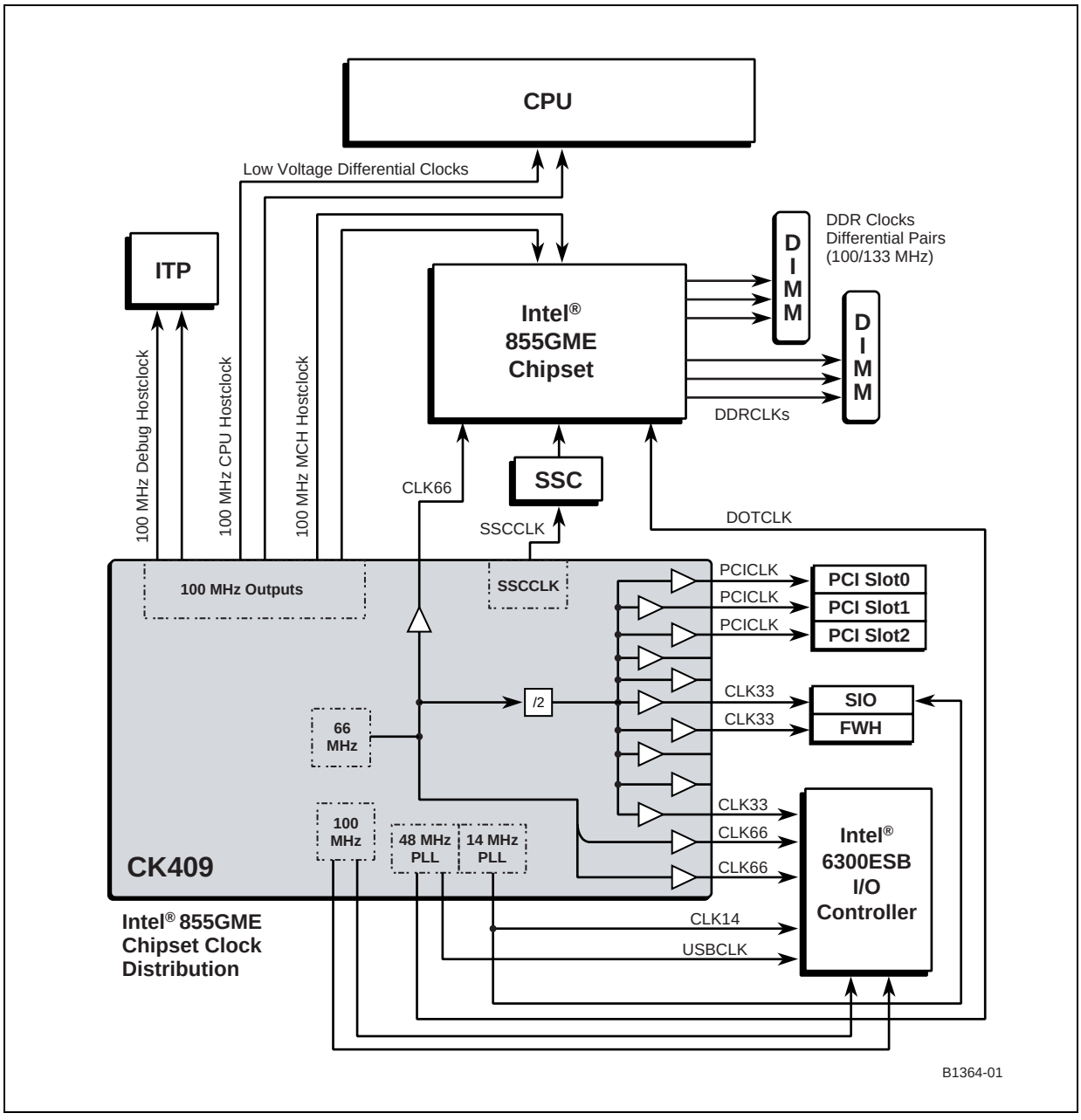
Note: When used in Intel® 855GME chipset platforms, the CK409 is configured in the unbuffered mode and a host clock swing of 710 mV.

Table 104. Individual Clock Breakdown

Clock Group	Frequency	Driver/Pin	Receiver/s	Comments
HOST_CLK	100 MHz	CK409 CPU[2:0]	CPU GMCH Debug Port	Length matched Differential signaling
CLK66	66 MHz	CK409 3V66[5:0]	GMCH Intel® 82801DB I/O Controller Hub 4 (ICH4)	Length matched
CLK33	33 MHz	CK409 PCIF[2:0] PCI[6:0]	ICH4 SIO FWH	Length matched to CLK66 Synchronous but not edge aligned with CLK66 Phase delay of 1.5 ns to 3.5 ns
PCICLK (Expansion)	33 MHz	CK409 PCI[6:0] PCIF[2:0]	PCI Conn #1 PCI Conn #2 PCI Conn #3	Length matched to CLK33 CLK33 length minus 2.5 inches
CLK14	14 MHz	CK409 REF0	ICH4 SIO	Independent clock
DOTCLK	48 MHz	CK409 48 MHz	GMCH	Independent clock
SSCCLK	48/66 MHz	CK409 VCH	GMCH	Independent clock
USBCLK	48 MHz	CK409 48 MHz	ICH4	Independent clock

Figure 137 depicts the system clock subsystem including the clock generator, major platform components, and all the related clock interconnects.

Figure 137. Clock Distribution Diagram



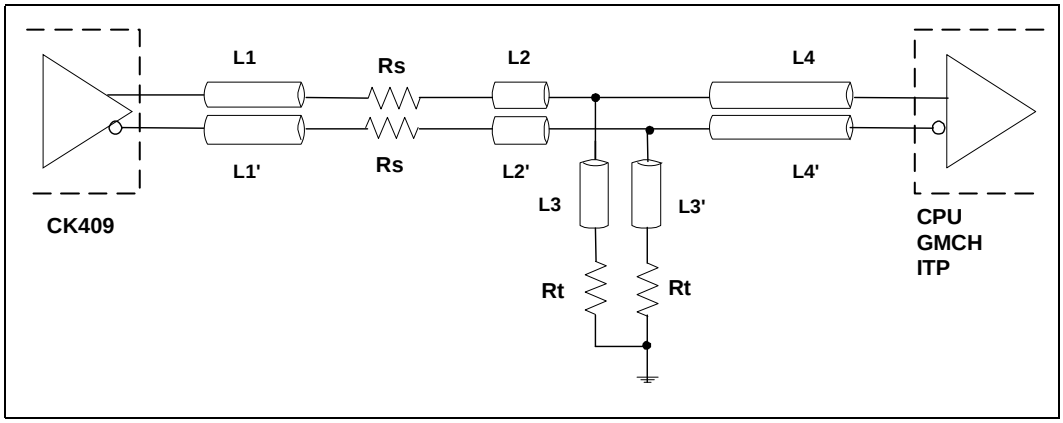
11.2 Clock Group Topologies and Routing Constraints

The topology diagrams and routing constraint tables provided on the following pages define the recommended topology and routing rules for each of the platform level clocks. These topologies and rules have been simulated and verified to produce the required waveform integrity and timing characteristics for reliable platform operation.

11.2.1 Host Clock Group

The clock synthesizer provides three pairs of 100 MHz differential clock outputs using a 0.7 V voltage swing. The 100 MHz differential clocks are driven to the Intel® Pentium® M processor, the GMCH, and the processor debug port with the topology shown in Figure 138. The host clocks are routed point-to-point as closely coupled differential pairs on the motherboard, with dedicated buffers for each of the three loads. These clocks utilize a source shunt termination scheme as shown below.

Figure 138. Source Shunt Termination Topology



The clock driver differential bus output structure is a Current Mode Current Steering output, which develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt. The resulting amplitude is determined by multiplying IOUT by the value of Rt. The current IOUT is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of Rt to match impedances or to accommodate future load requirements.

The recommended termination for the differential bus clock is a Source Shunt termination. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

The recommended value for Rt is a 49.9 Ω ± 1% resistor. The tight tolerance is required to minimize crossing voltage variance. The recommended value for Rs is 33 Ω ± 5%. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

The IREF pin (CK409 pin #52) should be tied to ground through a 475 Ω ± 1% resistor, making the IREF 2.32 mA. Table 105 presents the host clock group routing constraints.

Table 105. Host Clock Group Routing Constraints

Parameter	Definition
Class Name	HOST_CLK
Class Type	Individual Differential Pairs
Topology	Differential Source Shunt Terminated
Reference Plane	Ground Referenced (contiguous over length)
Single Ended Trace Impedance (Zo)	55 Ω ±15%
Differential Mode Impedance (Zdiff)	100 Ω ±15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Inner Layer Pair Spacing (edge to edge) (except as allowed below)	7.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Nominal Outer Layer Pair Spacing (edge to edge) (except as allowed below)	5.0 mils
Minimum Spacing to Other Signals	25 mils
Serpentine Spacing	25 mils
Maximum Via Count	5 (per side)
Series Termination Resistor Value	33 Ω ±5%
Shunt Termination Resistor Value	49.9 Ω ±1%
Trace Length Limits – L1 & L1’	Up to 500 mils
Trace Length Limits – L2 & L2’	Up to 200 mils
Trace Length Limits – L3 & L3’	Up to 500 mils
Trace Length Limits – L4 & L4’	2.0” to 8.0”
Total Length Range– L1 + L2 + L4	2.0” to 8.5”
Length Matching Required	Yes (Pin to Pad)
HCLK to HCLK# Length Matching	± 10 mils (per segment) ± 10 mils (overall)
CPU Clock to GMCH Clock Length Matching	Match HCLKs (pin to pad) ± 20 mils Match L1 segment to ± 10 mils across all pairs. Refer to Section 11.2.1.2 for more information.
Breakout Region Exceptions	No breakout exceptions allowed.

NOTES:
1. Differential pairs should be routed as a closely coupled side-by-side pair on a single layer over their entire length.
2. To minimize skew it is recommended that all clocks be routed on a single layer. If clock pairs are to be routed on multiple layers, the routed length on each layer should be equalized across all clock pairs.
3. To minimize skew it is recommended that all clock pairs be length matched from CK409 pin to CPU and GMCH die-pad, and length compensated on the motherboard for differences in package length and for socket/interposer effective length. A table of package lengths and equivalent socket length is provided.
4. The motherboard length of the ITP connector clock pair should be matched to the motherboard length of the CPU clock pair plus the length of the BPM#[4:0] signals, within ± 50 ps.

11.2.1.1 Host Clock Group General Routing Guidelines

When routing the 100 MHz differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.

If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.

Do not place vias between adjacent complementary clock traces. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

11.2.1.2 Clock-to-Clock Length Matching and Compensation

The HCLK pairs to the CPU and GMCH should be matched as close as possible in total length from CK409 pin to the die-pad of the receiving device. In addition, the L1/L1' segments of all three clock pairs should be length matched to within ±10 mils. Pair-to-pair overall length matching requires knowledge of the package lengths of various CPUs, and the GMCH, as well as the effective length of the CPU socket/interposer if used. This information is provided in Table 106.

After routing lengths are defined for the CPU and GMCH, match the motherboard length of the ITP clock pair to the motherboard length of the CPU clock pair.

Table 106. Clock Package Length

Parameter	Length
Intel® Pentium® M Processor Package Length	BCLK0: 447 mils BCLK1: 447 mils
Intel® 855GME chipset GMCH Package Length	BCLK: 1138 mils BCLK#: 1145 mils
CPU Socket Equivalent Length	157 mils

11.2.1.3 EMI Constraints

Clocks are a significant contributor to EMI and should be treated with care. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to the VSS reference plane only.

11.2.2 CLK66 Clock Group

The 66 MHz clocks are series terminated and routed point-to-point on the motherboard, with dedicated buffers for each of the loads. These clocks are all length tuned to match each other and the CLK33 clocks. Figure 139 depicts the CLK66 clock group topology. Table 107 presents the CLK66 clock group routing constraints.

Figure 139. CLK66 Clock Group Topology

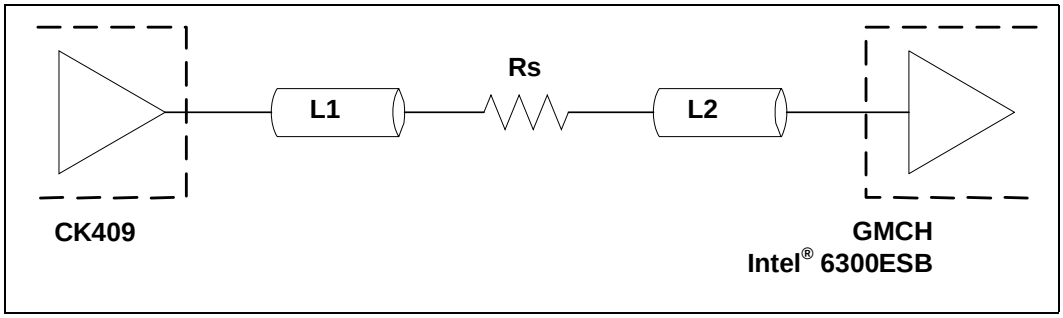


Table 107. CLK66 Clock Group Routing Constraints

Parameter	Definition
Class Name	CLK66
Class Type	Individual Nets
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ±15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4 (per side)
Series Termination Resistor Value	33 Ω ±5%
Trace Length Limits – L1	Up to 500 mils (breakout segment)
Trace Length Limits – L2	4.0” to 8.5”
Total Length Range – L1 + L2	4.0” to 9.0”
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	±100 mils CLK66 to CLK66
Breakout Region Exceptions. (Reduced spacing for GMCH and ICH breakout region)	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

NOTE: The overall length of CLK66 is considered the reference length for CLK66 and CLK33, except USBCLK and CLK14. The length of this clock should be set within the range and then used as the basis for defining the length of all other length matched clocks.

11.2.3 CLK33 Clock Group

The 33 MHz clocks are series terminated and routed point-to point on the motherboard with dedicated buffers for each of the loads. These clocks are length tuned to match the CLK66 clocks, however, they are out of phase due to an internal phase delay in the CK409. Figure 140 depicts the CLK33 group topology. Table 108 presents the CLK33 clock group routing constraints.

Figure 140. CLK33 Group Topology

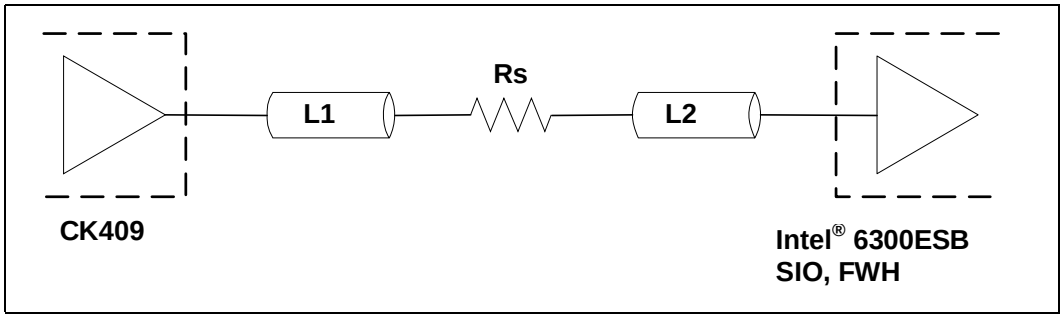


Table 108. CLK33 Clock Group Routing Constraints

Parameter	Definition
Class Name	CLK33
Class Type	Individual Nets
Topology	Series Terminated Point-to-Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ±15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ±5%
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	4.0” to 8.5”
Total Length Range – L1 + L2	CLK66 Length
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Matching	±100 mils CLK33 to CLK33 to CLK66
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

11.2.4 PCI Clock Group

The PCI clocks are series terminated and routed point-to-point as on the motherboard between the CK409 and the PCI connectors with dedicated buffers for of the three slots. These clocks are synchronous to the CLK33 clocks and are length tuned to compensate for the segment on the PCI daughtercard. Figure 141 depicts the PCI clock group topology. Table 109 presents the PCICLK clock group routing constraints.

Figure 141. PCI Clock Group Topology

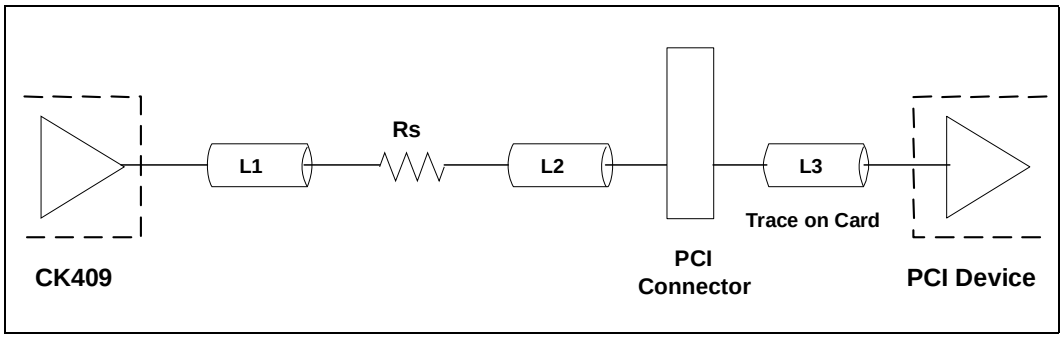


Table 109. PCICLK Clock Group Routing Constraints

Parameter	Definition
Class Name	PCICLK
Class Type	Individual Nets
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ±15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ±5%
Trace Length Limits – L1	Up to 500 mils (breakout segment)
Trace Length Limits – L2	1.5” to 8.0”
Trace Length Limits – L3	2.5” (as per PCI specification)
Total Length Range – L1 + L2	CLK33 – 2.5” (for nominal matching)
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	±2.0” PCICLK to PCICLK to (CLK33 – 2.5”)
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

11.2.5 CLK14 Clock Group

The 14 MHz clocks are series terminated and routed point-to-point on the motherboard. A single clock output is shared between the two loads. These clocks are length tuned to each other but are not synchronous with any other clocks. Figure 142 depicts the CLK14 clock group topology. Table 110 presents the CLK14 clock group routing constraints.

Figure 142. CLK14 Clock Group Topology

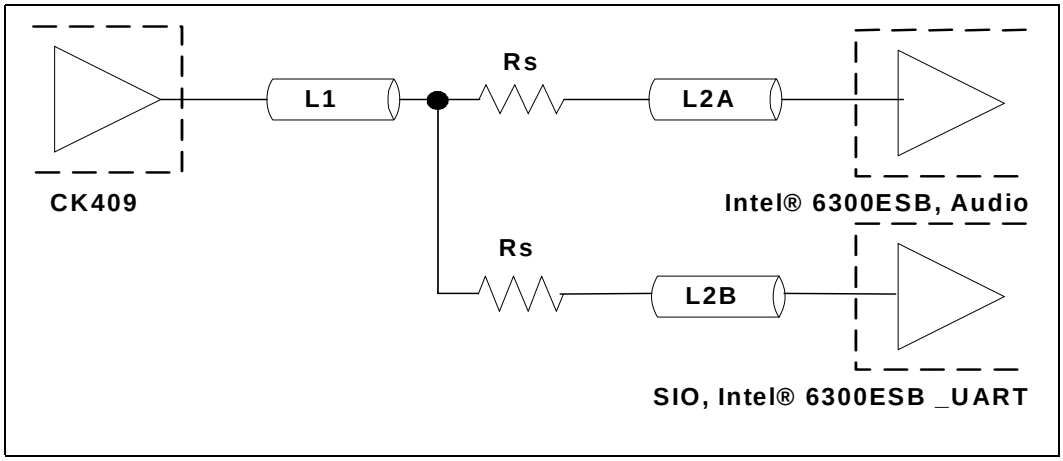


Table 110. CLK14 Clock Group Routing Constraints

Parameter	Definition
Class Name	CLK14
Class Type	Individual Nets
Topology	Dual Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ±15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4 (per driver/receiver path)
Series Termination Resistor Value	33 Ω ±5%
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2A, L2B	2.0” to 8.5”
Total Length Range – L1 + L2A & L1 + L2B	2.0” to 9.0”
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	±500 mils CLK14A to CLK14B
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

11.2.6 DOTCLK Clock Group

The 48 MHz DOTCLK is series terminated and routed point-to-point on the motherboard. This clock operates independently and is not length-tuned to any other clock. Figure 143 depicts the DOTCLK clock topology. Table 111 presents the DOTCLK clock routing constraints.

Figure 143. DOTCLK Clock Topology

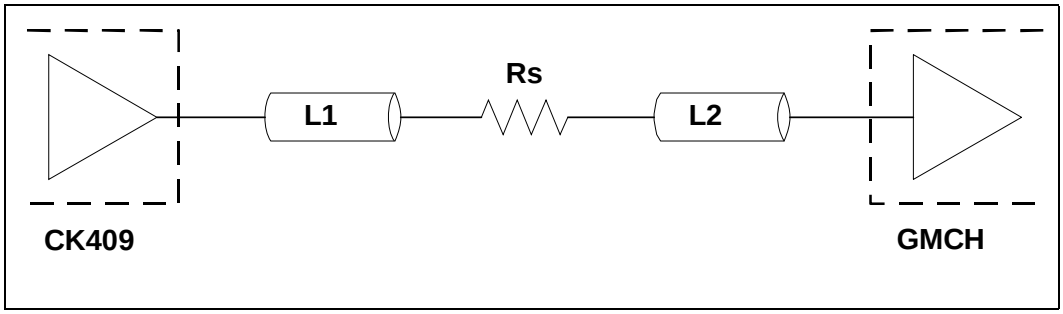


Table 111. DOTCLK Clock Routing Constraints

Parameter	Definition
Class Name	DOTCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	25 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ± 5%
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	2.0” to 8.0”
Total Length Range – L1 + L2	2.0” to 8.5”
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

NOTE: The DOTCLK is used internally by the GMCH to generate the pixel clock and must exhibit very low jitter. Care should be taken to avoid routing through noisy areas and spacing rules should be observed. Guard traces may be employed if necessary with ground stake vias on no less than 0.5- inch intervals.

11.2.7 SSCCLK Clock Group

The 48/66 MHz SSCCLK operates independently and is not length tuned to any other clock. This clock employs a spread-spectrum device in its path to reduce EMI. The overall clock path is divided into two segments as shown in Figure 144, with each segment series terminated and routed point-to-point. Table 112 presents the SSCCLK clock routing constraints.

Figure 144. SSCCLK Clock Topology

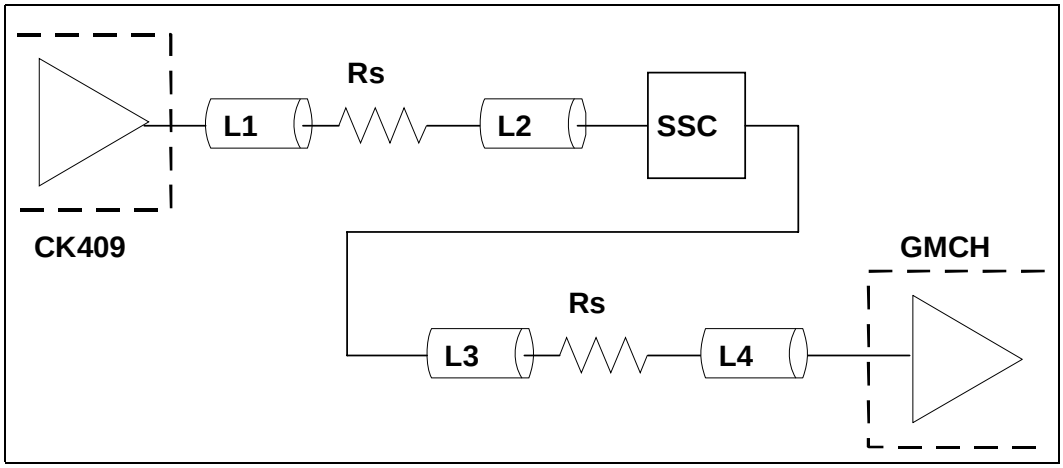


Table 112. SSCCLK Clock Routing Constraints

Parameter	Definition
Class Name	SSCCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ±15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Maximum Via Count	4 (per driver/receiver path)
Series Termination Resistor Value	33 Ω ±5%
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	1.0” to 4.0”
Trace Length Limits – L3	Up to 500 mils
Trace Length Limits – L4	1.0” to 7.0”
Total Length Range – L1 + L2 + L3 + L4	3.0” to 8.5”
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

11.2.8 USBCLK Clock Group

The 48 MHz USBCLK is series terminated and routed point-to-point on the motherboard. This clock operates independently and is not length tuned to any other clock. Figure 145 depicts the USBCLK clock topology. Table 113 presents the USBCLK clock routing constraints.

Figure 145. USBCLK Clock Topology

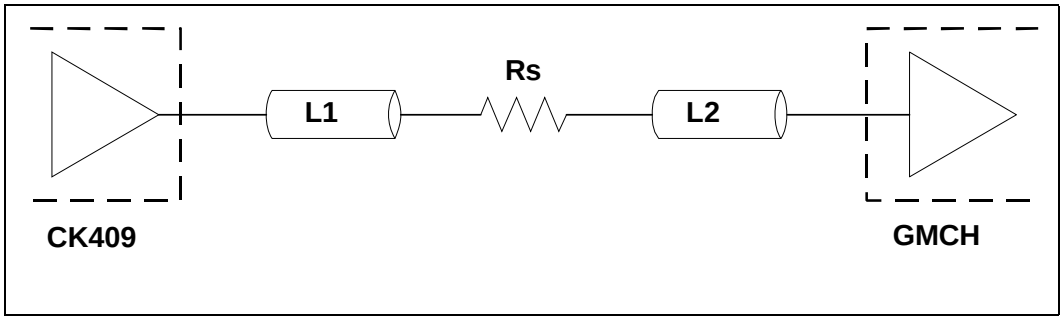


Table 113. USBCLK Clock Routing Constraints

Parameter	Definition
Class Name	USBCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω ± 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (See exceptions below.)	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω ± 5%
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	3.0” to 12.0”
Total Length Range – L1 + L2	3.0” to 12.5”
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

11.2.9 SRC Clock Group

11.2.9.1 SRC Clock Topology

The clock synthesizer provides one set of 100-MHz differential clock outputs. The differential clocks are driven to the Intel® Pentium® M Processor and Embedded Intel® 855GME Chipset with Intel® 6300ESB I/O Controller Hub for serial-ATA as shown in Figure 137.

The clock driver differential bus output structure is a Current Mode Current Steering output that develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt.

The recommended termination for the differential bus clock is a Shunt Source Termination. See Figure 146 for an illustration of this terminology scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver's output parasitics which would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be 49 Ω and Rs should be 33 Ω. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

Figure 146. Source Shunt Termination

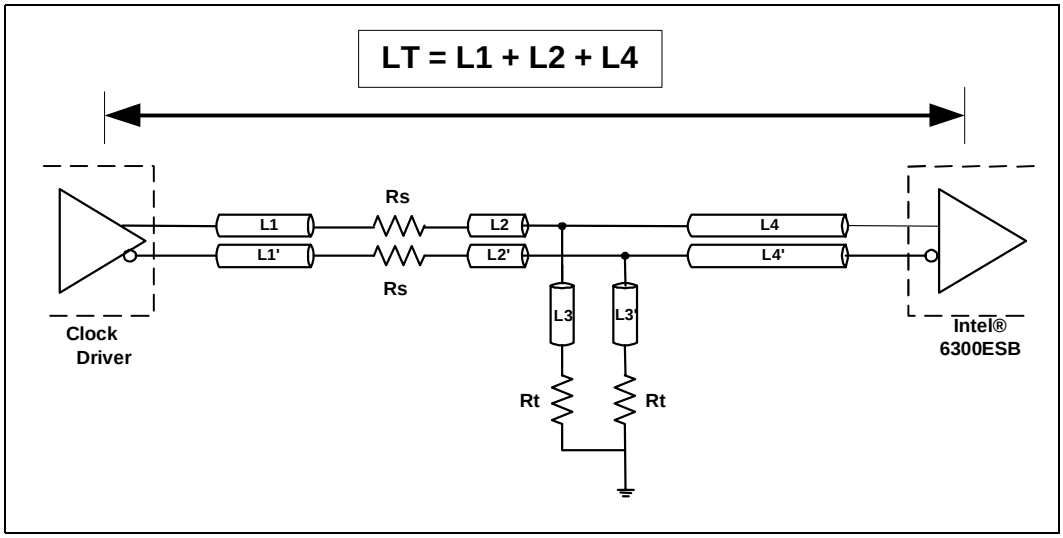


Table 114. SCR/SCR# Routing Guidelines (Sheet 1 of 2)

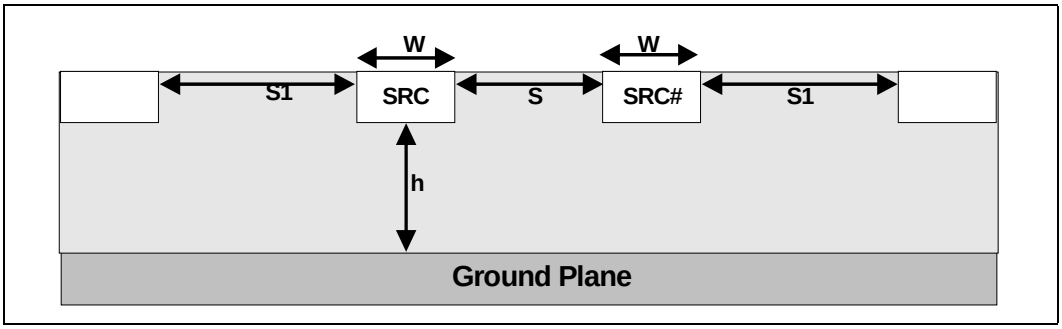
Layout Guideline	Value	Illustration	Notes
Trace Width	5 mils	Figure 147	
Differential Pair Spacing	11 mils	Figure 147	1, 2, 3
Spacing to Other Traces	25 mils	Figure 147	
Serpentine Spacing	Maintain a minimum 25 mils. Keep parallel serpentine sections as short as possible. Minimize 90-degree bends. Make 45-degree bends, if possible.		

Table 114. SCR/SCR# Routing Guidelines (Sheet 2 of 2)

Layout Guideline	Value	Illustration	Notes
Motherboard Impedance – Differential	100 Ω typical		4
Routing Length – L1, L1': Clock Driver to Rs	0.5 inch max	Figure 146	6, 7
Routing Length – L2, L2': Rs to Rs-Rt Node	0 – 0.2 inch	Figure 146	6, 7
Routing Length – L3, L3': Rs-Rt Node to Rt	0 – 0.2 inch	Figure 146	6, 7
Routing Length – L4, L4': Rs-Rt Node to Load	2 – 15 inches	Figure 146	
SCR – SCR# Length Matching	± 10 mils		
Rs Series Termination Value	33 Ω ± 5%	Figure 146	
Rt Shunt Termination Value	49.9 Ω± 5% (for 55 Ω odd mode MB impedance)	Figure 146	5

NOTES:
1. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
2. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network
3. Set line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack up.
4. The differential impedance of each clock pair is approximately 2*Zsingle-ended*(1-2*Kb) where Kb is the backwards cross-talk coefficient. For the recommended trace spacing, Kb is very small, and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
5. Rt shunt termination value should match the motherboard impedance.
6. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ringback.
7. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in Er and the impedance variations due to physical tolerances of circuit board material.

Figure 147. Trace Spacing for SRC Clocks



11.2.9.2 SRC General Routing Guidelines

- When routing the 100 MHz differential clocks, do not split up the two halves of a differential clock pair between layers. Route to all agents on the same physical routing layer referenced to ground.
- If a layer transition is required, make sure skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Do not place vias between adjacent complementary clock traces, and avoid differential vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias may be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

Schematic Checklist Summary 12

The following checklist provides design recommendations and guidance for Intel® Pentium® M/ Celeron® M processor systems with the Intel® 855GME chipset.

The schematic checklist is a tool used to ensure that design recommendations detailed in this Platform Design Guide have been followed prior to schematic reviews. The items contained in this checklist attempt to address important connections and critical supporting circuitry; however, **it is not a complete list**. For complete design recommendations, refer to the main content of this document (referred to as the Platform Design Guide) and the appended Customer Reference Board (CRB) schematics. The information in this guide is subject to change.

Note: Unless otherwise specified the default tolerance on resistors is ± 5 percent.

12.1 Intel® Pentium® M/Celeron® M Processor Checklist

12.1.1 Connection Recommendations

Table 115 presents the connection recommendations. Figure 148 depicts the routing illustration for INIT# (for Intel Pentium M/Celeron M processor). Figure 149 depicts the voltage translation circuit for PROCHOT# (for Intel Pentium M/Celeron M processor).

Table 115. Connection Recommendations (Sheet 1 of 3)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	√
A20M#				Point-to-point connection to the 6300ESB, (A20M# signal).	
BR0#				Point-to-point connection to GMCH (BREQ0# signal).	
COMP0, COMP2	27.4 Ω ± 1% pull-down to GND			Resistor placed within 0.5” of processor pin. Trace shall be 27.4 Ω ± 15%.	
COMP1, COMP3	54.9 Ω ± 1% pull-down to GND			Resistor placed within 0.5” of processor pin. Trace shall be 55 Ω ± 15%.	
DPSLP#	4.7 KΩ pull-up to VCCP at CPU 1 KΩ pull-up to VCCP at GMCH			Used only with the ICH4-M. The 6300ESB does not provide this signal.	
FERR#	56 Ω pull-up to VCCP	56 Ω from pull-up to 6300ESB pin		Point-to-point connection to 6300ESB (FERR# signal), with pull-up resistor and series resistor placed by the 6300ESB.	
GTLREF	1 KΩ ± 1% pull-up to VCCP 2 KΩ ± 1% pull-down to GND			Voltage divider shall be placed within 0.5” of processor pin.	

Table 115. Connection Recommendations (Sheet 2 of 3)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	√
IERR#	56 Ω pull-up to VCCP			IERR# is a 1.05 V signal. Voltage translation logic and/or series resistor may be required if used.	
INIT#			R1 = 1.3 KΩ R2 = 330 Ω Rs = 330 Ω	Point-to-point connection to the 6300ESB (INIT# signal). Voltage translation circuit is required if connecting to FWH. Signal is T-split from the 6300ESB to FWH. Refer to Figure 148.	
IGNNE#				Point-to-point connection to the 6300ESB (IGNNE# signal).	
LINT0				Point-to-point connection to the 6300ESB (INTR signal).	
LINT1				Point-to-point connection to the 6300ESB (NMI signal).	
PROCHOT#	56 Ω pull up to VCCP		R1 = 1.3 KΩ R2 = 330 Ω Rs = 330 Ω	PROCHOT# is a VCCP signal. Voltage translation logic may be required if used. **When Voltage Translation is Required:** Driver isolation resistor (Rs) shall be placed at the beginning of the T-split to the system receiver. Refer to Figure 149.	
PSI#				May be left as NC, if not used for IMVP.	
PWRGOOD	330 Ω pull-up to VCCP			Point-to-point connection to an output of an AND gate (AND of PWRGD_3V and CPU_VR_PWRGD) with resistor placed by the processor.	
RESET#	220 Ω ± 5% pull-up to VCCP WHEN USING ITP700FLEX	22.6 Ω ± 1% from pull-up to ITP700FLEX		**When ITP700FLEX is Not Used:** Point-to-point connection to GMCH (CPURST# signal). **When ITP700FLEX is Used:** RESET# connects from processor to GMCH (CPURST# signal) and then forks out to ITP700 FLEX, with pull-up and series damping resistor placed next to ITP.	
SLP#				Point-to-point connection to the 6300ESB (CPUSLP# signal).	
SMI#				Point-to-point connection to the 6300ESB (SMI# signal).	
STPCLK#				Point-to-point connection to the 6300ESB (STPCLK# signal).	

Table 115. Connection Recommendations (Sheet 3 of 3)

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	√
TEST[3:1]	1 KΩ pull-down to GND (default: no stuff)			For each signal, stuffing option for pull-down shall be provided for testing purposes. For normal operation, leave the resistors unpopulated.	
THERMTRIP#	56 Ω pull-up to VCCP	56 Ω from pull-up to the 6300ESB pin		Point-to-point connection to an 6300ESB (THRMTRIP# signal), with pull-up and series resistors placed by 6300ESB. THERMTRIP# is a VCCP signal. When connecting to device other than an 6300ESB, voltage translation logic may be required.	
VCC[72:1]	Connect to CPU_CORE			From Intel® IMVP-IV specification power supply.	
VCCA[3:0]	Connect to V1P8			The Low Voltage Intel® Pentium® M Processor on 90 nm process with 2 MB L2 cache will support a Vcca of 1.8V or 1.5V.	
VCC1_05 [25:1]	Connect to VCCP				
VCCSENSE, VSSSENSE	54.9 Ω ± 1% pull-down to GND (Default: no stuff)			For each signal, stuffing option for pull-down shall be provided for testing purposes. Also, a test point for differential probe ground shall be placed between the two resistors. For normal operation, leave the resistors unpopulated.	
GND[192:1]	Connect to GND				

Figure 148. Routing Illustration for INIT# (for Intel® Pentium® M/Celeron® M Processor)

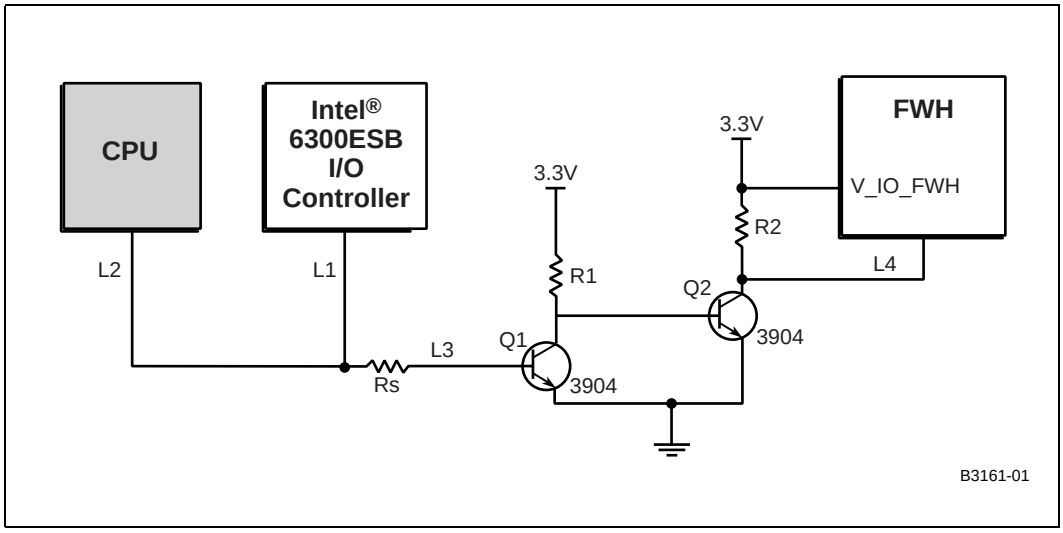
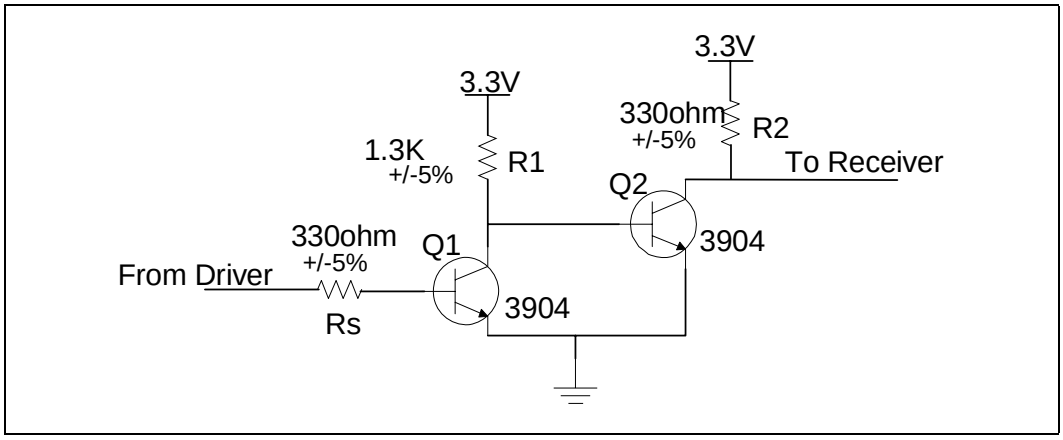


Figure 149. Voltage Translation Circuit for PROCHOT# (for Intel® Pentium® M/Celeron® M Processor)



12.1.2 In Target Probe (ITP)

Table 116 presents the In Target Probe (ITP) information.

Table 116. In Target Probe (ITP)

Pin Name	System Pull-up/Pull-down	Series Termination Resistor (Ω)	Notes	√
BPM[5:0]#			Connect to processor directly.	
DBR#	150-240 Ω pull-up to VCC3		When using ITP on interposer card, DBR# shall also be connected to DBR# pin at the processor. The 150-240 Ω pull-up resistor shall be placed within 1 ns of the ITP700FLEX connector. The CPU shall **not** be power cycled when DBR# is asserted.	
RESET#	220 Ω ± 5 % pull-up to VCCP when using ITP700FLEX	22.6 Ω ± 1% from pull-up to ITP700FLEX	Refer to the RESET# notes in Table 115.	
FBO			Connect to TCK pin of processor. Refer to Section 4.3.1.1 for layout details.	
TCK	27.4 Ω ± 1% pull-down to GND		Connect to processor, with resistor placed by ITP. Refer to Section 4.3.1.1 for layout details.	
TDI	150 Ω pull-up to VCCP		Connect to processor with resistor placed by the processor. Refer to Section 4.3.1.1 for layout details.	
TDO	54.9 Ω ± 1% pull-up to VCCP	22.6 Ω ± 1% from pull-up to ITP700FLEX	Connect to processor with resistors placed by ITP. When ITP not used, this signal may be left as NC.	
TMS	39.2 Ω ± 1% pull-up to VCCP		Connect to processor with resistor placed by ITP.	
TRST#	680 Ω pull-down to GND		Connect to processor with resistor located anywhere between processor and ITP.	
VTAP, VTT[1:0]	Connect to VCCP		One 0.1 µF decoupling cap near ITP is required. Refer to Section 4.3.1.1 for layout details.	

12.1.3 Decoupling Recommendations

12.1.3.1 VCCP (I/O)

Table 117 presents the VCCP (I/O) decoupling recommendations.

Table 117. VCCP (I/O) Decoupling Recommendations

Description	C, µF	ESR, mΩ	ESL, nH	Notes	√
Low Frequency Decoupling (Polymer Covered Tantalum - POSCAP, Neocap, KO Cap)	2 x 150 µF	42 mΩ (typ)/2	2.5 nH/2	Refer to Section 4.4.4 for implementation of recommended decoupling.	
High Frequency Decoupling (0603 MLCC, >= X7R)	10 x 0.1 µF	16 mΩ (typ)/10	0.6 nH/10		

12.1.3.2 VCCA (PLL)

Table 118 presents the VCCA (PLL) decoupling recommendations.

Table 118. VCCA (PLL) Decoupling Recommendations

Description	C, µF	Notes	√
Mid Frequency Decoupling (Polymer Covered Tantalum - POSCAP, Neocap, KO Cap)	4 x 10 µF	Place one 10 µF and one 0.01 µF for each VCCA pin.	
High Frequency Decoupling (0603 MLCC, >= X7R). Place next to Pentium M processor.	4 x 0.01 µF	Place one 10 µF and one 0.01 µF for each VCCA pin.	

12.1.3.3 VCC (CORE)

Table 119 presents the VCC (CORE) decoupling recommendations.

Table 119. VCC (CORE) Decoupling Recommendations (Sheet 1 of 2)

Option	Description	C, µF	ESR, mΩ	ESL, nH	√
#1	Low-Frequency Decoupling (Polymer Covered Tantalum – POSCAP, Neocap, KO Cap)	12 x 150 µF	36 mΩ (typ)/12	2.5 nH/12	
	Mid-Frequency Decoupling (0612 MLCC, X5R or better)	15 x 2.2 µF	5 mΩ (typ)/15	0.2 nH/15	
#2	Low-Frequency Decoupling (1206 MLCC, X5R or better)	40x10 µF	5 mΩ (typ)/40	1.2 nH/40	
	Mid-Frequency Decoupling (0612 MLCC, X5R or better)	15 x 2.2 µF	5 mΩ (typ)/15	0.2 nH/15	

NOTES:
1. Decoupling guidelines are recommendations based on Intel reference board design. The Intel Customer Reference Board uses option #4. This is the preferred recommendation for decoupling.
2. When deciding on overall decoupling solution, customers may need to take layout and PCB board design into consideration.
3. Option #4 is to be used with small footprint (100 mm^2 or less) 0.36 µH ± 20% inductors.

Table 119. VCC (CORE) Decoupling Recommendations (Sheet 2 of 2)

Option	Description	C, µF	ESR, mΩ	ESL, nH	√
#3	Low Frequency Decoupling (Polymer Covered Aluminum – SP Cap, A0 Cap)	5 x 330 µF	15 mΩ (max)/5	3.5 nH/5	
	Low Frequency Decoupling (1206 MLCC, >= X5R)	25 x 10 µF	5 mΩ (typ)/25	1.2 nH/25	
	Mid Frequency Decoupling (0612 MLCC, >= X5R)	15 x 2.2 µF	5 mΩ (typ)/15	0.2 nH/15	
#4 (Note 1)	Low-Frequency Decoupling (Polymer Covered Aluminum – SP CAP, AO Cap)	4 x 220 µF	12 mΩ (max)/4	3.5 nH/4	
	Mid-Frequency Decoupling (0805 MLCC>= X5R)	35 x 10 µF	5 mΩ (typ)/35	0.6 nH/35	

NOTES:
1. Decoupling guidelines are recommendations based on Intel reference board design. The Intel Customer Reference Board uses option #4. This is the preferred recommendation for decoupling.
2. When deciding on overall decoupling solution, customers may need to take layout and PCB board design into consideration.
3. Option #4 is to be used with small footprint (100 mm^2 or less) 0.36 µH ± 20% inductors.

12.2 CK409 Clock Checklist

12.2.1 Connection Recommendations

Table 120 presents the CK409 connection recommendations.

Table 120. CK409 Connection Recommendations (Sheet 1 of 2)

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	√
3V66_[0] 3V66_[1]*		33 Ω ± 5%	When the signal is used, one 33 ohm series resistor is required. When the signal is NOT used, it shall be left as NC (Not Connected) or connected to a test point. *Two possible topologies for 3V66_1: • Use directly for GMCH's DREFSSCLK. • Use as input to an SSC device with SSC output to GMCH's DREFSSCLK.	
3V66_[4:2]		33 Ω ± 5%	The Intel CRB routes 3V66[2] (pin 21) to GCLKIN on GMCH. The other two signals route to 6300ESB (CLK66) and AGP connector (AGPCLK).	
CPU[0], CPU[0]# CPU[1], CPU[1]# CPU[2], CPU[2]#	49.9 Ω ± 1% pull- down to GND	33 Ω ± 5%	Use one pair for the processor and another pair for GMCH. When onboard ITP is implemented, the third pair of clock signals is used for the ITP connector. Otherwise, it may be routed to the dedicated ITP clock pins on the processor socket. Refer to Chapter 11 for all routing requirements.	

Table 120. CK409 Connection Recommendations (Sheet 2 of 2)

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	√
DOT_48MHZ		33 Ω ± 5%	Connect to GMCH's DREFCLK.	
FS_A, FS_B			Used for selecting the host clock frequency.	
IREF	475 Ω ± 1% pull-down to GND		Adjusts IREF to 2.32 mA.	
PCI[6:0]		33 Ω ± 5%	Connect to various PCI devices and other 33 MHZ clock inputs for devices such as FWH and SIO (LPC). Use one clock for the 6300ESB. Unused clock pins shall be left as NC or connected to a test point.	
PCIF[2:0]		33 Ω ± 5%		
PWRDWN#	Terminate to VCC3_CLK through 1 K Ω resistor.		The Intel CRB does not support S1M state.	
REF[0:1]		33 Ω ± 5%	This is the 14.318 MHz clock reference signal for the 6300ESB, SIO and LPC. Each receiver requires one 33-ohm series resistor.	
USB_48MHZ		33 Ω ± 5%	Connect to the 6300ESB's 48 MHz clock input.	
XTAL_IN, XTAL_OUT	Terminate each pin to GND through a 10 pF ± 5% capacitor.		Connect to a 14.318 MHz crystal, placed within 500 mils of CK409.	
VDD[7:0], VDDA, VDD_48MHZ	Connect to VCC3.		Refer to clock vendor datasheet for decoupling info.	
VSS[5:0], VSSA, VSS_48MHZ	Connect to GND.			
VSSIREF	Connect to GND.			

12.3 Intel® 855GME Chipset GMCH (82855GME) Checklist

12.3.1 System Memory

12.3.1.1 GMCH System Memory Interface Checklist

Table 121 presents the GMCH system memory interface checklist. Figure 150 depicts the reference voltage level for SMVREF.

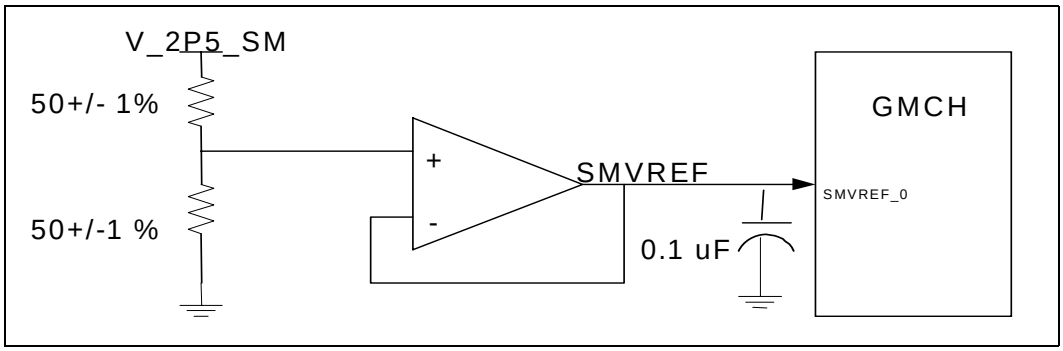
Table 121. GMCH System Memory Interface Checklist (Sheet 1 of 2)

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	√
SRCVENIN#			This signal shall be routed to a via next to ball and left as a NC.	
SRCVENOUT#			This signal shall be routed to via next to ball and left as a NC.	
SBA[1:0]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0 and DIMM 1.	
SCAS#	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0 and DIMM 1.	
SRAS#	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0 and DIMM 1.	
SWE#	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0 and DIMM 1.	
SCKE[1:0]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0	
SCKE[3:2]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 1	
SCS#[1:0]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0	
SCS#[3:2]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 1	
SDQ[63:0]	56 Ω pull-up to V_1P25_MEMVTT	10 Ω	Connect to DIMM 0 and DIMM 1.	
SDM[7:0]	56 Ω pull-up to V_1P25_MEMVTT	10 Ω	Connect to DIMM 0 and DIMM 1.	
SDQS[7:0]	56 Ω pull-up to V_1P25_MEMVTT	10 Ω	Connect to DIMM 0 and DIMM 1.	
SDQ[71:64]	56 Ω pull-up to V_1P25_MEMVTT	10 Ω	When ECC support is not implemented, SDQ[71:64], SDM8, and SDQS8 shall be left as NC. For ECC support, these signals connect to DIMMs.	
SDM8	56 Ω pull-up to V_1P25_MEMVTT	10 Ω	When ECC support is not implemented, SDQ[71:64], SDM8, and SDQS8 shall be left as NC. For ECC support, these signals connect to DIMMs.	

Table 121. GMCH System Memory Interface Checklist (Sheet 2 of 2)

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	√
SDQS8	56 Ω pull-up to V_1P25_MEMVTT	10 Ω	When ECC support is not implemented, SDQ[71:64], SDM8, and SDQS8 shall be left as NC. For ECC support, these signals connect to DIMMs.	
SMA[12:6,3,0]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0 and DIMM 1.	
SMA[5,4,2,1]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 0.	
SMAB[5,4,2,1]	56 Ω pull-up to V_1P25_MEMVTT		Connect to DIMM 1.	
SCK0, SCK0# SCK1, SCK1#			These clock signals route differentially directly to DIMM 0. Alternatively, refer to Section 5.5.1 for information regarding GMCH clock routing flexibility.	
SCK2, SCK2#			Route these signals differentially directly to DIMM 0. Alternatively, refer to Section 5.5.1 for information regarding GMCH clock routing flexibility.	
SCK3, SCK3# SCK4, SCK4#			These clock signals route differentially directly to DIMM 0. Alternatively, refer to Section 5.5.1 for information regarding GMCH clock routing flexibility.	
SCK5, SCK5#			Route these signals differentially directly to DIMM 1. Alternatively, refer to Section 5.5.1 for information regarding GMCH clock routing flexibility.	
SMVREF_0	Resistor divider to V_2P5_SM consists of two identical resistors (50 Ω – 150 Ω 1%)		Signal voltage level = V_2P5_SM/2. Optionally, the Intel CRB may support a buffer to provide the necessary current and reference voltage to SMVREF. Refer to Figure 150. Place a 0.1 µF cap by GMCH, DIMM 0, and DIMM 1 pins. Refer to Section 4.8.2.2 for more information.	
SMVSWINGL	604 Ω 1% pull-up to V_2P5_SM 150 Ω 1% pull-down to GND		Signal voltage level = 1/5 * V_2P5_SM. Need 0.1 µF cap at the GMCH pin.	
SMVSWINGH	150 Ω 1% pull-up to V_2P5_SM 604 Ω 1% pull-down to GND		Signal voltage level = 4/5 * V_2P5_SM. Need 0.1 µF cap at the GMCH pin.	
SMRCOMP	60.4 Ω 1% pull-up to V_2P5_SM 60.4 Ω 1% pull-down to GND		Signal voltage level = 1/2 * V_2P5_SM. Need 0.1 µF cap between V_2P5_SM and GND near the voltage divider.	

Figure 150. Reference Voltage Level for SMVREF



12.3.1.2 DDR DIMM Interface Checklist

Table 122 presents the DDR DIMM interface checklist.

Table 122. DDR DIMM Interface Checklist

Pin Name	Configuration	Notes	√
NC (FETEN) (pin 167)		Signal may be left as NC (Not Connected).	
CS[3:2]# (pin163, 71)		Signal may be left as NC.	
BA2 (pin 113)		Signal may be left as NC.	
VREF (pin 1)	Connected to 82855GME SMVREF signal	Signal voltage level = V_2P5_SM/2. Place a 0.1µF cap by GMCH, DIMM 0, and DIMM 1 pins.	
VDD[9:1]	Connect to V_2P5_SM	Power must be provided during S3.	
VDDSPD	Connect to V_2P5_CORE		
SA[2:1]	Connect to GND	These lines are used for strapping the SPD address for each DIMM.	
SA0	DIMM 0: connect to GND DIMM 1: connect to V_2P5_SM	These lines are used for strapping the SPD address for each DIMM.	
VSS[22:1]	Connect to GND		
NC (pin 10)		Signal may be left as NC.	
SDA/SCL	Connect to the 6300ESB SMBUS and SMLINK through isolation circuitry.		
NC (pin 90)		Signal may be left as NC.	
A13 (pin 103)		Signal may be left as NC.	
VDDQ[16:1]	Connect to V_2P5_SM		
VDDID (pin 82)		Signal may be left as NC.	
NC[4:1] (pins 9,101,102,173)		Signal may be left as NC.	

12.3.1.3 DIMM Decoupling Recommendation Checklist

Table 123 presents the DIMM decoupling recommendation checklist.

Table 123. DIMM Decoupling Recommendation Checklist

Pin Name	F	Qty	Notes	√
V_1P25_MEMVTT	0.1 µF 4.7 µF† 470 µF	(55†) 3 4	Place one 0.1 µF cap close to every two pull-up resistors terminated to V_1P25_MEMVTT (VTT for DDR signal termination). Place two 4.7 µF caps at either end of the VTT island and one near the center. Four 470 µF capacitors may be placed as bulk decoupling. Refer to Section 4.8.1.3 for more information.	
V_2P5_SM	0.1 µF 100-150 µF (220 µF†) (100 µF†)	9 (15†) 4 (3†) (1†)	A minimum of nine high frequency caps are recommended to be placed between the DIMMS. A minimum of four low frequency caps are required. Refer to section Section 4.8.3.2 for more information.	

† Used on Intel CRB.

12.3.2 Frontside Bus (FSB) Checklist

Table 124 presents the FSB Checklist. Figure 151 depicts the Intel® 855GME Chipset HXSWING and HYSWING reference voltage generation circuit.

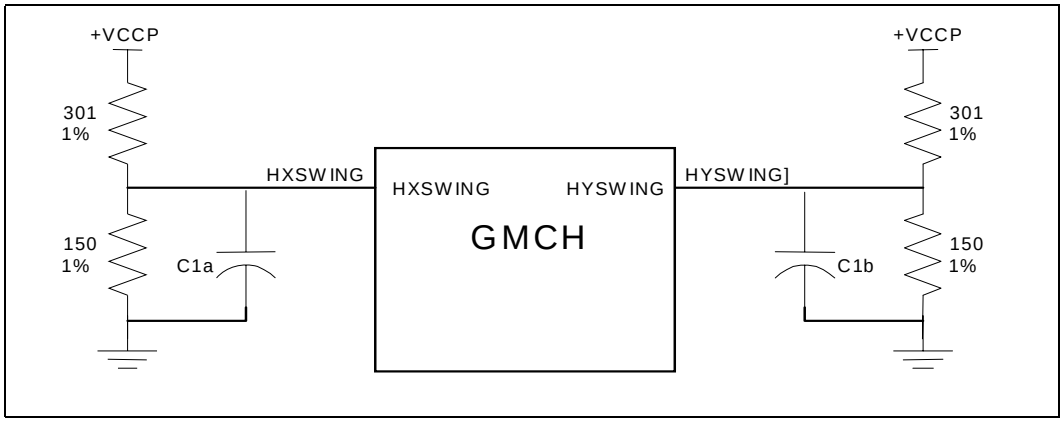
Table 124. FSB Checklist (Sheet 1 of 2)

Pin Name	System Pull-up/Pull-down	Notes	√
ADS#		Connect directly to processor (ADS# signal).	
HTRDY#		Connect directly to processor (TRDY# signal).	
DRDY#		Connect directly to processor (DRDY# signal).	
DEFER#		Connect directly to processor (DEFER# signal).	
HITM#		Connect directly to processor (HITM# signal).	
HIT#		Connect directly to processor (HIT# signal).	
HLOCK#		Connect directly to processor (LOCK# signal).	
BREQ0#		Connect directly to processor (BR0# signal).	
BNR#		Connect directly to processor (BNR# signal).	
BPRI#		Connect directly to processor (BPRI# signal).	
DBSY#		Connect directly to processor (DBSY# signal).	
RS[2:0]#		Connect directly to processor (RS[2:0]# signals).	
HA[31:3]#		Connect directly to processor (A[31:3]# signals).	
HREQ[4:0]#		Connect directly to processor (REQ[4:0]# signals).	
HADSTB[1:0]#		Connect directly to processor (ADSTB[1:0]# signals).	

Table 124. FSB Checklist (Sheet 2 of 2)

Pin Name	System Pull-up/Pull-down	Notes	√
BCLK, BCLK#	Refer to the CK409 Checklist for CPU[0], CPU[0]#, CPU[1], CPU[1]#, CPU[2], and CPU[2]#.	Connect to CK409.	
HDSTBN[3:0]#		Connect directly to processor (DSTBN[3:0]# signals).	
HDSTBP[3:0]#		Connect directly to processor (DSTBP[3:0]# signals).	
DINV[3:0]#		Connect directly to processor (DINV[3:0]# signals).	
CPURST#	220 Ω 6% pull-up to VCCP. 22.6 Ω 1% series to ITP (pin 12). Refer to the Pentium® M Processor Checklist for RESET#.	Connect to processor (RESET# signal) and ITP (if implemented).	
HD[63:0]#		Connect directly to processor (D[63:0]# signals).	
DPWR#		Connect directly to processor (DPWR# signal).	
DPSLP#	1 KΩ pull-up to VCCP at GMCH. 4.7 KΩ pull-up to VCCP at CPU.	Used only with the ICH4-M. The 6300ESB does not provide this signal.	
HXSWING	301 Ω 1% pull-up to VCCP 150 Ω 1% pull-down to GND	Signal voltage level = 1/3 of VCCP. C1a = 0.1 µF. C1b=0.1 µF. Refer to Figure 151.	
HYSWING	301 Ω 1% pull-up to VCCP 150 Ω 1% pull-down to GND	Signal voltage level = 1/3 of VCCP. C1a=0.1 µF. C1b=0.1 µF. Refer to Figure 151.	
HXRCOMP	27.4 Ω 1% pull down to GND	One pull-down resistor where trace shall be 10 mil wide with 20 mil spacing. Refer to Section 4.8.3.2.	
HYRCOMP	27.4 Ω 1% pull down to GND	One pull-down resistor where trace shall be 10 mil wide with 20 mil spacing. Refer to Section 4.8.3.2.	
HDVREF[2:0]	49.9 Ω 1% pull-up to VCCP 100 Ω 1% pull-down to GND	Signal voltage level = 2/3 of VCCP. Need one 0.1 µF cap and one 1 µF cap near voltage divider.	
HAVREF	49.9 Ω 1% pull-up to VCCP 100 Ω 1% pull-down to GND	Signal voltage level = 2/3 of VCCP. Need one 0.1 µF cap and one 1 µF cap for voltage divider.	
HCCVREF	49.9 Ω 1% pull-up to VCCP 100 Ω 1% pull-down to GND	Signal voltage level = 2/3 of VCCP. Need one 0.1 µF cap and one 1 µF cap for voltage divider.	

Figure 151. Intel® 855GME Chipset HXSWING and HYSWING Reference Voltage Generation Circuit



12.3.3 Hub Interface Checklist

Table 125 presents the hub interface checklist.

Table 125. Hub Interface Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
HI[10:0]		Connect to the 6300ESB (HI[10:0] signals). Refer to Section 8.1 for more information.	
HLSTB (S)		Connect to the 6300ESB (HL_STBS signal).	
HLSTB# (F)		Connect to the 6300ESB (HL_STBF signal).	
HLVREF	Refer to Section 8.1.4.2.	Signal voltage level = 0.35 V ± 8%.	
PSWING	Refer to Section 8.1.4.2.	Signal voltage level = 2/3 of V1P2_GMCH or 0.8 V ± 8%.	
HLRCOMP	37.4 Ω 1% pull-up to 1.35V core voltage	Refer to Section 8.1.5 for more information.	

12.3.4 Graphics Interfaces Checklist

12.3.4.1 Low Voltage Digital Signalling (LVDS) Checklist

Table 126 presents the LVDS checklist.

Table 126. LVDS Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
LIBG	1.5 KΩ 1% pull-down to GND		
IYAP[3:0]/ IYAM[3:0] IYBP[3:0]/ IYBM[3:0]		When any of these LVDS data pairs are unused, they may be left as NC. The Intel CRB routes these data pairs directly to a 30-pin dual channel LVDS connector.	
ICLKAP/ICLKAM ICLKBP/ICLKBM		When either of these LVDS clock pairs is not used, it may be left as NC.	
DDCPCLK, DDCPDATA	2.2 k to 10 k pull-up to 3.3 V if not used.	LVDS Panel DDC Clock/Data pair to collect digital display EDID information.	
PANELVDDEN	100 k pull-down	Used for LVDS Panel Power control.	
PANELBKLTEN	100 k pull-down	Used for LVDS Panel backlight enable.	
PANELBKLTCTL	100 k pull-down	Used for LVDS Panel backlight brightness control.	

12.3.4.2 Digital Video Out (DVO) Checklist

Table 127 presents the DVO checklist. Figure 84 depicts the DPMS clock implementation.

Table 127. DVO Checklist (Sheet 1 of 2)

Pin Name	System Pull-up/Pull-down	Notes	√
DVORCOMP	40.2 Ω 1% pull-down to GND	Trace shall be 10-mil wide with 20-mil spacing.	
GVREF	1 KΩ 1% pull-up to V_1P5_CORE 1 KΩ 1% pull-down to GND	Signal voltage level = 1/2 of V_1P5_CORE. Need 0.1 µF cap at GMCH pin and near ADD slot pin (if implemented).	
DVOCD[11:0]		When unused, these signals may be left as NC. DVO Routing is to ADD connector on Intel CRB. For AGP these signals are: GAD[29:19] and GCBE#. See Chapter 3.6.3 of the 855GME datasheet for exact assignment.	
DVOCCLK, DVOCCLK#		When unused, these signals may be left as NC. For AGP these signals are: GAD_STB1, GAD_STB1#.	
DVOCHSYNC		When unused, these signals may be left as NC. For AGP this signal is: GAD[17].	
DVOCVSYNC		When unused, these signals may be left as NC. For AGP this signal is: GAD[16].	
DVOCBLANK#		When unused, these signals may be left as NC. For AGP this signal is: GAD[18].	

Table 127. DVO Checklist (Sheet 2 of 2)

Pin Name	System Pull-up/Pull-down	Notes	√
DVOCFLDSTL	100 KΩ pull-down to GND	Pull-down resistor required only if signal is unused (10 K-100 K). It is up to DVO device to drive this signal. For AGP this signal is: GAD[31].	
DVOBCINTR#	100 KΩ pull-up to V_1P5_CORE	Pull-up resistor required only if signal is unused (10 K-100 K). It is up to the DVO device to drive this signal. For AGP this signal is: GAD[30].	
DVOBCCLKINT	100 KΩ pull-down to GND	Pull-down resistor required only if signal is unused (10 K-100 K). It is up to the DVO device to drive this signal. For AGP this signal is: GAD[13].	
DVOBD[11:0]		When this port is unused, it may be left as NC. For AGP these signals are: GAD[12:2]. Refer to Chapter 3.6.3 of the 855GME datasheet for exact assignment.	
DVOBCLK, DVOBCLK#		When this port is unused, it may be left as NC. For AGP these signals are: AD_STB0, AD_STB0#	
DVOBHSYNC		When this port is unused, it may be left as NC. For AGP this signal is: GAD[0].	
DVOBVSYNC		When this port is unused, it may be left as NC. For AGP this signal is: GAD[1].	
DVOBBLANK#		When this port is unused, it may be left as NC. For AGP this signal is: GCBE#1.	
DVOBFLDSTL (pin M2)	100 KΩ pull-down to GND	Pull-down resistor required only if this signal is unused (10K-100K). For AGP this signal is: GAD[14].	
MI2CCLK, MI2CDATA	2.2 KΩ pull-up to V_1P5_CORE	Pull-up resistor required on each signal even if they are unused (2.2 K-100 K). This signal is 1.5 V tolerant. It may require voltage translation circuit. For AGP these signals are: GIRDY#, GDEVSEL#.	
MDVICLK, MDVIDATA	2.2 KΩ pull-up to V_1P5_CORE	Pull-up resistor required on each signal even if they are unused (2.2 K-100 K). This signal is 1.5 V tolerant. It may require voltage translation circuit. For AGP these signals are: GTRDY#, GFRAME#.	
MDDCCLK, MDDCDATA	2.2 KΩ pull-up to V_1P5_CORE	Pull-up resistor required on each signal even if they are unused (2.2 K-100 K). This signal is 1.5 V tolerant. It may require voltage translation circuit. For AGP these signals are: GSTOP#, GAD[15].	
ADDID[6:0]		Leave as NC. For AGP these signals are: GSBA[6:0].	
ADDID7	1 KΩ pull-down to GND if DVO device is onboard	When DVO interface is not used, this signal may be left as NC. Otherwise, pull-down is needed. For AGP this signal is: GSBA[7].	
GCLKIN	33 ohm series at CK409	Connect to CK409, 66 MHz clock.	
DVODETECT	1 KΩ pull-up to V_1P5_CORE if DVO interface is unused	When DVO interface is used, leave as NC. This signal has internal pull-down. For AGP this signal is: GPAR.	
DPMS		Connect to 1.5 V version of the 6300ESB's SUSCLK or a clock that runs during S1. For AGP this signal is: GPIPE. See Section 7.2.11 for the DPMS clock isolation circuit.	

12.3.4.3 Digital-to-Analog Converter (DAC) Checklist

Table 128 presents the DAC checklist.

Table 128. DAC Checklist

Pin Name	System Pull-up/Pull-down	In Series	Notes	√
REFSET	124-137 Ω 1% pull-down to GND		137 Ω used on Intel CRB.	
RED #	Connect to GND.		Need to connect to RED's return path.	
BLUE #	Connect to GND.		Need to connect to BLUE's return path.	
GREEN#	Connect to GND.		Need to connect to GREEN's return path.	
RED	On GMCH side of ferrite bead: 75 Ω 1% pull-down to GND, 3.3 pF cap to GND, ESD diode protection for V_1P5_CORE On VGA side of ferrite bead: 3.3 pF cap to GND	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
BLUE	On GMCH side of ferrite bead: 75 Ω 1% pull-down to GND, 3.3 pF cap to GND, ESD diode protection for V_1P5_CORE. On VGA side of ferrite bead: 3.3 pF cap to GND	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
GREEN	On GMCH side of ferrite bead: 75 Ω 1% pull-down to GND, 3.3 pF cap to GND, ESD diode protection for V_1P5_CORE On VGA side of ferrite bead: 3.3 pF cap to GND	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
HSYNC	33 pF cap to GND at connector (470 pF†)	39 Ω	Requires unidirectional buffer. See Section 6.1.6.	
VSYNC	33 pF cap to GND at connector (470 pF†)	39 Ω	Requires unidirectional buffer. See Section 6.1.6.	

† Value used on Intel CRB.

12.3.5 Miscellaneous Signal Checklist

Table 129 presents the Miscellaneous signal checklist.

Table 129. Miscellaneous Signal Checklist

Pin Name	System Pull-up/Pull-down	Notes	√
RSTIN#		Reset: (I) Connect to the 6300ESB PCI_RST# pin (if ~4 loads). May need to be buffered.	
PWROK		Power OK: (I) 3 V signal. Indicates GMCH power is stable.	
AGPBUSY#	8.2k pull-up to VCC3	AGP Busy: (O)	
DDCACLK, DDCADATA	2.2k pull-up to Vcc5 after translation logic	CRT DDC Clock/Data Needs to be translated from 3 V to 5 V.	
EXTTS_0	10 KΩ 1% pull-up to VCC3		
LCLKCTLB		Used for SSC chip data control on Intel CRB. Leave this signal as NC if not used.	
LCLKCTLA		Used for SSC chip data control on Intel CRB. Leave as NC if not used.	
DREFCLK	33 ohm series at CK409.	DAC Display Clock Input Connect to CK409 48 MHz DOT CLK (pin 38).	
DREFSSCLK	33 ohm series at CK409.	LVDS SSC Clock Input. 48 MHz or 66 MHz, SSC or non-SSC. Connect to CK409 3V66_1/VCH CLK (pin 35). Optional to connect to SSC chip for enhanced spread.	
GST2 (C2) GST1 (C3) GST0 (C4)	Leave as NC or 1 KΩ pull-up to V_1P5_CORE	These pins have internal pull-down. Refer to Table 130 for GST[2:0] configuration options.	

12.3.5.1 Intel® Pentium® M/Celeron® M Processor GST[2:0] Configurations

Table 130 presents the Intel Pentium M/Celeron M processor GST[2:0] configurations.

Table 130. GST[2:0] Configurations

Pentium® M Processor GST[2:0] Configuration	FSB	DDR	Gfx Core Clock Low	Gfx Core Clock High
000	400	266	133	200
001	400	200	100	200
010 (UXGA for 855GME only)	400	200	100	133
111 (855GME only)	400	333	166	250

12.3.6 GMCH Decoupling Recommendations Checklist

Table 131 presents the GMCH decoupling recommendations checklist.

Table 131. GMCH Decoupling Recommendations Checklist (Sheet 1 of 2)

Pin Name	Configuration	F	Qty	Notes	√
VCC[18:1]	Connect to V1P35_GMCH.	0.1 µF 150 µF 10 µF	4 2 1	Bulk decoupling is based on VR solutions used on CRB design.	
VTTLF[21:1]	Connect to VCCP	0.1 µF 270 µF 10 µF	3 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
VTTHF[5:1]		0.1 µF	5	Connect pins directly to caps to GND.	
VCCHL[8:1]	Connect to V1P35_GMCH.	0.1 µF 10 µF	2 1	Bulk decoupling is based on VR solutions used on CRB design.	
VCC_SM[37:1]	Connect to V_2P5_SM.	0.1 µF 150 µF	11 2	Bulk decoupling is based on VR solutions used on CRB design.	
VCC_QSM[2:1]	Connect to V_2P5_SM with filter network.	0.1 µF 4.7 µF+1Ω	1 1 each	0.68 µH from power supply to GMCH pins. On GMCH side of inductor: one 0.1 µF to GND, 4.7 µF + 1 Ω to GND.	
VCCASM[2:1]	Connect to V1P35_GMCH with filter network.	0.1 µF 100 µF	1 1	1 µH from power supply to GMCH pins, with caps on GMCH side of inductor.	
VCC_DVO[16:1]	Connect to V_1P5_CORE.	0.1 µF 10 µF 150 µF	2 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
VCC_ADAC[2:1]	Connect to V_1P5_CORE.	0.01 µF 0.1 µF 220 µF (no stuff)	1 1 1	Route VSSADAC to other side of the caps, then to ground. Consider a 0-ohm 0805 resistor between the caps and V_1P5_CORE. This and the 220 µF cap footprint are there in case there is noise issue with the VGA supply.	
VCC_ALVDS	Connect to V_1P5_CORE	0.1 µF 0.01 µF	1 1	Route VSSALVDS to other side of the caps, then to ground.	
VCC_DLVDS[4:1]	Connect to V_1P5_CORE	0.1 µF 22 µF 47 µF	1 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
VCC_TXLVDS[4:1]	Connect to V_2P5_CORE	0.1 µF 22 µf 47 µF	3 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
VCC_GPIO[2:1]	Connect to VCC3	0.1 µF 10 µF	1 1	Bulk decoupling is based on VR solutions used on CRB design.	
VCC_AHPLL	Connect to V1P35_GMCH	0.1 µF	1		

NOTE: Decoupling guidelines are recommendations based on our reference board design. Customers may need to take layout and PCB board design into consideration when deciding on overall decoupling solution.

Table 131. GMCH Decoupling Recommendations Checklist (Sheet 2 of 2)

Pin Name	Configuration	F	Qty	Notes	√
VCC_GPLL	Connect to V1P35_GMCH	0.1 µF	1		
VCC_ADPLLA	Connect to V1P35_GMCH with filter network	0.1 µF 220 µF	1 1	0.1 µH (1 ohm series on CRB) from power supply to GMCH pins, with caps on GMCH side of inductor.	
VCC_ADPLLB	Connect to V1P35_GMCH with filter network	0.1 µF 220 µF	1 1	0.1 µH (1 ohm series on CRB) from power supply to GMCH pins, with caps on GMCH side of inductor.	

NOTE: Decoupling guidelines are recommendations based on our reference board design. Customers may need to take layout and PCB board design into consideration when deciding on overall decoupling solution.

12.4 Intel® 6300ESB Checklist

Note: Platforms were validated with all interfaces in use.

Caution: Inputs to the 6300ESB must not be left floating unless otherwise noted.

12.4.1 PCI-X Interface Checklist

Table 132. PCI-X Interface Checklist

Checklist Items	Recommendations	Interface not used	Reason/Impact
PXAD[32:63]	8.2 KΩ pull-up resistors to VCC3.3	May leave as no connect	
PXAD[0:31]	No extra pull-ups needed	May leave as no connect	
PXPCICLK	Ensure this pin is connected to a 66MHz clock output of the clock generator (CK409) through a 33 Ω resistor	Ensure this pin is connected to a 66MHz clock output of the clock generator (CK409) through a 33 Ω resistor	
PXRCOMP	30 Ω ±1% pull-down resistor to Vss	30 Ω ±1% pull-down resistor to Vss	Place close to the 6300ESB
PXACK64#	8.2 KΩ pull-up resistor to VCC3.3	8.2 KΩ pull-up resistor to VCC3.3	
PXM66EN	10 KΩ pull-up resistor to VCC3.3	10 KΩ pull-up resistor to VCC3.3	See *PCI-X Specification 1.0a* for more recommendations on PXM66EN connections

Table 132. PCI-X Interface Checklist

Checklist Items	Recommendations	Interface not used	Reason/Impact
PXPCIXCAP	4.7 KΩ pull-up resistor to VCC3.3 For three slot configurations 8.2 KΩ pull-up resistor to VCC3.3 For all other configurations	May leave as no connect	When the signal is read as a logic high there is no effect. (Does not support PCI-X 133 MHz). See *PCI-X Specification 1.0a* for more recommendations on PXPCIXCAP connections
PXREQ64#	8.2 KΩ pull-up resistor to VCC3.3	8.2 KΩ pull-up resistor to VCC3.3	
PXREQ[0:1]# PXREQ[2]# / GPIO[0] PXREQ[3]# / GPIO[1]	8.2 KΩ pull-up resistors to VCC3.3	8.2 KΩ pull-up resistors to VCC3.3	
PXGNT[0:1]# PXGNT[2]# / GPIO[16] PXGNT[3]# / GPIO[17]	No extra pull-ups needed	May leave as no connect	These signals are actively driven by the 6300ESB
PXDEVSEL#	8.2 KΩ pull-up resistor to VCC3.3	8.2 KΩ pull-up resistor to VCC3.3	
PXFRAME#	8.2 KΩ pull-up resistor to VCC3.3	8.2 KΩ pull-up resistor to VCC3.3	
PXIRDY#	8.2 KΩ pull-up resistor to VCC3.3	8.2 KΩ pull-up resistor to VCC3.3	
PXPAR	No extra pull-ups needed	May leave as no connect	
PXPAR64	8.2 KΩ pull-up resistor to VCC3.3	May leave as no connect	
PXPERR#	8.2 KΩ pull-up resistor to VCC3.3	8.2 KΩ pull-up resistor to VCC3.3	
PXSERR#	8.2 KΩ pull-up resistor to VCC3.3	8.2 KΩ pull-up resistor to VCC3.3	See *PCI-X specification rev 1.0a*
PXSTOP#	8.2 KΩ pull-up resistor to VCC3.3	8.2 KΩ pull-up resistor to VCC3.3	
PXTRDY#	8.2 KΩ pull-up resistor to VCC3.3	8.2 KΩ pull-up resistor to VCC3.3	
RASERR#	8.2 KΩ pull-up resistor to VCC3.3	May leave as no connect	
PXC/BE#[4:7]	8.2 KΩ pull-up resistors to VCC3.3	May leave as no connect	
PXC/BE#[0:3]	No extra pull-ups needed	May leave as no connect	
PXPCLKI	No extra pull-ups needed Ensure this is connected to PXPCLK04 through a 33 Ω resistor	No extra pull-ups needed Ensure this is connected to PXPCLK04 through a 33 Ω resistor	Feedback clock.

Table 132. PCI-X Interface Checklist

Checklist Items	Recommendations	Interface not used	Reason/Impact
PXPCLKO4	No extra pull-ups needed Ensure this is connected to PXPCLKI through a 33 Ω resistor	No extra pull-ups needed Ensure this is connected to PXPCLKI through a 33 Ω resistor	This signal is actively driven by the 6300ESB
PXPCLKO[0:3]	No extra pull-ups needed Ensure this is connected to the PCI-X/PCI Device through a 33 Ω resistor	May leave as no connect	These signals are actively driven by the 6300ESB
PXPCIRST#	No extra pull-up needed Connected to the MCH, External Controllers (LAN etc.), FWH, SIO Controllers and Glue Chip respective reset signals.	No extra pull-up needed Connected to the MCH, External Controllers (LAN etc.), FWH, SIO Controllers and Glue Chip respective reset signals.	These signals are actively driven by the 6300ESB
PXIRQ[0:3]#/ GPIO[33:36]	8.2 KΩ pull-up resistors to VCC3.3	May leave as no connect	
PXPLOCK#	8.2 KΩ pull-up resistors to VCC3.3	8.2 KΩ pull-up resistors to VCC3.3	See *PCI-X specification rev 1.0a*
PCIXSBRST#	When utilizing this pin ensure the circuit shown in Section 9.10.3 is implemented Connected to all devices that reside on the PCI-X bus.	May leave as no connect	The external circuit ensures proper functionality
IDSEL (On PCI-X Connector)	A 100 Ω series resistor on IDSEL should be connected to the PCI-X AD bus.	N/A	Improves signal quality when connected
3.3 Vaux (On PCI-X Connector)	Leave this unconnected on the PCI-X slots.	N/A	6300ESB does not support PCI-X bus power management.

12.4.2 PCI Interface Checklist

Table 133. PCI Interface Checklist (Sheet 1 of 3)

Checklist Items	Recommendations	Interface not used	Reason/Impact
DEVSEL#, FRAME#, IRDY#	Recommend an 8.2 KΩ pull-up resistor to V_{CC}3.3 or a 2.7 Ω K pull-up resistor to V_{CC}5.	Recommend an 8.2 KΩ pull-up resistor to V_{CC}3.3 or a 2.7 Ω K pull-up resistor to V_{CC}5.	See *PCI 2.2 Component Specification* pull-up recommendations for V_{CC}3.3 and V_{CC}5.
PAR	No extra pull-up needed	Recommend an 8.2 KΩ pull-up resistor to V_{CC}3.3	
PCICLK	Ensure this pin is connected to a 33MHz clock output of the clock generator (CK409) through a 33 Ω resistor	Recommend an 8.2 KΩ pull-up resistor to V_{CC}3.3	This signal is not 5 V tolerant

Table 133. PCI Interface Checklist (Sheet 2 of 3)

Checklist Items	Recommendations	Interface not used	Reason/Impact
PERR#, PLOCK#	Recommend an 8.2 KΩ pull-up resistor to $V_{CC}3.3$ or a 2.7 Ω K pull-up resistor to $V_{CC}5$.	Recommend an 8.2 KΩ pull-up resistor to $V_{CC}3.3$ or a 2.7 KΩ pull-up resistor to $V_{CC}5$.	See *PCI 2.2 Component Specification* pull-up recommendations for $V_{CC}3.3$ and $V_{CC}5$.
PME#	No extra pull-up needed.	May leave as no connect.	PME# is in the Resume power plane and has an internal pull-up resistor. See sectionSection 9.10.4 for PME# wiring recommendations.
SERR#, STOP#, TRDY#	Recommend an 8.2 KΩ pull-up resistor to $V_{CC}3.3$ or a 2.7 KΩ pull-up resistor to $V_{CC}5$.	Recommend an 8.2 KΩ pull-up resistor to $V_{CC}3.3$ or a 2.7 KΩ pull-up resistor to $V_{CC}5$.	See *PCI 2.2 Component Specification* pull-up recommendations for $V_{CC}3.3$ and $V_{CC}5$.
PIRQ[H:E]#/ GPIO[5:2]	Recommend a 2.7 KΩ pull-up resistor to $V_{CC}5$ or 8.2 KΩ resistor to $V_{CC}3.3$.	Recommend a 2.7 KΩ pull-up resistor to $V_{CC}5$ or 8.2 KΩ resistor to $V_{CC}3.3$.	In Non-APIC Mode, the PIRQx# signals may be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in Section 9.9.2. Each PIRQx# line has a separate Route Control Register. (See the 6300ESB EDS for more information.) In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: • PIRQ[E]# is connected to IRQ20 • PIRQ[F]# is connected to IRQ21 • PIRQ[G]# is connected to IRQ22 • PIRQ[H]# is connected to IRQ23

Table 133. PCI Interface Checklist (Sheet 3 of 3)

Checklist Items	Recommendations	Interface not used	Reason/Impact
PIRQ[A:D]#	Recommend a 2.7 KΩ pull-up resistor to $V_{CC}5$ or 8.2 KΩ to $V_{CC}3.3$.	Recommend a 2.7 KΩ pull-up resistor to $V_{CC}5$ or 8.2 KΩ to $V_{CC}3.3$.	In Non-APIC Mode, the PIRQx# signals may be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15 as described in Section 9.9.2. Each PIRQx# line has a separate Route Control Register. (See the 6300ESB EDS for more information.) In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: • PIRQ[A]# is connected to IRQ16 • PIRQ[B]# is connected to IRQ17 • PIRQ[C]# is connected to IRQ18 • PIRQ[D]# is connected to IRQ19
REQ#[0:3]	Recommend an 8.2 KΩ pull-up resistor to $V_{CC}3.3$ or a 2.7 KΩ pull-up resistor to $V_{CC}5$	Recommend an 8.2 KΩ pull-up resistor to $V_{CC}3.3$ or a 2.7 KΩ pull-up resistor to $V_{CC}5$	See *PCI 2.2 Component Specification* pull-up recommendations for $V_{CC}3.3$ and $V_{CC}5$.
GNT#[0:3]	No external pull-up resistors are required on PCI GNT signals. However, when external pull-up resistors are implemented they must be pulled up to $V_{CC}3.3$.	May leave as no connect	These signals are actively driven by the 6300ESB.
AD[0:31],C/BE[0:3]#	No extra pull-up needed	Recommend 8.2 KΩ pull-up resistors to $V_{CC}3.3$	
IDSEL (on PCI Connectors)	A 300 Ω to 900 Ω series resistor on IDSEL should be connected to the PCI AD bus,	N/A	Improves signal quality when connected

12.4.3 Hub Interface Checklist

Table 134. Hub Interface Checklist

Checklist Items	Recommendations	Reason/Impact
HI[11]	When HI_11 is not used: Pull to V_{SS} through a weak pull-down resistor: ~60 Ω (when trace impedance is 60 Ω) ~56 Ω (when trace impedance is 56 Ω) ~50 Ω (when trace impedance is 50 Ω)	HI[11] will be driven by the 6300ESB (should be terminated low depending on board trace resistance).
HI[0:10]	No extra pull-up resistor	
HI_STBF	No extra pull-up resistor	
HI_STBS	No extra pull-up resistor	
HICLK	Ensure this pin is connected to a 66MHz clock output of the clock generator (CK409) through a 33 Ω resistor	
HICOMP	Tie the HICOMP pin to a 52.3 Ω ±1% (when trace impedance is 60 Ω) or 48.7 Ω ±1% (when trace impedance is 56 Ω), or 43.2 Ω ±1% (when impedance is 50 Ω) pull-up resistor (to V_{CC}1_5).	ZCOMP is no longer supported.
HIREF	350 mV (See voltage divider recommendations in Section 8.1.4.)	
HI_VSWING	800 mV (See voltage divider recommendations in Section 8.1.4.)	

12.4.4 FWH/LPC Interface Checklist

Table 135. FWH/LPC Interface Checklist

Checklist Items	Recommendations	Interface not used	Reason/Impact
FWH[0:3]/ LAD[0:3]	No extra pull-ups required. Connect straight to FWH/LPC.	May leave as no connect	6300ESB integrates 20 KΩ nominal pull-up resistors on these signal lines.
LDRQ[0:1]	No extra pull-ups required. Connect straight to LPC.	May leave as no connect	6300ESB integrates 20 KΩ nominal pull-up resistors on these signal lines.
FWH[4]/ LFRAME#	No extra pull-ups required. Connect straight to FWH/LPC.	May leave as no connect	6300ESB integrates 20 KΩ nominal pull-up resistors on these signal lines.
FWH Decoupling	Follow vendor recommendation.	May leave as no connect	

12.4.5 GPIO Checklist

Table 136. GPIO Checklist

Checklist Items	Recommendations	Reason/Impact
GPIO Pins	**GPI[0:7]:** These pins are in the Core Power Well. These signals are inputs thus they need to be pulled up. Unused core well inputs must be pulled up to $V_{CC}3.3$ or $V_{CC}5$. Pull-ups (8.2 KΩ) must use the $V_{CC}3.3$ plane. Pull-ups (2.7 KΩ) must use the $V_{CC}5$ plane. GPI[0:1] may be used as REQ[2:3]#. GPI[2:5] may be used as PIRQ[E:H]#. Signals GPI[0:5] are 5 V tolerant **GPI[8] & GPI [11:13]:** These pins are in the Resume Power Well. Pull-ups (8.2 KΩ) must use the V_{CC}SUS3.3 plane. These signals are inputs thus they need to be pulled up. Unused resume well inputs must be pulled up to V_{CC}Sus3.3. These signals are **NOT** 5 V tolerant. **GPO[16:23]:** These pins are in the Core Power Well Fixed as output only. May be left NC. GPO[16:17] may be used as GNT[2:3]#. These signals are NOT 5 V tolerant. **GPO[24,25,27,28]:** I/O pins. Default as outputs so may be left as NC. These pins are in the Resume Power Well. GPIO[24,25, 28:27] From resume power well. (**Note:** Use 8.2 KΩ pull-up to $V_{CCSus}3.3$ when these signals are pulled-up). **NOTE:** These signals are **NOT** 5 V tolerant.	Ensure ALL unconnected signals are OUTPUTS ONLY!
GPIO Pins	**GPIO[32:43]:** I/O pins. From core power well. Default as outputs so may be left as NC. GPIO[32] may be used as WDT_TOUT# GPIO[33:36] may be used as PXIRQ[0:3]# GPIO[40:43] these GPIOs have High Strength Output Capability (for driving LEDs) These signals are **NOT** 5 V tolerant. **GPIO[56:57]:** Output pins. From Resume power well. These are OD signals, use 8.2 KΩ pull-ups to $V_{CCSus}3.3$	Ensure ALL unconnected signals are OUTPUTS ONLY!

12.4.6 USB Checklist

Table 137. USB Checklist

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
USBP[0:3]P, USBP[0:3]N	No external resistors are required.	May leave as no connect	Effective output driver impedance of 45 Ω provided.
OC[0:3]#	No external resistors are required.	May leave as no connect	
USBRBIAS#	Connected to the same 22.6 Ω ±1% resistor to GND as USBRBIAS.	May leave as no connect	
USBRBIAS	22.6 Ω ±1% connected to GND.	May leave as no connect	
CLK48	Ensure this pin is connected to a 48MHz clock output of the clock generator (CK409) through a 33 Ω resistor	May leave as no connect	

12.4.7 Power Management Checklist

Table 138. Power Management Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Reason/Impact
PWROK	Recommend a 10 KΩ pull-down to GND. This signal should be connected to power monitoring logic, and should go high no sooner than 100 ms after both V_{CC}3.3 and V_{CC}1_5 have reached their nominal voltages.	Timing Requirement
RSMRST#	Recommend a 10 KΩ pull-down resistor to GND. This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both V_{CC}Sus3.3 and V_{CC}Sus1_5 have reached their nominal voltages.	Timing Requirement
PWRBTN#	No extra pull-up resistors	This signal has an integrated pull-up of 18 KΩ - 42 KΩ. This signal is internally debounced inside the 6300ESB.
RI#	RI# does not have an internal pull-up. Recommend an 8.2 KΩ pull-up resistor to V_{CC}Sus3.3	When this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.
SLP_S3#, SLP_S4#, SLP_S5#	No pull up/down resistors needed.	Signals driven by 6300ESB
SUS_STAT#/LPCPD#	No extra pull-up resistors	Driven by the 6300ESB
SUSCLK	No extra pull-up resistors	Driven by the 6300ESB

Table 138. Power Management Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Reason/Impact
SYS_RESET#	Recommend an 8.2 KΩ pull-up resistor to $V_{CCSus}3.3$. Also recommend a 100 Ω to 1 KΩ pull-down resistor isolated from SYS_RESET# by means of a normally open switch.	Input to 6300ESB cannot float. This pin forces an internal reset to the 6300ESB after the signal is internally debounced.
THRM#	Connect to temperature sensor. Pull-up when not used (an 8.2 KΩ pull-up resistor to $V_{CC}3.3$).	Input to 6300ESB cannot float. THRM# polarity bit defaults THRM# to active low, so pull up.
THRMTRIP#	A pull-up resistor to the V_CPU_IO well (62 Ω). See Processor Design Guide to insure proper pull-up value.	Input to the 6300ESB cannot float.
VRMPWRGD	A 8.2 KΩ pull-up to Vcc3.3	

12.4.8 CPU Signals Checklist

Note: Ensure processor recommendations for the following signals are taken into consideration as well as the following recommendations.

Table 139. CPU Signals Checklist

Checklist Items	Recommendations	Reason/Impact
A20GATE	Pull-up signal to $V_{CC}3.3$ through a 10 KΩ resistor. or If software control of A20M# is desired, connect to a GPIO that is driven high at the rising edge of reset	Typically driven by an open drain external micro-controller. If this signal is not used pull-up to $V_{CC}3.3$ through a 10 KΩ resistor.
A20M#, CPUSLP#	No external resistors required	Push/pull buffers now drive the output signals.
FERR#	Requires a external pull-up resistor to V_CPU_IO.(62Ω)	
IGNNE#	No external resistors required	Push/pull buffers now drive the output signals.
INIT#	See Section 9.13.4 for more information.	
INTR, NMI	No external resistors required	Push/pull buffers now drive the output signals.
RCIN#	Pull-up signals to $V_{CC}3.3$ through a 10 KΩ resistor.	Typically driven by an open drain external micro-controller.
SERIRQ	External 8.2 KΩ pull-up resistor to $V_{CC}3.3$ is recommended.	
SMI#, STPCLK#	No external resistors required	Push/pull buffers now drive the output signals.

12.4.9 System Management Checklist

Table 140. System Management Checklist

Checklist Items	Recommendations	Reason/Impact
SMBCLK, SMBDATA,	Typical value of pull-up resistors is 8.2 KΩ to VccSus3.3. Value of pull-up resistors determined by line load. Connect SMLINK[0] to SMBCLK and SMLINK[1] to SMBDATA	Requires external pull-up resistors. Typical value and power well determined by SMBus Architecture and Design Consideration section. Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low power sections. In order to be fully compliant with the *SMBus 2.0 specification* (which requires the Host Notify cycle), the SMLink and SMBus signals **must** be tied together externally. This recommendation ensures proper functionality of the SMBus 2.0/SMLink Interface for legacy TCO and for cases when an external ASF controller is used.
SMLINK[1:0]	Requires external 8.2 KΩ pull-up resistors to VccSus3.3. Connect SMLINK[0] to SMBCLK and SMLINK[1] to SMBDATA	Value of pull-up resistors determined by line load. To be fully compliant with the *SMBus 2.0 specification* (which requires the Host Notify cycle), the SMLink and SMBus signals **must** be tied together externally. This recommendation ensures proper functionality of the SMBus 2.0/SMLink Interface for legacy TCO and for cases when an external ASF controller is used.
INTRUDER#	Pull signal to V_{CC}RTC (VBAT) through a 1 MΩ signal.	
SMBALERT#/ GPIO[11]	See GPIO section when SMBALERT# not implemented.	

12.4.10 RTC Checklist

Table 141. RTC Checklist

Checklist Items	Recommendations	Reason/Impact
RTCRST#	Use a 20 KΩ pull-up resistor to VccRTC and a 1.0 µF cap to ground.	Time constant due to RC filter on this line should be 18-25 ms.
RTCX1, RTCX2	Connect a 32.768 kHz Crystal Oscillator across these pins with a 10 MΩ resistor. See Section 9.11.2 for capacitor guidelines.	The external circuitry shown in Section 129 is required to maintain the RTC's accuracy. The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.
VBIAS	Ensure the VBIAS pin of the 6300ESB is connected to Vbatt through a 0.047 µF cap. (See Section 9.11.6.)	For noise immunity on VBIAS signal.

12.4.11 UART Checklist

Table 142. UART Checklist

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
SIU0_CTS#	No extra pull-ups needed	May leave as no connect	
SIU1_CTS#	No extra pull-ups needed	May leave as no connect	Internal Pull-up (15 KΩ – 35 KΩ)
SIU0_DCD#	No extra pull-ups needed	May leave as no connect	
SIU1_DCD#	No extra pull-ups needed	May leave as no connect	Internal Pull-up (15 KΩ – 35 KΩ)
SIU0_DSR#	No extra pull-ups needed	May leave as no connect	
SIU1_DSR#	No extra pull-ups needed	May leave as no connect	Internal Pull-up (15 KΩ – 35 KΩ)
SIU0_DTR#	No extra pull-ups needed	May leave as no connect	Strap Function: TOP Swap (See the 6300ESB EDS for more information) Pull-down to GND to use TOP Swap function. Value depends on platform specifics.
SIU1_DTR#	No extra pull-ups needed	May leave as no connect	Internal Pull-up (15 KΩ – 35 KΩ)
SIU0_RI#	No extra pull-ups needed	May leave as no connect	
SIU1_RI#	No extra pull-ups needed	May leave as no connect	Internal Pull-up (15 KΩ – 35 KΩ)
SIU0_RTS#	No extra pull-ups needed	May leave as no connect	Driven by the 6300ESB Do NOT pull down this signal.
SIU1_RTS#	No extra pull-ups needed	May leave as no connect	Internal Pull-up (15 KΩ – 35 KΩ)
SIU0_RXD	No extra pull-ups needed	May leave as no connect	
SIU1_RXD	No extra pull-ups needed	May leave as no connect	Internal Pull-up (15 KΩ – 35 KΩ)
SIU0_TXD	No extra pull-ups needed	May leave as no connect	
SIU1_TXD	No extra pull-ups needed	May leave as no connect	Internal Pull-up (15 KΩ – 35 KΩ)
UART_CLK	Recommend a 48 MHz clock source	May leave as no connect	See Section 9.12

12.4.12 AC'97 Checklist

Table 143. AC'97 Checklist

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
AC_BITCLK	No extra pull-down resistors required. Series termination resistor 33 Ω to 47 Ω from the motherboard codec to the 6300ESB.	May leave as no connect	This pin has a weak internal 20 KΩ nominal pull-down.
AC_RST#	No extra pull-down resistor required.	May leave as no connect	Internal Pull-down (9 KΩ -50 KΩ)
AC_SDOUT	Use a jumper to an 8.2 KΩ pull-up resistor. Should not be stuffed for default operation. Series termination resistor 0 Ω to 47 Ω to the on-board codec and to the CNR.	May leave as no connect	This pin has a weak internal 20 KΩ nominal pull-down. Strap Function: Safe Mode (See the 6300ESB EDS for more information) To properly detect a safe-mode condition, a strong pull-up will be required to override this internal pull-down.
AC_SDIN[2]	Requires a 10 KΩ pull-down to GND when a CNR card is used on the platform. Series termination resistors 33 Ω to 47 Ω from the AC_SDIN lines to the 6300ESB.	May leave as no connect	This pin has a weak internal 20 KΩ nominal pull-down. For platforms routing AC_SDIN[2] to CNR, the additional 10 KΩ pull-down is required to set the proper DC level for CNR card switching circuitry. Used for a codec detection/addressing mechanism on the CNR card.
AC_SDIN[1], AC_SDIN[0]	Internal pull-downs in the 6300ESB; no external pull-downs required. Series termination resistors 0 Ω to 47 Ω from the AC_SDIN lines to the 6300ESB.	May leave as no connect	These pins have a weak internal 20 KΩ nominal pull-down.
AC_SYNC	No extra pull-down resistor required.	May leave as no connect	Some implementations add termination for signal integrity. This signal is platform specific.

12.4.13 Miscellaneous Signals

Table 144. Miscellaneous Signals Checklist

Checklist Items	Recommendations	Reason/Impact
CLK14	Ensure this pin is connected to a 14 MHz clock output of the clock generator (CK409) through a 33 Ω resistor	

Table 144. Miscellaneous Signals Checklist

Checklist Items	Recommendations	Reason/Impact
SPKR	See Section 9.4.3 for more information.	Strap function: No Reboot (See the 6300ESB EDS for more information) Has integrated pull-down. The integrated pull-down is only enabled at boot/reset for strapping functions; at all other times, the pull-down is disabled.

12.4.14 Serial ATA Checklist

Table 145. Serial ATA Checklist

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
SATA[0:1]RXN, SATA[0:1]RXP	No extra series termination resistors or other pull-ups/pull-downs are required.	May leave as no connect	
SATA[0:1]TXN, SATA[0:1]TXP	No extra series termination resistors or other pull-ups/pull-downs are required.	May leave as no connect	
SATACLKN	Connect a 33 Ω series resistor between the CK409 and this signal	May leave as no connect	
SATACLKP	Connect a 33 Ω series resistor between the CK409 this signal	May leave as no connect	
SATALED#	Recommend a weak external pull-up to Vcc3.3	May leave as no connect	Open Drain signal
SATARBIASN	Short this signal with SATARBIASP at package. Connect to a 24.9 Ω ±1% resister to GND.	May leave as no connect	
SATARBIASP	Short this signal with SATARBIASN at package. This signal can be connected to the same 24.9 Ω ±1% resistor only if SATARBIASP is not used to connect the resistor to ground.	May leave as no connect	See section Section 9.1.1.5

12.4.15 IDE Checklist

Table 146. IDE Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
PDD[15:0], SDD[15:0]	No extra series termination resistors or other pull-ups/pull-downs are required. PDD7/SDD7 does not require a 10 KΩ pull-down resistor. Refer to *ATA ATAPI-6 specification.*	May leave as no connect	These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but may range from 21 Ω to 75 Ω.

Table 146. IDE Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Interface Not Used	Reason/Impact
PDDACK#, PDIOR#, PDIOW#, PDA[2:0], PDCS1#, PDCS3#, SDDACK#, SDIOR#, SDIOW# SDA[2:0], SDCS1#, SDCS3#	No extra series termination resistors. Pads for series resistors may be implemented should the system designer have signal integrity concerns.	May leave as no connect	These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but may range from 21 Ω to 75 Ω.
PDDREQ, SDDREQ	No extra series termination resistors. No pull down resistors needed.	May leave as no connect	These signals have integrated series resistors in the 6300ESB. These signals have integrated pull down resistors in the 6300ESB.
PIORDY, SIORDY	Pull-up to V_{CC}3.3 through 4.7 KΩ resistors. No extra series termination resistors.	Pull-up to V_{CC}3.3 through 4.7 KΩ resistors.	These signals have integrated series resistors in the 6300ESB.
IRQ14, IRQ15	Recommend 8.2 KΩ to 10 KΩ pull-up resistors to VCC3.3. No extra series termination resistors.	Pull-up to V_{CC}3.3 through 8.2 KΩ to 10 KΩ resistors.	
IDERST# (On connector)	The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal.	N/A	
Cable Detect	Host Side/Device Side Detection (*recommended method*): Connect IDE pin PDIAG#/CBLID# to an 6300ESB GPIO pin. Connect a 10 KΩ resistor to GND on the signal line. Device Side Detection: Connect a 0.047 µF capacitor from IDE pin PDIAG#/CBLID# to GND. No 6300ESB connection.	N/A	The 10 KΩ resistor to GND prevents GPI from floating when no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. **NOTE:** All Ultra DMA drives supporting modes greater than Mode 2 will have the capability to detect cables.

12.4.16 Power Checklist

Table 147. Power Checklist

Checklist Items	Recommendations	Reason/Impact
V_{CC}3.3	Use twelve 0.1 µF and four 0.01 µF decoupling caps	
V_{CC}1_5	Use six 0.1 µF and two 0.01 µF decoupling caps	
V_{CC}Sus3.3	Use four 0.1 µF, one 0.01 µF, and one 1.0 µF decoupling cap	
V_{CC}Sus1_5	Use four 0.1 µF decoupling caps	
V_CPU_IO	The power pins should be connected to the proper power plane for the CPU's CMOS Compatibility Signals. Use one 0.1 µF decoupling cap.	
V_{CC}PLL	Use three 0.1 µF decoupling caps	
V_{CC}HI	Use two 0.1 µF decoupling caps	
VCCREF	Use one 1.0 µF decoupling cap	
V5_REF	Use one 0.1 µF decoupling cap V5REF is the reference voltage for 5 V tolerant inputs in the 6300ESB. V5_REF **must** power up before or simultaneous to V_{CC}3.3. It must power down after or simultaneous to V_{CC}3.3.	Proper connection ensures functionality of system features (i.e., USB 2.0)
V5_REF_Sus	Use one 0.1 µF decoupling cap V5_REF_Sus is the reference voltage for 5 V tolerant inputs in the 6300ESB. V5_REF_Sus **must** power up before or simultaneous to V_{CC}Sus3.3. It must power down after or simultaneous to V_{CC}Sus3.3. For most platforms this is not an issue because V_{CC}Sus3.3 is usually derived from V5_REF_Sus.	Proper connection ensures functionality of system features (i.e., USB 2.0)
V_{CC}RTC	Use two 0.1 µF decoupling caps, one close to the 6300ESB, and one close to the battery. No clear CMOS jumper on V_{CC}RTC. Use a jumper on RTCRST# or a GPI, or use a safe mode strapping for Clear CMOS	
VCCA	Use one 0.1 µF decoupling cap	

Layout Checklist 13

This checklist selectively highlights some of the design considerations that should be reviewed prior to manufacturing Intel® Pentium® M/ Celeron® M processor systems that implement the Intel® 855GME/6300ESB chipset. Items contained within the checklist attempt to address important connections to these devices and any critical supporting circuitry. **This is not a complete list, and it does not ensure that a design will function properly.** Refer to details in this document and the appended Customer Reference Board schematics for complete design recommendations. The recommendations and considerations in this guide are subject to change.

The following recommendations are a summary of the information presented in this design guide. They are based on the example 8-layer stackup detailed in Chapter 3. Deviation from the example stackup will require thorough signal integrity and timing simulations.

13.1 Processor Checklist

Table 148 presents the processor layout checklist.

Table 148. Processor Layout Checklist (Sheet 1 of 7)

Checklist Items	Recommendations	Comments
Intel® Pentium® M Processor Front Side Bus Interface Signals		
A[31:3]#[1] ADSTB[1:0]#[2] DSTBN[3:0]#[3] DSTBP[3:0]#[4] DINV[3:0]# D[63:0]#[5] REQ[4:0]#[6]	• Trace impedance = 55 Ω ± 15%. • Use strip-line routing, referencing ground planes above and below the signal layer. • Route data strobes and data signals 4/12 with board trace length between 0.5 and 5.5 inches. • Use GMCH die-pad to processor pin length for all length matching operations. • Length match data strobes of the same group to within ± 25 mils of each other and to the average length of their associated data signal group. • Route all data signals as groups, on the same layer, and balance within group ± 100 mils with respect to the associated strobes. • Route address strobes 4/12 and address signals 4/8 with board trace length between 0.5 and 6.5 inches. • Trace length match address strobes to ± 200 mils of average length of their associated address signals group.	• AGTL+ Source Synchronous Signals. • Refer to Section 4.1.3 for more information.
ADS# BNR# BR0# DBSY# DRDY# HIT# HITM# LOCK# DPWR# BPRI# DEFER# RS[2:0]# TRDY#[8]	• Trace impedance = 55 Ω ± 15%. • Use strip-line routing, referencing solid ground planes. • Route traces using 4/8 mils spacing with board trace length between 1.0 and 6.5 inches. • Trace length matching is not required for common clock signals. • Package length compensation is necessary in determining minimum board trace length.	• AGTL+ Common Clock Signals. • Refer to Section 4.1.2 for more information.
RESET#[7]	• **When ITP700 Is Not Used:** • Trace impedance = 55 Ω ± 15%. • Use strip-line routing, referencing solid ground planes. • Route traces using 4/8 mils spacing with board trace length between 1.0 and 6.5 inches. • Trace length matching is not required for common clock signals. • Package length compensation is necessary in determining minimum board trace length.	• Refer to ITP Section of this layout checklist for treatment of RESET# signal when implementing ITP700FLEX debug port. • AGTL+ Common Clock Signal. • Refer to Section 4.1.6 for more information.

Table 148. Processor Layout Checklist (Sheet 2 of 7)

Checklist Items	Recommendations	Comments
6300ESB Interface Signals		
IERR#	• May be routed as a test point or to any optional system receiver. • May be routed as strip-line or micro-strip with trace impedance = 55 Ω ± 15%. • Place series resistor R1 within 3 inches of system receiver. • Place pull-up resistor Rtt within 3 inches of series resistor R1. • Pull-up voltage for termination resistor Rtt is VCCP (1.05).	• Asynchronous AGTL+ Output Signal. • Refer to Topology 1A in Section 4.1.5.1 for resistor values and trace length recommendations.
PROCHOT#	• May be routed as strip-line or micro-strip with trace impedance = 55 Ω ± 15%. • Use recommended voltage translation logic for an appropriate system receiver. • Pull-up voltage for termination resistor Rtt is VCCP (1.05) • Place series resistor Rs at the beginning of trace T-split and within 3 inches from Q1.	• Asynchronous AGTL+ Output Signal. • Refer to Topology 1C in Section 4.1.5.3 for resistor values and trace length recommendations.
FERR# THERMTRIP#	• Connect FERR# to the processor and the Intel® 6300ESB. • Recommend connecting processor signal THERMTRIP# to the 6300ESB, but may be connected to any optional system receiver, with consideration for any voltage level translation if necessary. • May be routed as strip-line or micro-strip with trace impedance = 55 Ω ± 15%. • Place series resistor R1 within 3 inches of system receiver. • Place pull-up resistor Rtt within 3 inches of series resistor R1. • Pull-up voltage for termination resistor Rtt is VCCP (1.05).	• Asynchronous AGTL+ Output Signals. • Refer to Topology 1B in Section 4.1.5.2 for resistor values and trace length recommendations. • Refer to Section 4.1.5.7 for voltage translation recommendations.
IPWRGOOD	• May be routed as strip-line or micro-strip with trace impedance = 55 Ω ± 15% • Route point-to-point between an AND gate output (AND of PWRGD_3V and CPU_VR_PWRGD) signal and CPU signal PWRGOOD, trace length range between 0.5 and 12 inches. • Place a termination resistor Rtt within 3 inches of CPU pin. T-split routing should not be used. • Pull-up voltage for termination resistor Rtt is VCCP (1.05)	• Asynchronous Open Drain CMOS Input Signal. • Refer to Topology 2A in Section 4.1.5.4 for resistor values and detailed routing recommendations.

Table 148. Processor Layout Checklist (Sheet 3 of 7)

Checklist Items	Recommendations	Comments
IGNNE# LINT0/INTR LINT1/NMI SMI# SLP# A20M# STPCLK#	• May be routed as strip-line or micro-strip with trace impedance = 55 Ω ± 15%. • Implement a point-to-point connection between the 6300ESB and CPU, trace length range between 0.5 and 12 inches. • No additional components are necessary for this topology.	• Asynchronous CMOS Input Signals. • Refer to Topology 2B in Section 4.1.5.5.
INIT#	• May be routed as strip-line or micro-strip with trace impedance = 55 Ω ± 15%. • Route signal point-to-point between the 6300ESB and CPU, trace length range between 0.5 and 12 inches. • Voltage level translation is required from the 6300ESB INIT# pin to FWH. • Place series resistor Rs at the beginning of trace T-split and within 3 inches from Q1.	• Asynchronous CMOS Input Signal. • Refer to Topology 3 in Section 4.1.5.6 for resistor values and trace length recommendations. • Refer also to Section 4.1.5.7 for more details on voltage translation recommendations. • The Intel customer reference board makes use of an optional alternative circuit for FWH voltage translation. Refer to schematic appendix.
Processor In Target Probe (ITP) Signals for ITP700FLEX Debug Port		
BPM[3:0]# PRDY# PREQ#	• Route as a point-to-point transmission line connections from CPU pins to the ITP700FLEX connector via Zo = 55 Ω ± 15% traces. Limit trace length to shorter than 6 inches. **ITP700** to **CPU** BPM[3:0]# BPM[3:0]# BPM4# PRDY# BPM5# PREQ# • Length match to each other within ± 50 ps. • These signals also must be length matched to the net lengths of the RESET# signal within ± 50 ps, as detailed in Section 4.3.1.1. • Keep a minimum of 2:1 spacing in between these signals and to other signals. • Reference these signals to ground planes and avoid routing across power plane splits. • The number of routing layer transitions should be minimized. When layout constraints require a routing layer transition, any such transition shall be accompanied with ground stitching vias placed within 100 mils of the signal via with at least one ground via for every two signals making a layer transition.	• Refer to Section 4.3 for important design considerations when implementing ITP700FLEX. • Refer to Section 4.1.1.4 for details on signal propagation time to distance relationships for the length matching requirements shown in this table as periods of time. • Refer to Section 4.1.10 for default strapping and placement when ITP debug port is not implemented.

Table 148. Processor Layout Checklist (Sheet 4 of 7)

Checklist Items	Recommendations	Comments
RESET#[7]	• **When ITP700 Is Used**: • Fork out this signal from GMCH (**do not T-split**) and route to CPU and to Rtt/Rs termination network placed near ITP700FLEX debug connector. • Complete routing by connecting Rs to the ITP700FLEX connector, limiting trace length to less than 0.5 inches (L3). • Rtt is pulled-up to VCCP and should be placed right next to Rs. • Trace length from GMCH to the Rtt/Rs network near the debug connector should be limited to less than 6 inches (L2). • The forked trace from the GMCH to the CPU should be limited to a length range of 1 to 6 inches (L1). • ITP700FLEX debug operation requires matching L2 + L3 - L1 length to within ± 50 ps of the length of the BPM[4:0] signals detailed above. • Keep a minimum of 2:1 spacing in between these signals and to other signals. • Reference these signals to ground planes and avoid routing across power plane splits. • The number of routing layer transitions should be minimized. When layout constraints require a routing layer transition, any such transition shall be accompanied with ground stitching vias placed within 100 mils of the signal via with at least one ground via for every two signals making a layer transition.	• Refer to Section 4.1.6 and Section 4.3 for details on ITP700FLEX/RESET# routing recommendations and resistive network resistor values.
DBR#	• **When ITP700 Is Used**: • Route to system reset logic with a pull-up resistor to target system VCC. • Place pull-up resistor within 1 ns of the ITP700FLEX debug connector.	
TCK	• **When ITP700 Is Used**: • Fork out this signal from the CPU (**do not T-split**) and route to the TCK pin and the FBO pin of ITP700FLEX debug connector. • Parallel termination resistor to ground is placed within ±200 ps of ITP700 connector.	• Refer to Section 4.3.1.1 for details on routing CPU TAP logic signals for ITP700 debug operation.
TDI	• **When ITP700 Is Used**: • Route between CPU and debug connector pin. • Parallel termination resistor to VCCP is placed within ±300 ps of CPU pin.	

Table 148. Processor Layout Checklist (Sheet 5 of 7)

Checklist Items	Recommendations	Comments
TDO	• **When ITP700 Is Used**: • Route from CPU pin to a pull-up resistor to VCCP placed near the debug connector TDO pin. • Place a series resistor connecting the pull-up resistor to the ITP700FLEX debug connector, limiting trace length from the series resistor to the debug connector to less than 1 inch.	
TRST#	• **When ITP700 Is Used**: • Route between CPU and debug connector pin. • Parallel termination resistor to ground should be placed anywhere between CPU and ITP700. Avoid any trace stub from signal line to parallel termination resistor.	
TMS	• **When ITP700 Is Used**: • Route between CPU and debug connector pin. • Parallel termination resistor to VCCP should be placed within ±200 ps of the ITP700FLEX debug connector pin.	
Other Signals		
BCLK, BCLK#	• Refer to Section 11.2.1 for a detailed discussion on this topic. • CPU BCLK, BCLK# from CK409 should be routed as differential pairs and length matched to the GMCH BCLK, BCLK# signals. • When routing the 100 MHz differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground. • If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents. • Do not place vias between adjacent complementary clock traces. • Vias placed in one half of a differential pair must be matched by a via in the other half. • Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1. • **When ITP700 Is Used**: • ITP BCLK, BCLK# should be routed with similar recommendations, but should be length matched to within ±50 ps of the system bus clock pairs and the additional length of the BPM[4:0]# signals, to ensure correct operation of ITP700FLEX.	• Refer to host clock group routing guidelines detailed in Section 11.2.1. • Refer to Chapter 10 for detailed breakdown of all system clock routing recommendations.

Table 148. Processor Layout Checklist (Sheet 6 of 7)

Checklist Items	Recommendations	Comments
COMP[0,2]	• Terminate each signal to ground with 27.4Ω ±1% resistors. • Connect each to CPU with a Zo = 27.4Ω trace that is less than 0.5 inches from the pin. • Spacing from other switching signal traces should be a minimum of 25 mils.	• Refer to Section 4.1.9.1 for detailed layout recommendations.
COMP[1,3]	• Terminate each signal to ground with 54.9Ω ±1% resistors. • Connect each to CPU with a Zo = 55Ω trace that is less than 0.5 inches from the pin. • Spacing from other switching signal traces should be a minimum of 25 mils.	• Refer to Section 4.1.9.1 for detailed layout recommendations.
Processor Power and GND Measurement/Sense Signals		
VCCSENSE VSSSENSE	• Route traces of equal length using 3:1 spacing, Zo = 55 Ω ± 15%. • Place via next to the processor socket's pin for measurement of CPU_VCC/VSS. • Place a ground via 100 mils from each test point via. • All other signals shall be a minimum of 25 mils (preferably 50 mils) from VCCSENSE and VSSSENSE routing.	• Refer to Section 4.1.11 for more information.
Processor Decoupling, VREF, and Filtering		
GTLREF	• Connect CPU GTLREF pin to a 1 K Ω ± 1% and 2 K Ω ± 1% resistive divider to VCCP. • No decoupling on this signal. • Connect voltage divider node to CPU GTLREF pin with a Zo = 55 Ω trace that is shorter than 0.5 inches • Minimum separation from other switching signals should be 25 mils.	• Refer to Section 4.1.8 for more information.

Table 148. Processor Layout Checklist (Sheet 7 of 7)

Checklist Items	Recommendations	Comments
VCC (CORE) Decoupling	• Recommended bulk decoupling: • (4) 220 µF SP caps - ESR 12 mΩ (max) and ESL 3.5 µH, placed near CPU north power corridor (pin map row AF). • Recommended mid-frequency decoupling: • (35) 10 µF 0805 caps - ESR 5 mΩ (typ) and ESL 0.6 nH placed in and near package outline. • Sharing of vias between several VCC-CORE pins or ground pins is not allowed.	• It is highly recommended that decoupling guidelines detailed in Section 4.4.3 be followed for efficient VRM performance.
VCCP Decoupling	• Recommended bulk decoupling: • (2) 150 µF POSCAP - ESR 42 mΩ (typ) and ESL 2.5 nH, placed one each near the CPU and the GMCH packages. • (10) 0.1 µF X7R 0603 caps - ESR 16 mΩ (typ) and ESL 0.6 nH, placed on the secondary side within the CPU package outline.	• Refer to Section 4.4.4 for processor VCCP decoupling recommendations.

NOTES:
1. A[31:3]# pins on the processor correspond to HA[31:3]# pins on the GMCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the GMCH.
3. DSTBN[3:0]# pins on the processor correspond to HDSTBN[3:0]# pins on the GMCH.
4. DSTBP[3:0]# pins on the processor correspond to HDSTBP[3:0]# pins on the GMCH.
5. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the GMCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the GMCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the GMCH. Refer to the ITP portion of this checklist, Section 4.1.6 and Section 4.3.1.1 for treatment of RESET# when using ITP700FLEX debug port.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the GMCH.

13.2 Intel® 855GME Chipset GMCH (82855GME) Layout Checklist

Table 149 presents the Intel® 855GME chipset GMCH layout checklist.

Table 149. Intel® 855GME Chipset GMCH Layout Checklist (Sheet 1 of 6)

Checklist Items	Recommendations	Comments
Host Interface Signals		
ADS# BNR# BPRI# BREQ0#[1] CPURST#[2] DBSY# DEFER# HA[31:3]#[3] HD[63:0]#[4] HADSTB[1:0]#[5] HDSTBN[3:0]#[6] HDSTBP[3:0]#[7] HIT# HITM# HLOCK#[10] HREQ[4:0]#[8] HTRDY#[9] DRDY# RS[2:0]# DINV[3:0]#	• Refer to the Processor section of this checklist.	
DDR System Memory Interface		
SCK[5:0] SCK[5:0]#	• Refer to the detailed discussion on this topic in Section 5.4.3 • Route as closely-coupled differential pairs, 3 clock pairs to each DIMM. • Spacing to other DDR signals should not be less than 20 mils. Isolation from non-DDR signals should be 25 mils. • Route on internal layers, except for pin escapes. • Nominal internal trace width 7 mils and nominal internal spacing 4 mils. • Routed trace length limits are 3.5 to 6.5 inches. • Length match clock pairs to ±10 mils. • Match all DIMM0 clocks to X0 ± 25 mils • Match all DIMM1 clocks to X1 ± 25 mils • Match all DIMM0 clock lengths and match all DIMM1 clock lengths. • Use GMCH package lengths for pad-to-pin length tuning. • Differential mode impedance is 70 ohms ± 15% • Maximum breakout length is 0.3 inches • Maximum via count of 2 per side	• Refer to the detailed routing guidelines in Section 5.4.3.

Table 149. Intel® 855GME Chipset GMCH Layout Checklist (Sheet 2 of 6)

Checklist Items	Recommendations	Comments
SDQ[71:0] SDM[8:0] SDQS[8:0]	• See a detailed discussion on this topic in Section 5.4.4 • Route SDQ/SDM with trace impedance 55 Ω ± 15% using 2:1 spacing. • Route SDQS strobes similarly with 3:1 spacing. • Isolation from non-DDR signals should be 20 mils. • Overall min/max length to the DIMM must comply with clock length matching requirements. • The full data bus SDQ[63:0], mask bus SDM[7:0], and strobe signals SDQS[7:0] should be routed on the same internal signal layer. • It is required that the SDQ byte group and the associated SDM and SDQS signals within a byte lane be routed on the same internal layer. • Maximum recommended via count per signal is 6.	• Refer to the detailed routing guidelines in Section 5.4.4.
SCKE[3:0] SCS[3:0]#	• See a detailed discussion on this topic in Section 5.4.5 • Route with trace impedance 55 Ω ± 15% using 2:1 spacing. • Isolation from non-DDR signals should be 20 mils. • GMCH pad to DIMM trace length limits are 2 to 6 inches. • Place parallel termination resistor within 2 inches of DIMM pad. • Overall min/max length to the DIMM must comply with clock length matching requirements. • Maximum recommended via count per signal is 3.	• Refer to the detailed routing guidelines in Section 5.4.5.
SRAS# SCAS# SWE# SMA[12:6,3,0] SBA[1:0]	• See a detailed discussion on this topic in Section 5.4.6. • Route with trace impedance 55 Ω ± 15% using 2:1 spacing. • Isolation from non-DDR signals should be 20 mils. • GMCH pad to first DIMM trace length limits are 2 to 5.5 inches. • Total DIMM to DIMM spacing should be less than 2 inches. • Place parallel termination resistor within 1.5 inches of the second DIMM pad. • Overall min/max length to the DIMM must comply with clock length matching requirements. • Maximum recommended via count per signal is 6.	• Refer to the detailed routing guidelines in Section 5.4.6.

Table 149. Intel® 855GME Chipset GMCH Layout Checklist (Sheet 3 of 6)

Checklist Items	Recommendations	Comments
SMA[5,4,2,1] SMAB[5,4,2,1]	• See a detailed discussion on this topic in Section 5.4.7. • Route with trace impedance 55 Ω ± 15% using 2:1 spacing. • Isolation from non-DDR signals should be 20 mils. • GMCH pad to DIMM trace length limits are 2 to 6 inches. • Place parallel termination resistor within 2 inches of the DIMM pad. • Overall min/max length to the DIMM must comply with clock length matching requirements. • Maximum recommended via count per signal is 3.	• Refer to the detailed routing guidelines in Section 5.4.7.
RCVENIN# RCVENOUT#	• Internally shunted on Intel 855GME chipset - no external connection necessary. • Recommendation is that both signals be transitioned to the secondary side with vias next to the package balls to facilitate probing.	• Refer to the detailed routing guidelines in Section 5.4.8.
DDR System Memory Decoupling		
GMCH VCCSM Decoupling	• Requires a minimum of (11) 0603, 0.1 µF caps placed within 150 mils of the GMCH package. • Distribute evenly along the DDR memory interface, placed perpendicular to the GMCH with the power side of the caps facing the GMCH. • Each GMCH ground and VCCSM power ball should have its own via. • Each via should be as close to the associated cap pad as possible, within 25 mils and with as thick a trace as possible. • Two 150 µF caps between GMCH and 1st DIMM.	• Refer to Section 4.8.1.1 for more information.
DDR VDD Bypass Caps	• Place 9 evenly spaced 0.1 µF 0603 caps between the DIMMs. • A wide trace from each cap should connect to a via that transitions to the ground plane layer. • A wide trace should connect the 2.5 V side of each cap to a via that transitions to the 2.5 V plane, each via placed as close to the cap pad as possible. • Each cap should also connect to the closest 2.5 V DIMM pin on either DIMM connector with a wide trace. • Four 100 - 150 µF caps near the DIMMs.	• Helps minimize return path discontinuities. • Refer to Section 4.8.1.2 for more information.

Table 149. Intel® 855GME Chipset GMCH Layout Checklist (Sheet 4 of 6)

Checklist Items	Recommendations	Comments
DDR VTT Decoupling	• Decouple VTT termination rail using one 0603 0.1 µF capacitor per two DDR signals. • Spread out placement across the VTT termination rail, connecting directly to the rail, so that each parallel termination resistor is within 100 mils of one of these high-frequency capacitors. • Each ground via should be as close to the associated cap pad as possible, within 25 mils and with as thick a trace as possible. • Also, place one 4.7 µF ceramic capacitor on each end of the termination island, and place one 4.7 µF ceramic capacitor near the center of the termination island. • Low frequency bulk decoupling requirements at the VTT termination rail should be met with (4) 470 µF caps placed evenly across the VTT rail, including one cap at each end.	• Refer to Section 4.8.1.3 for more information.
Hub Interface		
General Guidelines	• Route hub interface data and strobes with trace impedance 55 Ω ± 15% using 2:1 spacing and VSS reference. • Route hub interface strobe and its complement as a differential pair, length matched within ± 10 mils. • Maximum length for both data and strobe signals is 6 inches. • Hub interface data and strobe signals are routed on the same layer, transitioning together when a layer change is required. • Keep layer changes to a minimum, using only 2 vias per net.	• Refer to Section 8.1 for detailed routing recommendations. • The platform design guide example references routing guidelines for the 8-bit Hub Interface using enhanced (parallel) termination.
Clocks and Reset Signals		
BCLK BCLK#	• For a detailed discussion on this item, see Section 11.2.1. • The differential host clock pair should be length matched to ± 10 mils and to the processor BCLK/BCLK# pair within ± 20 mils overall (match L1 segments to ± 10 mils across all pairs). • Route as strip-line traces 4/7 mils spacing (except as allowed for pin escapes). • Total length range is 2 to 8.5 inches.	• Refer to host clock group routing guidelines detailed in Section 11.2.1. • Refer to Chapter 10 for detailed breakdown of all system clock routing recommendations.

Table 149. Intel® 855GME Chipset GMCH Layout Checklist (Sheet 5 of 6)

Checklist Items	Recommendations	Comments
GCLKIN	• Place series resistor close to CK409, within 500 mils. • Total trace length range is 4 to 9 inches. • Minimum spacing 20 mils. • Overall length of CLK66 is considered the reference length for all other CLK66 and CLK33, except USBCLK and CLK14. • The length of CLK66 traces should be matched within ± 100 mils and then used as the basis for defining the length of all other length matched clocks.	• Refer to CLK66 clock group routing guidelines detailed in Section 11.2.1.
RSTIN#	• Connect to PCIRST# output of the 6300ESB.	
GMCH Decoupling, VREF, and Filtering		
HLRCOMP HLVREF PSWING	• GMCH HLRCOMP signal should be strapped to 1.2 V via 27.4 Ω ± 1% HLRCOMP resistor with trace impedance 55 Ω ± 15%. • HLVREF and PSWING voltage requirements must be set appropriately for proper hub interface operation. The case is similar for HIREF and HIVSWING signals on 6300ESB.	• Refer to Section 8.1.4 for HI specific voltage requirements and several options for voltage divider circuits.
HXRCOMP HYRCOMP	• Each signal should be pulled to ground with a 27.4 Ω ± 1% resistor. • Max trace length to the resistor should be less than 0.5 inches and should be 18 mils wide to achieve the characteristic impedance target of 27.4 Ω. • Maintain 25 mil separation from any switching signals.	• This signal is used to calibrate the Host AGTL+ I/O buffers characteristics to specific board characteristics. • Refer to Section 4.8.3.2 for more information.
HDVREF[2:0] HAVREF HCCVREF	• Max length from pin to voltage divider for each reference voltage should be less than 0.5 inches. • 10 mil traces are recommended.	• To provide constant and clean power delivery to the data, address, and common clock signals of the host AGTL+ interface. • Refer to Section 4.8.3.1 for recommended individual voltage divider circuits.

Table 149. Intel® 855GME Chipset GMCH Layout Checklist (Sheet 6 of 6)

Checklist Items	Recommendations	Comments
HXSWING HYSWING	• Voltage divider components for each input should be placed within 0.5 inches of their respective pins. • Use a 15 mil wide trace maintaining a minimum of 25 mils separation to other signals.	• The HXSWING and HYSWING inputs of GMCH are used to provide reference voltage for the compensation logic. • Refer to Section 4.8.3.3 for more information.
Analog Power Filtering	• There are 8 analog circuits that require filtered supplies on the Intel 855GME chipset.	• Refer to Section 4.8.3.4 for detailed filter requirements.

NOTES:
1. The BREQ0# pin on the GMCH corresponds to the BR0# pin on the processor.
2. The CPURST# pin on the GMCH corresponds to the RESET# pin on the processor.
3. HA[35:3]# pins on the GMCH correspond to A[31:3]# pins on the processor.
4. HD[63:0]# pins on the GMCH correspond to D[63:0]# pins on the processor.
5. HADSTB[1:0]# pins on the GMCH correspond to ADSTB[1:0]# pins on the processor.
6. HADSTBN[3:0]# pins on the GMCH correspond to DSTBN[3:0]# pins on the processor.
7. HADSTBP[3:0]# pins on the GMCH correspond to DSTBP[3:0]# pins on the processor.
8. HREQ[4:0]# pins on the GMCH correspond to REQ[4:0]# pins on the processor.
9. The HTRDY# pin on the GMCH corresponds to the TRDY# pin on the processor.
10. The HLOCK# pin on the GMCH correspond to LOCK# pin on the processor.

13.3 Intel® 6300ESB Layout Checklist

13.3.1 8-Bit Hub Interface Layout Checklist

Table 150. 8-Bit Hub Interface Layout Checklist

#	Layout Recommendations	Comments
1	Data traces need to be routed 5 mils wide with 15 mils spacing.	
2	Strobe traces need to be routed 5 mils wide with 20 mils spacing from other signals, 15 mils spacing intra-pair.	
3	In order to breakout of the MCH and 6300ESB package the Hub Interface signals may be routed 5 on 5. Signals need to be separated within 300 mils of the package.	
4	Maximum trace length is eight inches.	
5	Data signals must be matched within ±0.25 inches of the HI_STB differential pair.	
6	HI_STB/HI_STBS and HI_STB#/HI_STBF lengths need to be matched.	
7a	(Single Reference Driver Circuit only) HIREF divider should be placed no more than four inches of away from MCH or 6300ESB.	
7b	(Local Reference Divider Circuit only) HIREF dividers should be placed no more than four inches of away from MCH or 6300ESB.	
8	HI signals need to be referenced to ground.	

13.3.2 Serial ATA Interface Layout Checklist

Table 151. Serial ATA Interface Layout Checklist

#	Layout Recommendations	Comments
1	Route SATA signals ground referenced.	
2	Route SATA signals using a minimum of vias and corners. This reduces signal reflections and impedance changes. Use a maximum of two vias per trace. Vias should be matched on traces within a transmit or receive pair.	
3	When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.	
4	Do not route SATA traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.	
5	Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch when possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to SATA signals, high-speed clocks, as well as slower signals that might be coupling to them.)	
6	Keep SATA signals clear of the core logic set. High current transients are produced during internal state transitions. These transients may be difficult to filter out.	
7	Keep traces at least 90 mils away from the edge of the plane (Vcc or GND depending on which plane to which the trace is routed). This helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB.	
8	Maintain parallelism between SATA differential signals with the trace spacing needed to achieve 79.3 Ω differential impedance. (Recommended: 7 mils width, 6 mils spacing.)	
9	Minimize the length of high-speed clock and periodic signal traces that run parallel to SATA signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 100 mils.	
10	Use 100 mils minimum spacing between SATA signal pairs and other signal traces. This helps to prevent crosstalk.	
11	SATA signal pair traces should be trace length matched. Max trace length mismatch between SATA signal pair (such as TXN and TXP) should be no greater than 10 mils.	
12	Maximum length from the 6300ESB to the SATA connector should not be greater than eight inches.	
13	SATARBIASP and SATARBIASN should be routed 5 on 5 with a single trace 500 mils or less to the 24.9 Ω 1% resistor to ground.	

13.3.3 IDE Interface Layout Checklist

Table 152. IDE Interface Layout Checklist

#	Layout Recommendations	Comments
1	Traces need to be routed 5 mils wide and 7 mils spaces	
2	Max trace length is eight inches long.	
3	The two strobe signals must be matched within 100 mils of each other. The data lines must be within ± 500 mils of the average length of the two strobe signals.	
4	If series resistors are used, they should be placed close to the IDE connector.	

13.3.4 USB 2.0 Layout Checklist

Table 153. USB 2.0 Layout Checklist (Sheet 1 of 2)

#	Layout Recommendations	Comments
1	With minimum trace lengths, route high-speed clock and USB differential pairs first.	
2	Route USB signals ground referenced.	
3	Route USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.	
4	When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.	
5	Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.	
6	Stubs on USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. When a stub is unavoidable in the design, the sum of all stubs on a given data line should not be greater than 200 mils.	
7	Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch when possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.)	
8	Keep USB signals clear of the core logic set. High current transients are produced during internal state transitions, which may be difficult to filter out.	
9	Keep traces at least 90 mils away from the edge of the plane (V_{CC} or GND depending on which plane to which the trace is routed). This helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB.	
10	Maintain parallelism between USB differential signals with the trace spacing needed to achieve the target differential impedance.	

Table 153. USB 2.0 Layout Checklist (Sheet 2 of 2)

#	Layout Recommendations	Comments
11	Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 100 mils.	
12	Use 45 mils minimum spacing between USB signal pairs and other signal traces. This helps to prevent crosstalk.	
13	USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pair (such as DM1 and DP1) should be no greater than 60 mils.	
14	No termination resistors are needed for USB.	
15	Short USBRBIAS and USBRBIAS# at the package, connect with a 5 mils width, 5 mils spacing single trace 500 mils or less to the 22.6 Ω 1% resistor to ground.	
16	Maximum length from the 6300ESB to the backpanel should not exceed recommend length	
17	Maximum length from the 6300ESB to the CNR should not exceed recommend length	
18	Maximum length from the 6300ESB to the Front Panel connector should not exceed recommend length	

13.3.5 AC'97 Layout Checklist

Table 154. AC'97 Layout Checklist

#	Layout Recommendations	Comments
1	5 mils trace width, 10 mils spacing between traces.	
2	AC_SDIN Max Trace Length 6300ESB to the Primary Codec or CNR connector is 14 inches	
3	AC_SDOUT Max trace length 6300ESB to the Primary Codec or CNR connector is 14 inches	
4	AC_BIT_CLK Max trace length 6300ESB to the Primary Codec or CNR connector is 14 inches	
5	Series termination resistor on AC_BIT_CLK line should be no more than 3.0 to 8.0 inches from the 6300ESB.	

13.3.5.1 RTC Layout Checklist

Table 155. RTC Layout Checklist

#	Layout Recommendations	Comments
1	RTC LEAD length = one inch maximum	
2	Minimize capacitance between RTCX1 and RTCX2.	
3	Put GND plane underneath Crystal components.	
4	Don't route switching signals under the external components (unless on other side of board).	

Table 155. RTC Layout Checklist

#	Layout Recommendations	Comments
5	RTC signals should be ground referenced.	

13.3.6 PCI-X Layout Checklist

Table 156. PCI-X Layout Checklist

#	Layout Recommendations	Comments
1	Eight inches maximum to the first slot, then 1.5 inches to each subsequent slot. PCI-X clocks and loop-back clocks are scaled accordingly. (See Section 9.10.1 through Section 9.10.2 for more information.)	
2	Place the PXRCOMP pull-down resistor as close to the 6300ESB as possible	
3	IDSEL (See Section 9.10.2.)	
4	Signals should be routed with 5 mils trace width and 12 mils spacing. (edge-to-edge)	

13.3.7 PCI Layout Checklist

Table 157. PCI Layout Checklist

#	Layout Recommendations	Comments
1	Ten inches maximum to the first slot, then one inch to each subsequent slot. PCI clocks and loop-back clocks are scaled accordingly (see Figure 120 for more information).	
2	Signals should be routed with 5 mils trace width and 7 mils spacing.(edge-to-edge)	
3	Clock signals should be routed with 5 mils trace width and 50 mils spacing.(edge-to-edge)	
4	IDSEL (See Section 9.10.2 for more information.)	

13.3.8 FWH Decoupling Layout Checklist

Table 158. FWH Decoupling Layout Checklist

#	Layout Recommendations	Comments
1	0.1 µF capacitors should be placed between the V_{CC} supply pins and the V_{SS} ground pins, no less than 390 mils from the V_{CC} supply pins.	
2	4.7 µF capacitors should be placed between the V_{CC} supply pins and the V_{SS} ground pins, no less than 390 mils from the V_{CC} supply pins.	

13.3.9 Power Delivery Checklist

Table 159. Power Delivery Checklist

#	Layout Recommendations	Comments
1	Standby power rails (V5REF_Sus & VccSus3_3) should be implemented though planes.	Will reduce trace antennae effect
2	Decoupling capacitors should be placed as close as possible to the package (100 mils nominal)	See Section 4.8.9 for more details on capacitor placement

Schematics A

The following schematics of the Intel® 855GME chipset are included in this section.

- Cover Page
- TABLES: Block Diagram
- TABLES: Reset Map
- TABLES: Clock Distribution
- TABLES: GPIO/IDSEL Mapping
- TABLES: Voltage Distribution
- CORE: CK_409 (Main Clock Generation)
- CORE: CPU Connector, 1 of 2
- CORE: CPU Connector, 2 of 2
- CORE: CPU Pull-Ups, PLL Circuitry, TJPRO Connector
- CORE: GMCH
- CORE: GMCH Circuitry
- CORE: GMCH PLL, Straps, LVDS Clock Generation
- CORE: DDR Series Termination
- CORE: DIMM Connectors
- CORE: DDR Parallel Termination (Strobes, CNTRL)
- CORE: DDR Vterm Caps
- CORE: AGP Digital Display Connector
- CORE: VGA Connector
- ICH: 6300ESB
- ICH: ICH Pull-up/Pull-downs
- CORE: LVDS
- ICH: IDE Primary and Secondary
- ICH: USB Back Panel Connectors
- ICH: USB Front Panel VREG and OC#
- ICH: PCI Slots 3 - 1
- ICH: PCI Pull-ups
- SMBUS Isolation
- LAN: 82562EM
- AUDIO: Codec (AD1885 or CS4201)
- AUDIO: Codec Filtering Caps

- AUDIO: Aux-In, CD-In, Line-In: ATAPI Headers
- AUDIO: Mic-In
- AUDIO: Line-Out
- AUDIO: Front Panel Audio Header
- AUDIO: Transient Control
- AUDIO: Analog VREG
- SIO: LPC47M102
- SIO: Floppy
- SIO: Keyboard and Mouse Ports (PS/2)
- SIO: Parallel Port
- SIO: COM1
- FWH: MFG Mode and Recovery Jumpers
- GLUE4
- PC Speaker
- Front Panel Header
- Mounting Holes
- FAN: Fan Headers (3)
- VREG: 2.5 V Memory, Standby Memory
- VREG: 1.25 V Memory VVT
- VREG: ATX Power Connector 2X10
- VREG: Battery, PCI VAUX, USB_NCH and USB_PCH
- VREG: USB Back Panel, PS/2
- VREG: 1.5 V Stand-by and 3.3 V Stand-by
- VREG: Bulk Decoupling
- VREG: 2.5 V STR Decoupling
- VREG: Core 1.5 V
- VREG: IMVP-IV
- VREG: CPU Decoupling, CPU VREG Decoupling
- DEBUG: ITP Port and Pull-ups
- Revision History