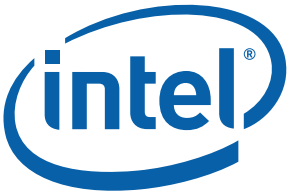

Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit

User's Guide

October 2008

Order Number: 320067-002US

Contents

Figures

Tables

Revision History

Date	Revision	Description
August 2008	001	Initial release
October 2008	002	Updated Section 6.1.13 and included new graphics in Sections 2, 3, 5, 6.

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1.0 Introduction

This document provides user guide information for the Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit. The document contains a high-level description of the Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit, technical reference, configuration and setup information. The document also includes Pre-boot Firmware usage and recovery information.

Note: The "Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Board" is referred to as "Intel® EP80579 Development Board" throughout this document.

The "Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit" is referred to as "Intel® EP80579 Development Kit" throughout this document.

1.1 Document Organization

The following chapters are included in this document:

- Chapter 1.0, "Introduction" gives an overview of the information contained in this document, as well as a list of acronyms.
- Chapter 2.0, "Product Specification" introduces key features of the Intel® EP80579 Development Board.
- Chapter 3.0, "System Overview" provides a system overview of the Intel® EP80579 Development Board.
- Chapter 4.0, "Technical Reference" includes an illustration of LEDs, connector locations, connector/header descriptions, and pinout tables.
- Chapter 5.0, "Pre-boot Firmware" provides an introduction to AMI Aptio* 4.5 Pre-boot Firmware on the Intel® EP80579 Development Board.
- Chapter 6.0, "Platform Setup" provides specifics for configuring the Intel® EP80579 Development Board.
- Chapter 7.0, "Error Messages and Beep Codes" lists Port 80h POST codes, system initialization checkpoints and provides a brief description of each.
- Chapter 8.0, "Socketed Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Extraction and Insertion Instructions" provides instructions how to extract and insert the Intel® EP80579 Integrated Processor from the Intel® EP80579 Development Board.

1.2 Related Documents

Table 1 lists the hardware, software and platform documents that will assist in the development process:

Table 1. Related Documents

Document Title	Document Number
Intel® EP80579 Integrated Processor Product Line Datasheet	320066-001
Intel® EP80579 Integrated Processor Product Line Platform Design Guide	320068-001

1.3 Acronyms

Table 2 describes acronyms that are used throughout this document.

Table 2. Acronym Table (Sheet 1 of 2)

Acronym	Description
ACPI	Advanced Configuration and Power Interface specification
APIC	Advanced Programmable Interrupt Controller
ASU	Acceleration Services Unit
BIOS	Basic Input/Output System
CAN	Controller Area Network specification
DDR2	Double Data Rate 2
DEC	Double-bit Error Detection
DIMM	Dual In-line Memory Module
ECC	Error Checking and Correction
EFI	Extensible Firmware Interface specification
EHCI	The Enhanced Host Controller Interface (EHCI) specification describes the register-level interface for a Host Controller for the Universal Serial Bus (USB) Revision 2.0
FPGA	Field-Programmable Gate Array
FSB	Front Side Bus
FXO	Foreign Exchange Office
FXS	Foreign Exchange Subscriber
FWH	Firmware Hub
GbE	Gigabit Ethernet
HSS	High Speed Serial Bus
IA	Intel Architecture
LEB	Local Expansion Bus
MAC	Media Access Controller
PCIe	PCI Express*
PHY	Physical Layer Device
POST	Power-On Self-Test
PXE	Pre-Boot Execution Environment
SATA	Serial ATA
SEC	Single-bit Error Correction

Table 2. Acronym Table (Sheet 2 of 2)

Acronym	Description
SIO	Super IO Controller
SMBIOS	System Management BIOS specification
SPI	Serial Peripheral Interface Bus
SOC	System on Chip
UART	Universal Asynchronous Receiver/Transmitter
UHCI	Universal Host Controller Interface
USB	Universal Serial Bus

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2.0 Product Specification

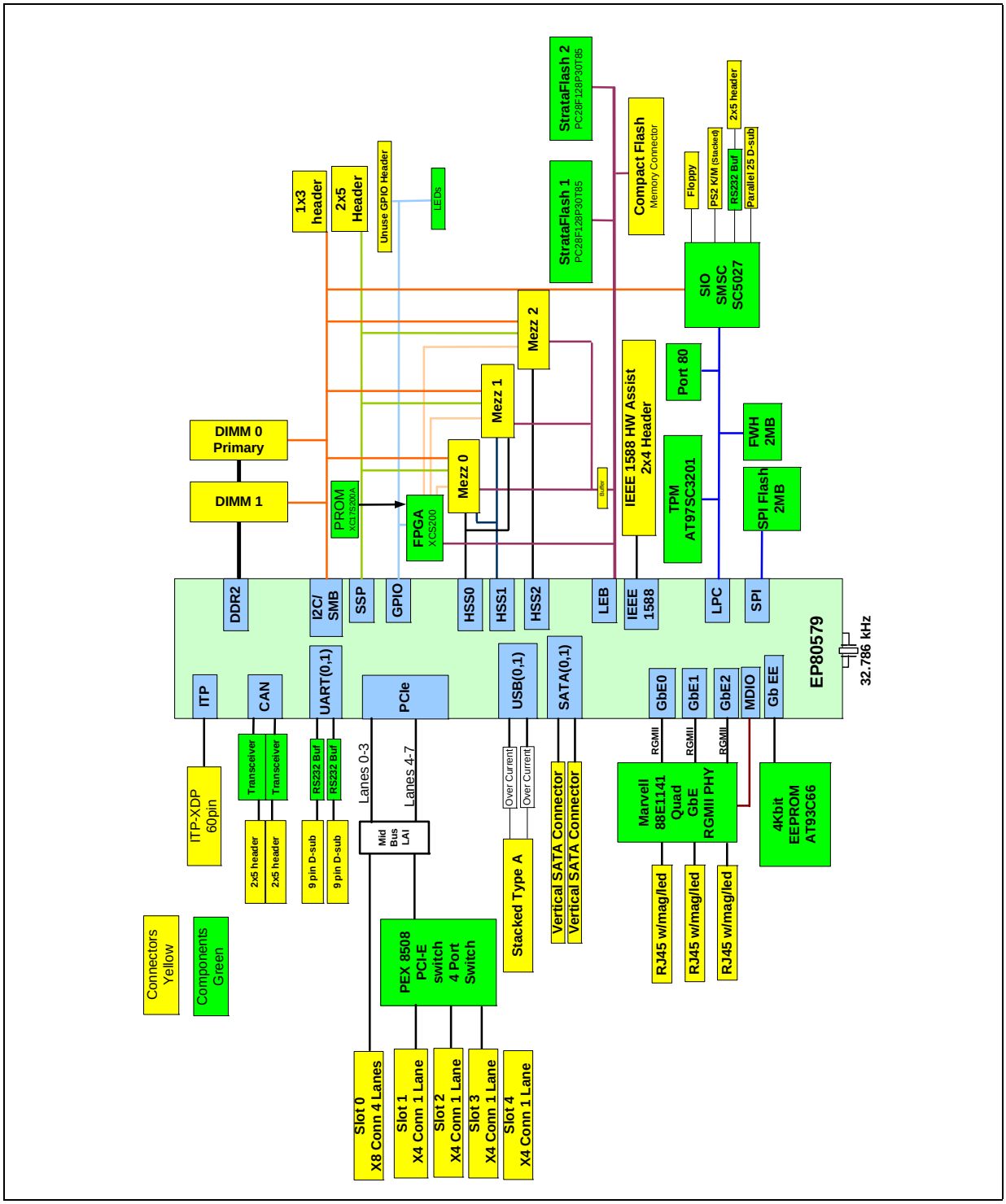
2.1 Overview

This chapter contains an overview of the Intel® EP80579 Development Kit product specifications. See the *Intel® EP80579 Integrated Processor Product Line Platform Design Guide* for implementation details.

2.1.1 Product Description and Board Architecture

Figure 1 shows the functional blocks of the Intel® EP80579 Development Board.

Figure 1. Block Diagram of the Intel® EP80579 Development Board



2.1.2 Feature List

Table 3 summarizes the major features of the Intel® EP80579 Development Board.

Table 3. Feature List

Feature	Description	Comments
Form Factor	13.00 inches x 10.75 inches	
SOC (processor and chipset)	Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology	Integrated IA SOC
Video	External PCIe card	Matrox Millennium G550 PCIe
System Memory	• Support for two 240-pin DDR2 DIMMs • Support for 400\533\667\800 MHz DDR2 • Support for 256 MB to 4 GB memory • Support for ECC and non-ECC • Support for both registered and unbuffered DIMMs	For DDR2-800 MHz, only single rank or dual rank DIMM on DIMM 0 slot is supported
Pre-boot Firmware	• EFI v1.1 compliant based on AMI Aptio* 4.5	
Peripheral/IO Interfaces	• Three UART ports • Three Gigabit Ethernet (GbE) with RJ45 ports • Two Controller Area Network (CAN) buses with 2x5 headers • Two USB ports • Two SATA ports • One floppy drive interface • PS/2 mouse and keyboard • One parallel port • CompactFlash* connector	• Two USB ports support UHCI or EHCI configurations • Two serial ports supported from SOC connected to 9-pin D-sub and the 3rd serial port from SIO connected to 2x5 header • Two SATA ports support Gen 2.0
Expansion Capabilities	• One PCI Express x4 interface in x8 slot • Four PCI Express x1 interfaces in x4 slots • Three HSS/SSP/LEB mezzanine slots	Mezzanine slots provide support for acceleration services SKU applications
Firmware Hub and SPI Flash	• Socketed 2 MB FWH • Socketed 2 MB SPI Flash	Selectable Boot Options between FWH and SPI Flash.
Hardware Control or Monitor Subsystem	• Voltage sensor to detect out of range voltage values • Thermal sensor to detect out of range thermal values • One processor and three AUX fan connectors • Fan speed control	

2.2 Package Components

The complete package for the Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Develpment Kit includes the following:

- Intel® EP80579 Integrated Processor:
  - — One Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology at 1200 MHz (installed with heatsink and fan)
  - — One Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology at 600 MHz (supplied)
- Hardware:
  - — Memory SDRAM: One 1 GB DDR2 800 MHz
  - — Video Card: One PCI Express* x1 Graphics Adapter card
  - — Hard drive: SATA hard drive

  - DVD-ROM drive: SATA DVD-ROM drive
- Cable:
  - 10-pin header to DB9 Serial cable: CAN interface adapter cables (also used for SIO Tertiary UART)
  - Serial ATA cables
  - Power cord
- Power Supply:
  - One standard ATX12V power supply

2.3 System I/O

2.3.1 Intel® EP80579 Development Board I/O

The Intel® EP80579 Integrated Processor provides the following I/O capabilities on the Intel® EP80579 Development Board:

- Two DDR2 DIMM sockets
- Two UART ports
- Two SATA ports
- Two USB ports
- Two CAN interfaces
- Three HSS/SSP/LEB mezzanine slots
- One x4 PCI Express* interface in x8 slot
- Four x1 PCI Express interfaces in x4 slots through PEX 8508 PCIe switch
- Three GbE RJ45 ports

Note: The mezzanine slots support add-in cards. See Section 2.10 for order information for supported add-in cards.

2.3.2 Super I/O (SIO)

The Intel® EP80579 Development Board utilizes SIO to provide the following I/O capabilities:

- PS/2 mouse and keyboard port
- One parallel port
- One floppy drive interface
- One UART port

2.3.3 PEX 8508 PCI Express* Switch

The Intel® EP80579 Integrated Processor provides a x8 PCI Express interface that is configured as two independent x4 PCI Express interfaces. One of the x4 PCI Express interfaces is connected to a PEX 8508 PCI Express switch to provide support for four x1 PCI Express interfaces in x4 slots.

2.3.4 Marvell* 88E1141 Quad Ethernet Transceiver

The Quad Ethernet transceiver is a Gigabit Ethernet physical layer device (PHY). The three GbE MAC controllers from the Intel® EP80579 Integrated Processor are connected to a 88E1141 Quad Ethernet Transceiver to provide three GbE RJ45 ports over copper.

Note: The Intel® EP80579 Development Board does not support Wake On LAN (WOL), but the Intel® EP80579 Integrated Processor does support WOL.

2.4 System Memory

The Intel® EP80579 Development Board has two DIMM sockets and supports the following memory features:

- DDR2-400, DDR2-533, DDR2-667, DDR2-800 registered/unbuffered DIMM
- Two single-rank or one dual-rank DIMM(s) (for DDR2-800 MHz, only one single-rank or dual-rank DIMM on DIMM 0 slot is supported)
- ECC or Non-ECC (with ECC enabled, SEC/DED are supported)
- Total system memory: Minimum 256 MB and maximum 4 GB
- 256 Mbit, 512 Mbit, 1 Gbit, and 2 Gbit density parts in the x8 configuration

Table 4 shows the memory configurations that are supported by the Intel® EP80579 Development Board.

Table 4. DDR2 Memory Configuration

DDR2[1] Frequency	DIMM 1	DIMM 0
400	Registered	Registered
400	Empty	Registered
400	Unbuffered	Unbuffered
400	Empty	Unbuffered
533	Registered	Registered
533	Empty	Registered
533	Unbuffered	Unbuffered
533	Empty	Unbuffered
667	Registered	Registered
667	Empty	Registered
667	Unbuffered	Unbuffered
667	Empty	Unbuffered
800	Empty	Registered
800	Empty	Unbuffered
1. Actual supported frequencies are determined by the SKU used.		

Note: Certain restrictions apply when two ranks are used. Both ranks need to be either:

- Registered or unbuffered. Mixing of registered and unbuffered ranks is not supported.
- 64-bit mode only. 32-bit mode does not supported dual rank.

2.4.1 Supported DIMM Slot Populations

Table 5 shows the supported DDR2 DIMM populations.

Table 5. Supported DIMM Slot Populations

DIMM Configuration	DIMM1	DIMM0
1 Single Rank	Empty	Populated
2 Single Rank	Populated	Populated
1 Dual Rank	Empty	Populated

2.5 Supported Operating Systems

The Intel® EP80579 Development Kit is validated with the following operating systems:

- Red Hat Enterprise Linux* 5
- FreeBSD* 6.2
- Microsoft Windows* XP Embedded* SP2

Note: Operating systems are not distributed with the Intel® EP80579 Development Board, kit, or processor.

2.6 Supported Pre-boot Firmware Features

The Intel® EP80579 Integrated Processor Pre-boot Firmware is based on the AMI Aptio* 4.5 core and is compliant with the EFI v1.1 specification.

Table 6 provides an overview of the Pre-boot Firmware features.

Table 6. Pre-boot Firmware Features (Sheet 1 of 2)

Feature	Description
Boot devices	Supports booting from: • SATA hard drive • SATA DVD-ROM drive • USB drive • Floppy drive • LAN card in PCIe slot • PXE boot from internal GbE ports
PCI Express	Initializes and supports PCI Express cards that are plugged into the Intel® EP80579 Integrated Processor Product Line
USB	Supports USB 1.1 and USB 2.0 interfaces
CMOS header	Detects clearing CMOS with clear CMOS header
Watchdog timer	Supports two-stage Watchdog timer
APIC and ACPI control	Provides ability to enable and disable APIC and ACPI support. Supported ACPI states: • G0(S0) - Working • G1(S3) - Sleeping [Suspend to RAM] • S4 - Suspend to disk • G2(S5) - Soft Off Supports C0, C1, and C2 states

Table 6. Pre-boot Firmware Features (Sheet 2 of 2)

Feature	Description
Memory	Detects and supports ECC/Non-ECC memory
Functionality control	Provides all possible options for enabling or disabling Intel® EP80579 Integrated Processor functionality: • Parallel Port • USB 0/1 • SATA 0/1 • SATA Gen2 • CAN 0/1 • SSP 0/1 • PCI Express Controller Port A0/A1 • GbE 0/1/2
Serial console redirection	Provides console redirection through serial port

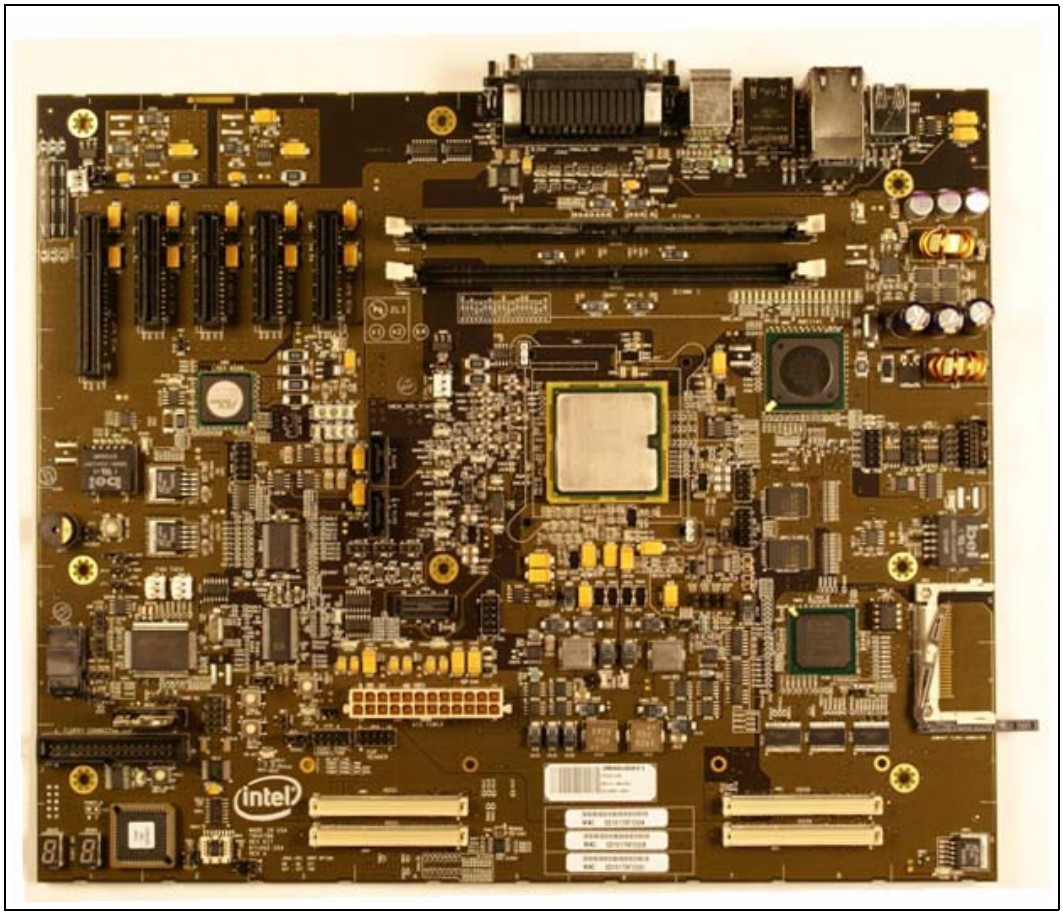
2.7 Intel® EP80579 Development Board Overview

Table 7 and Figure 2 identify the Intel® EP80579 Development Board.

Table 7. Intel® EP80579 Development Kit Revision Identification and Color Scheme

Product	GPIO 1	GPIO 0	Board Solder Mask Color
Intel® EP80579 Development Board	1	1	Black

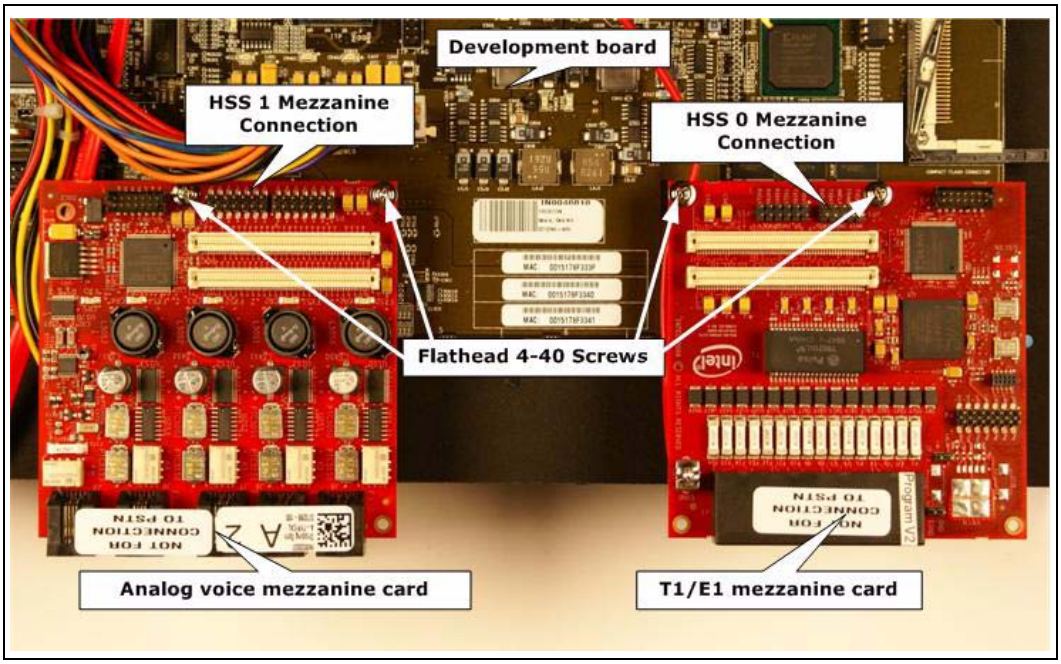
Figure 2. Intel® EP80579 Development Board



2.8 Mezzanine Cards

The Intel® EP80579 Development Board supports two types of mezzanine cards: the Intel® EPAVM80579 Analog Voice Mezzanine Card (4-port analog voice card) and the Intel® EPTEM80579 Quad T1/E1 Mezzanine Card (quad T1/E1 card). Figure 3 shows the mezzanine cards installed onto the Intel® EP80579 Development Board. The mezzanine card(s) can be installed into any HSS port connector. See Section 2.10 for ordering information.

Figure 3. Mezzanine Cards



2.9 Power Supply

The Intel® EP80579 Development Kit comes with a standard, off-the-shelf ATX12V power supply.

2.10 Ordering Information

Table 8. Ordering Information

Product Name	Product Code	MM#
Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit	EP80579TRXDK	898430
Intel® EPTEM80579 Quad T1/E1 Mezzanine Card (quad T1/E1 card)	EP80579TRXT1E1	898435
Intel® EPAVM80579 Analog Voice Mezzanine Card (4-port analog voice card)	EP80579TRXVOI	898436

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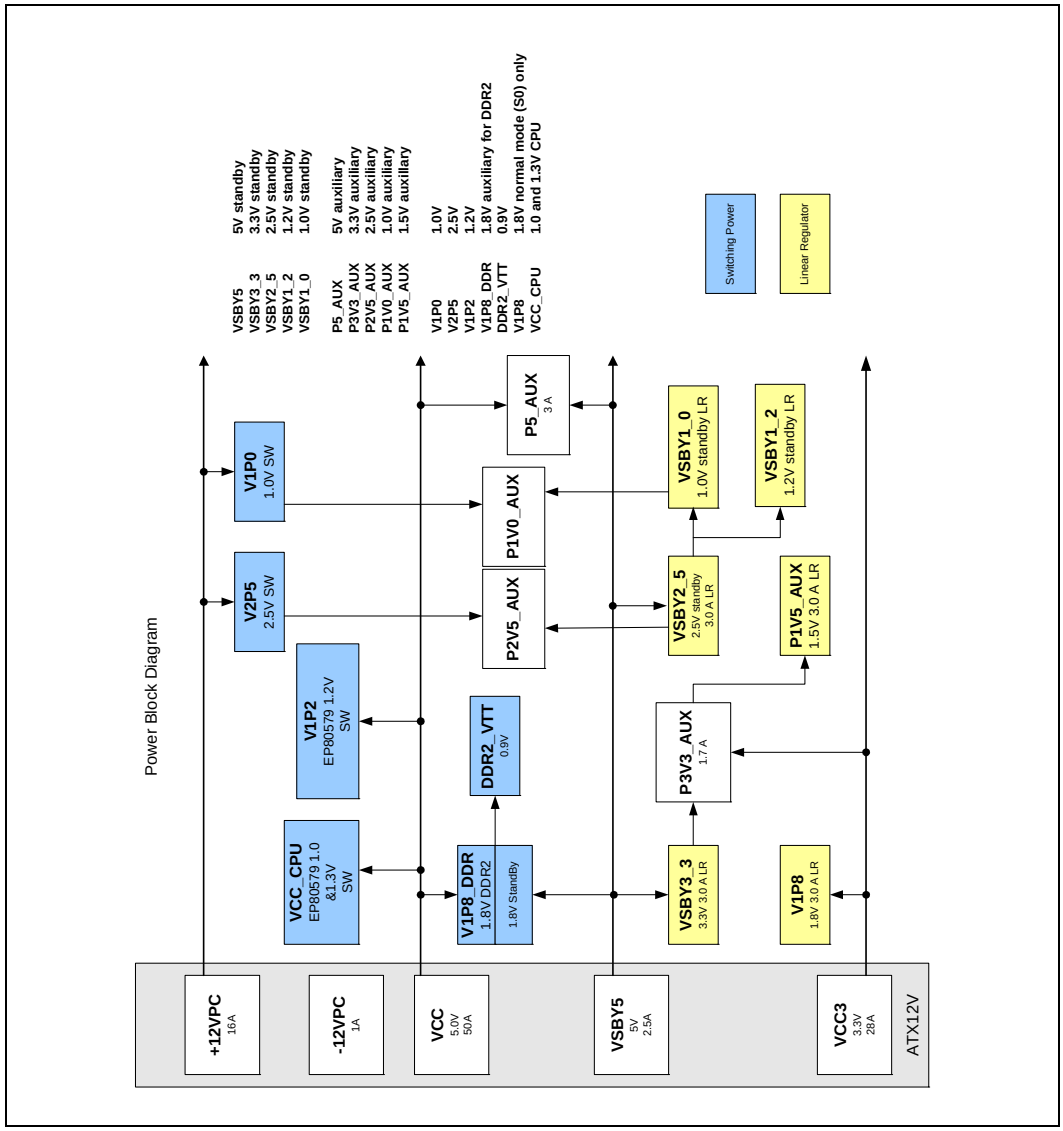
3.0 System Overview

3.1 Power Distribution

Figure 4 shows the power distribution for the Intel® EP80579 Development Board. For details on power distribution logic, see the Schematics and bill of materials for the Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit.

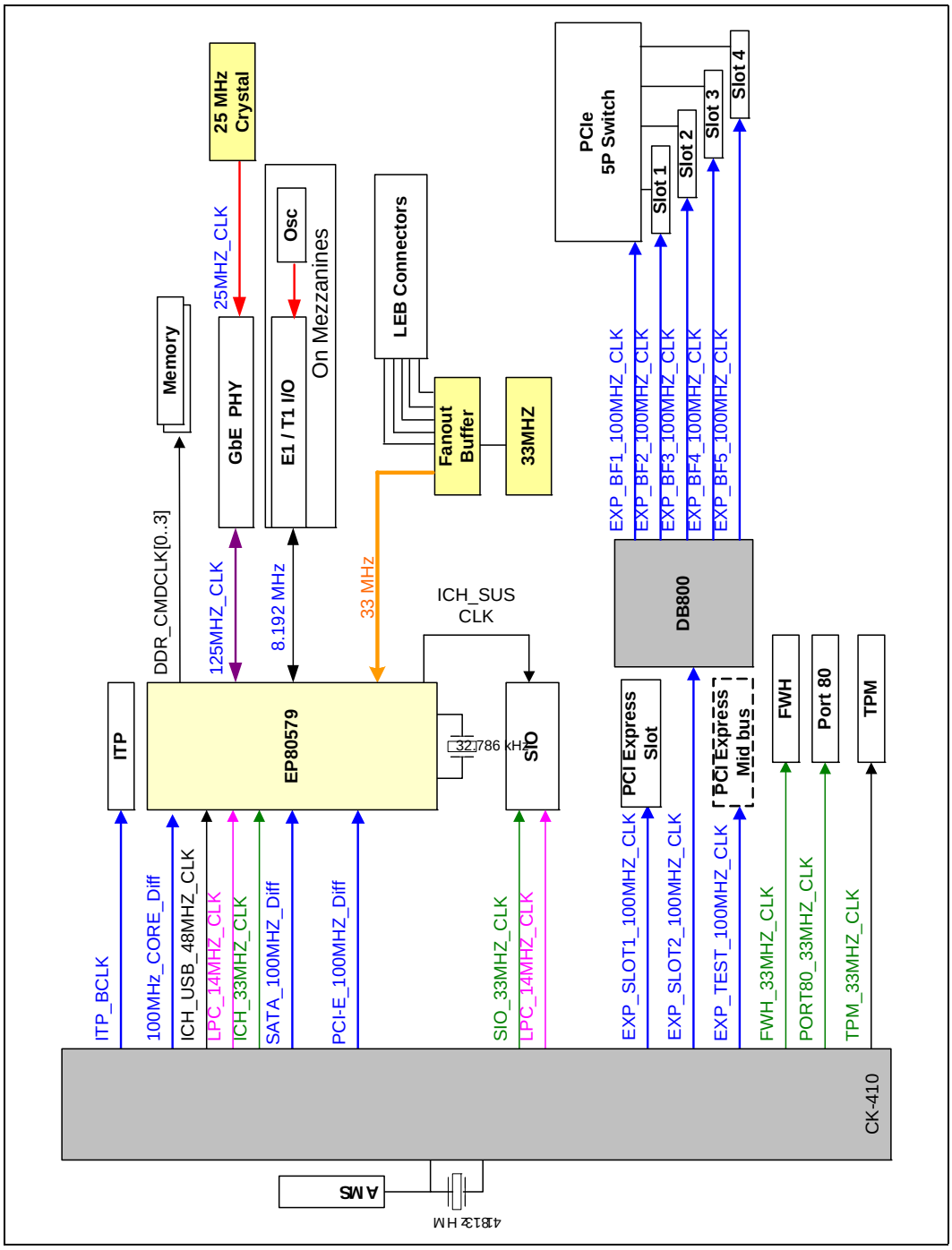
Figure 4. Power Distribution Block Diagram



3.2 Platform Clocking

The Intel® EP80579 Development Board uses one CK-410 clock synthesizer to generate the host differential pair clocks and the 100 MHz differential clock to the DB800. The DB800 then generates the 100 MHz differential pair clock for PCI Express devices. Figure 5 shows the board clocking configuration.

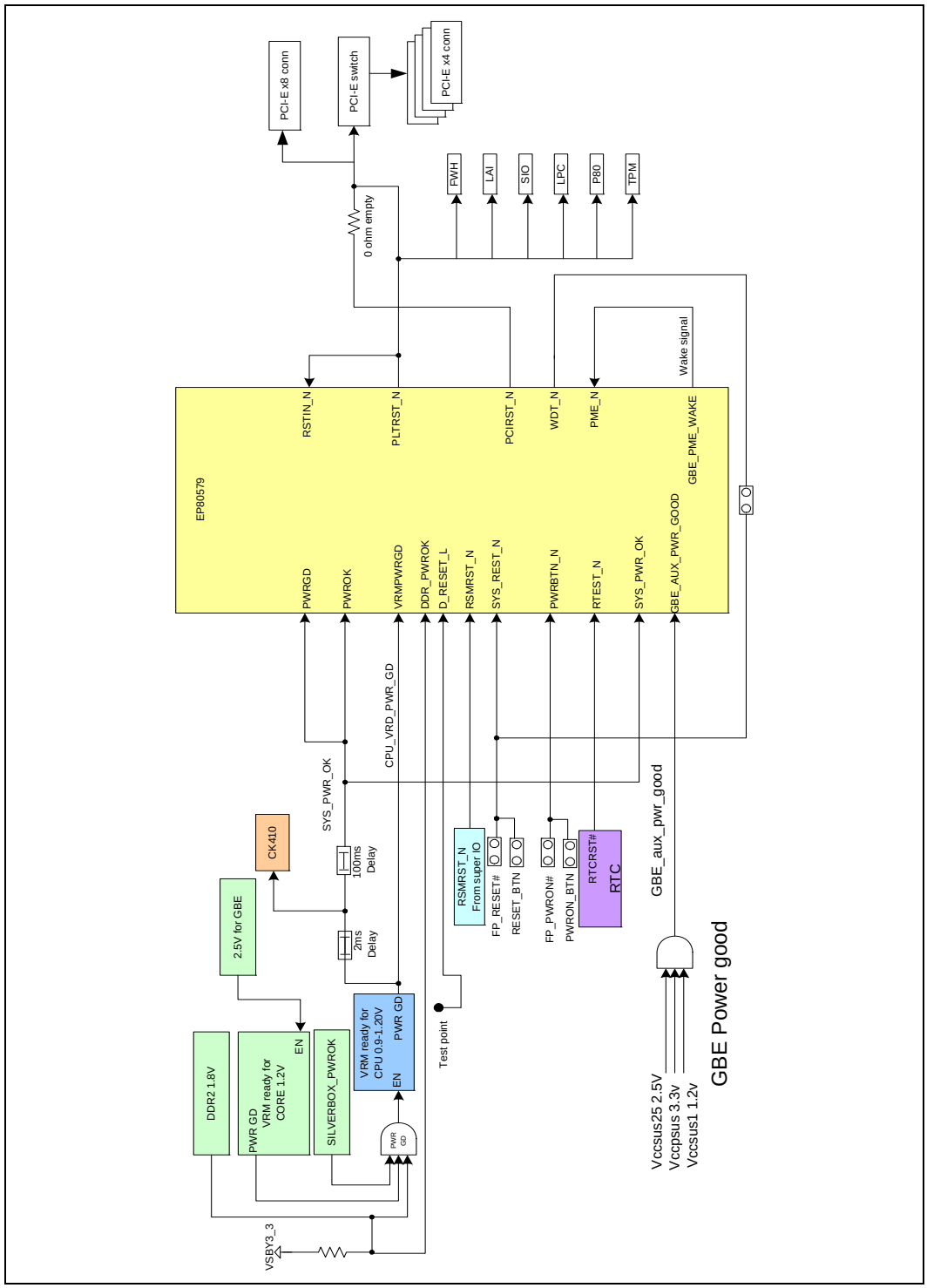
Figure 5. Clock Block Diagram



3.3 Platform Reset

Figure 6 depicts the reset logic for the Intel® EP80579 Development Board.

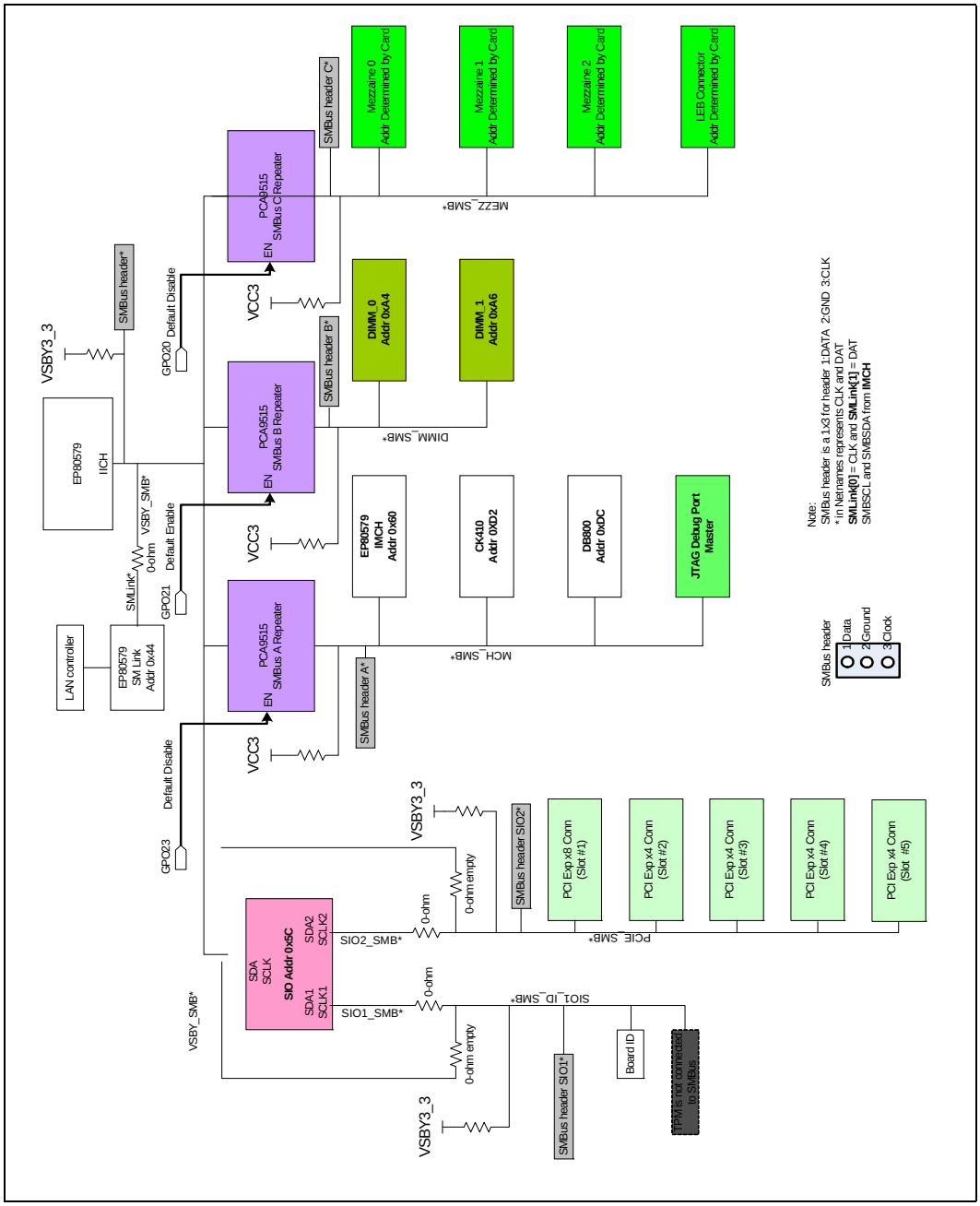
Figure 6. Reset Diagram



3.4 SMBus

The Intel® EP80579 Development Board provides system management communication through SMBus connectivity. The SMBus is implemented as a single bus with three repeaters used for voltage translation, fan out and isolation on the Intel® EP80579 Development Board. Figure 7 shows the block diagram of the SMBus system on the Intel® EP80579 Development Board.

Figure 7. SMBus System Block Diagram



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4.0 Technical Reference

This chapter provides hardware reference information for the Intel® EP80579 Development Board, including location of components, connector/header pinout information, jumper settings and switch settings. Figure 8 shows the Intel® EP80579 Development Board components layout.

4.1 Board Components Layout

Figure 8 and Figure 9 show the front view and back view of the Intel® EP80579 Development Board. Figure 10 shows the external peripheral connectors. Table 9 identifies the components and connectors called out in Figure 8, Figure 9, and Figure 10.

Figure 8. Front View of the Board Components

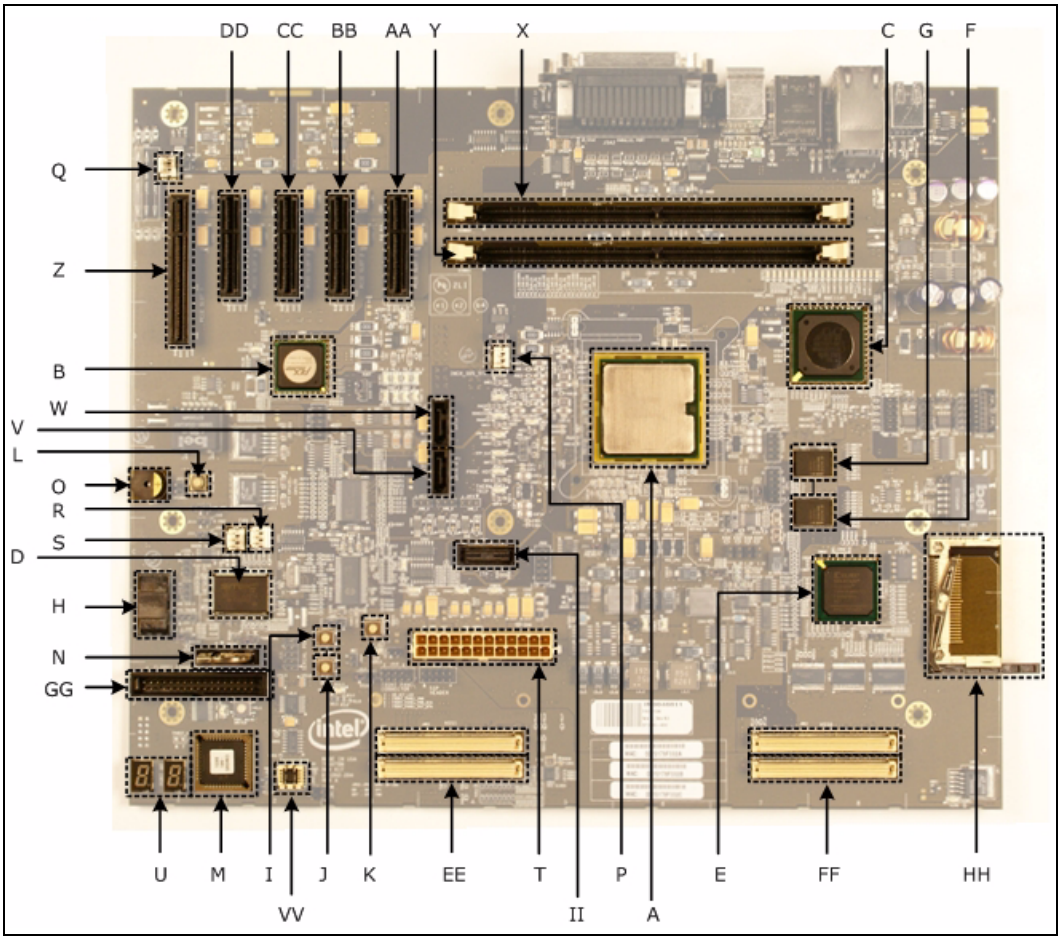


Figure 9. Back View of the Board Components

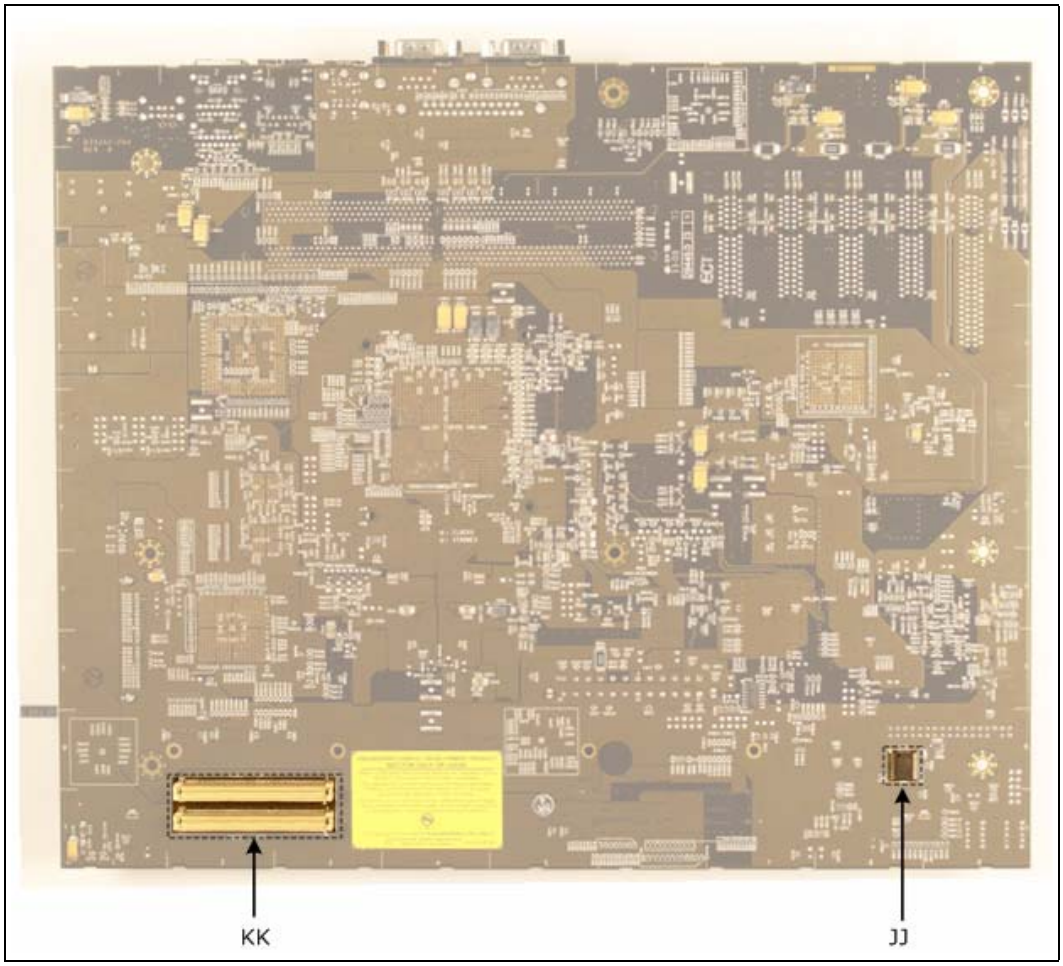


Figure 10. Side View of the Board Connectors

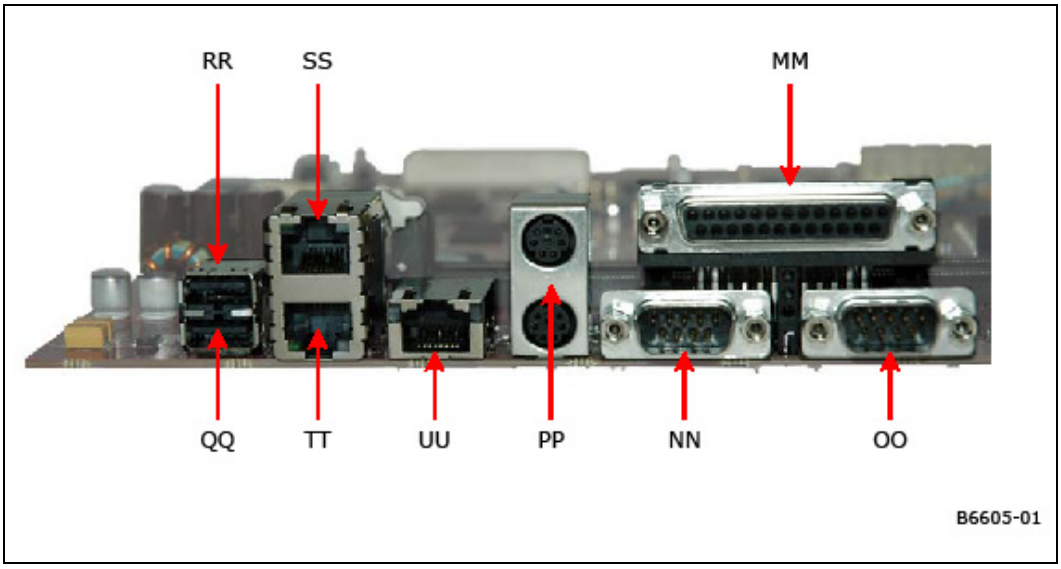


Table 9. Component and Connector Layout Description (Sheet 1 of 2)

Call-out	Component/Connector
A	Intel® EP80579 Integrated Processor
B	PEX PCIe Switch Chip
C	Marvell 88E1141 Quad PHY
D	Super IO Controller
E	FPGA
F	Flash memory 0
G	Flash memory 1
H	FWH
I	Power button
J	Reset button
K	Sleep button
L	PCIe Wake button
M	Port 80 IC
N	CMOS battery
O	On-board speaker
P	CPU FAN connector
Q	AUX FAN connector
R	AUX0 FAN connector
S	AUX1 FAN connector
T	ATX power connector
U	Two 7-segment display (Port 80)
V	SATA port 0
W	SATA port 1

Table 9. Component and Connector Layout Description (Sheet 2 of 2)

Call-out	Component/Connector
X	DDR2 DIMM0
Y	DDR2 DIMM1
Z	Slot 0 x8 connector 4 lanes PCI Express
AA	Slot 1 x4 connector 1 lane PCI Express
BB	Slot 2 x4 connector 1 lane PCI Express
CC	Slot 3 x4 connector 1 lane PCI Express
DD	Slot 4 x4 connector 1 lane PCI Express
EE	Mezzanine connector 1
FF	Mezzanine connector 0
GG	Floppy Connector
HH	CF connector
II	ITP-XDP connector
JJ	Trusted Platform Module
KK	Mezzanine connector 2
MM	Parallel port
NN	COM0 (Intel® EP80579 UART Port 0)
OO	COM1 (Intel® EP80579 UART Port 1)
PP	PS/2 mouse (top)/keyboard (bottom)
QQ	USB port 0
RR	USB port 1
SS	RJ-45 Ethernet port 0
TT	RJ-45 Ethernet port 1
UU	RJ-45 Ethernet port 2
VV	SPI Flash

4.2 IA-32 Core Frequency Selection

The Intel® EP80579 Integrated Processor Product Line is offered in SKUs with a 1200 MHz, 1066 MHz or 600 MHz IA-32 core frequency. The Intel® EP80579 Development Board is designed to use the Intel® EP80579 Integrated Processor's V_SEL and BSEL signals to provide the required input clocks and voltages for each of these IA-32 cores. For Intel® EP80579 Integrated Processor SKUs with the 1200 MHz IA-32 core, V_SEL can be used to force the IA-32 core to run at 1066MHz.

Note: 1200 MHz SKUs can be run at 1066 MHz (but not at 600 MHz).

1066 MHz SKUs can only run at 1066 MHz.

600 MHz SKUs can only run at 600 MHz

Table 10 describes how to configure the Intel® EP80579 Development Board to support the different IA-32 core frequencies.

Table 10. Intel® EP80579 IA-32 core Frequency Selection

IA-32 core Maximum Operating Frequency (MHz)	Desired IA-32 core Operating Frequency (MHz)	J7F2 Jumper Setting (V_SEL in Table 13)	J7G6 Jumper Setting (BSEL in Table 13)	Comments
600	600	Short 2-3[1]	Short 2-3[1]	Requires a SKU with a 600 MHz IA-32 core frequency
1066	1066	Short 2-3[1]	Short 2-3[1]	
1200	1066	Short 1-2-3[2]	Short 2-3[1]	Allows 1200 MHz IA-32 core to run at 1066 MHz
1200	1200	Short 2-3[1]	Short 2-3[1]	

1. "Short 2-3" means to use a 2 pin jumper to shunt pins 2-3 together
2. "Short 1-2-3" means to use a jumper to shunt pins 1-2-3 together

4.3 SMBus Address

Table 11 shows the SMBus device addresses on the Intel® EP80579 Development Board.

Table 11. SMBus Connectivity

Devices	Address	Power Rail
Primary from Intel® EP80579		
SIO	0x5C	3.3V
EP80579 Processor - IICH slave device	0x44	3.3V
SMBus A		
EP80579 Processor - IMCH slave device	0x60	3.3V
DB800	0xDC	3.3V
CK410	0xD2	3.3V
ITP	Master	3.3V
SMBus B		
DIMM 0	0xA4	3.3V
DIMM 1	0xA6	3.3V
SMBus C		
HSS Mezzanine 0	Determined by card	3.3V
HSS Mezzanine 1	Determined by card	3.3V
HSS Mezzanine 2	Determined by card	3.3V

4.4 System LEDs

The Intel® EP80579 Development Board provides LEDs as indicators for system signals and voltages, as provided in Table 12. Figure 11 shows the location of the LEDs. System LEDs are lit when the signal or voltage is active.

Figure 11. Layout of LEDs

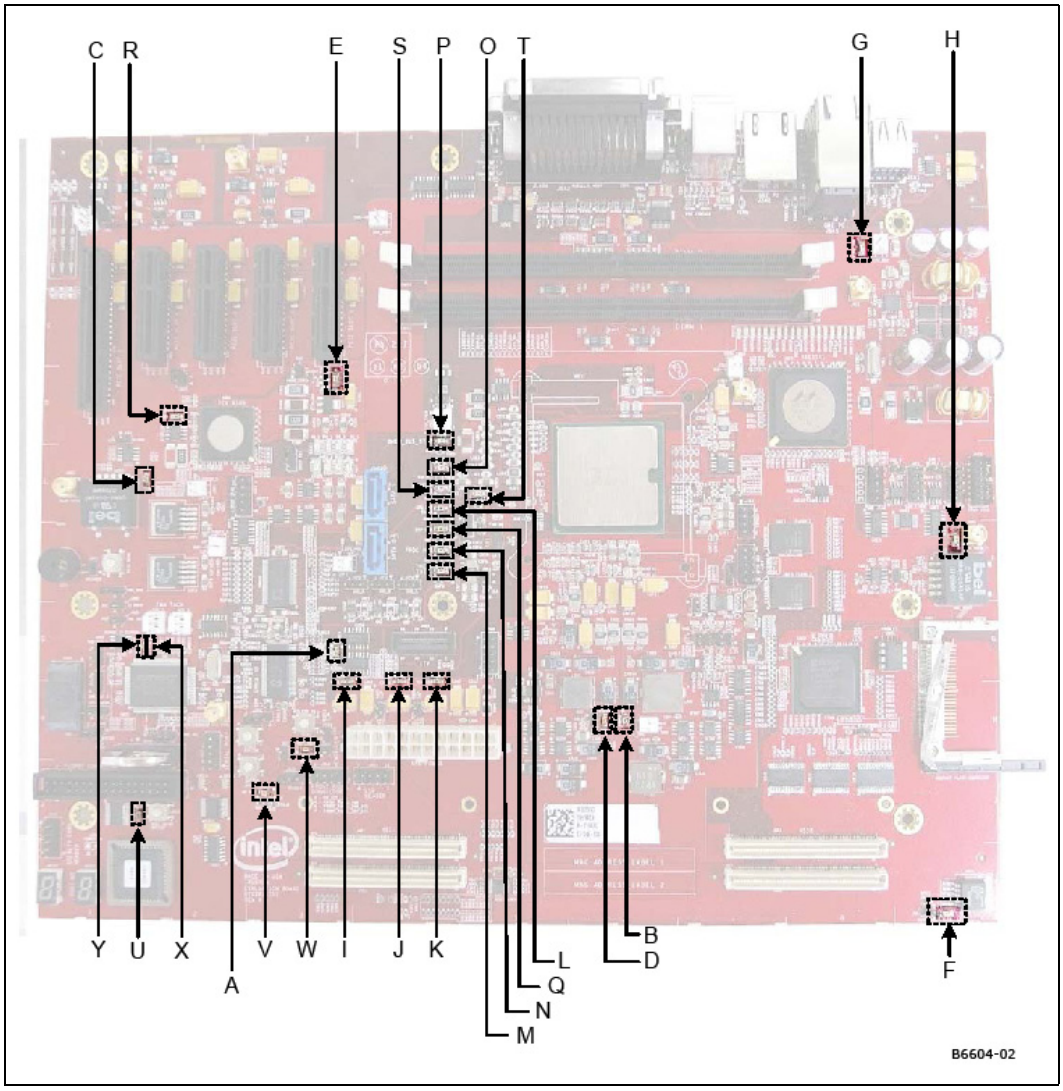


Table 12. Signal and Voltage LED Indicators (Sheet 1 of 2)

Call-out	Signal	Label Name	LED Color	Description
A	PWRGD	DS3G1	Green	Power-good LED
B	VCC_CPU	DS6H2	Green	VCC for processor LED
C	1.0V	DS2E1	Green	1.0V LED
D	1.2V	DS6H1	Green	Front Panel Power LED
E	1.5V	DS3D1	Green	1.5V Auxiliary LED

Table 12. Signal and Voltage LED Indicators (Sheet 2 of 2)

Call-out	Signal	Label Name	LED Color	Description
F	1.8V	DS9K1	Green	1.8V LED
G	1.8V DDR	DS8B1	Green	1.8V DDR LED
H	2.5V	DS9F1	Green	2.5V LED
I	3.3V	CR3G1	Green	3.3V LED
J	5.0V	CR4G1	Green	5V LED
K	5.0V Standby	CR4G2	Green	5V standby LED
L	CPU_RESET#	DS4E3	Red	Processor reset
M	CPU_THERMTRIP#	DS4F3	Red	Processor Thermtrip triggered
N	CPU_PROCHOT	DS4F2	Red	Processor PROC_HOT signal triggered
O	IMCH_CPUSLP	DS4E1	Red	Processor entering sleep state
P	IMCH_SUS_STAT	DS4D1	Red	Suspend status. System entering a low power state.
Q	IMCH_STPCLK	DS4F1	Red	Suspend Clock: output clock from RTC generator circuit to use as a refresh clock.
R	PEX_FATAL_ERR	DS2D1	Red	Error in PCIe switch
S	IERR	DS4E2	Red	Processor encountered an error. May require a reboot.
T	SLP_S3#	DS5E1	Green	Sleep S3
U	INIT33V	DS1J1	Red	Firmware Hub Init
V	SATA LED	DS3J1	Green	SATA hard drive activity status
W	WDT_Timer_Out	CR3H1	Green	Watchdog timer expired
X	SIO_LED_GRN	DS2G2	Green	General purpose LED for SIO
Y	SIO_LED_YLW	DS2G1	Yellow	General purpose LED for SIO

4.5 Fixed I/O Map and Interrupts

See the *Intel® EP80579 Integrated Processor Product Line Platform Design Guide* for information about fixed I/O maps and interrupts.

4.6 Jumper Block

Figure 12 shows the location of the jumper blocks. Table 13 lists the settings and usage of the jumpers. Review Figure 12 and Table 13 before changing the default jumper settings.

Warning: Do not move jumpers when the power is on. Always turn off the power and unplug the power cord from the power supply before changing a jumper setting. Otherwise, the Intel® EP80579 Integrated Processor may be damaged.

Figure 12. Jumper Block Locations

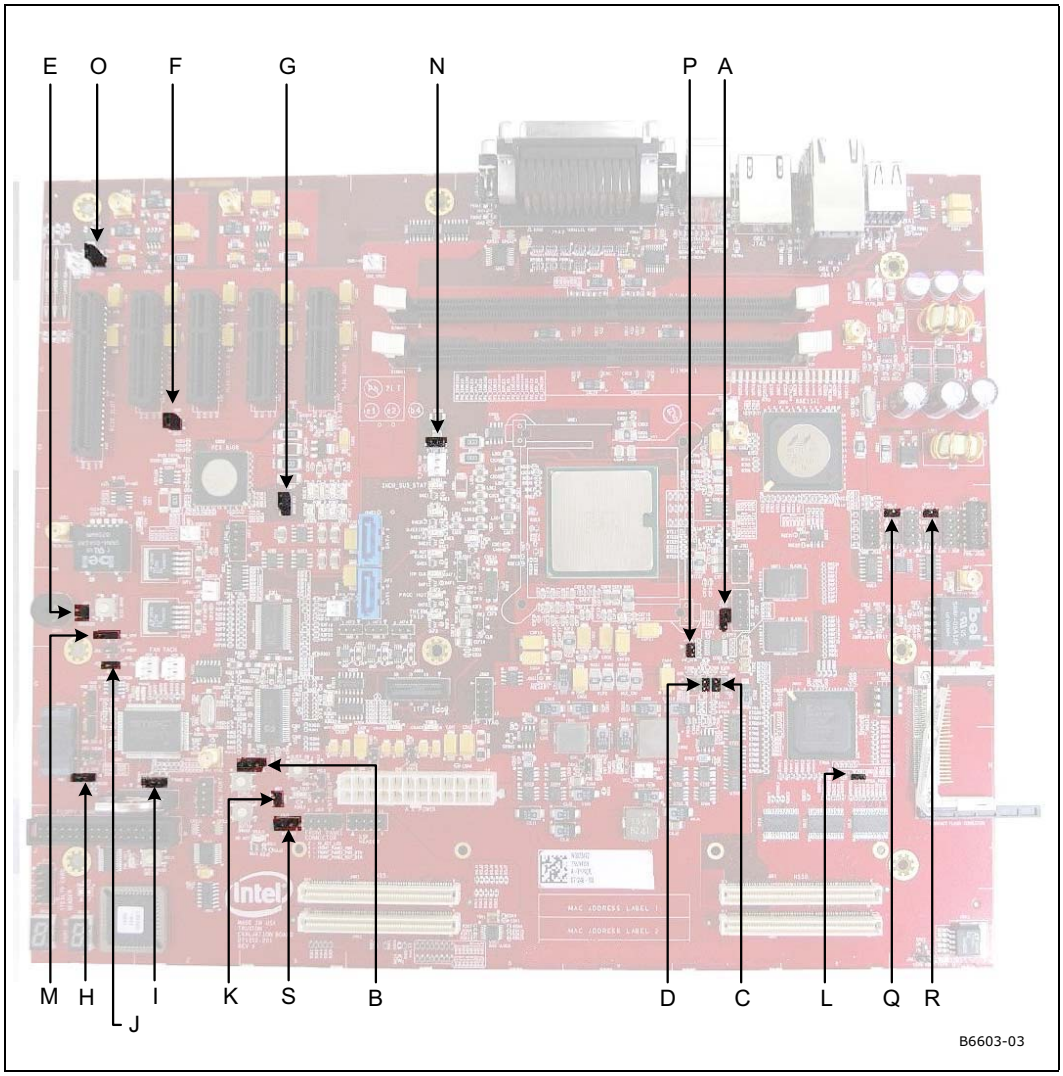


Table 13. Jumper Block Descriptions (Sheet 1 of 3)

Location	Jumper Name	Ref Des	Description	Default Position
A	V_SEL	J7F2	SKU and Voltage Selection: See Table 10	2-3
B	BSEL	J3H1, J7G6	FSB frequency selection: See Table 10	2-3
C	1.0V Override (V_SEL)	J7G4	**Intel Internal Test Only** 1.0V override selection: Short = Force IA core voltage to 1.0V ***Note:*** R3U6 0 ohms resistor needs to be removed. Open = IA core voltage is determined based on V_SEL signal and BSEL	Open

Table 13. Jumper Block Descriptions (Sheet 2 of 3)

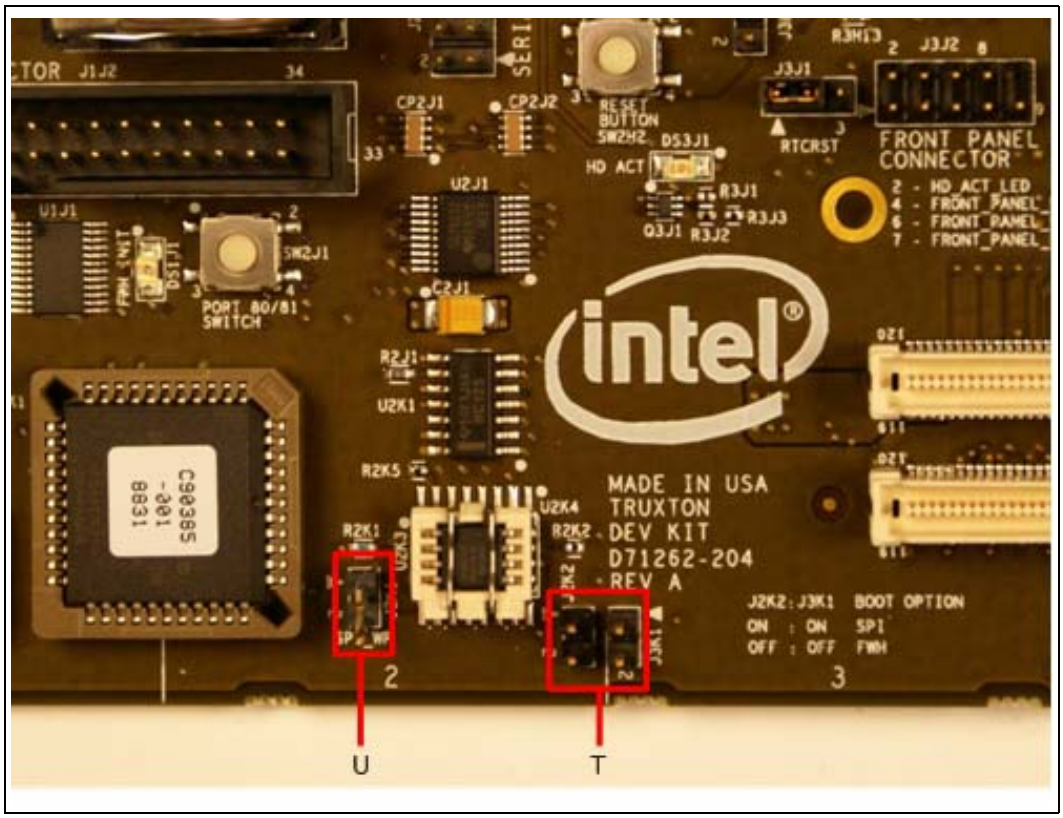
Location	Jumper Name	Ref Des	Description	Default Position
D	1.3V Override (V_SEL)	J7G3	**Intel Internal Test Only** 1.3V override selection: Short = Force IA core voltage to 1.3V ***Note:*** R3U7 0 ohms resistor needs to be removed. Open = IA core voltage is determined based on V_SEL signal and BSEL	Open
E	No Reboot Strap	J1F1	Short = No reboot on second time-out of TCO timer Open = Reboot on second time-out of TCO timer	Open
F	PLX PCIe Switch EEPROM Present	J2D1	Manually disable PLX PCIe switch EEPROM: Short = EEPROM is present Open = EEPROM is not present	Short
G	PLX PCIe Switch Reset	J3E1	Manually reset PLX PCI Express switch: 1-2 = Normal 2-3 = Resetting PLX PCI Express Switch	1-2
H	Quad GbE PHY Reset	J1H2	Manually reset Quad GbE PHY: Short = Normal Open = Resetting Quad GbE PHY	Short
I	SIO Disable	J2H2	Manually disable SIO: Short = Normal Open = Disabling SIO	Short
J	Top Block Lock	J1G1	Locking FWH Top Block: Short = Locking Top Block Open = Top Block is not locked	Open
K	Watchdog Timer Reset	J3H3	Enable to generate reset when WDT expires: Short= Generates WDT reset Open = No WDT reset	Open
L	FPGA Program	J8H1	Enable to program FPGA: Short = Programs FPGA Open = Normal	Open
M	FWH Program	J1F2	Enable to program and erase FWH: Short = Allow normal program or erase of FWH Open = No program or erase allowed	Open
N	CPU FAN Speed Override	J4D1	Processor speed override: Short = Full speed Open = SIO PWM speed control	Open
O	Aux FAN Speed Override	J1B1	Aux fan speed override: Short = Full speed Open = SIO PWM speed control	Open
P	Front Panel Sleep Signal	J7G1	GPIO 30 is configured to external sleep signal jumper: Short = Manually generate sleep signal Open = Normal	Open
Q	CAN0 Termination	J9E1	CAN Bus 0 Termination: Short = Terminate CAN Bus 0 Open = CAN Bus 0 not terminated	Open
R	CAN1 Termination	J9E2	CAN Bus 1 Termination: Short = Terminate CAN Bus 1 Open = CAN Bus 1 not terminated	Open

Table 13. Jumper Block Descriptions (Sheet 3 of 3)

Location	Jumper Name	Ref Des	Description	Default Position
S	CMOS Clear Section 5.11	J3J1	Reset CMOS: 1-2 = Normal 2-3 = Clear CMOS	1-2
T	Boot Option for SPI Boot or FWH Boot Selection	J2K2, J3K1	Boot Option Selection: Figure 13 J2K2, J3K1 = GPIO17, GPIO33 Open, Open -> Boot From FWH (default) Open, Short -> RESERVED Short, Open -> RESERVED Short, Short -> Boot From SPI Flash	1-2
U	SPI Flash Write Protection	J2K1	SPI Flash WP: Figure 13 Short = Write Protected Open = Normal (default)	1-2

Figure 13 shows the SPI and FWH boot selection option.

Figure 13. SPI and FWH Boot Option Jumpers



4.7 Header Blocks

Figure 14 and Table 14 describe the location of the headers.

Warning: Before applying power to the Intel® EP80579 Integrated Processor, ensure that the headers are connected correctly. Improper configuration of the Intel® EP80579 Development Board headers may result in board damage.

Figure 14. Header Locations

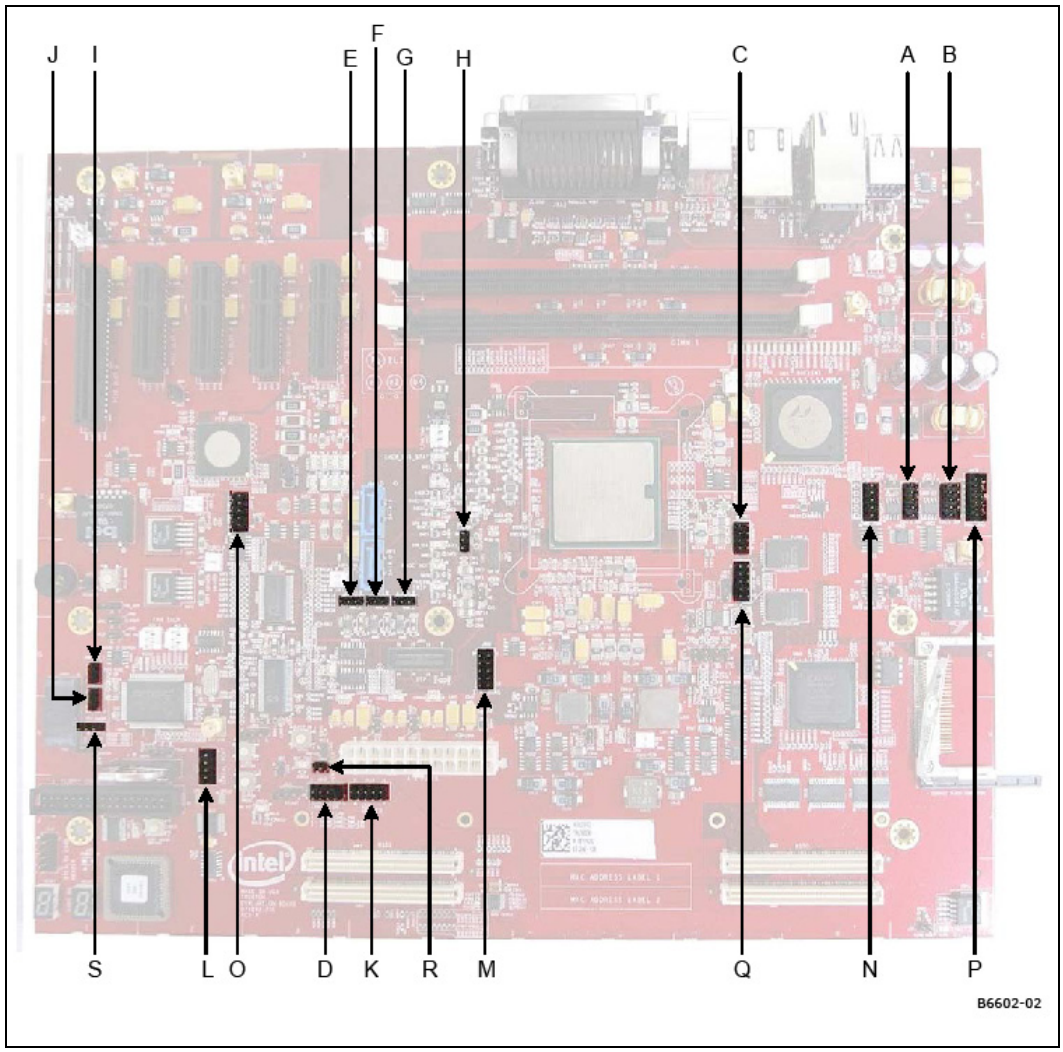


Table 14. Header Block Descriptions (Sheet 1 of 2)

Location	Header Name	Ref Des	Pinout Signal Description
A	CAN0	J9E3	Table 21
B	CAN1	J9E4	Table 21
C	IEEE 1588-2008 Hardware-assist	J7E1	Table 22
D	Front panel	J3J2	Table 23
E	SMBUS_A	J4F2	Table 24

Table 14. Header Block Descriptions (Sheet 2 of 2)

Location	Header Name	Ref Des	Pinout Signal Description
F	SMBUS_B	J4F3	Table 24
G	SMBUS_C	J4F4	Table 24
H	VSBY_SMB	J5E1	Table 24
I	SIO1 SMBUS	J1G2	Table 24, connected to Board ID EEPROM
J	SIO2 SMBUS	J1G3	Table 24, connected to PCIe slot
K	SSP	J4J1	Table 25
L	COM3 (Tertiary SIO UART)	J2J1	Table 26
M	Intel® EP80579 JTAG	J5G2	Table 27
N	88E1141 JTAG	J8E1	Table 27
O	PEX 8058 JTAG	J3E2	Table 27
P	FPGA JTAG	J9E5	Table 28
Q	GPIO header	J7F1	Table 29
R	Intruder	J3H4	Optional intruder switch header: 1: MICH_INTRUDER 2: GND
S	CPU thermal diode	J1H1	Access to processor thermal diode: 1: CPU_THERM_DC 2: CPU_THERM_DA 3: GND

4.8 Connector/Header Pinout Information

4.8.1 ITP-XDP Connector Pinout

The Intel® EP80579 Development Board provides a 60-pin ITP-XDP connector for system debugging purposes. For ITP-XDP pinout, refer to Table 15.

Table 15. ITP-XDP Connector (Sheet 1 of 2)

Pin	Name	Pin	Name
1	GND	2	GND
3	PREQ_N	4	NOA_CLK_0
5	PRDY_N	6	NOA_CLK_1
7	GND	8	GND
9	BPM_3 / NOA_0	10	NOA_8
11	BPM_2_N / NOA_1	12	NOA_9
13	GND	14	GND
15	BPM_1_N / NOA_2	16	NOA_10
17	BPM_0_N / NOA_3	18	NOA_11
19	GND	20	GND
21	NC	22	NC
23	NC	24	NC
25	GND	26	GND
27	NOA_4	28	NOA_12

Table 15. ITP-XDP Connector (Sheet 2 of 2)

Pin	Name	Pin	Name
29	NOA_5	30	NOA_13
31	GND	32	GND
33	NOA_6	34	NOA_14
35	NOA_7	36	NOA_15
37	GND	38	GND
39	PWRGOOD	40	BCLK_P
41	DFXTEST	42	BCLK_N
43	1.8V	44	1.8V
45	PCICLK	46	RESET_N
47	PCICLK REF	48	DBR_N
49	GND	50	GND
51	SMBUS_DATA	52	TDO
53	SMBUS_CLK	54	TRST_N
55	NC	56	TDI
57	TCK	58	TMS
59	GND	60	XDP_PRSNT_N

4.8.2 ATX12V Power Connector Pinout

The Intel® EP80579 Development Board comes with a 2x12 main power connector. This connector is compatible with a 2x10 power connector. The board supports the use of ATX12V power supplies with either 2x10 or 2x12 main power cables. Table 16 shows the pinout of the main power supply.

Table 16. Main ATX Power Supply Connector

Pin	Description	Pin	Description
1	+3.3 V	13	+3.3 V
2	+3.3 V	14	-12 V
3	GND	15	GND
4	+5 V	16	PS-ON#
5	GND	17	GND
6	+5 V	18	GND
7	GND	19	GND
8	PWROK	20	NC
9	+5 V (Standby)	21	+5 V
10	+12 V	22	+5 V
11	+12 V*	23	+5 V*
12	+3 V*	24	GND*

* The pin is not connected when using a 2x12 power supply cable.

4.8.3 LEB CompactFlash* Connector Pinout

The Intel® EP80579 Development Board utilizes the Local Expansion Bus interface that is connected to the CompactFlash connector and runs in True IDE mode. For more information, refer to *CF+ and CompactFlash Specification Revision 4.0*, *5/24/06* for the standard True IDE mode pinout.

4.8.4 HSS Mezzanine Connectors Pinout

The Intel® EP80579 Development Board implements three sets of mezzanine connectors dedicated to HSS devices. There are two primary cards intended for use with the Intel® EP80579 Development Board, an Intel® EPAVM80579 Analog Voice Mezzanine Card (4-port analog voice card) and a Intel® EPTEM80579 Quad T1/E1 Mezzanine Card (quad T1/E1 card). The two cards are different with respect to the offset of the mezzanine connectors: one is offset left, and the other is offset right.

Each mezzanine card has two 120-pin connectors associated with it. The first connector is referred to as the standard connector and the second connector is referred to as the expansion connector. The standard connector includes primary and secondary HSS interfaces, expansion bus, GPIOs and interrupt. The expansion connectors include SSP signals, extra GPIOs and 8 expansion bus chip select signals.

Table 17 lists the primary and secondary HSS port numbers in each HSS mezzanine slot.

Table 17. HSS to Mezzanine Organization

HSS Mezzanine Number	Primary HSS I/F	Secondary HSS I/F	Natively Supported Card
0	HSS0	HSS1	E1/T1
1	HSS1	HSS0	Dual footprint
2	HSS2		E1/T1

The Intel® EP80579 Development Board utilizes three GPIO pins to provide interrupts on the HSS mezzanine connectors. Table 18 provides the GPIO pins that are used as HSS interrupts.

Table 18. HSS Interrupt GPIO Pin Names

Pin Name	HSS Interrupt Number
GP16_IRQ24	HSS0_INT_OUT
GP17_IRQ25	HSS1_INT_OUT
GP18_IRQ37	HSS2_INT_OUT

Table 19 shows the pinout of the standard mezzanine connector. Table 20 provides the pinout of the expansion mezzanine connector.

Table 19. Standard Mezzanine Connector Pinout (Sheet 1 of 3)

Pin	Name	Pin	Name
1	NC	2	NC
3	NC	4	NC
5	EX_DATA_1	6	EX_DATA_0
7	EX_DATA_3	8	EX_DATA_2

Table 19. Standard Mezzanine Connector Pinout (Sheet 2 of 3)

Pin	Name	Pin	Name
9	HSSn[1]_GPIO_0	10	HSSn[1]_GPIO_1
11	EX_DATA_5	12	EX_DATA_4
13	EX_DATA_7	13	EX_DATA_6
15	GND	16	GND
17	EX_DATA_9	18	EX_DATA_8
19	EX_DATA_11	20	EX_DATA_10
21	NC	22	NC
23	EX_DATA_13	24	EX_DATA_14
25	EX_DATA_15	26	EX_DATA_16
27	GND	28	GND
29	EX_ADDR_1	30	EX_ADDR_0
31	EX_ADDR_3	32	EX_ADDR_2
33	EX_ADDR_5	34	EX_ADDR_4
35	EX_ADDR_7	36	EX_ADDR_6
37	GND	38	GND
39	EX_ADDR_9	40	EX_ADDR_8
41	EX_ADDR_11	42	EX_ADDR_10
43	EX_ADDR_13	44	EX_ADDR_12
45	EX_ADDR_15	46	EX_ADDR_14
47	GND	48	GND
49	EX_ADDR_17	50	EX_ADDR_16
51	EX_ADDR_19	52	EX_ADDR_18
53	EX_ADDR_21	54	EX_ADDR_20
55	EX_ADDR_23	56	EX_ADDR_22
57	GND	58	GND
59	EX_CLK_HSSn[1]	60	EX_RD_N
61	GND	62	EX_WR_N
63	EX_ALE	64	EX_RDY_N
65	EX_IOWAIT_N	66	HSSn[1]_INT_OUT
67	EX_CS_N_i[4]	68	3.3V
69	NC	70	3.3V
71	5V	72	3.3V
73	5V	74	3.3V
75	5V	76	3.3V
77	5V	78	3.3V
79	5V	80	3.3V
81	5V	82	3.3V
83	HSSn[1]_GPIO_2	84	HSSn[1]_GPIO_3
85	GND	86	GND
87	HSS_JTAG_TCK	88	HSSn[1]_GPIO_4

Table 19. Standard Mezzanine Connector Pinout (Sheet 3 of 3)

Pin	Name	Pin	Name
89	HSS_JTAG_TDI	90	RST_N
91	HSS_JTAG_TDO	92	HSS_TXFRAME_y[3]
93	HSS_JTAG_TMS	94	HSS_TXCLK_y[3]
95	GND	96	HSS_TXDATA_y[3]
97	HSS_TXDATA_x[2]	98	GND
99	HSS_TXFRAME_x[2]	100	HSS_RXDATA_x[2]
101	NC	102	HSS_RXFRAME_x[2]
103	HSS_TXCLK_x[2]	104	NC
105	GND	106	HSS_RXCLK_x[2]
107	NC	108	GND
109	HSS_RXCLK_y[3]	110	NC
111	HSS_RXFRAME_y[3]	112	HSS_RXDATA_y[3]
113	12V	114	2.5V
115	12V	116	2.5V
117	12V	118	2.5V
119	12V	120	2.5V

1. n is the HSS mezzanine slot number. All HSSn_GPIO_[2:0] signals are routed to FPGA.
2. x is the primary HSS port signal.
3. y is the secondary HSS port signal.
4. i is 4, 5, and 6 for mezzanine 0, 1 and 2 respectively.

Table 20. Expansion Mezzanine Connector (Sheet 1 of 3)

Pin	Name	Pin	Name
1	1.8V	2	1.8V
3	GND	4	GND
5	HSSn[1]_GPIO_0	6	HSSn[1]_GPIO_1
7	HSSn[1]_GPIO_2	8	HSSn[1]_GPIO_3
9	GND	10	GND
11	HSSn[1]_GPIO_4	12	HSSn[1]_GPIO_5
13	HSSn[1]_GPIO_6	13	HSSn[1]_GPIO_7
15	GND	16	GND
17	HSSn[1]_GPIO_8	18	HSSn[1]_GPIO_9
19	HSSn[1]_GPIO_10	20	HSSn[1]_GPIO_11
21	GND	22	GND
23	HSSn[1]_GPIO_12	24	HSSn[1]_GPIO_13
25	HSSn[1]_GPIO_14	26	HSSn[1]_GPIO_15
27	GND	28	GND
29	EX_ADDR_24	30	SSPS_CLK
31	SSPS_FRM	32	SSPS_TXD
33	SSPS_RXD	34	SSPC_EXTCLK
35	5V	36	5V

Table 20. Expansion Mezzanine Connector (Sheet 2 of 3)

Pin	Name	Pin	Name
37	EX_RDY_N_3	38	NC
39	EX_RDY_N_1	40	EX_RDY_N_2
41	NC	42	EX_RDY_N_0
43	EX_CLK_HSSn[1]	44	NC
45	NC	46	NC
47	EX_BE_3_N	48	EX_BE_2_N
49	EX_BE_1_N	50	EX_BE_0_N
51	EX_BURST	52	NC
53	NC	54	NC
55	EX_CS_N_7[2]	56	EX_CS_N_6[2]
57	NC	58	EX_CS_N_4[2]
59	EX_CS_N_3[2]	60	EX_CS_N_2[2]
61	EX_CS_N_1[2]	62	EX_CS_N_0[2]
63	NC	64	NC
65	CLK_32_IN	66	HPI_GPIO_34[2]
67	NC	68	NC
69	CLK_32_IN	70	EX_REQ_GNT_N[2]
71	EX_GNT_REQ_N[2]	72	NC
73	NC	74	EX_WFTXFER[2]
75	NC	76	NC
77	EX_WAIT_N[2]	78	EX_SLAVE_CS_N[2]
79	EX_BURST[2]	80	NC
81	3.3V	82	3.3V
83	3.3V	84	3.3V
85	GND	86	GND
87	HSSn[1]_INT_OUT	88	NC
89	NC	90	NC
91	GND	92	GND
93	NC	94	GPIO_5
95	GPIO_6	96	GPIO_7
97	GND	98	GND
99	GPIO_8	100	GPIO_9
101	GPIO_10	102	GPIO_11
103	GND	104	GND
105	GPIO_12	106	GPIO_13
107	GPIO_14	108	GPIO_15
109	GND	110	GND
111	GND	112	3.3V
113	3.3V	114	3.3V
115	3.3V	116	3.3V

Table 20. Expansion Mezzanine Connector (Sheet 3 of 3)

Pin	Name	Pin	Name
117	3.3V	118	3.3V
119	MEZZ_SMBDAT	120	MEZZ_SMBCLK
1. n = 0 for mezzanine 1. For mezzanines 0 and 2, these pins are not connected. 2. Only available for mezzanine 1. These pins are not connected for mezzanines 0 and 2.			

4.8.5 CAN Header Pinout

Both Intel® EP80579 Integrated Processor Controller Area Network (CAN) interface pins connect to two individual CAN transceivers. After conditioning by the transceiver, the CAN signals will go to two separate 10-pin headers. For the CAN connector pinout, see Table 21.

Table 21. CAN Header Pinout

Pin	Signal Name	Pin	Signal Name
1	NC	2	CAN GND
3	CAN Low	4	CAN High
5	CAN GND	6	NC
4	NC	8	NC
5	NC	10	Key (no pin)

4.8.6 IEEE 1588-2008 Hardware-Assist Header Pinout

IEEE 1588-2008 Hardware-assist is used to achieve ethernet and CAN time synchronization. On the Intel® EP80579 Development Board, the IEEE 1588-2008 Hardware-assist control I/O signals are connected to a 2x4 header. Table 22 provides the IEEE 1588-2008 Hardware-assist header pinout.

Table 22. IEEE 1588-2008 Hardware-Assist Signal Header Pinout

Pin	Signal	Pin#	Signal
1	1588_TESTMODE_DATA	2	1588_SPS
3	ASMSSIG	4	AMMSSIG
5	1588_RX_SNAP	6	1588_TX_SNAP
7	GND	8	GND

4.8.7 Front Panel Header

The Intel® EP80579 Development Board has a 10-pin keyed header for the front panel connector. This section describes the functions of the front panel header. Table 23 shows the pinout.

Table 23. Front Panel Header Pinout

Pin	Signal	Description
Hard Drive Activity LED		
1	HD_ACT_LED_P	Hard drive activity LED +
2	HD_ACT_LED_N	Hard drive activity LED -
Power LED		
3	FP_PWR_LED_P	Power LED +
4	FP_PWR_LED_N	Power LED -
Power On/Off Switch		
5	GND	Ground
6	FP_PWR_BTN_N	Power on/off switch
Reset Switch		
7	FP_Reset_BTN_N	Power reset switch
8	GND	Ground
Others		
9	GND	Ground
10	Key (no pin)	Key (unconnected)

4.8.8 SMBus Header

The Intel® EP80579 Development Board provides four external headers to support access to the SMBus. For the SMBus header pinout, refer to Table 24.

Table 24. SMBus Header Pinout

Pin	Signal
1	Data
2	Ground
3	Clock

4.8.9 SSP Header

The Intel® EP80579 Development Board provides a 2x5 header to access the processor's SSP I/O pins. Table 25 provides the pinout of the SSP header.

Table 25. SSP Header Pinout

Pin	Signal	Pin	Signal
1	NC	2	SSP_SFRM
3	SSP_TXD	4	GND
5	SSP_RXD	6	GND
7	SSP_CLK	8	GND
9	SSP_EXTCLK	10	+3V3

4.8.10 SIO Tertiary (Third) UART Header

The Intel® EP80579 Development Board utilizes the SIO to provide a third UART and RS-232 connectivity. The UART is connected to a 2x5 header. The pinout is provided in Table 26.

Note: SIO Tertiary UART can utilize the CAN cable interface.

Table 26. Tertiary UART Pinout

Pin	Signal	Pin	Signal
1	DCD	2	DSR
3	RXD	4	RTS
5	TXD	6	CTS
7	DTR	8	RI
9	GND	10	NC

4.8.11 JTAG Access Headers

The Intel® EP80579 Development Board provides JTAG access headers for debug purposes. Table 27 includes the Intel® EP80579, PCI Express switch, and Quad Ethernet PHY JTAG access header pinout. Table 28 lists the FPGA JTAG access header pinout.

Table 27. Intel® EP80579, PEX8508 and 88E1141JTAG Header Pinout

Pin	Signal	Pin	Signal
1	TRST_N	2	GND
3	TDI	4	GND
5	TDO	6	GND
7	TMS	8	GND
9	TCK	10	GND

Table 28. FPGA JTAG Header Pinout

Pin	Signal	Pin	Signal
1	GND	2	3.3V
3	GND	4	TMS
5	GND	6	TCK
7	GND	8	TDO
9	GND	10	TDI
11	GND	12	NC
13	GND	14	NC

Note: The FPGA JTAG header is not a standard header. The manufacturer and part number are Molex and 87832-142077.

4.8.12 GPIO Header

The Intel® EP80579 Development Board provides a GPIO header that can access the nine GPIO pins listed in Table 29.

Table 29. GPIO Header Pinout

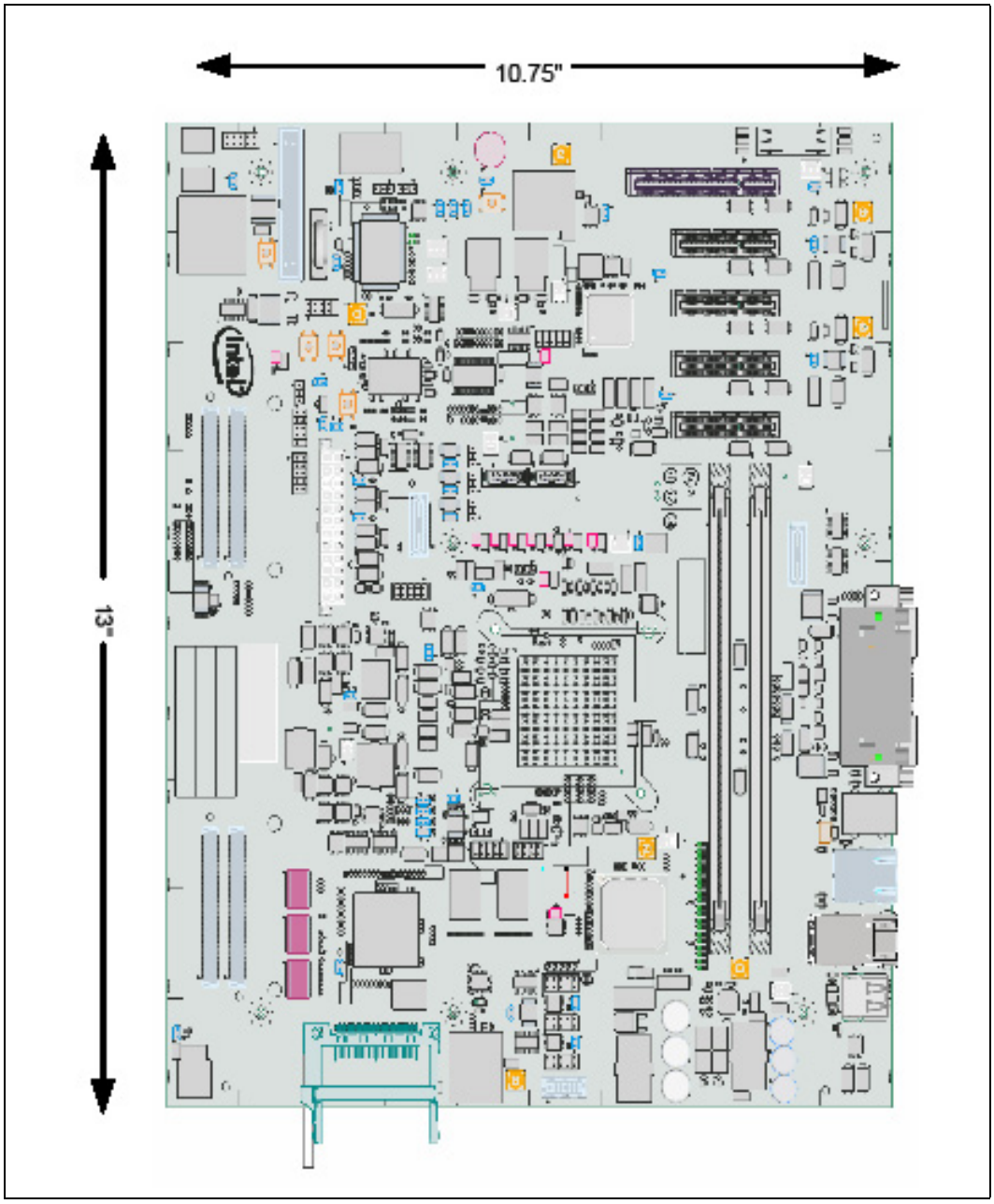
Pin	Signal	Pin	Signal
1	GP25_IRQ38	2	GP4_PIRQG_N
3	GP31_IRQ31*	4	GP3_PIRQF_N
5	GP28_IRQ30*	6	GP2_PIRQE_N
7	GP34_IRQ34*	8	GPIO<1>
9	GPIO<0>	10	GND
* These pins are connected to FPGA /HSS.			

4.9 Mechanical Considerations

4.9.1 Form Factor

The Intel® EP80579 Development Board is designed to accommodate three mezzanine slots. A full sized Intel® EP80579 Development Board is 13" wide by 10.75" deep (330.2mm X 273.05mm). Locations of the I/O connectors and mounting holes are in compliance with the ATX specification. Figure 15 illustrates the mechanical form factor of the Intel® EP80579 Development Board.

Figure 15. Form Factor of Intel® EP80579 Development Board



4.10 Electrical Considerations

4.10.1 DC Loading

Table 30 lists the DC loading characteristics of the Intel® EP80579 Development Board. This data is based on DC analysis of all the active components within the Intel® EP80579 Development Board that impact its power delivery subsystems. The analysis does not include PCI Express add-in cards.

Minimum load values assume a light load placed on the Intel® EP80579 Development Board that is similar to an environment with basic OS (operating system), idled at the platform, and no applications running.

Maximum load values in Table 30 indicate the Intel® EP80579 Development Board runs with four add-on network cards via PCIe and onboard network ports all transferring files. Also Burn in program was running with multiple instances of memory test running.

The values are not based on specific SKU or memory configurations, but are based on the minimum and maximum current draw possible from power delivery subsystem to processor, memory and external interfaces.

See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for the overall system power requirements of the add-in cards. The selection of power supply at the system level is dependent on the system's usage model and not necessarily tied to a particular SKU of the EP80579 Processor.

Table 30. DC Loading Characteristics Mode

Voltage Rails		+3.3 V	+5 V	+12 V	-12 V	+5 VSB
Minimum Loading	DC Current (Amps)	2.98	3.72	1.23	0	.75
	Power (Watts)	10.1	19.4	14.6	0	3.7
Maximum Loading	DC Current (Amps)	5.31	5.46	1.26	.03	1.15
	Power (Watts)	17.8	28.4	15.3	0.5	5.8

4.10.2 PCI Express Add-in Connector Considerations

The Intel® EP80579 Development Board is designed to provide 2 amps (average current drain) to each add-in connector, for both the +3.3V and +12V supplies. The maximum current drawn by the add-in connector for a fully loaded board (all five PCIe connectors filled) must not exceed 10A for both the +3.3V and +12V supplies.

4.10.3 Fan Connector Current Capability

Table 31 shows the current capability of the Intel® EP80579 Development Board fan connectors.

Table 31. Fan Connector Current Capability

Name	Maximum Available Current /A
CPU Fan	3.0
Aux Fan	3.0
Aux0 Fan	3.0
Aux1 Fan	3.0

4.11 Thermal Considerations

The Intel® EP80579 Development Board is included with a heatsink thermal solution that is to be installed on the EP80579 Processor. This thermal solution has been tested in an open air environment at room temperature and is sufficient for evaluation purposes. The THERMTRIP# and PROCHOT# signals are connected to LEDs on the Intel® EP80579 Development Board. Pre-boot Firmware on the Intel® EP80579 Development Board will enable thermal throttling at 50% duty cycle when PROCHOT# is activated, and the processor will shut down automatically if THERMTRIP# is activated.

Warning: There is NO thermal protection circuitry implemented on the Intel® EP80579 Development Board. The system designer must ensure that adequate thermal management or thermal protection circuitry are provided for any customer-derived designs.

§ §

5.0 Pre-boot Firmware

5.1 Introduction

The Pre-boot Firmware is executed when the system is powered up or reset. It initializes and configures system memory, devices and buses/interfaces.

The Pre-boot Firmware is based on the AMI Aptio* 4.5 core and compliant to EFI v1.1. The Pre-boot Firmware is stored in the Firmware Hub (FWH) or SPI (Serial Peripheral Interface) Flash; the FWH or SPI Flash can be updated using a flash utility tool that is provided by Intel or by using a floppy drive connected to the floppy header.

The Pre-boot Firmware setup menu can be used to view and modify the system settings for the Intel® EP80579 Development Board. The setup menu is accessed by pressing the <Del> key during Pre-boot Firmware boot up (before the operating system boot begins). The setup menu bar is shown in Table 32.

5.2 Pre-boot Firmware Boot Flow

After a hardware reset of the Intel® EP80579 Integrated Processor, and once the IA CPU has executed the reset micro-code, the IA CPU restores to the reset vector (0xFFFF_FFF0) and starts fetching from the FWH or SPI flash device. The Pre-boot Firmware starts executing from the reset vector regardless of whether wake is from S3, S4, or S5. To determine if it is an S3 resume, the firmware checks the SUS_TYP field in the power management controller. If it is not S3, then normal boot occurs. If it is S3, then the firmware also checks the power failure bits (PWRBTNOR_STS, PWR_FLR, PWROK_FLR). If these are set to 1, then the memory contents cannot be relied on and a normal boot is followed. If it is an S3 resume and the power failure bits are not set, then the S3 boot path is followed. The normal boot path is used for cold reset and for S4/S5 resume. From a firmware perspective, there is no difference between S4 and S5. The following steps describe the boot sequence after reset before hand over to the OS.

5.3 Pre-boot Firmware Features

5.3.1 Pre-boot Firmware Setup Menu

Table 32 shows the Pre-boot Firmware setup main menu and provides a brief description of each menu option. Table 33 provides the function keys that can be used when navigating and selecting options from Pre-boot Firmware menus.

Table 32. Pre-boot Firmware Setup Main Menu

Main	Advanced	Chipset	Security	Boot	Exit
Displays processor and memory configuration Setup for CMOS system date and time	Configures advanced features and settings	Configures different major components	Setup passwords and security features	Selects boot options and configurations	Saves or discards changes to setup program options

Table 33. Pre-boot Firmware Setup Program Function Keys

Function Key	Description
< or >	Moves cursor left or right in the main menu
^ or v	Moves cursor up or down to select sub-menu items
Enter	Executes command or selects the submenu
F7	Discard changes
F8	Load the fail-safe default
F9	Load the optimal default configuration value for the current menu
F10	Save the current configuration and exit the setup menu
ESC	Exit the setup menu

5.4 Serial Console Redirection

The Pre-boot Firmware supports redirection of both video and keyboard via a serial port. When console redirection is enabled, the remote console terminal sends keystrokes to the Intel® EP80579 Development Board Pre-boot Firmware and the Pre-boot Firmware redirects the video to the console terminal.

As an option, the Intel® EP80579 Development Board can be operated without keyboard or video and can run entirely via the remote serial console. This includes accessing the Pre-boot Firmware setup menu.

Console redirection ends when operating system boot up begins. After boot up begins, the operating system is responsible for continuing the redirection.

Note: Pre-boot Firmware console redirection is text only. Graphical data, such as logos, are not redirected.

5.4.1 Default Settings

Table 34 shows the default settings of the serial console redirection.

Table 34. Serial Console Redirection Default Settings

Parameters	Default
Port Number	COM 1
Baud Rate	115200
Data Bits	8
Parity	None
Stop bits	1
Flow Control	None

5.5 PXE Boot Support

The Pre-boot Firmware supports the EFI PXE implementation for on-board gigabit ethernet on Gigabit Ethernet Port 0. See Chapter 15 of the *Extensible Firmware Interface Reference Specification*, *v1.10*. The PXE driver will be included in the Pre-boot Firmware image to support this feature.

5.6 System Management BIOS (SMBIOS)

The Pre-boot Firmware provides support for the *System Management BIOS Reference Specification, v2.4* to create a standardized interface for manageable attributes that are expected to be supported by DMI-enabled computer systems. The Pre-boot Firmware provides this interface via data structures through which the system attributes are reported. Using SMBIOS, a system administrator can obtain the following information about server components:

- types
- capabilities
- operational status
- installation date
- other information

5.7 Legacy USB Support

The Pre-boot Firmware supports legacy USB during POST, which allows a user to enter and configure the Pre-boot Firmware setup via a USB keyboard.

5.8 Pre-boot Firmware Recovery and Updates

The Intel® EP80579 Development Board Pre-boot Firmware can be updated by using the Pre-boot Firmware programming tool software flash utility (flash programmer). The Pre-boot Firmware Update for the Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit *(Pre-boot Firmware)* and the Pre-boot Firmware Update Tool for the Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit *(AFUEFI Flash Utility)* are available to download.

To access the Pre-boot Firmware, Pre-boot Firmware Update Tool, and associated collateral, use the following steps:

1. In a Web browser, go to http://www.intel.com/go/soc.
2. For software, click the tab for “Tools & Software.”
3. For documentation, click the tab for “Technical Documents.”

If the Pre-boot Firmware is corrupted or any configuration setting is incorrect, causing the Pre-boot Firmware to not boot, the Pre-boot Firmware must be reflashed into the Intel® EP80579 Development Board firmware device (FWH or SPI Flash) using an external firmware device (FWH or SPI Flash) programmer, or the USB boot recovery method can be used.

Use the following procedure to perform a USB boot recovery:

1. Make sure the BIOS image on the USB key is the same version as the FWH or SPI Flash.
2. Rename the BIOS image on the USB key to AMIBOOT.ROM
3. Restart the board, and immediately and repeatedly press the Ctrl + Home keys until you hear a beep. The BIOS screen then loads with the Recovery option.
4. Select the option to “Proceed with Flash Update.”
5. After the flash update is complete, select Enter to restart the board.

5.8.1 Updating Pre-boot Firmware

To update the Pre-boot Firmware flash image on the Intel® EP80579 Development Board firmware device (FWH or SPI Flash), use the *Pre-boot Firmware Update Tool for the Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit (AMI’s Aptio* Flash Update Utility — AFUEFI)*.

Updated Pre-boot Firmware images for the Intel® EP80579 Development Board may be made available by Intel. The current Pre-boot Firmware image is available from the download center. The instructions in Section 5.8.2 guide you through the process of updating the firmware image. These instructions may also be used to re-flash the image to the firmware device (FWH or SPI Flash) if the Pre-boot Firmware image on the board becomes corrupt.

5.8.2 AMI’s Aptio* Flash Update Utility (AFUEFI)

Use the following instructions to update the Intel® EP80579 Development Board Pre-boot Firmware image using a USB memory stick and AMI’s Aptio* Flash Update Utility.

Necessary hardware:

- Intel® EP80579 Development Board
- Socketed Firmware Device (FWH or SPI Flash)
- USB memory stick

Necessary software:

- Pre-boot Firmware Update for the Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit *(Pre-boot Firmware Image)* (Image on the board must be equal or later than TRXTA053.ROM)
- Pre-boot Firmware Update Tool for the Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit (AMI’s Aptio* Flash Update Utility — AFUEFI)

Steps to update the flash image:

1. Load the AFUEFI utility onto the USB memory stick.
2. Load the Pre-boot Firmware image onto the USB memory stick. (Image on the board must be equal or later than TRXT053.ROM.)
3. Boot the Intel® EP80579 Development Board to the EFI shell. If needed, change the boot setting in the BIOS Setup Selection to boot from the EFI shell (If the boot option is not selectable, disconnect each bootable device from the Intel® EP80579 Development Board (hard drive, CDROM, etc.) to bypass booting to any of these devices).
4. Insert the USB memory stick into the USB port.
5. Once the system recognizes the USB memory stick (activity seen on the USB memory stick), several commands are available:
   — Type “map -r” to list all devices available.
   — Type “fs0:” to enter the USB device.
   — Type “ls” to list all files.
6. Execute the “fs0:” command and then start the AFUEFI utility:
   — Type “AFUEFI <*Pre-boot Firmware image name*> /X /P /B /N”. (The <Pre-boot Firmware image name> will be similar to TRXTA030.ROM.)
7. Reboot the Intel® EP80579 Development Board after the flash update has completed.

Use BIOS Setup to confirm that the image has been updated to the new flash image.

5.9 Boot Options

The user can choose to boot from any one of the following:

- SATA hard drive
- SATA DVD-ROM drive
- USB drive
- Floppy drive
- LAN card in PCIe connector
- PXE boot from internal GbE

The default order for the boot device precedence is as follows:

1. Floppy drive
2. Hard drive
3. CD-ROM drive
4. PXE network boot

5.9.1 Changing the Boot Device

Use the following procedure to change the boot device:

1. Press the <Del> key during POST to enter the Pre-boot Firmware setup menu.
2. Use the arrow keys to navigate to the <BOOT> menu.
3. Move the cursor to <Boot Device Priority>.
4. Select the desired booting sequence list.

Note: Follow the instructions on the right side of the Pre-boot Firmware screen to navigate and change Pre-boot Firmware settings.

5.9.2 Booting without Attached Devices

The Pre-boot Firmware has been designed so that after passing POST, the operating system loader is invoked even if the following devices are not present in the embedded application environment:

- Video controller card
- Keyboard
- Mouse

5.10 Security Features

The Pre-boot Firmware includes security features that restrict access to the Pre-boot Firmware setup menu and to define who is allowed to boot the Intel® EP80579 Development Board. A supervisor password and a user password can be set for the Pre-boot Firmware setup menu and for booting the Intel® EP80579 Development Board, with the following restrictions:

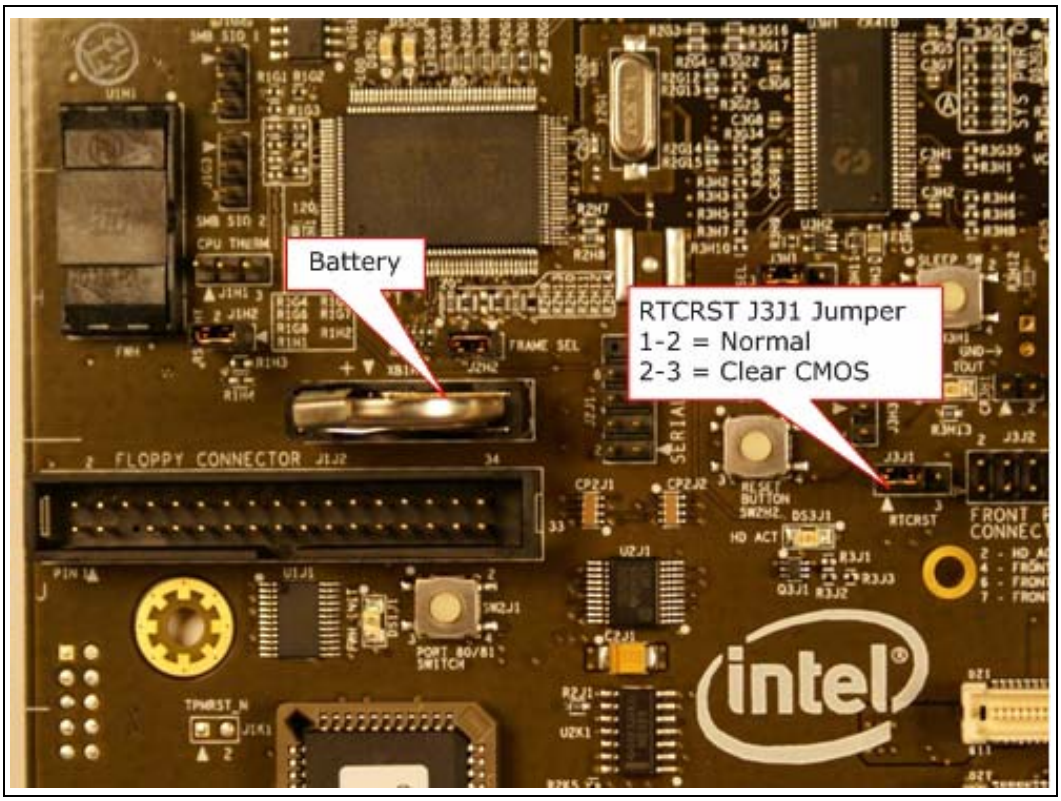
- The supervisor password gives unrestricted access to view and change all the options in the Pre-boot Firmware setup menu. This is supervisor mode.
- The user password gives restricted access to view and change options in the Pre-boot Firmware setup menu. This is user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password bar of the setup menu allows the user restricted access to the setup menu.
- If both the supervisor and user passwords are set, the user can enter either the supervisor or user password to access setup. User has access to setup respective to which password is entered.
- Setting the user password restricts who can boot the Intel® EP80579 Development Board. The password prompt is displayed before device boot. If only the supervisor password is set, the Intel® EP80579 Development Board boots without asking for a password. If both passwords are set, the user can enter either password to boot.
- For enhanced security, use different supervisor and user passwords.
- Valid password characters are A-Z, a-z and 0-9. Passwords can be up to 16 characters in length.

5.11 Clearing CMOS

The Intel® EP80579 Development Board provides a feature to clear the CMOS clock and date setting. Clearing the CMOS does not restore the original default setting for the Pre-boot Firmware. Here are the steps to clear CMOS:

1. Power down the Intel® EP80579 Development Board completely (via ATX power supply).
2. Remove the battery from the socket.
3. Move jumper J3J1 to cover pins 2-3 and wait for a few seconds.
4. Restore the jumper to the original position, covering pins 1-2.
5. Replace the battery in the socket, ensuring it is in the correct position.

Figure 16. CMOS Location



If the administrator password in the Pre-boot Firmware is set and the user forgets the password, the Intel® EP80579 Development Board Pre-boot Firmware must be reflashed (see Section 5.8).

If the Pre-boot Firmware is completely corrupted, or any configuration setting is incorrect, causing the Pre-boot Firmware to not boot, the Pre-boot Firmware must be reflashed into the Intel® EP80579 Development Board firmware device (FWH or SPI Flash) using an external firmware device (FWH or SPI Flash) programmer (not AFUEFI).

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6.0 Platform Setup

This section describes setting up the Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit for operation.

Note: This document assumes that the user is familiar with basic concepts required to install and configure hardware for a PC system.

The Intel® EP80579 Development Board is shipped as an open system attached to an acrylic base. Some assembly is required. Standoffs are mounted on the acrylic base to provide flexibility in changing hardware configurations and peripherals, such as is necessary in a lab environment. Because the board is not enclosed in a protective chassis, the user must adhere to safety precautions in handling and operating the Development Board.

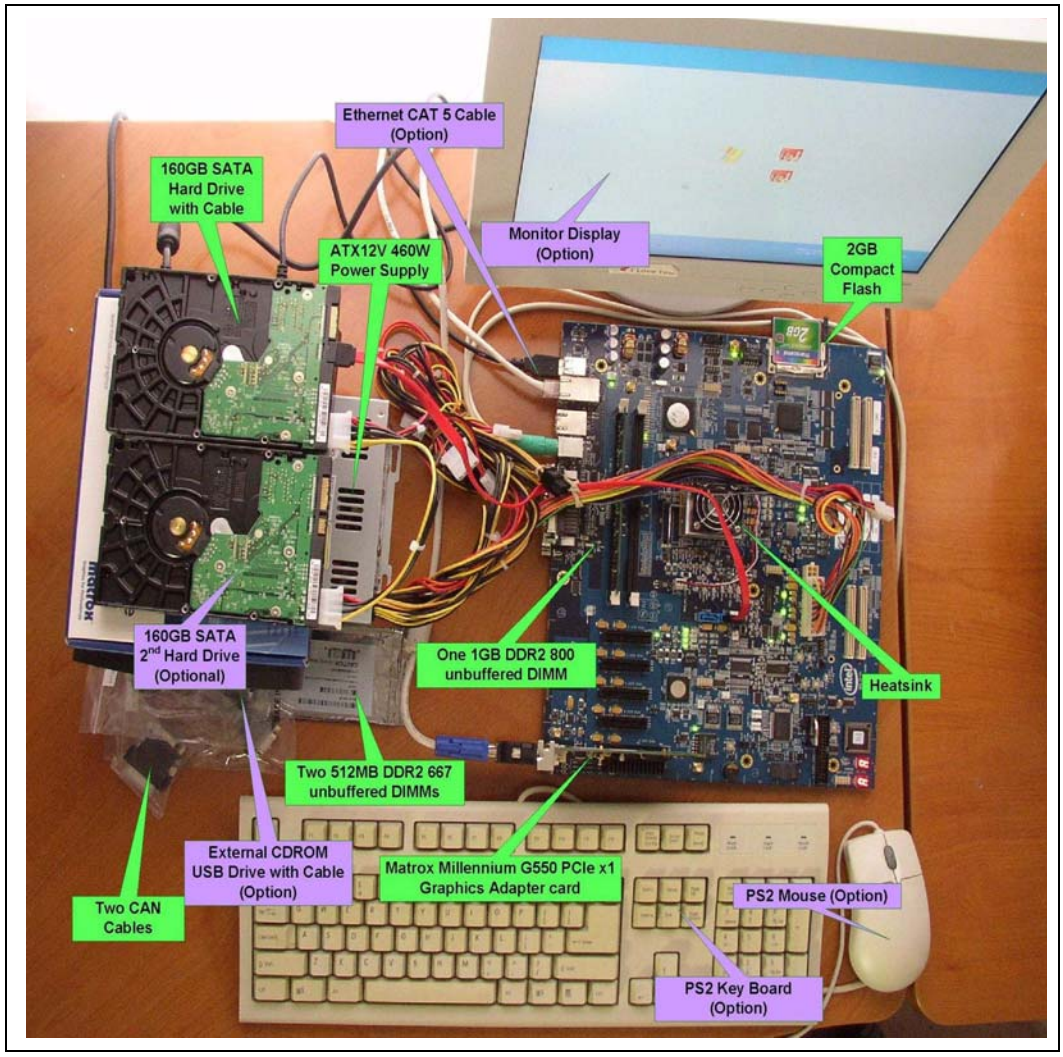
6.1 Setting up the Platform

Ensure that all components listed in Section 2.2 arrive together. Once all components have been identified and located, installation and setup can begin. Figure 17 shows the basic setup for the Intel® EP80579 Development Board (components described by a green text box are included in the Intel® EP80579 Development Kit package. Components described by a purple text box are optional and are not included in the Intel® EP80579 Development Kit package).

This section describes how to set up the Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit for operation. All jumpers are set to their defaults and the platform is ready to boot. See Table 13 for jumper locations and default settings.

Note: This document assumes that the user is familiar with the basic concepts required to install and configure hardware for a PC system.

Figure 17. Intel® EP80579 Development Kit Basic Setup



6.1.1 Safety

The Intel® EP80579 Development Board ships as an open system with standoffs installed on an acrylic base allowing for maximum flexibility to change hardware configurations and peripherals in a lab environment. Since the board is not in a protective chassis, the user is required to take safety precautions in handling and operating the board. Some assembly is required before use.

Ensure a safe and static-free work environment before removing any components from their anti-static packaging. The Intel® EP80579 Development Board is susceptible to electrostatic discharge, which may cause failure or unpredictable operation. The Intel® EP80579 Development Board must be operated on a flame retardant surface because a chassis is not included with the platform.

Caution: Connecting the wrong cable or reversing a cable may damage the board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to the board.

Caution: The power supply cord is the main disconnect device to main power (AC power). The socket outlet should be installed near the equipment and should be readily accessible. To avoid shock, ensure that the power cord is connected to a properly wired and grounded receptacle. Do not connect/disconnect any cables or perform installation/ maintenance of the boards for this product during an electrical storm. Ensure that any equipment to which this product will be attached is also connected to properly wired and grounded receptacles.

Note: Ensure that setting up the ATX power supply is the final step performed in the process of assembly.

6.1.2 Connecting the SATA Cables

The Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit provides two Serial ATA (SATA) connectors. Connect the cables to the appropriate drives sequentially, starting with Port 0 and ending with Port 1. See Figure 18 and Figure 19 for the location of the SATA connectors.

Note: Intel recommends connecting the boot drive to SATA Port 0.

Figure 18. Connecting SATA Port 0

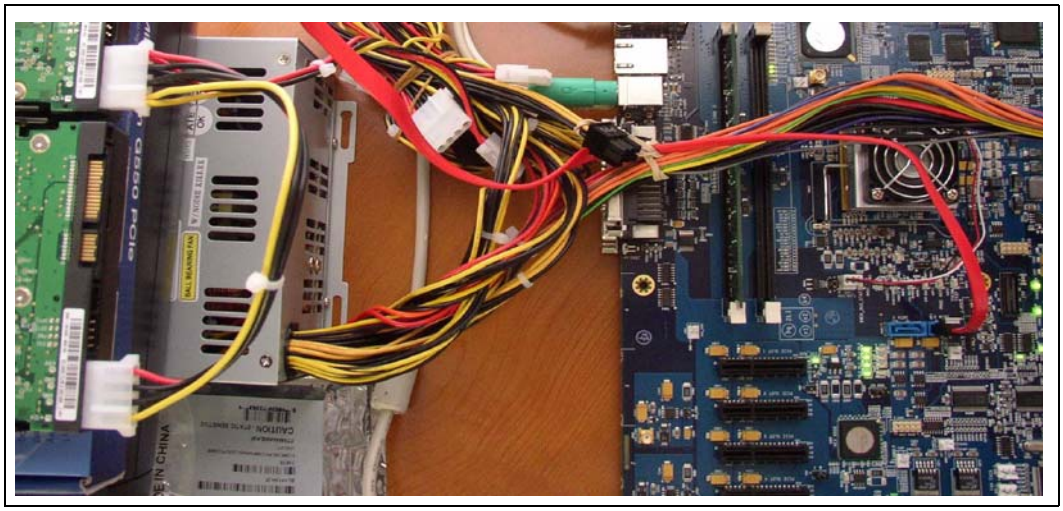
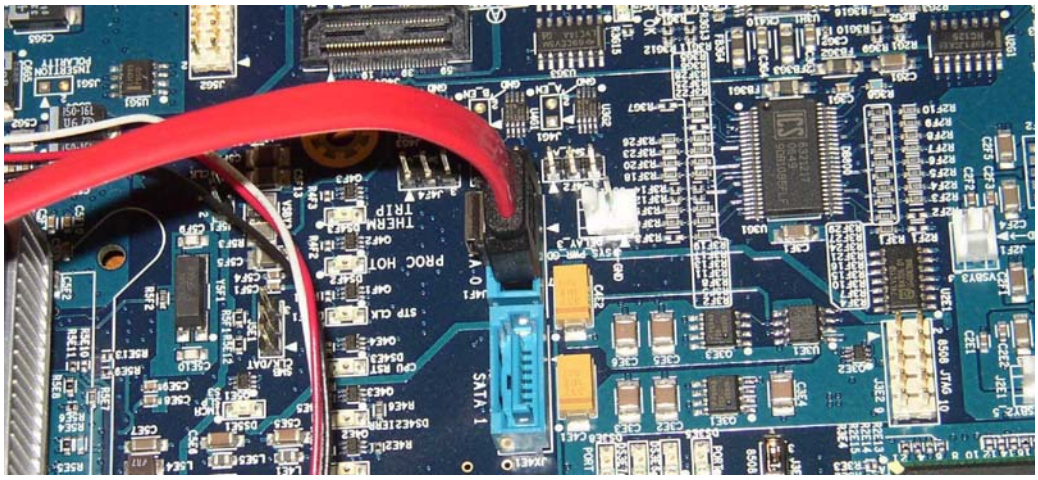


Figure 19. Close-up of Connection SATA Port 0

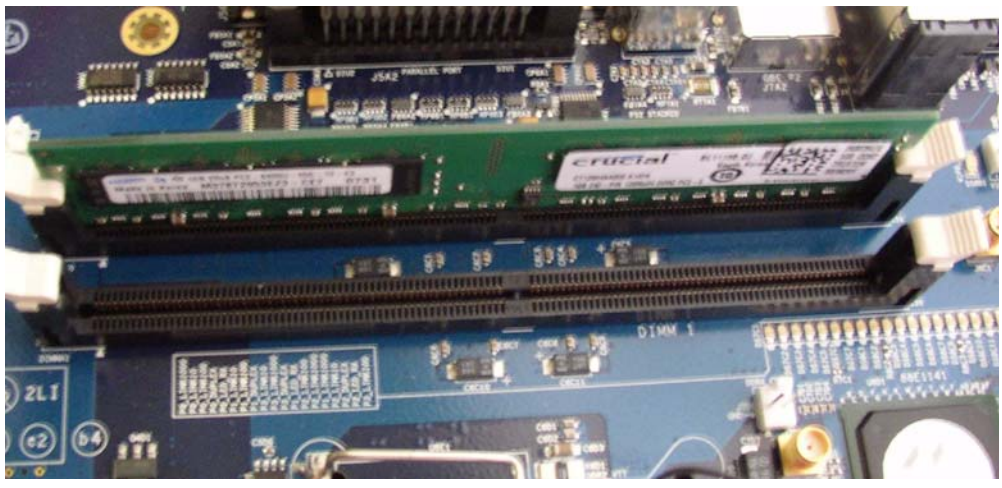


6.1.3 Installing Memory

The reference kit includes one 1 GB DDR2-800 DIMM. Use the following procedure to install the DIMM:

1. Ensure the tabs on the slot are open or rotated outward from the slot.
2. Line up the first DIMM above the DIMM 0 socket (the DIMM is keyed so that it only fits in the slot in one orientation). The DIMM 0 socket is the furthest DIMM socket from the processor. See Figure 20.
3. Firmly, but carefully insert the DIMM into the slot until the tabs close.

Figure 20. Memory Installation - 1 GB DDR-800 DIMM in DIMM 0 Socket



Note: If only a single DIMM is used, always install it in the DIMM 0 socket.

Caution: Do NOT bend the board when installing the memory. Several components are located near the memory slots, and excessive board flex may lead to solder joint failure.

6.1.4 Connecting the Processor Heatsink and Fan

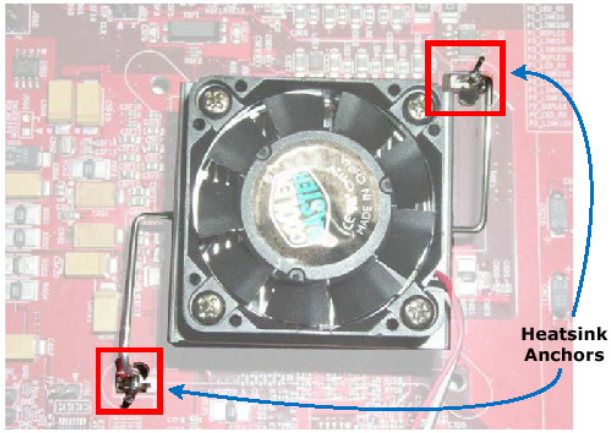
Connect the active CoolerMaster* heatsink to the Intel® EP80579 Integrated Processor and then plug the fan into the CPU FAN connector, as follows:

1. Clean the top surface of the Intel® EP80579 Integrated Processor IHS with a clean towel and isopropyl alcohol.

Note: There may be a protective liner or cover over the Thermal Interface Material (TIM) on the bottom of the heatsink. If one is present, remove it before assembling the heatsink.

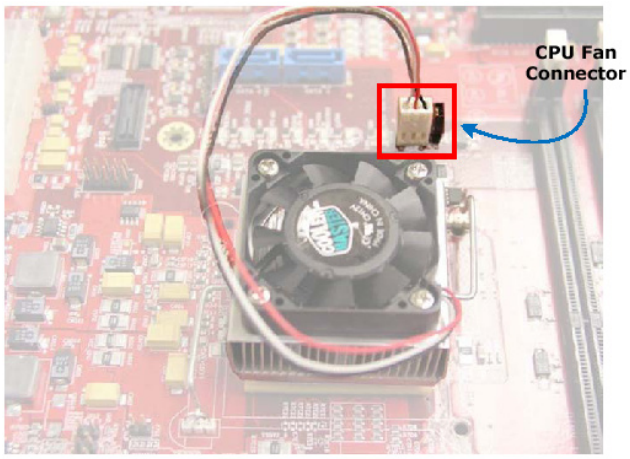
2. Hook one end of the heatsink clip to one of the soldered-down anchors located near the corner of the Intel® EP80579 Integrated Processor package. Securely hold the other end of the heatsink clip.
3. Hold the clip firmly to the anchor to prevent the heatsink from moving. Attach the other end of the clip to the other anchor in the opposite corner of the package. Ensure that the heatsink is level and centered on the Intel® EP80579 Integrated Processor package. Figure 21 shows a proper installation of the heatsink.

Figure 21. Proper Installation of Heatsink



4. Plug the fan connector into the CPU FAN connector on the Intel® EP80579 Development Board. Figure 22 shows the location of the CPU FAN connector. See Section 4.1 for the location of the CPU FAN connector.

Figure 22. Location of CPU FAN Connector



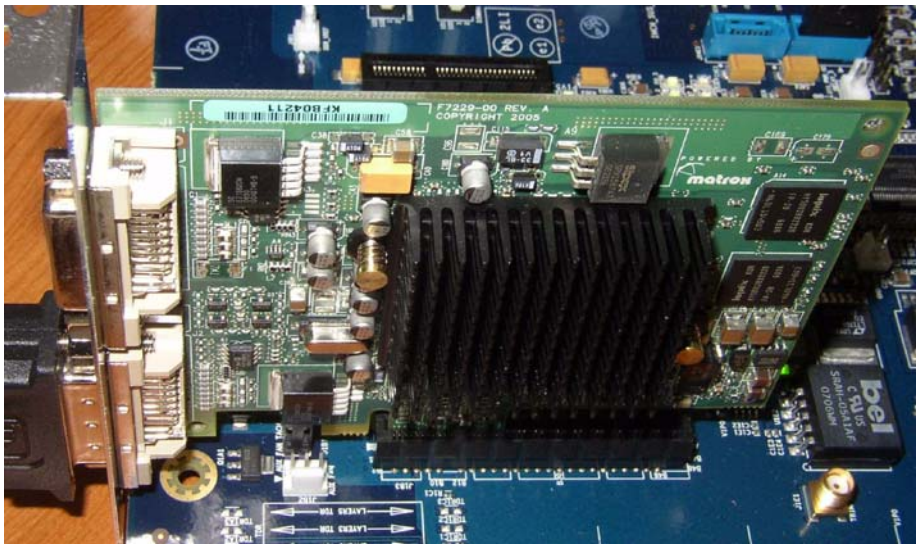
Warning: Do not apply power to the Intel® EP80579 Development Board until the heatsink and fans are correctly installed.

The processor fan must be connected to the CPU FAN connector, not to a chassis fan connector (AUX/AUX0/AUX1). Connecting the processor fan to a chassis fan connector may result in on-board component damage that may halt fan operation.

6.1.5 Installing the PCI Express Video Card

Install the PCIe x1 graphics adapter card into any one of the PCIe slots, 0-4. Figure 23 shows the graphics adapter card installed into slot 0. The video cable must connect to the bottom port of the graphics adapter card.

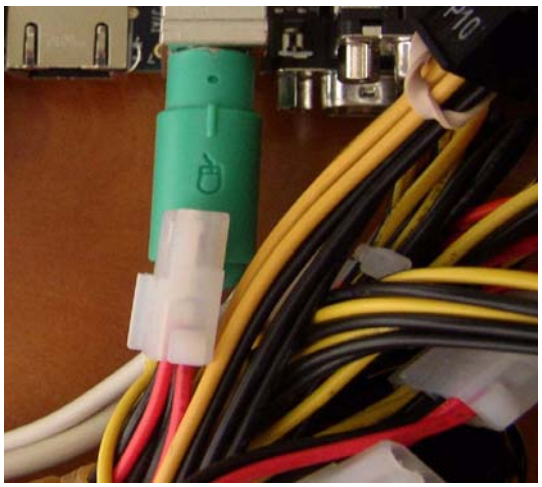
Figure 23. Graphics Adapter Installation - PICe Slot 0



6.1.6 Connecting the Keyboard and Mouse

Figure 24 shows a PS/2 mouse and keyboard connection to the stacked PS/2 connector on the rear panel of the board. The bottom connector is the keyboard connector and the top connector is the mouse connector. Alternatively, a USB keyboard and a USB mouse can be connected to the Intel® EP80579 Development Board's USB connectors.

Figure 24. Connecting the PS/2 Keyboard and PS/2 Mouse



Note: The mouse and keyboard are not supplied by Intel.

Note: The serial redirection feature can be enabled to remotely access the board through a serial cable without attaching a keyboard or mouse to the Intel® EP80579 Development Board. See Section 6.1.7 for more information.

6.1.7 Connecting the Serial Cable for Console Redirection

Connect one end of a serial cable to one of the serial ports on the board and the other end of the serial cable to the host computer with a serial console terminal installed.

Note: The serial cable is not supplied by Intel.

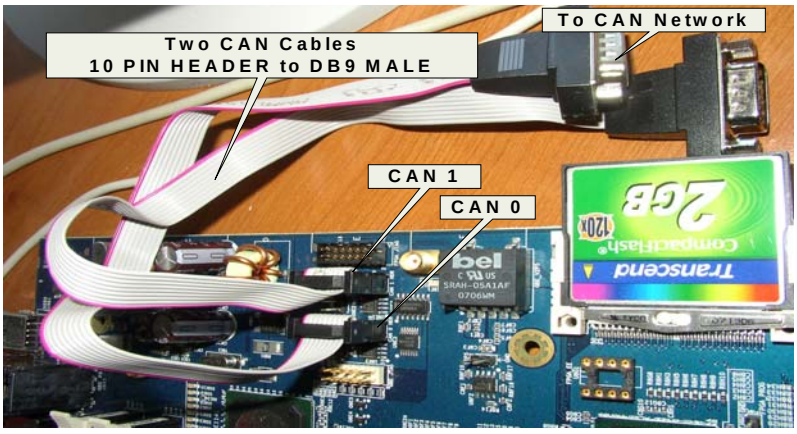
Note: Ensure that the port setting on the terminal console is the same as the Pre-boot Firmware serial redirection port setting. See Chapter 5.0, "Pre-boot Firmware" for the default setting of the Pre-boot Firmware serial redirection feature.

6.1.8 Connecting the CAN Interface Cables (optional)

There are two CAN ports, CAN port 0 (inner 10-pin header) and CAN port 1 (outer 10-pin header) as shown in Figure 25. The (10-pin header to DB9) cables provided should be used to connect the CAN network.

CAN interface cables can be used as COM3 (SIO Tertiary UART) in J2J1 2x5 header. See Table 26, Table 14, and Figure 14 for more information.

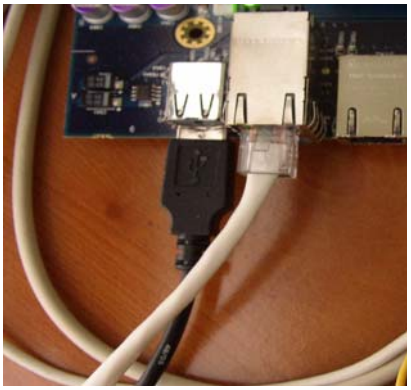
Figure 25. Connecting the CAN Interface Cables



6.1.9 Connecting the DVD-ROM Drive and GbE Ethernet Port

Figure 26 also shows the Ethernet cable connection to GbE Ethernet port 0 (the cable on the right). Connect the SATA DVD-ROM cable to SATA Port 1. See Figure 19 on page 59 for the SATA Port 0 and SATA Port 1 locations.

Figure 26. Connecting Ethernet Cable Port 0



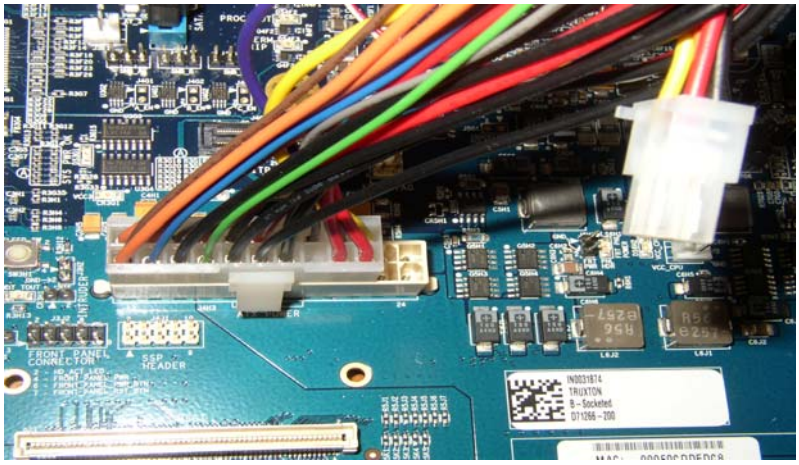
Note: The Ethernet cable is not supplied by Intel.

6.1.10 Connecting the Power Cables

Use the following procedure to connect the power cables:

1. The board supports the use of ATX12V power supplies with either 2x10 or 2x12 main power cables.
2. Plug the main connector into the Intel® EP80579 Development Board. Ensure that the plug clip lines up with the clip lock and the connector pins easily fit into their appropriate slots. When using a power supply with a 2x12 main power cable, attach the cable to the right-most part of the main power connector, leaving pins 11, 12, 23, and 24 unconnected, as shown in Figure 27.
3. Plug in the power connectors from each of the SATA drives and disk drives.

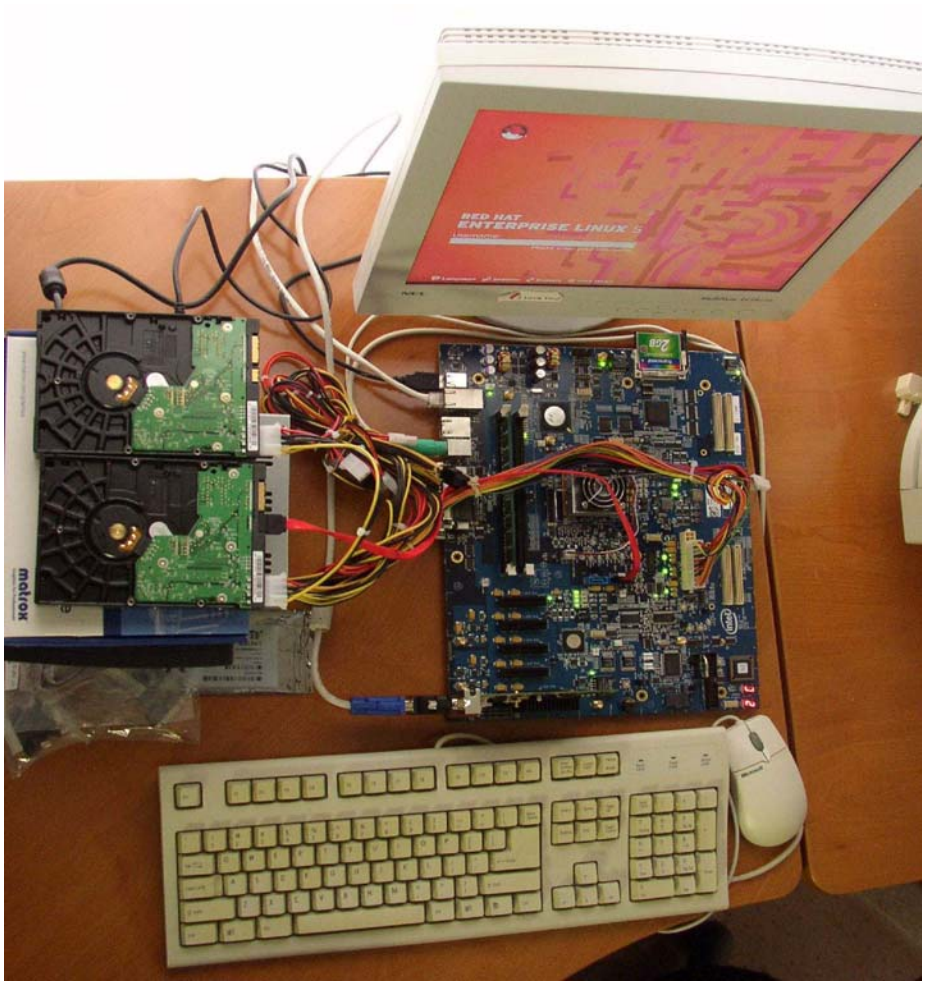
Figure 27. Connecting ATX Power Supply Cable



6.1.11 Stand-alone Target Platform

Figure 28 shows the system setup when the Intel® EP80579 Development Board is configured as a stand-alone target platform.

Figure 28. Intel® EP80579 Stand-alone Target Platform



6.1.12 Powering Up the System

Warning: Ensure the steps in the previous sections were precisely followed before powering up the system.

Use the following procedure to power up the Intel® EP80579 Development Board:

1. Ensure that the processor heatsink and fan are installed according to the procedure in Section 6.1.4.
2. Leaving the On/Off switch in the OFF position, plug the power cable into the back of the power supply.
3. Once the board is set up, plug the power cord into the power source.
4. Switch on the power supply.
5. Press the power button to start the system. See Figure 8 and Table 9 for the location of the power button.

6.1.13 Connecting Mezzanine Cards (optional)

The Intel® EP80579 Development Board supports two types of mezzanine cards: the Intel® EPAVM80579 Analog Voice Mezzanine Card (4-port analog voice card) and the Intel® EPTEM80579 Quad T1/E1 Mezzanine Card (quad T1/E1 card). Figure 29 shows the mezzanine cards installed onto the Intel® EP80579 Development Board.

The Intel® EPAVM80579 Analog Voice Mezzanine Card can be installed into any HSS port connector either top or bottom, however because of the size and mounting hole orientation, the Intel® EPTEM80579 Quad T1/E1 Mezzanine Card is restricted to top assembly installation on HSS0 or HSS1 or both ports.

Warning: Do not apply power to the Intel® EP80579 Development Board until the mezzanine cards are installed correctly.

The installation process is simple, however it does require careful handling of the boards to avoid damage.

Tools and parts required:

- One flathead screwdriver (not provided)
- Two flathead 4-40 stainless steel screws per card (provided with card)

Use the following procedure to install the mezzanine card:

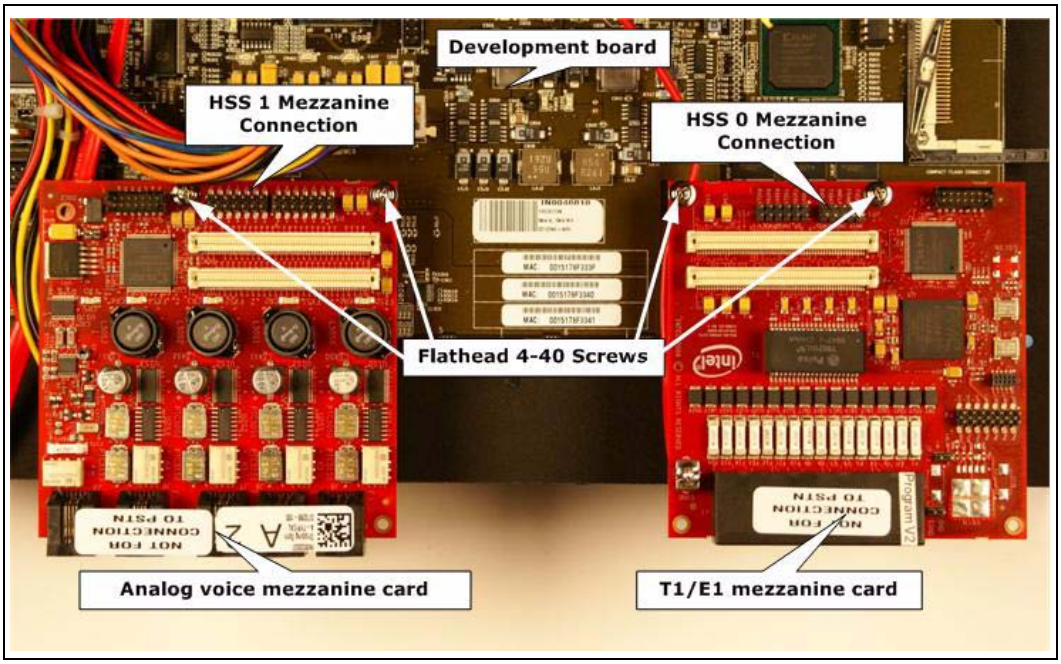
1. Insert the desired mezzanine card as shown in Figure 29. Note that the connectors have guides to make the insertion easier and allow proper mating of pins.
2. Once the card has been fully inserted, take one of the 4-40 screws, place it into the mounting hole shown in Figure 29, and screw it in the threaded stand off.
3. Repeat the process with the second screw.
4. Tighten both screws. Note that the amount of torque required can be sufficiently achieved by two fingers operating the screwdriver.

The previous installation is optional and applies only when the Intel® EP80579 Development Board is used to perform functions for the Time Division Multiplexing (TDM) interface.

Only certain SKUs may contain this feature. This feature must be enabled with Intel® EP80579 Integrated Processor Product Line software. See the processor software documentation for more information.

Caution: To avoid product damage, do not bend or use excessive force when installing the mezzanine cards. Press the cards down only at the mezzanine connectors.

Figure 29. Connecting the Mezzanine Cards (optional)



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7.0 Error Messages and Beep Codes

7.1 Pre-boot Firmware Beep Codes

The Intel® EP80579 Development Board speaker provides audible error message (beep code) information during POST. Table 35 provides information about the beep codes:

Table 35. Beep Code Types

Type	Pattern	Frequency
Memory error	Three long beeps	1280Hz
Thermal warning	Four alternating beeps: High tone, low tone, high tone, low tone	High tone: 2000Hz Low tone: 1600Hz

7.2 Pre-boot Firmware Error Messages

Whenever a recoverable error occurs during POST, the Pre-boot Firmware displays an error message describing the problem. Table 36 lists the error messages and provides a brief description of each.

Table 36. Pre-boot Firmware Error Messages

Error Message	Description
CMOS battery low	The battery may be losing power. Replace the battery soon.
CMOS checksum bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run setup to reset the values.
Memory size decreased	Memory size has decreased since the last boot. If no memory was removed, then memory may be bad.
No boot device available	System did not find a device to boot.

7.3 Debugging the EFI

During Intel® EP80579 Development Board power-up, the Pre-boot Firmware generates debug messages that can be used to determine the point / module at which an error occurred. Several messages are displayed from the memory initialization, SEC, PEI, and DXE phase. The debug messages can be accessed through the serial port when the serial port is configured according to the settings in Table 34 on page 51.

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8.0 Socketed Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Extraction and Insertion Instructions

8.1 Tools and Preparation

The EP80579 Processor connects to the Intel® EP80579 Development Board by a socket that allows the user to replace the processor with a different EP80579 Processor SKU. This section provides directions on how to insert and extract the processor.

Caution: **Carefully follow these directions, otherwise the processor and platform may be damaged**.

Tools needed:

- Advanced Interconnects Dual-sided Extraction Tool
  Or (quantity 2) Advanced Interconnects Single-sided Extraction Tool
- ESD strap

Consumable items needed:

- Disposable towels
- Heatsink thermal grease

Figure 30. EP80579 Processor Location

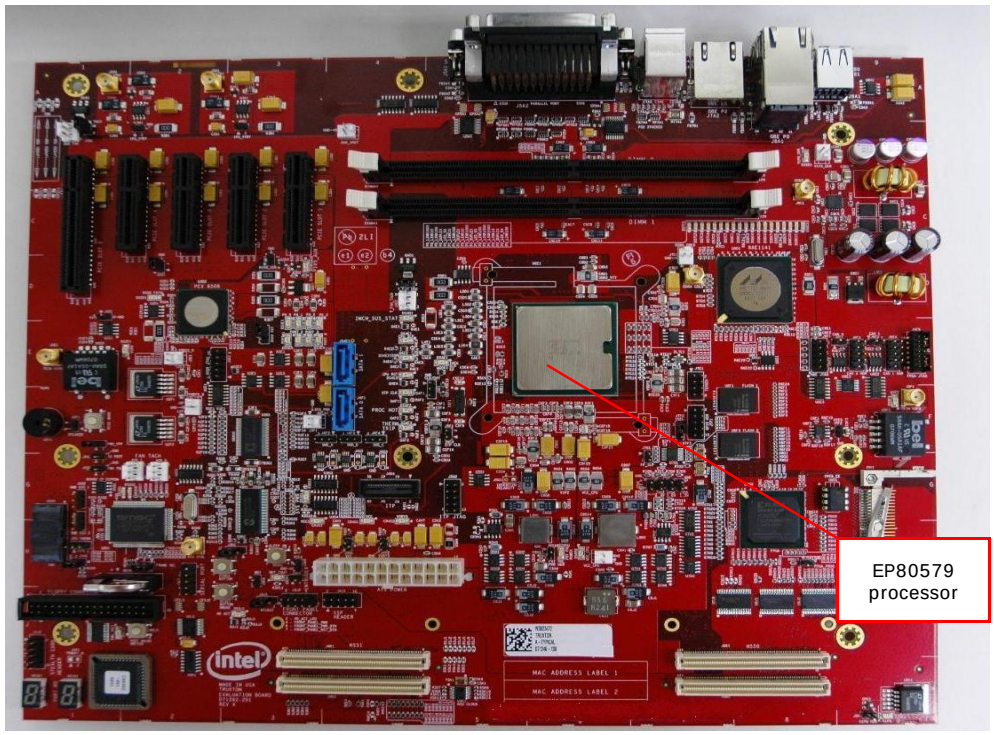
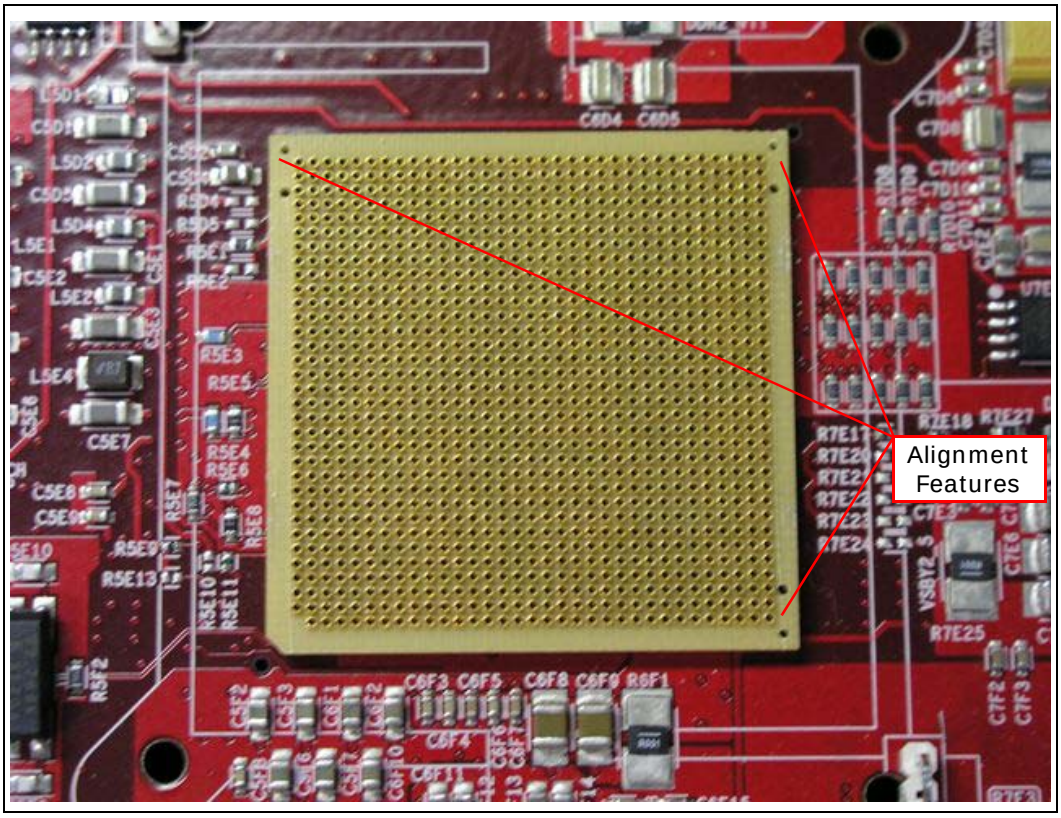
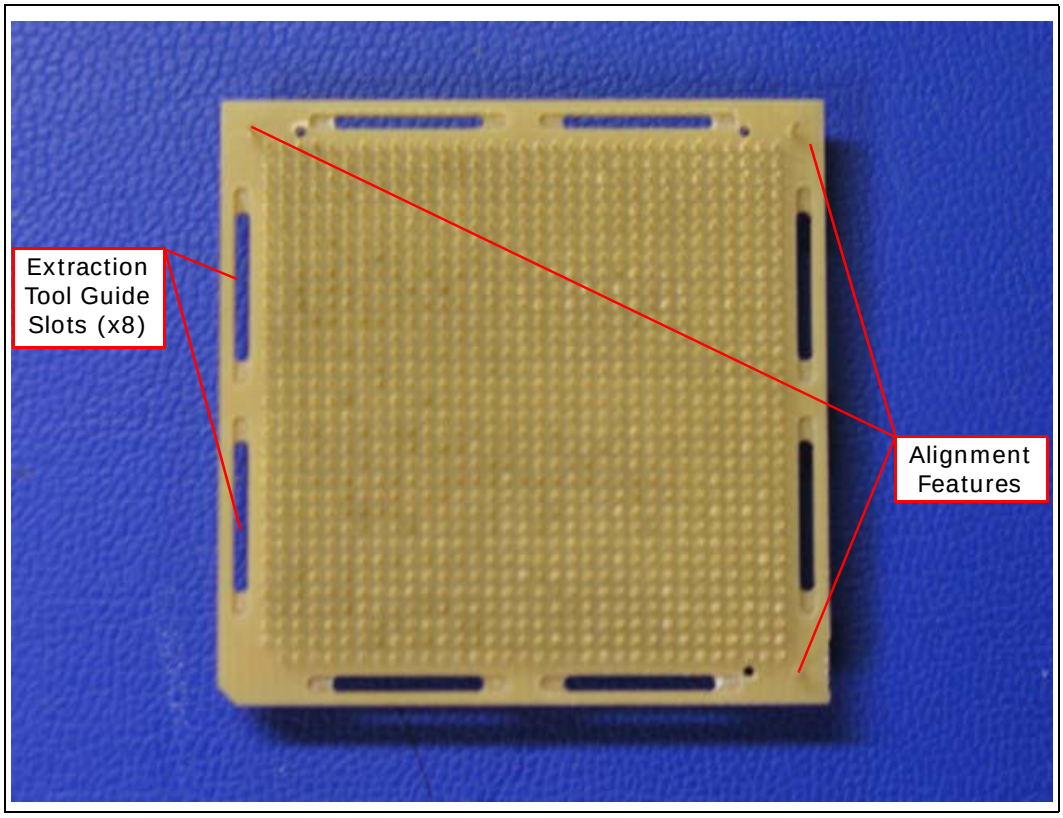


Figure 31. Advanced Interconnections 1088 POS PGA-to-BGA Socket



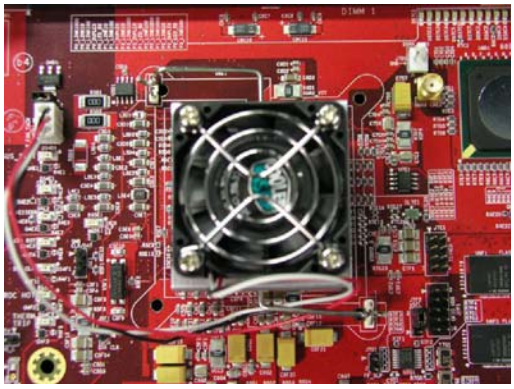
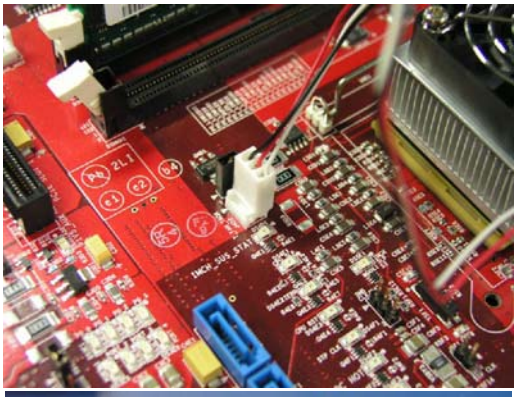
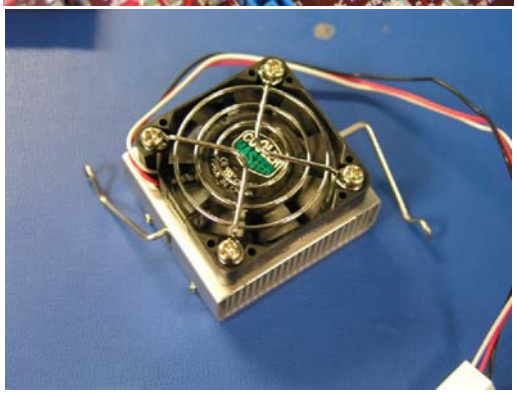
Socket alignment features include holes at three corners.

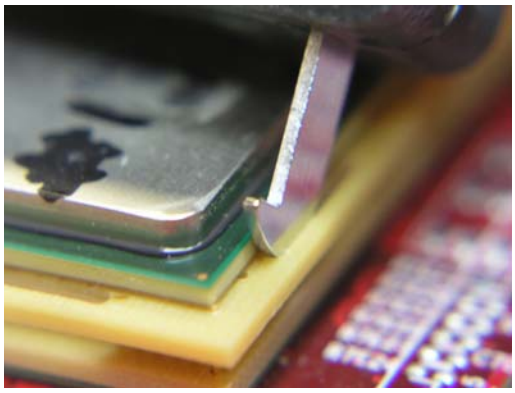
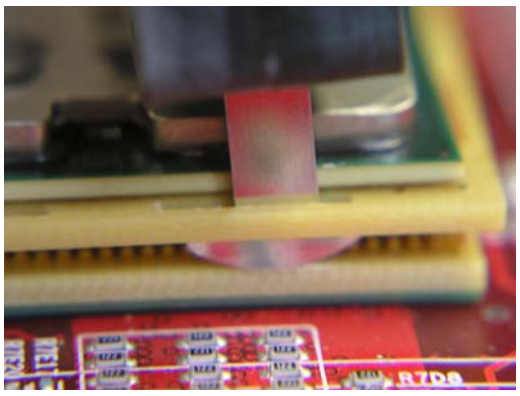
Figure 32. Advanced Interconnections 1088 BGA-to-PGA Interposer (pin side facing up)

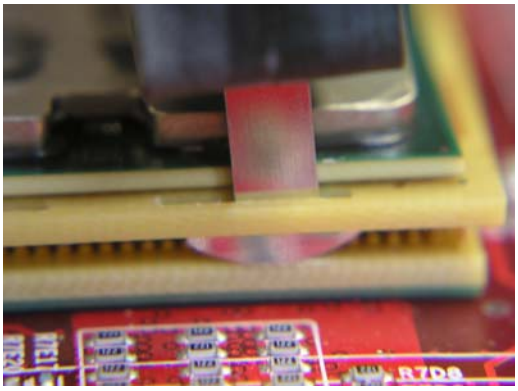
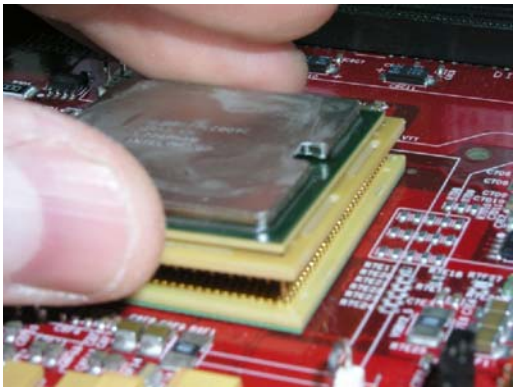


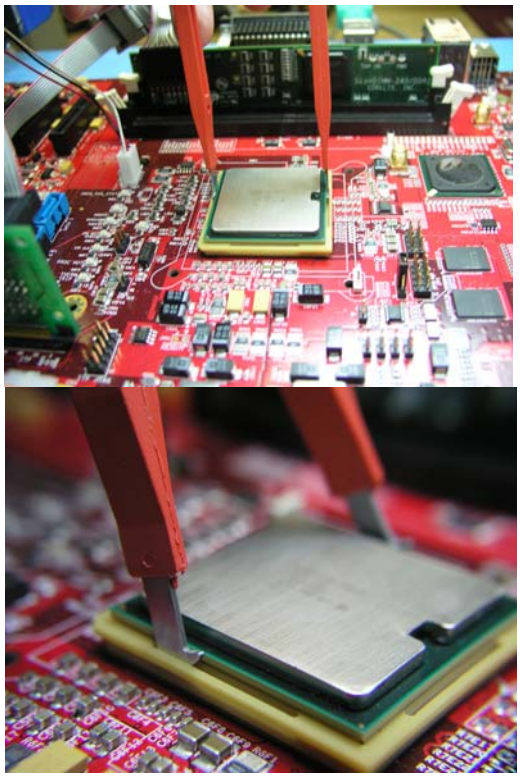
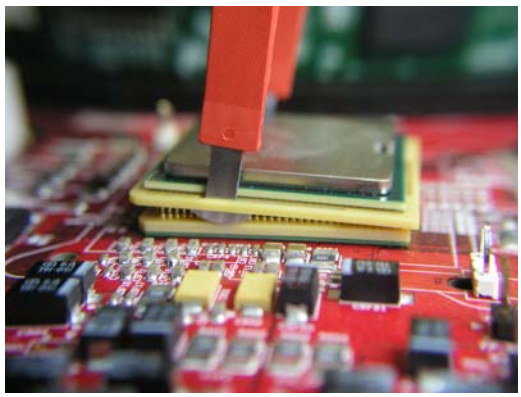
Interposer alignment features include posts at three corners.

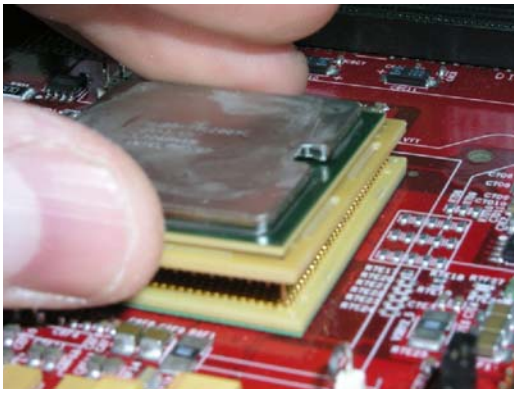
8.2 Extraction Instructions — Intel® EP80579 Development Board with Advanced Interconnects Interposer

Steps		Figures
1.	Disengage CPU heatsink/fan retention clips from board mounted anchor clips located at opposing corners of CPU location.	
2.	Unplug heatsink fan cable from CPU fan header on board. Remove heatsink from top of CPU integrated heat spreader by twisting base of heatsink ¼ turn clockwise or counterclockwise. ***Note:*** If using a dual-sided extraction tool go to step #3 and continue reading below. If using a single-sided extraction tool, go to step #8.	 

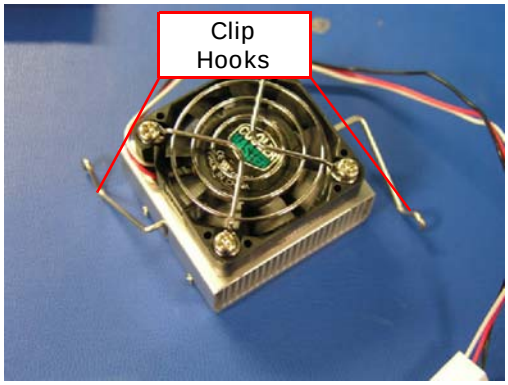
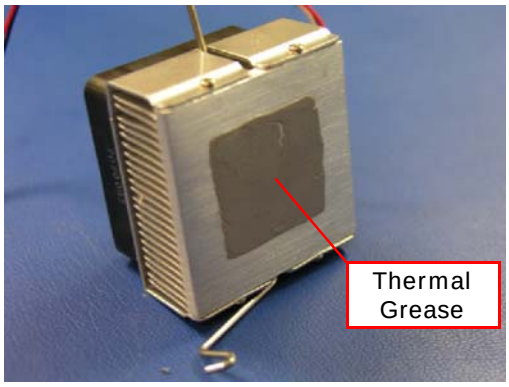
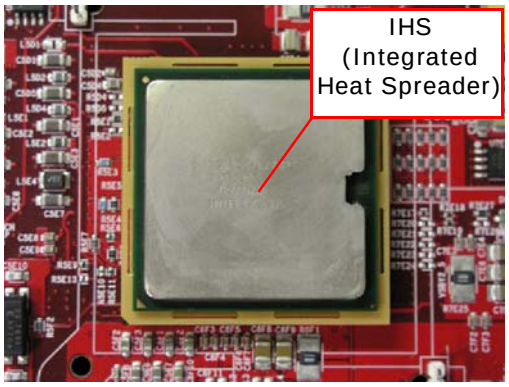
Steps	Figures
3. Insert the extraction tool blades into the guide slots located on edges of interposer. Slide the blade edges of the tool towards the center end of guide slots (located along center line of CPU) and engage both sides of the extraction tool under end of guide slots.	
The extraction tool blade has a semi-circular cam shape that is allows the tool to impart a positive Z direction (*out of the board*) force on bottom edge of interposer via a cam-like action. 4. Gently **pull** the arm of extraction tool until interposer pins begin to pull out of the socket. Remove the socket extraction tool from the guide slots.	
5. Insert the extraction tool blades into the adjacent guide slots on the edges of the interposer. Slide the blade edges of the tool towards the center end of guide slots (located along center line of CPU) and engage both sides of the extraction tool under the end of the guide slot.	

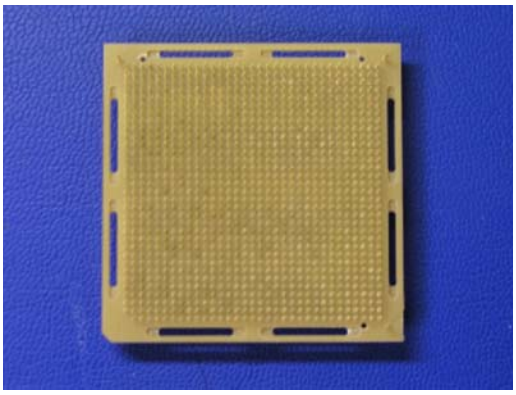
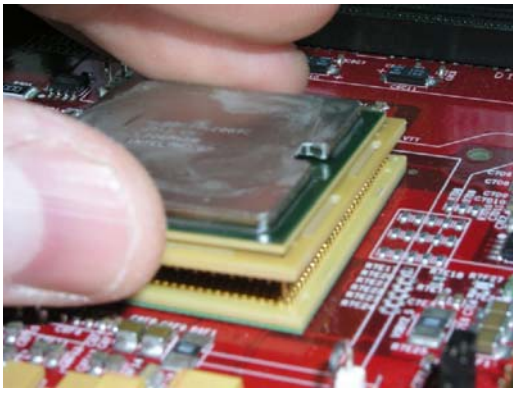
Steps		Figures
6.	Gently **push** the arm of the extraction tool until interposer pins continue to release from socket further. Remove the socket extraction tool from the guide slots. By alternating the extraction motion and positioning the tool at the front and back interposer slot locations, the operator can keep the extraction motion uniform in the positive Z direction (*out of the board*).	
7.	Repeat steps 3 through 6 as necessary to release the interposer and CPU from socket. Grasp the edges of the interposer and manually extract the loose part from the socket assembly. **Take care to protect exposed pins from damage.** **Extraction complete.** If needed, see Section 8.2, "Extraction Instructions — Intel® EP80579 Development Board with Advanced Interconnects Interposer to install a new part.	

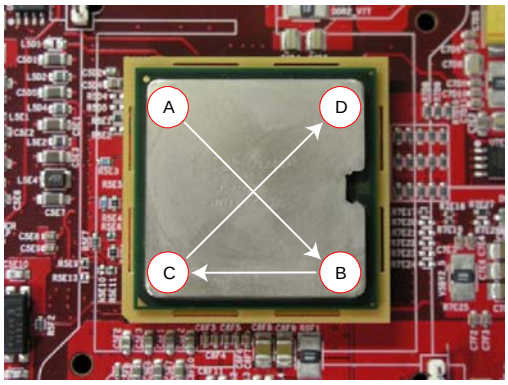
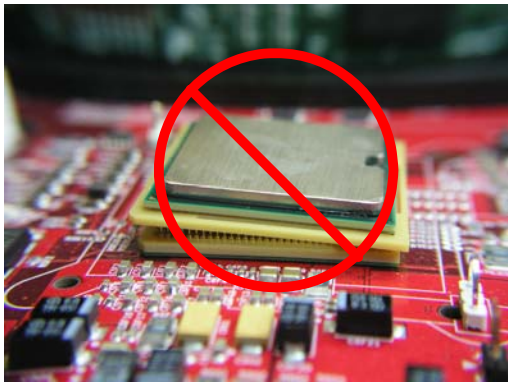
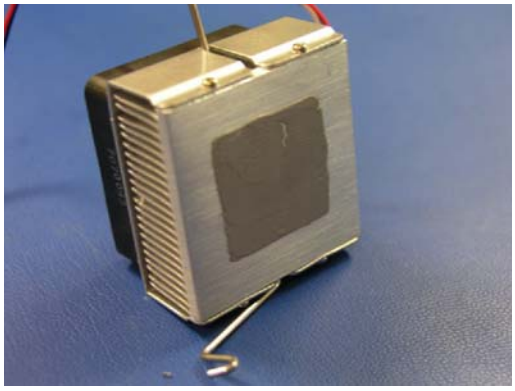
Steps	Figures
8. (**For Single-sided Extraction Tools** - **Continued from step 2**) Insert the two extraction tool blades into the guide slots located on the edges of the interposer. Slide the blade edges of towards the center end of the guide slots (located along center line of CPU) and engage both extraction tools under the ends of guide slots.	
Extraction tool blades have a semi-circular cam shape that allows the tool to impart a positive Z direction (*out of the board*) force on bottom edge of interposer via a cam-like action. 9. Gently and uniformly **pull** the arms of the extraction tools until the interposer pins and CPU begin to pull out of the socket. Remove the socket extraction tools from guide slots.	

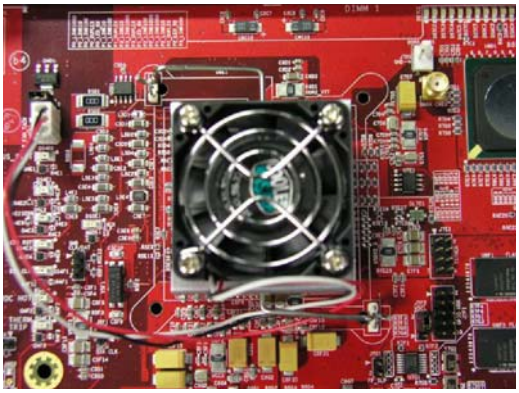
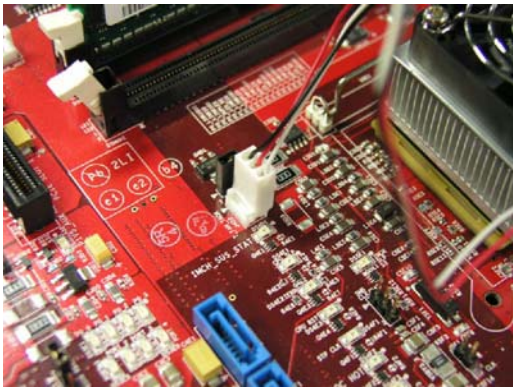
Steps		Figures
10.	Insert the extraction tools' blades into the opposing guide slots located on edges of interposer. Slide the blade edges towards the center end of the guide slots (located along center line of CPU) and engage both sides of the extraction tools under the ends of guide slots.	
11.	Gently **push** the arms of the extraction tools until interposer pins and the CPU continue to release from socket. Remove the extraction tools from the guide slots. By alternating the extraction motion and the position of the tools at the front and back interposer slot locations, the operator is able to keep the extraction motion uniform in the positive Z direction (*out of the board*).	
12.	Repeat steps 8 through 11 as necessary to release interposer and CPU from socket. Grasp the edges of the interposer and manually extract the loose part from the socket assembly. **Take care to protect exposed pins from damage.** **Extraction complete**. If needed, see Section 8.3, "Insertion Instructions — Intel® EP80579 Development Board with Advanced Interconnects Interposer to install a new part.	

8.3 Insertion Instructions — Intel® EP80579 Development Board with Advanced Interconnects Interposer

Steps		Figures
1.	The figures at the right shows the heatsink top and bottom view. The thermal grease, shown in the bottom view, is important to ensure heat transfer from the integrated heat spreader (IHS) to the heatsink.	 
2.	Wipe the surface of the CPU integrated heat spreader surface with a clean towel. Ensure surface is free from debris.	

Steps	Figures
3. Inspect the bottom of the interposed part for bent pins. If any pins are damaged or bent, do not install the part. Attempting to do so may damage the socket.	
The interposer pin array includes three slightly larger diameter, offset alignment pins located at three corners. The fourth corner is truncated. These alignment pins and corner feature ensure that the orientation of the interposed part with respect to the socket is correct. 4. Ensure that surface of socket is free from debris. Align the three corner alignment posts of the CPU and interposer assembly with the matching holes on the corners of the socket.	

Steps		Figures
5.	While holding the back of the Intel® EP80579 Development Board in the CPU area for support, press down on top of the CPU's integrated heat spreader to engage the interposer pins with the socket holes. Use the recommended pattern illustrated in the adjacent figure when applying force in the negative Z direction (*into the board*) to help preserve uniformity and symmetry of insertion. Not doing so may result in an improper connection. Inspect the sides of the part when engaged with socket to check for skewing. If present, (illustrated at right) correct it before moving to step 6. ***Note:*** Specification for interposer insertion force calls for up to ~80 lbf to ensure proper engagement of interposer with socket.	 
6.	If not present, apply thin layer of heatsink grease or thermal compound to the bottom of the heatsink fan.	

Steps		Figures
7.	Hook one end of the heatsink clip to one of the anchors located near the corner of the CPU. Securely hold the other end of the heatsink clip. Hold the clip firmly to the anchor to prevent the heatsink from moving. Attach the other end of the clip to the other anchor.	
8.	Plug in the heatsink fan cable to the CPU fan header on board. Ensure that the heatsink is level and centered on the CPU package and adjust it as necessary before using the Intel® EP80579 Development Board.	

Note: If you need to remove the heatsink, follow step 8 and then step 7.

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