July, 1997

Revision 1.4

80C186XL/80C188XL PROCESSOR RESET HYSTERESIS

Abstract

Designs using the 80C186XL/80C188XL processors must introduce sufficient hysteresis in the reset circuitry to ensure proper processor reset operation. Intel strongly recommends that all designs using the 80C186XL/80C188XL and 80L186XL/80L188XL processors include external hysteresis on the reset pulse generation circuitry. This document provides information on processor reset and reset hysteresis.

Throughout this document, references to the 186XL processors include all the package types of the 80C186XL, 80C188XL, 80L186XL, and 80L188XL processors.

Introduction

The 186XL processors were introduced in 1991 as a higher performance, lower power replacement for the 80C186/80C188 processors. The 186XL processors use a 1 micron process, which is inherently faster than the 1.5 micron process used to produce the 80C186/80C188 processors.

To provide the best upgrade solution from the 80C186/80C188 processors, internal Schmitt triggers were designed to meet worst-case scenarios for TTL and CMOS signal-level specifications (V_{IL} = 1.5*V_{CC} and V_{IH} = 3.0 V). As a result, hysteresis on the RES# pin of the 186XL processor is insufficient to protect against very slow rise time signal edges. V_{IL} and V_{IH} specifications were a higher priority design consideration than hysteresis.

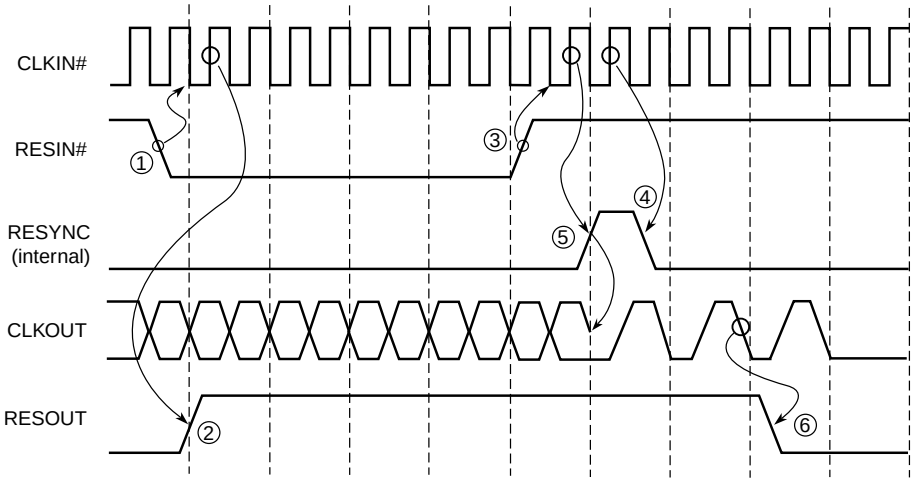
In environments with little noise, there are usually minimal problems due to decreased hysteresis. Designs with a long RC time constant on the reset input or measurable noise need to change the RC constant to a smaller value. Adding hysteresis via an external Schmitt trigger is strongly recommended for all designs.

Reset

An active RES# causes the processor to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the clock. The processor begins fetching instructions approximately 2.5 clock cycles after RES# is returned HIGH. For proper initialization, V_{CC} must be within specifications and the clock signal must be stable for more than four clocks with RES# held LOW. RES# is internally synchronized.

Reset may be either cold (power-up) or warm. A cold reset is performed when the RES# input is asserted during power supply and oscillator startup. The processor's pins assume their reset pin states a maximum of twenty eight (28) X1 periods after X1 and V_{CC} stabilize. RES# must be asserted an additional four X1 periods after the device pins assume their reset states. An RC time constant of 100 ms is usually sufficient.

Asserting RES# when the system is in operation constitutes a warm reset. In this case, assert RES# for at least four CLKOUT periods. The device pins assume their reset states on the second falling edge of X1 following the assertion of RES#.



NOTES:
1. Setup of RESIN# to falling CLKIN.
2. RESOUT goes active.
3. RESIN# allowed to go inactive after minimum 4 CLKOUT cycles.
4. RESYNC pulse generated.
5. RESYNC pulse drives CLKOUT low, resynchronizing the clock generator.
6. RESOUT goes inactive on the second falling CLKOUT edge following CLKOUT resynchronization.

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Figure 1. Clock Synchronization at Reset

Hysteresis

Hysteresis is the difference in the voltage between the positive-going switching threshold and the negative-going switching threshold at the input. Table 1 compares observed hysteresis values for the 186 and the 80C186/80C188 processors. A limited number of parts were tested to represent typical production material. All values given are at room temperature, as the value varies little over the operating temperature range.

Table 1. Observed Hysteresis Values

	Hysteresis @ Max V_{CC}	**Hysteresis @ Min V_{CC}**	**Range**
186XL	0.5589 V (avg.)	0.5844 V (avg.)	0.5119 V to 0.6950 V
80C18x	0.6755 V (avg.)	0.6558 V (avg.)	0.6369 V to 0.6950 V

A simple RC circuit to drive the RESET signal is highly susceptible to noise because of the large time constant and resulting slow rise time associated with the circuit. A singular switching point separates what is defined as a logic high signal and a logic low signal. It is possible that system or environmental noise could cause a rising signal to toggle from low to high, then high to low again in immediate succession. These low-to-high and back transitions can place the processor in an unknown state. Once the RESET changes from low to high, it must be held high for a minimum amount of time before it can be driven low again.

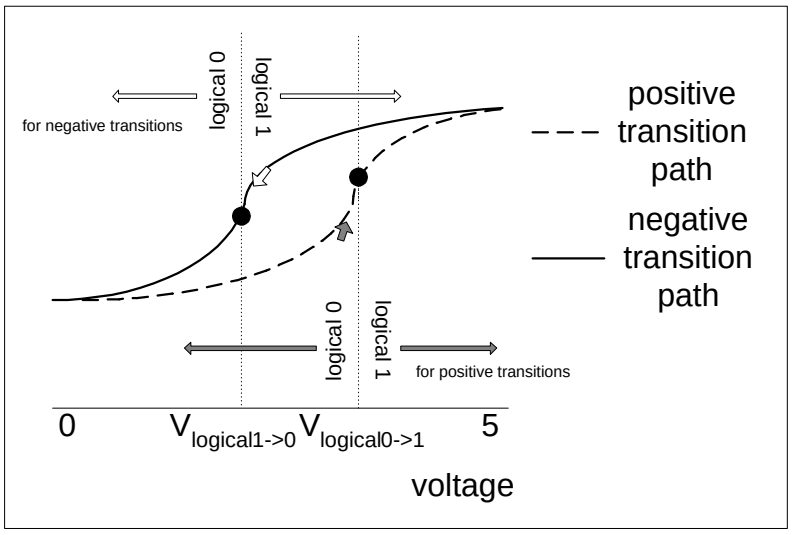

Figure 2. Hysteresis Graph of the RESET Signal

Hysteresis must be added to the RES# input so that the switching point for a low-to-high transition differs from the switching point for a high-to-low transition (see Figure 2). This ensures that any noise on the reset pin is unable to cause a rising RESET signal to toggle once it has gone from low-to-high.

To add hysteresis, an external Schmitt trigger must be designed into the reset circuit. This can be implemented as either one non-inverting Schmitt trigger or, more commonly (and with greater cost efficiency), as two inverting Schmitt triggers in series (see Figure 3). Another alternative is to use one of the many reset circuits available in the industry. As an example, the MAX698* or MAX701* should operate acceptably and is available from MAXIM Integrated Products, Inc., (408) 737-7600.

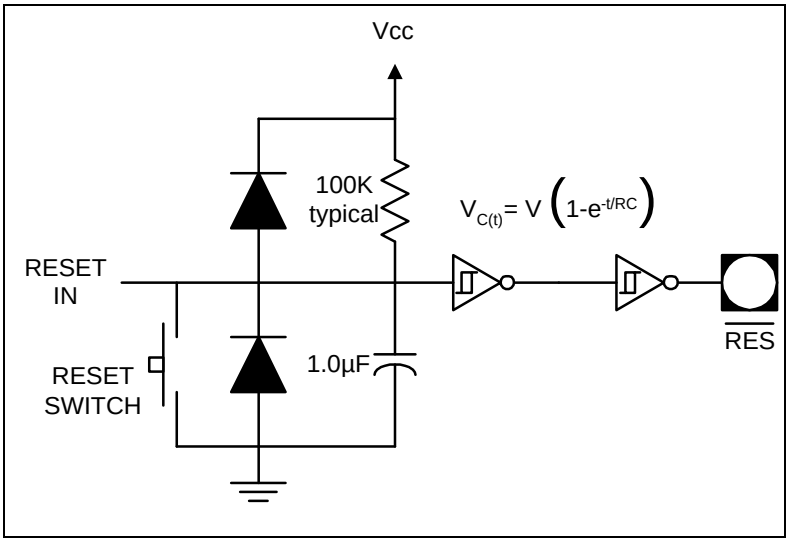

Figure 3. Simple RC Circuit with External Schmitt Triggers for Power-up Reset

* Third-party brands and names are the property of their respective owners.

Conclusion

Due to limited hysteresis on the RES# input pin, with resulting sensitivity to noise, Intel strongly recommends that all designs using the 80C186XL/80C188XL and 80L186XL/80L188XL processors include external hysteresis on the reset circuitry.

References

To order these documents using Intel's FaxBack service, call (800) 628-2283 in the U.S. and Canada, +44(0) 793-496646 in Europe, and (916) 356-3105 in any other location.

80C186XL/C188XL C-Step Compatibility With The 80186/188, Rev. 0.0, April 3, 1995
FaxBack #2370
http://support.intel.com/oem_developer/embedded_ia/186/design/2370.HTM

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Oscillator/Crystal Information for the 186 Family
FaxBack #2403
http://support.intel.com/oem_developer/embedded_ia/186/design/2403.HTM

Clarifying the Reset Operation for the 80C186XL/80C188XL
FaxBack #2404
http://developer.intel.com/design/intarch/technote/2404.HTM