Celeron™ Processor Mobile Module: Mobile Module Connector 2 (MMC-2) at 700 MHz, 650 MHz, 600 MHz, 550 MHz, 500 MHz, and 450 MHz

Datasheet

Product Features

- Mobile Celeron processor with processor speeds of 700 MHz, 650 MHz, 600 MHz, 550 MHz, 500 MHz, 450 MHz
- On-die, primary 16-K Instruction cache and 16-K Write Back Data cache
- On-die, 128-K L2 cache
  - —Four-way set associative
  - —Runs at the speed of the processor core
- Fully compatible with previous Intel mobile microprocessors
  - —Binary compatible with all applications
  - —Support for MMX™ technology
- Supports streaming SIMD
- Power management features providing low-power dissipation
  - —Quick Start mode
  - —Deep Sleep mode
- Integrated math co-processor
- Integrated Active Thermal Feedback (ATF) system
- Programmable trip point interrupt or poll mode for temperature reading
- Intel 82443BX Host Bridge system controller
  - —DRAM controller supports 3.3-V SDRAM at 100 MHz
  - —Supports PCI CLKRUN# protocol
  - —SDRAM clock enable support and self-refresh of SDRAM during Suspend mode
  - —PCI bus control 3.3V only, *PCI Specification, Revision 2.1* compliant
- Supports single AGP 66-MHz, 3.3-V device
- Two-piece thermal transfer plate (TTP) for heat dissipation
  - —The CPU TTP is made of nickel-plated copper
  - —The BX TTP is made of aluminum
- Mobile Celeron processor core voltage regulation supports input voltages from 7.5V to 21.0V DC
  - —Above 80% peak efficiency

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Revision History

Date	Revision	Updates
February 2000	1.0	Initial Release
April 2000	2.0	Revision 2.0 contains the following updates: •Added the new 550-MHz processor speed •Updated Section 4.5, “Power Consumption in Power Management Modes” •Added Table 16, “Power Consumption Values II” •In Table 20, “BCLK Signal Quality AC Specifications at the Processor Core” note 3 was updated for clarification •Added maximum and minimum designators to Figure 4, “BCLK Waveform at the Processor Core Pins” for clarity •Rewrote Section 5.3.3, “Power Planes: Bulk Capacitance Requirements” for clarity •Added 550-MHz TDPmodule values to Table 27, “Thermal Design Power Specifications
April 2000	3.0	Revision 3.0 contains the following updates: •Added product tracking codes (PTCs) for conversion modules. See Table 16, “Power Consumption Values II”
May 2000	4.0	Revision 4.0 contains the following updates: •Added new processor speeds 650 MHz and 600 MHz •Added Table 17, “Power Consumption Values III”, which contains new power management data
September 2000	5.0	Revision 5.0 contains the following updates: •Added new 700-MHz processor speed •Revised Table 17, “Power Consumption Values III”

1.0 Introduction

This document provides the technical information for integrating the Intel Celeron processor mobile module connector 2 (MMC-2) into the latest notebook systems for today's notebook market.

Building around this design gives the system manufacturer these advantages:

- Avoids complexities associated with designing high-speed processor core logic boards
- Provides an upgrade path from previous Intel mobile modules using a standard interface

1.1 References

Refer to the following documents for additional information on the Celeron processor mobile module.

- *Mobile Celeron™ Processor in BGA2 and Micro-PGA2 Packages at 700 MHz, 650 MHz, 600 MHz, 500 MHz, 450 MHz, and 400A MHz datasheet (Order Number 245417)*
- *Intel® 440BX AGPSet: 82443BX Host Bridge/Controller Datasheet (Order Number: 290633-001)*
- *82371AB PCI-to-ISA/IDE Xcelerator (PIIX4) (Order Number: 290562-001)*
- *Intel® 82371MB (PIIX4E/M) Specification Update*
- *CK97 Clock Synthesizer/Driver Specification (OR-1089)*
- *Intel® Mobile Module MMC-2 Simulation and Validation Kit Rev. 4.0 (OR- 2333)*
- *Intel® Pentium® III Processor Mobile Module System Electronics 100-MHz Layout Guidelines Rev. 1.0 (OR-1780)*
- *Mobile Pentium® III Processor/440BX AGPset Recommended Design and Debug Practices (RDDP-A) 100 MHz Rev. 2.0 (SC-2760)*
- *66/100 MHz PC SDRAM Unbuffered SO-DIMM Specification Rev 1.0*
- *Intel® Mobile Module Design Guide (AP-590)*
- *Pentium® II Processor Mobile Module MMC-2 Insertion & Extraction User Manual Rev 1.0*
- *Mobile Pentium® II Processor Mobile Module 400-Pin BGA Connector Assembly Development Guide Rev. 1.0*
- *Focused Discussion on Intel® Mobile Modules Design for Mfg. & Best Methods for MHPG Customers Rev. 1.0 (OR-1385)*
- *EMI design Guide (order number ORMD6-0859)*
- *Intel® Mobile Module Newsletters*
- *Intel ® Mobile Module Thermal Diode Temperature Sensor Application Note*
- *Intel® MMC-2 Standoff/Receptacle Height Spreadsheet*
- *AGP Interface Specification Version 2.0*

2.0 Architecture Overview

A highly integrated assembly, the Celeron processor mobile module contains the mobile Celeron processor core with with a 100-MHz processor system bus speed (PSB) and processor speeds of 700 MHz, 650 MHz, 600 MHz, 550 MHz, 500 MHz, and 450 MHz.

The Intel 440BX AGPset provides immediate system-level support for the mobile Celeron processor and includes the PIIX4E/M PCI/ISA Bridge and the 82443BX Host Bridge. The PIIX4E/M provides extensive power management capabilities and supports the Intel 82443BX Host Bridge. A notebook's system electronics must include a PIIX4E/M device to connect to the mobile module.

Key features of the Intel 82443BX Host Bridge include: the DRAM controller supporting SDRAM at 3.3Vwith a burst read at 4-1-1-1; the 82443BX Host Bridge also provides a PCI CLKRUN# signal to request the PIIX4E/M to regulate the PCI clock on the PCI bus; the 82443BX clock enables Self-Refresh mode of SDRAM during Suspend mode and is compatible with SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM) modes of power management. E_SMRAM mode supports write-back cacheable SMRAM up to 1 MB.

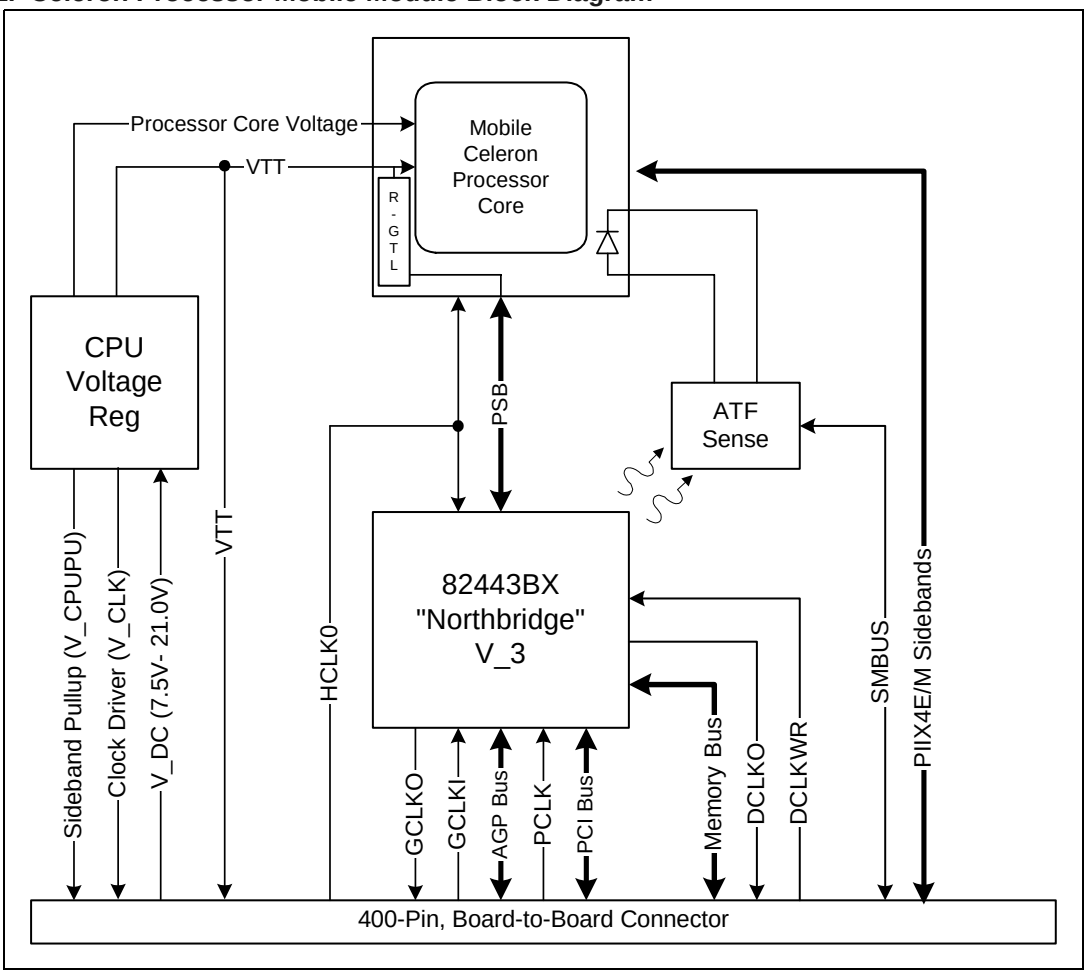
The thermal transfer plates (TTP) on the processor and the 82443BX Host Bridge provide heat dissipation and thermal attach points for the manufacturer's thermal solution.

An on-board voltage regulator converts the system DC voltage to the processor's core and I/O voltage. Isolating the processor voltage requirements allows the system manufacturer to incorporate different processor variants into a single notebook system. Supporting input voltages from 7.5V to 21.0V, the integrated module voltage regulator enables an above 80% peak efficiency and de-couples the processor voltage requirements from the system.

Also incorporated is active thermal feedback (ATF) sensing, compliant to the *ACPI Specification Rev 1.0.*

Figure 1 illustrates the block diagram of the Celeron processor mobile module.

Figure 1. Celeron Processor Mobile Module Block Diagram



3.0 Signal Information

This section provides information on the signal groups for the Celeron processor mobile module. The signals are defined for compatibility with future Intel mobile modules.

3.1 Signal Definitions

Table 1 provides a list of signals by category and the corresponding number of signals in each category. For proper signal termination, please contact your Intel Field Representative for further information.

Table 1. Connector Signal Summary

Signal Group	Number of Pins
Memory	109
AGP	60
PCI	58
Processor/PIIX4E/M Sideband	8
Power Management	7
Clocks	9
Voltage: V_DC	20
Voltage: V_3	16
Voltage: V_3S	9
Voltage: V_5	3
Voltage: VCCAGP	4
Voltage: V_CPUPU	1
Voltage: V_CLK	1
ITP/JTAG	9
Module ID	4
Ground	45
Reserved	37
Total	400

3.1.1 Signal List

The following notations are used to denote signal type:

I	Input pin
O	Output pin
O D	Open-drain output pin requiring a pullup resistor
I D	Open-drain input pin requiring a pullup resistor

I/O D Input/Open-drain output pin requiring a pullup resistor

I/O Bi-directional input/output pin

The signal description also includes the type of buffer used for a particular signal:

GTL+ Open-drain GTL+ interface signal

PCI PCI bus interface signals

AGP AGP bus interface signals

CMOS The CMOS signals, depending on functional group, are 1.5V, 2.5V, or 3.3V.

3.1.2 Memory Signal Description

Table 2 provides descriptions of the memory interface signals.

Table 2. Memory Signals

Name	Type	Voltage	Description
MECC[7:0]	I/O CMOS	V_3	**Memory ECC Data:** These signals carry Memory ECC data during access to DRAM. ***ECC is not supported on the mobile module.***
CSA[5:O]#	O CMOS	V_3	**Chip Select (SDRAM):** These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low.
DQMA[7:0]	O CMOS	V_3	**Input/Output Data Mask (SDRAM):** These pins act as synchronized output enables during a read cycle and as a byte mask during a write cycle.
MAB[9:0]# MAB[10] MAB[12:11]# MAB[13]	O CMOS	V_3	**Memory Address (SDRAM):** This is the row and column address for DRAM. The 82443BX Host Bridge system controller has two identical sets of address lines (MAA and MAB#). The mobile module supports only the MAB set of address lines. For additional addressing features, please refer to the *Intel® 440BX AGPSet: 82443BX Host Bridge/ Controller Datasheet (Order Number: 290633-001).*
MWEA#	O CMOS	V_3	**Memory Write Enable (SDRAM):** MWEA# should be used as the write enable for the memory data bus.
SRASA#	O CMOS	V_3	**SDRAM Row Address Strobe (SDRAM):** When active low, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and pre-charge.
SCASA#	O CMOS	V_3	**SDRAM Column Address Strobe (SDRAM):** When active low, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access.
CKE[5:0]	O CMOS	V_3	**SDRAM Clock Enable (SDRAM):** SDRAM clock enable pin. When these signals are deasserted, SDRAM enters power-down mode. Each row is individually controlled by its own clock enable.
MD[63:0]	O CMOS	V_3	**Memory Data:** These signals are connected to the DRAM data bus. They are not terminated on the mobile module.

3.1.3 AGP Signals

Table 3 provides descriptions of the AGP interface signals.

Table 3. AGP Signal Descriptions

Name	Type	Voltage	Description
GAD[31:]	I/O AGP	V_3	**AGP Address/Data**: The standard AGP address and data lines. This bus functions in the same way as the PCI AD[31:0] bus. The address is driven with FRAME# assertion, and data is driven or received in following clocks.
GC/BE[3:0]#	I/O AGP	V_3	**AGP Command/Byte Enable:** This bus carries the command information during AGP cycles when PIPE# is used. During an AGP write, this bus contains byte enable information. The command is driven with FRAME# assertion and byte enables corresponding to supplied or requested data are driven on the following clocks.
GFRAME#	I/O AGP	V_3	**AGP Frame:** Not used during AGP transactions. Remains deasserted by an internal pullup resistor. Assertion indicates the address phase of a PCI transfer. Negation indicates that the cycle initiator desires one more data transfer.
GDEVSEL#	I/O AGP	V_3	**AGP Device Select**: This signal provides the same function as PCI DEVSEL#. It is not used during AGP transactions. The 82443BX Host Bridge system controller drives this signal when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
GIRDY#	I/O AGP	V_3	**AGP Initiator Ready**: Indicates the AGP-compliant target is ready to provide all write data for the current transaction. Asserted when the initiator is ready for a data transfer.
GTRDY#	I/O AGP	V_3	**AGP Target Ready**: Indicates the AGP-compliant master is ready to provide all write data for the current transaction. Asserted when the target is ready for a data transfer.
GSTOP#	I/O AGP	V_3	**AGP Stop:** This signal provides the same function as PCI STOP#. It is not used during AGP transactions. Asserted by the target to request the master to stop the current transaction.
GREQ#	I AGP	V_3	**AGP Request:** AGP master requests for AGP.
GGNT#	O AGP	V_3	**AGP Grant:** This signal provides the same function as on PCI. Additional information is provided on the ST[2:0] bus. PCI Grant: Permission is given to the master to use PCI.
GPAR	I/O AGP	V_3	**AGP Parity**: A single parity bit is provided over GAD[31:0] and GC/BE[3:0]. This signal is not used during AGP transactions.
PIPE#	I AGP	V_3	**Pipelined Request:** Asserted by the current master to indicate a full width address that is to be queued by the target. The master queues one request each rising clock edge while PIPE# is asserted.
SBA[7:0]	I AGP	V_3	**Sideband Address**: This bus provides an additional conduit to pass address and commands to the 82443BX Host Bridge System Controller from the AGP master.
RBF#	I AGP	V_3	**Read Buffer Full**: RBF# indicates if the master is ready to accept previously requested, low-priority read data.

Table 3. AGP Signal Descriptions

Name	Type	Voltage	Description
ST[2:0]	O AGP	V_3	**Status Bus:** This signal provides information from the arbiter to an AGP Master on what it may do. These bits only have meaning when GGNT is asserted.
ADSTB[B:A]	I/O AGP	V_3	**AD Bus Strobes**: Provide timing for double-clocked data on the GAD bus. The agent providing data drives these signals. These are identical copies of each other.
SBSTB	I/O AGP	V_3	**Sideband Strobe**: Provides timing for a sideband bus. The SBA[7:0] (AGP master) drives the sideband strobe.

3.1.4 PCI Signals

Table 4 provides descriptions of the PCI signals.

Table 4. PCI Signal Description

Name	Type	Voltage	Description
AD[31:0]	I/O PCI	V_3	**Address/Data:** The standard PCI address and data lines. The address is driven with FRAME# assertion, and data is driven or received in the following clocks.
C/BE[3:0]	I/O PCI	V_3	**Command/Byte Enable:** The command is driven with FRAME# assertion, and byte enables corresponding to supplied or requested data are driven on the following clocks.
FRAME#	I/O PCI	V_3	**Frame:** Assertion indicates the address phase of a PCI transfer. Negation indicates that the cycle initiator desires one more data transfer.
DEVSEL#	I/O PCI	V_3	**Device Select:** The 82443BX Host Bridge drives this signal when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O PCI	V_3	**Initiator Ready:** This signal is asserted when the initiator is ready for data transfer.
TRDY#	I/O PCI	V_3	**Target Ready:** The signal is asserted when the target is ready for a data transfer.
STOP#	I/O PCI	V_3	**Stop:** Asserted by the target to request the master to stop the current transaction.
PLOCK#	I/O PCI	V_3	**Lock:** Indicates an exclusive bus operation and may require multiple transactions to complete. When LOCK# is asserted, nonexclusive transactions may proceed. The 82443BX supports lock for CPU initiated cycles only. PCI initiated locked cycles are not supported.
REQ[4:0]#	I PCI	V_3	**PCI Request:** PCI master requests for PCI.
GNT[4:0]#	O PCI	V_3	**PCI Grant:** Permission is given to the master to use PCI.
PHOLD#	I PCI	V_3	**PCI Hold:** This signal comes from the expansion bridge. It is the bridge request for PCI. The 82443BX Host Bridge will drain the DRAM write buffers, drain the processor-to-PCI posting buffers, and acquire the host bus before granting the request via PHLDA#. This process ensures that GAT timing is met for ISA masters. The PHOLD# protocol has been modified to include support for passive release.
PHLDA#	O PCI	V_3	**PCI Hold Acknowledge:** This signal is driven by the 82443BX Host Bridge to grant PCI to the expansion bridge. The PHLDA# protocol has been modified to include support for passive release.
PAR	I/O PCI	V_3	**Parity:** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.

Table 4. PCI Signal Description

Name	Type	Voltage	Description
SERR#	I/O PCI	V_3	**System Error:** The 82443BX asserts this signal to indicate an error condition. For further information, refer to the *Intel® 440BX AGPSet: 82443BX Host Bridge/Controller Datasheet (Order Number: 290633-001)*.
CLKRUN#	I/O D PCI	V_3	**Clock Run:** An open-drain output and input. The 82443BX Host Bridge requests the central resource, PIIX4E/M, to start or maintain the PCI clock by asserting CLKRUN#. The 82443BX Host Bridge tri-states CLKRUN# upon deassertion of Reset (since CLK is running upon deassertion of Reset).
PCI_RST#	I CMOS	V_3	**Reset:** When asserted, this signal asynchronously resets the 82443BX Host Bridge. The PCI signals also tri-state, compliant with *PCI Rev 2.1 Specifications*.

3.1.5 Processor and PIIX4E/M Sideband Signals

Table 5 provides descriptions of the processor and PIIX4E/M sideband signals.

Table 5. Processor and PIIX4E/M Sideband Signal Description

Name	Type	Voltage	Description
FERR#	O D CMOS	V_CPUPU	**Numeric Co-processor Error:** This pin functions as an FERR# signal supporting co-processor errors. This signal is tied to the co-processor error signal on the processor, and it is pulled active low by the processor to the PIIX4E/M.
IGNNE#	I D CMOS	V_CPUPU	**Ignore Error:** This open-drain signal is connected to the Ignore Error pin on the processor, and it is driven by the PIIX4E/M.
INT#	I D CMOS	V_CPUPU	**Initialization:** INIT# is asserted by the PIIX4E/M to the processor for system initialization. This signal is an open-drain.
INTR	I D CMOS	V_CPUPU	**Processor Interrupt:** INTR is driven by the PIIX4E/M to signal the processor that an interrupt request is pending and needs to be serviced. This signal is an open-drain.
NMI	I D CMOS	V_CPUPU	**Non-maskable Interrupt:** NMI is used to force a non-maskable interrupt to the processor. The PIIX4E/M ISA bridge generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. This signal is an open-drain.
A20M#	I D CMOS	V_CPUPU	**Address Bit 20 Mask:** When enabled, this open-drain signal causes the processor to emulate the address wraparound at 1 MB, which occurs on the Intel 8086 processor.
SMI#	I D CMOS	V_CPUPU	**System Management Interrupt:** SMI# is an active low synchronous output from the PIIX4E/M that is asserted in response to one of many enabled hardware or software events. The SMI# open-drain signal can be an asynchronous input to the processor. However, in this chipset SMI# is synchronous to PCLK.
STPCLK#	I D CMOS	V_CPUPU	**Stop Clock:** STPCLK# is an active-low, synchronous open-drain output from the PIIX4E/M that is asserted in response to one of many hardware or software events. STPCLK# connects directly to the processor, and it is synchronous to PCICLK. When the processor samples STPCLK# asserted, it responds by entering a low-power state (Quick Start). The processor will only exit this mode when this signal is deasserted.

NOTE: See Table 8 for V_CPUPU definition.

3.1.6 Power Management Signals

Table 6 provides descriptions of the power management signals. The SM_CLK and SM_DATA signals refer to the two-wire serial SMBus interface. Although this interface is currently used solely for the digital thermal sensor, the SMBus contains reserved serial addresses for future use.

Table 6. Power Management Signal Descriptions

Name	Type	Voltage	Description
SUS_STAT1#	I CMOS	V_3ALWAYS	**Suspend Status:** This signal connects to the SUS_STAT1# output of PIIX4E/M. It provides information on host clock status, and it is asserted during all suspend states.
VR_ON	I CMOS	V_3	**VR_ON:** Voltage regulator ON. This 3.3-V (5.0-V tolerant) signal controls the operation of the voltage regulator. VR_ON should be generated as a function of the PIIX4E/M SUSB# signal, which is used for controlling the “Suspend State B” voltage planes. This signal should be driven by a digital signal with a rise/fall time of less than or equal to 1 µS. ($V_{IL,max}$ =0.4V, $V_{IH,min}$ =3.0V.)
VR_PWRGD	O	V_3	**VR_PWRGD:** This signal is driven high by the mobile module to indicate that the voltage regulator is stable. The signal is pulled low using a 100-K resistor when inactive. It can be used in some combination to generate the system PWRGOOD signal.
BXPWROK	I CMOS	V_3	**Power OK to BX:** This signal must go active at least 1 mS after the V_3 power rail is stable, and 1 mS prior to deassertion of PCIRST#.
SM_CLK	I/O D CMOS	V_3	**Serial Clock:** This clock signal is used on the SMBus interface to the digital thermal sensor.
SM_DATA	I/O D CMOS	V_3	**Serial Data:** Open-drain data signal on the SMBus interface to the digital thermal sensor.
ATF_INT#	O D CMOS	V_3	**ATF Interrupt:** This signal is an open-drain output signal of the digital thermal sensor.

NOTE: V_3ALWAYS is a 3.3-V supply and is generated whenever V_DC is available and supplied to the PIIX4E/M resume well.

3.1.7 Clock Signals

Table 7 provides descriptions of the clock signals.

Table 7. Clock Signal Definitions

Name	Type	Voltage	Description
PCLK	I PCI	V_3	**PCI Clock In:** PCLK, an input to the mobile module, is one of the system's PCI clocks. This clock is used by all of the 82443BX Host Bridge logic in the PCI clock domain. This clock is stopped when the PIIX4E/M PCI_STP# signal is asserted and/or during all suspend states.
HCLK0	I CMOS	V_CLK	**Host Clock In:** This clock is input to the mobile module from the CK100-M/CK100-SM clock source. The processor and the 82443BX Host Bridge system controller use HCLK0. This clock is stopped when the PIIX4E/M CPU_STP# signal is asserted and/or during all suspend states.
HCLK1	I CMOS	V_CLK	**Host Clock In:** This clock is an input to the mobile module from the CK100-M/CK100-SM clock source. ***This signal is not implemented on the mobile module***.
DCLK0	O CMOS	V_3	**SDRAM Clock Out:** A 66-MHz SDRAM clock reference generated internally by the 82443BX Host Bridge system controller onboard PLL. It feeds an external buffer that produces multiple copies for the SO-DIMMs.
DCLKRD	I CMOS	V_3	**SDRAM Read Clock:** Feedback reference from the SDRAM clock buffer. The 82443BX Host Bridge System Controller uses this clock when reading data from the SDRAM array. ***This signal is not implemented on the mobile module*** .
DCLKWR	I CMOS	V_3	**SDRAM Write Clock:** Feedback reference from the SDRAM clock buffer. The 82443BX Host Bridge system controller uses this clock when writing data to the SDRAM array.
GCLKIN	I CMOS	V_3	**AGP Clock In:** The GCLKIN input is a feedback reference from the GCLKO signal.
GCLKO	O CMOS	V_3	**AGP Clock Out:** This signal is generated by the 82443BX Host Bridge system controller onboard the PLL from the HCLK0 host clock reference. The frequency of GCLKO is 66 MHz. The GCLKO output is used to feed both the PLL reference input pins on the 82443BX Host Bridge system controller and the AGP device. The board layout must maintain complete symmetry on loading and trace geometry to minimize AGP clock skew.
FQS	O CMOS	V_3S	**Frequency Select:** This output indicates the desired host clock frequency for the mobile module.

3.1.8 Voltage Signals

Table 8 provides descriptions of the voltage signals.

Table 8. Voltage Descriptions

Name	Type	Number of pins	Description
V_DC	I	20	**DC Input:** 7.5V ~ 21.0V
V_3S	I	9	**SUSB# controlled 3.3V:** A power managed 3.3-V supply. An output of the voltage regulator on the system electronics. This rail is off during STR, STD, and Soff.
V_5	I	3	**SUSC# controlled 5.0V:** A power managed 5.0-V supply. An output of the voltage regulator on the system electronics. This rail is off during STD and Soff.
V_3	I	16	**SUSC# controlled 3.3V:** A power managed 3.3-V supply. An output of the voltage regulator on the system electronics. This rail is off during STD and Soff.
VCCAGP	I	4	**AGP I/O Voltage**: This voltage rail is not implemented on the module and is defined for upgrade purposes only. Intel recommends that this voltage rail be connected to V_3 on the system electronics.
V_CPUPU	O	4	**Processor I/O Ring:** Driven by the mobile module to power processor interface signals such as the PIIX4E/M open-drain pullups for the processor/PIIX4E/M sideband signals. V_CPUPU is tied to 1.5V for the mobile module.
V_CLK	O	1	**Processor Clock Rail:** Driven by the mobile module to power CK100-M VDDCPU rail.

3.1.9 ITP and JTAG Pins

Table 9 provides descriptions of the ITP and JTAG signals, which the system manufacturer can use to implement a JTAG chain and an ITP port if desired.

Table 9. ITP and JTAG Pins

Name	Type	Voltage	Description
TDO	O	V_CPUPU	**JTAG Test Data Out:** Serial output port. TAP instructions and data are shifted out of the processor from this port.
TDI	I	VTT	**JTAG Test Data In:** Serial input port. TAP instructions and data are shifted into the processor from this port.
TMS	I	VTT	**JTAG Test Mode Select:** Controls the TAP controller change sequence.
TCLK	I	VTT	**JTAG Test Clock:** Testability clock for clocking the JTAG boundary scan sequence.
TRST#	I	VTT	**JTAG Test Reset:** Asynchronously resets the TAP controller in the processor.
FS_PREQ#			**Debug Mode Request:** Driven by the ITP – makes request to enter debug mode.
FS_PRDY#	O	VTT	**Debug Mode Ready:** Driven by the processor – informs the ITP that the processor is in debug mode.
FS_RESET#	O	VTT	**Processor Reset:** Processor reset status to the ITP.
VTT	O	VTT	**GTL+ Termination Voltage:** Used by the POWERON pin on the ITP debug port to determine when target system is on. POWERON pin is pulled up using a 1-KΩ resistor to VTT. Other ITP signals might use this power rail for pullup.

NOTE: FS_RESET# and FS_PRDY# are pulled up to VTT inside the mobile processor core.

3.1.10 Miscellaneous Pins

Table 10 provides descriptions of the miscellaneous signal pins.

Table 10. Miscellaneous Pins

Name	Type	Number	Description
Module ID[3:0]	O CMOS	4	**Module Revision ID**: These pins track the revision level of the mobile module. A 100-K pullup resistor to V_3S must be placed on the system electronics for these signals. See Section 8.0 for more detail.
Ground	I	45	Ground
Reserved	RSVD	33	Unallocated Reserved pins. ***All Reserved pins must not be connected.***

3.2 Connector Pin Assignments

Table 11 lists the signals for each pin of the connector to the system electronics. Refer to Section 3.3 for the pin assignments.

Table 11. Connector Pin Assignment

Pin Number	Row A	Row B	Row C	Row D	Row E
1	SBA5	ADSTBB	GND	GAD31	SBA7
2	GAD25	GAD24	SBA6	SBA4	SBA0
3	GAD30	GAD29	GAD26	GAD27	GND
4	GND	VCCAGP	GAD4	GAD6	GDA8
5	RBF#	GAD1	GAD3	GAD5	GC/BE0#
6	BXPWROK	RESERVED	GAD2	ADSTBA	GND
7	MD0	MD1	V_3	CLKRUN#	GAD7
8	MD2	MD33	GND	MD32	MD34
9	MD36	MD4	MD3	MD35	MD34
10	MD7	MD38	MD37	MD6	MD5
11	MD41	MD42	MD40	MD39	MD8
12	MD43	MD11	GND	MD10	MD9
13	MD14	MD45	MD44	MD13	MD12
14	MECC4	MECC0	ND15	ND47	ND46
15	SCASA#	MWEA#	MECC5	RESERVED	GND
16	GND	MID1	DQMA0	DQMA1	RESERVED
17	V_3	DQMA4	MID0	DQMA5	CSA#
18	CSA1#	CSA2#	CSA4#	CSA3#	GND
19	SRASA#	CSA5#	MAB0#	MAB1#	RESERVED
20	RESERVED	RESERVED	MAB2#	RESERVED	MAB3#
21	RESERVED	MAB4#	GND	RESERVED	MAB6#
22	RESERVED	RESERVED	MAB5#	RESERVED	MAB7#
23	MAB8#	RESERVED	RESERVED	MSB9#	MAB10
24	RESERVED	MAB11#	MAB12#	RESERVED	DCLK0
25	MAB13	V_3	GND	CKE0	DCLKRD
26	CKE1	MID2	CKE3	CE4	GND
27	CKE5	CKE2	MID3	RESERVED	RESERVED#
28	RESERVED	RESERVED	DQMA2	DCLKWR	GND
29	GND	VTT	RESERVED	FS_PREQ#	DQMA3
30	FS_RESET#	V_3	MD26	GND	MD25
31	FS_PRDY#	GND	MD58	MD57	MD60
32	RESERVED	SMCLK	TDO	TCLK	FERR#
33	RESERVED	SMDAT	TDI	TMS	IGNNE#

Table 11. Connector Pin Assignment

Pin Number	Row A	Row B	Row C	Row D	Row E
34	RESERVED	FQS	RESERVED	TRST#	ATF_INT#
35	RESERVED	V_5	V_3S	V_3S	V_3S
36	V_CPUPU	V_5	V_3S	V_3S	V_3S
37	V_CLK	V_5	V_3S	V_3S	V_3S
38	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
39	V_DC	V_DC	V_DC	V_DC	V_DC
40	V_DC	V_DC	V_DC	V_DC	V_DC

Pin Number	Row F	Row G	Row H	Row J	Row K
1	GREQ#	GND	PIP#	SBA3	GND
2	ST0	ST1	SBA1	SBSTB	GCLKI
3	GGNT#	ST2	SBA2	GND	CGLK0
4	GAD13	GSTOP#	GAD16	GAD20	GAD23
5	GAD12	GPAR	GAD18	GAD17	GC/BE3#
6	GAD10	GAD15	GFRAME#	GND	GAD22
7	GAD11	GC/BE1#	GTRDY#	GC/BE2#	GAD21
8	GAD9	GAD14	GDEVESEL#	GIRDY#	GAD19
9	GND	VCCAGP	GND	VCCAGP	GAD28
10	AD0	AD4	AD2	AD3	AD1
11	GND	C/BE0#	AD6	GND	AD5
12	VCCAGP	AD10	AD7	AD8	AD9
13	MECC1	AD13	GND	AD12	AD11
14	SERR#	PAR	AD15	C/BE1#	AD14
15	AD16	TRDY#	STOP#	DEVSEL#	PLOCK#
16	AD19	GND	AD17	GND	AD18
17	AD23	AD30	AD24	C/BE2#	AD21
18	AD27	AD22	C/BE3#	AD26	PCLK
19	PCI_RST#	GND	AD20	AD28	GND
20	RESERVED	PHOLD#	AD31	AD29	AD25
21	IRDY#	FRAME#	GND	REQ1#	REQ0#
22	GND	GNT2#	REQ2#	REQ3#	GNT3#
23	GNT1#	GNT4#	GNT0#	REQ4#	GND
24	GND	PHLDA#	GND	V_3	MD59
25	DQMA6	MECC7	MD50	MD51	MD54
26	MECC2	MD48	MD18	MD52	MD24

27	DQMA7	MD16	MD19	GND	MD23
28	MECC6	MD17	MD21	MD53	MD55
29	MECC3	MD49	MD20	MD22	MD56
30	MD27	MD28	GND	MD62	MD63
31	GND	MD29	MD61	MD30	MD31
32	DMI#	INTR	VR_ON	GND	GND
33	NMI	SUS_STAT1#	VR_PWRGD	GND	HCLK0
34	A20M#	STPCLK#	INIT#	GND	GND
35	V_3	V_3	V_3	GND	HCLK1
36	V_3	V_3	V_3	GND	GND
37	V_3	V_3	V_3	V_3	V_3
38	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
39	V_DC	V_DC	V_DC	V_DC	V_DC
40	V_DC	V_DC	V_DC	V_DC	V_DC

3.3 Pin and Pad Assignments

The 400-pin MMC-2 connector has a 1.27-mm pitch and a BGA-style surface mount. Refer to Section 6.1.3 for size information. Figure 2 shows the MMC-2 connector pad assignments.

Figure 2. MMC-2 Connector Pad Footprint

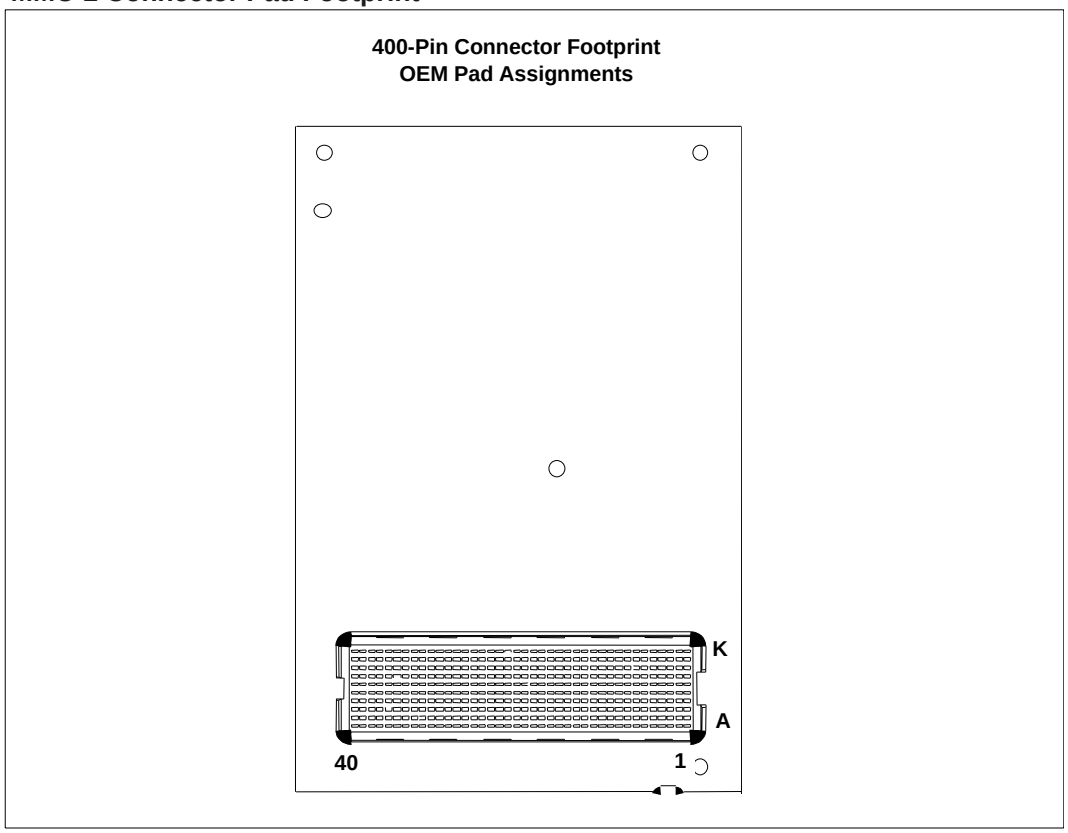


Table 12 summarizes some of the connector key specifications.

Table 12. Connector Specifications

Parameter	Condition	Specification
Material	Contact	Copper Alloy
	Housing	Thermo Plastic Molded Compound: LCP
Electrical	Current	0.5A
	Voltage	50 VAC
	Insulation Resistance	100 MΩ
	Termination Resistance	20-mΩ maximum at 20 mV open circuit with 10 mA
	Capacitance	5-pF maximum per contact
Mechanical	Mating Cycles	50 cycles
	Connector Mating Force	50 lbs (22.7 kg) maximum
	Contact Unmating Force	30 lbs (13.6 kg) maximum

4.0 Functional Description

4.1 Celeron Processor Mobile Module

The Celeron processor mobile module offers processor speeds of 700 MHz, 650 MHz, 600 MHz, 550 MHz, 500 MHz, and 450 MHz with a 100-MHz PSB.

4.2 L2 Cache

The on-die L2 cache is 128K, four-way set associative, and runs at the speed of the processor core.

4.3 The 82443BX Host Bridge System Controller

Intel's 82443BX Host Bridge system controller is a highly integrated device that combines the bus controller, the DRAM controller, and the PCI bus controller into one component. The 82443BX Host Bridge has multiple power management features designed specifically for notebook systems such as:

- CLKRUN#, a feature that enables controlling of the PCI clock on or off.
- The 82443BX Host Bridge suspend modes, which include Suspend-To-RAM (STR), Suspend-To-Disk (STD), and Power-On-Suspend (POS).
- System Management RAM (SMRAM) power management modes, which include Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM). C_SMRAM is the traditional SMRAM feature implemented in all Intel PCI chipsets.
- E_SMRAM is a new feature that supports write-back cacheable SMRAM space up to 1 MB. To minimize power consumption while the system is idle, the internal 82443BX Host Bridge clock is turned off (gated off) when there is no processor and PCI activity. This is accomplished by setting the G_CLK enable bit in the power management register in the 82443BX through the system BIOS.

4.3.1 Memory Organization

The memory interface of the 82443BX Host Bridge is available at the connector. This allows for the following:

- One set of memory control signals, sufficient to support up to three SO-DIMM sockets and six banks of SDRAM at 100 MHz.
- One CKE signal for each bank.

Memory features **not** supported by the 82443BX Host Bridge system controller standard MMC-2 mode are:

- Eight banks of memory
- 256-Mb memory devices
- Second set of memory address lines (MAA[13:0])

- Extended Data Out (EDO) DRAM
- 66-MHz memory bus

The mobile module's clocking architecture supports the use of SDRAM. The clocking mode for 100-MHz SDRAM memory configurations allows all host and SDRAM clocks to be generated from the same clocking source on the system electronics. For complete details about memory device support, organization, size, and addressing when using SDRAM memory and trace length guidelines, refer to the *Intel® Pentium® III Processor Mobile Module System Electronics 100-MHz Layout Guidelines Revision. 1.0* (OR-1780).

4.3.2 Reset Strap Options

Several strap options on the memory address bus define the behavior of the mobile module after reset. Other straps are allowed to override the default settings. Table 13 shows the various straps and their implementation.

Table 13. Configuration Straps for the 82443BX Host Bridge System Controller

Signal	Function	Module Default Setting	Optional Override on System Electronics
MAB[12]#	Host Frequency Select	Strapped high on the module for 100 MHz	None
MAB[11]#	In Order Queue Depth	No strap, maximum queue depth is set at 8	None
MAB[10]#	Quick Start Select	Strapped high on the module for Quick Start mode	None
MAB[9]#	AGP Disable	No strap, AGP is enabled	Strap high to disable AGP
MAB[7]#	MM Configuration	No strap, standard MMC-2 mode	None
MAB[6]#	Host Bus Buffer mode select	Strapped high on the module for mobile PSB buffers	None

4.3.3 PCI Interface

The PCI interface of the 82443BX Host Bridge is available at the MMC-2 connector. The 82443BX Host Bridge supports the PCI Clockrun protocol for PCI bus power management. In this protocol, PCI devices assert the CLKRUN# open-drain signal when they require the use of the PCI interface. Refer to the *PCI Mobile Design Guide* for complete details on the PCI Clockrun protocol.

The 82443BX Host Bridge is responsible for arbitrating the PCI bus. The 82443BX Host Bridge can support up to five PCI bus masters. There are five PCI Request/Grant pairs, REQ[4:0]# and GNT[4:0]#, available on the connector to the system electronics.

Note: The PCI interface on the MMC-2 connector is 3.3V only. PCI devices that are 5.0V are not supported.

The 82443BX Host Bridge system controller is compliant with the *PCI 2.1 Specification*, which improves the worst case PCI bus access latency from earlier PCI specifications. The 82443BX Host Bridge supports only Mechanism #1 for accessing PCI configuration space. This implies that signals AD[31:11] are available for PCI IDSEL signals. However, since the 82443BX Host Bridge

is always device #0, AD11 will never be asserted during PCI configuration cycles as an IDSEL. The 82443BX reserves AD12 for the AGPbus. Thus, AD13 is the first available address line usable as an IDSEL. Intel recommends that AD18 be used by the PIIX4E/M.

4.3.4 AGP Interface

The 82443BX Host Bridge system controller is compliant with the *AGP Interface Specification Revision 2.0*, which supports an asynchronous AGP interface coupling to the 82443BX core frequency. The AGP interface can achieve real data throughput in excess of 500 MB per second using an AGP 2X graphics device. Actual bandwidth may vary depending on specific hardware and software implementations.

4.4 Power Management

4.4.1 Clock Control Architecture

The clock control architecture has been optimized for notebook designs. The clock control architecture consists of seven different clock states: Normal, Stop Grant, Auto Halt, Quick Start, HALT/Grant Snoop, Sleep, and Deep Sleep states. The Auto Halt state provides a low-power clock state that can be controlled through the software execution of the HLT instruction. The Quick Start state provides a very low-power, low-exit latency clock state that can be used for hardware controlled "idle" states. The Deep Sleep state provides an extremely low-power state that can be used for Power-On-Suspend states, which is an alternative to shutting off the processor's power. The exit latency of the Deep Sleep state is 30 µS. The Stop Grant state and the Quick Start clock state are mutually exclusive. For example, a strapping option on signal A15# chooses which state is entered when the STPCLK# signal is asserted. Strapping the A15# signal to ground at Reset enables the Quick Start state. Otherwise, asserting the STPCLK# signal puts the processor into the Stop Grant state.

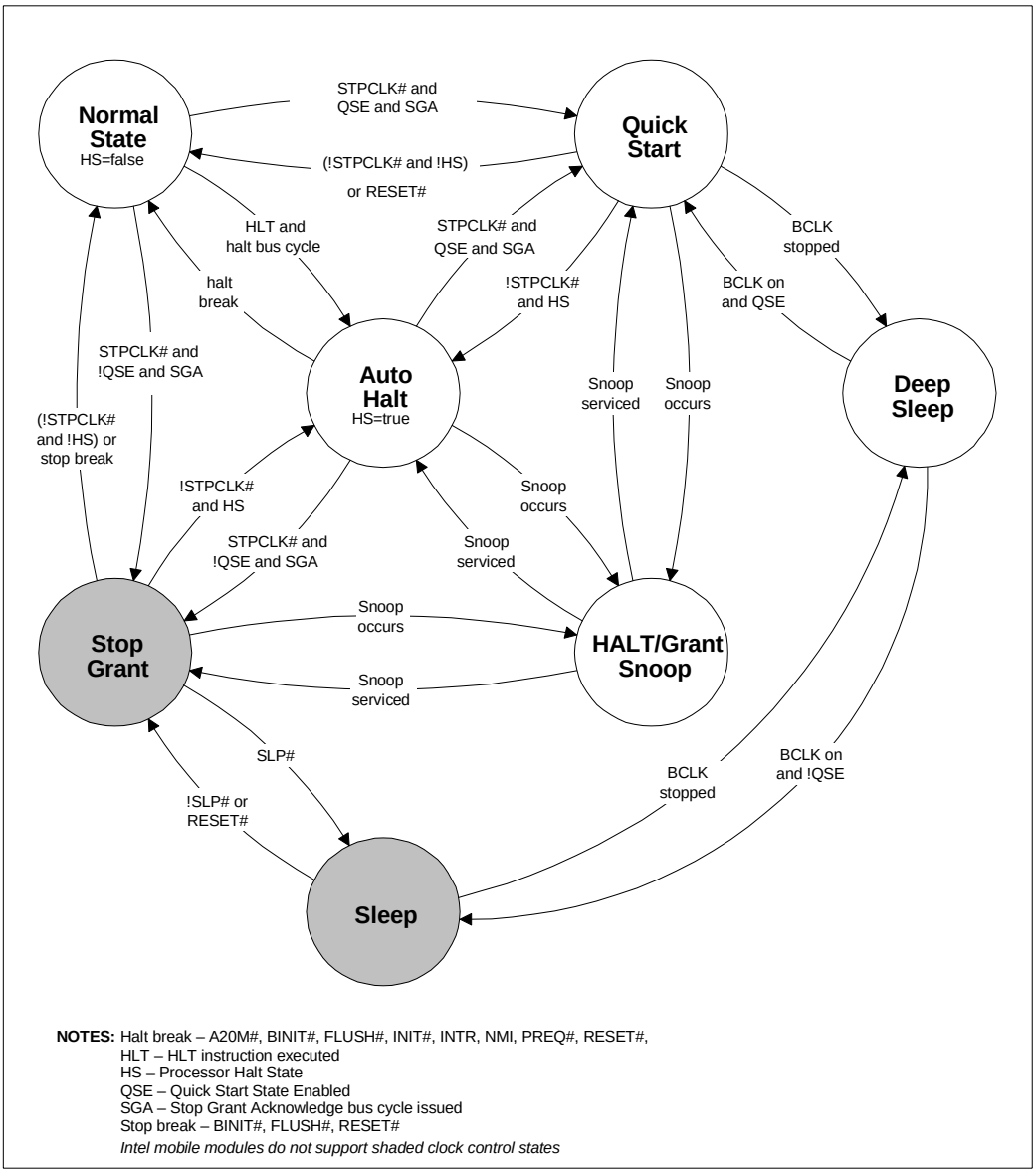
Figure 3 illustrates the clock control architecture. Performing state transitions not shown in Figure 3 are neither recommended nor supported.

Table 14. Clock State Characteristics

Clock State	Exit Latency	Snooping	System Uses	Notes
Normal	N/A	Yes	Normal program execution	Note 4
Auto Halt	Approximately 10 bus clocks	Yes	Software controlled entry idle mode	Note 2
Stop Grant	10 bus clocks	Yes	Hardware controlled entry/exit mobile throttling	Note 1
Quick Start	Through Snoop, to HALT/Grant Snoop state: immediate Through STPCLK#, to Normal state: 10 bus clocks	Yes	Hardware controlled entry/exit mobile throttling	Note 2
HALT/Grant Snoop	A few bus clocks after the end of snoop activity	Yes	Supports snooping in the low-power states	
Sleep	To Stop Grant state 10 bus clocks	No	Hardware controlled entry/exit desktop idle mode support	Note 1
Deep Sleep	30 µS	No	Hardware controlled entry/exit mobile POS support	Note 3

NOTES:
1. Intel mobile modules do not support the Sleep and Stop Grant clock states.
2. These values are not 100% tested and are specified at 50°C by design and characterization.
3. This value is not 100% tested and is specified at 35°C by design and characterization.
4. Specification marked N/A are not available.

Figure 3. Clock Control States



NOTES: Halt break – A20M#, BINIT#, FLUSH#, INIT#, INTR, NMI, PREQ#, RESET#,
HLT – HLT instruction executed
HS – Processor Halt State
QSE – Quick Start State Enabled
SGA – Stop Grant Acknowledge bus cycle issued
Stop break – BINIT#, FLUSH#, RESET#
Intel mobile modules do not support shaded clock control states

4.4.1.1 Normal State

The normal operating mode where the processor's core clock is running and the processor is actively executing instructions.

4.4.1.2 Auto Halt State

This is a low-power mode entered by the processor through the execution of the HLT instruction. The power level of this mode is similar to the Stop Grant state. A transition to the Normal state is made by a halt break event (one of the following signals going active: NMI, INTR, BINIT#, INIT#, RESET#, FLUSH#, or SMI#).

Asserting the STPCLK# signal while in the Auto Halt state will cause the processor to transition to the Stop Grant state or the Quick Start state, where a Stop Grant Acknowledge bus cycle will be issued. Deasserting STPCLK# will cause the processor to return to the Auto Halt state without issuing a new Halt bus cycle.

The SMI# (System Management Interrupt) is recognized in the Auto Halt state. The return from the SMI handler can be to either the Normal state or the Auto Halt state. See the *Intel® Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information. No Halt bus cycle is issued when returning to the Auto Halt state from System Management Mode (SMM).

The FLUSH# signal is serviced in the Auto Halt state. After flushing the on-chip, the processor will return to the Auto Halt state without issuing a Halt bus cycle. Transitions in the A20M# and PREQ# signals are recognized while in the Auto Halt state.

4.4.1.3 Stop Grant State

The Celeron processor mobile module does not support the Stop Grant state.

The processor enters this mode with the assertion of the STPCLK# signal when it is configured for Stop Grant state (via the A15# strapping option). The processor is still able to respond to snoop requests and latch interrupts. Latched interrupts will be serviced when the processor returns to the Normal state. Only one occurrence of each interrupt event will be latched. A transition back to the Normal state can be made by the deassertion of the STPCLK# signal, or the occurrence of a stop break event (a BINIT#, FLUSH#, or RESET# assertion).

The processor will return to the Stop Grant state after the completion of a BINIT# bus initialization unless STPCLK# has been deasserted. RESET# assertion will cause the processor to immediately initialize itself. However, the processor will stay in the Stop Grant state after initialization until STPCLK# is deasserted. If the FLUSH# signal is asserted, the processor will flush the on-chip caches and return to the Stop Grant state. A transition to the Sleep state can be made by the assertion of the SLP# signal.

While in the Stop Grant state, assertions of SMI#, INIT#, INTR, and NMI (or LINT[1:0]) will be latched by the processor. These latched events will not be serviced until the processor returns to the Normal state. Only one of each event will be recognized upon return to the Normal state.

4.4.1.4 Quick Start State

This is a mode entered by the processor with the assertion of the STPCLK# signal when it is configured for the Quick Start state (via the A15# strapping option). In the Quick Start state the processor is only capable of acting on snoop transactions generated by the PSB priority device. Because of its snooping behavior, Quick Start can only be used in single processor configurations.

A transition to the Deep Sleep state can be made by stopping the clock input to the processor. A transition back to the Normal state (from the Quick Start state) is made only if the STPCLK# signal is deasserted.

While in this state the processor is limited in its ability to respond to input. It is incapable of latching any interrupts, servicing snoop transactions from symmetric bus masters, or responding to FLUSH# and BINIT# assertions. In the Quick Start state, the processor will not respond properly to any input signal other than STPCLK#, RESET#, or BPRI#. If any other input signal changes, then the behavior of the processor will be unpredictable. No serial interrupt messages may begin or be in progress while the processor is in the Quick Start state.

RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Quick Start state after initialization until STPCLK# is deasserted.

4.4.1.5 HALT/Grant Snoop State

The processor will respond to snoop transactions on the PSB while in the Auto Halt, Stop Grant, or Quick Start state. When a snoop transaction is presented on the system bus, the processor will enter the HALT/Grant Snoop state. The processor will remain in this state until the snoop has been serviced and the PSB is quiet. After the snoop has been serviced, the processor will return to its previous state. If the HALT/Grant Snoop state is entered from the Quick Start state, then the input signal restrictions of the Quick Start state still apply in the HALT/Grant Snoop state (except for those signal transitions that are required to perform the snoop).

4.4.1.6 Sleep State

Intel mobile modules do not support the Sleep state.

The Sleep state is a very low power state in which the processor maintains its context and the phase locked loop (PLL) maintains phase lock. The Sleep state can only be entered from the Stop Grant state. After entering the Stop Grant state the SLP# signal can be asserted, causing the processor to enter the Sleep state. The SLP# signal is not recognized in the Normal state or the Auto Halt state.

The processor can be reset by the RESET# signal while in the Sleep state. If RESET# is driven active while the processor is in the Sleep state, then SLP# and STPCLK# must immediately be driven inactive to ensure that the processor correctly initializes itself.

Input signals (other than RESET#) may not change while the processor is in or transitioning into or out of the Sleep state. Input signal changes at these times will cause unpredictable behavior. Thus, the processor is incapable of snooping or latching any events in the Sleep state.

While in the Sleep state the processor can enter its lowest power state, the Deep Sleep state. Removing the processor's input clock puts the processor in the Deep Sleep state. PICCLK may be removed in the Sleep state.

4.4.1.7 Deep Sleep State

The Deep Sleep state is the lowest power mode that the processor can enter while maintaining its context. Stopping the BCLK input to the processor enters the Deep Sleep state— while the processor is in the Sleep state or the Quick Start state. For proper operation, the BCLK input should be stopped in the low state.

The processor will return to the Sleep state or the Quick Start state from the Deep Sleep state when the BCLK input is restarted. Due to the PLL lock latency, there is a 30.0-µs delay after the clocks have started before this state transition happens. PICCLK may be removed in the Deep Sleep state. PICCLK should be designed to turn on when BCLK turns on when transitioning out of the Deep Sleep state.

The input signal restrictions for the Deep Sleep state are the same as for the Sleep state, except that RESET# assertion will result in unpredictable behavior.

4.5 Power Consumption in Power Management Modes

The power data is broken down into each power rail. Each power rail is supplied to the module through the MMC-2 connector. The total power values are based on typical power consumption. The data is captured at T_{amb} = 25°C, T_{TTP} = 25 °C, and V_DC = 18.0V.

Note: The values in Table 15 and Table 16 below are not 100% tested and have been characterized by design.

Table 15, Table 16, and Table 17 provide the module power consumption values in various power management modes. Because mobile modules with the same frequencies may have different printed circuit board (PCB) revisions, refer to the product tracking code (PTC) lists before each table below to match the correct power consumption information with the correct mobile module.

Table 15 applies to mobile modules with the following PTCs.

- PMN50001001AA
- PMN45001001AA

Table 15. Power Consumption Values I

State	V_DC	V_5	V_3	V_3S	Total Power
Auto Halt	2.19W	0.08W	2.27W	0.57W	4.17W
Quick Start	1.77W	0.08W	2.04W	0.62W	3.43W
Deep Sleep	1.29W	0.08W	0.24W	0.45W	1.35W
STR	0.04W	0.01W	0.01W	0.00W	0.05W

NOTE: These power values should be used as power supply guidelines for power management modes. They have some guardband added for design margin. Therefore, the total power does not necessarily add up as the sum of each power rail. "Total Power" is the sum of " the individual "raw" power requirements with guardband added.

Table 16 applies to mobile modules with the following PTCs.

- PMN65001201AB
- PMN60001201AB
- PMN55001201AB
- PMN50001201AC
- PMN45001201AC
- PMN65001101AA
- PMN60001101AA
- PMN55001101AA
- PMN50001101AB
- PMN45001101AB

Table 16. Power Consumption Values II

State	V_DC	V_5	V_3	V_3S	Total Power
Auto Halt	2.56W	0.06W	2.31W	0.03W	4.93W
Quick Start	2.10W	0.06W	2.00W	0.03W	4.13W
Deep Sleep	1.64W	0.05W	0.26W	0.04W	1.96W
STR	0.03W	0.01W	0.02W	0.00W	0.05W

NOTE: These power values should be used as power supply guidelines for power management modes. They have some guardband added for design margin. Therefore, the total power does not necessarily add up as the sum of each power rail. "Total Power" is the sum of the individual "raw" power requirements with guardband added.

Table 17 applies to mobile modules with the following PTCs.

- PMN70001201AA

Table 17. Power Consumption Values II

State	V_DC	V_5	V_3	V_3S	Total Power
Auto Halt	2.81W	0.18W	2.23W	0.02W	5.05W
Quick Start	2.35W	0.18W	1.97W	0.04W	4.37W
Deep Sleep	1.46W	0.22W	0.25W	0.04W	1.88W
STR	0.05W	0.00W	0.01W	0.00W	0.06W

NOTE: These power values should be used as power supply guidelines for power management modes. They have some guardband added for design margin. Therefore, the total power does not necessarily add up as the sum of each power rail. "Total Power" is the sum of the individual "raw" power requirements with guardband added.

5.0 Electrical Specifications

The following section provides the electrical specifications for the Celeron processor mobile module.

5.1 System Bus Clock Signal Quality Specifications

5.1.1 BCLK DC Specifications

Table 18. BCLK DC Specifications

Symbol	Parameter	Min	Max	Unit
$V_{IL,BCLK}$	Input Low Voltage, BCLK	- 0.3	0.5	V
$V_{IH,BCLK}$	Input High Voltage, BCLK	2.0	2.625	V

NOTE: $V_{ILX,min}$ and $V_{IH,max}$ only apply when BCLK is stopped. BCLK should be stopped in the low state. See Table 19 for the BCLK voltage range specifications when BCLK is running.

5.1.2 BCLK AC Specifications

Table 19. BCLK AC Specifications at the Processor Core Pins

T#	Parameter	Min	Nom	Max	Unit	Note
	System Bus Frequency	N/A	100.0	N/A	MHz	Notes 5, 6
	BCLK Period	N/A	10.0	N/A	nS	Notes 2, 5, 6
	BCLK Period Stability	N/A	N/A	± 250	pS	Notes 3, 4, 5, 6
T3:	BCLK High Time	2.85	N/A	N/A	nS	At > 1.7V, Notes 5, 6
T4:	BCLK Low Time	2.55	N/A	N/A	nS	At > 0.7V, Notes 5, 6
T5:	BCLK Rise Time	0.175	N/A	0.875	nS	0.9V ~ 1.6V, Notes 5, 6
T6:	BCLK Fall Time	0.175	N/A	0.875	nS	1.6V ~ 0.9V, Notes 5, 6

NOTES:
1. All AC timings for GTL+ and CMOS signals are referenced to the BCLK rising edge at 1.25V. All CMOS signals are referenced at 0.75V.
2. The internal core clock frequency is derived from the PSB clock. The PSB clock to core clock ratio is determined during initialization and is predetermined by the Intel mobile module. The BCLK period allows a +0.5 nS tolerance for clock driver variation.
3. This value is measured on the rising edge of adjacent BCLKs at 1.25V. The jitter present must be accounted for as a component of BCLK skew between devices.
4. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The -20 dB attenuation point, as measured into a 10-pF to a 2-pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer. See the *CK97 Clock Synthesizer/Driver Specification (OR-1089)* for further details.
5. These values are not 100% tested and are specified by design characterization as a clock driver requirement.
6. Specifications labeled N/A are not available.

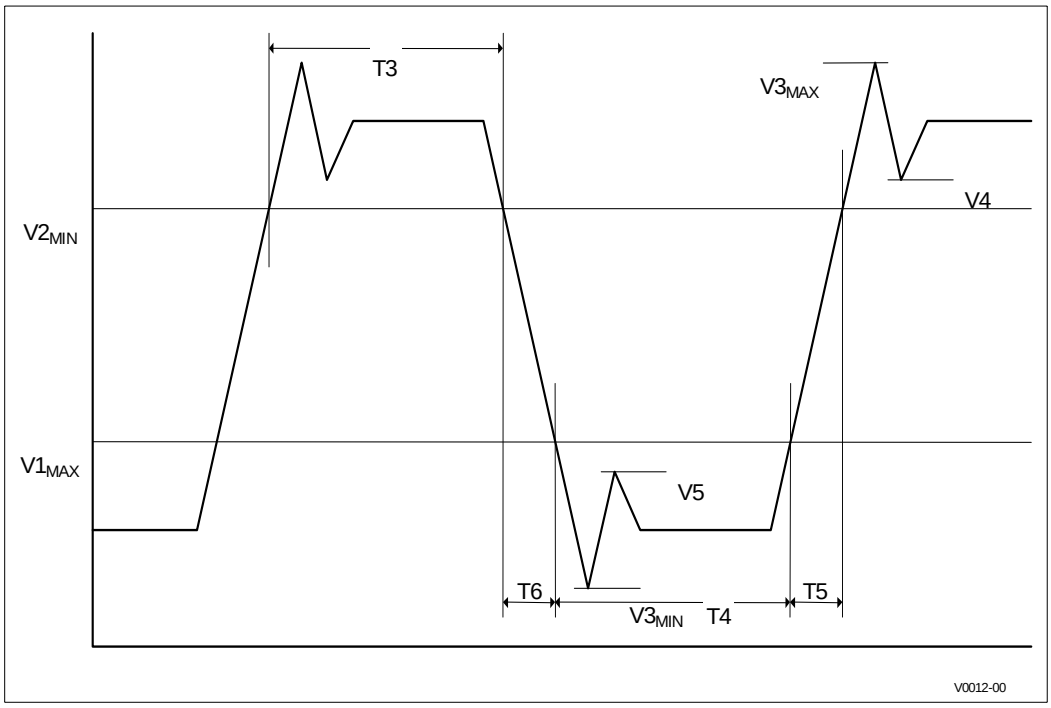
Table 20 describes the signal quality specifications at the processor core for the PSB clock (BCLK) signal. Figure 4 describes the signal quality waveforms for the PSB clock at the processor core pins For proper signal termination, refer to the "Clocking Guidelines" section in the *Mobile Pentium® III Processor/440BX AGPset Recommended Design and Debug Practices (RDDP-A) 100 MHz Rev. 2.0* (SC-2760).

Table 20. BCLK Signal Quality AC Specifications at the Processor Core

T#	Parameter	Min	Max	Unit	Notes
V1	$V_{IL,BCLK}$	-0.3	0.7	V	Note 1
V2	$V_{IH,BCLK}$	1.7	2.625	V	Note 1
V3	V_{IN} Absolute Voltage Range	-0.7	3.5	V	Undershoot, Overshoot, Note 2
V4	Rising Edge Ringback	1.7	N/A	V	Absolute Value, Notes 3, 4
V5	Falling Edge Ringback	N/A	0.7	V	Absolute Value, Notes 3, 4
	BCLK Rising/Falling Slew Rate	0.8	4.0	V/nS	

NOTES:
1. On the rising edge of BCLK, there must be a minimum overshoot to 2.0V. The clock must rise monotonically between $V_{IL,BCLK}$ and 2.0V and fall monotonically between $V_{IH,BCLK}$ and $V_{IL,BCLK}$.
2. These specifications apply only when BCLK is running. See Table 18 for the DC specifications when BCLK is stopped. BCLK may not be above $V_{IH,BCLK,MAX}$ or below $V_{IL,BCLK,MIN}$ for more than 50% of the clock cycle.
3. The rising edge ringback voltage is the minimum absolute voltage that the BCLK signal can dip back to after passing the $V_{IH,BCLK,MIN}$ (rising) voltage limits. The falling edge ringback voltage is the maximum absolute voltage that the BCLK signal can dip back to after passing the $V_{IL,BCLK,MAX}$ (falling) voltage limits.
4. Specifications labeled N/A are not available.

Figure 4. BCLK Waveform at the Processor Core Pins



5.2 System Power Requirements

Table 21 provides the DC power supply design criteria.

Table 21. System Power Requirements

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{DC}	DC Input Voltage	7.5	12.0	21.0	V	
I_{DC}	DC Input Current	0.1	2.6	5.0	A	Notes 1,2
I_{DC_RMS}	RMS Ripple Current	N/A	N/A	7.5	A	Notes 4,6
I_{DC_Surge}	Maximum Surge Current for V_{DC}	N/A	N/A	20.0	A	Notes 3,6
V_5	Power Managed 5.0-V Supply	4.75	5.0	5.25	V	
I_5	Power Managed 5.0-V Current, Operating	20.0	50.0	100.0	mA	
I_{5_Surge}	Maximum Surge Current for V_5	N/A	N/A	1.5	A	Notes 3,6
V_3	Power Managed 3.3-V Supply	3.135	3.3	3.465	V	
I_3	Power Managed 3.3-V Current	0.8	1.2	3.0	A	
I_{3_Surge}	Maximum Surge Current for V_3	N/A	N/A	4.0	A	Notes 3,6
V_{CPUPU}	Processor I/O Ring Voltage	1.375	1.5	1.625	V	
I_{CPUPU}	Processor I/O Ring Current	0.0	10.0	20.0	mA	
V_{CLK}	Processor Clock Rail Voltage	2.375	2.5	2.625	V	
I_{CLK}	Processor Clock Rail Current	24.0	35.0	80.0	mA	Note 5

NOTES:
1. V_DC is set for 12.0V in order to determine typical V_DC current.
2. V_DC is set for 7.5V in order to determine maximum V_DC current.
3. A 20-µS duration.
4. This is V_DC dependent. See Figure 7 for data of IDC-RMS vs. V_DC.
5. These values are system dependent.
6. Specifications labeled N/A are not applicable.

5.3 Processor Core Voltage Regulation

The DC voltage regulator (DC/DC converter) is designed to support the core voltage and I/O ring voltage for current and future Intel mobile processors. The DC voltage regulator provides the appropriate mobile Celeron processor core voltage, the GTL+ bus termination voltage, the processor sideband signal pull-up voltage, and the clock driver buffer voltage. Of these voltages, only the processor sideband pullup voltage (V_CPUPU) and the clock driver buffer voltage (V_CLK) are delivered to the system electronics.

The mobile module supports input DC voltage range of 7.5V ~ 21.0V from the system battery or power supply for mobile applications.

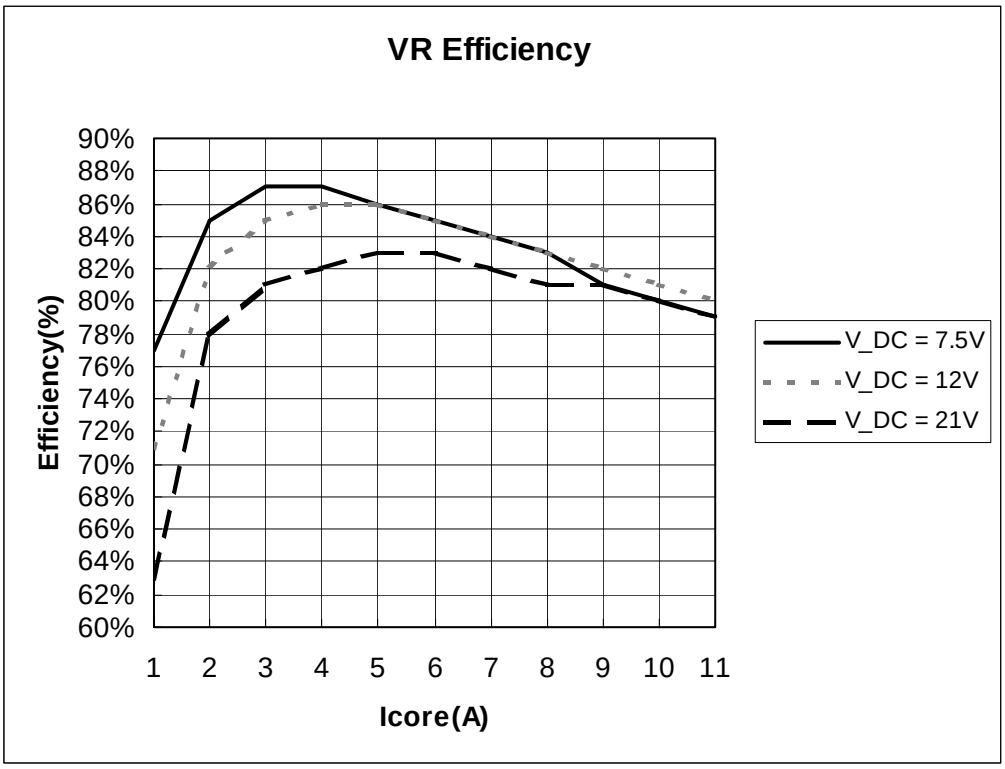
5.3.1 Voltage Regulator Efficiency

There are three voltage regulators on the mobile module. These voltage regulators generate the core voltage used by the CPU and the voltage for the CPU I/O ring voltage. The core voltage regulator provides the required current from the V_DC supply and its relative efficiencies are shown in Table 22 and Figure 5. The V_CLK and Vtt voltage regulators tap the V_3 plane.

Table 22. Vcore Power Conversion Efficiency

Vcore = 1.60V			
Icore (A)	**Efficiency at V_DC + 7.50V**	**Efficiency at V_DC + 12.0V**	**Efficiency at V_DC + 21.0V**
1	77%	71%	63%
2	85%	82%	78%
3	87%	85%	81%
4	87%	86%	82%
5	86%	86%	83%
6	85%	85%	83%
7	84%	84%	82%
8	83%	83%	81%
9	81%	82%	81%
10	80%	81%	80%
11	79%	80%	79%

Figure 5. VR Efficiency Chart



5.3.2 Voltage Regulator Control

The VR_ON pin on the connector allows a 3.3-V signal to control the voltage regulator. The system manufacturer can use this signal to turn the voltage regulator on or off. VR_ON should be controlled as a function of the same signal (SUSB#) used to control the system's switched 5.0-V/ 3.3-V power planes. The PIIX4E/M defines Suspend B as the Power Management state in which power is physically removed from the processor and the voltage regulator. In this state, the SUSB# pin on the PIIX4E/M controls these power planes. The mobile module provides the VR_PWRGD signal, which indicates that the voltage regulator power is operating at a stable voltage level. The system manufacturer should use this signal on the system electronics to control power inputs and to gate PWROK to the PIIX4E/M South Bridge. Table 23 provides the detailed definitions and sequences of the voltage signals.

Table 23. Voltage Signal Definitions and Sequences

Signal	Source	Definition and Sequences
V_DC	System Electronics	V_DC is required to be between 7.5V and 21.0V DC and is driven by the system electronics' power supply. V_DC powers the mobile module DC-to-DC converter for the processor core and I/O voltages. ***The mobile module cannot be hot inserted or removed while V_DC is powered on.***
V_5	System Electronics	V_5 is supplied by the system electronics for the voltage regulator.
V_3	System Electronics	V_3 is supplied by the system electronics for the 443BX and powers the mobile module's linear regulators for generating the V_CLK and V_CPUPU voltage rails. V_3 stays on during suspend.
V_3S	System Electronics	V_3S is supplied by the system electronics and is shut off during suspend.
VR_ON	System Electronics	VR_ON is a 3.3-V signal that enables the voltage regulator circuit. When driven active high the voltage regulator circuit is activated. The signal driving VR_ON should be a digital signal with a rise/fall time of less than or equal to 1.0 µS. ($V_{IL,max}$=0.4V, $V_{IH,min}$ =3.0V.)
V_CORE	Module	A result of VR_ON being asserted, V_CORE is an output of the DC-DC regulator on the mobile module and is driven to the core voltage of the processor.
VR_PWRGD	Module	Upon sampling the voltage level of V_CORE (minus tolerances for ripple), VR_PWRGD is driven active high. If VR_PWRGD is not sampled active within 1 second of the assertion of VR_ON, then the system electronics should deassert VR_ON. After V_CORE is stabilized, VR_PWRGD will assert to logic high (3.3V). This signal must not be pulled up by the system electronics. VR_PWRGD should be "logically ANDed" with V_3S to generate the PIIX4E/M input signal, PWROK. The system electronics should monitor VR_PWRGD to verify it is asserted high prior to the active high assertion of PIIX4E/M PWROK.
V_CPUPU	Module	V_CPUPU is 1.5V. The system electronics uses this voltage to power the PIIX4E/M-to-processor interface circuitry.
V_CLK	Module	V_CLK is 2.5V. The system electronics uses this voltage to power the HCLK[0:1] drivers for the processor clock.

The following list includes additional specifications and clarifications of the power sequence timing and Figure 6 provides an illustration.

1. The VR_ON signal may only be asserted to a logical high by a digital signal after V_DC ≥ 7.5V, V_5 ≥ 4.5V, and V_3 ≥ 3.0V.
2. The Rise Time and Fall Time of VR_ON must be less than or equal to 1.0 µS.
3. VR_ON has its $V_{IL\ max}$ = +0.4V and $V_{IH\ min}$ = +3.0V.
4. The VR_PWRGD will get asserted to logic high (3.3V) after V_CORE is stabilized and V_DC reaches 7.5V. This signal should not and can not be pulled up by the system electronics.
5. In the power-on process, Intel recommends to raise the higher voltage power plane first (V_DC), followed by the lower power planes (V_5, V_3), and finally assert VR_ON after above voltage levels are met on all rails. The power-off process should be the reverse process, i.e. VR_ON gets deasserted, followed by the lower power planes, and finally the higher power planes.

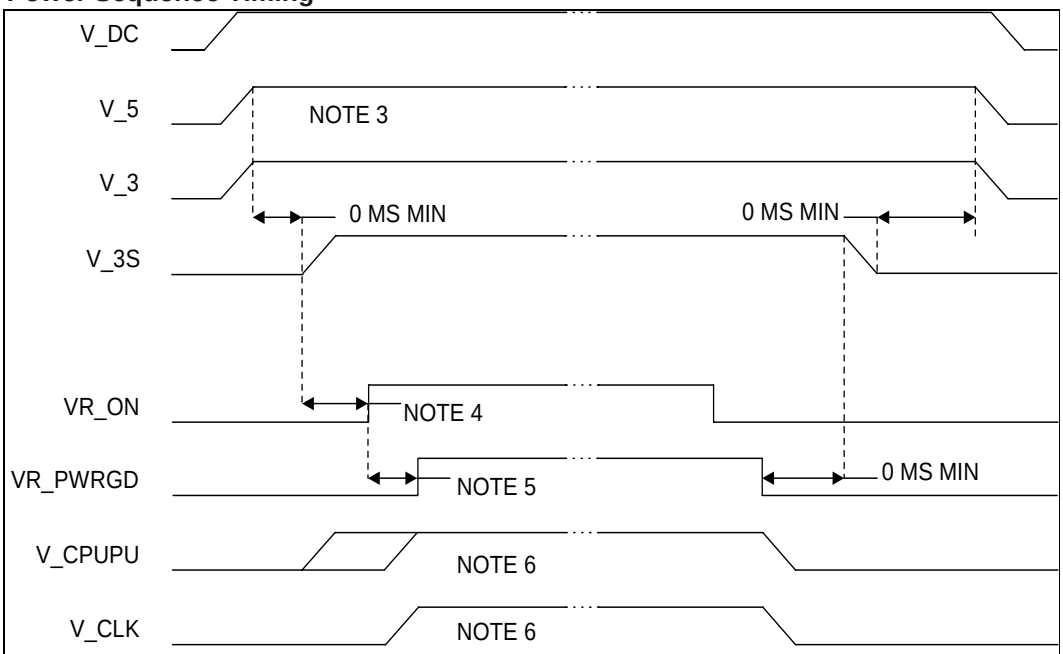
6. VR_ON must monotonically rise through its V_{IL} to V_{IH} and fall through its V_{IH} to V_{IL} points. The sign of slope can not change between V_{IL} and V_{IH} in rising and V_{IH} and V_{IL} in falling.
7. VR_ON must provide an instantaneous in-rush current to the mobile module with the following values as listed in Table 24.

Table 24. VR_ON In-rush Current

	Instantaneous	DC Operating
Maximum	41.0 mA	0.1 µA
Typical	0.2 mA	0.0 µA

8. VR_ON Valid-Low Time: This specifies how long VR_ON needs to be low for a valid off before VR_ON can be turned back on again. In going from a valid on to off and then back on, the following conditions must be met to prevent damage to the system or the mobile module:
   - VR_ON must be low for 1.0 mS
   - The original voltage level requirements for turn-on must be met before assertion of VR_ON (i.e. V_DC ≥ 7.5V, V_5 ≥ 4.5V, and V_3 ≥ 3.0V)

Figure 6. Power Sequence Timing



NOTES:
1. PWROK on I/O board should be active on when VR_PWRGD is active and V_3S is good.
2. CPU_RST from I/O board should be active for a minimum of 6.0 mS after PWROK is active and PLL_STP# and CPU_STP# are inactive. Note that PLL_STP# is an AND condition of RSMRST# and SUSB# on the PIIX4E/M.
3. This is the 5V power supplied to the MMC-2 connector. This should be the first 5.0-V plane to power up. It stays on during suspend.
4. V_DC >= 7.5V, V_5>=4.5V, V_3S>=3.0V.
5. VR_PWRGD is specified active by the module regulator within less than or equal to 6.0-mS maximum after the assertion of VR_ON.
6. V_CPUPU and V_CLK are generated on the mobile module.

5.3.3 Power Planes: Bulk Capacitance Requirements

The placement of sufficient bulk capacitance on the system electronics board is critical to the operation of the mobile module and to ensure that the system design can accommodate future high frequency modules. Intel has provided the maximum possible bulk capacitance on the mobile module. However, in order to achieve proper filtering and in-rush current protection, it is imperative that additional filtering be provided on the system electronics board. Table 25 details the bulk capacitance requirements for the system electronics.

Note: Observe the voltage rating requirement for the capacitors on each respective voltage rail.

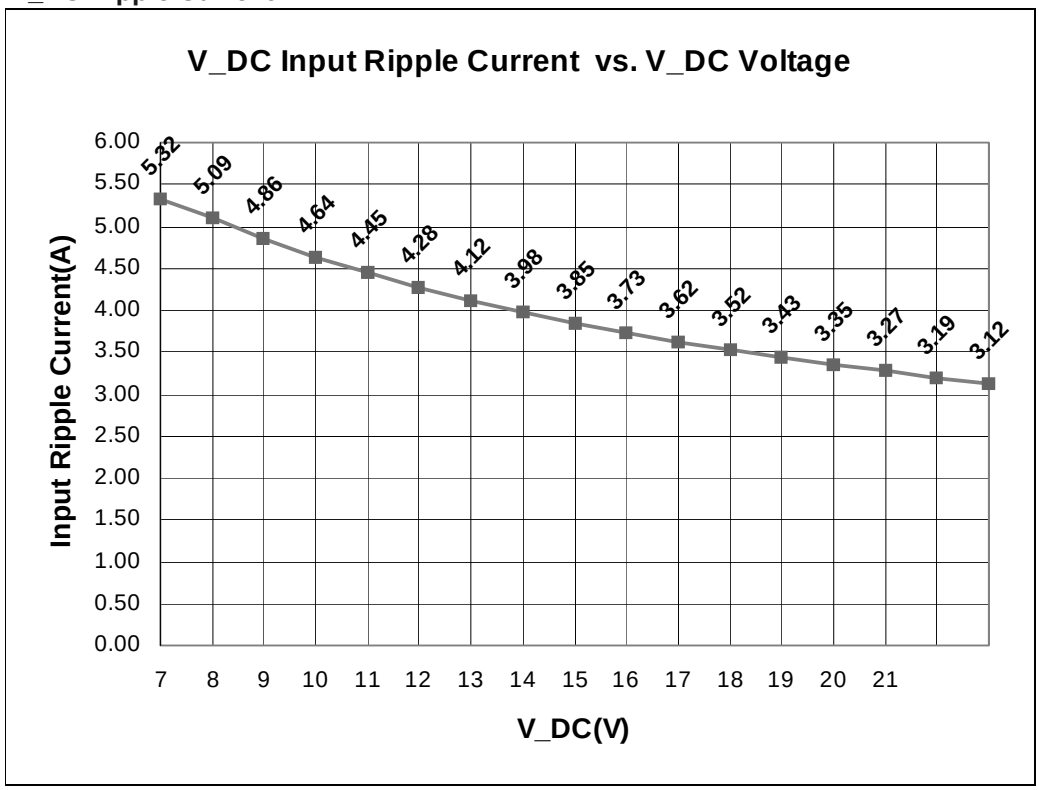
Table 25. Bulk Capacitance Requirements

Power Plane	Bulk Capacitance Requirements			High Frequency Capacitance Requirements	Notes
	Total Capacitance	ESR Max	RMS Ripple Current		
V_DC	100.0 µF	20.0 mΩ	3.0A~ 5.0A	0.1 µF, 0.01 µF	Notes 1,3,4,5,6
V_5	100.0 µF	100.0 mΩ	1.0A	0.1 µF, 0.01 µF	Notes 1,4,5,6
V_3	470.0 µF	100.0 mΩ	1.0A	0.1 µF, 0.01 µF	Notes 1,4,5,6
V_3S	100.0 µF	100.0 mΩ	N/A	0.1 µF 0.01 µF	Notes 1,4,5,6
VCC_AGP	22.0 µF	100.0 mΩ	1.0A	0.1 µF, 0.01 µF	Notes 1,4,5,6
V_CPUPU	2.2 µF	N/A	N/A	8200.0 pF	Notes 1,5,6,7
V_CLK	10.0 µF	N/A	N/A	8200.0 pF	Notes 1,2,5,6,7

NOTES:
1. Placement of above capacitance requirements should be located near the connector.
2. V_CLK filtering should be located next to the system clock synthesizer.
3. The Ripple current specification depends on the V_DC input for the module. See Figure 7 below.
4. If Tantalum* Capacitors are used, a 50% voltage derating practice must be observed. For example, a 5.0-V rail requires a 10.0-V rated capacitor.
5. In order to reduce ESR, Intel recommends the use of multiple bulk capacitors rather than a single large capacitor.
6. Intel strongly recommends that system manufacturers pay close attention to capacitor design considerations. Specifically, the "Capacitance vs. Temperature De-rating Curve," "Capacitance vs. Applied DC Voltage De-rating Curve," and the "Capacitance vs. Frequency De-rating Curve." Some capacitor dielectrics are particularly susceptible to these conditions, for example Y5V ceramic capacitors.
7. Specifications labeled N/A are not available.

Figure 7 shows the dependence of V_DC ripple current on V_DC.

Figure 7. V_DC Ripple Current



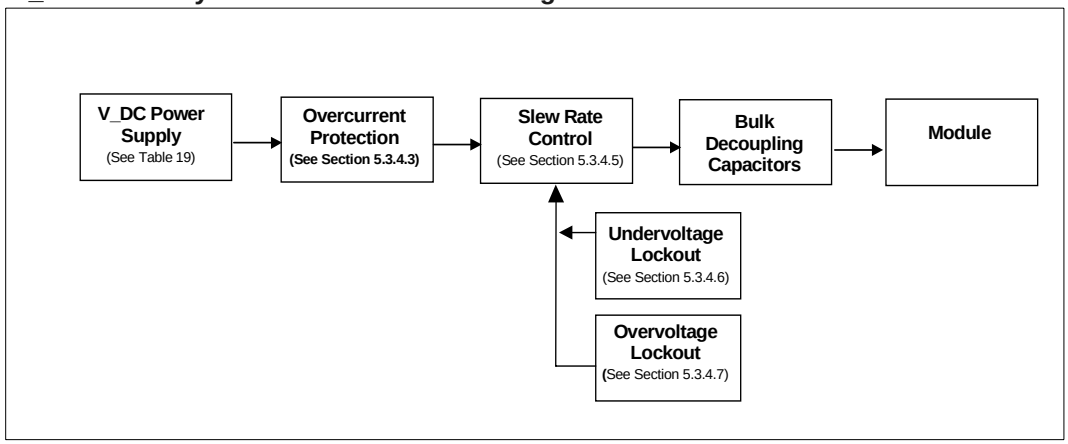
5.3.4 Surge Current Guidelines

5.3.4.1 DC Power System Protection

The recommended DC Power System Protection consists of the following:

- A DC Power Supply that is capable of delivering 7.5V to 21.0V to the mobile module
- An Overcurrent Protection circuit that provides a means to limit the maximum current available to the system
- A Slew Rate Control circuit that provides a controlled voltage slew rate at turn on, which provides protection for components sensitive to fast voltage rise times
- An Undervoltage Lockout circuit that protects against potentially damaging high currents, which might be encountered if the DC Power Supply voltage is too low
- An Overvoltage Lockout circuit that provides protection from potentially damaging high DC Power Supply voltages
- Bulk Decoupling Capacitors that provide filtering and a reservoir of energy, which can provide a faster transient response than the power supply

Figure 8. V_DC Power System Protection Block Diagram



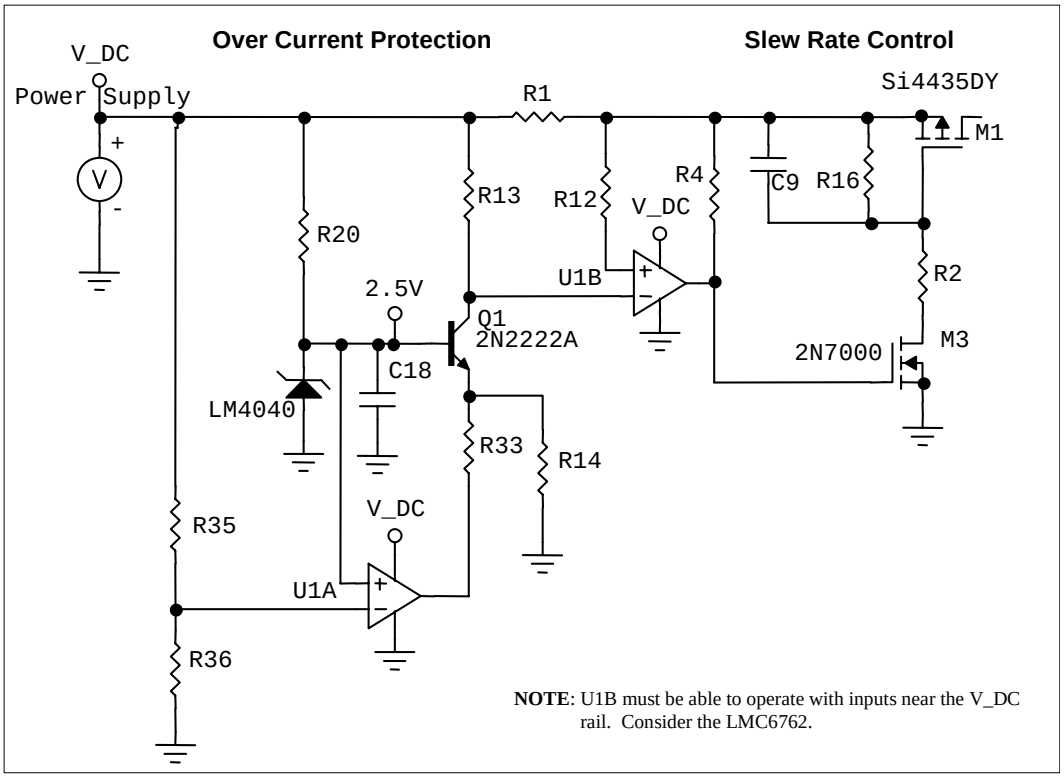
5.3.4.2 V_DC Power Supply

The power supply must be able to deliver 7.5V to 21.0V to the mobile module, measured at the mobile module.

5.3.4.3 Overcurrent Protection

The Overcurrent Protection circuit provides a way to limit current drawn by the mobile module. Under normal operating conditions, I_DC should not exceed 3.0A at V_DC = 7.5V. To allow for component variations and margining issues, a reasonable I_DC Current Limit would be 6.0A.

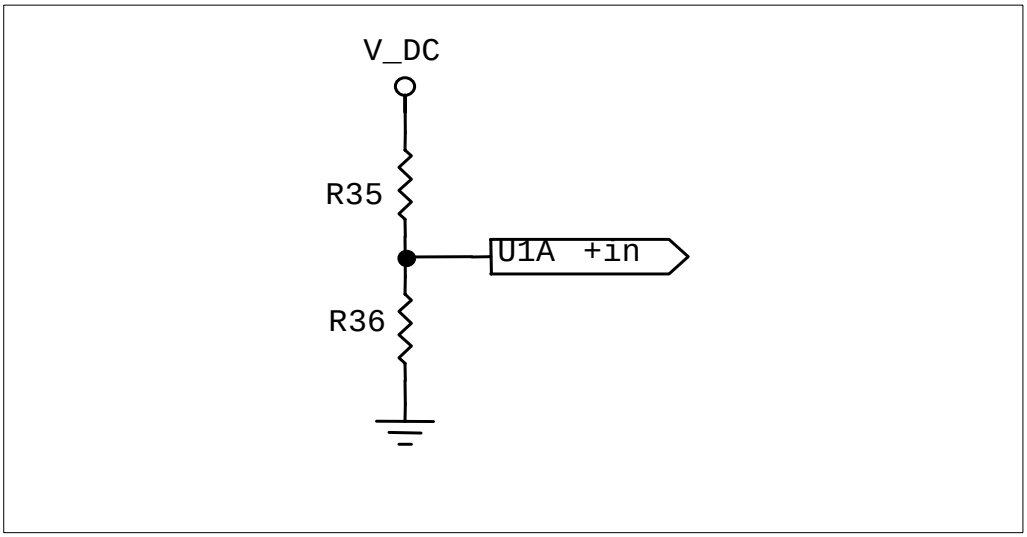
Figure 9. Overcurrent Protection Circuit



At the other end of the V_DC input range, the current will be somewhat less. At 14.0V, for example, the corresponding power could be produced with only 3.0A. In this example, a comparator, U1A, will be used to sense when V_DC is over 14.0V and will shift the current limit from 6.0A to 3.0A.

- Let I_DC(limit)= 6.0A
- Let I_DC(limit2)= 3.0A
- Let b(Q1)= 100
- Let R1= 5.0 mΩ= 0.005Ω
- Let R12= 100.0Ω
- Let R13= 100.0Ω
- Let V(R14)≈ 1.8V
- Let I(R20)≈ 100.0 µA
- Let C36= 2.0K

Figure 10. Current Shift Model



5.3.4.4 Current Limit Shift Point

The comparator U1A should switch when the non-inverting input is equal to the 2.5-V reference on the inverting input, or when the voltage applied to V_DC is equal to the selected switch point and the voltage dropped across R36 is 2.5V. In this example, the change should occur when V_DC= 14.0V.

Equation 1.

$$R35 := \frac{(V\_DC - Vref)}{\frac{Vref}{R36}} \qquad R35 := \frac{(14 - 2.5)}{\frac{2.5}{2000}}$$

(The nearest standard 1% value is 9.01 kΩ)

The comparator U1A will pull its output low when V_DC falls below 14.0V, which will effectively put R33 in parallel with R14.

When power is initially applied to the circuit, C18 charges up to 2.5V through R20. This slowly rising voltage is applied to the base of the current source, Q1. The voltage on R14 is approximately 2.5V minus the base-emitter drop of about 0.7V (at 25°C): $V_{(R14)} \approx 1.8V$. Q1 is a 2N2222A with a moderate β of about 100. Therefore, the current through R13 is approximately equal to the current through R14.

The charging of C18 provides a small increment of delay as U1 will not allow R4 to pull up the Gate of M3 until Q1 has pulled the non-inverting input of U1 down slightly.

The voltage developed across R1 is a function of the load. See Equation 2 below.

Equation 2.

$$V(R1) = I\_DC * R1$$

If the maximum I_DC expected is 3.0A, consider setting the I_DC Current Limit at 6.0A. If the Current Sense resistor, R1, is selected to be 5.0 mΩ (0.005Ω), the maximum voltage developed across this resistor can be calculated.

Consider now the case where V_DC is above 14.0V. See Equation 3 below.

Equation 3.

I_DC(limit)*Rsense= 3.0A*5E-3= 15.0 mV)

The Offset voltage applied to the inverting input of the comparator, U1B, should then be 15.0 mV. If R13 is selected to be 100.0Ω, the current can then be calculated as shown in Equation 4 below.

Equation 4.

Ioffset= 15.0 mV/100.0Ω= 150.0 µA

Note: For a successful design, the input offset of the comparator should also be considered. One option is that the design offset is at least ten times greater than the device offsets.

The value of R14 can now be calculated with Equation 5.

Equation 5.

R14= 1.8V/150.0 µA= 12.0 kΩ

(The nearest 1% value is 12.1K.)

Consider now the case when V_DC drops below 14.0V, and the current limits shift to 6.0A.

Equation 6.

I_DC(limit)*Rsense= 6.0A*5E-3= 30.0 mV

The Offset voltage applied to the inverting input of the comparator, U1B, should then be 30.0 mV. If R13 is selected to be 100.0Ω, the current can then be calculated as shown in Equation 7 below.

Equation 7.

Ioffset= 30.0 mV/100.0Ω= 300.0 µA

The value of the parallel combination of R14 and R33 can now be calculated as shown in Equation 8 below.

Equation 8.

Rcombo= 1.8V/300.0 µA= 6.0 kΩ

R14 is a 12.0-K resistor. If R33 is also 12.0K, then the parallel combination will be 6.0K.

In R20, the LM4040-2.5 has a very wide operating current range from 60.0 µA to 15.0 µA. In order to provide the current source base drive you will need Equation 9.

Equation 9.

Ibase≈ Ic/b=300.0 µA/100= 3.0 µA

If 100 µA is selected for I(R20), it would be adequate for the reference and current source base drive. Since both of these currents must be satisfied at the low power supply margin, a V_DC of 7.5V will be assumed.

Equation 10.

$$R20 = (V\_DC - Vref)/I(R20) = (7.5-2.50)/100.0\ \mu A = 50.0\ k\Omega$$

(To allow for component tolerances, 51.0 kΩ is recommended.)

5.3.4.5 Slew Rate Control

The Slew Rate Control regulates the rate that the power supply voltage is applied to the system.

- Let the Threshold voltage of M1, V_t = -1.0V
- Let M1 $V_{GS(sat)}$ = -2.4V, also denoted as V_{sat}
- Let R16 = 100.0 kΩ
- Let t_delay = 500.0 µS
- Let C_{total} = The sum or the Bulk capacitors + the sum of the module capacitors = 5 X 22.0 µF + 2 X 4.7 µF=119.4 µF

M1 is a low RDS(on) P-Channel MOSFET, such as the Siliconix* Si4435DY. When the power supply voltage is applied and increased to a value that exceeds the Lockout value, (7.5V will be used in this example), the Undervoltage Lockout circuit allows R4 to pull up the gate of M3 to start a turn-on sequence. M3 pulls its drain toward ground, forcing current to flow through R2. M1 will not start to source any current until after t_delay, with t_delay defined as shown in Equation 11 and Equation 12 below.

Equation 11.

$$t\_delay := -R2 \cdot C9 \cdot \ln\left(1 - \frac{Vt}{V\_DC - Vg}\right)$$

Equation 12.

$$Vgs := \frac{R16}{R16 + R2}\ V\_DC$$

The published minimum threshold of the Si4435DY is a V_{GS} of -1.0V, i.e. C9 must charge to 1.0V before M1 starts to turn on. The delay, t_delay, is the time required to charge C9 to 1.0V.

Assuming a negligible voltage drop across M3, when M3 is on, the voltage on the Gate of M1, V_G, with respect to ground, is the voltage developed across R2: $V_G \equiv V_{(R2)}$. If a minimum steady-state bias on M1 should be -4.5V, then this will be the voltage dropped across R16. At the low end of the V_DC margin, i.e. 7.5V, V_G can be derived from Equation 13 below.

Equation 13.

$$V_G = V\_DC + V_{GS} = 7.5V - 4.5V = 3.0V \text{ (with respect to ground)}$$

Equation 14.

$$R2 := \frac{Vg \cdot R16}{V\_DC - Vg} \quad , \qquad R2 = 66.67\ k\Omega$$

(The nearest standard 1% value is 66.5 kΩ. The example will continue with R2= 66.5 kΩ.)

Rearranging Equation 8 to solve for C9 yields Equation 15.

Equation 15.

$$C9 := \frac{-t\_delay}{R2 \cdot \ln\left(1 - \frac{Vt}{V\_DC - Vg}\right)}$$

Now a value for C9 can be calculated as shown in the Equation 16 below.

Equation 16.

$$C\ 9 = 0.354\ \mu F$$

(A close standard value of 0.33 µF will yield a t_delay of 466.0 µS.)

The ramp-up time, t_ramp, is defined as shown in Equation 17.

Equation 17.

$$t\_ramp := -R2 \cdot C9 \cdot \ln\left(1 - \frac{Vsat}{Vgs}\right) - t\_delay$$

If M1 has a VGS(sat) of -2.4V, then Equation 18 applies.

Equation 18.

$$t\_ramp = 948.8\ \mu S$$

The maximum current during the power-up ramp is shown in Equation 19 below.

Equation 19.

$$Imax := Ctotal\left(\frac{d}{dt} v\right) \approx Ctotal \cdot \frac{V\_DC}{t\_ramp}$$

If the total capacitance, Ctotal on the V_DC bus, is 119.4 µF, then see Equation 20 below.

Equation 20.

$$Imax = 0.944A$$

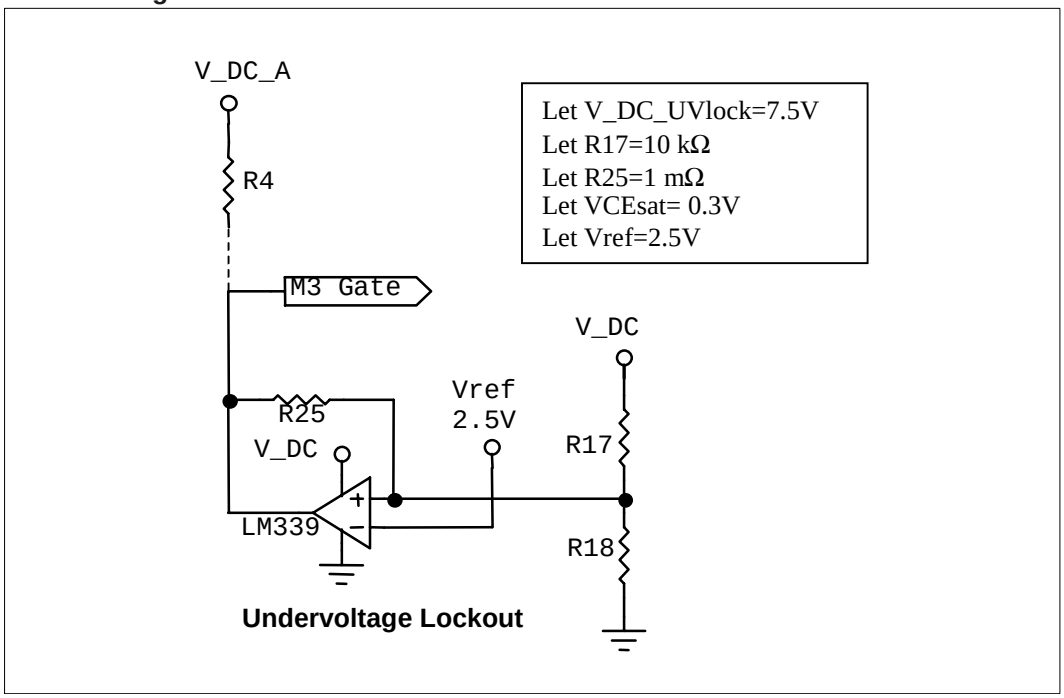
From the values assumed and calculated, t_delay = 466.0 µS, t_ramp = 949.0 µS, and Imax = 944 mA.

5.3.4.6 Undervoltage Lockout

The circuit below shows the Undervoltage Lockout portion of the V_DC Supply circuit. This circuit protects and locks out the applied voltage to the mobile module to prevent an accidental turn-on at low V_DC supply voltages.

Warning: A low voltage applied to the mobile module could result in destructive current levels.

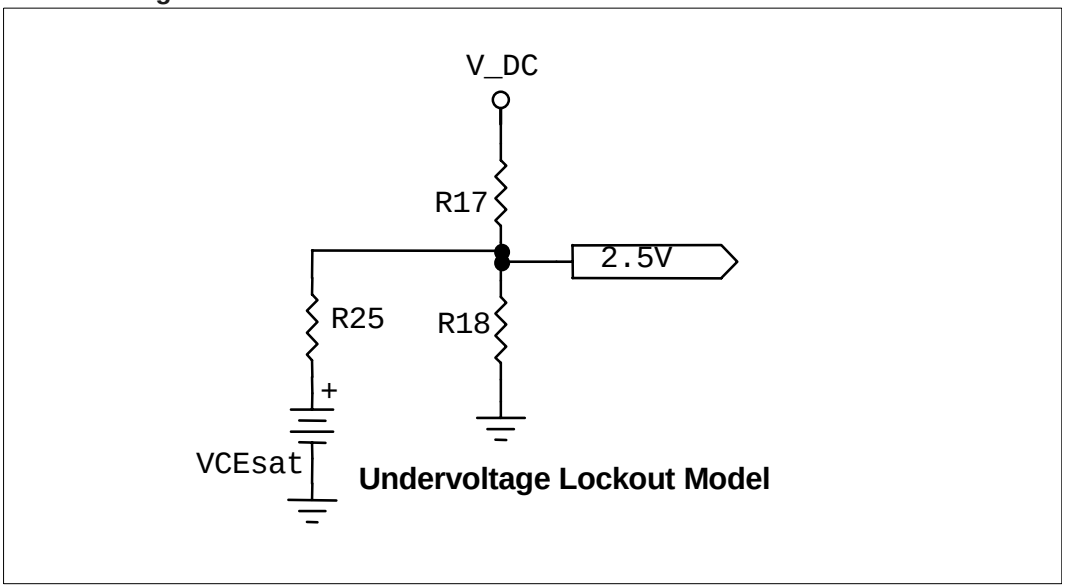
Figure 11. Undervoltage Lockout



The output of the LM339 comparator is an open-collector and is low when the applied voltage at V_DC is less than 7.5V, which holds the Gate of M3 low. Consequently, the Slew Rate Controller is not allowed to turn on. The 2.5-V reference, V_{ref}, voltage is derived from D7 in Figure 9. When non-inverting input of the comparator exceeds V_{ref}, 2.5V, the comparator trips and allows its output to go to a High Z state. The gate of M3 can then be pulled up by R4, starting the controlled Power-up Slew.

The model in Figure 12 will be used to calculate the Undervoltage Lockout trip point.

Figure 12. Undervoltage Lockout Model



VCEsat is the saturation voltage of the comparator output transistor. The comparator trip point voltage can be calculated with Equation 21.

Equation 21.

$$V\_DC\_UVlock := Vref + \left(\frac{Vref}{R18} + \frac{Vref - VCEsat}{R25}\right) R17$$

If power to the mobile module is to be held off until V_DC exceeds 7.5V, Equation 21 can be rearranged to solve for R18.

Equation 22.

$$R18 := \frac{Vref \cdot R17 \cdot R25}{R25 \cdot (V\_DC\_UVlock - Vref) - R17 \cdot (Vref - VCEsat)}$$

A value for R18 can be determined by plugging these values into Equation 23.

Equation 23.

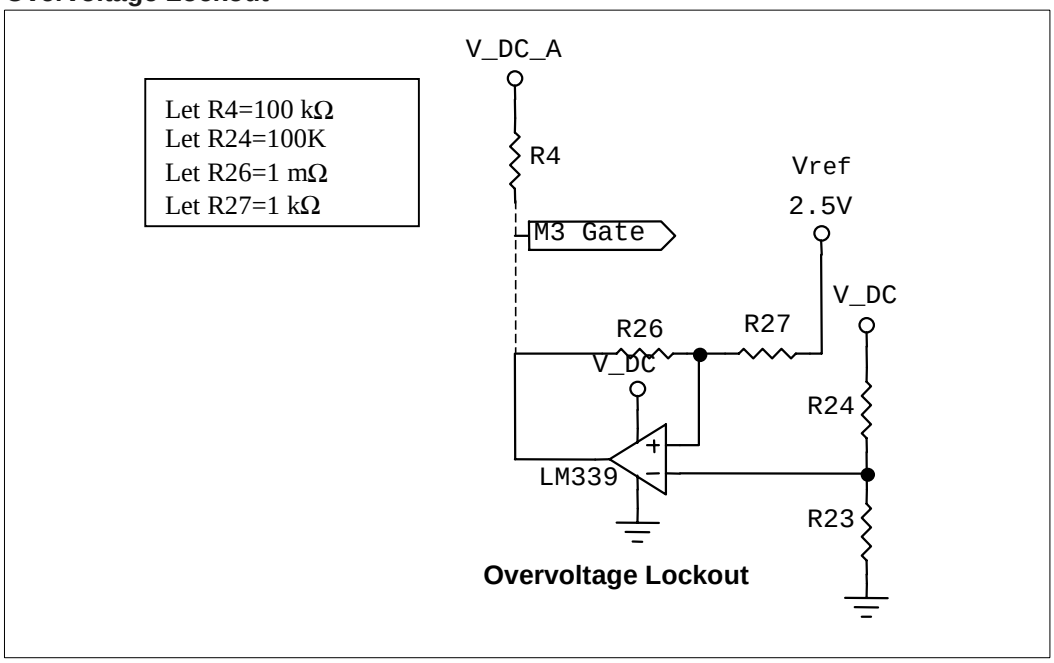
$$R18 = 5.022\ k\Omega$$

(4.99 kΩ is a standard 1% resistor value, which would provide lockout below 7.532V.)

5.3.4.7 Overvoltage Lockout

The mobile module operates with a maximum input voltage of 21.0V. This circuit can be set to lock out the input voltage if it exceeds the desired input.

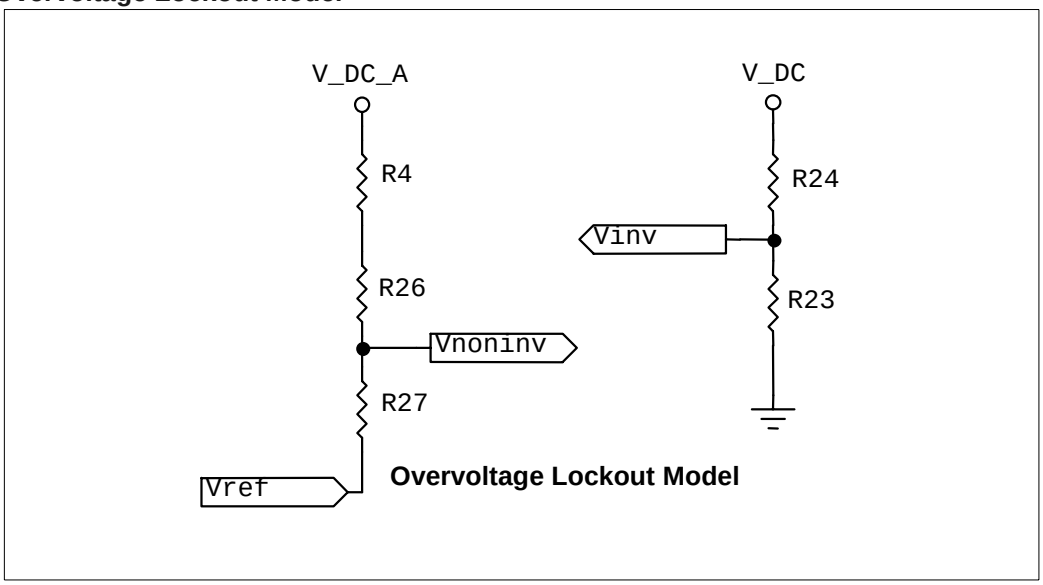
Figure 13. Overvoltage Lockout



The LM339 comparator is an open-collector output and is pulled low when the applied voltage at V_DC is too high, thus disabling the Slew-rate circuit.

The model in Figure 14 below will be used for component calculations.

Figure 14. Overvoltage Lockout Model



Assume that the desired V_DC Overvoltage Lockout is 21.0V. Using Equation 24, the input to the non-inverting input of the OV Lockout comparator can be calculated using the following equations.

Equation 24.

$$Vnoninv := Vref + \frac{R27 \cdot (V\_DC\_OVlock - Vref)}{R4 + R26 + R27}$$

Equation 25.

$$Vnoninv = 2.517V$$

Equation 26.

$$Vinv := \frac{(V\_DC\_OVlock \| R23)}{R23 + R24}$$

The output of the OV Lockout comparator will become active and pull down when the inverting input becomes greater than the 2.517V input on the non-inverting input. Equation 26 can be rearranged to solve for R23.

Equation 27.

$$R23 := \frac{R24 \cdot Vinv}{V\_DC\_OVlock - Vinv}$$

The OV Lockout comparator trip point is defined by Vinv = Vnoninv = 2.517V. Equation 28 provides a solution for R23.

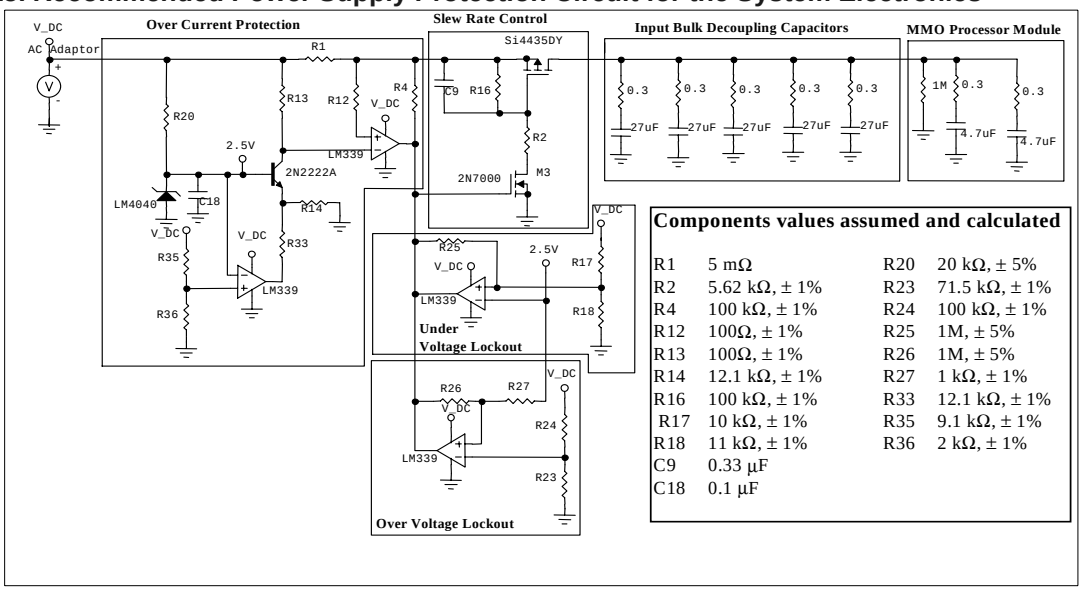
Equation 28.

$$R23 = 13.618\ k\Omega$$

(The nearest standard 1% value is 13.7 kΩ.)

If V_DC exceeds 6.0V, the voltage on the OV Lockout comparator inverting input will exceed 2.517V causing the comparator to trip.When the comparator trips, its output is low. Consequently, the Power Skew Control circuit is disabled, which will disconnect V_DC from the mobile module.

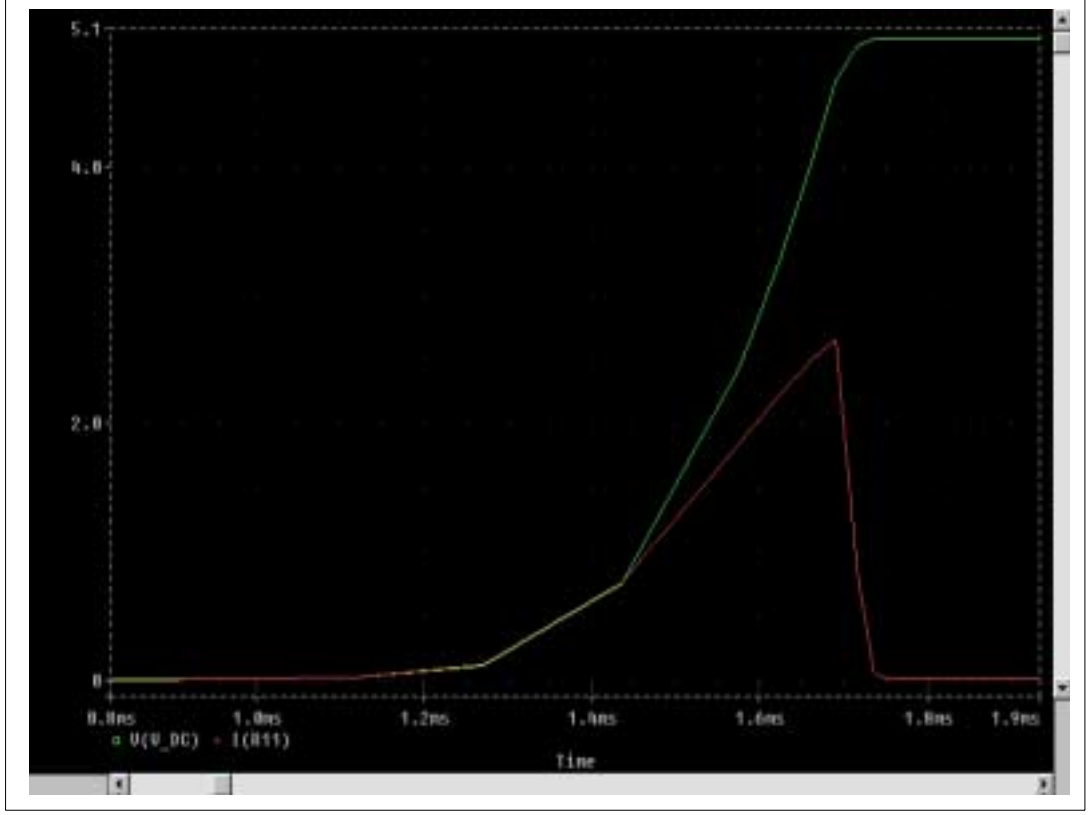
Figure 15. Recommended Power Supply Protection Circuit for the System Electronics



Components values assumed and calculated

R1	5 mΩ	R20	20 kΩ, ± 5%
R2	5.62 kΩ, ± 1%	R23	71.5 kΩ, ± 1%
R4	100 kΩ, ± 1%	R24	100 kΩ, ± 1%
R12	100Ω, ± 1%	R25	1M, ± 5%
R13	100Ω, ± 1%	R26	1M, ± 5%
R14	12.1 kΩ, ± 1%	R27	1 kΩ, ± 1%
R16	100 kΩ, ± 1%	R33	12.1 kΩ, ± 1%
R17	10 kΩ, ± 1%	R35	9.1 kΩ, ± 1%
R18	11 kΩ, ± 1%	R36	2 kΩ, ± 1%
C9	0.33 µF		
C18	0.1 µF		

Figure 16. Simulation of V_DC Voltage Skew



5.4 Active Thermal Feedback

Table 26. Thermal Sensor SMBus Address

Function	SMBus Address
Thermal Sensor	1001 110

5.5 Thermal Sensor Configuration Register

The configuration register of the thermal sensor controls the operating mode (Auto Convert vs. Standby) of the device. Since the processor temperature varies dynamically during normal operation, Auto Convert mode should be used exclusively to monitor processor temperature.

Table 27 shows the format of the configuration register. If the RUN/STOP bit is low, then the thermal sensor enters Auto Convert mode. If the RUN/STOP bit is set high, then the thermal sensor immediately stops converting and enters the Standby mode. The thermal sensor will still perform temperature conversions in Standby mode when it receives a one-shot command. However, the result of a one-shot command during Auto Convert mode is not guaranteed. Intel does not recommend using the one-shot command to monitor temperature when the processor is active, only Auto Convert mode should be used. The thermal sensor can be configured in various interface modes for temperature sampling. Intel recommends interfacing the thermal sensor using Interrupt mode. For more detailed information regarding interface methods, please see the *Intel® Mobile Module Thermal Diode Temperature Sensor Application Note* available through your Intel Field Representative.

Table 27. Thermal Sensor Configuration Register

Bit	Name	Reset State	Function
7 MSB	MASK	0	Masks SMBALERT# when high
6	RUN/STOP	0	Standby mode control bit. If low, the device enters Auto Convert mode. If high, the device immediately stops converting and enters Standby mode where the one-shot command can be performed.
5-0	RFU	0	Reserved for future use

NOTE: All RFU bits should be written as “0” and read as “don’t care” for programming purposes.

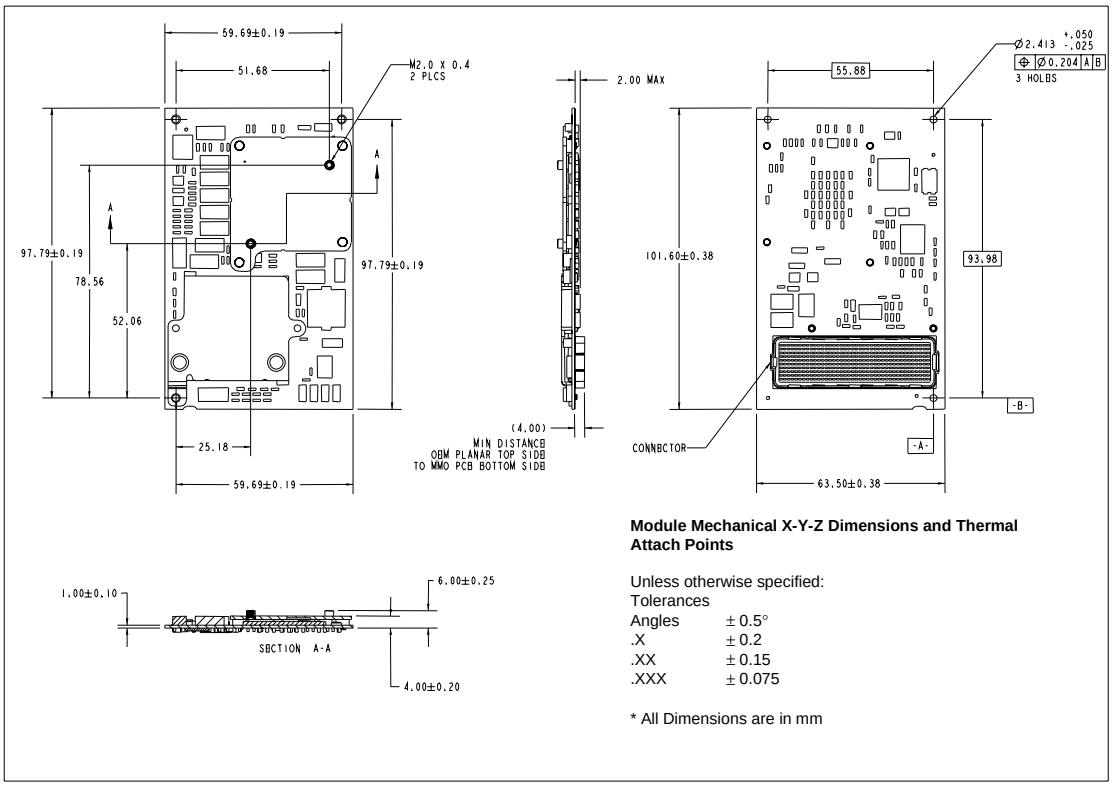
6.0 Mechanical Specification

This section provides the physical dimensions of the Celeron processor mobile module.

6.1 Mobile Module Dimensions

Figure 17 shows the board dimensions and the connector orientation.

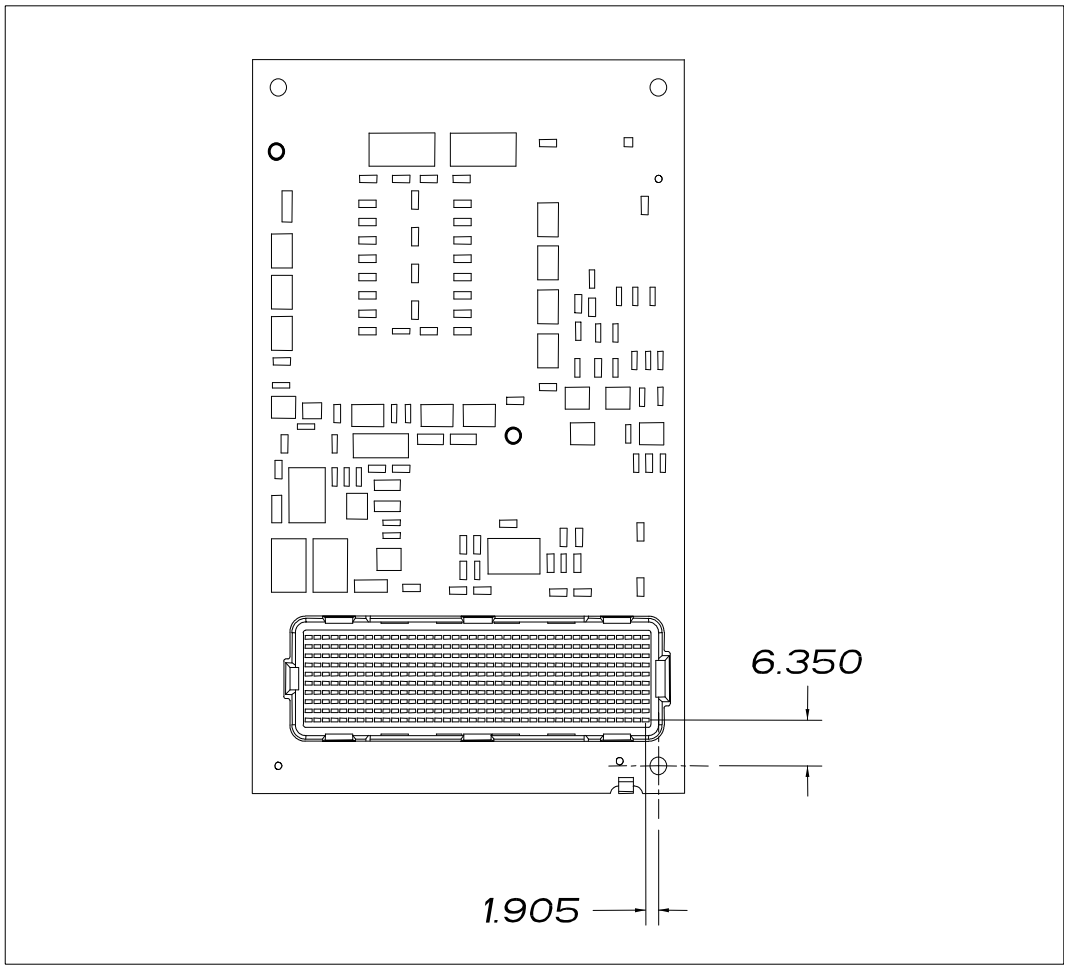
Figure 17. Board Dimensions and MMC-2 Connector Orientation



6.1.1 Pin 1 Location of the MMC-2 Connector

Figure 18 shows the location of pin 1 of the 400-pin connector.

Figure 18. Board Dimensions and MMC-2 Connector—Pin 1 Orientation

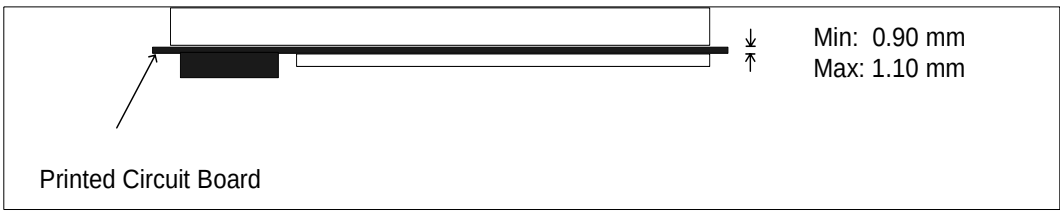


6.1.2 Printed Circuit Board

Figure 19 shows the minimum and maximum thickness of the printed circuit board (PCB). The range of PCB thickness allows for different PCB technologies to be used with current and future Intel mobile modules.

Note: The system manufacturer must ensure that the mechanical restraining method and/or system-level EMI contacts are able to support this range of PCB for compatibility with future Intel mobile modules.

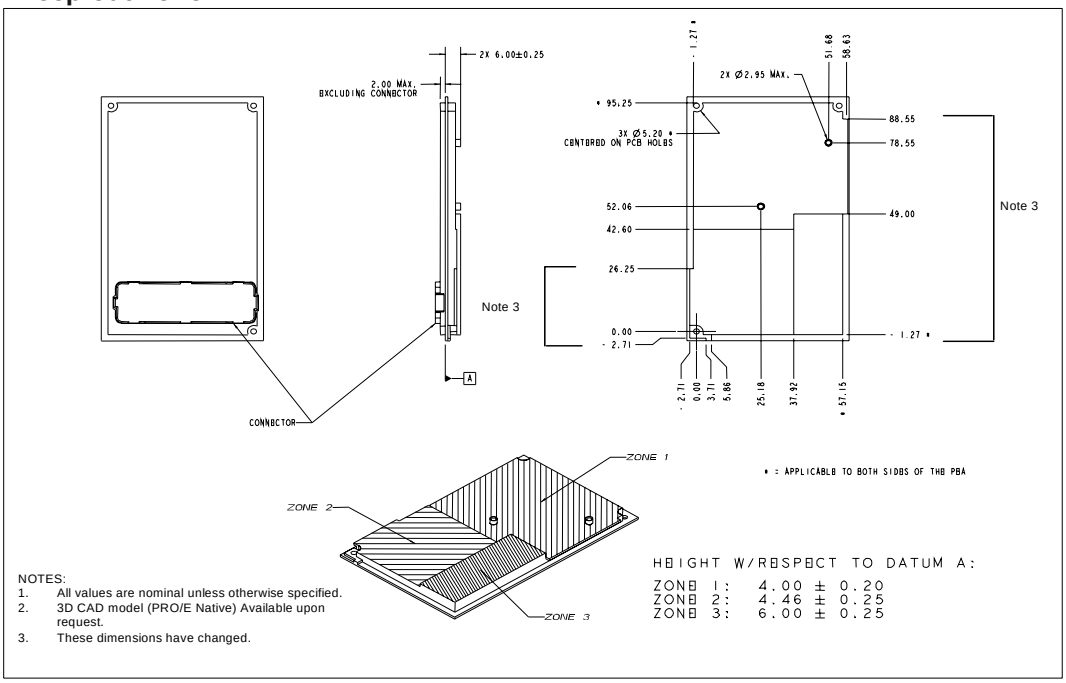
Figure 19. Printed Circuit Board Thickness



6.1.3 Height Restrictions

Figure 20 shows the mechanical stack-up and the associated component clearance requirements. This is the module keep-out zone and should not be entered. The system manufacturer establishes board-to-board clearance between the mobile module and the system electronics by selecting one of three mating connectors available in heights of approximately 4 mm, 6 mm, and 8 mm. The three sizes provide flexibility in choosing the system electronics components between the two boards. Information on these connectors can be obtained from your Intel Field Representative.

Figure 20. Keep-out Zone



6.2 Thermal Transfer Plate

A thermal transfer plates (TTP) provide heat dissipation on the processor and the 82443BX. The TTP may vary on different generations of Intel mobile modules. The TTP provides the thermal attach point where a system manufacturer can transfer heat through the notebook system using a heat pipe, a heat spreader plate, or a thermal solution. Attachment dimensions for the thermal interface block to the TTP are provided in Figure 21, Figure 22, and Figure 23. The TTP on the mobile module is designed to be a high efficiency spreader. To fully take advantage of the mobile module thermal design and optimize the system thermal performance, the contact area (Ac) needs to be a minimum of 30 mm x 30 mm. While it crucial to maximize the contact area, it is equally important to ensure that the contact area and/or the mobile module is free from warpage in an assembled configuration.

Warning: If warpage occurs, the thermal resistance of the mobile module could be adversely affected.

When attaching the mating block to either TTP, Intel recommends that a thermal elastomer be used as an interface material. This material reduces the thermal resistance. The system thermal interface block should be secured with M2 screws using a maximum torque of 1.5 Kg*cm to 2.0 Kg*cm (equivalent to 0.147 N*m to.197 N*m). The thread length of the M2 screws should be 2.25-mm

gageable thread (2.25-mm minimum to 2.80-mm maximum). The mobile module is designed to ensure that the thermal resistance between the processor die center and a point directly above on the TTP surface is ≤ to 1.0° C/W, under the following set of conditions.

- R_{TTP-a} = TTP (center point) to ambient = ~2.4° C/W
- A_c = Contact area centered between the two TTP attach points = 30 mm x 30 mm.

Figure 21. 82443BX Thermal Transfer Plate (Reference Only)

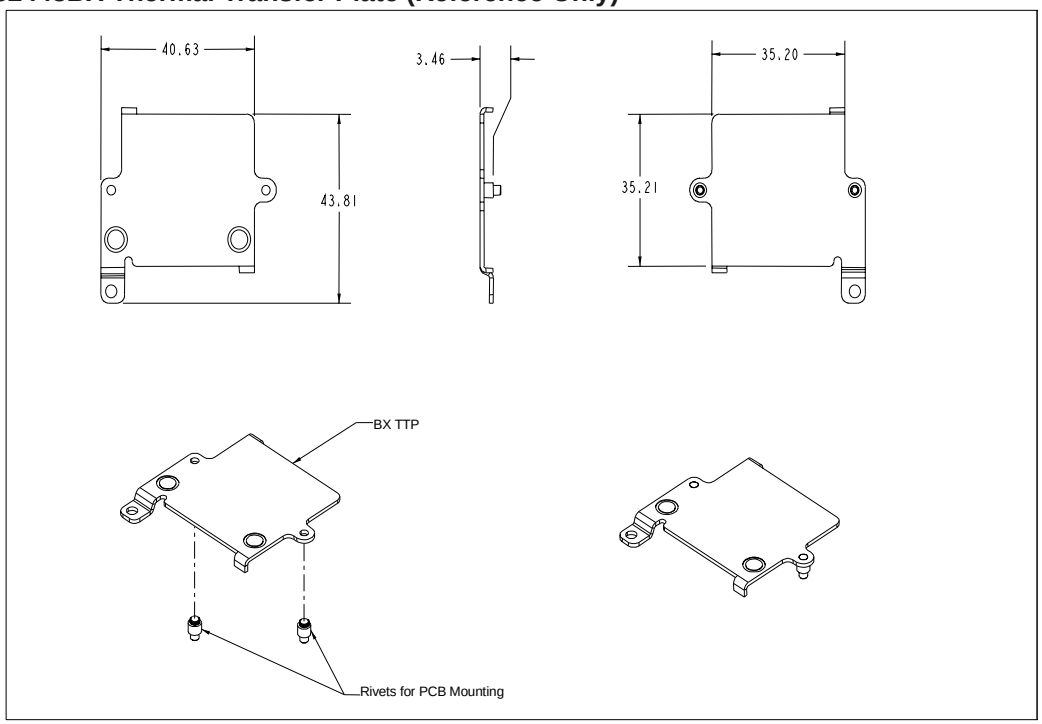


Figure 22. 82443BX Thermal Transfer Plate Detail

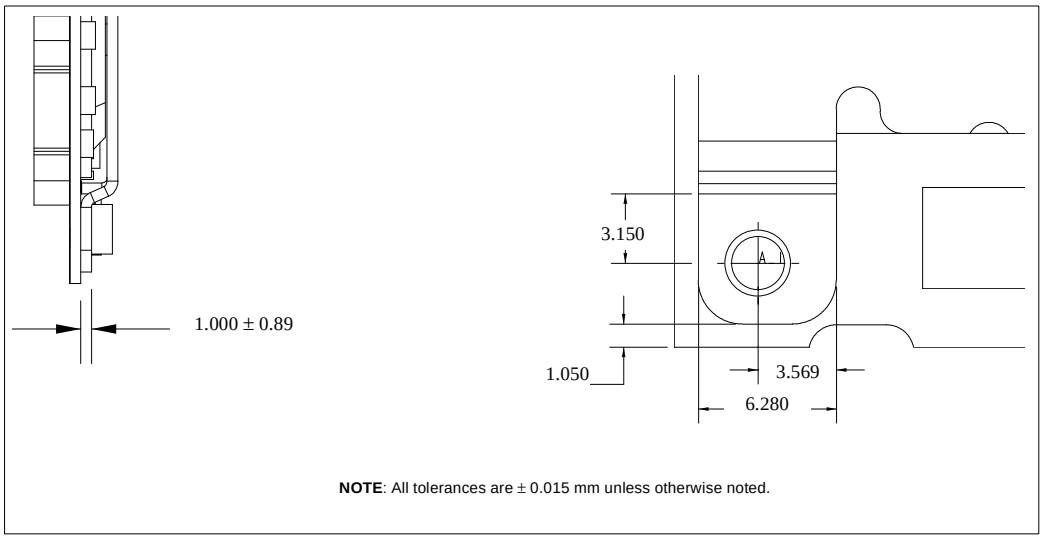
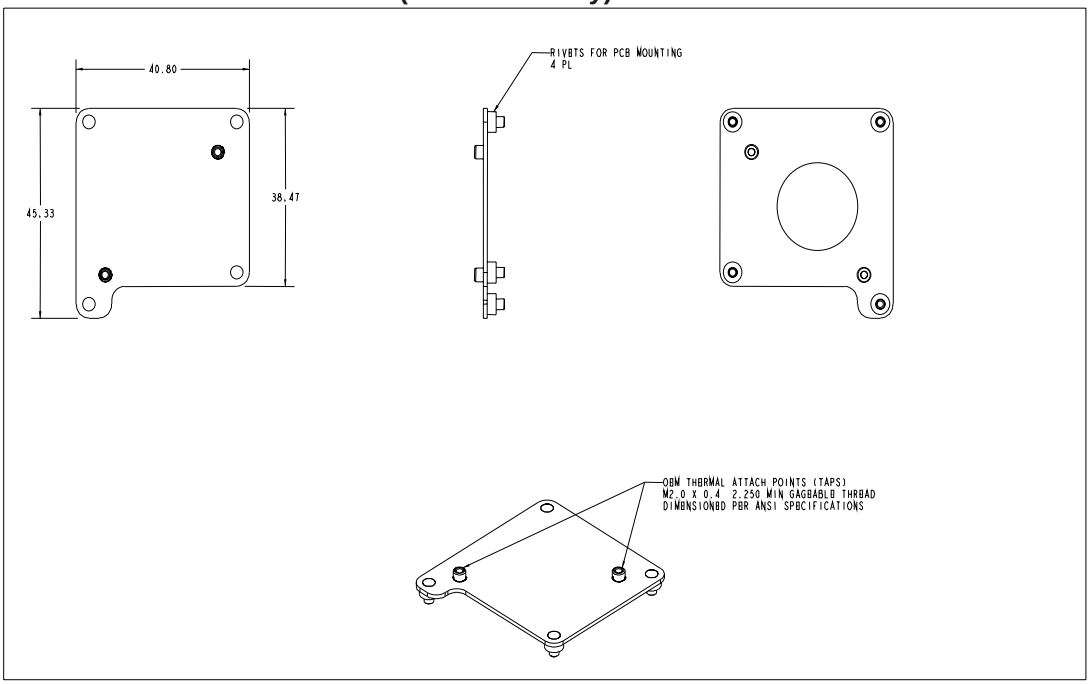


Figure 23. CPU Thermal Transfer Plate (Reference Only)



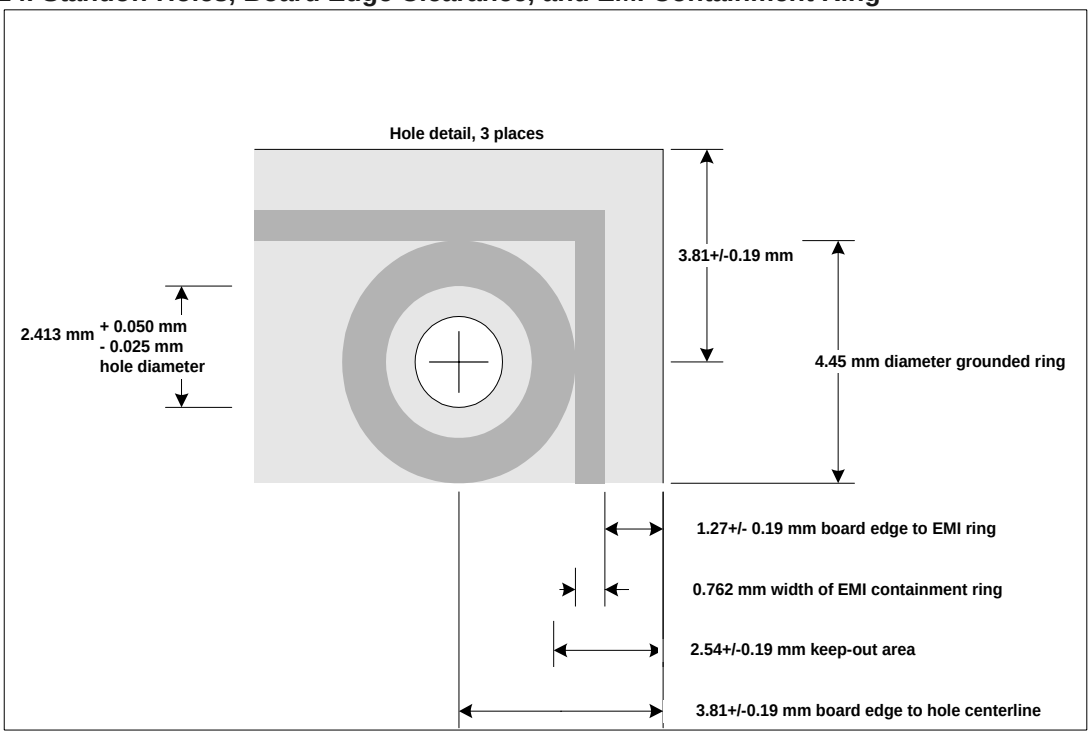
6.3 Mobile Module Physical Support

6.3.1 Mobile Module Mounting Requirements

Three mounting holes are available for securing the mobile module to the system base or the system electronics. See Figure 17 for mounting hole locations. These hole locations and board edge clearances will remain fixed for all Intel mobile modules. All three mounting holes should be used to ensure long term mechanical reliability and EMI integrity of the system. The board edge clearance includes a 0.762-mm (0.030 inches) wide EMI containment ring around the perimeter of the module. This ring is on each layer of the module PCB and is grounded. The hole patterns also have a plated surrounding ring to use a metal standoff for EMI shielding purposes. Standoffs should be used to provide support for the installed mobile module. However, the warpage of the baseboard can vary and should be calculated into the final dimensions of the standoffs used. All calculations can be made with the *Intel® MMC-2 Standoff/Receptacle Height Spreadsheet*. Information on this spreadsheet can be obtained from your local Intel representative.

Figure 24 shows the standoff support hole details, the board edge clearance, and the dimensions of the EMI containment ring. No components are placed on the board in the keep-out area.

Figure 24. Standoff Holes, Board Edge Clearance, and EMI Containment Ring



6.3.2 Mobile Module Weight

The Celeron processor mobile module weighs approximately 56 grams.

7.0 Thermal Specification

7.1 Thermal Design Power

The power handling capability of the system thermal solution may be reduced to less than the recommended typical Thermal Design Power (TDP) as shown in Table 28 with the implementation of firmware/software control or "throttling" that reduces the CPU power consumption and dissipation. The typical TDP is the typical power dissipation under normal operating conditions at nominal V_CORE (CPU power supply) while executing the worst case power instruction mix. This includes the power dissipated by all of the relevant components. During all operating environments, the processor junction temperature, TJ, must be within the specified range of 0° C to 100 ° C.

Table 28. Thermal Design Power (TDP $_{MODULE}$) Specification

Symbol	Typical 700 MHz	Typical 650 MHz	Typical 600 MHz	Typical 450 MHz	Typical 500 MHz	Typical 550 MHz
TDP $_{Module}$	19.1W	17.8W	16.6W	14.1W	15.0W	15.4W

NOTES:
1. During all operating environments, the processor temperature, T_j, must be within the special range of 0 °C to 100°C.
2. TDP_{Module} is a thermal solution design reference point for thermal solution readiness for total module power.
3. Module equals core + 82443BX + VR.

8.0 Labeling Information

Intel mobile modules are tracked in two ways. The first is by the product tracking code (PTC). Intel uses the PTC label to determine the assembly level of the mobile module. Figure 25 shows where PTC can be found on the module. The PTC contains 13 characters and provides the following information.

Example: PMN700001201AA

Key: AABCCCDDEEEFF

Definition:

AA- Processor Module = PM

B- Celeron Processor (.18µ) Mobile Module = N

CCC- Speed Identity = 700 MHz, 650 MHz, 600 MHz, 550 MHz, 500 MHz, and 450 MHz

DD- Cache Size = 01 (128K)

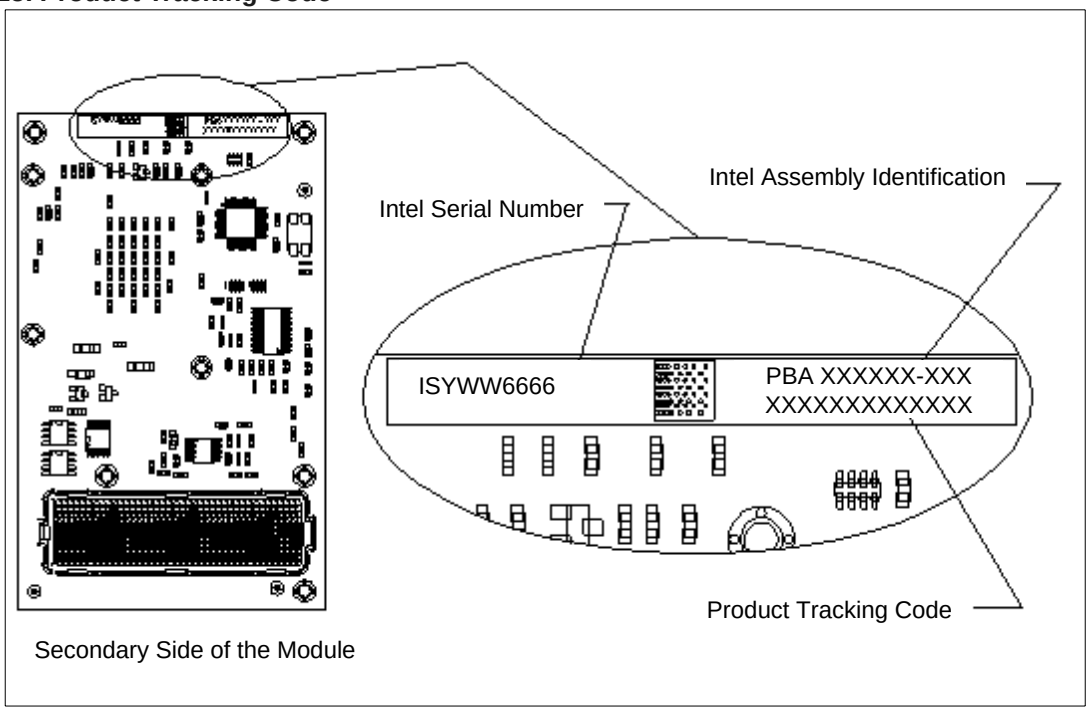
EEE- Notifiable Design Revision (Start at 001)

FF- Notifiable Processor Revision (Start at AA)

Note: For other Celeron processor mobile modules, the second field (B) is defined as:

- Celeron Processor Mobile Module (MMC-1) = H
- Celeron Processor Mobile Module (MMC-2) = I
- Pentium® II Processor Mobile Module (MMC-1) = D
- Pentium II Processor Mobile Module (MMC-2) = E
- Pentium II Processor Mobile Module With On-die Cache (MMC-1) = F
- Pentium II Processor Mobile Module With On-die Cache (MMC-2) = G
- Pentium III Processor Mobile Module (MMC-2) = L
- Pentium III Processor Mobile Module Featuring Intel SpeedStep Technology (MMC-2) = M

Figure 25. Product Tracking Code



The second tracking method is by a generated software utility. Four strapping resistors located on module determine its production level. If connected and terminated properly, up to 16 module-revision levels can be determined. A generated software utility can then read these ID bits with CPU IDs and stepping IDs to provide a complete module manufacturing revision level. For current PTC and module ID bit information, please refer to the latest Intel mobile module product change notification (PCN) letter, which can be obtained from your local Intel Field Representative.

9.0 Environmental Standards

The environmental standards are defined in Table 29.

Table 29. Environmental Standards

Parameter	Condition	Specification
Temperature Cycle	Non-operating Operating	-40 °C to 85 °C 0 °C to 55 °C
Humidity	Unbiased	85% relative humidity at 55°C
Voltage	V_5 V_3	5.0V ± 5% 3.3V ± 5%
Shock	Non-operating Unpackaged Packaged Packaged	Half Sine, 2G, 11 mS Trapezoidal, 50G, 11 mS Inclined impact at 5.7 feet/S Half Sine, 2 msec at 36 inches simulated free fall
Vibration	Unpackaged Packaged Packaged	5 Hz to 500 Hz, 2.2-gRMS random 10 Hz to 500 Hz, 1.0 gRMS 11,800 impacts 2 Hz to 5 Hz (low frequency)
ESD Damage	Human Body Model	Non-powered test of the mobile module only for non-catastrophic failure. The mobile module is tested at 2 kV and then inserted in a system for functional test.