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## Intel<sup>®</sup> IXP455 Network Processor

Ideal for communications and embedded networking applications

#### **Product Highlights**

- Member of the Intel® IXP4XX product line of network processors for Small-to-Medium Enterprise (SME) communications and embedded networking applications
- High-performance Intel XScale® core speeds of up to 533 MHz provide scalable processing headroom to flexibly support a broad range of OEM applications while minimizing power consumption
- Integrated hardware acceleration for cryptography speeds encryption and authentication for security applications
- Built-in LAN and WAN, I<sup>2</sup>C, and Synchronous Serial Port (SSP) interfaces reduce overall system cost and simplify development
- Integrated DDR1-266 SDRAM controller for higher data throughput
- Consistent Intel IXP4XX product line software and hardware architecture protects customers' development investments and speeds deployment of a standards-based product portfolio

### **Product Overview**

The highly integrated, single-chip design of the Intel® IXP455 network processor provides a unique combination of performance, reliability, and flexibility, and extends Intel XScale technology into a broad range of applications that require built-in communications functionality such as networking gateways, security appliances, interactive clients, test and instrumentation, RFID readers, and networked print imaging applications. The Intel IXP455 network processor is supported by a robust application development environment for the Intel IXP4XX product line. This includes pre-integrated and pre-validated development infrastructures and operating systems, development platforms, software components, and debug tools from Intel, members of the Intel® Communications Alliance, and other third-party providers.



#### Consistent Intel® IXP4XX Product Line Architecture for Application Flexibility and Ease of Development

The Intel IXP455 network processor shares a unique distributed processing architecture with the rest of the IXP4XX product line, helping to speed development for a range of applications. Each processor combines a high-performance Intel XScale core with additional Network Processor Engines (NPEs), running their instruction streams in parallel, to achieve wire-speed packet processing performance. The Intel XScale core is compliant with Intel® StrongARM\* Version 5TE. Designed using Intel® 0.18-micron process technology, the core delivers a high MIPS/power consumption ratio and provides ample processing headroom for value-added software features.

The three NPEs in the Intel IXP455 network processor are designed to complement the Intel XScale core for many computationally intensive data plane operations, including IP header inspection and modification, packet filtering, packet error checking, checksum computation, and flag insertion and removal. The NPE architecture includes an ALU, self-contained internal instruction and data memories, and an extensive list of I/O interfaces, together with hardware acceleration elements. The hardware acceleration elements associated with each NPE target a set of networking applications, providing an increase to the speed of specific networking tasks that would otherwise take many MIPS to complete by a stand-alone RISC processor.

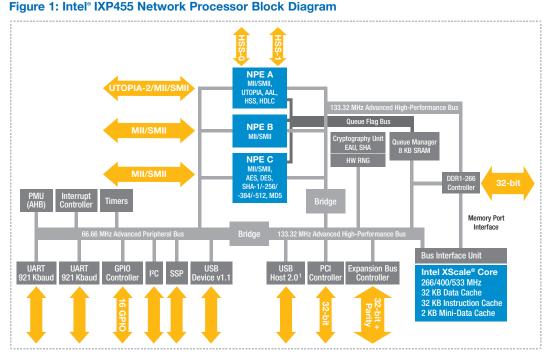
See Figure 1 for a block diagram of the Intel IXP455 network processor. A 10/100 Ethernet interface is attached to each NPE, which is capable of handling 100 Mbps, full-duplex Ethernet packet filtering, and each NPE can support Layer 2 and, in some cases, Layer 3 packet classification and processing. For example, NPE A has two High-Speed Serial (HSS) ports as well as one UTOPIA-2 interface which enable it to handle AAL (1/2/5) Segmentation and Reassembly (SAR) functions. NPE C also has three hardware acceleration elements to speed encryption and authentication for security applications. The extensive hardware capabilities of the NPEs are under the control of microcoded algorithms that are accessed via Application Programming Interfaces (APIs) released as a software library with the processor. Customer applications configure and interact with the NPEs through the high-performance API layer running on the Intel XScale core. Sample "codelets" demonstrate how to use each service or function provided by the Intel XScale core library and the underlving hardware.

#### Highly Integrated Design Lowers System Cost

On-chip integration of a wide variety of functions and commonly used interfaces saves the cost of implementing separate devices and enables easier integration with other hardware. The Intel XScale core includes integrated multiply-and-accumulate functions that support multimedia processing without the need for external hardware. The Intel IXP455 network processor solution includes a floating-point library, a powerful DSP software library, and robust general and multimedia signal processing kernels optimized for maximum performance on the Intel XScale core. To further reduce total chip count, the processor includes an integrated DDR1-266 SDRAM controller, interrupt controller, GPIO port, UARTs, watchdog timer, and general-purpose timers. To further reduce system cost the IXP455 network processor features a USB version 1.1-device controller, a USB 2.0 low-speed and full-speed compatible host-only controller, UTOPIA-2 interface and two HSS ports. Peripheral devices can be directly connected through a 32-bit expansion bus interface that supports external mastering capability and optional byte-wide parity configuration. The PCI 2.2 host and option interface provide the flexibility to directly connect to a variety of devices.

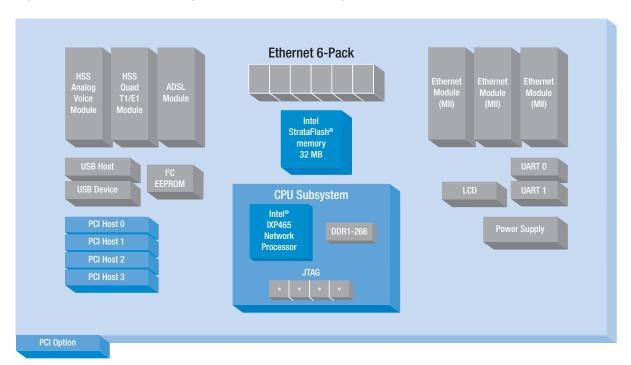
#### Integrated Security Hardware Acceleration Elements

The IXP455 network processor includes integrated hardware acceleration for security applications by implementing popular IPSec cryptography algorithms such as AES, single-pass AES-CCM, and DES/3DES, which support a variety of VPN and wireless (WEP, WEP2, WPA, and WPA2) protocols. Supported authentication algorithms include MD-5, SHA-1, SHA-256, SHA-384, and SHA-512. (Inclusion of SHA-384 and SHA-512 allows 256-bit key authentication to pair with 256-bit AES support.) Using the NPE for dedicated hardware acceleration enables the processing of cryptography and authentication algorithms to be offloaded from the Intel XScale core. The Intel XScale core API calls allow the cryptography and authentication elements to be used by any interface within the



<sup>1</sup>USB 2.0 host supports low-speed (1.5 Mbps) and full-speed (12 Mbps) modes.

#### Figure 2: Intel® IXDP465 Development Platform Block Diagram



IXP455 network processor. This provides maximum flexibility for all interfaces, especially when dealing with security issues over wireless. The IXP455 network processor also includes hardware to accelerate public key exchange, digital signatures, and key generation algorithms.

#### **Operating Systems, Tools, and Applications Support Rapid Development**

The Intel® IXP400 software solution provides a common software framework for the IXP455 network processor, and the Intel® IXP46X and Intel® IXP42X product lines of network processors. Intel IXP455 network processor-based solutions build on the current IXP42X-based ecosystem and code investment, providing customers with a broad range of development tools and applications, together with support for multiple operating systems.

- Intel® IXP400 Software v2.0
- Intel® IXP400 DSP Software
- Intel® IXP400 Software Floating-Point Library v2.0
- MontaVista Linux Professional Edition 3.1\*
- Wind River VxWorks\* Developers Toolkit (VDT) 2.2.1
- Wind River Platform for Network Equipment (PNE) 2.1\*
- Red Hat RedBoot\* and Tool Chain v2.0

#### Intel<sup>®</sup> IXDP465 Development Platform for Faster Time-to-Market

The Intel® IXDP465 development platform is a powerful tool for development and verification of hardware and software for the Intel IXP455 network processor. Developers can use this flexible and extendable platform to conduct rapid initial chip assessment, performance evaluation, prototyping, and product development. See Figure 2 for a diagram of the development platform. Optional modules include:

- HSS<sup>2</sup> analog (4-FXS, 1-FXO) voice module
- HSS<sup>2</sup> quad T1/E1 module
- One ADSL or UTOPIA-2<sup>2</sup> module
- Two additional Ethernet MII<sup>2</sup> modules

#### Intel<sup>®</sup> Communications Alliance

With Intel® development platforms, developers can design comprehensive systems combining products from Intel and third-party vendors to accelerate time-to-market and reduce development costs. For more information on third parties in the Intel® Communications Alliance who support Intel network processors and their development environment, visit: www.intel.com/go/ica

<sup>2</sup>Requires Intel<sup>®</sup> IXP400 software.

Features	Benefits
Intel XScale $^{\circ}$ core available at 266, 400, and 533 MHz	Delivers high MIPS/power consumption ratio and provides ample processing headroom for value-added software features
32-bit 33/66 MHz PCl v2.2-compatible, host and option interface	Provides flexibility to directly connect devices including 802.11x chips, PCMCIA controllers, and cable MAC/PHYs
<ul> <li>USB v1.1 device controller</li> <li>USB v2.0 host controller, supports low-speed and full-speed modes only</li> </ul>	Industry-standard interface for connection to a wide array of devices
32-bit, DDR1-266 SDRAM interface for 32 MByte to 1 GByte of memory	High-bandwidth memory interface
<ul> <li>32-bit expansion bus interface with parity</li> <li>Master/Target capable</li> <li>25-bit address</li> </ul>	<ul> <li>Glueless connection to other devices</li> <li>External mastering capability allows external devices to communicate with each other and with internal peripherals resulting in shared memory subsystem design and lower system cost</li> </ul>
Up to three integrated 10/100 Ethernet MACs with MII interface	<ul> <li>Industry-standard networking interface</li> <li>Multiple ports allow lower system cost, multiple LAN port support, and concatenation of networking modules</li> </ul>
UTOPIA-2 interface with multiple ADSL/G.SHDSL or VDSL PHY support	Industry-standard WAN interface
Two High-Speed Serial (HSS) ports for connecting to T1/E1 or SLIC/CODEC	Connects to T1/E1 or SLIC/CODEC for voice support
Silicon functional assistance for Random Number Generation	Accelerates public key exchange, authentication and key generation
Integrated hardware support for popular cryptography algorithms	Acceleration for popular applications such as IPSec and SSL VPNs (AES/AES-CCM/3DES/DES/SHA-1/SHA-256/ SHA-384/SHA-512/MD-5/RSA/DSA/Diffie-Hellman algorithms)
Two high-speed UARTs support up to 921 Kbaud each	Provides an interface for debug and passing control information
Integrated I <sup>2</sup> C and SSP interfaces	Provides serial interface for common embedded and communications application; reduces system BOM
Spread-spectrum clocking	Improves system reliability by reducing EMI
Comprehensive pre-validated, pre-integrated "out-of-the-box" development infrastructures ready for application development using Linux* and VxWorks*	Ease of design and fast time-to-market
<ul> <li>544-ball PBGA package</li> <li>35 mm x 35 mm, 1.27 mm ball pitch</li> <li>Lead-free packages available</li> <li>Commercial temperature (0° to 70° C)</li> <li>Extended temperature (-40° to 85° C)</li> </ul>	<ul> <li>High-performance package provides improved reliability</li> <li>Lead-free packages help meet environmental regulations</li> <li>Extended temperature support for industrial control and automation applications</li> </ul>

#### **Intel Access**

Developer's Site	developer.intel.com
Intel® Network Processors Web page	www.intel.com/go/networkprocessors
Intel in Communications	http://intel.com/communications
Intel® Technical Document Center	http://www.intel.com/go/techdoc (800) 548-4725 7 a.m. to 7 p.m. CST (U.S. and Canada) International locations please contact your local sales office.
General Information Hotline	(800) 628-8686 or (916) 356-3104 5 a.m. to 5 p.m. PST

UNITED STATES AND CANADA Intel Corporation Robert Noyce Bldg. 2200 Mission College Blvd. P.O. Box 58119 Santa Clara, CA 95052-8119 USA EUROPE Intel Corporation (UK) Ltd. Pipers Way Swindon Wiltshire SN3 1RJ UK

ASIA-PACIFIC Intel Semiconductor Ltd. 32/F Two Pacific Place 88 Queensway, Central Hong Kong, SAR JAPAN Intel Japan (Tsukuba HQ) 5-6 Tokodai, Tsukuba-shi 300-2635 Ibaraki-ken Japan SOUTH AMERICA Intel Semicondutores do Brazil LTDA Av. Dr. Chucrl Zakian, 940-10° andar 04583-904 São Paulo-SP Brazil

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The Intel® IXP455 Network Processor may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available upon request.

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