EECS 270

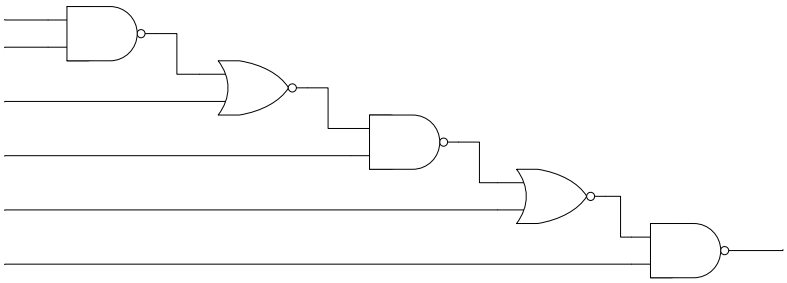
Homework #4

1. Given the circuit below and the following gate propagation delays:

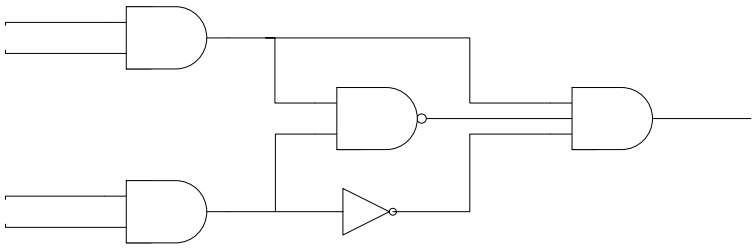
$$t_{pHL}^{NAND} = 0.5ns \qquad t_{pHL}^{NOR} = 1.0ns$$
$$t_{pLH}^{NAND} = 0.75ns \qquad t_{pLH}^{NOR} = 1.25ns$$

Compute $t_{pHL}^{A \rightarrow Q}$ and $t_{pLH}^{A \rightarrow Q}$ under the following input combination **(2)**:

B = 1, C = 0, D = 1, E = 0, F = 1



2. Given the circuit below with inverter delays $t_{pHL} = t_{pLH} = 1ns$ and all other delays $t_{pHL} = t_{pLH} = 2ns$:



   a) Assume that A has a rising transition (i.e., A = 0 → 1). What fixed input values are necessary on B, C, and D such that there is a transition at the output Q? What is the propagation delay $t_{pLH}^{A \to Q}$? **(2)**
   b) What are $t_{pHL}^{C \to Q}$ and $t_{pLH}^{C \to Q}$, given inputs A = B = D = 1? Show a timing diagram for each case. **(2)**
   c) Is this circuit free of static hazards? Explain.
   **** Note that this is not a 2 level circuit, so the K-map analysis covered in class does not apply here. **** **(1)**

3. page 303, 4.22 d, e, g **(3)**

4. page 74, 2.2 b, d, f **(3)**

5. Perform the following number conversions: **(2)**

   a) $317_8 = ?_2$
   b) $46701_8 = ?_{16}$
   c) $10\ 0101\ 0011.0101_2 = ?_{10}$
   d) $117.375_{10} = ?_{16}$

A

B

C

D