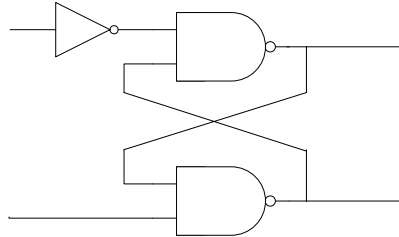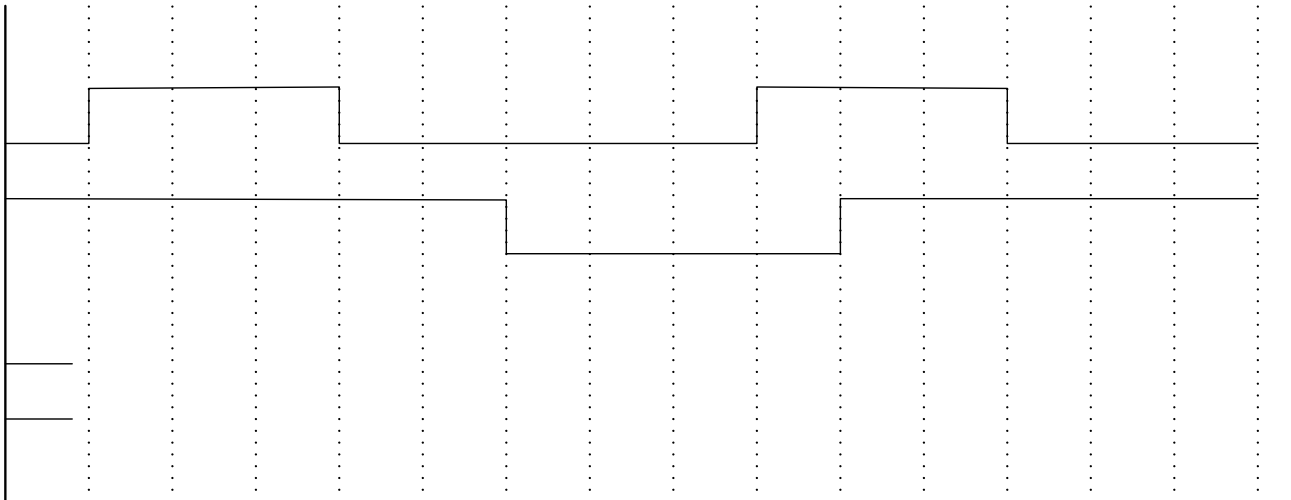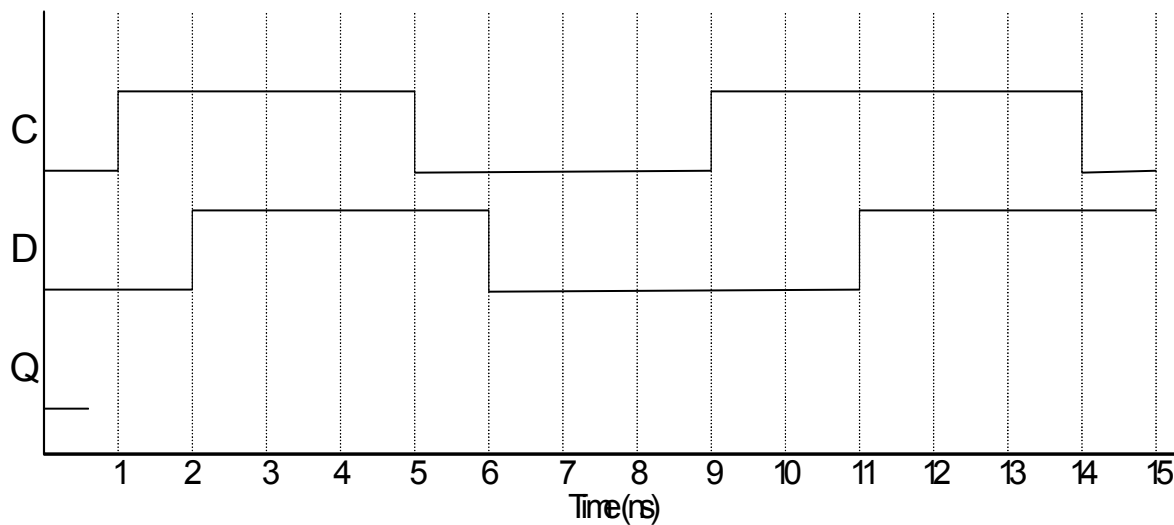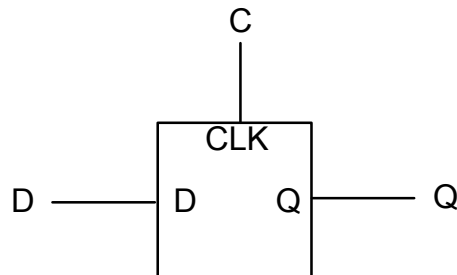# EECS 270

Homework #7

1. (a) Using the above circuit, and given the waveforms for inputs X and
    Y below, complete the waveforms for Q and QB. Assume the delay of
    each gate is 1ns. Show all causality arrows. (**4**)

(b) For what values of inputs X and Y are the outputs Q and QB not
complements of each other? (**2**)

2. (a) Complete the following timing diagram for the D latch below. Assume that for this latch, $t^{CLK \to Q}_{pHL} = t^{CLK \to Q}_{pLH} = 1ns$ (latch delay from input CLK to Q), and $t^{D \to Q}_{pHL} = t^{D \to Q}_{pLH} = 2ns$ (latch delay from input D to Q). **(3)**

3. Consider a chain of six scan flip-flops: SF1 through SF6, connected as follows:

$$TI \rightarrow SF1 \rightarrow SF2 \rightarrow SF3 \rightarrow SF4 \rightarrow SF5 \rightarrow SF6 \rightarrow TO$$

(a) How many cycles with TE = 1 are needed to read the states of all flip-flops? **(1)**

(b) If SF2 is broken (i.e., has a manufacturing fault), how many cycles with TE = 1 are necessary to detect this with one test vector? (Do not include the cycles needed to scan in the test pattern). **(1)**

(c) Is it possible to reliably say whether SF2 is broken by comparing the output bits read off TO with what's expected when there are no faults? **(1)**

4. Given the J-K flip-flop below, hook up the inputs (adding any necessary gates) such that it behaves logically like a negative-edge triggered D flip-flop, also shown below. **(3)**

J   Q —— out

K   QB —— outB