EECS 312: Digital Integrated Circuits
Homework #4

Reading: 6.1-6.3

1. **Pseudo-NMOS Gates**: Consider a 3-input NOR gate implemented in pseudo-NMOS driving a dynamic gate. For the PMOS device in the NOR gate, let W_p=1.05μm and L_{eff} = 0.2μm. For each of the NMOS devices, let L_{eff} =0.2μm.
   - **a.** Solve for the W_n of each NMOS device (all sized equally), such that the rising delay of the pseudo-NMOS gate is minimized without violating the noise margin of the dynamic gate.
   - **b.** Find all possible values of V_{OL} (depending on input patterns) using the sizes from part A.
   - **c.** What is the average static power consumption of the pseudo-NMOS gate if all input combinations are equally likely? Use the sizes obtained in part A and ignore channel-length modulation (meaning Id will not be a function of V_{ds} in saturation) to simplify the calculations.

2. **Pass Transistor Logic:** Consider the circuit in Figure 4.1. Assume the inverter switches ideally at VDD/2, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.
   - **a.** What is the logic function performed by this circuit? (Write a function for OUT)
   - **b.** Explain why this circuit has non-zero static power dissipation.
   - **c.** Using only 1 transistor, design a fix to the *pass transistor* design so that there will not be any static power dissipation in the circuit. Qualitatively explain how you would choose the size of the transistor.
   - **d.** Implement the same function using *transmission gates*.
   - **e.** Replace the pass-transistor network in Figure 4.1 with a *pass transistor* network that computes the following function: *x* = *ABC* at the node x. Assume you have the true and complementary versions of the three inputs A,B and C.

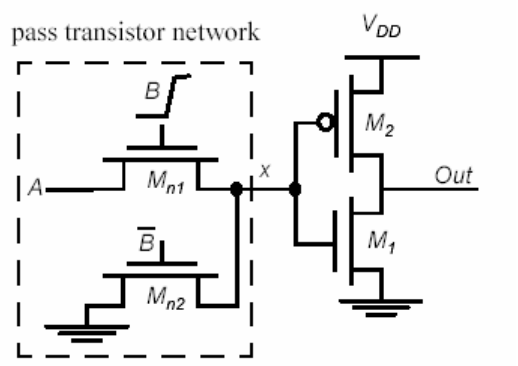

Figure 4.1

3. **Dynamic Logic:** Consider the domino gate below in Figure 4.2.
   - **a.** Determine the logic function OUT.
   - **b.** Let the NMOS devices in the dynamic gate have W=3μm and minimum channel length (sizes are notated on Figure 4.2). The inverter has W_n=2μm and W_p=4μm (also L_{min}). To calculate junction capacitances, assume that Csb = Cdb = 0.6 fF/μm of device width for both NMOS and PMOS devices. Calculate C_{gc} only at the input to the static CMOS inverter. Ignore overlap capacitances in this entire problem. Determine the reduction in voltage at the input to the inverter under worst-case charge sharing conditions.
   - **c.** Besides reliability problems, what is the least desirable side-effect of charge sharing in dynamic circuits similar to the gate in Figure 4.2? Briefly explain.

d. Sweep β of the inverter from 0.5 to 10 (keep (W_p + W_n) the same) and plot t_{plh} (defined from the inputs A,B,C,D to node OUT). Let there be a capacitor of 50 fF (C_L) on node OUT (don't calculate any capacitances) and assume a wiring capacitance of 8 fF (C_W) on the dynamic node. Use the capacitance approximations from part B for junction and gate capacitances. Assume the clock is in the evaluate phase and *inputs A, B and C transition high simultaneously (step inputs) while D remains low.* Also consider the input transition time dependency of the delay through the inverter. Use the linearized model for this with K=0.15.

e. Using Figure 4.7 and results from D, what is a good β ratio for the static inverter in Figure 4.2?

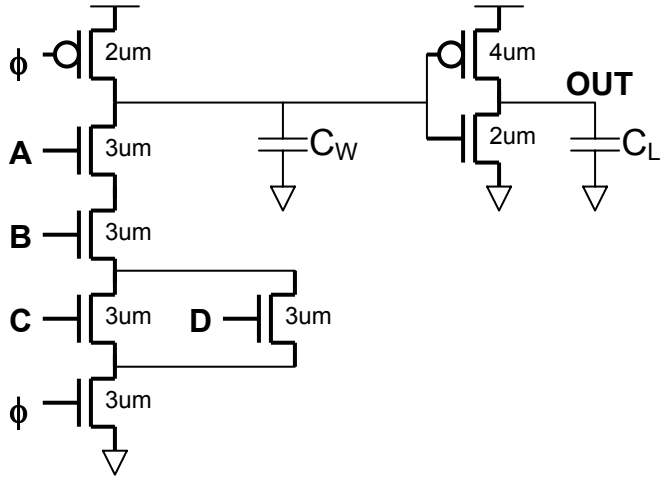

Figure 4.2

4. Dynamic Logic: Consider a conventional 4-stage Domino logic circuit as shown in Figure 4.3 in which all pre-charge and evaluate devices are clocked using a common clock ϕ. For this entire problem, assume that the pull-down network is simply a single NMOS device, so that each Domino stage consists of a dynamic inverter followed by a static inverter. Assume that the pre-charge time, evaluate time, and propagation delay of the static inverter are all *T*/2. Assume that the transitions are ideal (zero rise/fall times).

a. Draw a timing diagram for signals *Out1*, *Out2*, *Out3* and *Out4*, when the *IN* signal goes high before the rising edge of the clock ϕ. Assume that the clock period is 10 T time units.

b. Suppose that there are no evaluate transistors at the 3 latter stages. Assume that the clock ϕ is initially in the pre-charge state (ϕ=0 with all nodes settled to the correct pre-charge states), and the block enters the evaluate period (ϕ=1). Is there a problem during the evaluate period, or is there a benefit? Explain.

c. Suppose that there are no evaluate transistors at the 3 latter stages. Assume that the clock ϕ is initially in the evaluate state (ϕ=1), and the block enters the pre-charge state (ϕ = 0). Is there a problem, or is there any benefit, if the last three evaluate transistors are absent? Explain.

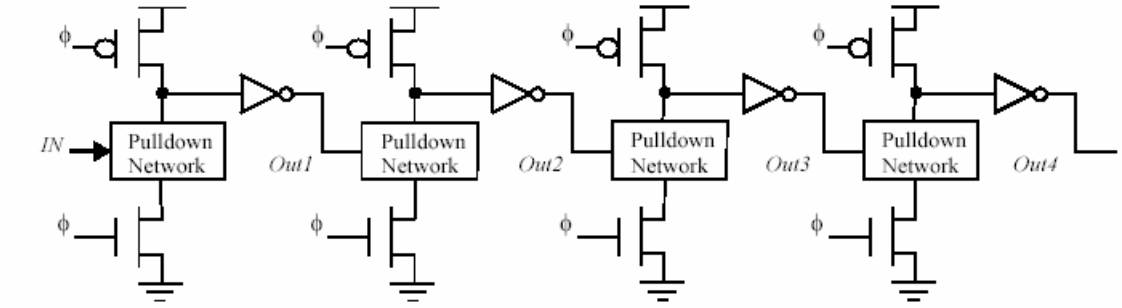

Figure 4.3

5. **Combinational Gates:** Use default parameters unless alternate values are given.
   - **a.** Determine the worst case t_{pHL} and t_{pLH} transitions in the complex gate given in Figure 4.4. Indicate an initial and final input pattern in each case. Calculations are not required.
   - **b.** Write a logic equation for the complex gate in Figure 4.4.

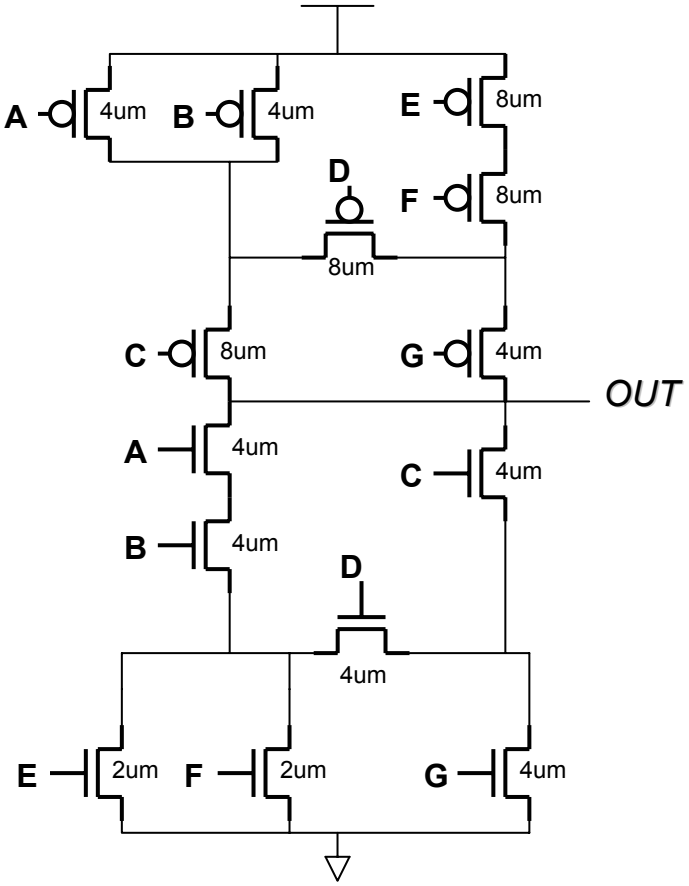

Figure 4.4

   - **c.** Consider a stack of 3 NMOS devices in series connected to ground (as in a 3 input NAND). Calculate the delays (Elmore delay) for an initial sizing of 4, 4, 4μm and a stack tapered sizing of 3.5, 4 and 4.5μm (see Figure 4.5 below). Assume that C_L=20fF includes all relevant capacitances at the output node and you may use the 0.6fF/um of device width approximation for C_{db}/C_{sb}. What percent improvement is seen when stack tapering is used?
   - **d.** If the output load of the gate in part C is increased 10X to 200fF, does stack tapering become *more* useful or *less* useful? Briefly explain your answer (*no calculations required*).

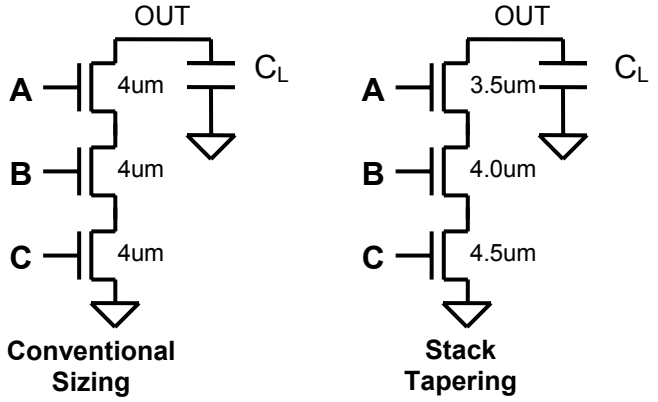

Figure 4.5

6. **Transmission Gate Logic:** A simplistic implementation of a 12 input AND/NAND enabled gate using transmission gate logic is implemented by chaining 12 complementary transmission gates in series. Each transmission gate has a fixed size *0.5μm PMOS device and 0.5μm NMOS device*. Inverters may be inserted into the chain of transmission gates to improve the delay of the chain. A standard *1μm PMOS, 0.5μm* NMOS static CMOS inverter is available to insert (at various points) into the chain to optimize the delay of the gate. There is an error in the text regarding the resistance of a transmission gate (Eq 6.34) that is corrected below in Figure 4.6. Calculate the R_{eq} at 1.25 V for the transmission gate. Calculate t_{pbuf} as the average delay of an inverter driving itself (consider C_{gc} and use the 0.6fF/um approximation to calculate junction capacitances – do not consider overlap capacitance).

$$R_n = \frac{V_{DD} - V_{out}}{I_{Dn}} = \frac{V_{DD} - V_{out}}{k'_n \left(\frac{W}{L}\right)_N \left((V_{DD} - V_{out} - V_{Tn}) V_{DSATn} - \frac{V_{DSATn}^2}{2} \right)}$$
$$\approx \frac{V_{DD} - V_{out}}{k_n (V_{DD} - V_{out} - V_{Tn}) V_{DSATn}}$$

Figure 4.6 (Eq. 6.34)

a. How many inverters need to be inserted into the chain to obtain the optimal delay, given the fixed sizes given above? Ignore the output polarity of the gate, either NAND or AND functionality is acceptable at the output.

b. What is the optimal delay obtained from part A.

c. Given a delay constraint of 260 ps (from input to output), how many inverters should be inserted to minimize the energy subject to the delay constraint? Ignore the output polarity of the gate, either NAND or AND functionality is acceptable at the output.

EECS 312 HW4: Noise Margin vs. Beta Ratio

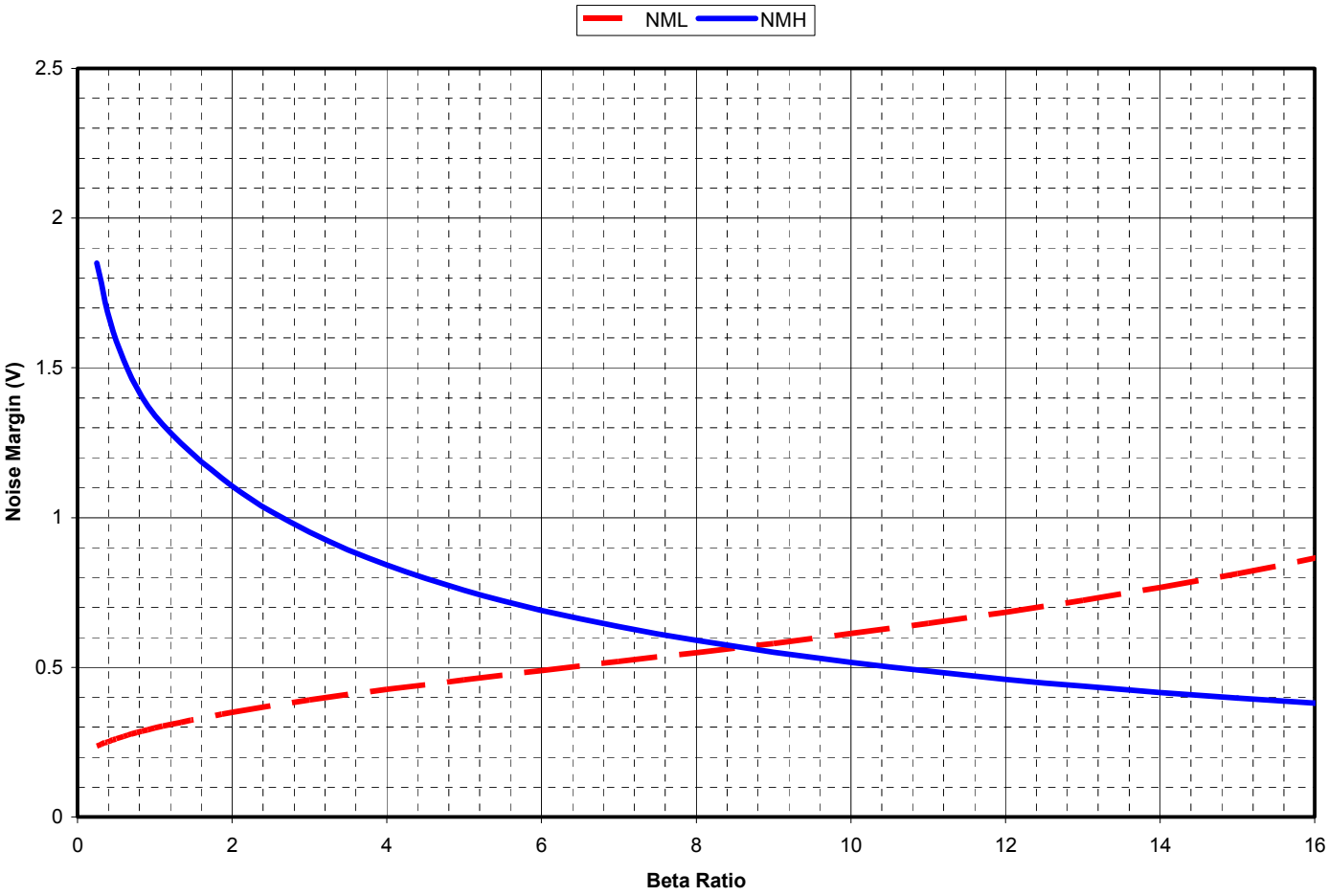

Figure 4.7

(Disclaimer: *do not refer to this noise margin chart for anything other than this homework*)