Lab 4
Dynamic Logic and Sequential Circuits

Objectives:

(1) Analysis of charge sharing, feedthrough, and charge leakage in dynamic logic and the effectiveness of keepers on the performance of domino logic.
(2) Estimation of Setup time of a static D-latch, and delay comparison of a static and dynamic D-latch.

PART 1 : Dynamic Logic Analysis

Create a schematic (as shown in Fig. 1) of a 2-input dynamic NAND gate loaded with a CMOS inverter (domino logic). Place a 20fF capacitance at node X, a 2fF capacitance at node Y and a 2fF capacitance at node Z. The device properties of all the transistors in this schematic are set to **W=0.5U L=0.25U AS=0.3125P AD=0.3125P PS=1.75U PD=1.75U.**

Note that all the NMOS have their source connected to ground. The body of the NMOS is connected to the lowest voltage and the body of the PMOS is connected to the highest voltage in the circuit. This would ensure that the source-body junction would never get forward biased even though you would see body effect on V_T.

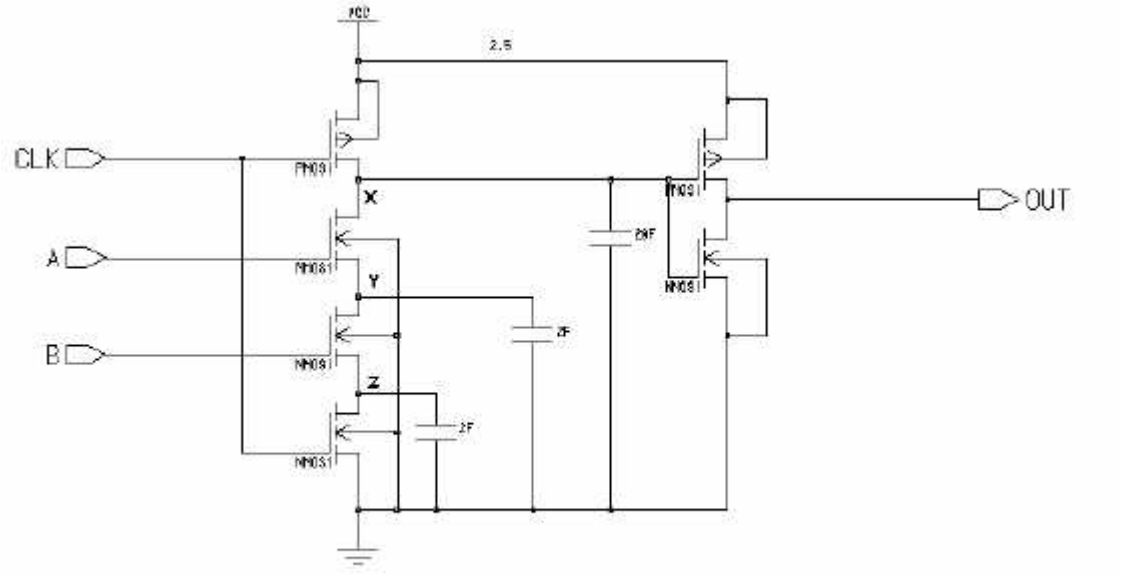

Fig. 1 The schematic of dynamic AND logic

Observing the effects of charge sharing & feedthrough

The phenomena of charge sharing and feedthrough are commonly observed in dynamic logic. These effects tend to result in glitches of the output and internal waveforms. For the schematic shown above, set the waveforms for input ports A, B and CLK (clock) as in Fig. 2. You need to monitor the voltage output at nodes X, Y, Z. The rise times and fall times should be set to 0 for A, B, and CLK.

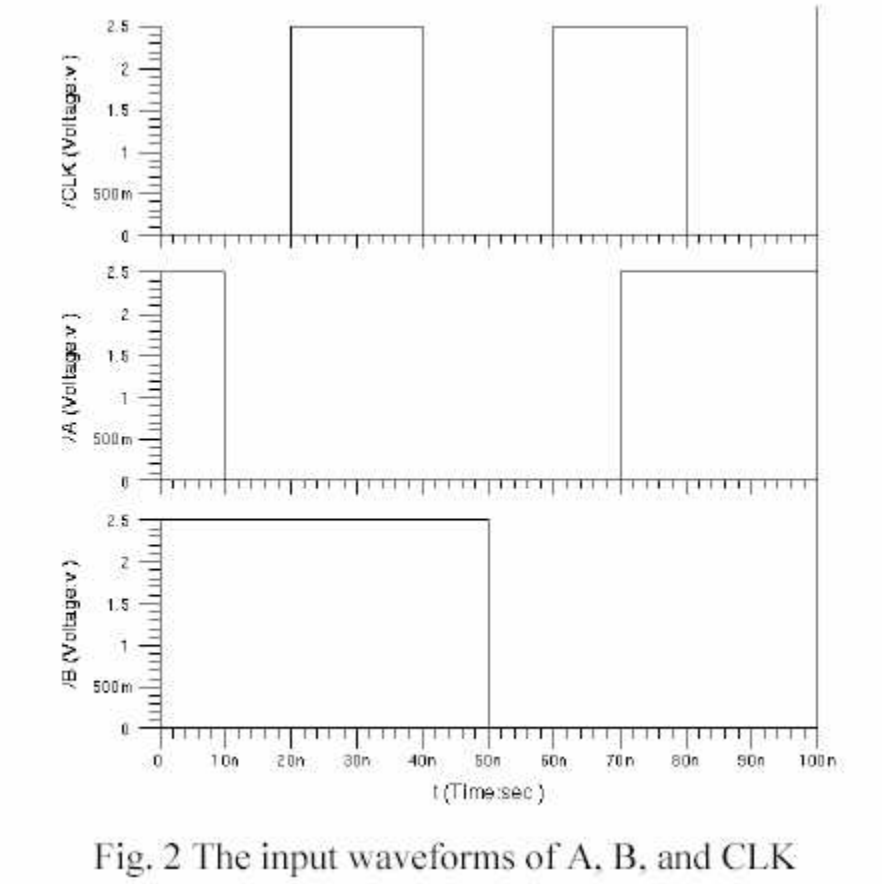

Fig. 2 The input waveforms of A, B, and CLK

Exercise 1:

(1) Plot the voltages at node X, Y, and Z (figure 4-1). You might want to put the voltages of A, B, and CLK in the same plot for easy comparisons.

(2) During the 2nd evaluate phase, input A transitions high while B is low. An obvious charge sharing effect is observed. What are the voltage levels at nodes X and Y as a result? What is your expectation from hand calculation ignoring parasitic device capacitances? Use V_{th} = 0.365 and γ=0.4 for this part to get results close the model file.

(3) Some small glitches are observed in your output waveform. For example at the t = 40 ns, what do you think leads to the observed glitches at nodes Y and Z (be specific)? How do you explain the voltage glitch at node X when t=60 ns.

Simulation of voltage drop due to leakage current

During the evaluation phase, if the pull-down network is not conductive, the output voltage tends to drop due to the leakage currents present. Here, we simulate this behavior using the schematic from Fig. 1. Set up your ***Transient Analysis*** by precharging node X to 2.5V with A = B = 0 V.

Exercise #2:
(1) Plot the voltage at node X versus time (figure 4-2).
(2) What is the final voltage value at node X? Justify qualitatively.
(3) If we can tolerate a voltage drop of 10% of V_{dd} (due to charge leakage) what is the minimum clock frequency allowed for this circuit? (Indicate the relevant measurements with a cursor in figure 4-2).

The function of keeper

If a PMOS (**W=0.5U L=0.25U AS=0.3125P AD=0.3125P PS=1.75U PD=1.75U)** is added to the schematic shown in Fig.1, it can work as a keeper to combat the effects of charge leakage and charge sharing.

Use the following waveforms (as in Fig. 3) for CLK, A and B. Find the pull-up delay t_{pLH} and pull-down delay t_{pHL} for this NAND gate (with keeper). Also do this for the gate without the keeper. Measure delay from the inputs (A,B) to node X.

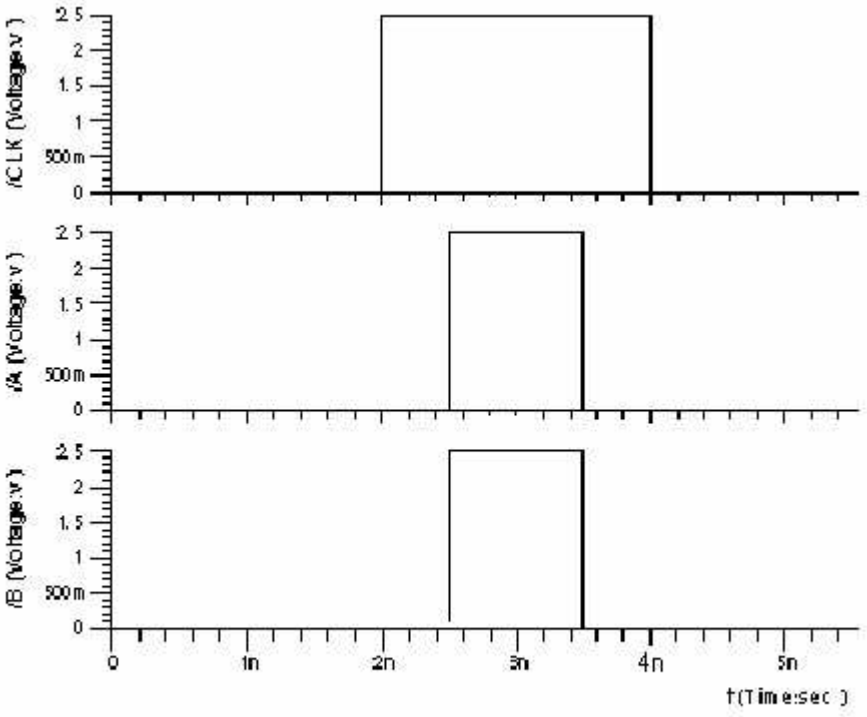

Fig. 3 Input waveform for investigation of delay times

Exercise #3:
(1) Print out the schematic with the keeper included (figure 4-3).
(2) Find t_{pLH} and t_{pHL} for the circuits with the restorer and without the restorer. For t_{pLH}, which one is larger? Is it reasonable? Why (this is tricky!)? What is the relationship between t_{pHL} values? Justify.

Effect of keeper sizing on functionality

In this part, we are interested in finding an upper bound on the width of the keeper. We need to sweep the width of the device and observe the output transition that might be violated on increasing the width.

Use "Design Change" option in accusim to change the width of the keeper to a variable (i.e. in the INSTPAR property box, put W=wp). Then select Setup > Others > Variable and define the variable wp in the variable name box, leave the value box blank and select 'number' for variable type. Define a transient analysis and add appropriate forces to the inputs A and B. Sweep the parameter wp (use sweep – global variable and select wp) and plot output X by selecting Chart > Family of curves. From this plot you should be able to choose a width beyond which the device functions incorrectly. This is the upper bound on the width of the keeper.

Exercise #4:
(1) Submit the 'family of curves' plot of the output X for the values of W swept. Choose the range and step of the sweep for W judiciously so that the plot is not cluttered (figure 4-4).
(2) Describe qualitatively how would the constraint on the keeper width change if β of the inverter (load of dynamic gate) is increased.

PART 2: Comparison of dynamic and static D-latches

Create two schematics for the circuits shown below in Fig.4 (a static and dynamic D-latch). All the PMOS and NMOS transistors have the device properties set as **W=0.5U L=0.25U AS=0.3125P AD=0.3125P PS=1.75U PD=1.75U**

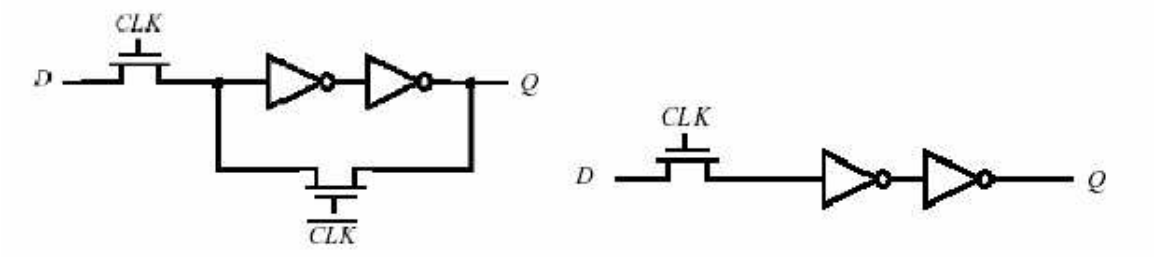

Fig. 4 Static D-latch (left) and dynamic D-latch (right)

Setup time t_{setup} of Static D-latch:

You need to find the setup time t_{setup} for the **static** D-latch only. Note that set-up times can be different for high and low input values (D is the input). Use step inputs for CLK and D to find the 'two' setup time values.

Hint : Use staggered waveforms for D and CLK such that the distance between the edges changes with time. Observe the point where output Q cannot follow D due to setup time violation. A quick inspection of the circuit should give you a starting point/estimate for the setup time (ex: 1 transmission gate delay, 2 inverter delays, their sum?)

Exercise #5:
(1) Plot D, CLK, Q on one chart and zoom in to show 2-3 periods of CLK on each side of setup time violation. Submit two plots corresponding to low and high input (figure 4-5 & 4-6).
(2) What are the values for t_{setup} in the case of a high voltage being captured and a low voltage being captured? (try to be accurate to a few ps).
(3) Determine the best and worst case D-Q delay.
Hint : D-Q delay depends on the arrival time D with respect to CLK.

Delay time comparison of dynamic and static D-latches

You will need to set up the waveforms properly to ensure you measure the correct delays. Use a rise/fall time of 0.5ns for the CLK and D inputs.

Exercise #6:
(1) Measure the CLK-Q delays (tphl and tplh) for both the static and dynamic latches. You need not submit a plot. If you are designing a heavily pipelined high performance system, which latch would you prefer and why ?