EECS 312: Digital Integrated Circuits

Homework #8

Reading: 9.3.3 (Repeater Design), 5.4.3 (Buffer Design), 4.1-4.3 (Wires)

1. **Interconnect and Scaling:** Given an isolated wire (unrealistic) with the given dimensions: W=1.5um, H_{wire}=0.8um, t_{di}=0.5um, $\varepsilon_{ox}=4\varepsilon_o$, L=14mm
   - **a.** What is the total **capacitance** of this wire? Use three models:
     i. The simple rule of thumb presented in lecture
     ii. The detailed empirical equation in Figure 1.1 below.
     iii. Use table 4-2 from Rabaey and assume that this is a 5th-level metal running directly over 4th-level metal.

$$C_{wire} = \varepsilon_{di}\left[\left(\frac{W}{T_{di}}\right) + 0.77 + 1.06\left(\frac{W}{T_{di}}\right)^{0.25} + 1.06\left(\frac{H}{T_{di}}\right)^{0.5}\right]$$

Figure 1.1

   - **b.** What is the total **resistance** of the wire? Use Table 4-4 in Rabaey to find resistivity and calculate the resistance for two metals:
     i. Aluminum (Al)
     ii. Copper (Cu)
   - **c.** Suppose this wire connects a driver and a series of receivers. The driver is a CMOS inverter with $W_p=2W_n=20\mu m$ (L_{min} is used). The receivers are 6 inverters that are equal to the size of the driver. Use the Aluminum resistance calculated in (b) and the capacitance calculated by Figure 1.1 from (a) to calculate this delay (see Lecture 25). What is the propagation delay t_{phl} of this driver? What percentage of the delay is due to the resistance of this wire?
   - **d.** Scale the default process technology and the given wire parameters two generations (where S=1.4 for one generation). Use Copper interconnect and recalculate the t_{phl} from the driver to the receiver described in (c). What is the percentage of delay due to the resistance of this wire?

2. **Repeater Design:** Consider the wire described in problem 1, with the gate load described in (c). Use the capacitance calculated by Figure 1.1 and the resistance of aluminum interconnect for the following questions. Assume default technology (250nm).
   - **a.** Use the tapered buffering approach to driving this wire for optimal delay. Assume that the initial inverter is $W_P=2W_N=2um$ (β is fixed at 2) and that $\gamma=1$. When sizing the chain, ignore resistance. However, when the chain is sized, add the wire delay (including resistance) to the delay of the final stage (see Lecture 25). Find the optimal delay and the total area of the transistors used in the tapered design.
   - **b.** Use the repeater insertion technique (pg. 466-467) to optimize delay. Use the detailed approach of Equation 9.9 and 9.10 in the text. Find the optimal delay and the total area of the transistors used in the repeater based design.
   - **c.** Why is a direct comparison between the results from (a) and (b) unfair as the problem is described?