EECS 312: Digital Integrated Circuits
Homework #2 Solutions

1. K_{eq} Approximation and FO4 Delay:

a) In general, we begin by finding the area and perimeter of the diffusion regions in each of the 5 identically sized devices.

$$AD_n = 2.5 * L_{drawn} * W_n = (0.625um)(0.8um) = 0.5\ um^2$$
$$PD_n = W_n + 2(2.5 * L_{drawn}) = 0.8 + 1.25\ um = 2.05\ um$$
$$AD_p = 2.5 * L_{drawn} * W_p = (0.625um)(1.6um) = 1\ um^2$$
$$PD_p = W_p + 2(2.5 * L_{drawn}) = 1.6 + 1.25\ um = 2.85\ um$$

Case 1

For case 1, the values for a rise time transition and a falltime transition are the same since the transition is over the same voltage range (0.25 to 2.25 V).

$$K_{eq(NMOS,10-90)} = \frac{-(0.9)^{0.5}}{((-2.25)-(-0.25))(1-0.5)}\left[((0.9)-(-2.25))^{0.5} - ((0.9)-(-0.25))^{0.5}\right] = 0.6663$$

$$K_{eqsw(NMOS,10-90)} = \frac{-(0.9)^{0.44}}{((-2.25)-(-0.25))(1-0.44)}\left[((0.9)-(-2.25))^{0.56} - ((0.9)-(-0.25))^{0.56}\right] = 0.6988$$

$$K_{eq(PMOS,10-90)} = \frac{-(0.9)^{0.48}}{((-2.25)-(-0.25))(1-0.48)}\left[((0.9)-(-2.25))^{0.52} - ((0.9)-(-0.25))^{0.52}\right] = 0.6770$$

$$K_{eqsw(PMOS,10-90)} = \frac{-(0.9)^{0.32}}{((-2.25)-(-0.25))(1-0.32)}\left[((0.9)-(-2.25))^{0.68} - ((0.9)-(-0.25))^{0.68}\right] = 0.7694$$

	t_{phl}	t_{plh}	t_{rise}	t_{fall}
NMOS K_{eq}	0.57	0.79	0.6663	0.6663
NMOS K_{eqsw}	0.61	0.81	0.6988	0.6988
PMOS K_{eq}	0.79	0.59	0.6770	0.6770
PMOS K_{eqsw}	0.86	0.7	0.7694	0.7694

$$\sum C_{db(tpHL)} = 0.57(AD_n)(C_{jn}) + 0.61(PD_n)(C_{jswn}) + 0.79(AD_p)(C_{jp}) + 0.86(PD_p)(C_{jswp})$$
$$\sum C_{db(tpHL)} = 0.57(0.5)(2) + 0.61(2.05)(0.28) + 0.79(1)(1.9) + 0.86(2.85)(0.22)$$
$$\sum C_{db(tpHL)} = 2.96\ fF$$
$$\sum C_{db(tpLH)} = 0.79(AD_n)(C_{jn}) + 0.81(PD_n)(C_{jswn}) + 0.59(AD_p)(C_{jp}) + 0.7(PD_p)(C_{jswp})$$
$$\sum C_{db(tpLH)} = 0.79(0.5)(2) + 0.81(2.05)(0.28) + 0.59(1)(1.9) + 0.7(2.85)(0.22)$$
$$\sum C_{db(tpLH)} = 2.815\ fF$$
$$\sum C_{db(tfall)} = 0.67(AD_n)(C_{jn}) + 0.70(PD_n)(C_{jswn}) + 0.68(AD_p)(C_{jp}) + 0.77(PD_p)(C_{jswp})$$
$$\sum C_{db(tfall)} = 0.67(0.5)(2) + 0.70(2.05)(0.28) + 0.68(1)(1.9) + 0.77(2.85)(0.22)$$
$$\sum C_{db(tfall)} = 2.846\ fF = \sum C_{db(trise)}$$

Case 2
For case 2 we assume that $K_{eq}=K_{eqsw}=1$. This simplifies to only one C_{db} calculation.

$$\sum C_{db} = (AD_n)(C_{jn}) + (PD_n)(C_{jswn}) + (AD_p)(C_{jp}) + (PD_p)(C_{jswp})$$
$$\sum C_{db} = (0.5)(2) + (2.05)(0.28) + (1)(1.9) + (2.85)(0.22)$$
$$\sum C_{db} = 4.101 fF$$

Case 3
For case 3 we assume that $K_{eq}=K_{eqsw}=0.7$. This simplifies to only one C_{db} calculation.

$$\sum C_{db} = 0.7\left((AD_n)(C_{jn}) + (PD_n)(C_{jswn}) + (AD_p)(C_{jp}) + (PD_p)(C_{jswp})\right)$$
$$\sum C_{db} = 0.7\left((0.5)(2) + (2.05)(0.28) + (1)(1.9) + (2.85)(0.22)\right)$$
$$\sum C_{db} = 2.8707 fF$$

Now we can calculate the remaining capacitances that do not depend upon the transitions. For the driving inverter, we have to consider the miller effect on the overlap capacitances.

$$\sum C_{gd(driving)} = 2C_{gd0n}W_n + 2C_{gd0p}W_p$$
$$\sum C_{gd(driving)} = 2(0.31)(0.8) + 2(0.27)(1.6)$$
$$\sum C_{gd(driving)} = 1.36\ fF$$

The fanout capacitance includes gate-channel capacitance and overlap capacitances for each device in **each** fanout inverter (4X).

$$\sum C_{gn(fanout)} = W_n L_{eff} C_{ox} + W_n (C_{gs0n} + C_{gd0n})$$
$$\sum C_{gn(fanout)} = 0.8(0.2)(6) + 0.8(0.31 + 0.31)$$
$$\sum C_{gn(fanout)} = 1.456\ fF$$
$$\sum C_{gp(fanout)} = W_p L_{eff} C_{ox} + W_p (C_{gs0p} + C_{gd0p})$$
$$\sum C_{gp(fanout)} = 1.6(0.2)(6) + 1.6(0.27 + 0.27)$$
$$\sum C_{gp(fanout)} = 2.784\ fF$$
$$C_{fanout} = 4\left(C_{gp} + C_{gn}\right) = 16.96\ fF$$

b) Now we need to calculate the Resistances to be used in the Delay metric calculations.

$$R_{eqNMOS} = 0.8\frac{V_{DD}}{I_{Dsatn}} = 0.8\frac{2.5}{0.8(731E-6)} = 3419\Omega$$
$$R_{eqPMOS} = 0.8\frac{V_{DD}}{I_{Dsatp}} = 0.8\frac{2.5}{1.6(300E-6)} = 4166.7\Omega$$
$$R_{10-90NMOS} = 0.55\frac{V_{DD}}{I_{Dsatn}} = 0.55\frac{2.5}{0.8(731E-6)} = 2351.2\Omega$$
$$R_{10-90PMOS} = 0.55\frac{V_{DD}}{I_{Dsatp}} = 0.55\frac{2.5}{1.6(300E-6)} = 2864.6\Omega$$

$C_L(1, tphl) = C_{db} + C_{gd} + C_{fanout} = 21.28\ fF$

$C_L(1, tplh) = 21.135\ fF$

$C_L(1, trise) = 21.166\ fF$

$C_L(2) = 22.421\ fF$

$C_L(3) = 21.19\ fF$

Delay metric		Case (i)	Case (ii)	Case (iii)
t_{pLH}	Calculated value (ps)	61.00ps	64.74ps	61.19ps
	% error vs. case (i)	0	+6.1%	+0.3%
t_{pHL}	Calculated value (ps)	50.42ps	53.12ps	50.21ps
	% error vs. case (i)	0	+5.4%	-0.4%
t_{rise}	Calculated value (ps)	133.39ps	141.30ps	133.54ps
	% error vs. case (i)	0	+5.9%	+0.1%
t_{fall}	Calculated value (ps)	109.48ps	115.98ps	109.61ps
	% error vs. case (i)	0	+5.9%	+0.1%

c) Case 1 Advantage: Accurate
Case 1 Disadvantage: Complex and time consuming

Case 2 Advantage: Simple/Fast, provides upper bound (conservative)
Case 2 Disadvantage: Fairly inaccurate

Case 3 Advantage: Simple/Fast, provides good accuracy (normally)
Case 3 Disadvantage: May underestimate and give optimistic delay values

2. Transistor Sizing:

a) The capacitances for device M1 (C_{db} and C_{gd}) are fixed, since we know the size of M1, but we must solve for the capacitances in M2 as a function of unkown sizes W_n and W_p.

$$\sum C = (C_{db1} + C_{gd1}) + 3(C_{gc2} + C_{gd2} + C_{gs2})$$

$$C_{db1} = 0.7((1.2 * 0.625)(2) + (1.25 + 1.2)(0.28) + (2.4 * 0.625)(1.9) + (2.4 + 1.25)(0.22)) = 4.0873\ fF$$

$$C_{gd1} = 2(0.31)(1.2) + 2(0.27)(2.4) = 2.04\ fF$$

$$C_{gc2} = (C_{ox})(W_n)(L_{eff}) + (C_{ox})(W_p)(L_{eff}) = 1.2(W_n + W_p)$$

$$C_{gd2} = C_{gd0n}W_n + C_{gd0p}W_p = 0.31W_n + 0.27W_p$$

$$C_{gs2} = C_{gs0n}W_n + C_{gs0p}W_p = 0.31W_n + 0.27W_p$$

$$C_L = 6.13 + 3(1.82W_n + 1.74W_p) = 6.13 + 5.46W_n + 5.22W_p$$

b) Now we must derive a relationship between Wp and Wn in M2 that will enable us to reduce the equation in part A to a single variable. Symmetric transient behavior can be interpreted as equal rising and falling delay times.

$$t_{pHL} = t_{pLH}$$

$$0.8\frac{V_{DD}}{W_n I_{dsatn}} = 0.8\frac{V_{DD}}{W_p I_{dsatp}} \Rightarrow \frac{1}{W_n I_{dsatn}} = \frac{1}{W_p I_{dsatp}} \Rightarrow \frac{W_p}{W_n} = \frac{I_{dsatn}}{I_{dsatp}} = \frac{731E-6}{300E-6} = 2.43 = \beta$$

c) First we must use part A and part B to create a simple equation for the capacitance at node Vmid.

$$\begin{aligned} C_L &= 6.13 + 5.46W_n + 5.22W_p \\ &= 6.13 + 5.46W_n + 5.22(2.43W_n) \\ &= 6.13 + 18.15W_n \end{aligned}$$

Since we know that the beta ratio for balanced rising and falling delay metrics is 2.43 from part b, we know that the PMOS device in M1 will pull-up node Vmid slower than the NMOS device will pull-down. Then we must solve for the largest size of M2 with the rise and fall time under 100ps at node Vmid.

$$2.2R_{P(10-90)}C_L \le 100\,ps$$

$$2.2\left(0.55\frac{V_{DD}}{W_{p1}I_{dsatp}}\right)(6.13 + 18.15W_{n2}) \le 100\,ps$$

$$2.2\left(0.55\frac{2.5}{(2.4)(300E-6)}\right)(6.13 + 18.15W_{n2}) \le 100\,ps$$

$$(6.13 + 18.15W_{n2}) \le 23.8016\ fF$$

$$W_{n2} \le 0.9736\ um$$

$$W_{n2} = 0.9736\ um$$

$$W_{p2} = 2.3659\ um$$

d) With the sizes for the M2 Inverter, we must calculate the delay metrics for this structure. Since the sizing was determined for equal rising and falling delays, our R_{eq} and $R_{10\text{-}90}$ values should be equal for NMOS and PMOS devices. This will simplify the calculations to 2 calculations to find all four delay metrics.

$$\begin{aligned} C_L &= C_{M2} + C_{fanout} + C_{wire} \\ &= \left(0.7\left[(AD_n)(C_{jn}) + (PD_n)(C_{jswn}) + (AD_p)(C_{jp}) + (PD_p)(C_{jswp})\right] + 2(C_{gd0n}W_n) + 2(C_{gd0p}W_p)\right) + 30\ fF \\ &= 0.7\left[(0.609)(2) + (2.2236)(0.28) + (1.479)(1.9) + (3.6159)(0.22)\right] + 2(0.31)(0.9736) + 2(0.27)(2.3659) + 30 \\ &= 35.694\ fF \end{aligned}$$

$$R_{eqNMOS} = 0.8\frac{V_{DD}}{W_n I_{dsatn}} = 2810.17\Omega \approx R_{eqPMOS}$$

$$R_{(10-90)NMOS} = 0.55\frac{V_{DD}}{W_n I_{dsatn}} = 1931.99\Omega \approx R_{(10-90)PMOS}$$

$$t_{pHL} = t_{pLH} = 0.693R_{eqNMOS}C_L = 69.51\ ps$$

$$t_{rise} = t_{fall} = 2.2R_{(10-90)NMOS}C_L = 151.71\,ps$$

Reasonable rounding errors may be seen here.

3. Noise Margins

a) Calculate V_M using equations 5.3 and 5.4.

$$r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{(-30)(0.8)(-1)}{(115)(0.5)(0.63)} = 0.662526$$

$$(5.3)\ V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1+r}$$

$$= \frac{\left(0.43 + \frac{0.63}{2}\right) + 0.6625\left(2.5 + -0.4 + \frac{-1}{2}\right)}{1+0.6625}$$

$$= 1.0857\ V$$

$$(5.4)\ V_M \approx \frac{rV_{DD}}{1+r} = 0.9963\ V$$

The approximate is not that accurate for every situation.

b) Now we can use the linear extrapolation method for finding the noise margins of the gate.

$$I_D(V_M) = \frac{W_n}{L_{eff}}\left(k_n'\right)\left(V_{GT}V_{\min} - 0.5\left(V_{\min}^2\right)\right)(1+\lambda_n V_{DS})$$

$$= 2.5(115E-6)(0.63)(V_M - 0.4365 - 0.5(0.63))(1+0.06(V_M))$$

$$= 65.729\ uA$$

$$g = \frac{-1}{I_D(V_M)}\frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p}$$

$$= \frac{-1}{65.729uA}\frac{(2.5)(115)(0.63) + (4)(-30)(-1)}{0.16} = -28.633$$

$$NM_H = V_{DD} - \left(V_M - \frac{V_M}{g}\right)$$

$$= 2.5 - \left(1.0857 - \frac{1.0857}{-28.633}\right)$$

$$= 1.376\ V$$

$$NM_L = V_M + \frac{V_{DD} - V_M}{g}$$

$$= 1.0857 + \frac{1.4143}{-28.633}$$

$$= 1.0363\ V$$

c) The noise source can be converted into a voltage through the Q = CV relationship.
$Q = CV \Rightarrow 0.02pC = 19fF * V_{noise} \Rightarrow V_{noise} = 1.0526\ V$
The noise voltage exceeds the low noise margin (in the high gain region) yet it does not cross the switching threshold of 1.0857 V (V_M).

d) To solve for the resized W_p that would increase the NM_L such that the noise margin would not be violated by the noise event, an iterative technique is required. It is impractical to attempt to solve for a closed form equation that yields the optimal value of W_p. First one can solve for the required W_p through the V_M in the extrapolation method (assuming a constant gain). After a W_p is found, the gain equation can be updated with a new current and the W_p value can be refined again in the same manner. Excel and MATLAB are useful tools to automate this iterative process. Several iterations is sufficient to obtain an answer for the homework assignment.

Solve for the required V_M ignoring any change in gain (g).

$$V_{IL} = 1.0526 = V_M + \frac{V_{DD} - V_M}{g}$$

$$V_M \approx 1.10144\ V$$

Solve for the Width of the PMOS using the V_M equation (5.3)

$$r = \frac{V_M - \left(V_{Tn} + \frac{V_{DSATn}}{2}\right)}{\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right) - V_M}$$

$$W_p = \frac{k_n V_{DSATn} L_{eff}}{k_p' V_{DSATp}} \left(\frac{V_M - \left(V_{Tn} + \frac{V_{DSATn}}{2}\right)}{\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right) - V_M} \right)$$

$$W_p \approx 1.2075E-6 \left(\frac{1.101 - (0.43 + 0.315)}{(2.5 - 0.4 - 0.5) - 1.101} \right)$$

$$W_p \approx 0.8615\ um$$

Use the new size to recalculate gain and iterate in this loop again.

Wp = 0.866339 um after several iterations.

e) Since we did not consider the effect of the size increase on the input capacitance value of 19fF the above calculation is an estimate. As we increased the size of the PMOS device, the actual input capacitance would increase. Since the noise event was of fixed charge, an increase in capacitance would therefore lower the noise voltage. A lower noise voltage than calculated indicates that our resizing of the PMOS device overcompensated for or overestimated the noise source in the problem. A smaller increase in the size of the PMOS would be sufficient.

4. VTC Curves

a) See attached plot.

b) See attached plot.

c) In a static CMOS inverter, the inverter is normally in a state with V_{in} = 0 or V_{dd} unless the gate is transitioning. If we look at the edges of the VTC/Current plot from a and b, we notice that there is no current conducting in these regions of the plot. Therefore, under static, non-transient conditions, CMOS has no power consumption.

EECS 312: HW2 VTC Curve