EECS 312: Digital Integrated Circuits
Homework #3

Reading: 5.5

1. **Energy and Power Consumption**: Consider an IC designed for portable applications such as a laptop computer. The system is designed with a 39 Watt-hour battery and you may assume that the IC is the only device consuming any power from the battery (all peripherals have zero power consumption – idealistic!). The IC contains a clocked network with 10,000 nodes (assume all inverters) with an average capacitive load (C_L) of 40fF, and another 5×10^6 un-clocked nodes (assume all inverters) with capacitive loads (C_L) of 6fF and a switching activity $\alpha_{sw} = 0.10$. The IC runs at a nominal frequency of 1GHz. Assume that the average device width is 4um. Use $V_{th}=0.25V$ and subthreshold swing, $S_S = 90$ mV/decade for the subthreshold calculations. Use the default technology for any additional parameters needed.

   a) Considering only dynamic power consumption, calculate the power consumption of the IC and the amount of time before a fully charged battery is discharged.
   b) To obtain a more accurate estimate of battery time, now consider the added impact of subthreshold current on the battery life. Calculate the static power consumption of the IC, assuming all nodes are driven by inverters. Recalculate the amount of time required to discharge a fully charged battery. What percentage reduction in battery life is seen (compared to part A)?
   c) One technique used in portable applications to reduce power consumption, is lowering the supply voltage (i.e. when the laptop is unplugged). Calculate the power consumption (static and dynamic) when the supply voltage is reduced to 1.8V. How long does a battery charge last with reduced V_{DD}?
   d) Another technique used to reduce power consumption is to reduce the switching frequency of the device. Calculate the power consumption (static and dynamic) when the frequency of the IC is reduced to 600MHz. How long does the battery charge last with reduced frequency?

2. **Self Loading Effect:** A CMOS inverter with $W_p=2W_n$ drives a fixed fan-out capacitance of C_{FAN}. You are given a simple relationship for total load capacitance at the output of the inverter,

$$C_L=[(C_{FAN} + 0.4375) + (4.7415\ W_n)]\ fF$$

   a) Plot the derivative of t_{pHL} with respect to W_n over the range 0.25um < W_n < 4um for $C_{FAN} = 5$, 10 and 15 fF (on the same plot). Use the given capacitance equation.
   b) Using the plots from part A, what do you think is a good size for this driver (for each C_{FAN}) considering the general power/area/delay tradeoff (for each C_{FAN})? Give support for your answer.
   c) Now consider the impact of sizing on energy usage. Plot the Energy-Delay Product (Energy per cycle * Delay(t_{pHL})) of this inverter vs. W_n over the range 0.25um < W_n < 10um for $C_{FAN} = 5$, 10 and 15 fF (on the same plot). See Equation 5.56 from Rabaey, except we will use only the t_{pHL} instead of t_p. Use the given capacitance equation.
   d) What are good sizes when considering EDP? Give support for your answer. How do these sizes compare to your answer from part B?

3. Complex Logic Gates:
a) Using the circuit diagram below, determine the function at node OUT in terms of A,B,C,D,E,F, and G.
b) Determine the "dual" to part A using Demorgan's Law.
c) Draw a complex gate that implements the following function:

$$OUT = \overline{(A+B)\cdot(F+CDE)}$$