EECS 312: Digital Integrated Circuits
Homework #2

Reading: 5.3, 5.4

1. **K_{eq} Approximation and FO4 Delay**: Consider a CMOS inverter with fan-out of 4 identical inverters. Both the driving inverter and the fan-out gates have W_n=0.8um, W_p=1.6um, L_{drawn}=0.25um, and L_{eff}=0.2um. This problem uses our default 0.25um CMOS technology including the below capacitance parameters (on the top of the next page). We will neglect any wiring parasitics (resistance and capacitance) in this problem.

   a) We want to calculate the delay of this inverter. As such, we need to lump all the relevant capacitances into a single C_L at the output node. Along the lines of Example 5.4 of the text, compute the total capacitance C_L using the following approximations for junction capacitance:
   i) Use the K_{eq} parameters from example 5.3 on page 196 to find C_{db} for the PMOS and NMOS devices. You will also need to calculate K_{eq} for rise-time and fall-time calculations for both NMOS and PMOS devices. (4 C_{db} for NMOS and 4 C_{db} for PMOS).
   ii) Use K_{eq} = 1 for all components of C_{db}
   iii) Use K_{eq} = 0.7 for all components of C_{db}. This approximation is based on the fact that K_{eq} is *typically* in the range of 0.5-0.9.

   For cases (ii) and (iii) there will be no difference between C_{db} values for high→low and low→high transitions. In case (i), there will be different C_{db} values for each transition. Among cases (i), (ii), and (iii), there will be no difference in capacitances other than C_{db}.

   b) Calculate t_{plh}, t_{phl}, t_{rise}, and t_{fall} for all three cases above (i, ii, iii). Using case (i) as the reference, find the % error obtained when using the approximations of cases (ii) and (iii). Note the sign of the error (e.g. +5% error, -8% error, etc.). Use the simple RC model presented in class to find delays. You can use a table similar to the one below to record your answers. The delays calculated in this equation are "fan-out of 4" delays, meaning that they are a measure of the delay of a gate in this technology with a fan-out of 4 identical gates (often referred to as FO4 delay). This is often used as a benchmark of a given process technology (similar to ring oscillator delay).

Delay metric		Case (i)	Case (ii)	Case (iii)
t_{pLH}	Calculated value (ps)			
	% error vs. case (i)	0		
t_{pHL}	Calculated value (ps)			
	% error vs. case (i)	0		
t_{rise}	Calculated value (ps)			
	% error vs. case (i)	0		
t_{fall}	Calculated value (ps)			
	% error vs. case (i)	0		

   c) List one brief advantage and disadvantage of each of the three methods of calculating C_{db} listed above (cases i, ii, and iii)?

Capacitance parameters for default technology:

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NMOS
+ CGDO = 3.1E-10   CGSO = 3.1E-10   CJ = 2.0E-3   CJSW = 2.8E-10
PMOS
+ CGDO = 2.7E-10   CGSO = 2.7E-10   CJ = 1.9E-3   CJSW = 2.2E-10
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2. **Transistor Sizing**: We want to determine the transistor sizes (widths) of the devices in the inverters labeled M2 in Figure 1. M1 and M2 denote particular size combinations of NMOS and PMOS devices in inverters. Inverter M1 has a PMOS device with W_p=2.4um and an NMOS device with W_n=1.2um. Use the K_{eq} = 0.7 approximation and standard capacitance parameters above to develop a capacitance C_L equation for V_{mid} in terms of the W_p and W_n of each device in M2. Assume the standard 0.25um process technology parameters. Remember to consider the Miller effect when calculating capacitances for this problem. All devices will use minimum channel length.
   - **a)** Develop an equation for the capacitance at node V_{mid} as a function of W_n and W_p of M2.
   - **b)** The NMOS and PMOS devices *(in M2)* must be sized using a ratio (W_p/W_n) that yields symmetric transient behavior. Derive an expression for a ratio, β, for which transient behavior *from V_{mid} to V_{out}* is symmetric. Calculate β.
   - **c)** Using the results from part A and B, calculate the maximum width of the NMOS and PMOS device in each M2 inverter, such that the t_{rise} and t_{fall} of node V_{mid} are *at or below 100ps* and the transient behavior *from V_{mid} to V_{out}* is symmetric. *First identify the slower transition (t_{rise} or t_{fall}), and then solve for the size that results in a 100ps transition for the slower transition.*
   - **d)** Using the sizes obtained in *part C*, calculate the t_{plh}, t_{phl}, t_{rise}, and t_{fall} of the shaded M2 inverter considering a lumped fan-out and interconnect cap of 30 fF + any intrinsic device capacitances (again re-use any relevant capacitance figures from problem 1).

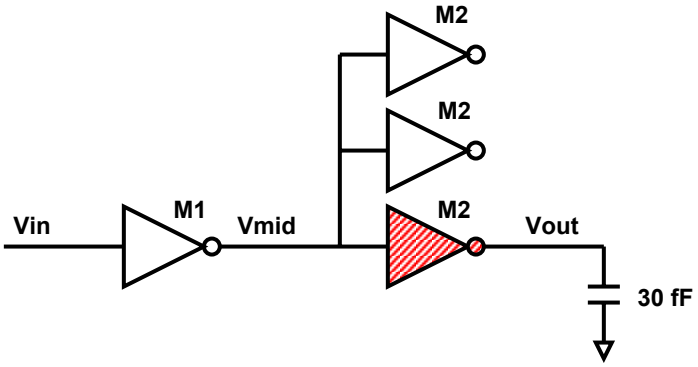

Figure 1: Inverter Circuit

3. **Noise Margin**: A CMOS inverter is designed with W_n=0.5um and W_p=0.8um. The total input capacitance on the input node of this gate is 19 fF. Assume all additional device parameters match the default 0.25um technology.

   - **a)** Calculate the V_M for this gate using both Eq. 5.3 and 5.4 from the text. How close is the approximation in Eq. 5.4 to the result from Eq. 5.3?
   - **b)** Find NM_H and NM_L for the gate. Solve for the gain using *5.10a* and use the linear extrapolation method from lecture to estimate V_{IH} and V_{IL}. *Use the V_M from Eq. 5.3 in the rest of the problem.*
   - **c)** A noise source injects 0.02pC of charge onto the input node of the gate which was formerly at 0V. Does the noise source cause the inverter to enter a region of high gain (Noise Margin Violation)? Does the noise source cause the device to reach the *switching threshold*?

d) Holding the value of W_n constant, resize the PMOS width, W_p, such that the noise source in part C would not violate the noise margin of the inverter. Use the linear extrapolation method for calculating noise margins. **Simplifying Assumption**: *Assume that the input capacitance of 19 fF does not vary with the transistor sizing (fixed value).*

e) Consider the effect of resizing the PMOS device on the input capacitance (originally 19 fF). Does our simplifying assumption in part D lead to an overestimation or underestimation of the required width? Why?

4. VTC Calculations: A CMOS inverter is designed with W_n=1.4um and W_p=3um. Assume all additional device parameters match the default 0.25um technology.

a) Using Excel or Matlab (or another suitable software tool), plot the VTC for this inverter.

b) On the same plot, graph the current between V_{DD} and Ground as a function of V_{in}.

c) Using the plot as support, justify the statement "CMOS has no static power consumption."