Lab 3

Objective
- Analysis of power/energy characteristic of a CMOS inverter
- Analysis of Pseudo NMOS and Pass transistor logic characteristic

Part 1 : Dynamic and Short Circuit Energy Dissipation

For this part of the lab you can use the circuit from Lab2, figure 3. For simulation of power/energy in CMOS, run a *Transient* simulation. The *time step* and *Stop Time* are set at 1P and 2N respectively. Define the input signal as follows:

Initial Value: 2.5V Pulsed Value: 0V
Delay Time: 0.5N Rise Time: 0.3N Fall Time: 0.3N
Pulse Width: 2N Period: 3N

Run the simulation. To view the current at a particular node, you need to click at the node. A + sign appears at the node indicating that it has been selected. Now click on the button 'Chart' of the right menu window associated with RESULT. The curve window will automatically pop up.

Calculation of charge and energy from current vs. time plot
In order to calculate the energy, we should first integrate the current vs. time curves to obtain the charge transferred. This can be done as follows:
(1) Make sure the appropriate current node is selected
(2) In the right **RESULT** window, click **WF Measure**. A window pops out.
(3) Select **Run Data** and **A**.
(4) In the *Signal Type* field, select **Current**.
(5) **/I$XXX/D** should appear in the field of *Signal A*. XXX is an integer corresponding the node selected.
(6) Select **Integral at TIME** for *Measurement Function.*

Exercise 1:
(1) **Output two current vs. time plots and label them as figure 3-1 and 3-2. These currents correspond to the total dynamic power and short circuit power respectively (you have to select the appropriate nodes from the circuit to determine these currents).**
(2) **Integrate Figures 3-1 and 3-2 as described above and answer the following questions.**
(3) **Give the total energy drawn from the power supply and the energy associated with short-circuit current.**
(4) **What is the ratio of short circuit energy and total dynamic energy? Is it close to the rule of thumb mentioned in class?**
(5) **What is the theoretical prediction for energy drawn from the power supply considering the load capacitance? Is the simulation result close to this prediction? If not, give two reasons for the discrepancy.**

Part 2 : Static Power Dissipation

To obtain the static power of a CMOS inverter a **DCOP** analysis is used. Run the simulation with the input voltage fixed at 2.5V. Select both the PMOS and the NMOS, and click **DC Power** in the result window. A window with power data will pop up. In the same manner, find the static power when the input is equal to 0V.

Exercise 2:
1) **Determine the static power for both the NMOS and PMOS with Vin = 2.5V and Vin = 0V.**
2) **When V_{in} = 0V, is the power consumed by the PMOS and the NMOS equal? If not, why?**
3) **Using the dynamic energy drawn from the power supply calculated in Exercise 1, calculate the switching frequency (fsw) that would yield equal amounts of dynamic and static power consumption for this circuit. Assume the likelihood of low and high inputs are equal.**
4) **Calculate the subthreshold swing (S_S) for the NMOS device. Submit the relevant graph labeled as figure 3-3. (You can change the axis of a plot to log scale or change its resolution by selecting the desired axis and pressing RMB and choosing edit > change).**
5) **Using the I_{off} expression from class and the subthreshold swing (S_S) found above, calculate the V_{th} for the NMOS device.**

Part 3 : Ratioed design and delay times for Pseudo-NMOS NAND gate

Create a schematic of a 2-input NAND pseudo-NMOS gate with a CMOS inverter as its only load. Place a 100fF capacitance at the output of the CMOS inverter. Let all the NMOS transistors in this schematic along with the PMOS of the inverter have the following parameters W=0.5U L=0.25U AS=0.3125P AD=0.3125P PS=1.75U PD=1.75U. Then set W=0.5U L=0.25U for the PMOS load of the NAND gate, the area and perimeter of source and drain are ignored in order to simply the process of searching out the right width for this PMOS load.

As discussed in the lecture, the swing of pseudo-NMOS is not rail-to-rail; therefore, V_{OL} is not equal to down 0V. This leads to the leakage current and power dissipation in NMOS of the inverter. In our case, the maximum allowable static power dissipated by the inverter is **0.2μW**. Your goal is to find the right size of PMOS load of NAND gate to meet this requirement. The width of PMOS can be changed by clicking the button *Design Change* in the right window. Make sure the PMOS is highlighted. Then click on Change Property. Change the width of PMOS by correcting the *INSTPAR* properties listed in the pop-up window. If you want to use preliminary hand calculations to start your search, please provide that with your submission.

Exercise 3:

1. **Hand in the necessary calculations and the methodology for finding the final device width for achieving a static power dissipation of 0.2µW for the CMOS inverter. You need to show the static power dissipation by plotting the product of the voltage and the dominant current contributing to static power dissipation (figure 3-4). (You will find WF Function option in the results menu useful for plotting the product of two signals).**
2. **Using the PMOS sizing from above, plot the pull-up (A: 1 → 0, B: 1 → 0) and pull-down delays (A: 0 → 1, B: 0 → 1) for this pseudo-NMOS NAND gate (Figure 3-5) ? Is the ratio of these two delays reasonable? Explain.**

Part 4 : V_{th} drop of NMOS Pass Transistor

In Figure 1-1, the output of the first NMOS is connected to the gate of the second NMOS. Set *B* and *C* inputs as 2.5V, conduct DC sweep of input A from 0V to 2.5V to observe the output Y. For Figure 1-2, the output of the first NMOS is connected to the s/d of the second NMOS. Set *B* and *C* inputs as 2.5V, conduct DC sweep of input A from 0V to 2.5V to observe the output Y. All the NMOS have W=0.5U L=0.25U AS=0.3125P AD=0.3125P PS=1.75U PD=1.75U.
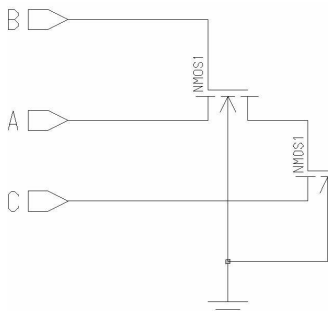

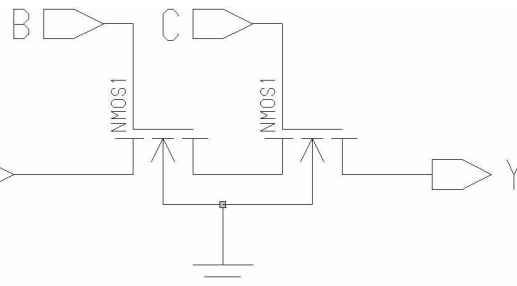**Figure 1-1 Configuration 1**   **Figure 1-2 Configuration 2**

Exercise 4:

1. **What are the simulated output high voltages at node Y for these 2 cases? Are they the same? Why or why not?**
2. **Hand calculate the expected output high voltage at node Y for each case based on our default technology from lecture. Are these values close to the simulated results?**
3. **You need to submit two plots resulting from the DC sweeps together with your answers to this exercise. Label them as figure 3-6 and 3-7.**

Part 5 : Equivalent Resistance of CMOS Transmission Gates

In order to avoid the problem of V_{th} loss of single NMOS pass transistor, one NMOS and one PMOS are combined together as a pass logic. For our simulation, the schematic is shown as Figure 2. Both the PMOS and NMOS have W=0.5U L=0.25U AS=0.3125P AD=0.3125P PS=1.75U PD=1.75U.
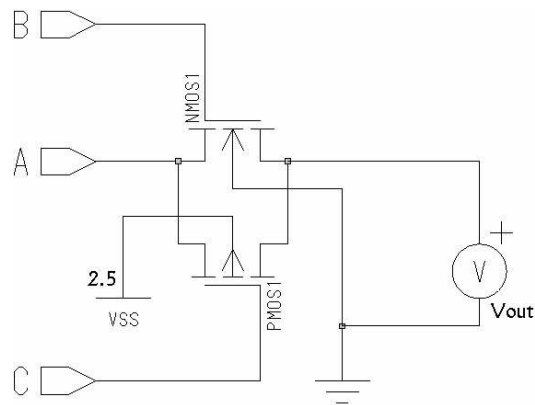
Figure 2. Pass Transistor

Set input B and A at 2.5V, input C at 0V, then conduct DCOP analysis of V_{out} to obtain the current characteristics.

Exercise 5:

1. **Submit the Id vs. Vout plot (figure 3-8).**
2. **Plot the equivalent resistance (large-signal) as a function of output voltage (figure 3-9). (You might find the WF Function useful for this purpose). Note that the voltage drop across the pass transistor is not equal to V_{out} (You might find it useful to refer to figure 6-48 from the text book).**