EECS 312: Digital Integrated Circuits
Homework #5

Reading: 7.1-7.3

1. **V_{DD}/V_{th} Scaling**: Consider a single stage of a ring oscillator in our default technology with Wp=Wn=0.5μm, fan-out is 1, and no interconnect loading. Assume the total capacitive load presented to each stage of the ring oscillator is 3fF. Assume that S_S is 90 mV/decade. Ignore short-circuit power in this problem.

   a. For a single stage plot energy, delay, energy*delay, and energy*delay^2 vs. Vdd for a range from 0.6V to 3.5V. Normalize each quantity with respect to its value at Vdd=2.5V. For delay, use $t_p = (t_{pHL} + t_{pLH})/2$. Let the ratio of V_{dsat}/V_{DD} remain constant.
   b. Now let the ratio V_{th}/V_{DD} remain constant as V_{DD} is reduced and repeat part (a). Note that this analysis does not consider the impact of static power so it is overly optimistic.
   c. If we can tolerate a speed penalty of 30% relative to the nominal gate delay at V_{DD}=2.5V, how much lower dynamic power consumption will the scaling strategy of part (b) yield compared to that of part (a)? *Use the graphs from (a) and (b).*
   d. Plot P_{static}, P_{dyn} and the sum of P_{static} and P_{dyn} for a single stage over the voltage range from (a) using the V_{th} scaling approach from (b). Assume a clock frequency of 1GHz and a switching activity of 0.12. Consider the input states (high and low) to be equally likely.
   e. Now consider the impact of V_{th} reduction on static power for a single stage. At the V_{DD} and V_{th} design point used in (c) (for the approach from (b)), calculate the percentage increase in static power consumption compared to the default values of V_{DD} and V_{th} for out technology.
   f. Assuming a clock frequency of 1GHz governing the inputs to the circuit, calculate the limit on the activity factor α_{sw} of the circuit such that the V_{DD}/V_{th} scaling is effective in reducing overall power consumption. *Use the V_{DD}/V_{th} point from the 30% penalty calculated in (c) (for V_{DD}/V_{th} reduction).* You may assume that leakage power occurs whether the circuit is switching or not.

2. **Combinational Logic in Sequential Systems:** Consider the circuit in Figure 2.1. The design requirement for this sequential system is a 2 GHz clock frequency. The D Latches used in the sequential circuit have the following performance characteristics: t_{CLK-Q} = 45ps, t_{D-Q} = 35ps, t_{setup} = 25ps, t_{hold} = 85ps. Use the sizes given in the chart below for this problem. Consider the input capacitance of each D-Latch as 8 fF and the output risetime/falltime of each D Latch is 60ps. The clock rise/fall time is 90ps. Consider the input slope dependence on *delay* using our linear model with K=0.15 (for the latest arriving signal at each gate). Consider both out1 and out2 for all delay and timing calculations in this problem. For worst-case calculations, all inputs not explicitly connected to a latch may be assumed to be connected to the output of a latch where the data is available at the latest time (that ensures proper functionality) before the edge of the clock that will close the latch (make it non-transparent). Use the 0.6 fF/um approximation for junction capacitances and calculate C_{gc} only for gate capacitances in this problem, also add 4 fF of wiring capacitance at each gate output node (6 gates total in this problem).

   a. Are there limitations on the size of the pre-charge devices X1 and Z1? Explain. Find applicable upper and lower limits on pre-charge device Z1 (quantitative).
   b. Find the *maximum* delay through the circuit from inputs (in1,in2) to outputs (out1,out2).
   c. Find the *minimum* delay through the circuit from inputs to outputs.
   d. Does this circuit operate properly in a 2 GHz system? If not, identify the setup and/or hold time violations and propose a sizing change to a single transistor that will correct any issues.

e. If the *hold time* is violated and transistor sizes are fixed to the sizes in the table below, what is an alternative solution that can be implemented *easily* without altering the core logic function?
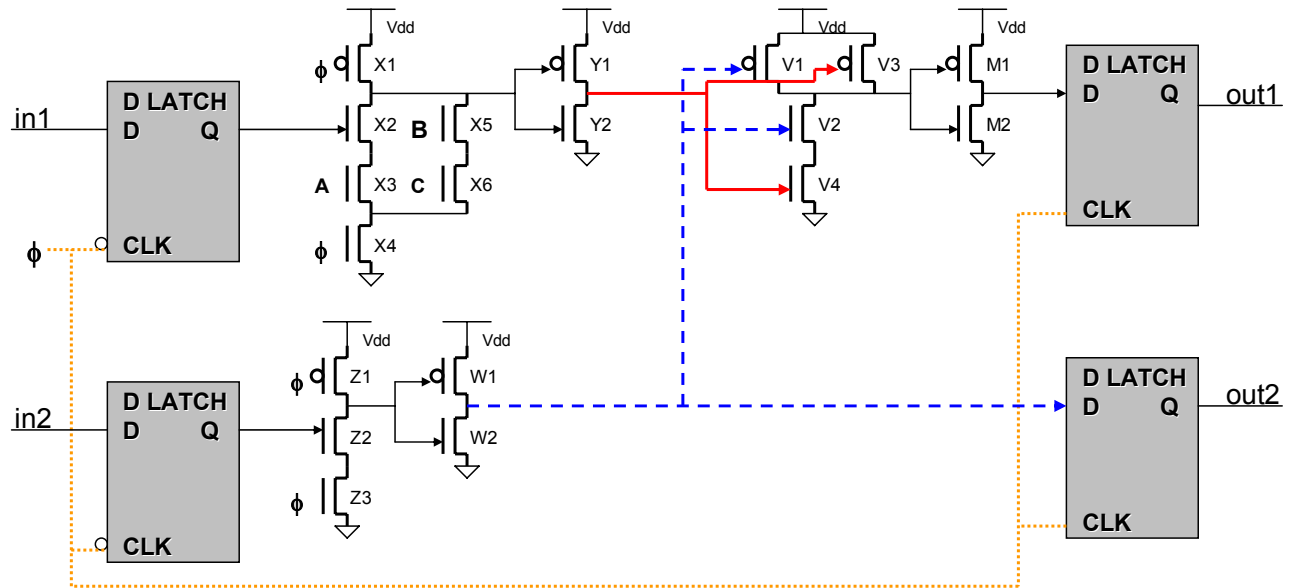

Figure 2.1 Sequential System

Note: The latches for the inputs are transparent when the clock is low (negative latches) and the latches at the outputs are transparent when the clock is high (positive latches). There is an error in the lecture slides on this topic (concerning the input bubble on the clock connection).

EECS 312 HW5 P2 Transistor Size Table					
X1	1.0 um	V1	0.8 um	W1	3.0 um
X2	1.0 um	V2	1.0 um	W2	1.0 um
X3	1.0 um	V3	0.8 um	M1	2.0 um
X4	2.0 um	V4	1.0 um	M2	1.0 um
X5	1.5 um	Z1	1.0 um		
X6	1.5 um	Z2	2.0 um		
Y1	1.5 um	Z3	2.0 um		
Y2	0.5 um				

3. **Design Problem:** This problem is intended to familiarize you with the strategies and techniques that will be useful for your final design project for this class. The goal of the design problem is to implement the function detailed below (Figure 3.1), minimizing total transistor width and worst-case delay. You may use any combination of logic styles and sizing techniques that we have covered in class, or that you are ambitious enough to explore. The design must run at 2.5V V_{DD} and the default threshold voltages. For your simulations, assume all inputs are driven by static CMOS inverters with W_p=1um and W_n=0.5um (you should measure delay from the input of these

inverters) and inputs to these inverters have a risetime and falltime of 75ps. The final output load should be 50fF. Static power consumption beyond leakage is unacceptable in this design.

$$X = ABC + B\overline{C}D + \overline{B}CE \qquad (3.1)$$

a. Minimize A * t_p^2 where A is the sum of total transistor area (W*L_{drawn}) and t_p is the worst-case delay. If a clock is used in your solution, penalize A by a factor of 1.5 to account for clock routing and buffering area.
b. Justify your initial topology and performance figures with hand calculations.
c. Verify hand calculations with SPICE simulation using the techniques learned in the lab assignments. Submit plots of your circuit topology with the worst-case path highlighted and simulation waveforms verifying functionality and worst-case delay.

Top student solutions will be presented in the homework solutions after the assignment is graded.