EECS 312: Digital Integrated Circuits
Homework #4 Solutions

1. Pseudo-NMOS Gates:

a) The worst-case low output voltage condition will occur when only one pull-down transistor is active. One transistor will provide the lowest current resisting the pull-up current provided by the weak PMOS transistor. Begin, by setting the currents through the NMOS and PMOS devices equal. Since V_{OL} should be fairly low (less than V_{th}) we can assume that NMOS will be in the linear region and the PMOS device will be saturated. To minimize the rising delay, we should minimize the size of the NMOS devices (which minimizes the capacitive loading of the output node). However, we must ensure that the worst-case V_{OL} is less than the switching threshold of a dynamic gate (V_{th}).

Considering CLM:

$$k_n'\left(\frac{W_n}{L_{eff}}\right)\left((V_{DD}-V_{th})(V_{OL})-\frac{V_{OL}^2}{2}\right)=k_p'\left(\frac{W_p}{L_{eff}}\right)\left((V_{DD}-V_{th})V_{dsat}-\frac{V_{dsat}^2}{2}\right)(1+\lambda(V_{DD}-V_{OL}))$$

$$(115E-6)\left(\frac{W_n}{0.2}\right)\left((2.5-0.43)(0.43)-\frac{0.43^2}{2}\right)=(30E-6)(5.25)\left((2.5-0.4)1-\frac{1}{2}\right)(1+0.1(2.5-0.43))$$

$$W_n=0.663um$$

Without CLM:

$$k_n'\left(\frac{W_n}{L_{eff}}\right)\left((V_{DD}-V_{th})(V_{OL})-\frac{V_{OL}^2}{2}\right)=k_p'\left(\frac{W_p}{L_{eff}}\right)\left((V_{DD}-V_{th})V_{dsat}-\frac{V_{dsat}^2}{2}\right)$$

$$(115E-6)\left(\frac{W_n}{0.2}\right)\left((2.5-0.43)(0.43)-\frac{0.43^2}{2}\right)=(30E-6)(5.25)\left((2.5-0.4)1-\frac{1}{2}\right)$$

$$W_n=0.549um$$

b) Now we repeat the method from (a) and solve for V_{OL} considering the NMOS device sizes of 0.663 um. There are two roots from each equation; the value near V_{th} (but less than V_{th}) is the root to use.

Considering CLM:
V_{OL}(2 inputs on) = 0.2065 V
V_{OL}(3 inputs on) = 0.1360 V

Without CLM:
V_{OL}(2 inputs on) = 0.2026 V
V_{OL}(3 inputs on) = 0.1327 V

c) Now to calculate the average static power consumption, we can use the VOL values calculated in the previous parts of the problem with the unified current model.

Considering CLM:

$$I_{Dn}(1) = (3.315)(115E-6)\left((2.5-0.43)(0.43) - \frac{0.43^2}{2}\right) = 304.2uA$$

$$I_{Dn}(2) = (6.63)(115E-6)\left((2.5-0.43)(0.2065) - \frac{0.2065^2}{2}\right) = 309.8uA$$

$$I_{Dn}(3) = (9.945)(115E-6)\left((2.5-0.43)(0.1360) - \frac{0.1360^2}{2}\right) = 311.6uA$$

$$P_{AVG} = (1/8)(2.5)(0) + (1/8)(2.5)(311.6uA) + (3/8)(2.5)(309.8uA) + (3/8)(2.5)(304.2uA)$$

$$P_{AVG} = 672.9uW$$

Without CLM:

$$I_{Dn}(1) = I_{Dn}(2) = I_{Dn}(3) = (2.745)(115E-6)\left((2.5-0.43)(0.43) - \frac{0.43^2}{2}\right) = 252.0uA$$

$$P_{AVG} = (1/8)(2.5)(0) + (7/8)(2.5)(252.0uA)$$

$$P_{AVG} = 551.2\ uW$$

Power is a greater concern than the noise in this case. This static power consumption becomes prohibitively high long before the design is in risk of crossing the switching threshold of the next gate. As you can see, CLM makes a large difference in this type of problem. The CLM solution above isn't even completely accurate, since it isn't considered for the NMOS transistors in the calculation of V_{OL}.

2. Pass Transistor Logic:

a) The circuit is a NAND gate.

b) When A=B= VDD, the voltage at node x is $V_X=V_{DD}-V_{tN}$. This causes static power dissipation at the inverter the pass transistor network is driving.

c) See the figure below. To minimize static power consumption, device Mr is added (as a level restorer). The size of M_r should be chosen so that when one of the inputs A or B equals 0, either M_{n1} or M_{n2}, would be able to pull node X to $V_{DD}/2$ or less.

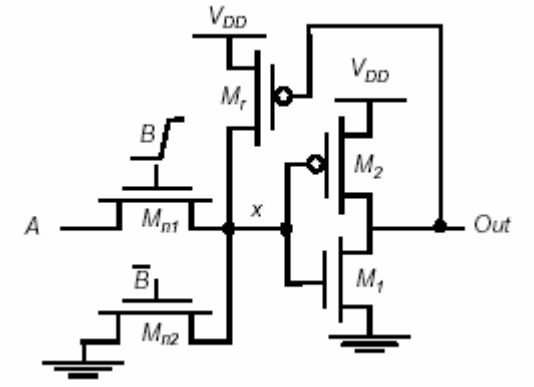

Figure 2.1

d) See the figure below for one possible NAND gate implementation using transmission gates.

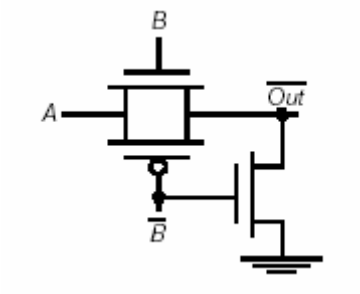

Figure 2.2

e) One possible *pass transistor* implementation of the function ABC.

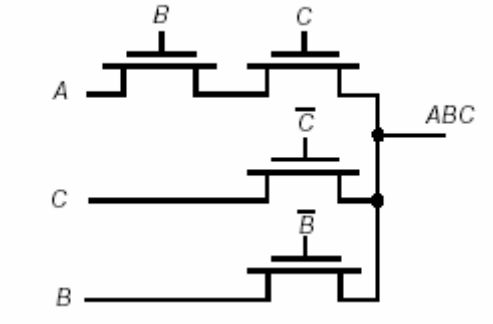

Figure 2.3

3. Dynamic Logic:

a) $OUT = AB(C + D)$ when the clock signal is high (the evaluation period of the gate).

b) Charge-sharing occurs during the evaluate phase of a dynamic gate (when the clock is high). For our particular circuit, when inputs A and B are high and C and D are low, two large internal capacitances are connected to the dynamic output node. To calculate the charge-sharing, we need to compare the capacitances of the internal nodes to the capacitance of the output node.

$$C_{out} = (2+3)(0.6) + (6(0.2))(4+2)\ fF = 10.2\ fF$$
$$C_{\text{int}} = ((3+3) + (3+3+3))(0.6) = 9\ fF$$
$$\Delta V_{out} = \frac{C_{\text{int}}}{C_{out} + C_{\text{int}}} V_{DD} = 1.17\ V$$

c) Besides charge-sharing leading to a potential glitch in the output signal which can easily cause timing or functionality failures (reliability) in circuits, the more common side-affect is increased static power dissipation in the static gate following a dynamic output node.

d) See attached plot.

e) Based upon the results from D, it is clear that we would like a high b ratio. However, we cannot violate the noise margin with the charge sharing values from (b). The C_{wire} capacitance was originally intended to be included in (b), but was mistakenly left out. With less concern over noise margin, a decent range for β is nearer to the 3-5 range for this type of gate. Based upon the actual constraints, our **β should be near 1.5-1.6**. With the consideration of C_{wire}, the change in Vout is 0.827 V. This would be closer to the 4-5 range for β.

4. Dynamic Logic:

a) The timing diagram is shown below for the dynamic circuit.

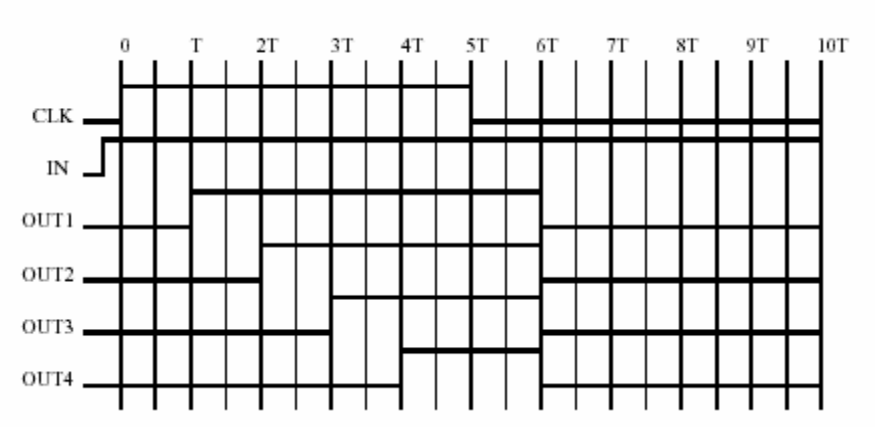

Figure 4.1

b) There is no problem during the evaluate stage. The pre-charged nodes remain charged until a signal propagates through the logic, activating the pull-down network and discharging the node. In fact, this topology improves the circuit's robustness in terms of charge sharing affecting the output for any generic pull-down network, and reduces the body effect in the pull-down network.

c) There is a problem during the pre-charge stage. If all pre-charged nodes are discharged during the evaluate stage, when the pre-charge FETs simultaneously turn on, the pull-down networks will initially remain on, creating a short circuit. This continues in each gate until the previous gate charges, disabling its pull-down network.

5. Combinational Gates:

a) Worst-case initial states are not unique and there are several equally acceptable answers. The final states for both transitions are unique.

Worst Case t_{pLH}: Initial 1101100, **1110100**, 1100101 Final **1101000**

Worst Case tpHL: Initial 1110000, **1101000**, 0111000, 1011000 Final **1110100**

Note: Many static CMOS combinational gates have the property highlighted above in red. The worst-case final state of one transition is the worst-case initial state for the opposite transition. This is not always true, but can be useful when first analyzing a combinational gate.

b) $OUT = \overline{AB(E+F+DG)+C(G+D(E+F))}$

c) To calculate the pull-down delay of each transistor stack, we will use the Elmore delay equations.

Conventional

$$R_{eq} = 0.8\left(\frac{V_{DD}}{I_{Dsat}}\right) = 0.8\left(\frac{2.5}{(4um)731E-6}\right) = 684\,\Omega$$

$$C_{out} = 20\,fF$$

$$C_{in1} = 0.6\,fF(4+4) = 4.8\,fF$$

$$C_{in2} = 0.6\,fF(4+4) = 4.8\,fF$$

$$t_{pHL} = 0.693\left(R_{eq}(C_{out}+C_{in1}+C_{in2})+R_{eq}(C_{in1}+C_{out})+R_{eq}(C_{out})\right)$$

$$t_{pHL} = 35.3\,ps$$

Stack Tapering

$$R_{3.5} = 0.8\left(\frac{2.5}{(3.5um)731E-6}\right) = 782\Omega$$

$$R_{4.0} = 0.8\left(\frac{2.5}{(4um)731E-6}\right) = 684\Omega$$

$$R_{4.5} = 0.8\left(\frac{2.5}{(4.5um)731E-6}\right) = 608\Omega$$

$$C_{out} = 20\ fF$$

$$C_{in1} = 0.6\,fF(3.5+4) = 4.5\ fF$$

$$C_{in2} = 0.6\ fF(4+4.5) = 5.1\,fF$$

$$t_{pHL} = 0.693\left(R_{4.5}\left(C_{out}+C_{in1}+C_{in2}\right)+R_{4.0}\left(C_{in1}+C_{out}\right)+R_{3.5}\left(C_{out}\right)\right)$$

$$t_{pHL} = 34.9\ ps$$

$$Percent\ Change = \frac{34.9-35.3}{35.3} = 0.0098$$

Stack Tapering delivers a minimal improvement (~1%) in delay with an output capacitance of 20 fF. This result is slightly misleading, since the stack tapering actually reduces the capacitance at the output node under normal circumstances since the transistor has a smaller C_{db}. If this is considered, the tapering achieves ~2% performance advantage.

d) When the output capacitance is increased 10X to 200fF the performance of stack tapering is reduced, since the internal capacitances, which stack tapering aims to discharge more rapidly, are negligible when compared to the output capacitance. Specifically in this example, the performance is actually worse, since the series resistance of 3.5,4,4.5 is slightly higher than the 4,4,4 design. Be careful when using these "optimizations", they do not always guarantee results.

6. Transmission Gates:

Before solving any portion of this problem, several useful values need to be calculated. The t_{pBUF} of an inverter, the resistance of the transmission gate and devices in the inverter need to be calculated to use in each part of the following problem.

$$t_{pLH}(inv) = 0.693\left(0.8\frac{V_{DD}}{I_{Dsat}}\right)\left(\left(W_n+W_p\right)\left(6\,{}^{fF}\!/_{um^2}\cdot 0.2um\right)+\left(W_n+W_p\right)\left(0.6\,{}^{fF}\!/_{um}\right)\right)$$

$$= 0.693(6666.66\ \Omega)(2.7\ fF) = 12.47\ ps$$

$$t_{pHL}(inv) = 0.693(5471.96\Omega)(2.7\ fF) = 10.24\ ps$$

$$t_{p\,BUF}(avg) = 11.355\ ps$$

$$R_{n2.5} = \frac{V_{DD} - V_{out}}{I_{Dn}} = \frac{1.25}{(115)\left(\frac{0.5}{0.2}\right)\left((2.5-1.25-0.43)(0.63)-\frac{0.63^2}{2}\right)} = 13665.96\,\Omega$$

$$R_{p2.5} = \frac{V_{DD} - V_{out}}{I_{Dp}} = \frac{1.25}{(-30)\left(\frac{0.5}{0.2}\right)\left((-2.5-(-0.4))(-1)-\frac{1^2}{2}\right)} = 10416.66\,\Omega$$

$$R_{eq2.5} = R_{n2.5} \parallel R_{p2.5} = 5911.05\ \Omega$$

$$R_{n0} = \frac{V_{out}}{I_{Dn}} = \frac{1.25}{(115)\left(\frac{0.5}{0.2}\right)\left((2.5-0.43)(0.63)-\frac{0.63^2}{2}\right)} = 3932.37\,\Omega$$

$$R_{p0} = \frac{-V_{out}}{I_{Dp}} = \frac{-1.25}{(-30)\left(\frac{0.5}{0.2}\right)\left((-1.25-(-0.4))(-1)-\frac{1^2}{2}\right)} = 47619.04\,\Omega$$

$$R_{eq0} = R_{n0} \parallel R_{p0} = 3632.41\ \Omega$$

$$R_{AVG} = 4771.73\ \Omega$$

a) To calculate the optimal number of inverters for the chain, we just need to use the equation (6.39) from the book.

$$C_{node} = 2(0.5+0.5)\left(0.6\,{}^{fF}/_{um}\right) = 1.2\ fF$$

$$m_{opt} = 1.7\sqrt{\frac{t_{pBUF}}{CR_{AVG}}} = 2.39$$

Since the value for spacing is a whole number we must round to the nearest whole number spacing, which would be 2, leading us to **add 5 inverters**. Another viable approach is to round after determining the number of inverters to add. However, this leads to uneven spacing between inverters and does not work well with the optimization equations for delay. In a real design, it may yield a better result to take 12/2.39 = 5.02 inverters and round to 4. The delay models used in this approach do not consider adding an inverter to the beginning of the chain, however, that is the usual technique in practice. This is why we add (n/m -1) inverters.

b) Using equation (6.38) from the text, we can calculate for the delay using the optimal inverter spacing of 2 from the previous problem.

$$t_p = 0.69\left[C_{node}R_{AVG}\left(\frac{n(m+1)}{2}\right)\right] + \left(\frac{n}{m}-1\right)t_{pBUF}$$

$$t_p = 128\ ps$$

c) Now we need to set the equation for delay equal to 260 ps and solve for m_{opt}.

$$260\,ps = 0.69\left[(1.2\,fF)(4771.73)\left(\frac{12(m+1)}{2}\right)\right] + \left(\frac{12}{m}-1\right)(11.4\,ps)$$

$$Solving\ for\ m\ yields:$$

$$m_{opt} = 9.86$$

We must round to 9 to obtain our desired delay. This leads to adding a single inverter with spacing of 9. Since we are adding a single inverter, the ideal situation would be to place it in the middle of the inverter chain (m=6). This yields a delay of 177 ps, so we are definitely below the delay constraint.

Figure for Problem 3