# EECS 312: Digital Integrated Circuits
Homework #5 Solutions

1. **$V_{DD}/V_{TH}$ Scaling:**
   - **a)** See attached plot.
   - **b)** See attached plot.
   - **c)** Using readings from the graphs, for (a) we can tolerate reducing $V_{DD}$ to 2.1 V without $V_{th}$ scaling. This leads to a normalized energy consumption of 0.7. Using $V_{th}$ scaling, we can reduce the $V_{DD}$ to 2 V, and achieve a normalized energy of 0.64. By scaling $V_{th}$ we can save and additional 8-8.5% for a 30% delay penalty. As one can tolerate higher delay penalties, the relative savings due to $V_{th}$ scaling increase.
   - **d)** See attached plot.
   - **e)** Several hand calculations can lead to an exact answer:

$$P_{stat}(V_{DD}) = \tfrac{1}{2} V_{DD}\left(I_{offn} + I_{offp}\right)$$
$$P_{stat}(2) = 2(0.5)(0.5um)(10ua/um)\left(10^{(-0.344/0.09)} + 10^{(-0.32/0.09)}\right)$$
$$P_{stat}(2) = 2.144\,nW$$
$$P_{stat}(2.5) = 2.5(0.5)(0.5um)(10ua/um)\left(10^{(-0.43/0.09)} + 10^{(-0.4/0.09)}\right)$$
$$P_{stat}(2.5) = 0.329\,nW$$
$$\%Increase = 551.99$$

   - **f)** We can set the total power at VDD = 2 V equal to the total power at VDD = 2.5 V and solve for $\alpha_{sw}$. The scaling in this situation is usually going to be effective in reducing power.

$$P_{total}(2.5) = P_{dyn}(2.5) + 0.329\,nW$$
$$P_{total}(2.0) = P_{dyn}(2.0) + 2.144\,nW$$
$$P_{dyn}(2.0) + 2.144\,nW \le P_{dyn}(2.5) + 0.329\,nW$$
$$1GHz(\alpha_{sw})(3\,fF)(2^2) + 1.815\,nW \le 1GHz(\alpha_{sw})(3\,fF)(2.5^2)$$
$$12uW(\alpha_{sw}) + 1.815\,nW \le 18.75uW(\alpha_{sw})$$
$$\alpha_{sw} \ge 2.688\times10^{-4}$$

2. **Sequential Systems**
   - **a)** For device X1, it must be sized large enough to precharge the dynamic node to at least 90% of $V_{DD}$ (lower limit → rise-time). It is unlikely that a large precharge device at X1 will violate hold time at the input to the upper latch, however, at some point the capacitance added to the dynamic node will cause a setup time failure. (upper limit → capacitance added).
     For device Z1, we must size it large enough to pre-charge the dynamic node to around $V_{DD}$.
     We can use rise-time as an approximation of 0-90% charging time. More accurate solutions are acceptable (recalculating $R_{0\text{-}90}$ + charging constant, etc.).

$$t_{rise} \le 250\,ps$$
$$2.2(R_{10-90})C_L \le 250\,ps$$
$$2.2\left(0.55\frac{2.5}{300(W_p)}\right)(10 + 0.6W_p) \le 250\,ps$$
$$W_p \ge 0.513um$$

Device Z1 also could cause a hold time violation at the input to the lower latch if the pre-charge device is too large. For this path, we include no internal capacitances in the calculation.

$$\begin{aligned}
\left(t_{pLH} + kt_{fall-clk}\right) + \left(t_{pHL-inv} + kt_{rise-dynZ}\right) &\geq 85\,ps \\
\left(t_{pLH} + 13.5\,ps\right) + \left(31.41\,ps + kt_{rise-dynZ}\right) &\geq 85\,ps \\
t_{pLH-dyn} + kt_{rise-dynZ} &\geq 40.09\,ps \\
\left[0.69\left(0.8\tfrac{2.5}{300(W_{Z1})}\right) + 0.15\left(1.21\tfrac{2.5}{300(W_{Z1})}\right)\right]\left(10 + W_{Z1}(0.6)\right) &\geq 40.09\,ps \\
61.12\,ps / W_{Z1} &\geq 36.423\,ps \\
W_{Z1} &\leq 1.678\,um
\end{aligned}$$

**b)** The maximum delay through the circuit begins at node in1 and propagates to out1. (During evaluate). If there are additional questions about the calculation of any of these intermediate steps, please see Eric in office hours.

$$\begin{aligned}
Max &= \left(t_{D-Q}\right) + \left(t_{pHL-X} + kt_{rise-latch}\right) + \left(t_{pLH-Y} + kt_{fall-X}\right) + \left(t_{pHL-V} + kt_{rise-Y}\right) + \left(t_{pLH-M} + kt_{fall-V}\right) + t_{D-Q} \\
Max &= \left(35\,ps\right) + \left(62.66\,ps\right) + \left(42.26\,ps\right) + \left(44.89\,ps\right) + \left(49.72\,ps\right) + 35\,ps \\
Max &= 269.53\,ps
\end{aligned}$$

**c)** The minimum delay is calculated from in2 to out2 as follows:

$$\begin{aligned}
Min &= \left(t_{D-Q}\right) + \left(t_{pHL-Z} + kt_{rise-latch}\right) + \left(t_{pLH-W} + kt_{fall-Z}\right) + t_{D-Q} \\
Max &= \left(35\,ps\right) + \left(32.61\,ps\right) + \left(33.23\,ps\right) + 35\,ps \\
Max &= 135.84\,ps
\end{aligned}$$

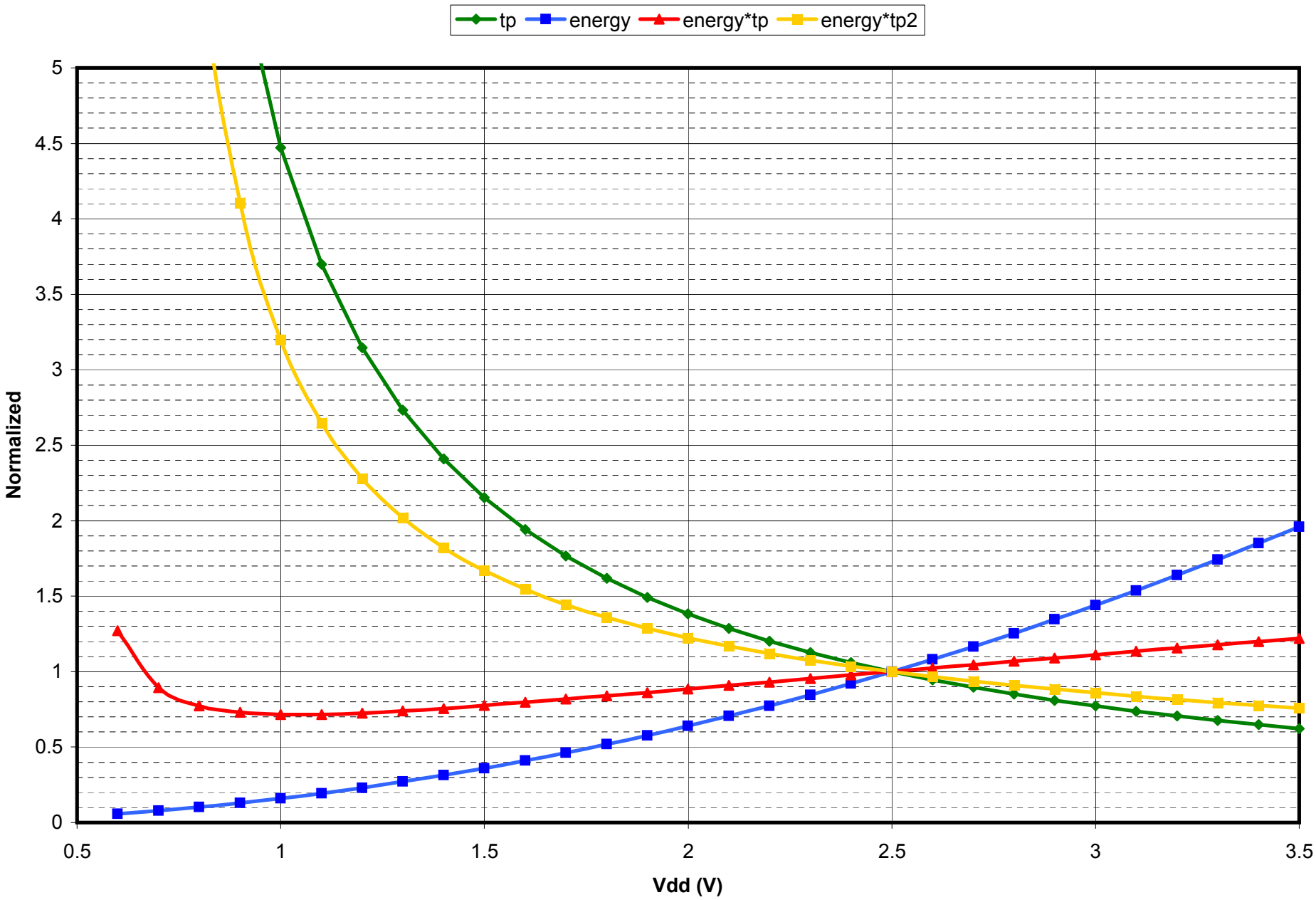
**d)** To determine whether this circuit operates at a frequency of 2GHz, we must analyze the circuit for setup time and hold time violations. The values calculated in (b) and (c) will be useful to complete this analysis. First, we must consider the max-delay path and determine whether the setup time is violated. If the input to latch in1 arrives at the latest time (25 ps before the clock edge) we have a D-Q delay that begins propagating 25 ps before the clock edge. Therefore, this contributes 35-25 or 10 ps to our maximum delay time. Now, we can add the delays from the maximum delay calculation until inverter M. This leads to: 10+62.66+42.26+44.89+49.72 = 209.53 ps. Finally, we can check if the signal arrives before the setup time is violated. 209.53 ps is less than 225 ps ($T_{cycle} - T_{setup}$). There is no setup time violation.

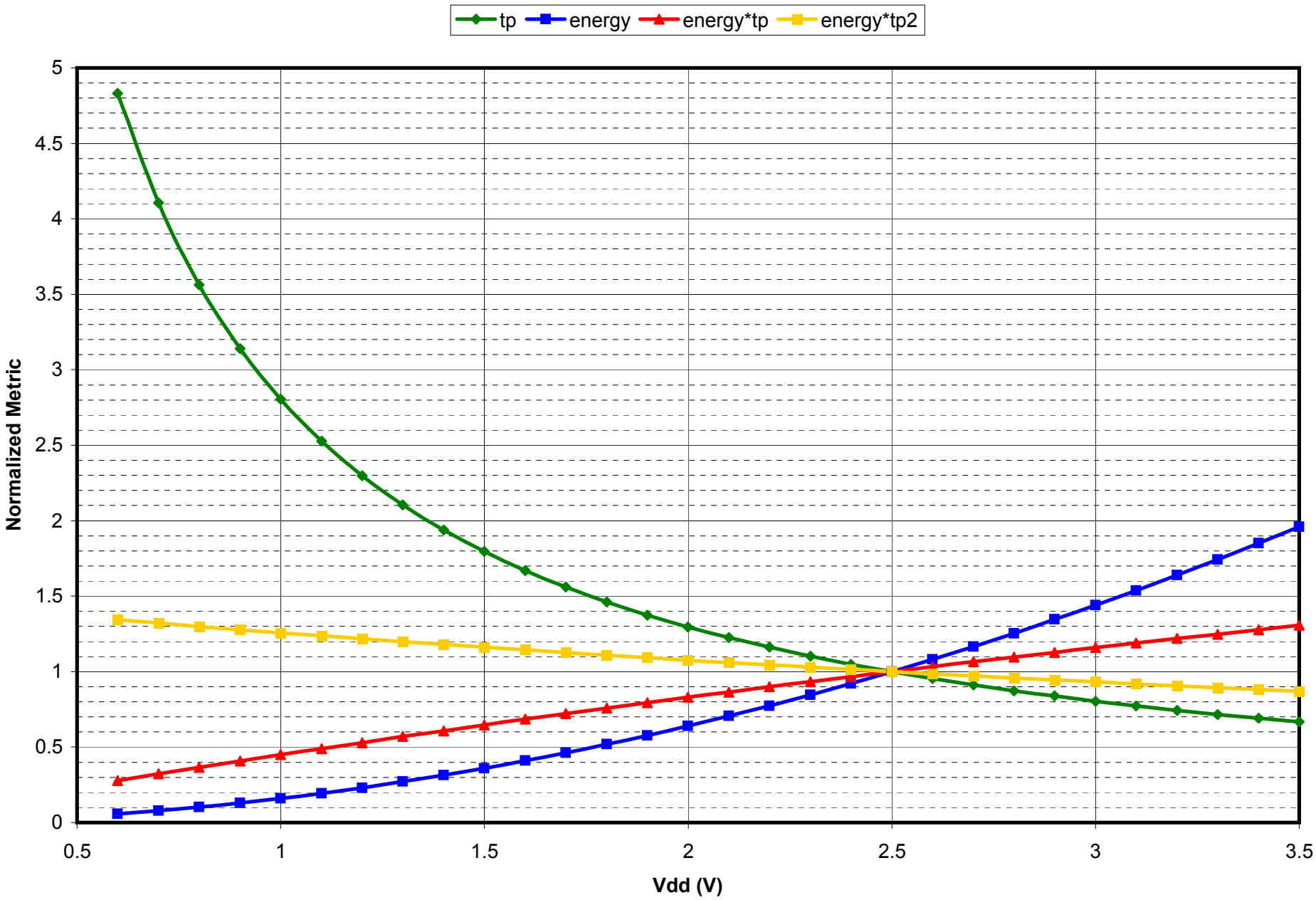
Now we must check the min-time path from (c) to determine whether there is a hold time violation in our circuit. Before we consider the numbers in this problem, we should think about how to set-up this condition. Hold time occurs when the input to a latch changes within a certain time relative to the closing edge of a latch. Therefore, we would require an evaluate path to propagate through Z and W AFTER the clock falls. This is impossible (in the absence of clock skew) since the pre-charge devices are activated when the clock falls. Therefore, since we know that the sizes of pre-charge devices fall within the acceptable range from (a), we can say there is no hold time violation.

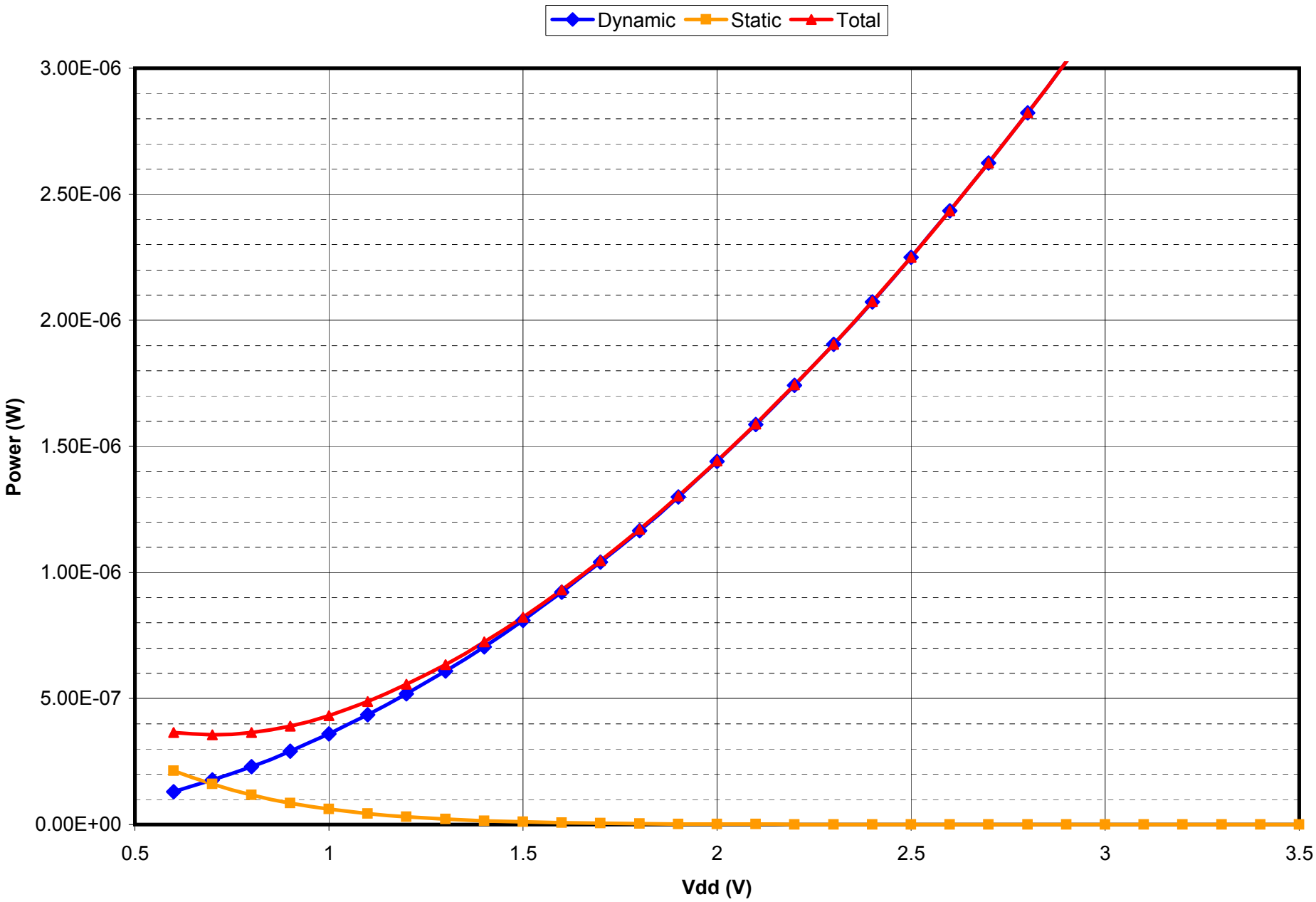
This circuit should work properly at 2GHz.

**e)** A simple solution would be to add a pair of inverters between inverter W and the latch in 2. This path is non-critical and easily solves a hold time violation in a pinch (this is obviously non-optimal, but sometimes you just need to fix something).

## EECS 312 HW5 P1 A: Energy and Delay Metrics vs. Vdd Scaling




EECS 312 HW5 P1 B Energy Delay Metrics vs. Vdd/Vth Scaling
tp
energy
energy*tp
energy*tp2
Normalized Metric
Vdd (V)
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
0.5
1
1.5
2
2.5
3
3.5


EECS 312 HW5 P1 D Power Consumption vs. Vdd/Vth Scaling
Dynamic
Static
Total
3.00E-06
2.50E-06
2.00E-06
1.50E-06
1.00E-06
5.00E-07
0.00E+00
Power (W)
0.5
1
1.5
2
2.5
3
3.5
Vdd (V)