EECS 312: Digital Integrated Circuits
Homework #3 Solutions

1. Energy and Power Consumption:

a) Here we consider the dynamic power consumed by the IC (not including short circuit power). The key is to recognize that we have clocked nodes (α_{sw} = 1) and some un-clocked nodes in the design (α_{sw} < 1). The dynamic power can be calculated separately for both types of nodes and summed to find the total dynamic power.

$$P_{dyn} = P_{dyn,clocked} + P_{dyn,un-clocked}$$

$$P_{dyn,clocked} = N\left(C_{Lavg}V_{DD}^{2}\right)f_{clock}\alpha_{sw,clocked}$$

$$P_{dyn,clocked} = 10,000\left(40\,fF(2.5)^{2}\right)1E9(1) = 2.5W$$

$$P_{dyn,unclocked} = 5E6\left(6\,fF(2.5)^{2}\right)1E9(0.10) = 18.75W$$

$$P_{dyn} = 2.5 + 18.75 = 21.25W$$

$$t_{battery} = \frac{39W-h}{21.25W} = 1.8353\ hours$$

b) In part b, we calculate the static power consumption of the IC and add that to the dynamic power from part A.

$$I_{off(avg)} = 10\ uA/um\left(W_{navg}\right)\left(10^{\frac{-V_{th}}{S_{s}}}\right)$$

$$I_{off(avg)} = 40uA\left(10^{\frac{-0.25}{0.09}}\right) = 66.724\ nA/device$$

$$P_{static} = NI_{off(avg)}V_{DD} = (5,010,000)(66.724\ nA)(2.5) = 835.72\ mW$$

$$P_{total} = P_{static} + P_{dyn} = 22.0857\ W$$

$$t_{battery} = \frac{39W-h}{22.0857W} = 1.76585\ hours$$

c) Now we recalculate the total power (static and dynamic) considering a reduction in supply voltage V_{DD} to 1.8 V.

$$P_{dyn,clocked} = 10,000\left(40\,fF(1.8)^{2}\right)1E9(1) = 1.296\ W$$

$$P_{dyn,unclocked} = 5E6\left(6\,fF(1.8)^{2}\right)1E9(0.10) = 9.72\ W$$

$$P_{static} = 5.01E6(66.724\ nA)(1.8) = 601.72\ mW$$

$$P_{total} = 11.6177\ W$$

$$t_{battery} = \frac{39W-h}{11.6177W} = 3.3569\ hours$$

d) Returning to a normal supply voltage of 2.5V, we consider a reduction in frequency from 1 GHz to 600 MHz.

$$P_{dyn,clocked} = 10{,}000\big(40\,fF(2.5)^2\big)6E8(1) = 1.5\ W$$

$$P_{dyn,unclocked} = 5E6\big(6\,fF(2.5)^2\big)6E8(0.10) = 11.25\ W$$

$$P_{static} = 5.01E6(66.724\ nA)(2.5) = 835.72\ mW$$

$$P_{total} = 13.5857\ W$$

$$t_{battery} = \frac{39W-h}{13.5857W} = 2.8707\ hours$$

In practice, the voltage reduction is often used with frequency scaling in portable applications. As we reduce the voltage, the delay of every device is increased in our system and therefore a reduction in frequency is required to operate the device without errors. It is interesting to note that the frequency reduction technique does not reduce static power consumption, so as static power increases (through increases in I_{off} with each technology) dual voltage/voltage reduction schemes will become increasingly attractive in all design spaces (not just portable).

2. Self Loading Effect:
a) See attached plot.
b) From inspection of the plot generated in part A, we realize that increasing the width of the transistor delivers diminishing returns to our delay t_{pHL}. As size is increased, device area and power (through device capacitances) also increase. Therefore, we would like to select sizes for the devices near the "inflection point" where the derivative of delay flattens. For 5fF load, a size between 0.5 – 1um is reasonable. For 10fF load, a size of 0.7 – 1.2 um is reasonable and for a 15fF load, a size between 0.9 – 1.4um is near optimal (considering the plot we have constructed). After these sizes, the self-loading effect dominates the delay calculation and the intrinsic device capacitances therefore dominate the overall load capacitance. At this point, increasing W_n results in no performance gain, as the additional current is counteracted by the increase in capacitance.
c) See attached plot.
d) To determine reasonable device sizes from the EDP plot, we consider the minimum points on each trace to be desirable, as we aspire to minimize both energy consumption and delay time.

5fF load → ~0.9 um
10fF load → ~2.1 um
15fF load → ~3 um

As with part B, after these points in each trace, intrinsic device capacitance begins to dominate the overall capacitance and the delay is not reduced and energy consumption begins to increase. Clearly, larger devices do not always yield better performance. The sizes from the EDP plot are slightly larger than the devices sizes from the delay derivative analysis alone. At very small device sizes, the energy required to charge the intrinsic device capacitances is negligible (dominated by C_{FAN}). While optimizing EDP, saving additional delay time (no matter how small) is beneficial as long as the energy is not increased. However, considering the area of the devices (increasing with W_n), smaller sizes as in part B, may be a better choice in many practical circumstances.

3. Complex Logic Gates:
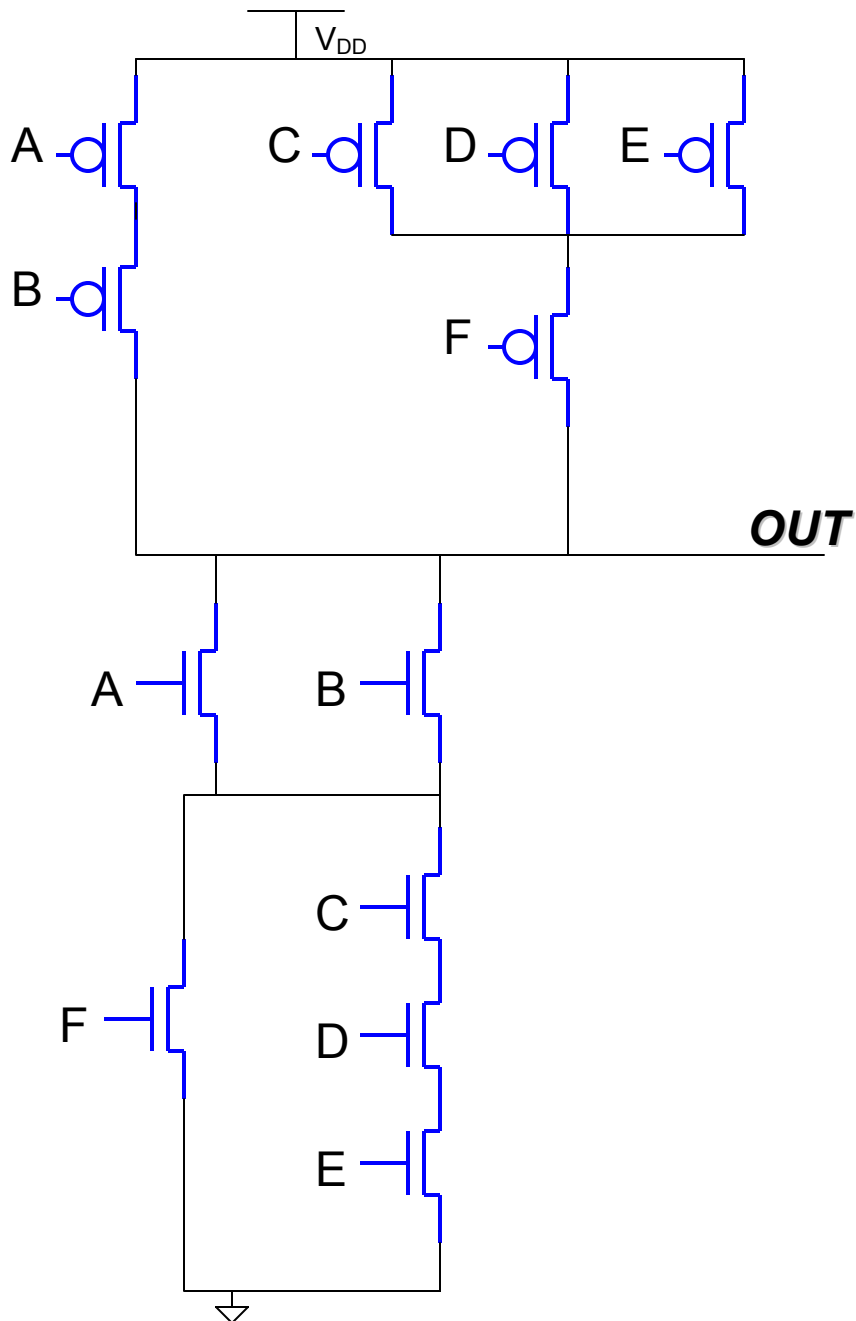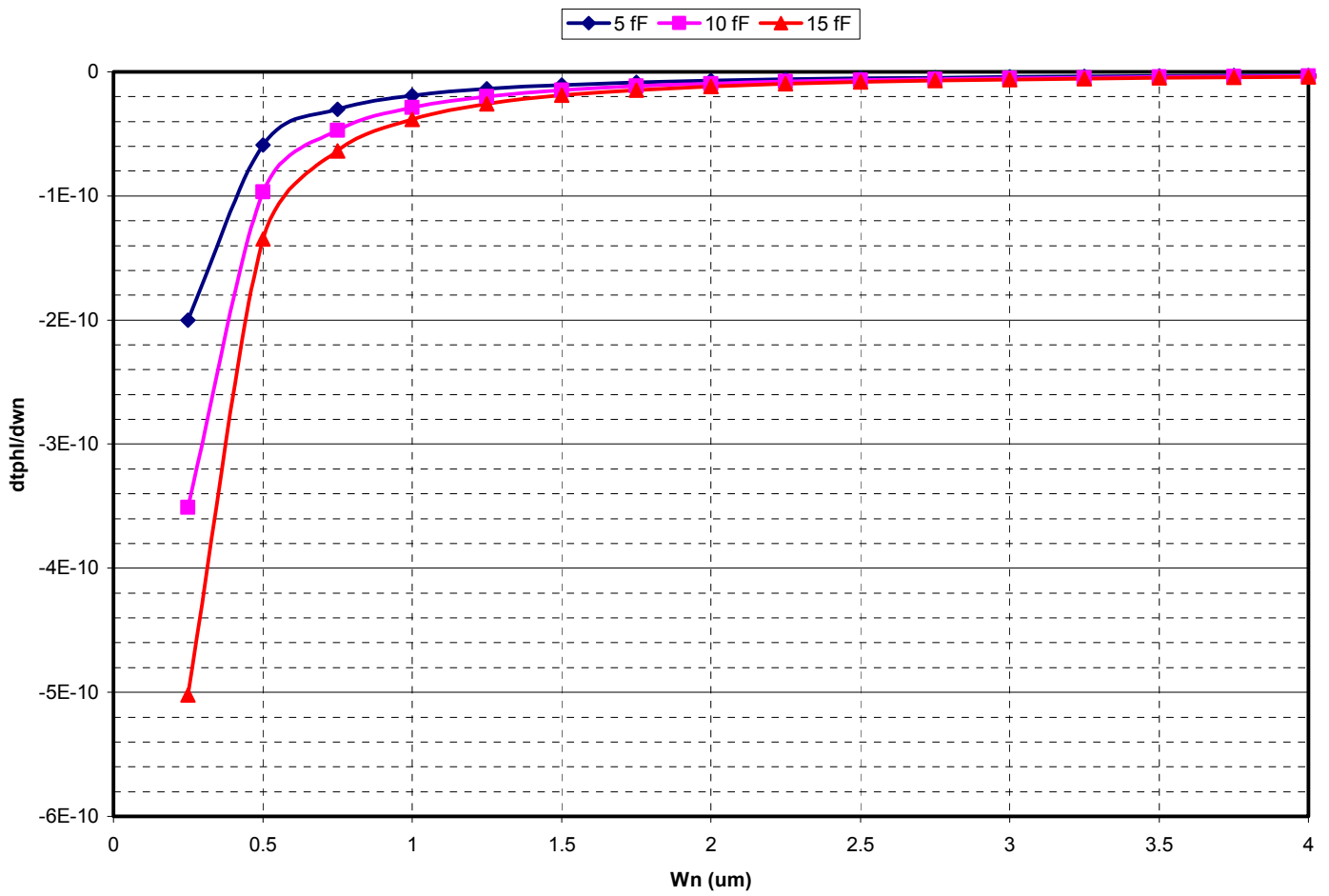**a)** $OUT = \overline{G\big(ABC + (F(D+E))\big)}$

b) Using DeMorgan's…

$$OUT = \overline{G(ABC + (F(D+E)))}$$
$$= \overline{G} + \overline{(ABC + (F(D+E)))}$$
$$= \overline{G} + \left(\left(\overline{ABC}\right)\left(\overline{F(D+E)}\right)\right)$$
$$= \overline{G} + \left(\left(\overline{A} + \overline{B} + \overline{C}\right)\left(\overline{F} + \overline{(D+E)}\right)\right)$$
$$= \overline{G} + \left(\left(\overline{A} + \overline{B} + \overline{C}\right)\left(\overline{F} + \overline{D}\,\overline{E}\right)\right)$$

Note the final answer of A and B are interchangeable; it depends on whether you generated the original equation from the PMOS or the NMOS network.

c) Drawing the Complex Gate (many topologies are possible – just one below)

EECS 312 HW3 P2a: dtphl vs. Wn

EECS 312 HW3 P2C: Wn vs. EDP