# EECS 312: Digital Integrated Circuits
Homework #8 Solutions

1. **Interconnect and Scaling:**
   - **a.** What is the total **capacitance** of this wire? Use three models:
     - i. The simple rule of thumb yields **2 pF/cm * 1.4cm = 2.8 pF**
     - ii. Using the detailed equation:

$$C_{wire} = 3.9(8.854E-14)\left[\left(\frac{1.5}{0.5}\right) + 0.77 + 1.06\left(\frac{1.5}{0.5}\right)^{0.25} + 1.06\left(\frac{0.8}{0.5}\right)^{0.5}\right] = 2.247\ pF/cm$$

$$C_{wire} = 2.247\ pF/cm(1.4cm) = 3.145\ pF$$

     - iii. Use table 4-2 from Rabaey…

$$\begin{aligned} C_{total} &= C_{pp} + C_{fringe} \\ &= (1.5um)(14{,}000um)(38aF/um^2) + 2(52aF/um)(14{,}000um) \\ &= 798\ fF + 1456\ fF \\ &= 2.254\ pF \end{aligned}$$

   - **b.** What is the total **resistance** of the wire?
     - i. Aluminum (Al)

$$R_{sheet} = \frac{\rho}{H_{wire}} = \frac{2.7E-8}{0.8um} = 0.03375\,\Omega$$

$$R_{total} = R_{sheet}\frac{L}{W} = R_{sheet}\frac{14{,}000}{1.5} = 315\,\Omega$$

     - ii. Copper (Cu)

$$R_{sheet} = \frac{\rho}{H_{wire}} = \frac{1.7E-8}{0.8um} = 0.02125\,\Omega$$

$$R_{total} = R_{sheet}\frac{L}{W} = R_{sheet}\frac{14{,}000}{1.5} = 198.33\,\Omega$$

   - **c.** Using the detailed delay model from class, we consider any term with $r_w$ to be due to wire resistance.

$$\begin{aligned} C_{int} &= 0.6\,fF/um(30um) = 18\ fF \\ C_{wire} &= 3.145\,pF \\ C_{load} &= 6(6\,fF/um^2)(0.2um)(30um) = 216\ fF \\ r_w &= 0.0225\,\Omega/um \\ c_w &= 0.2246\,fF/um \\ R_d &= 0.8\left(\tfrac{2.5}{10(731E-6)}\right) = 273.6\,\Omega \\ t_{phl} &= 0.69R_d(18 + 3145 + 216\,fF) + 0.38(315)(3145\,fF) + 0.69(315)(216\,fF) \\ &= 637.9\,ps + 376.5\,ps + 46.9\,ps = 1.06ns \\ & 40\%\ due\ to\ r_{wire} \end{aligned}$$

**d.** Scale two generations. $S^2$ = ~2, assuming 2.

$$t_{phl}(scaled) = 0.69(R_d)\left(\frac{C_{int}}{S^2} + C_{wire} + \frac{C_{gate}}{S^2}\right) + 0.38(S^4 R_{wire})(C_{wire}) + 0.69(S^4 R_{wire})\left(\frac{C_{gate}}{S^2}\right)$$

$$= 0.69(273.6)(9fF + 3145fF + 108fF) + 0.38(793)(3145fF) + 0.69(793)(108fF)$$

$$= 615.8ps + 948.1ps + 59.1ps = 1.62ns$$

$$62\%\ due\ to\ r_{wire}\ (despite\ Copper)$$

2. **Repeater Design:**

**a.** Use the tapered buffering approach to driving this wire for optimal delay…

$$C_{in} = (3um)(6fF/um^2)(0.2um) = 3.6fF$$

$$C_L = C_{wire} + C_{load} = 3.145pF + 216fF$$

$$F = \frac{3.361pF}{3.6fF} = 933.6$$

$$f_{opt} \approx 3.6 \rightarrow N = \frac{\log(933.6)}{\log(3.6)} = 5.339$$

$$t_{p0} = 0.69(0.5)\left(0.8\left(\frac{2.5}{(731)}\right) + 0.8\left(\frac{2.5}{2(300)}\right)\right)(3.6fF) = 7.538ps$$

$$t_{p0}(5) = (5)(7.538ps)\left(1 + \sqrt[5]{933.6}\right) + 0.38(315)(3.145pF) + 0.69(315)(216fF) = 609.1ps$$

$$t_{p0}(6) = (6)(7.538ps)\left(1 + \sqrt[6]{933.6}\right) + 0.38(315)(3.145pF) + 0.69(315)(216fF) = 610.1ps$$

$$W_{total}(5) = \left(\frac{f^N - 1}{f - 1}\right)A_{unit} = \left(\frac{3.93^5 - 1}{2.93}\right)(3um)(0.25um) = 239.7um^2$$

**b.** Use the repeater insertion technique (pg. 466-467) to optimize delay. Use the detailed approach of 9.9 and 9.10 in the text. Find the optimal delay and the total area of the transistors used in the repeater based design.

$$R_d = 0.8(0.5)\left(\frac{2.5}{731} + \frac{2.5}{2(300)}\right) = 3034\Omega$$

$$C_d = 3.6fF$$

$$m_{opt} = L\sqrt{\frac{0.38rc}{0.69R_d C_d(\gamma + 1)}} = 14{,}000\sqrt{\frac{0.38(0.0225)(0.2246fF)}{0.69(3034)(3.6fF)(2)}}$$

$$m_{opt} = 4.99$$

$$s_{opt} = \sqrt{\frac{R_d c}{rC_d}} = 91.72$$

$$t_p = 4\left(0.69\frac{3034}{91.72}\left(91.7(3.6fF) + \frac{3.145pF}{5} + 91.7(3.6fF)\right) + 0.69\left(\frac{315}{5}\right)(91.7(3.6fF)) + 0.38(0.225)(0.0225)(2800)^2\right)$$

$$+\left(0.69\frac{3034}{91.7}\left(91.7(3.6fF) + \frac{3.145pF}{5} + 216fF\right) + 0.69\left(\frac{315}{5}\right)(216fF) + 0.38(0.225)(0.0225)(2800)^2\right)$$

$$t_p = 286.64ps$$

$$W_{total} = 5(91.72)(3um)(0.25um) = 343.95um^2$$

**c.** This comparison is not completely even, since in (a), the input capacitance is held fixed to a 3um gate. In (b), the input capacitance of the repeater chain is allowed to be very large, 91.72X the input cap of (a). Therefore the delay comparison is not appropriate, since the repeater chain loads the previous stage more than the tapered buffer chain. An appropriate comparison could be made by creating a small tapered buffer chain for the input of the repeater setup.