INSTRUCTIONS

Read all of the instructions and all of the questions before beginning the exam.

There are four problems on this midterm exam, totaling 100 points. The credit for each problem is given to help you allocate your time accordingly. You have a total of 90 minutes to finish this exam. Do not spend all of your time on one problem.

This is an open-book, open-notes exam.

Please place a circle or box around your answers (quantitative ones).

I have <u>underlined</u> the portion of each question that specifically lists what you need to provide in your answer.

Unless otherwise noted on a particular problem, you must show your work (in the space provided plus the back of the pages) for all problems to receive full credit; simply providing answers will result in only partial credit, even if the answers are correct. If you require extra space beyond what is provided, be sure to turn in any material that is required to support your solutions. Note that there is extra work space at the end of this exam booklet.

Turn in the entire exam, including this cover sheet.

Be sure to provide units wherever necessary.

Problem 1 (18 points)

Figure 1a is a plot of the VTC of the CMOS inverter (using our default technology) shown in Figure 1b.
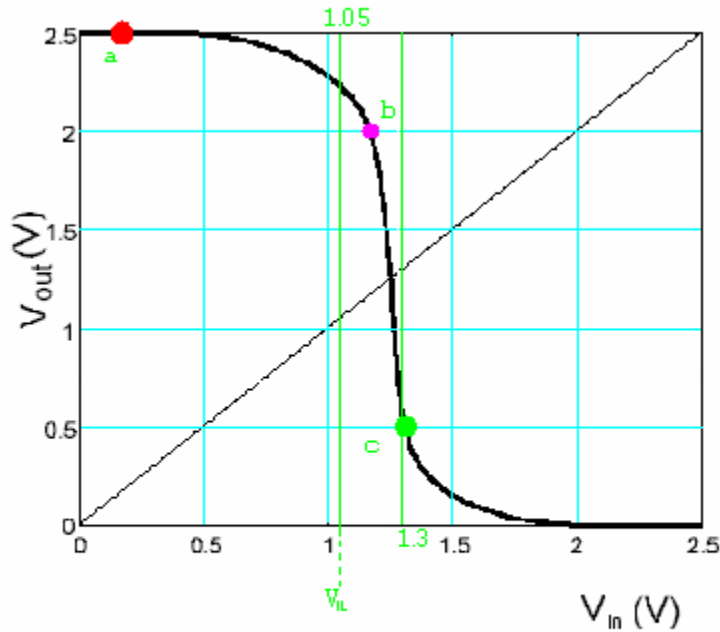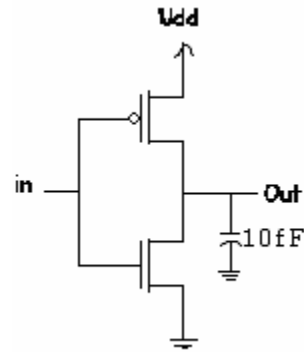

Figure 1a
CMOS VTC

Figure 1b
CMOS inverter

a) The VTC has three points marked on it – **a**, **b**, & **c**. <u>List the region of operation</u> of the NMOS and the PMOS for all three points in the below table. (6 points)

Point	NMOS operating region	PMOS operating region
a		
b		
c		

b) Give quantitative <u>justification for the operating region at point **c**</u> for both NMOS and PMOS. (4 points)

c) If the capacitance at the output of the inverter is increased to 100fF, what change in V_{IL} would you observe? Give a qualitative explanation. (4 points)

d) Based on the VTC shown, do you expect t_{rise} at node OUT to be less than, greater than, or roughly equal to t_{fall} at node OUT? Support your answer. (4 points)

Problem 2 (11 points)

Our default technology with L_{drawn} of 0.25μm is approximately two technology generations old. The scale factor between consecutive technologies is typically 1.4. Starting with the gate in Figure 2, apply full scaling to our technology to reflect two generations of technology scaling. Then, <u>compute the ratio of dynamic to static power</u> for the new gate (in the target technology). To find dynamic power, use the switching patterns of Figure 3 which are applicable for the original technology. Assume subthreshold swing S_s is constant across scaling at 90mV/decade and that the load capacitance (5 fF in the initial technology) represents the gate-to-channel capacitance of the fanout stages. This last point should help you determine how the load changes with scaling. Assume the clock frequency scales with the inverse of gate propagation delay and the node switching activity remain constant with scaling. For computing static power, assume the input V_{in} is 0 V.
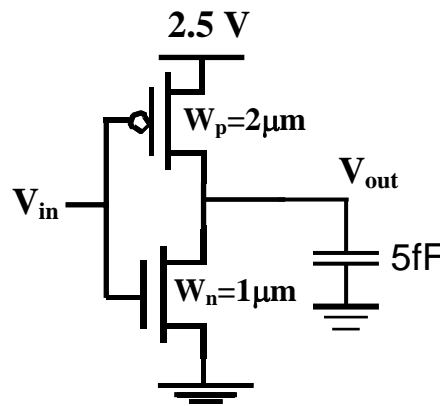

Figure 2: Initial gate in our default technology.
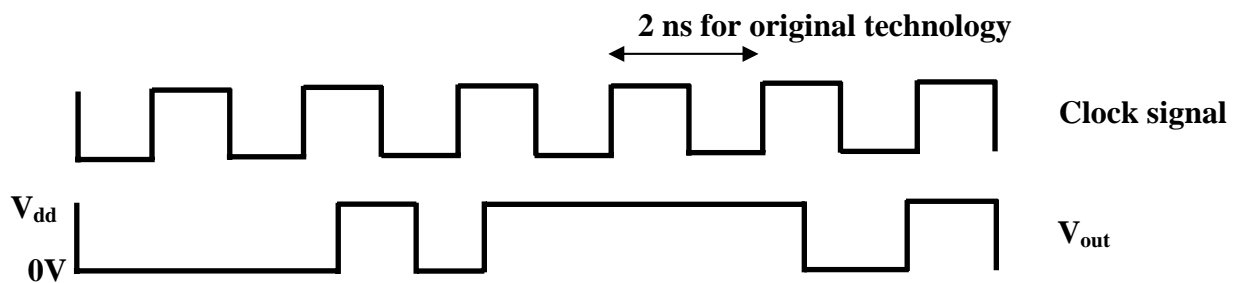

Figure 3: Clock and output node waveforms. Clock period is shown for the initial technology.

Problem 2 work space

Problem 3 (50 points)

a) <u>Implement the function X</u> below in a single complex combinational gate using the minimum number of transistors and with the minimum number of transistors connected to the output (X) node. (8 points)

$$X = \overline{(A \bullet B + G) \bullet (C \bullet D + E + F)}$$

b) <u>Calculate the width of the PMOS and NMOS</u> devices in INV1 in Figure 4 below such that the delay from a falling "step" input at node IN to the falling output at node OUT is equal to 110ps and the Beta ratio of INV1 matches the Beta ratio in INV2. INV2 has the following device sizes: $W_p = 6\mu m$ and $W_n = 3\mu m$. All relevant capacitances at node OUT are included in the lumped 78 fF of capacitance notated on the figure (i.e., do not calculate any capacitances relating to node OUT). Let the only capacitance at node MID be equal to the C_{gc} of INV2. You must consider the input slope effect on delay for INV2, using a value of K=0.1 within the model presented in the lecture. (11 points)
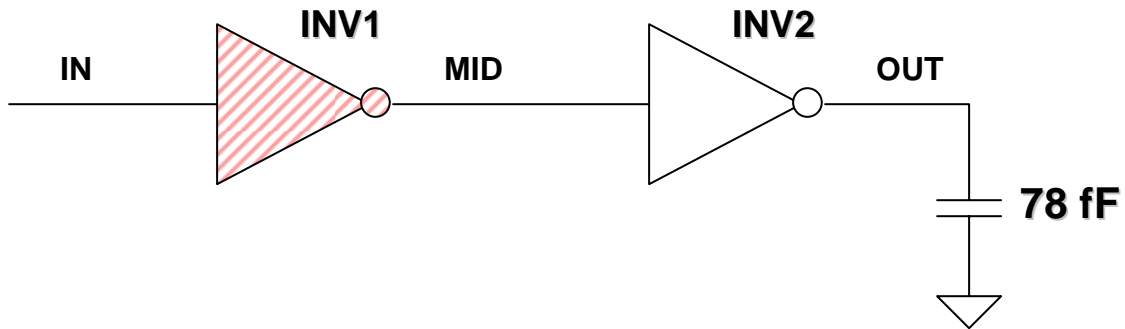

Figure 4

c) <u>Size the complex gate</u> from part (a) such that its pull-up and pull-down networks have the same worst-case output resistance as INV1 that you sized in part (b). You can label transistors in part (a) and list their sizes below to answer this question. (7 points)

d) <u>Label and compute the values of the internal capacitances</u> on the complex gate diagram from part A. Let $C_{sb} = C_{db} = 0.6$ fF/μm of device width (these values are valid for both NMOS and PMOS) connected to each internal node. Considering the internal capacitances, <u>identify the worst-case t_{pLH} transition</u> (including the initial and final states). (8 points)

e) <u>Calculate the worst case t_{pLH}</u> of the complex gate with a total output load of 60 fF (this value includes *all* parasitic capacitances at the output node) while ignoring internal capacitances. Then, under the same conditions, <u>re-calculate the delay</u> considering the internal capacitances. <u>What percentage error</u> do you observe for t_{pLH} when neglecting the internal capacitances of this complex gate? (12 points)

f) Suppose that the total output load capacitance increases by a factor of 10 to 600fF. With the device sizes fixed, <u>how do you expect the error from part (e) to change</u> as a result of this new load capacitance? Qualitatively support your answer; you do not need to recalculate anything for this problem. (4 points)

Problem 3 work space

Problem 4 (21 points)

Figure 5 shows a logic gate which looks similar to a CMOS inverter but the NMOS and PMOS have been exchanged. Use our default technology parameters in this problem and ignore body bias throughout the problem. You do not need to calculate any capacitances in this problem.
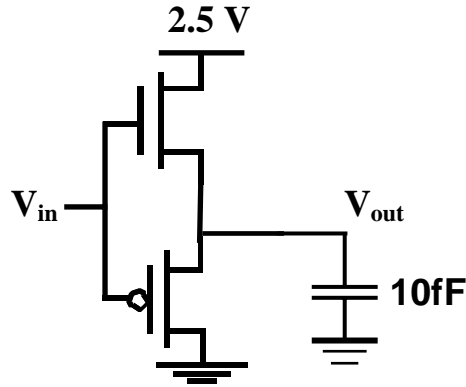

Figure 5

(a) <u>Roughly sketch the VTC</u> of this logic gate (draw V_{out} against V_{in} as V_{in} sweeps from 0 to V_{dd}). <u>Provide accurate numerical values</u> for (i) V_{OL} and (ii) V_{OH} and mark them on your VTC. (10 points)

(b) <u>Compute the energy</u> dissipated by this gate in one complete switching cycle. (Assume that all the capacitance is lumped into the 10fF load at the output node). (7 points)

(c) <u>Does this gate exhibit static power dissipation</u>, other than leakage currents? Justify your answer. (4 points)