EECS 312: Digital Integrated Circuits
Homework #7 Solutions

1. DRAM:

    a. During a WRITE-1 operation, the bit-line is charged to V_{DD} and the word-line is held at a high voltage. Since the transistor in the DRAM is an NMOS device it stores a "weak" 1 on the internal capacitance, so we need to consider the body effect.

$$\begin{aligned}
V_{write-1} &= V_{DD} - V_{tn}(V_{write-1}) \\
&= 2.5 - \left(0.43 + 0.4\left(\sqrt{0.8 + V_{write-1}} - \sqrt{0.8}\right)\right) \\
&= 1.785\ V
\end{aligned}$$

$$\begin{aligned}
V_{read-1} &= \frac{C_{BL}V_{PRE} + C_{int}V_{write-1}}{C_{total}} \\
&= \frac{187.5\,fC + 44.625\,fC}{175\,fF} \\
&= 1.3264\,V
\end{aligned}$$

    b. Now we can solve for limits upon the pre-charge voltage that will allow us to sense the bit-line voltage swing with our 50-mV sense amplifier. The READ-1 case will constrain how high we can set the pre-charge and the READ-0 case will set how low we can drop the pre-charge.

$$V_{final} - V_{PRE-HI} = 0.05$$

$$\frac{1.785 C_{int} + V_{PRE-HI}C_{BL}}{C_{int} + C_{BL}} - V_{PRE-HI} = 0.05$$

$$-0.142857 V_{PRE-HI} = -0.205$$

$$V_{PRE-HI} = 1.435V$$

$$V_{PRE-LO} - \frac{V_{PRE-LO}C_{BL}}{C_{BL} + C_{int}} = 0.05$$

$$0.142857 V_{PRE-LO} = 0.05$$

$$V_{PRE-LO} = 0.35V$$

    c. Now, we want to maximize the voltage swing available to our sense amplifier, by selecting the pre-charge voltage that will lead to the highest minimum swing from a READ-0 and READ-1. It turns out to be a set of linear equations with opposite slope, so the maximum value occurs when the swing voltages are equal, hence we solve for the intersection of the equations.

$$V_{swing-HI} = \frac{1.785 C_{int} + V_{PRE}C_{BL}}{C_{total}} - V_{PRE}$$

$$V_{swing-LO} = V_{PRE} - \frac{V_{PRE}C_{BL}}{C_{total}}$$

$$V_{swing-HI} = V_{swing-LO} = 127.5\,mV$$

$$V_{PRE} = 0.8925V$$

d. The plot of refresh times is included at the end of the solutions. To calculate refresh time, we need to calculate the leakage current when a 1 is stored and when a 0 is stored in the storage node of the DRAM. When a 1 is stored, the bit-line will be at a pre-charge voltage lower than the stored value, and will be the source of the transistor. We can calculate the V_{th} from the pre-charge voltage and then the relevant leakage current. When a 0 is stored, the source will be the internal node of the DRAM cell. Therefore, we need to find the voltage range of interest (from 0 to the highest voltage that still produces a 50 mV swing) and calculate V_{th} and the leakage at the midpoint of the range. Then we need to calculate the amount of charge required to charge the internal node to the last point (voltage-wise) where a 50 mV swing is produced on the output. Using the relationship between CV and current, we can find the refresh time.

Using the plot, the ideal voltage to reduce the amount of energy spent refreshing the DRAM is around **1.40-1.41 V**. Note that the technique used in the problem is an aggressive approximation.

e. If the word-line is charged between -0.5 and 3 V, the DRAM will have much better performance. When the 3V is passed across the gate during a write, the V_{th} drop problem will be greatly reduced and a much higher value will be stored on a WRITE-1. When all of the DRAM cells are deactivated, the -0.5V on the gate will reduce leakage current, which improves the refresh time – reducing the frequency that we need to restore all of the values in the DRAM. A drawback to doing this is the increased power consumption on the word-line and the complexity of having multiple voltage supplies on chip.

2. Buffer Design:

a. To find the optimal delay and number of buffer stages we use the equations from the book.

$$F = \frac{C_L}{C_{g,1}} = \frac{4\,pF}{1.2\,fF(1.5)} = 2222.222$$

$$f_{opt} \approx 3.6 \rightarrow N = \frac{\log(2222.22)}{\log(3.6)} = 6.016$$

$$R_{unit} = \frac{1}{2}\left(0.8\left(\frac{2.5}{(731E-6)(0.5)}\right) + 0.8\left(\frac{2.5}{(300E-6)(1)}\right)\right) = 6069.31\Omega$$

$$t_{p0} = 0.693R_{unit}C_{unit} = 0.693(6069.31)(1.8E-15) = 7.571\,ps$$

$$t_p(6) = (6)t_{p0}\left(1 + \sqrt[6]{2222.22}\,/\,\gamma\right) = 209.5\,ps$$

$$t_p(7) = (7)t_{p0}\left(1 + \sqrt[7]{2222.22}\,/\,\gamma\right) = 212.3\,ps$$

b. To calculate the energy of the buffer chain, we need to sum all of the gate capacitances and the junction capacitances of the buffers and use the $C_LV_{DD}^2$ equation.

$$C_{chain} = \sum C_g + \sum C_{int} = (1+\gamma)\sum C_g$$

$$= (1+\gamma)\left(\frac{f^N-1}{f-1}C_{unit}\right) = 3.06\,pF$$

$$E_{chain} = C_{chain}V_{DD}^2 = 19.125\,pJ$$

$$E_{total} = (C_{chain} + C_L)V_{DD}^2 = 44.125\,pJ$$

c. There are two techniques to investigate for reducing the energy consumption of this tapered buffer chain. Using the optimal design and reducing V_{DD}, and resizing the chain.

Technique 1: Reducing V_{DD}

$$1.5(209.5\ ps) = (6)t_{p0}\left(1 + \sqrt[6]{2222.22}\right)$$

$$t_{p0} = 11.356\ ps$$

$$R_{unit} = 9143.55\Omega$$

$$V_{DD} = 1.583V$$

$$E_{chain} = C_{chain}V_{DD}^{2} = (3.06\,pF)(1.583)^2 = 7.668\ pJ$$

$$E_{total} = (C_{chain} + C_L)V_{DD}^{2} = (7.06\,pF)(1.583)^2 = 17.692\ pJ$$

Technique 2: Resizing the Chain (remove buffers and recalculate f)

My initial approach to solving this problem was to allow the final stage to consume a larger portion of the delay constraint while driving the load. This method will require less energy consumption. A simpler constant f technique is also included below for students who did not make this assumption.

Remove 1 buffer and try N=5

$$1.5(209.5\ ps) = (4)t_{p0}(1 + f_5) + t_{p0}\left(1 + \frac{4\,pF}{1.8\,fF\left(f_5^{4}\right)}\right)$$

$$314.25\ ps = 30.284\ ps(1 + f_5) + 7.571\left(1 + \frac{2222.22}{f_5^{4}}\right)$$

$$f_5 = 3.098$$

$$E_{chain} = C_{chain}V_{DD}^{2} = (0.488\,pF)(2.5)^2 = 3.05\ pJ$$

$$E_{total} = (C_{chain} + C_L)V_{DD}^{2} = (0.488 + 4)(2.5)^2 = 28.05\ pJ$$

Remove 2 buffers and try N=4

$$1.5(209.5\ ps) = (3)t_{p0}(1 + f_4) + t_{p0}\left(1 + \frac{4\,pF}{1.8\,fF\left(f_4^{3}\right)}\right)$$

$$314.25\ ps = 22.713\ ps(1 + f_4) + 7.571\left(1 + \frac{2222.22}{f_4^{3}}\right)$$

$$f_4 = 4.529$$

$$E_{chain} = C_{chain}V_{DD}^{2} = (0.428\,pF)(2.5)^2 = 2.676\ pJ$$

$$E_{total} = (C_{chain} + C_L)V_{DD}^{2} = (0.428 + 4)(2.5)^2 = 27.676\ pJ$$

N=3 cannot produce a delay within the constraint.

When considering the chain energy only, the resizing approach seems far superior; however, the V_{DD} scaling overall is much more effective in reducing energy (and easier to implement).

Alternate Solution

Remove 1 buffer and try N=5

$$f_5 = \sqrt[5]{2222.22} = 4.67$$

$$t_{p0} = 5(7.571ps)(1+4.67) = 214.63ps$$

$$E_{chain} = C_{chain}V_{DD}^2 = (2.177pF)(2.5)^2 = 13.61\,pJ$$

$$E_{total} = (C_{chain} + C_L)V_{DD}^2 = (2.177+4)(2.5)^2 = 38.61\,pJ$$

Remove 2 buffers and try N=4

$$f_4 = \sqrt[4]{2222.22} = 6.87$$

$$t_{p0} = 4(7.571ps)(1+6.87) = 238.335ps$$

$$E_{chain} = C_{chain}V_{DD}^2 = (1.366pF)(2.5)^2 = 8.5375\,pJ$$

$$E_{total} = (C_{chain} + C_L)V_{DD}^2 = (1.366+4)(2.5)^2 = 33.5375\,pJ$$

N=3 cannot produce a delay within the constraint.

d. If γ is reduced due to a new technology, Figure 5-21 in the text shows that f_{opt} is reduced. When f_{opt} is reduced, we can use **more buffers**, since the intrinsic delay is reduced. The effect on energy is **unclear**, it depends on the numbers. More buffers leads to more capacitance as the $C_L/(f-1)$ equation predicts, but the $(1+\gamma)$ term in the capacitance calculation will be reduced. Many times this will actually lead to lower energy consumption.

EECS 312 HW7 P1 DRAM Pre-Charge Voltage vs. Refresh Time