Lab 2

Objectives:

1. To generate I_d vs. V_{ds} curves for both NMOS and PMOS devices simulated using level 53 SPICE model and compare to our default technology I-V characteristics.
2. To simulate a CMOS inverter to obtain its VTC and general delay properties and estimate certain parameters to compare with hand calculations.
3. To simulate and analyze a 7-stage ring oscillator.

1. Id vs. Vds curves for NMOS and PMOS

Schematic Capture of NMOS:

Create a schematic for NMOS transistor with an Input port, Output port and a voltage source connected to the output port. The schematic looks like the one in Figure 1. Make sure that you change the value of the *INSTPAR* property of the voltage source (right click → properties → modify multiple) from 5 to VDS. For the NMOS, set the following values in *INSTPAR* dialog box. **W=0.5U L=0.25U AS=0.3125P AD=0.3125P PS=1.75U PD=1.75U.**

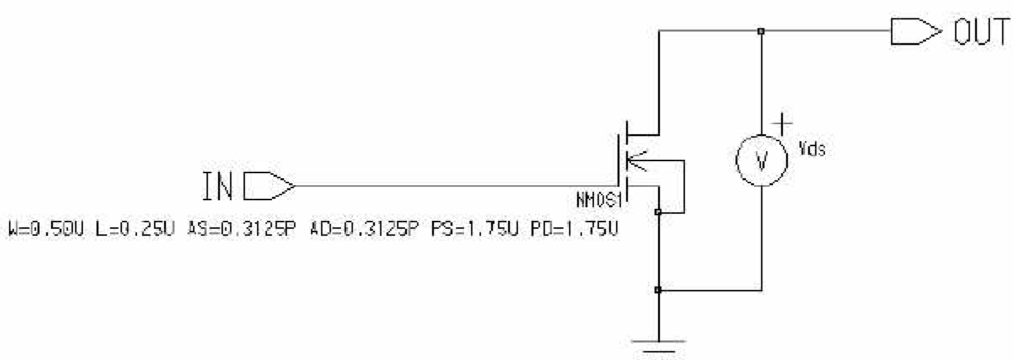

Figure 1. NMOS transistor schematic to obtain the Id-Vds curve.

Simulation

For simulation of NMOS, run a **DCOP simulation**. Set V_{GS} = 1V. Vary V_{ds} from 0 to 2.5V in steps of 0.1V. To do this, carry out the following steps:

(a) First set up a **DCOP** analysis in the **SETUP > ANALYSIS** menu by selecting **DCOP** and then pressing **OK**.

(b) Then add a **DC** force of 1V on **/IN** port through **ADD FORCE.**

(c) **ADD KEEPS** to **ALL**.

(d) Click LMB on the voltage source connected to the output port.

(e) Now select **Run > Sweep Runs > Property on Instance**. A window opens. You will see the /I$X in the "Instance name" where X is some positive number. Take note of this number as you'll need it later. Click LMB on the Select Property.

(f) Select **INSTPAR=VDS**.

(g) Click LMB on **Sweep** and **Linear**.

(h) Enter "0" in **From** field,"2.5" in the **To** field and 0.1 in **By** field.

(i) *For AC Analysis, plot* **Mag.**

(j) Click **OK**.

This runs the sweep analysis. You'll see the values of Vds being swept.

Note: If you want to overwrite the sweep results into only one collection (say, sweep1), then while you edit the window, enter the desired collection in the "Store results into collection named" field. While loading the waveform, make sure you load from the appropriate collection.

After the simulation has stopped, click the LMB on **Results>Chart>Family of Curves**. Click LMB on "Choose Collection". Click LMB on **Sweep**. By default, the latest sweep is the one with largest suffix. For example, if you have sweep, sweep1, and sweep2, then sweep2 is the latest analysis collection. You would want to select that. In the signal name window, type the instance number **/I$X/POS** (use the value of X which appeared in the "Instance name" above in this step) and type **//ground** in the reference name. If you now click the LMB on OK, you'll see the Id-Vds waveform for Vgs=1V.

Note: If you see the plot upside down, change /I$X/POS to /I$X/NEG.

Repeat the above steps for Vgs=0.5V, 1.5V, 2V, and 2.5V (meaning re-set the DC Force on the **/IN** port to each of these values). In order to put these individual charts together, you need to drag the legend to a common chart.

Repeat the procedure for a PMOS device at level 53 to obtain I_d vs. V_{ds} curve for PMOS with the same dimensions. The schematic of PMOS is shown in Figure 2.

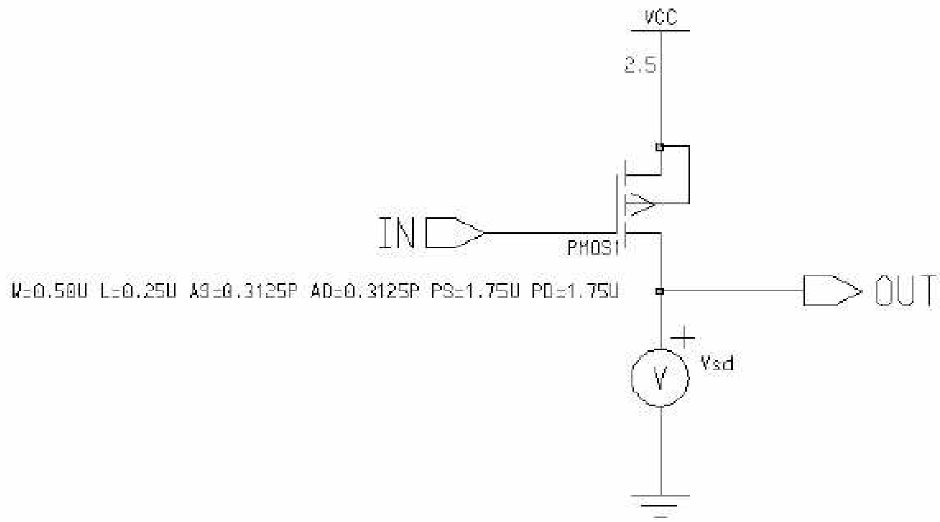

Figure 2. PMOS transistor schematic to obtain the Id-Vds curve.

Exercise #1:

(1) Output the I_d vs. V_{ds} curves for NMOS with V_{GS} = 0.5, 1, 1.5, 2, 2.5 V. <u>(They would resemble Figure 3-19 from your textbook)</u> **Label this as Figure 2-1 in your submission. Show the drain currents corresponding to $|V_{ds}|=|V_{gs}|=2.5V$ by placing a cursor.**

(2) Output the I_d vs. V_{ds} curves for PMOS with $|V_{GS}|$ = 0.5, 1, 1.5, 2, 2.5 V. <u>(They would resemble Figure 3-21 from your textbook)</u> **Label this as Figure 2-2 in your submission. Show the drain currents corresponding to $|V_{ds}|=|V_{gs}|=2.5V$ by placing a cursor.** *(Caution: The definition of V_{DS} is drain voltage – source voltage, don't be misguided by the potential of the voltage source attached at the output of PMOS. Similarly take care while labeling V_{GS}).*

(3) Calculate R_{eq} for V_{dd}= 2.5V based on simulation results for both PMOS and NMOS. Based on this data, which device do you think is more sensitive to V_{dd}, the PMOS or NMOS?

(4) Using our default technology hand calculate the drive currents for PMOS and NMOS at $|V_{ds}|=|V_{gs}|=2.5V$ based on the unified I-V model. Are your results close to the results from part (1)? If not, speculate as to why the results may be different.

(5) Calculate $R_{10\text{-}90}$ for both NMOS and PMOS with V_{dd} = 2.5V.

2. Voltage Transfer Characteristics (VTC)

Schematic Capture of CMOS:

To start simulating the CMOS inverter circuit, you need to first create the schematic in DA as usual. Make sure to change the **ASIM_MODEL** and **MODEL** names to **PMOS1** for the PMOS transistor and **NMOS1** for the NMOS transistor. Your schematic would look like figure 3. Once the schematic is complete, check, save, and finally create viewpoint as instructed in the previous lab.

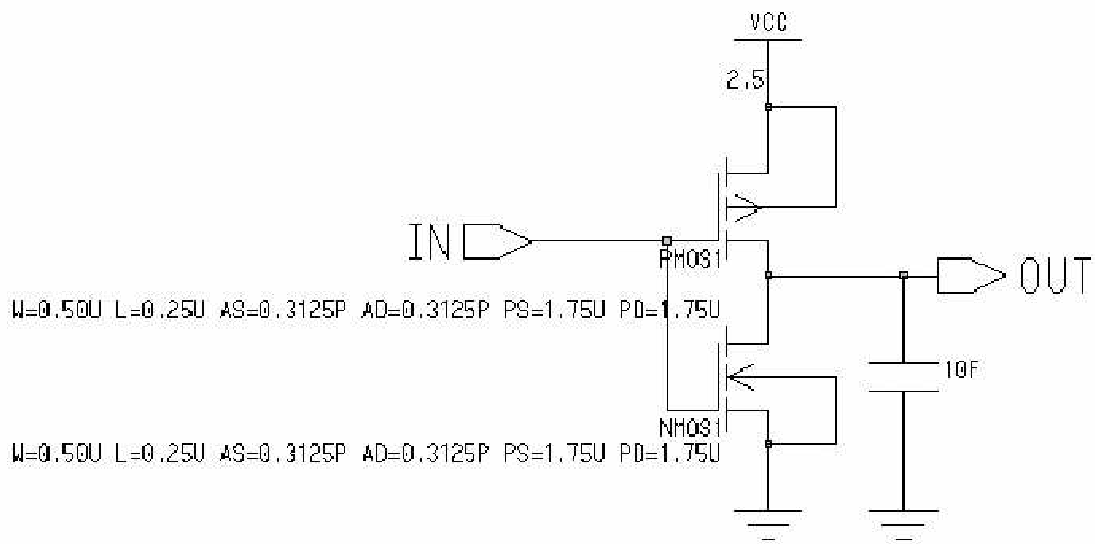

Figure 3. CMOS inverter

Simulation of the V_{out} versus V_{in} transfer function

After you have created the schematic and the viewpoint successfully, you can simulate your circuit in Accusim.

In order to simulate the static transfer characteristics, we perform a **DC SWEEP** analysis. Follow the steps below.
(a) In the schematic window, select **IN.**
(b) Click on the **DC MODE** button in the palette menu.
(c) Click on the **SETUP ANALYSIS** button in the palette menu. A dialog box will appear in the main window. Click on **DC Sweep** in the *Analysis* field. In the field of *Sweep Item*, select **Force Nets.** The *Source Type* is **Voltage**. Enter **/IN** and **//ground** for *Positive Net* and *Negative Net* separately. Enter **0**, **2.5,** and **0.01** respectively for **Start Value, Stop Value** and **Increment** fields. Click on **OK.** You can change the value in the field of increment to change the accuracy of your simulation. Smaller value corresponds to better accuracy, but slower simulation.
(d) Click on **RUN**.

(e) You will see a message that the server is running in the status window. Once that is done, click on OUT in the schematic window and click on **TRACE** in the palette menu to trace the voltage transfer characteristics of the inverter.

Gain Curve for Calculation of noise margin.

The most common definition for V_{IL} and V_{IH} is the input voltage when the slope is –1 in the transfer curve. To find these values, we need to plot gain first:
(a) Select **RESULT** in the palette menu of accusim window.
(b) Select **WF FUNCTION.** A window pops up. Select **Run Data**.
(c) Select **AvsB**. For both signals, select **Voltage** as the signal type.
(d) Now select **/OUT** as signal A and **/IN** as signal B. Do not change the "Measuring data from run:". By default it points to the latest run.
(e) Now in the **Waveform Functions**, select **Derivative.**
(f) Select **New** in the chart window.
(g) Click on **OK.**

Exercise #2:
(1) Output the Voltage Transfer Characteristic (V_{out} vs. V_{in}), label it as Figure 2-3.
(2) Output the plot of gain (gain vs. V_{in}) and label it as Figure 2-4.
(3) Find V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_H and NM_L from Figures 2-3 and 2-4. V_{IL} and V_{IH} should be obtained from the input voltages where gain is equal to –1.
(4) Find V_M from the simulated VTC.
(5) Use the extrapolation method to find V_{IL} and V_{IH} (described in class), and compare them with the values obtained in part (3).
Please label all the values you obtain from the plots by cursors.

3. CMOS Inverter Delay Analysis

The schematic used in this part is the same as that in Figure 3. We will sweep the load capacitance to figure out its impact on the following

- t_{fall} : fall time
- t_{rise} : rise time
- t_{pHL} : delay time for high to low transition
- t_{pLH} : delay time for low to high transition

Define the input waveform as follows :
Initial Value: 0 Pulsed Value: 2.5 Delay Time: 0 Rise Time: 0 Fall Time: 0 Pulse Width: 10N Period: 11N.

The **Time Step** and **Stop Time** are **0.1P** and **10N** respectively. Sweep load capacitance C_L from 0fF to 300fF in steps of 10fF. The simulation is similar to the sweeping process used for resistance in Lab #1. Put a voltage trace on the output port. Rise time is obtained by the following steps after you have run the simulation.

(a) Click on **Results->Chart…->Parametric Plot** on the menu on the top. A window will pop up.
(b) For X-axis, make sure it corresponds to the capacitance. For Y axis, in the field of *signal*, type **/OUT**. Type **//ground** in the field of *reference*. Then select **Fall time** in the *function* window**.**
(c) Click **Setup Function Options** below *function*. In the window popped out, set *Proximal Value* as **0.25**, *Distal Value* as **2.25**, *Proximal/Distal Type* as **Actual** and *Number of Histogram Bins* as **30000**. Then click on **OK**.
(d) Click **NEW** for *Chart Window* after you set up the parameters. Choose a title for the curve.
A plot of the output voltage rise time vs. load capacitance is obtained. For the delay time t_{pHL} , follow step (a) and (b), but select **Crosspoint** in *function*. Then, replace step (c) by the following operation:
Click **Setup Function Options** below *function*. In the window popped out, set *Crosspoint Mesial Value* as **1.25**, *Crosspoint Mesial Usage* as **Actual** and *Number of Histogram Bins* as **30000**. Then click on **OK**.
(d) Click **NEW** for *Chart Window* after you set up the parameters. Choose a title for the curve.

t_{rise} and t_{pLH} are found using another input pulse, which is different from the last pulse only in the following parameters: **Initial Value=2.5** and **Pulsed Value=0.** This simply changes the input from a low-to-high step to a high-to-low step. The procedure to obtain curves for t_{rise} and t_{pLH} are the same as described for t_{fall} and t_{pHL}.

Exercise #3:
(1) Create plots for t_{rise}, t_{fall}, t_{pHL} and t_{pLH} as functions of C_L individually. Label them as Figures 2-5, 2-6, 2-7, and 2-8.
(2) Using the R_{eq} and R_{10-90} values extracted in Exercise 1 (for V_{dd}=2.5V), generate plots of t_{plh}, t_{phl}, t_{rise}, and t_{fall} using the RC approach described in class. These are Figures 2-9, 2-10, 2-11, and 2-12. You can do this in Excel or a similar program.
(3) Compare the simulation results with the simplified RC model – how accurate is the model typically for the various cases (e.g. 5%, 10%, 20% error, more accurate for 50% delay than rise/fall time or vice versa, more accurate for PMOS or NMOS?)?
(4) Examine the simulated delay at C_L = 0. According to the RC model, the delay for this case should be zero. Why is it not?

4. Ring Oscillator

In order to obtain the delay time of the CMOS inverter, we designed a 7-stage ring oscillator as shown in Figure 4.

After you draw an inverter, you can make 6 copies of it and **Add Wire** to connect them. Next, the Ground and the OUT ports are connected. Finally, the first inverter's power supply should be replaced with a voltage source. This is done to allow for a transient analysis.

The properties of the individual CMOS inverters are the same as those of the CMOS inverter introduced previously in this lab (i.e. W_p=W_n=0.5µm, L=0.25µm, AD, AS, PD, PS parameters are the same). They are not shown in Figure 4 for clarity. (in the modify properties menu, the INSTPAR property can be selected to be *hidden* instead of *visible* if desired).

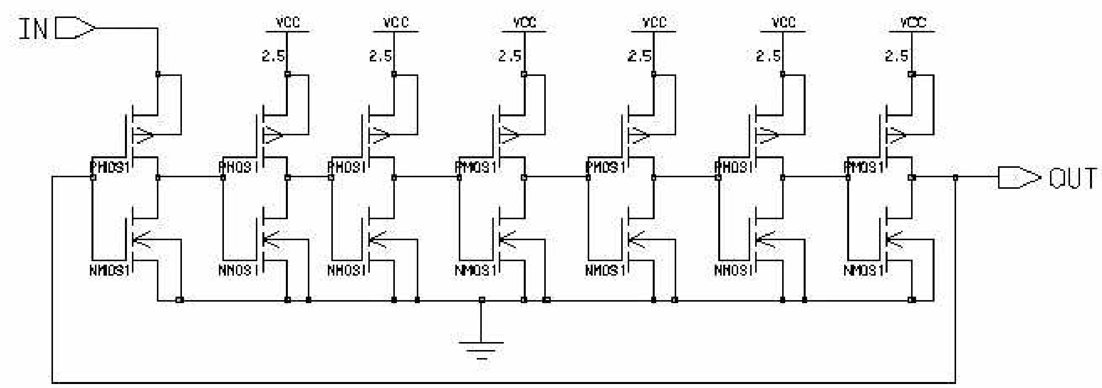

Figure 4. 7-stage ring oscillator schematic

Set up a **Transient Analysis** with 0.1P step time and 3N run time. In the setup analysis step, check the box called "Use initial conditions." Click on the setup box and use "selected" nets. You should have the /OUT net selected before doing this step. Set the initial condition to 0V and leave the right side choice to "guess." Use **Add Force** to set the voltage of /IN as 2.5V. Put traces on two consecutive output nodes (for example, /OUT and the input to the last inverter in Figure 4). Measure the period of /OUT using cursors. Then equate the time period as

$$T=2t_pN \qquad (N=7)$$

The delay of this design is to be obtained from the above equation.

Exercise #4:

(1) Output the traces of /OUT and an adjacent inverter output as Figure 2-13.

(2) Find t_p and t_{pHL} and t_{pLH} using cursors in the same plot. Verify their relationship as described in lecture.

(3) Now verify that ring oscillator frequency does not depend on device sizes. To do this, change W_n=W_p=2.5μm. We must also update the junction capacitance geometry parameters (AD,AS,PD,PS). These are calculated based on Equation 3.45 in the textbook. Note that the length of the source and drain regions (L_s in textbook Figure 3-33) is unchanged when the device width is increased. Re-simulate with the larger device sizes and compare the period T to that found with W_n=W_p=0.5μm. If there are discrepancies, can you think of possible reasons?

(4) Include a trace of /OUT for W_n=W_p=2.5μm showing the period measured using cursors (Figure 2-14). You do not need to measure t_{pHL} and t_{pLH} in this case.