312: Final Exam

INSTRUCTIONS

Read all of the instructions and all of the questions before beginning the exam.

The credit for each problem is given to help you allocate your time accordingly. You have a total of 120 minutes to finish this exam. Do not spend all of your time on one problem.

This is an open-book, open-notes exam.

Please place a circle or box around your answers (quantitative ones).

I have underlined the portion of each question that specifically lists what you need to provide in your answer.

Unless otherwise noted on a particular problem, you must show your work (in the space provided plus the back of the pages) for all problems to receive full credit; simply providing answers will result in only partial credit, even if the answers are correct. If you require extra space beyond what is provided, be sure to turn in any material that is required to support your solutions. Note that there is extra work space at the end of this exam booklet.

Turn in the entire exam, including this cover sheet.

Be sure to provide units where necessary.

Use the default technology unless otherwise specified.

1. Dynamic logic has its major advantage over static CMOS in one of our key performance metrics. Name the metric and give three reasons for the superiority of dynamic logic in this area. [5 points]

2. a) Express node OUT in terms of the gate inputs (A,B,C,D,E,F,G) in Figure 2.1? [4 points]

b) Draw the corresponding pull-down network for Figure 2.1, minimizing transistor count and minimizing the number of devices connected to node OUT. [4 points]

c) This complex gate must be sized to match the worst-case output resistance of the inverter below (INV1 in Figure 2.2). INV1 has a design constraint that the power supply noise must be less than 1% of V_{dd} while t_{plh} is minimized. Let $\beta = 2$ in INV1 and only consider power supply noise on V_{dd}. The inductance associated with the power network is 1 nH. C_{Load} in Figure 2.2 represents all relevant capacitances – do not calculate any capacitances in this problem.

i. Find the sizes (W_n and W_p) of INV1. [7 points]
ii. Size all devices in the complex gate of Figure 2.1 to match the worst-case output resistance of INV1 with the above sizes. [5 points]

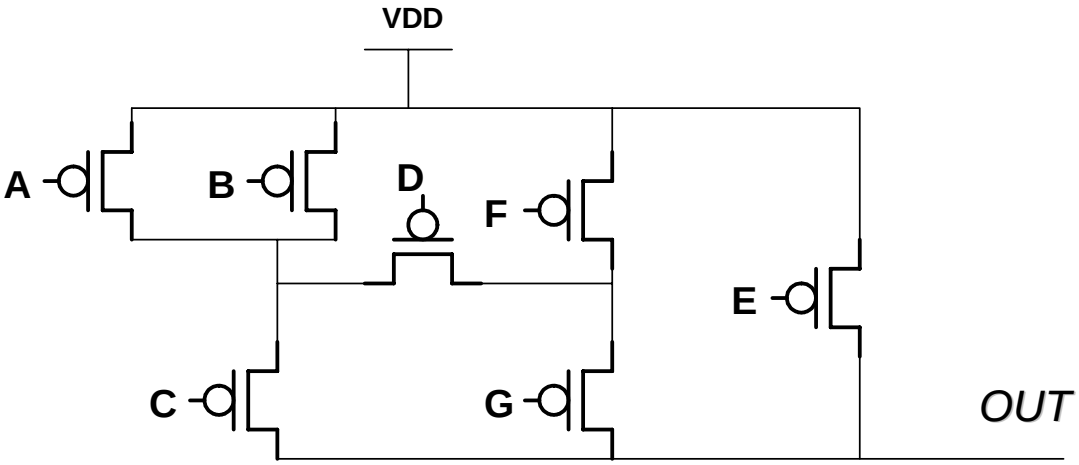


Figure 2.1

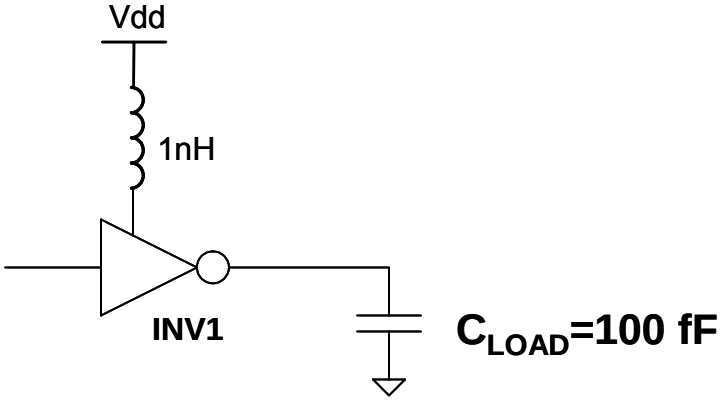


Figure 2.2

Work space, problem 2

3. Consider an inverter in our 0.25μm CMOS technology with W_p=4μm, W_n=1μm and minimum channel length for both devices. Apply constant-field (full) scaling with S = 5; this represents a technology that will be available in roughly the year 2010. Find the ***exact*** V_{OL} of this scaled inverter when $V_{in} = V_{dd}$ (it is not exactly 0V). Assume that S_s is constant at 90mV/dec with scaling. Ignore channel-length modulation. [8 points]

4. Consider a wire with the following dimensions: L = 8mm, W = 1μm, H_{wire} = 1μm, ρ = 2.7 $\mu\Omega$-cm, and $\varepsilon_{di}=4\varepsilon_0$. Let γ=1 and use the default technology parameters for this problem. Ignore overlap capacitances.

   a. Calculate the total wire resistance and capacitance (use rule of thumb for capacitance). [3 points]

   b. Use the repeater insertion methodology to calculate the optimal number of repeaters to insert on this wire. Then, calculate the delay of the repeater chain assuming that the fanout at the end of the wire is a repeater of optimal size (that you calculated). For this part, also assume there is a step input into the first repeater. [9 points]

   c. Create a tapered buffer chain starting from a $W_p=2W_n=1\mu$m inverter to drive the initial repeater from part (b). Calculate the delay of the tapered buffer chain (i.e., up to the input of the initial repeater). What is the total delay to drive this wire including both the repeater and tapered buffer structures? [8 points]

5. a) Given the gate in Figure 5.1 below, provide the function OUT. [3 points]
   b) What is the purpose of the PMOS transistor, M_3? [2 points]
   c) Is this a static or dynamic circuit? [1 point]
   d) Is it a ratioed or non-ratioed circuit? [2 points]

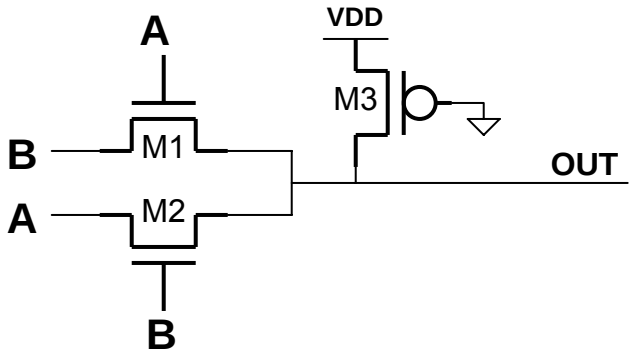


Figure 5.1

6. Consider a metal 5 wire running over metal 4 with sheet resistance of 0.1 $\Omega/\square$ and wire width of 0.6μm. Let the driver be an inverter with W_n = 5μm and β = 3.

   a) Give a rough estimate of how long the wire must be before its resistance should be considered in computing total gate delay. HINT: This should not require a t_p calculation. [5 points]

   b) How does an increase in wire width change your answer above? (respond qualitatively, indicating a $\uparrow$ or $\downarrow$ in your answer to (a) with brief explanation). [2 points]

   c) How does a change in V_{dd} alter your answer above? (respond qualitatively again). [3 points]

7. Three different designers (D1, D2, D3) implemented the same logic function with different circuit topologies as shown in Figure 7.1 (A, B, C, D are the inputs and Z is the output). They used cells from a standard library for which the area and delay numbers are provided (refer to Table 7.1). *(W_{total} is a measure of the total area of these devices).*

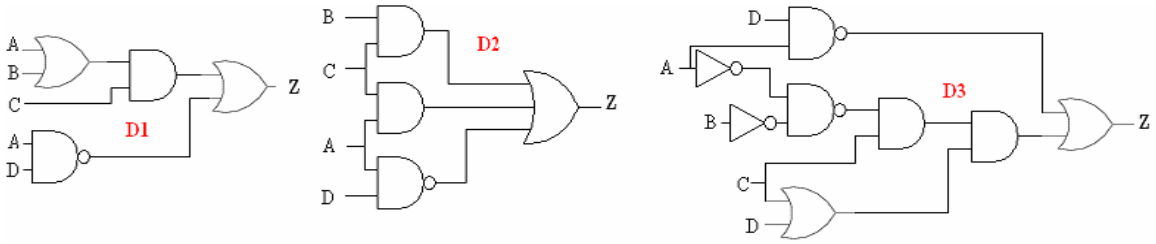


Figure 7.1

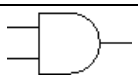
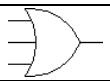
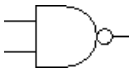
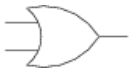
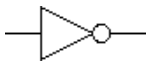
Logic Gate	W_{total} (µm)	Delay (units)	Logic Gate	W_{total} (µm)	Delay (units)
	11	3		21	5
	8	2		10	3
	3	1			

Table 7.1: Cell Library

Your job is to evaluate these circuit topologies based on delay and energy metrics. For all the following parts in this question, support your answer with numbers from the library.

(a) Which one of these designs is the fastest? [4 points]
(b) Which one of these designs is likely to have the lowest energy (ignore possible internal node switching activity differences among the designs)? Explain briefly. [4 points]
(c) Which one is least susceptible to hold time violations? Explain briefly. [3 points]

8. Figure 8.1 shows an array (128 X 64) of 6T SRAM cells (4μm x 3μm). The word line is being driven by an inverter (W_p = 10μm, W_n = 4μm) with a step input. The bit line capacitances are C_{BL} = 100fF each. Assume that a successful read operation requires that the bit line voltage (initially precharged to V_{dd} = 2.5 V) changes by ΔV = 250 mV. The sense amplifiers have an input to output delay of 25 ps. All transistors in the SRAM cell have minimum channel length and W = 0.5 μm.

For device capacitance calculations, consider gate capacitance (C_{GC}) only. Ignore all overlap and junction capacitances. The word line has sheet resistance of $R_{\square}$ = 0.5 Ω/□ and a width of 0.3μm. Use the rule of thumb from class to calculate wire capacitance. Ignore the resistance of the bitline. You can use our pre-defined equivalent resistance definition (i.e., you do not need to recompute an R_{eq} for the differing voltage swing of interest in this case).

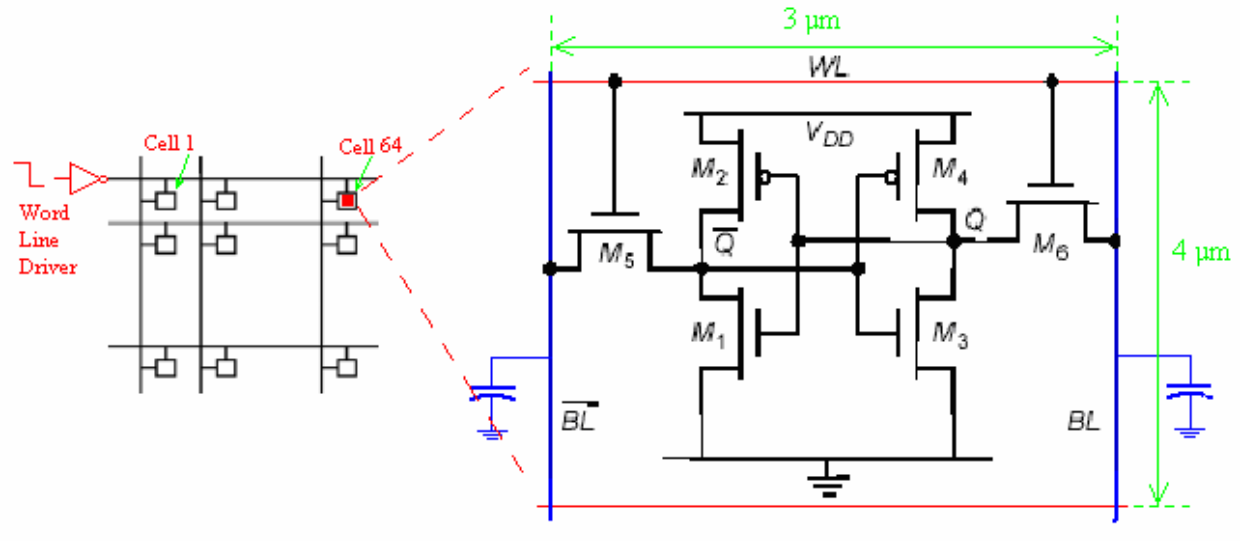


Figure 8.1

(a) Assuming that the last cell of a row (cell 64) stores a '0' value at Q, calculate the READ ACCESS time for this cell. READ ACCESS time is defined as the delay from the word line driver's input transition to the output of the sense amplifiers. [13 points]

(b) Estimate the difference in read time between the first (cell 1) and last cell (cell 64) (both store a '0' at Q). NOTE: This part of the question should not require much calculation effort (and definitely not a re-calculation of part (a) for cell 1). [5 points]