EECS 312: Digital Integrated Circuits
Homework #7

Reading: 5.4.3 (Buffer Design), 12.2.3 (DRAM)

1. **DRAM**: A 1T DRAM cell is represented by the following circuit diagram (Figure 1). The bit line is pre-charged to $V_{DD}/2$ using a pre-charge circuit when a read is expected. Also the WRITE circuit is used to bring the potential of the bit line to V_{DD} or 0V during the WRITE operation with the word line at V_{DD}. Use our default technology.

   a. A WRITE-1 operation (both the bit line and word line are driven to 2.5V) is performed, followed by a READ-1 operation (in this case, the bit line is pre-charged to $V_{dd}/2$). Assuming zero leakage current in the circuit, find the resulting voltage at the bit line after the READ-1 operation.
   b. Find the upper and lower voltage bounds for the pre-charge voltage on the bit-line such that both READ-1 and READ-0 operations work properly with a sense amplifier that required 50 mV of voltage change. In a realistic system with leakage current, why is it a bad idea to pre-charge the bit-line to either of the voltage boundaries?
   c. Solve for the bit-line pre-charge voltage ($V_{bitline}$) that will produce the greatest worst-case voltage swing on the bit-line during a READ operation. Assume no leakage current.
   d. Plot the required refresh time of the cell for storage of a 1 and storage of a 0 for the voltage range found in (b). Assume W=L=0.25um and S_S=90mV. Calculate leakage currents at the midpoint of the voltage swing of interest (this is an aggressive assumption). Using the plot, what pre-charge voltage leads to the least power consumption for the array?
   e. Suppose we let the word line swing from -0.5V to 3V. How does this help the performance? Answer qualitatively and refer to how both the voltage levels help. Also provide one drawback to doing this.
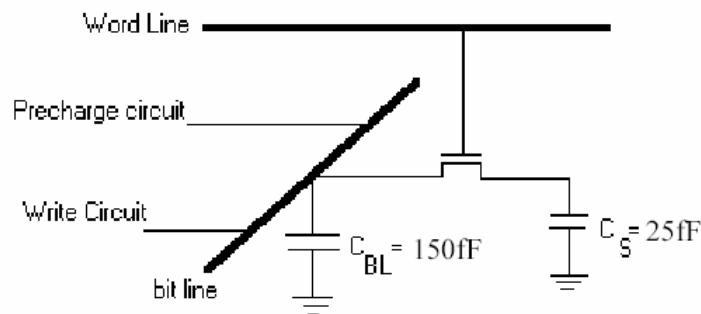

Figure 1

2. **Buffer Design:** Suppose we must design a buffer chain to drive an 4pF load capacitance. The input to our chain is an inverter with the sizes W_P=1um and W_N=0.5um. Assume that γ = 1. Calculate input capacitances using C_{gc} only (ignore overlap).
   a. Calculate the optimal delay and number of buffer inverters using our default technology parameters.
   b. Calculate the energy consumption of the optimal buffer chain (one high and one low transition):
      i. Buffer Chain only.
      ii. Buffer Chain including the output capacitance of 4pF.

c. Assume that we are allowed a 50% delay penalty when designing the chain. The goal is to reduce the energy consumption of the circuit, and we are allowed to either reduce the supply voltage of the existing design or resize the chain and/or size of inverters in the chain. Quantitatively analyze each option and calculate (for each):

   i. Energy consumption of the buffer chain including the output capacitance.
   ii. Energy consumption of the buffer chain only.

   Which technique is better considering only the buffer chain? Which technique is better considering the buffer chain and the fixed output capacitance?

d. In SOI transistors, γ is much less than 1 due to reduced junction capacitances. Qualitatively describe the impact on buffer chain design. Would you have more or less buffers for a given capacitance? Would this affect energy? If so, how?