EECS 312: Digital Integrated Circuits
Homework #1 Solutions

1. IC Cost and Economics:

a) The general process for part A, is to calculate the dies/wafer, then the yield, cost of die, variable cost, followed by the cost per IC for both designs on both fabrication facilities. The **ASIC design should be fabricated in the 4 inch facility** and the **Microprocessor (uproc) should be fabricated in the 8 inch facility**.

$$\frac{Dies}{Wafer}_{(general\ eq.)} = \frac{\pi\left(\frac{Wafer\ Size}{2}\right)^2}{Die\ Area} - \frac{\pi(Wafer\ Size)}{\sqrt{2(Die\ Area)}}$$

$$\frac{Dies}{Wafer}_{(4inch,uproc)} = \frac{\pi\left(\frac{(10.16\,cm)}{2}\right)^2}{3.2\ cm^2} - \frac{\pi(10.16\ cm)}{\sqrt{2(3.2\ cm^2)}}$$

$$\frac{Dies}{Wafer}_{(4inch,uproc)} = 12$$

$$\frac{Dies}{Wafer}_{(4inch,ASIC)} = 279$$

$$\frac{Dies}{Wafer}_{(8inch,uproc)} = 76$$

$$\frac{Dies}{Wafer}_{(8inch,ASIC)} = 1206$$

$$Yield_{(general\ eq.)} = \left(1 + \frac{Die\ Area \times Defect\ Density}{\alpha}\right)^{-\alpha}$$

$$Yield_{(4inch,uproc)} = \left(1 + \frac{(3.2\ cm^2) \times 0.5\ cm^{-2}}{3}\right)^{-3}$$

$$Yield_{(4inch,uproc)} = 0.2773$$

$$Yield_{(4inch,ASIC)} = 0.8847$$

$$Yield_{(8inch,uproc)} = 0.2453$$

$$Yield_{(8inch,ASIC)} = 0.8721$$

$$Cost\ of\ Die_{(general\ eq.)} = \frac{Cost\ of\ Wafer}{Yield \times \frac{Dies}{Wafer}}$$

$$Cost\ of\ Die_{(4inch,uproc)} = \frac{\$150.00}{0.2773 \times 12}$$

$$Cost\ of\ Die_{(4inch,uproc)} = \$45.06$$

$$Cost\ of\ Die_{(4inch,ASIC)} = \$0.61$$

$$Cost\ of\ Die_{(8inch,uproc)} = \frac{\$800.00}{0.2453 \times 76}$$

$$Cost\ of\ Die_{(8inch,uproc)} = \$42.90$$

$$Cost\ of\ Die_{(8inch,ASIC)} = \$0.76$$

$$Variable\ Cost_{(general)} = \frac{Die + Packaging + Testing}{Functional\ Test\ Yield}$$

$$Variable\ Cost_{(4inch,uproc)} = \frac{45.06 + 25.00 + 2.78}{0.95}$$

$$Variable\ Cost_{(4inch,uproc)} = \$76.68$$

$$Variable\ Cost_{(4inch,ASIC)} = \$2.07$$

$$Variable\ Cost_{(8inch,uproc)} = \frac{42.90 + 25.00 + 2.78}{0.95}$$

$$Variable\ Cost_{(8inch,uproc)} = \$74.40$$

$$Variable\ Cost_{(8inch,ASIC)} = \$2.23$$

$$Cost\ \ per\ \ IC_{(general)} = Variable\ Cost\ of\ IC + \left(\frac{Fixed\ \ NRE\ \ Cost}{Volume}\right)$$

$$Cost\ \ per\ \ IC_{(4inch,uproc)} = \$76.68 + \left(\frac{\$200,000,000}{50,000,000}\right) = \$80.68$$

$$Cost\ \ per\ \ IC_{(4inch,ASIC)} = \$2.07 + \left(\frac{\$2,000,000}{1,000,000}\right) = \$4.07$$

$$Cost\ \ per\ \ IC_{(8inch,uproc)} = \$74.40 + \left(\frac{\$200,000,000}{50,000,000}\right) = \$78.40$$

$$Cost\ \ per\ \ IC_{(4inch,uproc)} = \$2.23 + \left(\frac{\$2,000,000}{1,000,000}\right) = \$4.23$$

b) In part b, a new 12 inch facility is proposed, and the microprocessor design is being considered for the new facility. We must solve for a constraint on the defect density of the new fab such that the 12 inch fab would result in cost savings over the previous fabrication selection in part A (8 inch fab). The first thing we know is that the best cost per IC from the 8 inch fab is \$78.40.

$$Cost\ \ per\ \ IC_{(uproc)} \geq Variable\ Cost + \left(\frac{Fixed\ Cost}{Volume}\right)$$

$$\$78.40 \geq Variable\ Cost + \left(\frac{(\$1,000,000,000 + \$200,000,000)}{50,000,000}\right)$$

$$Variable\ Cost \leq \$54.40$$

$$\$54.40 \geq \frac{Die\ Cost + \$25.00 + \$2.78}{0.95}$$

$$Cost\ \ per\ Die \leq \$23.90$$

$$\$23.90 \geq \frac{Wafer\ Cost}{Yield \times \frac{Dies}{Wafer}} = \frac{\$1500}{Yield \times 190}$$

$$Yield \geq 0.3303$$

$$0.3303 \leq \left(1 + \frac{(3.2\ cm^2) \times (Defect\ Density)}{3}\right)^{-3}$$

$$Defect\ Density \leq 0.4187\ cm^{-2}$$

2. Capacitance Calculations:

a) First, calculate the area and perimeter of the drain regions.

$$AD(area\ of\ drain)_{NMOS} = (L_{drawn} * 2.5) * (W_n)$$
$$= (0.25um)(2.5) * (4um) = 2.5\ um^2$$
$$PD(perimeter)_{NMOS} = (2 * 2.5L_{drawn}) + W_n$$
$$= (2 * 0.625um) + 4um = 5.25um$$
$$AD(area\ of\ drain)_{PMOS} = (0.25um)(2.5) * (6um) = 3.75\ um^2$$
$$PD(perimeter)_{PMOS} = (2 * 0.625um) + 6um = 7.25um$$

For C_{db} calculations, consider a 0 → VDD and VDD → 0 transition on the drain. Since we care about 50% delay, this translates to 0 → VDD/2 and VDD → VDD/2 transitions on the drain.

For 0 → VDD/2 Transition:

NMOS

Bulk is held to ground, so at V_{drain} = 0, we have the zero-bias case. As V_{drain} increases the depletion region grows and C_j decreases.

Calculate K_{eq} for this transition:

V_{high} = -1V and V_{low} = 0V (negative due to reverse bias).

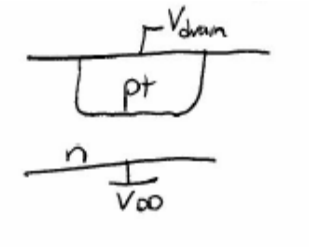
$$K_{eq}(NMOS,lh) = \frac{-(0.9)^{0.5}}{((-1)-0)(1-0.5)}\left[((0.9)-(-1))^{0.5} - ((0.9)-0)^{0.5}\right] = 0.815$$

$$K_{eqsw}(NMOS,lh) = \frac{-(0.9)^{0.44}}{((-1)-0)(1-0.44)}\left[((0.9)-(-1))^{0.56} - ((0.9)-0)^{0.56}\right] = 0.835$$

PMOS

Bulk is held to Vdd, so when V_{drain}=0, we actually have a large reverse bias across the bulk-drain junction.

V_{high}= -2V and V_{low}= -1V since the bias across the junction changes from -2V to -1V as the drain transitions from 0 to VDD/2.



$$K_{eq}(PMOS,lh) = \frac{-(0.9)^{0.48}}{((-2)-(-1))(1-0.48)}\left[((0.9)-(-2))^{0.52} - ((0.9)-(-1))^{0.52}\right] = 0.627$$

$$K_{eqsw}(PMOS,lh) = \frac{-(0.9)^{0.32}}{((-2)-(-1))(1-0.32)}\left[((0.9)-(-2))^{0.68} - ((0.9)-(-1))^{0.68}\right] = 0.733$$

$$\begin{aligned} C_{db}(NMOS,lh) &= AD_{NMOS} * C_j * K_{eq} + PD_{NMOS} * C_{jsw} * K_{eqsw} \\ &= (2.5\ um^2)(2\times10^{-3}\ F/m^2)(0.815) + (5.25\ um)(2.8\times10^{-10}\ F/m)(0.835) \\ &= 5.30245\ fF \end{aligned}$$

$$\begin{aligned} C_{db}(PMOS,lh) &= AD_{PMOS} * C_j * K_{eq} + PD_{PMOS} * C_{jsw} * K_{eqsw} \\ &= (3.75\ um^2)(1.9\times10^{-3}\ F/m^2)(0.627) + (7.25\ um)(2.2\times10^{-10}\ F/m)(0.733) \\ &= 5.63651\ fF \end{aligned}$$

For VDD → VDD/2 Transition:

NMOS

Calculate K_{eq} for this transition:

V_{high} = -2V and V_{low} = -1V (negative due to reverse bias).

$$K_{eq}(NMOS,hl) = \frac{-(0.9)^{0.5}}{((-2)-(-1))(1-0.5)}\left[((0.9)-(-2))^{0.5} - ((0.9)-(-1))^{0.5}\right] = 0.616$$

$$K_{eqsw}(NMOS,hl) = \frac{-(0.9)^{0.44}}{((-2)-(-1))(1-0.44)}\left[((0.9)-(-2))^{0.56} - ((0.9)-(-1))^{0.56}\right] = 0.653$$

Note that these values are 25-30% smaller than those for the 0 → VDD transition. This is because in the VDD → 0 transition the NMOS drain-bulk junction has a larger reverse bias on it leading to a smaller average capacitance (this is only true since we restrict our attention to the first half of the transition).

PMOS

V_{high}= -1V and V_{low}= 0V

$$K_{eq}(PMOS,hl) = \frac{-(0.9)^{0.48}}{((-1)-(0))(1-0.48)}\left[((0.9)-(-1))^{0.52} - ((0.9)-(0))^{0.52}\right] = 0.822$$

$$K_{eqsw}(PMOS,hl) = \frac{-(0.9)^{0.32}}{((-1)-(0))(1-0.32)}\left[((0.9)-(-1))^{0.68} - ((0.9)-(0))^{0.68}\right] = 0.876$$

The K_{eq} values are larger than in the 0 → VDD/2 transition, since the reverse bias over the junction is less in this case.

$$\begin{aligned} C_{db}(NMOS,hl) &= AD_{NMOS} * C_j * K_{eq} + PD_{NMOS} * C_{jsw} * K_{eqsw} \\ &= (2.5\ um^2)(2\times10^{-3}\ F/m^2)(0.616) + (5.25\ um)(2.8\times10^{-10}\ F/m)(0.653) \\ &= 4.03991\ fF \end{aligned}$$

$$\begin{aligned} C_{db}(PMOS,hl) &= AD_{PMOS} * C_j * K_{eq} + PD_{PMOS} * C_{jsw} * K_{eqsw} \\ &= (3.75\ um^2)(1.9\times10^{-3}\ F/m^2)(0.822) + (7.25\ um)(2.2\times10^{-10}\ F/m)(0.876) \\ &= 7.25397\ fF \end{aligned}$$

Gate-Channel Capacitance (C_{GC}):

$$\begin{aligned} C_{gc}(NMOS) &= C_{ox}WL_{eff} \\ &= \left(\frac{\varepsilon_{ox}}{t_{ox}}\right)W_n(0.8 * L_{drawn}) = \left(\frac{3.9\varepsilon_o}{(5.75E-7\ cm)}\right)(4E-4\ cm)(0.2E-4\ cm) \\ &= 4.804\ fF \end{aligned}$$

$$\begin{aligned} C_{gc}(PMOS) &= \left(\frac{\varepsilon_{ox}}{t_{ox}}\right)W_p(0.8 * L_{drawn}) = \left(\frac{3.9\varepsilon_o}{(5.75E-7\ cm)}\right)(6E-4\ cm)(0.2E-4\ cm) \\ &= 7.206\ fF \end{aligned}$$

Gate-Drain Overlap Capacitance (C_{GD}):

The intended way to calculate this was to use the SPICE Model parameter C_{GD0} to calculate the overlap capacitance in a simple manner. If you used C_{ox} method of calculating the overlap capacitance you may have obtained different figures (you will still receive credit). The SPICE model was modified from a previous technology generation to reflect our default technology and is not valid for every calculation.

$$C_{gd}(NMOS) = C_{gd0}W_n$$
$$= (3.1\times10^{-10}\ F/m)(4um) = 1.24\ fF$$
$$C_{gd}(PMOS) = C_{gd0}W_p$$
$$= (2.7\times10^{-10}\ F/m)(6um) = 1.62\ fF$$

b) Layout Issues: The idea behind the two layout diagrams is to illustrate the manner of calculating the area and perimeter of the transistor in our equations for capacitance. In the conventional layout, we use the equations from the solution above. For the folded layout, one can see that the drain region (the center strip in the diagram) has a significantly reduced area. So we can begin by recalculating the areas and perimeters for the C_{db} calculation.

$$AD(area\ of\ drain)_{NMOS} = (L_{drawn} * 2.5) * \left(\frac{W_n}{2}\right)$$
$$= (0.25um)(2.5) * (2um) = 1.25\ um^2$$
$$PD(perimeter)_{NMOS} = (2 * 2.5L_{drawn})$$
$$= (2 * 0.625um) = 1.25um$$

According to our methods, the area is reduced in half, as the width of each device in this "parallel configuration" is half of the previous width. The perimeter is greatly reduced, since both "Width" edges are conducting regions (not counted).

$$C_{db}(NMOS, hl) = AD_{NMOS} * C_j * K_{eq} + PD_{NMOS} * C_{jsw} * K_{eqsw}$$
$$= (1.25\ um^2)(2\times10^{-3}\ F/m^2)(0.616) + (1.25\ um)(2.8\times10^{-10}\ F/m)(0.653)$$
$$= 1.76855\ fF$$
$$C_{gc}(NMOS) = C_{ox}W_2L_{eff} + C_{ox}W_2L_{eff}$$
$$= \left(\frac{\varepsilon_{ox}}{t_{ox}}\right)2W_2(0.8 * L_{drawn}) = \left(\frac{3.9\varepsilon_o}{(5.75E-7\ cm)}\right)2(2E-4\ cm)(0.2E-4\ cm)$$
$$= 4.804\ fF$$
$$C_{gd}(NMOS) = C_{gd0}W_2 + C_{gd0}W_2$$
$$= (3.1\times10^{-10}\ F/m)2(2um) = 1.24\ fF$$

The folded layout results in a 56% reduction in the C_{db} capacitance, but the other capacitances remain the same (since there is still 4um worth of gate width). In reality, the width of the drain is slightly greater in the folded layout (greater that 2.5 L_{drawn}), but the folded layout usually results in a significant savings in C_{db} capacitance.

The folded layout will lead to a slightly faster circuit (delay and rise times) and slightly less power consumption. The folded layout also appears to be more compact and manageable (as it is in many process technologies), but this is ultimately up to the design rules of a particular technology – not a blanket statement.

3. RC Network Review:

a) First one must determine the time for a clock cycle, realize that the final voltage is 0 and 95% of the final voltage is (2.5-0)*0.05 =0.125V.

$$t_{period} = \frac{1}{1.2GHz} = 833.33\ ps$$

$$V_{final} = V_{initial} e^{-t/RC}$$

$$0.05 = e^{-t_{period}/R(3*24.4\ fF)}$$

$$\ln(0.05) = \frac{-t_{period}}{R_{eq}(73.2\,fF)}$$

$$-2.9957 = \frac{-833.33\ ps}{R_{eq}(73.2\,fF)}$$

$$R_{eq} = 3800\ \Omega$$

b) If the capacitance is increased to 3(28.3 fF) = 84.9 fF, we must calculate the time required to reach the 0.125V voltage point. The calculation below shows that the circuit will still operate within a clock cycle at 1GHz.

$$t_{period} = \frac{1}{1.2GHz} = 833.33\ ps$$

$$V_{final} = V_{initial} e^{-t/RC}$$

$$0.125V = 2.5e^{-t/RC}$$

$$\ln(0.05) = \frac{-t_{period}}{(3800\Omega)(84.9\,fF)}$$

$$t_{period} = 966.48\ ps$$

$$t_{period} < \frac{1}{1GHz} = 1000\ ps$$

4. Unified I-V Model:

a) This is a PMOS device.

b) Using measurements 1 & 4, V_{T0} = -0.5 V.

$$\frac{I_{D1}}{I_{D4}} = \frac{k\frac{W}{L}\left(V_{GT1}V_{\min 1} - \frac{V_{\min 1}{}^2}{2}\right)(1+\lambda V_{DS1})}{k\frac{W}{L}\left(V_{GT4}V_{\min 4} - \frac{V_{\min 4}{}^2}{2}\right)(1+\lambda V_{DS4})}$$

$$1.5 = \frac{\left((-2.5-V_{T0})(-1) - \frac{(-1)^2}{2}\right)(1+\lambda 2.5)}{\left((-2.0-V_{T0})(-1) - \frac{(-1)^2}{2}\right)(1+\lambda 2.5)}$$

$$2.25 + 1.5V_{T0} = 2 + V_{T0}$$

$$V_{T0} = -0.5V$$

c) Using measurements 1 & 5, γ = -0.44897 $V^{1/2}$

$$\frac{I_{D1}}{I_{D5}} = \frac{k\frac{W}{L}\left(V_{GT1}V_{\min 1} - \frac{V_{\min 1}{}^2}{2}\right)(1+\lambda V_{DS1})}{k\frac{W}{L}\left(V_{GT5}V_{\min 5} - \frac{V_{\min 5}{}^2}{2}\right)(1+\lambda V_{DS5})}$$

$$1.171875 = \frac{\left(\left(-2.5-\left(-0.5\right)\right)\left(-1\right)-\frac{\left(-1\right)^2}{2}\right)\left(1+\lambda 2.5\right)}{\left(\left(-2.5-\left(-0.5+\gamma\left(.4903\right)\right)\right)\left(-1\right)-\frac{\left(-1\right)^2}{2}\right)\left(1+\lambda 2.5\right)}$$

$$1.171875\left(\left(2.0-0.49\gamma\right)-0.5\right)=1.5$$

$$\gamma = -0.44897\ V^{1/2}$$

d) Using measurements 1 & 6, λ = -0.05 V^{-1}

$$\frac{I_{D1}}{I_{D6}} = \frac{k\frac{W}{L}\left(V_{GT1}V_{\min 1} - \frac{V_{\min 1}{}^2}{2}\right)(1+\lambda V_{DS1})}{k\frac{W}{L}\left(V_{GT6}V_{\min 6} - \frac{V_{\min 4}{}^2}{2}\right)(1+\lambda V_{DS6})}$$

$$1.0465 = \frac{\left(\left(-2.5-V_{T0}\right)\left(-1\right)-\frac{\left(-1\right)^2}{2}\right)\left(1+\lambda\left(-2.5\right)\right)}{\left(\left(-2.5-V_{T0}\right)\left(-1\right)-\frac{\left(-1\right)^2}{2}\right)\left(1+\lambda\left(-1.5\right)\right)}$$

$$1.0465\left(1+\lambda\left(-1.5\right)\right)=\left(1+\lambda\left(-2.5\right)\right)$$

$$\lambda = -0.05\ V^{-1}$$

e) 1 → Saturation
2 → Cutoff
3 → Saturation
4 → Saturation
5 → Saturation
6 → Saturation
7 → Linear