EECS 312: Digital Integrated Circuits
Homework #1

Reading: Section 1.3, 3.2.3, 3.3 of Rabaey

1. a) An electronic design company is preparing to launch two new products, a high-performance, high-volume microprocessor and a low-volume ASIC unit. Several fabrication facilities implementing the desired technology are available to them, including a 4-inch wafer fab and an 8-inch wafer fab. Calculate the *cost per IC* of each design at each fabrication plant (4 calculations, 2 per 4-inch and 2 per 8-inch). Identify the minimum cost fabrication facility for each design.

   The microprocessor die size is 3.2 cm^2 and the projected volume is 50,000,000 units over the lifetime of the product. The cost of packaging the microprocessor is $25.00 per part, cost of testing per part is $2.78, and the non-recurring engineering design cost is $200,000,000.00. The ASIC design is 0.25 cm^2 and the projected volume is only 1,000,000 units. The cost of packaging the ASIC is $0.67, cost of testing is $0.69, and the design cost is $2,000,000.00. For both designs, the functional test yield rate is 95% and α=3. Information on the fabrication options is listed in the table below. *(Hint: Carry significant digits to ensure proper answers)*

Fabrication Facilities for Problem 1		
	4 Inch Fab	**8 Inch Fab**
Cost per Wafer	$150.00	$800.00
Wafer Size (in.)	4	8
Wafer Size (cm)	10.16	20.32
Defect Density (cm^{-2})	0.5	0.56

   b) The operations department suggests studying the impact of transitioning to a new 12-inch fabrication facility for production of the microprocessor part. The 12-inch fabrication facility will cost an additional $1,000,000,000.00 to construct for this project. Develop a constraint on the defect density of this new facility that will ensure cost savings over the previous minimum cost solution. Volume cost for 12-inch wafers is estimated to be $1500/wafer.

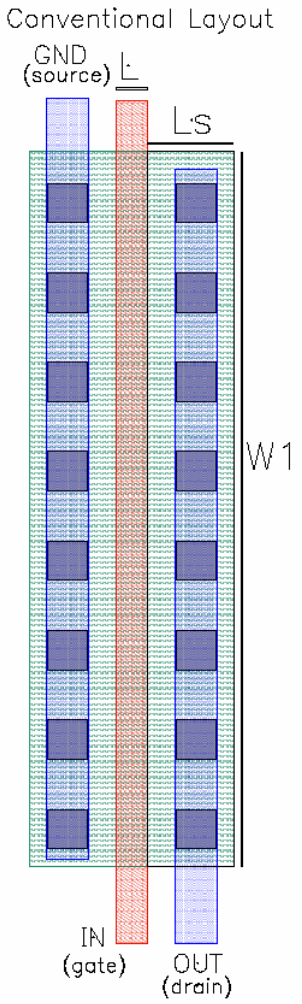
2. a) Given the below SPICE model parameters, determine the junction capacitances C_{db}, the gate-to-channel capacitance, and the gate-to-drain overlap capacitances of both an NMOS and PMOS device, shown in Figure 2.1. Let W_n = 4um and W_p = 6um while L_{drawn} = 0.25um and L_{eff} = 0.2um for both N and P-type devices. Use an approximation that the length of the source/drain regions (L_s in Sec. 3.3 of text) is equal to 2.5*L_{drawn}. To determine the voltage swing(s) of interest to calculate the junction capacitances, consider that the drain of both the NMOS and PMOS devices will swing from 0V to V_{dd} and from V_{dd} to 0. V_{dd} in this case is 2V and we are concerned with the capacitances relevant to 50% delay calculations. Therefore, you should have a total of 4 C_{db} calculations, 2 each for NMOS and PMOS (See Table 2.1). Ignore the bias dependent nature of C_{gc} as mentioned in lecture. Units for and definitions of relevant SPICE parameters are provided in the Lecture Notes from 1/14 which can be downloaded from the course website.

```
.MODEL CMOSN NMOS (                                    LEVEL   = 3
+ TOX     = 5.75E-9          NSUB    = 1E17            GAMMA   = 0.4317311
+ PHI     = 0.7              VTO     = 0.4238252       DELTA   = 0
+ UO      = 425.6466519      ETA     = 0               THETA   = 0.1754054
+ KP      = 2.501048E-4      VMAX    = 8.287851E4      KAPPA   = 0.1686779
+ RSH     = 4.062439E-3      NFS     = 1E12            TPG     = 1
+ XJ      = 3E-7             LD      = 3.162278E-11    WD      = 1.23288E-8
+ CGDO    = 3.1E-10          CGSO    = 3.1E-10         CGBO    = 0
+ CJ      = 2.0E-3           PB      = 0.9             MJ      = 0.5
+ CJSW    = 2.8E-10          MJSW    = 0.44            PBSW    = 0.9)
```

```
.MODEL CMOSP PMOS (                                          LEVEL   = 3
+ TOX     = 5.75E-9          NSUB    = 1E17                  GAMMA   = 0.6348369
+ PHI     = 0.7              VTO     = -0.5536085            DELTA   = 0
+ UO      = 250              ETA     = 0                     THETA   = 0.1573195
+ KP      = 5.194153E-5      VMAX    = 2.295325E5            KAPPA   = 0.7448494
+ RSH     = 30.0776952       NFS     = 1E12                  TPG     = -1
+ XJ      = 2E-7             LD      = 9.968346E-13          WD      = 5.47511E-9
+ CGDO    = 2.70E-10         CGSO    = 2.7E-10               CGBO    = 0
+ CJ      = 1.9E-3           PB      = 0.9                   MJ      = 0.48
+ CJSW    = 2.2E-10          MJSW    = 0.32                  PBSW    = 0.9)
```

Table 2.1 Required Capacitances		
	NMOS	PMOS
C_{db} high-to-low		
C_{db} low-to-high		
C_{gc}		
C_{gd}		

b) Figure 2.2 displays an alternative layout design of a transistor, often referred to as a "folded" layout. It is similar to a pair of transistors connected in parallel to a common drain node. Using the K_{eq}, Cj, and C_{jsw} calculated in part A, compare the capacitances C_{db}, C_{gc}, and C_{gd} with the conventional layout. Do this for the high-to-low transition of an NMOS device only. You may assume that L_s for the folded layout is equal to 2.5*L_{drawn}. What is a possible advantage of this structure, given that it will provide an equal amount of drain current to the conventional design?



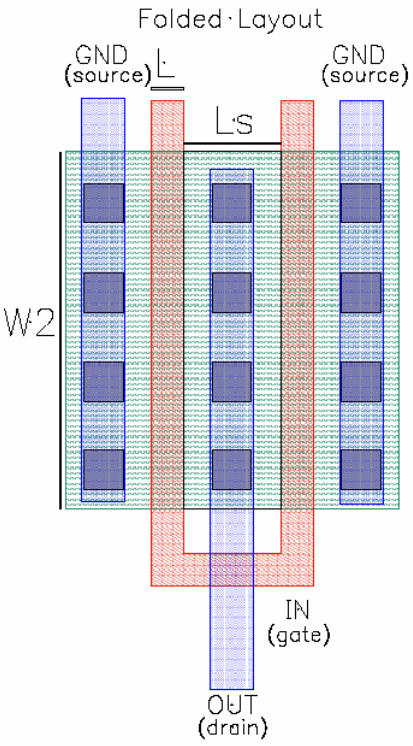
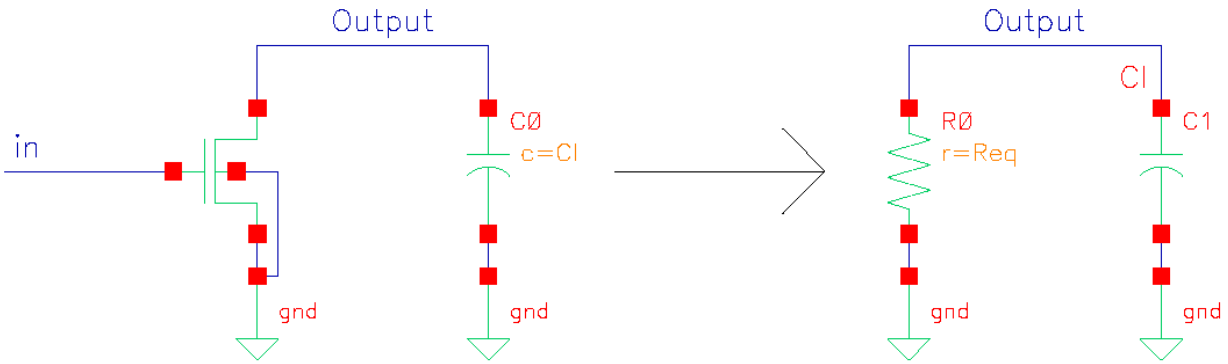


Figure 2.1 Conventional Layout **Figure 2.2** Folded Layout

3. a) As a circuit designer, you control a block of a large scale design in a product that is nearing a time-to-market deadline. The design is targeted to reach 1.2 GHz, optimistically, and the circuit must reach 95% of its final voltage on a falling transition within the clock cycle. The circuit in question is modeled by a simple first-order RC network with a fanout of 3 identical gates with each having 24.4 fF of input capacitance. Find the maximum acceptable value for R_{eq} in the circuit below.

   b) Three days later, a fellow engineer mentions that the fanout of you circuit has increased to 3 identical gates with each having 28.3 fF of input capacitance. The minimum acceptable frequency for market profitability is 1GHz. Will the product be able to meet the minimum performance goal with the increased fanout while using the previously calculated R_{eq}? Show all calculations used to make this judgment.



This simple circuit can be modeled by a first-order RC network for the purposes of this problem.

4. Given Table 4.1, the goal of this problem is to derive important device parameters from these data points. As the measured transistor is processed in a deep-submicron technology, the '**unified model**' holds. From the material constants, we also could determine that the saturation voltage *VDSAT* is equal to -1 V. You may also assume that -2ΦF = -0.6V. ***NOTE: The parameter values on Table 3.3 do NOT hold for this problem.*** *(Hint: You will be working with the 'unified model' in many situations this semester, it may be worth your time to setup a file in Matlab or Excel to assist with these calculations.)*

   a) Is the measured transistor a PMOS or an NMOS device? Explain your answer.
   b) Determine the value of V_{T0}.
   c) Determine γ.
   d) Determine λ.
   e) Given the obtained answers, determine for each of the measurements the operation region of the transistor (choose from *cutoff, linear, and saturation*). Annotate your finding in the right-most column of table 4.1.

Table 4.1: Measurements taken from MOS devices at various terminal voltages.

Measurement number	VGS (V)	VDS (V)	VSB (V)	ID (μA)	Operation Region?
1	-2.5	-2.5	0	-84.375	
2	1	1	0	0.0	
3	-0.7	-0.8	0	-1.04	
4	-2.0	-2.5	0	-56.25	
5	-2.5	-2.5	-1	-72.0	
6	-2.5	-1.5	0	-80.625	
7	-2.5	-0.8	0	-66.56	