312: Exam 2

INSTRUCTIONS

Read all of the instructions and all of the questions before beginning the exam.

There are four problems on this midterm exam, totaling 100 points. The credit for each problem is given to help you allocate your time accordingly. You have a total of 90 minutes to finish this exam. Do not spend all of your time on one problem.

This is an open-book, open-notes exam.

Please place a circle or box around your answers (quantitative ones).

I have <u>underlined</u> the portion of each question that specifically lists what you need to provide in your answer.

Unless otherwise noted on a particular problem, you must show your work (in the space provided plus the back of the pages) for all problems to receive full credit; simply providing answers will result in only partial credit, even if the answers are correct. If you require extra space beyond what is provided, be sure to turn in any material that is required to support your solutions. Note that there is extra work space at the end of this exam booklet.

Turn in the entire exam, including this cover sheet.

Be sure to provide units wherever necessary.

Problem 1 (35 points)

a) Generally, in a pipelined register-based design, is the setup time <u>more, less, or equally important</u> compared to clock-to-Q delay when trying to achieve very high clock frequencies? *Briefly* explain why. (4 points)

b) Specifically, in the circuit below (Figure 1.1) would you prefer FF1 to have a <u>fast clock-to-Q delay OR a fast setup time</u> (choose 1 or the other but not both) for maximum performance? *Briefly* explain why. (4 points)
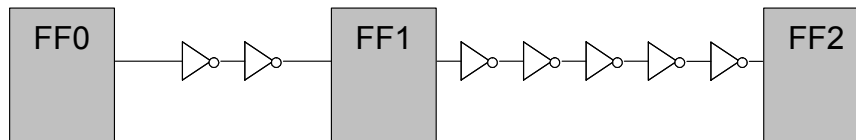

Figure 1.1

c) For the master-slave edge triggered register configuration shown in Figure 1.2, answer the following questions. (5 points)
   i) Two mechanisms were discussed in the lecture for overwriting the data stored in the latch. <u>Which one does the latch in figure 1.2 use</u>?
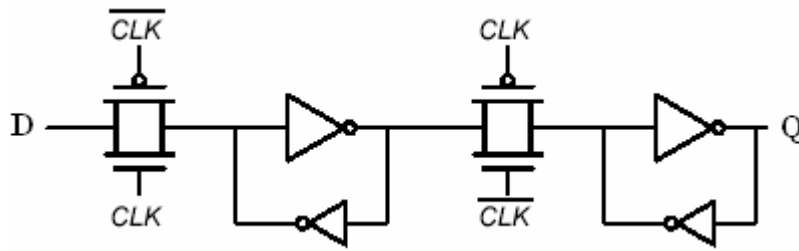   ii) Is this a <u>positive</u> or <u>negative</u> edge triggered register?

Figure 1.2

d) In the latch of Figure 1.3 below, compute the setup time when D is low (that is, a low value is being passed from D to X). The definition of setup time in this case requires that static power in the inverter must be eliminated (except leakage current). Assume the initial voltage at node X is (Vdd-Vthn(Vx)) = 1.8V. You must compute the equivalent resistance of the pass transistor at the midpoint of the voltage swing of interest. Let the width of the NMOS pass transistor be W=1um and the PMOS/NMOS sizes of the inverter are 2um and 1um respectively. Use the 0.6fF/um junction capacitance assumption and ignore overlap capacitance. (12 points)
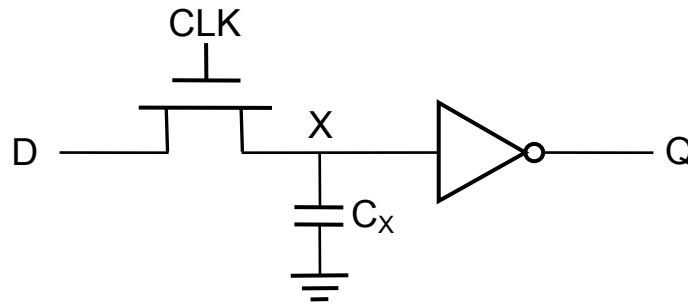

Figure 1.3

e) Given the following clock and data waveforms in Figure 1.4, <u>draw the output waveforms</u> for a 1) positive edge-triggered register and 2) a negative latch. The timing characteristics of these sequential elements are: Tclk-Q = 4 units, TD-Q = 3 units, Tsetup = Thold = 2 units. Vertical dashed lines have a separation of one unit. Note the clock period is equal to 24 units. Clearly mark on the figure where setup and hold time violations occur for each sequential element. (10 points)
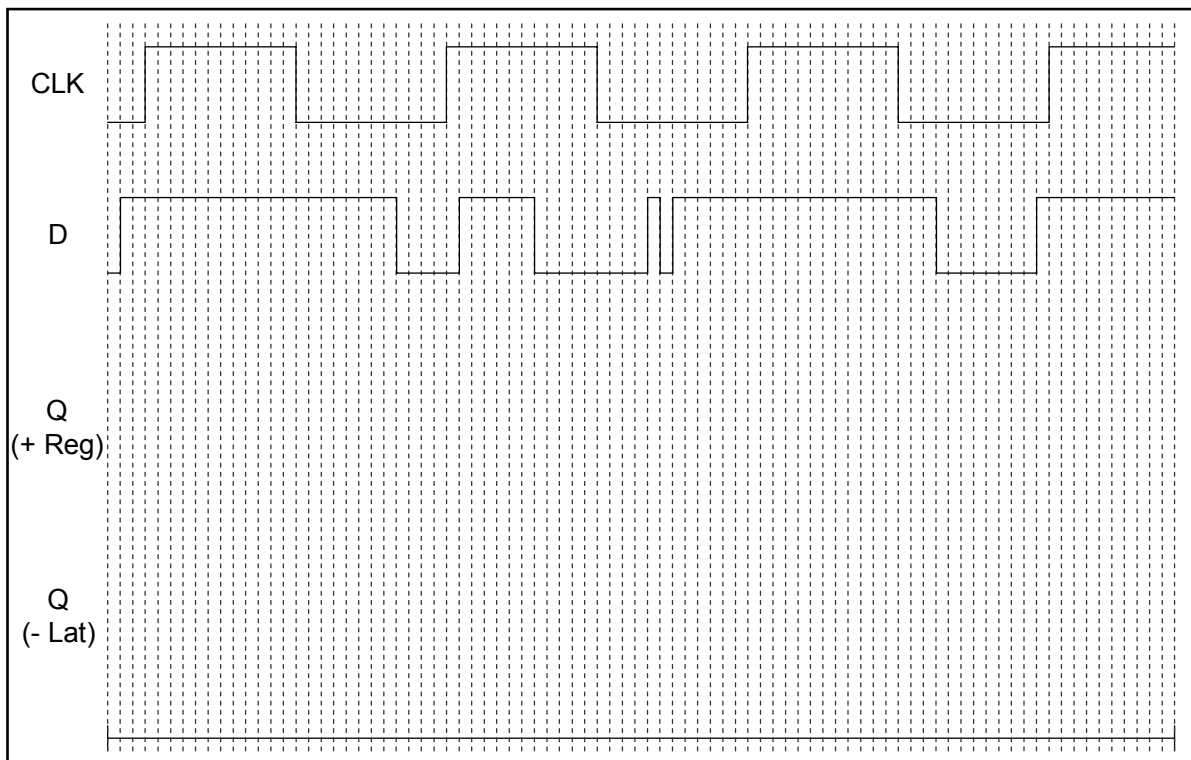

Figure 1.4

Problem 2 (35 points)

In this problem, use the 0.6 fF/um approximation for C_{db}/C_{sb} and calculate gate capacitances ignoring overlap capacitance (C_{GC} only). Let the wiring capacitance C_W on the dynamic node be equal to 4.5 fF and use the Elmore delay when appropriate.
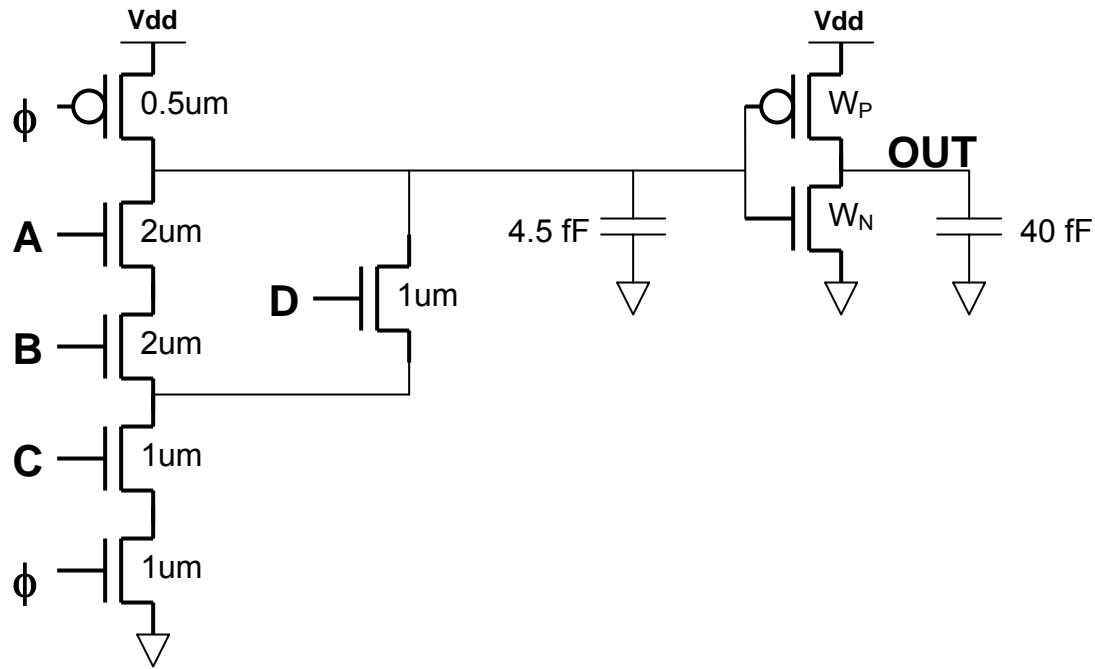

Figure 2.1

a) <u>What function</u> does the circuit in Figure 2.1 implement, from inputs (A,B,C,D) to OUT? Do not include the clock in your Boolean function. (3 points)

b) Find a sizing budget (<u>total width W_P + W_N</u>) for the output inverter such that worst-case t_{pHL} of the dynamic node is less than 90ps. Clearly identify the worst-case input combination in your solution and ignore input slope effects. (8 points)

c) Assign sizes from the sizing budget obtained in (b) such that worst-case V_{OL} at OUT does not exceed 50 mV and delay from inputs to OUT is minimized. Give your answer as <u>values for W_N and W_P</u> of Figure 2.1. (10 points)

d) What is the <u>worst-case static power consumption</u> through the output inverter with the sizes obtained from (c). (5 points)

e) Assume you are using the dynamic gate from Figure 2.1 in a sequential system with latches. <u>What type of latch</u> (positive or negative) must be used to drive the inputs to the dynamic gate? Explain. (3 points)

f) Now, we remove the evaluate transistor and re-size the remaining devices in the dynamic pull-down stack to match the worst-case resistance of the pull-down stack shown in Figure 2.1. Using the same output inverter sizes obtained in (b) and (c), <u>would the worst-case V_{OL} at OUT be higher or lower</u> in this new footless domino configuration? Also, <u>would the evaluate path be faster or slower</u>? Explain qualitatively (no calculations). (6 points)

Problem 3 (15 points)

Consider the 6T SRAM cell in Figure 3.1. Assume a '0' is initially being held at Q and we want to write a '1' from BL to the cell. Let $W_{M1} = W_{M2} = W_{M3} = W_{M4} = 0.5$um. Find a constraint on the width of M6 such that a '1' can be written into the cell. As opposed to the very conservative approach of the textbook, apply a more aggressive analysis to determine when the data is effectively written into the cell. Hint: use Figure 3.2. Consider body bias when necessary (using Figure 3.3) and ignore impact of $\overline{BL}$ and M5 (that is, do not consider the impact of the helpful positive feedback). Assume the driver for the bit line is infinitely strong.
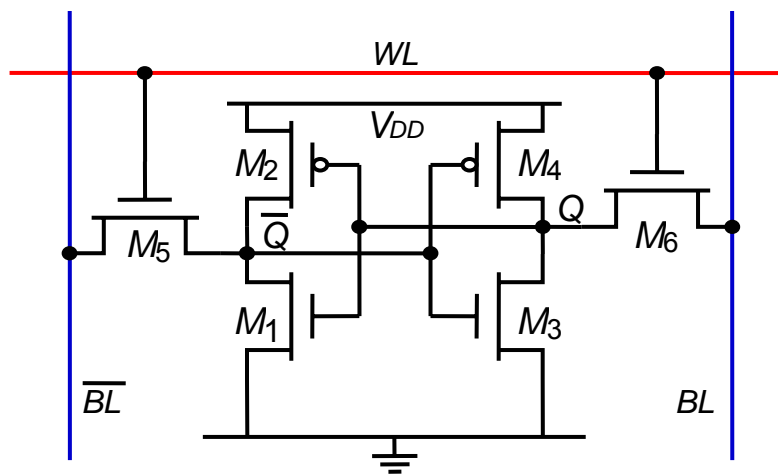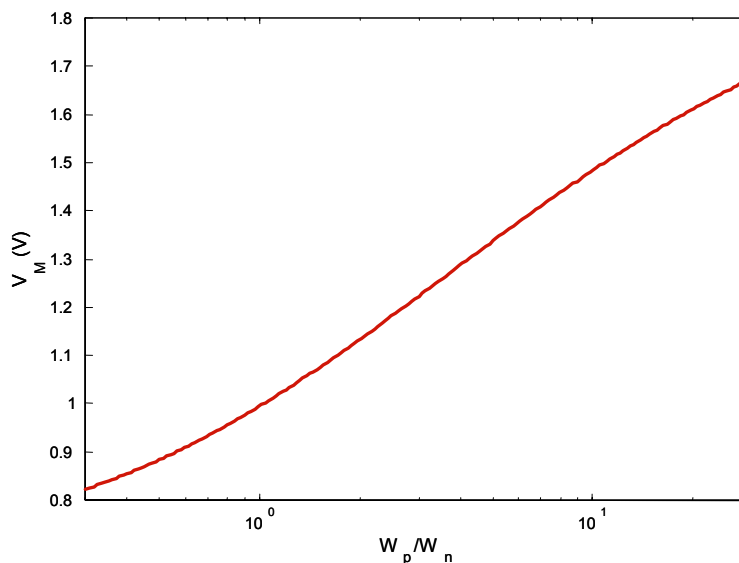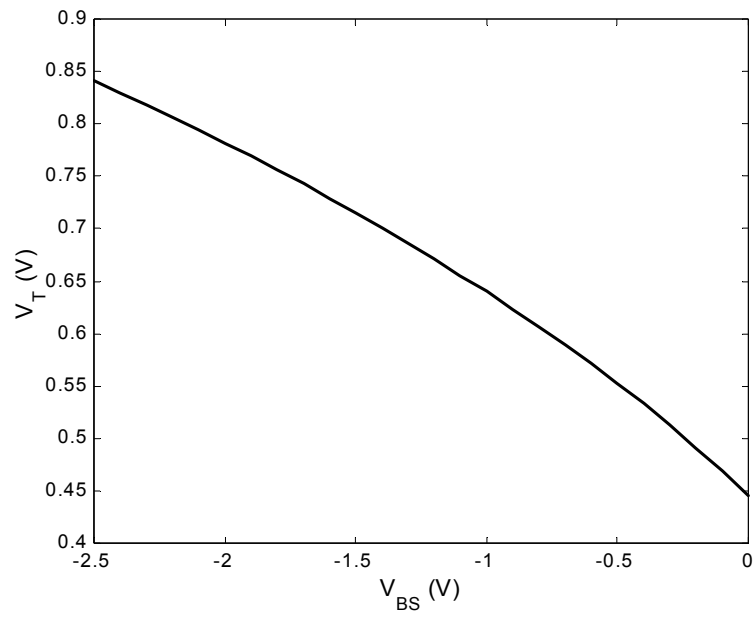

Figure 3.1

Figure 3.2

Figure 3.3

Problem 4 (15 points)

Figure 4.1 shows a PMOS dynamic gate. With reference to the 'Clk' and input ('A' & 'B') waveforms given in the same figure, answer the following questions.

a) Express the gate output (at node X) as a function of A and B. (3 points)
b) Label the precharge (this phase actually discharges the C_{load} capacitor) and evaluate phases on the clock waveform.   (3 points)
c) Suppose you need to find the potential V_{out} at instance t_0. Consider the effect of charge sharing to find two expressions for V_{out} in terms of V_{dd}, V_{ab}, C_{load}, C_{ab}, V_{tn} and V_{tp} (note that all these parameters may not be required). You also need to state the conditions on ΔV_{ab} (change in V_{ab} due to charge sharing) under which these cases are valid.   (9 points)

> Notes: No numerical calculations are required. Ignore leakage. The low and high levels on the waveforms are 0 and V_{dd} respectively.
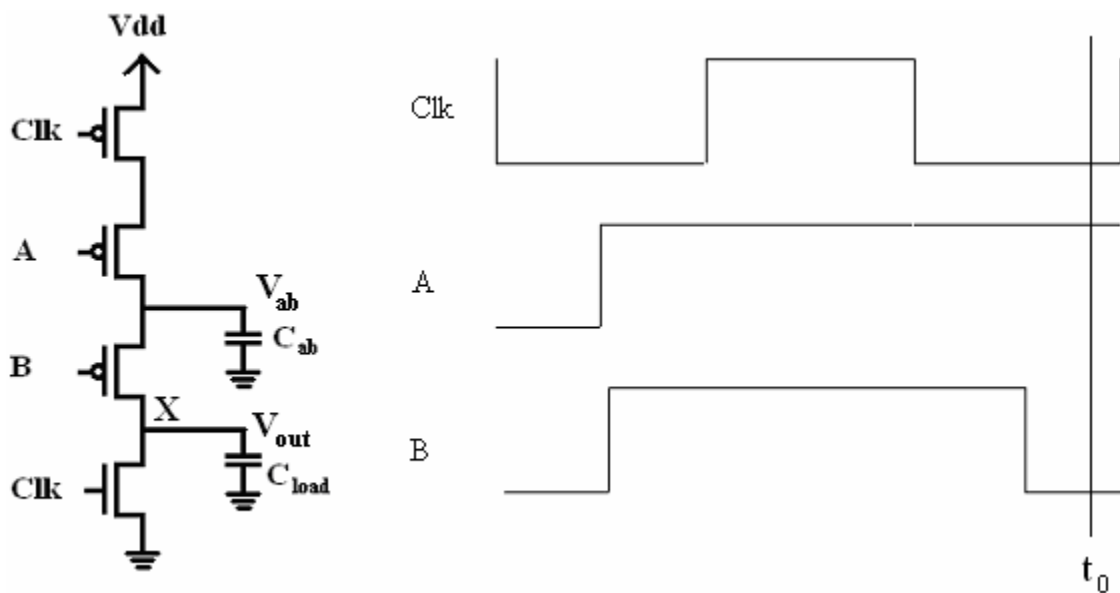

Figure 4.1