LAB #4 Gate Oxidation, Poly-Si Deposition, and Oxide Measurement

Note:

This semester, this lab was done for you. The gate oxidation was done as describe below in the research lab by the lab instructor. The poly dep was done through the MEMS exchange service at Case-Western Reserve University. The deposition condition we would have used in our lab are noted below. Case uses a slightly lower deposition temperature (~605º) but this slight difference will not affect our final results.

Purpose:

We will grow Gate Oxide and measure oxide thickness in the Teaching Lab. The Poly-Si gate deposition will be carried out in the Research Lab by Staff. The Poly-Si gate deposition has to be done in the Research Lab. The wafers will be cleaned before Gate Oxidation and before Poly-Si gate deposition. The gate oxide will be grown to provide electrical isolation between the Poly-Si gate and the channel region.

Process Steps:

1. RCA clean the device wafer and bare monitor wafers.

2. Oxidize the wafers to grow the gate oxides including the device wafer and bare monitor wafers:

i) Set the furnace temperature to 1000 °C and 3 slpm N_2 flow.

ii) Load the wafers in the boat and insert the sled into the elephant.)_

iii) Remove the end cap from the tube and gentle place the elephant in place. Push the sled to the center of the tube using the push rod. Remove the elephant and replace the end cap.

iv) When the temperature re-stabilizes at 1000 °C, begin the following oxidation sequence:

60 min Dry O_2 @ 3 slpm

This should provide a gate oxide thickness of ~50 nm.

v) Pull the sled into the elephant. Remove the elephant and replace the end cap. Allow the wafers to cool, then transfer them to the carriers.

3. Measure the gate oxide thickness on your monitor wafer (#2) using the ellipsometer.

The following will be done by Staff in Research Lab:

4. Deposit Poly-Si including the device wafer and monitor wafers leaving at least one gate oxide monitor wafer with no poly.
   This is a Low Pressure Chemical Vapor Deposition (LPCVD) Technique. The condition used provides a deposition rate for Poly-Si at 9.4 nm/min and ~0.5 μm thick Poly-Si will be deposited. An RCA clean is carried out before the Poly-Si deposition to avoid contamination.

SiH_4 80 sccm (standard cubic centimeter per minute); 625 °C; ~120 mTorr; ~60 min.

5. Measure Poly-Si thickness on field/gate oxide using Lietz SP on monitor wafers #3 and 4.

INFORMATION TO BE INCLUDED IN THE LAB REPORT #2

1. List 2 process conditions that can be used to improve gate oxide quality. Describe 3 types of defects in gate oxide and how they affect device performance.

2. Discuss the effects of gas and pressure on Poly-Si properties.

3. Compare Al gate to Poly-Si gate: list 2 advantages and 2 disadvantages.

4. Carry out Tsuprem4 simulation of gate oxidation and Poly-Si deposition (use the saved structure from Lab #2):
   a) Gate oxide using the same conditions as used in the lab.
   b) Repeat (a) but use wet oxide instead.
   c) Poly-Si gate using the same conditions as used in the lab after (a).
   Include the output files and the plots of dopant distribution. Calculate oxide thickness for (a) and (b) using Deal-Grove model and compare to simulations. Explain their differences. Summarize the oxide thickness grown, Si consumed, linear rate constant, parabolic rate constant, B concentration and B diffusion constants in Si and SiO_2. Discuss dopant distribution after poly-Si deposition. (34 points)

5. Evaluate the measured thickness and uniformity for gate oxide and Poly-Si. Discuss the importance of having uniformity thickness for gate oxide and Poly-Si.