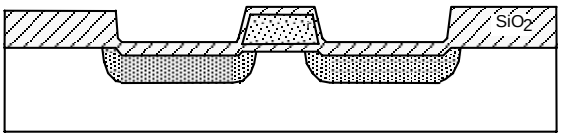
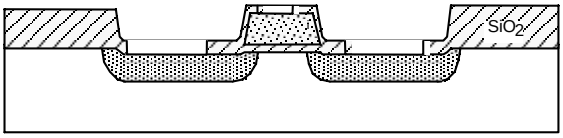
LAB #7

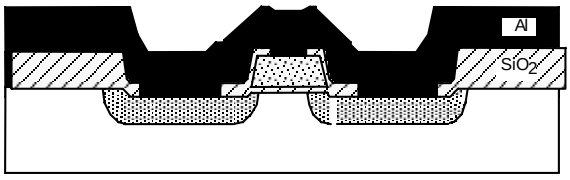
Lithography III for Contact, Contact Etching, and Al Deposition



N+ doped Poly-Si gate and S/D Junctions after Lab #6



Align and Define Contact Pattern Mask
Etch Contact Holes Through Oxide



Deposit Al Over Entire Wafer

The contact openings for Gate are further back and outside the active area.
The contact openings for Source/Drain are within the active area.

- **Measure the Step Height between the Field Oxide and the S/D Regions**
- **Discuss effects of Surface Topography on Photolithography and Device Performance**
- **Discuss effects of Oxide Etch Time**
- **Discuss Al Deposition and other Deposition Technique**
- **Sketch Top View and Cross-Sectional View of Transistor**

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Lithography III for Contact, Contact Etching, and Al Deposition

Purpose:

Contacts holes for source/drain and gate levels will be patterned by optical lithography. The oxide in the contact holes will be etched to the source/drain and gate levels. This oxide was grown during the phosphorus drive-in in Lab#6. In addition, Al will be deposited on the wafer.

Process Steps:

1. Photolithography steps for contact openings:
   Coat wafers with resist and pre-bake following the procedures used in Lab #3.

2. **Align and expose** third mask (contact opening definition):
   [CONTACT MASK]
   POSITIVE PROCESS
   Good alignment is important. You may need to adjust the exposure time. Record the exposure time.

3. Develop and post-bake resist. Record the development time.
   Inspect under the microscope with the photoresist filter in to see if the patterns are fully developed. If not, continue to develop as advised by lab instructor. Inspect carefully for error in alignment across the wafer, and have your wafer checked by lab instructor. If the error is too large, the wafer must be stripped of resist and the lithography must be redone.

4. Descum: Use Technics PE II - A Plasma Etch System:
   300 mTorr of O_2 for 30 sec at 25 W rf power.

5. Based on the BHF etch time needed to remove the oxide grown during phosphorus drive-in obtained in Lab#6, etch the oxide from the device wafer and make sure that the open areas dewet. Rinse and inspect for residual oxide in the contacts over the source/drain (S/D) and the Poly-Si gate contacts. Significant remaining oxides will prevent ohmic contact formation. Excessive over-etch could short the S/D regions to the substrate or the Poly-Si Gate, as well as undercut the Gate Oxide.

6. Strip the resist from the device wafer using PRS 2000 at 110 °C for 2 min, followed by organic solvent clean of 1 min in Acetone, 1 min in IPA, and 3 min in DI H_2O.

7. Evaluate the step height between the field oxide and the source/drain regions by dektak.

Al deposition may be carried out on the new system in the teaching lab or by the staff in the research lab. The research lab conditions would be:

8. Pre-metal clean (include device wafer and monitor wafer #10):
    a) 10:1 HF dip until the Si surface dewets
    b) Normal rinse
    c) Spin Dry

9. Deposit Al using Sputter Deposition (about 500 nm):
    Background pressure ~$5x10^{-6}$ Torr; Ar flow rate = 35 sccm; Voltage = 360 V; Current = 3 A; Pressure during deposition ~7 mTorr; Deposition Rate = 36 nm/min.

INFORMATION TO BE INCLUDED IN THE LAB REPORT #2

1. What are the exposure time, development time, and alignment accuracy (include sketch of alignment marks)? Discuss 2 photolithography problems related to surface topography. Do you expect different results (resolution and resist profile) for Poly-Si gate contacts vs. S/D contacts if the focus is on the Poly-Si gate and not on the S/D regions? List 2 techniques to reduce the problem of topography when defining small features using photolithography.

2. What is the oxide etch time? What happens if there is resist residue on the wafer before the oxide etch? What will happen to the contact resistance, isolation between the source/drain (S/D) and the substrate or Poly-Si Gate, and the Gate Oxide if there is substantial Under-Etch or Over-Etch for the oxide.

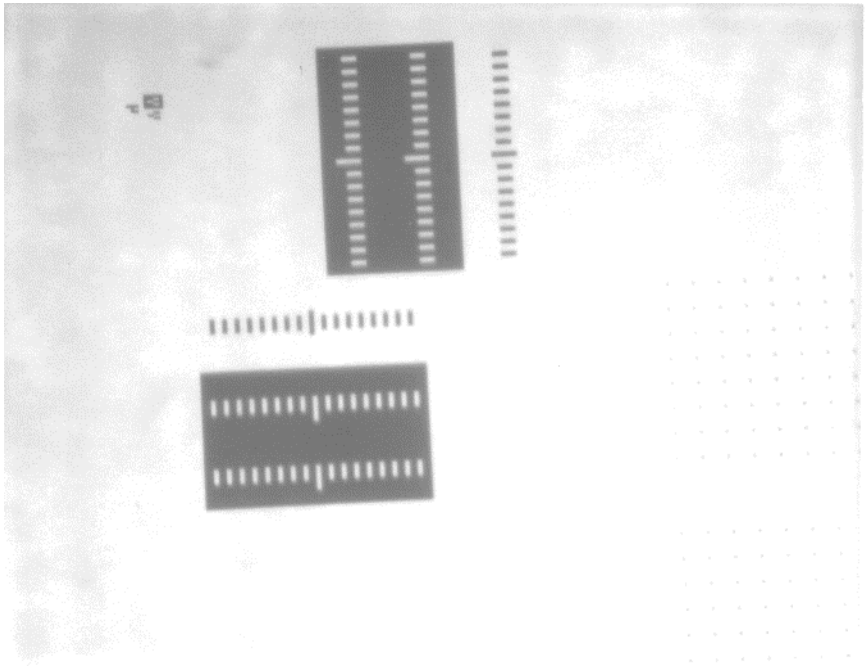
3. Evaluate the step height between the field oxide and the source/drain regions. Does it agree with your expectation? Take into account all the oxide grown in previous Labs. How does a large step height affect the device performance?

4. List 2 important parameters to control during Al deposition for high quality metal contact. Describe 1 other technique to deposit Al and how does it compare with the one used in the Lab?

5. Sketch the top view and cross sectional view of a transistor site after step #5. Label materials and layer thickness.

Contact Mask to open up Contacts for Transistors

Contact Openings for Source, Gate, and Drain



Alignment Marks for Contact Mask