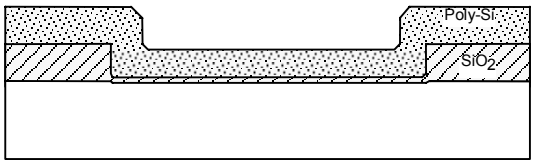
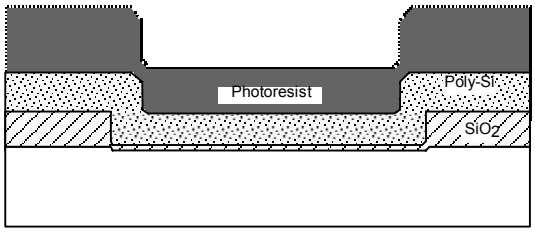
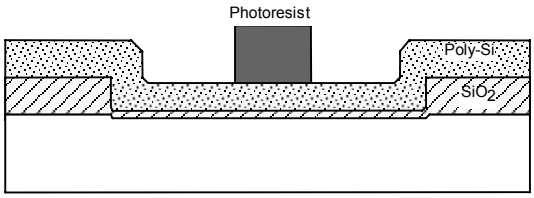
LAB #5 Photolithography II to define Poly-Si Gate, Plasma Etching of Poly-Si, and Wet Etching of Gate Oxide



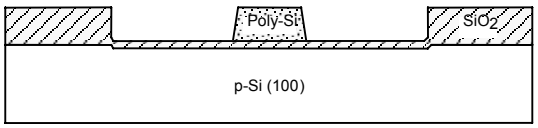
Gate Oxide Grown Lab 4
Poly-Si Deposited in Research Lab by Staff



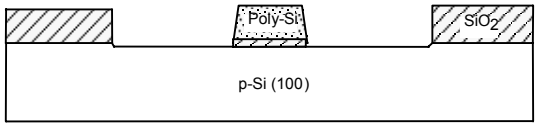
Coat with Photoresist and Spin



Align, Expose and Develop Mask Level 2, The Gate Level



Plasma Etching of Poly-Si Gate and Photoresist Strip



Wet Etching of Gate Oxide

- **Measure Sheet Resistance of Poly-Si; Poly-Si and Gate Oxide Step**
- **Discuss Alignment Accuracy and Resolution of Gate Patterns**
- **Discuss Controlling Factors for Plasma Etching**
- **Discuss Gate Oxide Wet Etching**
- **Sketch Cross Sections and Top View of MOSFET**

LAB #5 Photolithography II to define Poly-Si Gate, Plasma Etching of Poly-Si, and Wet Etching of Gate Oxide

Purpose:

In this lab, you will use photolithography to define the patterns for Poly-Si gate. This lithography step defines the smallest dimension on the wafer, which is the channel length of the MOSFETs. The shortest channels on the mask are 1 μm long. A parallel plate plasma etching system will be used to dry etch the Poly-Si Gates. The Gate Oxide on top of the source and drain regions will be removed by wet etching.

Process Steps:

1. Measure as deposited Poly-Si sheet resistance on monitor wafer #3 using four-point probe:
   You need to get 5 data points (1 center and 4 corners) from a wafer for uniformity analysis.

2. Photolithography steps for Poly-Si gate including the device wafer and monitor wafers #3 and 4:
   Coat wafers with resist and prebake following the procedures used in Lab #3.

3. **Align and expose** second mask (Poly-Si gate area definition):
   [POLY MASK]
   POSITIVE PROCESS
   Record exposure time.

4. Develop and postbake resist following the procedures used in Lab #3:
   Inspect under the microscope with the photoresist filter in to see if the patterns are fully developed. If not, continue to develop as advised by Mr. Briggs. **Inspect carefully for the shortest channels and error in alignment across the wafer, and have your wafer checked by the lab instructor.** If the error is too large, the wafer must be stripped of resist and the lithography must be redone.
   Record development time.
   Sketch the results of your alignment including the gate position within the active device area and the alignment marks. Estimate your alignment accuracy and record the smallest gate dimension obtained on your device wafer.

   The Poly-Si Gate length (channel length) varies from 1 to 40 μm by design. However, some of the 1 μm gates do not show up on the mask. You should check to make sure that

MOSFETs with 2 μm gates show up on your wafer.

5. Descum: Use Technics PE II - A Plasma Etch System:
   300 mTorr of O_2 for 30 sec at 25 W rf power.

6. **Plasma etch Poly-Si Gates** in Technics PEII-A using monitor wafers 3 and 4 for etch test:
   Gas Flow: 25.0 sccm (standard cubic centimeter per minute) of pre-mixed gas with 10% O_2 in SF_6/ O_2
   Pressure: 200 mTorr
   rf power: 75 W
   Etch Time: 2 min 40 sec
   These are just the starting conditions. The lab instructor will help you to adjust them (etch time, rf power, pressure, etc.) for your wafer. Calibration runs are needed before etching your device wafer.
   If etching is non-uniform, you may need to etch half way, open up the chamber, and then rotate the wafer to finish up the etching.
   Inspect carefully for residual Poly-Si after etching, and continue etching if necessary to clear the wafer. Do not continue etching if any evidence of gate oxide etch-through develops.
   Again, since the Poly-Si gates have the most critical dimension for your transistors, you need to have good control of the dry etching step.
   Record the uniformity of your Poly-Si etching. Draw a map to identify the areas with working devices (complete etching of poly-Si gate and gate oxide without too much undercutting). This record of working devices will be needed when you do device testing.

7. Strip the photoresist from the wafers. Since the photoresist tends to be hardened after plasma etching, you may need to use an O_2 plasma etching to remove all the photoresist:
   Wet etch in PRS 2000 at 100 °C for 2 min.
   Plasma etch in O_2 at 300 mTorr and 25 W rf power for 1 min.

8. Dektak the Poly-Si step on the monitor wafer after dry etching of the Poly-Si.

9. Inspect your device wafer under the microscope. Pay particular attention to the apparent color in the source/drain regions to make sure all Poly-Si is removed.

10. Use the gate oxide monitor wafer (#2) to find an etch time for the **removal of the gate oxide in BHF** (~30 sec). When you have a dewet time for the monitor, etch the device wafer for the same time. Rinse and inspect for residual oxide in the source/drain regions. Significant remaining oxides will block the phosphorus pre-deposition. Excessive over-etch will damage the oxide under the gate.
    You need to stop the oxide etching by **quickly** rinsing the wafer in DI H_2O.

11. Dektak the Poly-Si step on the monitor wafer after wet etching of the Gate Oxide.

INFORMATION TO BE INCLUDED IN THE LAB REPORT #2

1. Evaluate and explain the measured sheet resistance and uniformity for Poly-Si. Discuss how the gate resistance affects the device performance.

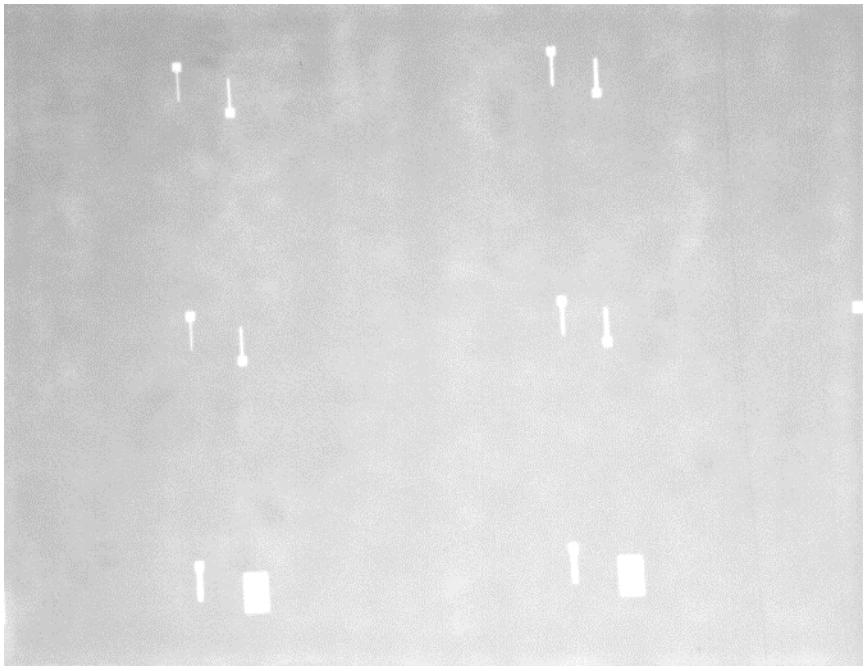
2. What are the exposure time, development time, alignment accuracy, and shortest channel length patterned? Discuss 3 important parameters (radiation source, resist, and process conditions) that can be used to print smaller gate lengths. Explain two problems if you don't have accurate alignment.

3. What are the Poly-Si etch time, etch step, and etch uniformity? Discuss 2 ways to improve etch uniformity (system design, gas flow, power distribution) and 3 process conditions (power, pressure, gases) that can be controlled to etch smaller features.

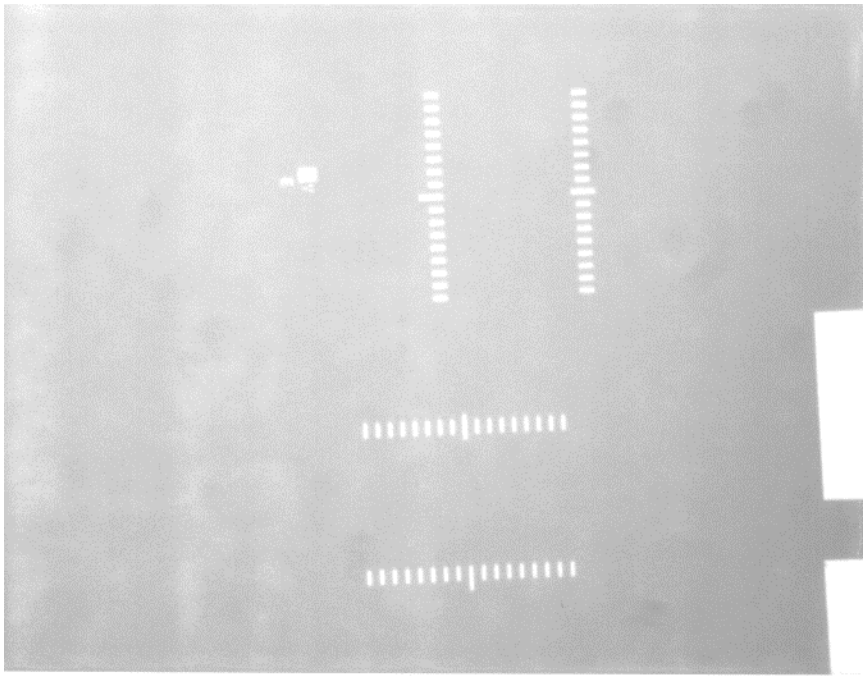
4. What are the oxide etch time and step height after oxide etch? What is the estimated etch profile and how could one get vertical profile in gate oxide? What are the effects of wet etching the gate oxide underneath the Poly-Si too long or too short on device performance?

5. Sketch the cross section of a MOSFET after Steps #6 and 10. Pay special attention to the profile after the etching of the Poly-Si gate and gate oxide. Sketch top view of a MOSFET after Step #10. Remember to label materials and thickness.

Poly-Si Gate Mask to define Conducting Channel (Critical Dimension)



Gate Length varying from 4 to 40 µm



Alignment Marks for Poly Mask