Solid State Device Laboratory

Lab Report #4 Assignment: Final Report

Comprehensive Process Report:

Perform 1-D Tsuprem IV simulations for your devices that cover the complete process for:

1. The gate region of the transistors
    a. Simulate the process based on the nominal intended conditions
    b. Adjust the gate oxidation condition appropriately to match the spectroscopic ellipsometry result for the gate oxide monitor (data on class web site)
    c. Include the Tsuprem electrical simulation of the transistor threshold voltage
2. The S/D region of the transistors
3. The field oxide region (for regions covered by poly-Si)
    a. Simulate the process based on the nominal intended conditions
    b. Adjust the field oxidation condition appropriately to match the spectroscopic ellipsometry result for the gate oxide monitor (data on class web site)
    c. Include the Tsuprem electrical simulation of the poly gate field transistor threshold voltage
4. The field oxide region (for regions covered by Al)
    a. Adjust the field oxidation condition appropriately to match the spectroscopic ellipsometry result for the gate oxide monitor (data on class web site) (from part 3.b above).
    b. Estimate the amount of field oxide that was lost from various etch steps. List the process step, the estimated amount lost, and include any appropriate measurement data on this issue.
    c. Including the effects of etching of the field oxide, use the Tsuprem electrical statement to estimate the Al gate field transistor threshold voltage

For each region, construct a table showing the predicted results from Tsuprem of all major parameters (film thickness, sheet resistances, junction depths, etc.) In the same table, show any relevant measurements from the laboratory (film thickness, sheet resistances, junction depths, etc.). Comment briefly on any differences between simulation and measurement. The objective will be to summarize your process results. You may be repeating commentary you have made in earlier reports, so keep it brief and to the point. Only brief comments on these procedures should be included in you final process report

Device Results Report:

Summarize in tables the following information:

1. For the large area diode (cell 20 on the test die):
    a. Diode reverse breakdown voltage, forward ideality factor (n), and saturation current I_s. If possible, estimate the series resistance R_s also.
    b. Comment on all these values vs. what you would expect given the process parameters and device dimensions. Given that this is an n+/p diode and assuming that long-region recombination behavior applies, estimate the relevant minority carrier lifetime.

2. 40x40μm transistor
    a. Measure the gate characteristic with V_{DS}=50mV and VGS=(V_T-1V) to at least (V_T+10V), extract V_T for V_{SB}=0, 1, 2, 3, 4, 5 V.
        i. Compare V_T at V_{SB}=0 to the theoretically expected value.
        ii. Extract the body effect parameter γ. Use this to extract an effective substrate doping N_B
    b. Subthreshold swing parameter S for V_{SB}=0, 1, 2, 3, 4, 5 V
        i. For V_{SB}=0, use this value to estimate the interface state density D_{it}.
        ii. Why does S change with V_{SB}?
    c. Extract and plot the surface mobility vs. gate bias (from the gate characteristic measurement).
    d. Plot the surface mobility vs. average vertical field (E_{ave}) (from the gate characteristic measurement).
    e. From the Drain Characteristics, extract the V_T and average mobility from the saturation region. How do these values compare with those of the gate characteristic measurement?
    f. Also from the drain characteristics measurements, what is the smallest working transistor?
3. For all the functioning MOSFET gate lengths with W=40μm:

a. Measure the gate characteristic with V_{DS}=50mV and VGS=(V_T-1V) to at least (V_T+10V), extract V_T for V_{SB}=0V. Is there significant variation of V_T with gate length?
b. Extract the transconductance (g_m) over a set V_{GS} range for all these devices. Choose this range of V_{GS} so that the gate characteristic is linear.
c. Using the data from b, estimate the ΔL between the MASK gate dimensions and the electrically effective L's.
d. Using the estimate of c, plot the surface mobility vs. average vertical field (from linear region gate characteristic data) for all of your working transistors (W=40μm). Is there any significant variation due to channel length?

Tsuprem output files should be attached to the back of the report. Your report should not require me to look at your Tsuprem text files for numbers. Include those in the question answers. You should take care to discuss differences between Tsuprem, hand calculations, and lab measurements in as much technical depth as you can.

You can attach plots of your electrical test results as an appendix as well. However, only the most relevant ones should be included in the body of the report for grading.