Quiz 4

EECS 427: VLSI Design I

CLOSED BOOK, CLOSED NOTES

Underlined text highlights the specific parts of questions you need to answer. Please keep explanations as **brief as possible while getting across the key point**. This will demonstrate to me that you know the material well.

1. Qualitative (30 points, 6 each)

a) What are the two primary reasons why memory yield is often low compared to standard logic circuits?

b) Give two main reasons why leakage power in memory is potentially more significant than in logic.

c) Why are soft errors due to alpha particles/cosmic rays becoming more problematic in scaled technologies?

d) List two negative side effects associated with designing a clock distribution network with slew rates that are *too fast*.

e) From a noise margin perspective is IR drop on the ground rail more of a problem for dynamic or static circuits? Why?

2. (Parts a and b are independent of each other) (28 points)

a) See the below transformation where $w = w_u + w_l$:

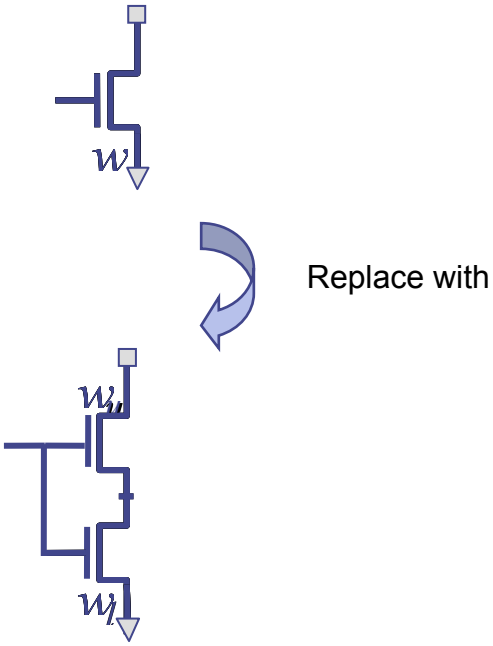


Figure 1

What is the primary drawback of this transformation? Also, does the transformation/replacement provide *active mode*, *standby mode*, *both,* or *no* leakage reduction relative to the initial (upper) configuration?

b) Given the simple circuit block between latches in Figure 2, first determine the lowest leakage state (ABC=???) to be assigned during standby mode. Then for each of the latches 1, 2, and 3, determine which latch style shown below should be used. Assume 'clk' is held low during standby mode through clock gating techniques.

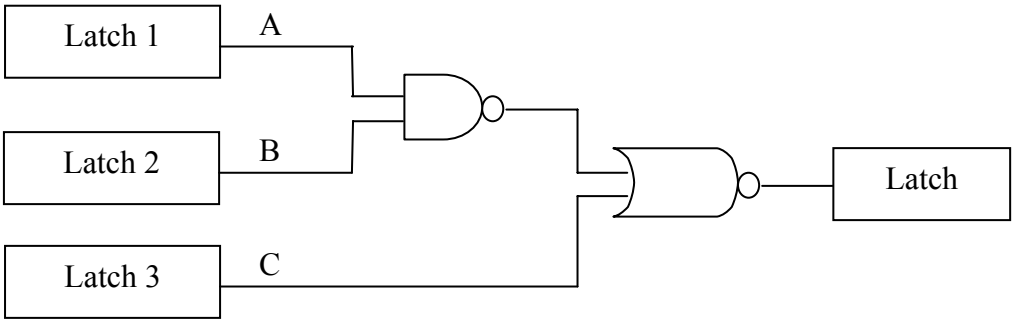
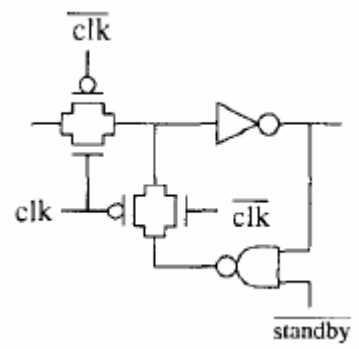
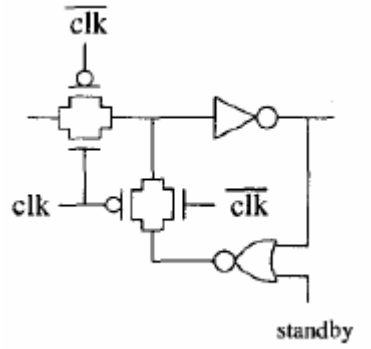


Figure 2



Latch style 1



Latch style 2

3. (12 points)

a) In Figure 3, assume there is a long bus structure with large coupling capacitances between each wire. The standard non-inverting repeater is shown at the top of Figure 3 and consists of two standard CMOS inverters. These non-inverting repeaters are replaced by the (also non-inverting) design at the bottom of Figure 3. *Concisely* explain what primary benefit the new circuit has compared to the original repeaters.

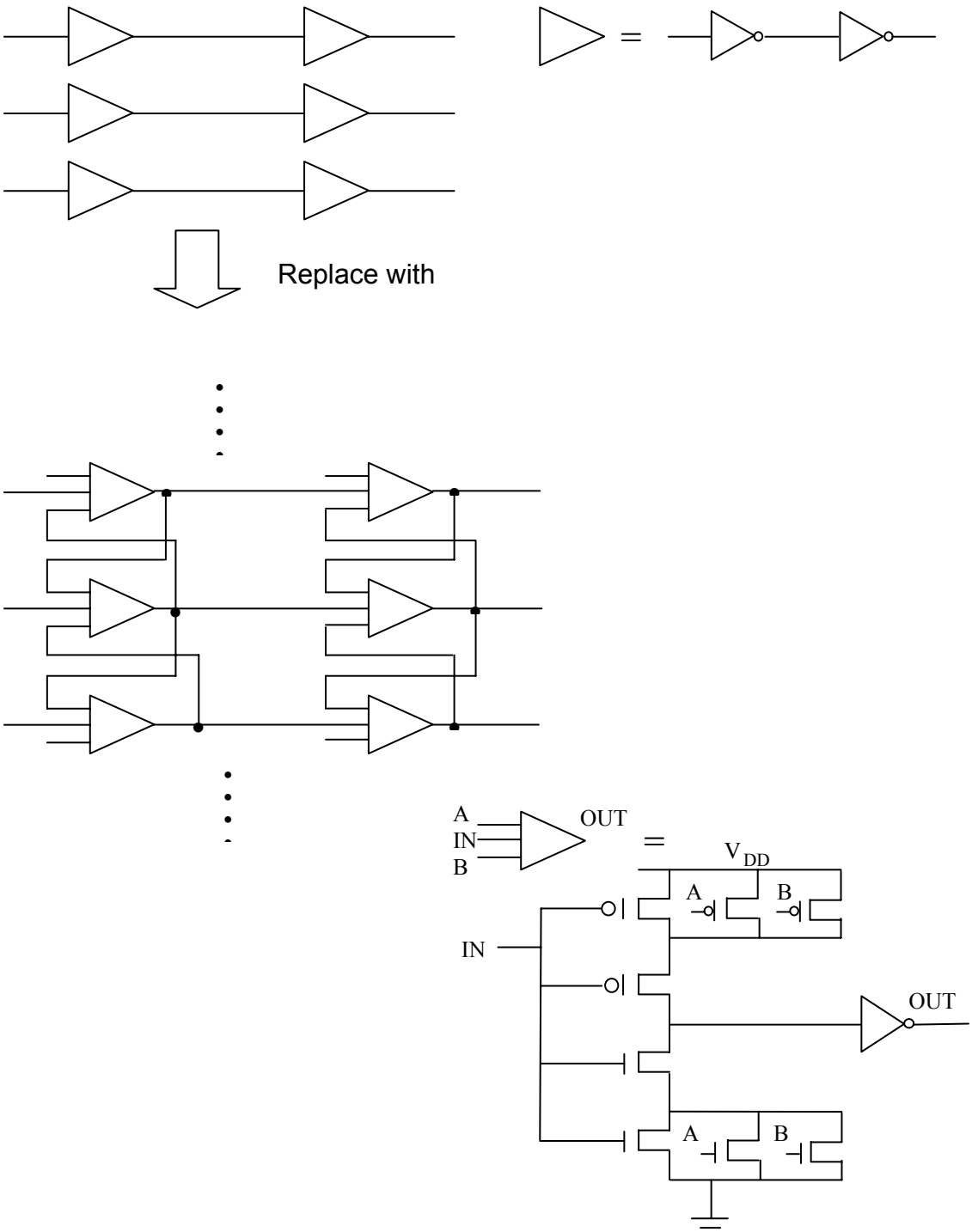


Figure 3

4. This question relates to the circuit in Figure 4. Let the nominal NMOS Vth be 0.45V and NMOS Vth considering worst-case body effect is 0.65V. (30 points)

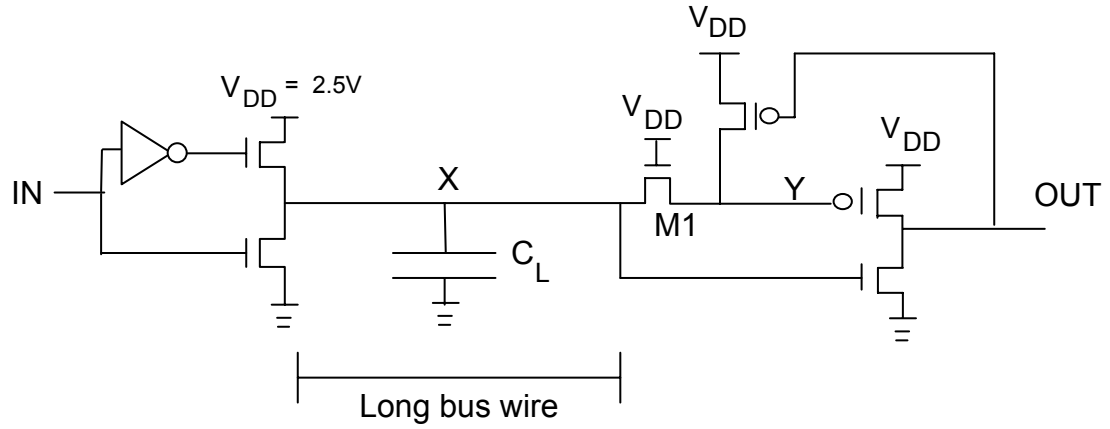
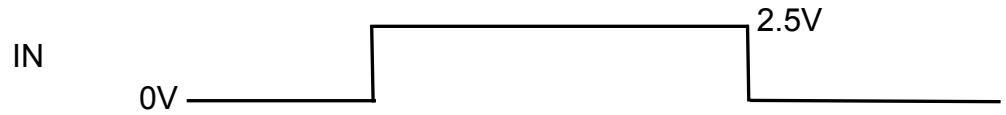


Figure 4

a) Assuming IN toggles from 0 to 2.5V and back to 0V, draw the corresponding waveforms at nodes X, Y, and OUT. Be explicit about voltage levels in steady-state. Do not worry about accuracy/precision on the x-axis (time).



b) What energy savings do you expect from the circuit in Figure 4 compared to the case where C_L is driven by a simple inverter (V_{dd}=2.5V) and the receiver is also a simple inverter? Express the savings as a ratio and assume C_L dominates relative to other capacitances in the system.

c) If the pass transistor M1 is removed, shorting nodes X and Y, what would the energy savings then be, again expressed as a ratio relative to the case with a simple inverter as driver and receiver?

d) Now assuming M1 is still present in the circuit, does the receiver in Figure 4 consume appreciable static power in steady-state besides leakage currents? If so, explain.