

Quiz 3

EECS 427: VLSI Design I

CLOSED BOOK, CLOSED NOTES!!

Underlined text highlights the specific questions you need to answer.

1. (30 points)

a) Is the following piece of Verilog code behavioral or structural?

```
module half_adder (a,b,sum,carry);  
  input a, b;  
  output sum, carry;  
  reg sum, carry;  
  always @ (a or b)  
  begin  
    carry = a & b;  
    sum = a ^ b;  
  end  
endmodule
```

b) Generate the complete set of test vectors to check for a stuck-at 0 fault at G3 in the circuit below (Figure 1).

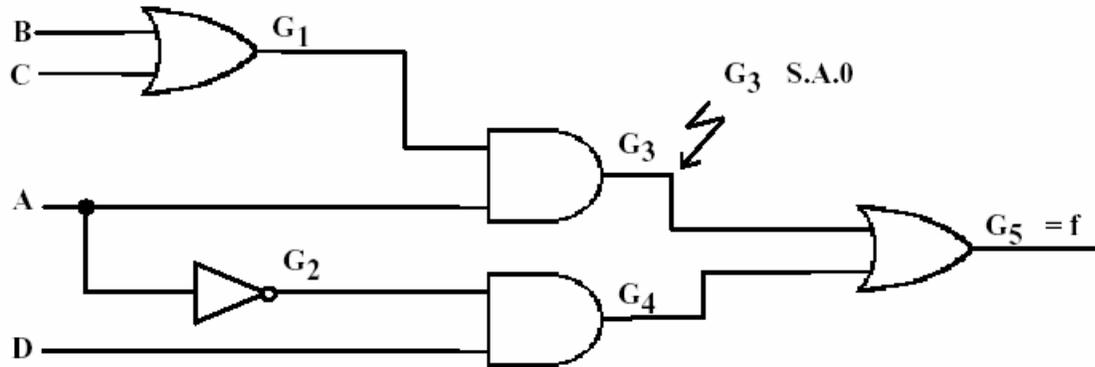


Figure 1

c) For a 3-input NAND gate, there are 8 possible single stuck-at faults and 8 possible input vectors. How many test vectors are actually needed to cover all possible faults? List them.

2. (40 points)

a) Given the plot of CLK-Q delay vs. data arrival time and using the 4 data points shown, find minimum D-Q delay for this register. Taking the definition of setup time as the point at which CLK-Q delay rises 5% from nominal, what is the setup time of this register?

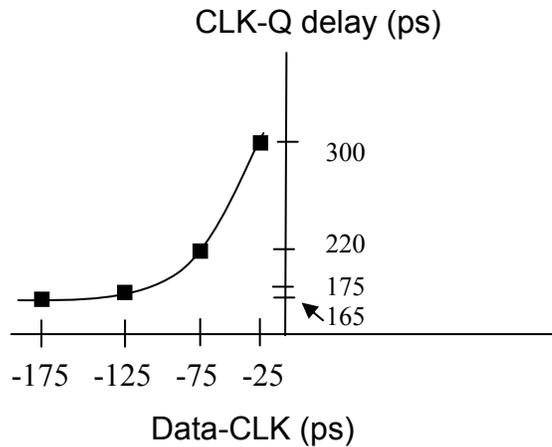


Figure 2

b) Explain qualitatively why pulsed registers have faster CLK-Q delays than traditional master-slave edge-triggered registers. Also, what is a major disadvantage of pulsed registers?

3. (30 points)

a) What are the two main reasons that SRAM arrays use sense amplifiers?

b) Why are row decoders in SRAMs particularly suited to the use of dynamic circuits?

c) In the below latch-based sense amplifier (Figure 4), explain whether or not the PMOS device gated by \overline{SE} is necessary and why.

d) Also, what function does the added NMOS pass transistor gated by signal EQ perform? What is the relationship between signals EQ and SE ?

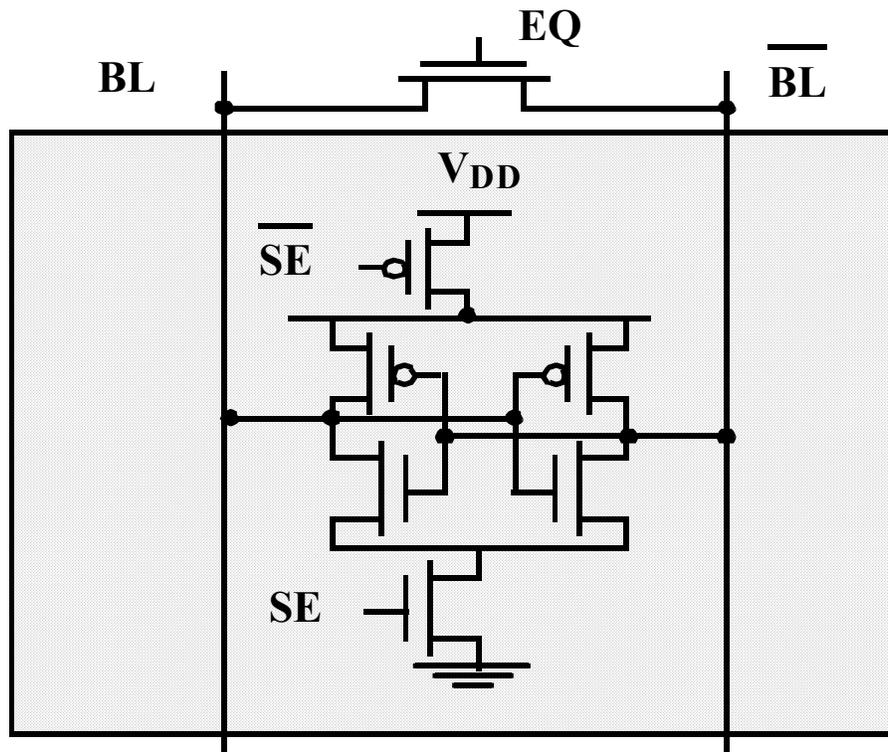


Figure 4