CAD1   Inverter/Nand/2:1 Mux

Assignment

Create schematics, symbols, and layouts for an inverter and a 2-input nand gate. Using these symbols and layouts, create a schematic, symbol, and layout for a 2:1 mux using 3 2-input nand gates and 1 inverter. Perform design-rule-checks (DRC) and a layout-vs.-schematic (LVS) check on the layouts of the inverter, 2-input nand, and 2:1 mux. Then, get accurate propagation delays for the 2:1 mux by extracting parasitic capacitances from the layout and simulating the circuit with Eldo. Add the resultant rise and fall propagation delays to your schematics and re-simulate in Modelsim.

You probably will not use any of these cells in your final project, so don't be concerned about choosing the "right" cell height or choosing optimal transistor sizes. Try to minimize area and feel free to use all layers available to you. While layout area will be considered in grading, do not spend a lot of time optimizing the layout to save on area.

The first two cad assignments are to be done on your own. You may discuss use of the cad tools and basic layout concepts with other students, but your design, particularly your layout, should be created by yourself.

Description

- Create a directory in your class account called **cad1**. All of your files will need to be in this directory in order to be graded.
- Make the **schematics** and **symbols** for the inverter and 2-input nand using Design Architect (**da**). Call the inverter ports **in** and **out**. Call the nand ports **in0**, **in1**, and **out**.
- **Simulate** the inverter and nand in Modelsim and verify correct functionality. Test all possible inputs for both gates. Create the input stimulus as you did in the inverter tutorial, by creating a small verilog module that instantiates the device under test and forces the inputs. For example, you might have a file called testnand.v containing a module testnand that instantiates nand2.
- Follow the guidelines of *The Design and Simulation of an Inverter* to create layouts for the inverter and 2-input nand. Make sure that you use the same names to label the inputs and outputs of the gates in IC Station that are used on the symbol. Keep in mind when designing these gates that they will be used in the layout of the 2:1 mux. Examples of things to keep in mind: (1) How will you route between the 4 cells? (2) How will you place the cells to create a 2:1 mux? (3) Where will you place your input and output ports? For example, you could place all your cells in a straight line or in a square. **Choose a configuration that minimizes interconnect length.**
- Perform a Design Rules Check (**DRC**) on the layouts of the inverter and nand gates. Save the DRC reports into the files **drc_<component_name>.rep**. For directions please refer to *The Design and Simulation of an Inverter*.
- Generate an **lvs viewpoint** for the inverter and nand as illustrated in the inverter tutorial.
- Perform a Layout Versus Schematic (**LVS**) on the layouts of the inverter and nand gates. Save the LVS reports to the files **lvs_<component_name>.rep**. For directions please refer to *The Design and Simulation of an Inverter*.
- Make the **schematic** for the 2:1 mux using the previously designed inverter and nand gates. To instantiate the inverter and nand in the 2:1 mux sheet use the **choose symbol** command from the palette. Use the Navigator to reach the appropriate directory if the

inverter and nand are in a different directory from the mux. In this document, the mux will be called **mux2**.

You also need to include the **delay** component from theTSMC25_lib between your final nand gate and the output. This will be used to add the delays observed in EZwave. The delay component has RISE and FALL properties attached to its **out** pin. These can be changed later to include the rise and fall delays of the mux. The delay component has no layout counterpart but since it is *transparent* to LVS, you should not have any problems.

- Generate an **lvs viewpoint** for the 2:1 mux in DA as illustrated in the inverter tutorial.
- **Simulate** the 2:1 mux in Modelsim and verify correct functionality. Force values on the two inputs and select such that all possible input combinations are accounted for.
- Follow the guidelines of *The Design and Simulation of an Inverter* to create layout for the 2:1 mux.

The only structures that you may use in the 2:1 mux are the cells created earlier in this CAD assignment and metal1, metal2, metal3, or polysilicon to connect those cells. Make sure that you use the same names to label the inputs and outputs of the 2:1 mux in IC Station that are used on the symbol. Also try to minimize your use of upper metal layers.

- Perform a Design Rules Check (**DRC**) on the layouts of the 2:1 mux, saving the DRC report.
- Perform a Layout Versus Schematic (**LVS**) on the layout of the 2:1 mux, again, saving the report.
- Extract the capacitance values from the 2:1 mux using **ICextract(M)**. Save the PEX reports**.** For directions please refer to *The Design and Simulation of an Inverter*.
- Use Eldo to simulate the circuit in the analog domain. Refer to the inverter tutorial for details as to how to use it. Prior to doing this, add an additional 25fF load on the mux output as described in the inverter tutorial.
- Insert the delays obtained from EZwave into the 2:1 mux schematic. You need to modify the **rise** and **fall** properties to the delay component in the output stage of the 2:1 mux.
- Resimulate the schematic in Modelsim to verify that it functions as before. You should see a slight shift in the output waveforms because of the added delays.

Requirements

For the first CAD experiment, you need to have the following files in the directory **cad1**:

- inverter, 2-input nand and 2:1 mux schematics and layouts (leave in DA or IC format).
- Modelsim .wlf and .do (see NOTE below) files for the inverter, 2-input nand and 2:1 mux without delays added.
- Modelsim .wlf and .do files for the 2:1 mux with delays added.
- Eldo configuration files (see NOTE below) for the rise and fall delays for the 2:1 mux: <component_name>_<configuration name>. If you have multiple traces for a given component, give a descriptive name.
- Wave .jpgs (see NOTE below) of the critical path waveforms generated by Eldo.
- DRC report from ICrules for the inverter, 2-input nand, and 2:1 mux.
- LVS report from ICtrace for the inverter, 2-input nand, and 2:1 mux.
- PEX reports from ICextract for the 2:1 mux.
- Include a README file containing the full path names for all of the cells the grader is to look at, and any comments you wish to pass on to the grader. Include in the file the maximum rise and fall times. List the nodes between which the rise and fall delays were maximum, and explain why. Provide a brief paragraph describing any relevant points in your design. Any comments will be taken into consideration when your assignments are graded.

For this and future cad assignments, follow these submission guidelines:

- Call the README file README (not readme, readthis, info, cad1_readme, etc.)
- drc reports: drc_<component_name>.rep
- lvs reports: lvs_<component_name>.rep
- pex reports: pex_lumped_<component_name>.rep, pex_netlist_<component_name>.rep
- Modelsim .do (.wlf): vsim_<component_name>.do (.wlf). Ditto the above for comments for Eldo files.

NOTE:

Creating Eldo Configuration files:
A configuration file is created by default each time you run Eldo. When you're in the simulation mode, click on *Session* in the palette, then on *Copy Configuration…* Enter a descriptive name, and click OK. Now, when you modify forces, etc. the settings will be saved under this configuration. Upon submission, make sure this configuration contains the most up to date forces you set.

Creating Wave .jpgs:
When you view your waveforms in EZ Wave, use cursors to find your rise and fall delays. Save an image of your waveforms with the cursors in place that helped you calculate delay. Do this by selecting File > Export in EZwave and save waveforms with descriptive name (i.e. rise_delay.jpg).

Creating Modelsim .wlf and .do files:
For modelsim, a .wlf file is created by default each time you run vsim. This file contains the complete simulation database but no information regarding which waveforms should be displayed and in what order to display them. That is determined by the modelsim .do file. You can specify the name of this file when you launch vsim: *vsim -wlf vsim_inverter.wlf* will save the database to vsim_inverter.wlf. The .wlf file will be saved properly ONLY if you exit the simulation properly via File->Quit. If you ctrl-C out of the simulator, you may get a corrupted .wlf that the grader cannot load. After displaying the signals in the waveform window, you can save the waveform window format by selecting File->Save Format. This will open a pop-up prompting you for a filename. The modelsim .do file will come in handy for you in later cad assignments as you can save and restore waveform configurations quickly. You should verify that your .wlf and .do files work properly in modelsim by loading the .wlf (File->Open->Dataset) then load the .do in the waveform window (File->Load Format).