Assignment

To design a register cell.

Description

In this CAD assignment, you will design, layout and simulate a 1-bit register (flip-flop) cell. Your full-custom datapath will require a couple of multi-bit registers and you should design this 1-bit register as a bit-sliced component for this purpose. You probably won't use this cell in your final datapath but this exercise will introduce you to complex leaf-cell design as well as datapath-style layout concepts. Note that once again you must work on your own for this assignment.

Implementation

It is often desirable to be able to reset asynchronously the state of the register to a known value (usually zero).

A typical logic gate implementation of a positive edge triggered master-slave D flip-flop is shown in Figure 1.

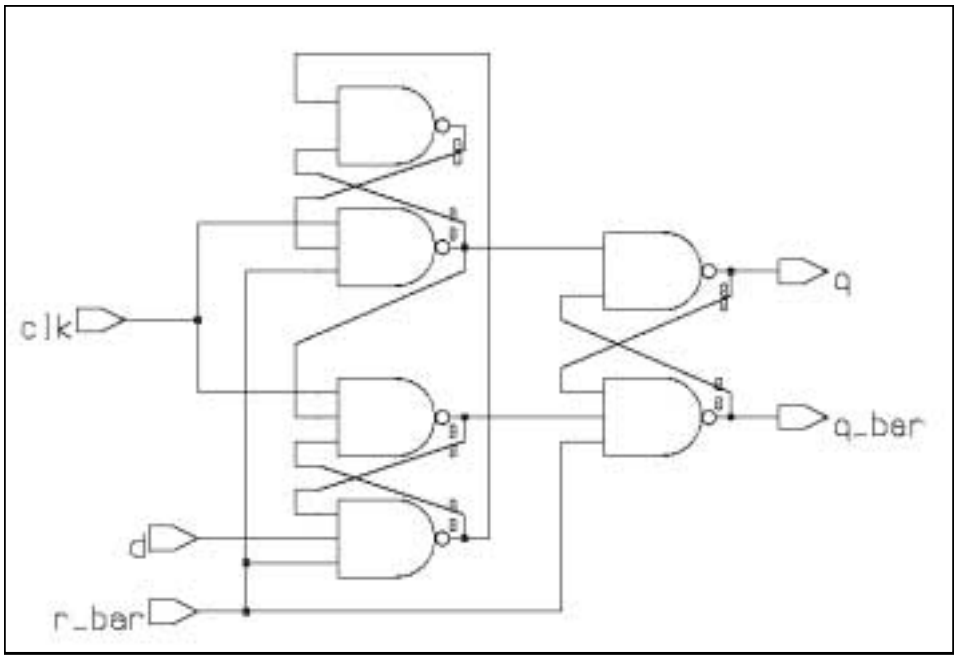

Figure 1: Positive Edge Triggered Flip-Flop Using Logic Gates

An example for a static CMOS transmission gate-based implementation is shown in Fig. 2. Use of this design, or similar designs more adapted to CMOS technology, would result in many fewer transistors than the flip-flop of Fig. 1, and it is not recommended that Fig. 1 be used. Note that a conceptually simpler starting point would be a flip-flop composed of two latches (connected in master/slave configuration) like the master latch in Fig. 2.

The flip-flop could be further compacted by using a dynamic or pseudo-dynamic style with two-phase or single-phase clocking, but we do not support these design styles for EECS427. At this time, Modelsim will not support dynamic circuits modeled at the switch level.

Layout Considerations

Compared to CAD1 you should pay more attention to the layout aspects of this design. Consider this a bit-sliced component with a target bit-slice width (pitch) no less than 75 lambda. Bit-slice widths larger than 100

lambda will likely result in odd aspect ratios for your complete datapath. If the bit-slice pitch is too small (e.g. 40 lambda), you may find in the future that you don't have enough space to route data buses over top of the datapath. Your layout must be a flat layout - i.e. no hierarchy. This will result in a more compact layout. On this and all future CAD assignments, we will be looking more closely at your layout density.

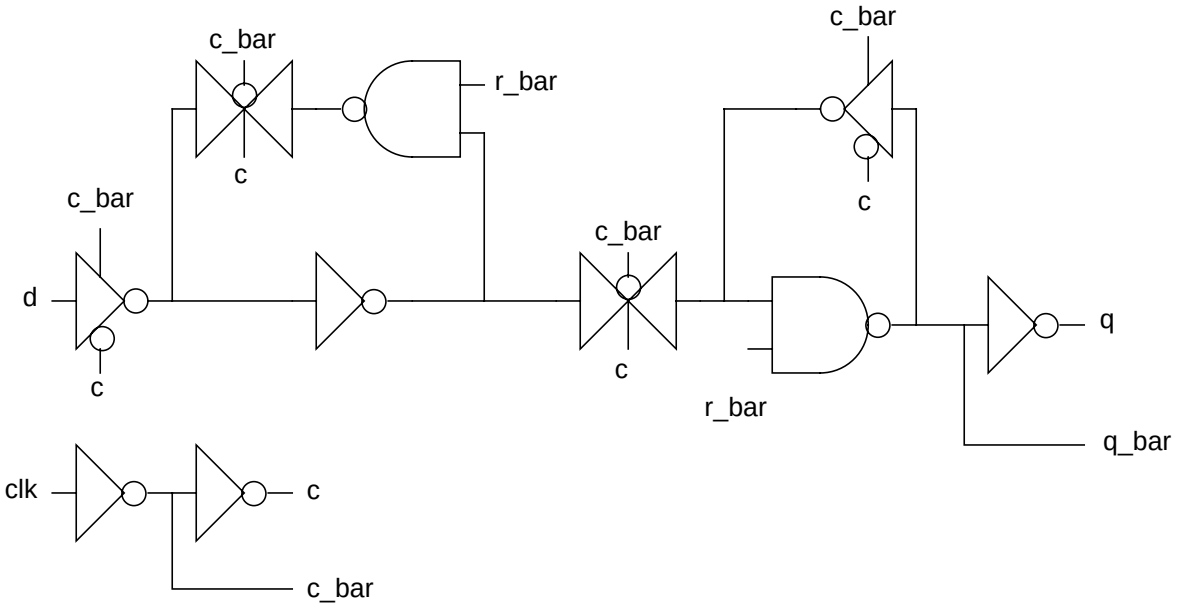

Figure 2: Positive Edge Triggered Flip-flop Using CMOS Transmission Gates and Clocked Inverters

Procedure

Schematic design

Make a directory called **cad2** and do all your work in that directory. Choose the type of flip-flop that you wish to implement, but be sure to make the top-level cell resettable asynchronously to zero. You do not have to be concerned about speed performance of your designs yet. This will come into play in CAD3.

Create a transistor level schematic of the D flip-flop and an eldonet viewpoint.

Digital Simulation

Run Modelsim on the dff cell to exhaustively simulate the various input and output combinations.

Layout and Verification

When implementing the layout of your cell, you should keep in mind the various layout considerations. While doing DRC and LVS, follow the same procedure as in CAD 1. Be sure to match the ordering of the inputs in your schematic and layout. Save the DRC and LVS reports as **drc_<comp_name>.rep** and **lvs_<comp_name>.rep** respectively.

Extract the parasitic capacitances and back annotate those as you did in CAD 1. While editing the output capacitance, ADD a capacitance of 25fF to the cap_net value of the output "q" to account for the load capacitance that may be caused by the circuit that the dff drives. Save the PEX reports as **pex_lumped_<comp_name>.rep** and **pex_netlist_<comp_name>**.

Analog Simulation

Run Eldo on the dff and obtain the rise and fall CLK-Q delay times as well as the rise and fall setup times for the dff (Exactness not required for the calculation of setup time). Use the 'cursor' to find your delay estimates. Save an image of your waveforms with the cursors in place that helped you calculate delay. Do this by selecting File > Export in EZwave and save waveforms with descriptive name.

Add rise/fall delays to your digital models

Add a delay module in your schematic at the output of the dff and add your RISE and FALL CLK-Q delays and then simulate in Modelsim again.

Comments

- Refer to the handout "Datapath Floorplanning and Routing in a Three Metal Layer Process" for an overview of datapath-style layout. Bit-sliced layout design and following a routing plan that allows for over-cell routing will lead to a good physical design. Again, you probably won't use this in your final project so mistakes will not be costly.
- Reports are a very useful source of information for debugging. All Mentor tools have facilities to generate reports. These are usually accessible from the **Report** option in the pulldown menu. Please make use of these to get information which might prove valuable for sorting out problems. For example, suppose you have mistakenly added a port to the wrong layer and its causing a problem in LVS. If you select all the shapes in the cell and do:

  Report > Ports

  You can get a list of all the ports and the layers they are associated with. This will help identify the errant port. A shortcut for generating a report is to select an object, then, while holding down the middle mouse button, drawing a lower case "r" on the schematic/layout sheet.

Requirements

You should have the following in your **cad2** directory.

- Schematics of your D flip-flop with the delays added.
- Modelsim .wlf and .do files showing functional verification of your 1-bit register, with delays. Briefly describe each simulation in your README file.
- Layout of the D flip-flop.
- Make sure your Eldo config file and your wave.jpg's show the following: maximum rise and fall CLK-Q delays and setup time for each. Rise/fall delays are measured from the 50% point of CLK to the 50% of the Q output transition. You do not have to be exact about the setup time - just get within a few picoseconds.
- DRC report from ICrules for the D flip-flop.
- LVS report from ICtrace(M) for the D flip-flop.
- The ICextract report files showing the parasitic capacitances and real s/d areas and perimeters for the D flip-flop.
- A README file with the names/paths to all the requested files (layout, schematics, drc report, do-files, etc.). Include a few short paragraphs describing your choice of design and verification.