EECS 427
Homework 1
Relevant sections to review: 3.3.2, 5.3, 5.4, 6.2, 7.1.1, 7.2.3

Default technology: the minimum drawn channel length = 0.25um, the effective channel length for L_{drawn} of 0.25um is 0.2um, nominal V_{dd}=2.5V, see table "CMOS (0.25um) – Unified Model" on inside back cover of Rabaey for other parameters.

Unless otherwise specified assume that the junction capacitance of a MOSFET is equal to half of its gate-to-channel capacitance C_{gc} (i.e., $C_{db} = C_{sb} = C_{gc}/2$). Ignore overlap capacitances. Assume cutoff region when computing gate capacitance (Table 3-4) and note that the relevant channel length term for the capacitor area is the effective channel length.

1. In a CMOS inverter with minimum channel length transistors and W_n=1um:
    a. Find W_p such that $V_M \leq 1V$ and t_{plh} is minimized.
    b. Also, find t_{plh} in this case when the total output capacitance is 10fF. Refer to Table 3.3 of Rabaey (pg 106) to help in computing delay. However, make the change that the table entries are for W=0.25um and L_{eff}=0.2um. Ex: for V_{dd}=1V and W_n=0.5um, R_{eq} = 35kΩ/(0.5/0.25) = 17.5kΩ. In Equation 5.3 of Rabaey, $r = k_p*V_{dsatp} / k_n*V_{dsatn}$ but is NOT equal to $v_{satp}*W_p/v_{satn}*W_n$.

2. Fanout of four inverter delay (FO4) is a commonly used metric to define both the speed of a technology process and the extent of pipelining used in modern microprocessors. It is defined as the delay of an inverter driving 4 copies of itself with no wire loading.

    a. For the book's default technology and Wp/Wn = 2, compute the FO4 inverter delay assuming that the junction capacitance of an inverter is equal to ½ its gate capacitance. Let the delay be given by the greater of t_{phl} and t_{plh}.
    b. Also, Intel's 0.13um process has a ring oscillator (i.e., fanout of one inverter) delay of 8ps. Using this information to determine the FO4 delay, compute the number of FO4 inverter delays in a clock cycle for the 3GHz Pentium 4 that uses this process technology.

3.
    a. Implement the equation $X = ((\underline{A} + \underline{B})\cdot(\underline{C} + \underline{D} + \underline{E}) + \underline{E}) \cdot \underline{G}$ in a CMOS gate.
    b. Size the devices so that the output resistance is the same as that of an inverter with W_n = 0.5um and W_p = 1.5um.
    c. Which input pattern(s) give the worst and best equivalent pull-up or pull-down resistance? If there are multiple input patterns that provide worst-case resistance, you only need to provide one.

4. See Figure 1 for a timing diagram of a positive edge-triggered register with data input D and output Q. Draw the corresponding output waveform given the relevant timing information for setup and hold times and clock-q delay. Please mark times at which either the setup or hold time are violated. Assume Q is initially low.

5. Let there be a 2-in NAND with inputs A and B; all devices in the gate have W = 1um and L_{drawn}=0.25um. In the NMOS stack, input A is the topmost device. The steady-state initial input pattern is 00 (AB=00) and then input A changes from 0 to Vdd. How much energy is drawn from the supply voltage as a result of this input change? Do not consider the energy used to charge the gate capacitances connected to input A.

T_{CLK-Q} = 3 units, T_{setup} = T_{hold} = 2 units

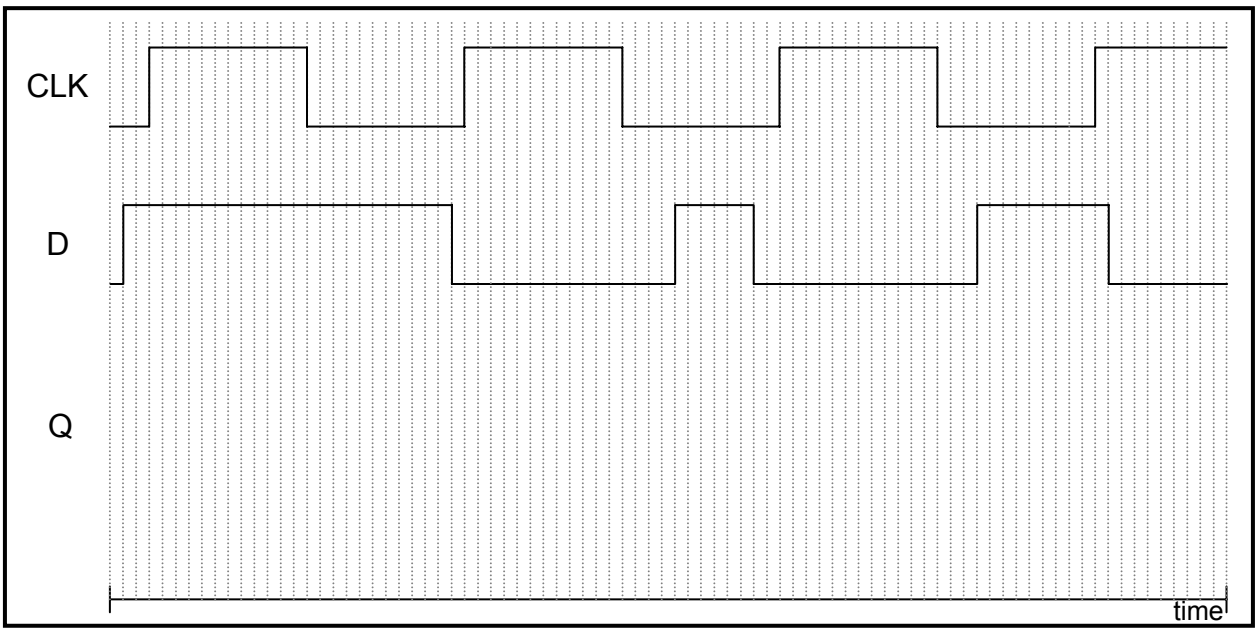

Figure 1.