Quiz 1
EECS 427: VLSI Design I

CLOSED BOOK, CLOSED NOTES!!

Underlined text highlights the specific questions you need to answer.

1. Given the layout in Figure 1, draw cross-section A-A'. You must label the various materials and layers in the cross-section. Also, what purpose do the multiple substrate and well contacts serve? *Briefly* explain. Finally, what type of logic gate does this layout represent? [35 points]

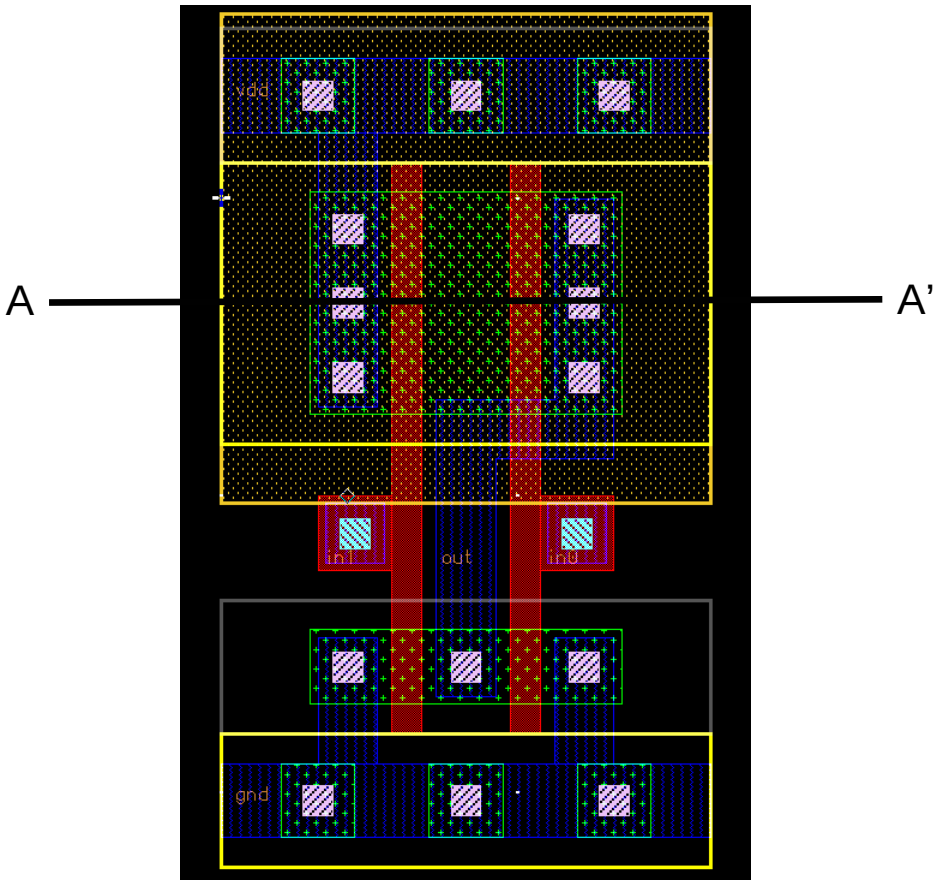

Figure 1

2. What function F does the gate in Figure 2 perform? [10 points]

   Highlight the transistor(s) that form the critical path of this gate. What input pattern triggers this worst-case delay and which of the two inputs must switch to activate this worst-case pattern? (Only final state is needed, not initial. Assume PMOS devices are twice as wide as NMOS.) [17 points]

   AB =
   Circle one: A switches OR B switches

   What are V_{OL} and V_{OH} of this gate? (You should answer V_{OL} and V_{OH} symbolically, not numerically, but be as specific as needed). [8 points]

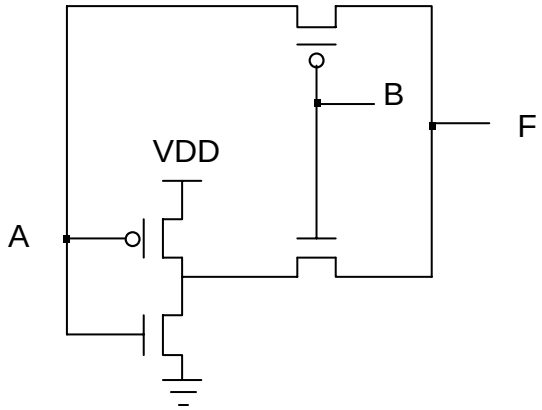

Figure 2

3. Figure 3 shows a 16-bit carry bypass adder that is broken up into 4 blocks of 4 bits each. Find the first-order worst-case delay of this adder to generate the 16-bit sum (ignore the final carry out) given the following delay parameters: Multiplexer delay is 150ps, calculation of propagate and generate bits takes 150ps, delay of a single-bit adder to produce the sum is 150ps, the delay of a single-bit adder to produce the carry-out is 100ps, delay of a 4-input AND gate is 200ps. Also find the best-case delay through the adder. [30 points]

   BONUS CREDIT (do this part last): If you could rearrange the carry bypass adder of Figure 3 by making the blocks different sizes (leaving the number of blocks at four), how would you partition the adder and what would the minimal delay be given the above delay parameters? [10 bonus points]

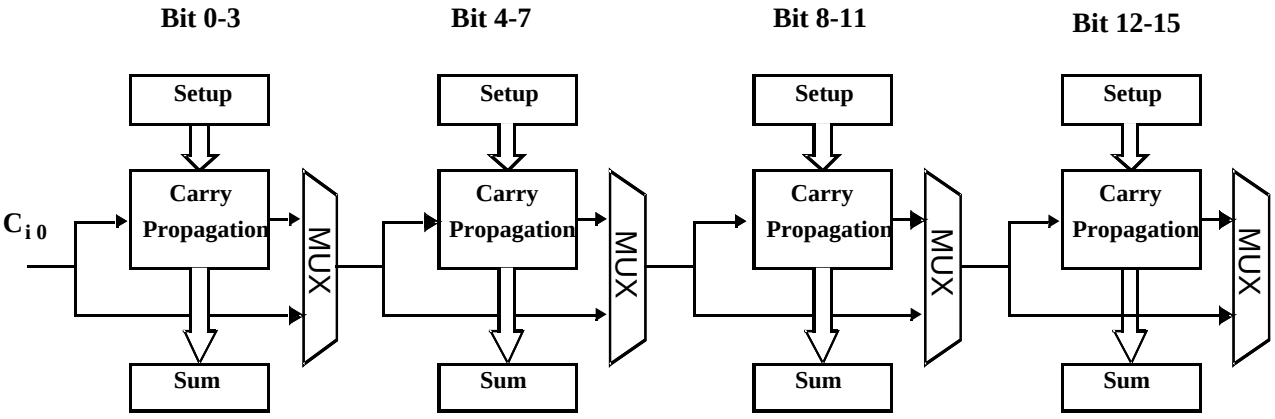

Figure 3