Quiz 2
EECS 427: VLSI Design I

<u>CLOSED BOOK, CLOSED NOTES!!</u>

<u>Underlined text</u> highlights the specific questions you need to answer.

1. Arithmetic units [29 points total]

   a) A portion of example 11.5 from the Rabaey text is shown below. There is a minor error in the example – <u>find this error</u>. [4 points]

   Example 11.5: Modified Booth's Recoding
   Consider the 8-bit binary number 01111110 shown earlier. This can be divided into four overlapping groups of three bits, going from *msb* to *lsb*: 00(1), 11(1), 11(1), 10(0).

   b) <u>Perform twos complement binary multiplication</u> of -6 times 7 using a 4-bit multiplicand and multiplier. Use modified booth recoding on the multiplier which is 7 in this case. [15 points]

   c) The use of a log shifter with base 4 instead of 2 is helpful in reducing the number of series connected pass transistors in shifters with potentially large shift amounts. A drawback is the need to re-encode the shift amount, whereas in $\log_2$ shifters this information is already encoded properly. For a 16-bit $\log_4$ shifter, <u>how many control bits are required</u>? Also, <u>provide the mapping from the binary encoded data 0111</u> (shift amount of 7) to the actual $\log_4$ shifter control bits. [10 points]

$x_{i+2}x_{i+1}x_i$	Add to partial product
000	+0Y
001	+1Y
010	+1Y
011	+2Y
100	-2Y
101	-1Y
110	-1Y
111	-0Y

Figure 1. Modified Booth's recoding.

2. Figure 2 shows an unpipelined datapath. Data you will need for this problem is included in Table 1. The delay of each functional unit scales identically with Vdd. Assume MOSFET saturation drain current is governed by the following relation: $I_{dsat} \propto (Vdd-Vth)^{1.5}$. Vth in this process is constant at 0.4V and the nominal Vdd is 2.5V. [65 points total]

a) <u>Find the maximum achievable clock frequency</u> in this design ignoring clock skew. [10 points]

b) For a fixed clock frequency (taken from part (a)) assume it is possible to run the arithmetic units in this unpipelined design at one of two different supply voltages, 2.5V and 1.5V. <u>Which unit(s) would you run at 1.5V</u> and <u>what is the resulting power savings</u> (expressed as a percentage savings) compared to the initial design? Ignore level conversion. [15 points]

c) Implement a 2-stage pipeline version of this datapath with the goal of balancing the delays of the two pipeline stages as much as possible (<u>provide a diagram showing where you inserted registers</u>). Now reduce the *single global Vdd* (note: no longer dual Vdd as in part (b)) as far as possible to achieve maximum power savings with the constraint that throughput, indicated by clock frequency, cannot be reduced below the initial unpipelined case. <u>What is the achievable power reduction</u> by using pipelining in this datapath? [25 points]

d) If some worst-case clock skew, δ, were introduced in this system, <u>how would it impact the power savings</u> (state whether it would increase or decrease and why)? If the skew were introduced by mismatched wire capacitances in the routing paths to the various registers in the system, <u>would the skew depend upon the supply voltage</u>? Briefly explain why or why not. [15 points]
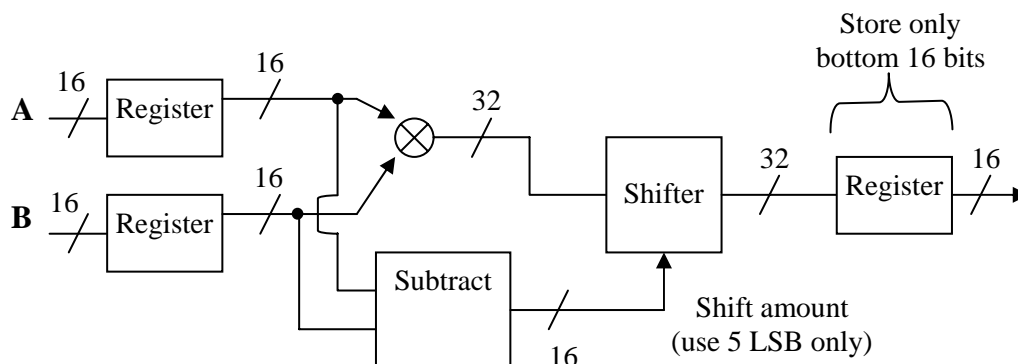

Figure 2

Table 1: Delay values (at Vdd=2.5V) and capacitances of each functional unit

Functional Unit	Delay	Capacitance
Multiplier, $\otimes$	8ns	1pF
Subtract	3ns	300fF
Shifter	2ns	350fF
16-bit register	Setup time: 100ps Clk-Q: 500ps	100fF

3. Peer contribution forms should have been completed through CAD5 before taking this quiz to receive the 6 points for this problem.