EECS 470
Homework 4

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1. Consider the following access pattern: `A, B, C, A`. Assume that A, B, and C are memory addresses each of which are in a different block of memory. Further, assume A, B and C are generated in a uniformly random way **and that a "true" LRU replacement algorithm is used. Further, assume that any given block has an equal chance of being placed in either "way".**
   What is the probability that the second instance of "A" will be a hit if:
   - The cache has 2 lines and is direct-mapped [1].
   - The cache has 2 lines and is a direct-mapped hash-cache [1].
   - The cache has 2 lines and is fully-associative [1].
   - The cache has 4 lines and is direct-mapped [2].
   - The cache has 4 lines and is fully-associative[1].
   - The cache has 4 lines and is 2-way set-associative [2].
   - The cache has 4 lines and is 2-way skew-associative [3].

   (For this problem, you may either solve this mathematically or through simulation. In either case you need to show your work (or code).

2. Consider a 4KB direct-mapped cache backed-up by a 256KB 2-way associative cache. The L2 is *inclusive* of the L1. Say the L1 has a T_{hit} of 2 cycles, the L2 has a T_{hit} of 15 cycles, and the L2 has a T_{miss} of 120 cycles. Answer the following questions:
   a. What would be the average memory access time if the L1 has a hit rate of 90% and the L2 has a hit rate of 50%? Assume accesses are only sent to the L2 if they miss in the L1 [2].
   b. There is a proposal to add an L0 cache of 1KB. The L0 would have a 1 cycle access time and memory requests would only be passed on to the L1 if the L0 missed. The L1 would be inclusive of the L0 and accesses that hit in the L1 and/or L2 before would continue to do so. What hit-rate would be needed to get a tie with the original configuration? (Use the hit-rate numbers from part a as needed.) [3]

c. In part b we said that the L1 is only accessed if the L1 misses. Let's assume we didn't do that and instead accessed both the L1 and L0 in parallel. What would be the disadvantages of doing this (or opportunity costs, however you want to look at it) as compared to not having an L0 at all [3]?

3. Provide an example of when *bypassing*, that is not putting a line into the cache even though the line was accessed, could improve the hit rate of a cache [3].

4. 5.23ab on page 522 [5].

5. 5.3ab (L1 cache only) [3].