EECS 470 Homework 2

This assignment is worth a bit less than 2% of your grade in the class and is graded out of 30 points. Remember you may drop one homework assignment or quiz score.

1. Consider the following assembly instructions:

```
start:R1=MEM[R2+0]
      R2=MEM[R2+4]
      branch done if(R2==0)
      R3=R1+R3
      branch start
done: halt
```

   a. If all entries in the rename table currently point to the appropriate architected register, and if the next available physical register is P1 (then P2, P3, etc.) show how each assembly command executed will be translated if the above program branches to done after the 3rd time R2 is changed. You will need to "translate" many of the commands more than once… [3]
   b. Describe, using "C/C++" terms, what the above program seems to be doing (think structures and pointers…)[1].

2. A.7ab [2]
3. 1.1ab [3]
4. 2.4bc [4] (note an answer to a is in the back of the book.)
5. 3.1[6]

6. In standard written English, explain what conditions must be true in order for Tomasulo's I (the algorithm found in section 3.3) in order for the processor to do the following. (ie. what conditions would have to be true for these actions to be done?) [4]
   a. A given instruction has its registers renamed.
   b. A given instruction is sent to a reservation station.
   c. A given instruction is sent to its execution unit.
   d. A given instruction is allowed to leave its execution unit.

7. Consider the three types of data hazards, RAW, WAW, WAR. What portion of Tomasulo's I handles each data dependency? That is, what causes each type of dependency not to cause incorrect program behavior even though we are executing out of order? Relate your answers back to question 6. [4]

8. You are given a standard 5-stage pipeline which is also 2-way superscalar. Branches are resolved in the memory stage and predicted not-taken. 20% of the instructions are branches and 50% of those are not taken. Assume the *only* source of stalling (that is the only thing that prevents an IPC of 2) is branches. What would be the IPC of the processor? (hint, think about what it means for 2 instructions to be in the same stage at the same time with respect to program order!) Show and explain your work. [3]