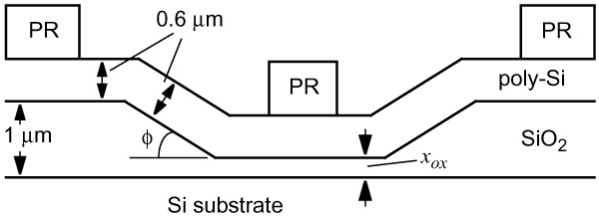
EECS 523 Homework#4

1- 0.6μm of polysilicon is conformally deposited on a wafer with topography as shown below. In etching the polysilicon (directional etch), it is required that all unmasked polysilicon be cleared without etching into the substrate. Assume that the polysilicon etching process has the following selectivities: polysilicon/SiO_2 = 8/1, polysilicon/photoresist = 2/1. Determine the maximum allowable step angle in ϕ the thin to thick oxide transition if the thin oxide thickness x_{ox} is 5nm or 40nm.



2- The following pages comprise an actual 2 μm p-well CMOS process flow with poly-to-poly capacitors (useful for non-digital applications, so we won't concern ourselves with it). No details are spared in this flow; even equipment names are given, as are diagnostic steps used to verify each step. LPCVD furnace program names are also given. These details are included to present a more realistic situation. In doing this problem, you must sift through the extraneous information and concentrate on the recipe information (i.e., temperatures, times, implant doses, etc....).

Answer the following questions based upon this process.

(a) Draw a qualitative cross-section corresponding to line A-A' in the layout (figure 1). Identify layers and try to draw their thickness to scale. (You should distinguish between CVD oxides and thermally grown oxides—i.e. label them.) Note that although capacitors are not used in this layout, you may need to account for the process steps involved with poly-to-poly capacitor formation to get a sufficiently accurate cross-section. (Note that mask layers are identified in the drawing below. '*df*' = dark field (i.e., box shows where an opening in the PR will be) and '*cf*' = clear field (i.e., box shows the portion to be covered by PR)

(b) What is the gate oxide thickness t_{ox}?

(c) What is the depth x_{jn} of the NMOS n^+ S/D junctions at the end of the process? (You will need to consider all the Dt products for each implant. Neglect any step at temp < 900^oC)

(d) What is the depth x_{jp} of the PMOS p^+ S/D junctions at the end of the process?

(e) What is the gate-overlap capacitance
   (i) For NMOS devices?
   (ii) For PMOS devices?

(f) What is the threshold voltage V_{thn} for the NMOS devices of this process for zero source-to-bulk voltage, V_{sb}=0? Assume that the fixed charge in the gate oxide is negligible. (Note that this may or may not be a good assumption. Don't be surprised if you get a strange value for V_{thn}.)

(g) What is the threshold voltage V_{thp} for the PMOS devices of this process for zero source-to-bulk voltage, V_{sb}=0? Assume that the fixed charge in the gate oxide is negligible. (Note that this may or may not be a good assumption. Don't be surprised if you get a strange value for V_{thp}.)

(h) Calculate $k_n'=\mu_n C_{ox}$ and $k_p'=\mu_p C_{ox}$ for this process.

(i) Assuming the p-well is tied to ground, what is the minimum value of voltage on a metal line over the field region in the p-well that would invert the p-well surface?

(j) Assuming the n-substrate is tied to V_{DD}=5V, what is the maximum value of voltage on a metal line over the field region in the n-substrate that would invert the n-substrate surface?

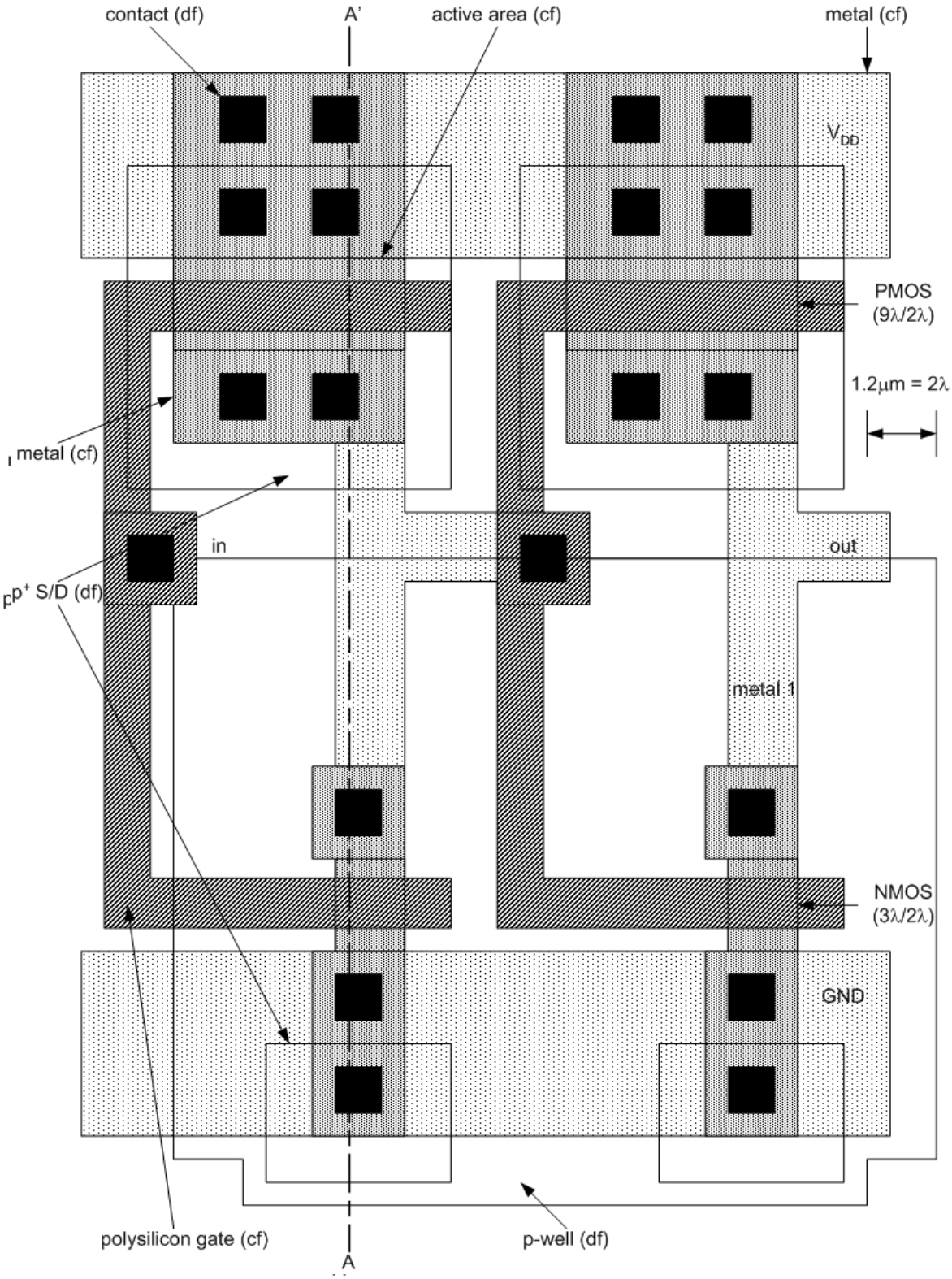

contact (df)
A'
active area (cf)
metal (cf)
V_{DD}
PMOS
(9λ/2λ)
1.2μm = 2λ
metal (cf)
in
out
p+ S/D (df)
metal 1
NMOS
(3λ/2λ)
GND
polysilicon gate (cf)
p-well (df)
A

Figure 1

CMOS Process

2 μm, P-well, double poly-Si, single metal

0.0 Starting wafers: 8-12 ohm-cm, n-type, <100>
Control wafers: PWELL (n-type), PCH (n-type) Scribe lot and wafer number on each wafer, including controls.
Measure bulk resistivity (ohm-cm) of PWELL on Sonogage.

1.0 Initial Oxidation: target = 1000(+/- 5%) A

1.1 TCA clean furnace tube (tylan2).

1.2 Standard clean wafers, include PWELL and PCH.
Stnd clean: piranha clean, DI rinse, BHF dip, spin-dry. Pls see process module in the lab manual)

1.3 Wet oxidation at 1000°C (SWETOXB):
5 min dry O_2
~9.5 min wet O_2
5 min dry O_2
20 min dry N_2
Measure t_{ox}=

2.0 Punch-Through Implant
Blanket implant: Phosphorus, 145 keV, 1.2E12/cm^2.
Include PWELL and PCH.

3.0 Well Photo Mask:
Control wafers are not included in any photoresist step.
(PWELL proceeds to Step 4.0, PCH to Step 5.4)

3.1 Standard clean wafers in sink8.
Dehydrate wafers in oven for >30 min. at 120°C.

3.2 Standard I-Line process:
Spin, expose, develop, inspect, descum, hard bake.
No etch. Resist is left on wafers.

4.0 Well Implant: Boron (B11), 3E12/cm^2, 80 keV.
Include PWELL.

5.0 Well Drive-In: target x_j = ** μm, t_{ox} = 3500 A

5.1 TCA clean furnace tube (tylan2).

5.2 Etch pattern into oxide in 5/1 BHF.
Strip oxide off of PWELL.

5.3 Remove PR in O_2 plasma. Piranha clean wfrs in sink8.

5.4 Stnd clean wfrs in sink6 include PWELL and PCH.

5.5 (a) Well drive at 1150°C (WELLDR):
4 hrs dry O_2
5 hrs dry N_2
(b) Measure oxide thickness on work wafer.
Measure two points on three wafers from different locations on the boat: front, middle and rear.
t_{ox}(well) = t_{ox}(outside of well) =
(c) Strip oxide and measure R_s on PWELL and PCH.
R_{sPWELL}= R_{sPCH}=

5.6 TCA clean the furnace tube after well drive-in is done.

6.0 Pad Oxidation/Nitride Deposition:
target = 300 A SiO_2 + 1000 A Si_3N_4

6.1 TCA clean furnace tube (tylan5). Reserve tylan9.

6.2 Etch oxide in 5/1 BHF until wafers dewet.

6.3 Standard clean wafers in sink6, include a T_{ox} monitoring wafer, PWELL and PCH.

6.4 Dry oxidation at 950°C (SGATEOX):
~1 hr. dry O_2
20 min dry N_2 anneal.
Measure T_{ox} on monitoring wafer. T_{ox}=

6.5 Deposit 1000 A of Si_3N_4 immediately (SNITC).
Include PWELL and PCH.
approx time = 23 min., temp.= 800°C.
Measure nitride thickness on 3 work wafers, using t_{ox} obtained in 6.4. PWELL and PCH proceed to Step 13.3.

7.0 Active Area Photo Mask:
Standard KTI process.
Offset: x = 3.2420, y = 0.6155.

8.0 Nitride Etch:
Plasma etch in lam1.
Measure T_{ox} on each work wafer. (1 pnt measurement).
Do not remove PR. Inspect.
Measure PR thickness covering active area. tpr=
PR must be >8 kA. Hard bake again for >2hrs at 120°C.

9.0 P-Field Photo Mask: (basically, the pwell mask)

9.1 Standard KTI process. (Second photo)
Inspect! Inside well, field is open and active areas are covered with Si_3N_4 and PR.

9.2 Measure PR thickness on active area with as200.
Wafers cannot be passed unless PR is >8 kA. tpr=

10.0 P-Field (Channel Stop) Ion implant: B11, 100 keV, 1E13/cm^2

11.0 N-Field Photo Mask: (inverse of the pwell mask)

11.1 Remove PR in O_2 plasma. Piranha clean wfrs in sink8.
Dehydrate wfrs in oven for >30 min. at 120°C.

11.2 Standard I-Line process.
Well area is covered with PR, active area with Si_3N_4.

12.0 N-Field (Channel Stop) Ion Implant: Phosphorus, 40 keV, 5E12/cm^2.

13.0 Locos Oxidation: target = ** A

13.1 TCA clean furnace tube (tylan2).

13.2 Remove PR in O_2 plasma. Piranha clean wfrs in sink8.

13.3 Stnd clean wfrs in sink6 include PWELL and PCH.
Dip in 10/1 BHF until field area dewets.

13.4 Wet oxidation at 950°C (SWETOXB):
5 min dry O_2
4 hrs 40 min wet O_2
5 min dry O_2
20 min N2 anneal
Measure T_{ox} on 3 work wfrs. T_{ox}=

14.0 Nitride Removal

14.1 Dip in 5/1 BHF for 30 sec., include PWELL and PCH. (To remove thin oxide on top of the nitride)

14.2 Etch nitride off in phosphoric acid at 145°C.

15.0 Sacrificial Oxide: target = 200 (+/- 20) A

15.1 TCA clean furnace tube (tylan5).

15.2 Stnd clean wfrs in sink6, include PWELL and PCH.
Dip in 10:1 BHF until PWELL and PCH dewet.

15.3 Dry oxidation at 950°C (SGATEOX):
30 min dry O_2
20 min N_2 anneal
Measure T_{ox} on 3 wfrs. T_{ox}=

16.0 Threshold Implant:
Blanket implant: B11, 30 keV. Doses (/cm^2): 9E11.

17.0 Gate Oxidation/Poly-Si Deposition:

17.1 TCA clean furnace tube (tylan5); reserve tylan11.

17.2 Stnd clean wfrs, include PWELL, PCH and, 3 T_{ox} and 1 Tpoly1 monitoring wafers.

17.3 Dip off sacrificial oxide in 10/1 H2O/HF until PWELL and PCH dewet (approx. 1 min).

17.4 Dry oxidation at 950°C (SGATEOX):
2 hr. dry O_2
20 min N_2 anneal.
Measure 5 pnts on each of 3 T_{ox} monitoring wfrs. T_{ox}=

17.5 Immediately after oxidation deposit 4500 A phos doped poly-Si (SDOPOLYH).
approx.time = 2 hr. 40 min., temp.= 610°C
Include Tpoly1, PWELL and PCH.
Tpoly1= Measure 5 pnts.
PWELL and PCH proceed to Step 20.2.

18.0 Gate Definition Mask:
Standard I-Line process.

19.0 Plasma etch poly-Si

19.1 Etch poly in Lam4. (CCl4/He/O2 at 300 W, 280 mT)

19.2 Measure T_{ox} in S/D area of each work wafer.

19.3 Remove PR in plasma O_2. Piranha clean wfrs in sink8.
Measure line width of 2 um gates on each work wafer.
One pnt measurement in 19.2 and 19.3.

20.0 Capacitor formation:
Target = ** A SiO_2 on 1st poly + 4500 A 2nd poly

20.1 TCA clean furnace tube (tylan2). Reserve tylan11.

20.2 Standard clean wafers, include PWELL,PCH, Tpoly1 and one of gate oxidation monitoring wafers as a 2nd poly monitoring wafer, Tpoly2.
Tpoly2 proceeds to Step 20.4.
From here on: only 10 sec dip in 25/1 H2O/HF after piranha.

20.3 Dry oxidation at 950°C (SDRYOXB):
55 min dry O_2
20 min N_2 anneal.
Measure oxide thickness on poly with nanometrix
tox(PWELL) = tox(PCH) =
PWELL proceeds to Step 24. PCH proceeds to Step 25.

20.4 Second poly-Si deposition: immediately after oxidation deposit 4500 A of phosphorus doped poly-Si (SDOPOLYH):
approx time = 2 hr 30 min, temp.= 610°C. Tpoly2=

21.0 Capacitor Photo Mask:
Standard I-Line process.

22.0 Plasma etch poly-Si:

22.1 Etch 2nd poly in Lam4. Inspect.

22.2 Measure T_{ox} in S/D area on each work wafer.

22.3 Remove PR in O_2 plasma. Piranha clean wfrs in sink8.
Dehydrate wfrs in oven for > 30 min. at 120°C.

22.4 Measure channel length on nanoline. This measurement can be done at any step before Step 28.

23.0 N^+ S/D Photo Mask: (inverse of p^+ S/D)
Stnd I-Line process. Do not hard bake.
Inspect. PMOS areas are PR covered. Capacitor areas are not.

24.0 N^+ S/D Implant: Arsenic, 160 keV, 5E15/cm^2, incl. PWELL.

25.0 N^+ S/D Anneal

25.1 TCA clean furnace tube (tylan7).

25.2 Remove PR in O_2 plasma and piranha clean wafers in sink8 (no dip here).

25.3 Standard clean wafers in sink6, incl. PWELL and PCH.

25.4 Anneal in N_2 at 925°C for 1 hr 15 min (N_2ANNEAL).

26.0 P^+ S/D Photo Mask:
Stnd I-Line process.
All areas are covered with PR except PMOS areas.

27.0 P+ S/D Implant: B11 at 30 keV, 5E15/cm^2, include PCH.

28.0 PSG Deposition and Densification: target = 7000 (+/- 200) A

28.1 Remove PR in O_2 plasma and piranha clean wafers in sink8 (no dip).

28.2 Stnd clean wfrs in sink6 (10 sec dip)
Include PWELL, PCH and one PSG monitoring wafer.

28.3 Deposit 7000 A PSG, PH_3 flow at 10.3 sccm (SDOLTOD).
approx.time = 35 min. (check current dep. rate)
temp. = 450°C

28.4 Densify glass in tylan2 at 950°C, immediately after PSG deposition (PSGDENS). Include PSG control.
5 min dry O_2, 20 min wet O_2, 5 min dry O_2.
Measure tPSG=
Etch oxide on PWELL and PCH, and measure poly sheet resistivity on PWELL and PCH with prometrix.

28.5 Do wet oxidation dummy run afterwards to clean tube:
1 hr wet oxidation at 950°C (SWETOXB).

29.0 Contact Photo Mask:
Stnd I-Line process.

30.0 Contact Etch:
Plasma etch in Lam2. CHF_3/CF_4/He, ~800 watts.

31.0 Back side etch:

31.1 Remove PR in O_2 plasma, piranha clean wfrs in sink8 (no dip).
Dehydrate wafers in oven at 120°C for >30 min.
