EECS 523 Homework #9

1. Let the delay of a single inverter be modeled by the following equation

$$\tau \propto \frac{C\sqrt{L}\sqrt{t_{ox}}}{V_{DD}{}^{0.3}\left(0.9-\frac{V_t}{V_{DD}}\right)^{1.3}}$$

Let

$$\frac{V_{DD}}{5} < V_t < \frac{V_{DD}}{4}$$

$$L_{\min} > 4l$$

$$C = 0.36 \times L + \frac{1.5\times 10^{-3} L}{t_{ox}} \text{ where C in pF, } t_{ox} \text{ in } \mu\text{m, L in } \mu\text{m}$$

$$E_{ox} = \frac{V_{DD} - 0.2}{t_{ox}} < 6\frac{MV}{cm}$$

$$x_{j\min} = 0.05\mu m$$

   (a) If a current technology has V_{DD} = 1.8V, V_T = 0.4V, t_{ox} = 4nm, x_j = 0.1 μm and a single stage delay of 50ps, find the best delay for a scaled technology with V_{DD} =1V.
   (b) The E_{OX} constraint contains a (V_{DD} – 0.2) term. What does this 0.2V refer to? If $\varphi_{ms} + \psi_s$ is very small.
   (c) What is the minimum allowable poly-gate doping (N_{GATE}) based on the above information?

2. Let I_{DSAT} be the drive current when $V_{GS} = V_{DS} = V_{DD}$. A current technology has these parameters:
   V_{DD} = 1.8V, L_{eff} = 0.13 μm, x_j = 0.06 μm, t_{ox} = 4nm, V_T = 0.4V, $N_{SUB} = 4 \times 10^{17}$ cm^{-3}, α = 0
   (a) Focusing on PMOS, calculate I_{DSAT} normalized to device width for this technology and a scaled version of it with S = 2. Use constant-field scaling and short channel MOS I-V models. Assume $\nu_{SAT} = 8 \times 10^6$ cm/s.
   (b) Find the subthreshold swing for both the current and scaled technologies. Estimate the increase in I_{OFF} (subthreshold current at V_{GS} = 0 per unit width) exhibited by the scaled device relative to one of the original technology. Assume the current for each technology at $V_{GS} = V_T$ is of the same ratio as the I_{DSAT}'s.