EECS 523 Final Exam

Name :

ID #

INSTRUCTIONS

Read all of the instructions before beginning the exam.

You have a total of 120 minutes to finish this exam.

This is an open-book, open-notes exam.

Unless otherwise noted on a particular problem, you must show your work (in the space provided plus the back of the pages) for all problems to receive full credit; simply providing answers will result in only partial credit, even if the answers are correct. If you require extra space beyond what is provided, be sure to turn in any material that is required to support your solutions.

Turn in the entire exam, including this cover sheet.

Put your name on any additional material that you submit.

1- (3points) Which one of the following reasons is most responsible for the reduction of oxidation rate of silicon at higher oxide thickness?

   a) Lack of enough oxygen atoms in the furnace.
   b) Diffusion of oxygen through silicon wafer.
   c) Oxidation becomes reaction rate limited.
   d) Diffusion of oxygen through the oxide.

2- (3points) In a MOSFET device with a fixed channel length and channel doping concentration, how can DIBL be further reduced using t_{ox} and x_j?

   a) Reduce t_{ox} and x_j .
   b) Reduce t_{ox} and increase x_j .
   c) Increase t_{ox} and x_j .
   d) Increase t_{ox} and reduce x_j .

3- (3points) Name four methods to suppress or eliminate Latch-up in CMOS structures.

1)
2)
3)
4)

4- (3points) Which one of the following MOS devices exhibits Kink-effect?

a) Bulk CMOS with one well.
b) Twin tub CMOS structure.
c) Partially depleted MOS/SOI.
d) Fully depleted MOS/SOI.

5- (3points) Which one of the following leakage currents determines the minimum gate oxide thickness?
a) Hot carrier gate current.
b) Subthreshold current.
c) Direct tunneling current.
d) Fowler-Nordheim tunneling current.

6- (6points) According to the effect of drain and source series resistances on drain current, which of the following configuration is more suitable for LDD structures? Give good reasons for your selection:
a) Having the low-doped regions on both sides near the source and drain.
b) Having the low-doped region just near the source.
c) Having the low-doped region just near the drain.

7- (3points) Which of the following fabrication process is to suppress subsurface DIBL or punchthrough current?
a) Double diffused drain or so called DDD.
b) Halo implantation near drain side.
c) Growing sidewall spacer.
d) Increasing source/drain doping concentration.

8- The following parameters are given for a metal gate NMOS transistor. φ_{ms} = - 0.85, t_{OX} = 4nm, x_j = 0.08μm, α = 0, V_T = 0.4V, L_{eff} = 100nm, ν_{SAT} = 10^7 cm/s, μ_0 = 670 cm^2/v-sec, Na = 5×10^{17} cm^{-3} , $\varepsilon_{OX} = \varepsilon_0\ \varepsilon_r$ = 35×10^{-14} F/cm, ε_{si} =10^{-12} F/cm, V_{DD} = 2V. Also, ν = 1.6, E_0= 0.67 Mv/cm (used in mobility equation), A_i =2×10^6 /cm, B_i =1.7 MV/cm, T= 300°K and n_i = 1.5×10^{10} cm^{-3}. Use these parameters in the following problems as required.

A - (10points) Find the Ideality factor K_I for this transistor if V_{GS} = 2V

B – (3points) Using the result in (A), is it beneficial to further shrink the device length?

C – (10points) Compute the drain current per unit width of the device with V_{GS} = V_{DS} = V_{DD} = 2V (use iteration to find V_{DSAT} if required, of course you don't need to iterate more than twice).

D – (6points) What is the DC lifetime of the device under these conditions?

E - (6points) To increase the DC lifetime calculated above to 20 years, how much LDD region should be added to this structure?

F - (5points) If the given V_T is measured at I_D = 0.1μA, what is the amount of off-current of this device?

G – (5points) Considering Rs = R_D = 100 Ω for the above MOS transistor with a channel width of W= 2μm, find the amount of degradation in the device drain current calculated in part (C) due to these series resistances.

H - (8points) If the device is scaled down by S=1.4 using constant field scaling method, how much does it change the DC lifetime of the device? Consider the same structure but without the LDD region.

I - (6points) what is the effect of this scaling on the off-current of the device? Use the condition given in question (F).

9- We want to redesign and fabricate the above MOS transistor with an N-type poly gate (keeping all the dimensions and substrate doping the same). If the measured threshold voltage excluding the voltage drop in the poly is $V_T = 0.3$ V, find:

a) (7points) The amount of doping concentration in poly.

b) (10points) The real threshold voltage of this device if we consider the voltage drop inside the poly.