EECS 523 Exam #1

Name :

INSTRUCTIONS

Read all of the instructions before beginning the exam.

You have a total of 60 minutes to finish this exam.

This is an open-book, open-notes exam.

Unless otherwise noted on a particular problem, you must show your work (in the space provided plus the back of the pages) for all problems to receive full credit; simply providing answers will result in only partial credit, even if the answers are correct. If you require extra space beyond what is provided, be sure to turn in any material that is required to support your solutions.

Turn in the entire exam, including this cover sheet.

Put your name on any additional material that you submit.

No.	1	2	3	4	5	6	7	8	9
Grades	10	5	5	10	8	12	15	20	15

1- Write the equations for all the power consumptions in a **CMOS** circuitry, when is driven by a sharp rising and falling high frequency square wave signal.

2- For the following reason, silicon is added to aluminum prior to deposition on silicon surface.
   a) To eliminate the problem of its evaporation.
   b) To prevent aluminum spiking.
   c) To enhance its sputtering capability.
   d) In order to form a better silicide.

3- Which one of the following statement is most suited to **PECVD** reactor?
   a) The deposited film has good quality.
   b) Low temperature deposition of high quality Silicon Nitride and Silicon Oxide with the help of plasma.
   c) It is the preferred process for the deposition of polysilicon.
   d) Low temperature growth is the benefit of using this system of deposition.

4- How do you compare Evaporator, Sputtering and CVD systems from conformity of the deposited layer viewpoint? Give very brief reasons for your answer.

5- In which one of the following lithography system, the size of the transferred images from mask to wafer is more sensitive to temperature? Give a reason for your selection.
   a) Contact printing
   b) Proximity printing
   c) Projection printing

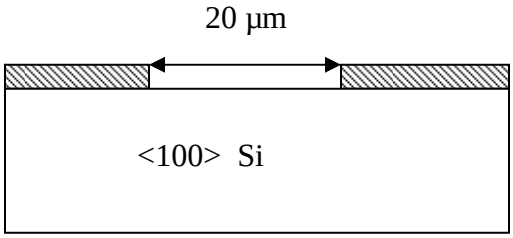
6- A boron implantation has been carried out on bare silicon with 10 keV energy. What is the actual dose in silicon? Draw the expected impurity distribution and write the necessary formulas (no numerical result is needed). What is the common problem of directly implanting impurities in silicon? (Just give the name with very little description).

7- High-energy oxygen atoms are implanted in silicon in order to form a buried layer of silicon dioxide. If the desired SiO_2 layer is 0.25μm thick, what is the required oxygen dose to be implanted in silicon?

8- A 20μm square window is etched in 100nm thick oxide over <100> silicon as shown below. The wafer is then etched in KOH silicon etchant for 10 minutes with a rate of 1μm/min. Answer the following questions:

a) Draw the cross- section view of the wafer after etching.

b) The wafer is then oxidized in dry O2 at 1100°c for 60 minutes, what is the thickness of the oxide on different parts of the silicon surface including the etched surfaces? Use the given oxidation graphs to determine the oxidation thickness.



9- A .5μm thin poly has been implanted with both phosphorus and boron impurities with a dose of 5×10^{15} cm^{-2} and 3×10^{15} cm^{-2} respectively. Suppose the wafer has been annealed for enough time that a uniform spreading of impurities is achieved in the poly layer. Assuming that none of the impurities has the chance to escape from the poly, what are the net electron and hole concentrations in the poly? Is the poly P, N or a mixture of P and N type semiconductor?