

EECS 523: Homework #6

- 1- Given the following, $L_{\text{drawn}} = 130\text{nm}$, $L_D = 25\text{nm}$, $t_{\text{ox}} = 23\text{\AA}$, $V_{DD} = 1.2\text{V}$, $V_{\text{th}} = 0.25\text{V}$, $N_{\text{SUB}} = 1 \times 10^{17} \text{cm}^{-3}$ and $\mu_n = 730 \text{cm}^2/\text{V}\cdot\text{sec}$.

a) Plot I_D vs. V_D of the device for $V_{GS} = V_{DD}$ and $V_{SB} = 0\text{V}$ use the long channel model including channel shortening effect. Normalize I_D to device width (Use MATLAB or Excel).

b) I_D ($V_{DS}=V_{GS}=V_{DD}$) has been empirically determined to be $650\mu\text{A}/\mu\text{m}$. By what factor does the simple square law theory overestimate the current drive?

- 2- Find the temperature dependency of V_T and S_t (First include all the temperature dependent terms and then you can neglect the less important terms in order to simplify the final results). Ignore the temperature dependency of the flat band voltage.

For $t_{\text{ox}} = 10\text{nm}$, $N = 5 \times 10^{17} \text{cm}^{-3}$, find V_T and S_t for $T = 300^\circ\text{K}$, 373°K . Assume NMOS with N^+ Poly gate.

- 3- To see the effect of DIBL:

a) Derive equation (1) in the article handed out in the class.

b) Using equation 2 in the paper and the following parameters, plot V_s vs y for:

i) $L = 0.2 \mu\text{m}$, $V_d = 2.75 \text{V}$.

ii) $L = 1 \mu\text{m}$, $V_d = 2.75 \text{V}$.

Assume NMOS with N^+ Poly gate, $V_g = 0.4\text{V}$, $t_{\text{ox}} = 10\text{nm}$, $\eta = 1$, $N_a = 5 \times 10^{17}$.