Project Ideas - EECS 627

Projects can be combined to make more comprehensive designs. For example, a low power Microcontroller project could be combined with an MPEG decoder project to form a larger more interesting design. Preferred team size if 2 - 4 students. Smaller or larger team sizes are allowed based on project size.

IP-Blocks:

- Encryption chip for the Advanced Encryption Standard (Rijndael algorithm) with self-test upon power-up

- Public key encryption using Montgomery or Galois Field multiplier

- IP Packet Forwarding Engine (with possibly with Encryption / Decryption)

- USB (Universal Serial Bus) Function Controller for a Microcontroller (e.g. ARM, MIPS, etc.)

- PCI Controller for a Microcontroller

- Ethernet Controller for packet transmission/reception and encapsulation / de capsulation

- Viterbi decoder

- Turbo coders

- Game or graphics coprocessor for rendering acceleration

- Arithmetic co-processor implementing complex numerical algorithms

- MPEG compression / decompression

- JPEG encoder / decoder

- DSP core with multiple MAC units and VLIW instructions

- Application specific processors with ISAs specifically designed for efficient execution of compression or encryption algorithms

- Based band digital signal processing, such as JPS or Bluetooth

Analog:

- CDMA encoder / decoder (analog)

- PLL

- DLL

- Switch Cap / DAC / ADC

- VCO

- Low voltage analog design

Custom Design / Technology Studies:

- Simplified MIPS/ARM ISA processor with dynamic power management techniques

- Trade-off study of different dynamic power management methods for data path

- Low power (static and dynamic) cache design (with dynamic or static Vt / Vdd scaling)

- Multi-Vdd Microcontroller design with voltage converters

- Dual-Vt / DTCMOS Microcontroller design for high performance / low leakage power

- Microcontroller with dynamic voltage and frequency scaling

- Asynchronous micro controller datapath

- GALS (globally asynchronous / locally synchronous) SOC or processor design

- Adiabatic datapath design

- High speed arithmetic coprocessor or datapath using advanced logic family such as SR-Domino or CPL logic

- New clocking schemes (such as rotary clocks)

- Library design issues (large libraries vs. small etc.)

- Timing flow and timing closure issues

Something different:

- Image sensor array with image processor

- MEMS

- Reconfigurable computing