EECS 627, Lab Assignment 3

1 Introduction

In this lab assignment, you will use *Cadence ICFB* and *Calibre* to become familiar with the process of DRC/LVS checks on a design. So far, you have placed-routed the blocks and done the global assembly of a small chip. The next step is to perform the design rule checks and verifying that the layout generated by silicon ensemble actually matches the Verilog file. Because of the oncoming design review-I in two weeks, this lab has been kept simple and you will perform DRC/LVS on only the multiplier block of your design.

2 ICFB and Calibre setup

You will have to perform   steps in order to setup your environment for Candence-ICFB and Mentor-Calibre

3 Steps for performing DRC/LVS

You need to import the mult.def generated by silicon ensemble to create a layout view of multiplier in ICFB. There are 4 cell-views in ICFB: abstract, layout, schematic and symbol. .def file corresponds to the abstract view. So it needs to be converted to the layout view and a .gds2 of the layout has to be generated through ICFB.

You have to perform the following steps in the following order to create a layout view and export the gds2 file from ICFB

- icfb &

- A command window will open. Type the following in the command window:

  load "CALIBRE/calibre.skl"

  This is necessary to interface calibre and ICFB

- Import the def file mult.def using the following options in GUI:

  File -> Import -> def

     Library Name: tsmc18

     Cell Name : mult

     View Name : abstract

     DEF File Name : mult.def

A new window with abstract of multiplier will be created. If you have not reached so far, there is something wrong in your setup. Now save the abstract:

   Design -> SaveAs -> tsmc18

      Cell Name: mult

      View Name: abstract

- Now the layout view has to be generated from the abstract view. For that first we will select all the polygons and instantiations in the abstract view and then replace them with their layout view. Perform the following steps:

   Edit -> search

   A new window will open. Perform the following tasks in the new window:

      add criteria -> change cell name to view name= abstract

      apply (this will select everything)

      select all

      replace view name = layout

      Replace all

   You have successfully generated the layout view. Now save the design as follows:

   design -> save as -> layout

- Now the generated layout has to be flattened. Do File -> open in the ICFB command window. A new window will open. Change Library to tsmc18. You should see your mult block there with both its abstract and layout views. Open the layout view and perform the following operation to flatten the design

   Edit -> search

   A new window will open. Perform the following tasks in the new window:

      add criteria -> change cell name to view name = layout

      apply (this will select everything)

      select all

   Edit -> Heirarchy -> Flatten

      preserve pins

   Again save the layout using design -> save as -> layout

- Generate gds2 for mult: In the main command window,

   File -> export -> stream

      library name : tsmc18

      top cell name : mult

      view name : layout

      output file : mult.calibre.gds

      User defined data : (This opens a new window)

         Layer Map Table: opus.map

   The log file for export is PIPO.LOG.

- Run RVE from ICFB: RVE is the Calibre interface. You will see "Calibre" as the right most menu. Click on Calibre -> Run RVE

3.1 DRC

   calibre -gui & (on shell prompt)

   DRC

      Runset File Path -> New Runset

      rules -> generic018.drc

      Inputs -> flat, layout -> mult.calibre.gds (should be green in color)

      primary cell -> mult

   Run DRC

DRC RVE

   Z -> zoom to highlights

3.2 LVS

- Generate schematic from APR verilog output using the following command in shell prompt:

  v2lvs -v mult_APR.v -o mult.cdl -s /usr/caen/generic/artisan/tsmc18/aci/sc/lvs_netlist/tsmc18.cdl -s0 Vss -s1 Vdd

- Click on LVS on the main Calibre window:

  LVS

     rules -> generic018.lvs

     inputs -> flat, layout vs netlist, layout name, netlist name, Primary cell

     report -> mult.lvs.report

     setup -> lvs options ->

              Supply: Unclick Abort Lvs on power/ground net errors

                  Power: VDD

                  Gnd: VSS

            ERC: Unclick run ERC

     Run LVS

  All the errors will be shown in transcript window. In case of no errors, you will see the well-know smiley of Mentor. Congratulations! you have become familiar with all the major tools you will be using in your project.

4 Deliverables

  Include only the following files in your tar-ball:

- README.txt : Any problems encountered and their solution (if solved)
- mult.drc.report
- mult.lvs.report