

Al Fazio

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Patents

- » 5,065,364, Apparatus for Providing Block Erasing in a Flash EPROM, 11/12/1991
- » 5,239,505, Floating Gate Non-Volatile Memory with Blocks and Memory Refresh, 8/24/1993
- » 5,245,570, Floating Gate Non-Volatile Memory with Blocks and Select Transistors, 9/14/1993
- » 5,402,370, Circuitry and Method for Selecting a Drain Programming Voltage for a Nonvolatile Memory, 3/28/1995
- » 5,440,505, Method and Circuitry for Storing Discrete Amounts of Charge in a Single Memory Element, 8/8/1995
- » 5,442,586, Method and Apparatus for Controlling the Output Current Provided by a Charge Pump Circuit, 8/15/1995
- » 5,455,794, Method and Apparatus for Controlling the Output Current Provided By a Charge Pump Circuit, 10/3/1995
- » 5,475,693, Error Management Processes for Flash EEPROM Memory Arrays, 12/12/1995
- » 5,497,119, High Precision Voltage Regulation Circuit for Programming Multilevel Flash Memory, 3/5/1996
- » 5,508,958, Method and Apparatus for Sensing the State of Floating Gate Memory Cells by Applying a Variable Gate Voltage, 8/16/1996
- » 5,523,972, Method and Apparatus for Verifying the Programming of Multi-Level Flash EPROM Memory, 6/4/1996
- » 5,546,042, High Precision Voltage Regulation Circuit for Programming Multilevel Flash Memory, 8/13/1996
- » 5,566,125, Method and Circuitry for Storing Discrete Amounts of Charge in a Single Memory Element, 10/15/1996
- » 5,677,869, Programming Flash Memories Using Strict Ordering of States, 10/14/1997
- » 5,701,266, Programming Flash Memories Using Distributed Learning Methods, 12/23/1997
- » 5,729,489, Programming Flash Memory Using Predictive Learning Methods, 3/17/1998
- » 5,737,265, Programming Flash Memory Using Data Stream Analysis, 4/7/1998
- » 5,742,543, Flash Memory Device Having a Page Mode of Operation, 4/21/1998

- » 5,748,546, Sensing Scheme for Flash Memory with Multilevel Cell, 5/5/1998
- » 5,801,991, Deselected Wordline that Float During MLC Programming of a Flash Memory, 9/1/1998
- » 5,828,616, Sensing Scheme for Flash Memory with Multilevel Cell, 10/27/1998
- » 5,892,710, Method and Circuitry for Storing Discrete Amounts of Charge in a Single Memory Element, 4/6/1999
- » 6,091,618, Method and Circuitry for Storing Discrete Amounts of Charge in a Single Memory Element, 7/11/2000
- » 6,518,618, Integrated Memory Cell and Method of Fabrication, 2/11/2003

Publications/Speakerships

- » Mielke, N., Fazio, A.; "Reliability Comparison of FLOTOX and Textured Polysilicon E2PROMs", IEEE International Reliability Physics Symposium, 1987
- » Woo, B.J., Ong, T.C., Fazio, A., Park, C., Atwood, G., Holler, M., Tam, S.; Lai; "A Novel Memory Cell Using Flash Array Contactless EPROM (FACE) technology", Electron Devices Meeting, Technical Digest, International, pp. 91-94, 1990
- » Ong, T.C., Fazio, A., Mielke, N., Pan, S., Righos, N., Atwood, G., Lai, S.; "Erratic Erase in ETOXTM Flash Memory Array", VLSI Technology, Digest of Technical Papers, Symposium on , pp. 83 - 84, 1993
- » Bauer, M., Alexis, R.; Atwood, G.; Baltar, B.; Fazio, A.; Frary, K.; Hensel, M.; Ishac, M.; Javanifard, J.; Landgraf, M.; Leak, D.; Loe, K.; Mills, D.; Ruby, P.; Rozman, R.; Sweha, S.; Talreja, S.; Wojciechowski, K.; "A Multilevel-Cell 32Mb Flash Memory," Technical Digest IEEE International Solid State Circuits Conference, 1995, pp. 132,133.
- » Atwood, G.; Fazio, A.; Mills, D.; Reaves, B.; "Intel StrataFlash® Memory Technology Overview", Intel technology Journal, Q4 1997
- » Fazio, A.; Bauer, M.; "Intel StrataFlash® Memory Technology Development and Implementation", Intel technology Journal, Q4 1997
- » Fazio, A., "A High Density High Performance 180 nm Generation Etox™ Flash Memory Technology", Electron Devices Meeting, Technical Digest. International, pp. 267 - 270, 1999
- » Bauer, M.; Alexis, R.; Atwood, G.; Baltar, B.; Fazio, A.; Frary, K.; Hensel, M.; Ishac, M.; Javanifard, J.; Landgraf, M.; Leak, D.; Loe, K.; Mills, D.; Ruby, P.; Rozman, R.; Sweha, S.; Talreja, S.; Wojciechowski, K.; "A Multilevel-Cell 32 Mb Flash Memory", Multiple-Valued Logic, 2000. (ISMVL 2000) Proceedings. 30th IEEE International Symposium on, pp.367-368, 2000
- » Member of a Panel at the IEEE International Solid State Circuits Conference - "How Will Future Portable Systems Store and Access Data" - February 2001.
- » Fazio, A.; Keeney, S.; Lai, S. "ETOXTM Flash Memory Technology: Scaling and Integration Challenges" Intel Technology Journal, Volume 6, Issue 2, May 2002.
- » Franca-Neto, L.M.; Pardy, P.; Ly, M.P.; Rangel, R.; Suthar, S.; Syed, T.; Bloechel, B.; Lee, S.; Burnett, C.; Cho, D.; Kau, D.; Fazio, A.; Soumyanath, K.; "Enabling High-Performance Mixed-Signal System-on-a-Chip (SoC) in High Performance Logic CMOS Technology", VLSI Circuits Digest of Technical Papers, Symposium on, pp. 164-167, 2002
- » Member of a Panel at the IEEE International Electron Devices Meeting - "Embedded Memories for SoC - What Makes Sense?" - December 2002.
- » Fazio, A; "0.13um Logic+Flash: Technology and Applications", IEEE Non-Volatile Semiconductor Memory Workshop (NVSMW), 2003
- » Electron Device Society, Santa Clara Chapter, Symposium on Memories; "130nm Flash+Logic Technology", 2003

- » Member of a Panel at the Symposium on VLSI Circuits - "What is the Vision of Unified Custom Memory? Main or Niche" - June 2003.
- » Fazio, A; "A 130nm Flash+Logic+Analog Modular Technology", International Symposium on VLSI Technology, Systems, and Applications, pp. 60-63, 2003
- » UC Berkeley Solid State Seminar; "Flash Memory Technology: Integration, Multi-Level-Cell and Scaling", 2003
- » Fazio, A; "Flash Memory Scaling", Material Research Society Bulletin, Vol. 29, No. 11, November 2004
- » Member of a Panel at the Semiconductor Research Corporation (SRC) Forum on NVM Memories - November 2004.
- » Fazio, A.; "Future Direction of Non-Volatile Memory Technologies", Material Research Society Fall Meeting, Symposium D.1, December 2004

Professional Affiliations

- » Financial Chairman, IEEE Non-Volatile Semiconductor Memory Workshop, 1995
- » Technical Chairman, IEEE Non-Volatile Semiconductor Memory Workshop, 1997
- » General Chairman, IEEE Non-Volatile Semiconductor Memory Workshop, 1998