Gregory F. Taylor
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Patents

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- 7,501,845, On-chip frequency degradation compensation, 3/10/2009 (with Ravisangar Muniandy and Payman Aminzadeh)
- 7,471,102, Measuring threshold voltage of transistors in a circuit, 12/30/2008 (with Atul Maheshwari)
- 7,417,459, On-die offset reference circuit block, 8/26/2008 (with Timothy M Wilson and Songmin Kim)
- 7,394,274, On-chip frequency degradation compensation, 7/1/2008 (with Ravisangar Muniandy and Payman Aminzadeh)
- 7,348,790, AC testing of leakage current in integrated circuits using RC time constant, 3/25/2008 (with Tawfik R. Arabi, Srirama Pedarla, Patrick Elwer, and Dan Murray)
- 7,282,937, On-chip frequency degradation compensation, 7/1/2008 (with Ravisangar Muniandy and Payman Aminzadeh)
- 7,242,261, Voltage control for clock generating circuit, 7/10/2007 (with Keng L. Wong; Hong-Piao Ma)
- 7,233,162, Arrangements having IC voltage and thermal resistance designated on a per IC basis, 6/19/2007 (with Tawfik Arabi, Hung-Piao Ma, Gregory M. Iovino, Shai Rotem, and Avner Kornfeld)
- 7,199,624, Phase locked loop system capable of deskewing, 4/3/2007 (with Keng L Wong and Chee How Lim)
- 7,157,924, Method and apparatus for on die voltage fluctuation detection, 1/2/2007 (with Ali Muhtaroglu, Kent Callahan, and Tawfik Arabi)
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- 7,049,865, Power-on detect circuit for use with multiple voltage domains, 5/23/2006 (with Rachael J Parker, Mark L Neidengard, and Patrick J Ott)

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- 6,985,041, Clock generating circuit and method, 1/10/2006 (with Keng L. Wong, Niraj Bindal, Hong-Piao Ma, George Geannopoulos, and Edward A. Burton)
- 6,967,496, AC testing of leakage current in integrated circuits using RC time constant, 11/22/2005 (with Tawfik R. Arabi, Srirama Pedarla, Patrick Elwer, and Dan Murray)
- 6,924,710, Voltage ID Based Frequency Control for Clock Generating Circuit, 8/2/2005 (with Keng L. Wong, Hong-Piao Ma, Chee How Lim, Robert Greiner, Edward A. Burton, and Douglas R. Huard)
- 6,885,231, Variable delay element for use in delay tuning of integrated circuits, 4/26/2005 (with Ravishankar Kuppuswamy)
- 6,874,083, Method and apparatus to ensure proper voltage and frequency configuration signals are defined before applying power to processor, 3/29/2005 (with Ananda Sarangi, Rachael Jade Parker, and Edward P. Osburn)
- 6,809,606, Voltage ID based frequency control for clock generating circuit, 10/26/2004 (with Keng L. Wong, Hong-Piao Ma, Chee How Lim, Robert Greiner, Edward A. Burton, and Douglas R. Huard)
- 6,792,489, Multistage configuration and power setting, 9/14/2004 (with Edward P. Osburn and Ananda Sarangi)
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- 6,771,134, Frequency control for clock generating circuit, 8/3/2004 (with Keng L. Wong, Hong-Piao Ma, Chee How Lim, and Edward A. Burton)
- 6,747,470, Method and apparatus for on die voltage fluctuation detection, 6/8/2004 (with Ali Muhtaroglu, Kent Callahan, and Tawfik Arabi)
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- 6,727,597, Integrated circuit device having C4 and wire bond connections, 4/27/2004 (with George L. Geannopoulos)
- 6,717,455, Apparatus and Method to Use a Single Reference Component in a Master-Slave Configuration for Multiple Circuit Compensation, 4/6/2004 (with Usman A. Mughal, Razi Uddin, Chee How Lim, and Songmin Kim)
- 6,691,241, Delay tuning to improve timing in multi-load systems, 2/10/2004
- 6,671,847, I/O Device Testing Method and Apparatus, 12/30/2003 (with Chi-Yeu Chao, Tawfik R. Arabi, and Thomas D. Barrett)

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- 6,584,591, Timing control for input/output testability, 6/24/2003
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- 6,157,206, On-chip termination, 12/5/2000 (with Jack A. Price, and Chee How Lim)
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- 6,075,285, Semiconductor package substrate with power die, 6/13/2000 (with George L. Geannopoulos and Larry E. Mosley)
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