CMOS Transistor Scaling Past 32nm and Implications on Variation

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Intel Corporation

AGENDA

I. Overview – variation sources
II. Next generation variation – lithography
III. Next generation variation – polish
IV. Next generation devices
V. Measurements, results and interpretation
VI. Closing thoughts

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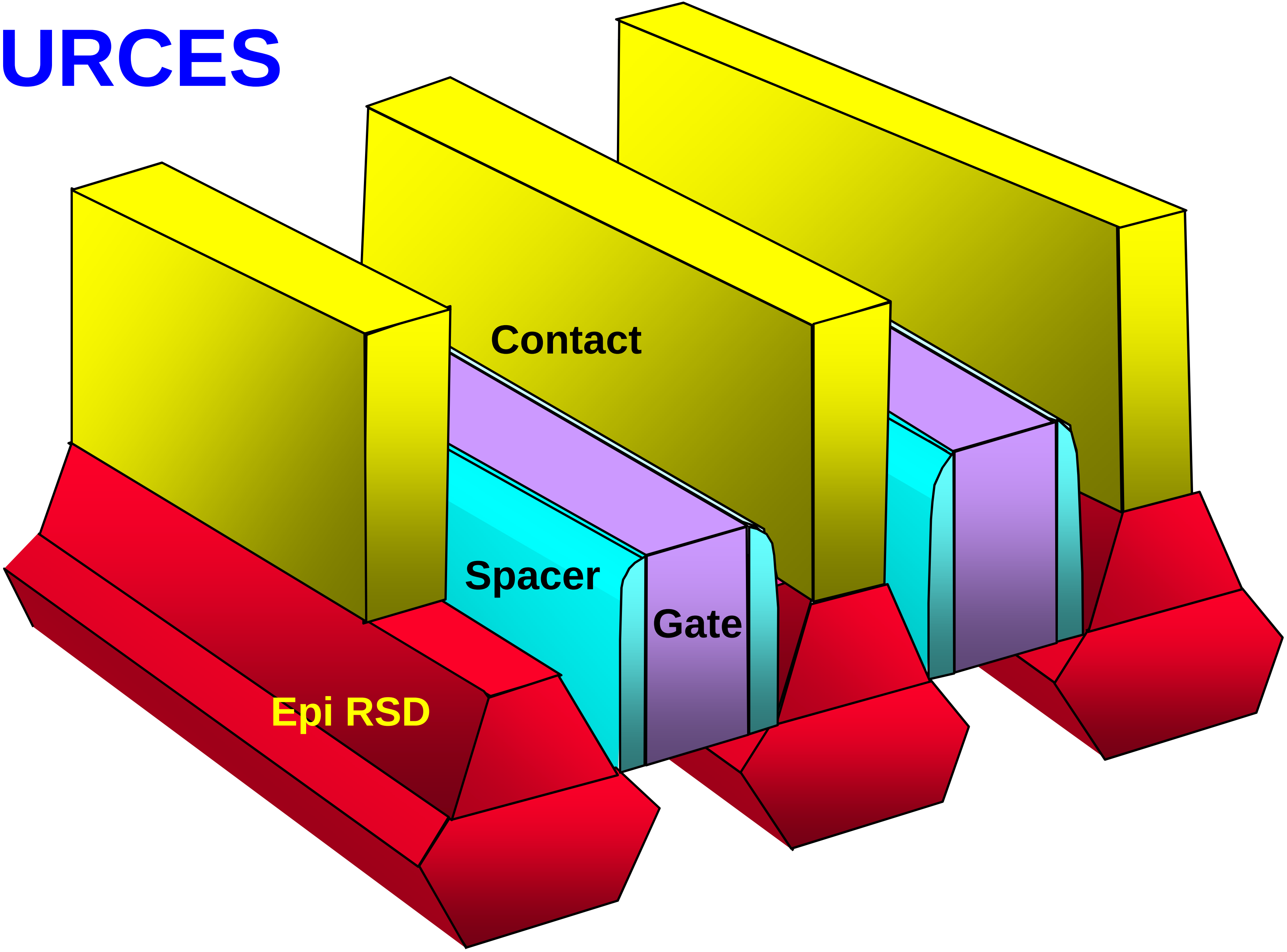
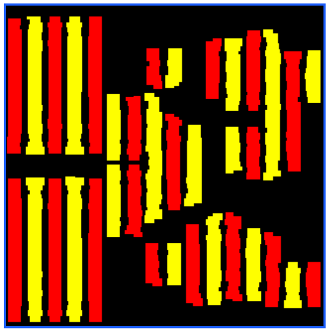
VARIATION SOURCES



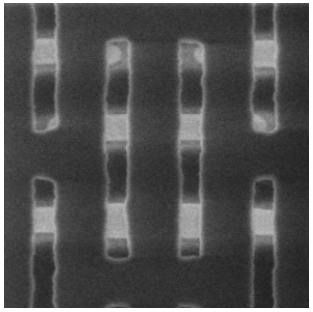
VA
SO

OPC



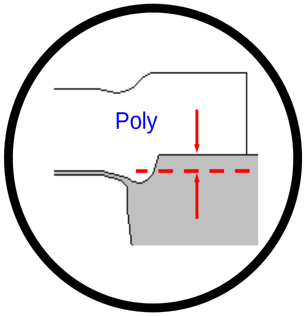
Kuhn ICCV 2009

LER/LWR



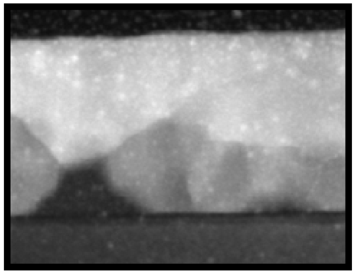
Kuhn ITJ 2009

STI Polish

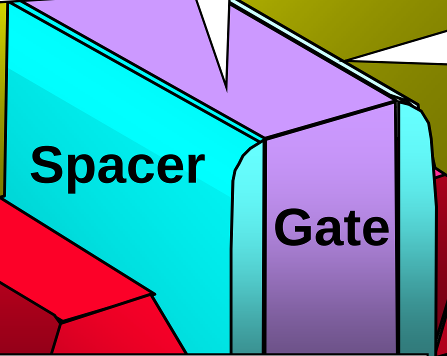


Kuhn ICCV 2009

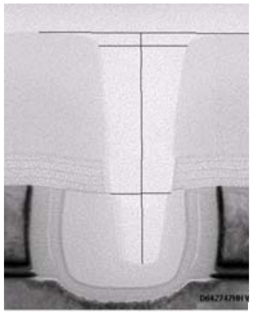
Gate granularity



Ranade IEDM 2005

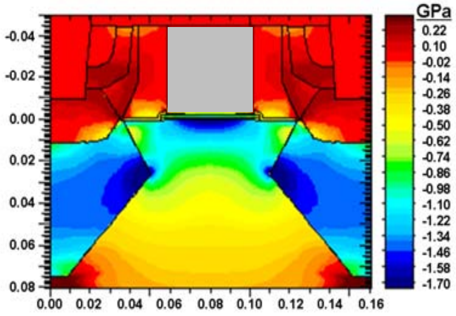


Gate polish



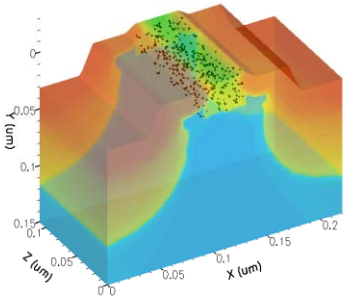
Steigerwald IEDM 2008

Strain



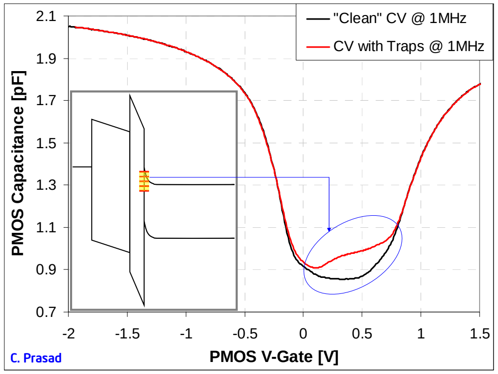
Auth, VLSI 2008

RDF + implants



Kuhn iEDM 2007

Oxide



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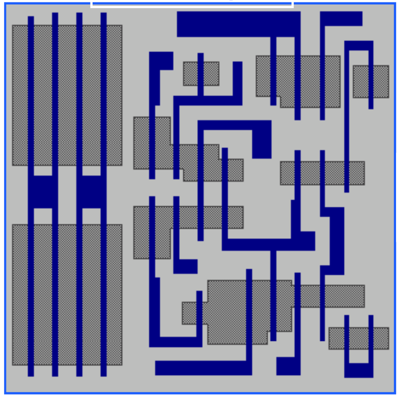
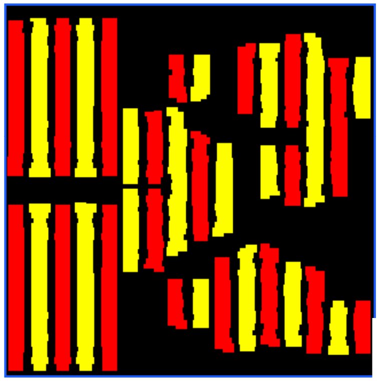


OPC/RET

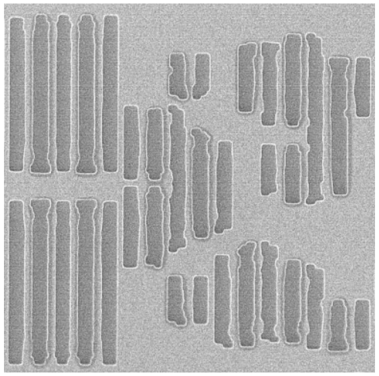
Phase mask data



Trim mask data

Reticle manufacturing

Phase mask



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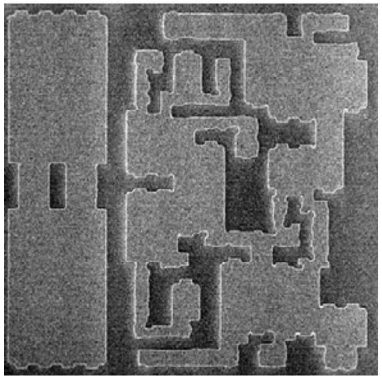
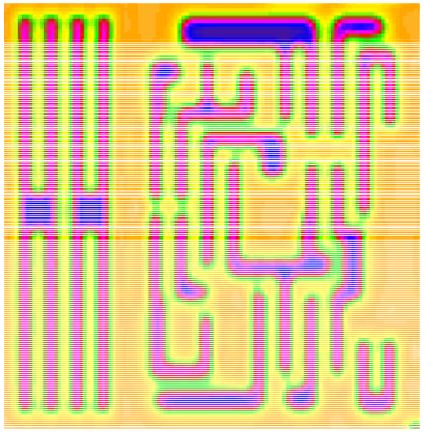
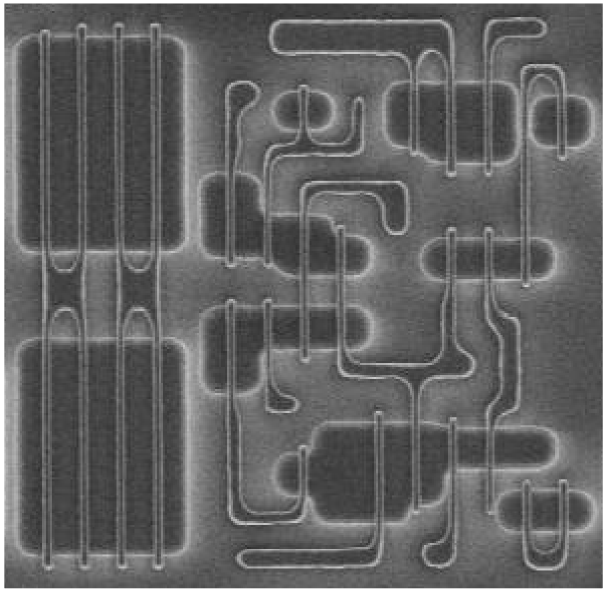


Exposure



Etch

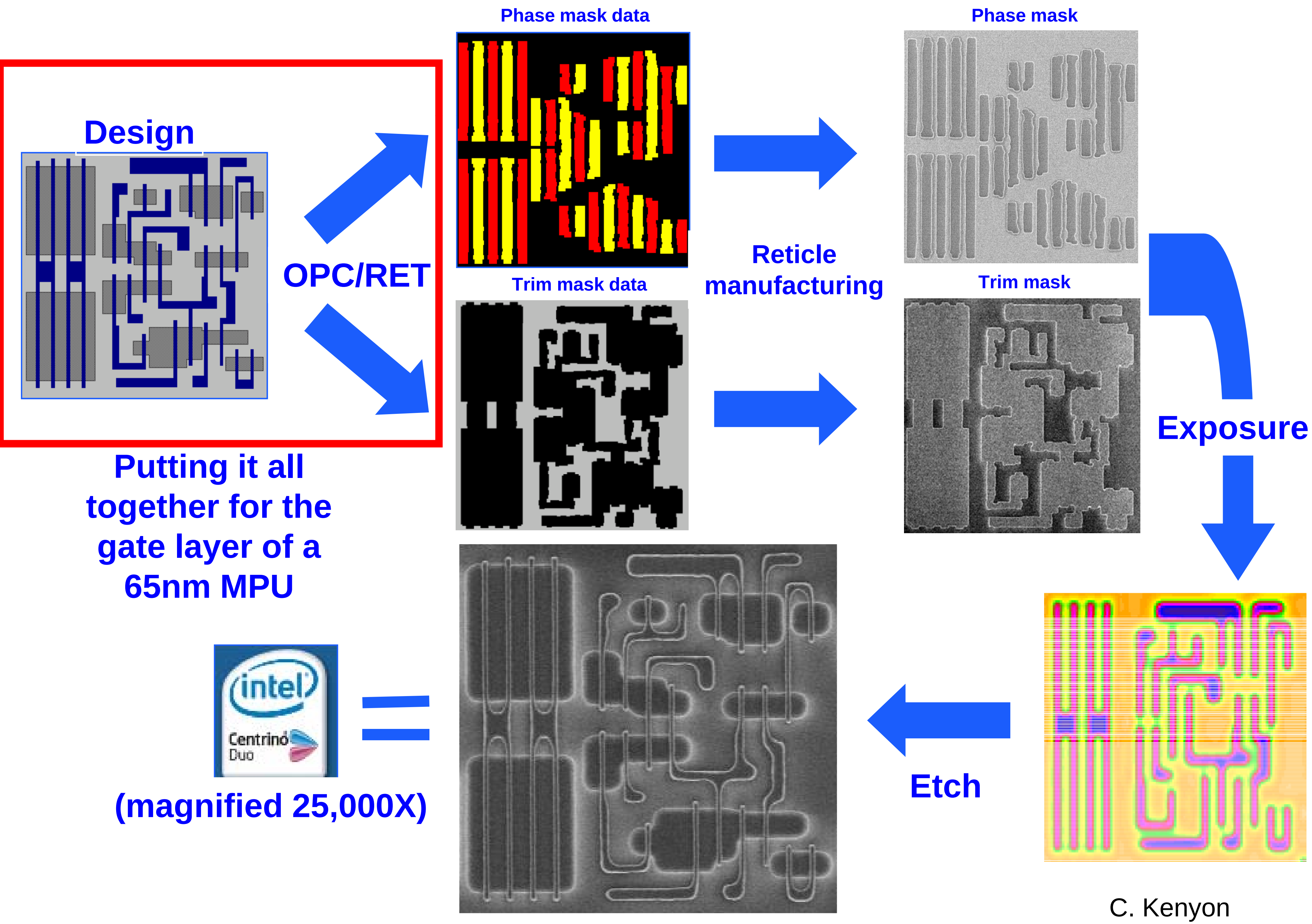


Putting it all together for the gate layer of a 65nm MPU

intel Centrino Duo =

(magnified 25,000X)

C. Kenyon
TOK conf.
Dec. 2008



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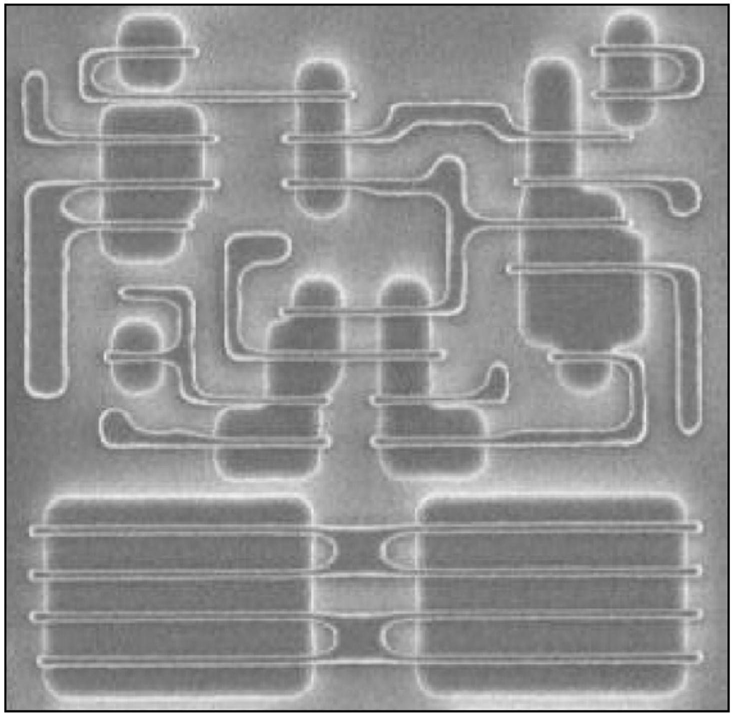
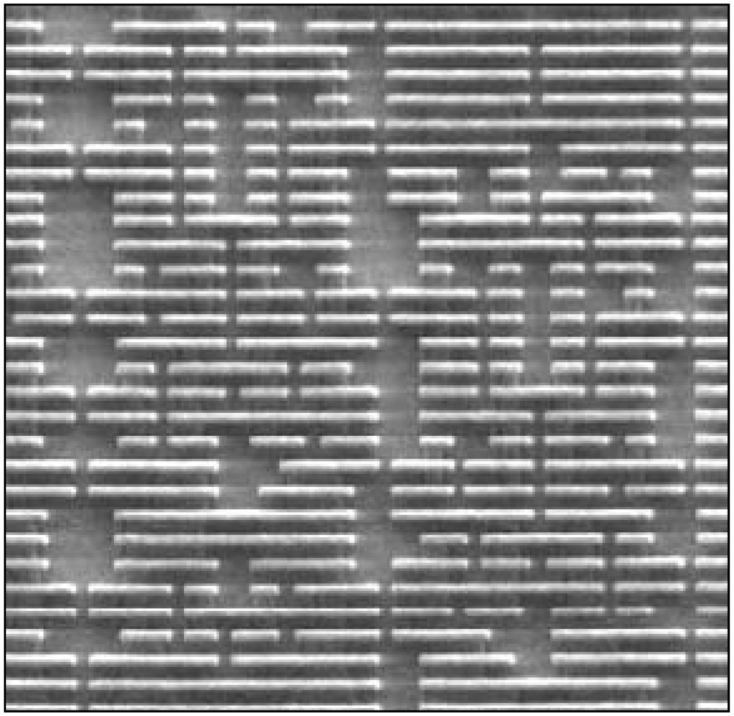
Layout Restrictions 65nm to 32nm



65 nm Layout Style

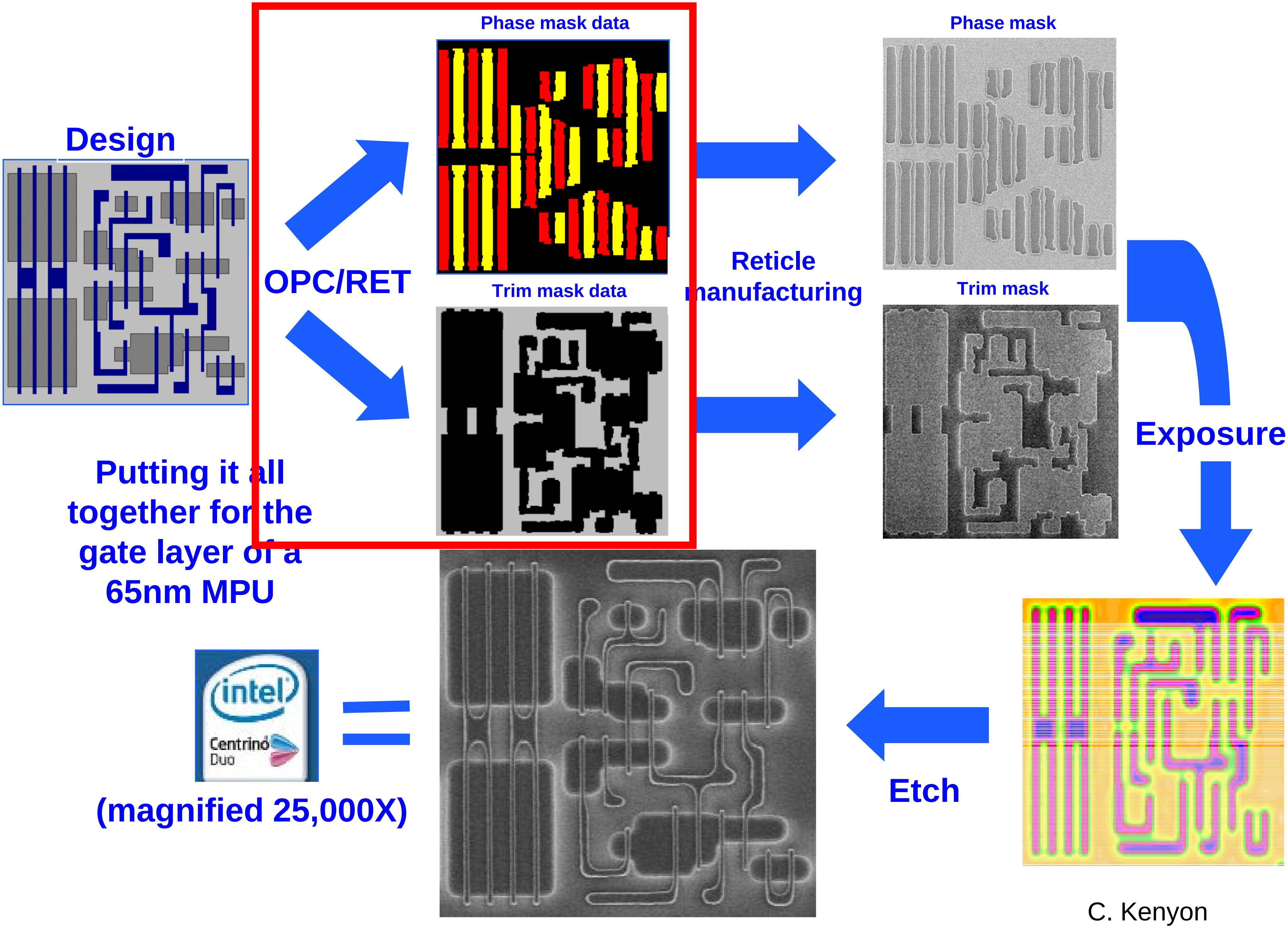
- Bi-directional features
- Varied gate dimensions
- Varied pitches



32 nm Layout Style

- Uni-directional features
- Uniform gate dimension
- Gridded layout

M. Bohr, ISCC, 2009



Putting it all together for the gate layer of a 65nm MPU

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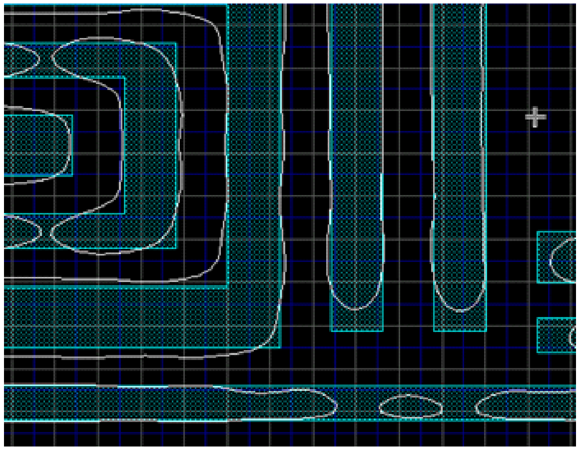
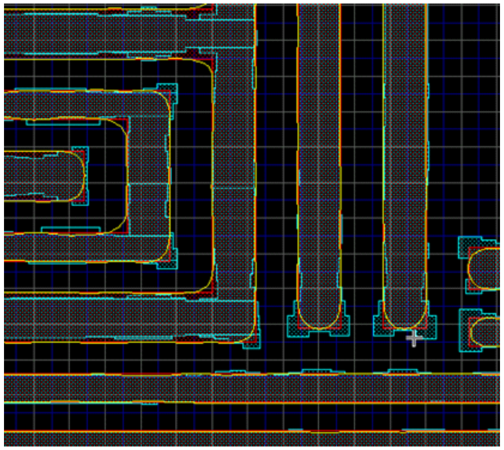
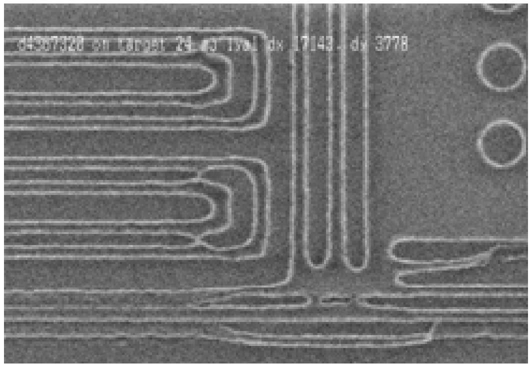
Optical Proximity Correction (OPC)
As a Resolution Enhancement Technique



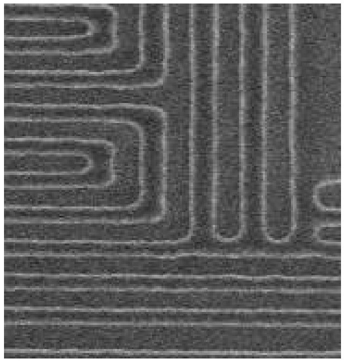
Contour prediction – no OPC



Contour prediction – with OPC



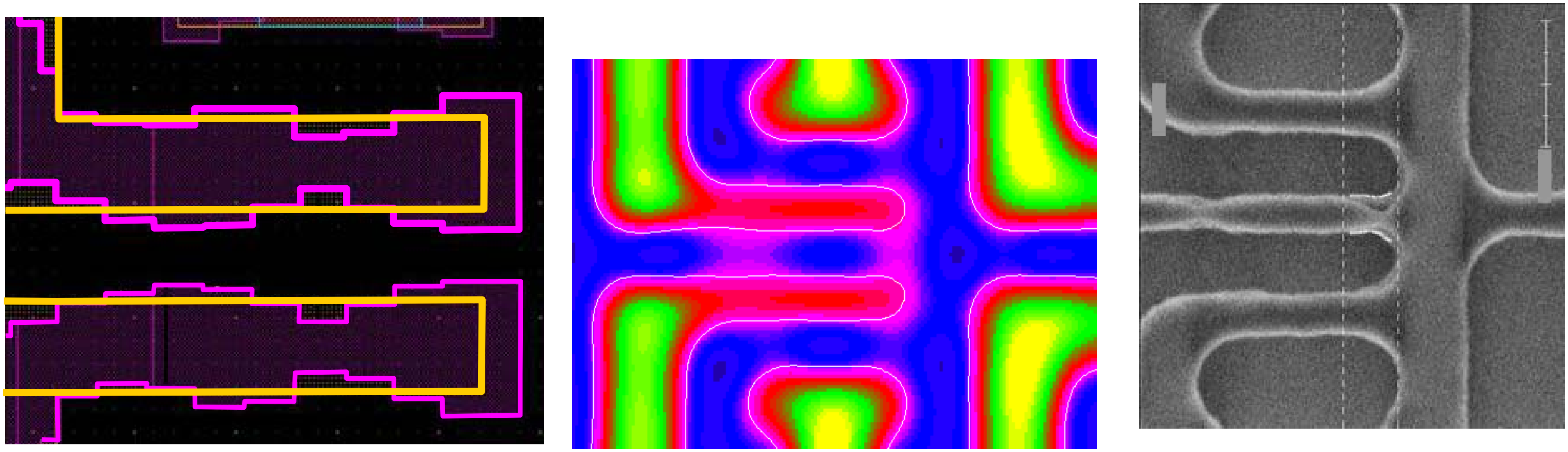
SEM Image – no OPC



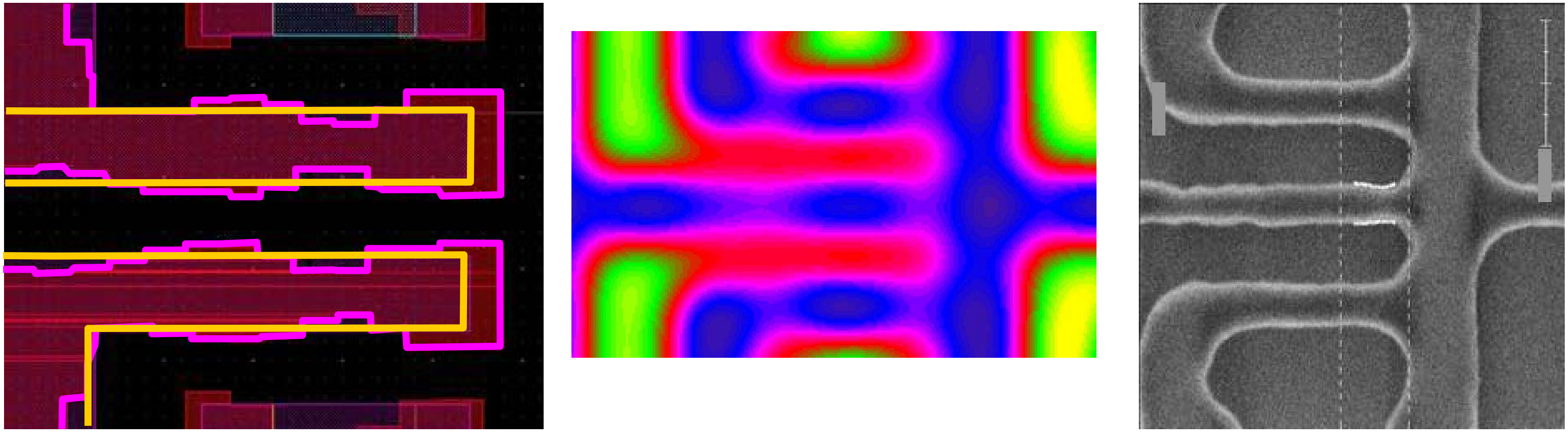
SEM Image – with OPC

K. Wells-Kilpatrick: 2007

45nm: OPC as a Variation Management Technique



Top-down resist CD meets spec, but poor contrast leads to poor resist profile which gets transferred to metal pattern after etch, resulting in shorting marginality

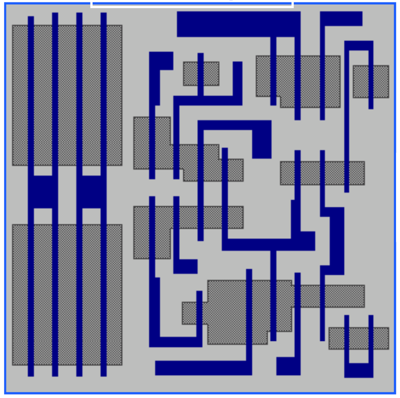


Computational lithography solution

K. Kuhn, IEDM 2007

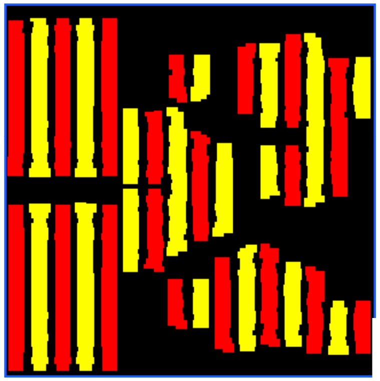
Putting it all together for the gate layer of a 65nm MPU

Design



OPC/RET

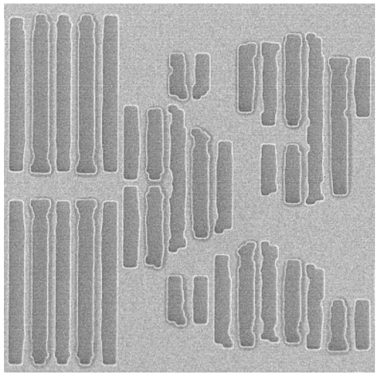
Phase mask data



Trim mask data

Reticle manufacturing

Phase mask



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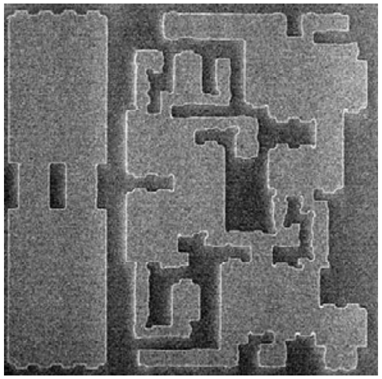
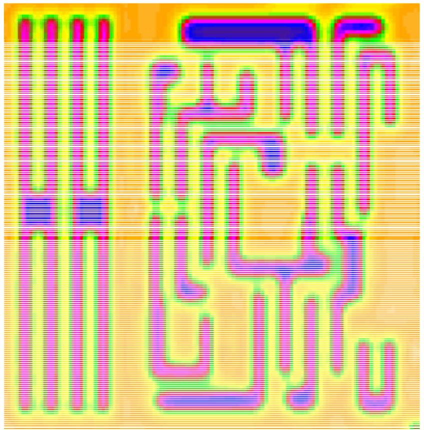
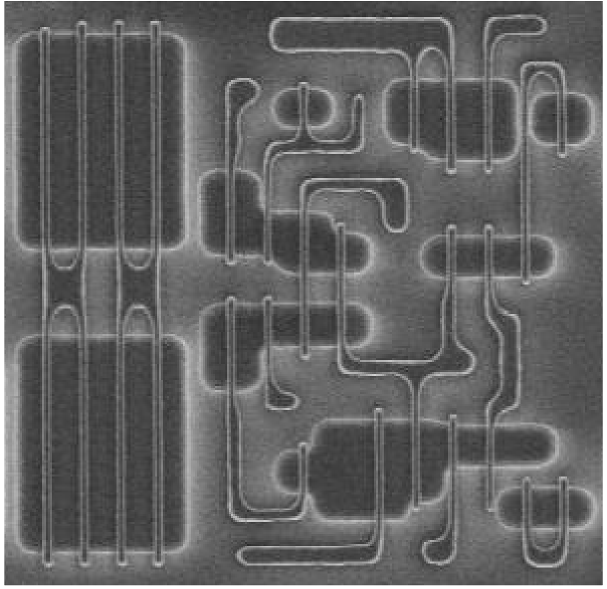


Exposure



Etch



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MEEF

Mask Error Enhancement Factor

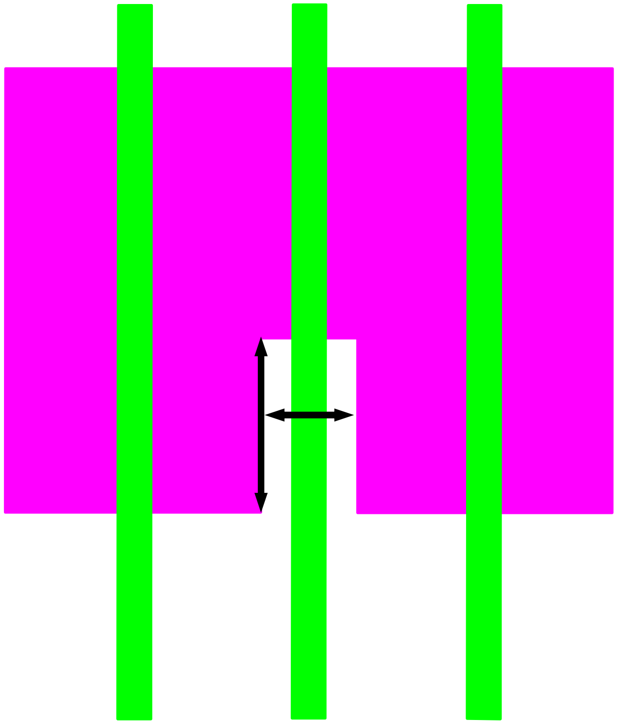
- MEEF is a scaling factor that causes certain layout geometries to exhibit a greater sensitivity to mask dimension tolerances.
- Any dimensional error in the mask is magnified on the wafer by the MEEF value.

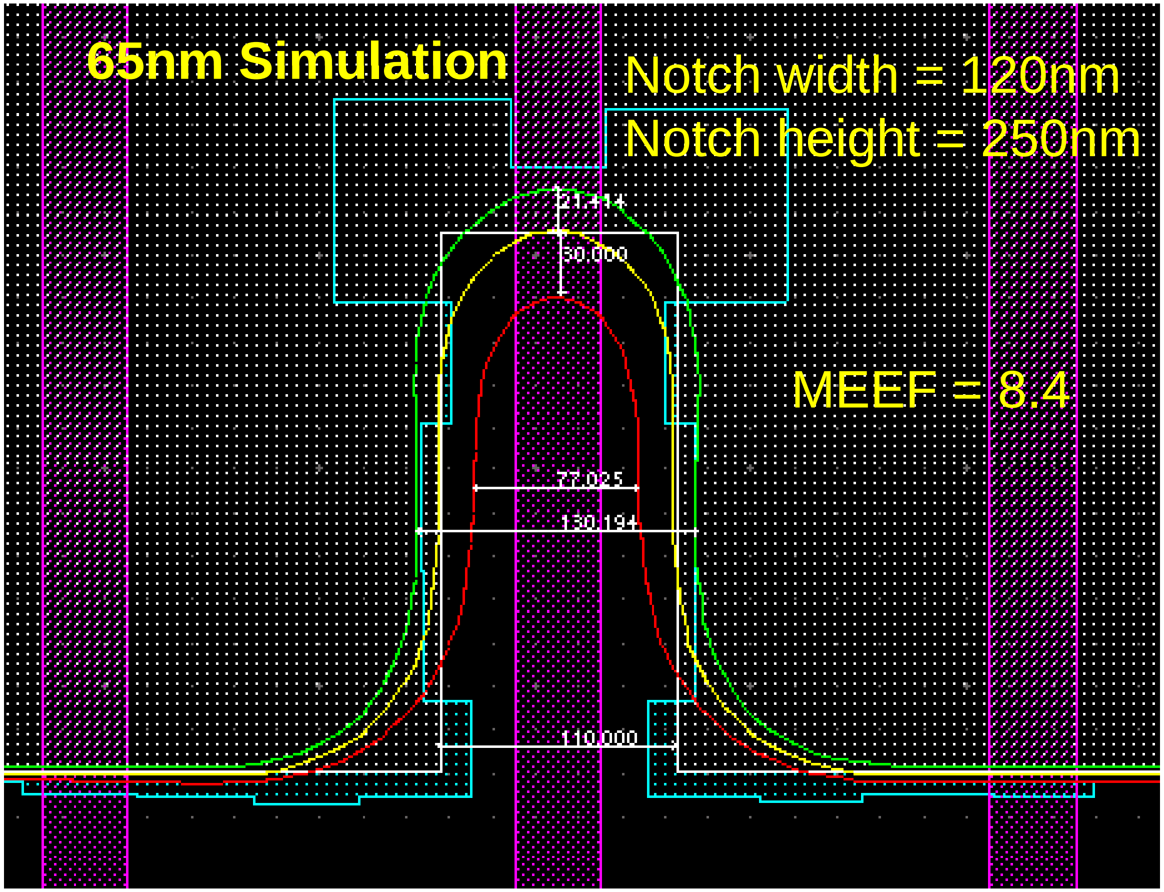
$$\Delta W_{wafer} = MEEF * \Delta W_{mask}$$

- Depending on the value of the mask error and the lithography exposure/focus conditions the final printed pattern can be either larger or smaller.

MEEF Impact on Ze Error

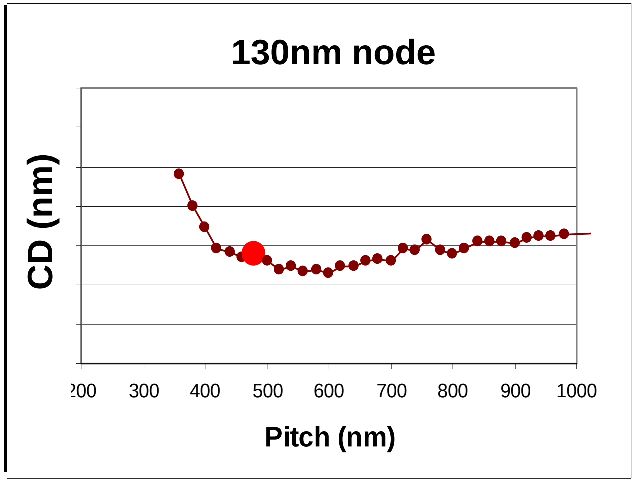
Ze error can be either positive or negative



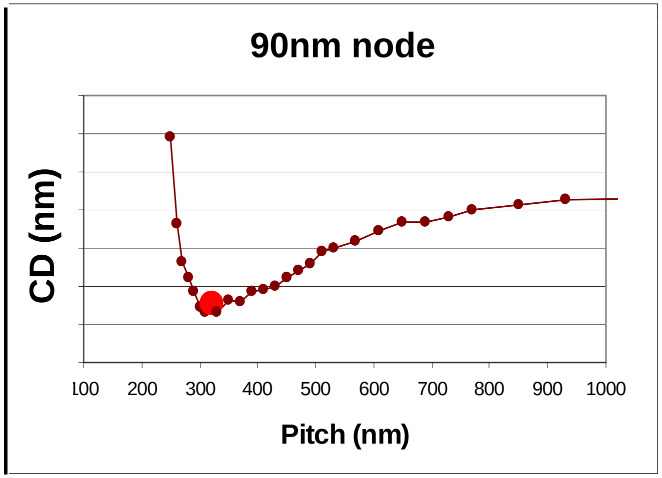


Yellow: DCCD contour after OPC
Green: with -3.375 nm mask making error
Red: with 3.375 nm mask making error

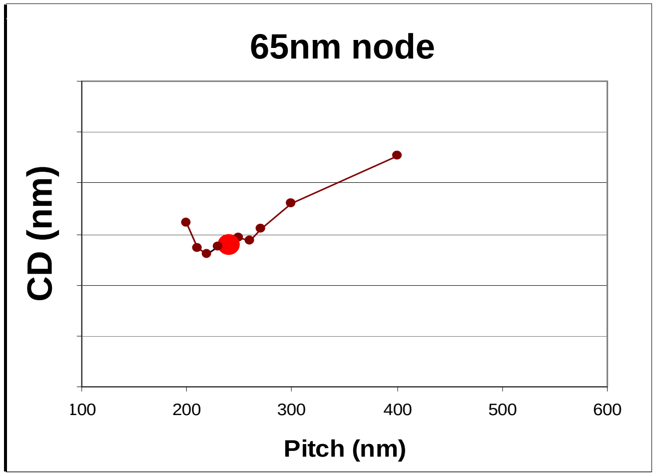
MEEF and Historical gate CD vs. pitch



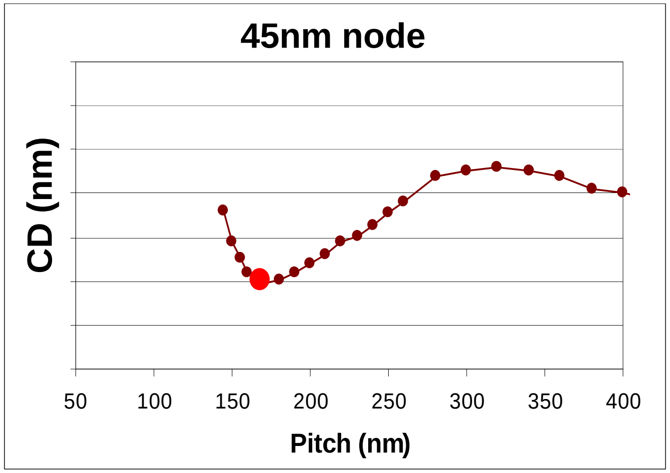
248nm; OAI; model-based OPC



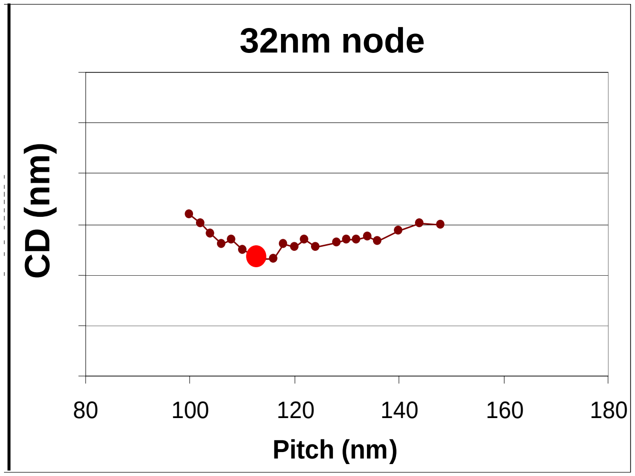
193nm; OAI; model-based OPC



193nm; APSM; model-based OPC



193nm; APSM; model- based OPC double patterning



193nm; immersion; APSM; model- based OPC; double patterning; polarization

● Contacted gate pitch

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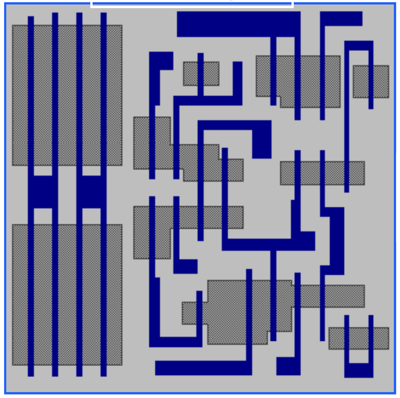
Low MEEF requires targeting in the "flat" portion of CD vs. pitch
Process innovations continue this trend in the 32nm node

Putting it all together for the gate layer of a 65nm MPU

Design



OPC/RET

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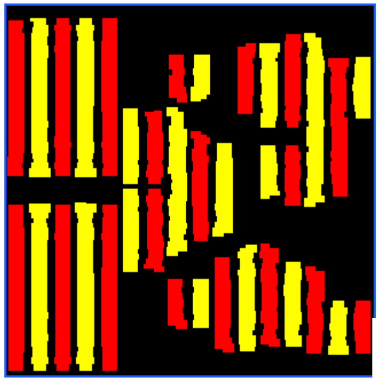
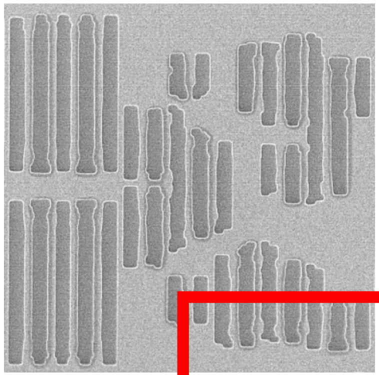


Trim mask data

Reticle manufacturing

Phase mask



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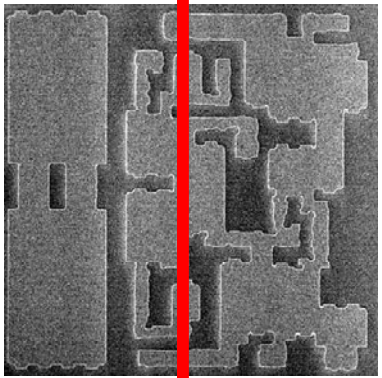

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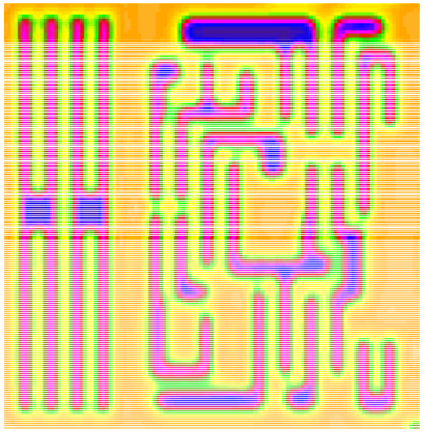

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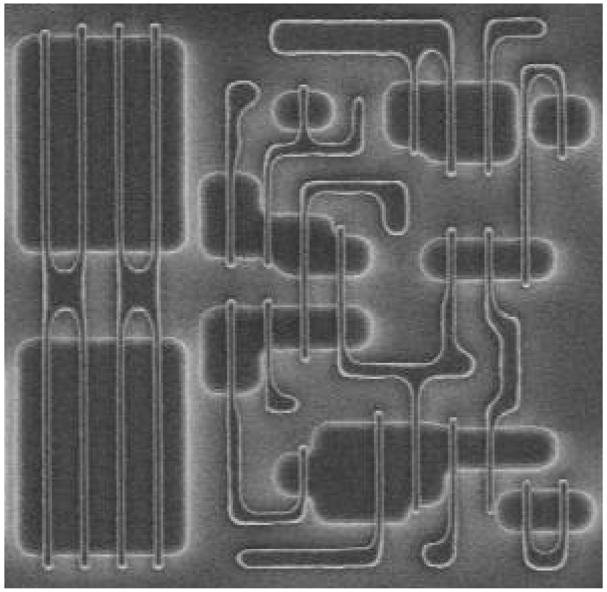

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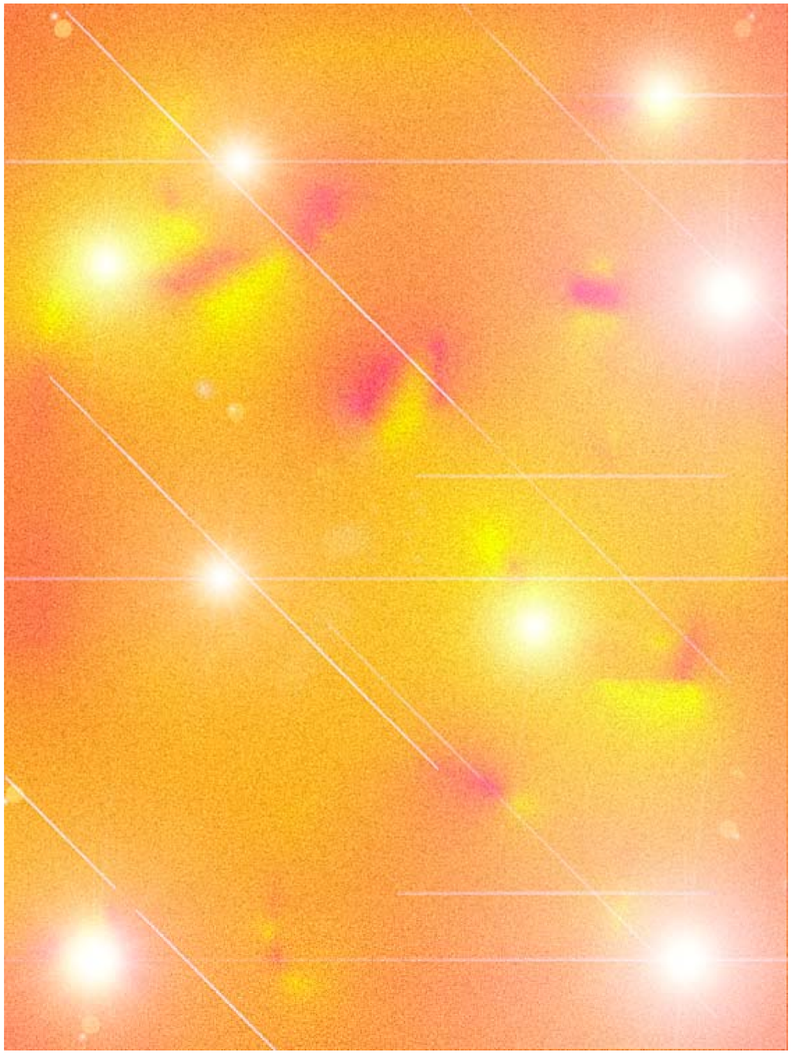
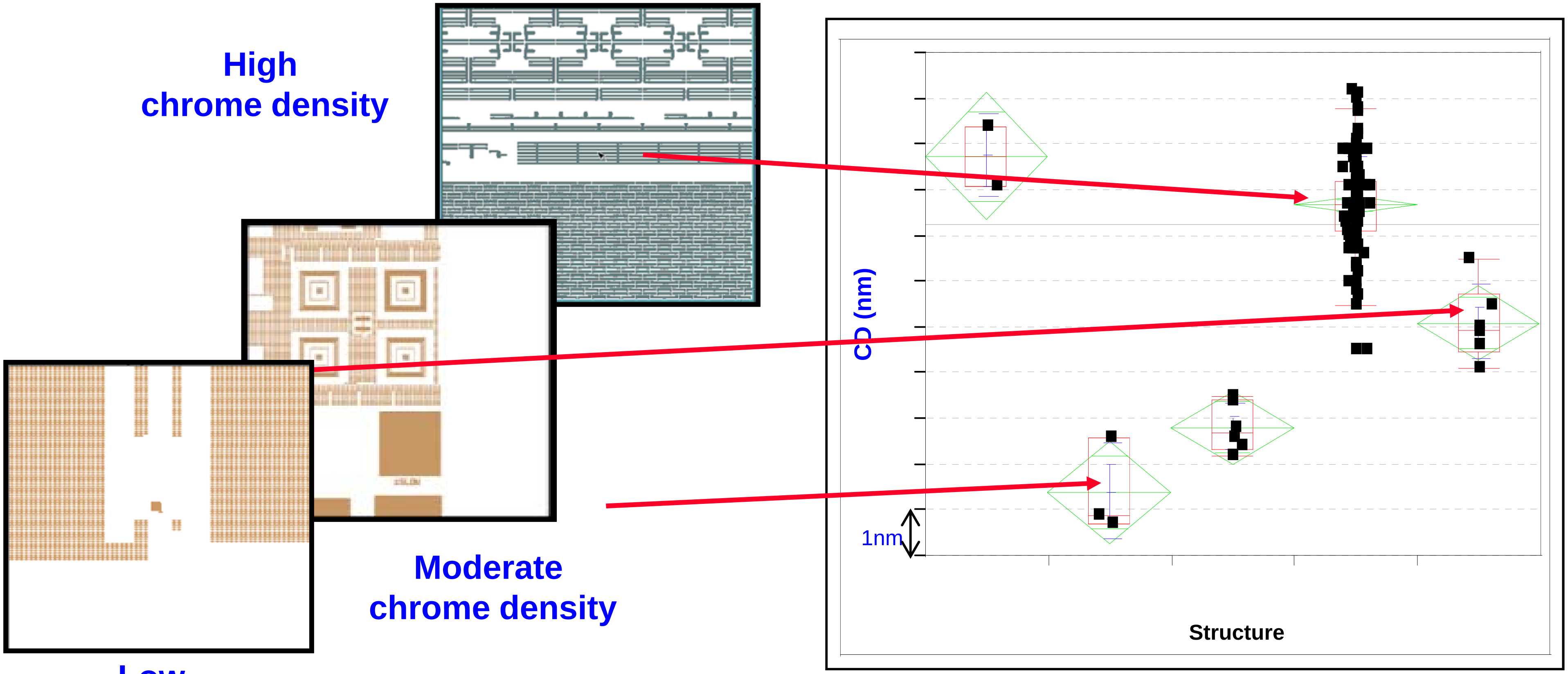
FLARE



- Flare is unwanted scattered light arriving at the wafer
- Flare is caused by interactions that force the light to travel in a "non-ray trace" direction.
- Flare is both a function of local environment around a feature (short range flare) and the total amount of energy going through the lens (long range flare).

Impact of flare on gate CDs

All structures have identical reticle CD and pitch



High chrome density

Moderate chrome density

Low chrome density

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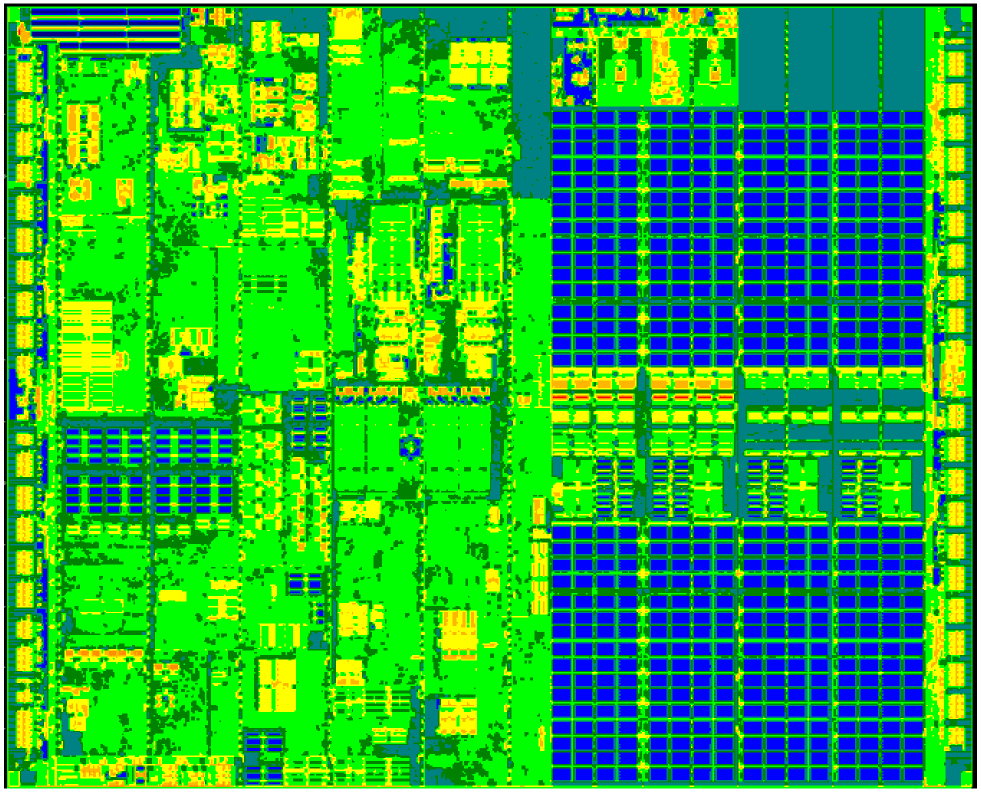
- **During 65nm process development, large CD deviations were observed for structures having identical pitch and reticle CD due to flare**
- **Gates only 500μm away from one another could be >5nm different in CD**

Flare Variation Improvement with OPC

Color Code		Chrome Fraction
🟦	109:0	56.0 – 63.0
🟦	108:0	49.0 - 56.0
🟦	107:0	42.0 – 49.0
🟩	106:0	35.0 – 42.0
🟩	105:0	28.0 – 35.0
🟨	104:0	21.0 – 28.0
🟧	103:0	14.0 – 21.0
🟧	102:0	7.0 – 14.0
🟥	101:0	0.0 – 7.0

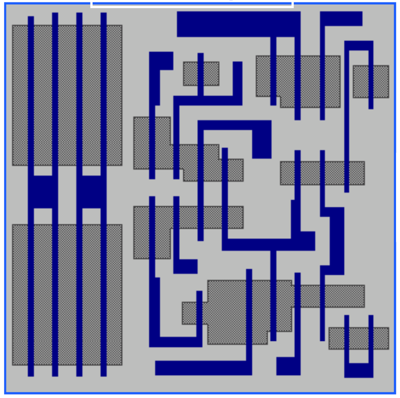


Development effort produced an algorithm capable of scanning designs and binning regions by local chrome fraction

Binning algorithm is combined with flare-calibrated OPC model

C. Kenyon, TOK conf., Dec. 2008

Design



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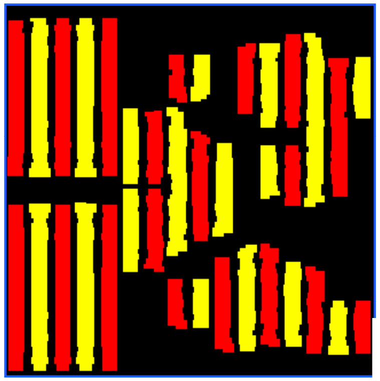

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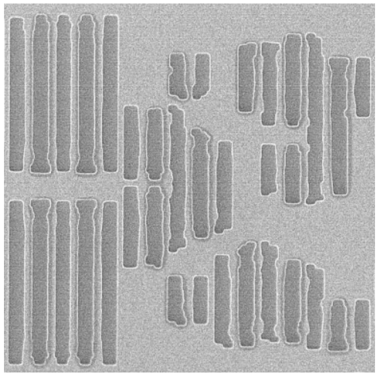

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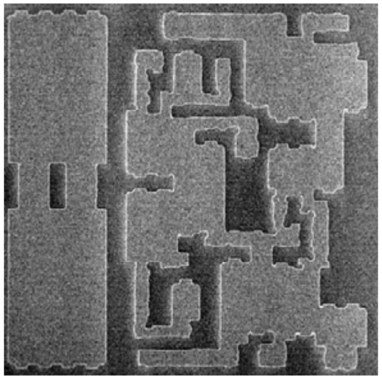
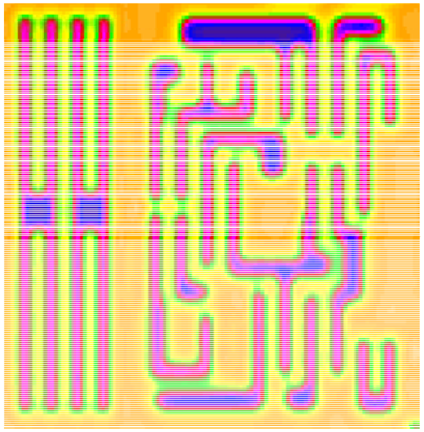
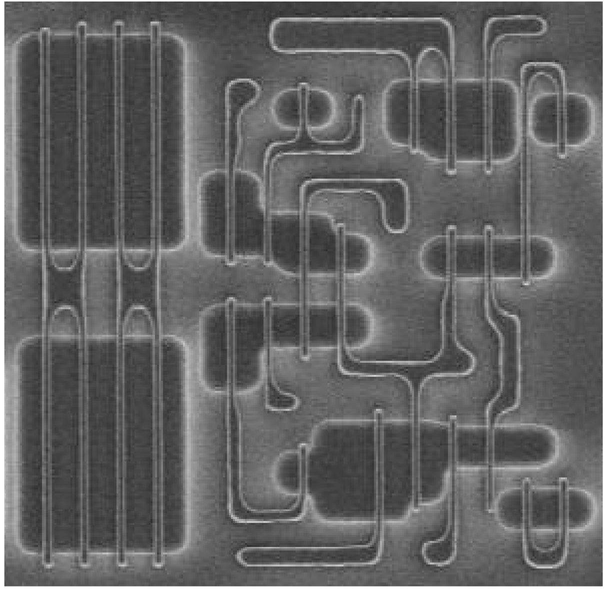


Exposure



Etch



Putting it all together for the gate layer of a 65nm MPU

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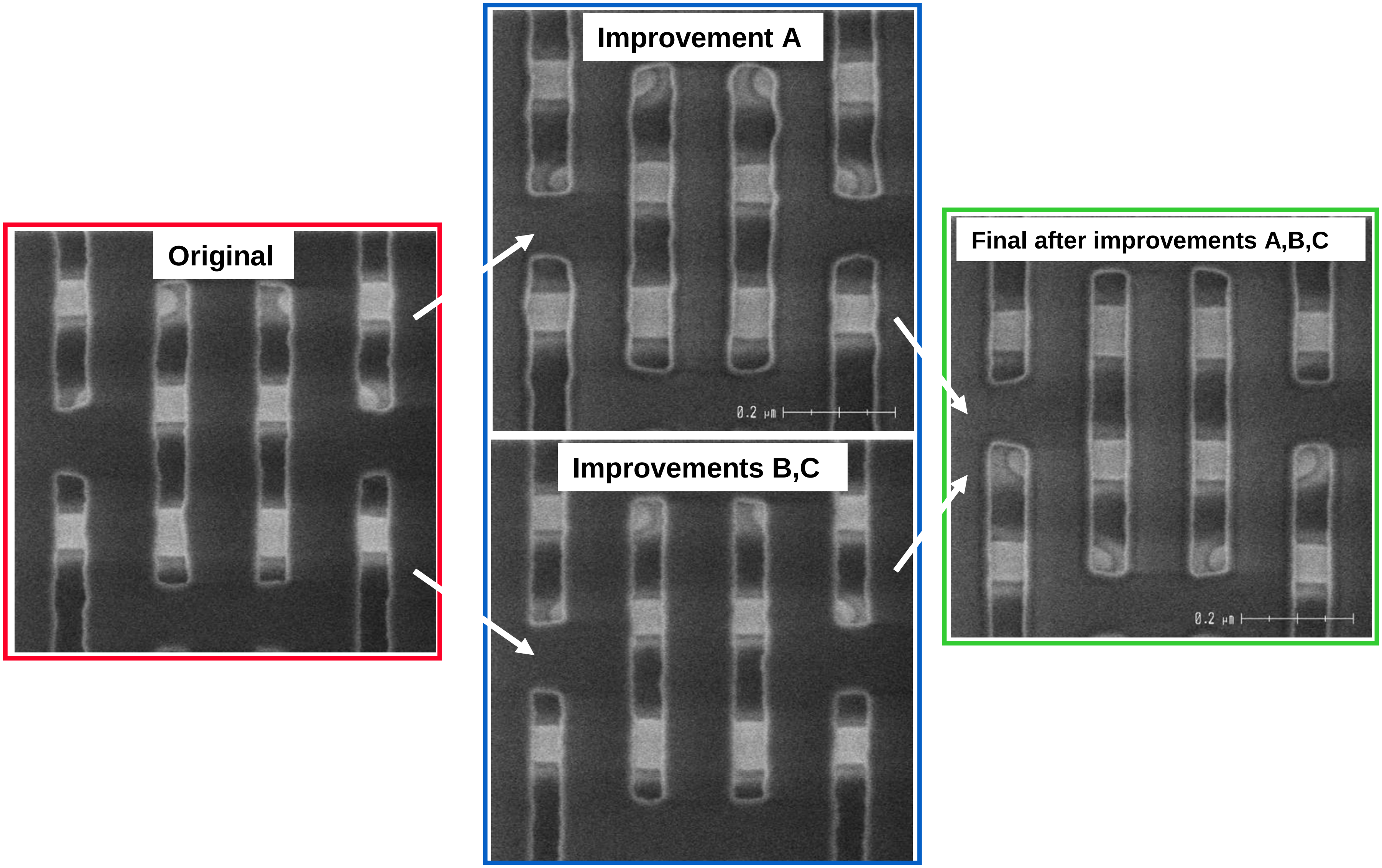
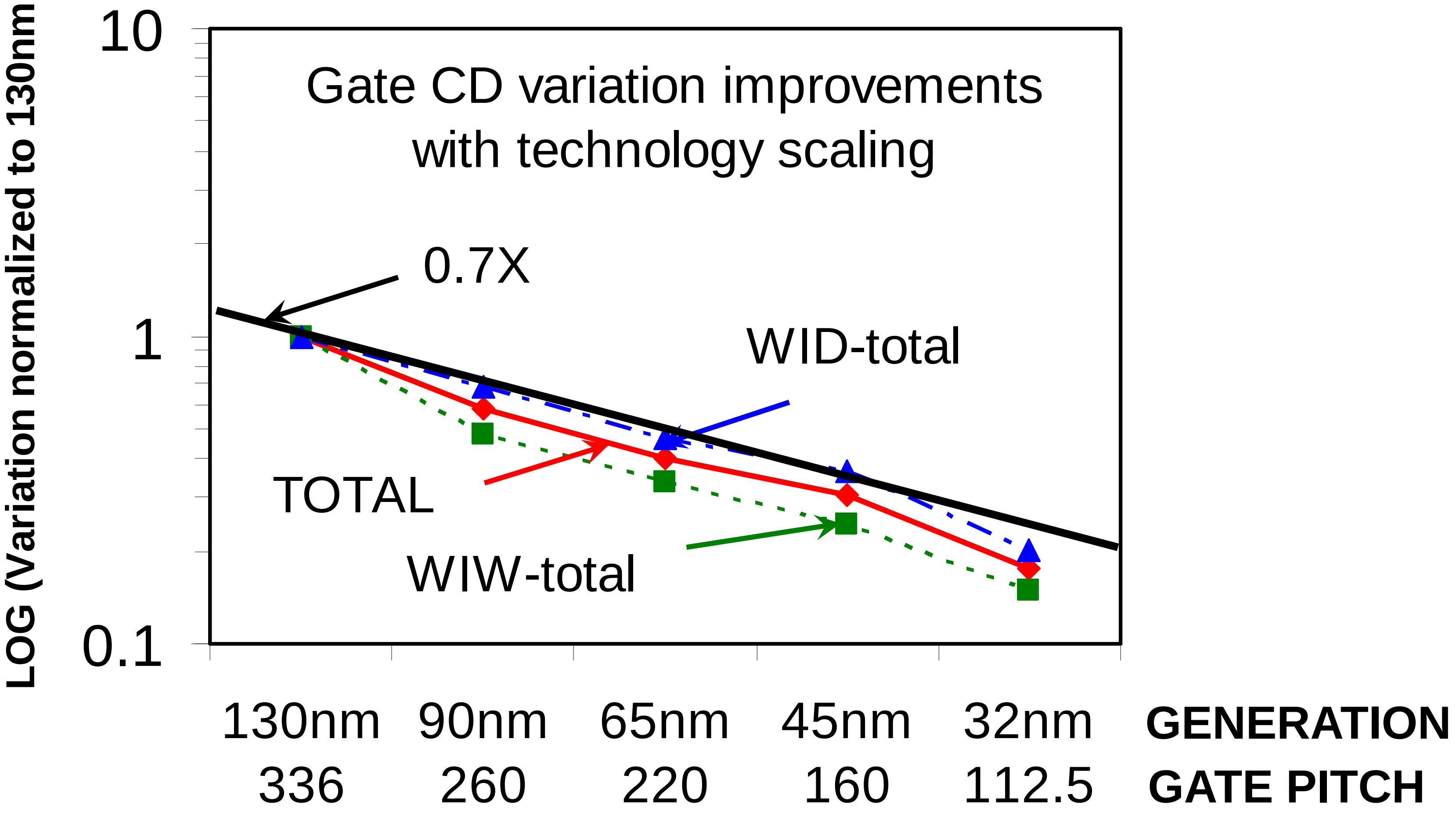
45nm highlights role of lithography/etch in resolving LER/LWR



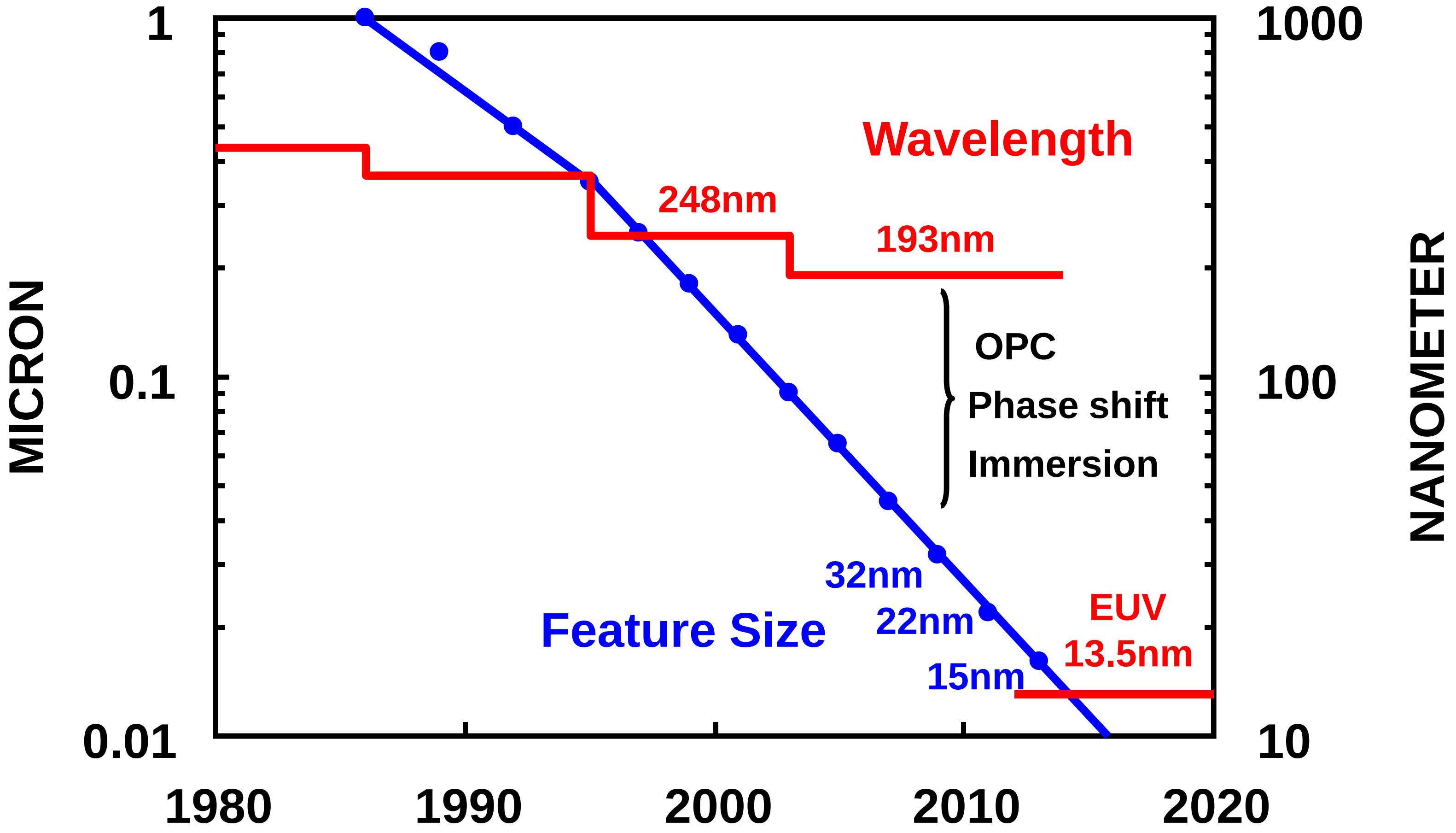
K. Kuhn, ITJ, 2008

Technology Trend
Systematic Gate CD Lithography Variation



Critical to management of variation is the ability to deliver a 0.7X gate CD variation improvement in each generation enabled by continuous process technology improvements

Lithography Pipeline



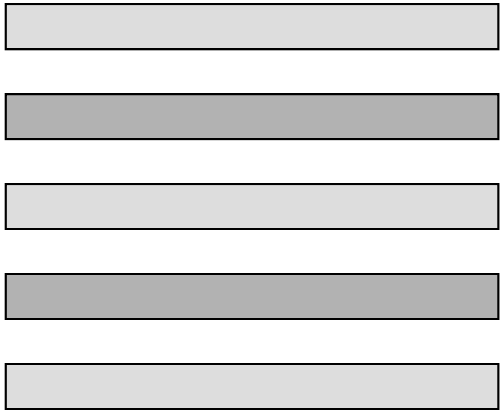
Extend 193nm Optical Lithography as far as possible
Deploy EUV Lithography when available/affordable

Non-EUV Lithography Beyond 32 nm

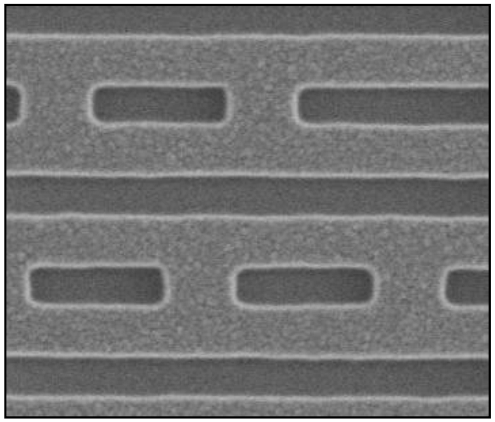
Double Patterning

- Pitch doubling
- Improved 2-D features

Pitch Doubling

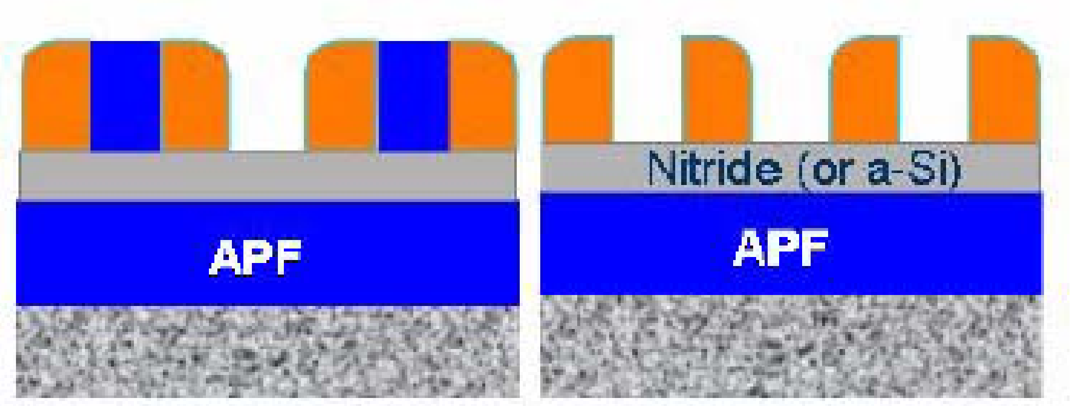


2-D Features



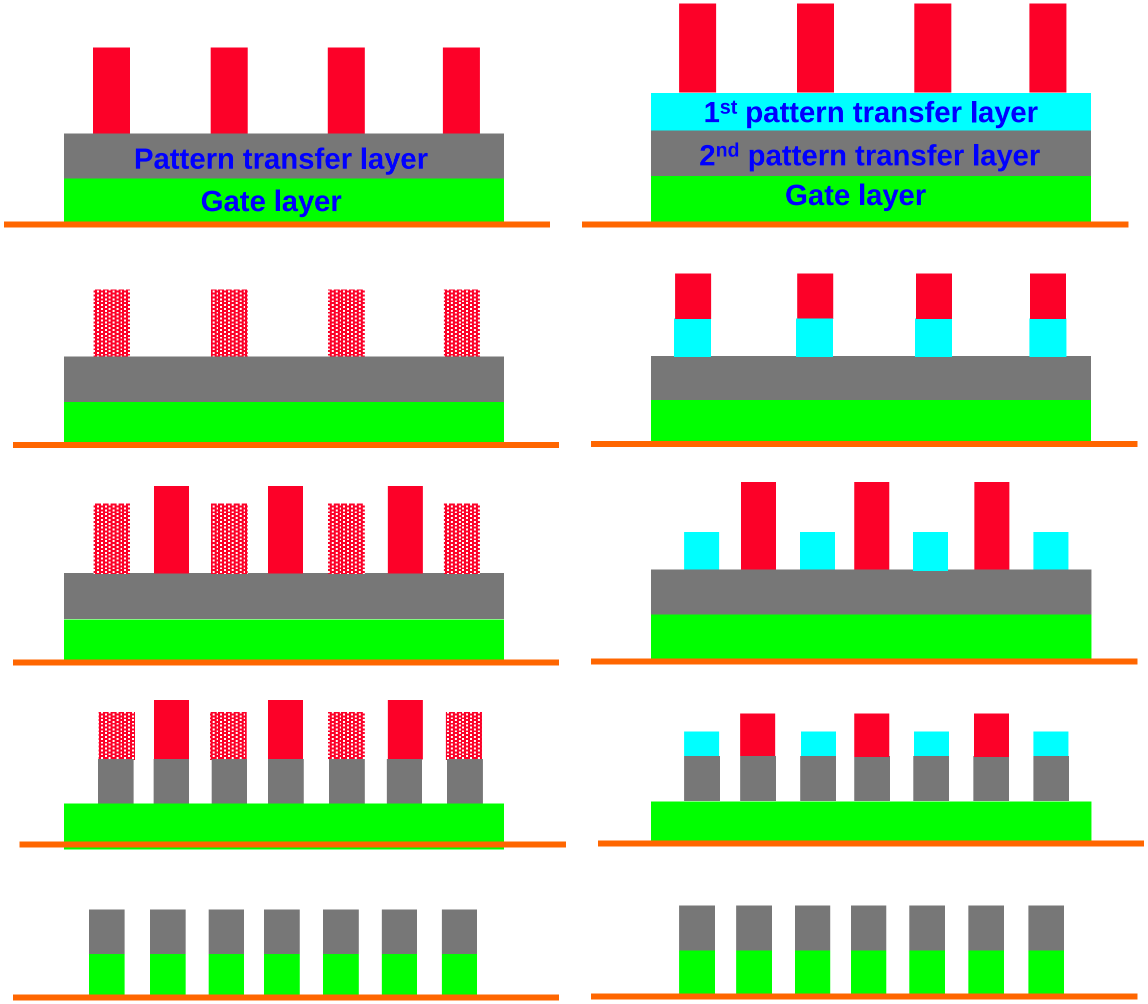
Spacer Gate Patterning

- Pitch doubling
- Improved variation



M. Bohr, ISCC, 2009
Bencher et al, Proc. of SPIE Vol. 6924 69244E-7

Pitch doubling and gate CD control



Resist freeze

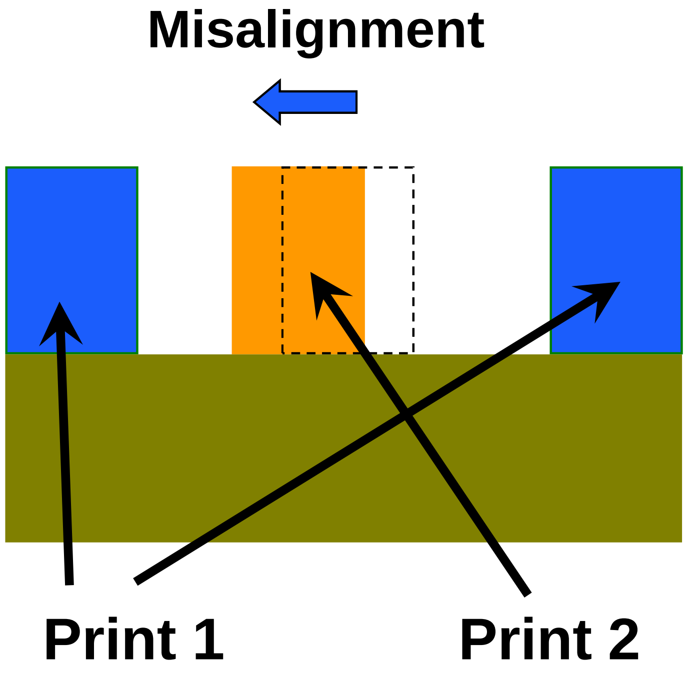
Double Pattern Transfer

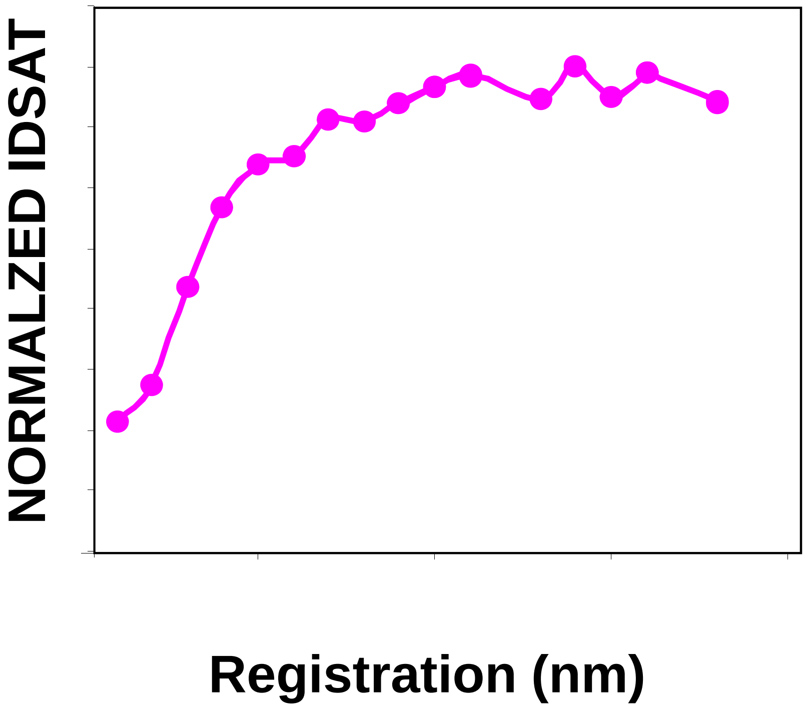
Neither Resist Freeze nor Double Pattern Transfer achieve full benefit of patterning at ½ pitch

Both techniques still require resolution of a very small space (MEEF, LWR etc.)

C. Kenyon, TOK conf., Dec. 2008

Disadvantages of Double-patterning

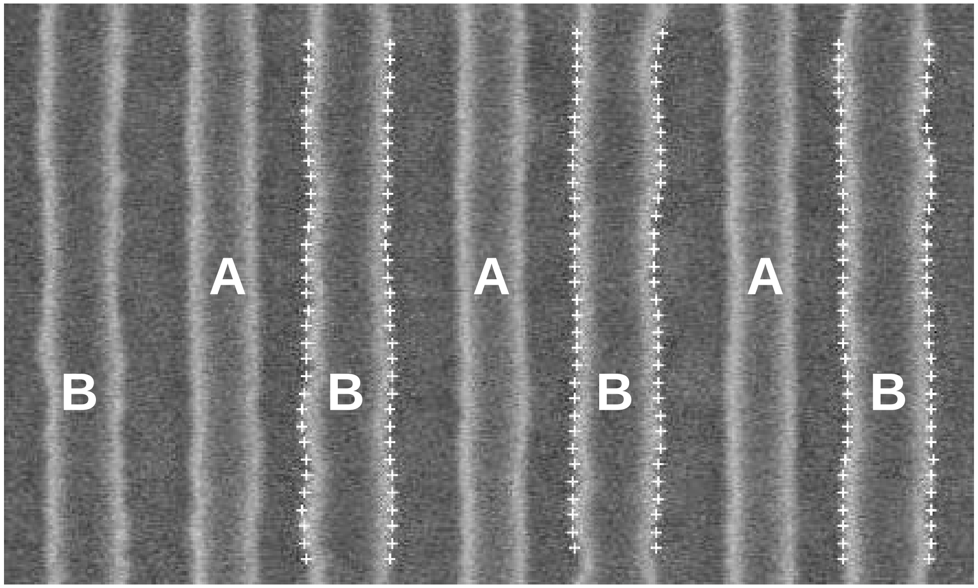


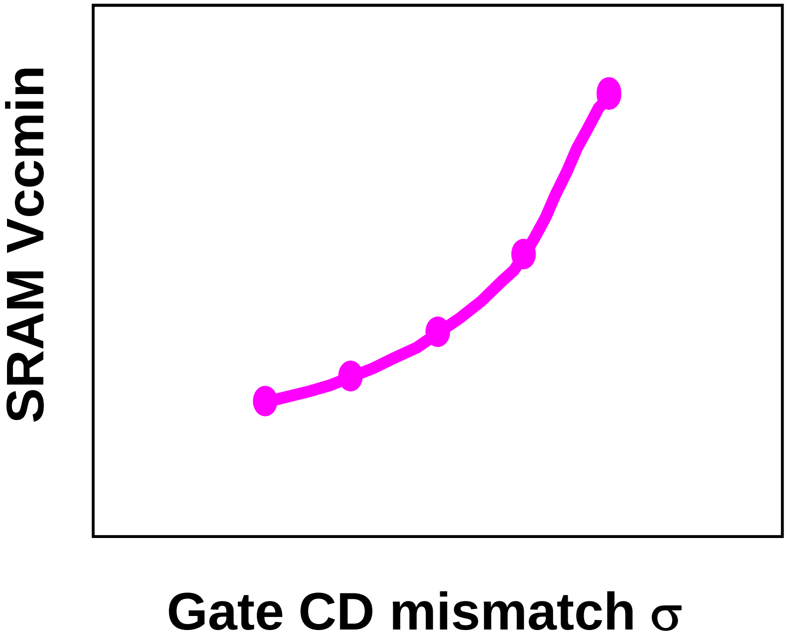


Misalignment between the 2 exposures is a crucial liability for this technique and can limit its usability

Transistor parameters can be affected by asymmetry between the source and drain regions

Pitch doubling and gate CD matching



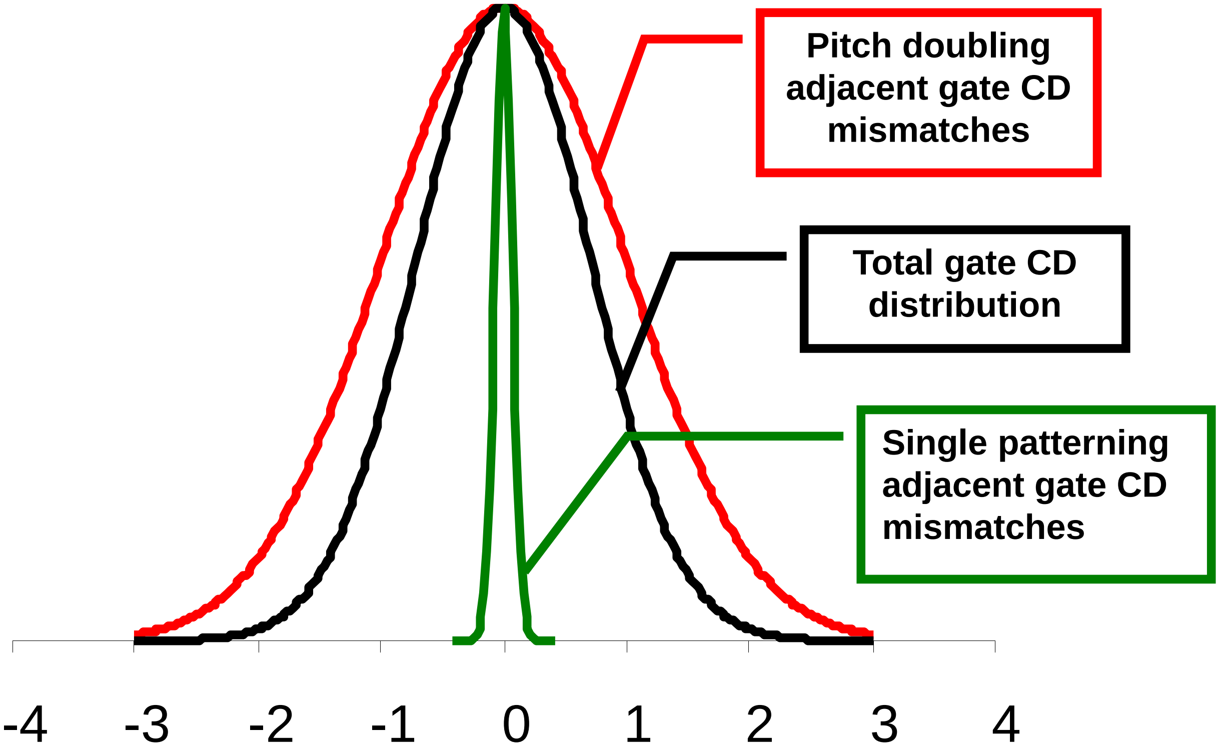


Pitch doubling eliminates the close correlation which currently exists between the CDs of adjacent gates

This has implications for memory cells and other circuits which depend upon this CD matching

C. Kenyon, TOK conf., Dec. 2008

Pitch doubling and gate CD matching



Pitch doubling adjacent gate CD mismatches

Total gate CD distribution

Single patterning adjacent gate CD mismatches

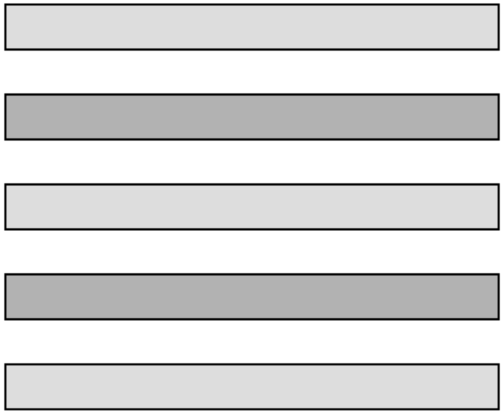
Single patterning: the distribution of CD mismatches between adjacent gates is a very small fraction of total gate CD variation

Pitch doubling: the distribution of CD mismatches is GREATER than the total gate CD variation

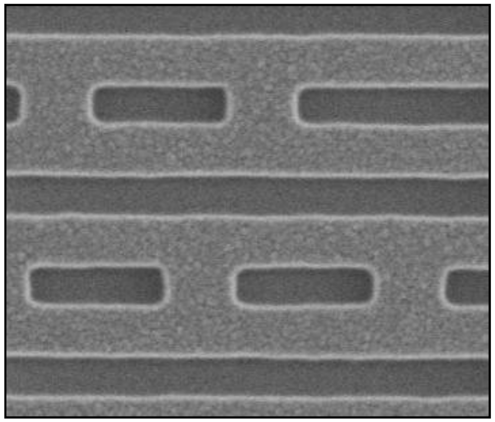
C. Kenyon, TOK conf., Dec. 2008

Non-EUV Lithography Beyond 32 nm

Pitch Doubling



2-D Features

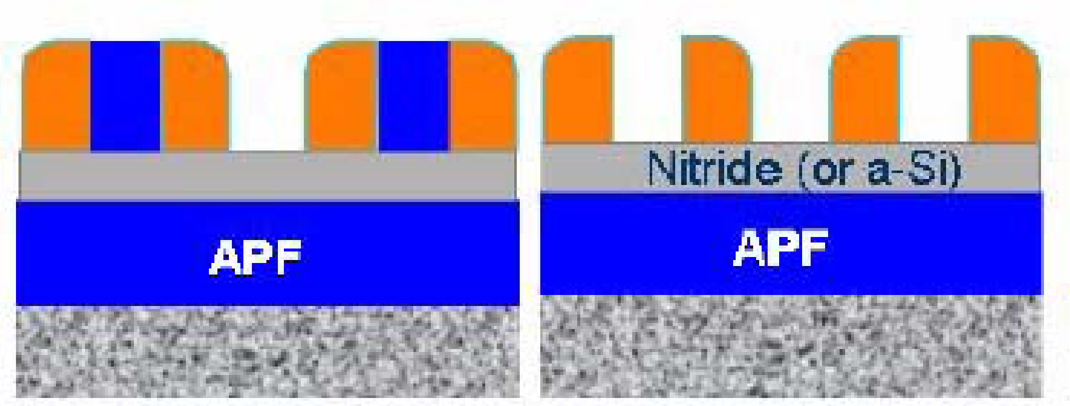


Double Patterning

- Pitch doubling
- Improved 2-D features

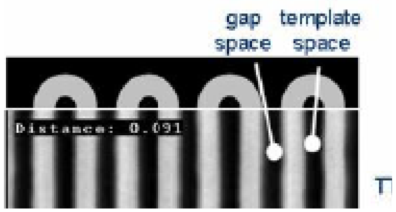
Spacer Gate Patterning

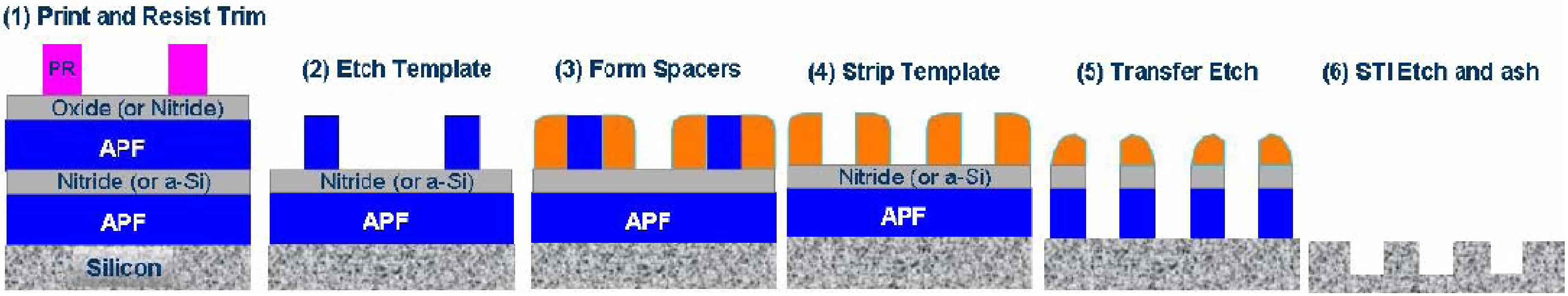
- Pitch doubling
- Improved variation

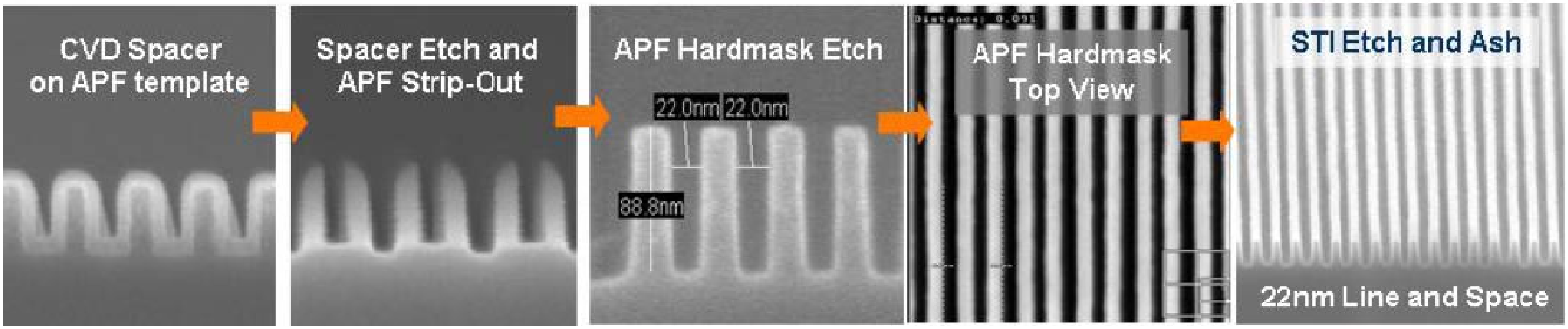


M. Bohr, ISCC, 2009
Bencher et al, Proc. of SPIE Vol. 6924 69244E-7

Alternative: Spacer patterning



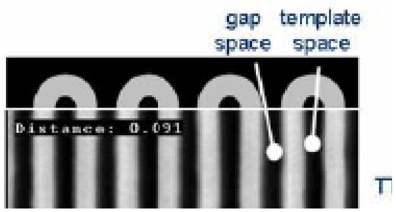


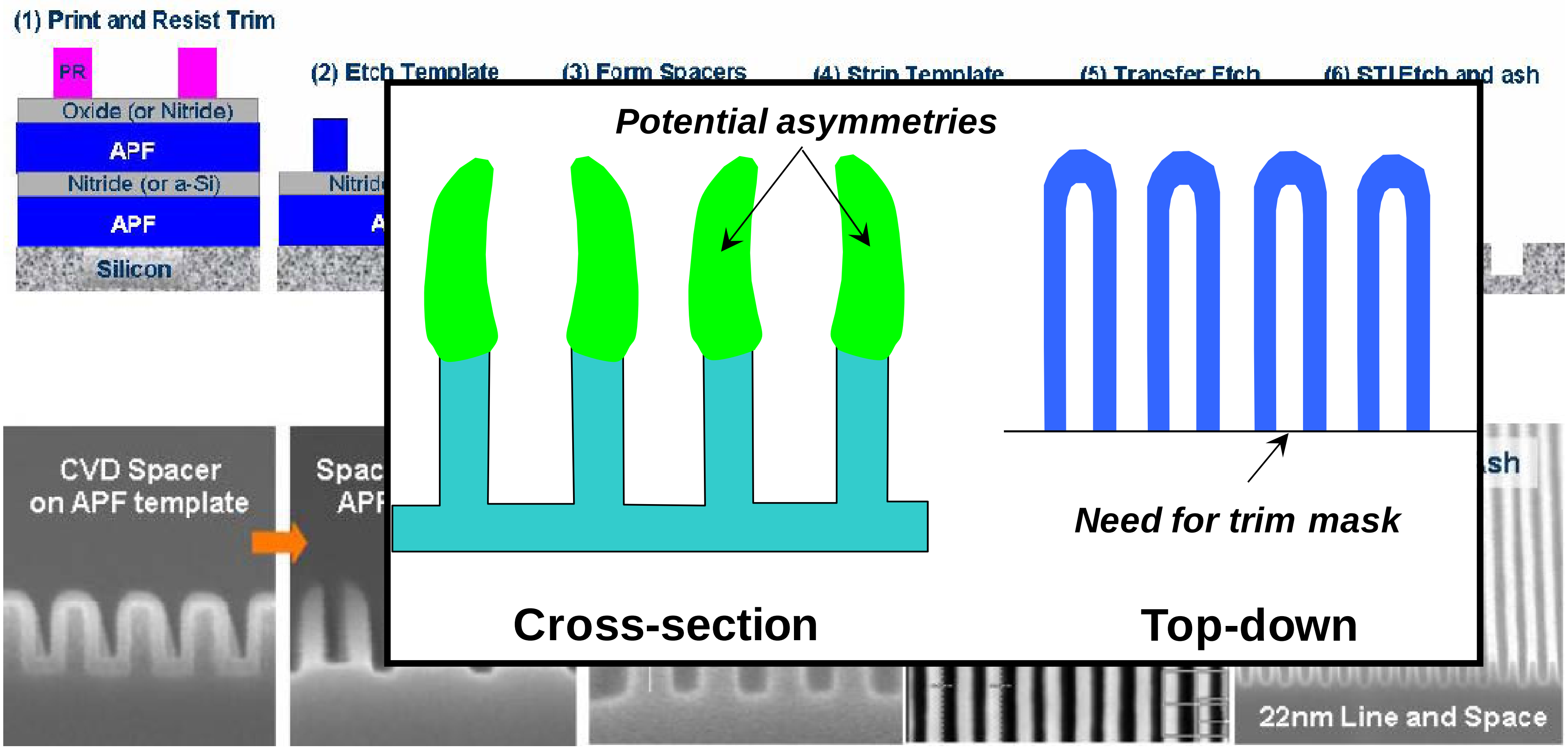


Spacer patterning retains correlation between doubled features

Bencher et al, Patterning by CVD Spacer Self Alignment DoublePatterning (SADP), Proc. of SPIE Vol. 6924 69244E-7

Alternative: Spacer patterning





However spacer patterning comes with challenges of its own

Bencher et al, Patterning by CVD Spacer Self Alignment DoublePatterning (SADP), Proc. of SPIE Vol. 6924 69244E-7

AGENDA

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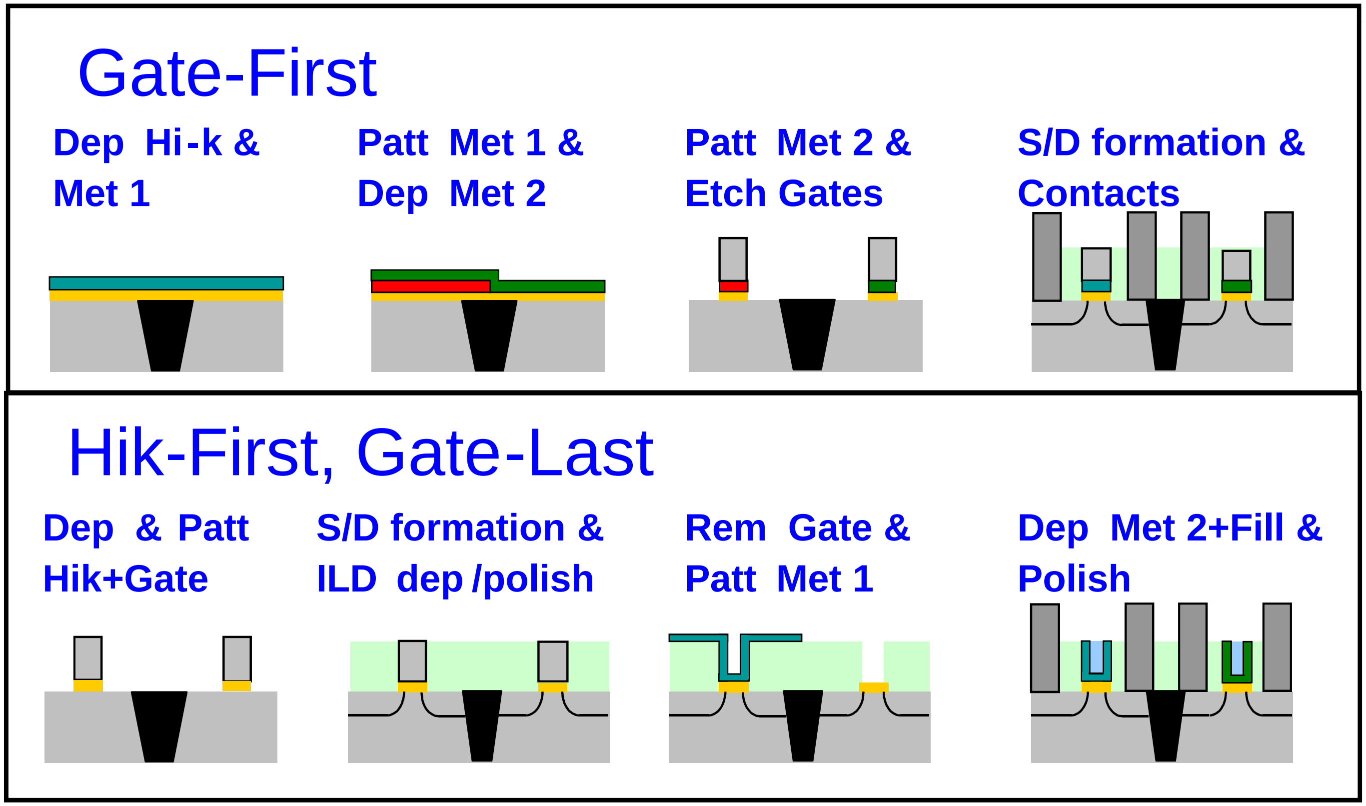
HiK-MG: Gate First vs Gate Last



Gate-First

Dep Hi-k & Met 1

Patt Met 1 & Dep Met 2

Patt Met 2 & Etch Gates

S/D formation & Contacts

Hik-First, Gate-Last

Dep & Patt Hik+Gate

S/D formation & ILD dep /polish

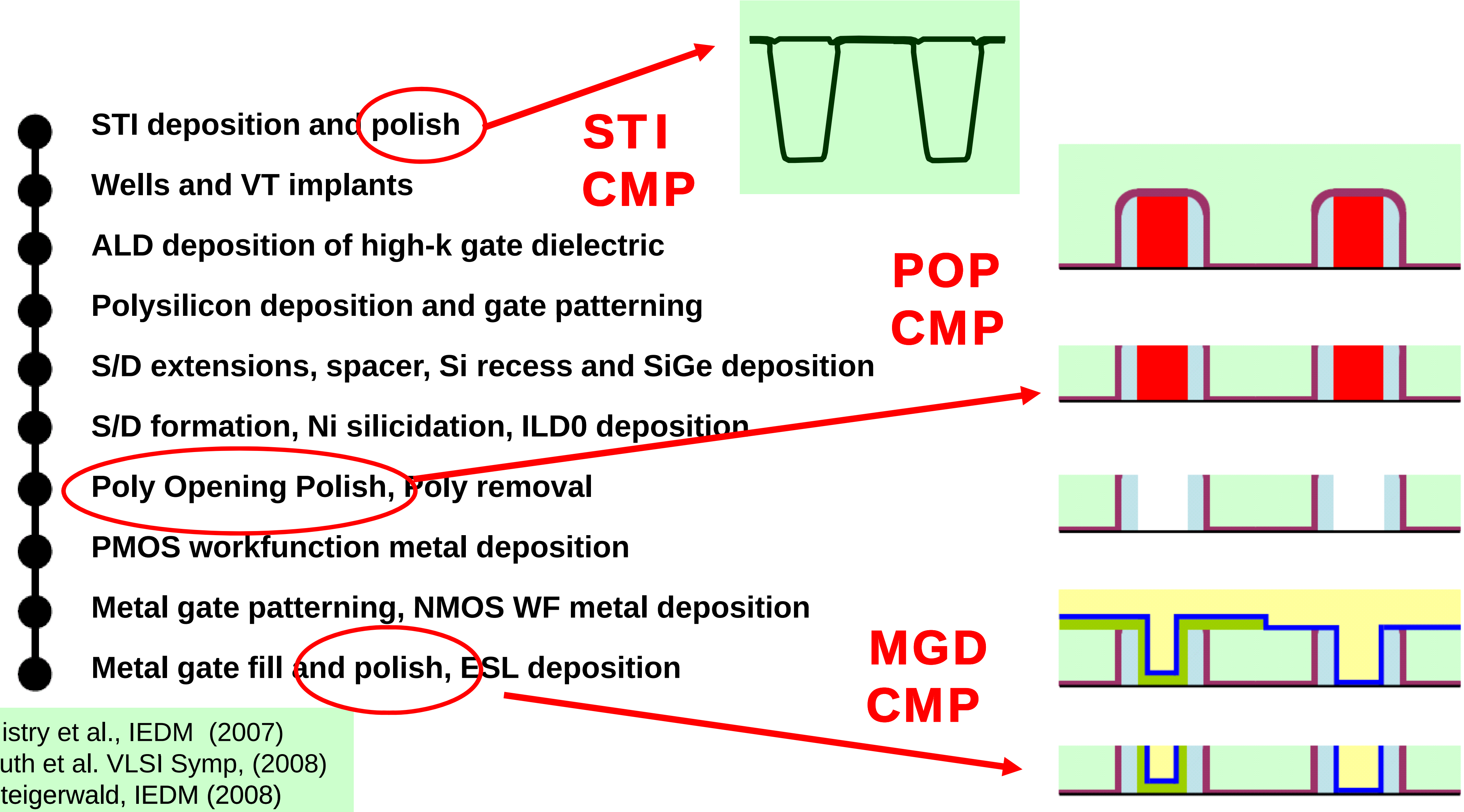
Rem Gate & Patt Met 1

Dep Met 2+Fill & Polish

Advantages of gate last flow

- **High Thermal budget available for Midsection**
  - Better Activation of S/D Implants
- **Low thermal budget for Metal Gate**
  - Large range of Gate Materials available
- **Significant enhancement of strain**
  - Both NMOS and PMOS benefit

CMP Integration at 45 nm – HiK Metal Gate



- STI deposition and polish
- Wells and VT implants
- ALD deposition of high-k gate dielectric
- Polysilicon deposition and gate patterning
- S/D extensions, spacer, Si recess and SiGe deposition
- S/D formation, Ni silicidation, ILD0 deposition
- Poly Opening Polish, Poly removal
- PMOS workfunction metal deposition
- Metal gate patterning, NMOS WF metal deposition
- Metal gate fill and polish, ESL deposition

K.Mistry et al., IEDM (2007)
C.Auth et al. VLSI Symp, (2008)
J. Steigerwald, IEDM (2008)

First Generation HiK – Replacement Metal Gate
Three critical CMP operations in the FE

CMP Integration at 45 nm – HiK Metal Gate

- **STI deposition and polish**
- Wells and VT implants
- ALD deposition of high-k gate dielectric
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- S/D extensions, spacer, Si recess and SiGe deposition
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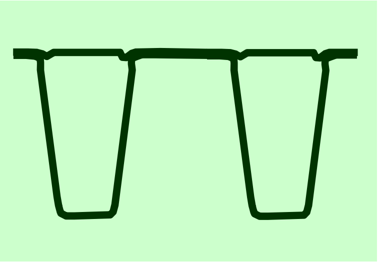
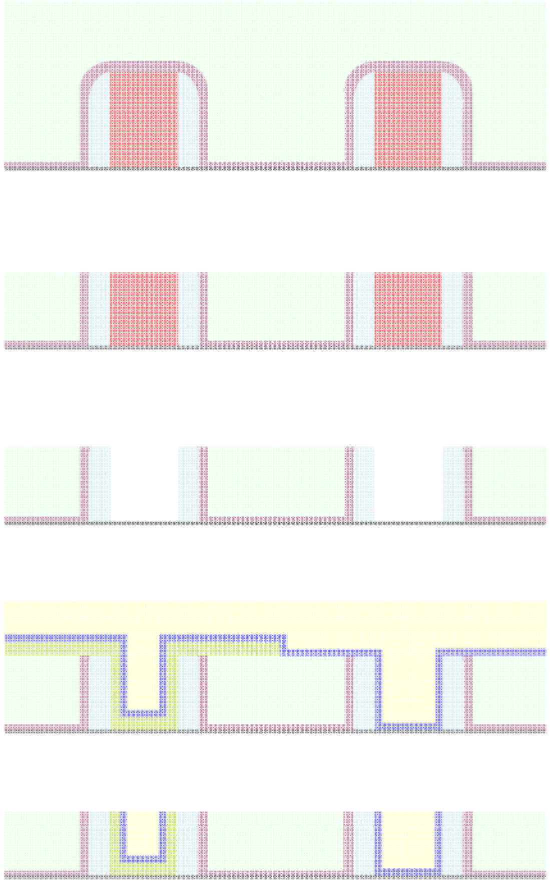
STI CMP



POP CMP

MGD CMP



K.Mistry et al., IEDM (2007)
C.Auth et al. VLSI Symp, (2008)
J. Steigerwald, IEDM (2008)

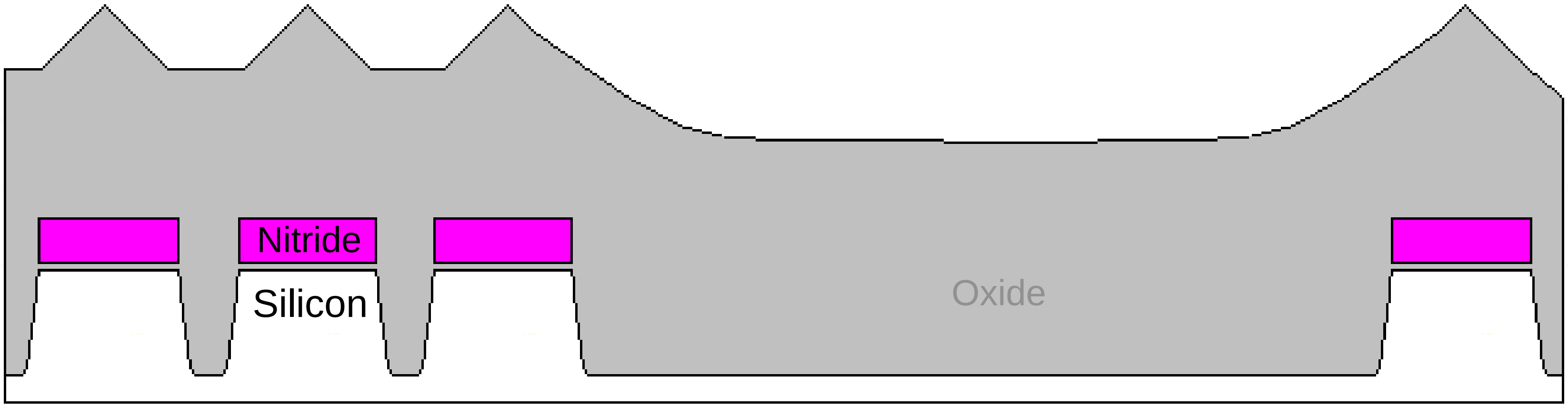
First Generation HiK – Replacement Metal Gate
Three critical CMP operations in the FE

STR Pattern Density Variation Impact

High Pattern Density

Low Pattern Density

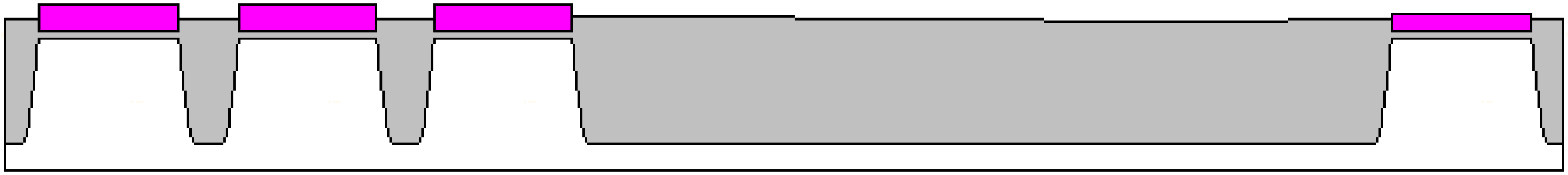
Post STI
Deposition



Slower Polish Rate

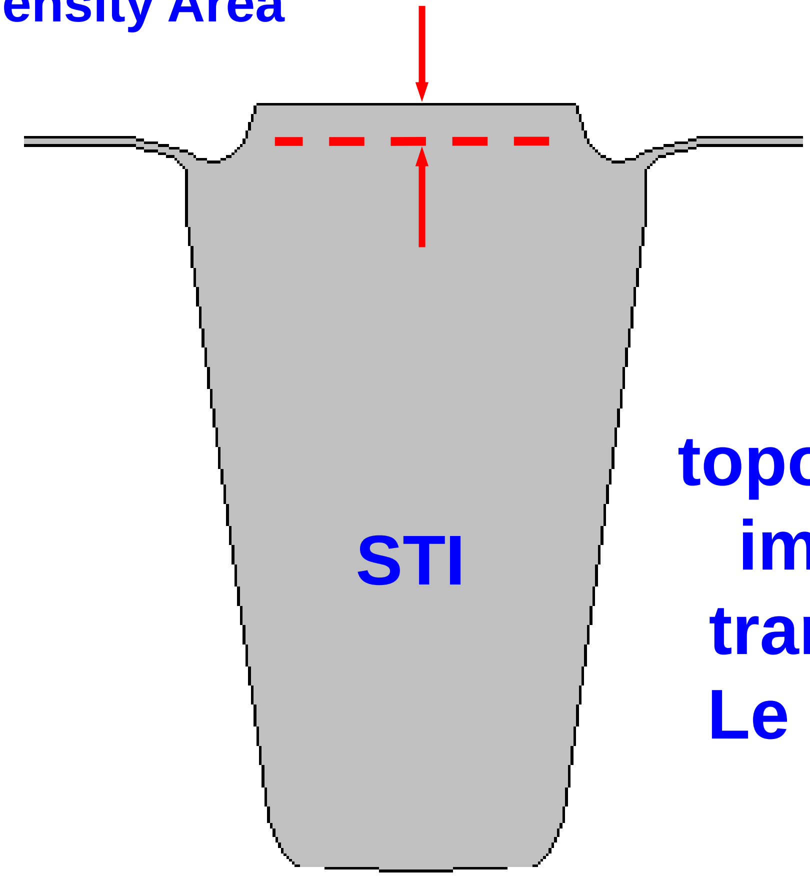
Faster Polish Rate

Post STI
Polish



STI Step Height Variation

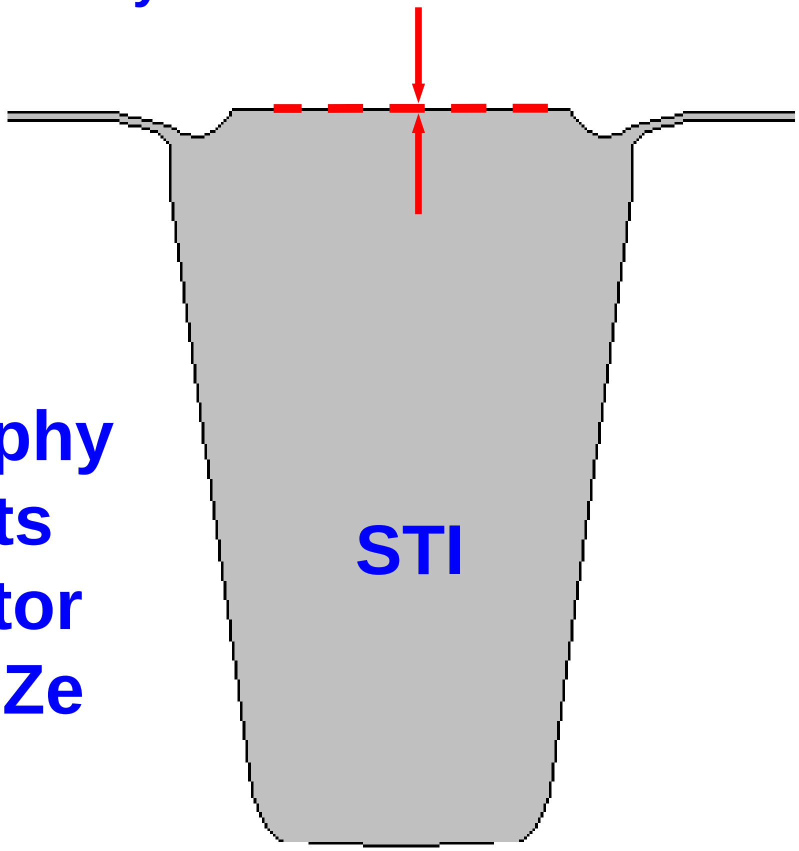
High Pattern Density Area



Positive Step Height

STI topography impacts transistor Le and Ze

Low Pattern Density Area

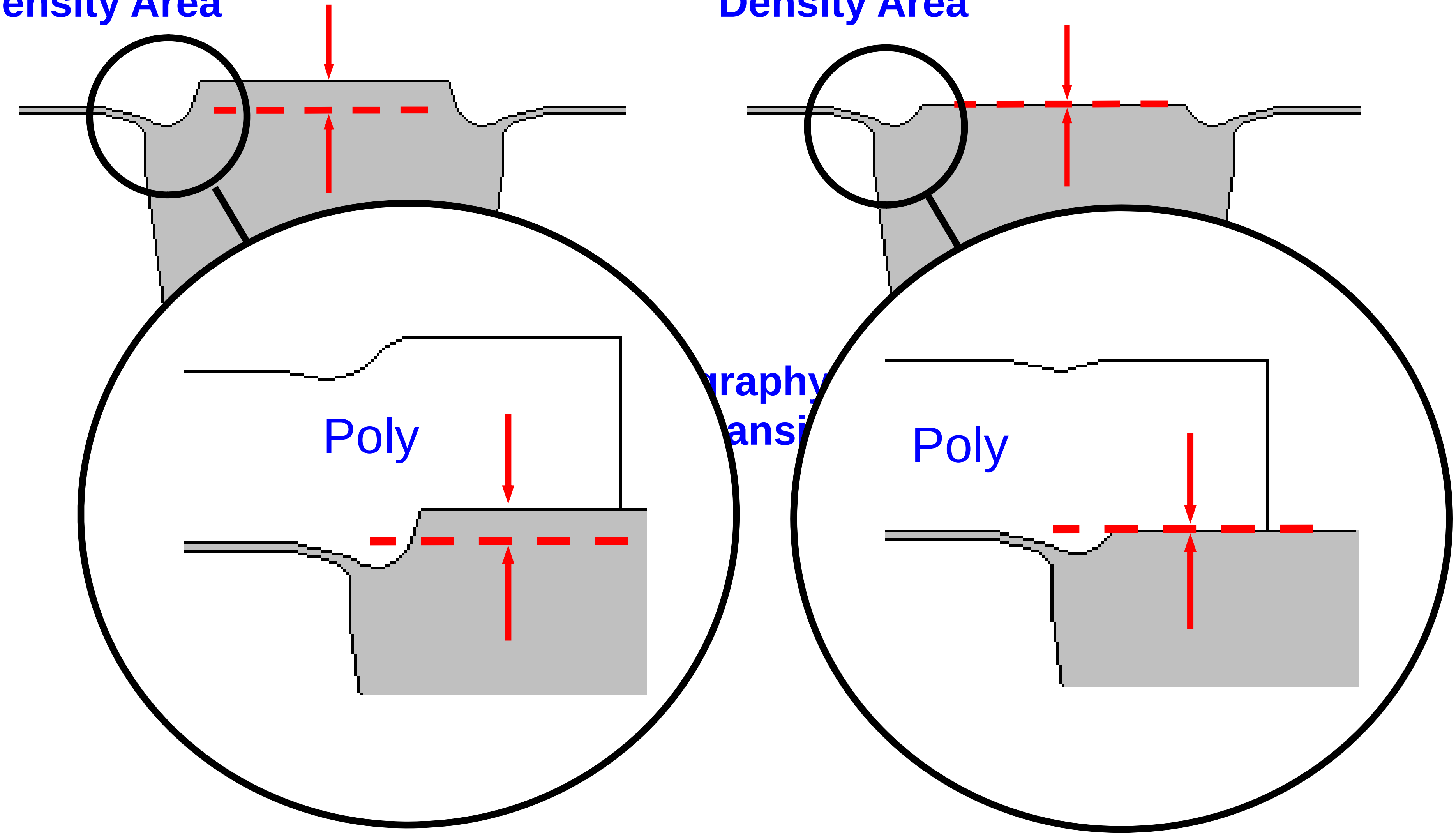


Zero Step Height

STI Step Height Variation

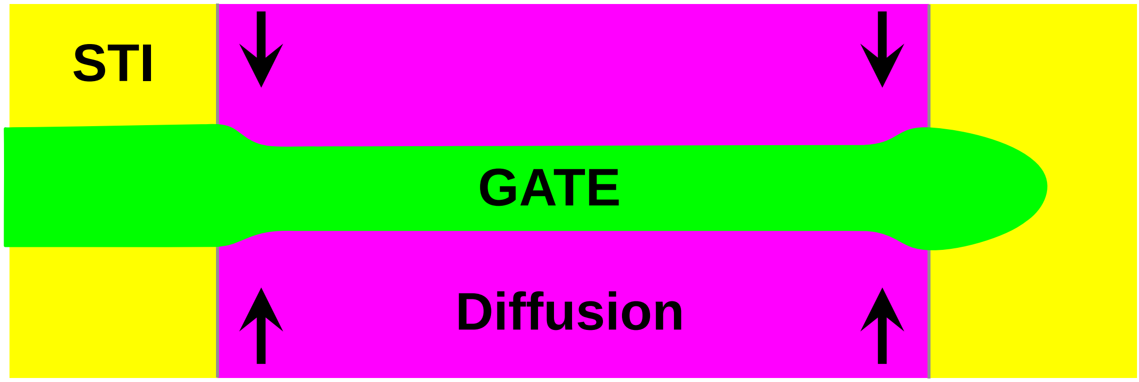
High Pattern Density Area

Low Pattern Density Area



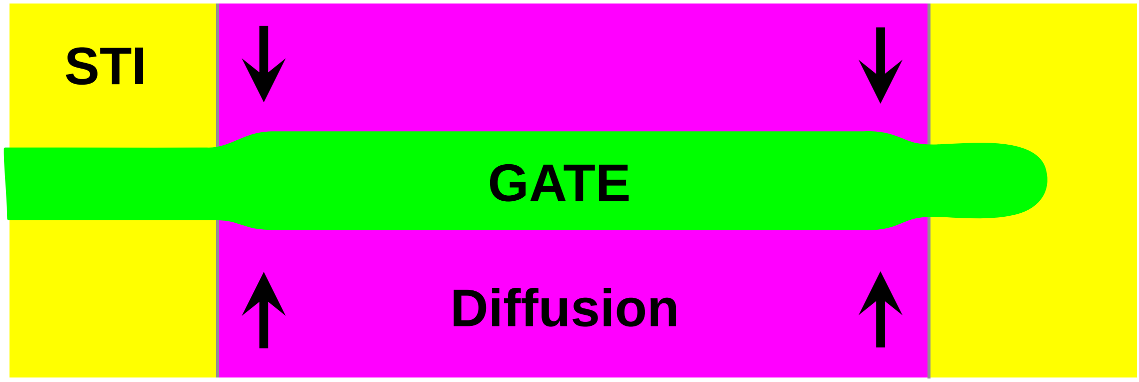
STI Step Height Impact on Gate CD

Negative
Step Height



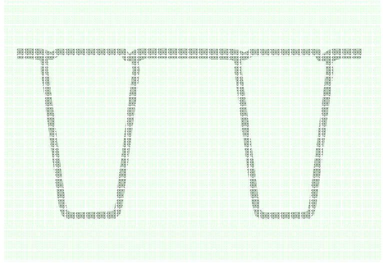
“Dogbone”
Lg is longer at the diffusion boundary

Positive
Step Height



“Icicle”
Gate CD is shorter at the diffusion boundary

CMP Integration at 45 nm – HiK Metal Gate



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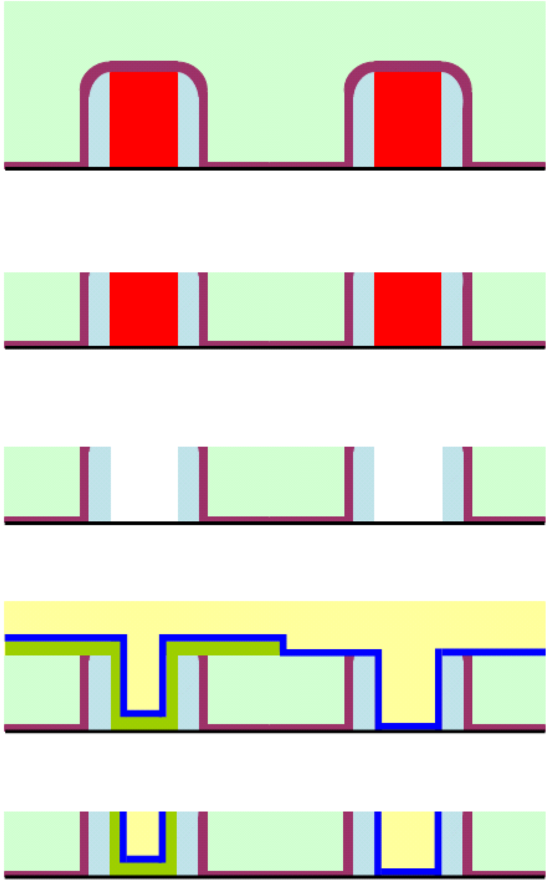
STI CMP

POP CMP

MGD CMP

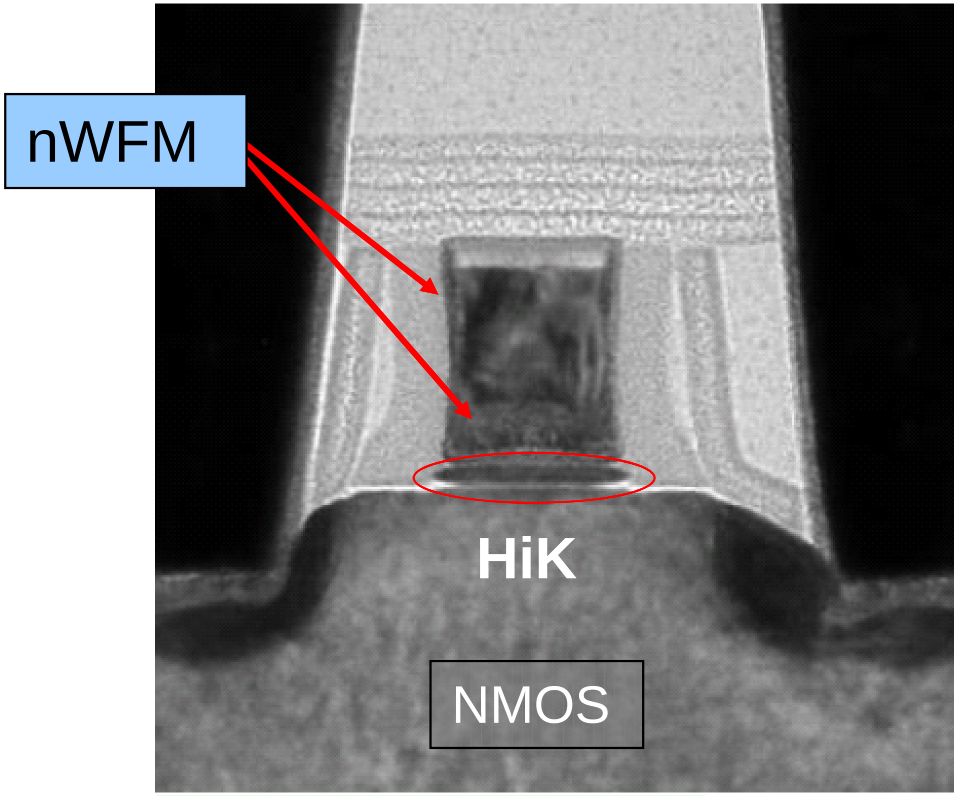


K.Mistry et al., IEDM (2007)
C.Auth et al. VLSI Symp, (2008)
J. Steigerwald, IEDM (2008)

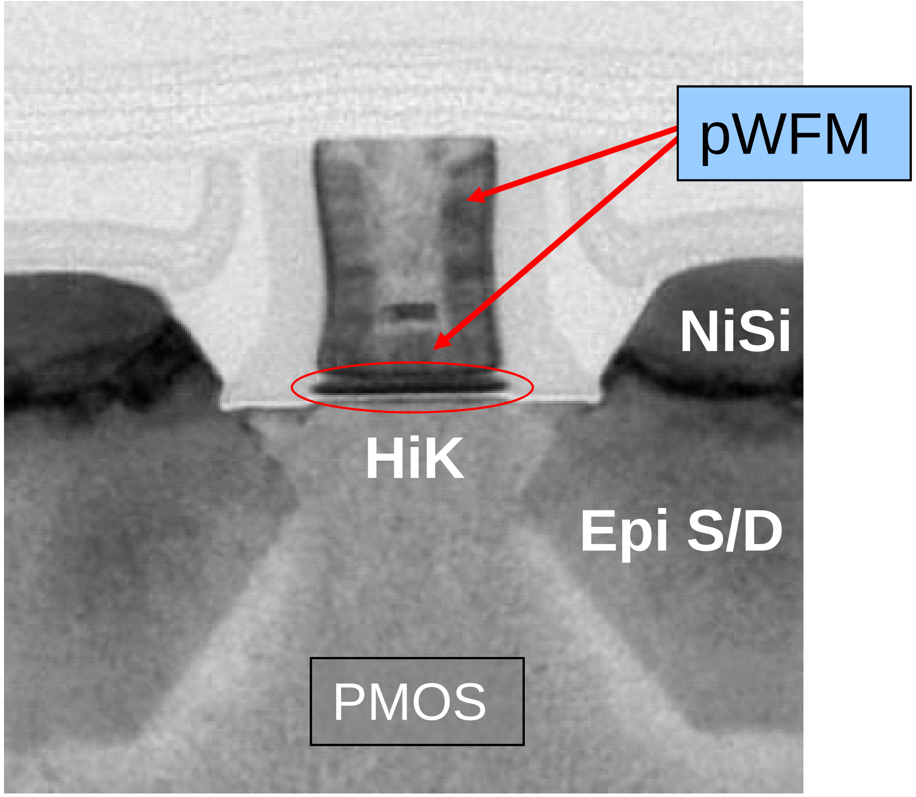
First Generation HiK – Replacement Metal Gate
Three critical CMP operations in the FE

Variation Challenges of RMG CMP Steps

- **Gate height control critical to reducing variation**
- **PMOS/NMOS differences complicate CMP**



C.Auth et al. VLSI Symp, (2008)



J. Steigerwald, IEDM 2008

Variation Challenges of RMG CMP Steps

OVERPOLISH

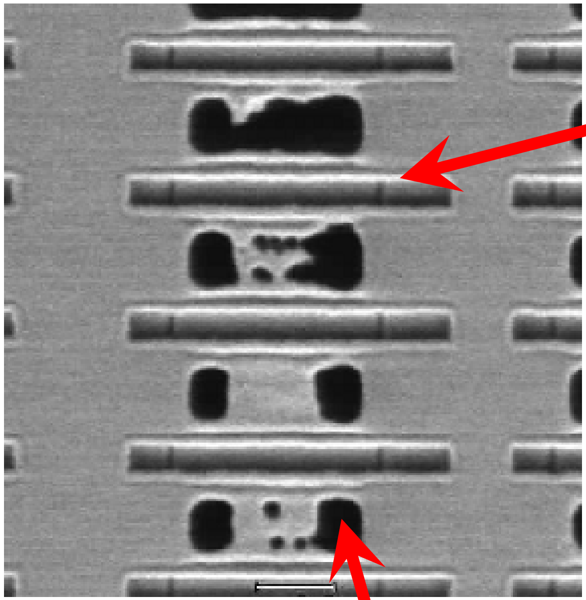
Exposes raised S/D

Rext/mobility impact

UNDERPOLISH

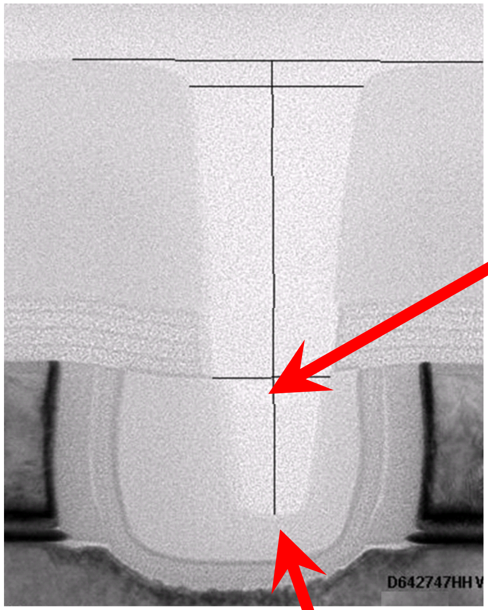
Underetched contact

Rext impact



Gate region

S/D region – attacked during poly etch



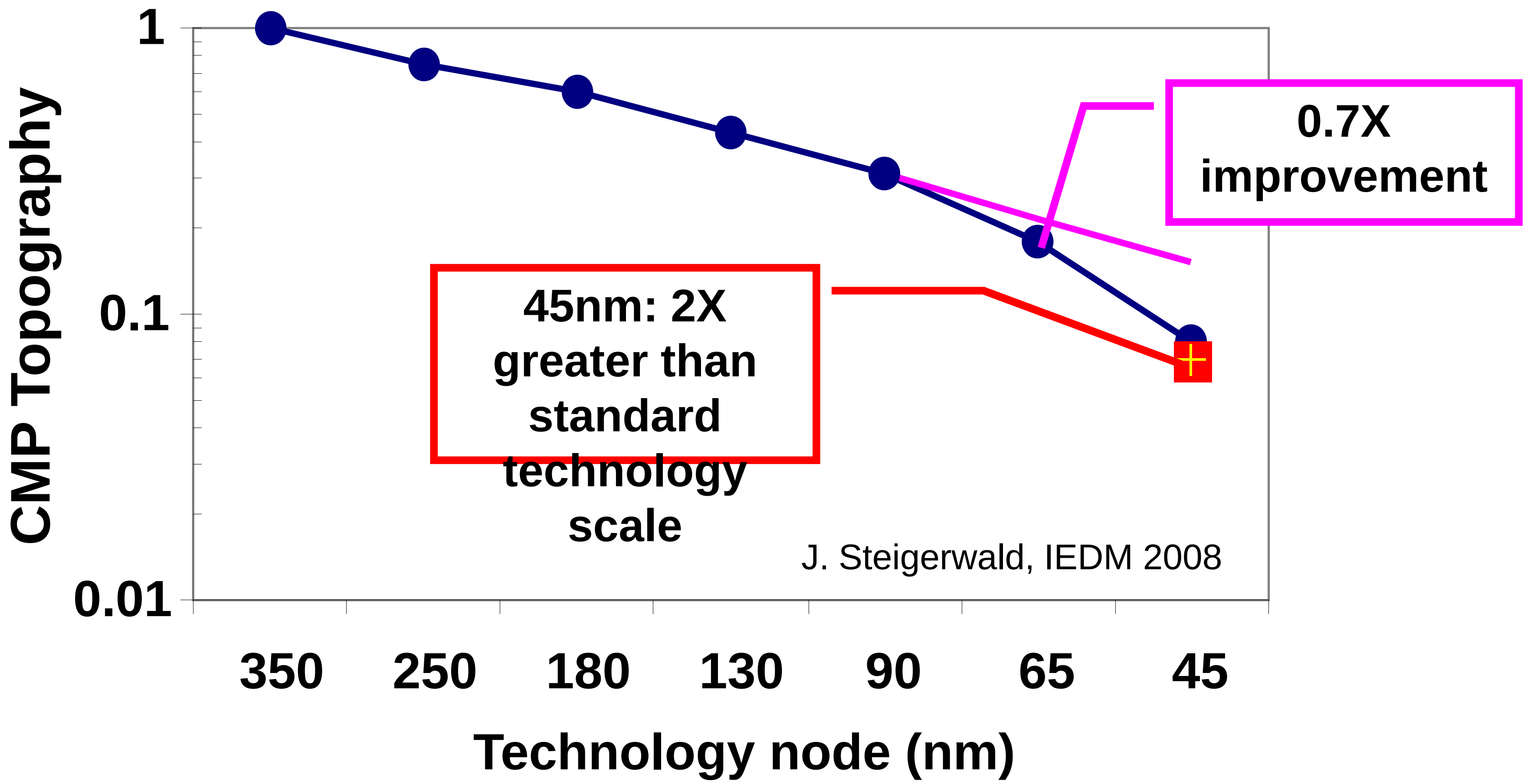
NMOS S/D region contact

S/D region – marginal contact

J. Steigerwald, IEDM 2008

45 nm: POP CMP Improvement

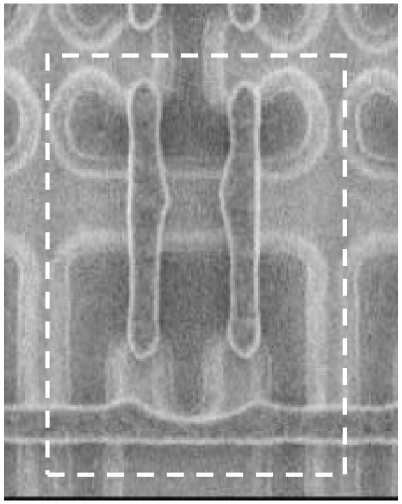
Overscaling Topography Improvement



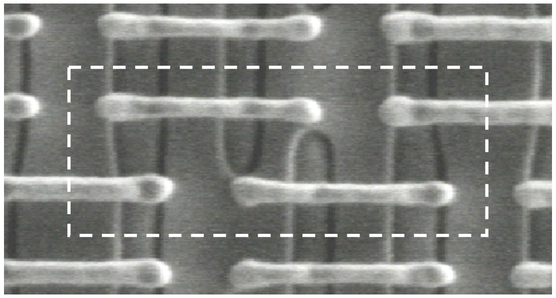
J. Steigerwald, IEDM 2008

Improvements in polish enabled dramatic improvements in topography variation

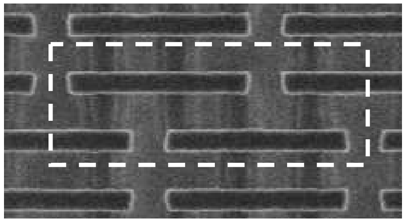
Generational Improvements
Patterning and Polish



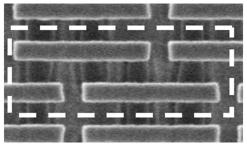
90nm – TALL
1.0 μm^2



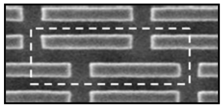
65nm – WIDE - 0.57 μm^2



45nm – WIDE
0.346 μm^2



32nm – WIDE
0.171 μm^2



22nm – WIDE
0.092 μm^2

65nm to 22nm: Patterning and polish enhancements

- Improved CD uniformity across STI boundaries
- Square corners (eliminate “dogbone” and “icicle” corners)

AGENDA

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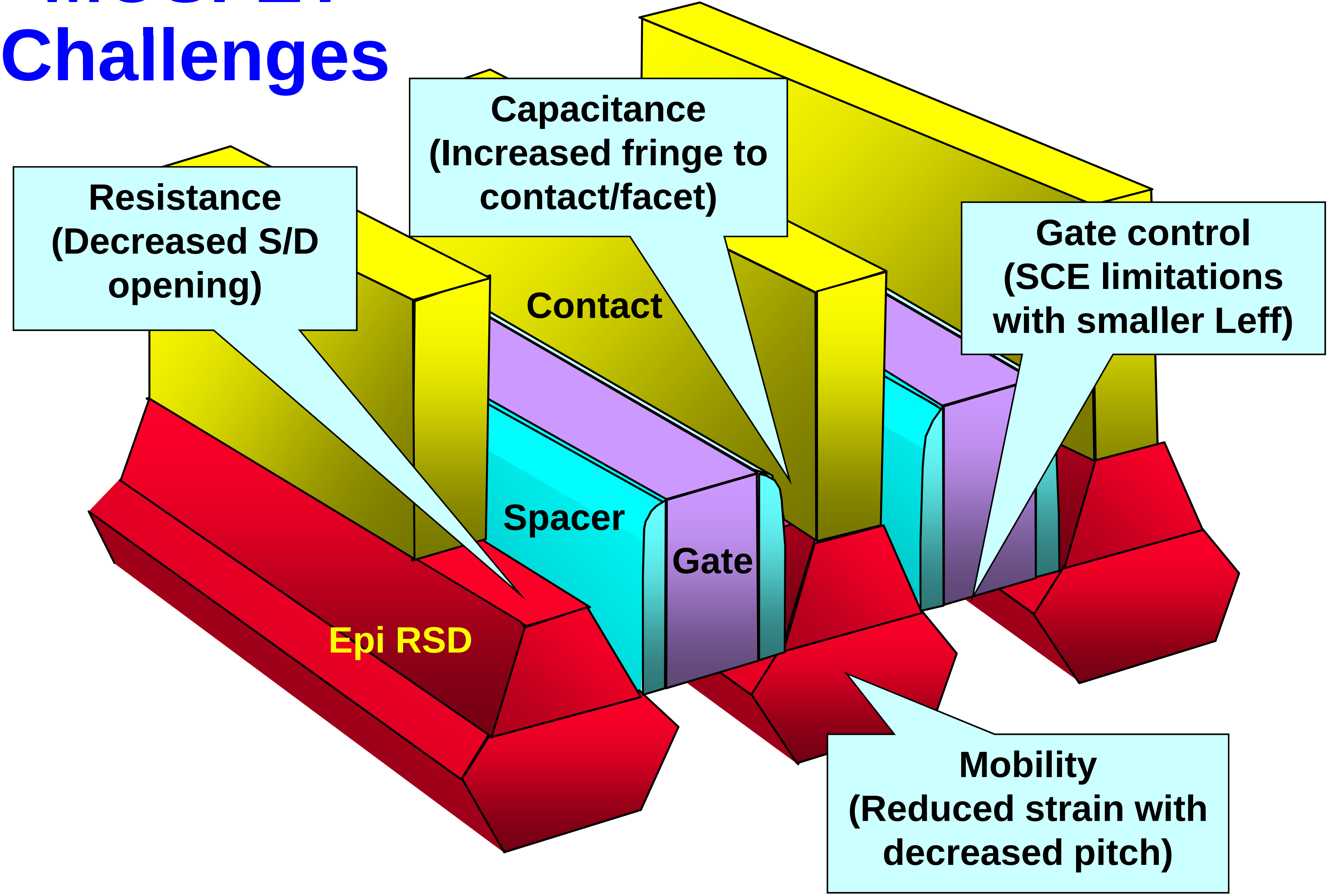
MOSFET Challenges



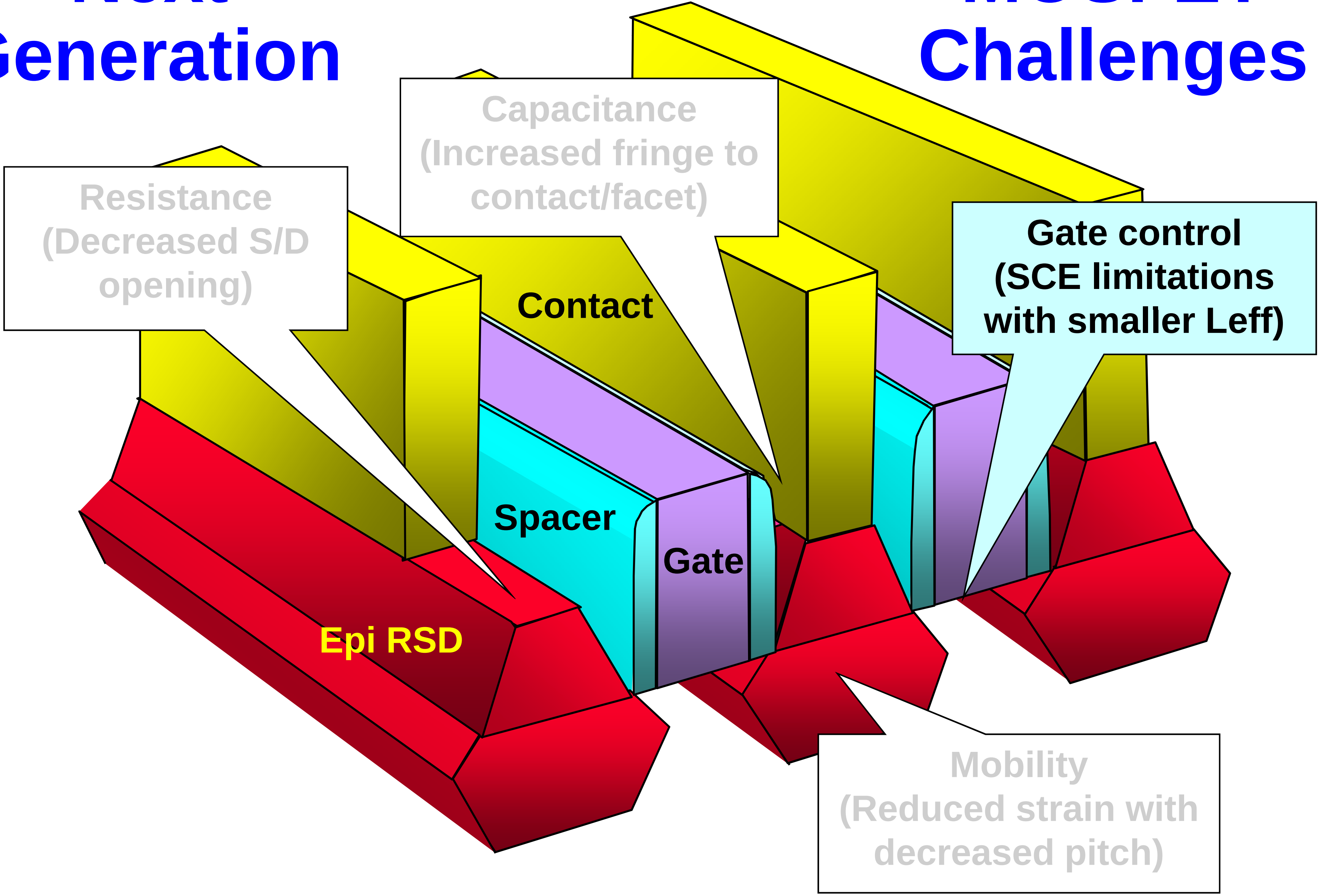
Resistance (Decreased S/D opening)

Capacitance (Increased fringe to contact/facet)

Gate control (SCE limitations with smaller Leff)

Mobility (Reduced strain with decreased pitch)

Next Generation MOSFET Challenges



Resistance (Decreased S/D opening)

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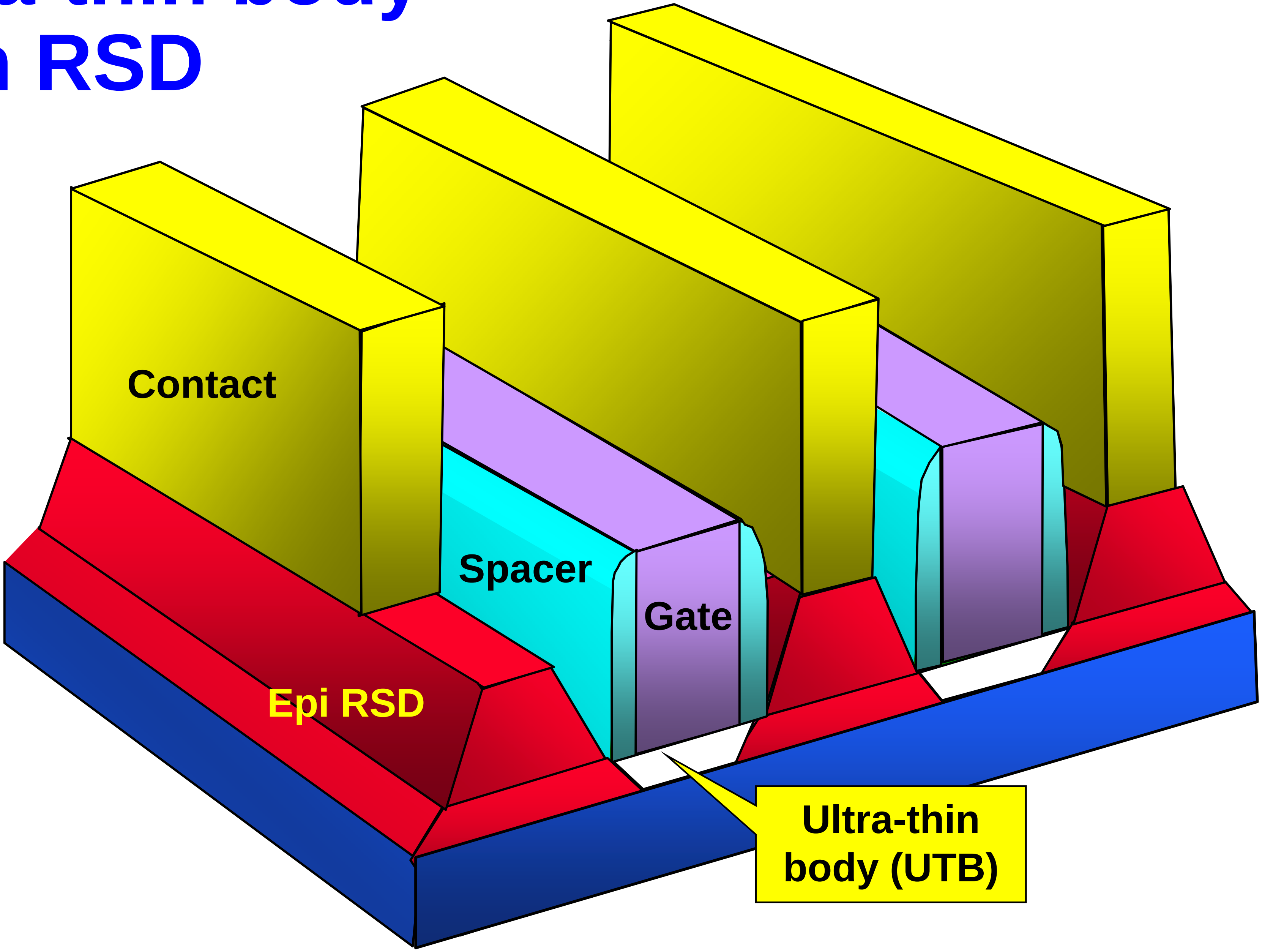
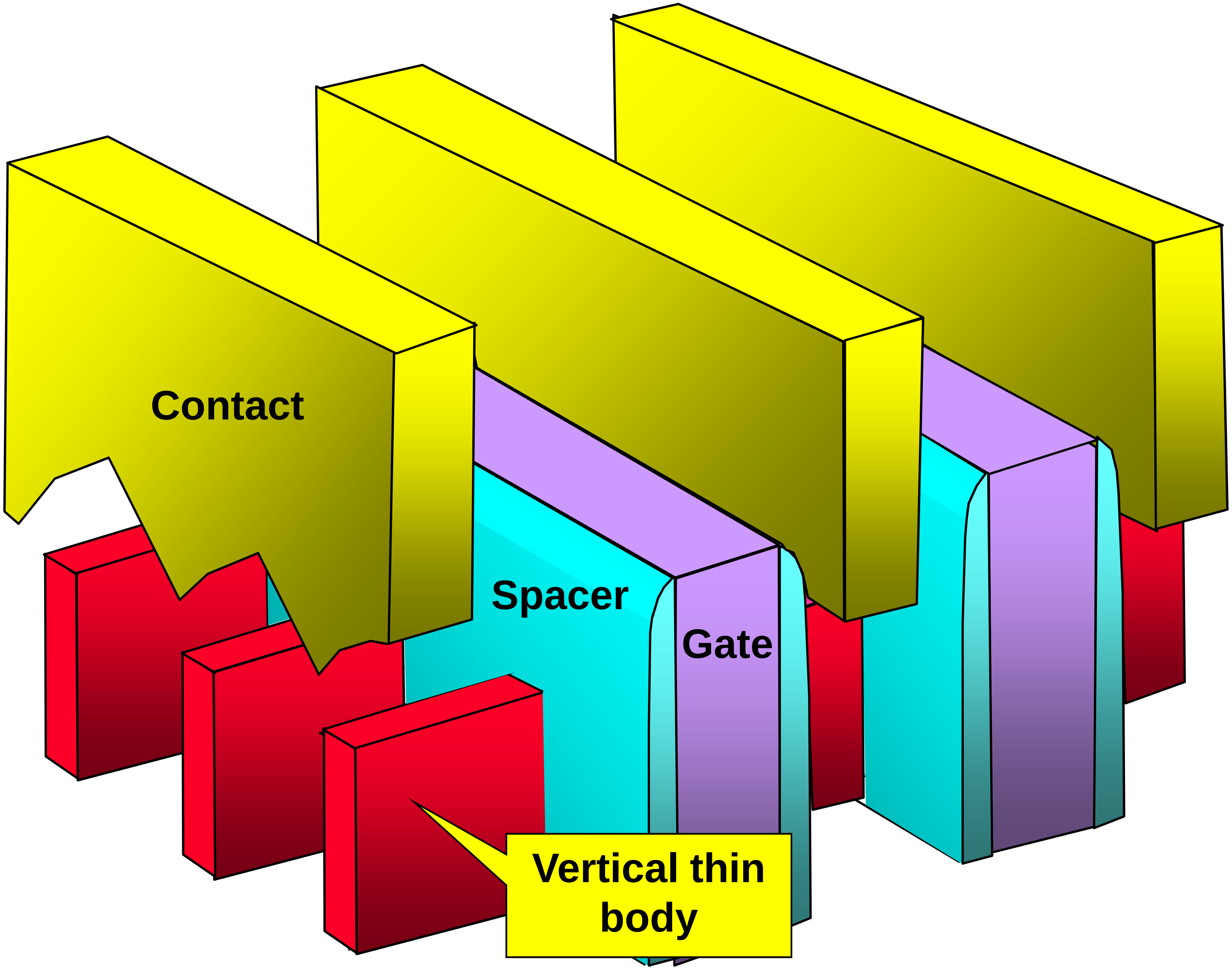
Ultra-thin body with RSD

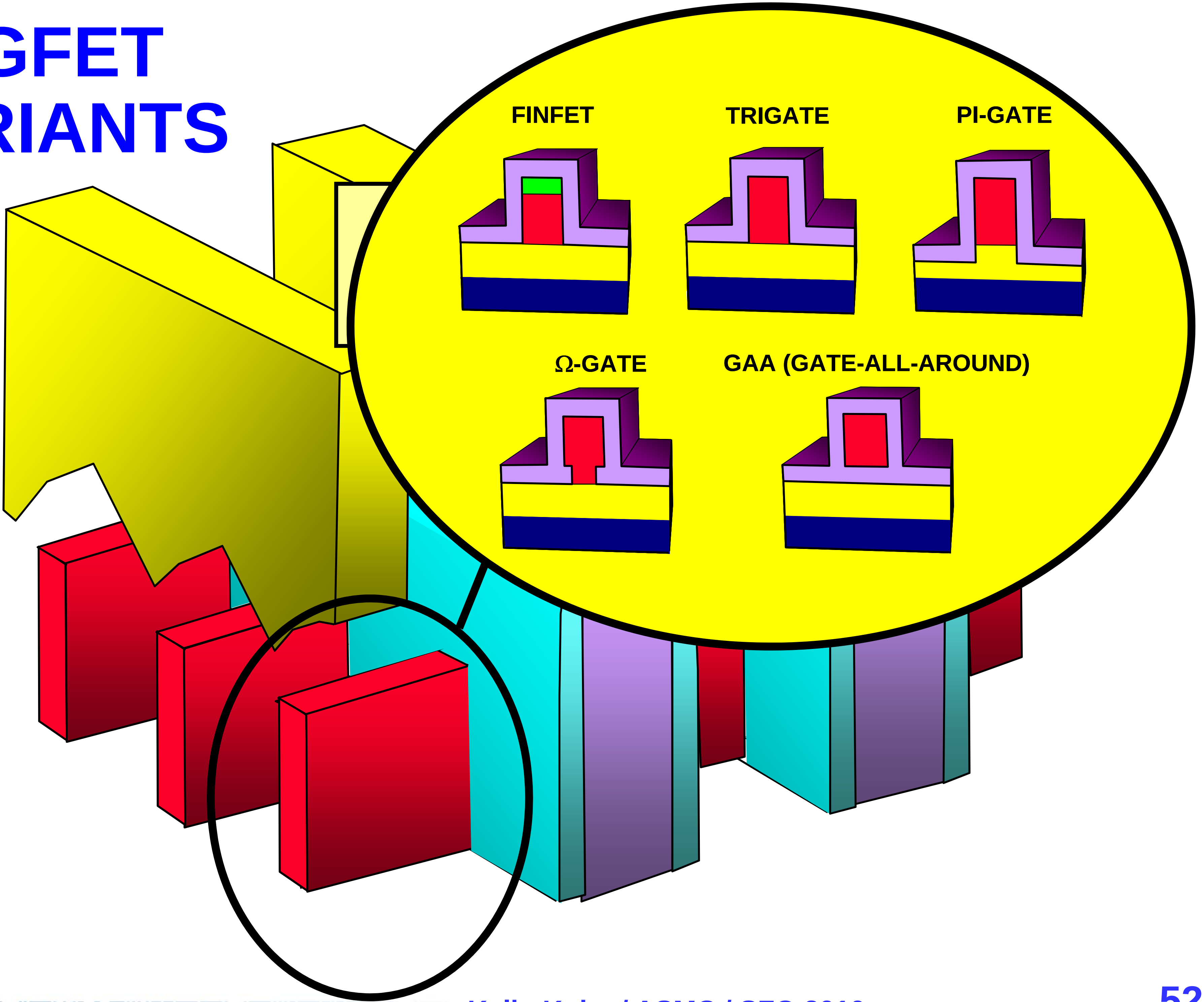


MuGFET

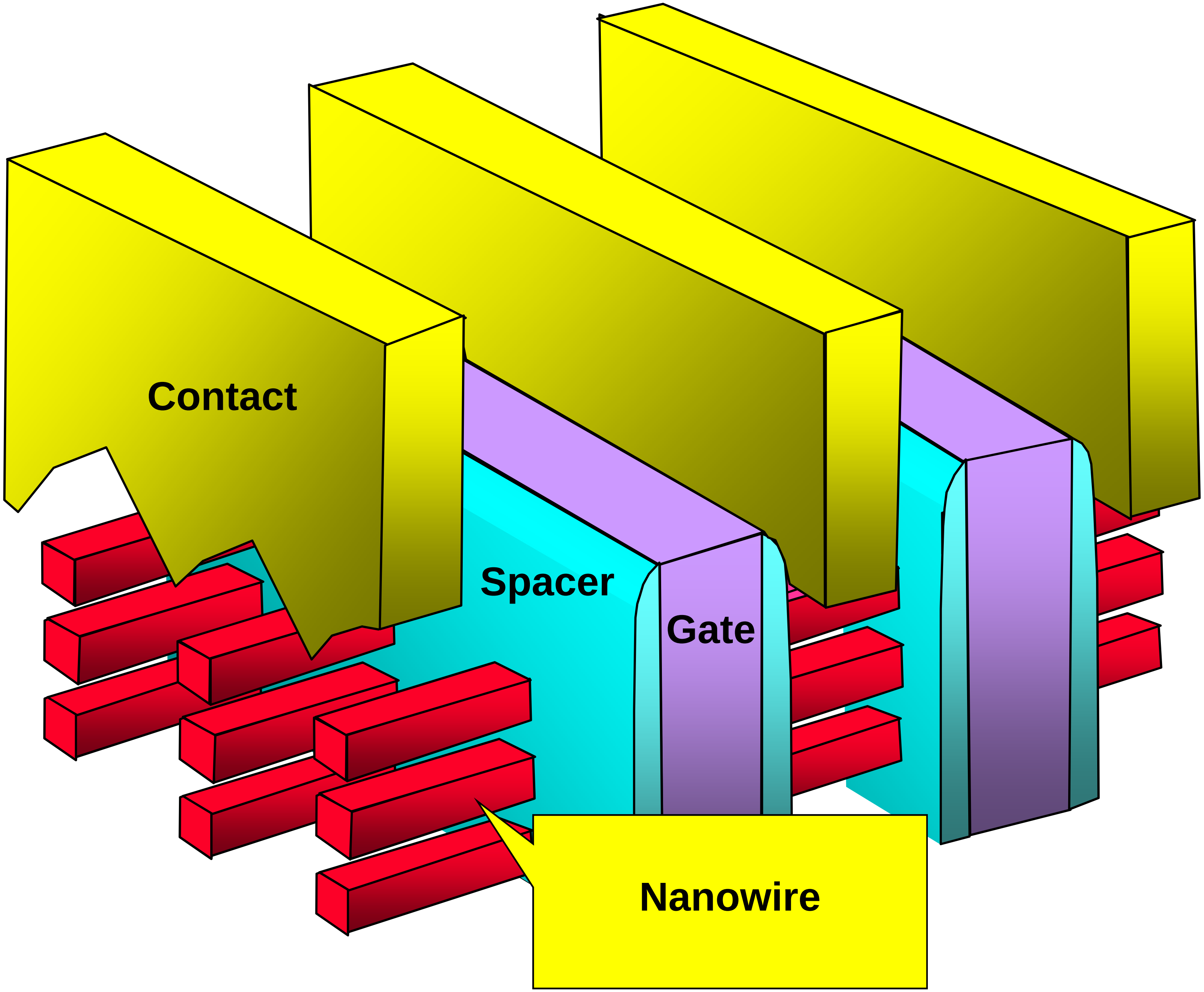


Vertical thin body

MuGFET VARIANTS



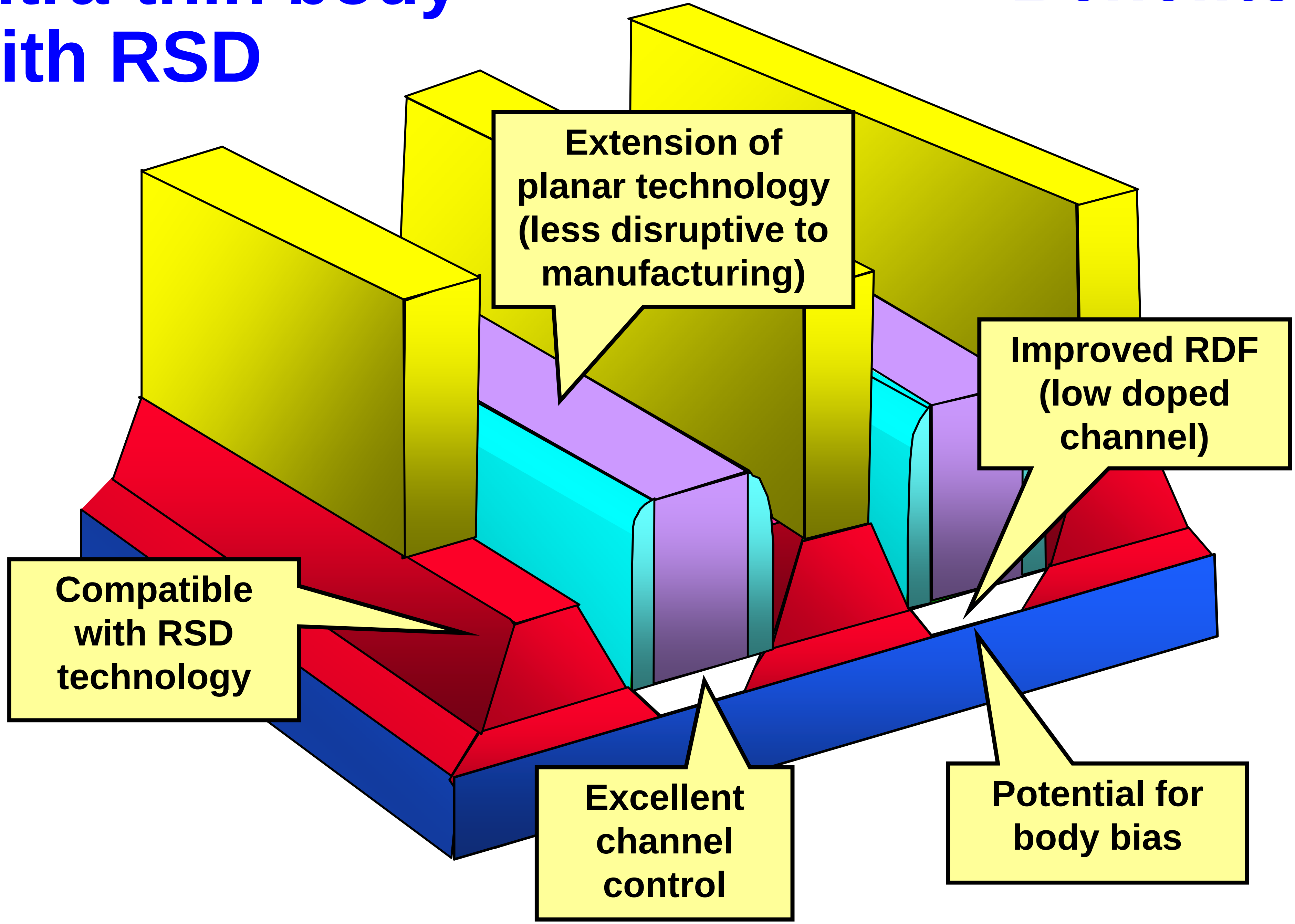
Nanowire



Looking at all these in more detail

Ultra-thin body with RSD

Benefits



Extension of planar technology (less disruptive to manufacturing)

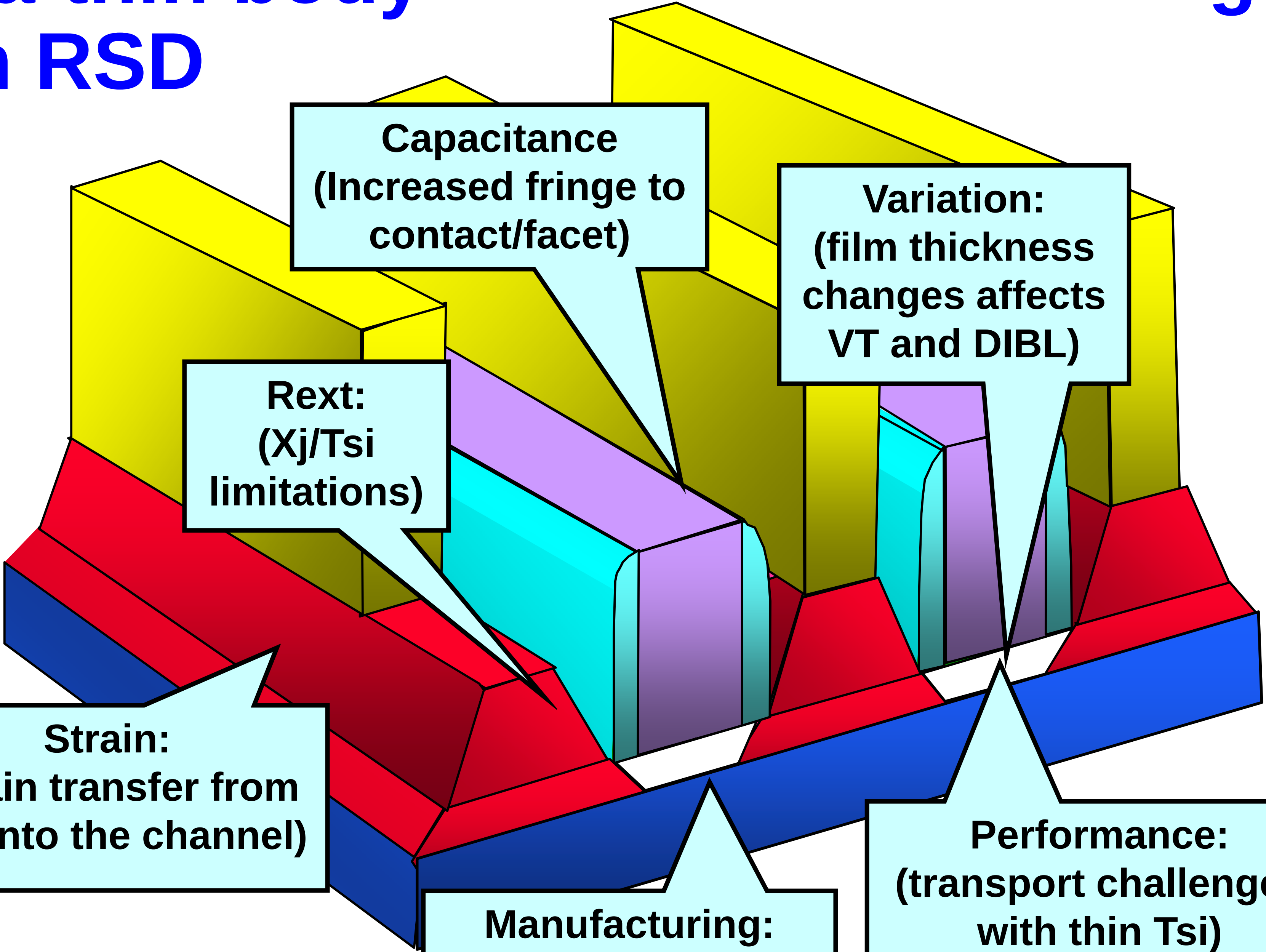
Improved RDF (low doped channel)

Compatible with RSD technology

Excellent channel control

Potential for body bias

Ultra-thin body with RSD Challenges



Capacitance:
(Increased fringe to contact/facet)

Variation:
(film thickness changes affects VT and DIBL)

Rext:
(Xj/Tsi limitations)

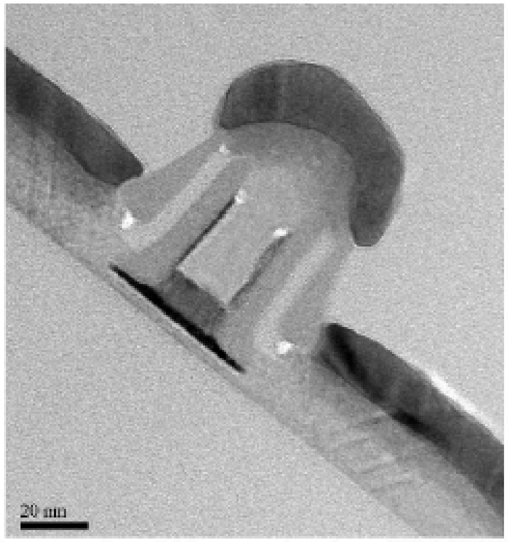
Strain:
(strain transfer from S/D into the channel)

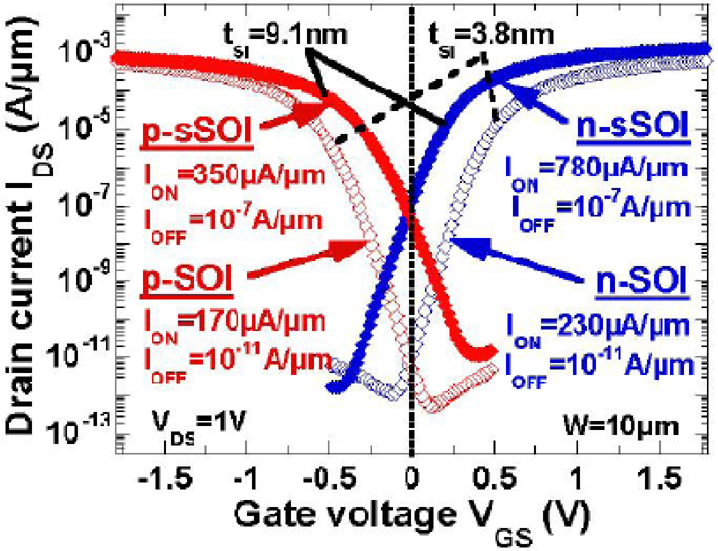
Performance:
(transport challenges with thin Tsi)

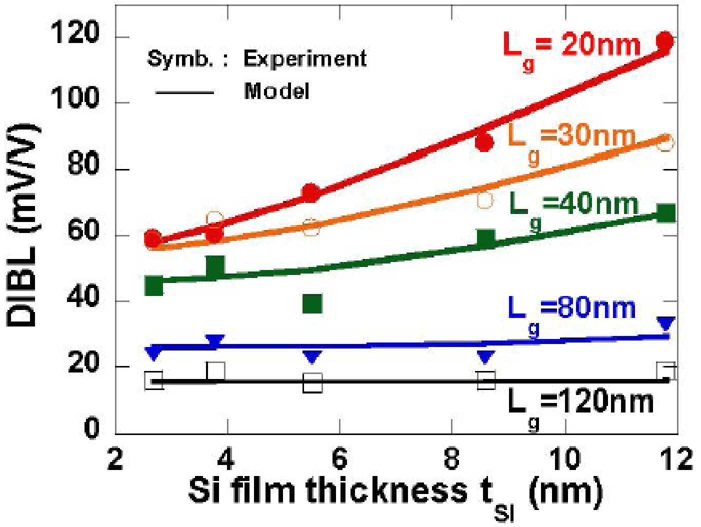
Manufacturing:
(requires both thin Tsi and thin BOX)

Ultra-thin body

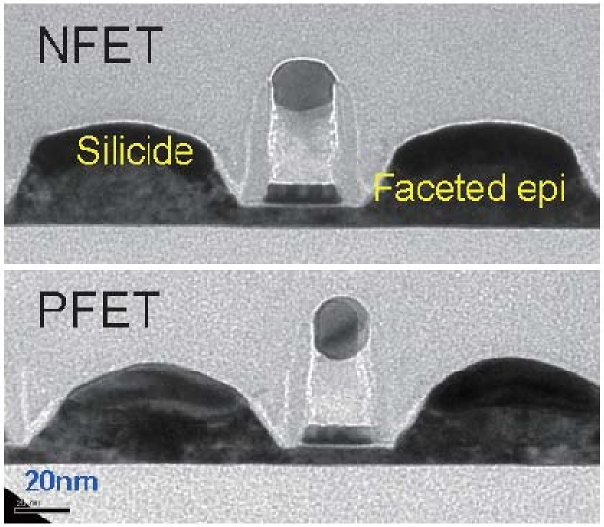
Barral – CEA-LETI– IEDM 2007

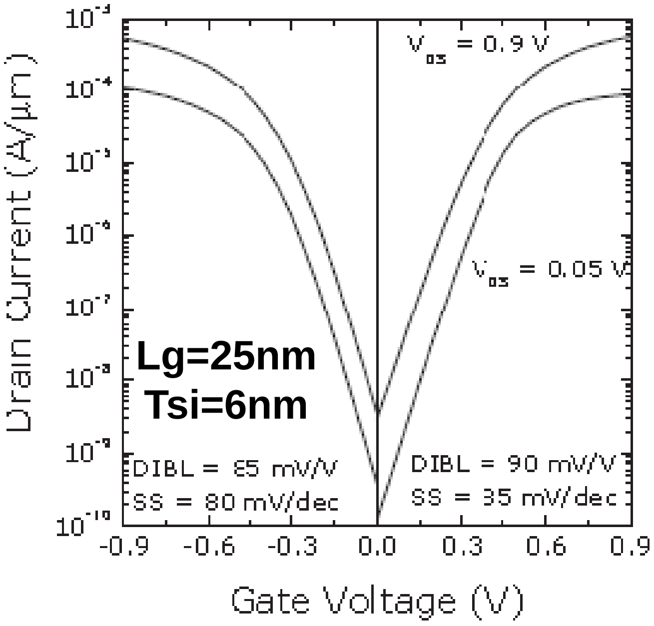


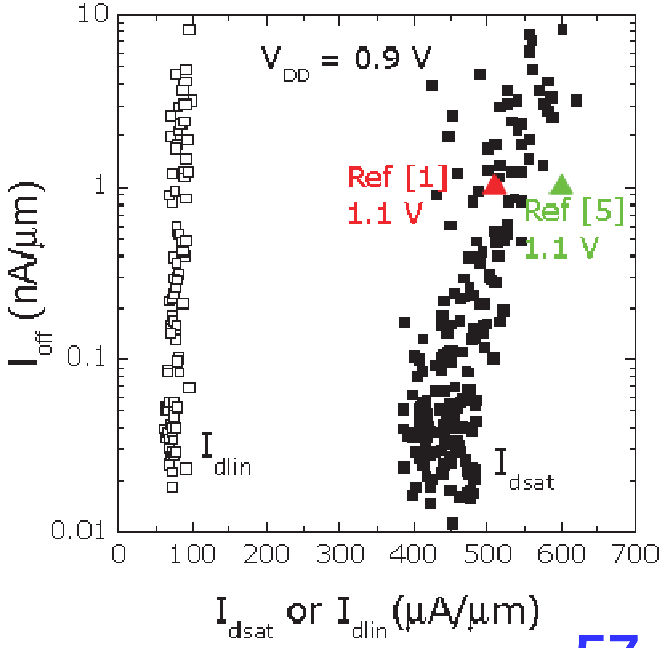




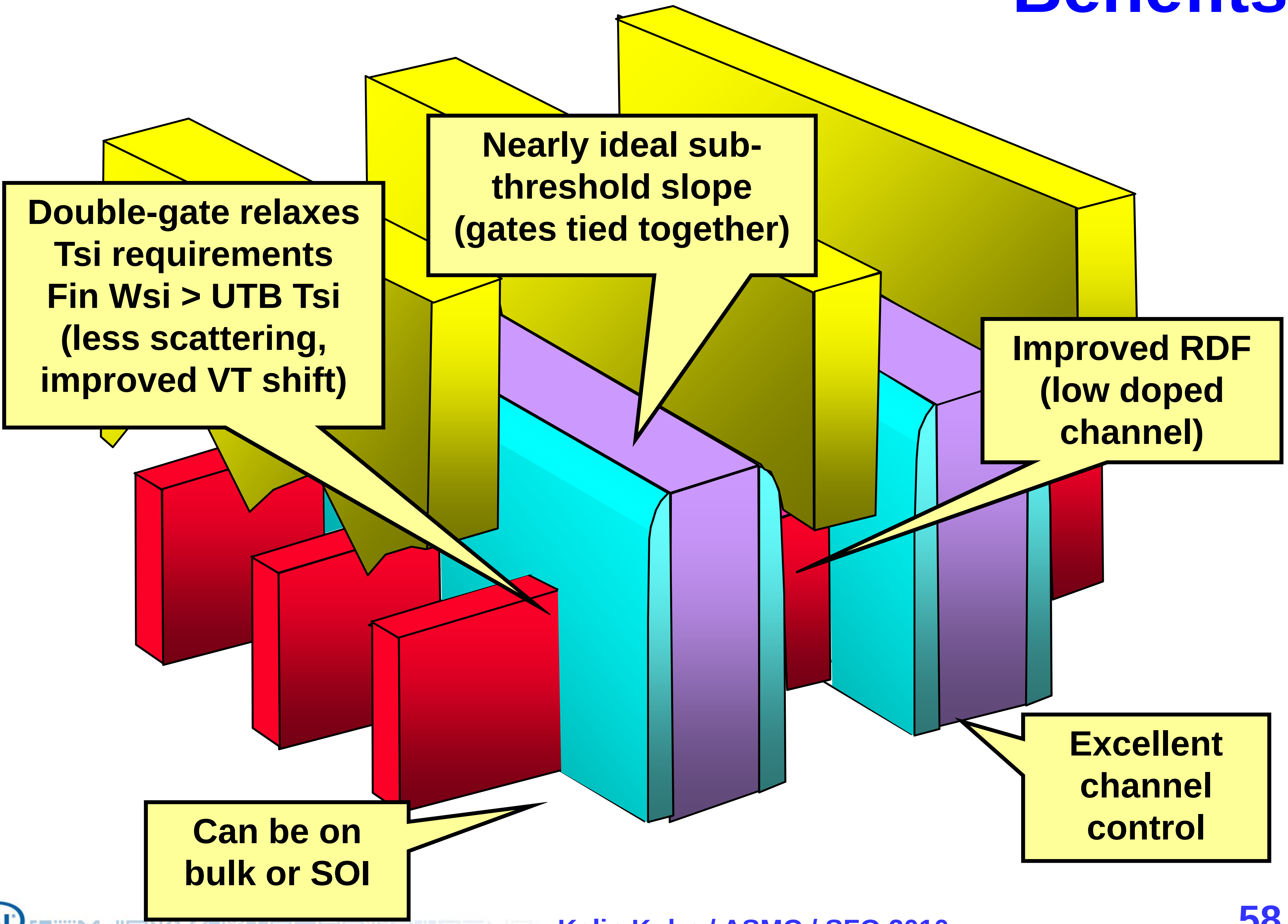
Cheng – IBM – VLSI 2009







MuGFET Benefits



Double-gate relaxes Tsi requirements Fin Wsi > UTB Tsi (less scattering, improved VT shift)

Nearly ideal sub-threshold slope (gates tied together)

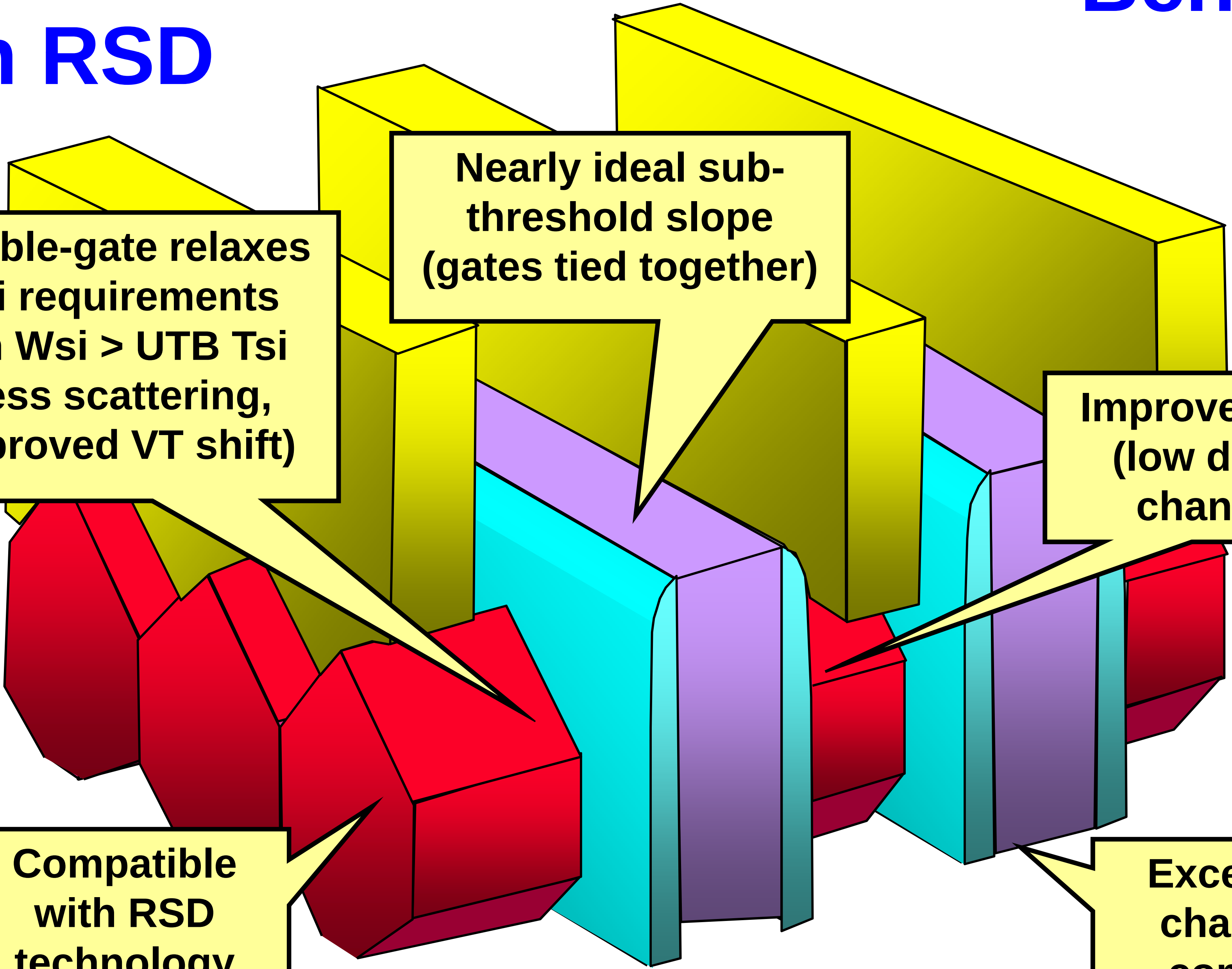
Improved RDF (low doped channel)

Excellent channel control

Can be on bulk or SOI

MuGFET with RSD

Benefits



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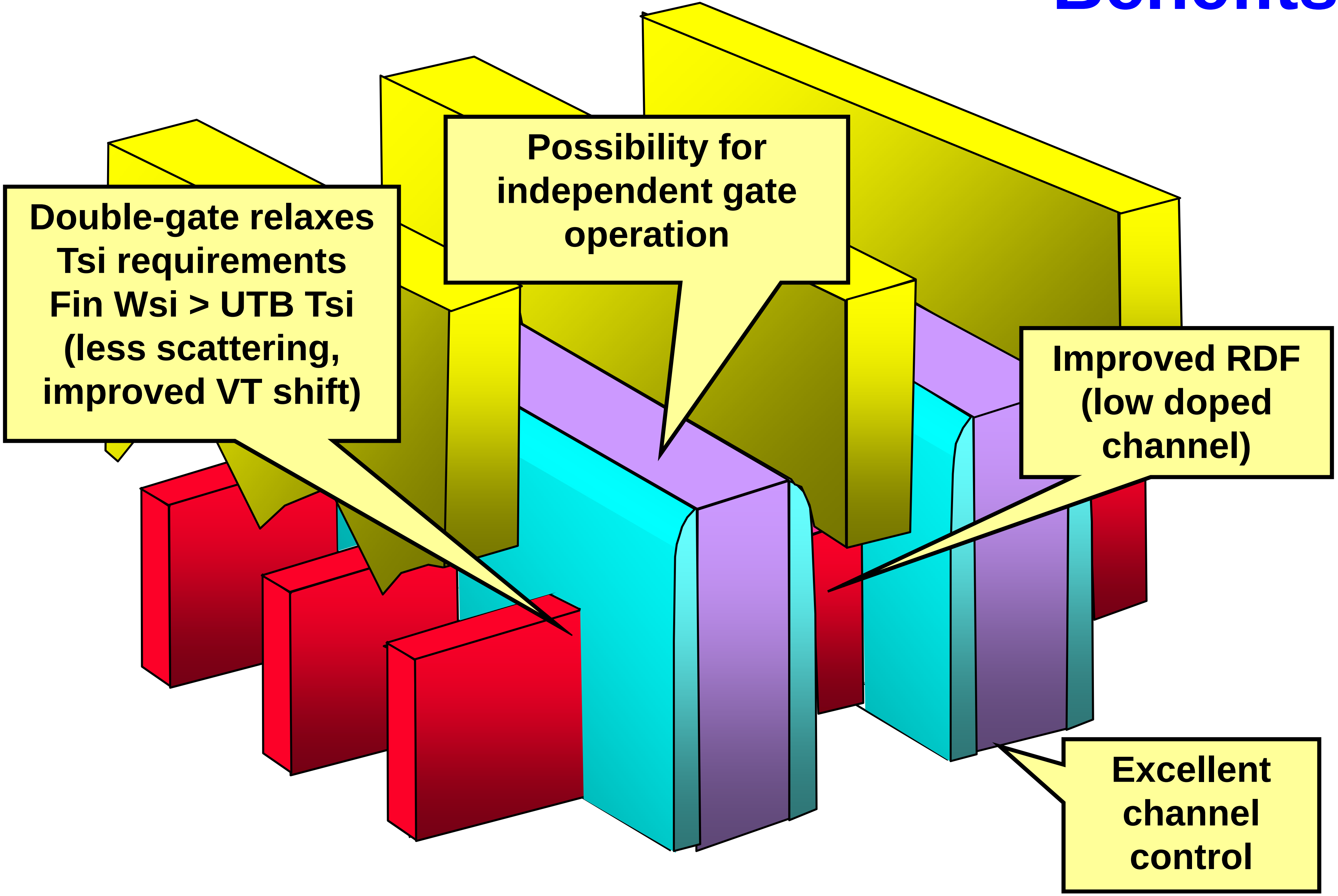
Improved RDF (low doped channel)

Compatible with RSD technology

Excellent channel control

MuGFET Benefits



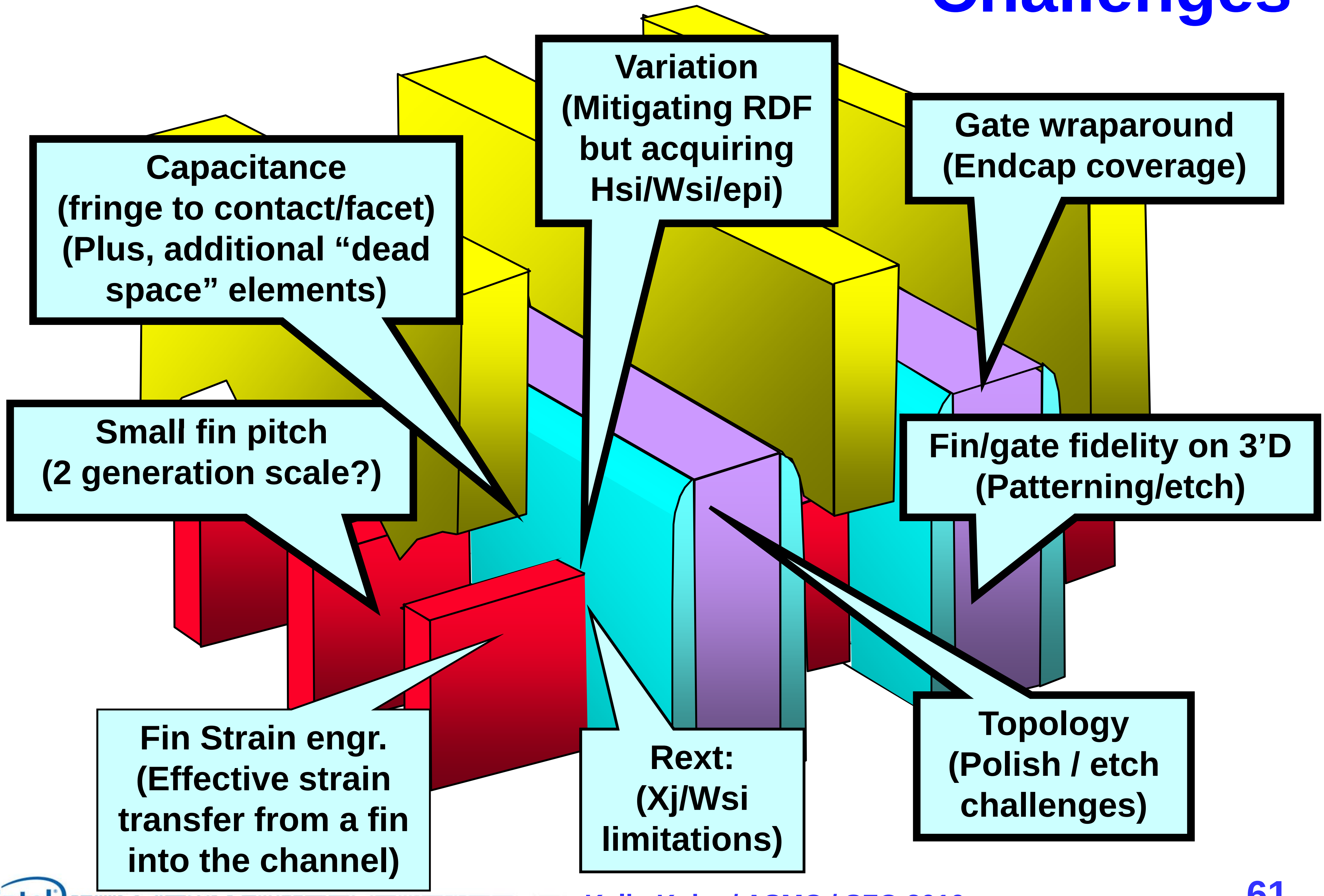
Double-gate relaxes Tsi requirements Fin Wsi > UTB Tsi (less scattering, improved VT shift)

Possibility for independent gate operation

Improved RDF (low doped channel)

Excellent channel control

MuGFET Challenges



Variation (Mitigating RDF but acquiring Hsi/Wsi/epi)

Gate wraparound (Endcap coverage)

Capacitance (fringe to contact/facet) (Plus, additional “dead space” elements)

Small fin pitch (2 generation scale?)

Fin/gate fidelity on 3’D (Patterning/etch)

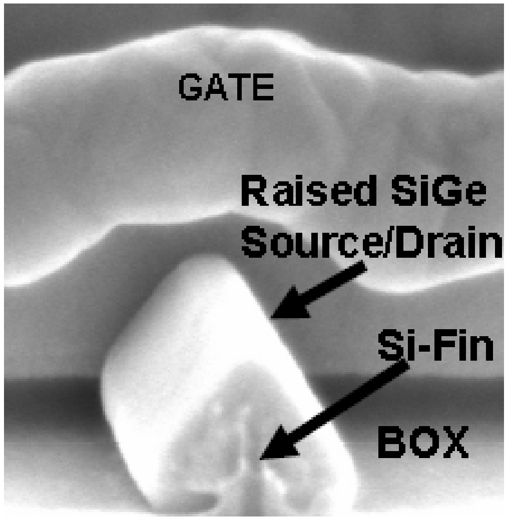
Fin Strain engr. (Effective strain transfer from a fin into the channel)

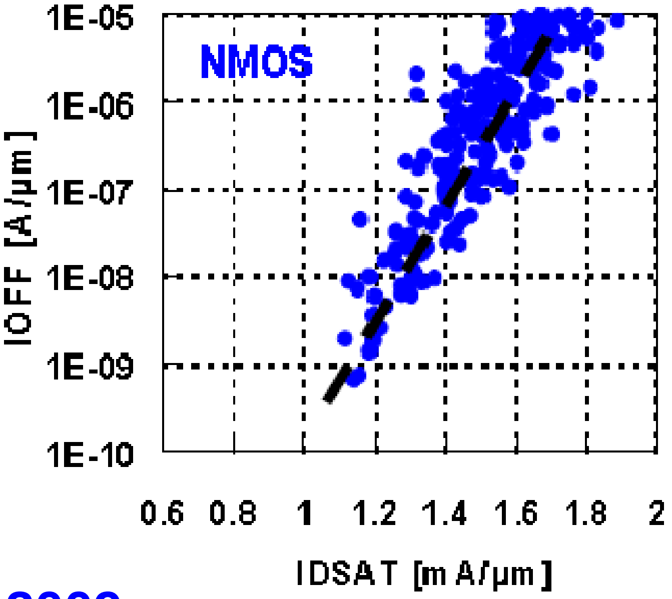
Rext: (Xj/Wsi limitations)

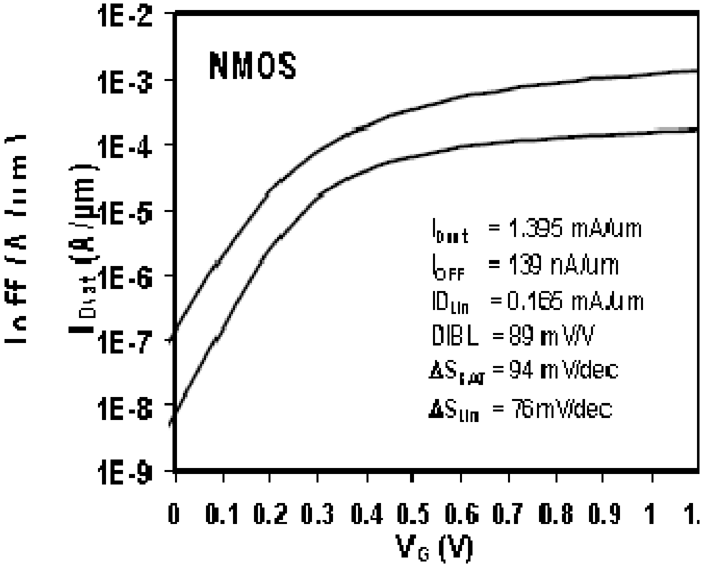
Topology (Polish / etch challenges)

MuGFET

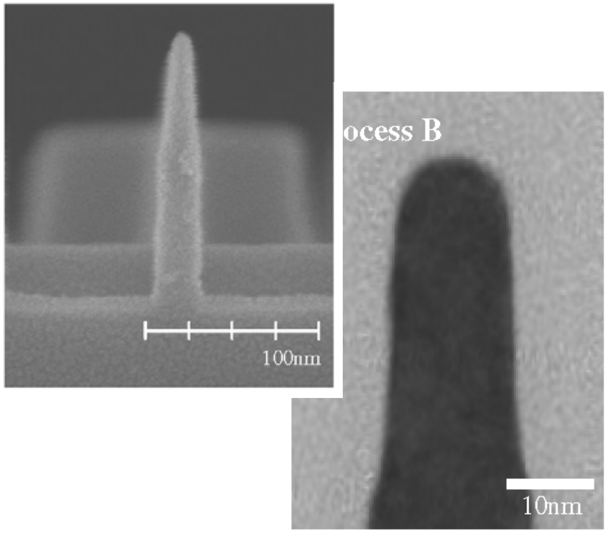
Kavalieros – Intel – IEDM 2006

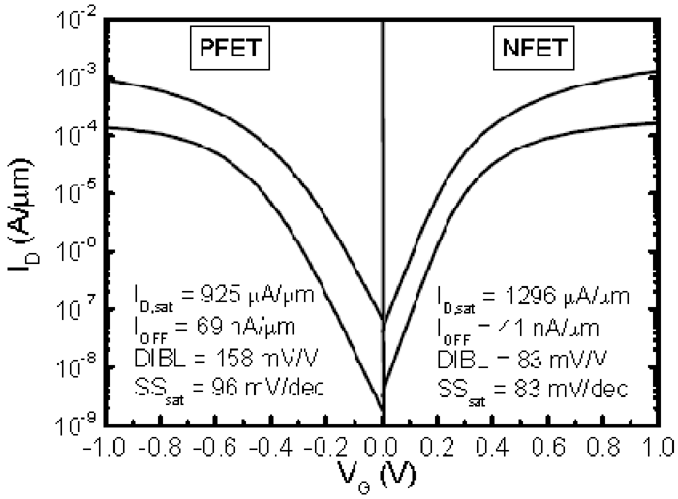


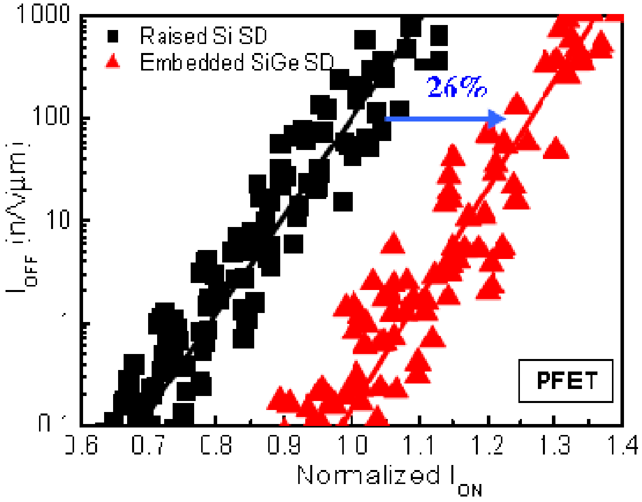




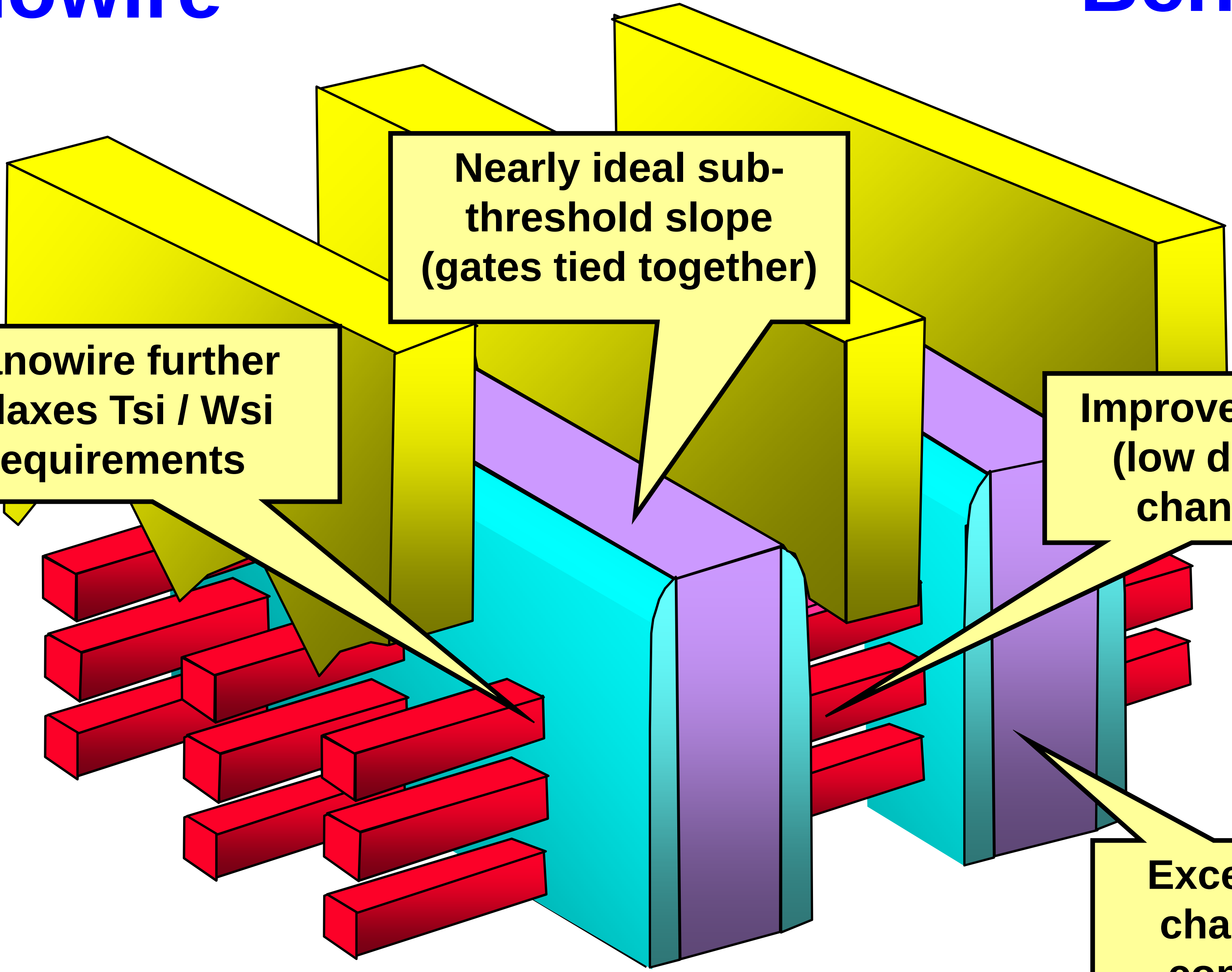
Chang – TSMC – IEDM 2009







Nanowire Benefits



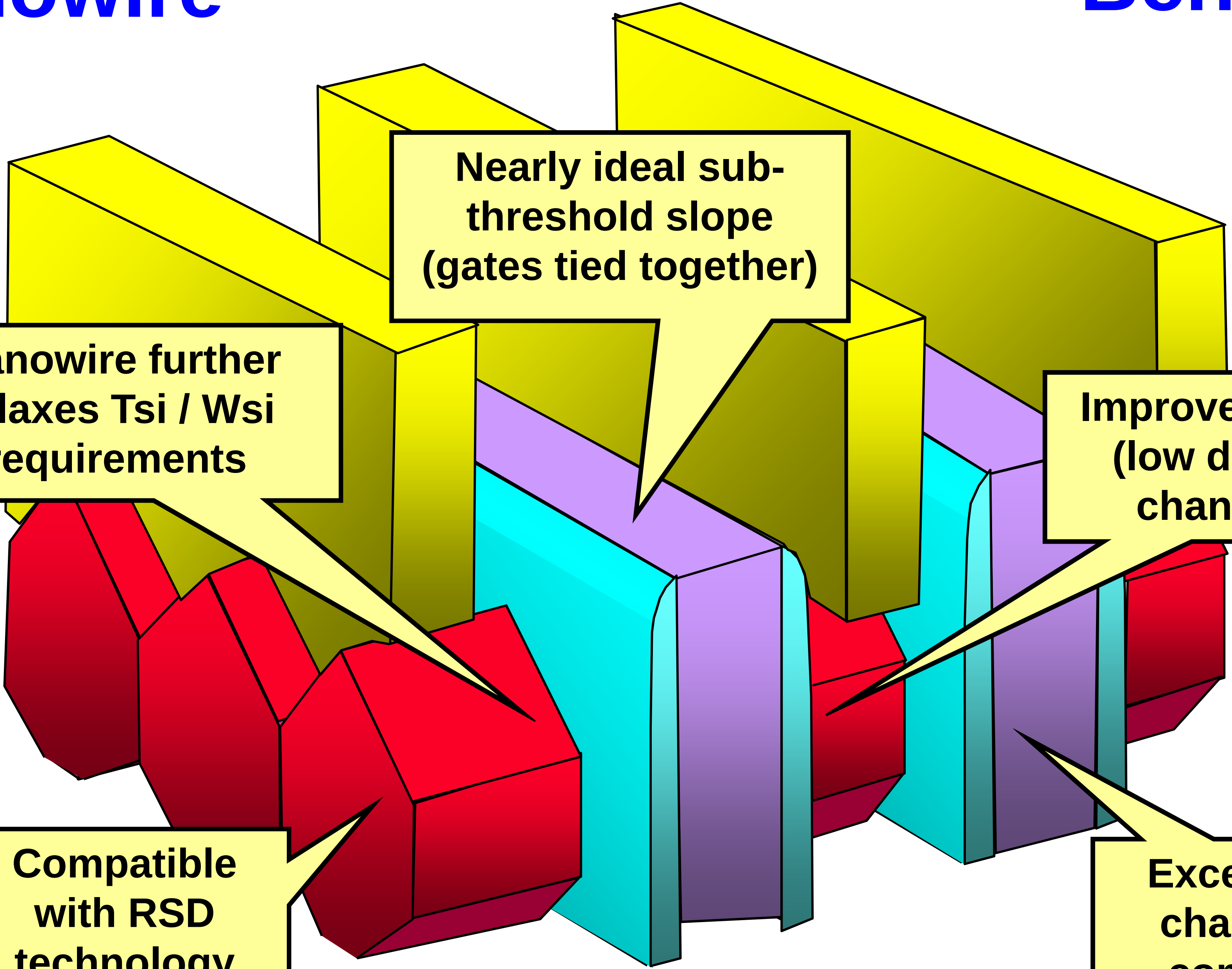
Nanowire further relaxes Tsi / Wsi requirements

Nearly ideal sub-threshold slope (gates tied together)

Improved RDF (low doped channel)

Excellent channel control

Nanowire Benefits



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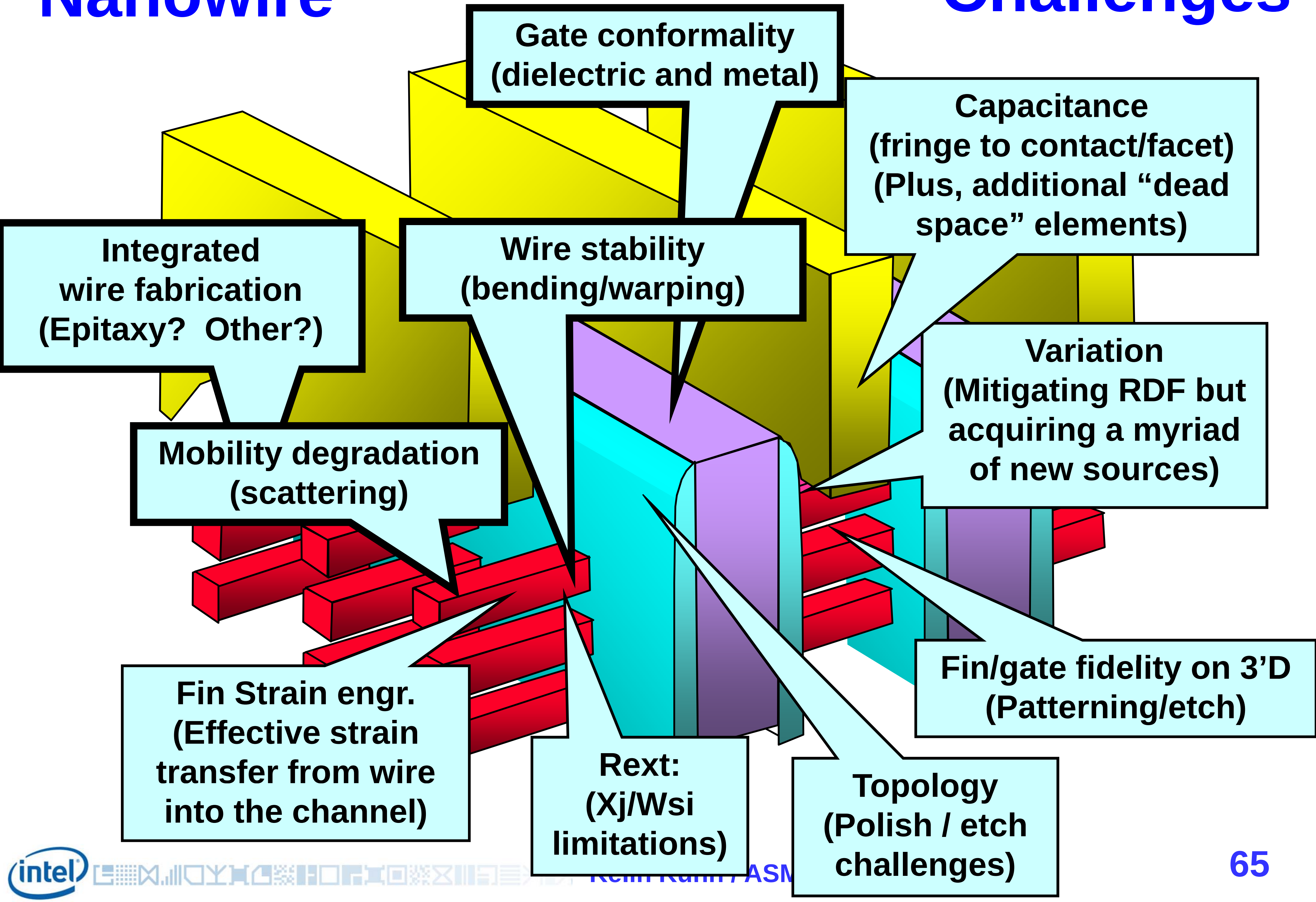
Nanowire Challenges



Gate conformality (dielectric and metal)

Capacitance (fringe to contact/facet) (Plus, additional “dead space” elements)

Integrated wire fabrication (Epitaxy? Other?)

Wire stability (bending/warping)

Variation (Mitigating RDF but acquiring a myriad of new sources)

Mobility degradation (scattering)

Fin/gate fidelity on 3’D (Patterning/etch)

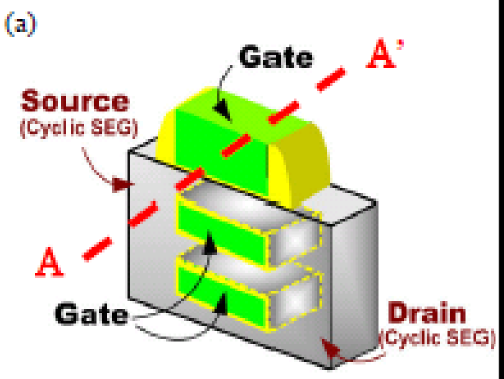
Fin Strain engr. (Effective strain transfer from wire into the channel)

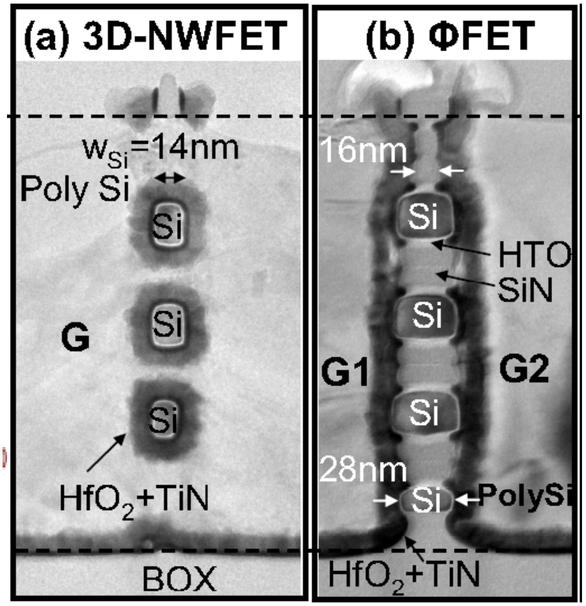
Rext: (Xj/Wsi limitations)

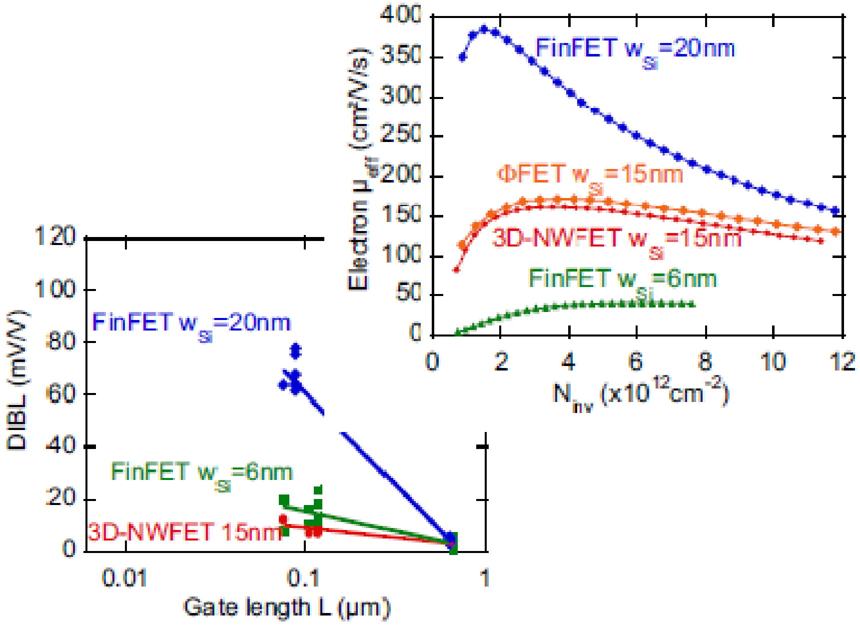
Topology (Polish / etch challenges)

Nanowire FETs

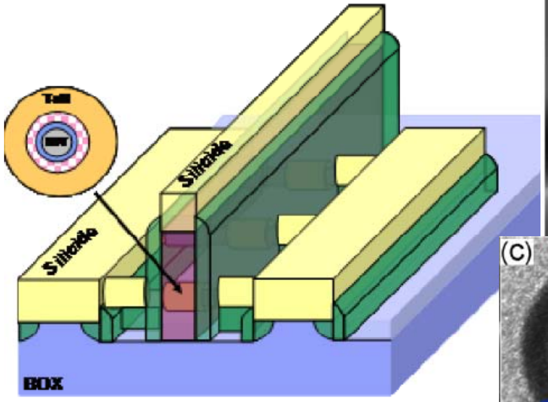
Dupre – CEA-LETI – IEDM 2008

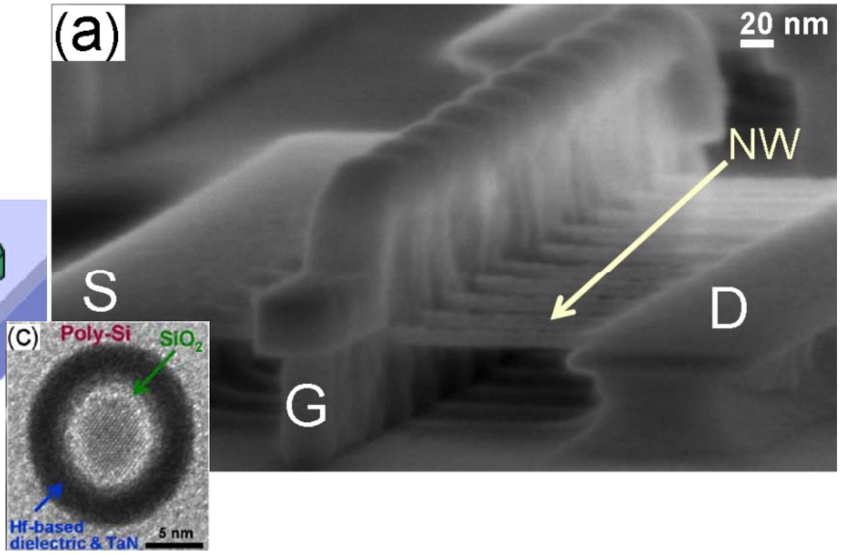


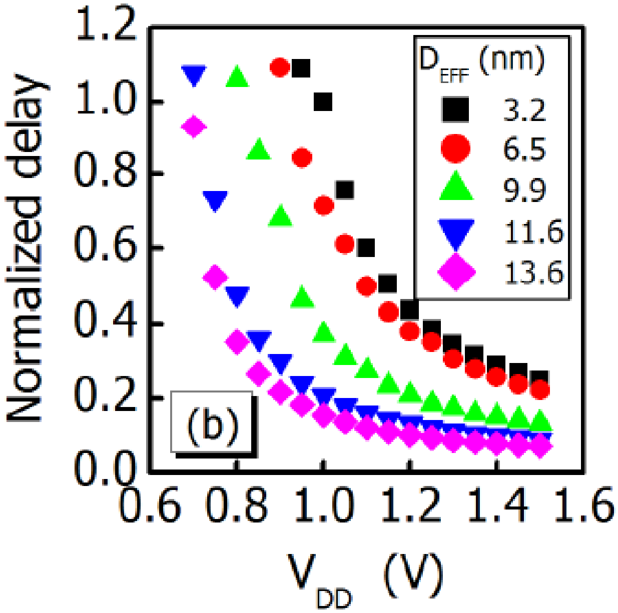




Bangsaruntip – IBM – IEDM 2009





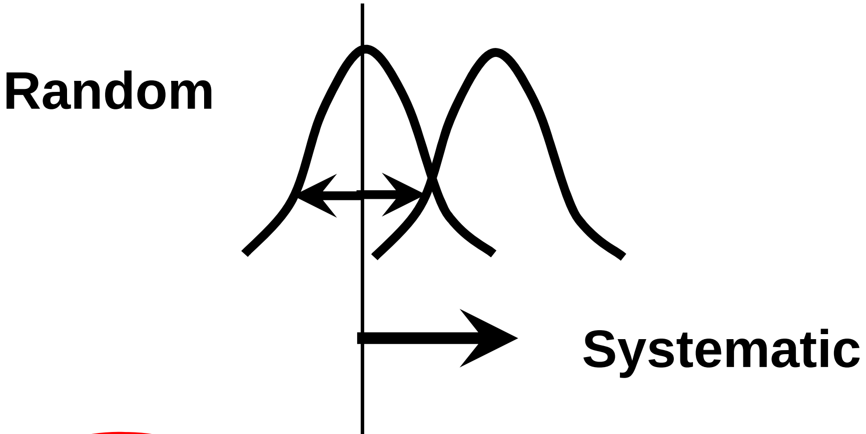


AGENDA

I. Overview – variation sources
II. Next generation variation – lithography
III. Next generation variation – polish
IV. Next generation devices
V. Measurements, results and interpretation
VI. Closing thoughts

Systematic and Random

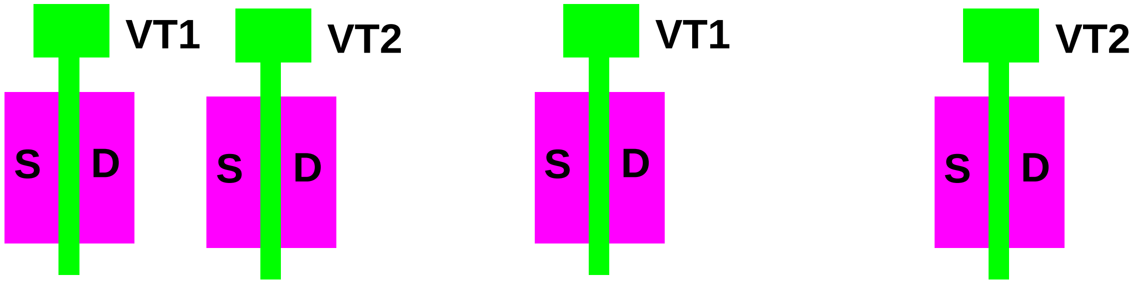
- **Statistician's viewpoint:**



- **Process engineer's viewpoint:**

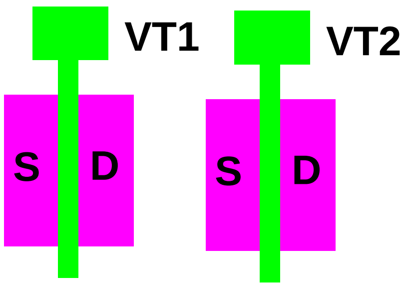
Random **Systematic**

- **Device engineer's viewpoint:**



Random **Systematic**

Measurement of Random and Systematic VT Variation at the Device Level



Traditional method:

1. Measure two identical adjacent devices and extract the difference σ(VTA-VTB)
2. Measure the entire population of all devices and extract σ(VTpop)

Random Variation for a matched pair

$$Random_{mp} = StdDev(VT_A - VT_B) = \sigma(DVT)$$

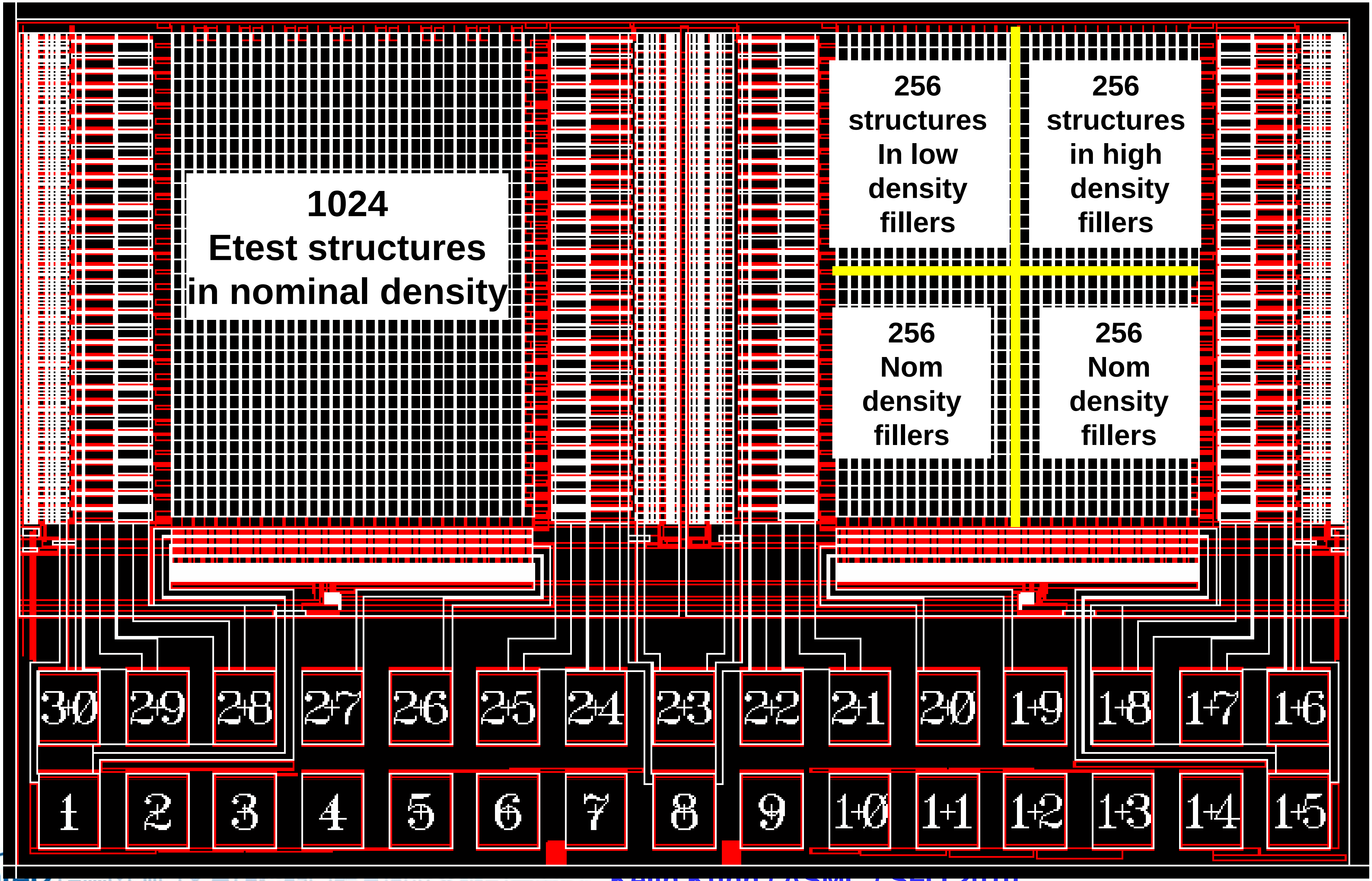
Random Variation for a single device

$$Random_{one-device} = \frac{StdDev(VT_A - VT_B)}{\sqrt{2}} = \frac{\sigma(DVT)}{\sqrt{2}}$$

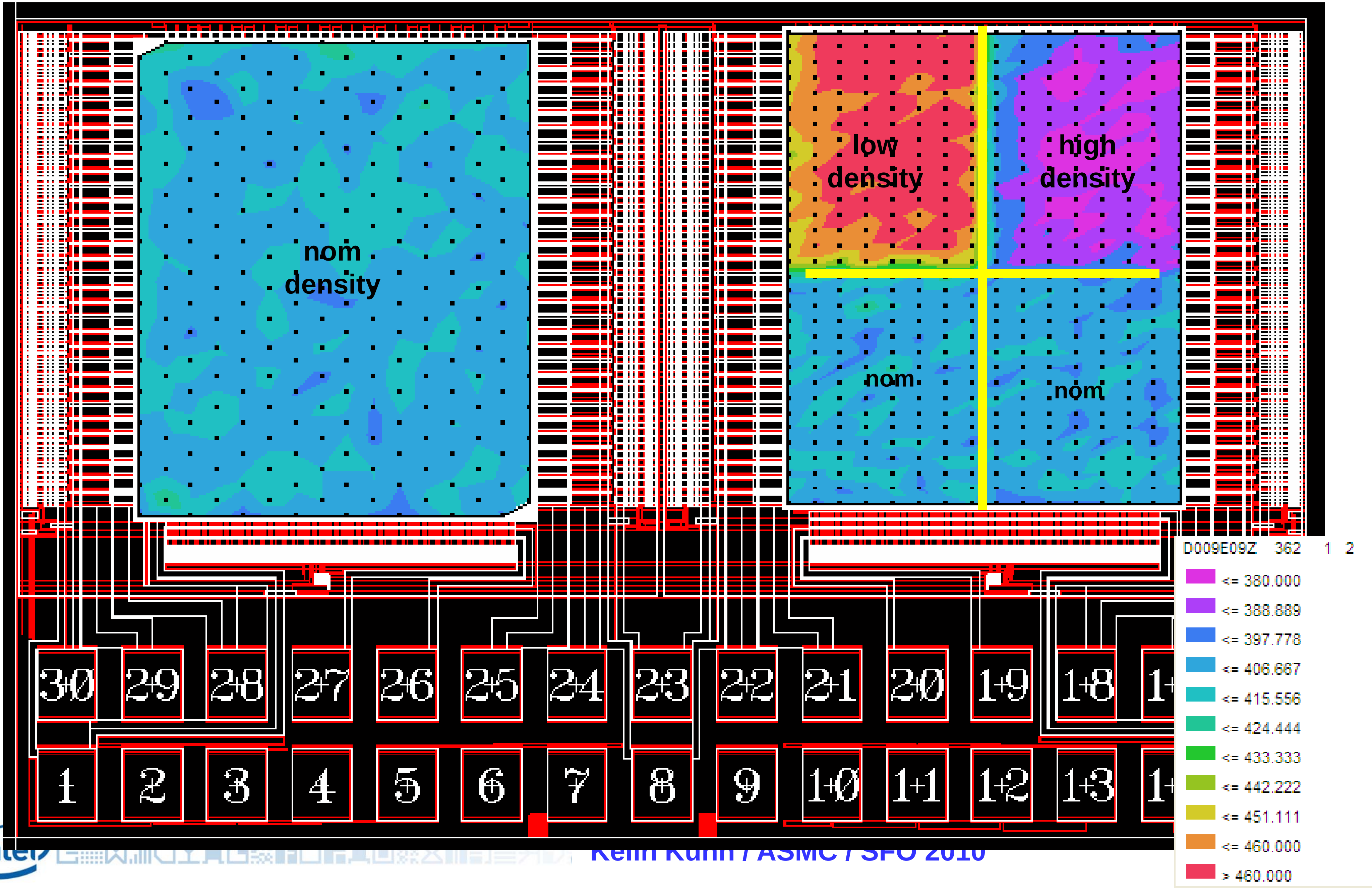
Systematic Variation for a single device

$$Systematic = \sqrt{(\sigma VT_{pop})^2 - \left(\frac{\sigma(DVT)}{\sqrt{2}}\right)^2}$$

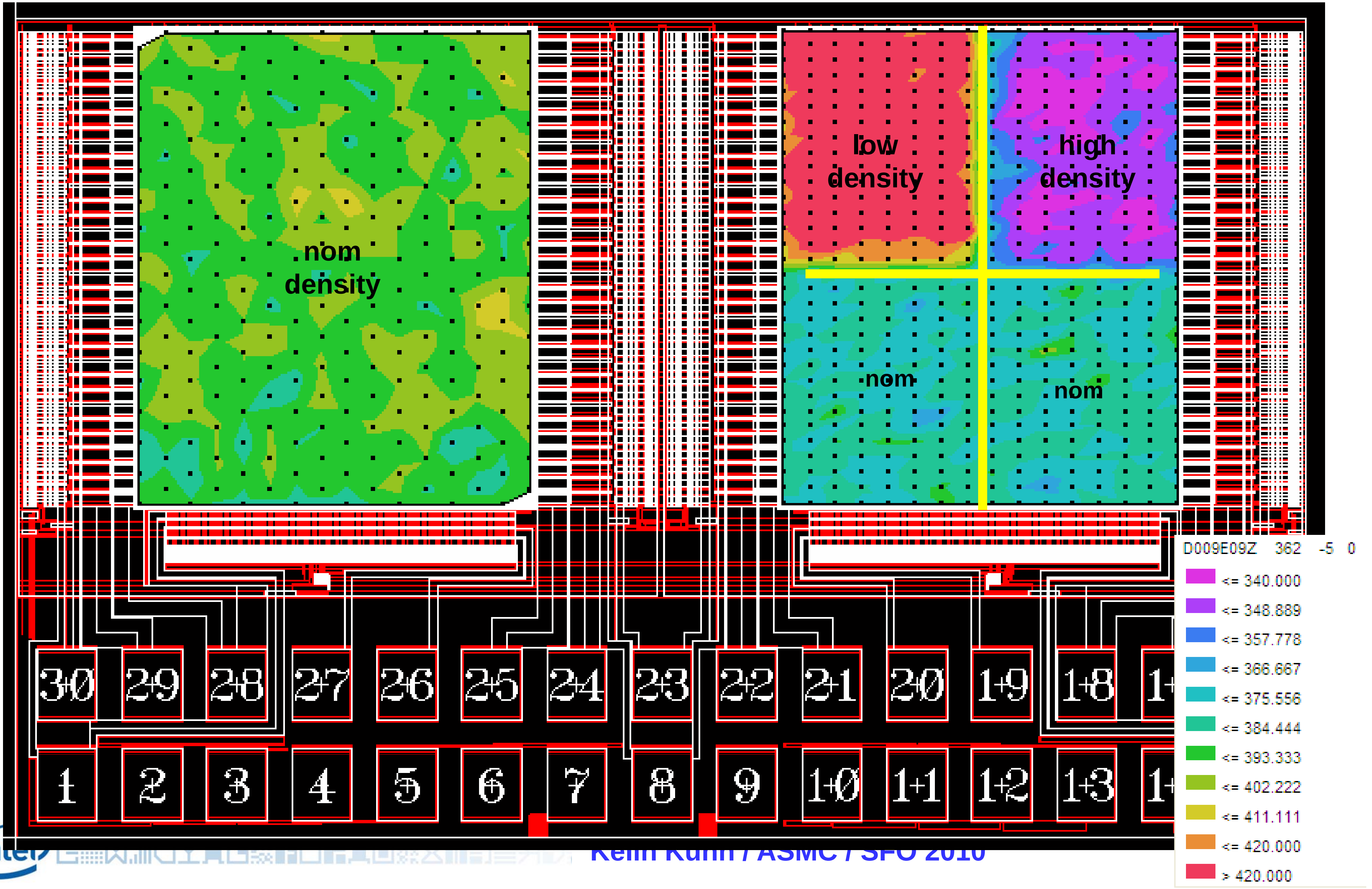
Using Arrays for Variation Measurement (this example is metal resistors)



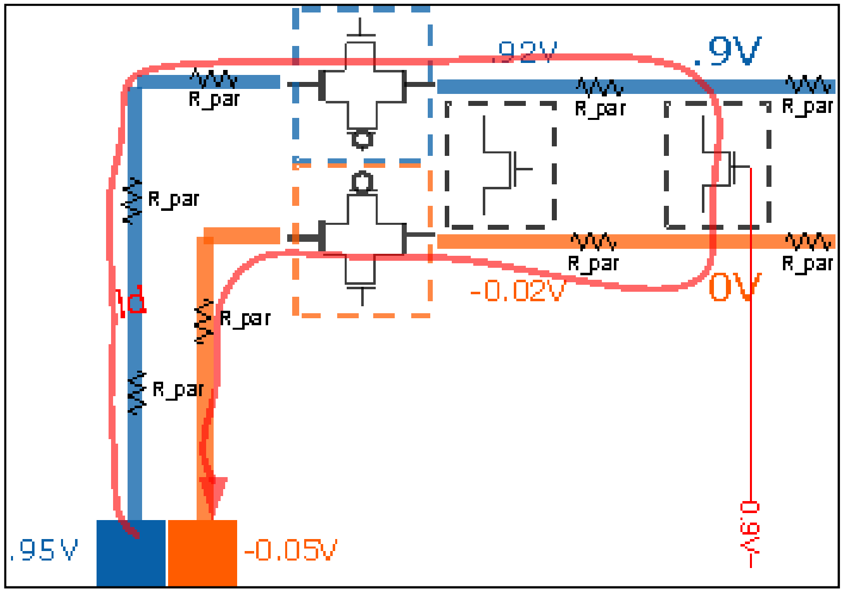
Using Arrays for Variation Measurement (this example is metal resistors)

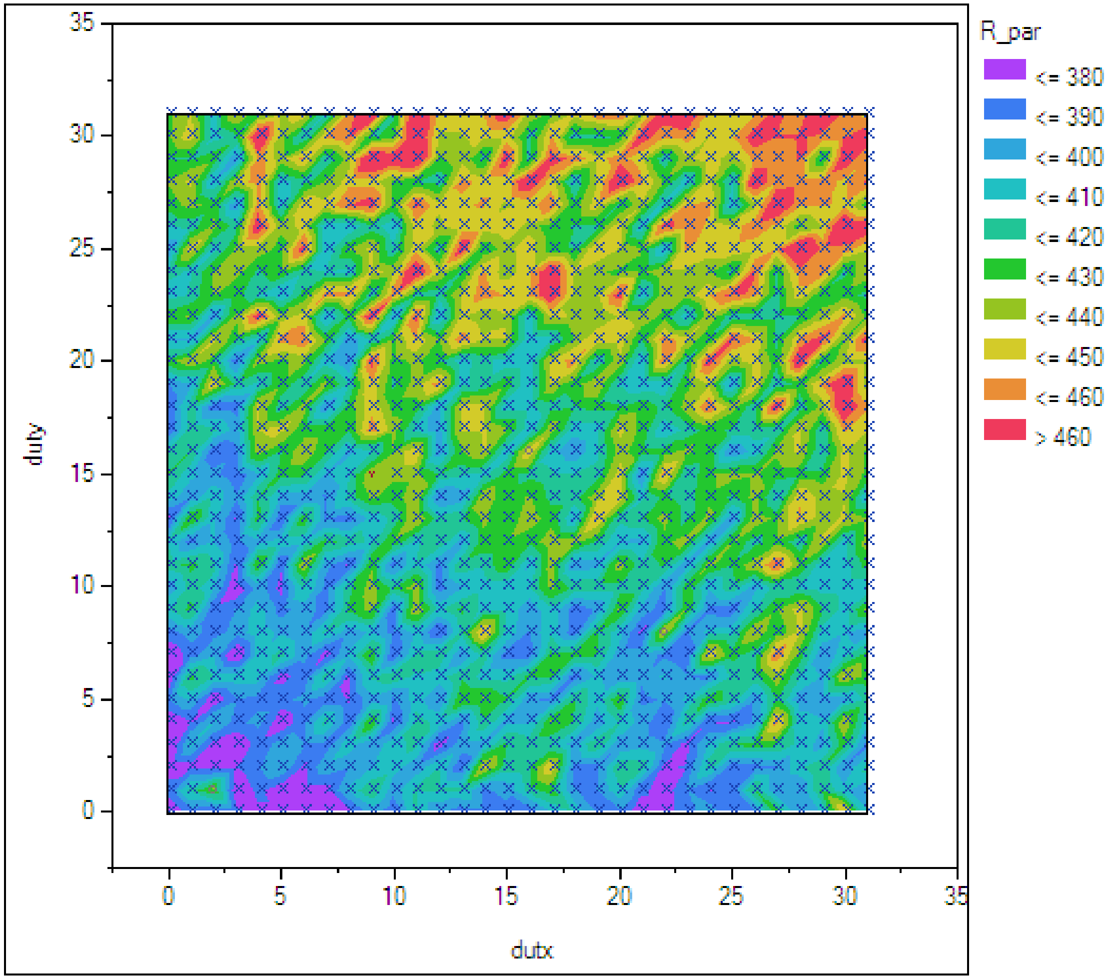


Using Arrays for Variation Measurement (this example is metal resistors)



Important of Comprehending de-Biasing in Arrays





Random and Systematic Variation for Matched Ring Oscillators

Random:

- Calculate Delta

$$Delta = \frac{FreqA - FreqB}{FreqA + FreqB} * \frac{200}{\sqrt{2}}$$

- **Random Variation**

$$\boxed{Rand = StdDev(Delta)}$$

per data unit

Systematic:

- Total Sigma

$$\sigma = StdDev(FreqA)$$

per data unit

- Grand Mean

$$\mu = \frac{Mean(FreqA) + Mean(FreqB)}{2}$$

- **Systematic Variation**

$$\boxed{Syst = \sqrt{\left(\frac{\sigma}{\mu} * 100\right)^2 - Rand^2}}$$

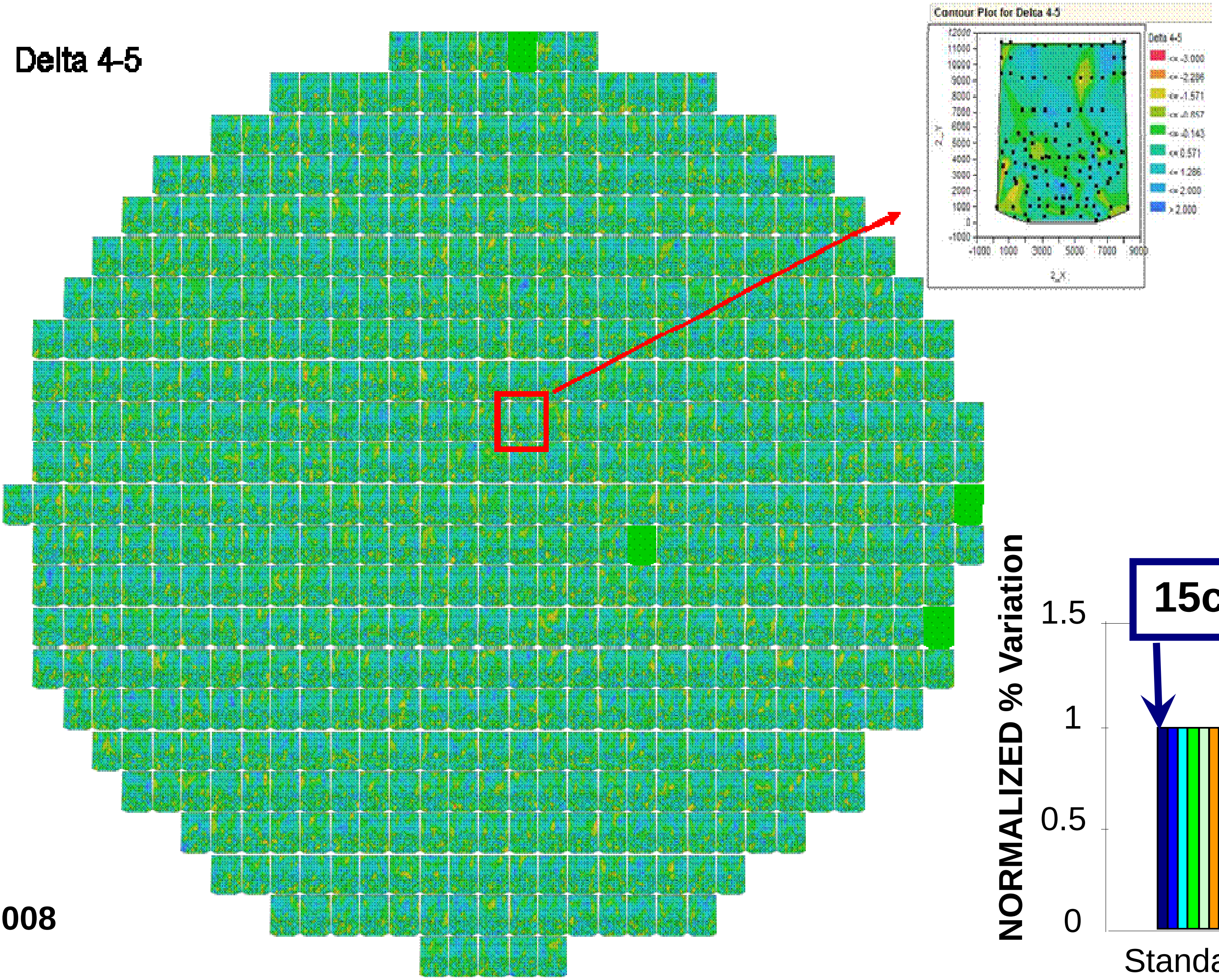
per data unit

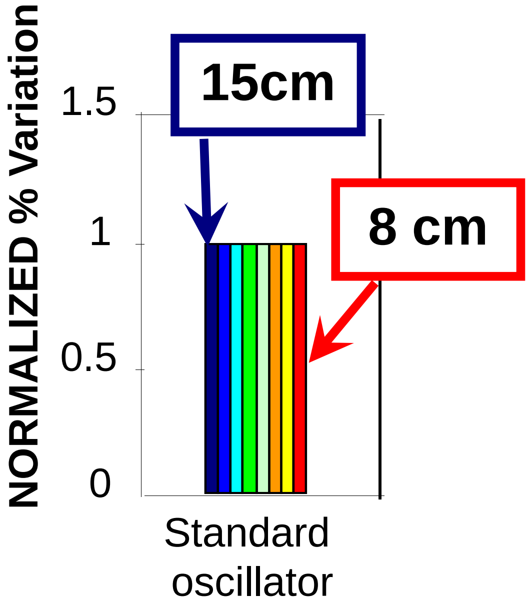
Total Variation:

$$\boxed{Total = \frac{StdDev(FreqA)}{Mean(FreqA)} * 100}$$

per data unit

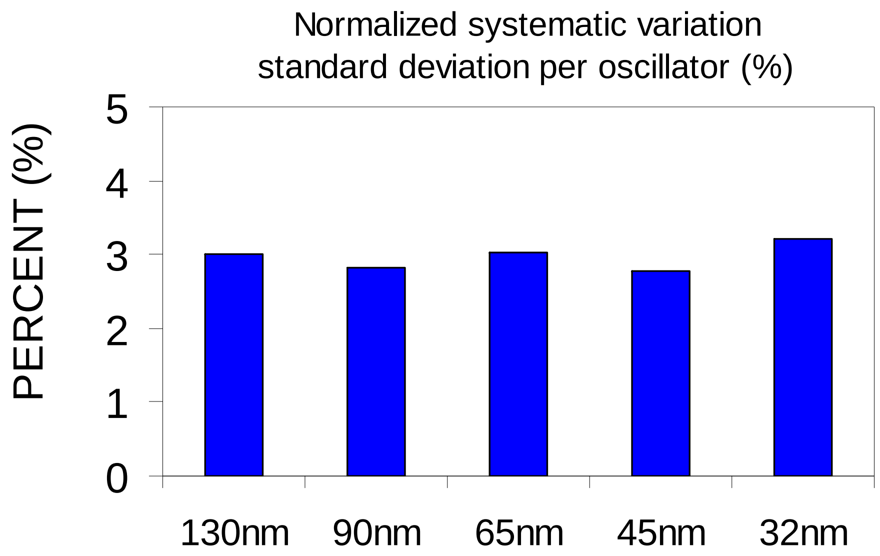
45nm Product wafer: Random variation



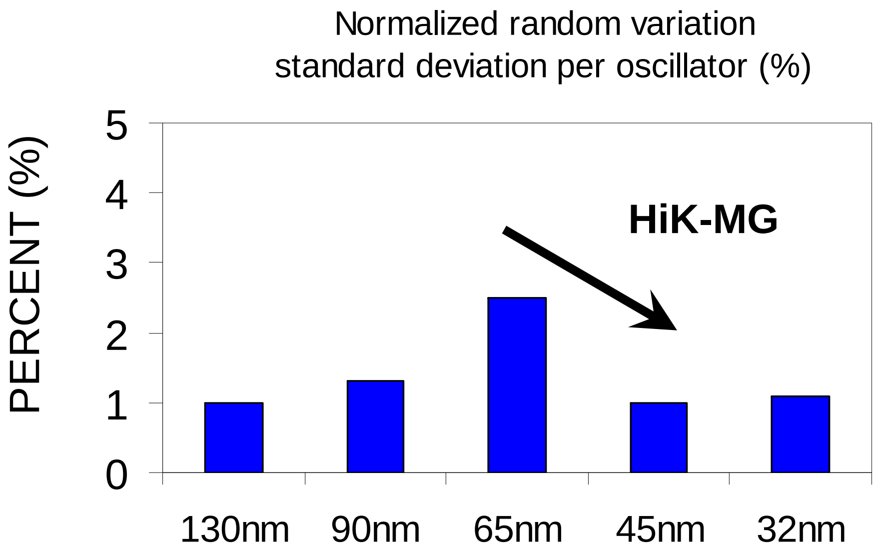


K. Kuhn, ITJ 2008

Random and Systematic Variation Trends



Systematic WIW variation is comparable from one generation to the next



Random WIW variation in 32nm is comparable to 45nm and significantly improved over 65nm and 90nm due to HiK-MG

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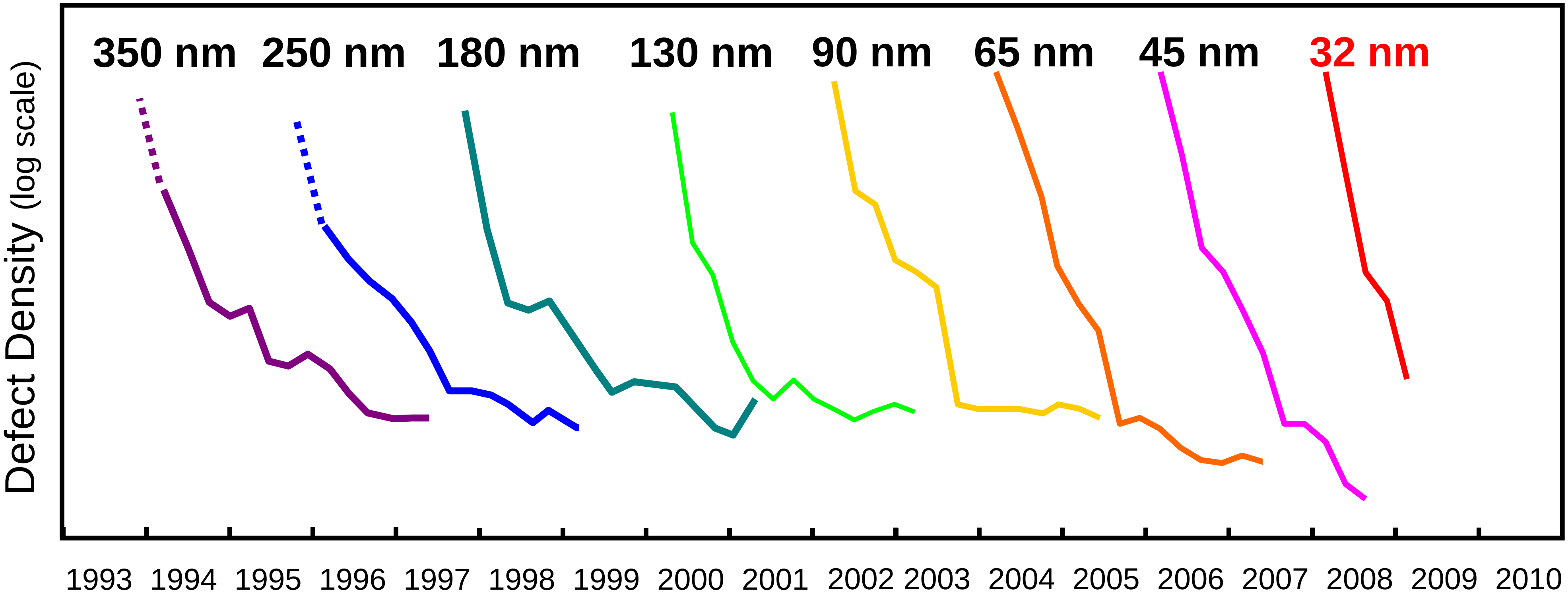
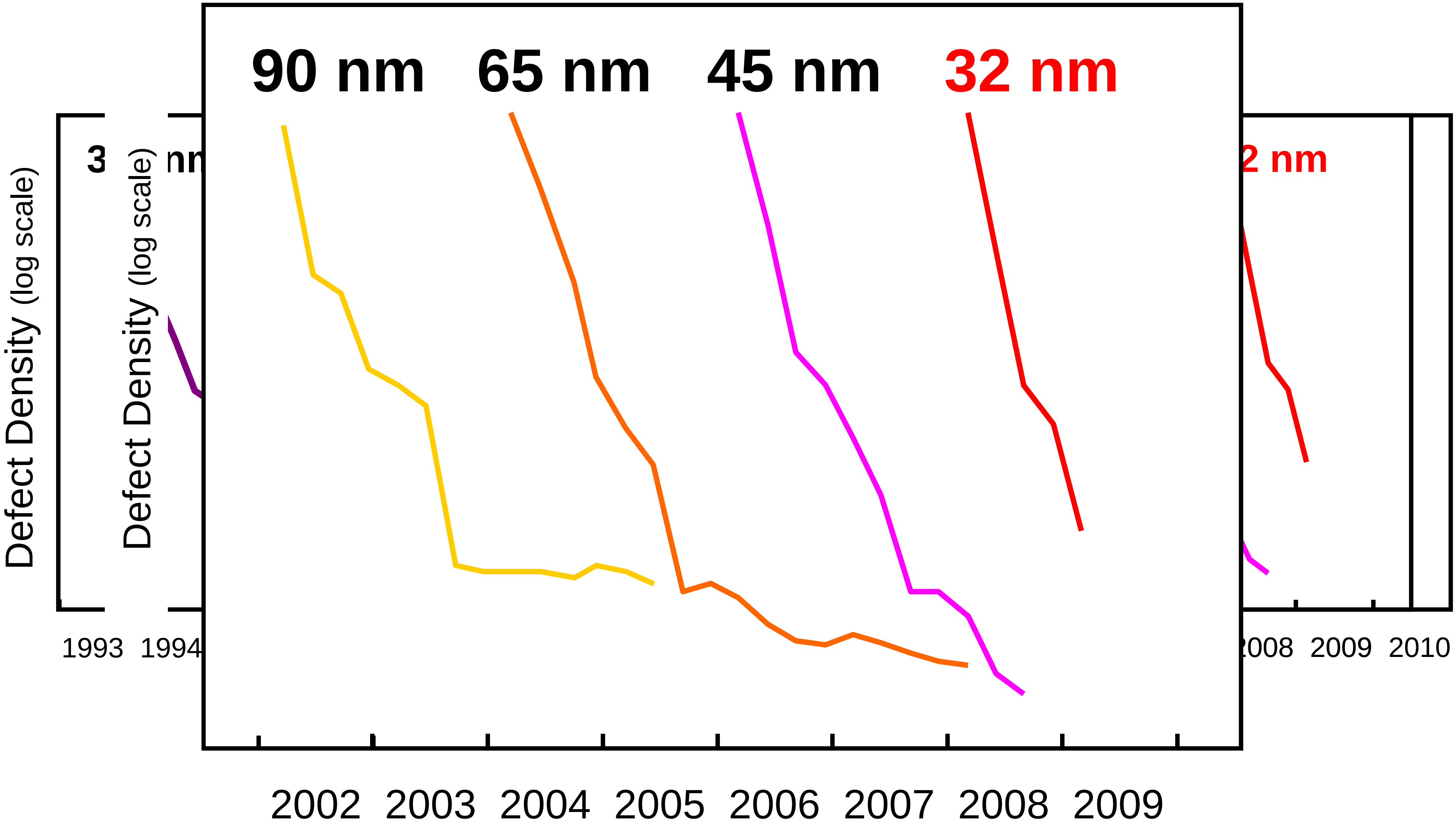
Yield: A pragmatic measure of variation

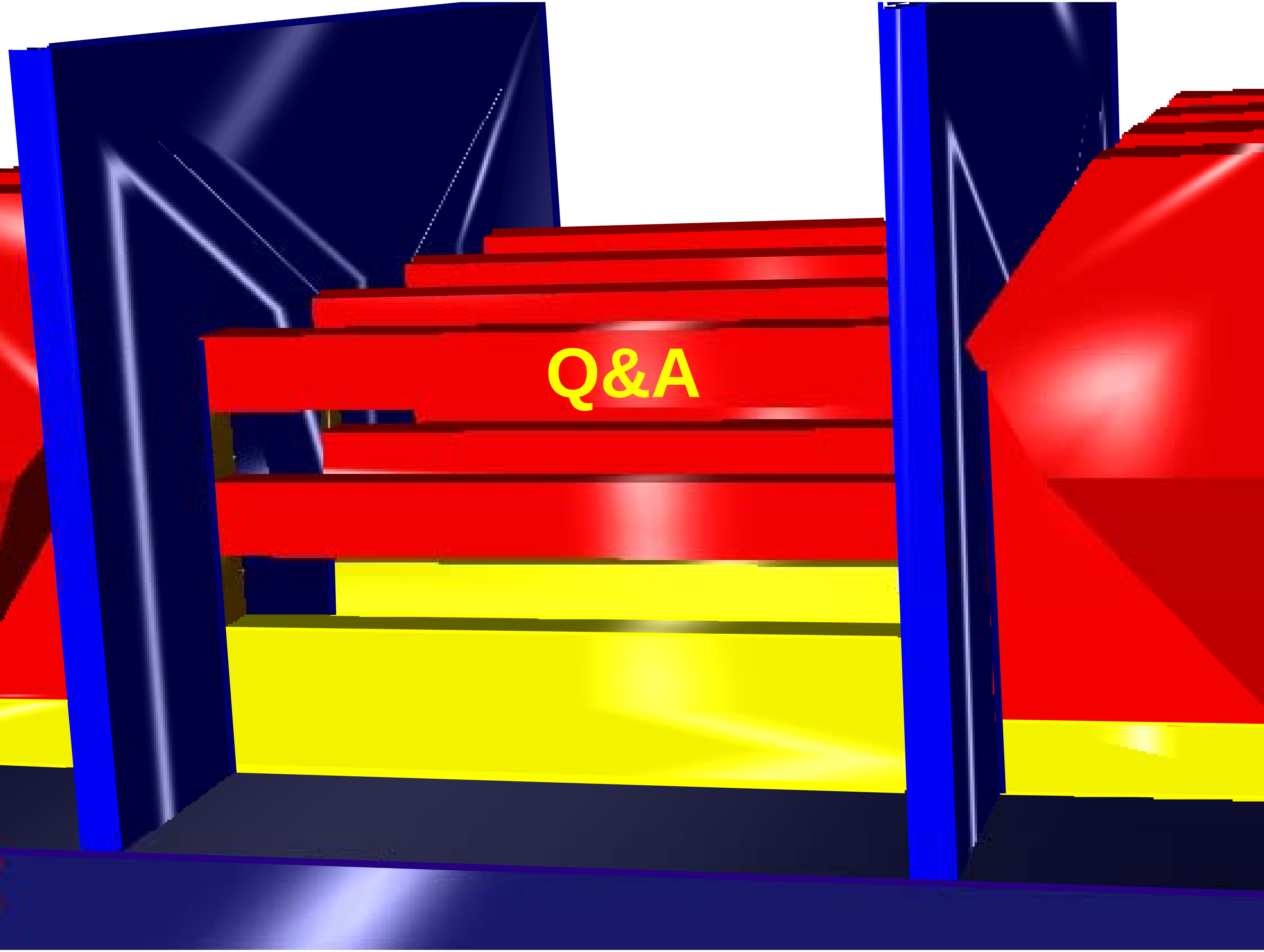


Yield: A pragmatic measure of variation



Closing Thoughts

Process variation is not an insurmountable barrier to Moore's Law, but is simply another challenge to be overcome.



Q&A