Past, Present and Future: SiGe and CMOS Transistor Scaling

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Intel Corporation

AGENDA

- Past (Scaling)
- Present (Planar SiGe S/D)
- Future
  - Planar Ge channel
  - Non-planar architectures
  - Tunnel FETs
- Summary

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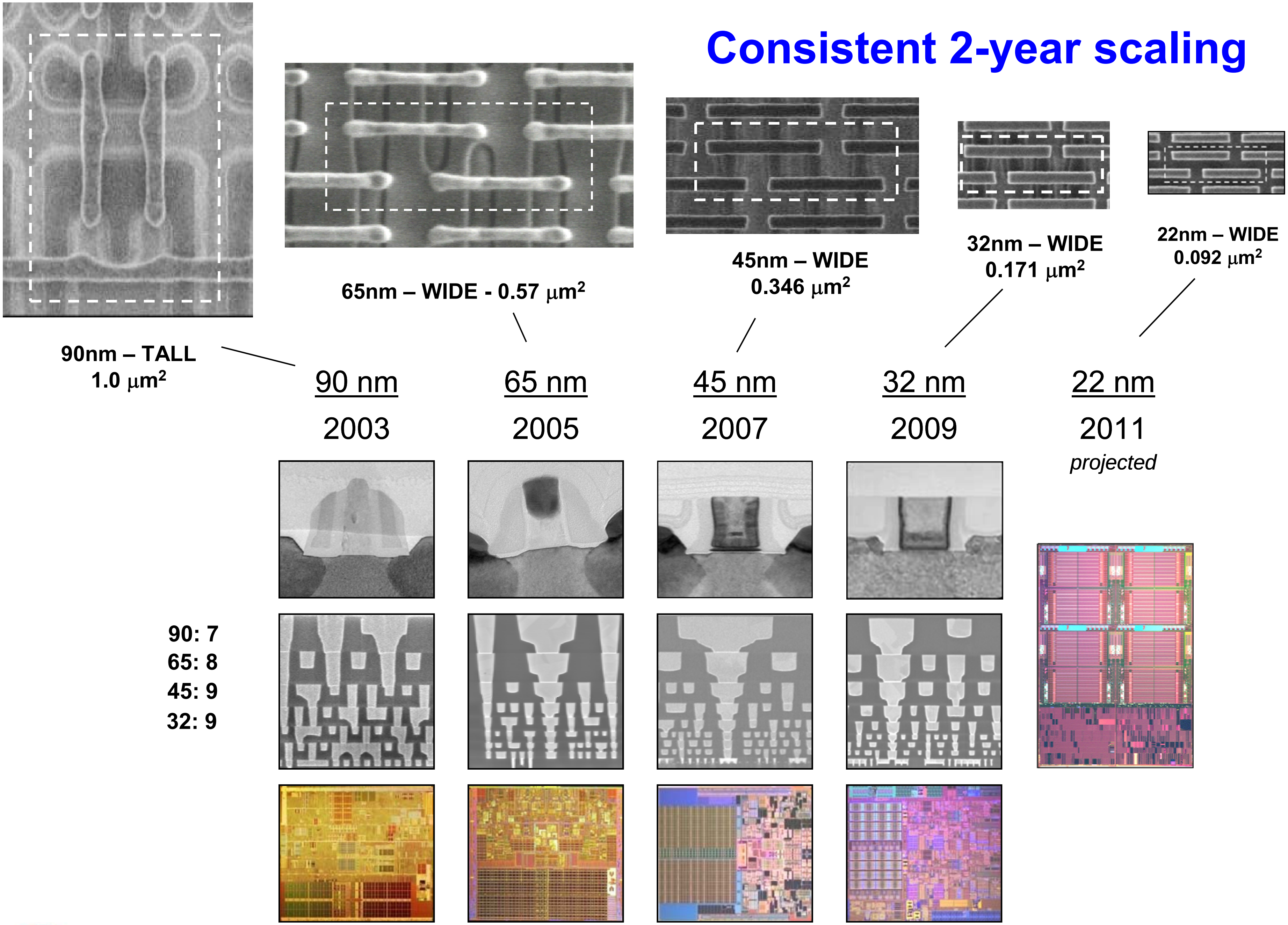
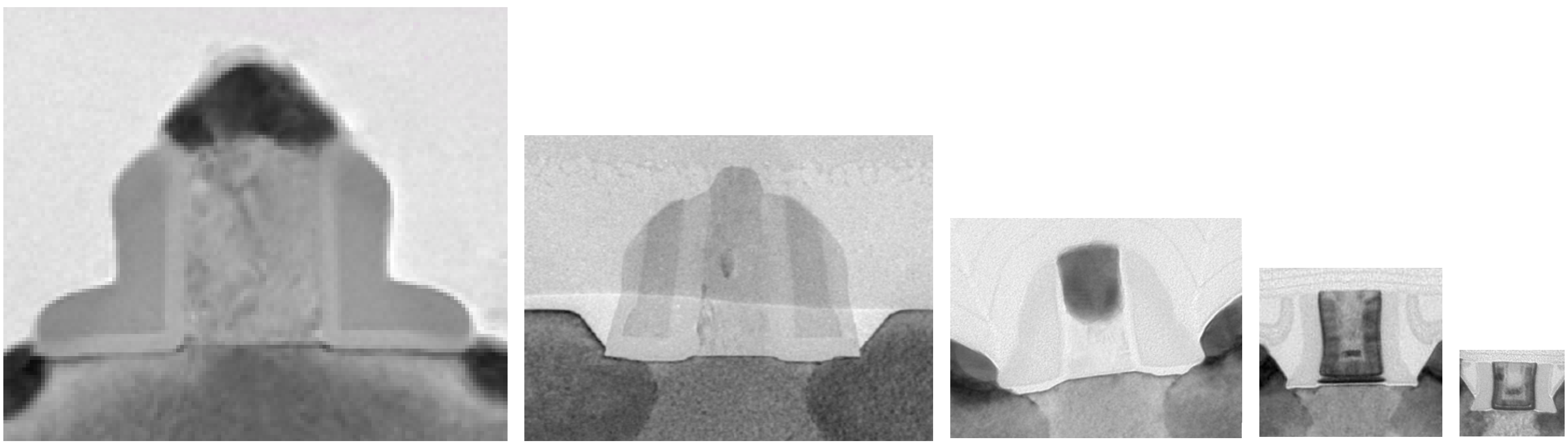
Consistent 2-year scaling



Changes in Scaling

THEN	NOW
• Scaling drove down cost	• Scaling drives down cost
• Scaling drove performance	• Materials drive performance
• Performance constrained	• Power constrained
• Active power dominates	• Standby power dominates
• Independent design-process	• Collaborative design-process



130nm 90nm 65nm 45nm 32nm

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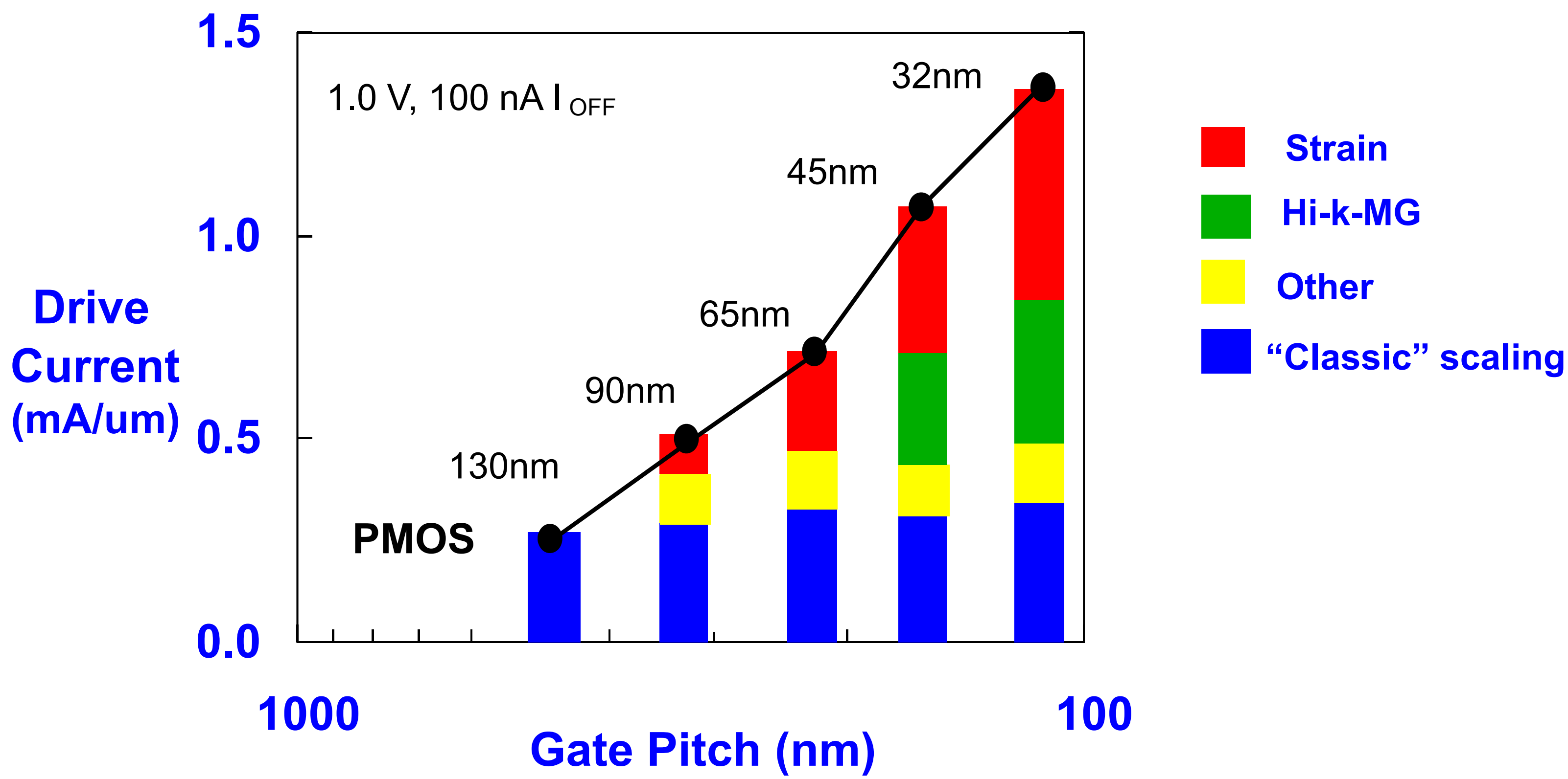
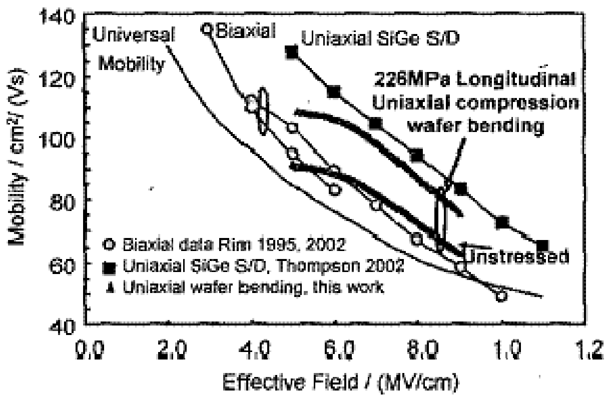
Transistor Performance Trend

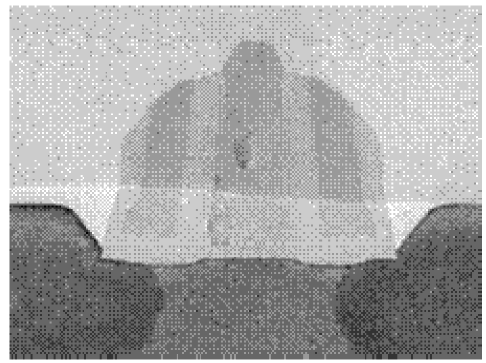


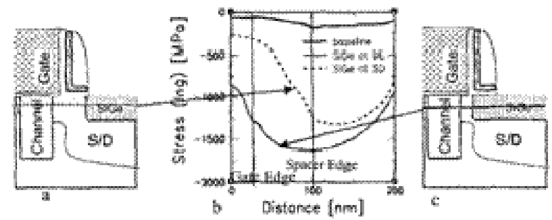
Strain is a critical ingredient in modern transistor scaling

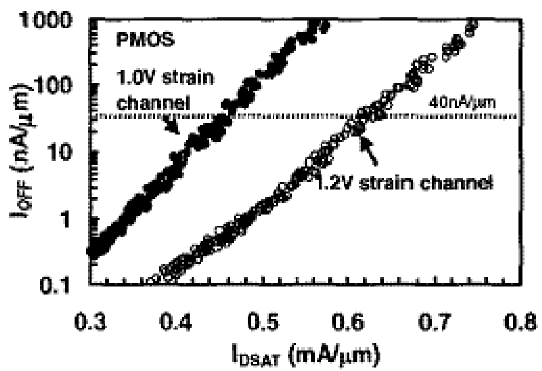
Strain was first introduced at 90nm, and its contribution has increased in each subsequent generation

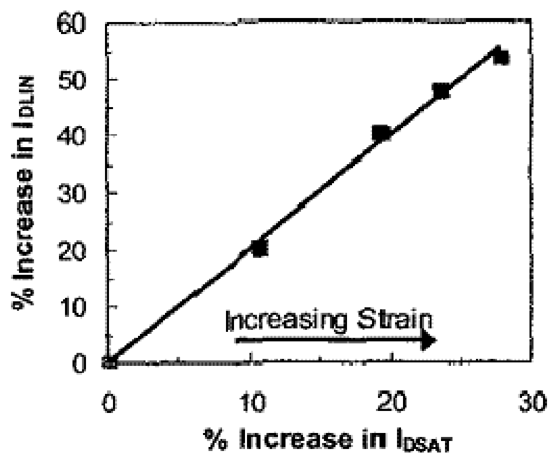
Uniaxial Strain Enhancement with Embedded SiGe (PMOS)

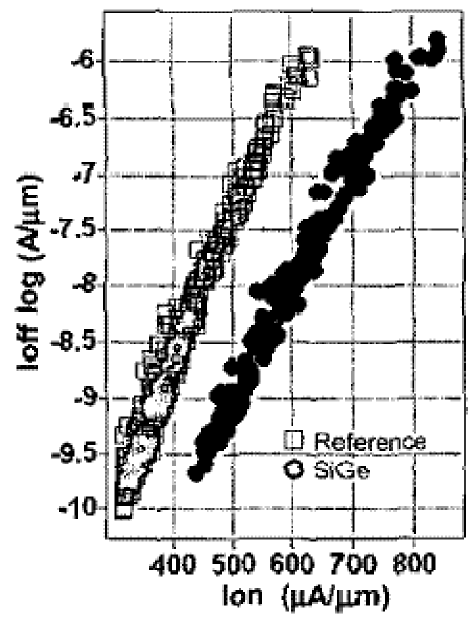












Thompson – Intel
IEDM 2002 / 2004 [28-30]

Ghani – Intel
IEDM 2003 [31]

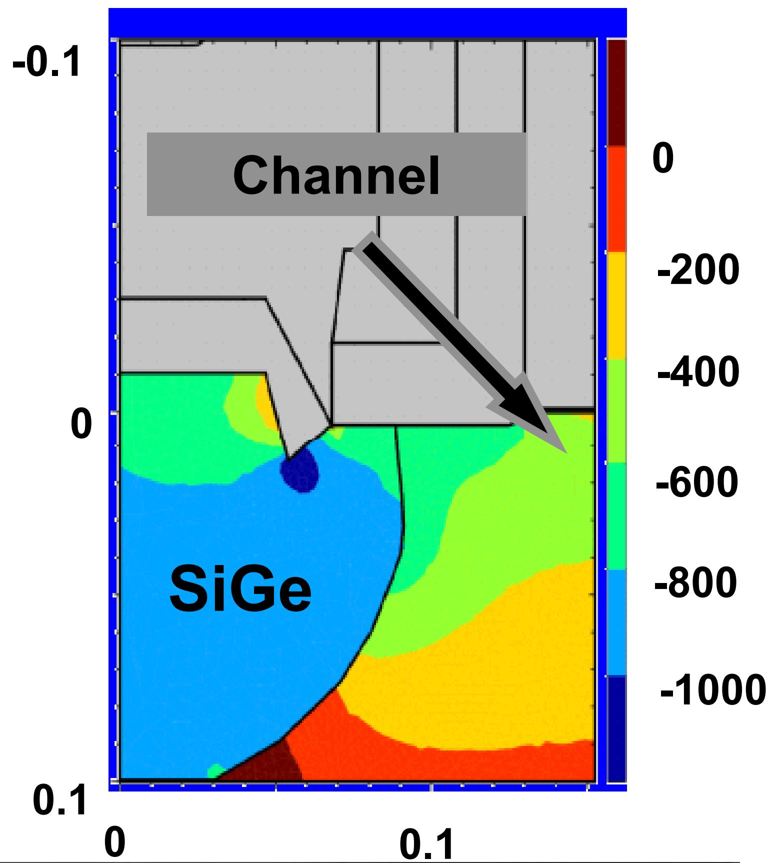
Chidambaram
TI / Applied Materials
VLSI - 2004 [32]

Transistor Results: Channel Strain

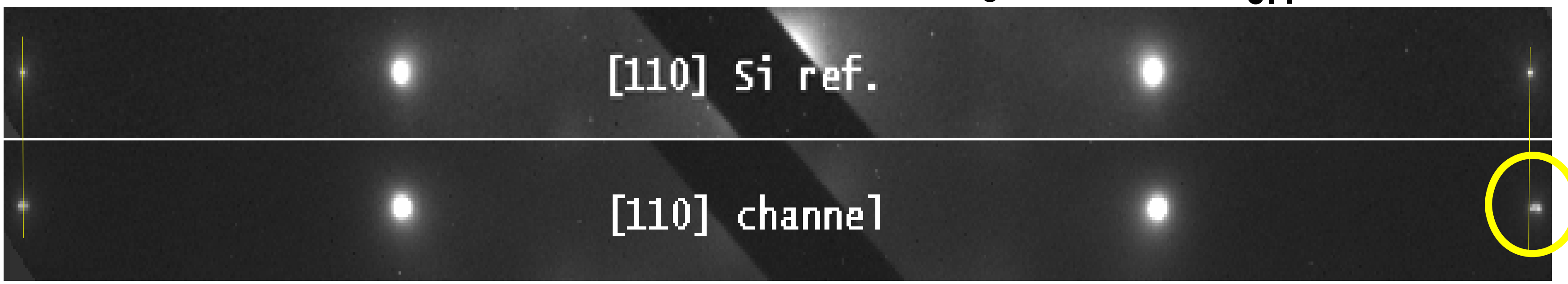
- Simulations show epitaxial S/D transistor has uniaxial compressive channel strain

  (Giles VLSI'04, [24])
- TEM electron diffraction measurements confirm 0.6% lattice displacement

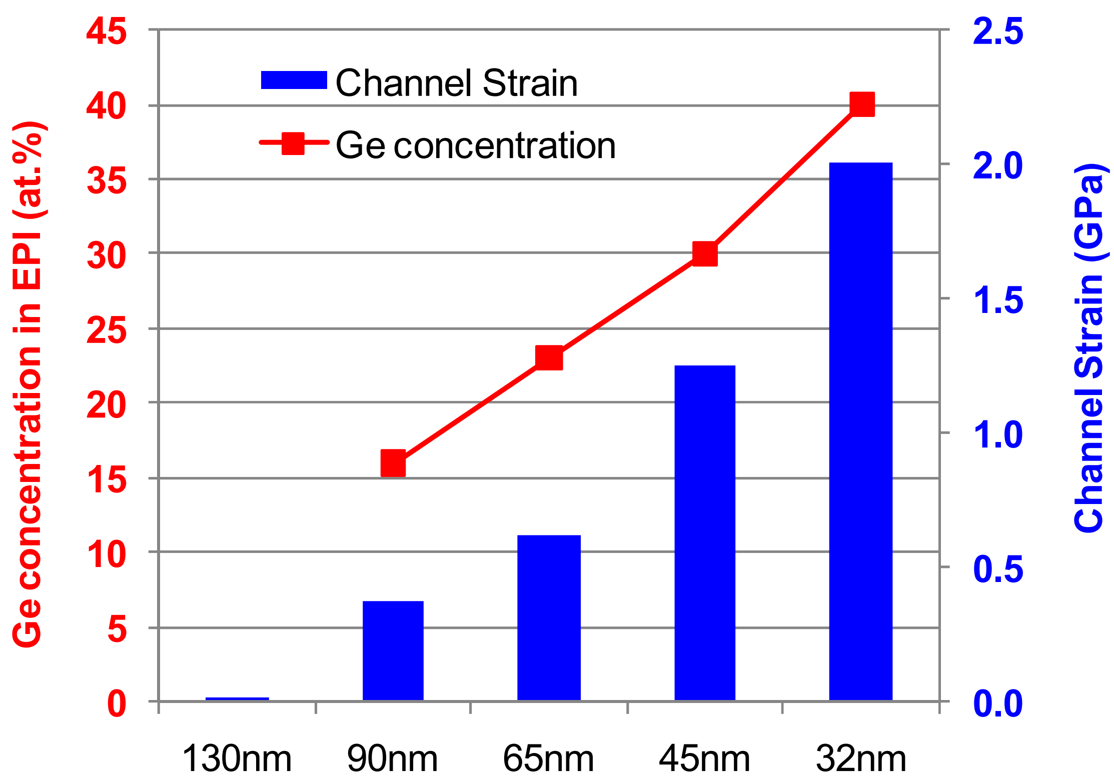
  (Mistry, VLSI'04, [26])



L_{GATE}=50nm



Technology Strain Trend



Strain is a critical ingredient in modern transistor scaling

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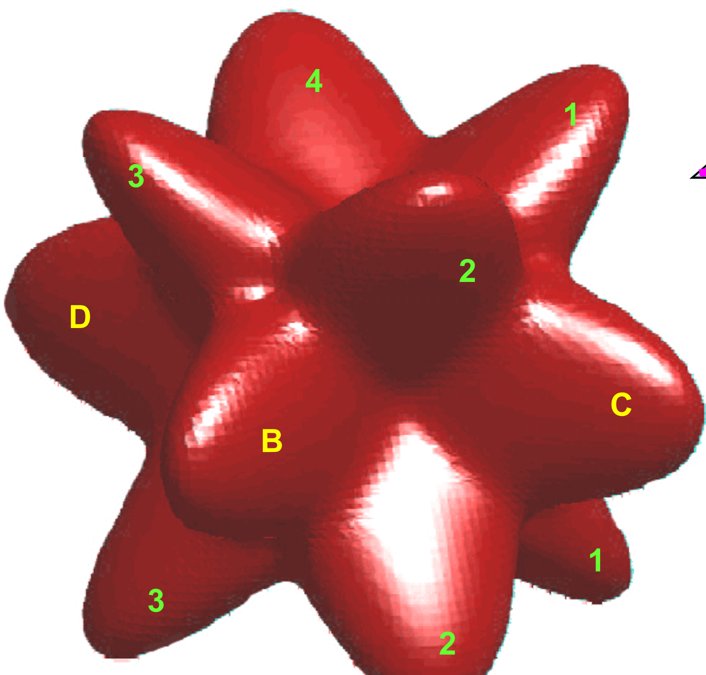
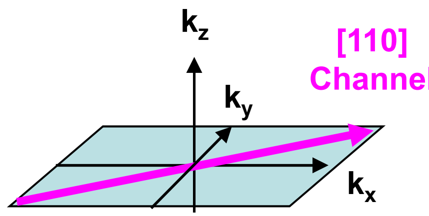
K.P Bandstructure: No Stress

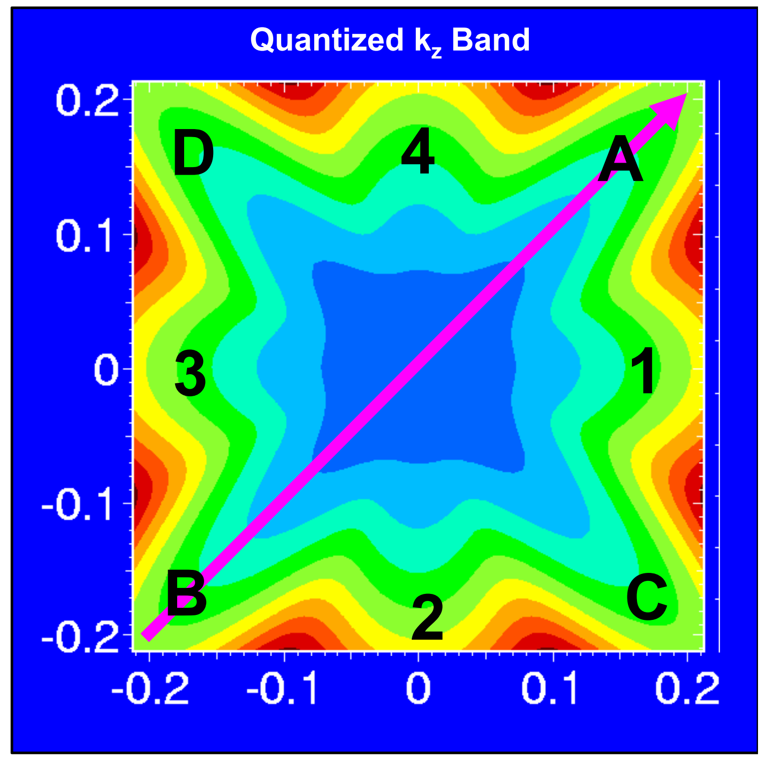
- Bulk heavy hole has 12 nodes
  - 4 of them are in k_z=0 plane
- Vertical gate field confines holes into an inversion layer
  - Moves from a bulk to a confined band structure
- 8 off-plane nodes projected to k_z=0 plane in quantized k.p



Bulk Band



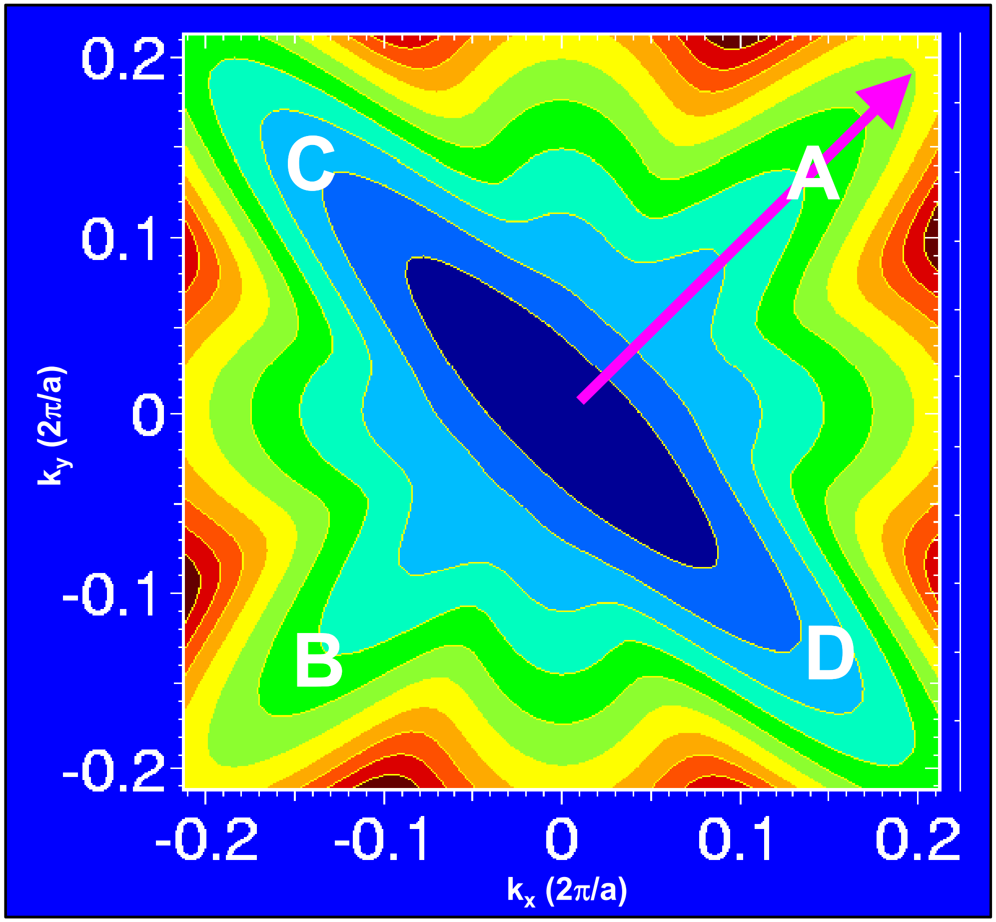
In-plane
Wings A,B,C,D
Off-plane
Wings 1,2,3,4



Giles et al., Wang et al.: IEDM 2004, 2006

Uniaxial Stress along [110]

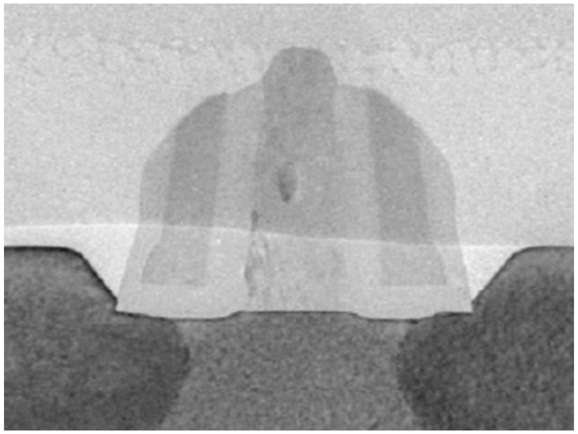
- Uniaxial stress along [110] has shear and biaxial components
- Shear compression lowers the energy of (C,D)
- Holes redistribute from (A,B) to (C,D)
- The effective mass and density of states (DOS) for scattering are reduced



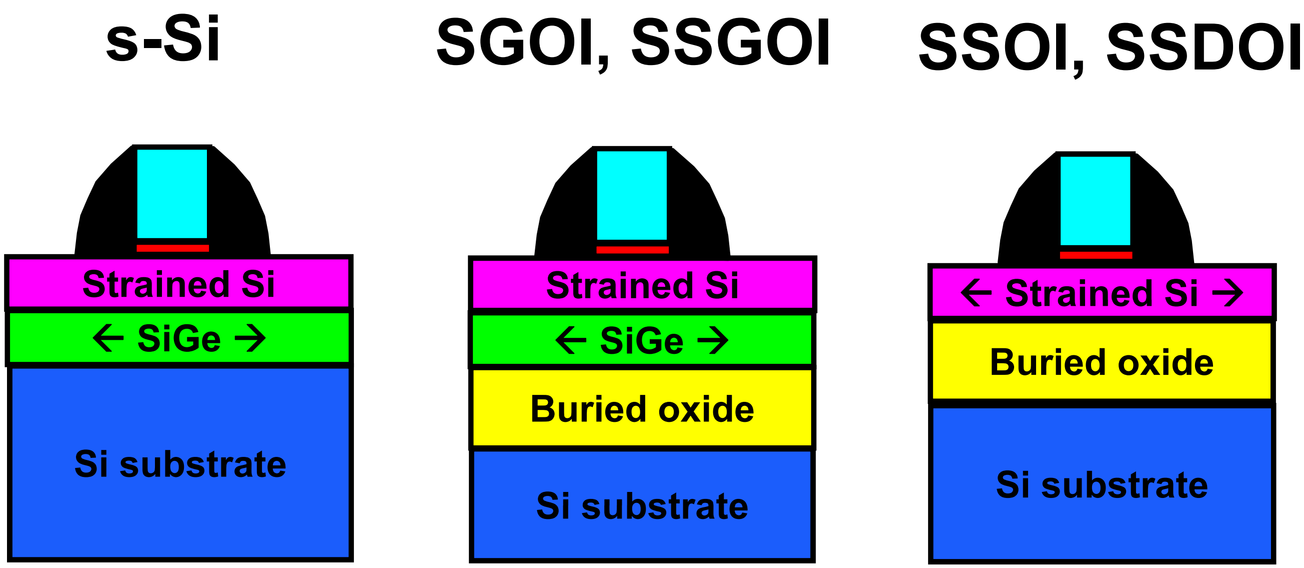
1GPa uniaxial stress along [110], (001) surface, 1MV/cm effective field, 30meV energy contours

Giles et al., Wang et al.: IEDM 2004, 2006

Uniaxial vs Biaxial



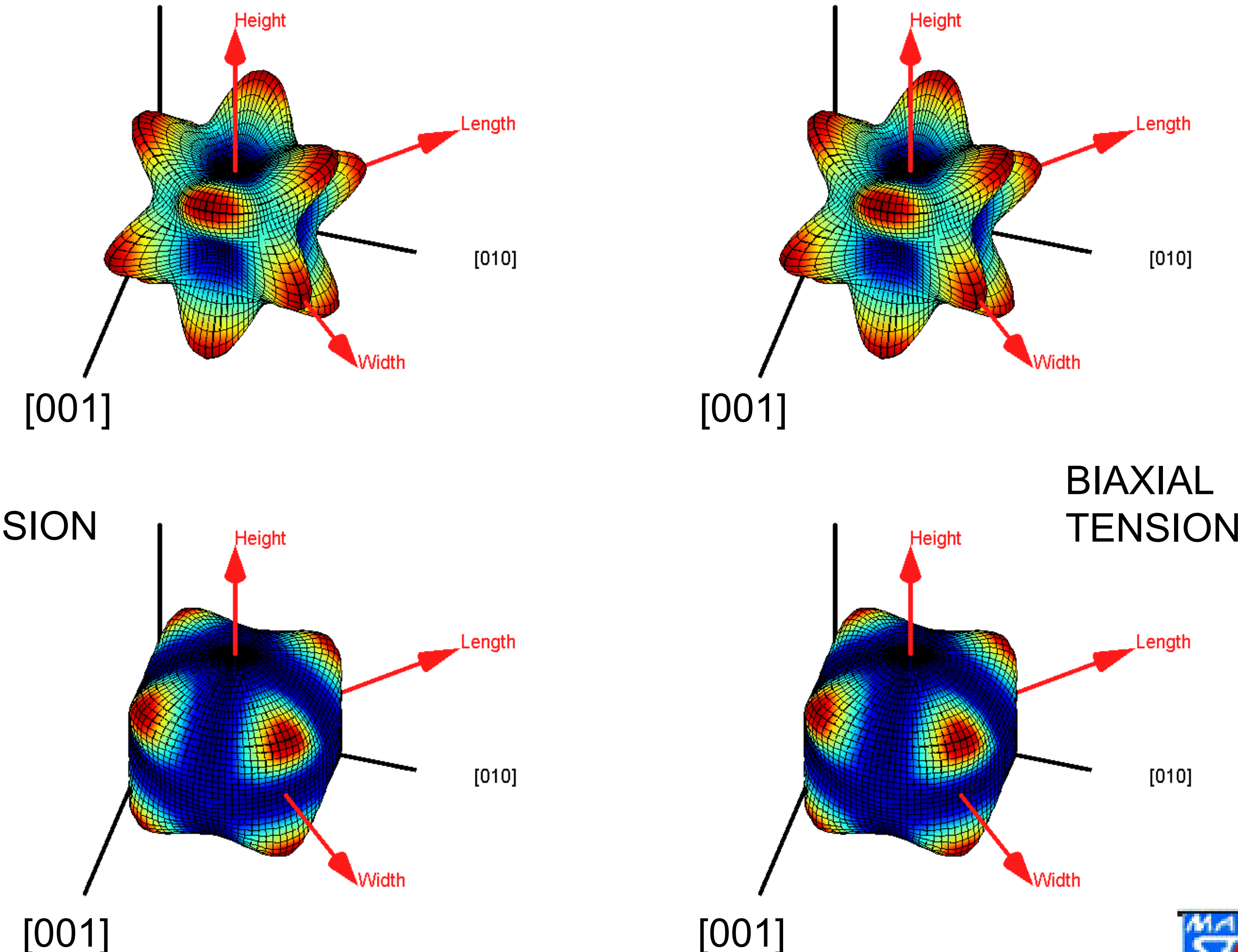
- Uniaxial strain introduced in a Si channel by SiGe in the S/D region.
- Biaxial strain introduced in a Si channel by SiGe below the channel region (or by a bonding process starting with SiGe below the channel region).

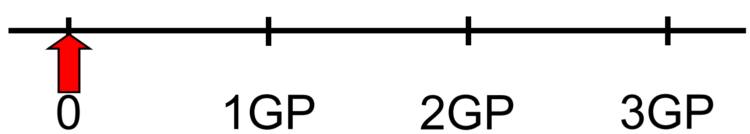


Calculated using MASTAR (http://www.itrs.net/models.html)

UNIAXIAL
COMPRESSION

BIAXIAL
TENSION





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IEDM SC 2008

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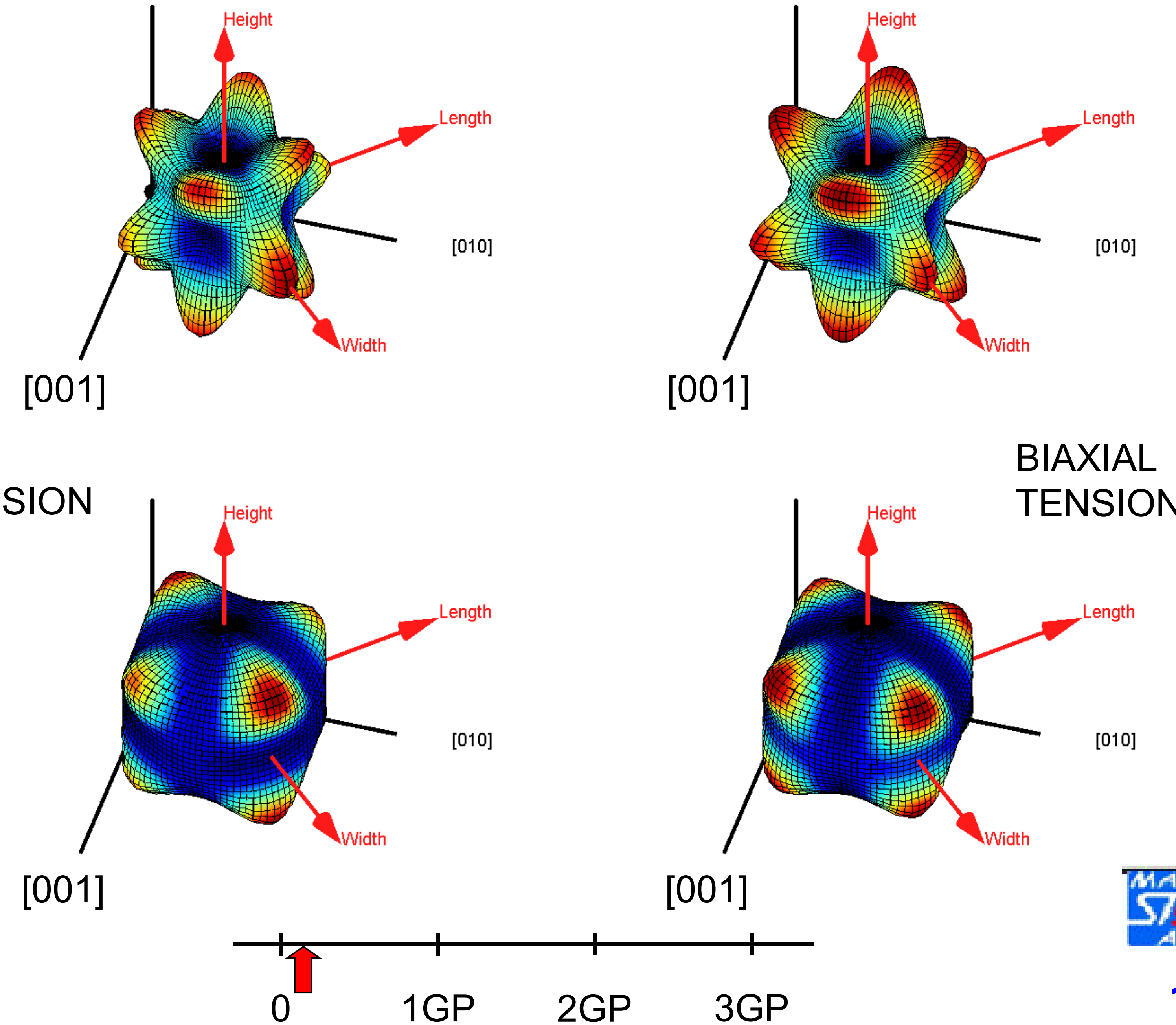

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IEDM SC 2008

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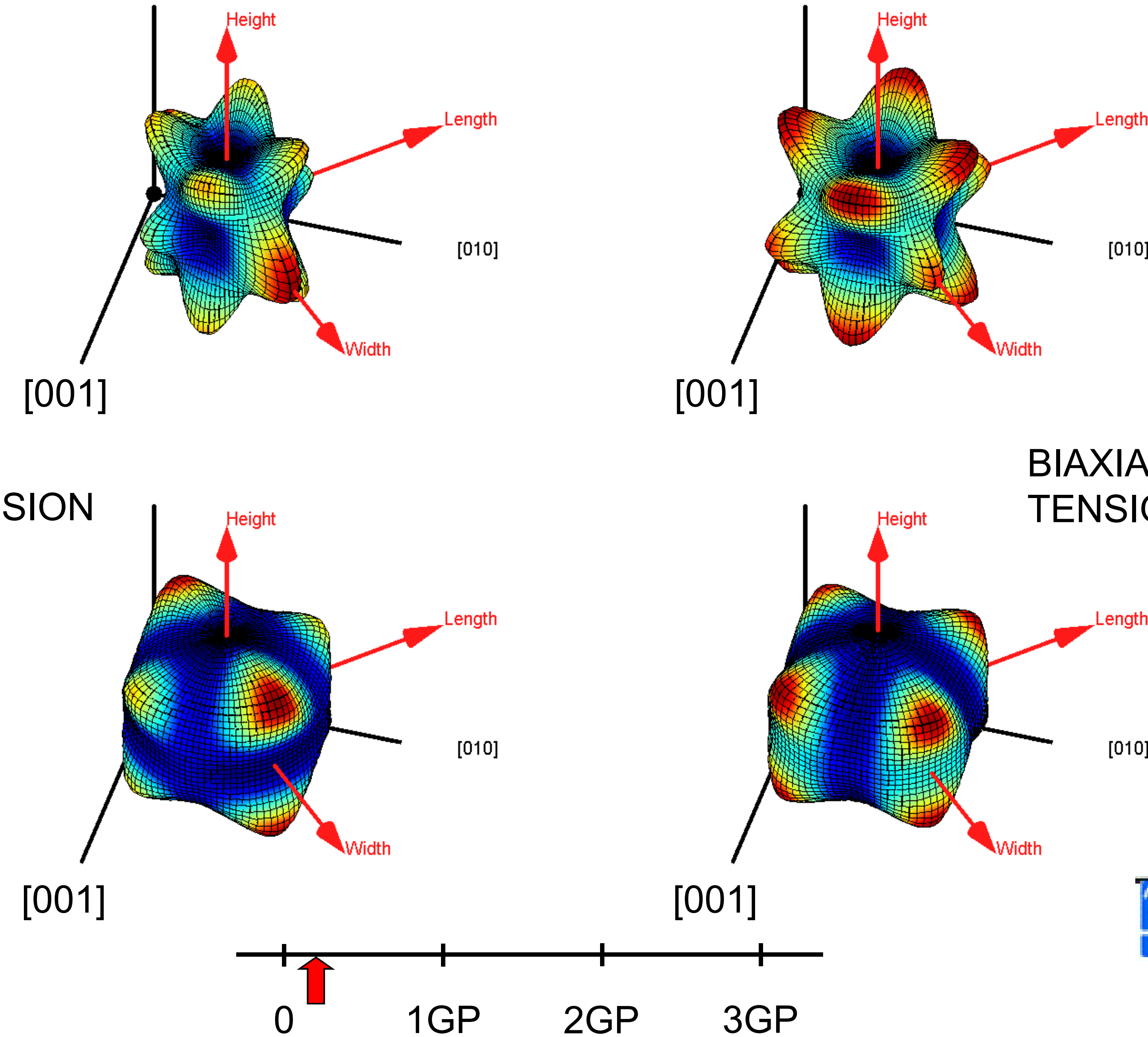
UNIAXIAL COMPRESSION

BIAXIAL TENSION



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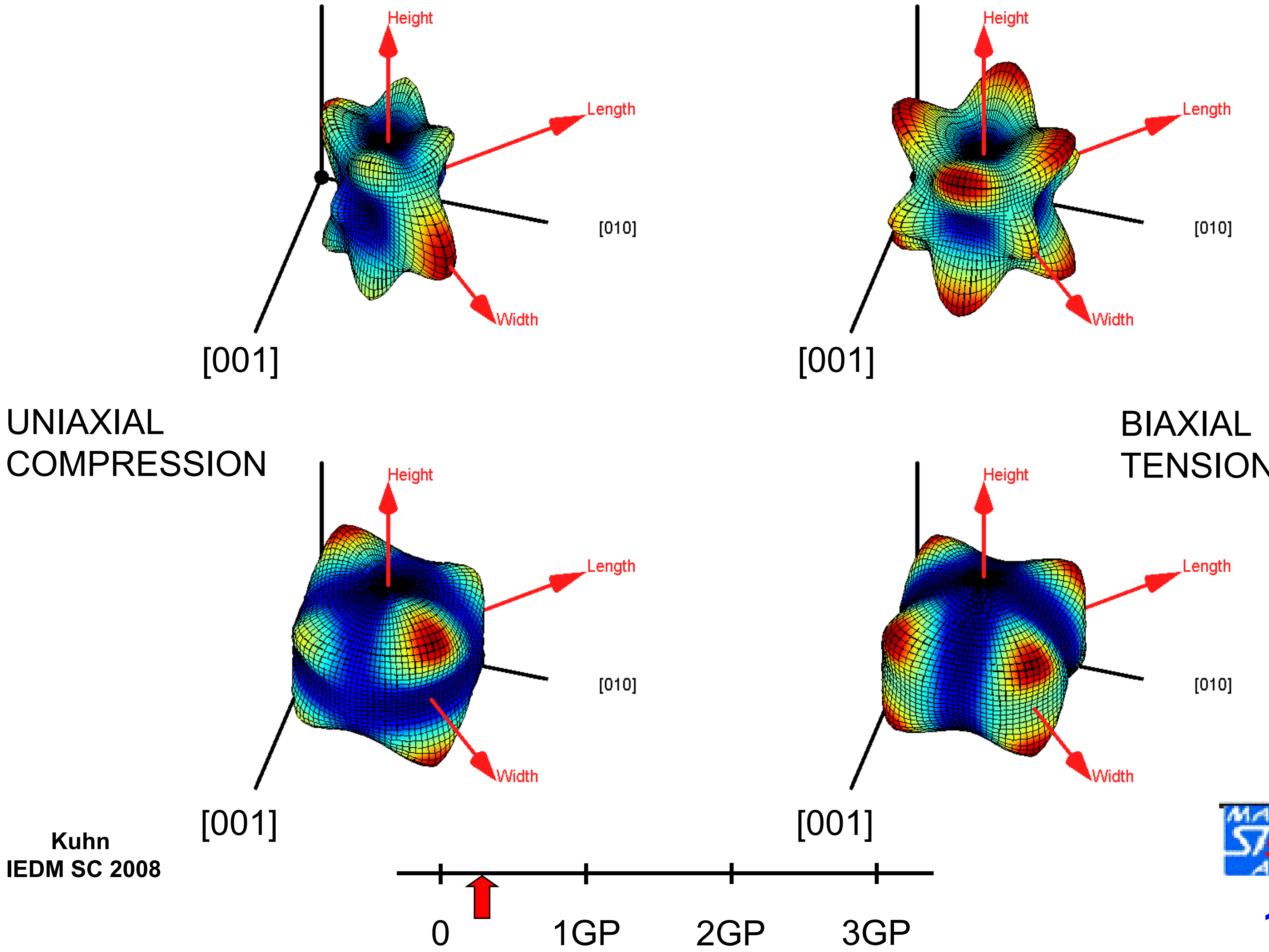

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IEDM SC 2008

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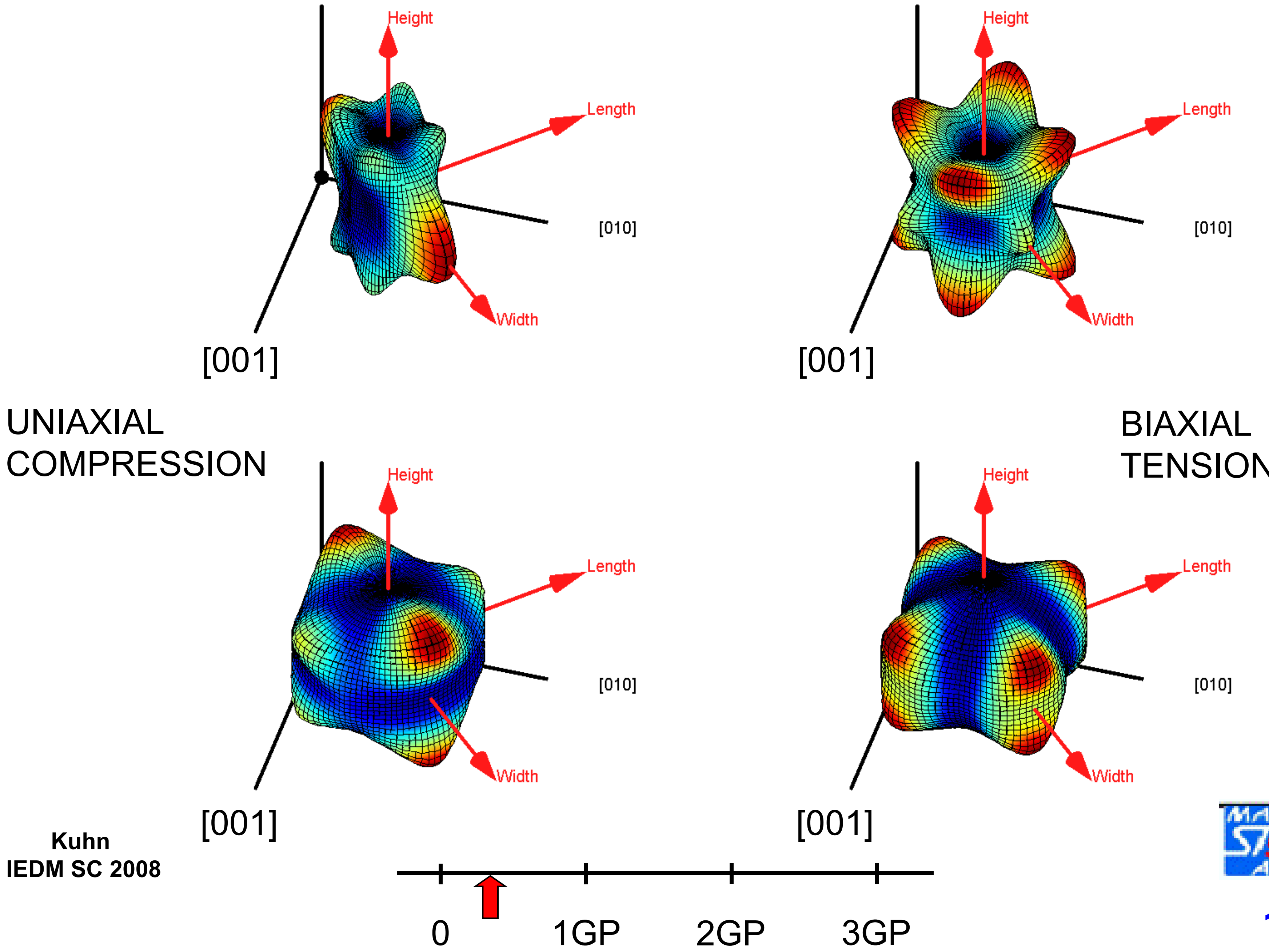

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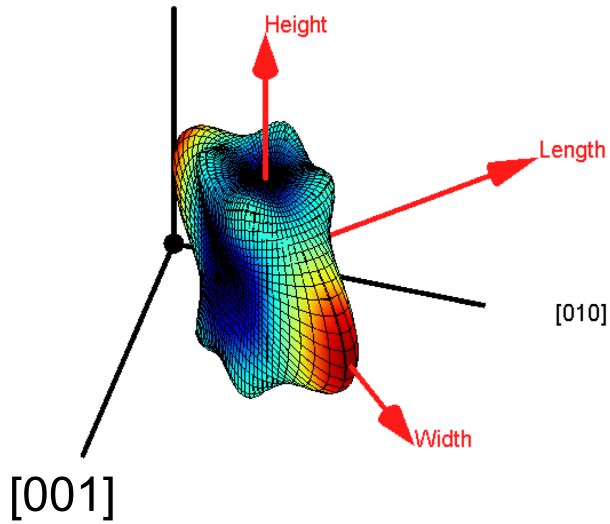

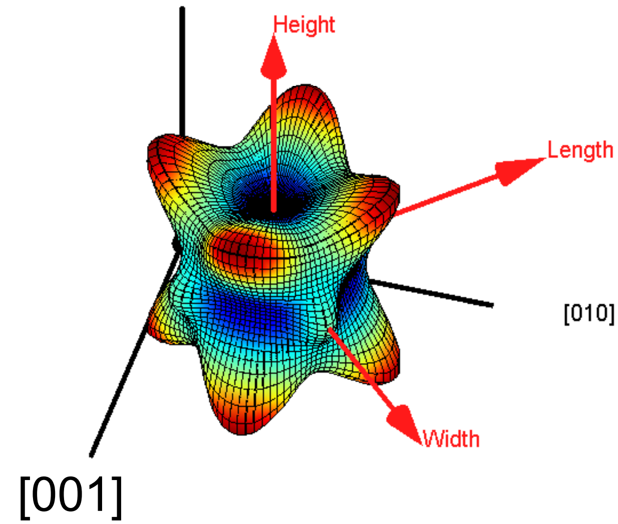

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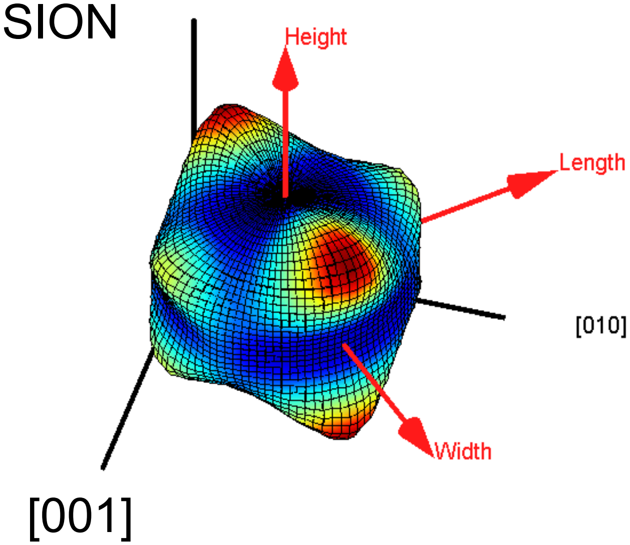
COMPRESSION



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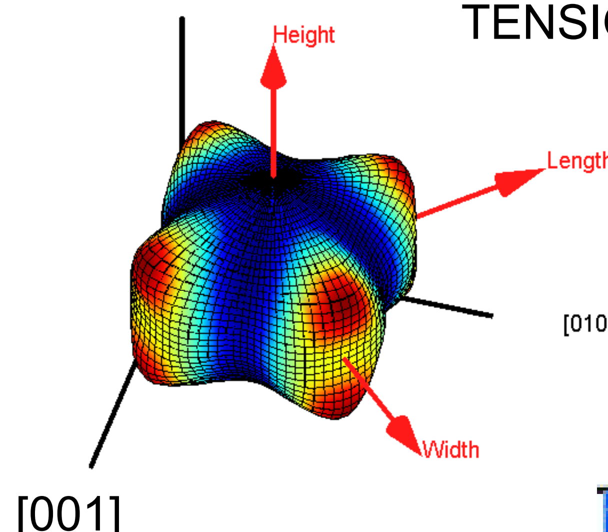

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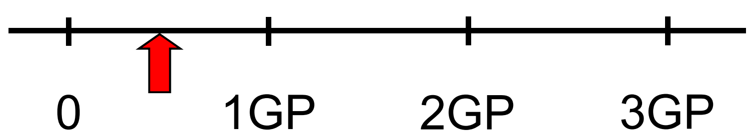
IEDM SC 2008



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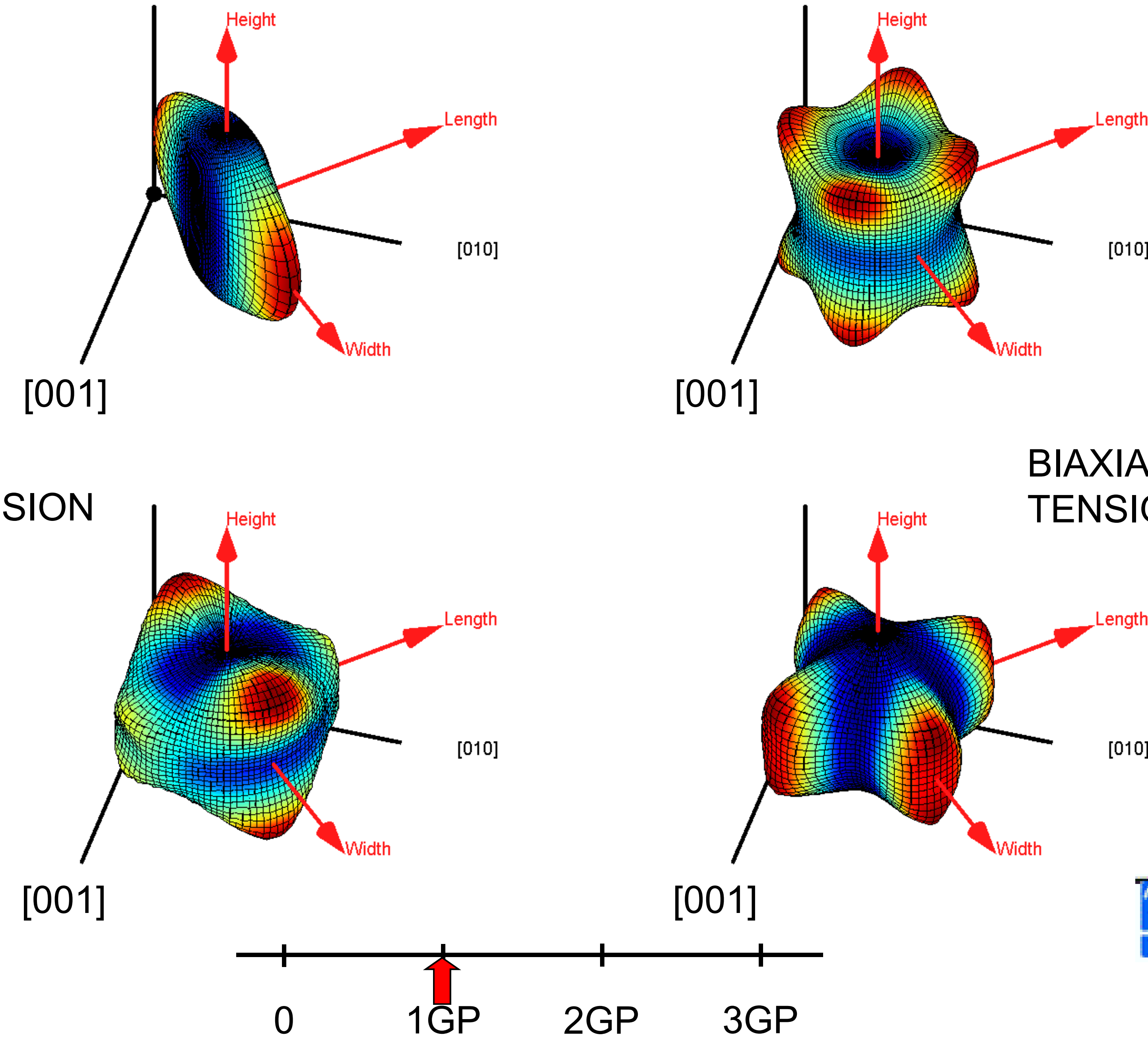

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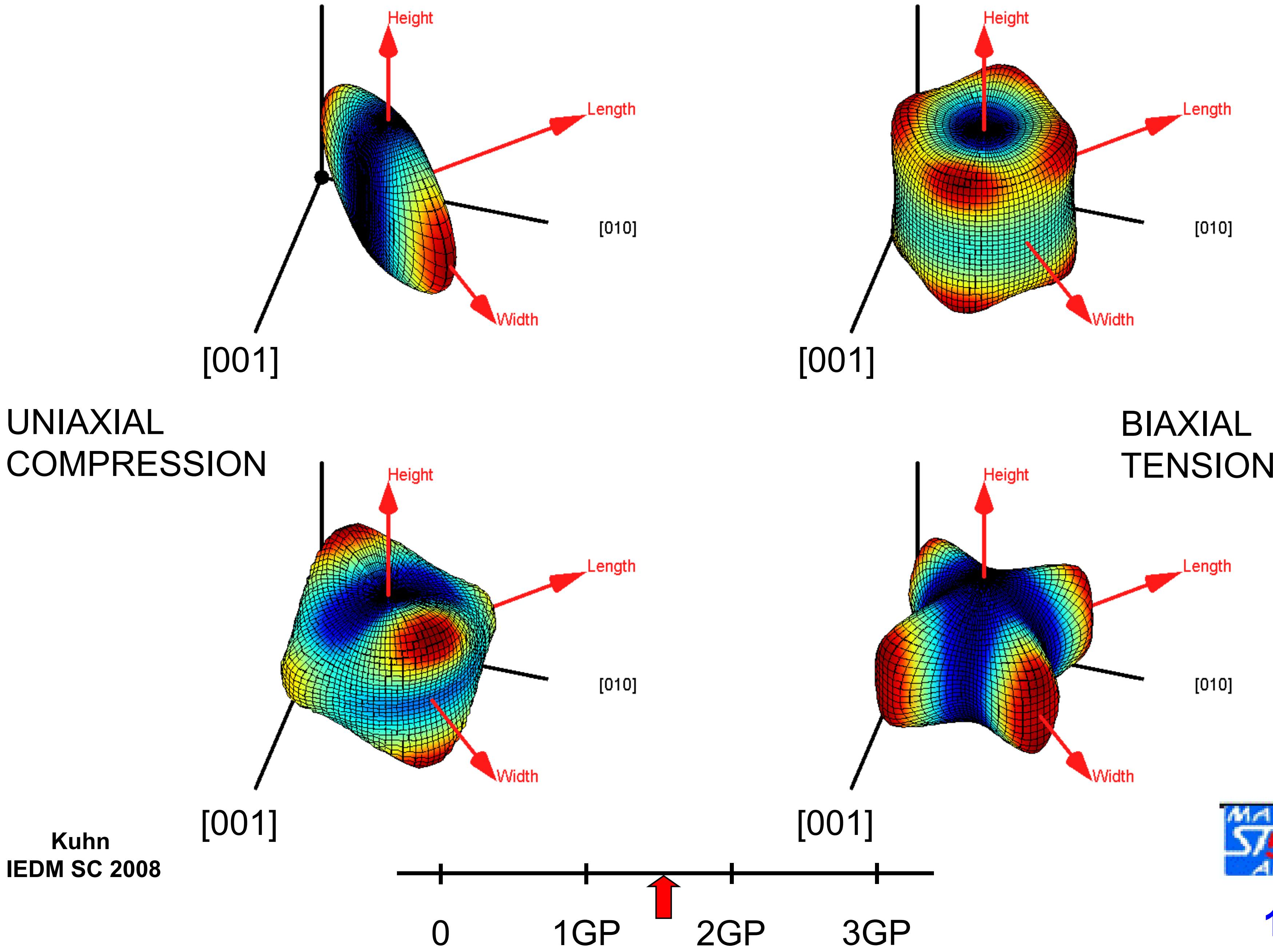

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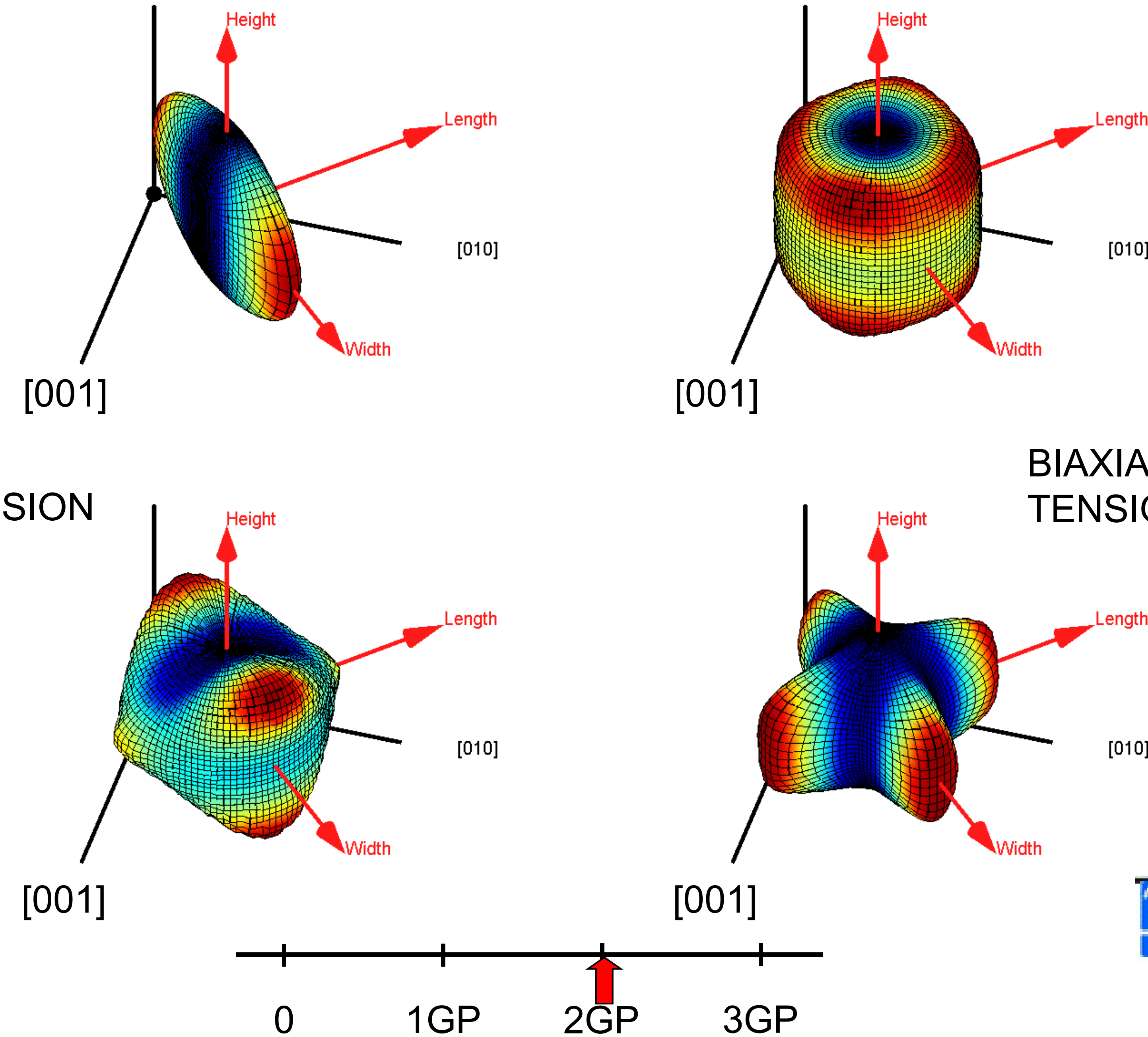

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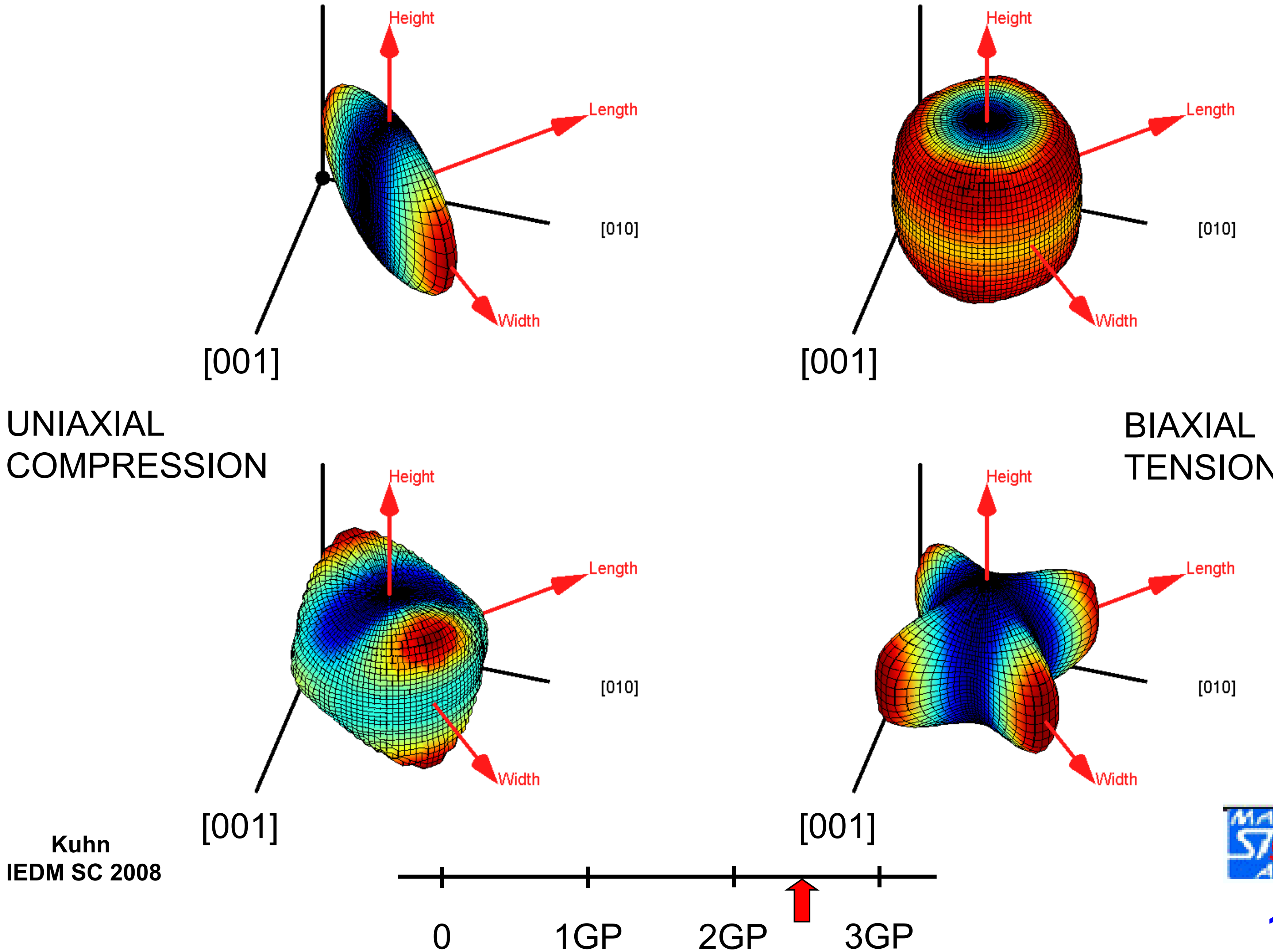
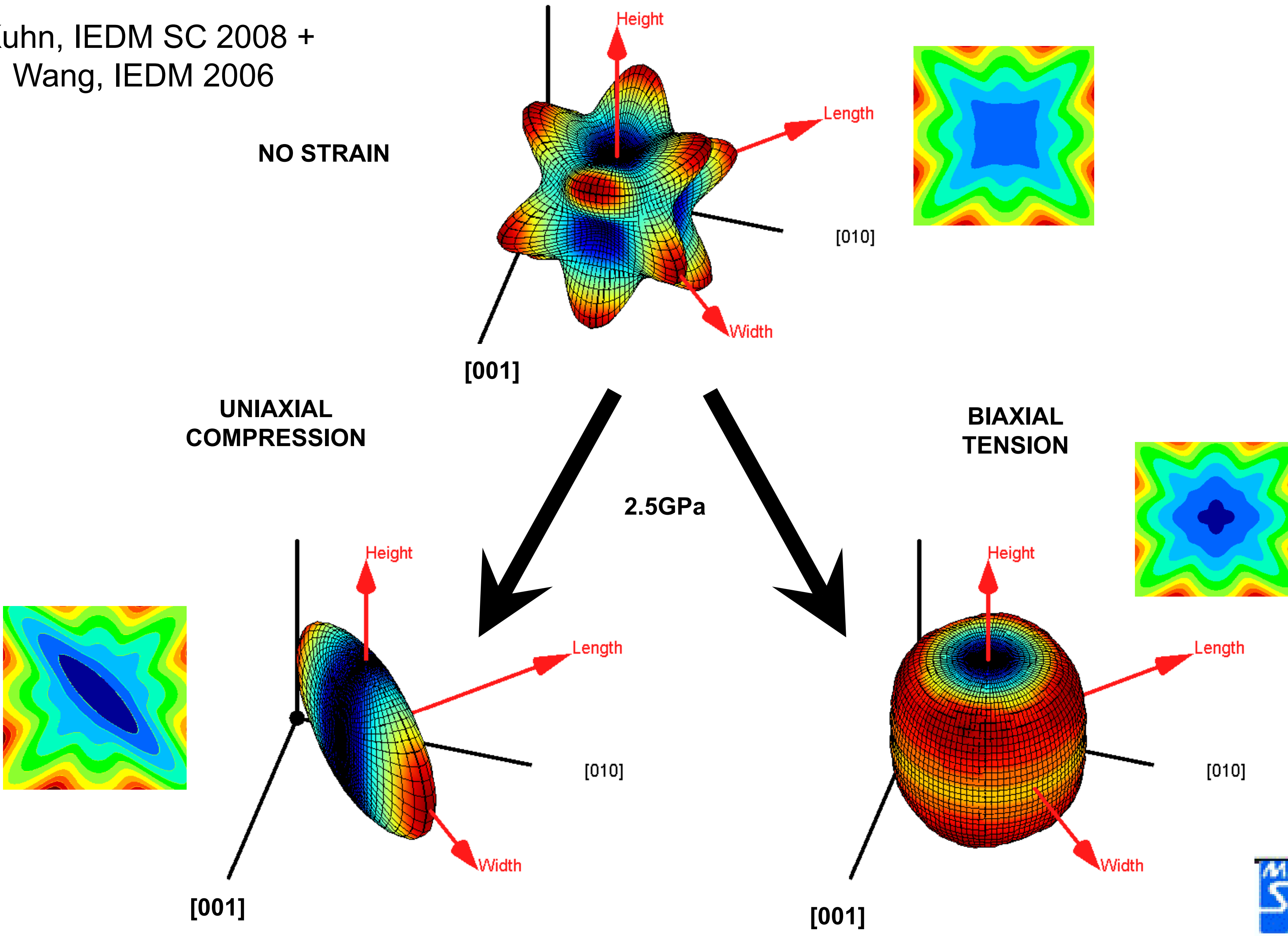


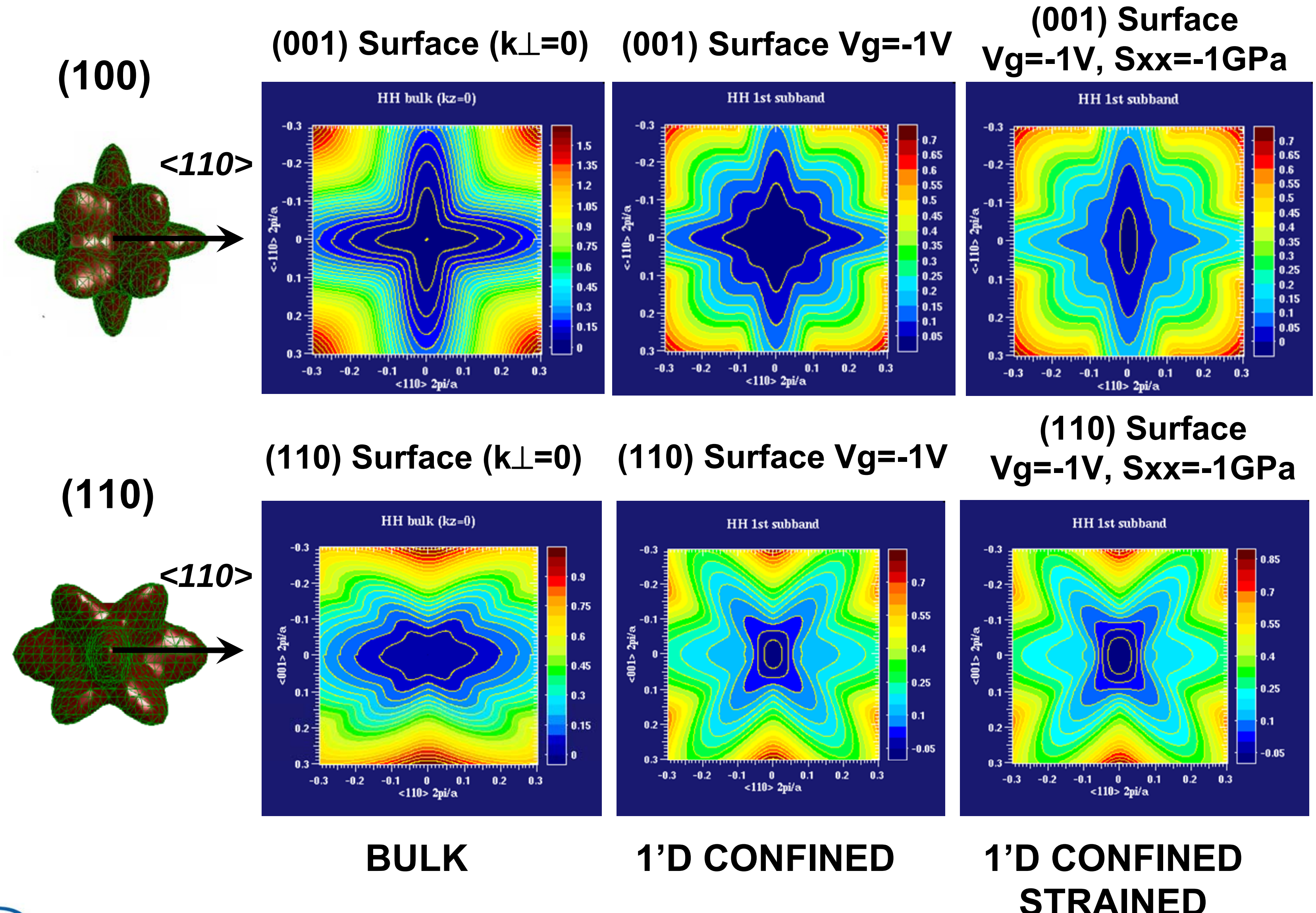
Kuhn
IEDM SC 2008

Kuhn, IEDM SC 2008 +
Wang, IEDM 2006



3D plots Calculated using MASTAR (http://www.itrs.net/models.html)

Orientation and Strain:
More complex for non-(100) orientations



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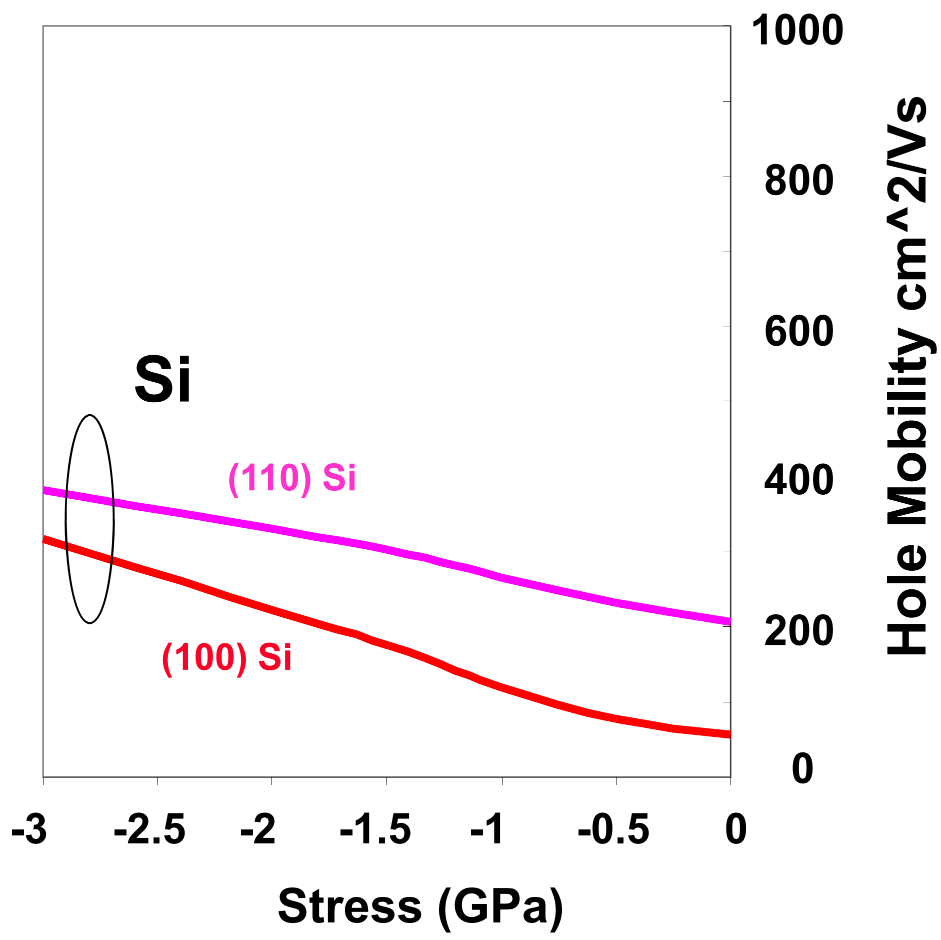


Orientation and Strain: More complex for non-(100) orientations

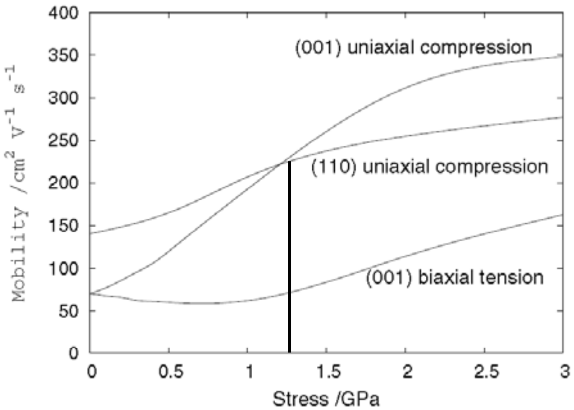
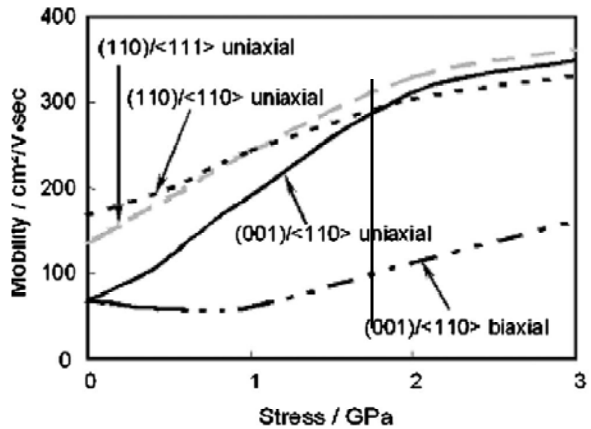
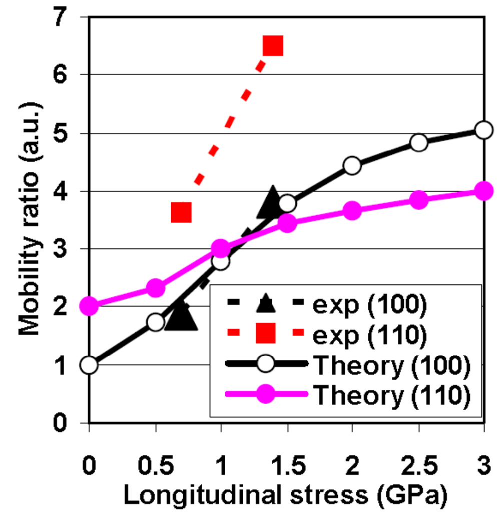


Fig. 9. Modeled mobility vs. longitudinal stress on (100) and (110) wafers. Note the low density of states on (110) limits the stress enhanced mobility.



[G. 3. Hole mobility vs stress (inversion charge=$1\times10^{13}/cm^2$). The en-hancement factor is the highest for (001)/⟨110⟩ and lowest for (110)/⟨110⟩ p-MOSFETs. At high stress (~3 GPa), the three longitudinal compressive uniaxial stress cases have comparable hole mobility.



Thompson – U of Florida
IEDM 2006

Sun – U of Florida
JAP 2007

Yang – AMD/IBM
IEDM 2007

"While (100) mobilities agree reasonably well, a strong discrepancy exists for (110) mobilities" - Yang, AMD/IBM, IEDM 2007, with reference to Thompson, IEDM 2006)

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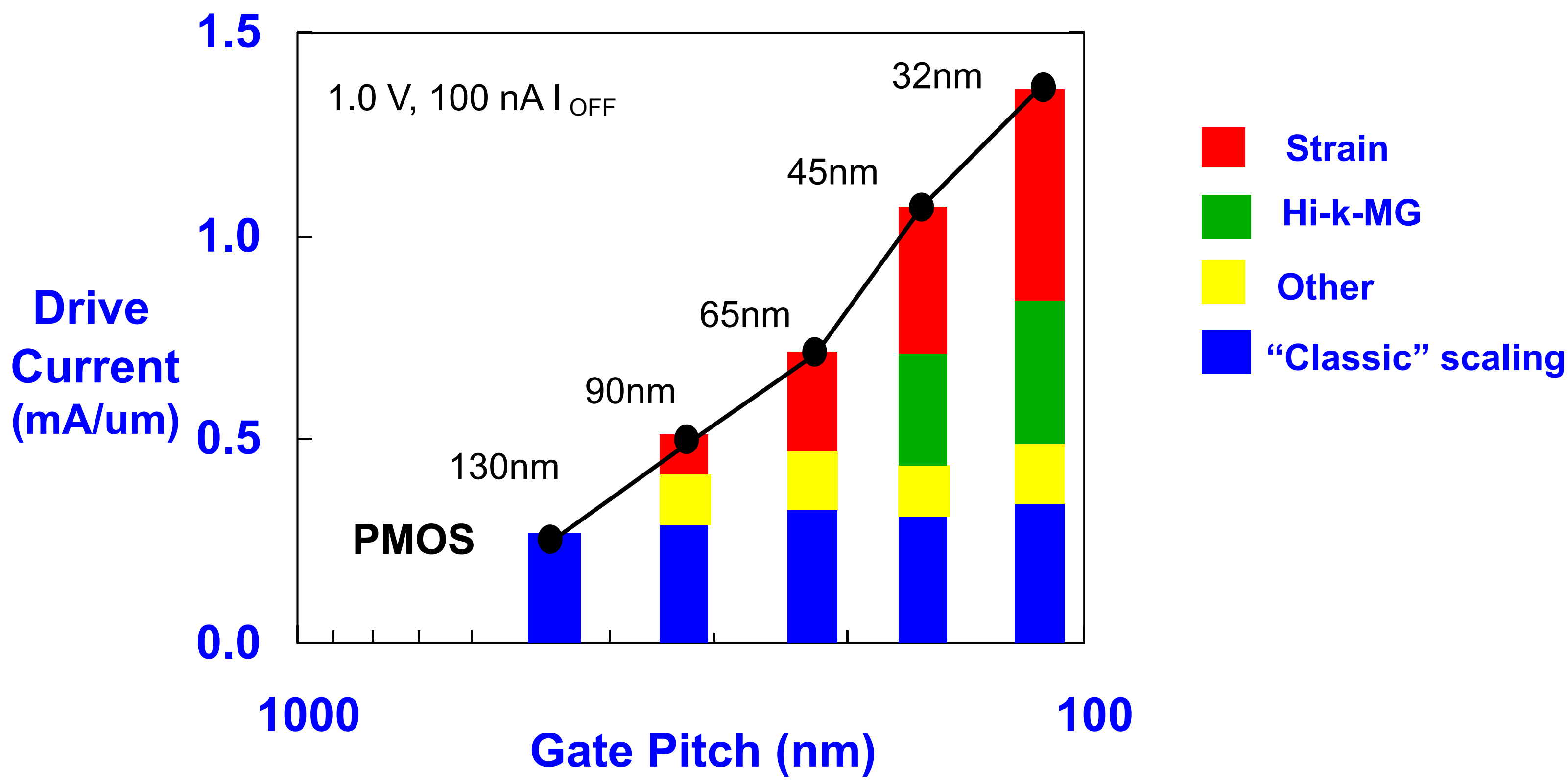
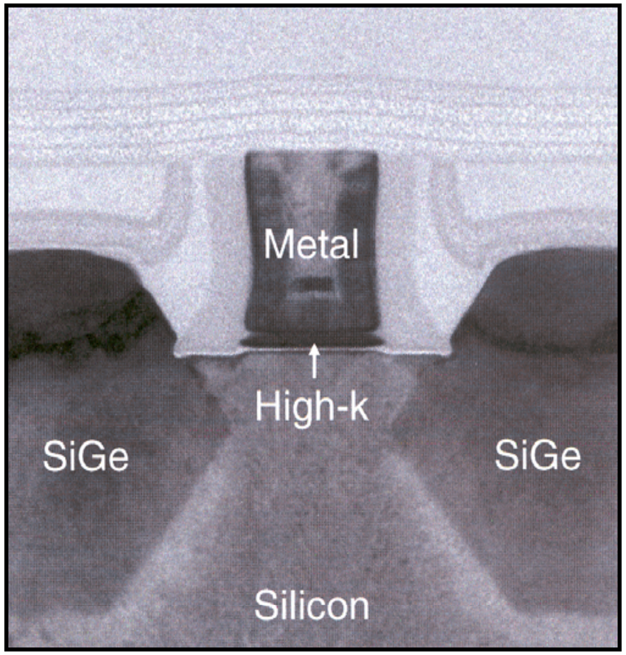
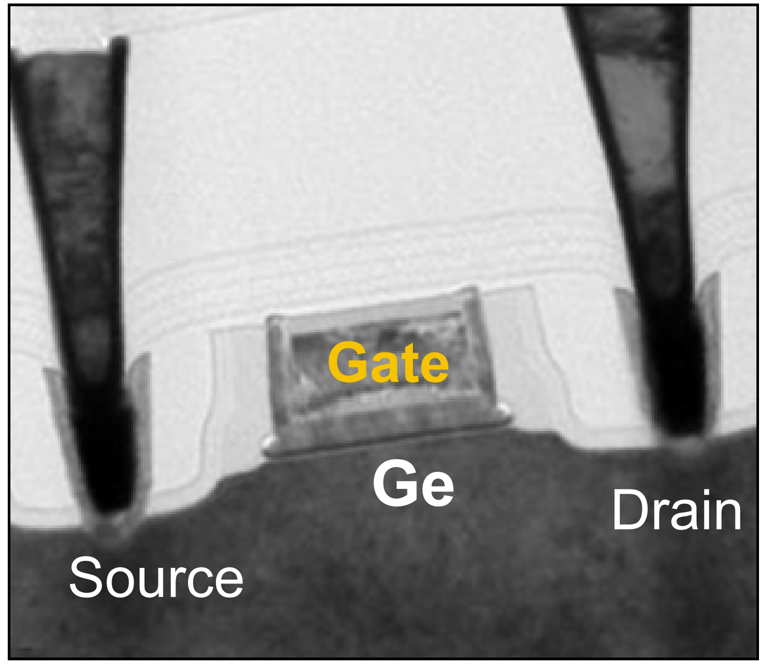


Manufacturable HiK-MG transistors were first introduced in the 45nm generation

Si vs Ge MOSFETs



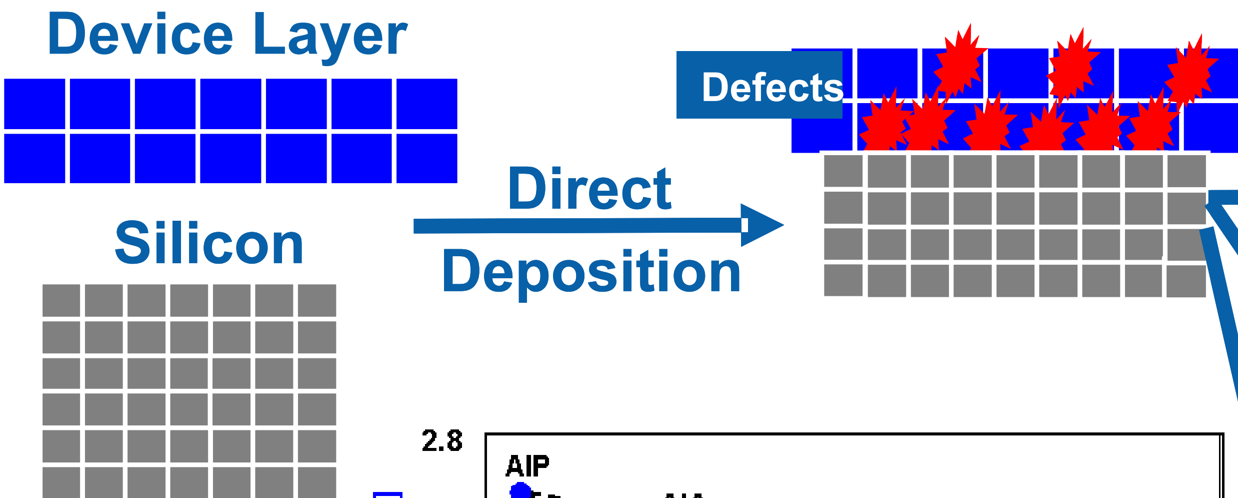
Intel 45nm HiK-MG Si device [43]

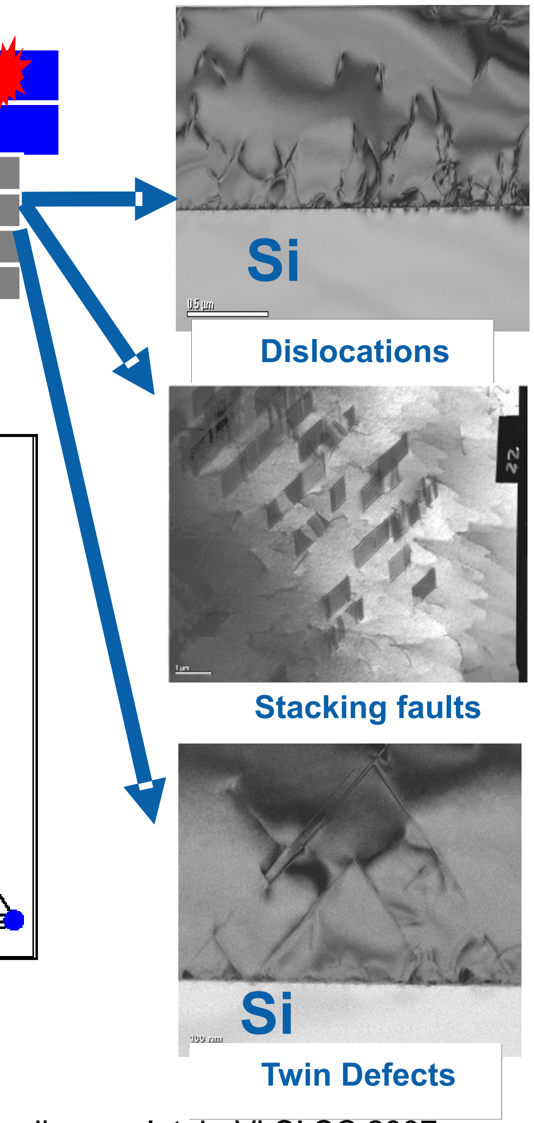


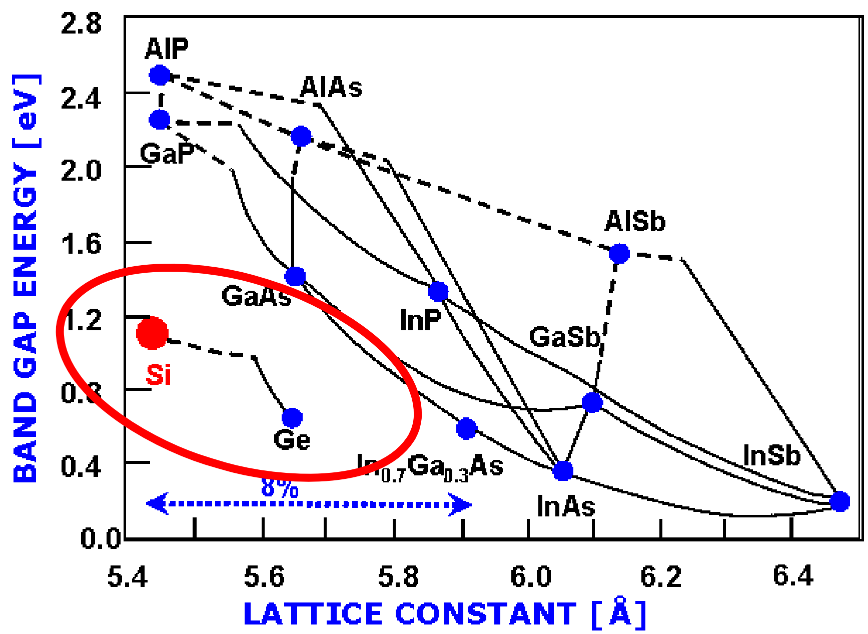
Intel HiK-MG Ge device

The introduction of manufacturable HiK-MG transistors has led to the reconsideration of Ge channels

Challenge of Lattice Mismatch Issues

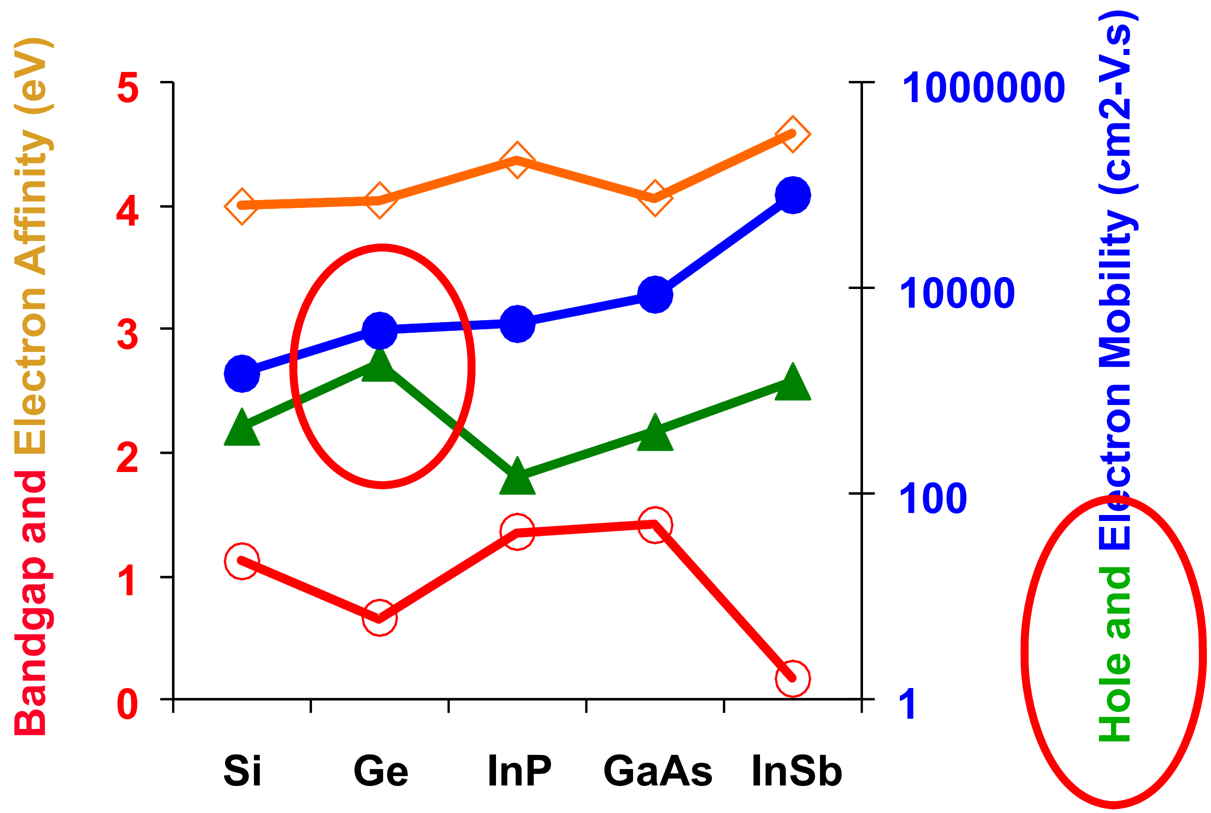






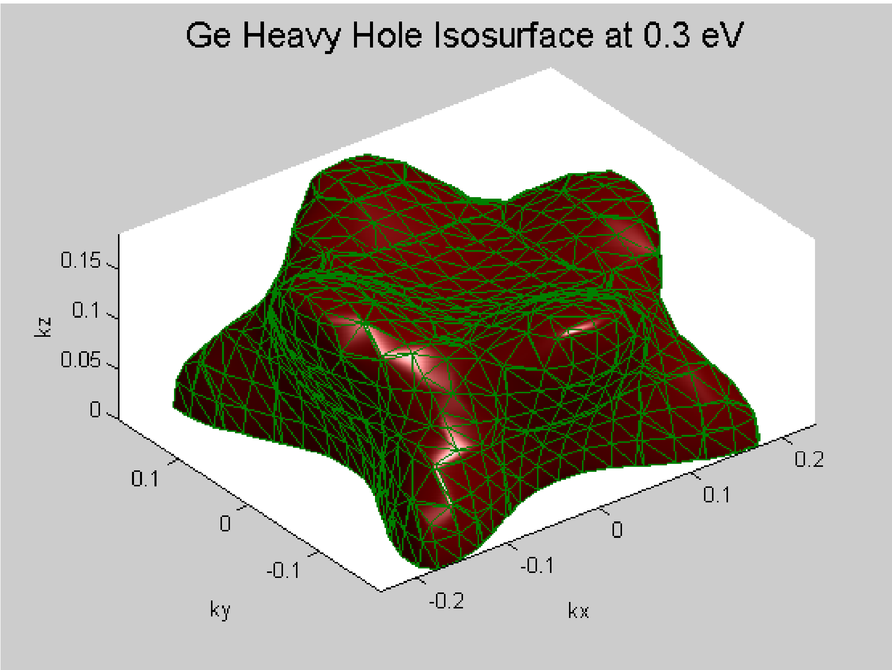
Adapted from J. Kavalieros – Intel - VLSI SC 2007

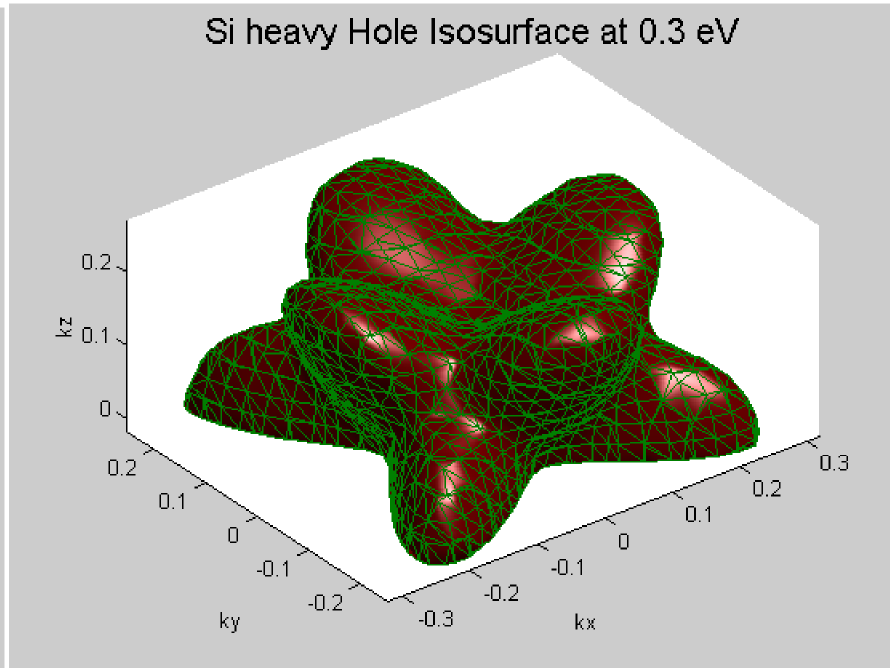
Ge and PMOS



Ge mobility makes it uniquely interesting for PMOS

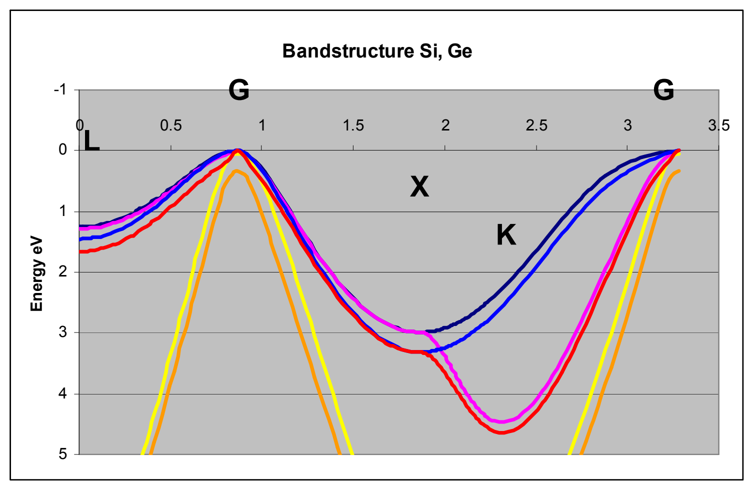
Si vs Ge Bandstructure/Parameters



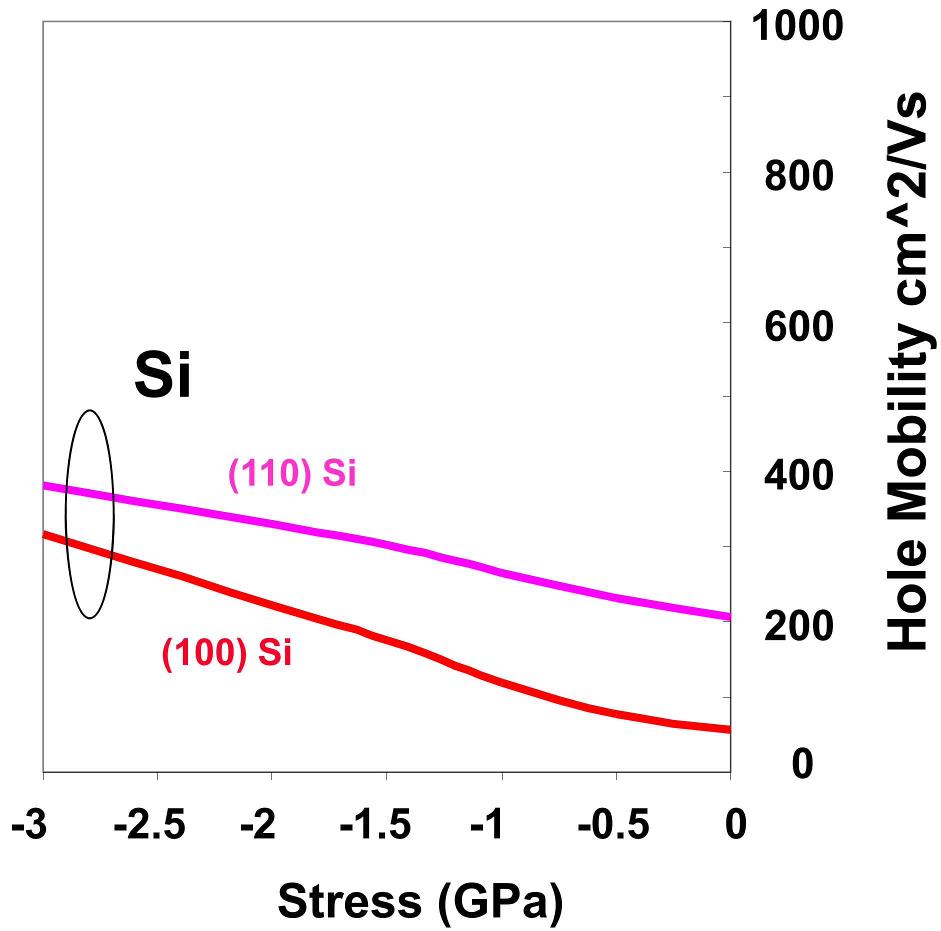


Band Masses at Gamma point (using kp parameters, in m_e):

	HH	LH	SO
Si	0.59	0.15	0.24
Ge	0.38	0.04	0.07



Low Field Long Channel Mobility
(as a function of stress)



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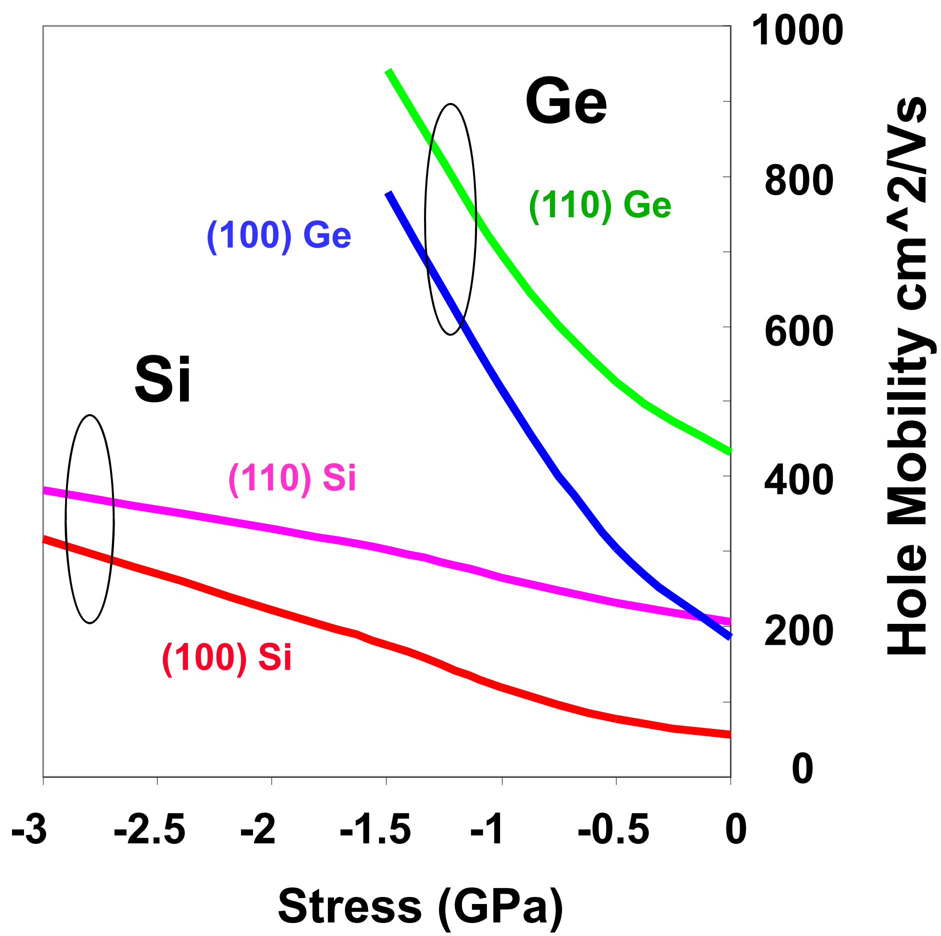
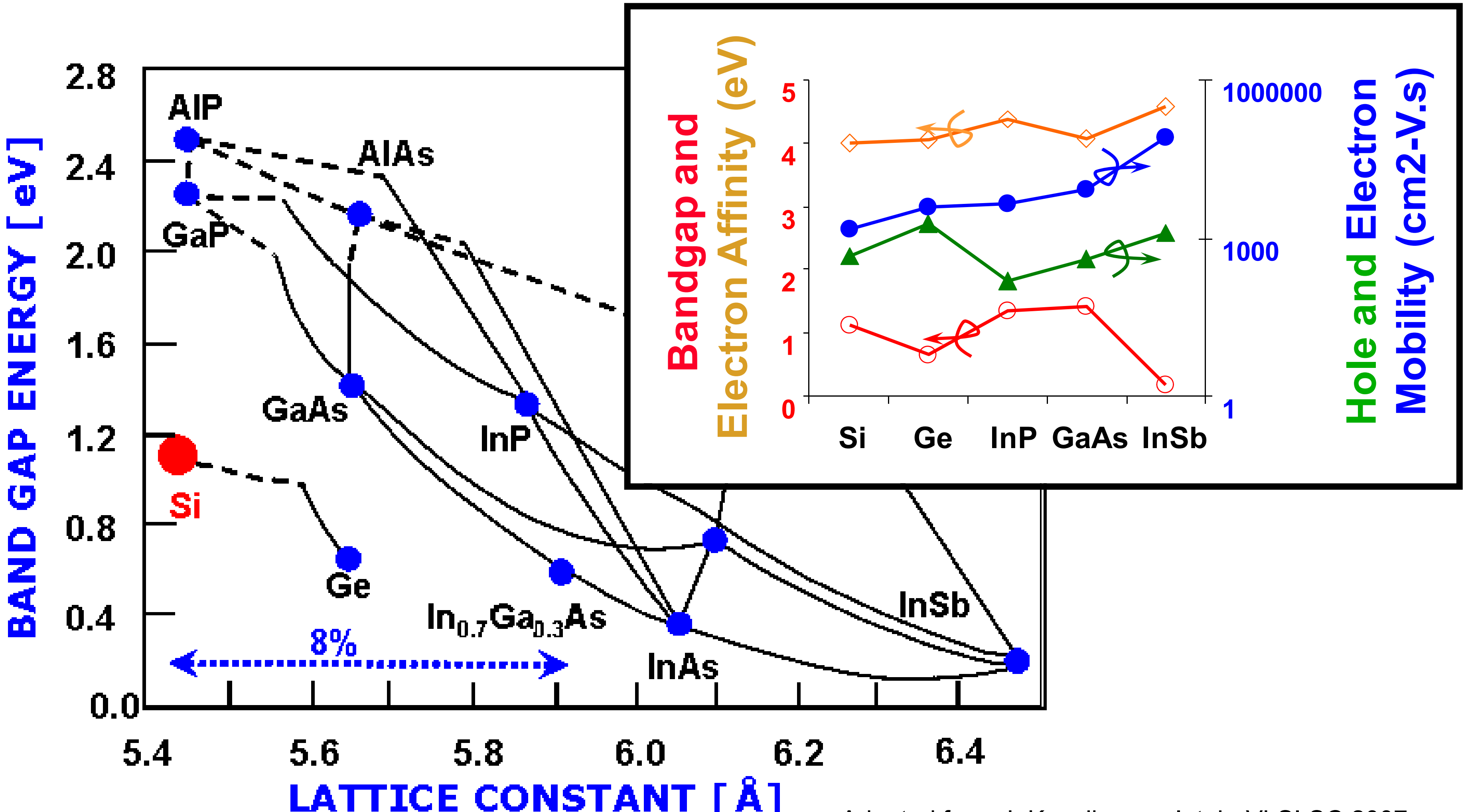


III-V vs Ge: NMOS
The Lure of High Mobility



Adapted from J. Kavalieros – Intel - VLSI SC 2007
K. Kuhn – ECS 2010

Low m* MOSFETs: "Density-of-states bottleneck"

From R. Kim

- **On-current of a MOSFET**

$$I = Q\upsilon$$

- **Velocity υ**
  - Diffusive : mobility μ, $\upsilon = \mu \mathscr{E}$
  - Ballistic: injection velocity υ_{inj}
  - Light $m^* \rightarrow$ high μ, high υ_{inj}
- **Charge Q**
  - MOS limit ($C_Q \gg C_{ox}$), $C \approx C_{ox}$
  - Light $m^* \rightarrow$ less D (C_Q), less C, less Q
  - More important for thin oxide (large C_{ox}),

  "DOS bottleneck"

$$Q = C\left(V_G - V_{th}\right)$$

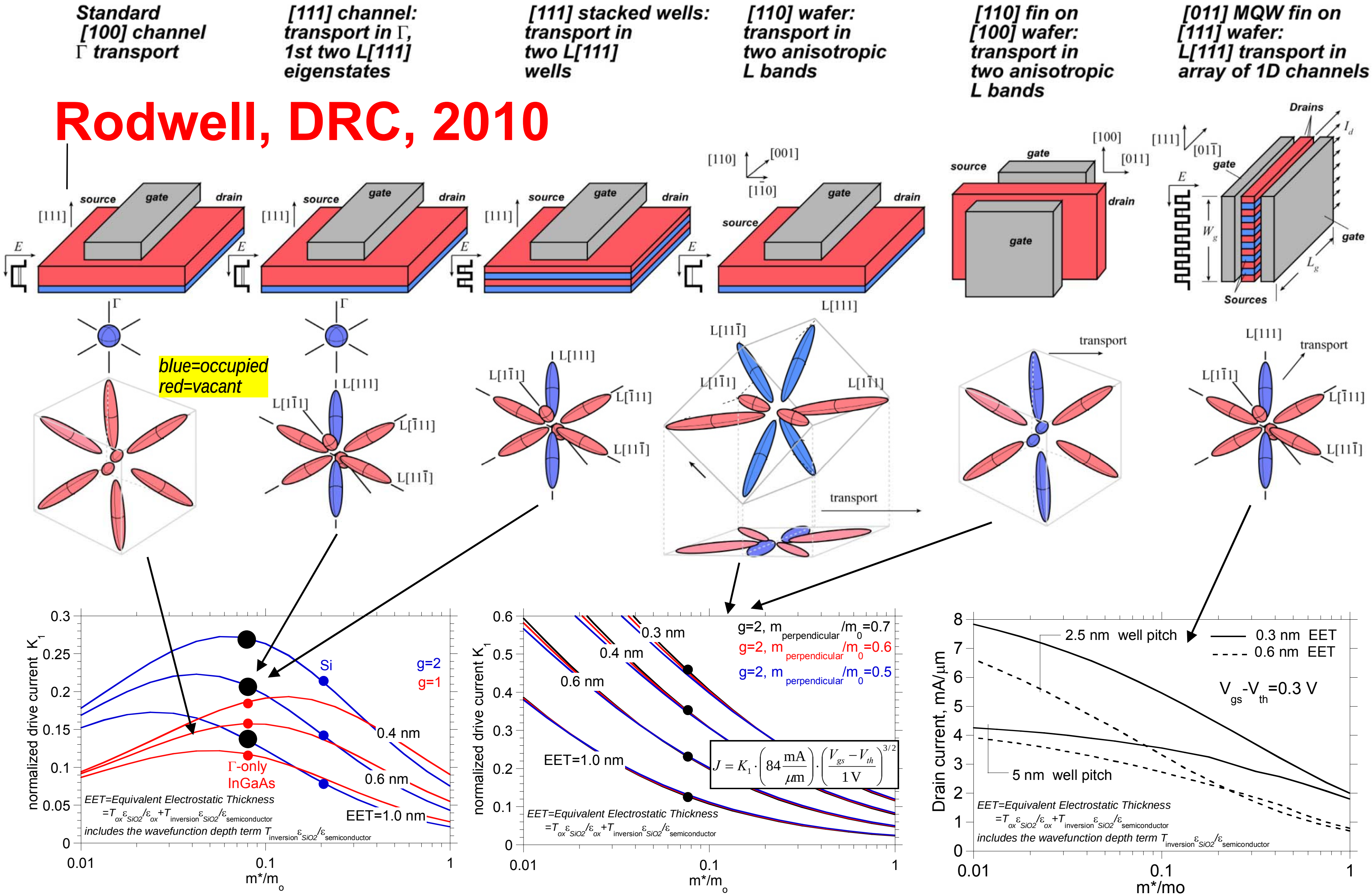
$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_Q}$$

$$C_Q = q^2 D$$

5 High-Current L & Γ-L channels: 5 Approaches

Rodwell et al, 2010 Device Research Conference 6/21/2010

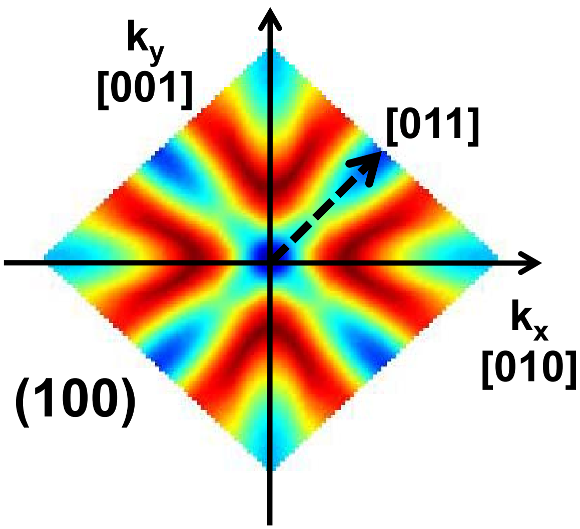
Rodwell, DRC, 2010

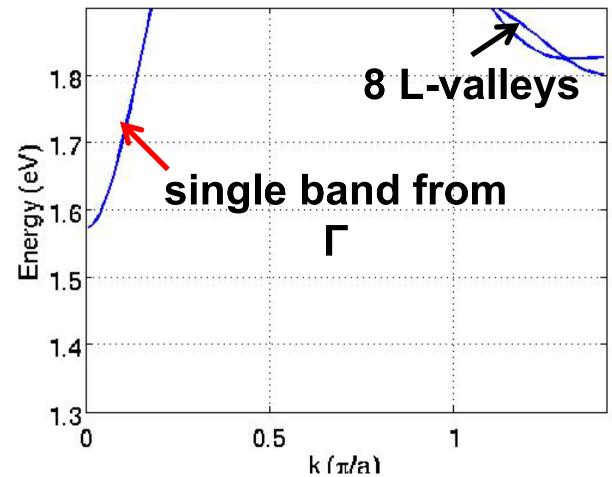


Use of L-valleys: GaAs

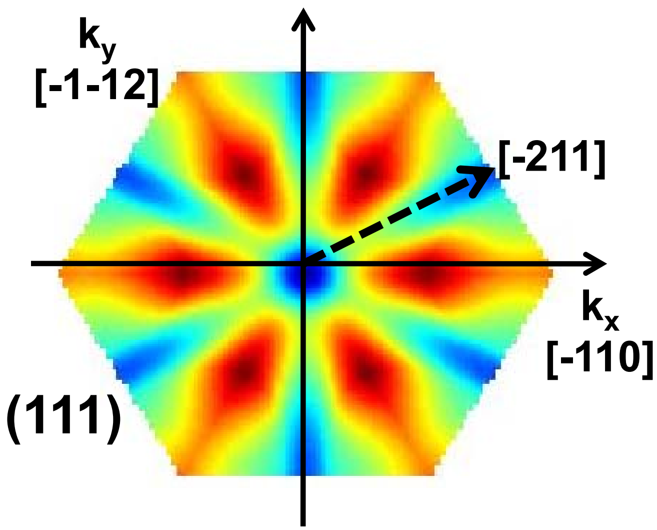
From R. Kim

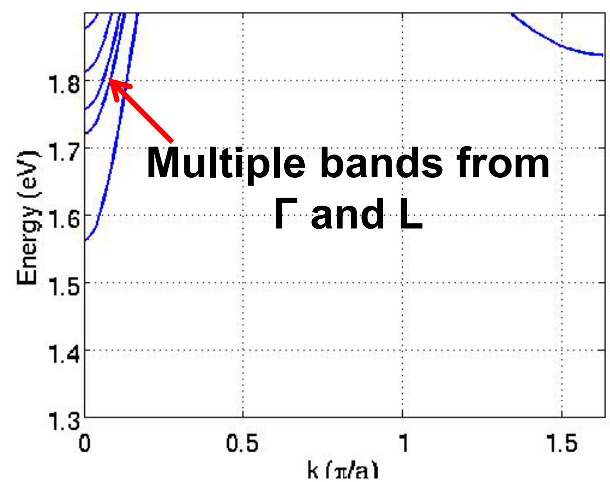
- **GaAs 4 nm**





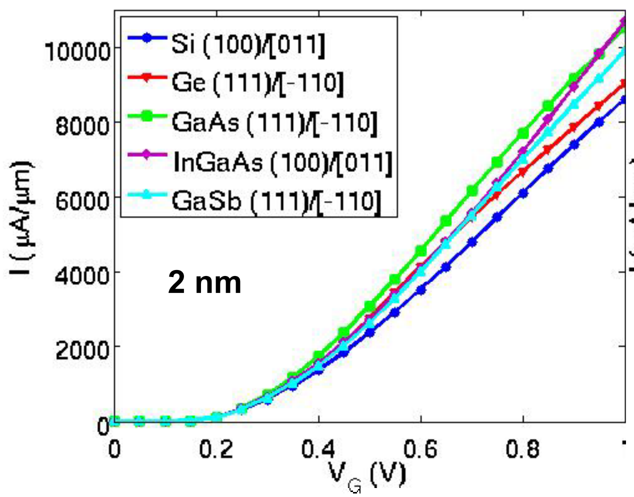
Small DOS with high v_{inj}
High DOS with low v_{inj}



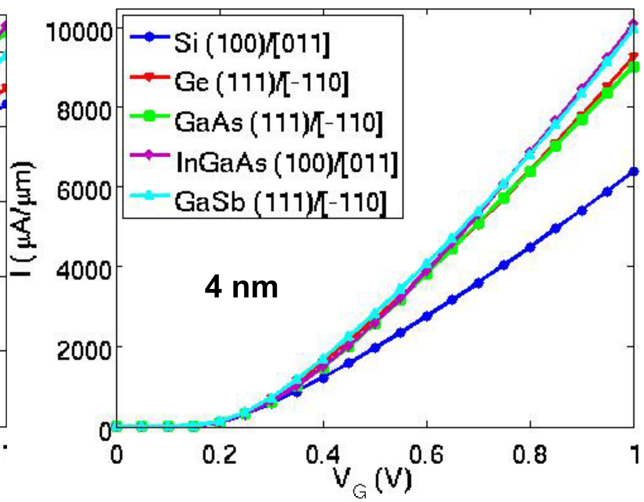


More DOS with high v_{inj}

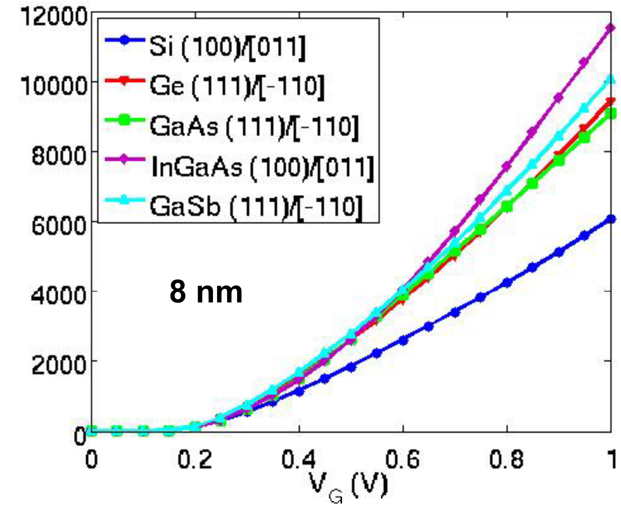
Different body thicknesses (EOT=1.0 nm)



GaAs>InGaAs>GaSb>Ge>Si

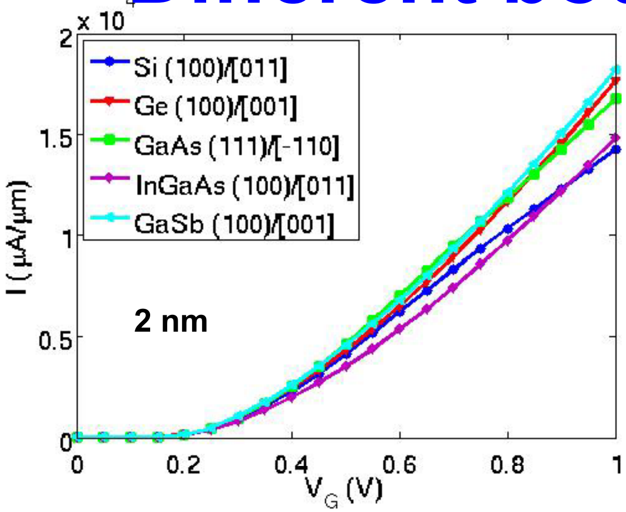


GaSb,InGaAs>Ge,GaAs>Si

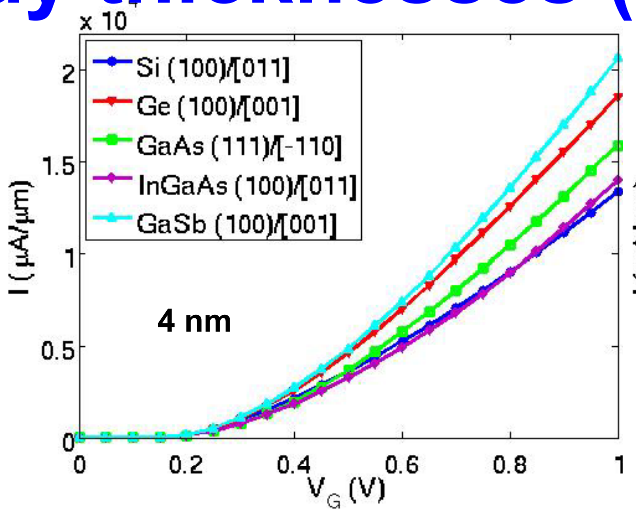


InGaAs>GaSb>Ge,GaAs>Si

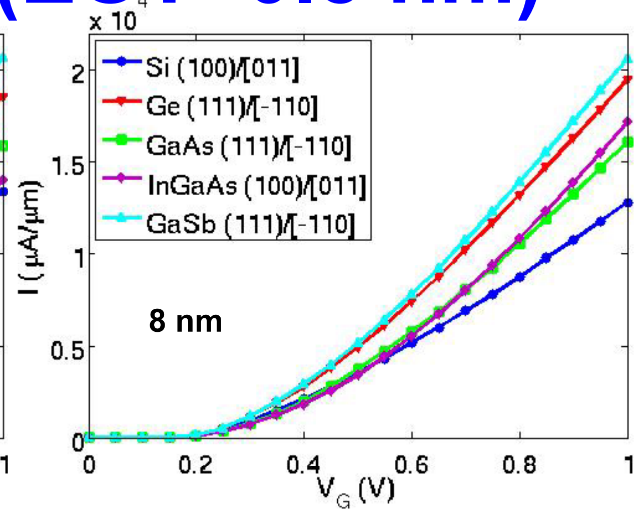
Different body thicknesses (EOT=0.5 nm)



GaSb>GaAs>Ge>Si>InGaAs



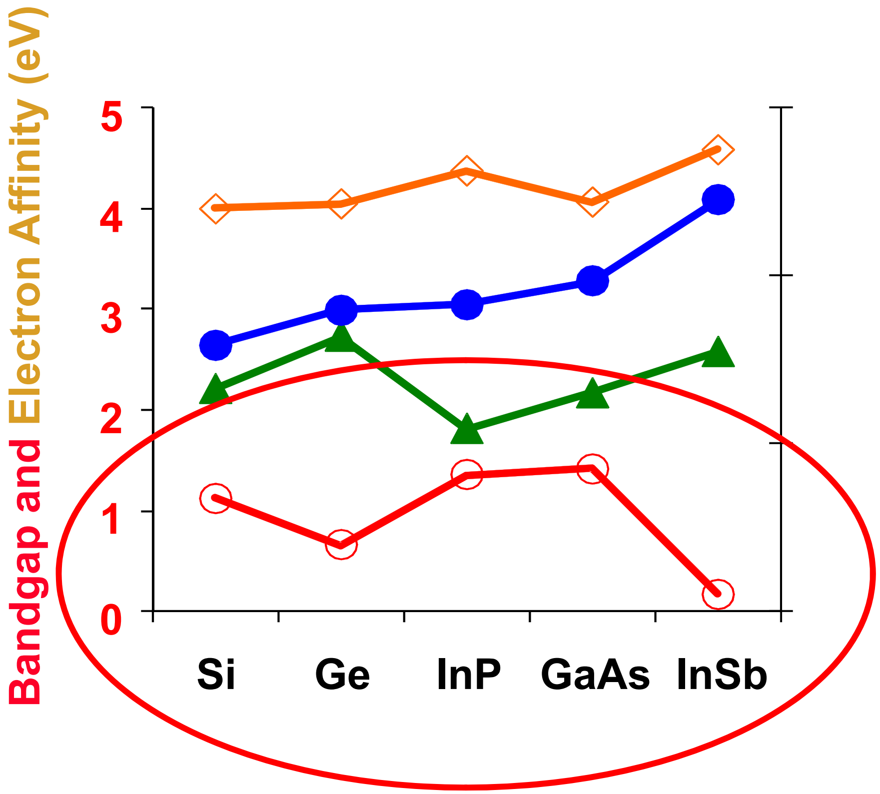
GaSb>Ge>GaAs>Si,InGaAs



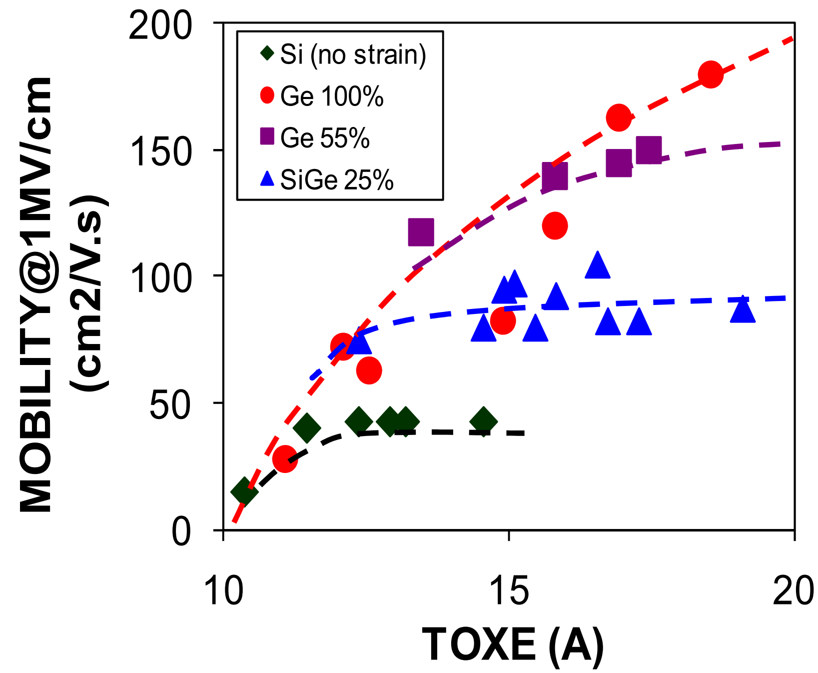
GaSb>Ge>GaAs, InGaAs>Si

From R. Kim

Ge Historical Issues:
Still critical today



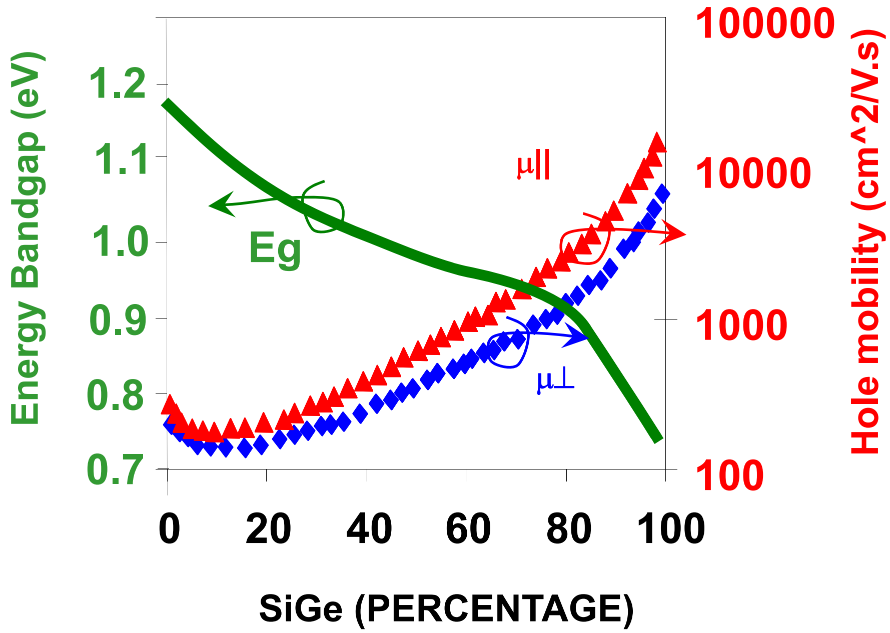
Narrow Bandgap

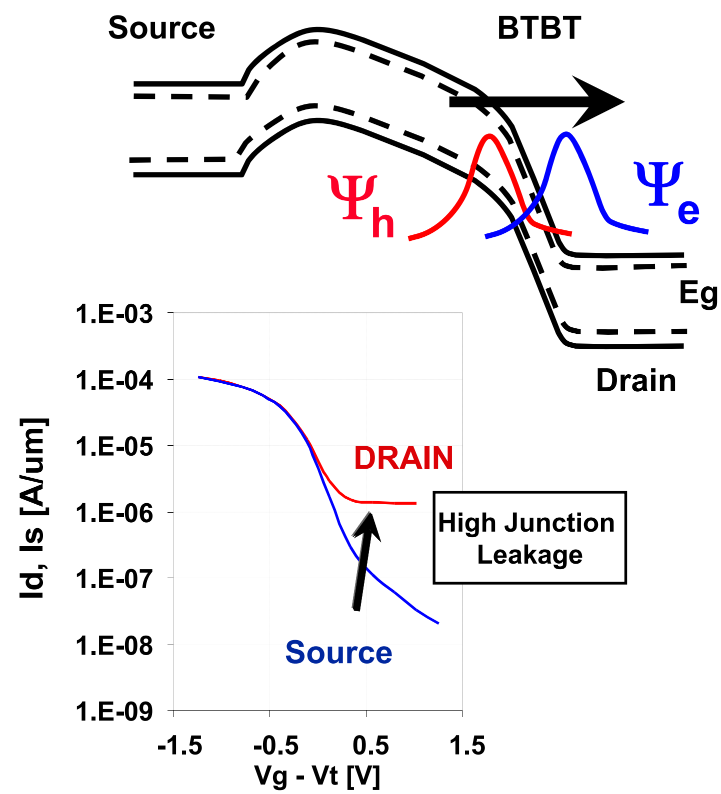


Poor Quality Dielectric

Narrow Bandgap

Adapted from Saraswat [59], Krishnamohan [60]

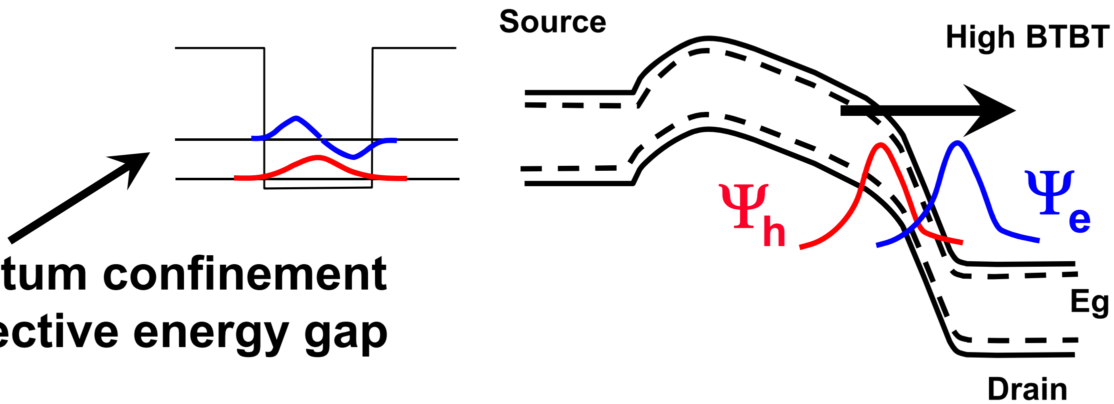




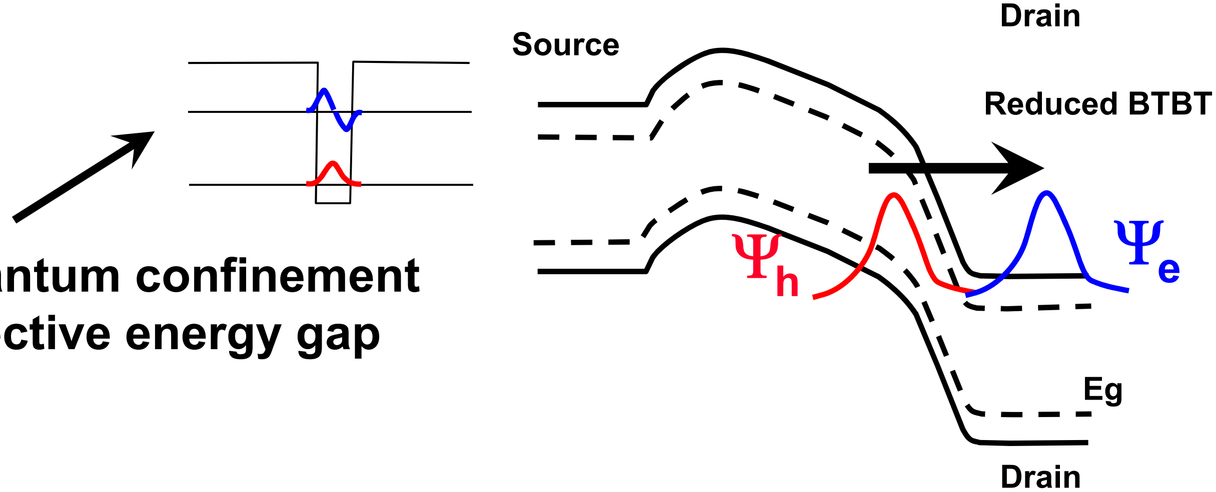
Band-to-band tunneling: challenge for low Eg materials

Narrow Bandgap

Adapted from Saraswat [59], Krishnamohan [60]



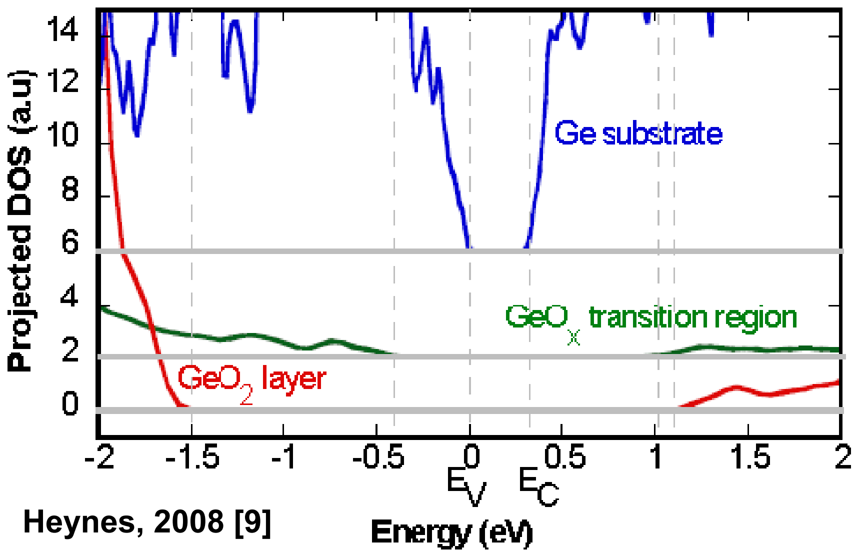
Weak quantum confinement
Narrow effective energy gap



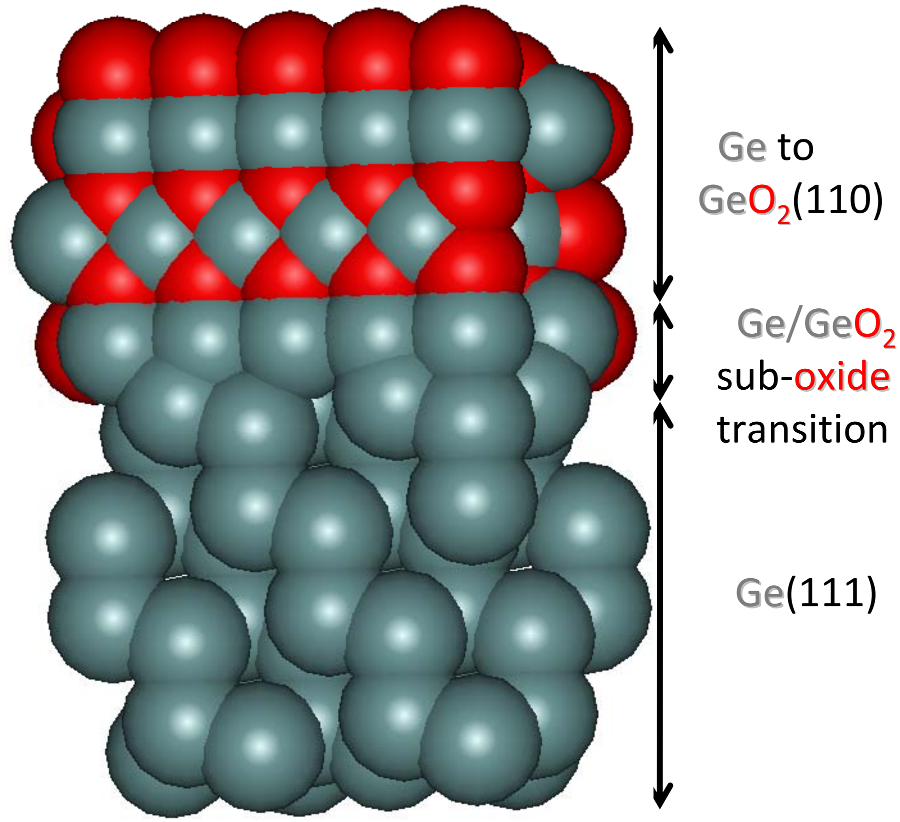
Strong quantum confinement
Wide effective energy gap

Two solutions: Use lower voltages and/or use quantum confined systems

Dielectric Quality



Heynes, 2008 [9]

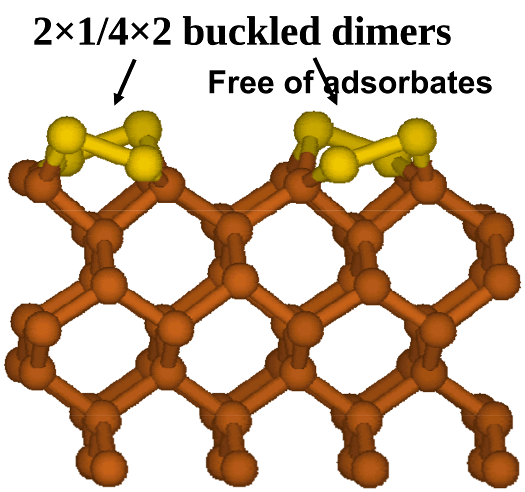


Since HiK-MG dielectrics typically form with a bilayer (the HiK + an interface layer) the challenge of germanium oxide still exists.

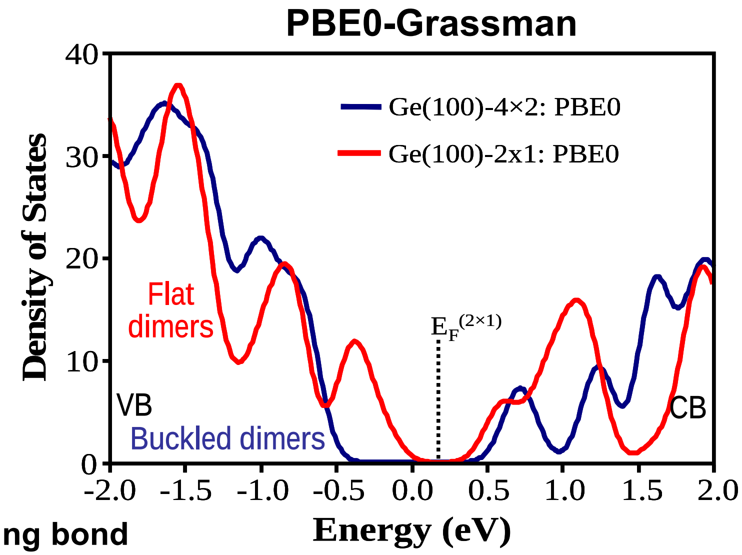
Germanium oxide exists in several morphologies, unfortunately, most are hydroscopic and/or volatile.

E. Chagarov, T. Grassman, A. Kummel (UCSD)

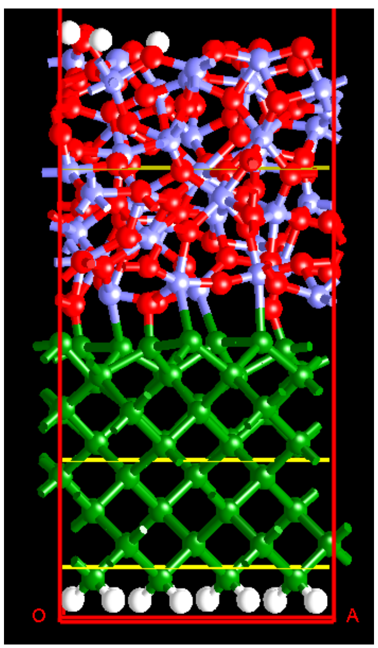
a-MO_2/Ge without and with Passivation (2010 Sematech)

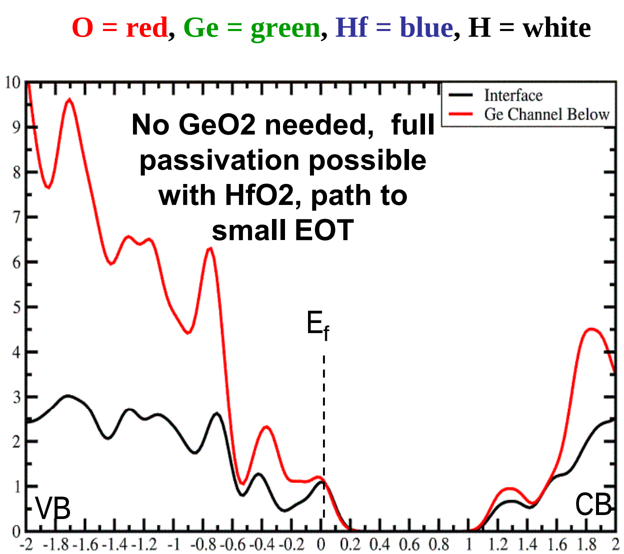


Each Ge atom has ½ filled dangling bond



- Although ideal Ge(100) is unpinned, flat dimers or undimerized Ge atoms can pin the Fermi level.
- As shown on the left the ideal surface has a bulk like bandgap due to tilted dimers which will be absent at oxide-Ge interfaces.
- Therefore, oxide must passivate ALL tricoodinated Ge surface atoms



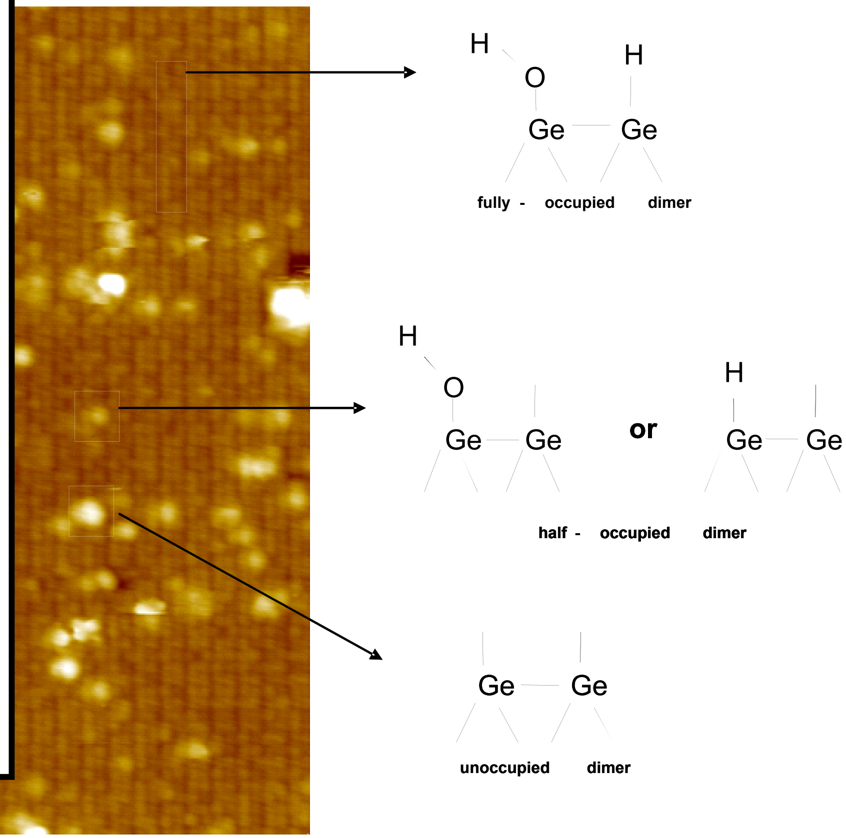


- Density function theory molecular dynamics (DFT-MD) was used to bond amorphous HfO_2 to Ge(100) and anneal at 700K. Interface has a mix of Ge-O and Ge-Hf bonds.
- Oxides passivate dangling bonds; 100% of interfacial Ge have 4 bonds. Interface is abrupt and Ge lattice is undisturbed.
- DOS shows a bandgap of 0.8 eV with no midgap states either in the interface or the channel. Fermi level shift from dipoles at oxide/vacuum interface being fixed.

Ge-J. Lee, T. Kaufman-Osborn, A. Kummel (UCSD)

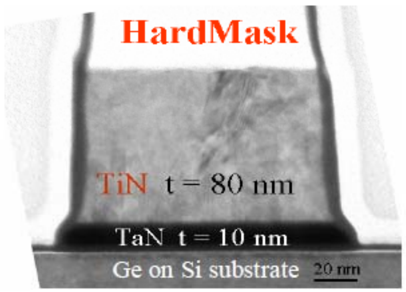
Monolayer Functionalization of Ge (2010 Sematech)

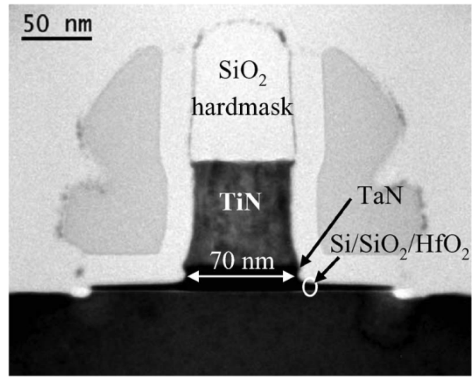
•The key requirement for scaling oxides on Ge while maintaining high mobility is functionalizing the Ge(100) with a monolayer of reactive sites.
•This is challenging as even the most stable germanium oxides react with the substrate to form volatile suboxide.
•The Kummel group at UCSD has used STM to show that very large doses of water onto clean 300K Ge(100) can functionalize 99% of the unit cells with Ge-H and Ge-OH bonds.
•These bonds are sufficiently reactive with TMA (trimethyl aluminum) that the ALD process can be initiated at 300K for the first layer.
•Key message: A 300K process has been developed to template the ALD processes in nearly every unit cell for EOT scaling without disrupting the substrate lattice.



- Ge-OH and Ge-H sites cover Ge(100) surface (rectangle) with >10^6L dose of H_2O at 300K
- Fuzzy bright features are unreacted dangling bonds (squares). Can passivate with H or annealing
- ½ ML of Ge-OH perfect template for nucleation of TMA for scaled ALD gate oxide (even HfO_2)
- XPS studies show this surface reacts at 300K with TMA to form ½ ML of Ge-O-Al bonds which are stable up to 450C thereby functionalizing the surface for ALD of high-k.

Ge Dielectric:
Another strategy: use an Si passivation layer





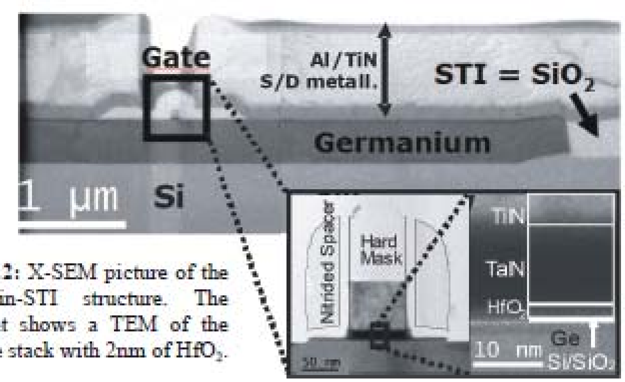
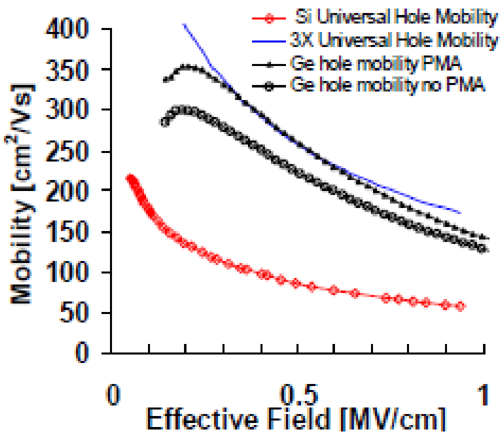
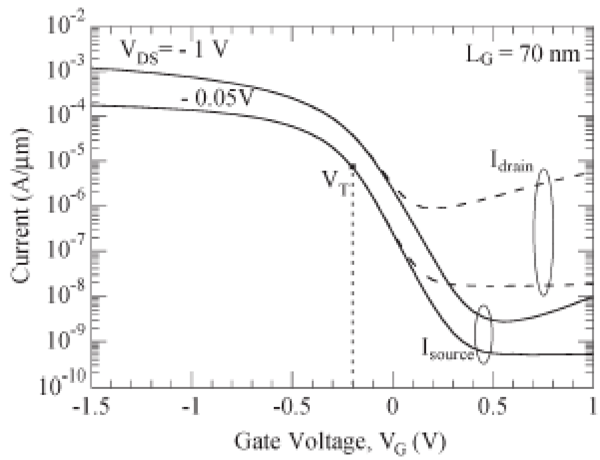
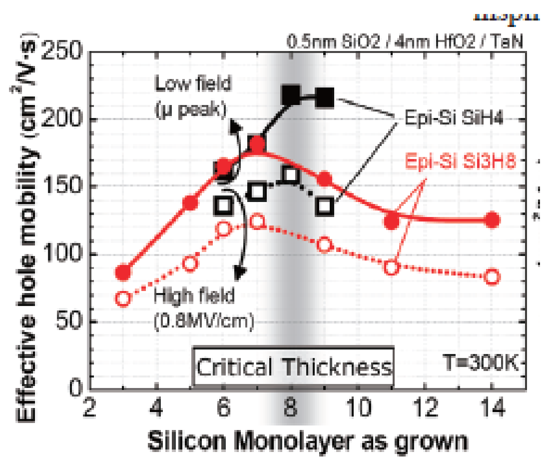


Fig.2: X-SEM picture of the Ge-in-STI structure. The inset shows a TEM of the gate stack with 2nm of HfO_2.





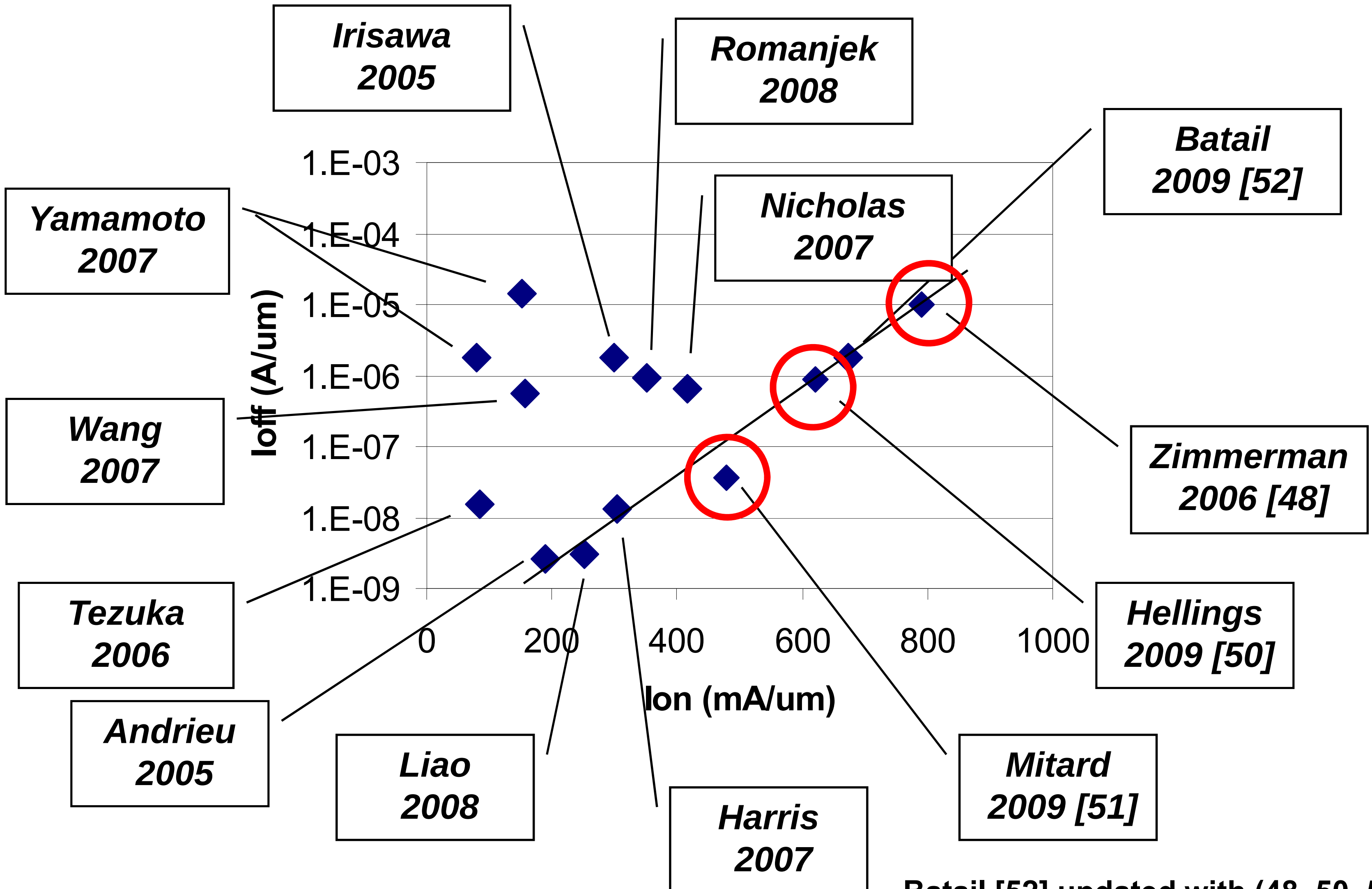


Zimmerman – Intel/IMEC
IEDM 2006 [48]
Si passivation

Hellings – IMEC/Leuven
EDL 2009 [50]
Si passivation

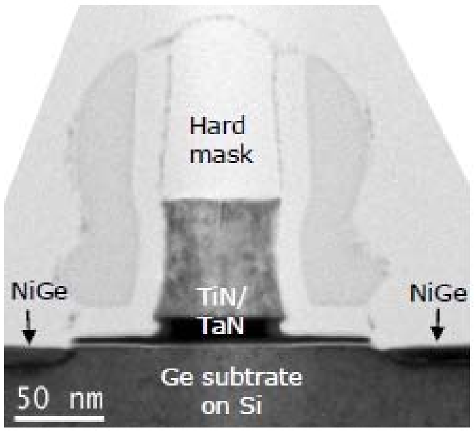
Mitard – IMEC/Leuven
VLSI 2009 [51]
Si passivation

Ge Benchmarking

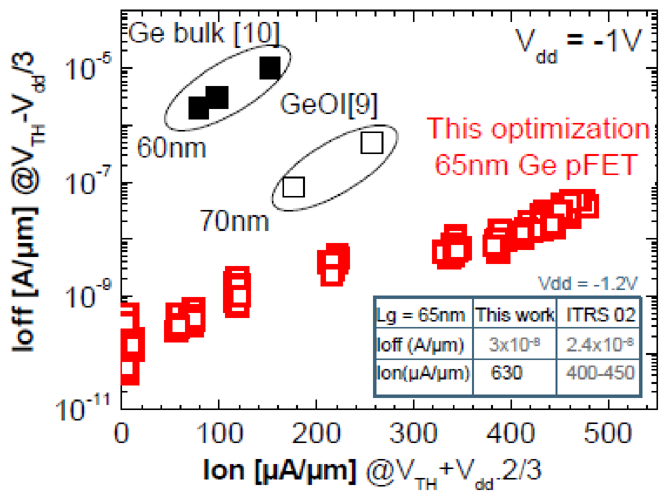


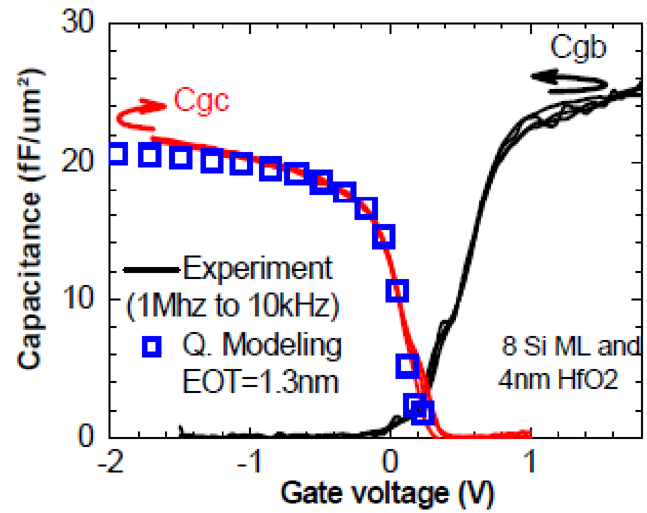
Batail [52] updated with (48, 50, 51, 52)

Mitard, IMEC/Leuven, IEDM 2008

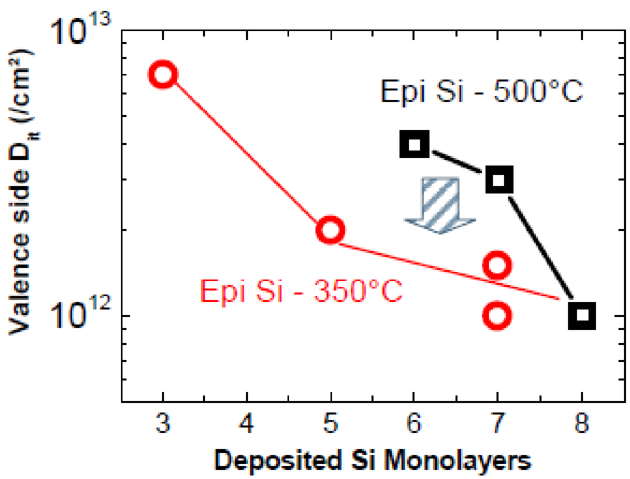


Ultra-thin Si cap + 4nm HfO2

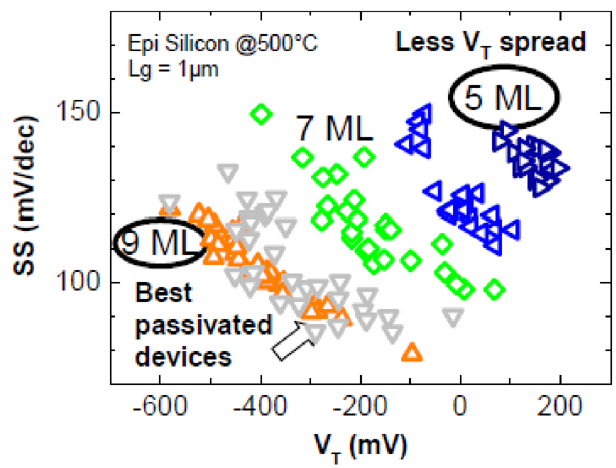


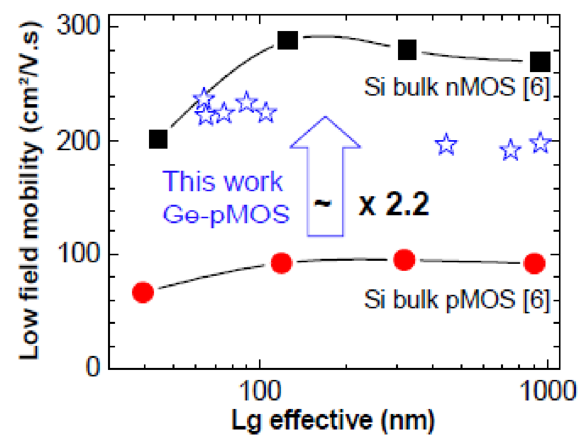


Inversion EOT 13A



Dit integrated over valence band





Mitard, IMEC/Leuven, VLSI 2009

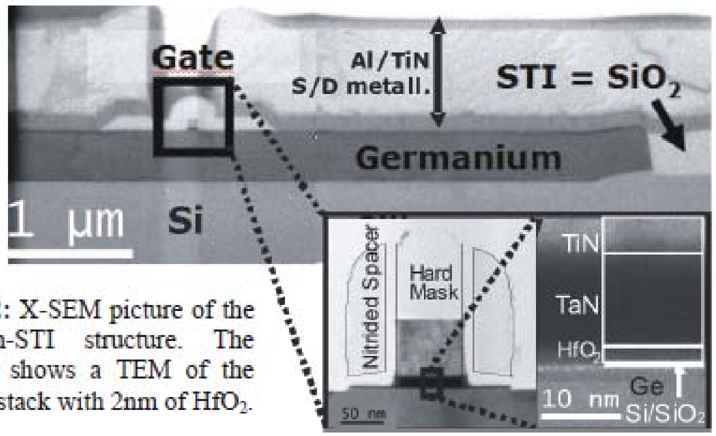


Fig.2: X-SEM picture of the Ge-in-STI structure. The inset shows a TEM of the gate stack with 2nm of HfO_2.

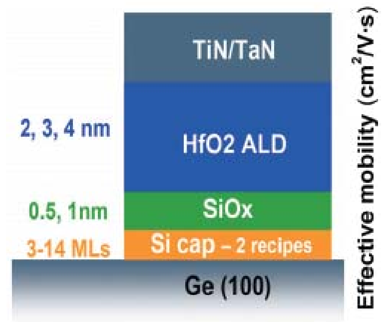
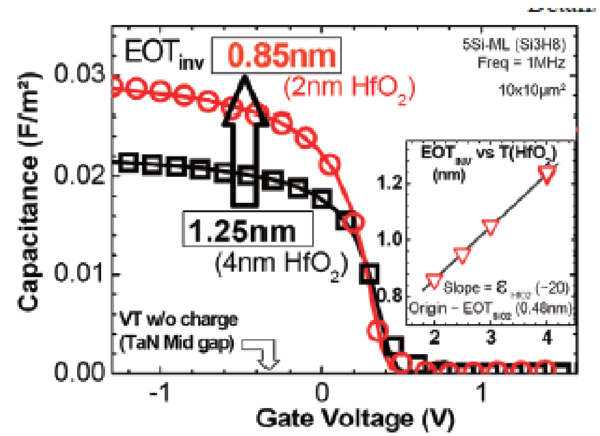
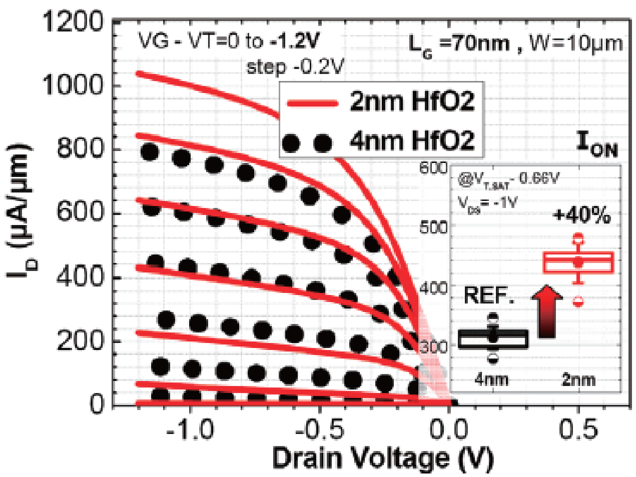
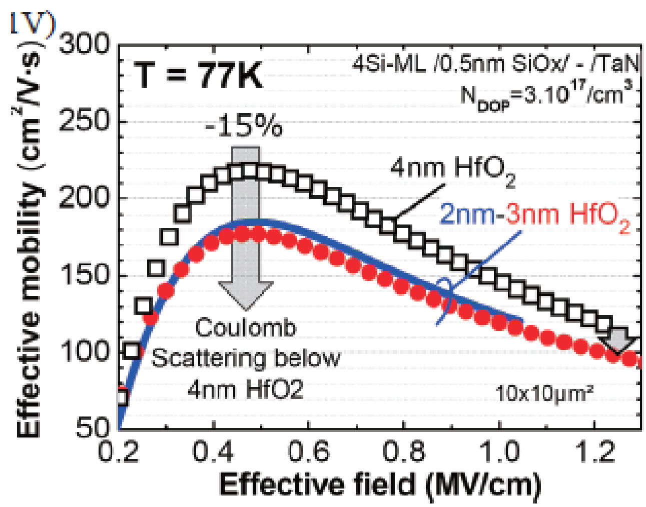


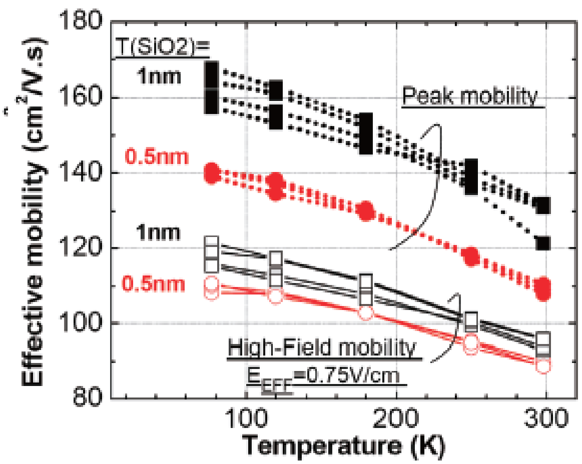
Fig.6: Schematic view of the various High-K/Metal gate stacks studied here. EOT_{INV}: 0.85-1.62nm







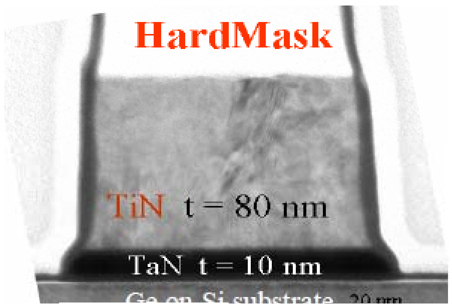
Higher Coulomb scattering
For 2 or 3nm HfO2

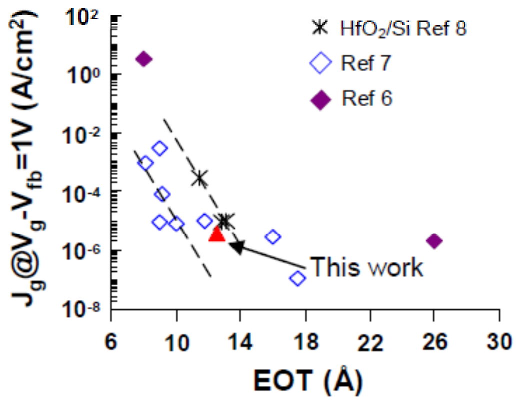


Higher Coulomb scattering
For thinner TL SiO2

Zimmerman, IMEC/Intel, IEDM 2006

6A epi-Si, partially oxidized after growth+4nm HfO2





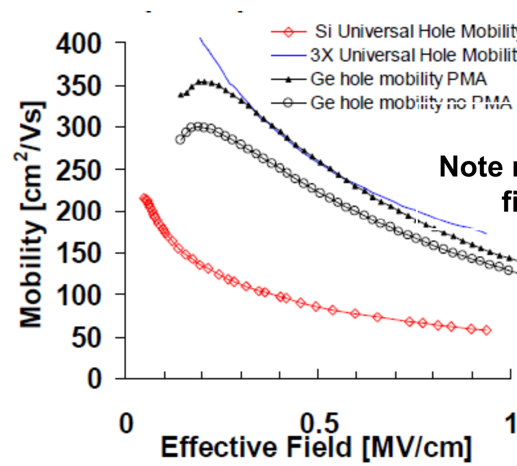
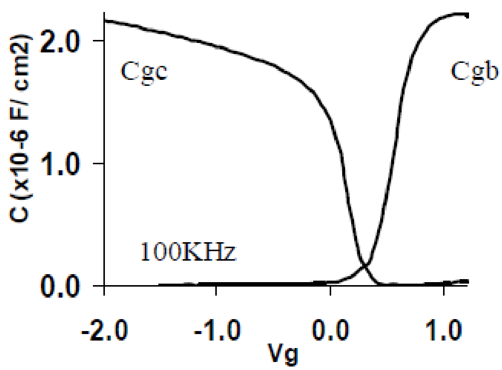


Fig. 4 Hole mobility vs. effective field for a 10μm x 10μm pMOS as in Fig. 2 and 3, with and without a PMA. The mobility enhancement is maintained for large fields.

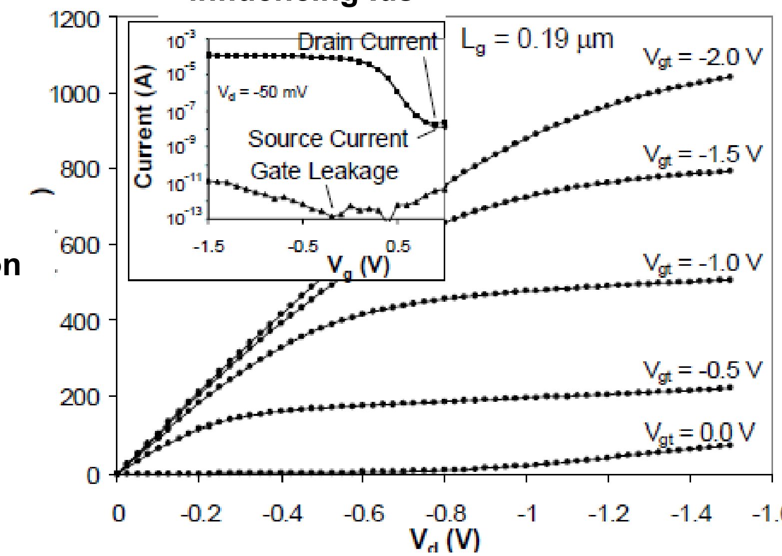
10x10um Note respectable high field mobility

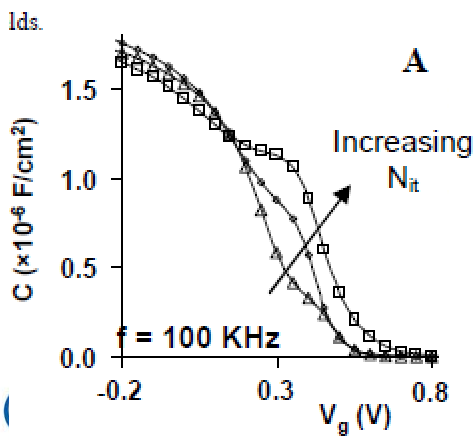


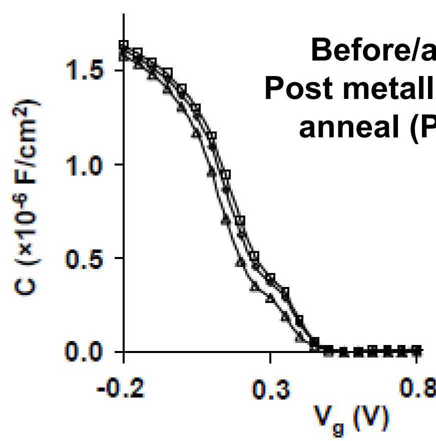
CET = 16A, EOT = 12/12.5A

10x10um structure

Jg not influencing Ids

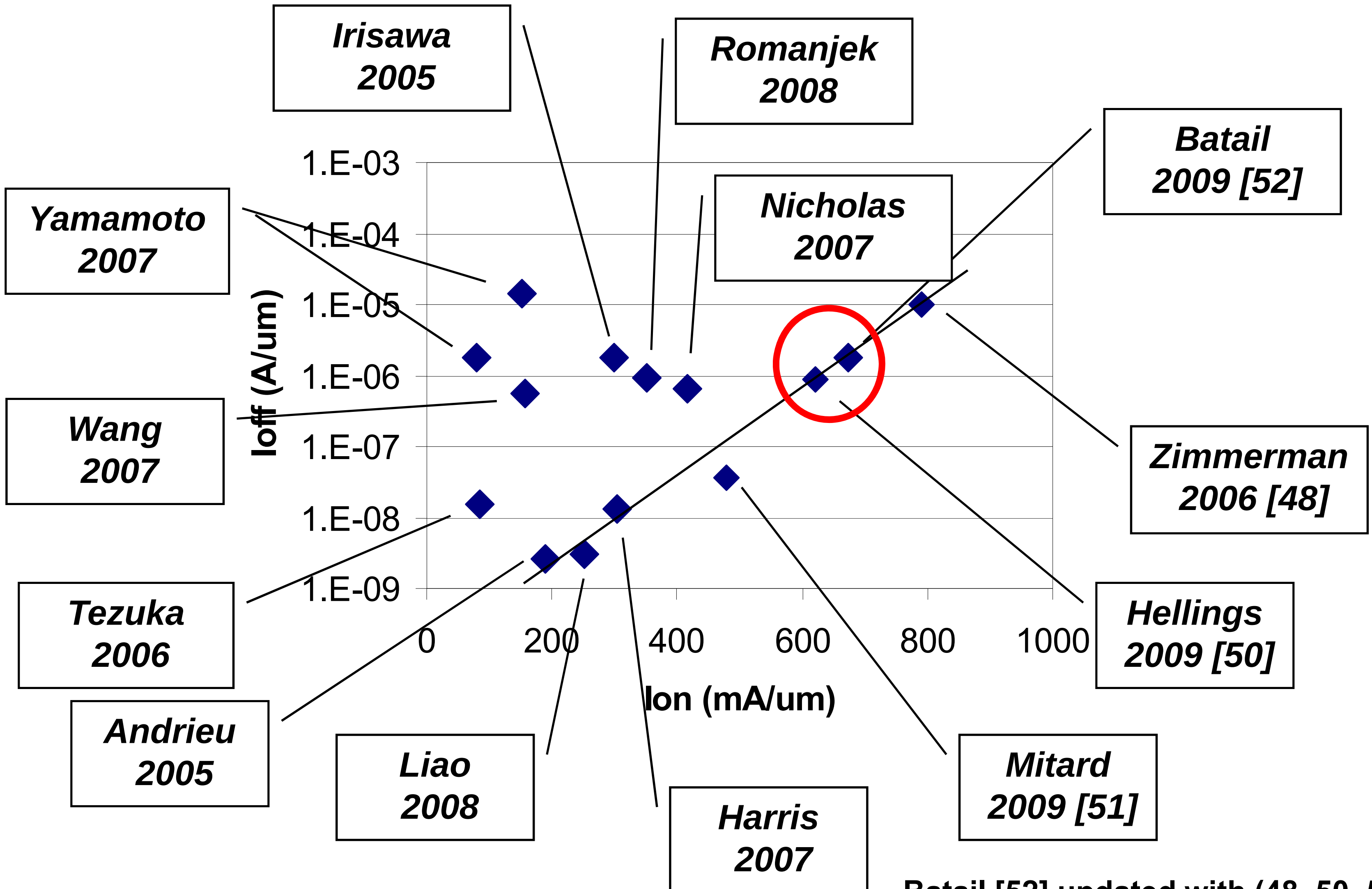






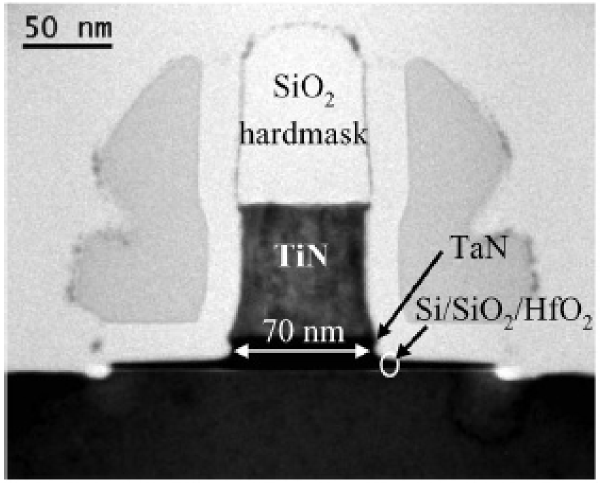
Before/after Post metallization anneal (PMA)

Ge Benchmarking



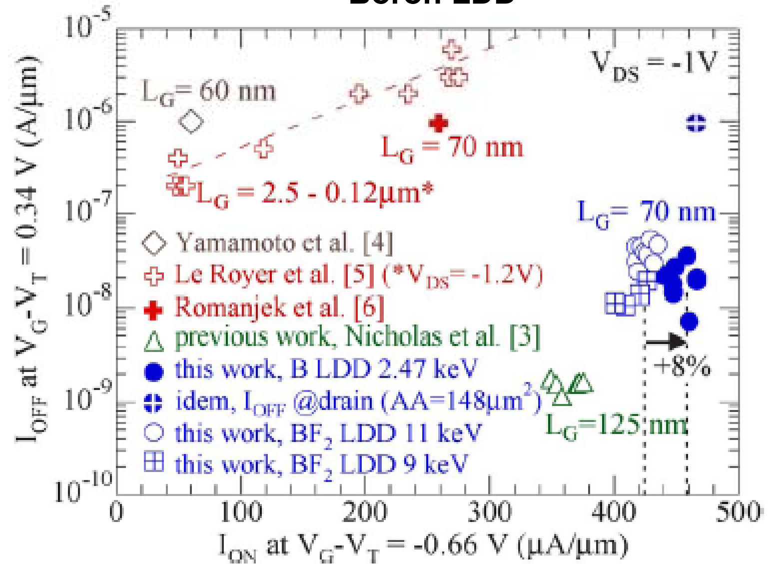
Batail [52] updated with (48, 50, 51, 52)

Hellings – IMEC/Leuven, EDL 2009

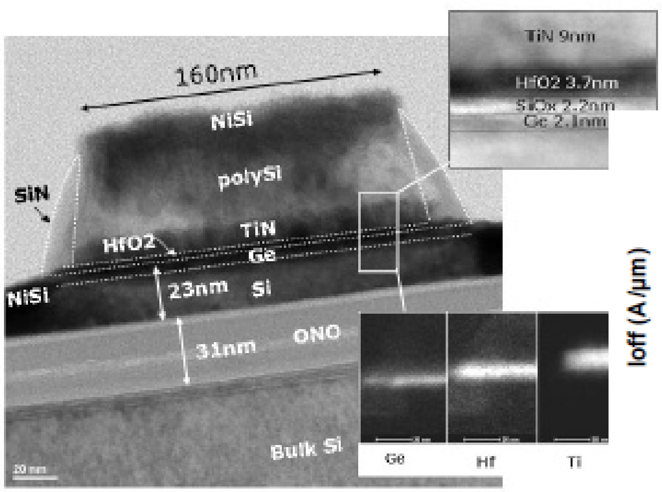


Ultra-thin Si cap + 4nm HfO2

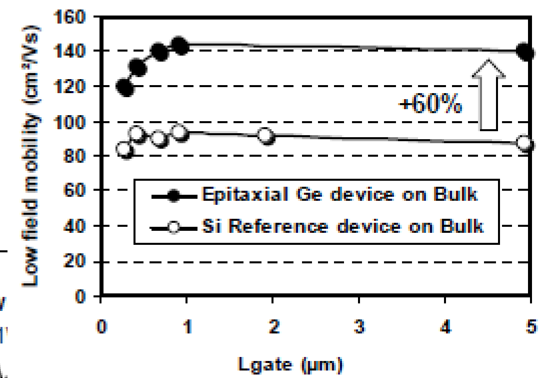
Boron LDD

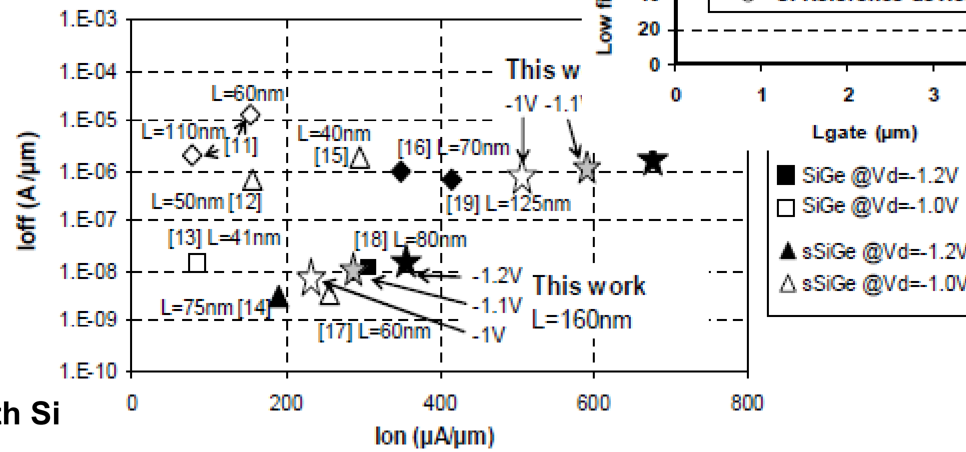


Batail – ST-Micro, IEDM 2008



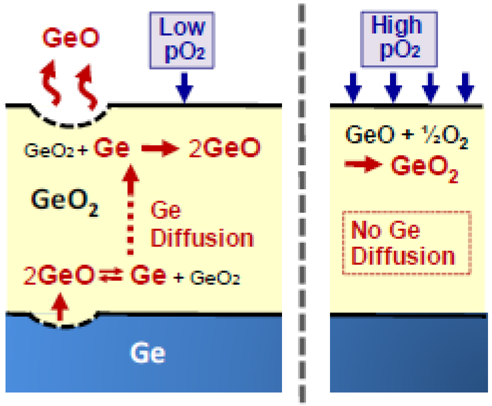
Selective epitaxy of pure Ge capped with Si





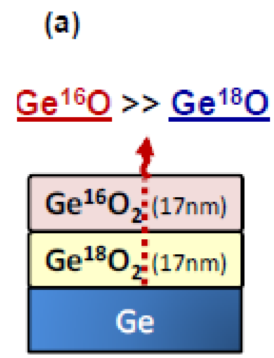
Kita (U. Tokyo) IEDM 2009

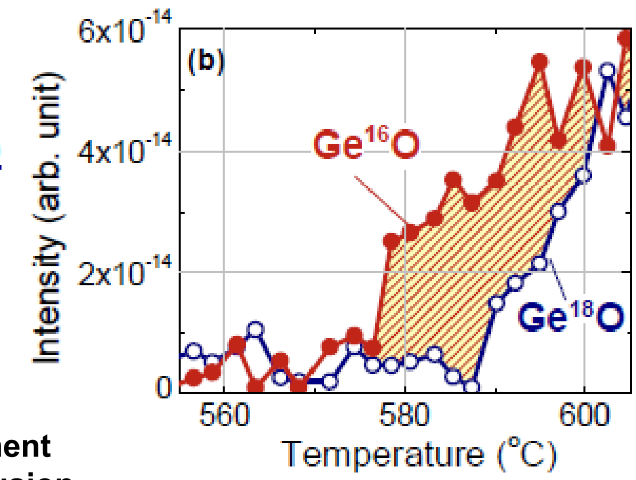
Another strategy: Advanced GeO_2 processing



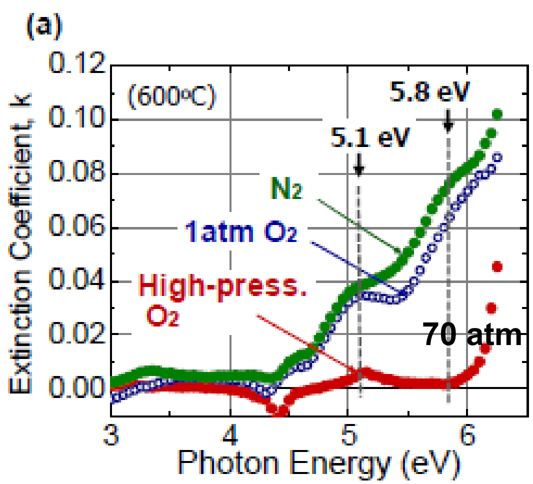
Ge diffusion

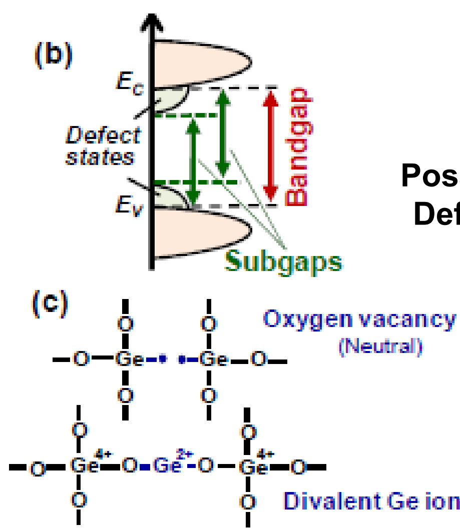
High-pressure O2 (HPO) suppresses surface reaction



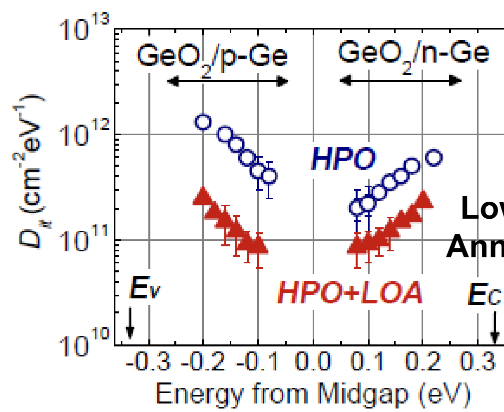


Isotope experiment Suggests Ge diffusion





Possible Defects

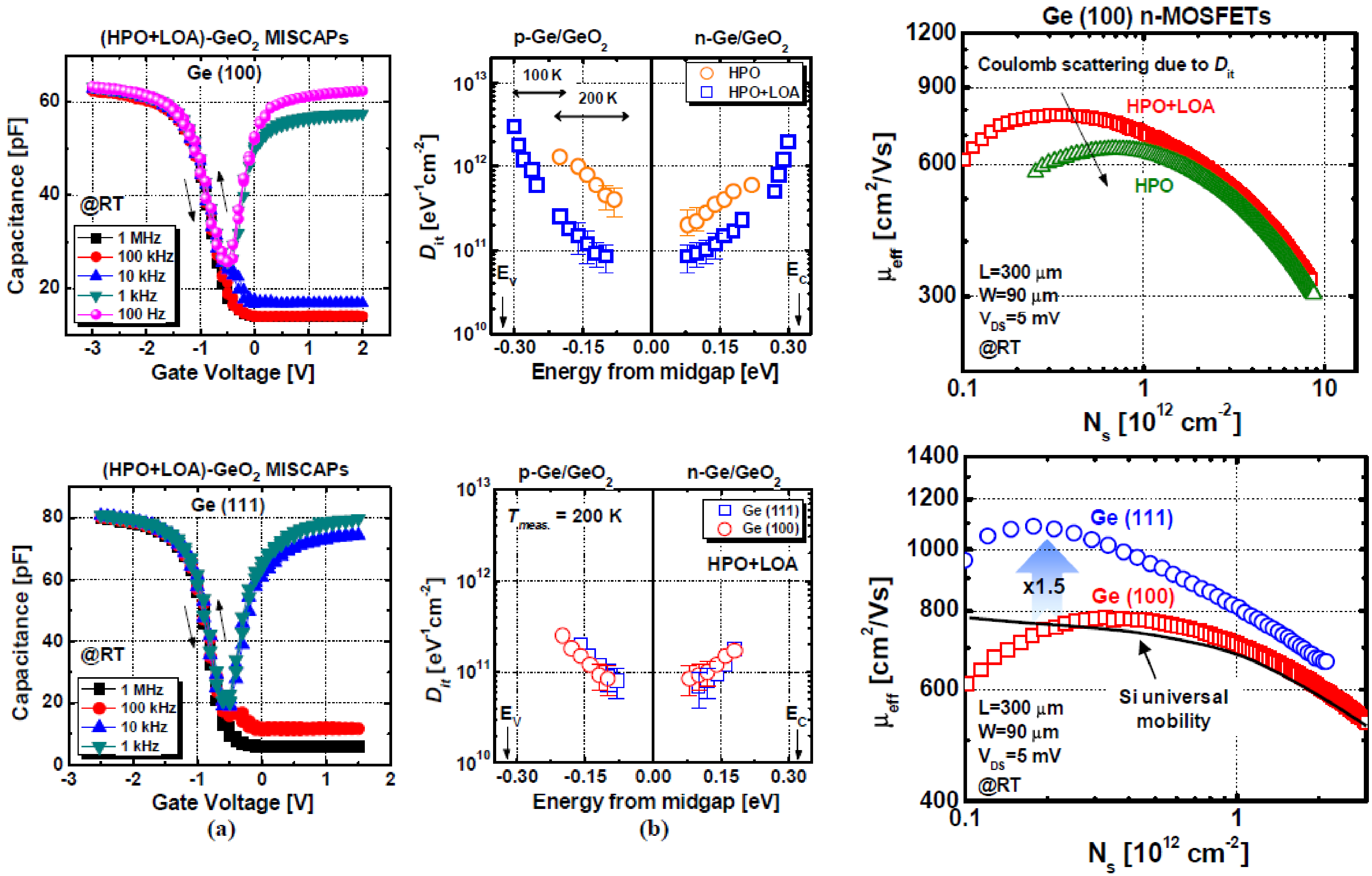


Low-T oxygen Annealing (LOA)

Fig. 10. Interface states density (D_{it}) of GeO_2/Ge interface fabricated by high-pressure O_2 oxidation (HPO), evaluated by conductance method at 200 K. D_{it} is further improved by the employment of low-temperature oxygen annealing (LOA) at 400°C, in 1atm O_2 for 30 min after HPO. The HPO + LOA process results in the mid-gap D_{it} less than 10^{11} $cm^{-2}eV^{-1}$.

Lee (U. Tokyo) IEDM 2009

High pressure O_2 (HPO) + Low-Temperature Oxygen Anneal (LOA)

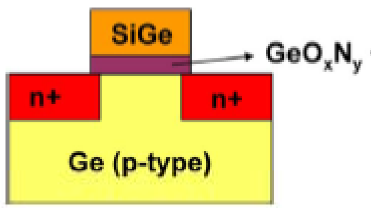


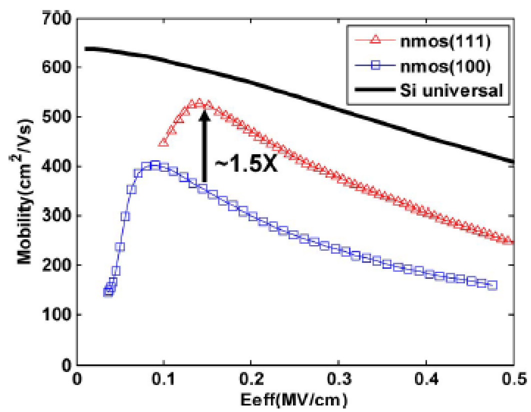
Kuzum (Stanford) IEDM/TED 2009

GeOxNy + Low-Temperature Oxygen Anneal (LOA)

TABLE I
Si-CMOS-LIKE PROCESS FLOW

1.	Pre-diffusion clean for Ge
2.	GeON growth & LPCVD SiO_2 for isolation
3.	Active area lithography & oxide etch
4.	GeON growth & LPCVD SiO_2 for gate stack
5.	Poly SiGe deposition
6.	Gate lithography & etch
7.	Source/Drain Implant
8.	Dopant activation anneal
9.	Backend dielectric
10.	Ti/Al contact pads
11.	FGA anneal





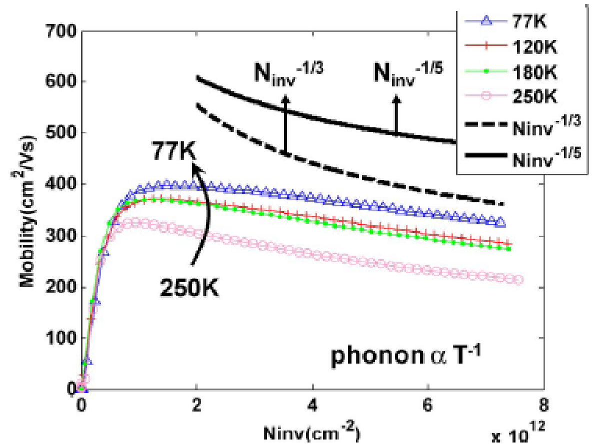
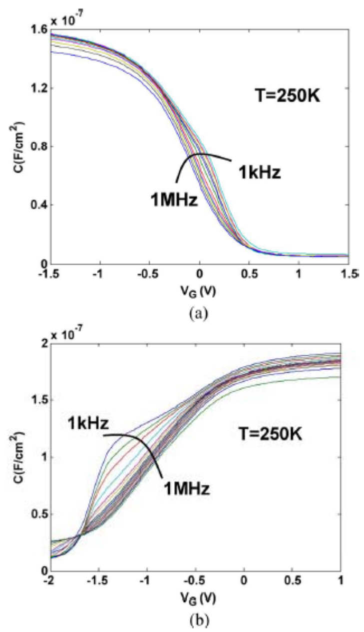


Fig. 11. Effective hole mobility versus inversion charge density is plotted in the 77 K–250 K temperature range for the (100) substrate. $N_{\mathrm{inv}}^{-1/3}$ and $N_{\mathrm{inv}}^{-1/5}$ dependences are plotted as references. $\mu_p \alpha T^{-1}$ also indicates the effect of phonon scattering.



g. 2. (a) CV characteristics for the p-substrate correspond to the lower half the bandgap, which is closer to the valence-band edge. (b) CV characteristics r the n-substrate correspond to the upper half of the bandgap, which is closer the conduction-band edge. Frequency dispersion (kink at low frequencies in e depletion region) is consistent with D_{it} results [Fig. 3].

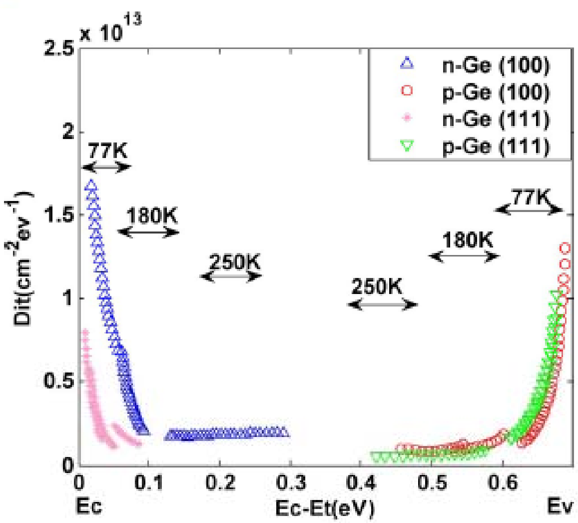


Fig. 3. D_{it} versus trap energy (E_t) in the Ge bandgap for MOSFETs fabricated on the (100) and (111) substrates for the 77 K–250 K temperature range. D_{it} is extracted for the same devices used in mobility characterization. An n-substrate (PMOS) is used for the upper half of the bandgap, while a p-substrate (NMOS) is used for the lower half. The entire bandgap is covered with measurements done at 77 K, 180 K, and 250 K.

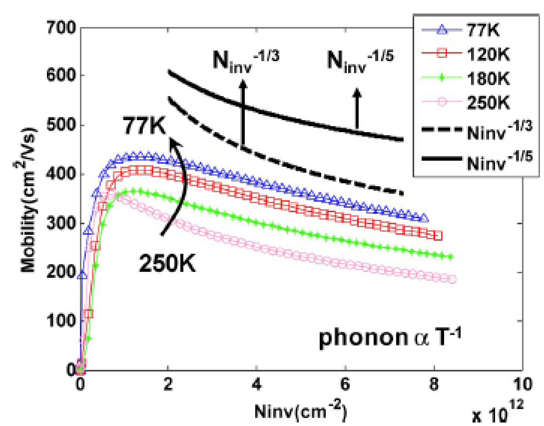


Fig. 13. Effective hole mobility versus inversion charge density is plotted in the 77 K–250 K temperature range for the (111) substrate. Mobility values and temperature and inversion charge density dependences look quite similar to the (100) case, which also indicates that phonon scattering is the dominant mechanism.

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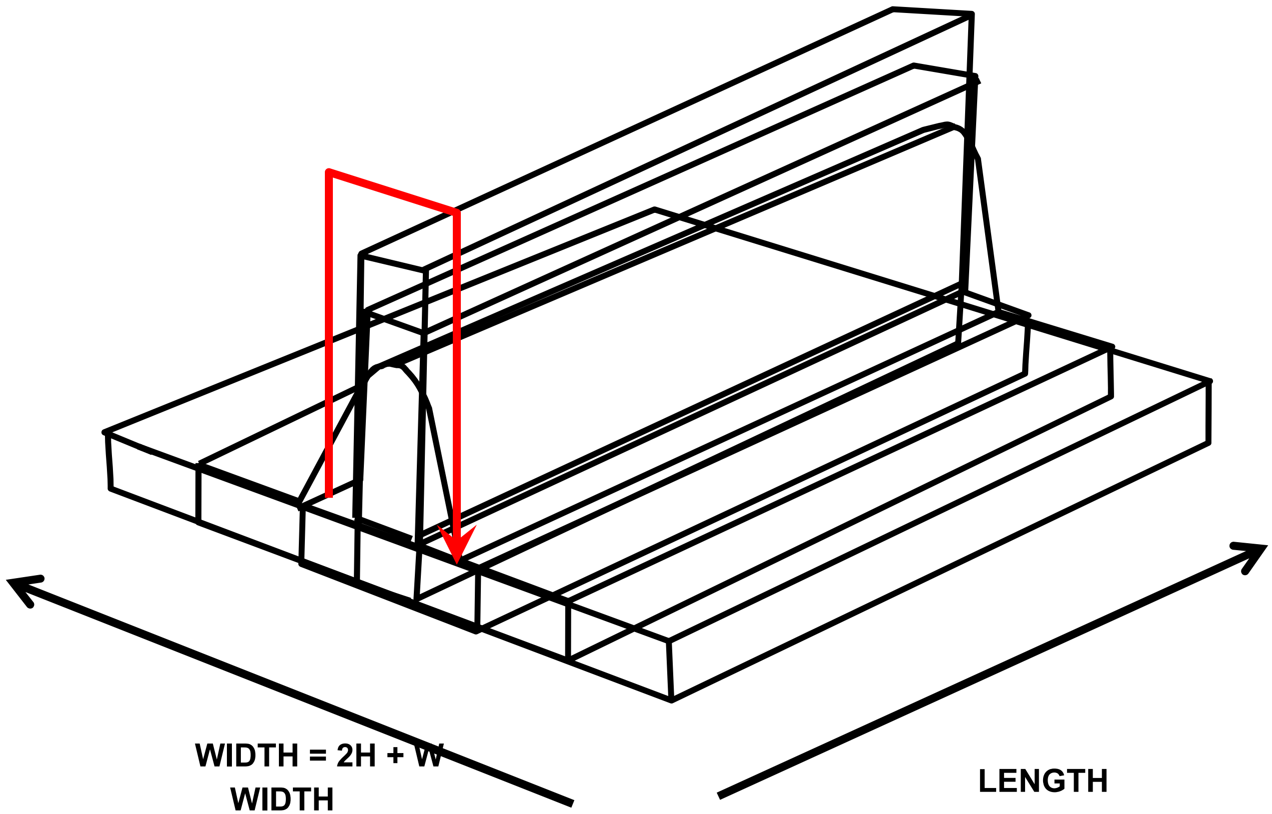
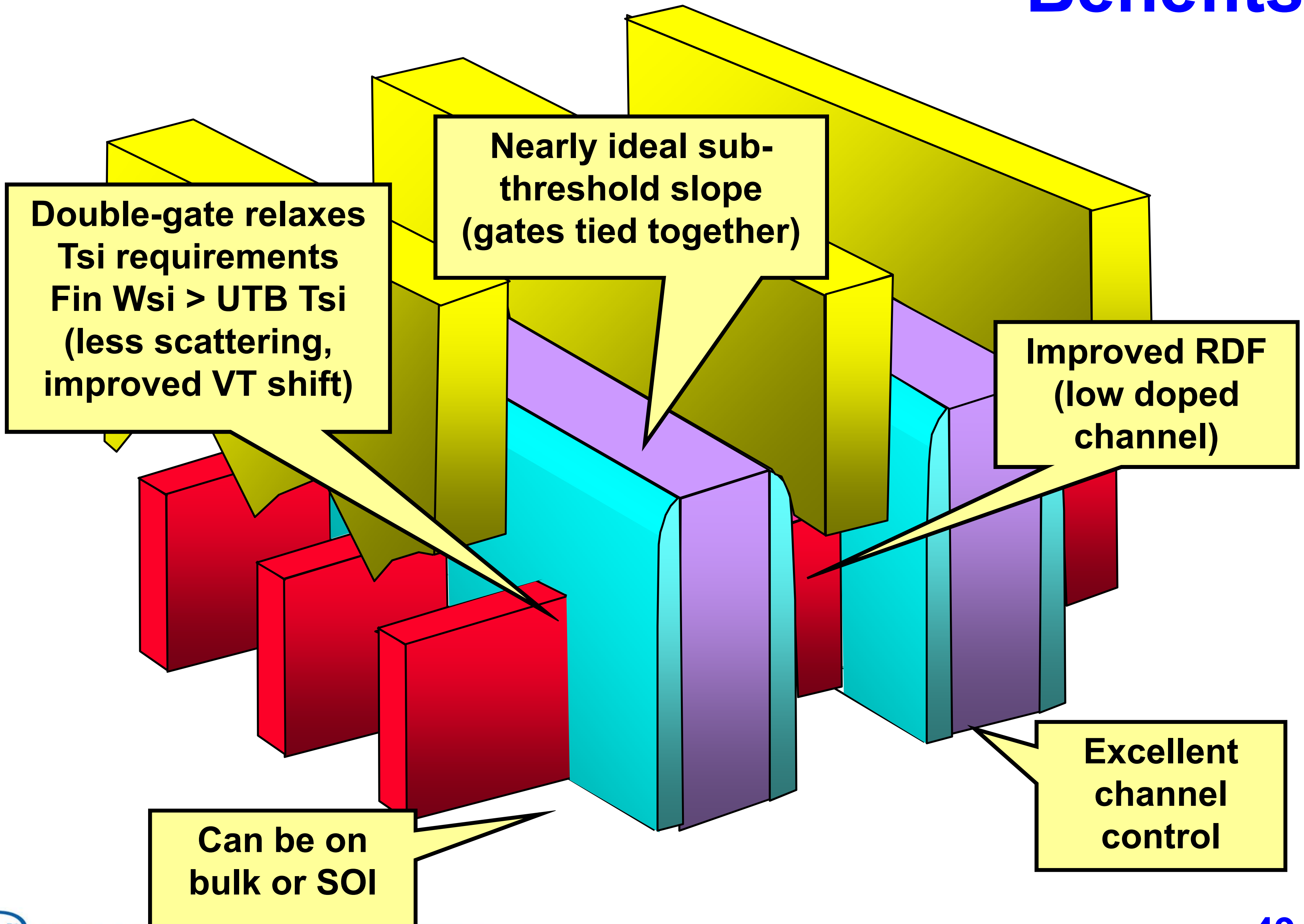


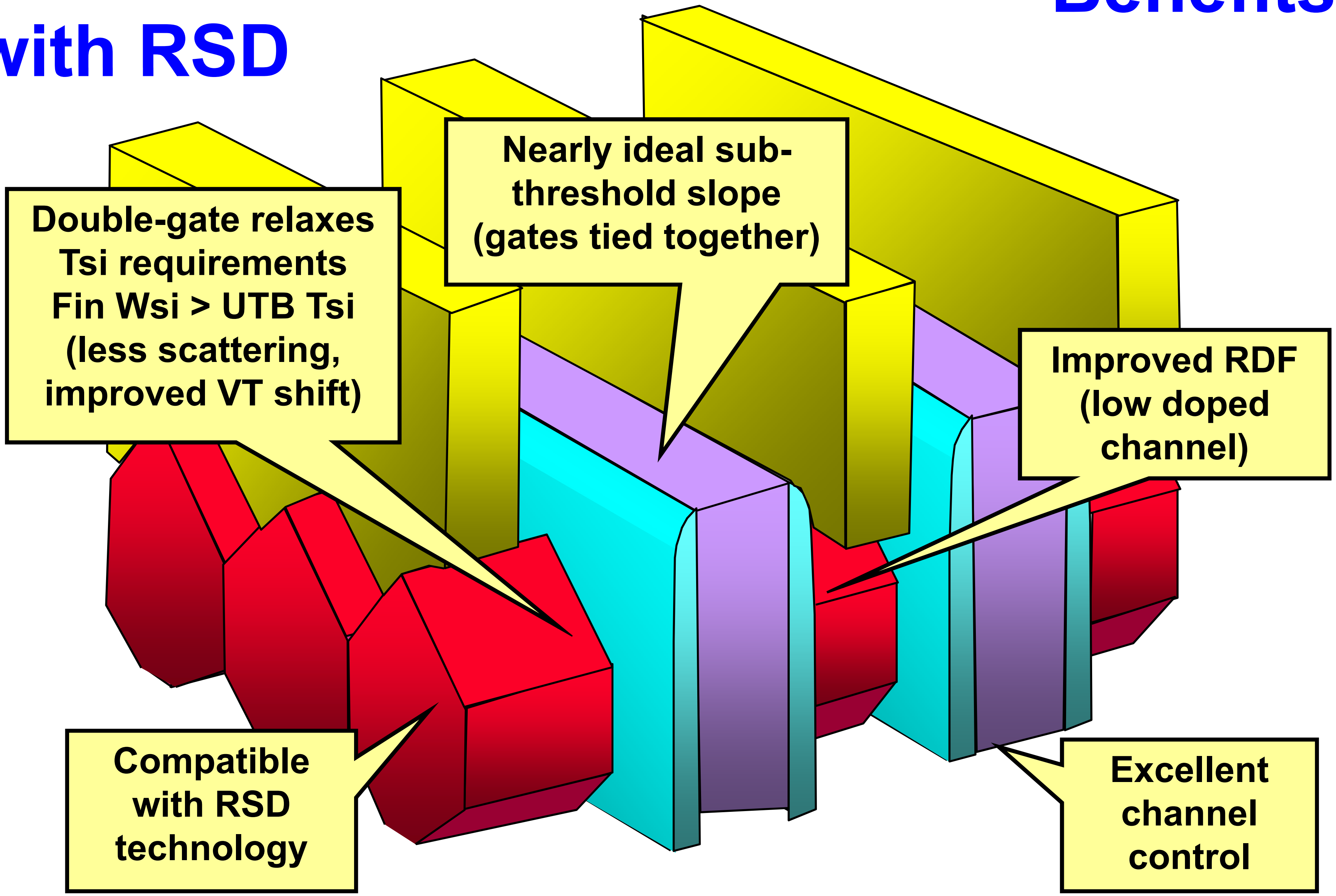
Non-planar architectures

MuGFET Benefits

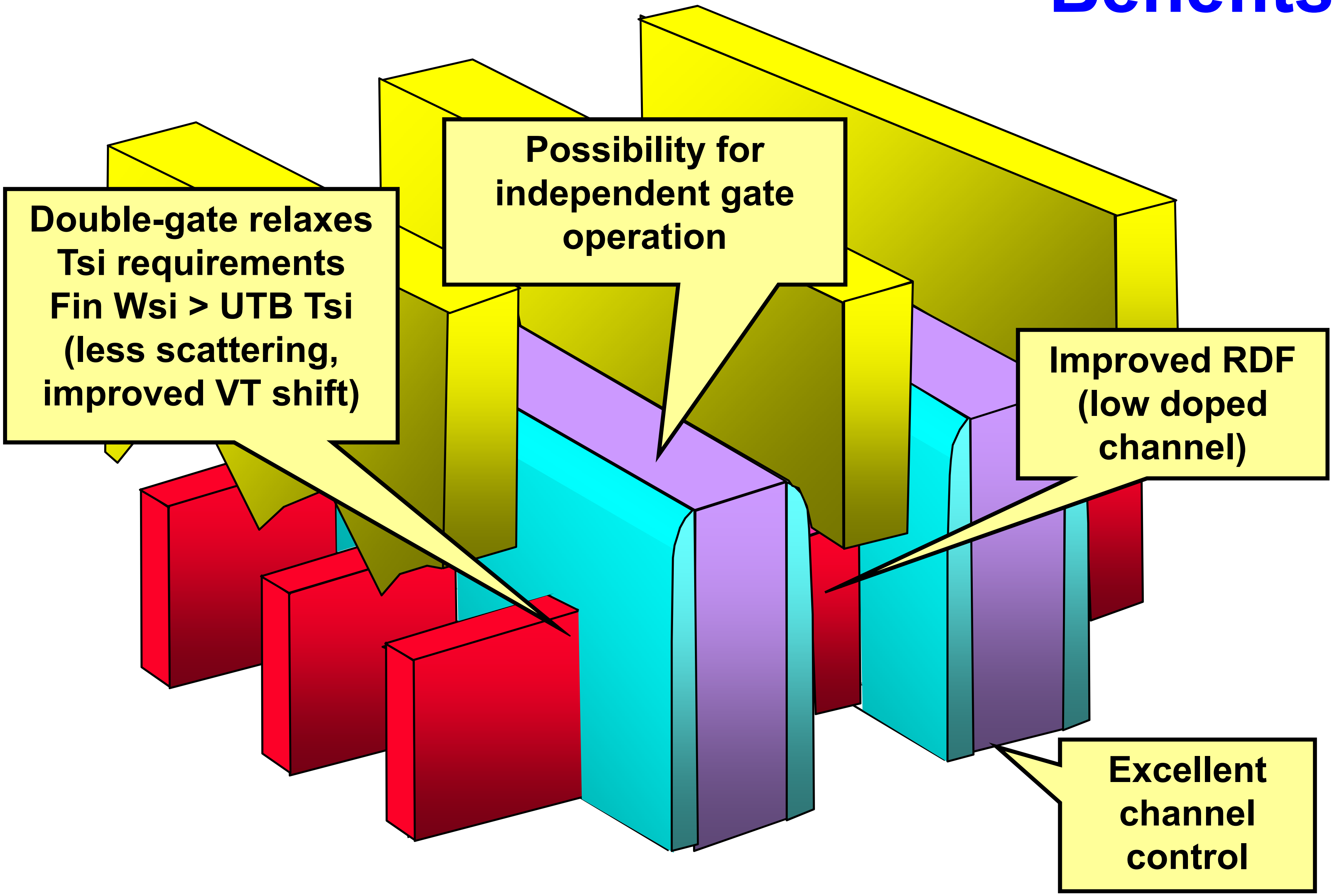


MuGFET with RSD

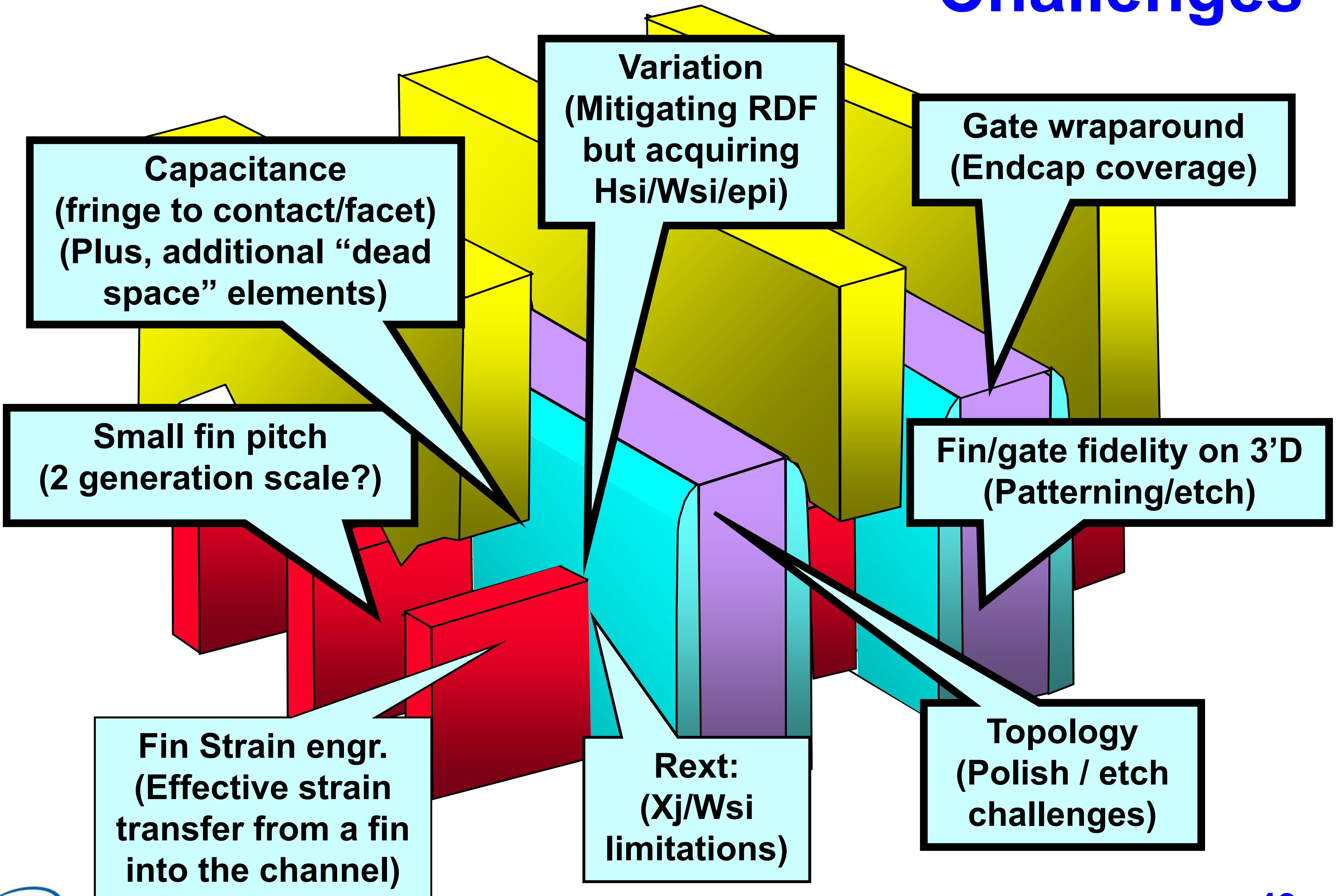
Benefits



MuGFET Benefits

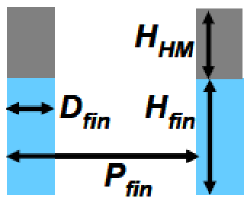


MuGFET Challenges

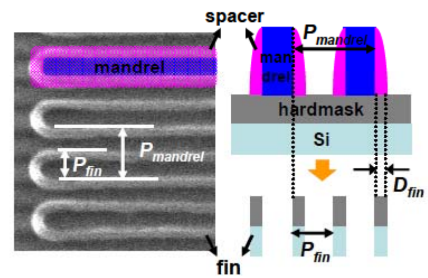


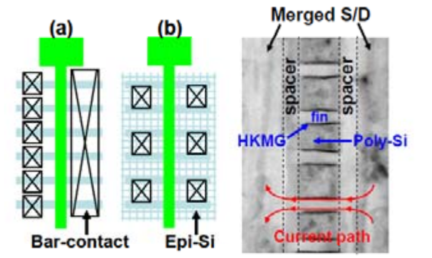
Kawasaki – Toshiba / IBM – IEDM 2009

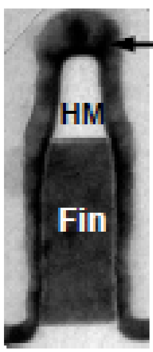
MuGFET



Year of production	2015	2018	2021
node (nm)	22	16	11
P_{fin} (nm)	40	28	21
D_{fin} (nm)	12	8	6
H_{fin} (nm)	28	20	15
SRAM cell size (μm^2)	0.063	0.03	0.015
L_g at cell (nm)	24	16	12

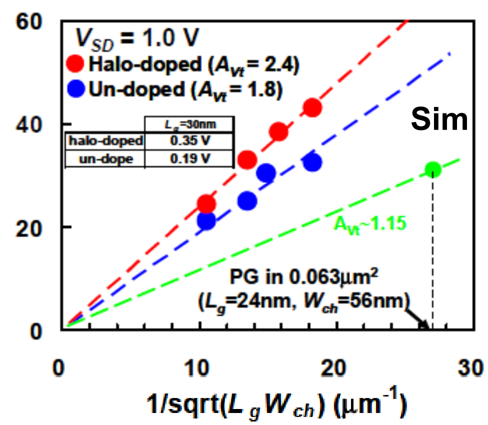


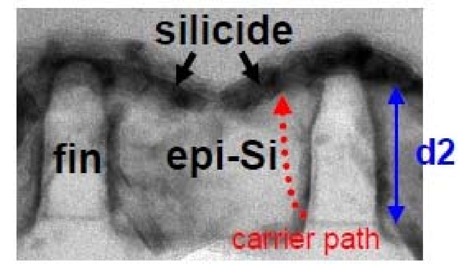




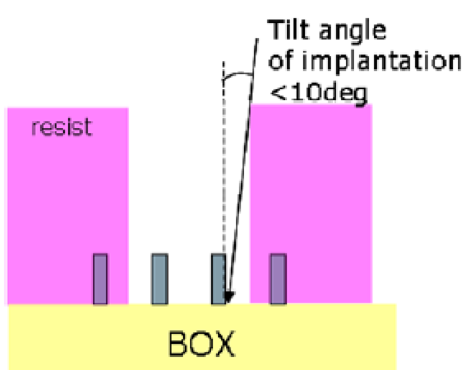
The thickness of HKMG should be uniform along fin height.

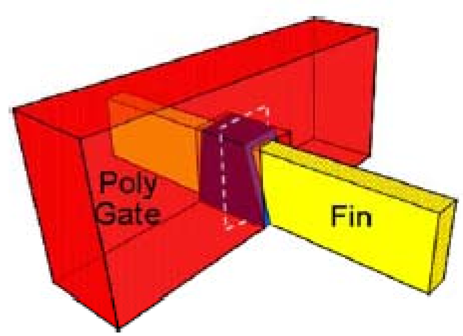
source of σV_t	origin
T_{ox} variation	non-uniform thickness of HK
ε_{ox} variation	non-uniform composition of HK
WF avriation	non-uniformity of MG
	grain size variation
	multi-surface oritations
charges	traps and states

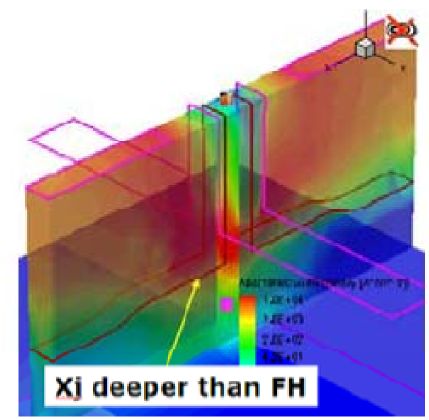




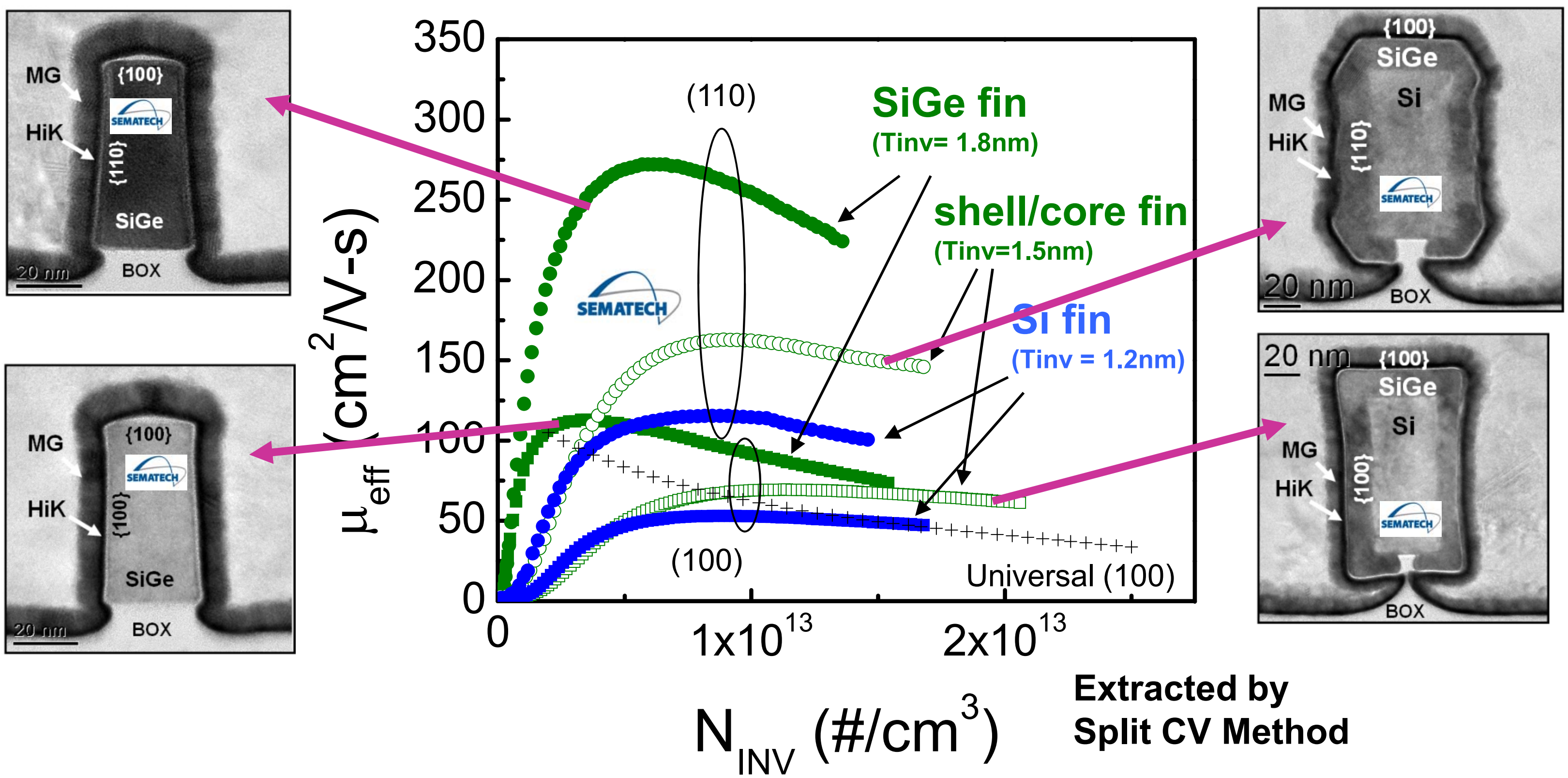
Jurczak – IMEC - SOI 2009







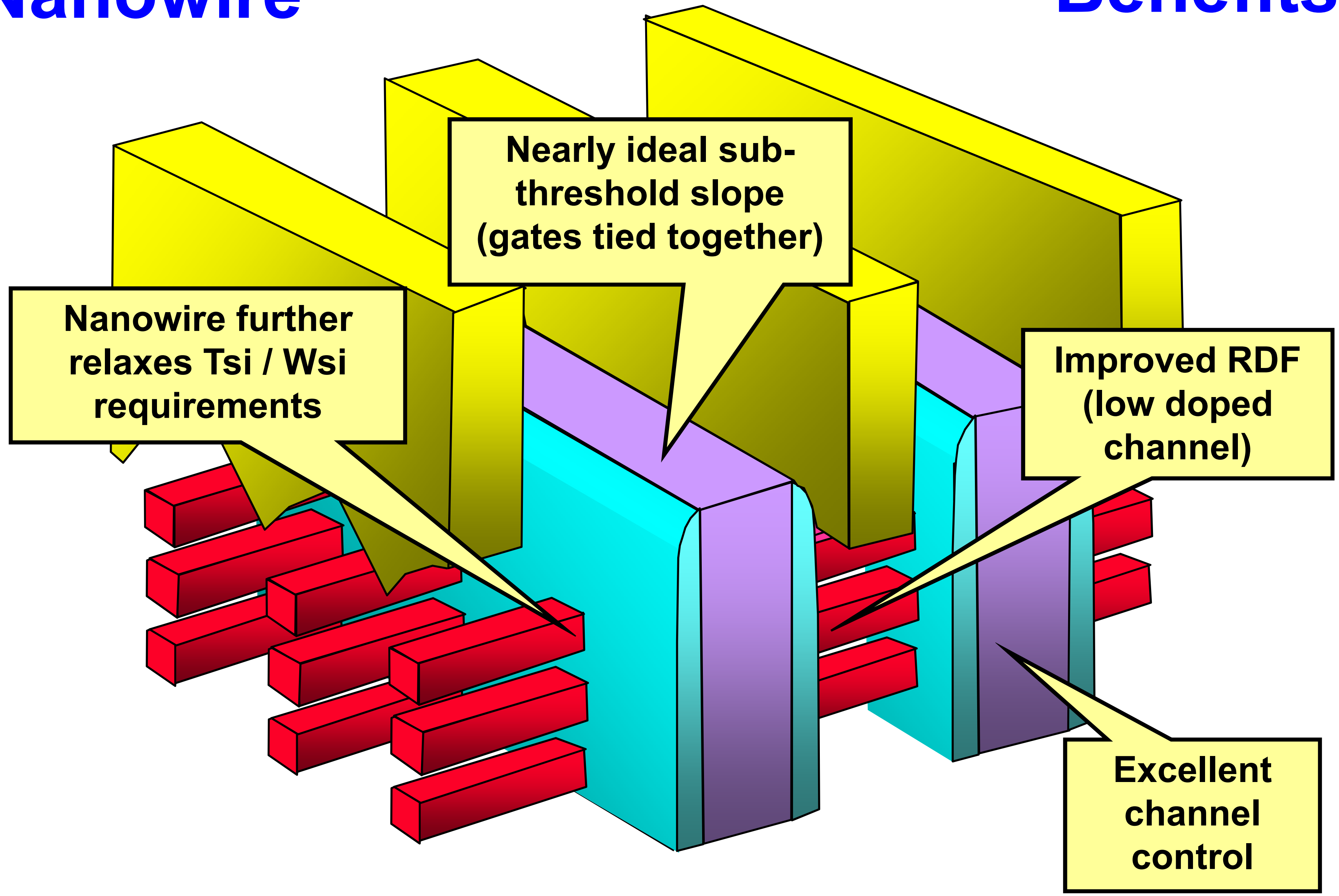
High Mobility SiGe FinFETs



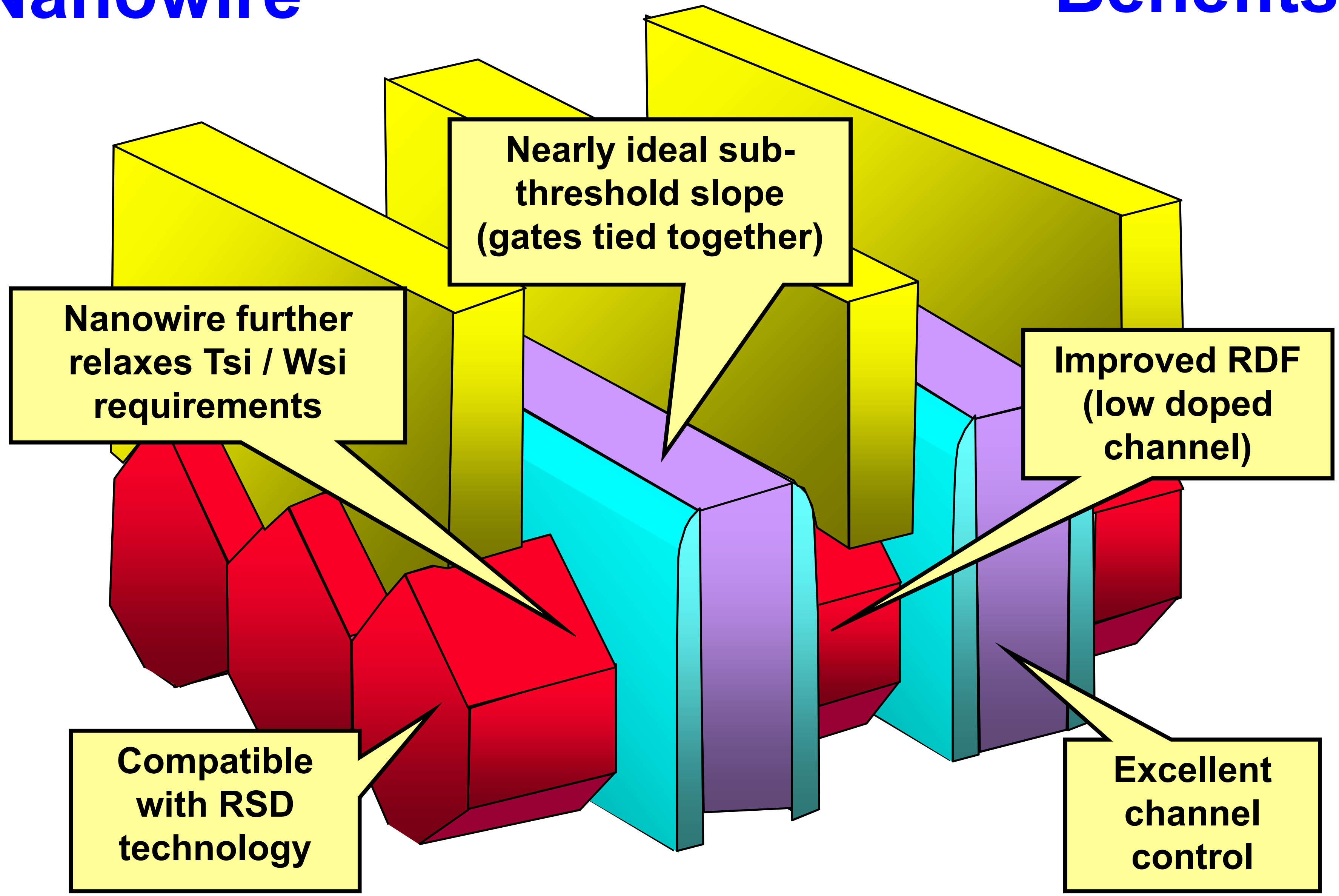
Extracted by Split CV Method

- SiGe PFETs have higher mobility than Si fins.
- Potential for performance > strained Si in non-planar devices

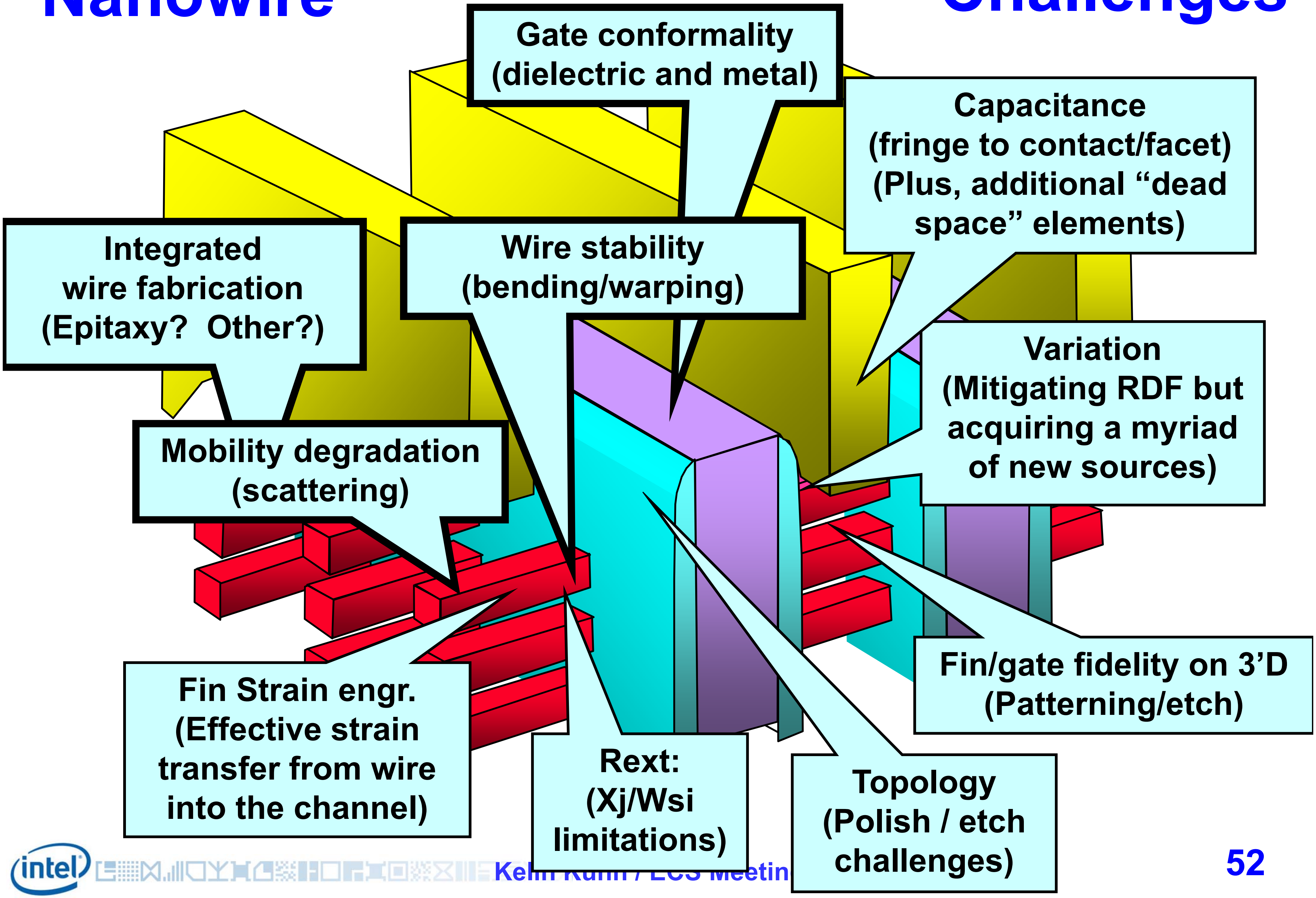
Nanowire Benefits



Nanowire Benefits

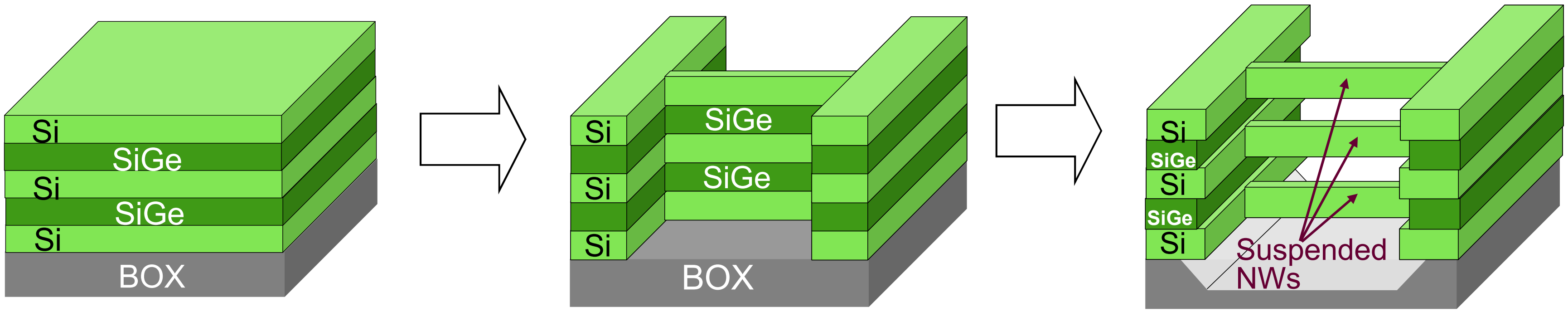


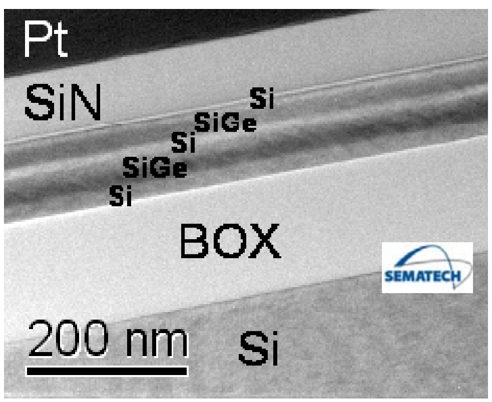
Nanowire Challenges

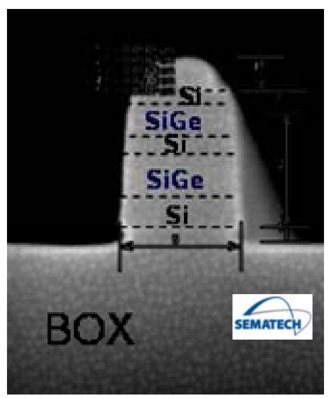


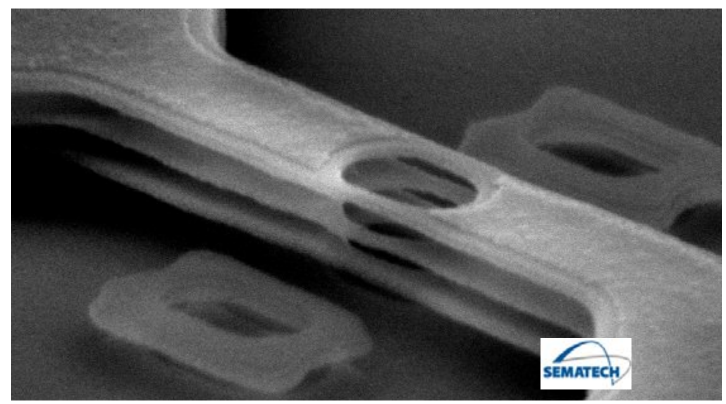
Stacked Si Nanowire Formation using SiGe

SiGe/Si Superlattice | Fin etch | Selective SiGe etch



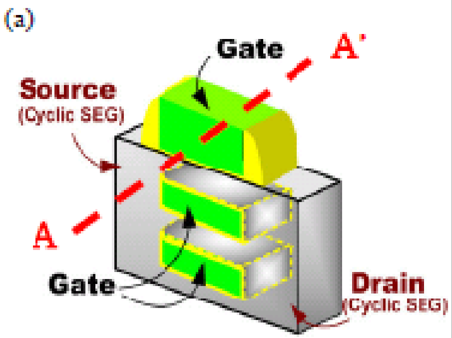


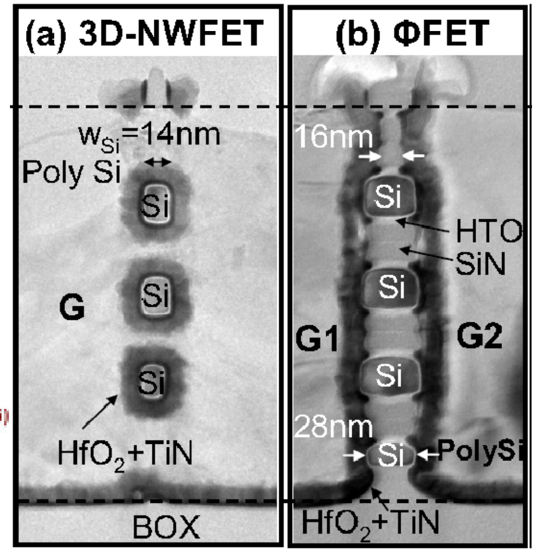


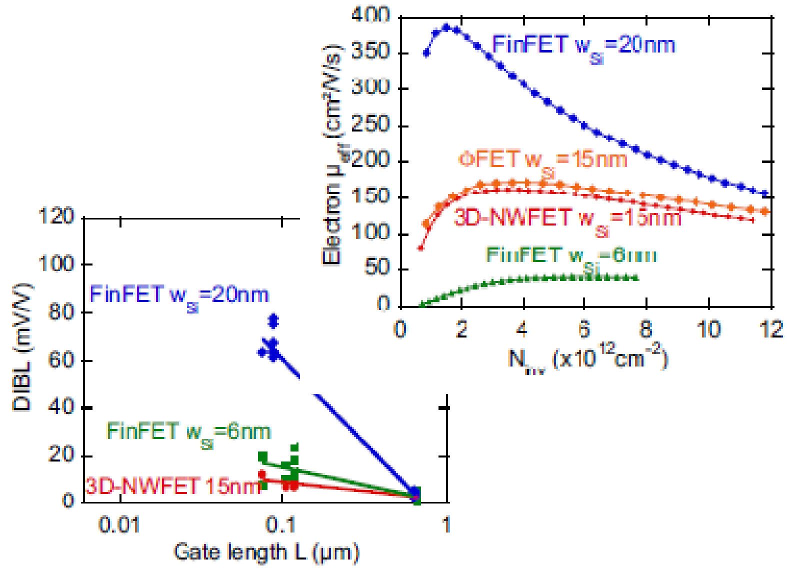


Nanowire FETs

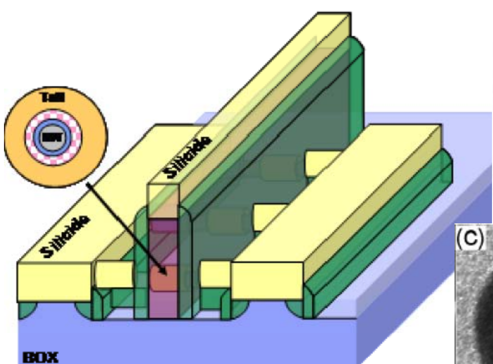
Dupre – CEA-LETI – IEDM 2008

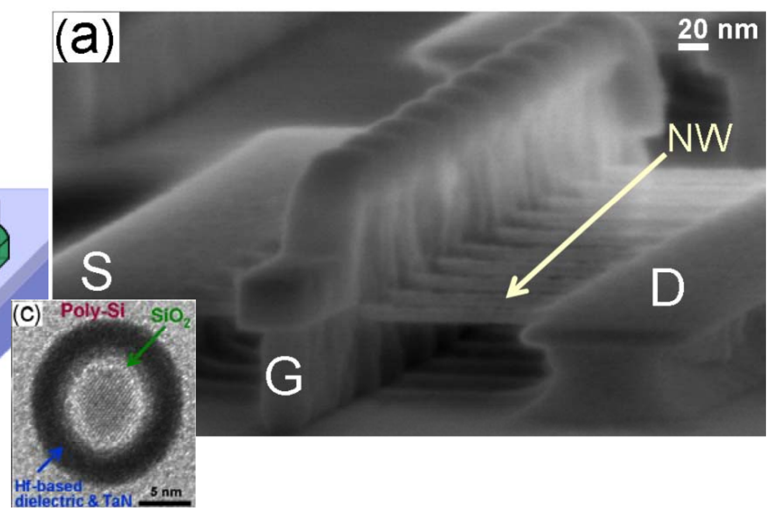


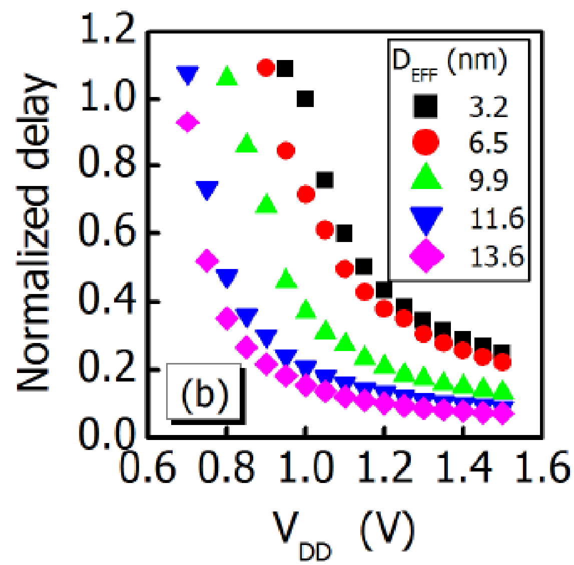




Bangsaruntip – IBM – IEDM 2009

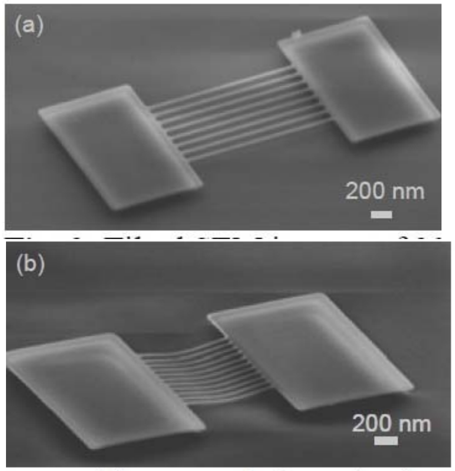


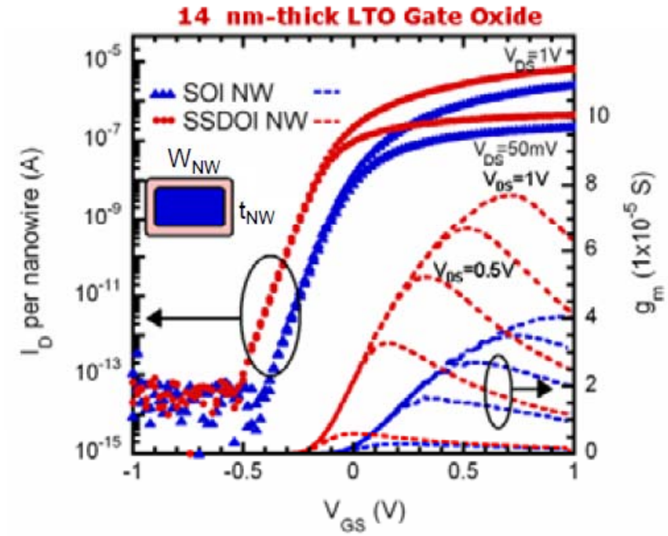


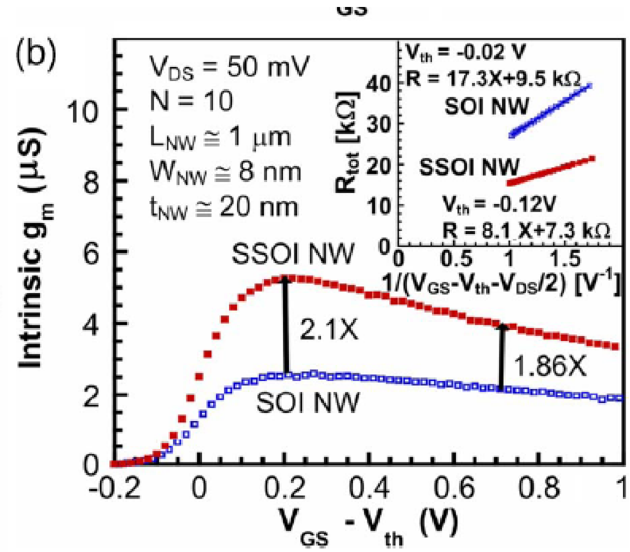


Nanowire FETs

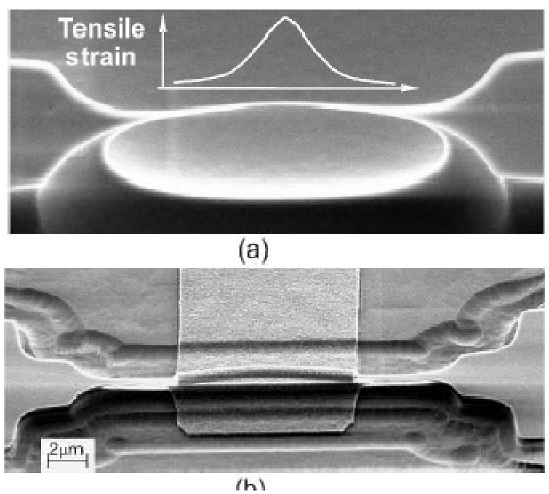
Hashemi/Hoyt – MIT
IEDM 2008 EDL/ESSDRC 2009

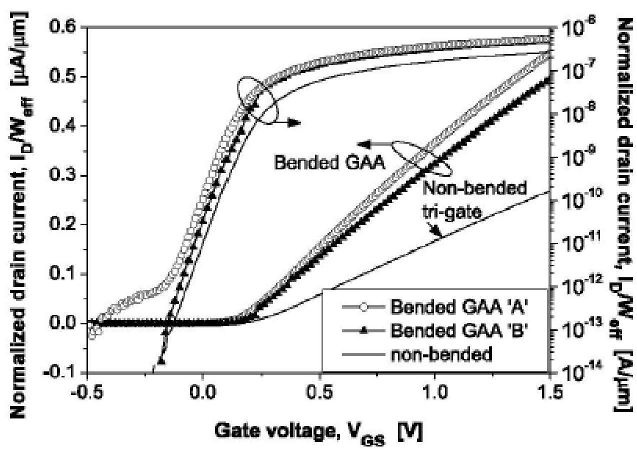


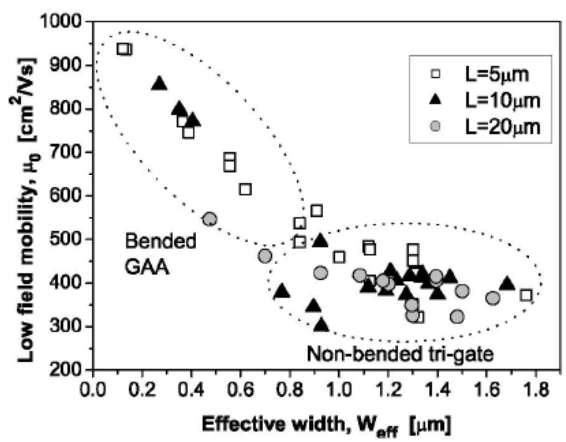




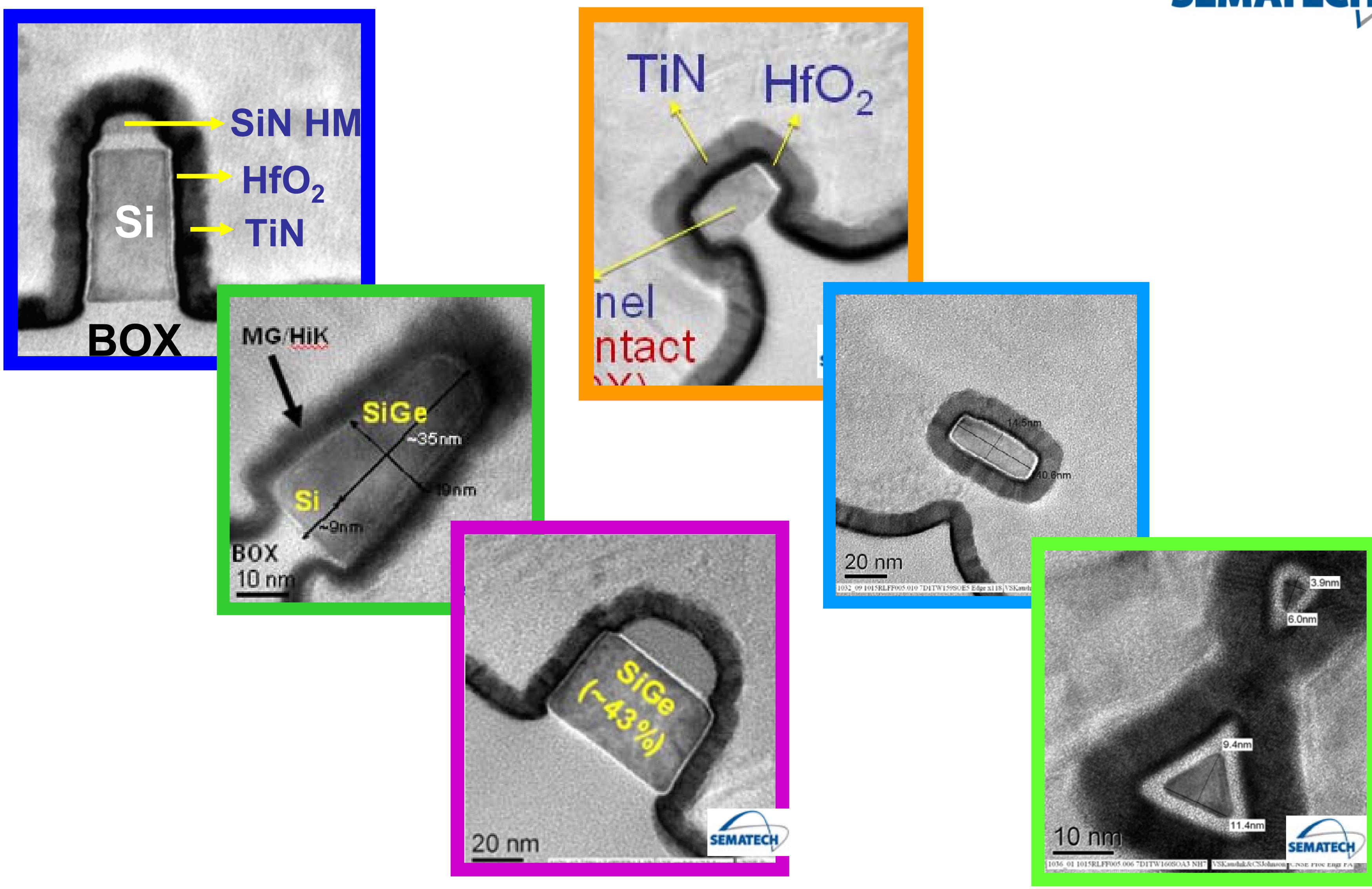
Moselund – Ecole Polytechnique, Switzerland
IEDM 2007







Non-planar options



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TFET (Tunneling Field-Effect Transistor)

Principle of operation

- Band-to-band- tunneling through source barrier, modulated by gate field

Advantages

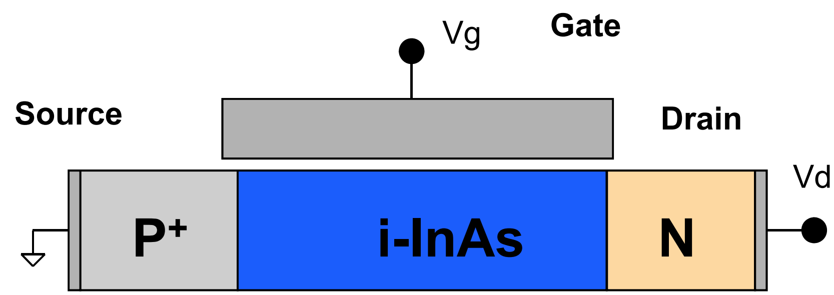
- Steep (< 60 mV/dec) sub-threshold slope
- Large Ion/Ioff ratio

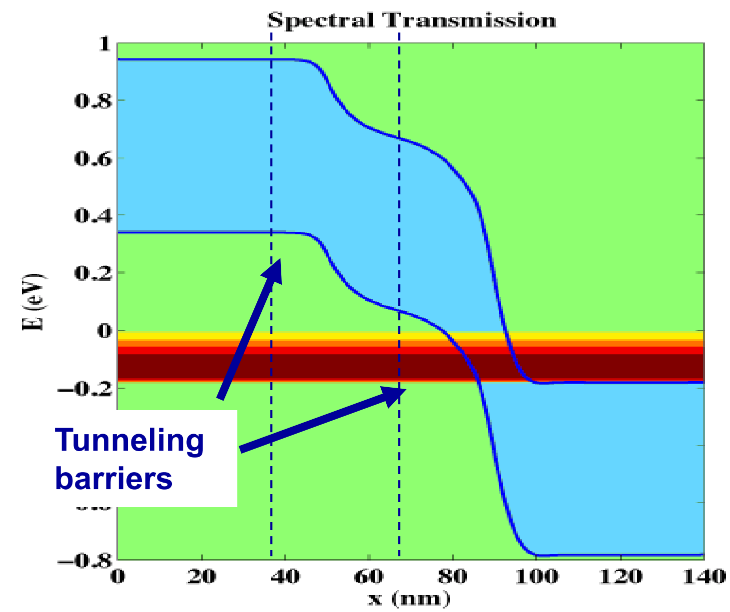
Disadvantages

- Low drive currents
- Ambipolar conduction
- Unidirectional conduction
- Potentially high hot-e^- effects

Materials choice?

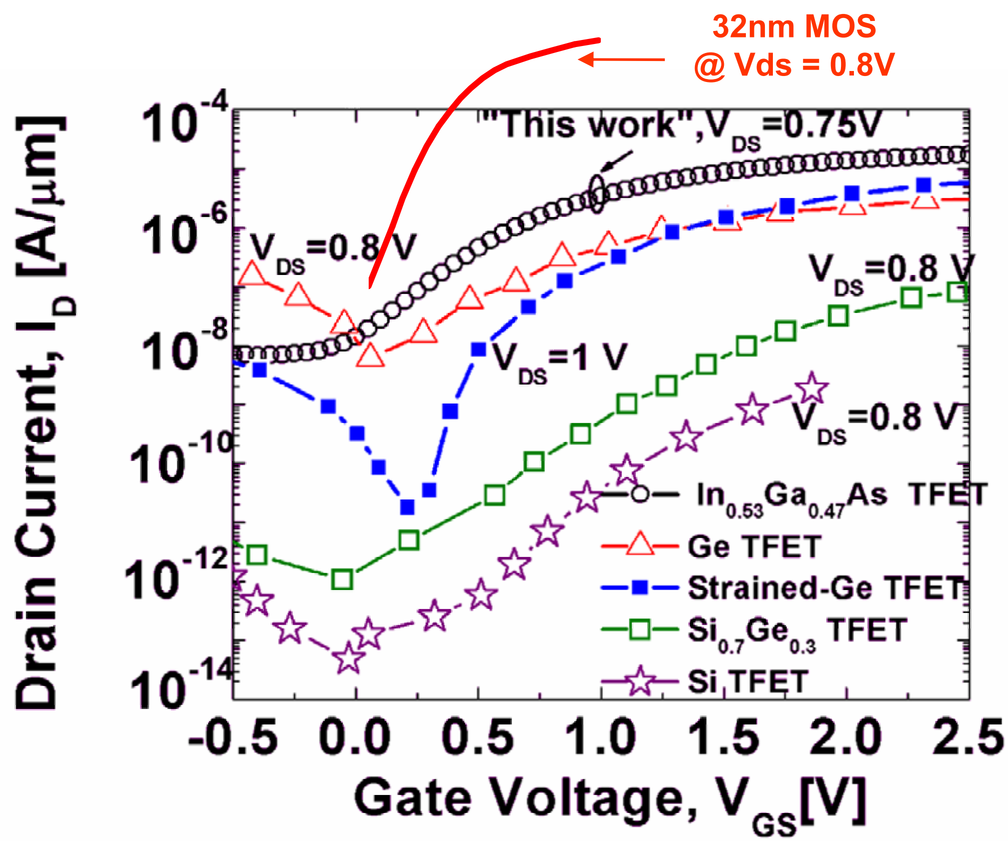
- A KEY question is whether some clever combination of Si, Ge, or $Si_{1-x}Ge_x$ can deliver enough drive current for viable TFETs.





Courtsey M. Luisier (Purdue)
M. Luisier and G. Klimeck, EDL, 2009

Best Demonstrated TFETs



S. Mookerjea et al., IEDM '09

- **Still MUCH lower drive currents than conventional MOS**
- **Require band-gap engineering with hetero-junction δ layers**
- **Sub-threshold slope still poor**

	Ref. [2]	Ref. [3]	Ref. [4]	[1]
SS (mV/dec)	52.8	42	~300	46
I_{ON} (μA/μm)	12.1	0.01	1E-4	1.2
I_{ON}/I_{OFF}	1E4	1E4	1E2	7E7

Table. I. Comparison to reported silicon TFETs. (V_{DS}=V_{GS}-V_{BTBT}=1.0V)

[1] K. Jeon, et al., VLSI (11.4.1.-1) 2010
[2] W. Choi et al., IEEE-EDL vol.28, no.8, p.743 (2007)
[3] F. Mayer et al., IEDM Tech Dig., p.163 (2008)
[4] T. Krishnamohan et al., IEDM Tech Dig., p.947 (2008)

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Summary

- **Strain from e-SiGe S/D PMOS is a critical part of modern CMOS technology - replacement technologies must exceed the "high bar" set by e-SiGe PMOS.**
- **Strained SiGe/Ge PMOS offers a potential mobility advantage over strained Si. However, gate dielectric engineering remains the key roadblock to competitive performance.**
- **Non-planar architectures will be of increasing interest for the 15nm node and beyond. Integrating e-SiGe S/D and/or Si/SiGe channels in non-planar architectures offers significant new challenges.**
- **TFETs are gaining visibility as potential ultra-low power devices, leveraging better than 60mV/dec SS. Significant challenges to constructing Si-Ge/SiGe TFETs with competitive drive currents.**

Questions?