The Ultimate CMOS Device and Beyond

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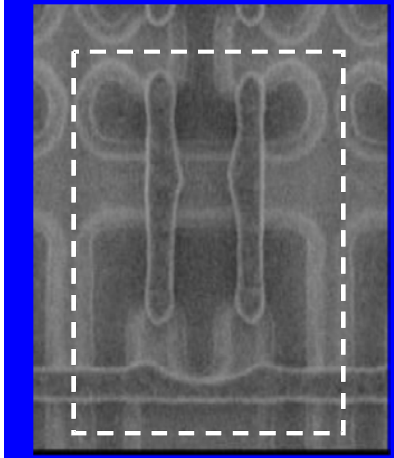
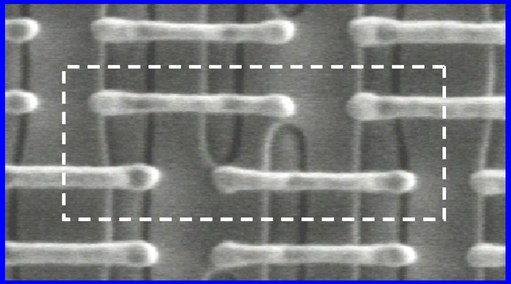
Intel Corporation, Technology and Manufacturing Group, Hillsboro, OR 97124, USA

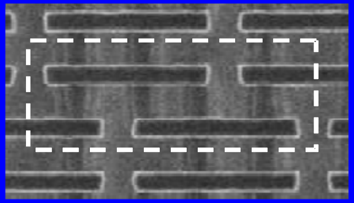
Process Evolution Over Time



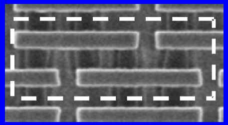
90nm – TALL
1.0 μm^2



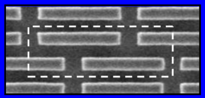
65nm – WIDE
0.57 μm^2



45nm – WIDE
0.346 μm^2

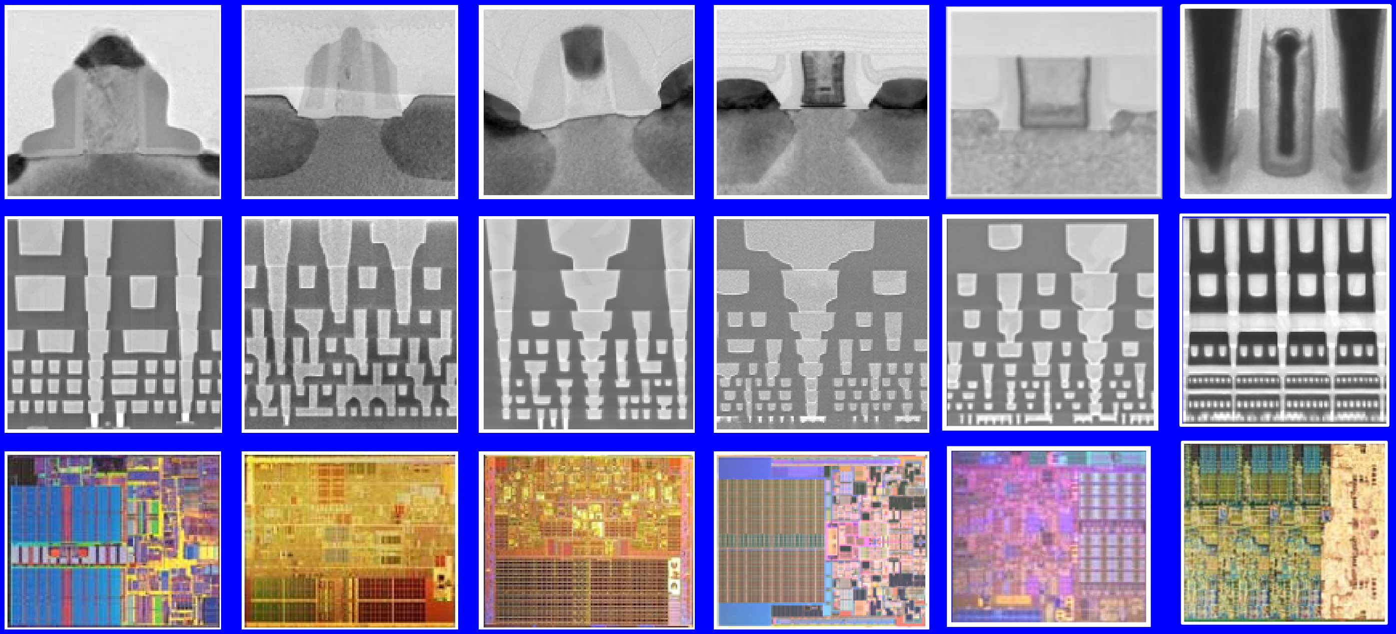


32nm – WIDE
0.171 μm^2



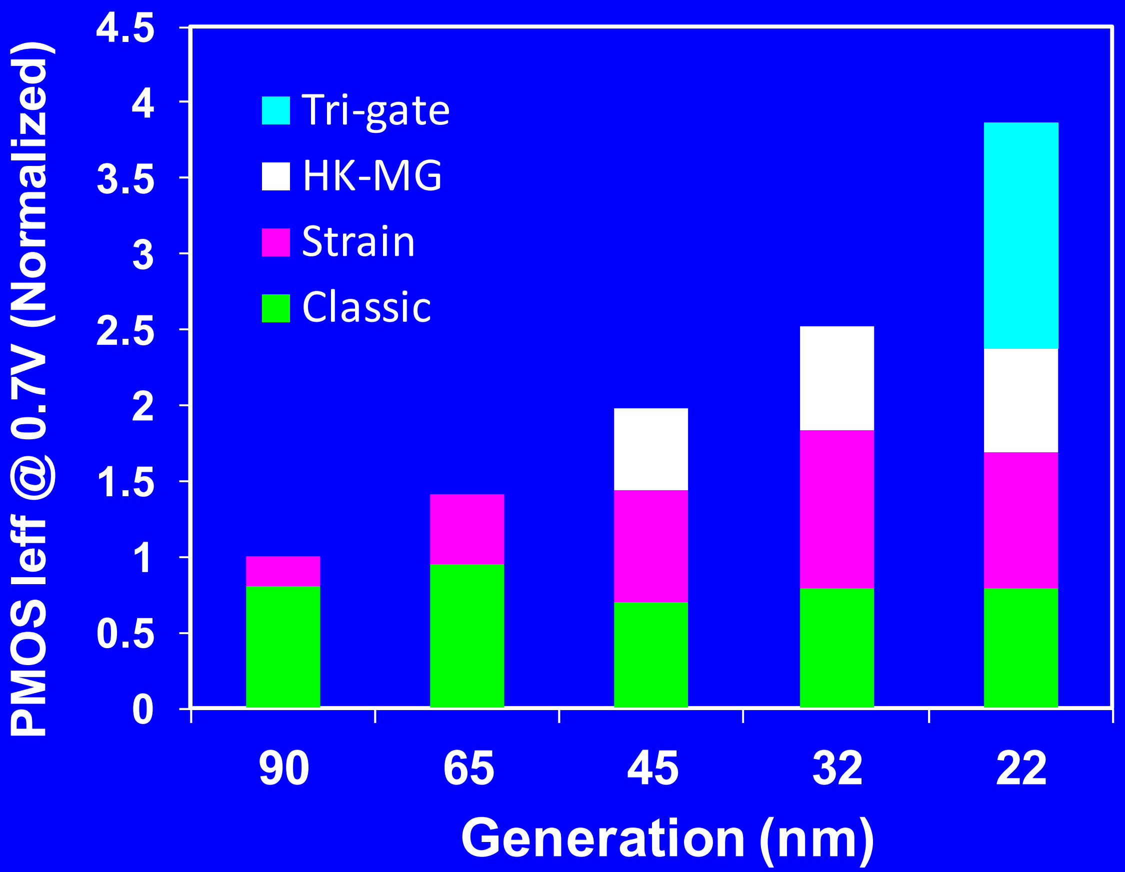
22nm – WIDE
0.092 μm^2

130 nm	90nm	65nm	45nm	32nm	22nm
2001	2003	2005	2007	2009	2011



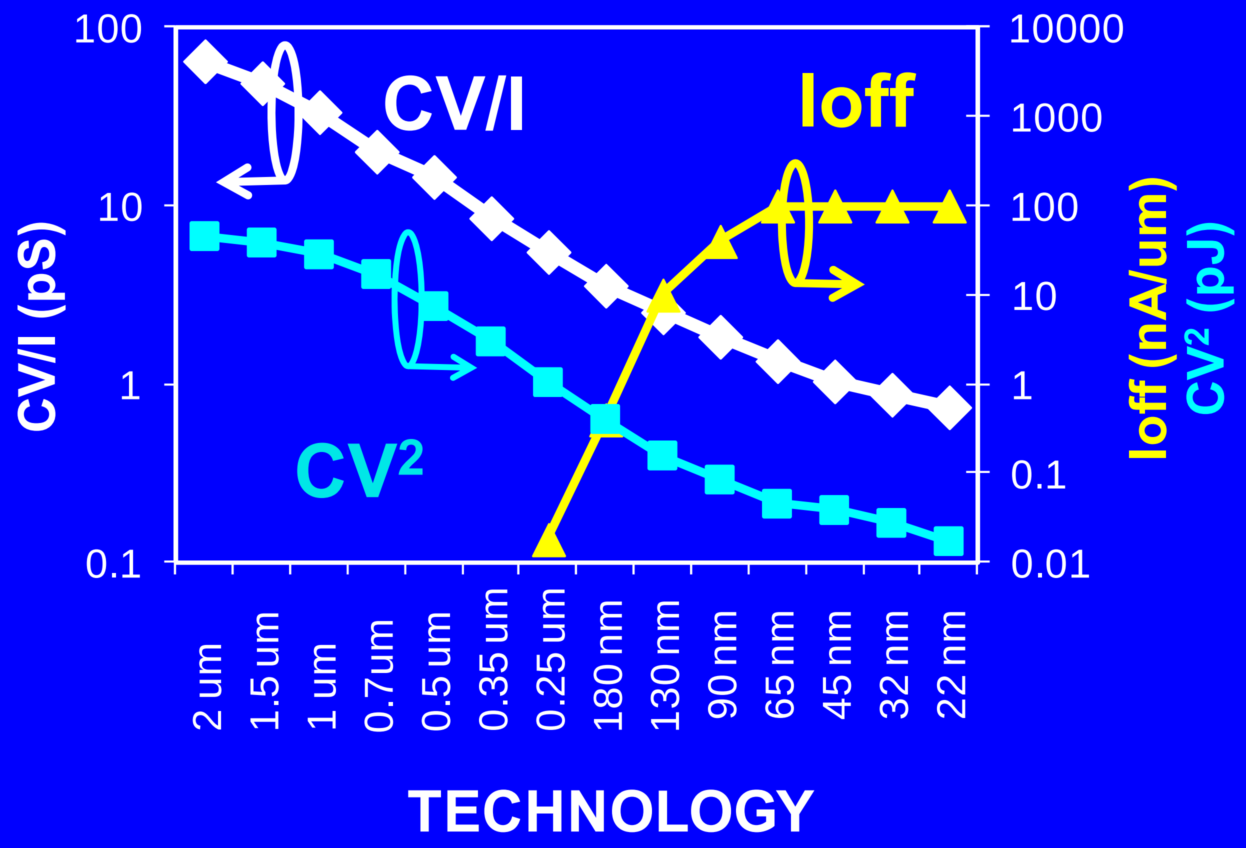
Bohr
Intel Press
release
2012

Supporting the Moore's Law Roadmap



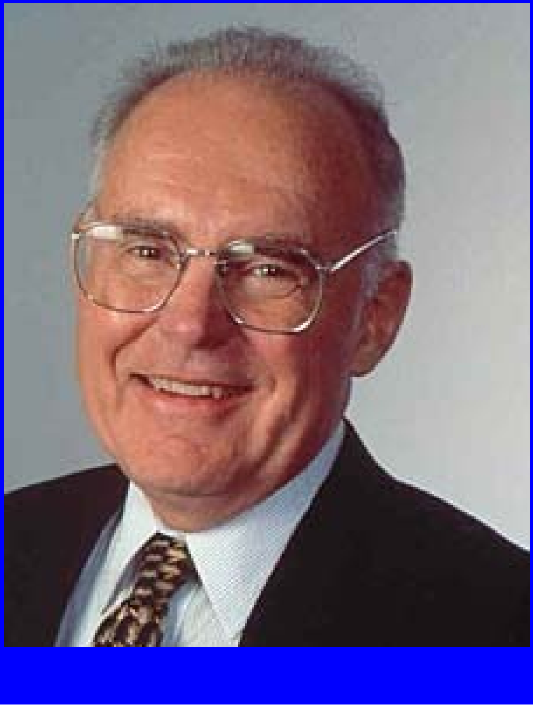
Manufacturing implementation of
strain, HK-MG and non-planar TriGate devices
continues to support and energize the Moore's Law roadmap

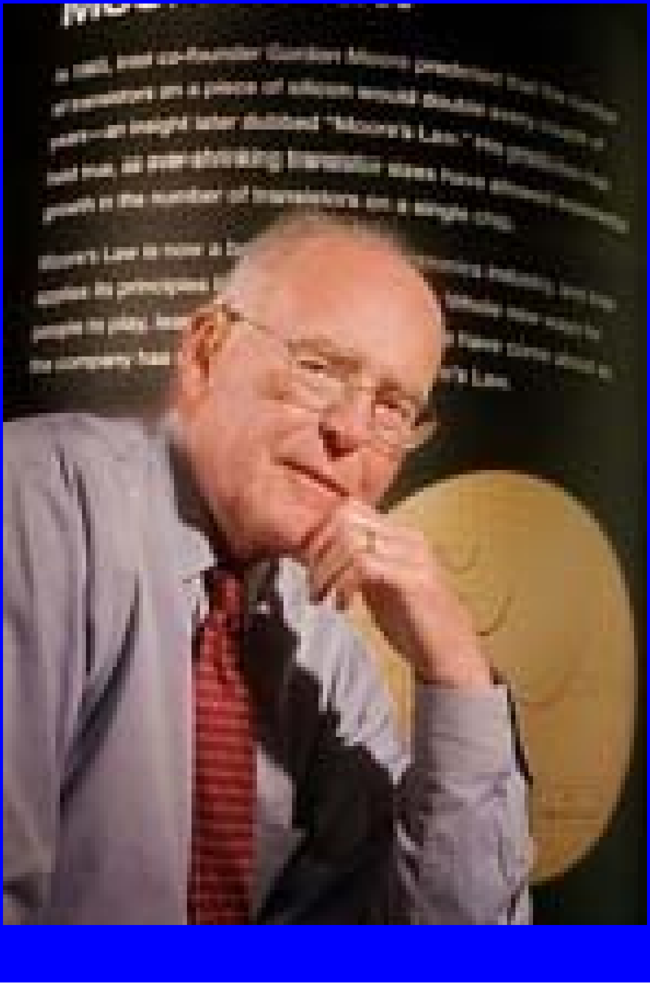
CV/I, CV^2 and Ioff Trends (Average of N and PMOS)



CV/I and CV^2 have steadily improved over time
even in the presence of dramatic shifts in transistor targeting
driven by consumer demand for lower power mobile products.

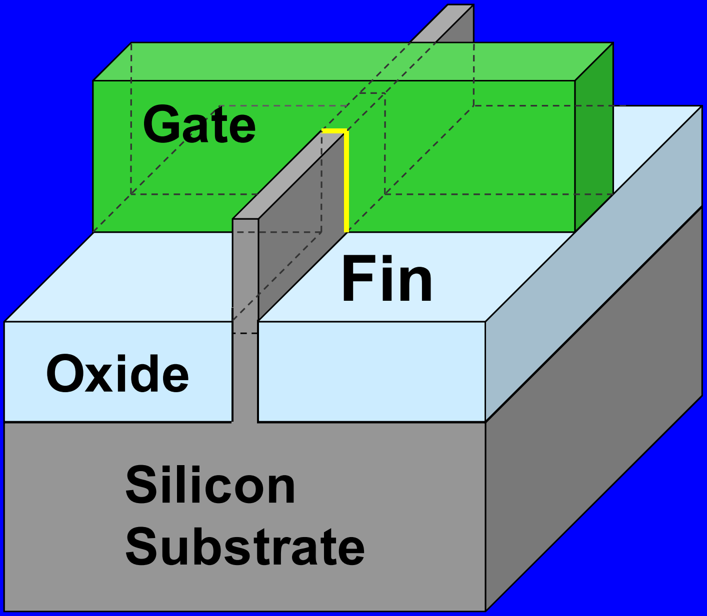
MORE
MOORE

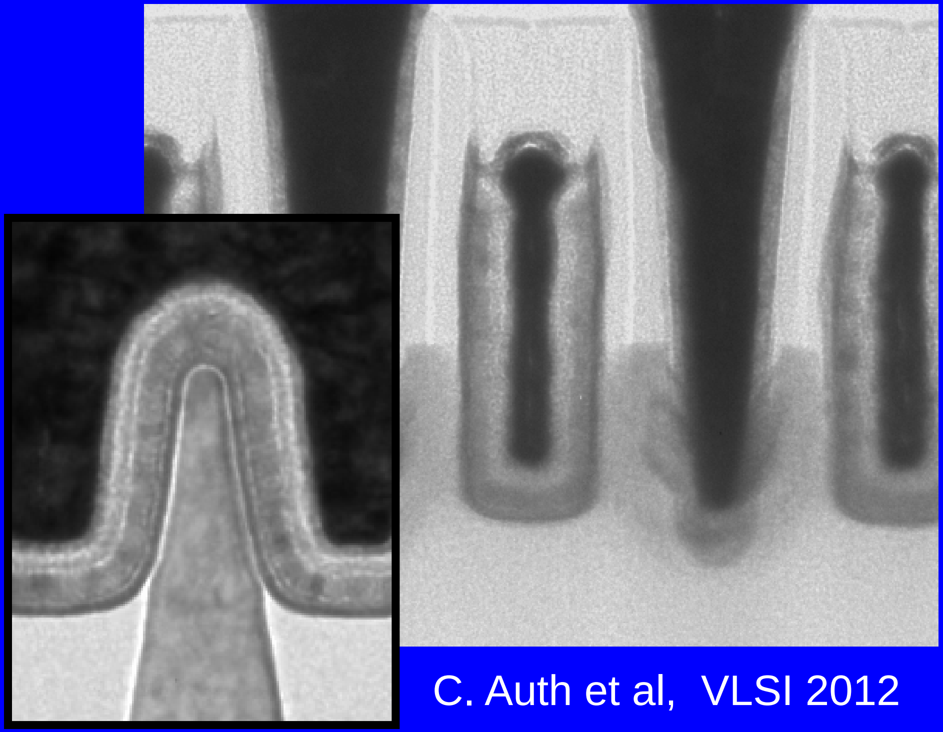




22nm TriGate – End of the Planar Era

2012

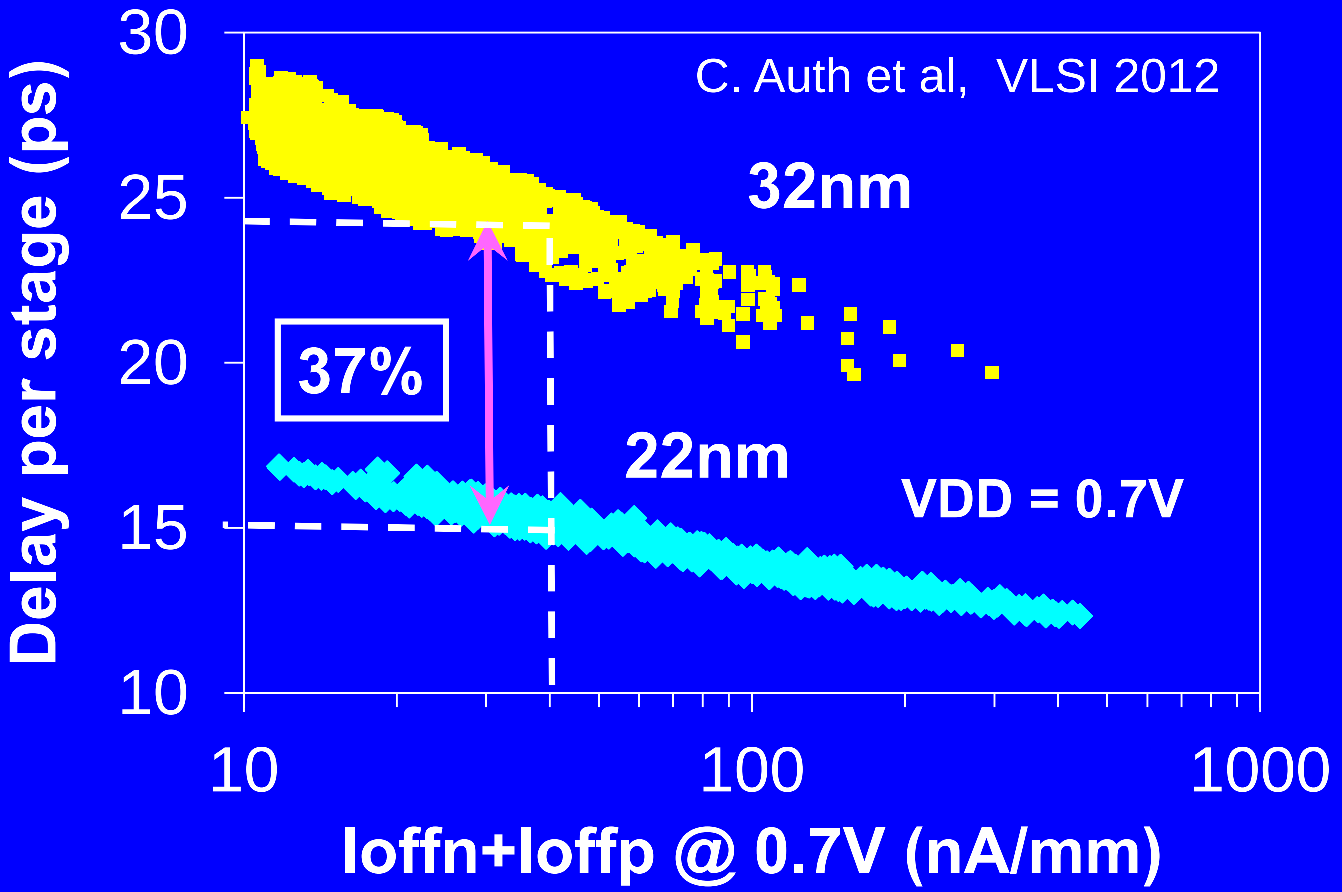




C. Auth et al, VLSI 2012

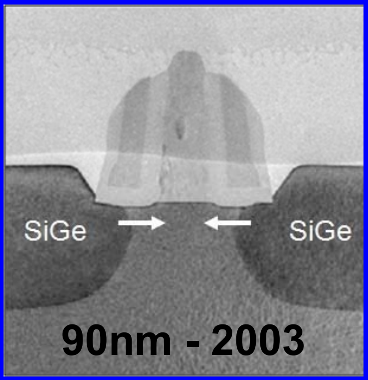
The introduction of the TriGate device in the 22nm node marked the end of the planar device era

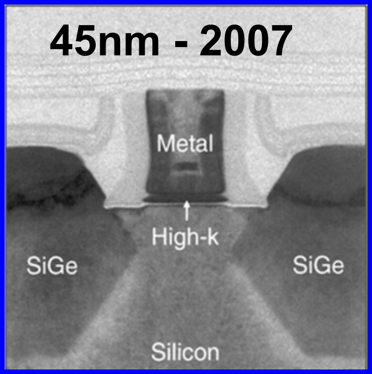
22nm TriGate Performance Comparison

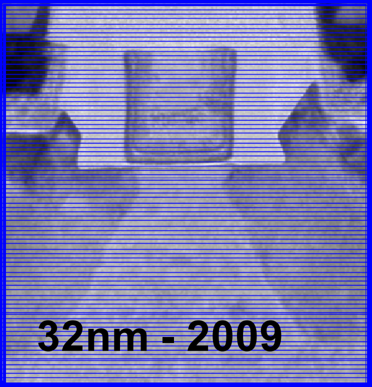


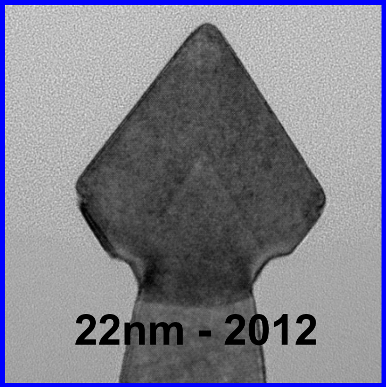
The 22nm TriGate delivers >35% performance improvement over the 32nm generation at 0.7V with 40nA/μm I_{off}

TriGate: Innovation in Manufacturing

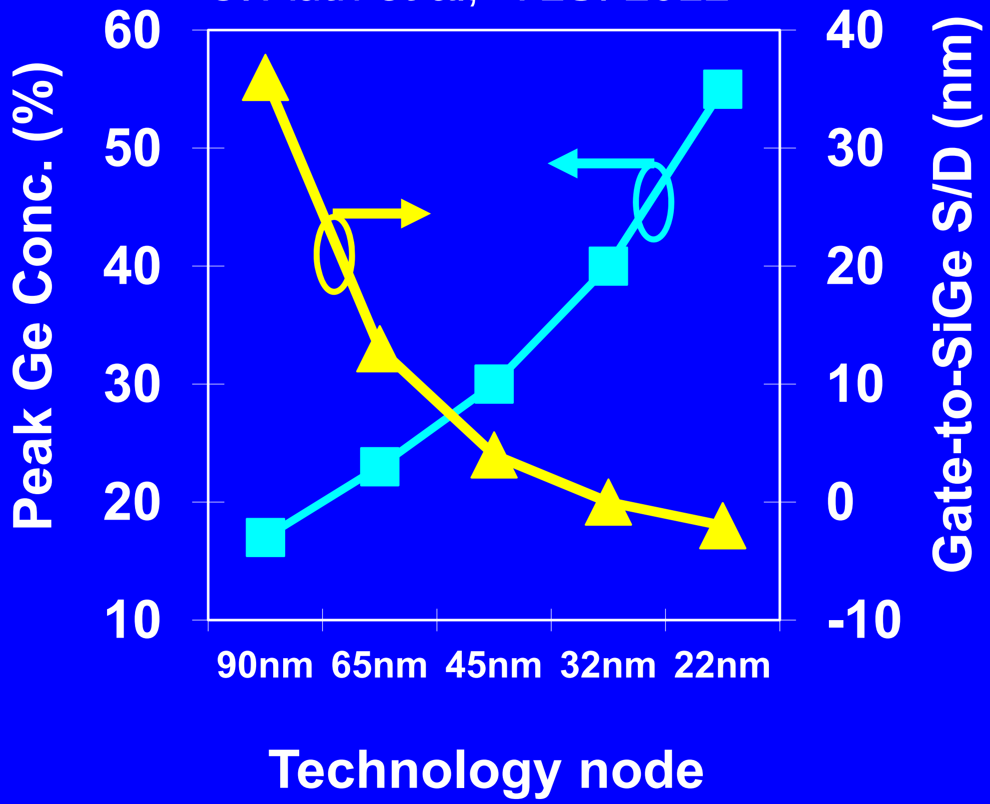








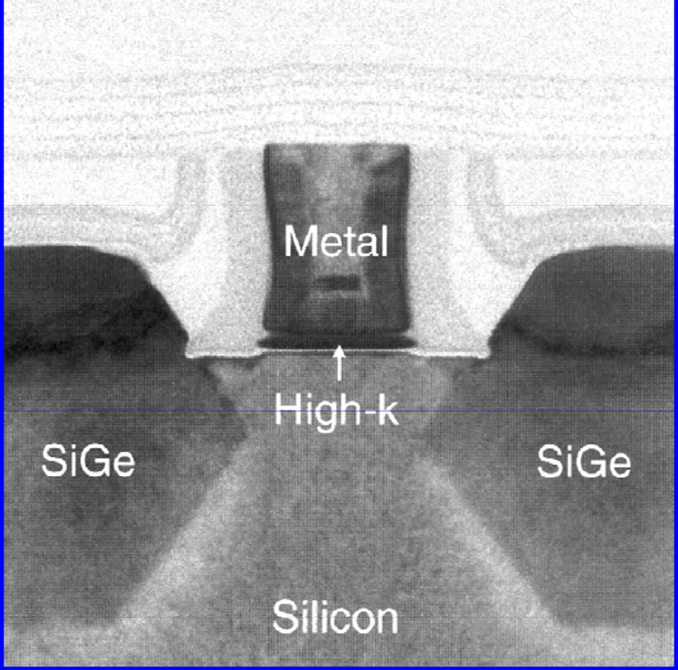
C. Auth et al, VLSI 2012



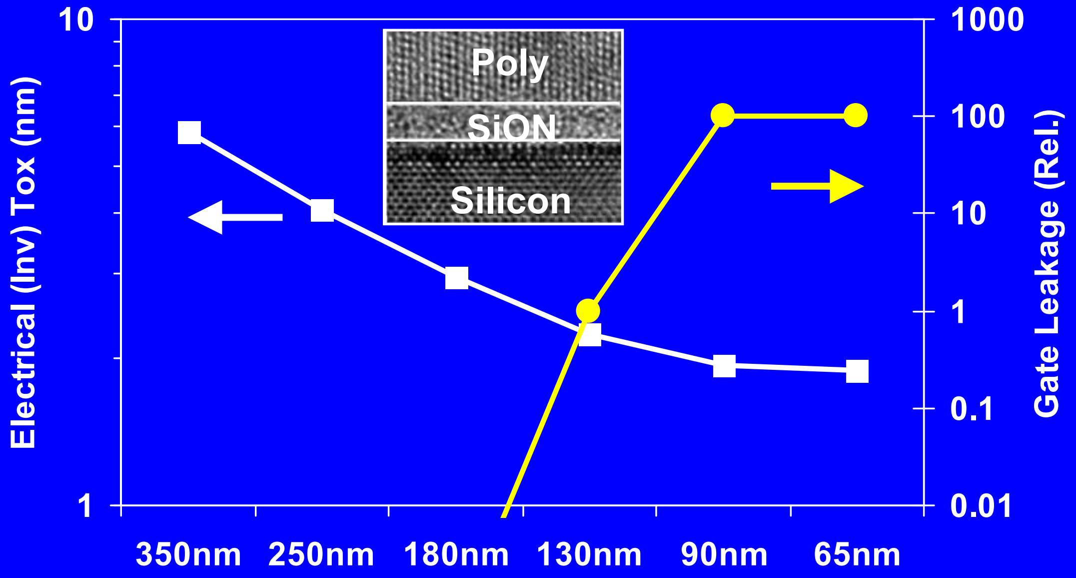
Successfully integrating 22nm TriGate devices required innovative new manufacturing technologies

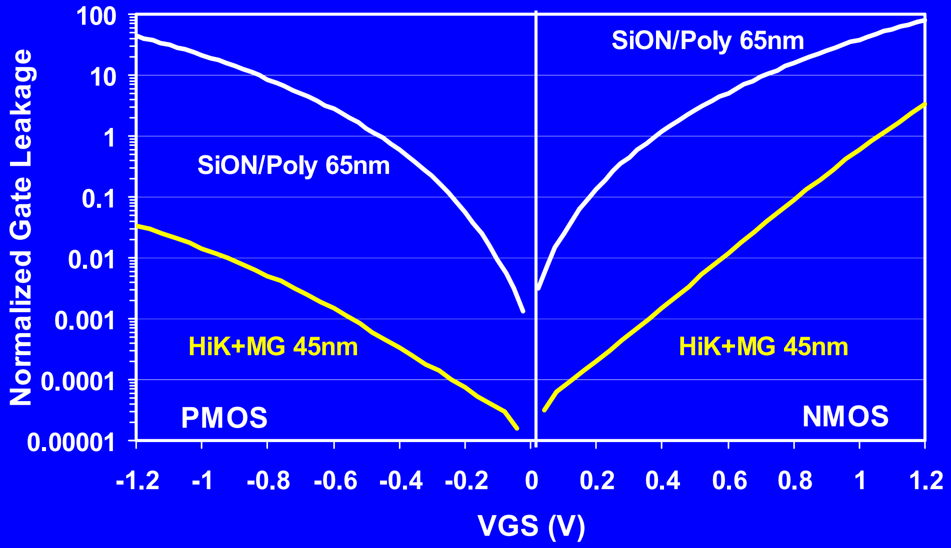
Electrostatics Improvement with HiK-MG

2007

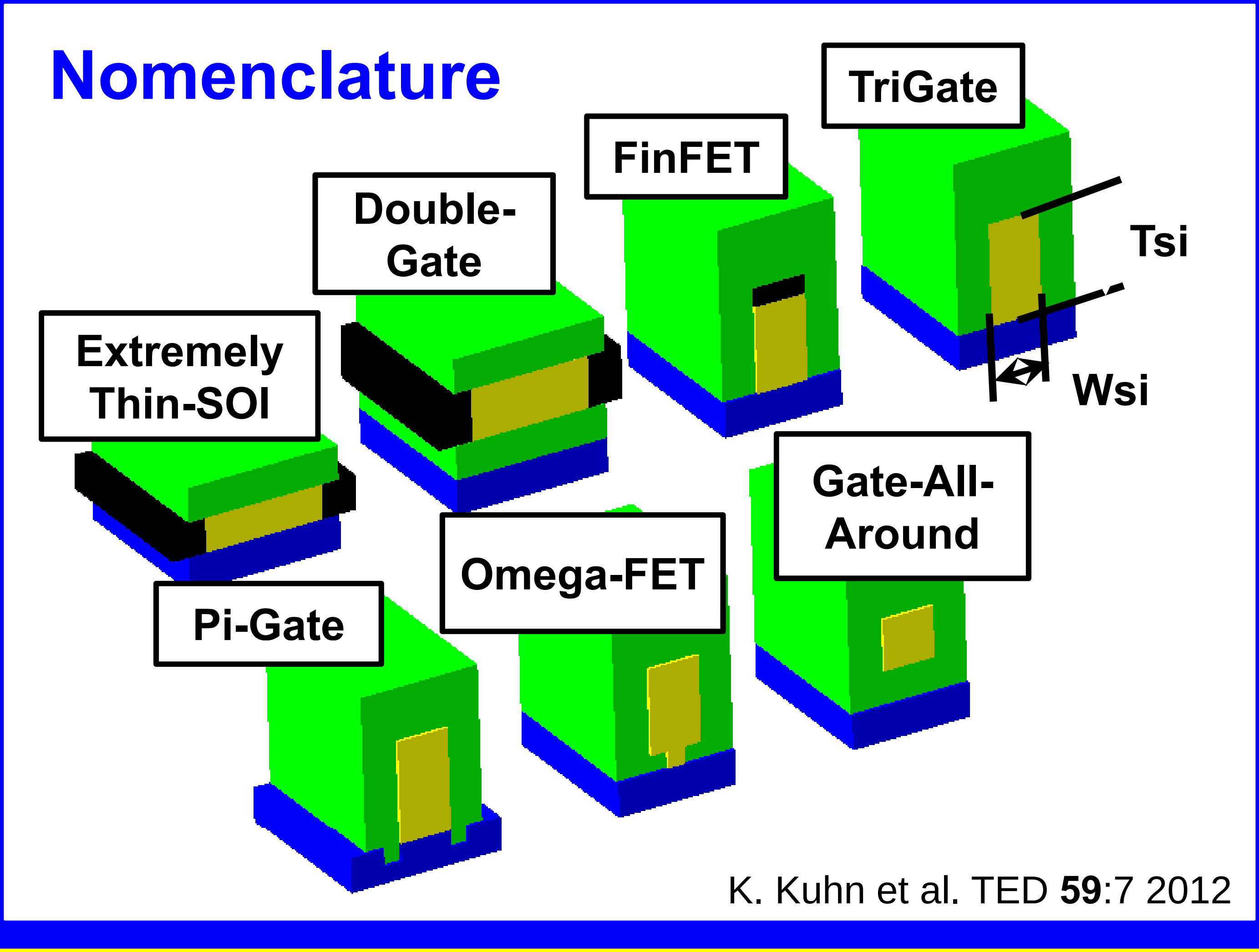


K. Mistry et al, IEDM 2007





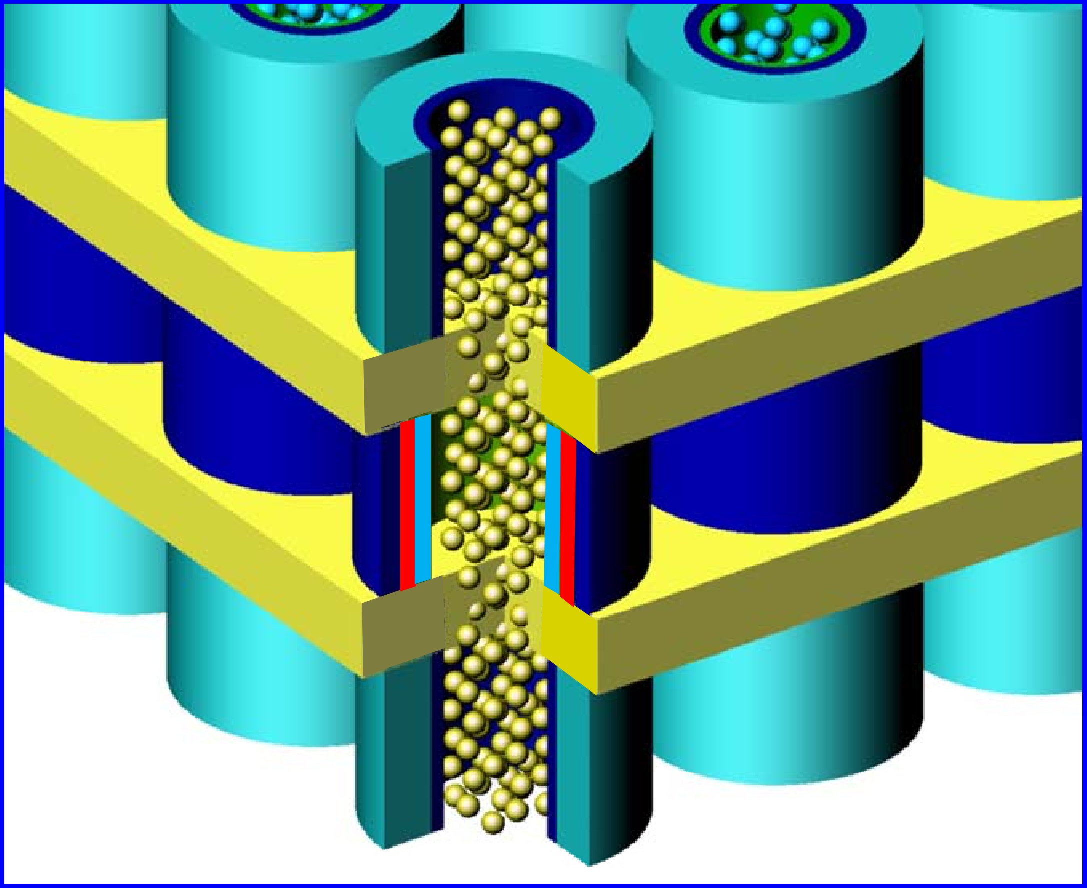
Nomenclature



K. Kuhn et al. TED **59**:7 2012

A variety of advanced architectures have been proposed for improved electrostatic control

GAA: Gate-all-around Architecture



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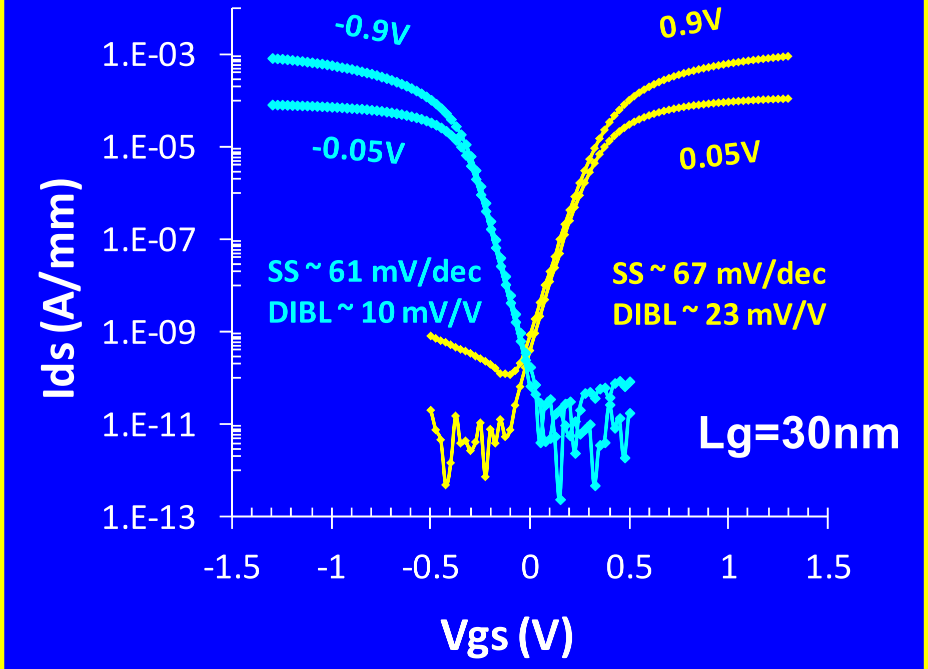
The Gate-all-around architecture is the limit of structural electrostatic control

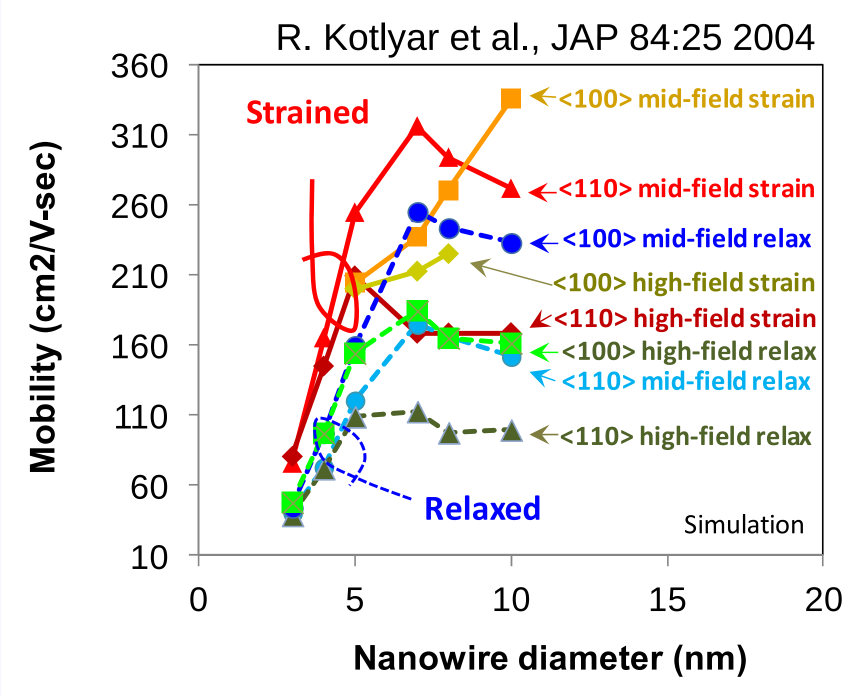
GAA: Gate-all-around Architecture

BENEFITS



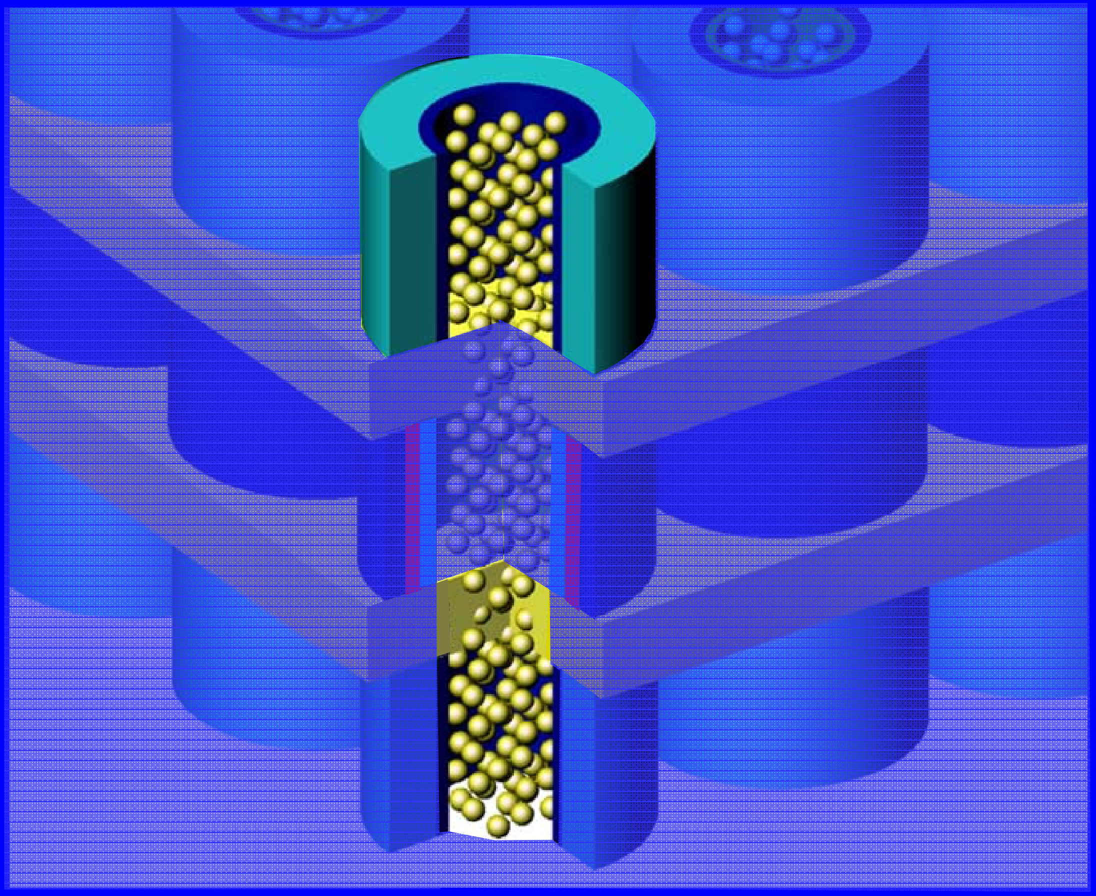
Outstanding
short channel control

CHALLENGES



Mobility degradation
with diameter

Parasitic Rext



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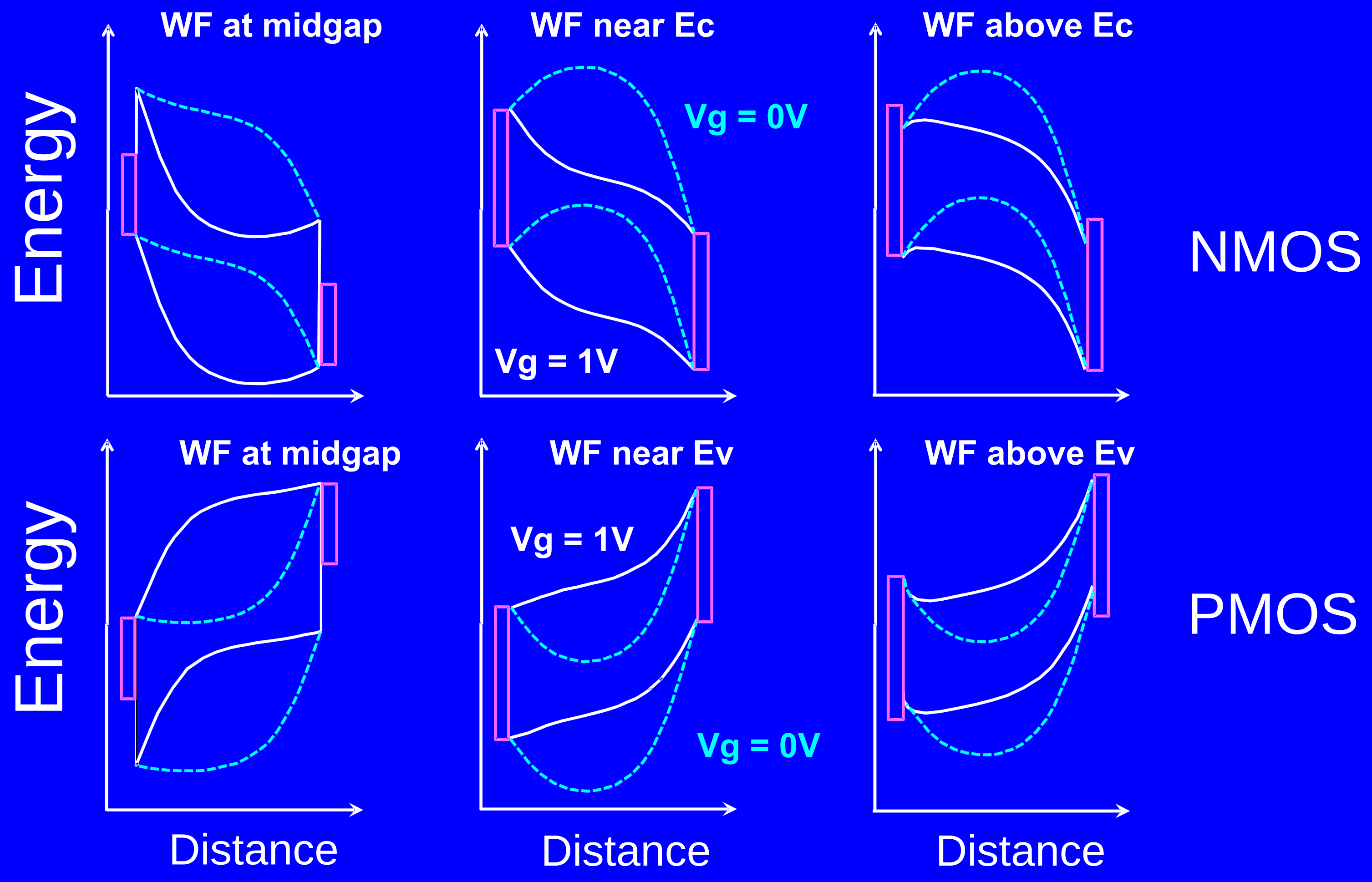
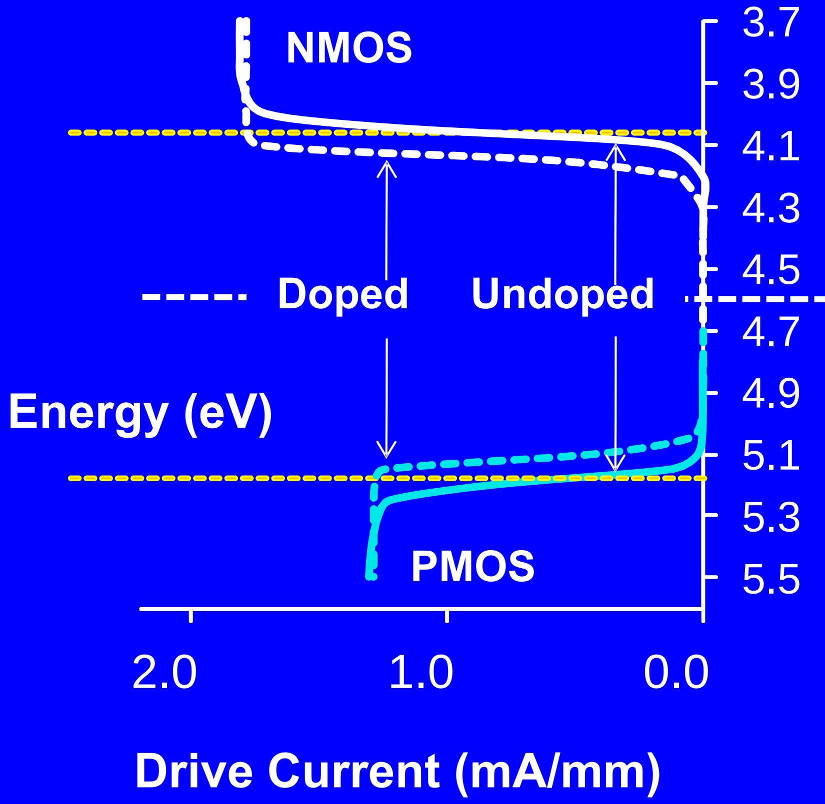
Parasitic external resistance continues to be a significant challenge in modern devices.

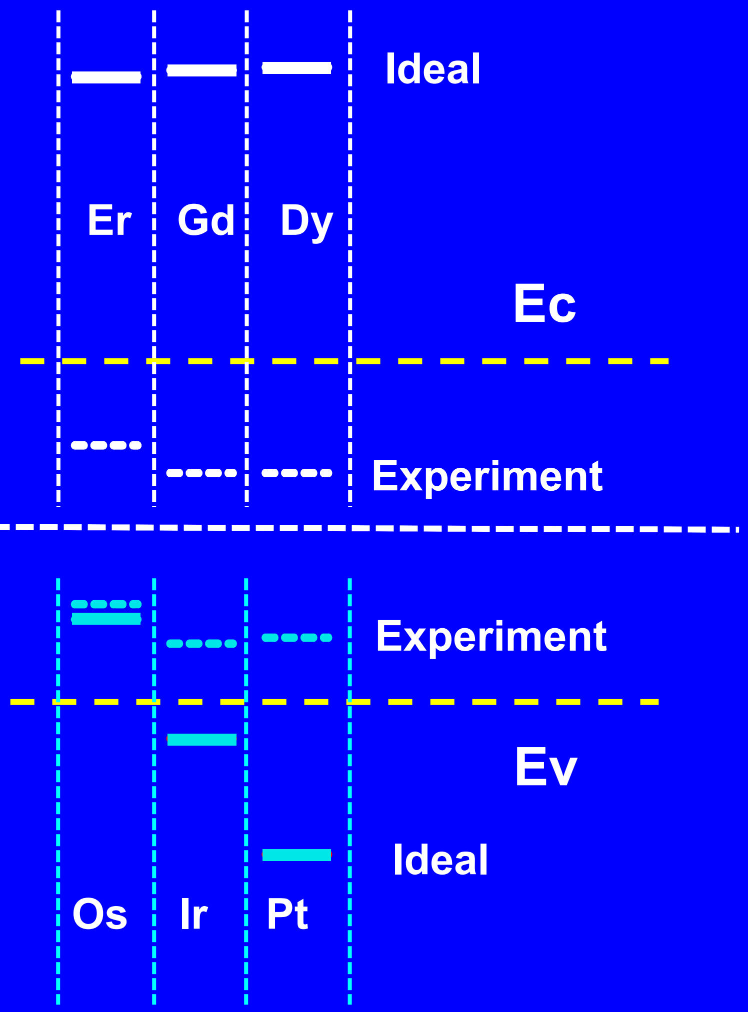
Metal Source-Drain Devices



In a Metal S/D device the metal workfunction needs to be at or above bandedge

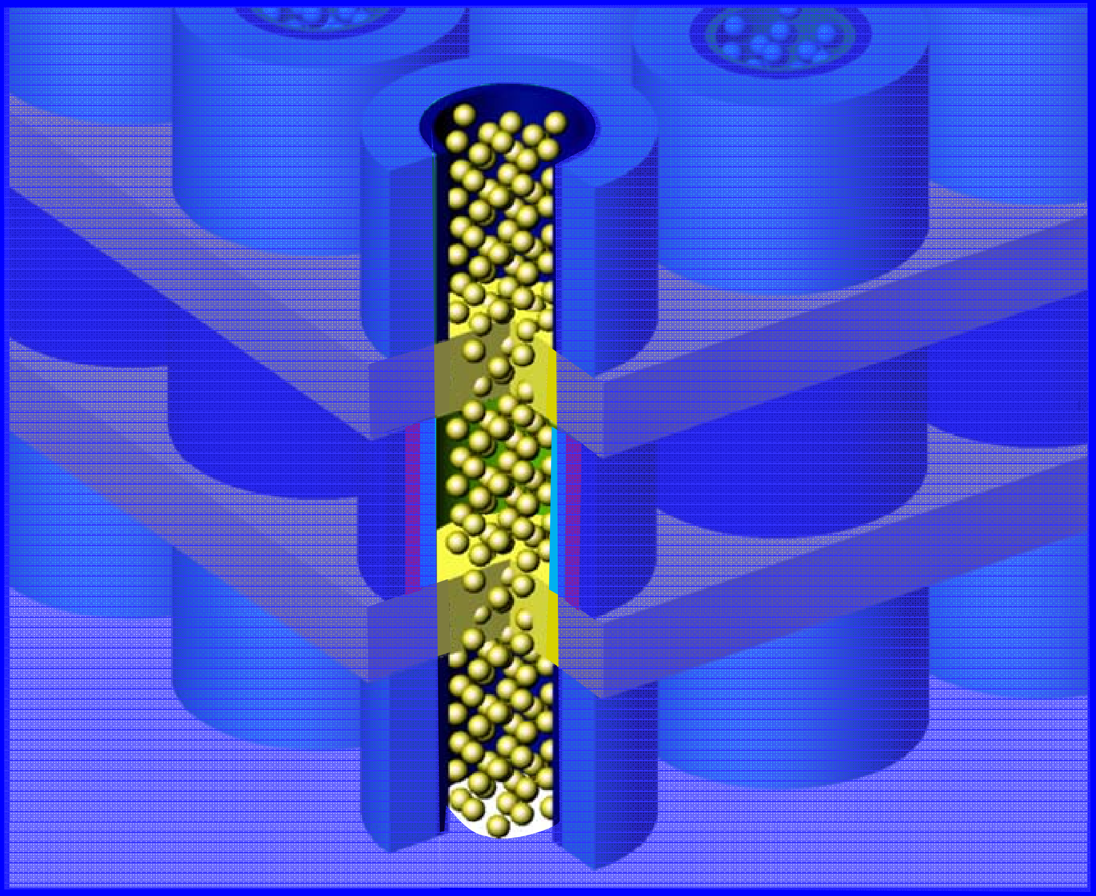
Metal S/D Devices





The challenge with metal S/D devices is resolving Fermi-level pinning at the metal-semiconductor junction

Advanced Channel Materials



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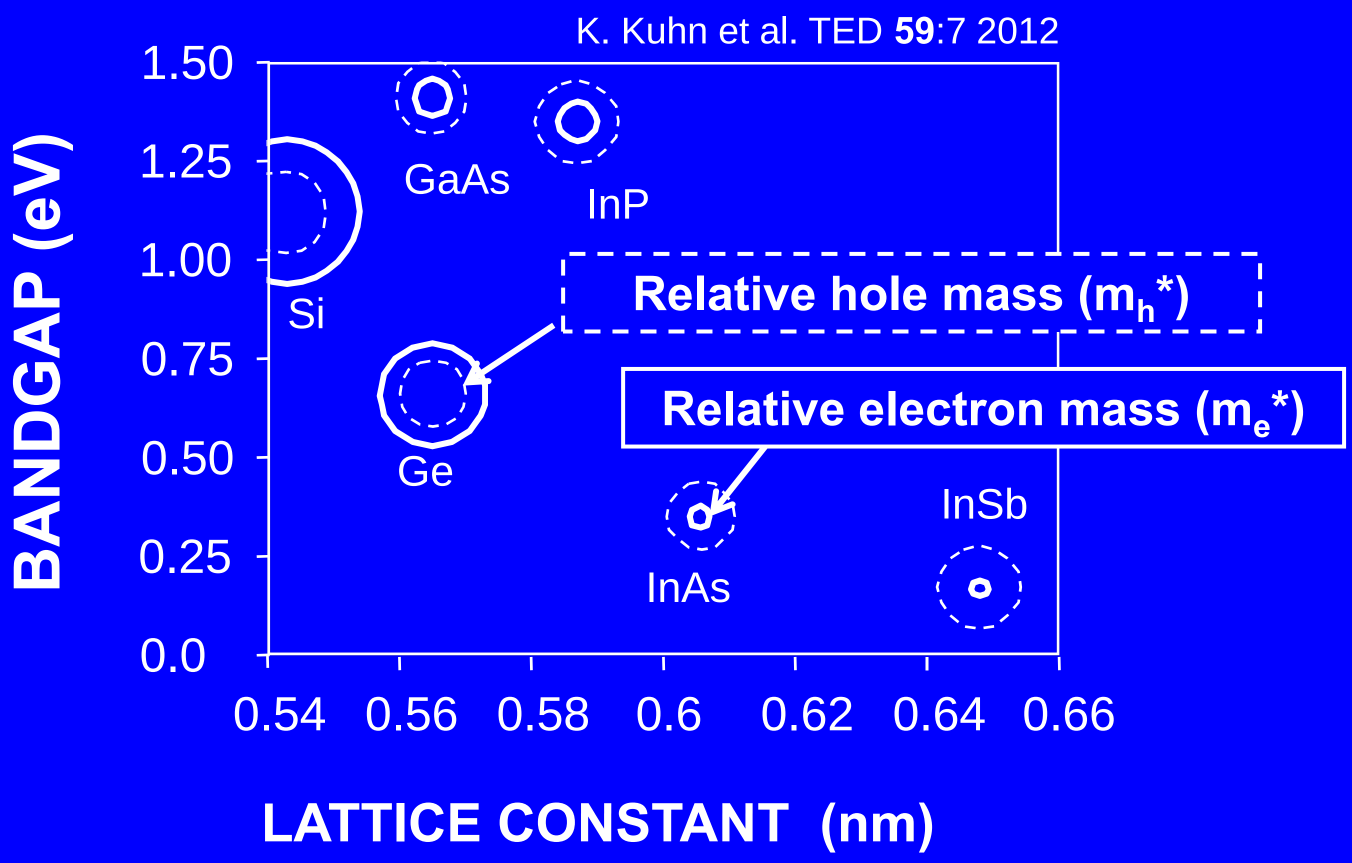
$I=Qv$

A number of non-silicon advanced channel materials are under evaluation

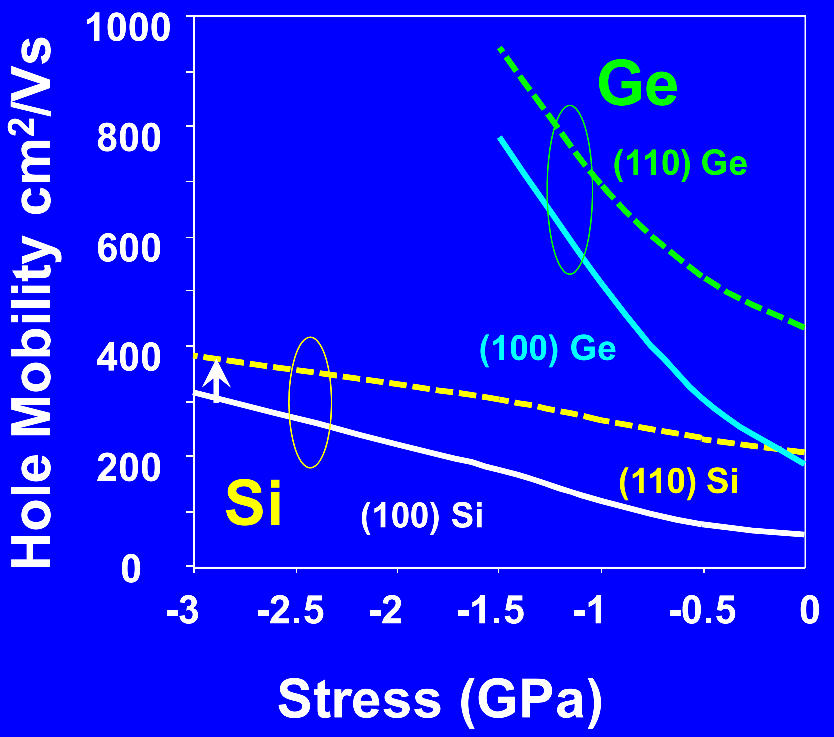
“Traditional” Advanced Channel Materials



The traditional advanced channel materials have improved effective mass in comparison with silicon

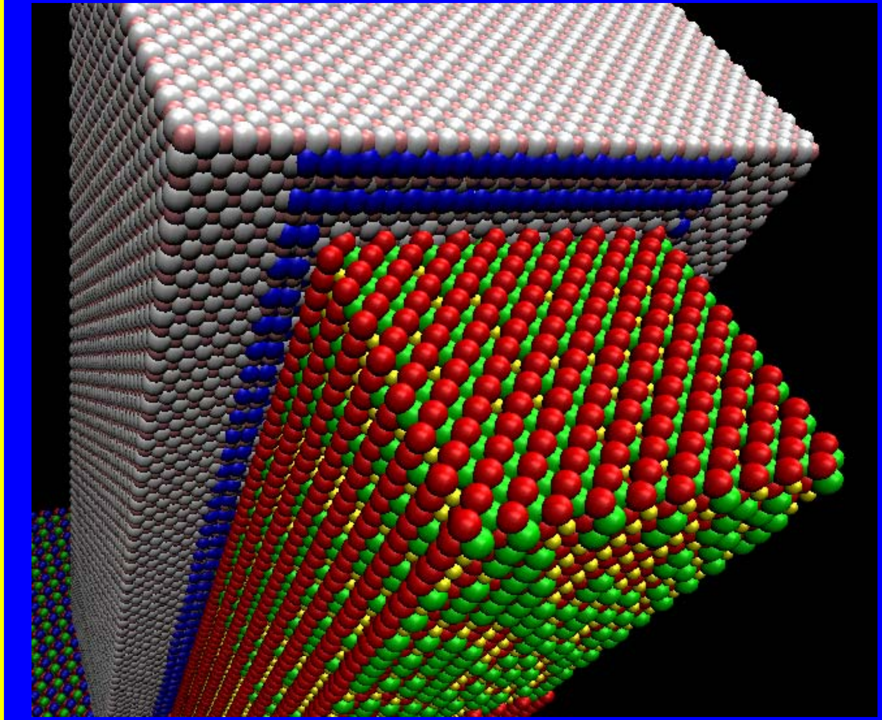
“Traditional” Advanced Channel Materials

BENEFITS



Better mobility and better mobility with stress

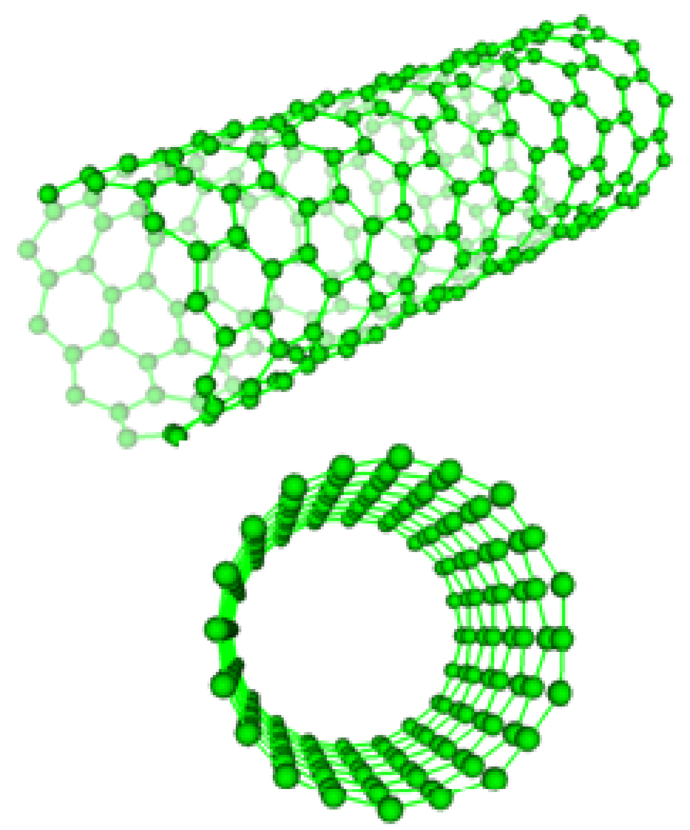
CHALLENGES

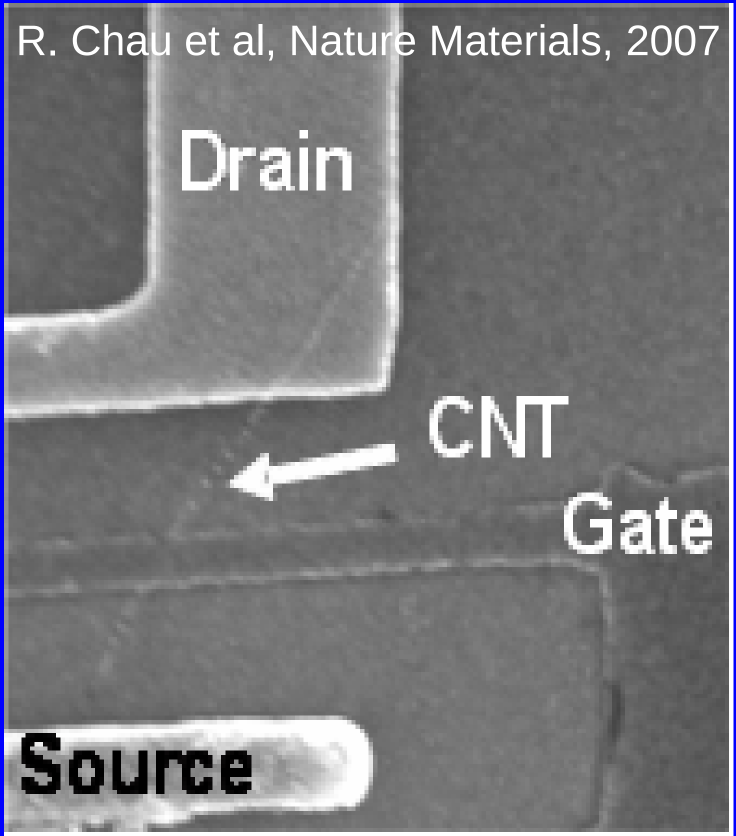


Fabricating high quality gate dielectrics on the channel

K. Kuhn et al. ECS Trans. **33**:6, 2010

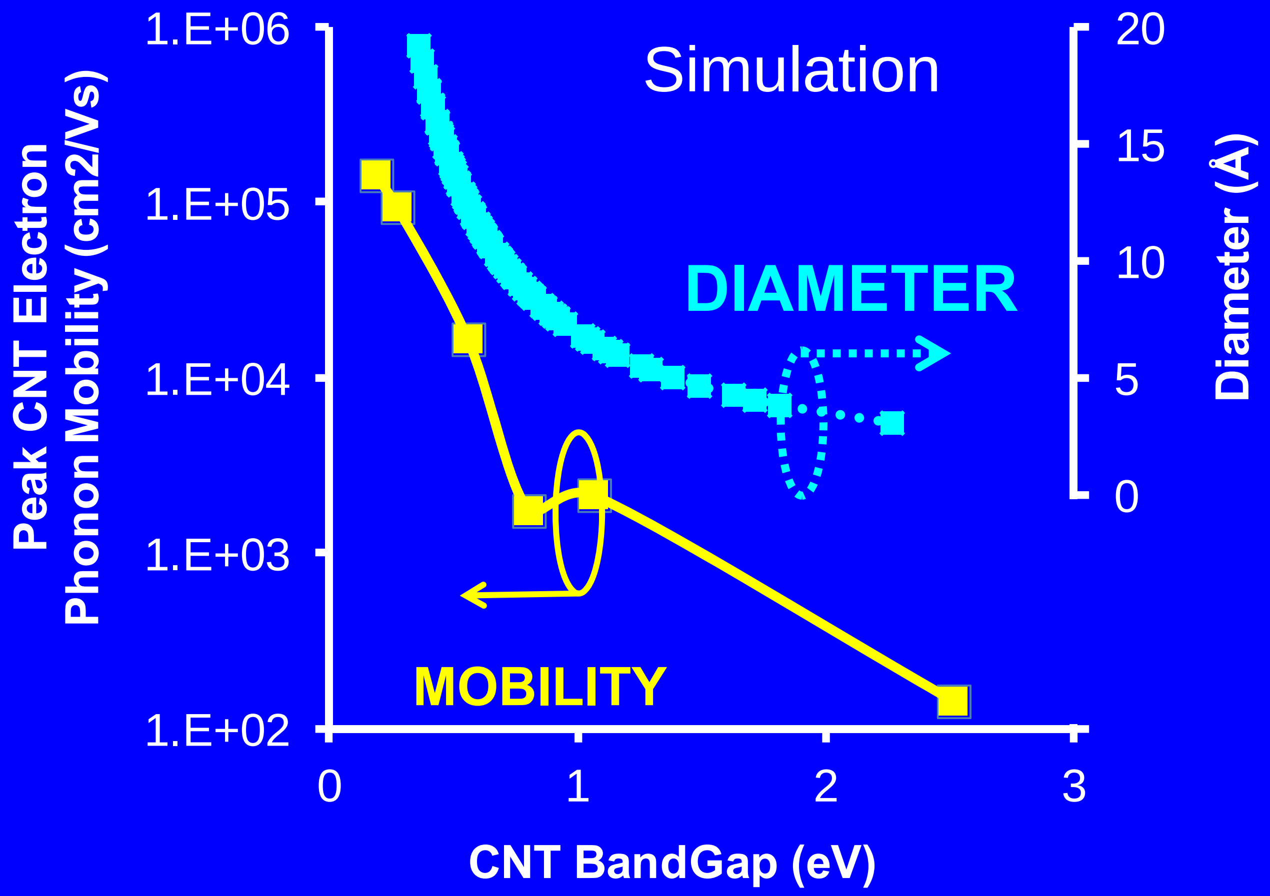
2’D Advanced Channel Materials




R. Chau et al, Nature Materials, 2007

2’D Advanced Materials: The possibility for both improved effective mass and reduction of scattering.

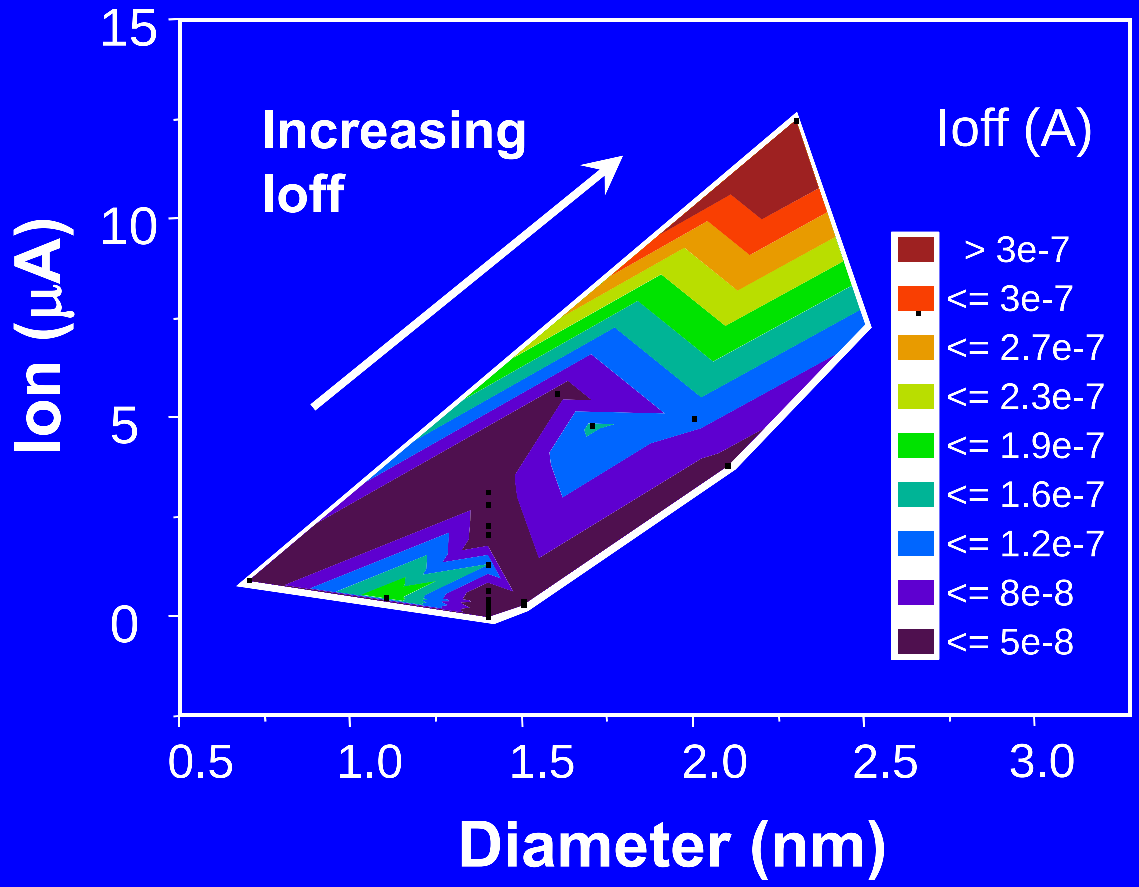
Carbon-based Advanced Channel Materials



Carbon-based materials: A key challenge is that the highest mobility materials have the lowest bandgaps

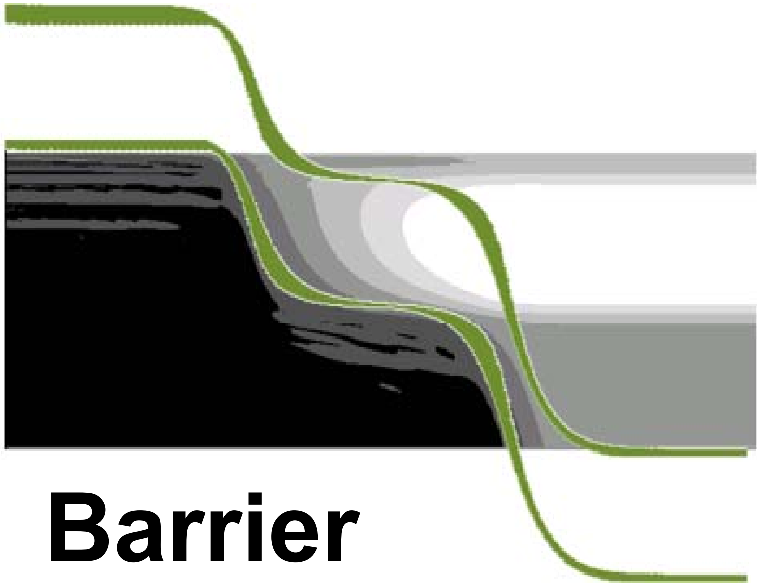
R. Chau et al, Nature Materials, 2007

Carbon-based Advanced Channel Materials

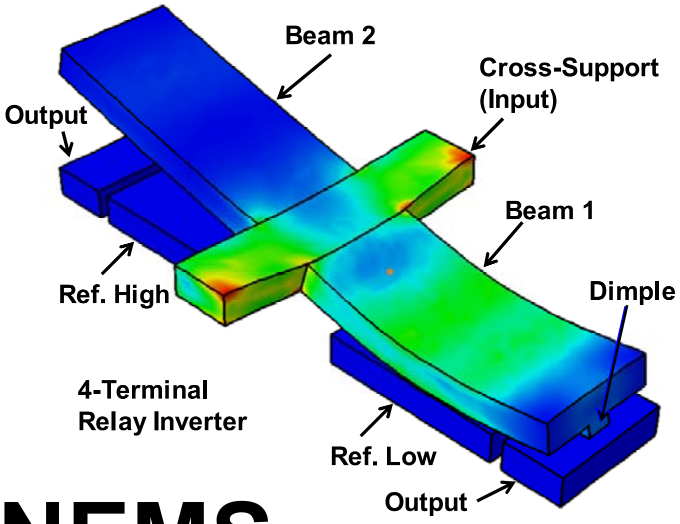


Carbon-based materials: A key challenge is that the highest mobility materials have the highest Ioff

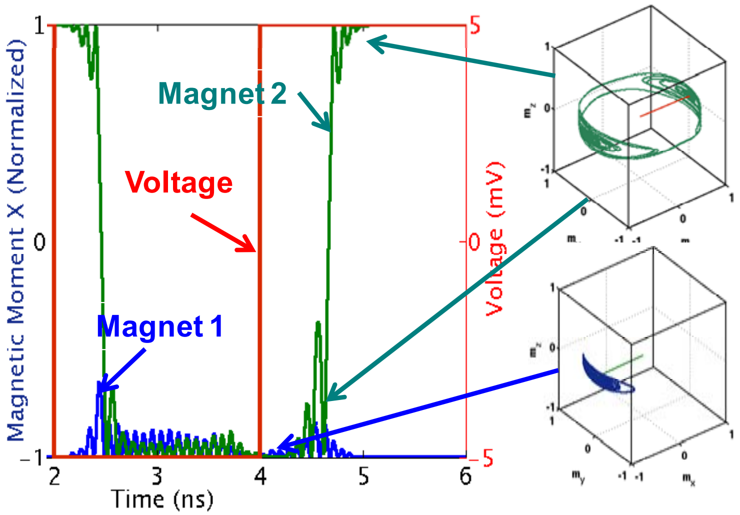
MORE THAN MOORE



Barrier

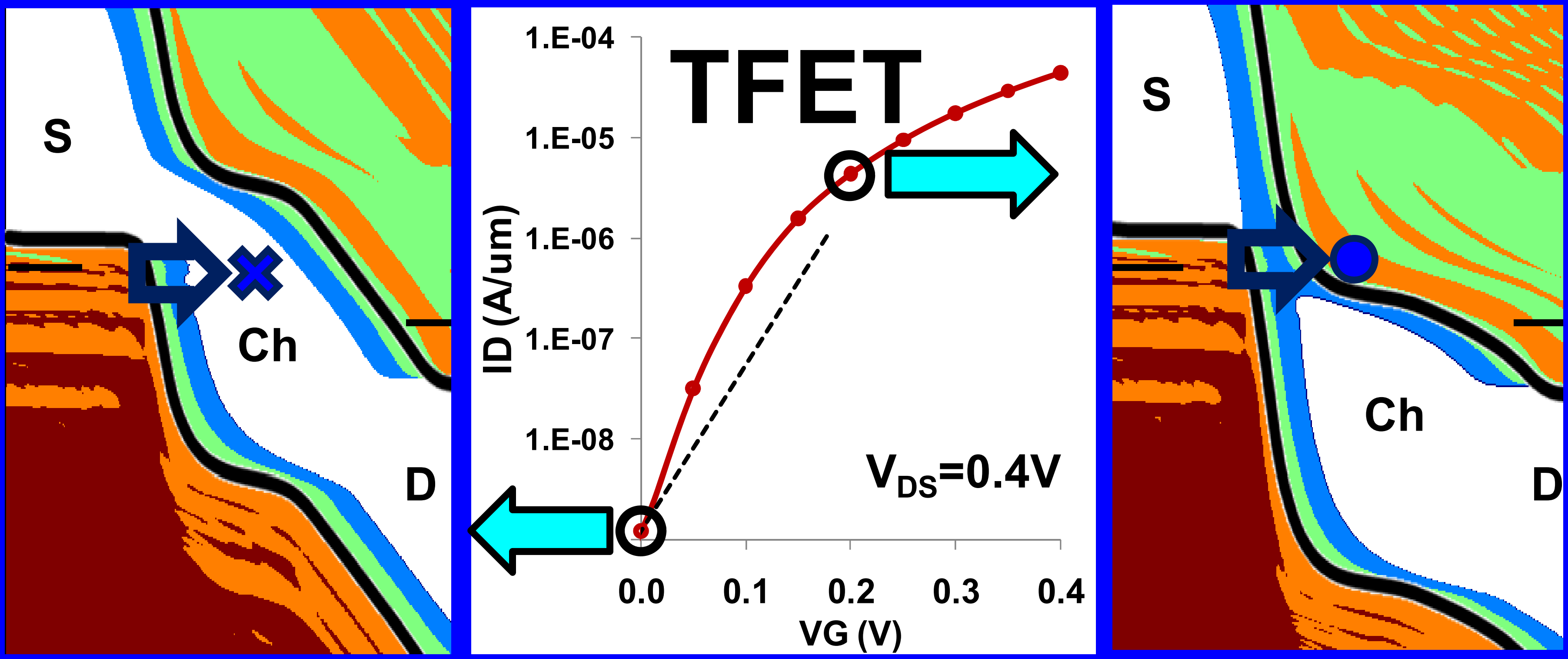


NEMS



Non-charge

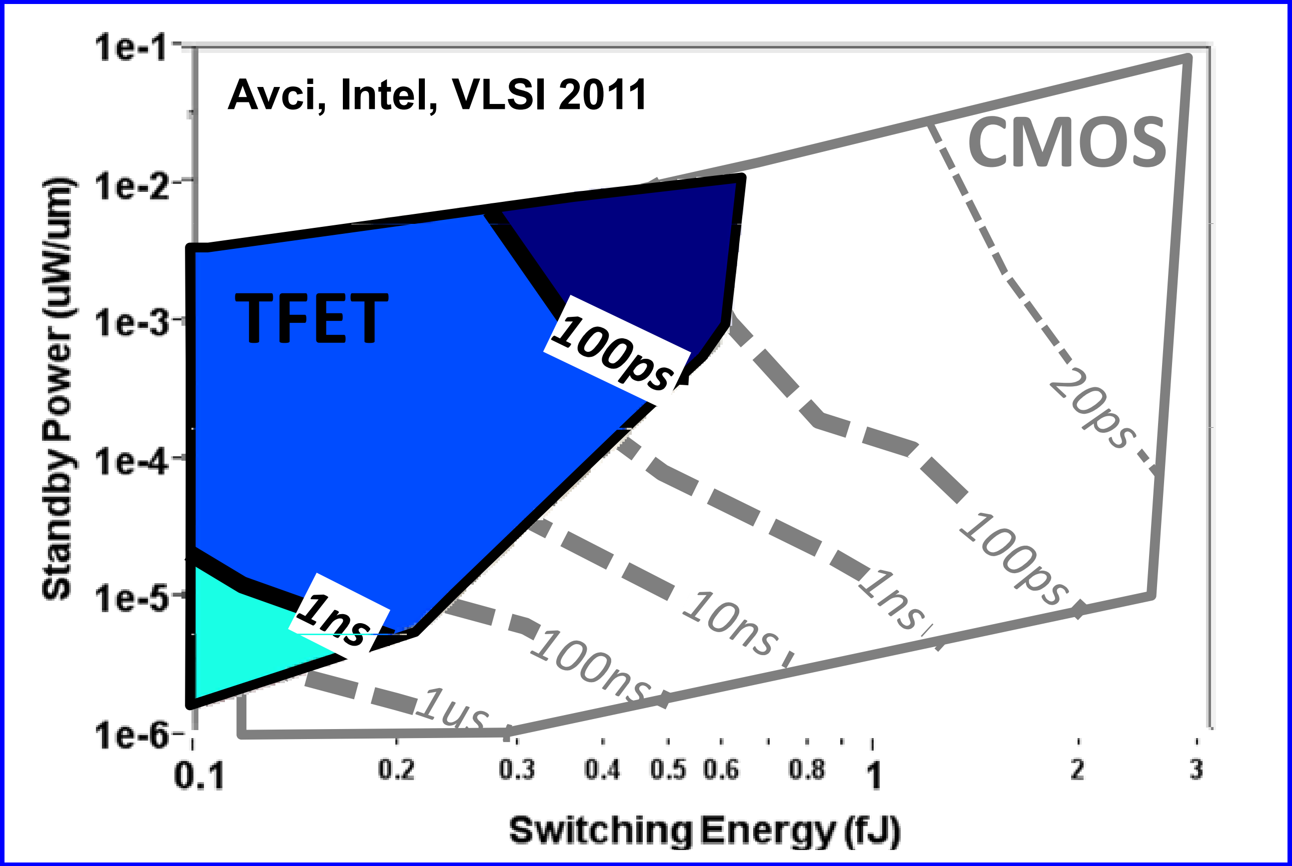
Barrier Engineering (Ex: Tunnel FET)



Avci, Intel, VLSI 2011

Tunnel FETs: Tunnel FETs circumvent the 60mV/dec subthreshold slope limit by tunneling through the S/D barrier

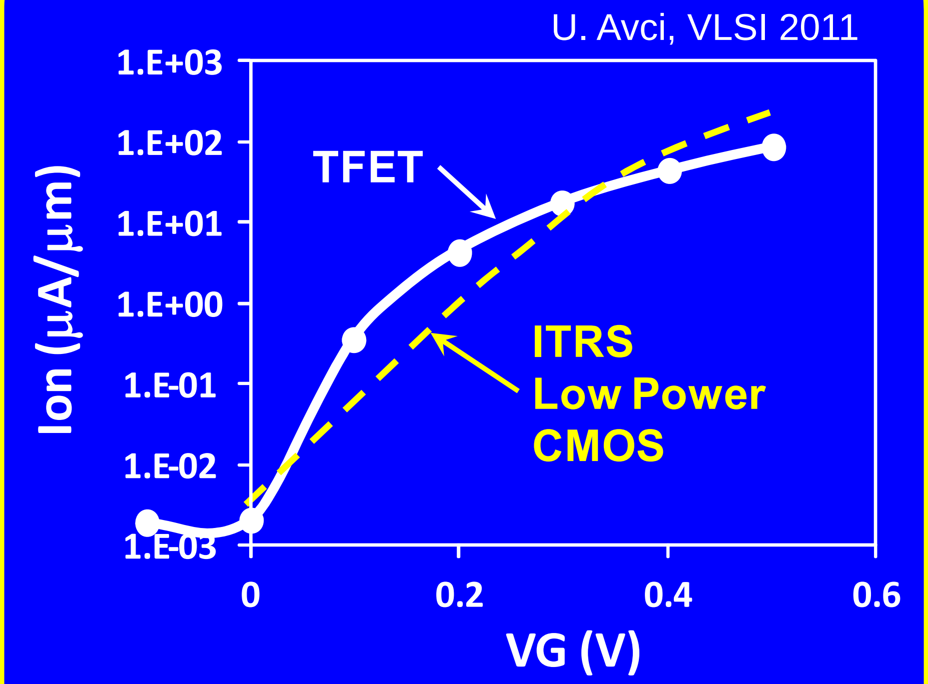
Barrier Engineering (Ex: Tunnel FET)


Avci, Intel, VLSI 2011

Tunnel FETs: At low switching energy,
an InAs TFET is theoretically capable of providing
more than 8x performance advantage over a MOSFET

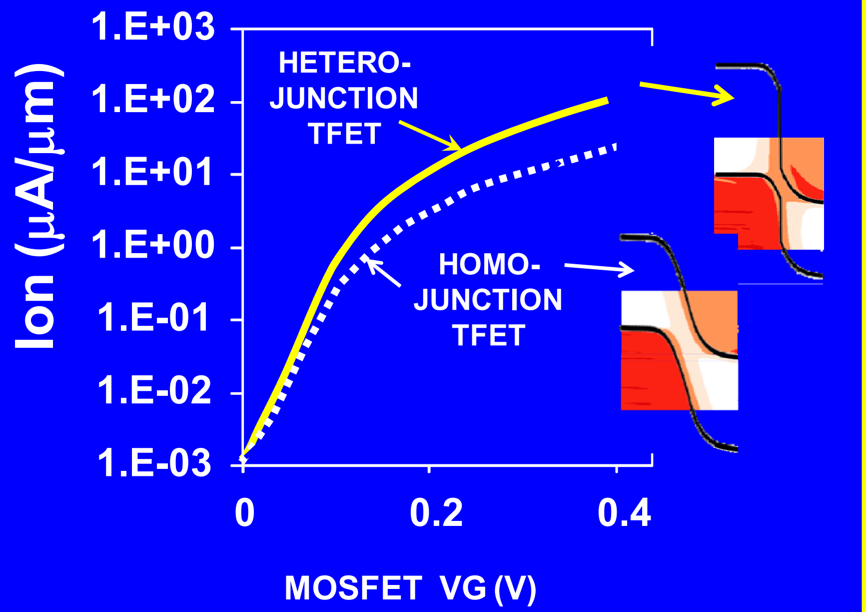
Barrier Engineering (Ex: Tunnel FET)

BENEFITS

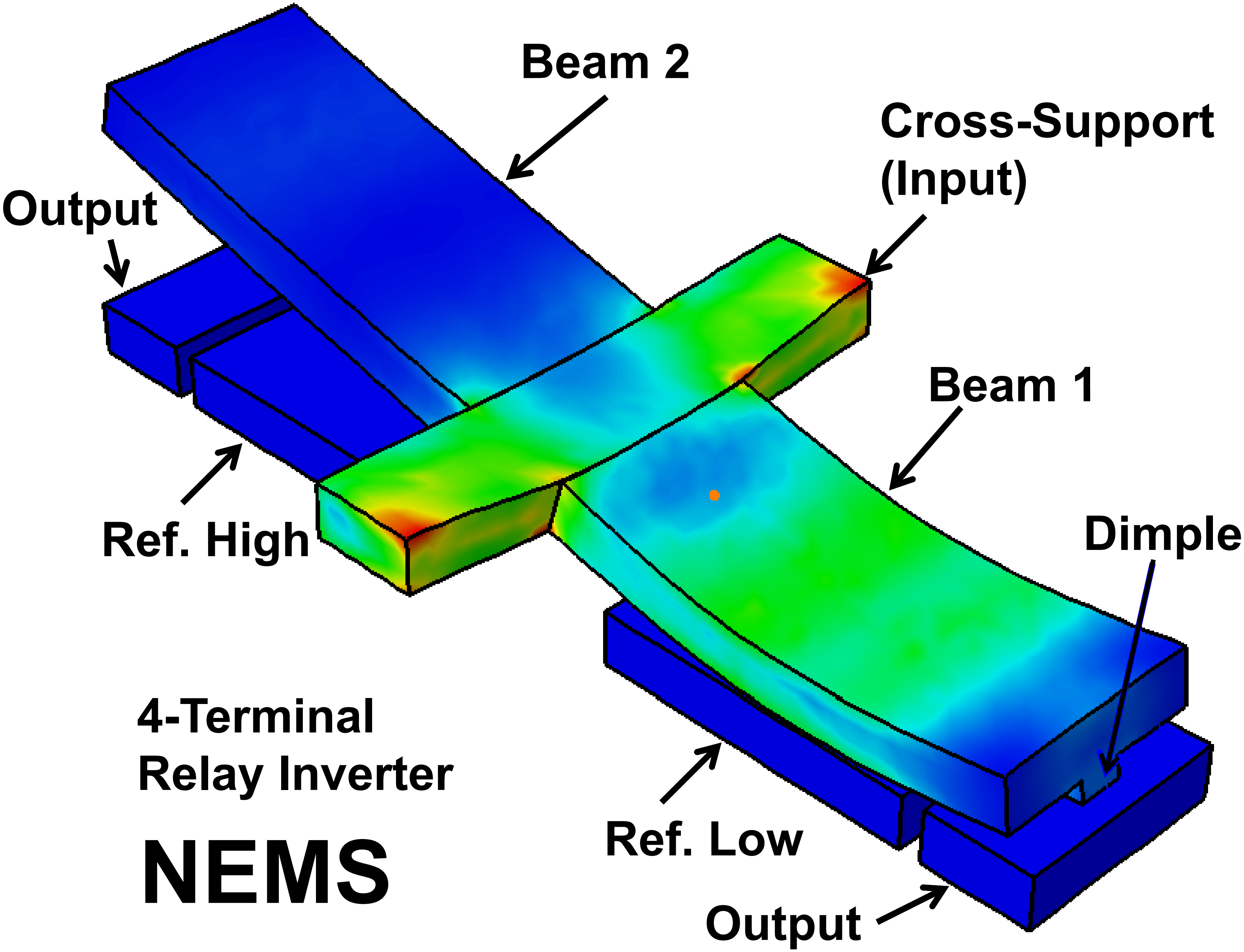


Better sub-threshold slope:
Tunneling through the barrier

CHALLENGES



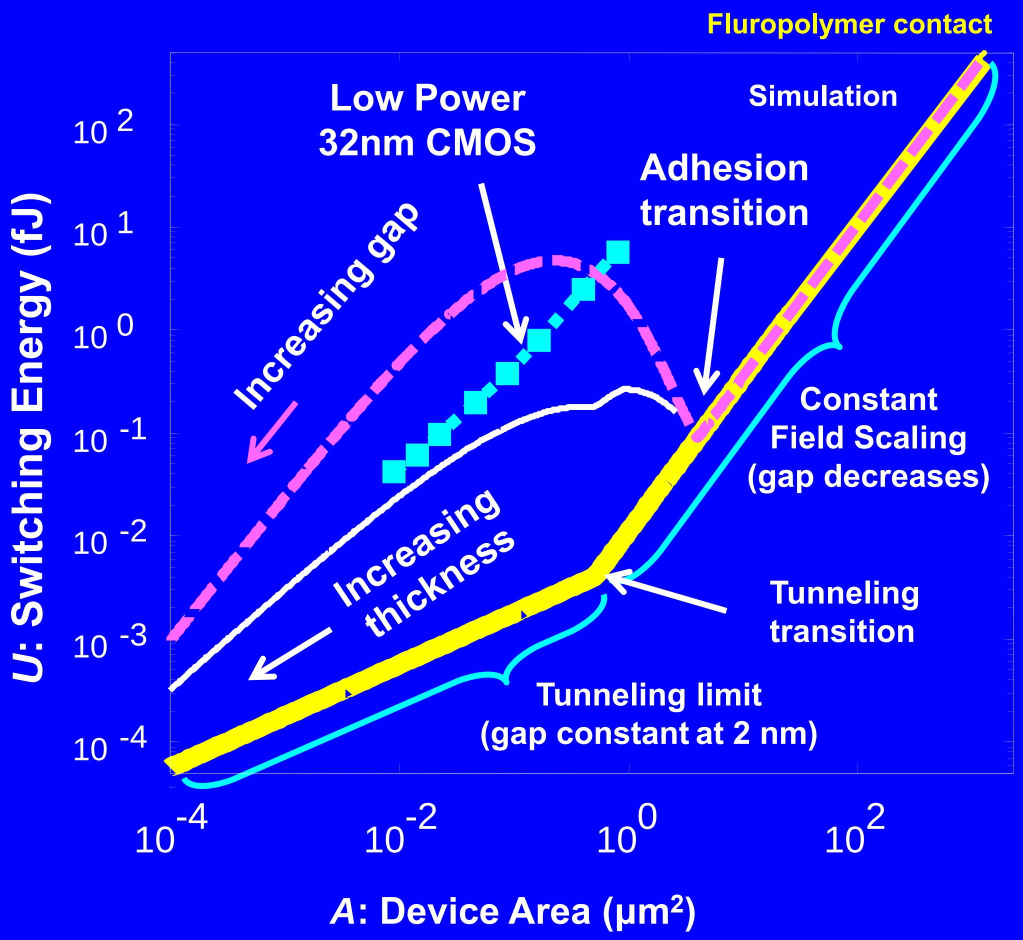
Requires offset bandedges:
Exotic heterostructures

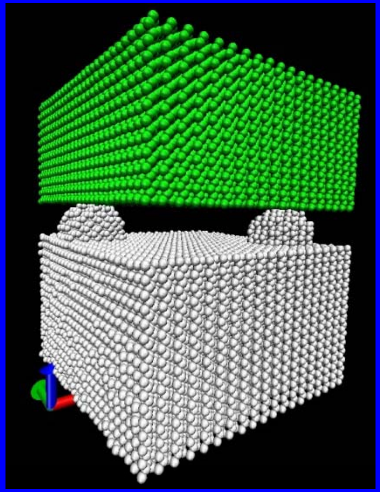


4-Terminal
Relay Inverter

NEMS

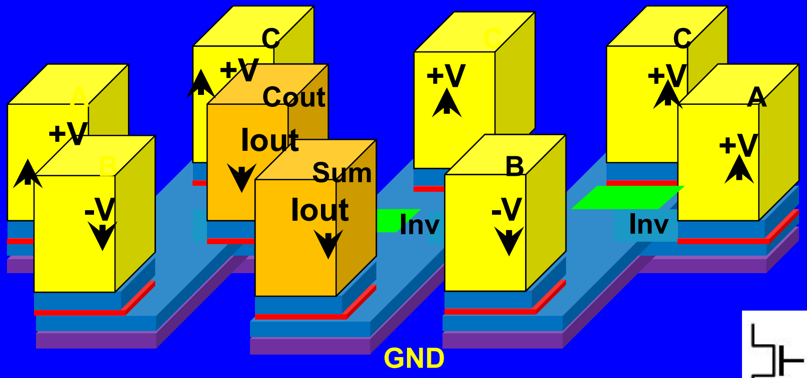
Nano-mechanical Devices



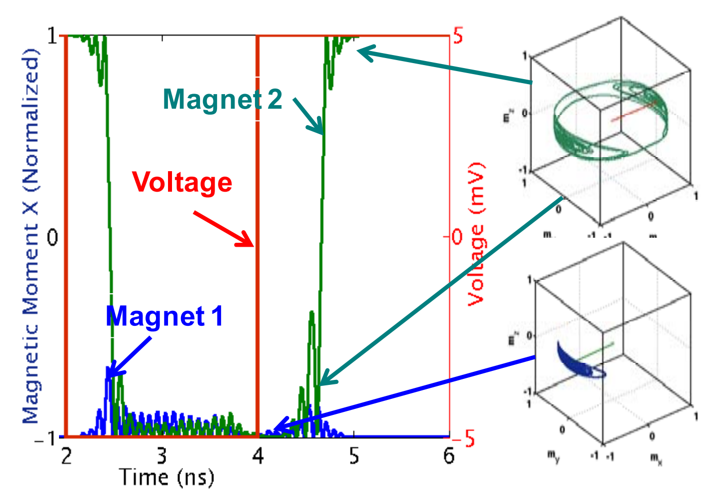


NEMS: The possibility of lower power operation than CMOS but face adhesion challenges at small dimensions

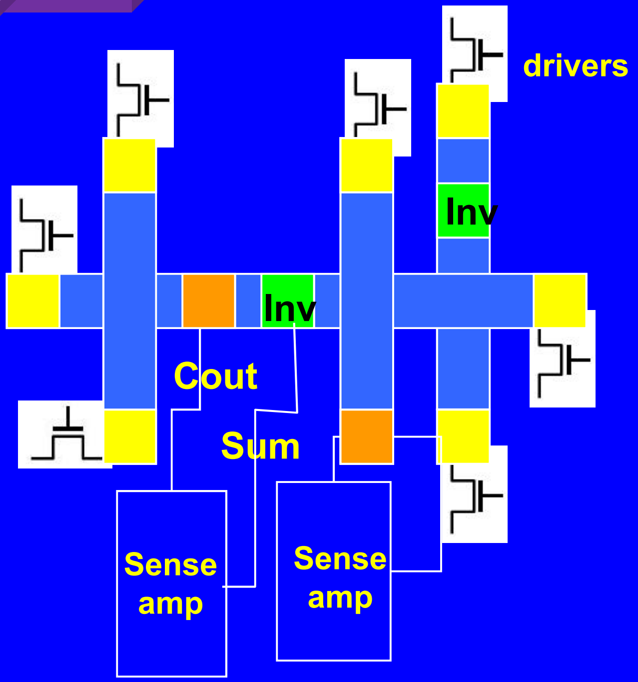
Spin-Torque Logic Devices



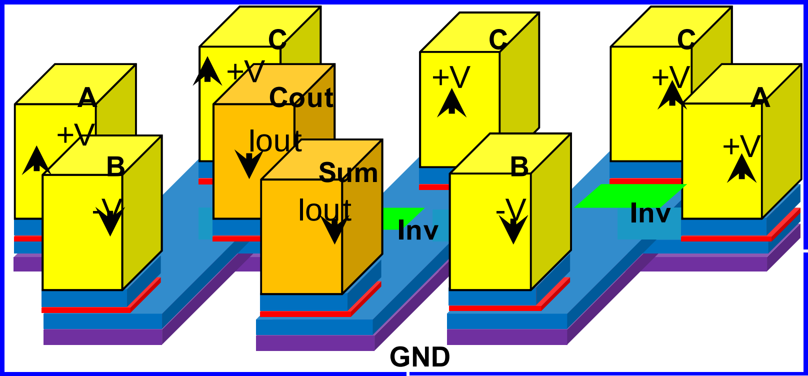
3 STMGs
7 driver transistors



S. Manipatruni et al., http://arxiv.org/abs/1112.2746, 2011



Spin Torque Logic: The orientation of the spin of the electron is used to carry information.

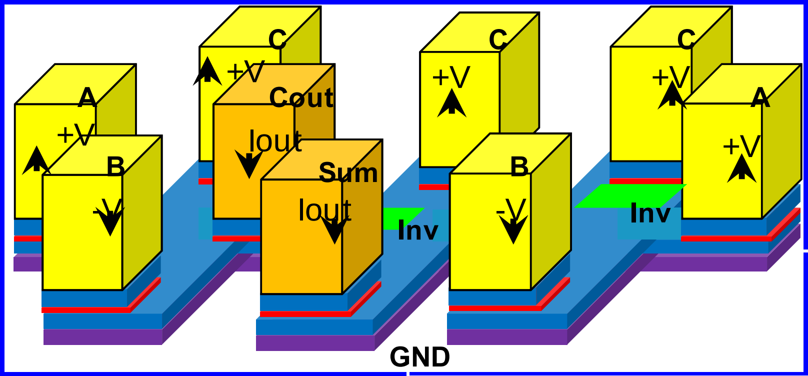


Spin-Torque Devices BENEFITS

	CMOS	STMG	MTJ+CMOS
Area/gate (um^2)	5.0	**1.3**	4.9
Switching time (pS)	16	2826	1.25
Power/gate active (μW)	70.6	**45.6**	163.0
Power/gate standby (μW)	0.81	**0**	0
Throughput/area Mops/nS/cm^2	79.4	13.4	10.2
Non-volatile	No	**Yes**	Yes

D. E. Nikonov et al., Intermag Tech. Digest, BT-08, 2012.

Spin-Torque Devices CHALLENGES



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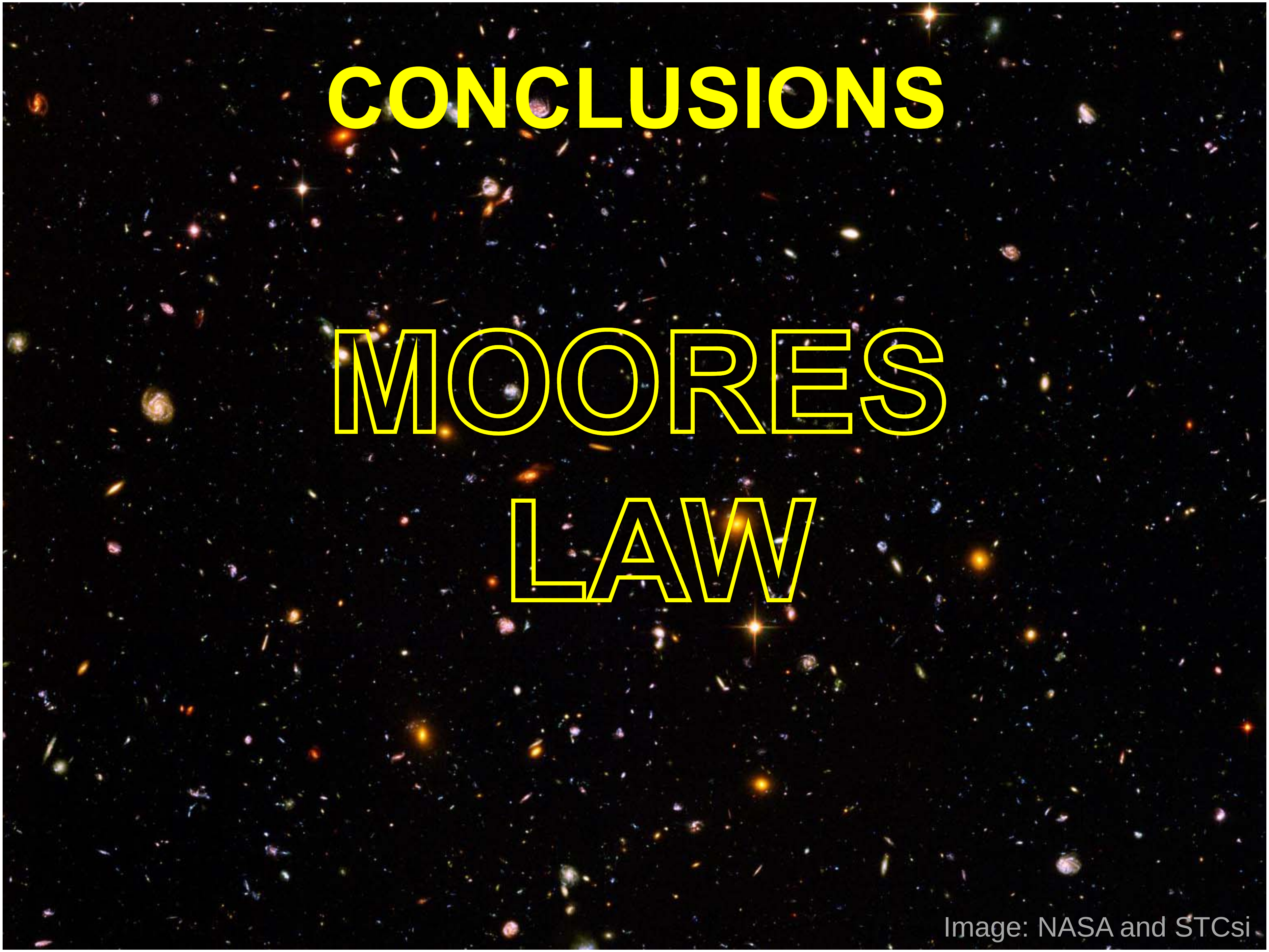
Throughput/area Mops/nS/cm^2	79.4	**13.4**	10.2
Non-volatile	No	Yes	Yes

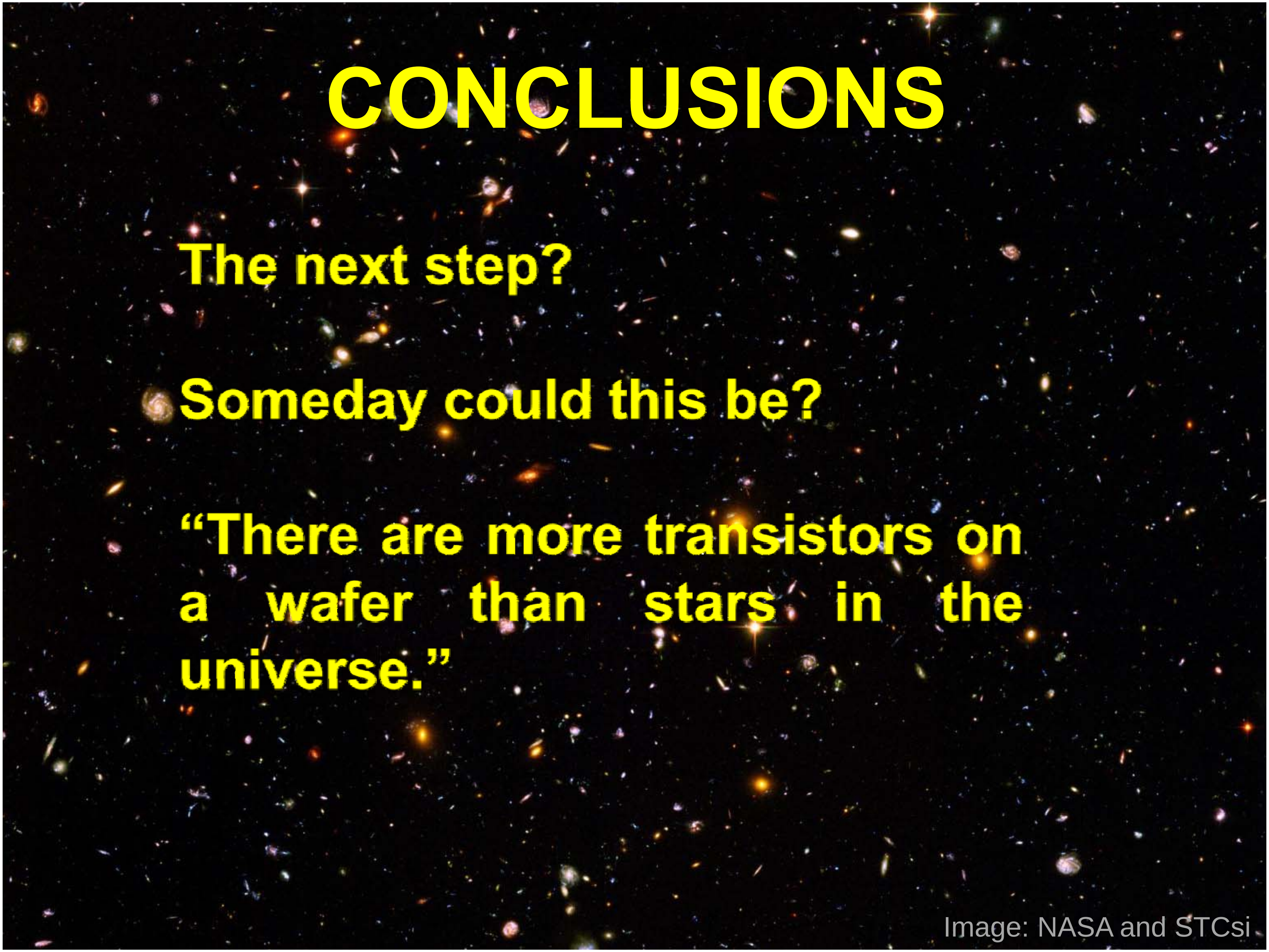
D. E. Nikonov et al., Intermag Tech. Digest, BT-08, 2012.

CONCLUSIONS



MOORES
LAW

Image: NASA and STCsi



CONCLUSIONS

The next step?

Someday could this be?

“There are more transistors on a wafer than stars in the universe.”

Image: NASA and STCsi

Q&A