

The logo for the Intel Developer Forum 2011. The text "IDF2011" is rendered in a large, white, sans-serif font with a glowing effect. A starburst graphic, composed of multiple thin lines radiating from a central point, is positioned behind the final "1" of "2011".

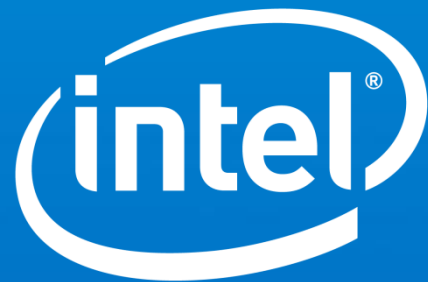
**IDF2011**

**INTEL DEVELOPER FORUM**

AHEAD OF THE CURVE  
STRAIGHT TO THE FUTURE

IDF2011

INTEL DEVELOPER FORUM



Sponsors of Tomorrow.™



# JUSTIN R. RATTNER

Vice President

Director, Intel Labs and  
Intel Chief Technology Officer

Intel Senior Fellow

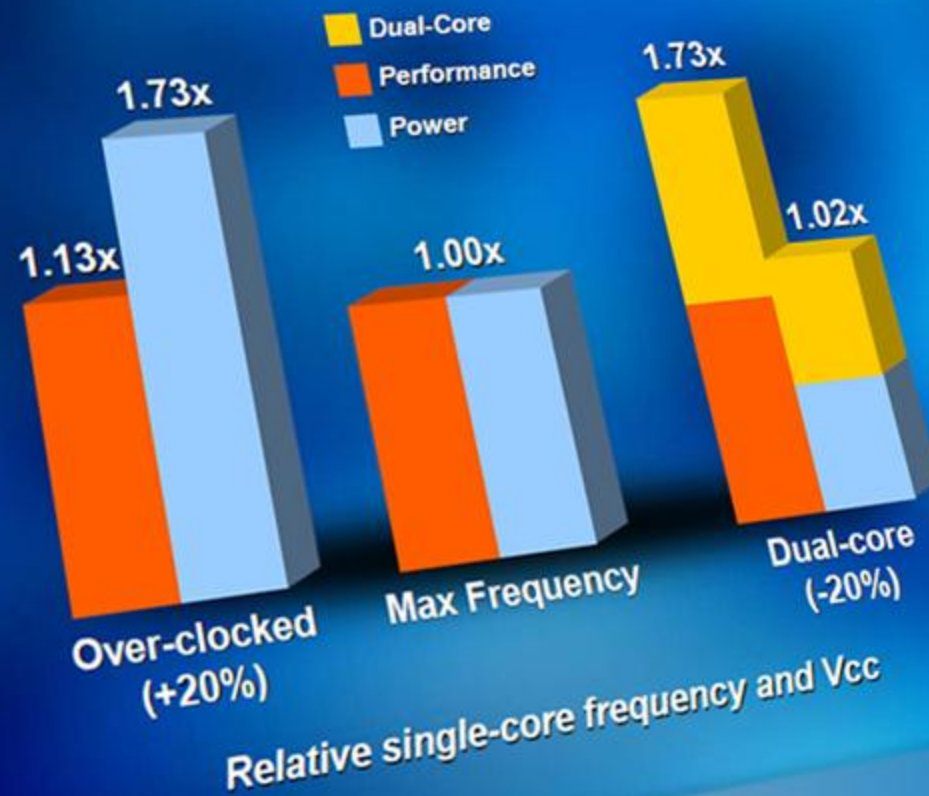


# *THE FUTURE: ACCELERATED*

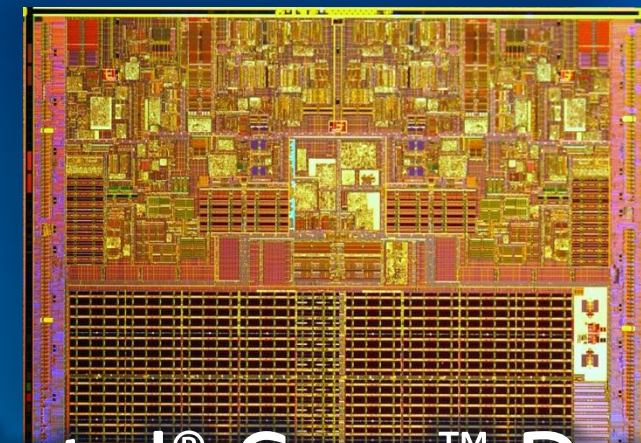
**IDF2011**  
INTEL DEVELOPER FORUM

Sponsors of Tomorrow. 

## Multi-Core Energy-Efficient Performance



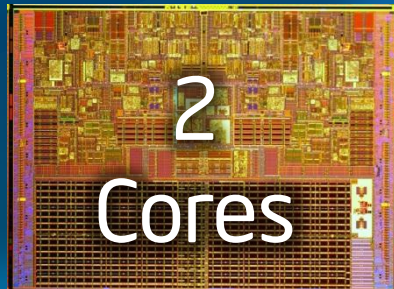
*The Motivation for Moving  
Beyond a Single Core*  
**5 YEARS AGO**



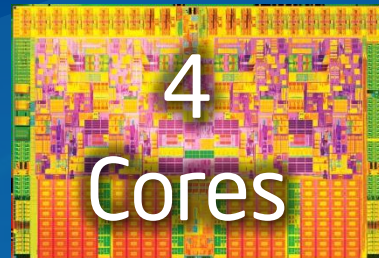
Intel® Core™ Duo

# We've Come a LONG WAY IN FIVE YEARS

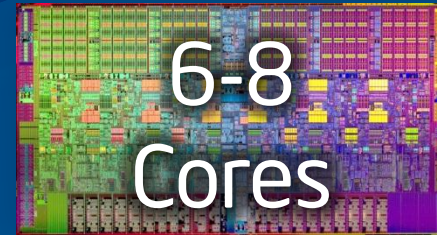
2006



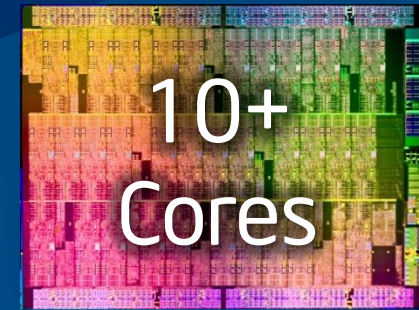
2007



2010



2011+

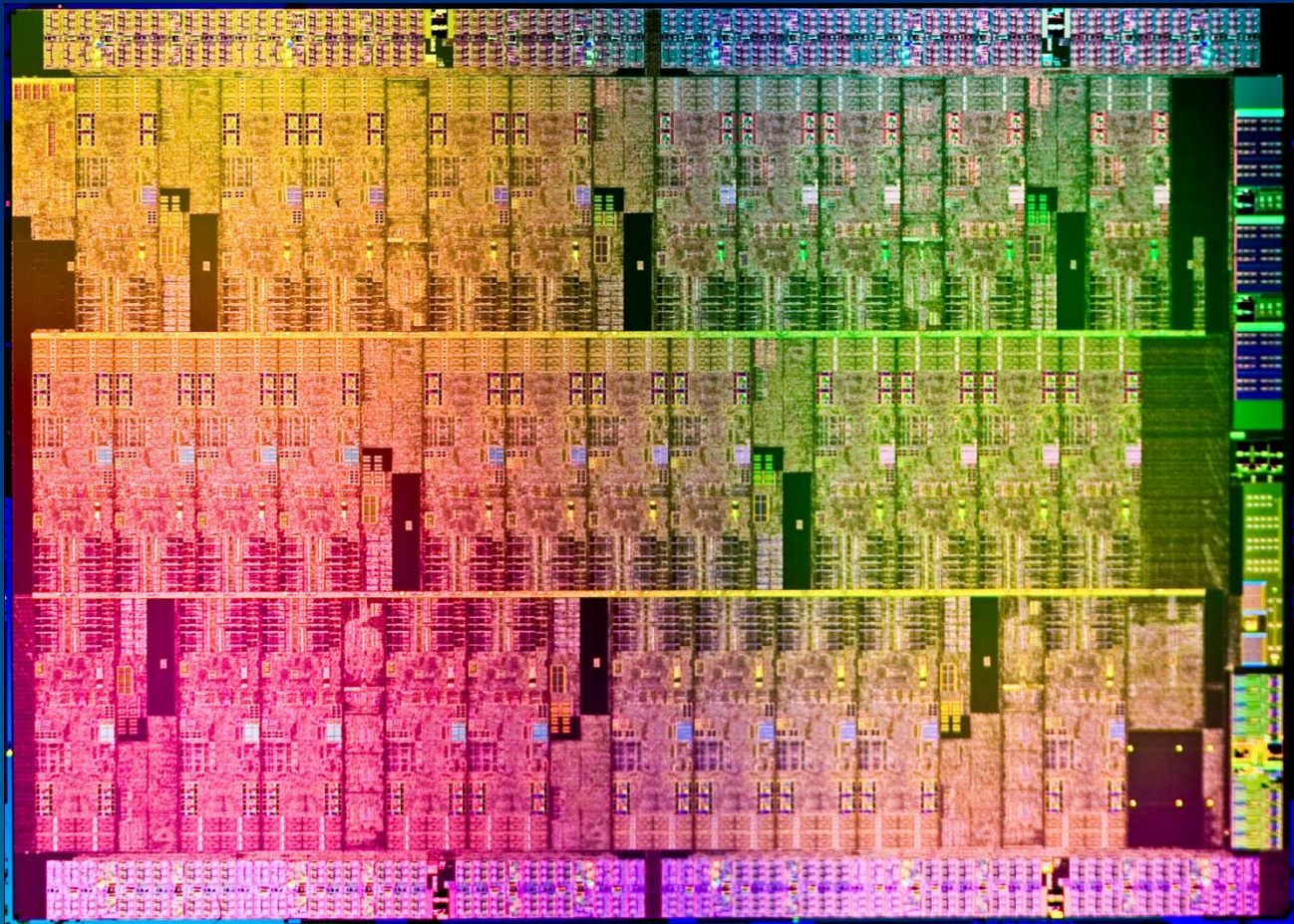


## The Evolution of Multi-core and Many-core Computing

# Industry's First General Purpose Many Core Architecture

## *Intel® Many Integrated Core (Intel® MIC) Architecture*

Knights Ferry Software Development Platform



### Processing Highly Parallel Workloads

- Utilizes many small, low-power IA cores
- Supports many, many more threads

### Programmability and Scalability

- Benefits from standard IA programming and memory model

### Production Systems Coming Soon

- Knights Corner to launch on 22nm with >50 cores to provide outstanding performance for HPC users

# Terascale: Intel's Many-core Research Program

## Compute Intensive Applications

Virtual Environments



Educational Simulation



Financial Modeling



Media Search & Manipulation



Web Mining Bots



## Thread Aware Execution Environment

### Scalable Architectures

e.g. 48-core Single-Chip Cloud Computer

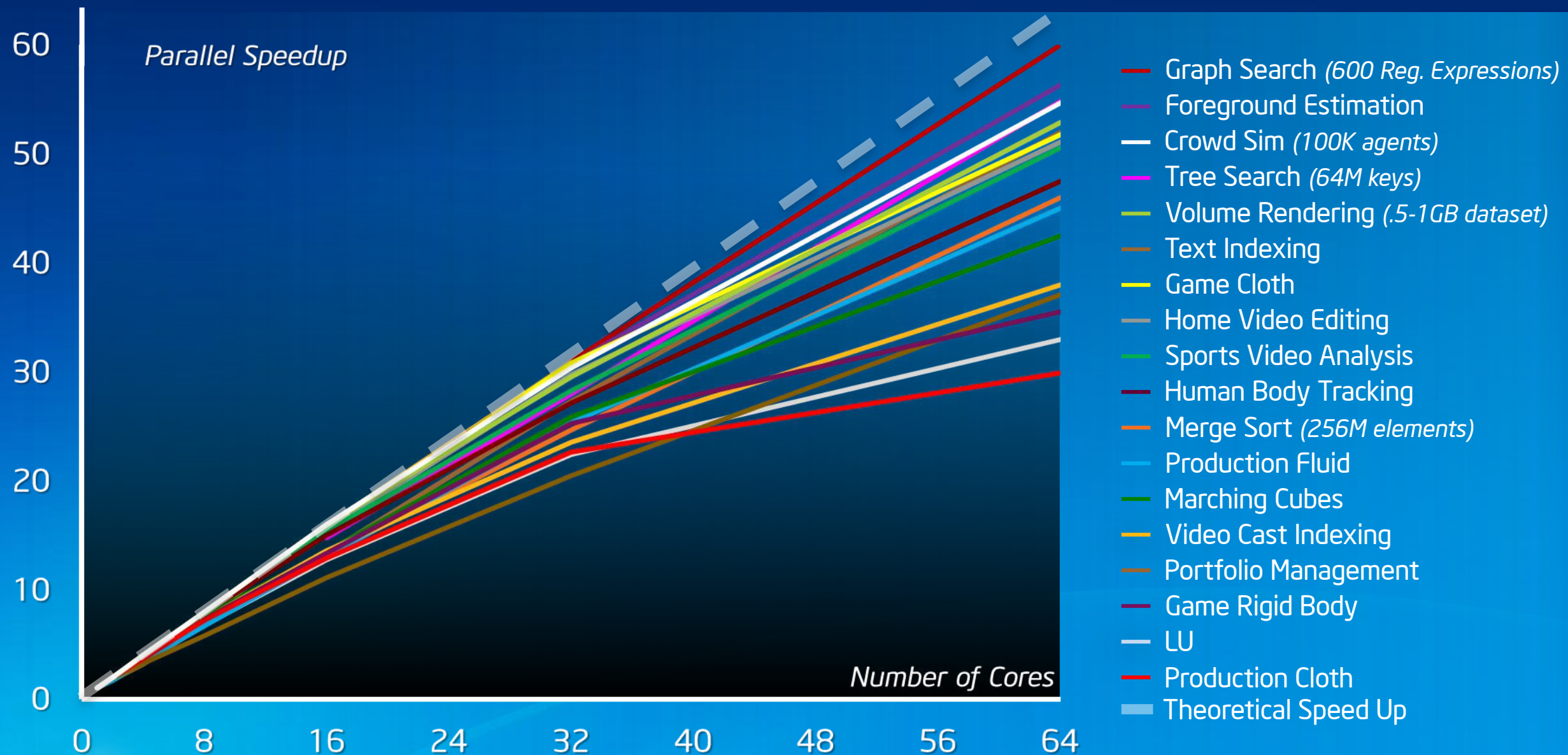
Stacked,  
Shared Memory

High Bandwidth  
and Low-Latency  
Communications

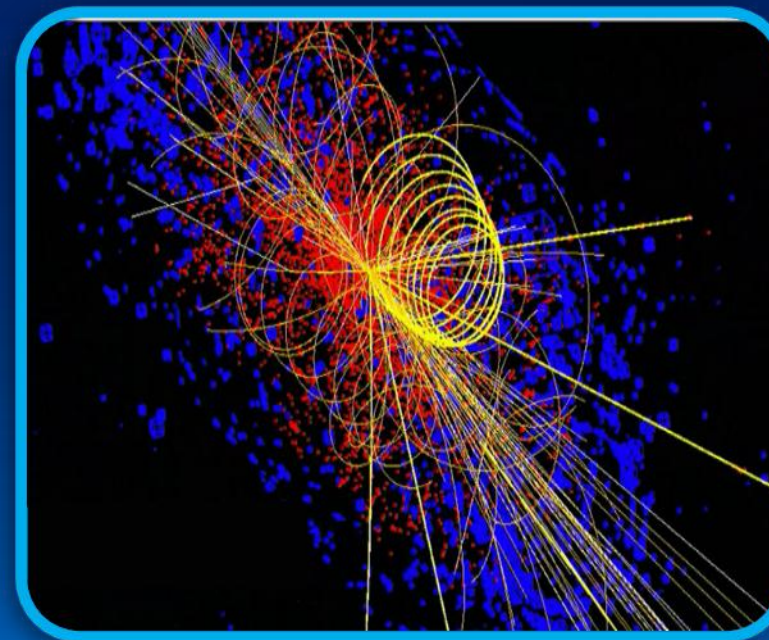
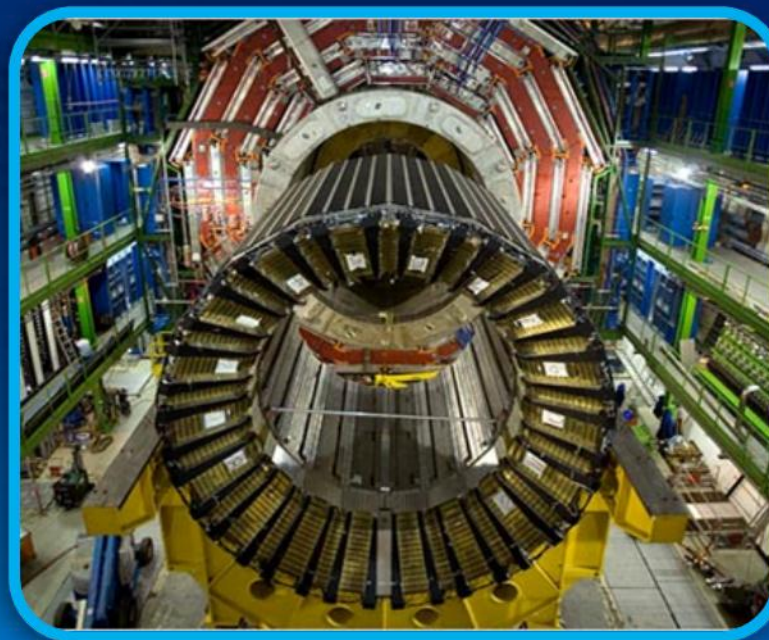


# Excellent Scaling Across Broad Range Of Applications

*Constantly evaluating options for all workloads*



Welcome!



**Andrzej Nowak**  
*CERN openlab*

# *CERN's Particle Accelerator* **Large Hadron Collider**

## Large Hadron Collider

- 27 km in circumference
- 100 m underground
- Operates at 1.9° Kelvin

It has now been up and running since  
November 2009

40 million collisions per second, resulting in  
15 – 25 Petabytes of data per year

# Data Handling and Computation for Physics Analysis

## High Level Trigger

Online trigger and filtering

## Simulation

Event Simulation

## Reconstruction

Selection & Reconstruction

Event Reprocessing

Raw Data

## Analysis

10% Event Summary

Processed Data

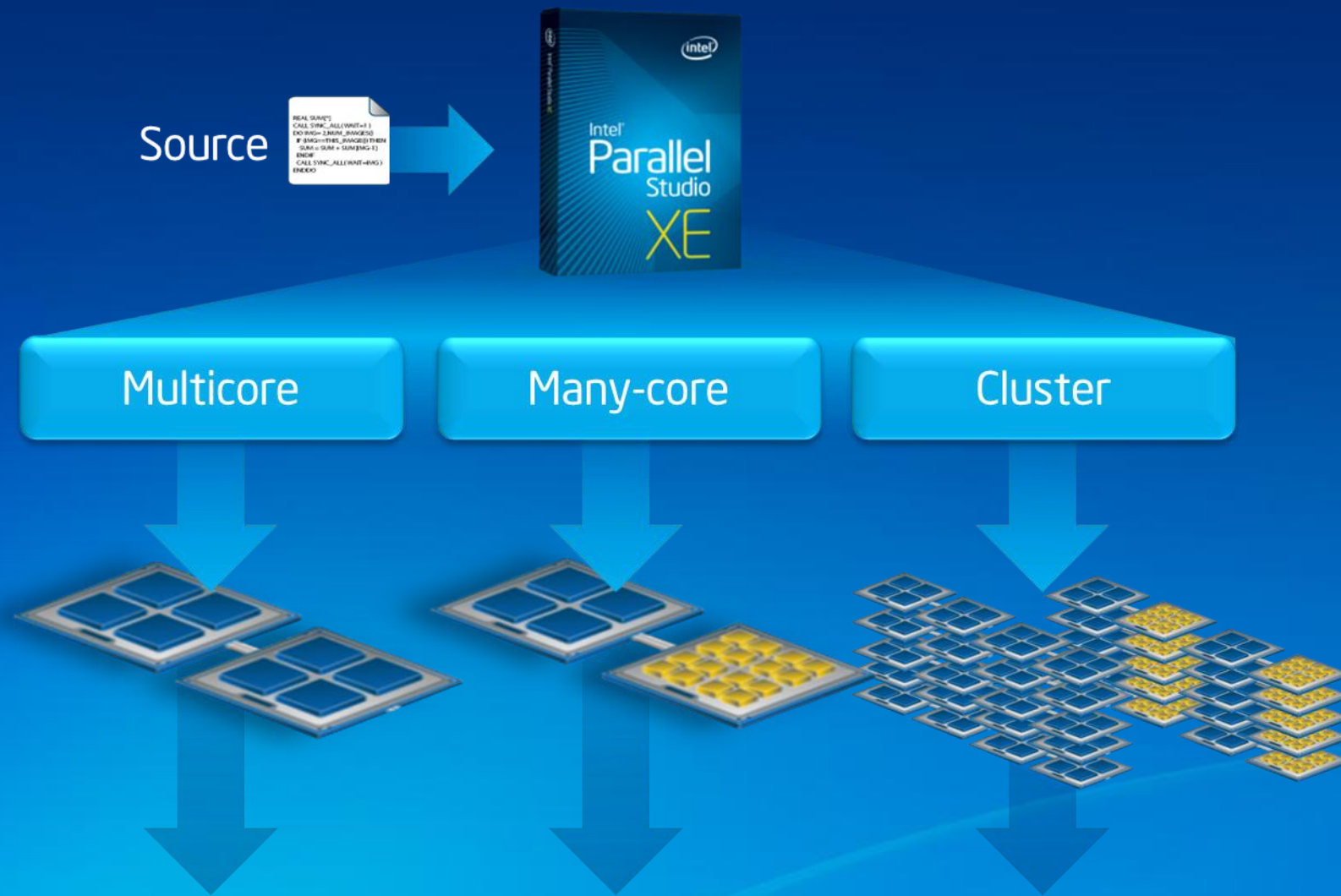
Batch Physics Analysis

Interactive Physics Analysis

1% Analysis Objects  
(extracted by physics topic)

# Intel® MIC Architecture Programming

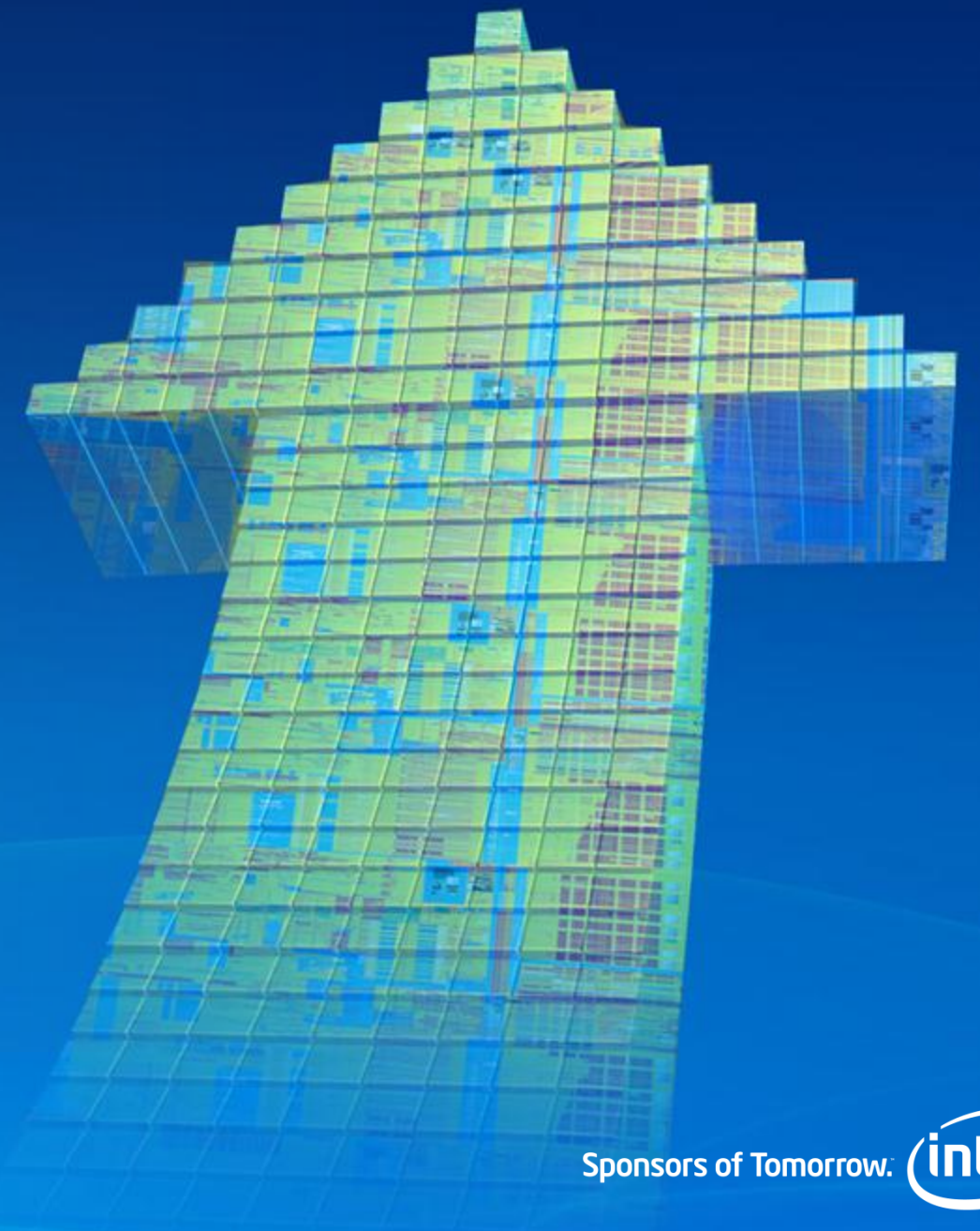
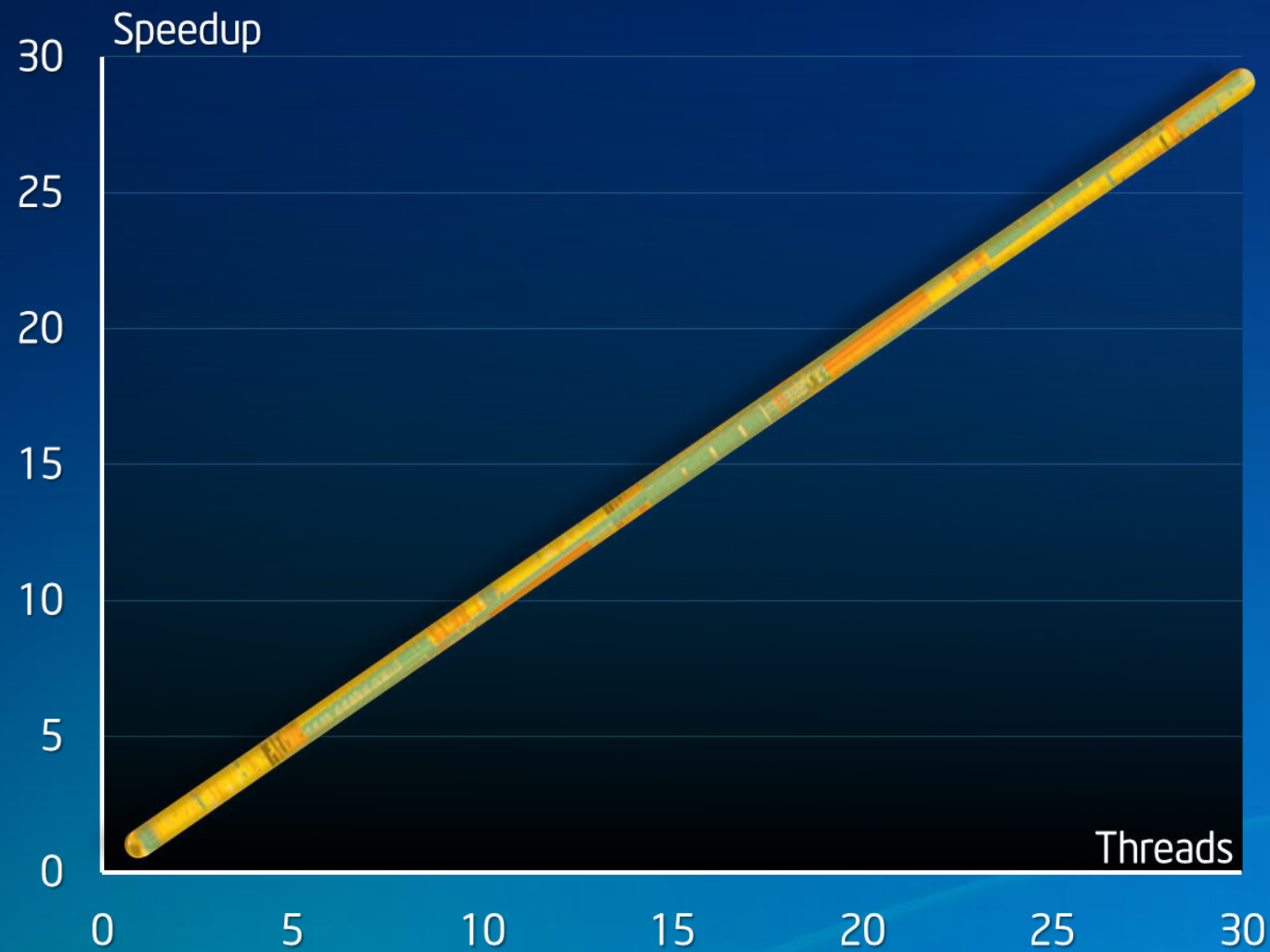
*Eliminates need for multiple programming models*



## Common with Intel® Xeon® Processors

- Languages
- C, C++, Fortran compilers
- Intel developer tools and libraries
- Coding and optimization techniques
- Ecosystem support

# Scalability of CERN Trackfitter Workload on MIC



# Yet There Has Been Quite a Lot of Angst about Multi- and Many-core

"Faster Chips Are Leaving  
Programmers in Their Dust"

*December 16, 2007*

**The New York Times**

"Multicore Chips Pose  
Challenge for In"

*March 20, 2008*

**PCWorld**

"Wall ahead in  
multicore programming"

*May 3, 2011*

**EE|Times**

bits Snag: Tiny  
Outsize Power"

*st 1, 2011*

**York Times**

"Ni  
The Parallel Programming Crisis"

*March 1, 2008*

**Rebel Science News**

*Do you have to be a*  
**NINJA PROGRAMMER**

*to actually write multi- and many-core applications?*



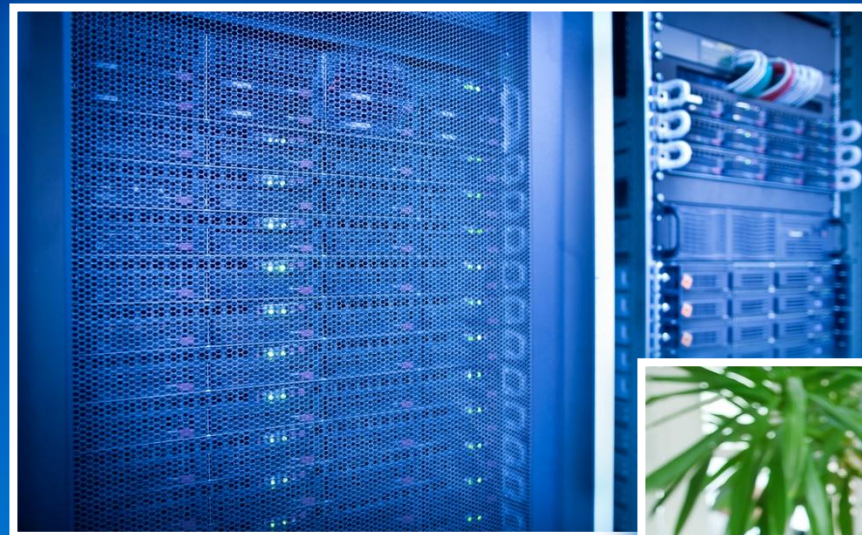


# The Growing Diversity of **MULTI- AND MANY- CORE COMPUTING**

*PC Security*



*Mega Data Center*



*Wireless Comms*



*Web Apps*

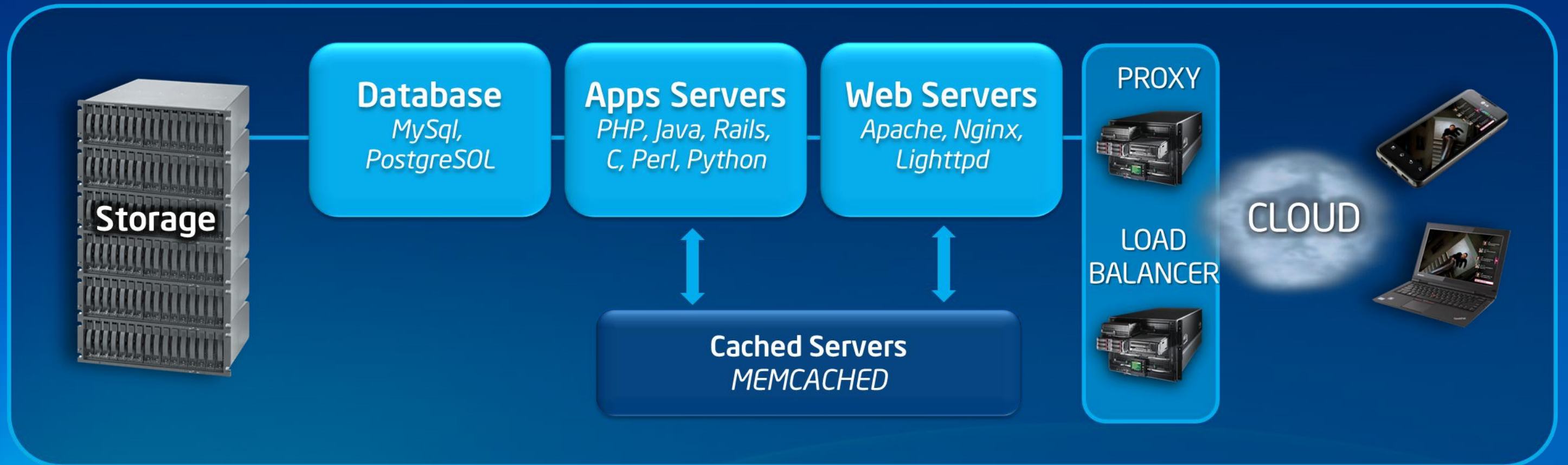




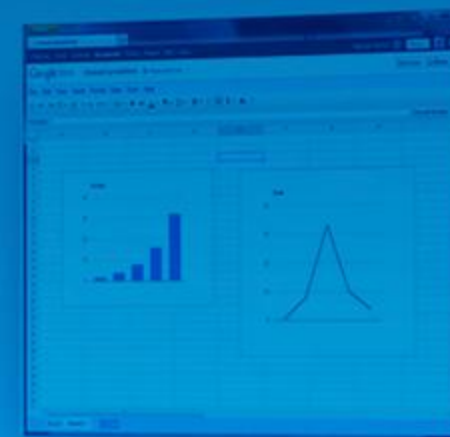
*Improving the Access of Large-Scale,*  
**CONTENT IN THE CLOUD**

# Memory Caching in the Cloud with Memcached

*A high-performance, open source, distributed memory object caching system*



# Bringing the Power of Multi-core to **WEB APPS**



# We Believe in an Open Web

And we're dedicated to keeping it that way.

## Firefox

Now with a new look, su  
awesomeness than ever!

Get Firefox »

Get Firefox on your phone



Firefox

### In the news

New Tools in Mozilla Firefox Help Develop  
Web Forward



# Bringing the Power of Multi-core to **WEB APPS**

**Brendan Eich**  
*CTO Mozilla*

# JavaScript™ : A Cornerstone of Web App Development for Over a Decade

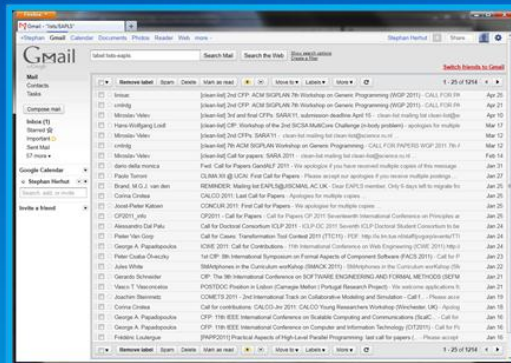
DHTML  
Circa  
1999



- HTML5**
- Storage
  - Multimedia
  - 3D & Effects
  - Device Access
  - Connectivity

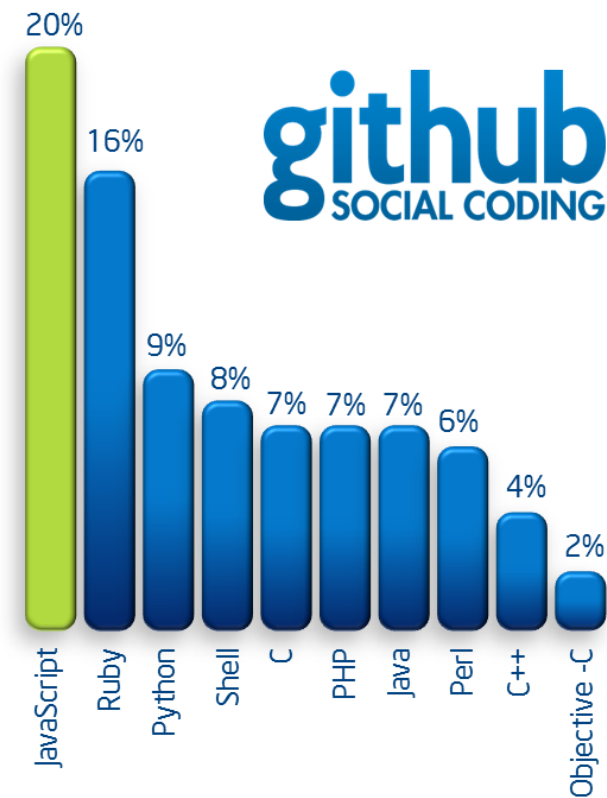
HTML5  
Circa  
2009

AJAX  
Circa  
2003



WebGL  
Circa  
2011

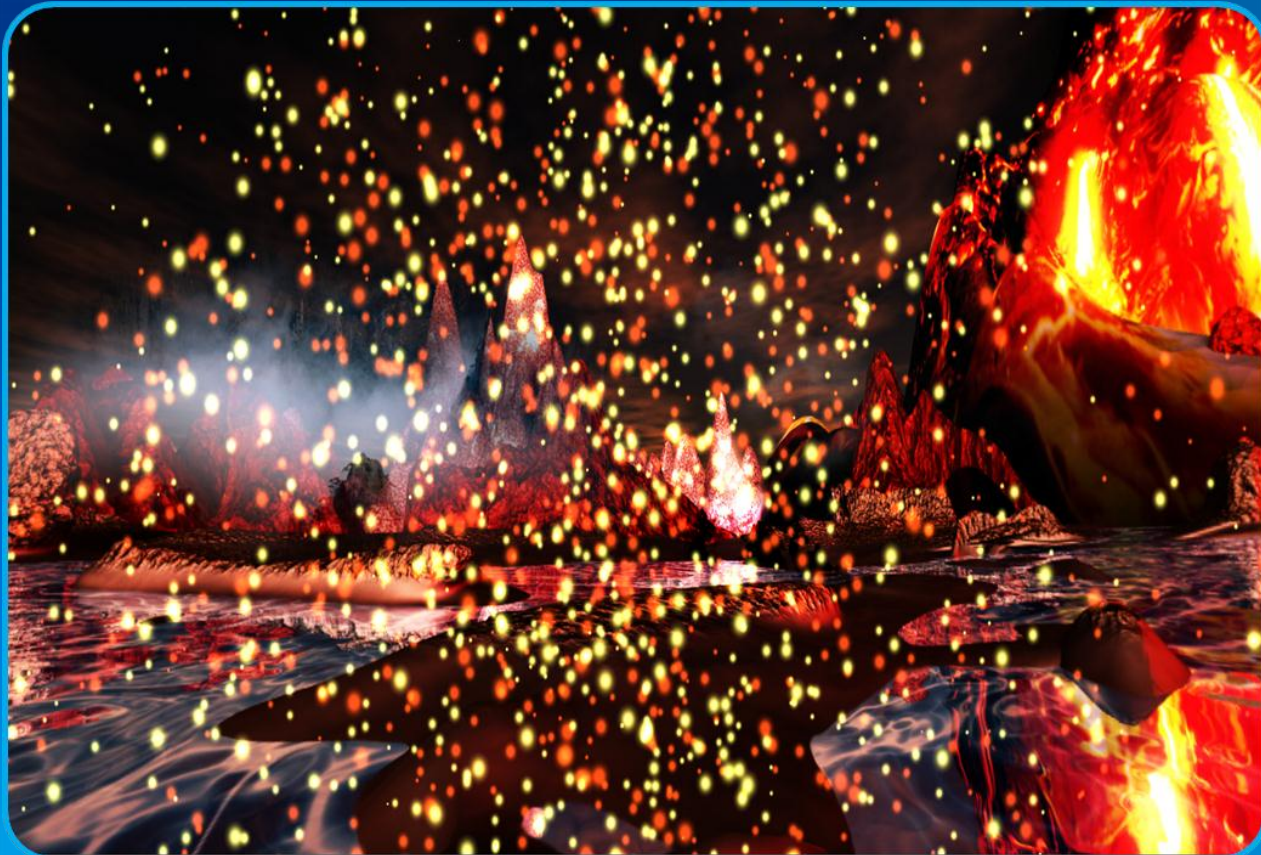
Most popular language on github



*Significant performance potential if JavaScript™ could harness multi-core hardware*

# River Trail: Parallel Extensions for JavaScript™

## 3D NBODY IN FIREFOX



Research software extends JavaScript™ to enable data-parallel processing

- Unlocks SSE/AVX + multi-core to web apps
- Interoperates with HTML5 and WebGL
- Targets applications such as computer vision, cryptography, and 3D games

Open source release on Github  
[github.com/rivertrail](https://github.com/rivertrail)

Can An LTE Base Station  
Be Implemented With  
A Multi-core PC?

**THERE'S AN  
APP FOR THAT!**

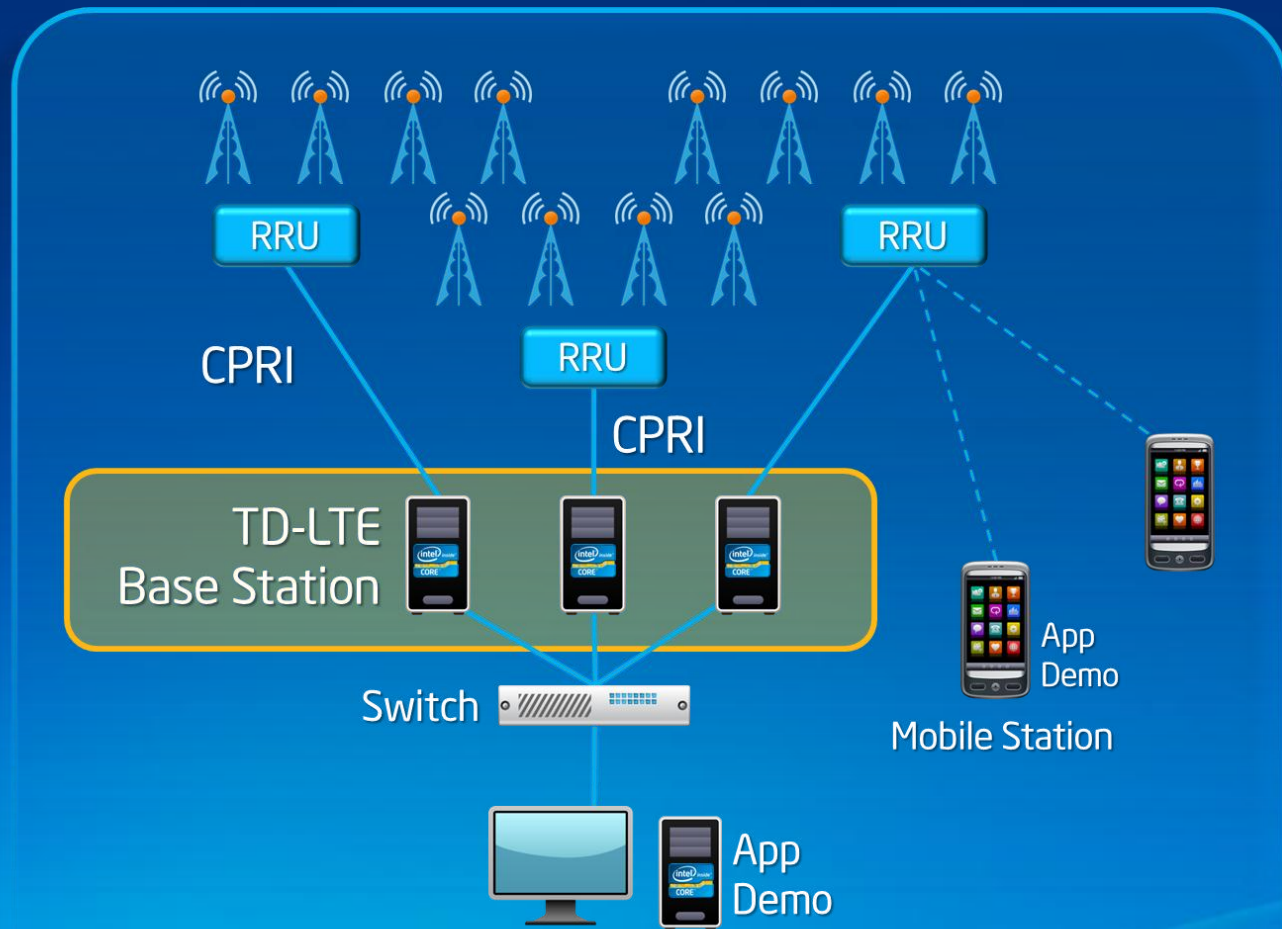




# Cloud Radio Access Network (CRAN)

*A research collaboration between Intel and China Mobile*

## Overall CRAN Architecture



Replacing traditional base station hardware with  
2<sup>nd</sup> Generation Intel® Core™ i7 + Software

## IDF Beijing 2011



Ms. Huang Yuhong  
GM of China Mobile Research Institute

# Prototyping an LTE BASE STATION with Multi-core IA



## Baseband SW

PHY uplink

PHY downlink

Real time RX

Real time TX

Common Public Radio Interface  
(CPRI) Emulator Driver

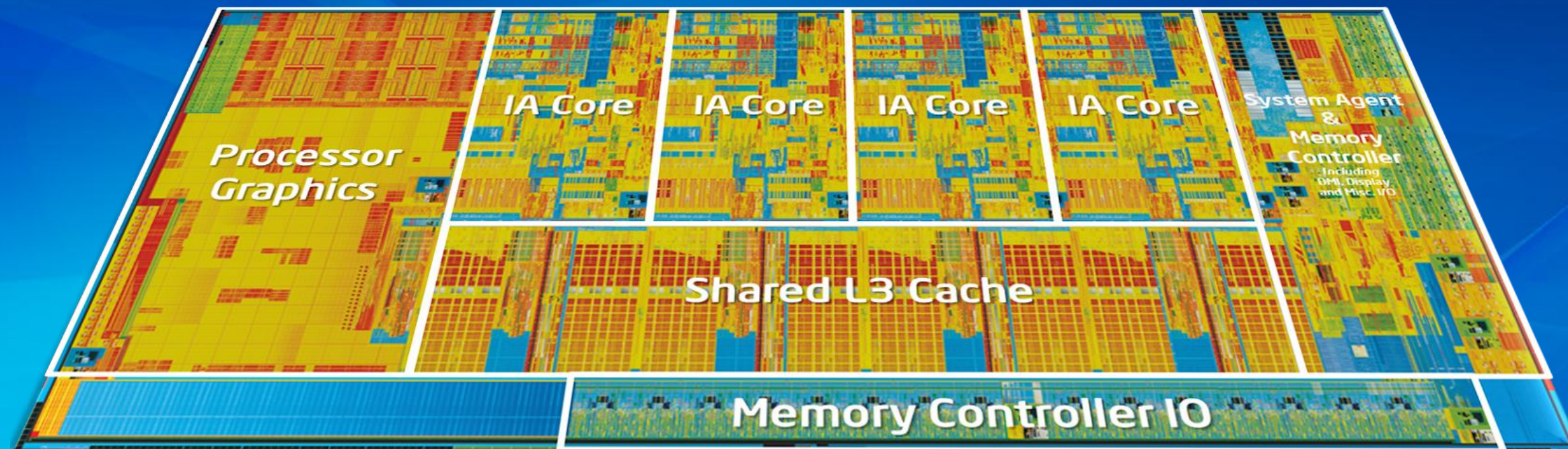
Operating System  
Linux + Real time patch

2nd Generation Intel® Core™ i7  
Quad-Core Platform



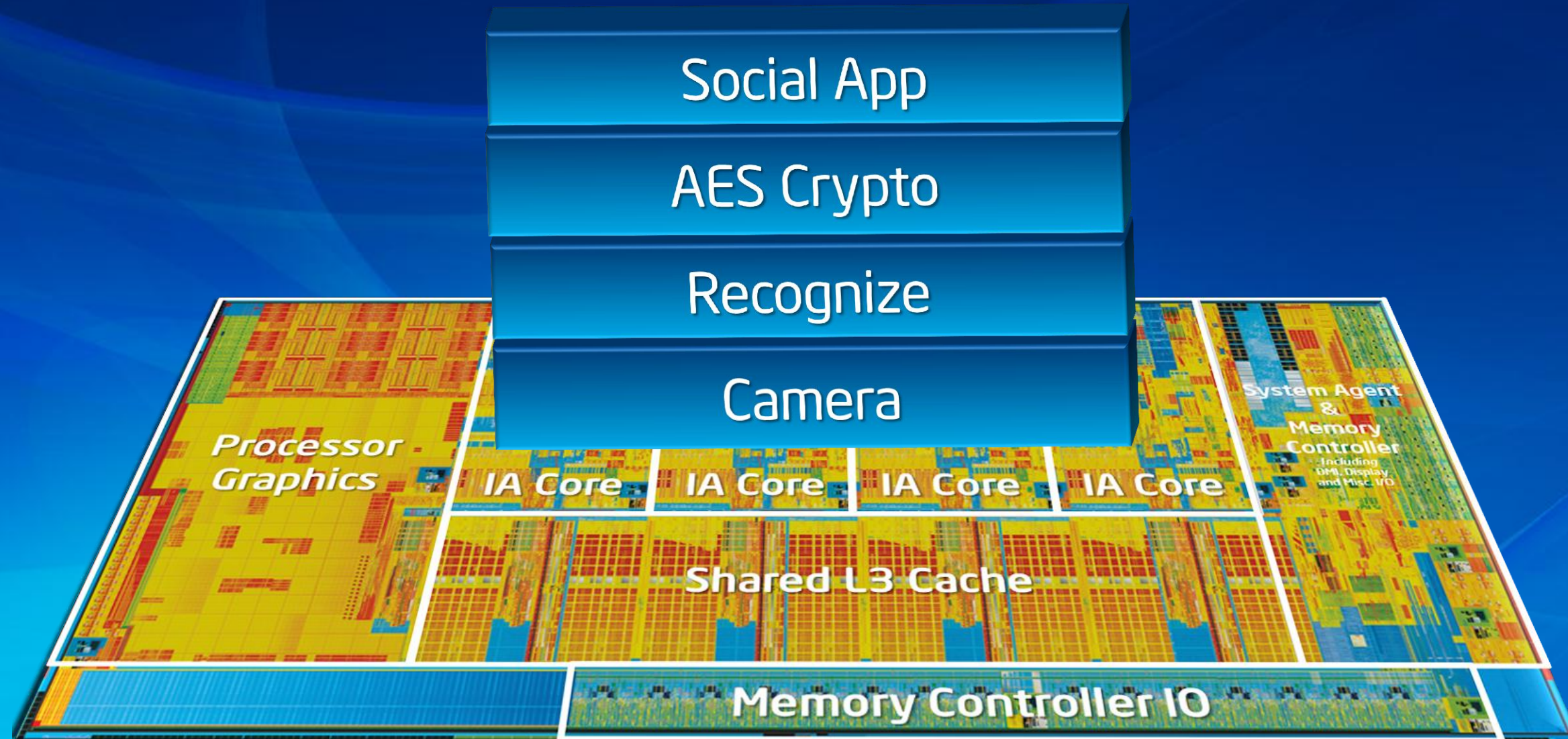
# *IMPROVING SECURITY ON THE* **PERSONAL COMPUTER**

# Enhancing Security with Heterogeneous Multi-core Computing

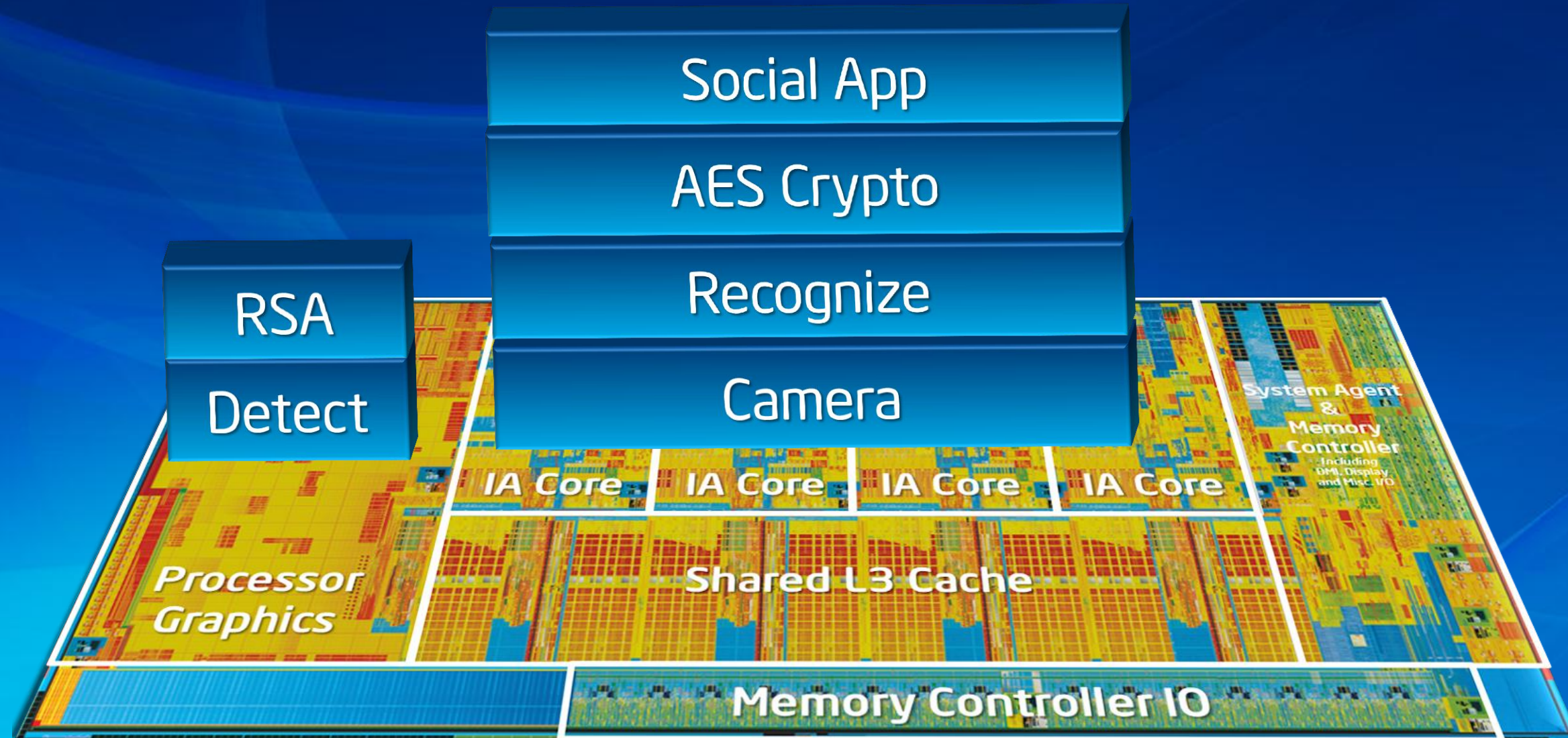


2<sup>nd</sup> Generation Intel® Core i7

# Enhancing Security with Heterogeneous Multi-core Computing



# Enhancing Security with Heterogeneous Multi-core Computing



# Looking to the future... Where Are We Headed?

# Many-core Computing at the Extremes

2W - 100 GigaFLOPS



20MW - ExaFLOPS



*10 year goal: ~300X Improvement in energy efficiency  
Equal to 20 pJ/FLOPS at the system level*



Technology  
The Future of Technology

Archives About this Blog

Technology Group and Director of Microproc  
ologies for Intel's future microprocess

gn of the 8051 family of microcontrol  
ercomputers. Borkar is an adjunct m  
er 60 articles and holds 41 patents.

a master's degree in Electrical Engin  
or degrees in Physics from the University of Bombay in 1979.



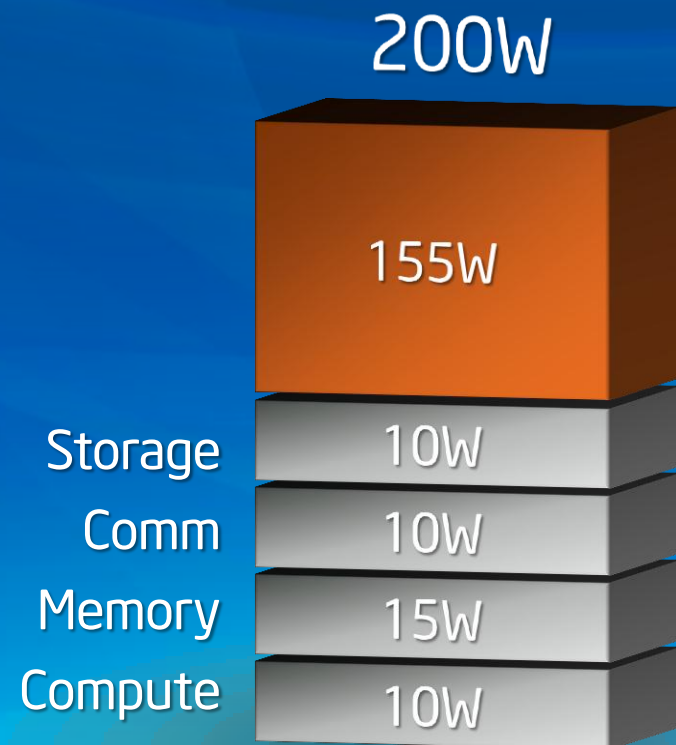
# *Taking Many-core* **TO THE EXTREME**

**Shekhar Borkar**

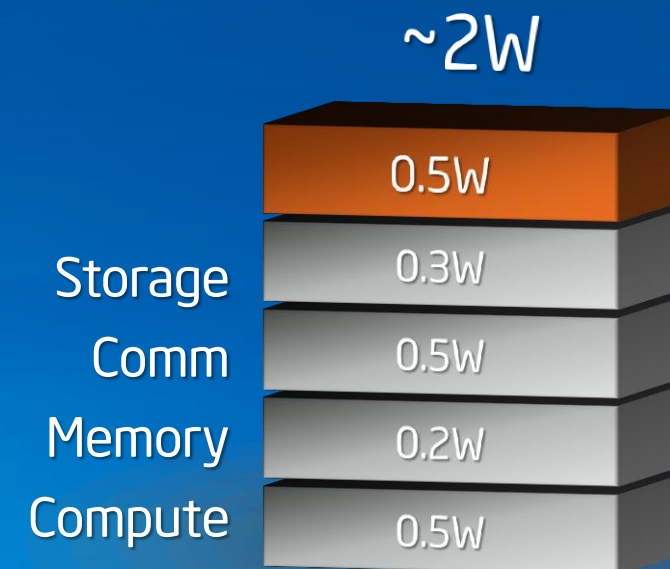
*Intel Fellow and Principal Investigator  
DARPA Ubiquitous High Performance Computing*

# What it Takes to Achieve Extreme Scale

Today's 100 GFLOPS  
*Intel® Xeon® System*



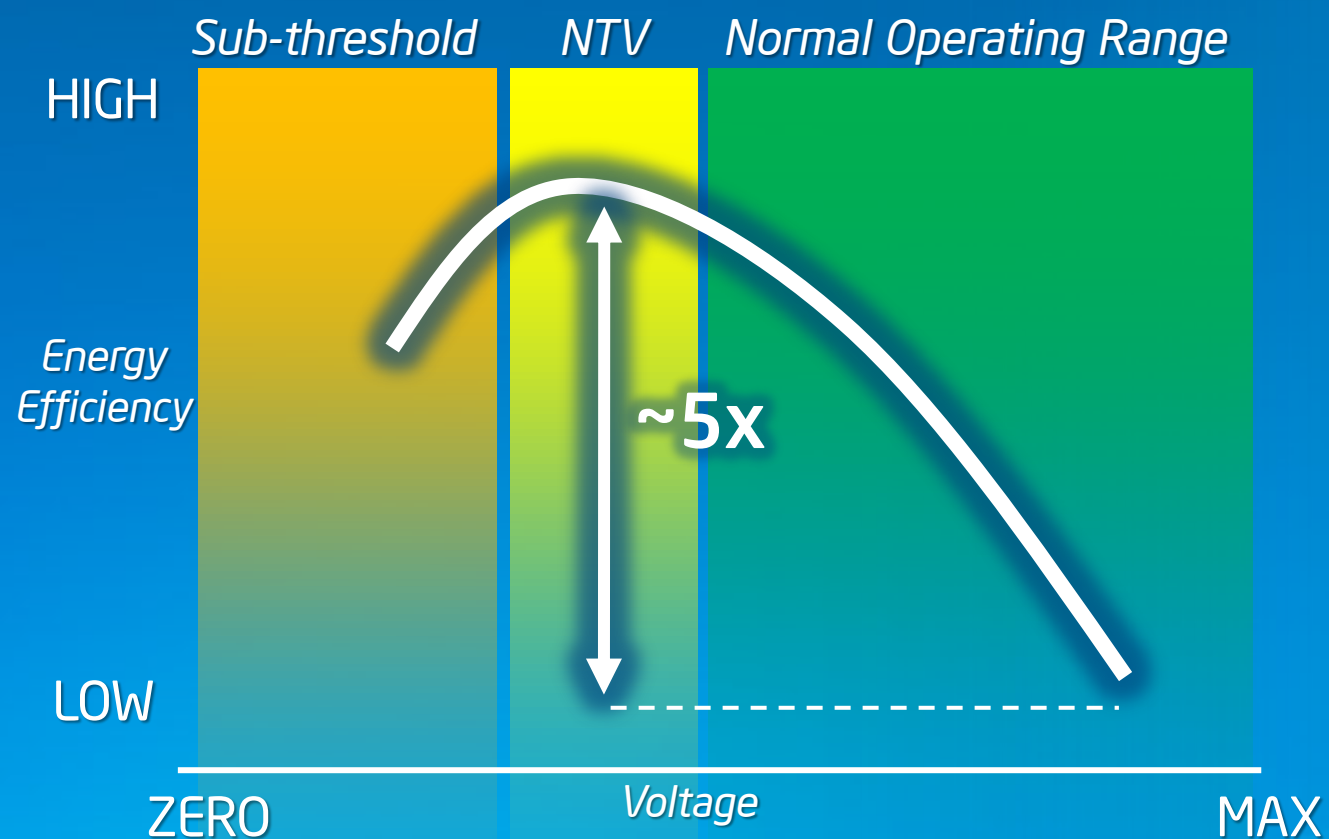
2018  
*Extreme Scale 100 GFLOPS System*



*Lowering CPU power does not automatically result in low power systems*

# Benefits of Near Threshold Voltage Operation

*Peak energy efficiencies at NTV and fine-grain power management*



## Potential For...

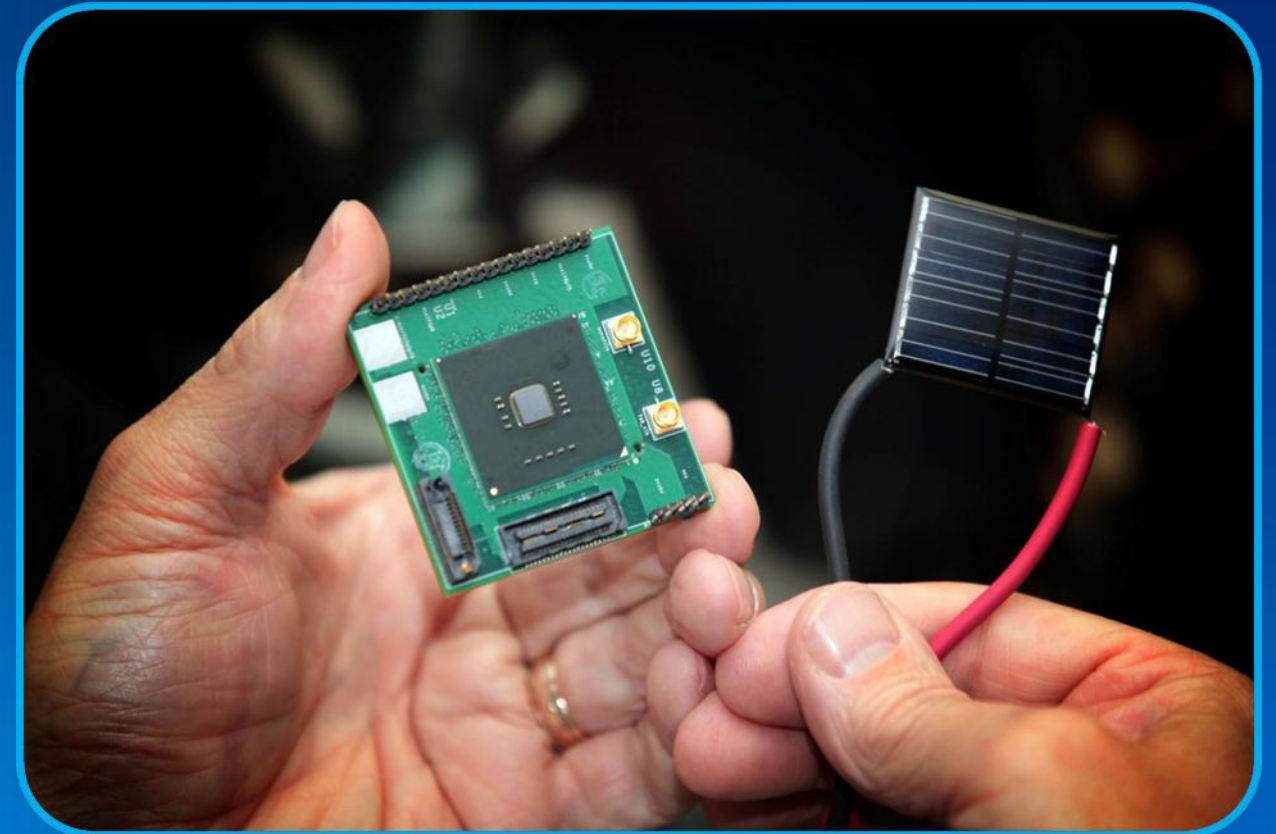
- More always-on / instant wake devices
- Intelligent everyday devices with battery/solar powered CPUs
- Longer battery lives for mobile computing
- Scalable many-core chips for the datacenter
- Meeting extreme-scale compute challenges

# Claremont: A Near Threshold Voltage IA Processor

First processor to demonstrate benefits of Near Threshold Voltage circuits

IA concept chip can ramp from full performance to ultra low power (<10mW)

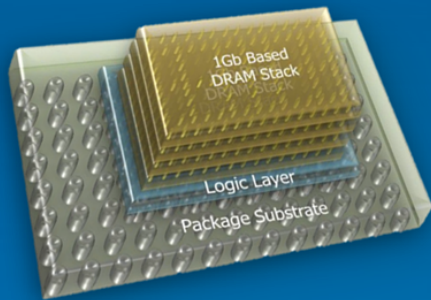
Scales to over **10X** the frequency when running at nominal supply voltage



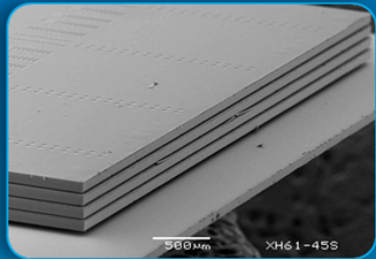
*Enables Ultra Low-power Devices with Wide Dynamic Operating Range*

# Hybrid Memory Cube: Experimental DRAM

*Highest performance and most energy efficient DRAM memory in the industry*



Hybrid DRAM Stack



Research Collaboration  
with Micron Technology

Lowest ever energy per bit (~8pJ per bit)  
7x better energy-efficiency than today's DDR3  
128GBps (>1 Terabit per second) bandwidth  
Highest ever bandwidth to a single DRAM device

Technology	VDD	BW GB/s	Power (W)	mW/GB/s	pJ/bit
SDRAM PC133 1GB ECC Module	3.3	1.1	7.7	7226	903.3
DDR3-1333 4GB ECC Module	1.5	10.7	4.6	432	54.0
HMC Gen1 512MB Cube	1.2	128.0	8.0	62	7.78

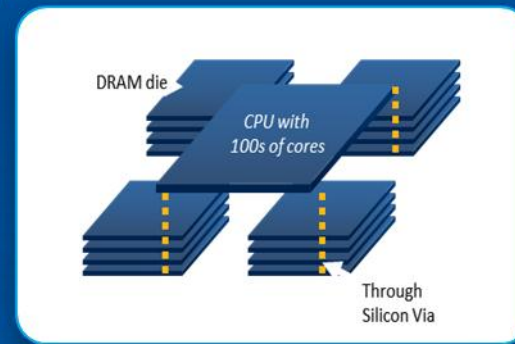
# Extreme Scale Computing Research Agenda



Extreme  
Energy  
Efficiency



Fine-Grain  
Power  
Management



Efficient  
Memory  
Subsystem



Self-Aware  
Computing  
Operation



Programming  
for Extreme  
Parallelism

*System-Wide Breakthroughs Needed Across the Board*

*What We've Really Been  
Talking About Here Today*  
**IS THE FUTURE...**



# THE TOMORROW PROJECT

CONVERSATIONS ABOUT THE FUTURE

## Join the Conversation by Visiting:

Theater of Tomorrow in the IDF Tech Showcase

<http://techresearch.intel.com/tomorrowproject>



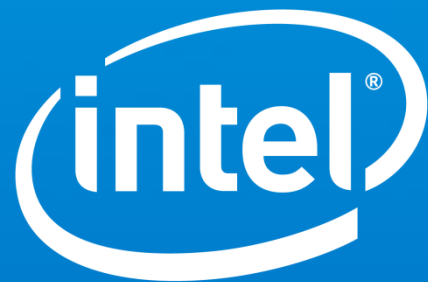
# LIMITLESS POSSIBILITIES

WE ARE HERE



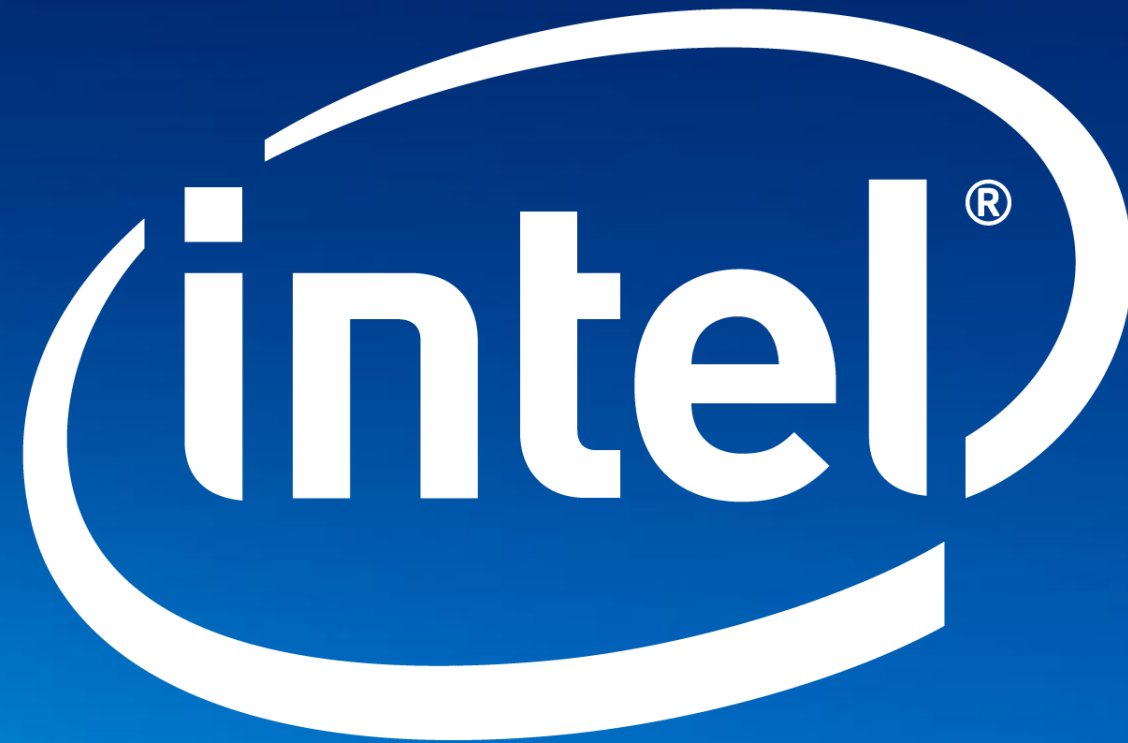
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