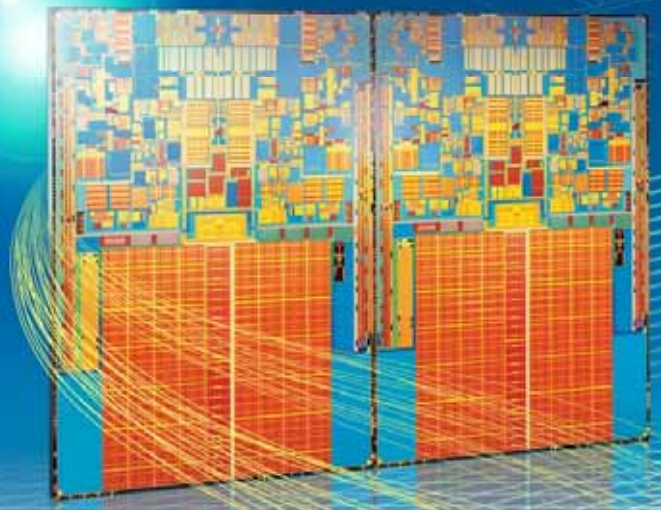
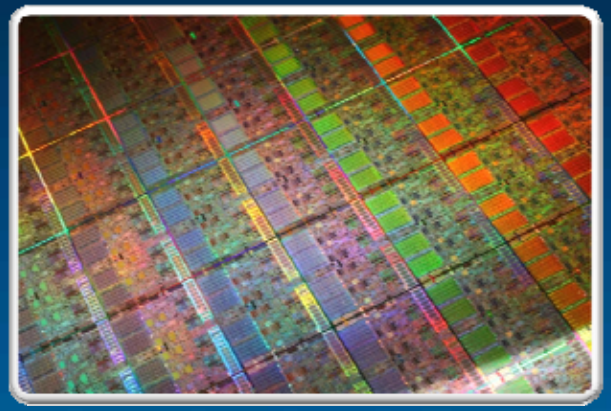
Invent the new reality.



Intel Developer
FORUM

Intel Architecture =



Embedded + Dynamic + Visual

Pat Gelsinger
Senior Vice President and Co-General Manager
Digital Enterprise Group

In Retrospect

"We are heading toward a world of a billion – a billion connected computers."

Andrew S. Grove
Chairman & CEO, Intel Corporation
IDF, February 17, 1998

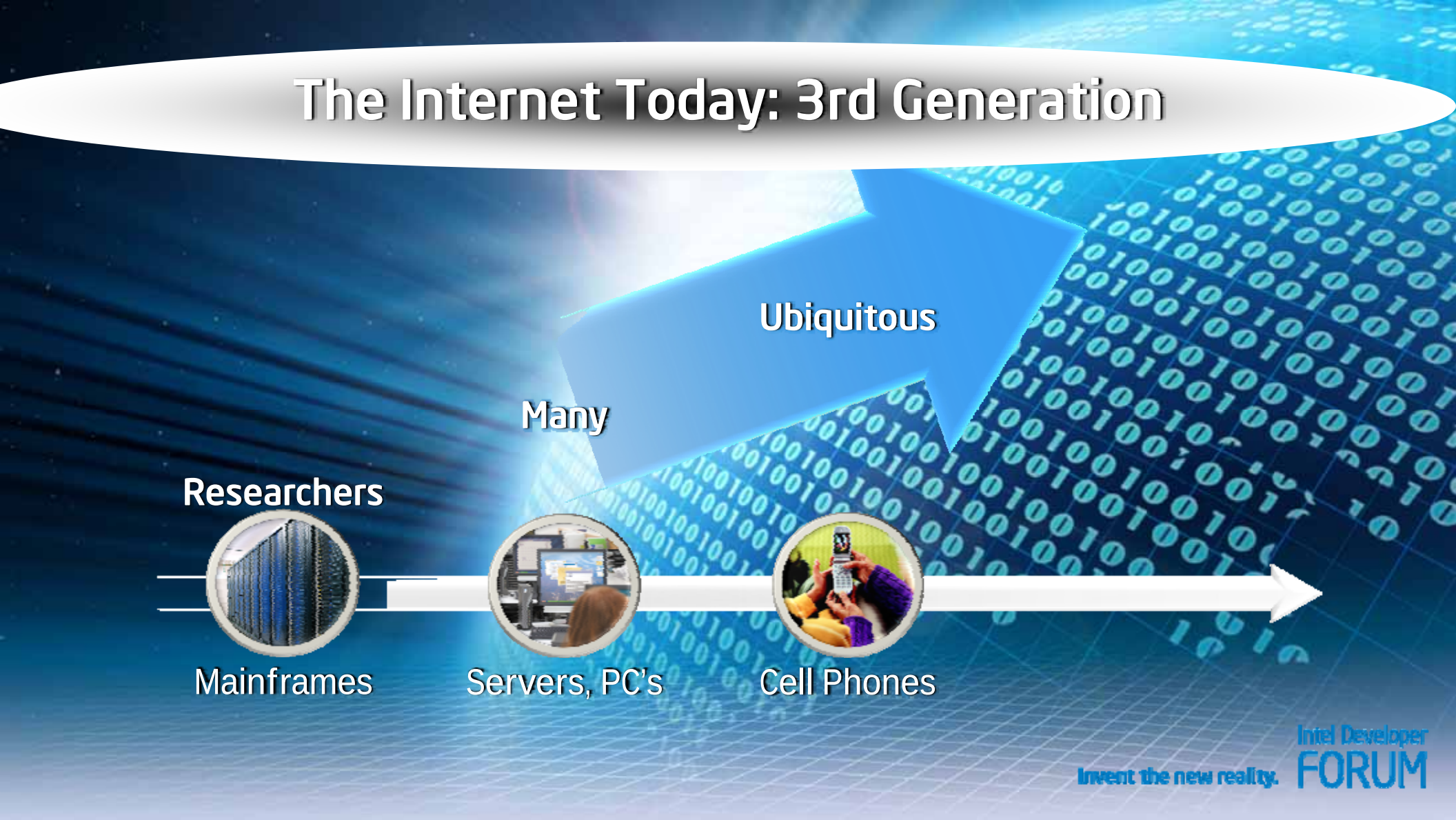
"Our vision is for a billion interconnected computers attached to the Internet. The mobile or wireless vision is a billion subscribers who can talk to each other and also have Internet access."

Craig Barrett
CEO, Intel Corporation
IDF August 22, 2000

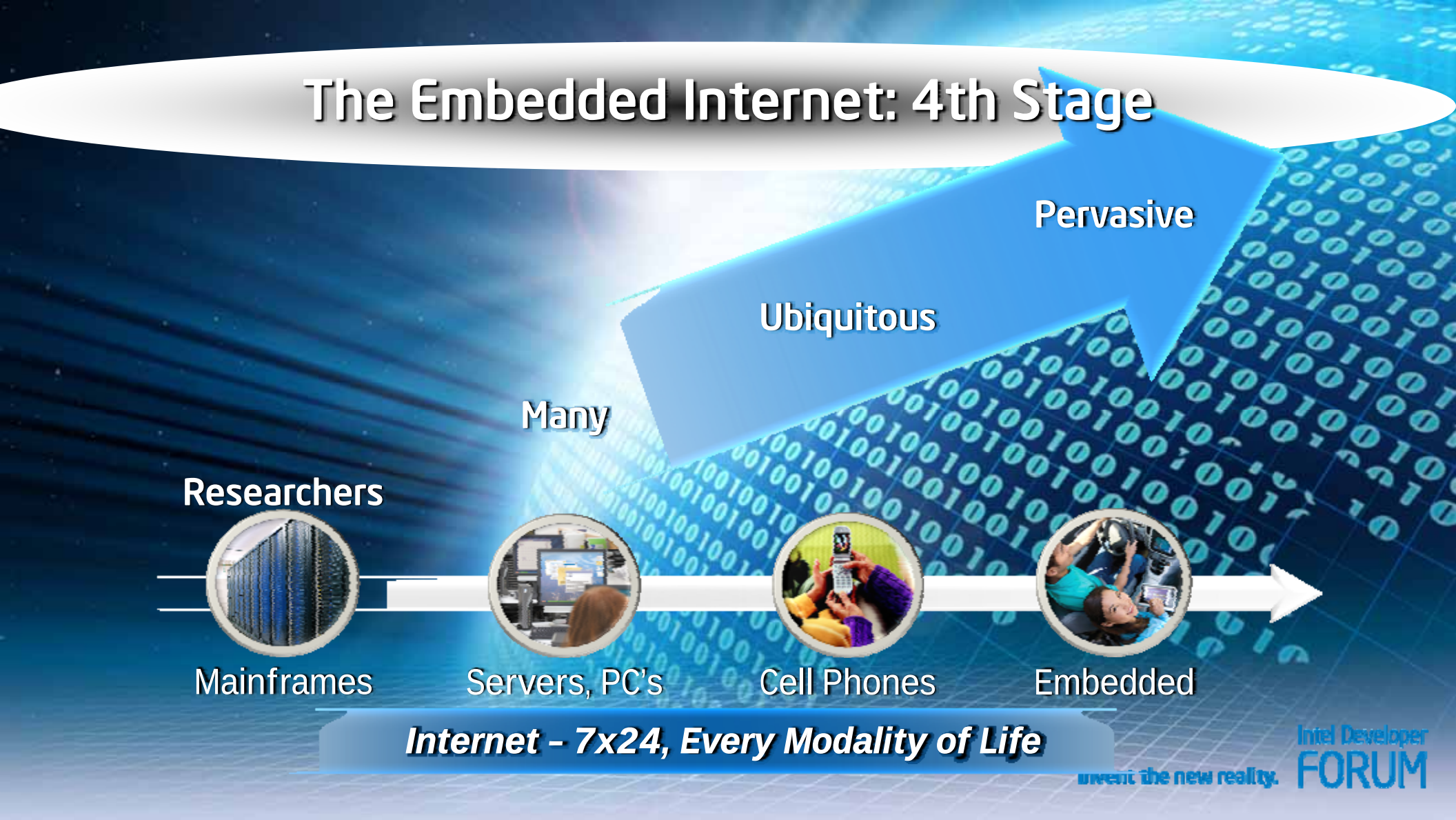
"The vision of a billion connected phones and a billion connected handsets is happening . By 2010, those same trends will give us a 1.5B connected PCs, except this time, it's broadband . Those same trends will give us 2.5B connected handsets."

Paul Otellini
President & COO, Intel Corporation
IDF, Sept 23, 2003

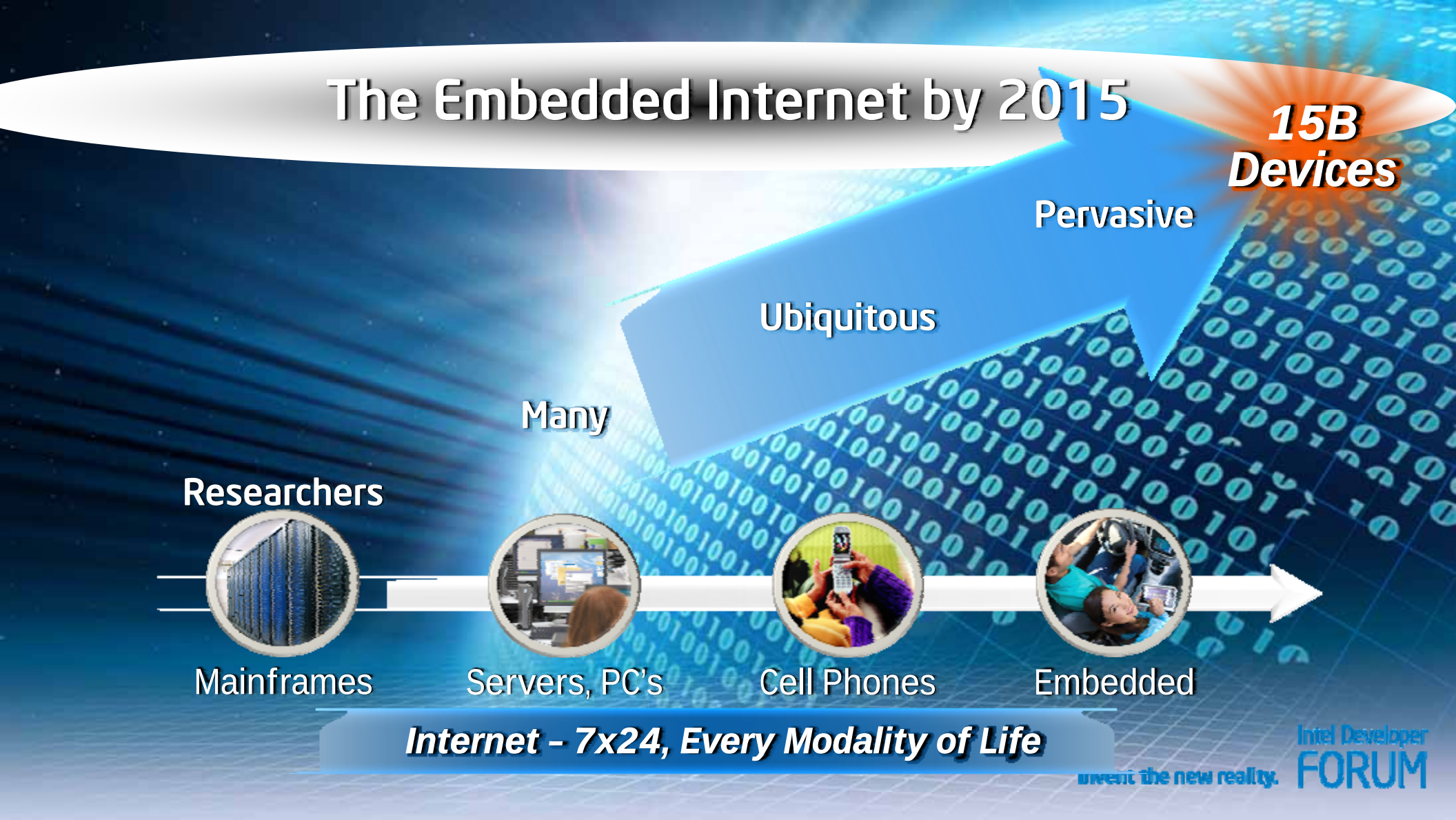
The Internet Today: 3rd Generation



The Embedded Internet: 4th Stage



The Embedded Internet by 2015



The Next Wave of Devices






"Personal"

"Public"

Towards 15B Devices by 2015

Top Barriers

- Reliability and Long Life
- Software Scalability
- Low Power and Low Cost
- Privacy and Data Security
- IPv4 Addressing
- Open Standards

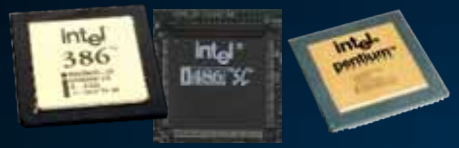
Towards 15B Devices by 2015

Top Barriers	Solutions
Reliability and Long Life	Intel® Products
Software Scalability	Intel Architecture
Low Power and Low Cost	Intel® Atom™ Processor and SoCs
Privacy and Data Security	Encryption, Standards, Policy
IPv4 Addressing	Drive Towards IPv6 by 2012
Open Standards	Wifi, WiMAX, RFID, Bluetooth ZigBee, Z-Wave, LTE, P2P SIP, Open IPTV

Serving the Embedded Segment Since 1976

1970's | 1980's | 1990's | 2000 | 2005 →

Silicon



1st Integrated Chipset For Embedded

Ecosystem

Intel Creates 1st Embedded Ecosystem Program

Market

Intel Enters Embedded Market Segment

Keynote at 1st Embedded Systems Conference

Intel Revenue $500M+ In Embedded

Intel Revenue $1B+ In Embedded

Embedded Market Segment Is Growing

Celebrating 30+ Years in Embedded

Invent the new reality. Intel Developer FORUM

The Preferred Architecture for Embedded Internet

Scalable Architecture

intel Xeon inside

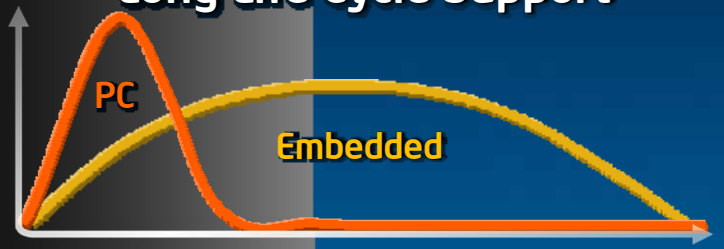
intel Core 2 inside

intel Atom inside

Solutions from <1W-130W

Intel Architecture

Long Life Cycle Support



Purpose Built Solutions

World's Best Ecosystem and Tools

intel Embedded and Communications Alliance

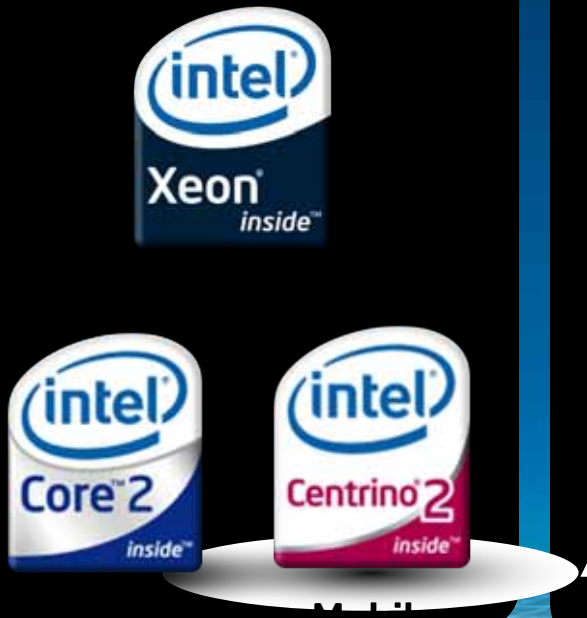
Embedded Products Today and Future

Traditional Embedded IA

Desktop Mobile

Embedded Products Today and Future

Traditional Embedded IA



New Low Power IA

Introduced: April 2008

Fan-less

<5W Platform

Small Footprint

~700 Embedded Customer Design Engagements

Accelerating Conversion From Other Architectures

Embedded Products Today and Future

Traditional Embedded IA

Desktop Mobile

New Low Power IA and SoCs for Embedded

Announced July 2008

First IA SOC since 80386EX in 1994

- Intel® QuickAssist Technology
- Communications I/O

Industrial temperature offering

45% area savings*, 30% power savings*

Q3'08 production

Embedded Products Today and Future

Traditional Embedded IA

Desktop Mobile

New Low Power IA and SoCs for Embedded

Q1'09

2H'09

Home Automation

Open Architecture

Low-power

Small Form Factor

IP Media Phones:

Resetting Expectations For The Home Phone

Invent the new reality.

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In-Vehicle Infotainment:
Bringing IT to the Car

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Emerging Open Infotainment Platform

Design Services

Middleware and Applications

Board Vendors/ODMs

Operating Systems

Complimentary Auto Silicon

- TV: Terrestrial/Satellite
- Rich 3D GPS
- Social Networking
- Online Gaming
- Video On Demand
- Office Synch
- NG Remote Diagnostics

Supported by Broad Eco-System

Industry Momentum

"BMW Group welcomes Intel's commitment to the automotive infotainment space, enabling us to bridge the gap between current automotive implementations and the consumer sector."

Christoph Grote
Senior Vice President Information & Communication Systems
BMW Group

BMW Group

"A more open and standard approach to infotainment product development will enable the automotive industry to more quickly meet the consumer demands for Multimedia and Internet access."

Tsuguo NOBE
General Manager
NISSAN MOTOR CO., LTD.

NISSAN MOTOR COMPANY

"With open infotainment platforms, our traditional tier 1 suppliers could concentrate on using their engineering power to create new innovations for us. I also expect quality improvements since multiple suppliers will be able to use and test the same software."

Mr Häussermann
VP Infotainment Development
Daimler - Mercedes Benz

DAIMLER

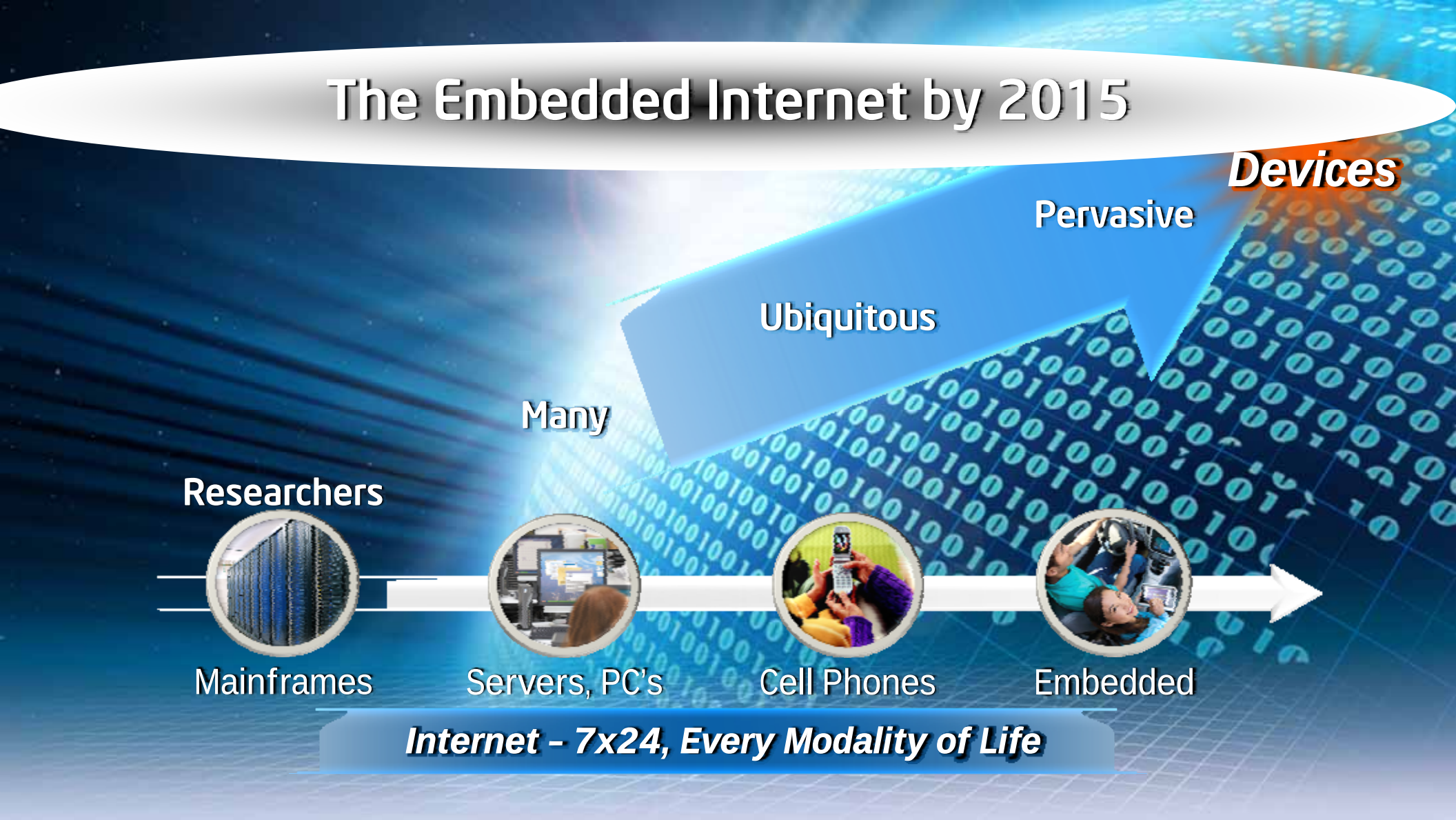
In-Vehicle Infotainment

Alex Busch
Information and Communication Systems
BMW Group

"... the solution for the future could be to add vehicle-specific components and requirements to existing IT technology and make it suitable for use in cars."

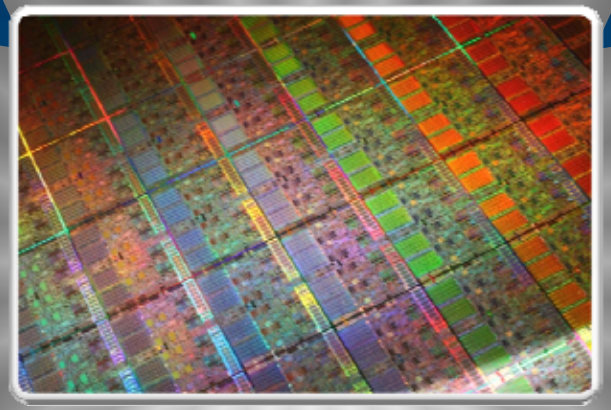
(Source: BMW Group press release, March 12, 2008, http://www.press.bmwgroup.com/pressclub/gb02.nsf, BMW Innovation Day 2008)

The Embedded Internet by 2015



Intel Architecture

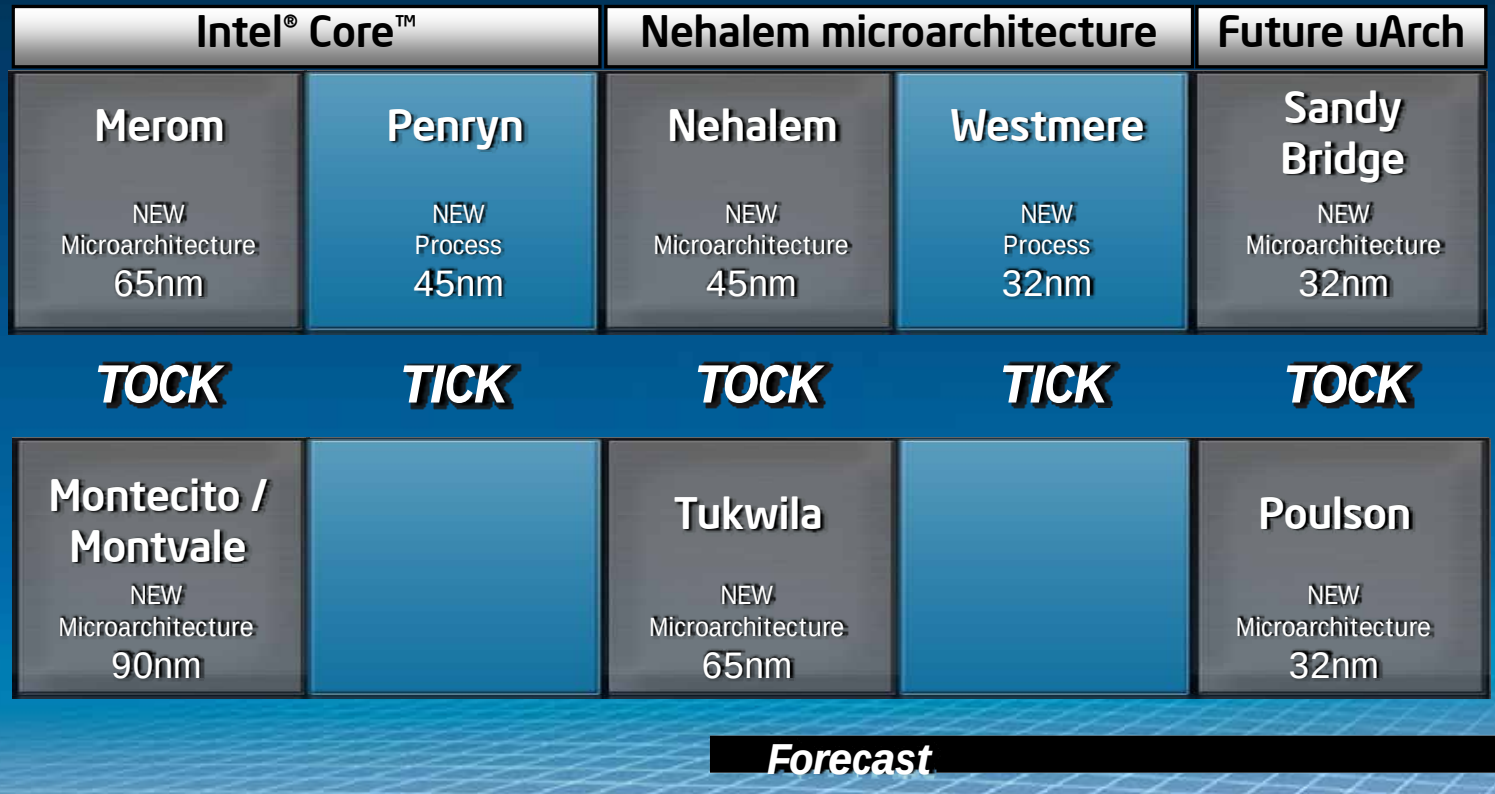
Embedded +



Dynamic +

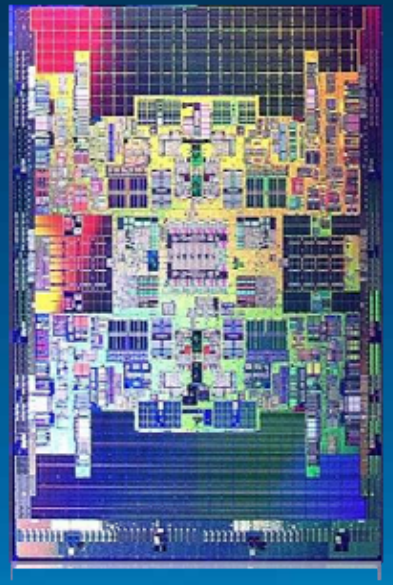
Visual

Tick-Tock Development Model:
Predictable, Sustained Microprocessor Leadership



Next Generation Intel® Itanium® (Tukwila)

- 1st 2B transistor chip
- Built for mission critical enterprise
  - On-die error protection
  - RAS
  - Advanced power and thermal management
- 2nd generation Virtualization Technology
- Strong roadmap with Poulson and Kittson



"With Intel's upcoming quad-core Tukwila processor, Windows Server solutions running on Itanium-based systems will provide an even more scalable and reliable datacenter foundation for our customers."

Bill Laing
Corporate Vice President
Windows Server Division,
Microsoft

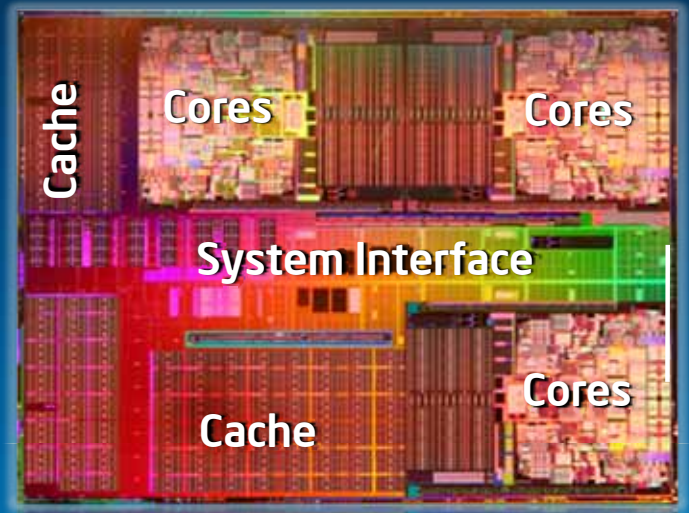
Business Critical Capabilities for Most Demanding Systems

Intel® Xeon® 7400 Series (Dunnington)

Virtualization platform of choice – just got better

Investment Protection
- Intel VT FlexMigration
- Socket compatible with Xeon™ 7300

45 nm high-k
- 6 cores
- 16MB shared L3 cache



Extending MP Leadership in September 2008

Intel® Xeon® Processor 7400 Series: Setting New Enterprise Performance Records

IBM

TPC Benchmark* C - DB2
1,200,632 tpmC
First 8S 1 M+ TPC-C database result for Xeon!

hp

TPC Benchmark* C – SQL Server
634,825 tpmC

Sun microsystems

SPECjbb*2005 - – Java HotSpot JVM
531,669 bops

DELL

TPC Benchmark* E
671.4 tpsE

intel

vConsolidate –
VMware* ESX 39% better**

FUJITSU COMPUTERS SIEMENS

SPECint*_rate2006
277 peak score

Unquestioned Expandable Server Leadership

**Intel Xeon X7460 (16M cache, 2.66GHz, 1066FSB) 6-Core compared to Intel Xeon X7350 (4M cache, 2.93GHz, 1066FSB) Quad-Core

Nehalem Family

Server and Workstation

Efficient Performance (2S)

Expandable (4S+)

Business and Consumer Clients

High End Desktop

Mainstream Client

Thin and Light Notebook

Nehalem: Innovative New Architecture

2, 4 or 8 Cores

Integrated Memory Controller

QuickPath Interconnect

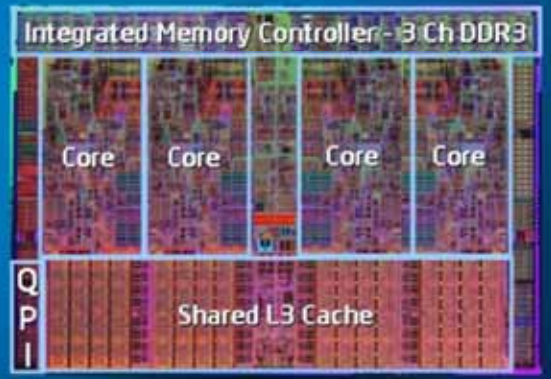
2-way Simultaneous Multi-threading

Microarchitecture Enhancements

Dynamic Power Management

SSE 4.2

Q4'08 Production



Fall 2007 IDF

Intel Developer FORUM

Invent the new reality.

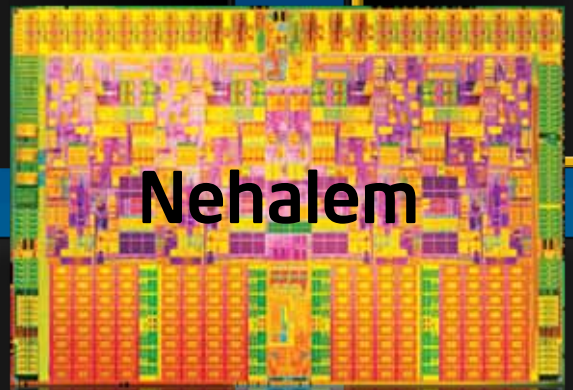
Nehalem: Next Generation Micro-architecture

Energy Efficient Performance

Intel Hyper-Threading Technology

Turbo Mode

Dynamic Power Management



Intel's 2nd Generation Virtualization

3x Memory Bandwidth

Best in Class Bandwidth with QPI

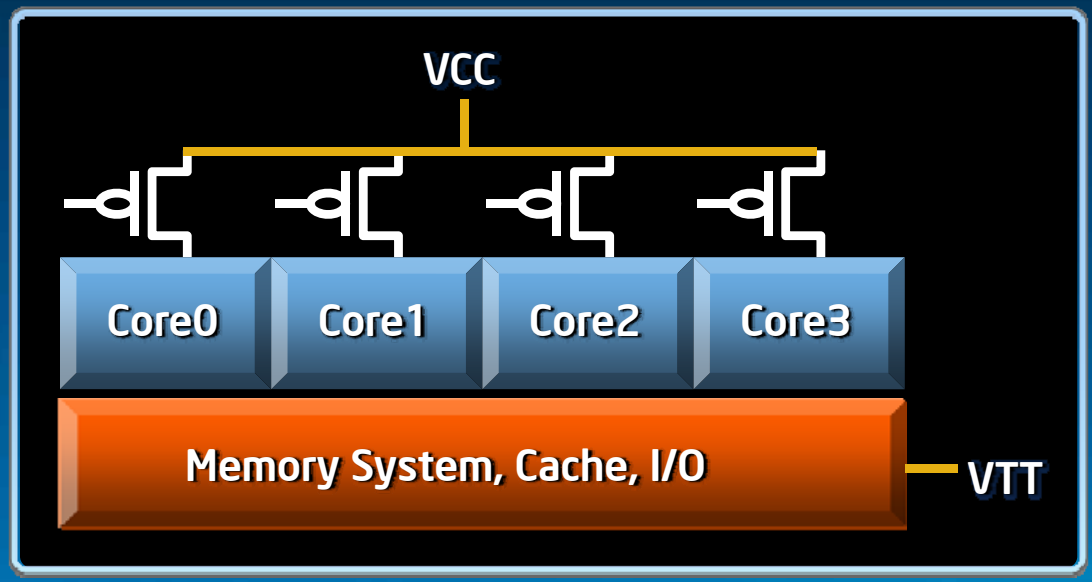
Industry's First Dynamically Scalable Architecture


Rajesh Kumar
Intel Fellow
Director, Circuit & Low Power Technologies
Intel Corporation
Invent the new reality.
Intel Developer
FORUM

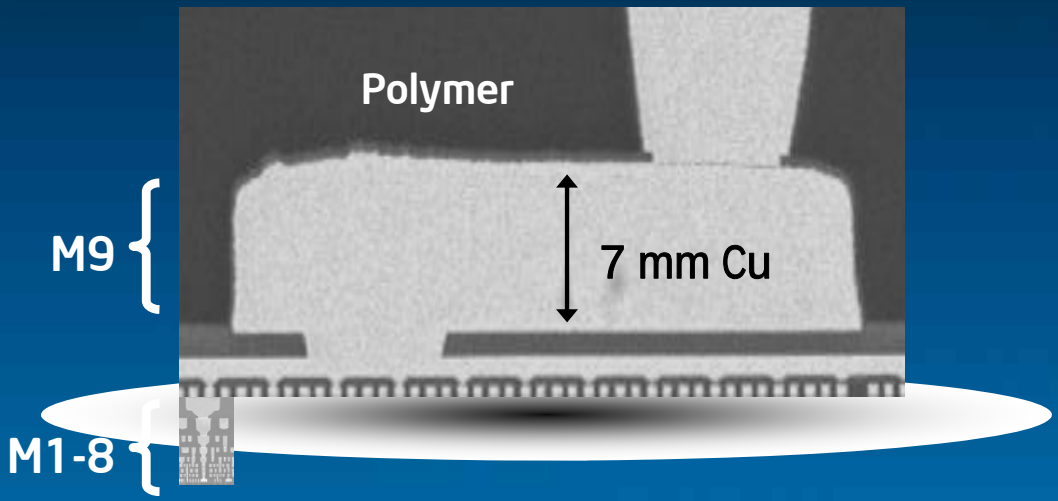
Integrated Power Gate

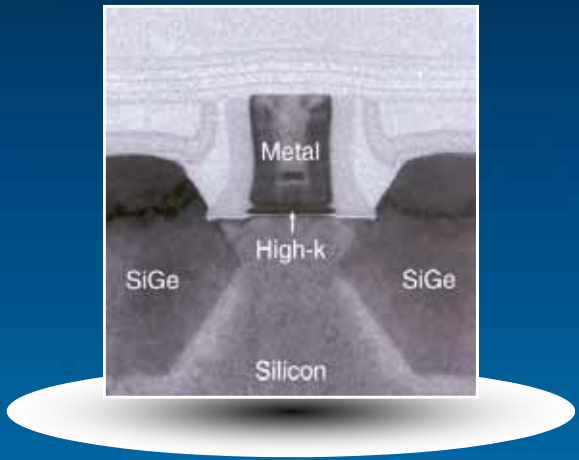
Clock Gate
- Standard in all Intel CPUs
- Eliminates switching power
- Leakage power remains

Power Gate: New
- Eliminates switching and leakage power
- Enables idle cores to go to near zero power (C6) independently
- Transparent to platform and software
- No incremental platform cost



Power Gates Silicon Technology



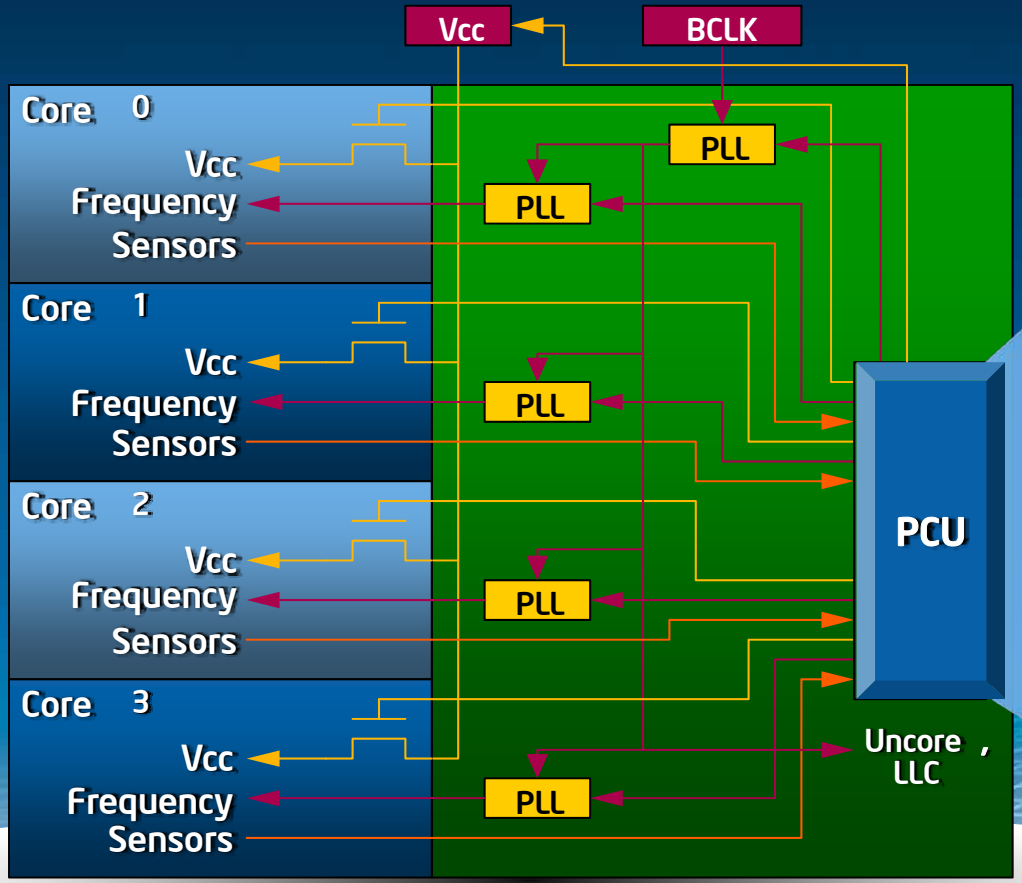


Package Like Metal (M9) Deposited On Silicon to Create Low On-resistance

Specialized, Ultra-low Leakage Transistor Developed for High Off-resistance

Intel Design and Process Technology Co-development

Power Management: Power Control Unit



- Integrated microcontroller
- Controlled by firmware
- Real time sensors for current/ power, voltage, temperature
- Enables sophisticated algorithms for current operating conditions

Nehalem Turbo Mode

Nehalem Turbo Mode

Power Gates

Near Zero Power For Inactive Cores

Nehalem Turbo Mode

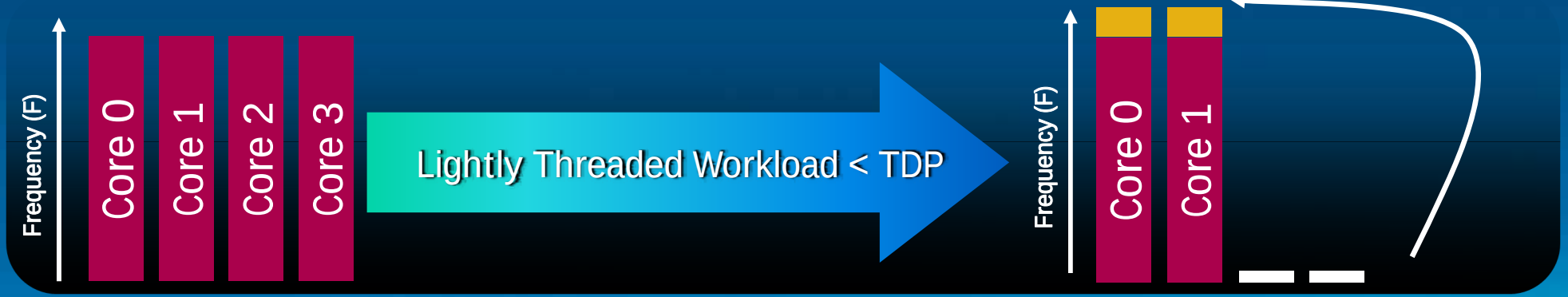
Power Gates

Near Zero Power For Inactive Cores

Turbo Mode

Adds Additional Performance Bins*
In Response To Workload

No Turbo



*within power and thermal constraints

Nehalem Turbo Mode

Power Gates

Near Zero Power For Inactive Cores

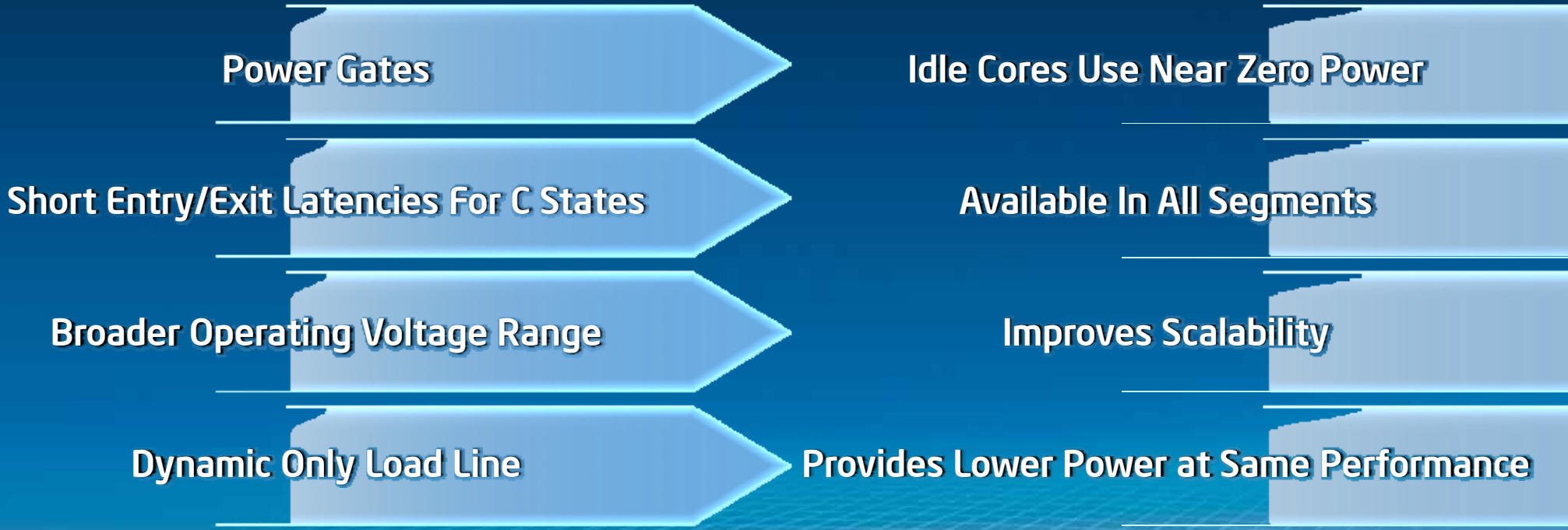
Turbo Mode

Adds Additional Performance Bins*
In Response To Workload

Dynamically Delivering Optimal Performance and Energy Efficiency

*within power and thermal constraints

Nehalem Innovations: Dynamic Power Management



Nehalem Family

Server and Workstation

Efficient Performance (2S)

Business and Consumer Clients

High End Desktop

World's Most Adaptable Server Platform

Today's Focus:

HPC

Content Creation

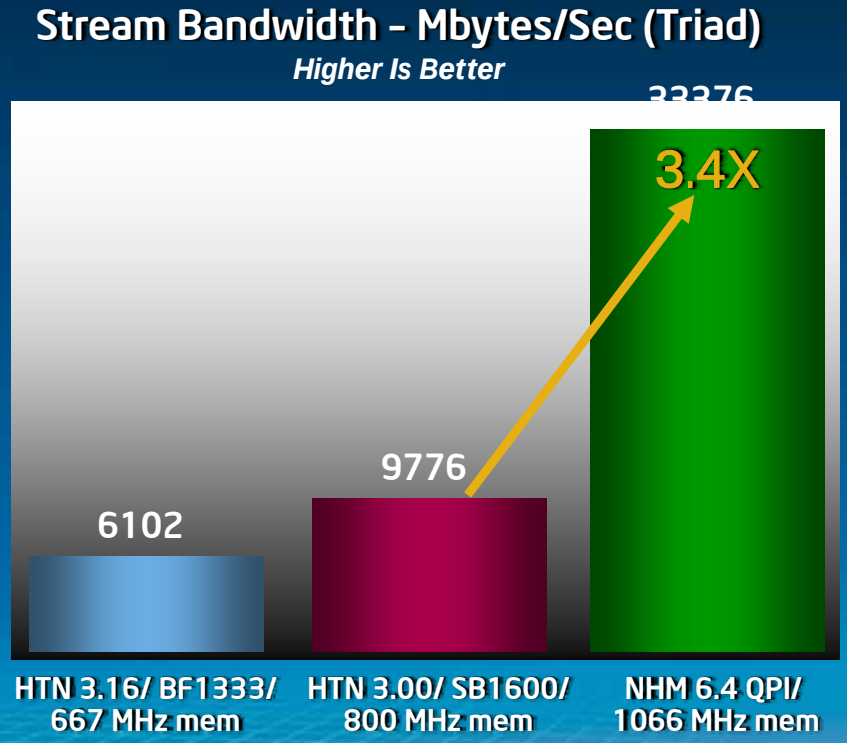
Virtualization

Nehalem – EP

Energy Efficient
- Performance on demand with Turbo mode
- Dynamic power management

Outstanding Performance
- Best in class bandwidth with QPI up to 25.6 GB/s
- DDR3 and supports 18 DIMM up to 288 GB

Designed for Virtualization
- Investment protection with FlexMigration
- Rapid VM migration with I/O optimizations



World's Most Adaptable Server Platform

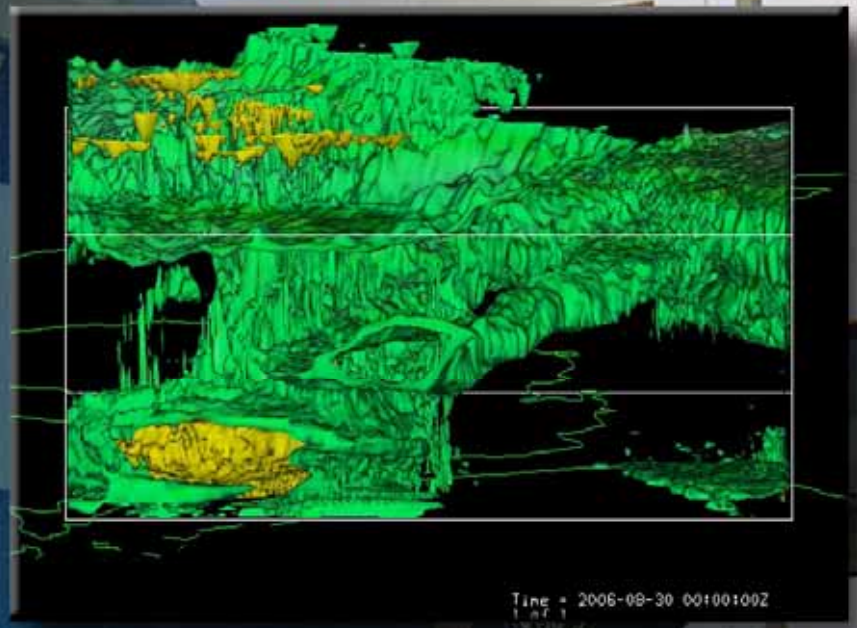
Source: Intel Internal measurements – August 2008

*** With 16 GB DIMMs**

Nehalem – EP: HPC and Visual Problem Solving

"The next-generation processor (Nehalem) and system technology will deliver a monumental increase in computing power, enabling further advances in scientific discoveries and engineering achievements in support of future NASA missions."

Rupak Biswas,
Director, NAS Division NASA



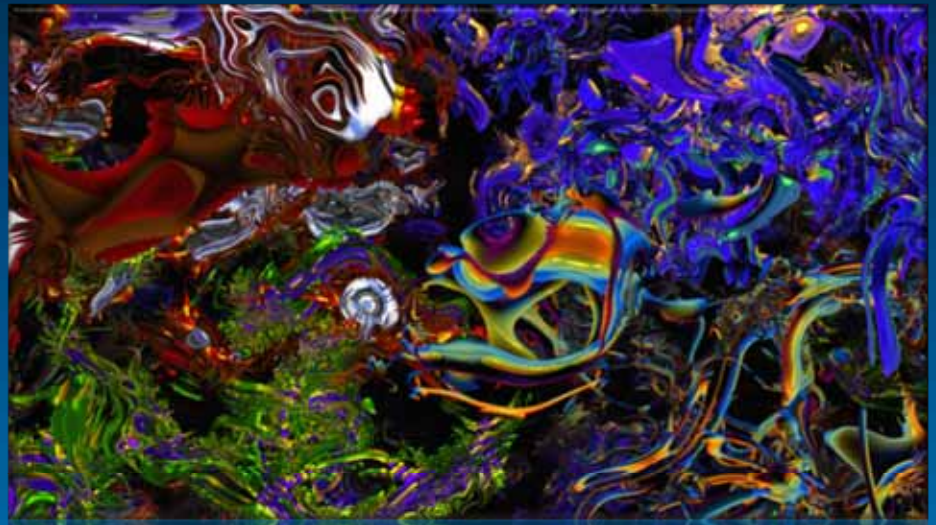
The Content Industry Embraces IA

Nehalem – EP: Advances in Content Creation

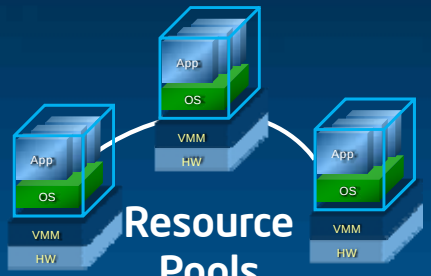
"Nehalem enables the creation of vast new worlds of complexity that were inconceivable before. I'm reeling from an exploding universe of inspiring possibilities. The dream of creating extended high resolution animations of the elaborate visions in my mind's eye is finally becoming a reality."

Kevin Mack
Oscar award-winning Digital Artist at Sony

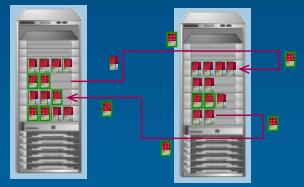
Nehalem – EP: Advances in Content Creation



Nehalem Platform: Designed for Virtualization 2.0



Resource Pools



VM Migrating over the network

Flexible Workload Management

Intel VT FlexMigration

Hardware and Software Evolution

New Capabilities: VT-x2, Intel Dynamic Power Manager

Enabling Ecosystem Support

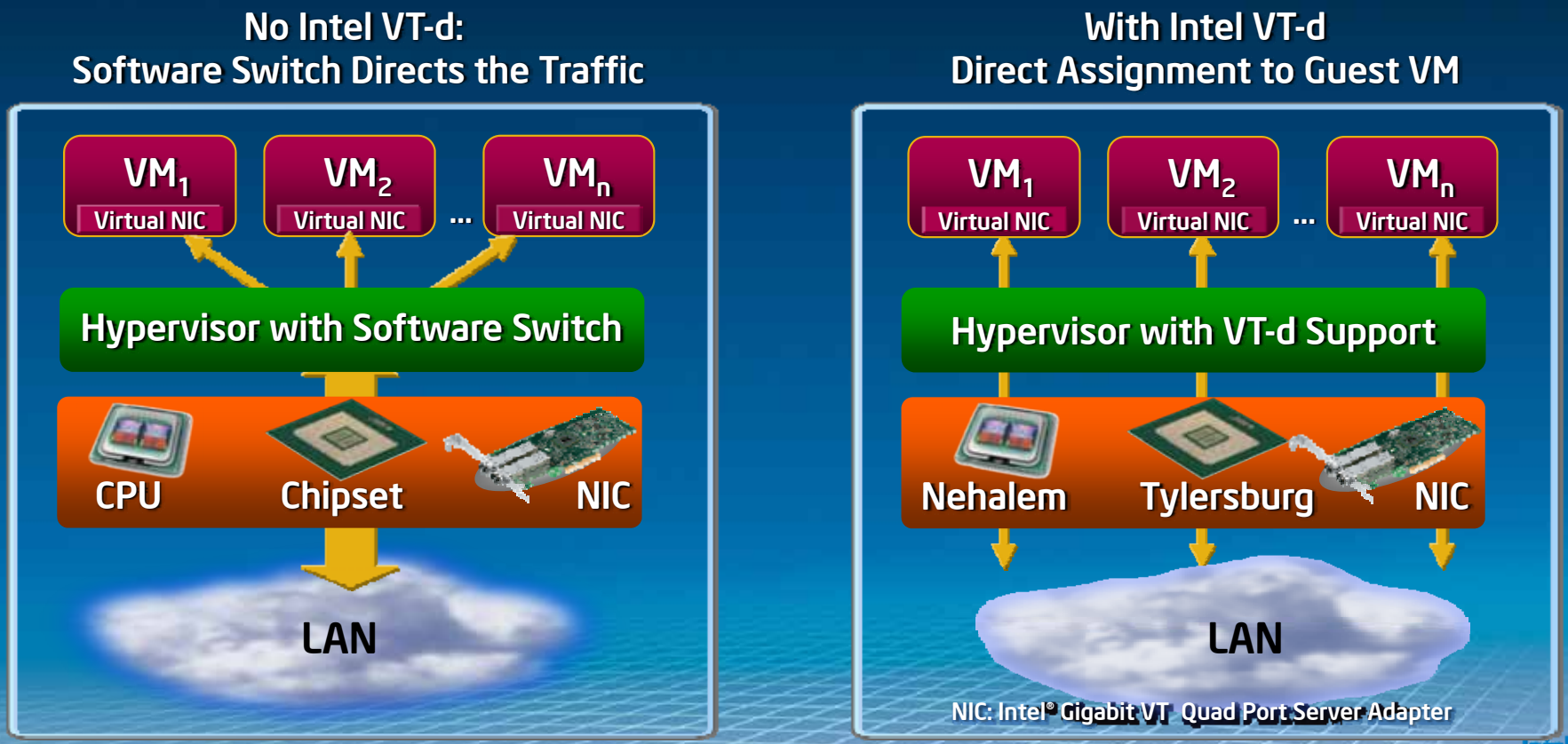
I/O Designed for Virtualization

Intel VT for Connectivity

Intel VT for Directed I/O: VT-d2

Fiber Channel Over Ethernet

Nehalem/Tylersburg VT-d Demo



Intel and Microsoft: Virtualization Collaboration

Intel® Dynamic Power Node Manager

- New dynamic approach to power budgeting for virtualized environment

Vary P-states and T-states for optimal performance/power ratios

"Microsoft and Intel have worked together to optimize Hyper-V for Intel Virtualization Technology and support the upcoming Dunnington processor. We're already seeing outstanding performance from our complementary software and hardware, which together provide our customers with amazing capabilities."

Bob Muglia
Senior Vice President
Microsoft Server & Tools Business

Nehalem Family

Server and Workstation

Efficient Performance (2S)

Expandable (4S+)

Business and Consumer Clients

High End Desktop

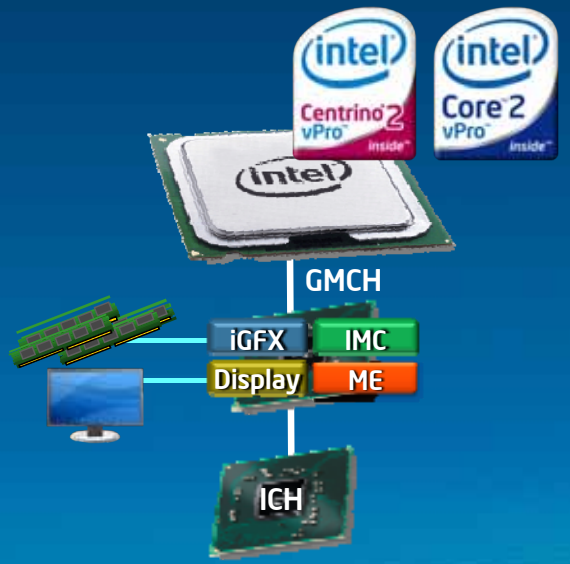
Mainstream Client

Thin and Light Notebook

Nehalem: Repartitioning the Client Platform

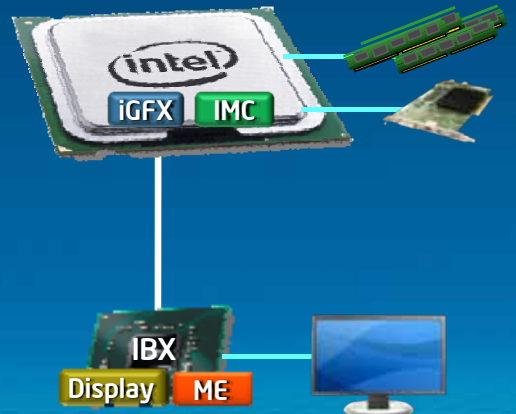
2008

Montevina and McCreary Platforms
3 Chip Solution



Calpella and Piketon Platforms
2 Chip Solution

Auburndale and
Havendale



- Scalable : 2 to 4 Cores
- Integrated memory controller
- Intel® Hyper-Threading and Turbo mode

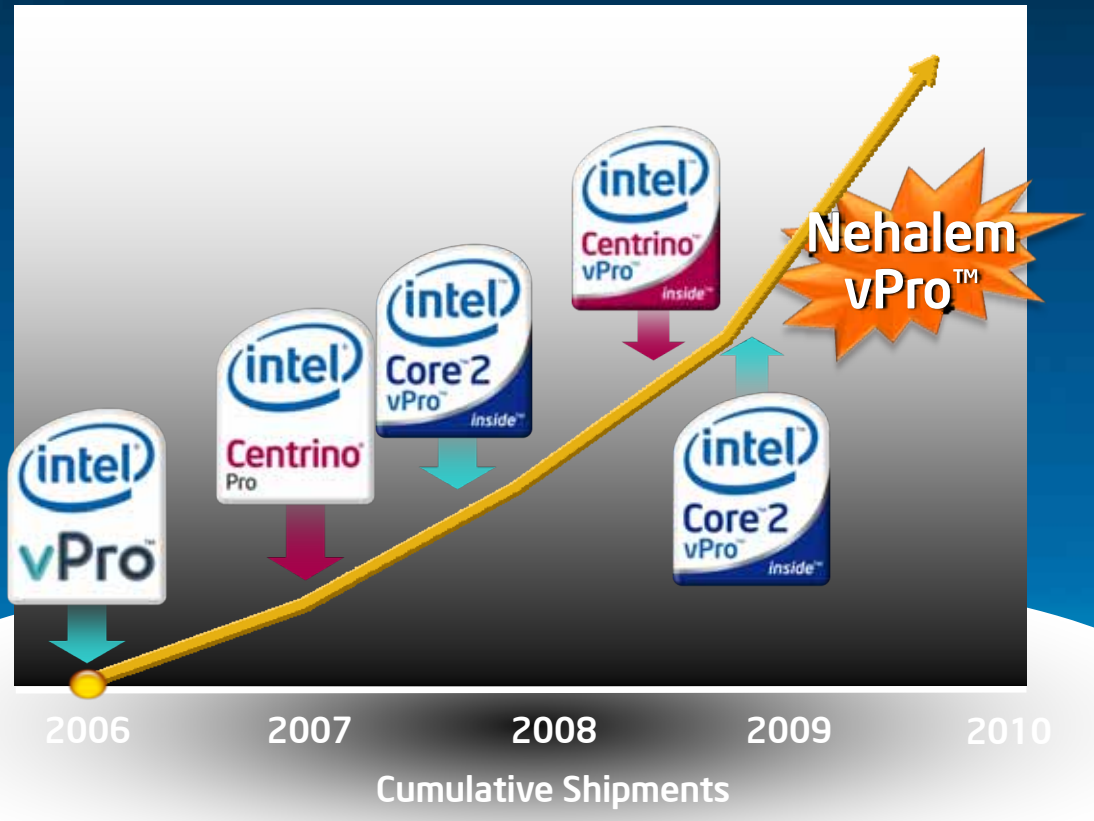
Introducing Ibex Peak:

- New product category
- Core platform capabilities

Higher Integration, Leading Performance with Lower Power

GMCH=Integrated Graphics Memory Controller Hub, ICH=I/O Controller Hub, PCH=Platform Controller Hub, GPU=Graphics Processor Unit
ME = Manageability Engine, VE= Virtualization Engine

Intel® vPro™: Critical Mass



60% of Fortune 100 Companies

All Leading OEMs

5000 Active Channel Partners

80+ ISV Partners

All Major Verticals

Worldwide

Intel® vPro™: Customers Activating in Volume

verizon

25,000 Clients

80% Desk-side Visits

45% Power Expense

850,000 lbs CO_2 Emissions

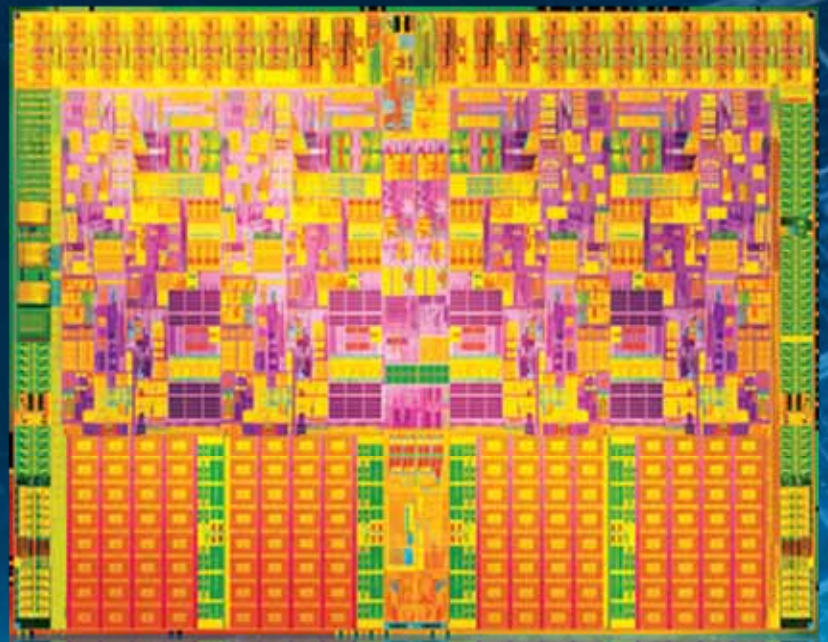
472% 4-year ROI

Unquestioned Leadership: Intel Core i7 Processor and X58 Chipset

- 4 cores - 8 threads
- Intel® Hyper-Threading technology
- Turbo mode
- 8 MB of Intel® Smart cache
- Intel® QuickPath interconnect
- Integrated 3-ch DDR3 memory controller
- PCI Express* 2.0 for discrete graphics


Intel Developer
Invent the new reality.
FORUM

IA is "Dynamic"



Nehalem is the First Dynamically Scalable Microarchitecture

World's Most Adaptable Server Platform

Extending Unquestioned Leadership

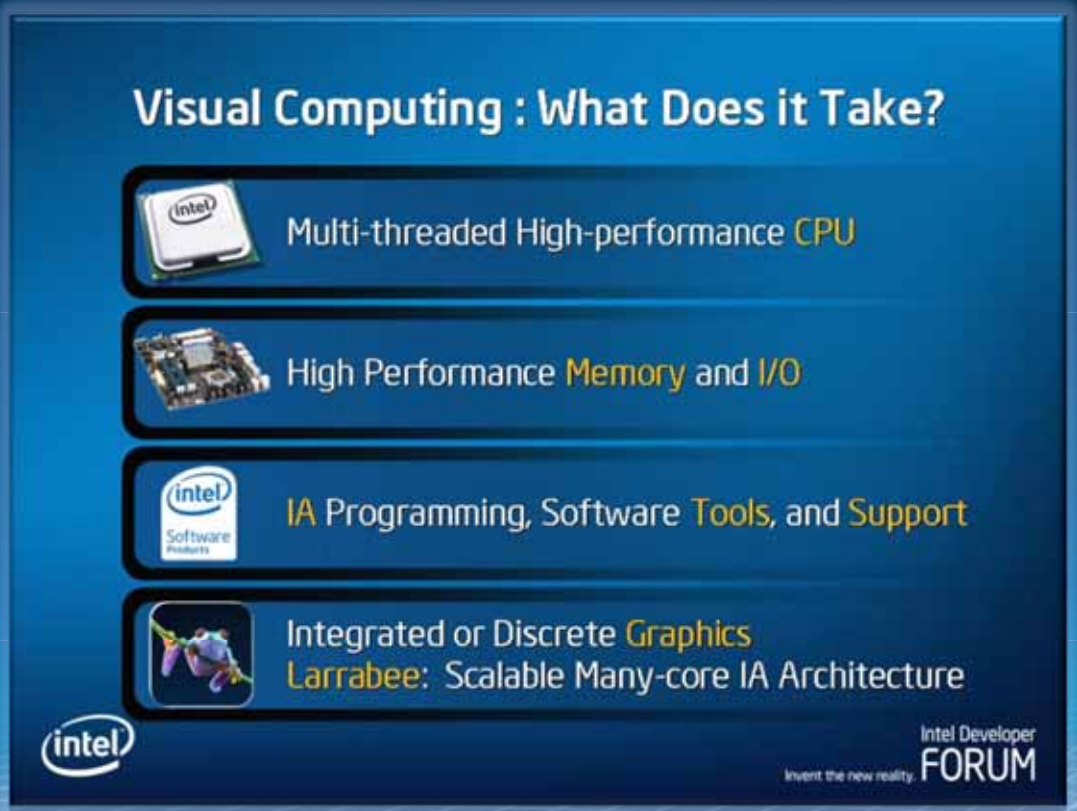
Intel Architecture

Embedded +

Dynamic +

Visual

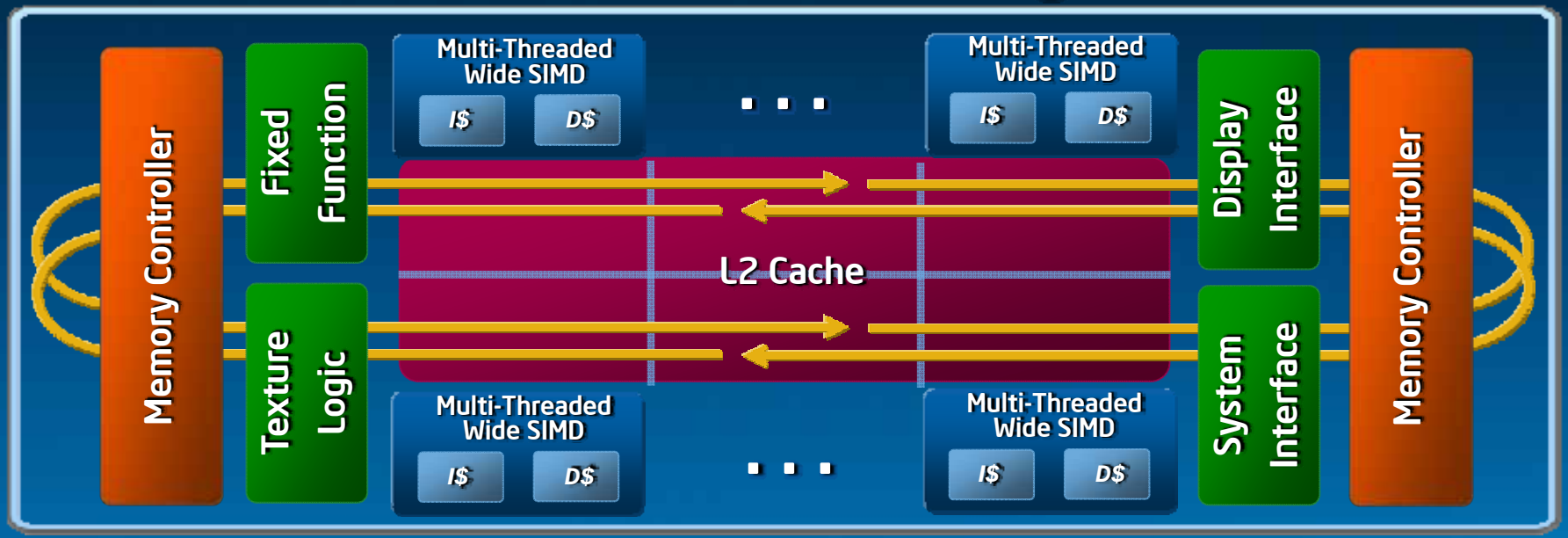
Visual Computing: Spring'08 IDF



Intel Developer FORUM
Invent the new reality.


Larry Seiler
Sr. Principal Engineer,
Visual Computing Group
Intel Corporation
Invent the new reality.
Intel Developer
FORUM

Larrabee: Block Diagram



- Multiple IA cores
  - In-order, short pipeline
  - Multi-thread support
- 16-wide vector units
  - Extended instruction set
- Fully coherent caches
- 1024-bit ring bus
- Dedicated texture logic
  - Supports virtual memory

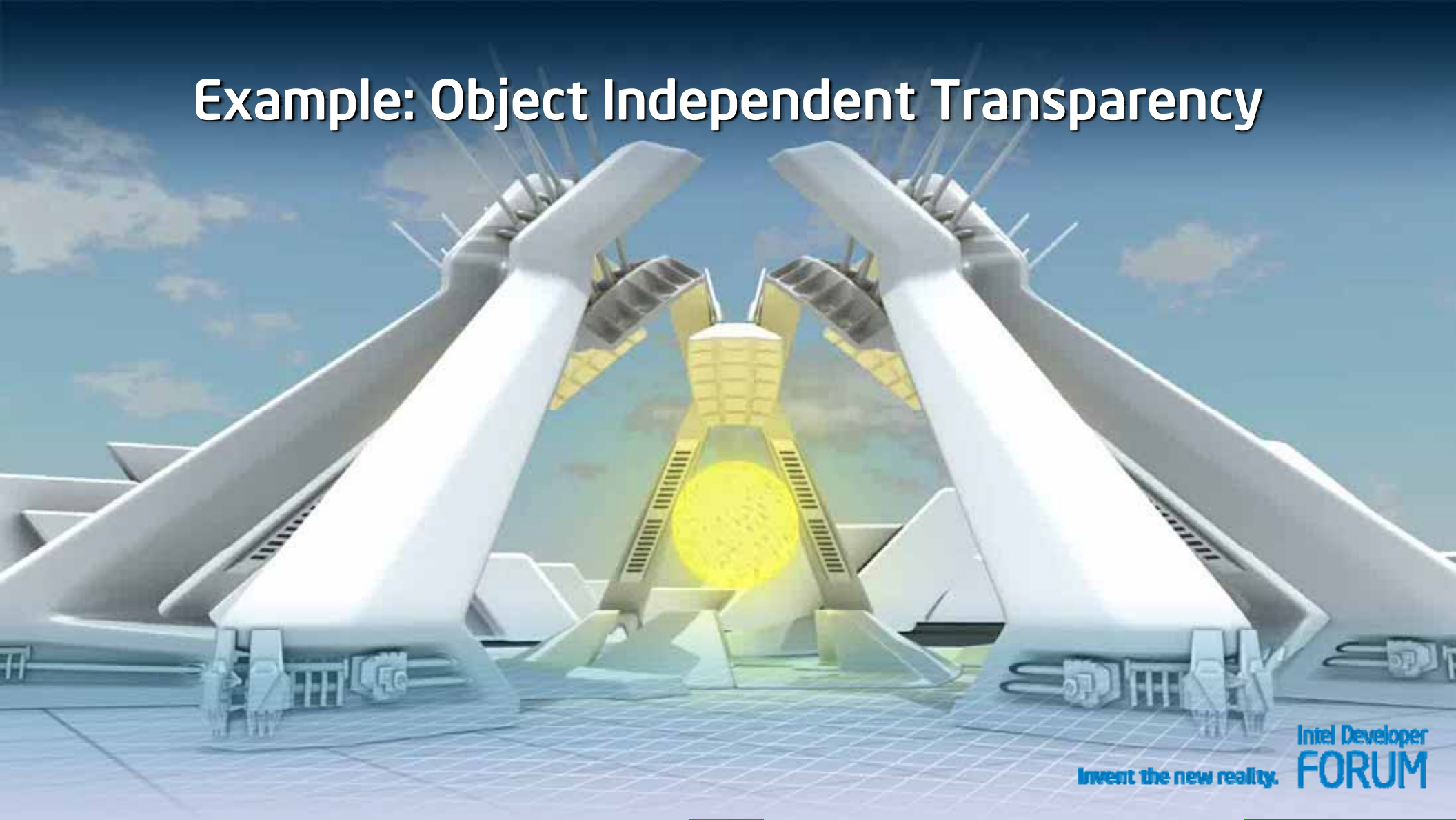
Transparency Example without Sorting

The small dragon was drawn first, so its translucent wing pops through the wing of the large dragon.

Transparency Example with Sorting

The translucent pixels are sorted so that the small dragon's wing is drawn behind the large dragon.

Example: Object Independent Transparency



Standard Shadow Map Algorithm

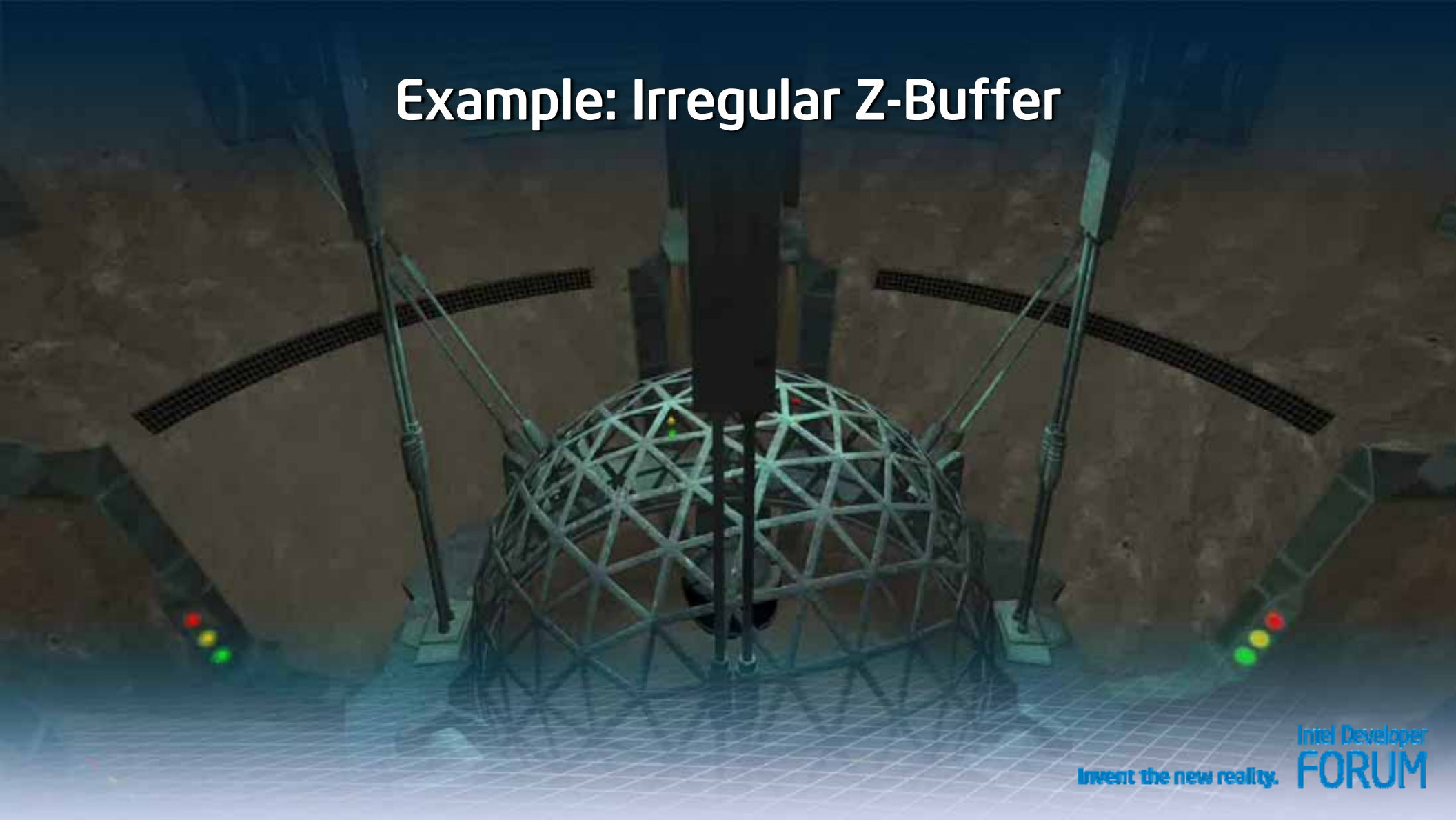
Jagged Edge Artifacts Are Evident With Shadow Maps

Shadows with Irregular Z-Buffer

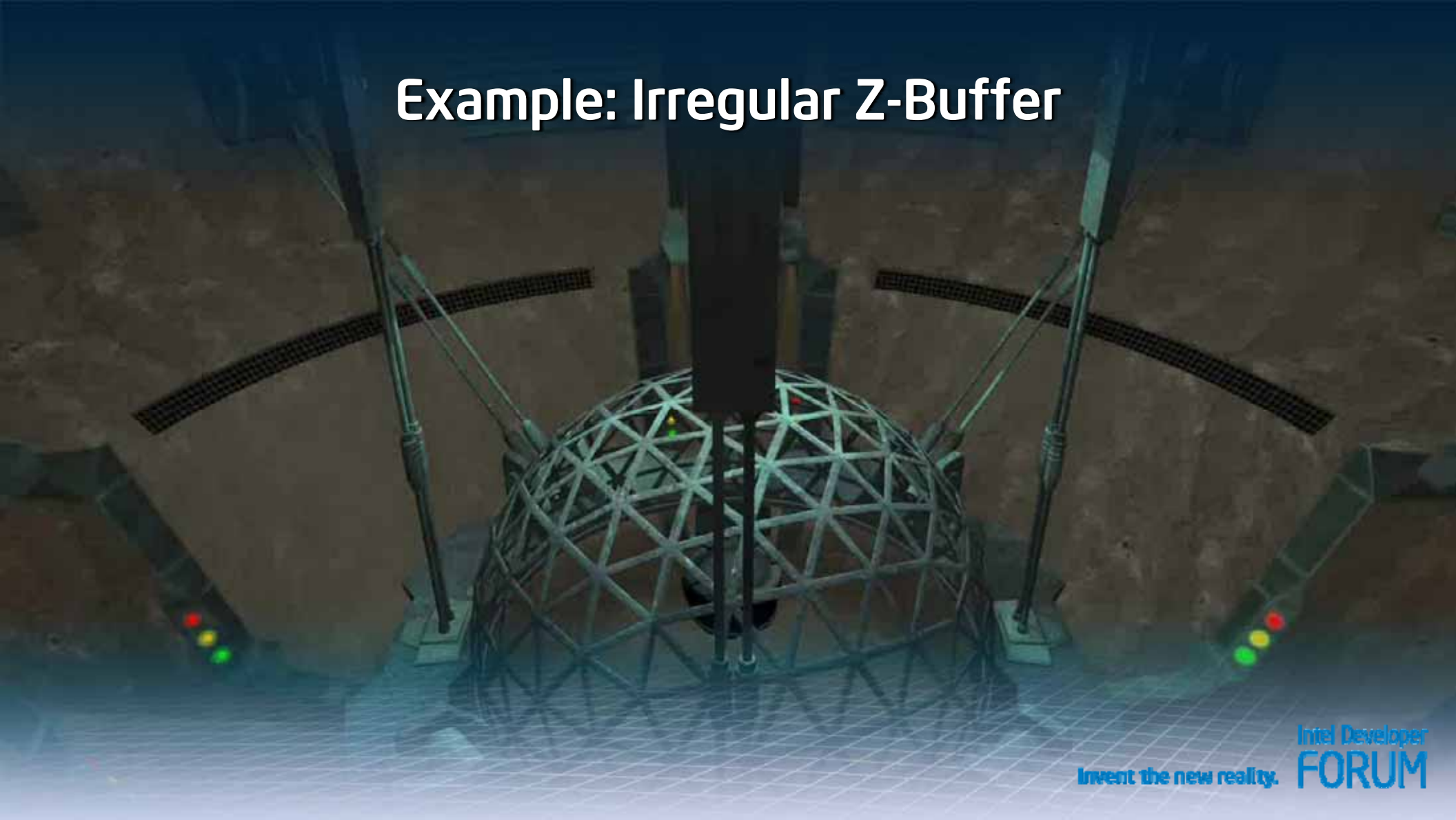
With Irregular Z-buffer, Clean Edge Details Are Always Rendered

Johnson, G., et al. 2005. *The irregular Z-Buffer: Hardware acceleration for irregular data structures.* ACM Transactions on Graphics, October 2005, ACM Press, New York, NY

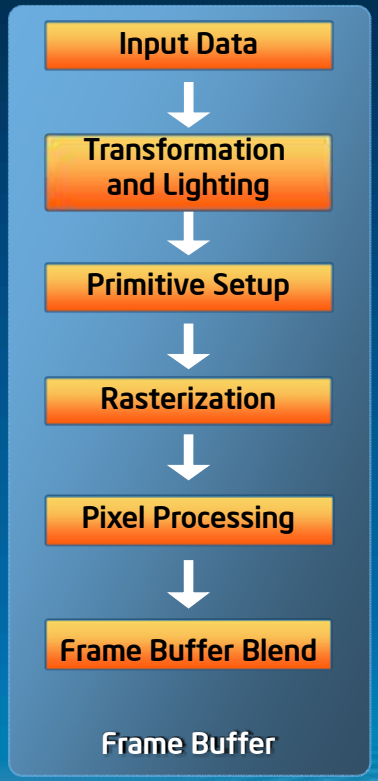
Example: Irregular Z-Buffer



Example: Irregular Z-Buffer



GPUs Are More Computationally Efficient?

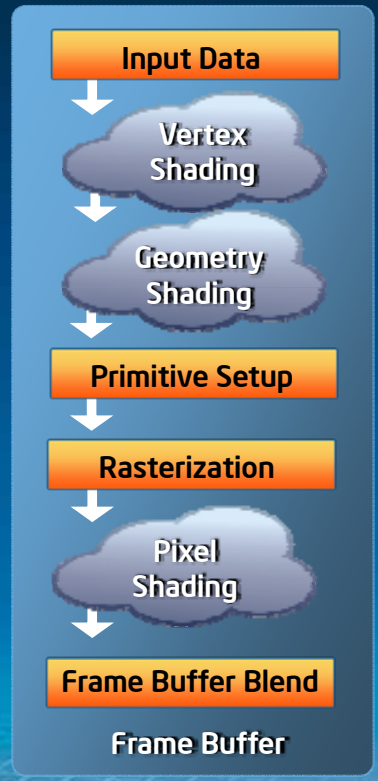


Pre 2001: Fixed Function

Early graphics processors
- Offloaded graphics from the CPU
- Simple, fixed function pipeline
- Many companies made products

GPU performance ramp
- 1.7x FLOPS increase per year *
- High computational density gained by increased parallelism
- Also by larger die & more power

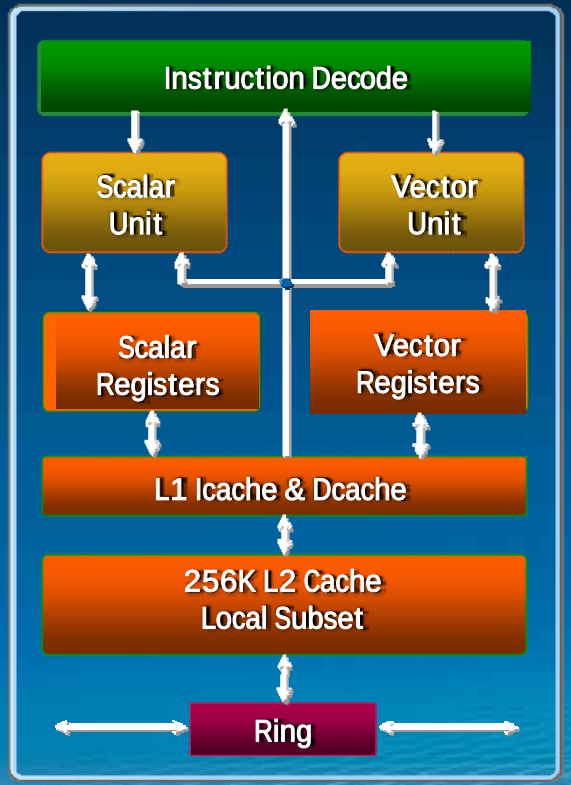
Changing graphics pipeline
- Programmable stages added
- Increasing design complexity
- Fewer companies involved



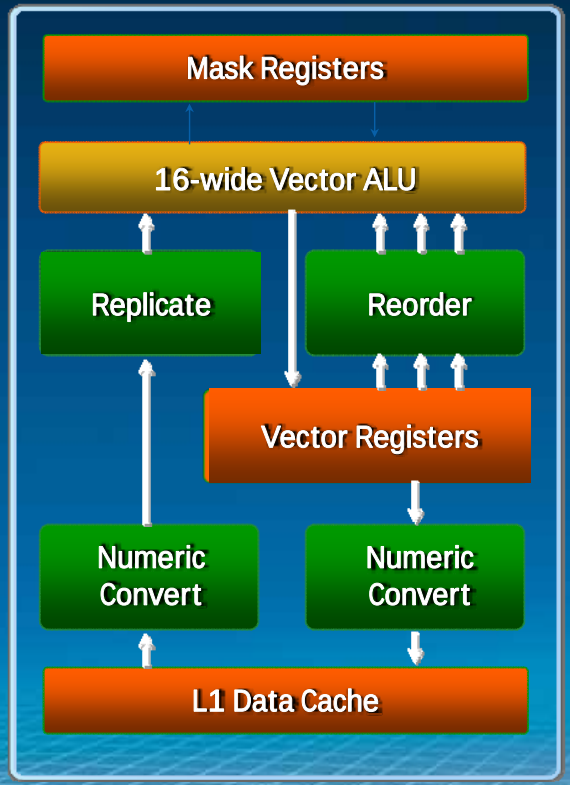
Post 2006: Programmable

* Data from John Owens, "Experiences with GPU Computing", 8th Annual IEEE/NATEA Conference, 2007 (see slide 12)

Larrabee: High Computational Density

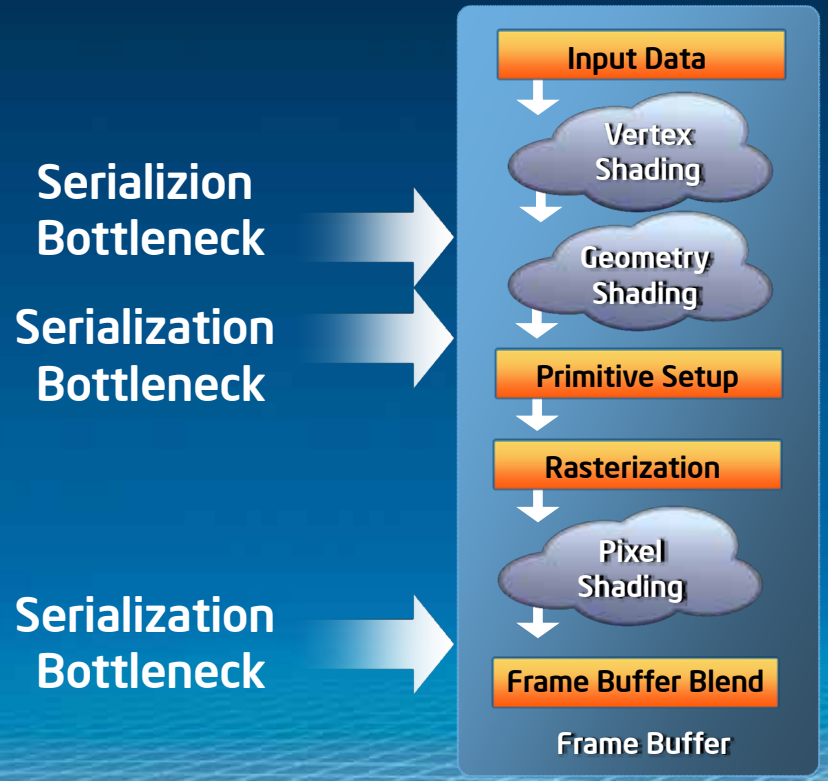


Larrabee CPU Core



Larrabee Vector Unit

Standard HW Rendering Pipeline Is Best?

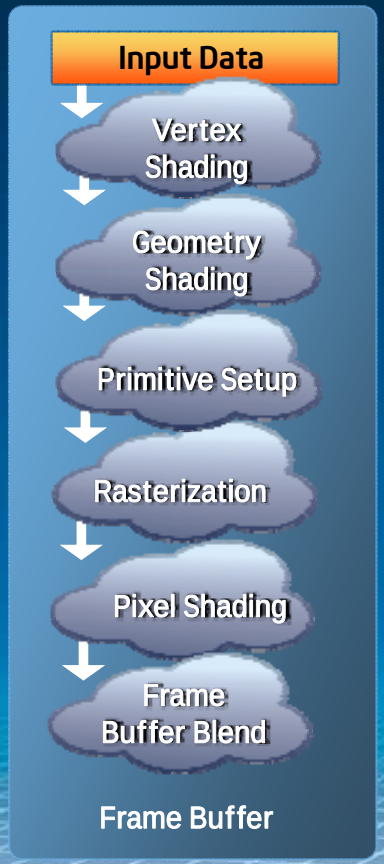


Larrabee: Removes Serialization Bottlenecks

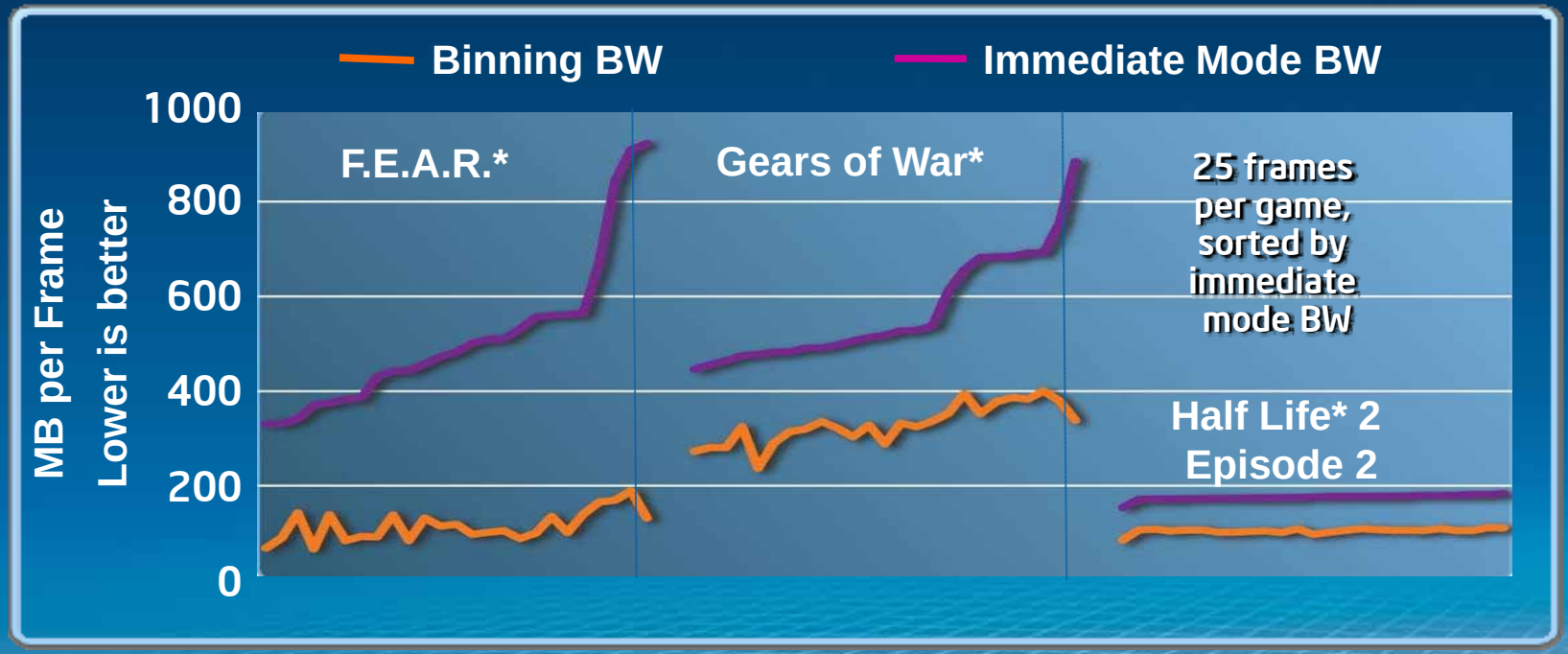
Synchronize
By Vertex Buffers

NO Serial Processing

Synchronize
By Tile Completion

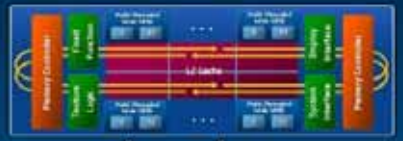


Larrabee Bandwidth: Binning Wins over Immediate!



Data in graph taken from Seiler, L., Carmean, D., et al. 2008. *Larrabee: A many-core x86 architecture for visual computing.* SIGGRAPH '08: ACM SIGGRAPH 2008 Papers, ACM Press, New York, NY

Graphics Processing Requires Programmability



Larrabee

Multi-core

Multi-threading

Single Thread

IA: Highly Programmable

Increasing Throughput Performance

Fully Programmable?

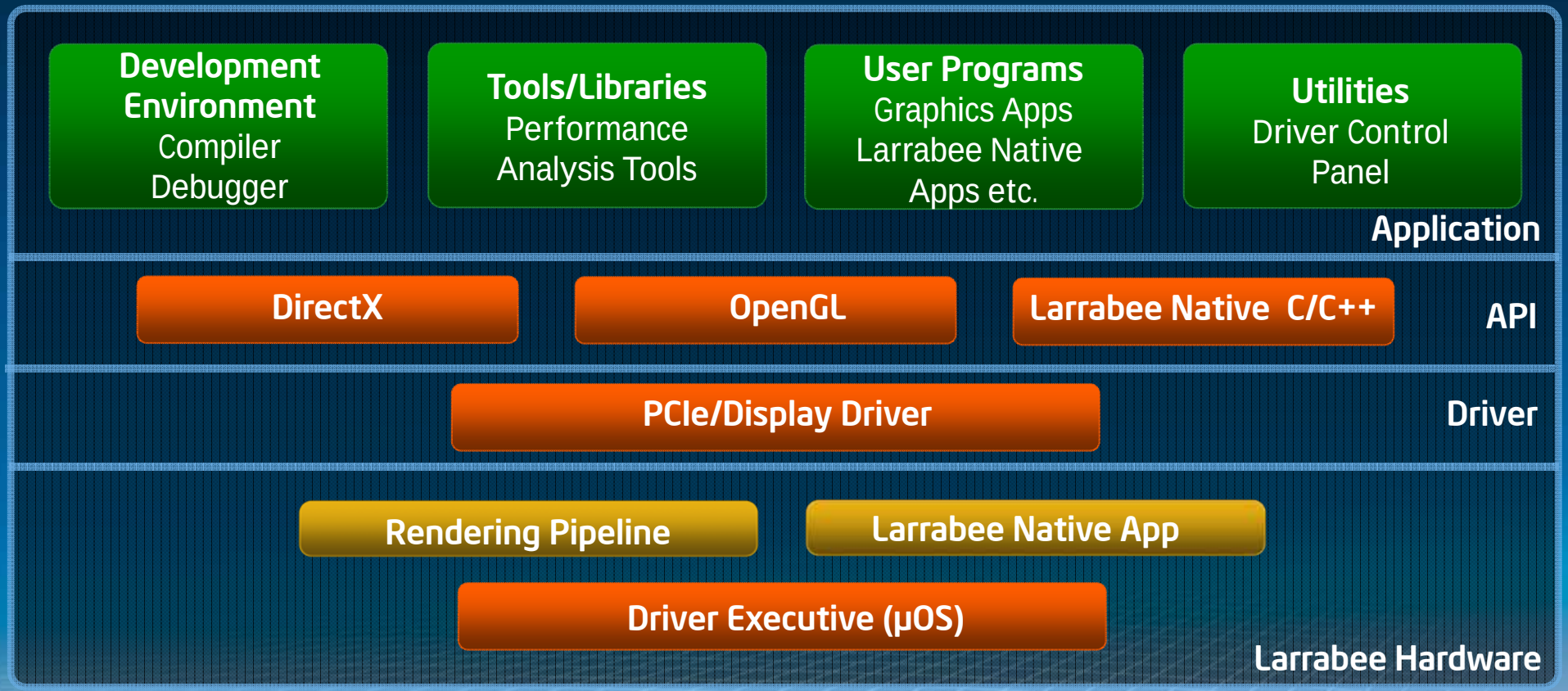
Partially Programmable

Fixed Function

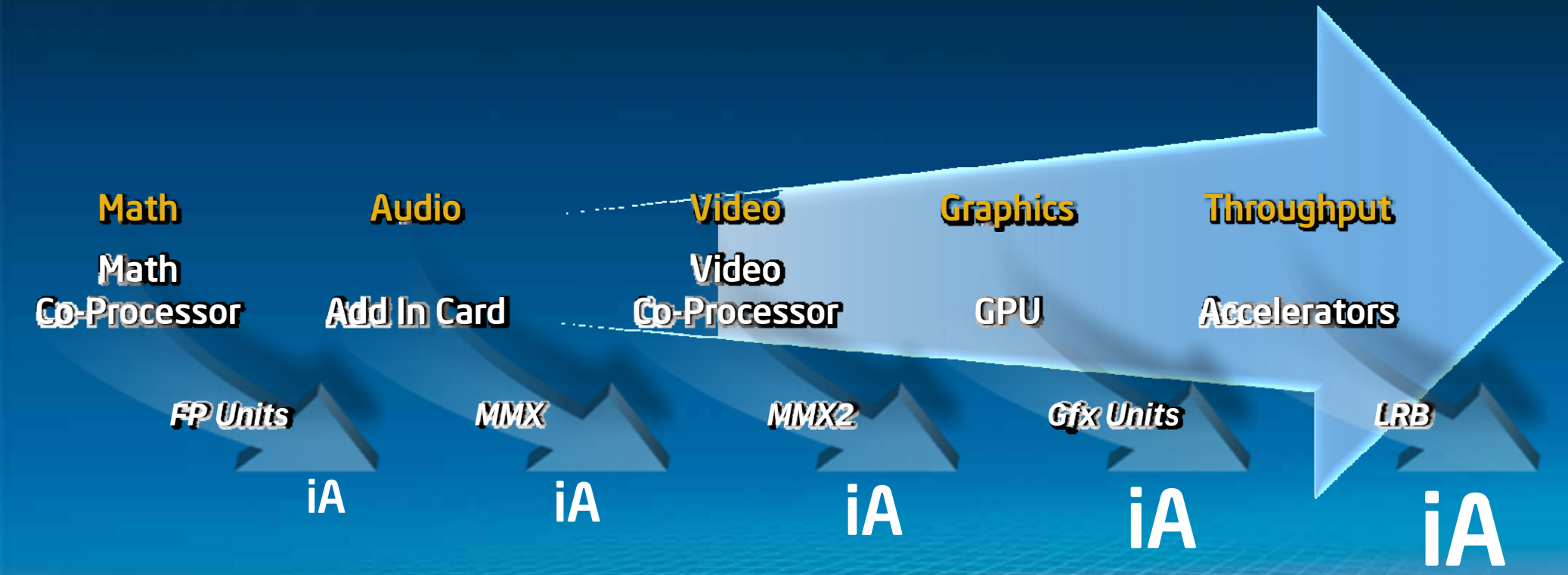
GPU: High Parallelism

Increasing Programmability

Larrabee: CPU-like Software Stack

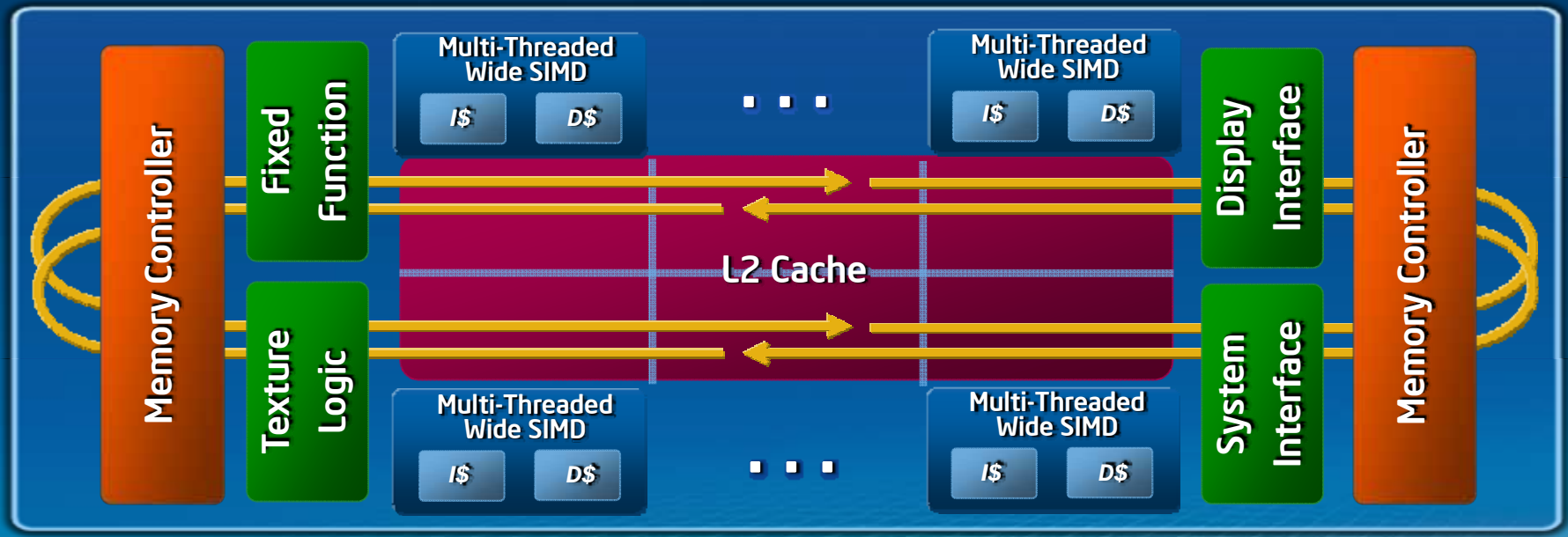


Intel Architecture Evolution



To Learn More About Larrabee, Please Attend

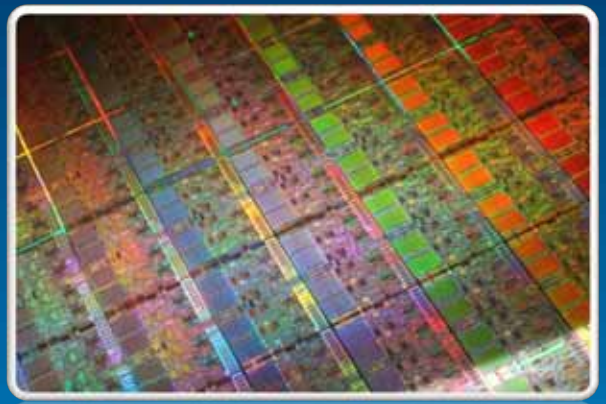
Wednesday	4:00 PM	Chalk Talk "Visual Computing Trends"
Thursday	10:10 AM	Larrabee: A Many-Core Intel® Architecture for Visual Computing



Larrabee: The Architecture For Visual Computing

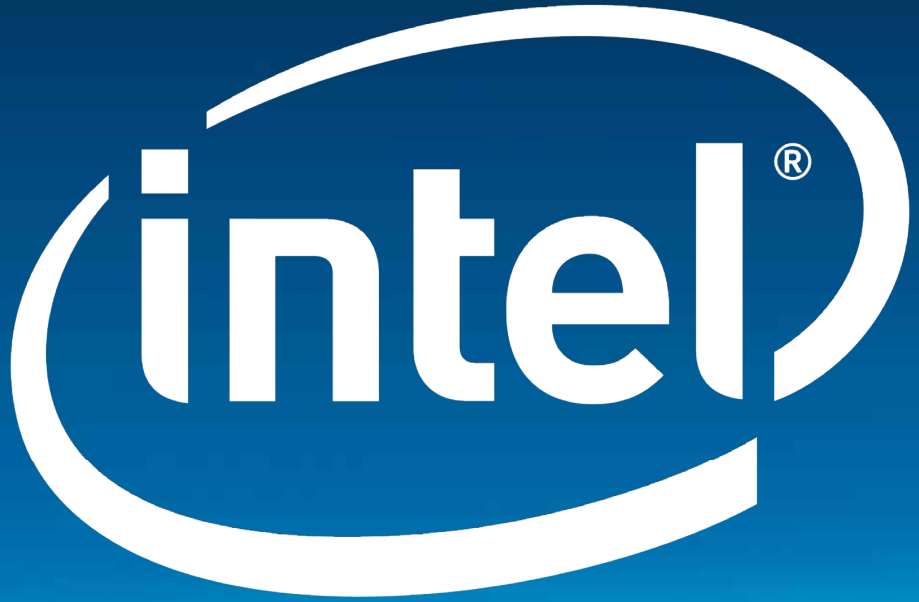
Intel Architecture =

Embedded +



Dynamic +

Visual


intel

Intel® Xeon® Processor 7400 Series Performance results
Configuration details

All results published/Submitted/Approved as of August 19, 2008.

Configuration Details:
4P SPECjbb*2005 details:
Intel Xeon processor X7460, platform details: Sun* Sun Fire* X4450 with four Intel Xeon X7460 (6-core, 16M cache, 2.66GHz, 1066FSB), 64 GB memory, Java* HotSpot* 32-bit Server VM on Solaris* v1.6.0P, Solaris* 10 10/08. Score 531,669; submitted Aug-2008. For more information see: http://www.spec.org/

4P SPECint*_rate2006 details:
Intel Xeon processor X7460, platform details: Fujitsu-Siemens* PRIMERGY* RX600 S4 with four Intel Xeon X7460 (6-core, 16M cache, 2.66GHz, 1066FSB), 16 GB (16 * 4GB Samsung* DDR2 5300F, 2 rank, CL5), 64-Bit SUSE* LINUX Enterprise S, Intel C++ Compiler for Linux32 and Linux64. Score 277, submitted Aug-2008. For more information see: http://www.spec.org/cpu2006/results

4P TPC Benchmark* E details:
Intel Xeon processor X7460, platform details: Dell* PowerEdge* R900 with four Intel Xeon processors model X7460 (6-core, 16M cache, 2.66GHz, 1066FSB), 128 GB memory, Microsoft* SQL Server* 2008 Enterprise x64-Edition, Microsoft* Windows* Server 2008 Enterprise x64-Edition. Submitted Aug-2008. For more information see: http://www.tpc.org. 4S/24C/24T, $500.55/tpsE. Availability Sep-08.

4P vConsolidate 1.1 on VMware* ESX Server 3.5 details: Result shown is a ratio of Xeon X7350 to Xeon X7460. Approved by Vmware – August 2008
Intel Xeon processor X7460, platform details: 4U Intel® S7000FC4UR (Fox Cove) Qual Server with four Intel Xeon X7460 (6-core, 16M cache, 2.66GHz, 1066FSB), 32GB memory (16 * 2GB FB-DIMM 667MHz Kingston* KVR667D2D4F5/4G), Fiber Channel Adapter: 2 * HBA Dual-Port QLE2462 PCIe* (one idle), Storage configuration: EMC* Clarion* CX3-40f 4Gb 15-slot array. Single RAID controller with 4 GB cache and a battery, dual PSMs with dual AC inputs. RAID 0, SAN: 10 * Hitachi* 146GB 15K RAID 0 FC HDD, 2 * DELTA DSP-1570BB, Fans: 8, VMware* ESX Server 3.5 Update 2 RC (Build 94067).

Intel Xeon processor X7350, platform details: 4U Intel® S7000FC4UR (Fox Cove) Qual Server with four Intel Xeon X7350 (Quad-Core, 8M cache, 2.93GHz, 1066FSB) , 32GB memory (16 * 2GB FB-DIMM 667MHz Kingston* KVR667D2D4F5/4G), Fiber Channel Adapter: 2 * HBA Dual-Port QLE2462 PCIe* (one idle), Storage configuration: EMC* Clarion* CX3-40f 4Gb 15-slot array. Single RAID controller with 4 GB cache and a battery, dual PSMs with dual AC inputs. RAID 0, SAN: 10 * Hitachi* 146GB 15K RAID 0 FC HDD, 2 * DELTA DSP-1570BB, Fans: 8, VMware* ESX Server 3.5 Update 1 GA (build 82663).

4P TPC Benchmark* C details:
Intel Xeon processor X7460, platform details: Hewlett-Packard* ProLiant* DL580 G5 Server with four Intel Xeon X7460 (6-core, 16M cache, 2.66GHz, 1066FSB), 256GB memory, Microsoft* SQL Server* 2005 Enterprise x64-Edition SP2, Microsoft* Windows* Server 2003 R2 Enterprise x64-Edition. 4P/24C/24T, Score 634,825 @ $1.10/tpmC. Submitted Aug-2008. Availability Sep-08.

8P TPC Benchmark* C details:
Intel Xeon processor X7460, platform details: IBM* System x* 3950 M2 with eight Intel Xeon X7460 (6-core, 16M cache, 2.66GHz, 1066FSB), 512 GB memory, IBM DB2 9.5, Red Hat* LINUX 5.2 (64-bit). Submitted Aug-2008. For more information see: http://www.tpc.org. 8S/48C/48T, $1.99/tpmC. Availability Oct-08.