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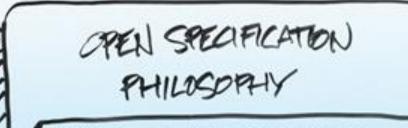
ALE.

BOB BAKER Senior Vice President General Manager,

Technology and Manufacturing Group





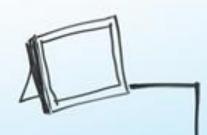


VITAN VINU CONNECTIVIT









Silicon Leadership: **Delivering Innovation**

Relentless Pursuit of Moore's Law

Innovations in Silicon Technology

Extending Leadership for New Opportunities



Moore's Law Still Drives Intel



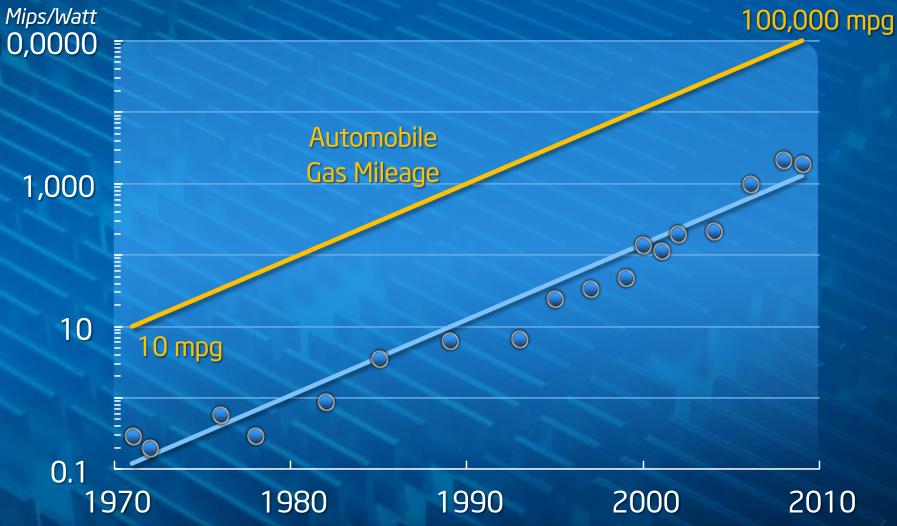
Source: WSTS/Dataquest/Intel

IDF2009

INTEL DEVELOPER FORUM

10¹⁰

Intel CPU Mips per Watt Trend



10,0000

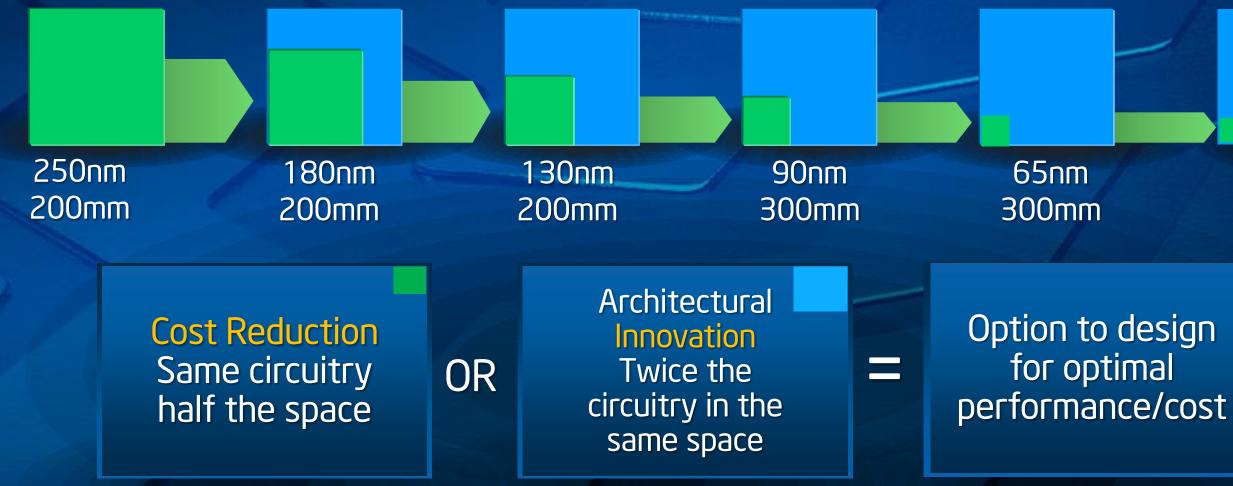
1,000

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If gas mileage improved as fast as CPU Mips/Watt, we'd have cars today with ~100,000 mpg



The Fundamental Driver of Cost and Innovation





45nm 300mm

45 nm Products Across the Board

Dual Core

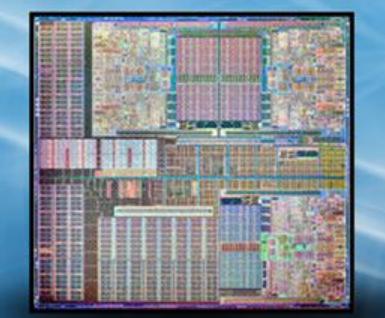
Single Core

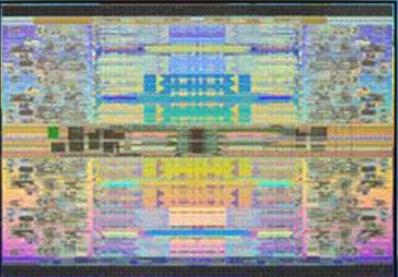






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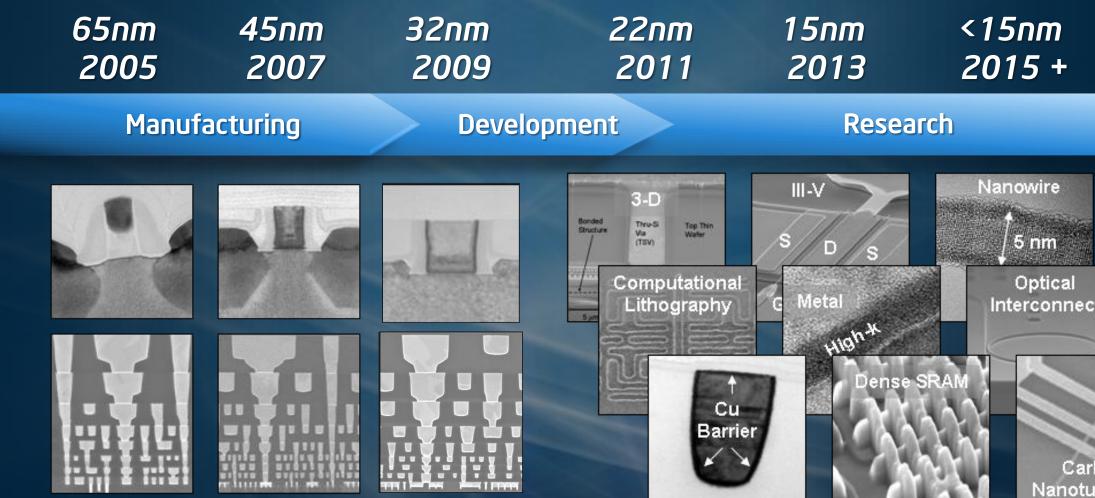


Revolutionary high-k + metal gate transistors >200 million units shipped





Innovation-Enabled Technology Pipeline: Researchers are Moving on to Investigation of Novel Technology Options

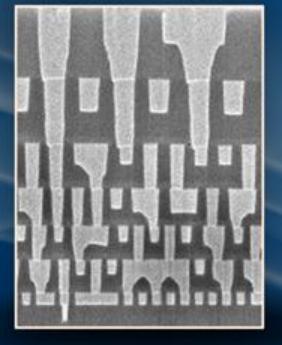




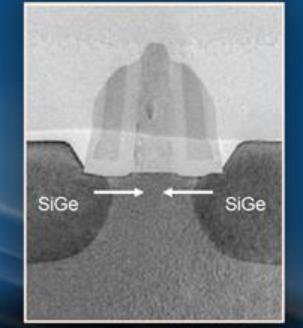
Interconnect

Carbon Nanotube FET

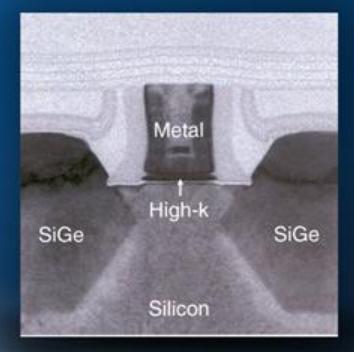
The New Era of Scaling



Copper + Low-k



Strained Silicon



High-k + Metal Gate



Modern CMOS scaling is as much about material innovation as dimensional scaling

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	55 Cs	56 Ba	57 La	72 Hf	73 Ta 180.9479	74 W	75 Re (Bostian) (86,207	76 Os	77 Ir 192,217	78 Pt	79 Au	80 Hg	81 TI 204.1813	82 Pb	83 Bi	84 P		other distances in the local distance in the	80 R = 0
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Jesús A. del Alamo

Home Team Research

Teaching Brief Bio Publications In the News Contact



lesús del Alamo is Donner Professor, MacVicar Faculty Felox and Professor af Electrical Engineering in the Department of Electrical Engineering and Computer Science Massachusetts institute of Technology

Prof. del Alamo leads a research program on 5i and compound serve underto transistor technologies for RF, incrosove and estimeter wave applications. His students have recently tabricated nanometer-scale transition with word record frequency operation. Prof. del Alamo is also investigating the use of 8-V compound seniconductors to

develop a new generation of deepty scaled transistors for future optal applications, Hs goals to elent Moore's law using 8-V semiconductors *

Prof. del Alamo is also engaged in exploring the technology and pedagogy of orene aboratories ("Laby") for science and engineering education. His team has developed laboratory set ups for electrical engineering education that have been accessed by thousands of students from around the word -

MIT MT. | EECS

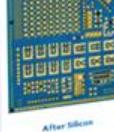
the Site Map Contact

technology laboratories.

Professor Jesus del Alamo **Professor of Electrical Engineering**

Donner Professor, MacVicar Faculty Fellow Department of Electrical Engineering and Computer Science

Massachusetts Institute of Technology

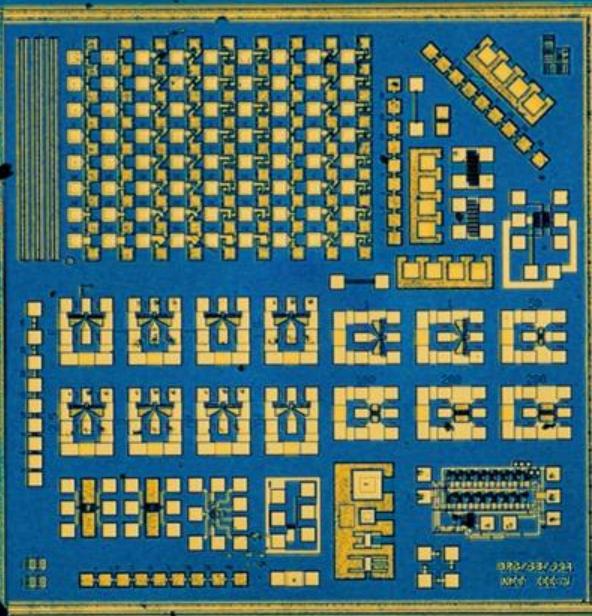




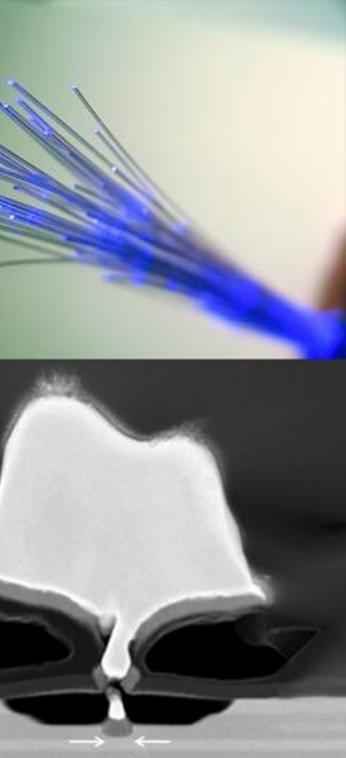


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<u>0.1 µ</u>m





Continuing Moore's Law

Scaling Enables Lower Cost and Higher Capability

Opportunities to Extend Moore's Law

Researchers Doing Innovative Work





Silicon Leadership: **Delivering Innovation**

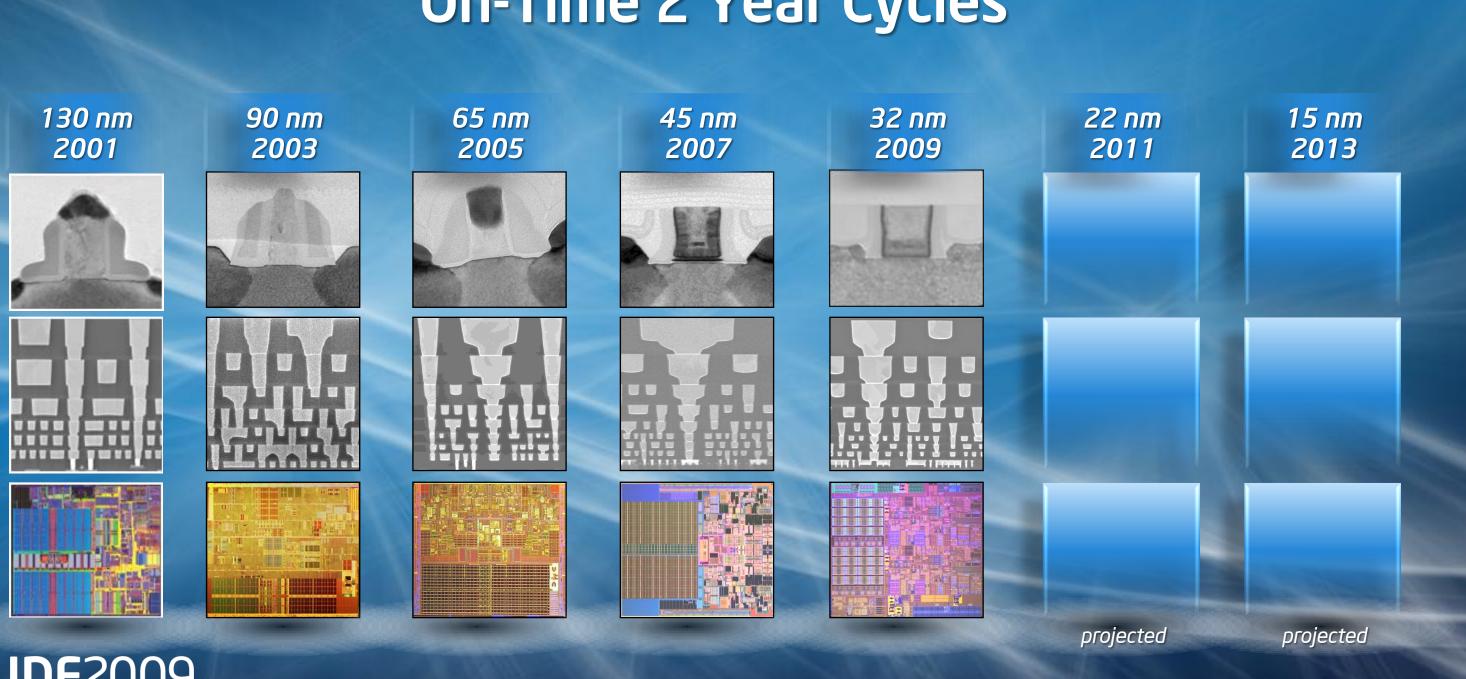
Relentless Pursuit of Moore's Law

Innovations in Silicon Technology

Extending Leadership for New Opportunities



On-Time 2 Year Cycles



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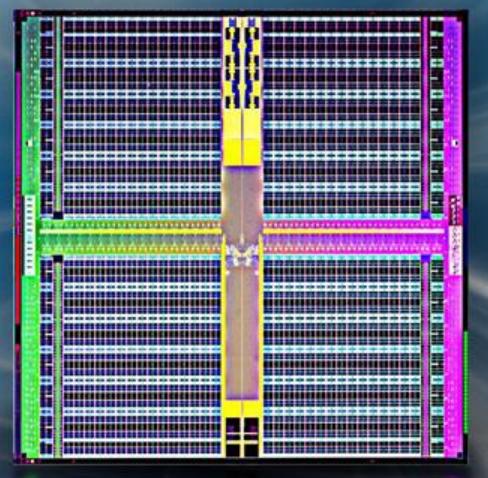
32nm - Extending Technology Leadership

Industry-leading features:

- 2nd generation high-k/metal gate transistors
- 4th generation strained silicon
- Highest reported drive currents
- 0.7x pitch scaling enables 50% area reduction

First to demonstrate working 32nm processors

Intel's 32 nm process is certified for production



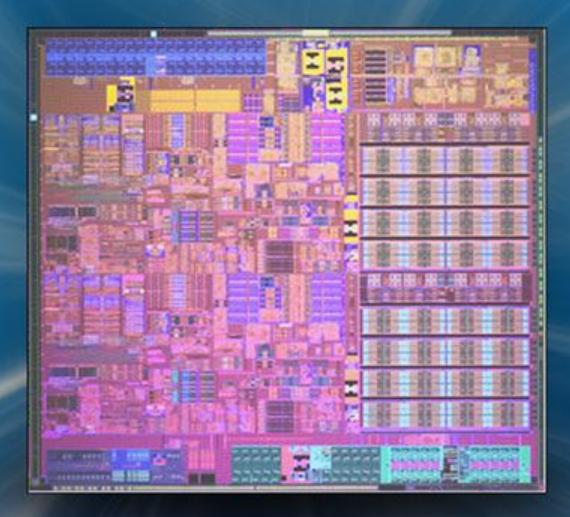
291 Mbit SRAM >1.9 billion transistors





0.171 um2 cell size 3.8 GHz operation

32 nm Westmere Microprocessor in Production





CPU wafers are moving through the factory in support of planned Q4 revenue production

32nm Manufacturing Fabs: \$7B Investment Over 2 Years







Fab 32 Arizona

INTEL DEVELOPER FORUM







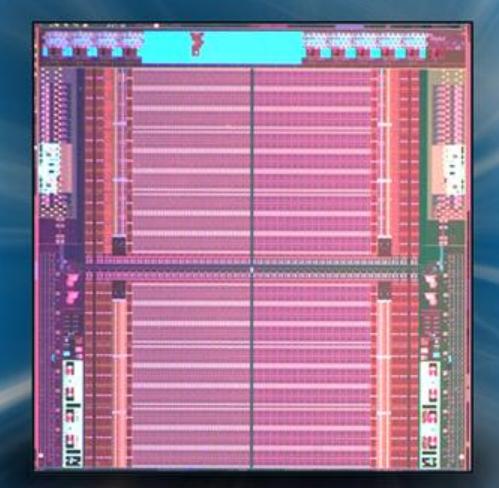
Fab 11*X* New Mexico

The World's First 22 nm SRAM





The World's First 22 nm SRAM



364 Mbit array size

>2.9 billion transistors

3rd generation high-k + metal gate transistors

Same transistor and interconnect features as on 22 nm CPUs



Demonstrating working 22 nm SRAMs is an important milestone towards building working 22 nm microprocessors





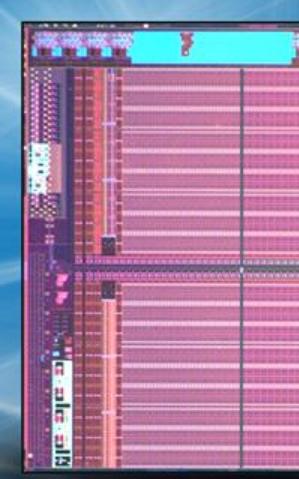
22 nm Optimized for Wide Range of Applications

High density 0.092 um² SRAM cell



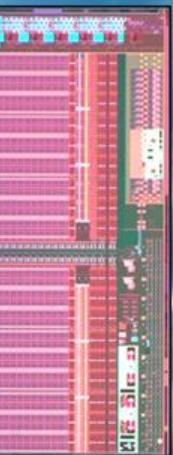
Low voltage 0.108 um² SRAM cell





0.092 um2 is the smallest SRAM cell in working circuits reported to date





Silicon Leadership: **Delivering Innovation**

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New Segment Opportunities: Internet Connected Devices



CE

Embedded





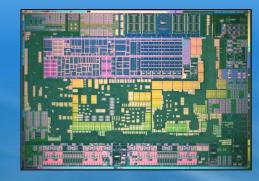
New Segments Require New Technology and Manufacturing Capabilities

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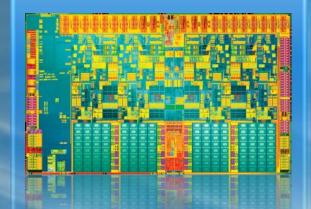
Source: Intel

45nm SoCs

CE Sodaville



Embedded Jasper Forest





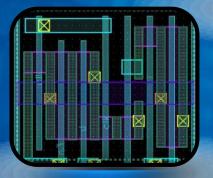
Initial 45 nm Intel[®] processor based SoC products



Source: Intel

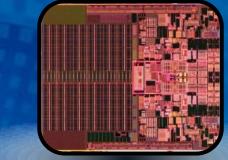
Integrated Device Manufacturer Advantage

Process



Design Tools

Design for Manufacturing **Co-Optimized Process + Product** Rapid Yield Learning Early Product Ramp



Product



Manufacturing

Masks





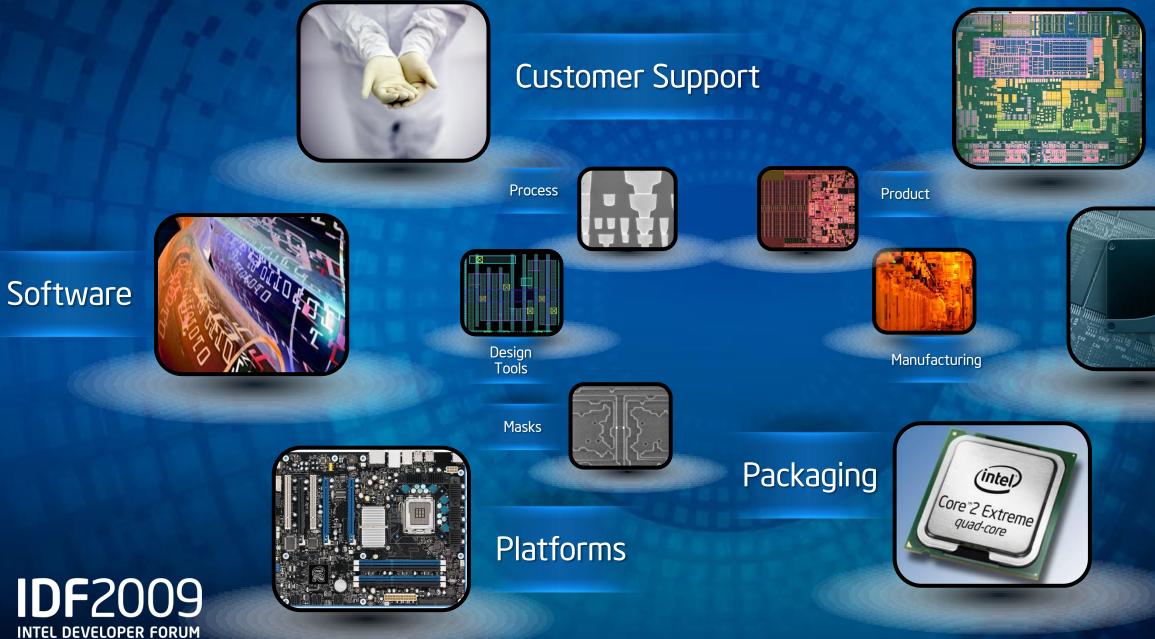


Packaging





Expanded Support for New Opportunities





SoCs



Метогу

SoC Process Builds on CPU Process

	45	5nm	32	nm	
	2007	2008	2009	2010	201
Process:	P1266	P1266.8	P1268	P1269	P12
Products:	CPU	SoC	CPU	SoC	CP
	P1266	P1266.8	P1268	P1269	Ρ1

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CPU and SoC versions of each process generation to provide transistors, interconnects and other device features optimized for each product line



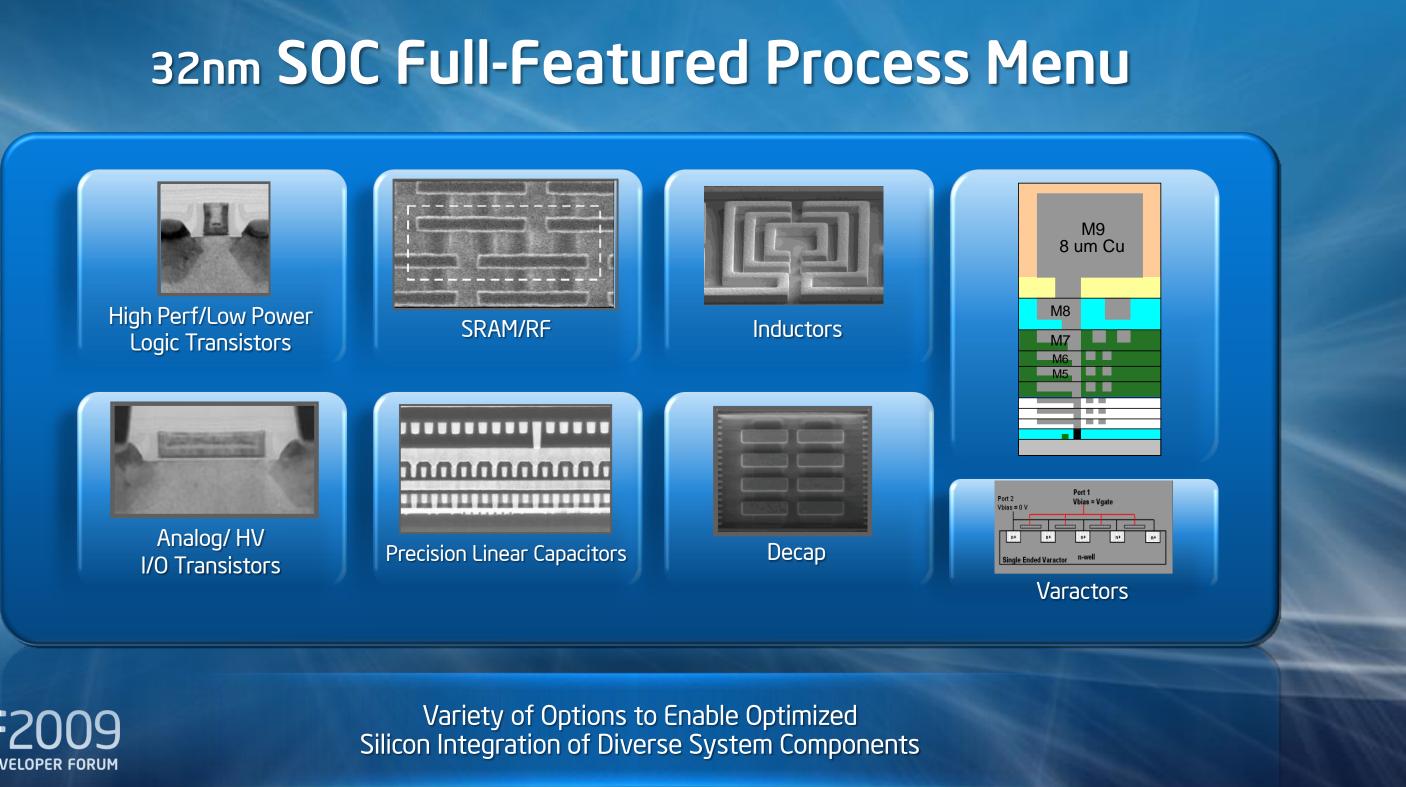
22nm

2012

P1271 70

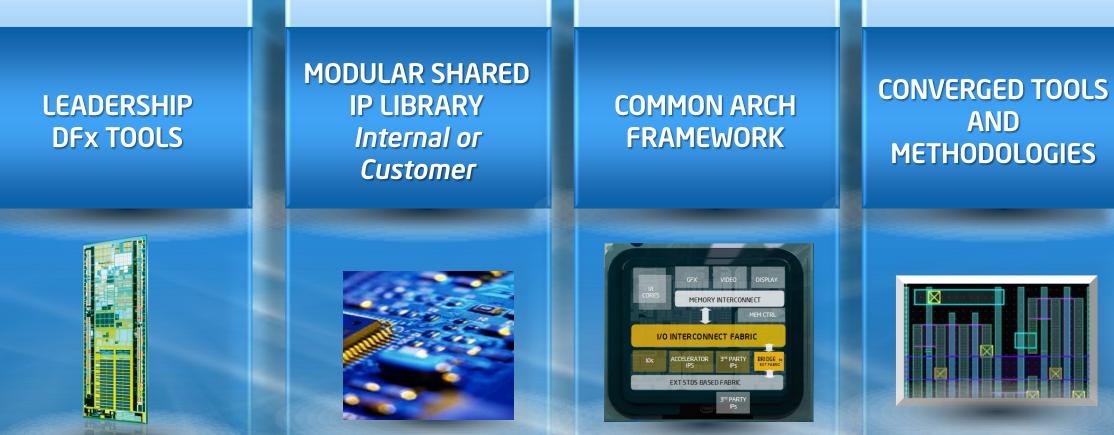
U

SoC





SoC Design and Manufacturing Tools Benefits: Time to Market, Modularity, Flexibility, Customization



Soc DESIGN TECHNOLOGY LAYER

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Intel 32nm Package Options: Enabling SOC Optimization in Integration, Form Factor and Cost

MCP FCBGA 2mm thick

DISCRETE FCMB <1 mm thick

SINGLE DIE FCBGA 1.6mm thick

> **POP FCMB** < 0.8 mm thick



0 000 000



Faster Factories Enable Improved Customer Response

Better Commitment

Faster Factories

62% CYCLE TIME REDUCTION

Cycle Time Days

2006

2007

2008

2009



Quicker Order to Delivery



Faster Factories Enable Improved Customer Response

Faster Factories

Better Commitment

BX INCREASE IN YES IN ONE DAY

2007

2008

2009



-

Quicker Order to Delivery



Faster Factories Enable Improved Customer Response

Faster Factories

Better Commitment

25% **IMPROVEMENT IN LESS THAN A YEAR**

July

2008

December January

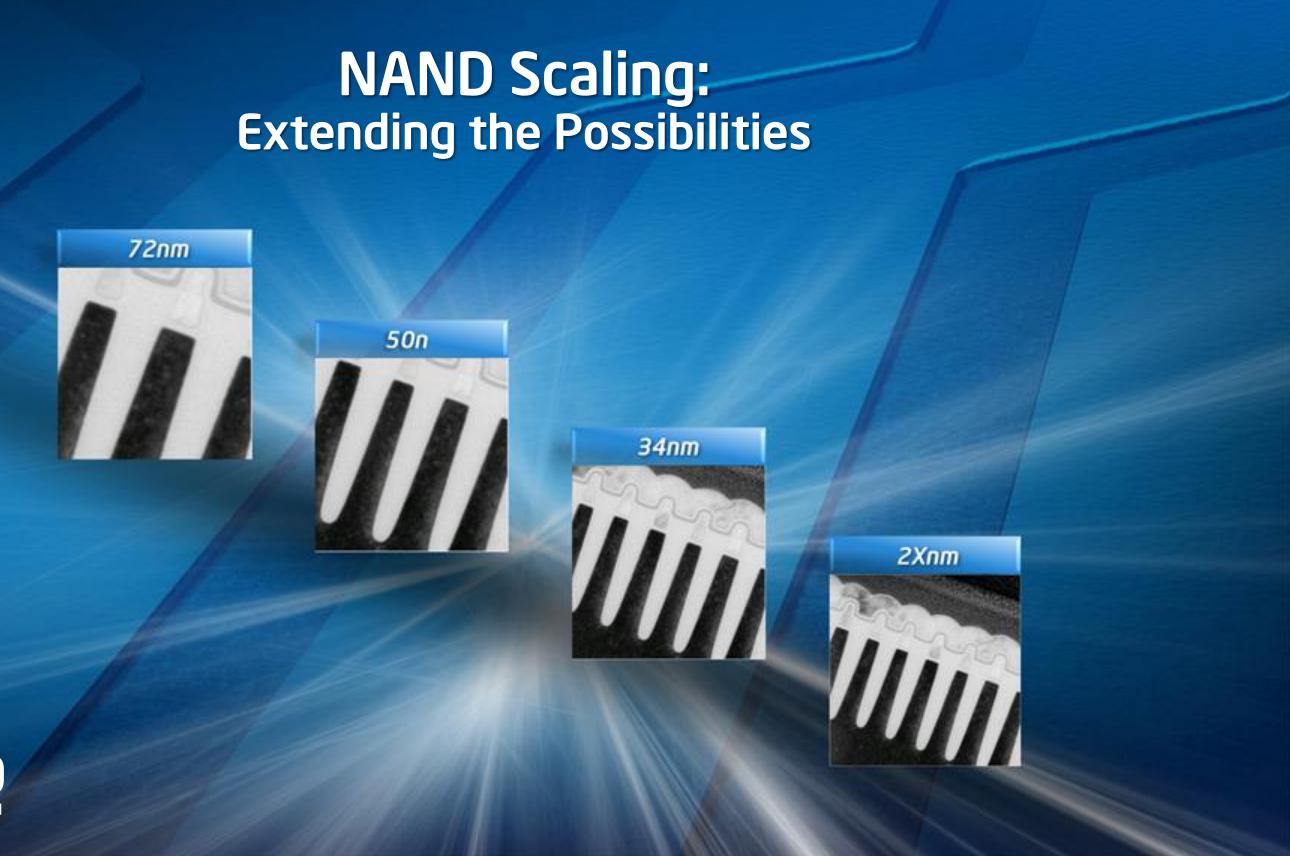
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Quicker Order to Delivery









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Intel® X25-E Extreme SATA Solid-State Drive

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Rick Coulson Intel Senior Fellow

Director, Storage Technologies Technology and Manufacturing Group

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Platform Co-Optimizations with SSDs

SSDs benefit existing platforms

Storage subsystems lag

Co-optimizing SSDs and platform Improves performance, scalability, power efficiency, total cost

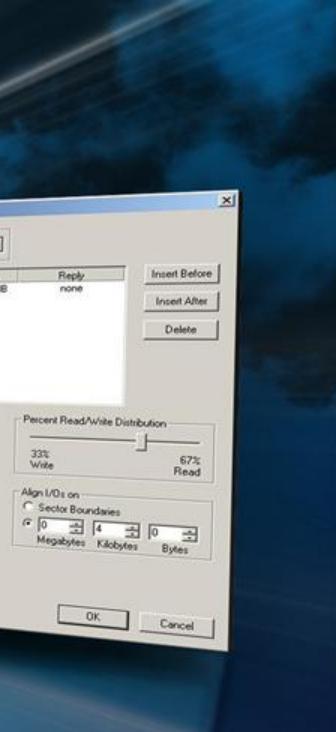




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In Closing...

Relentless Pursuit of Moore's Law

Innovations in Silicon Technology

Extending Leadership for New Opportunities



Sponsors of Tomorrow.