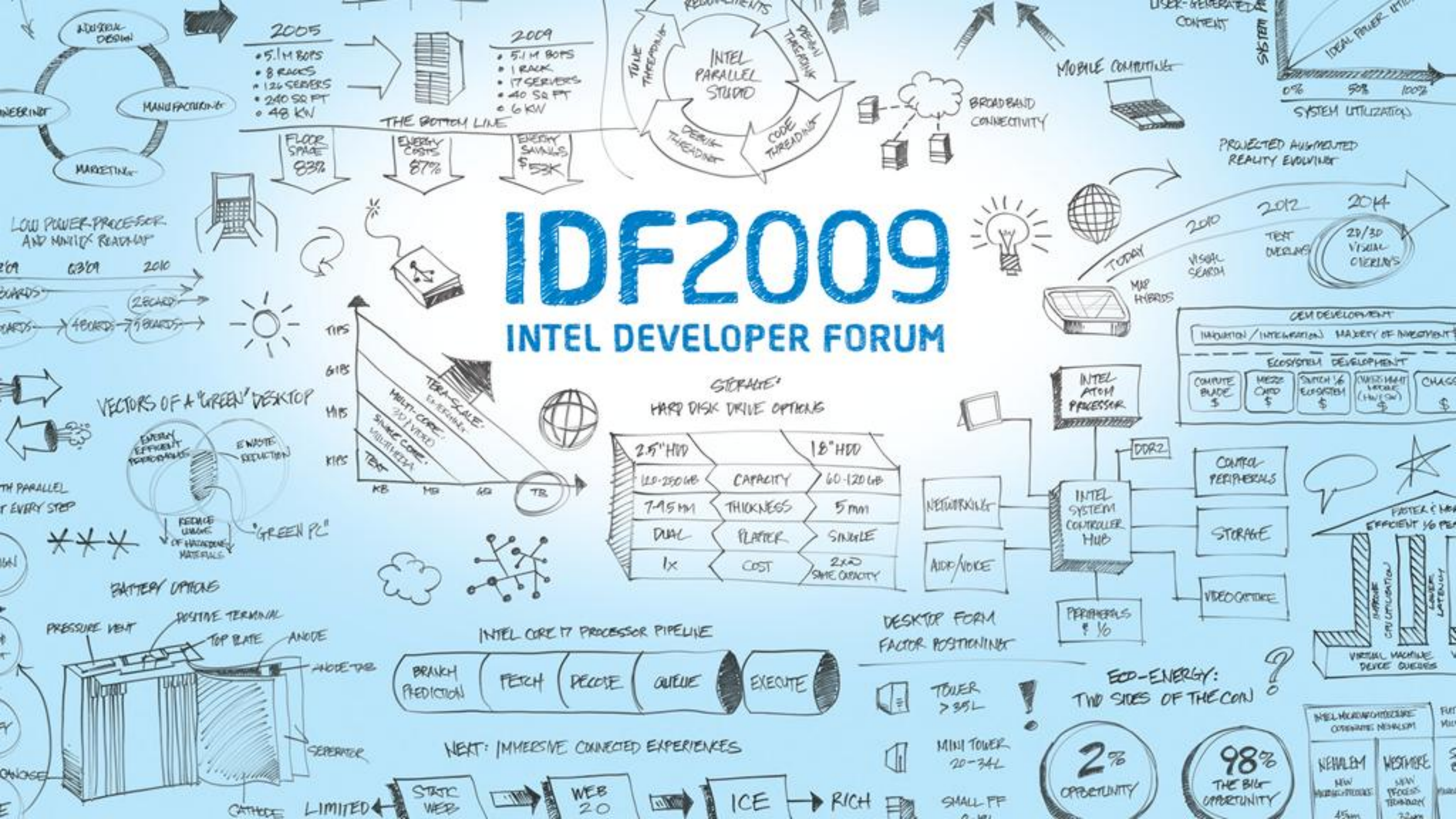
IDF2009
INTEL DEVELOPER FORUM
INDUSTRIAL DESIGN
MANUFACTURING
MARKETING
2005
• 5.1M BOPS
• 8 RACKS
• 126 SERVERS
• 240 SQ FT
• 48 KW
2009
• 5.1M BOPS
• 1 RACK
• 17 SERVERS
• 40 SQ FT
• 6 KW
THE BOTTOM LINE
FLOOR SPACE 83%
ENERGY COSTS 87%
ENERGY SAVINGS $53K
INTEL PARALLEL STUDIO
REQUIREMENTS
DESIGN THREADING
CODE THREADING
DEBUG THREADING
TUNE THREADING
MOBILE COMPUTING
BROADBAND CONNECTIVITY
USER-GENERATED CONTENT
IDEAL POWER
SYSTEM UTILIZATION
0%
50%
100%
PROJECTED AUGMENTED REALITY EVOLVING
TODAY
2010
2012
2014
MAP HYBRIDS
VISUAL SEARCH
TEXT OVERLAYS
2D/3D VISUAL OVERLAYS
LOW POWER PROCESSOR AND MINI ITX ROADMAP
2010
VECTORS OF A "GREEN" DESKTOP
ENERGY EFFICIENT PERFORMANCE
E-WASTE REDUCTION
REDUCE USAGE OF HAZARDOUS MATERIALS
"GREEN PC"
TIPS
GIPS
MIPS
KIPS
KB
MB
GB
TB
TERA-SCALE
MULTI-CORE
SINGLE CORE
STORAGE:
HARD DISK DRIVE OPTIONS
2.5" HDD
1.8" HDD
160-250 GB
CAPACITY
60-120 GB
7-9.5 MM
THICKNESS
5 mm
DUAL
PLATTER
SINGLE
1x
COST
2x SAME CAPACITY
OEM DEVELOPMENT
ECOSYSTEM DEVELOPMENT
COMPUTE BLADE $
MEZZ CARD $
INTEL ATOM PROCESSOR
DDR2
NETWORKING
AUDIO/VOICE
INTEL SYSTEM CONTROLLER HUB
CONTROL PERIPHERALS
STORAGE
VIDEO CAPTURE
PERIPHERALS & I/O
BATTERY OPTIONS
PRESSURE VENT
POSITIVE TERMINAL
TOP PLATE
ANODE
ANODE TAB
SEPERATOR
CATHODE
INTEL CORE I7 PROCESSOR PIPELINE
BRANCH PREDICTION
FETCH
DECODE
QUEUE
EXECUTE
NEXT: IMMERSIVE CONNECTED EXPERIENCES
LIMITED
STATIC WEB
WEB 2.0
ICE
RICH
DESKTOP FORM FACTOR POSITIONING
TOWER > 35L
MINI TOWER 20-34L
SMALL FF
ECO-ENERGY:
TWO SIDES OF THE COIN
2% OPPORTUNITY
98% THE BIG OPPORTUNITY
NEHALEM
WESTMERE
VIRTUAL MACHINE DEVICE QUEUES

BOB BAKER

Senior Vice President
General Manager,
Technology and Manufacturing Group

Silicon Leadership:
Delivering Innovation

Relentless Pursuit of Moore's Law

Innovations in Silicon Technology

Extending Leadership for New Opportunities

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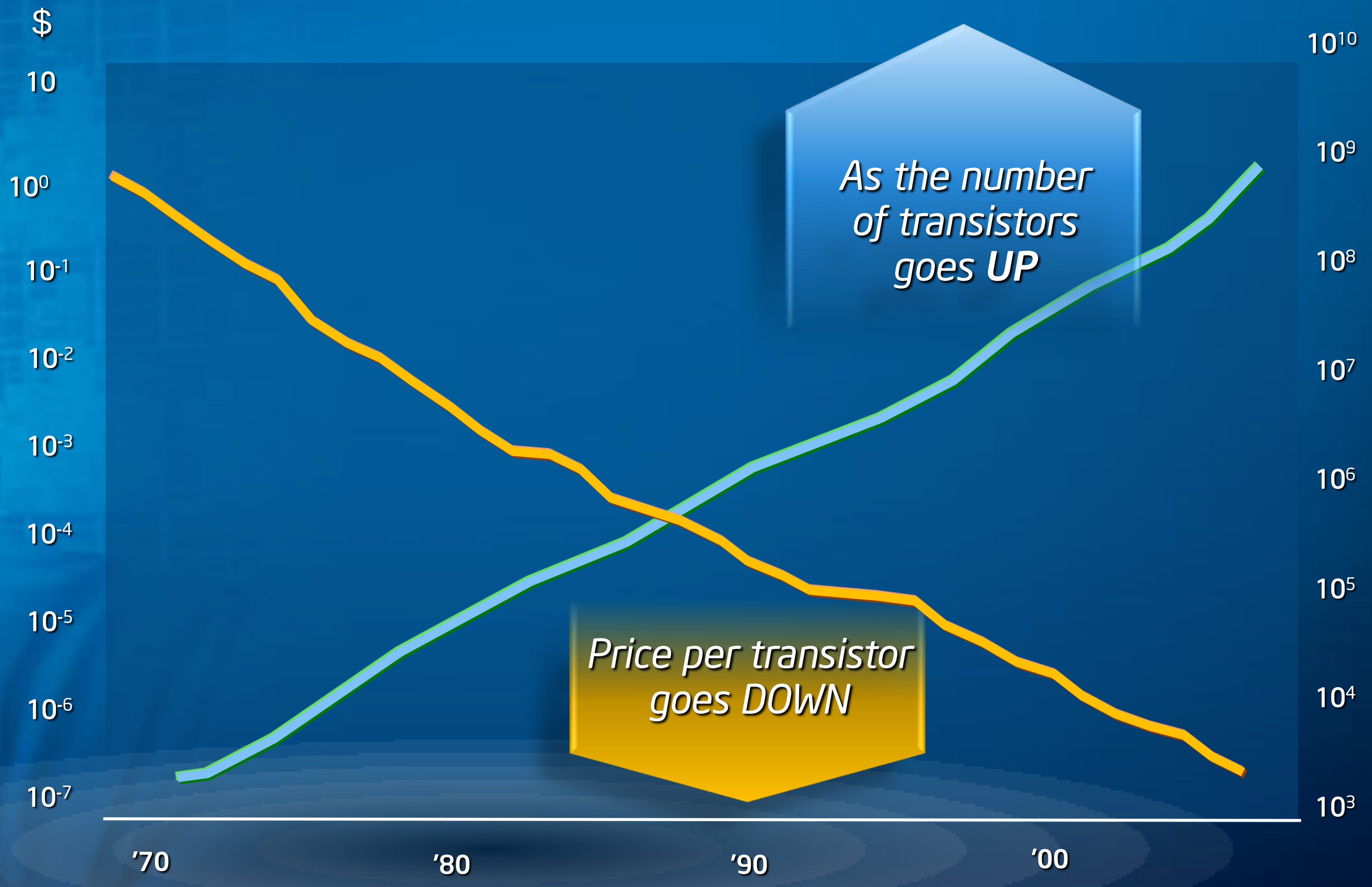
Moore's Law Still Drives Intel



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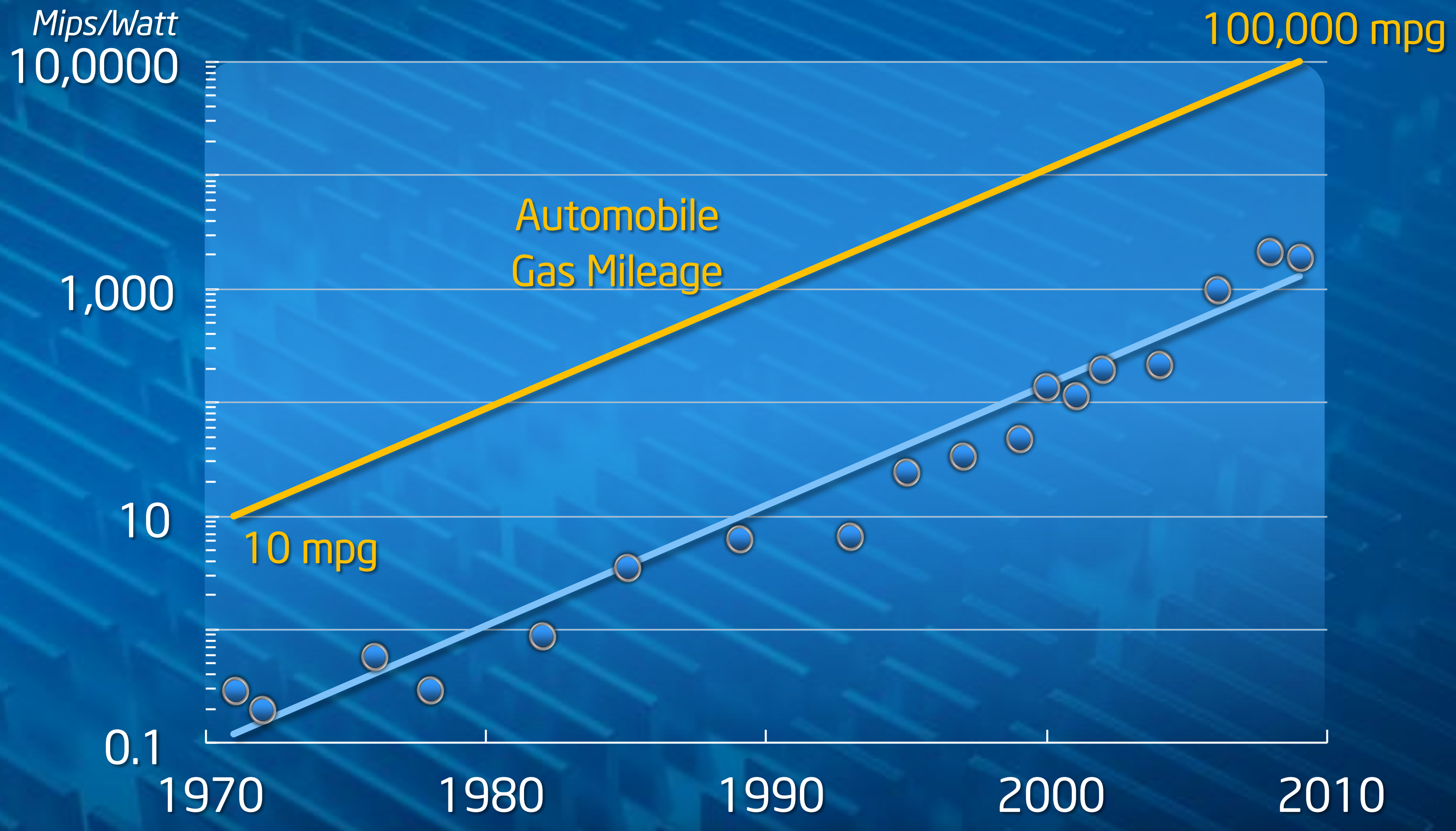
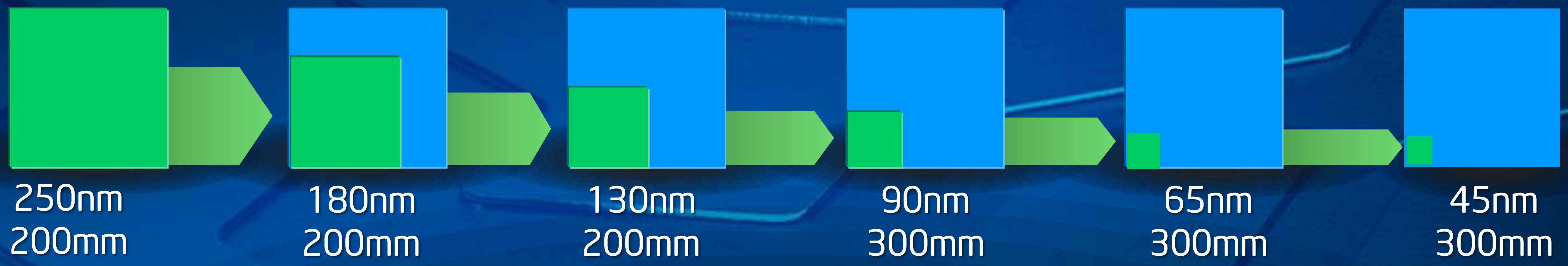
Source: WSTS/Dataquest/Intel

Intel CPU Mips per Watt Trend



If gas mileage improved as fast as CPU Mips/Watt,
we'd have cars today with ~100,000 mpg

The Fundamental Driver of Cost and Innovation



Cost Reduction
Same circuitry half the space

OR

Architectural **Innovation**
Twice the circuitry in the same space

=

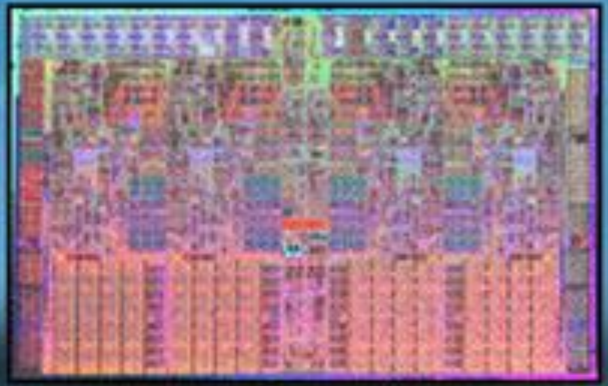
Option to design for optimal performance/cost

Source: Intel

45 nm Products Across the Board

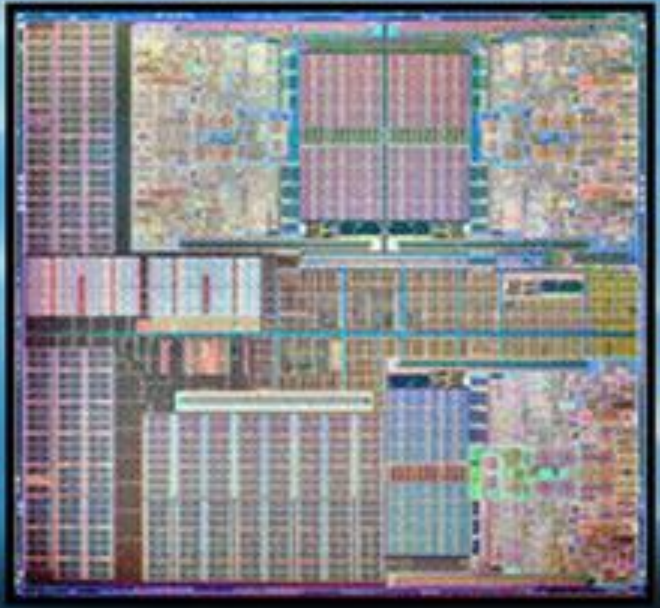
Single Core

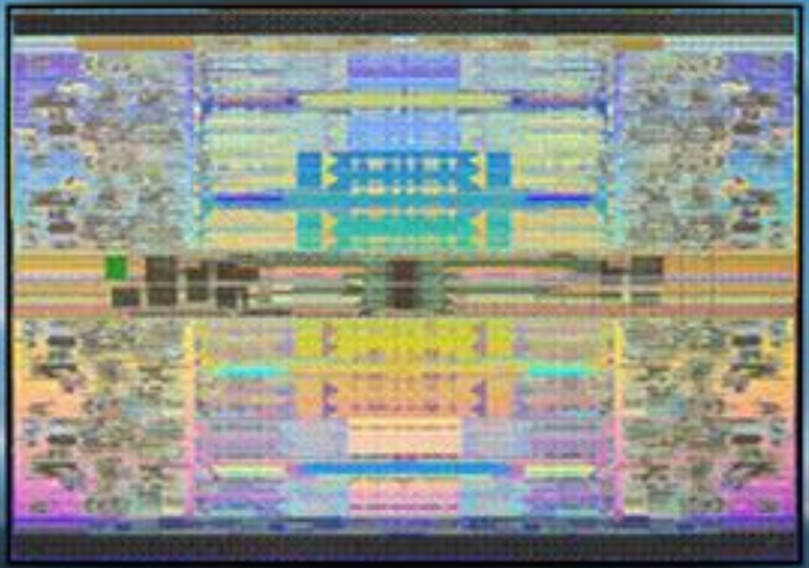
Dual Core



Quad Core

6 Core





8 Core

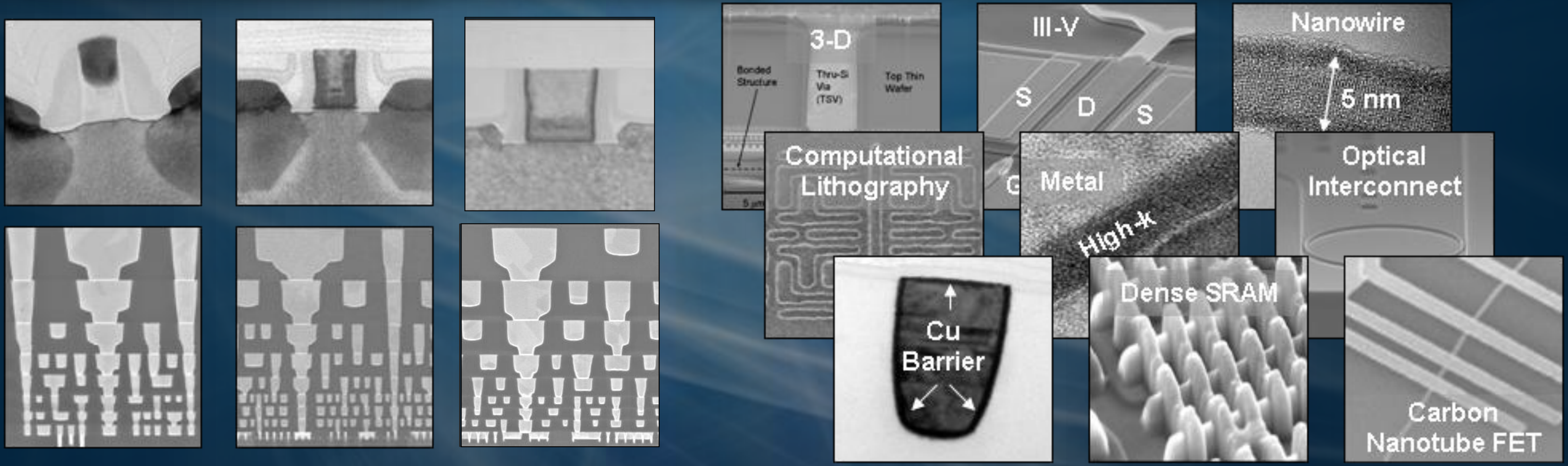
Revolutionary high-k + metal gate transistors
>200 million units shipped

Innovation-Enabled Technology Pipeline:

Researchers are Moving on to Investigation of Novel Technology Options

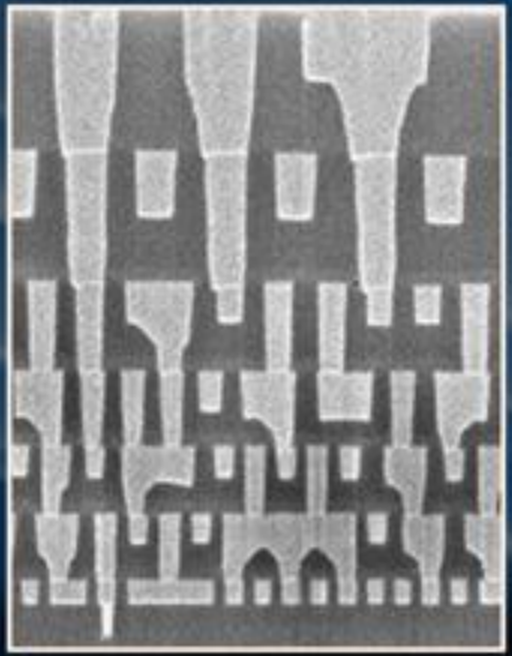
65nm	45nm	32nm	22nm	15nm	<15nm
2005	2007	2009	2011	2013	2015 +

Manufacturing → Development → Research

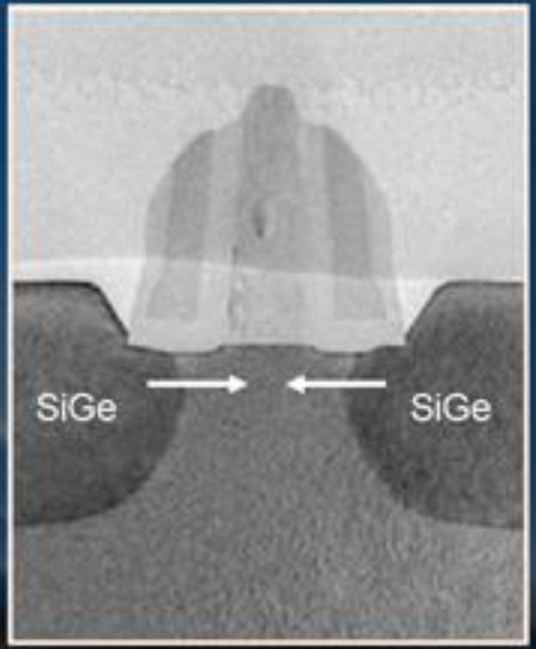


Future options subject to change

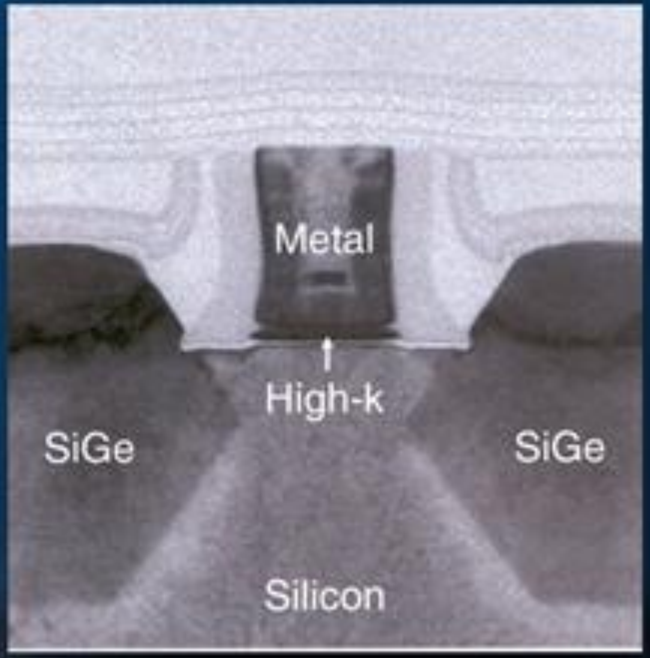
The New Era of Scaling



Copper + Low-k



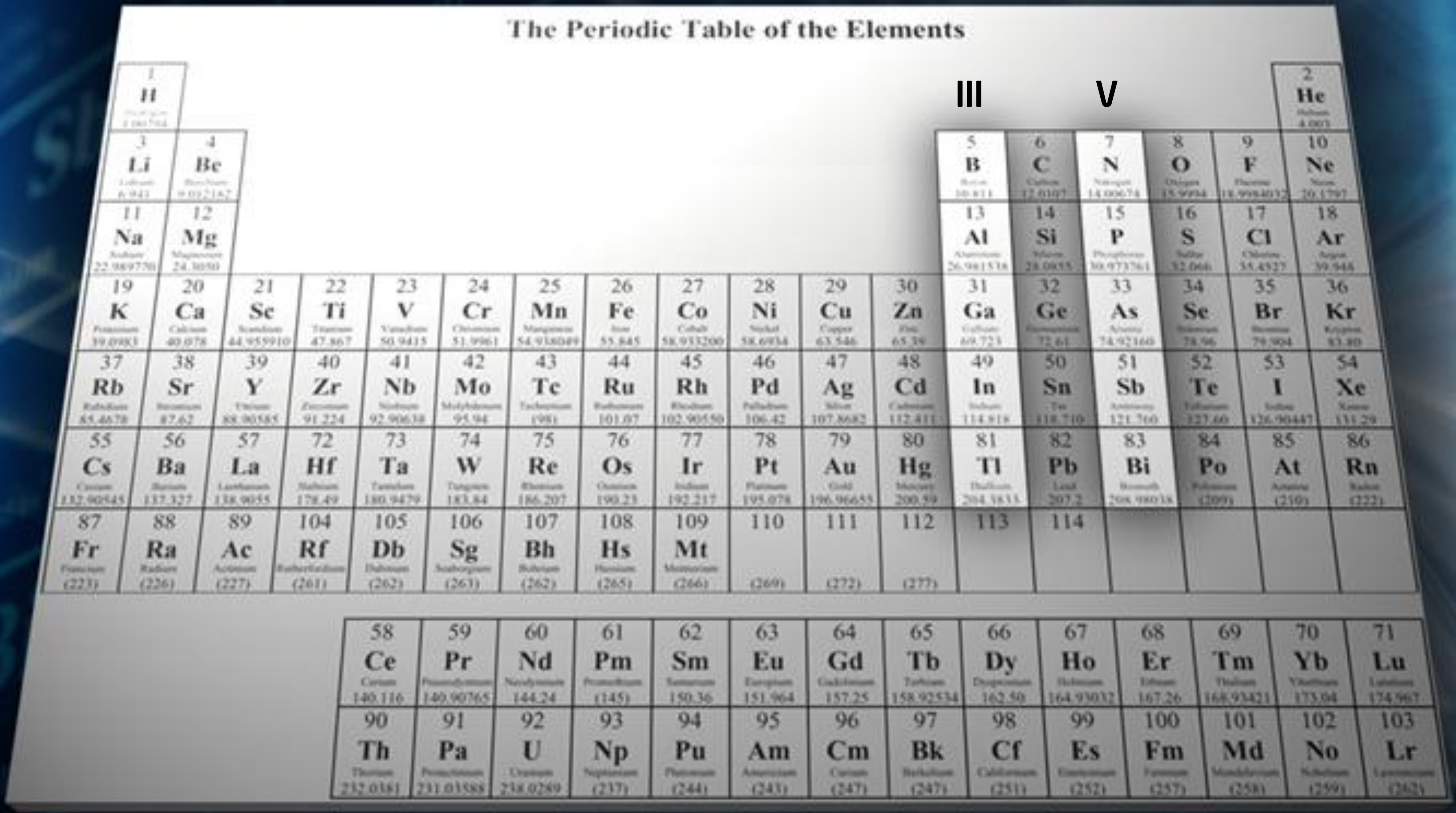
Strained Silicon



High-k + Metal Gate

Modern CMOS scaling is as much about material innovation as dimensional scaling

III-V

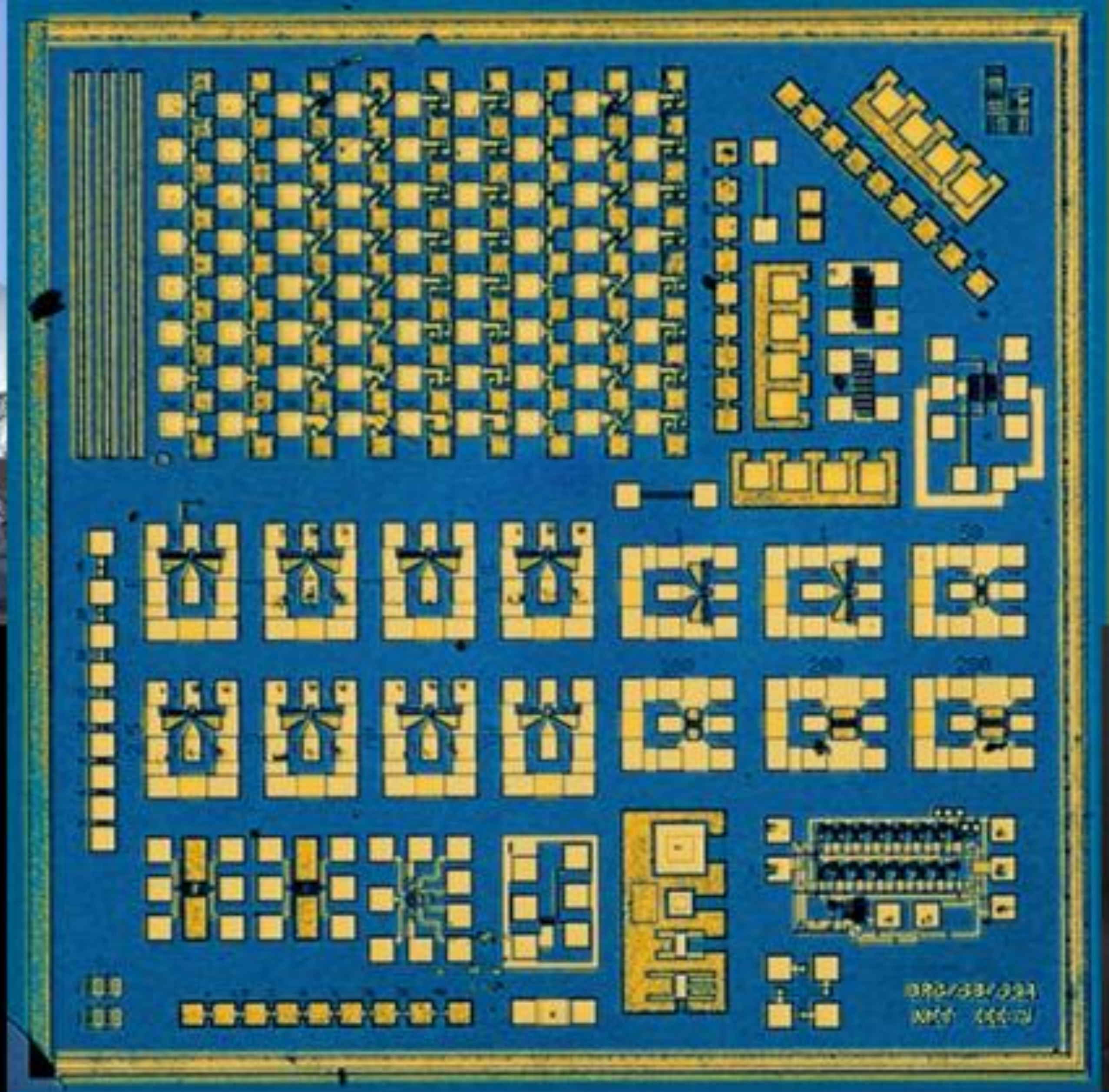

The Periodic Table of the Elements
III
V
1 H
2 He
3 Li 4 Be 5 B 6 C 7 N 8 O 9 F 10 Ne
11 Na 12 Mg 13 Al 14 Si 15 P 16 S 17 Cl 18 Ar
19 K 20 Ca 21 Sc 22 Ti 23 V 24 Cr 25 Mn 26 Fe 27 Co 28 Ni 29 Cu 30 Zn 31 Ga 32 Ge 33 As 34 Se 35 Br 36 Kr
37 Rb 38 Sr 39 Y 40 Zr 41 Nb 42 Mo 43 Tc 44 Ru 45 Rh 46 Pd 47 Ag 48 Cd 49 In 50 Sn 51 Sb 52 Te 53 I 54 Xe
55 Cs 56 Ba 57 La 72 Hf 73 Ta 74 W 75 Re 76 Os 77 Ir 78 Pt 79 Au 80 Hg 81 Tl 82 Pb 83 Bi 84 Po 85 At 86 Rn
87 Fr 88 Ra 89 Ac 104 Rf 105 Db 106 Sg 107 Bh 108 Hs 109 Mt 110 111 112 113 114
58 Ce 59 Pr 60 Nd 61 Pm 62 Sm 63 Eu 64 Gd 65 Tb 66 Dy 67 Ho 68 Er 69 Tm 70 Yb 71 Lu
90 Th 91 Pa 92 U 93 Np 94 Pu 95 Am 96 Cm 97 Bk 98 Cf 99 Es 100 Fm 101 Md 102 No 103 Lr

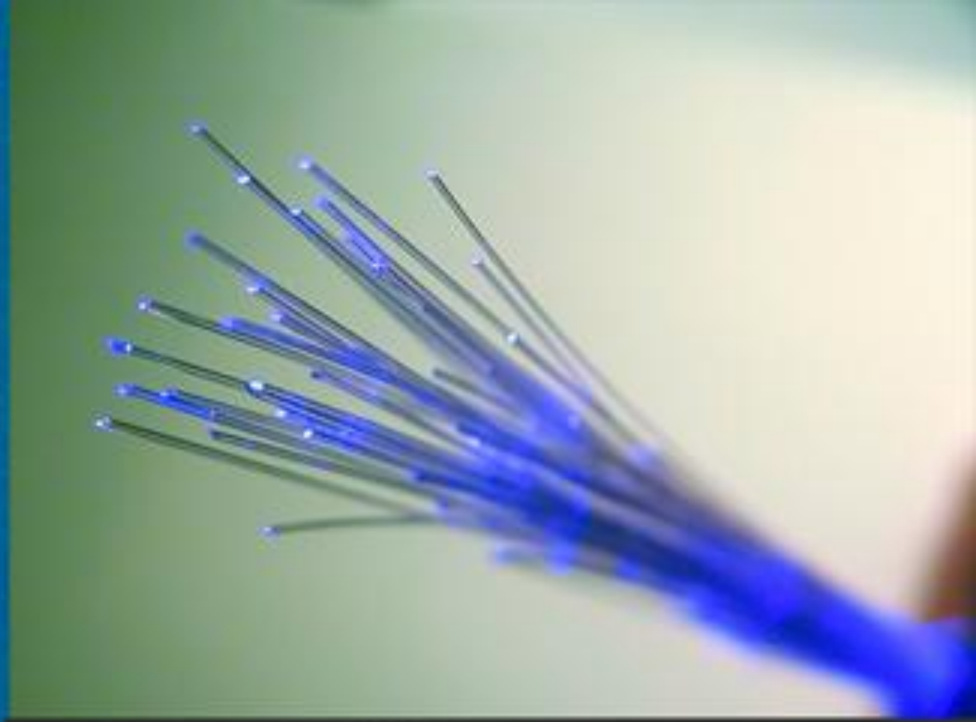
Professor Jesus del Alamo

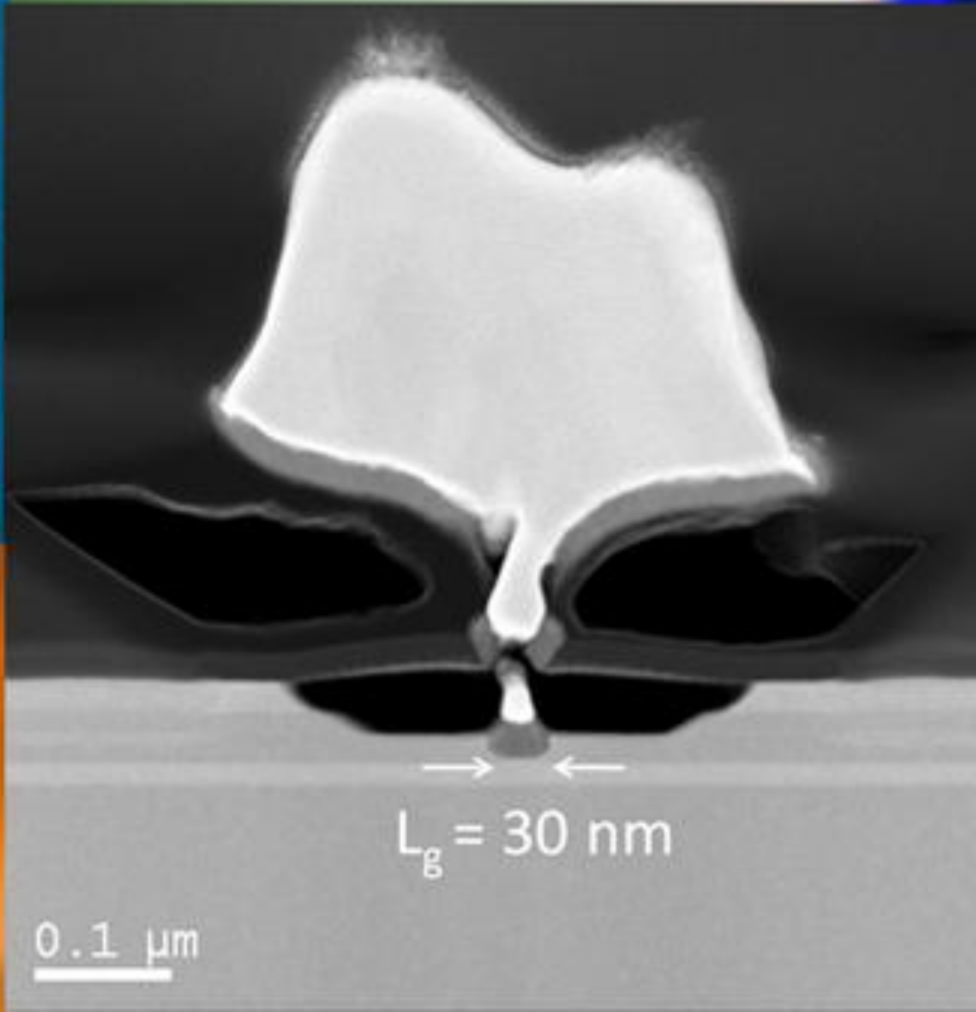
Professor of Electrical Engineering

Donner Professor, MacVicar Faculty Fellow
Department of Electrical Engineering
and Computer Science

Massachusetts Institute of Technology






Lg = 30 nm
0.1 µm

Continuing Moore's Law

Scaling Enables Lower Cost and Higher Capability

Opportunities to Extend Moore's Law

Researchers Doing Innovative Work

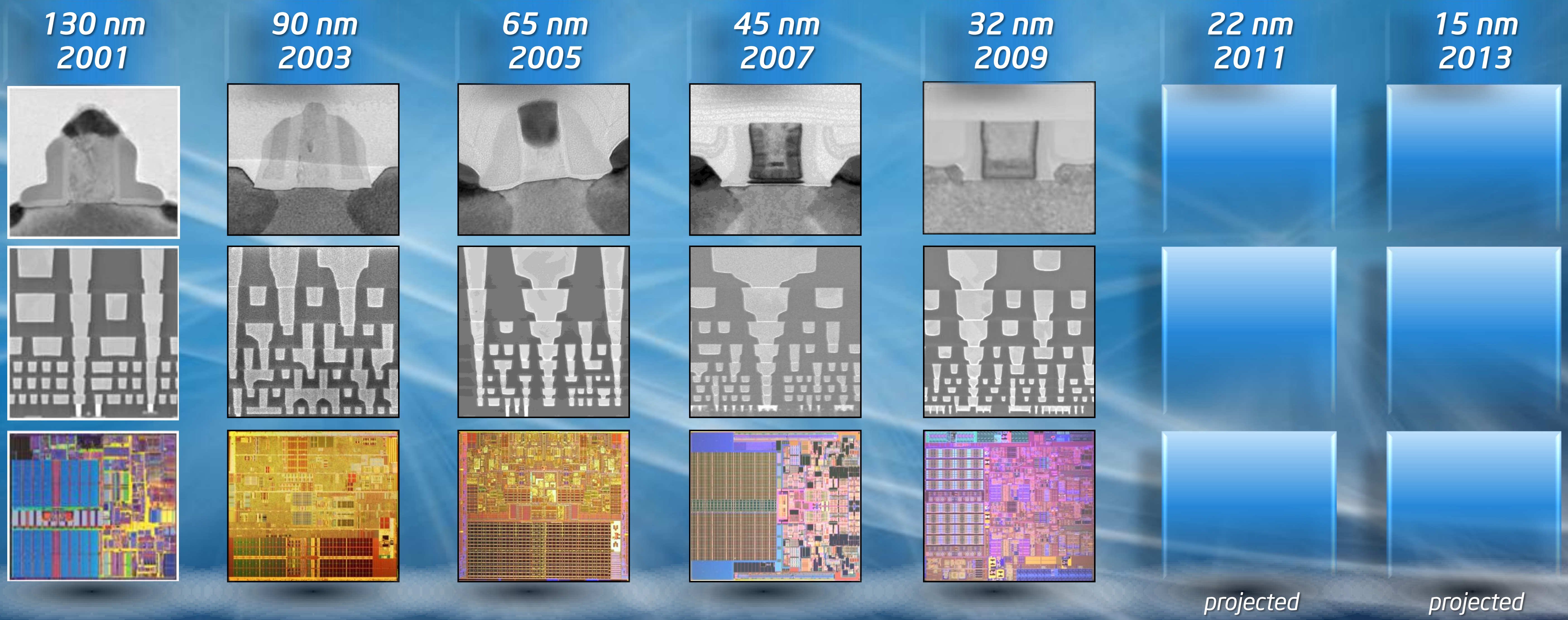
Silicon Leadership:
Delivering Innovation

Relentless Pursuit of Moore's Law

Innovations in Silicon Technology

Extending Leadership for New Opportunities

On-Time 2 Year Cycles



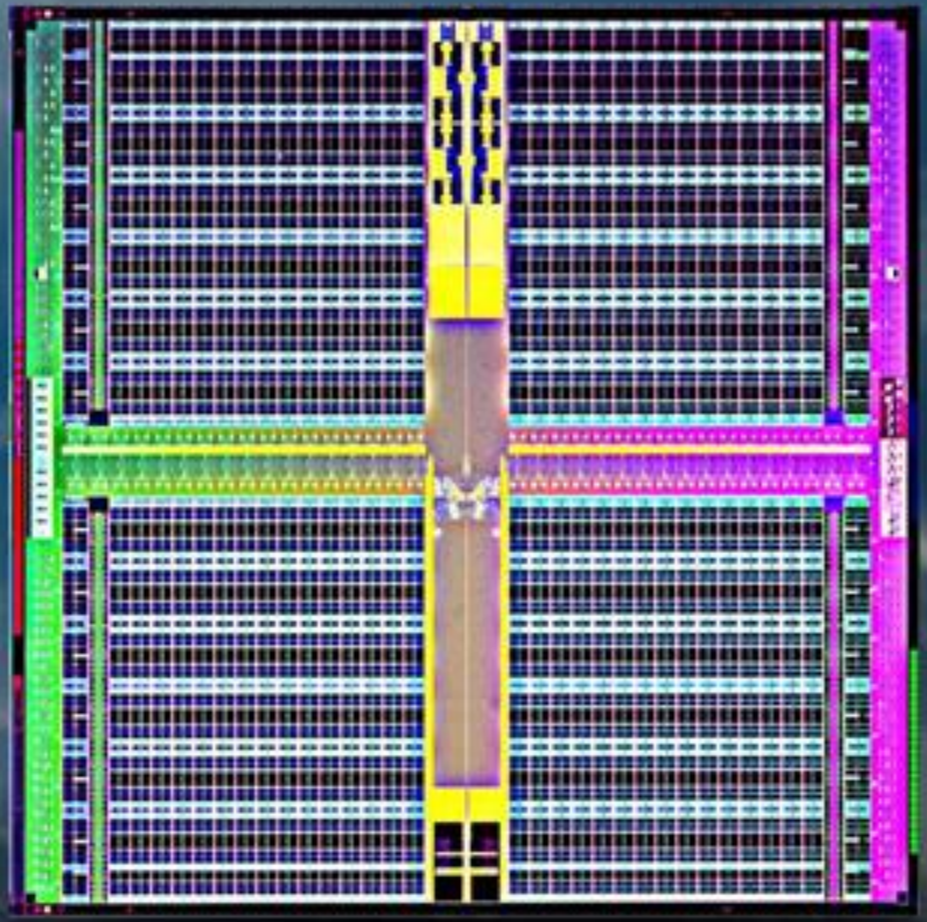
32nm - Extending Technology Leadership

Industry-leading features:

- 2nd generation high-k/metal gate transistors
- 4th generation strained silicon
- Highest reported drive currents
- 0.7x pitch scaling enables 50% area reduction

First to demonstrate working 32nm processors

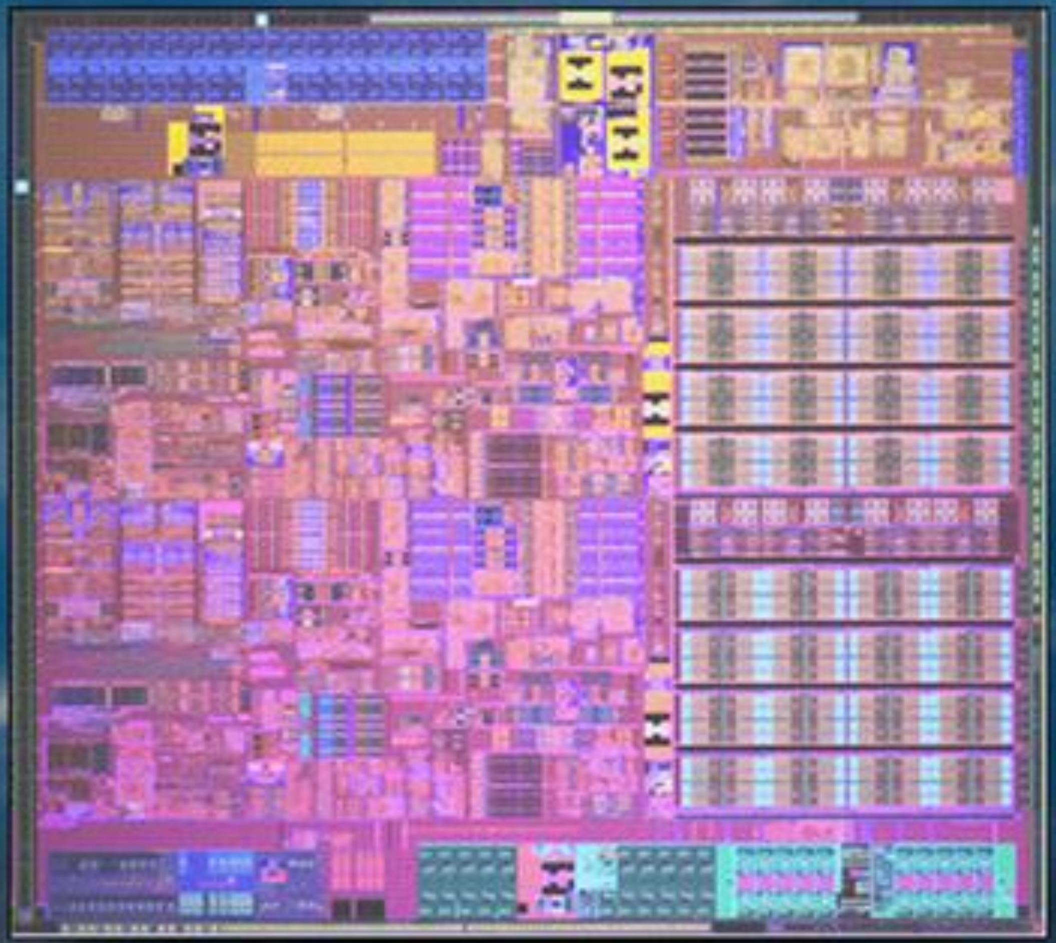
Intel’s 32 nm process is certified for production



291 Mbit SRAM
>1.9 billion transistors

0.171 um2 cell size
3.8 GHz operation

32 nm Westmere Microprocessor in Production



CPU wafers are moving through the factory
in support of planned Q4 revenue production

32nm Manufacturing Fabs:
$7B Investment Over 2 Years

D1D
Oregon

D1C
Oregon

Fab 32
Arizona

Fab 11X
New Mexico

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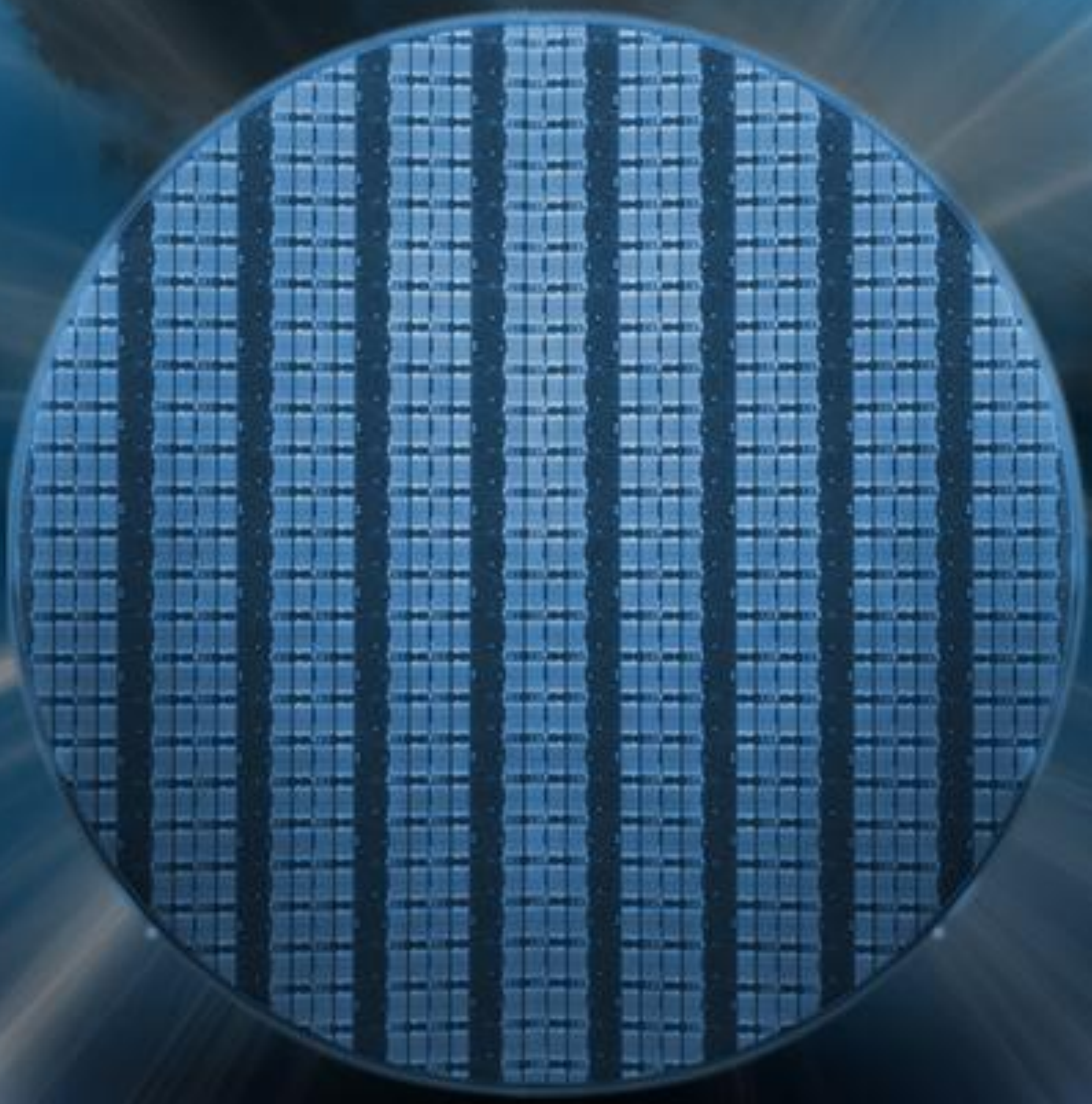
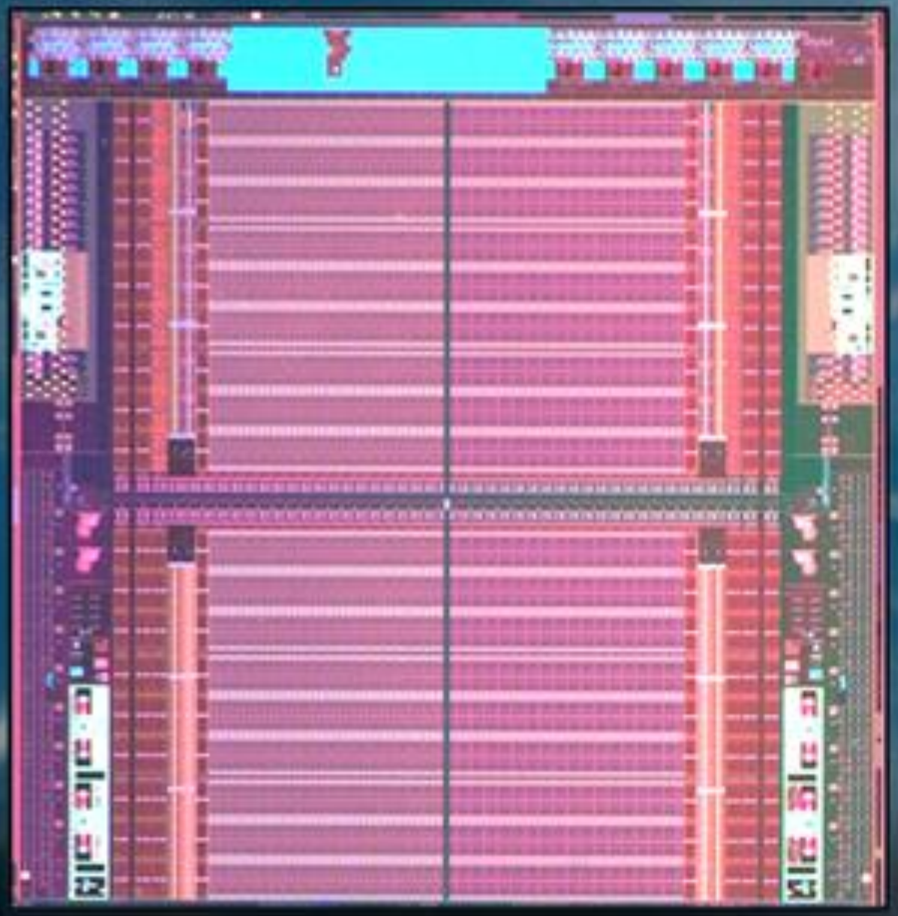
The World's First 22 nm SRAM



The World's First 22 nm SRAM



364 Mbit array size

>2.9 billion transistors

3rd generation high-k + metal gate transistors

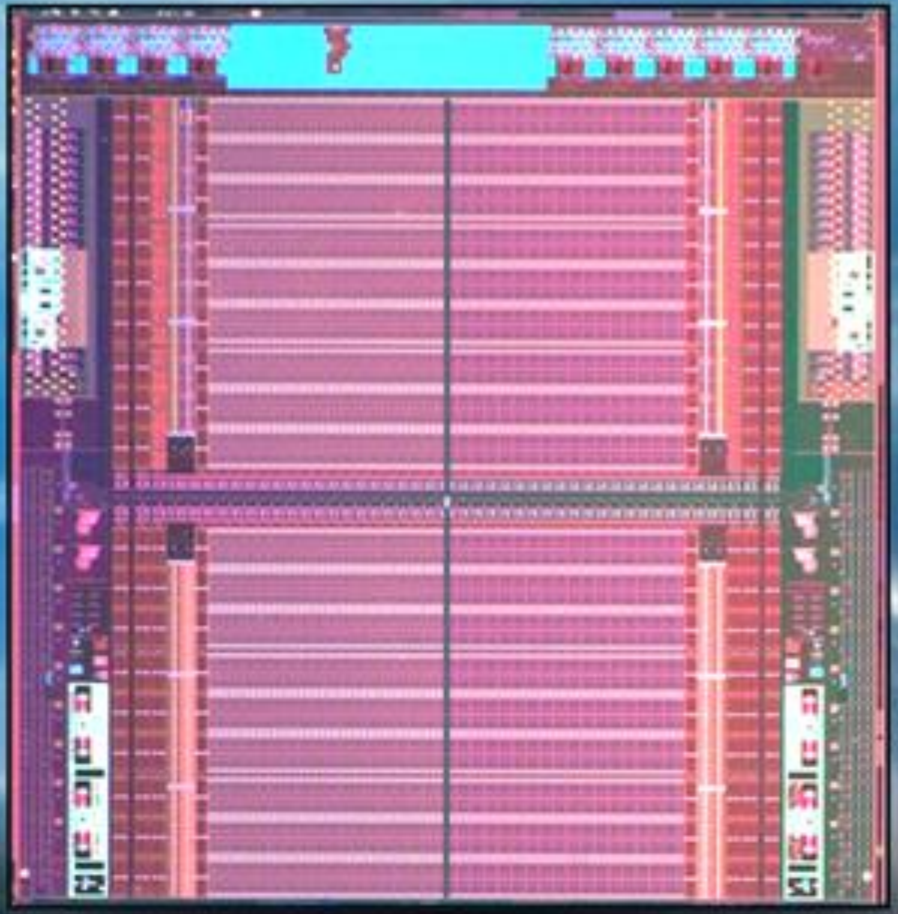
Same transistor and interconnect features as on 22 nm CPUs

Demonstrating working 22 nm SRAMs is an important milestone towards building working 22 nm microprocessors

22 nm Optimized for Wide Range of Applications

High density
0.092 um^2 SRAM cell

Low voltage
0.108 um^2 SRAM cell



0.092 um2 is the smallest SRAM cell
in working circuits reported to date

Silicon Leadership:
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New Segment Opportunities:
Internet Connected Devices

CE

Embedded

Handhelds

New Segments Require New
Technology and Manufacturing Capabilities

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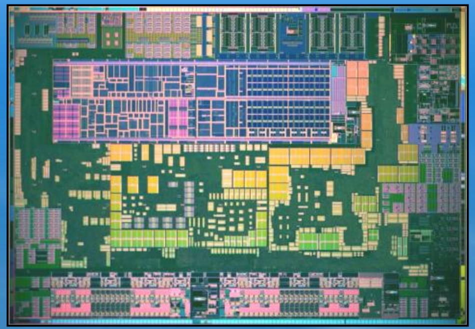
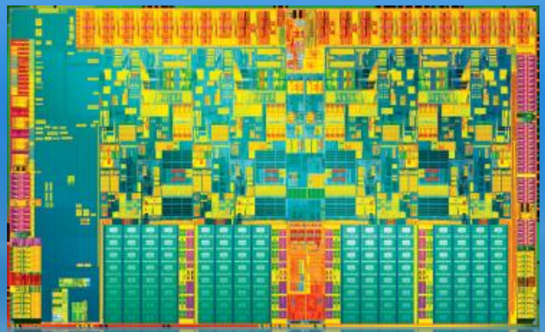
Source: Intel

45nm SoCs

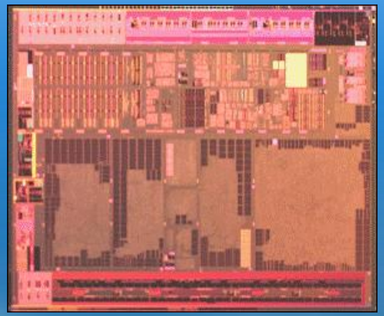
CE
Sodaville



Embedded
Jasper Forest



Handhelds
Lincroft



Initial 45 nm Intel® processor based SoC products

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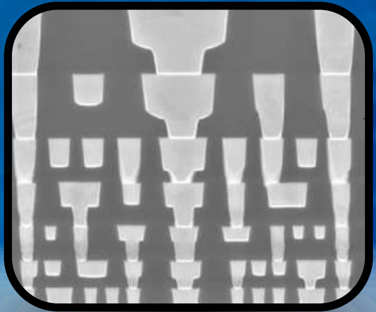
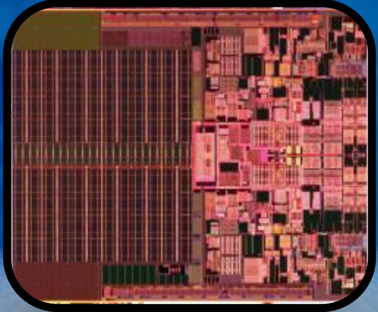
Source: Intel

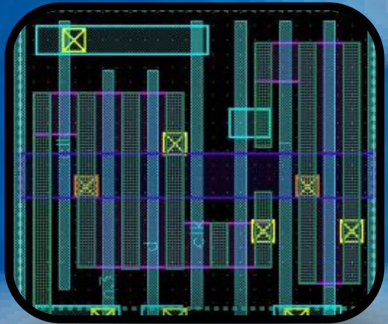
Integrated Device Manufacturer Advantage

Process





Product



Design Tools

Design for Manufacturing

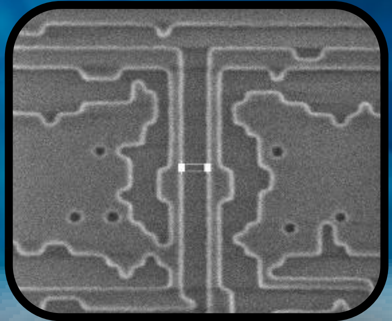
Co-Optimized Process + Product

Rapid Yield Learning

Early Product Ramp

Manufacturing

Masks



Packaging

Expanded Support for New Opportunities

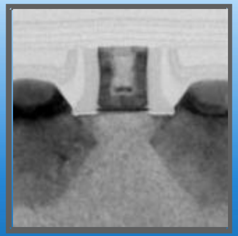
SoC Process Builds on CPU Process

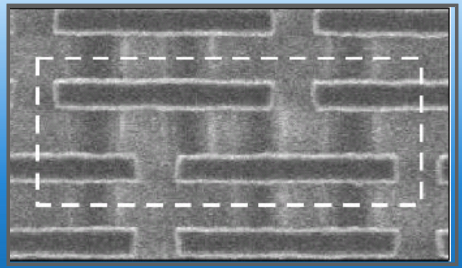
	45nm		32nm		22nm	
	2007	2008	2009	2010	2011	2012
Process:	**P1266**	**P1266.8**	**P1268**	**P1269**	**P1270**	**P1271**
Products:	**CPU**	**SoC**	**CPU**	**SoC**	**CPU**	**SoC**

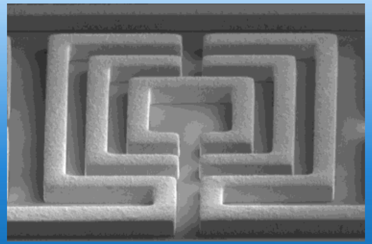
CPU and SoC versions of each process generation to provide transistors, interconnects and other device features optimized for each product line

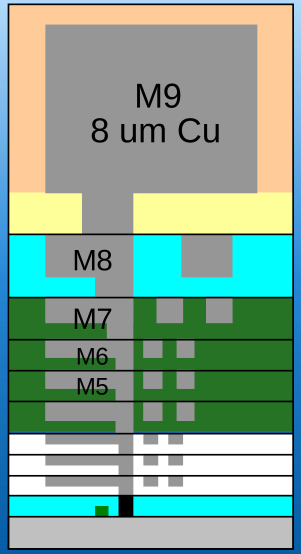
Source: Intel

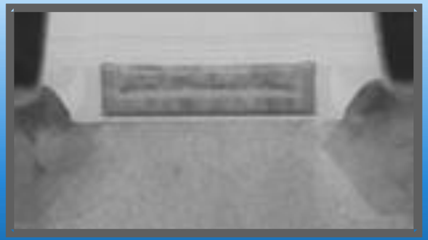
32nm SOC Full-Featured Process Menu

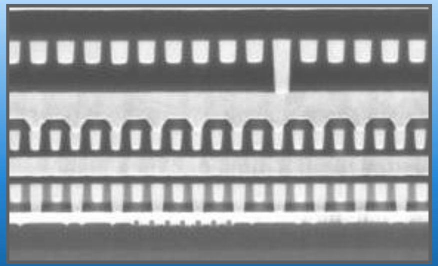

High Perf/Low Power Logic Transistors

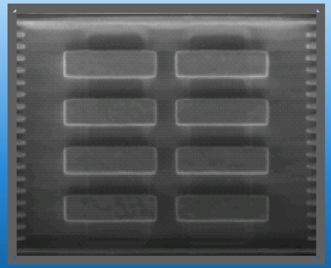

SRAM/RF

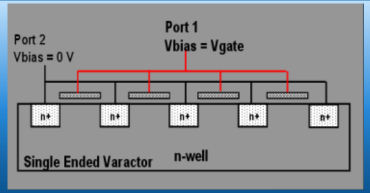

Inductors




Analog/ HV I/O Transistors


Precision Linear Capacitors


Decap



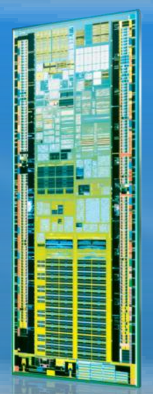
Varactors

Variety of Options to Enable Optimized Silicon Integration of Diverse System Components

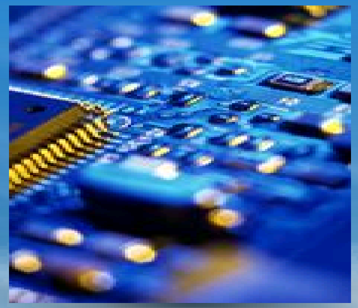
SoC Design and Manufacturing Tools

Benefits: Time to Market, Modularity, Flexibility, Customization

LEADERSHIP DFx TOOLS

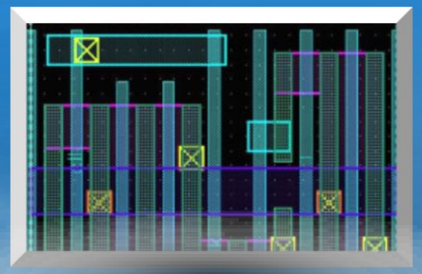


MODULAR SHARED IP LIBRARY
Internal or Customer



COMMON ARCH FRAMEWORK

CONVERGED TOOLS AND METHODOLOGIES



SoC DESIGN TECHNOLOGY LAYER

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INTEL DEVELOPER FORUM

Source: Intel

Intel 32nm Package Options:
Enabling SOC Optimization in Integration, Form Factor and Cost

MCP FCBGA
2mm thick

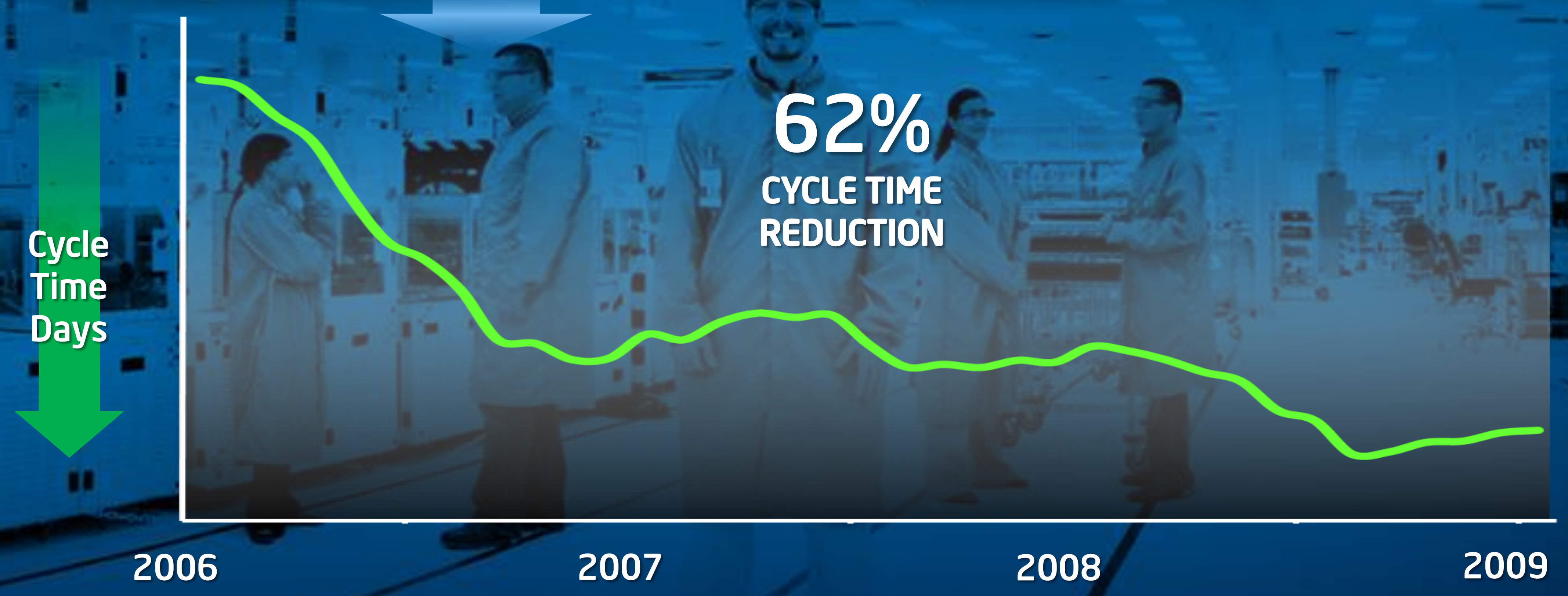
SINGLE DIE FCBGA
1.6mm thick

DISCRETE FCMB
<1 mm thick

POP FCMB
<0.8 mm thick

Faster Factories Enable Improved Customer Response

Faster Factories *Better Commitment* *Quicker Order to Delivery*



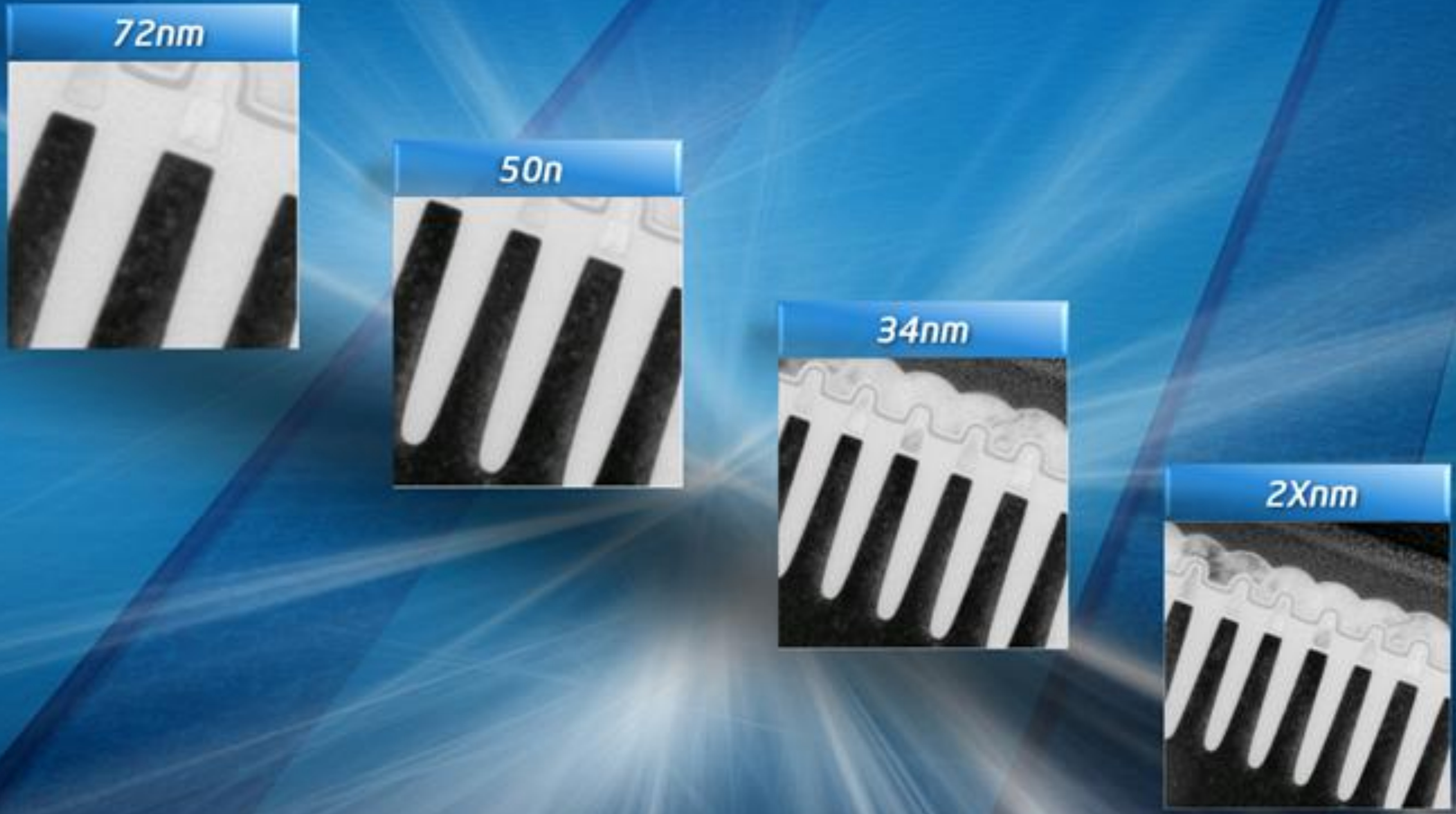
Faster Factories Enable Improved Customer Response

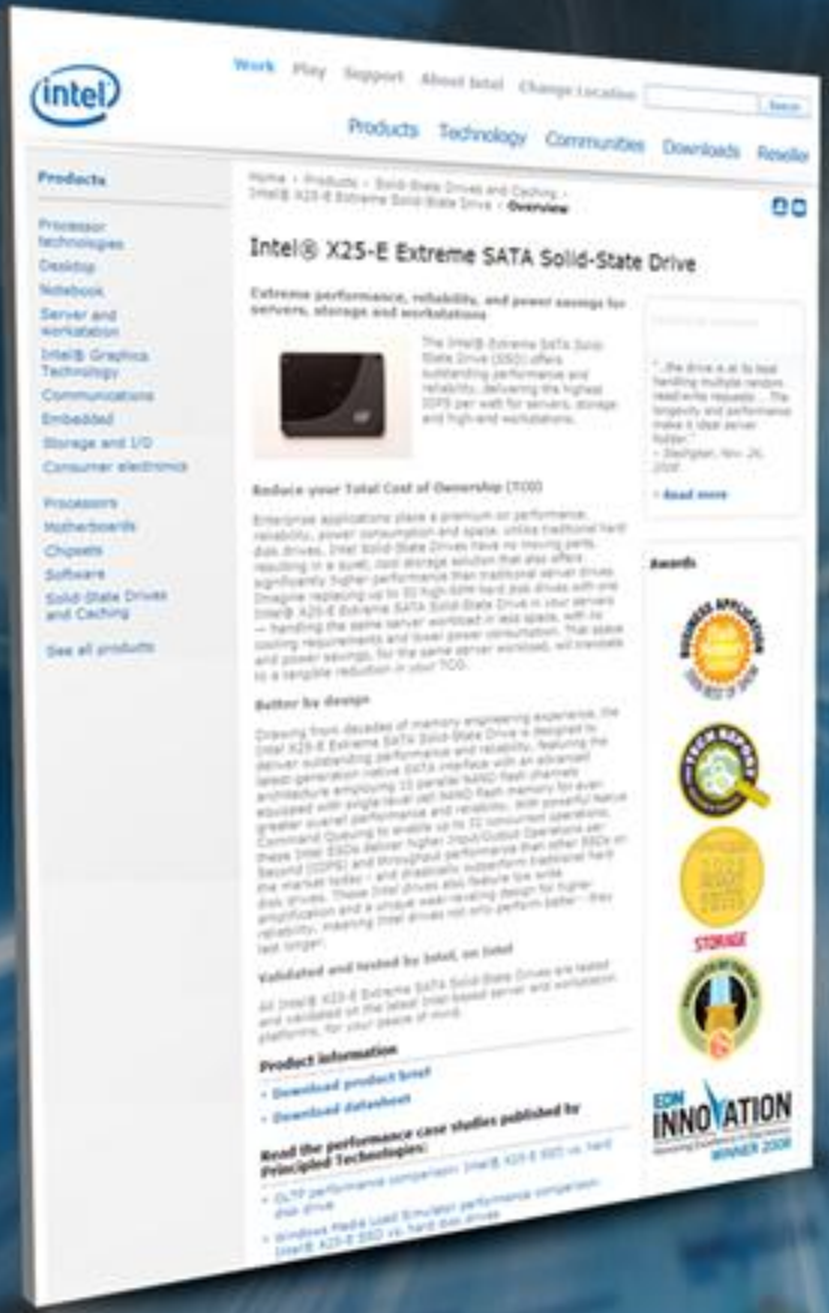
Faster Factories | *Better Commitment* | *Quicker Order to Delivery*

Faster Factories Enable Improved Customer Response

Faster Factories — *Better Commitment* — *Quicker Order to Delivery*

NAND Scaling:
Extending the Possibilities





Rick Coulson

Intel Senior Fellow

Director, Storage Technologies
Technology and Manufacturing Group

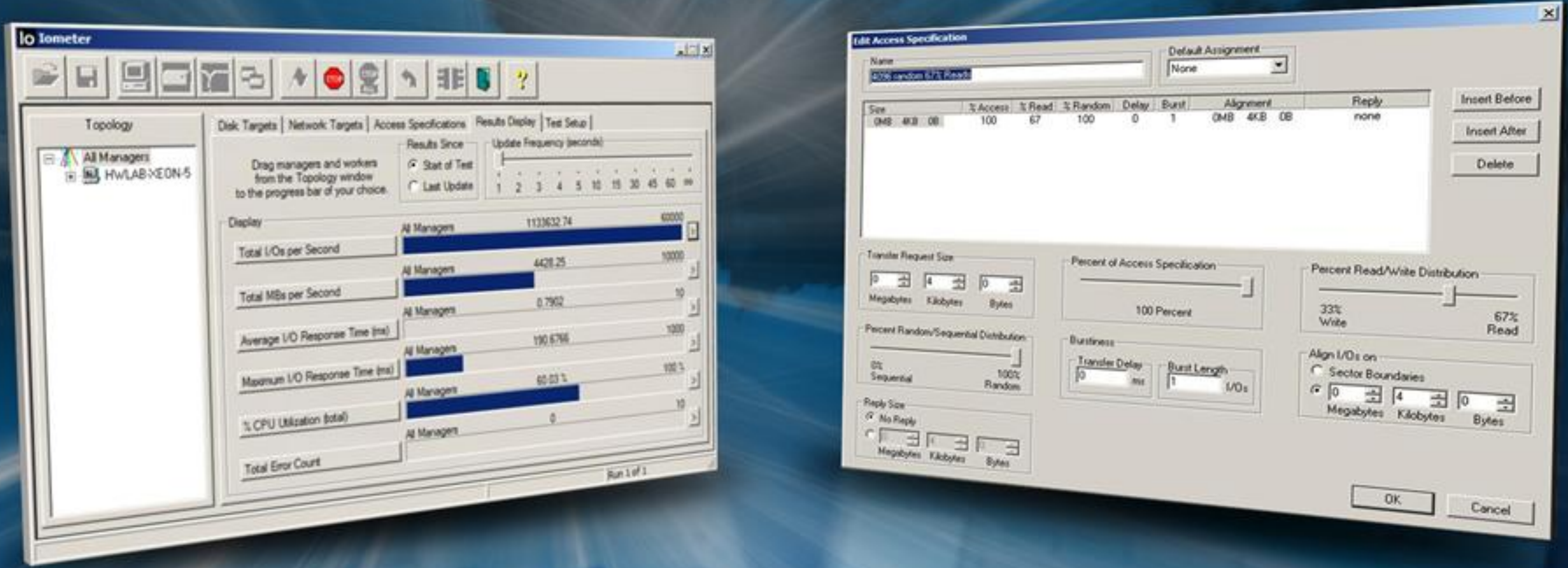
Platform Co-Optimizations with SSDs

SSDs benefit existing platforms

Storage subsystems lag

Co-optimizing SSDs and platform

Improves performance, scalability, power efficiency, total cost



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In Closing…

Relentless Pursuit of Moore's Law

Innovations in Silicon Technology

Extending Leadership for New Opportunities

Sponsors of Tomorrow.™