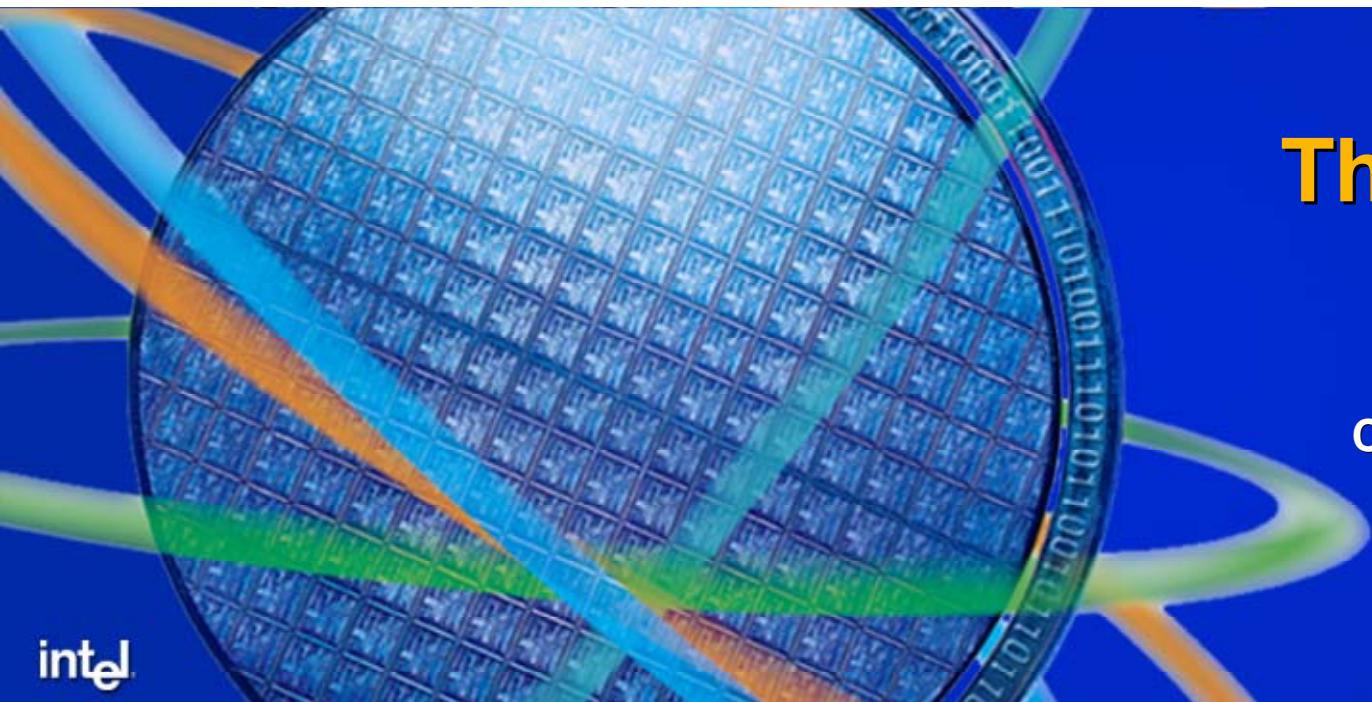


# Intel Developer Forum



# The Era Of Tera

**Pat Gelsinger**  
Chief Technology Officer  
Senior Vice President

Intel  
**Developer**  
Forum

intel

# The Information Age



Intel

Intel  
**Developer**  
Forum

# The Information Age

*Innovation Is The Fuel*

*Need Is The Catalyst*





# The End Of The Road?

**No New Needs ...**

*Today Good Enough?*

**Innovation Getting Harder ...**

*Or Too Expensive?*



# Lessons From History

1980



First PC 1981

Intel  
**Developer**  
Forum

# Lessons From History



# Lessons From History



1995  
Internet  
Multimedia  
Joystick  
Speakers

Intel  
**Developer**  
Forum

# Lessons From History



**INFORMATION WEEK** **LANGALETTER** 

How Fast Is Fast Enough?

For new hardware, I think about 400-MHz is adequate for just about any application... So a 400-MHz box shouldn't become obsolete anytime soon.

Frank Langa  
October 6, 1999

**Intel**  
**Developer**  
**Forum**

# Lessons From History



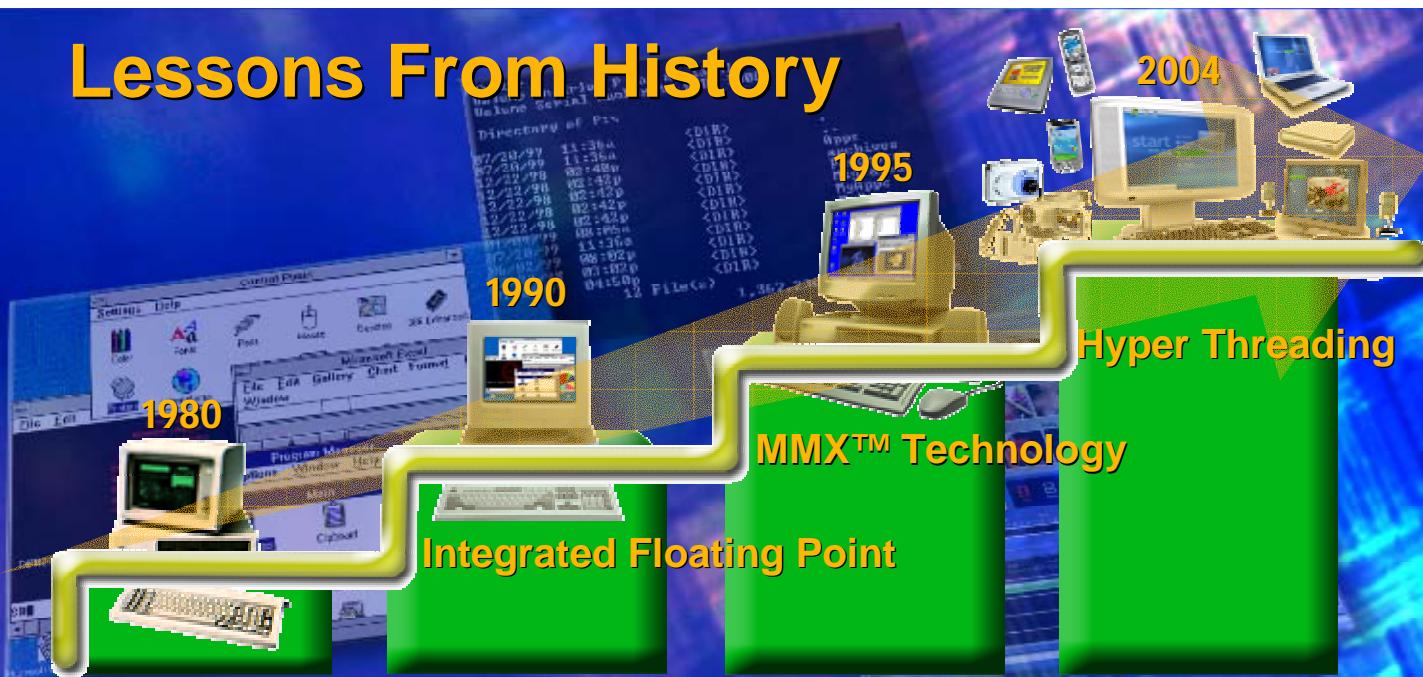
Intel  
Developer  
Forum

# Lessons From History



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Developer  
Forum

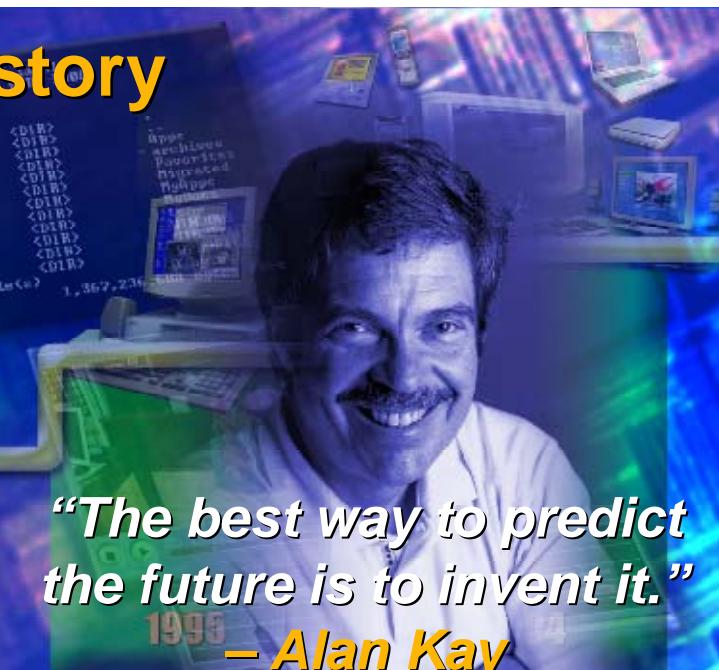
# Lessons From History



# Lessons From History



*The best way to predict  
the future is to invent it.*  
— Alan Kay



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# Today's Digital Transformation



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# Only The Tip Of The Iceberg

*Byte = 8 bits  
Kilobyte =  $10^3$   
Megabyte =  $10^6$   
Gigabyte =  $10^9$   
Terabyte =  $10^{12}$   
Petabyte =  $10^{15}$   
Exabyte =  $10^{18}$   
Zettabyte =  $10^{21}$   
Yottabyte =  $10^{24}$*

U.S. Broadcast Media	14,893 TB
Worldwide Filmed Content	420,254 TB
Worldwide Printed Content	1,633 TB
Internet	532,897 TB
World Telephone Calls	17,300,000 TB
Worldwide Magnetic Content	4,999,230 TB
Worldwide Optical Content	103 TB
Electronic Flows Of New Info	17,905,340 TB

Source: How much information 2003

# A Glimpse Of The Future

*Digital Immersion*

*Beyond Creation & Consumption*

*Every Minute,*

*Every Where,*

*Every Body*



# The RMS View



# The RMS View

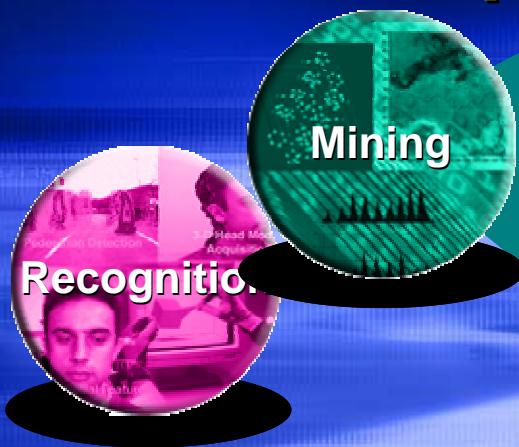


Human-computer Interfaces  
Multimodal Detection  
Statistical Computing  
Clustering and Classification  
Machine Learning



# The RMS View

Streaming Data Mining  
Web Mining  
Content-based Image Retrieval  
Summarization



# The RMS View



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Photo-realism  
Real-world Animation  
Audio/Video/Image Synthesis  
Document Synthesis

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Forum

# The RMS View

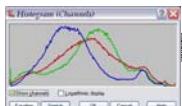


**Workload** Convergence  
Driving **Architectural**  
Convergence

# The Era of Tera

Dataset Size

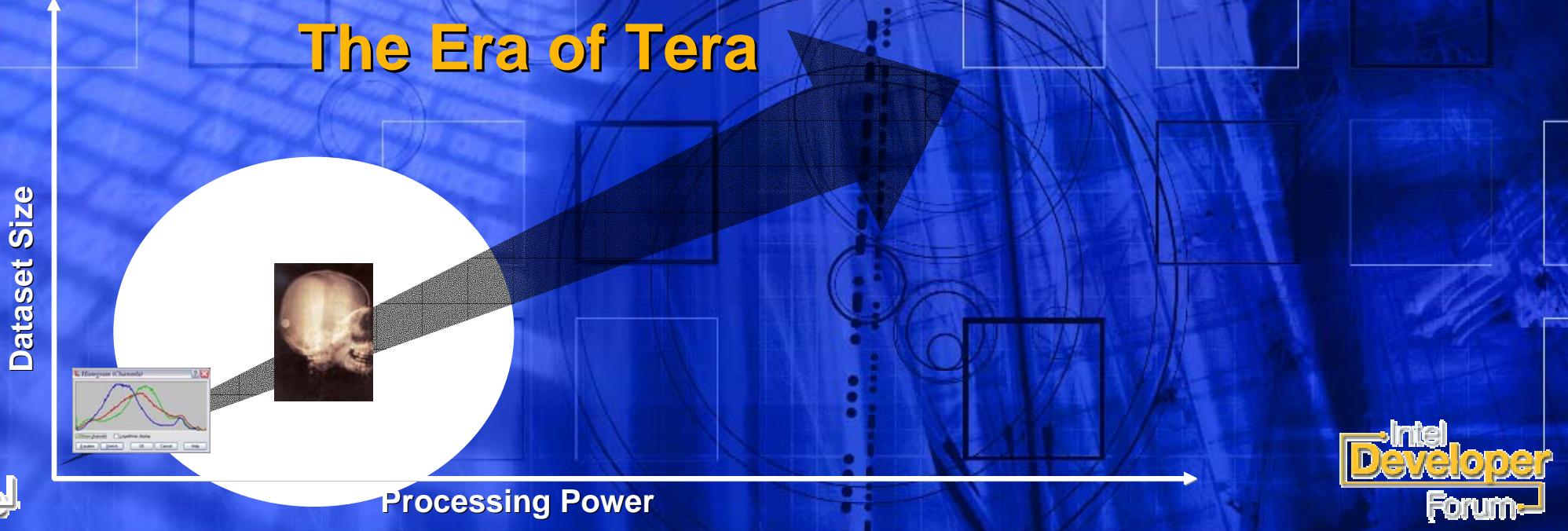
Processing Power



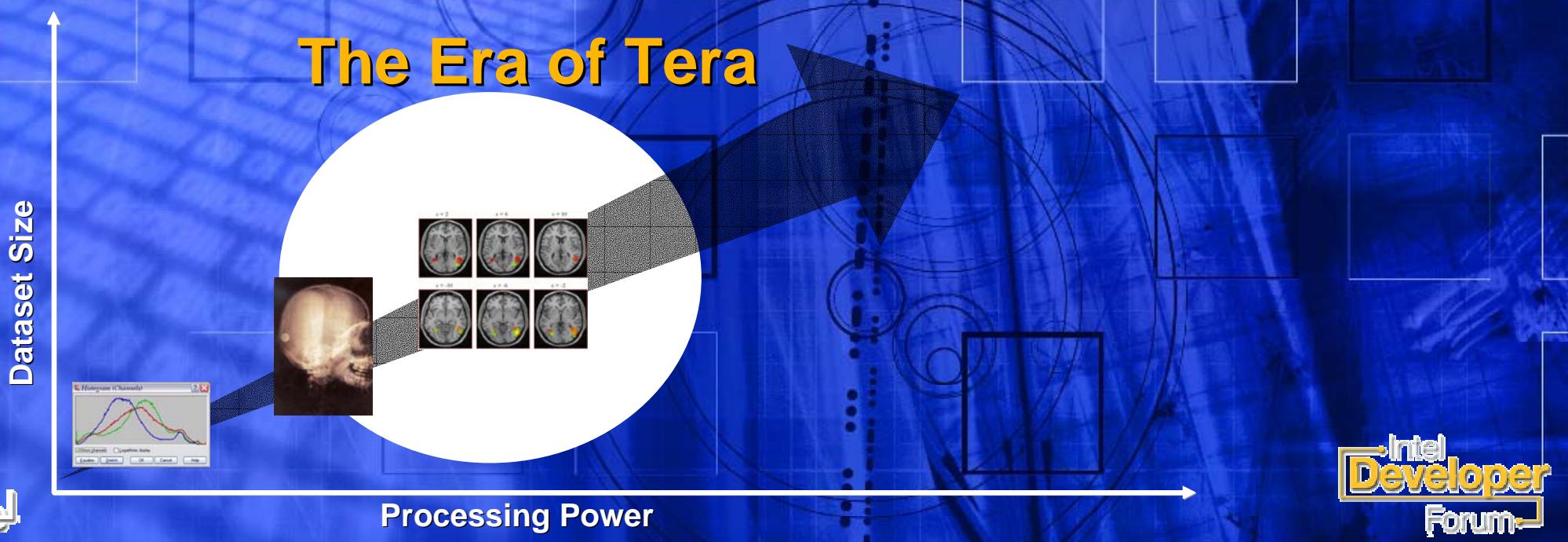
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**Developer**  
Forum



# The Era of Tera



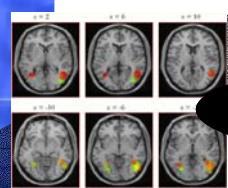
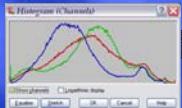
# The Era of Tera



# The Era of Tera

Dataset Size  
↑

Processing Power  
→



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Forum

# The Era of Tera

Dataset Size

Terabytes

Gigabytes

Megabytes

Kilobytes  
KIPS

Processing Power

GIPS

TIPS



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Forum

R ecognition

M ining

S ynthesis



Intel  
**Developer**  
Forum



## Philipp Slusallek

- Professor for Computer Graphics, Saarland University, Germany
- Visiting Assistant Professor Stanford University, 1998 - 1999
- Co-founder of “inTrace GmbH”

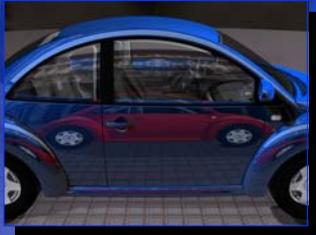


# Rasterization vs. Ray Tracing



## Rasterization

- Wrong reflection
- Incorrect shadows
- Complex content creation

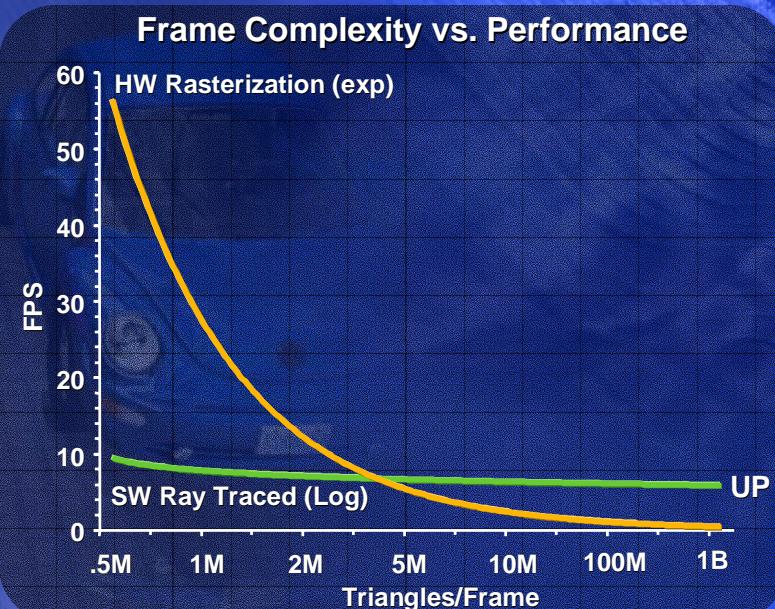


## Ray Tracing

- Reliable, true reflections and shadows
- Simple content creation
- Scalable

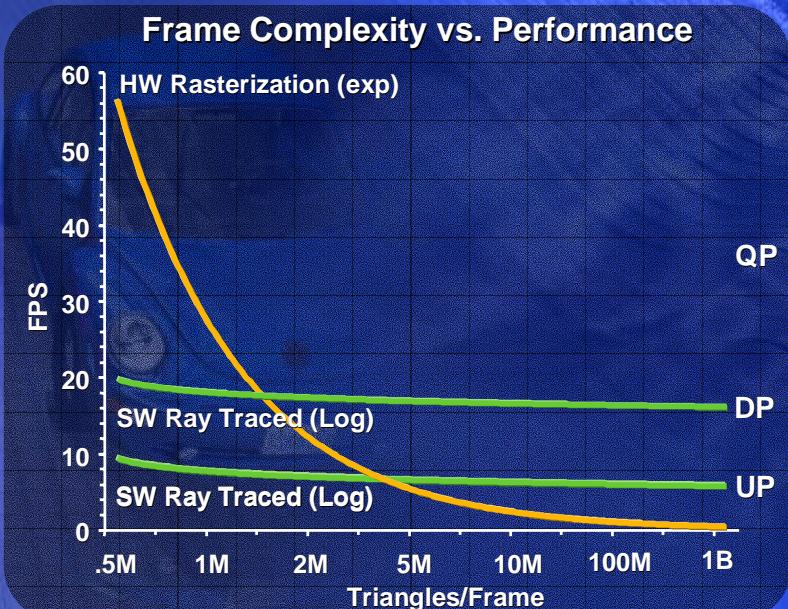


Sunflowers: one *billion* polygons and shadows (4 fps @ 640x480)



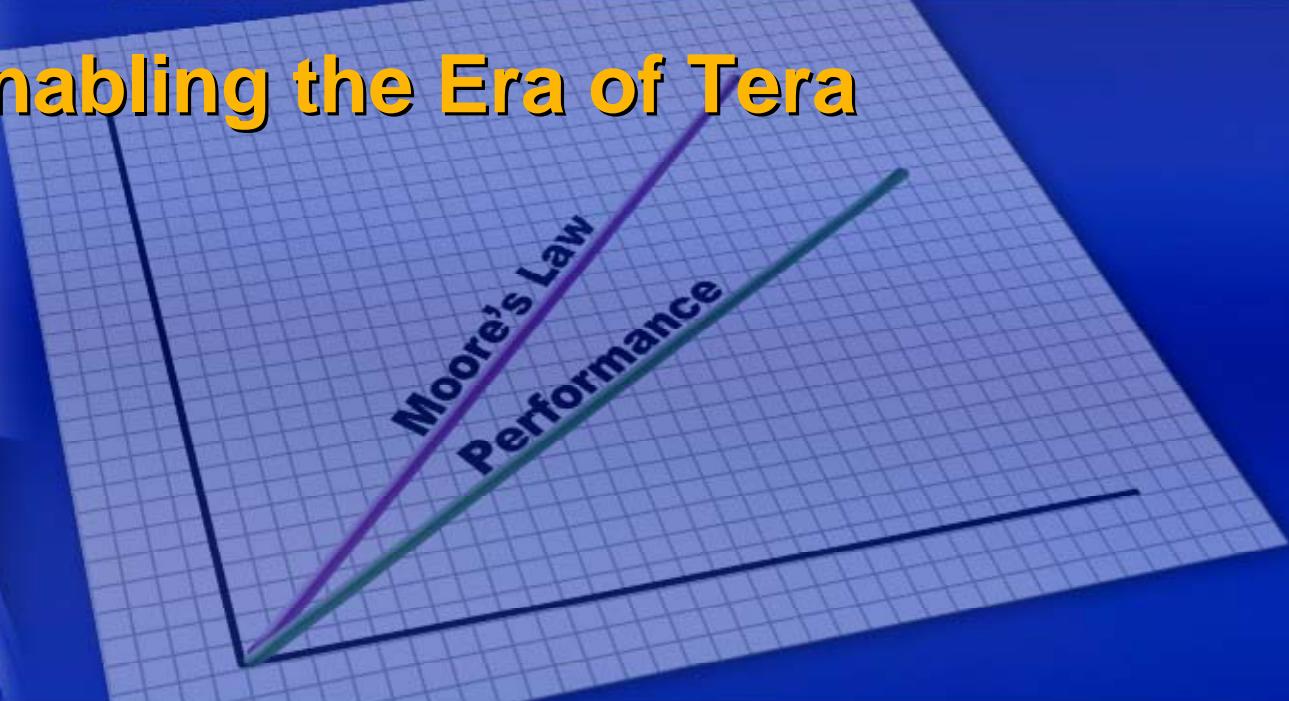


Sunflowers: one **billion** polygons and shadows (4 fps @ 640x480)





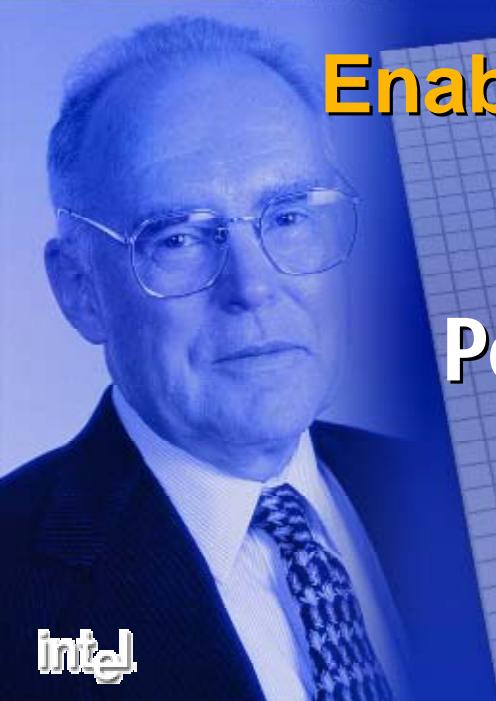
# Enabling the Era of Tera



A graph on a grid background showing two upward-sloping lines. The upper line is purple and labeled "Moore's Law". The lower line is green and labeled "Performance". Both lines start at the same point on the left and curve upwards to the right, indicating exponential growth over time.

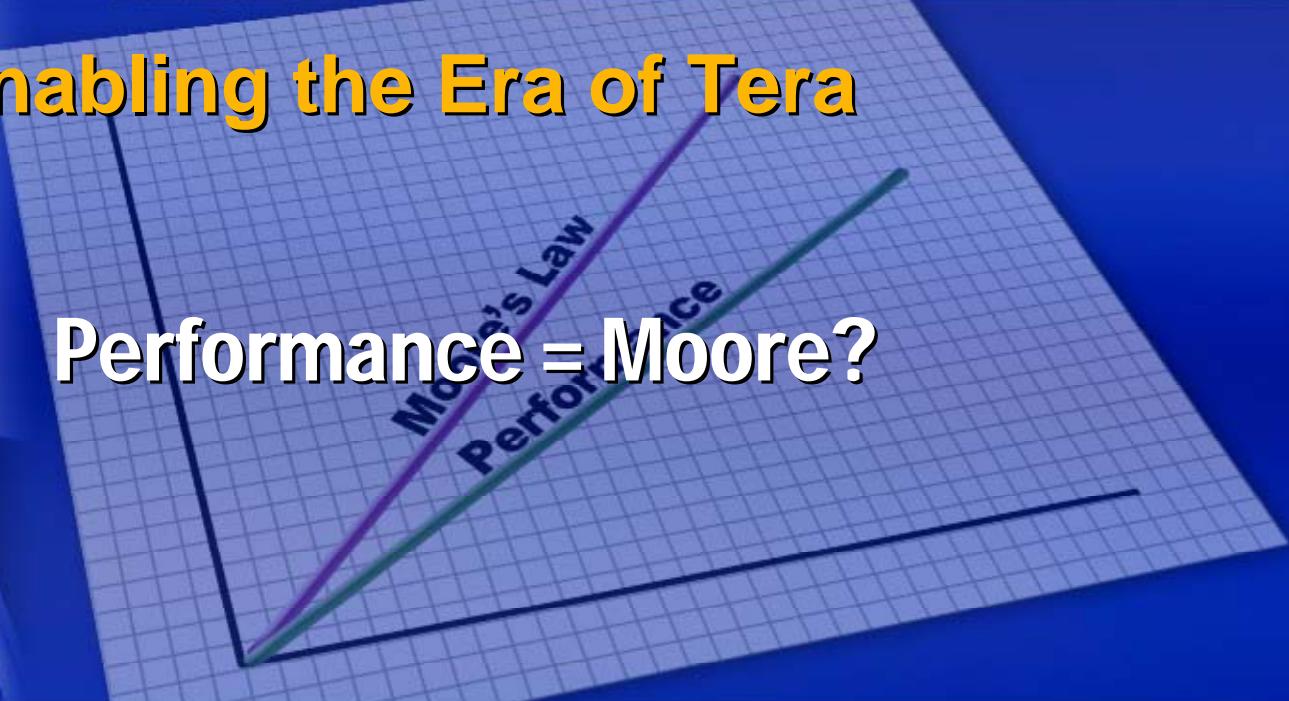
Moore's Law  
Performance





# Enabling the Era of Tera

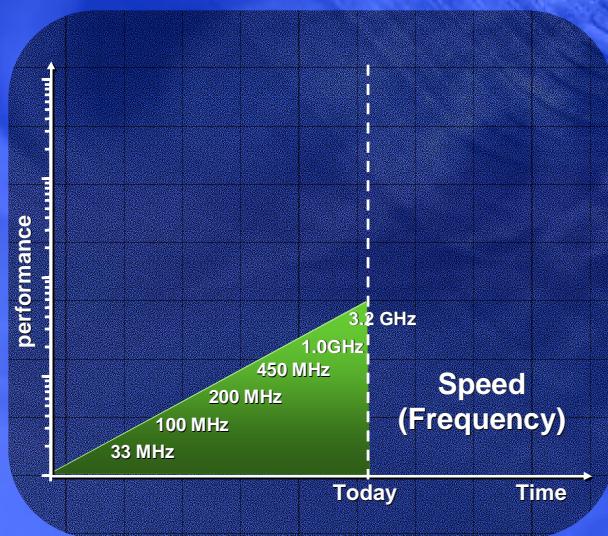
Performance = Moore?



A graph on a grid background showing two intersecting diagonal lines. The upper line is purple and labeled "Moore's Law". The lower line is green and labeled "Performance". The two lines intersect at the origin of the graph.



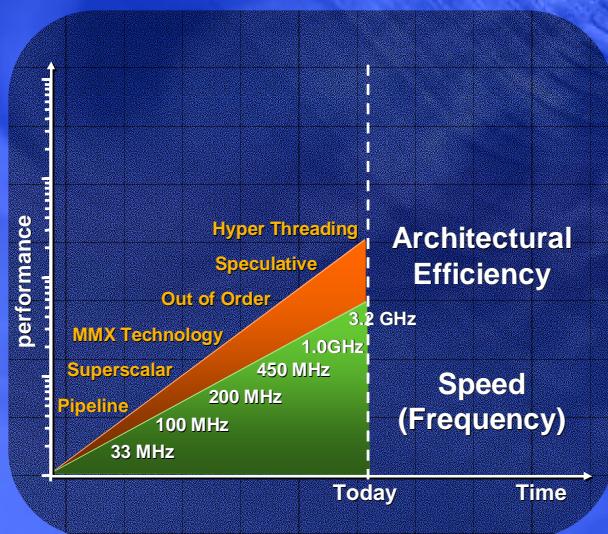
# Enabling the Era of Tera



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# Enabling the Era of Tera

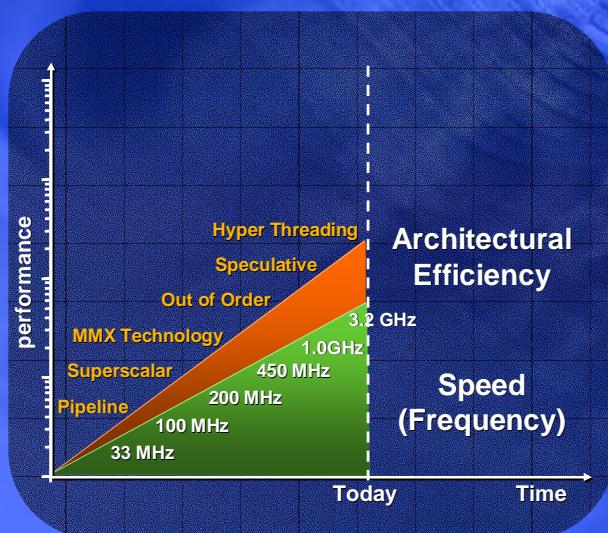


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Developer  
Forum

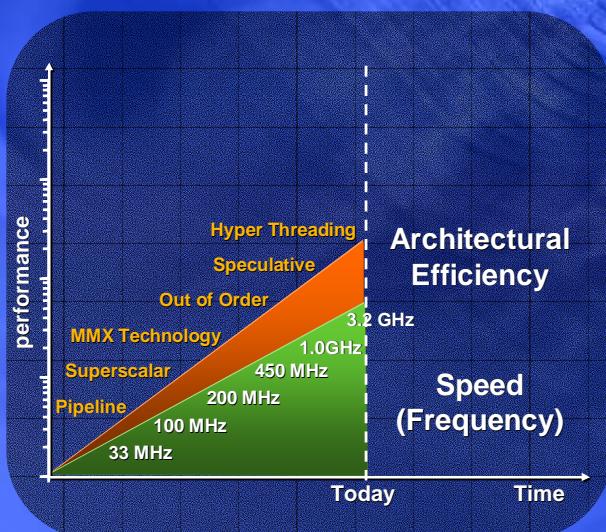
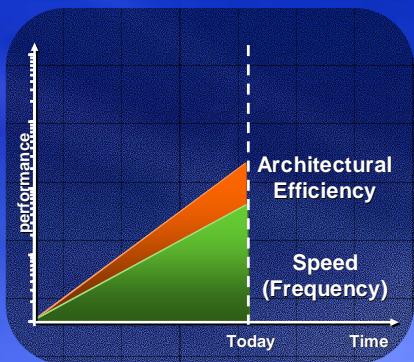
intel

# Enabling the Era of Tera

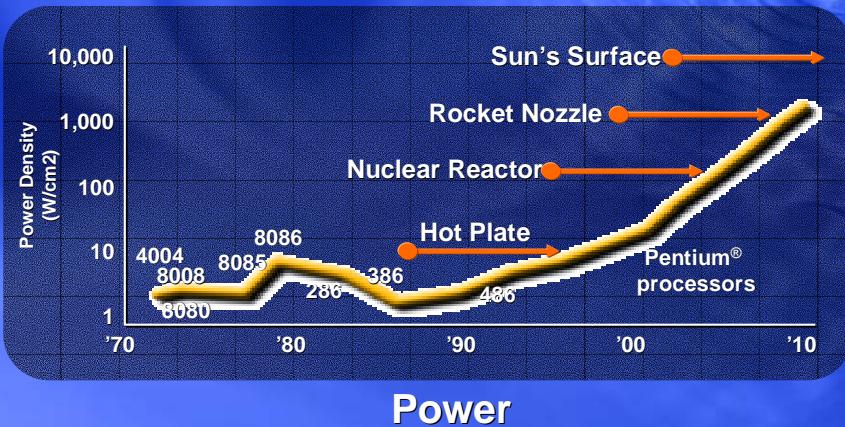
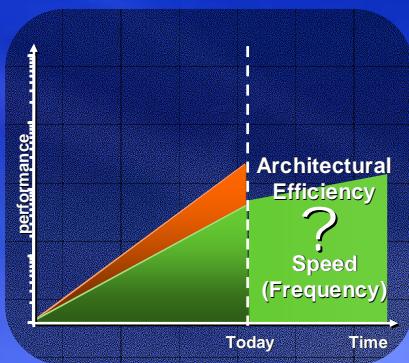
*Performance =  
Speed  
+  
Architectural  
Efficiency*



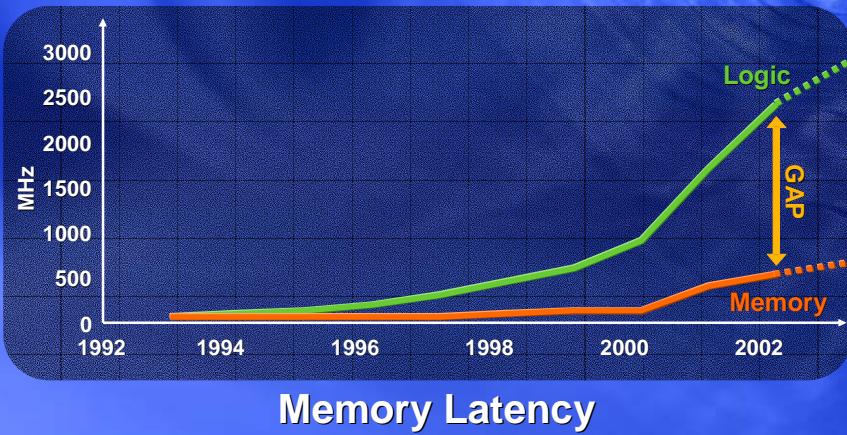
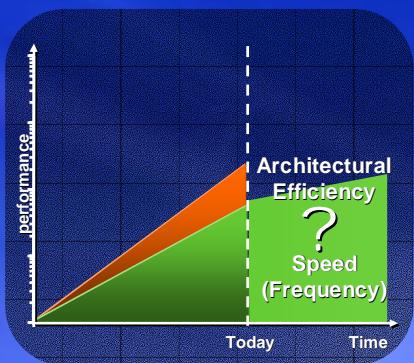
# Enabling the Era of Tera



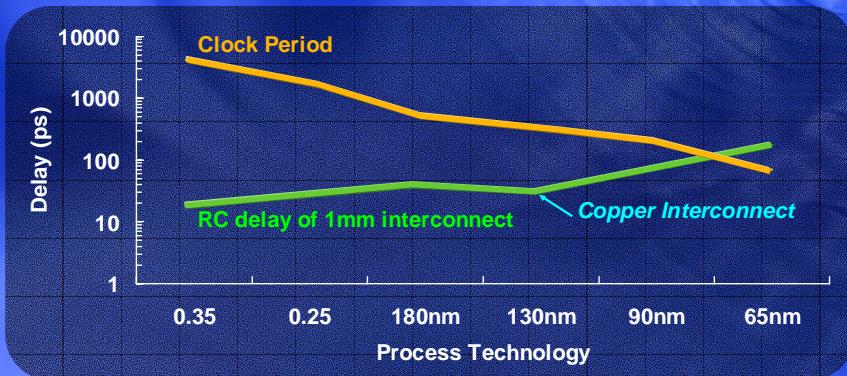
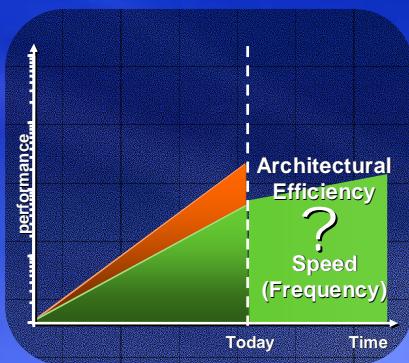
# Enabling the Era of Tera



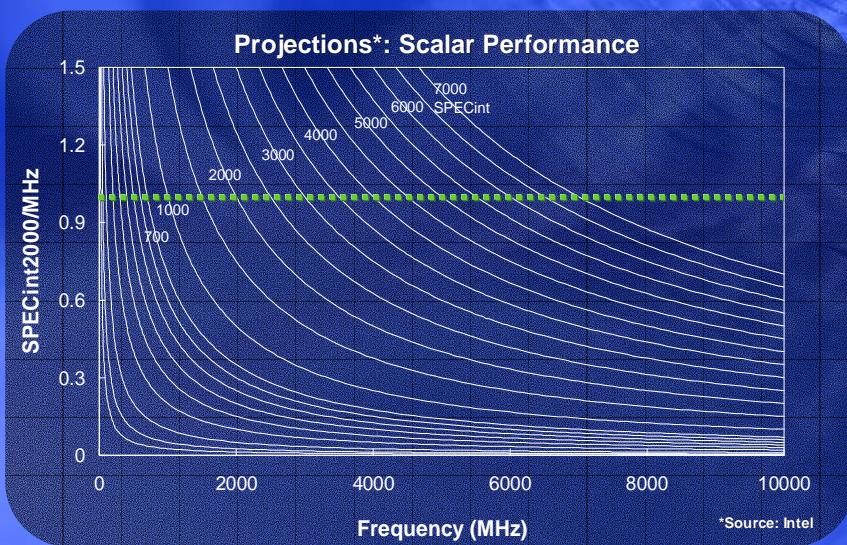
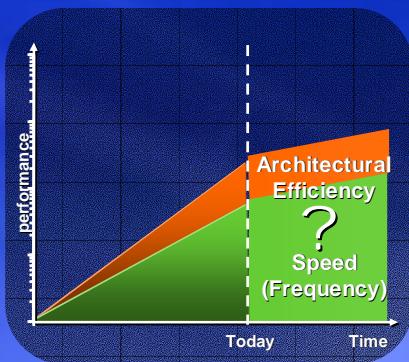
# Enabling the Era of Tera



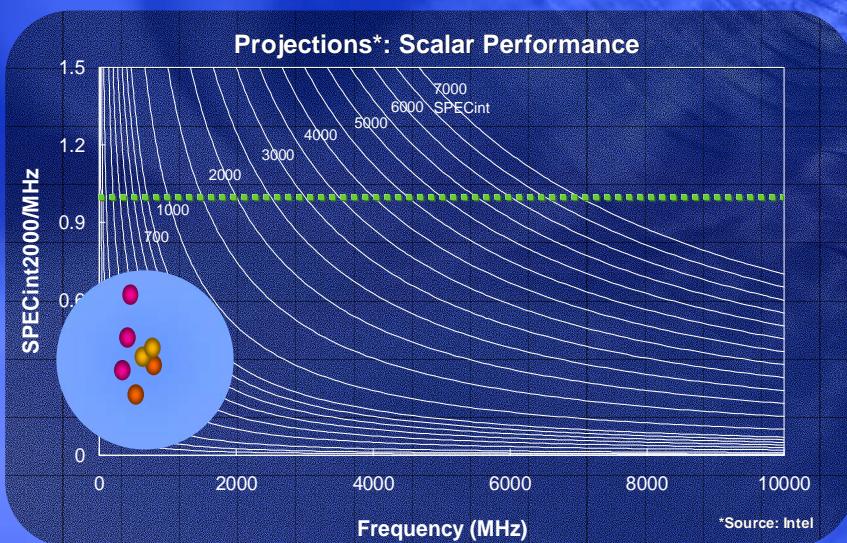
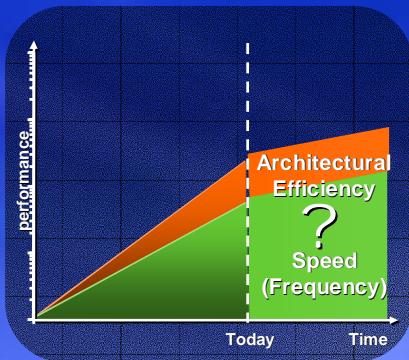
# Enabling the Era of Tera



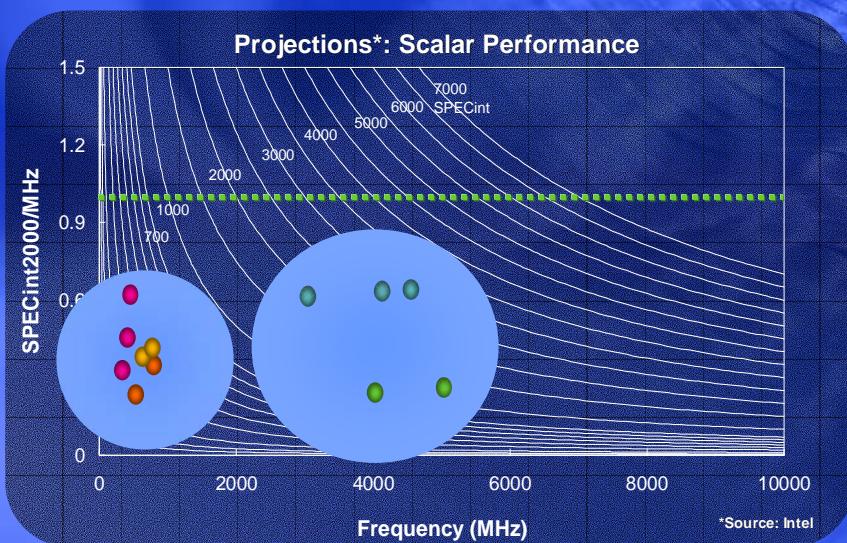
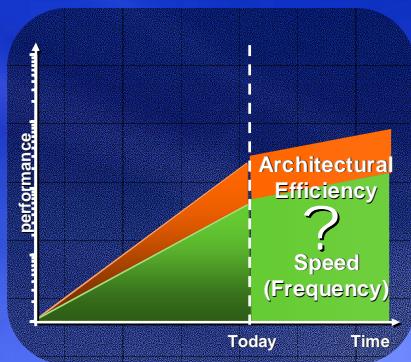
# Enabling the Era of Tera



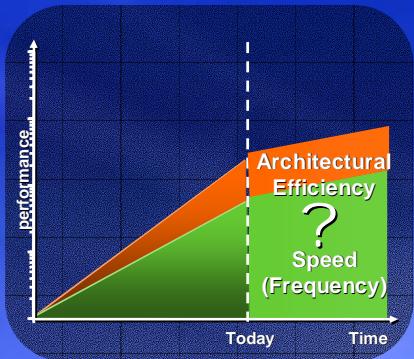
# Enabling the Era of Tera



# Enabling the Era of Tera



# Enabling the Era of Tera



*Need An Architectural  
Paradigm Shift*

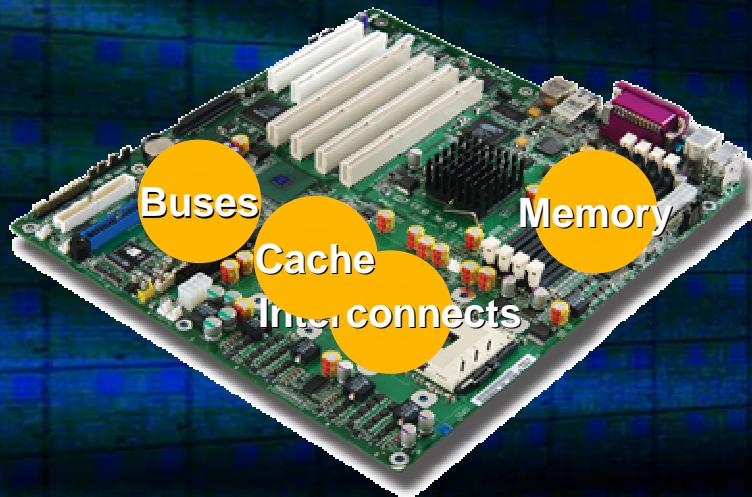


# A New Architectural Approach



# A New Architectural Approach

Platform  
Focused



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**Developer**  
Forum

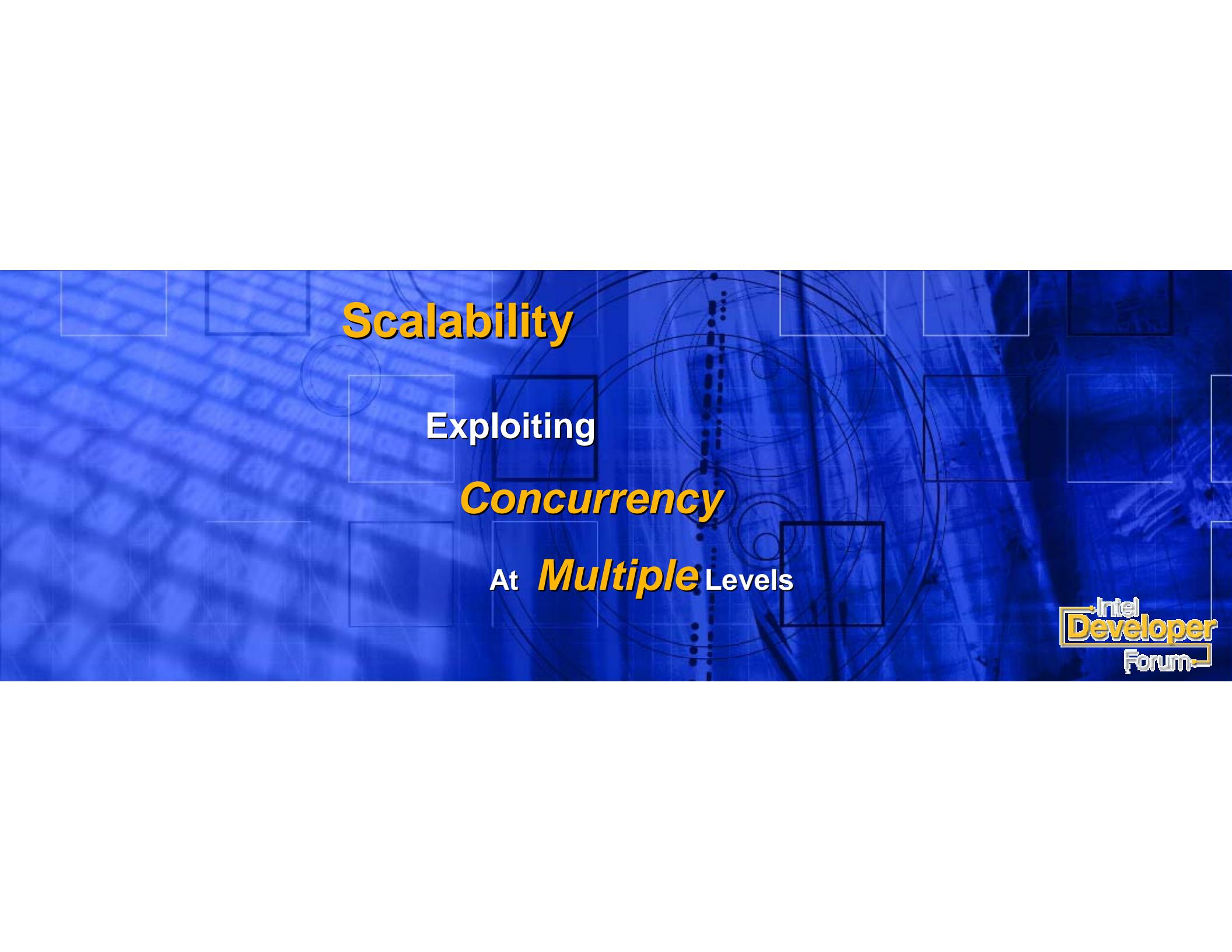
# A New Architectural Approach

Scalability

Adaptability

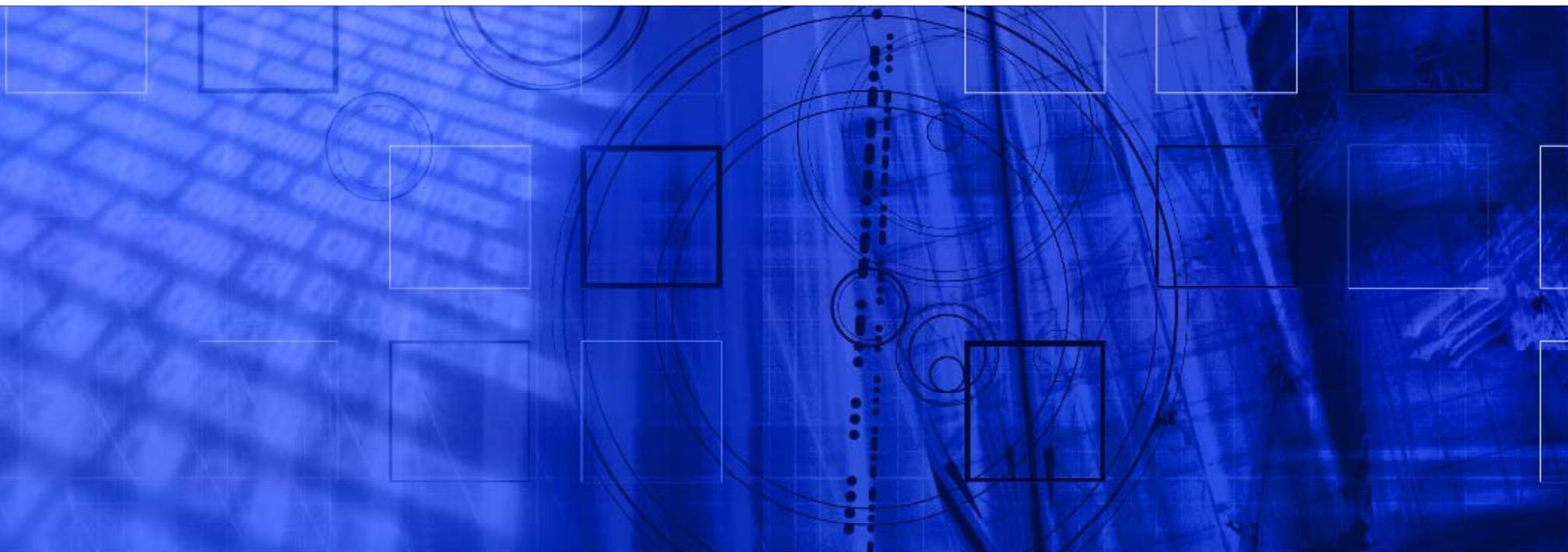
Programmability

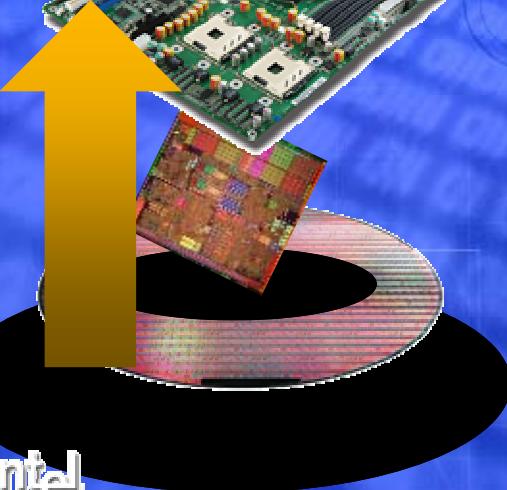




**Scalability**  
Exploiting  
**Concurrency**  
At **Multiple** Levels



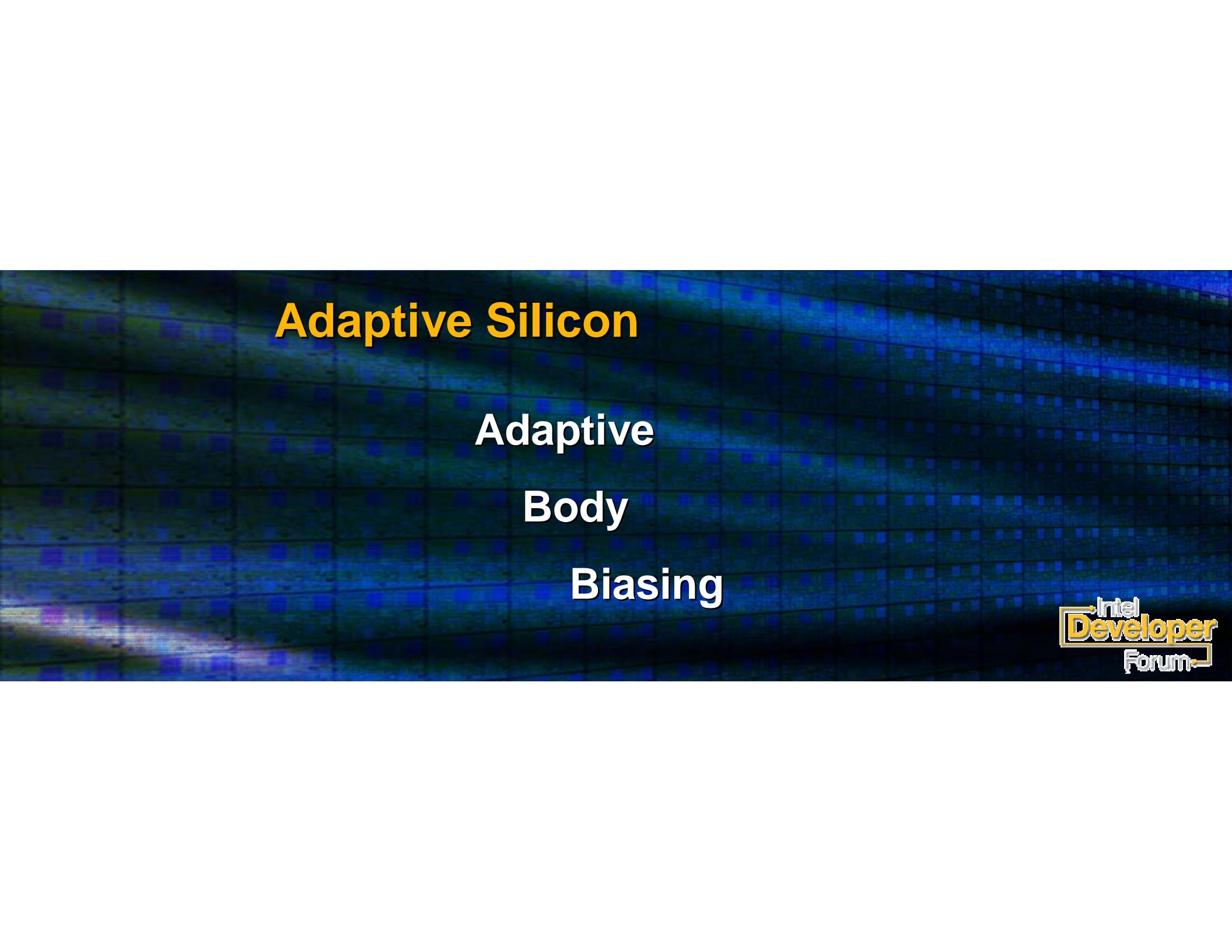




# Adaptability

Adapting To  
*Workload-driven  
Power-performance*  
Requirements

Intel  
**Developer**  
Forum

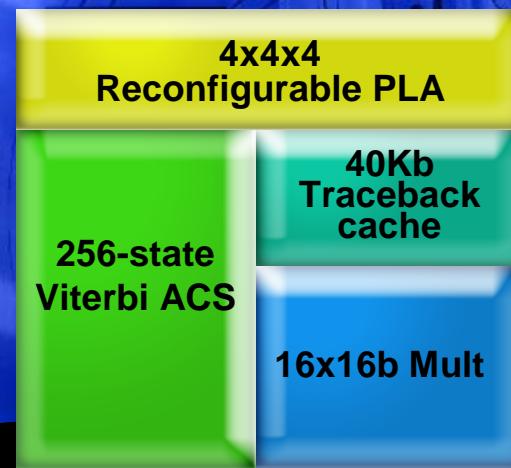


# Adaptive Silicon

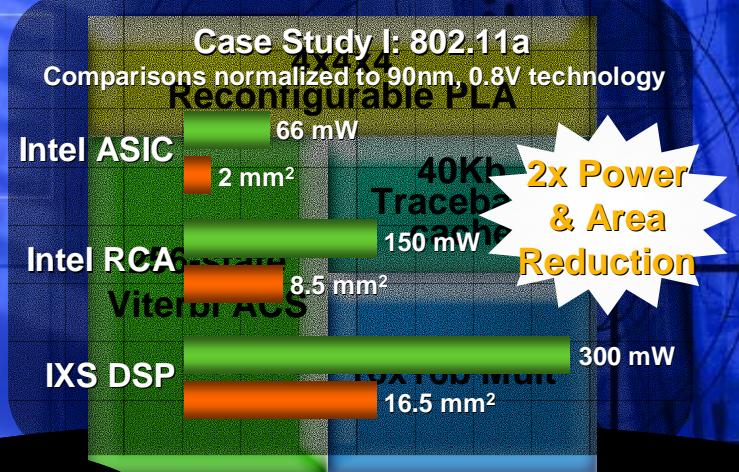
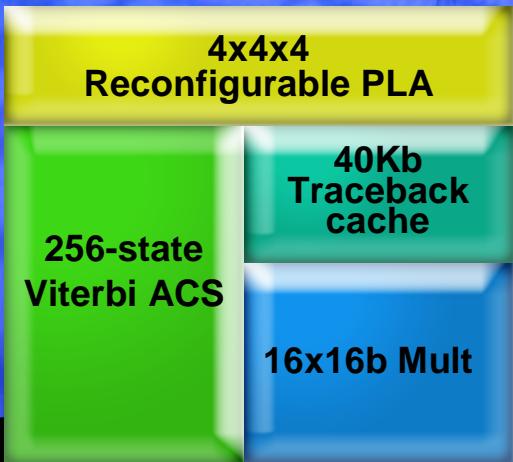
Adaptive  
Body  
Biasing



# Adaptive Micro-architecture



# Adaptive Micro-architecture

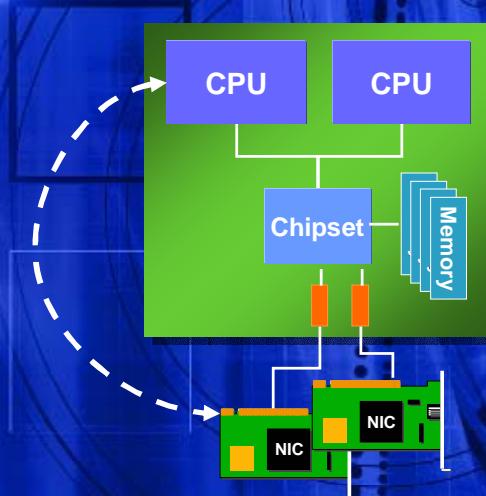


# Adaptive Platform Packet Processing Challenge

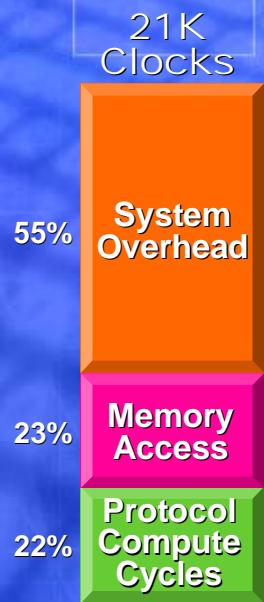
Maximize CPU Cycles For  
User Applications

Yet...

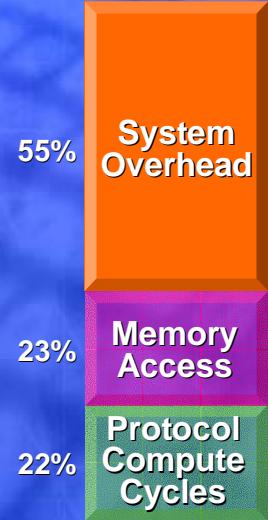
Process Packet Payloads  
At Line Rates



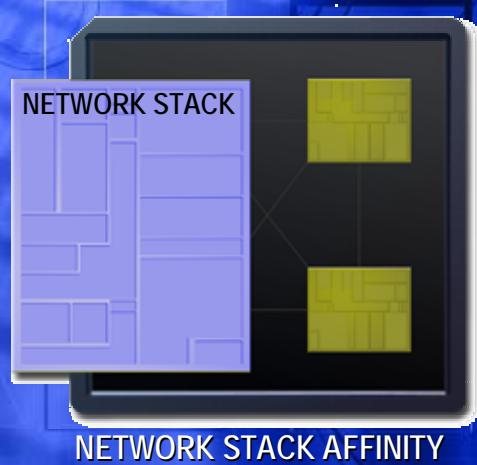
# Adaptive Platform



21K  
Clocks



# Adaptive Platform



21K  
Clocks

55%

**System  
Overhead**

23%

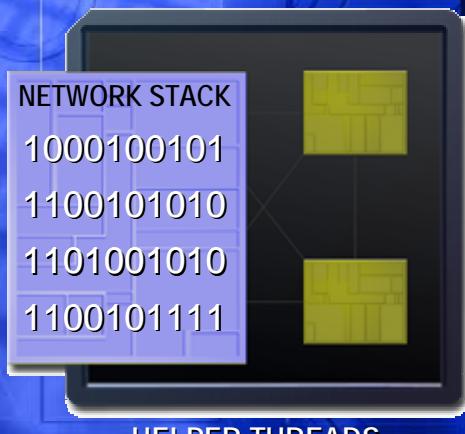
**Memory  
Access**

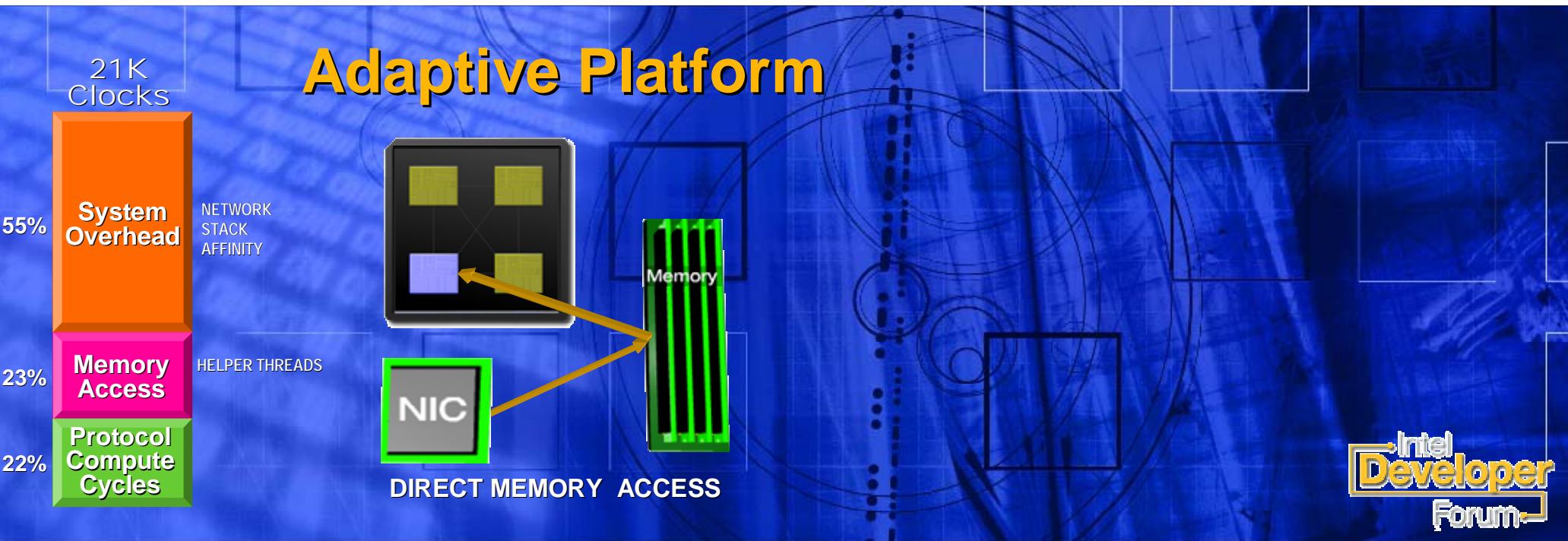
22%

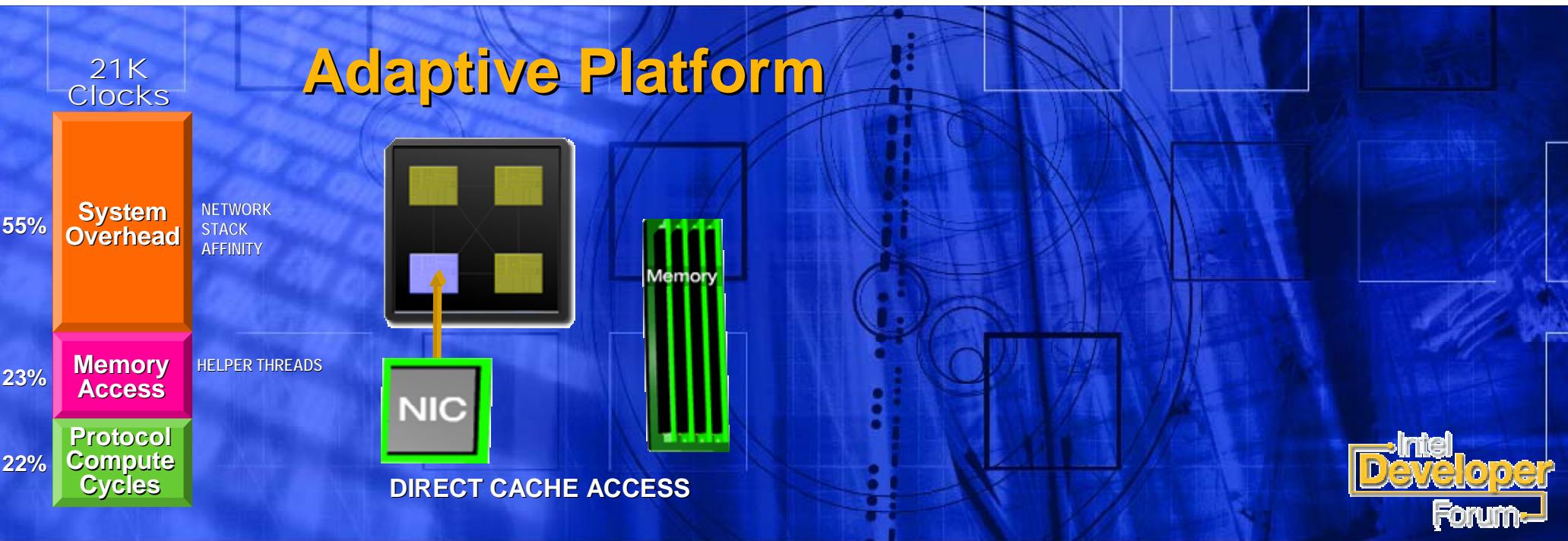
**Protocol  
Compute  
Cycles**

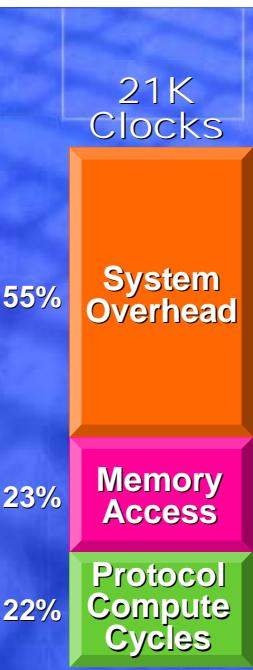
NETWORK  
STACK  
AFFINITY

# Adaptive Platform

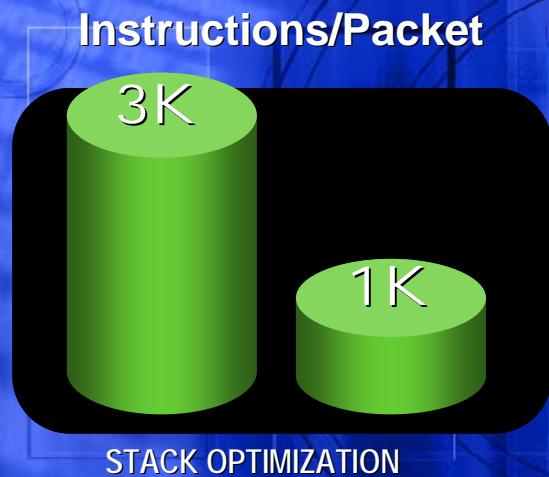






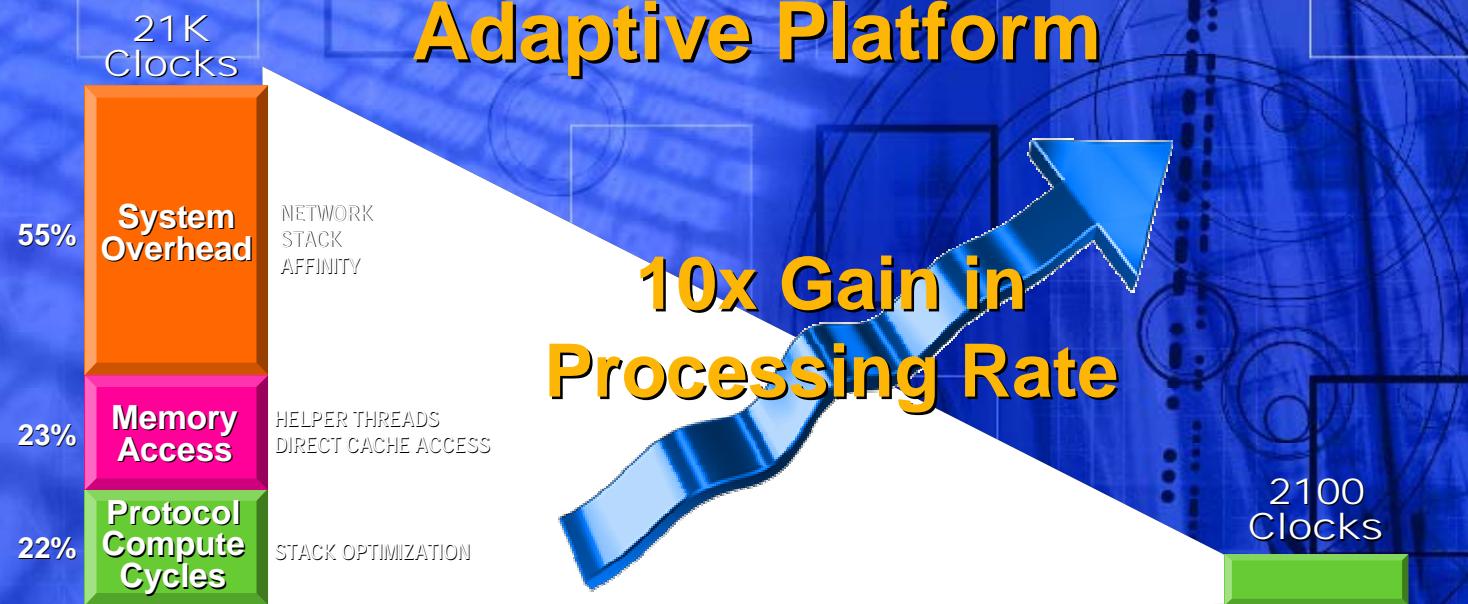


# Adaptive Platform



# Adaptive Platform

10x Gain in  
Processing Rate

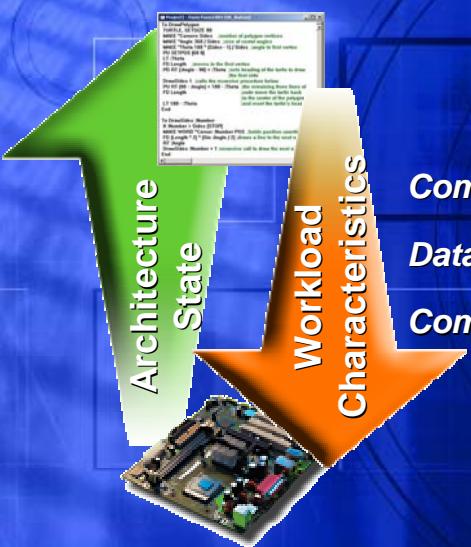


# Programmability



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# Programmability



*Computational Concurrency*

*Data Decomposition*

*Communication/Synchronization*



# Programmability

*Cores/Threads*  
*Adaptable Caches*  
*Adaptable Interconnects*



*Architecture State*  
*Workload Characteristics*

*Computational Concurrency*  
*Data Decomposition*  
*Communication/Synchronization*



# Enabling the Era Of Tera

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# **Enabling the Era Of Tera**

*Innovation = Multi-everywhere*



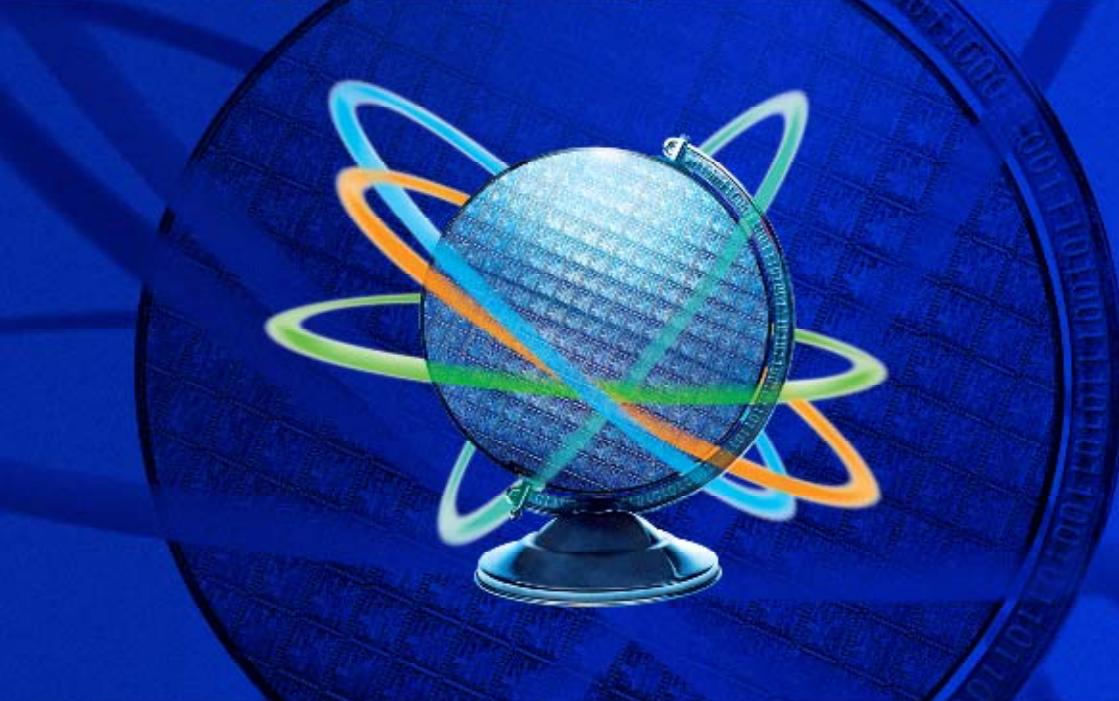


# **Enabling the Era Of Tera**

*Innovation = Multi-everywhere*

*Catalyst = Digital Transformation*

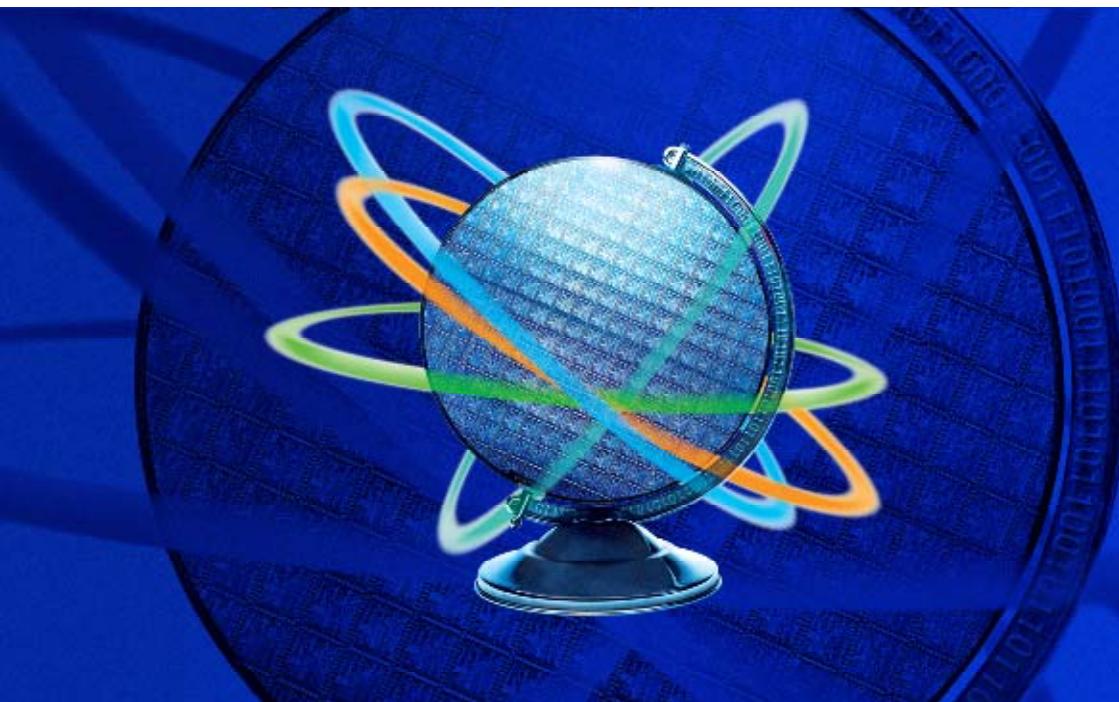




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