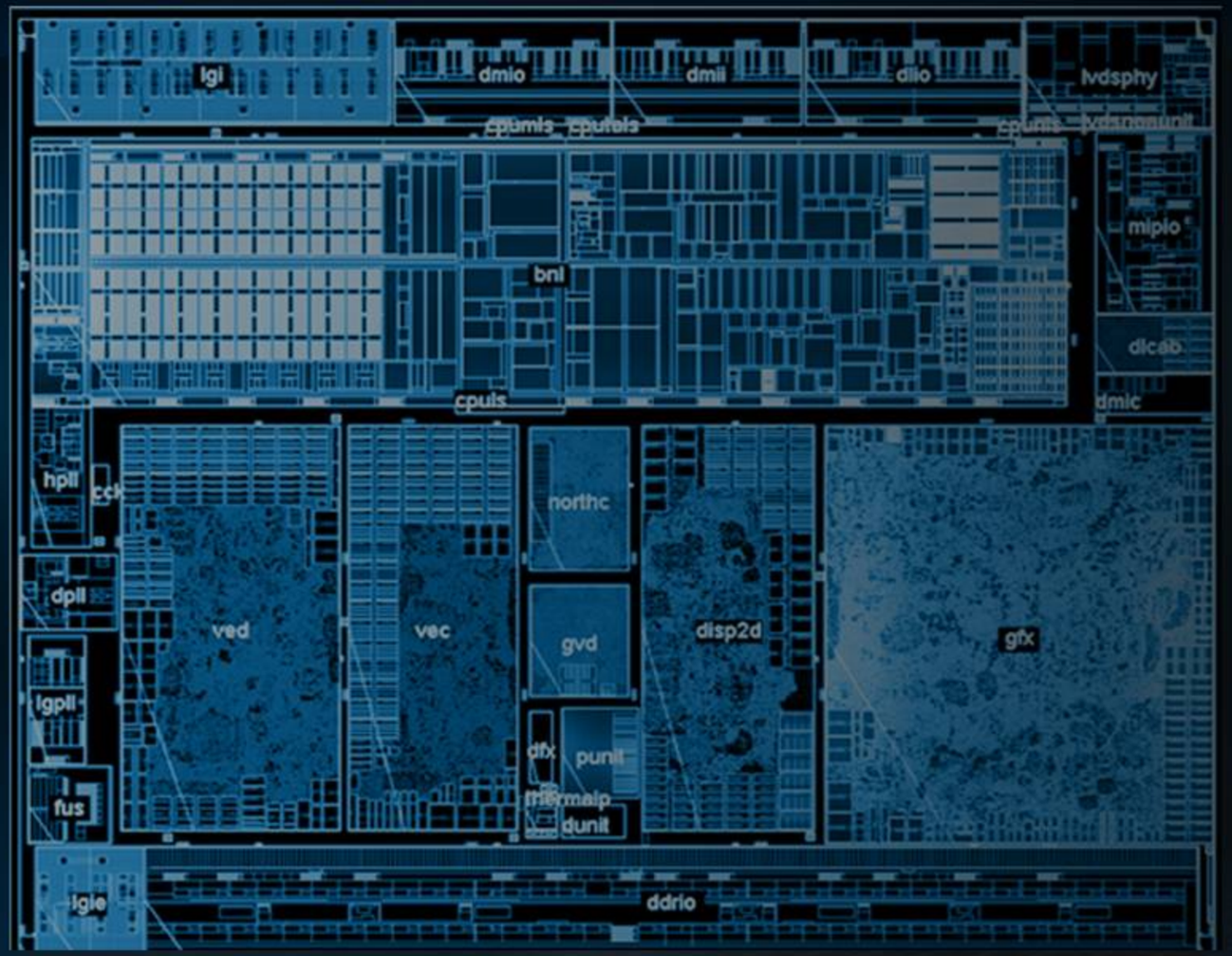


Enabling IA SoCs with Intel's Technology and Manufacturing Innovation

Sunit Rikhi
Vice President, Technology & Manufacturing Group

Shared SoC Design & Manufacturing Technology Layers

SoC DESIGN TECHNOLOGY LAYER

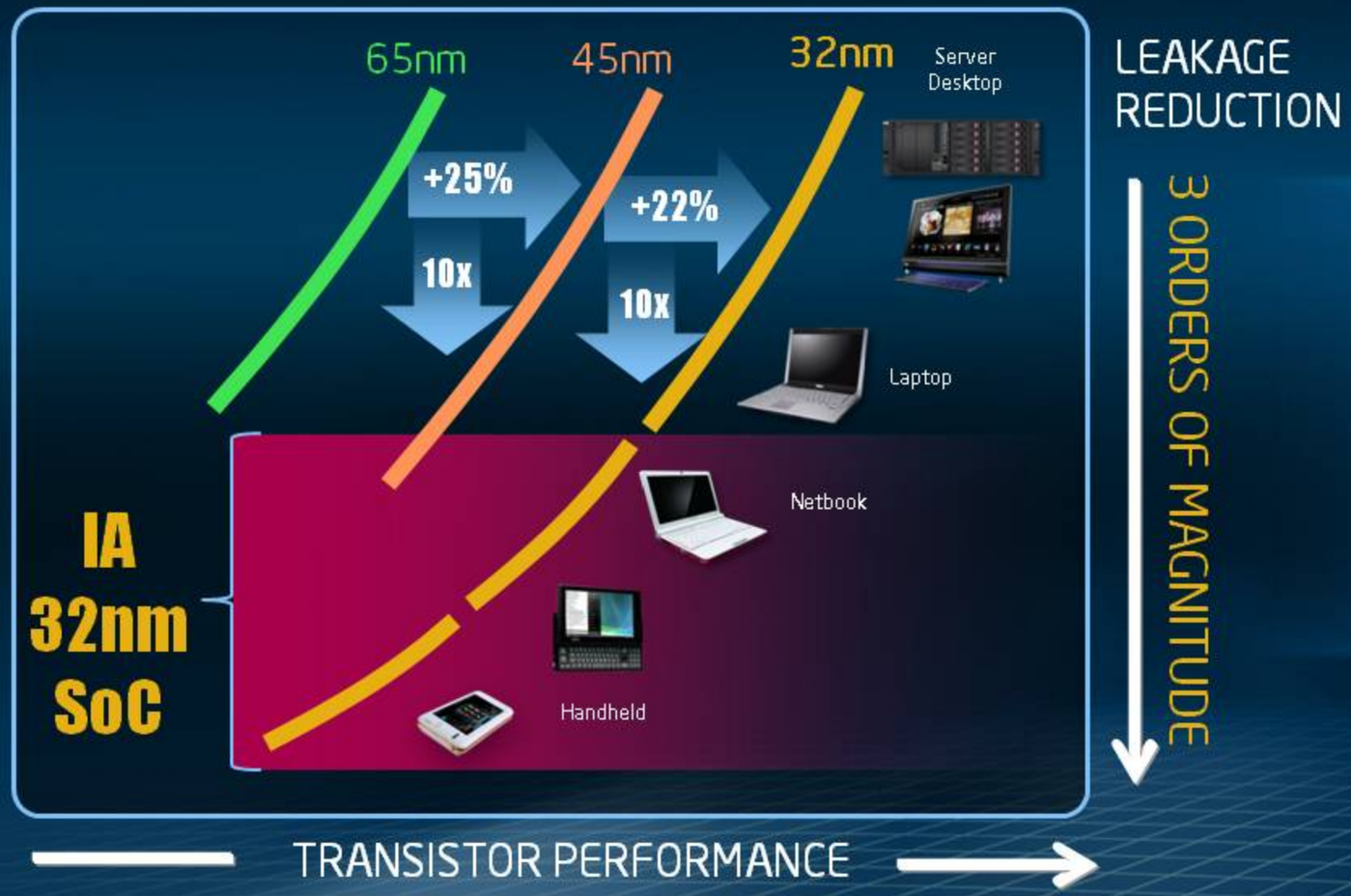
PROCESS TECHNOLOGY & MANUFACTURING LAYER

Shared Process & Manufacturing Technology Layer

PROCESS TECHNOLOGY & MANUFACTURING LAYER

Silicon Process Technology Advantage

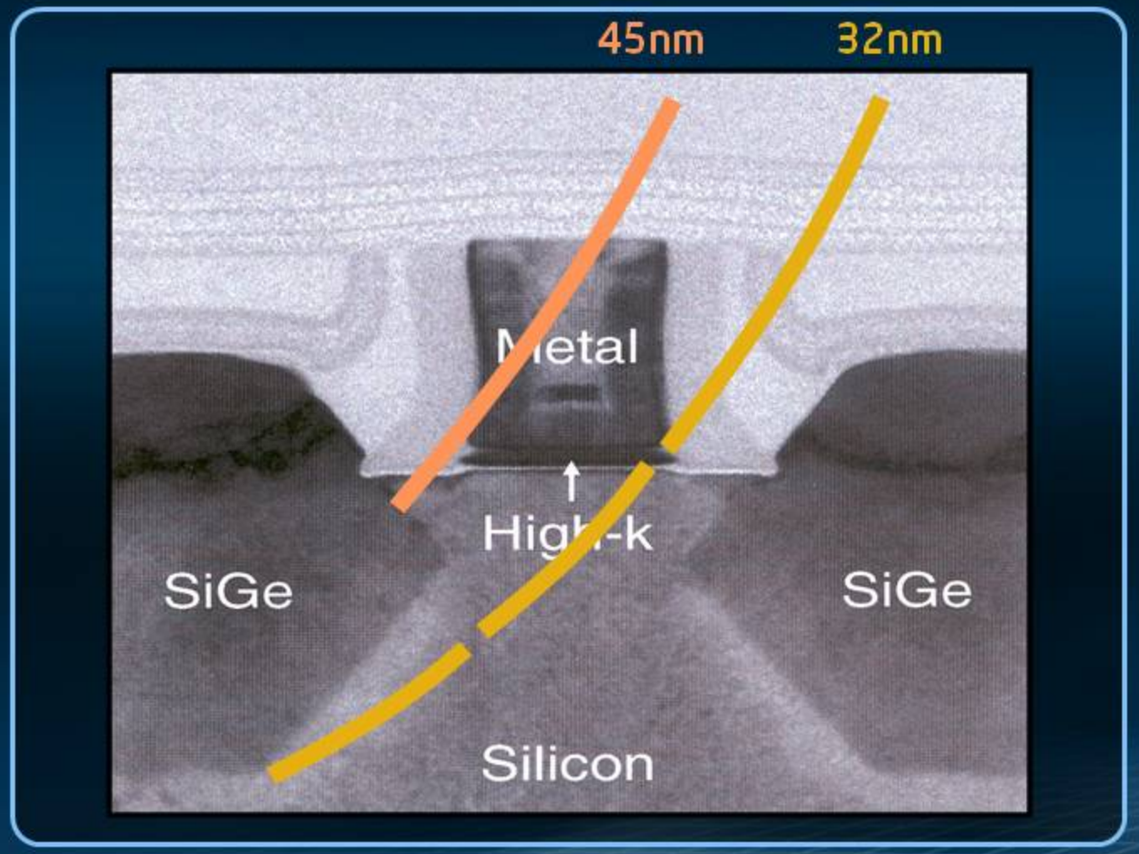
Faster Transistors and Improved Power at 32nm



INTEL 32nm SoC TECHNOLOGY EXTENDS THE REACH OF IA

The Enabler

Intel's Hi-K/Metal Gate Transistor Technology



LEAKAGE REDUCTION

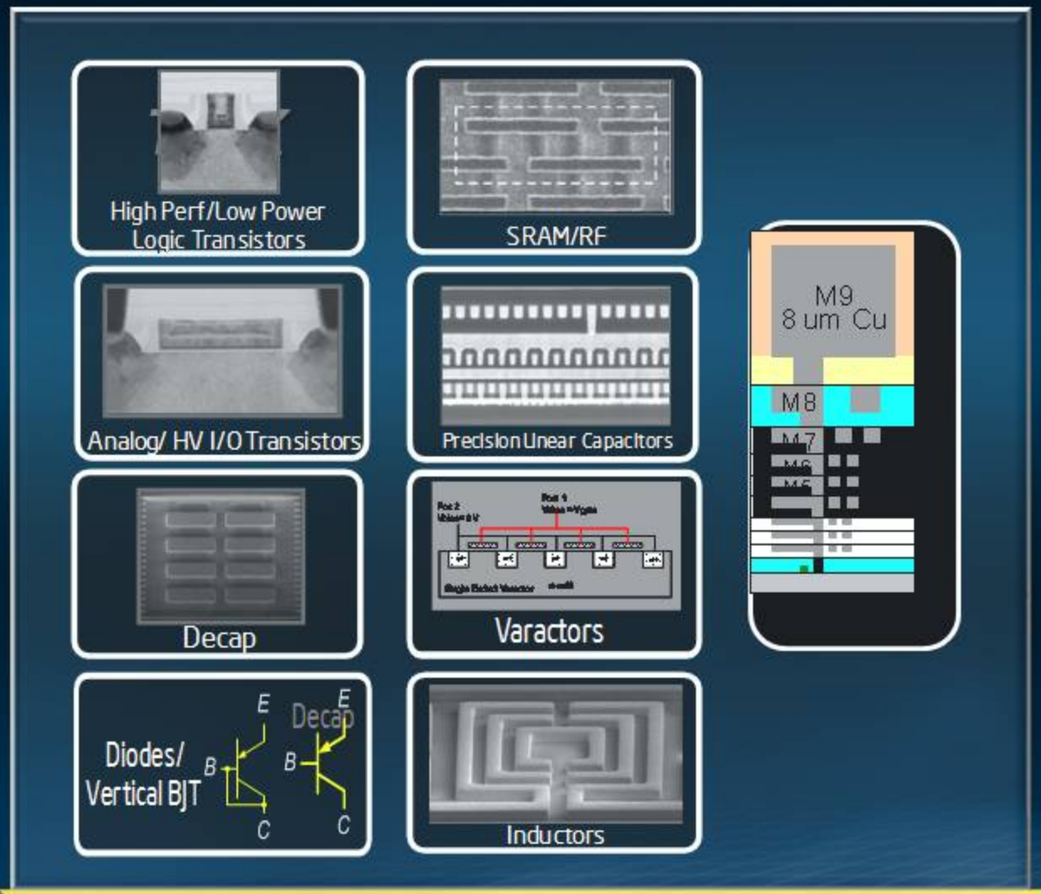
3 ORDERS OF MAGNITUDE

TRANSISTOR PERFORMANCE

45nm: IN PRODUCTION SINCE 2H'07

32nm: ON TRACK FOR 2nd GEN RAMP IN 2H'09. HIGHEST DRIVE CURRENT AND SMALLEST GATE PITCH OF ANY REPORTED 32nm/28nm TECHNOLOGY

32nm SOC Full-Featured Process Menu

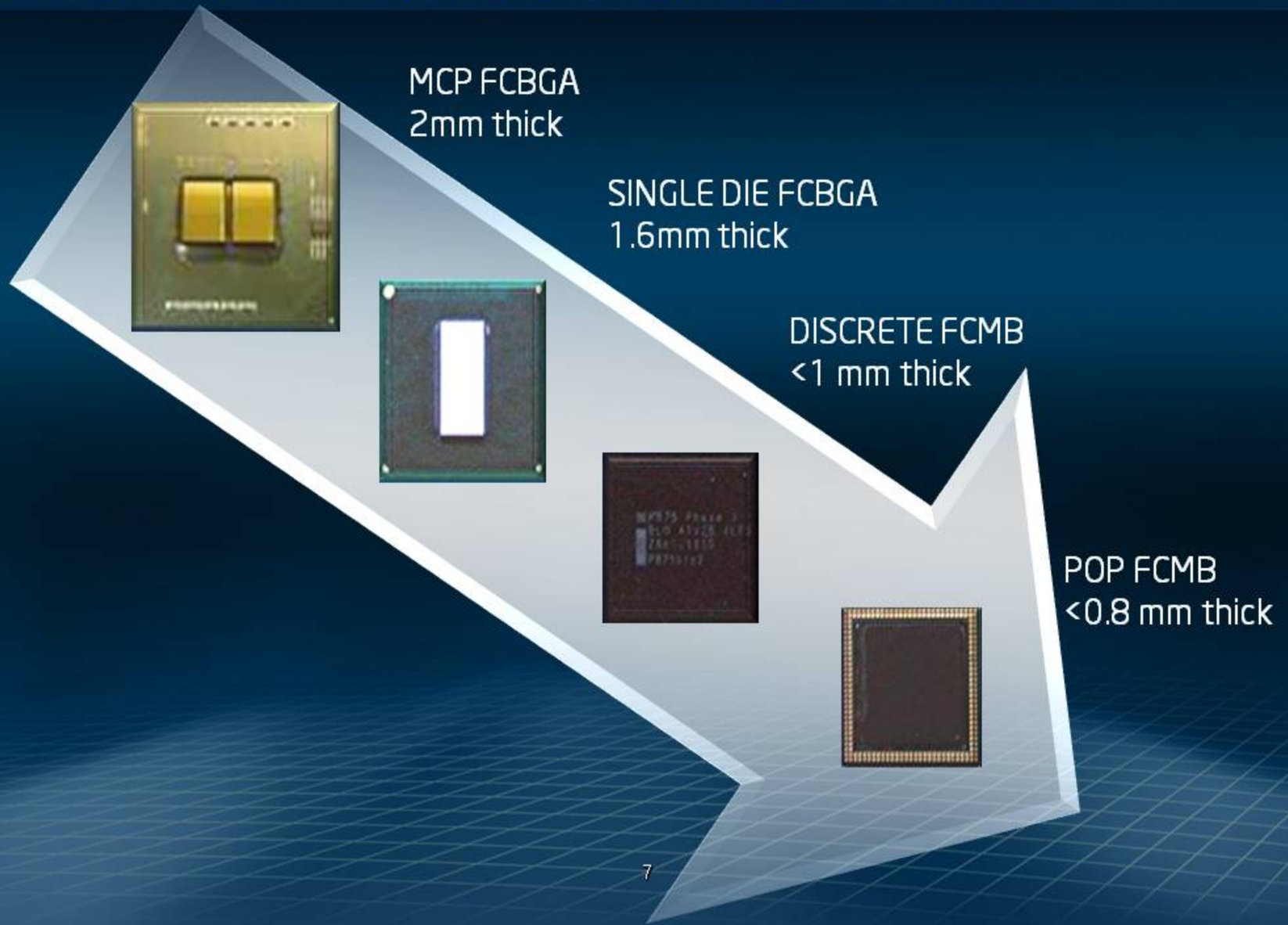


LOGIC TRANSISTOR	HIGH PERF	✓
	STD PERF-PWR	✓
	LOW PWR	✓
	HIGH PERF/LOW PWR	✓
I/O TRANSISTOR	1.8V	✓
	2.5V	✓
	3.3V	✓
METALS	HIGH PERF (CPU)	✓
	HIGH DENSITY	✓
	LOW COST	✓
	ULTRA HIGH DENSITY	✓
EMBEDDED MEMORY	e-SRAM	✓
	E-OTP/FUSE	✓
BASIC ANALOG	MOM, MOS CAP	✓
	INDUCTOR (L)	✓
ADV MIXED SIGNAL/RF	PRECISION R	✓
	PRECISION C	✓
	HIGH Q L	✓
	DEEP N W	✓
	HIGH RES SUB	✓

VARIETY OF OPTIONS TO ENABLE OPTIMIZED SILICON INTEGRATION OF DIVERSE SYSTEM COMPONENTS

Intel 32nm Package Options

Enabling SOC Optimization in Integration, Form Factor and Cost

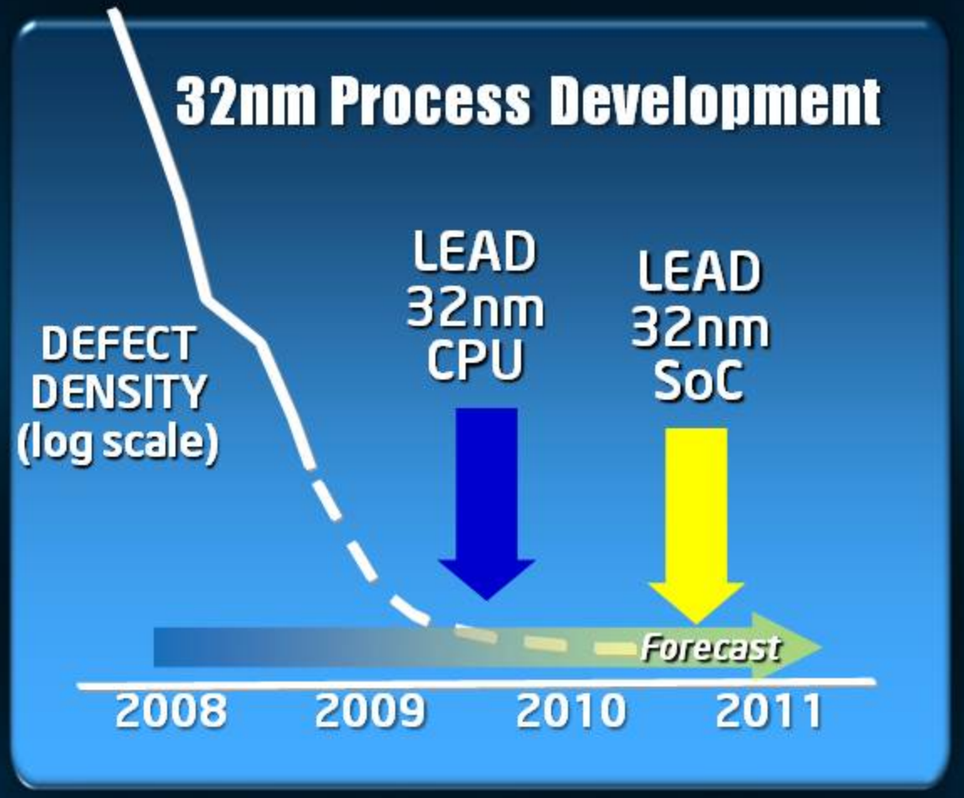


Intel's Lead Free Package Technology

ALL OPTIONS ARE LEAD FREE FOR TECHNOLOGY NODES 45nm AND BELOW

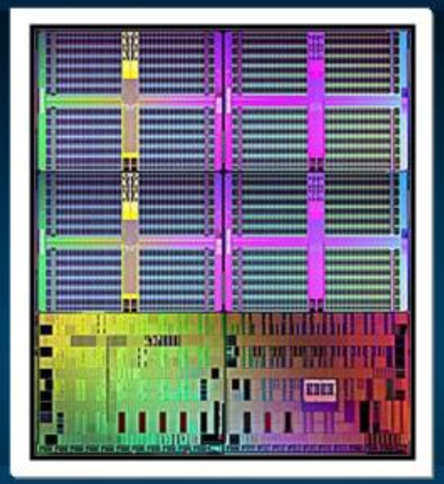
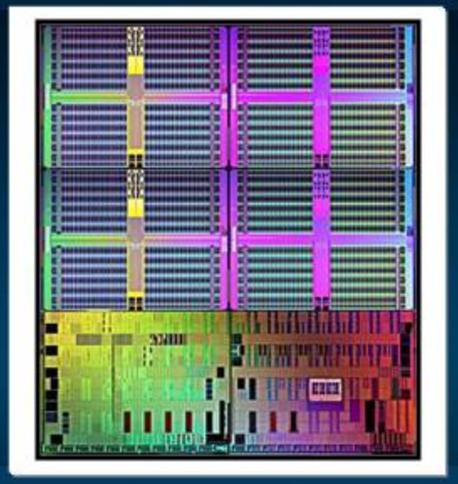
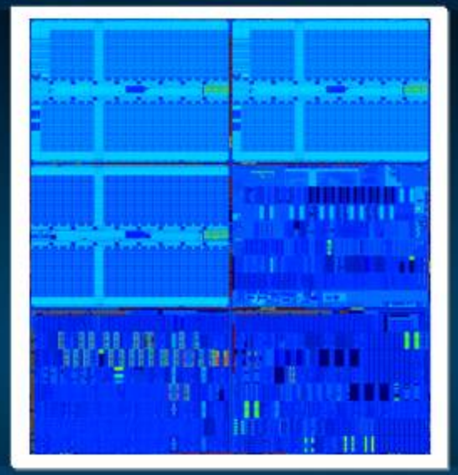
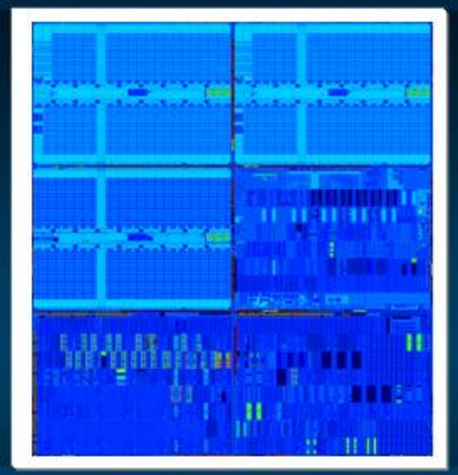
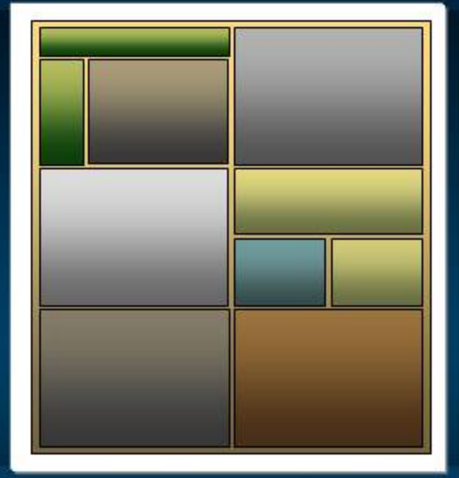
Common Process Platform

Low Power SoC Process...



INTEL's 32nm SOC PROCESS DEVELOPMENT SHARES INVESTMENT AND LEARNING ON A COMMON PLATFORM WITH CPU PROCESS

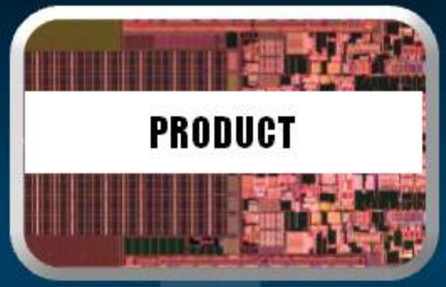
32nm Silicon Shuttles

SHUTTLE:	1	2	3	4	5
SILICON DATE:	Q307	Q208	Q308	Q109	Q309
TECH FOCUS:	CPU TD	CPU Tech Cert	SOC TD	SOC Tech Cert	SOC Feature Refinements
PROD FOCUS:	Lead CPU Memory IP	Lead CPU Memory + Mixed-Signal IP	Lead SOC Memory IP	Lead SOC Memory + Mixed-Signal IP	Multi-Product Mixed Signal IP

UNFOLDING THE MAGIC OF 2nd GEN 32nm TECHNOLOGY

Extending Decades of IDM Co-optimization to SOCs



Co-optimized decisions from definition to ramp

Synchronized execution

Rapid yield learning & ramp

32nm Manufacturing Investment

D1D, Oregon
(now)

F32, Arizona
(2010)*

D1C, Oregon
(Q409)*

F11x, New Mexico
(2010*)

Intel News Release

Intel to Invest $7 Billion in U.S. Manufacturing Facilities

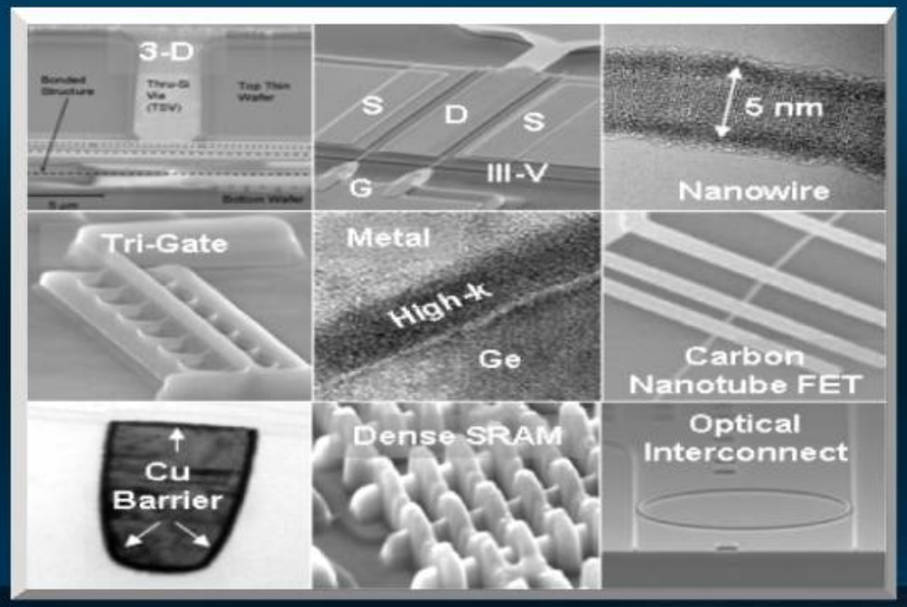
2-Year Plan to Focus on Leading-Edge Technologies

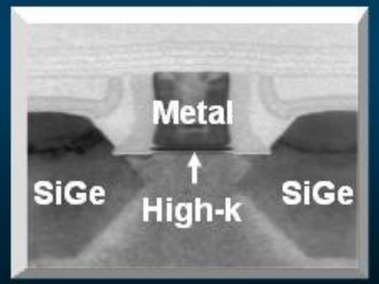
WASHINGTON, DC, Feb. 10, 2009 – Intel President and

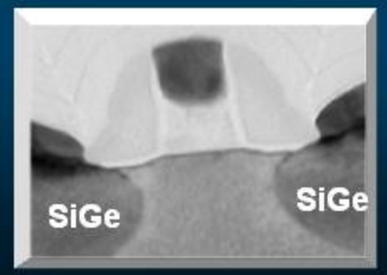
* Projected

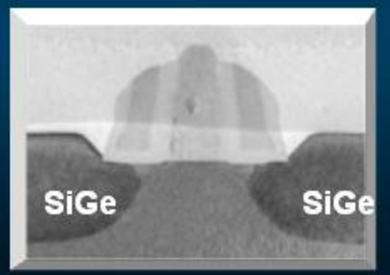
A full, flowing, innovation pipeline

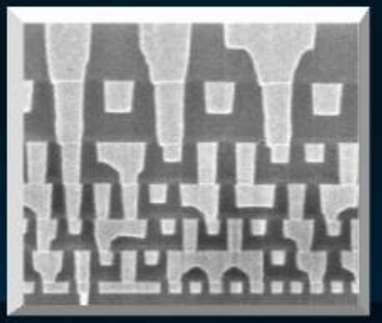
<22nm 2013+	22nm 2011	32nm 2009	45nm 2007	65nm 2005	90nm 2003
RESEARCH	DEVELOPMENT		MANUFACTURING		











AND AS FAR AS WE CAN SEE… THE MAGIC CONTINUES

Future options subject to change

Shared SoC Technology Layer

SoC DESIGN TECHNOLOGY LAYER

PROCESS TECHNOLOGY & MANUFACTURING LAYER

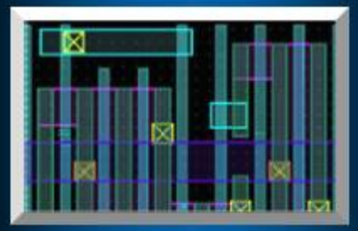
Shared SoC Technology Layer

LEADERSHIP ATOM CORE

MODULAR SHARED IP LIBRARY

COMMON ARCH FRAMEWORK

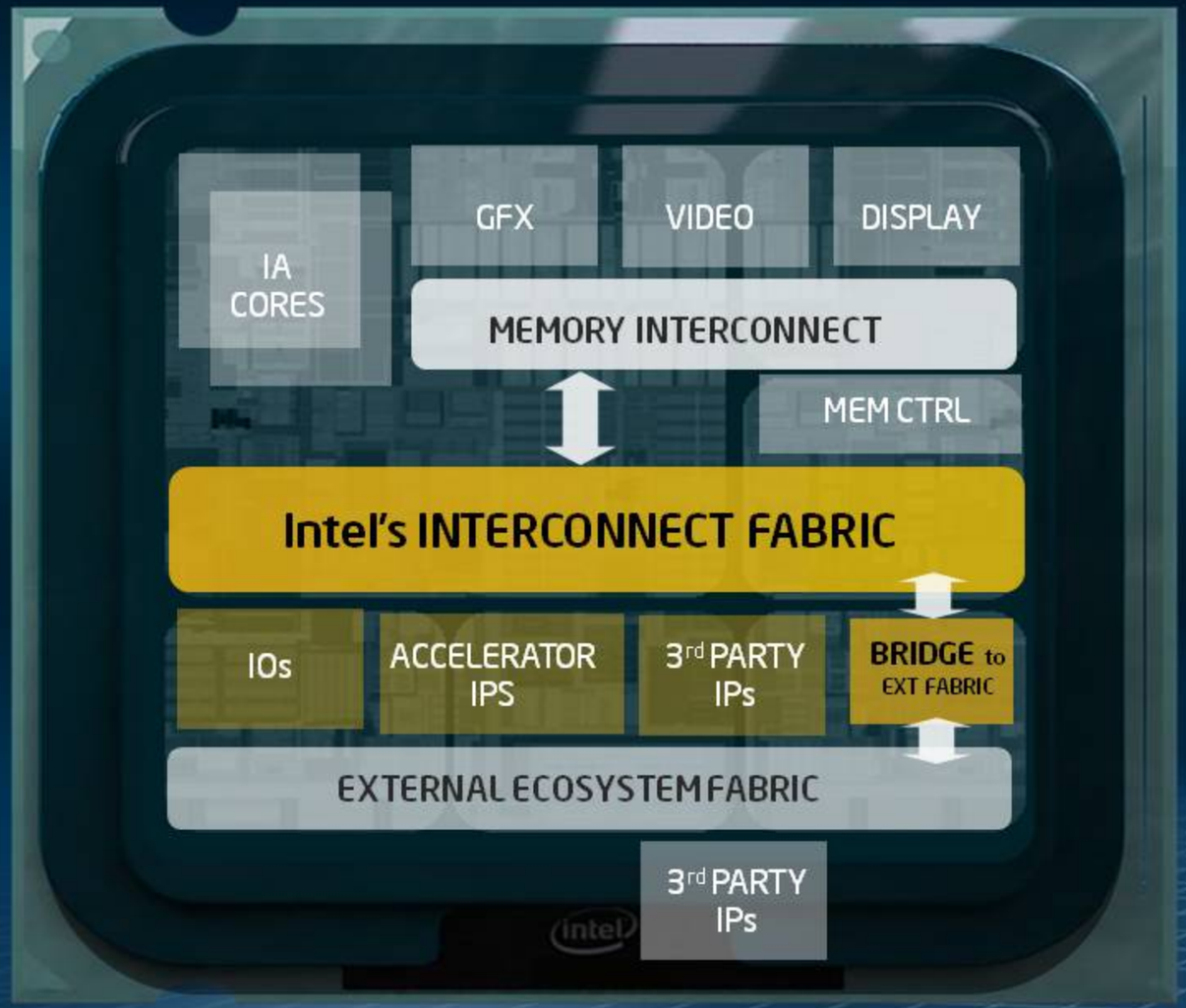
COVERGED TOOLS & METHODOLOGIES



SoC DESIGN TECHNOLOGY LAYER

BENEFITS: TTM; MODULARITY/FLEXIBILITY/CUSTOMIZATION; COST/POWER/PERF/SIZE

IA-based Common Architecture Framework



IA SOFTWARE COMPATIBILITY

MODULAR INTEGRATION

BRIDGE TO EXTERNAL ECOSYSTEM FABRIC

Intel SoC Products

MID

EMBEDDED

CE

Intel Smart SoC Products

EMBEDDED

EP80579

FULL FEATURE SoC
ACCELERATORS
QUICK ASSIST TECH

MIDS

LINCROFT

45nm; ATOM CORE
CPU/GFX/MEM/DISPLAY
ADV. PWR MGMT

CE

CE 3100

15 UNIQUE IP PIECES
AUDIO-VIDEO DECODE
GRAPHICS
DISPLAY PROCESSING

CE

SODAVILLE

45nm; ATOM CORE
SEGMENT OPTIMIZED

+ **FOURTEEN 32nm SoCs IN PROGRESS***

*Future options subject to change

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45nm product is manufactured on a lead-free process. Lead is below 1000 PPM per EU RoHS directive (2002/95/EC, Annex A). Some EU RoHS exemptions for lead may apply to other components used in the product package.

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Q&A

Intel Mid-Summer Technology Summit

July 29, 2009