2008 ISSCC
Intel Paper Highlights

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2008 ISSCC Intel Paper Summary

- **Under embargo until February, 3, 9 p.m. PST 2008**

- 14 new papers
- **Processor Technology**: First details of Silverthorne, the low-power IA processor and Tukwila, the new quad-core Itanium® processor - world's first 2 billion transistor microprocessor
- **Wireless Technology**: Four papers on new wireless developments including the first 65nm CMOS Class E power amp
- **Memory Technology**: Four papers including the world's first demonstrable multi-level cell (MLC) device using PCM technology
- **Tera-scale Technology**: Four papers including 2T gain cell DRAM built on 65nm CMOS technology with 2ns access time
- **Process Technology**: Re-publication of high-K metal gate CMOS technology paper from IEDM

Silverthorne: A Low Power 45nm IA Processor
Optimized for Mobile Internet Devices

"A Sub-1W to 2W Low-Power IA Processor for Mobile Internet Devices in 45nm High-K Metal-Gate CMOS"

- Ground-up new IA micro-architecture designed for low power operation
  - Dual issue in-order pipeline with HT
  - Fully Core 2 Duo ISA compatible
- 10x lower power than ULV Dothan
  - Deep power down (C6) architecture
  - Optimized register-file and cache 6T bit cells
  - CMOS mode on quad-pumped FSB IO
  - Split IO power supply

Sea-of-FUBs Chip Layout

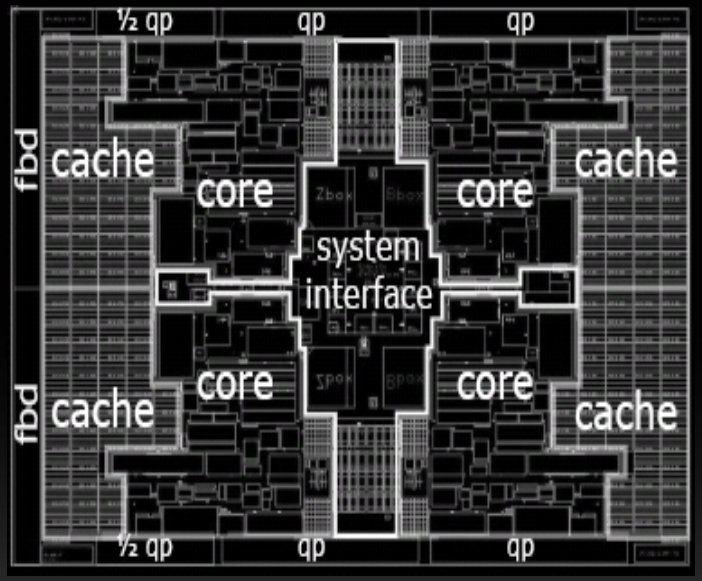
Mobile Internet Devices

High Performance and Low Power Architecture Enables Full Internet Experience in Your Pocket

Tukwila: New Quad-Core Itanium® Processor
Worlds first 2 Billion Transistor Microprocessor

"A 65nm 2-Billion-Transistor Quad-Core Itanium® Processor"

- Upto 2GHz, Quad Core w/ Multi-Threading (8T)
- >2x* performance vs Dual-Core Itanium® Processor 9100 series
- 30MB on-die cache
- QuickPath interconnect and dual integrated memory controllers
- Advanced RAS
- Energy Efficiency

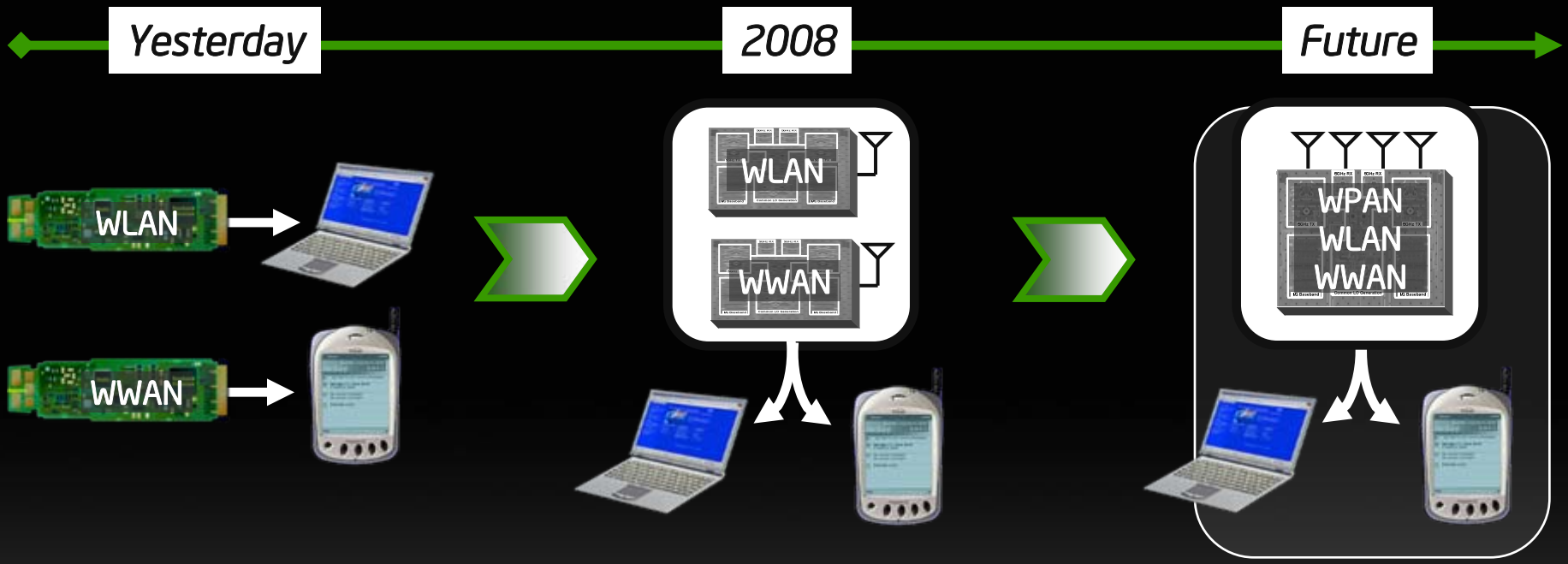


Tukwila Micrograph

~2x performance at 25% more power (130W sku)

*>2x Performance ➔ This is based on comparison between Intel's performance projections (1/15/08) on 4-socket benchmarks (TPC-C, SpecintRate, and SpecfpRate) for Tukwila Vs measurements on Intel Itanium® Processor 9100 Series (Montvale)

The Wireless "Radio" Evolution



Discrete Radios

One standard

Bulky, costly

Inflexible

Integrated Radios

Full CMOS Integration

Dual-standard

+Performance, -Cost, -TTM

Digital Multi-Radios

Reconfigurable CMOS Radios

Multi-standard

Tunable antenna

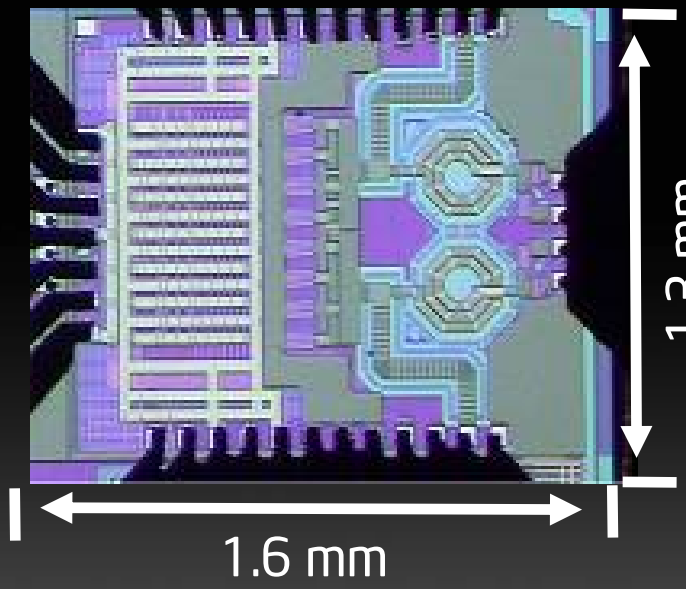
Vision: Connectivity Anytime, Anywhere for Everyone

65nm CMOS Power Amplifier for Multi-Radio

Worlds first Class E PA at 65nm

"A 28.6dBm, 65nm Class-E PA with Envelope Restoration by Pulse-Width and Pulse-Position Modulation"

- Delivers close to 1 Watt RF output power for WWAN
- Uses novel digital technique to introduce complex modulation required for high data rates
- Implemented in digital 65nm CMOS process for easy integration with other digital processing



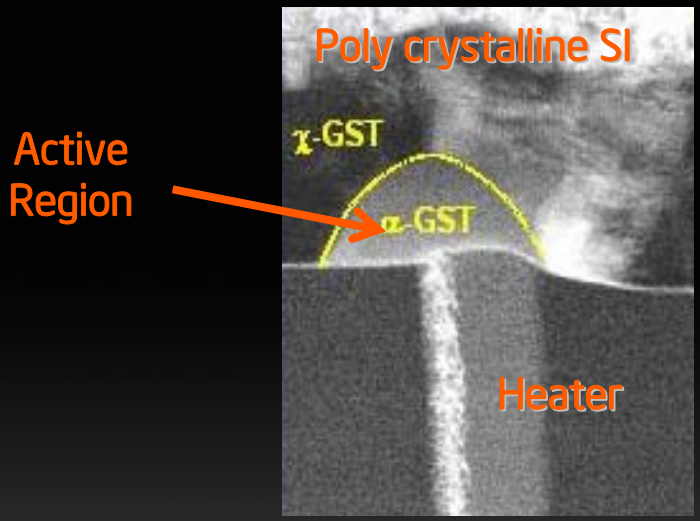
First Class E PA in 65nm CMOS (28.6dBm power output)

Multi-Level Phase Change Memory*

First demonstrable MLC device using PCM technology

"A Multi-Level Cell Bipolar-Selected Phase Change Memory"

- 256 Mbit 90nm micro-trench technology
- A new "programming algorithm" creating two additional states between amorphous and crystalline
- Similar to observing H_2O in either a liquid (water) state or in a crystalline (ice) state.



World's first demonstrable multi-level cell (MLC) device using PCM technology

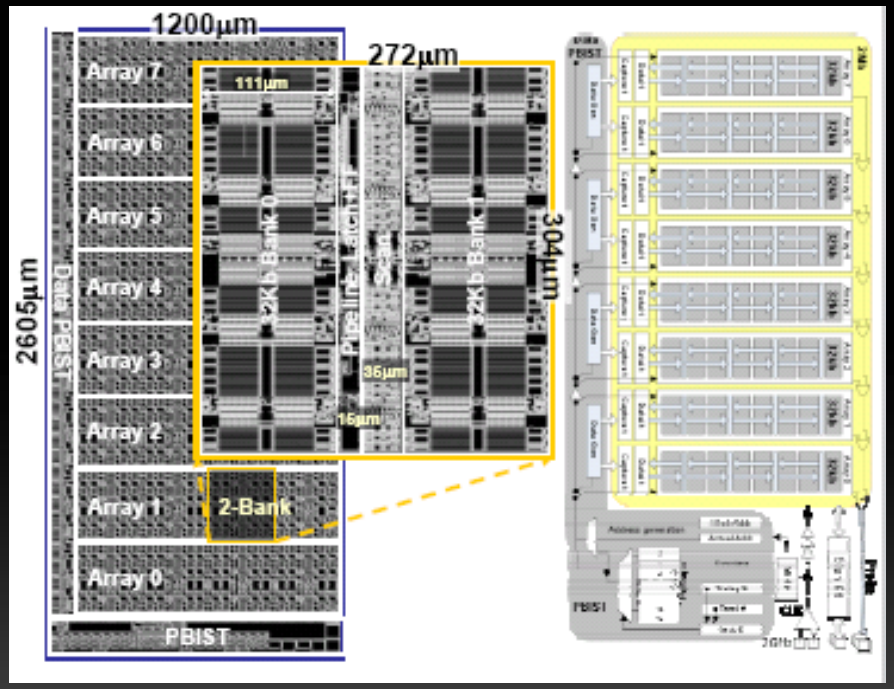
* Joint Development between Intel and ST Microelectronics

High-Density Integrated Memory

2T gain cell DRAM built on 65nm CMOS technology

"2GHz 2Mb 2T Gain-Cell Memory Macro with 128GB/s Bandwidth in a 65nm Logic Process"

- Twice the memory density vs. on-chip SRAM
- Much faster than DRAM: 128GB/s running at 2GHz
- 2ns access time
- Sustains 8-cycle successive access to the same memory bank



2Mbit macro with view of 2-bank and macro organization.

Fast DRAM built on native 65nm CMOS Technology

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- **Memory Technology**: Four papers including the world's first demonstrable multi-level cell (MLC) device using PCM technology
- **Tera-scale Technology**: Four papers including 2T gain cell DRAM built on 65nm CMOS technology with 2ns access time
- **Process Technology**: Re-publication of high-K metal gate CMOS technology paper from IEDM

List of Papers (15)

- PROCESSOR
  - "A Sub-1W to 2W Low-Power IA Processor for Mobile Internet Devices in 45nm High-K Metal-Gate CMOS"
  - "A 65nm 2-Billion-Transistor Quad-Core Itanium® Processor"
- WIRELESS TECHNOLOGY
  - "A 1x2 MIMO Multi-Band CMOS transceiver with an integrated Front End in 90nm CMOS for 802.11agn WLAN applications"
  - "A 28.6dBm, 65nm Class-E PA with Envelope Restoration by Pulse-Width and Pulse-Position Modulation"
  - "A 28mW Spectrum-Sensing Reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT ΔΣ ADC for 802.11n/WiMax Receivers"
  - A 39.1-to-41.6GHz ΣΔ Fractional-N Frequency Synthesizer in 90nm CMOS
- MEMORY TECHNOLOGY:
  - "A Multi-Level Cell Bipolar-Selected Phase Change Memory."
  - "A 45nm Self-Aligned-Contact Process 1Gb NOR Flash with 5MB/s Program Speed."
  - "A 50nm 8Gb NAND Flash Memory with 100MB/s Program Throughput and 200MB/s DDR Interface"
- TERA-SCALE:
  - "A 27Gb/s Forwarded-Clock I/O Receiver using an injection-Locked LC-DCO in 45nm CMOS"
  - "Energy-Efficient and Metastability-Immune Timing-Error Detection and Instruction-Replay-Based Recovery Circuits for Dynamic-Variation Tolerance"
  - "A 320mV 56 μW 411GOPS/W Ultra-Low Voltage Motion Estimation Accelerator in 65nm CMOS"
  - "2GHz 2Mb 2T Gain-Cell Memory Macro with 128GB/s Bandwidth in a 65nm Logic Process"
- 45NM HIGH-K METAL GATE PROCESS TECHNOLOGY
  - "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free1 Packaging"
  - "A 153Mb-SRAM Design with Dynamic Stability Enhancement and Leakage Reduction in 45nm High-K Metal-Gate CMOS Technology"

Processor Technology Papers

"A 65nm 2-Billion-Transistor Quad-Core Itanium® Processor"

- World's first 2B+ Transistor Microprocessor ➔ Enables a big leap in performance and capabilities e.g. quad-core, higher system integration, advanced RAS (Reliability, Availability, Serviceability, large cache (30MB) and QuickPath architecture ➔ New high-speed QuickPath interconnect and dual QuickPath integrated memory controllers coupled with leading-edge RAS.
- Quad-core coupled with higher bandwidths and large caches enable doubling the performance of Tukwila over the current Intel® Itanium® 9100 series processor

"A Sub-1W to 2W Low-Power IA Processor for Mobile Internet Devices in 45nm High-K Metal-Gate CMOS"

- The 45nm high-k metal-gate silverthorne microarchitecture will implement ground-breaking power management techniques to aggressively reduce dynamic and leakage power.

*>2x Performance ➔ This is based on comparison between Intel's performance projections (1/15/08) on 4-socket benchmarks (TPC-C, SpecintRate, and SpecfpRate) for Tukwila Vs measurements on Intel Itanium® Processor 9100 Series (Montvale)

3x Logic Circuits ➔ This is based on doubling the cores and a new crossbar-based system interface (about the size of two cores)

Wireless Technology Papers

"A 1x2 MIMO Multi-Band CMOS transceiver with an integrated Front End in 90nm CMOS for 802.11agn WLAN applications"

- Complete transceiver implemented in standard 90nm CMOS process for low power consumption, low cost and small form factors such as mobile internet devices, handheld or PDAs

"A 28mW Spectrum-Sensing Reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT ΔΣ ADC for 802.11n/WiMax Receivers"

- First reconfigurable ADC proves increased process speed can be exploited for better performance; Lowest power consumption in its class; enables a radio to support WiFi/WiMAX bandwidths in a power efficient manner.

"A 39.1-to-41.6GHz ΣΔ Fractional-N Frequency Synthesizer in 90nm CMOS"

- First mm-wave CMOS synthesizer with <3kHz frequency resolution. Wirelessly transfer a full HD movie from one device to another in under one minute (compared to 1.5 hours for legacy WLAN)

"A 28.6dBm, 65nm Class-E PA with Envelope Restoration by Pulse-Width and Pulse-Position Modulation"

- First Class E power amplifier in 65nm CMOS

Memory Technology Papers

"A 153Mb-SRAM Design with Dynamic Stability Enhancement and Leakage Reduction in 45nm High-K Metal-Gate CMOS Technology"

- High-performance and low-power SRAM based on the industry's first 45nm high-k metal gate technology; provides a 2x density improvement, 10x leakage reduction, and 27 percent frequency increase over Intel's 65nm technology

"A 45nm Self-Aligned-Contact Process 1Gb NOR Flash with 5MB/s Program Speed."

- Smallest reliable flash cell in 45nm high-k metal gate technology
- 5 MB/sec program performance, the smallest periphery circuitry, and a robust sense scheme

""A 50nm 8Gb NAND Flash Memory with 100MB/s Program Throughput and 200MB/s DDR Interface"

- New high speed NAND flash technology that can greatly enhance access and transfer of data in devices using silicon for storage

A Multi-Level Cell Bipolar-Selected Phase Change Memory"

- Provides for very fast read and writes at lower power than conventional flash; Allows for more stable data retention; Higher density at lower cost per Mbyte

Tera-scale Technology Papers

"Energy-Efficient and Metastability-Immune Timing-Error Detection and Instruction-Replay-Based Recovery Circuits for Dynamic-Variation Tolerance"

- A test chip with approximately 30% performance gain by "overclocking" the chip and up to 30% reduction in energy consumption by reducing voltage

"2GHz 2Mb 2T Gain-Cell Memory Macro with 128GB/s Bandwidth in a 65nm Logic Process"

- New category of integrated DRAM memory increasing performance of future tera-scale applications: Twice the memory density vs. on-chip SRAM, faster than DRAM: 128GB/s running at 2GHz

"A 320mV 56μW 411GOPS/W Ultra-Low Voltage Motion Estimation Accelerator in 65nm CMOS"

- Video motion-estimation accelerator could enable ultra-low power video encoding for mobile devices; 10x better throughput than best reported accelerator; ultra-low voltage of 0.3V yields

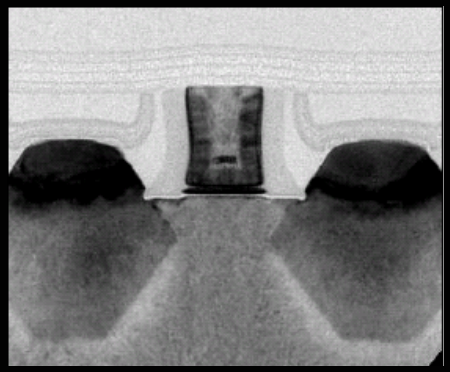
"A 27Gb/s Forwarded-Clock I/O Receiver using an injection-Locked LC-DCO in 45nm CMOS"

- *The best energy efficiency of any I/O receiver over 20Gb/s: 1.6mW/Gb/s*

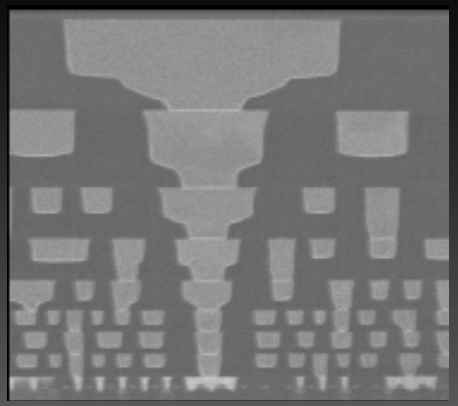
Process Technology 45nm Technology

"A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free1 Packaging"

- The 'first' use of trench (rectangular) contacts to replace square contacts, for improved performance and local routing capability for improved layout density
- The technology features the smallest transistor pitch reported at the 45nm generation, providing better transistor packing density as well as a small static random access memory (SRAM) cell size of 0.346µm2.
- The process features nine copper interconnect layers with extensive use of low-k interlayer dielectrics for improved power and performance integrated with lead-free1 packaging
- For the first time, the process integrates a very thick copper power redistribution interconnect layer using a polymer inter layer dielectric (ILD).



TEM micrograph of high-k + metal gate PMOS transistor



TEM Micrograph Cross-section of 8 of the 9 Cu interconnect layers