Silicon Technology Leadership and the New Scaling Paradigm

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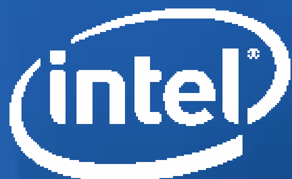
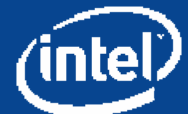
Santa Clara
June 20, 2007



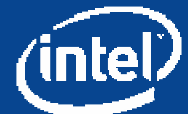
Key Messages

- Intel's R&D pipeline will sustain Moore's Law for the foreseeable future
- 45 nm high-k + metal gate is the most significant innovation in transistor technology in 40 years
- Intel has removed 100 percent of the lead across its entire portfolio of packages in its 45nm family of microprocessors
- Intel continues its unwavering commitment to support R&D for future technologies and to deliver the benefits of Moore's Law to our customers



Outline

- Intel's Silicon R&D Pipeline
- From Geometrical Scaling to Equivalent Scaling
- DFM
- Getting the Lead out
- Future Technology Options
- Summary



Delivering Moore's Law

Feature Size (um)

10
1
0.1
0.01
1970 1980 1

Smalle

Cost per Transistor ($)

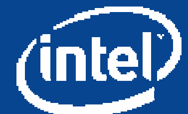
10^{0}
10^{-3}
10^{-6}
10^{-9}
1970 1980 19

Lower cost

Transistor Count

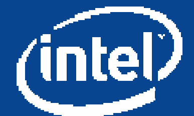
10^{9}
10^{6}
10^{3}
1970 1980 1990 2000 2010 2020

Enables more transistors and increased performance



Moore's Law =

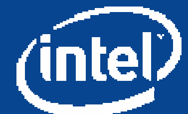
Transistor Budget +
Lowest Power and Lowest Cost



Intel's Silicon R&D Pipeline

Research Development Manufacturing

Continuous flow of new technologies from research to development to manufacturing



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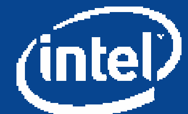
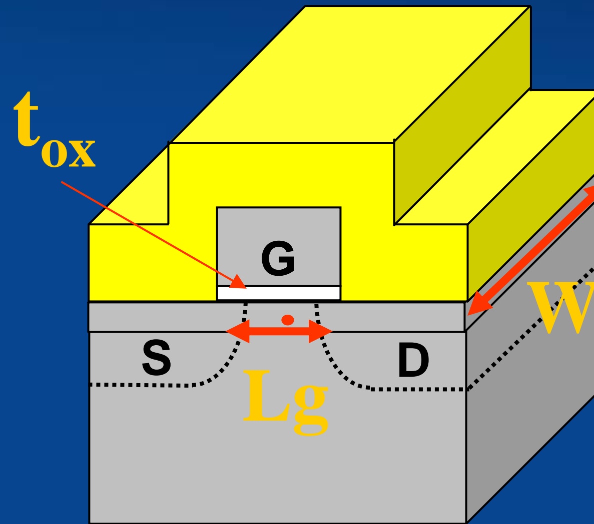


Transistor Trade-offs

$$I_{DSat} \sim \frac{1}{2} \mu C_{ox} \left(\frac{W}{Lg}\right)(V_{DD} - V_T)^2$$

Increase Cox

=>Reduce t_{ox}

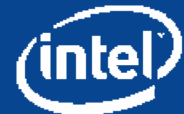


Reduce **Lg**

Reduce V_{DD}

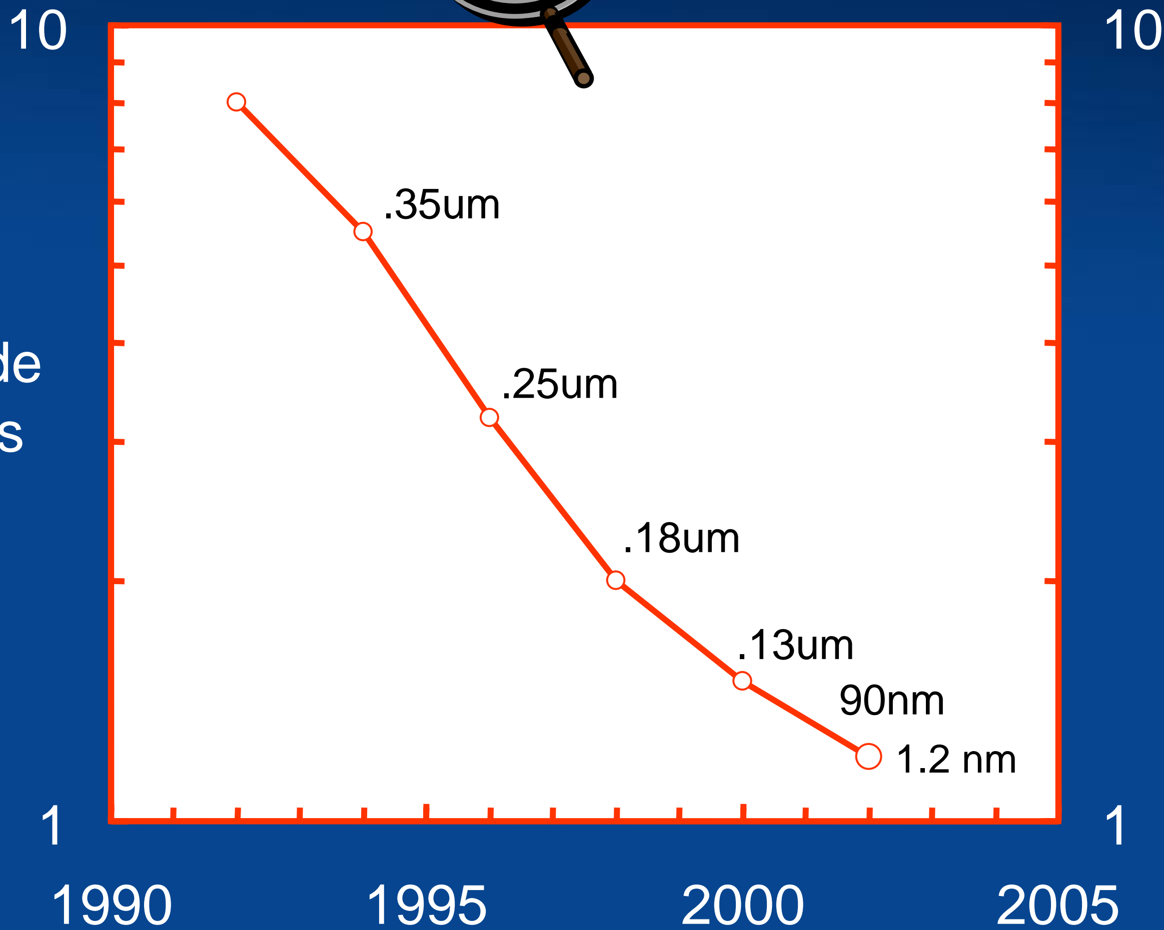
$$F_{Max} = I_{DSat} / V_{DD} C_{ox}$$

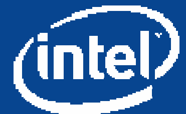
$$Power = V_{DD}^2 C_{ox} F_{Max}$$



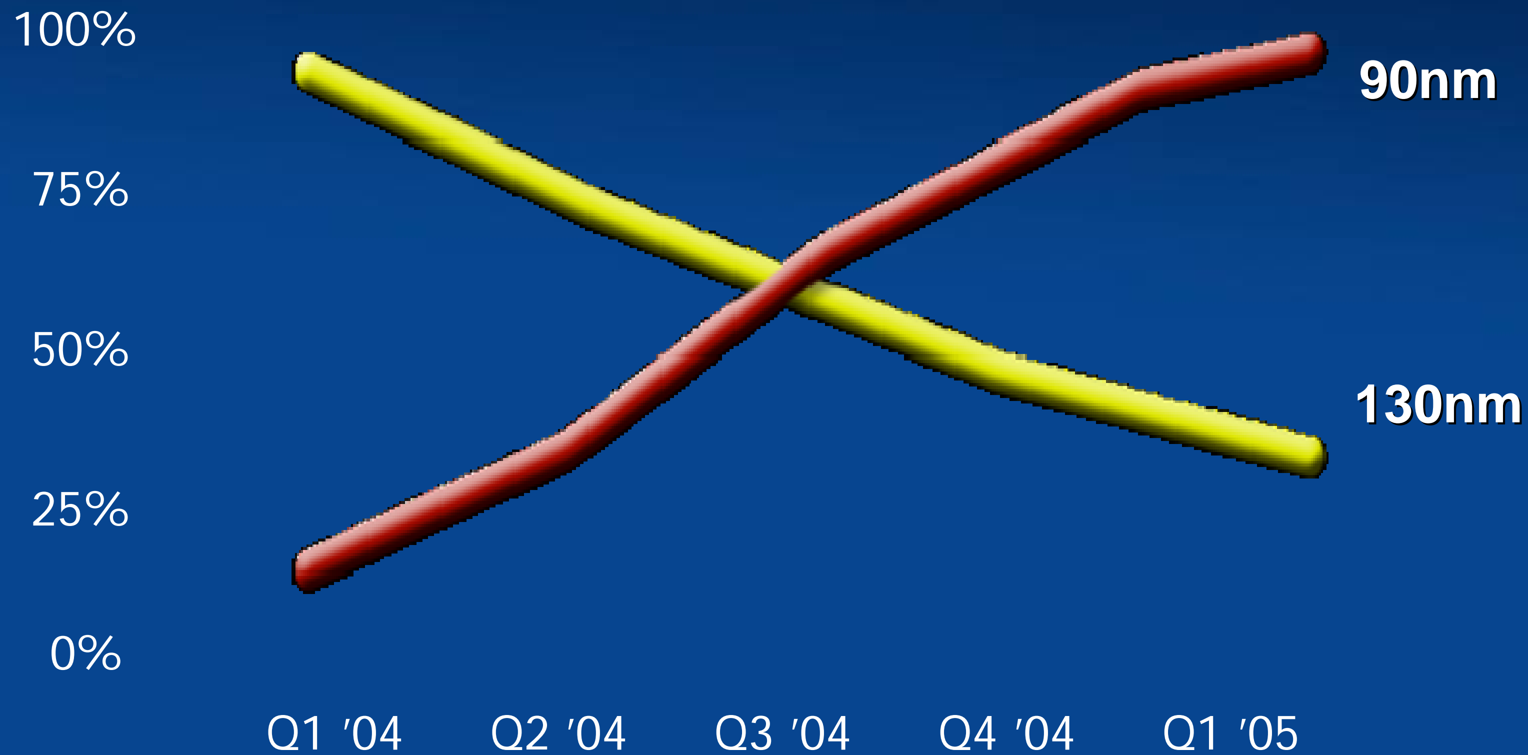
Gate Oxide Scaling

$$\frac{I_{DSat}}{W} \sim \frac{1}{2} \mu \frac{\varepsilon_o \varepsilon_s}{t_{ox}} \frac{1}{Lg} (V_{DD} - V_T)^2$$

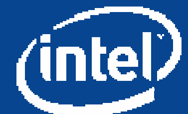




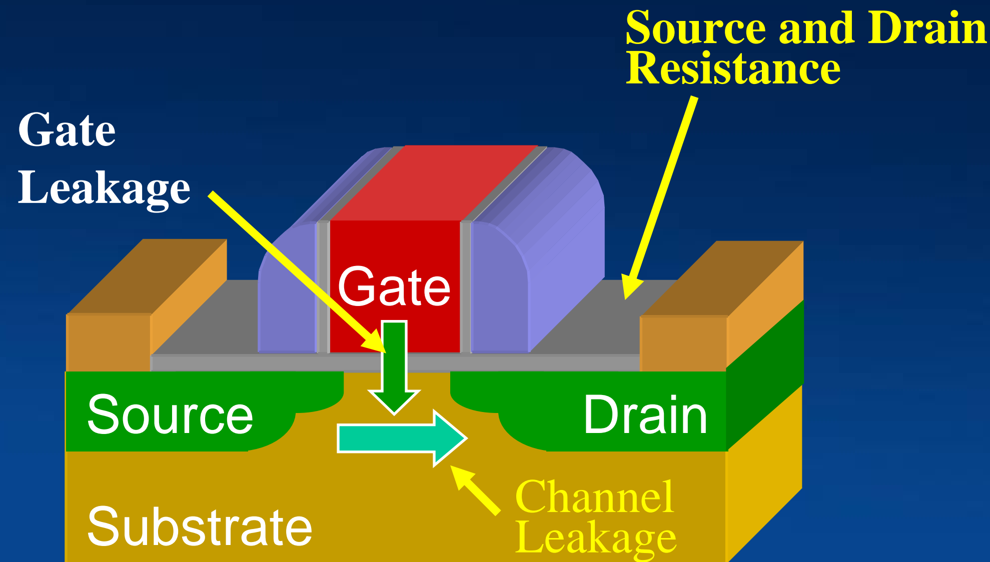
Intel Ramped Production Ahead of Industry on 90 nm Technology Generation



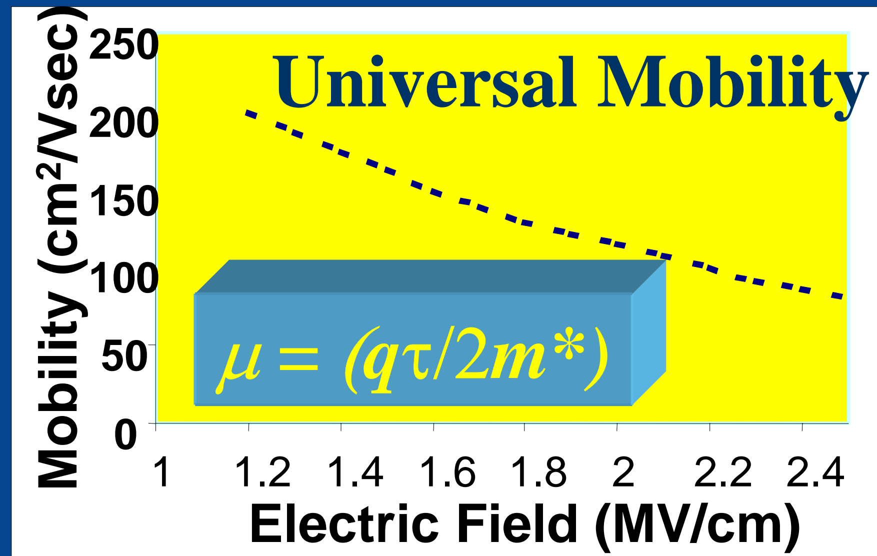
90 nm crossover occurred in Q3 '04



Geometrical Scaling Limitations



- S/D Leakage
- Gate Leakage
- S/D Resistance
- Decreased Mobility



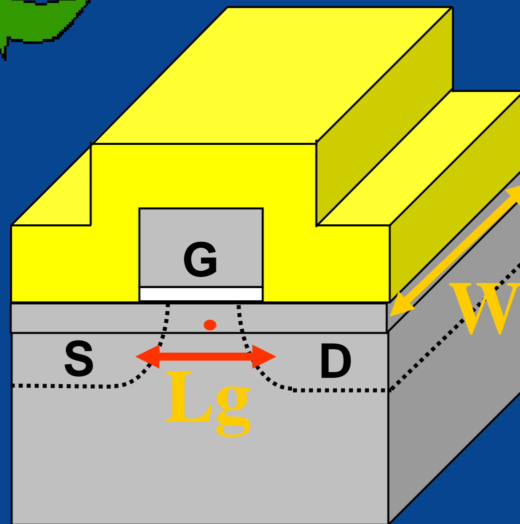
New Transistor Trade-off

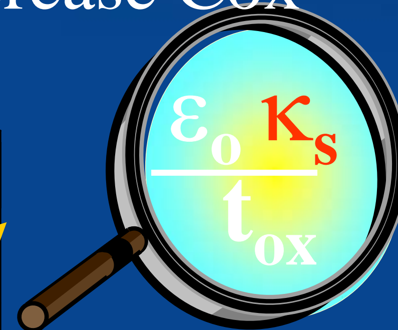
$$I_{DSat} \sim \frac{1}{2} \mu C_{ox} \left(\frac{W}{Lg}\right)(V_{DD} - V_T)^2$$

Increase μ

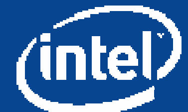
Increase Cox

Reduce **Lg**





New Material



Gate Oxide Scaling

Gate Oxide Thickness (nm)

Node	Gate oxide thickness
.35um	
.25um	
.18um	
.13um	
90nm	1.2 nm
65nm	

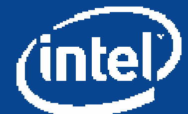
Y-axis: 1 to 10 (log scale). X-axis: 1990, 1995, 2000, 2005.

Gate

1.2nm SiO_2

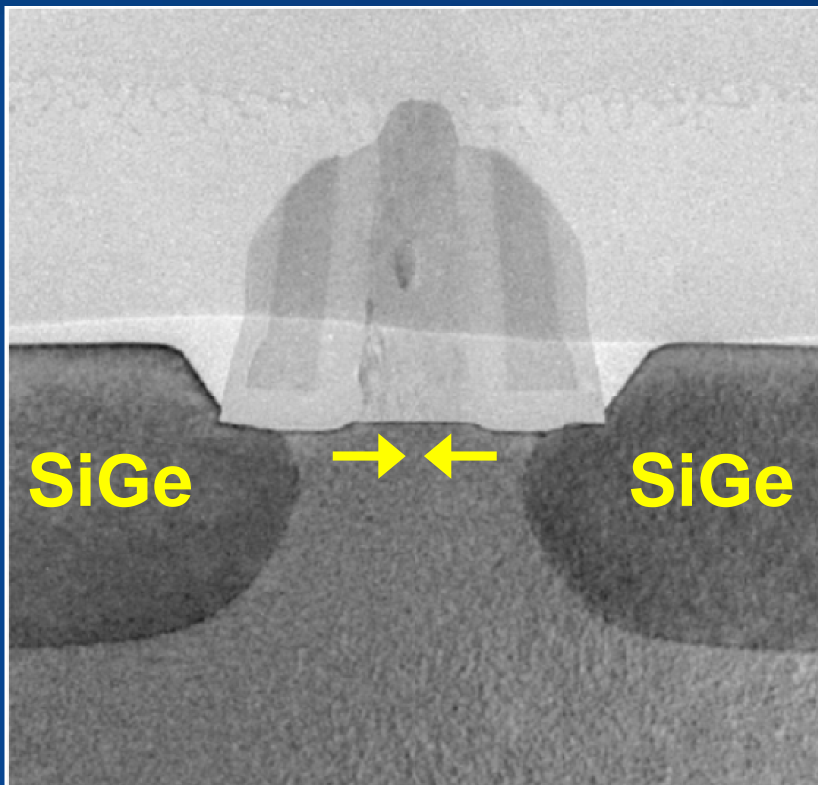
Silicon substrate

Gate oxide scaling is reaching its limits

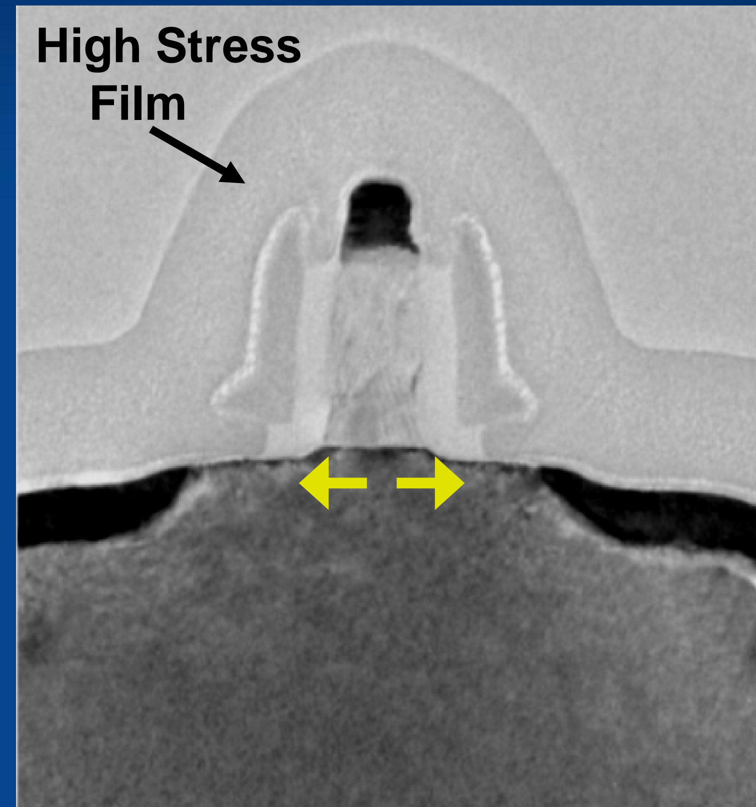


Mobility Innovation

Strained P-Channel Transistor



Strained N-Channel Transistor



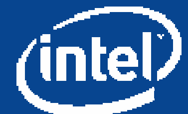
Source: Intel

Improved Transistor Performance

1000	
1.0 V	PMOS, NMOS

1000
1.0 V
PMOS
NMOS
100
I_{OFF}
(nA/um)
90 nm
2002
2004
65 nm
2004
10
1
0.2
0.4
0.6
0.8
1.0
1.2
I_{ON} (mA/um)

65 nm transistors increase drive current 10-15% with enhanced strain



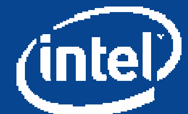
Improved Transistor Performance

1000
100
10
1
I_{OFF} (nA/um)
1.0 V
PMOS
NMOS
90 nm
2002
2004
65 nm
2004
0.2
0.4
0.6
0.8
1.0
1.2
I_{ON} (mA/um)

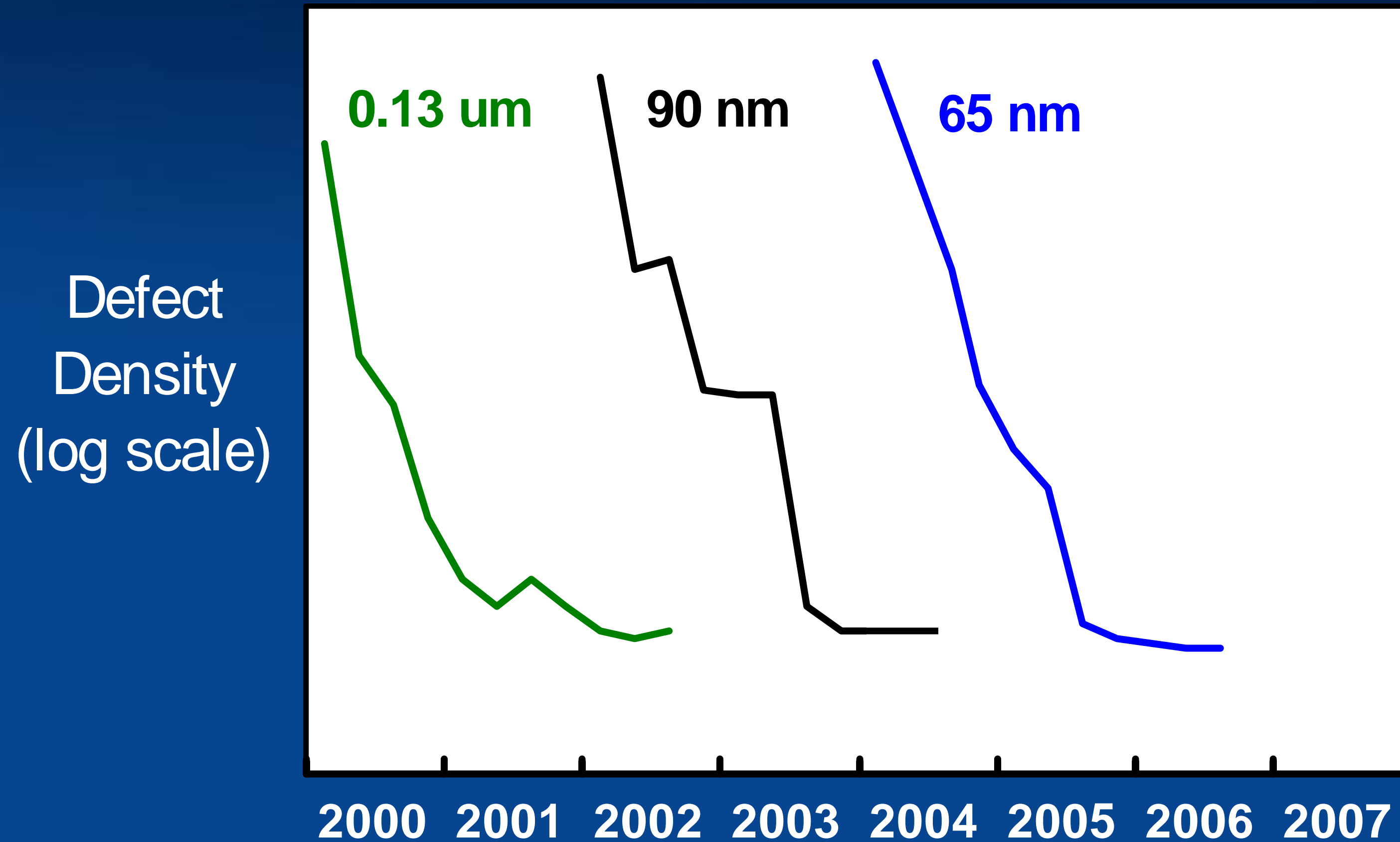
Power Saving Feature

65 nm transistors can alternatively provide ~4x leakage reduction

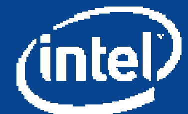
No other company has matched these performance-leakage capabilities



65 nm Yield Improvement Trend



65 nm is Intel's highest yielding process ever



Intel Only:
Process + Products + Production

100%
75%
50%
25%
0%

90 nm

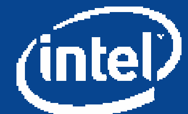
65 nm

FORECAST

Q1'06 Q2'06 Q3'06 Q4'06 Q1'07

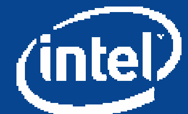
65 nm crossover occurred in Q3 '06

>120 million units shipped so far



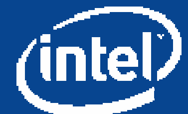
65 nm Summary

- Intel has been shipping 65 nm processors since October 2005, more than one year ahead of the competition
- Intel has shipped >120 million 65 nm
- Only Intel has three 65 nm / 300 mm fabs shipping in volume



Logic Technology Evolution

Process Name	P860	P1262	P1264	P1266	P1268
Lithography	130 nm	90 nm	65 nm	45 nm	32 nm
1st Production	2001	2003	2005	2007	2009
Wafer (mm)	200/300	300	300	300	300



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  - High-k+ Metal gate for 45nm technology
- DFM
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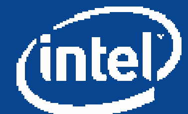
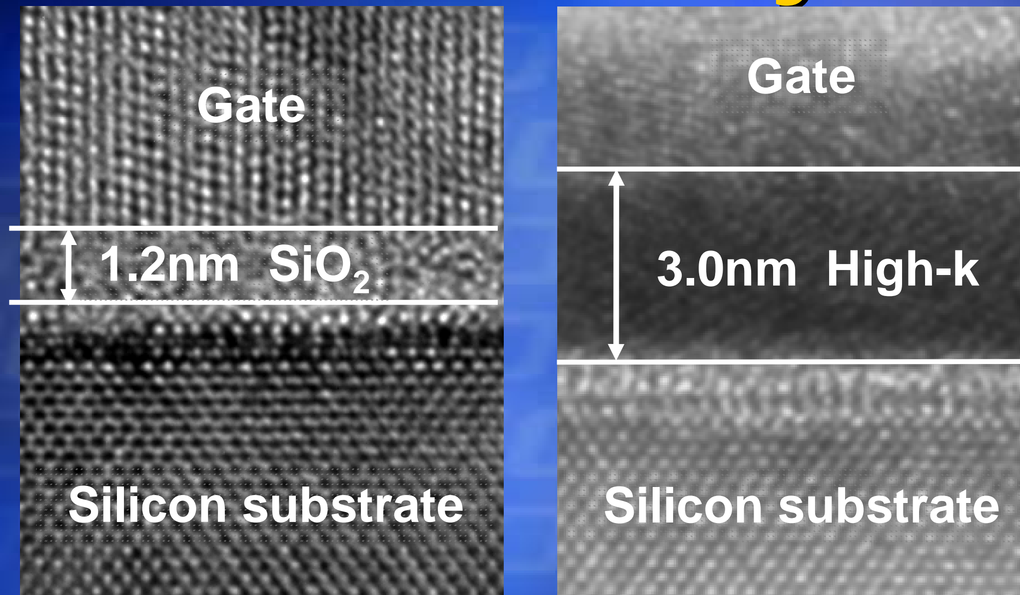


High-k Dielectric reduces leakage substantially



Benefits compared to current process technologies

	High-k vs. SiO_2	Benefit
Capacitance	60% greater	*Much faster transistors*
Gate dielectric leakage	> 100x reduction	*Far cooler*

November 4th, 2003

intel

intel

Continuation of Moore's Law

Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268	P1270
1st Production	1997	1999	2001	2003	2005	2007	2009	2011
Process Generation	0.25μm	0.18μm	0.13μm	90 nm	65 nm	45 nm	32 nm	22 nm
Wafer Size (mm)	200	200	200/300	300	300	300	300	300
Inter-connect	Al	Al	Cu	Cu	Cu	Cu	Cu	?
Channel	Si	Si	Si	Strained Si	Strained Si	Strained Si	Strained Si	Strained Si
Gate dielectric	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	High-k	High-k	High-k
Gate electrode	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Metal	Metal	Metal

Introduction targeted at this time

Subject to change

Intel found a solution for High-k and metal gate

November 4th, 2003

45 nm Technology Benefits

45 nm benefits compared to 65 nm

~2x	improvement in transistor density, for either smaller chip size or increased transistor count
~30%	reduction in transistor switching power
>20%	improvement in transistor switching speed or
>5x	reduction in source-drain leakage power
>10x	reduction in gate oxide leakage power

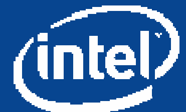
These performance and leakage improvements would not be possible without high-k + metal gate

45nm High-k Performance/Power Benefits

Transistor Performance vs. Leakage

65 nm
45 nm
1000
Leakage Current (nA/um)
100
20% Higher Drive
>5x Lower Leakage
10
0.5
1.0
1.5
Transistor Drive Current (rel.)

Source: Intel Internal



Gate Oxide Leakage

10
1
1000
100
10
1
0.1
0.01

Physical Tox (nm)

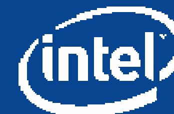
Gate Leakage (rel.)

SiO_2

.50um .35um .25um .18um .13um 90nm 65nm 45nm 32nm

Technology Generation

Gate oxide scaling stopped due to leakage



Gate Oxide Leakage

Physical Tox (nm): 10, 1

Gate Leakage (rel.): 1000, 100, 10, 1, 0.1, 0.01

SiO_2

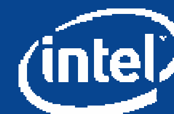
Hi-k

Hi-k

.50um .35um .25um .18um .13um 90nm 65nm 45nm 32nm

Technology Generation

High-k dielectric breaks through this barrier



High-k + Metal Gate Transistors

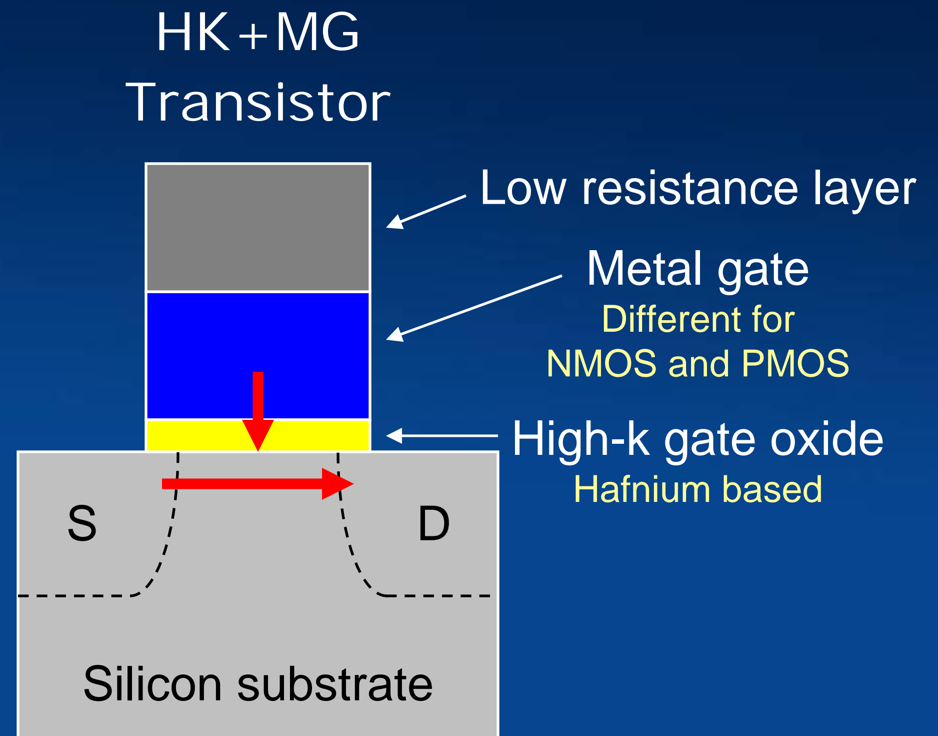
Metal Gate

Increases the gate field effect

High-k Dielectric

Increases the gate field effect

Allows use of thicker dielectric to reduce gate leakage

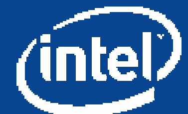


High-k + Metal Gate Combined

Transistor drive current increased >20%

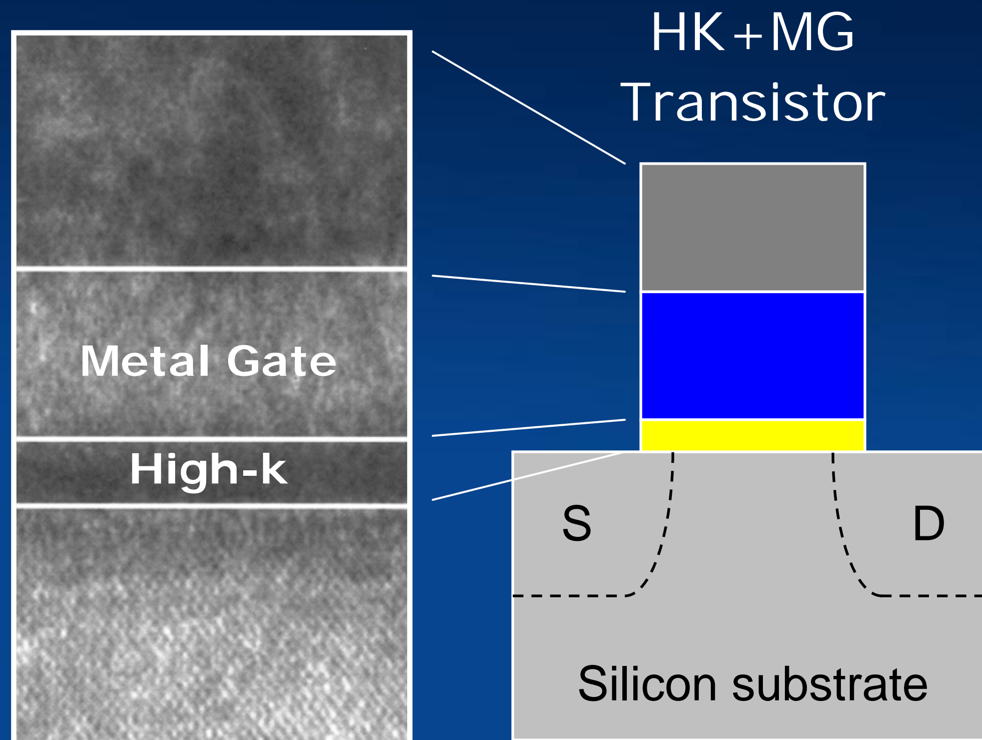
Or source-drain leakage reduced >5x

Gate oxide leakage reduced >10x



High-k + Metal Gate Transistors

- ✓ Integrated 45 nm CMOS process
- ✓ High performance
- ✓ Low leakage
- ✓ Meets reliability requirements
- ✓ Manufacturable in high volume



"The implementation of high-k and metal gate materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s"

— Gordon Moore

Density Scaling on Track

SRAM Cell Size

Year	Generation
1994	0.35 um
1996	0.25 um
1998	0.18 um
2000	0.13 um
2002	90 nm
2004	65 nm
2006	45 nm

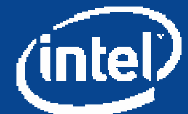
Cell Area (μm^2): 100, 10, 1, 0.1

Years: 1992, 1994, 1996, 1998, 2000, 2002, 2004, 2006, 2008

0.5x every 2 years

$0.346\ \mu m^2$ Cell
193 nm Dry Lithography

Cost-effective 193 nm dry lithography extended to 45 nm generation



45 nm SRAM Chip

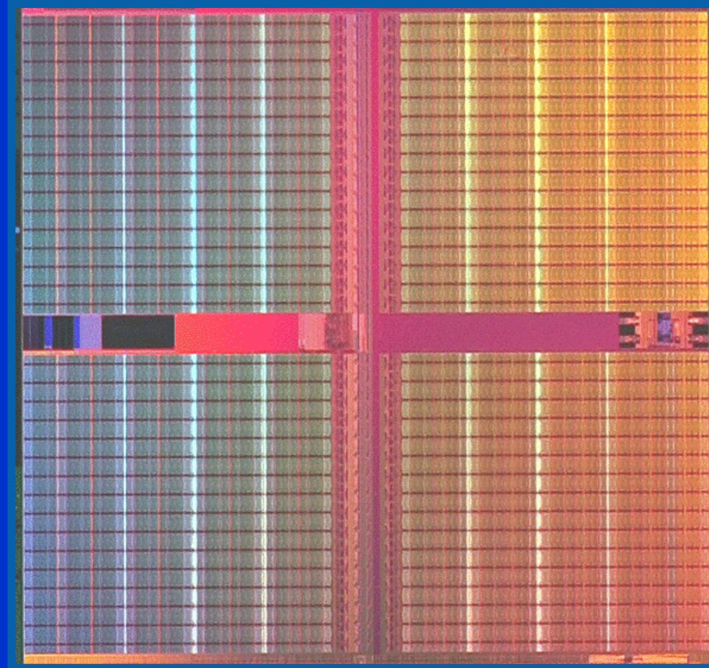
$0.346\ \mu m^2$ cell

153 Mbit density

119 mm^2 chip size

>1 billion transistors

Functional silicon in Jan '06



45 nm SRAM test vehicle includes all transistor and interconnect features to be used on 45 nm microprocessor

January, 2006

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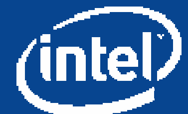


CPU Shipments (65nm vs. 45nm)

100%
90
80
70
60
50
40
30
20
10
0

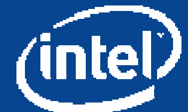
65 nm

45 nm

2H'07 Q1'08 Q2'08 Q3'08 Q4'08

Forecast →

Source: Intel Internal



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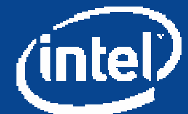
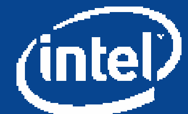


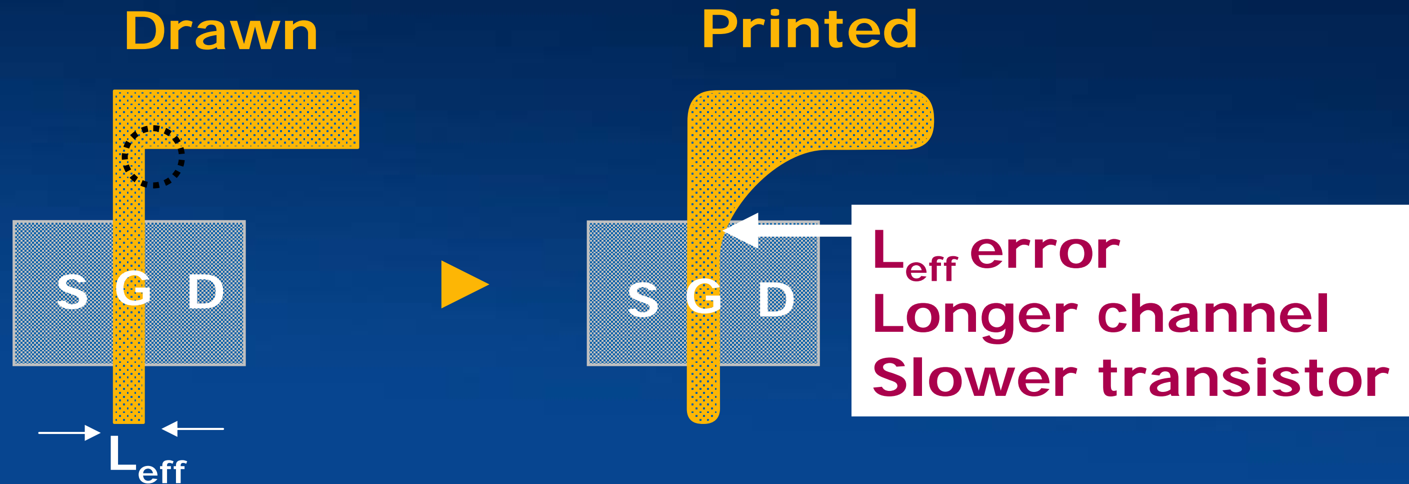
Design for manufacturing (DFM)

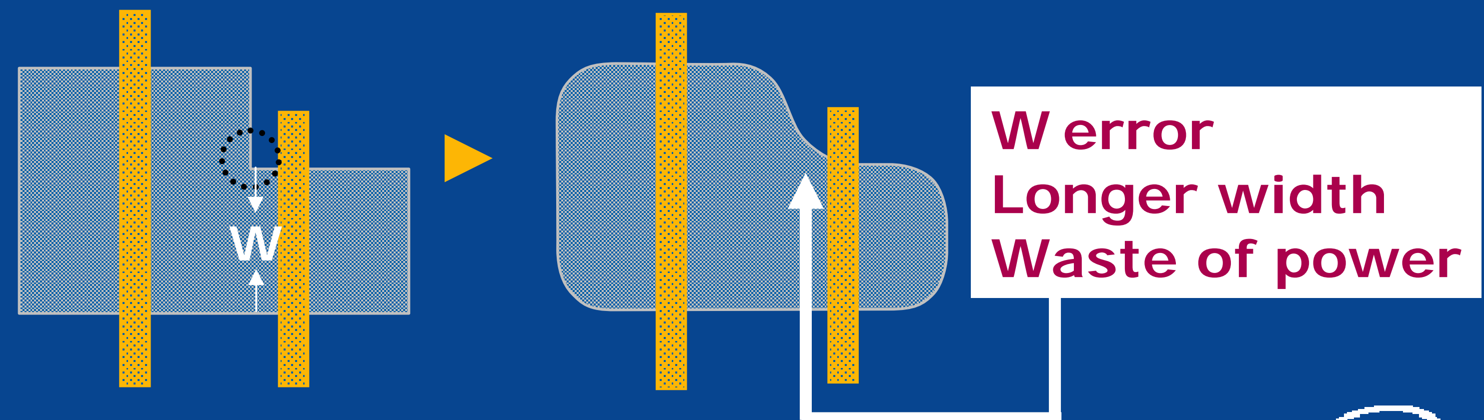
- Moore's Law depends on scaling physical dimensions
- Small variations in dimensions and doping can cause significant variation in function, power and performance
- "DFM" is a set of Design-Process methodologies that reduces and mitigates "variability"

DFM is the solution to the variability challenge



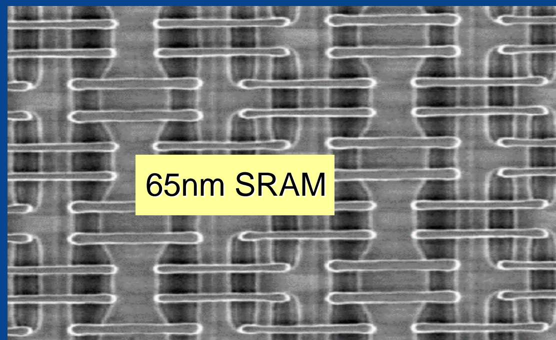
Rounding in transistor layouts

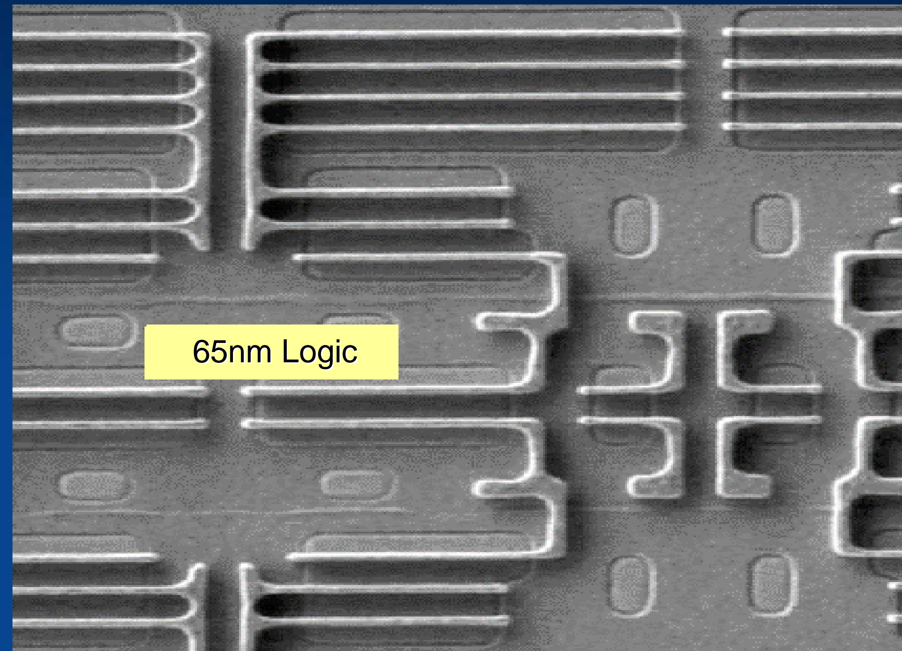




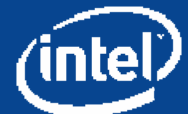
intel

Litho DFM solution: Advanced APSM masks w/ Litho DFM



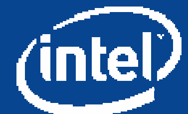


Intel was first to ramp Alternating Phase Shift Masks (APSM) with litho DFM for 65nm gate patterning and L_{eff} control



Lithography

Enhancements have extended 193 nm dry lithography to the 45 nm generation



Lithography

1
0.1
0.01
micron

1000
10

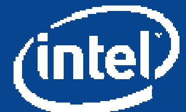
1980
1990
2000
2010
2020

Lithography Wavelength
248 nm
193 nm

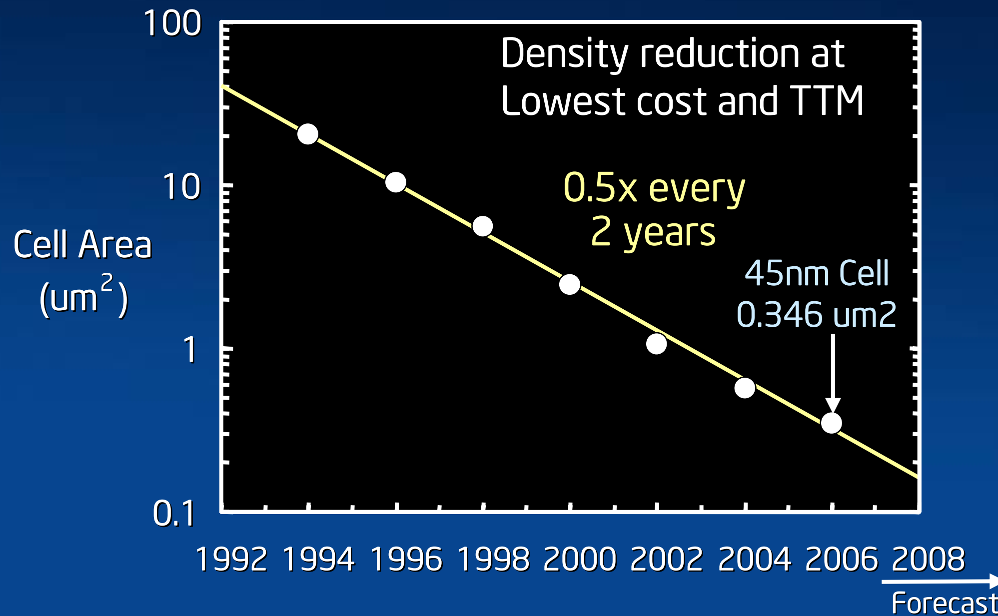
Feature Size
65 nm
45 nm
32 nm

Optical proximity correction
Higher numerical aperture
Phase shift masks
Immersion lithography

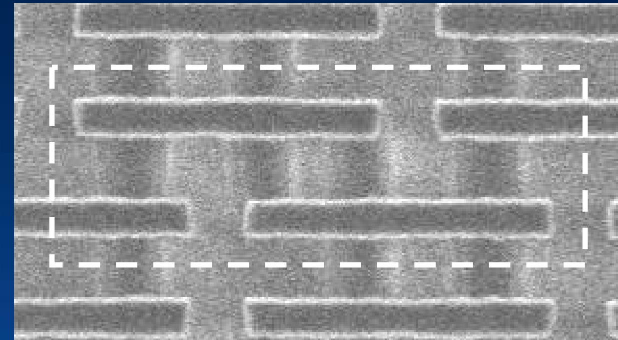
Immersion lithography will extend 193 nm at least to the 32 nm generation



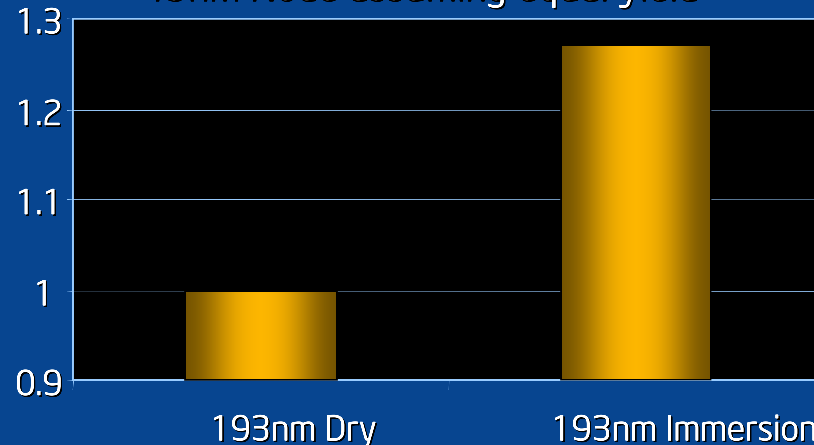
Committed to Provide the Best Total Cost at 45nm

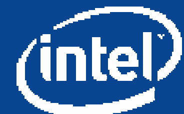


SRAM - Functional silicon in Jan '06

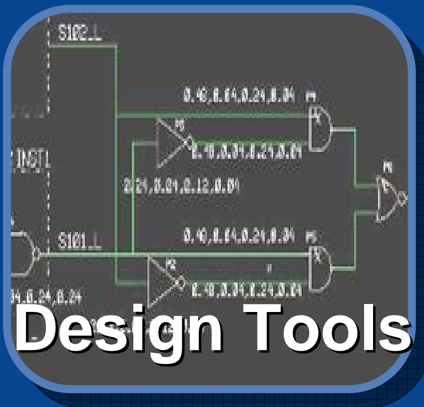


Exceptional Gate control through PSM and Double Patterning

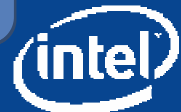




Intel DFM advantage: Collaboration of diverse disciplines



Diverse disciplines collaborate under one roof to co-optimize DFM solutions

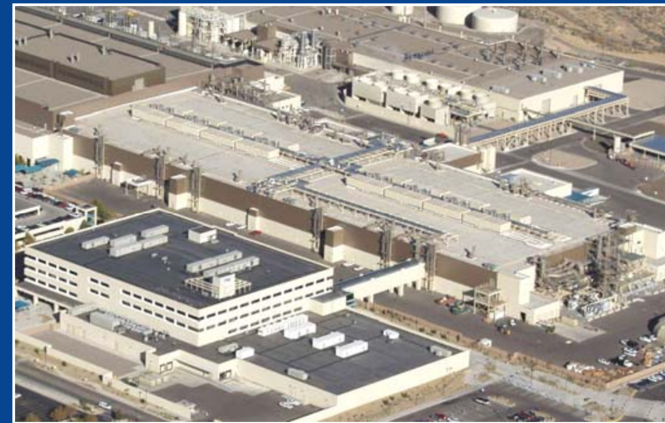


45 nm Manufacturing Fabs

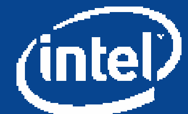
D1D Oregon - 2H '07

Fab 32 Arizona - 2H '07

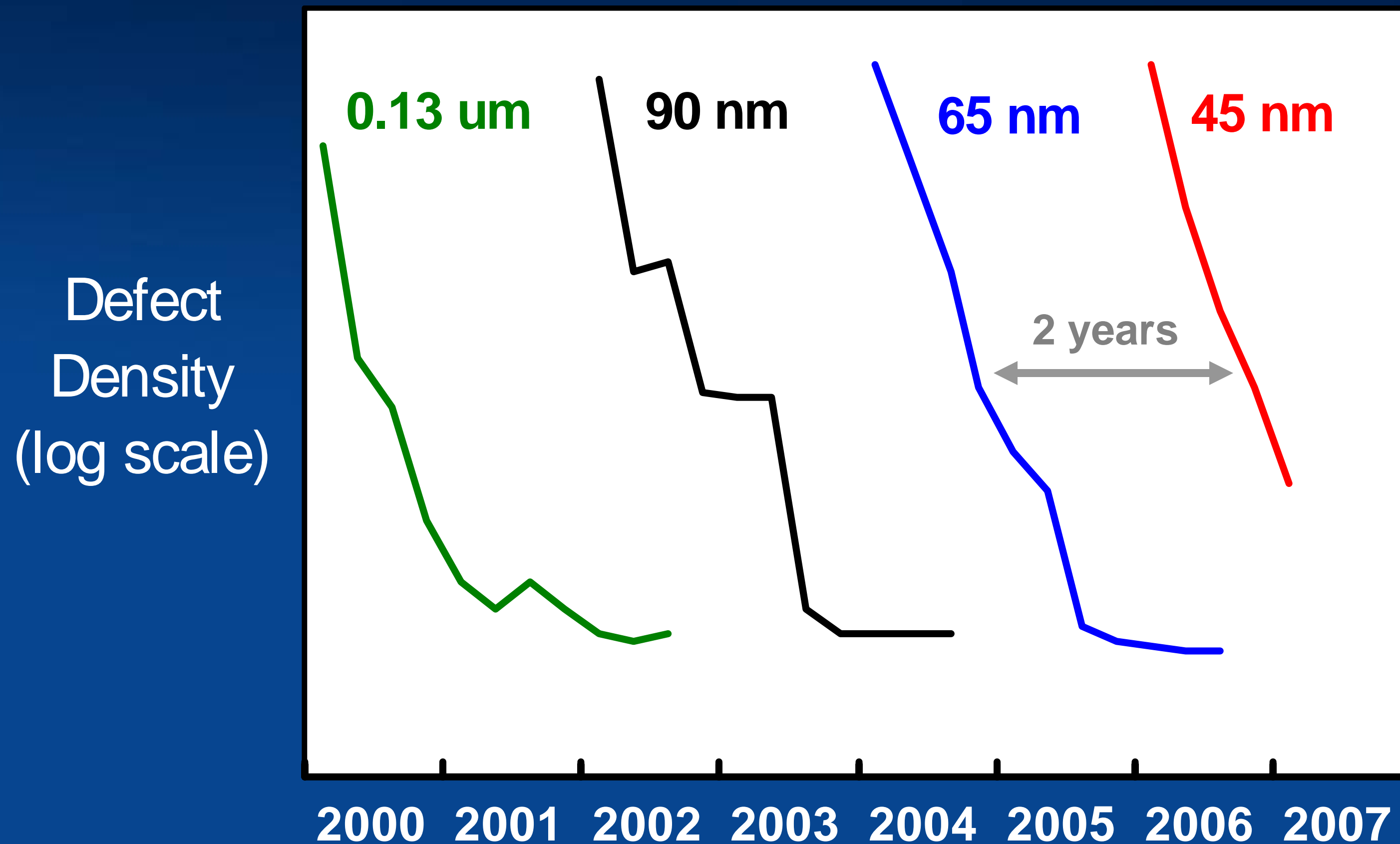
Fab 28 Israel - 1H '08



Fab 11X New Mexico - 2H '08

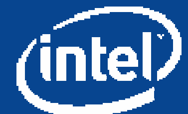


45 nm Yield Improvement Trend

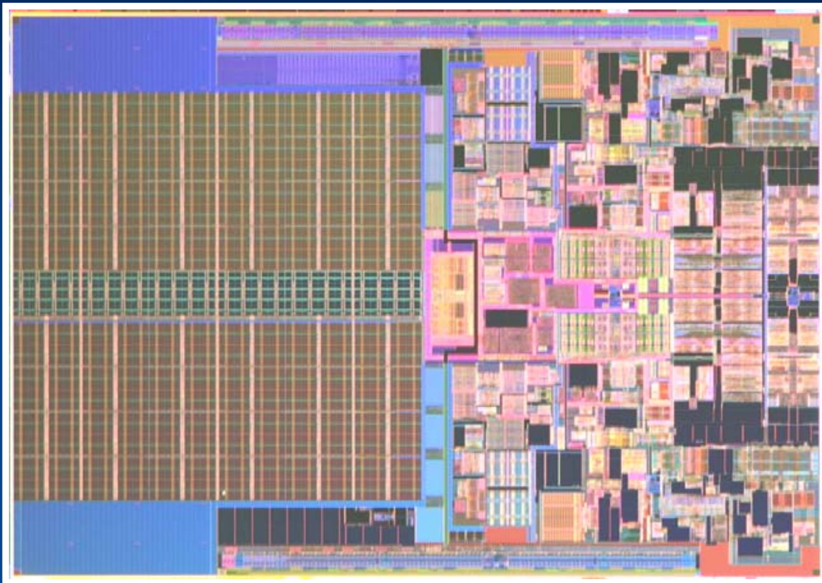


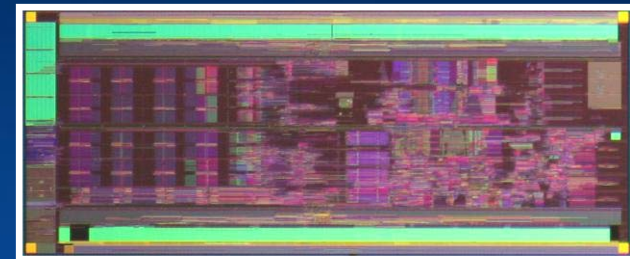
45 nm defect reduction trend at expected 2 year offset

45 nm on track for production in 2H '07



World's First Working 45 nm CPUs





Penryn

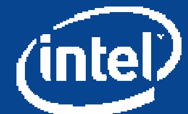
45 nm Hi-k Intel® Core™2 and Intel Xeon™ processors

Mobile, Desktop, Workstation, and Server Optimized

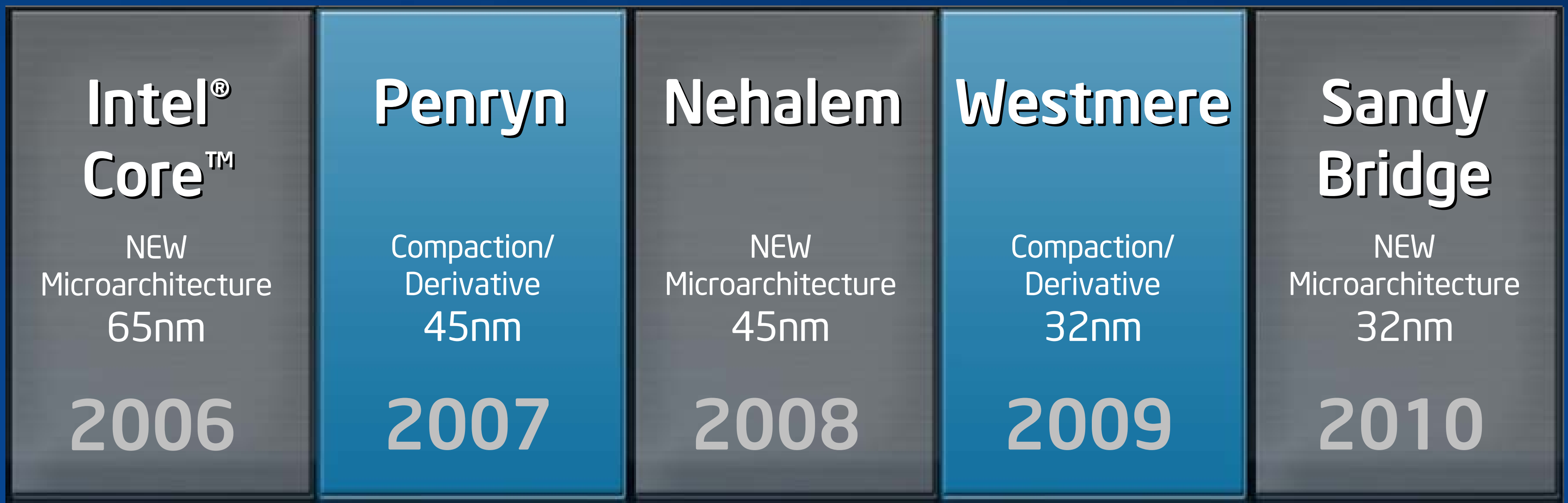
Silverthorne

45 nm Hi-k new low power microarchitecture

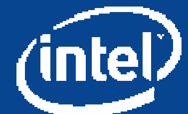
Mobile Internet Devices and Ultra-Mobile PCs



Tick/Tock: Our Model for Sustained Microprocessor Leadership



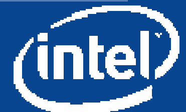
Forecast



Driving Down Power and Size

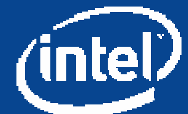
CPU + CHIPSET

Source: Intel Internal



Outline

- Intel's Silicon R&D Pipeline
- From Geometrical Scaling to Equivalent Scaling
- DFM
- Getting the Lead out
- Future Technology Options
- Summary



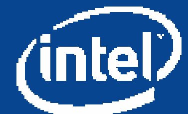
Summary

– Intel has removed 100 percent of the lead (Pb) across its entire portfolio of packages in its 45nm family of microprocessors
  – … 65nm chipsets will transition to 100% lead-free in 2008

– Intel's 45nm Hi-k metal gate process technology represents a dramatic transition to new materials that enable energy efficient performance microprocessors

– Intel's family of 45nm microprocessors will begin production in second half of 2007

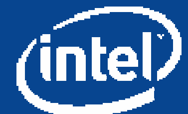
– Intel's effort to eliminate lead in our products is part of broader strategy to support an environmentally sustainable future



Reduced Environmental Footprint

- **Recent Successes**
  - Launched Intel® Core™2 Duo processors: for desktops up to 40% faster and 40% more energy efficient
  - Transitioned Intel® StrataFlash® Cellular Memory packages to halogen-free technology.
  - Saved over 9 billion gallons of fresh water through our water reuse and recycling practices
  - Recycled more than 70% of our chemical and solid wastes
  - Reduced our global warming gas emissions the equivalent of removing 50,000 cars from the road
  - Named Technology Super Sector Leader by Dow Jones Sustainability Index for the 6th year running

Intel 2006 Corporate Social Responsibility report recently posted online http://www.intel.com/intel/cr/gcr06/overview.htm



Eliminating the Lead (Pb) in Intel Components

Flip-Chip Pin Grid Array (FC-PGA)

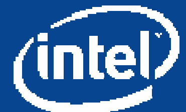
Flip-Chip Bump
Lead
^RoHS Exempt
Capacitors
Lead
Pin Grid
Lead
socket

Flip-Chip Ball Grid Array (FC-BGA)

Flip-Chip Bump
Lead
^RoHS Exempt
Capacitors
Lead

Printed Circuit Board
Solder Balls
Lead

*95% of the Lead Content Removed from Flip-chip Packages in 2004



*Percentage based on weight

Lead-Free Solder Properties Affect Low-K Inter Layer Dielectric

At reflow temperature

Silicon Die
CTE* 2.8 ppm/ºC

Flip Chip Bump

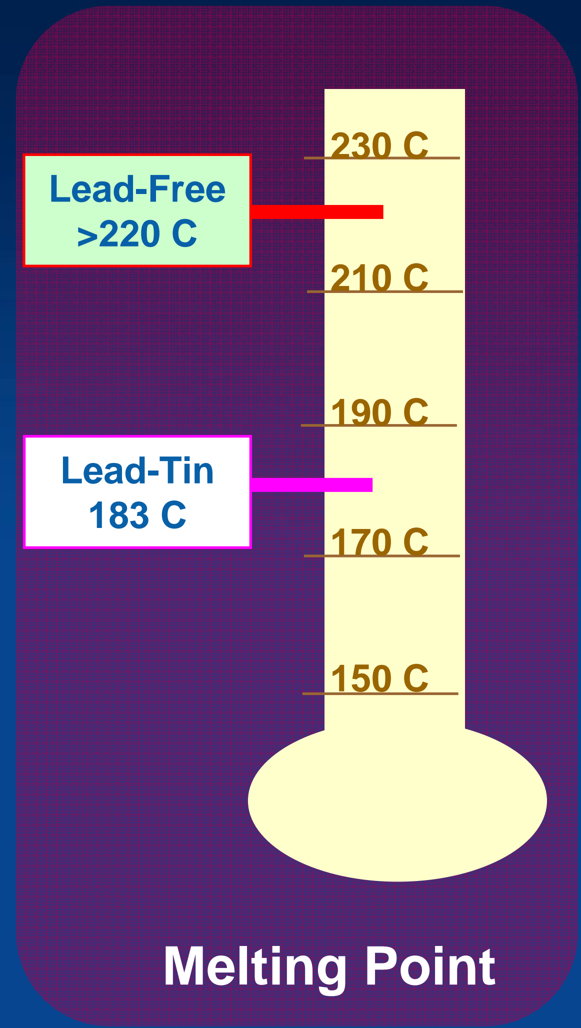
Package
CTE* 17 ppm/ºC
(Copper Laminate)

Cooling

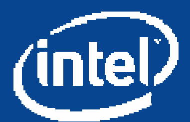
Heating

At room temperature

The Package shrinks more than the chip

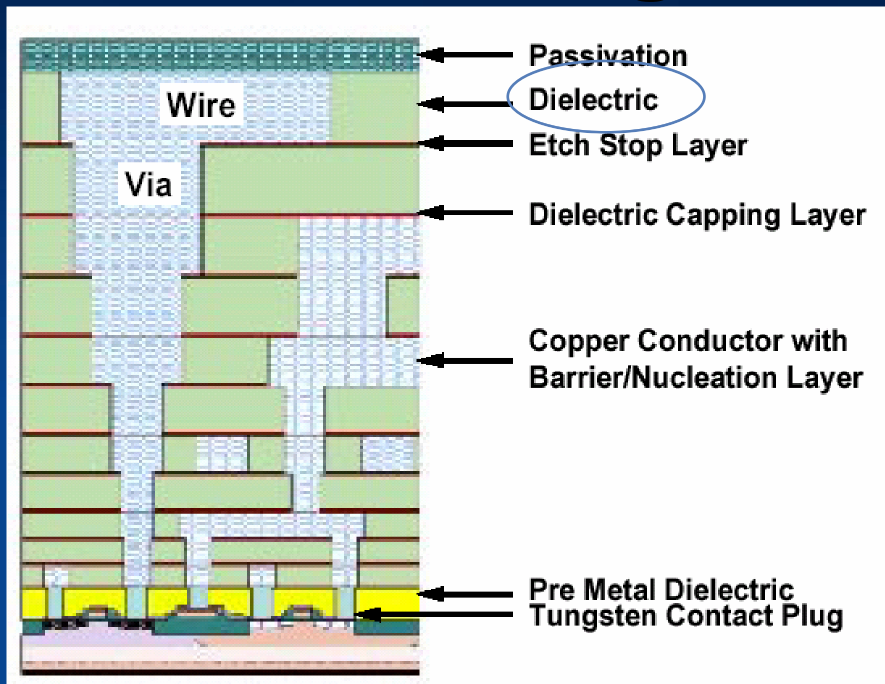


Lead-free solder increases stress



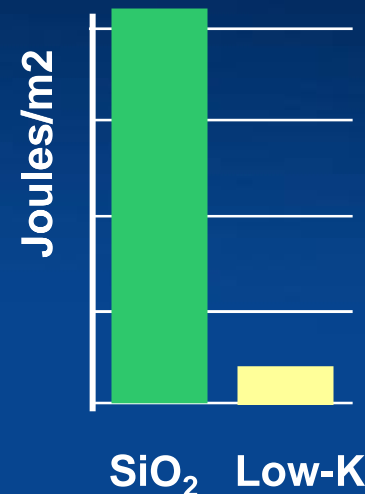
* CTE = Coefficient of Thermal Expansion *PPM= Parts Per Million

Low-K Silicon & Lead-free Package Integration Challenge



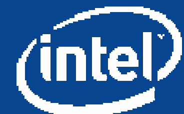
example silicon cross-section

ILD Strength



SiO_2 Low-K

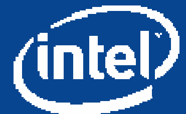
- **Successful Integration of Silicon & Lead-Free Flip Chip Package Technologies requires a significant reduction in**
  - **Inter Layer Dielectric (ILD) Stress**



SiO_2= Silicon Dioxide K = “dielectric constant” which measures the relative permittivity of a material.

Lead-free Flip-Chip Package Technology Challenges

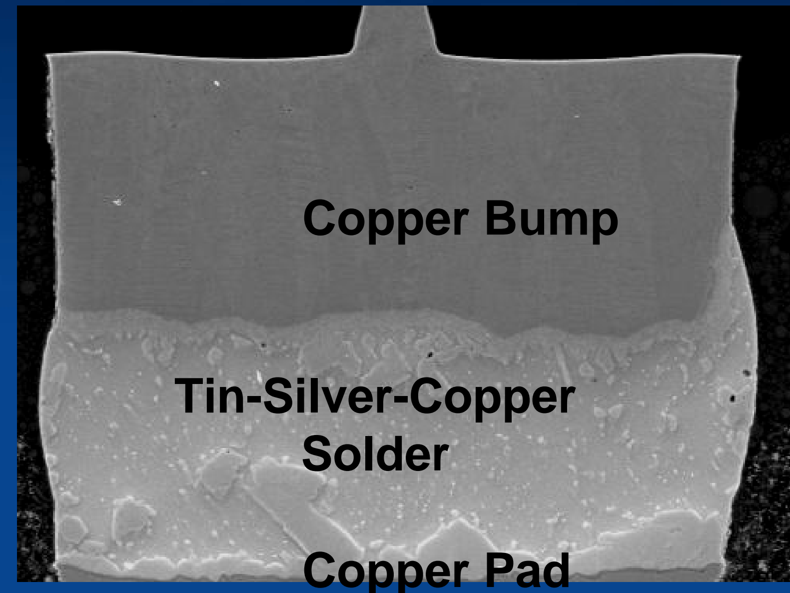
Many Challenges had to be overcome to remove the remaining 5% of Lead (Pb)



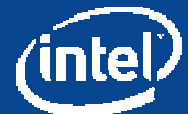
Introducing Intel's 45nm 100% Lead-Free Technology

Traditional High-Lead Bumps

Lead-free Advanced Bump Metallurgy



Solders containing lead have been replaced with a copper column and lead-free solder



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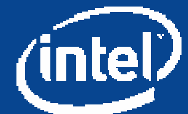
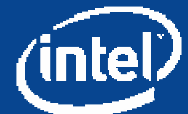


For further information on Intel's lead free technology, please visit

www.intel.com/technology/silicon



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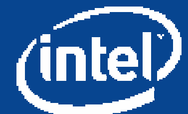
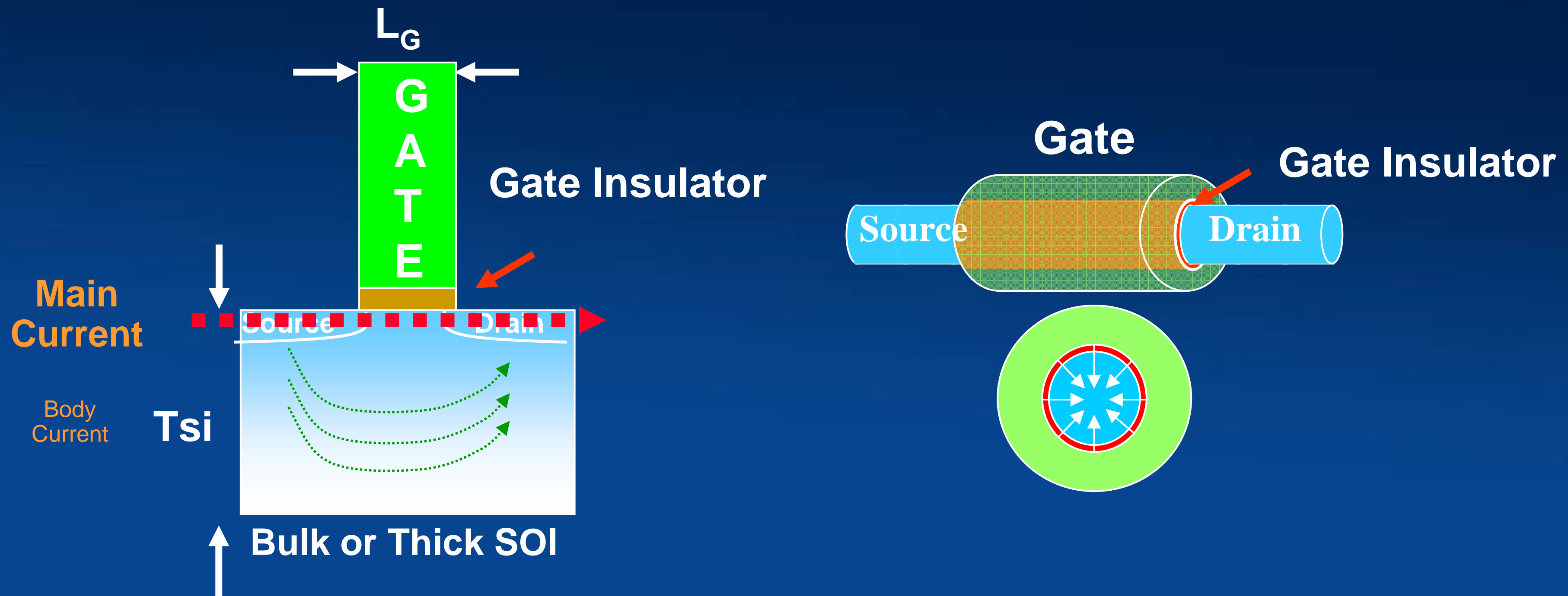


Improving on a Planar Transistor



- In planar devices on-current is mostly carried in a thin top layer
- Body current is a source of leakage when the device is off
- An ideal transistor would have a gate surround a very thin channel
- This gives the highest on to off ratio & therefore <u>highest power efficiency</u>

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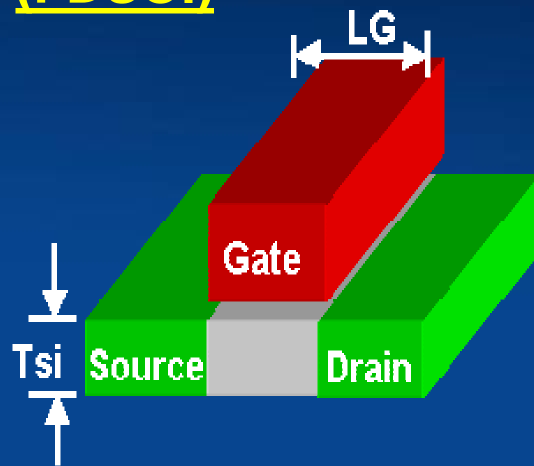
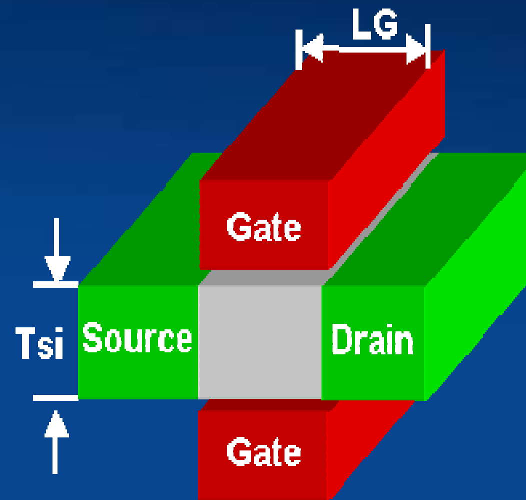
Fully Depleted Transistor Structures

Planar Single Gate (FDSOI)



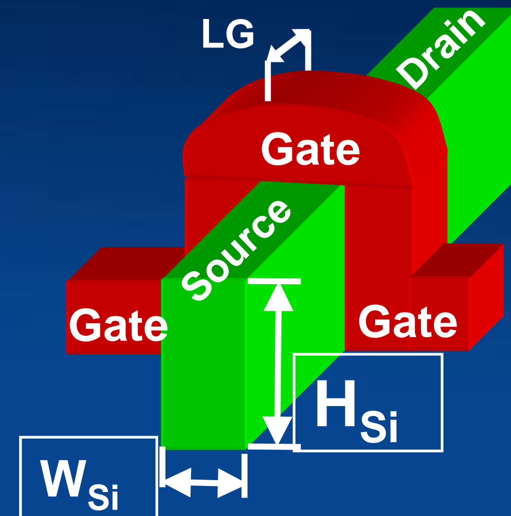
1. Ultra thin Tsi
2. Limited to SOI

Planar Double-Gate



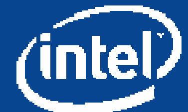
1. Wider Tsi than planar
2. Non Self-aligned

Non Planar Tri-Gate

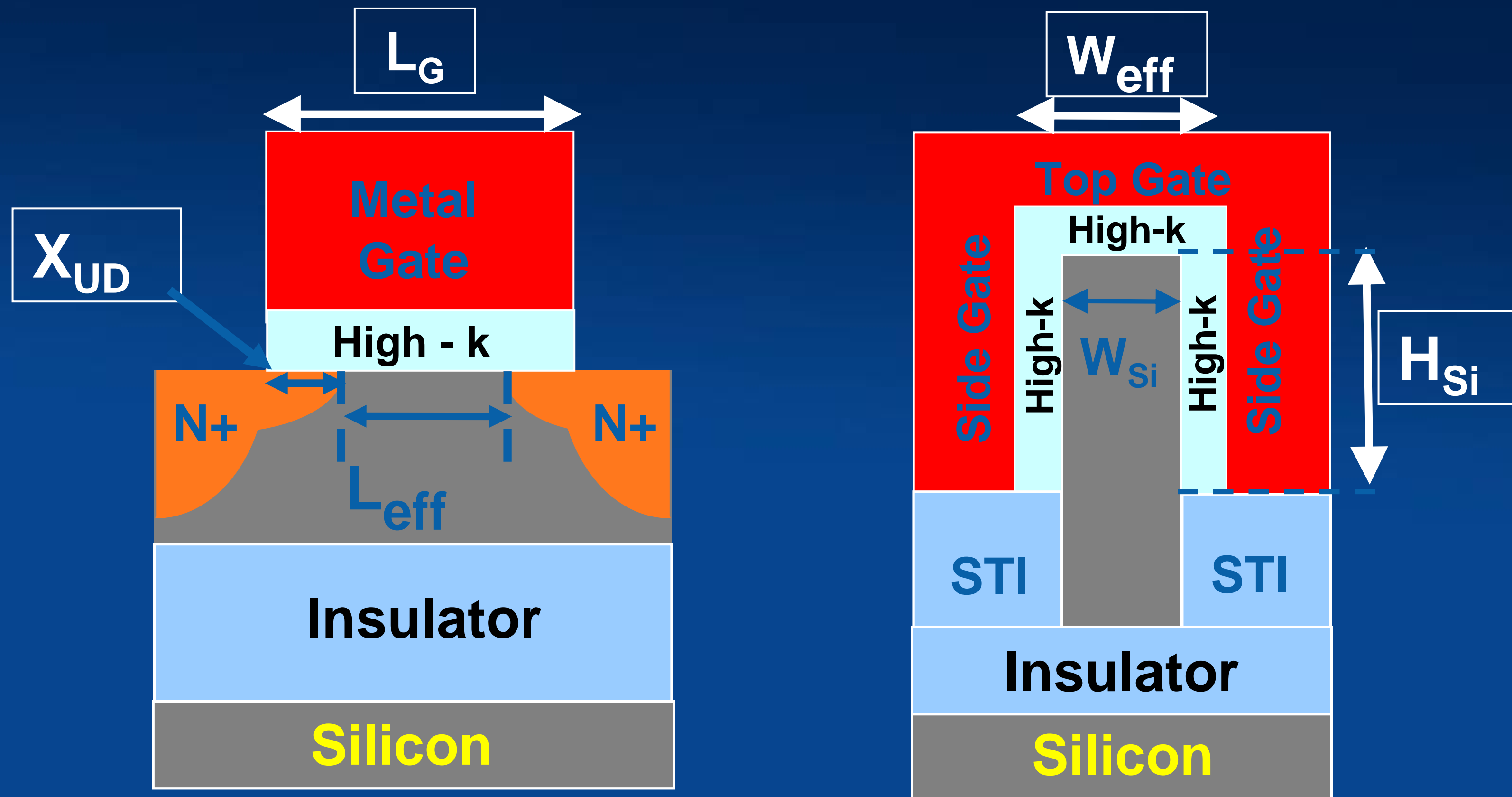


1. FIN W_{Si} is wider than planar T_{Si}
2. Self-Aligned gates
3. Bulk-Si or SOI

- Fully depleted thin-body devices improve SCE performance.
- Tri-Gate is the most favorable architecture for L_G scaling.



Tri-Gate Critical Dimensions



- I_{DSAT} is normalized by $Z_T = W_{Si} + 2*H_{Si}$
- Tri-gate electrostatics strongly depend on the ratio of L_{eff} / W_{eff} as defined by: $L_{eff} = L_G - 2 * X_{UD}$

$$W_{eff} = W_{Si} + 2(\varepsilon_{Si}/ \varepsilon_{OX})*T_{OX}$$

intel

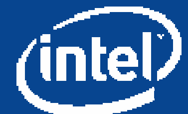
Tri-Gate Transistor:
"A template for the future"

GATE
DRAIN
SOURCE
CHANNEL- Si, nanotubes, nanowires …

GATE
DRAIN
SOURCE

Source: Intel

Technical details presented at:
ISSDM Conference, Japan, Sept 17, 2002
By Robert Chau



Tri-Gate FIN Critical Dimensions

HfO_2 High-k Dielectric

Near Mid-Gap Metal Gate

CVD Poly

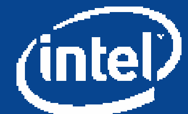
W_{Si}

H_{Si}

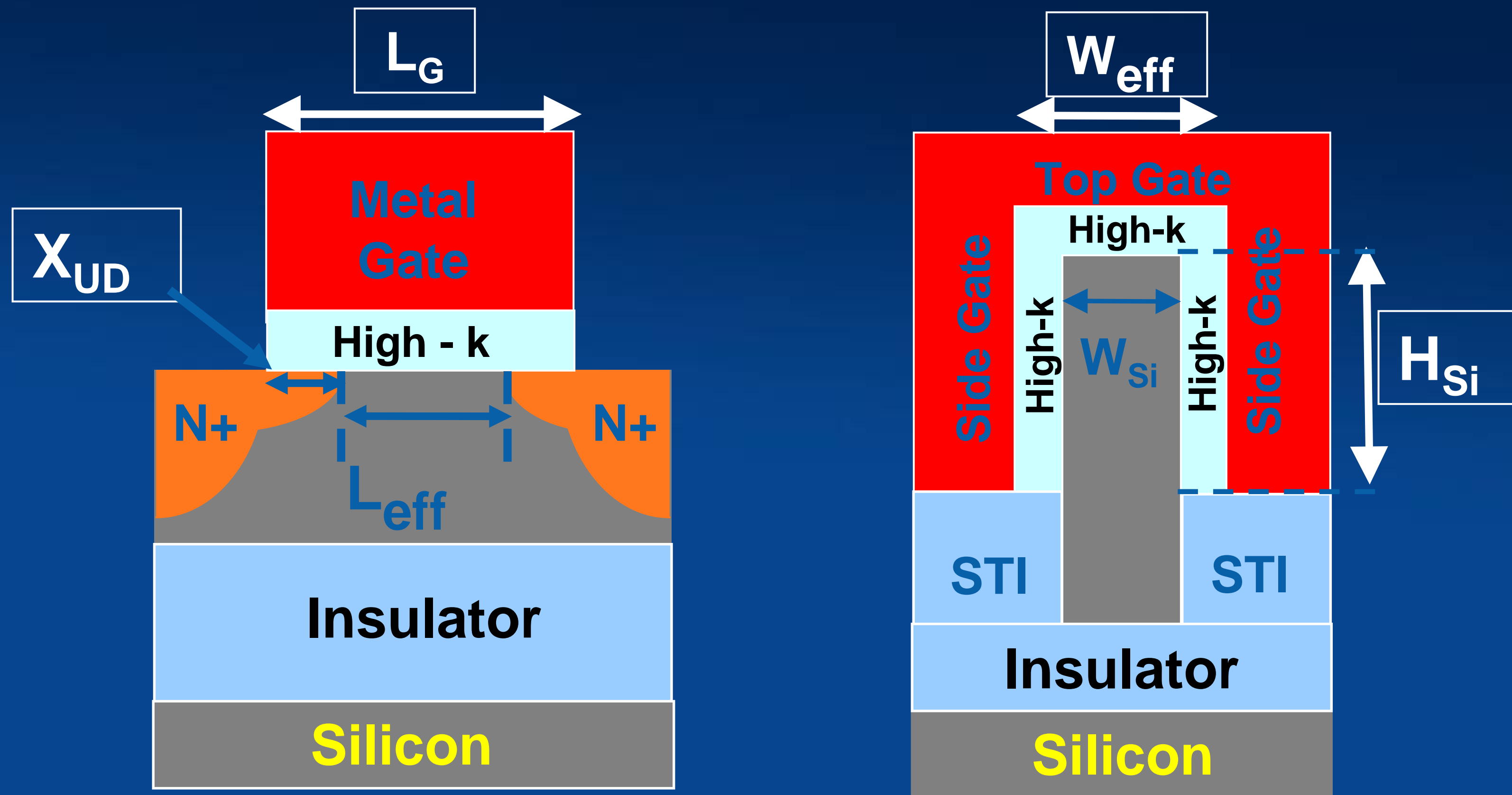
Si FIN

Z_{Total}

VLSI Symposium, 6-2006



Tri-Gate On…….



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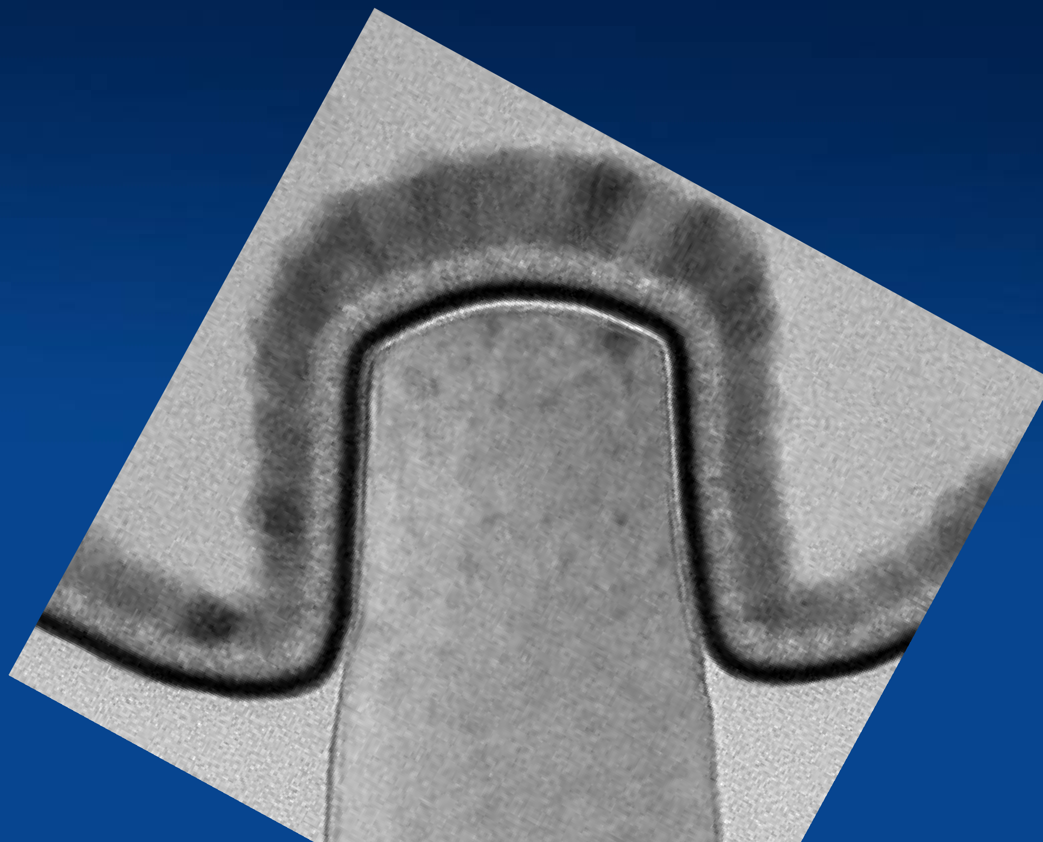
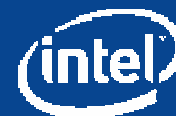
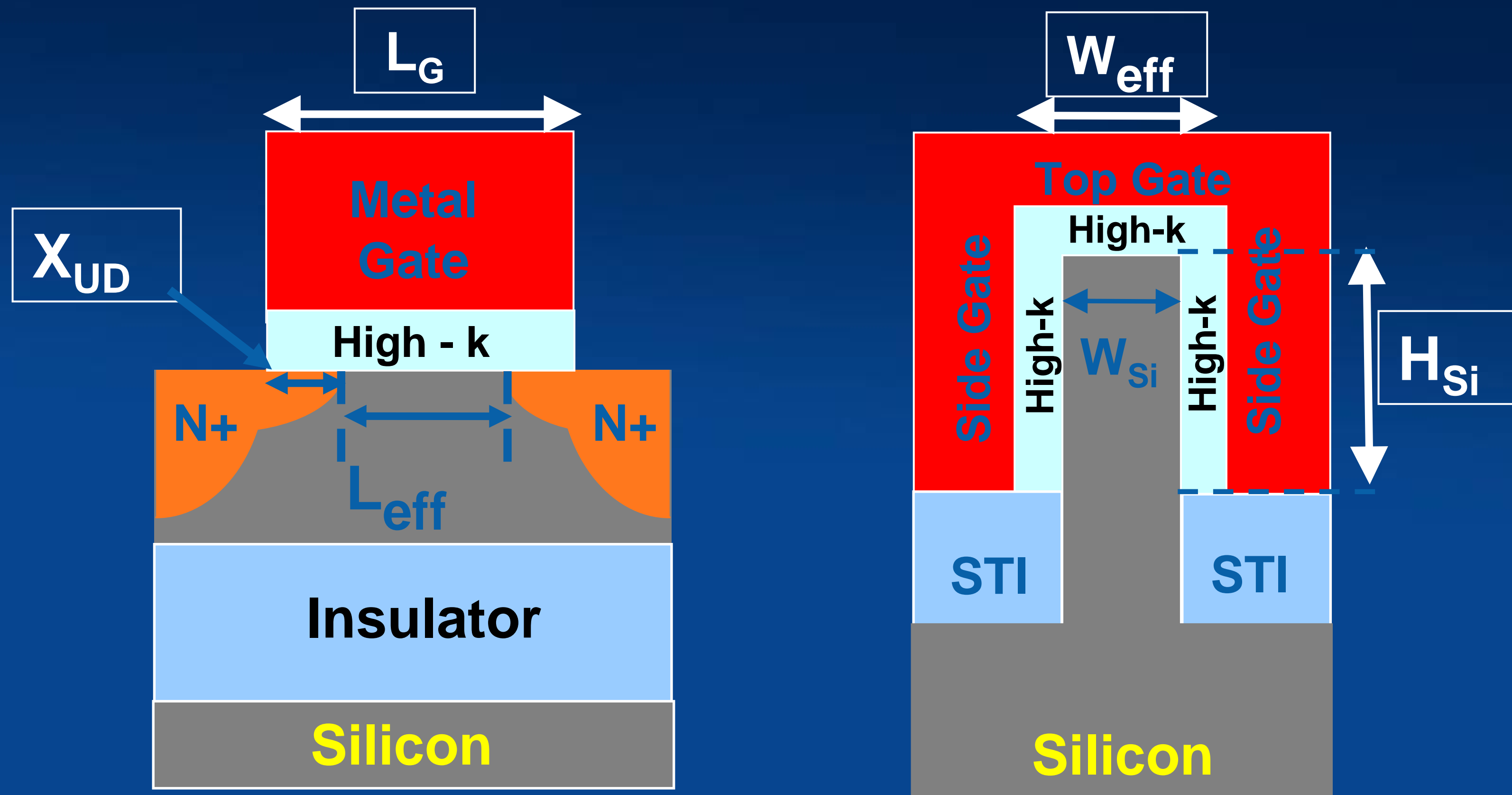
Tri-Gate On Bulk!



Silicon



Tri-Gate On…….



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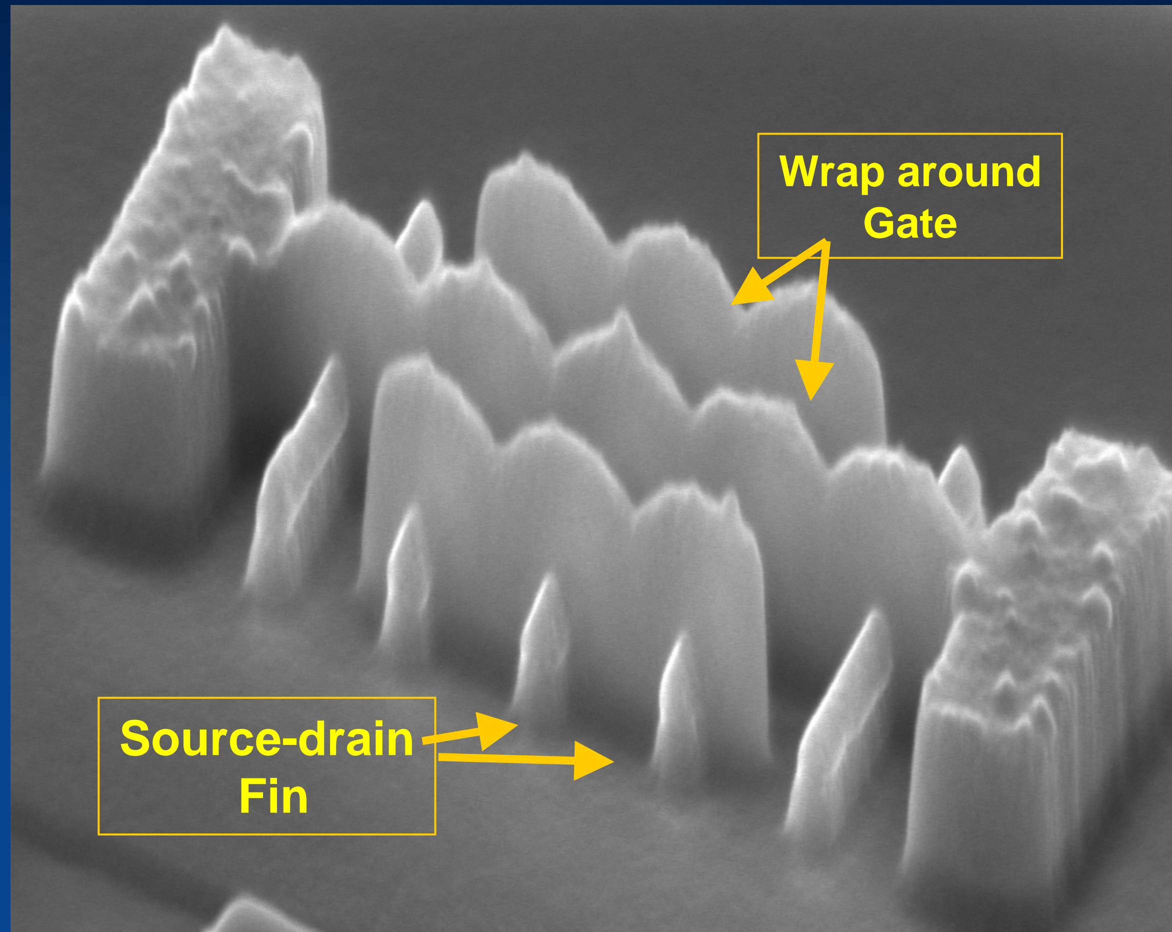
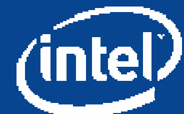
The Key is Optimizing the Integration



1. Tri-gate gives better off current and therefore less wasted power
2. High k – metal gate gives both higher speed and less wasted power
3. Strained Si produces higher speed and less wasted power

The sum of all these pieces is once again world leading transistors



Compound Semiconductors

Column III

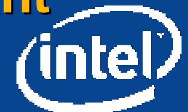
Column V

The periodic table of the elements

	1A	2A	3A	4A	5A	6A	7A	8			1B	2B	3B	4B	5B	6B	7B	0
1	H																	He
2	Li	Be											B	C	N	O	F	Ne
3	Na	Mg											Al	Si	P	S	Cl	Ar
4	K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
5	Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
6	Cs	Ba	L	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
7	Fr	Ra	A															
		L	La	Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu	
		A	Ac	Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr	

Si = Silicon
Al = Aluminum
Ga= Gallium
In = Indium
P = Phosphorous
As = Arsenic
Sb = Antimony

- Silicon in transistor channel is replaced by "III-V compound semiconductor"
- Result is much higher electron mobility, meaning significant performance and power improvements



Increasing Electron Mobility

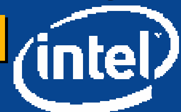
Increased mobility in the transistor channel leads to higher performance and less energy consumption

$$I_{DSAT} \propto \frac{W}{L} \cdot \mu \cdot C_{OX}$$

Relative mobility

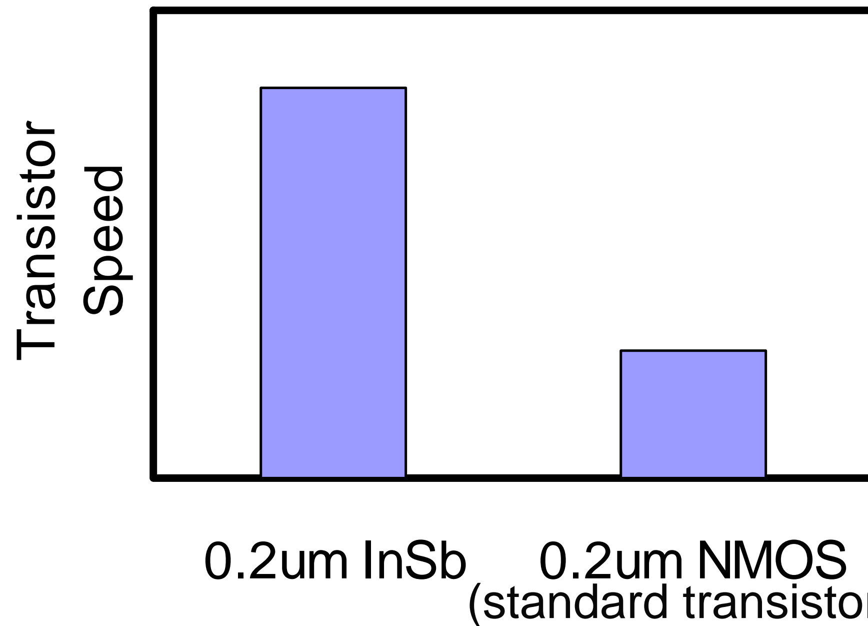
	Compound Semiconductors		
Si	GaAs	InAs	InSb
1	8	33	50

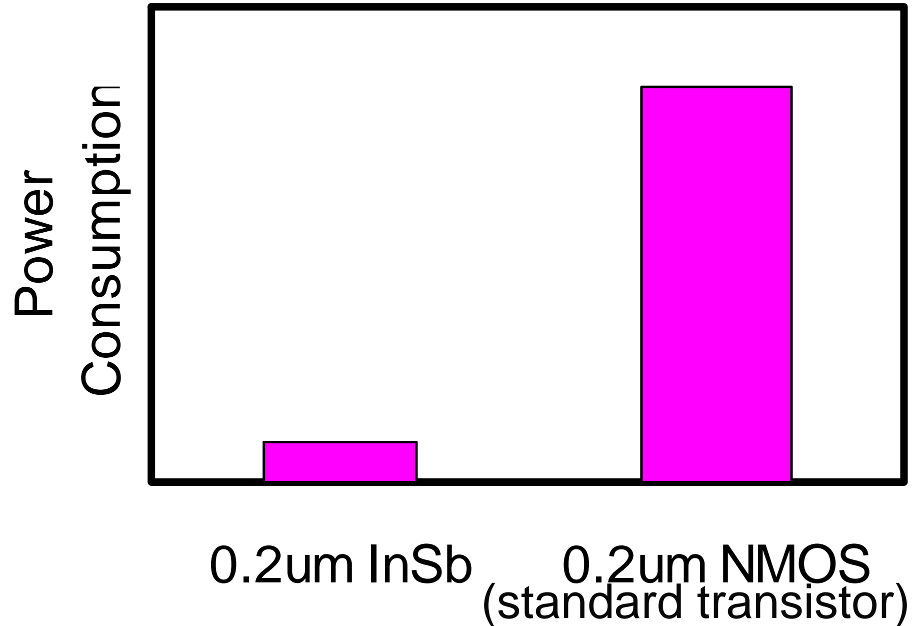
Compound semiconductors have higher electron mobility than Si; InSb (indium antimonide) is highest of all



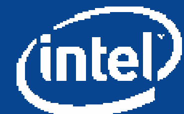
Looking ahead

CMOS to continue for 15-20 years or more; Moore's Law could be extended indefinitely via new architectures, heterogeneous integration, 3D





III/V is a 2015 Transistor option
- **3x faster or 10x lower power**
- **Integration with silicon key**



IEDM 2004

Depletion and Enhancement Mode

Gate

Source

Drain

$Al_xIn_{1-x}Sb$ barrier

Semi-insulating GaAs substrate for epitaxial growth

InSb QW

Recessed Gate

Etch Stop Layer

Source

Drain

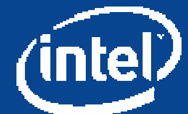
$Al_xIn_{1-x}Sb$ barrier

Semi-insulating GaAs substrate for epitaxial growth

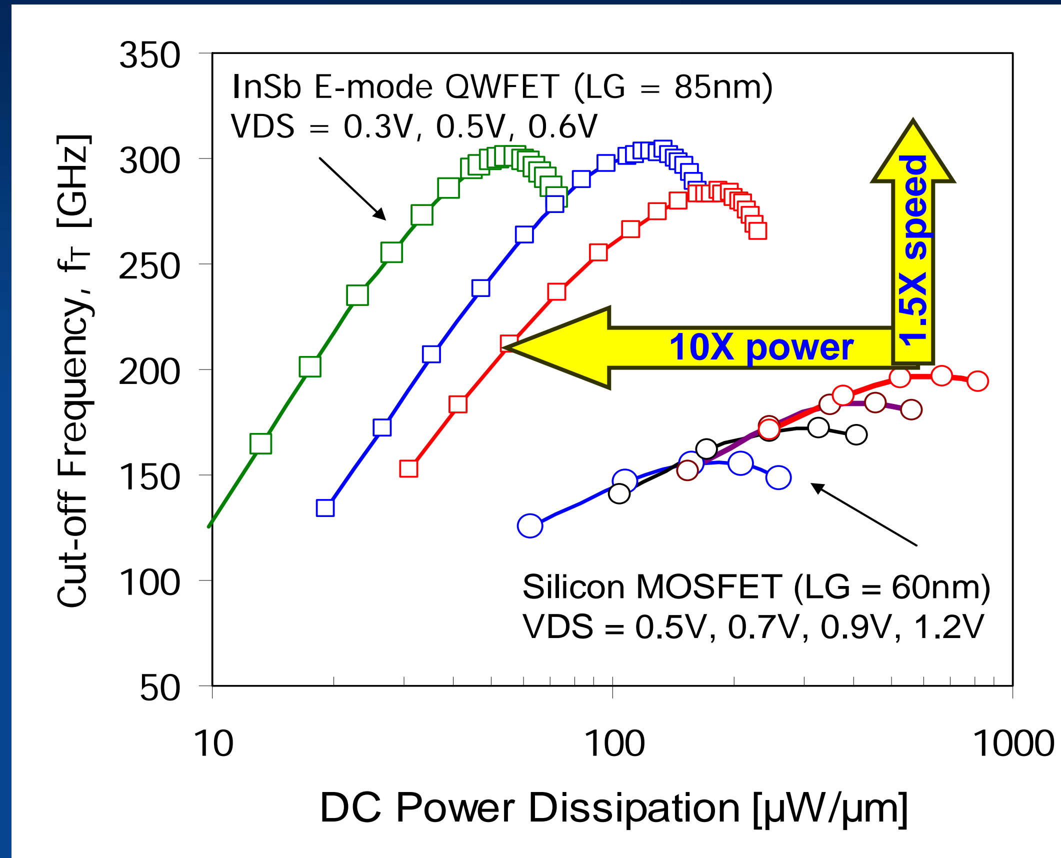
Depletion mode (Normally ON)

Enhancement mode (Normally OFF)

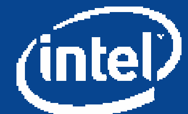
A novel gate recess process is used to fabricate enhancement mode InSb QWFETs



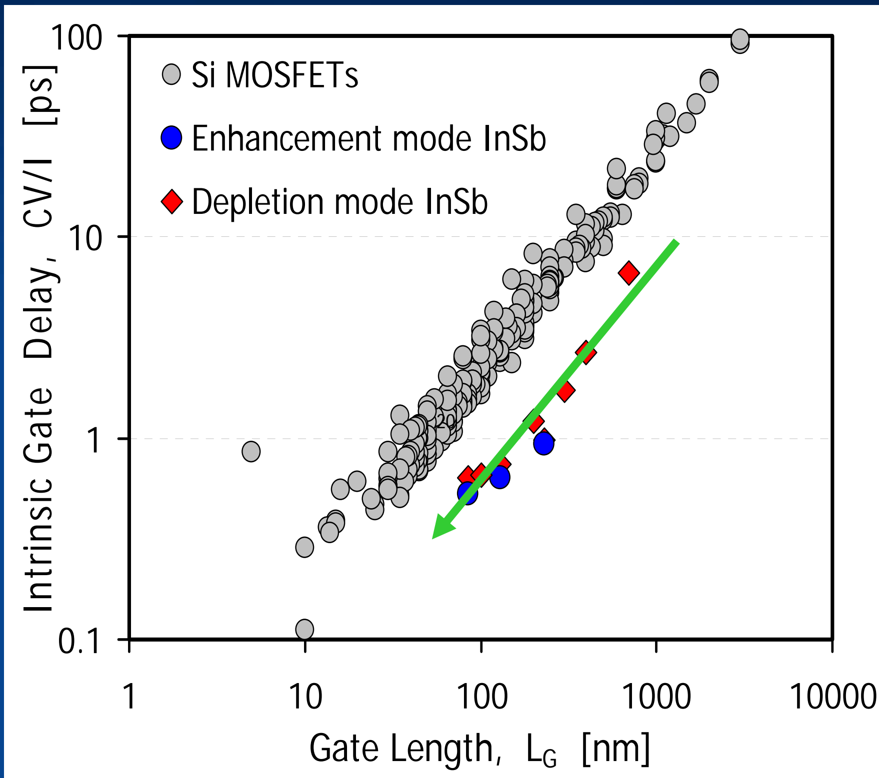
Speed, Power, Performance

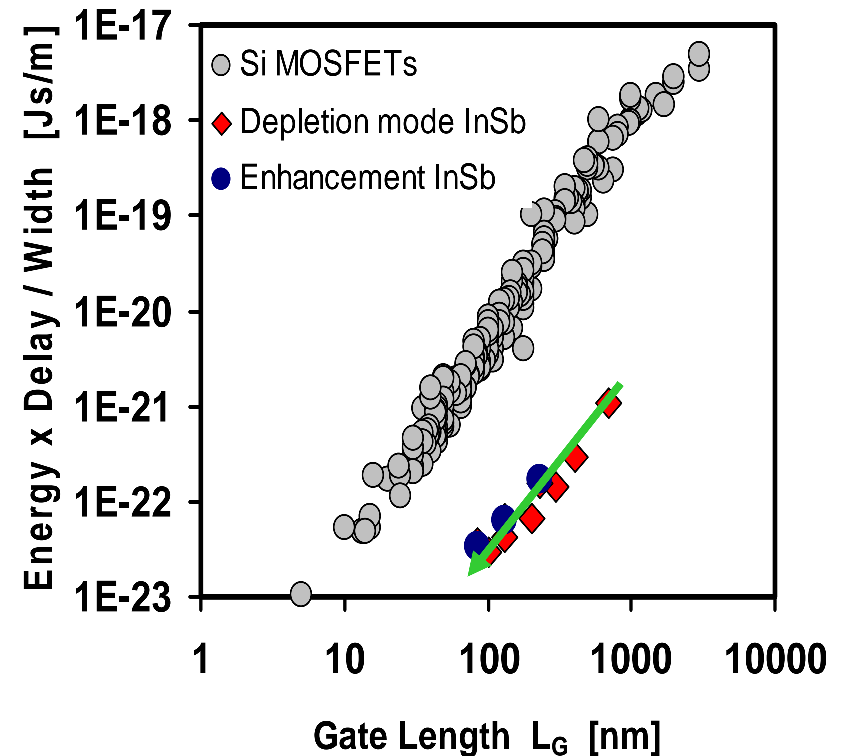


InSb QWFETs show > 10x reduction in active power dissipation compared to Si MOSFETs



Benchmarking InSb QWFETs

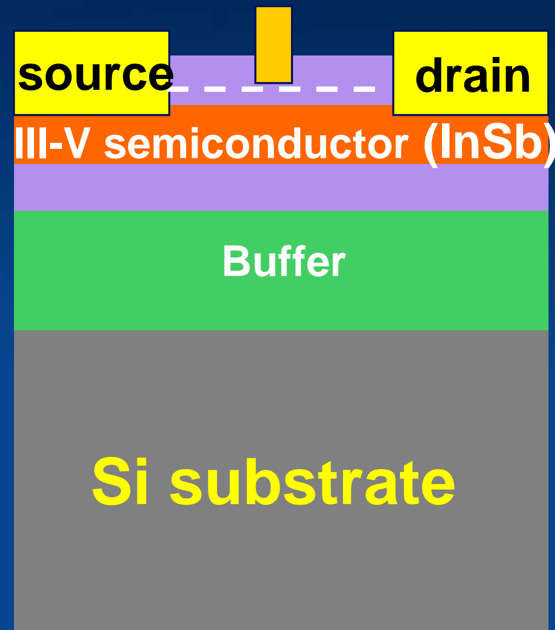




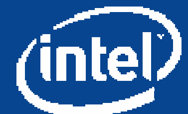
InSb transistors show significant improvement in intrinsic gate delay and energy-delay product over Si MOSFETs at equivalent gate length

intel

Integration on Si Platform



Current research on incorporation of new transistor onto the existing Si platform



Innovation-Enabled Technology Pipeline

90 nm
2003

65 nm
2005

45 nm
2007

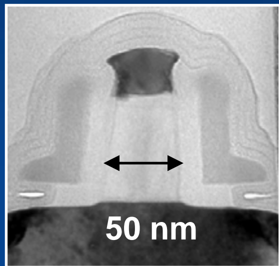
32 nm
2009

2011+

Manufacturing

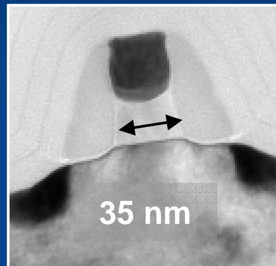
Development

Research



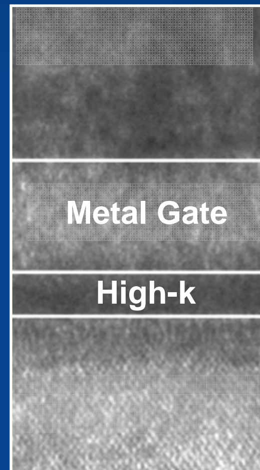
SiGe S/D

Strained Silicon

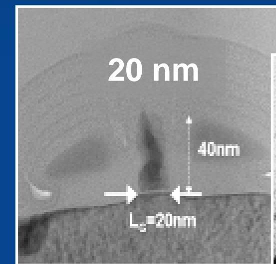


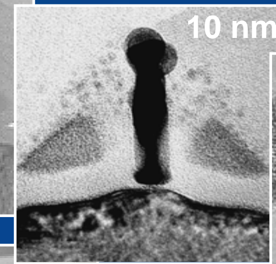
SiGe S/D

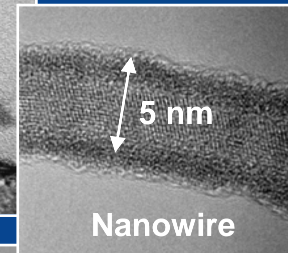
2nd generation Strained Silicon

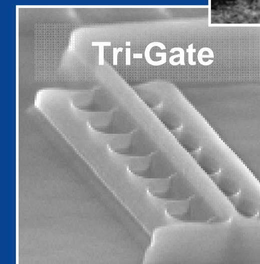


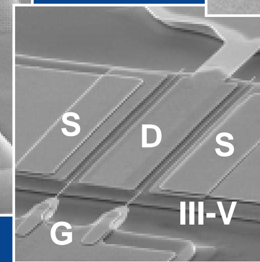
High-k
Metal gate



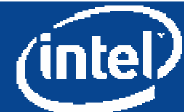






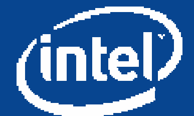


Future options subject to change



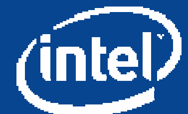
Moore's Law =

Transistor Budget +
Lowest Power and Lowest Cost



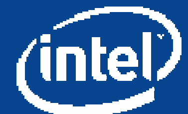
Outline

- Intel's Silicon R&D Pipeline
- From Geometrical Scaling to Equivalent Scaling
- DFM
- Getting the Lead out
- Future Technology Options
- Summary



Summary

- Intel's R&D pipeline will sustain Moore's Law for the foreseeable future
- 45 nm high-k + metal gate is the most significant innovation in transistor technology in 40 years
- Intel has removed 100 percent of the lead across its entire portfolio of packages in its 45nm family of microprocessors
  - … 65nm chipsets will transition to 100% Lead-free in 2008
- Intel continues its unwavering commitment to support R&D for future technologies and to deliver the benefits of Moore's Law to our customers



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